HIGH PERFORMANCE RF AND BASEBAND BUILDING BLOCKS FOR WIRELESS RECEIVERS

A Dissertation

by

FARAMARZ BAHMANI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2006

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Jose Silva-Martinez
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ABSTRACT

High Performance RF and Baseband Building Blocks for

Wireless Receivers. (May 2006)

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Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Because of the unique architecture of wireless receivers, a designer must understand both the high frequency aspects as well as the low-frequency analog considerations for different building blocks of the receiver. The primary goal of this research work is to explore techniques for implementing high performance RF and baseband building blocks for wireless applications. Several novel techniques to improve the performance of analog building blocks are presented. An enhanced technique to couple two LC resonators is presented which does not degrade the loaded quality factor of the resonators which results in an increased dynamic range.

A novel technique to automatically tune the quality factor of LC resonators is presented. The proposed scheme is stable and fast and allows programming both the quality factor and amplitude response of the LC filter.

To keep the oscillation amplitude of LC VCOs constant and thus achieving a minimum phase noise and a reliable startup, a stable amplitude control loop is presented. The proposed scheme has been also used in a master-slave quality factor tuning of LC filters.

An efficient and low-cost architecture for a 3.1GHz-10.6GHz ultra-wide band frequency synthesizer is presented. The proposed scheme is capable of generating 14 carrier frequencies.

A novel pseudo-differential transconductance amplifier is presented. The proposed scheme takes advantage of the second-order harmonic available at the output current of pseudo-differential structure to cancel the third-order harmonic distortion.

A novel nonlinear function is proposed which inherently removes the third and the fifth order harmonics at its output signal. The proposed nonlinear block is used in a bandpass-based oscillator to generate a highly linear sinusoidal output.

Finally, a linearized BiCMOS transconductance amplifier is presented. This transconductance is used to build a third-order linear phase low pass filter with a cut-off frequency of 264MHz for an ultra-wide band receiver.

DEDICATION

To my beloved Father and Mother,

To my Brothers and Sisters,

For all their love and support.

ACKNOWLEDGEMENTS

I am deeply grateful to my advisor, Prof. Edgar Sánchez-Sinencio, for his guidance and support throughout the course of this research work. Professor Sánchez-Sinencio showed me a great insight into the playful analog design, and helped me to develop a nonjudgmental, optimistic, and meticulous approach towards research and life. I am also grateful for his criticism, patience, and encouragement.

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Special thanks to my parents, my brothers and sisters who have been always there for me. Without their love and support I would never have been able to accomplish what I have now. Their love was the strength I needed to go through to this challenge. Otherwise, it would have been unbearable. They deserve the most.

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CHAPTER I

INTRODUCTION

The radio frequency (RF) and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones, cable modems, and RF identification (RFID) tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. In the field of communication circuit design, the realization of the complete integration of RF transceivers and digital signal processing blocks onto a single integrated circuit (IC) is a logical area in which to develop system-on-chip (SoC) solutions. Presently, with the growing demand for multi-functional wireless consumer devices, the need for full integration of the RF and logic circuits in wireless communications systems is becoming increasingly evident. Meanwhile, the lower cost and faster advance of CMOS processes has motivated extensive efforts in designing RF CMOS circuits. CMOS technologies exhibit properties and limitations that directly impact the design of a receiver from the architecture level to the device level and from the RF front end to the baseband processor.

Complexity, cost, power dissipation, and the number of external components have been the primary criteria in selecting receiver architecture. As IC technologies evolve, however, the relative importance of each of these criteria changes, allowing approaches that once seemed impractical to return as plausible solutions.

RF architectures impose severe requirements upon the performance of their constituent circuits. The very small signal amplitude received by the antenna in the

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This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

presence of large interferers mandates both careful allocation of noise and linearity to various stages and sufficient suppression of spurious components generated in the frequency synthesizers and the power amplifier. As with most analog systems, RF circuits suffer from tradeoffs among various parameters such as noise, gain, linearity, frequency and supply voltage.

1.1. Motivation

Because of the unique architecture of wireless receivers, a designer must understand both the high frequency aspects as well as the low-frequency analog considerations for different building blocks of the receiver. The primary goal of this research work is to explore techniques for implementing high performance RF and baseband building blocks for wireless applications. The objectives of this work can be summarized as

- To investigate the feasibility of employing on-chip LC bandpass filters in order to eliminate the bulky ceramic, crystal, or pre-select filters used in receiver front ends. This aims to obtain a fully integrated receiver, thereby reducing the power consumption, area, cost, and matching issues. However, due to implementation of passive elements, mainly inductors, the quality factor of this kind of filters are subject to variations. Implementation of the quality factor tuning schemes for LC filters is also part of the objective of this research work.
- To devise an efficient ultra-wide band frequency synthesizer to downconvert the entire 7.5GHz frequency range of the UWB signal.

- To develop new circuit techniques to make feasible the on-chip integration of Transconductance-C (Gm-C) baseband low pass filters. This research pushes outward the main limitations of Gm-C filters, which are dynamic range, frequency response stability and high frequency performance. The Gm-C filter topology was chosen for its high-speed, low power consumption and tenability advantages. The dynamic range of the integrated Gm-C filter is increased on a circuit level by introducing a new linearized transconductance circuit. A highly linearized oscillator, to be used in the frequency tuning of the Gm-C filters, is also presented.

Fig. 1.1 visualizes the contributions of this research work on different parts of a wireless receiver chain.

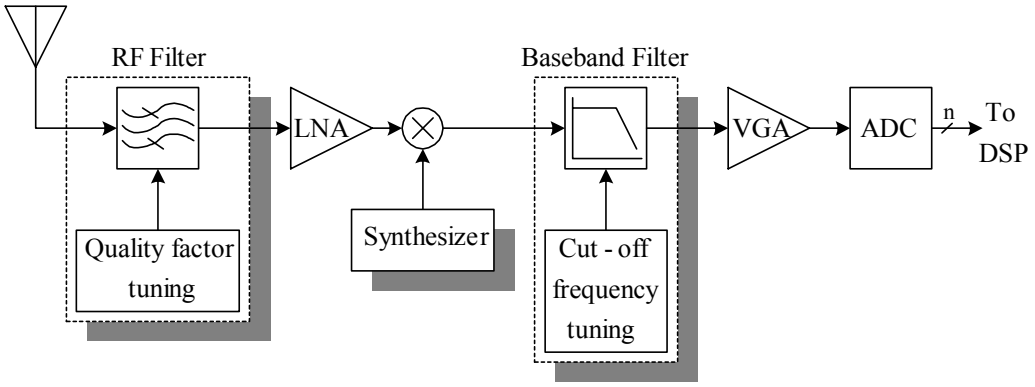


Fig. 1.1 Contributions of this research work in a wireless receiver.

1. 2. Dissertation Organization

Chapter II presents an overview of some commonly implemented wireless receiver topologies along with a qualitative analysis of the filtering requirements for each

type of system. Some inherent advantages and disadvantages for each type are also briefly covered. Specifications that define the operational characteristics of wireless receivers are also examined and the requirements of some current wireless standards are analyzed to highlight performance parameters required for integrated filters.

Chapter III discusses the issue of RF bandpass filter prototype selection, and explains why a forth order mutual electric coupled-resonator LC filter is chosen as the prototype in this work. The building blocks that make up this filter are presented along with the overall circuit architectures.

Chapter IV presents a novel feedback loop which can achieve accurate voltage controlled oscillator (VCO) loss- control and robust amplitude regulation. For GHz-range coupled-resonator LC bandpass filters, one popular approach to tune the quality factor of each resonator uses a VCO to set the time constant of the tracking resonator. Amplitude regulation is needed in this case to reduce distortion caused by the non-linearity of the active devices in the VCO so that the tuning error can be kept low.

Due to process tolerances and temperature variations the quality factor of LC resonator filters can change. In Chapter V a new technique for quality factor tuning of second order LC filters is presented. The tuning accuracy and stability of the proposed technique are analyzed. The design of the tuning system and its performance are also discussed.

Chapter VI presents the design of transconductor circuits that can be used to build tunable Gm-C filters for wireless receivers. There is always a trade-off between the linearity, the bandwidth and the tuning range of the Gm circuits. A pseudo-differential

(PD) transconductance is presented. When implemented in a unity gain voltage buffer, the proposed transconductance can minimize the overall linearity of Gm-C filters.

In Chapter VII a highly linearized oscillator is presented which can be used as the reference for center/cut-off frequency tuning of baseband filters. A multilevel hard limiter (MHL) is proposed which inherently removes the most critical odd harmonics from the frequency spectrum of the output signal. Detailed analysis of the proposed MHL block along with the measurement results is presented.

Finally, In Chapter VIII two building blocks of a UWB receiver are studied. A linearized transconductance suitable for high frequency implementation of a Gm-C low pass filter is proposed. Furthermore, an efficient architecture for the UWB frequency synthesizer is presented.

1. 3. Major Contributions of This Dissertation

The contributions of this dissertation can be divided in two categories of RF frequencies and Baseband Frequencies. Two main building blocks of primary concern in the RF frequency range are LC filters and LC VCOs. One of the challenges associated with the integrated LC filters is their quality factor tuning. In this dissertation two techniques to automatically tune the quality factor of this kind of filters are proposed. Furthermore, a stable and fast amplitude control loop to automatically regulate the oscillation amplitude of integrated LC VCOs is proposed. Moreover, an efficient and low-cost architecture for ultra-wide band receivers is proposed which covers the entire frequency range of 3.1GHz to 10.6GHz.

In the baseband frequencies, a novel pseudo-differential transconductance amplifier is proposed. The proposed transconductance is also used to build a bandpass based oscillator. A novel nonlinear transfer function is proposed which inherently removes the 3^{rd} and 5^{th} order harmonics form the frequency spectrum of its output signal. A new BiCMOS transconductance is proposed to implement a 264MHz low pass filter used in the ultra-wide band receivers.

CHAPTER II

RECEIVER ARCHITECTURES

2.1. Introduction

The major challenge in RF transceiver design is to utilize, more effectively, the continuously scaling technologies in order to improve the integration level of RF transceivers. This should result in further improvement in power dissipation, form factor, and cost [1]-[3]. A wireless transceiver consists of two main parts, an analog front end which performs frequency upconversion/downconversion of the modulated information signal, and a digital back-end where the actual modulation/demodulation of the signal takes place, through extensive use of digital signal processing techniques. Although the continued downscaling has resulted in better integration and lower power consumption in the transceiver back-end, this is not the case for the front-end, where integration level and lower power consumption is more related to the physical limitations of the transceiver topology rather than the used technology. Thus, it is this analog transceiver front-end, the part which represents the interface between the antenna and the digital signal processing back-end, which is the main bottleneck for advancement in RF transceiver design [3].

Wireless receiver design, and the need for creating a compact, power efficient system-on-a-chip requires that both the digital and analog/RF part circuitry to be implemented on the same chip. CMOS has proved to be a strong contender in this field, with the larger amount of digital circuitry benefiting from a higher transistor density and therefore smaller size and lower fabrication cost [2]. This explain the greater tendency, in

recently published RF CMOS work, towards single-chip transceiver realization than seen in complementary IC's for cellular and cordless telephones developed in industry [2].

One of the key components of portable devices used in wireless communication systems is the receiver, which senses an incoming signal and extracts the desired information. Since the Federal Communications Commission (FCC) regulates the frequency at which signals can be translated, the incoming signal is typically centered at a frequency which is much larger than the bandwidth of the desired signal.

In a real wireless transmission environment, the received signal is almost always far from ideal. The signal which reaches the receiver can be very weak because of attenuation by objects which obstruct the transmission path between the transmitter and receiver or simply because of the loss due to spatial separation between the transmitter and receiver. In addition, the received signal can include unwanted signals along with the desired one. These unwanted signals, or interfaces, can be significantly stronger than the desired signal.

Due to the limited amount of attenuation achievable by practical filter designs as well as the noise and distortion introduced by circuits used to implement the RF front-end, the design of a highly-integrated, low-power becomes increasingly challenging when the received signal consists of a very weak desired signal in the presence of strong adjacent interferes.

This chapter provides an overview of various receiver architectures, starting with the heterodyne architecture, which, unfortunately, is not very amenable to high levels of integration, and followed by an overview of a few other receiver architectures which are more conductive to single-chip implementation.

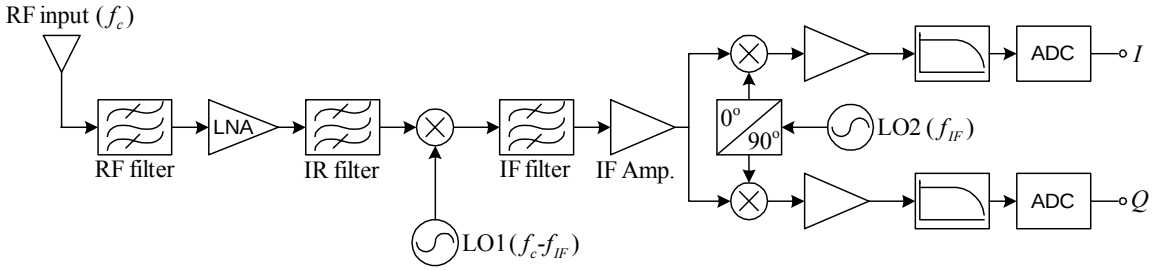


Fig. 2.1 Heterodyne architecture block diagram.

2.2. Heterodyne Architectures

The heterodyne receiver operates by down-converting incoming RF signals to baseband in multiple frequency steps. The heterodyne architecture is commonly used in current commercial receiver implementations because of its excellent sensitivity and selectivity performance [1].

A block diagram of the heterodyne architecture with two frequency translation steps is illustrated in Fig. 2.1. In this architecture, the signal received at the antenna first passes through an RF filter before being amplified by a low noise amplifier (LNA). The signal is then filtered by an image reject (IR) filter before being frequency translated to an intermediate frequency (IF) by the first local oscillator (LO). At the intermediate frequency the signal is further filtered and amplified before being frequency translated to baseband along parallel in-phase (I) and quadrature (Q) signal paths by the second LO. At baseband, the signal is further amplified and filtered before being converted to a digital signal by the analog-to-digital converter (ADC).

2.2.1. Image Problem

As detailed in Fig. 2.1, there are three different filter blocks normally incorporated into this type of receiver. Bandpass filtering is required for the band-select RF and channel select IF filters, while the image reject filtering is often achieved with a bandstop notch circuit. Operationally, different channels can be selected by changing the frequency of the local oscillator (LO) that heterodynes with the RF signal in the mixer. The selection of the intermediate frequency in this architecture is directly related to the image problem. In Fig. 2.2, the desired signal centered at the carrier frequency f_c is frequency translated to the intermediate frequency f_{IF} by an LO located at the frequency f_c-f_{IF}. However, the signal centered at the image frequency f_c-2f_{IF} is also frequency translated to f_{IF}. Since the image signal can be much stronger than the desired signal, the image signal must be sufficiently attenuated before frequency translation.

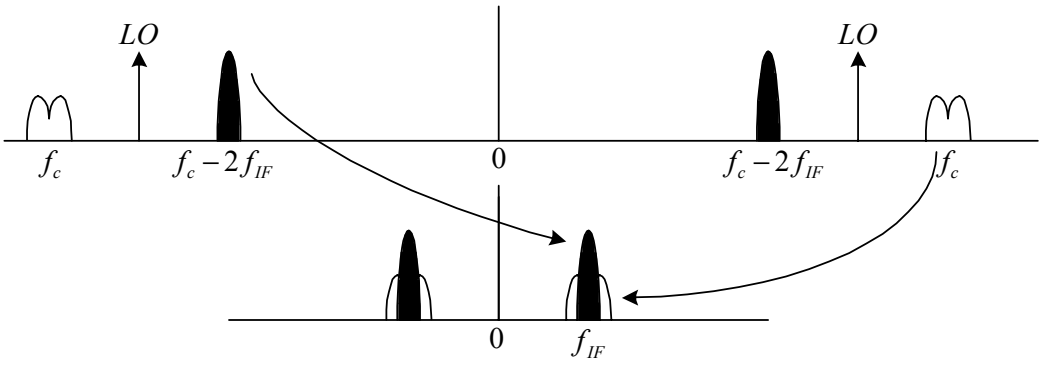


Fig. 2.2 The image problem.

The choice of f_{IF} depends on the characteristics of practical filter implementations. For a typical ceramic filter, the amount of attenuation increases at frequencies further away from the center frequency f_0. Consequently, in order to achieve a large amount of image signal attenuation, it is preferable to select a high intermediate frequency so that

the image signal is far away from the center frequency of the filter. However, a high intermediate frequency also increases the design challenges in the IF filtering and amplification circuits. Therefore, the choice of f_{IF} must be based on following tradeoffs:

- A high intermediate frequency results in maximum image signal attenuation from the IR filter, while
- A low intermediate frequency results in relaxed IF filtering and amplification requirements.

Since small physical size and low power consumption are two critical design goals in the design of portable units, the heterodyne architecture is inadequate and other receiver architectures which are more amendable to highly-integrated, low-power implementations must be considered for future wireless communications systems. These architectures include:

- The direct-conversion architecture
- The image-reject architecture
- The low-IF architecture

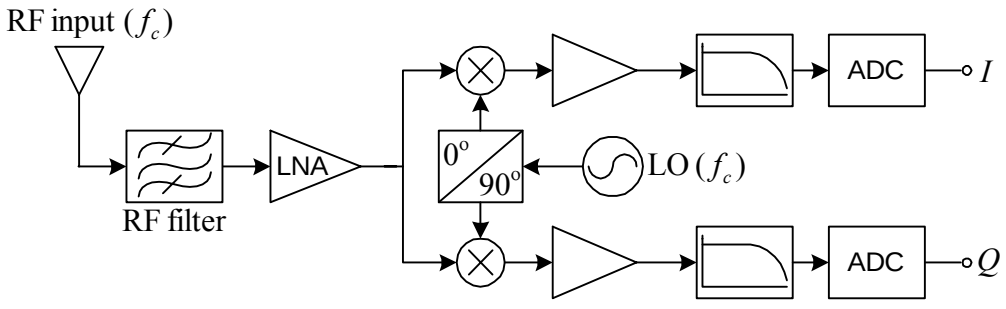


Fig. 2.3 Direct-conversion architecture block diagram.

2.3. Direct-Conversion Architecture

The direct-conversion architecture, also known as zero-IF or homodyne architecture, translates the incoming RF signal directly to baseband frequency. The block diagram of this architecture is shown in Fig. 2.3 [3]. The direct-conversion architecture offers two main advantages over the heterodyne receiver. First, the problem of image rejection is nullified because the IF frequency for this type of receiver is zero. Second, the IF filter and amplifier stages are replaced by low-frequency counterparts which are easily integrated on-chip. However, two practical considerations have limited the use of the direct-conversion architecture: DC offsets and flicker noise. DC offsets are problematic for two reasons. First, DC offsets can saturate the baseband circuits. Second, even if the baseband circuits do not saturate, DC offsets, if uncorrected, degrade the bit-error rate (BER) performance of the system.

There are three primary sources of DC offsets: LO self-mixing, even-order distortion, and baseband circuit mismatch. Finite isolation from the LO port to the RF port of the mixer leads to DC offset at the mixer output that results from LO self-mixing. LO leakage back to the antenna can also create interference output signals that can adversely affect other nearby users. Also, because of the limited gain in zero-IF receivers provided by the RF amplifier and mixer, the downconverted signal is very sensitive to noise. This is particularly problematic in CMOS technology, which suffers from a large flicker noise component generated by MOS transistors at low frequencies. One alternative to the zero-IF problem is the implementation of a ‘low-IF’ frequency plan.

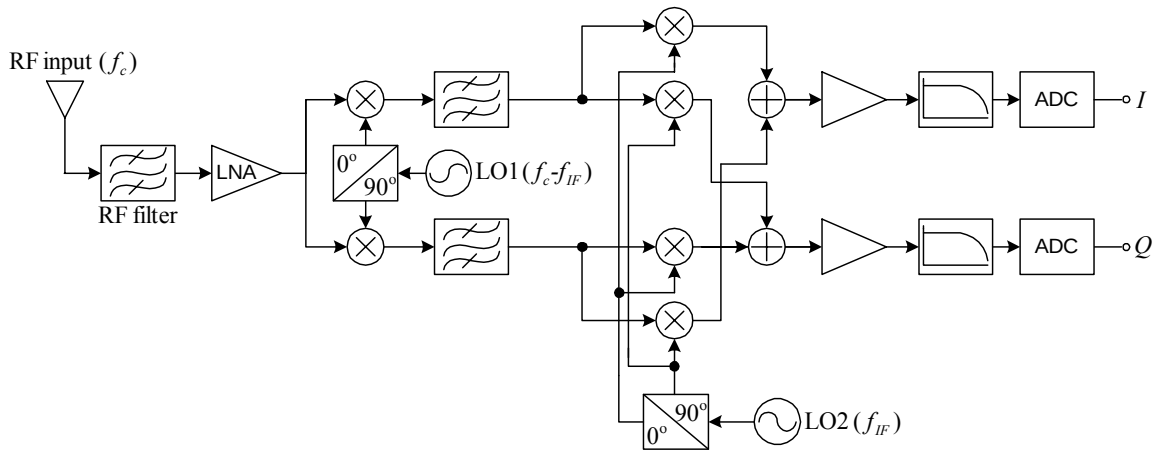


Fig. 2.4 Image-reject (Weaver) architecture block diagram.

2.4. Image-Reject Architecture

In the heterodyne architecture, the image problem arises from the use of a real sinusoidal LO signal to frequency translate the input signal to an intermediate frequency. More specifically, the Fourier transform of a real sinusoidal LO signal, $\cos(2\pi f_{LO1}t)$, consists of a negative frequency component at $-f_{LO1}$ can a positive frequency component at $+f_{LO1}$:

$$\cos(2\pi f_{LO1}t) \leftrightarrow \frac{1}{2}[\delta(f - f_{LO1}) + \delta(f + f_{LO1})] \tag{2.1}$$

During the frequency translation process, the negative frequency component of the LO signal downconverts the positive frequency component of the desired signal to f_{IF}, while the positive frequency component of the LO signal downconverts the negative frequency component of the image signal also to f_{IF}.

The process description of the mechanism behind the image problem suggests a potential solution: use a complex sinusoidal LO signal to downconvert the input signal to

the intermediate frequency. The Fourier transform of a complex sinusoidal LO signal, $e^{-2\pi f_{LO1}t}$, consists of only a negative frequency component at $-f_{LO1}$:

$$e^{-2\pi f_{LO1}t} \leftrightarrow \delta(f + f_{LO1}). \tag{2.2}$$

When the input signal is multiplied by the LO signal, only the positive frequency components of the input signal are translated to the intermediate frequency. The complex mixing function described above can be implemented using the image-reject mixer. This complex mixing function serves as the basis for the image-reject receiver architecture, also called the Weaver architecture [4]-[7], illustrated in Fig. 2.4.

Unfortunately, in practice the amount of image rejection achievable by implementations based on this architecture is limited by the gain mismatch between the different paths of the receiver as well as by the quadrature phase mismatch between the I and Q signals in the two local oscillators.

The Weaver architecture is also susceptible to DC offsets and flicker noise. Self-mixing due to the second LO can occur during downconversion of the received signal from the intermediate frequency to baseband. And similar to the direct-conversion architecture, even-order distortion and baseband circuit mismatch can also result in DC offset in the Weaver architecture. In addition, since the desired signal is frequency translated to baseband prior to analog-to-digital conversion, flicker noise from the baseband analog amplifiers and filters can potentially corrupt the desired signal.

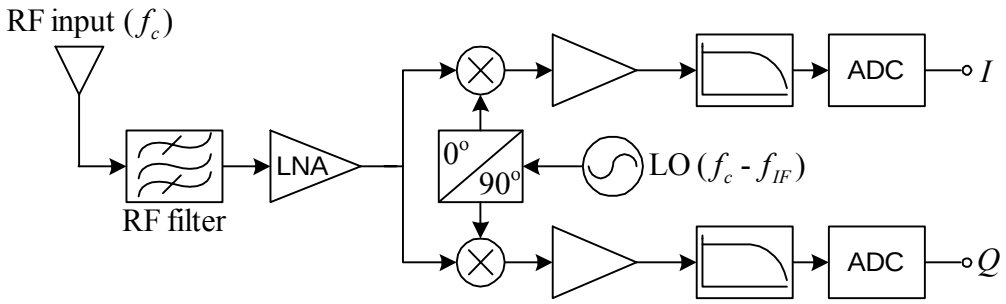


Fig. 2.5 Low-IF architecture block diagram.

2.5. Low-IF Architecture

One way to avoid the problems associated with DC offsets and flicker noise is to perform analog-to-digital conversion at the intermediate frequency. By using digital circuit techniques to downconvert the desired signal from the intermediate frequency to baseband as well as to perform the subsequent amplification and filtering, impairments associated with analog implementation techniques can be avoided. However, due to conversion speed limitations in analog-to-digital converters, this approach is limited to low intermediate frequencies, and consequently, a third receiver architecture which is based on this technique is called the low-IF architecture [8]-[10]. Fig. 2.5 shows the block diagram of a low-IF architecture.

Since the received signal is downconverted to an intermediate frequency, the low-IF architecture must also content with the image problem. Consequently, the same image-reject mixing technique used in the Weaver architecture must also be used in the low-IF architecture. This architecture is limited to applications which have relaxed image-rejection requirements at small frequency offsets from the desired signal.

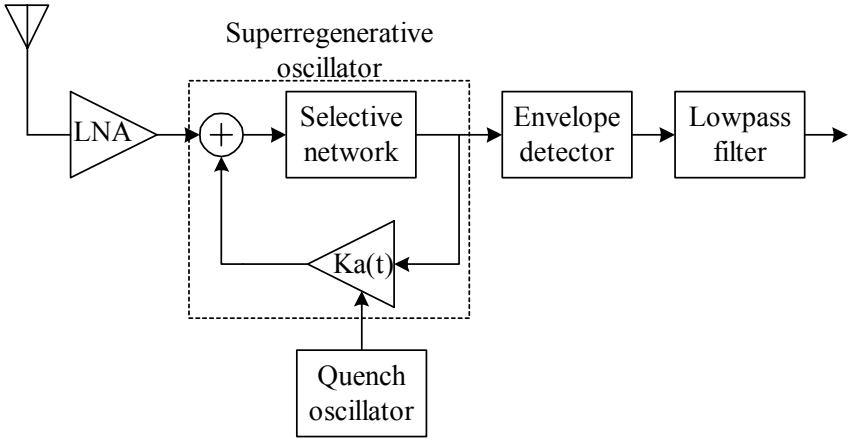


Fig. 2.6 Superregenerative architecture block diagram.

2.6. Superregenerative Architecture

The detailed block diagram of the superregenerative receiver is shown in Fig. 2.6 [11]-[12]. The core of the diagram is the superregenerative oscillator. It is an RF oscillator that is controlled by a low-frequency quench oscillator, which causes the RF oscillations to rise and die out repeatedly. The RF oscillator can be modeled as a frequency-selective network fed back through a variable-gain amplifier. This gain is modified by the quench oscillator, making the closed-loop system alternatively unstable and stable. The primary function of the low-noise amplifier (LNA) is to isolate the antenna from the oscillator. Otherwise, the relatively large amplitude RF pulses present in the oscillator will generate an appreciable radiated power that can cause interference in other systems.

Currently, the major application of the Superregenerative receiver is in short-distance RF links, in which reduced cost and low power consumption are required. Among these applications are remote control systems (such as garage door openers, robotics, and model ships and airplanes), short-distance telemetry, and wireless security.

2.7. Receiver Architecture Selection Guidelines

System level specifications, such as modulation schemes, signal bandwidth, and interference rejection requirements, strongly influence the choice of receiver architecture. The advantages and disadvantages of the heterodyne architecture, direct-conversion architecture, the image-reject architecture, and the low-IF architecture are summarized in Table 2-1.

Table 2-1 Receiver architecture performance summary

	Advantage	Disadvantage
Heterodyne	Excellent sensitivity and selectivity performance.	Large number of discrete components.
Direct conversion	Minimal number of RF components	DC offsets and flicker noise
Image reject	Facilitates integration of low phase noise LO.	Large number of RF components. DC offsets and flicker noise. Image-rejection is limited by gain and phase mismatches.
Low IF	Minimal number of RF components. Avoids problems associated with DC offsets and flicker noise	ADC sampling frequency must be at least $f_{IF}+f_{sig}$ Image rejection is limited by gain and phase mismatches

2.8. Short-Range Wireless Communication Standards

Many standards exist today for connecting various devices. At the same time, every device has to support more than one standard to make it inter-operable between different devices. These standards deliver opportunities for rapid ad hoc connections, and the possibility of automatic, unconscious, connections between devices. They will virtually eliminate the need to purchase additional or proprietary cabling to connect individual devices, thus creating the possibility of using mobile data in a variety of applications. Wired LANs have been very successful in the last few years and now with the help of these wireless connectivity technologies, wireless LANs (WLAN) have started emerging as a much more powerful and flexible alternatives to the wired LANs.

There are many such technologies/standards and notable among them are Bluetooth, IEEE 802.11.b and ultra wide band (UWB). These technologies compete in certain fronts and are complementary in other areas.

2.8.1. Bluetooth

Bluetooth is a high-speed, low-power microwave wireless link technology, designed to connect phones, laptops, PDAs and other portable equipment together with little or no work by the user [13]. Unlike infra-red, Bluetooth does not require line-of-sight positioning of connected units. The technology uses modifications of existing wireless LAN techniques but is most notable for its small size and low cost. Whenever any Bluetooth-enabled devices come within range of each other, they instantly transfer address information and establish small networks between each other, without the user

being involved. Bluetooth technology operates in the 2.56 GHz ISM band and uses FHSS (frequency hop spread spectrum) in a 10m to 100m range.

2.8.2. 802.11 (“Wi-Fi”)

Wi-Fi's popularity really took off with the growth of high-speed broadband Internet access in the home. It was and remains the easiest way to share a broadband link between several computers spread over a home. The growth of hotspots, free and fee-based public access points, have added to Wi-Fi's popularity. The latest variant was 802.11g. This Wi-Fi technology, like 802.11a, uses a more advanced form of modulation called orthogonal frequency-division multiplexing (OFDM), but enables it to be used in the 2.4 GHz band. 802.11g can achieve speeds of up to 54 Mbps [14].

Today 802.11 is rapidly proliferating all over the planet. Nonetheless, it still faces a number of technological challenges. A major one is range. The farthest a device can currently stray and still receive an adequate signal from an 802.11 access point is about 300 feet and that's if there are no major walls or other substantial physical obstructions. Other major challenges 802.11 faces include how to improve data throughput speeds, enhance security, and improve quality of service.

2.8.3. Ultra-Wideband (UWB)

Ultra-Wideband (UWB) technology brings the convenience and mobility of wireless communications to high-speed interconnects in devices throughout the digital home and office. Designed for short-range, wireless personal area networks (WPANs), UWB is the leading technology for freeing people from wires, enabling wireless

connection of multiple devices for transmission of video, audio and other high-bandwidth data. UWB, short-range radio technology, complements other longer range radio technologies such as Wi-Fi, WiMAX and cellular wide area communications. It is used to relay data from a host device to other devices in the immediate area (up to 10 meters, or 30 feet).

Specifically, UWB is defined as any radio technology having a spectrum that occupies a bandwidth greater than 20 percent of the center frequency, or a bandwidth of at least 500 MHz. UWB systems use Orthogonal Frequency Division Multiplexing (OFDM) to occupy these extremely wide bandwidths. UWB's combination of broader spectrum and lower power improves speed and reduces interference with other wireless spectra. In the United States, the FCC has mandated that UWB radio transmissions can legally operate in the range from 3.1 GHz up to 10.6 GHz, at a limited transmit power of -41dBm/MHz [15]. Consequently, UWB provides dramatic channel capacity at short range that limits interference.

To illustrate the range of frequencies and IF bandwidths in current receiver designs Table 2-2 shows the allocation information pertaining to several commercially available wireless devices. Additionally, commercially available SAW filters are routinely incorporated for intermediate frequency (IF) discrimination in receiver architectures for cellular telephone standards, with these IF frequencies ranging from 85 MHz to 400 MHz [16]. Although required IF frequencies vary widely depending on the receiver type and frequency plan, this information provides a general idea of current commercial IF frequency requirements. Dynamic range (DR) requirements associated with some wireless standards for cellular telephone, WLAN, and PAN are presented in

Table 2-2 for reference. These specifications are important in determining the practicality of implementing front-end integrated RF CMOS filters as these filters have finite maximum input signals and minimum noise characteristics which fundamentally limit the dynamic range achievable in the overall receiver.

Table 2-2. Frequency allocations for wireless devices

Device	Frequency allocation (MHz)	Channel BW (MHz)	Receiver sensitivity	RF Power
WLAN 802.11.a	5725-5850	54	-82dBm to -65dBm	50mW;250mW; 1W
WLAN 802.11.b, (Wi-Fi)	2400-2484	5.5-11	-76dBm	30dBm
Bluetooth (PAN)	2400-2484	1.0	-70dBm	0dBm; 20dBm
UWB	3100-10600	500	-	-41.3dBm/MHz
ZIGBEE	868/915MHz 2.4GHz	5	-88dBm and -92dBm	0.5mW to 10mW

Table 2-3 Wireless standard dynamic range requirements.

Receiver Type	Dynamic Range (dB)
CDMA Cellular	79 (-104 to -25 dBm)
GSM Cellular	87 (-102 to -15 dBm)
Bluetooth PAN	50 (-70 to -20 dBm)

With the rapid advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. Hence, the cost and size will be further reduced. Second, to further improve transceiver integration, the LC tanks associated with the VCO's are required to be on board.

The recent advent of wireless communications has created a need for high-selectivity, integrated, continuous-time filters in the GHz range, in which inductorless active filters have encountered serious difficulties. Bandpass filters that utilize LC tank circuits have the advantage of being less sensitive to parasitic capacitance attributable to active device structures or on-chip signal routing. This allows for the implementation of filter circuits at higher operational frequencies, as these parasitic capacitors can actually be absorbed into the total reactance required for the design frequency. Even though LC-based filters offer higher dynamic range with respect to Gm-C filters [11], they suffer from the large silicon area occupied by the inductors. Alternately, filters based on Gm-C structures are fundamentally affected by the presence of these parasitics, where the inherent excessive capacitance values tend to increase the overall capacitance at a particular node, having the effect of reducing the highest achievable operational frequency. In comparison with the LC-based filters, the Gm-C filters occupy less silicon area but demand more power consumption. Furthermore, due to the contribution of noise associated with the active elements the dynamic range of this kind of filters are usually low.

The main difficulties in integrating RF filters on-chip are:

1- High dynamic range requirement. An inductorless active filter can realize a high quality-factor bandpass transfer function, but cannot deliver reasonable dynamic range performance at gigahertz frequencies with low power. On the other hand, a pure passive LC bandpass filter can have a large dynamic range and requires no power supply, but needs high quality factor on-chip inductors. An active LC filter is a compromise between the above two types of filters. It uses on-chip inductors, and compensates the losses in the on-chip reactive components by active means. With the aid of active components, an active LC filter can realize a high quality factor bandpass transfer function with little or no insertion loss or even with gain in the passband. Although at present the dynamic range of active LC filters is still not sufficient for them to be included in wireless receivers, it is large enough to allow their use in wireless transmitters. Consequently, it turns out that the dynamic range requirement is the most important factor to enable RF filters on-chip. The experimental results for quality factor of on-chip inductors in CMOS and BiCMOS technologies suggest a quality factor around 5 and 15, respectively. However, Using the MEMS technique, the quality factor of on-chip inductors can reach as high as 30.

2- The need for automatic tuning circuits. This is probably the second most important factor to enable RF filters on-chip. For RF filters the required quality factor is still relatively high (typically, 20~60), which makes them very sensitive to the process, voltage, and temperature variations. High frequency operation also makes the tuning design very difficult.

3- Low-power requirement. This requirement is true especially for mobile applications. As more and more functions are integrated, the design is facing more and

more battery life problems. Power management will help, but in general we would prefer low-power designs for mobile applications.

CHAPTER III

A FOURTH-ORDER ACTIVE LC BAND PASS FILTER

3.1. Introduction

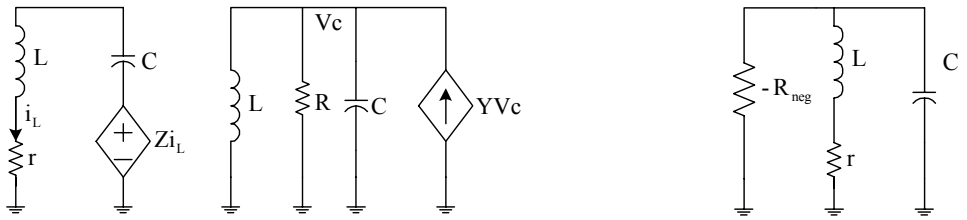
Surface acoustic wave (SAW) filters are applied extensively in today's communication equipment. These high performance components have reached a key [17] position in current communication technology assisting the efforts to increase the spectral efficiency of limited frequency bands for higher bit rates. During the last decade, driven by booming wireless technology business, great and important progress in SAW device performance was made, and a variety of innovative applications were developed. These developments are based on technological improvements. SAW technology has evolved to the GHz range in recent years and now routinely covers the frequency range up to 3GHz. This frequency band is used as carrier frequency for many new wireless communication and sensor applications. SAW filters are not suitable for monolithic implementation and are usually implemented off-chip since silicon is not a piezoelectric material. Some attempts can be found in the literature [18] that implements an integrated SAW filter using a ZnO-SiO2-Si layered structure. The aluminum inter-digital transducers are located at the ZnO-SiO2 [18]-[19] interface to obtain a high piezoelectric material combining the attractive SAW propagation with a relatively easy fabrication process. The reduced size and weight of the complete system will be an advantage in cordless telephone, car radio, and all kinds of portable consumer electronics product. Moreover, receiver architectures, such as in radio, television, and other telecommunication systems use higher IF frequencies to improve the interfering signal rejection.

Recent allocations of radio frequency spectrum for cellular services have placed new emphasis on the development of small, low-cost, wireless products [20]-[21]. The commercial sector has responded with the introduction of chip sets with increasing levels of integration. However, to date, virtually all high performance wireless products continue to rely on discrete LC, crystal, ceramic, or SAW devices for the realization of RF pre-selection and IF channel selection filtering [11].

Researchers have attempted to design high Q bandpass filters by enhancing lossy integrated inductors [17]-[29]. Shunt mounted resonators, composed of an inductor and capacitor in parallel can be used to realize RF bandpass filters [30]-[33]. Shown in Fig. 3.1(a), active Q-enhancement for LC filters can be implemented by placing the lossy monolithic inductors in a positive feedback loop containing an amplifier to realize high Q filters [26]. Another equivalent approach is to connect a negative resistor in parallel with the LC resonator, and this resistor can be linearized to yield a filter with improved linearity [27] (see Fig. 3.1(b)). Furthermore, the negative resistor has to be variable to tune Q over process and temperature variations.

3.2. Q-Enhancement Technique

Regardless of the coupling mechanism between the resonators, losses associated with the on-chip reactive components change the center frequency and loaded quality factor of the filter. Having estimated and modeled the total resistive loss of the resonator, a negative resistor ($-1/G_{neg}$) can be added to compensate its effect. The Q-enhancement technique, shown in Fig. 3.2, is widely used to boost the Q of the filter [17]-[23].



(a) (b)

Fig. 3.1 Active Q-enhancement using (a) positive feedback (b) negative resistance.

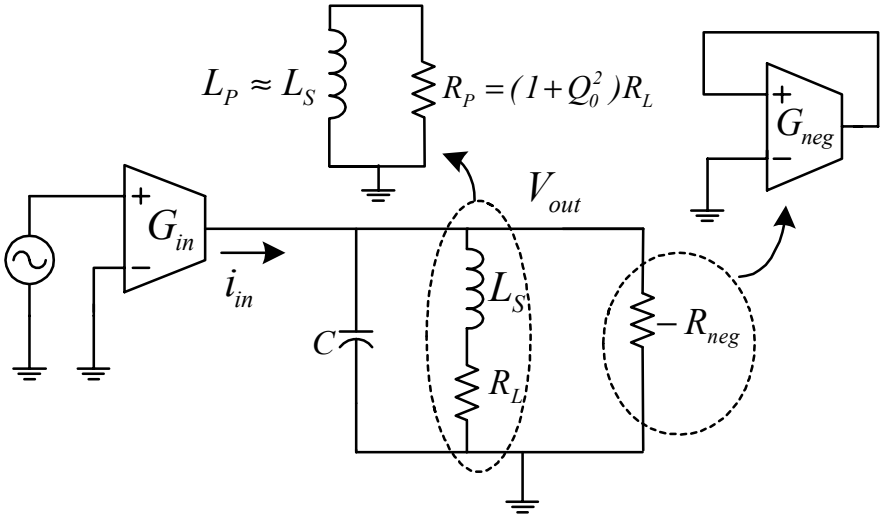


Fig. 3.2 Q-enhancement technique applied to a RLC filter

The series combination of the inductor (L_S) and its loss (R_L) can be modeled as a parallel combination of L_P=L_s(1+1/Q_0^2) and R_P=R_L(1+Q_0^2) where Q_0=$L\omega_0/R_L$. Thus, the center frequency ω_0, quality factor Q and the bandwidth BW of the resonator in Fig. 3.2 can be described as:

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{1-\frac{G_{neg}R_P}{Q_0^2}} = \frac{1}{\sqrt{LC}}\sqrt{1-\frac{1-\frac{Q_0}{Q}}{Q_0^2}} \qquad (3\text{-}1)$$

$$Q = \frac{1}{1 - G_{neg} R_P} Q_0 = \frac{G_P}{G_P - G_{neg}} Q_0 . \tag{3-2}$$

$$BW = \frac{\omega_0}{Q} = \frac{1}{\sqrt{LC} Q_0^2} \sqrt{\frac{Q_0^2 - G_{neg} R_P}{(1 - G_{neg} R_P)^2}} \tag{3-3a}$$

As (3-1) shows, the quality factor of the inductor (Q_0) modifies the center frequency and the Q of the resonator. Thus at high frequencies, due to the higher loss, a larger G_{neg} is required which results in changing both Q and ω_0. Note that (3-2) is valid only around the LC tank's resonant frequency, due to the fact that the equivalent parallel conductance from the inductor loss varies with frequency.

The series combination of the inductor L and its loss R_L can be modeled as a parallel combination of $L_P = L(1 + 1/Q_0^2)$ and $R_P = R_L(1 + Q_0^2)$. If the inductor quality factor Q_0 is large enough then, $L_P \cong L$ and $\omega_0^2 \approx 1/LC$. In this case the loaded quality factor of the tank depends on the exact relation between R_P and G_{neg} (see (3-2)). The frequency response of the filter in Fig. 3.2 can be approximated as

$$H(s) = \frac{V_o(s)}{V_{in}(s)} \cong \frac{-(G_m / C)s}{s^2 + \frac{G_p - G_{neg}}{C} s + \frac{1}{LC}} = \frac{-A_0 \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{3-3}$$

where $G_p = 1/R_p$, $A_0 = G_m / (G_P - G_{neg}) = G_m Q \sqrt{L/C}$ and $Q = \sqrt{C/L} / (G_p - G_{neg})$.

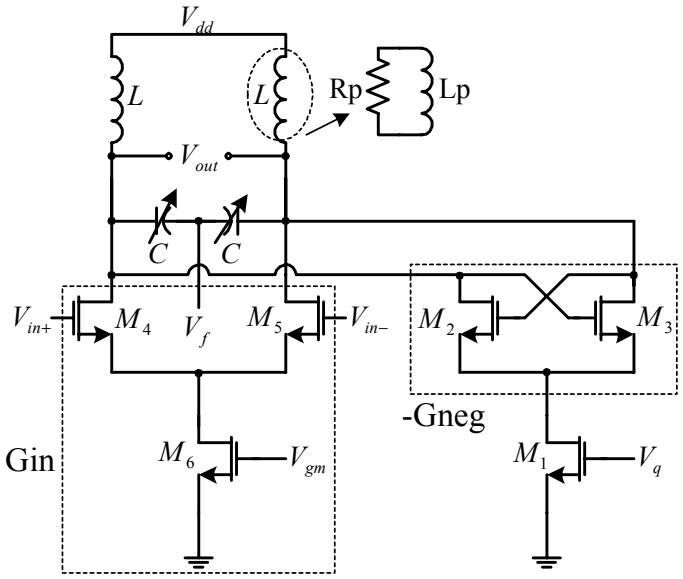


Fig. 3.3 *Q*-enhanced LC bandpass filter.

Fig. 3.3 shows the circuit implementation of a second-order *Q*-enhanced LC filter. The center frequency tuning is achieved through varactors which are PMOS transistors implemented in separate wells (in an n-well technology) and with their drain/source terminals connected together to the well terminal. The capacitance seen by the gate is adjusted by changing the voltage V_f and exploiting the variation of the gate capacitance when the transistor goes from weak inversion to the accumulation region [23].

The cross coupled transistors M_2-M_3 form the negative transconductance -G_{neg} which based on (3-2) changes the quality factor of the filter. The transconductance G_{neg} has the following dependence on V_q.

$$G_{neg} = \beta_q \left(V_q - V_T \right) \tag{3-4}$$

where $\beta_q = 0.5 \mu C_{ox} \sqrt{0.5 (W/L)_{2,3} (W/L)_1}$ and $(W/L)_{2,3}$ and $(W/L)_1$ refer to the (W/L) ratios of $M_{2,3}$ and M_1 in Fig. 3.3, respectively.

The control voltage V_{gm} changes the transconductance G_m of the input differential pair M_4-M_5 thus, changing the peak amplitude gain A_0 of the filter while keeping the Q invariant. Note that G_m as a function of V_{gm} can be expressed as

$$G_m = \beta_m \left(V_{gm} - V_T\right) \tag{3-5}$$

where $\beta_m = 0.5\mu C_{ox}\sqrt{0.5\left(W/L\right)_{4,5}\left(W/L\right)_6}$ and $(W/L)_{4,5}$ and $(W/L)_6$ refer to the (W/L) ratios of $M_{4,5}$ and M_6 in Fig. 3.3, respectively.

Thus, using (3-4) and (3-5) the peak amplitude gain A_0, defined in (3-3), can be expressed as,

$$A_0 = \frac{G_m}{G_P - G_{neg}} = \frac{2\beta_m\left(V_{gm} - V_T\right)}{G_P - \beta_q\left(V_q - V_T\right)}. \tag{3-6}$$

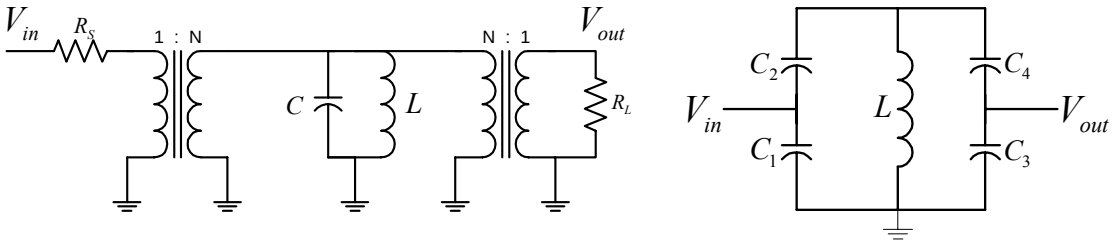
In a similar way the quality factor Q can be expressed as,

$$Q = \frac{\sqrt{C/L}}{G_P - \beta_q\left(V_q - V_T\right)}. \tag{3-7}$$

3.3. Higher Order LC Filter Implementation

For a single ideal LC resonator considered between a source of impedance R_S and a load of impedance R_L, the loaded Q_L becomes R_P/X_P where $R_P = R_S||R_L$ and X_P is the reactance of the inductor or capacitor at resonance. For source and load impedances of 50Ω, the overall loaded Q_L and ultimately the frequency selectivity would be low. One solution to this problem is to implement an impedance transformer that can shift the source and load impedance up in value such that the effective source and load impedances seen by the resonator are higher. This is illustrated in Fig. 3.4(a). However,

the wire-wound impedance transformers shown in Fig. 3.4(a) are not usually used in practice.



(a) (b)

Fig. 3.4 Single LC resonator with (a) ideal impedance transformers (b) tapped capacitor transformers.

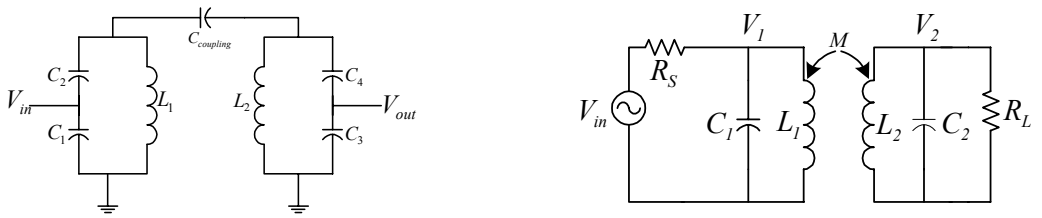
A more convenient way of realizing the impedance transformation is to use a tapped capacitor or inductor. The tapped capacitor, shown in Fig. 3.4(b), is usually preferred for practical reasons. The impedance matching between the input and output impedances can be achieved by proper ratio between the tapped capacitors. The impedance transformation ratio at the input and output can be expressed as

$$n_{in} = \left(\frac{C_1}{C_1 + C_2} \right)^2 \tag{3-7a}$$

$$n_{out} = \left(\frac{C_3}{C_3 + C_4} \right)^2 \tag{3-7b}$$

Observe from (3-7a) and (3-7b), depending on the values of input and output impedances the capacitor ratios can be high which results in using big capacitors.

When realizing a practical narrow-band bandpass filter, two or more resonators are needed. The resonators must be coupled together, and the most common means of accomplishing this is to use capacitors, as shown in Fig. 3.5(a).



(a) (b)

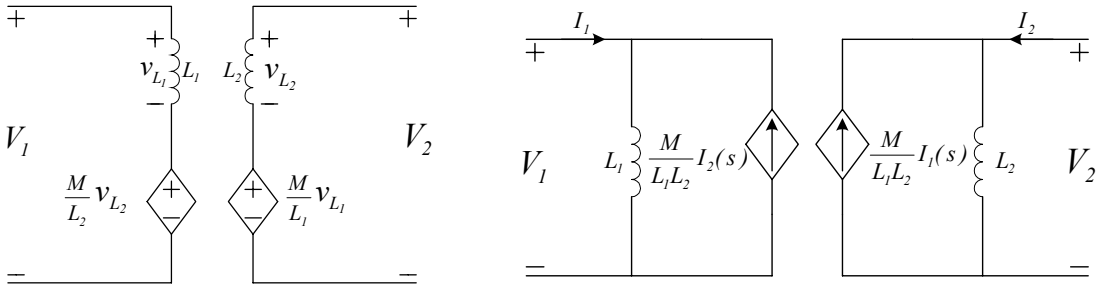
Fig. 3.5 Schematic of a coupled resonator bandpass filter using (a) capacitor (b) mutual inductance

The choice of the coupling capacitor value is important. Too high a value results in over-coupling and a broadening of the response; on the other hand, too low a value results in under-coupling and excessive insertion loss. On-chip capacitor values usually show significant variations which demand a separate tuning scheme. Alternatively, by using mutually coupled inductors (Fig. 3.5(b)), the problem of the variation in the inductance value is solved since their values depend mostly on layout, which usually is less sensitive to process variations [33].

3.4. Coupled Resonators Implementation

As mentioned previously, to establish a magnetic coupling between two on chip inductors, we can use either layout [24] or circuit techniques [25]. In the former case, coupled-inductor resonators are implemented using on chip interleaved spiral inductors

on the top level metal and patterned ground shield to improve the quality factor. In this technique, large capacitive coupling can cause the phase difference of the currents in the coupled-inductors to deviate from the desired 90^{o} in addition to the capacitive loss. Also, there is no control on the magnetic coupling to change the quality factor of the filter.



(a) (b)

Fig. 3.6. Two possible emulations of coupled inductors based on (3-9) (a) using VCVS's (b) Norton equivalent using CCCS's [31].

Another technique to couple two inductors is to emulate the magnetic coupling in an electrical way [25]. Starting with the equations describing an ideal transformer, there are different ways to emulate it. One option is,

$$V_1(s) = L_1 s I_1(s) + \frac{M}{L_2} L_2 s I_2(s) \quad and \quad V_2(s) = \frac{M}{L_1} L_1 s I_1(s) + L_2 s I_2(s) \tag{3-8}$$

where M and $K = M / \sqrt{L_1 L_2}$ are the mutual inductance and the coupling coefficient, respectively.

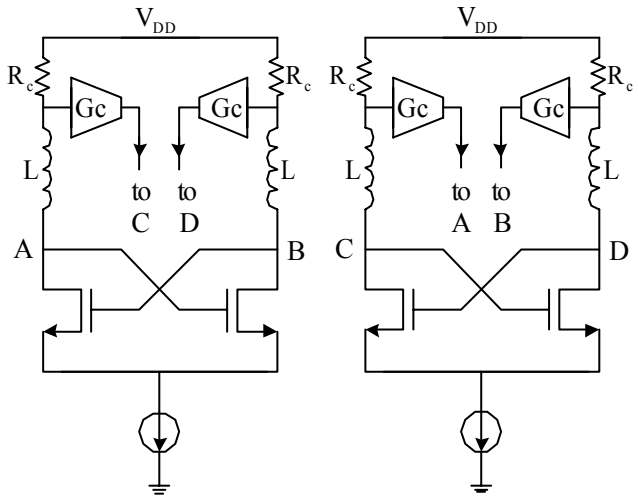


Fig. 3.7. Emulation technique proposed in [25].

Two possible implementations based on (3-8) are shown in Fig. 3.6. The main drawback of Fig. 3.6(a) is the need of voltage summation in the input and output branches. Fig. 3.6(b) is the basic idea used in [25], in which instead of detecting the current before it flows into each inductor, the net current of each inductor is detected as a voltage drop across a resistor in series with the inductor (see Fig. 3.7). This series resistor degrades the quality factor of the inductor and the linearity of the filter.

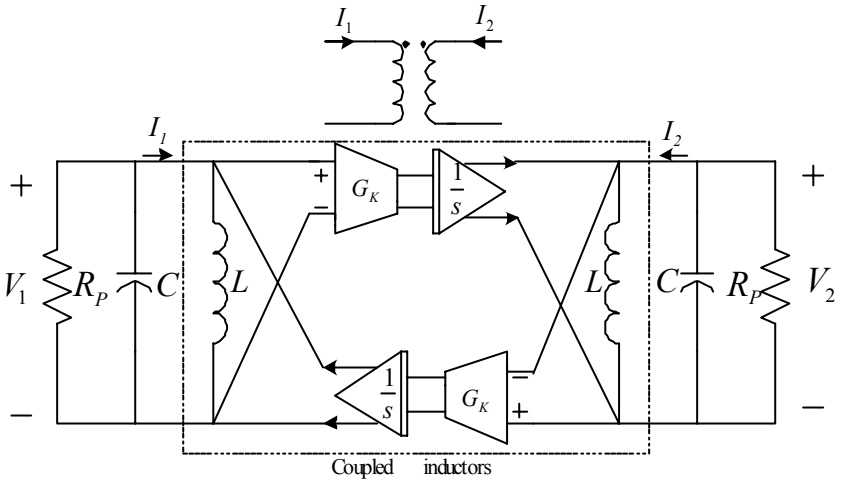


Fig. 3.8 Proposed emulation technique for coupled inductors.

3.4.1. Proposed Coupled Inductors Emulator

The transformer equations in (3-8) can be written in a form suitable for both high frequency operation and practical implementation using current addition instead of voltage addition:

$$V_1(s) \approx L_1 s\left[I_1(s) + \frac{1}{s}\frac{M}{L_2 L_1} V_2(s) \right]. \tag{3-9}$$

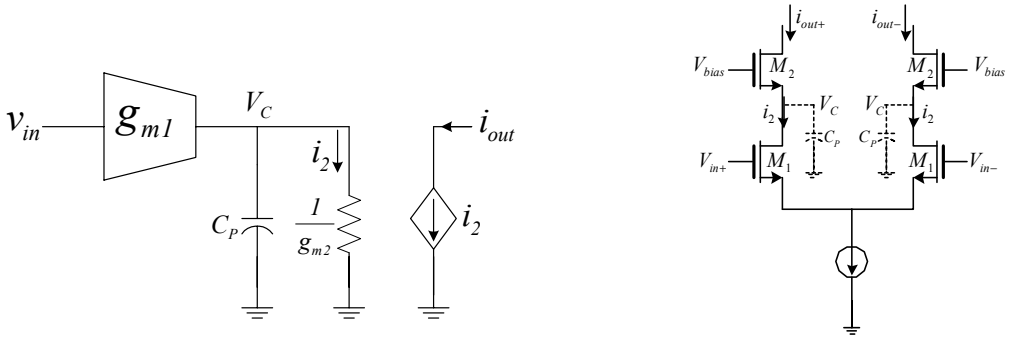
Equation (3-9) is obtained using the approximation $V_2 \approx L_2 s I_2(s)$ which is based on the fact that since the two inductors are a great distance apart in space and there is no magnetic coupling between them, their mutual inductance is very small and K is close to zero (loosely coupled). Similarly,

$$V_2(s) \approx L_2 s\left[I_2(s) + \frac{1}{s}\frac{M}{L_2 L_1} V_1(s) \right]. \tag{3-10}$$

Equations (3-9) and (3-10) suggest that the mutual effect of V_2 and V_1 can be emulated by converting voltage V_2 and V_1 to current using a transconductance block with

gain $G_K=M/(L_1L_2)$ and then integrating this current. Fig. 3.8 shows the proposed implementation of coupled inductors based on (3-9) and (3-10).

The combination of the G_K and integrator operation can be implemented using a properly sized cascode structure, as shown in Fig. 3.9.



(a) (b)

Fig. 3.9 Cascode structure used as G_K cell (a) Conceptual single-ended; (b) Fully-differential implementation.

Consider the small signal equivalent circuit of a cascode G_K circuit shown in Fig. 3.10. Since the output is connected to the LC resonator, C_{gd2} and C_{db2} can be merged with the capacitor of the tank. Thus, their effect in the following analysis can be neglected.

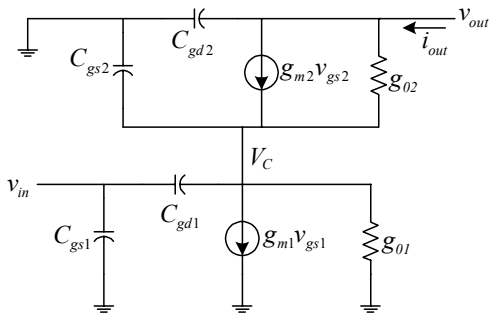


Fig. 3.10 Small signal differential-mode equivalent circuit of a cascode structure

C_P in Fig. 3.10 is the total parasitic capacitance at node V_C which is mainly dominated by C_{gs2}. Straight analysis yields:

$$G_K(s) = G_0 \frac{s+z}{s+p} = \frac{G_0}{s} \frac{s+z}{1+\frac{p}{s}} \tag{3-11}$$

where,

$$z \approx \frac{g_{m1} A_{v2}}{C_{gs2} - A_{v2} C_{gd1}} \tag{3-12}$$

$$p \approx \frac{g_{m2}}{C_{gs2} + C_{gd1}} \tag{3-13}$$

$$G_0 \approx \frac{C_{gs2} - A_{v2} C_{gd1}}{(C_{gd1} + C_{gs2}) / g_{02}} \tag{3-14}$$

where $A_{v2}=g_{m2}/g_{02}$.

Note that the zero will occur after the pole implying that in the frequency range of $p<\omega<z$ the output current of Fig. 3.9 is the integrated version of its input voltage. In this frequency range, (3-11) can be approximated as:

$$G_K(s) \approx G_0 \frac{z}{s} = \frac{g_{m1} g_{m2}}{(C_{gs2} + C_{gd1})s} = \frac{G_{K0}}{s} \tag{3-15}$$

where $G_{K0}=g_{m1}g_{m2}/(C_{gs2}+C_{gd1})$.

Thus, assuming $L_1=L_2=L$, the relation between the coupling circuit design parameters and the filter specifications can be found as:

$$\frac{g_{m1} g_{m2}}{(C_{gs2} + C_{gd1})C} \approx K\omega_0 \tag{3-16}$$

where C is the resonance capacitance of the varactors and K is the coupling coefficient.

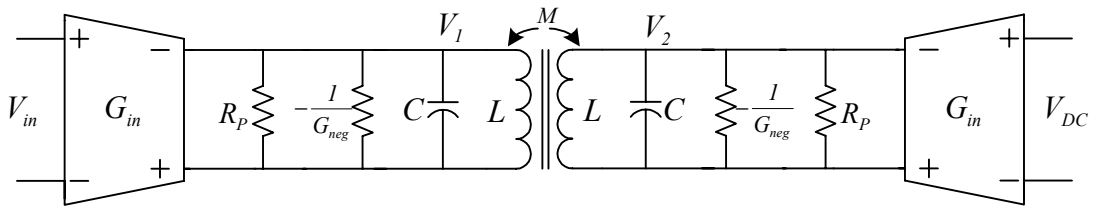


Fig. 3.11 A fourth-order LC bandpass filter.

3.5 Fourth-Order Band Pass Filter Architecture

Consider Fig. 3.5(b) with R_S=R_L=2R, L_1=L_2=L and C_1=C_2=C. For a fourth-order filter the ideal design equations for equal LC resonators can be calculated as [34]:

$$LC = \frac{1}{\omega_0^2},\ K = \frac{1}{\sqrt{2}Q},\ R = Q\sqrt{2\frac{L}{C}},\ \frac{\omega_0}{Q} = \frac{\sqrt{2}}{RC} \tag{3-17}$$

In critical coupling (flat passband), i.e. $\omega_0 / Q = 1/\sqrt{2}$, R has no effect on bandwidth but can change the peak and flatness of the passband. In other words, while the resonant (center) frequency $\omega_0 = KQ\sqrt{2/LC}$ is tuned by changing K, the value of R needs to be adjusted properly to preserve the flatness of the passband, which is to keep $\omega_0 / Q = 1/\sqrt{2}$. Note that at the center frequency and in critical coupling the absolute value of the transfer function from V_{in} to V_2 is the same as V_{in} to V_1. Furthermore, there is a 90° phase shift between V_1 and V_2.

A simple fourth-order LC bandpass filter can be built using two equal resonators with their lossy inductors coupled to each other by a factor of K, as shown in Fig. 3.11. The transfer function of the filter using an arbitrary notation [24] can be written as:

$$H(j\omega)=\frac{V_2(j\omega)}{V_{in}(j\omega)}=\frac{-jG_{in}\dfrac{K}{(1-K^2)LC^2}\omega}{\left(-\omega^2+j\dfrac{\omega_0}{Q}\omega+\omega_0^2\right)^2-\left(\dfrac{K}{(1-K^2)LC}\right)^2} \tag{3-18}$$

where $\omega_0=1/\sqrt{L(1-K^2)C}$, $Q=R/\sqrt{L(1-K^2)/C}$ and $R=1/(G_P-G_{neg})$.

As equation (3-18) shows, the magnetic coupling *K* between the two inductors affects both ω_0 and Q. For a fixed ω_0, the effect of *K* can be compensated by varactor capacitance *C*. Once ω_0 is fixed, the bandwidth of the filter can be tuned by changing *K*. For proper operation of the magnetic coupling emulator, any magnetic coupling due to the interaction between the two inductors should be kept to a minimum. One way to accomplish that is by placing the inductors far from each other. Another option is to use a neutralization technique [11]. The former approach is used in the work presented here. Fig. 3.12 shows the circuit implementation of the fourth-order bandpass filter based on Fig. 3.8, Fig. 3.9 and Fig. 3.11.

G_{in} converts the input voltage to a current, and also tunes the passband gain of the filter. G_{in} consists of a differential pair connected to the LC tank. The differential pair consisting of M_{C1}-M_{C2} and I_K realizes the emulator (G_K/s in Fig. 3.8) which is connected in a cross coupled manner, in which the amount of coupling is controlled by I_K. M_{neg}'s implement the Q-enhancement negative transconductance G_{neg}, as depicted in Fig. 3.2. On-chip spiral inductors and CMOS varactors form the resonators. The inductor parameters were calculated using ASITIC [28]. The varactors were realized using simple PMOS transistors with drain and source connected to ground [35].

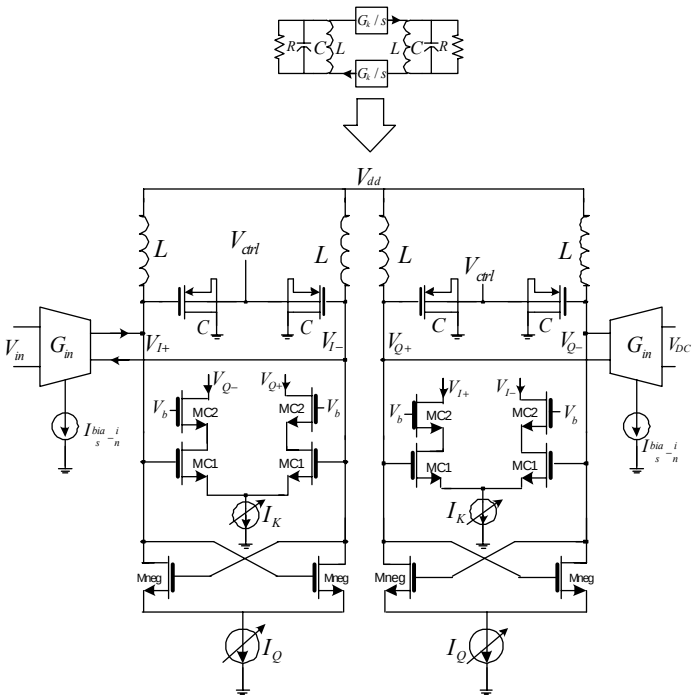


Fig. 3.12 Fourth-order LC bandpass filter circuit implementation.

The gate voltage V_{ctrl} modifies the capacitance value of the varactor. Total losses of the resonators were calculated in a realistic estimation of inductor's Q which for this technology is around 2 to 3. Using (1b) the value of the negative resistor ($-2/G_{neg}$) can be calculated based on the required quality factor of the filter. The bias current I_Q sets the value of G_{neg} for the filter Q-enhancement.

3.5.1. Nonlinearity Analysis

Following the approach presented in [25], the nonlinearity of individual parameters (G_{neg}, G_{in}, G_k and C_V) taken into account one at the time can be determined with the assumption that the rest of the circuit is linear. This approach provides insight as

to which parameters contribute most to the total nonlinearity. A detailed expression of the nonlinearity due to each individual block can be found in [23] and [29].

The two parameters which are affected by the full output voltage swing are G_{neg} and G_K. Due to the negative transconductance at the resonance frequency, the total output impedance of each resonator is extremely high. Thus, to generate a finite output voltage swing, a very small coupling current $G_K V_I$ (and $G_K V_Q$) is required. In other words, the coupling transconductance G_K is a small value and its impact on the overall nonlinearity of the filter can be ignored. Furthermore, the harmonics generated by the G_K parameter get attenuated more due to the integration property of G_K at the resonance frequency. Considering the negative transconductance G_{neg} as the main source of nonlinearity, the 1-dB compression point of a second order LC filter can be approximated as [17]:

$$V_{1dB-Gneg}^2 \approx 1.16 \frac{G_{neg}^2}{\mu C_{ox} \frac{W}{L} G_{in}^2} \left(\frac{G_P - G_{neg}}{G_{in}} \right)^2 . \tag{3-19}$$

Note that the predicted $V_{1\text{-}dB\text{-}Gneg}$ of (3-19) and the total $V_{1\text{-dB}}$ from transistor level circuit simulation with Q=20 differ by 33%. To increase the linearity of the Q-enhancement, source degeneration resistors for G_{neg} or attenuating the input signal to G_{neg} [27] could be used. Similar discussion can be held to study the two-tone behavior of the filter. The IM3 of the filter due to two input tones with equal amplitudes of A_{in} and at two frequencies close to ω_0 can be approximated as:

$$IM3_{Gneg} \approx \frac{3A_{in}^2}{4\sqrt{2}(1-K^2)LQ\omega_0} \frac{\beta_{in}^2}{G_{in}^2} \frac{1}{G_{neg}} \tag{3-20}$$

where, $\beta = 1/2 \mu C_{ox} W/L$.

Note that by having a better coupling between the two resonators, i.e. K≈1, the IM3 can significantly increase. Simulation results for two cases with Q=75, ω_0=2.5GHz and different inductor losses verify the inverse relation between IM3 and G_{neg}, so that for Q_{01}=2.7 and Q_{02}=2 the IM3/G_{neg} ratio is -38.6dBc/8.46mA/V and -33dBc/9.9mA/V, respectively.

3.5.2. Noise Analysis

The total input referred noise of Fig. 3.12 can be expressed as:

$$\overline{V}^2_{noise-in} = \frac{(1+\alpha)\gamma}{A_v^2}\frac{2KT}{3CG_P}\frac{Q}{Q_0}\left[\frac{G_{in}}{1+\alpha}+\left|G_{neg}\right|+G_K+\frac{3G_P}{2}\right] \tag{3-21}$$

where γ accounts for the excess noise of short-channel devices and α<1 is defined as [31]:

$$\alpha = \frac{\int_0^\infty \left|Z_I(f)\right|^2 df}{\int_0^\infty \left|Z_Q(f)\right|^2 df} \tag{3-22}$$

where $Z_I(f)$ and $Z_Q(f)$ are the total impedances seen by the in-phase and quadrature output nodes which at resonance are equal and can be approximated as $1/(G_P\text{-}G_{neg})$, thus α=1. A_V is the absolute value of voltage gain from input to the in-phase (V_I=V_1) and quadrature (V_Q=V_2) outputs which at the resonance frequency are equivalent and can be approximated as:

$$A_v(j\omega_0) \approx \left|\frac{V_I(j\omega_0)}{V_{in}(j\omega_0)}\right| = \left|\frac{V_Q(j\omega_0)}{V_{in}(j\omega_0)}\right| = \frac{1}{\sqrt{2}}QG_{in}(1-K^2)L\omega_0 . \tag{3-23}$$

Based on (3-21) and (3-23), one way to reduce noise is to increase A_V by increasing G_{in}; however, this brings an increase in nonlinearity and power consumption due to the increased G_{in}. Having larger G_P (i.e. smaller R_L) helps to significantly reduce noise and power consumption. It also gives a raise to the center frequency of the filter for

the same amount of power consumption (See (3-1) and (1b)). Simulation result for Q=66 and ω_0=2.5GHz shows 15dB gain and 162μV input referred noise in 40MHz bandwidth. Based on (3-21) and (3-23), the predicted noise is 12% smaller and gain is 14% greater than the simulation results. These differences are mainly due to the approximate values (α=1, K=0.02 and γ=1.5) used to evaluate (3-21) and (3-23) as well as second-order effects not included in the approximation.

3.5.2. Dynamic Range and Power Consumption

The total 1dB compression point of the filter is due to the nonlinearity contributions of all the parameters. Considering all these nonlinearity sources makes the analysis very difficult. Instead, assuming G_{neg} as the only nonlinear element, the dynamic range (DR) of the filter can be approximated as:

$$DR = \frac{V_{1dB}^2}{\overline{V}_{noise}^2} \approx \frac{1.16(V_{GS} - V_{th})_{G_{neg}}^2 G_P}{(1+\alpha)\gamma \frac{4KT\beta_{neg}^2}{3C}\left(\frac{G_{in}}{1+\alpha} + |G_{neg}| + G_K + \frac{3G_P}{2}\right)} (\frac{Q_0}{Q})^2 . \quad (3\text{-}24)$$

Having a less resistive loss (R_L) in series with the inductor increases $G_P = 1/(Q_0^2 R_L)$ and reduces the required negative transconductance G_{neg}, which means a significant increase in G_P-G_{neg}. By increasing G_P-G_{neg} the Q is decreased and based on (3-25) this leads to increase in DR. Also, decreasing G_{in} improves the dynamic range as it reduces the swing of the voltage at the output and linearizes the filter. Furthermore, increasing G_P-G_{neg} helps to reduce the power consumption. At the resonance frequency, the power dissipated due to the loss of the resonator can be calculated as:

$$P_{diss} \approx \frac{1}{\beta_{neg}^2}(1+G_{K0}^2)\frac{G_{neg}^4}{G_P}. \tag{3-25}$$

For a fixed quality factor of the filter, having less resistive loss (greater G_P) results in a smaller G_{neg} and consequently smaller P_{diss}. Simulation results show that increasing inductor loss by 10% increases G_{neg} by 7% which leads to 70% increases in P_{diss}.

Table 3-1 compares some of the most important parameters of the proposed filter with those of [31] in terms of the resistance ratio R_S/R_L, where R_S is the additional resistor in series with the inductor used in [31] to sense current, and R_L is the inherent resistive loss of the inductor. The last column in Table 3-I compares the simulation results of the proposed LC filter with [31], both designed to have the same Q=50 and center frequency of 2.4GHz. These results are obtained based on the following parameters: G_{in}=3mA/V, L=2.5nH and C=1.4pF, Q_0=2.5.

Table 3-1 Comparison Table

Parameter ratio	Approximated Expressions	Evaluated expression (dB)	Simulation (dB)
$\overline{V}_{1dB}^2 / \overline{V}_{1dB}^{2\,'}$	$\left(1+\frac{R_S}{R_L}\right)/\left(1-\frac{R_S}{R_L}\right)$	2.23	4
$\overline{V}_{noise}^2 / \overline{V}_{noise}^{2\,'}$	$1/(1+\frac{R_S}{R_L})^2$	-2.27	-2.8
DR / DR'	$\left(1+\frac{R_S}{R_L}\right)^3 / \left(1-\frac{R_S}{R_L}\right)$	5	7.6
$P_{diss} / P_{diss}^{'}$	$1/\left(\left(1+\left(\frac{R_S}{R_L}\right)^2\right)\left(1+\frac{R_S}{R_L}\right)\right)$	0.705	0.83

In Table 3-I, parameters marked with the prime sign (‘) are those of [25] and the comparison has been carried out with the assumption of having the same Q and ω_0 for both cases. As Table 3-I shows, having less resistance in series with the inductor results in lower loss and consequently lower G_{neg} which leads to a higher 1dB compression point. Also, lower loss means lower noise associated with the loss which in connection with the improved 1dB compression point results in a significant increase in dynamic range.

3.6. Test-Chip Measurement Results

The filter chip prototype was fabricated in AMI 0.5μm CMOS technology. The micrograph is shown in Fig. 3.13 which occupies a silicon area of 0.15mm^2.

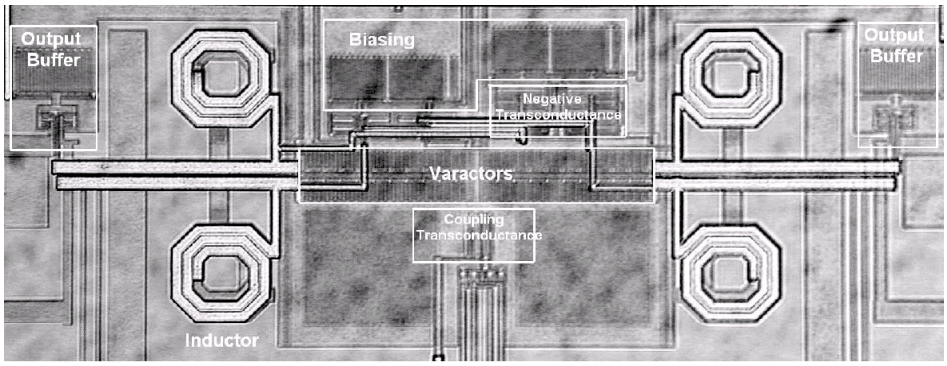


Fig. 3.13 Chip micrograph of the filter

The measurement setup for the transfer function and the intermodulation distortion of the filter are shown in Fig. 3.14 and Fig. 3.15, respectively.

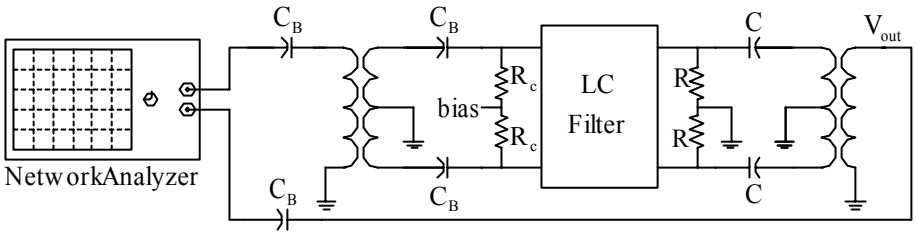


Fig. 3.14 Measurement setup for transfer function

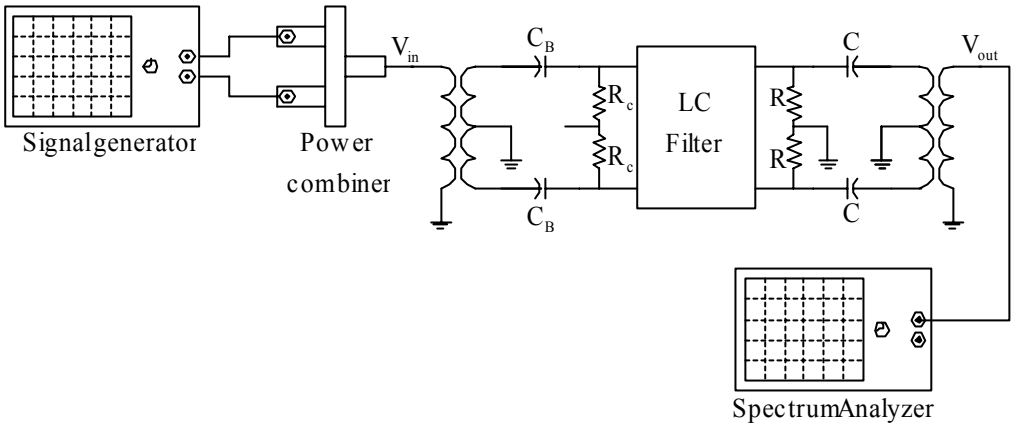


Fig. 3.15 Measurement setup for intermodulation distortion

The nominal power supply is 2.7V. Note that a simple open drain output buffer is employed to drive the 50Ω load of the instrument which shows a stand-alone attenuation of around -25dB at 2.5GHz. Simultaneous adjustments are made with both coupling (G_K) and Q tuning (G_{neg}) to keep one of the outputs constant while adjusting the other one. By tuning the amplitude and Q of the filter, once the two plots intersect, the coupling between them can be tuned to gain the optimum flatness over the band. The center frequency can be tuned from 2.42GHz up to 2.528GHz realizing a 4.3% tuning range. Note that to preserve the 4^{th} order nature of the filter at different center frequencies, the above procedure should be repeated to tune the filter. Fig. 3.16 shows the magnitude of

the frequency response of the both V_I (upper trace) and V_Q (lower trace) outputs of the filter which at the center frequency of 2.51GHz shows a -14dB passband gain. Note that due to -25dB attenuation of the output buffer, the actual passband gain of the filter is 11dB.

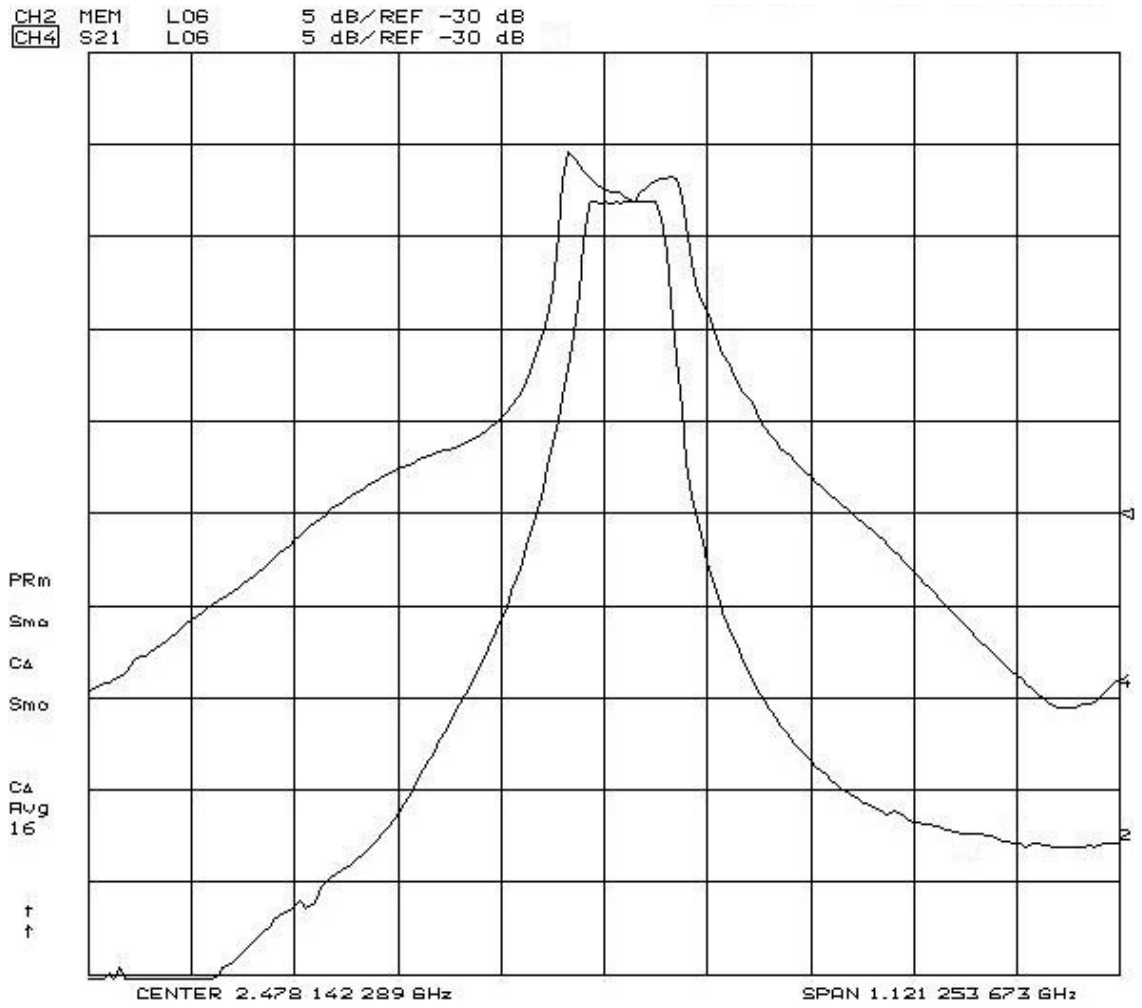


Fig. 3.16 Magnitude response (5dB/div) of both in-phase and quadrature outputs at f_0=2.51GHz (Note that the output buffer has -25dB attenuation).

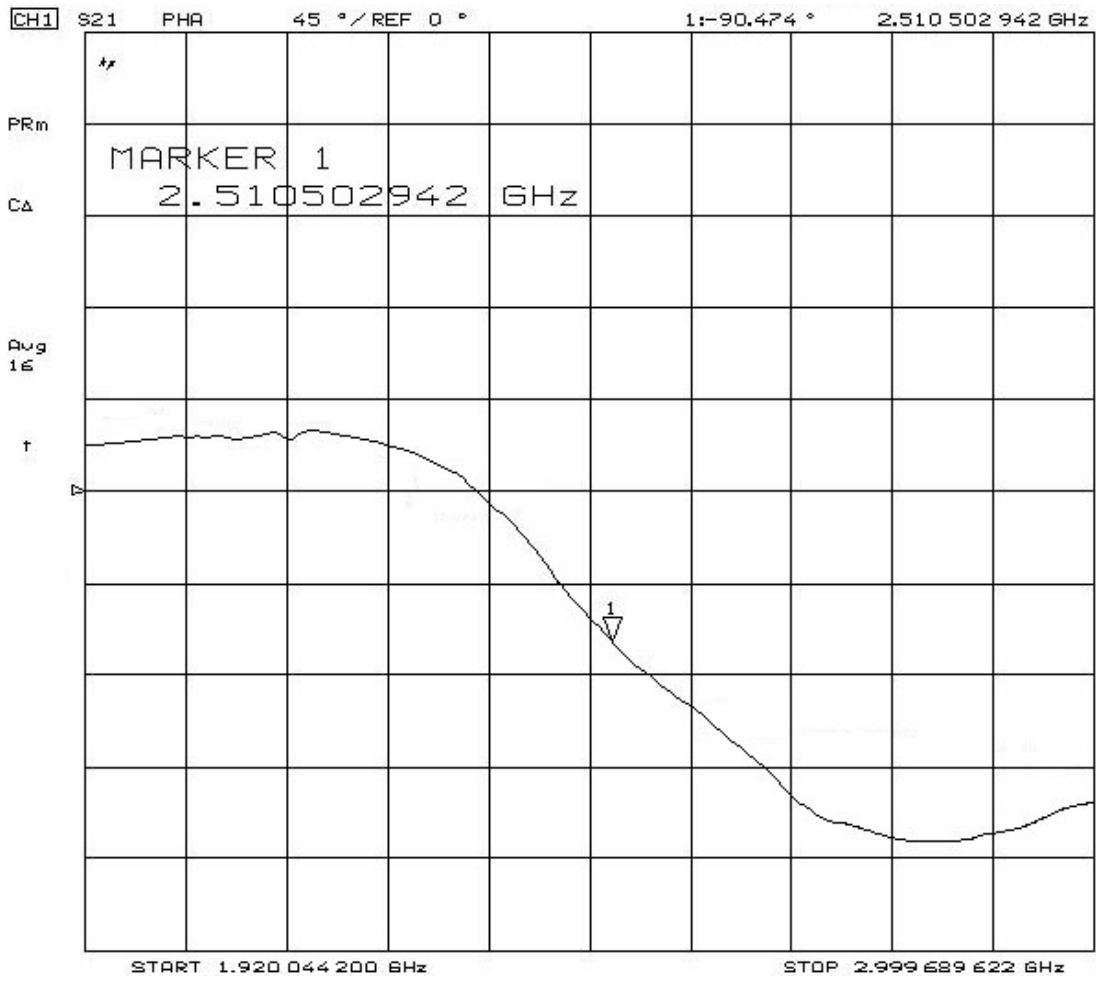


Fig. 3.17 Phase difference (45°/div) between the two in-phase and quadrature outputs.

Fig. 3.17 shows the phase difference between V_I and V_Q outputs and observe that they are in phase quadrature (-90 degree) at the filter center frequency. By changing coupling (G_K) the bandwidth of the filter can be tuned at the resonance frequency; which changes both the Q and the center frequency of the filter as depicted in Fig. 3.18. This figure shows the quadrature output of the filter (V_Q in Fig. 3.10) for four different values of G_K. The best measured ripple in the passband shows about ±0.4dB. The bandwidth tuning range is nearly 10%. To maintain a fixed center frequency while tuning the bandwidth, a separate center frequency tuning through V_{ctrl} is carried out. Fig. 3.19 shows

the center frequency tuning of the quadrature output (V_Q) by changing the control voltage V_{ctrl} of the varactors manually. To maintain the flatness of the passband, the Q and coupling coefficient (G_K) of the two resonators need to be tuned while the center frequency is changed.

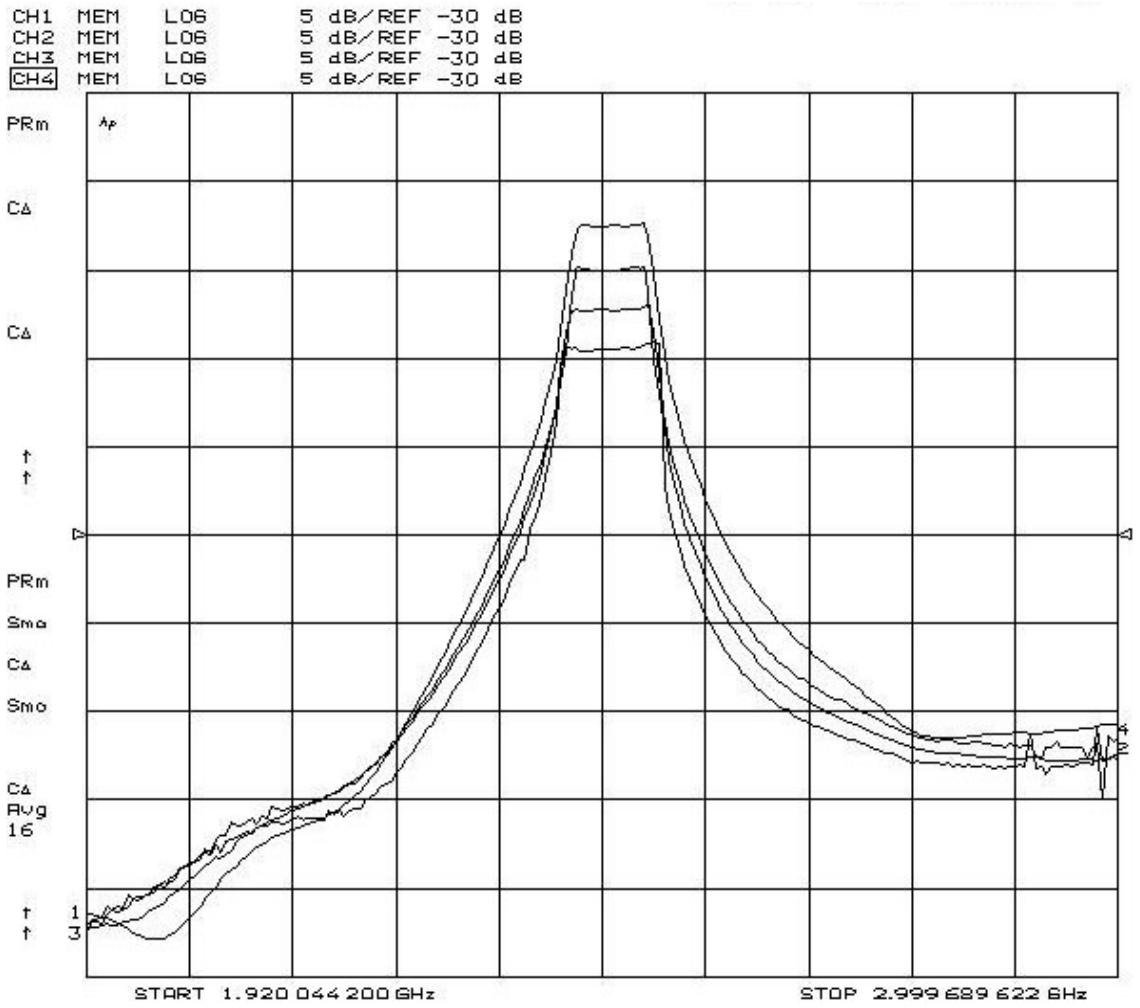


Fig. 3.18 Bandwidth tuning obtained by changing G_K (5dB/div). Upper trace for BW= 92.1MHz, and lower one for BW=102MHz.

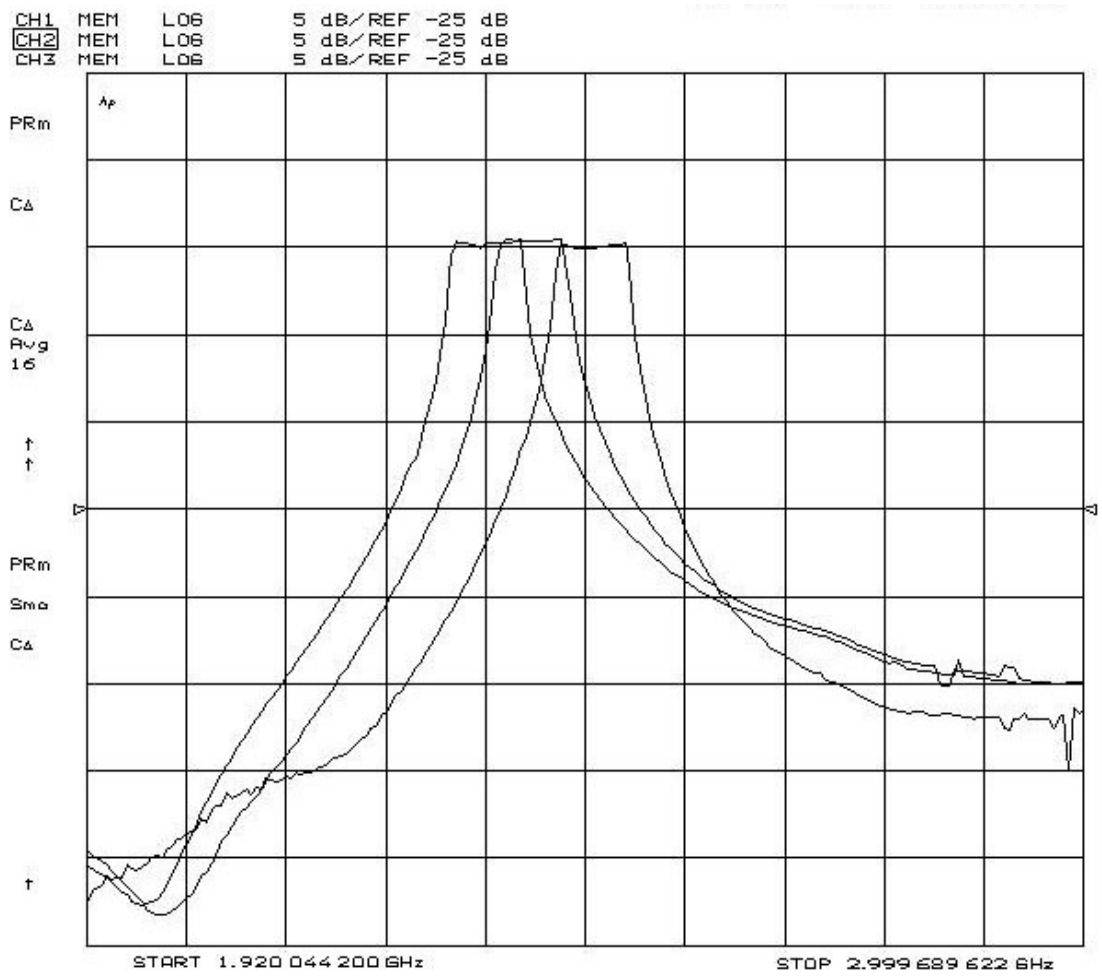


Fig. 3.19 Center frequency tuning (~108MHz/div) between 2.42GHz and 2.528GHz.

Fig. 3.20 shows the two-tone intermodulation distortion measurement. The two tones with equal amplitude of -38dBm are applied at 2.5GHz and 2.51GHz. The measured IM3 in a 1MHz resolution bandwidth is -38dBc. Fig. 3.21 shows the measured 1dB compression point at 2.5GHz which shows -19dBm and -32dBm 1-dB compression points for input and output, respectively. The corresponding SFDR is 39dB and the measured output noise density at the center of the band is -164dBm/Hz. Thus, the output noise integrated over the 100MHz filter's bandwidth, in a 1MHz bandwidth resolution is -84dBm, which yields a 1dB compression point dynamic range, noise figure and SFDR

of 52dB, 32dB and 39dB, respectively. The filter has a passband gain of 11dB and around 30dB of image rejection at $f_0 \pm 100$MHz. The minimum power supply for proper operation is 2.4V. A summary of the filter results is shown in Table 3-2.

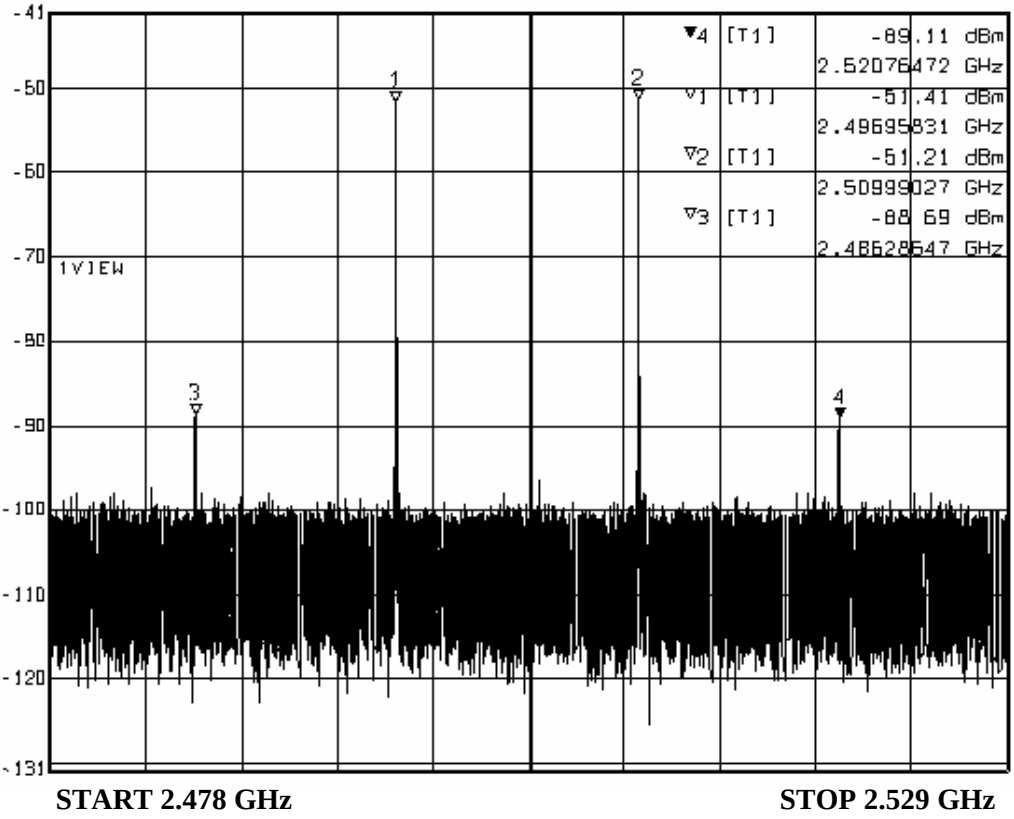


Fig. 3.20 Two tone (at 2.5GHz and 2.51GHz) intermodulation measurement.

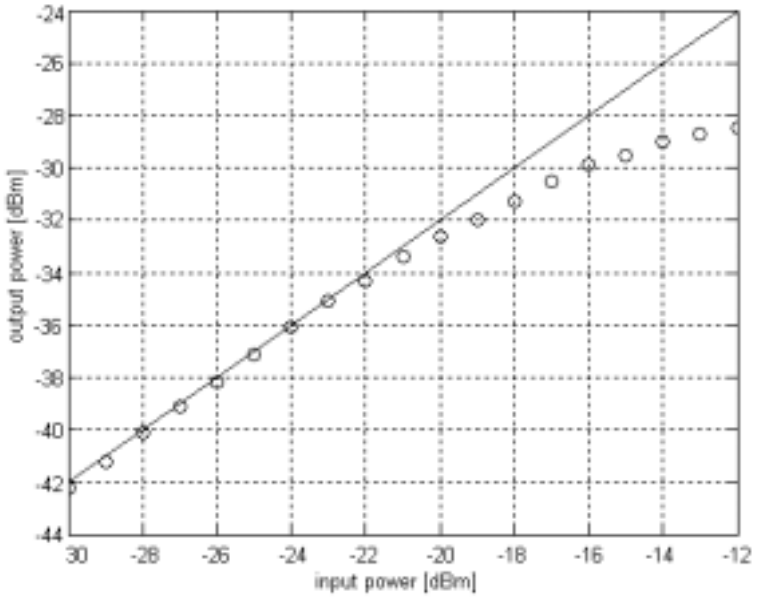


Fig. 3.21 1dB compression point measurement at 2.5GHz and BW=92MHz.

Table 3-2 Fourth-Order Filter Performance Parameters Comparison

	[25]	This work
$f_0(GHz)$	1.8	2.5
$BW(MHz)$	80	92
Ripple in passband(dB)	$<\pm 0.25$	$<\pm 0.4$
Passband gain	9	11
Q_0^*	2.7	2.7
1-dB compression DR (dB)	42	52
Current drain (mA)/Power supply (V)	16/2.7	15/2.7
Technology	*HP 0.5μm CMOS*	*AMI 0.5μm CMOS*
Relative Area(mm^2) per pole	0.0375	0.0375

CHAPTER IV

A STABLE VCO AMPLITUDE CONTROL LOOP

4.1. Introduction

In practical implementations of LC oscillators, due to dependence of the oscillation amplitude on the square of the oscillation frequency and the bias current of the LC tank [36], a stable amplitude control loop is essential to maintain constant oscillation amplitude over the tuning range of the VCO and to optimally bias the VCO over different conditions. Furthermore, using an amplitude control loop the bias current of the VCO can be tuned to achieve an optimum phase noise performance. A stable amplitude control loop, besides providing the above advantages for a single running VCO, it plays a key role in tuning the quality factor of Gigaherts LC filters. In this chapter a stable amplitude control loop is presented and its effect on improving the performance of LC VCO's is demonstrated. It has been also shown that the proposed amplitude control loop can be used to tune the quality factor of 2^{nd} order LC filters.

4.2. Loss-Control Feedback Loop

Besides its application in the VCO-based *Q*-tuning scheme, in practical implementations of LC oscillators, due to dependence of the oscillation amplitude on the square of the oscillation frequency and the bias current of the LC tank, a stable amplitude control loop is essential to maintain a constant oscillation amplitude over the tuning range of the VCO and to optimally bias the VCO over different conditions.

4.2.1 *Nonlinear Behavior of Q-enhanced LC Resonator*

A lossless LC resonant tank has an ideal quality factor of infinity and, with a nonzero initial condition, produces a steady sinusoidal oscillation. However, mainly due to losses associated with the integrated spiral inductors, the achievable quality factor of the tank in the GHz frequency range is, in practice, low. This loss kills the oscillation. As explained in 3.2, to over compensate the total loss of the LC tank, a *Q*-enhancement technique can be achieved by introducing a negative loss (resistor) through a positive feedback around the tank. Fig. 4.8 shows the conceptual implementation of the *Q*-enhancement technique.

The non-linear transfer characteristic of $-G_{neg}$ can be approximated by the following third degree polynomial. Even order terms do not appear due to the nature of the fully differential circuit,

$$i_{G_{neg}} = -a_1 v_{out} + a_3 v_{out}^3 \tag{4-1}$$

where, $a_1>0$ and $a_3>0$.

Applying Kirchoff's current law at the output node, the non-linear differential equation governing the oscillator of Fig. 4.1 can be found as

$$\frac{d^2 v_{out}}{dt^2} - \frac{a_1 - G_p}{C}\left(1 - \frac{3a_3}{a_1 - G_p} v_{out}^2\right)\frac{dv_{out}}{dt} + \omega_0^2 v_{out} = 0 \tag{4-2}$$

where, $\omega_0 = 1/\sqrt{L_P C}$.

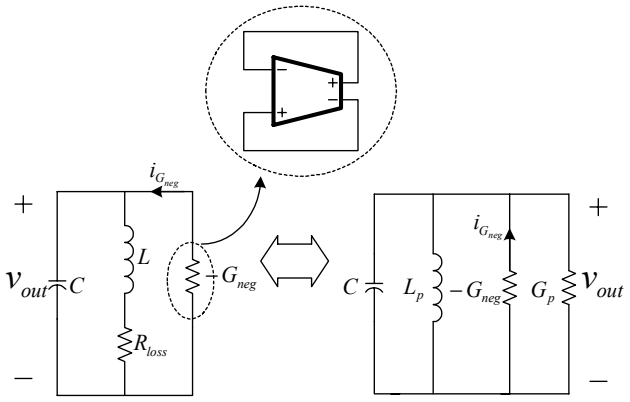


Fig. 4.1 *Q*-Enhancement LC resonator.

Assuming a steady state response for the output voltage $v_{out}(t)=A_s\sin(\omega_0 t+\varphi)$ in Fig. 4.1, the describing function (DF) of $-G_{neg}$, which is the *linear* transconductance gain relating the amplitudes of the fundamental frequency component of the output current to that of the input voltage [37], can be expressed as $G_{neg,DF}=\dfrac{I_{Gneg}(s)}{V_{out}(s)}=-a_1+\dfrac{3}{4}a_3A_s^2$.

Thus, in the *s*-domain, the describing equation of the circuit can be expressed as

$$s^2+b(A_s)s+\omega_0^2=0 \tag{4-3}$$

where, $b(A_s)=\dfrac{1}{C}\left(G_p-a_1+\dfrac{3a_3}{4}A_s^2\right)$.

In the oscillator's dynamic amplitude control mechanism, the position of the real part of the poles ($b(A_s)$ in (4-3)) depends on the oscillation amplitude A. If A is less than the desired steady state amplitude A_s, the poles move into the right half plane, making the amplitude increase. If A is greater than A_s, the poles move into the left half plane, decreasing the amplitude. As a consequence of this property, the poles will stay on the imaginary axis for $A=A_s$. In other words, the stability requirement [38] requires $\dfrac{db(A_s)}{dA}>0$.

Next, VCO amplitude regulation techniques based on the LCF scheme currently available in the literature are discussed.

4.3. Loss Control Feedback Mechanism

Fig. 4.2 shows the block diagram of an oscillator with a dynamic amplitude control mechanism in which V_f and V_C control the frequency and amplitude of the oscillation, respectively.

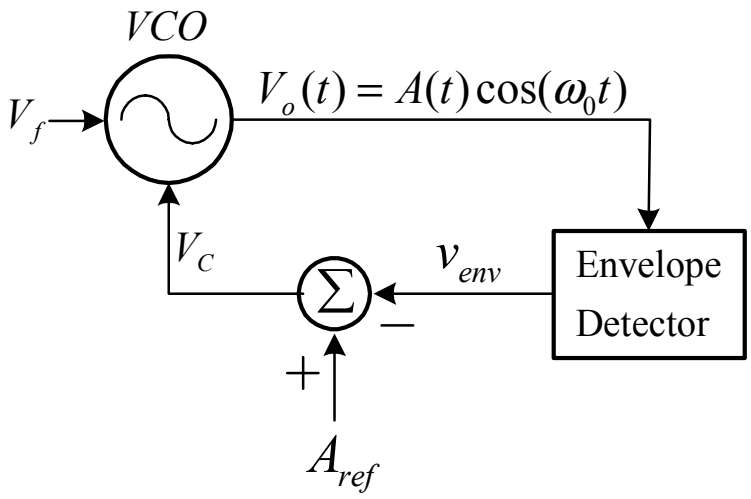


Fig. 4.2 Oscillator with amplitude control feedback.

In practical realizations of an oscillator, usually the signal V_C in Fig. 4.2 changes with ω_0, which means the oscillation amplitude changes as ω_0 changes even when the A_{ref} is fixed. As shown in Fig. 4.3(a), integrating the error signal V_C before going to the oscillator can minimize this effect [39]. Assuming V_C linearly controls the real part of the poles in (4-3) i.e., $b(s)=\alpha V_C(s)$, the frequency response of the amplitude control loop $A(s)$ in Fig. 4.3(a) [39] as a function of the input reference $A_{ref}(s)$ can be described as

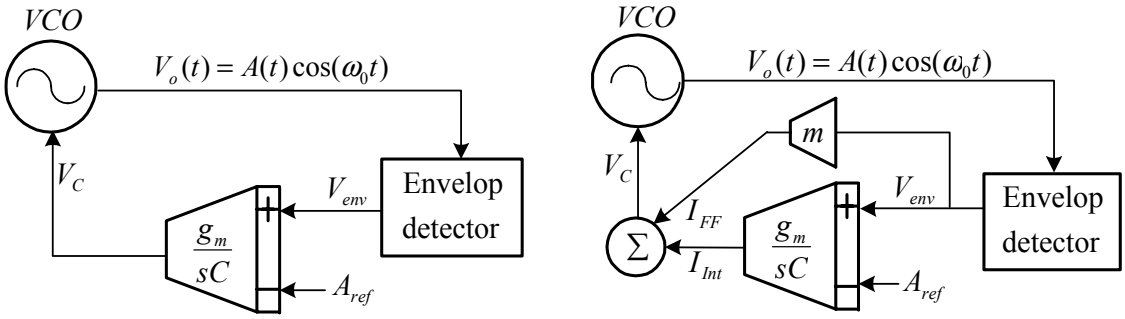


Fig. 4.3 Oscillator with amplitude regulation loop (a) unconditionally unstable AGC [39] (b) conditionally stable AGC using a feed forward path [40].

$$H(s) = \frac{A(s)}{A_{ref}(s)} = \frac{\frac{\alpha A_s}{2\tau_{Int}}}{s^2 - \frac{\alpha A_s \tau_{ENV}}{2\tau_{Int}} s + \frac{\alpha A_s}{2\tau_{Int}}} \tag{4-4}$$

where, A_s, τ_{Int} and τ_{ENV} are the oscillation amplitude at ω_0, the integrator and the envelop detector time constants, respectively.

The procedure of obtaining (4-4) is explained in detail in the next section. By observing the change of signs of the coefficients of the denominator of (4-4), based on the Routh-Hurwitz criteria [34] and [41], one can conclude the poles are located in the right half plane. This equation will be derived as a particular case of our proposed architecture in Section IV.

The loop in Fig. 4.3(a) can be made conditionally stable by introducing a feed forward path (m) as depicted in Fig. 4.3(b) and reported in [40]. Unfortunately, this scheme requires stringent limitations on m for stability purposes and degrades the phase noise of the oscillator by injecting the low frequency noise associated with the feedback loop to the control voltage V_C. This effect has been analyzed extensively in a bipolar

implementation of the amplitude control loop in [41]. Next, an alternative solution is proposed which overcomes the previous drawbacks.

4.3.1. *Proposed Loss-Control Feedback Loop*

Fig. 4.4 shows the proposed LCF loop scheme. This technique not only relaxes the stability requirement imposed on the local feedback *F*, to be discussed next, but it also generates a low pass filter which reduces and bounds the low frequency noise effect of the LCF loop.

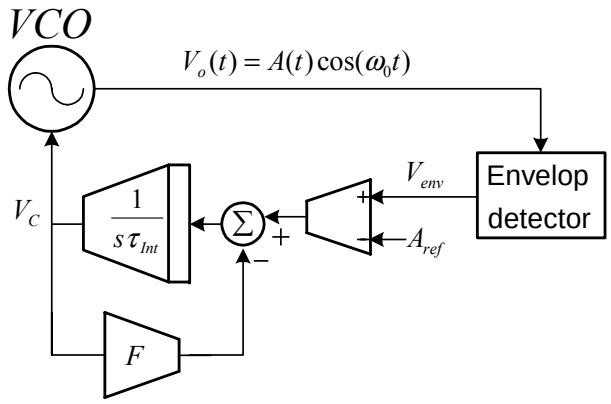


Fig. 4.4 Proposed loss control feedback loop for amplitude tuning.

With regard to the selective properties of the resonant circuit of the oscillator, i.e. the first order harmonic component markedly predominates over the other harmonics, we assume the solution in the form $v_{out}(t)=A(t)\sin(\omega t+\varphi)$, where $A(t)$ is the waveform of the envelope with the steady state amplitude of $A(\infty)=A_s$. Substituting $v_{out}(t)$ in (4-2) results in

$$\begin{aligned}&\left(\frac{d^2A(t)}{dt^2}-\omega^2A(t)\right)\sin(\omega t)+2\omega\frac{dA(t)}{dt}\cos(\omega t)\\&-\frac{a_1-G_P}{C}\left(1-\frac{3a_3}{a_1-G_P}A(t)^2\sin^2(\omega t)\right)\left(\frac{dA(t)}{dt}\sin(\omega t)+\omega A(t)\cos(\omega t)\right)\\&+\omega_0^2A(t)\sin(\omega t)=0\end{aligned} \tag{4-4a}$$

Leaving out all the components other than the fundamental frequency in (4-4a), yields the following coefficients for sine and cosine terms, which must be identically zero.

$$\left(\frac{G_P - a_1}{C} + \frac{3a_3}{4C}A(t)^2\right)\frac{dA(t)}{dt} + \left(\omega_0^2 - \omega^2\right)A(t) = 0 \tag{4-5a}$$

$$2\frac{dA(t)}{dt} + \left(\frac{G_P - a_1}{C} + \frac{3a_3}{C}A(t)^2\right)A(t) = 0. \tag{4-5b}$$

The steady state oscillation amplitude A_s can be obtained from (4-5b) by setting $dA(t)/dt=0$. Thus, the first term in (4-5b) becomes zero which means that in the second term either $A(t)$ or the expression inside the brackets should be zero. Having $A(t)=0$ results in no oscillation, thus the expression inside the brackets in (4-5b) can be solved for the steady state amplitude A_s which results in $A_s = 2\sqrt{\frac{a_1 - G_P}{3a_3}}$. However, the transient behavior of $A(t)$ before reaching the steady state can be analyzed by solving (4-5b) for $A(t)$.

$$A(t) = A(t_0)\exp\left(-\frac{1}{2}\int_{t_0}^{t} b(\tau)d\tau\right) = A(t_0)\left(1 - \frac{1}{2}\int_{t_0}^{t} b(\tau)d\tau + \frac{1}{8}\left(\int_{t_0}^{t} b(\tau)d\tau\right)^2 + \Lambda\right) \tag{4-6}$$

where, $b(\tau) = \frac{G_P - a_1}{C} + \frac{3a_3}{C}A(\tau)^2$.

For oscillation amplitude close to the stable amplitude $A(t_0)=A_s$, the term $b(t)$ in (4-6) approaches zero and thus, the corresponding exponential term in (4-6) can be approximated by its first two terms of the Taylor expansion:

$$A(t) \approx A_s - \frac{A_s}{2}\int_{t_0}^{t} b(\tau)d\tau. \tag{4-7}$$

Note that $b(t)$ is a function of $A(t)$ and ω_0, and since $A(t)$ is controlled by V_C (see Fig. 4.6), in the frequency domain $b(t)$ is a function of s and v_c. Therefore, in the frequency domain, (4-7) can be expressed as:

$$A(s) = -\frac{A_s}{2s} b(s, v_c) . \tag{4-8}$$

The exact dependence of b on v_c in (4-8) depends on the implementation of the oscillator, but for small signal analysis we may assume they are linearly dependent [40].

$$b(s) = \alpha v_C(s) . \tag{4-9}$$

To investigate the small signal behavior of the LCF loop in Fig. 4.4, the envelope detector's output ($V_{ENV}(t)$) is assumed to always be a delayed version of $A(t)$. This is due to the fact that the source follower behaves like a low pass filter with the time constant of τ_{ENV} . Thus, in frequency domain the transfer function of the envelope detector can be expressed as:

$$\frac{V_{ENV}(s)}{A(s)} = \frac{1}{1 + s\tau_{ENV}} \cong (1 - s\tau_{ENV}) \tag{4-10}$$

where, τ_{ENV} is the time constant of the envelope detector.

Note that in the amplitude control loop in Fig. 4.4, $v_C(s)$ can be expressed as $\frac{A(s)(1 - s\tau_{ENV}) - A_{ref}}{F + s\tau_{Int}}$. Thus, using (4-8) and (4-9), the frequency response of the amplitude of the LCF loop can be found as

$$A(s) = \frac{\frac{\alpha A_s}{2\tau_{Int}} A_{REF}(s)}{s^2 + \frac{1}{\tau_{Int}}\left(F - \frac{\alpha A_s \tau_{ENV}}{2}\right)s + \frac{\alpha A_s}{2\tau_{Int}}} = \frac{K A_{ref}(s)}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4-11}$$

where, τ_{Int} is the time constant of the integrator in Fig. 4.4.

To guarantee the stability of (4-11), the coefficients of the denominator should have the same polarity, thus the following requirement for F can be obtained to ensure stability of the proposed LCF loop in Fig. 4.4.

$$F > \frac{\alpha A_s \tau_{ENV}}{2}. \tag{4-12}$$

Equation (4-12) represents a second order system with a the damping factor of $\xi = (F - \frac{\alpha A_s \tau_{ENV}}{2}) / \sqrt{2\alpha A_s \tau_{Int}}$ which for a critically damped (Butterworth like) step response, i.e., $\xi = 1/\sqrt{2}$, the exact value of F can be found as

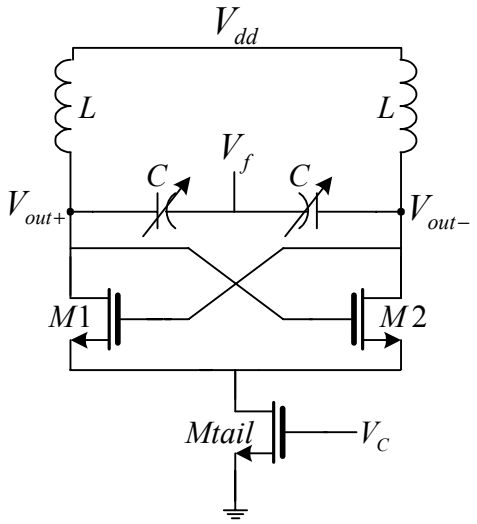


Fig. 4.5 LC oscillator core in Fig. 4.11.

$$F = \frac{\alpha A_s \tau_{ENV}}{2} + \sqrt{\alpha A_s \tau_{Int}} \quad ; \quad \text{For } \xi = 1/\sqrt{2}. \tag{4-13}$$

In the case of the LC oscillator shown in Fig. 4.5, which is modeled in Fig. 4.1, the parameter α in the above expressions can be derived using the characteristic equation of the circuit.

$$s^2 + \frac{G_P - G_{neg}}{C} s + \frac{1}{L_P C} = 0 \,. \tag{4-14}$$

Comparing (4-14) with (4-3) reveals that $b=(G_P-G_{neg})/C$ which for $G_{neg} = \frac{1}{2}\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{tail}}$ and $I_{tail} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{tail}(V_C - V_{th})^2$ yields the following expression for α (see (4-9)):

$$\alpha \approx \frac{\mu_n C_{ox}}{2\sqrt{2C}}\sqrt{\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_{tail}} \tag{4-15}$$

where, $(W/L)_1$ and $(W/L)_{tail}$ are the W/L ratios of M_1 and M_{tail} in Fig. 4.5, respectively.

For typical values of $\alpha=2\times10^9$, $A_s=0.1$V and $\tau_{ENV}=2$nsec, (4-12) results in $F>0.2$. Observe from (4-11), a higher value of F yields a higher damping factor ξ and thus less overshoot in the step response of the loop. However, since in terms of circuit implementation, F represents the ratio of two different transconductance's, a higher F results in increased power consumption.

4.3.2. *Transient Response of the Proposed LCF Loop*

The effect of F on the transient response of the amplitude control loop in Fig. 4.5 can be explored using the model depicted in Fig. 4.6. The envelope detector in Fig. 4.6 is considered ideal. The parameter F in this model is equal to the ratio of G_{m2}/G_{m1}.

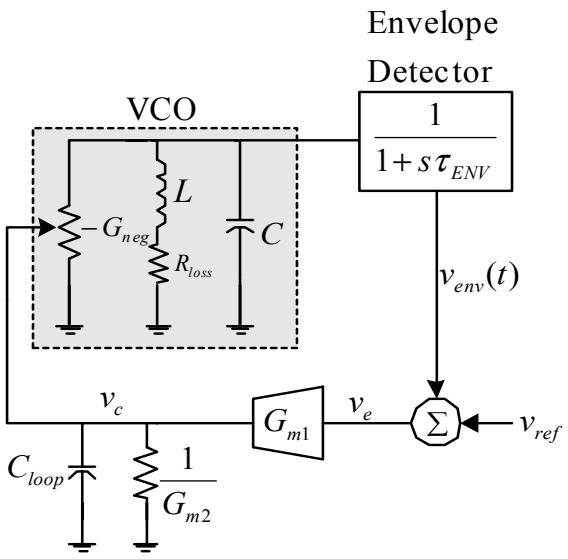


Fig. 4.6 Macro model of the proposed LCF of Fig. 4.4.

A step input is assumed for the reference signal $A_{ref}(t)$ so that it changes from A_{r0} to A_{r1} at t=0, and the corresponding steady-state oscillation amplitudes are A_{01} and A_{02}, respectively. The control voltage v_c in Fig. 4.6 can be expressed as

$$v_c = \frac{G_{m1}}{G_{m2}} v_e - \frac{C_{loop}}{G_{m2}} \frac{dv_c}{dt}. \tag{4-16}$$

where, $v_e = A(t) - A_{02}$.

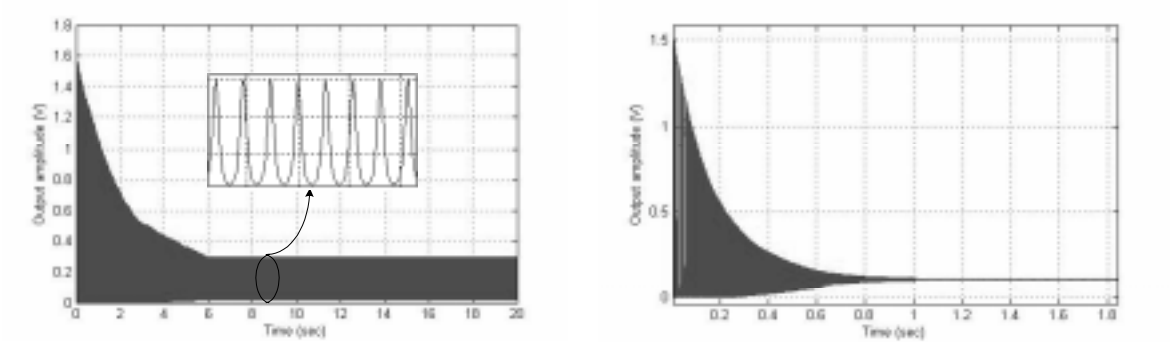
From (4-6) it can be found that

$$\frac{dA(t)}{dt} = -\frac{b(t)}{2} A(t). \tag{4-17}$$

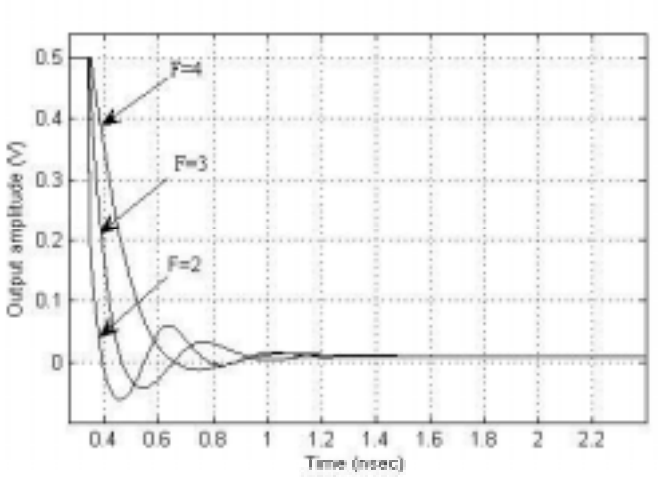
By substituting (4-16) and (4-17) in (4-9), the equation governing the transient behavior of the amplitude dynamics of the system in Fig. 4.6 can be solved.

$$\frac{d}{dt}\left(\frac{\dot{A}}{A}\right) + \frac{1}{\tau_{Int}}\left(\frac{\dot{A}}{A}\right) + \frac{\alpha G_{m1}}{2C_{loop}}\left(A(t) - A_{02}\right) = 0. \tag{4-18}$$

where, $\dot{A} = dA(t)/dt$ and $\tau_{Int} = C_{loop}/G_{m2} = C_{loop}/(FG_{m1})$.



(a) (b)



(c)

Fig. 4.7 Basic amplitude response of the (a) conventional control loop in Fig. 4.3(a); (b) control loop in Fig. 4.3(b); (c) proposed control loop of Fig. 4.4.

The numerical solutions of (4-18) for A_{02}=0.1V and for both the proposed (see (4-11) and Fig. 4.4) and the reported amplitude control loops in Fig. 4.3 are shown in Fig. 4.7. As Fig. 4.7(a) shows, removing the local feedback F, which corresponds to $\tau_{Int}=\infty$, results in an unstable system (see Fig. 4.3(a)). By using (4-12) and following the above procedure used to derive (4-18), the poles of the unstable system are determined to be located at $\pm j\sqrt{\alpha G_{m1} A_s /(2C_{loop})}$.

In a similar way, the step response of the amplitude control loop in Fig. 4.3(b) is shown in Fig. 4.7(b). By selecting proper value of the feed forward m in this scheme, the

loop can be stable. However, there is a large settling time at the output, which shows the behavior of a damped oscillation in the form of $e^{-\xi t}\sin\omega_f t$. In the previous behavioral expression for the output, $\xi=1/(2L(G_P-G_{neg}))$ and $\omega_f = \sqrt{\omega_0^2 - \xi^2}$ are the damping factor and the natural frequency of free oscillations in the circuit of Fig. 4.1.

In Fig. 4.6, when the local feedback $F=C_{loop}/(G_{m1}\tau_{Int})$ is present, the system becomes stable primarily due to a non-zero τ_{Int}. Depending on the value of $\tau_{Int,}$ the step response of the system can change from being over damped (small τ_{Int}) to under damped (large τ_{Int}). Assuming $G_{m1}=1m/\Omega$, the transient response of (4-18) for three different values of F has been shown in Fig. 4.7(c). Note that higher F, which corresponds with higher G_{m2}, results in smaller τ_{Int} and thus smaller settling time. While increasing G_{m2} improves the settling time of the transient response and reduces the noise associated with G_{m2}, it also increases power consumption. The power consumed by G_{m2} can be expressed as:

$$P_{diss} = V_{dd} I_{G_{m2}} = \frac{V_{dd}}{2\mu C_{ox}\left(\frac{W}{L}\right)_2} G_{m2}^2 . \tag{4-19}$$

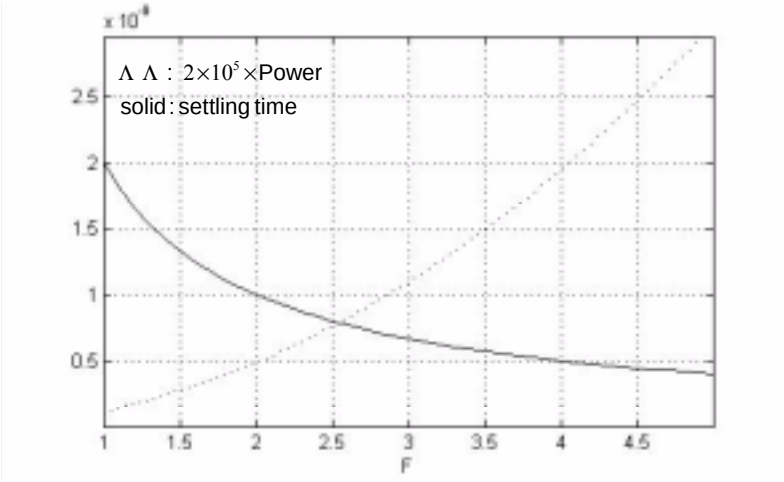


Fig. 4.8 Power consumption of G_{m2} cell and settling time as a function of F.

An optimum value of G_{m2} requires a trade off between the settling time of the step response of the amplitude control loop depicted in Fig. 4.7(c), and the power consumption described in (4-19). These two parameters, for C_{loop}=2pF and $(W/L)_2$=50, as a function of G_{m2} are plotted in Fig. 4.8.

4.3.3. *Circuit Implementation of the Proposed LCF Loop*

Fig. 4.9 shows the fully integrated circuit implementation of the proposed LCF loop together with the LC oscillator. Cross-coupled transistors M_3-M_4 compose the negative transconductance $-G_{neg}$ which is controlled by the tail current source (M_5). The implemented inductors use the top metal layer and are designed and optimized using AISTIC [42]. The varactors are accumulation-mode PMOS capacitors, and are realized using multiple simple PMOS transistors connected in parallel with drain and source connected to ground. The control voltage V_f at the bulk terminal modifies the capacitance value of each varactor.

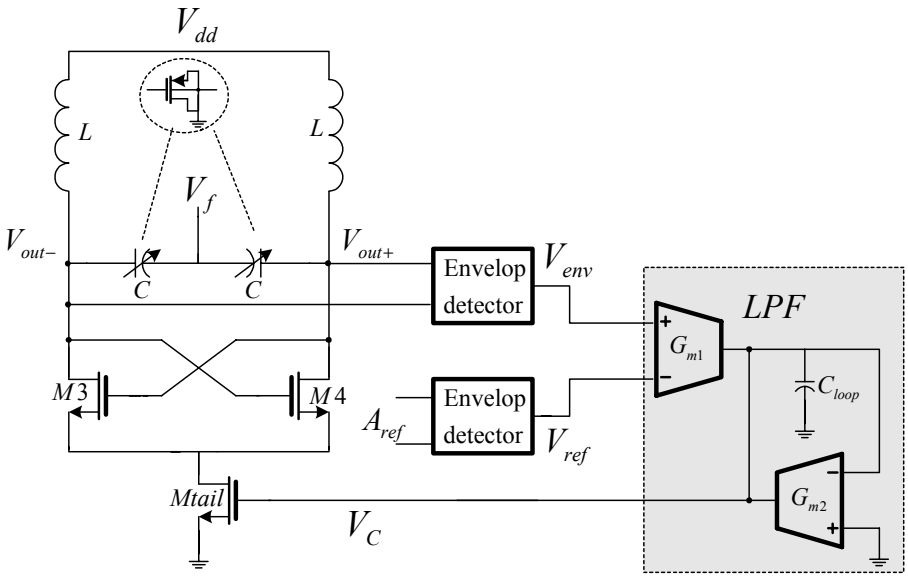


Fig. 4.9 Fully differential implementation of the proposed loss control feedback loop.

Fig. 4.10 depicts the circuit used as the envelop detector [43]. The transfer function of this circuit is derived in (4-10). Assuming that the DC voltage at the inputs of ME1-ME2 are high enough to drive these transistors in the saturation region, then this circuit is just a simple source follower and can detect any signal amplitude as long as it doesn't push the transistors to leave the saturation region. The main issue associated with the envelop detector is the trade-off between its speed and accuracy. Increasing its bias current results in a faster transient response, while decreasing it improves the accuracy of the output voltage. The total parasitic capacitance at the output node is represented by C_{ENV}. G_{m1} and G_{m2} cells used in Fig. 4.9 are implemented based on the simple three-current mirrors OTA's [44], and their ratio is determined by the stability factor $F=G_{m2}/G_{m1}$. A total capacitance of 2pF is used to implement C_{loop}.

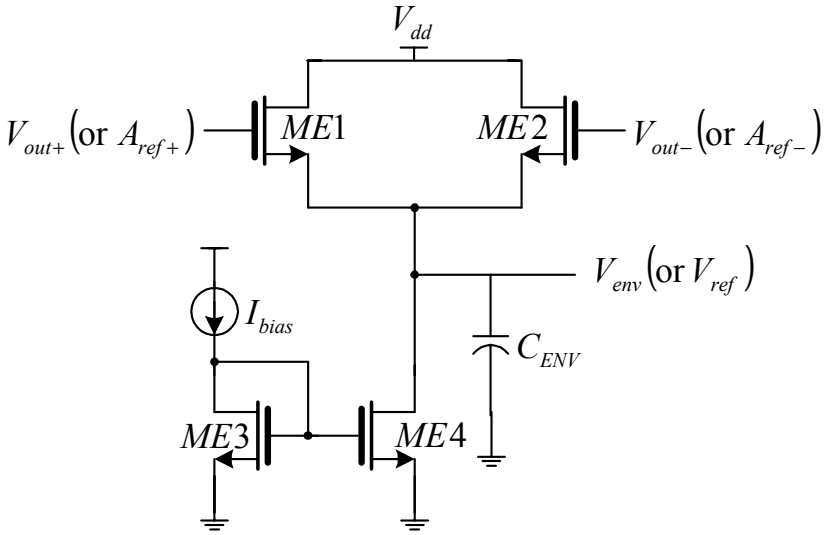


Fig. 4.10 Schematic of the envelop detector.

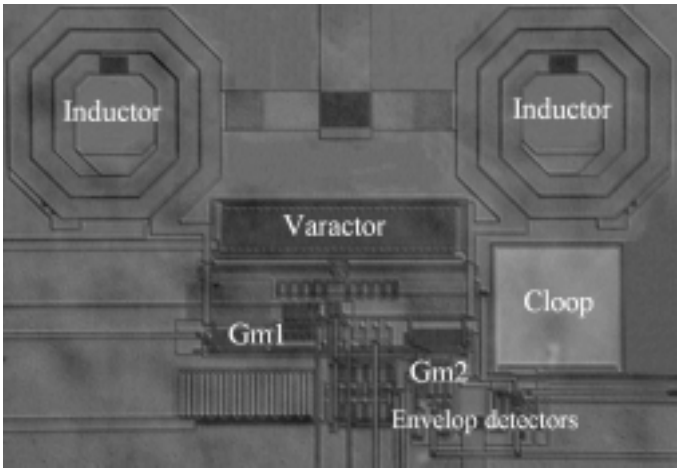


Fig. 4.11 Chip microphotograph.

4.4. Experimental Results

A test chip has been fabricated in the TSMC 0.35μm CMOS process available through, and thanks to, MOSIS. The chip micro photograph is shown in Fig. 4.11. The entire oscillator and the control loop, along with additional on-chip buffers, occupy an area of 0.038mm^2 and 0.008mm^2, respectively. All the measurements described in this section include the effect of the on-chip buffers with a measured attenuation of -20dB at 2.2GHz (for 50Ω termination). The oscillator operates from a single 2.8V supply voltage, and consumes 8mA current. The oscillator operates from a minimum power supply voltage of 1.8V up to 2.8V. The measurement setup for the phase noise of the LC VCO is shown in Fig. 4.12.

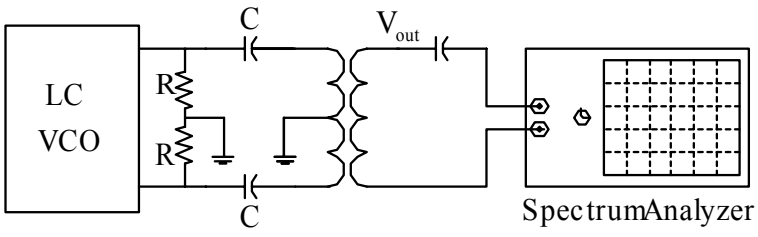


Fig. 4.12 Measurement setup for phase noise

Fig. 4.13 shows the measured phase noise for an oscillation frequency of 2.3GHz under the stable condition of F=2. The phase noise at an offset frequency of 1MHz from the carrier is -125dBc/Hz. Note the feedback factor F in Fig. 4.4 can be changed using G_{m2} in Fig. 4.9. Reducing F to a value smaller than the critical value in (4-14) makes the LCF loop unstable. To verify this statement, Fig. 4.14 shows the measured phase noise of the unstable LCF loop, i.e. F=0. Due to the instability of the loop, the control voltage V_C is changing and it modulates the amplitude and frequency of oscillation which changes the zero crossing points and results in the deterioration of the phase noise performance.

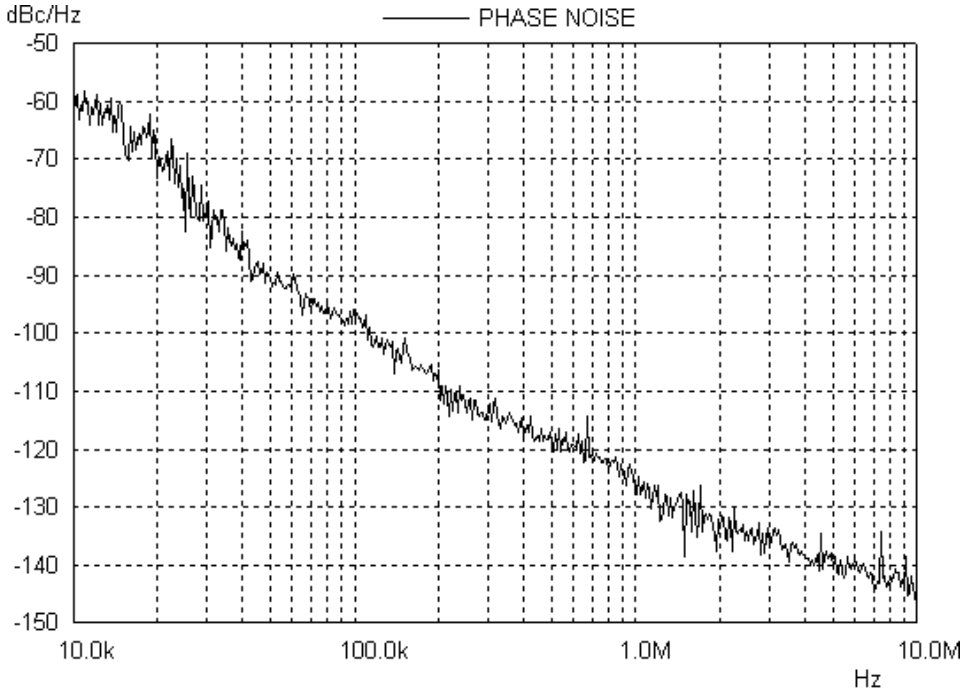


Fig. 4.13 Measured phase noise of the VCO at 2.3GHz under stable LCF loop condition, i.e., F=2.

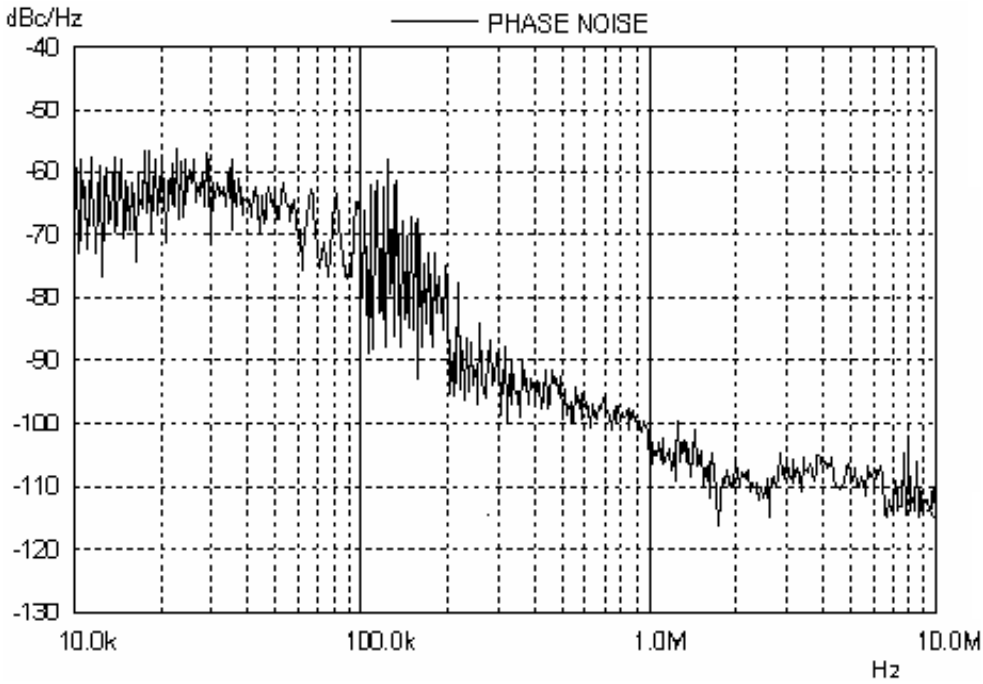


Fig. 4.14 Measured phase noise of the VCO at 2.3GHz under unstable LCF loop condition, i.e., F=0.

The robust and stable step response of the proposed scheme is verified through measurement and this result is shown in Fig. 4.15. This figure shows the transient behavior of the control voltage V_C for a reference amplitude step from 2.8V to 2.2V. The result shows a very close match with the behavioral model depicted in Fig. 4.7(c).

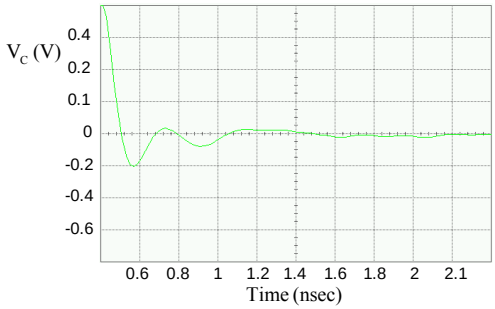


Fig. 4.15 Measured AC transient response of the feedback loop for F=2 (DC level=1.8V and A_{ref} is a pulse wave with frequency of 20MHz).

Fig. 4.16 shows the measured oscillation frequency range versus the tuning voltage V_f as a function of the power supply. The results show the frequency range is fairly independent of the supply voltage and can vary from 2GHz to 2.5GHz.

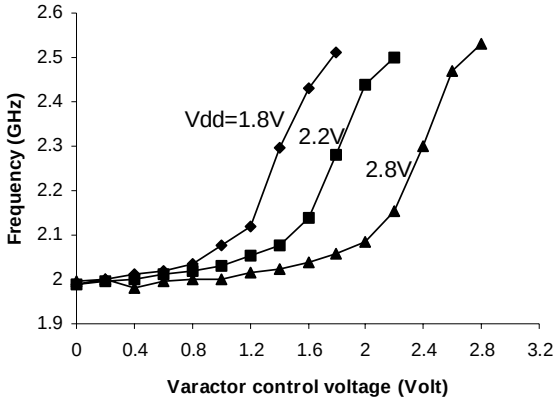


Fig. 4.16 Experimental oscillation frequencies versus varactor control voltage as a function of the power supply.

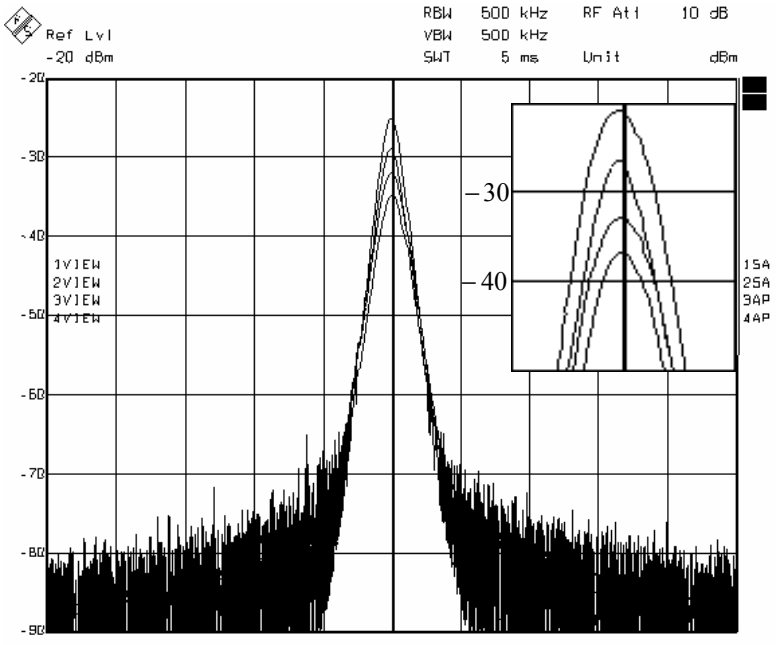


Fig. 4.17 Measured oscillation amplitude (-25, -29, -33, -36) dB for four different reference voltages (from bottom to top: 1.4V, 1.9V, 2.1V and 2.5 V).

The oscillation amplitudes for four different reference voltages are measured and the results are shown in Fig. 4.17. By applying different reference amplitudes, the control voltage V_C in Fig. 4.9 changes. Under this condition, the variation of the oscillation amplitude versus V_C is plotted in Fig. 4.18. The output amplitude shows a monotonic behavior with respect to the bias voltage of the tail current. Note that the level of the signal at the output already contains the -20dB attenuation due to the output buffer.

Fig. 4.18 also shows the HD3 of the output amplitude, as well as the measured phase noise at 1MHz offset from the carrier frequency, as a function of the control voltage V_C. At lower control voltages, the oscillation amplitude is lower and the phase noise is relatively poor, but the HD3 is higher primarily due to the smaller voltage swing across the LC tank. At very high values of the control voltage, the tail current transistor (M_{tail}) moves to the triode region and this leads to larger noise sources in the tank. The increased noise in the tank degrades both phase noise and the HD3. The optimum point in this figure, in terms of the lowest phase noise value, occurs at a bias voltage around 2V. At this bias, the variation of the oscillation frequency with respect to the tail current fluctuations is minimum.

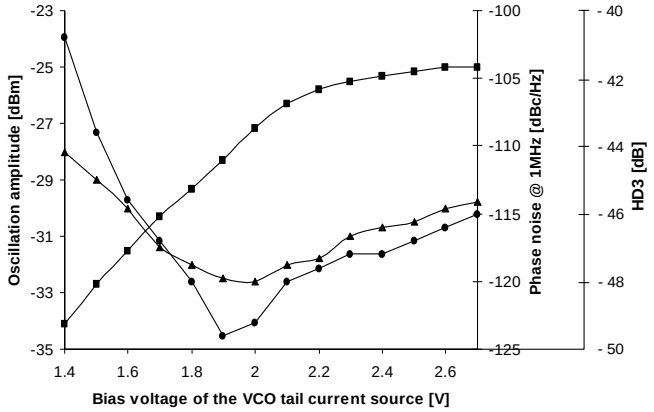


Fig. 4.18 Measured oscillation amplitude (■), phase noise (●) and HD3 (▲) vs. the control voltage of the tail current source (V_C in Fig. 4.9).

4.5. Quality Factor Tuning of LC Filters

The tuning techniques can be classified into two categories: indirect (master-slave) tuning and direct tuning. Indirect tuning was the first technique developed for real time tuning of continuous time filters [45]-[46]. As shown in Fig. 4.19, indirect tuning uses a master as the plant in the tuning control system. The control loop tunes the master in such a way that certain signals generated by the master lock to the references. The resulting control signals are then used to tune both the master and slave filters.

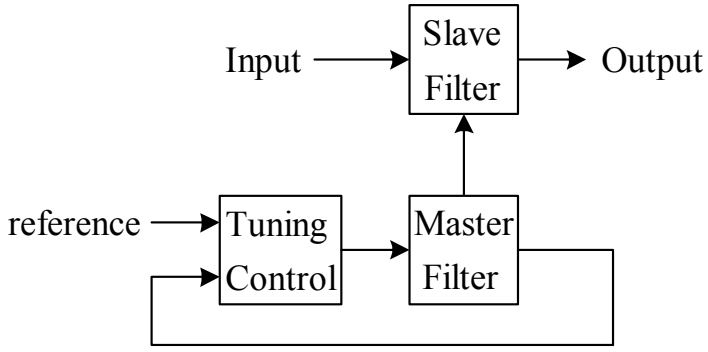


Fig. 4.19 Indirect (master-slave) tuning scheme

Direct tuning was the first technique proposed to achieve better tuning accuracy than indirect tuning [47]. The basic concept behind direct tuning is shown in Fig. 4.20. Here the filter itself becomes the plant in the tuning control system, and it is periodically taken away from the signal path for tuning. Hence, the tuning accuracy does not rely on matching and is much improved.

Depending on whether we use a filter or an oscillator as the plant in the tuning system, we have voltage-controlled filter (VCF) tuning [45]-[50] and voltage-controlled oscillator (VCO) tuning [51]-[54].

Because VCF tuning needs a reference signal with low harmonic content and a phase detector having low offsets, it is very difficult to realize it at GHz frequencies. Furthermore, for *Q*-enhanced LC filters, automatic tuning is more difficult than for Gm-C filters because the filter's critical frequencies depend on the passive devices' values and are not as easily controlled as Gm to C ratio in Gm-C filters.

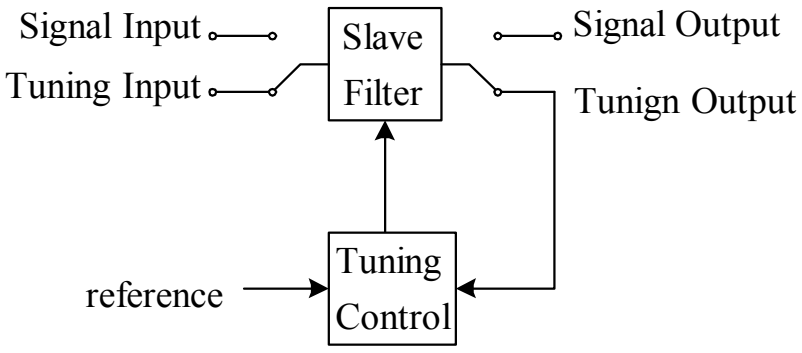


Fig. 4.20 Direct tuning scheme.

In general, the VCO-based tuning has the advantage over the VCF-based system that no input reference is needed. In addition, since the amplitude and phase of a VCO are, theoretically, independent thus, the *Q*-tuning loop and frequency tuning loop do not interfere. Unlike the VCO-based tuning system, the amplitude of the VCF's output signal varies with frequency, thus the *Q*-tuning loop heavily relies on the accuracy of the frequency tuning loop. However, a problem of the VCO-based tuning system is that the inherent nonlinearity of the VCO affects the accuracy of the *Q*-tuning loop.

4.6. VCO-Based Q-tuning

The VCO-based *Q*-tuning scheme, shown in Fig. 4.21, has been successfully implemented for high order MMIC bandpass filters [55].

This technique assumes a 0dB pass band insertion loss for the cascaded equal LC resonators in the slave filter which mandates that their quality factors should be infinite. The exact value of G_{neg} for an infinite Q can be obtained from a master VCO with the same LC resonator of the filter so that its resonant frequency is equal to the center frequency of the filter.

An infinite Q, i.e. poles on the $j\omega$ axis, for the VCO means oscillation with constant, regulated amplitude. An automatic amplitude control (AAC) loop detects the oscillation amplitude and compares it with a dc reference voltage using an integrator whose output is the *Q*-control voltage. The dc reference voltage is chosen so that the oscillation amplitude is maintained at a level low enough to ensure a good matching between its tank characteristics and the slave filter. Next we are showing that the above

technique can be also used to tune the quality factor of a single LC band pass filter to finite values of Q.

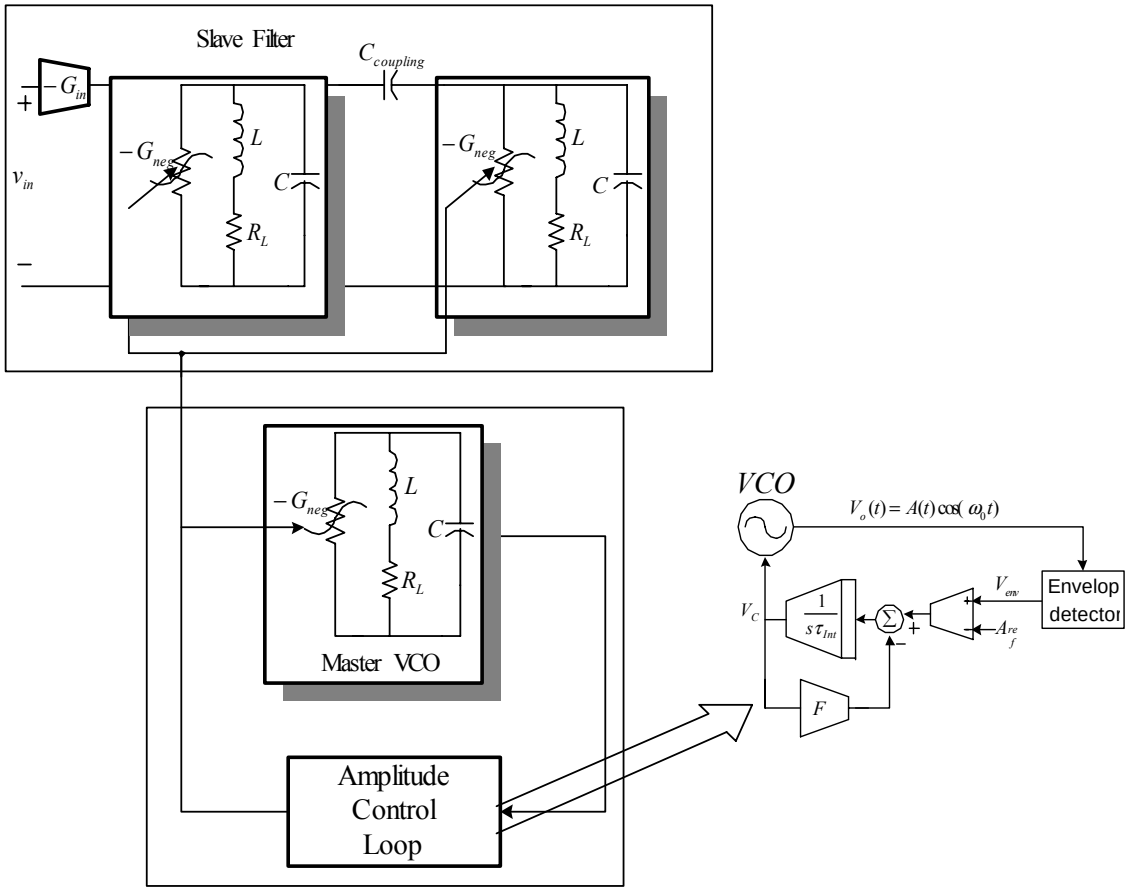


Fig. 4.21 VCO-based Q-tuning scheme.

4.6.1 *Principle of Operations*

Fig. 4.22(a) shows a second order LC resonator which can be considered as the slave filter in Fig. 4.20 but with only one resonator. Fig. 4.22(b) shows the master VCO used in Fig. 4.21. The quality factor of the Q-enhanced LC resonator [56], shown in Fig. 4.22(a), in which the resistive loss of the tank has been compensated by adding the negative transconductance of G_{neg} at the resonance frequency can be expressed as

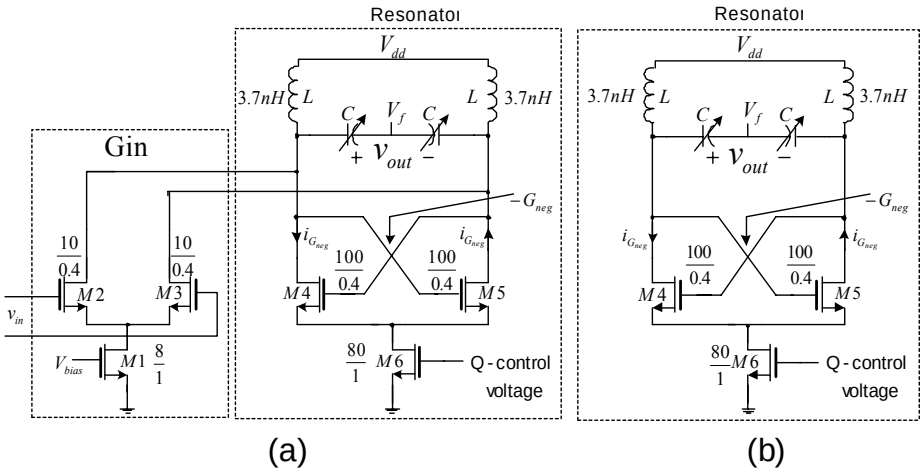


Fig. 4.22 (a) *Q*-enhanced LC filter (b) LC VCO

The quality factor of the *Q*-enhanced LC resonator, shown in Fig. 4.22(a), in which the resistive loss of the tank has been compensated by adding the negative transconductance of G_{neg} at the resonance frequency can be expressed as

$$Q = \frac{1}{G_P - G_{neg}} \sqrt{\frac{C}{L}}. \tag{4-20}$$

where, $G_P=(Q_0^2 R_L)^{-1}$ and Q_0 is the quality factor of the inductor. Typical values of Q_0 in 0.35μm CMOS technology are around 2.7 to 3.

Fig. 4.22(b) shows the circuit implementation of the master VCO which requires $|G_{neg}|>G_P$. The steady-state oscillation amplitude of this VCO has been derived in Section 3-2-1

$$A_s = 2\sqrt{\frac{|a_1| - G_P}{3a_3}} \quad , for\ |a_1| > G_P. \tag{4-23}$$

The above result for A_s can also be obtained using the describing-function technique [57]. The negative transconductance G_{neg} used in the LC tank of the filter behaves more linear than the one used in the oscillator due to the fact that the LC tank in

the filter experiences a smaller voltage swing. This means that the characteristics of G_{neg} of the filter in (4-1) can be, in practice, approximated as $G_{neg} \approx |a_1|$. Thus, from (4-20) and (4-23) the following relation between the quality factor of the slave filter and the steady state oscillation amplitude A_s of the master VCO can be approximated as

$$|Q| \cong \frac{4}{3a_3 A_s^2}\sqrt{\frac{C}{L}}\,. \tag{4-24}$$

Observe from (4-24) that the quality factor of the filter can be tuned by changing the oscillation amplitude A_s of the VCO. The above analysis of the VCO-based Q-tuning scheme of the 2nd order LC filters are experimentally demonstrated next and the results are also applicable to the higher order MMIC filters [55].

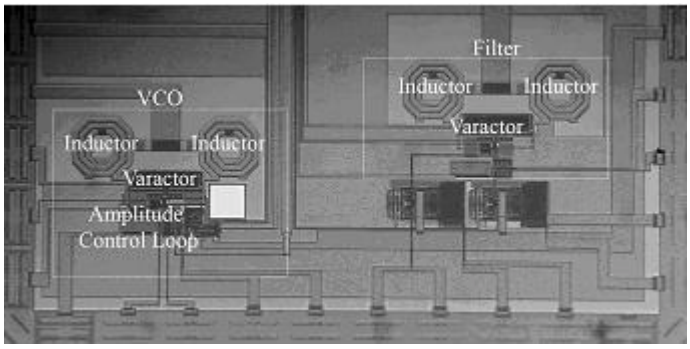


Fig. 4.23 Microphotograph of the VCO-based Q-tuning scheme.

4.6.2 *Experimental Results*

Fig. 4.23 shows the microphotograph of the fabricated prototype in a TSMC 0.35μm, 2-poly, 4-metal standard CMOS technology. The whole master VCO with the AAC loop along with the slave filter occupies an area of 0.08mm^2 and 0.066mm^2 and they consume 7mA and 8mA from a 1.8V supply voltage, respectively. A simple open drain output buffer is employed as the output buffer to drive the 50Ω load of the

instrument which shows a stand-alone attenuation of around -10dB at 2.25GHz. Fig. 4.24 shows the measurement setup to tune the quality factor of the LC filter.

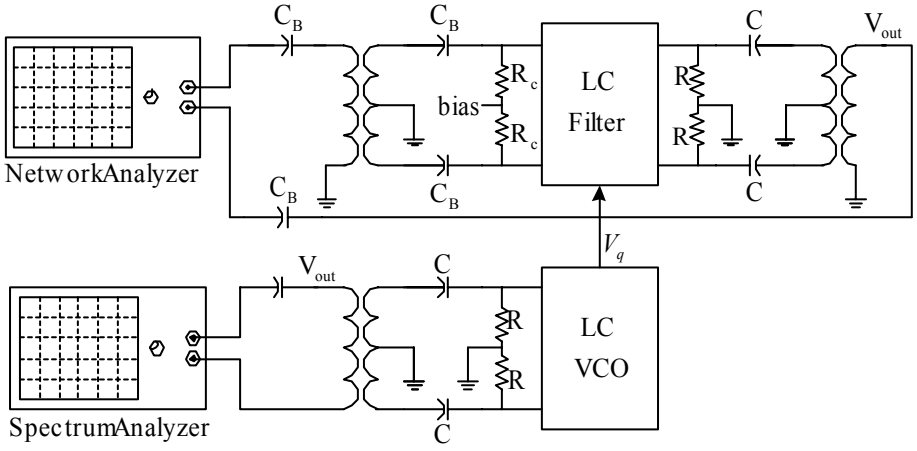


Fig. 4.24 Measurement setup to tune the quality factor of the LC filter.

The measured characteristic of the amplitude control loop of the VCO is shown in Fig. 4.25 which shows a monotonic behavior with respect to the input reference voltage. This figure also shows the measured settling time of the *Q*-control voltage for different input reference voltages which demonstrate the stable performance of the AAC loop. The spurious-free dynamic range (SFDR) of the tuned LC filter is also shown in this figure. Note that by increasing the input reference voltage the quality factor of the filter is decreased and thus the SFDR is increased.

Fig. 4.26 shows the measured amplitude response of the slave filter in the *Q*-tuning loop. This figure shows that by changing the dc voltage reference of the amplitude control loop the quality factor of the slave filter can be tuned from 110 to 300 while the total current consumption changes from 15mA to 13mA, respectively

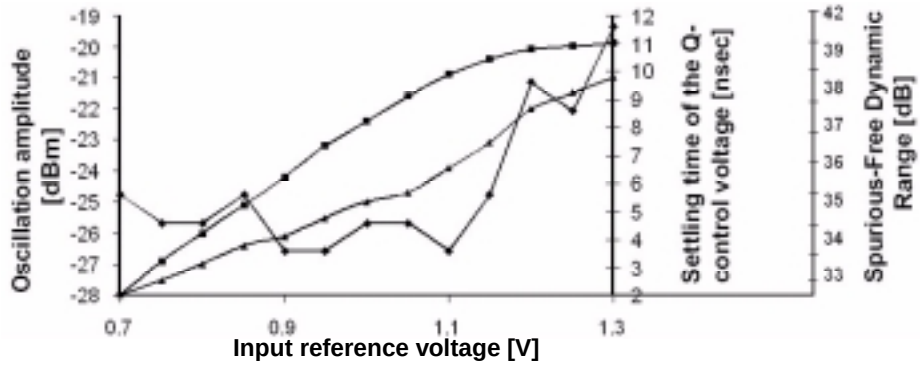


Fig. 4.25 Measured oscillation amplitude (■), settling time of the Q-control voltage (◆) and the SFDR (▲) of the tuned filter

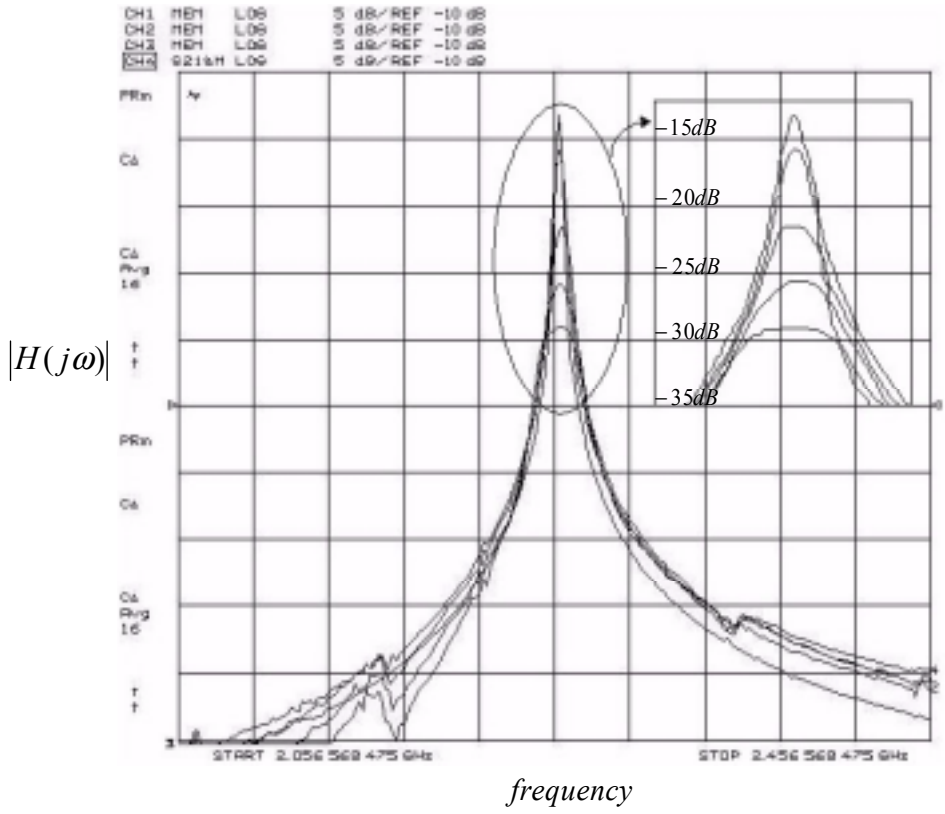


Fig. 4.26 Measured amplitude response of the LC filter for different values of Q. (5dB/div. vertical and 40MHz/div. horizontal)

CHAPTER V

AN ACCURATE AUTOMATIC QUALITY FACTOR TUNING SCHEME FOR 2nd-ORDER LC FILTERS

5.1. Introduction

Traditionally, gigahertz filters were implemented off-chip with lumped RLC components, but recently, the increasing demand for portable low-cost radio frequency front ends has motivated the emergence of integrated LC filters [58]. However, the implementation of integrated LC filters continues to present a challenge. The low quality factor of on-chip inductors requires the introduction of active circuitry implementing a negative resistance to compensate for the losses associated with the inductance [59]. Furthermore, the large unpredictable variations in component values and parasitics of monolithic implementations produce large variations in the resonance frequencies and filter quality factors. These variations make the filter completely useless unless some kind of tuning can be done after fabrication. Even in this scenario, the variations in temperature and operating conditions make it necessary to include automatic tuning circuitry to have a practical commercial product.

Automatic frequency tuning schemes for LC filters have already been developed [58], [60] and [61]. They employ the same techniques used for G_m-C filters [62]-[66]. A master filter in a VCO configuration is used to sense the oscillation frequency and a PLL is used to lock the oscillation frequency of the VCO to the desired reference frequency. However, the quality factor (Q) tuning scheme of LC filters cannot follow the same

principles of *Gm-C* filters due to the lack of precise relation between Q and amplitude response at the center frequency.

This chapter introduces a technique for automatic tuning of the quality factor of the LC filters which relies neither on the phase information of the filter nor the exact value of the amplitude gain at the center frequency. The quality factor tuning is achieved based on the adjustment of the amplitude response of the filter at the center and one of the cut-off frequencies. Furthermore, since most of the information is processed at very low frequencies good accuracies are obtained. For example it can achieve an accuracy of 1.9% for Q=50. This technique is validated through experimental results. We will present a preliminary Q-tuning architecture to reach the final proposed stable architecture.

5.2. Automatic Quality Factor Tuning

5.2.1 *Existing Quality Factor Tuning Techniques*

The traditional Q-tuning schemes reported for G_m-C filters [64]-[69] are not applicable to LC filters mainly because most of them rely on the fact that $H(j\omega_0) = Q$. Currently, available Q-tuning schemes for high frequency LC filters manipulate the frequency response of the filter in a digital [70]-[73] or an analog [61] feedback loop.

In [70] the quality factor tuning is achieved by converting the LC filter to an oscillator and then varying the negative transconductance until the desired (stable) Q is achieved. However, this technique relies on the assumption that the variation of the negative transconductances in the filter and the oscillator is constant which is valid only if a relatively high quality factor inductor is used in the resonator.

In [71] the center frequency and the quality factor tuning are achieved by comparing the amplitude gain at three different frequencies. Low accuracy of the gain comparison at high frequencies and relying on the matching between the sampling times of the error signal at different frequencies are the main drawbacks of this technique.

In [72] a digital tuning scheme based on the phase comparison of the filter at different frequencies is presented. However, finite resolution of the needed frequency synthesizer, phase offset and parasitic poles and zeros of the filter limit its performance especially for high frequency applications.

The scheme presented in [73] is based on direct characterization of the complete frequency response of the filter, and it is not adaptable to automatic *Q*-tuning. Finally, the VCO-based *Q*-tuning approach presented in [61] is a great advance in the theory of automatic *Q*-tuning of LC filters. It varies the negative transconductance to tune a number of LC resonators to behave as ideal (loss-less) resonators based on a master-slave approach. However, the fact that the negative transconductance added to the LC resonators compensate the losses of the passive components only at one particular frequency imposes restriction on wider frequency range filters.

5.2.2 *Proposed Quality Factor Tuning Scheme*

We will present how the proposed tuning scheme evolved. The first proposal (Fig. 5.1) is the basis for the proposed scheme illustrated in Fig. 5.2. The approach presented in this work in principle achieves tuning of any arbitrary values of Q and amplitude gain A_0 at resonance. This approach uses information of the transfer function at two different frequencies. Assuming that these two frequencies are the center and one of the -3dB cut-off frequencies (ω_L), an iterative scheme to tune the Q and the gain of the filter at the

center frequency is proposed. Based on the fact that $|H(j\omega_0)| = A_0$ and $|H(j\omega_{3dB})| = A_0/\sqrt{2}$, the following results can be obtained.

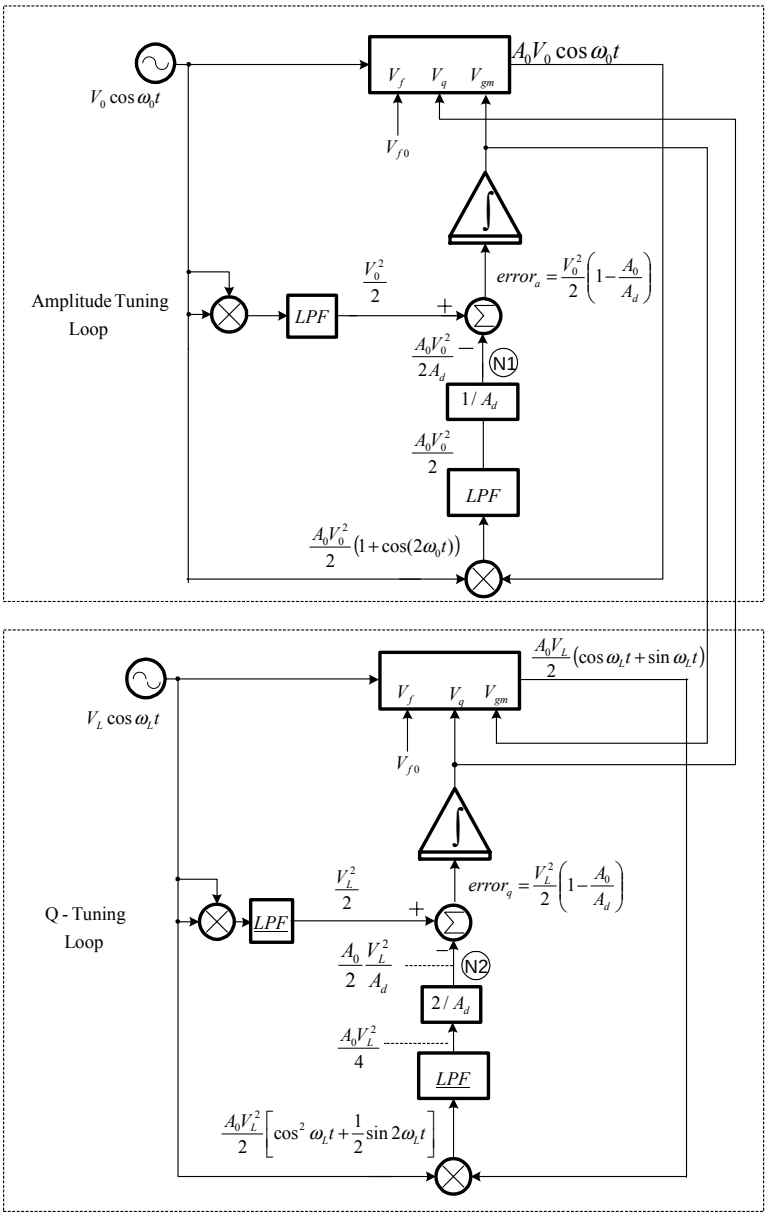


Fig. 5.1 Proposed schemes for amplitude and quality factor tuning.

$$\omega_L = \omega_0\left[\sqrt{1+\frac{1}{4Q^2}}-\frac{1}{2Q}\right] \approx \omega_0\left(1-\frac{1}{2Q}\right) \tag{5-1}$$

$$H(j\omega_L) = \frac{A_0}{2}(1+j) = \left|\frac{A_0}{2}\sqrt{2}\right| \angle 90 \tag{5-2}$$

Assuming that the input signal is $V_0\cos(\omega_0 t)$ and filter is tuned at the desired center frequency ω_0, the peak amplitude gain A_0 can be tuned using the amplitude tuning loop shown in Fig. 5.1. When the amplitude tuning loop settles to its steady state i.e., $error_a$=0, the peak amplitude gain A_0 at the center frequency is tuned to the desired amplitude gain of A_d. The steps to achieve A_d are indicated in Fig. 5.1.

Based on the -3dB cut-off frequency information, the quality factor of the filter can be tuned to the desired Q_d using the Q-tuning loop shown in Fig. 5.1. This technique relies on the fact that Re(H($j\omega_L$))=A_0/2. Note that according to (5-1) the output of the filter at ω_L has two components with equal amplitudes of A_0/2 but 90° phase difference. This explains the presence of sin($\omega_L t$) and cos($\omega_L t$) at the output of the filter in the Q-tuning loop in Fig. 5.1. The voltage V_q, which controls the quality factor of the filter, is adapted such that when the loop settles to its steady state, the equality $error_q = V_L^2\left(A_0 / A_d - 1\right)/2 \approx 0$ is satisfied.

Unfortunately the controls V_{gm} and V_q cause the two amplitude and Q-tuning loops interact. Assume the amplitude control loop is not yet calibrated such that the overall gain is too low, then the Q-tuning loop (even if V_q is correct) will see too small an output signal and think the Q is too large. V_q will then be erroneously adjusted to reduce the Q, This Q reduction (through V_q) will produce a further reduction in the gain A_0 (as can be deduced from equations (3-6) and (3-7)), resulting in an unstable tuning scheme. An extensive analysis, illustrated in subsection D, has been carried out to study the stability

of the preliminary proposed scheme in Fig. 5.1 and the results confirm that this technique is not stable.

5.2.3 *Proposed Stable Q-Tuning Scheme*

To fix the instability problem, the *Q*-tuning loop needs to know that the amplitude is too small (not yet settled). This can be accomplished by sending the amplitude error signal, $error_a$ in Fig. 5.1, to the *Q*-tuning loop. Fig. 5.2 shows the modified *Q*-tuning scheme.

The amplitude tuning loop of Fig. 4.2 remains the same as the one in Fig. 5.1. The computed amplitude error is defined as

$$error_a = \frac{V_0^2}{2}(1-\frac{A_0}{A_d}). \tag{4-3}$$

Equation (5-3) shows that when $error_a$=0 the amplitude gain A_0 at the center frequency is equal to the desired amplitude A_d. Note that at the same time the quality factor of the filter is tuned by the *Q*-tuning loop. Assume that the real part of the gain at the cut-off frequency ω_L is $A_L \neq A_0/2$ i.e., the output of the filter in the *Q*-tuning loop of Fig. 5.2 is $A_L V_0(\cos(\omega_L t)+\sin(\omega_L t))$. Thus, the error signal in this loop can be expressed as

$$error_q = error_a - \frac{V_L^2}{2}(1-\frac{A_0}{A_d}) = \frac{V_0^2}{2}(1-\frac{A_0}{A_d}) - \frac{V_L^2}{2}(1-\frac{2A_L}{A_d}). \tag{5-4}$$

Observe from (5-3), when $A_0=A_d$ the $error_q$ becomes zero if $A_L=A_0/2$ which means that the quality factor is appropriately tuned. Also note that the feedback signal FB in Fig. 5.2 does not degrade the performance of the *Q*-tuning loop due to mismatches in the input amplitudes V_0 and V_L. Provided that the amplitude tuning loop has been already settled to $A_0=A_d$ and the condition $V_0 \neq V_L$ holds, if $A_L=A_d/2$ then $error_q$ becomes zero which means that the quality factor is correctly tuned.

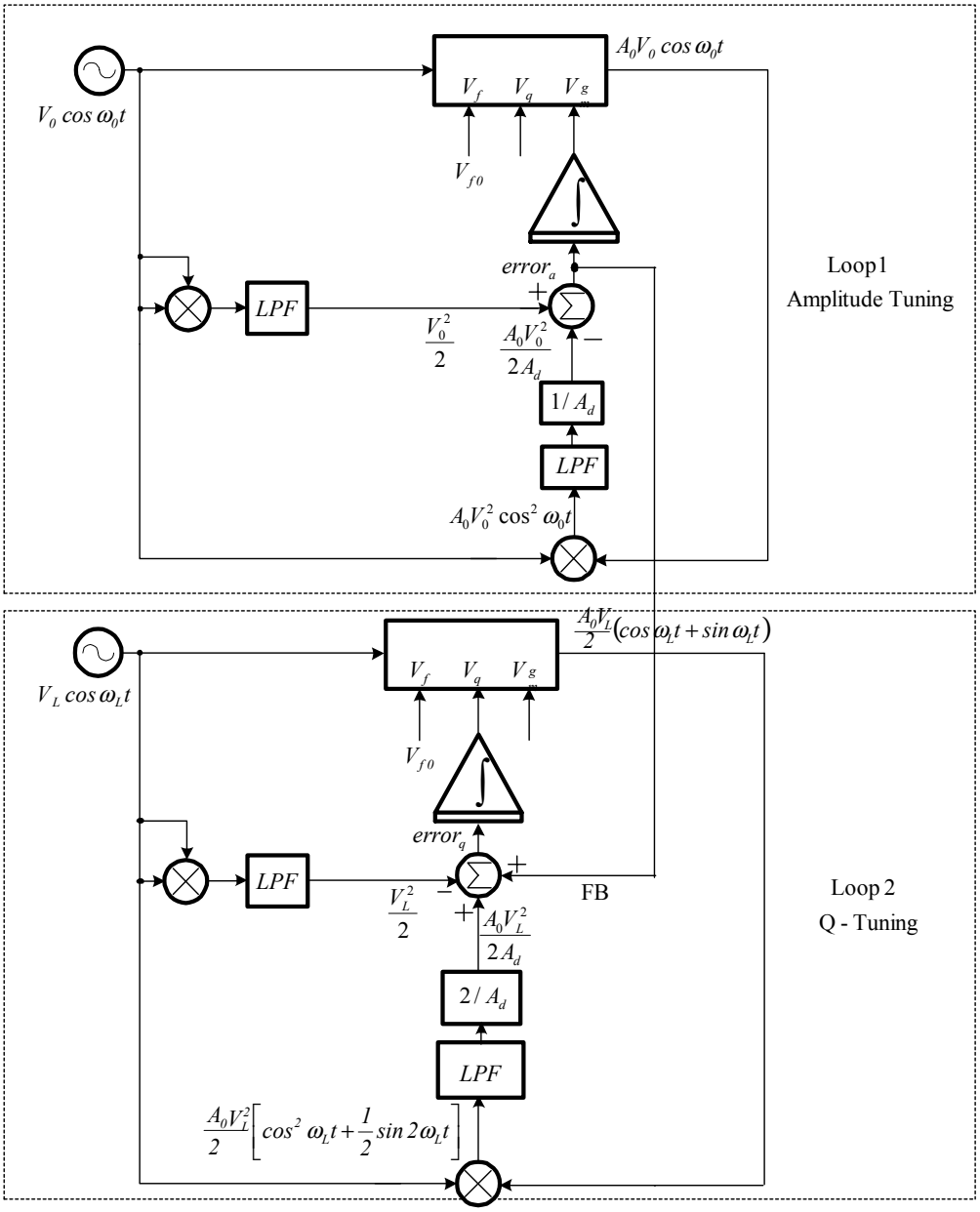


Fig. 5.2 Final stable *Q*-tuning scheme.

Let us study analytically the basics of the behavior of the *Q*-tuning loop. As explained above, the *Q*-tuning loop (both in Fig. 5.1 and Fig. 5.2) adapts the real part of the gain at the lower cut-off frequency to be $A_0/2$. Let us suppose the filter *Q* has not been already properly tuned so that the filter bandwidth deviates from the desired $\Delta\omega_d=\omega_0/(2Q_d)$ one to

the actual $\Delta\omega_a=\omega_0/(2Q_a)$. As a consequence, the actual real part of the gain at the applied ω_d (which is the target lower cut-off frequency), A_0/δ_q deviates from the target $A_0/2$ value. Using (3) and assuming $Q_d>>1$, the real part of $H(j\omega_d)$ can be expressed as

$$\mathrm{Re}\left(H(j(\omega_0-\Delta\omega_d))\right)=\frac{A_0}{1+\frac{\Delta\omega_d^2}{\Delta\omega_a^2}}=\frac{A_0}{\delta_q}. \tag{4-5}$$

From (5-5) and using that $\Delta\omega_d/\Delta\omega_a=Q_a/Q_d$, the actual factor δ_q can be related with the error of the quality factor tuning as

$$\delta_q=1+\frac{Q_a^2}{Q_d^2} \tag{5-6}$$

$$\frac{\Delta Q_a}{Q_a}=\frac{Q_d-Q_a}{Q_a}=\sqrt{\delta_q-1}-1. \tag{5-7}$$

When the Q-tuning loops in Fig. 5.1 and Fig. 5.2 reach their equilibrium states $\delta_q=2$ and therefore $Q_a=Q_d$. That is, the actual Q (Q_a) is equal to the desired Q_d.

5.3.4 *Stability Analysis*

Bellow, the stability of the Q-tuning schemes shown in Fig. 5.1 and Fig. 5.2 is analyzed assuming the second order LC filter shown in Fig. 3.3 is being tuned.

We can compute the target equilibrium values of the controlling voltages V_q and V_{gm} of the second order filter shown in Fig. 3.3. They can be deduced imposing that at the equilibrium $A_0=A_d$ and $Q=Q_d$, and using equations (3-6) and (3-7). The following solution for V_{q0} and V_{gm0} can be obtained.

$$V_{q0}=V_T+\frac{1}{\beta_q}\left(G_P-\frac{1}{Q_d}\sqrt{\frac{C}{L}}\right). \tag{5-8}$$

$$V_{gm0} = V_T + \frac{A_d}{2\beta_m}\left(G_P - \beta_q (V_{q0} - V_T)\right). \tag{5-9}$$

In the next, we will demonstrate that both tuning systems shown in Fig. 5.1 and Fig. 5.2 with the LC second order filter shown in Fig. 3.3 have the above values of V_{q0} and V_{gm0} as equilibrium point. However, the nature of the equilibrium points of both systems is very different from an stability point of view.

Let us first study the dynamics of the system shown in Fig. 5.1. The derivatives of the two control voltages V_{gm} and V_q in the amplitude and Q-tuning loops in Fig. 5.1 can be expressed as

$$\dot{V}_{gm} = \frac{V_0^2}{2}(1 - \frac{A_0}{A_d}) \tag{5-10}$$

$$\dot{V}_q = \frac{V_L^2}{2}(\frac{2A_0}{A_d \delta_q} - 1) \tag{5-11}$$

where, δ_q and A_0 are defined in (5-6) and (3-6), respectively.

Substituting δ_q and A_0 for their expressions in (5-6) and (3-6) and redefining variables (u=G_p-β_q(V_q-V_T), v=β_m(V_{gm}-V_T) and $\dot{V}_{gm} = \dot{v}/\beta_m$ and $\dot{V}_q = -\dot{u}/\beta_q$), equations (5-10) and (5-11) can be re-expressed as

$$\dot{u} = -K_L(\frac{4v}{A_d u}\frac{1}{1 + \frac{C}{LQ_d^2}\frac{1}{u^2}} - 1) \tag{5-12}$$

$$\dot{v} = K_0(1 - \frac{2v}{A_d u}) \tag{5-13}$$

where, $K_L = \beta_q V_L^2 / 2$ and $K_0 = \beta_m V_0^2 / 2$.

Equations (5-12) and (5-13) allow to identify $u_0 = \sqrt{C/L}/Q_d$ and $v_0 = A_d\sqrt{C/L}/(2Q_d)$ as an equilibrium point (which is the same equilibrium point defined by (5-8) and (5-9)). However, to find other equilibrium points the null isoclines of the system defined by $\dot{u}=0$ and $\dot{v}=0$ need to be obtained. Then using the phase portrait concept the qualitative behavior of the system given any initial condition can be determined [74].

The above technique has been applied to (5-12) and (5-13) for the following parameters: A_d=1, C=1.6pF, L=3.7nH, V_L=V_0=1, β_q=14.25m/Ω, β_m=1.425m/Ω and Q_d=10. The phase portrait of the system is plotted in Fig. 5.3.

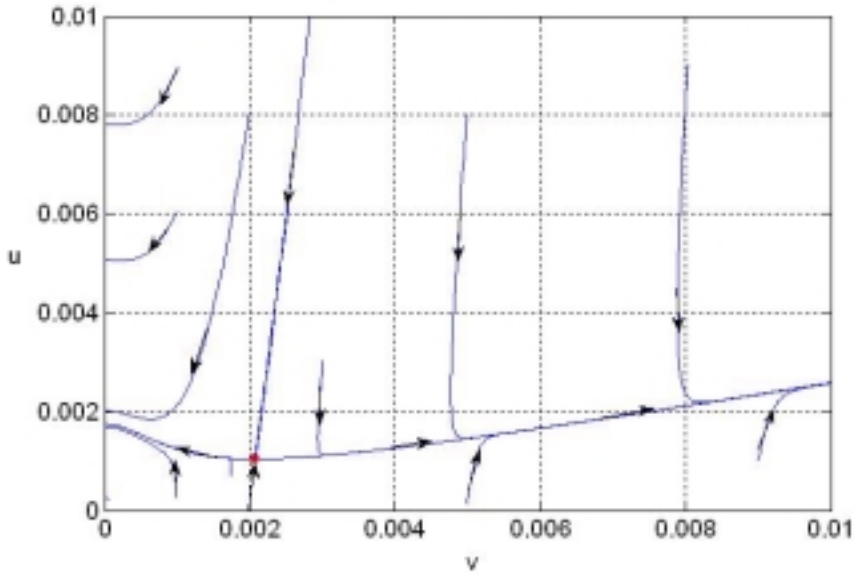


Fig. 5.3 Phase portrait corresponding to Fig. 5.1.

Observe that the equilibrium point in Fig. 4.3 is a saddle point which is stable only for one trajectory. However, the system is unstable for any other initial conditions in the state space. Note that form the null isoclines of the system there is another

equilibrium point corresponding with $u<0$ and $v<0$ which is not considered here as it is not a feasible solution.

The same approach described above has been also used to study the stability of Fig. 5.2. Since the amplitude tuning loop (Loop1) in both schemes of Fig. 4.1 and Fig. 5.2 are the same thus the expressions for $\dot{I}_{gm}$ and $\dot{v}$ remain intact. However, the expressions for $\dot{I}_q$ and $\dot{u}$ are changed to the following expressions.

$$\dot{I}_q = \frac{V_L^2}{2}\left(\frac{2A_0}{A_d\delta_q} - 1\right) + \frac{V_0^2}{2}\left(1 - \frac{A_0}{A_d}\right) \tag{5-14}$$

$$\dot{u} = -K_L\left(\frac{\frac{4v}{A_d u}}{1 + \frac{C}{LQ_d^2}\frac{1}{u^2}} - 1\right) - \frac{\beta_q K_0}{\beta_m K_L}\left(1 - \frac{2v}{A_d u}\right). \tag{5-15}$$

The same equilibrium point $u_0 = \sqrt{C/L}/Q_d$ and $v_0 = A_d\sqrt{C/L}/(2Q_d)$ can be identified from equations (5-14) and (5-15). Let us identify its stability behaviour using the phase-portrait concept. Fig. 5.4 shows the phase portrait of the system defined by (5-14) and (5-15) using the same filter parameters. This figure clearly shows that the equilibrium point is a stable node and the system is asymptotically stable for any given initial condition in the state space.

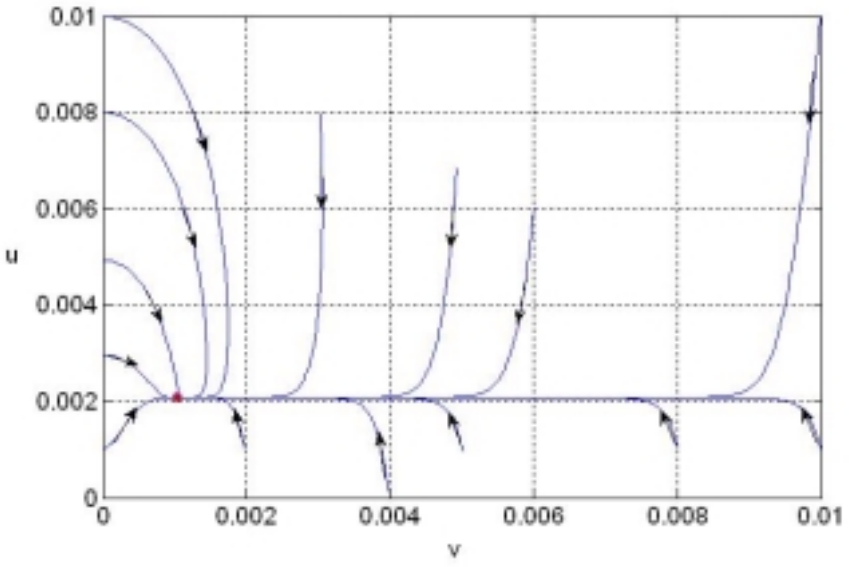


Fig. 5.4 Phase portrait corresponding to Fig. 5.2.

The behavioral performance of the previously proposed tuning schemes has been examined using SIMULINK and their stability properties have been confirmed through SIMULINK simulations. The conceptual block diagram of the second-order LC bandpass filter used in the SIMULINK simulations is shown in Fig. 5.5.

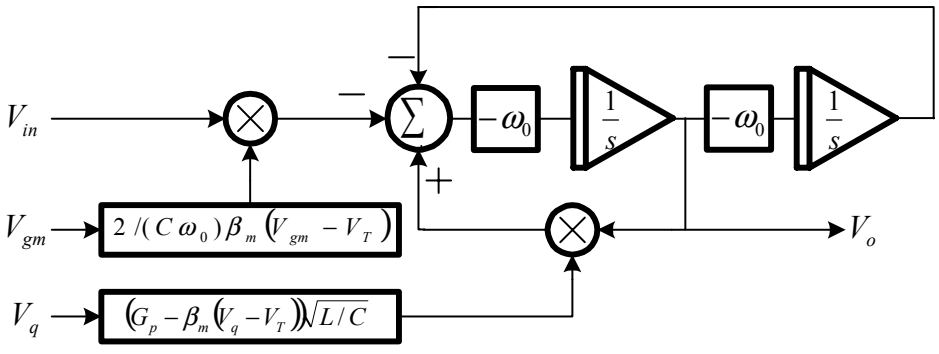
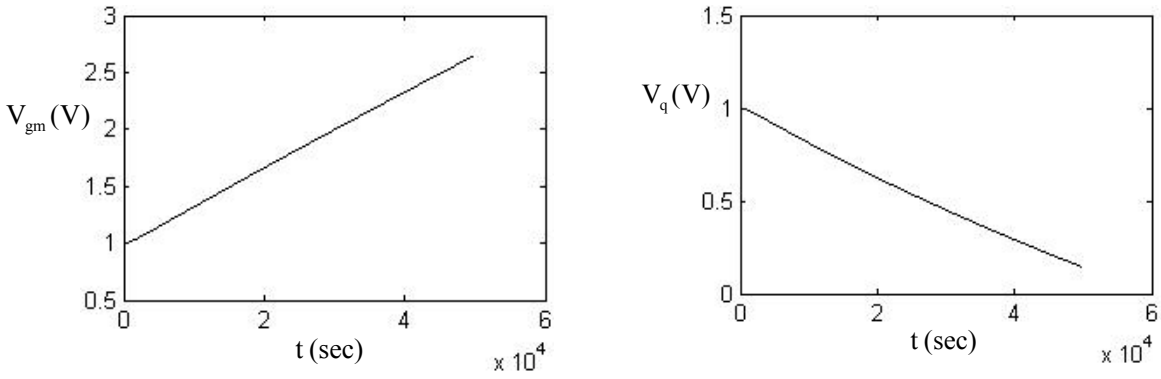


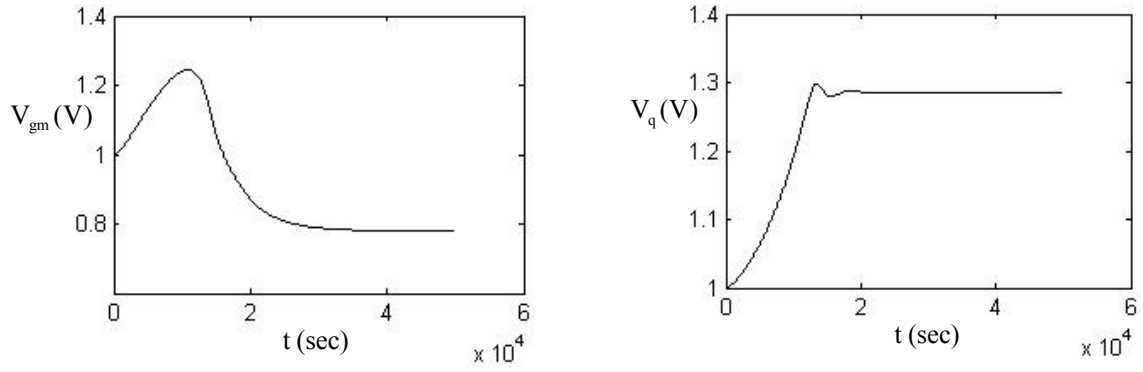
Fig. 5.5 Conceptual block diagram of the filter used in SIMULINK simulations.



(a) (b)

Fig. 5.6 SIMULINK simulation of the tuning scheme of Fig. 5.3 (a) Evolution of the V_{gm} voltage versus time, and (b) evolution of the V_q voltage versus time.

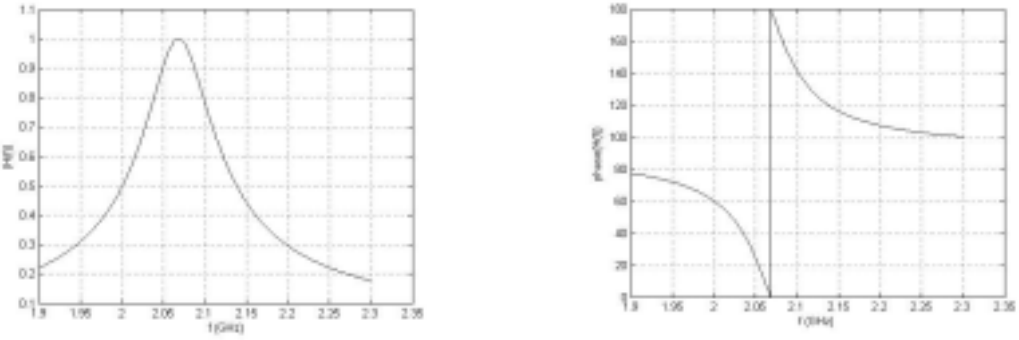
Fig. 5.6 shows the results of a simulation of the tuning scheme proposed in Fig. 5.1. The simulation is done for the following target values, ω_0=13×10^{9}rad/s, A_d=1 and Q=26. The filter parameters are the same used in the previous computations. The initial conditions of the loops were set to V_{gm}=1 and V_q=1. For that system, the equilibrium point is V_{gm0}=0.78V and V_{q0}=1.286V. In the simulation, we can observe how the system diverges from the equilibrium point as can be foreseen from the system phase portrait.



(a) (b)

Fig. 5.7 SIMULINK simulation of the tuning scheme of Fig. 5.4 (a) Evolution of the V_{gm} voltage versus time, and (b) evolution of the V_q voltage versus time.

Fig. 5.7 shows the results of a simulation of the tuning scheme proposed in Fig. 5.2. The target values, filter parameters and initial conditions are the same ones used in the previous simulation of Fig. 5.6. However, we can observe, that in this case the system control voltages V_{gm} and V_q evolve towards their stable equilibrium point. Fig. 5.8 shows the magnitude and phase plots of the resulting tuned filter. It has the desired Q and the desired gain at resonance.



(a) (b)

Fig. 5.8 (a) Magnitude and (b) phase plots of the tuned filter in Fig. 5.2 for Q=26 and A_d=1 at f_0=2.07GHz

4.3. Non-ideal Effects

4.2.1 *Remarks on the effect of parasitic capacitances*

The main source of parasitics in the circuit implementation of the LC filter is shown in Fig. 5.9. The overall transfer function of the filter can be expressed as

$$H(s)=\frac{V_{out+}(s)-V_{out-}(s)}{V_{in+}(s)-V_{in-}(s)}=\frac{-\frac{G_m}{C_T}\left(1-\frac{C_{id}}{G_m}s\right)s}{s^2+\frac{G_P-G_{neg}}{C_T}s+\frac{1}{LC_T}} \tag{5-16}$$

where, C_T=C+4C_{od}+C_{os}; C_{id} is the gate-drain capacitance of M_4-M_5 and C_{od} and C_{os} are the gate-drain and gate-source capacitances of M_2-M_3, respectively.

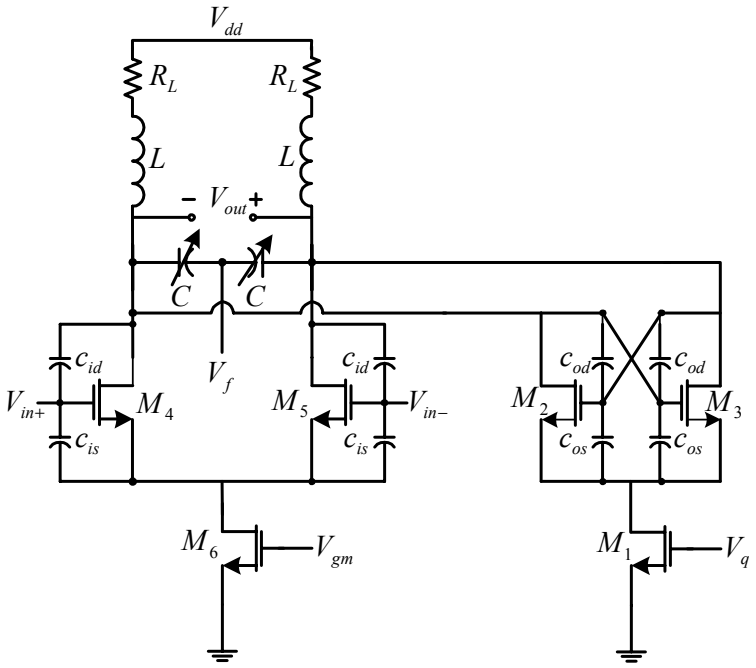


Fig. 5.9 Parasitic capacitances of the filter.

Comparing (3-3) and (5-16) reveals that by considering the parasitic capacitances, center frequency will decrease to $1/\sqrt{LC_T}$, which can be corrected in a frequency tuning loop, while Q will increase to $\sqrt{C_T/L}/(G_p - G_{neg})$. Note that at the center frequency, the phase of the amplitude transfer function of the filter will change from 0° to $\tan^{-1}\left(\frac{C_{id}}{C_T}\frac{1}{\sqrt{LC_T}}\right)$ and the amplitude response of the filter will increase by a factor of $\sqrt{1+\left(\frac{C_{id}}{C_T}\right)^2\frac{1}{LC_T}}$. However, since the proposed Q-tuning scheme in Fig. 5.2 is not relying on the phase and absolute value of the peak amplitude gain of the filter, the above variations in these parameters will not affect the performance of the presented scheme. In summary, our proposed tuning scheme can absorb these parasitic effects.

5.3.2 *Remarks on the Effect of the DC Offsets*

Assume the DC offset of the combination of the multipliers together with the LPFs and the summers in Fig. 5.2 can be modeled as additive terms of γ and θ, respectively. Recall that the gain of the real part of the filter at ω_L is A_0/δ_q, with δ_q ideally equal to 2. Following the steps shown in Fig. 5.10, the final error of loop1 can be found as

$$error_a = \frac{V_0^2}{2} - \frac{A_0}{A_d}\frac{V_0^2}{2} + \left(\gamma_1 - \frac{\gamma_2}{A_d} + \theta_a\right). \tag{5-17}$$

Thus, in steady state the relative error of the peak amplitude gain can be expressed as

$$\frac{\Delta A_0}{A_0} = \frac{A_d - A_0}{A_d} = -\frac{2}{V_0^2}\left(\gamma_1 - \frac{\gamma_2}{A_d} + \theta_a\right). \tag{5-18}$$

Similarly, the final error of the loop2 and the corresponding relative Q-tuning error can be expressed as

$$error_q = \frac{V_0^2}{2}(1 - \frac{A_0}{A_d}) - \frac{V_L^2}{2}(1 - \frac{A_0}{A_d\delta_q}) - \gamma_3 + \gamma_1 - \frac{\gamma_2}{A_d} + \frac{2\gamma_4}{A_d} + \theta_q \tag{5-19}$$

$$\frac{\Delta\delta_q}{\delta_q} = \frac{-\gamma_3 + \gamma_1 - \frac{\gamma_2}{A_d} + \frac{2\gamma_4}{A_d} + \theta_q}{\frac{V_L^2}{2} + \gamma_3 - \frac{2\gamma_4}{A_d} + \theta_a - \theta_q} \tag{5-20}$$

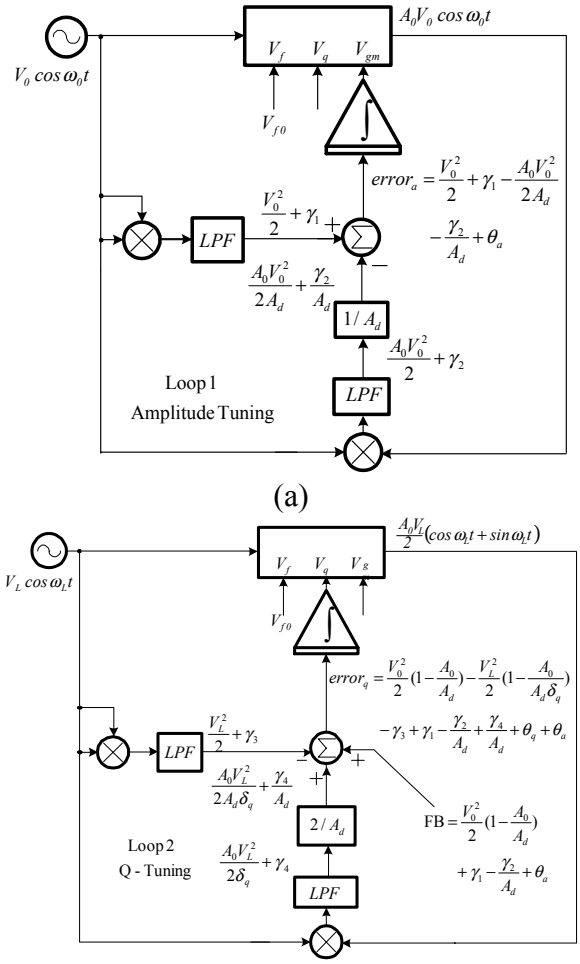
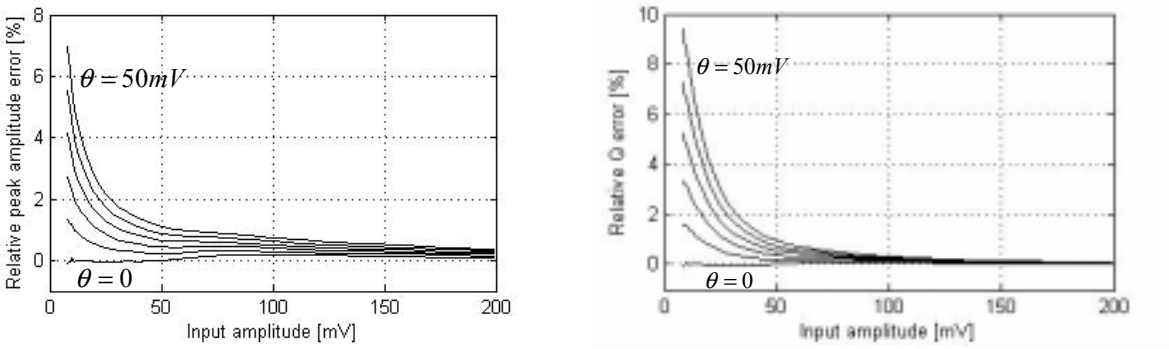


Fig. 5.10 Effects of the DC offsets on the *Q*-tuning scheme of Fig. 5.2 (a) Loop1 (b) Loop2

The numeric value of γ has been accurately extracted as a function of the input amplitude from the difference between the simulation and the measurement results (see Fig. 5.15). Assuming A_d=1, the relative errors in (5-18) and (5-20) for θ=0 to θ=50mV in steps of 10mV have been plotted in Fig. 5.11.



(a) (b)

Fig. 5.11 Estimated errors vs. θ (a) relative peak amplitude error (b) relative Q error

Based on these results the relative errors of the amplitude and the Q-tuning loops for V_{in}=50mV and θ=50mV are around 1.2% and 2.5%, respectively. As Fig. 5.11 shows, besides minimizing the DC offsets of different blocks, by increasing the input amplitude the relative errors in the amplitude and the Q-tuning loops can be decreased. For example by increasing the input amplitude by 10%, for θ=50mV and V_{in}=10mV, the above errors decrease by 0.1% and 0.12%, respectively. Furthermore, under the influence of process variations due to the mobility (10%), threshold voltage (10%) and width (5%) deviations of MOS transistors as well as 15% degradation in the sheet resistance of the top metal layer, the simulation results show that the quality factor of the filter is changed by 8% which can be tuned back using the proposed scheme.

5.4. Test Chip Measurement Results

A prototype has been designed in a TSMC 0.35μm, 2-poly, four metal standard CMOS technology. The microphotograph is shown in Fig. 5.12 which occupies a silicon area of 0.0725mm^2 and contains a filter with two multipliers.

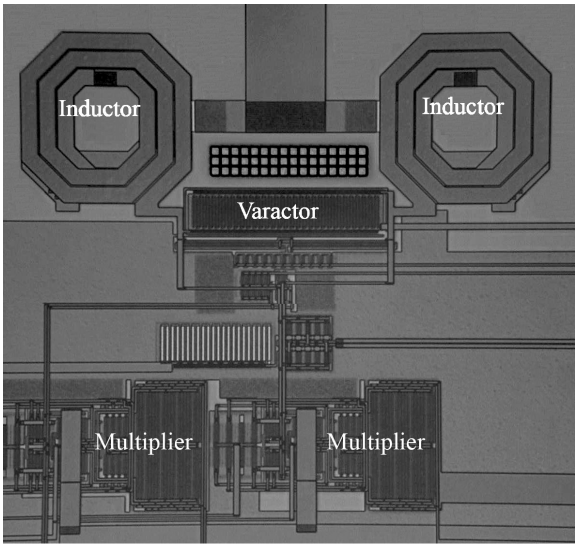


Fig. 5.12 Chip microphotograph.

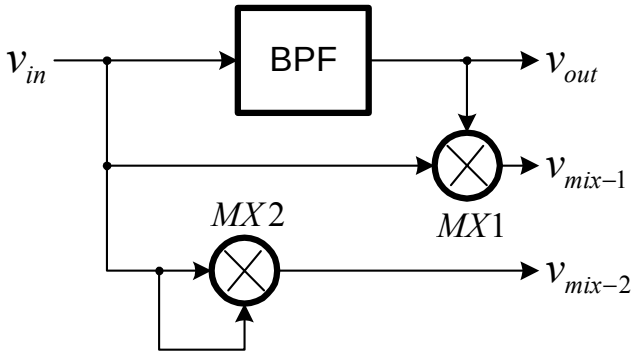


Fig. 5.13 Block Diagram of the fabricated chip.

A simple open drain output buffer is employed at the output of the filter to drive the 50Ω load of the instrument which shows a stand-alone attenuation of around -10dB at 1.8GHz. Fig. 5.13 shows the block diagram of the fabricated prototype chip. Note that we are using only one loop (filter). Note that the input sinusoids at ω_0 and ω_L can be generated by a fractional-N synthesizer with an LC oscillator. However, we have used external inputs in the following experimental results.

Fig. 5.14 shows the transistor level implementation of the multiplier [75].

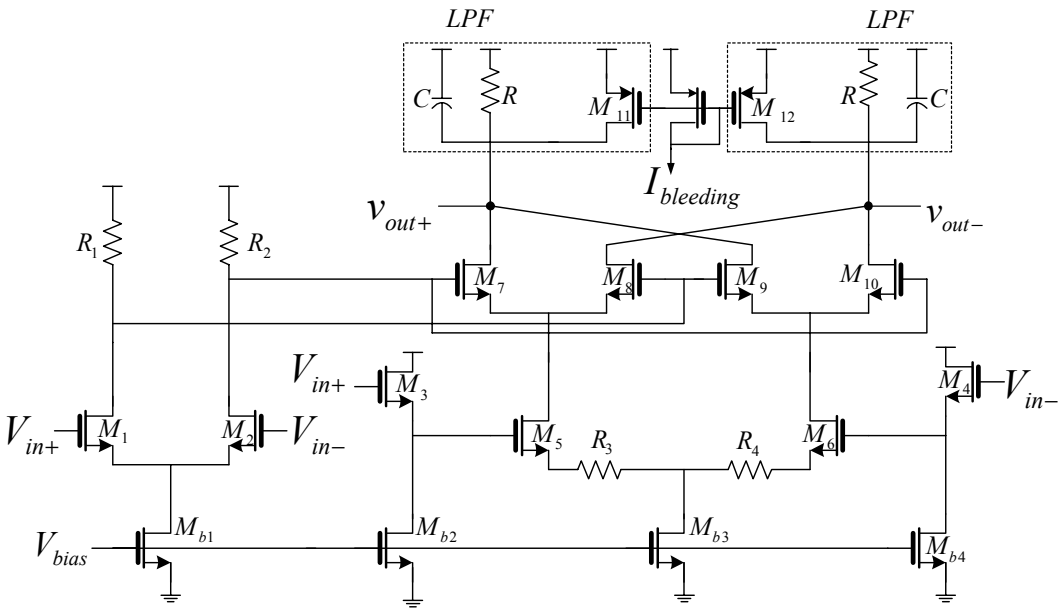


Fig. 5.14 Schematic of the multiplier [75] with the RC LPF as its load.

The injected current, called bleeding current, allows separate control of current flowing through the drive stage (M_1 and M_2) from the current switches (M3-M6). For the same drive bias current, bleeding reduces the current flowing through the current switches and load resistance. Thus, the flicker noise contributed by the switches is significantly reduced and allows us to use large load resistors which increase the conversion gain. Since the load of the multiplier is resistive, the need of a common mode feedback circuit at the multiplier output is avoided.

It is of great importance to have exact knowledge of the DC performance of the multiplier for different input amplitudes. This has been carried out by the precise extraction of the DC output of the multiplier using the HP4156C while the test chip is shielded by the test fixture Agilent 16442A. The above setup is set to operate in the long time (1sec) mode during which the measured output is averaged over 1000 samples.

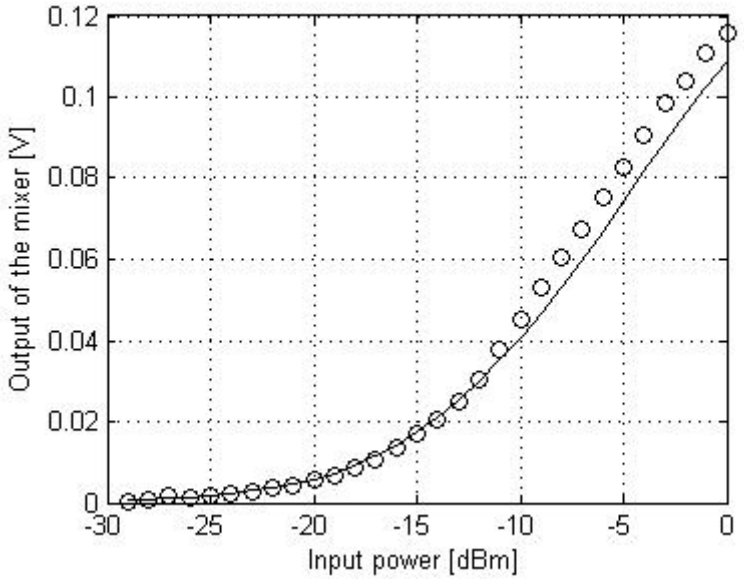


Fig. 5.15 DC level at the output of the multiplier MX2 in Fig. 5.13 as a function of the input amplitude at 2 GHz (circles: measured, solid line: simulated).

Fig. 5.15 compares the measured and simulated DC output voltages of the multiplier with both inputs connected together. Note that the deviation of the measured data from the simulation data for amplitudes greater than -3dBm is mainly due to the large signal operation of the multiplier which no longer provides the exact multiplication of the input amplitudes.

In this experimental prototype we chose to implement the low frequency portion of the control loops off-chip. That gives us more flexibility in the loops configuration during the testing process of the proposed procedures. However, as can be observed from Fig. 5.1 and Fig. 5.2, all the off-chip operations are just simple mathematical expressions of the signals at low frequency and thus, are appropriate for full integration of the entire tuning loop. Furthermore, the center frequency of the filter has been tuned manually throughout the following measurement results.

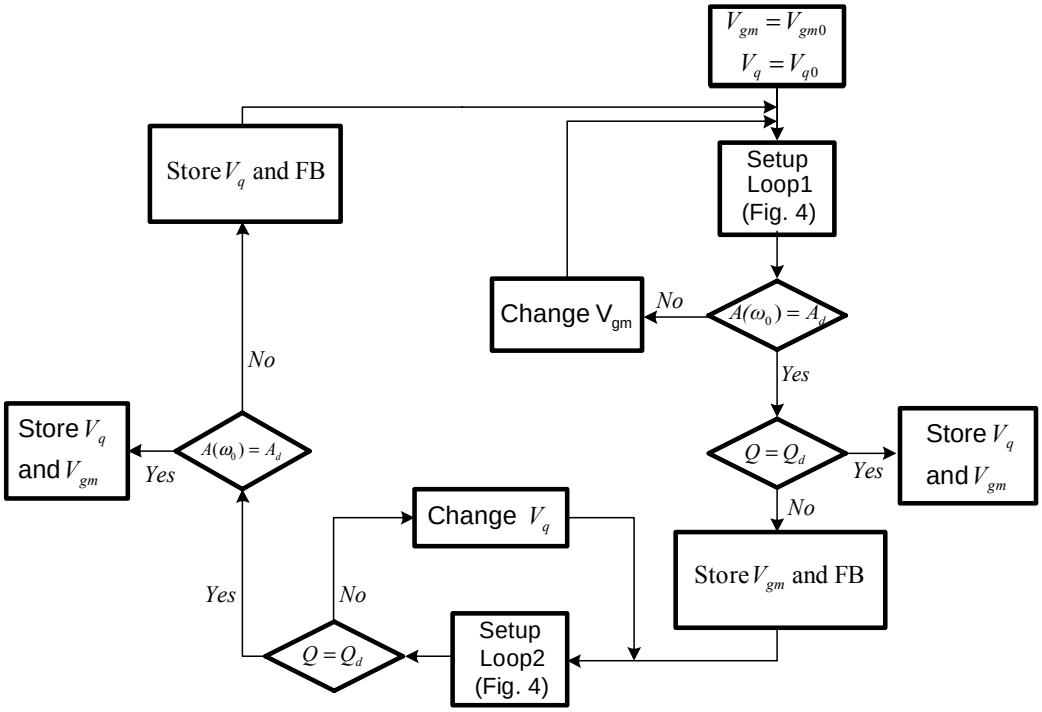


Fig. 5.16 Tuning algorithm using one filter.

The Q-tuning procedure can be summarized as follows. Assume that for an arbitrary constant voltage V_{gm0}, the center frequency ω_0 is already set. By applying an input signal at ω_0 to the loop1 in Fig. 5.2, the controlling voltage V_{gm} will settle to a final voltage V_{gmf} for which $error_a$ becomes zero i.e., $A_0=A_d$. Then for $V_{gm}= V_{gmf}$, by applying the feedback signals FB, the Q-tuning loop in Fig. 5.2 (Loop2) will settle to a final control voltage of $V_q=V_{qf}$ for which $error_q$ becomes zero i.e., $A_L=A_d/2$. In the case that we don't have two separate filters to tune the Q and the amplitude simultaneously the above procedure has to be repeated several times to get the desired amplitude and Q. Fig. 5.16 shows the flow chart of the tuning procedure using only one filter.

Fig. 5.17 shows the measured frequency response of the filter using a network analyzer for five different values of A_d and Q tuned from 60 to 220 at the center

frequency of 1.97GHz. The current consumption of the filter for Q of 60 and 220 are 3.6mA and 4.3mA, respectively.

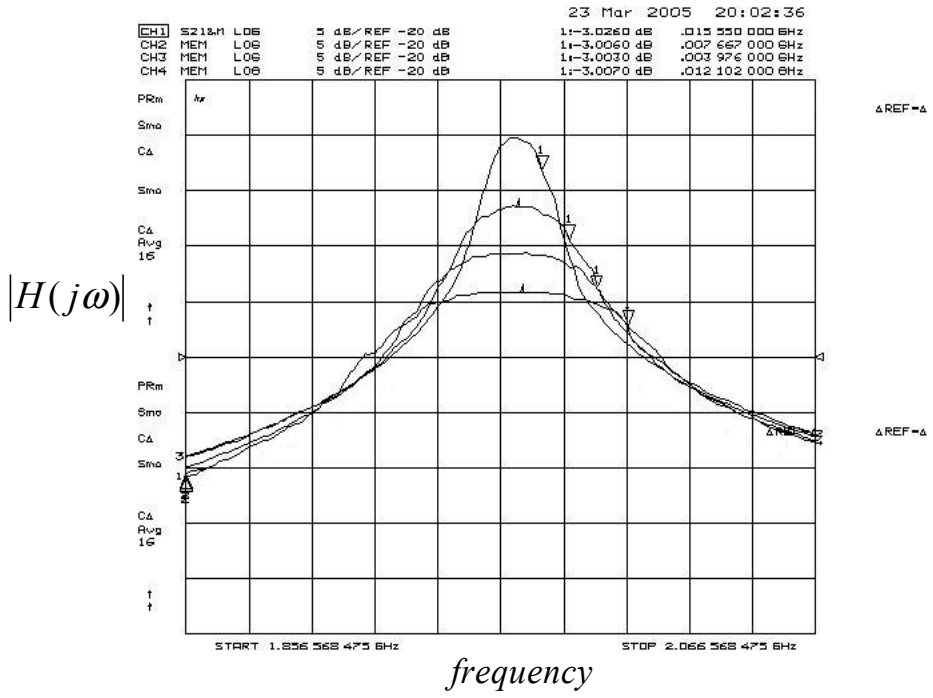


Fig. 5.17 Amplitude A_0(dB)={-15, -10, -5, 0} and Q-tuning Q={60, 80, 120, 220}measurement results.

Table 5-1 Summary of experimental results of tuning Q for different amplitudes

Targeted values		Achieved values		Number of Iterations	Tuning error (%)
Q_d	A_d (dB)	Q	A_0(dB)		Q-Tuning
60	-15	63	-14	5	4.7
80	-10	84	-11	7	4.7
120	-5	127	-7	9	5.5
220	0	246	-0.2	11	10.5

As shown in Table 5-1, which summarizes the performance of the tuning scheme, susceptibility of the filter to oscillate at very high values of Q results in higher tuning error with more iterations of the off-chip control loop.

The measured frequency response of the filter for fixed amplitude of A_d=0dB and Q tuned from 60 to 120 is shown in the Fig. 5.18. In this case, since only Q is a variable in the tuning scheme, better performance has been achieved in terms of tuning error and number of iterations. The performance of the tuning loop for this case is summarized in Table 5-2.

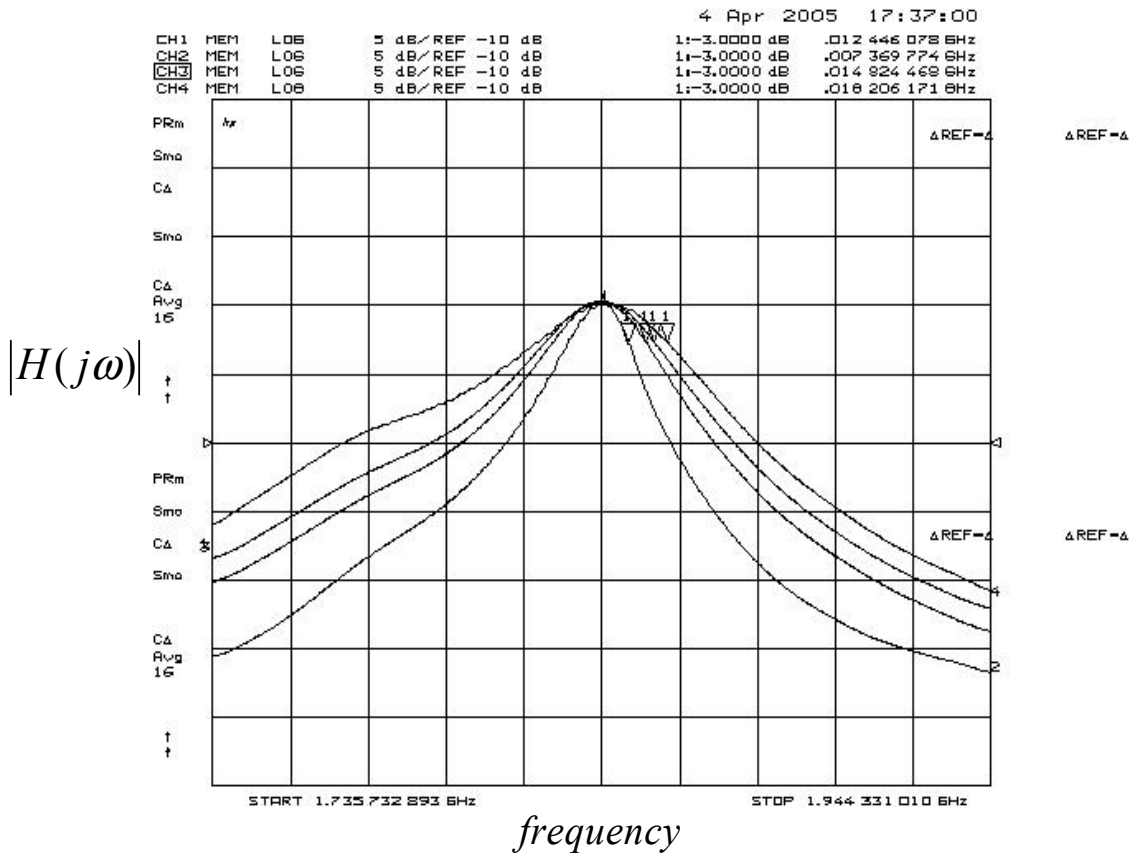


Fig. 5.18 Q-tuning measurement results for Q={50, 60, 70, 120} and fixed amplitude of A_0=0dB at ω_0=1.84GHz.

Table 5-2 Summary of experimental results of tuning Q for fixed amplitude at ω_0=1.84GHz.

Targeted values		Achieved values		Number of Iterations	Tuning error (%)
Q_d	A_d (dB)	Q	A_0(dB)		Q-Tuning
50	0	51	0	5	1.9
60	0	62	-0.1	7	3.2
70	0	74	-0.1	7	5.4
120	0	125	-0.2	9	6.9

CHAPTER VI

A HIGHLY LINEAR PSEUDO-DIFFERENTIAL 3rd-ORDER LOW PASS FILTER

6.1. Introduction

The development of a host of portable wireless communication systems increases a demand for high performance and highly integrated circuits. High frequency low distortion continuous time filters are among the key building blocks for most of the high performance systems like ADCs and asymmetrical digital subscriber loops (ADSLs) [76]. Due to the rapid increase in the power consumption of the classical Active-RC filters to maintain their quality performance at higher frequencies, fully balanced G_m-C filters have received considerable attention [76]-[81]. However, due to the lack of large feedback gain on the integrators in the implementation of Gm-C filters, higher frequency of operation and larger signal linearity are imposed on them.

In analog/mixed signal processing, fully differential structures are preferred in comparison with their single-ended counterparts because they result in a larger dynamic range and a better rejection to power-supply noise and clock feedthrough. The main disadvantages of the fully differential approach are the increased power and area requirement due to the common mode feedback (CMFB) circuit and the limitation of filter speed due to the loading of the CMFB circuit on the differential path. Furthermore, the CMFB circuit is intrinsically slower than the differential one and thus, in the presence of mismatches which lead to an interaction between the common mode and differential

paths, plays a greater role than the differential one in determining the maximum operating frequency of fully differential Active-RC filters.

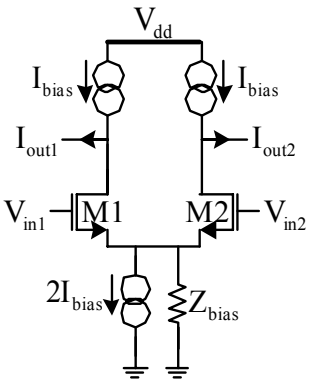
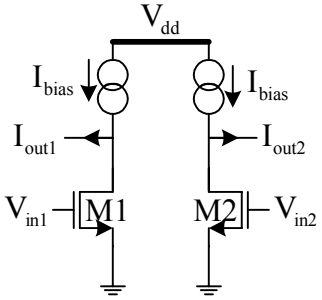
For applications of even lower power supply voltage and larger signal swing, pseudo-differential (PD) structures, [82]-[84], become more advantageous since they avoid the voltage drop across the biasing current source which due to considerations in matching, noise and output impedance should be at least few hundreds of mV. However, since in the PD structure the two input branches operate independently and the whole structure can be seen as differential only if the input signal is balanced, i.e. $V_{in}\pm=V_{cm}\pm v_{ac}/2$, a careful and efficient control over the common-mode behavior of the circuit is required. In fact a common-mode signal at the OTA inputs follows the same path as the differential signal, which is the only one containing the information and the only one of interest for analog processing. If the OTA output is taken differentially, any common-mode signal is ignored, thus leaving virtually the same differential information as in a truly differential implementation. This, however, is true only if the common mode at the OTA outputs is low enough not to push the OTA out of its linear operating regime. This means that the common-mode signal allowed at the input of the OTA must be low. In the presence of mismatches a differential-mode signal can arise due to the common-mode signal multiplied by the mismatch factor. Thus a low input common mode voltage helps in this way too. Another cause of increased common-mode signal at the OTA outputs is the unwanted signals such as the power supply noise, which can be capacitively coupled to both the OTA inputs. A well-designed bias circuit and a careful layout to avoid as many couplings as possible have to be used. Another important issue is that, in pseudo-differential transconductors, the current consumption, the linearity and, at

least as second order effect, the transconductance are functions of the CM input voltage. A CM signal therefore can originate a large amount of distortion also in the process of differential signals.

Considering the effect of mobility degradation in short channel transistors, Table 6-1 summarizes some of the important features of FD and PD transconductors for $V_{in1,2}=V_{CM}\pm V_{in}/2$. In this table V_{DSAT} represents the saturation voltage of the input transistors and A_{in} is the magnitude of the differential input signal. As stated above, removing the tail current source, in a PD structure, reduces the minimum supply voltage V_{ddmin} and increases the output voltage swing which yields a higher dynamic range (DR) with respect to the FD structure. Removing the tail current source, however, results in larger common-mode gain (A_{CM}). In a FD structure, the common-mode gain can be reduced by increasing the output resistance of the tail current source. However, for the PD structure, the common and differential mode gains, A_{CM} and A_{DM}, are equal, resulting in CMRR=A_{DM}/A_{CM}=1. This large A_{CM}, in PD structures, can lead to huge common-mode variations at the OTA outputs unless a fast and strong CMFB is used. Furthermore, in a PD structure, a second order term always appears at the output current which its amplitude depends on the V_{CM} and the second-order transconductance (g_2) of the input transistors.

In this chapter, a linearized PD CMOS OTA is presented. The behavior of a PD voltage buffer is studied and the effect of the second order harmonic on the overall linearity is explored. Analytical results show that the third order harmonic distortion (HD3) of the output voltage of a PD buffer is related to the amplitude of the second order harmonic.

Table 6-1 Summary of fully differential and pseudo-differential OTA's performance

		
$G_{m\text{-}DM}$	$g_{m1}=g_{m2}=g_m$	$g_{m1}=g_{m2}=g_m$
$G_{m\text{-}CM}$	$\frac{g_{m1}}{1+g_{m1}Z_{bias}}$	$g_{m1}=g_{m2}=g_m$
i_{out}	$g_m v_{in}-(g^2_2/g_m-g_3/4)v^3_{in}$	$g_m v_{in}+2g_2 v_{in}V_{CM}+g_3(3v_{in}V^2_{CM}+v^3_{in}/4)$
HD3	$\frac{1}{32}\left(\frac{A_{in}}{V_{CM}-V_{thn}}\right)^2$	$\frac{\theta A^2_{in}}{3(V_{CM}-V_{thn})(2-3\theta(V_{CM}-V_{thn}))-4\theta A^2_{in}}$
DR	$\approx 0.3V_{DSAT}/v_{noise\text{-}in}$	
V_{ddmin}	$V_{thn}+2V_{ds1}+V_{dsp}$	$V_{thn}+2V_{dsatn}+V_{dsatp}$
Output swing	$V_{CM}+V_{TH}<V_{out}<V_{dd}-V_{dsp}$	$V_{ds1}<V_{out}<V_{dd}-V_{dsp}$
A_{DM}	$g_m(r_{on}\|\|r_{op})$	$g_m(r_{on}\|\|r_{op})$
A_{CM}	$g_m(r_{on}\|\|r_{op})/Z_{bias}$	$g_m(r_{on}\|\|r_{op})$
CMRR	$Z_{bias}>>1$	$=1$

6.2. OTA Architecture

Considerable work has been reported in the literature on improving the linearity of continuous time Gm-C filters [83], [85]-[87]. The challenge in this area has been on processing large signals at high frequencies and reducing the harmonic distortion of such

circuits. However, little has been done on the effect of the system on the linearity performance of the OTA's as their main building blocks.

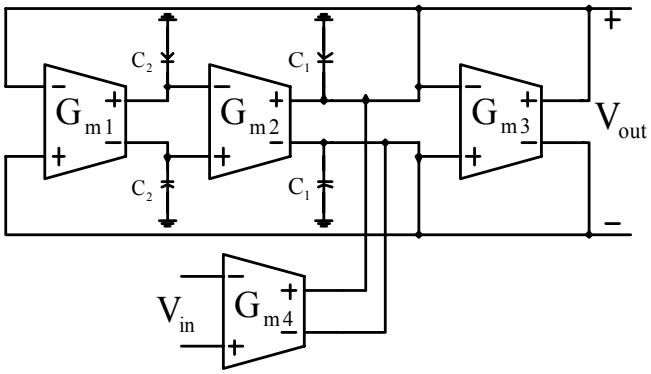


Fig. 6.1 Second-order Gm-C bandpass filter.

Consider the Gm-C implementation of a second-order bandpass filter illustrated in Fig. 6.1. This topology is often preferred with respect to other versions since an additional lowpass output is available [88]. Furthermore, it has the advantage that allows controlling the common-mode voltage at both integrator outputs. In addition a minimum sensitivity of the quality factor with respect to capacitance mismatch is achieved by choosing C1=C2 [88]. Assuming C1=C2=C and neglecting finite output impedances of the OTA's the transfer function of this filter can be expressed as

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{(\frac{G_{m4}}{C})s}{s^2+(\frac{G_{m3}}{C})s+\frac{G_{m1}G_{m2}}{C^2}} \tag{6-1}$$

where, the center frequency and quality factor of the filter can be expressed as $\omega_0=\sqrt{G_{m1}G_{m2}}/C$ and $Q=\sqrt{G_{m1}G_{m2}}/G_{m3}$, respectively.

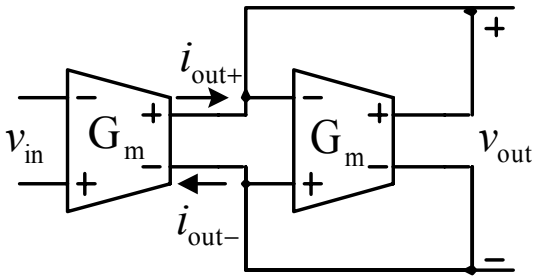
Note that the gain of the filter at the center frequency ω_0 is $|H(j\omega_0)| = G_{m4} / G_{m3}$ which for $G_{m3}=G_{m4}$ becomes one. This is considered as the worse scenario for the linearity of the output signal in presence of a relatively large input signal.

In pseudo-differential implementation the control of the common-mode output voltage can be done taking advantage of the presence of lossy-integrators which are generally used to introduce dumping. In fact a pseudo-differential transconductor closed in a negative feedback, creates a low impedance to ground for both the differential and common-mode signals. This automatically controls the common-mode output voltage. This is not the case for fully differential signal and thus a common-mode feedback must be implemented separately. Thus, in Fig. 6.1 the common mode output voltage is controlled by Gm3 which creates low impedance to ground, meaning that Gm2 and Gm4 don't need to have CMFB circuits. Thus, due to the high output impedance, the only block which its output voltage needs to be controlled is the G_{m1}.

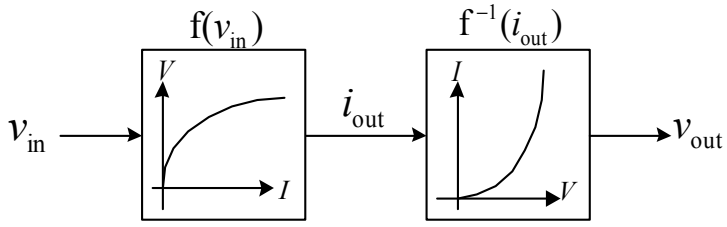
As far as the linearity is concerned, G_{m1} has a little effect on the overall linearity of the output voltage in Fig. 6.1. This is due to the fact that the output impedance seen by G_{m1} is large and since the voltage swing at this point is limited thus, G_{m1} should be small. Assuming that $G_{m1}=G_{m2}$, the effect of G_{m2} on the linearity of the output voltage is negligible too. Therefore, it can be concluded that the bottle neck for large signal linearity is the output node at which, for $G_{m3}=G_{m4}$, the signal swing is as large as the input swing.

The above fact can be generalized to the voltage buffer, shown in Fig. 6.2(a), which is a series combination of two identical G_m blocks in a unity gain negative feedback loop. The first G_m in Fig. 6.2(a) converts the input voltage (V_{in}) to current (I_{out}) with some degree of nonlinearity. This nonlinear current flows across a diode connected

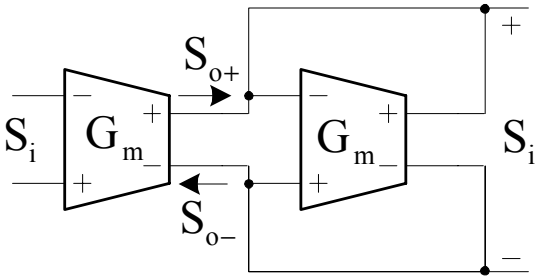
G_m, which behaves as a nonlinear resistor, deteriorating more the linearity of the output voltage. As illustrated in Fig. 6.2(b), only if the V-I transfer function of the diode connected G_m was exactly the inverse of the I-V transfer function of the input G_m, the output signal would be very linear. However, due to the large swing of signal across the drain-source of both Gm cells, the two transfer functions are not quite the same.



(a)



(b)



(c)

Fig. 6.2 (a) voltage mode buffer (b) conceptual implementation of Fig. 6.2(a) (c) general representation of Fig. 6.2(a)

The linearity behavior of the system shown in Fig. 6.2(a) can be analyzed using the control theory. Consider the general representation of Fig. 6.2(a) as depicted in Fig. 6.2(c). The input and output signals in this figure can be expressed as

$$S_o = a_1 S_i + a_2 S_i^2 + a_3 S_i^3 + \Lambda$$
$$S_i = b_1 S_o + b_2 S_o^2 + b_3 S_o^3 + \Lambda$$

By substituting S_i in S_o in the above equations, and equating both sides the following relation between the coefficients of S_i and S_o can be obtained

$$b_1 = \frac{1}{a_1}; \quad b_2 = -\frac{a_2}{a_1^3}; \quad b_3 = \frac{a_3}{a_1^4} - \frac{2a_2^2}{a_1^5}$$

Observe from the expression of b_3 the second harmonic term of S_o can be used to cancel the third order harmonic distortion of S_i, i.e. b_3=0.

The above idea can be applied to linearize some analog circuits which inherently contain even order information at their output. One example of such circuits is PD OTA's. To explore the linearity behavior of the output signal of Fig. 6.2(a), consider its PD implementation shown in Fig. 6.3. Transistors M_1 and M_2 are identical with the same W/L ratios and considering the θ effect, their I-V characteristics can be expressed as:

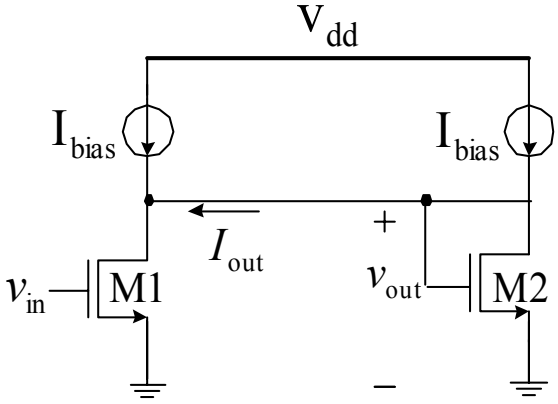


Fig. 6.3 PD implementation of Fig. 6.2(a).

$$i_D = \frac{1}{2}\frac{\mu_n C_{ox}}{1+\theta V_{ds}}(\frac{W}{L})(V_{GS}-V_{th})^2 . \tag{6-2}$$

Based on (6-2), the output current of M1 contains higher order harmonics. Assuming an input sinusoidal signal $V_{in} = A_{in}\cos(\omega t)$, the output current of M1 can be expressed as

$$i_{out} = I_{DC} + B_1\cos(\omega t) + B_2\cos(2\omega t) \tag{6-3}$$

where,

$$B_1 = -\beta_1 A_{in} V_{th}(2+3\theta V_{th}) = \beta_1 B_{1r} \tag{6-4}$$

$$B_2 = \frac{1}{2}\beta_1 A_{in}^2(1+3\theta V_{th}) \tag{6-5}$$

$$I_{DC} = \beta_1\left((1+\theta V_{th})V_{th}^2 + \frac{1}{2}A_{in}^2(1+3\theta V_{th})\right) \tag{6-6}$$

where, $\beta_1 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})$, $B_{1r} = A_{in}V_{th}(2+3\theta V_{th})$ and $B_{2r} = A_{in}^2(1+3\theta V_{th})/2$.

Using (6-2)-(6-6), the third-order harmonic distortion (HD_3) of the output voltage v_{out}=v_{GS2} can be found as:

$$HD3 \cong \frac{B_1^2}{24I_{DC}^2} - \frac{B_2}{4I_{DC}}. \tag{6-7}$$

To verify the accuracy of (6-7) a simulation has been carried out and for I_{DC}=90μA, A_{in}=1Vp-p, W/L=10 and θ=0.3 a HD_3 of -76.8dB is obtained. Hand calculation based on (6-7) predicts a HD3 of -79.3dB.

6.2.1. *Mismatch Effect*

Mismatch between transistors M1 and M1' in Fig. 6.4 will cause a variation in their output currents which results in a non-zero second order harmonic and a degraded third-order harmonic. To address this issue let us re-write (6-4) and (6-5) as

$$B_1 = \beta_1 B_{1r} \tag{6-8}$$

$$B_2 = \beta_1 B_{2r} \tag{6-9}$$

where, $B_{1r} = A_{in}V_{th}(2 + 3\theta V_{th})$ and $B_{2r} = A_{in}^2(1 + 3\theta V_{th})/2$.

Using (6-8) and (6-9) and following the same procedure used to derive (6-7), after a few laborious derivations, the following expressions for HD3 and HD2 of the output voltage in Fig. 6.4 can be drawn.

$$HD3' \cong \left(\frac{\beta_1^3 + \beta_1'^3}{\beta_1 + \beta_1'}\right)\frac{B_{1r}^2}{24I_{DC}^2} - \left(\frac{\beta_1^2 + \beta_1'^2}{\beta_1 + \beta_1'}\right)\frac{B_{2r}}{4I_{DC}} \tag{6-10}$$

$$HD2' \cong \left(\frac{\beta_1 - \beta_1'}{\beta_1 + \beta_1'}\right)\frac{B_{2r}}{B_{1r}} - (\beta_1 - \beta_1')\frac{B_{1r}}{8I_{DC}} + \left(\frac{\beta_1^3 - \beta_1'^3}{\beta_1 + \beta_1'}\right)\left(\frac{3B_{1r}B_{2r}}{16I_{DC}^2} + \frac{8B_{2r}^3}{3B_{1r}I_{DC}^2}\right) \tag{6-11}$$

where, β_1 and β_1' represent the β factors of M_1 and M'_1, respectively.

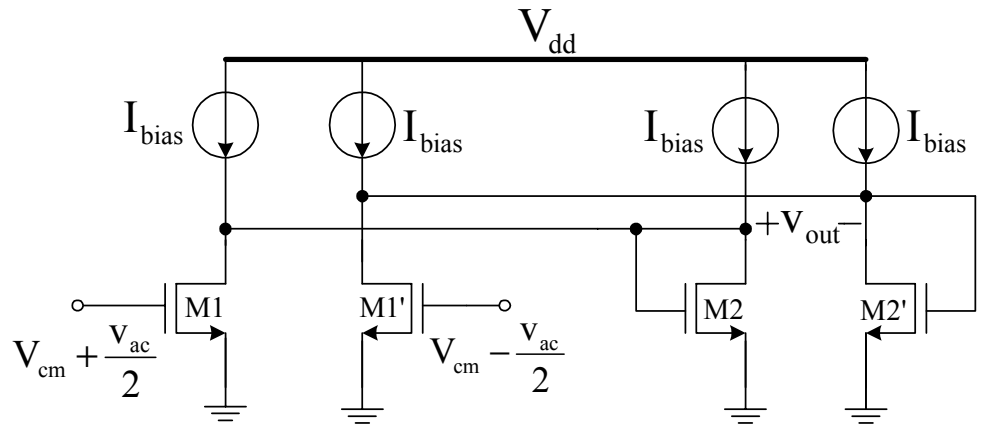


Fig. 6.4 Differential implementation of Fig. 6.3.

For a mismatch of $\beta_1/\beta'_1=\delta$, HD3' in (6-10) can be calculated as

$$HD3' \cong \frac{HD3}{1+\delta} + \frac{\delta^2}{1+\delta}\left(\frac{\delta B_{1r}^2}{24 I_{DC}^2} - \frac{B_{2r}}{4 I_{DC}}\right) \tag{11b}$$

Note that for $\delta=1$, i.e., $\beta_1=\beta'_1$, HD2'=0 and (6-10) reduces to (6-7).

6.2.2. *Proposed Linearized PD OTA*

A careful look at (6-7) reveals that by properly increasing the second order harmonic of the output current of M_1 the overall HD3 of the output voltage can be decreased. Thus, to linearize the structure of Fig. 6.2, the second order harmonic of the output current needs to be properly generated and injected back to the output node.

The chain nature of the G_m-C filter implementation allows each G_m cell to take advantage of its following G_m cell to extract some of its output signal properties. This is a well known technique that in fully differential implementation of G_m-C filters with source degenerated G_m cells, the DC operating point of the output voltage of each cell can be extracted by the following cell. In the next section we will show that using this

technique, besides extracting the DC operating point of the output voltage in the PD implementation, the second order harmonic of the output signal can be extracted as well.

Based on the above discussion, Fig. 6.5 shows the block diagram of the proposed OTA. The dashed block, called OTA2, is the diode connected Gm cell in a voltage buffer structure and it contains the DC operating point and the second-order harmonic extractions of the output signal to be used in the CMFB loop and the linearizing technique, respectively. OTA1 doesn't need to be as complicated as the OTA2 since its input voltage is assumed to be linear. However, in a structure like Fig. 6.1, OTA1 needs to contain the DC extraction circuitry to be used by the preceding OTA block. The details of the circuit implementation of different blocks in Fig. 6.5 are presented in the next section.

6.3. Circuit Implementation

Fig. 6.6 shows the core, G_m in Fig. 6.5, of the proposed OTA circuit. In comparison with the traditional PD structure [84], cross coupling of the output branches results in a differential property for each output current which not only improves the common mode rejection ration (CMRR) but also increases the effective g_m by a factor of 2 i.e., $I_{out1} - I_{out2} = 2g_{m1}(V_{in1} - V_{in2})$. This increase in the effective g_m, however, deteriorates the signal to noise ration (SNR) at the output node.

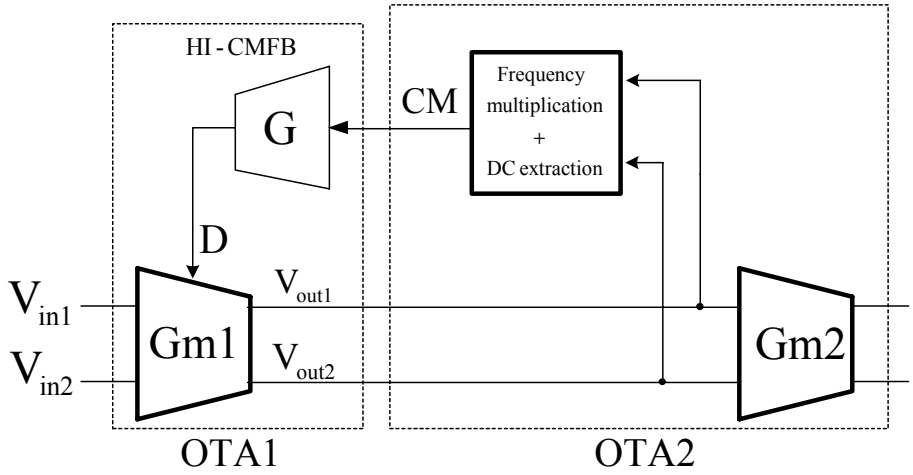


Fig. 6.5 Block diagram of the proposed OTA.

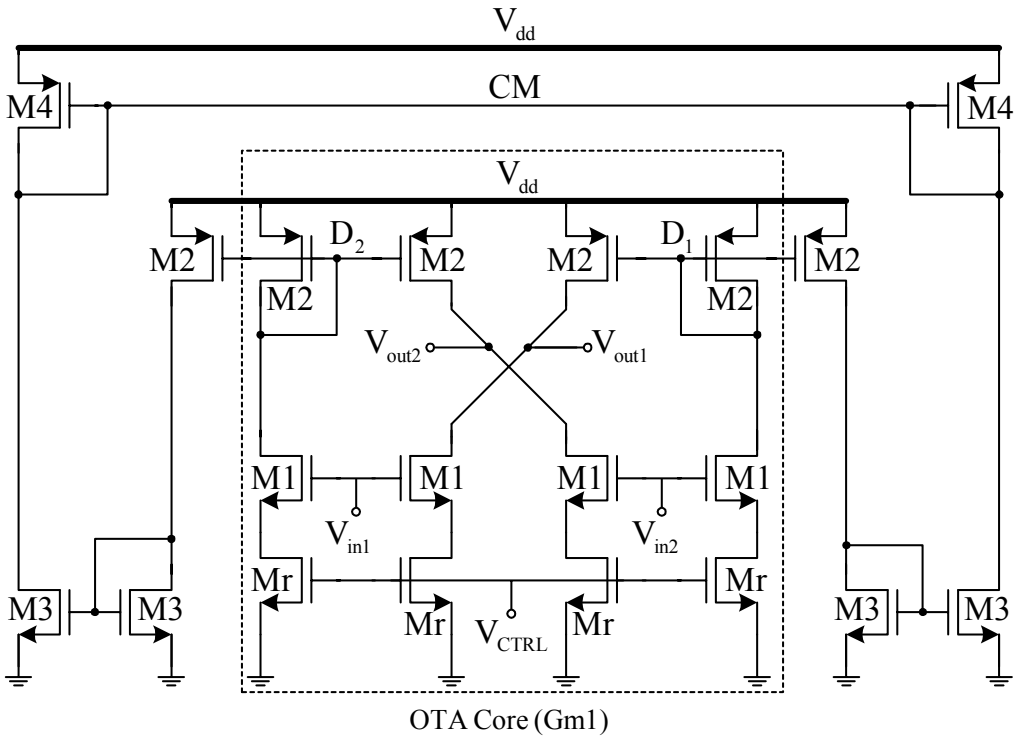


Fig. 6.6 Proposed OTA core.

The combination of M2-M4 extracts the DC information of the input voltage. A simplified version of this operation is shown in Fig. 6.7. To extract the DC information of

the input signal, the output currents of M1L and M1R, which are two identical g_m cells with complementary inputs, are summed up at the node CM. Using $I_{1L}=I_{DC}+\alpha_1 V_{in1}+\alpha_2 V^2_{in1}$, $I_{1R}=I_{DC}+\alpha_1 V_{in2}+\alpha_2 V^2_{in2}$ and $V_{in1}=-V_{in2}=v_{ac}/2$, the total current flowing into the node CM can be expressed as

$$I_{CM} = I_{1L} + I_{1R} = 2I_{DC} + \frac{\alpha_2 v_{ac}^2}{2}. \tag{6-12}$$

where, $I_{DC} = 0.5\mu C_{ox} W / L\left(V_{DCin} - V_{th}\right)^2$.

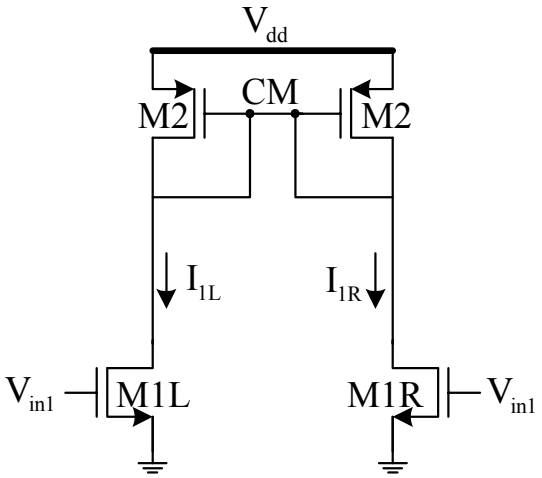


Fig. 6.7 DC and second-order harmonic extraction circuit.

In the above expressions, α_1 and α_2 are the transcnductances associated with the first and the second order harmonics, respectively. Thus, the voltage at node CM can be expressed as

$$V_{CM} = -\frac{4I_{DC}}{g_{m2}} - \frac{\alpha_2 v_{ac}^2}{g_{m2}}. \tag{6-13}$$

Substituting $v_{ac}=A_{in}\cos\omega t$ in (6-13) results in the following expression for V_{CM}

$$V_{CM} = V_{DC} - A_{CM}\cos(2\omega t) \tag{6-14}$$

where,

$$V_{DC} = \frac{-4I_{DC}}{g_{m2}} - \frac{\alpha_2 A_{in}^2}{2g_{m2}} \tag{6-15}$$

$$A_{CM} = \frac{\alpha_2 A_{in}^2}{2g_{m2}}. \tag{6-16}$$

Observe from (6-15), the first term contains the information of the input DC voltage and the second term contains the information of the second-order harmonic. In other word, the node CM in Fig. 6.7 contains the essential information needed to stabilize the DC output voltage in a CMFB loop as well as to linearize the small signal output current. Thus, the net information of the frequency multiplication, DC extraction and adder blocks in Fig. 6.5 can be easily obtained at the node CM in Fig. 6.7.

It is worth mentioning that to extract the DC information the input voltages could have directly connected to the gates of M3's in Fig. 6.6, removing the parasitic pole at the gate of M3. However, this scenario increases the parasitic capacitances seen by the input signals which ultimately reduce the frequency of operation.

6.3.1. *Harmonic Injection*

Fig. 6.8 shows the feedback circuit used to inject the second-order harmonic information back to the first G_m cell. Considering the negative sign of the small signal information in (6-15), node D in Fig. 6.8 is the only node in the G_m structure which can properly conduct the injected second-order harmonic to the output. Furthermore, the output impedance of the G_m cell is not affected by the injecting feedback circuit connected to the node D. To ensure that the DC component of the injected current will not affect the DC bias current of the main Gm, the reference current for Mfb has been

generated using the circuit shown in Fig. 6.8. In this circuit the capacitor C_f=1pF sufficiently attenuate the small signal components of the reference current.

In PD circuits the control of the common mode output voltage can be done by taking advantage of the presence of lossy integrators which are generally used to introduce dumping. In fact a PD transconductor closed in negative feedback, creates a low impedance to ground for both the differential and common mode output voltages.

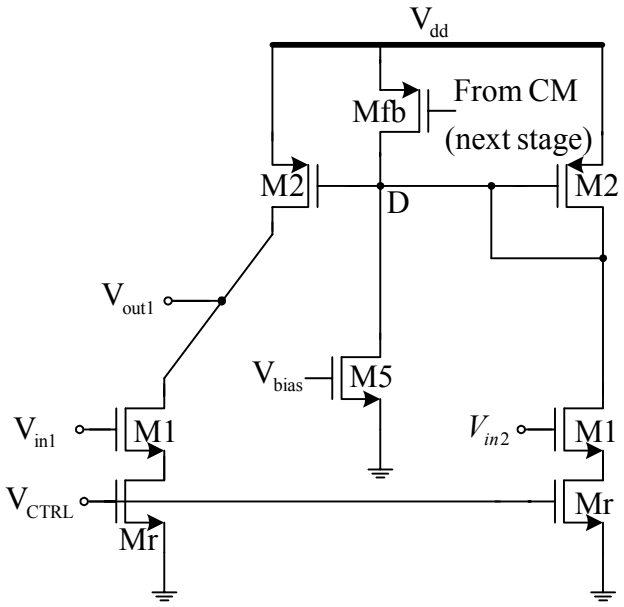


Fig. 6.8 Second-order harmonic injection circuit.

6.3.2. *CMFB Loop*

If the proposed Gm cell is not loaded with a similar diode connected Gm cell the harmonic injection block, M5-Mfb in Fig. 6.8, can be used to adjust the output DC operating point. Thus, for this scenario the combination of M5-M5fb along with the DC extraction circuit of the following Gm cell is called the CMFB loop. In this case, the

control voltage V_{bias} of M5 serves as the reference voltage for the CMFB loop while the DC information of the output nodes is available at the CM node of the following Gm cell. By changing V_{bias}, the DC current of M5 is changing. Then, this current is compared with the DC current of Mfb which has the information of the output DC voltage. The difference between I_5 and I_{Mfb} flows across the diode connected transistor M2 which mirrors this difference to the output node. The outcome of the above procedure changes the DC operating point of the output node. Transistors Mr in Fig. 6.6 and Fig. 6.8 are operating in triode region and are used to tune the G_m value of the OTA cell and their drain-source resistors can be changed by control voltage V_{CTRL}. The overall CMFB loop gain can be found as

$$A_{CMFB} = \frac{-g_{m1}}{(g_{m3}+sC_{CM})}\frac{g_{mfb}}{(g_{m2}+sC_D)}\frac{g_{m2}}{(g_{o1}+g_{o2}+sC_L)}. \tag{6-17}$$

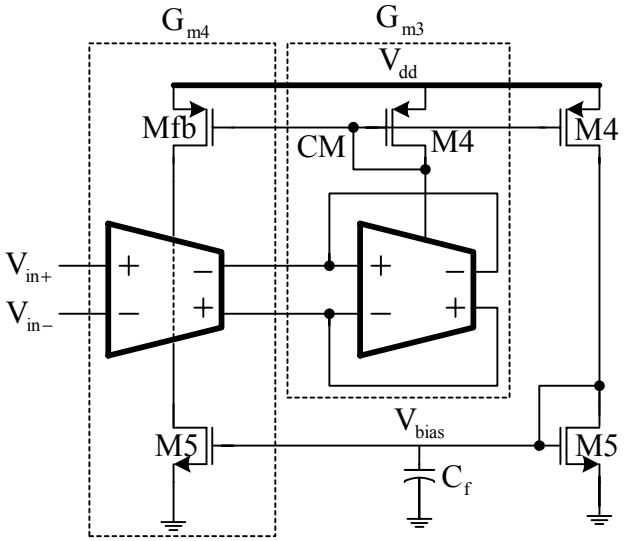


Fig. 6.9 Biasing the harmonic injection circuit.

Assuming $C_L>C_D>C_{CM}$, the dominant pole is located at the output node and the frequency behavior of the CMFB loop can be tuned by changing the load capacitance C_L. The common-mode gain A_{cm} and common-mode rejection ration (CMRR) of the proposed Gm cell at very low frequencies can be expressed as

$$A_{cm} = \frac{\dfrac{g_{m1}}{g_{on}+g_{op}+sC_L}}{1+\dfrac{g_{m2}}{(g_{on}+g_{op}+sC_L)}\dfrac{g_{m1}}{(g_{on}+g_{op}+g_{mfb}+sC_{CM})}\dfrac{g_{mfb}}{(2g_{on}+g_{op}+g_{m2}+sC_D)}} \tag{6-18}$$

$$A_{cm}(0) = \frac{g_{m1}}{g_{on}+g_{op}+g_{m1}} \cong 1 \tag{6-19}$$

$$CMRR(0) = \frac{A_{dm}(0)}{A_{cm}(0)} \cong \frac{2g_{m1}}{g_{on}+g_{op}} \quad . \tag{6-20}$$

Fig. 6. 9 shows the biasing circuit for the harmonic injection block. The complete schematic of the proposed OTA is shown in Fig. 6.10.

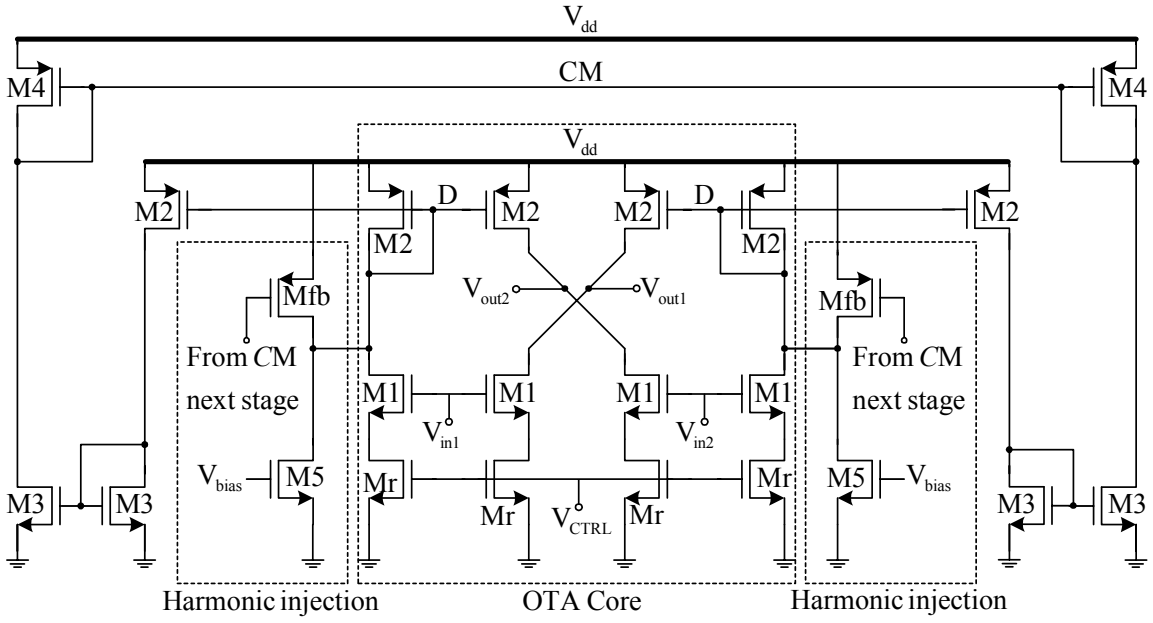


Fig. 6.10 Complete schematic of the proposed OTA.

A. Noise Analysis

Considering only the thermal noise, the corresponding input referred noise voltage of the proposed transconductance cell as well as the harmonic injection circuit (Fig. 6.9) can be expressed as:

$$\overline{V}_{n-rms}^{2} = \frac{16KT(BW)}{3g_{m1}}\left\{1+\frac{g_{m-2f}+g_{m3}+g_{m5}}{2g_{m1}^{2}}\right\} \tag{6-21}$$

where, BW is the equivalent noise bandwidth.

As (6-21) shows by increasing g_{m1} the input referred noise can be reduced at the price of increasing power. Using (6-4)-(6-7) and (6-21) the total signal to noise ratio at the input (SNR_{in}) can be expressed as:

$$SNR_{in} = \frac{V_{in-rms}^{2}}{\overline{V}_{n-rms}^{2}} = 10\log\left[\frac{3g_{m1}I_{DC}HD3}{4KTK_{n}(BW)}\frac{1+\frac{g_{m3}+g_{m5}+g_{m6}}{2g_{m1}^{2}}}{\frac{K_{n}(2+3\theta V_{th})^{2}V_{th}^{2}}{6I_{DC}}-\frac{1}{2}(1+3\theta V_{th})}\right] \tag{6-22}$$

As (6-22) shows, for a given HD3, increasing g_{m1} improves the SNR_{in} but at the same time, it increases the power consumption.

6.3.4. 3rd *Order Low Pass Filter*

As illustrated in Fig. 6.11, as an application of the proposed PD OTA, a 3rd order LPF based on ladder structure is implemented. It consists of 7 PD OTA and the cut off frequency is programmable around 10.7 MHz by changing the value of G_m's.

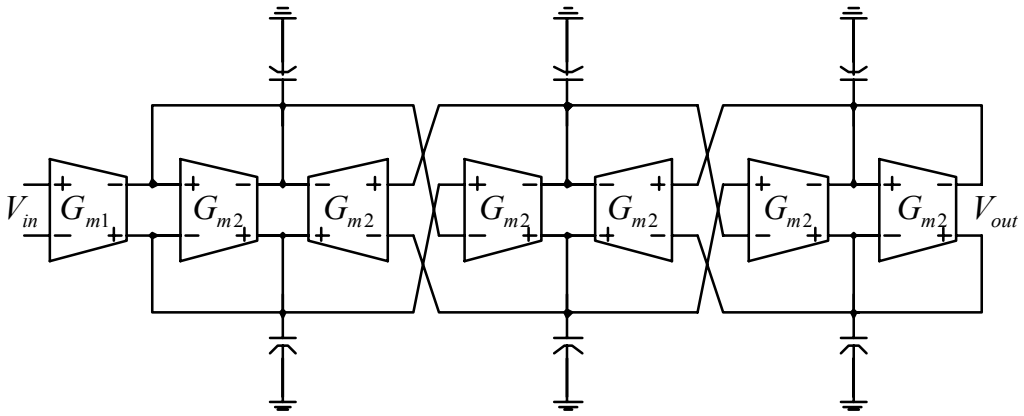


Fig. 6.11 Block diagram of the 8th order Butterworth LPF.

6.4. Measurement Results

A 3rd order low pass filter using the proposed OTA has been fabricated in AMI 0.5μm CMOS process available through MOSIS. Fig. 6.12 shows the micrograph of the chip which occupies an area of 0.019mm^2. Fig. 6.13 and Fig. 6.14 show the measurement setups for transfer function and intermodulation distortion of the PD LPF, respectively.

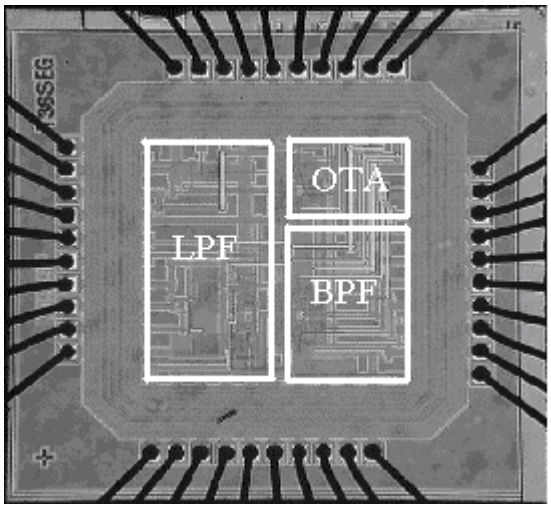


Fig. 6.12 Microphotograph of the fabricated chip.

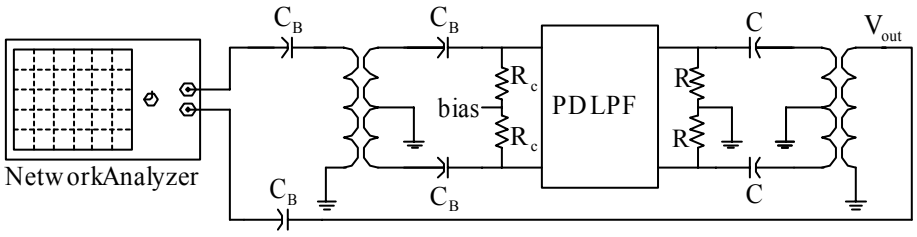


Fig. 6.13 Measurement setup for transfer function.

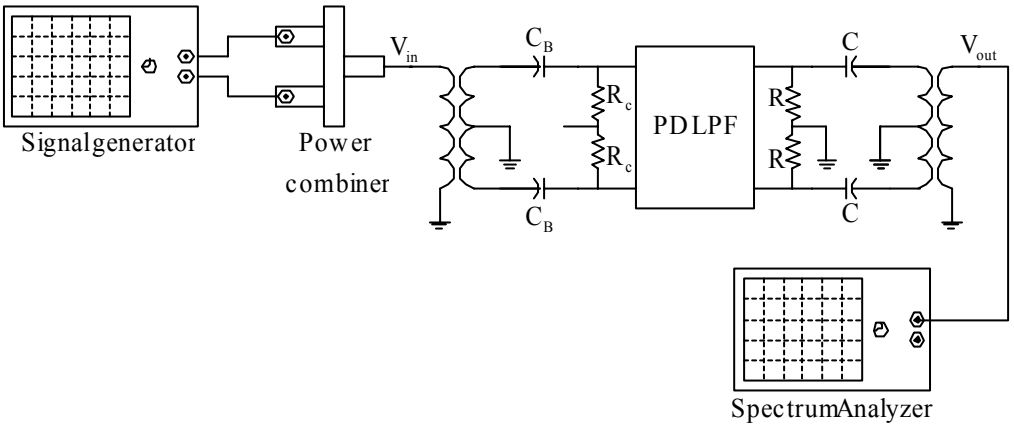


Fig. 6.14 Measurement setup for intermodulation distortion.

A source degenerated buffer, shown in Fig. 6.15, is used as buffer to characterize the OTA and the filter's performances. Fig. 6.16 shows the frequency spectrum of the buffer for a signal at 10.7 MHz with $1V_{PP}$ amplitude. Fig. 6.17 shows the frequency spectrum of the proposed OTA implemented in the structure of Fig. 6.4.

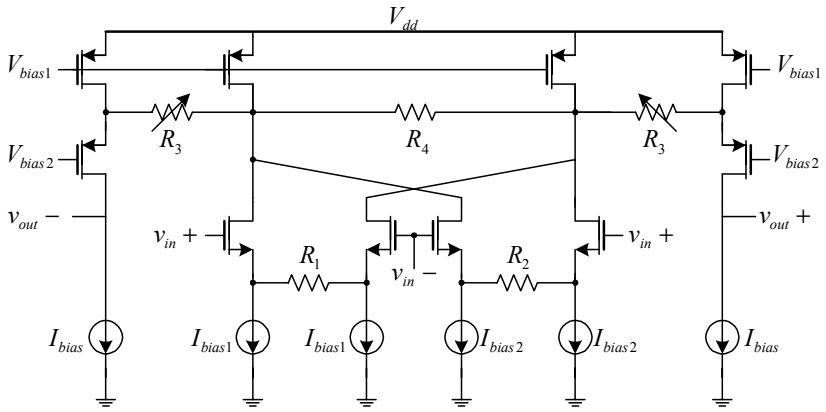


Fig. 6.15 Output buffer.

A HD3 of -69dB for an input signal at 10.7 MHz and 1 V_{PP} is obtained. Fig. 6.18 shows the two tones measurement result. The two tones are applied at 11.9 MHz and 12 MHz with total amplitude of 1 V_{PP}. The measured IM3 is -67dBm. Fig. 6.19 shows the IM3 measurement results for 10 different chips to explore the effect of the process variations on the OTA performance. The measured CMRR of the OTA is 55dB at 10 MHz and the measured input referred noise spectral density at 40 MHz is $1.1\,nV/\sqrt{Hz}$.

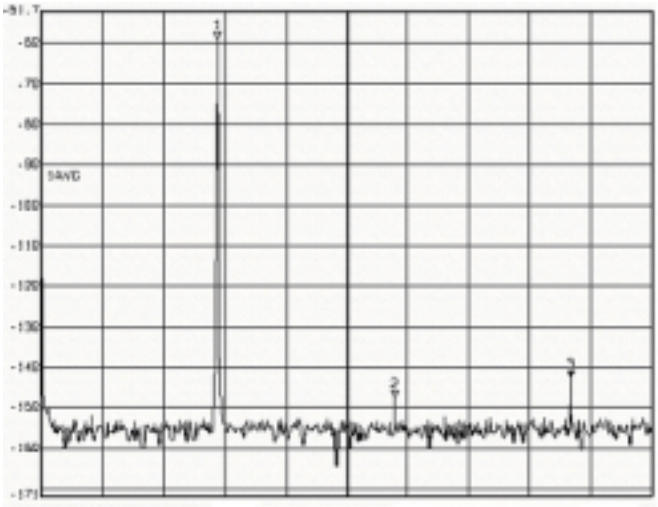


Fig. 6.16 Frequency spectrum of the output buffer.

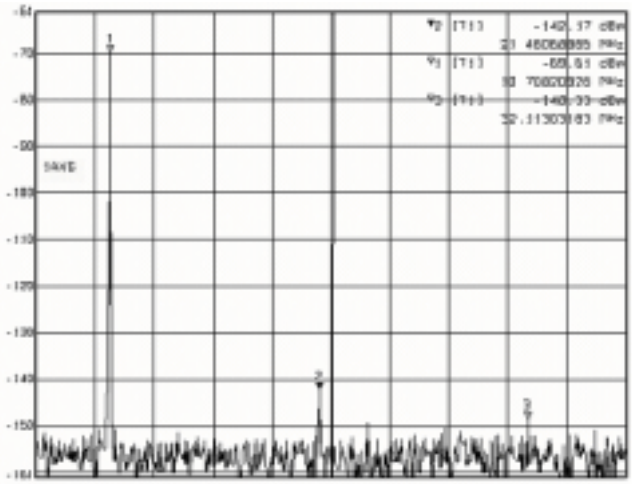


Fig. 6.17 Frequency spectrum of the proposed OTA.

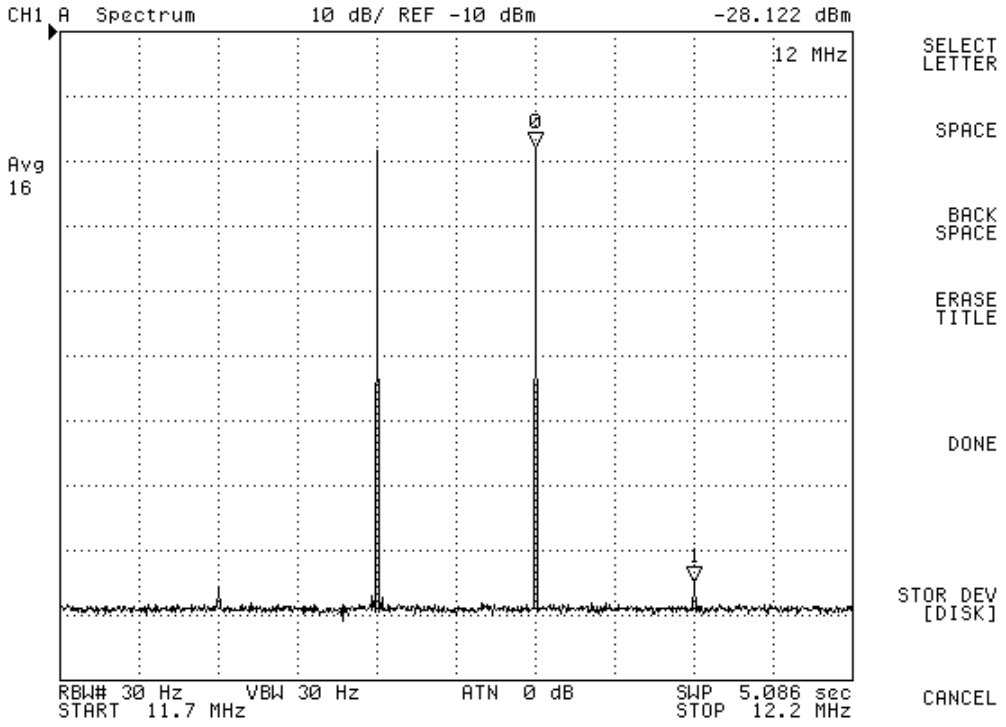


Fig. 6.18 IM3 measurement of the proposed OTA.

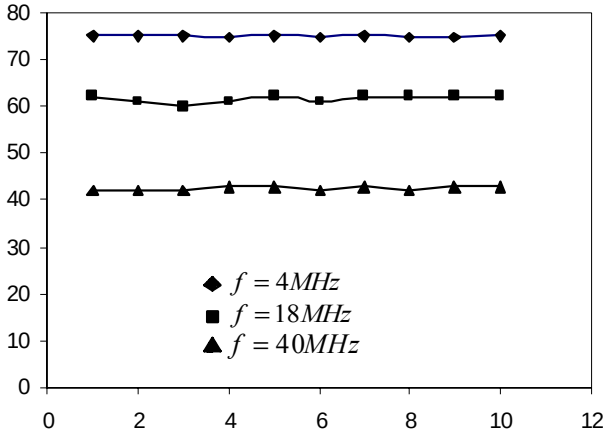


Fig. 6.19 Measured IM3 for 10 chips at three different frequencies.

Fig 6-20 shows the measured frequency response of the filter. The filter cut off frequency can be tuned from 12MHz to 24MHz. The total output noise integrated over a bandwidth of 12 MHz is about 300μVrms. This corresponds to 66dB of dynamic range for 0.5% total harmonic distortion (THD). Fig. 6.21 shows the two tone measurement result for the LPF. The two tones are applied at 11.9MHz and 12MHz with total amplitude of 1 V_{PP} and the measured IM3 is -63dBm. Fig. 6.22 shows the frequency response of the bandpass filter with the center frequency of 10.7MHz. Illustrated in Fig. 6.23, using two tones at 10MHz and 11MHz with 1Vpp total amplitude, an HD3 of -65dB can be obtained for the BPF. Table 6-2 compares the measured results of this work with the previously reported publications.

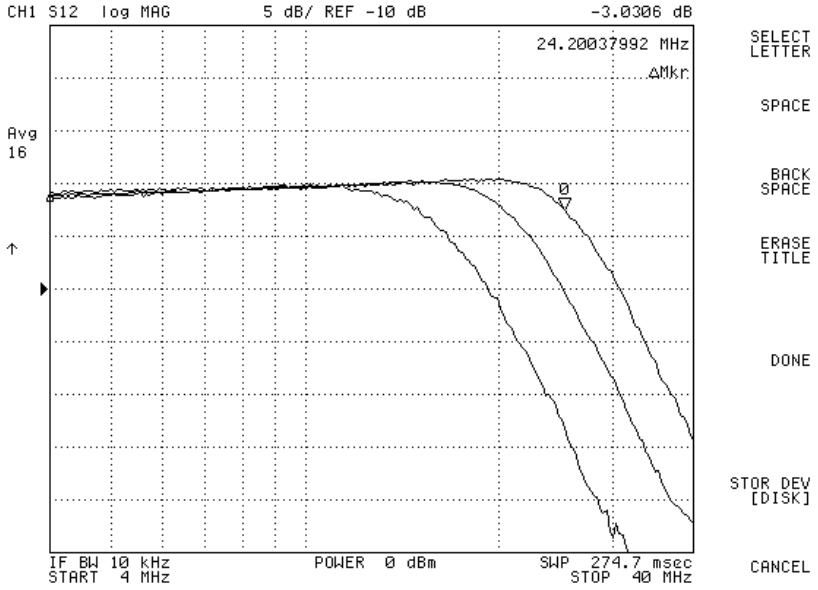


Fig. 6.20 Frequency response of the third-order filter.

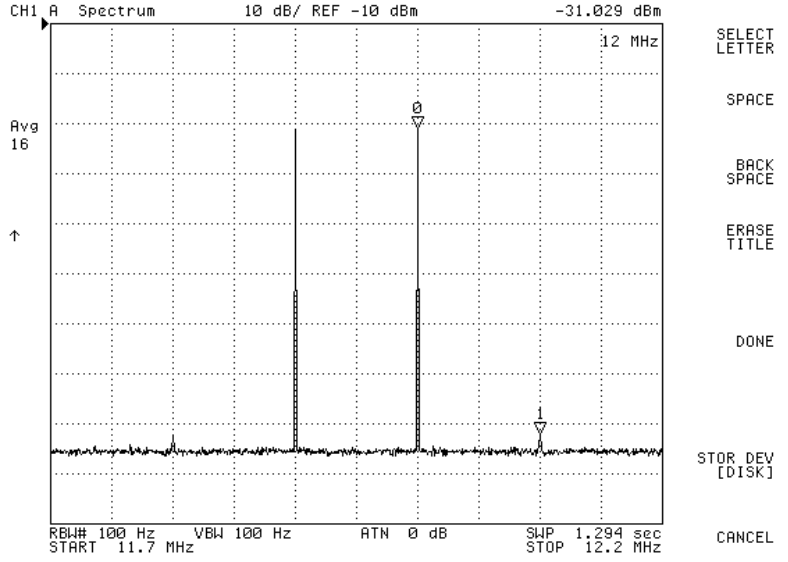


Fig. 6.21 IM3 measurement of the third-order LPF.

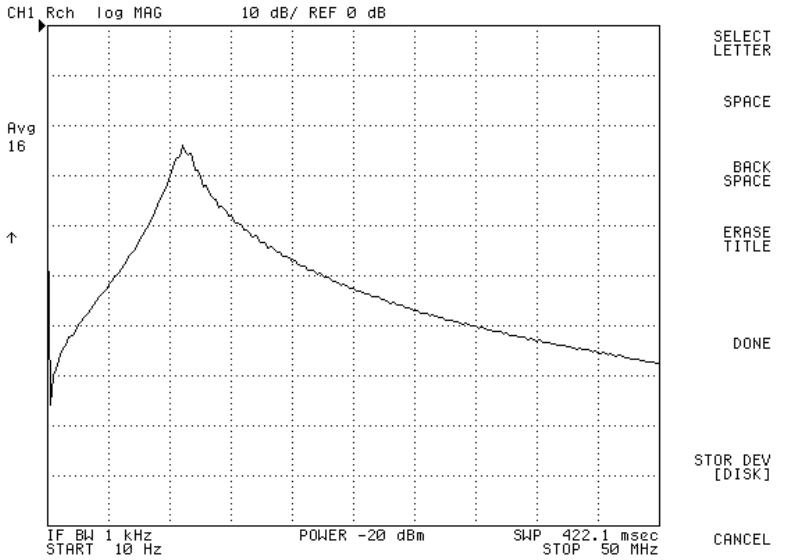


Fig. 6.22 Frequency response of the 2nd order band pass filter in Fig. 6.1.

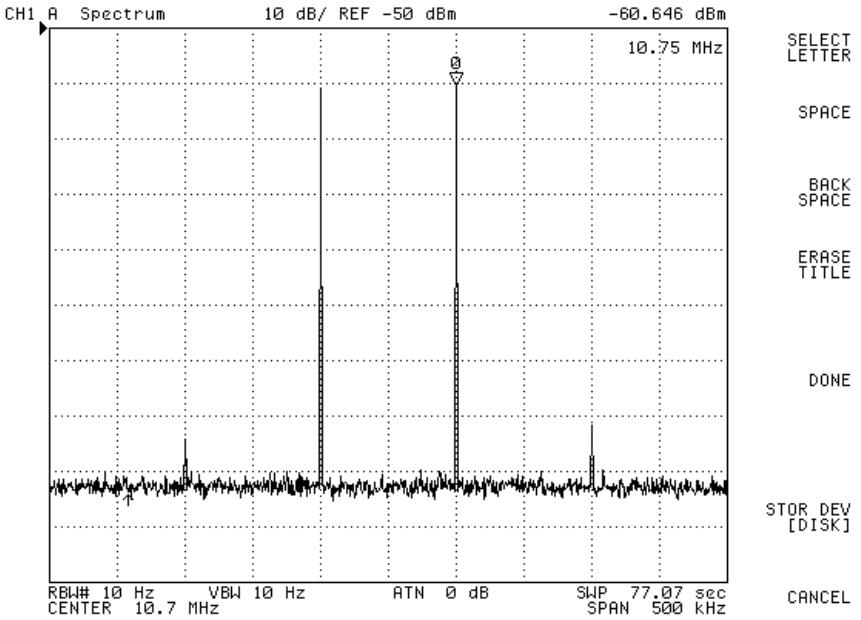


Fig. 6.23 IM3 measurement of the 2rd order BPF.

Table 6-2 Summary of experimental results of the PD LPF

Reference	[87]	[82]	This work
Filter order	5	4	3
f_{-3dB}	100 kHz	100 MHz	12 MHz-24 MHz
IM3 @ V_{in} @ frequency	-	40 dB 700 mVpp 100 MHz	63 dB 1 Vpp 12 MHz
Dynamic range	57 dB	45	66
Power supply	> 0.9 V	3.3V	3.3 V
Current consumption	10.5 μA	26 mA	20 mA
Area	0.2 mm^2	0.158 mm^2	0.105 mm^2
Technology	N/A	0.5μm CMOS	0.5μm CMOS

CHAPTER VII

A LOW THD BANDPASS-BASED OSCILLATOR USING MULTILEVEL HARD LIMITER

7.1. Introduction

Sine wave generators are required in a number of diverse application areas, including audio testing, calibration equipment, transducer drivers, power conditioning and automatic test equipment. As the other characteristics of integrated circuits improve with technology, the linearity and spectral purity of the signals generated in systems become increasingly important.

Producing and manipulating the sine wave function is a common problem encountered by circuit designers. A sinusoidal oscillator is a combination of a selective (linear) circuit to set the oscillation frequency, a power boosting element at the oscillation frequency, and an active element (limiter) to stabilize the oscillation amplitude [89].
To start up the oscillation, the poles of the linearized circuit have to be on the right half plane (RHP) of the complex frequency plane. The actual placement of the poles on the imaginary axis is due to the nonlinear components in a positive feedback loop.

The selective network is ideally composed entirely of linear elements and includes reactive components, which can be reduced to a simple resonant circuit or a bandpass filter. The active element has the essential feature of being nonlinear (hard limiter) and is assumed to be free from reactive parameters. Therefore its behavior is defined by a static characteristic of arbitrary shape. The property of the static characteristic of the nonlinear active element (limiter) essentially determines the level of

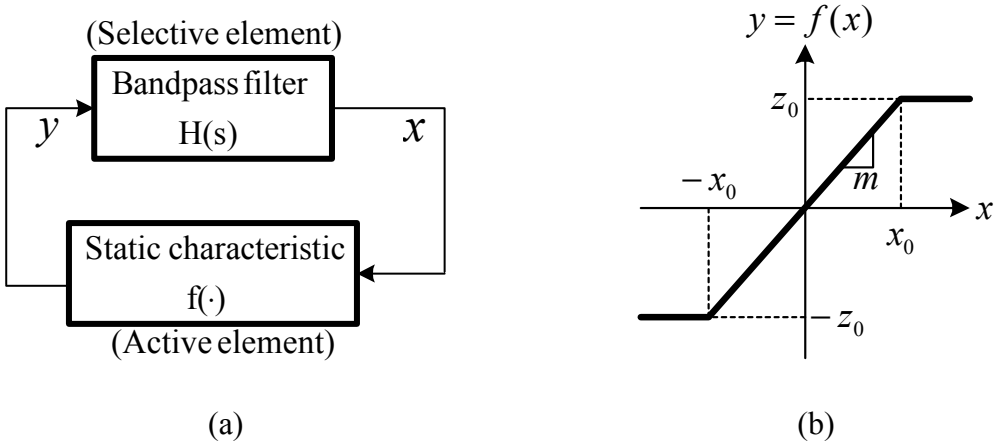
distortion of the generated sinusoidal signal. However, the nonlinearities may cause the oscillation frequency to deviate from that expected based on linear operation if the amplitude becomes excessive. For example in a master-slave tuning scheme a voltage controlled oscillator (VCO) with significant nonlinearities, even though locked to the external clock with a phase locked loop (PLL), results in a poor tracking operation. Thus, VCO linearity is critical and is maintained by controlling the amplitude of the oscillation so that the effect of the selective circuit nonlinearities on the oscillation frequency is minimized. Amplitude control can be achieved with an automatic gain control circuit or more simply with a carefully designed hard limiter circuit.

LC tank [90] and active-RC [91] circuits are among the most popular approaches to implement oscillators. While for practical reasons the former approach is not preferred for implementations at relatively low-frequencies, the later one suffers from the frequency limitation of the active elements (Opamp) operating in closed loop. Operational transconductance amplifier (OTA) based oscillators seems to be a better solution for frequencies below GHz due to the fact that they have high frequency poles and operate in open loop architectures [92].

7.2. Bandpass-Based Oscillator Theory

The bandpass-based oscillator, shown in Fig. 7.1(a), consists of a bandpass filter as the selective element together with a hard limiter as the active element in positive feedback [92]-[94]. The conventional oscillator uses a two level comparator as indicated in Fig. 7.1(b) where $|Z_0|$ is the clamping amplitude and x_0 is the threshold for the input

signal. i.e., $f(x)=x$ for $x<x_0$ and $f(x)=Z_0$ for $x>x_0$. A sound use of the bandpass filter in this structure allows decoupling the amplitude and frequency controls of the oscillator.



(a) (b)

Fig. 7.1 (a) Bandpass based oscillator model (b) Conventional static characteristic.

That is, the oscillation amplitude is indirectly controlled by the clamping levels $|Z_0|$ of the active element (comparator) while the oscillation frequency is changed by tuning the center frequency of the bandpass filter. The above property is due to the fact that only at the center frequency of the bandpass filter the loop gain phase becomes zero. If the gain in the feedback loop is made much larger than unity (before clamping), the feedback loop can be viewed as a sine-to-square wave converter. Due to the presence of the bandpass filter which attenuates the harmonics of the square wave but the fundamental one, the describing function (DF) [95] method can be used to study the dynamic behavior of the loop. In this technique, the input of the nonlinearity is assumed to be an undistorted sinusoidal signal, $x(t)=A_0\sin(\omega_0 t)$. The higher order harmonics present in the output signal $y(t)$ in Fig. 7.1(a) are supposed to be filtered out sufficiently

by the bandpass filter. Assuming $A_0 > x_0$, the amplitude of the fundamental component $a\sin(\omega_0 t)$ of $y(t)$ can be found from its Fourier series as

$$a = \frac{1}{T}\int_{-T/2}^{T/2} f(A_0 \sin\omega_0 t)\sin\omega_0 t dt \tag{7-1a}$$

$$a = \frac{2mA_0}{\pi}\left[\sin^{-1}\left(\frac{x_0}{A_0}\right) + \frac{x_0}{A_0}\sqrt{1-\left(\frac{x_0}{A_0}\right)^2}\right] \tag{7-1b}$$

where, m is the slope of the non-linear characteristic in Fig. 7.1(b) and T is the period of the signal.

Thus, the describing function of the nonlinear block in Fig. 7.1(b), which is the linear gain relating the amplitude of the fundamental component at the output to that of the input, can be expressed as

$$N(A_0) = \frac{a}{A_0} = \begin{cases} \dfrac{2m}{\pi}\left[\sin^{-1}\left(\dfrac{x_0}{A_0}\right) + \dfrac{x_0}{A_0}\sqrt{1-\left(\dfrac{x_0}{A_0}\right)^2}\right] & A_0 > x_0 \\ m & A_0 < x_0 \end{cases} . \tag{7-2}$$

Therefore, the hard limiter function $f(\cdot)$ in Fig. 7.1(a) can be expressed as a piece-wise linear function which its slope depends on the oscillation amplitude A_0, i.e., $\frac{df(x)}{dx} = \frac{y}{x} \approx N(A_0)$. Hence, the describing function of the whole oscillator in Fig. 7.1(a) can be related to the transfer function of the bandpass filter ($H(s)$) as

$$H(s) = \frac{X(s)}{Y(s)} = \frac{1}{N(A_0)} . \tag{7-3}$$

Assume the bandpass filter has the following transfer function

$$H(s) = \frac{k_0 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{7-4}$$

where, Q and ω_0 are the quality factor and the center frequency of the bandpass filter, respectively.

Using (7-3) and (7-4), the time domain differential equation associated with the closed loop block diagram of Fig. 7.1(a) can be written as

$$\frac{d^2 x(t)}{dt^2} + \frac{dx(x)}{dt}\left[\frac{\omega_0}{Q} - k_0 N(A_0)\right] + \omega_0^2 x(t) = 0 \,. \tag{7-5}$$

Once the steady state is achieved, i.e. when the coefficient of $dx(t)/dt$ in (7-5) becomes zero, the oscillation amplitude A_0 can be determined from (7-5). This is due to the fact that the poles placement at the resonant frequency has to be just on the imaginary axis.

$$A_0 \cong N^{-1}\left(\frac{\omega_0}{k_0 Q}\right). \tag{7-6}$$

Observe that the oscillation frequency is equal to ω_0 and independent of the oscillation amplitude. Next we propose a multilevel hard limiter scheme that combined with a bandpass filter yields an enhanced THD of the bandpass-based oscillator waveform.

7.3. Proposed Multilevel Hard Limiter

Little has been reported in the literature regarding the optimum shape of multilevel hard limiter (static characteristic) block in order to minimize its output harmonic distortion. Regarding the possible nonlinearities to be used in the feedback loop of Fig. 7.1(a), some restrictions must be made; otherwise the study of the oscillation

made by the describing function (DF) methodology is not feasible. We will exclusively focus on switching characteristics, i.e., slopes are only zero or infinity. Furthermore, practical implementation of these elements is relatively easy.

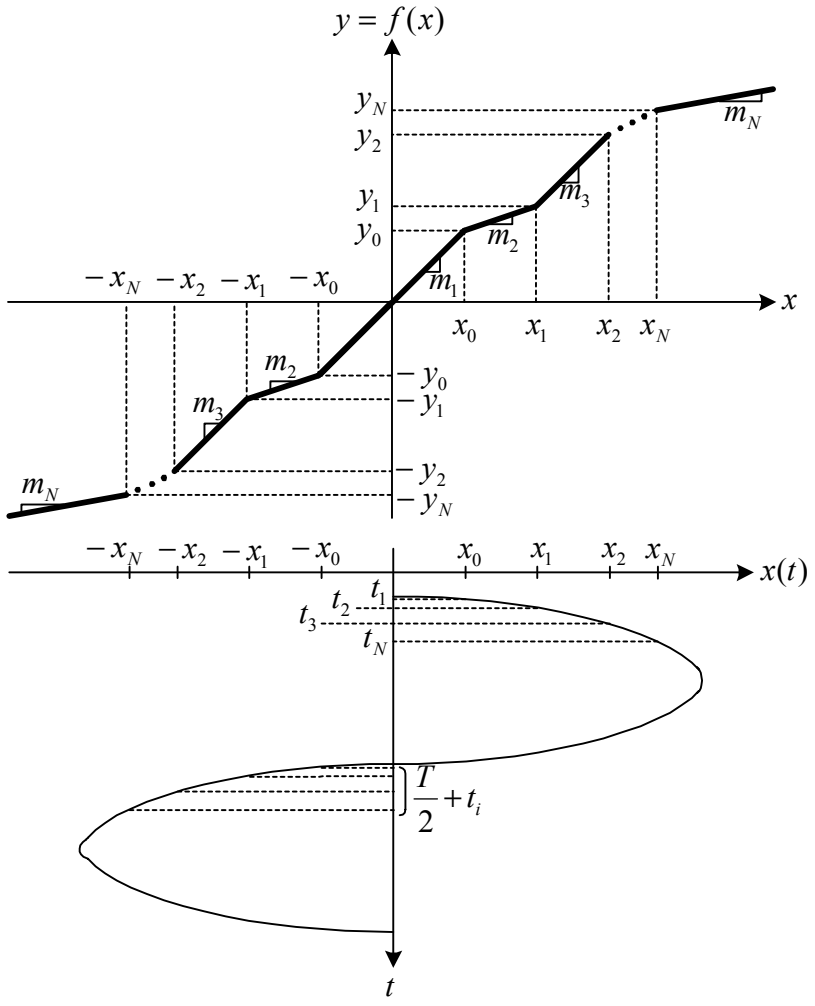


Fig. 7.2 Generalized static characteristic.

7.3.1. *Optimum Static Characteristic* (*Multilevel Hard Limiter*)

For the generalized static characteristic in Fig. 7.2, the output must be bounded therefore the slope of m_N should be zero, where N is the number of levels.

To determine the remaining slopes in Fig. 7.2, the input and output of the static characteristic block are assumed to be $x(t)\approx A_0\sin\omega_0 t$ and $y(t)\approx a\sin\omega_0 t$, respectively. Note, due to the odd symmetry of Fig. 7.2, $y(t)$ does not contain any cosine terms. To find the output amplitude a, the time t_i where the input amplitude A_0 exceeds the voltage level of x_i must be known.

$$t_i = \frac{1}{\omega_0}\sin^{-1}\left(\frac{x_i}{A_0}\right) \quad ; i = 1, 2, \mathrm{K}\ , N-1. \tag{7-7}$$

Using (7-1a) and $f(x)$ for different intervals of x in Fig. 7.2 the output amplitude a with m_N=0 can be found as

$$a = \frac{A_0}{2\pi}\sum_{i=1}^{N-1}\sum (m_{i+1} - m_i) r(\rho_i) \tag{7-8}$$

where,

$$r(\rho_i) = \frac{2}{\pi}\left[\sin^{-1}(\rho_i) + \rho_i\sqrt{1-\rho_i^2}\right] \tag{7-9}$$

and,

$$\rho_i = x_i / A_0 \tag{7-10}$$

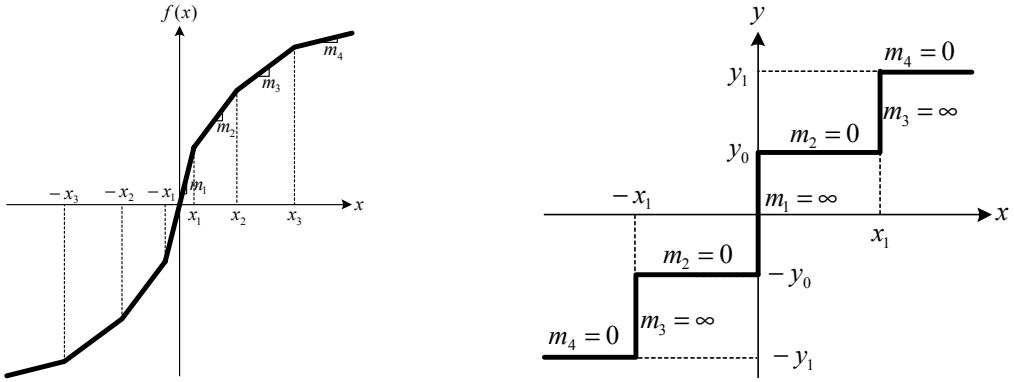
Thus, based on (7-8) the describing function of Fig. 7.2 can be expressed as

$$N(A_0) = \frac{1}{2\pi}\sum_{i=1}^{N-1}\sum (m_{i+1} - m_i) r(\rho_i)\,. \tag{7-11}$$

Suitable choices of $r(\rho_i)$ and m_i can minimize the output harmonics. This is explored next. As an example, a system with N=4 will be analyzed. The transfer characteristic of the analyzed system is shown in Fig. 7.3(a). The describing function can be found as

$$N(A_0)=\frac{1}{2\pi}\left(m_3 r(\rho_3)+(m_2-m_3)r(\rho_2)+(m_1-m_2)r(\rho_1)\right). \tag{7-12}$$

When the circuit reaches a steady-state oscillation (i.e. $s=j\omega_0$) the slopes of the hard limiter characteristic of Fig. 7.3(a) can be obtained using equations (7-6) and (7-12).



(a) (b)

Fig. 7.3 (a) 4-level static characteristic (b) 4-level MHL optimized to reduce THD.

$$m_1=\frac{\frac{2\pi\omega_0}{k_0 Q}-m_3\left(r(\rho_3)-r(\rho_2)\right)-m_2\left(r(\rho_2)-r(\rho_1)\right)}{r(\rho_1)} \tag{7-13}$$

$$m_2=\frac{\frac{2\pi\omega_0}{k_0 Q}-m_3\left(r(\rho_3)-r(\rho_2)\right)-m_1 r(\rho_1)}{r(\rho_2)-r(\rho_1)} \tag{7-14}$$

$$m_3=\frac{\frac{2\pi\omega_0}{k_0 Q}-m_1 r(\rho_1)-m_2\left(r(\rho_2)-r(\rho_1)\right)}{r(\rho_3)-r(\rho_2)}. \tag{7-15}$$

Using (7-8) for N=3, the Fourier series coefficients a_n of the output of the MHL block for $A_0>x_2$ can be calculated as

$$a_n = (m_1 - m_2)P_n(\rho_1) + (m_2 - m_3)P_n(\rho_2) + m_3 P_n(\rho_3), \quad n = 1, 3, 5, 7, \Lambda \tag{7-16}$$

where, the index *n* represent the odd harmonics.

The P_n functions are introduced to simplify the notation for a_n. The P_n functions to calculate the first four odd harmonics are shown in Table 7-1.

Table 7-1 $P_n(\rho_i)$ functions for a_n, i=1, 3, 5 and 7

n=1	$P_1(\rho_i) = r(\rho_i)$
n=3	$P_3(\rho_i) = -2\rho_i^3\sqrt{1-\rho_i^2}$
n=5	$P_5(\rho_i) = \frac{2}{3}\rho_i(3-4\rho_i^2)\sqrt{1-\rho_i^2(3-4\rho_i^2)^2} - 2\rho_i(1-2\rho_i^2)\sqrt{1-\rho_i^2}$
n=7	$P_7(\rho_i) = \frac{\rho_i}{3}(1-2\rho_i^2)\sqrt{(1-\rho_i^2)\left(1-16\rho_i^2(1-2\rho_i^2)(1-\rho_i^2)\right)} - -\frac{2}{3}\rho_i(3-4\rho_i^2)\sqrt{1-\rho_i^2(3-4\rho_i^2)^2}$

It is important to note that for all $P_n(\rho_i)$ functions in Table I $P_n(0)$=0. This property will be exploited to find the optimum slopes of the non-linear characteristic of Fig. 7.2 and Fig. 7.3(a) to null the third and the fifth harmonic components.

If $\rho_2 = \rho_3$, the expression for a_n can be simplified to

$$a_n = (m_1 - m_2)P_n(\rho_1) + m_2 P_n(\rho_2), \quad n = 1, 3, 5, 7, \Lambda \ . \tag{7-17}$$

Analyzing Fig. 7.3(a) and using $\rho_2 = \rho_3$, which implies $r(\rho_2)=r(\rho_3)$ and $x_2=x_3$, results in $m_3 = \infty$. The same result could have been obtained from (7-15) knowing $r(\rho_2)=r(\rho_3)$ implying a denominator of zero.

Our ultimate goal is to minimize the number of harmonics at the output of the multilevel hard limiter. The first step in doing this was setting $m_3 = \infty$. To further simplify a_n, the remaining terms must be reduced. The second term in (7-17) can be made zero by choosing $m_2=0$, or by setting $\rho_2=0$ implying $x_2=0$. When m_3 was set to infinity previously, x_2 was made equal to x_3. Therefore, $x_2=x_3=0$ would result in $m_1=m_2=m_3=\infty$ and the static characteristic in Fig. 7.3(a) would result in a two-level hard limiter (comparator). From here, the scenario of $m_2=0$ is a better option to null the second term without compromising the characteristic of the active element.

To null the remaining term in (7-17), there are two possibilities. First, m_1 can be set to 0. However, this choice of $m_1=0$ results in a dead band in the characteristic of the nonlinear block and prevents the start-up of the oscillator (see Fig. 7.3(a)). The second method to cancel the first term in (7-17) would be to set $\rho_1=0$. Having $\rho_1=0$ implies $x_1=0$ and $r(\rho_1)=0$ which makes $m_1 = \infty$. From (7-13), having $r(\rho_1)=0$ will also result in $m_1 = \infty$, verifying the result. Fig. 7.3(b) shows the resultant 4-level MHL with $m_1 = \infty$, $m_2 = 0$, $m_3 = \infty$ and $m_4 = 0$.

Note that in (7-17), the product of m_i and $P_i(\rho_1)$ cannot be zero ($m_i \times P_i(\rho_1)=\infty\times 0$). This multiplication implies a_i must always have a finite value. Although the output harmonics cannot be made zero, the THD at the output of the active element can be minimized if odd slopes ($m_1, m_3, m_5, \ldots$) are made infinite and even slopes ($m_2, m_4, m_6, \ldots$) are made zero.

From the previous example where $N=4$, a more general output static characteristic can be obtained to minimize the output harmonics of the hard limiter. For even integer number of levels N it is required that $N=2^k$, where k is an integer number. The

generalized static characteristic for minimized output harmonics is shown in Fig. 7.4. Next the detailed analysis of finding the optimum values of x_i's and y_i's to null the third and the fifth order harmonics at the output of the MHL block is presented.

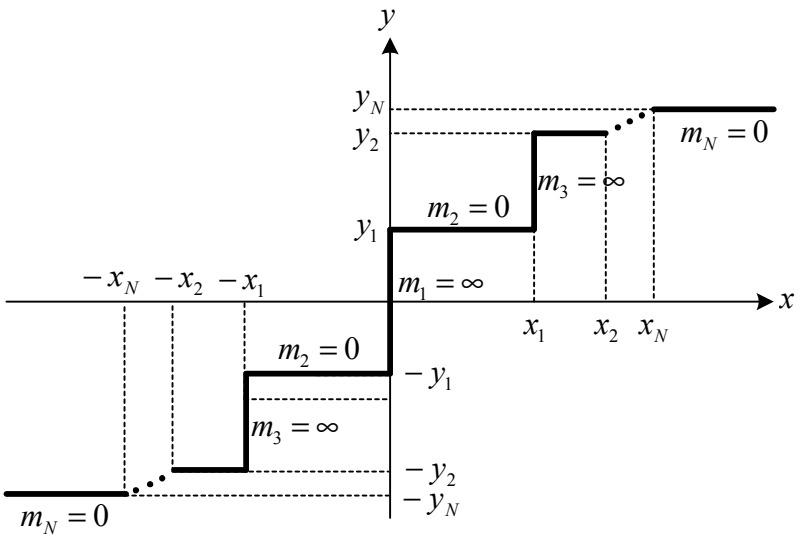


Fig. 7.4 Generalized static characteristic for minimum output harmonics

7.3.2 *Time Domain Characterization*

Previously, the slopes of the MHL block were determined based on a combination of a general analysis and a specific example. However, to implement the MHL block into a practical system, the values of x_i and y_i must be exactly determined. If a sine wave is applied as the input to the generalized static characteristic shown in Fig. 7.4, the resulting positive half wave is shown in Fig. 7.5. To obtain the values of x_i and y_i, a Fourier analysis must be performed on the output of the MHL (see Fig. 7.5).

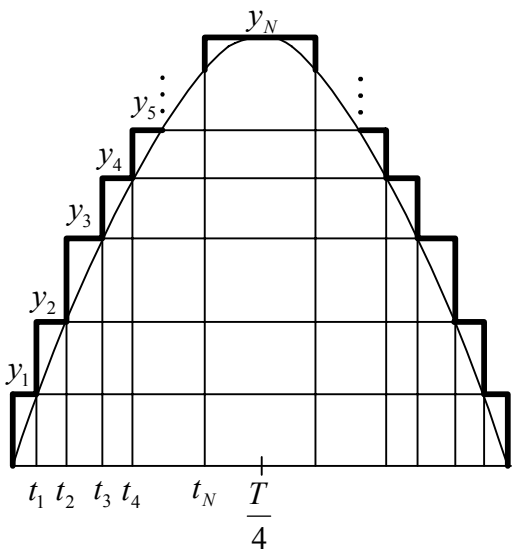


Fig. 7.5 Output of MHL for N slopes and a sine wave input.

To begin, a simple comparator will be used as the limiter building block. The reference level of this block will be taken as zero such that the generated output will be a square waveform. The output of this comparator with a reference of zero will be denoted $f_o(t)$. There are two methods which may be used to obtain the output waveform shown in Fig. 7.5.

The first implementation focuses on using the sum of the outputs of $2N$-1 comparator's with different references of $\pm y_i$. However, if this method is used, besides the increased power consumption and complexity, the exact times (t_i) where the output's are summed will vary based on fluctuations in the reference levels of the different comparator's. These fluctuations will produce an unwanted output waveform which could cause the system to not operate as desired.

The second implementation to obtain the MHL output as shown in Fig. 7.5 is based on using only one comparator with a reference voltage of zero. To illustrate this

methodology, again we use the previous example of a 4-level static characteristic. The output of this block for a sinusoidal input is shown in Fig. 7.6.

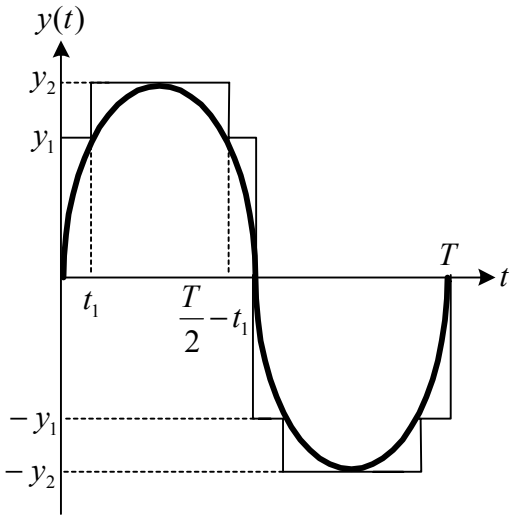


Fig. 7.6 Input (thin) and output (thick) of the nonlinear characteristic of Fig. 7.3(b).

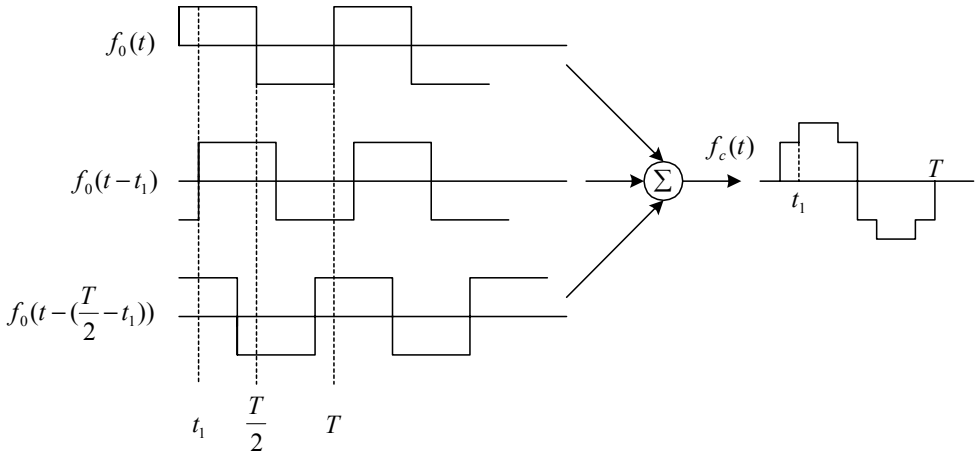


Fig. 7.7 Decomposition of the output of the MHL block.

As depicted in Fig. 7.7, the output of this block $f_c(t)$ can be obtained by summing $f_0(t)$ (ideal comparator output) together with two other properly scaled and time shifted versions of $f_0(t)$.

$$f_c(t) = y_1 f_0(t) + \frac{y_2}{2} f_0(t - t_1) - \frac{y_2}{2} f_0(t - (\frac{T}{2} - t_1)) \tag{7-18}$$

where, y_1 and y_2 are amplitudes of the stairs of waveform of Fig. 7.6

Note that due to the symmetry of $f_c(t)$, the even harmonics of its Fourier series are zero. The first odd harmonics of $f_c(t)$ can be expressed as

$$a_c(\omega_0) = y_2 \left\{ \frac{y_1}{y_2} + \cos\left(\frac{2\pi}{T_1} \right) \right\} a_0(\omega_0) \tag{7-19}$$

$$a_c(3\omega_0) = y_2 \left\{ \frac{y_1}{y_2} + \cos\left(\frac{6\pi}{T_1} \right) \right\} a_0(3\omega_0) \tag{7-20}$$

$$a_c(5\omega_0) = y_2 \left\{ \frac{y_1}{y_2} + \cos\left(\frac{10\pi}{T_1} \right) \right\} a_0(5\omega_0) \tag{7-21}$$

where, $T_1=T/t_1$ and $a_0(n\omega)$ and $a_c(n\omega)$, n=1, 3 and 5, are the coefficients of the Fourier series of $f_0(t)$ and $f_c(t)$, respectively.

A careful examination of (7-20) and (7-21) shows that in the case of a linear relation between y_1 and y_2, a proper value of T_1 can make the two terms inside the brackets zero. To find this proper value of T_1, the terms of $\cos(i\pi / T_1)$ for i=2, 6 and 10 as functions of T_1 are plotted in Fig. 7.8. In order to simultaneously null the third and the fifth order harmonics, it is required that T_1=8 which yields $\cos(6\pi/T_1)=\cos(10\pi/T_1)=-\sqrt{2}/2$. Thus, to make (7-20) and (7-21) zero, y_1 and y_2 have to be related as

$$\frac{y_2}{y_1} = \sqrt{2}\,. \tag{7-22}$$

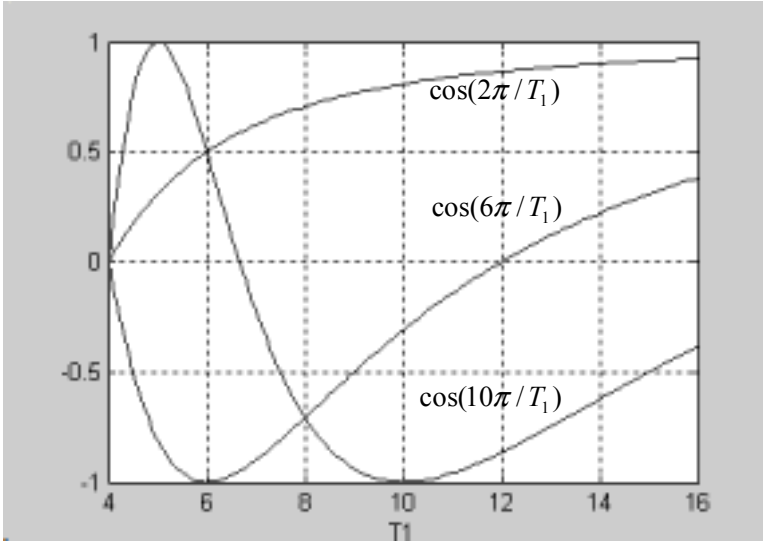


Fig. 7.8 $\cos(i\pi / T_1)$ for i=2, 6 and 10 as functions of $T_1=T/t_1$.

7.3.3. *General Case: Multilevel Hard Limiter*

From the previous example, a general expression for the output $f(t)$ of the MHL block in Fig. 7.5 can be derived by induction as

$$f_c(t) = f_0(t) + \sum_{i=1}^{N-1} \left\{ y_i f_0(t - t_i) - y_i f_0\left(t - \left(\frac{T}{2} - t_i \right) \right) \right\}. \tag{7-23}$$

By substituting (7-23) into (7-1a), the following expression for the Fourier series of the output signal $f_c(t)$ can be found.

$$a_c(n\omega_0) = a_0(n\omega_0) \left\{ 1 + \sum_{i=1}^{N-1} \left[y_i \left(1 - (-1)^n \right) \cdot \cos(\omega_0 t_i) \right] \right\}, \; n = 3, 5, 7, \Lambda \tag{7-24}$$

where, $a_c(n\omega_0)$ and $a_0(n\omega_0)$ are the Fourier series coefficients of $f_c(t)$ and $f_0(t)$, respectively.

It can be demonstrated that for specific values of k and n, the following expressions of t_i and y_i make (7-24) zero.

$$t_i = \frac{T}{2^{K+2}} i, \quad i = 1, 2, 3, \Lambda \tag{7-25}$$

$$y_i = \cos\left(\frac{\pi}{2^{K+1}} i\right), \quad i = 1, 2, 3, \Lambda \tag{7-26}$$

The above fact has been visualized in Fig. 7.9 for k=1, 2, 4, and 8 and $n=f/f_0$.

In the case of 4-level MHL, i.e. k=2 in Fig. 7.9, the absence of the third and the fifth order harmonics in the frequency spectrum of the output signal of the proposed MHL has a significant effect on increasing the spectrum purity of the sinusoidal output without any extra effort to implement a significantly high-Q bandpass filter. The harmonic distortion expressions for different number of levels are presented in Table 7-2.

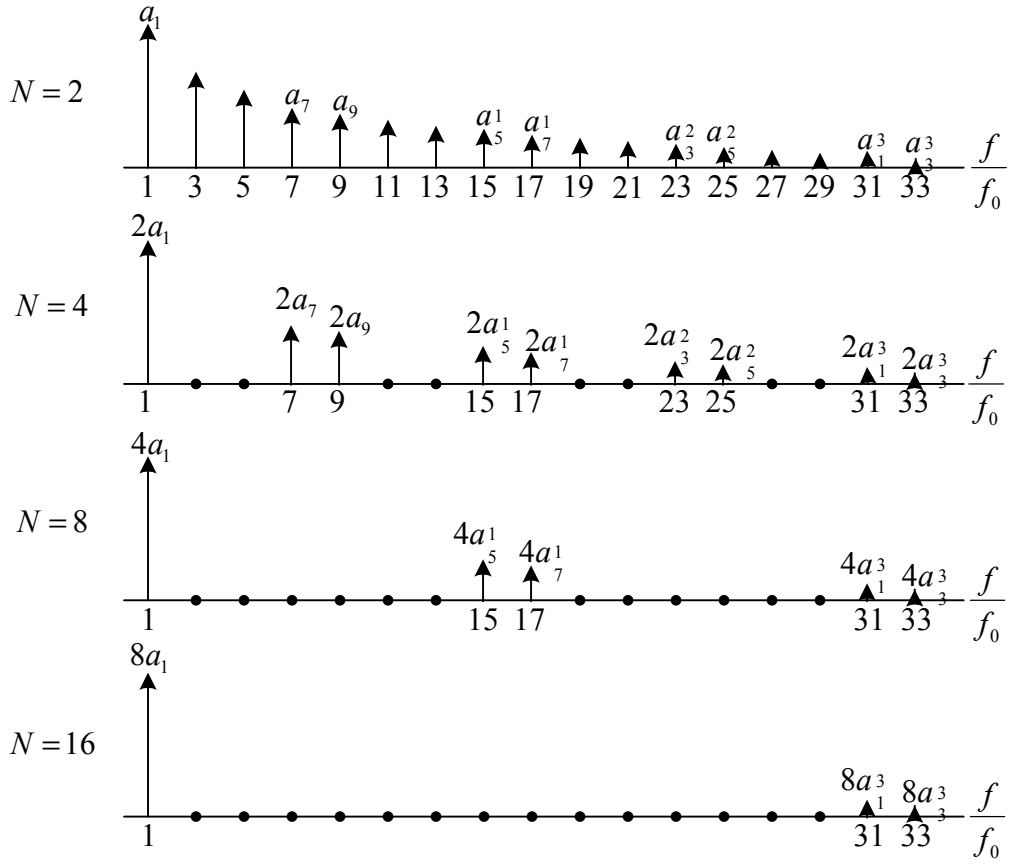


Fig. 7.9 Frequency spectrum of the MHL (limiter) with different possible levels.

Table 7-2 Comparison of THD expressions for different levels

Number of levels	THD
N=2	$\sqrt{HD_3^2+HD_5^2+HD_7^2+HD_9^2+HD_{11}^2+HD_{13}^2+\Lambda}$
N=4	$\sqrt{HD_7^2+HD_9^2+HD_{15}^2+HD_{17}^2+HD_{23}^2+HD_{25}^2+\Lambda}$
N=8	$\sqrt{HD_{15}^2+HD_{17}^2+HD_{31}^2+HD_{33}^2+\Lambda}$
N=16	$\sqrt{HD_{31}^2+HD_{33}^2+\Lambda}$

7.3.4. *Non-Ideal Effects*

In implementation of $f_c(t)$, based on (7-23), the main sources of non-idealities are finite slops (m_i) and inaccuracy in the switching time t_i. Considering the above effects, the output waveform of the previously studied 4-level MHL block in Fig. 7.3 can be modeled as the waveform shown in Fig. 7.10. In this figure, the deviation of the slopes from their ideal (infinity) values correspond to the deviation of t_0 and t_1 from their ideal values, zero and $T/8$, respectively. The nth Fourier series coefficient, taking into account these non-idealities, can be calculated as

$$\hat{a}_c(n\omega_0)=\frac{\left(1-(-1)^n\right)\mathrm{sinc}(\frac{n\omega_0 t_0}{2})}{n\pi}\left[y_1\cos(\frac{n\omega_0 t_0}{2})+(y_2-y_1)\cos\left(n\omega_0(t_1+\frac{\Delta t_1}{2})\right)\right] \quad (7\text{-}27)$$

.

where, $\Delta t_1=(y_2-y_1)/m_3$ and $t_0=y_1/m_1$.

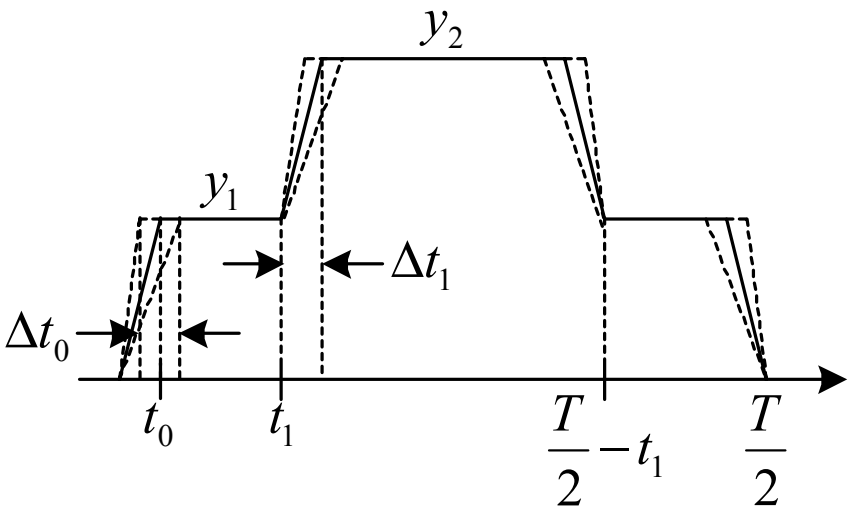


Fig. 7.10 Non-ideal effects due to finite slopes of Fig. 7.3.

Note that for Δt_1=0 and t_0=0, (7-27) becomes (7-24). The overall THD of this waveform as well as the third and the fifth order harmonic distortions (HD3 and HD5) are shown in Fig. 7.11 and Fig. 7.12, respectively. The horizontal axes correspond to t_0 and t_1 and the vertical axis corresponds to distortion. Note that for values of $t_0 \neq 0$ and $t_1 \neq T/8$, the HD3 and the HD5 grew drastically from zero while the overall THD improves.

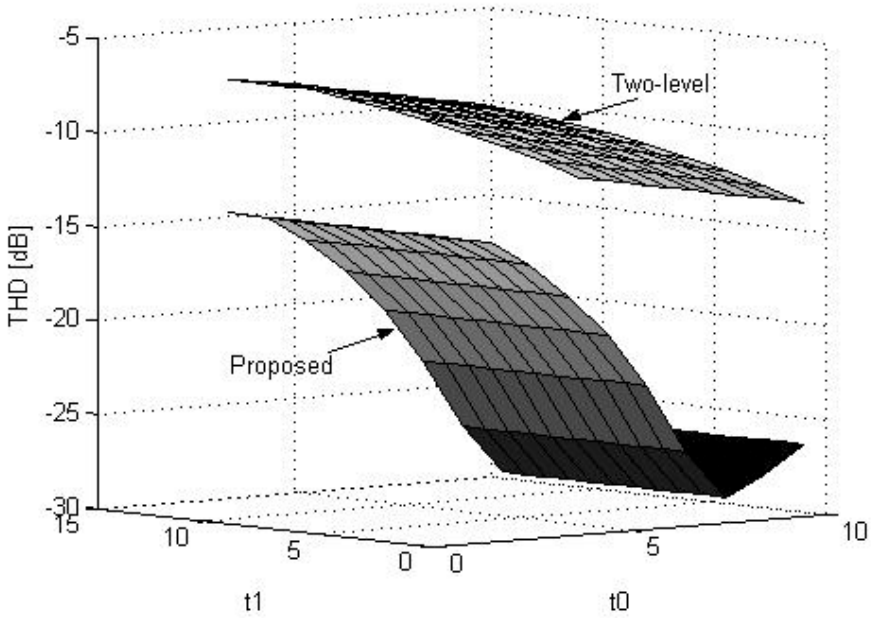
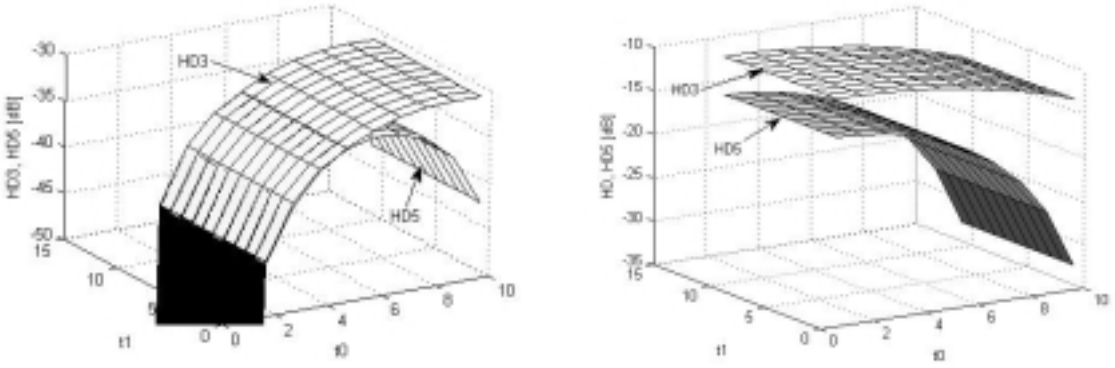


Fig. 7.11 THD of the proposed 4-level and the two-level (comparator) MHL's as a function of t_0 and t_1 in Fig. 7-6



(a) (b)

Fig. 7.12 HD3 and HD5 as a function of t_0 and t_1 for (a) proposed 4-level MHL (b) two-level (comparator) MHL.

The improvement in the THD is expected due to finite slopes but it is not of interest since the higher harmonics of the output get attenuated by the bandpass filter

anyway. However, as Fig. 7.12 shows, even with deviation of t_0 and t_1 from their ideal values, the HD3 and the HD5 of the proposed MHL are considerably below their corresponding values for the conventional two-level hard limiter.

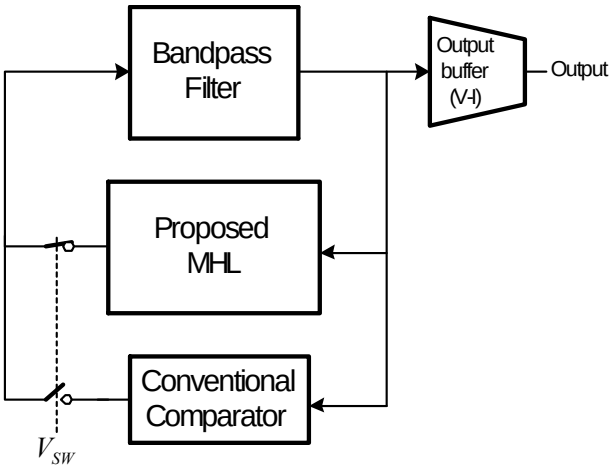


Fig. 7.13 Overall block diagram of the oscillator for testing purpose.

7.4. Circuit Implementation

Fig. 7.13 shows the overall block diagram of the fabricated chip. A conventional two-level hard limiter (comparator) is included in the design to compare its performance against the proposed MHL block. A linearized transconductance buffer [98] is employed to monitor the output signal.

7.4.1. *Bandpass filter design*

To increase the linearity of the oscillator, besides increasing the Q, the nonlinearities associated with the bandpass filter need to be minimized. Hence, a bandpass filter using the linearized pseudo-differential OTA [96] has been designed. Fig. 7.14(a) shows the block diagram of the two-integrator loop biquad Gm-C filter. This topology is often preferred with respect to other versions since an additional low pass

output is available. Furthermore, it has the advantage of allowing the control of the common-mode voltage at both integrator outputs. In addition a minimum sensitivity of the quality factor with respect to capacitance mismatch is achieved by choosing C1=C2 [97].

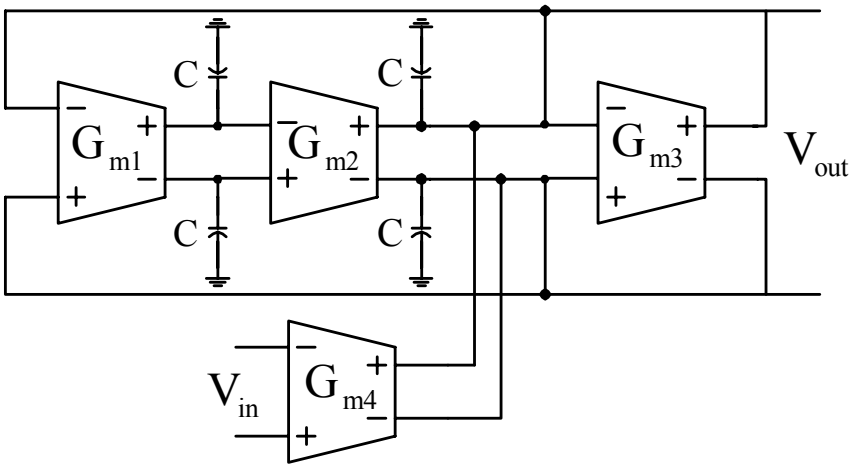


Fig. 7.14 (a) Biquad Gm-C BPF.

7.4.2. *MHL Static Characteristic Implementation*

The main challenge in implementing the nonlinear characteristic of the MHL in Fig. 7.3(b) is the accuracy of the comparison of the sinusoidal input with zero and x_1. This problem can be avoided by emulating the performance of the static characteristic based on the decomposition of the waveforms in square waves as shown in Fig. 7.7. In this technique the output signal of the bandpass filter is only compared with zero and two independent delay lines generate the other two time-shifted waveforms. Its implementation is shown in Fig. 7.15. This implementation requires three tasks of comparison, time delay and digital to analog (DAC) conversion. The input comparator

compares the input signal with ground to generate the base square wave $f_0(t)$ in Fig. 7.7. Two separate delay lines generate $f_0(t\text{-}t_1)$ and $f_0(t\text{-}(T/2\text{-}t_1))$. In order to properly adjust the delay times, the delay cells on the signal path can be configured using two DMUX cells. However, for simplicity these DMUX cells are not incorporated in our design and the delay cells are controlled using only a 3-bit control word. The total numbers of inverters used in this design for $f_0(t\text{-}t_1)$ and $f_0(t\text{-}(T/2\text{-}t_1))$ are 8 and 24, respectively.

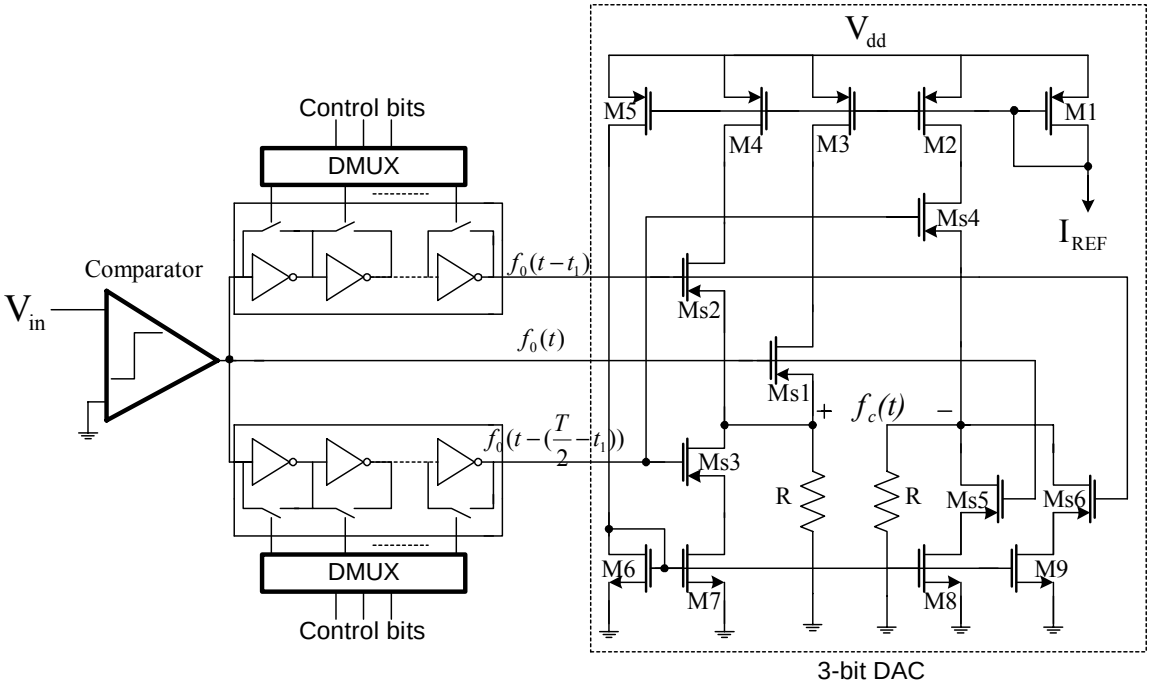


Fig. 7.15 Implementation of the proposed MHL block.

The square wave $f_0(t)$ and its delayed versions are controlling two groups of switches, Ms1-Ms3 and Ms4-Ms6, which conceptually form a 3-bit DAC circuit. Transistors M1-M9 provide the reference currents for the switches Ms1-Ms6. The three switches of Ms1-Ms3 generate the positive portion of the composite pulse $f_c(t)$ while its negative portion is generated by Ms4-Ms6. The currents of these two groups of switches

after being summed up at the output nodes, across $f_c(t)$, are converted to voltage using two matched resistors R=10kΩ.

To implement the $\sqrt{2}$ ratio between the two levels of the output voltage (see (7-22)) the currents following through the switches have to be properly scaled with respect to I_{REF}=20μA which result in the following relations between the current sources in Fig. 7.15.

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_5 \text{ and } \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_8 \tag{7-28}$$

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_4 = 0.7\left(\frac{W}{L}\right)_1 \text{ and } \left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_9 = 0.7\left(\frac{W}{L}\right)_6. \tag{7-29}$$

To compensate the effect of the process variations on the absolute values of the delays, the delay networks are made configurable using two independent 3-bit words. Moreover, reducing the mismatch between delay cells by careful layout design can improve the accuracy of the delay line. However, a more precise implementation of the delay line can be obtained by using a delay locked loop (DLL) [99] at the cost of more complexity and increased power consumption.

The input comparator [100], required in Fig. 7.15, is depicted in Fig. 7.16. It is a synchronous high-speed comparator consists of a cascade of a preamplifier, latch, self-biased differential amplifier, and output driver. The quiescent current of the comparator is 90μA. The most critical parameter in this comparator is its input offset voltage. However, since we are reusing the output waveform to generate the 4-level signal, this offset won't affect the performance of our circuit. Note that based on Fig. 7.7, any offset in $f_0(t)$ will uniformly affect the other two shifted signals.

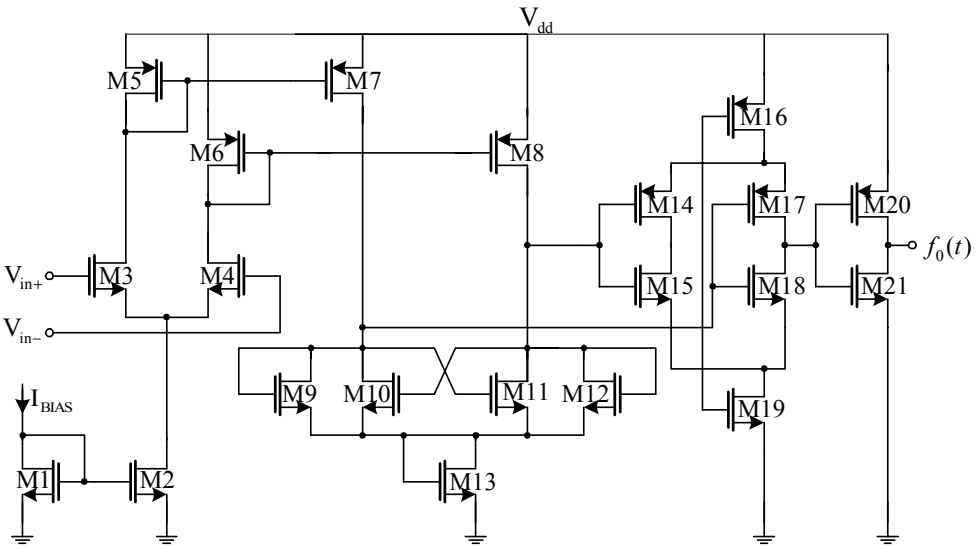


Fig. 7.16 Two stages Opamp used as the comparator [100].

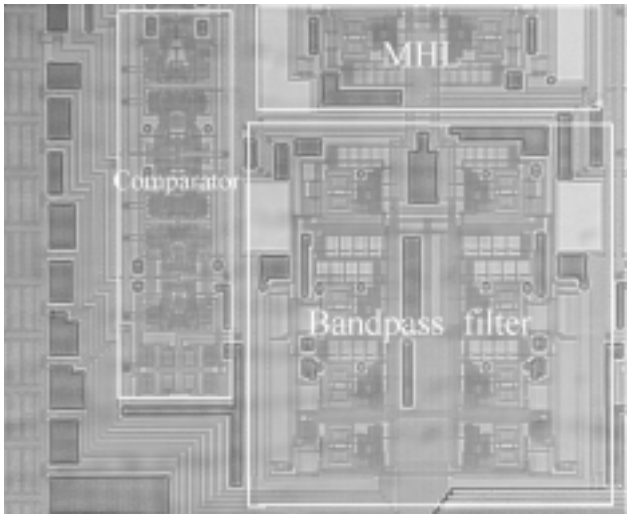


Fig. 7.17 Layout of the chip.

7.5. Experimental Results

The oscillator chip prototype was fabricated in TSMC 0.35μm CMOS technology through and thanks to MOSIS. The micrograph is shown in Fig. 7.17. The die size

occupies a silicon area of about 3.15mm^2. Fig. 7.18 shows the measurement setup for BP-based oscillator.

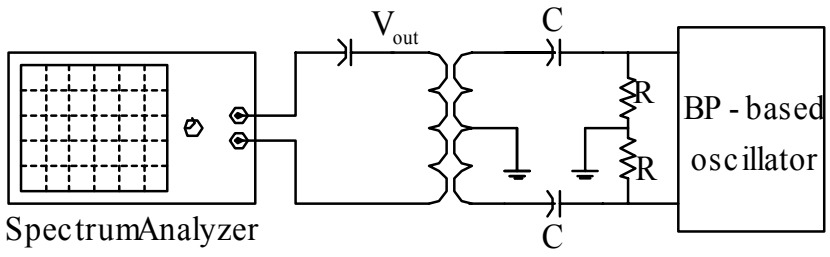


Fig. 7.18 Measurement setup for BP-based oscillator.

Fig. 7.19 shows the measured frequency response of the BPF which shows a center frequency and quality factor of around 10.6MHz and 20, respectively.

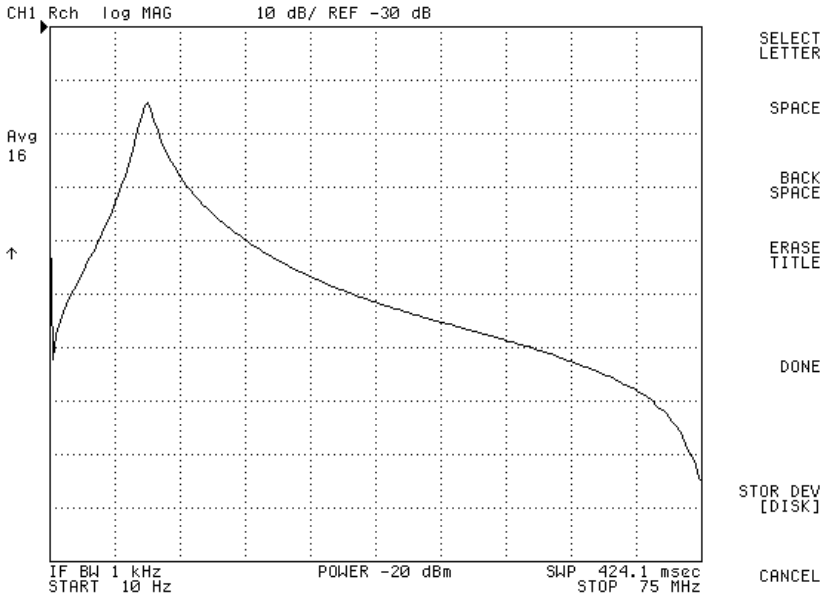


Fig. 7.19 Frequency response of the bandpass filter (vertical: -30dB/div. horizontal: 7.5MHz/div.).

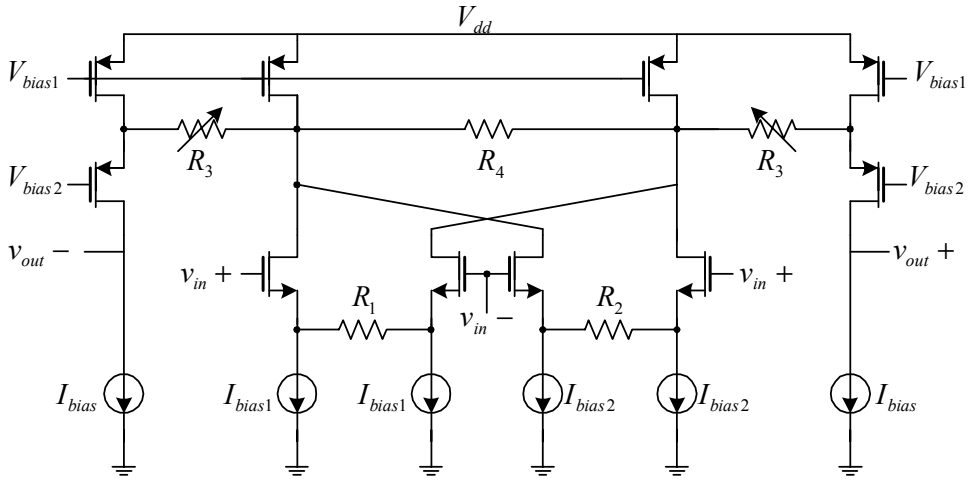


Fig. 7.20 Schematic of the output buffer [98] in Fig. 7.13.

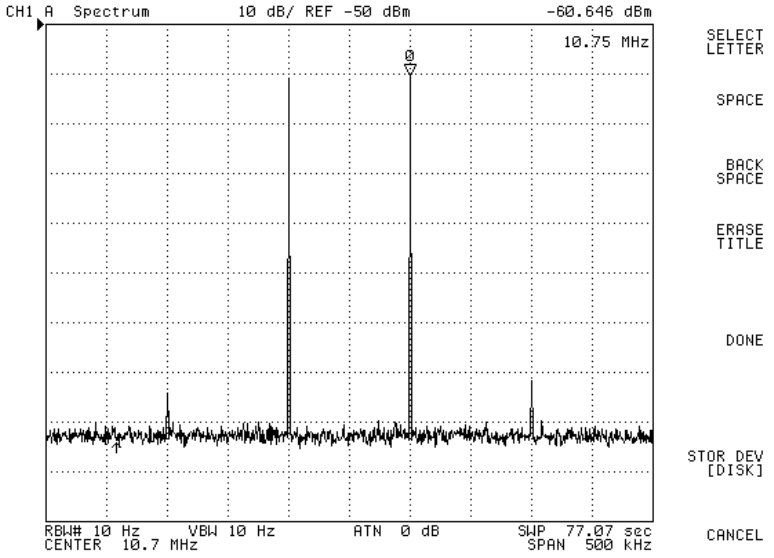


Fig. 7.21 IM3 measurement results for the buffer.

A linear buffer, shown in Fig. 7.20, is used at the output of the bandpass filter to convert the internal voltage mode signals to current [98]. The linearity of the buffer is adjustable through I_{bias2}. To characterize the contribution of the bandpass filter on the overall HD3 of the oscillator, an IM3 measurement has been carried on the cascade

combination of the bandpass filter and the buffer and the result is shown in Fig. 7.21. The two input tones are at frequencies of 10.65MHz and 10.75 MHz with equal amplitudes of 0.5Vpp. The best obtained IM3 of the buffer is -63dBm. Note that the more linear the bandpass filter, the more linear the output signal. However, in this research work the emphasis is on the nonlinearity associated with the nonlinear block.

By closing the loop of the filter and the nonlinear block the circuit starts oscillating and its output spectrum for both cases of the conventional comparator and the proposed MHL are shown in Fig. 7.22 and Fig. 7.23, respectively. Note that to have a fair comparison between the two scenarios the reference current I_{REF} in Fig. 7.15 has been adjusted so that the oscillation amplitudes of both cases are the same. Comparing these results shows a -24dB improvement in reduction of the third order harmonic distortion at the output of the filter in the case of the proposed MHL. Observe that the fifth order harmonic is reduced by several dB in Fig. 7.23 but its improvement is not as visible as the third order one due to the attenuation of the filter. However, the seventh order harmonics are comparable which is consistent with the analytical results obtained in (7-24). It is important to mention that the measured result in the case of the proposed MHL block is the best obtained result through adjusting the delay cells in Fig. 7.15 which tunes the delay time of t_1 in Fig. 7.6. This has been achieved by changing the digital word controlling the delay cells in Fig. 7.15 in order to maintain the requirement of $T_1=T/t_1=8$. If we assume that the first 7 harmonics are the main harmonics at the output, the overall THD of the measured frequency spectrums of Fig. 7.22 and Fig. 7.23 can be calculated as -38.63dB and -53.16dB, respectively.

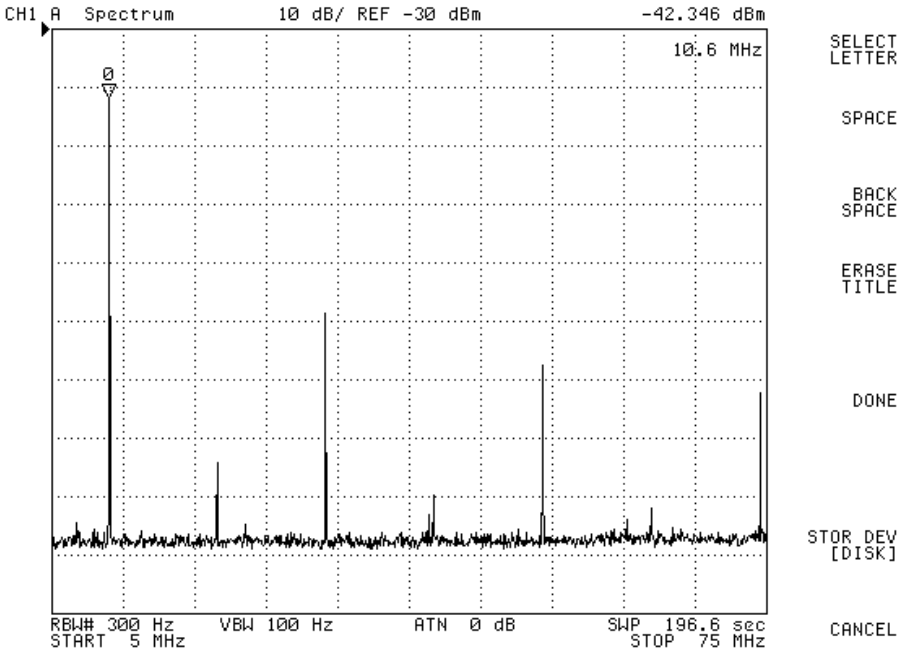


Fig. 7.22 Output spectrum of the oscillator with a conventional two-level comparator.

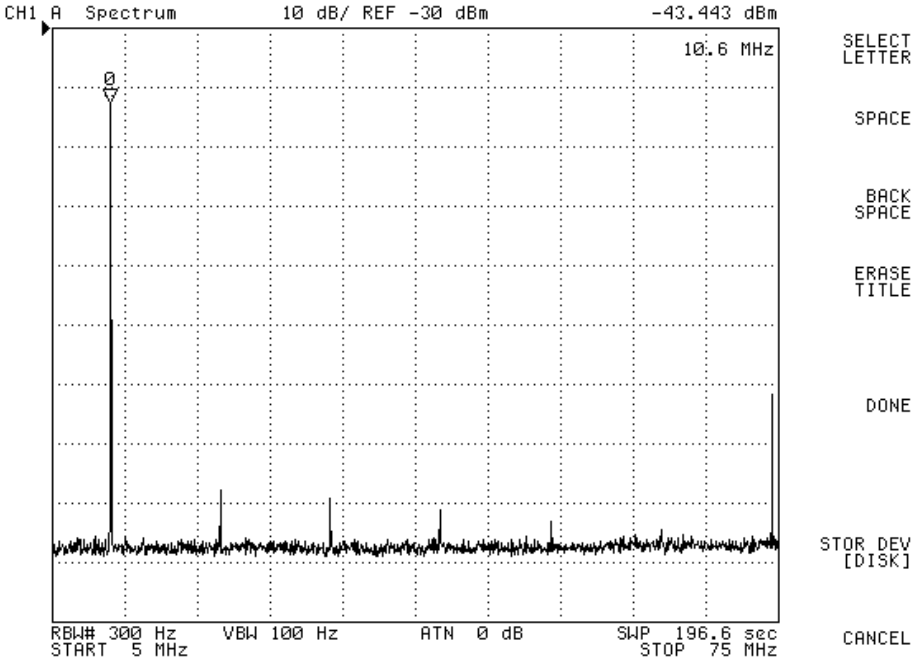


Fig. 7.23 Output spectrum of the oscillator with the proposed multilevel comparator.

These results show that more than 14 dB improvement in the THD can be achieved by using the proposed MHL block. Fig. 7.24 shows the theoretical predictions of THD versus different quality factors of the bandpass filter for both the comparator and the MHL block. This figure shows that, for the measured quality factor of 15, the experimental results are in good agreement with the theory.

Fig. 7.25 shows the effect of the delay cells on the THD of the proposed architecture in both simulation and measurement cases. As it can be seen from this figure there is only one optimum delay for which the measured THD is minimized and this value is around 1/8 of the fundamental period *T*. Deviation from this optimal value for delay results in a degraded THD as it has been verified by the measurement results.

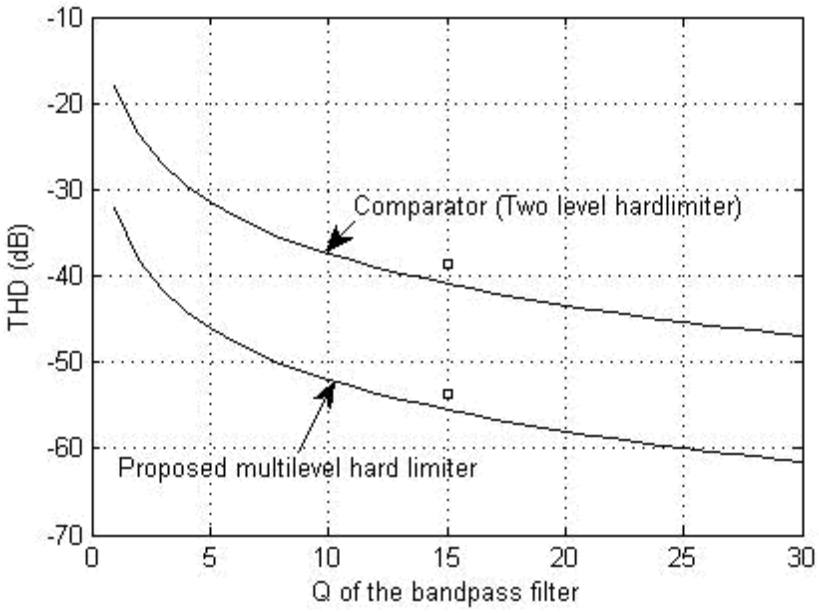


Fig. 7.24 THD of the oscillator as a function of the quality factor (solid lines: analytical, circles: experimental).

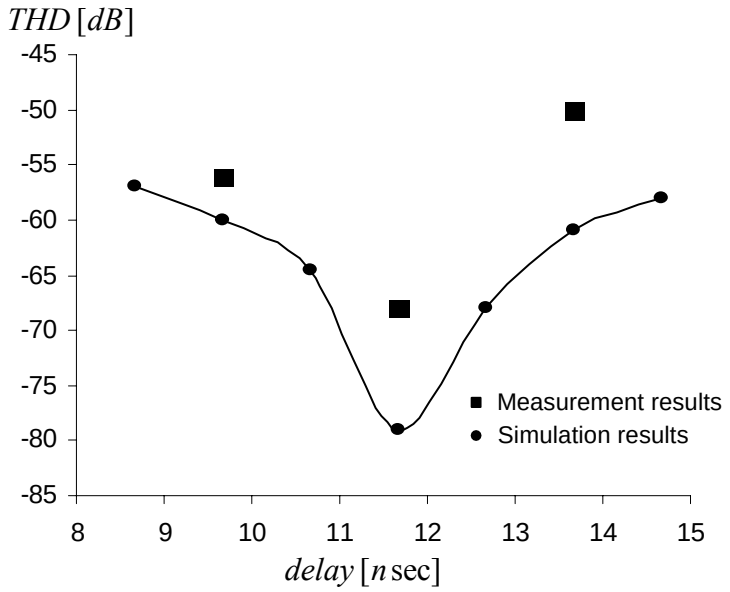


Fig. 7.25 THD as a function of the delay time (see Fig. 7.15).

CHAPTER VIII

ULTRA-WIDE BAND LOW PASS FILTER AND SYNTHESIZER

8.1. Introduction

Requirements for analog baseband signal processing in cellular communications are highly dependent on the receiver architecture. Recent demands for multistandard transceivers has been leading to frequent use of direct conversion architectures, notably because of their high integration potential and their relative system design easiness. The point of this research work is to provide a linear phase low pass filter to be used in a zero-IF UWB receiver between the down-conversion mixer and the analog-to-digital converter.

There are mainly two types of filters: digital filters and analog filters. While the data samples are discrete for digital filters, analog filters process continuous signals. Analog filters can be divided into passive (using only passive components) and active filters (using Opamp's and OTA's). Active filters can also be classified as Active-RC, Switched-Capacitor, Gm-C and LC filters. Passive filters don't employ amplifiers and usually are off-chip filters (to have very high selectivity) and are not suitable for integration. Active RC and Switched-Capacitor filters need very large unity gain frequency and very wide bandwidth. Since a Gm cell in a Gm-C integrator operates in open loop configuration, a Gm-C filter implementation can reach a very high speed up to the unity-gain frequency of the Gm cell. Consuming a lot of power by the Gm cells and

being sensitive to the parasitic effects make Gm-C implementation unsuitable for very high frequency (GHz) range.

8.1.1. *Linear Phase Filter Approximation*

The primary purpose of this kind of filters is to limit the signal and noise bandwidth. In general, there are no stringent magnitude response requirements in the passband or stopband, but it must have a linear phase or constant group delay for all signal frequencies to maintain the data integrity. Non-uniform group delay causes phase distortion and leads to detection problems. In practice, a small group delay deviation or a ripple of about 5% is permitted and a filter with an order of 4-7 maybe used [101]-[102].

8.1.2. *Bessel-Thomson and Equiripple Linear Phase Filter Approximations*

Bessel-Thomson approximation (maximally flat delay) and equiripple delay approximation are the two main filter approximations used for the design of filters with approximately constant group delay [103]. For a fourth-order linear phase filter, the normalized frequencies ω_i and Q_i for both Bessel-Thomson and 0.05^o Equiripple linear phase filters are shown in Table 8-1 and Table 8-2. Note that $\omega^2_0 = \omega_1\omega_2$.

Table 8-1 4^{th}-order Bessel-Thomson linear phase filter parameters

Filter Section	ω_i (rad/sec)	Q_i
Biquad 1	1.419	0.522
Biquad 2	1.591	0.806

Table 8-2 4th-order 0.05˚ equiripple linear phase filter parameters

Filter Section	ω_i (rad/sec)	Q_i
Biquad 1	1.007	0.573
Biquad 2	1.599	1.148

From Tables 8-1 and 8-2 we can see that for the Bessel-Thomson filter, the biquad section's Q_i's are smaller, and the ω_i's are more closely clustered. However, the group delay for the 0.05˚ equiripple filter is flat up to $1.5f_{cut\text{-}off}$ vs. $1.0f_{cut\text{-}off}$ for the Bessel-Thomson filter. Also, equiripple filter has a better selectivity than the Bessel-Thomson filter with the same order [102].

8.2. UWB Low Pass Filter Specifications

Besides adequate -3dB bandwidth, the main issue associated with the UWB LPF is maintaining the linear phase characteristic over the entire pass band so that the information arrived at the ADC experience a constant delay. The second issue associates with the attenuation of the next channel. These two issues can limit the flexibility of the order and type of the filter.

Based on the first estimation of the total group delay variation of the whole system which is 1nsec, a total group delay of 0.5nsec has been allocated to the LPF. Also, from system level specification an attenuation of at least 20dB in the transient region is enough to meet the UWB specs. However, we decided to shoot for 25 dB attenuation in our calculations. Fig. 8.1 visualizes the above explanations. Having a tight restriction on

the variation of the group delay suggests the use of the linear phase approximation to implement the filter.

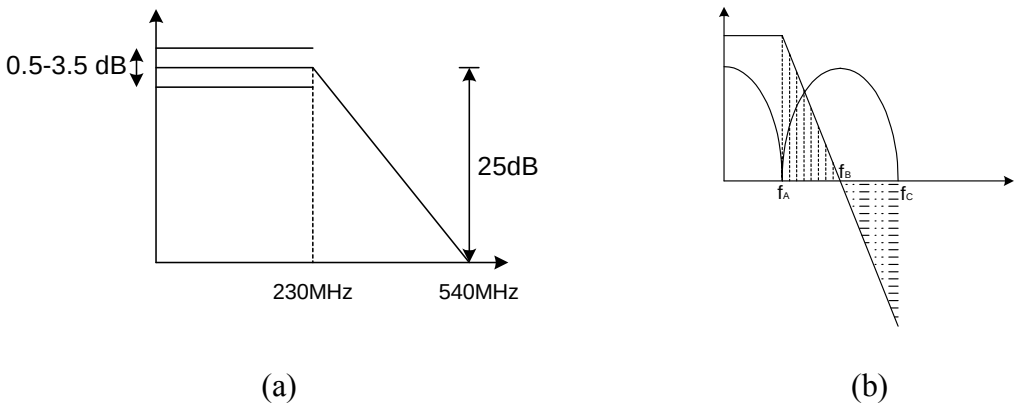


Fig. 8.1 Characteristics of the UWB LPF.

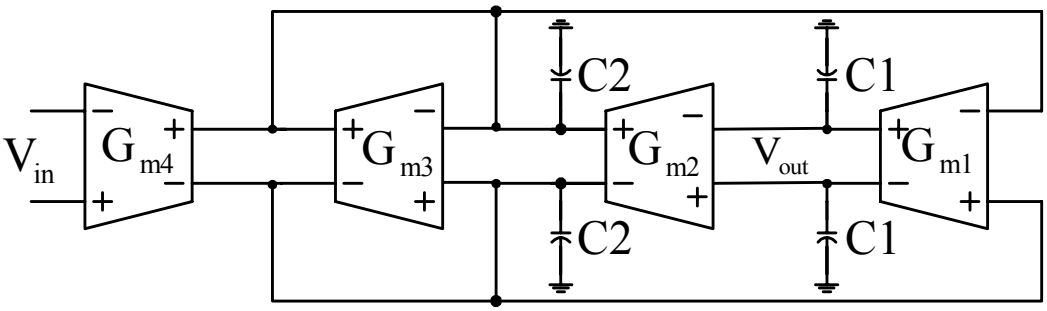


Fig. 8.2 Block diagram of a biquad Gm-C LPF.

8.2.1 *Design equations for Linear Phase Approximation*

Fig. 8.2 shows the block diagram of a second-order (biquad) Gm-C filter. The transfer function of this filter, neglecting the output transconductances of the OTAs, can be expressed as

$$H_{LP}(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{8-1}$$

where, $\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$ and $Q = \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}}$.

Note that the exact value of each g_{mi} associated with the desired Q_i of the biquad can be obtained as

$$g_{mi} = \omega_0 C_i \tag{8-2}$$

$$Q_i = \frac{g_{mi}}{g_{m-diode-i}} \tag{8-3}$$

Using Table 8-2, (8-2) and (8-3), the required parameters for a second-order LPF with ω_0=256MHz have been found and the results are shown in Table 8-3

Table 8-3 Design parameters

	$g_{m1}=g_{m2}$	$g_{m3}= g_{m4}$	C_1	C_2
BQ#1	2.798m	4.88m	0.58p	1.18p

8.3. Operational Transconductance Amplifiers (OTAs)

OTAs can be generally classified as: single-ended, fully-differential (FD), and Pseudo-differential (PD) OTAs. Usually fully differential OTAs are preferred because they provide better dynamic range over their singlae-ended counter parts, this is mainly due to their larger signal swing, better distortion performance and better common-mode noise and supply noise rejection. The main drawback of using fully differential OTAs is

that a Common-Mode Feedback (CMFB) circuit must be added. The design of a good CMFB is nontrivial. The speed of the common mode path should be comparable to that of the differential path; otherwise the common-mode noise (e.g. power supply noise) may be significantly amplified such that the output signal becomes distorted. Also, the CMFB circuit is often a source of noise injection and increase the load capacitance that needs to be driven.

8.3.1. *Proposed Transconductance Circuit*

Like every design targeted at portable electronics, our design has to be concerned with power efficiency, but stringent linearity and noise performances are required as well, notably because of the presence of strong blockers (possibly at a much higher level than the handled signal) at the receiver input.

The linearity/distortion requirements for such a cell are of course highly dependent on the standard and the system architecture. Noise specifications require a low input-referred noise power spectral density. The induced needed dynamic range is then achievable with a variable gain stage at the filter input. Consequently, this gain stage shifts the filter linearity specifications accordingly. This quite severe requirement is only achievable with a very linear transconductor. The need for a widely tunable, very linear transconductor led us to the use of the MOS transistor in its triode region since this allows a direct control on the MOS's transconductance value through its V_{DS}. Furthermore, a source degenerated source follower can be used to further linearized the transconductance. Fig. 8.3 shows the proposed Gm cell.

The operation of this Gm cell can be intuitively explained by noting that the BJT transistors (Q_1-Q_2) are working in their active region while the NMOS transistors (M_1-

M_2) are working in their triode region. Since the base-emitter voltage of the BJT's are quite constant, the assumption of having a fixed DC voltage at node A and B is valid. Note that $V_A=V_B=V_{DC}-V_{be}$. This means that the gate voltage (V_{DC}) of M1-M2 is greater that their drain (V_A and V_B) voltages which guarantees that M1 and M2 are in triode region. Due to different sign of input signals to each stage, the output current of M1 (I_1) is subtracted from the current (I_2) generated by the source degenerated stage. Thus, the output current I_{out} shows a better linearity at the cost of lower Gm value.

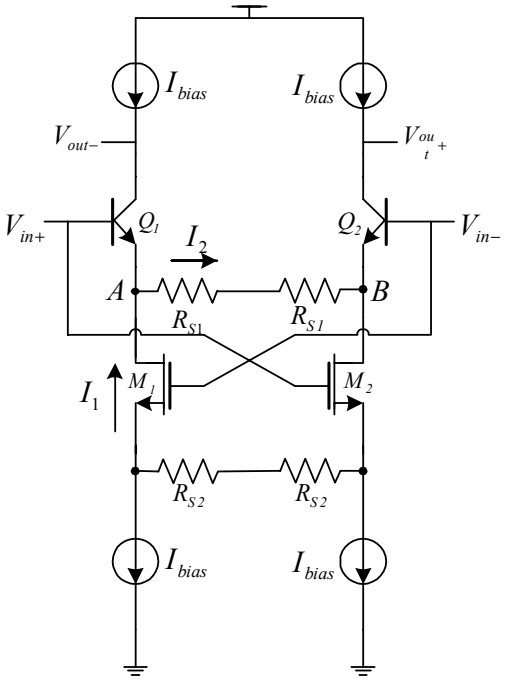


Fig. 8.3 Proposed BiCMOS Gm cell.

8.3.2. *Principle of Operation*

Considering the first order model describing the linear region of MOS transistor, the resistance of M_1-M_2 as a function of the input voltage can be written as:

For M2 :

$$R(v_{in}) = \frac{1}{\beta(v_{in} + V_{DC} - V_{th})} = \frac{1}{\beta(V_{DC} - V_{th})(1 + \frac{v_{in}}{V_{DC} - V_{th}})}$$
$$\Rightarrow R(v_{in}) \approx \frac{1}{\beta(V_{DC} - V_{th})}\left(1 - \frac{v_{in}}{V_{DC} - V_{th}}\right) = R_{DC} - \frac{v_{in}}{R_{DC}(V_{DC} - V_{th})} = R_{DC} - Kv_{in} \quad (8\text{-}1)$$

Similarly the on-resistance of M1 can be found as

$$R(-v_{in}) \approx R_{DC} - Kv_{in} \quad (8\text{-}2)$$

Fig. 8.4 shows the simulated on-resistance of M_1 and M_2 for W/L=5µ/1µ. Observe that for small perturbations of input signal around 0V, the small signal resistances of M_1 and M_2 have different signs and can be considered linear, i.e., the currents generated by M_1 and M_2 in Fig. 8.3 have opposite directions.

As (8-1) and (8-2) show by increasing the input voltage (v_{in}) the resistance of M_1 increases while the resistance of M_2 decreases. This property of M_1 and M_2 combined with the effect of the source degeneration resistance R_{S2}, as the following analysis shows; generate a negative linear resistor connected to the emitters of Q_1 and Q_2 which is subtracted form the current flowing to R_{S1} making the output current more linear.

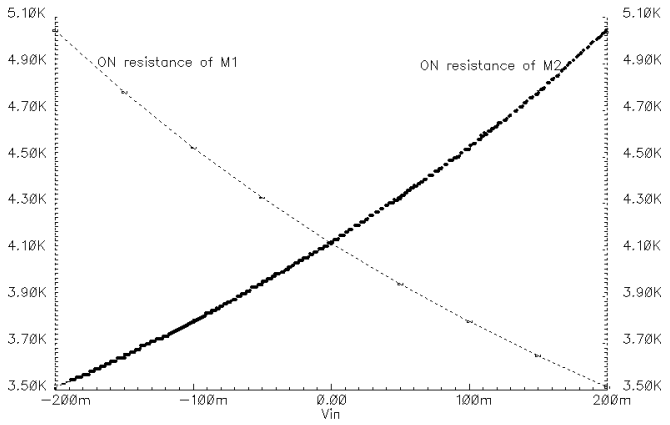


Fig. 8.4 Simulation results for an NMOS with W/L=5µ/1µ.

To derive the small signal transconductance of the proposed Gm cell, consider the half-circuit small signal model of the proposed circuit in Fig. 8.5. In this figure, $R(-v_{in})$ corresponds to the on-resistance of M_1.

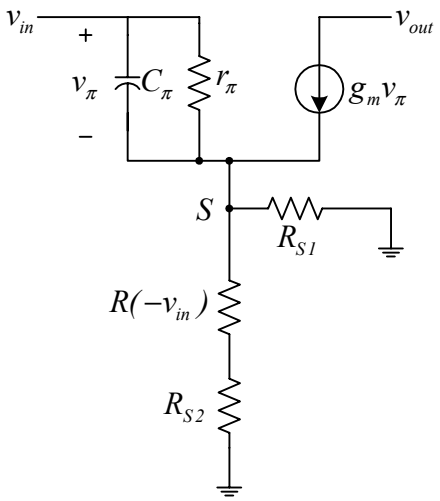


Fig. 8.5 Half circuit small signal model of Fig. 8.3.

$$R_{eff} = R_{S1} \| (R(-v_{in}) + R_{S2})$$

$$i_{out} \approx \frac{1}{R_{eff}} = \frac{(R_{S1}+R_{S2})(1+\frac{R(-v_{in})}{R_{S1}+R_{S2}})}{R_{S1}R_{S2}(1+\frac{R(-v_{in})}{R_{S2}})} \approx \frac{1}{R_{S1}\|R_{S2}}\left(1+\frac{R(-v_{in})}{R_{S1}+R_{S2}}\right)\left(1-\frac{R(-v_{in})}{R_{S2}}\right)$$

$$i_{out} \approx \frac{1}{R_{S1}\|R_{S2}}\left(1+\frac{R(-v_{in})}{R_{S1}+R_{S2}}-\frac{R(-v_{in})}{R_{S2}}\right) = \frac{1}{R_{S1}\|R_{S2}}\left(1+(\frac{-R_{S1}}{R_{S2}(R_{S1}+R_{S2})})R(-v_{in})\right)$$

$$i_{out} \approx \frac{v_{in}}{R_{S1}\|R_{S2}}\left(1-\frac{R_{S1}\|R_{S2}}{R_{S2}^2}R(-v_{in})\right) = \frac{v_{in}}{R_{S1}\|R_{S2}} - \frac{R(-v_{in})}{R_{S2}^2}v_{in}$$

$$i_{out} \approx \frac{v_{in}}{R_{S1}\|R_{S2}} - \frac{R_{DC}+Kv_{in}}{R_{S2}^2}v_{in} = \frac{v_{in}}{R_{S1}\|R_{S2}} - \frac{R_{DC}}{R_{S2}^2}v_{in} - \frac{K}{R_{S2}^2}v_{in}^2$$

$$\Rightarrow i_{out} \approx \left(G_{s1}+G_{s2}-\frac{G_{s2}^2}{G_{DC}}\right)v_{in} = G_{m,eff}v_{in} \tag{8-3}$$

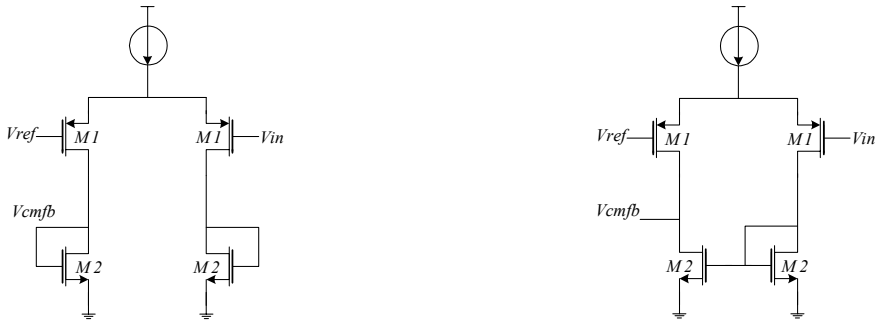
where, $G_{si}=1/R_{si}$ for i=1,2 and $G_{DC}=1/R_{DC}$.

As (8-3) shows, besides linearizing the output current, the total $G_{m,eff}$ of the proposed cell can be tuned independently using R_{S1} and/or R_{S2}.

8.3.3. *Common Mode Feedback (CMFB) Circuit*

Taking advantage of the filter architecture in Gm-C implementation along with the source-degenerated Gm cells provide a simple solution for CMFB circuit which is not necessarily fast enough. This is due to the nondominant poles close to the GBW of the CMFB circuit. To partially overcome this problem one may provide a faster path for common mode (CM) signal [104] or a more simple circuit for comparison purpose [105]. The procedure of designing the CMFB circuit follows these steps:

1- Fig. 8.6(a) shows a very simple amplifier, usually used in CMFB circuits. The gain of this amplifier is mainly the gain of the CMFB loop. Depend on the size of M_2's, the frequency response can be good enough. But since V_{cmfb} is going to be connected to "at least" two more transistor with the same size of M_2, the total capacitance at V_{cmfb} becomes relatively high, lowering the GBW of the CMFB. This problem can be alleviated by changing the architecture from differential to single ended (Fig. 8.6(b)). In this case besides the increase in gain, the dominant pole of the loop is also increased due to reduced output capacitance at node V_{cmfb}.



(a) (b)

Fig. 8.6 CMFB amplifier (a) low gain (b) high gain.

2- The total load capacitance can be split in two parts so that one of them is grounded (C_{S2}) and the other one (C_{S1}) can serve as the high speed CM path by connecting it to a proper node (See Fig. 8.7). By grounding one of the splitted capacitors, we are ensuring that there is a path which allows the output node to respond to sudden CM variations. Connection of C_{S1} is important since the CM loop created by C_{S1} should be negative for stability purposes. The best possible point is V_{ext} of the next Gm. Besides having a negative loop, this connection can be explained in this way that at high frequencies the splitted capacitors C_{s1}'s act as common mode detector and node V_P indeed contains the common mode information. This means that node V_P at high frequencies is doing the same job as node V_{ext} does at lower frequencies, expediting the process of extraction of the CM signal.

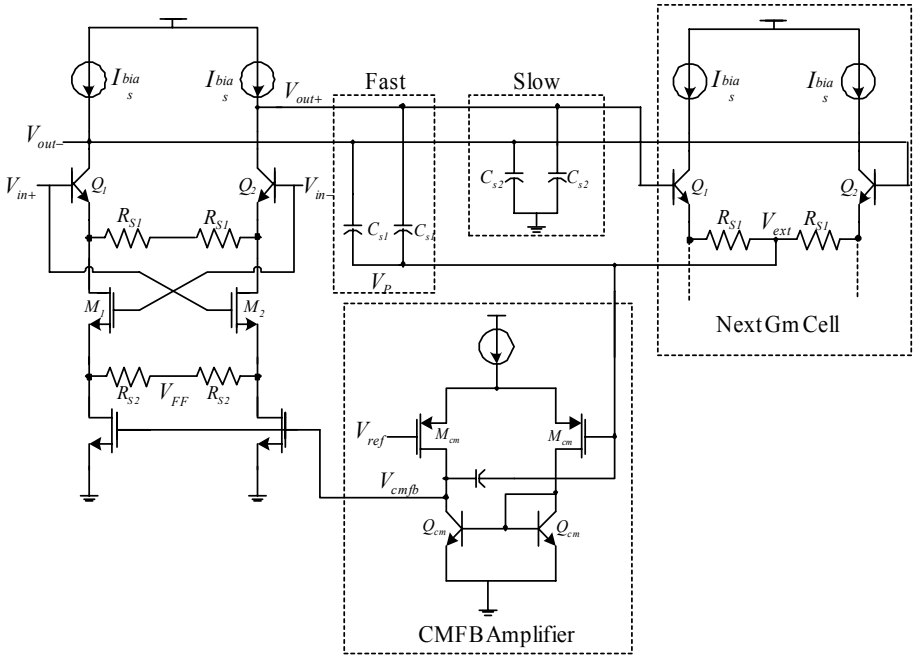


Fig. 8.7 Complete schematic of the OTA with its CMFB circuit.

3- Since the CMFB amplifier has a positive gain (from V_{ext} to V_{cmfb}), its amplification process at high frequencies can be accelerated by providing a direct path from V_{ext} to V_{cmfb}. This feedforward path is implemented using C_{FF}. The effect of C_{FF} can be viewed from the point of Miller effect. At node V_{cmfb} we have a negative capacitance which reduces the total capacitive load at node V_{cmfb}, pushing the major non-dominant pole further away from unity gain frequency.

8.3.4. *Simulation Results*

Fig. 8.7 has been designed and implemented in IBM6hp 0.25µ process. Fig. 8.8 compares the HD3 performance o fthe proposed Gm cell against the conventional source degenerated one. As it can be seen from these plots, for the same value of Gm, the proposed Gm cell can improve the HD3 of the output current by at least 7dB.

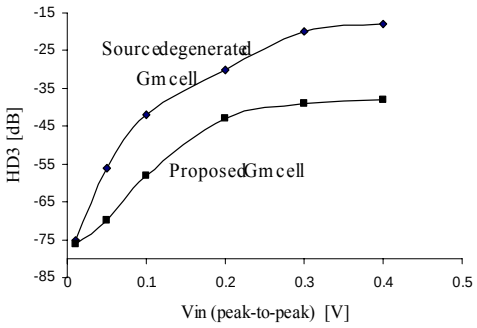


Fig. 8.8 HD3 vs. input amplitude at f_{in}=200MHz.

The stability of the enhanced CMFB loop has been verified through its small signal simulation. As Fig. 8.9 shows, the CMFB loop has a 3dB cut-off frequency of 350MHz with a phase margin of 54˚. The transient behavior of the CMFB loop in response to a current impulse with different amplitudes is shown in Fig. 8.10.

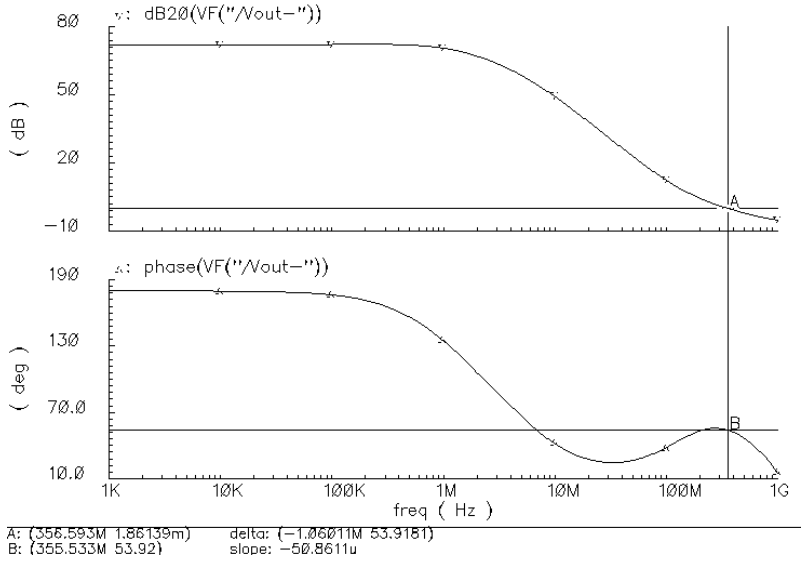


Fig. 8.9 Amplitude and phase response of the CMFB loop.

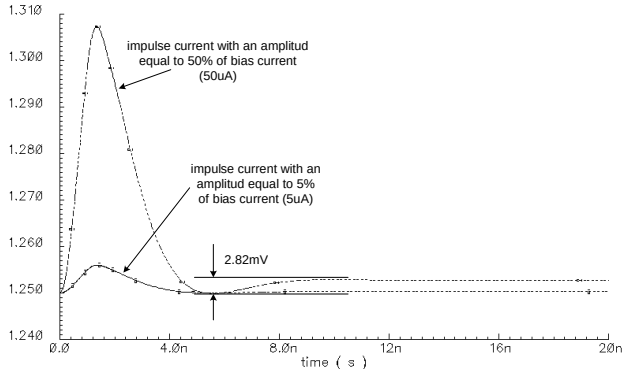


Fig. 8.10. Transient responses to a common mode current pulse at the output

Fig. 8.11 shows the simulation results of a 3th order LPF. The third pole is implemented at the input using a passive pole to increase the magnitude roll off.

The in-band and out-band linearity of the 3rd order LPF are measured by applying two tones at the cut-off frequency and the center frequency of the adjacent channel, respectively. Fig. 8.12 shows the simulation results. For two tones of equal amplitudes of -28dBm, the input and output IP3 are 19dBm and 20.5dBm, respectively.

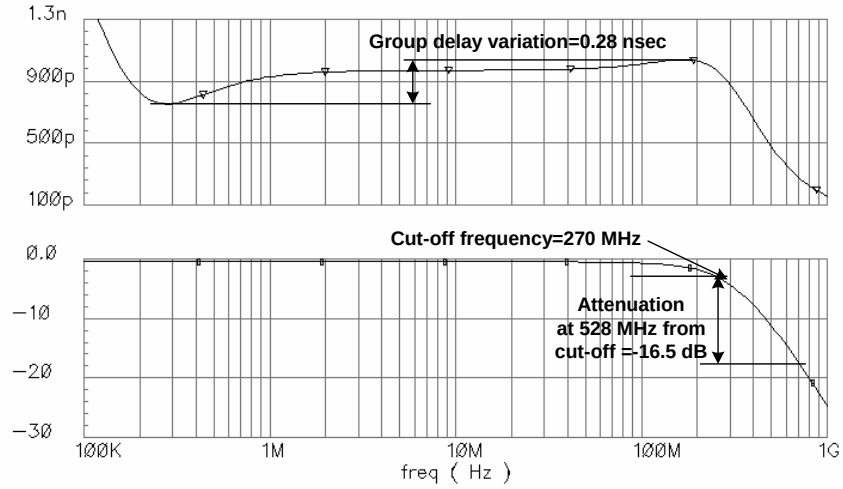


Fig. 8.11 Simulation results of the 3rd order linear phase LPF; Top plot: group delay, Bottom plot: magnitude response.

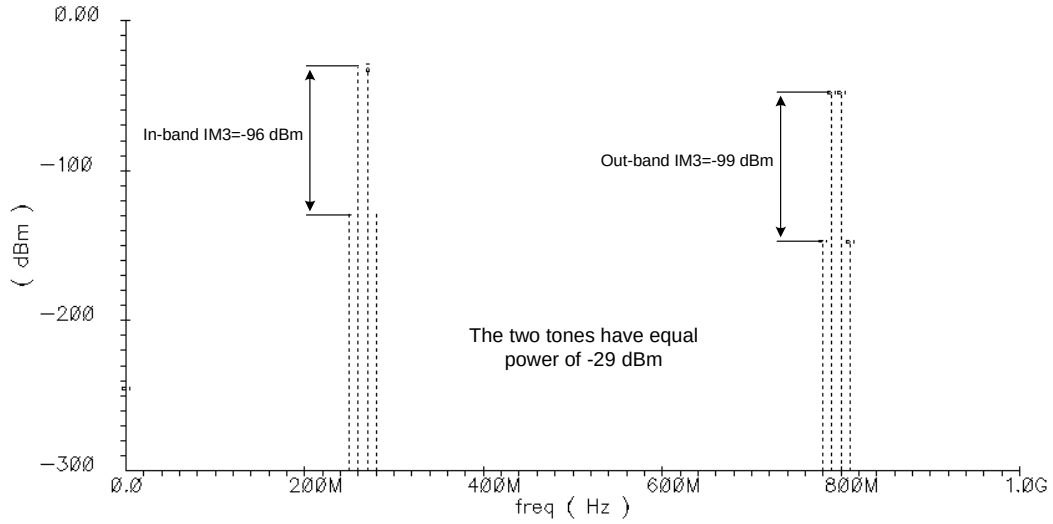


Fig. 8.12 In-band and out-band linearity.

8.3.5. *Experimental Results*

The above filter has been implemented in the SiGe IBM6hp 0.25µm process. Fig. 8.13 shows the chip micrograph of the LPF. It occupies an area of 200µm×180µm and consumes about 7mA current from a 2.5V power supply. Fig. 8.14 shows the frequency response of the LPF. Since the inputs to the LPF weren't accessible, the magnitude response of the LPF was obtained by sweeping the frequency at the input of the receiver. Fig. 8.15 shows the delay of the LPF between its input and output. The variation in the delay is the same as group delay which in this case is around 0.315nsec.

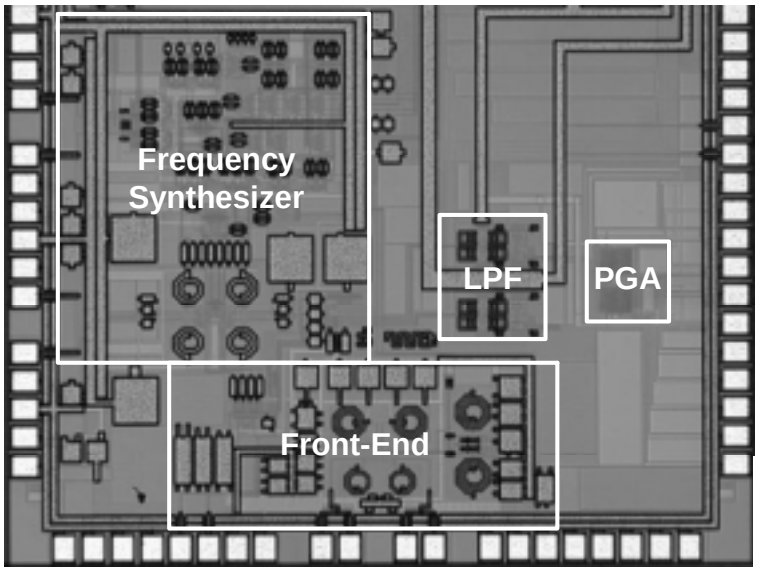


Fig. 8.13 Microphotograph of the UWB receiver.

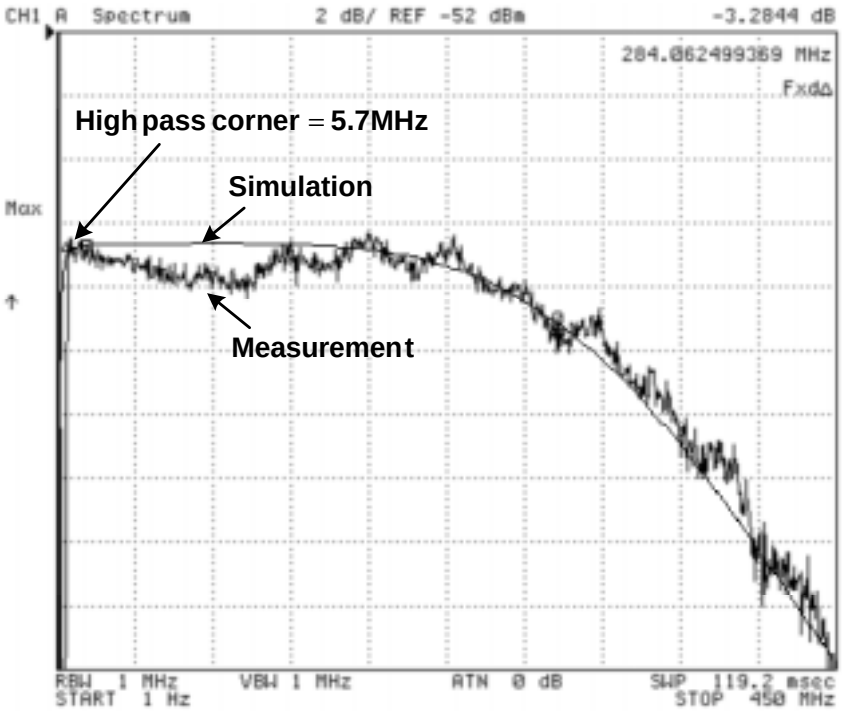


Fig. 8.14 Magnitude response of the UWB LPF.

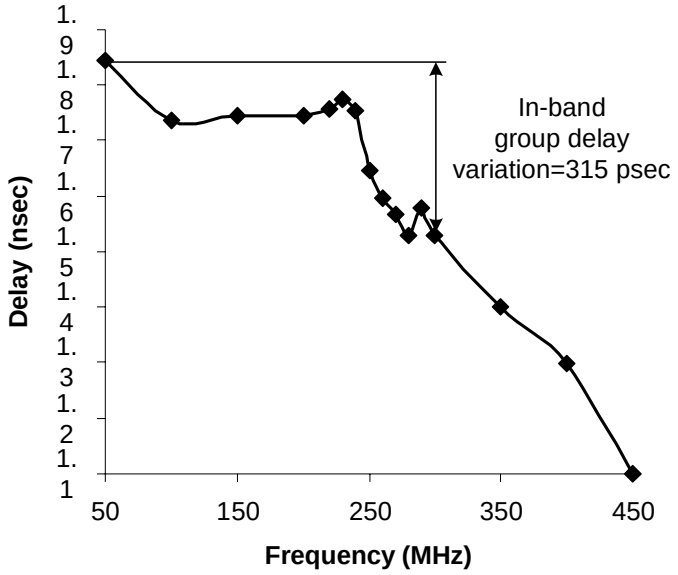


Fig. 8.15 Delay variations form input to output of the LPF.

8.4. UWB Frequency Synthesizer Architecture

Ultra-Wide Band (UWB) systems have recently received a great deal of interest due to their potential for high-speed wireless communication [106]–[108]. As part of IEEE P802.15, multiband orthogonal frequency division multiplexing (MB-OFDM) with fast frequency hopping is proposed as a means of high bit-rate wireless communication in the UWB spectrum. In mode-2 devices, the spectrum is divided into 528-MHz bands spanning 3.1–8.2 GHz, as shown in Fig. 8.16. The receiver front-end of such a system should have high linearity and a wideband local oscillator (LO) capable of frequency hopping in less than 9 ns. These features must be obtained at moderate power consumption and, to minimize cost, on a single chip.

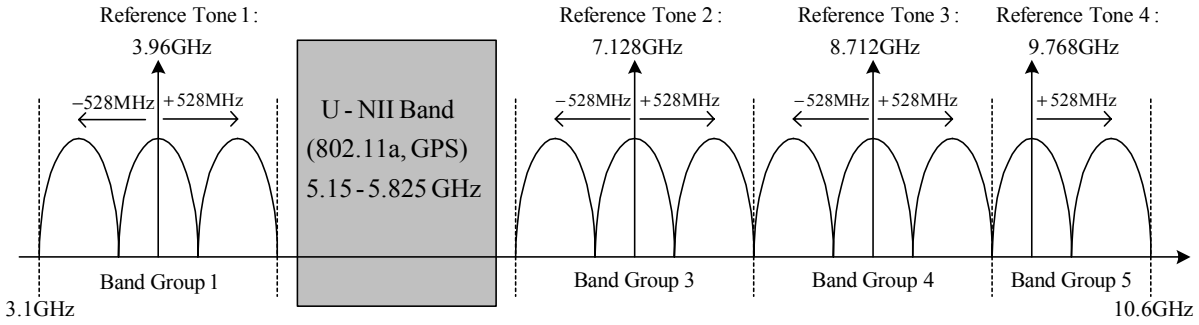


Fig. 8.16 UWB frequency planning.

According to the regulations from the Federal Communications Commission (FCC), Washington, DC, UWB devices for communication applications can operate in the 3.1–10.6-GHz frequency band while employing at least 500 MHz of bandwidth (measured at 10-dB points) with a power spectral density (PSD) of less than 41.25 dBm/MHz [107]. In the multiband (MB) orthogonal frequency-division multiplexing (OFDM) proposal [108] the 7500-MHz UWB spectrum is divided into 14 bands of 528 MHz each. The bands are grouped into five band groups, as shown in the upper section of Fig. 8.16. Only the first band group, corresponding to the lower part of the spectrum (3.1–4.8 GHz), is considered as mandatory by the current standard proposal. The remaining band groups have been defined and left as optional to enable a structured and progressive expansion of the system capabilities. Current efforts from semiconductor companies for the implementation of UWB devices focus on the first band group to achieve a faster time-to-market and affordable power consumption with current CMOS [109] and BiCMOS [110] technologies. The realization of UWB radios for operation in the entire 3.1–10.6-GHz range is an open research area, which leads to various design challenges at both the system and circuit levels.

As in other wireless systems, the frequency synthesizer has the crucial function of generating the local oscillator (LO) signal that drives the down-converter in the receiver path and the up-converter in the transmitter. There are at least two demanding requirements that make a frequency synthesizer for an MB-OFDM UWB radio significantly different from the widely explored synthesizers for narrow-band wireless systems, which are: 1) the range of frequencies to be generated spans several gigahertz and 2) the time to switch between different band frequencies within a band group should be less than 9.47 nS [108]. This requirement prevents the use of a standard phase-locked loop (PLL)-based synthesizer as a solution for this application [111].

A compact frequency-synthesizer architecture is proposed and is shown in Fig. 8.17. It can be seen that in this architecture all the reference tone generations involve a final up conversion by a 792-MHz tone. A significant reduction in power and area would be expected due to the small number of mixers with multiple frequency output. However, this architecture still needs a broad-band SSB up converter for the generation of all the reference tones (up conversion with 792 MHz).

Harmonics can be curtailed by low-pass filtering at different stages, but suppressing the unwanted sidebands demands additional filtering (bandpass or band notch) for the different IF generated in the synthesizer.

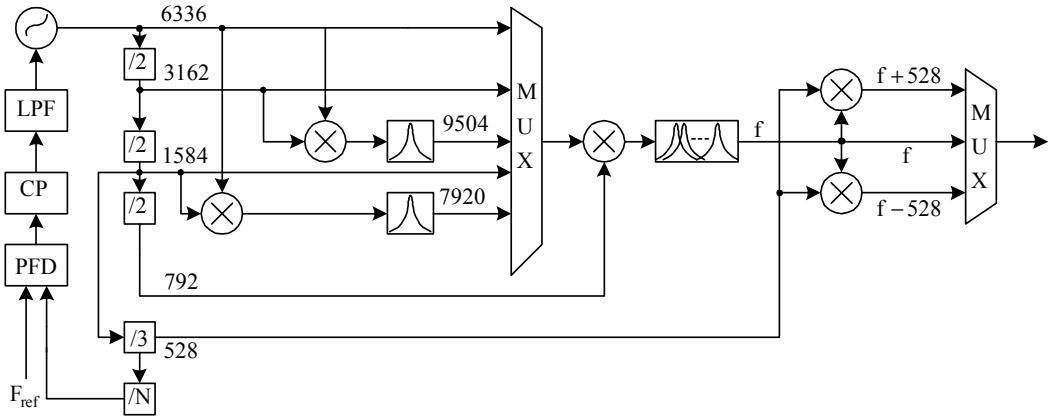


Fig. 8.17 Proposed UWB frequency synthesizer.

In the above architecture, this would imply a wide tuning-range bandpass (or notch) filter to cater to the wide range of IF generated (especially after the up conversion with 792 MHz) apart from the dedicated filtering wherever required (see Fig. 8.17). One possibility is to have dedicated SSB mixer blocks and filtering for generation of each reference tones, but that would be at the expense of higher power consumption. It must be mentioned here that the last two mixers used to generate the bands adjacent to the reference frequency (up/down conversion by 528 MHz) also have a multiple frequency input and output and would have to be broad-band. However, this structure with two mixers and one multiplexer at the end of the frequency synthesizer is common to all of the architectures presented in this work. Since filtering at the final stage would demand a broad-band tunable filter spanning several gigahertz, it is not practical and is, hence, not employed at the output of the last mixers in any of the architectures. Hence, the aim would be to have the reference frequency as spectrally pure as possible before the final up/down conversion. Therefore, an important consideration is to minimize the number of up/down-conversion operations in the generation of any reference frequency to reduce

the spurs within the UWB spectrum. The above discussion highlights some of the most important considerations for the design of a frequency synthesizer in an UWB system.

CHAPTER IX

CONCLUSIONS

In this dissertation, the design issues of high frequency continuous-time integrated filters have been examined. What mainly limit the performance of an analog filter are the non-idealities of the used building blocks and the circuit architecture. Several novel techniques and architectures have been proposed. On the circuit level, new building blocks have been introduced. A 4^{th} order LC filter with an enhanced scheme to couple the LC tanks is shown. The proposed coupling scheme does not degrade the quality factor of inductors in the tank.

A novel quality factor tuning for 2^{nd} order LC filters is proposed. The information of the magnitude response at the center and one of the cut-off frequencies is used to tune both the amplitude and the quality factor of the filter using two independent yet interacting loops. Furthermore, the synergic interaction between the loops makes the proposed scheme stable and insensitive to the mismatch between the input amplitudes.

An enhanced loss control scheme incorporating an integral feedback to automatically tune the oscillation amplitude of LC oscillators is proposed. The proposed loss control feedback (LCF) loop is practically unconditionally stable and its stability is examined i) by linearizing the system around the stable point using a perturbation method and ii) by numerically solving the nonlinear differential equation of the LCF loop describing the transient behavior of the step response of the loop.

A linearized fully balanced fully symmetric pseudo-differential operational transconductance amplifier (OTA) has been presented. Despite the previously reported

pseudo-differential architectures, the output current of the proposed OTA is a function of the differential input signals. It has been shown that the linearity of the proposed OTA can be improved by manipulating the second order harmonic which is inherently present at the output current of the pseudo-differential structure. The linearity behavior of the proposed OTA is measured in a unity gain negative feedback configuration which is the worst scenario in terms of large signal linearity.

In order to reduce the total harmonic distortion (THD) of a bandpass-based oscillator, instead of using a conventional hard limiter, a multilevel hard limiter (MHL) is proposed which inherently removes the third and the fifth order harmonics from the frequency spectrum of its output signal. The input-output characteristic of the proposed MHL contains slope values of only zero and infinity, making it easy to implement. The optimal height and width of each stair of the MHL characteristic is derived.

A linearized high frequency transconductance cell to build an UWB LPF is proposed. Due to the high bandwidth of this kind of filters, a fast common mode feedback loop is also proposed to reject the variations of common mode signals and preserve a high CMRR. Furthermore, an optimum and efficient UWB frequency synthesizer is proposed which is capable of generating all the carrier frequencies from 3.1GHz to 10.6GHz.

REFERENCES

[1] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Prentice Hall, 1998.

[2] B. Razavi, "Architectures and circuits for RF CMOS receivers," *in IEEE Proceeding of the Custom Integrated Circuits Conference,* pp. 393-400, 1998.

[3] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1399-141-, Dec. 1995.

[4] J. C. Rudell, J. J. Ou, T. B. Cho, G. Chein, F. Brianti, J. A. Weldson and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 2071-2088, Dec. 1997.

[5] J. R Long, "A low voltage 5.1-5.8-GHz image-reject downconverter RF IC," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1320-1328, Sept. 2000.

[6] L. Der, B. Razavi, "A 2GHz CMOS image-reject receiver with sign-sign LMS calibration", *IEEE Conference on Solid-State Circuits*, pp. 294-295, Feb. 2001.

[7] F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour, A. Kheirkhahi, M. Nariman, S. Bhatia and M. Conta, "A 27mW GPS radio in 0.35μm CMOS", *IEEE Conference on Solid-State Circuits*, pp. 398-476, Feb. 2002.

[8] J. Crols and M. S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1483-1492, Dec. 1995.

[9] H. Darabi, J. Chiu, S. Khorram, K. H. Joung, Z. Zhimin, M. Hung, B. Ibrahim, E. Geronaga, L. H. Trann, A. Rofougaran, "A dual-mode 802.11b/Bluetooth radio in 0.35μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 698-706, Mar. 2005.

[10] H. Chun-Huat, M. Gupta, L. Sang-Hoon, D. Kang, S. Bang-Sup,"A CMOS TV tuner/demodulator IC with digital image rejection", *IEEE Conference on Solid-State Circuits*, pp. 432-608, Feb. 2005.

[11] R. Feicker and O. Rojas, "Modeling and simulation of the superregenerative receiver", *IEEE Transaction on Consumer Electronics*, vol. 43, no. 2, pp. 92-102, May. 1997.

[12] F. X. Moncunill-Geniz, P. Pala-Schonwalder and O. Mas-Casals, " A generic approach to the theory of Superregenerative reception", *IEEE Trans. Circuits & System-I,* vol. 52, no. 1, pp. 54-70, Jan. 2005.

[13] N.J. Muller, *Bluetooth Demystified*, New York, Mc Graw Hill, 2001.

[14] Specifications of the IEEE 802.11 System, 1999. http://www.ieee.org (Accessed on March 4th 2004).

[15] FCC, "Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems", *ET-Docket 98-153,* http://www.fcc.gov/oet/dockets/ et98-153/ (Accessed on March 4th 2004).

[16] Triquint Semiconductor, Sawtek Products, [Online document], Available HTTP: http://www.triquint.com/prodserv/divisions/sawtek/handset/if_filters.cfm.

[17] S. Pipilous, Y. P. Tsividis, J. Fenk, and Y. Papananos, " A Si 1.8GHz RLC Filter with Tunable Center Frequency and Quality Factor" *, IEEE J. Solid-State Circuits*, vol. 31, no. 10, pp. 1517-1525, October 1996.

[18] C.C.W. Ruppel, L. Reindl, and R. Weigel, "SAW devices and their wireless communications applications," *IEEE Microwave Magazine*, vol. 3, no.2, pp. 65-71, June 2002.

[19] J.H.Visser, M.J. Vellekoop, A.Venema, E. van der Drift, P.J.M. Rek, A.J. Nederlof, and M.S. Nieuwenhuizen, "Surface acoustic wave filters in ZnO-SiO2-Si layered structures," in *Proc. of the Ultrasonics Symposium*, Montreal, Canada, 1989, vol. 1, pp. 195-200.

[20] N. J. Colmenares, "The FCC on personal wireless," *IEEE Spectrum,* vol. 31, no. 5, pp. 3946-3947, May 1994.

[21] A. A. Abidi, "Radio-frequency integrated circuits for portable communications," in *Proc. IEEE CICC,* 1994, pp. 8.1.1-8.1.8.

[22] W. B. Kuhn, N. K. Yanduru, A. S. Wyszynski, " Q-Enhanced LC bandpass filter for integrated wireless applications", *IEEE Trans. Microwave Theory & Techniques*, Vol. 46, No. 12, pp. 2577-2586, December 1998.

[23] F. Dügler, E. Sánchez-Sinencio, J. Silva-Martínez, " A 1.3-V 5mw fully integrated tunable bandpass filter at 2.1 GHz in 0.35 μm CMOS", *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 918-928, June 2003.

[24] D. Li, Y. P. Tsividis, "Design Techniques for Automatically Tuned Integrated Gigahertz-Range Active LC Filters" , *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 967-977, Aug. 2002.

[25] A. N. Mohieldin, E. Sánchez-Sinencio, J. Silva-Martínez, " A 2.7-V 1.8-GHz Fourth-Order Tunable LC Bandpass Filter Based on Emulation of Magnetically Coupled resonators", *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1172-1181, July 2003.

[26] R. Duncan, K.W. Martin, A.S. Sedra, " A Q-Enhanced Active-RLC Bandpass Filter", *IEEE Trans. Circuits & System-II,* vol. 44, no. 5, pp. 341-346, May 1997.

[27] W. Gao, W. M. Snelgrove, "A linear integrated LC bandpass filter with Q-

enhancement" *IEEE Trans. on Circuits and Systems*, vol. 45, no. 5, pp. 635-639, May. 1998.

[28] A. M. Niknejad and R. G. Meyer," Analysis, design and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470-1481, Oct. 1998.

[29] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Boston, MA: Kluwer, 1998.

[30] T. Soorapanth, S. S. Wong, "A 0 dB-IL, 2140±30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS" *IEEE J. Solid-State Circuits*, vol. 37, pp. 579-586, May. 2002.

[31] B. Georgescu, H. Pekau, J. Haslett, J. McRory, "Tunable coupled inductor Q-enhancement for parallel resonant LC tanks" *IEEE Trans. on Circuits and Systems*, vol. 50, no. 10, pp. 705-713, Oct. 2003.

[32] S. Bantas, Y. Koutsoyannopoulos, "CMOS active-LC bandpass filters with coupled-inductor Q-enhancement and center frequency tuning" *IEEE Trans. on Circuits and Systems*, vol. 51, no. 2, pp. 69-76, Feb. 2004.

[33] H. Xin, W. B. Kuhn, "A fully integrated Q-enhanced LC filter with 6 dB noise figure at 2.5 GHz in SOI" *IEEE Symp. Radio Frequency Integrated Circuits*, pp. 643-646, Jun. 2004.

[34] A. I. Zverev, *Handbook of Filter Synthesis*. New York: Wiley, 1967.

[35] T. Soorapanth, C. P. Yue, and D. K. Shaeffer et al., "Analysis and optimization of accumulation-mode varactor for RF IC's" *IEEE Symposium of VLSI Circuits Digest of Technical Papers*, pp. 32-33, Jun. 1998.

[36] A. Zanchi, ; Samori, C.; Levantino, S.; Lacaita, A.L, "A 2-V 2.5-GHz-104-dBc/Hz at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 611- 619, April 2001.

[37] A. Rodriguez-Vazquez, B. Linares-Barranco, J. L. Huertas and E. Sánchez-Sinencio, "On the design of voltage-controlled sinusoidal oscillators using OTAs," *IEEE Trans. Circuits Syst. I*, vol. 37, no. 2, pp. 198-211, Feb. 1990.

[38] B. Linares-Barranco, T. Serrano-Gotarredona, J. Ramos-Martos, J. Ceballos-Caceres, J.M. Mora, A. Linares-Barranco, "A Precise 90º Quadrature OTA-C Oscillator Tunable in the 50-130-MHz Range," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 4, pp. 649-663, Apr. 2004.

[39] D. Li and Y. P. Tsivids, "A Loss-Control Feedback Loop for VCO Indirect Tuning of RF Integrated Filters," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 3, pp. 169-175, Mar. 2000.

[40] E. Vannerson and K. C. Smith, "Fast Amplitude Stabilization of an RC Oscillator," *IEEE J. Solid-State Circuits*, vol. 9, no. 4, pp. 176-179, Aug. 1974.

[41] A. Zanchi, C. Samori, A. L. Lacatia, S. Levantino, "Impact of AAC Design on Phase Noise Performance of VCOs," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 6, pp. 537-547, Jun. 2001.

[42] A. M. Niknejad and R. G. Meyer," Analysis, design and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, Oct. 1998.

[43] J. Silva-Martinez, M. S. J. Steyaert and W. Sansen, "Design techniques for high-performance full-CMOS OTA-RC continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 27, no. 7, Jul. 1992.

[44] P.E. Allen and D. Holberg, *CMOS Analog Circuit Design,* New York, NY: Oxford University Press, 2002.

[45] J. R. Canning and G. A. Wilson, "Frequency discriminator circuit arrangement", U. K. patent, 1 142 093, Jan. 14, 1976.

[46] K. R. Rao, V. Sethuraman and P. K. Neelakanta, "A novel 'follow the master' filter", *Proc. IEEE*, vol. 65, no. 12, pp. 1725-1726, Dec. 1977.

[47] Y. Tsividis, "Self-tuned filters", *El. Letters*, vol. 17, no. 12, pp. 406-407, Jun. 1981.

[48] H. Khorammabadi and P. R. Gray, "High frequency CMOS continuous time filters", *IEEE J. of Solid State Circuits,* vol. 19, no. 12, pp. 939-948, Dec. 1984.

[49] V. Gopinathan, Y. Tsividis, K. Tan and R. K. Hester, "Design consideration for high frequency continuous time filters and implementation of anti-aliasing filter for digital video", *IEEE J. of Solid State Circuits,* vol. 25, no. 6, pp. 1368-1378, Dec. 1990.

[50] M. Banu and Y. Tsividis, "An elliptic continuous time CMOS filter with on-chip automatic tuning", *IEEE J. of Solid State Circuits,* vol. 20, pp. 1114-1121, Dec. 1985.

[51] K-S. Tan and P. R. Gray, "Fully integrated analog filters using bipolar-JFET technology", *IEEE J. of Solid State Circuits,* vol. 13, no. 6, pp. 814-821, Dec. 1978.

[52] R. Schaumann, M. S. Ghausi, K. R. Laker, *Design of Analog Filters*, Englewood Cliffs, NJ: Prentice Hall, Inc. 1990.

[53] D. Senderowicz, D. A. Hodges and P. R. Gray, "An NMOS integrated vector-locked loop", *IEEE Proc*. ISCAS, pp. 1164-1167, 1982.

[54] Y. Wang and A. A. Abidi, "CMOS active filter design at very high frequencies", *IEEE J. of Solid State Circuits,* vol. 25, no. 6, pp. 1562-1574, Dec. 1990.

[55] V. Aparin and P. Katzin, "Active GaAs MMIC band-pass filters with automatic frequency tuning and insertion loss control," *IEEE J. of Solid State Circuits,* vol. 30, no. 10, pp. 1068–1073, Oct. 1995.

[56] R. Duncan, K. W. Martin and A. S. Sedra, "A Q-enhanced active-RLC bandpass filter," *IEEE Trans. Circuits & Systems–II* vol. 44, no. 5, pp. 341–346, May 1997.

[57] Gloria Huertas Sánchez, *Oscillation-Based Test for Mixed Signal Circuits*, PhD Dissertation, University of Sevilla, Sevilla, Spain, 2004.

[58] M. H. Koroglu and P. E. Allen, "LC notch filter for image-reject applications using on-chip inductors," *IEE Electronics Letters*, vol. 37, no. 5, May 2001.

[59] R. Duncan, K.W. Martin, A.S. Sedra, " A *Q*-Enhanced active-RLC bandpass filter," *IEEE Trans. Circuit Syst. II,* vol. 44, no. 5, pp. 341-346, May 1997.

[60] S. Pipilos, Y. P. Tsividis, J. Fenk and Y. Papananos, "A Si 1.8 GHz RLC filter with tunable center frequency and quality factor," *IEEE J. of Solid-State Circuits*, vol. 31, no. 10, pp. 1517-1525 Oct. 1996.

[61] D. Li and Y. Tsividis, "Design techniques for automatically tuned integrated gigahertz-range active filters," *IEEE J. of Solid-State Circuits*, vol. 37, no. 8, pp. 967-977, Aug. 2002.

[62] C. Park and R. Schaumann, "Design of 4-MHz analog integrated CMOS transconductance-C bandpass filter," *IEEE J. of Solid-State Circuits*, vol. 23, no. 4, pp. 987-996, Aug. 1988.

[63] J. M. Khoury, "Design of a 15-MHz CMOS continuous-time filter with on-chip

tuning," *IEEE J. of Solid-State Circuits*, vol. 26, no. 12, pp. 1988-1997, Dec. 1991.

[64] J. Silva-Martinez, M. Steyaert, and W. Sansen, "A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. of Solid-State Circuits,* vol. 27, no. 12, pp. 1843–1853, Dec. 1992.

[65] R. Schaumann and M. Tan, "The problem of on-chip automatic tuning in continuous-time integrated filters," *IEEE Int. Symp. on Circuit and Syst.*, pp. 106-109, 1989.

[66] H. Khorramabadi and P.R.Gray, "High-frequency CMOS continuous time filters", *IEEE J. of Solid-State Circuits*, vol. 19, no. 6, pp. 963-967, Dec. 1984.

[67] K. A. Kozma, D. A. Johns and A. S. Sedra, "Automatic tuning of continuous-time integrated filter using an adaptive filter technique," *IEEE Trans. Circuit Syst. II*, vol. 38, no. 11, pp. 1241-1248, Nov. 1991.

[68] J. M. Stevenson and E. Sánchez-Sinencio, "An accurate quality factor tuning Scheme for IF and high-*Q* continuous-time filters," *IEEE J. of Solid-State Circuits*, vol. 33, no. 12, pp. 1970-1978, Dec. 1998.

[69] P. Kallam, E. Sánchez-Sinencio and A. I. Karsilayan, "An enhanced adaptive *Q*-tuning scheme for a 100-MHz fully symmetric OTA-based bandpass filter," *IEEE J. of Solid-State Circuits*, vol. 38, no. 4, pp. 585-593, Apr. 2003

[70] X. He and W. B. Kuhn, "A 2.5-GHz low-power, high dynamic range, self-tuned *Q*-enhanced LC filter in SOI," *IEEE J. of Solid-State Circuits*, vol. 40, no. 8, pp. 1618-1628, Aug. 2005.

[71] L. Hengesheng and A. I. Karsilayan, "An accurate automatic tuning scheme for high-*Q* continuous-time bandpass filters based on amplitude comparison," *IEEE Trans.*

Circuit Syst, II, vol. 50, no. 8, pp. 415-423, Aug. 2003.

[72] T. Sumesaglam and A. I. Karsilayan, "A digital automatic tuning technique for high-order continuous-time filters," *IEEE Trans. Circuit Syst. I*, vol. 51, no. 10, pp. 1975-1984, Oct. 2004.

[73] C. DeVries and R. Mason, "A 0.18μm CMOS, high *Q*-enhanced bandpass filter with direct digital tuning" ", *IEEE Conference on Custom Integrated Circuits*, pp. 279-282, May 2002.

[74] H. K. Khalil, *Nonlinear Systems*, Upper Saddle River, NJ, Prentice Hall Inc., 2002.

[75] S.-G. Lee and J.-K Choi, "Current-reuse bleeding mixer," *IEE Electronics Letters*, vol. 36, pp. 696-697, Apr. 2000.

[76] J. Y. Lee, C. C. Tu and W. H. Chen, "A 3 V linear input range tunable CMOS transconductor and its application to a 3.3 V 1.1 MHz Chebyshev low-pass Gm-C filter for ADSL," *IEEE Custom Integrated Circuit Conf.* pp. 387-390, May. 2000

[77] T. Itakura, T. Ueno, H. Tanimoto and T. Arai, "A 2Vpp linear input-range fully balanced CMOS transconductor and its application to a 2.5V 2.5MHz Gm-C LPF," *IEEE Custom Integrated Circuit Conf.* pp. 509-512, May 1999.

[78] H. Voorman and H. Veenstra "Tunable high-frequency Gm-C filters," *IEEE, J. Solid-State Circuits*, vol. 35, no. 8, pp. 1097-1108, Aug. 2003

[79] E. Rodriguez-Villegas, A. Yufera and A. Rueda "A 1.25-V micropower Gm-C filter based on FGMOS transistors operating in weak inversion" *IEEE, J. Solid-State Circuits*, vol. 39, no. 1, pp. 100-111, Jan. 2003.

[80] S. Hori, T. Maeda, N. Matsuno and H. Hida "Low-power widely tunable Gm-C filter with an adaptive DC-blocking, triode-biased MOSFET," *IEEE European Solid-State*

Circuits Conference, pp. 99-102, Sept. 2004.

[81] D. Chamla, A. Kaiser, A. Cathelin and D. Belot "A Gm-C low-pass filter for zero-IF mobile applications with a very wide tuning range," *IEEE, J. Solid-State Circuits*, vol. 40, no. 7, pp. 1143-1450, Jul. 2005.

[82] A.N. Mohieldin, E. Sanchez-Sinencio, J. Silva-Martinez, " A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector", *IEEE, J. Solid-State Circuits*, vol. 38, pp. 663-668, Apr. 2003

[83] A.N. Mohieldin, E. Sanchez-Sinencio, J. Silva-Martinez, " Nonlinear effects in pseudo differential OTAs with CMFB" *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 762-770, Oct. 2003.

[84] P. Kallam, E. Sanchez-Sinencio, A.I. Karsilayan, "An enhanced adaptive Q-tuning scheme for a 100-NHz fully symmetric OTA-based bandpass filter" *IEEE, J. Solid-State Circuits*, vol. 38, pp. 585-593, Apr. 2003

[85] J. Silva-Martinez, M. S. J. Stayert and W. M. C. Sansen, "A large-signal very low distortion transconductance for high frequency continuous-time filters" *IEEE, J. Solid-State Circuits*, vol. 26, pp. 949-955, Jul. 1991.

[86] A. Lewinski, J. Silva-Martinez," OTA linearity enhancement technique for high frequency applications with IM3 below -65dB*", IEEE Custom Integrated Circuit Conf.* pp. 181-184, Jun. 2003.

[87] D. Python, A. S. Porret, C. Enz, "A 1 V 5th-order Bessel filter dedicated to digital standard processes" *IEEE Custom Integrated Circuit Conf.* pp. 505-508, May. 1999.

[88] F. Rezzi, A. Baschirotto and R. Castello, "A 3 V 12-55 MHz BiCMOS pseudo-differential continuous-time filter" *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 896-903,

Nov. 1995.

[89] A. R. Bergen, L. O. Chua, A. I. Mees, and E. W. Szeto ”Error bounds for general describing function problems,” *IEEE Trans. Circuits Syst.,* vol. CAS-29, pp. 345-354, June 1982.

[90] A. Hajimiri and T. H. Lee, “Design issues in CMOS differential LC oscillators,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717-724, May 1999.

[91] J. Vosper, R. Deloughry and B. Wilson, “Multiphase active-RC sinusoidal oscillators incorporating lowpass and allpass sections,” *IEEE European Conf. Circuit Theory and Design*, pp. 27-30, Aug. 2005.

[92] A. Rodriguez-Vazquez, B. Linares-Barranco, J. L. Huertas, E. Sánchez-Sinencio, “On the Design of Voltage-Controlled Sinusoidal Oscillators Using OTA’s” *IEEE Transaction on Circuits and Systems*, vol. 37, No. 2, pp. 198-211, Feb. 1990.

[93] C. J. M. Verhoeven, A. V. Staveren, “First and second order oscillators” *IEEE Int. Symp. on Circuits and Systems*, Tutorial Guide. pp: 6.1_1-6.1_31, May 2001.

[94] B. Linares-Barranco, A. Rodriguez-Vazquez, E. Sánchez-Sinencio and J. L. Huertas, “CMOS OTA-C high-frequency sinusoidal oscillators,” *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 160-165, Feb. 1991.

[95] D. Vazquez, G. Leger, G. Huertas, A. Rueda and J. L. Huertas, “A method for parameter extraction of analogue sine-wave signals for mixed-signal built-in-self-test applications,” *European Conf. Design, Automation and Test*, vol. 1, pp. 298-303, Feb. 2004.

[96] F. Bahmani, E. Sánchez-Sinencio, “A Highly Linear Pseudo-Differential Transconductance” *IEEE European Solid State Conference*, pp. 111-114, Sept. 2004.

[97] F. Rezzi, A. Baschirotto and R. Castello, "A 3 V 12-55 MHz BiCMOS pseudo-differential continuous-time filter" *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 896-903, Nov. 1995.

[98] J. Chen, E. Sánchez-Sinencio, J. Silva-Martinez, "Frequency-dependent harmonic distortion analysis of a linearized cross-coupled CMOS OTA and its application to OTA-C filters," *To appear in IEEE Transaction on Circuits and Systems-I*, 2006.

[99] F. Baronti, D. Lunardini, R. Roncella and R. Saletti, "A self-calibrating delay-locked delay line with shunt-capacitor circuit scheme" *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 384-387, Feb. 2004.

[100] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design Layout, and simulation*. Piscataway, NJ: IEEE Press, 1998, Chap. 26.

[101] J. A. Weldon, J. C. Rudell, L. Li, R. Sekhar Narayanaswami, M. Otsuka, S. Dedieu, T. Luns, T. King-Chun, L. Cheol-Chun, P. R. Gray, "A 1.75 GHz highly-integrated narrow-band CMOS transmitter with harmonic-rejection mixers" *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003-2015, Dec. 2001.

[102] M. Chen, *Low-voltage, low-power circuits for data communication systems*, PhD Dissertation, Texas A&M University, College Station, 2003.

[103] A. B. Williams and F. J. Taylor, *Electronic Filter Deign Handbook*. Second edition. New York: McGraw Hill, 1988.

[104] J. Silva-Martinez, J. Adult, J. M. Rocha-Perez, M. Robinson and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system" *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 216-225, Feb. 2003.

[105] P. Pandery, J. Silva-Martinez and L. Xuemei, "A 500 MHz OTA-C 4th order lowpass filter with class AB CMFB in 0.35μm CMOS technology" *IEEE Custom Integrated Circuits Conference*, pp. 57-60, Oct. 2004.

[106] A. Batra, J. Balakrishnan, G. R. Aiello, J. R. Foerster, and A. Dabak, "Design of a multiband OFDM system for realistic UWB channel environments," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 9, pp. 2123–2138, Sep. 2004.

[107] "First report and order, revision of part 15 of the Commission's rules regarding ultra-wideband transmission systems," FCC,Washington, DC, ET Docket 98-153, Feb. 14, 2002.

[108] A. Batra *et al.*, "Multi-band OFDM physical layer proposal for IEEE 802.15 Task Group 3a," *IEEE*, Piscataway, NJ, IEEE P802.15-03/268r3-TG3a, Mar. 2004.

[109] B. Razavi, T. Aytur, F.-R. Yang, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A 0.13 _m CMOS UWB transceiver," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2005, pp. 216–217.

[110] J. Bergervoet, K. Harish, G. van der Weide, D. Leenaerts, R. van de Beek, H.Waite, Y. Zhang, S. Aggarwal, C. Razzell, and R. Roovers, "An interference robust receive chain for UWB radio in SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2005, pp. 200–201.

[111] R. Harjani, J. Harvey, and R. Sainati, "Analog/RF physical layer issues for UWB systems," in *Proc. 17th Int. VLSI Design Conf.*, Jan. 2004, pp. 941–948.

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