HAFNIUM-DOPED TANTALUM OXIDE HIGH-K GATE DIELECTRIC FILMS FOR FUTURE CMOS TECHNOLOGY

A Dissertation

by

JIANG LU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2005

Major Subject: Chemical Engineering

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Approved by:

Chair of Committee, Yue Kuo
Committee Members, Kenneth R. Hall
Ohannes Eknoyan
Mosong Cheng
Head of Department, Kenneth R. Hall

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ABSTRACT

Hafnium-Doped Tantalum Oxide High-K Gate Dielectric Films for Future CMOS Technology.

(December 2005)

Jiang Lu, B.S., East China University of Science and Technology, Shanghai, China

Chair of Advisory Committee: Dr. Yue Kuo

A novel high-k gate dielectric material, i.e., hafnium-doped tantalum oxide (Hf-doped TaO_x), has been studied for the application of the future generation metal-oxide-semiconductor field effect transistor (MOSFET). The film's electrical, chemical, and structural properties were investigated experimentally. The incorporation of Hf into TaO_x impacted the electrical properties. The doping process improved the effective dielectric constant, reduced the fixed charge density, and increased the dielectric strength. The leakage current density also decreased with the Hf doping concentration. MOS capacitors with sub-2.0 nm equivalent oxide thickness (EOT) have been achieved with the lightly Hf-doped TaO_x. The low leakage currents and high dielectric constants of the doped films were explained by their compositions and bond structures. The Hf-doped TaO_x film is a potential high-k gate dielectric for future MOS transistors.

A 5 Å tantalum nitride (TaN_x) interface layer has been inserted between the Hf-doped TaO_x films and the Si substrate to engineer the high-k/Si interface layer formation and properties. The electrical characterization result shows that the insertion of a 5 Å TaN_x between the doped TaO_x films and the Si substrate decreased the film's leakage current

density and improved the effective dielectric constant ($k_{effective}$) value. The improvement of these dielectric properties can be attributed to the formation of the TaO_xN_y interfacial layer after high temperature O_2 annealing. The main drawback of the TaN_x interface layer is the high interface density of states and hysteresis, which needs to be decreased.

Advanced metal nitride gate electrodes, e.g., tantalum nitride, molybdenum nitride, and tungsten nitride, were investigated as the gate electrodes for atomic layer deposition (ALD) HfO_2 high-k dielectric material. Their physical and electrical properties were affected by the post metallization annealing (PMA) treatment conditions. Work functions of these three gate electrodes are suitable for NMOS applications after 800°C PMA. Metal nitrides can be used as the gate electrode materials for the HfO_2 high-k film.

The novel high-k gate stack structures studied in this study are promising candidates to replace the traditional poly-Si-SiO_2 gate stack structure for the future CMOS technology node.

DEDICATION

For my family

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I would like to express my deepest appreciation to my Ph.D. advisor, Dr. Yue Kuo, for his consistent support, guidance, advice and encouragement throughout my five years of study at Texas A&M University. From him, I have learned the sincere spirit of being a researcher and scientist in the fields of industry and academia. His devotion and commitment to the work have inspired me to continue and accomplish the research on the state-of-the-art technology.

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CHAPTER I

INTRODUCTION

1.1. Challenge for Si-based CMOS Transistor Scaling

1.1.1. SiO_2 Gate Dielectric Material

The success of the silicon based semiconductor industry was mainly attributed to the excellent material and electrical properties of its native oxide: silicon dioxide (SiO_2), which has served as the gate dielectric for integrated circuit (IC) applications for more than 40 years.[1-4] SiO_2 can be thermally grown on Si with an easy fabrication process and good control of thickness and SiO_2/Si interface quality. The excellent properties of the SiO_2 gate dielectric material as shown in Table I, includes a high resistivity, a high melting point, a high amorphous to crystallization temperature, a large band gap, large electron and hole band offset, excellent dielectric breakdown strength, and a low defect density interface with Si substrate.[1-2] In addition, SiO_2 has the combination of some other required properties for the complementary metal-oxide-semiconductor (CMOS) field effect transistor (FET) devices, including high mobility of holes and electrons in CMOSFET devices channel, low electron or hole trapping density, and excellent CMOS processing.[3-4] The SiO_2/Si interface is the heart of the CMOS gate stack structure. Since the CMOS, as shown in Figure 1, devices constitute the building blocks of the integrated circuit, SiO_2 became the most economically and technically important material for the semiconductor industry. Indeed, Si, instead of other semiconductor materials such as Ge

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This dissertation follows the style and format of *Journal of the Electrochemical Society*.

and GaAs, was selected as the main material for the microelectronic semiconductor industry due to the lack of a stable native oxide and a low defect density interface for other semiconductor materials.

Table I Dielectric properties of SiO_2 gate dielectric [1-2]

SiO_2 is the only stable oxide phase on Si
Melting Point ~1713°C
Crystallization temperature ~1100°C
Resistivity~10^{15}Ω-cm
Dielectric Strength ~15MV/cm
Energy band gap ~9.0eV
Electron band offset with Si ~3.2eV
low interface (SiO_2/Si) state density ~$10^{10}eV^{-1}cm^{-2}$, after H_2 passivation
low charge trapping density ~$10^{10}cm^{-2}$

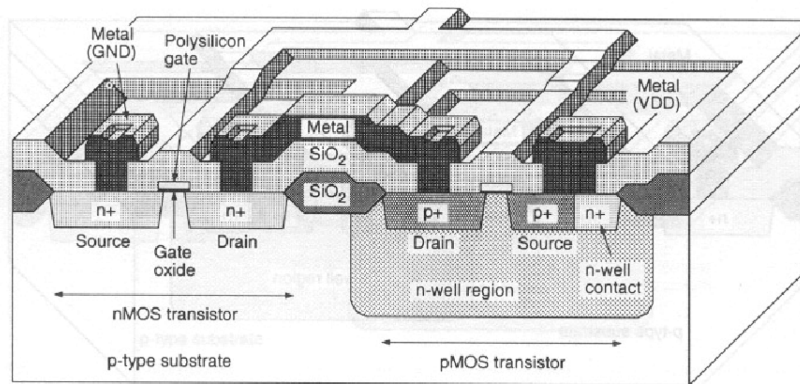


Figure 1 Schematic of a CMOSFET. (after reference 2)

1.1.2. Scaling of the CMOS Device

The scaling of the MOSFET devices to smaller physical dimensions has became the driving force for the semiconductor industry to meet the market's demand for greater functionality and performance of the integrated circuit at a low cost.[5-6] This was the primary activity of advanced device development almost since the basic technology was established. By reducing the device dimensions of the integrated circuits, the device performance can be greatly improved in terms of switch speed.[1] Meantime, the manufacturing cost of each device can also be reduced by decreasing the device dimensions.

The improvement of the device performance can be achieved by scaling the gate channel length of the MOSFET device structure. The drive current (I_D) of a device available to switch its load devices increases linearly with the decrease of the physical channel length, which usually provides an improvement in the circuit speed. This can be explained by a simple model of an on-state transistor current as, [7]

$$I_D = \frac{W}{L}\mu C_{inv}(V_{GS} - V_T)V_{DS} \quad [1]$$

where W is the effective channel width, L is the effective channel length, μ is the carrier mobility in the channel (assumed constant here), C_{inv} is the gate capacitance density with channel in inversion, V_{GS} is the gate to source voltages, and V_{DS} is the drain to source voltages, and V_T is the threshold voltage. Equation 1 shows I_D will increase linearly with V_{DS}. Eventually, I_D will saturate when V_{DS}=$V_{DS\,sat}$=V_{GS}-V_T and yield [7]

$$I_D = \frac{W}{L}\mu C_{inv}\frac{(V_{GS} - V_T)^2}{2} \quad [2]$$

Based on this simple model, the drive current of a device increases linearly with the decrease of the physical channel length. Meanwhile, the gate area of the minimum MOSFET device will also decrease with the reduction of the gate channel length, which will reduce the input capacitance and the current required by the load devices to achieve switching, and thus improve the circuit speed. Therefore, the benefit in device reduction for the improvement of the device performance is two-fold.

The economic benefit in device reduction is even more straightforward. Since the semiconductor devices are manufactured by single-wafer or batch processes, packing more devices onto each wafer can lower the manufacturing cost for each device. In the semiconductor industry, function cost (dollar/device) is the conventional term used to describe the manufacturing cost for the semiconductor manufacturer. For decades, a continuously falling functional cost has been a critical factor in stimulating an ongoing demand for electronics and semiconductor products worldwide. As the capital investment and expecting revenue increased, the industry had to expand the total number of transistors built or the number of transistors per chip to maintain an essentially flat manufacturing cost per square centimeter of Si wafer area. As a result, the critical dimensions of CMOS devices decreased from 10-20 μm to below the 0.1 μm range over the last half-century of the microelectronic industry development.

Moore observed the number of transistors per integrated circuit increased exponentially and the integrated circuit density doubled every 18 months; this is now known as Moore's law.[8-9] He predicted that this trend would continue. Figure 2 shows the advancement of the Intel processor. Moore's law has been successfully maintained for

thirty years, and still holds true today. Semiconductor industry expects that it will continue at least through the end of this decade.

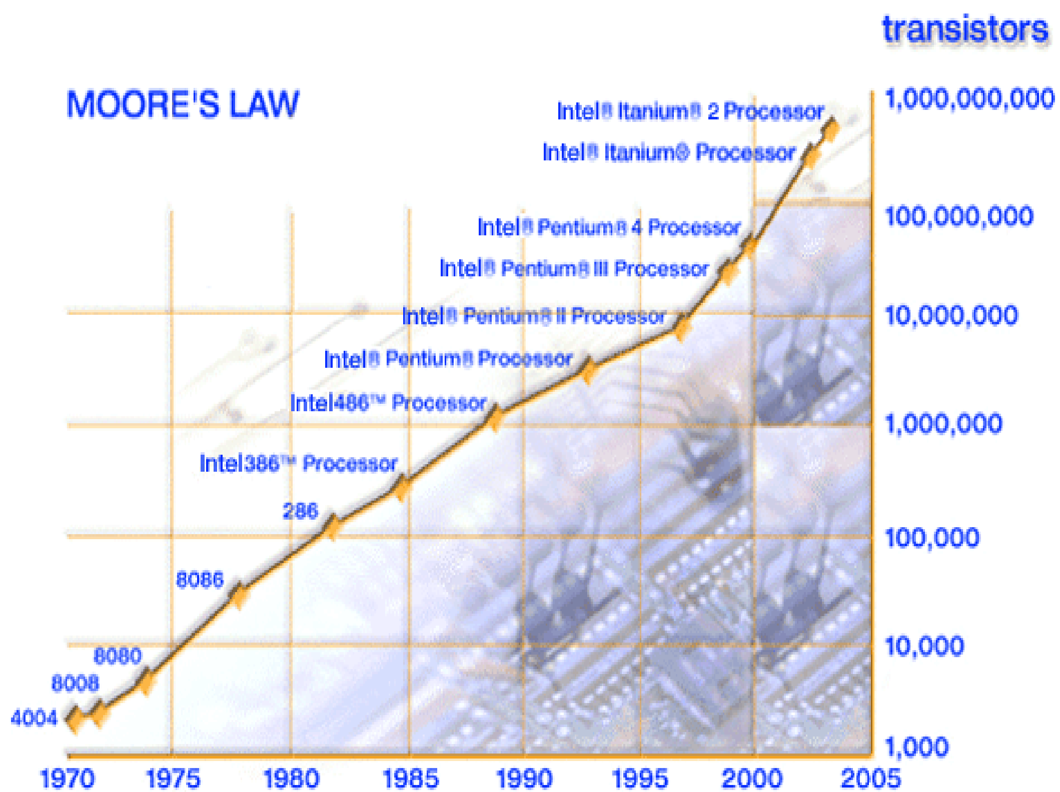


Figure 2 Illustration of Moore's law. (After reference 9)

1.1.3. Scaling of the Gate Oxide

The scaling down of the device dimensions could not be done randomly. With the reduction of the gate channel length and gate area, the inversion gate capacitance density C_{inv} will decrease accordingly, as shown in Eq.3,

$$C_{inv} = \frac{\varepsilon_0 kA}{t} \qquad [3]$$

where ε_0 is the permittivity of the vacuum (8.85×10^{-14}F/cm), k is the dielectric constant of the gate dielectric material, and t is the physical thickness of the gate dielectric. The physical thickness of SiO_2 gate dielectric films should be approximately linearly scaled down together with the lateral channel dimensions of the CMOS device in order to maintain the same amount of gate control over the channel.

Figure 3 shows the ratio of gate channel length (L_E) to gate oxide thickness (T_{ox}) was ~45 over the past thirty years.[10] A more detailed device scaling requirement was provided by the International Technology Roadmap for Semiconductors to keep the industry on Moore's Law. [11] As illustrated in Table II, [3, 11] the equivalent oxide thickness (EOT) of the gate dielectric material should decrease with the advance of the future generation of Si-based MOSFET technologies. EOT less than 1.5nm will be required for both the high performance application devices and low operating power application devices when the technology node scales down to 70nm, which should be fulfilled in the year 2006.

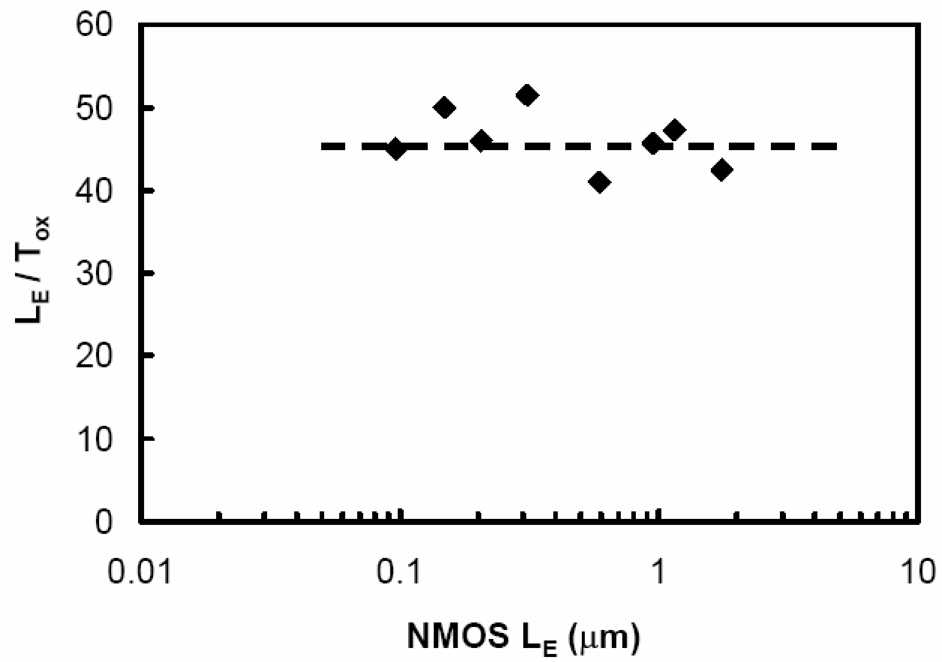


Figure 3 The L_E/T_{ox} ratio was fixed ~45 for Intel® process technology over 30 years. (After reference 10)

Table II EOT requirements for the future generation of MOSFET technology [3, 11]

Technology node (nm)	Production Year	EOT (nm)	
		High Performance	Low Operating Power
150	**2001**	**1.3-1.6**	**2.0-2.4**
130	**2002**	**1.2-1.5**	**1.8-2.2**
107	**2003**	**1.1-1.4**	**1.6-2.0**
90	**2004**	**0.9-1.4**	**1.4-1.8**
80	**2005**	**0.8-1.3**	**1.2-1.6**
70	**2006**	**0.7-1.2**	**1.1-1.5**
65	**2007**	**0.6-1.1**	**1.0-1.4**
45	**2010**	**0.5-0.8**	**0.8-1.2**
25	**2016**	**0.4-0.5**	**0.6-1.0**

1.1.4. Problems of Ultra-thin SiO_2 Gate Dielectric

At this thickness, the conventional thermally grown SiO_2 gate oxide will approach its physical thickness limit due to several concerns, as illustrated in Figure 4: exponential increase in tunneling leakage current with decreasing gate oxide thickness, poor reliability, undesirable boron diffusion from the polysilicon gate through the oxide, and high density of defects and poor uniformity of the gate oxide.[5]

High Direct Tunneling Current

High gate tunneling current is the first concern to use the SiO_2 gate dielectric in the sub-100 nm MOSFETs. As the oxide thickness scales down below 1.5 nm, the dominant conduction mechanism for the leakage current will be a quantum mechanic tunneling mechanism, or direct tunneling. The direct tunneling gate-to-channel leakage current for SiO_2 increases exponentially as the thickness of the SiO_2 gate oxide decreases as shown in Figure 5.[12] For a 1.5 nm thick SiO_2 layer, the leakage current density will reach ~10A/cm^2 when the gate voltage is 1V, which will result in excessively high power consumption. According to the specification from the IRTS, the scaling limit of the SiO_2 gate oxide in terms of leakage current should be 2.2-2.5 nm for a low operating power application and 1.4-1.6 nm for a high performance application.[3, 11]

It was reported that transistors with 1.3-1.5 nm thick SiO_2 gate oxide could still be used for a high performance application but not for a low power application due to their high gate leakage current density (1-10 A/cm^2). [13-14] As the SiO_2 gate oxide thickness scaled down below 1.0-1.2 nm, no further improvement in transistor drive current could be achieved. [15-18]

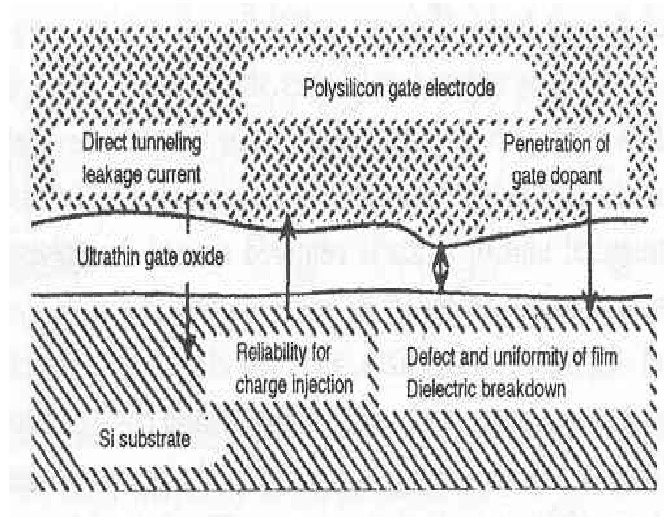


Figure 4 Concern of ultra-thin SiO_2 gate oxide. (After reference 5)

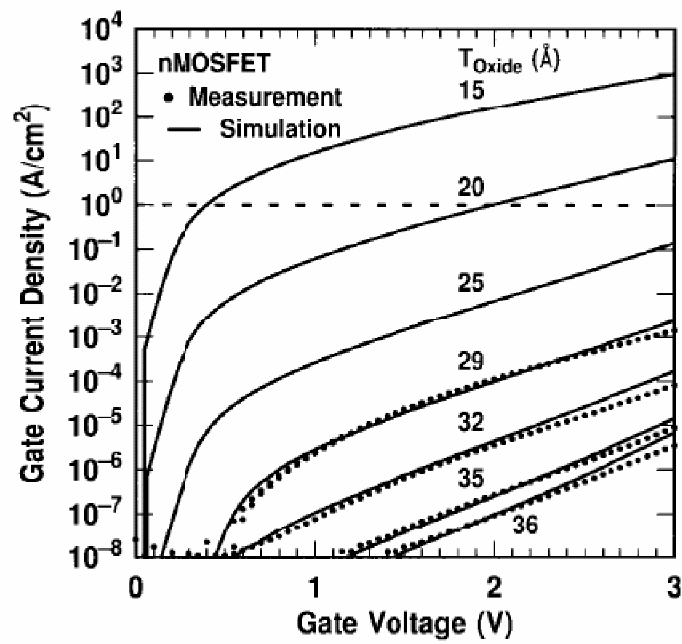


Figure 5 Measured and simulated gate leakage currents for SiO_2 dielectrics. (After reference 12)

Reliability Issue

The reliability aspect is another concern related to the SiO_2 gate oxide scaling. A stringent ten year lifetime and less than 0.01% failure rate are required for the CMOS devices.[19] Based on the extrapolations of time-dependent dielectric breakdown stress tests, a minimum 2.2 nm thick SiO_2 will be required to satisfy the reliability specifications of ITRS. However, a 1.6 nm thick SiO_2 was first reported to have reliability projections at an operation voltage of 1.6 V for over ten years. [20] More recently, a 1.4 nm thick SiO_2 was projected to meet the ten year reliability requirement at an operation voltage of 1.4V. [21] Similar conclusions had also been independently reached by several groups. [22-23] All of these observations suggest that no intrinsic reliability limitation existed for the SiO_2 ultra-thin gate oxide at least down to thicknesses of 1.4 nm. But some extrinsic reliability factors including contaminations and particles could still reduce to life time of the MOSFETs with ultra-thin SiO_2 gate oxides and become a serious reliability concern.

Boron Diffusion from the Poly-Si Gate

Boron in the heavily doped poly-Si gate electrode tends to penetrate through an ultra-thin SiO_2 gate oxide upon a high temperature treatment due to the large boron concentration gradient between the poly-Si gate and the Si channel region. This will lead to a high boron concentration at the Si channel and then cause an undesirable threshold voltage shift of the MOSFETs. The electrical characteristics of the devices will become unpredictable due to boron diffusion. Incorporation of nitrogen into the oxide can reduce the boron diffusion to a certain extent. But eventually, boron diffusion will be a significant concern for the practical application of the ultra-thin SiO_2 gate oxide.

Material Issues of Ultra-thin SiO_2

Some material properties of ultra-thin SiO_2 such as band gap and band offset may change with the decreasing SiO_2 gate oxide thickness. [24-27] Muller et al. studied 0.7-1.5 nm thick SiO_2 ultra-thin films on Si by energy loss spectroscopy (EELS), and they found that a minimum of two monolayer of SiO_2 would be needed to obtain a full band gap.[24] The thickness of a SiO_2 monolayer is about 3.5-4.0 Å, therefore at least a 0.7-0.8 nm thick SiO_2 gate oxide will be required to exhibit an insulator property. This thickness will be the ultimate scaling limit for the SiO_2 gate oxide.

1.1.5. Silicon Oxynitride Dielectrics

Silicon oxynitride or nitride/oxide stack structures were studied to replace SiO_2 as the alternative gate dielectric material. Since silicon nitride (Si_3N_4) has a higher dielectric constant (k~7) than SiO_2, a thicker film can be used for low gate leakage current, reduced boron diffusion, and better reliability.[28-30] In addition, proper incorporation of nitrogen (~0.1%) near the Si channel interface may also improve device performance.[31] However, too much nitrogen near the Si channel will degrade the performance of the MOSFETs with low carrier mobility and drive current. [32] Actually, silicon oxynitride has been used as a gate dielectric in most advanced high performance technologies. A 1.2 nm thick thin layer with a reasonable leakage current density may be used for the 70 nm node high performance technology. But with the further scaling of the gate oxide thickness to less than 1.0 nm, silicon oxynitride will lose its advantages due to high gate leakage current, high interface state density, and channel carrier mobility degradation.[33] In summary,

silicon nitride and oxynitride can only provide a near term solution for the CMOS transistor.

1.1.6. Poly Depletion Effects

Poly-Si gate electrodes have been used for Si based MOSFET structures for over 30 years because it is a self-aligned process. However, poly-Si gate electrodes will form a depletion layer in the poly-Si near the gate/dielectric interface, especially when the Si channel is biased to an inversion condition. Poly-Si nearest to the gate dielectric layer will behave like intrinsic Si and therefore, a corresponding increase of about 5 Å effective oxide thickness will be observed. With the decrease of the gate capacitance in inversion condition, the drive current will decrease accordingly. The poly depletion effects will be aggravated with a lower poly-Si doping concentration and a thinner gate oxide thickness. [34-36]

1.1.7. Quantum Mechanic Effects

Ultra-thin gate oxide may also lead to a quantum mechanical carrier quantization. [37] The decreasing gate oxide thickness and the increasing substrate doping density will cause a higher transverse electric field in the inversion layer. The sharp bending of the energy bands will cause a significant quantization of the carriers normal to the oxide/Si interface. The quantum mechanic effects occur when the carriers are confined in a narrow potential well. The quantum mechanic effects will cause the conduction and valence energy bands to split into sub-bands. The effective Si band gap increases slightly because the lowest sub-band is above the edge of the conduction band, as shown in Fig.6 (a). Due to the formation of the sub-bands, the charge distribution peak is shifted further from the surface than classical theory predicts, as illustrated in Fig.6 (b). [37] Hence, the centroid of induced charge shift into the Si substrate and a depletion region is formed near the oxide /Si interface, which is equivalent to adding a capacitor in series with the gate dielectric layer. About 3-5Å EOT increase will be contributed to the quantum mechanic effects of the Si substrate.[37]

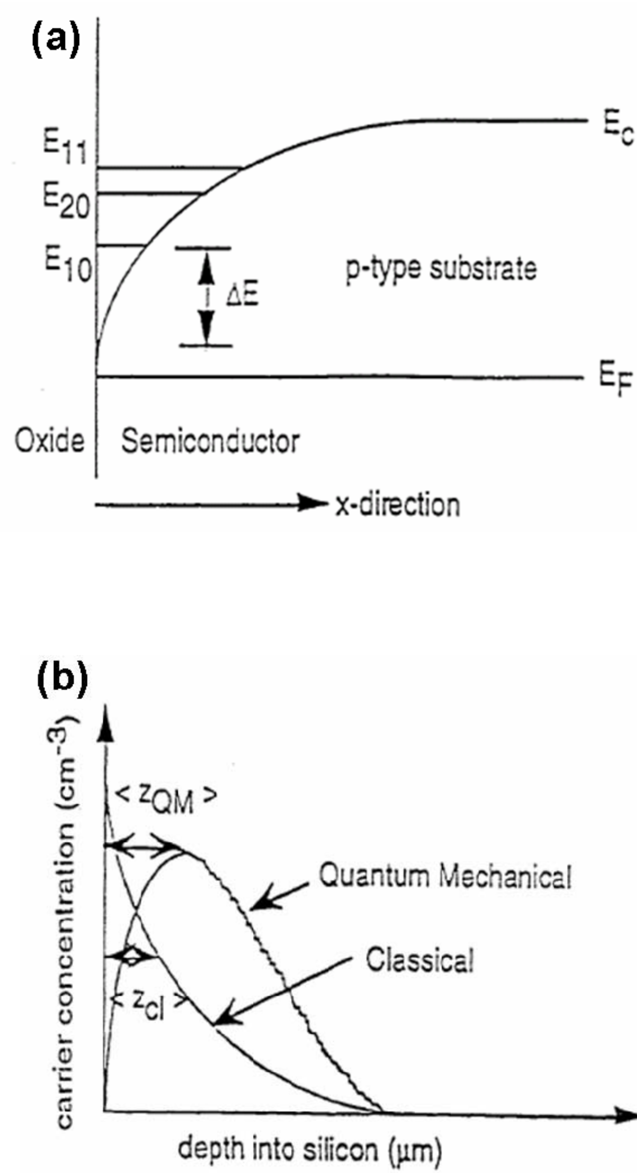
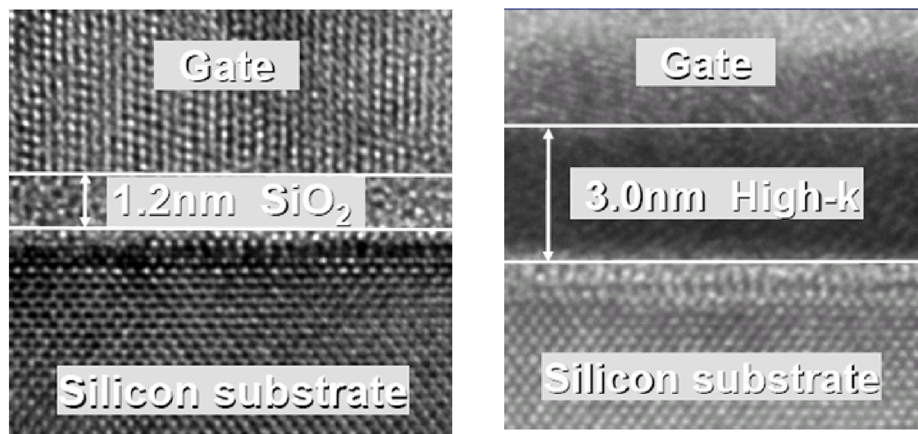


Figure 6 Illustrations of quantum mechanic effects. (After reference 37)

1.2. Alternative High-K Gate Dielectric Materials

As discussed in the previous section, as the channel length of MOSFETs scales down to sub-70 nm feature size, a corresponding SiO_2 gate oxide with a thickness less than 1.5 nm will be required. At this thickness, the conventional thermally grown SiO_2 gate oxide will approach its physical thickness limit due to three major problems: exponential increase in tunneling leakage current with decreasing film thickness, poor reliability, and undesirable boron diffusion from the poly-Si gate through the oxide. According to Eq. 3, using a new gate dielectric material with a high dielectric constant (k) to replace the SiO_2 will allow the use of a physically thicker gate dielectric layer while maintaining the same control of inversion charge. With a thicker insulating layer, the concern of a high tunneling current through the gate oxide and other reliability issues may be solved efficiently. Figure 7 shows that using a 3.0 nm thick high-k gate dielectric layer may improve the capacitance by 60% and decrease the leakage current density by 2 orders of magnitude. [38]



90nm Process	**Experimental High-K**
Capacitance 1X	Capacitance 1.6 X
Leakage 1X	Leakage 0.01X

Figure 7 Benefit of using high-k gate dielectric material vs. ultra-thin SiO_2 gate oxide. (After reference 38)

Equivalent oxide thickness (EOT) is a very important parameter for the alternative high-k gate dielectric materials. It is defined as the thickness of a SiO_2 gate oxide layer that would be required to achieve the same capacitance density as the desired high-k gate dielectric material. The relation between EOT and the physical thickness of a high-k gate dielectric material is given as,

$$\mathbf{EOT} = (\mathbf{k}_{\mathbf{SiO_2}} / \mathbf{k}_{\mathbf{high-k}})\mathbf{T}_{\mathbf{high-k}} \qquad [4]$$

where k_{SiO2} is the dielectric constant k value of the SiO_2 gate oxide, $k_{high\text{-}k}$ is the dielectric constant k value of the high-k gate dielectric material, and $T_{high\text{-}k}$ is the physical thickness of the high-k gate dielectric material. Further scaling of CMOS device dimensions may continue if smaller EOT can be achieved by using a thicker high-k dielectric layer. However, there are many issues related to the incorporation of high-k gate materials into the traditional CMOS fabrication process. A proper alternative high-k gate dielectric material has to be found to meet the stringent requirements for the gate dielectric.

1.2.1. Candidates for Alternative High-k Gate Dielectrics

Metal oxides, such as Ta_2O_5 and TiO_2, have been extensively studied as candidate materials due to their large dielectric constant k values, ranging from 20 to 80. But these oxide systems are not thermodynamically stable in direct contact with Si.[39] A low-k interface layer will be formed at an elevated temperature, which will degrade the overall performance of the high-k gate stack structure.

Al_2O_3 has also been widely studied as the alternative high-k gate dielectric material because of its robust material properties such as a high band gap (~9.0 eV), a high amorphous to crystalline transition temperature (~1000°C), and good thermodynamic

stability on Si. [40] But Al_2O_3 has a relatively low dielectric constant k value (~9) and thus it can only offer a short-term solution for CMOS device scaling. In addition, Al_2O_3 has a similar reactive ion etch (RIE) characteristic with Si, which makes it very difficult to integrate into a traditional CMOS fabrication flow.

Some researchers have done a lot of investigation on the group IIIB metal oxides such as Y_2O_3 and La_2O_3 because they have a reasonably high dielectric constant and good thermodynamic stability on Si.[41-45] The dielectric constant k value of Y_2O_3 is 17 grown on SiO_2. This value decreases to 12 when it is grown on bare Si possibly due to the growth of low-k interface layers upon high temperature treatment. Chin at el.[41] reported a very low EOT (~4.8 Å) can be achieved using a 3.3 nm thick La_2O_3 layers. Low leakage current density (~10^{-1}A/cm @ 1.0 V gate bias) and excellent interface state density (D_{it}~$3\times10^{10}$$eV^{-1}cm^{-2}$) were also obtained for these films. However, the pure La is very volatile and reactive at the exposure to the air and La_2O_3 tends to absorb water vapor from the air. These material properties require a very rigorous environment control during the fabrication process. Device reliability is another concern for the practical application of this material.

Group IVB metal oxides such as HfO_2 and ZrO_2 have attracted the most attention as alternative gate dielectrics. With an excellent thermodynamic stability on Si and relatively large barrier heights, HfO_2 and ZrO_2 were considered as the most promising alternative high-k gate dielectric material.[1,46-48] In addition, their silicates also exhibited excellent dielectric properties and were considered as a short term solution for the alterative gate dielectric material for one or two generation products.[49-51]

In addition to materials discussed earlier, many other metal oxides were also investigated as the candidate high-k gate dielectric materials, including Gd_2O_3, Pr_2O_3 and etc. [1] In spite of the excellent material properties of all of the above material systems, no material can meet all of the stringent requirements for the alternative gate dielectric material.

1.2.2. Materials Requirements for High-k Gate Dielectrics

There are a set of material and electrical requirements for a viable alternative high-k gate dielectric material, [1, 3] e.g.

- large energy band gap with high barrier height to Si substrate and metal gate to reduce the leakage current;
- good thermodynamic stability on Si to prevent the formation of a low-k SiO_2 interface;
- high amorphous-to-crystalline transition temperature to maintain a stable morphology after heat treatment;
- low oxygen diffusion coefficients to control the formation of a thick low-k interface
- low defect densities in high-k bulk films and at the high-k/Si interface with negligible CV hysteresis (<30 mV), low fixed charge density ($\sim10^{10}cm^{-2}eV^{-1}$), and low high-k/Si interface state density ($\sim10^{10}cm^{-2}eV^{-1}$);
- high carrier channel mobility (~90% of SiO_2/Si system);
- good reliability and a long life time.

In addition, the new high-k gate dielectric material must be compatible with current CMOS fabrication process flow and other materials used in the CMOS integrated circuits. In the following sections, some of the most important requirements for the high-k gate dielectric material will be introduced.

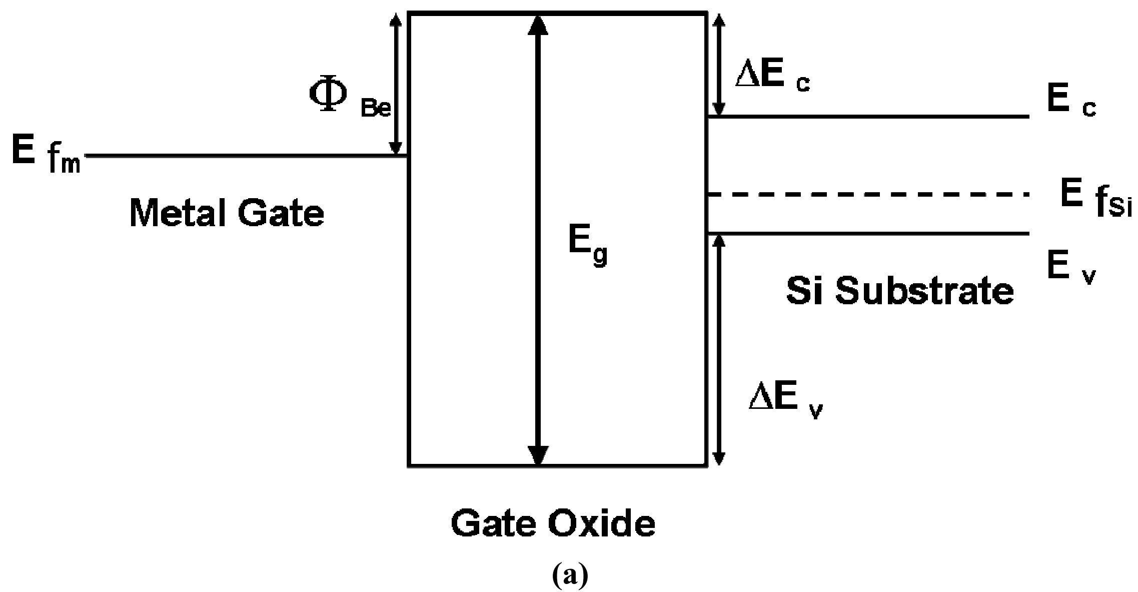
Energy Band Gap and Barrier Height

It is crucial to use a material with a high dielectric constant k value to replace SiO_2 as the gate dielectric material. However, the energy band gap (E_g) of a metal oxide is in an inverse relation to its dielectric constant k value, [52]

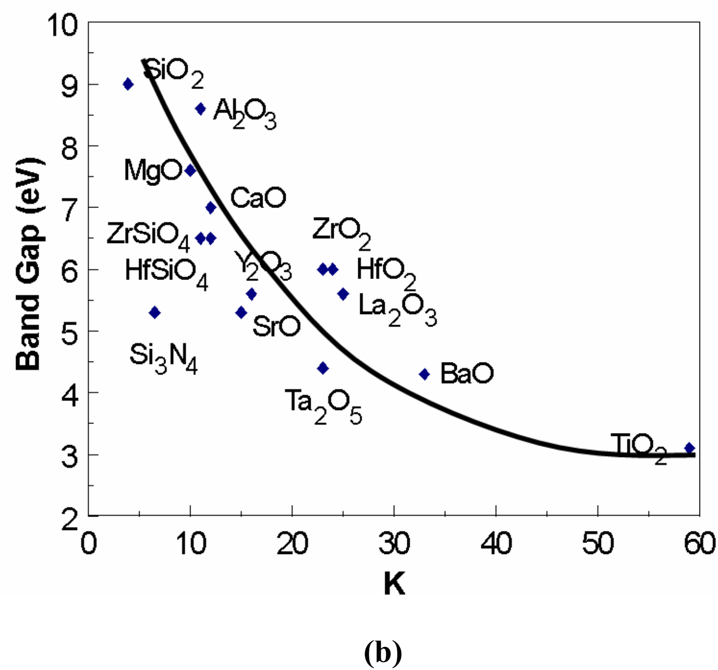
$$\mathbf{E_g = 20 \times \left(\frac{3}{2+k}\right)^2} \qquad [5]$$

Figure 8(a) shows a schematic band diagram of a MOS structure and Fig 8(b) shows the energy band gap and dielectric constant k values of some alternative candidate's high-k gate dielectric materials. [53] Generally, materials with a high-k value have a relatively small energy band gap as shown in Eq.5. A small energy band gap is usually equivalent to a small barrier height for the tunneling process.

When electrons travel from gate to Si substrate, the barrier height will be a potential barrier between the gate and dielectric (Φ_{Be}); when electrons travel from the Si substrate to the gate, the barrier height will be conduction band offset of the dielectric layers to Si (ΔE_c). For an electron direct tunneling conduction mechanism, the leakage current density through thin gate dielectric will increase exponentially with the decrease of barrier height.[54-55] Therefore, a high-k gate dielectric material with a large conduction band offset to Si will be preferred to avoid an unacceptable high leakage current through



(a)



(b)

Figure 8 (a) Band diagram of MOS structure, (b) band gap versus dielectric constant k value of some high-k gate dielectric candidate materials. [52]

Table III Band gap, conduction band offset, and valence band offset of some gate dielectric materials. [56-57]

Gate Dielectric Materials	Energy Band Gap E_g (eV)	Conduction Band Offset ΔE_c (eV)	Valence Band Offset ΔE_v (eV)
SiO_2	9	3.5	4.4
Si_3N_4	5.3	2.4	1.8
Al_2O_3	8.8	2.8	4.9
Y_2O_3	6	2.3	2.6
La_2O_3	4.3	2.3	0.9
Ta_2O_5	4.5	0.3	3.1
TiO_2	3.5	1.2	1.2
HfO_2	6	1.5	3.4
ZrO_2	5.8	1.4	3.3
$ZrSiO_4$	6	1.5	3.4

the gate dielectric. Simple metal oxides with a conduction band offset less than 1.0 eV will be inappropriate for the gate dielectric applications with a Si substrate. Robertson et al. theoretically calculated the energy band gap and band offsets of many candidate high-k gate dielectric materials, as summarized in the Table III. [56-57]

Thermodynamic Stability on Si

If a thin high-k gate dielectric material is not thermodynamically unstable on Si, it tends to react with Si at an elevated temperature and an interface layer will be formed between the high-k layer and Si substrate as illustrated in Figure 9.

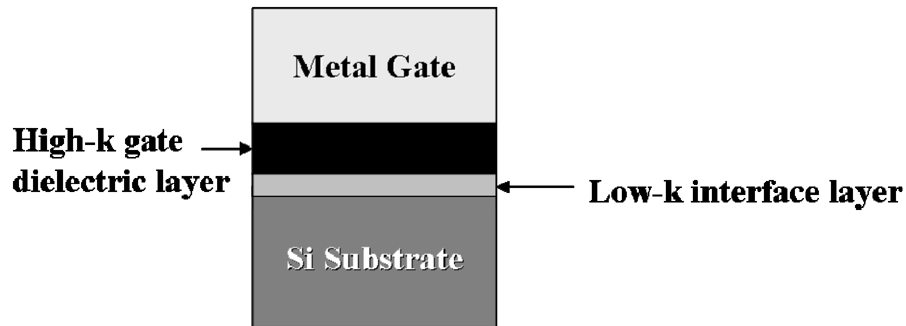


Figure 9 High-k gate stack structure with a low k interface between high-k and Si.

This interface layer usually has a similar k value with SiO_2 and acts as a series capacitor with the high-k dielectric layer. This low-k interface will play an important role in the electrical properties of the final high-k gate stack structures. It will set the ultimate scaling limit for the high-k gate stack structures as shown in the Eq.6,

$$\mathbf{EOT} = \frac{3.9 \times \mathbf{T}_{low-k}}{\mathbf{k}_{low-k}} + \frac{3.9 \times \mathbf{T}_{high-k}}{\mathbf{k}_{high-k}} \qquad [6]$$

where $T_{low\text{-}k}$ is the physical interface layer thickness, $k_{low\text{-}k}$ is the k value of the interface layer, $k_{high\text{-}k}$ is the k value of high-k layer, and $T_{high\text{-}k}$ is the physical thickness of the high-k gate dielectric material. The formation of this low-k interface layer must be minimized in order to achieve a low EOT. A high-k gate dielectric material with a good thermodynamic stability on Si should be used. Otherwise, a barrier layer with a high

dielectric constant k value has to be inserted between the high-k layer and Si to hinder the formation of a low-k interface layer.

Ternary phase diagrams can be used to predicate the thermodynamic stability of metal oxide on Si.[1,58-59] Figure 10 (a) and (b) shows no direct tie lines between Ta_2O_5 and Si or between TiO_2 and Si at ~700°C to 900°C when the thermodynamic equilibrium state is reached. When Ta_2O_5 and TiO_2 are in direct contact with Si, they tend to phase separately into SiO_2 and metal oxide or silicide. The tie lines in the ternary phase diagram of the Zr-Si-O system suggest both ZrO_2 and $ZrSiO_4$ can be stable in direct contact with Si at a high temperature. Based on the similar coordination chemistry between the Hf and Zr element, the same ternary phase diagram can be expected for the Hf-Si-O system.[1] Other independent studies confirmed that both HfO_2 and Hf silicate can be thermally stable in direct contact with Si up to a high temperature.[60-62]

Hubbard and Schlom calculated the Gibb's free energy governing the relevant chemical reactions for many high-k candidate materials.[39] Their results also indicated that ZrO_2 had a better thermodynamic stability on Si than Ta_2O_5 and TiO_2.

It is noted to point out that the phase diagram alone can be misleading about the interface layer formation. This is because the phase diagram data here are from the reaction of two stoichiometric materials at an equilibrium state. This may not be true for the ultra-thin high-k films deposited by CVD or PVD methods, because the films are formed in a non-equilibrium condition for both cases. The phase diagram can only be used as a reference for interface reaction in this study.

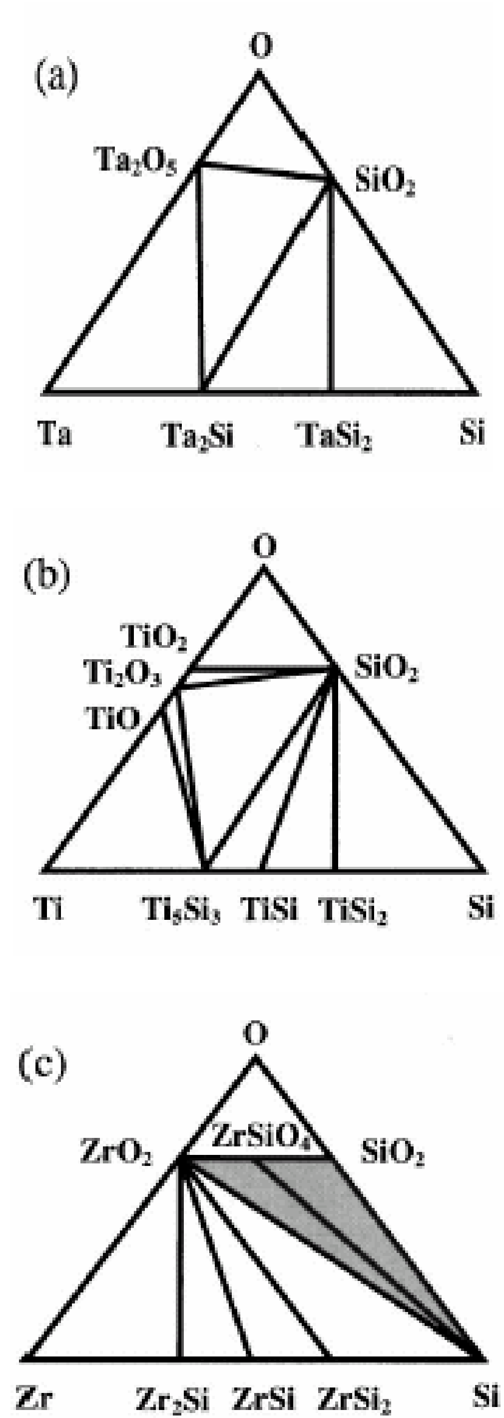


Figure 10 Ternary phase diagrams for (a) Ta–Si–O, (b) Ti–Si–O, and (c) Zr–Si-O systems at 700°C to 900°C. (From reference 1, 58-59)

Amorphous-to-Crystalline Transition Temperature

For the gate dielectric application, high-k gate dielectric materials are preferred to be amorphous throughout the CMOS fabrication process flow. A polycrystalline gate dielectric layer will suffer a high leakage current because the grain boundaries of the polycrystalline films may serve as a leaky path.[63-64] Variance in the grain size and crystal orientation of the polycrystalline films may also cause a non-uniform dielectric property within the dielectric films, which will become a reliability concern for the practical application. Although single crystal oxides may theoretically solve the problems caused by grain boundaries and provide films with good quality, they can only be grown by a molecular beam epitaxy (MBE) deposition method. [45, 65] However, it will be a great challenge to incorporate MBE deposition into the traditional CMOS fabrication process flow due to the inherent low throughput. In contrast, high quality amorphous high-k gate dielectrics can be easily deposited by commercial equipment. Amorphous high-k gate dielectric layers will also offer the reproducible and isotropic dielectric properties.

Almost all metal oxides of interest tend to crystallize either during deposition or after heat treatment. For traditional CMOS fabrication process flow, above 1000°C heat treatment will be needed for the source/drain and poly-Si dopant activation after ion implantation. Therefore, an amorphous-to-crystalline transition temperature above 1000°C will be required. For example, HfO_2 and ZrO_2 will crystallize at a very low temperature (~500°C). [66-67] Of all the high-k candidate materials, only Al_2O_3 can stay amorphous at this temperature. However, Al_2O_3 does not have a sufficient high dielectric constant k value. Adding a third element into the simple metal may increase the amorphous-to-crystalline transition temperature. [68]

High Quality Interface

SiO_2-Si offered the best interface quality (D_{it} ~10^{10} $eV^{-1}cm^{-2}$) for the Si channel area of the MOSFETs. A comparable interface quality will be expected between the high-k gate dielectric and Si. However, almost all high-k materials exhibit one or two orders of magnitude high interface state density and significant flatband voltage shift ΔV_{FB} mainly due to a high fixed charge density. The origin of the high interface defect density is still under intensive investigation.

Lucovsky et al. [69] reported that bonding constrains of the high-k materials may play a significant role determining high-k/Si interface quality. Experiment results showed that if the average number of bonds per atom is over 3 for a metal oxide, an over-constrained high-k/Si interface will form and the D_{it} will increase exponentially. Other degradation of device performance will also be expected, i.e., high leakage current density and low electron channel mobility. Similarly, a metal oxide with a low coordination number will form an under-constrained high-k/Si interface, which will also lead to a high interface state density and poor device performance. In addition, formation of metal silicide at the interface will also generate unfavorable bonding conditions to the device characteristics. Ideally, no metal oxide or silicide should be present at or close to the dielectric/Si interface.

Of all the high-k gate dielectric candidate materials, Ta_2O_5 and TiO_2 will form an over-constrained interface with Si. Y_2O_3 and La_2O_3 will form an under-constrained interface with Si. Only ZrO_2 and HfO_2 can meet the requirements of bonding constrains. However, these two materials have high oxygen diffusivities, which will present another challenge for the interface thickness control.[70]

1.3. Doped TaO_x Gate Dielectric

Tantalum pentoxide (Ta_2O_5) has been the most widely studied alternative high-k gate dielectric material due to its high dielectric constant value (~25). In addition to CMOS devices, it may also be used in other applications, such as optical devices, high density dynamic random access memory (DRAM), thin-film electroluminescent (TFEL) devices, and biological sensors.[71-75] However, Ta_2O_5 has several disadvantages to serve as a high-k gate dielectric for the Si-based CMOS transistors, including poor thermodynamic stability with Si, small electron barrier height with the Si conduction band, and low amorphous-to-crystallization temperature (~650-700°C). [39,64,76-79] Therefore, pure Ta_2O_5 cannot serve as the alternative high-k gate dielectric material for the future generation CMOS transistors without a barrier interface layer.[1]

Dielectric properties of the binary metal oxide can be improved by the doping technique, i.e., adding a third element into the binary metal oxide high-k gate dielectric.[80-82] Ta_2O_5 is a good base material for this purpose because its chemical structure is stable after adding proper amounts of dopants.[83] Different types of dopants, e.g., Zr, Ti, Al, have been added into the Ta_2O_5 and the improvement of dielectric properties, such as dielectric constant, frequency dissipation factor, and temperature coefficient, had been reported.[83-85] In addition, adding a third element into the binary metal oxide may also improve its amorphous-to-crystallization temperature by distorting the original bond structure order.[86] In this study, the dielectric properties of the sputter-deposited Hf-doped TaO_x high-k gate dielectric were studied by electrical and chemical characterizations.

1.4. Insertion of Nitride Interface Layer

A high quality high-k/Si interface layer is crucial for high performance CMOS devices. Both the chemical composition and fabrication process of the bulk high-k dielectric layer can affect the properties of the high-k/Si interface layer. [87-88] Although some promising high-k materials, e.g., HfO_2 and ZrO_2, are theoretically predicted to be stable in direct contact with Si, a low quality interface layer may still exist after a high temperature annealing treatment, which will limit the ultimate EOT scalability of the high-k gate stack structures. [1, 87-90] Therefore, the most challenging issue for implementing the high-k gate dielectric materials for the MOSFET applications is engineering the high-k/Si interface layer.

Insertion of a high-quality interface layer between the high-k gate dielectrics and Si substrate is a possible solution to hinder the formation of a low quality interface layer. A silicon nitride (Si_3N_4) or oxynitride (SiON) interface layer has been used to reduce the formation of low quality SiO_x between the Ta_2O_5 and Si wafer.[64,91-92] It was reported that incorporation of nitrogen into the bulk high-k layer or interface layer would decrease the oxygen diffusion and therefore minimize the formation of the SiO_x interface layer.[87 of John] Since the Si_3N_4 and SiON interface layer have a dielectric constant k value greater than that of SiO_x, the overall effective dielectric constant k value will be increased. Incorporation of the nitrogen into the high-k gate stack structures may also improve its thermal stability and amorphous-to-crystalline transition temperature. [93-94] In addition, the nitrogen atoms are effective to reduce the leakage current by blocking the electron transport at the interface and releasing the stress between the stacked layers. However, the traditional silicon nitride or oxynitride interfacial layer does not have a very high k

value and therefore, cannot contribute too much to the overall capacitance or dielectric constant of the stacked high-k gate dielectrics. In this study, a 5 Å thin, non-stoichiometric TaN_x interface layer is investigated as the barrier interface layer between the high-k gate dielectric and Si wafer.

1.5. Metal Gate Electrodes

The major problem of the conventional poly-silicon gate electrode is the depletion of carriers within the polysilicon in the MOS inversion region, which will result in loss of current drive and transconductance of the transistor.[95] This poly-silicon depletion is a serious problem for sub micron CMOS devices because the active poly-silicon dopant concentration is low at the poly-silicon/gate oxide interface as a result of shallow junctions. In addition, the sheet resistance of the poly-silicon increased drastically with the continuous scaling of the device dimensions, which would limit the MOSFET circuit's speed. Boron dopant penetration through the thin gate oxide during the activation thermal cycle is another problem for the conventional poly-silicon gate electrode, which leads to a shift of the threshold voltage.[1]

Repacking the conventional poly-silicon gate electrode with a metal gate electrode may potentially eliminate all of the limitations of poly-silicon. Using a metal gate electrode may also minimize the interaction between a high-k gate dielectric and the poly-Si. In addition, the use of a metal gate electrode may also avoid the high temperature poly-Si dopant activation annealing and hence lower the overall thermal budget of the CMOS fabrication flow.[96]

However, the integration of a metal gate electrode into the conventional CMOS fabrication process flow will also impose some serious manufacturing and reliability challenges because the metal electrodes should have excellent thermal/chemical stability and process compatibility with high k dielectrics and conventional CMOS processing sequences.[97] In this study, the TaN, MoN, and WN gate electrodes were thoroughly evaluated for the integration with the 2.5 nm ALD deposited HfO_2 high-k dielectric films.

1.6. Outline of the Dissertation

Chapter II will first introduce the equipment setups for the device fabrication process. Basic theory of sputtering deposition for high-k gate dielectric and metal gate electrodes will be reviewed in the second part of this chapter. The instrumentation and background of the physical and chemical characterization methods for high-k gate dielectric and metal gate electrodes will be discussed in the third part. Finally, the electrical measurement setups and methodology will be discussed.

Chapter III focuses on the Hf doping effects on the material and electrical properties of the 10 nm thick Hf-doped TaO_x films. Physical and electrical properties of hafnium (Hf)-doped tantalum oxide thin films were studied. The Hf doping effects on the high-k gate stack's structures, composition, thickness, dielectric constant, charges, and leakage current density were investigated. The Hf dopant affects not only the bulk film but also the interface layer material and electrical properties. Compared with the un-doped film, the lightly doped film exhibited improved dielectric properties, such as a higher dielectric constant, a lower fixed charge density, a large dielectric strength, and a lower leakage current. The post deposition annealing process, such as the temperature and the time, also

influence the high-k film's dielectric properties. In summary, the Hf-doped tantalum oxide film is a promising high-k gate dielectric material for future metal-oxide-semiconductor devices.

Chapter IV focuses on the ultra-thin lightly Hf-doped TaO_x films. Lightly Hf-doped tantalum oxide with an equivalent oxide thickness as low as 1.3 nm have been successfully prepared and studied. The doped film has a bulk layer dielectric constant greater than 28 and an interface layer dielectric constant greater than 8. The doping process changed the bulk and the interface layer structures as well as energy band gaps. The post-deposition annealing atmosphere revealed major impacts on material and electrical properties. The new high-k material is a viable gate dielectric film for future metal-oxide semiconductor transistors.

Chapter V discusses the effects of insertion of a TaN_x interface layer on the dielectric properties of the 10 nm thick Hf-doped TaO_x films. A 0.5 nm thick tantalum nitride (TaN_x) thin film was deposited between the Hf-doped TaO_x high dielectric constant (high-k) film and silicon wafer to hinder the formation of the SiOx interface layer during the subsequent high temperature annealing step. This interface contributes to the lower leakage current density, higher dielectric constant, improved dielectric breakdown strength, and larger charge trapping. The improvement is attributed to the formation of the TaO_xN_y interfacial layer, which was confirmed by secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS).

Chapter VI will study the TaN, MoN, and WN gate electrodes on the 2.5 nm ALD deposited HfO_2 high-k dielectric films. High-k gate dielectrics with appropriate gate electrodes are critical to future CMOS device performance. Hafnium oxide is one of the

most promising high-k materials. Since a traditional poly-Si gate has many practical limits for high-k gate electrode applications, e.g., undesired interface layer formation and dopant diffusion, other conductive materials are being actively sought for this purpose. Metal nitrides are possible candidates because they can be easily prepared by a sputtering method, are usually difficult to react with the adjacent oxide layer, and are good diffusion barriers for dopants. In this study, the authors investigated the influence of various types of metal nitride electrodes, i.e., molybdenum nitride (MoN), tungsten nitride (WN), and tantalum nitride (TaN), on electrical characteristics of MOS capacitors with hafnium oxide as the gate dielectric material. Dielectric properties, including equivalent oxide thickness, leakage current, flatband voltage, and interface state density were studied. Work functions of different gate electrodes were determined. Process parameters, such as the annealing temperatures were varied to investigate their influence on the capacitor's electrical properties. Physical properties of interface and bulk layers were characterized with EELS, HRTEM, SIMS, and XRD. Metal nitride electrode materials and process parameters drastically influenced dielectric properties.

Chapter VII summarizes all of the work in this study and draws the conclusions.

CHAPTER II

EXPERIMENTAL SETUP AND ANALYTICAL METHODS

2.1 Introduction

The first part of this chapter will briefly introduce the equipments used for the MOS capacitor fabrication. Basic theory related to the plasma and RF sputtering will be reviewed in the second part. The third part of the chapter will focus on physical and chemical characterizations of high-k films and metal gate electrodes. The instrumentation and theories of ellipersometer, time-of-flight secondary ion mass spectroscopy (TOF-SIMS), electron spectroscopy for chemical analysis (ESCA), X-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM) will also be reviewed. The last part of this chapter will introduce the electrical characterization in this study. Measurement setup and methodology used to extract the important electrical properties of high-k films and metal gate electrodes will be discussed.

2.2 Experimental Equipments for MOS Capacitors Fabrication

2.2.1. RF Reactive Sputtering Machine

All of the high-k films were deposited by a magnetron radio frequency (13.56MHz) reactive sputtering machine. Figure 11 is a schematic of the sputtering machine. This sputtering machine is equipped with three sputtering guns, two RF matching network boxes, two RF generators, one DC generator, and two mass flow controllers (MFC) to process gas. A 2-inch diameter metal target can be used for each sputtering gun. Two metal targets e.g., Ta and Hf, can be used simultaneously to deposit Hf-doped TaO_x high-k films in an Ar/O_2 mixture ambient. The compositions of the as-deposited films were

varied by adjusting the sputtering powers for each target. The high-k film thickness was controlled by deposition time. Al gate electrode and backside Al of the MOS capacitor were deposited by a DC sputtering deposition in a pure Ar ambient with an Al metal target. The metal nitride gate electrode, e.g., TaN, MoN, or WN was deposited by a RF reactive sputtering in an Ar/N_2 mixture ambient with a Ta, Mo, or W metal target, respectively. A base pressure of 4×10^{-7} Torr can be reached with a turbomolecular pump and a mechanic backing pump. During the high-k film deposition, the working pressure in the sputtering chamber was fixed at 5×10^{-3} Torr. The substrate and chamber walls were kept at room temperature during the sputtering deposition.

2.2.2. Annealing Tube Furnace

After sputtering deposition of high-k gate dielectric films, as-deposited films will go through a post deposition annealing (PDA) to remove the defects caused by the sputtering process. A tube furnace was used for this purpose. Figure 12 is the schematic of the annealing tube furnace in our lab. N_2 and O_2 gases were used for the PDA of high-k as-deposited films. Post metallization annealing (PMA) of the Al gate electrode and back side Al can also be performed in this tube furnace with a forming gas (N_2 90% /H_2 10%) ambient. A 300°C FG annealing of a MOS capacitor may reduce the high-k/Si interface state density and improve the Ohmic contact for the backside Al. A maximum 1000°C can be reached for this heating system. A base pressure of 4×10^{-2} Torr can be achieved with a roughing pump. The maximum flow rate for the process gases was 2000sccm.

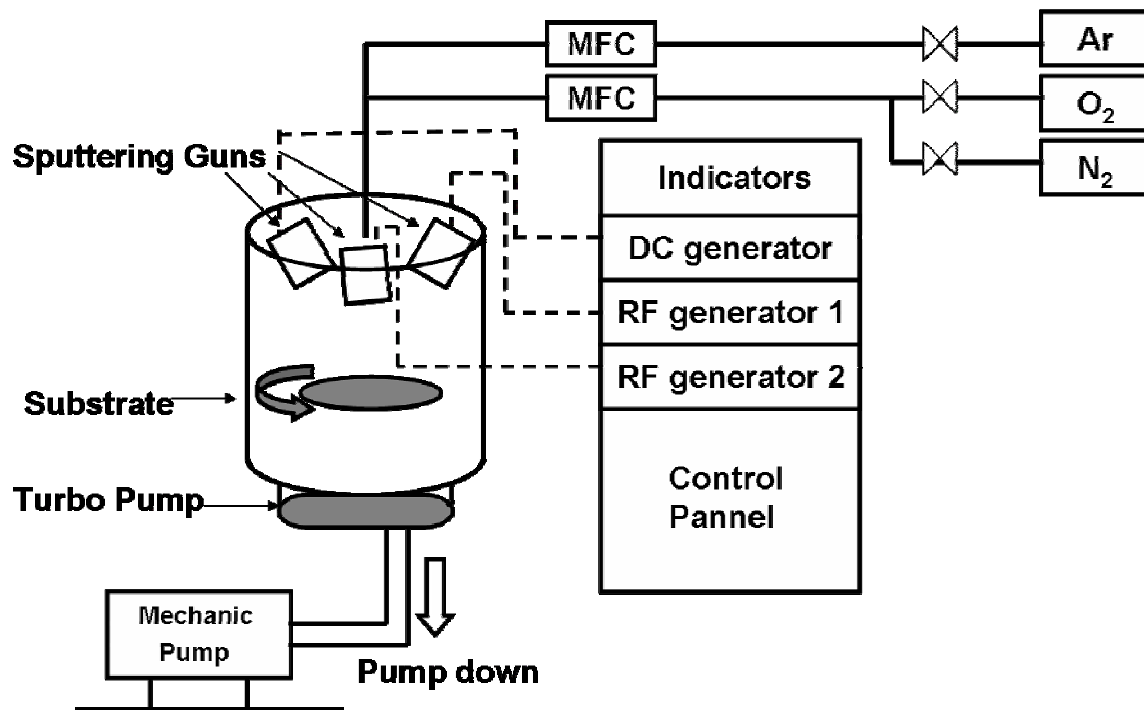


Figure 11 Schematic of the sputtering machine.

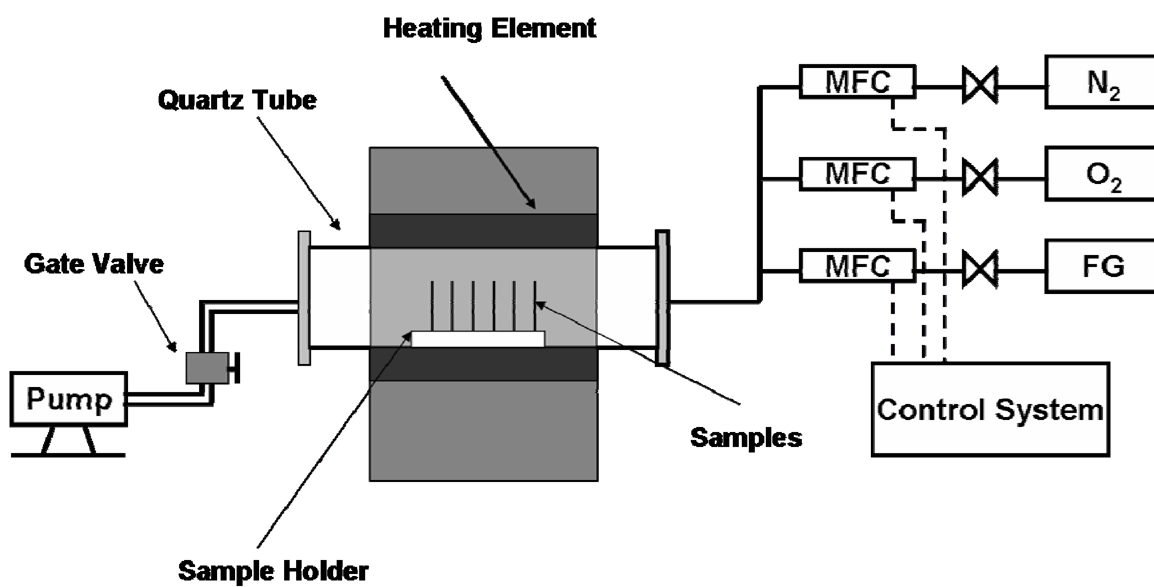


Figure 12 Schematic of the annealing tube furnace.

2.2.3. Load-Lock Chamber and Heating Chamber

A load-lock chamber was attached to the sputtering chamber to reduce the pumping down time. The advantage of the load-lock chamber is its small volume and therefore it can be pumped down to a moderately high vacuum for a short time. The bare Si wafer can be loaded on the sample holder of the transfer arm. It would take about 15 minutes for the load-lock chamber to reach a vacuum of 5×10^{-5} Torr. Then the samples can be transferred into the main sputtering chamber through the gate valve between the load-lock chamber and the main sputtering chamber without breaking the pressure of the main sputtering chamber. After the sample holder was transferred to the substrate, the transfer arm would pull back into the load-lock chamber and then the gate valve could be closed. After the sputtering deposition of the high-k films, the samples could be taken back into the load-lock chamber for further treatment. Using the load-lock chamber can not only improve the throughput of our fabrication process but also prevent the contamination of the main sputtering chamber from exposure to the air during the loading and unloading steps.

A stainless steel heating chamber was designed and built. An ultra high vacuum ($\sim1\times10^{-8}$ Torr) may be reached by this heating chamber. A resistive button substrate heater was used as the heating element in the heating chamber. This substrate heater can provide a much higher temperature ramp rate (~100°C/min) than the annealing tube furnace. Three process gases (N_2, O_2 and FG) were connected to the heating chamber. The gas flow rates of the process gases were controlled via metering valves. The high vacuum heating chamber can provide an ultra clean annealing ambient. High ramp rate

substrate heaters may minimize the thermal budget of the annealing process by reducing the temperature ramp up time.

This heating chamber was connected to a load-lock chamber later to form a multi-chamber reaction system as illustrated in figure 13. With such a multi-chamber reaction system, a set of MOS capacitor fabrication procedures may be in-situ accomplished. For example, once a HF cleaned Si bare wafer was loaded into the load-lock chamber, the processing steps, such as high-k deposition, PDA, metal gate deposition, and PMA can be performed without breaking vacuum by transferring the sample back and forth through the load-lock chamber. Reproducible physical and electrical characteristics of the MOS capacitors may be expected by minimizing the moisture and contamination due to exposure to the air.

2.2.4 Photolithography and Shadow Masks

Two methods were used for the metal gate electrode area patterning: photolithography and shadow masks.

Photolithography is the most common processing step in the mass production of CMOS fabrication. It can transfer the patterns of the photomasks to the underlying Si wafer. For a typical integrated circuit fabrication process, more than twenty complete lithographic steps are required on each wafer. For more complex microelectronic configurations, about thirty to forty complete sequences of lithography operations will be necessary. Thus, photolithography processes play a crucial role in the microelectronic fabrication process.

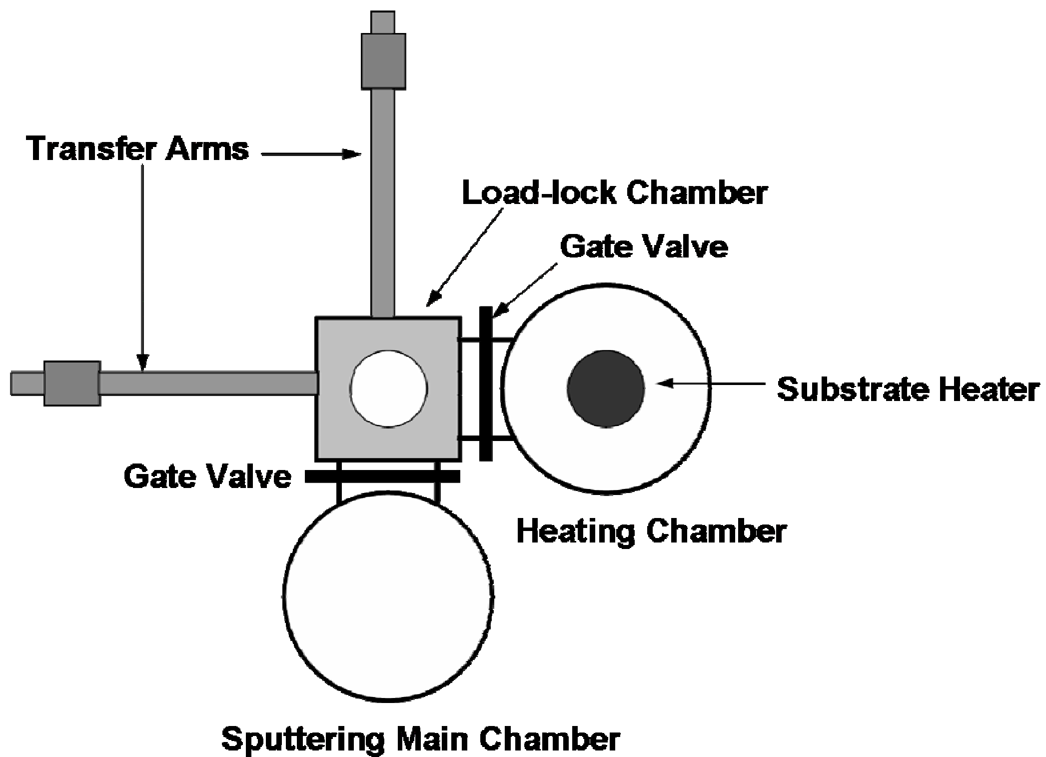


Figure 13 Schematic of the multi-chamber reaction system.

In this work, only one mask was needed to fabricate a MOS capacitor with a high-k gate dielectric layer. Figure 14 is the fabrication process flow chart to define the metal gate electrode of the MOS capacitor. After the metal gate deposition, the positive photo resist (AZ 1512 or AZ 3312 Clariant, Somerville, NJ) was spin coated on the metal surface at 4000 rpm. After 1 minute of 90°C soft baking on a heat plate, the samples were then exposed to UV light for 15 seconds. A Quintel Q4000 series mask contact aligner (Quintel Corporation, San Jose, CA) was used for the UV exposure. It is a top and bottom side contact lithography printer with the video-view split field microscope used for fine line lithography do to 1 micron or better. The samples were developed in a 66% AZ MIF 300 developer (Clariant, Somerville, NJ) solution for 90 seconds to remove the UV-exposed photo resist to get a pattern. After 3 minutes of 120°C hard baking on a heat plate, metal film on the open area was then etched away by wet etchant solutions or reactive ion etching (RIE). At last, the remaining photo resist was stripped by an acetone solution followed by deionized (DI) water.

Meanwhile, the metal gate electrode definition can also be accomplished by using a shadow mask. The shadow mask is a metal sheet with many small holes. The metal gate electrode area can be easily defined by a direct deposition through the shadow mask put on the Si wafer. This method is very simple and widely used in the worldwide high-k gate dielectric and metal gate electrode research to form a MOS capacitor.

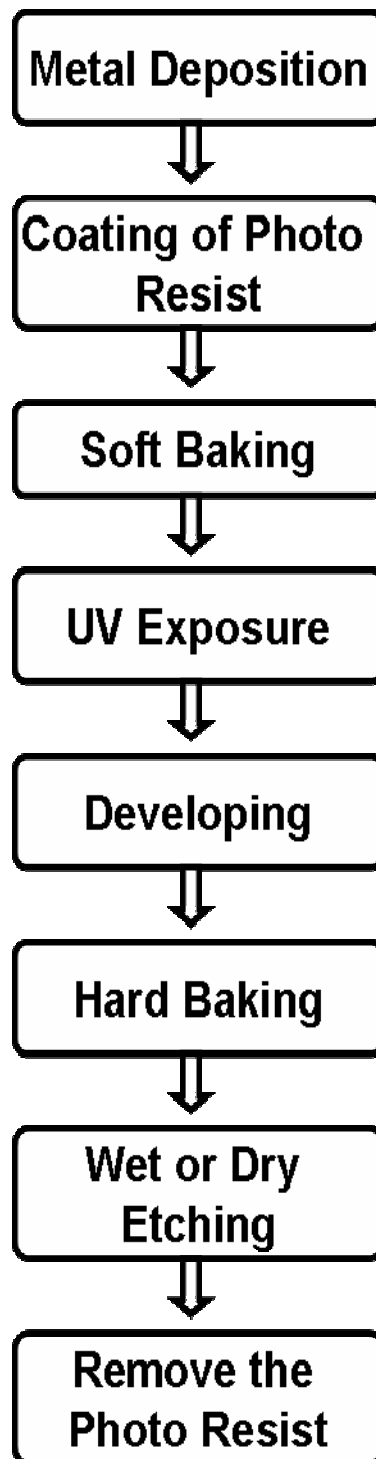


Figure 14 The process flow chart to define the metal gate electrode of MOS capacitor.

The advantage of using a shadow mask is its easy fabrication procedure and less environmental concern by avoiding many chemicals used in traditional photolithography and wet/dry etching processes. In addition, the wet etchants for many new metal gate materials are still unknown and an RIE dry etching process may generate plasma damages to the metal gate/high-k gate stack structures, which may introduce some uncertain factors in determining the film characteristics. However, the shadow mask cannot be used in the traditional CMOS fabrication process because it doesn't have capability for alignment. Therefore, it can only be used in the research stage.

There are some other disadvantages related to using a shadow mask. The metal sheet of the shadow mask must be very thin to minimize the shadow effect during the film deposition. But, a very thin metal sheet will easily wrap up in daily handling. A non-uniformity of gate electrode area may be expected due to the shadow effect and inherent variance of the hole area of the shadow masks. A measurement of each gate electrode area before the electrical characterization will be necessary to obtain an accurate result. This gate area measurement can be performed with a microscope or a Dektak 3 Stylus Profilometer.

In this study, gate electrode definition methods were chosen depending on the gate electrode materials. Photolithography and wet etching were used to define the Al gate electrode. Shadow masks were used to define the metal nitride gate electrodes due to the difficulty in finding a proper wet etchant solution.

2.3 Plasma Thin Film Deposition

2.3.1. Plasma Processing Fundamental

Plasma processing has become one of the most important and common chemical processes in the microelectronics industry. It is involved in almost 50% of traditional CMOS integrated circuit fabrication processes. Its applications include sputtering, plasma enhanced chemical vapor deposition (PECVD), plasma etching, ashing, implantation, surface cleaning/modification, and other rapidly growing areas. The plasma machines account for a major portion of equipment costs in a state-of-the-art semiconductor fab.

Plasma is the most common form of matter, accounting for more than 99% of the visible universe. When a matter is heated beyond its gaseous state, some outer shells of electrons will separate from the atoms. Then the matter will become a mixture of positive ions and free electrons, which is electrically neutral. Not all atoms have to be ionized to form plasma. Weakly ionized plasma discharges are used in typical microelectronic processing. Only a very small portion of atoms are excited or ionized in plasma processing. For example, the radicals only account for 1.0% of the total plasma, and the total charged species are usually less than 0.01%.[98] The rest of the gas remains as neutral atoms or molecules. Therefore, plasma is composed of free charged particles, radicals, atoms, and molecules and fields that exhibit collective effects.

In plasma processing, plasma is usually generated and sustained by a DC or RF electrical filed. When electrons from an applied electric field randomly collide with molecules, if the energy of the electrons is high enough to dissociate gas molecules, the electron energy can be transferred to molecules by elastic collisions. Thus activated radicals, ions, and neutrals can be produced by the elastic collisions. An optional

magnetic field can be applied to confine the electrons in the plasma in a desired region to improve the efficiency. The plasma can be sustained as long as the electric field is present.[98-99]

A simple plasma reactor consists of two parallel-plate electrodes in a chamber under vacuum. Figure 15 is the schematic of a typical electrically driven plasma diagram in a parallel-plate electrode.[98] When the plasma is driven by an ac signal, the electrons will move with an electrical field caused by a RF driving voltage and collide with molecules to generate reactive species in the central region. In the central region, electron flux is the same as ion flux ($n_e = n_i$). The central region is quasineutral and filled with reactive species. It also produces lights of various wavelengths, which can be utilized for the analysis of the plasma state. In addition, there is no potential drop across this region; therefore the bulk plasma is considered a good conductor.

At a high frequency RF excitation, the slow ions near the electrode cannot follow the voltage change because they are big and sluggish. However, since electrons are light and energetic, they diffuse quickly and are quickly recombined at the electrode. Thus positive charge layers ($n_i >> n_e$) form near the electrodes. The positive charge layer is called sheath, which is dark and does not emit light. The net positive charge within the sheaths leads to sharp potential drops between the bulk plasma and two electrodes, and thus this positive charge layer is considered as a bad conductor. Since the positive ions are accelerated through the sheath region, the sharp potential drops are responsible for the ion bombardment energy on the cathode electrode. The advantage of the plasma processing lies in the fact that the ionized gas has an electron temperature of above 10,000 K, thus

the thin film deposition or dry etching processing can be carried out at a low thermal temperature. In this way, some undesired

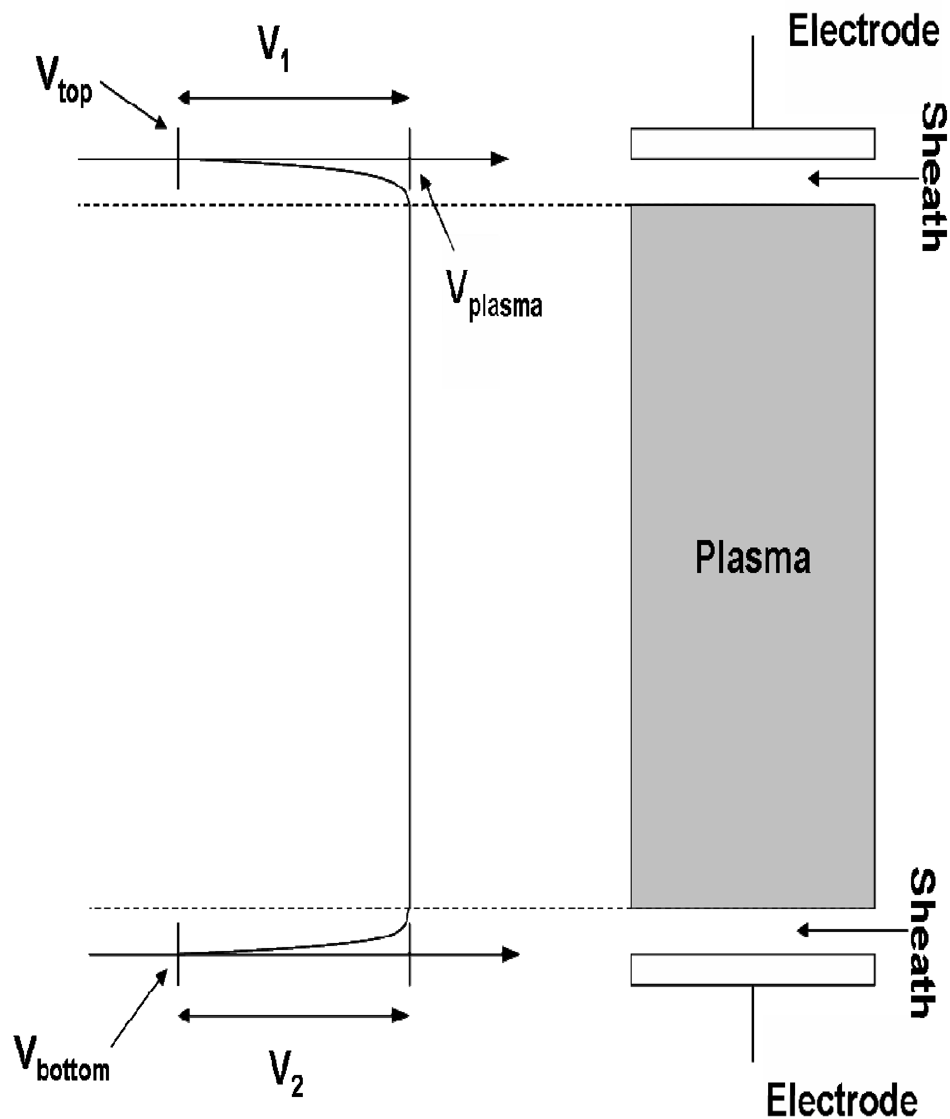


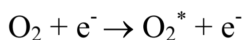
Figure 15 Schematic of an electrically driven plasma state and dc voltage profile in parallel plate electrodes. (After reference 98)

reaction or contamination related to high temperature treatment may be eliminated or minimized. The primary disadvantage of the plasma processing is its tendency to cause damage and defects due to the high electric field present during the deposition and etching processes.

2.3.2. Plasma Chemistry

Plasma chemistry deals with the behavior of reactions in a weakly ionized gas composed of ions, electrons, and free radicals. Reactive species, such as ions, electrons, radicals, and atoms are produced in the plasma by collisions between electrons and atoms or molecules. For example, the following electron-gas and gas-gas reactions may occur in O_2 plasma.[100]

1) Molecular excitation

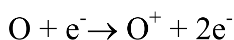


$O_2 + e^- \rightarrow O_2^* + e^-$

2) Molecular dissociation

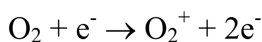
$O_2 + e^- \rightarrow 2O + e^-$

3) Atomic ionization



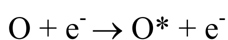
$O + e^- \rightarrow O^+ + 2e^-$

4) Molecular ionization



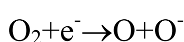
$O_2 + e^- \rightarrow O_2^+ + 2e^-$

5) Atomic excitation



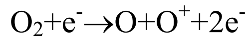
$O + e^- \rightarrow O^* + e^-$

6) Dissociative attachment



$O_2 + e^- \rightarrow O + O^-$

7) Dissociative ionization



$O_2 + e^- \rightarrow O + O^+ + 2e^-$

Where, O^* and O_2^* are the excited species. The reactive species generated in O_2 plasma are O, O_2^*, O^+, O^-, and O_2^+. The major neutral species are atomic O and molecular O_2. The main ions are O^+ and O_2^+.[21, 22 of hyunho] The above reactions are simplified reaction conduct models. The exact mechanism of the plasma chemistry is very complex and is still not clear.

2.3.3. DC Sputtering

DC sputtering was used to deposit Al gate electrodes and backside Al in a pure Ar ambient in this study. Figure 16 is the schematic of a DC sputtering system and DC exited glow discharge. The electrons flow between the electrodes with a DC electrical field. These electrons collide with the Ar gas molecules to ionize the Ar to Ar^+. Then both Ar^+ and electrons will accelerate under the electrical field to enter into collisions with more neutral Ar molecules, which will lead to an avalanche multiplication effect. The electrical field density, Ar gas pressure, and the electrode's distance will determine the magnitude of the avalanche multiplication effect. Figure 16 (a) shows the Ar^+ ion moves toward the cathode and bombards the target on the cathode, knocking out the surface material by momentum transfer. The secondary electrons emitted from the target make more ionizing collisions with the neutral Ar molecules, sustaining the glow discharge.

Figure 16 (b) shows the nature of a DC glow discharge.[99] Crook's dark space is the most important region because almost all of the voltage drops in the vicinity of the

cathode. Both Ar^+ ions and electrons are accelerated in the crook's dark space, resulting in a high-energy Ar^+ ion bombardment to the target. A dark space also exits near the anode, but it is very thin and it is a relatively field-free region. The bright negative glow fills the most space between the two electrodes. The positive column and the Faraday dark space are not required for the DC discharge for normal operation. When two electrodes get close, the Crook's dark space and negative glow will not be affected, but the positive column and the Faraday dark space will shrink. The basic principle of the DC glow discharge may also be extended to the RF excited glow discharge.

In addition, the polarity of the DC sputtering system can be reversed to etch the substrate prior to film deposition, which is known as the back-sputtering process. The back-sputtering process has the capability for in situ cleaning of the substrate. For example, this technique can be used to etch away the native oxide on the Si substrate before the high-k deposition. However, since this back-sputtering process may damage the crystalline structure of the Si substrate and induce an undesired interface layer, only dilute HF solution was used to remove the native oxide on the Si substrate.

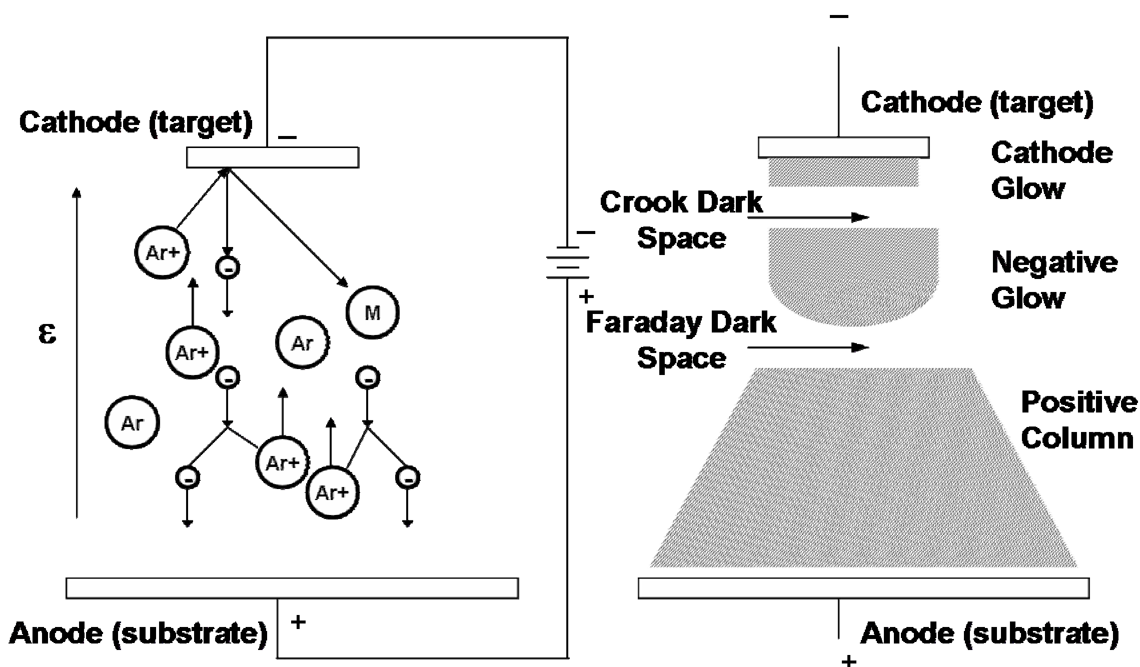


Figure 16 Schematic of (a) DC sputtering system configuration and (b) DC exited glow discharge.[99]

2.3.4. RF Reactive Sputtering

DC sputtering is mainly used to deposit conducting targets. It is not appropriate for insulating materials because the positive charges will build up on the cathode (target). In order to deposit insulator like high-k gate dielectrics, RF sputtering is usually used. In the RF sputtering technology, a high frequency (13.56 MHz) alternating voltage power supply is used, so that the charge build-up on the sputtering target can be avoided because ions and electrons alternately bombard the target. Since the RF sputtering makes more efficient use of the electron impact ionization, a low working pressure (~1 mTorr) may be

used, which may reduce the scattering of material sputtered from the target and improve the sputtering yield.

Figure 17 is the schematic of a RF sputtering system configuration. For a RF sputtering system with a blocking capacitor, the potential drop near the electrode depends on the electrode gate area. For example, the potential drops at electrode 1, V1, and at electrode 2, V2 are inversely related to the surface areas of A_1 and A_2, as below:

$$\left(\frac{\mathbf{V_1}}{\mathbf{V_2}}\right) = \left(\frac{\mathbf{A_2}}{\mathbf{A_1}}\right)^{\mathbf{N}} \quad [7]$$

where n = 4 for the ideal system. Experimental results suggest the typical values for N are between 1 and 2.[98] Therefore, in order to minimize the sputtering of substrates and chamber walls during the alternating RF signals, the target is much smaller than the substrate and chamber wall to ensure a large potential drop and electrical field near the sputtering targets.

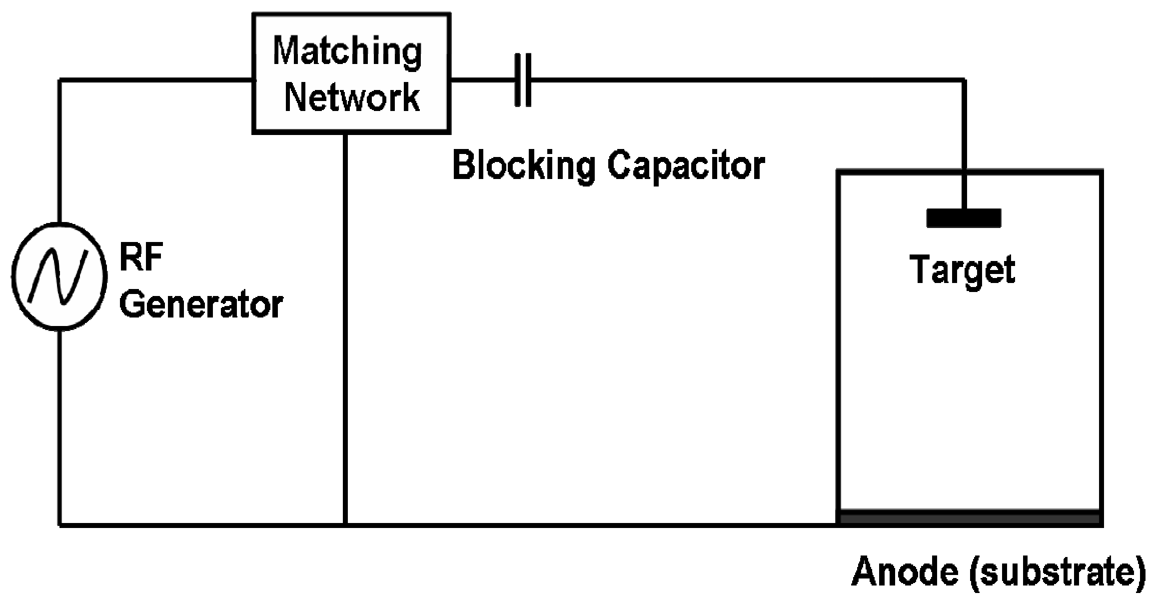


Figure 17 Schematic of a typical RF sputtering system configuration.[99]

For reactive sputtering, a second process gas, i.e., O_2 or N_2, in addition to Ar has to be introduced into the chamber, whose dissociation products chemically react with the target. RF reactive sputtering is widely used to deposit oxide and nitride, as well as carbide and silicide. Although, oxide and nitride can be directly used as sputtering targets, they are not mechanically robust enough to handle a high-power flux without cracking; hence metal targets are commonly used in reactive sputtering for high deposition rate and controllable film stoichiometry. In this study, both high-k gate dielectric layers and metal nitride gate electrodes are deposited by a RF reactive sputtering method using metallic targets in an Ar/O_2 and Ar/N_2 ambient, respectively.

In RF reactive sputtering, chemical reactions may occur at both target and substrates depending on the operation conditions. There are two operation modes for reactive sputtering using metal targets: metallic mode and cover mode. If high Ar flux and low reactive gas flux are used, the target remains metallic during the deposition, which is called metallic mode. If low Ar flux and high reactive gas flux are used, the target is covered by compound during the deposition, which is called cover mode. A higher deposition rate can be achieved for the metallic mode operation. Fixing the Ar flux and varying the reactive gas flux, a hysteresis can be observed for transitions between the covered modes to metallic modes. For example, the transition flux for decreasing the flux to pass from the covered to metallic mode is lower than the transition flux for increasing the flux to pass from the metallic to covered mode. A switch between high and low deposition rate mode will occur at the hysteresis region for a sputtering machine in the absence of a feedback control system, which is undesirable in the practical processing operation. [98]

In this study, the Hf-doped TaO_x high-k gate dielectric films were deposited in cover mode RF reactive sputtering operation to ensure better stoichiometry and film uniformity; the metal nitride gate electrodes, such as TaN, MoN, and WN, were deposited in metallic mode RF reactive sputtering operation for a high deposition rate.

2.4 Physical and Chemical Characterization

The high-k film thickness and refractive index (RI) were measured with a single wavelength (632.8nm) ellipsometer (Rudolph i1000). The physical thicknesses of various metal gate electrodes, such as Al, TaN, MoN, and WN, were estimated with a profilometer (Veeco Dektak stylus). Other physical and chemical properties of Hf-doped TaO_x high-k film and various metal gate electrodes were probed with various advanced analytical tools. A time of flight secondary ion mass spectroscopy (ToF-SIMS) was used to determine the element depth profile. Electron spectroscopy for chemical analysis (ESCA, Kratos Axis His 165), or known as X-ray photoelectron spectroscopy (XPS), was performed to analyze the chemical bonding structure and elemental composition in the high-k stack structure. X-ray diffractometry (XRD, Bruker D8) was used to investigate the crystallinity of the metal gate electrodes. High-resolution transmission electron microscopy (HRTEM) was used to study the interface formation. Theoretical background and instrumentation of these techniques will be briefly reviewed in the following sections.

2.4.1. Ellipsometer

An ellipsometer can be used to measure the refractive index and the thickness of semi-transparent thin films. It can be used to measure a film with thickness ranging from

2 nm to several micrometers. The principal of this instrument is to measure and simulate the changes in the polarization state of a light beam reflected from transparent layers, such as a dielectric layer. When a light transmits through a dielectric layer, the phase of the incoming wave will depend on the refractive index of the dielectric material. Figure 18 is the schematic of the ellipersometer equipment and its reflection model.

As shown in figure 18, an ellipsometer is made up of a laser source (632.8 nm He/Ne laser for Rudolph i1000), a polarizer, a quarter wave plate, a detector, and an analyzer.[101] The quarter wave plate can provide a state of polarization which can be varied from linearly polarized light to elliptically polarized light by varying the angle of the polarizer. After the layer beam is reflected from the high-k dielectric layer, it will be analyzed with the analyzer. The detail calculation procedures and principal of this instrument can be found elsewhere.[101] It is noteworthy to point out that using an ellipsometer to measure the high-k film thickness is a fast and nondestructive method, which is its major advantage. The measured film thickness can be confirmed with the HRTEM result.

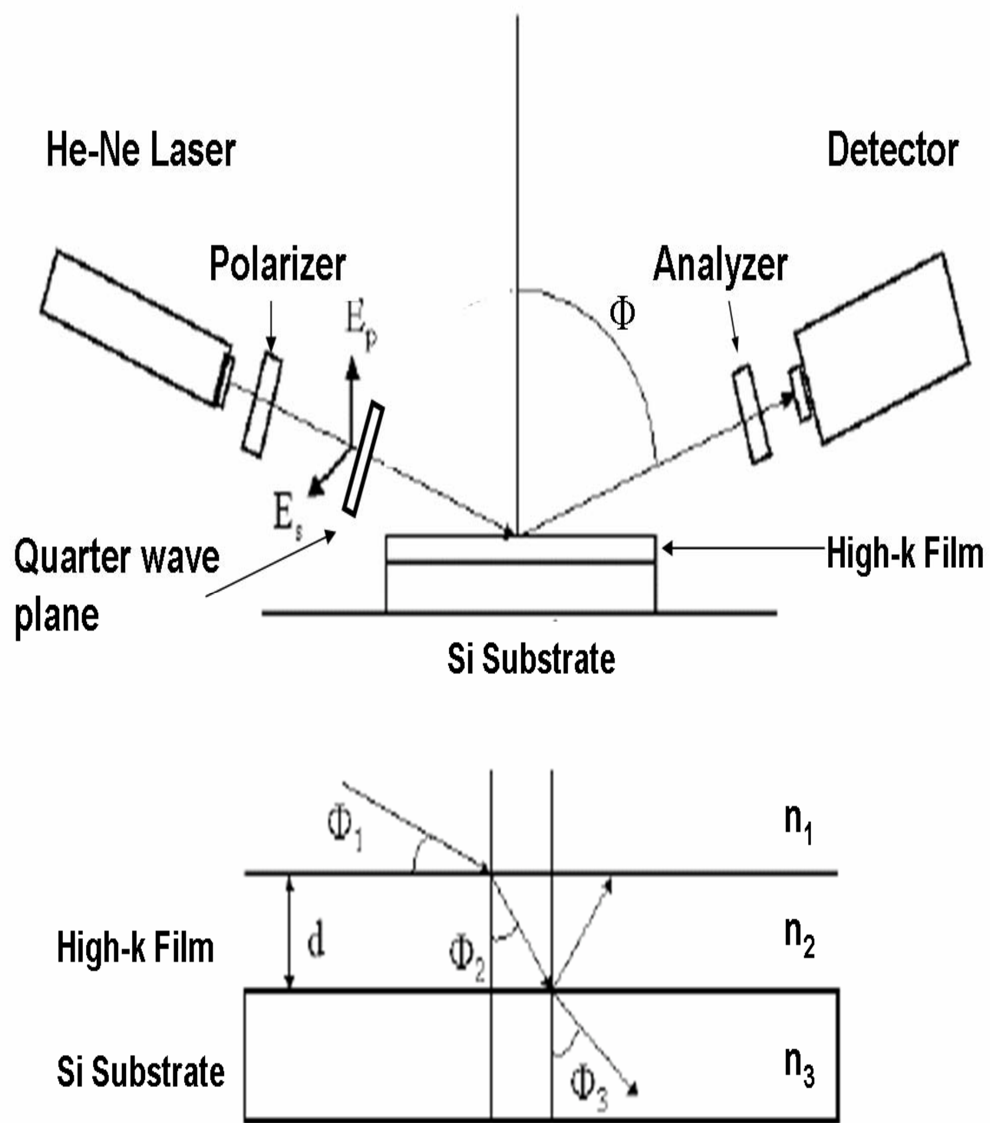


Figure 18 Schematic of an ellipsometer system and light reflection model. (After reference 101)

2.4.2. Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS)

Time of flight secondary ion mass spectrometry (ToF-SIMS) is a very powerful and versatile analytical technique for semiconductor characterization. It is the most sensitive beam technique, with the detection limits for element even in the ppm range (10^{14}-10^{15} cm^{-3}). The lateral resolution of SIMS is typically between 0.5 to 100 μm and the depth resolution can be as small as 5 nm. It is capable of detecting all elements as well as isotopes and molecular species.

Figure 19 is a schematic illustration of the ToF-SIMS system.[104] Primary ions, such as Ar+, O_2^+, Cs^+, or Ga^+ with energy of 5-20 keV, bombard the sample surface to cause the secondary elemental or cluster ions to emit from the surface. The secondary ions then fly toward the mass spectrometer with the same kinetic energy. Ions with lower mass have higher flight velocity than those with higher mass. Thus they will reach the secondary-ion detector earlier. As a result, the mass separation is obtained in the flight time from the sample surface to the detector. The flight time (t_f) of various ions are measured and related to the mass to charge (m/q) ratio as follows:

$$\frac{m}{q} = \frac{2Vt_f^{\,2}}{L^2} \qquad [8]$$

where L is the flight distance from the sample to the detector, and V is the potential drop. Since the m/q is solely a function of the t_f, fragments with different mass can be identified.

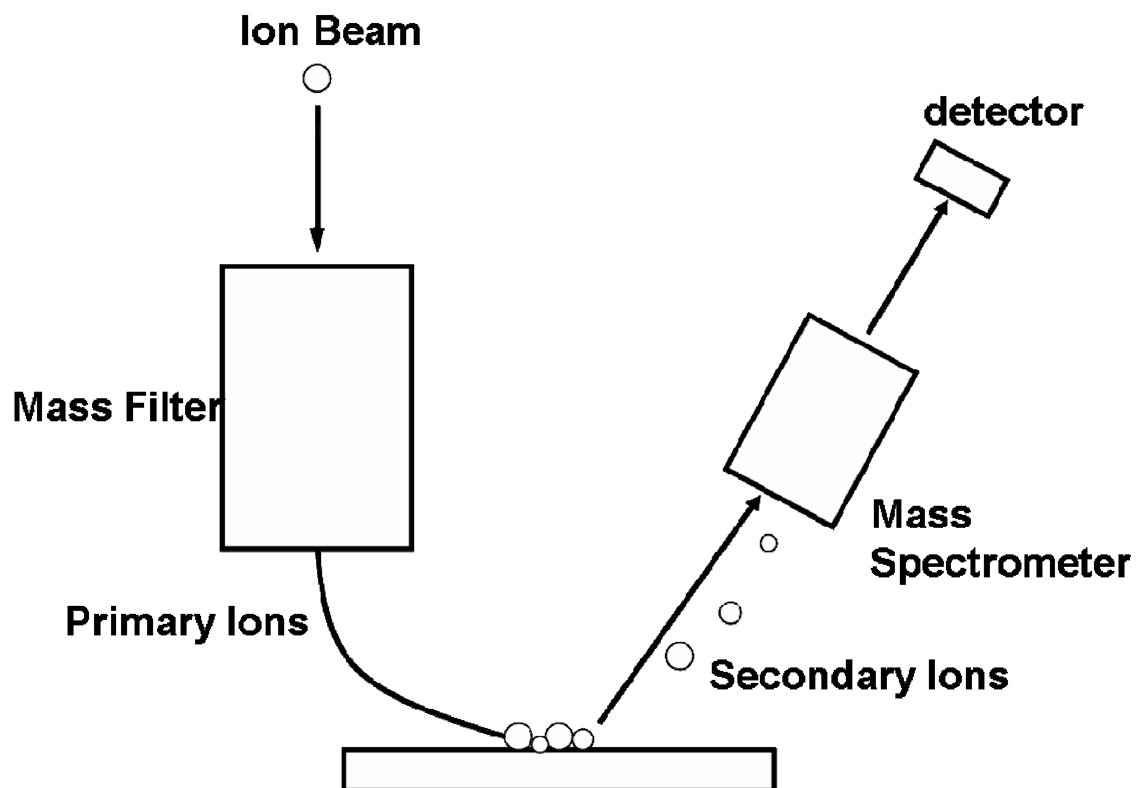


Figure 19 ToF-SIMS system schematic.[104]

SIMS can provide quantitative depth profiling information of various elements or ion clusters by converting secondary ion yield to density. Many factors, such as sputter yield, ionization efficiency, atomic fraction of ions and primary ion beam current, have been known for the conversion of signal intensity to density. However, some of these factors are poorly known and some assumptions have to be made for calculation, which present a formidable challenge for a successful quantitative SIMS analysis. Accurate quantitative SIMS can only be successfully used to measure the ion-implanted dopants depth profiling by using standards with composition and matrices identical or similar to the unknown samples. For current research of high-k gate dielectrics and metal gates, qualitative SIMS measurements are widely used due to the absence of standards.

In this study, ToF-SIMS was used to investigate the elemental depth profile information of various metal gate electrodes and high-k gate dielectric films. Other information including the interface composition and impurity level can also be studied by this technique. The time to sputtering depth conversion was made by measuring the sputtering crater depth afterwards. However, interpretation of the depth profiling information should be done very carefully due to some inherent weaknesses of this technique, including matrix effects, molecular interference, and depth intermixing as a result of the sputtering process.

2.4.3. X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS), also commonly known as Electron Spectroscopy for Chemical Analysis (ESCA), is a most widely used analysis technique to investigate the chemical bonding structure and composition of the constituent elements.

All other elements in the periodic table can be analyzed by XPS, except for hydrogen and helium.

Figure 20 shows the electronic process of XPS electron emission and a XPS measurement schematic. When the sample surface is irradiated with an X-ray, the electrons of the core levels can be ejected from the sample. The electrons can be emitted from all of the levels as long as the photon energy is larger than the electron binding energy, which is known as the photoelectron effect. The kinetic energy E_K of the electron is measured and related to the binding energy E_B as in the following,

$$E_B = h\nu - E_K - \Phi \qquad [9]$$

where $h\upsilon$ is the primary X-ray energy and Φ is the work function of the spectrometer. Monochromatic Al ($K\alpha$ =1486.6 eV) and Mg ($K\alpha$=1256.6eV) X-ray sources are commonly used in the XPS instrument to achieve narrow X-ray line widths. A work function between 3 to 4 eV is widely used for spectrometer.

The binding energy of an element is mainly affected by its chemical bonding environment and thus the chemical state of the element can be determined. The primary application of the XPS is to identify the compound from the binding energy shift as a result of chemical structure changes of the sample atoms. The compounds and elements are identified from the binding energy peaks of the XPS peaks location. The mass and atomic ratios of different elements are calculated for the peak heights and area of the XPS spectrum.

The lateral resolution of XPS analysis is about 1 cm^2 due to the difficulty in focusing the X-ray. Efforts have been made to reduce this area and a spot size of 10 μm can be analyzed with the state-of-the-art instrument. Another disadvantage of the XPS lies in its

relatively low sensitivity. A minimum solid density of 5×10^{19} cm^{-3} or 0.1% atomic concentration will be required for a compound or element to be detected.

In this study, an Axis Ultra XPS instrument (Kratos Analytical Inc. Chestnut Ridge, NY) equipped with a monochromatic Al Kα (1486.6 eV) X-ray source was used to investigate the chemical bonding state of various Hf-doped TaO_x high-k films and their interface layers. The carbon C 1s emission at 284.6 eV was used as a reference to correct the charging effect.

Since XPS is a surface sensitive analytical technique, the detection depth is governed by the escape electron mean free path, which is between 0.5 to 5.0nm. For samples thicker than this mean free path, depth profiling by inert ion beam sputtering may be used to acquire the chemical state information at the high-k/ Si interface. This technique was successful in identifying the chemical structure of the TaN interface after a high temperature O_2 PDA. For samples with thicknesses below 5.0 nm, angle resolved XPS (ARXPS) can be used to differentiate the chemical bonding states between bulk high-k film and high-k/Si interface. By tilting the sample position, the detection depth of XPS analysis will vary with the angle between the sample surface and the trajectory of the emitted photo-electron.

In addition, the O1s energy loss spectroscopy can also be extracted from the XPS spectra. The energy band gap (E_g) of the doped and un-doped metal oxide can be calculated from the O1s energy loss spectroscopy. [87,102] Since the valence band offset (ΔE_v) of metal oxide to Si can also be calculated from the valence band spectra of the XPS analysis, the conduction band offset (ΔE_c) can be calculated as following, [103]

$$\Delta E_c = E_g - \Delta E_v - 1.1 \qquad [10]$$

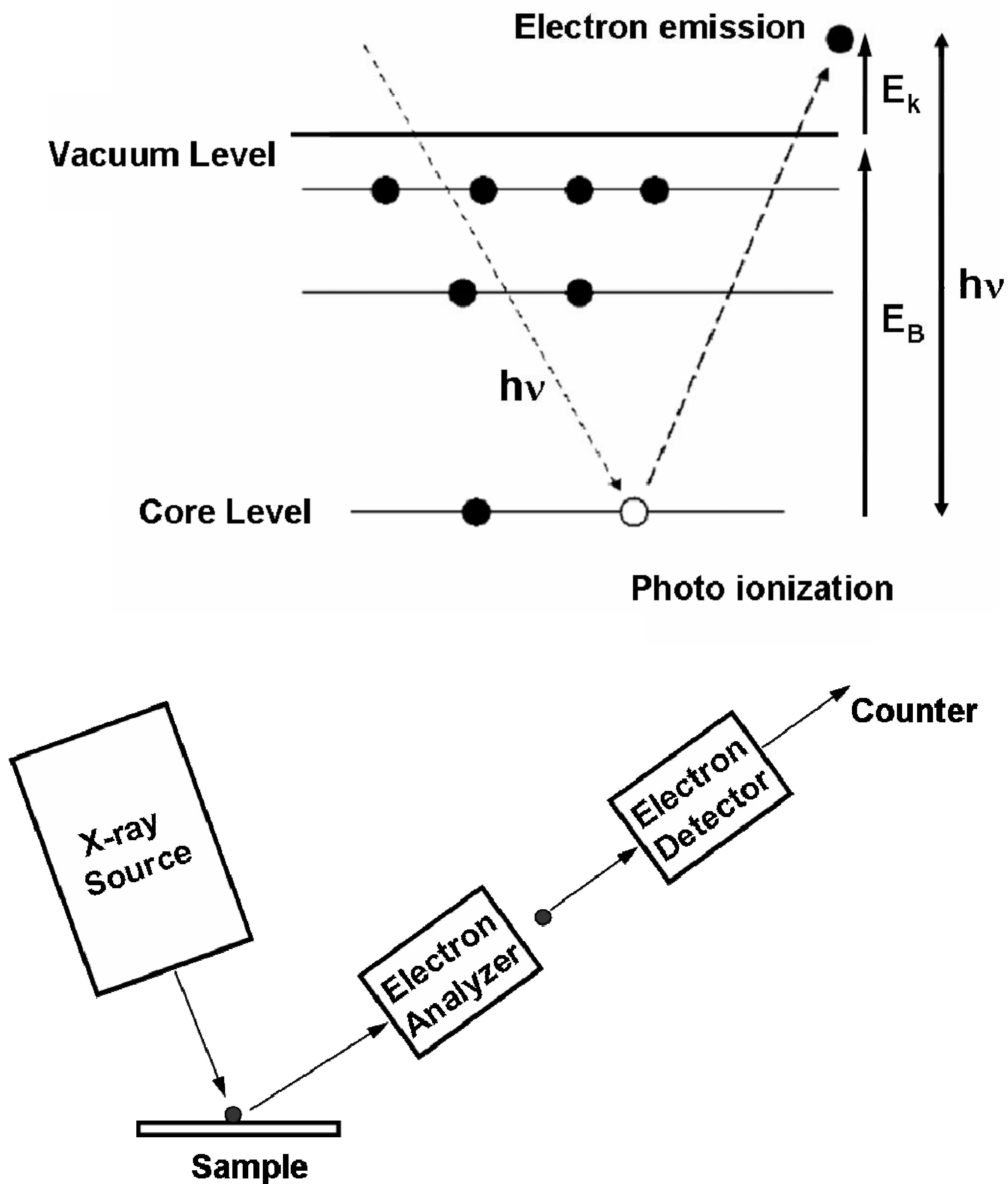


Figure 20 The electronic process of XPS electron emission and a XPS measurement schematic.[104]

2.4.4. High Resolution Transmission Electron Microscopy (HRTEM)

High Resolution Transmission Electron Microscopy (HRTEM) is a very important analytical tool used to study atomic-size level structure information. It has been widely used in the semiconductor characterization to analyze the interfaces, including oxide-semiconductors, metal-semiconductors, and semiconductor-semiconductors. The primary advantage of the HRTEM is its extremely high resolution (~0.15nm), which is mainly attributed to the short wave length of the electron. However, HRTEM suffers a limited depth resolution and thus requires a sample thickness less than 100nm to be transplanted to electrons. The sample preparation for HRTEM analysis is a tedious and time-consuming process, which makes this technique very slow and expensive.

Figure 21 is a schematic of a HRTEM system.[104] Electrons from an electron gun are accelerated to about 100-400 kV and then focused on the sample by two condenser lenses. A diffraction pattern in the back focal plane and a magnified image in the image plane is formed by the transmitted and forward scattered electrons. The structural information can be obtained with the formation of this diffraction pattern. There are three TEM imaging modes: bright-field, dark-field, and high-resolution. The TEM image contrast mainly depends on the scattering and diffraction of electrons. Transmitted electrons form bright-field images and diffracted beams form dark-field images. Parameters such as mass contrast, thickness contrast, diffraction contrast, and phase contrast will affect the image contrast.[104]

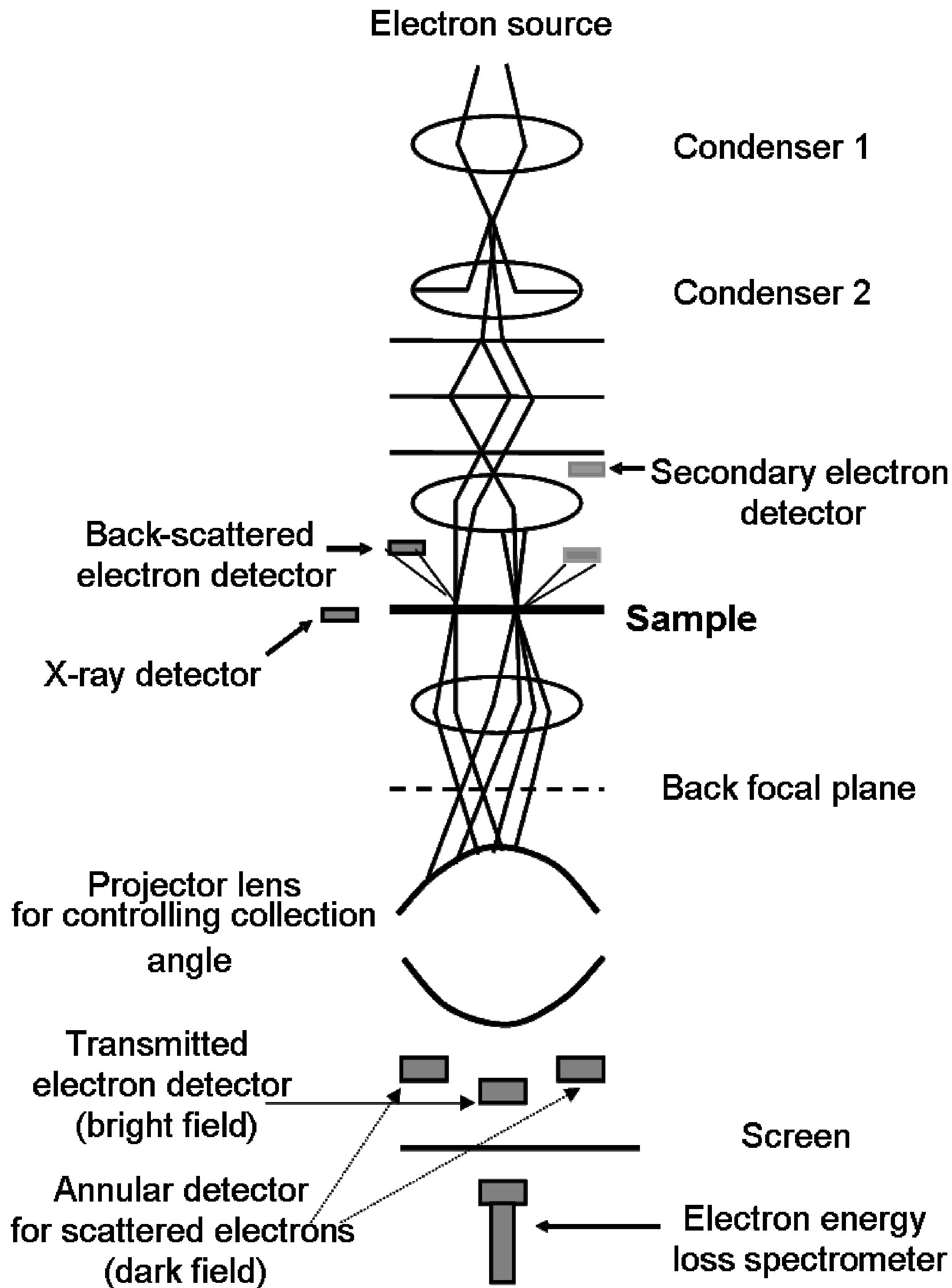


Figure 21 Schematic of a HRTEM system. (After reference 104)

Electron energy loss spectroscopy (EELS) is usually used in association with HRTEM to analyze the distribution of electron energies for electrons transmitted through the sample. EELS was also used in this study to provide microanalytical and structural information of the metal gate/high-k stack structure by using a high-resolution electron beam.

2.4.5. X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a very powerful non-destructive technique for material characterization. It can come up with information on structures, phases, and preferred crystal orientations as well as other structural parameters including average grain size, crystallinity, and crystal defects. XRD is widely used in high-k gate dielectric research to determine the morphology of high-k films and determine the amorphous-to-crystalline transition temperature of various high-k materials after thermal treatment. It is also used to determine the crystal structures of different metal gate electrodes.

A monochromatic CuK_{α} X-ray (λ = 1.5418 Å) source is most commonly used for the XRD equipments. Figure 22 is the schematic of X-ray diffraction.[105-106] The X-ray beam impinges on the sample surface with an incident angle θ. X-ray diffraction peaks are observed if a constructive interference is formed between two reflected X-ray beams by the parallel crystal plains. The peak intensities are determined by the atomic decoration within the lattice planes. Hence, the X-ray diffraction pattern can be used to determine the periodic atomic arrangements in a given material. Standard database for X-ray powder diffraction pattern is essential for quick phase identification for a large variety of

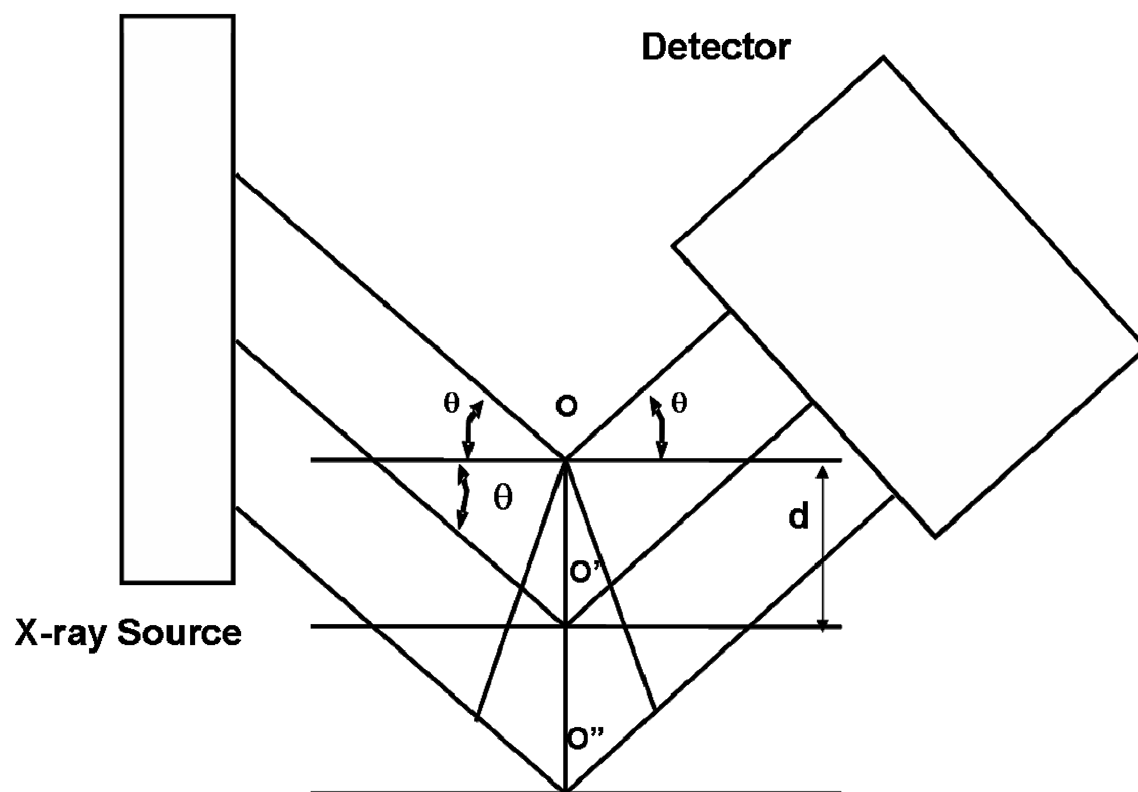


Figure 22 Schematic of an X-ray diffraction equipment.[105-106]

crystalline samples. The crystal spacing can be related to the incident angle θ by Bragg's law as following, [105]

$$n\lambda = 2d \sin\theta \qquad [11]$$

where d is the spacing distance between two parallel planes, n is an integer, and λ=1.5418 Å is the fixed wave length of the CuK_α X-ray source. In addition, the averaged crystallite (grain) size can also be estimated from the peak location and width (FWHM).[106]

In this study, the crystal structures of various metal nitride gate electrodes after different thermal treatments were determined by XRD. The XRD analysis was performed on a Bruker D8 Powder X-ray diffractometer, equipped with CuK_α radiation, a diffracted beam graphite monochromater to cut the K_β component, and a scintillation detector.

2.5 Electrical Characterization

2.5.1. Measurement Setup

In order to obtain the electrical properties of the high-k gate dielectric films and metal nitride gate electrodes, Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements were performed. An HP 4284A LCR meter was used for high-frequency C-V measurement. An HP 4140B pico-ampere meter or an HP 4155C semiconductor parameter analyzer was used for I-V measurement. A Labview 6®-program (National Instruments) was used to control the measurements and record the results.

The measurement equipment setup for the C-V and I-V measurements is very important to obtain accurate measurement results. Since small gate electrode areas (10^{-3}-10^{-5} cm^2) are usually used for the MOS capacitors, only very weak electrical signals can

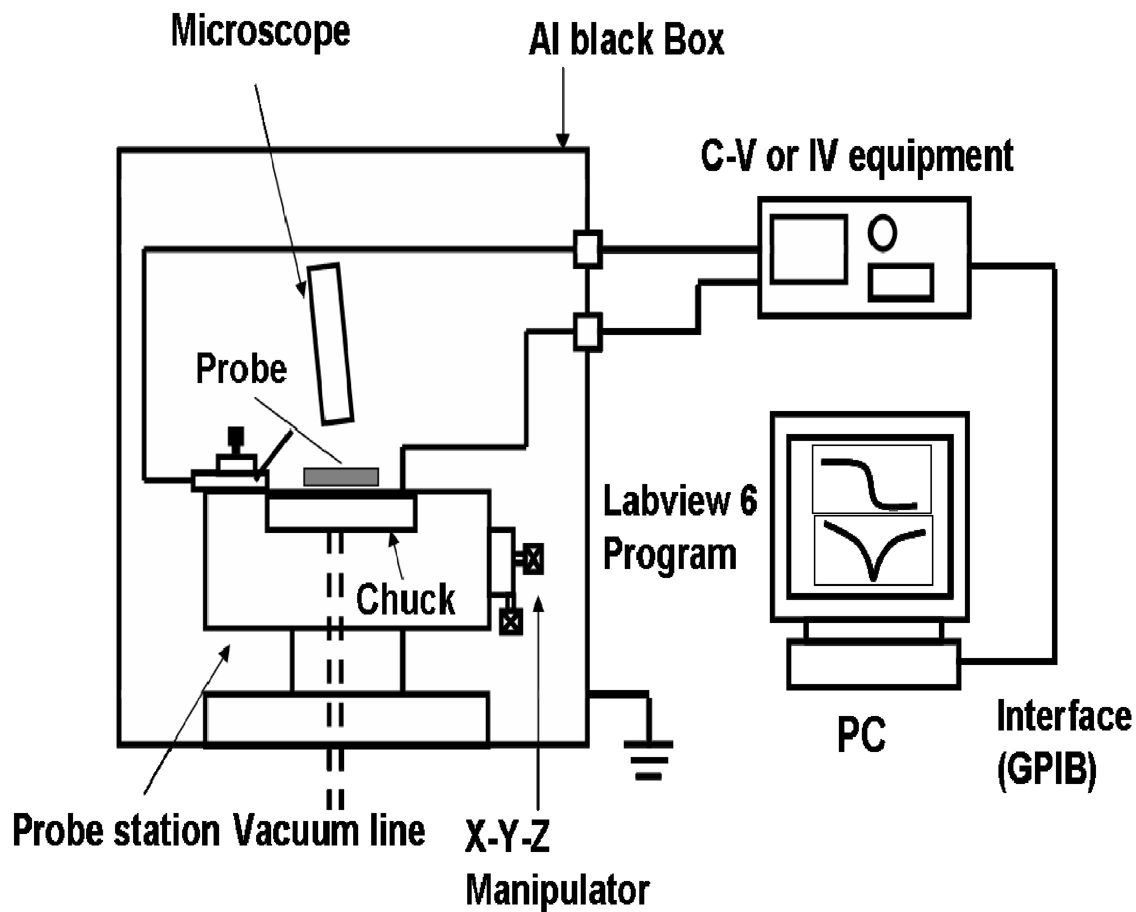


Figure 23 Schematic of the C-V and I-V equipments setup in a black box.

be detected, e.g., the capacitance value was in a range of 10-100 pF and the leakage current value was in a range of 10-100 pA. Therefore, the probe station (Signatone S-1160) together with its wiring was encapsulated inside a light-proof Al-made black box to ensure a completely dark environment for measurement. The black box was electrically grounded to shield against environmental from exterior interferences, such as electrical noises, light, heat, and vibration. A dry ambient should be ensured inside the black box because the moisture may induce a high leakage current.

In addition, the cabling, cable routing, and the measurement chuck should also be carefully connected. A tri-axial gold-plated hot chuck, co-axial and tri-axial cables were connected with the probe station to improve the sensitivity of the electrical measurements. Figure 23 is the simple schematic for the C-V and I-V equipments setup.

2.5.2 Capacitance-Voltage (C-V) Measurement

The Capacitance-Voltage (C-V) technique is the most commonly used tool for the electrical characterization of high-k gate dielectrics and metal gate electrodes. Many important electrical properties of high-k gate dielectrics, including dielectric constant, EOT, flatband voltage, fixed charges, bulk charges, and interface state density can be extracted from the high frequency (HF) C-V measurement. The work function of the metal gate electrodes can also be calculated from the C-V measurement by plotting the flatband voltage and EOT of MOS capacitors with various thicknesses. The inversion capacitance can provide the information of the Si substrate doping concentration. In addition, carrier generation recombination lifetime can also be extracted by using C-t data. All of these electrical properties from the C-V measurement may provide critical device

and process information for high-k and metal gate research. The exact methods to extract these electrical properties from C-V measurement have been explained in later discussions.

In this study, an HP 4284A precision LCR meter was used for the C-V measurement. During the C-V measurement, a small sinusoidal AC drive signal is superimposed on a linear DC voltage ramp to sweep over the bias range from accumulation region to inversion region. The frequency of this sinusoidal AC voltage can be varying from 20 Hz to 1 MHz. A high frequency (above 100 KHz) CV curve is commonly used. Capacitance, conductance, and impedance values can be determined by selecting an appropriate equivalent circuit model for the device being characterized. For example, a parallel mode can be used to measure the differential capacitance (C_{dif}) and the conductance (G) at the same time. Then, the impedance (Z) can be calculated based on C_{dif} and the G.

The HP 4284A precision LCR meter applies the high-frequency drive signal through the metal gate electrode via probe needle. The measurement signal is picked up through the backside of the substrate, via the gold-plated chuck. The gold-plated chuck should be electrically floating to avoid diverting the drive signal to the ground. It should be noted that the polarity of the measurement is reversed—the drive signal is applied to the substrate, and the signal is measured at the gate via the probe needle —the additional capacitance of the chuck on which the substrate rests will complicate the interpretation of the measurement data. Besides, the chuck itself will act as an antenna, which may pick up noise from the environment.

During a C-V measurement of the MOS capacitor, small-signal AC may lose energy due to the presence of series resistance. Serious resistance can cause errors in the

extraction of the right capacitance and EOT values from a C-V curve, especially for ultra-thin SiO_2 and high-k dielectric layers. Series resistance is caused from several sources, such as the contact between the probe needle and gate electrode, native oxide on the metal gate, the contact between the Si to chuck, resistance of the bulk Si substrate, and non-uniform doping distribution of the bulk Si. Efforts have been made to minimize the series resistance. For example, a backside Al can be deposited after removing the backside SiO_2 with a buffer HF solution to improve the contact between the Si substrate to the gold-plated chuck. A high doping concentration Si wafer can be used to reduce the bulk Si substrate resistance. In addition, the effect of the series resistance can be greatly reduced if the C-V measurement is performed at a low frequency. Despite all of these efforts, it is almost impossible to completely get rid of the series resistance effects on the C-V measurement. A series resistance correction is necessary before extracting any useful information from the C-V curves.

A general approach of series resistance measurement and correction has been proposed by Nicollian et al. [55] When the MOS capacitor is biased in an accumulation condition, the series resistance (R_s) can be calculated by the following relation, [55]

$$\mathbf{R_s = \frac{G_{ma}}{G_{ma}^2 + \omega C_{ma}^2}} \quad [12]$$

where C_{ma} is the measured accumulation capacitance, G_{ma} is the measured accumulation conductance, and ω is the angular frequency. The corrected capacitance (C_c) and the corrected conductance (G_c) can be determined with the calculated R_s by the following relations, [55]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \quad [13]$$

$$G_C = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \quad [14]$$

$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s \quad [15]$$

where C_m is the measured capacitance of the C-V curve of interest and G_m is the measured conductance across the terminals of the MOS capacitors. Hence, the real oxide capacitance (C_{ox}) of the MOS capacitor can be calculated from Eq.13 knowing C_{ma}, G_{ma}, and R_s.

2.5.3 Current-Voltage (I-V) Measurement

Current-Voltage (I-V) Measurement is another important electrical characterization method. An HP 4140B pico-ampere meter or an HP 4155C semiconductor parameter analyzer was used in this study. They are mainly used to measure the leakage current density and the conduction mechanism of the MOS capacitors with a high-k gate dielectric layer. In addition, they can also be used for some reliability characterization of the high-k gate dielectrics and metal gate electrodes, including time-dependent dielectric breakdown (TDDB), charge to breakdown (QBD), and stress-induced leakage Current (SILC). The HP 4155C semiconductor parameter analyzer can also be used for quasistatic C-V measurement.

During the I-V measurement, a ramped or stepwise DC bias is applied on the top gate electrode of an MOS capacitor via the probe needle. The probe needle will serve as both the DC bias source and current signal detector. For the HP 4140B pico-ampere meter, a

HP 16053A connection selector is needed to connect the guard ring of the triaxial cable on the current meter to the voltage source because it has a separate voltage source (V_A) and current meter (I). For the HP 4155C semiconductor analyzer, no additional connector is needed since the source/monitor unit (SMU) configuration of the voltage/current source already has this ability.

If a ramped DC bias is used, measured current may be contributed from tow components, leakage current and displacement current. A slow ramp DC bias, e.g., 0.01 V/second, should be used to minimize the displacement current component, especially when the leakage current is very small. If a stepwise DC bias is used, a relatively long delay time, e.g., 1-2 seconds, is preferred for the same purpose. However, if the delay time is too long, the DC bias will serve as a constant voltage stress, causing an excessive high leakage current due to electron trapping.

CHAPTER III

DIELECTRIC PROPERTIES OF 10 NM-THICK HAFNIUM-DOPED TANTALUM OXIDE GATE DIELECTRICS

3.1 Introduction

As the channel length of MOSFETs scales down to sub 70 nm feature size, the SiO_2 gate oxide thickness needs to be reduced accordingly, e.g., less than 1.5 nm.[11] At this thickness, the SiO_2 layer shows some problems, such as a high leakage current, poor reliability, and undesirable boron diffusion from the polysilicon gate.[1, 3-4] When a gate dielectric material with a high dielectric constant (k) is used to replace SiO_2, many of the problems can be solved because a physically thicker layer can be used.

Many binary metal oxides, such as Ta_2O_5, HfO_2, ZrO_2, Y_2O_3, and Al_2O_3, are considered promising candidates and are under extensive investigation. All of these materials have many advantages as a high-k gate dielectric, but very few materials can meet all of the requirements of gate dielectrics. For example, Ta_2O_5 has been widely studied as an alternate high-k gate dielectric because it has a high dielectric constant (~25) and has been used as a dielectric material in high-density dynamic random access memory (DRAM). But Ta_2O_5 is not thermodynamically stable in direct contact with silicon and it will react with the silicon substrate to form a low-k interface layer at a raised temperature.[39] Since this interface layer has a k value lower than that of the bulk high-k dielectric films, it can drastically reduce the effectiveness of the high-k dielectric films. In addition, Ta_2O_5 has a relatively small band gap (4.4eV) and electron offset (0.3eV) with respect to the Si conduction band, which may lead to a high leakage current.[1,56] Meanwhile, it was reported that HfO_2 has good thermodynamic stability on

top of silicon and a high-k value (~25).[48, 107-108] It also has a relatively wide band gap (~6.0eV) and a high electron offset (1.5eV). [48] However, HfO_2 crystallizes at a relatively low temperature e.g., ~400°C -500°C for thick films[109] and ~700°C for thin films[110],which will dramatically increase the leakage current and cause other reliability problems of uniformity and surface morphology during a conventional CMOS fabrication process flow.

To improve the dielectric properties of the simple metal oxides, the doping technique, i.e., adding a third element into the binary oxide high-k gate dielectric, had been studied by many researchers. This could potentially combine the desirable properties from individual oxides while eliminating or reducing the undesirable properties of end member oxides. It has been reported that Ta_2O_5 is a good base oxide for the doping technique because its structure does not change significantly with the addition of another oxide.[83-85] Many studies have been done to improve Ta_2O_5-based alloy oxide systems. Ti, Al, and Zr have been used as dopants.[83-85, 111] Ta_2O_5-based nanolaminate structures with ZrO_2, HfO_2, and Al_2O_3 were also investigated by many researchers.[74, 112-113] All of these studies proved that the dielectric properties of Ta_2O_5 could be improved with the doping process. Moreover, it was observed that by adding a third element into the binary metal oxide, the amorphous to polycrystalline temperature would increase, which could lower the leakage current of the high-k films.[114] In this study, the physical and electrical properties of various Hf-doped TaO_x films were investigated for the application of alternative high-k gate dielectric material.

3.2 Experimental

All of the Hf-doped TaO_x thin films were deposited on p-type (100) silicon wafers (doping concentration of 10^{14}-$10^{15}cm^{-3}$) by co-sputtering from separate Hf and Ta targets using two 13.56 MHz RF generators for sputtering. The sputtering was done in a 1:1 Ar/O_2 gas mixture with a total flow rate of 40sccm at 5mTorr and room temperature. The Si wafer was pre-cleaned with a dilute HF solution to remove the native oxide. Before film deposition, both targets were pre-sputtered with Ar to remove any possible contamination. The Ta sputtering power was fixed at 100 W and the Hf sputtering power was varied between 20 W and 180 W. In addition, un-doped TaO_x and HfO_x films were also deposited at 100 W to serve as references. The film's physical thickness was controlled at about 10 nm by adjusting the deposition time. During deposition, the substrate holder was rotated at 20 rpm to ensure the film uniformity. A post deposition annealing (PDA) step was carried out in a quartz tube furnace under the O_2 200 Torr atmosphere at 600°C for 60 minutes or 700°C for 10 minutes.

After the PDA step, an aluminum (Al) film was sputter-deposited on top of the high-k layer. The Al gate electrode (with an area of 0.00125 cm^2) was defined with a mask aligner and wet etched with a mixture of H_3PO_4, HNO_3, CH_3COOH, and H_2O. Another 2000 Å Al was deposited on the backside of the silicon wafer for better contact. The complete MOS capacitors were treated with a post-metal annealing (PMA) step under the forming gas (N_2:H_2=9:1) ambient at 300°C for 30 minutes.

The film's refractive index and thickness were determined by a Rudolph i1000 ellipsometer with a fixed wavelength of 638.2nm. All films in this study had a refractive index between 1.9 and 2.1. X-ray photoelectron spectroscopy (XPS) with an Al Kα X-

ray (hυ=1486.6eV) monochromatic X-ray source was used to study the chemical composition and bond structure of the high-k films. All of the peaks were corrected with the charging factor using C 1s at 284.6 eV as the reference. A time-of-flight secondary ion mass spectroscopy (ToF-SIMS) was also used to assess the stacked film composition. The film was sputtered with gallium at 2 keV at an angle of 70º. The interface layer thickness between the high-k film and the Si substrate was determined by high-resolution transmission electron microscopy (HRTEM).

Electrical properties, such as dielectric constant, flat-band voltage, fixed charge density, hysteresis, and interface state density were extracted from the capacitor's capacitance-voltage (C-V) curve in the accumulation region, which was measured with a HP 4284A Precision LCR Meter. The leakage current density and breakdown strength were determined from the current-voltage (I-V) curve, which was measured with a HP 4140B pico-Ampere Meter.

3.3 Hf Doping Effects on Chemical and Physical Properties

3.3.1. Influence of Hf Dopant Concentration on Bulk High-k Film Material Properties

Figure 24 shows the Hf/ (Hf+Ta) atomic ratio as a function of Hf co-sputtering power with the Ta sputtering power fixed at 100W. The ratios were determined by XPS. The Hf/ (Hf+Ta) atomic ratio increases monotonically with the increase of the Hf co-sputtering power, but the relationship is not linear. This figure clearly shows that the Hf doping concentration in the films can be adjusted by varying the Hf co-sputtering power. In later discussions, the Hf co-sputtering power will be used to represent the dopant conditions.

For example, Hf (20W)-TaO_x means the film deposited with Hf 20W co-sputtering power, which corresponds to a Hf/ (Hf+Ta) ratio of 0.25.

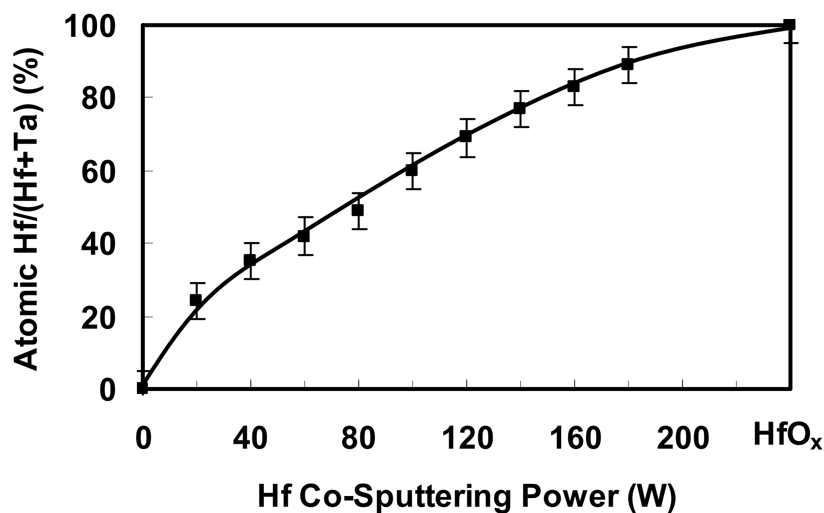


Figure 24 Atomic Hf/ (Hf+Ta) ratio of various Hf-doped TaO_x films as a function of Hf co-sputtering power. During the deposition, the Ta sputtering power was fixed at 100 W and the Hf sputtering power was varied from 20 W to 180 W.

Figure 25 shows the normalized XPS Ta 4f and Hf 4f spectra of un-doped and Hf-doped TaO_x films after 700°C O_2 PDA. All XPS spectra are well fitted with a single spin-orbit split voigt function pair. The least-squares method analysis of Hf 4f and Ta 4f XPS spectra indicated that neither Hf nor Ta sub oxides were formed in these films. Therefore, the doped film is a mixture of fully oxidized Ta_2O_5 and HfO_2. For the un-doped TaO_x film, the binding energy of Ta $4f_{7/2}$ peak is 26.7eV. For the Hf (20W)-doped TaO_x film, the Ta $4f_{7/2}$ peak shifts to a low binding energy of 26.3eV. For the Hf (180w)-doped TaO_x films, the Ta $4f_{7/2}$ peak shifts to an even lower binding energy of 26.2 eV. Fig.2 (b) shows that the Hf $4f_{7/2}$ peak in the Hf (20W)-doped TaO_x film has a higher binding energy than the un-doped HfO_x films, i.e., 17.1 eV vs. 16.7 eV. However, the Hf $4f_{7/2}$ core level binding energy decreases with the increase of Hf content, e.g., 16.9 eV at the Hf co-sputtering power of 180W. A similar trend has been observed on the 600°C O_2 annealed Hf-doped TaO_x films.

It was reported that the binding energy of a metal oxide shifted due to the presence of a dissimilar metal.[115-117] Barr [115] reported when two oxides were mixed to form an alloy oxide, the cation of the more ionic metal oxide would become more ionic, and the cation of the more covalent metal oxide would become more covalent. Therefore, the charge of the more ionic cation is expected to be larger in the mixed oxide than in the pure oxide. The charge of the more covalent cation is expected to be smaller in the mixed oxide than in the pure oxide. Since the core level chemical state is a good reference of the cation charge state, the XPS binding energy of the element in the mixed oxide will be different from that of the pure oxide. Guittet et al. [116] discussed the general phenomenological rule of a $ZrSiO_4$ system using theoretical calculations. They concluded that the charge transfer

played an important role in the XPS binding energy shift. The Hf is a more ionic cation than Ta because the average bond iconicity of HfO_2 and Ta_2O_5 are 0.68 and 0.61, respectively.[117] Therefore, in the Hf-doped TaO_x film, the Hf 4f core level shifts to a higher binding energy and the Ta 4f core level shifts to a lower binding energy compared with those in the un-doped oxides.

In addition, Lucovsky et al. [117-118] reported the charge transfer involved all elements in the mixed oxide films, which was an essential factor affecting the core level binding energy shift. In the Hf-doped TaO_x film, both Ta (electronegative=1.50) and O (electronegative=3.44) are more electronegative than Hf (electronegative=1.30). As the Hf/ (Ta+Hf) atomic ratio increases, the partial positive charges of Ta and Hf decrease, and the negative partial charge of O increases. Therefore the corresponding binding energies of the Ta 4f and Hf 4f peaks decrease as the Hf/ (Hf+Ta) atomic ratio increases in the film due to charge transfer.

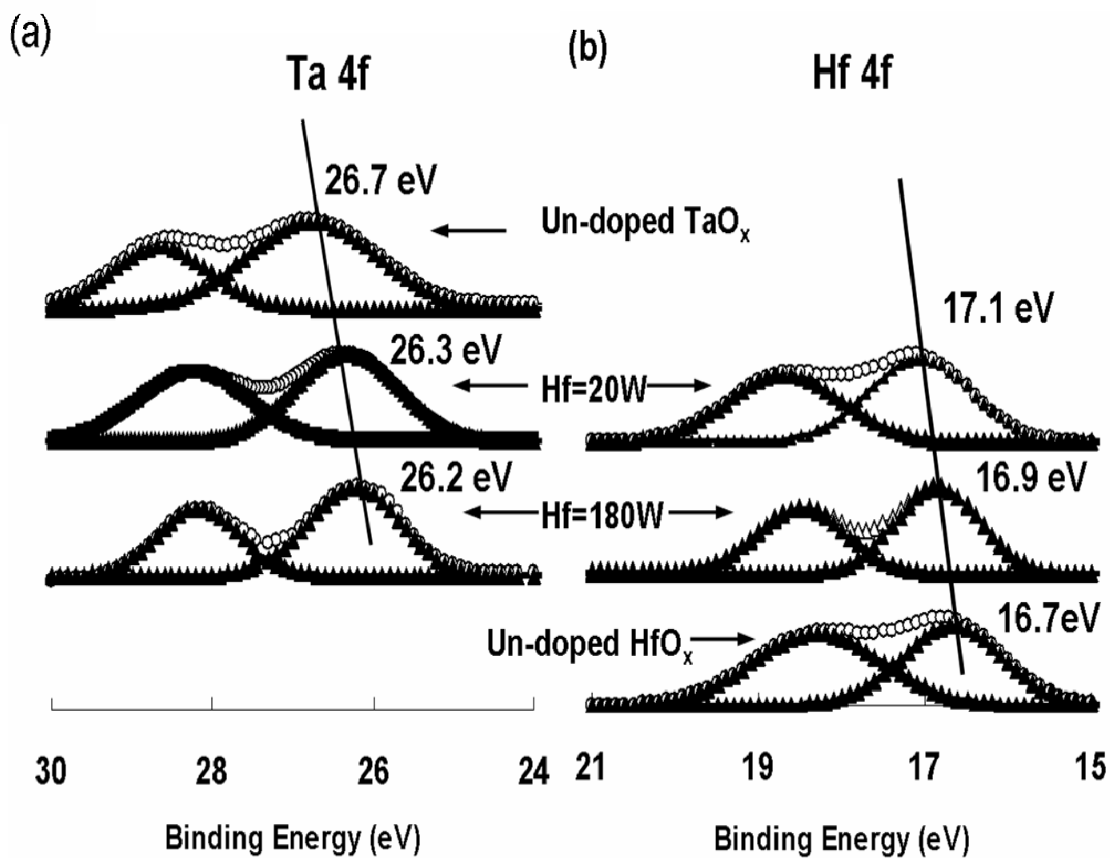


Figure 25 Normalized XPS spectra of Hf-doped TaO_x films and un-doped films, after annealed in O_2 at 700°C for 10 minutes: (a) Ta 4f, (b) Hf 4f.

3.3.2. Influence of Hf Dopant Concentration on Interface Layer Composition

Figure 26 (a) shows the SIMS depth profile of an un-doped TaO_x film on Si after 700°C-10 min O_2 PDA. The Si signal was detected at the interface region, which mainly came from the Si_2O cluster ion signal as shown in the inset of Fig. 26 (a). The strong Si_2O signal suggests the formation of a SiO_x interface layer in the sample. This result is consistent with the report of poor thermodynamic stability of Ta_2O_5 when it is in direct contact with Si at an elevated temperature.[39] Figures 26 (b)-(c) shows that the Si signal still exists at the interface region of the Hf-doped TaO_x films, but the magnitude is much lower. The Si signal in the doped film mainly came from the Si_2O and $HfSiO_2$ ion clusters as shown in the insets of Fig. 26 (b)-(c). The presence of the $HfSiO_2$ ion cluster signals suggests the formation of $HfSi_xO_y$ in the interface layer region after incorporation of HfO_x into the TaO_x film. A similar result was observed in the un-doped HfO_x sample as shown in Fig. 26 (d). These results suggest that the interfacial layer composition has been transformed from SiO_x-like to $HfSi_xO_y$-like after the Hf doping process. From the insets of Fig.26 (a)-(c), the count of Si_2O cluster ion signals in the Hf-doped TaO_x interface layer is an order of magnitude lower than that of the un-doped TaO_x interface layer. The Si_2O ion cluster count decreased further with the increase of the Hf concentration in the film. This result implies the doping of Hf into TaO_x can effectively hinder the formation of SiO_x at the interface. Additionally, the ratio of $HfSiO_2$ to Si_2O at the interface increased with the increase of Hf doping concentration in the bulk films, as shown in insets of Fig. 26 (b)-(d). Therefore, the interfacial layer composition is directly influenced by the Hf dopant concentration in the bulk layers.

The phase diagram of a Ta-Si-O system shows Ta_2O_5 is not stable when it is in direct contact with Si and tends to separate into SiO_x and metal oxide or silicide.[1, 39] Therefore, it is not easy to form a stable ternary homogeneous compound in the Ta-Si-O system. In this study, Fig.26 (a)-(c) shows that the Ta signal decays rapidly before the Si signal reaches the peak value. Therefore, the interfacial layer is Ta-deficient. Albers et al. reported that the interfacial layer was transformed from a Ta-Si-O mixture to pure SiO_2 after 800°C O_2 annealing.[119] However, since tie lines exist in the phase diagram of the Hf-Si-O system, HfO_2 and $HfSi_xO_y$ may co-exist in the presence of Si.[3] The formation of the $HfSi_xO_y$ interfacial layer between the HfO_2 and Si substrate had been reported previously.[120-122] The SiO_x interface could react with HfO_x to form $HfSi_xO_y$.[120] Si atoms could also diffuse into the bulk high-k film during high temperature annealing and react with Hf to form a Hf silicate.[121] Therefore, the Hf doping process can convert the SiO_x interface layer into the Hf silicate layer, and therefore, reduce the Si_2O ion signal as well as hinder the formation of the low permittivity SiO_x interface layer. Since the $HfSi_xO_y$ has a higher k value than SiO_x, it will contribute to the overall k value of the high-k gate stack. Moreover, it was reported that this kind of silicate-Si interface had similar interface quality as a SiO_x-Si interface, [1] which is potentially important to the gate dielectric application because the interface state density and carrier mobility are dependent on the interface quality.

Figure 26 also shows Hf ion signals diffuse deeper toward the Si substrate than Ta ion signals. Ta ion signals decay abruptly in the interface layer. The Hf ion signals persist throughout the high-k stack layers and start to decay at almost the same position as the Si signal peak. This is consistent with the SIMS analysis indicating $HfSi_xO_y$ is formed at the

high-k/Si interface and Hf atoms are involved in the interface layer formation process. However, even though Hf ion signals exhibit long decay tails into the Si substrate as shown in Fig.26 (b)-(d), it does not necessarily mean Hf atoms diffuse into the Si substrate. Nieveen et al. [123] observed similar long tailing of Hf ion signals into the Si substrate during the SIMS analysis of high-k HfO_2 and $HfSiO_4$ dielectric films. They performed SIMS and XPS backside depth profiles on the same sample and confirmed that there were no Hf atoms intrinsically present in the Si substrate and the long Hf tails were due to the SIMS sputtering process. Therefore, the long Hf ion signal decay tail observed in this study is likely from the sputter beam-induced artifact in the standard SIMS profile process.

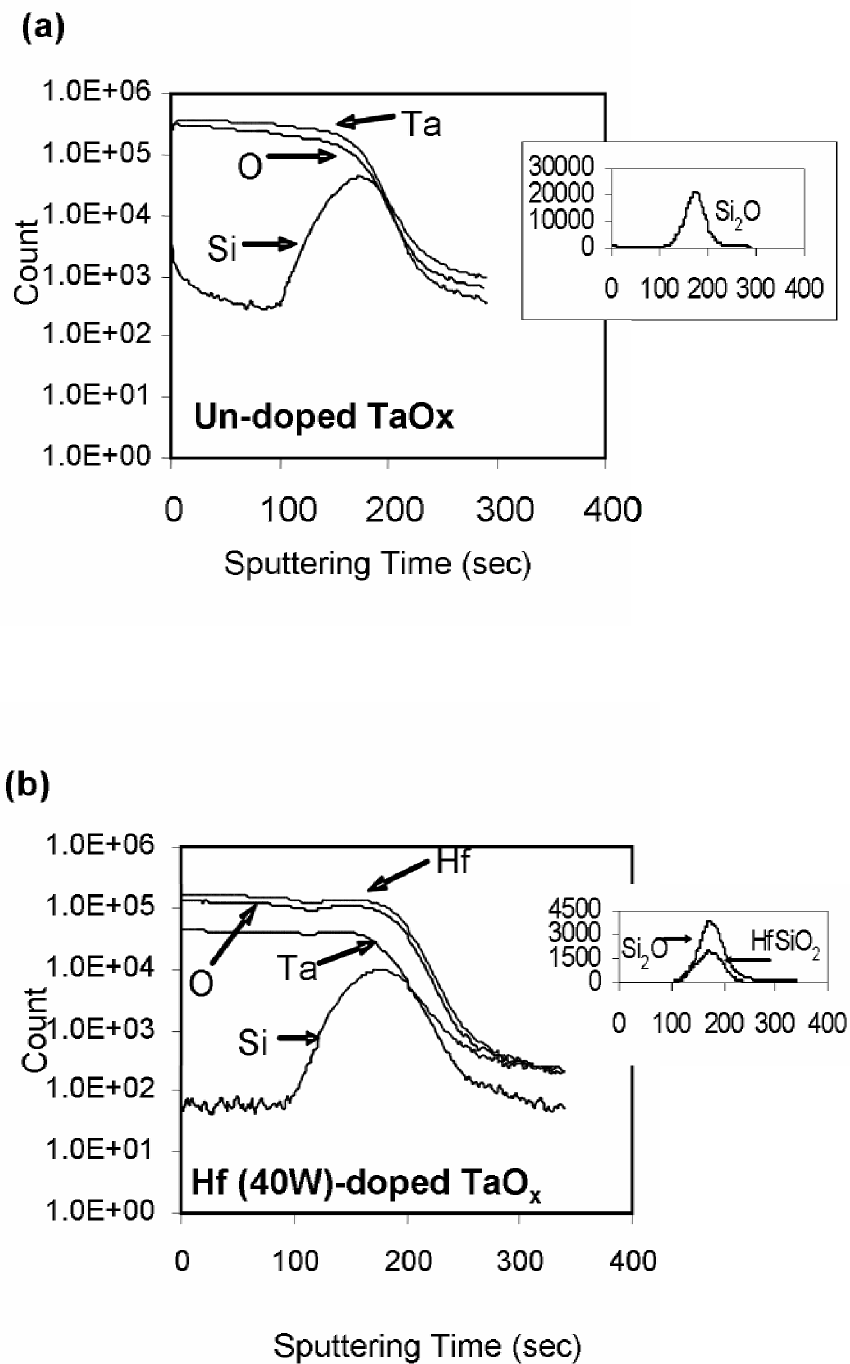
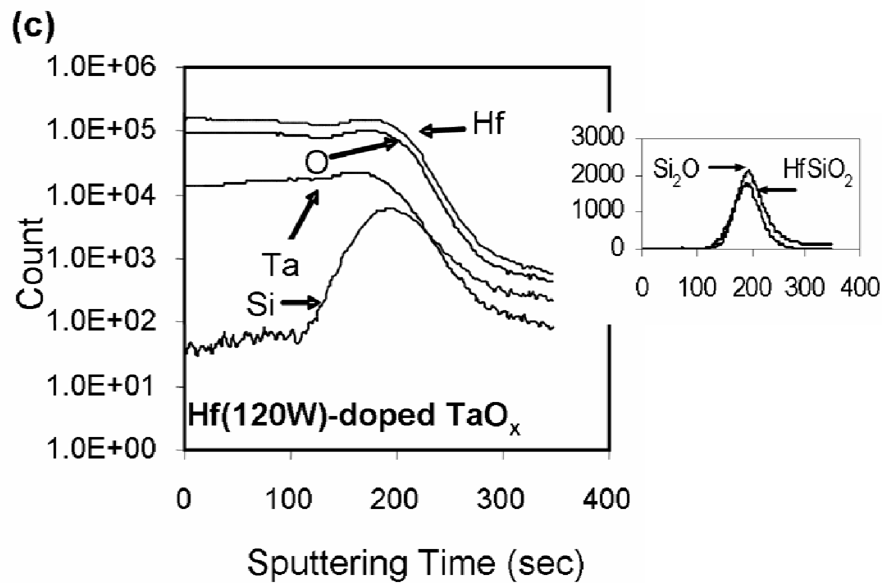


Figure 26 SIMS profiles: (a) un-doped TaO_x, (b) Hf (40 W)-doped TaO_x, (c) Hf (120 W)-doped TaO_x, and (d) un-doped HfO_x. All films were annealed in O_2 at 700°C for 10 minutes.



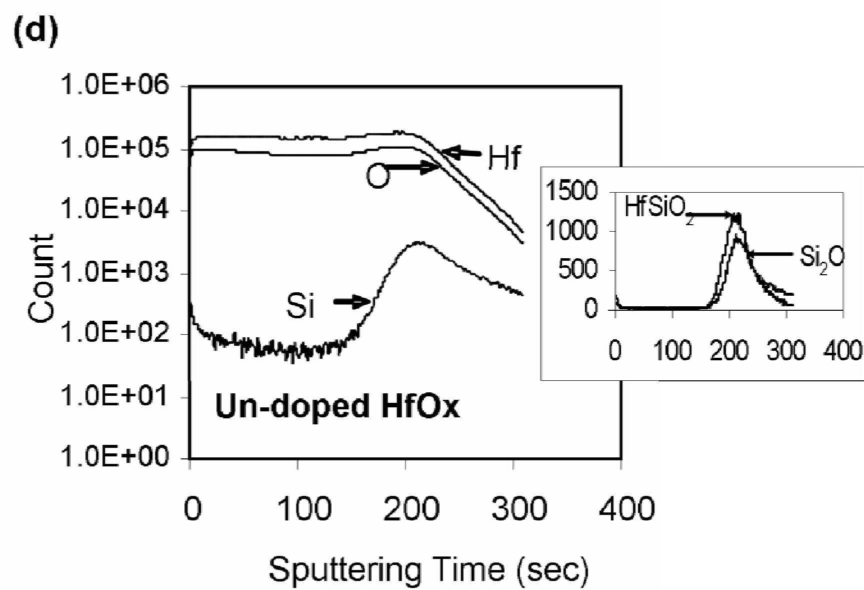


Figure 26 continued.

3.3.3. Influence of Hf Dopant Concentration on Interface Layer Thickness

Figure 27 shows the HRTEM cross-sectional views of three types of films, i.e., un-doped TaO_x, lightly Hf (20W)-doped and heavily Hf (160W)-doped TaO_x. These samples were annealed at 700°C for 10 minutes in an O_2 ambient. For all cases, an amorphous interface layer was formed between the high-k layer and the silicon substrate. Figure 28 shows the interface layer thickness measured from the HRTEM figures vs. the Hf content in the bulk high-k film. The interface layer thickness decreases from 25 Å to 21 Å when the Hf sputtering power increased from 0W to 60W. For moderately and heavily Hf-doped films, e.g., the Hf sputtering power above 80W, the interface layer thickness was reduced to as low as 15 Å, which is comparable to that formed from the pure HfO_2 film.[48] The decrease of the interface layer thickness can also be correlated with the decrease of the Si_2O ion signal intensity from the SIMS analysis, which was discussed in the previous section. These two results indicate the interface layer thickness between Ta_2O_5 and Si can be reduced with the Hf doping process. The decrease of the interface layer may be attributed to better thermodynamic stability of HfO_2 compared with Ta_2O_5 when in direct contact with Si. It was reported when the as-deposited Ta_2O_5 films were annealed in the N_2 or O_2, the interface layer was formed by the reaction between the high-k layer and Si.[124] With the high heat of formation of the HfO_2, i.e., ΔH_f=271Kcal/mol, [48, 110] the HfO_x component in the Hf-doped TaO_x films can limit the reaction between the high-k layer and Si and therefore decrease the interfacial layer thickness. This result indicates that the thermodynamic stability of Hf-doped TaO_x can be improved with the inclusion of the HfO_x component.

To further investigate the Hf doping effects on the interface layer thickness, the three films in Fig. 27 were further annealed for extended periods of time, i.e., 60 minutes and 180 minutes under the same 700°C, O_2 ambient. Figure 29 shows HRTEM images of these samples. Figure 30 is a summary of the interface layer thicknesses of samples with different Hf dopant concentration and annealing times. Several conclusions can be summarized from this figure. First, the interface layer thickness increases with the annealing time. The increase rate is high at the beginning and low after a long time. Second, the interface layer thickness decreased with the increase of the Hf sputtering power. However, the difference is reduced with the extension of the annealing time. The interface layer formation is controlled by two mechanisms: 1) interface reaction between high-k film and Si and 2) diffusion of reactants through the interface layer. Since O atoms have a low diffusion rate through the interface layer, the diffusion of Si atoms through the already formed interface layer should be the limiting factor for the second mechanism.[124] When the annealing time is short, e.g., 10 minutes, the interface layer is thin. Si can easily diffuse through the interface layer. Therefore, the bulk high-k film properties, e.g., the thermal stability of HfO_2 and Ta_2O_5 in the presence of Si, controlled the interface layer formation process. When the annealing time is long, e.g., 180 min, the interface layer is thick. It takes a long time to diffuse the Si through the interface layer to the reaction site. Therefore, the bulk high-k film property is less influential to the interface layer thickness after a long time of annealing. Beyond 180-minute annealing, there is no drastic increase of the interface layer thickness, whether the film is un-doped or doped. The interface layer formation process appears to be self-limited after a long annealing time.

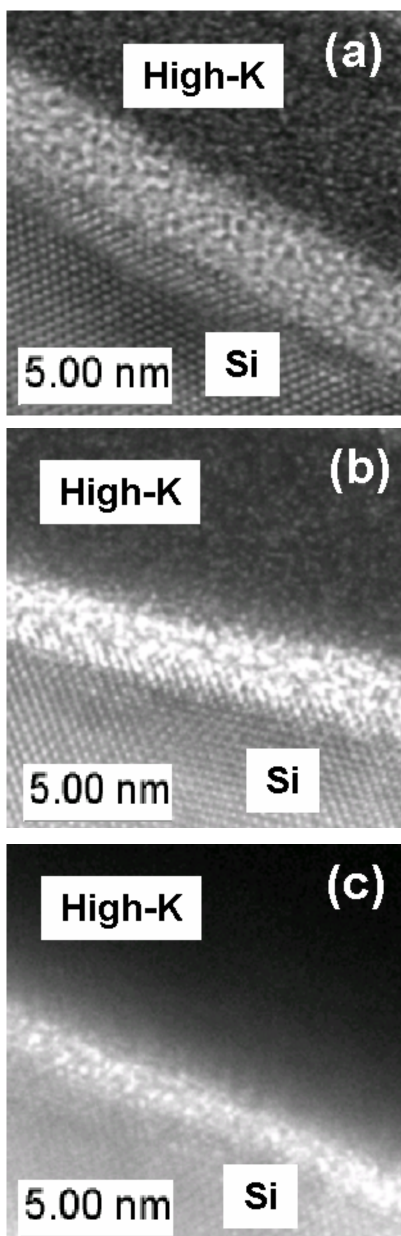


Figure 27 HRTEM cross-sectional views of (a) un-doped TaO_x, (b) Hf (20W)-doped TaO_x, (c) Hf (160W)-doped TaO_x after 700°C-10 min O_2 annealing.

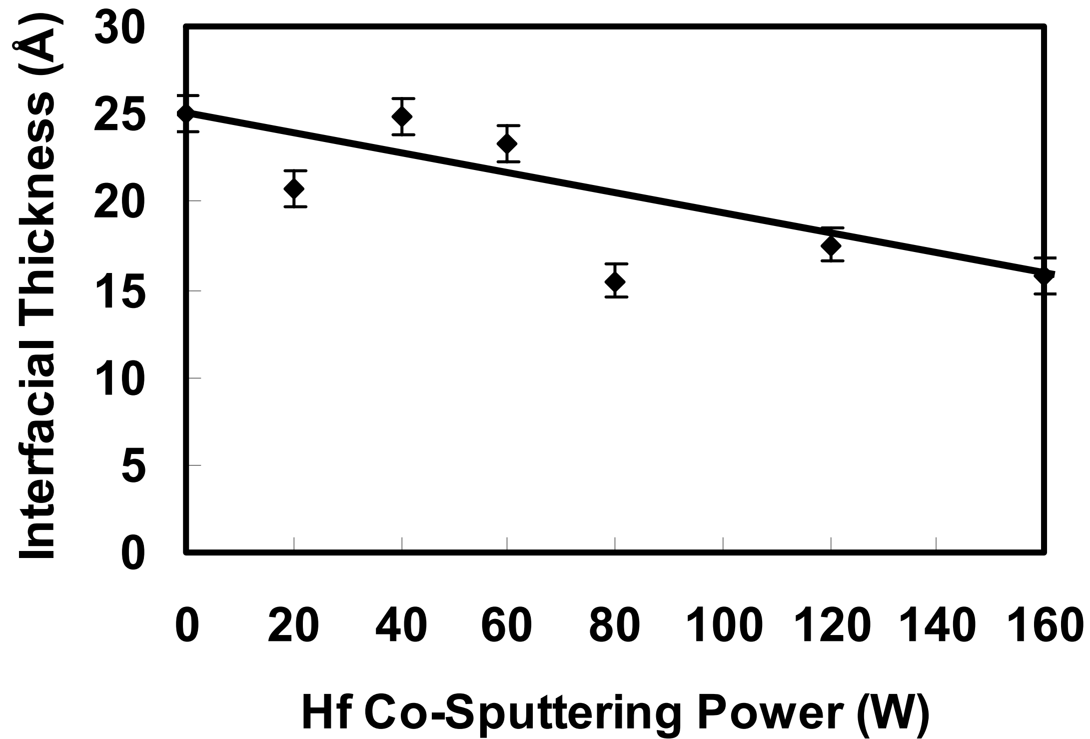


Figure 28 Interface layer thicknesses at high-k/silicon contact region vs. the Hf co-sputtering power of various Hf-doped TaO_x samples after 700°C-10 minutes O_2 annealing.

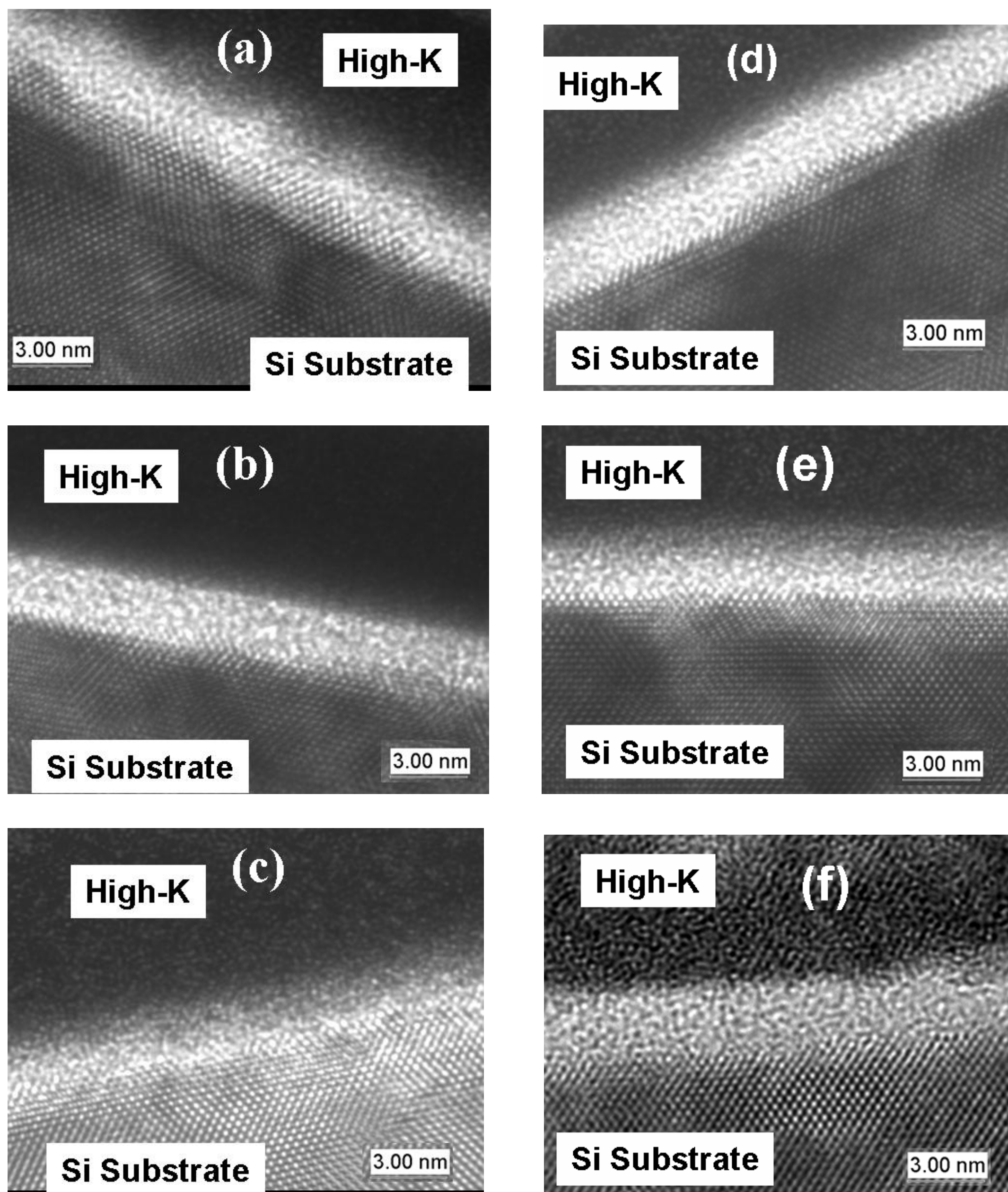


Figure 29 HRTEM cross-section view of (a) un-doped, (b) Hf (20W)-doped, and (c) Hf (160W)-doped TaO_x films, after 700ºC-60 min O_2 annealing; (d) un-doped, (e) Hf (20W)-doped, and (f) Hf (160W)-doped TaO_x films, after 700ºC-180 min O_2 annealing.

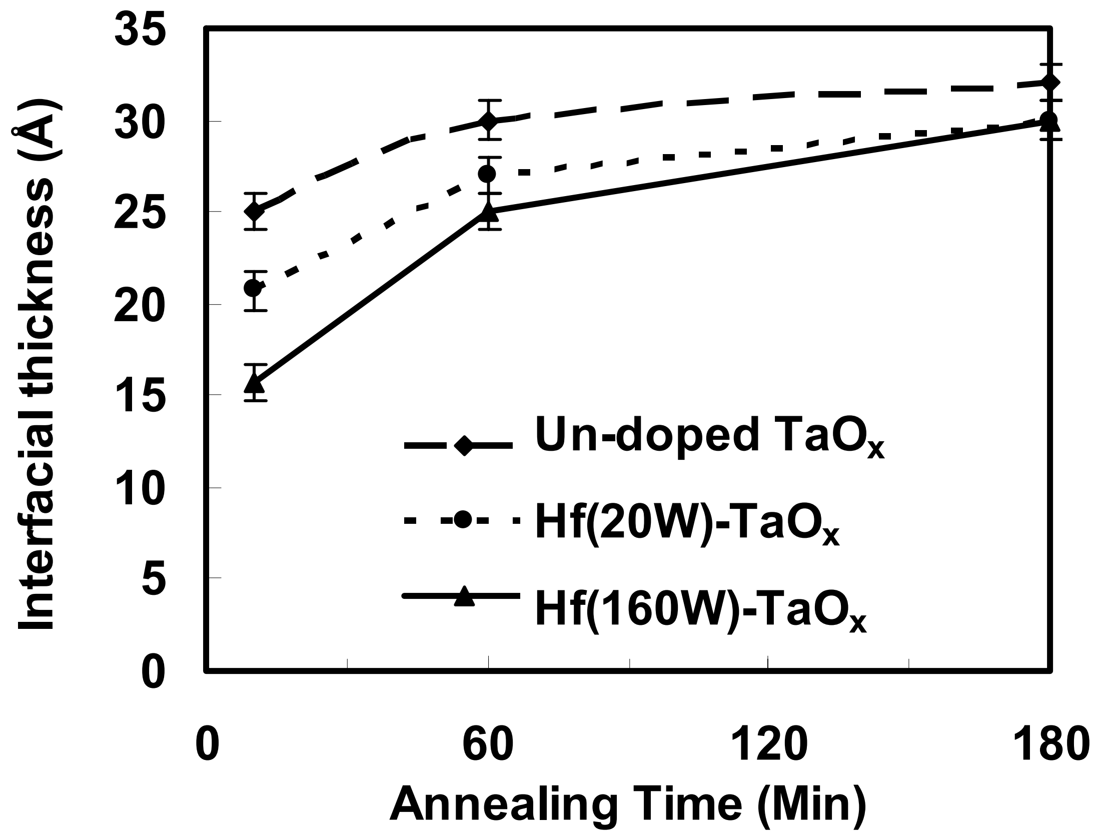


Figure 30 Interface layer thicknesses at high-k/silicon contact region vs. the 700°C O_2 annealing time.

The 180 min-annealed Hf (160W)-doped TaO_x film was partially crystallized as shown in Fig. 29 (f). This is due to 1) the excessive thermal budget in the annealing process and 2) the crystallization temperature of HfO_2 being lower than that of Ta_2O_5. However, the Hf (20W)-doped TaO_x film was still amorphous after 180 minutes annealing. This phenomenon is consistent with reports that the amorphous-to-polycrystalline transition temperature of a metal oxide can be increased by the addition of a certain amount of dopant.[114, 125]

3.4 Hf Doping Effects on the Electrical Properties

3.4.1. Influence of the Hf Dopant Concentration on the Effective Dielectric Constant (k_{eff})

Figure 31 shows variations of the k_{eff} as a function of the Hf co-sputtering power. The physical thickness of these films is around 10 nm. The k_{eff} values were calculated based on the maximum capacitance in the accumulation region of the C-V curves measured at a frequency of 1 MHz after a series resistance correction.[55] For a high frequency C-V curve, i.e., measured at 1 MHz, the measured accumulation capacitance is always lower than the real oxide capacitance due to the presence of the series resistance in the capacitor. The effect of the series resistance is especially significant at a high frequency. Although the series resistance of the MOS capacitor can be minimized during the fabrication process, a series resistance correction is required to extract the correct oxide capacitance and k_{eff} from the measured high frequency C-V curves. The k_{eff} value increased with the Hf concentration and then decreased with the further increase of the Hf concentration. The k_{eff} peaked at 20W, which has an Hf/ (Hf+Ta) atomic ratio around 0.25. The same trend

was observed at different PDA conditions, i.e., 600°C-60 min. The increase of k_{eff} at the low Hf doping concentration can be attributed to the improvement of the interface layer properties. For example, Fig.28 shows that the interface layer thickness decreases with the increase of the Hf concentration, which enhances the k value. However, the k value decreases with the further increase of the Hf dopant concentration, which is contradictory to the above statement. Therefore, other explanations are required. Similar nonlinear improvement of intrinsic dielectric constant k values was widely observed on other doped Ta_2O_5 films.[83-85, 111] It is possible that the doping process changed the density or structure of the bulk high-k films. Devine and Revesz [126] have shown theoretically some mixed oxides may exhibit a nonlinear improvement of the dielectric constant k value due to the changes of effective molecular polarizations and molecular volume after the doping process. It was also reported that adding a proper amount of network modifier ions (e.g., Hf and Zr) into some dielectric materials can improve the dielectric constant even at a low concentration range.[1, 127] An enhancement of the dielectric constant beyond that predicted from a simple linear interpolation is expected. The incorporation of Hf or Zr atoms into a metal oxide may change the localized bonding order of the material and therefore lead to an increased contribution of the vibrational mode to the dielectric constant.[127-129] However, at a high doping concentration, the excessive Hf-O or Zr-O bonds may reduce the contribution of the vibration mode to the dielectric constant and therefore, eliminate the effects of the localized bonding order.

In short, the improvement of k_{eff} values of the Hf-doped TaO_x films can be attributed to two factors: thinner interface layer thickness and improvement of the bulk high-k film properties.

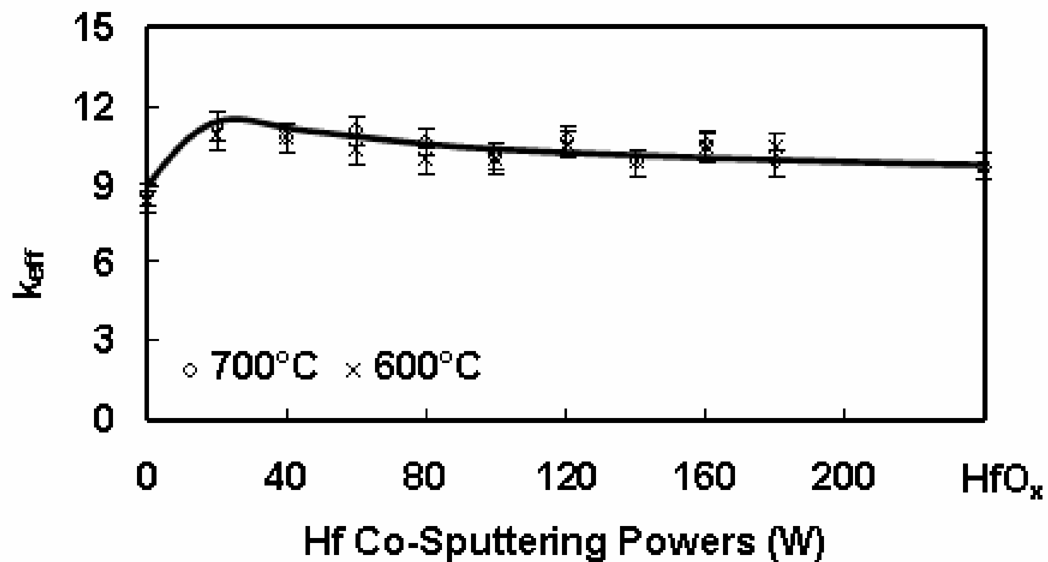


Figure 31 Effective dielectric constant K values of various Hf-doped TaO_x films as a function of the Hf co-sputtering power. Film thickness is around 10 nm for all of these samples.

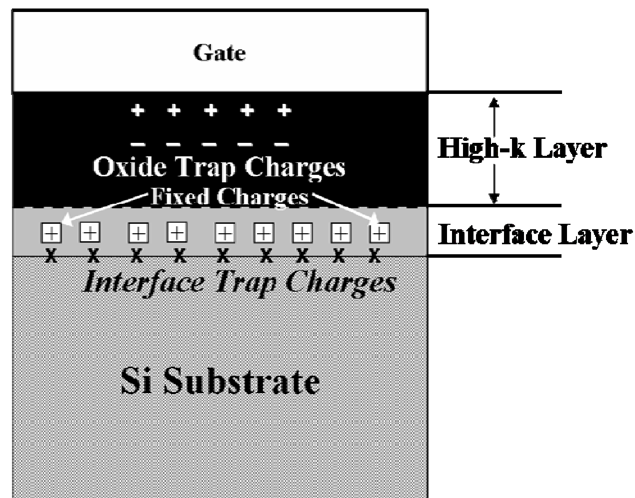
3.4.2. Influence of the Dopant Concentration on the Electrical Properties of the High-k Stack

The C-V measurements of all Hf-doped and undoped TaO_x films have negative flat-band voltage shifts (V_{FB}). This indicates the presence of net positive fixed charges in

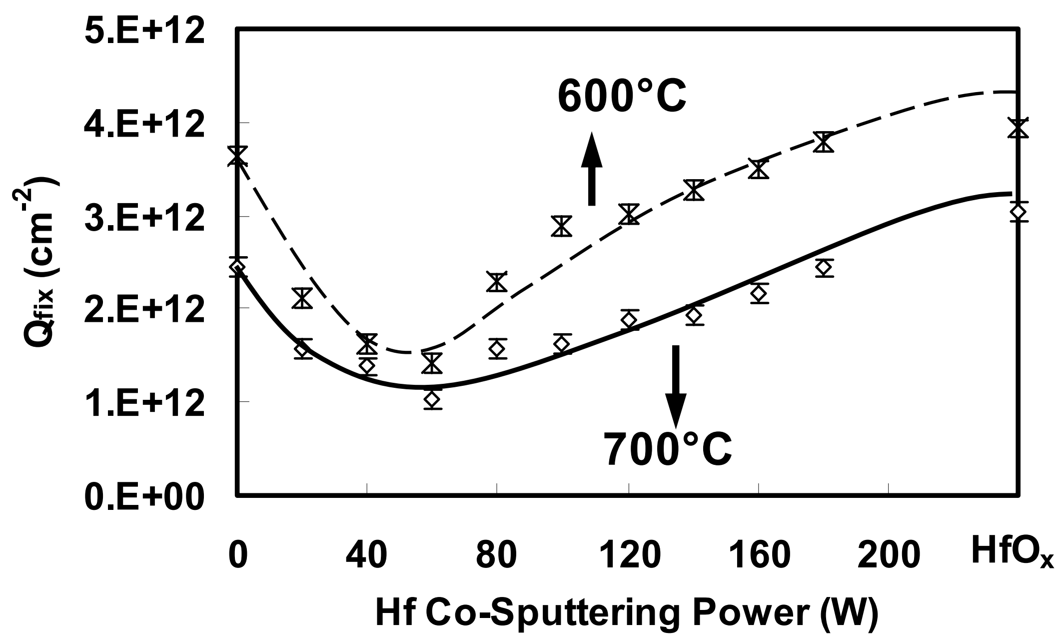
these films. Figure 32 (b) shows the fixed charge density (Q_{fix}) calculated based on the following equation, [54]

$$V_{FB} = \phi_{MS} - \frac{Q_{fix}}{C_{ox}} \qquad [16]$$

where V_{FB} is the flat band voltage extracted from the C-V curves; ϕ_{MS} is the difference of work function between the Al gate and Si substrate, i.e., -0.8 V; C_{ox} is the accumulation capacitance per unit area. Figure 32 (b) shows Q_{fix} as a function of Hf co-sputtering power. For both 600°C and 700°C PDA temperature, the lightly Hf doped film, e.g., Hf/(Hf+Ta) ~0.25-0.49, has the lowest Q_{fix} of $\sim 1\times 10^{12}$ cm^{-2}. The decrease of the fixed charge density is related to the bond structure in the film. For example, it was reported the flat band voltages of Ta_2O_5/Al_2O_3 and HfO_2/Al_2O_3 mixed oxides shifted to a more positive direction than their respective composing oxides.[125] Both positive and negative flat band voltage shifts have been observed in HfO_2 dielectric under various fabrication processes. [110, 130] The amount of positive fixed charge density may be minimized at a certain Hf dopant concentration due to charge compensation.[1, 131] In addition, the 700°C annealing sample exhibited a lower fixed charge density than the 600°C annealed samples irrespective of the Hf dopant concentration. This is because the higher annealing temperature is more efficient in reducing the positive charge, e.g., by fixing oxygen vacancies and dangling bonds, than the lower annealing temperature [64, 111]



(a)



(b)

Figure 32 (a) Terminology for charges in the MOS structure, (b) fixed charge density vs. Hf co-sputtering power after 600ºC and 700ºC O_2 annealing.

Figure 33 shows the C-V curves of the Hf (20W)-doped TaO_x films annealed at 600°C and 700°C. A counter-clockwise hysteresis is observed after a forward-and-reverse voltage sweep from –3V to +3V. The hysteresis is attributed to the negative oxide charge trapping in the bulk high-k films.[104] For the 600°C O_2 annealed sample, hysteresis of about 100mV was observed. It was lowered to about 30 mV after the 700°C O_2 annealing. The charge trapping can be greatly reduced by 700°C O_2 post-deposition annealing. The oxide charge trapping density (Q_{ot}) of the Hf (20W)-doped TaO_x is $5.0\times10^{11}cm^{-2}$ for 600°C annealed samples and $1.56\times10^{11}cm^{-2}$ for 700°C annealed samples. High temperature annealing can effectively reduce the defects caused by the plasma deposition process. [132] A similar trend was obtained in all other Hf-doped and un-doped TaO_x samples.

Figure 34 shows the interface state density (D_{it}) of doped and un-doped TaO_x samples vs. the Hf co-sputtering power. The D_{it} was extracted from C-V curves at flat-band voltage by using Lehovec's method.[133] For all doped and un-doped samples, the D_{it} values are in the range of $1\sim2\times10^{12}$ $cm^{-2}eV^{-1}$. Neither the Hf doping concentration nor the annealing temperature has noticeable effects on the D_{it}. In the previous section of the SIMS and HRTEM analysis, it has been demonstrated that a $HfSi_xO_y$-like interface layer was formed between Hf-doped TaO_x film and Si substrate after high temperature annealing. Since the interface properties of the $HfSi_xO_y$-Si are similar to those of the SiO_x-Si interface layer, the D_{it} can be independent of the Hf doping concentration. In addition, the 700°C annealed samples always exhibited a slightly lower D_{it} than 600°C annealed samples of the same Hf doping concentrations, which can be attributed to the formation of a high quality interfacial layer after a higher annealing temperature.[134]

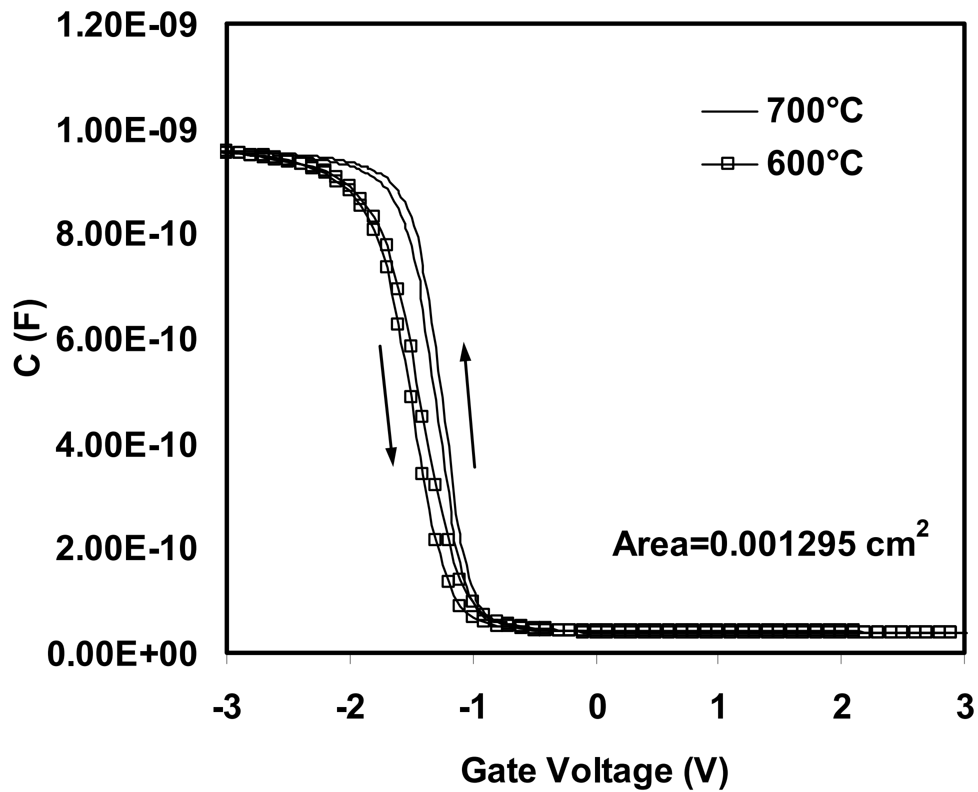


Figure 33 1MHz C-V curves of Hf (20W)-doped TaO_x films. The curve with a solid line represents the 700°C annealed samples, and the curves with a solid line and squares represent the 600°C annealed samples.

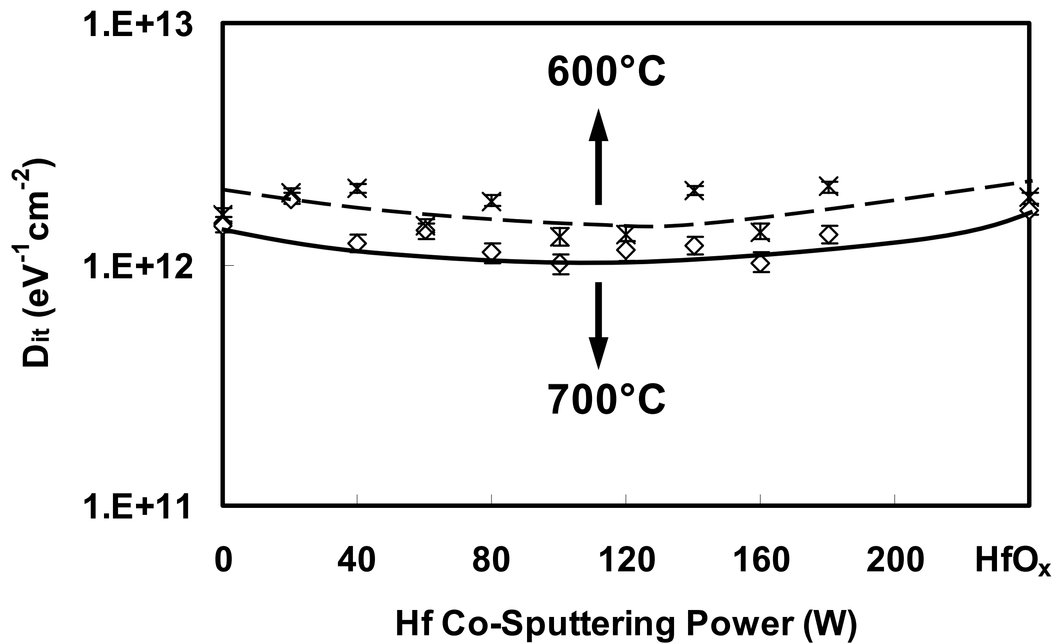


Figure 34 Interface State Density vs. Hf co-sputtering power after 600ºC and 700ºC O_2 annealing.

3.4.3. Influence of the Dopant Concentration on Leakage Current and Breakdown Phenomena

The I-V curves of all these Hf-doped TaO_x capacitors were measured at both the accumulation region (negative bias) and the inversion region (positive bias). Figure 35 shows the current density (J) vs. electric field (E) curves of all films are asymmetric except at the low bias field, e.g., between -1 MV/cm and 1 MV/cm. The leakage current densities in the inversion region are generally lower than those in the accumulation region. The leakage current densities tend to saturate at high electric fields under positive gate voltage for all of the Hf-doped TaO_x films. This is mainly attributed to the limited amount of available minority carrier (electron) densities in the space charge region of the p-type silicon substrate.[135-136]

Fig.35 (a) also shows that for the un-doped TaO_x samples, an abrupt breakdown occurs at –4.5MV/cm. However, no breakdown was observed for the lightly and moderately Hf-doped TaO_x films, i.e., Hf sputtering power at a range of 20~80W. However, breakdown occurs again for the films with higher Hf co-sputtering powers, e.g., Hf sputtering power higher than 100 W as shown in Fig. 35 (b). Therefore, an appropriately Hf-doped TaO_x film exhibits a higher dielectric strength than un-doped TaO_x and the heavily Hf-doped TaO_x film. Similar results are also obtained on 600°C annealed samples. More severe breakdown phenomena were observed for 600°C annealed samples. The film's breakdown strength is consistent with its fixed charge density, i.e., the low Q_{fix} sample has a high breakdown strength. A high-k film with a high defect charge density may easily form a conductive breakdown path in the high-k stack due to the charge trapping. Therefore, samples with a high Q_{fix} breakdown at a

relatively low electrical field. Another contributing factor for the early breakdown of the heavily Hf-doped TaO_x films is the interface layer. For example, the heavily doped high-k film has a thinner interface layer with a different composition from the lightly doped film.

Figure 36 shows the leakage current density (J) at -1 MV/cm as a function of Hf co-sputtering power after 600°C and 700°C annealing. The leakage current densities of the 600°C annealed samples are slightly higher than those of the 700°C annealed samples. The reduction of leakage current density at high temperature annealing is consistent with the reduction of the defect charge density. As discussed in the previous section, both the fixed charged density and the oxide trap decrease with the increase of the annealing temperature. The leakage current density slightly decreases with the increase of the Hf dopant concentration. This may be attributed to the change of the electron barrier height of the film. The relatively small reduction of the leakage current density with the doping process is consistent with the film morphology, which remains amorphous after 700°C 10 minutes annealing. Although it was reported Ta_2O_5 and HfO_2 crystallized at relatively low temperatures, the thin film at this thickness is difficult to crystallize because of the surface energy hindrance.[114]

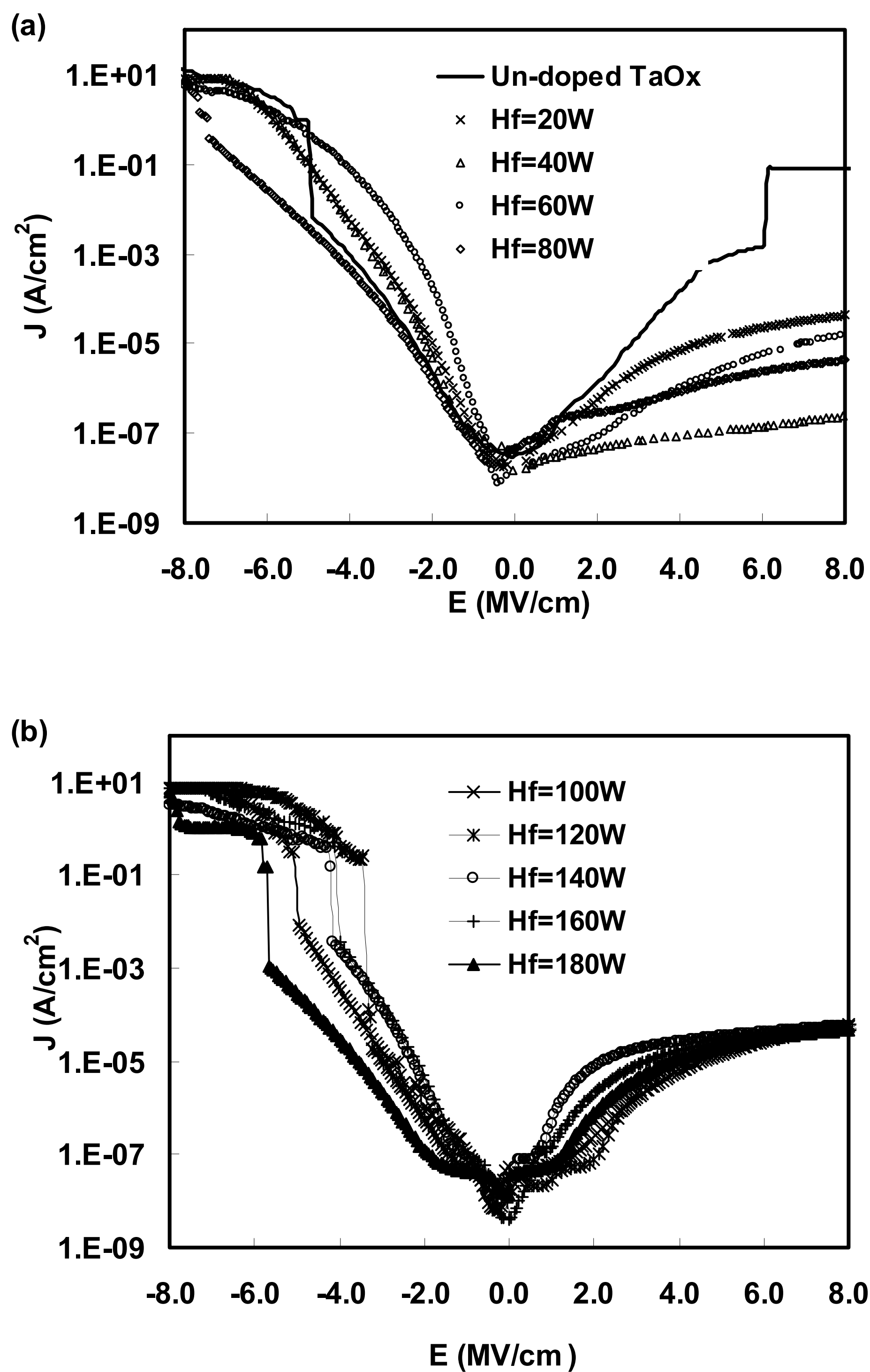


Figure 35 I-V curves of the (a) un-doped TaOx and lightly/moderately Hf-doped TaO_x films, (b) heavily lightly Hf-doped TaO_x films, after 700ºC-10 min O_2 annealing.

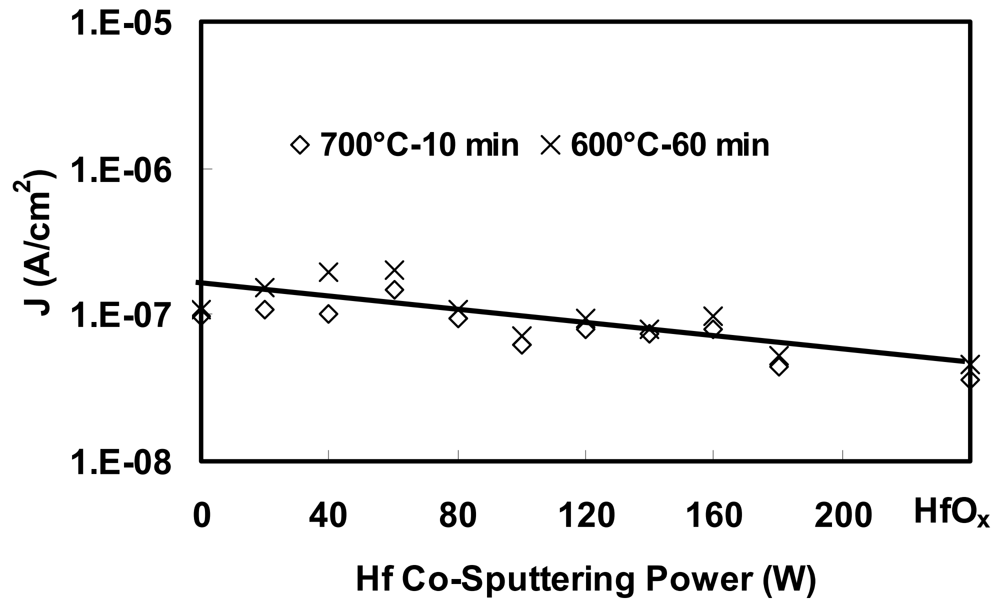


Figure 36 Leakage current density at –1MV/cm vs. the Hf co-sputtering power annealing conditions after 600°C and 700°C O_2 annealing.

3.5 Summary

Material and electrical properties of Hf-doped TaO_x thin films deposited by the RF reactive co-sputtering were studied by XPS, SIMS, HRTEM, C-V, and I-V. Influences of process parameters, e.g., Hf co-sputtering power, post-deposition annealing temperature, and annealing time, to high-k properties were investigated. The Hf dopant affects both the bulk and interface structures of the TaO_x film. The XPS and SIMS data showed the binding energy shifts and the composition changes with the dopant concentration. The doping process reduced the interface layer thickness, too. The moderately and heavily Hf-doped TaO_x thin films formed thinner interface layers at the silicon contact region than the un-doped TaO_x or lightly Hf-doped TaO_x films. The annealing time affected the interface layer thickness change more pronouncedly at the short period than at the long period. The incorporation of Hf into TaO_x impacted the electrical properties. The doping process improved the effective dielectric constant, reduced the fixed charge density, and increased the better dielectric strength. The leakage current density in the film decreased with the Hf concentration. However, the heavily Hf-doped TaO_x film suffered from the low dielectric breakdown strength and its dielectric constant was slightly higher than that of the un-doped TaO_x film. High temperature post-deposition O_2 annealing effectively reduced the defect charges in the high-k stack structures. In summary, the Hf-doped TaO_x films have many advantages over the un-doped TaO_x and HfO_x films. Therefore, doping is a promising method in preparing high quality gate dielectric materials for future generation CMOS devices.

CHAPTER V

HAFNIUM-DOPED TANTALUM OXIDE HIGH-K GATE DIELECTRIC WITH SUB-2 NM EQUIVALENT OXIDE THICKNESS

4.1 Introduction

In chapter III, it was reported that when Ta_2O_5 film was doped with hafnium (Hf), many of its physical and electrical properties, such as the amorphous-to-polycrystalline transition temperature, interface layer quality, k_{eff}, dielectric breakdown strength, and leakage current density, improved. For the Hf-doped TaO_x films, the optimized dielectric properties were achieved at a Hf/ (Hf+Ta) ratio of ~0.25. For future MOSFET gate dielectric applications, the equivalent oxide thickness (EOT) of the high-k film should be small, e.g., less than 2 nm. In this chapter, the feasibility of preparing the Hf-doped tantalum oxide into an ultra-thin film under various post-deposition annealing (PDA) atmospheres will be investigated.

4.2 Experimental

The Hf-doped TaO_x thin film was deposited on a p-type (100) Si wafer by reactive co-sputtering using separate Ta and Hf targets in a 1:1 Ar/O_2 gas mixture at 5mTorr and room temperature. The sputter powers of the Ta and Hf targets were fixed at 100W and 20W, separately. The Hf/ (Hf+Ta) atomic ratio of the film was kept constant, i.e., 25%. The PDA process was carried out under an O_2 or N_2 atmosphere at 700°C for 5 minutes

in a quartz tube. About 200nm of aluminum (Al) was sputter deposited through a shadow mask to the high-k surface to form the gate electrode. The backside of the wafer was also deposited with Al for better contact. The post-metal annealing (PMA) process was done at 300°C for 30 minutes in the forming gas (H_2:N_2 = 1:9) atmosphere. The film's physical thickness was measured with a Rudolph i1000 ellipsometer, which was confirmed with the transmission electron microscopy (TEM) picture. The chemical bond structure and composition of the bulk and interface layers were characterized with the angle resolved X-ray photoelectron spectroscopy (ARXPS). Electrical properties of the capacitors were calculated from capacitance-voltage (C-V) and current-voltage (I-V) data collected using an Agilent 4284A precision LCR meter and a 4140B pico-Ampere meter, separately.

4.3 Electrical Properties of sub-5nm Hf-doped TaO_x

4.3.1. Capacitance-Voltage (C-V) Characteristics

Figure 37 shows the C-V curves of 4.2-nm and 5.0-nm thick Hf-doped TaO_x films with N_2 or O_2 PDA atmospheres. Films with the same physical thickness exhibit different capacitances when they are annealed under different atmospheres. The O_2 annealed sample always yields a higher EOT than the N_2 annealed sample. For example, the 4.2-nm thick film has an EOT of 1.3 nm under a N_2 PDA atmosphere but 1.6 nm under an O_2 PDA atmosphere. The 5.0-nm thick film has an EOT of 1.48 nm under a N_2 PDA atmosphere but 1.86 nm under an O_2 PDA atmosphere.

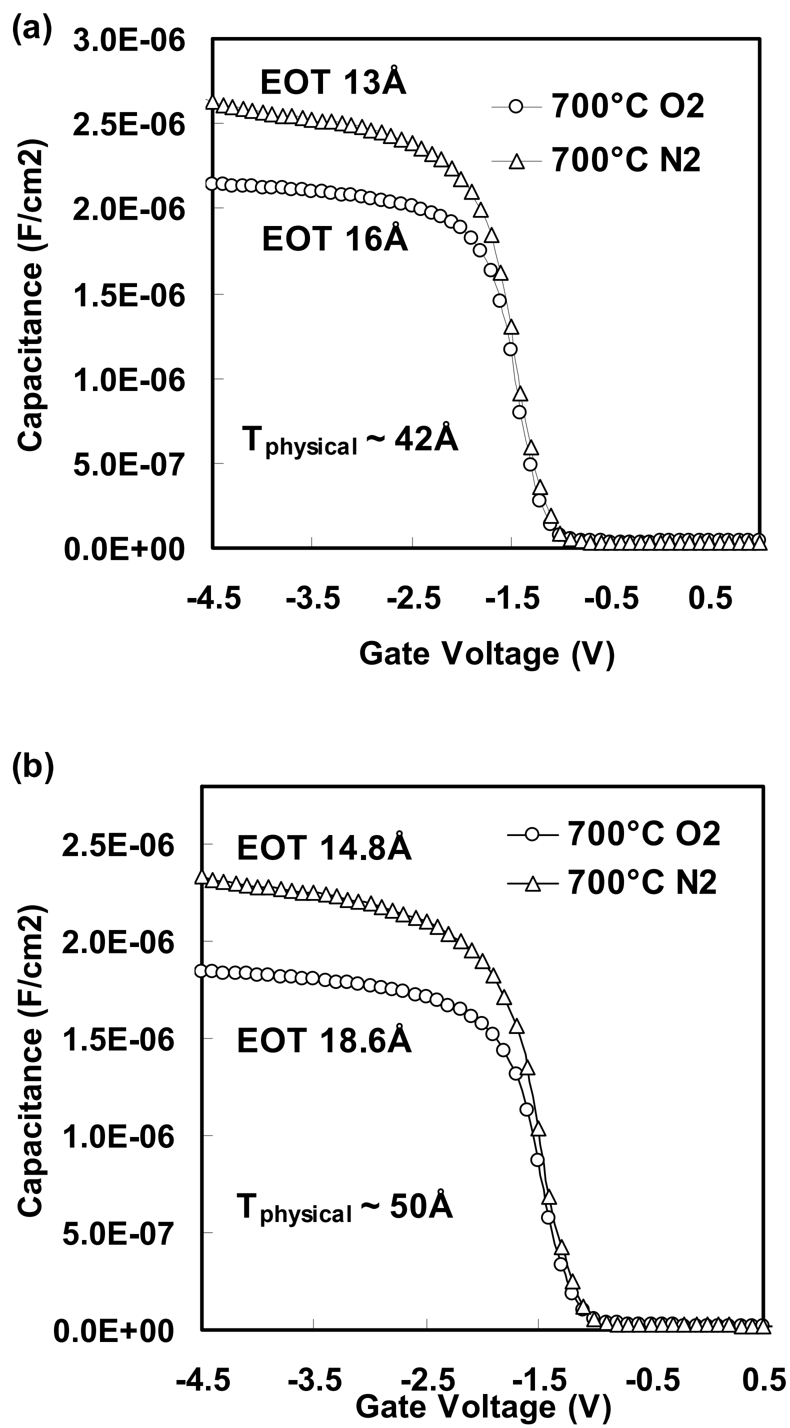


Figure 37 100KHz C-V curves after N_2 and O_2 annealed samples: (a) 4.2- nm thick film, (b) 5-nm thick film.

Figure 38 is a plot of the EOT vs. physical thickness. The linear relationship between the EOT and the physical thickness allows for the extraction of the bulk film's k value, i.e., from the slope, and the interface layer EOT, i.e., from the y-intercept.[137] The k value of the bulk high-k film is 29.2 for a N_2 annealed sample and 27.8 for an O_2 annealed sample. They are higher than those of an un-doped HfO_2 or Ta_2O_5 film, i.e., 21~26.[1] The higher dielectric constant of the doped bulk film may be attributed to factors such as changes of molar polarization, molar volume, or local bond coordination.[1,117,126]

Figure 38 also shows that the N_2 annealed sample has a thinner interface layer EOT than the O_2 annealed sample i.e., 0.9 nm vs. 1.1 nm. Both interface layer EOTs are lower than their physical thicknesses, i.e., 2.0~2.2 nm determined from TEM pictures. Therefore, the k value of the interface layer formed between the Hf-doped TaO_x film and the Si wafer is higher than that formed between the un-doped Ta_2O_5 and Si, i.e., 8~9 vs. 3.9. The formed interface is probably a silicate, such as $HfSi_xO_y$ that has a k value of 8~9.[116, 137-138]

The interface state density (D_{it}) of these samples was calculated from the C-V curves using the Lehovec method. Figure 39 shows the variation of the interface state density D_{it} as a function of film thickness. With the increase of the film thickness, the interface state density of the Hf-doped TaO_x high-k stack drastically decreased after both O_2 and N_2 annealing. Similar trends were also observed for the Zr-doped TaO_x high-k stack structures with different metal gate electrodes, which was attributed to the influence of metal gate sputtering deposition on the underlying high-k film.[139] In addition, O_2 annealed samples always exhibited a low D_{it} than N_2 annealed samples of the same

thickness. Therefore, the ultra-thin high-k film's electrical properties are sensitive to the PDA atmosphere.

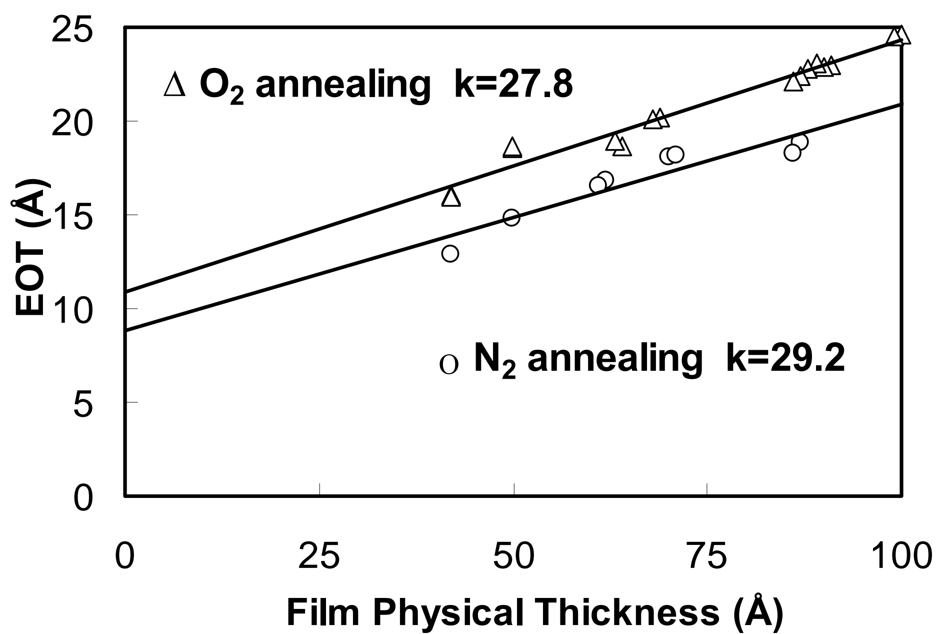


Figure 38 EOT vs. physical thickness plot. The linear relationship between the EOT and the physical thickness allows for the extraction of the bulk film's k value, i.e., from the slope, and the interface layer EOT, i.e., from the intercept to the y-axis.

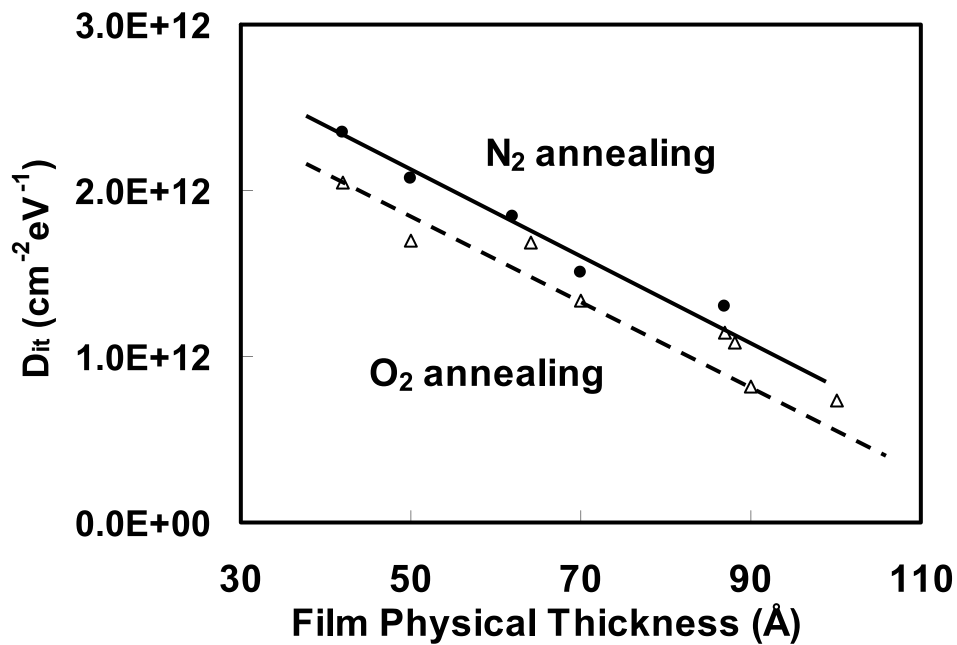


Figure 39 Interface state densities D_{it} of Hf-doped TaO_x vary as a function of film thickness. The interface state density (D_{it}) of these samples was calculated from the C-V curves using the Lehovec method.

4.3.2. Current-Voltage (I-V) Characteristics

Figure 40 shows the J-V curves of the 4.2nm thick films annealed under different ambient. At the negative bias voltage, the O_2 annealed film has a lower leakage current than the N_2 annealed film, i.e., by two orders of magnitude in the accumulation region. At the positive bias voltage, the same trend is also observed. However, the leakage current in the strong inversion region is saturated and independent of the annealing atmosphere mainly due to the limited amount of minority carrier (electron) densities in the p-type silicon substrate. The N_2 annealed films always exhibit a higher leakage current density than the O_2 annealed film of the same physical thickness.

Figure 41 is the leakage current densities measured @ V_{FB}-1 V of various film thicknesses annealed under an O_2 or N_2 atmosphere. Fig. 41 shows that 1) the leakage current increases with the film's physical thickness, and 2) the N_2 annealed film has a higher leakage current density than the O_2 annealed film based on the same physical thickness. The high leakage current of the N_2 annealed film can be attributed to its lower EOT.

Figure 42 shows variations of the leakage current @ V_{FB}-1 V as a function of EOT. The leakage current decreases with the EOT. The slope of N_2 annealed samples is larger than the O_2 annealed samples, implying a high leaky characteristic possibly due to the existence of the Ta sub-oxide as discussed in later sections. The high leakage current of the N_2 annealed film can be attributed to its thinner interface layer thickness. However, compared to the poly-Si-SiO_2 with the same EOT, both of the N_2 annealed and O_2 annealed samples exhibit a lower leakage current density by more than three orders of magnitude.

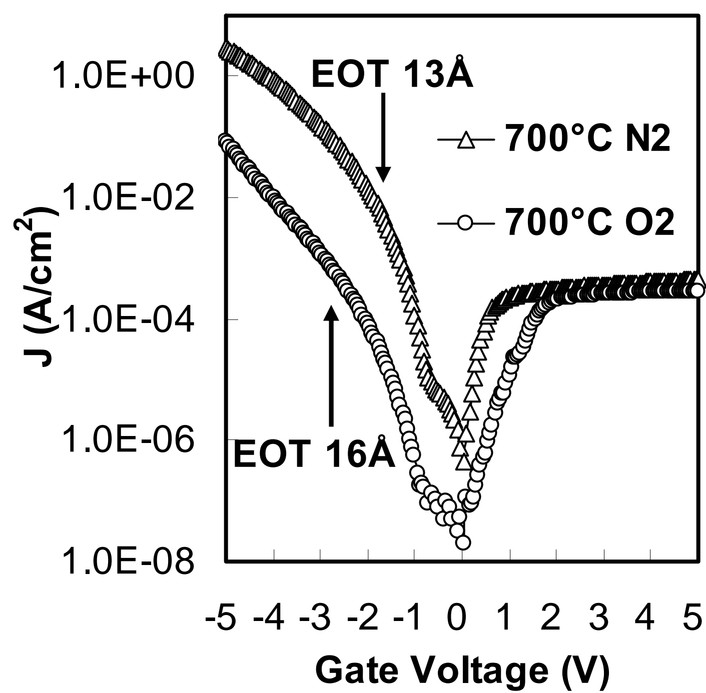


Figure 40 J-V curves of 4.2-nm thick films after N_2 and O_2 annealing.

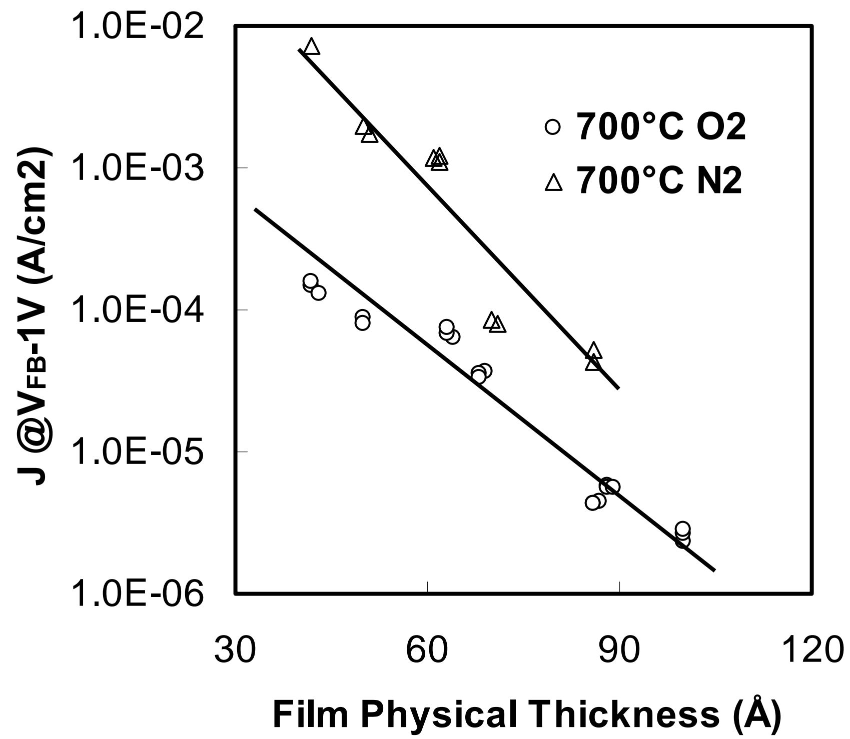


Figure 41 Leakage current densities measured at V_{FB}-1V of various film thicknesses annealed under O_2 or N_2 atmosphere.

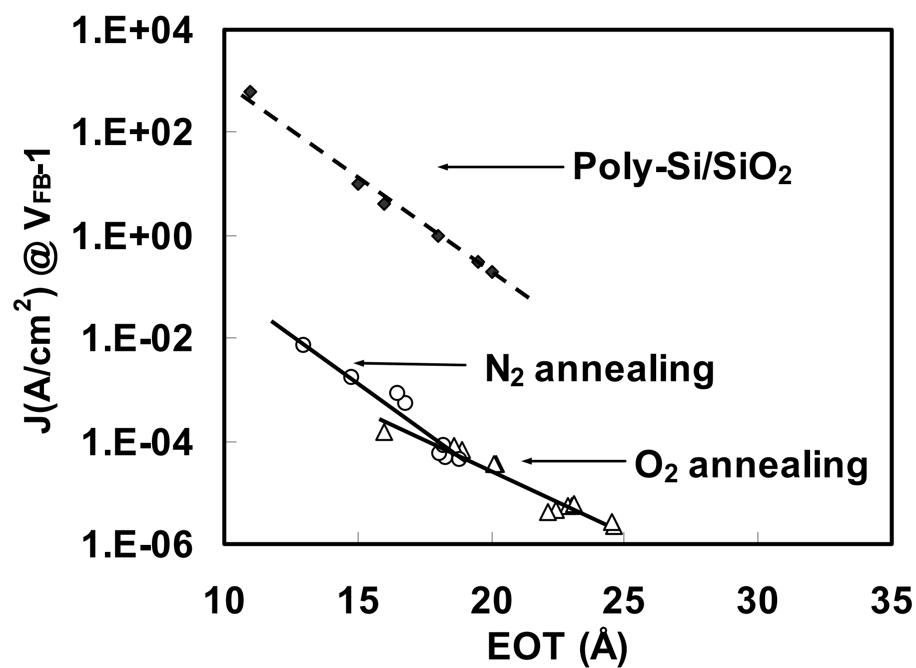


Figure 42 The leakage current densities of various samples @ V_{FB}-1 V vary as a function of EOT.

4.4 Material Properties of sub-5 nm Hf-doped TaO_x

Figure 43 shows an XPS spectra of the 4.2-nm thick Hf-doped TaO_x sample after O_2 annealing. Fig.43 (a) shows that the Ta with the $4f_{7/2}$ peak binding energy (BE) of 26.4 eV was fully oxidized without a silicide or sub-oxide shoulder. Fig.43 (b) shows the Hf 4f spectra at 90° (vertical to surface) and 30° grazing angles. The Hf $4f_{7/2}$ peak was deconvoluded into two peaks, i.e., 16.9 eV and 17.6 eV. The former peak corresponds to the HfO_2 compound and the latter peak corresponds to the $HfSi_xO_y$ compound. [116, 137-138] The intensity ratio of the latter peak to the former peak decreases with the decrease of the grazing angle. Therefore, $HfSi_xO_y$ is located near the Si interface region rather than in the bulk layer. This is consistent with SIMS and other analytical results reported by various groups. [121,137-138] The $HfSi_xO_y$ interface layer is also consistent with its high-k value observed in Fig.38.

Figure 44 shows XPS spectra of the same high-k film as Fig. 43 except the N_2 PDA environment. Fig.44 (a) shows the Ta $4f_{7/2}$ peak is composed of a main peak at 26.5 eV and a small peak at 25.6 eV. The former corresponds to fully oxidized Ta_2O_5 and the latter corresponds to the tantalum sub-oxide, i.e., TaO_x $x<2.5$. The intensity ratio of the sub-oxide peaks to the full oxide peaks in Fig.44 (a) is almost independent of the grazing angle. Therefore, the Ta sub-oxide exists in the bulk film. The Hf $4f_{7/2}$ peak in Fig. 44 (b) could also be deconvoluded into two peaks similar to those in Fig.43 (b). The absence of low BE peaks suggests that the film does not contain Hf sub-oxide (HfO_x $x<2$) or silicide (Hf-Si). Therefore, in the N_2 annealed sample, Hf is easier to oxidize than Ta. This can be explained by the low electronegativity of Hf compared with Ta, i.e., 1.3 vs. 1.5.[117] The intensity ratio of $HfSi_xO_y$ to HfO_2 in Fig. 44 (b) is higher than that in Fig. 43 (b), i.e., 0.65

vs. 0.35 at the grazing angle of 90°. Therefore, the N_2 annealed film has a higher Hf concentration at the high-k/Si interface than the O_2 annealed film.

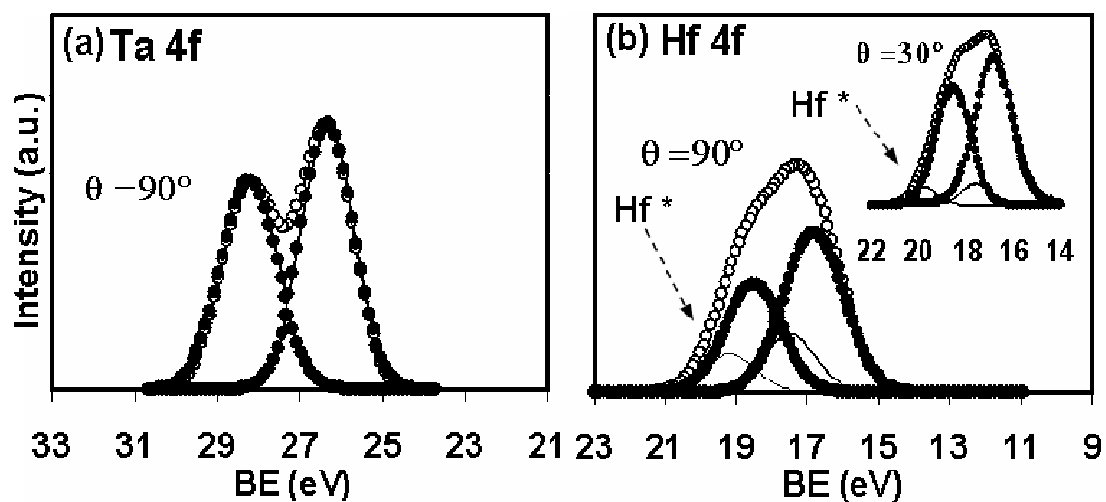


Figure 43 ARXPS spectra of 4.2-nm thick O_2 annealed Hf-doped TaO_x sample (a) Ta 4f at grazing angle of 90°, (b) Hf 4f at grazing angles of 90° and 30°.

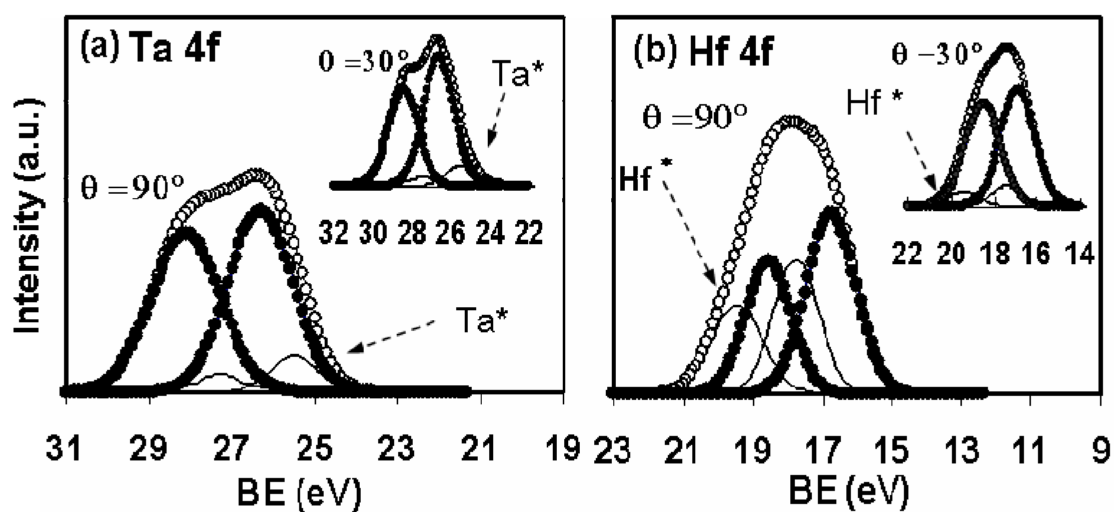


Figure 44 ARXPS spectra of 4.2-nm thick N_2 annealed Hf-doped TaO_x sample (a) Ta 4f at grazing angles of 90° and 30°, (b) Hf 4f at grazing angles of 90° and 30°.

Figure 45 (a) shows Si 2p spectra of the 4.2-nm thick Hf-doped TaO_x films with PDA under O_2 and N_2 atmospheres. Both Si peaks can be deconvoluded into three peaks, i.e., BEs of 99.6 eV, 102.6 eV, and 103.5 eV. The first peak is the Si-Si bond from the silicon wafer. The second peak is higher than the Si^{3+} bond and can be contributed to SiO(Hf) in the $HfSi_xO_y$ interface layer.[2,137-138] The third peak is the Si-O bond from SiO_2. The SiO(Hf)/Si-O peak ratio of the N_2 annealed sample is lower than that of the O_2 annealed sample. Therefore, the interface layer of the O_2 annealed sample is closer to the SiO_2 structure than that of the N_2 annealed sample and the interface layer of the N_2 annealed sample is similar to $HfSi_xO_y$. This result is consistent with the D_{it} and EOT values of these two films as discussed in Fig. 39.

Figure 46 shows energy band gaps of un-doped Ta_2O_5 and Hf-doped TaO_x with different PDA atmospheres. The energy band gaps were estimated from the O 1s energy-loss spectra. [87,102] It is clear that the energy band gaps decreased in the order of O_2 annealed Hf-doped TaO_x (5.0 eV) > N_2 annealed Hf-doped TaO_x (4.8 eV) > O_2 annealed un-doped Ta_2O_5 (4.4 eV). A similar relation was detected using the internal photoemission spectroscopy, i.e., the Hf-Ta mixed oxide has a wider energy band gap than the un-doped Ta_2O_5.[140] The small energy band gap of N_2 annealed doped film can be attributed to the formation of a Ta sub-oxide.[141]

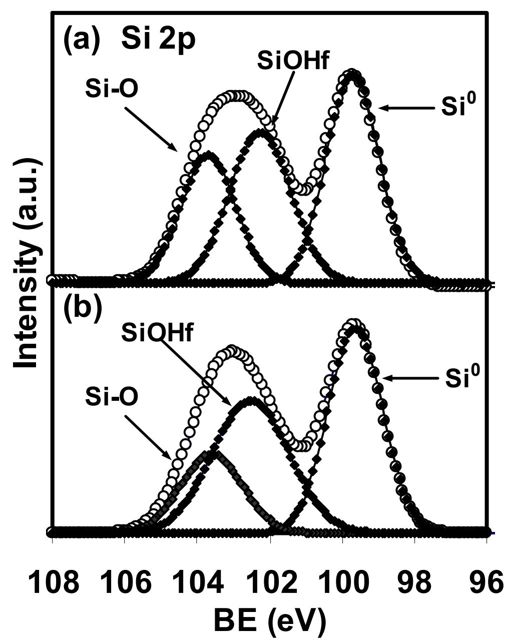


Figure 45 XPS Si 2p spectra at a 90° grazing angle of the 4.2-nm thick Hf-doped TaO_x samples after 700°C PDA under (a) O_2 and (b) N_2 atmosphere.

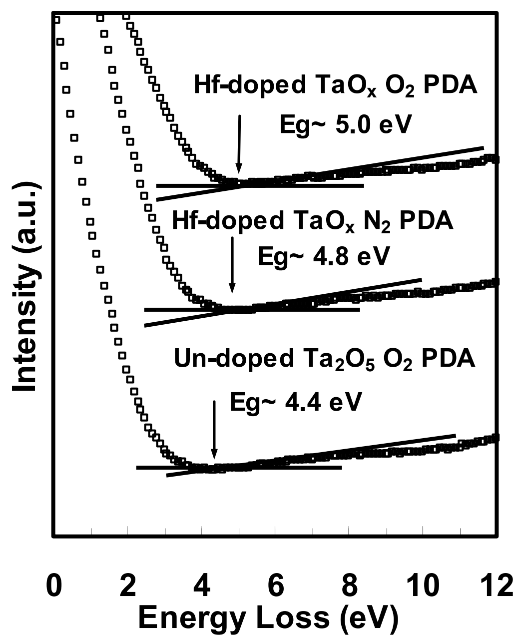


Figure 46 O 1s energy loss spectra for 10-nm thick Hf-doped TaO_x and un-doped TaO_x, the energy band gap values can be estimated from the onset of the loss peak increase.

4.5 Summary

Hf-doped TaO_x high-k films with sub-2 nm thick EOTs have been demonstrated and studied. The low leakage currents and high dielectric constants of the doped films were explained by their compositions and bond structures. The Hf-doped TaO_x film contains $HfSi_xO_y$ in the interface layer irrespective of the PDA atmosphere. However, the O_2 annealed film contains more oxidized bulk film and less silicate-rich interface layers. The energy band gaps in doped and un-doped films could be explained by the film structure. In summary, the Hf-doped TaO_x film is a potential high-k gate dielectric for future MOS transistors.

CHAPTER V

EFFECTS OF THE 5 Å TANTALUM NITRIDE INTERFACE LAYER ON HAFNIUM DOPED TANTALUM OXIDE HIGH-K FILMS*

5.1 Introduction

Ta_2O_5 is a promising high-k gate dielectric material due to its high dielectric constant and successful application in storage capacitors. However, Ta_2O_5 is thermally unstable when it is in contact with silicon. It forms an interfacial layer with poor electrical properties at an elevated annealing temperature. A lower than expected k value is observed on TaO_x film when the thickness is thin. Previous results show that some dielectric properties of Ta_2O_5 could be effectively improved by adding hafnium into the structure. However, the low quality SiO_x-type interface still exists. It was proposed that incorporation of nitrogen into the interfacial layer could suppress the formation of the SiO_x interface layer, which resulted in the increase of the overall capacitance or dielectric constant.[90, 112] However, the traditional silicon nitride or oxynitride interfacial layer does not have a very high k value and therefore, cannot contribute too much to the overall capacitance or dielectric constant of the capacitors.

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Its properties can be significantly influenced by its stoichiometry, microstructure, and deposition parameters.[142] For example, a non-stoichiometric tantalum nitride (TaN_x) thin film could be oxidized to nonconductive TaO_xN_y after high-temperature annealing in O_2.[143-144] Since the TaO_xN_y film has a high k value, e.g., approximately over 26, [93,145] the formation of this interfacial layer by oxidizing the TaN_x layer can contribute to the high effective k value ($k_{effective}$). The leakage current density could be lowered down, too. In this study, a 5 Å thin, non-stoichiometric TaN_x interface layer is inserted between the Hf-doped TaO_x film and Si substrate to interfere with the formation of the inferior SiO_x interface layer during the high temperature O_2 annealing process.

5.2 Experimental

Substrates used in this study were p-type (100) Si wafers (10-80 Ω·cm). A standard HF pre-clean step was performed prior to the loading of the bare Si wafer into the sputtering chamber. The 5 Å thick TaN_x film was then deposited by reactive magnetron sputtering using the Ta target at 5 mTorr and room temperature after a base pressure of 5×10^{-6} Torr was achieved. In order to improve the uniformity of the TaN_x layer, the deposition rate was purposely slowed by setting the flow rate ratio of Ar/N_2 gas mixture at 1:4. The Hf- doped TaO_x thin films were subsequently co-sputtered using two separate targets, i.e., Ta and Hf in a 1:1 Ar/O_2 gas mixture without breaking the vacuum. The HfO_x concentration in the bulk film was varied by changing the sputtering power of the Hf target between 20W and 100W, while the Ta-sputtering power was fixed at 100W. The film thickness can be controlled by adjusting the deposition time. The un-doped TaO_x and HfO_x films were also deposited to serve as references for the purpose of comparison. After deposition, the as-deposited films were annealed in a quartz tube at

600°C for 60 minutes or 700°C for 10 minutes under O_2. After annealing, about 4000Å-thick aluminum (Al) dots were deposited on the sample through a shadow mask to form the gate electrode of the metal-oxide-semiconductor (MOS) capacitor. After another 2000Å-thick Al layer was deposited on the backside of the Si wafer, the post-metal annealing was performed at 300°C for 30 min under N_2 or forming gas (90%N_2/10%H_2) at atmosphere.

The refractive index and the thickness of the film were determined by a Rudolph i1000 elliposometer. The total physical thickness of Hf-doped TaO_x films, with or without a TaN_x interface, was controlled at about 10nm for each sample. The film's electrical properties were determined from C-V and I-V measurements using a HP 4284A Precision LCR Meter at 1 MHz and a HP 4140B pico-Ampere Meter, separately. The $k_{effective}$ was extracted from the C-V curve in the accumulation region. The interfacial composition and chemical states were analyzed with Secondary Ion Mass Spectroscopy (SIMS) and Electron Spectroscopy for Chemical Analysis (ESCA).

5.3. Influence of TaN_x Interface Layer on Film's Electrical Characteristics

5.3.1. TaN_x Interface Layer Effect on $I_{leakage}$

I-V curves for all of these Hf-doped TaO_x capacitors were measured at both the accumulation region (negative bias) and the inversion region (positive bias), as shown in Figure 47. There is no abrupt change of the curve in these curves. All Hf-doped TaO_x films have lower leakage current densities than that of the undoped TaO_x film. The 80W Hf-doped film even has a lower leakage current density than that of the undoped HfO_x film.

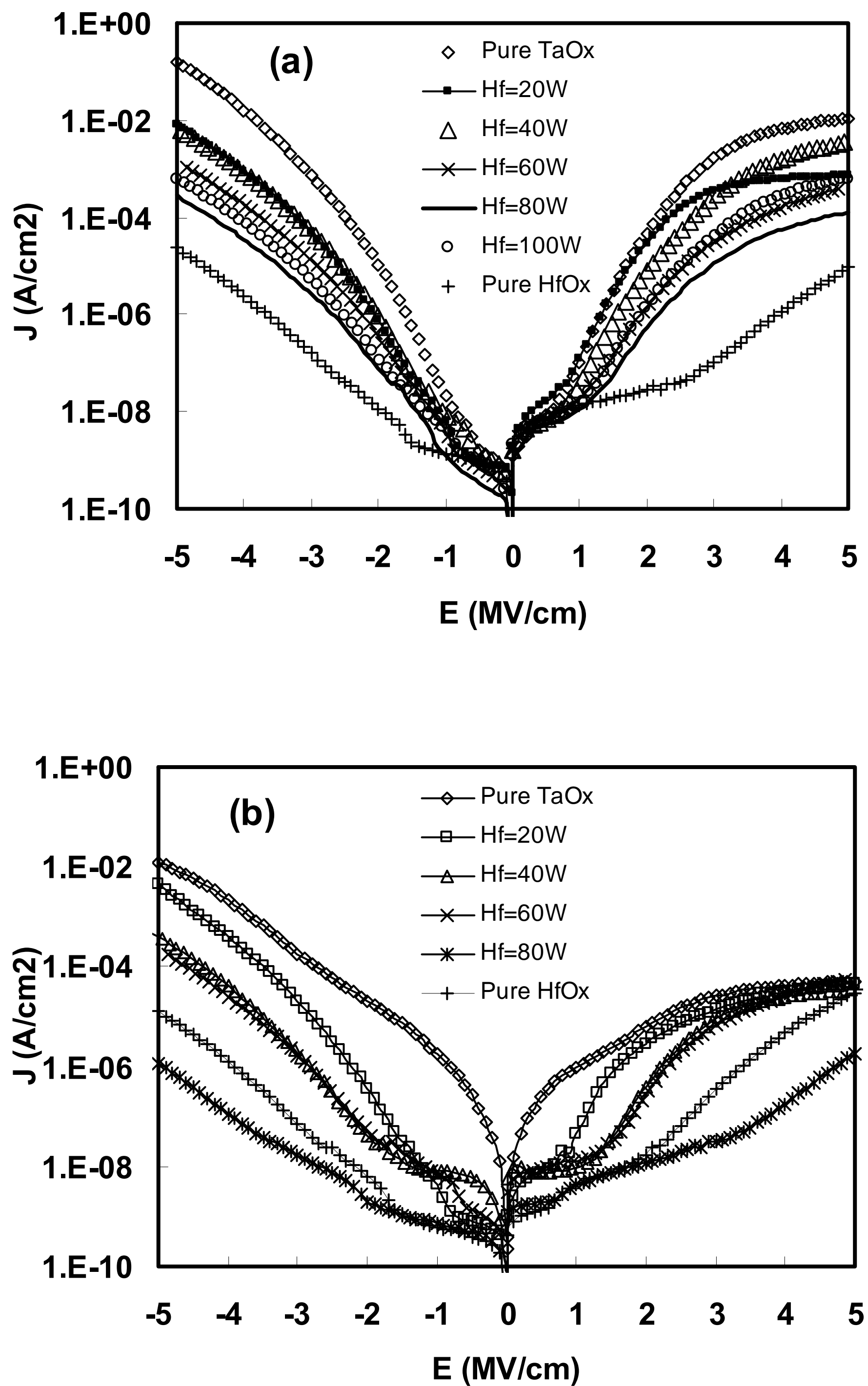


Figure 47 Leakage current density vs. electric field of Hf-doped TaO_x including a 5 Å thick TaN_x interface layer after (A) 600ºC-60 min O_2 annealing; (B) 700ºC-10 min O_2 annealing.

Figures 48 show the leakage current densities at –1 MV/cm of the gate field of the doped TaO_x films with and without the TaN_x interface layer. All the samples in the Fig. 48 (a) were annealed at 600 ºC for 60 minutes in O_2. All of the samples in Fig. 48 (b) were annealed at 700 ºC for 10 minutes in O_2. For Hf-doped TaO_x and pure HfO_2 films, the leakage current density is reduced to a factor of more than 10 regardless of annealing temperature. For undoped TaO_x, leakage current density slightly decreased for the film after the 600 °C-60 min annealing condition. The exact cause for the reduction of leakage current is complicated. It is possible that the incorporated nitrogen at the interfacial layer might be responsible for lowering the leakage current density by blocking the electron transport or varying the stress of the final film structure. Some other researchers observed the same improvement of the leakage current characteristics after the introduction of nitrogen into the interfacial layer, and they suggested that the reduction of leakage current density could be explained by a low trap density due to the incorporation of nitrogen into the oxide. [90,146, 147] Fig. 48 also shows that the reduction of the leakage current is enhanced with the increase of the Hf content in the films with the TaN_x interface layer, which is consistent with the fact that the HfO_2 film is less leaky than the Ta_2O_5 film.[112] Therefore, the Hf-doping effect on the leakage current density of the TaO_x film exists whether the TaN_x interface layer is added or not. For undoped TaO_x film with a TaN_x interface, an increase of leakage current density was observed under the 700ºC-10 min annealing condition. This increase may involve a complicated phase transition in bulk or interface layers because undoped TaO_x film has a relatively lower amorphous to polycrystalline transition temperature than that of doped TaO_x film.

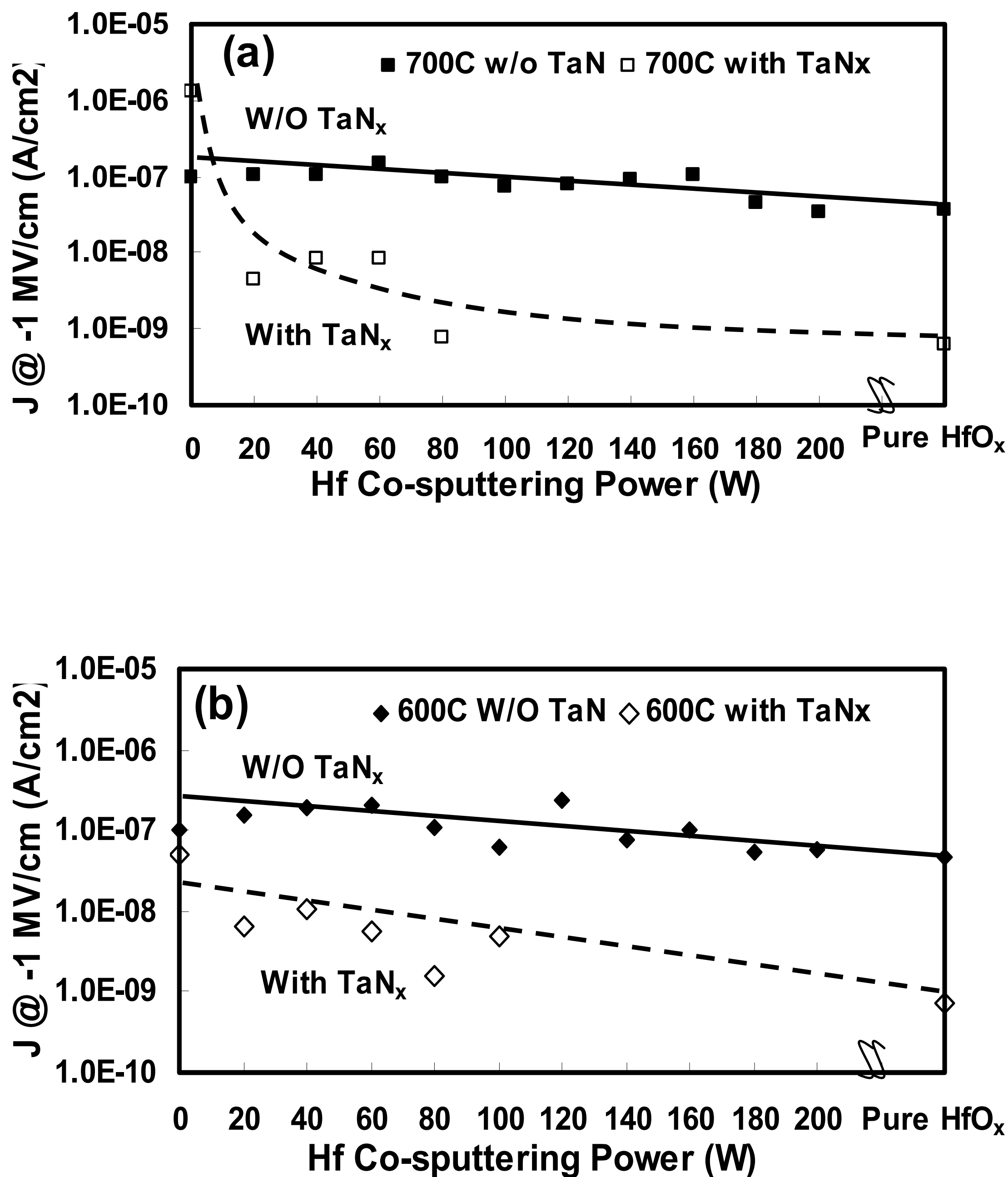


Figure 48 The leakage current densities at –1 MV/cm electrical filed of the Hf-doped TaO_x films with and without the TaN_x interface layer, (a) samples were annealed at 600ºC for 60 minutes in O_2, (b)samples were annealed at 700 ºC for 10 minutes in O_2.

5.3.2. Influence of the TaN_x Interface Layer on Breakdown Characteristics of Undoped TaO_x

It is well known that pure TaO_x thin films suffer a problem of low breakdown voltage. In this study, it was observed that the undoped TaO_x films without a TaN_x interface layer have abrupt breakdowns at both highly positive and negative biased conditions whether the film was annealed at 600°C or 700°C under O_2, while the film with the TaN_x interface layer does not have the breakdowns, as shown in figure 49. No abrupt breakdown was observed in other Hf-doped TaO_x or undoped HfO_2 thin films with a TaN_x interface layer either as shown in Fig. 47. There may be two explanations for the improvement of dielectric characteristics. First, the TaN_x interface layer was oxidized during the process of high temperature O_2 annealing and the interface layer was converted to TaO_xN_y. Since TaO_xN_y films form a thinner interface layer with the silicon wafer than TaO_x, smaller compressive stress will develop in the interface oxide layer.[93] The other explanation may be attributed to the incorporation of nitrogen into interfacial oxide during the high temperature O_2 annealing process. It was reported that dielectric properties of oxynitrides could be improved by incorporating nitrogen into a SiO_x/Si interface with bond states such as Si_2=N-O and Si_3=N, which are capable of reducing the strain at the SiO_x/Si interface and therefore decrease defect density and minimize charge traps.[148-149]

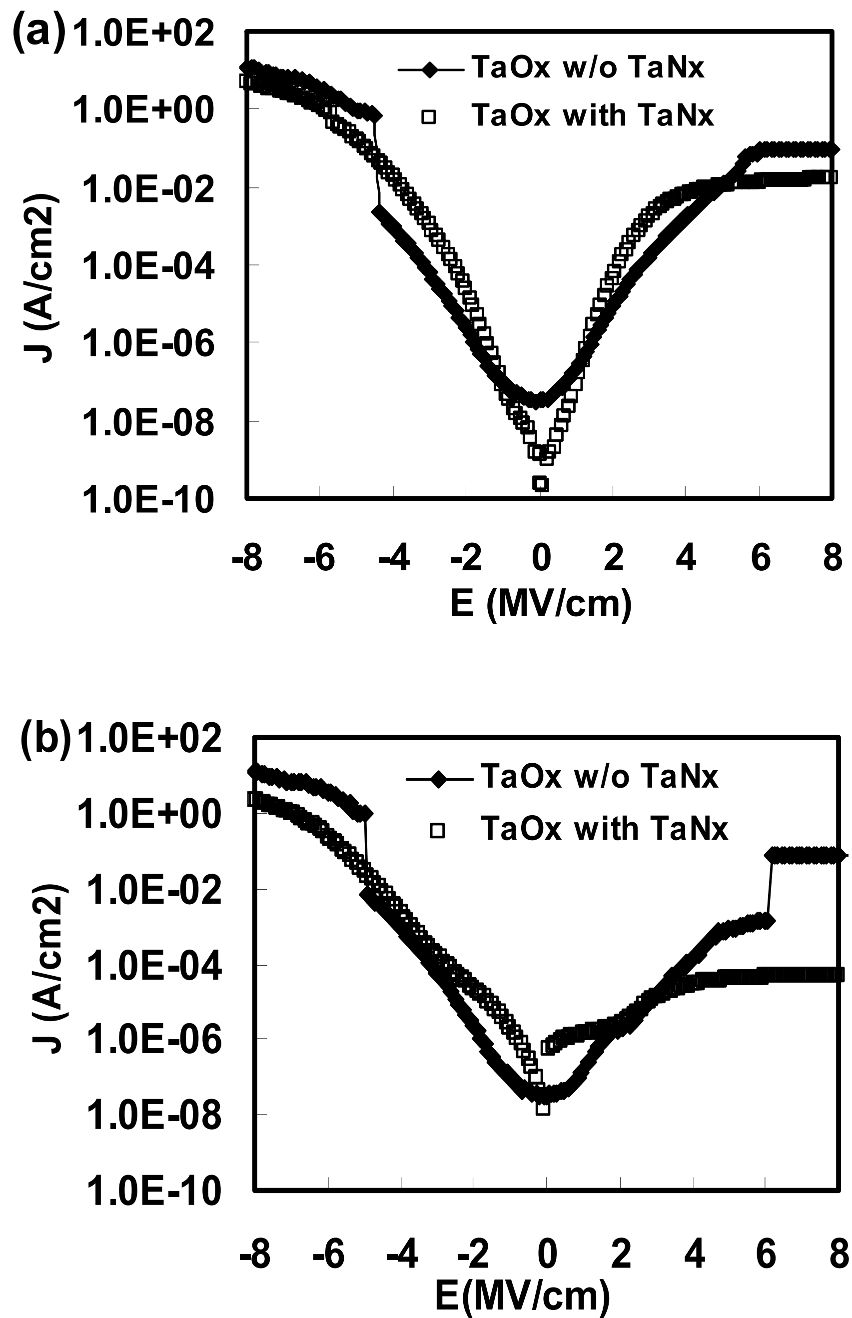


Figure 49 J-E curves undoped TaO_x films with or without the TaN_x interface layer after annealing at (a) 600ºC for 60 min and (b) 700ºC for 10 min under O_2.

5.3.3. Influence of both Hf dopant and TaN_x Interface Layer on the Leakage Current and Breakdown Characteristic of Hf-doped TaO_x

In the previous chapter, it was observed that the dielectric breakdown characteristic could be improved by slightly doping Hf into the TaO_x. In this study, it was observed that the insertion of a TaN_x interface layer can also improve the dielectric breakdown strength of the undoped TaO_x. Figure 50 shows the J-E curves of doped and un-doped TaO_x films. The undoped TaO_x film breaks down at a low electrical field of -5MV/cm. When the film is doped with Hf, there is no breakdown for up to -6MV/cm. The improvement of the dielectric breakdown strength was observed in the lightly Hf-doped films, such as at the Hf/ (Hf+Ta) ratio in the range of 0.24 and 0.49 from ESCA analysis. However, when the Hf concentration is high, the breakdown phenomenon was observed again. The improvement of the low breakdown at the low dopant concentration can be attributed to the better dielectric strength of HfO_2 compared with that of Ta_2O_5. The recurring breakdown phenomenon at the high dopant concentration is probably contributed by the early breakdown of the thinner interface layer. The leakage current densities of doped and un-doped TaO_x films are similar at the low negative electrical field range, which is in the accumulation region. With the insertion of the TaN_x interface, the leakage current density of Hf-doped TaO_x decreases by one order of magnitude in the accumulation region. The formation of the TaO_xN_y interface layer might play an important role for the dramatic decrease of the leakage current density. Previously, we also observed that the Hf-doped TaO_x film has a higher dielectric constant after the insertion of the TaN_x interface layer, which is probably also due to the formation of the new interface layer.

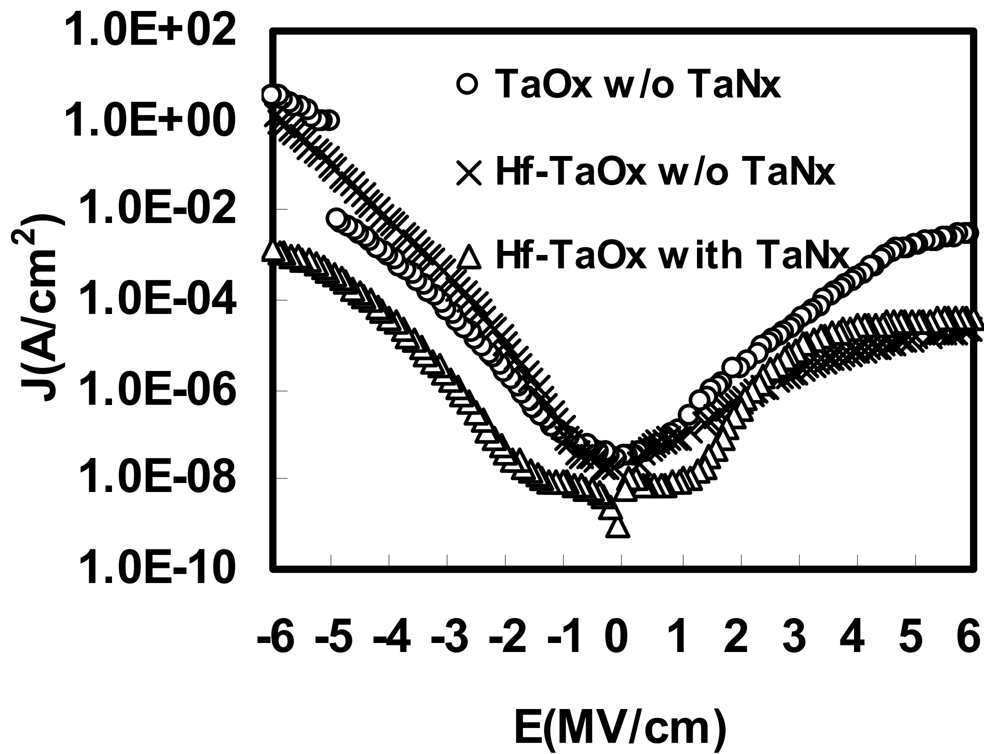
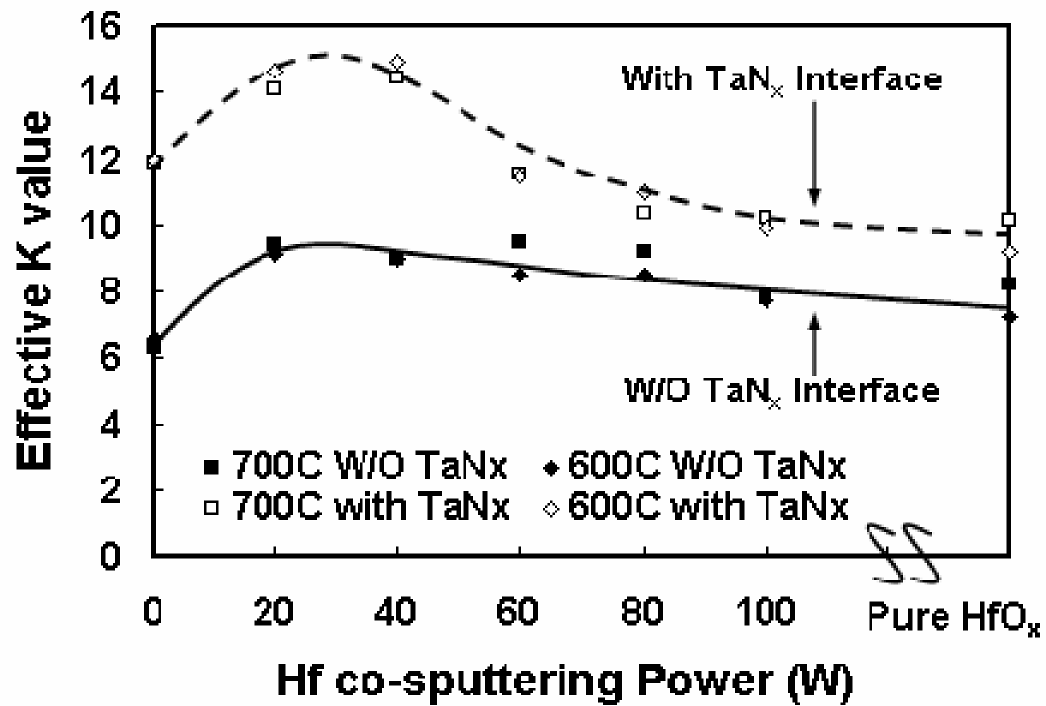


Figure 50 J-E curves of un-doped and lightly Hf-doped TaO_x films with and without an inserted TaN_x interface layer. All samples were annealed at 700 ºC for 10 minutes in O_2.

5.3.4. TaN_x Interface Layer Effect on k_{eff} Value

Figure 51 shows variations of the k_{eff} values of various Hf-doped TaO_x films with and without the TaN_x interface layer. In both cases, the physical thickness of the films is around 10 nm and the C-V measurement was performed at 1MHz. The effective dielectric constant k_{eff} was calculated from the maximum capacitance of the accumulation region without taking quantum mechanical effects into consideration. Annealing temperature (e.g., 600°C or 700°C) doesn't have major effects on the k_{eff} values for all Hf-doped TaO_x samples with or without the TaN_x interface layer. The k_{eff} value increases with the addition of the TaN_x interface layer for both Hf-doped and undoped TaO_x films. The increase can be explained by the TaN_x barrier effects on oxygen diffusion [150] and the formation of a thin interface TaO_xN_y insulating layer after high temperature O_2 annealing .[143-144] Since TaO_xN_y has a higher k value than that of the SiO_x film formed between the un-doped TaO_x and silicon wafer, e.g., over 26 vs. 4,[93, 145] the conversion of TaN_x to TaO_xN_y during high temperature O_2 annealing favored the increase of the overall dielectric constant. The similar increase of dielectric constant was also reported when silicon nitride or oxynitride was used as passivation interface layer. They attributed the improvement of the k_{eff} to the nitrogen's barrier effect on oxygen diffusion and the fact that silicon nitride or oxynitride has a twice dielectric constant k value than that of SiO_x.[1,90,112] In addition, the phenomenon of the anomalous enhancement of the k value of the film with the addition of a small amount of Hf, which was previously observed, is preserved with the existence of the TaN_x interface layer.



Figures 51 k_{eff} values vary as a function of Hf co-sputtering power of various Hf-doped TaO_x films with and W/O the TaN_x interface layer.

5.3.5. TaN_x Interface Layer Effect on Flat Band Voltage Shift

By comparing the measured flat band voltage (V_{FB}) with the ideal flat band voltage (V^o_{FB}), the flat band voltage shift (ΔV_{FB}) can be calculated. The ideal V°_{FB} is the difference of the work function between the metal gate and silicon substrate. In this case, the V°_{FB} is about –0.8V, assuming the Al gate work function of 4.1V and the substrate doping concentration is 10^{14}-$10^{15}/cm^3$. The measured V_{FB} is the corresponding voltage bias at the flat-band capacitance (C_{FB}) in the C-V curve. The C_{FB} can be determined by the following equation, [7]

$$C_{FB} = \frac{1}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{L_D}{\varepsilon_{Si}}} \qquad [17]$$

where L_D is the Debye length for the P silicon substrate with the doping concentration of N_a

$$L_D = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_a}} \qquad [18]$$

In most cases, ΔV_{FB} is attributed to the fixed charge in the dielectric film. Figure 52 shows that the flat band voltage shift increases negatively with the addition of the TaN_x interface layer after both 600°C and 700°C O_2 annealing, which suggests the increase of positive charges to the layered high-k gate stack structure. This observation is consistent with previous reports by other researchers that the C-V curve of the TaO_xN_y film has a more negative, e.g., by about 0.17 V, than that of the Ta_2O_5 film because of nitrogen induced positive charges to the interface.[93] Figure 51 also shows that a high temperature, e.g.700 ºC, can substantially decrease the voltage shift of the Hf-doped TaO_x film whether it has a TaN_x interface layer or not. However, the extra positive charges

introduced by the TaN_x interface layer cannot be totally eliminated at this temperature. Fig. 52 also shows that the lightly Hf-doped film has a lower flat band voltage shift than those of other doped or undoped films. The lowest shift occurs around the Hf co-sputtering range that has the highest k value, as shown in Fig. 51. Since this phenomenon happens independent of the existence of the TaN_x interface layer, other factors may be responsible for these phenomena. For example, the film with the highest k value and the lowest flat band shift may have the lowest stress among all of the films. The 5 Å TaN_x Interface layer may not have a major influence on the stress of the original film.

5.3.6. TaN_x Interface Layer Effect on Interface State Density (D_{it})

Figure 53 shows the D_{it} values of various Hf-doped TaO_x with and without the TaNx interface estimated at flat-band condition using the Lehovec method. The annealing temperature e.g., 600ºC or 700ºC, has negligible effects on the D_{it} for films doped with different Hf concentrations with or without the TaN_x interface. For all doped and un-doped samples without the TaN_x interface, the D_{it} values are in the range of $1\sim2\times10^{12}$ $cm^{-2}eV^{-1}$. For samples with the TaN_x interface, the D_{it} values are increased to the range of $2\sim8\times10^{12}$ $cm^{-2}eV^{-1}$. A similar phenomenon of increasing the D_{it} value with the insertion of a nitride interface layer was reported on the ZrO_2 film.[66] In addition, for the sample with the TaN_x interface, the D_{it} value increased slightly with the increase of the Hf co-sputtering power. Since the increase of D_{it} with Hf doping concentration is not observed for the sample without the TaN_x interface, the increase might be attributed to the stack layer structure, which affects its physical and chemical properties, such as stress, composition, and chemical states.

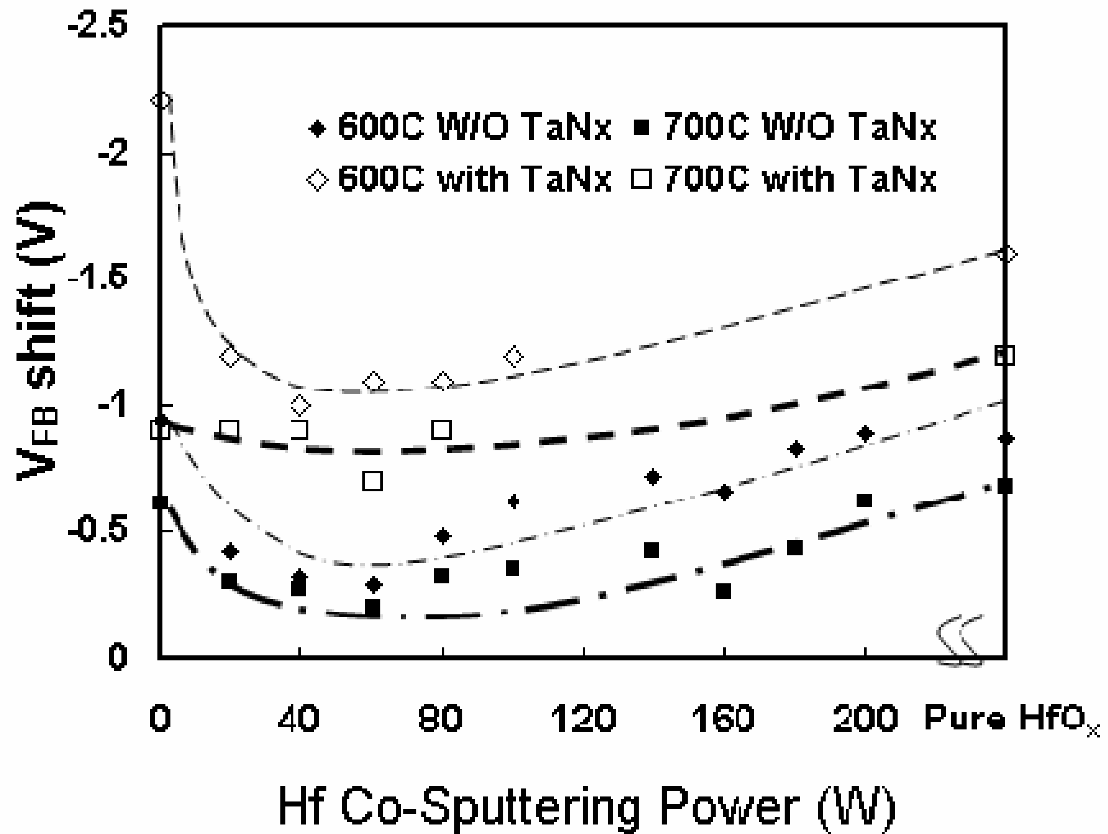


Figure 52 Flat-band voltage shifts of various Hf-doped films with and without the TaN_x after either 600ºC or 700ºC annealing.

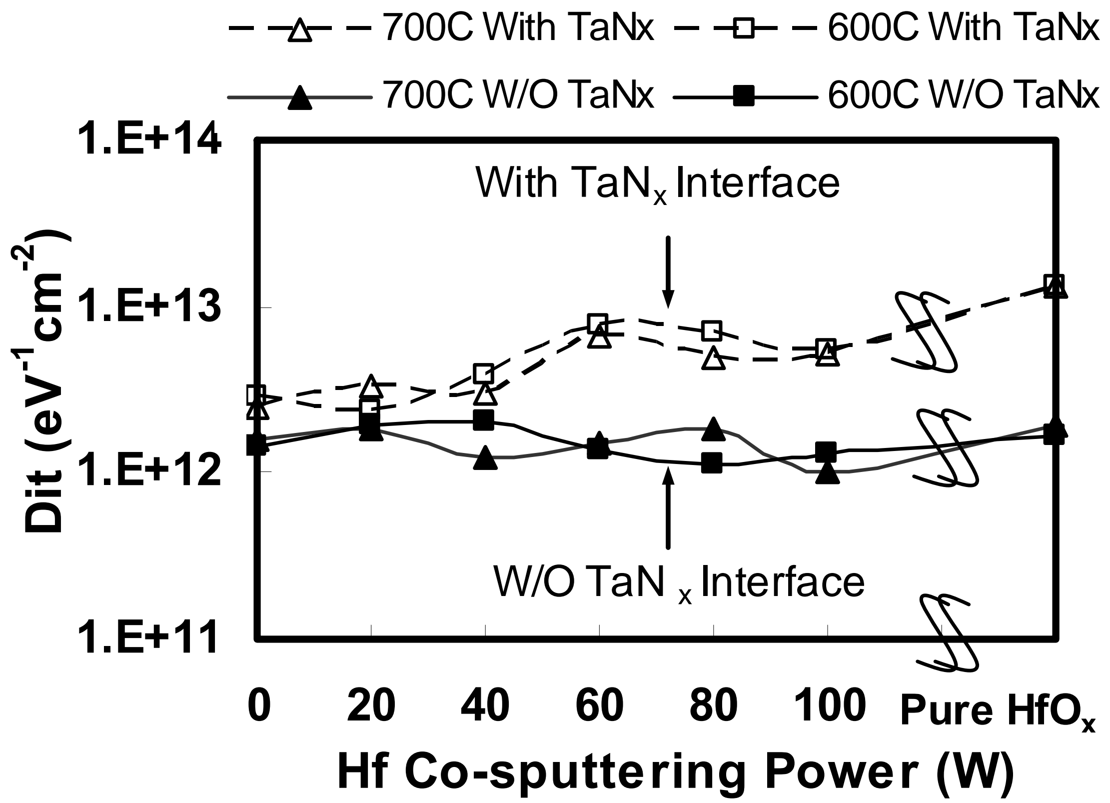


Figure 53 D_{it} of doped and un-doped TaO_x films with and without the TaN_x interface after 600°C or 700°C annealing.

5.3.7. TaN_x Interface Layer Effect on C-V Hysteresis (ΔV_{FB})

Figure 54 is a summary of the hysteresis offset of the flat-band voltage (ΔV_{FB}) of doped and un-doped TaO_x/TaN_x structures at different annealing temperatures. A counter-clockwise hysteresis was observed for all doped and un-doped TaO_x/TaN_x samples after a forward-and-reverse voltage sweep from –5V to +3V. This hysteresis is attributed to negative charge trapping in the oxide or at interface.[104] For most samples, the ΔV_{FB} is reduced dramatically to below 50 mV after 700°C O_2 annealing. Similar annealing effects on hysteresis were observed for samples without the TaN_x interface layer. For thin silicon oxide films, it is well known that oxide-trapped charges could be annealed out by low-temperature treatment (~550°C).[104] However, in this case a higher annealing temperature, e.g., 700°C, is required to anneal them out. Others also reported similar phenomenon on nitrided Si substrates, e.g., ΔV_{FB} ~ 30 mV after > 700°C annealing in O_2 or Ar.[112] For the sample without the TaN_x interface, a low ΔV_{FB}, e.g., ~100 mV, was observed after 600°C O_2 annealing, which decreased to 20~30mV after 700°C O_2 annealing. It was reported that Ta_2O_5 deposited on nitrided silicon had a larger hysteresis than that of the film deposited on silicon because nitride was easier to trap charges.[151] The hysteresis increased further after 800°C annealing due to the crystallization of the Ta_2O_5.[151] Since the doping method can keep the film amorphous even after 800ºC annealing, the increase of hysteresis could be avoided.

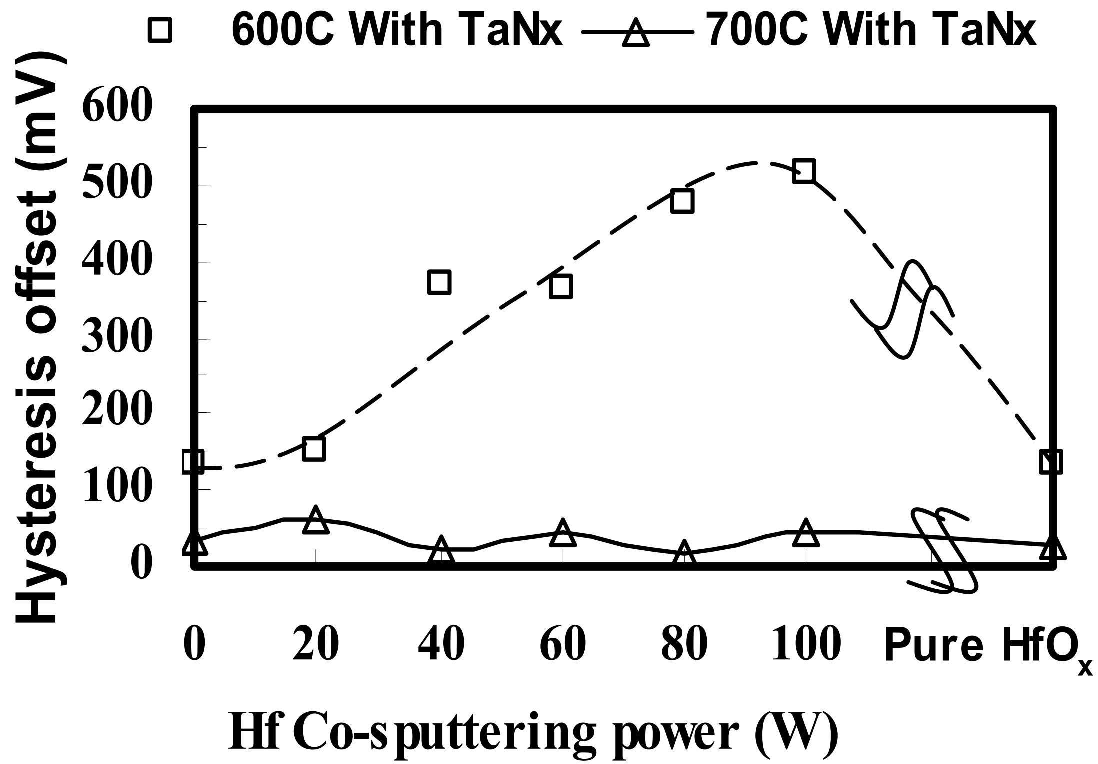


Figure 54 Hysteresis offset (ΔV_{FB}) of doped and un-doped TaO_x films with TaN_x after 600°C or 700°C annealing.

5.3.7. Comparison of SiN_x and TaN_x Interfacial Layers

The incorporation of nitrogen into the interfacial layer has many advantages over the SiO_x interfacial layer formed between the high-k dielectric film and the silicon substrate. For example, nitrogen can suppress boron and oxygen diffusion and improve thermal stability. Many methods have been proposed to incorporate nitrogen into the interfacial layer. The most popular method is to pre-treat the silicon surface in NH_3 or NO_2 to form a thin silicon nitride or oxynitride layer before the deposition of the high-k dielectric layer to prevent the oxidation of the silicon substrate. Since silicon nitride or oxynitride has a k value almost twice that of SiO_x, the improvement of the dielectric constant had been achieved with the insertion of these interfacial layers. [90, 112] However, silicon nitride and oxynitride do not have very high k values, which limit the ultimate scalability of overall equivalent oxide thickness (EOT). In addition, silicon nitride or oxynitride has a high interface density of states, which deteriorates many transistor characteristics such as mobility. In this study, non-stoichiometric TaN_x was used as the oxidation-barrier layer. TaN_x is easily converted into non-conductive TaO_xN_y film during high temperature O_2 annealing.[143-144] TaO_xN_y itself is a good insulator with a high k value, and its deposition process is compatible with the TaO_x deposition process. The improvement of the $I_{leakage}$ and $k_{effective}$ with the insertion of the TaN_x film is expected after high temperature O_2 annealing. The increase of the fixed charges due to the TaN_x insertion of film is a characteristic of the nitride layer. A higher temperature annealing process will be necessary to further reduce the fixed charge density.

5.4. Chemical Characterization of the Interface Layer

5.4.1. SIMS Depth Profile of Undoped TaO_x With and Without a TaN_x Interface Layer

Figure 55 (a) shows the SIMS depth profile of the 700 °C O_2 annealed, undoped TaO_x film without the TaN_x interface layer. Very strong Si_2O cluster ion signals were detected at the interface region. These ion signals indicate the formation of a SiO_x interfacial layer between the un-doped TaO_x and Si substrate. The TaO ion signals, which represent bulk TaO_x, are uniform across the bulk film. However, these TaO ion signals decrease abruptly when they reach the interface region, which implies that the interfacial layer is dominated by SiO_x, there being only a very small amount of Ta atoms in the interfacial region. This is consistent with the previous report that Ta_2O_5 is thermally unstable on top of Si, and at about 25Å thick SiO_x interfacial layer is formed during post-deposition high temperature annealing process.[39] Since the k value of this SiO_x interfacial layer is very low, the formation of this interfacial layer will degrade the overall dielectric performance dramatically.

Figure 55 (b) shows the SIMS depth profile of the TaO_x/TaN_x/Si structure after 700°C O_2 annealing. Even though the Si_2O cluster ion signals are still detected at the TaO_x and Si interface region, the signal intensities decrease by a factor of 10 compared to the un-doped TaO_x film without the TaN_x interface. This decrease might be partially due to a matrix effect but is most likely due to the barrier effect of the thin TaN_x layer on the oxygen diffusion. In addition, the TaN cluster ion signal peak was detected at the interfacial region, which confirms the incorporation of nitrogen into the interfacial layer. At the corresponding TaN ion signal peak position, the TaO ion signal density is still very

high, which means that there are large amounts of TaO ions in the same interface region. These TaN ion signals, together with the TaO ion signals in the interface region, indicate the existence of a non-stoichiometric TaO_xN_y layer at the interface before the ion-sputtering of SIMS analysis. It had been reported that tantalum oxynitride could be decomposed into TaO_x and TaN by ion sputtering.[152] The assumption of the formation of a TaO_xN_y interfacial layer can also be confirmed by XPS depth profiling, which will be discussed in the next section. The relative peak position of the Si_2O and TaN cluster ion signals indicates that this interfacial layer is composed of two regions. The top region is TaO_xN_y rich with a relatively higher k value, and the bottom region is SiO_x rich with a relatively lower k value. Therefore, the enhancement of the $k_{effective}$ value could be explained by the formation of the complicated high-k interfacial layer.

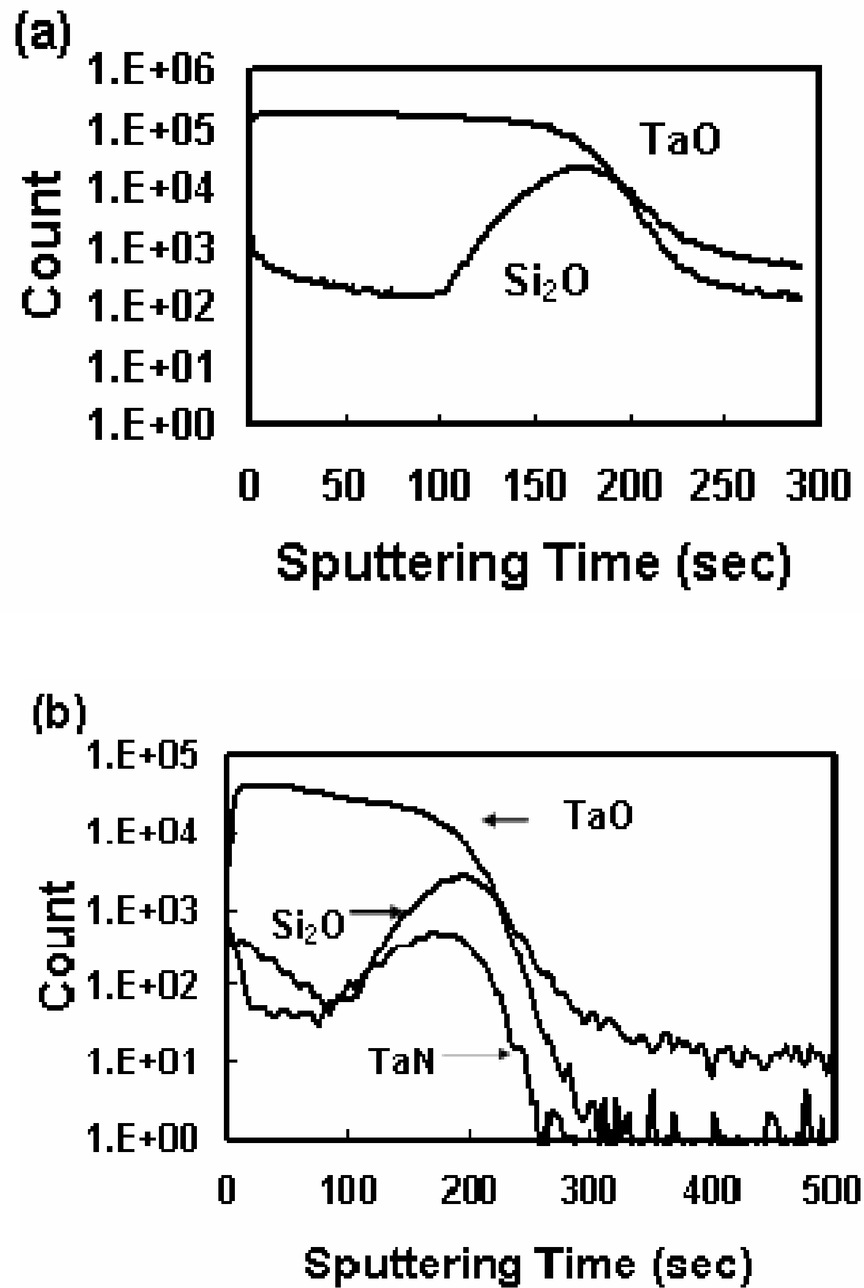


Figure 55 SIMS depth profile of (a) TaO_x/Si film after 700 ºC-10min O_2 annealing and (b) TaOx/TaN_x/Si film after 700 ºC-10min O_2 annealing.

5.4.2. SIMS Depth Profile of Undoped TaO_x With and Without a TaN_x Interface Layer

Figure 56 shows the SIMS depth profiles of the 700°C O_2 annealed Hf (20W)-doped TaO_x films with and without the TaN_x interface layer. The Hf, Ta and O ion cluster signals were detected, which represent the HfO_x and TaO_x in the bulk film. For the film without the TaN_x interface layer, both Si_2O and $HfSiO_2$ ion signals were observed in the interface region. The $HfSiO_2$ cluster ion signal indicates the existence of the $HfSi_xO_y$ component because the bulk film was doped with Hf. The Si_2O cluster ion signal count in the interface of the Hf-doped film, as shown in Fig.56 (a), is lower than that of the interface of the undoped TaO_x film under the same fabrication condition as shown in Fig. 55 (a). This indicates that the Hf component can hinder the interface layer formation, which agrees with the TEM result, i.e., the interface layer thickness of Hf-doped films is less than that of un-doped TaO_x.

For the 700°C O_2 annealed Hf (20W)-doped TaO_x sample with the TaN_x interface layer, components, such as N, Si_2O, and $HfSiO_2$, were detected at the interface region. $HfSiO_2$ cluster ion signals indicate the existence of the $HfSi_xO_y$ in the interface after doping Hf into the TaO_x. The Si_2O ion signal's density of the Hf-doped films is lower than that of un-doped TaO_x with a TaN_x interface as shown in Fig. 55 (b) by a factor of 3, which may explain the improvement of the dielectric constant of Hf-doped TaO_x relative to the un-doped TaO_x. However, the ratio of $HfSiO_2$ to Si_2O decreases slightly with the insertion of the TaN_x interface. This can be explained by the barrier effect of the TaN_x interface to the diffusion of the Hf atom into the silicon substrate.

Figure 56 shows that the Hf-silicate interface layer is formed independently of the presence of the TaN_x interface. Since the Hf-silicate have a higher k value than that of SiO_x, their formation contributes to the improvement of the $k_{effective}$.

The TaN ion signals were also detected, but their profile cannot be identified accurately with SIMS due to the interference effect of the HfO cluster ions. Instead, the N ion signals could be used as an indication of the TaO_xN_y interface layer because it was observed that N signals have the similar trend with that of TaN signals in the undoped TaO_x films with the insertion of the TaN_x interface. The relative peak position of these ion cluster signals suggests that the $HfSi_xO_y$ interface layer is located at the same position of the SiO_x interface layer.

SIMS results also indicate that nitrogen, instead of just being located at the interface region, diffuses into the bulk TaO_x film after high temperature annealing. This nitrogen diffusion is not serious because the concentration of nitrogen is out of the detection limit of XPS. However, it might play an important role in enhancing the film's dielectric properties. The decrease of leakage current density and the flat-band voltage shift characteristic observed in previous sections could also be attributed to the existence of nitrogen content in the bulk film.

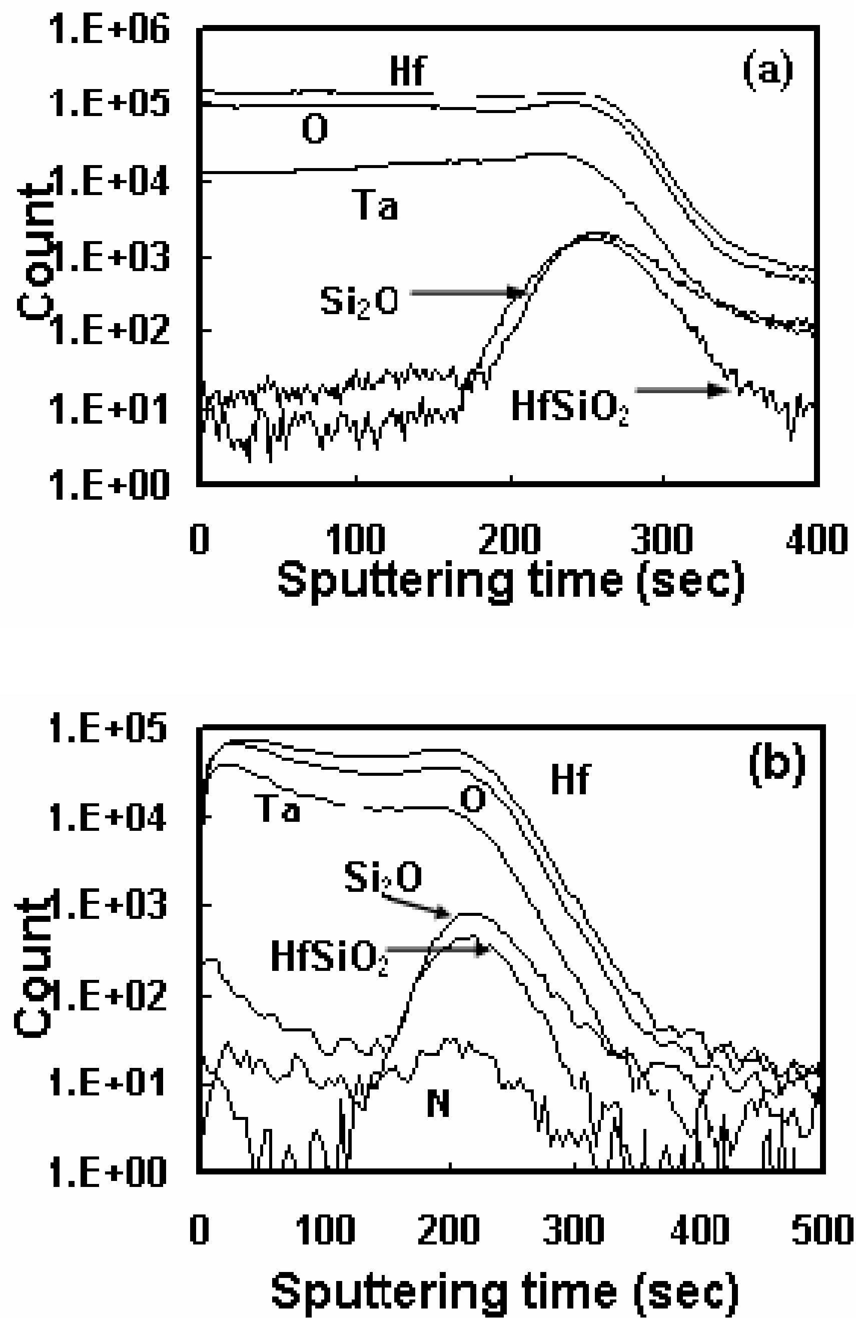


Figure 56 TOF-SIMS profiles of Hf (20W)-doped TaO_x films (a) without and (b) with the inserted TaN_x interface layer, after 700ºC-10 min O_2 annealing.

5.4.3. XPS Depth Profiling of Hf-doped TaO_x with TaN_x Interface Layer

The chemical structure of the Hf-doped TaO_x with the TaN_x interface layer was investigated by XPS depth profiling. Figure 57 shows that the chemical state of Ta 4f spectra changes across the Hf-doped $TaO_x/TaN_x/Si$ high-k gate stack structure. The film was sputter etched with Ar+ ions. Figure 57 shows that only typical Ta_2O_5 characteristic peaks, e.g., at ~26.2 eV and ~28.1 eV, were observed for the fresh surface before ion sputtering. After a 300 sec or 600 sec ion sputtering, two additional low energy doublets can be observed at the interface layer. The peak binding energies of the first doublet are located at ~23.6 eV and ~25.5 eV, which can be attributed to the Ta-N bonds. The peak binding energies of the second doublet are located between the Ta-O bonds and Ta-N bonds, e.g., at ~24.6 eV and ~26.5 eV, which may be attributed to the Ta-O bonds with the presence of a third N atom, e.g., Ta-O (N). The observation of the Ta-N and Ta-O (N) bonds at the interface layer region is consistent with the presence of TaO and TaN ion clusters at the interface layers detected by SIMS analysis. SIMS and depth profiling XPS analysis confirmed the formation of a non-stoichiometric TaO_xN_y interface layer as suggested by the electrical analysis in the previous section. Therefore, the inserted TaN_x layer changed the interface layer structure after high temperature annealing in O_2 by intermixing TaO_x and TaN_x. The TaO_xN_y interface layer is a good insulator and crucial for high-k gate dielectric applications because it has a low leakage current and a high dielectric constant.

Figure 58 shows the Hf 4f spectra of the same sample with the same ion etching condition. Figure 58 shows that only typical HfO_2 characteristic peaks, e.g., at ~17.0 eV and ~18.8 eV, were observed for the no etch and 300 sec etch films. The lack of the low

binding energy peaks suggested that no hafnium nitride or oxynitride was formed in either bulk film or interface when the TaN_x interface layer was inserted between the Hf-doped TaO_x film and Si. This is consistent with the SIMS result that no HfN ion clusters were detected in these samples. After the 600 sec ion sputtering, an additional low energy doublet can be observed at the interface layer. The peak binding energies of this doublet are located at ~17.6 eV and ~19.4 eV, which is higher than that of the typical Hf-O bonds of the HfO_2. These high binding energy peaks can be attributed to the formation of Hf-silicate interface layer. [120-121]

Figure 59 shows the Si 2p spectra of the same sample with the same ion etching condition. The 99.3 eV peaks observed after 300 and 600 seconds of ion sputtering could be attributed to the Si atoms from the Si substrate. The two small 102.8 eV peaks, which appear after 300 and 600 seconds of ion sputtering, can be contributed to the oxidized Si atoms from the interface layer. The high-energy features in the Si spectra provide some information about interfacial Si atoms. For example, the relative SiO_x interface layer thickness can be estimated from the ratio between the high binding energy Si peak areas to the low binding energy Si peak areas.[151] Compared to the Si 2p spectra of the corresponding undoped TaO_x film as shown in Figure 60, the oxidized Si atoms contained in the interfacial layer of Hf-doped films are much lower than that of the undoped film, which is consistent with the SIMS results in the previous section. Both SIMS and XPS results confirm that the doping of Hf into the TaO_x can effectively constrain the formation of a SiO_x-rich interfacial layer. This observation is also consistent with the TEM result that Hf doping of the Ta_2O_5 thin film effectively reduces the interfacial SiO_x thickness.

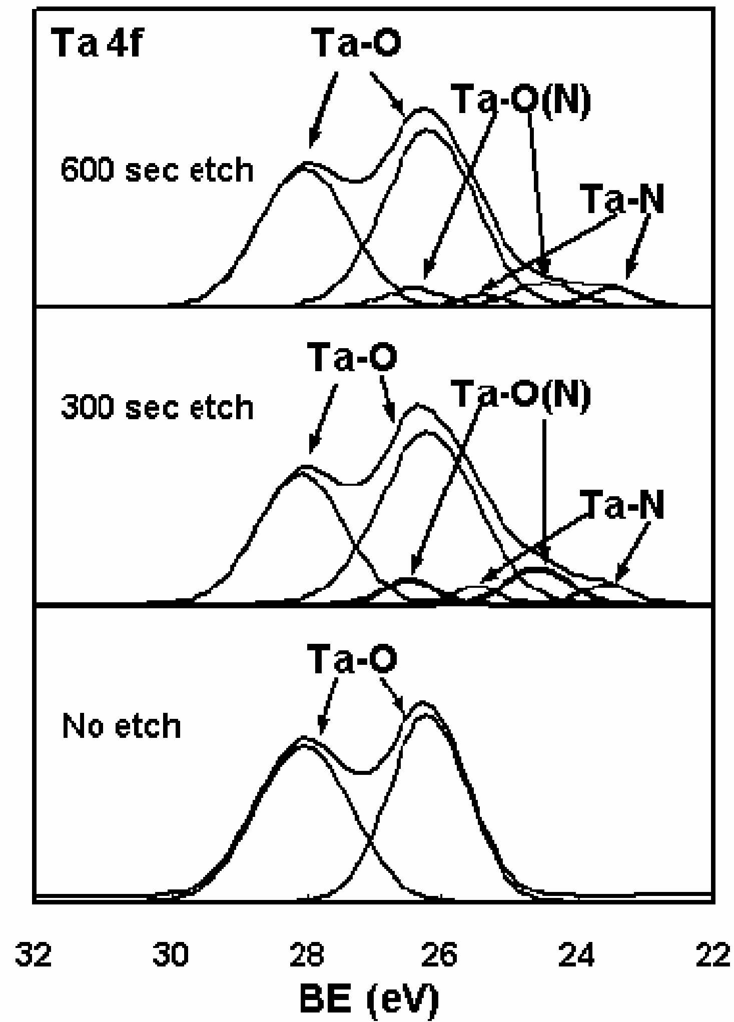


Figure 57 Ta 4f spectra of a Hf-doped $TaO_x/TaN_x/Si$ high-k gate stack structure after 700°C-10 min O_2 annealing. The film was sputter etched with Ar+ ions for 0 sec, 300 sec, and 600 sec.

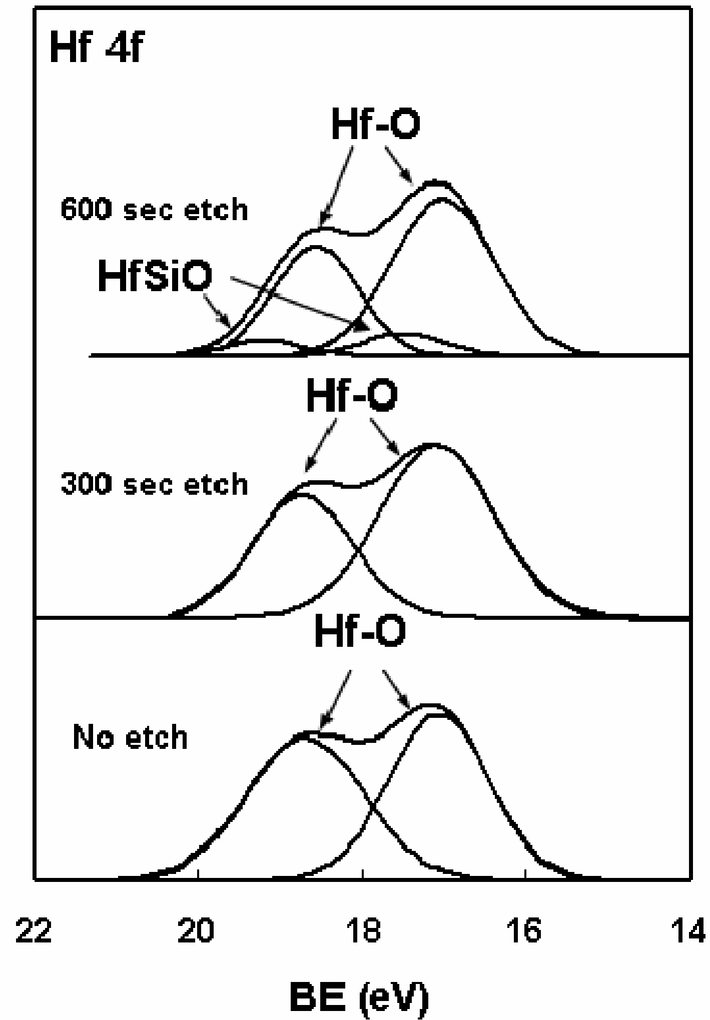


Figure 58 Hf 4f spectra of a Hf-doped $TaO_x/TaN_x/Si$ high-k gate stack structure after 700°C-10 min O_2 annealing. The film was sputter etched with Ar+ ions for 0 sec, 300 sec, and 600 sec.

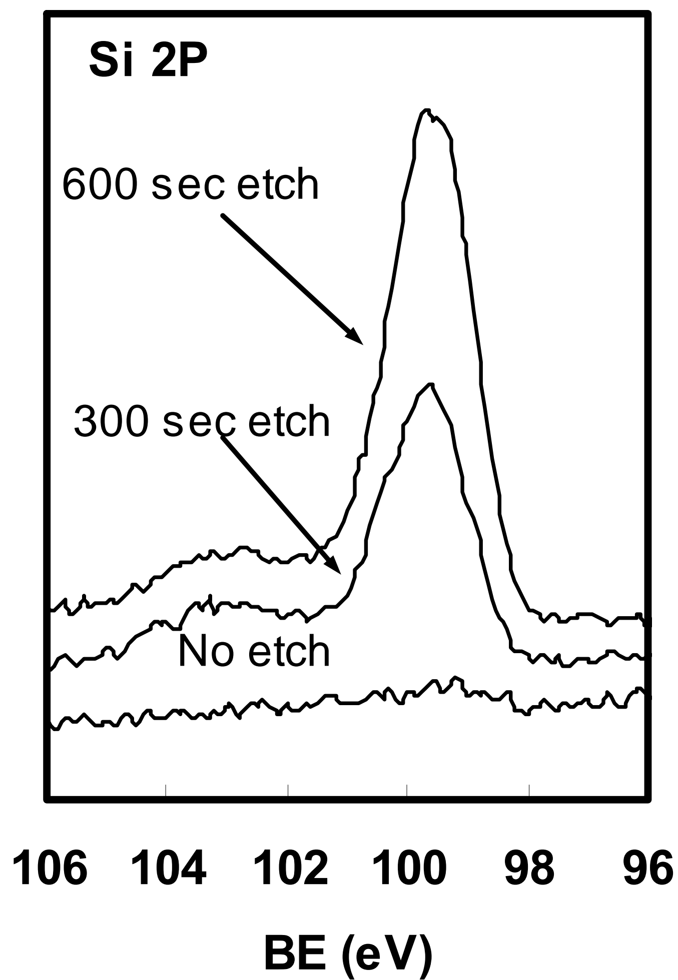


Figure 59 Si 2p spectra of a Hf-doped $TaO_x/TaN_x/Si$ high-k gate stack structure after 700°C-10 min O_2 annealing. The film was sputter etched with Ar+ ions for 0 sec, 300 sec, and 600 sec.

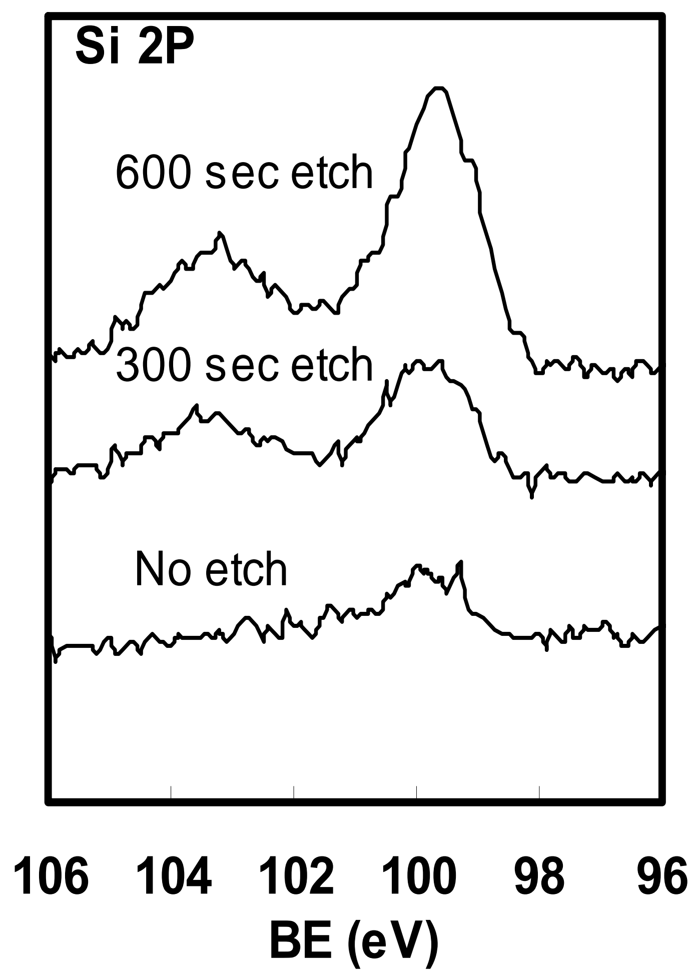


Figure 60 Si 2p spectra of an undoped $TaO_x/TaN_x/Si$ high-k gate stack structure after 700°C-10 min O_2 annealing. The film was sputter etched with Ar+ ions for 0 sec, 300 sec, and 600 sec.

5.4.4. Interface Layer Structure with Hf Doping and TaN_x Interface Layer

Figure 61 (a)-(c) are summaries of the interface layer structures and compositions formed between the silicon substrate and (a) undoped TaO_x, (b) Hf-doped TaO_x without an inserted TaN_x interface, and (c) Hf-doped TaO_x with an inserted TaN_x interface layer, after the 700°C-10 min temperature O_2 annealing step. These schematic structures were drawn based on TEM, SIMS and depth profiling XPS analysis. For the undoped TaO_x, the major component in the interface layer is SiO_x and the interface thickness is about 2.5 nm after the 700ºC, 10-minute O_2 annealing. For the Hf-doped TaO_x, Hf is involved in the interface formation process. The interface layer is thinner, e.g., 1.5 to 2.4 nm, and is composed of SiO_x and $HfSi_xO_y$. The incorporation of Hf into the bulk TaO_x film could increase the effective dielectric constant k value of the high-k film because the resulting interface layer has a higher k value than that of SiO_x.

With the insertion of the TaN_x interface layer, the newly formed interface contains a TaO_xN_y after high temperature O_2 annealing, which is a diffusion barrier for O atoms and hinders the formation of the low quality interface layer. In addition, the interface layer structure is changed from the single-zone to the multi-zone where the TaO_xN_y interface layer is sandwiched between the bulk high k layer and the $HfSi_xO_y/SiO_x$ interface layer. However, the inserted 5 Å TaN_x interface layer cannot completely block the formation of a SiO_x-like interface during the O_2 annealing. Although the SiO_x-like interface is undesirable from the overall dielectric constant viewpoint, a high quality SiO_2-like interface layer is desirable from the point of view of a low interface state density, which is critical for the high MOSFET field-effect mobility.[1]

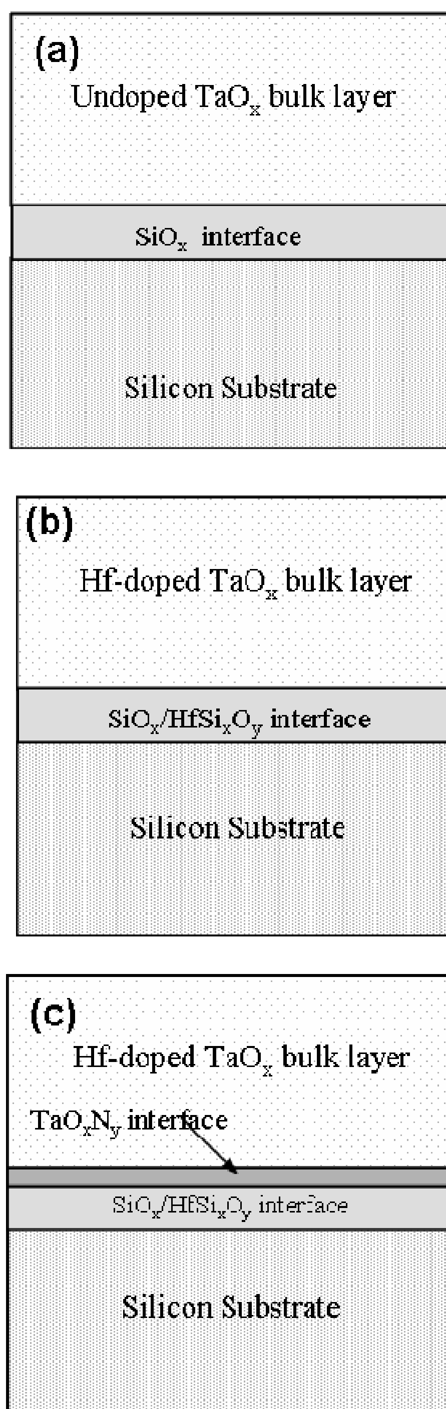


Figure 61 Interface layer structures and compositions formed between the silicon substrate and (a) un-doped TaO_x, (b) Hf-doped TaO_x without an inserted TaN_x interface, and (c) Hf-doped TaO_x with an inserted TaN_x interface layer, after a high temperature O_2 annealing step.

5.5. Summary

The electrical characterization result shows that the insertion of a 5 Å TaN_x between the doped TaO_x films and the Si substrate could decrease the film's leakage current density and improve the $k_{effective}$ value. The improvement of these dielectric properties can be attributed to the formation of the TaO_xN_y interfacial layer after high temperature O_2 annealing. The SIMS and XPS results also show that existence of N and Hf in the interface formed between the Hf-doped TaO_x films and Si wafer. The high-k dielectric film's properties are improved by the combination of doping the bulk film and inserting a thin TaN_x interface layer although a complicated multi-layer interface layer is formed. The main drawback is the high interface density of states and hysteresis, which needs to be lowered down.

CHAPTER VI

METAL NITRIDE GATE ELECTRODE ON HAFNIUM OXIDE GATE DIELECTRIC

6.1 Introduction

Unlike thermal grown SiO_2 gate dielectric, most high-k gate dielectric materials are not compatible with the polycrystalline silicon (poly-Si) gate electrode, i.e., forming an interface layer at the poly-Si/high-k contact region.[153-155] Other disadvantages related to the poly-Si gate electrode include poly-depletion, boron diffusion and high resistance.[156-158] As discussed earlier, poly-depletion will become a serious problem with the aggressive scaling down of the MOSFET dimension. In the traditional CMOS fabrication flow, the n+ and p+ poly-Si gate electrodes were formed with an ion implantation and subsequent high temperature activation. With the scaling of the device dimensions, shallow junction depths for source/drain decrease accordingly. A limited thermal budget of the dopants activation will be required, which leads to insufficient active dopants in the poly-silicon gate, especially at the oxide interface. The depletion of carriers within the poly-Si gate will increase the EOT in inversion region and therefore results in loss of current drive and transconductance of the transistor.[1] In addition, the gate resistance of poly-Si will increase drastically with the decrease of the device dimensions, which may reduce the speed of the MOSFET integrated circuits.

All the concerns related to the poly-Si gate electrode may be addressed by using a metal gate electrode. For example, metal gate electrodes do not have the problems of poly depletion and boron dopants diffusion. In addition, the metal gate electrode also has a much lower electrical resistivity. However, replacing the poly-Si gate electrode by a

metal gate electrode will introduce a lot of integration issues and imposes formidable a challenge for both manufacturing and reliability.

There are many requirements for the metal gate electrode, including low electrical resistivity, high thermal stability, low reactivity, adequate work functions for p-channel or n-channel devices, and easy to deposit and process.[96, 159-160] Refractory metals such as Tantalum (Ta), Tungsten (W), and Molybdenum (Mo) are promising gate electrode materials. However, pure metals may have relatively poor thermal stability and high chemical reactivity at elevated temperatures.[59, 161] Metal nitrides, such as tantalum nitride (TaN), molybdenum nitride (MoN), and tungsten nitride (WN), are good diffusion barriers with low resistance and high thermal stability.[162-164] Moreover, the work functions of the metal nitrides may be adjusted with the nitrogen contents.[165-167] Therefore, metal nitrides are potentially important gate electrode materials for high-k gate dielectrics in future MOSFET devices.

6.2 Experimental

The metal nitride film was sputter deposited on a ALD HfO_2 (2.5 nm thick) in two steps: 1) a thin nitrogen-rich film was deposited by sputtering the metal targets in a mixture of 50% N_2/50% Ar for 30 seconds, and 2) a second nitride film was deposited by sputtering the metal target in a mixture of N_2/Ar for 90 minutes. The optimum N_2/Ar ratio varies with the type of metal nitride. For example, for TaN, MoN, and WN electrodes, the N_2/Ar ratios were 5%/95%, 10%/90%, and 2.5%/97.5%, respectively. These ratios were selected for their low resistivity, which can be found elsewhere.[139] The sputtering pressure was fixed at 5 mTorr. The metal nitride gate was deposited through a shadow

mask. The gate electrodes were processed through a post metallization annealing (PMA) step in a N_2 ambient, at 10 Torr, for 10 seconds at 600°C or 800°C in a separate heating chamber attached to the load-lock chamber of the sputtering system. After the backside SiO_2 was stripped with a HF solution, a 300 nm thick aluminum (Al) film was DC sputter deposited to form the Ohmic contact. Lastly, all the MOS capacitors were annealed in a forming gas ambient (10% H_2/90% N_2) at 300°C for 30 minutes in a tube furnace. In the later discussions, the as-deposited samples are referred to the samples without the N_2 PMA step, but with the backside 300°C Al forming gas annealing step. For the metal nitride work function evaluation, MOS capacitors with various HfO_2 thicknesses were prepared and characterized.

The resistivities of the metal nitride films were measured with a four-point probe (Keithley DMM 196). The gate electrode/high-k interface layer structures were characterized with an energy dispersive x-ray spectroscopy (EDXS), electron energy loss spectroscopy (EELS), high-resolution transmission electron microscopy (HRTEM), time of flight second ion mass spectroscopy (TOF-SIMS), and x-ray diffraction (XRD). The electrical properties, such as equivalent oxide thickness (EOT), flatband voltage (V_{FB}), interface state density (D_{it}), and leakage current density (J) were estimated from the capacitance-voltage (C-V) and current voltage (I-V) data, which were measured with an Agilent HP 4284A Precision LCR Meter and an Agilent HP 4155C Parameter Analyzer, respectively. The work function (Φ_m) of a metal nitride gate electrode was extracted from the V_{FB} versus EOT curve.

6.3. Physical Properties

6.3.1. Microstructures of Gate Electrodes

The microstructures of three metal nitride gates were studied by XRD. Figure 62 (a) shows the XRD patterns of the as-deposited, 600°C and 800°C N_2 annealed TaN films. Prominent cubic-TaN (111) and (200) peaks were observed in all three samples. No metallic Ta crystal phases were observed in any of these films, suggesting the films were fully nitridized. The figures also show that the crystallinity of the TaN film improved with the increase of the PMA temperature. The (200) peak became sharp and narrow after both 600°C and 800°C PMA, which may be attributed to the increase of the crystal size or change of the bond structures. The nitrogen content is an important factor for the XRD peak shape. For example, it was reported that the XRD pattern of the as-deposited TaN films varied with the nitrogen partial pressure of the sputtering gas. The TaN (200) peak height increased first with the increase of nitrogen concentration, and then decreased with the further increase of the nitrogen concentration.[168] The increase of the TaN (200) peak height in Fig. 62 (a) implies an increase of crystallization with the increase of the annealing temperature. Separately, SIMS result, which is shown in Figure 63, confirms that the nitrogen concentration in the TaN film increases with the annealing temperature.

Fig.62 (b) shows the as-deposited MoN sample had a hexagonal Mo_5N_6 crystal structure. After high temperature PMA, it transformed to a cubic Mo_2N crystal structure. This structure was stable up to 800°C N_2 PMA. Similarly, Metallic Mo crystal phases were not observed in either as-deposited or annealed films. Change of the Mo/N ratio with the annealing temperature has been confirmed with SIMS analysis, as shown in Figure 63(b). For the film after 800°C PMA, further changes of crystal size or nitrogen

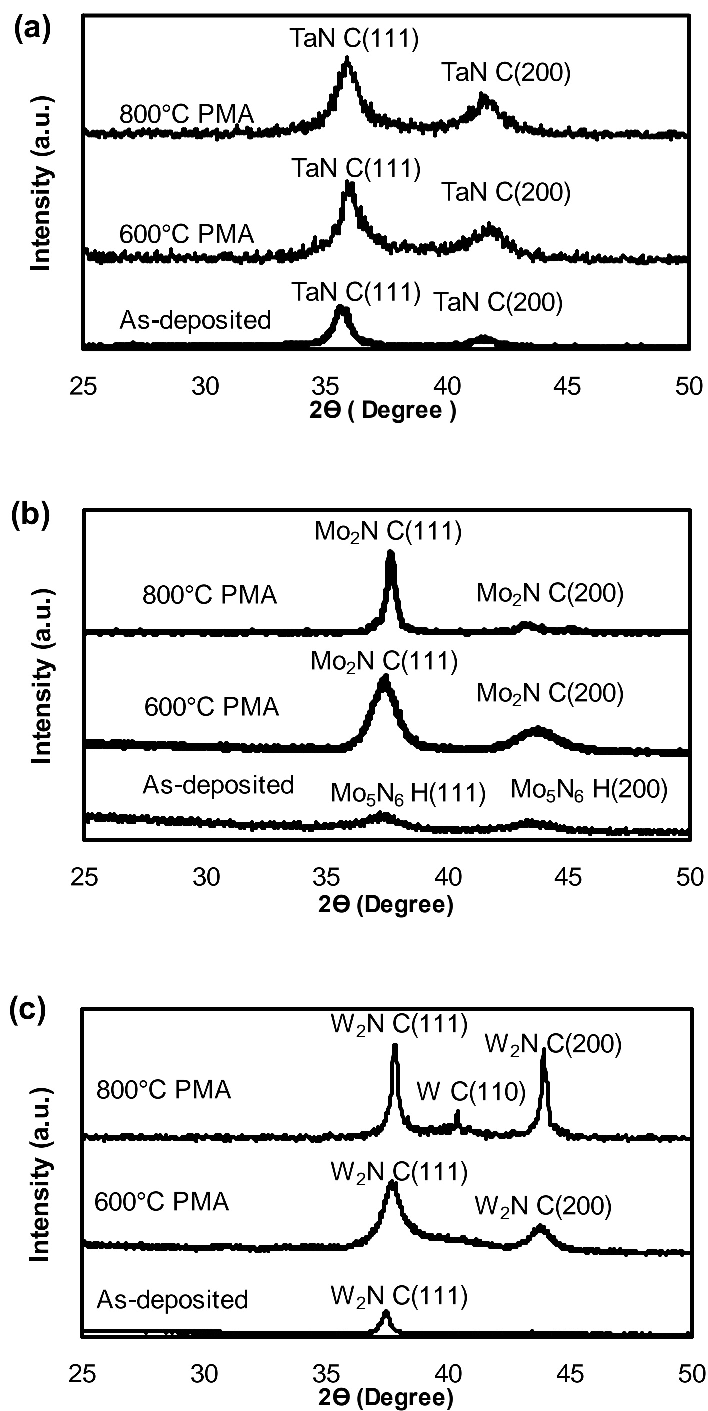


Figure 62 XRD patterns of (a) TaN, (b) MoN, (c) WN gate electrodes on 2.5nm HfO_2 films with and without N_2 PMA treatment. All the samples were annealed in forming gas at 300°C for 30min after backside Al deposition.

concentration in the MoN films may occur, which leads to a sharp Mo_2N C (111) peak and a small Mo_2N C (200) peak. It was reported that the formation of either a two-phase structure (Mo_2N and Mo) or a single-phase structure (Mo_2N) was determined by the initial nitrogen concentration in the as-deposited MoN_x film.[169-170] The film's microstructure was insensitive to the process condition once the Mo_2N phase was formed. In this study, only the single-phase structure Mo_2N was detected after high temperature PMA because the initial nitrogen concentration was high in the as-deposited film. A stable single phase Mo_2N crystal structure was formed when the PMA temperature was as high as 800°C.

Fig.62 (c) shows the as-deposited WN film had a cubic W_2N crystal structure, which suggests the as-deposited film was fully nitridized. The intensity of W_2N (111) and (200) peak heights increased with the PMA temperature. After 800°C PMA, a small W (110) peak appeared, which implies the formation of a metallic W phase. It was reported that the WN phase was not stable and a prominent W (110) peak was detected after 1025°C N_2 annealing.[171] The formation of a metallic W phase may be attributed to the dissociation of WN or the re-crystallization of amorphous WN_x component in the film. For example, the amorphous metal-rich WN_x ($x \ll 0.5$) film tends to recrystallize into W and W_2N phases at a relatively low temperature (~450°C).[172] Since the N_2/ ($Ar+N_2$) ratio in the sputtering gas steam was very low (~2.5 %), the as-deposited WN gate should be metal-rich and therefore, the formation of a metallic W phase after high temperature annealing is expected. Although the N-rich WN_x ($x>1$) film is more stable and recrystallizes at a higher temperature than the N-deficient WN_x film, the film has a much higher resistivity and, therefore, is less desirable for gate electrode applications.

6.3.2. Nitrogen Distributions in the Bulk Film and at the High-k Interface

The nitrogen concentration in the bulk metal nitride film across the nitride/HfO_2 interface is an important factor affecting electrical properties of the gate electrode as well as the MOS capacitor. Figure 63 (a) shows the TOF-SIMS depth profile of Ta-N ion clusters in the as-deposited film and after 600°C and 800°C PMA films. The as-deposited film shows N piled up at the HfO_2 interface, which is due to the two-step deposition process. After 600°C PMA, the nitrogen concentration in the bulk layer increased slightly, but the interface nitrogen concentration decreased. The increase of nitrogen concentration in the bulk TaN film is consistent with the XRD pattern change as shown in Fig. 62 (a). The decrease of the nitrogen concentration at the interface indicated that the original nitrogen atoms accumulated at the HfO_2 interface were weakly bonded, which could be removed by annealing at a moderate temperature. After 800°C PMA, the nitrogen concentration further increased slightly in the bulk TaN film, but a large increase of nitrogen concentration occurred near the metal nitride/HfO_2 interface. This increase of nitrogen concentration may be attributed to the formation of an N-rich TaN phase, e.g., Ta_3N_5, which will be discussed in later sections. This N-rich TaN phase has a high resistivity and may lead to serious interaction between the TaN gate electrode and the underlying high-k layer, which will be discussed in later sections.

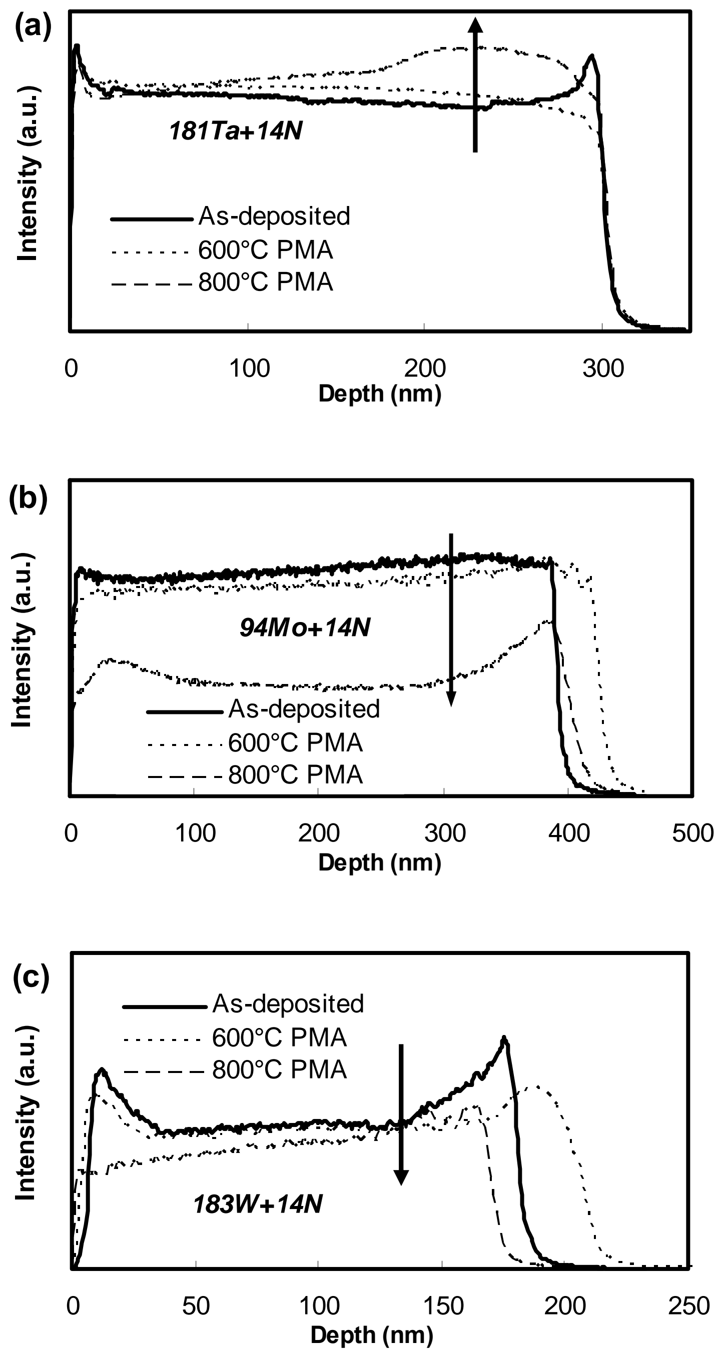


Figure 63 SIMS depth profiles of (a) TaN, (b) MoN, (c) WN gate electrodes. All the samples were annealed in forming gas at 300°C for 30min after backside Al deposition.

Fig. 63 (b) shows that the nitrogen concentration in the MoN film decreased after the PMA step. This result is also consistent with the XRD results, as the as-deposited film has the hexagonal Mo_5N_6 structure but the 600ºC PMA film has the cubic Mo_2N structure. The further decrease of nitrogen contents in the MoN gate electrodes after 800ºC PMA compared to 600ºC PMA implied that there could be some extra nitrogen in the crystalline Mo_2N matrix and could be lost during high temperature PMA. Fig. 63 (c) showing similar decreases of nitrogen concentrations were also observed in the WN films, which is consistent with the formation of a metallic W phase after 800°C N_2 PMA as shown in the XRD pattern. Schaeffer et al also reported a similar reduction of the nitrogen level with increased annealing temperature based on the SIMS analysis. [171] For example, about a 20% nitrogen loss was observed after 800°C and 900°C PMA condition; approximately 60% nitrogen loss was observed at 1025°C annealing.

6.3.3. Metal Nitride and HfO_2 Interaction

One major problem of poly-Si gates is the reaction with the high-k layer to form an interface layer. The interaction between the metal nitride gate and high-k gate dielectric layer was investigated by TEM and EELS/EDXS. Figure 64 (a) shows the thickness of the bulk high-k dielectric layer of the as-deposited sample is around 2.2~2.5nm. After 800°C PMA, the thicknesses of the bulk high-k dielectric layer increased by ~0.2 nm when the MoN and WN gate electrodes were above it as shown in Fig. 64 (b)-(c). A dramatic increase of the dielectric layer thickness (~0.7 nm) was observed when the TaN gate electrode was above it after 800°C PMA, as shown in Fig. 64 (d). This increase of the high-k dielectric layer thickness could be related to the increase of the nitrogen concentration after 800°C N_2 PMA as shown in the TOF-SIMS analysis of Fig. 63 (a). Figure 65 (a) shows the EELS profiles of O, N, and Si across the TaN/HfO_2 dielectric interface region. It is clear that O and N interdiffused through the contact region. Fig. 65 (b) shows EDXS profiles of the same sample. It also shows a serious outward diffusion of Hf atoms into the TaN gate electrode film. The elements profiles in Fig. 65 (a)-(b) suggest that a top interface layer containing Ta, Hf, O, and N atoms was formed at the TaN/HfO_2 contact area. Since this interface layer contains metal atoms, i.e., Hf and Ta, with similar size and atomic weight, it is difficult to differentiate this interface layer from the bulk HfO_2 film in the HRTEM image. Therefore, the thick high-k gate dielectric layer as shown in the HRTEM image may be contributed by both the top interface layer and the remaining bulk HfO_2 layer.

Although similar O and N interdiffusion profiles were detected by EELS on MoN/HfO_2/Si and WN/HfO_2/Si gate stack structures, the details were different. For

example, the interdiffusion between O and N in the TaN gate electrode sample was more serious than that in the MoN or WN gate electrode sample. The O shoulder stretched wider toward the metal gate area in sample with TaN gate electrode but relatively less in samples with MoN or WN gate electrode. HRTEM results also showed no dramatic increase of the bulk high-k gate dielectric thickness in these two stacks structures. Therefore, no serious interaction occurred at the MoN/ HfO_2 or WN/ HfO_2 interface after 800°C PMA. In this study, among the three metal nitride gate electrodes, TaN is least stable because it reacted with N_2 and HfO_2 at a high PMA temperature. Other researchers also reported similar results, e.g., there was some interdiffusion between Hf and Ta atoms after 1025ºC, but no Hf and W interdiffusion was reported at the same temperature.[171] These results may be contributed by the similarities between Ta and Hf atoms in terms of the weight, electronegativity, and radii.[173]

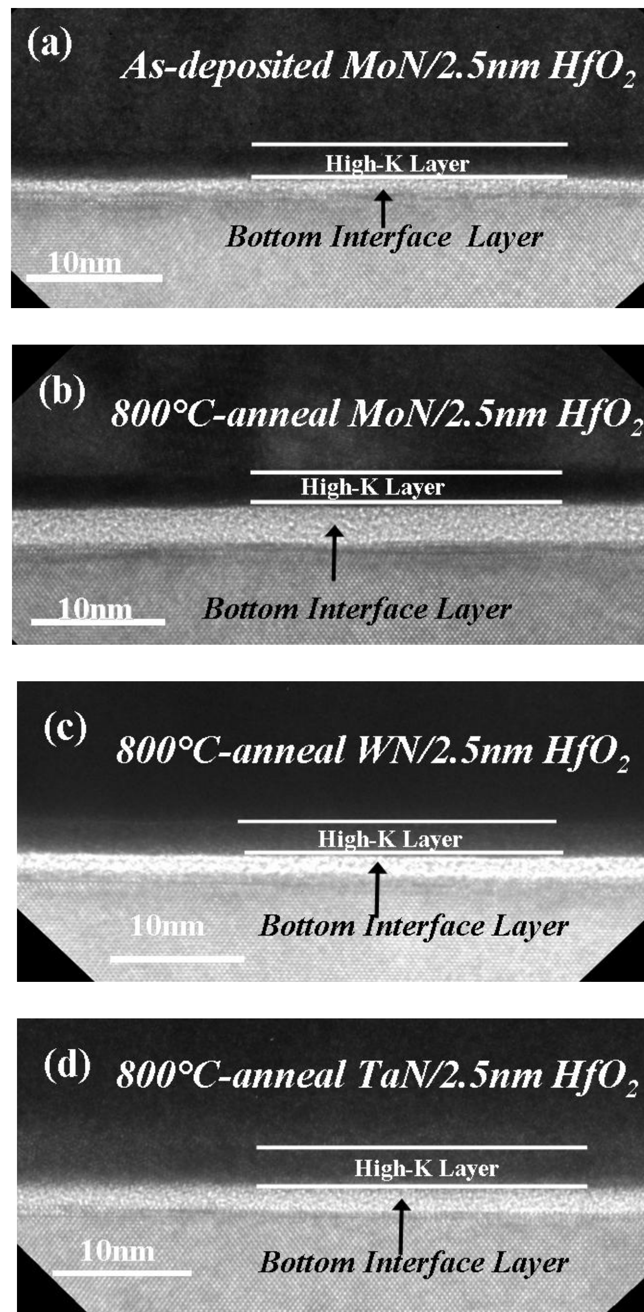


Figure 64 Comparison of high resolution TEM image of (a) as-deposited MoN/2.5nm HfO_2/Si stack, (b) 800°C PMA MoN/2.5nm HfO_2/Si, (c) 800°C PMA WN/2.5nm HfO_2/Si, (c) 800°C PMA TaN/2.5nm HfO_2/Si stack structures.

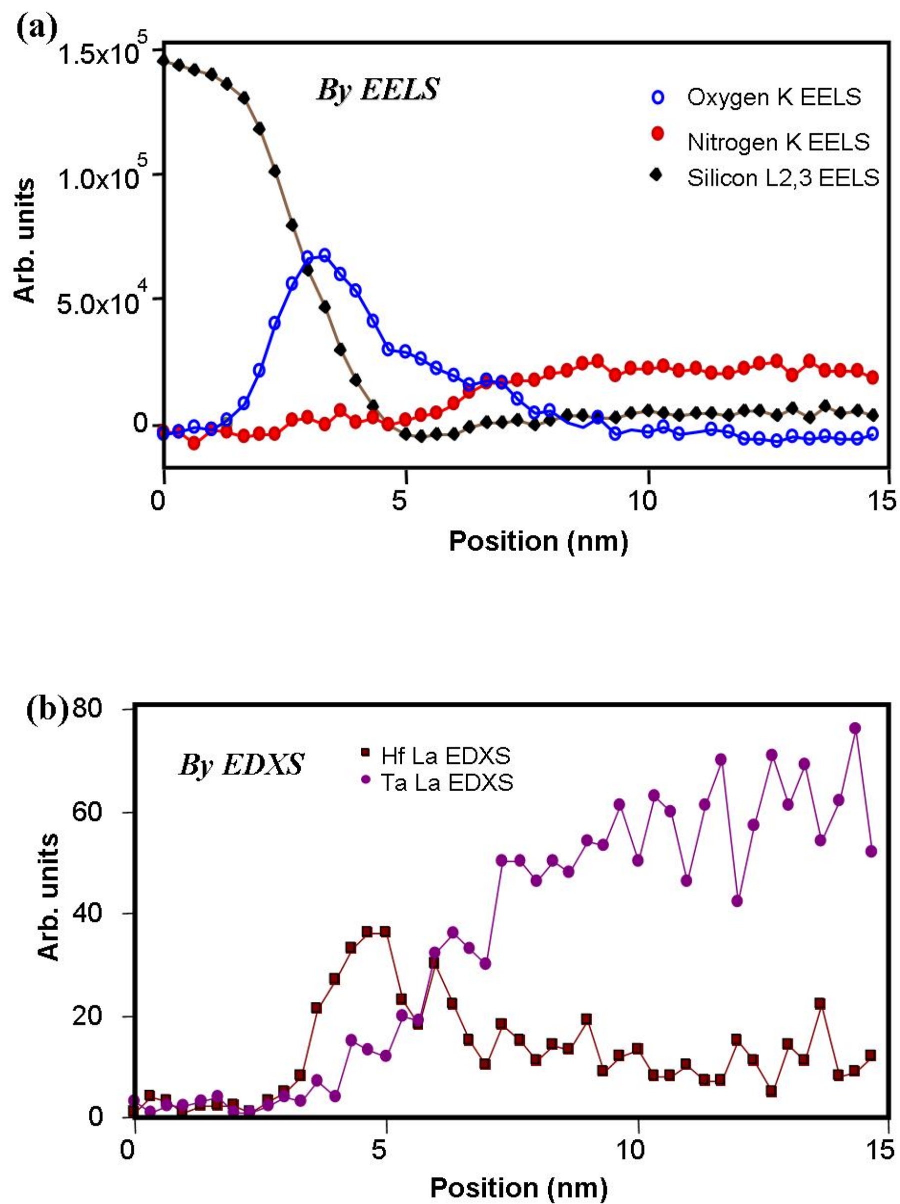
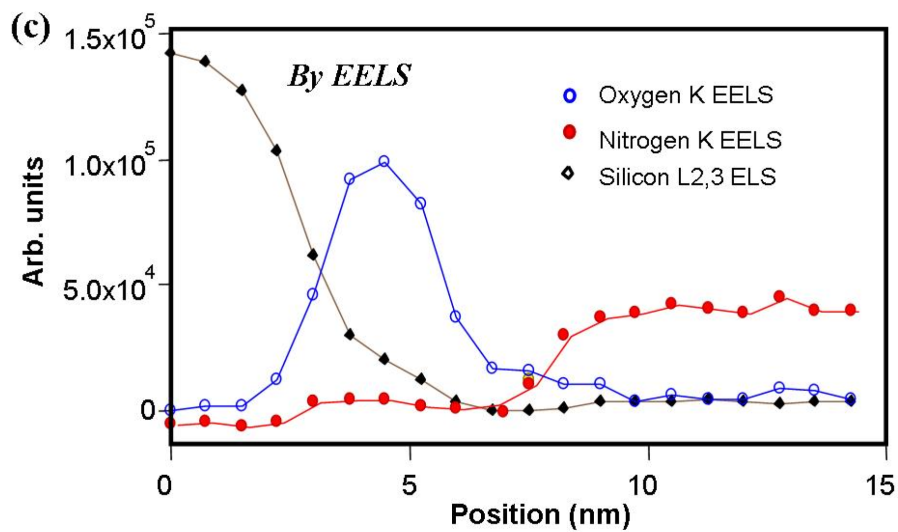


Figure 65 (a) EELS and (b) EDXS profiles of 800°C PMA TaN/2.5nm HfO_2/Si stack structures, (c) EELS profiles of 800°C PMA MoN/2.5nm HfO_2/Si stack structures, (d) EELS profiles of 800°C PMA WN/2.5nm HfO_2/Si stack structures.



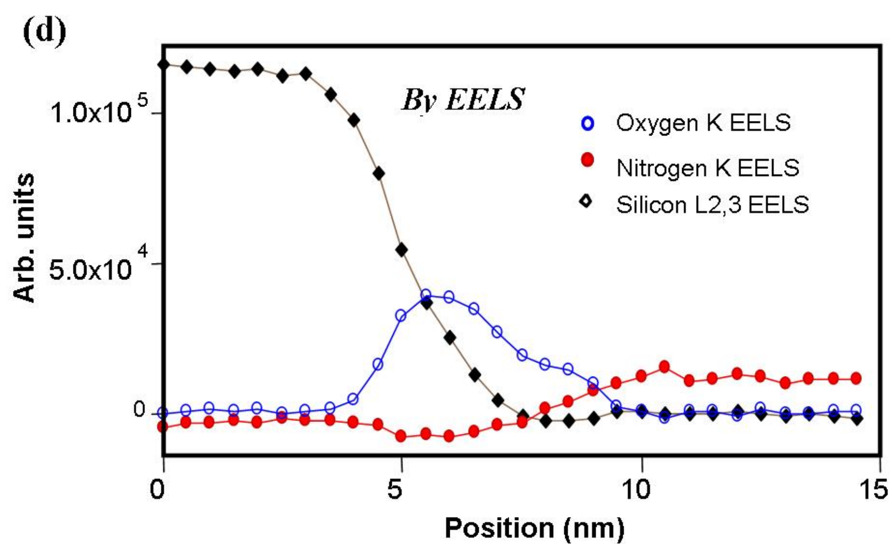


Figure 65 continued.

6.3.4. Metal Nitride Gate Influence on the Bottom HfO_2 and Si Interface Layer

An approximately 0.6 nm thick bottom interface layer was formed at HfO_2/Si interface for the as-deposited MoN/2.5 nm HfO_2/Si stack, as shown in the Fig. 64 (a). An increase of the bottom interface layer thickness was observed for all three metal nitride gate/HfO_2/Si stacks after 800°C PMA, as shown in the Fig. 64 (b)-(d). The bottom interface layer thicknesses could also be estimated from the inflection point of the EELS/EDXS profiles. Figure 66 is a summary of the bottom interface thickness measured from TEM and EELS/EDXS for all three metal gate samples after 800°C PMA. The bottom interface layer thicknesses estimated by the two methods are very close. They also show similar trends on annealing effects. For example, after 800°C PMA, the bottom interface layer thickness increases substantially for all three gate stack structures. Different gate electrodes affect the bottom interface layer thickness differently. Other researchers also reported that the gate electrode materials have some impact on the formation of the bottom interface layer.[171, 174] This may be attributed to the difference in the oxygen-block capabilities of various gate electrode materials at the high temperature.[174] Since the PMA ambient in this study was done under a high purity N_2 atmosphere, there must be some other reason for the increase of the bottom interface layer thickness. The SIMS analysis indicated that the oxygen impurity concentration in the as-deposited MoN gate electrode was the highest among all three gate electrodes, which is consistent with its thickest bottom interface layer after 800°C PMA. The lowest oxygen concentration was detected in the as-deposited WN gate electrode, which had the thinnest bottom interface layer after 800°C PMA. Based on this observation, the increase of the bottom interface layer thickness may be related to the oxygen impurity

concentration in the as-deposited gate electrode films. The high oxygen concentration in the MoN film may come from the target. More detailed analysis of the target is required to verify the above assumption. Results in this section suggest that any possible oxygen source in the process should be eliminated in order to reduce the bottom interface layer thickness.

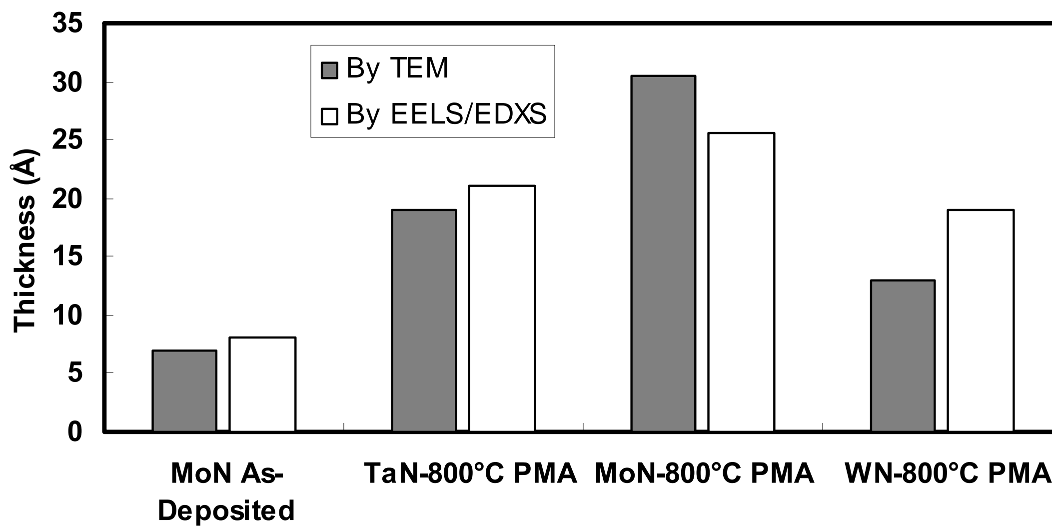


Figure 66 Bottom interface layer thickness for different gate electrodes with and without 800°C N_2 PMA. All the samples were annealed in forming gas at 300°C for 30min after backside Al deposition.

6.4. Electrical Properties

6.4.1. Resistivity

Table IV shows the resistivity of three metal nitride gate electrodes with different PMA temperatures. For as-deposited films, low resistivity (~50-70μΩ-cm) was achieved for all three gate electrode materials. However, the TaN gate electrode shows a sharp increase of resistivity after 800°C PMA. It was reported that the as-deposited TaN_x films with relatively high nitrogen concentration would have relatively low thermal stability in term of resistivity.[174-175] The sharp increase of resistivity after a high temperature anneal can be attributed to the formation of an N-rich TaN phase, such as Ta_3N_5.[171,176] In this study, SIMS analyses indicated an increase of nitrogen content in the TaN gate electrode after 800ºC N_2 PMA as shown in Fig. 63 (a), but no crystalline N-rich TaN structure was observed in the XRD patterns. The N-rich TaN phase may still be in amorphous phase. Tantalum nitride has many polymorphs and their properties vary depending on the nitrogen contents.[177]

The MoN and WN gate electrodes show a relatively stable resistivity up to 800°C PMA. A slight decrease of resistivity was observed for both gate electrodes materials. This observation is consistent with the slight nitrogen loss after high temperature PMA as shown in the SIMS profiles. The decrease of resistivity may also be attributed to the grain growth of the MoN and WN gate electrodes after the high temperature PMA, as shown in Fig. 62 (b)-(c).

Table IV Resistivity of metal gate electrodes on HfO_2 films with different PMA conditions.

Gate Electrodes	As-deposited	600°C N_2 PMA	800°C N_2 PMA
TaN	**70 μΩ-cm**	**80 μΩ-cm**	**5000 μΩ-cm**
MoN	**60 μΩ-cm**	**48 μΩ-cm**	**48 μΩ-cm**
WN	**50 μΩ-cm**	**36 μΩ-cm**	**36 μΩ-cm**

6.4.2. Equivalent Oxide Thickness

Figure 67 shows the equivalent oxide thickness (EOT) of TaN, MoN, and WN-gate electrodes/2.5 nm HfO_2 MOS capacitors at different PMA temperature. Low EOTs (0.9~1.1 nm) were achieved for the as-deposited samples. The EOT increased unanimously with the PMA temperature. The EOT increase can be attributed to the increase of the bottom interface layer thickness as shown in previous TEM and EELS results. The largest EOT (~3.0 nm) was observed for samples with the TaN gate electrode after 800ºC PMA. This can be explained by the formation of a thick top interface as a result of serious interaction between the TaN electrode and the HfO_2 film. The sample with the MoN gate electrode also shows a large EOT (~2.4 nm) after 800ºC PMA, which can be explained by the dramatic increase of the bottom interface layer thickness as shown in the TEM figure. Samples with the WN gate electrode display a relatively small variation of EOT after high temperature PMA, which is consistent with the TEM result shown in Fig. 64.

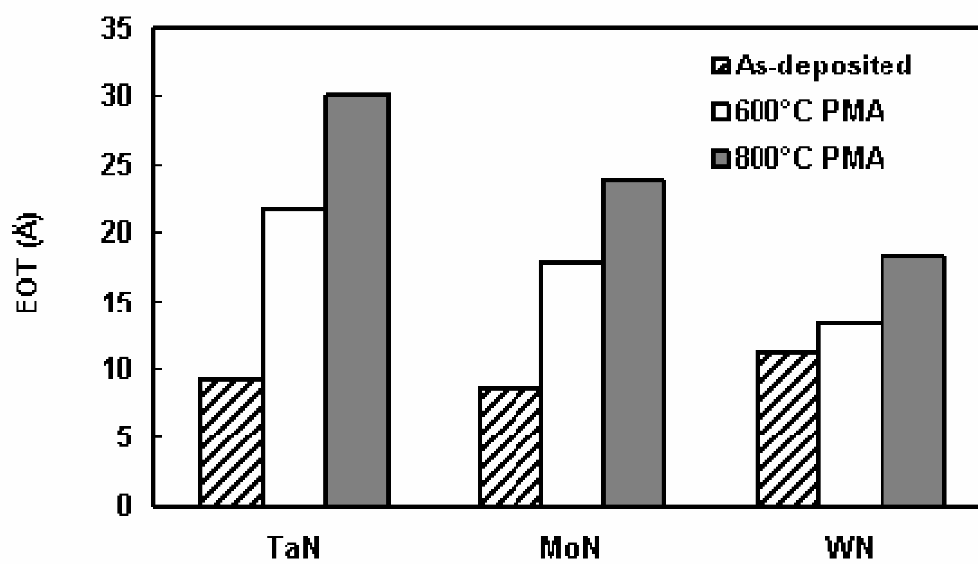


Figure 67 EOT variance with PMA treatments for samples with different gate electrodes.

6.4.3. Leakage Current Density

Figure 68 shows the leakage current density (J) vs. gate voltage (Vg) curves of capacitors with different metal nitride gates after (a) 600°C and (b) 800°C PMA. The 800°C PMA samples show lower leakage current densities than 600°C PMA samples. The decrease of the leakage current densities can be explained by the increase of EOT. The EOT value is contributed by both the bulk high-k and the interface layers. In addition to the film thickness, material properties of each layer, such as the composition and density, also affect the leakage current mechanism. Samples with the TaN gate electrode always show the lowest leakage current densities among the three types of samples. This is consistent with its large EOT value. However, for the 800°C PMA sample with the TaN gate electrode, the leakage current is three orders of magnitude lower than that of the 600°C PMA sample. The decrease of the leakage current density cannot be solely explained by the slight increase of EOT, i.e., 0.8 nm. The low leakage current could also be contributed by material property changes of the bulk high-k and interface layers. For example, Figure 65 (a)-(b) showed a serious interaction between TaN and HfO_2, which resulted in the formation of a top interface layer containing Ta, Hf, O, and N atoms? It was reported that the formation of an oxynitride interface layer would reduce the leakage current density of the high-k gate stack structure.[178-179]

The leakage current of the 800°C PMA sample with the WN gate electrode is about two orders of magnitude higher than that of the sample with the same PMA temperature but MoN gate electrode. However, the EOT of the former is only 0.6 nm lower than that of the latter. Therefore, other factors might contribute to the unusually high leakage current. One possible reason is the formation of a metallic W phase in the WN film, as

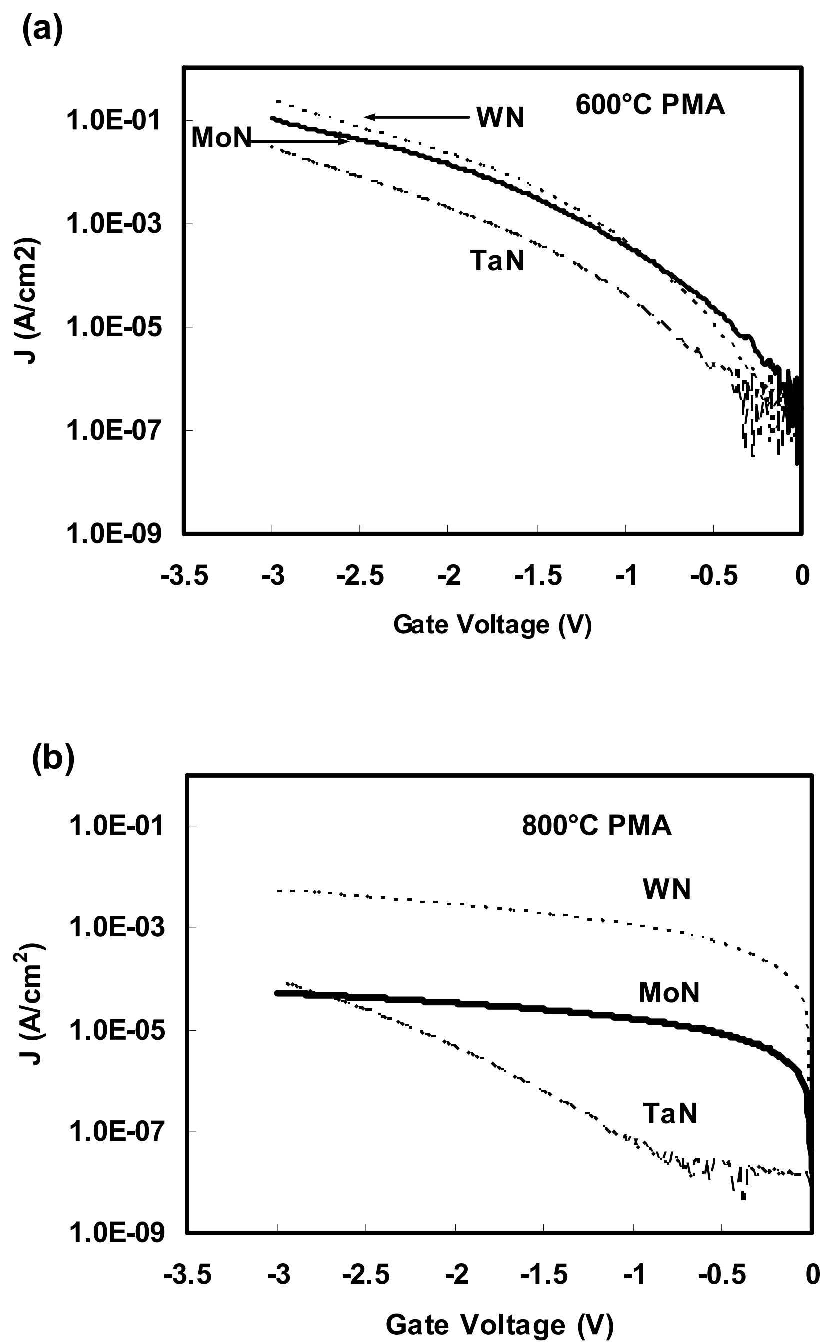


Figure 68 Comparison of leakage current densities for samples with different gate electrodes after (a) 600°C PMA, (b) 800°C PMA.

shown in the Fig. 62 (c). It was reported that for the same high-k gate dielectric films, a WN_x gate electrode showed a lower leakage current density than the W gate electrode.[180-181] WN_x is superior to W as a gate electrode because the nitrogen from WN_x can be incorporated into the high-k film. The metallic W in the WN electrode may change the metal gate/high-k top interface properties or even penetrate the high-k film to create a leaky path, which results in a high leakage current density.

6.4.4. Gate Electrodes Work Functions

The work functions (Φ_m) of the metal nitride gate electrode was extracted from the plots of flatband voltage (V_{FB}) versus EOT.[4,171] In this study, a simple linear relation between V_{FB} and EOT was assumed,

$$\mathbf{V_{FB} = \Phi_{ms} \pm \frac{Q_{eff}\ EOT}{\varepsilon_{SiO_2}}} \qquad [19]$$

where Q_{eff} is the effective oxide charge at the oxide interface, ε_{SiO_2} is the permittivity of SiO_2 (3.45×10^{-13}F/cm), and Φ_{ms} is the difference between the electrode work function (Φ_m) and Si substrate (p-type ~$10^{17}cm^{-3}$ doping level) work function (Φ_S ~ 5.09eV). The plus and minus (+/-) sign represents the positive and negative fixed charge, respectively. The Q_{eff} and the Φ_{ms} can be extracted from the slope and intercepts of the V_{FB} vs. EOT plot, respectively. The linear relationship in Eq.19 is only a simple model traditionally used to extract the work function assuming that the stacked high-k is a homogeneous layer. However, since the high-k stack is composed of two distinct layers, for more accurate characterization of the work function and charge densities, a large array

of samples, such as different SiO_2 interface layer and bulk high-k thicknesses, need to be prepared.[182]

According to calculations of Eq.19, the ϕ_M of TaN, MoN, and WN after 600°C PMA are about 5.0eV, 4.5eV, and 4.29eV, respectively. For films after 800°C PMA, the ϕ_M of TaN, MoN, and WN decreased to 4.23eV, 4.16eV, and 4.06eV, respectively. The work functions of all three gate electrodes materials are suitable for NMOS application after 800ºC PMA.[159,171] The small variation of work functions of MoN and WN gate electrodes between 600°C and 800°C PMA conditions can be explained by the minor changes of microstructures and chemical compositions as shown in XRD and SIMS results. For the TaN gate electrode, a drastic change of work function with PMA temperature was observed, which is due to its poor thermal stability and serious interaction with the HfO_2. The TEM, EELS, and SIMS results confirm the serious interaction at the TaN-HfO_2 interface after 800°C PMA. The change of work function after thermal treatment had been observed by many other researchers.[171,183] Crystallization, structure, and chemical composition can affect the work function of the metal gate electrodes above the HfO_2 films.[171,183] In this study, the change of work function can be related to the changes of the physical properties of metal nitride gate electrodes after high temperature PMA treatment.

6.4.5. Interface State Density

Figure 69 shows the change of interface state density (D_{it}) of 2.5nm HfO_2 films with different PMA temperatures. The D_{it} in this work was extracted at the midgap by the single frequency approximation method (Hill's method) from 1 MHz/100kHz frequencies C-V measurement.[184] For the samples with TaN and MoN gate electrodes, the D_{it}

decreased with the increase of the PMA temperature. This suggested that high temperature PMA anneal can be effective to anneal out the damage caused by the PVD gate deposition process.[185-186]

However, samples with WN gate electrodes show a different trend on the change of D_{it} after 800°C PMA. The 800°C PMA sample has a slightly higher D_{it} than the 600°C PMA sample. This phenomenon has been observed on Ta_2O_5 high-k films and the W/WN gate electrode. [185] The exact reason for the increase of D_{it} after high temperature anneal is still unknown. In this study, the increase of D_{it} for WN gate may be attributed to the formation of the metallic W phase in the WN gate electrodes after 800ºC PMA, which was close to the bottom high-k/Si interface and degraded the interface quality.

It should also be noticed that the D_{it} value is influenced by the metal gate electrode material. For example, samples with a TaN gate show a lower D_{it} value than those with the other two gate electrode materials regardless of the PMA temperature. The gate electrode material and metal gate deposition conditions were reported to affect the interface state density of MOS with SiO_2 and high-k gate dielectrics.[177, 185-186] There are several possible explanations. For example, some deposition processes may cause more damages to the thin gate dielectric film than other processes, e.g., high ion bombard energy or strong short wavelength light radiation during sputtering. In addition, different gate electrodes may have different stresses, which could affect the interface state density.[187] Another reason may be associated with the different barrier properties of metal gate electrodes related to diffusion of hydrogen atoms during the post metal forming gas annealing step. More detailed studies on the gate electrodes effects on the interface state density are under progress.

Figure 70 shows the D_{it} values for different metal nitride gate electrode on HfO_2 high-k gate dielectric films with different physical thickness after 800°C PMA. For TaN and WN gate electrodes, D_{it} decreased with the increase of HfO_2 physical thickness. However, for the MoN gate electrode, the HfO_2 physical thickness almost has negligible effects on the D_{it} value. Samples with TaN gate electrode always exhibit a lower D_{it} values than those with MoN and WN gate electrodes.

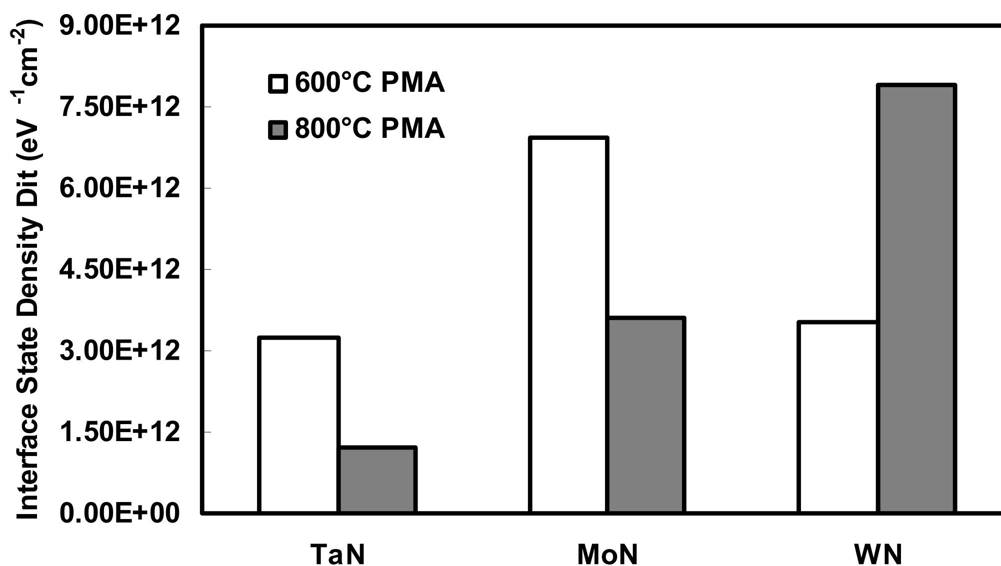


Figure 69 PMA temperature effects on the interface state density (D_{it}) for samples with different gate electrodes.

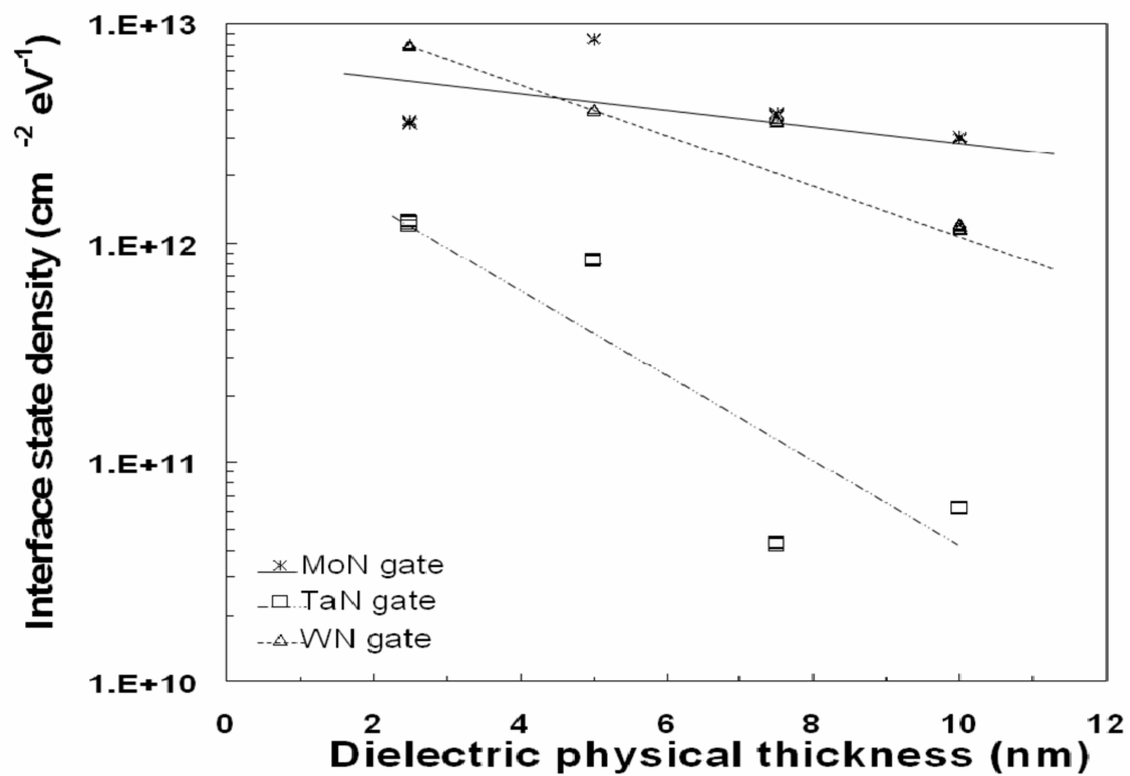


Figure 70 Interface state densities D_{it} vs. the undoped ALD deposited HfO_2 gate dielectric thicknesses for TaN, WN and MoN gate electrode at 800°C PMA condition.

6.4.6. Oxide Trap Density

Figure 71 shows the bulk oxide charge density (Q_{ot}) of 2.5nm HfO_2 films with different metal nitride gate electrode materials. The Q_{ot} was extracted from the hysteresis of the CV curves using the following equation.

$$\mathbf{Q_{ot} = -\frac{C_{ox}\Delta V_{FB}}{q}} \qquad [20]$$

where the ΔV_{FB} is the flat band voltage shift after a forward-and-reverse voltage sweep from –3V to +3V, q is the electronic charge, and C_{ox} is the accumulation capacitance per unit area. Fig. 71 shows that in all cases the Q_{ot} value decreases after the high temperature PMA step. High temperature annealing can effectively reduce defects in the high-k film caused by the sputter deposition process of the gate electrode. In addition, after PMA, the overall high-k stack physical thickness increased. Under the same sweep voltage condition, the effective electrical field and the amount of the injected charges decreased accordingly, which may also lead to a lower Q_{ot}. For samples with WN and MoN gate electrodes, a lower Q_{ot} was achieved by increasing the PMA temperature, e.g., from 600ºC to 800ºC. The lowest Q_{ot} was obtained for the sample with a WN gate electrode after 800ºC PMA. However, a slight increase of Q_{ot} was observed for the sample with the TaN gate electrode after 800°C PMA compared to the sample after 600°C PMA. This can be explained by the serious interaction between the TaN and HfO_2 film after 800°C PMA. EELS result in Fig. 65 (a)-(b) showed that a top interface layer containing Ta, Hf, O, and N atoms was formed at the TaN/HfO_2 contact region, which increased the oxide trap density of the high-k gate stack structure.[132, 188] Figure 72 shows the Q_{ot} values for different metal nitride gate electrodes on HfO_2 high-k gate dielectric

films with different physical thickness after 800°C PMA. For all three gate electrodes materials, the Qot values increase with the increase of the HfO_2 physical thickness. Samples with WN gate electrode always show exhibit a lower Q_{ot} values than those with TaN and MoN gate electrodes

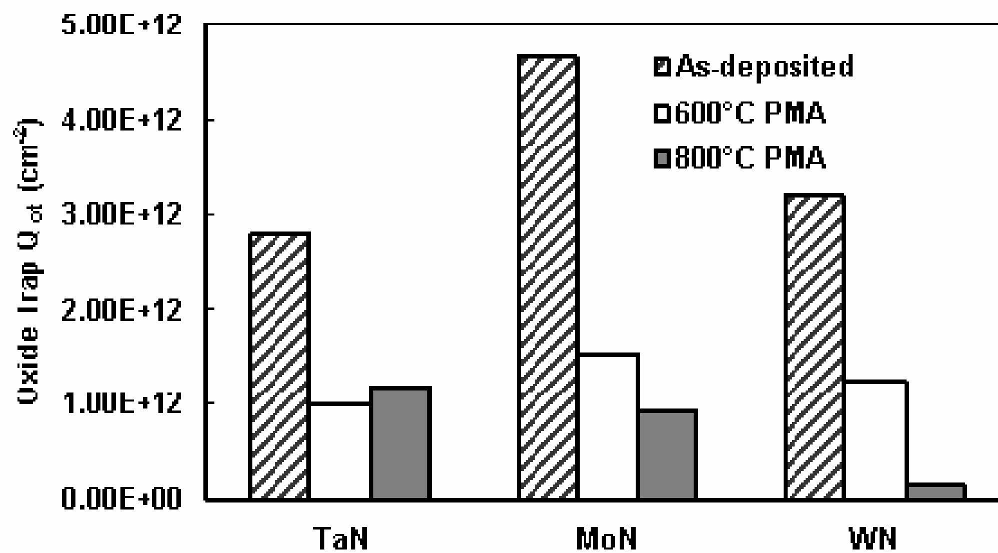


Figure 71 Oxide charge density (Q_{ot}) of samples with different gate electrodes.

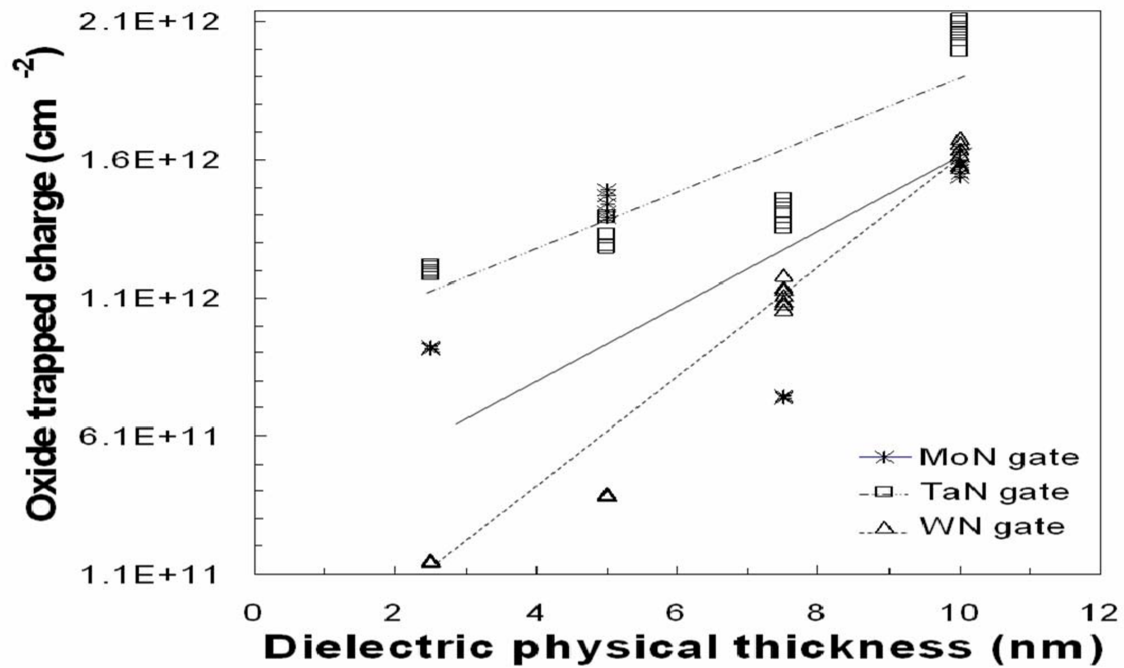


Figure 72 The variation of the oxide trapped charge Q_{ot} as a function of undoped ALD deposited HfO_2 gate dielectric thickness for each gate electrode at 800°C PMA condition.

6.5. Summary

TaN, MoN, and WN were investigated as gate electrodes for a 2.5 nm thick HfO_2 high-k dielectric material. Their physical and electrical properties were affected by the PMA treatment conditions. Serious interaction was observed at the TaN/HfO_2 interface after 800°C PMA and a top interface layer containing Ta, Hf, O, and N atoms was formed, which lead to an increase of EOT and bulk charge density. No significant interaction occurred at the WN/HfO_2 or MoN/HfO_2 interface. The metallic W was formed after 800°C PMA, which lead to a high leakage current density. The gate electrode material also affected the bottom interface's electrical properties. A thick bottom interface layer was formed at the HfO_2/Si interface for the sample with a MoN gate electrode, which lead to a high EOT after a high temperature PMA. Work functions of these three gate electrodes are suitable for NMOS applications after 800°C PMA. In summary, metal nitrides can be used as the gate electrode materials for the HfO_2 high-k film. However, when interpreting electrical properties, the deposition and after-deposition process conditions have to be specified carefully.

CHAPTER VII

SUMMARY AND CONCLUSION

Various Hf-doped TaO_x gate dielectric materials were deposited by the RF reactive co-sputtering. Material and electrical properties were studied by XPS, SIMS, HRTEM, C-V, and I-V. Influences of process parameters, e.g., Hf co-sputtering power, post-deposition annealing temperature, and annealing time, to high-k properties were investigated. The Hf dopant affects both the bulk and interface structures of the TaO_x film. The XPS and SIMS data showed the binding energy shifts and the composition changes with the dopant concentration. The interface layer thickness was reduced by the doping process, too. The moderately and heavily Hf-doped TaO_x thin films formed thinner interface layers at the silicon contact region than the un-doped TaO_x or lightly Hf-doped TaO_x films. The annealing time affected the interface layer thickness change more pronouncedly at the short period than at the long period. The incorporation of Hf into TaO_x impacted the electrical properties. The doping process improved the effective dielectric constant, reduced the fixed charge density, and increased the better dielectric strength. The leakage current density in the film decreased with the Hf concentration. However, the heavily Hf-doped TaO_x film suffered from the low dielectric breakdown strength and its dielectric constant was slightly higher than that of the un-doped TaO_x film. High temperature post-deposition O_2 annealing effectively reduced the defect charges in the high-k stack structures. The Hf-doped TaO_x films have many advantages

over the un-doped TaO_x and HfO_x films. Therefore, doping is a promising method in preparing high quality gate dielectric materials for the future generation CMOS devices.

Lightly Hf-doped TaO_x high-k gate dielectric films with physical thickness less than 5 nm were prepared into MOS capacitors. Sub-2 nm thick EOTs have been demonstrated and studied. The low leakage currents and high dielectric constants of the doped films were explained by their compositions and bond structures. The Hf-doped TaO_x film contains $HfSi_xO_y$ in the interface layer irrespective of the PDA atmosphere. However, the O_2 annealed film contains more oxidized bulk film and less silicate-rich interface layer. The energy band gaps in doped and un-doped films could be explained by the film structure. The lightly Hf-doped TaO_x film is a potential high-k gate dielectric for future MOS transistors.

5 Å TaN_x interface layer was inserted between the doped TaO_x films and the Si substrate. The electrical characterization result shows that the TaN_x interface layer could decrease the film's leakage current density and improve the $k_{effective}$ value. The improvement of these dielectric properties can be attributed to the formation of the TaO_xN_y interfacial layer after high temperature O_2 annealing. The SIMS and XPS results also show that existence of N and Hf in the interface formed between the Hf-doped TaO_x films and Si wafer. The high-k dielectric film's properties are improved by the combination of doping the bulk film and inserting a thin TaN_x interface layer although a complicated multi-layer interface layer is formed. The main drawback is the high interface density of states and hysteresis, which needs to be lowered down.

TaN, MoN, and WN were deposited by RF reactive sputtering on HfO_2 high-k dielectric material to as gate electrodes to form MOS capacitors. Their physical and

electrical properties were affected by the PMA treatment conditions. Serious interaction was observed at the TaN/HfO_2 interface after 800°C PMA and a top interface layer containing Ta, Hf, O, and N atoms was formed, which lead to an increase of EOT and bulk charge density. No significant interaction occurred at the WN/HfO_2 or MoN/HfO_2 interface. The metallic W was formed after 800°C PMA, which lead to a high leakage current density. The gate electrode material also affected the bottom interface's electrical properties. A thick bottom interface layer was formed at the HfO_2/Si interface for the sample with a MoN gate electrode, which lead to a high EOT after a high temperature PMA. Work functions of these three gate electrodes are suitable for NMOS applications after 800°C PMA. Metal nitrides can be used as the gate electrode materials for the HfO_2 high-k film.

REFERENCES

1. G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys.*, **89**, 5243 (2001).

2. M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, *J. Appl. Phys.*, **90**, 2057 (2001).

3. M. Houssa, *High-k Gate Dielectrics*, Institute of Physics Publishing, Bristol, UK (2004).

4. T. Hori, *Gate Dielectrics and MOS ULSIs: Principles, Technologies, and Applications*, Springer, Berlin, Germany (1997).

5. S. Wolf, *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*, Vol. 4, 1st ed., Lattice Press, Sunset Beach, CA (2002).

6. R. Dennard, F. Gaenssle, H. Yu, V. Rideout, E. Bassous, and A. Leblanc, *IEEE J. Solid-State Circuit*, **SC 9**, 256 (1974).

7. H. C. Casey, Jr., *Devices for Integrated Circuits: Silicon and III-V Compound Semiconductors*, John Wiley & Sons, New York (1999).

8. G. E. Moore, *Electron.*, **38**, 114 (1965).

9. Intel® website http://www.intel.com/research/silicon/mooreslaw.htm., (accessed on September 2005)

10. S. Thompson, P. Packan, and M. Bohr, *Intel Technol. J.*, **Q3**, 1 (1998).

11. *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, San Jose, CA (2001).

12. S-H. Lo, D.A. Buchanan, Y. Taur and W. Wang, *IEEE Electron Device Lett.*, **18**, 209 (1997).

13. R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 45.

14. B. E. Weir, P.J. Silverman, M. A. Alam, F. Baumann, D. Monroe, A. Ghetti, J. D. Bude, G. L. Timp, A. Hamid, T. M. Oberdick, N. X. Zhao, Y. Ma, M. M. Brown, D. Hwang, T. W. Sorsch, and J. Madic, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 437.

15. G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cireli, V.

Donnelly, M. Foad D. Grant, and M. Green, *Tech. Dig. - Int. Electron Devices Meet.*, **1997**, 930.

16. G. Timp, K. K. Bourdelle, J. E. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, and H. Gossmann, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 615.

17. G. Timp, J.Bude, K.K. Bourdelle, J. Garno, A. Ghetti, H. Gossmann, M. Green, G. Forsyth, Y. Kim, and R. Kleimann, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 55.

18. B. Yu, H. Wang, C. Riccobene, Q. Xiang, and M. Lin, *VLSI Tech. Symp. Dig.*, **2000**, 90.

19. R. Degraeve, N. Pangon, B. Kaczer, T. Nigam, G. Groeseneken, and A. Naem, *VLSI Tech. Symp. Dig.*, **1999**, 59.

20. B. E. Weir, P. J. Silverman, M. A. Alam, F. Baumann, D. Monroe, A. Ghetti, J. D. Bude, G. L. Timp, A. Hamad, and T. M. Oberdick, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 437.

21. M. Alam, B. Weir, P. Silverman, J. Bude, A. Ghetti, Y. Ma, M. M. Brown, D. Hwang, and A. Hamad, *Electrochem Society Proceeding Series*, p. 365 (2002).

22. H. Iwai, H. S. Momose, and S. Ohmi, *Electrochem Society Proceeding Series,* **2000**, 3.

23. J. H. Stahis, A. Vayshenker, P. R. Varekamp, E. Y. Yu, C. Montrose, J. McKenna, D. J. DiMaria, L.-K. Han, E. Cartier, R. A. Wachnik, and B. P. Linder, *VLSI Tech. Symp. Dig.*, **2000**, 94.

24. D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, *Nature*, **399**, 758 (1999).

25. S. Tang, R. M. Wallace, A. Seabaugh, and D. King-Smith, *Appl. Surf. Sci.*, **135**, 137 (1998).

26. J. B. Neaton, D. A. Muller, and N. W. Ashcroft, *Phys. Rev. Lett.*, **85**, 1298 (2000).

27. A. A. Demkov and O. F. Sankey, *Phys. Rev. Lett.*, **83**, 2038 (1999).

28. S. V. Hattangady, R. Kraft, D. T. Grider, M. A. Douglas, G. A. Brown, P. A. Tiner, J. W. Kuehne, P. E. Nicollian, and M. F. Pas, *Tech. Dig. - Int. Electron Devices Meet.*, **1996**, 495.

29. Y. Wu, and G. Lucovsky, *IEEE Electron Device Lett.*, **19**, 367 (1998).

30. X. W. Wang, Y. Shi, and T. P. Ma, *VLSI Tech. Symp. Dig.*, **1995**, 109.

31. H. Yang and G. Lucovsky, *Tech. Dig. Int. Electron Devices Meet.*, **1999**, 245.

32. V. Misra, H. Lazar, M. Kulkarni, Z. Wang, G. Lucovsky, and J. R. Hauser, *Mater. Res. Soc. Symp. Proc.*, **567**, 89 (1999).

33. M. Khare, X.W. Wang, and T.P. Ma, *IEEE Electron Device Lett.*, **20**, 57 (1999).

34. C. Y. Wong, J. Y. Sun, Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 238.

35. B. Yu, D. H. Ju, W. C. Lee, N. Kepler, T. J. King, and C. Hu, *IEEE Trans. Electron Devices*, **45**, 1253 (1998).

36. B. Ricco, R. Versari, and D. Esseni, *IEEE Electron Device Lett.*, **17**, 103 (1996).

37. J. R. Hauser and K. Ahmed, in *Characterization and Metrology for ULSI Technology: 1998 International Conference*, D. G. Seiler, A. C. Diebold, W. M. Bullis, T. J. Shaffner, R. McDonald, and E. J. Walters, Editors, p. 235, The American Institute of Physics, Melville, NY (1998).

38. Intel® website http://www.intel.com/technology/silicon/., (accessed on September, 2005)

39. K. J. Hubbard and D. G. Schlom, *J. Mater. Res.*, **11**, 2757 (1996).

40. A. Chin, C. C. Liao, C. H. Liu, W. J. Chen, and C. Tsai , *VLSI Tech. Symp. Dig.*, **1999**, 135.

41. A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, Symp. *VLSI Tech. Symp. Dig.*, **2000**, 16.

42. D.A. Buchanan, E.P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D Emic, P. Kozlowski, K. Chen, R.J. Fleming, P.C. Jamison, J. Browin, and R. Ardnt, *Tech. Dig. Int. Electron Devices Meet.*, **2000**, 223.

43. S. Guha, E. Cartier, M.A. Gribelyuk, N.A. Bojarczuk, and M.C. Copel, *Appl. Phys. Lett.*, **77**, 2710 (2000).

44. Y. H. Wu, M.Y. Yang, A. Chin, W.J. Chen, and C.M. Kwei, *IEEE Electron Device Lett.*, **21**, 341 (2000).

45. J. Kwo, M. Hong, A.R. Kortan, K.T. Queeney, Y.J. Chabal, J.P. Mannaerts, T. Boone, J.J. Krajewski, A.M. Sergent, and J. M. Rosamilia, *Appl. Phys. Lett.*, **77**, 130 (2000).

46. W.-J. Qi, R. Nieh, B. H. Lee, L. G. Kang, Y. Jeon, and J. C. Lee, *Appl. Phys. Lett.*, **77**, 3269 (2000).

47. W.-J. Qi, R. Nieh, B. H. Lee, L. G. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 145.

48. B. H. Lee, L. Kang, R. Nieh, W. J. Qi and J. C. Lee, *Appl. Phys. Lett.*, **76**, 1926 (2000).

49 G. D. Wilk and R. M. Wallace, *Appl. Phys. Lett.*, **74**, 2854 (1999).

50 G. D. Wilk and R. M. Wallace, *Appl. Phys. Lett.*, **76**, 112 (2000).

51 G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys.*, **87**, 484 (2000).

52. J. A. Duffy, *Bonding Energy Levels and Bands in Inorganic Solids*, John Wiley & Sons, New York (1990).

53. R. Liu, S. Zollner, P. Fejes, R. Gregory, S. Lu, K. Reid, D. Gilmer, B. Y. Nguyen, Z. Yu, R. Droopad, J. Curless, A. Demkov, J. Finder, and K. Eisenbeiser, *Mater. Res. Soc. Symp. Proc.*, **670**, K1.1.1 (2001).

54. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., John Wiley & Sons, New York (1981).

55. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, John Wiley & Sons, New York (1982),

56. J. Robertson, *J. Vac. Sci. Technol. B*, **18**, 1785 (2000),

57. J. Robertson and C. W. Chen, *Appl. Phys. Lett.*, **74**, 1168 (1999).

58. R. Beyers, *J. Appl. Phys.*, **56**, 147 (1984).

59. S. Q. Wang and J. W. Mayer, *J. Appl. Phys.*, **64**, 4711 (1988).

60. I. Barin and O. Knacke, *Thermochemical Properties of Inorganic Substances,* Springer, Berlin, (1973).

61. L. B. Pankratz, *Thermodynamic Properties of Elements and Oxides,* U.S. Dept. of Interior, Bureau of Mines Bulletin 672, U.S. Govt. Printing Office, Washington, D.C., (1982).

62. S. P. Murarka, *Silicides for VLSI Applications,* Academic, New York, (1983).

63. S. Ezhilvalavan and T.-Y. Tseng, *J. Mater. Sci. - Mater. Electron.*, **10**, 9 (1999).

64. C. Chaneliere, J. L. Autran, R. A. B. Devine, and B. Balland, *Mater. Sci. Eng.*, **R22**, 269 (1998).

65. K. Eisenbeiser, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopad, W. J. Ooms, L. Salem, S. Bradshaw, and C. D. Overgaard, *Appl. Phys. Lett.*, **76**, 1324 (2000).

66. C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, and E. Shero, *Appl. Phys. Lett.*, **81**, 1417 (2002).

67. E. P. Gusev, J. Cabral, C. M. Copel, C. D'Emic, and M. Gribelyuk, *Microelectron. Eng.*, **69**, 145 (2003).

68. J.-Y. Tewg, Y. Kuo, and J. Lu, *Electrochem. Solid-State Lett.*, **8**, G27 (2005).

69. G. Lucovsky, Y. Wu, H. Niimi, V. Misra, and J. C. Phillips, *Appl. Phys. Lett.*, **74**, 2005 (1999).

70. A. Kumar, D. Rajdev, and D. L. Douglass, *J. Am. Chem. Soc.*, **55**, 439 (1972).

71. Y. Takaishi, M. Sakao, S. Kamiyama, H. Suzuki, and H. Watanabe, *Tech. Dig. - Int. Electron Devices Meet.*, **1994**, 839.

72. F. Rubio, J. Denis, J. M. Albella, and J. M. Martinez-Duart, *Thin Solid Films*, **90**, 405 (1982).

73. J. L. Autran, R. A. B. Devine, C. Chaneliere, and B. Balland, *IEEE Electron Device Lett.*, **18**, 447 (1997).

74. K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, *Appl. Phys. Lett.*, **68**, 3737 (1996).

75. R. Polzius, T. Schneider, F. F. Biert, and U. Bilitewski, *Biosens. Bioelectron.*, **11**, 503 (1996).

76 S. Kimura, Y. Nishioka, A. Shintani, and K. Mukai, *J. Electrochem. Soc.*, **130**, 2414 (1983).

77 J. Robertson, *Appl. Surf. Sci.*, **190**, 2 (2002).

78 P. W. Peacock and J. Robertson, *J. Appl. Phys.*, **92**, 4712 (2002).

79 F. C. Chiu, J. J. Wang, J. Y. Lee, and S. C. Wu, *J. Appl. Phys.*, **81**, 6911 (1997).

80. H. Fujikawa and Y. Taga, *J. Appl. Phys.*, **75**, 2538 (1994).

81. K. Nomura, H. Ogawa, and A. Abe, *J. Electrochem. Soc.*, **134**, 922 (1987).

82. K. Nomura and H. Ogawa, *J. Electrochem. Soc.*, **138**, 3701 (1991).

83. R. F. Cava, W. F. Peck, and J. J. Krajewski, *Nature*, **377**, 215 (1995).

84. R. J. Cava, W. F. Peck, J. J. Krajewski, G. L. Roberts, B. P. Barber, H. M. O'Bryan, and P. L. Gammel, *Appl. Phys. Lett.*, **70**, 1396 (1997).

85. R. J. Cava and J. J. Krajewski, *J. Appl. Phys.*, **83**, 1613 (1998).

86. L. Manchanda, M. D. Morris, M. L. Green, R. B. van Dover, F. Klemens, T. W. Sorsch, P. J. Silverman, G. D. Wilk, B. Busch, and S. Aravamudhan, *Microelectron. Eng.*, **59**, 351 (2001).

87. S. Miyazaki, *Appl. Surf. Sci.*, **190**, 66 (2002).

88. R. M. Fleming, D. V. Lang, C. D. W. Jones, M. L. Steigerwald, D. W. Murphy, G. B. Alers, Y. H. Wong, R. B. van Dover, J. R. Kwo, and A. M. Sergent, *J. Appl. Phys.*, **88**, 850 (2000).

88. M. A. Gribelyuk, A. Callegari, E. P. Gusev, M. Copel, and D. A. Buchanan, *J. Appl. Phys.*, **92**, 1232 (2002).

89. H. Watanabe, *Appl. Phys. Lett.*, **78**, 3803 (2001).

90. P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, and J. G. Ekerdt, *J. Appl. Phys.*, **91**, 4353 (2002).

91. H. Shinriki, Y. Nishioka, Y. Ohji, and K. Mukai, *IEEE Trans. Electron Devices*, **36**, 328 (1989).

92. S. O. Kim and H. J. Kim, *Thin Solid Films*, **253**, 435 (1994).

93. H. J. Cho, D. G. Park, I. S. Yeo, J. S. Roh, and J. W. Park, *Jpn. J. Appl. Phys.*, **40**, 2814 (2001).

94. Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii, and T. Nakamura, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 861.

95. C. Y. Wong, J. Y.Sun, Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, *Tech. Dig. - Int. Electron Devices Meet.*, **1988**, 238.

96. A. Chatterjee, R. A. Chapman, K. Joyner, M. Otobe, S. Hattangady, M. Bevan, G. A. Brown, H. Yang, Q. He, D. Rogers, S. J. Fang, R. Kraft, A. L. P. Rotondaro, M. Terry, K. Brennan, S.-W. Aur, J. C. Hu, H.-L. Tsai, P. Jones, G. D. Wilk, M. Aoki, M. Rodder, and I.-C. Chen, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 777.

97. H. Zhong, G. Heuss, and V. Misra, *IEEE Electron Device Lett.*, **21**, 593 (2000)

98. M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Materials Processing*, John Wiley & Sons, Ltd., New York (1994).

99. S. K. Ghandhi, *VLSI Fabrication Principles, Silicon and Gallium Arsenide*, John Wiley & Sons, Ltd., New York (1994).

100. S. A. Campbell, *The Science and Engineering of Microelectronics Fabrication*, Oxford University Press, Oxford, UK (1996).

101. H. G. Tompkins and W. A. McGahan, *Spectroscopic Ellipsometry and Reflectometry - A User's Guide*, John Wiley & Sons, Ltd., New York (1999).

102. F. G. Bell and L. Ley, *Phys. Rev. B*, **37**, 8383 (1988)

103. R. Puthenkovilakam and J. P. Chang, *Appl. Phys. Lett.*, **84**, 1353 (2004).

104. D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed., John Wiley & Sons, New York (1998).

105. W. L. Bragg, *Proc. Camb. Phil. Soc.*, **17**, 43 (1913).

106. D. L. Chung, P. W. De Haven, H. Arnold, and D. Ghosh, *X-Ray Diffraction at Elevated Temperatures: A Method for In-Situ Process Analysis*, Chap. 1, VCH Publishers, New York (1993).

107. P. J. Spencer, *Hafnium: Physico-chemical Properties of Its Compound and Alloys*, Atomic Energy Review No. 8, P.25, IAEA, Vienna (1981).

108. M. Balog, M. Schieber, M. Michiman, and S. Patai, *Thin Solid Films*, **41**, 247 (1977).

109. W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, *IEEE Electron Device Lett.,* **23**, 649, (2002).

110. B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Joen, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 133.

111. J.-Y. Tewg, Y. Kuo, J. Lu, and B. Schueler, *J. Electrochem. Soc.*, **151**, F59

(2004).

112. H. Zhang and R. Solanki, *J. Electrochem. Soc.*, **118**, F63 (2001).

113. K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, *J. Electrochem. Soc.*, **144**, 300 (1997).

114. J.-Y. Tewg, Y. Kuo, and J. Lu, *Electrochem. Solid-State Lett.*, **8**, G27 (2005).

115. T. L. Barr, *J. Vac. Sci. Technol. A*, **9**, 1793 (1991).

116. M. J. Guittet, J. P. Crocombett, and M. Gautier, *Phys. Rev. B,* **63**, 125117 (2001).

117. G. Lucovsky, J. L. Whitten, and Y. Zhang, *Solid-State Electron.,* **46**, 1687 (2002).

118. G. Lucovsky, in *Proceedings of the International Workshop on Gate Insulator*, S. Ohmi, K. Fujita, and H. S. Momose, Editors, p. 14, Japan Society of Applied Physics, Japan (2001).

119. G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, *Appl. Phys. Lett.,* **73**, 1517 (1998).

120. O. Renault, D. Samour, D. Rouchon, P. Holliger, A. -M. Papon, D. Blin and S. Marthon, *Thin Solid Films*, **428**, 190 (2003).

121. T. Yamamoto, N. Morita, N. Sugiyama, A. Karen, and K. Okuno, *Appl. Surf. Sci.*, **203-204**, 519 (2003).

122. H. Wong, K. L. Ng, Nian Zhan, M. C. Poon, and C. W. Kok, *J. Vac. Sci. Technol. B*, **22**, 1094 (2004).

123. W. Nieveen, B. W. Schueler, G. Goodman, P. Schnabel, J. Moskito, I. Mowat and G. Chao, *Appl. Surf. Sci.*, **231-232**, 556 (2004).

124. H. Ono, Y. Hosokawa, T. Ikarashi, K. Shinoda, N. Ikarashi, K. Koyanagi, and H. Yamaguchi, *J. Appl. Phys.,* **89**, 995 (2001).

125. R. S. Johnson, J. G. Hong, C. Hinkle, and G. Lucovsky, *Solid-State Electron.*, **46**, 1799 (2002).

126. R. A. B. Devine and A. G. Revesz, *J. Appl. Phys.,* **90**, 389 (2001).

127. G. Lucovsky and B. Rayner, *Appl. Phys. Lett.,* **77**, 2912 (2000).

128. G. Lucovsky, G. B. Rayner, D. Kang, G. Appel, R. S. Johnson, Y. Zhang, D. E. Sayers, H. Ade, and J. L. Whitten, *Appl. Phys. Lett.*, **79**, 1775 (2001).

129. G. Lucovsky, Y. Zhang, G. B. Rayner, G. Appel, H. Ade, and J. L. Whitten, *J. Vac. Sci. Technol. B*, **20**, 1739 (2002).

130. L. Kang, B. H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, *IEEE Electron Device Lett.*, **21**, 181 (2000).

131. M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, *Appl. Phys. Lett.*, **77**, 1885 (2000).

132. R. Nieh, R. Choi, S. Gopalan, K. Onishi, C. S. Kang, H.-J. Cho, S. Krishnan, and J. C. Lee, *Appl. Phys. Lett.*, **81**, 1663 (2002).

133. K. Lehovec, *Solid-State Electron.*, **11**, 135 (1968).

134. K.-J. Choi, W.-C. Shin, and S.-G. Yoon, *J. Electrochem. Soc.*, **149**, F18 (2002).

135. M. A. Green, F. D. King, and J. Shewchun, *Solid-State Electron.,* **17**, 551 (1974).

136. A. Ghetti, C. Liu, M. Mastrapasqua, and E. Sangiorgi, *Solid-State Electron.,* **44**, 1523 (2000).

137. J.-F. Damlencourt, O. Renault, D. Samour, A.-M. Papon, C. Leroux, F. Martin, S. Marthon, M.-N. Semeria, X. Garros, *Solid-State Electron.*, **47**, 1613 (2003).

138. O. Renault, D. Samour, J.-F. Damlencourt, D. Blin, F. Martin, S. Marthon, N. T. Barrett, and P. Besson, *Appl. Phys. Lett.*, **81**, 3627 (2002).

139. J.-Y. Tewg, Y. Kuo, and J, Lu, *J. Electrochem. Soc.*, **152**, G643 (2005).

140. V. V. Afanas'ev, A. Stesmans, C. Zhao, M. Caymax, Z. M. Rittersma, and J. W. Maes, *Appl. Phys. Lett.*, **86**, 072108 (2005).

141. H. Demiryont, J. R. Sites, and K. Geib, *Appl. Opt.*, **24**, 490 (1985).

142. W. H. Lee, J. C. Lin and C. Lee, Mater. *Chem. and Phys.*, **68**, 267 (2001)

143. V. P. Kolonits, M. Czermann, O. Geszti and M. Menyhárd, *Thin Solid Films,* **45-55**, 123 (1985).

144. A. Arranz and C. Palacio, *Vacuum*, **45**, 1091 (1994).

145. H. Jung, K. Lm and H. Hwang, *Appl. Phys. Lett.*, **76**, 3630 (2000).

146. G. B. Alers, R. M. Fleming, Y. H.Wong, B. Dennis, A. Pinczuk, G. Redinbo, R. Urdahl, E. Ong and Z. Hasan, *Appl. Phys. Lett.*, **72** 1308 (1998).

147. S. Choi, S. Jeon, M. Cho and H. Hwang, *Jpn. J. Appl. Phys.*, **42**, L102 (2003).

148. A. Teramoto, H. Umeda, H. Tamura, Y. Nishida, H. Sayama, K. Terada, K. Kawase, Y. Ohno and A. Shigetomi, *J. Electrochem.Soc.*, **147**, 1888, (2000).

149. R. P. Vasquez and A. Madhukar, *Appl. Phys. Lett.*, **47**, 998 (1985).

150. B. H. Lee R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W. J. Qi, C. Kang and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 39.

151. Y-S. Lai, K-J. Chen and J-S. Chen, *J. Electrochem. Soc.*, **149**, F63 (2002).

152. A. O. Ibidunni, R. L. Masaitis, R. L. Opila, A. J. Davenport, H. S. Isaacs and J. A. Taylor. *Surf. Interface Anal.*, **20**, 559 (1993).

153. D. C. Gilmer, R. Hegde, R. Cotton, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, R. Rai, L. Prabhu, C. Hobbs, J. M. Grant, L. La, S. Samavedam, and B. Taylor, *Appl. Phys. Lett.*, **81**, 1288 (2002).

154. H. F. Luan, B. Z. Wu, L. G. Kang, R. Vrtis, D. Roberts, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 609.

155. C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, Y. Senzaki, D. Roberts, and D. L. Kwing, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 27.

156. K. Chen, M. Chan, P. K. Ko, C. Hu, and J. H. Huang, *Solid-State Electron.*, **38**, 1975 (1995).

157. N. D. Arora, R. Rios, and C. L. Huang, *IEEE Trans. Electron Devices.*, **42**, 935 (1995).

158. B. Yu, D. H. Ju, N. Kepler, T. J. King, and C. Hu, *VLSI Tech. Symp. Dig.*, **1997**, 155.

159. I. De, D. Johri, A. Srivastava, and C. M. Osburn, *Solid-State Electron.*, **44**, 1077 (2000).

160. E. Cartier, J. H. Stathis, and D. A. Buchanan, *Appl. Phys. Lett.*, **63**, 1510 (1993).

161. R. Pretorius, J. M. Harris, and M. -A. Nicolet, *Solid-State Electron.*, **21**, 667 (1978).

162. J. S. Reid, E. Kolawa, R. P. Ruiz, and M.-A. Nicolet, *Thin Solid Films*, **236**, 319

(1993).

163. G. S. Sandhu, *Thin Solid Films*. **320**, 1 (1998).

164. H. Li, S. Jin, H. Bender, F. Lanckmans, I. Heyvaert, K. Maex, and L. Froyen, *J. Vac. Sci. Technol. B.,* **18**, 242 (2000).

165. H. Wakabayashi, Y. Saito, K. Takeuchi, T. Mogami, and T. Kunio, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 253.

166. Q. Lu, R. Ronald, P. Ranade, T. J. King, and C. Hu, *VLSI Tech. Symp. Dig.*, **2001**, 45.

167. Y. S. Suh, G. Heuss, H. Zhong, S. N. Hong, and V. Misra, *VLSI Tech. Symp. Dig.*, **2001**, 47.

168. H. B. Nie, S. Y. Xu, S. J. Wang, L. P. You, Z. Yang, C. K. Ong, J. Li, and T. Y. F. Liew, *Appl. Phys. A.*, **73**, 229 (2001)

169. Y. G. Shen and Y. W. Mai, *Mater. Sci. Eng. B - Solid State Mater. Adv. Technol.*, **95**, 222 (2002).

170. Y. G. Shen, *Mater. Sci. Eng. A - Struct. Mater. Prop. Microstruct. Process.*, **359**, 158 (2003).

171. J. K. Schaeffer, S. B. Samavedam, D. C. Gilmer, V. Dhandapani, P. J. Tobin, J. Mogab, B. –Y. Nguyen, B. E. White, Jr., S. Dakshina-Murthy, R. S. Rai, Z. –X. Jiang, R. Martin, M. V. Raymond, M. Zalava, L. B. La, J. A. Smith, R. Garcia, D. Roan, M. Kottke, and R. B. Gregory, *J. Vac. Sci. Technol. B*, **21**, 11 (2003).

172. D. Ko, B. Park, Y. Kim, and J. Ha, et al. *1996 Advanced Metallization and Interconnect Systems for ULSI Application* in 1995. pp. 257-64. Pittsburgh, Mater. Res. Soc.

173. W. Hume-Rothery, *Acta Metall.*, **14**, 17 (1966).

174. H. Y. Yu, J. F. Kang, C. Ren, J. D. Chen, Y. T. Hou, C. Chen, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, and D. -L. Kwong, *IEEE Electron Device Lett.*, **25**, 70 (2004).

175. K. -Y. Choi and S. -G. Yoon, Electrochem. *Solid State Lett.*, **7** G47 (2004)

176. B. -Y. Tsui and C. -F. Huang, *J. Electrochem. Soc.*, **150**, G22 (2003)

177. N. Terao, *Jpn. J. Appl. Phys.,* **10**, 248 (1971).

178. Y. Kuo, J. Lu, and J.-Y. Tewg, *Jpn. J. Appl. Phys.*, **42**, L769 (2003)

179. J. Lu, Y. Kuo, J.-Y. Tewg, and B. Schueler, *Vacuum*, **74**, 539 (2004).

180. J. W. Lee, C. H. Han, J. -S. Park, and J. W. Park, *J. Electrochem. Soc.*, **148**, G95 (2001).

181. T. Yamada, M. Moriwaki, Y. Harshinao, S. Fujii, and K. Eriguchi, *Microelectron. Reliab.*, **41**, 697 (2001).

182. R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee, and V. Misra, *IEEE Electron Device Lett.*, **25**, 420 (2004).

183. H. Y. Yu, J. F. Fang, C. Ren, J. D. Chen, Y. T. Hou, C. Shen, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, and D. -L. Kwong, *IEEE Electron Device Lett.*, **25**, 70 (2004).

184. W. A. Hill, C. C. Coleman, *Solid-State Electron.*, **23**, 987 (1980).

185. H. -J. Cho, T. -H. Cha, K. -Y. Lim, D. -G. Park, J.-Y. Kim, J. -J. Kim, S. Heo, I. -S Yeo, and J. W. Park, *J. Electrochem. Soc.*, **149**, G403 (2002)

186. D. G. Park, K. Y. Lim, H. J. Cho, T. H. Cha, I. S. Yeo, J. S. Roh, and J. W. Park, *Appl. Phys. Lett.*, **80**, 2514 (2002).

187. H. Matsuhashi, S. Nishikawa, and S. Ohno, *Jpn. J. Appl. Phys.*, **28**, L2309 (1989)

188. J.-Y. Tewg, Y. Kuo, J, Lu, and B. Schueler, *J. Electrochem. Soc.*, **152**, G617 (2005).

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- **J. Lu**, Y. Kuo, and J. -Y. Tewg, "Hafnium-doped Tantalum Oxide High-K Gate dielectrics", J. Electrochem. Soc., Submitted, June 2005.
- Y. Kuo, **J. Lu**, and H. Nominanda, "Sputter Deposition of nm-Thick Films for Passivation of Organic Pellicles", Vacuum, Submitted, June 2005.
- **J. Lu**, Y. Kuo, S. Chatterjee, and J. -Y. Tewg, "Metal Nitride Gate Electrode Effects on Dielectric Properties of HfO_2 High-k Gate Dielectrics", J. Vac. Sci. Technol B, Submitted, May 2005.
- J.-Y. Tewg, Y. Kuo, **J. Lu**, and B. W. Schueler, "Influence of a 5 Å Tantalum Nitride Interface Layer on Dielectric Properties of Zirconium-Doped Tantalum Oxide High-k Films", J. Electrochem. Soc., 152, G617 (2005).
- J.-Y. Tewg, Y. Kuo, and **J. Lu**, "Zirconium-Doped Tantalum Oxide Gate Dielectric Films Integrated with Molybdenum, Molybdenum Nitride, and Tungsten Nitride Gate Electrodes", J. Electrochem. Soc., 152, G643 (2005).
- J.-Y. Tewg, Y. Kuo, and **J. Lu**, "Suppression of Crystallization of Tantalum Oxide Thin Film by Doping with Zirconium", Electrochem. Solid-State Lett., 8, G27 (2005).
- J.-Y. Tewg, Y. Kuo, **J. Lu**, and B. W. Schueler, "Electrical and Physical Characterization of Zirconium-Doped Tantalum Oxide Thin Films", J. Electrochem. Soc., 151(3), F59-F67, 2004.
- **J. Lu**, Y. Kuo, J. -Y. Tewg, and B. Schueler, "Effects of the TaNx Interface Layer on Doped Tantalum Oxide High-k Films", Vacuum, 74(3-4), 539-547, 2004.
- Y. Kuo, **J. Lu**, and J.-Y. Tewg, "Tantalum Nitride Interface Layer Influence on Dielectric Properties of Hafnium Doped Tantalum Oxide High Dielectric Constant Thin Films", Jpn. J. Appl. Phys., 42(7A), L769-L771, 2003.

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