VOLTAGE SENSING BASED BUILT-IN CURRENT SENSOR FOR I_{DDQ} TEST

A Dissertation

by

BIN XUE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2005

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Duncan M. Walker
Committee Members,	Jyh-Charn Liu
	Rabinarayan Mahapatra
	Henry F. Taylor
Head of Department,	Valerie E. Taylor

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ABSTRACT

Voltage Sensing Based Built-In Current Sensor for I_{DDQ} Test.

(December 2005)

Bin Xue, B.S., Xiamen University, China;

M.S., National University of Singapore

Chair of Advisory Committee: Dr. Duncan M. Walker

Quiescent current leakage test of the V_{DD} supply (I_{DDQ} Test) has been proven an effective way to screen out defective chips in manufacturing of Integrated Circuits (IC). As technology advances, the traditional I_{DDQ} test is facing more and more challenges. In this research, a practical built-in current sensor (BICS) is proposed and the design is verified by three generations of test chips. The BICS detects the signal by sensing the voltage drop on supply lines of the circuit under test (CUT). Then the sensor performs analog-to-digital conversion of the input signal using a stochastic process with scan chain readout. Self-calibration and digital chopping are used to minimize offset and low frequency noise and drift. This non-invasive procedure avoids any performance degradation of the CUT. The measurement results of test chips are presented. The sensor achieves a high I_{DDQ} resolution with small chip area overhead. This will enable I_{DDQ} of future technology generations.

DEDICATION

To my wife, my parents and my sister: without their support this wouldn't have been possible. And to my little sweetheart, Rochelle, who just turned 10 months old.

ACKNOWLEDGMENTS

First I would like to express my thankfulness to my advisor, Dr. Duncan M. (Hank) Walker, to whom I owe a lot. His insights in this particular research area, his technical guidance and spiritual support were invaluable to this work. Like other students under his guidance, I am also thankful to his patience and care for me and my family.

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1. INTRODUCTION

1.1 Introduction

The evaluation of the reliability and quality of a digital integrated circuit (IC) is commonly called "testing." As technology advances, the testing of integrated circuits is gaining in importance. Technology is so advanced that billions of transistors have been integrated into a chip. Moore's Law [1], which projects that the number of transistors per unit area doubles approximately every 18 months, has proven correct for the past few decades, and will continue to hold for at least a decade or more. The International Technology Roadmap for Semiconductors (ITRS) [2] has outlined the projections for future developments in the semiconductor industry and these projections are frequently updated to keep up with development.

At the present time, testing constitutes a large portion (~30%) of the total chip cost and the trend is that test cost will continue to rise. Decreasing silicon costs together with increasing complexity of integrated circuits are two of the most important elements of this trend [3]. The increasing complexity of ICs requires more efficient and effective test methodologies and techniques, otherwise the percentage of test cost is expected to increase even further. In addition, conventional fault models have their inherent limitations, which may lead to poor test quality and cause a significant increase in the

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This dissertation follows the style and format of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.*

overall cost of ICs. So it is becoming more evident that novel test techniques must be developed to keep up with technology advances, while keeping the total test cost at a reasonable level.

In order to ship only products of high quality and reliability to customers, IC manufacturers must ensure that fabricated chips conform to a series of strict specifications. This is accomplished by performing various tests at different stages of chip manufacturing, as shown in Fig. 1.

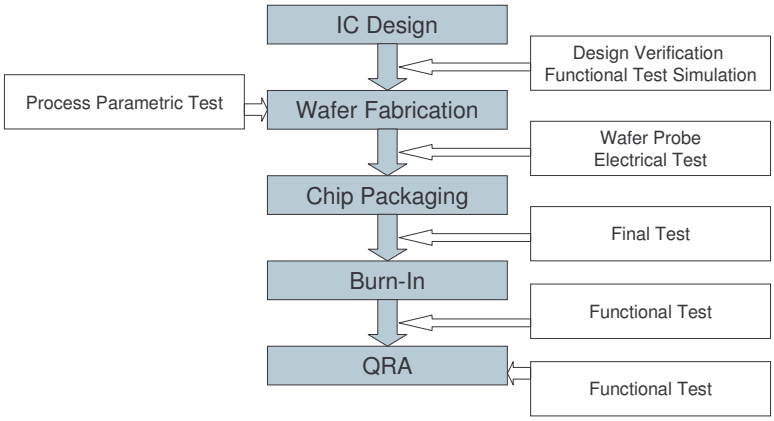

Fig. 1. Semiconductor IC test at each stage during fabrication.

The very first "test" is performed at the design phase and is called verification. The prototype design is "tested" to ensure that it matches its functional objectives, in other words, to verify the correctness of the design. Verification checks that all layout design rules are obeyed. Verification also checks the circuit to ensure the circuit performs the

intended functionality through circuit simulation with actual process electrical parameters.

The rest of the tests fall into two broad categories: *Boolean tests* and *parametric tests*. Boolean tests are straightforward in that failure (*hard fault*) conclusively detects chip malfunction. So it is a go/no-go type of test, which includes functional [4] and stuck-at tests [5]. For Boolean test, the test cost and test time associated with it are the main challenges. The Boolean test relies on test vectors and automatic test equipment (ATE) to conduct the test. The time to generation test vectors is one major factor of testing cost, because most Boolean test problems have NP-complete time complexity, which means that in the worst case, the CPU time grows exponentially with the size of the IC [6][7][8]. Even if the generation of a large number of test vectors is possible, the time it takes to apply them on the ATE would be enormously expensive, since the state-of-the-art ATE cost up to several million dollars. The ATE test time assigned to each chip is very limited due to the high cost of ATE and the volume of chips that must be tested. Therefore the IC test time is another critical factor of testing cost.

In contrast to Boolean tests, parametric tests, as the name implies, measure certain parameters of the circuit under test (CUT). The CUT is considered have a soft fault when the measurement falls outside of its specification range. Power supply quiescent leakage current (I_{DDQ}) test, voltage operating range test and speed test are good examples of parametric tests. Although different approaches probe different parameters, all parametric tests have one thing in common, which is the failure of a parametric test does not necessarily declare the chip faulty. The chip may still be able to perform its intended

function [9]. As an example a chip may function correctly even though it has above-normal leakage, so it consumes above-normal power or operates at below-normal clock frequency.

The cost of testing is not only confined to test vector generation and application. It also includes the cost of diagnosis, repair and scrap needed at higher levels of assembly due to poor test quality at lower levels. As indicated by Williams et al. [10], the cost to detect a defect at a higher level of assembly is 10 times as much as the cost to detect the same defect at a lower level. So it is imperative for testing techniques to detect a very high percentage of manufacturing defects.

1.2 Testing Terminologies

This subsection covers some of the common methods and terminologies concerning digital testing techniques. As we discussed, the primary purpose of testing is to screen out defects that occur in manufacturing, to ensure that only defect-free chips are packaged and shipped to customers. This requires the test methods to have the following properties: (1) the test speed must be fast enough to handle the large volume of chips during production; and (2) the test must have high defect coverage. In general, chips are subjected to two types of tests: *Functional tests* consist of input vectors and the corresponding responses. They check for proper operation of a verified design by testing the internal chip nodes. Functional tests cover a very high percentage of (logic and delay type) faults in logic circuits. *Parametric tests* checks for physical defects and ensure the product meet design specifications such as clock frequency, operating voltage range, and

maximum power dissipation.

There are many different approaches used in functional test algorithms. As shown in Fig. 2, McCluskey suggested the general division for testing algorithms into test pattern generation and output response analysis [11]. *Test pattern generation* refers to the work in generating an appropriate subset of all input combinations, such that a desired percentage of potential defects is activated and observed at the outputs. *Automatic test pattern generation* (ATPG) tools are based on various algorithms and their heuristics.

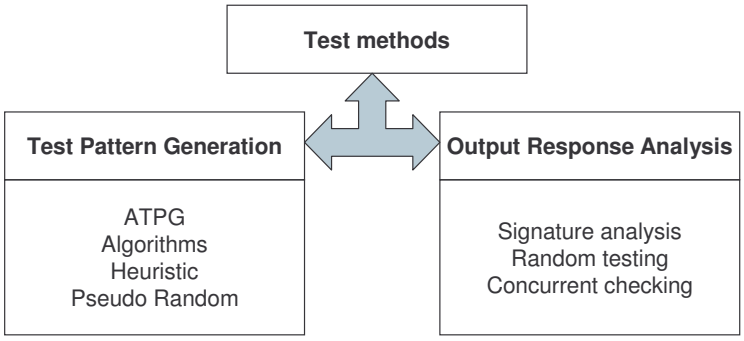

Fig. 2. Test method divisions.

Output response analysis encompasses methods which capture only the output stream and apply appropriate transformations, with the assumption that the circuit is stimulated by either an exhaustive or a random set of input combinations. Since the output stream is huge, data compaction is usually performed on the output stream prior to analysis.

Testing can also be divided into *on-line* and *off-line* methods:

- *On-line:* each output word from the circuit is tested during normal operation.

- *Off-line:* the circuit must suspend normal operation and enter a "test mode," at which time the appropriate test method is applied.

Usually off-line test can be executed either through external testing with ATE or through the use of *Built-In Self-Test* (BIST) structures. In contrast, on-line testing (also called *concurrent checking*) usually implies that the circuit contains some coding scheme which has been previously embedded in the circuit design.

Because of the enormous number of different defects that could be present in manufacturing, the resulting failures are grouped together based on their logical *fault* effect on the circuit functionality, and this leads to the construction of logical fault models as the basis for testing algorithms [12]. The most commonly used fault model is the *stuck-at fault,* in which a net is stuck at logic 0 or 1 (stuck-at-1 or stuck-at-0).

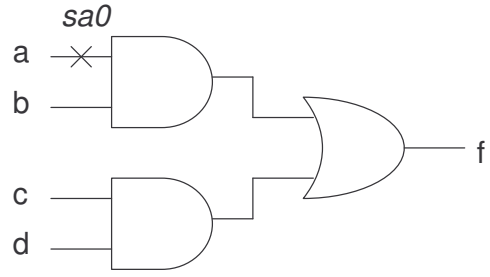

Fig. 3. Single stuck at fault example.

An example of stuck at fault is given in Fig. 3. Under fault free condition the logic function of the circuit is $f=ab+cd$. Assume there is a stuck at 0 (*sa0*) fault at input a, then the logic function would be transformed to $f=cd$. In order to catch this fault, a test

vector set must be able to activate the fault and the faulty result must be propagated to the primary output to be observed. In this example, a test vector set of {1,1,0,0} would detect the fault. Many of the physical defects can cause a stuck at 0 fault. For example, the input line of *a* is shorted to ground by a spot defect. The most common physical defects are:

- *Bridging Faults*: they occur when two or more lines are shorted together.
- *Stuck-Open Fault*: they occur when the signal net has an open circuit, usually due to an open via.

1.3 Motivation

An effective and efficient testing strategy should be evaluated by taking into consideration the capability of defect detection as well as the cost associated with it. Therefore ideal test methods should be able to catch as many defects as possible while keep the cost as low as possible. BIST is one such candidate because it has the potential to reduce the overall test cost. As transistor costs fall relative to ATE costs, and on-chip bandwidth and timing accuracy rises relative to off-chip bandwidth and timing accuracy, the cost of BIST falls relative to external testing with ATE. BIST can also be used to test chips at the package and board level, and in the field [13][14]. The primary costs of BIST are the chip area and design time associated with it, and the speed penalty of inserting BIST into on-chip logic paths. A good BIST approach should be able to detect a very high percentage of manufacturing defects and at the same time have modest area overhead and delay impact. It should be able to support fault diagnosis and in addition,

any necessary supporting ATE should be kept as simple and cheap as possible. This research is devoted to developing a BIST scheme for quiescent current testing, which can be widely used in current and future semiconductor technologies.

1.4 Objectives of the Research

The main goal of this research is to develop and evaluate a novel quiescent current sensing scheme for static Complementary Metal Oxide Silicon (CMOS) circuits. Integrated circuits using static CMOS technology are currently the dominant technology, because it offers reduced power consumption, design simplicity, and high circuit density. This research is therefore specifically targeted at testing digital CMOS ICs. We classify this research as a BIST approach because the technique utilizes Built-In Current Sensors (BICS) [15]. In addition to the standard advantages of BIST, the BICS approach allows the power grid to be virtually partitioned by multiple BICSs, so that the current measured by any one sensor remains small, even as total chip current rises in future technologies. Thus this research will extend I_{DDQ} test to future technologies while maintain the I_{DDQ} test efficiency and effectiveness.

1.5 Structure of the Dissertation

The dissertation gives a general testing overview in Section 2, which covers some basic concepts of test, including I_{DDQ} test. Section 3 covers the background on prior BICS approaches and requirements for a practical BICS design. Section 4 is devoted to evaluation of a magnetic field-effect transistor (MAGFET) as a sensing element in a

BICS. The proposed BICS design and analysis is described in Section 5. The principles of operation and the function of each module are described. This section also covers the evolution of the design over the three generations of test chips. Section 6 presents the experimental results of the three test chips, along with discussions of the measurement results. Section 7 concludes the dissertation and gives directions for future work.

2. BACKGROUND

2.1 Introduction

In this section we will provide a general overview of very large scale integrated circuit (VLSI) testing and then focus on I_{DDQ} test in detail, including its challenges in future technologies. The description will form the background for the later discussion on BICS test methodology. A short review of the IC manufacturing process flow is given first. Then failure modes and the underneath physical causes will be discussed and the models to represent these failures will be established. Classification of the various test methodologies and related key terminologies will be covered next. Then a detailed discussion of I_{DDQ} test.

2.2 IC Manufacturing Process Flow

Before discussing IC testing, we first briefly describe how an integrated circuit is fabricated. The IC chip manufacturing process consists of a series of steps of thin film deposition, photolithography, etching, implant/doping, and supporting processes. A greatly simplified description of a CMOS fabrication process flow is shown in Fig. 4. In step (a) the wafer is cleaned and laser scribed, then followed by silicon dioxide (SiO_2) growth. In step (b), photoresist is deposited and developed with openings for the n-well areas. Anisotropic plasma etch is applied at step (c) to open the n-well window on SiO_2. The n-well is then formed by implant of n-type dopants (phosphorus or arsenic or its compound). After the n-well is formed, the photoresist and SiO_2 are stripped and another

mask is applied to form the window for field oxide (FOX) at step (e). Usually before growing the field oxide, an implant step forms a channel stop layer beneath the field oxide, to prevent unwanted parasitic transistors. After field oxide growth, a thin gate oxide layer and a polysilicon layer are deposited. Then the cycle of masking, and etching is performed again to define the transistor gate in step (f). In step (g) the NMOS source and drain is formed by n-type implant while other areas are covered with photo resist to shield away the dopants. A similar procedure is repeated in step (h) to form the PMOS source and drain. Steps (a) to (h) are termed "front end" processing, since they form the transistors. The "back end" steps are then carried out to form interconnect between the transistors. In step (i), a SiO_2 dielectric layer is deposited and contact mask and etch is performed followed by the deposition of the contact layer. After that metal layer, via and inter-metal dielectric is applied alternately to conclude the remaining processing steps [16].

2.3 IC Manufacturing Defects

The manufacturing process is subject to contamination and variation. Given the small geometries and tight product tolerances, any tiny contamination or process fluctuation can cause product malfunction. Disturbances are usually classified into two categories, global and local [17]. Fluctuations of process or environment parameters that affect large areas of the wafer are termed *global disturbances*. For example, polysilicon under-etching on part of a wafer will increase transistor gate length and threshold voltage, reducing drive current and circuit speed. In contrast, particle contamination causes *local*

disturbances (or spot defects) that only affect small areas of the chip. Spot defects manifest themselves as shorts and opens in the circuit structure.

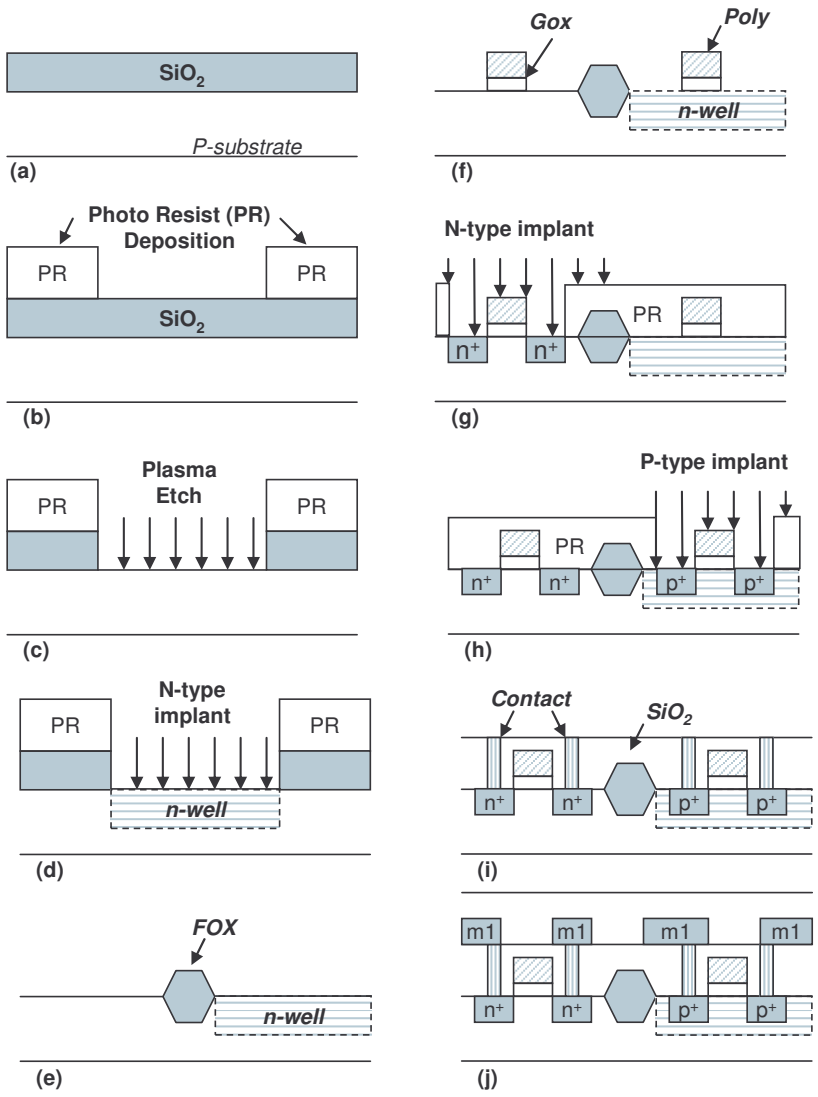

Fig. 4. Typical CMOS IC fabrication flow.

Fig. 5 depicts a typical spot defect causing metal shorts, in which three metal lines are

connected by the defect. The metal shorts caused by this defect are low resistance and change the circuit function.

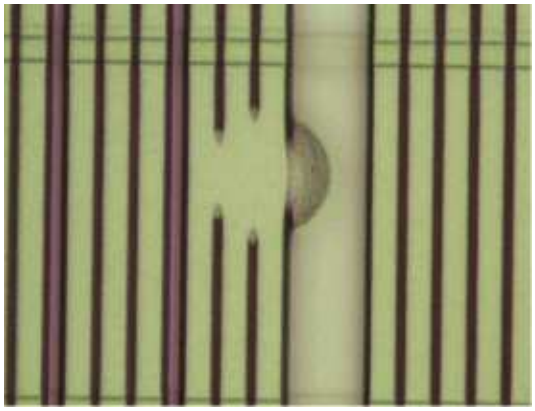

Fig. 5. A spot defect causing metal shorts.

Fig. 6 shows a resistive short caused by over-etching or photolithography distortion. The resistive nature of the defect may produce a delay increase, rather than functional failure. In other words, some defects may cause change in IC functional behavior while others change its performance. If the defect in Fig. 6 causes only a small delay increase, the circuit performance may not be affected, but the “almost” failure may reduce chip reliability. Defects combined with technology, layout and process may cause a wide variety of abnormality circuit behavior. There are many fault models constructed to emulate the behavior of defective ICs. The purpose of fault models is to simplify the test generation problem and to abstract away many process details.

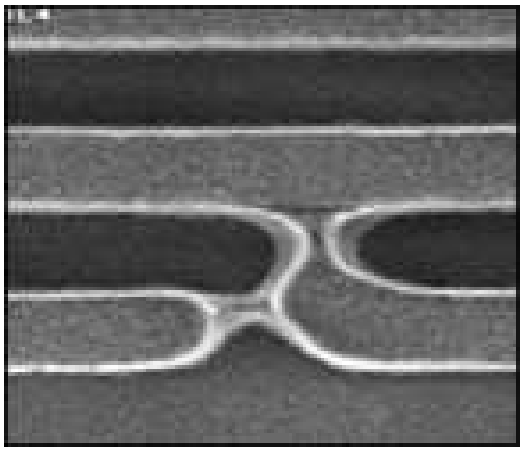

Fig. 6. Abnormal etch or deformation causing resistive open and short.

As the manufacturing process is disturbed by many types of defects, the manufacturing yield is lowered, and testing becomes of increased importance to maintain outgoing product quality. An estimate of the relationship between manufacturing yield, effectiveness of testing and outgoing product defect level is given in equation (2.1) [18]:

$$DL = \left(1 - Y^{(1-FC)}\right) \tag{2.1}$$

In (2.1), Y is the manufacturing yield, ranging from 1 (defect-free production) to 0 (all circuits are faulty). Typical yield values are low at the start of production and reach about 90% at maturity. Fault coverage (FC) is calculated as the percentage of faults detected over the total number of detectable faults. The value of FC ranges from 1 (all possible faults detected) to 0 (no faults detected). Our ultimate concern is the final defect level (DL). DL is defined as the probability of shipping a defective product after test and

is usually given in defects per million (DPM) or defective parts per million (DPPM). Competitive defect levels are in the range of 100-1000 DPM. It has been shown that tests with high fault coverage also have high defect coverage. Associating data to this equation gives interesting and practical results. Table I shows examples for some practical values of *Y* and *FC*. The main conclusion to be drawn is that for typical yield values, very high fault coverage must be achieved to obtain an acceptable defect level.

TABLE I. DEFECT LEVEL EXAMPLES.

Yield (Y)	Fault Coverage (FC)	Defect Level (DL)
0.1	0.9	200,000 DPM
0.9	0.99	1,000 DPM
0.9	0.9	10,000 DPM
0.5	0.99	7,000 DPM
0.5	0.999	700 DPM

Given the defect susceptibility of IC manufacturing, the fabrication of an IC chip includes a series of stringent tests to ensure the IC is defect-free and conforms to product specifications. In-line measurement data are collected throughout the wafer manufacturing process to ensure that critical process control parameters (e.g. gate oxide breakdown voltage) meet their specifications. At the end of the wafer processing, electrical test structures (usually located in the scribe lanes) are measured to provide process information and check for potential defects. An example test structure is the metal comb and serpentine to check for metal shorts and opens. After wafer fabrication,

each chip on the wafer will go through a thorough functional and parametric test. As discussed earlier, test vectors will be applied to the inputs of the IC and the outputs will be compared with predetermined values. If a discrepancy is detected, the chip is declared faulty and scraped. Parametric tests check a number of parameters to verify that they fall into the specification range. Only those chips passed all the above tests will be packaged. After packaging, functional test and parametric tests will be carried out again. Some defects do not cause chip failure, but can reduce reliability. These defects may cause chips to fail after a short operating life, termed infant mortality. Reduction of such failures can be achieved by subjecting chips to stress conditions before they are shipped. A burn-in (BI) test can be performed in which chips are subjected to high temperature and voltage for an extended time to force those potential defects to manifest themselves. The drawback of burn-in test is that it is quite expensive, so electrical tests that can detect reliability hazards are highly desirable. One test that has proven successful at screening out reliability hazards is I_{DDQ} test, which is described in more detail in the following section.

2.4 Principles of I_{DDQ} Testing

A unique characteristic of static CMOS integrated circuits is that there is no direct current flow when the circuit is in quiescent state, i.e. there is no transistor switching. Under ideal conditions, no current path exists from V_{DD} to GND so the current flow should be zero. In practice, the quiescent current (I_{DDQ}) is small since the only sources of current are transistor sub-threshold, gate oxide and junction leakage. An example of I_{DDQ}

test is shown in Fig. 7. A typical static CMOS inverter is shown with a PMOS and NMOS transistor connected in series. When the input V_{IN} is low (logic zero) the PMOS transistor is ON while the NMOS transistor is OFF. Thus the output V_{OUT} is high (logic one). The opposite conditions occur when V_{IN} is high (logic one). The right side of the figure shows the voltage and current waveforms. The input V_{IN} has a rising transition followed by a falling transition, which causes V_{OUT} to have a falling transition and then a rising transition. Spikes of current occur during the output transitions, when the load capacitance is being charged or discharged. The current flow is at its quiescent level the remainder of the time. Assume there is a spot defect in the gate oxide of the NMOS transistor that causes a resistive gate to source short. The circuit function remains unchanged, but when V_{IN} is high, current flows from V_{DD} through V_{IN} and the spot defect to GND. If a measurement of I_{DDQ} is taken at this moment, the elevated current will detect the defect. Some early work on the use of I_{DDQ} test and the associated fault models for defect screening can be found in [19][20]. In the example, I_{DDQ} is elevated only when the V_{IN} is high, because under this circumstance the defect is excited. We define a defect that only causes elevated current under some conditions as a *pattern-dependent* or *active* defect. In contrast, a *passive* defect [21] is the one that is pattern-independent. An example is a spot defect causing a short between V_{DD} and GND.

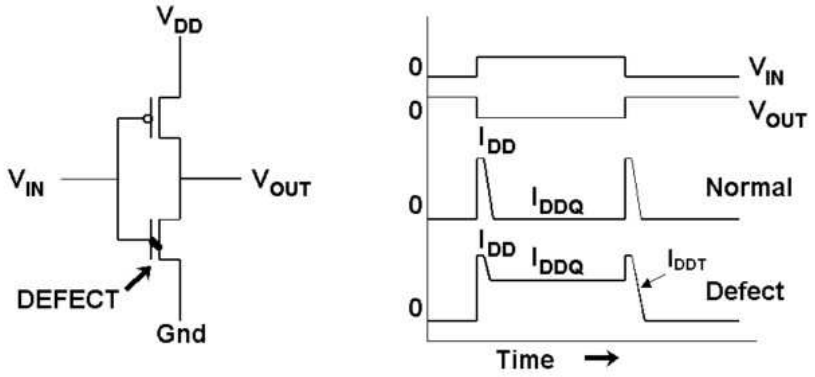

Fig. 7. CMOS inverter circuit and faulty/fault-free waveforms and current levels.

2.5 Advantages of I_{DDQ} Test

As discussed in the previous section, if the defective circuit I_{DDQ} is significantly higher than that of the defect-free circuit, we can readily group chips into defective and non-defective populations, as shown in Fig. 8. Under ideal conditions, both populations have a normal distribution (due to process variations) and are well separated from each other. Therefore a threshold I_{DDQ} can be specified in the gap to differentiate the two groups. Any chips with I_{DDQ} below the threshold are considered defect-free, while chips with their I_{DDQ} level higher than the threshold are classified at defective. Threshold setting is of particular importance in that an improper threshold may result in either too many good chips declared defective (overkill), which leads to lower yield and profit, or defective chips declared good (test escape), which increases defect levels.

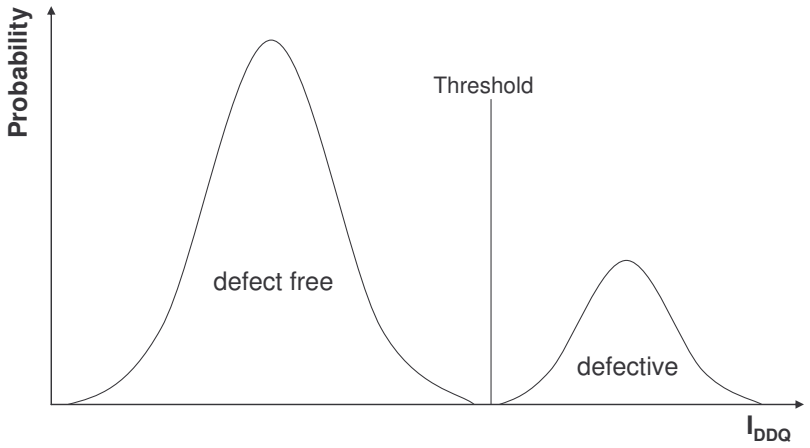

Fig. 8. Conceptual defect-free and defective chip I_{DDQ} distribution.

Once a proper I_{DDQ} threshold is determined, the I_{DDQ} test becomes an effective and efficient method for defect screening [22]. It has been shown that I_{DDQ} test achieves good coverage of physical defects that are not very well represented by classical fault models [23][24] and detects defects undetectable by conventional functional tests [25][26][27]. These defects include bridging defects, gate oxide shorts, floating gates and even some delay faults [28]. Unlike other test methodologies, power supply current is always observable, so I_{DDQ} test does not have the fault propagation requirements of stuck-at test. Because of these unique characteristics, especially the high fault coverage and cost effectiveness inherited from its simplicity, I_{DDQ} test has been widely utilized in industry [29][30][31].

I_{DDQ} test aids in localizing defects, particularly short circuits. If two nets have different voltages, but elevated I_{DDQ} is not observed, this means there is no short between these nets. This also makes it easier to debug the design and improve the process and yield. With an effective diagnosis method in hand, the product development

cost can be reduced and the overall time to market can be improved.

Some test solutions which combine I_{DDQ} with other test techniques have the potential to reduce or even eliminate burn-in (BI) test [32][33][34]. As we discussed earlier, burn-in test is used to screen out reliability hazards that cause infant mortality failure. A more accurate description of BI test is using the Arrhenius equation (2.2) and (2.3) to normalize failure rate predictions as a function of system operation temperature and/or voltage [35]. The elevated temperature and voltage in BI test accelerates the defect degradation [36], which also means that BI test is destructive [37]. One key challenge is that the fastest chips also have the highest power dissipation. During BI these chips can get so hot they go into thermal runaway and burn up, causing a large profit loss. Avoiding this overkill requires increasingly expensive temperature and voltage controls in the burn-in test fixture.

$$A_T = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)} \tag{2.2}$$

$$A_V = e^{\frac{E_a}{k}\left(\frac{1}{V_{use}} - \frac{1}{V_{stress}}\right)} \tag{2.3}$$

V and *T* are voltage and temperature respectively. Subscript ‘use’ represents the nominal condition while ‘stress’ refers to the stress condition. E_a is the defect activation energy, and *k* is Boltzmann’s constant. The model is built on the assumption that the performance parameter degradation is linear with respect to time. The probability of occurrence is an exponential function of temperature. As supply voltages scale down

with technology, ΔV ($V_{stress} - V_{use}$) keeps falling. Increased power consumption raises the operating temperature, so that ΔT ($T_{stress} - T_{use}$) also reduced. The combined reduction in ΔV and ΔT reduce the effectiveness of BI test or increase its cost. In contrast, I_{DDQ} test takes much less time and has lower cost. The non-destructive nature of I_{DDQ} test also avoids the overkill of BI test.

The advantages of I_{DDQ} test can be summarized as follows: simplicity; cost effectiveness; high fault coverage; capability of detect faults that escape other test methods; defect diagnosis and burn-in test alternative.

2.6 I_{DDQ} Test Challenges

As discussed above, the effectiveness of I_{DDQ} relies on the proper setting of the threshold value. A chip with I_{DDQ} higher than the threshold for some test vector is considered defective. The common practice for estimating the maximum defect-free I_{DDQ} is through model-based circuit simulations [38][39][40][41] or analytical methods [42]. The threshold value can also be determined by simulation [43][44][45] or empirical methods [46] using production data. The validity of this single I_{DDQ} threshold is based on the assumption that there is no ambiguity between the I_{DDQ} level of defect-free chips and defective chips. However, as technology advanced to the deep submicron era, the ambiguity of I_{DDQ} of defect-free chips and defective chips emerged. Reduced transistor threshold voltage, increased doping concentration levels, and more pronounced short channel effect [47] cause increased mean and variance in defect-free I_{DDQ} values, posing a great challenge for I_{DDQ} test.

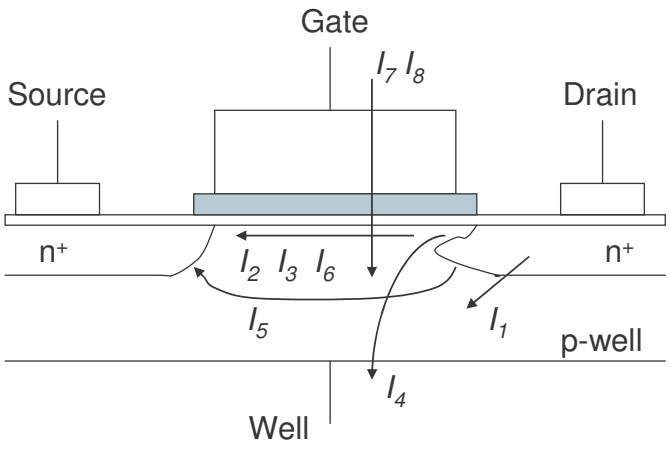

Fig. 9. Summary of leakage current mechanisms of deep submicron.

As shown in Fig. 9, the direct impact on the effectiveness of I_{DDQ} is the elevated off-state leakage current (I_{OFF}), which consists of the following components [48]:

- *pn* junction reverse bias current and gated diode leakage (I_1) which arises from two main components: minority carrier diffusion/drift near the edge of the depletion region and electron-hole pair generation in the depletion region of the reverse bias junction.
- Weak inversion or sub-threshold conduction current (I_2) between source and drain in a MOS transistor occurs when the gate voltage is below the threshold voltage V_{TH}.
- Drain-Induced Barrier Lowering (DIBL) (I_3) occurs when the depletion region of the drain interacts with the source near the channel surface to lower the source potential barrier. The source then injects carriers into the channel

surface without the gate playing a role. DIBL is enhanced at higher drain voltage and shorter gate length L_{eff}.

- Gate-Induced Drain Leakage (GIDL) (I_4) arises in the high electric field under the gate/drain overlap region causing deep depletion and effectively making the depletion width of drain to well *pn* junction thinner.
- Punchthrough (I_5) occurs when the drain and source depletion regions approach each other and electrically "touch" deep in the channel. It is a space-charge condition that allows channel current to exist deep in the subgate region causing the gate to lose control of the subgate channel region.
- Narrow width effect (I_6): Transistor V_{TH} in the nontrench isolated technologies increases for geometric gate widths on the order of ≤ 0.5 μm. And an opposite and more complex effect is seen for trench isolated technologies that show decrease in V_{TH} for effective channel widths on the order of ≤ 0.5 μm.
- Gate oxide tunneling (I_7) includes direct tunneling through the gate or Fowler-Nordheim tunneling through the oxide bands.
- Hot carrier injection (I_8): Short channel transistors are more susceptible to injection of hot carriers (holes and electrons) into the oxide. These charges are a reliability risk and are measurable as gate and substrate currents. It increases in amplitude as L_{eff} is reduced unless V_{DD} is scaled accordingly.

The dominating leakage component includes DIBL and weak inversion. As transistor geometries get smaller and smaller, the supply voltage and the threshold voltage (V_{TH})

keep dropping as well to limit electric fields. The sub-threshold leakage current significantly increases with reduced V_{TH}, since sub-threshold leakage is exponential in V_{TH} [49]. The combination of these factors is that I_{OFF} is rising rapidly with each technology generation. This makes it harder to differentiate good chips from bad chips, due to the two groups of chips overlapping with each other, as shown in Fig. 10 [50].

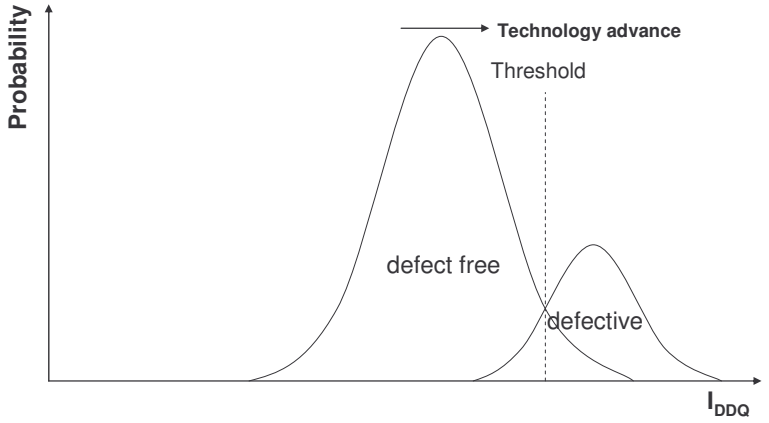

Fig. 10. Overlapping defect-free and defective I_{DDQ} values in deep submicron.

Another issue is the increasing variation of defect-free I_{DDQ} due to the variation in effective channel length and threshold voltage. This I_{DDQ} variation can be as high as an order of magnitude [45]. Fig. 11 illustrates the spatial variation of I_{DDQ} across a typical production wafer. This huge variation coupled with the high background leakage makes it difficult to set a threshold to distinguish defective chips from defect-free chips [50]. As shown in Table II, the International Technology Roadmap for Semiconductors (ITRS) projections for I_{DDQ} of high-performance microprocessor circuits indicate I_{DDQ} will keep

rising rapidly [47][50]. There has been much prior work devoted to the threshold setting problem, mainly focused on two directions. The first is to reduce the leakage current while the second is to reduce the effective signal variation. Substrate back-biasing [51], chip cooling for low temperature measurement and low supply voltage [52][53], dual threshold voltage technique [54], reduction of process variation [55] and internal or external chip supply grid partitioning have been proposed to help counter the problem of leakage and facilitate the I_{DDQ} threshold setting. Techniques targeting reduced signal variation include delta I_{DDQ} [56][57][58], current ratio (CR) [59][60][61], neighborhood current ratio (NCR) [62] and current signature [63][64][65]. These approaches have extended I_{DDQ} test to newer technologies, but alone are insufficient for the future.

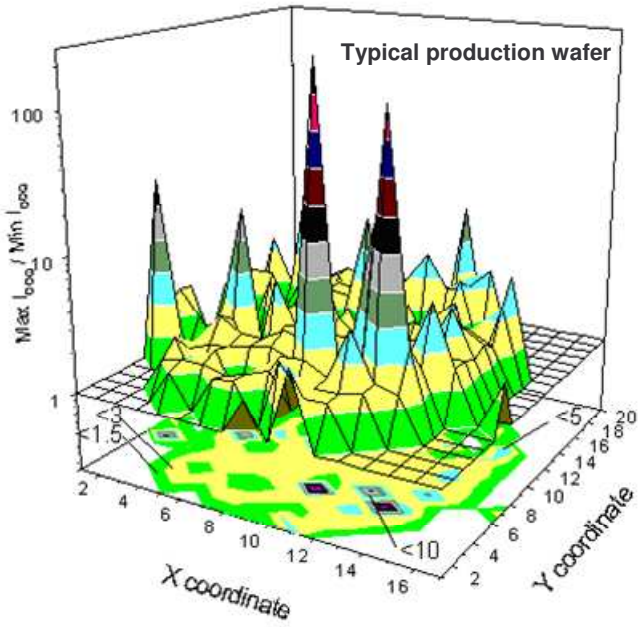

Fig. 11. Variation of Max/Min I_{DDQ} across a typical production wafer.

TABLE II. ITRS PROJECTIONS FOR I_{DDQ} OF HIGH-PERFORMANCE ICS.

Year	Maximum I_{DDQ}
2003	70-150 mA
2005	150- 400 mA
2008	400 mA-1.6 A
2011	1.6 - 8 A
2014	8-20 A

2.7 I_{DDQ} Test for Future Technologies

In spite of the difficulties I_{DDQ} test is facing, its unparalleled benefits necessitate that it continue to be used in future technologies. Researchers are exploiting every possible solution to extend this simple yet effective test method. As the chip size and complexity advances with technologies, functional test still needs to partner with $I_{DDQ,}$ as well as other test methods, to form a test suite to achieve the required fault coverage. With critical path delay test to check timing issues, stuck-at test to achieve fault coverage, and burn-in test to ensure reliability, the I_{DDQ} test will continue to play an important role in catching process-related defects such as bridging faults, gate shorts or delay faults which often escape other test methods. This unique characteristic of I_{DDQ} test becomes more useful as feature sizes shrink and chips become more vulnerable to smaller defects. Many benign defects of today will become fatal defects in future technologies. For an inherently low leakage process such as silicon-on-insulator (SOI) [66][67], I_{DDQ} test naturally becomes part of the test suite.

In the next section, we will focus on internal partitioning of the power supply grid using built-in current sensors (BICS). We will review prior BICS work and develop the requirements for our BICS. We will later examine and evaluate our BICS design according to these requirements.

3. REVIEW OF BUILT-IN CURRENT SENSOR METHODS

3.1 Introduction

I_{DDQ} test can be performed with external (off-chip) current monitors, or with internal (on-chip) monitors. External testing measures power supply current through the power pins of the integrated circuit, such as with a precision measuring unit of an ATE, or a load board sensor on the test head. Internal testing measures power supply current using a built-in current sensor (BICS) inserted in series with the power or ground grid of the CUT. External testing faces rapidly rising leakage currents, and transient currents. The larger transient currents require more decoupling capacitance, reducing I_{DDQ} test speeds. Internal testing has the advantage that multiple BICSs can be placed within a chip, reducing the background leakage seen by each sensor, permitting the extension of I_{DDQ} test to future technologies. Prior work on BICSs will be reviewed in the following sections.

3.2 BICS Challenges

At the present time, I_{DDQ} is measured off-chip. Although many BICS designs have been proposed, they have not been applied in practice. The major problems of these BICSs can be summarized as follows:

1. *Circuit under Test (CUT) performance degradation*: A voltage drop across the sampling device will occur when sampling the I_{DDQ} directly, which causes CUT performance degradation, typically 10-30% [68].

2. *Pass/fail and I_{DDQ} level*: Most BICSs were designed to compare with a reference current/voltage and make a pass/fail decision. However even with BICSs, the increased variance in I_{DDQ} makes pass/fail decision making obsolete. A BICS that can quantitatively measure the I_{DDQ} level would be more useful in that the results can be used in I_{DDX} algorithms.
3. *Fabrication process compatibility*: Some BICS designs need to use analog components such as resistors and capacitors that are not available in a digital CMOS process. Furthermore, some designs require accurate device matching and thus impose a great fabrication difficulty.
4. *External reference*: Most approaches require an external current or voltage reference. This increases the hardware requirement of the ATE.
5. *Adaptability*: Once implemented, most designs are difficult to adjust for different current resolution requirements.
6. *Area overhead*: Many BICS designs take too much chip area (especially to achieve a low delay penalty), so that they are impractical for use in industry.

3.3 Prior BICS Designs

A BICS consist of two primary parts: a sensing device and signal processing unit, such as an amplifier or comparator. The sensing strategy often determines the selection of the amplifier. The amplifier can be either voltage mode or current mode, depending on the signal produced by the sensing device.

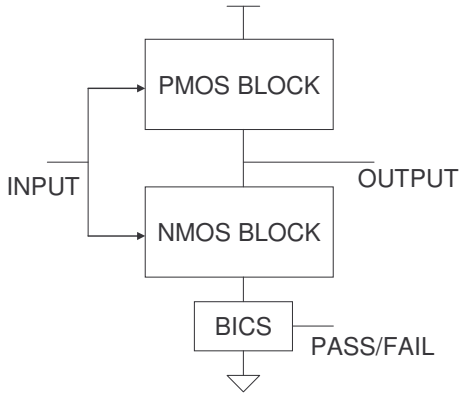

Fig. 12. Block diagram of a typical I_{DDQ} BICS.

Sensing devices include bipolar junction transistor (BJT) [69], *pn* junction diode [70][71][72][73][74][75], resistance of metal line [76], current mirror [77] or the load device of the voltage regulator [78][79]. Since sensing devices cannot be removed or turned off after testing, they will be present during normal circuit operation. Fig. 12 shows a general location of the BICS for I_{DDQ} testing, where the BICS is inserted between the CUT and GND. The BICS embedded in the circuit checks whether the quiescent current is below or above a threshold level, or produces a value. The voltage drop through the BICS sensing device indicates the existence of defects. The voltage drop might reduce the noise margin or speed of the CUT. For effective use, the BICS must minimize these effects. There have been several attempts to solve this problem: using dual (or even multiple) power supplies [80][81], bypass device [82] or bypass pad [83], Hall sensor [84][85], MAGFET sensor [86] or associating BICS with the voltage regulator.

We will review several typical BICS designs to get a better understanding of the

different approaches that have been proposed to date. We will first review a BICS using a BJT sensing device [73], as shown in Fig. 13. The incentive for using a BJT as a sensing device is that it can handle a large range of current, and the voltage drop is small under defect-free conditions, but large enough for a voltage comparator under defective conditions.

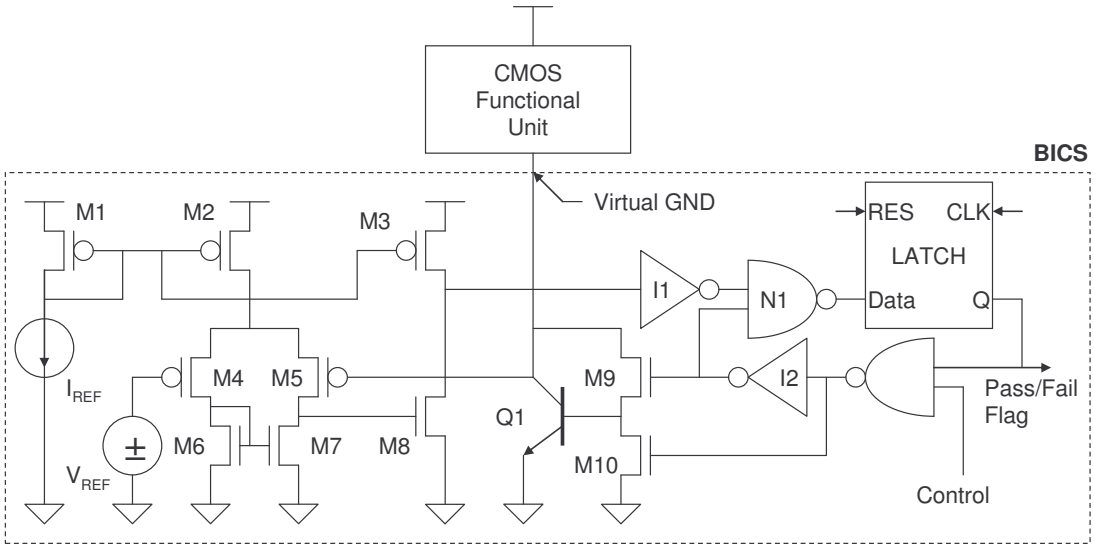

Fig. 13. BICS using BJT as sensing device.

The proposed BICS consists of the a voltage drop BJT device *Q1*, a comparator (*M1-M7*), a two-stage amplifier (*M3, M8, I1)*, a bistable, edge-sensitive latch generating a flag signal (*F*), a circuit breaker (*M9, M10, I2*), a reference voltage source (V_{ref}) and a current source (I_{ref}). One can see that this circuit sets the pass/fail flag to ONE and disconnects the CMOS functional unit from ground when V_{CE} of *Q1* is higher than V_{ref}. The essential elements of this BICS implementation are the low offset comparator and

an adequate V_{ref} voltage source. The exponential characteristic of the BJT voltage drop device is critical in minimizing the performance degradation of the CUT. While the design benefits from the unique BJT voltage and current handling characteristics, it also brings the difficulty of manufacturing process compatibility issue. The application of the BICS means a migration from a digital logic process to a bipolar process, which is much more complicated and expensive. Further, the diode drop across the BJT does not scale with technology, and so becomes an increasing fraction of total supply voltage in future technologies.

Fig. 14 depicts a BICS design using a diode to bypass the transient current and a transistor *T1* to function as the I_{DDQ} sensing device [74]. As with the BJT design, the diode has a 0.65V volt drop, which causes approximately a 14% CUT performance degradation, and does not scale with technology. The principle of the BICS design is simple, the I_{DDQ} will be converted to a voltage signal via *T1*, the signal is then compared with V_{ref} and resolved into a pass/fail decision through the flip-flop and a inverter.

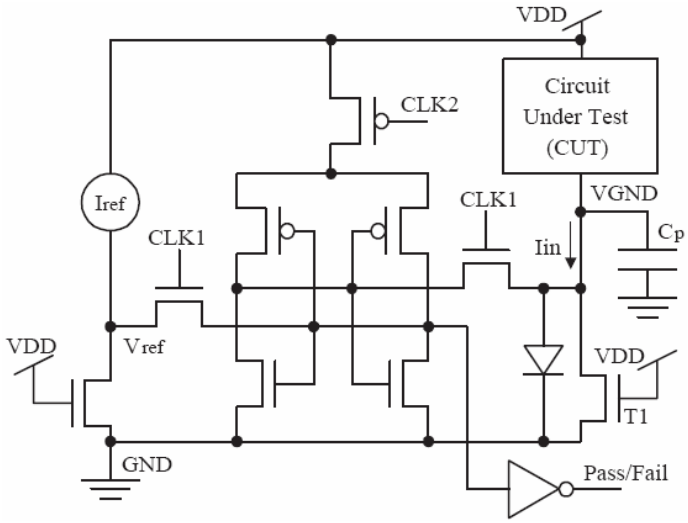

Fig. 14. BICS using diode as bypassing device.

In order to measure the I_{DDQ} correctly, parasitic capacitor *Cp* must be allowed to discharge completely. The settling time is determined by the time constant of $Cp \cdot R$, where *R* is the *T1* on resistance. The time constant indicates there is trade-off between test speed and resolution. To increase test speed, *R* needs to be reduced, but this also reduces resolution. Or we can increase test speed by reducing *Cp*, which will result in an increased CUT delay penalty, or require more CUT partitions and more BICS area. The optimum size of *T1* is determined by the threshold voltage value (V_{ref}). This type of design tests only one CUT at a time. The reference current is still needed and is fed to the opposite side of the CUT currently being tested. A modification of the design makes a small change and uses a differential scheme, in which the I_{ref} is replaced by another CUT so the circuit is symmetric with two CUT connected to the two current input terminals of the BICS. The benefit of this modification is that if both CUT has similar

Cp associated with them, then the BICS can run faster since the charging up effect is canceled.

A typical current mirror based BICS is shown in Fig. 15 [81]. The proposed BICS consists of a current mirror, a constant current source for reference and an inverter. NMOS transistor Q_0 is operated to switch either isolating or connecting the BICS, which enable the BICS to work in two modes: the normal mode or the test mode. In normal mode (TCLK is one) CUT current flows through Q_0. The speed degradation and area depend on the size of Q_0. The EXT pin can be used as an external connection to avoid the bypass transistor after testing is complete. In test mode, the BICS compares the quiescent current consumed by the CUT with the reference current. When the quiescent state current is greater than the reference current, the output signal PASS/FAIL is set to 1, which indicates the existence of a defect. Otherwise the signal is set to 0.

In the quiescent state Q_0 is turned off and the current mirror pair replicates the defective current I_{DEF}. The reference current source, I_{REF}, has a constant current value. The PMOS current mirror pairs, Q_3 and Q_4, replicates this reference current. Drains of the PMOS replicating transistor Q_4 and the NMOS replicating transistor Q_2 are connected to the input of the inverter to generate the PASS/FAIL signal, based on a comparison of I_{REF} to I_{DEF}.

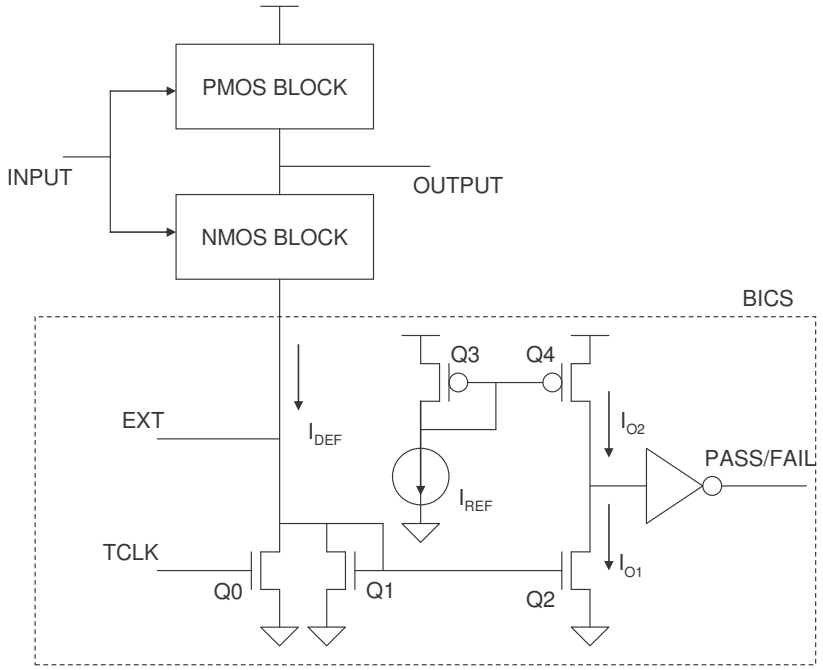

Fig. 15. Current mirror based BICS.

The operational amplifier (OP-AMP) is also used in some BICS designs. One of the OP-AMP BICS designs is depicted in Fig. 16 [82]. The BICS is integrated with a voltage regulator to provide on-chip low voltage source for low voltage circuits and to provide power bus stability. Since the BICS is not in series with the CUT after the V_{DD} power supply, the performance degradation can be neglected.

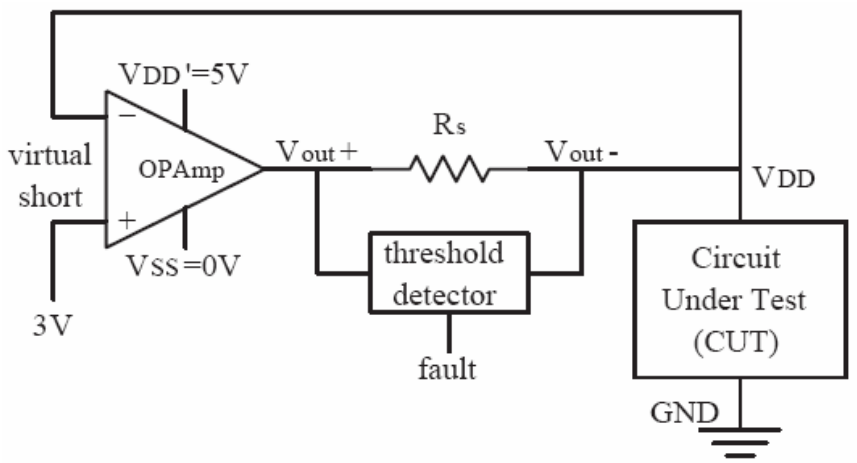

Fig. 16. The OPA based BICS scheme.

Because of the virtual short property of an OP-AMP, the voltage at the noninverting node V^+ is equal to the voltage of the inverting node V^- and no current flow into or out of either V^+ or V^- (high input impedance property of OP-AMP). The V^+ of the OP-AMP is connected to the original power supply and the V^- is connected to the V_{DD} node of the CUT. The OP-AMP is powered by an additional pair of power supplies V_{DD}' and V_{SS}, where V_{DD}' must be higher than V_{DD} and V_{SS} is common-grounded with other BICS modules. This scheme is typically used for relatively low power CUTs, due to the limited current sourcing abilities of practical power amplifiers. Between the output node of the OP-AMP and the V_{DD} node, there is a series resistor R_S. The two terminals of V_{OUT}^+ and V_{OUT}^- of R_S are connected with the inputs of a threshold detector. The detail of the threshold detector is not shown here. It consists of a differential amplifier, a sample and hold circuit and an output buffer. The R_S converts the I_{DDQ} to a voltage drop of V_{OUT}. This voltage drop is then used by the threshold detector to make a decision of

whether the CUT is fault free or not. When the reference current is set at 140 μA, the threshold voltage used by the threshold detector is only 50 mV. If a lower reference current level is used, an extremely sensitive power amplifier is needed, making this approach difficult to implement. A larger R_S can be used to enhance the sensitivity of the BICS, but the OP-AMP will only work properly when R_S is small. A variation of this design utilizes a long existing power wire in the CUT to function as the R_S. However, this type of sensing device produces a very weak signal, and thus requires a very sensitive amplifier.

3.4 The BICS Design Strategy of This Research

By reviewing the prior work on BICSs and analyzing the BICS challenges and benefits, we have conceived a practical BICS design. In this section we will discuss the design strategy. The key drawback of most prior BICS approaches is CUT performance degradation. The performance degradation is usually caused by the impedance of the sensing device. The requirements for the sensing device are that a small voltage drop can handle a larger range of current flow during transient operation and at the same time a small current increase in the quiescent state caused by defects should generate an appreciable voltage/current that can be measured and read out. A bypass device or bypass pad solves the problem, but at a price of extra area or extra pins, both of which are unacceptable. The proposed BICS uses a small section of the existing V_{DD} line (a small metal strip) as the sensing device, so it introduces no additional series impedance and so no performance degradation. The challenge is that the small defect current

through the low-resistance metal line will produce only a small voltage signal. For example, 10 squares of 100 mΩ metal will produce a 1 μV signal for a 10 μA defect current. The amplifier stage (stochastic sensor) must have correspondingly high gain.

BICS implemented by sensing the power line has the potential to speed up I_{DDQ} test since a large decoupling capacitor is not needed to bypass the sensing element. Fast I_{DDQ} test is desirable for use in a traditional BIST environment or for concurrent fault detection [75] [87].

Even with BICS, leakage currents are rising so rapidly that it is likely that I_{DDX} techniques must be used to achieve adequate resolution. This requires that the BICS provide the current level, rather than just a pass/fail value. When inserted into a power mesh, current flow on a given branch could change directions based on process variations, so the sensor should also supply current direction. This is also very useful in localizing a defect. BICS area overhead can also be reduced by using multiplexers [88] or ratioed logic [89].

The partition size (amount of circuitry sensed by one BICS) is variable depending on the technology and I_{DDQ} resolution. In addition, chip area overhead should also be taken into account. As technology advances, the leakage current rises drastically, causing background current to become the most dominant factor in determine the partition size. The partition size should be determined so that the background current of each partition does not overlap with faulty I_{DDQ} [90]. As shown in Table III, projections have been made on the requirements for partitioning the supply network to maintain a 10 μA background current within each partition [94]. The maximum allowable BICS area is for

a 1% area overhead. Since the proposed BICS design is larger than the allowable area for most technologies, the allowable background current must be relaxed to 100-1000 μA, and resolution enhancement techniques such as current ratios or delta I_{DDQ} can be used to achieve the desired defect detection. As the proposed BICS is capable of measure the current level, then a simple on-chip controller can be implemented to realize some of the enhancement algorithms, simplifying the ATE interface.

TABLE III. REQUIREMENTS ON SUPPLY NETWORK PARTITIONING.

Year	2002	2005	2008	2011	2014
Technology	130 nm	100 nm	100 nm	50 nm	35 nm
I_{DDQ}/transistor (nA) high perf	2.55	3.9	5.4	7.68	10.56
I_{DDQ}/transistor (pA) low power	2.55	3.9	5.4	7.68	10.56
Partition size (transistors) high perf	15686	10256	7408	5208	1894
Partition size (transistors) cost perf	15686	10256	7408	5208	1894
Partition size (transistors) low power	15686	10256	7408	5208	1894
Partition/chip MPU high perf	21.1K	86K	337K	1.35M	10.5M
Partition/chip MPU cost perf	4526	18.5K	72.8K	292K	2.3M
Partition/chip MPU low power	5	19	73	292	2275
Max BICS Area (transistors) high perf	157	103	74	52	19
Max BICS Area (transistors) cost perf	157	103	74	52	19
Max BICS Area (transistors) low power	157K	103K	74K	52K	19K

Based on the above analysis, in order to keep up with technology and maintain the efficiency and effectiveness I_{DDQ} test, a built-in current sensor should satisfy the following requirements:

- If the random intra-die I_{DDQ} variation is up to 20% and the transistor conduction current is up to 50 μA (based on ITRS for 35 nm technology), then

the background I_{DDQ} level should be kept to no more than 10 μA in order for the maximum random variation to equal the target defect current.

- The BICS should measure I_{DDQ} level and direction. I_{DDQ} spatial variations across the wafer calls for measurement of I_{DDQ} value instead of just pass/fail. The capability of measuring I_{DDQ} value will assist the spatial analysis. Measuring current direction is required if the BICS will be inserted into branches of a power mesh.
- The test should achieve a speed of 1 ms/vector in order to be competitive with the best current I_{DDQ} test techniques.
- There should be no CUT performance loss. The BICS should not introduce any significant series impedance into the power grid. In addition, the BICS should be able to completely power off when testing is completed.
- There should be no special technology requirements, so the BICS can be fabricated in a standard digital logic manufacturing process.
- I_{DDQ} test used to be a pass/fail test with a single threshold. This method can also be expanded to execute I_{DDX} based simple algorithms with an on-chip controller, in which delta I_{DDQ}, current ratios, min/max I_{DDQ}, current signature can be calculated.
- Our objective of the chip area overhead is that the total area taken by the BICS system should be less than one percent of the total chip area. As far as how the test is to be conducted, the BICS is designed to be usable at both wafer level and package level test.

So to summarize, our approach of BICS is focused on the abilities of high I_{DDQ} resolution with current level measurement capability, defect identification, localization and diagnosis, and at the meantime causing no CUT performance degradation.

4. MAGFET SENSOR SENSITIVITY

4.1 Introduction

The first stage of the proposed I_{DDQ} sensor system is the sensing element, which is imperative to the success of the I_{DDQ} sensor design. Since the sensing element is usually the only component that directly interacts with the CUT, care must be taken to ensure no (or very little) interference is introduced to avoid CUT performance loss. At the same time, the sensing element should be able to acquire enough signal for proper functioning of the next stage of the I_{DDQ} sensor system. We have evaluated two possible sensing elements: one is indirect sensing of supply current with a magnetic field-effect transistor (MAGFET) sensor, while the other is direct sensing via the voltage drop along a small section of a power line. We ultimately decided to go with the latter approach after analyzing both ideas. In this section we present a detailed study of the MAGFET sensitivity for on-chip non-uniform magnetic field and give the test chip experimental results. The feasibility of a MAGFET-based sensing element is also discussed.

4.2 MAGFET Sensor

According to basic electromagnetic theory, a change in the current density of a conducting wire will cause a change of the magnetic field in the surrounding region. By probing the magnetic field around the power line, we can determine the current flow in the power line. The indirect nature of the measurement makes the MAGFET an appealing choice for the sensing element of I_{DDQ} sensor system.

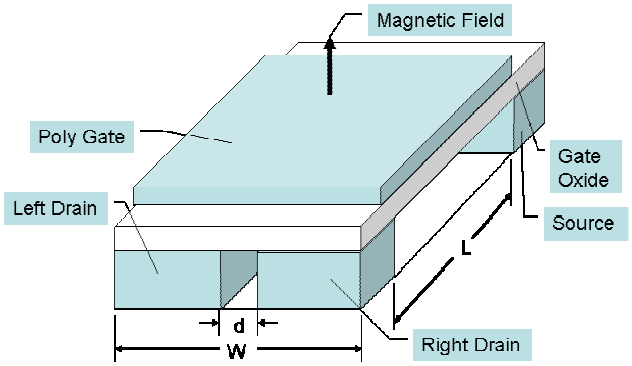

Fig. 17. Structure of a dual-drain magnetic field-effect sensor (MAGFET).

A MAGFET is a MOSFET with two drains. MAGFET operation is based on the fact that a perpendicular magnetic field will cause an imbalance in current flow through the two drains (as shown in Fig. 17) and therefore convert the magnetic field into a corresponding differential current. The underlying mechanism of the MAGFET is the Hall effect, which is the result of transverse electromotive force in a semiconductor device carrying an electrical current while it is exposed to a perpendicular magnetic field. This force causes an electrical field with a transverse orientation with respect to the device or a current direction. As shown in Fig. 18, the charged carriers are deflected by the Lorentz Force (F) in the direction perpendicular to the plane of v and B, depending on the direction of magnetic field B, the current direction and the carrier polarity (holes or electrons). The Lorentz Force is given by equation (3.1):

$$F = q\vec{v} \times \vec{B} \tag{3.1}$$

In (3.1) q is the charge of the carrier and v is the carrier velocity. So the Lorentz force is proportional to carrier charge, carrier velocity and the magnetic field strength. Due to

the Lorentz force, charge accumulates on the boundaries of the bulk silicon and therefore an electric field (Hall field E_H) is established. The Hall field and the Lorentz force together achieve equilibrium when the current generated by the Hall field equals the current generated by the Lorentz deflection. The relation can be represented by equation (3.2):

$$q\vec{v} \times \vec{B} + q\vec{E}_H = 0 \tag{3.2}$$

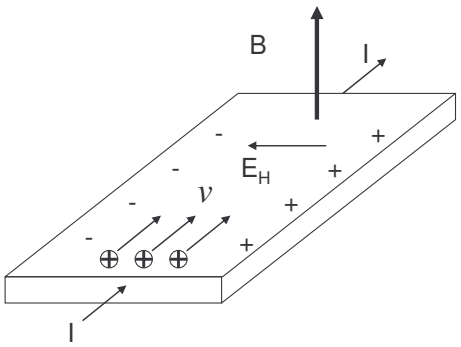

Fig. 18. The Hall effect on bulk silicon.

MAGFETs are able to sensing small magnetic fields [91][92] while been fully compatible with a CMOS process. These characteristics make the MAGFET a promising candidate for magnetic sensing applications. Extensive research on MAGFET sensitivity has been conducted, either in the form of numerical analysis or experimental study [91] [93][94][95][96]. Geometrical factors and second order geometrical factors were found to play a key role in affecting MAGFET sensitivity. The sensitivity relationship with respect to MAGFET operating point was also investigated. However, to our knowledge,

prior work assumed the magnetic field was a uniform external field perpendicular to the silicon surface. In contrast, the magnetic field produced by a power line on a chip is non-uniform and not perpendicular to the surface. In order to consider application of a MAGFET to detect the magnetic field around a power line, MAGFET sensitivity in such a configuration was studied. Various aspect ratio and geometric parameters of the MAGFET have been considered, and different bias conditions (both linear and saturation regions) have been taken into account.

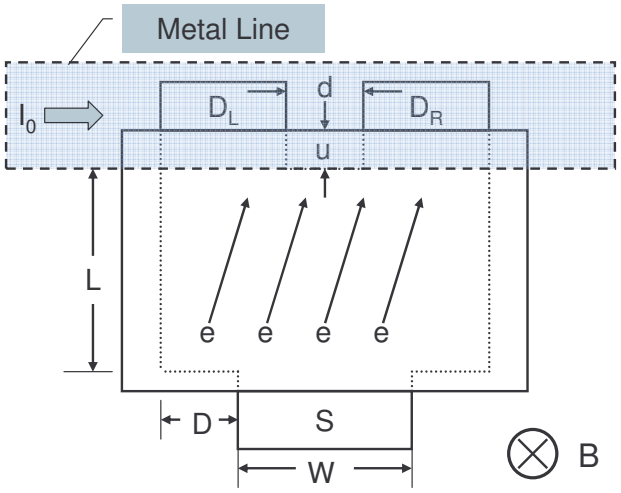

Fig. 19. Top view of MAGFET sensor and metal line above.

4.3 Modeling of Non-Uniform Magnetic Field

A model of the non-uniform magnetic field generated by the power supply line was developed. The configuration of the MAGFET and power supply line is shown in Fig. 19 (top view) and Fig. 20 (side view). The edge of the power supply line is placed

directly above the end of the common channel region, in order to maximize the magnetic field strength at the location of maximum carrier velocity, maximizing the Lorentz force and the current difference. The current flow in the metal line is left-to-right, so the magnetic field is going into the silicon surface at the MAGFET. The geometry parameters of the MAGFET include channel length *L*, channel width *W*, drain distance *d* and notch depth *u*. The V_{DD} metal line that generates the magnetic field to be measured is located vertical distance *h* above the MAGFET channel. The metal line has width *a* and thickness *b*. In this work we assume a uniform dielectric between the metal line and the MAGFET.

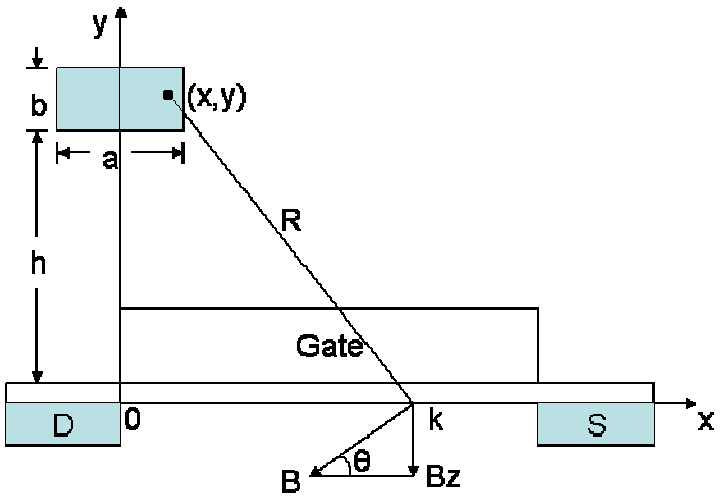

Fig. 20. Side view of the MAGFET sensor and metal line above.

Since the dimensions of the metal line are comparable to the MAGFET, the metal line cannot be simplified as a long thin wire for calculation of the magnetic field. However,

the metal line can be considered as a bundle of 'thin wires' whose magnetic fields are superimposed. The field is uniform along the direction of the wires, so only the field variation from MAGFET source to drain (location *k* in Fig. 20) must be considered. We approximate the MAGFET channel as thin enough that only the field at the silicon surface need be considered. Because of the low frequency nature of the current, the skin effect can be neglected, so the current density in the wire can be assumed to be uniform and therefore the current density for each thin wire is:

$$I = \frac{I_0}{ab} dxdy \quad . \tag{3.3}$$

In (3.3) I_0 is the total current of the metal line. So using the properties of the magnetic field of long thin wire, the magnetic field at channel location *k* is:

$$B = \frac{\mu_0 I}{2\pi R} = \frac{\mu_0 I_0}{2\pi abR} dxdy \quad . \tag{3.4}$$

As discussed above, we are only interested in B_z, the *z* axial component of the field, which is:

$$B_z(k) = B \cdot \sin\theta = \frac{\mu_0 I_0}{2\pi abR} dxdy \cdot \sin\theta \tag{3.5}$$

Since $R = \sqrt{y^2 + (k-x)^2}$ and

$$\sin\theta = \frac{k-x}{\sqrt{y^2 + (k-x)^2}}$$

then by integration of the contribution of each thin wire, the superposition of the magnetic field *z*-axial component at location *k* is:

$$B_z(k) = -\frac{\mu_0 I_0}{2\pi ab}\int_h^{b+h}\int_{-\frac{a}{2}}^{\frac{a}{2}}\frac{(k-x)}{y^2+(k-x)^2}dxdy \tag{3.6}$$

Through numerical calculation using MATLAB and actual process parameters, the magnetic field strength at different channel locations is shown in Fig. 21. A metal 2 power line with different current densities was used for the calculation. It was found that the magnetic field gradually increases from source to drain, then rises sharply to its peak level a few microns away from the wire edge, and then drops steeply until reaching zero at the wire edge. The results show that the power line edge should not be located directly above the end of the MAGFET notch, but should be located farther back, in order to maximize the field at the notch. This is in contrast to prior published approaches [97].

As expected, the magnetic field strength at each point in the channel is proportional to the power line current flow. As shown in Fig. 21(a) the magnetic field generated by a 1 A current is 2 times and 10 times that of a 500 mA and 100 mA current, respectively. The relationship between the magnetic field intensity and the metal line width is illustrated in Fig. 21(b). It was found the magnetic field profile spreads out as the metal width increase.

Simulations of the magnetic field generated by different metal layers carrying the same current were also performed. As illustrated in Fig. 22, the magnetic field decreases and the peak moves away from the origin (farther into the channel), for higher metal layers. The curves for M2 (metal 2), M3 (metal 3), M4 (metal 4) assume equal metal layer thicknesses. In fact M4 is thicker than the other metal layers. The curve M4T uses the actual thickness, showing that the magnetic field is lower due to lower current

density. The results clearly show that the power line should be on the lowest metal layer and have the smallest possible width, taking into routing constraints and current density and resistance limits.

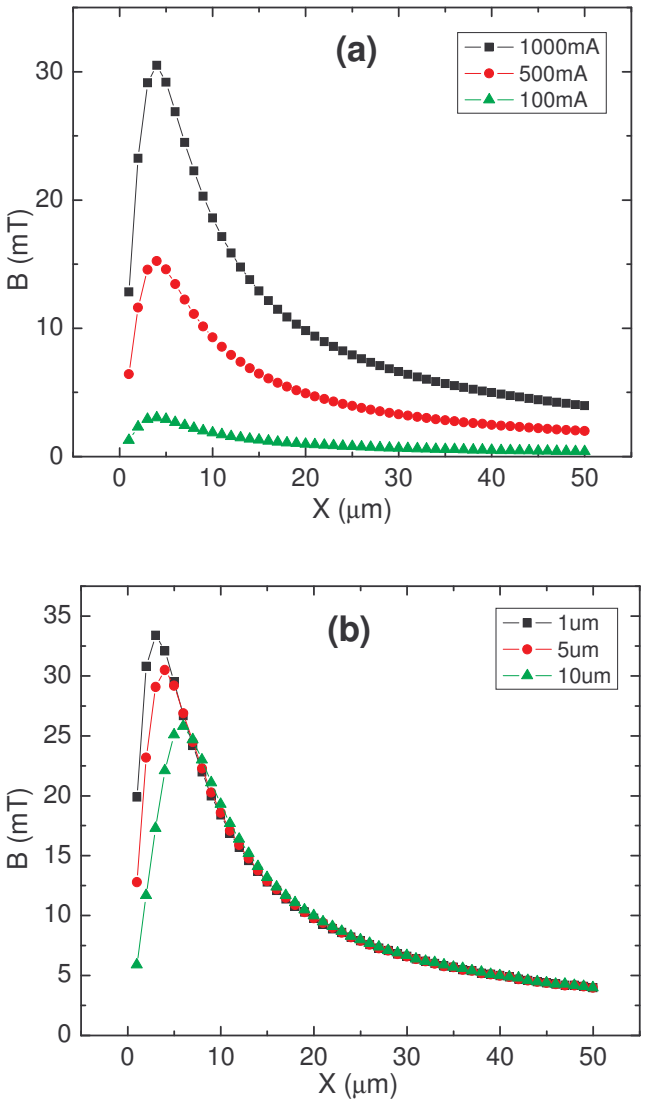

Fig. 21. (a) Magnetic field as a function of metal 2 line current and channel location. (b) Magnetic field as a function of metal 2 line width and channel location (current: 1000 mA).

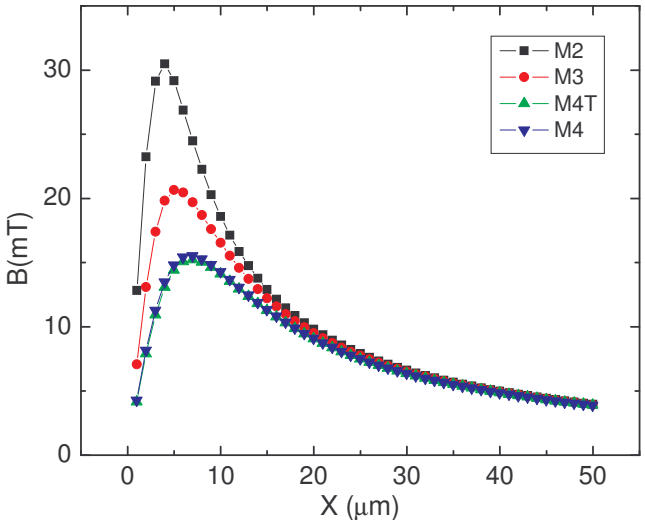

Fig. 22. Magnetic field for different metal layers for a current of 1000 mA.

4.4 Experimental Results of MAGFET Sensitivity

The test chip was fabricated with TSMC 350 nm technology, which has 2 polysilicon layers, 4 metal layers, a gate oxide thickness of 79 Å, and an NMOS threshold voltage of 0.59 V. A 3.3 V power supply was used. The packaging is a 40 pin ceramic DIP. The chip layout is shown in Fig. 23. The upper part of the chip contains the built-in current sensors that will be described in Sections 5 and 6. The lower part of the test chip contains 6 N-channel MAGFETs with geometry parameters listed in Table IV. Besides different channel (W/L) aspect ratios, the drain gap, notch depth and source narrowing were also varied. The metal lines were routed with the edge right above the edge of drain notch (refer to Fig. 19) for all MAGFETs except N4, which is 2 μm back from the notch end. All three available upper metal layers M2, M3 and M4 are used, with a metal line width of 5 μm.

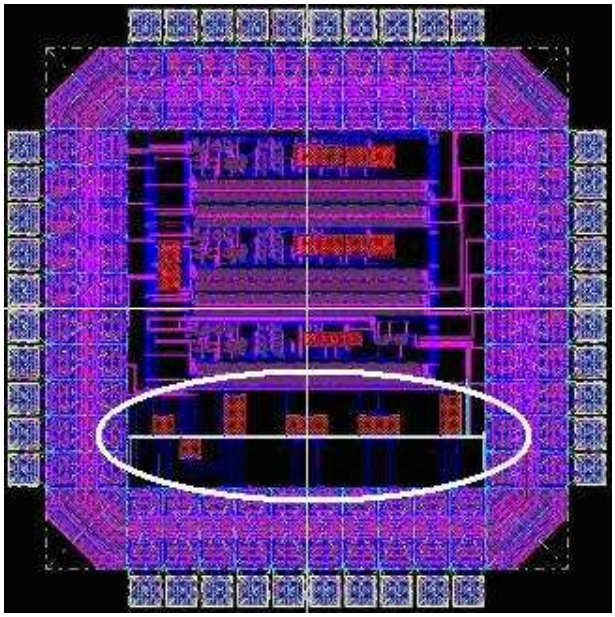

Fig. 23. The 350 nm test chip layout with 6 N-channel MAGFETs of different geometries (shown in circled area).

TABLE IV. GEOMETRY PARAMETERS OF TEST CHIP MAGFETS

MAGFET	W (μm)	L (μm)	D (μm)	d (μm)	u (μm)
N1	30	50	10	5	1
N2	30	50	10	2	1
N3	30	100	10	5	1
N4	30	100	10	5	3
N5	30	50	35	5	1
N6	60	50	20	5	1

The measurement setup is shown in Fig. 24. High input impedance operational amplifiers are used, with an input current of ~25 pA [97]. The two drain voltages are controlled by tuning the adjustable common mode voltages V_{dL} and V_{dR}. The two drain currents and their difference are:

$$I_L = \frac{V_L}{R} = \frac{V_{OL} - V_{dL}}{R} \quad , \tag{3.7}$$

$$I_R = \frac{V_R}{R} = \frac{V_{OR} - V_{dR}}{R} \quad , \tag{3.8}$$

$$\Delta I = \frac{\Delta V}{R} = \frac{V_L - V_R}{R} \quad . \tag{3.9}$$

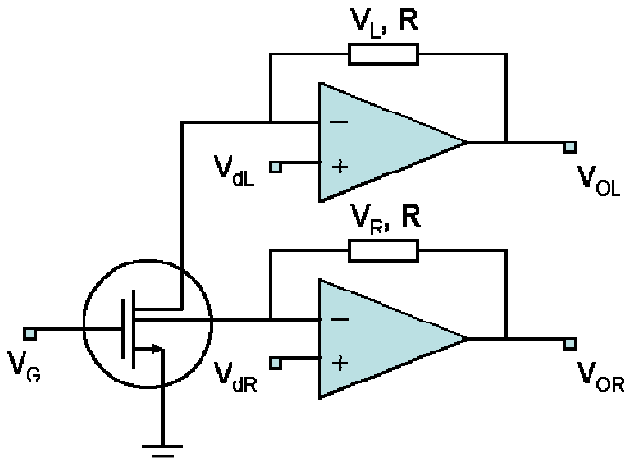

Fig. 24. Measurement circuit configuration for the MAGFET.

The MAGFET sensitivity measurements for N1 are plotted in Fig. 25 and Fig. 26. A series of different currents were forced through the M2 line to induce a variety of magnetic fields and the corresponding ΔV is obtained. Instead of marking the x-axis with current, the peak magnetic field was used. MAGFET sensitivity measurements in both the linear region (V_{GS}=1 V, V_{DS}=3.3 V) and saturation region (V_{GS}=3.3 V, V_{DS}=3.3 V) with bias currents of 600 μA, 400 μA and 200 μA were measured. We define the

MAGFET relative sensitivity as

$$S = \frac{\Delta I}{IB} \tag{3.10}$$

So the translated relative sensitivity from the measurement is 0.0063 T^{-1} and 0.0062 T^{-1} (or 0.63% T^{-1} and 0.62% T^{-1}) for the linear region and saturation region, respectively. This indicates the MAGFET sensitivity under non-uniform magnetic field is insensitive to operating region, in contrast to prior work with uniform fields, which showed the best results in saturation. The measured sensitivity of 0.63% T^{-1} and 0.62% T^{-1} is lower than previously reported values of 1.51% to 4% [97][98][99][100] and as high as 18.5% [101]. The lower sensitivity can be attributed to the fact that we are measuring sensitivity relative to the peak field, while prior work uses a uniform field.

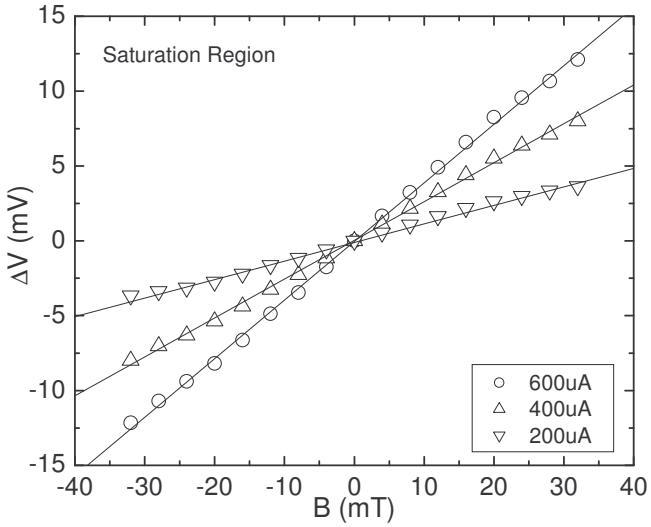

Fig. 25. MAGFET sensitivity (N1) at saturation region (R=100 KΩ).

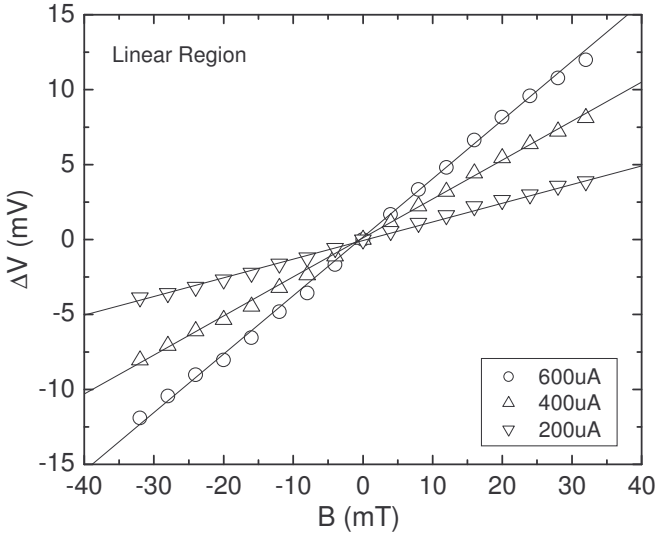

Fig. 26. MAGFET sensitivity (N1) at linear region (R=100 KΩ).

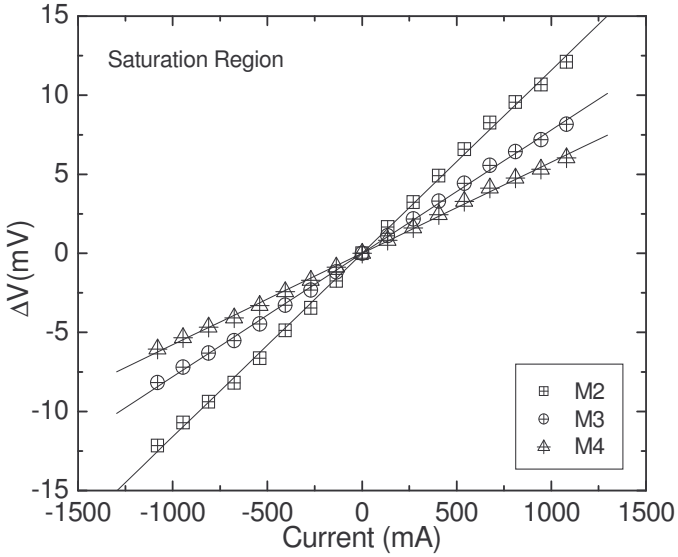

Fig. 27. MAGFET sensitivity (N1) under magnetic field generated by M2, M3 and M4.

MAGFET sensitivity for different metal lines was also investigated, as shown in Fig. 27. The MAGFET was biased in saturation (V_{GS}=3.3 V, V_{DS}=3.3 V) with a bias current

of 600 μA. Note the x-axis is the current applied. As predicted by the model, the MAGFET sensitivity for M3 was 67% of the sensitivity when using M2 and the sensitivity for M4 was 49% of M2.

The MAGFET sensitivity measurements for all devices are summarized in Table V. The highest sensitivity was achieved by N5, which was a wider device with source narrowing. The data shows that notch width and depth should be kept as small as possible. Drain gap degradation [97] manifests in N2 in that a smaller gap lead to higher sensitivity. Unlike previous studies on MAGFET sensitivity using a uniform magnetic field, the MAGFET aspect ratio did not significantly affect the sensitivity under a non-uniform magnetic field. This can be explained by the fact that the magnetic field generated by the metal lines becomes only significant only near the drains. However, since the magnetic field generated by a metal line extends for some distance, other current-carrying wires should be kept away from the MAGFET in order to minimize interference with the measurement.

Although MAGFET sensitivity for this on-chip non-uniform magnetic field seems to be less than that for a uniform magnetic field, it can still be used as the sensing element in a built-in current sensor. The following guidelines should be obeyed in order to achieve the highest possible sensitivity:

1. The current to be measured should run on the lowest possible metal layer, taking into account routing constraints.
2. The current should be run on the thinnest and narrowest metal line possible, taking into account resistance and current density constraints.

3. The metal line should be positioned so that the magnetic field is maximum at the end of the notch.
4. Other metal wiring should be kept away from the MAGFET in order to avoid interference
5. The MAGFET notch width and depth should be as small as possible, while the aspect ratio has some flexibility; Source narrowing should be used to improve the sensitivity.

TABLE V. EXPERIMENTAL RESULTS OF MAGFET SENSITIVITY FOR ALL DEVICES UNDER LINEAR (SL) AND SATURATION (SS) REGIONS

MAGFET	W/L	D	d	U	SL (%T^{-1})	SS (%T^{-1})
N1	30/50	10	5	1	0.63	0.62
N2	30/50	10	2	1	0.65	0.64
N3	30/100	10	5	1	0.62	0.62
N4	30/100	10	5	3	0.59	0.59
N5	30/50	35	5	1	0.67	0.68
N6	60/50	20	5	1	0.66	0.66

4.5 Which Way to Go: MAGFET or Direct Sensing?

The non-uniform magnetic field generated by on-chip metal lines has been studied using a model with simulation results, as well as test chip experimental results. The influence of MAGFET aspect ratio, notch depth and width, source narrowing and bias conditions on MAGFET sensitivity has been studied. As a result the general guidelines for MAGFET use for on-chip magnetic field monitoring have been given. Although a MAGFET is a plausible candidate for an I_{DDQ} sensing element, due to its non-contact

sensing property, its drawbacks outweigh the benefits. Based on the above results, we have decided to use direct voltage drop sensing of power supply lines, rather than MAGFET sensing. The reasons are:

1. In order to attain higher sensitivity, the MAGFET must sense lower metal layers, operating at high current density. In practice, power lines between cells are run on upper layers. Dropping down to a lower metal layer for the MAGFET would introduce a series resistance into the power grid.
2. The MAGFET is susceptible to disturbances arising from any current bearing metal lines in proximity to it. This requires additional chip area to accommodate in routing.
3. The external magnetic fields of the earth and nearby electrical equipment must be canceled. This requires using multiple MAGFETs [88][90].
4. A MAGFET sensor takes up substantial chip area in order to reduce flicker noise, and consumes appreciable power, due to its bias current.
5. Previous work [90] shows that MAGFETs have a low signal-to-noise ratio (SNR), which increases sensing time in a I_{DDQ} sensor system.

In contrast, the direct sensing approach taps two points of a small section of power line (e.g. 10 squares) to acquire a small voltage signal and feeds it to the next stage of the I_{DDQ} sensor system. This approach is flexible in terms of the metal line sensed, requires no area and has a signal level similar to that produced by the MAGFET, but with much lower noise. By analyzing and comparing the two sensing approaches, we favor the direct sensing method for our I_{DDQ} sensor system.

5. I_{DDQ} BICS SYSTEM DESIGN AND SIMULATION

5.1 Introduction

As discussed in the previous section, the proposed I_{DDQ} BICS senses the voltage drop on a section of supply line caused by the I_{DDQ} current. This voltage sensing approach was first used by van Lammeran [102], using an analog approach. Sunter proposed a related scheme using the IEEE 1149.4 analog test bus with external ATE [103]. Due to their analog nature, these approaches do not scale to large numbers of sensors. Previous work using a MAGFET sensor in a BICS had unacceptable noise level and calibration drift [90][104]. In view of these shortcomings, we propose a BICS design which is more robust and has the advantages of small area, low power, no chip speed penalty and it can be used for practical I_{DDQ} testing and diagnosis of large, high-performance chips. In this section we will discuss the details of each module of the proposed I_{DDQ} BICS and simulation results for the final design. All the simulations are carried out using Cadence Spectre for AMI 1.5 μm, TSMC 350 nm or TSMC 180 nm fabrication technologies. Since the sensor design have been implemented in three test chips of three different technologies, the variation and evolution of the design will also be presented.

5.2 Overview of Proposed Built-In Current Sensor System

The block diagram of the proposed BICS is shown in Fig. 28. The BICS system consists of a sensing element, a signal transmission circuit, an analog-to-digital conversion (ADC) circuit, a scan-chain counter, a data detector for calibration, and

calibration circuits.

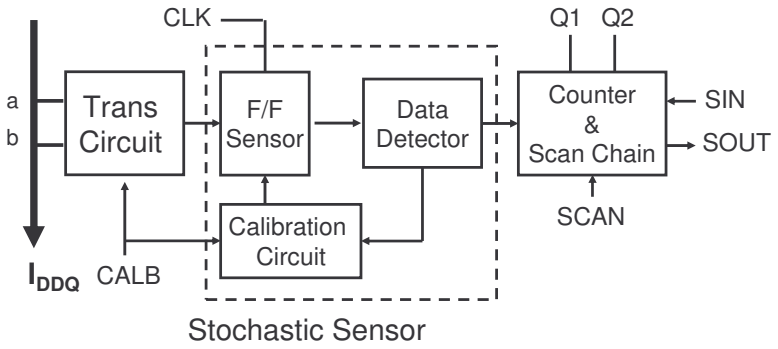

Fig. 28. Block diagram of the I_{DDQ} Built-In Current Sensor (BICS).

The BICS system works as follows. The voltage drop on the supply line between *a* and *b* passes through the transmission circuit and feeds the flip-flop stochastic sensor. The stochastic sensor amplifies the small signal and resolves into either a "1" or "0" in each clock cycle. The probability of resolving into each state is determined by the flip-flop signal-to-noise ratio (SNR) and the input voltage. The data detector converts this flip to a counter clock pulse in measurement mode (CALB=0) and calibration pulses in calibration mode (CALB=1). The generated bit stream of "0" and "1" is then accumulated in the counter. The counter value is the digital representation of the signal, so the stochastic sensor and counter form an analog-to-digital converter (ADC). The counter can then be converted to scan chain mode (SCAN=1) and the results scanned out. The self-calibration circuit nulls out any circuit imbalance and low frequency noise. The stochastic approach has two advantages: an ADC can be implemented in a small

area using digital components, and it can measure a signal much smaller than the random noise by operating in the metastable region and performing repeated measurements.

The input voltage signal in this design comes from the voltage drop through the resistance of a short section of a supply line (V_{DD}). With slight modification the BICS can be used to sense a ground line as well. The power line segment must be short enough to permit convenient tapping without requiring long and potentially noisy tap wires, and without interfering with the power grid design. For instance, ten squares of V_{DD} line with a sheet resistance of 10 mΩ/□ will generate a 1 μV signal when the current is 10 μA. We will use 1 μV as our desired signal resolution. Since the tap wires have insignificant capacitance, impedance and draw virtually no current from the CUT, the BICS does not introduce a performance penalty, unlike many other BICSs that introduce a series impedance. The BICS is fully digital and consumes little power in operation, and only leakage power when idle. These characteristics are essential if large numbers of sensors are to be used on a chip [105]. The design and functionality of each sensor module is elaborated in the following sections. A schematic of the design is shown in Appendix A.

5.3 Transmission Circuit

As shown in Fig. 29, the transmission circuit is placed between the probed power line and the flip-flop stochastic sensor. Inputs *ina/inb* tap a voltage signal at points *a* and *b* of the power line and feed pass transistors *P0/P1* to outputs *outa/outb*, which connect to the differential input *inn/inp* of the flip-flop stochastic sensor. The transmission circuit has two roles and is managed by the calibration control signal (*calb*). During measurement

(*calb*=0), the transmission circuit forms a low-pass filter between the input signal and flip-flop. During calibration (*calb*=1), the inputs are disconnected from the power line and the outputs are shorted and tied to V_{DD}. The flip-flop stochastic sensor requires its two inputs to be equalized to perform the calibration. In measurement mode, NMOS transistors *N0/N1* are used as capacitors to form low-pass filters in combination with PMOS transistors *P0/P1*. In order to minimize circuit area and avoid limiting test speed, the N0/N1 capacitors are sized so that the corner frequency of the low-pass filters are set to about 1 GHz. Since the differential input noise comes from the small sensing resistor, this corner frequency is adequate. During calibration *P0/P1* are turned off and the outputs are clamped to V_{DD} by *P4/P5* and equalized by *P3*. This permits calibration immediately prior to sensing, greatly reducing the drift requirements of the calibration circuit. The devices are larger than the technology minimum to reduce mismatch and noise. The circuit is designed to sense the V_{DD} line, but can be readily redesigned to sense the ground line. Sensing both V_{DD} and ground can reduce the number of sensors required [105].

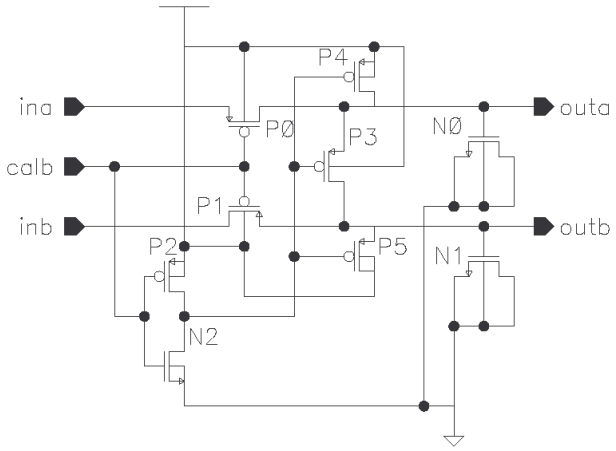

Fig. 29. I_{DDQ} BICS system component: Transmission circuit.

Simulation results of the transmission circuit are shown in Fig. 30. The inputs (not shown) are two sinusoidal waves of different magnitude and frequency. When calibration is low (*calb*=0 when *time* <1 ms), outputs replicate the inputs waveforms. After 1 ms, the control signal *calb* rises high and the outputs are tied to V_{DD}. The frequency on the inputs in this example is much higher than would be the case during I_{DDQ} testing (when the inputs should have almost DC values), so the transmission circuit introduces insignificant delay or attenuation of the input signal, but provides an input shorting capability for calibration.

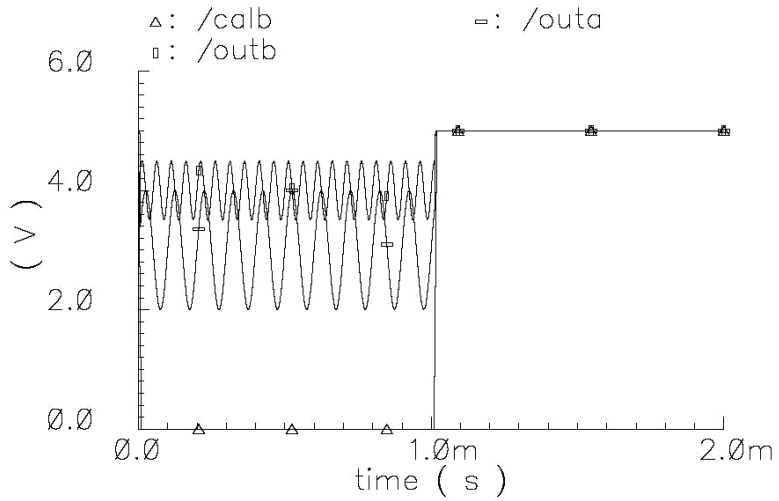

Fig. 30. Simulation waveform of the transmission circuit.

5.4 Flip-Flop Stochastic Sensor

Conventional methods to amplify small analog signals involve analog circuitry and relatively large chip area. In order to convert the small signal (~ μV) into a digital output, we use a flip-flop stochastic sensor operating in the metastable region to achieve high gain and analog-to-digital conversion. In each clock cycle the metastable flip-flop compares the signal with the background noise and resolves into either a "0" state or a "1" state. This evaluation process of signal versus noise is repeated a large number of times and the resulting bit stream is fed to the counter and accumulated there. Therefore the signal is statistically represented by the bit stream. Because the flip-flop is biased to the metastable region prior to each evalutaion, the slightest imbalance (even a random electron behavior) will cause the flip-flop to eventually settle to either of the stable states. Thus through this flip-flop stochastic sensor approach, small signals can be measured and converted to digital outputs.

5.4.1 Flip-Flop Stochastic Sensor Operation

In this research we implemented two types of flip-flop stochastic sensor. The first type is shown in Fig. 31. The main structure consists of two back-to-back inverters which form a flip-flop. The flip-flop is left-right symmetric. On each side there is an input transistor (*N1* or *N4*) in series with a calibration transistor (*N5* or *N6*) and together they form another pull down path which is in parallel with the pull down transistor of the inverter. The calibration transistor length is twice that of the input transistor, which makes the calibration gain twice that of the input. Simulation of the typical flip-flop switching events is illustrated in Fig. 32 and Fig. 33 shows the flip-flop resolution waveform. The operation of the flip-flop is as follows. When *P8* is turned off (*clk* is high), output nodes *outn* and *outp* are pulled to GND through *N1/N5* and N4/N6. When *P8* is turned on (*clk* is low), the differential input signal *inp/inn* is amplified with pulldown transistors *N1/N4* in series with calibration transistors *N5/N6*, working against pullup transistors *P6/P7*. The flip-flop nodes integrate the input signal until the cross-coupled pulldown transistors *N2/N3* turn on, comparing the signal to the noise, and positive feedback results in a flip-flop decision.

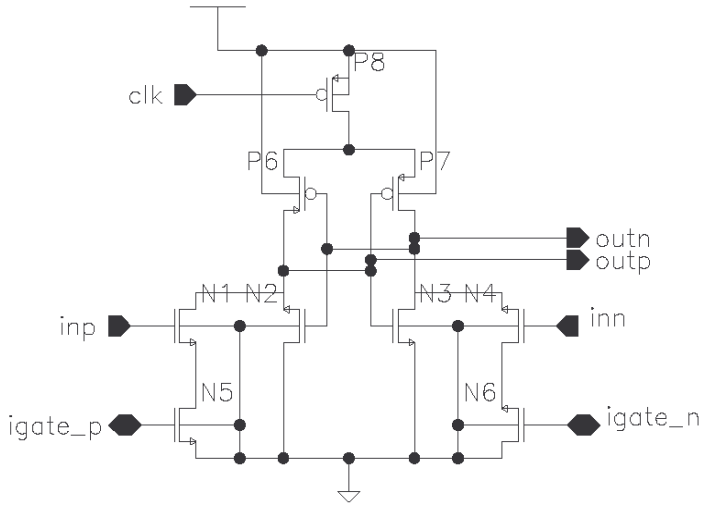

Fig. 31. Schematic of the first flip-flop stochastic sensor design.

This simple flip-flop design helps avoid unnecessary mismatch and redundant noise sources because more devices result in more mismatch and noise. Ideally, there should be no mismatch due to the fact that this circuit is perfectly symmetrical. However, in reality mismatch is always present because of process variation and circuit layout issues. To balance out this mismatch, we introduce the NMOS calibration transistors *N5/N6* for compensation purposes. The calibration transistors *N5* and *N6* are controlled by two independent calibration circuits which will be discussed below. These two calibration circuits provide a slight difference in the gate voltages of the calibration transistors, V_{igate_p} and V_{igate_n}, which force the flip-flop back to the balanced metastable state. A calibrated flip-flop has an equal chance to flip to one side or the other when there is no difference between inputs *inp* and *inn*. A differential input biases the probability that the flip-flop will flip to one side or the other.

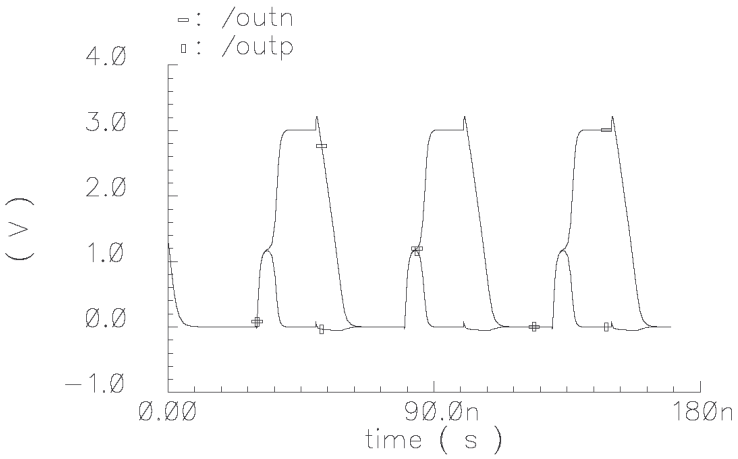

Fig. 32. Simulation waveform of typical flip-flop behavior.

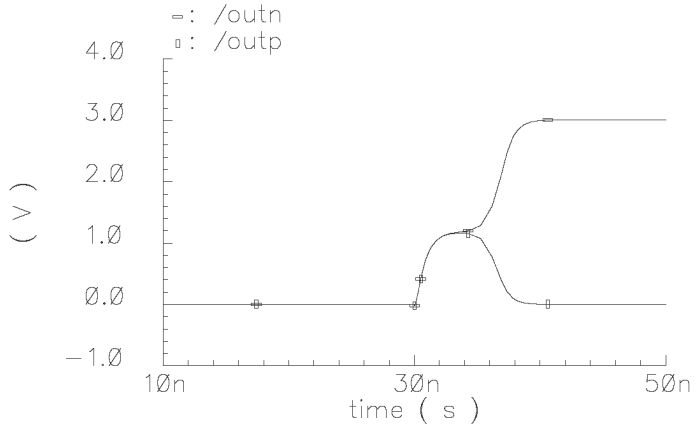

Fig. 33. Simulation waveform during flip-flop resolution.

The input pull-down paths mean that the flip-flop logic 1 output cannot reach V_{DD}, but settle at a lower voltage depending on the sizing of the pull-up and pull-down transistors. A higher logic 1 voltage requires the pull-down path to be as weak as possible. On the other hand, the flip-flop speed is very sensitive to the strength of the pull-down devices. The speed is also affected by the resolving time [106][107].

Resolving time is a function of the input signal difference, transistor sizing (i.e. transconductance g_m) and the load capacitance. A smaller input signal difference and larger parasitic capacitance lead to a longer resolving time. For 180 nm technology, the flip-flop can be clocked at well over 1 GHz with a resolving time of much less than a nanosecond.

5.4.2 Flip-Flop Stochastic Behavior

The response of a stochastic sensor follows a Gaussian cumulative density function (CDF) around the metastable point [108][109]. This can be approximated as linear when the signal is much smaller than the noise (the typical case), as shown in Fig. 34. The probability of getting a "0" or "1" from the flip-flop represents the equivalent magnitude of the analog input signal. The sign relative to 0.5 indicates the direction of I_{DDQ} flow. Since the CDF slope falls with rising noise amplitude, the "gain" of the stochastic sensor is inversely proportional to the noise. The noise has zero mean, so does not introduce an offset. The stochastic sensor achieves high sensitivity and high noise immunity through repetitive operation. Outputs of the stochastic sensor decisions, *outn/outp*, are fed into the counter. Using the slope of the CDF, the magnitude of the input can be deduced from the counter value. Knowing the magnitude of the input, the I_{DDQ} level can then be translated and derived, therefore this approach allows us to measure the I_{DDQ} level.

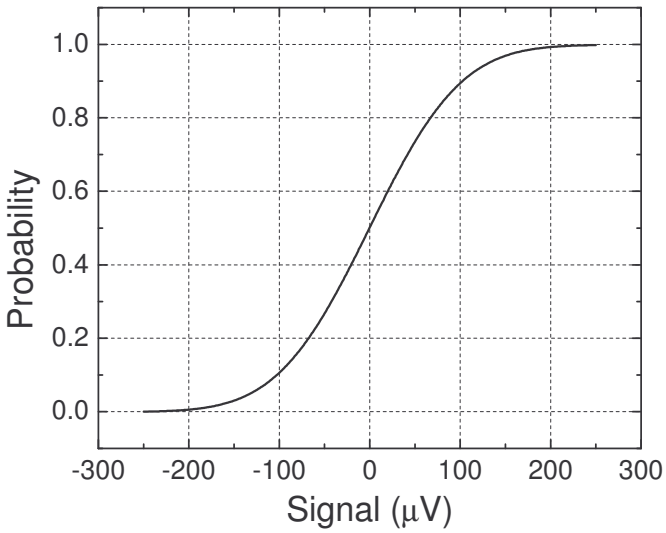

Fig. 34. Stochastic sensor conceptual transfer curve. The transfer curve can be approximated as linear in the center region when the signal is much smaller than the noise.

The predicted sampling variance for a flip-flop stochastic sensor is [110]:

$$\frac{pq}{N} \sim \frac{0.25}{N} \tag{5.1}$$

and the standard deviation is:

$$\sigma = [pq / N]^{\frac{1}{2}} \sim \frac{0.5}{\sqrt{N}} \tag{5.2}$$

where N is the number of measurement cycles and p and q are the probability for either side of the stochastic sensor to get a "1". This is close to 0.5 for our application. The probability for a "1" decision is given by:

$$p \sim 0.5 \pm \frac{1}{\sqrt{2\pi}} \int_0^S \exp^{-1/2u^2} \, du \tag{5.3}$$

where s is the signal to noise ratio (SNR). When $|s| << 1$, p can be approximated as

[110]:

$$p \sim 0.5 \pm \frac{s}{\sqrt{2\pi}} \tag{5.4}$$

So for N measurement cycles we have a "1" counter value of:

$$N \cdot p \sim N \cdot 0.5 \pm \frac{N \cdot s}{\sqrt{2\pi}} \tag{5.5}$$

As shown, lower noise results in higher gain. The BICS sampling process is a stochastic process so the number of samples N needs to be determined to guarantee the desired measurement resolution. It has been proved that the number of samples N required is [90]:

$$N \geq \frac{Z_{\alpha}^{2}}{s^{2}} \tag{5.6}$$

Z_{α} is determined from a t-distribution table based on the desired confidence level [109]. Therefore the sample size can be estimated with the SNR of the flip-flop and desired confidence level, as shown in Fig. 35. For example, if the SNR is 1/1000, then approximately 10^6 samples are needed to achieve a 99.9% confidence level.

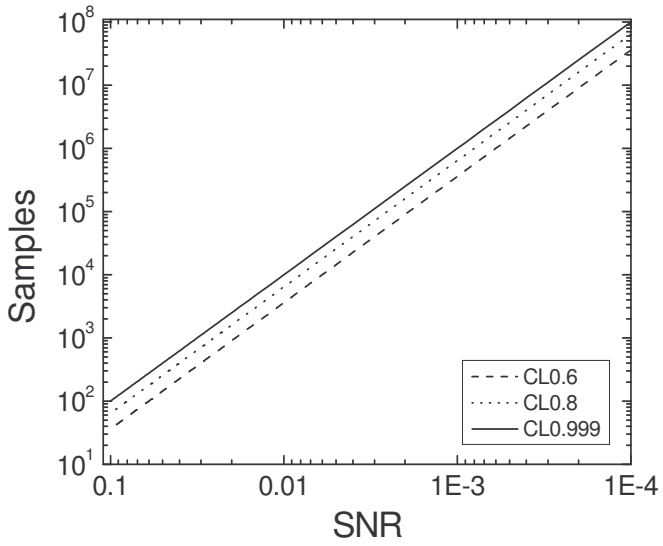

Fig. 35. Sample size is determined with SNR and desired confidence level.

5.4.3 Flip-Flop Stochastic Sensor Noise Analysis

The flip-flop noise comes from external noise and transistor noise. The transistor has two noise sources: thermal noise (white noise) and flicker noise [111], defined as follows:

$$S_{IW} = \begin{cases} \dfrac{4kT}{R_{FET}} & \textit{ohmic region} \\ \dfrac{8kTg_m}{3} & \textit{saturation} \end{cases} \tag{5.6}$$

$$S_{If} = \frac{2K_f K' I_{DQ}}{C_{OX} L^2 f} \tag{5.7}$$

where S_{IW} and S_{If} define the white noise and flicker noise spectral density, respectively, T is temperature in degrees Kelvin, k is Boltzmann's constant, R_{FET} is the equivalent field effect transistor (FET) resistance and g_m is the small signal transconductance. The RMS

noise current source in the frequency band [*f1, f2*] can be obtained from the spectral density:

$$I_{NB} = \sqrt{\int_{f_1}^{f_2} S_N \, df} \tag{5.8}$$

As flicker noise dominates in the lower frequency range while our BICS is intended for high frequency usage (>10 MHz), the thermal (white) noise is the main contributor in the BICS. The simulated flip-flop output noise voltage spectral density curve for 350 nm technology is shown in Fig 36. This is simulated by holding the flip-flop node voltages at their metastable values. Assuming a flip-flop frequency of 40 MHz, the noise band of interest is from 40 MHz to the cut off frequency at approximately 10 GHz. The flicker noise component was not included in Fig. 36. By integration of the calculated noise spectral density over the band, the total simulated input-referred RMS noise is 1.2 mV. For a 1 μV input signal, this is an SNR of 1/1200.

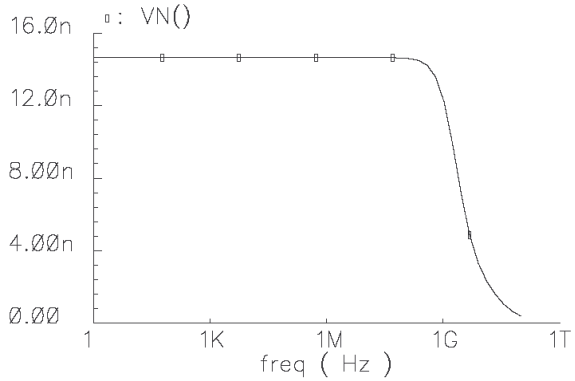

Fig. 36. Flip-flop noise simulation. Flicker noise is not included since only frequencies higher than 40 MHz are of interest.

5.4.4 Second Flip-Flop Stochastic Sensor Design

For our 180 nm technology test chip, we revised the flip-flop stochastic sensor to include a preamplifier, similar to a sense amplifier [112], as shown in Fig. 37. The preamplifier reduces the input-referred noise. Since the test chips are clocked at 40 MHz, the flip-flop transistor channel lengths are also increased to reduce the flip-flop bandwidth, reducing the noise level. The simulations are shown in Fig. 38. Compared with a sense amplifier, it has an essential difference. The two output nodes which are precharged by two clocked PMOS transistors (not shown) in a sense amplifier are replaced by one clocked PMOS transistor *P14* between the output nodes. The reduced precharge voltage increases flip-flop speed and lowers power dissipation. Two design variations are shown in Fig. 37. One has shunting transistor *N22* and one does not. This transistor reduces voltage swing and power dissipation. Simulation results indicate that the design without *N22* is faster with a similar noise level, so we used this design variation. Besides higher gain due to the preamplifier, this stochastic sensor design is faster than the previous design. During the precharge phase, our previous design discharged all nodes to GND when the clock was off, so takes longer for internal nodes to charge to the metastable point during evaluation. In the new design, since both output nodes are precharged to V_{DD}-|Vtp|-Vtn, the charge is recycled during the evaluation phase, reaching a decision faster. This also reduces power dissipation. Since we wish to minimize the noise for a fixed operating frequency, transistors are sized so that the new flip-flop design operates adequately at 40 MHz, but not much faster.

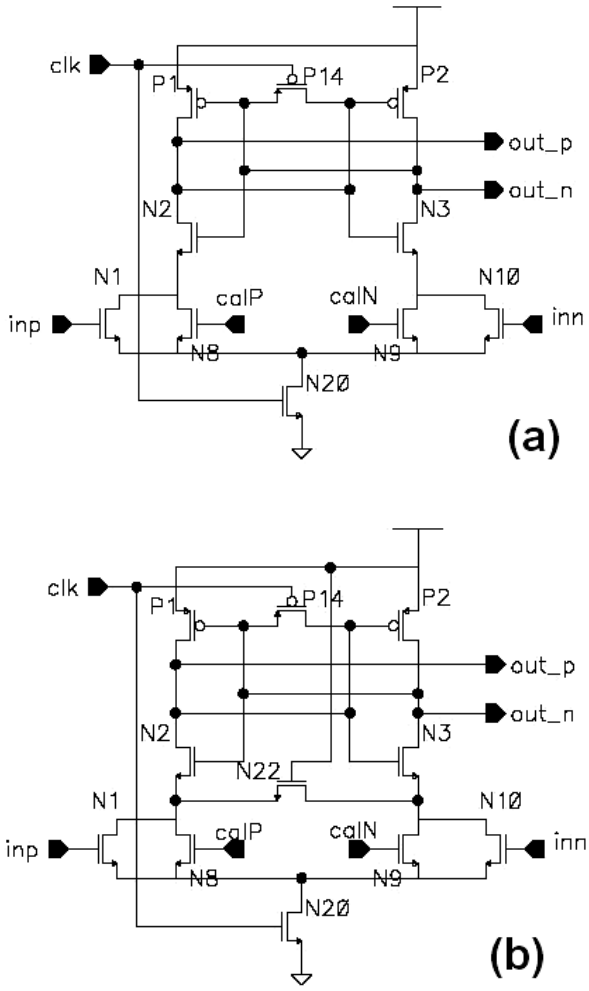

Fig. 37. Revised flip-flop stochastic sensor with (a) and without (b) shunting NMOS transistor N22.

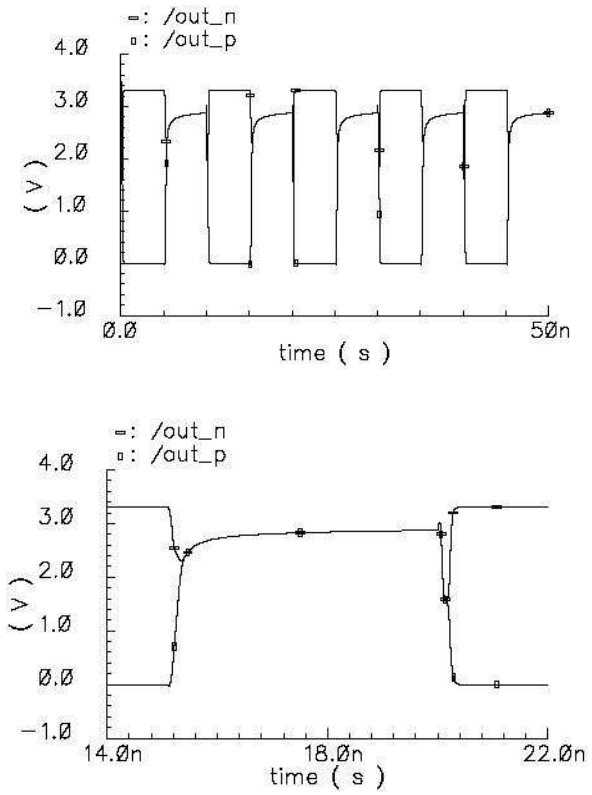

Fig. 38. Simulated waveform of the second flip-flop sensor design, including a close-up view of one switching event.

5.5 Data Detector Circuit

The data detector circuit is placed between the flip-flop stochastic sensor and the calibration circuit. There is one data detector for each side of the flip-flop, with the input signal *in* connected to the flip-flop output. In measurement mode (*calb*=0), the data detector does not operate and the flip-flop results are simply fed to the counter. In calibration mode (*calb*=1), whenever *in* falls to 0 (from being precharged to 1), the data detector generates calibration charge pump clock pulses to pump down the calibration voltage on the flip-flop side that produced the "0" and pump up the other side, as shown

in Fig. 42. This reduces the probability of the flip-flop making the same decision next time. The major component of the data detector is the pulse generator, which is implemented using the typical NOR latch scheme, as shown in Fig. 39. It produces non-overlapping pulse pairs *pu1/pu2* and *pd1/pd2*, which pump up/down the calibration voltage through the calibration circuit. Simulation of the data detector is shown in Fig. 40(a) and Fig. 40(b) for both pump down and pump up pulses.

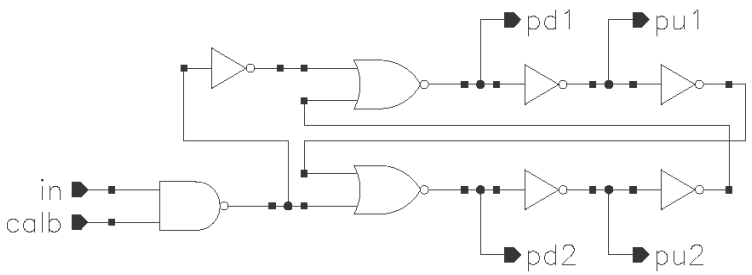

Fig. 39. Data detector can generate non-overlapping charge pump clock pulses.

The flip-flop outputs are also fed through 2-to-1 multiplexers controlled by *calb*. When *calb*=0, the flip-flop outputs clock the counters. When *calb*=1, the counter clocks are held stable. This permits calibration in the middle of a measurement without disturbing the partially measured value. This feature enables us to perform “digital chopping” analogous to analog chopping, to remove low-frequency noise and drift.

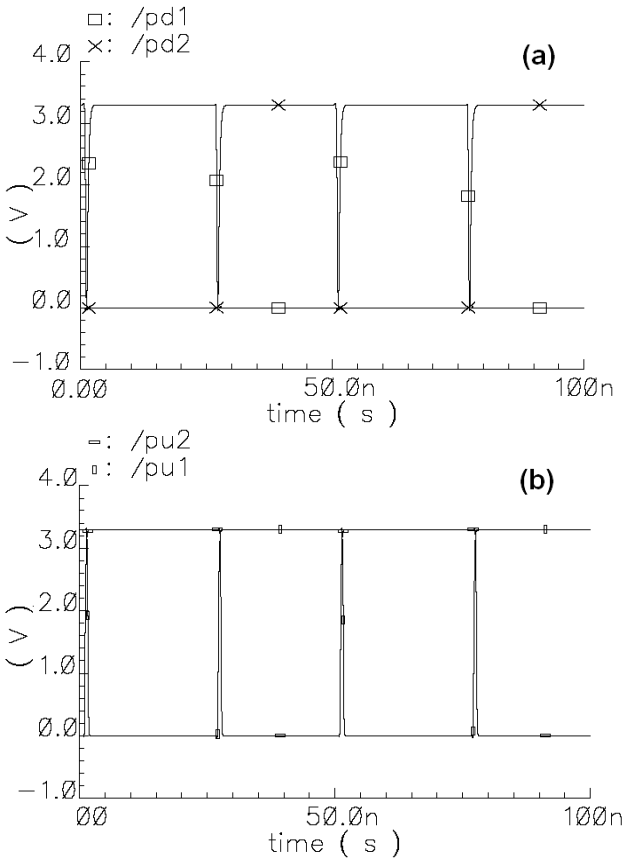

Fig. 40. Simulated non-overlapping pump down pulses (a) and pump up pulses (b).

The 350 nm test chip results suggested that the pump clocks might not be completely overlapping. For the180 nm test chip, two buffers were inserted into the feedback paths of the data detector pulse generator, in order to increase the dead time between pulses, as shown in Fig. 41. Overlapping pulses destroy calibration functionality.

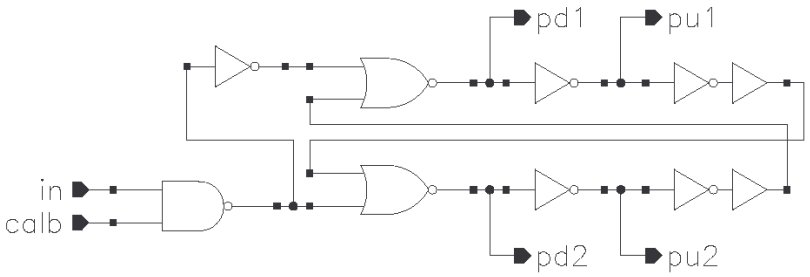

Fig. 41. Revised data detector with additional buffers to increase the non-overlapping interval.

5.6 Calibration Circuit

Although the flip-flop stochastic sensor achieves high gain, high resolution and noise immunity, it is extremely vulnerable to device mismatch, which is unavoidable in manufacturing. Due to the high gain, even a small mismatch will affect the resolution and accuracy. In order to correct the mismatch, a self-calibration scheme is introduced and used to control the gate voltage of calibration pulldown transistors *N5/N6* in the flip-flop stochastic sensor, as shown in Fig. 42. Mismatch resulting from manufacturing, layout or external noise can be compensated for through a slight imbalance of the calibration transistor gate voltages. The two pulse generation circuits will generate calibration pulses based on the two outputs of the flip-flop and these pulses will feed to two independent calibration circuits which control the gate voltage of *N5* and *N6*.

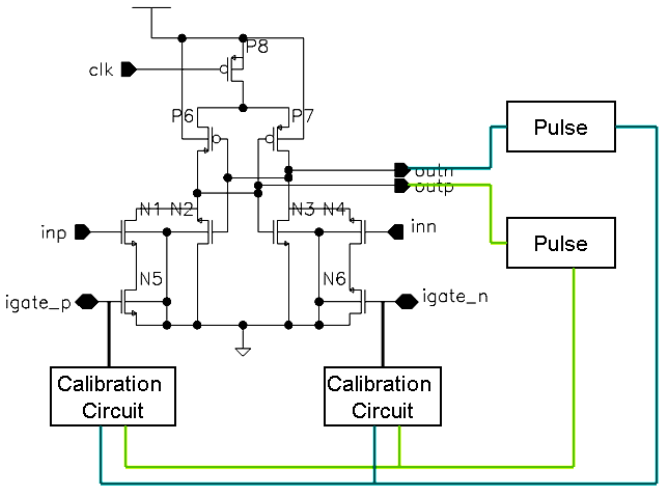

Fig. 42. Calibration scheme for flip-flop mismatch compensation.

The calibration circuit features high resolution, wide adjustment range and long holding time. As illustrated in Fig. 43, transistors *P6/N6* act as the reservoir capacitor, with balanced gate oxide leakage paths. Transistors *P1/P7* and *N1/N2* form a charge pump with symmetrical pullup/pulldown paths, controlled by nonoverlapping clocks *pu1/pu2* and *pd1/pd2* from the pulse generator circuits. To charge the reservoir capacitors, first *P1* is pulsed to charge the *P1/P7* parasitic junction capacitance and then *P7* is pulsed to transfer the charge to *P6/N6*. The discharge is realized through the pulldown charge pump *N1/N2* in a similar manner. Stack transistors *P2/P3/P4* and *N3/N4/N5* are shut off after calibration is completed and significantly reduce leakage [113] when holding the calibration voltage.

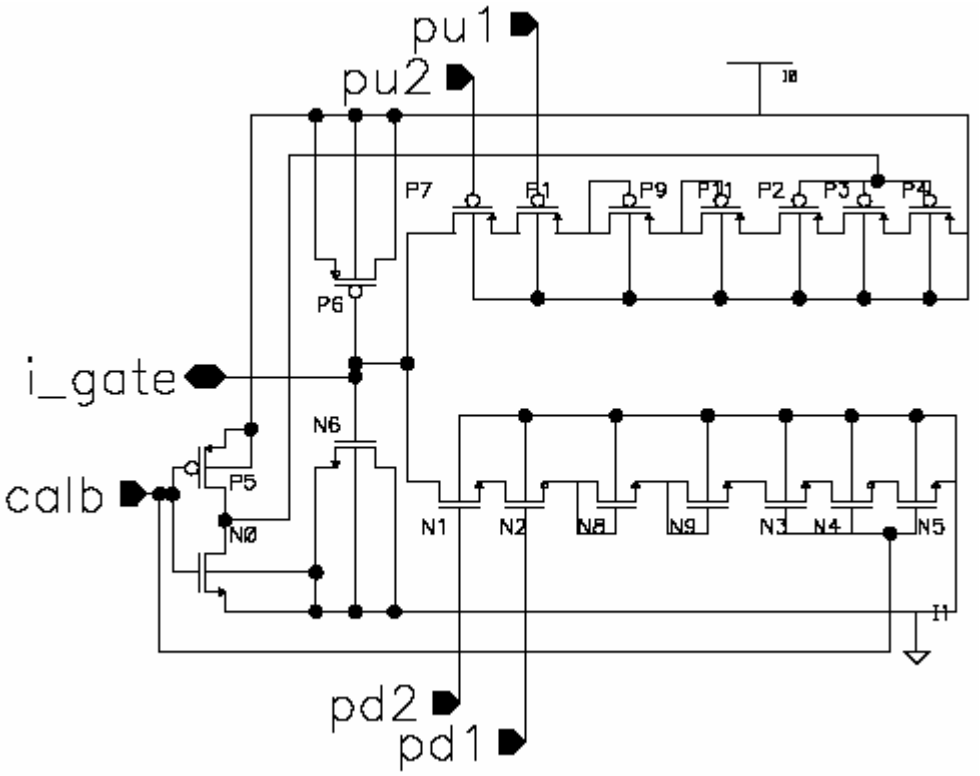

Fig. 43. Charge pump based calibration circuit.

Two “diode-connected” transistors, *P9/P11* and *N8/N9* have been added between the stack transistors and pumping transistors in both the pullup and pulldown paths. These transistors limit the calibration voltage range (and so increase its resolution), and act as resistors to limit the pumping current, also reducing the step size and the calibration voltage drift rate. In technologies with a lower supply voltage, such as TSMC 180 nm, only one diode-connected transistor is used, rather than two. A variation of this calibration circuit in newer technology, such as the TSMC 180 nm, is to reduce the number of two “diode-connected” transistors to only one. This maintains a reasonable calibration range.

The flip-flop stochastic sensor has two calibration circuits controlling the two calibration pulldown transistors independently. Simulation and experimental results indicate that before calibration starts, the calibration node *i_gate* will leak to an intermediate voltage high enough to turn on pulldown transistors *N5/N6* of the flip-flop as shown in Fig. 44. During calibration the off-balance flip-flop stochastic sensor will mostly flip to one side. The data detector generates pulses so that the calibration voltage on one side will ramp up while the other side ramps down to force the flip-flop back to a balanced state.

There are two primary challenges in the calibration circuit. The first is to achieve sufficient resolution (small calibration voltage step size) and the second is to curb the drift during the measurement mode. A suitable charge pump capacitance ratio determines the step size while the drift issue can be alleviated using high V_{TH} devices and stacking them. The drift requirement of the calibration circuit is further reduced by using "digital chopping". In a standard chopper operational amplifier, the inputs are periodically shorted, and any observed output voltage difference stored on capacitors and then subtracted from the signal during sensing [114][115]. In our digital chopping approach, measurement is performed for a certain number of cycles, then recalibration is performed for a certain number of cycles, and then the process is repeated. During calibration the counters do not change, so the output value is not affected. By using shorter measurement and calibration periods, the drift requirements of the calibration circuit are relaxed. This permits the calibration circuit to be used in future leaky technologies. Frequent recalibration also permits calibrating for temperature drifts and

low-frequency noise.

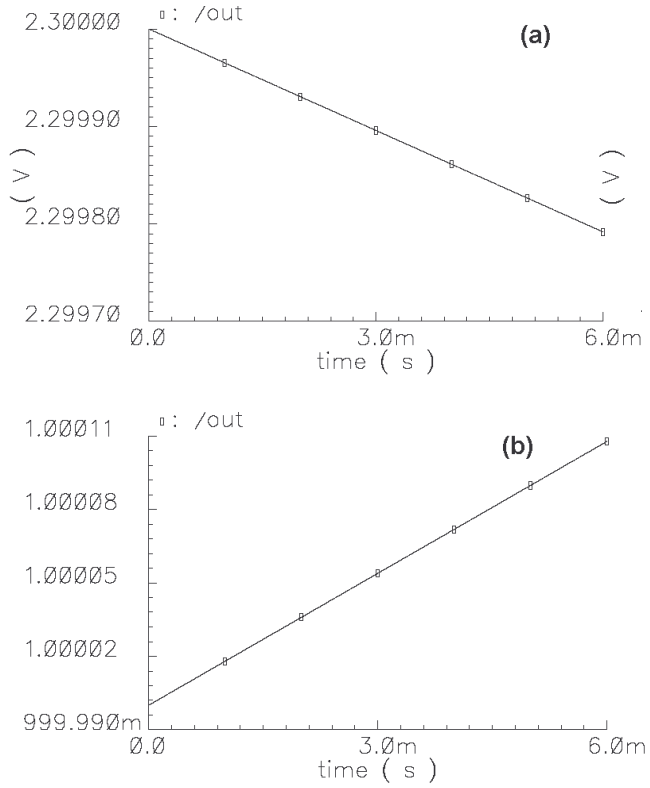

Fig. 44. Circuit simulation of calibration drift at room temperature with 2.3 V initial voltage (a) and 1.0 V (b), for 350 nm technology.

Circuit simulation of the drift rate was performed by setting an initial calibration voltage and measuring the node voltage drift with time. Two typical scenarios are presented with high/low initial voltage to show the drift down and drift up in 350 nm technology. Fig. 44(a) and (b) show the voltage drift down from 2.3 V and drift up from 1.0 V, respectively. Based on circuit simulation at room temperature, the downward drift rate is approximately 350 μV/10ms and upward drift is approximately 183 μV/10ms. In

practice drift should be less than this since the calibration voltage should be close to $V_{DD}/2$ (1.65 V). Assuming a measurement period of 1000 clock cycles at 40 MHz (25 μs), the differential drift should be slightly more than 1 μV per measurement period. If the drift is always in the same direction during a measurement period, this is the equivalent of an input offset of less than 1 μV. In practice the calibration voltage at the start of each measurement period will be above or below the equilibrium point, and so the equivalent offset due to drift should be much less than 1 μV. Thus calibration voltage drift is not a significant factor in sensor resolution. In newer technologies thick-oxide, high V_{TH} devices can be utilized to counteract the drift (leakage) problem, but at the expense of chip area.

A tradeoff must be made between the calibration resolution and calibration time, where the pump step size is the determining factor and is decided by the capacitance ratio. Circuit simulation of the calibration pump up/down process for 350 nm technology is shown in Fig. 45(a) and (b). For the pump up case there is a large step size variation since the calibration voltage tends to ‘saturate’ at 1.7 V. In contrast, the pump down case has a smaller variation in step size in the range of interest. The pump up process can be divided into coarse pumping and fine tuning phases. The coarse phase occurs below 1.7 V and the fine tuning phase at 1.7 V and above. In coarse pumping the average step size is 125 μV while in fine tuning the step size is only 4 μV. The sensor benefits from this behavior in that coarse pumping helps the sensor quickly reach the rough calibration zone while fine tuning phase makes it possible for the sensor to achieve the desired accuracy. The pump down is a more smooth semi-linear process with an average step

size of 31 μV. The simulated attainable pumping range is from 0.7 V to 2.11V. Beyond this range the pump step size balances the drift in the corresponding clock cycle. The actual lower bound is less than 0.7 V, but at that point the calibration transistor cuts off.

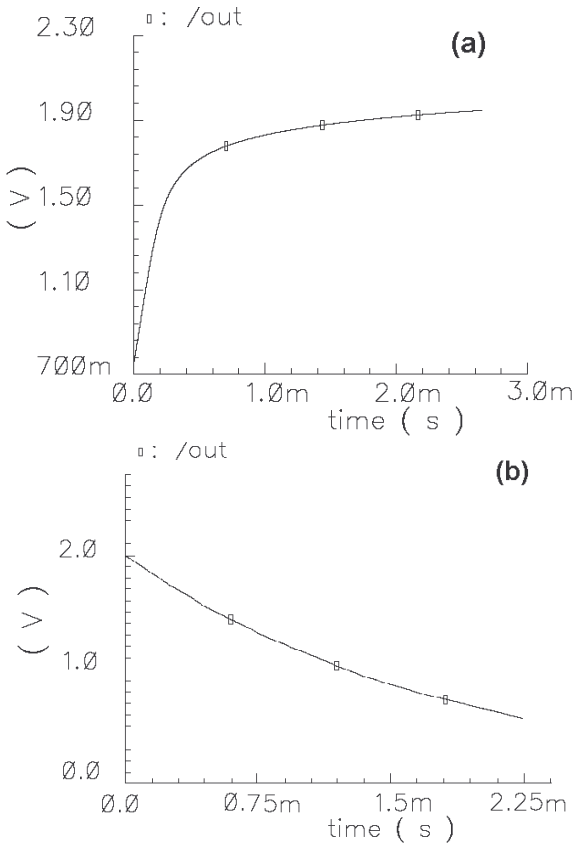

Fig. 45. Simulation of calibration voltage pumping up (a) and pumping down (b).

5.7 Counter and Scan Chain

As we discussed earlier, the stochastic analysis is a sampling process, so counters need to be incorporated in the BICS to accumulate the results from the flip-flop stochastic sensor. For easy initialization, readout and on-chip I_{DDX} algorithm

implementation, the counters should double as a scan chain. As such we combine the counter and scan-chain together yet maintain the simplicity of the design, since the counter/scan-chain takes most of the BICS system area and transistor count. Our 17-transistor counter/scan chain cell is illustrated in Fig. 46. The number of counter bits is determined by the flip-flop SNR and desired measurement resolution, but is set to 22-24 bits in our test chips. A schematic of an N bit counter formed by N cells is shown in Fig. 47. The counter/scan chain has two operating modes, i.e., count and scan. In count mode (*SCANB*=1) each cell forms a toggle flip-flop. In scan mode (*SCANB*=0), pull-down transistors *N9*, *N8/N5* and *N6/N7* are shut off. Serial input *T_1* is fed into the master stage through transmission gate *P4/N10* to inverter *P0/N0*. Weak inverter *P2/N2* provides feedback to make the master static. Transmission gate *P3/N1* and inverter *P1/N1* form the dynamic slave latch to output *T*. *Q1/Q1B* and *Q2/Q2B* are the non-overlapping scan clocks. In count mode, *N9* is on, *Q1*=0 (*Q1B*=1), *Q2*=1 (*Q2B*=0), transmission gate *P4/N10* is off and transmission gate *P3/N1* is on. The inputs *T_1* and its inverse *TB_1* control the pull-down paths *N8/N5* and *N6/N7*. When *N8/N5* is on, it pulls the input of inverter *P0/N0* low, flipping the cell so that node *B*=1and outputs *T*=0, and *TB*=1. When *N6/N7* is on, node *A*=1 and node *T*=1 and *TB*=0. Transistors *N4* and *N3* are used to store the previous state of *A/B*, and cause the cell to toggle on each input transition. The sequence of cells forms a ripple-carry counter. Since each bit flips at half the rate of the previous bit, the net active power dissipation of the counter is equivalent to two bits flipping every clock cycle. Circuit simulation shows that the 350 nm counter is able to operate at several hundred megahertz. In 1.5 µm, simulation indicates there are

small glitches in the toggle pulses, although experimental results showed no problems. As a precaution, noninverting buffers were added to the *T* and *TB* signals to concatenate adjacent counter cells in 350 nm technology. These buffers are not shown in Fig. 46and they were not included in the 180 nm design.

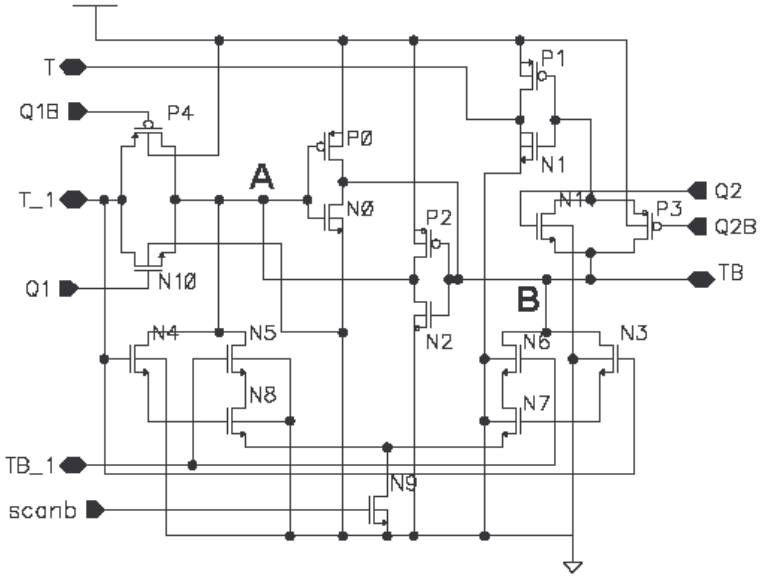

Fig. 46. Schematics of counter/scan chain cell.

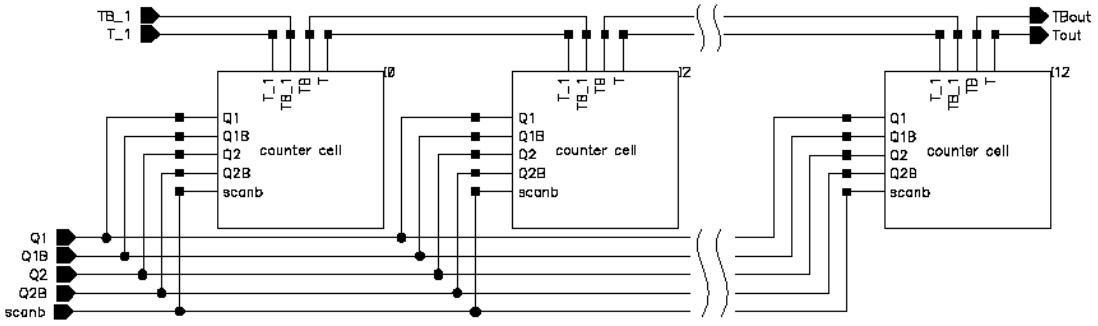

Fig. 47. Counter/scan chain cells form N bits counter.

5.8 Chip Partitioning and BICS Operation

We have discussed the benefits of BICS used in conjunction with CUT power supply partitioning. The main advantages are higher I_{DDQ} resolution and fault diagnosis and localization capabilities. A conceptual block diagram of chip partitioning with BICSs is shown in Fig. 48. The chip is divided into 16 partitions and in each partition we insert a BICS. All these BICS are hooked up together in series so that in scan operation they function as shift registers to initialize all the counters or output the results. The techniques for chip partitioning are discussed elsewhere [108]. The goal is to have comparable background leakage in each partition and the background leakage is small enough to differentiate from defective I_{DDQ}.

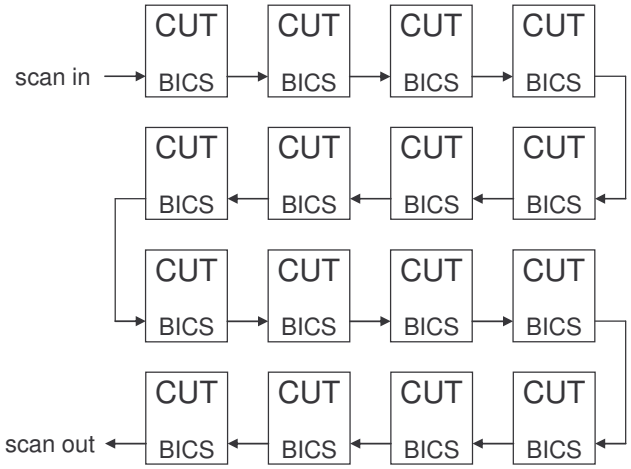

Fig. 48. Conceptual chip partition with BICS sensor network.

The operation of the proposed I_{DDQ} sensor consists of four different operation modes:

scan-in, calibration, measurement and scan-out. The timing chart of the BICS operation is illustrated in Fig. 49. The BICS operation is divided into 3 stages: scan-in in parallel with calibration, measurement and scan-out. In the scan-in mode, the counter/scan chain is operating as a shift register and reset by scanning in zeros serially using the scan clocks, with *SCANB* low. For the scan-out stage the measurement results can be obtained similarly. During scan-in, the external calibration signal (*CALB*) can be asserted along with the flip-flop clock to perform self-calibration. The normal measurement mode is initiated by removing *CALB* and applying flip-flop clocks. In the timing chart we do not show any recalibration during measurement. In practice recalibration periods are interleaved with measurement periods to perform "digital chopping". Similarly, scan-in and scan-out can be overlapped.

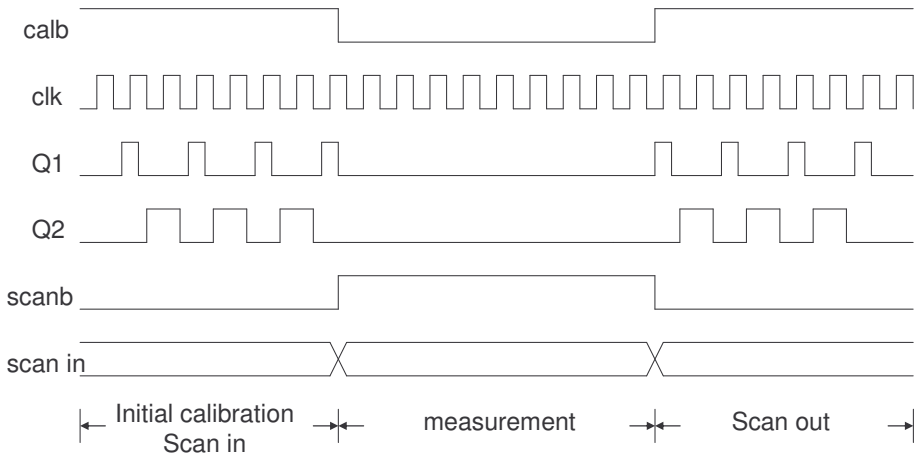

Fig. 49. Timing diagram of BICS sensor system operating modes.

5.9 BICS On-Chip Controller and Usage Methodology

As discussed above, the sensor operation depends on a number of external control signals. The number of control pins must be kept at a minimum. In addition, the ATE usage and bandwidth needed to operate the sensors should be minimized. One way to do this is to simplify the tester interface to realize a push button operation. This can be done by having an on-chip controller generate the sequence of calibration and scan controls, flip-flop clock and Q1/Q2 clocks. The tester interface could then consist of simple commands such as CLEAR and MEASURE, in which CLEAR would initialize the sensors while MEASURE would issue the sequence of calibration control and flip-flop clocks to perform the measurement. The MEASURE command could take parameters such as the total number of measurement cycles, and number of calibration and measurement cycles per period. After MEASURE, the tester could apply normal scan clocks, which would be converted into Q1/Q2 clocks by the controller, to read out the measurement values. The controller would feed in zeroes to reset the counters prior to the next measurement. The block diagram of the controller is shown in Fig. 50. It has 3 inputs: CLK, CLEAR and MEASURE. Based on the input conditions, the controller will automatically issue the calibration and scan controls. Rather than separate CLEAR and MEASURE inputs, the controller could use an IEEE 1149.1 tester interface.

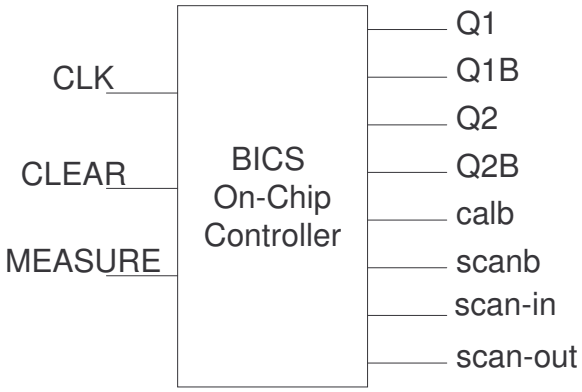

Fig. 50. BICS on-chip controller.

A more advanced controller can implement a simple test algorithm. For example, ΔI_{DDQ} can be implemented by scanning all sensor values into the controller, taking the difference between each measurement and the next, and remembering the max and min difference. The max and min values could then be read out for a tester decision, either after each I_{DDQ} measurement, or after all measurements are completed. A current ratio (CR) test could be implemented by scanning out all sensor values, remembering the max and min values, which can then be read by the tester and divided to compute the current ratio. The NNR test method first computes the average of all I_{DDQ} vectors for each chip. This can be implemented by having the controller compute the sum of all sensor values for all vectors, which can then be read by the tester and divided by the total number of sensors and vectors. The assumption in CR and NNR is that division is too expensive to implement in the controller and need only be done once, so it can be done by the ATE.

Controller designs such as discussed above are implemented purely in digital logic and are small compared to the chip area and aggregate BICS area (assuming many

BICSs). Since there is no concern about whether such controllers can be implemented in current and future technologies, they were not included on any test chip.

Due to the fact that the white noise spectral density is proportional to temperature, sensor gain falls with increasing temperature. Since temperature varies from sensor-to-sensor and over time, the gain must be calibrated if measurements are to be taken in terms of absolute I_{DDQ}. One solution is to bump up V_{DD}, measure the proportional increase in total chip I_{DDQ} and sensor values. If I_{DDQ} increases proportionally in all sensors, then the different sensor values indicate relative sensor gains. This also provides an indirect measurement of the temperature distribution across the chip. An alternative approach to gain calibration is to insert a switched current source into the V_{DD} line feeding each BICS sensor. This source would then provide a step increase in current, which would cause a corresponding increase in BICS counter value. Gain calibration becomes less important as statistical and self-scaling techniques such as NNR, CR and NCR are used for pass/fail determination.

5.10 BICS Area Overhead Reduction

For all built-in current sensor approaches, the most important concern is the area overhead. A successful design should achieve its design goals as well as keep the area overhead at minimum. Since the test chip was pad-limited in our design, no attempt was made to tightly-pack the sensor layout. The layout was also restricted to the first two metal layers to provide placement flexibility in using the sensor in a chip design. With this relatively loosely-packed layout, a full 350 nm sensor with two counters (up and

down) is approximately 83,490 μm^2 using two 50×50 μm calibration reservoir capacitors on each side of the flip-flop. A production sensor will only need one counter, reducing the area to 53,850 μm^2. Shrinking the calibration capacitors and tightly packing the layout, the sensor area should be approximately 30,000 μm^2, permitting 33 sensors to use no more than 1% of the area of a 1 cm^2 die. The relative area should scale with advanced technologies.

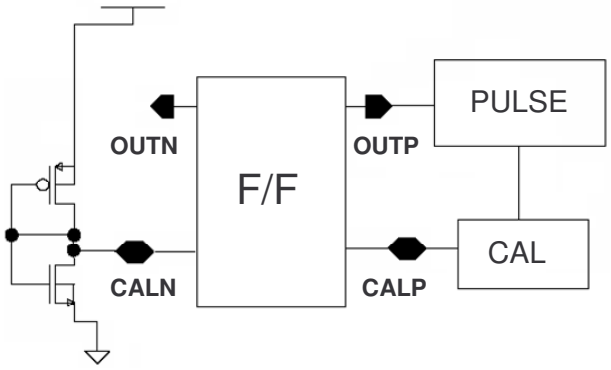

Fig. 51. BICS with single side calibration.

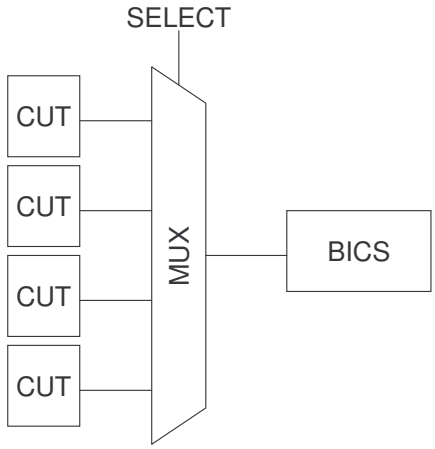

Fig. 52. Multiplex inputs enable several partitions to share one BICS.

There are several other area reduction techniques that can be utilized. The first is to replace the two-sided calibration with single-sided calibration. This can be done by replacing one calibration circuit with a constant voltage source, such as shown in Fig. 51. Based on our simulations and experimental results, one-sided calibration has enough range to cover flip-flop mismatch. The single-sided calibration also eliminates the need for one data detector. Another effective area reduction approach relies on sharing BICSs among several partitions. As shown in Fig. 52, the BICS input can be multiplexed among several partitions (CUTs). The multiplexer would be integrated with the transmission circuit, and so take little additional area. The multiplexer inputs can either be global signals or be supplied by scan chain bits. The drawback of multiplexing is the corresponding increase in total test time. The amount of multiplexing would be limited by the length of the tap wires, so would likely be limited to only 2-8 measurement points. An example would be measuring the two wires coming off each pad in a bumped chip.

5.11 Conclusions

In this section we have described our I_{DDQ} BICS design. The BICS architecture, functional modules, operation, usage methodologies and possible improvements have also been discussed. Circuit schematics, simulation results and modifications with technology evolution have also been presented. We have shown that the proposed BICS is able to yield high I_{DDQ} resolution and represent the I_{DDQ} level as a numerical value, which is a unique characteristic that other BICS approaches do not possess. The

quantitatively represented I_{DDQ} will not only reveal the actual value of I_{DDQ} but also make it possible to implement on-site resolution enhancement techniques such as delta I_{DDQ}, and current ratio. The proposed BICS will be used with chip power grid partitioning, which will simplify the process of defect localization and diagnosis. An on-chip controller will automatically coordinate the operation among the different functional modules inside the BICS and simplfiy the interface with the outside world. The BICS size is small enough to meet our area overhead objectives. In addition, further area reduction techniques have been explored. In the next section, we will present our test chip results for three generations of technologies.

6. TEST CHIP RESULTS AND DISCUSSION

6.1 Introduction

The proposed I_{DDQ} BICS design has been implemented in silicon. This section presents the experimental results of three test chips spanning three different technologies. The technologies used are AMIS 1.5 μm, TSMC 350 nm and TSMC 180 nm. Test chip fabrication was sponsored by the MOSIS Educational Program (MEP). For AMIS 1.5 μm and TSMC 350 nm test chips, we used the pad libraries offer by MOSIS, while for the TSMC 180 nm test chip we developed our own pad library. For each test chip, we measure the functionality and performance of all critical modules of the BICS as well as characterized the performance of the BICS system as a whole. Based on the test chips experimental results, a discussion on the impact of technology on our BICS design concludes this section.

6.2 AMIS 1.5 μm Test Chip

The AMIS 1.5 μm test chip was our first test chip fabricated with the original BICS design. The objective of the test chip was to verify our design concept, correctness and explore possible improvements for more advanced technologies. It was fabricated using the MOSIS 1.5 μm AMIS double-polysilicon, double-metal process with a gate oxide thickness of 310 Å. The threshold voltage is 0.59 V and -0.97 V for NMOS and PMOS devices, respectively. The chip measures 2.2 mm by 2.2 mm and is packaged in a 40-pin ceramic dual-inline package (DIP). The chip layout is shown in Fig. 53. The usable chip

area is occupied by two full sensor systems as well as standalone system components, which enable us to test the functionality of each component of the sensor. Each sensor system contains 22-bit up and down counters, for a total of 922 transistors. A production sensor would use only one counter, reducing the transistor count to 534. The white circles in the figure indicate the reservoir capacitors, with larger reservoir capacitors (X16) designated with the large circle in Fig. 53. Several reservoir capacitor sizes are incorporated to facilitate the study of calibration drift vs. capacitor size. The test fixture is based on a Xilinx FPGA Spartan system board D2E-DIO2. The FPGA was carefully programmed to generate test signals and store output results. An HP 1653B logic analyzer and an oscilloscope were also used to observe the output. A 40 MHz clock frequency was used for all measurements. This is the maximum clock rate of this test fixture, limited by the FPGA clock rate. The chip was operated at 3.0 V to match the test fixture.

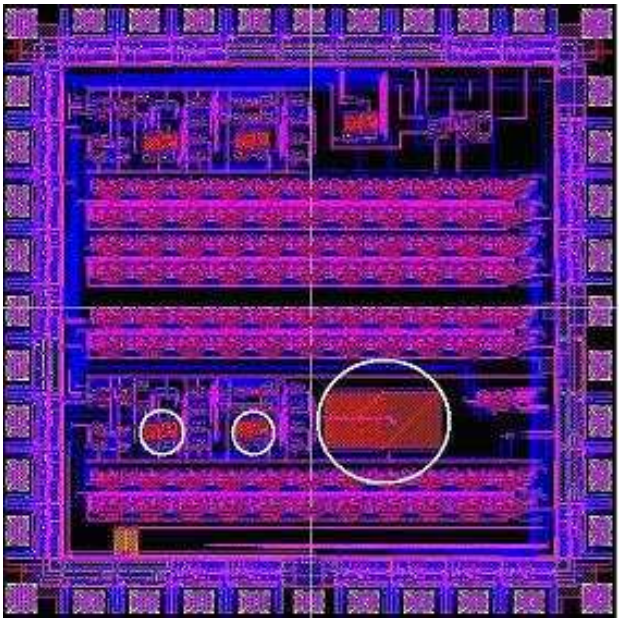

Fig. 53. Chip layout with reservoir capacitors circled.

The stochastic sensor transfer curve is shown in Fig. 54. The y-axis denotes the counter difference of the flip-flop decisions while the x-axis denotes the input voltage difference. We used 2^{20} repetitions for each measurement since this number will almost saturate the 22-bit counter. More repetitions would yield higher resolution, but takes longer test time. Longer test time may cause test accuracy to suffer due to calibration drift. Note the value of each point in the figure is an average of 10 measurements. Calibration is always performed before each measurement. As shown in Fig. 54, the stochastic behavior was observed. The gain of the sensor is approximately 800 counts/μV. Though calibration was done before each measurement, an offset of about 200 μV was observed, which is the result of a large calibration voltage step size, as discussed below. From the transfer curve, an effective noise level of about 800 μV can

be observed. This noise was found to be 4 times larger than our simulated noise level of 190 μV. Besides the internal noise, the external power supply was found to be the main source of noise. The supply noise is common mode in the calibration circuit and flip-flop, but is not completely cancelled, due to device mismatch. This chip did not implement digital chopping, which would cancel out this noise.

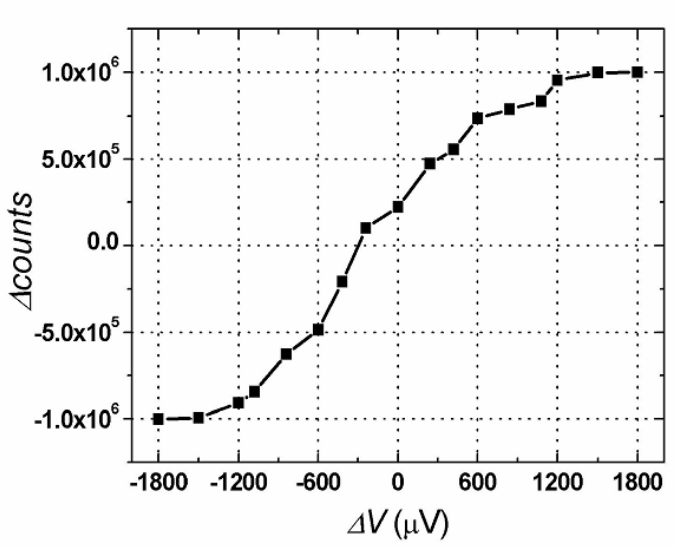

Fig. 54. Measured stochastic sensor transfer curve.

The average counter difference and standard deviation with respect to differential input voltage is listed in Table VI. The predicted sampling variance has been given in Eq. 5.1 in section 5.4.2 and the standard deviation (Eq. 5.2) is:

$$\sigma = [pq / N]^{\frac{1}{2}} \sim \frac{0.5}{\sqrt{N}} \qquad (6.1)$$

where N is the number of repetitions while p and q are the probability for either side of the stochastic sensor to get a "1", which is close to 0.5 in our intended I_{DDQ} test range. So for 2^{20} clock cycles, we have the ±σ in counts equal to ±512 counts. We also derived the probability for a "1" decision, which is given by (Eq. 5.5):

$$N \cdot p \sim N \cdot 0.5 \pm \frac{N \cdot s}{\sqrt{2\pi}} \tag{6.2}$$

where s is the signal to noise ratio. In our measurement $\frac{N \cdot s}{\sqrt{2\pi}}$ is equal to 800 counts/μV vs. one σ of ±500 counts. So the 3σ sampling noise is ±1500 counts/800 counts/μV, which is approximately ±1.9 μV. This is equivalent to a 19 μA I_{DDQ} 3σ resolution if 10 squares of 10 mΩ/□ metal are used for tapping the signal. The difference between two measurements has:

$$\Delta\mu = \mu_1 - \mu_2 \tag{6.3}$$

$$\text{and } \sigma_\Delta = \sqrt{\sigma_1^2 - \sigma_2^2} = \sqrt{2}\sigma \sim 9\mu A \tag{6.4}$$

so we end up with about 60% confidence interval for a 10 μA I_{DDQ} resolution. According to Table VI, the average standard deviation is 3076, which is about 6 times larger than the predicted variation of 512. Noise due to the large calibration step size is believed to cause this increased standard deviation.

TABLE VI. COUNTER AVERAGE AND STANDARD DEVIATION VS. INPUT VOLTAGE.

DeltaV(uV)	Average	σ
1800	1000000	0
1500	997933	2907
1200	953947	3224
1080	832050	4001
840	787326	3509
600	736727	2357
420	554643	3466
240	474376	2853
0	222930	3642
-240	100597	3198
-420	-208506	2487
-600	-485345	3414
-840	-627292	3795
-1080	-843434	5678
-1200	-908892	3760
-1500	-993616	4003
-1800	-1000000	0

Because of the older technology used and the chip area constraint, the size of the reservoir capacitor is limited and therefore the calibration pump ratio cannot achieve the targeted 1 μV calibration step size. For this design, the simulated ratio of pump capacitor to reservoir capacitor is close to 1 mV per step. This is about the same as the measured flip-flop mismatch of 1.2 mV. The measured average pump up and pump down step size was found to be 0.85 mV and 0.64 mV, respectively. The pump step size is a variable and depends on the reservoir capacitor voltage, in that it will approach 0 when the reservoir capacitor voltage is close to V_{DD} or GND. Although the step size is much larger than the intended resolution, the combined work of up and down pumps, or what we call the differential step, helps to calibrate the sensor in the metastable region. As illustrated in Fig. 54, the transfer curve shows an offset of 200 μV, which is the result of the calibration differential step, calibration drift during measurement and external power

supply noise. This chip did not implement digital chopping to remove the drift and external noise. This offset can easily be cancelled out by using the delta I_{DDQ} technique. This pump step size problem can be greatly alleviated using newer technology, since the minimum pump capacitance (junction capacitance) is drastically reduced compared to this older 1.5 μm technology.

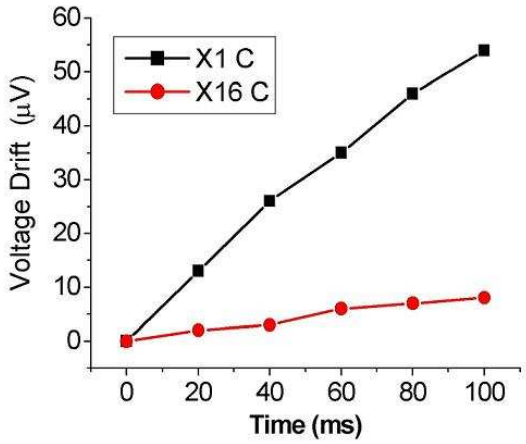

Fig. 55. Calibration circuit drift rate.

The measured drift rate of the calibration circuit is 12 μV per 20 ms, which is approximately an order of magnitude higher than the simulated results, as shown in Fig. 55. This is due to elevated subthreshold leakage, which is caused by a weak "0" generated from the FPGA test fixture. The drift rate is found to be significantly improved by increasing the size of the reservoir capacitor. With the reservoir capacitor size enlarged by 16 times, the drift rate drops to less than 2 μV per 20 ms. Therefore a

tradeoff must be made between the reservoir capacitor area and the desired drift rate. Digutal chopping was not implemented in this design, so this drift is present during measurement. At 40 MHz, the 2^{20} measurement cycles take 26.2 ms, so the drift is 2.6-15.7 μV during measurement. The gain of the calibration is about twice that of the supply line inputs, so this is equivalent to a drift of 5.2-31.4 μV during measurement. These values are much smaller than the calibration step size.

To summarize, the performance of the BICS and its components are characterized through a test chip fabricated with AMIS 1.5 μm technology. This sensor system is able to monitor the I_{DDQ} at a resolution level of 10 μA, but with a significant offset. Further work needs to be done to reduce the stochastic sensor internal/external noise to achieve targeted sensitivity. The calibration drift could become a problem due to elevated leakage in newer technology, although calibration step size becomes less of an issue. So for newer technology, we chose to pay more attention to the leakage related design issues in order to maintain the BICS effectiveness and accuracy.

6.3 TSMC 350 nm Test Chip

The second test chip was fabricated by MOSIS using TSMC 350 nm technology. The chip layout is shown in Fig. 56. The test chip includes a full sensor (with two 24-bit counters) and its variations. It also includes individual components. The lower portion of the test chip contains the MAGFET test structures discussed in Section 4. The standard 40-pin ceramic DIP was used for packaging. Under a low-density layout, a full sensor with two counters is 83,490 μm^2. Removing one counter reduces the area to 53,850 μm^2.

Shrinking the calibration capacitors and tightly packing the layout would reduce sensor area to 30,000 μm^2, permitting 33 sensors to use no more than 1% of a 1 cm^2 die.

Similar to the first test chip, the test fixture is based on a Xilinx FPGA Spartan system board D2E-DIO2. The FPGA was carefully programmed to generate test signals and store output results. An HP 1653B logic analyzer and an oscilloscope were also used to observe the output. A 40 MHz clock frequency was used for all measurements.

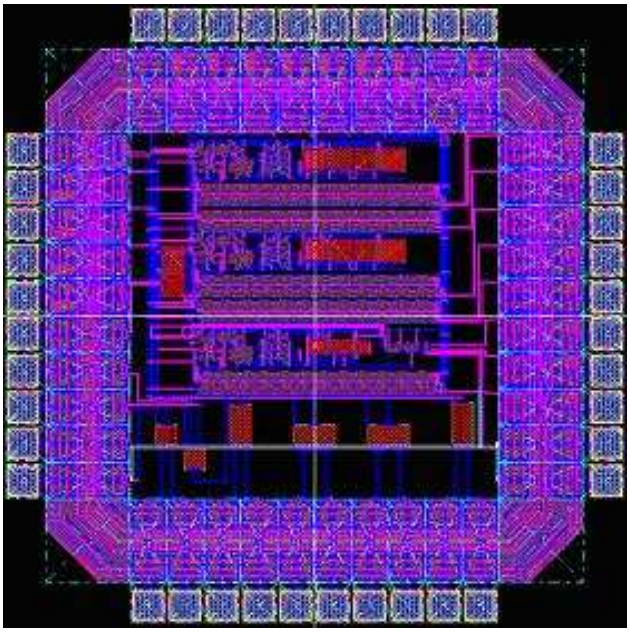

Fig. 56. TSMC 350 nm test chip layout.

6.3.1 Calibration Step Size and Drift Measurement

The standalone calibration circuit was measured to determine the calibration charge pump voltage step size and the calibration voltage drift rate. Measurements show a

calibration range from 330 mV to 2.03 V, compared to the simulated range of less than 0.7 V to 2.11 V. Since this range is primarily determined by transistor threshold voltages, and these are accurately characterized in the simulation models, there is good agreement between simulation and measurement.

As discussed earlier, the simulated calibration circuit pump up step size from simulation is 125 μV for the coarse phase and 4 μV for the fine tuning phase, and the average pump down step size is 31 μV. The two-phase characteristics of the pump up process were observed, with a measured coarse pump up step size of 232 μV and a fine tuning step size of 17 μV. The average pump down step size measured for the range 1.7 V down to 0.7 V was 87 μV. The measured step sizes are 2-4 times that of simulation.

The measured downward drift rate shown in Fig. 57 is 770 μV/10 ms, from an initial voltage of 1.9 V. This is twice the simulated value. A slightly lower drift rate was observed for an initial voltage close to $V_{DD}/2$.

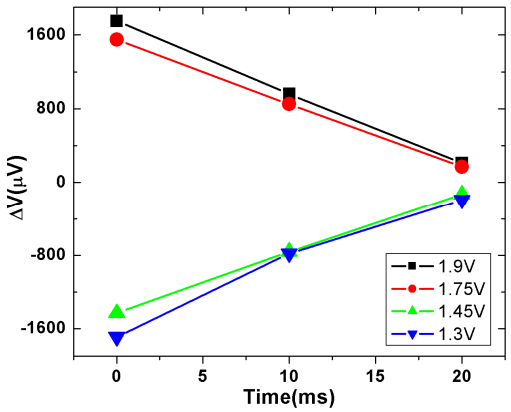

Fig. 57. Measured calibration drift rate with different initial conditions. The y-axis is the amount of drift.

The calibration node voltage was measured on the standalone calibration circuit through an unbuffered (analog) pad. This results in the capacitance and leakage of the package and test fixture being included in the measurement. The leakage of the instrument probe is small enough to neglect. The combined capacitance from the pad, package, socket and instrument probe is approximately 20 pF, or about equal to that of the calibration reservoir capacitance. This means that the actual on-chip step sizes and drift rates are double their measured values. Therefore, the measured step size is 4-8 times the simulated value and the drift rate is four times its simulated value. Since MOSIS does not characterize device models for leakage, a large leakage error is not surprising. However, the MOSIS device large signal and parasitic capacitance values are accurately characterized. Since the measured calibration range is close to the simulated range, this suggests that models of the stack and diode-connected transistors are accurate.

The only possible explanation for the large step size is a problem with the pumping transistor control. If the non-overlapping pump clocks do in fact slightly overlap, this would explain the larger step size. However, a careful analysis of the data detector circuit using back-annotated netlists with run-specific electrical characterization data indicates that it should work correctly. Another possible explanation is that V_{DD} and ground noise cause one pump transistor to turn partially on while the other is fully on. The pump transistors use normal V_{TH} devices. A glitch of 0.2-0.3 V on the supply lines (fed through the data detector to the pump transistor gates) could produce enough leakage to explain the observed pump step size. However, such glitches were not

observed on the supply lines at the package supply pins, and circuit power is low relative to supply impedance. Future designs will require a more robust pumping circuit.

6.3.2 Calibration Gain Measurement

The calibration gain was measured on the standalone flip-flop with external calibration voltages, using external counters to accumulate the results. The calibration gain was measured by shorting the flip-flop inputs to V_{DD} and slightly tweaking the calibration voltage. The calibration voltages used to balance the flip-flop were 1.907 V (on the "left" input) and 1.831 V (on the "right" input). The gain was then measured by manually adjusting the 1.907 V voltage up and down over a range of 10 mV with the other side fixed at 1.831 V and measuring the difference in up and down counter values. The results are shown in Fig. 58. The input voltage is the difference from the initial balance point. A total of 1M (2^{20}) measurement cycles were used for each measurement, and the measurement repeated ten times and averaged. Over the calibration voltage range of ±2000 μV the flip-flop response is approximately linear, and so was used to estimate the gain of 253 counts/μV. This is equivalent to a gain of 1012 counts/μV for 4M (2^{22}) measurement cycles.

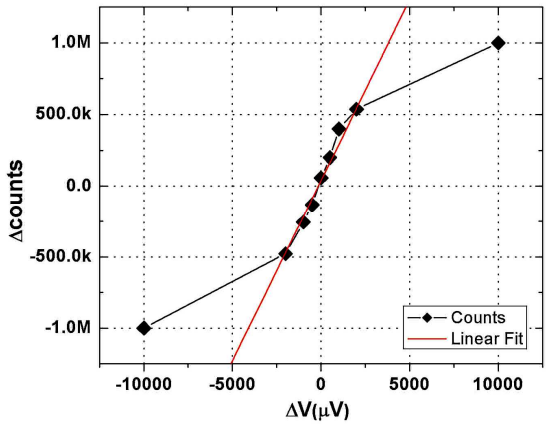

Fig. 58. Calibration voltage gain in terms of differential counter value vs. change in calibration voltage away from the flip-flop balance point. The flip-flop inputs were shorted to V_{DD}, and a total of 1M (2^{20}) measurement cycles were used for each measurement.

6.3.3 Flip-Flop Mismatch and Gain Measurements

The standalone flip-flop was measured to determine its mismatch and gain. The flip-flop was designed with a common centroid layout and dummy transistors in order to minimize mismatch. Given the layout techniques used and transistor geometries, the primary source of mismatch is variation in transistor threshold voltages. The external calibration voltages were manually adjusted until the up and down counter values were approximately equal. The limited resolution of the manual adjustment left a small amount of offset. Since the two calibration voltages are independent, there are no unique calibration values. A set of values above and below $V_{DD}/2$ were used, as shown in Table VII. The flip-flop mismatch ranged from 30 mV to 150 mV, depending on the operating point of the calibration transistors. In the triode region, the mismatch compensation voltage was small due to the higher calibration device resistance. Note that in the self-

calibration circuit one calibration voltage pumps up while the other pumps down, so the actual calibration voltage will be around $V_{DD}/2$, which suggests an expected nominal calibration voltage difference of about 50 mV for this particular flip-flop.

TABLE VII. MISMATCH COMPENSATION UNDER DIFFERENT CALIBRATION VOLTAGES.

Left (V)	2.524	2.171	1.939	1.673	1.211
Right (V)	2.374	2.079	1.856	1.621	1.181
Delta (mV)	150	92	83	52	30

The standalone flip-flop gain was measured by balancing the flip-flop at the three different calibration voltages, and measuring the gain curve for each of them for 4M (2^{22}) measurement cycles. The gain curve is the plot of counter difference vs. differential input voltage. Ten measurements were averaged for each input voltage. The results are shown in Fig. 59 and Table VIII. The flip-flop gain is slightly influenced by the calibration voltage. Increasing calibration voltage resulted in slightly lower gain, due to device operating points moving to a higher noise region. The highest gain of approximately 600 counts/μV is attained at the calibration voltage pair of 1.62 V/1.67 V, the pair closest to $V_{DD}/2$. Based on the gain curve, the estimated input-referred RMS voltage noise level is 1.5 mV, compared to the simulated value of 1.2 mV. The simulated value was measured as a steady-state value with the flip-flop operating point forced to the metastable point, and the real flip-flop devices transition between different operating regions, so this is good agreement between simulation and measurement.

TABLE VIII. FLIP-FLOP GAIN FOR DIFFERENT CALIBRATION BIAS.

Input (μV)	Calb A (1.62/1.67)	σ	Calb B (1.93/2.06)	σ	Calb C (2.53/2.37)	σ
420	234822	3951	280196	4712	340628	3919
210	82138	4742	110704	4006	151768	4503
0	13166	3387	8798	3719	-7062	4154
-210	-83144	3509	-105172	4121	-171298	4321
-420	-208198	3592	-307908	3997	-279760	4681

The flip-flop input gain of about 600 counts/μV for 4M cycles compares to a calibration gain of 1012 counts/μV. The calibration gain is 70% higher than the input gain because the calibration transistors have a longer channel length, and are at the bottom of the transistor stack. When the flip-flop is making a decision, both the input and calibration transistors operate in the linear region. The longer channel length of the calibration transistors means that they produce a larger resistance change per input voltage change than the input transistors, having a larger impact on flip-flop balance.

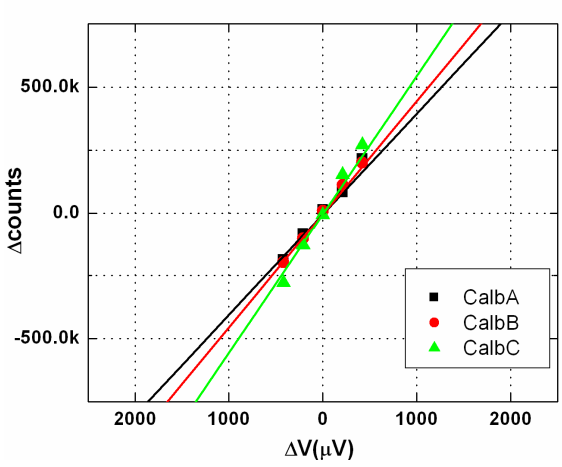

Fig. 59. Standalone flip-flop gain under different calibration bias.

6.3.4 I_{DDQ} Sensor System Measurements

The entire sensor system was measured. The input signal is taken from taps at two different locations 100 squares apart on a metal reference wire that emulates a V_{DD} line with a sheet resistance is 70 mΩ/□. So the sensing resistor is 7 Ω. This value is much larger than the expected production value of 100 mΩ in order to permit high resolution measurements.

Due to the leakage of the 350 nm technology, it is not possible to measure the BICS transfer curve without using digital chopping. The curve shown in Fig. 60 shows the difference in up and down counter values vs. sensor differential input voltage (set by adjusting the voltage on the reference wire). The curve was obtained using 4M measurement cycles at 40 MHz, with each measurement period of 500 measurement cycles following each calibration period of 200 calibration cycles. (This is referred to as Mode B below). The appropriate number of calibration and measurement periods are interleaved to achieve the desired total number of measurement cycles, with the last measurement period being truncated as necessary. The corresponding data is listed in Table IX. Each point on the transfer curve is the average of 10 measurements. An effective input-referred RMS voltage noise level of 5 mV can be observed from the transfer curve. This suggests that self-calibration and the surrounding clocked circuitry (data detector, counter) add an additional 3.5 mV of noise.

A linear fitting around the origin indicates a sensor gain of 450 counts/μV, compared to 600 counts/μV in the standalone flip-flop. This difference is due to the different effective noise levels. The counter offset for a 0 V input corresponds to an input voltage

offset of -194.4 μV.

Sampling theory predicts that the one-σ sampling noise (in terms of counter difference) for 4M measurement cycles should be 2048. The measured σ is about 3 times this value, and outside the 95% confidence range for ten samples when one considers that all samples are higher than predicted.

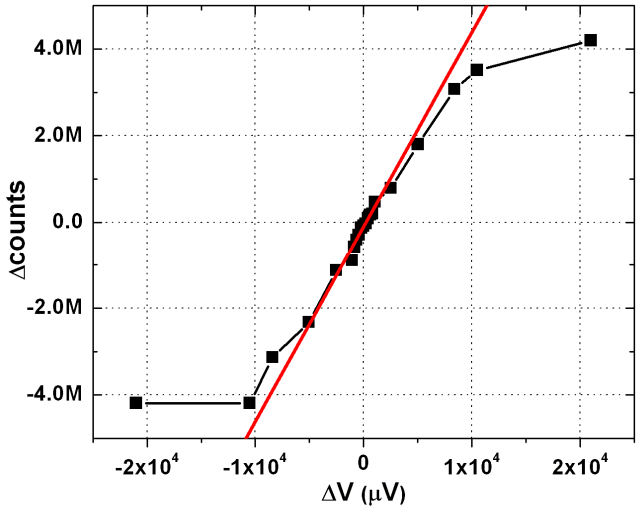

Fig. 60. BICS transfer curve using 4M measurement cycles, with 200 calibration cycles interleaved with 500 measurement cycles per period (mode B).

A possible explanation for the excess noise is a calibration sampling effect. As discussed above, the gain of the calibration circuit is approximately 1012 counts/μV of calibration voltage, so the observed σ of about 6000 is approximately the same as a variation in average differential calibration voltage of 6 μV between measurements. If 4M measurements are performed with 500 measurement cycles per measurement period,

then there are 8388 calibration periods. The measurement cycles that follow a calibration period use the last calibration voltage throughout the measurement period, so only 8388 calibration voltage samples are used. The 95% confidence interval for 8388 samples is approximately ±1%. The measured differential step size ranges from 208 to 638 μV (accounting for the test fixture capacitance). A 1% variation about these values would explain the extra observed measurement variation. This was evaluated with further experiments.

TABLE IX. COUNTER DIFFERENCE AND STANDARD DEVIATION UNDER DIFFERENT MEASUREMENT MODES.

	Mode A		Mode B		Mode C	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ
21000	4.19E+6	0	4.19E+6	0	4.19E+6	0
10500	3.78E+6	7197	3.51E+6	6037	3.31E+6	8117
8400	3.31E+6	7562	3.07E+6	7332	2.77E+6	6090
5040	2.58E+6	6680	1.80E+6	6983	1.60E+6	6744
2520	1.39E+6	6911	7.90E+5	8129	979831	6938
1050	984486	9039	4.69E+5	6638	399078	7551
840	739154	8768	1.91E+5	7663	221070	7109
630	693340	5983	1.72E+5	8902	112453	8290
420	532473	6412	8.83E+4	7709	68303	7886
210	438343	7702	-3.58E+4	7006	45849	8366
0	217564	8751	-8.75E+4	5192	-17989	6334
-210	105930	8003	-1.34E+5	11208	-53890	7420
-420	94268	7610	-2.97E+5	9132	-137392	8637
-630	-18755	7149	-4.11E+5	6990	-311322	5275
-840	-73421	9785	-5.76E+5	7633	-445530	5993
-1050	-296011	6907	-8.98E+5	8991	-617672	8418
-2520	-716608	7759	-1.13E+6	7834	-1.23E+6	7525
-5040	-1.71E+6	8460	-2.33E+6	10033	-2.11E+6	9021
-8400	-2.56E+6	10715	-3.13E+6	6132	-3.34E+6	8792
-10500	-3.39E+6	11561	-4.19E+6	0	-3.98E+6	10056
-21000	-4.19E+6	0	-4.19E+6	0	-4.19E+6	0

The sensor behavior for different number of calibration cycles per calibration period was evaluated. We define modes A, B and C for 100, 200 and 1000 calibration cycles respectively, interleaved with 500 measurement cycles, and a total of 4M measurement cycles. The results are shown in Fig. 61 and Table IX. Ten samples are taken for each input value for each mode. Mode C has the lowest offset and slightly higher gain than mode B. Mode A has poor offset and similar gain to mode B. The offset of modes A and B may be due to the initial calibration period, in which 100-200 cycles may not be enough to bring the flip-flop into initial calibration. Behavioral simulation indicates that initial calibration can take as long as 500 cycles. The variation in gain between the modes is within the 95% confidence interval, so any gain sensitivity to number of calibration cycles per period is small.

Behavioral simulation of the self-calibration process using Microsoft Excel was performed with the full range of measured calibration voltage step sizes and measured calibration gain. These simulations and an analytical model suggest that more calibration cycles per calibration period may increase the variance of the ending calibration voltage per period, effectively introducing noise and lowering gain. These simulations produce an effective calibration voltage RMS noise level of 0.6-1.2 mV and an input-referred noise level of 1-2 mV. This is well short of the measured noise that cannot be explained by measurement sampling. In addition, the predicted dependence on the number of calibration cycles per period does not match the data in Table IX. The simulation assumes equal up and down pump step sizes, and a linear flip-flop gain curve, which may explain its inaccuracy. The data for the 180 nm test chip below shows that some of

the variance is because the initial startup calibration period used here is too short.

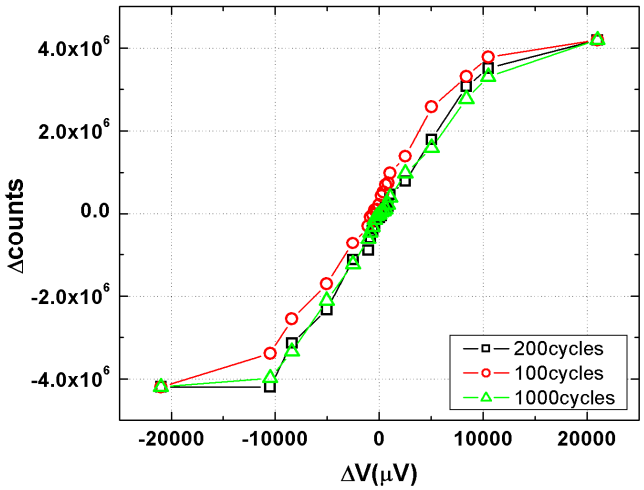

Fig. 61. Comparison of three chopping modes with 100, 200 and 1000 calibration cycles, respectively. A total of 4M measurement cycles were used, with 500 measurement cycles per measurement period.

The behavioral simulation and sampling theory predict that using more calibration periods should reduce calibration sampling noise. Sampling theory also predicts that using more measurement cycles should reduce measurement sampling noise. Both the number of calibration periods and the number of measurement cycles can be increased by increasing the total number of measurement cycles while keeping the number of measurement cycles and calibration cycles per period fixed. This experiment was performed using 500 cycles per measurement period and 200 cycles per calibration period, with the total number of measurement cycles varying from 128K to 4M. The results are shown in Table X. The relative σ of the counter differences increases by 4.33X for a 32X decrease in the number of measurement cycles. Sampling theory

predicts a relative σ increase of 5.66x (√32). Given that σ is computed with ten samples, the difference between measurement and theory is within the 95% confidence interval. We can conclude that the counter behavior largely follows sampling theory, with calibration period sampling increasing the total σ by 30-50% over the measurement sampling alone. This indicates that the flip-flop is primarily affected by internal white noise and calibration noise that effectively acts as white noise.

TABLE X. COUNTER DIFFERENCE AND STD. DEV. FOR DIFFERENT TOTAL MEASUREMENT CYCLES. ALL DATA WAS COLLECTED WITH 200 CALIBRATION CYCLES INTERLEAVED WITH 500 MEASUREMENT CYCLES. TEN MEASUREMENTS WERE TAKEN FOR EACH VALUE.

	2^{17} Cycles		2^{19} Cycles		2^{21} Cycles		2^{22} Cycles	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ	ΔCount	σ
21000	131072	0	524288	0	2097152	0	4194300	0
10500	87139	639	476721	2325	1978751	4138	3511290	6037
5040	59301	904	229850	1728	1151406	3904	1798770	6983
1050	28641	921	90675	1514	290116	3774	469078	6638
630	23057	776	49188	1874	67115	4133	172453	8902
210	15902	853	13213	2007	9983	4017	-35849	7006
0	5315	752	3329	1644	-13071	4318	-87453	5192
-210	2385	694	-9789	1779	-53379	3692	-133890	11208
-630	-1438	813	-33080	1940	-133904	3869	-411322	6990
-1050	-9309	665	-87821	2021	-377683	3743	-898422	8991
-5040	-41033	840	-264487	1867	-1279213	4212	-2327600	10033
-10500	-76706	798	-407209	1993	-1807152	4635	-4194300	0
-21000	-112303	1103	-524288	0	-2097152	0	-4194300	0
Average		813		1881		4039		5998

In order to compare the gain as a function of number of total measurement cycles, all measurements were scaled to 4M cycles, as shown in Table XI, and drawn together in Fig. 62. As can be seen, the flip-flop gain is relatively independent of the number of

measurement cycles. This matches sampling theory. The exception is 128K cycles, which has lower gain and higher offset. But the size of the confidence interval makes it difficult to conclude that the 128K experiment has significantly different behavior. The data further indicates that the flip-flop internal white noise is relatively independent of the number of measurement cycles and calibration periods. As discussed above, this does not match the simple simulation and analytical model that was developed to describe calibration behavior.

TABLE XI. SCALED COUNTER DIFFERENCES.

ΔV (μV)	128K	512K	2M	4M
21000	4194304	4194304	4194304	4194300
10500	2788448	3813768	3957502	3511290
5040	1897632	1838800	2302812	1798770
1050	916512	725400	580232	469078
630	737824	393504	134230	172453
210	508864	105704	19966	-35849
0	170080	26632	-26142	-87453
-210	76320	-78312	-106758	-133890
-630	-46016	-264640	-267808	-411322
-1050	-297888	-702568	-755366	-898422
-5040	-1313056	-2115896	-2558426	-2327600
-10500	-2454592	-3257672	-3614304	-4194300
-21000	-3593696	-4194304	-4194304	-4194300

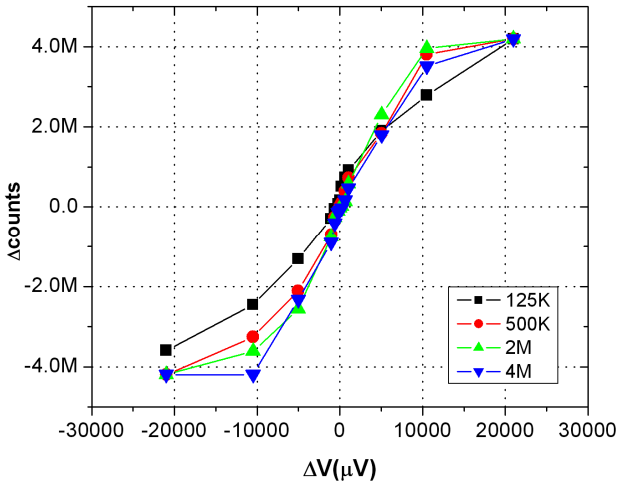

Fig. 62. Flip-flop transfer curves for different total measurement cycles, normalized to 4M counts.

The length of the measurement period was varied, for a calibration period of 200 cycles and 4M total measurement cycles. The measurement period ranged from 50 to 500 cycles. This varies the number of calibration periods from 8388 to 83866. Sampling theory says that more calibration periods should reduce calibration noise and effectively increase sensor gain and reduce offset. The results are shown in Table XII and Fig. 63. The results indicate that there is only a very slight improvement in gain and variation by using fewer measurements per measurement period while keeping the total number of measurement cycles fixed. For 50 measurements per period, the gain was 659 counts/μV, compared to a gain of 650 counts/μV for 500 measurements per period. These differences are within the confidence interval of the measurements. The gain figures here are higher than those listed previously due to considering gain only near the origin. The results suggest that more calibration periods will not significantly reduce the

effective calibration noise. The data shows that more calibration periods does significantly reduce the offset.

TABLE XII. COUNTER DIFFERENCE AND STD. DEV. WITH DIFFERENT MEASUREMENT CYCLES PER MEASUREMENT PERIOD FOR 4M TOTAL MEASUREMENT CYCLES AND 200 CALIBRATION CYCLES PER CALIBRATION PERIOD.

	50		100		200		500	
ΔV (μV)	ΔCount	σ	ΔCount	σ	ΔCount	σ	ΔCount	σ
1050	635728	6926	518843	6522	672950	8122	469078	6638
840	366719	5874	330309	7481	397520	5713	191070	7663
630	247467	5638	172453	7931	210903	7090	172453	8902
420	69055	7110	71828	8005	114663	7509	88303	7709
210	33760	6865	21083	6592	70035	7336	-35849	7006
0	-18862	6397	-37453	6935	-33649	6596	-87453	5192
-210	-119438	7008	-83890	7120	-99806	6983	-133890	11208
-420	-183792	7041	-217392	7437	-197665	6837	-297392	9132
-630	-359081	6659	-391322	7589	-351322	8285	-411322	6990
-840	-472306	6347	-577012	8226	-466211	9014	-575530	7633
-1050	-749564	6582	-856641	7852	-703034	8998	-898422	8991

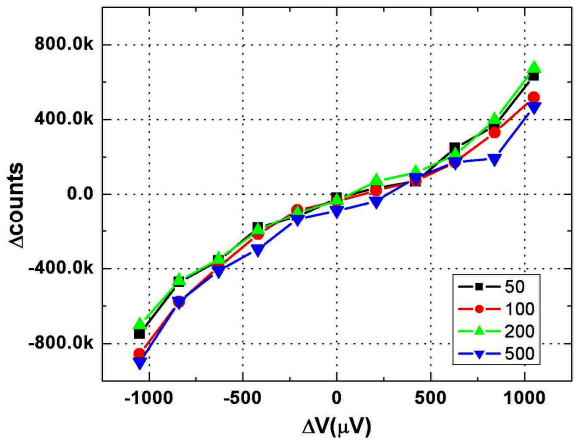

Fig. 63. Flip-flop transfer curve for different number of measurement cycles per measurement period, for 4M total measurement cycles. Fewer cycles per measurement period means more calibration periods. 200 calibration cycles were used per calibration period.

6.3.5 Conclusions

A 350 nm test chip was fabricated and tested. Based on the measured results, the overall optimal performance of the BICS can be summarized as follows:

- Gain – 659 counts/μV for 4M measurement cycles with 50 cycles per measurement period and 200 cycles per calibration period.
- Offset – -18,862 counts or the equivalent of 28.6 μV. This corresponds to 286 μA if sensing a 100 mΩ resistor. This offset is not important if using a self-scaling testing approach such as ΔI_{DDQ}. In applications where a lower offset is required, a smaller number of measurement cycles per measurement period can be used.
- Resolution – The two-σ variation in measurement values is approximately 12,000 counts. This is the equivalent of 18.2 μV or 182 μA if sensing a 100 mΩ resistor. This corresponds to 0.4% of the dynamic range.
- Dynamic Range – The BICS is fairly linear over the input range of ±5 mV, or 50 mA. A larger range can be obtained by sensing a smaller resistance.
- Measurement Time – The test fixture limited the measurement clock to 40 MHz, even though in simulation the BICS can operate at several hundred megahertz. Using 50 measurement and 200 calibration cycles per period and 4M total measurement cycles takes 524 ms. Using 500 measurement and 200 calibration cycles per period and 1M total cycles slightly reduces the measurement resolution, but reduces the measurement time to 36.7 ms. Clocking the sensor at 400 MHz (e.g. using a locally generated clock) would

reduce measurement time to 3.7 ms.

- Power Dissipation – The test chip structure did not permit measurement of an individual BICS, but the total power dissipation is small. During measurement the dissipation is equivalent to three flip-flops and a dozen gates switching each clock cycle. During calibration the dissipation is half of this. During scan the power is similar to scan chains of the same size.

The experimental results indicate three primary areas for further sensor improvement. The first is the high flip-flop noise level, due to its high bandwidth. If the flip-flop cannot be clocked at higher speed, it can be loaded to reduce its corner frequency to about 100 MHz. This will reduce noise by 13x, with a corresponding increase in sensor resolution or reduction in measurement time. The second area is the low flip-flop input gain, which can be increased significantly by using a differential preamplifier. This should provide a corresponding increase in resolution. The third area to improve is the calibration step size, since this would reduce the number of calibration periods required and reduce the calibration noise. The challenge is achieving a small step size without increasing the calibration capacitor size. A new 180 nm test chip incorporating these improvements was fabricated.

6.4 TSMC 180 nm Test Chip

As discussed in the previous two sections, our BICS design has been experimentally validated by two test chips of different technologies. The data gathered in those two test chips also indicates where improvement can be made for this new test chip. As leakage

becomes more and more an important issue for advanced technologies, the key improvements for this test chip are focused on leakage control in the calibration circuit. The calibration circuits are implemented using thick gate oxide (or high threshold voltage) transistors, while the remainder of the design uses regular devices.

6.4.1 Test Chip Architecture

Like previous test chips, this test chip consists of a full sensor system and several variations. In addition the important standalone sensor components, i.e. the flip-flop sensor, counter/scan chain, and calibration circuit, are also included for analysis of the performance of each individual component. The fabricated test chip floor plan is shown in Fig. 64.

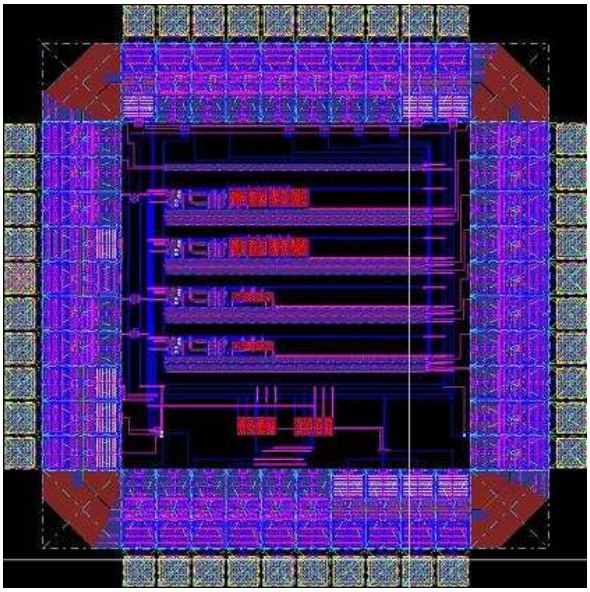

Fig. 64. TSMC 180 nm test chip layout.

Unlike previous test chips, there are no pad libraries available to us for this technology. So we have designed our own custom pad library for this test chip. A total of 5 different pads are developed: Pad-In, Pad-Out, Pad-Ref, Pad-VDD and Pad-GND. These pads operate at 3.3 V, while the core operates at 1.8 V. The die size is approximately 1800 μm by 2200 μm. The standard 40-pin ceramic DIP was used for packaging. Under a low-density layout, a full sensor with two counters is 52,125 μm^2. Removing one counter reduces the area to 33,125 μm^2. Shrinking the calibration capacitors and tightly packing the layout would reduce sensor area to 19,000 μm^2, permitting 52 sensors to use no more than 1% of a 1 cm^2 die. Compared with 350 nm technology, the smaller minimum feature size allows for an increase of 57% in terms of total number of BICSs.

For this technology the gate oxide thickness is 41 Å. The threshold voltages for NMOS and PMOS devices are 0.51 V and -0.52 V, respectively. Similar to the previous test chips, the test fixture is based on a Xilinx FPGA Spartan system board D2E-DIO2. The FPGA was carefully programmed to generate test signals and store output results. An HP 1653B logic analyzer and an oscilloscope were also used to observe the output. A 40 MHz clock frequency was used for all measurements.

6.4.2 Calibration Circuit Measurement

Four different calibration circuits have been implemented with a combination of regular devices and high threshold voltage devices, with different sizing. The details are listed in Table XIII.

TABLE XIII. FOUR CALIBRATION CIRCUITS.

	C1	C2	C3	C4
Regular Device	-	-	Yes	Yes
High V_{TH}	Yes	Yes	-	-
Regular sizing (50 μm × 50 μm)	Yes	-	Yes	-
4X Sizing (200 μm × 200 μm)	-	Yes	-	Yes

The measurement of the step size and drift rate of the 4 different calibration circuits are listed in Table XIV. Calibration circuit C1 (with high V_{TH} devices and reservoir capacitor size of 50 μm by 50 μm) is standard for our BICS and used as the baseline for comparison of the other 3 variations. It was found the drift rate for C1 is slightly better than that of the 350 nm test chip. This improvement can be attributed to the use of high threshold voltage transistors, which significantly reduce subthreshold leakage. As far as the step size and drift rate are concerned, the C2 type calibration circuits achieve the best performance because the reservoir capacitor is 4 times larger and the high threshold voltage devices are used. However, the larger reservoir capacitor size increases the overall sensor system area. The calibration circuits realized with regular devices (C3, C4) have considerably higher drift rate due to the elevated leakage for this technology, although their step size is comparable to C1 and C2. In theory, a smaller step size is expected for C3 and C4 because regular devices (with thinner gate oxide and high unit area capacitance) coupled with the minimal feature size should yield a better pump ratio. However, the advantages are canceled by the increased leakage. All step size are measured at approximately $V_{DD}/2$.

TABLE XIV. DRIFT RATE AND STEP SIZE OF FOUR CALIBRATION CIRCUITS.

	C1	C2	C3	C4
Downward Drift (from 1.1 V)	630 μV/10 ms	277 μV/10 ms	9.11 mV/10 ms	3.39 mV/10 ms
Upward Drift (from 0.7 V)	210 μV/10 ms	95 μV/10 ms	3.73 mV/10 ms	1.44 mV/10 ms
Step Size (pump up)	84 μV	39 μV	89 μV	41 μV
Step Size (pump down)	47 μV	24 μV	39 μV	31 μV

The measured calibration range is approximately 0.67-1.21 V. This range is narrower than the previous test chips because of the 1.8 V supply voltage. However, the range is still wide enough to calibrate typical flip-flop mismatch.

TABLE XV. MISMATCH MEASUREMENT OF FLIP-FLOP CIRCUIT.

Left (V)	1.113	1.005	0.913
Right (V)	1.049	0.943	0.876
Delta (mV)	64	62	37

6.4.3 Standalone Flip-Flop Circuit Measurement

Similar to the 350 nm test chip, the flip-flop mismatch measurement is conducted by feeding a pair of differential voltages to the gates of the two calibration transistors and manually forcing the flip-flop to operate in the metastable region. As seen in Table XV, the measured mismatch is 37 mV at approximately $V_{DD}/2$, or approximately 3%

mismatch.

TABLE XVI. STANDALONE FLIP-FLOP GAIN MEASUREMENT.

deltaV	counts	sigma
1920	1000000	0
1200	970443	887
720	857291	1110
480	578130	1381
360	437600	1353
240	270477	1022
120	134926	1567
0	43221	1564
-120	-109026	1301
-240	-209443	1087
-360	-421708	1430
-480	-596818	1375
-720	-803025	1101
-1200	-985300	1002
-1920	-1000000	0

The standalone flip-flop gain is measured with calibration fixed at 0.913V (left) and 0.876V (right). The results are shown in Table XVI and Fig. 65. Each data point is the average of 10 measurements, with 1M (2^{20}) measurement cycles. The curve fitting indicates that the new flip-flop design yields better gain, which is approximately 1270 counts/μV. The measured flip-flop input-referred RMS noise is approximately 450 μV, as opposed to the simulated value of 377 μV RMS (noise band from 40 MHz to cut off at 2.1 GHz). The good agreement between simulation and measurement indicates that the MOSFET white noise models are accurate for this technology.

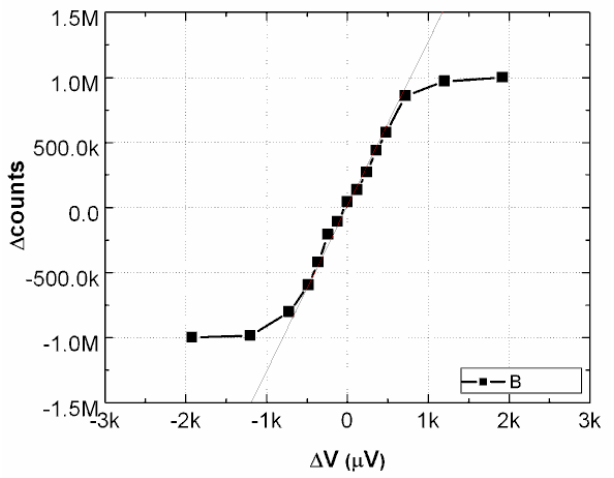

Fig. 65. Standalone flip-flop gain measurement.

6.4.4 BICS Sensor System Measurement

Based on the data analysis of the 350 nm test chip and this 180 nm test chip and experimenting with digital chopping periods, we found that optimal measurement results are obtained under certain restricted conditions. First, there should be enough initial calibration cycles to allow the sensor to achieve steady state calibration. Second, the number of measurement cycles during each measurement period should not be too large and the recalibration cycles should only be ample enough to bring the flip-flop back to the balanced state. Based on hand estimates, we choose 10,000 cycles for the initial calibration and use 200 calibration cycles interleaved with 200 measurement cycles for the digital chopping operation that follows the initial calibration. The sensor gain measurement is shown in Table XVII and Fig. 66. Each point is the average of 20 measurements. For each measurement a total of 4M measurement cycles were collected. In the previous test chip, each measurement was performed, the results recorded by

hand, and then the next measurement performed. In this work the measurements are performed back-to-back, with results stored in FPGA memory for later readout.

TABLE XVII. SENSOR GAIN MEASUREMENT.

deltaV	counts	sigma
9600	4.19E+06	0
6000	3.98E+06	2055
3360	2.77E+06	2732
1800	1.59E+06	2919
1200	9.10E+05	2640
720	7.01E+05	2862
480	4.27E+05	2513
360	3.60E+05	3066
240	2.44E+05	2526
120	9.87E+04	2632
0	2.03E+03	537
-120	-1.09E+05	2880
-240	-2.74E+05	2940
-360	-3.51E+05	2660
-480	-4.27E+05	2922
-720	-7.41E+05	2830
-1200	-9.95E+05	2904
-1800	-1.27E+06	2849
-3360	-2.56E+06	2851
-6000	-3.87E+06	2447
-9600	-4.19E+06	0

Sensor gain is obtained by performing a linear fit of the center region of Fig. 66. The sensor gain is approximately 973 counts/μV with an offset of 2.11 μV at 0 V input. Both figures are significantly better than the previous test chips. The offset can be explained by the limited number of calibration periods combined with the calibration step size. The input-referred noise level is approximately 3.5 mV, which means that approximately 3

mV of noise must come from other sources. This extra noise level is similar to that of the 350 nm test chip. One possible source is high frequency supply noise coupled to the calibration nodes through V_{DD} from other sensors clocked slightly out of phase with the one being measured. Since the calibration nodes have half the gain of the input nodes, 6 mV of equivalent differential noise on the calibration nodes would explain the measurements. The noise would be common mode, but the 3% flip-flop mismatch would turn 200 mV of common mode variation into 6 mV of differential variation. Due to the capacitive division of the storage capacitors, 400 mV of supply noise would be required to produce the 3 mV of equivalent input-referred noise. Measured supply noise is much lower than this, so this provides only a partial explanation. Another possible explanation may be that the different up and down calibration step sizes lead to oscillations in the calibration voltage that are not averaged out. But a definitive explanation has not been determined.

The average σ is 2619, which is much lower than the previous test chips, but still above the theoretical value of 2048. This could indicate that an even lengthier initial calibration period is required. The 2σ resolution of the sensor is then 2619*2/973=5.39 μV, which translates to 53.9 μA resolution when sensing a 100 mΩ section of power line. Note that the 21.1 μA offset is less than the resolution.

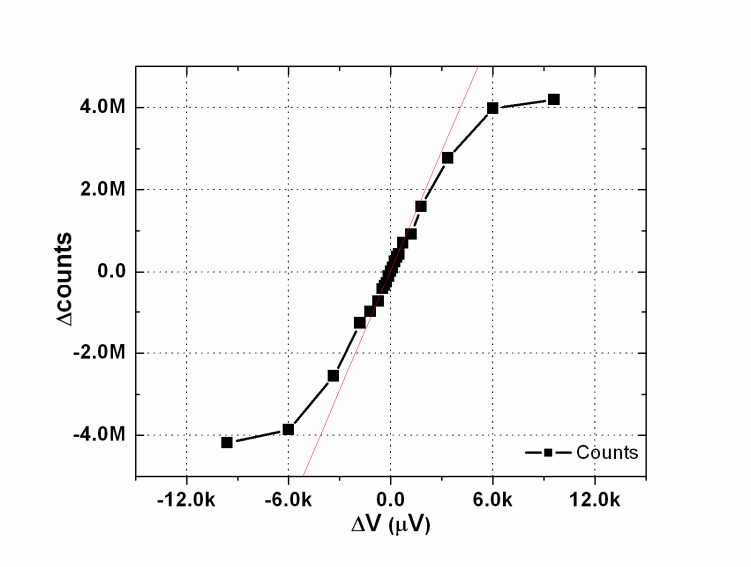

Fig. 66. Sensor gain measurement.

6.4.5 Conclusions

A 180 nm test chip was fabricated and tested. We noticed an overall performance improvement for this test chip compared to the 350 nm test chip, owing to several design improvements, including high threshold voltage devices for leakage sensitive circuitry and a new low noise flip-flop. Based on the measured results, the overall performance of the BICS can be summarized as follows:

- Gain – 973 counts/μV for 4M measurement cycles with 200 cycles per measurement period and 200 cycles per calibration period.
- Offset – 2030 counts or the equivalent of 2.11 μV. This corresponds to 21.1 μA if sensing a 100 mΩ resistor. This reduced offset is attributed to the smaller step size of the calibration circuit and the 10,000 initial calibration cycles. This offset is negligible and can be canceled out by using a self-scaling

testing approach such as ΔI_{DDQ}.

- Resolution – The two-σ variation in measurement values is approximately 5238 counts. This is the equivalent of 5.39 μV or 53.9 μA if sensing a 100 mΩ resistor. This is higher than our design goal, but still permits detection of most I_{DDQ} defects in 180 nm chips.
- Dynamic Range – The BICS is fairly linear over the input range of ±3.5 mV, or 35 mA. A larger range can be obtained by sensing a smaller resistance, at the expense of resolution.
- Area Overhead – Tightly packed the layout and using 6 metal layers for routing (instead of only two layers) would reduce sensor area to 19,000 μm^2, permitting 52 sensors to use no more than 1% of a 1 cm^2 die. This is enough sensors to handle the leakage of most chips fabricated in 180 nm technology. Sensor size can be further reduced with more advanced technologies.
- Measurement Time – The test fixture limited the measurement clock to 40 MHz, even though in simulation the 350 nm and 180 nm BICSs can operate at several hundred megahertz. In practical use, if the sensor is clocked at 400 MHz and using 500 measurement and 200 calibration cycles per period and collect 1M samples, the measurement time will be reduced to 3.7 ms. This does not meet our design goal, but is very competitive with current ATE solutions.
- Power Dissipation – As explained in the 350 nm test chip, the total power dissipation was not measured, but is small. During measurement mode the

dissipation is equivalent to three flip-flops and a dozen gates switching each clock cycle. During calibration the dissipation is half of this. During scan the power is similar to scan chains of the same size. When inactive, the sensor only dissipates leakage power.

7. CONCLUSIONS AND FUTURE WORK

7.1 Summary

This research has primarily focused on developing a practical built-in current sensor for I_{DDQ} test. The ultimate goal is to extend I_{DDQ} test to future technologies by moving I_{DDQ} test from a currently external test to an internal test, which is realized with built-in current sensors. To achieve this goal, the built-in current sensor solution is two-fold. First, it should be able to handle the challenge from high leakage advanced technologies and also achieve reasonable I_{DDQ} resolution. Second, the cost for implementing this approach must be low enough to be acceptable, which is 1% of chip area based on industry input. In this research, every effort has been made to accomplish the two objectives. A number of different sensor design alternatives were evaluated and the sensor circuit and layout design were carefully performed to achieve maximum performance at least cost. A series of test chips have been fabricated to validate our design. The test chips also helped us to optimize the sensor design, in particularly reducing noise sources. To summarize, our novel I_{DDQ} built-in current sensor has the following characteristics:

- Our BICS achieves an I_{DDQ} resolution of 53.9 μA (based on the 180 nm test chip), which is close to our goal of 10 μA. This resolution is higher than any other BICS approach that does not cause chip performance degradation.
- The BICS is able to measure I_{DDQ} level and direction. The ability to measure I_{DDQ} value instead of just pass/fail is the most important feature that other

approaches lack. In addition, the capability of measuring I_{DDQ} value will assist in spatial analysis of wafer test data.

- The BICS is capable of a test speed of 3.7 ms/vector, which is very competitive when compared with other I_{DDQ} test techniques, and faster than most of them.
- The BICS causes no CUT performance degradation. The BICS utilizes the voltage drop of existing power lines, and introduces no series impedance into the power grid. Most BICS designs cause performance degradation. In addition, the BICS can be completely powered off when testing is completed.
- The BICS is implemented in a purely digital logic process so it has no special technology requirements. This is in contrast to most BICS designs.
- The BICS area is less than 1% of total chip area. Our 180 nm test chip indicates that 52 BICS sensors can be inserted into a 1 cm^2 die without exceeding 1% area overhead.
- The BICS has the potential to be expanded to execute simple I_{DDX} algorithms with an on-chip controller, in which delta I_{DDQ}, current ratios, min/max I_{DDQ}, current signature can be calculated. This significantly reduces ATE requirements.
- The BICS can also facilitate defect localization through its partitioning of the supply grid.

As discussed above, the experimental results show that most of our objectives have been met. This corroborates our claim that our I_{DDQ} BICS is a promising candidate for

future I_{DDQ} test.

7.2 Future Work

In order for this BICS to be used in production, there are several areas that future work can focus on to make it more robust and cost effective. These areas are:

- Incorporate an on-board controller into the chip to coordinate the operation of all the BICS and implementing desired I_{DDX} algorithms. We have discussed the controller design in this work but the detailed design is not complete and no test chip has been fabricated and measured.
- Evaluate calibration alternatives that are less prone to drift and more immune to leakage associated with advanced technologies. One example would be flash transistors to perform course calibration with charge pumping for fine calibration.
- Reduce BICS area, such as multiplexing BICS inputs among multiple supply lines, at the expense of test time, or using one-sided calibration.
- Place and route of BICS and BICS application in a meshed power line structure, following the initial work done in this area [109].
- Determine and remove the additional 3 mV of high frequency noise that appears in the full sensor system, but not the standalone flip-flop. This would improve resolution by six times, or substantially reduce measurement time.
- Determine and remove the additional measurement-to-measurement variation, perhaps due to inadequate initial calibration, so that the variation matches the

theoretical sampling variation. This would improve resolution by 25% or reduce measurement time.

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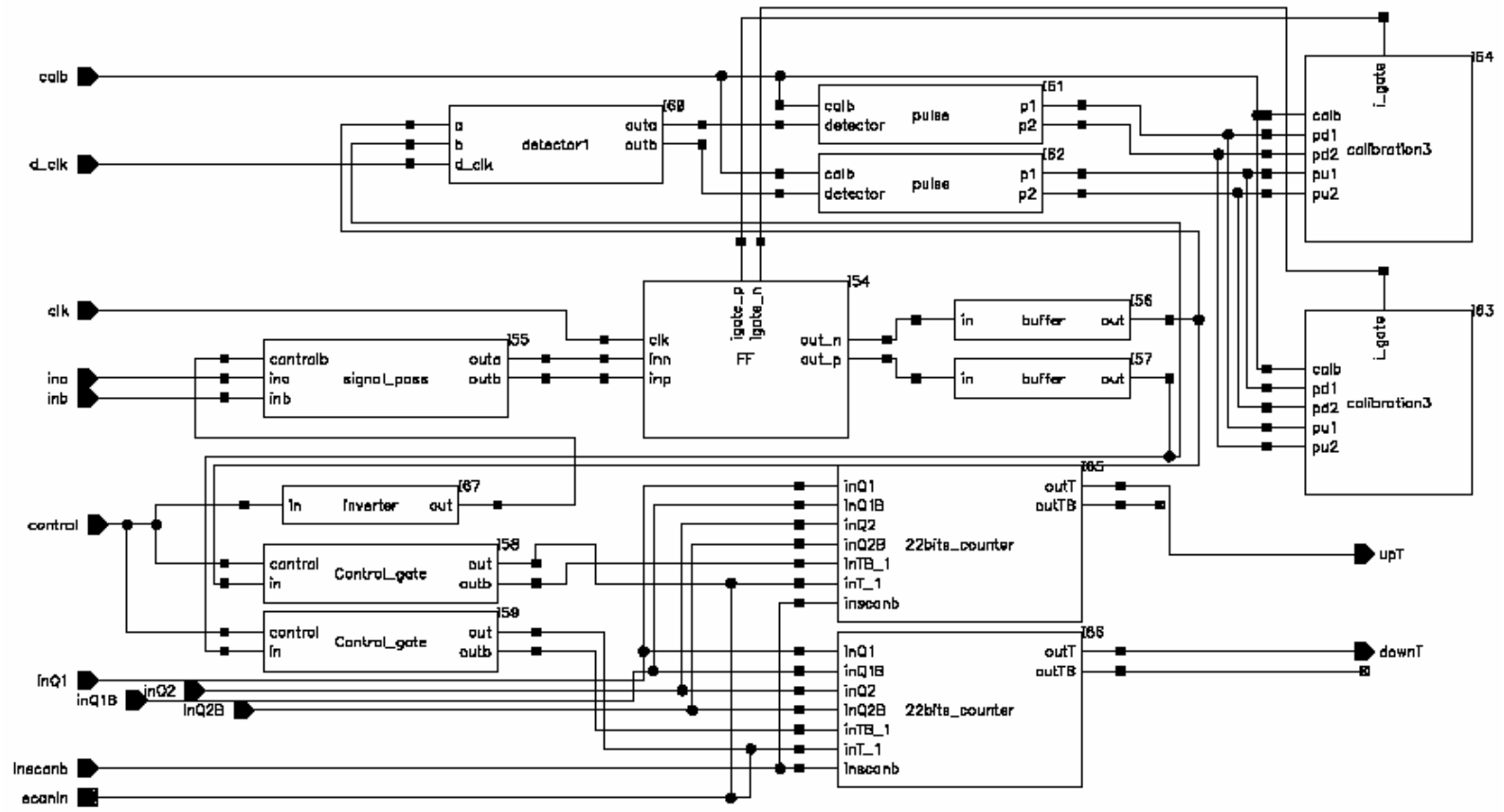
APPENDIX A

IDDQ BICS SYSTEM SCHEMATICS IN CADENCE



VITA

Bin Xue

No. 53 #06-101 Wuwei Rd.

Hefei, Anhui 230001

People's Republic of China

E-mail: xuebin777@hotmail.com

Mr. Bin Xue was born in Anhui, China in 1974. He obtained a B.S. in physics from Xiamen University, Xiamen, China in July 1997, an M.S. in physics from the National University of Singapore, Republic of Singapore, in August 2000 and a Ph.D. in computer engineering from Texas A&M University in December 2005. He worked as a Yield Engineer for Chartered Semiconductor Manufacturing Ltd., Singapore from August 2000 to January 2002 before joining Texas A&M University for his doctoral studies in January 2002. At Chartered, he was responsible for the yield analysis and improvement of the 0.5 μm digital logic process. His research interests are in the areas of VLSI testing, test oriented circuit design, and yield enhancement. He is interested in understanding the positive impact of technology that does not create a digital divide on the lives of common people. His non-technical interests include soccer, music and photography. He is a member of the IEEE.