DESIGN OF COMPACT FREQUENCY SYNTHESIZER FOR SELF-CALIBRATION IN RF CIRCUITS

A Thesis

by

SANGHOON PARK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2004

Major Subject: Electrical Engineering

DESIGN OF COMPACT FREQUENCY SYNTHESIZER FOR SELF-CALIBRATION IN RF CIRCUITS

A Thesis

by

SANGHOON PARK

Submitted to Texas A&M University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Approved as to style and content by:

Aydin Ilker Karsilayan (Chair of Committee)	Jose Silva-Martinez (Member)
Henry F. Taylor (Member)	Alexander Parlos (Member)
Chanan Singh (Head of Department)	

August 2004

Major Subject: Electrical Engineering

ABSTRACT

Design of Compact Frequency Synthesizer for Self-Calibration in RF Circuits.

(August 2004)

Sanghoon Park, B.S., Korea University, Seoul, Republic of Korea

Chair of Advisory Committee: Dr. Aydin Ilker Karsilayan

A compact frequency synthesizer based on a phase locked loop (PLL) is designed for the self-calibration in RF circuits. The main advantage of the presented frequency synthesizer is that it can be built in a small silicon area using MOSFET interface trap charge pump (ITCP) current generators. The ITCP current generator makes it possible to use small currents at nano-ampere levels so that small capacitances can be used in the loop filter. A large resistance, which is required to compensate for the reduced capacitances, is implemented using an operational transconductance amplifier (OTA). An ITCP current generator is used as a tail current source for the OTA in order to realize a small transconductance. The presented frequency synthesizer has the output frequency range from 570 MHz to 600 MHz with a 100 KHz frequency step. Total silicon area is about 0.3 mm^2 using AMIS 0.5 μm CMOS technology, and the power consumption is 26.7 mW with 3 V single power supply.

DEDICATION

To my parents, and my young sister

ACKNOWLEDGEMENTS

I gratefully acknowledge my advisor, Dr. Aydin Ilker Karsilayan for his guidance throughout this research. He also has provided a strong basis and great suggestions for my knowledge in the field of the analog circuit design.

I am so grateful for Dr. Ugur Cilingiroglu for his helpful instruction and suggestions in this research. I would like to thank Dr. Edgar Sanchez Sinencio, Dr. Jose Silva-Martinez who helped me gain my knowledge and skills.

Thanks also to other committee members, Dr. Henry F. Taylor, in the electrical engineering department, and Dr. Alexander Parlos, in the mechanical engineering department, for their time and valuable comments.

Finally, I am very thankful to MOSIS for the chip fabrication.

TABLE OF CONTENTS

Page

CHAPTER Page

LIST OF FIGURES

Page

Page

Page

LIST OF TABLES

Page

CHAPTER I

INTRODUCTION

1.1 Motivation

A frequency synthesizer is a system which has the ability to generate a precise frequency within a specific frequency range. Frequency synthesizers based on phase lock loops (PLL) are the most popular because of their accurate controllability, where the output frequency is a multiple of the reference frequency controlled by external inputs. The output frequency, f_{OUT}, of a frequency synthesizer can be given as:

$$f_{OUT} = f_O + k \cdot f_{STEP} \tag{1-1}$$

where f_O is the lower end of the range, k is the divider ratio, and f_{STEP} is the frequency step. Smaller f_{STEP} increases the resolution of the output frequency, and the total number of output frequencies is defined by k.

The presented frequency synthesizer is targeted for the self-calibration of RF circuits [1]-[3], and for the built-in test circuits [4]-[6]. However, frequency synthesizers are complex and sophiscated systems and usually require large chip area and external

---

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits*.

passive components. Therefore it is not easy to integrate the frequency synthesizer with other circuitry.

All the PLL based frequency synthesizer structures have a filter and one of the most area consuming parts is the passive capacitor in the filter. Since one of the main roles of the capacitor is to convert a current signal into a voltage signal, it is possible to scale the capacitance down by using a small current by:

$$V_{OUT} = \frac{I_{IN}}{sC} \tag{1-2}$$

where I_{IN} is the input current, C is the capacitance in the filter, and V_{OUT} is the converted output voltage. For example, if 1 KV/A is required for I_{IN}/C of Equ. 1-2, 10 μA input current with 10 nF capacitance and 10 nA input current with 10 pF capacitance can satisfy the requirement. However, the 10 nF and 10 pF capacitances require around 11.3 mm^2 (3.365mm × 3.365mm) and 1.13×10^{-2} mm^2 (106 μm × 106 μm) silicon area, respectively.

It is clear that a small current is required to reduce the area which in turn makes it easier to place the whole system on one integrated circuit. The presented frequency synthesizer focuses on how to make the passive components small enough for the integration without sacrificing other characteristics.

1.2 Main contributions

A MOSFET interface trap charge pump (ITCP) current generator is used in order to control a small current precisely. The interface trap charge of a MOSFET was discovered in 1969 [7], and a cascoded complementary structure, which is suitable for the analog circuit application, was presented in 2003 [8]-[9].

Cascoded complementary ITCP current generators enable a small capacitance to be used. The reduced capacitance, however, requires a large resistance to keep the zero frequency at the same position. Since passive element values in the integrated circuit are usually determined by the silicon area, it gives no merit to have a large passive resistance instead of the large capacitance. An alternative way to realize the large resistance is to use active circuits such as an operational transconductance amplifier (OTA) in unity gain feedback configuration, where the equivalent resistance is inversely proportional to the transconductance of the OTA. An ITCP current generator is used as a tail current source in the OTA so that a very small transconductance can be realized.

In summary, a very compact frequency synthesizer is designed with the help of an ITCP current generator. The ITCP structure is based on the cascoded complementary structure proposed in [8], and the active resistor using an OTA is employed to emulate the large resistance.

CHAPTER II

INTEGER-N FREQUENCY SYNTHESIZER

2.1 Integer-N frequency synthesizer architecture

A typical integer-N frequency synthesizer consists of five different blocks: phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO), and frequency divider (/M). The block diagram is shown in Fig. 2-1.

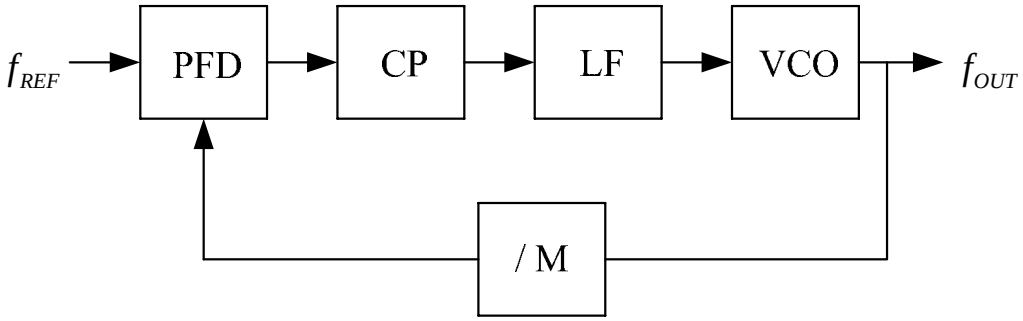


Fig. 2-1. Integer-N frequency synthesizer architecture

The most popular frequency synthesizer structures are direct digital, fractional-N, and integer-N synthesizers. Among these alternatives, the integer-N type is the best for its small size because its frequency variation step is exactly controlled by the reference

input frequency so that no extra circuitry is required for determining its step size. The relationship between the reference and output frequency is given by:

$$f_{OUT} = M \times f_{REF} \tag{2-1}$$

where the integer M can vary from M_L to M_H. The upper and lower bound of M depend on the VCO and frequency divider. Equ. 2-1 implies that the output frequency step is exactly the same as the reference frequency, so a smaller reference frequency results in a higher resolution synthesizer. However, a smaller reference frequency also makes the system slower because the settling time is affected by the loop bandwidth. The relationship between the loop bandwidth, ω_n, and settling time, t_S, can be approximately expressed by [10]:

$$t_S \approx \frac{1}{\zeta \omega_n} \ln\left(\frac{k}{M \mid \alpha \mid \sqrt{1-\zeta^2}} \right) \tag{2-2}$$

where ζ is the damping ratio, M is the divider ratio, k is the change in divider ratio, and α is the required settling accuracy. The t_S is inversely proportional to ω_n, so increasing ω_n results in smaller steeling time in Equ. 2-2. However, ω_n is limited by the stability condition originating from the fact that the frequency synthesizer is the mixed mode system.

In a typical synthesizer, the divider and PFD are digital blocks, whereas the LF and VCO usually consist of analog circuits. So the fact that two different systems are mixed in the frequency synthesizer necessitates discrete time analysis for the stability check. As the loop bandwidth becomes comparable with the input frequency, the PLL suffers from stability problems. F. M Gardner has derived the following stability limit based on the reference frequency and loop bandwidth [11]:

$$\omega_n^2 < \frac{\omega_{REF}^2}{\pi\left(R_1 C_1 \omega_{REF} + \pi\right)} \tag{2-3}$$

where ω_n is the loop bandwidth, ω_{REF} is the reference frequency, and R_1 and C_1 are components of the passive LF. Equ. 2-3 indicates the limitation on not only the upper bound of the loop bandwidth, but also the time constant of R_1 and C_1 for the given reference frequency [12]. In typical designs, the loop bandwidth should be less than approximately one tenth of the reference frequency [10].

2.2 Phase domain analysis

Another stability condition comes from the fact that an integer-N frequency synthesizer has a feedback loop. In case the loop bandwidth meets the stability limit described in Equ. 2-3, the feedback stability condition can be investigated through the phase domain analysis. The phase domain representation is shown in Fig. 2-2. The

combined gain of the PFD and CP is $I_P/2\pi$, and F(s) denotes the LF transfer function. The transfer function of the VCO and divider are combined into K_{VCO}/sM.

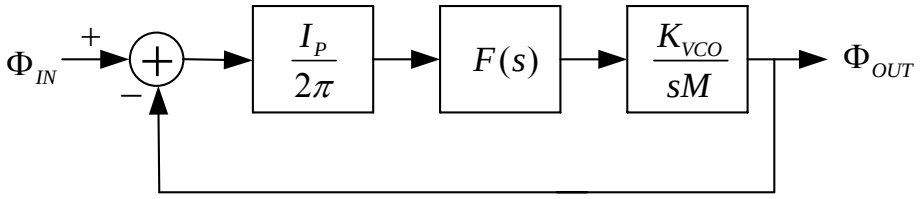


Fig. 2-2. Linear modeling of charge pump frequency synthesizer

The loop filter transfer function, F(s), can have various orders and structures to make the system have multiple poles and zeros at desirable frequencies. The simplest form is the first order loop filter as shown in Fig. 2-3, where I_P denotes the charge pump current and V_{CTRL} is the VCO control voltage.

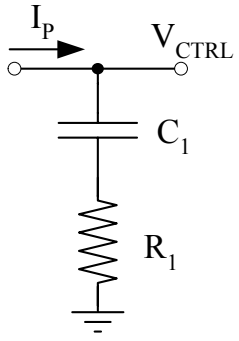


Fig. 2-3. First order loop filter

The transfer function of the first order loop filter is:

$$F(s) = \frac{V_{CTRL}}{I_P} = \frac{1 + sR_1C_1}{sC_1} \tag{2-4}$$

In Fig. 2-2, the open loop transfer function is:

$$H(s) = \frac{\Phi_{OUT}}{\Phi_{IN}} = \frac{I_P K_{VCO}(sC_1R_1 + 1)}{s^2 2\pi C_1 M} \tag{2-5}$$

There are two poles at the origin in the open loop transfer function, so at least one left half plane zero is needed before the unity gain frequency for a phase margin (PM) that will guarantee the stability of the feedback system. A left half plane zero is located at:

$$\omega_Z = \frac{1}{R_1C_1} \tag{2-6}$$

Any charge pump PLL which has the first order loop filter will suffer from a critical drawback. In single ended charge pump structure, the resistor in loop filter can introduce severe disturbances in the VCO control voltage [11]. Even in steady state, any minute non-ideal charge pump current due to the mismatch or charge injection from charge pump switching operations will result in significant voltage ripples via the series resistor, so the output frequency or phase is corrupted. To mitigate this ripple problem, a second capacitance is usually connected from the output of the loop filter to ground, so that F(s) becomes a second order loop filter.

In case of the second order loop filter, the stability problems become worse. F(s) is similar to the Equ. 2-4 except that it has one more pole due to the parallel connected C_2, which will degrade the phase margin:

$$F(s) = \frac{1 + sR_1C_1}{sC_1\left(1 + \frac{C_2}{C_1} + sR_1C_2\right)} \tag{2-7}$$

Then the open loop transfer function becomes:

$$H(s) = \frac{I_P K_{VCO}(sC_1R_1 + 1)}{s^2 2\pi C_1 M\left(1 + \frac{C_2}{C_1} + sR_1C_2\right)} \tag{2-8}$$

The second pole of F(s) is located at:

$$\omega_{P2} = \frac{1 + C_2/C_1}{R_1C_2} \tag{2-9}$$

In order to push the second pole over the unity gain frequency, C_2 is usually chosen less than 10 % of C_1, so ω_{P2} can be simplified to:

$$\omega_{P2} \cong \frac{1}{R_1C_2} \tag{2-10}$$

The unity gain frequency of the open loop transfer function is [13]:

$$\omega_C = \frac{I_P K_{VCO} R_1}{2\pi N}\left(\frac{C_1}{C_1 + C_2}\right)\frac{\cos(\phi_{P2})}{\sin(\phi_Z)} \tag{2-11}$$

where $\phi_Z = \tan^{-1}(\omega_C / \omega_Z)$ and $\phi_{P2} = \tan^{-1}(\omega_C / \omega_{P2})$. The open loop phase margin is:

$$\phi_m = \phi_Z - \phi_{P2} = \tan^{-1}\left(\frac{\omega_C}{\omega_Z}\right) - \tan^{-1}\left(\frac{\omega_C}{\omega_{P2}}\right) \tag{2-12}$$

In case of f_{REF} = 100 KHz, C_1 = 12.5 pF, C_2 = 0.5 pF, R_1 = 22 MΩ , I_P = 10 nA, and K_{VCO}/M = 140 KHz/V, the zero and second pole are located at 578 Hz and 14.5 KHz, respectively. The unity gain frequency and phase margin are 4.54 KHz and 65.4° using Equ. 2-11 and 2-12. Fig. 2-4 shows the gain in dB scale and phase response in degrees of the open loop transfer function.

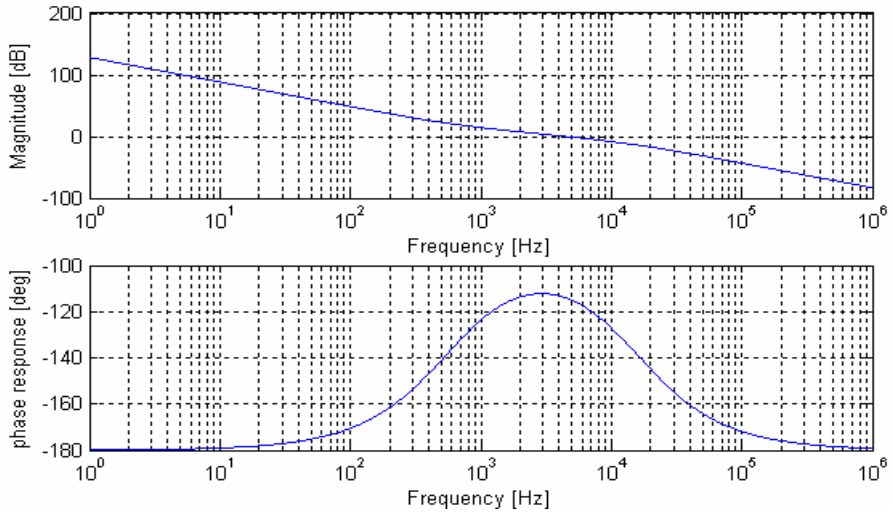


Fig. 2-4. Gain and phase response of the open loop transfer function

The unity gain frequency around 4.5 KHz and the phase margin about 65° matches well with the calculation results. In order to meet the stability condition given in Equ. 2-3, the unity gain frequency is set to approximately twenty times smaller than the reference frequency, where 65° phase margin can guarantee the stability condition of the feedback system. The stable step response of the feedback system with 65° phase margin is shown in Fig. 2-5, which also compares the step response of the second and third order charge pump phase locked loop (CPPLL) in order to check the effect of the second capacitor C_2 in the LP.

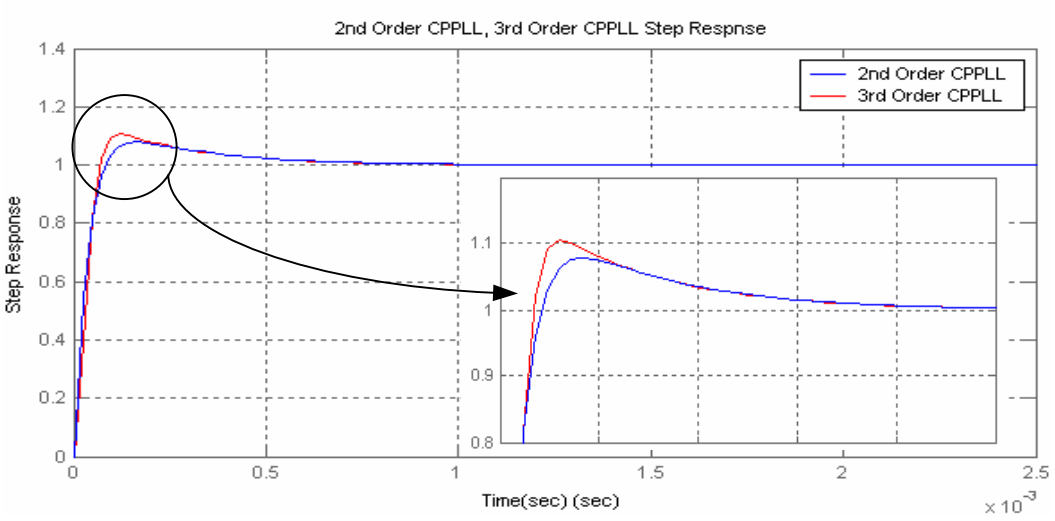


Fig. 2-5. Step response of the closed loop PLL

Since C_2 has a small value (4% of C_1), the second pole of the LF is located at much higher frequency than the unity gain frequency. The step response of the 3rd order CPPLL shows a little deviation from that of the 2nd order CPPLL.

CHAPTER III

INTERFACE TRAP CHARGE PUMP CURRENT GENERATOR

3.1 MOSFET interface trap charge pump

MOSFET interface trap charge pump (ITCP) current generators are used to implement the charge pump (CP) and the active resistor in the loop filter (LF). A very small current can be precisely controlled by using the ITCP circuit. All the required information about the MOSFET characteristics in the AMIS 0.5 μm CMOS technology follows the data parameters in [8]-[9].

The interface trap charge pump is based on the defects in the Si-SiO_2 interface of a MOSFET. According to the voltage level of the gate pulse, a small portion of the electrons under the channel is repeatedly trapped and released. Thus, the averaged charge transfer of these trapped charges can be considered an ITCP current. The MOSFET configuration as an ITCP circuit and the required condition for gate pulse transition level are shown in Fig. 3-1, where V_W and V_S denotes the well and source terminal voltage, respectively, and V_G is the gate pulse fluctuating from V_{SS} to V_{DD}. I_P is the average current resulting from the interface trap charge and I_I is the injection current due to the gate pulse.

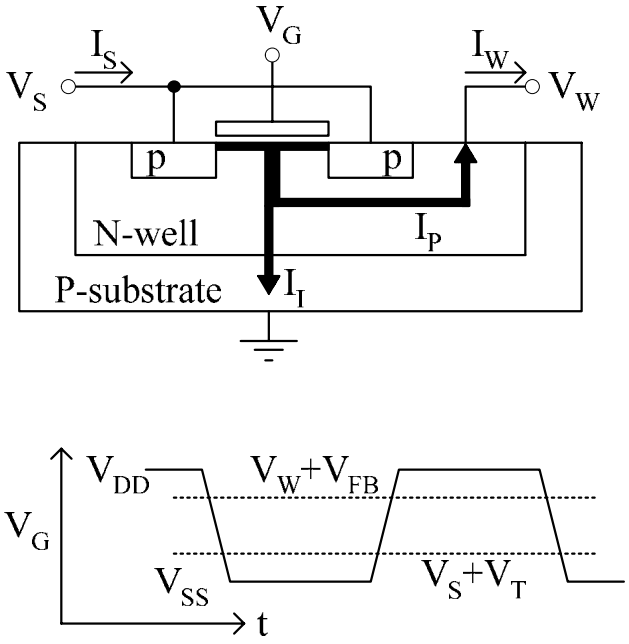


Fig. 3-1. MOSFET transistor and gate pulse

The accumulation condition is:

$$V_W < V_{DD} - V_{FB} \tag{3-1}$$

The inversion condition is:

$$V_S > V_{SS} - V_T \tag{3-2}$$

In case the gate pulse V_G and external bias voltages V_W and V_S satisfy Equ. 3-1 and 3-2, the charge transferred from the source to the well terminal by a pump device in one cycle is approximately given by [9]:

$$Q_P = q \cdot N_{it} \cdot A \tag{3-3}$$

where q = 1.6×10^{-19} [C] is the absolute value of the electron charge, A is the gate area of the pump, and N_{it} [m^{-2}] is the spatial density of the traps participating in charge pumping. Therefore the average current can be given by:

$$I_P = q \cdot N_{it} \cdot A \cdot f \tag{3-4}$$

where f is the frequency of the gate excitation pulse. I_P is quite controllable current component using both the gate pulse frequency and MOSFET transistor size, whereas there is one more current component in Fig. 3-1. Some of the mobile holes, which are colleted in the inversion phase, release and flow into the substrate instead of the source terminal during the upward transition of the gate pulse. The injection current, I_I, means the averaged charge flowing from the source to substrate [8].

3.2 Cascoded complementary ITCP current generator

A single PMOS pump shown in Fig. 3-1 is the simplest structure to transfer the charge from the source to well terminal, but the pulse feedthrough problem and the well terminal bias difficulty prevent a single PMOS pump from being used in the integrated circuits. All these shortcomings can be improved using a cascoded complementary pump structure shown in Fig. 3-2.

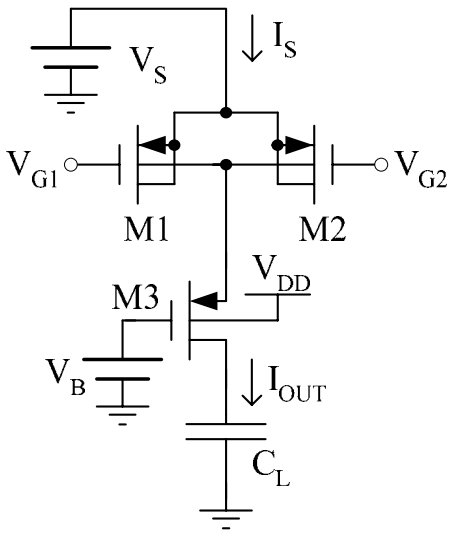


Fig. 3-2. Cascoded complementary ITCP current generator

The parallel pump devices denoted by M1 and M2 have the same size and operate with complementary gate excitation. The gate pulse feedthrough is considerably reduced by mobile charge sharing between the two pumps, and the well bias voltage of two pump devices is automatically set by the external bias V_B, which is outside of the current path [8]. Based on the cascoded complementary structure, a 10 nA ITCP current generator is designed. The cascoded transistor M3 plays an important role in setting the well terminal voltage, but its size has little effect on the charge pump mechanism. Thus, its size is selected to be the same as the charge pump transistors, M1 and M2. The design parameters are shown in Table 3-1.

Table 3-1. 10 nA cascoded complementary current source design parameters

Parameter	Value
Q	1.6×10^{-19} C
N_{it}	1.85×10^{-13} m^{-2}
$W_{M1, M2, M3}$	21 µm
$L_{M1, M2, M3}$	14.25 µm
$f_{VG1, VG2}$	6.4 MHz

Fig. 3-3 shows the simulation results in time domain.

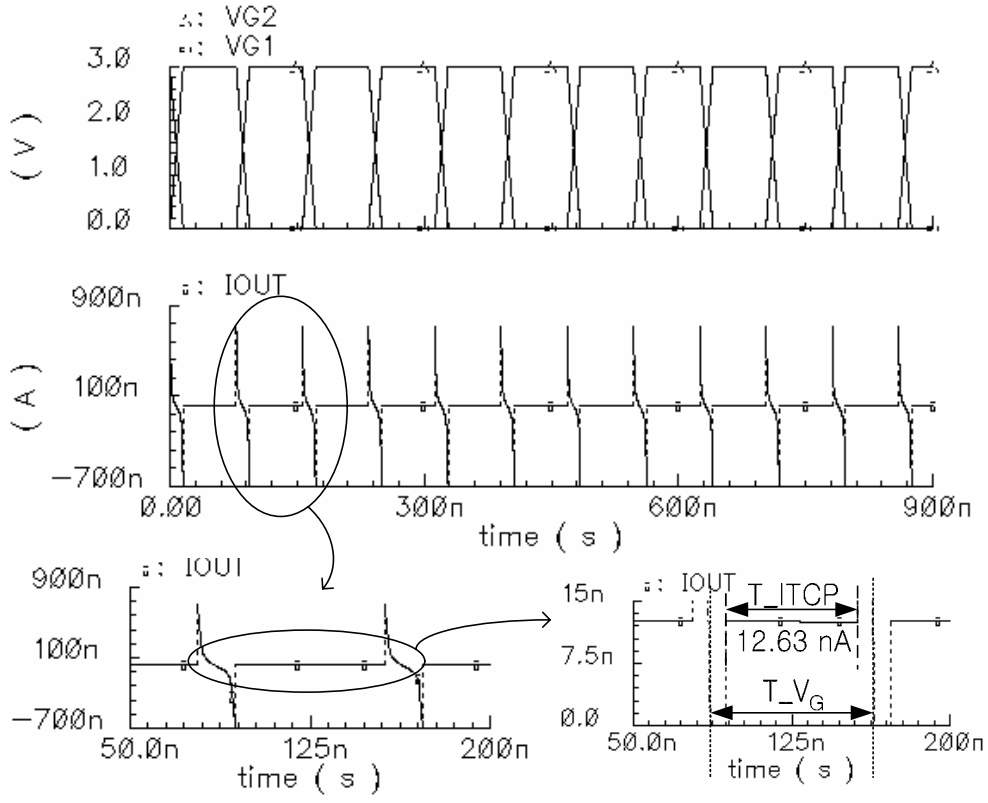


Fig. 3-3. Complementary gate pulses (V_{G1}, V_{G2}) and output current (I_{OUT})

The charge pump current, I_P, is the average current within one gate pulse time and the average current can be calculated by:

$$I_P = \frac{T\_ITCP(61.42\ ns)}{T\_V_G(78.1\ ns)} \times 12.63\,nA = 9.94\,nA \qquad (3\text{-}5)$$

Since the same size transistors result in the same channel charge and parasitic capacitance, a pair of the adjacent negative and positive current peaking cancels the pulse feedthrough effect. As the result, 12.63 nA current in Fig. 3-3 shows little variation in its absolute value during every gate pulses.

One more thing, which should be mentioned before proceeding to Chapter IV, is the simulation setup used. Interface trap charge is modeled by an additional circuit block designed using AHDL (Analog Hardware Description Language). Two such blocks are connected between the well and source terminals of M1 and M2 in Fig. 3-2. Generating one current pulse flowing from the source to well terminal during one gate pulse cycle, the AHDL block can emulate the charge transfer trapped by the interface region between Si-SiO_2. The code description for the ideal block is presented in the appendix.

CHAPTER IV

FREQUENCY SYNTHESIZER BUILDING BLOCKS

4.1 Phase-frequency detector

A phase-frequency detector (PFD) is a block which can detect a phase difference as well as a frequency difference between a reference signal and a feedback signal coming from the divider. A general tri-state phase-frequency detector is shown in Fig. 4-1 [14].

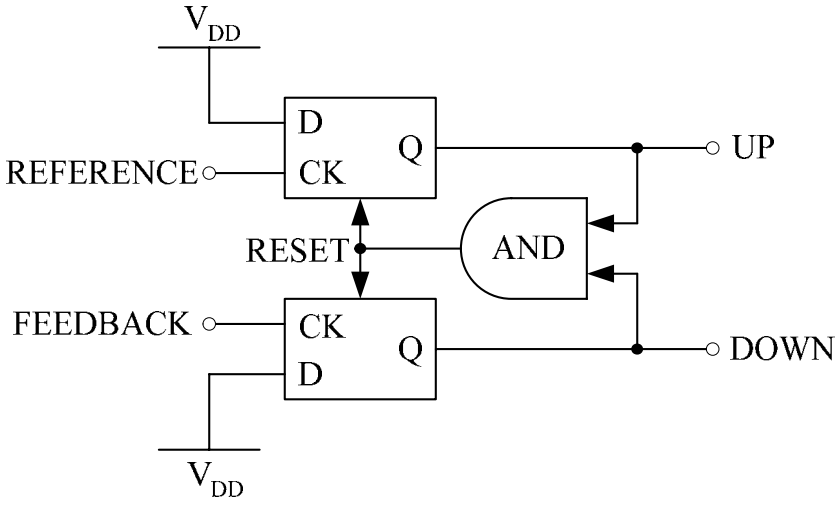


Fig. 4-1. Phase-frequency detector

The functionality of a PFD is depicted in Fig. 4-2 by its state diagram. When the rising edge of the reference signal leads that of the feedback signal, the output state of the PFD is: UP=1 and DOWN=0. The UP control signal triggers the charge pump to increase the VCO control voltage, which increases the VCO output frequency. When the rising edge of the reference signal lags that of the feedback signal, the output state of the PFD is: UP=0 and DOWN=1. The DOWN control signal triggers the charge pump to decrease the VCO control voltage, which decreases the VCO output frequency. The final state is the hold state when both UP and DOWN fall to the logic zero. In this case, the VCO control voltage remains unchanged as does the VCO output frequency.

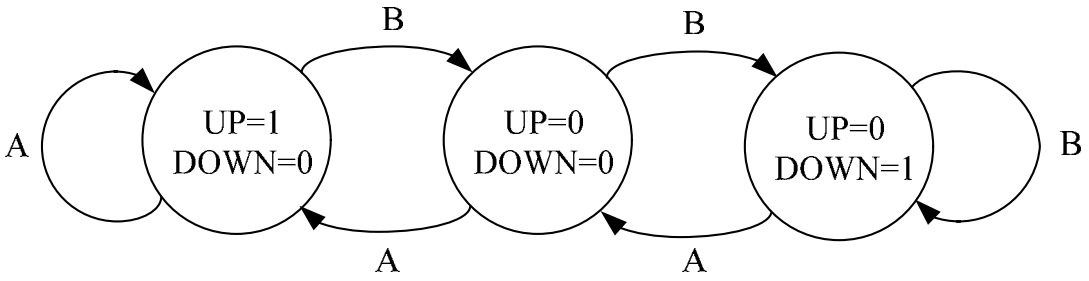


Fig. 4-2. Tri-state diagram of the PFD

In theory, there may be one more state when both UP and DOWN are logic high. The additional 4th state is hidden and not shown in Fig. 4-2 because it happens due to the delay time of the AND gate. The RESET signal is generated by the AND gate in the PFD's own feedback loop when both UP and DOWN are logic high, so the time duration of the hidden 4th state will be controlled by the transition delay of the AND gate. In

general, a delay element is inserted between the AND gate and RESET input of the D flip-flops in order to control the time duration of the hidden 4th state.

A delay element for controlling the 4th state is very important to correct the dead-zone problem. In case the phase difference between the reference and feedback signal is below a certain value, the UP and DOWN control signals can not reach their logic high level without a delay element due to the finite rising and falling speed, failing to turn on the charge pump [15].

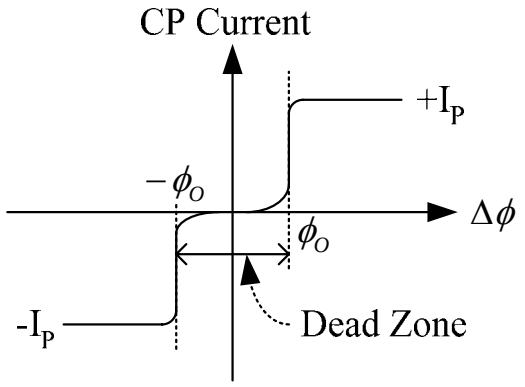


Fig. 4-3. Dead-zone problem in charge pump circuit

The dead-zone allows the VCO to accumulate a random phase error of as much as ϕ_O with respect to the input without any feedback signal as shown in Fig. 4-3. The dead-zone problem will be handled again with the charge pump structure in Section 4.2.

4.2 Charge pump

The charge pump (CP) has the function of converting the phase or frequency error generated by the phase-frequency detector (PFD) into an electric charge which increases or decreases the control voltage at the output of the loop filter (LF). The combined gain of the PFD, CP, and LF can be roughly expressed by the aspect ratio of $I_p/2\pi sC$. Therefore a small charge pump current reduces the capacitance size without sacrificing the total gain. A typical single ended CP structure with a capacitance load is shown in Fig. 4-4.

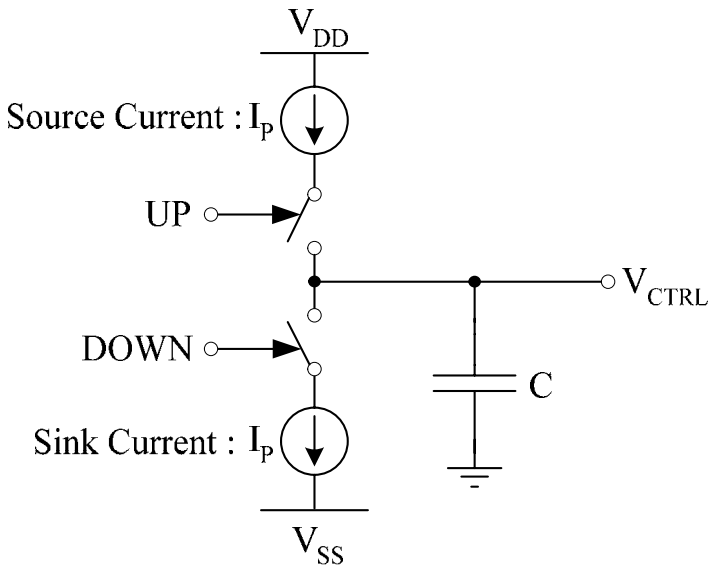


Fig. 4-4. Charge pump with a capacitor

The UP and DOWN control signal are the outputs of the PFD and the V_{CTRL} is the input of the voltage controlled oscillator (VCO) in Fig. 4-4. Two 10 nA interface trap charge pump (ITCP) current generators will replace the sink and source current. In the ITCP structure, the sink current and source current are based on I_P and I_S, respectively, in Fig. 4-5.

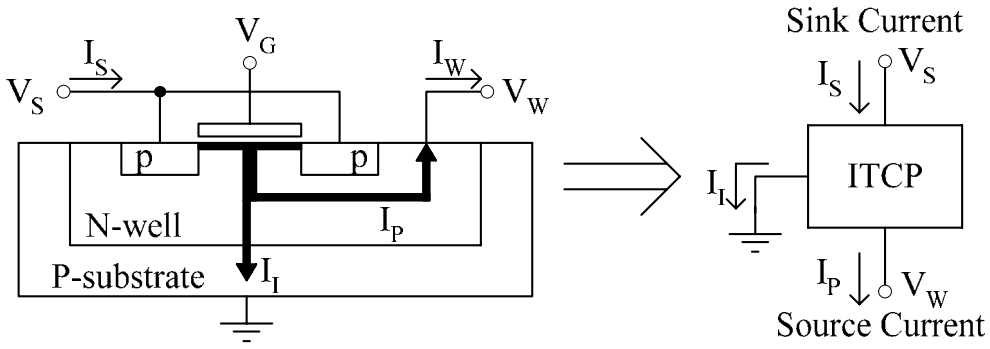


Fig. 4-5. ITCP sink and source current

Unfortunately, the ITCP sink current is difficult to control precisely because of the existence of the substrate injection current I_I which flows from the source terminal to the substrate. Thus, different current source configurations are used for the sink and source currents in the charge pump block.

The source current configuration consists of a cascoded complementary ITCP current generator and an extra cascode transistor at the output as shown in Fig. 4-6. Since the source current configuration and the sink configuration are different, transistor M4 will be used to reduce the mismatch between the two different structures.

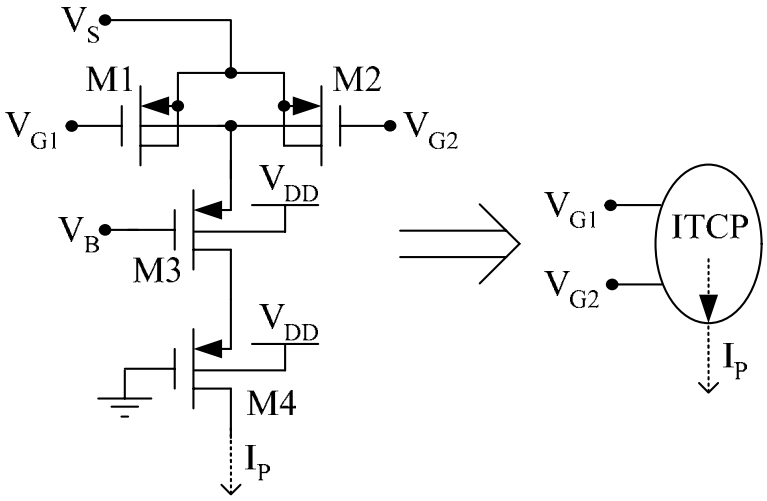


Fig. 4-6. Source current configuration

The sink current configuration can be built with the help of a current mirror. The ITCP current generator makes only a source current, but the current mirror will convert it to a sink current in Fig. 4-7.

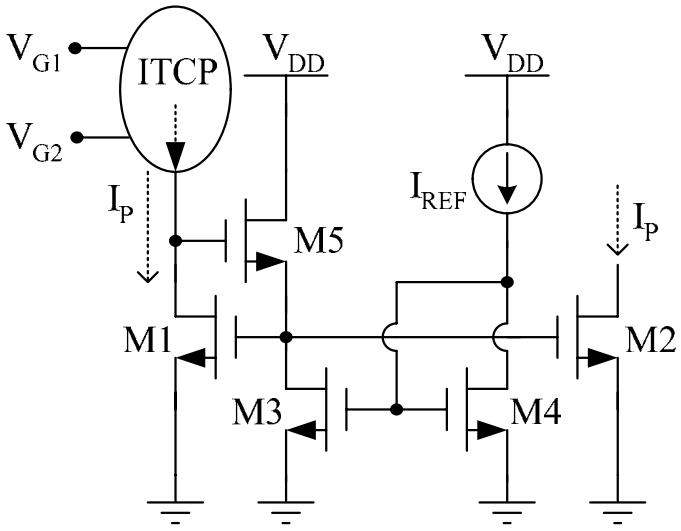


Fig. 4-7. Sink current configuration

A simple current mirror structure can not be used due to its slow switching speed, so an extra current mirror is inserted. The extra current mirror consisting of M3, M4, M5 and I_{REF} will increase the switching speed of the main current mirror consisting of M1 and M2.

An interface block is required in order to control two ITCPs in the charge pump with two PFD outputs. This block will supply ITCPs with the complementary gate pulses only when either the UP or the DOWN control signal is activated. The generation of complementary gate pulses will be explained in Section 4.5. Fig. 4-8 shows the interface block between the PFD and ITCP current generator in the source current configuration of the CP. Since the outputs of the PFD can be easily expanded to four different control signals, UP, DOWN, and their complementary signals which are $\overline{UP}$ and $\overline{DOWN}$, the interface block uses the $\overline{UP}$ for the source part and $\overline{DOWN}$ for the sink part instead of the UP and DOWN.

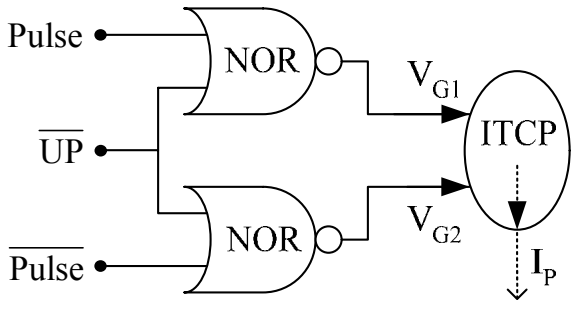


Fig. 4-8. Interface block between PFD and ITCP in the source current

The interface block shown in Fig. 4-8 has the ability to supply the ITCP circuit with the complementary gate pulses only when the $\overline{UP}$ signal is activated, which means that the charge pump flows the charging current into the loop filter when the UP is logic high. The same interface block is used for the ITCP in the sink current configuration with the $\overline{DOWN}$ control signal.

The fact that the sink and source current configurations are different results in the current mismatch problems. Thus, a delay element in the PFD can deteriorate the ripple on the V_{CTRL} due to the current mismatch by increasing time duration when both the sink and source current to be turned on. Moreover, at least one or two gate pulse time is required for the delay element in the PFD, so such a delay element will consume unacceptable silicon area in the integrated circuit. For example, in case the delay element is built using passive elements, the required RC time constant is about 300 ns. The reasonable R and C value for a 300 ns time constant will be 10 KΩ and 30 pF, respectively. Such large passive elements will offset the silicon area saved by using the ITCP current generators.

The PFD in the presented frequency synthesizer does not have any extra delay element, so the delay is just the AND gate transition time which is much smaller than that of the ITCP gate pulse. As a result, the VCO control voltage will show random variations resulting from the dead-zone of the PFD so that the VCO output frequency will suffer from random phase variations (jitter). Fine tuning both the CP and PFD

brings the VCO jitter within an acceptable range. The jitter problem will be explained in detail in Chapter V with the entire PLL simulation results.

4.3 Loop filter with active resistor

The loop filter (LF) plays an important role in not only guaranteeing the feedback stability condition by inserting a left half plane zero, but also in smoothing the VCO control voltage by suppressing high frequency components. Series combination of a capacitor (for converting the charge pump current into the voltage output) and a resistor (for compensating the phase margin) can build the simplest loop filter, but usually an additional parallel capacitance is connected to reduce the control voltage ripple. Higher order filters are better for the spectral purity of the VCO output frequency, but worse for the stability of the feedback loop. The second order loop filter is shown in Fig. 4-9.

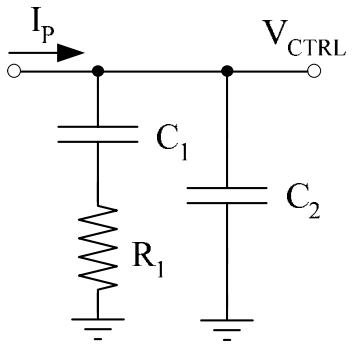


Fig. 4-9. Second order loop filter

I_P denotes the output current of the charge pump, V_{CTRL} is the VCO control voltage, and the passive component values are C_1 = 12.5 pF, C_2 = 0.5 pF, R_1 = 22 MΩ in Fig. 4-9. The small capacitance, which is totally 13 pF, is enough for the loop filter due to the interface trap charge pump (ITCP) current generator which supplies I_P of 10 nA. Although the capacitance is reduced by the ITCP, the large resistance, which is required in order not to change the zero frequency, raises another problem for the on-chip integration.

An active resistor using an operational transconductance amplifier (OTA) with unity gain feedback configuration is used to solve the problem of realizing a large resistance. The equivalent resistance is inversely proportional to the transconductance (G_m) of the OTA in Fig. 4-10. An ITCP current generator is used as a tail current source of the OTA to obtain a small G_m.

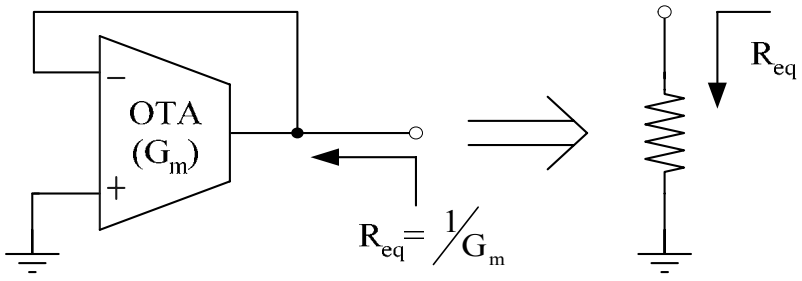


Fig. 4-10. Active resistor realized by an OTA

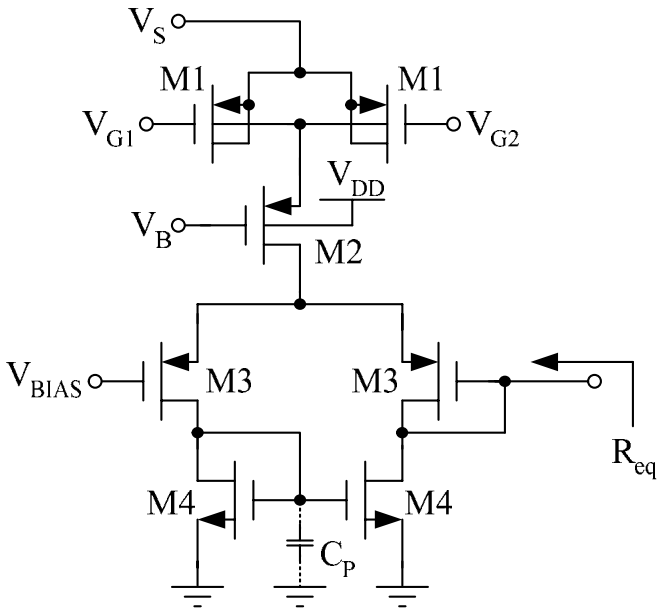


Fig. 4-11. Small G_m OTA with unity gain feedback configuration

The tail current supplied by the ITCP is too small to keep any transistor in the strong inversion, so it is a reasonable assumption that all the MOSFETs operate in the deep-subthreshold condition with nano-ampere bias currents. The transconductance expression under the deep-subthreshold is [9]:

$$G_m \cong \frac{2.3 I_P}{4S} \tag{4-1}$$

where S is called subthreshold-swing and defined by [16]:

$$S \cong 2.3 \frac{kT}{q}\left(1+\frac{C_t}{C_{OX}}\right) \tag{4-2}$$

where $C_{OX} = \varepsilon_{OX} / T_{OX}$ is the capacitance of the gate oxide and $C_t = \varepsilon_S / x_t$ is the capacitance of the surface depletion region.

Small signal transfer function of the active resistor is:

$$\mathrm{R}_{eq}(s) = \frac{\frac{1}{G_m(s)}}{1 + sC_{OUT}R_{OUT}} = \frac{1}{g_{m3}} \left(\frac{1 + s\frac{C_P}{g_{m4}}}{1 + s\frac{C_P}{2g_{m4}}} \right) \times \frac{1}{1 + sC_{OUT}R_{OUT}} \tag{4-3}$$

where C_P is the parasitic capacitance at the gate of M4 in Fig. 4-11. The three corner frequencies of $R_{eq}(s)$ are:

$$\omega_{Z1} = \frac{g_{m4}}{C_P} \tag{4-4}$$

$$\omega_{P1} = \frac{2g_{m4}}{C_P} \tag{4-5}$$

$$\omega_{P2} = \frac{1}{C_{OUT}R_{OUT}} \tag{4-6}$$

Usually ω_{P2} is located at a higher frequency than both ω_{P1} and ω_{Z1} because g_{m4} is very small. Therefore the condition that the zero frequency of the active resistor

should be located at a higher frequency than the unity gain frequency of the PLL, is enough for the active resistor design in order not to affect the PLL characteristics.

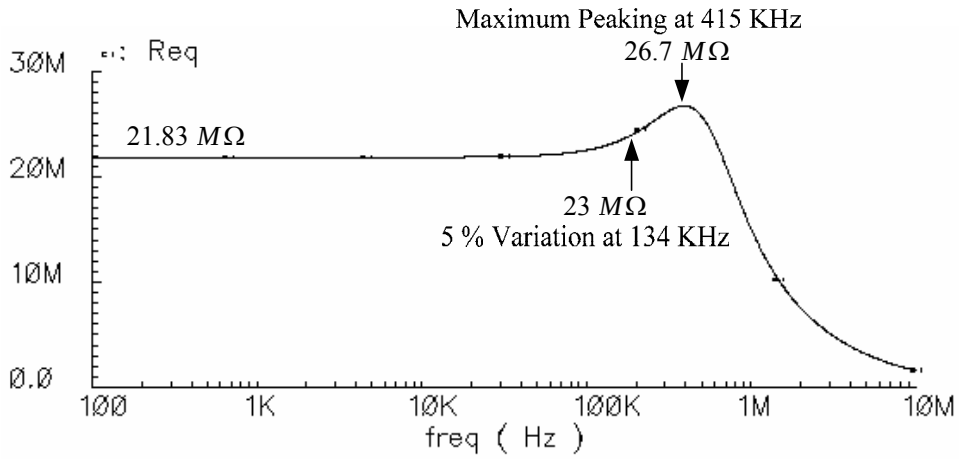


Fig. 4-12. Active resistor frequency response

Fig. 4-12 shows the frequency response of the active resistor. The 5 % variation of the equivalent resistance happens at 134 KHz, which is about twenty five times larger frequency than the unity gain frequency. Thus, the deviation of the equivalent resistance in the frequency response from its designed value of 22 MΩ can be negligible. Even though the active resistor shows little variation in the small signal response, its equivalent resistance can vary in the large signal response. I-V plot is shown in Fig. 4-13, and its derivation, which means the equivalent resistance, is shown in Fig. 4-14.

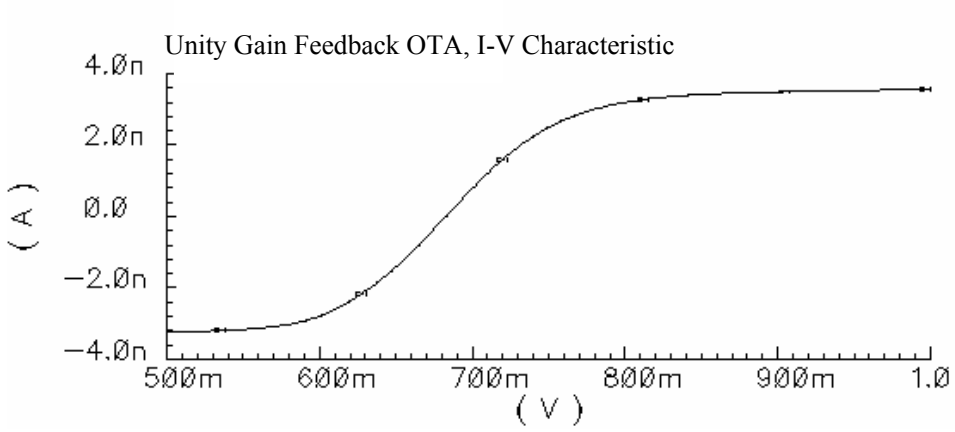


Fig. 4-13. Active resistor I-V plot

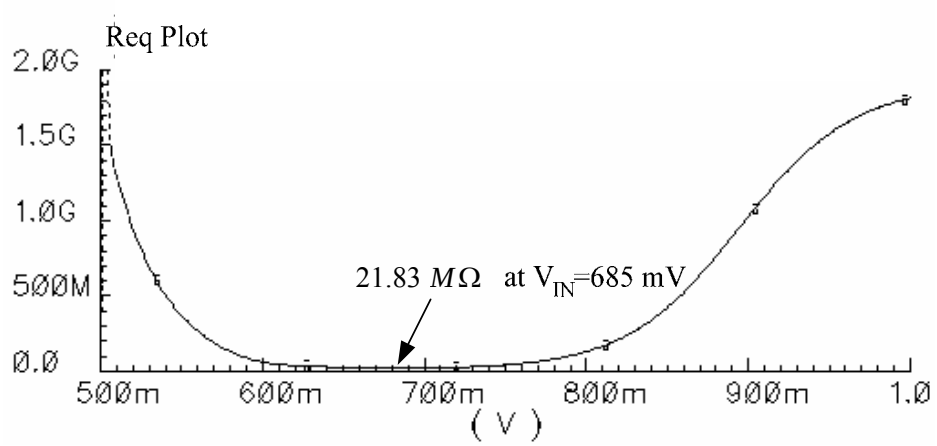


Fig. 4-14. Equivalent resistance variation

Fig. 4-12 and Fig. 4-13 show that the equivalent resistance depends on the voltage level at the OTA output. The variation of the equivalent resistance will not be problematic in steady state because the capacitance C_1 will work as a DC block so that the output node of the active resistor will be isolated from the VCO control voltage.

However, the increased resistance will push the poles and zero to lower frequencies than those of steady state, so the resistance variation will reduce the phase margin and result in a less stable system during a large transition. In Chapter V, the variation effect of the equivalent resistance will be shown in detail with the closed loop PLL simulation.

Fig. 4-15 compares the required areas between the active and passive resistor in the integrated circuit. A 22 MΩ passive resistor, which is made up with the 2nd poly layer, needs about 550 times larger silicon area than active resistor.

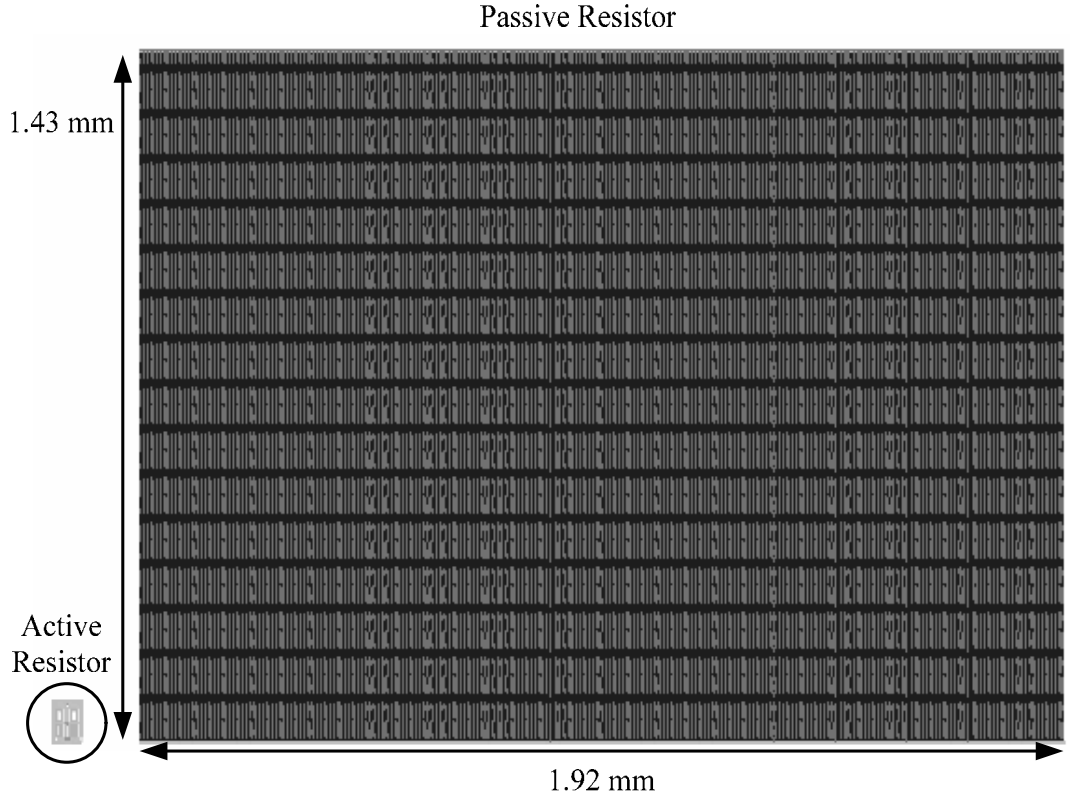


Fig. 4-15. Passive resistor vs. active resistor in realizing 22 MΩ

4.4 Voltage controlled oscillator

An oscillator is a physical building block that has the ability to generate a sinusoidal or a periodic pulse signal at a fixed frequency. However, a voltage controlled oscillator (VCO) has an additional input that can change the VCO output frequency.

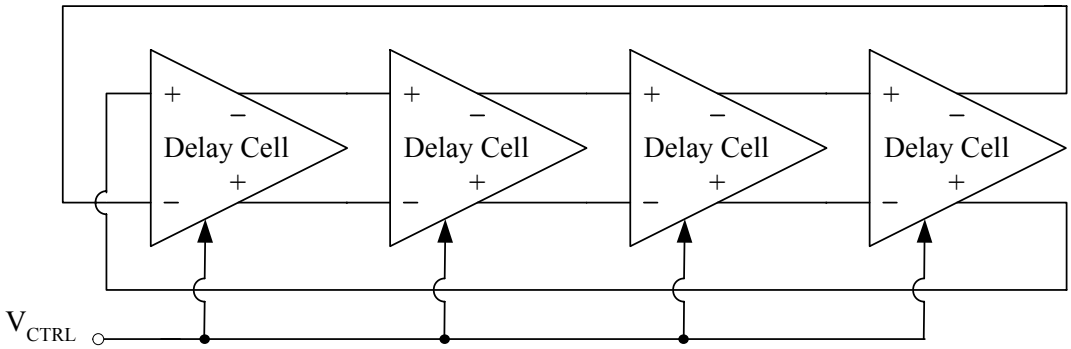


Fig. 4-16. 4 stage ring voltage controlled oscillator implementation

The differential implementation can utilize an even number of stages where one stage is configured as non-inverting. A 4 stage ring VCO is shown in Fig. 4-16 and the delay cell is shown in Fig. 4-17. The control voltage will change the tail current, as well as the output resistance, which is controlled by the transconductance of M3 or M4 in Fig. 4-17. The variation of the output resistance changes the time constant at the output, so the oscillation frequency varies

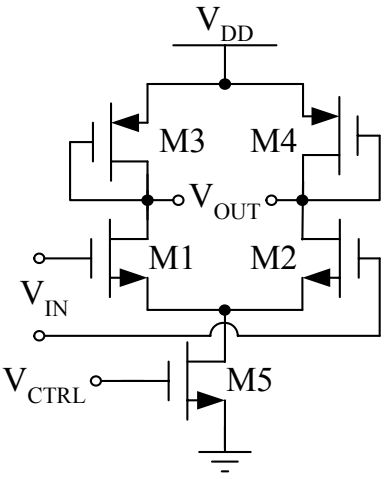


Fig. 4-17. Delay cell

Since the frequency tuning of the delay cell is based on the active devices, the relationship between the control voltage and VCO output frequency is not linear as shown in Fig. 4-18.

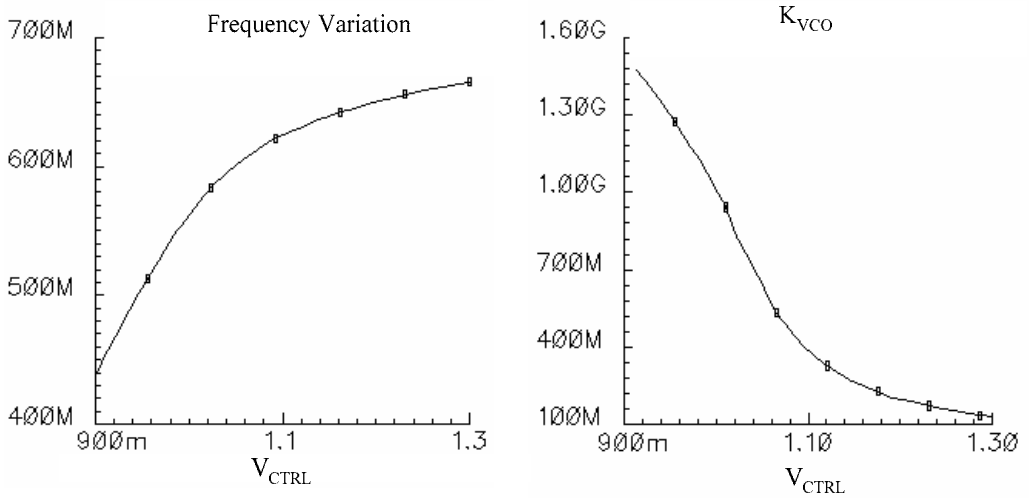


Fig. 4-18. Frequency and VCO gain variation with control voltage

Since the VCO output frequency variation does not change linearly with the control voltage, the VCO gain, K_{VCO}, is not constant. However, the VCO gain variation will not be critical because only the small portion of the control voltage will be used and a high enough phase margin of the open loop PLL can guarantee the stability condition regardless of the VCO gain variation within the selected control voltage range. The VCO characteristics are summarized in Table 4-1.

Table 4-1. VCO characteristics

V_{CTRL}	f_{VCO}	K_{VCO}
1 V	570 MHz	970 MHz/V
1.05 V	600 MHz	670 MHz/V

In the presented frequency synthesizer, a 30 MHz VCO output frequency variation, which corresponds to the total of 300 frequency steps in case of the 100 KHz reference frequency, is selected. The control voltage varies from 1 V to 1.05 V, resulting in the VCO frequency range from 570 MHz to 600 MHz. Including the divider ratio, the K_{VCO} can be recalculated according to the PLL format shown in Fig. 2-2. When the VCO output frequency is 600 MHz:

$$\left(\frac{K_{VCO}}{M}\right)_{MAX} = \frac{970\ MHz/V}{\left(\frac{570\ MHz}{100\ KHz}\right)} = 170\,KHz/V \tag{4-7}$$

If the VCO output frequency is 570 MHz:

$$\left(\frac{K_{VCO}}{M}\right)_{MIN} = \frac{670\ MHz/V}{\left(\frac{600\ MHz}{100\ KHz}\right)} = 112\ KHz/V \tag{4-8}$$

So the average K_{VCO}/M is 140 KHz/V and K_{VCO}/M variation is about ±20%.

4.5 Divider

A divider in the feedback path enables the PFD to compare the reference frequency with the divided VCO output frequency. A typical integer-N programmable divider, called pulse swallow divider, is shown in Fig. 4-19 [10]. The pulse swallow divider can change its divider ratio according to the external channel selection input.

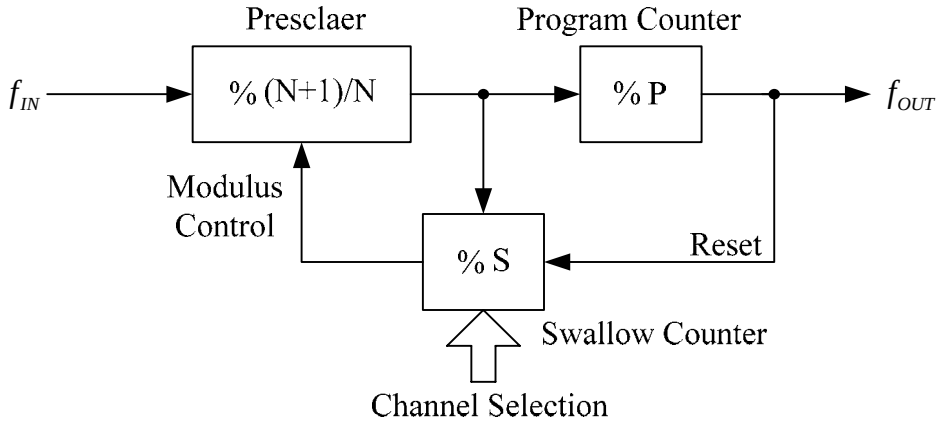


Fig. 4-19. Pulse swallow divider

When the program counter resets the swallow counter, the prescaler divides the frequency of the incoming signal by N+1 until the swallow counter finishes counting and activates the modulus control signal. When the modulus control signal is activated, the prescaler changes its divider ratio from N+1 to N until the program counter finishes counting and generates a reset signal. Therefore the divider output frequency is expressed by:

$$f_{OUT} = \frac{f_{IN}}{(PN + S)} \tag{4-9}$$

where P and S are the counting numbers of the program and swallow counter, respectively. Since the minimum change of S is one, the frequency step corresponds to the reference frequency of the PFD.

The speed of both the prescaler and digital counters is important in determining S, P, and N in Equ. 4-19. Since the maximum speed of the prescaler is usually slower than that of the VCO in the given technology, the prescaler limits the maximum frequency beyond which the frequency synthesizer can lose its tracking ability. On the other hand, the speed of the digital counters put a limit in the total number of frequencies which the frequency synthesizer can generate. Depending on the speed of the digital circuits, the counting number P has the maximum values, and limits the maximum number of S by:

$$P \geq S \tag{4-10}$$

The VCO output frequency is about 600 MHz and the reference frequency is 100 KHz. The frequency range of the presented frequency synthesizer is 30 MHz. As the result, a 9 bit swallow counter and a 10 bit program counter are selected. The maximum speed of the 10 bits program counter is less than 200 MHz, so an 8/9 prescaler is chosen for connecting the VCO frequency to the digital counters. The selected counting numbers, which are required for the target frequencies, are shown in Table 4-2.

Table 4-2. Divider design number

VCO f_{OUT}	P	S
570 MHz	700 (1 010 111 100)	100 (001 100 100)
600 MHz	700 (1 010 111 100)	400 (110 010 000)

4.5.1 Prescaler

A dual modulus prescaler is a high frequency divider that can change the divider ratio between N and N+1. Current mode logic (CML) technique is used in the prescaler design to follow the maximum speed in the given technology, but it should be optimized for low power consumption. Fig. 4-20 shows the 8/9 prescaler building block, which consists of a synchronous divide-by-2/3 circuit and two asynchronous divide-by-2 circuits.

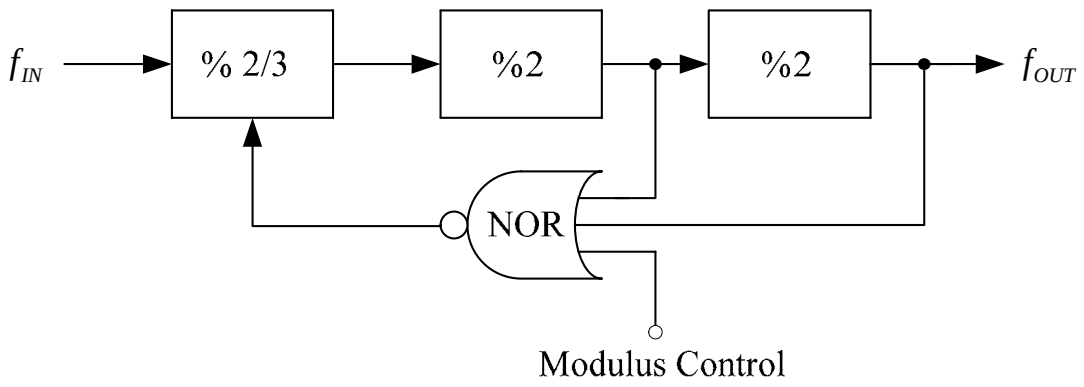


Fig. 4-20. 8/9 prescaler building block

According to the modulus control (MC) input, the 8/9 prescaler changes its divider ratio. The divider ratio will be 8 when the MC is logic high, and it will be 9 when the MC is low. A synchronous divide-by-2/3 circuit shown in Fig. 4-20 is designed using two CML DFFs and two CML NOR gates.

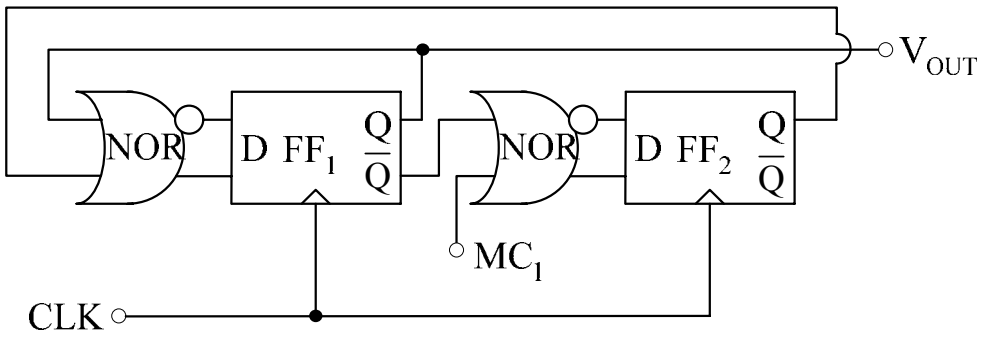


Fig. 4-21. Synchronous divide-by-2/3 circuit

The divide-by-2/3 circuit in Fig. 4-21 uses a symmetrical structure so that the loading effect at each FF output is minimized. Both FF_2 and FF_1 are loaded by one NOR

gate in Fig. 4-21. Even if the following output buffer will be connected to the output, the reduction of the FF_2 load capacitance helps to increase the maximum operating speed by approximately 40 % [17]. When MC_1 is logic high, FF_2 is disabled and the input CLK is divided by two. When the MC_1 is set to low, FF_2 is enabled and the CLK is divided by three. The simulation plot is shown in Fig. 4-22.

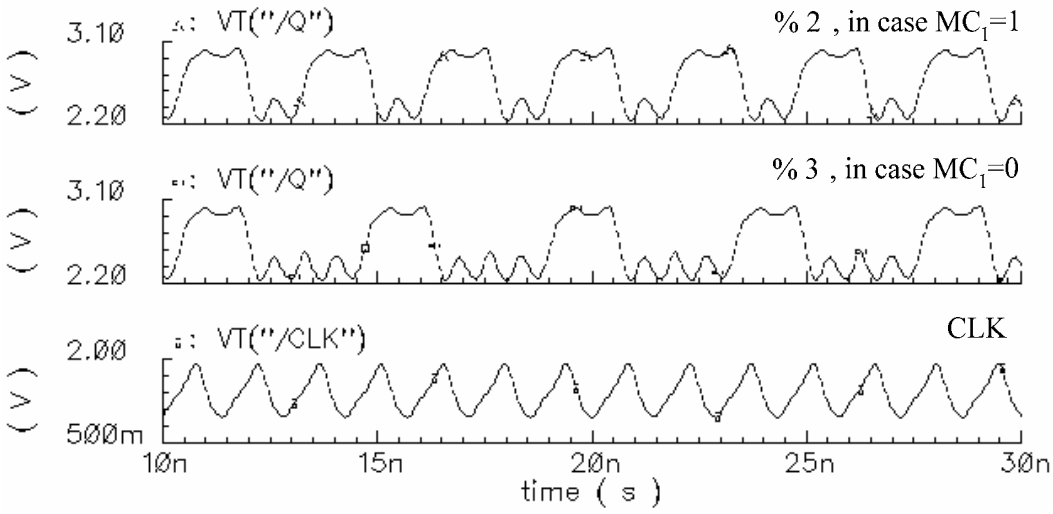


Fig. 4-22. Simulation of the divide-by-2/3 circuit

Another advantage coming from the divide-by-2/3 circuit is the simple structure because a CML NOR gate can be easily merged into an input differential pair of the CML DFF. The combinational CML of a NOR and a DFF is realized as depicted in Fig. 4-22, where V_R is the bias voltage which has the mid-point level of the two differential input swings, V_A and V_B.

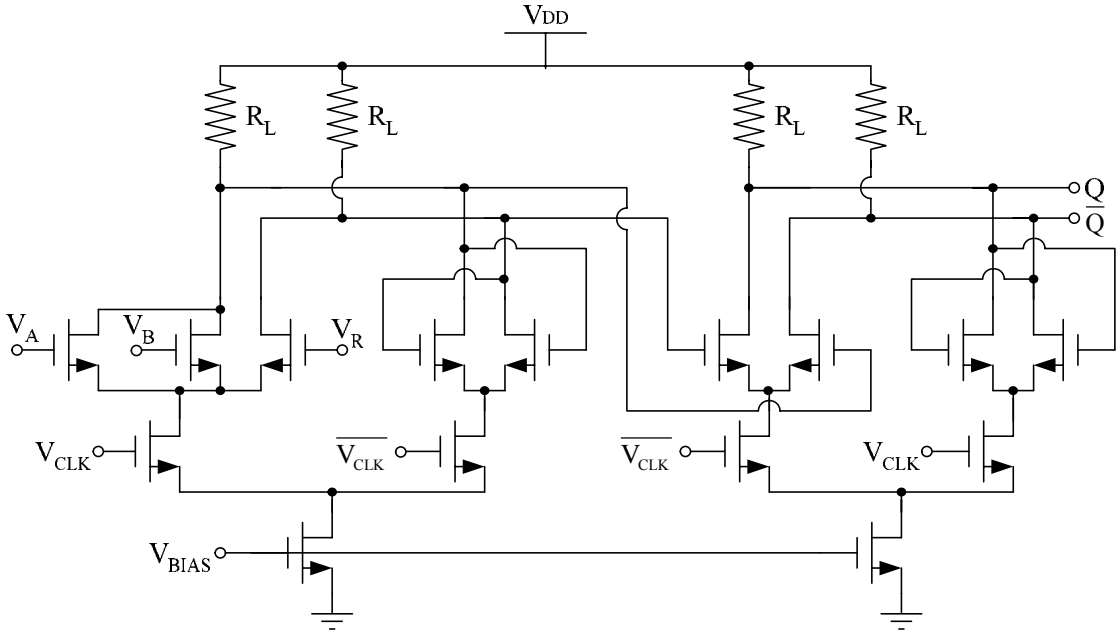


Fig. 4-23. Combinational CML of NOR and DFF

Designing the transistor sizes of the CML DFF is critical in a low voltage application because three transistors and one resistor are in series from V_{DD} to ground as shown in Fig. 4-23, so each transistor size should be carefully designed in a low voltage application. Even if a large tail current increases the switching speed, the large size also increases the parasitic capacitance at the output so that the overall speed decreases. On the other hand, a small size requires a large V_{DSsat} which can result in biasing problems. Usually latch differential pair can be designed with a smaller size than that of the input differential pair.

A divide-by-2 circuit in Fig. 4-20 consists of a DFF as shown in Fig. 4-24, which includes two CML D latches. The circuit diagram of the CML D latch is shown in Fig. 4-25.

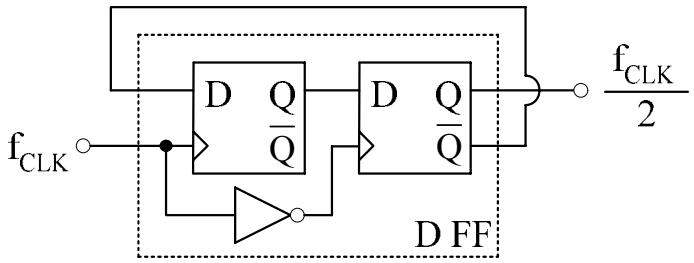


Fig. 4-24. Divide-by-2 circuit

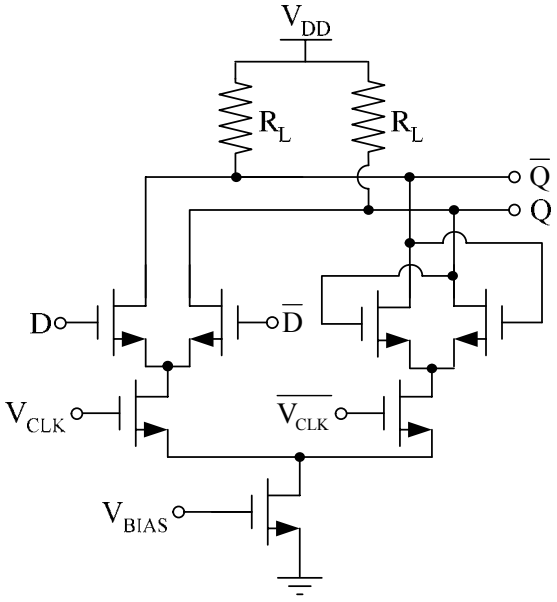


Fig. 4-25. CML D latch

Fig. 4-26 shows the 8/9 prescaler (see Fig. 4-20) simulation result when the modulus control (MC) signal is high. The MC signal is provided by the digital swallow counter. When the MC is high, the divide-by-2/3 does not change its divider ratio

because the high value of the MC signal forces MC_1 of divide-by-2/3 to be high. Therefore the prescaler works like a divide-by-8 circuit.

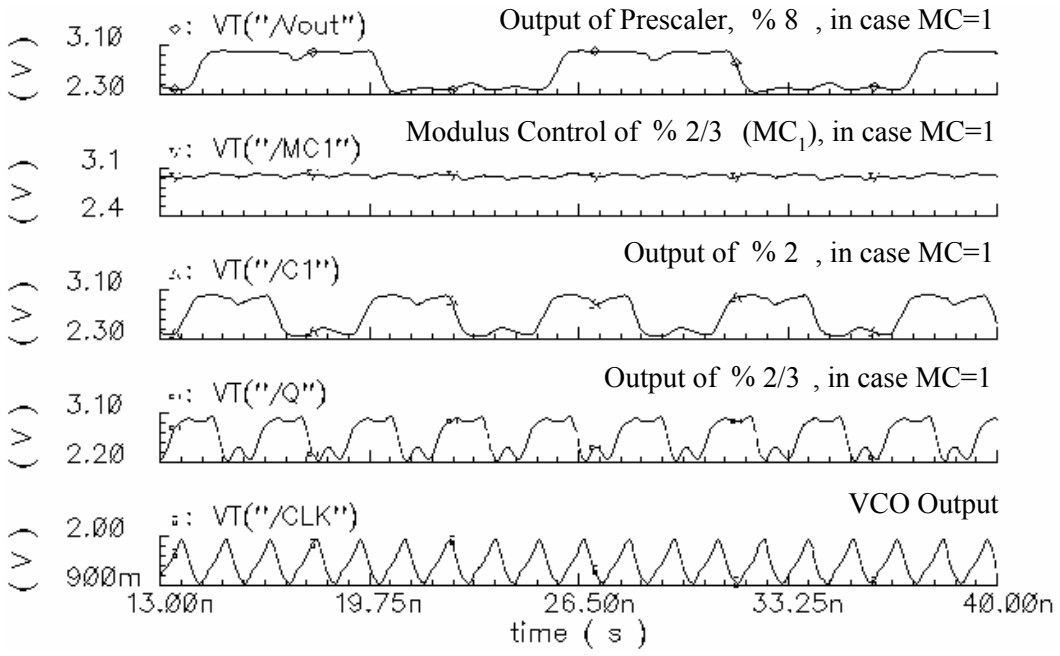


Fig. 4-26. 8/9 prescaler simulation when MC=1

Fig. 4-27 shows the 8/9 prescaler simulation result when the MC signal is low. Since MC is low, the divide-by-2/3 circuit can change its divider ratio depending on the level of MC_1. The prescaler divides the input signal by two when MC_1 is high. Among the 4 cycles of the divide-by-2/3 outputs in Fig. 4-26, the first 3 outputs are the results of the divide-by-2 operation and the last one cycle of the outputs is the result of the divide-by-3 operation. Thus, one cycle of the prescaler contains 9 cycles of the input signal.

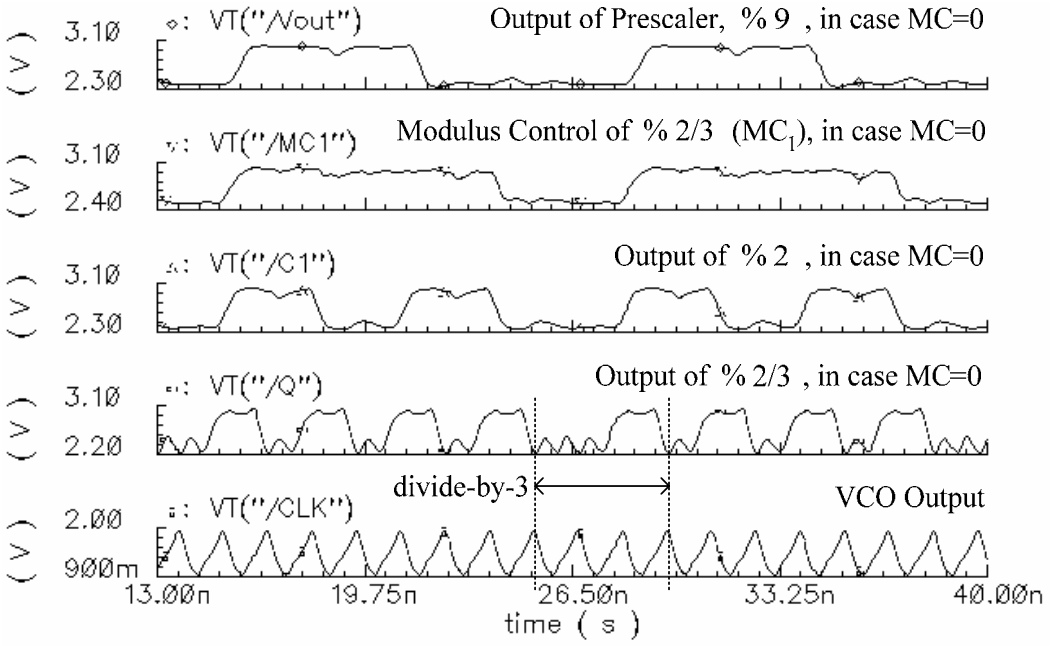


Fig. 4-27. 8/9 prescaler simulation when MC=0

The prescaler output is still an analog signal, so it can not drive directly the digital counters. In order to feed its output to digital counters, a comparator is needed. A single ended operational transconductance amplifier (OTA) structure is used as a comparator as shown in Fig. 4-28, where two inputs of Q and $\overline{Q}$ are the complementary signals coming from the prescaler, and OUT is the digital pulse which will be fed to both the program and swallow counters.

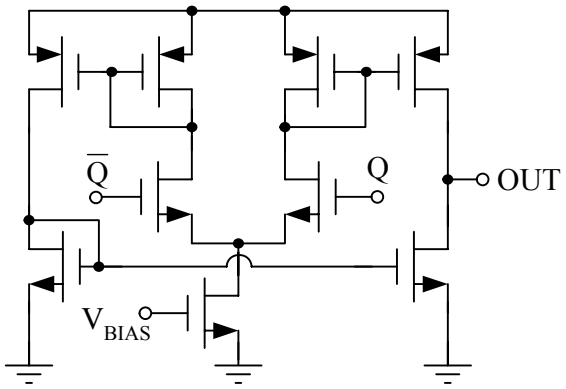


Fig. 4-28. Single ended OTA

Fig. 4-29 shows the VCO output and the output pulse of the combined circuit of the 8/9 prescaler and single ended OTA. The combined circuit of the prescaler and single ended OTA divides the VCO output by 8 or 9 depending on the MC.

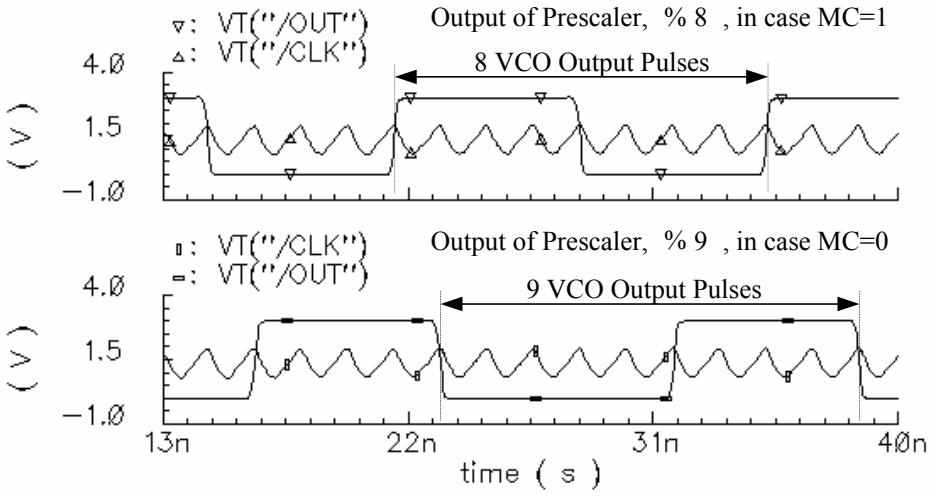


Fig. 4-29. Simulation of the 8/9 prescaler with the single ended OTA

4.5.2 Digital counters

The unit block of the digital counter is a divide-by-2 circuit shown in Fig. 4-24. However, the input frequency is low so that the D latches in Fig. 4-24 can be replaced by the conventional digital circuits. The program counter has 10 bits, so 10 DFFs are used in series. The swallow counter has 9 bits.

Based on the experimental results in [8], the maximum frequency, up to which an ITCP current can sustain its linearity with the gate pulse frequency, is almost 10 MHz in the AMIS 0.5 μm CMOS technology. Since the output frequency of the divider is exactly the same as the reference frequency in steady state and the reference frequency is 100 KHz, the input frequency of the sixth DFF from the output of the program counter is 6.4 MHz in steady state. This clock signal can be used as the gate pulse frequency for the ITCPs in both the charge pump and the active resistor in the loop filter. The DFF has two outputs Q and $\overline{Q}$ so that the complementary gate pulses for the ITCP can be extracted easily.

Any direct connection from one of the internal nodes of the program counter to the ITCPs results in a loading effect, so additional DFF is inserted for the complementary gate pulses without significant delay in the main signal path of the program counter as shown in Fig. 4-30. Totally four 6.4 MHz gate pulses are extracted from the program counter. One pair of the extracted complementary pulses is used for the ITCPs in the charge pump and the other is used for the ITCP in the active resistor.

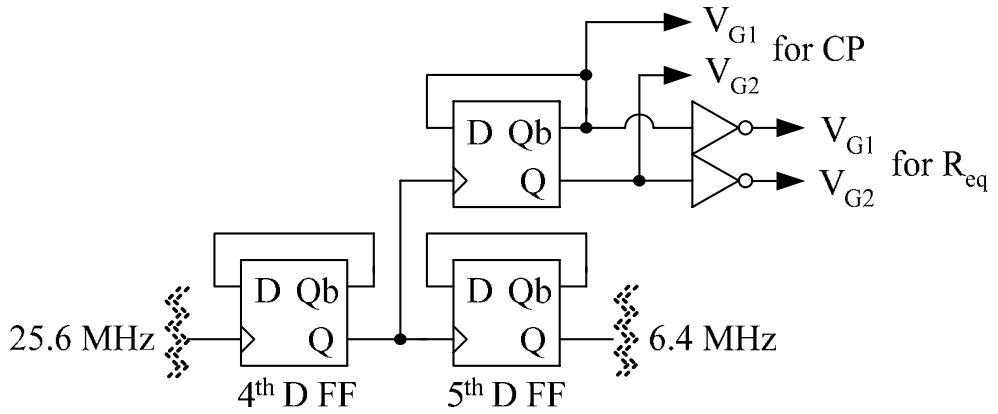


Fig. 4-30. Complementary gate pulses extraction from program counter

Fig. 4-31 shows the simulation plot of the program counter output and two high frequency pulses for the ITCP with 100 MHz input.

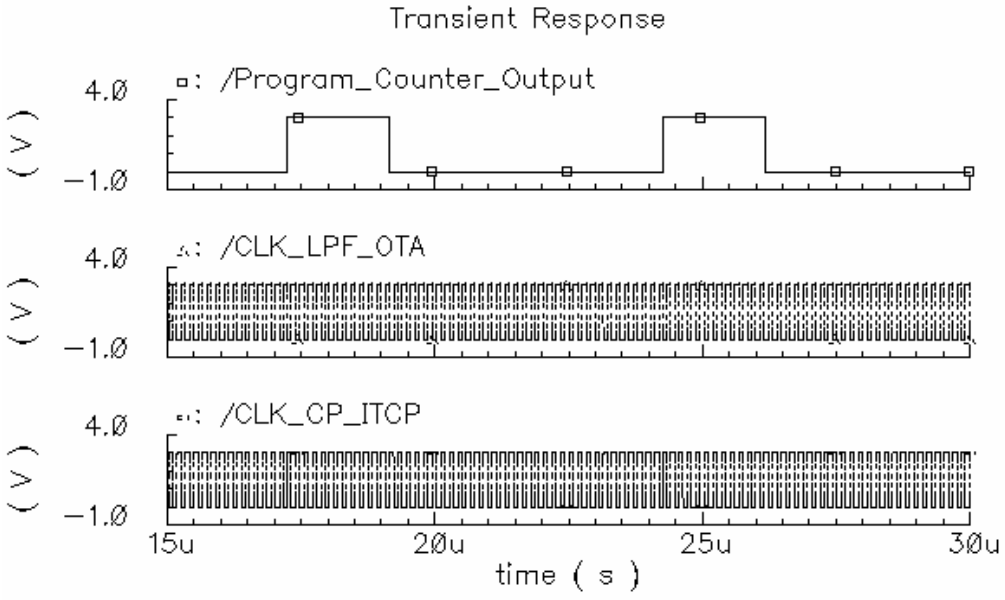


Fig. 4-31. Simulation of the program counter

Even though the frequency of both V_{G1} and V_{G2} will settle to 6.4 MHz at steady state, it shows some variation during the transient response time according to the VCO frequency variation. Since the frequency synthesizer has a 30 MHz output frequency range, the frequency variation of both V_{G1} and V_{G2} are approximately 320 KHz, which results in about 5 % I_P variation in the ITCP of the charge pump.

CHAPTER V

COMPACT FREQUENCY SYNTHESIZER

5.1 ITCP current test

A preliminary chip for testing the ITCP current generator was fabricated using AMIS 0.5 μm double-poly three-metal (2P3M) CMOS technology in February, 2003.

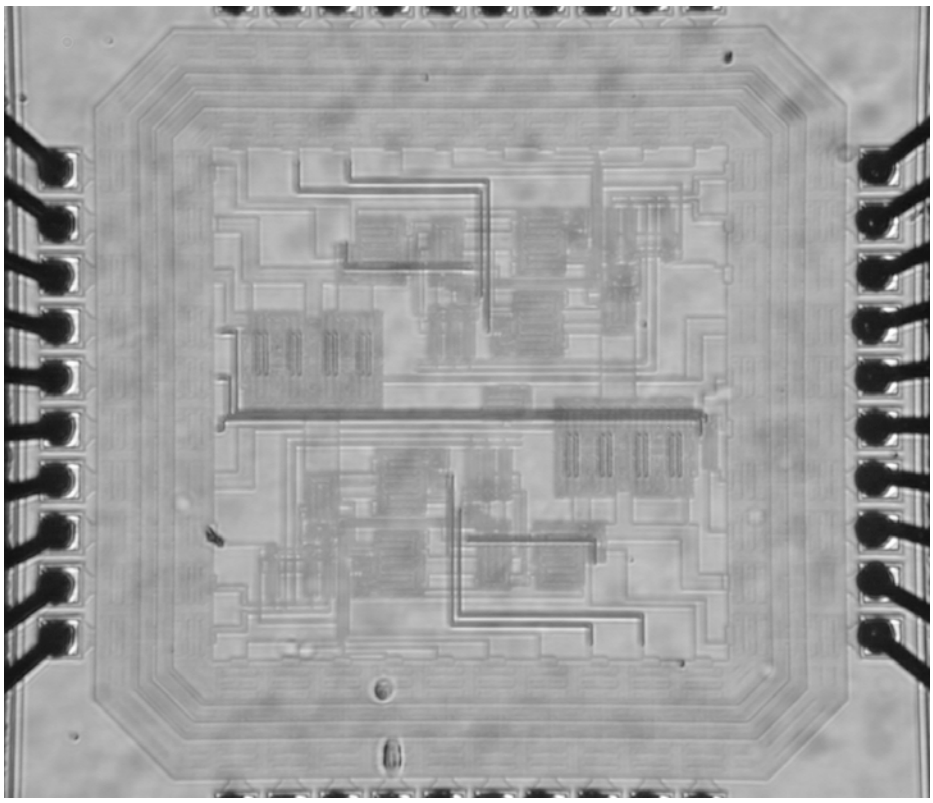
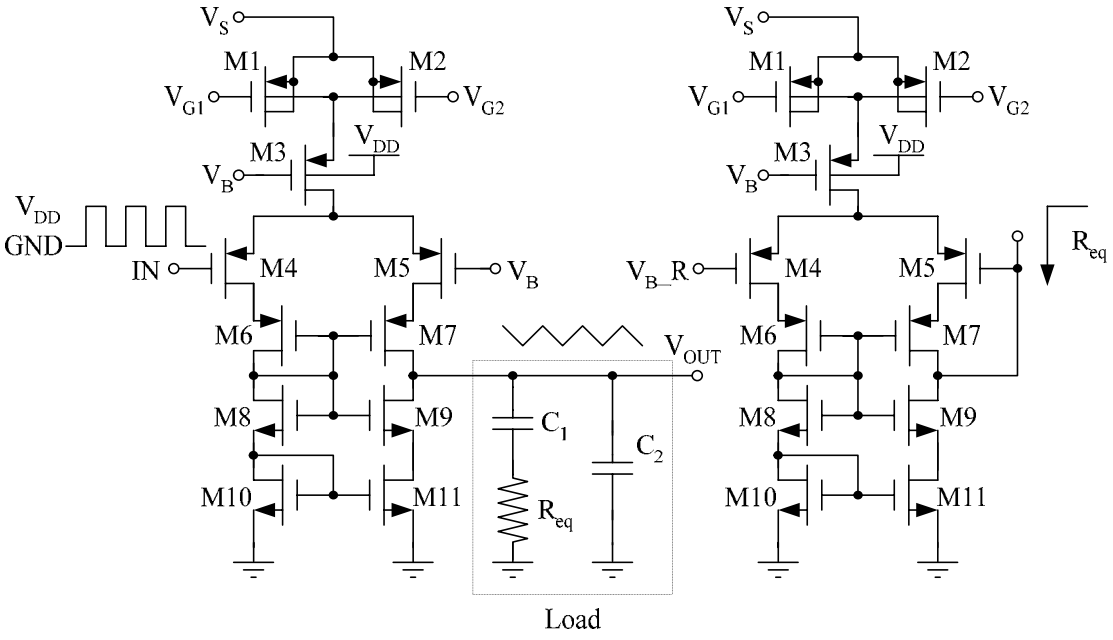


Fig. 5-1. Microphotograph of the preliminary chip

Even if the interface trap charge pump (ITCP) current and their applications such as a tunable low pass and band pass filter were tested and characterized in [8]-[9], the preliminary chip shown in Fig. 5-1 was designed for testing the switching capability and controllability of a nano-ampere level current in a digital environment. It included an operational transconductance amplifier (OTA) type current steering circuit as shown in Fig. 5-2.



(a) OTA with the loop filter (b) Active resistor in a cascode type

Fig. 5-2. Test circuit diagram

Since the pulse feedthrough effects can be serious enough to overwhelm a small ITCP current, any switching transistor can not be directly inserted in the current path. Thus, the OTA type current steering circuit is used for charging or discharging the load. In Fig. 5-2, in case the input is high, the PMOS transistor M4 is turned off so that all the transistors except M5 and M7 are turned off, and the ITCP current charges the load. In case the input is low, the current mirror consisting of M8, M9, M10, and M11 extracts the charge from the load.

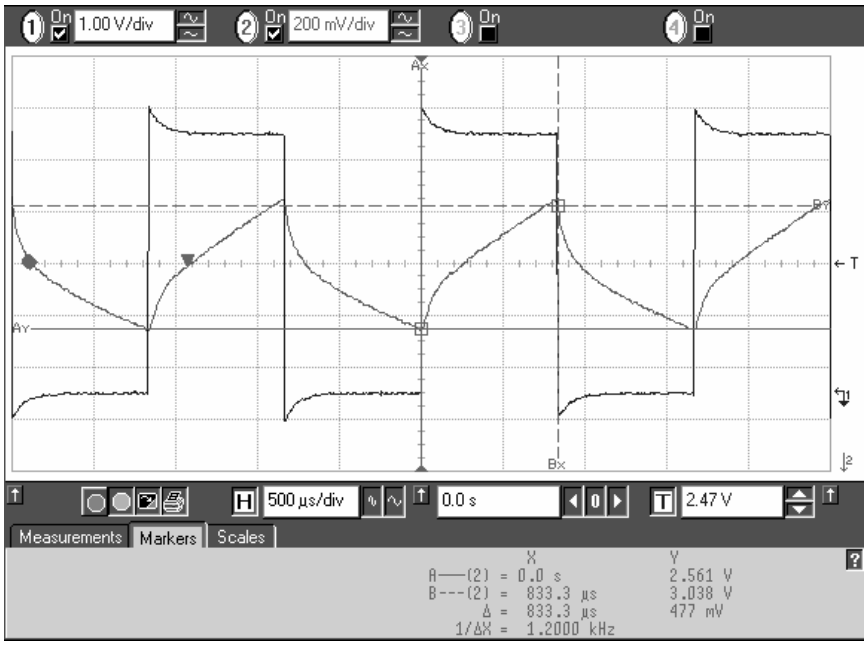


Fig. 5-3. Test result with f_{IN}=1 KHz

The test result in Fig. 5-3 shows the overlapped picture of the input and output. Since the ITCP current can not be simulated properly in the transistor level, the test result in Fig. 5-3 is useful to show the existence of the ITCP current.

5.2 Simulation results of the presented frequency synthesizer

All of the building blocks are incorporated in the frequency synthesizer. The VCO and divider are high speed parts based on the VCO output frequency, whereas the other blocks are based on low speed parts based on the loop bandwidth. As a result, the settling time depends on the loop bandwidth as shown in Equ. 2-2 and 2-3, but the required simulation time step should be determined by the VCO oscillation frequency.

Since it is almost impossible to simulate the whole frequency synthesizer due to the limitation on the memory space as well as the simulation time, the following simulation results are based on the PLL setup. All the high speed blocks were simulated and checked together in Chapter IV. Thus, the proper operation of the frequency synthesizer can be guaranteed if the stability condition of the PLL is satisfied under the maximum and minimum gain variations of the VCO and divider.

The step response of the control voltage is shown in Fig. 5-4. Since the control voltage directly changes the frequency of the VCO, the straight line of the control voltage after the initial transition time means that the loop has entered the phase locked condition. The initial condition of the control voltage is 1 V, and the final value in steady state is 1.028 V in Fig. 5-4, at which the combined gain of the VCO and the divider shows the average value of 140 KHz/V.

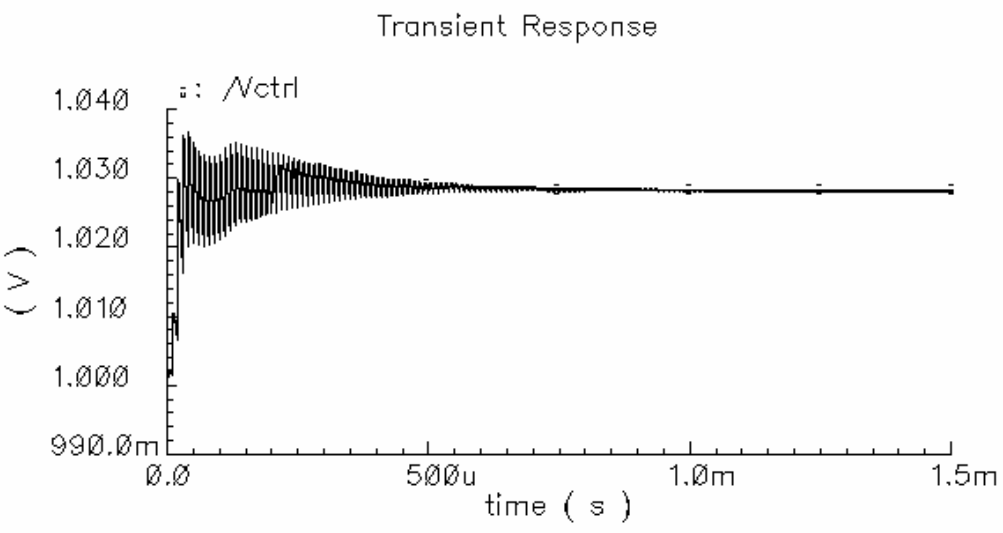


Fig. 5-4. Step response of the control voltage

Fig. 5-5 compares the responses between the ideal and presented frequency synthesizer case.

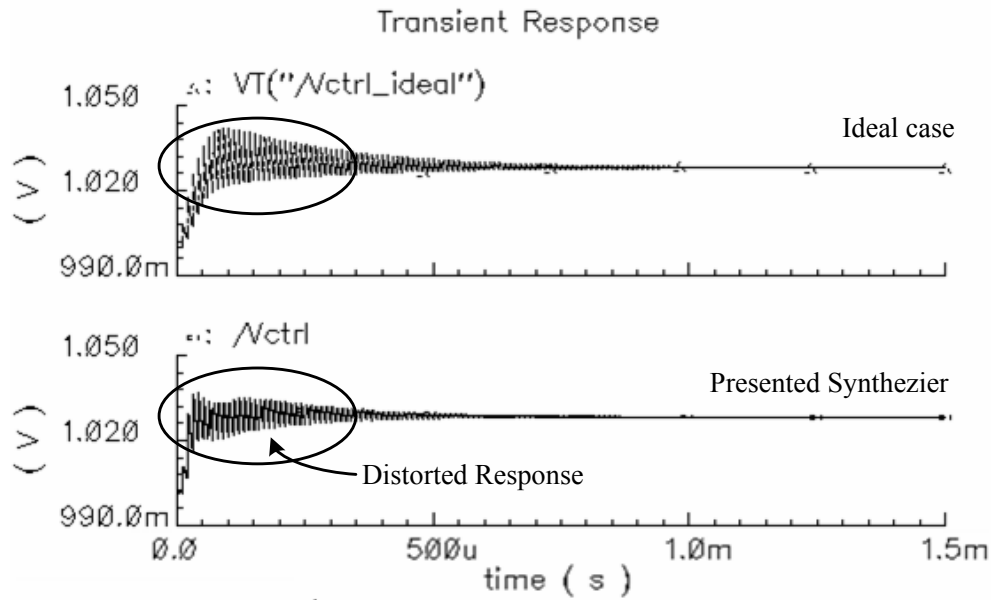


Fig. 5-5. Ideal PLL vs. presented frequency synthesizer

The output node of the active resistor is connected to the control voltage node through the capacitance C_1 in the loop filter. Thus, C_1 will separate the output node of the active resistor from the control voltage node in steady state, whereas any change of the control voltage node modulates the output node of the active resistor through the C_1. Due to the fluctuation of the output node voltage as shown in Fig. 5-6, the equivalent resistance of the active resistor varies and results in the distorted response in the presented frequency synthesizer, comparing with the ideal case as shown in Fig. 5-5.

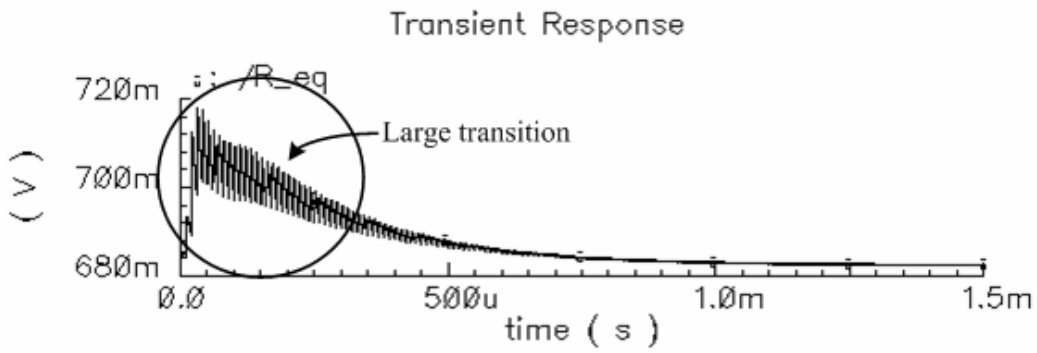


Fig. 5-6. Transient response of the output node voltage of the active resistor

In steady state, the control voltage contains the two non-ideal signals. One is the low frequency ripple due to the PFD dead-zone problem and the other is the high frequency ripple due to the active resistor. Fig. 5-7 shows the zoomed-in plot of the control voltage response which shows both high and low frequency ripples.

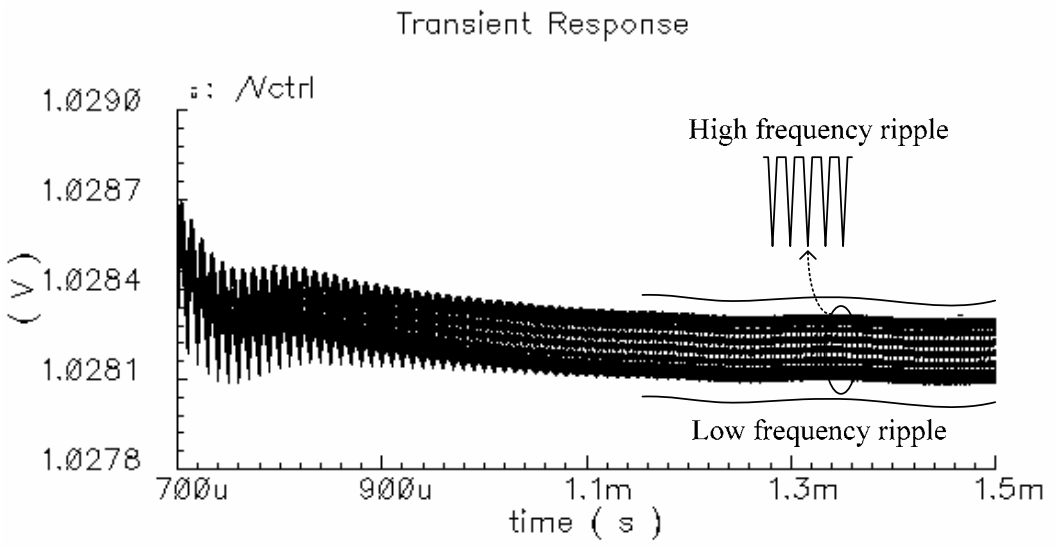


Fig. 5-7. Zoomed-in plot of the control voltage in steady state

The settling time is about 1.2 ms at which 100 KHz correction signal disappears and random variations become dominant in Fig. 5-7. The correction signal frequency is the output of the PFD, so it is exactly the same as the reference frequency, 100 KHz. After the phase difference between the reference and feedback signal is below a certain value, a low frequency ripple appears because of the dead-zone problem. Since the low frequency ripple is random, its frequency and amplitude are difficult to predict. Fig. 5-8 shows the zoomed-in plot of the low frequency random signal on the control voltage.

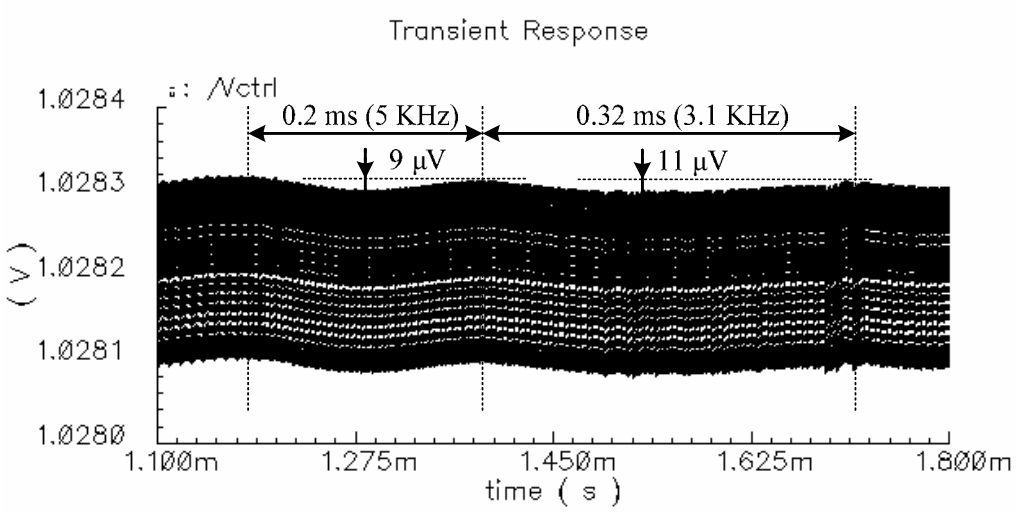


Fig. 5-8. Low frequency ripple on the control voltage

Considering the random variation of the low frequency ripple as an uncorrelated PFD noise source, the mathematical model can be constructed as shown in Fig. 5-9.

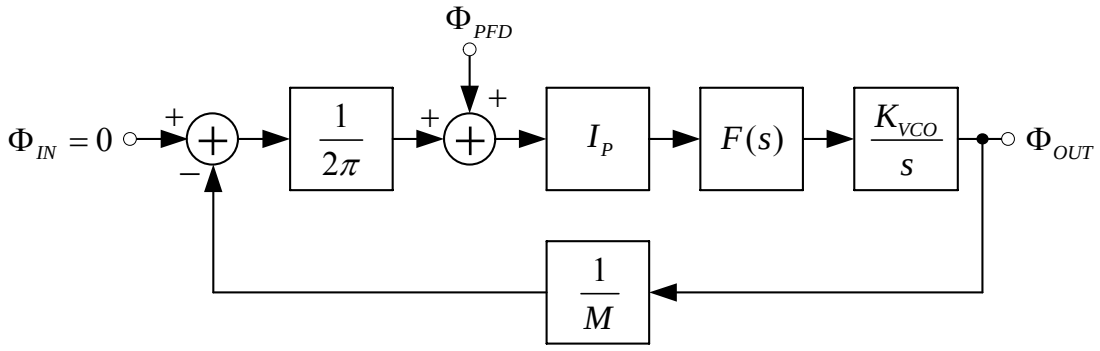


Fig. 5-9. Linear model for the low frequency ripple

The main effect of the low frequency ripple is the phase variation at the VCO output. The transfer function from the Φ_{PFD} to Φ_{OUT} is:

$$\frac{\Phi_{OUT}}{\Phi_{PFD}}(s)=\frac{2\pi MI_P K_{VCO}\left(sR_1C_1+1\right)}{s^3 2\pi MR_1C_1C_2+s^2 2\pi M\left(C_1+C_2\right)+sI_P K_{VCO}R_1C_1+I_P K_{VCO}} \qquad (5\text{-}1)$$

The low pass nature of the above transfer function indicates that any slow frequency jitter components will directly modulate the VCO output phase but the fast random variations will be suppressed. Fig. 5-10 shows the magnitude response in which the DC gain is about 91.5 dB and the -3dB frequency is 5.43 KHz.

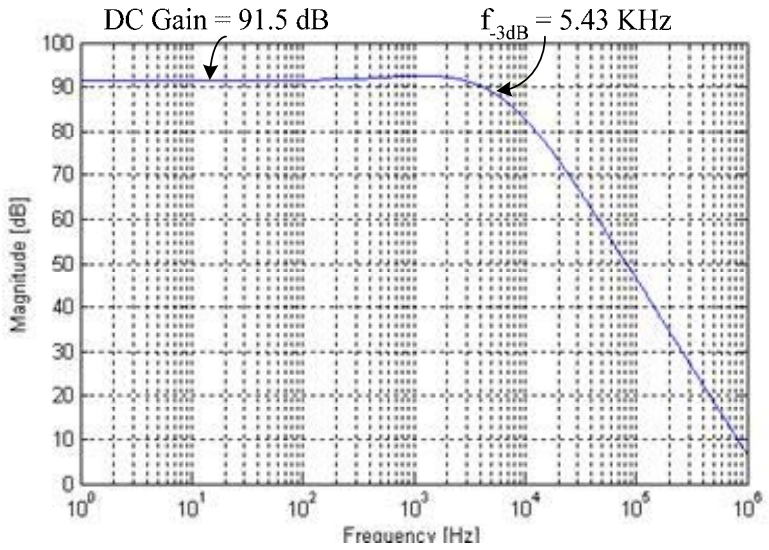


Fig. 5-10. Magnitude response of the low frequency ripple

Based on the magnitude response in Fig. 5-10 and the narrow band FM modulation theory [18], the expected VCO output frequency variation due to the low frequency ripple on the control voltage is shown in Fig. 5-11.

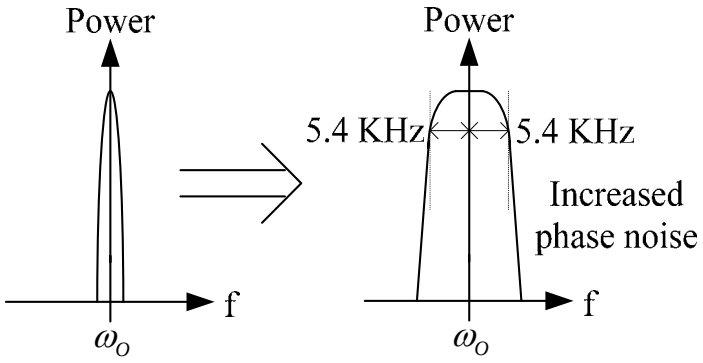


Fig. 5-11. Effect of the low frequency ripple in the frequency domain

Another non-ideal signal overlapped on the control voltage in Fig. 5-7 is the high frequency ripple, and its zoomed-in plot is shown in Fig. 5-12.

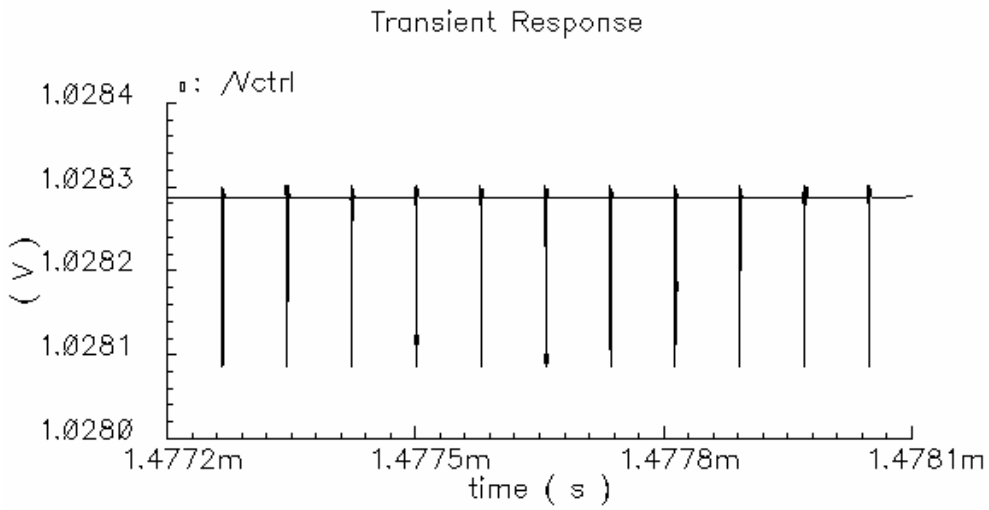


Fig. 5-12. Zoomed-in plot of the high frequency ripple

The active resistor consists of an OTA in unity gain feedback configuration. To reduce the transconductance of the OTA, an ITCP current generator is used as a tail current source. Since the active resistor is a continuous time block, two complementary pulses from the program counter always stimulate the ITCP, and the pulse feedthrough affect the output node through the C_1. The high frequency ripple on the control voltage with the complementary gate pulses are shown in Fig. 5-13.

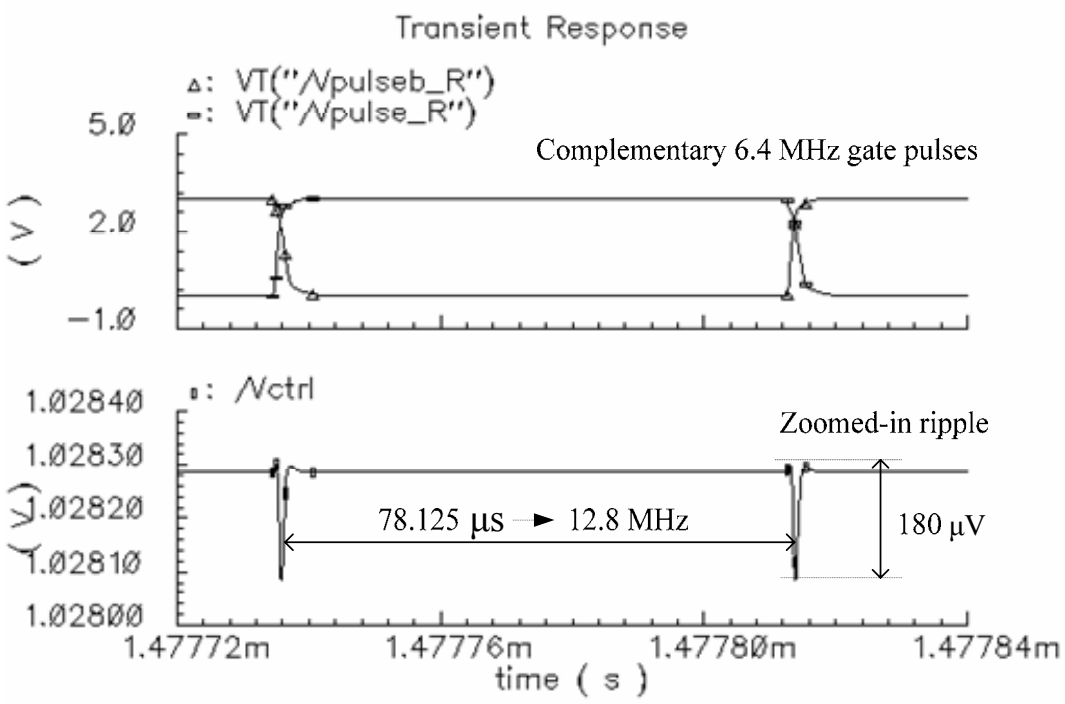


Fig. 5-13. Pulse feedthrough resulting from the active resistor

The peaking shown in Fig. 5-13 can be divided in two parts. The down-direction peaking occurs when the gate pulse starts to fall from V_{DD} because the strongly

accumulated electrons are pushed from the channel to the well terminal. On the other hand, the up-direction peaking occurs when the gate pulse rises from ground because the electrons are extracted from the well terminal. Small mismatch in the rising and falling time between the two complementary pulses results in the pulse feedthrough so that the periodic high frequency ripple on the control voltage exits in steady state as shown in Fig. 5-13.

One more interesting observation is that the frequency of the peaking becomes twice that of the gate pulses because every overlap between the rising and falling transition happens twice within one gate pulse cycle. Since the high frequency ripple resulting from the active resistor is periodic, the frequency spur will be shown in the frequency spectrum at 12.8 MHz away from the center frequency. The power level of the frequency spur can be also predicted by:

$$20 \cdot \log\left(\frac{V_P \cdot K_{VCO}}{2 \cdot \omega_{SPUR}}\right) = -45 \ dBc \qquad (5\text{-}2)$$

Equ. 5-3 indicates that the power of the frequency spur is about 45dB below the center frequency. Moreover, the spur is located 12.8 MHz away from the center frequency, so it can be suppressed more by an additional filter. Fig. 5-14 shows the expected frequency spectrum of the VCO output in steady state.

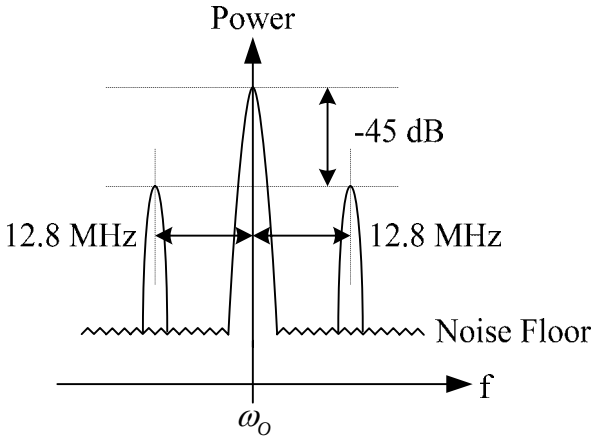


Fig. 5-14. Effect of the high frequency ripple in the frequency domain

Even though the combined gain of the VCO and divider is almost constant after the PLL has settled, the variation of the VCO gain can make the system less stable during the initial transition. The transient responses using the maximum and minimum values of the combined gain of the VCO and divider are shown in Fig. 5-15 and 5-16.

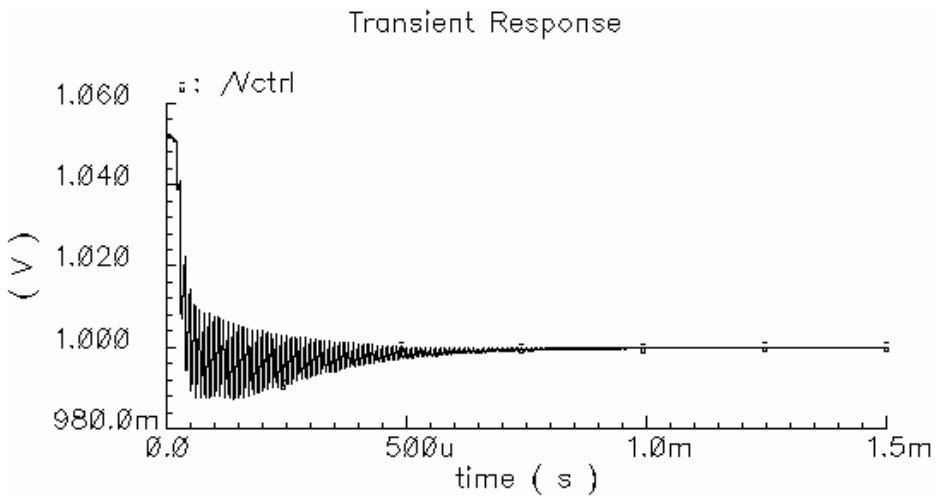


Fig. 5-15. Settling response of the maximum $(K_{VCO}/M)_{MAX}$, 170 KHz/V case

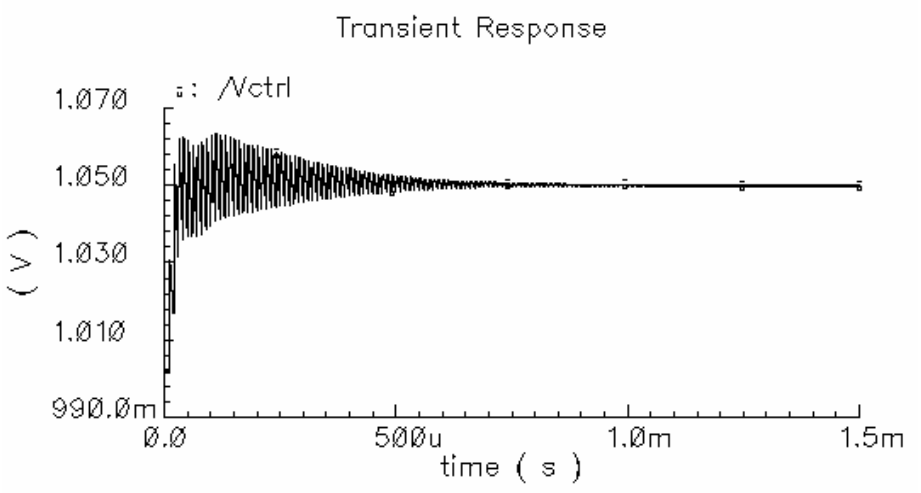


Fig. 5-16. Settling response of the minimum $(K_{VCO}/M)_{MIN}$, 110 KHz/V case

As derived in Section 4.2, the $(K_{VCO}/M)_{MAX}$ is about 170 KHz/V when the control voltage is 1 V and the $(K_{VCO}/M)_{MIN}$ is about 110 KHz/V when the control voltage is 1.05 V. The total variation is about $\pm 20\%$ from the design value of 140 KHz/V. As shown in Fig. 5-15 and 5-16, the PLL shows a stable step response under the conditions of both the maximum and minimum values because the phase response was designed with a sufficient margin of the stability.

Fig. 5-17 shows the control voltage response of the extreme case, in which the variation of the frequency steps is maximized. The control voltage changes from the minimum value of 1 V to the maximum value of 1.05 V, which corresponds to the VCO frequency from 570 MHz to 600 MHz.

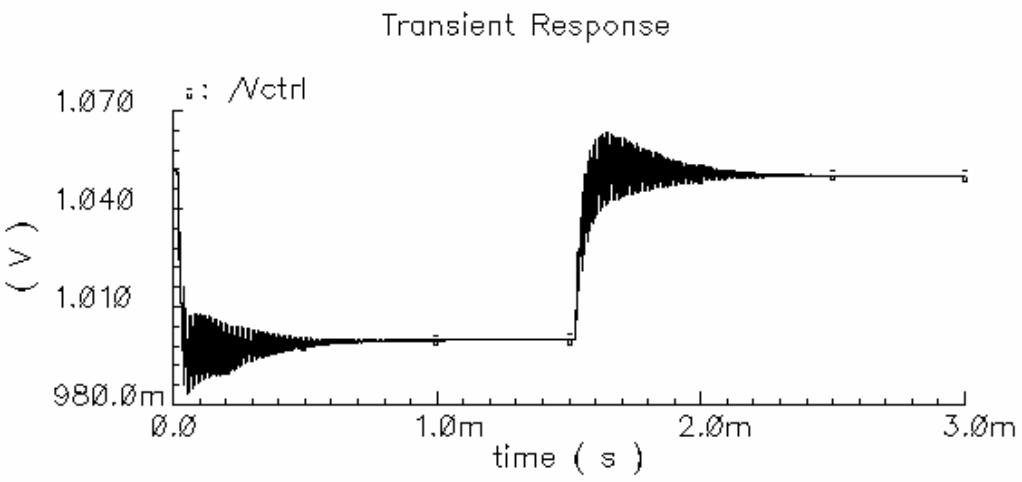


Fig. 5-17. Maximum frequency switching simulation

Total current consumption of the presented frequency synthesizer is 8.9 mA where 3 V single power supply is used. The fast building blocks, which include the VCO, VCO buffer, and prescaler, consume more than 90 % of the total power consumption. The current consumptions for each part are summarized in Table 5-1.

Table 5-1. Current consumption summary

Block	Current Consumption	Percentage
VCO	3.7 mA	41.6 %
Prescaler	3.1 mA	34.8 %
VCO Buffer	1.3 mA	14.6 %
LF Buffer	0.1 mA	1.1 %
PFD, CP, LF, Counters	0.7 mA	7.9 %
Total	8.9 mA	100 %

Total layout including pads is shown in Fig. 5-18, in which two frequency synthesizers are included and the bottom block is for the presented frequency synthesizer. The total layout size of the presented frequency synthesizer is about 0.3 mm^2 (0.8 mm × 0.38 mm) excluding the pads.

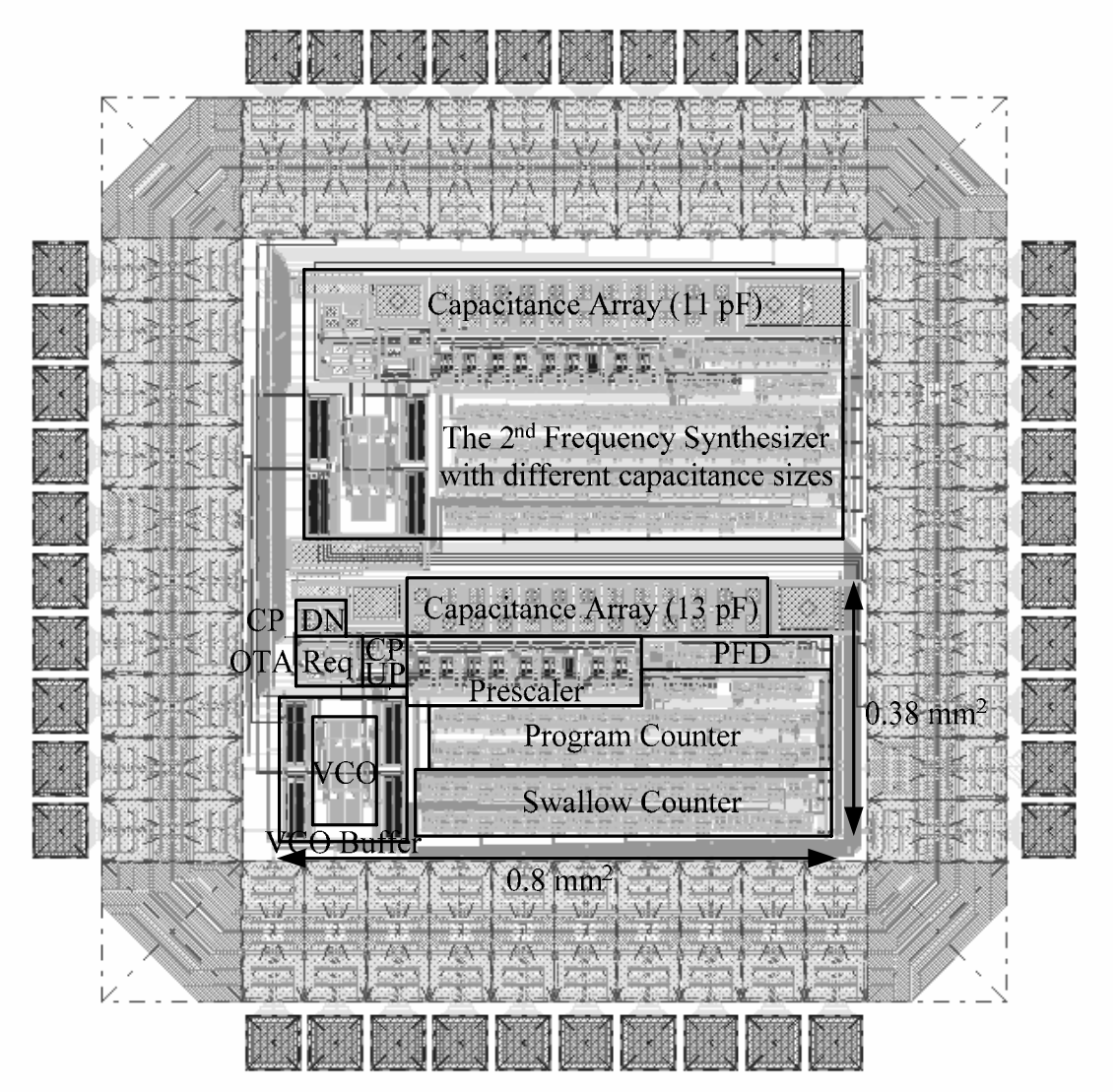


Fig. 5-18. Layout of the presented frequency synthesizer including pads

Table 5-2. Area consumption summary

Block	Silicon Area	Percentage
Program counter	0.059 mm^2	19.6 %
Swallow counter	0.052 mm^2	17.4 %
Capacitors in LF	0.040 mm^2	13.3 %
Prescaler	0.027 mm^2	9.1 %
VCO buffer	0.021 mm^2	7.0 %
VCO	0.012 mm^2	4.0 %
PFD and Interface block	0.008 mm^2	2.7 %
Charge pump	0.006 mm^2	2.1 %
Active resistor	0.005 mm^2	1.7 %

Since the capacitance is reduced by adopting the ITCP current generators, the digital counters become the biggest building blocks in the presented frequency synthesizer in Table 5-2. The 13 pF capacitance including both C_1 and C_2 occupied only 0.04 mm^2 which is 13.3 % of the total area.

Table 5-3 compares the presented frequency synthesizer with the state-of-art frequency synthesizers. The presented frequency synthesizer is the smallest one even though it used the AMIS 0.5 μm CMOS technology and the reference frequency is 100 KHz.

Table 5-3. Comparison

Design	Reference Frequency	Frequency Range	Total Area	Total Power	Used Technology
Shu [19] Mar. 2004	256 MHz	2.4 – 2.5 GHz	3.7 mm^2	49.5 mW	0.35 μm CMOS
Pellerano [20] Feb. 2004	10 MHz	5.14 – 5.7 GHz	0.6 mm^2	33.8 mW	0.25 μm CMOS
Chen [21] Jan. 2004	5 MHz	3.74(1.87) – 4.6(2.3) GHz	3.5 mm^2	80 mW	0.35 μm CMOS
Ahola [22] Jan. 2004	13 MHz	2 GHz Range	2.2 mm^2	22.6 mW	0.35 μm CMOS
This work	100 KHz	570 – 600 MHz	0.3 mm^2	26.7mW	0.5 μm CMOS

CHAPTER VI

CONCLUSIONS

A compact integer-N frequency synthesizer for the self calibration of RF circuits is presented. The main idea comes from the fact that a small charge pump current can reduce a passive capacitance without changing the loop gain. In order not to sacrifice other loop parameters, the resistance in the loop filter should be linearly increased as the capacitance decreases. The active resistor using an OTA is suggested. A small transconductance OTA is built with the help of a small tail current supplied by an ITCP current source.

A critical drawback of incorporating the ITCP current generator into the frequency synthesizer is the asymmetry in the charge pump block. The source and sink current of the charge pump have different structures because of the discrepancy between I_S and I_P of the ITCP. Another disadvantage comes from the interface block between the ITCPs of the charge pump and PFD. Since any delay element is not inserted in the PFD due to the size and current mismatch problems, the VCO output suffers from the jitter problems.

Finally, the layout of the presented frequency synthesizer shows that it requires only 0.3 mm^2 silicon area without any external components. Since the ITCP current makes small capacitance be enough for the loop filter, two digital counters become the largest blocks. The passive capacitance is 13 pF in total and occupies 13.3 % of the total silicon area.

REFERENCES

[1] Y. Chang, J. Wills, and J. Choma, "On-chip automatic direct tuning circuitry based on the synchronous rectification scheme for CMOS giga-hertz band front-end filter," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. 4, 2001, pp. 246-249.

[2] H. Liu and A. I. Karsilayan, "An accurate automatic tuning scheme for high Q continuous time bandpass filters based on amplitude comparison," *IEEE Trans. Circuits and Syst. II*, vol. 50, no. 8, pp. 415-423, August 2003.

[3] T. Sumesaglam and A. I. Karsilayan, "A digital approach for automatic tuning of continuous time high-Q filters," *IEEE Trans. Circuits and Syst. II*, vol. 50, no. 10, pp. 755-761, October 2003.

[4] J. Turin, Fluence technology Inc., "Built-in self-test, digital ATE team up," Electronic News, December 2000.

[5] C. K. Ong, K. T. Cheng, and L. C. Wang, "Delta-sigma modulator based mixed-signal BIST architecture for SOC," *Design Automation Conference,* 2003*, Proceedings of the ASP-DAC* 2003*. Asia and South Pacific*, pp. 669-674, January 2003.

[6] M. Mendez-Rivera, J. Silva-Martinez, and E. Sanchez-Sinencio, "On-chip spectrum analyzer for built-in testing analog ICs," *IEEE Int. Symp. Circuits and Systems 2002,* vol. 5, pp. V61-64, May 2002.

[7] J. S. Brugler and P. G. A. Jespers, "Charge pumping in MOS devices," *IEEE Trans. Electron Devices,* vol. 16, pp. 297-302, 1969.

[8] U. Cilingiroglu, A. Becker-Gomez, and K. T. Veeder, "An evaluation of MOS interface trap charge pump as an ultra constant current generator," *IEEE J. Solid State Circuits*, vol. 38, pp. 71-83, January 2003.

[9] A. Becker-Gomez, U. Cilingiroglu, and J. Silva-Martinez, "Compact sub-hertz OTA-C filter design with interface trap charge pump," *IEEE J. Solid State Circuits*, vol. 38, pp. 929-934, June 2003.

[10] B. Razavi, "RF microelectronics," Prentice Hill, 1997.

[11] F. M. Gardner, "Charge pump phase locked loops," *IEEE Trans. Comm.*, vol. COM-28, pp. 1849-1858, November 1980.

[12] D. K. Jeong, G. Borriello, D. A. Hodges, and R. H. Katz, "Design of PLL-based clock generation circuits," *IEEE Journal of Solid State Circuits,* vol. 27, pp. 1599-1607, November 1992.

[13] K. Shu, "Design of a 2.4 GHz CMOS monolithic fractional-N frequency synthesizer," Ph. D. dissertation, Texas A&M University, College Station, 2002.

[14] C. A. Sharpe, "A 3-stage phase detector can improve your next PLL design," *EDN*, pp. 55-59, September 1976.

[15] B. Razavi, "Design of analog CMOS integrated circuits," McGraw Hill, 2001.

[16] U. Cilingiroglu, "Systematic analysis of bipolar and MOS transistors," Artech House, 1993.

[17] C. Lam and B. Razavi, "A 2.6 GHz/5.2 GHz frequency synthesizer in 0.4 μm CMOS technology," *IEEE J. Solid State Circuits*, vol. 35, pp. 788-794, May 2000.

[18] V. Manassewitsch, "Frequency synthesizers, theory and design," Wiley, 1987.

[19] Z. Shu, K. L. Lee, and B. H. Leung, "A 2.6 GHz ring oscillator based CMOS frequency synthesizer with a fractional divider dual-PLL architecture," *IEEE J. Solid State Circuits*, vol. 39, pp. 452-462, March 2004.

[20] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5 mW 5 GHz frequency synthesizer with dynamic logic frequency divider," *IEEE J. Solid State Circuits*, vol. 39, pp. 378-383, February 2004.

[21] W.-Z. Chen, J.-X. Chang, Y.-J. Hong, M.-T. Wong, and C.-L. Kuo, "A 2 V 2.3/4.6 GHz dual band frequency synthesizer in 0.35 μm digital CMOS process," *IEEE J. Solid State Circuits*, vol. 39, pp. 234-237, January 2004.

[22] R. Ahola and K. Halonen, "A 1.76 GHz 22.6 mW ΔΣ fractional-N frequency synthesizer," *IEEE J. Solid State Circuits*, vol. 38, pp. 138-140, January 2004.

APPENDIX

AHDL CODE FOR THE INTERFACE-TRAP CHARGE

As presented in Chapter III, an AHDL block is used for emulating the interface-trap charge transfer from the source to well terminal. The following code is the description of the AHDL block. The originality of the following code comes from Dr. Ugur Cilingiroglu and Feyza Berber in the Analog and Mixed Signal Center in Texas A&M University.

```
// Spectre AHDL for Interface-Trap Charge
module trap_charge_pump(v_cco, iout,  vsrc)
  (Nit,area,vtrans_high,vtrans_low,tdel,trise,tfall)
node [V, I] v_cco, iout, vsrc;
parameter real Nit=2e14 from [0:inf);
parameter real area=3.33e-12 from [0:inf);
parameter real vtrans_high = 1.8 from [0:inf);
parameter real vtrans_low = 0.9 from [0:inf);
parameter real tdel=0 from [0:inf);
parameter real trise=1f from (0:inf);
parameter real tfall=1f from (0:inf);
```

```
{
  real iout_val;
  parameter real q=0.16a;
  real t1=0;
  real pulse_width=1;
  //real high_rising = 0;
  //real low_rising = 0;
  //real high_follows_low = 0;
  analog {
    if ($threshold(V(v_cco) - vtrans_low, +1)) {
      //low_rising = 1;
      //if (high_follows_low == 1){
      iout_val =(q*area*Nit)/pulse_width;
      //high_follows_low = 0;
      //}
         t1=$time();
    }
    if ($threshold(V(v_cco) - vtrans_low, -1)) {
    //low_rising = 0;
    if(iout_val > 0){
    iout_val = 0;
    }
```

```
    }
    if ($threshold(V(v_cco) - vtrans_high, +1)) {
      //if(low_rising == 1){
      //high_follows_low = 1;
      //}
      iout_val =0;
        pulse_width= $time()-t1;
    }
    I(vsrc, iout) <- $transition(iout_val,tdel,trise,tfall);
  }
}
```

VITA

Sanghoon Park was born in Seoul, Republic of Korea. He received the Bachelor of Engineering degree in the school of electrical engineering from Korea University, Seoul, Republic of Korea, in 2000. Mr. Park was admitted to the graduate school of Texas A&M University, College Station, TX with a Texas Instrument (TI) scholarship in the fall of 2001. He received the Master of Science degree in the electrical engineering under the supervision of Dr. Aydin Ilker Karsilayan in the Analog and Mixed Signal Center (AMSC). His research areas are focused on the design of the analog RF circuits. He can be reached by E-mail, zeussh@yahoo.co.kr and his permanent address is 209 Geoyeo Donga APT 209-1102, Songpa Seoul 138-902, Republic of Korea.