FRONT-END CIRCUITS

FOR CHEMICAL AND MOLECULAR SENSING

A Thesis

by

YOUNGBOK KIM

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2005

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Sameer Sonkusale
Committee Members,	Laszlo Kish
	Jose Silva-Martinez
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ABSTRACT

Front -end Circuits

for Chemical and Molecular Sensing. (August 2005)

Youngbok Kim, B.S., Yonsei University

Chair of Advisory Committee: Dr. Sameer Sonkusale

This research demonstrates two building blocks for CMOS integrated sensor IC for molecular or chemical sensing. One of them for molecular sensing is the capacitance sensing circuit to detect the change of the dielectric constant of novel nanowell devices. The size of nanowell (10nm-100nm) enables high fidelity detection and analysis through Broadband Dielectric Spectroscopy (BDS) of the parallel-plate capacitor formed by the nanowell and the targeted molecules. The signal tranduction is done by a novel, continuous-time detection circuit using a low-noise lock-in architecture which generates the current output containing the information about the admittance of the sensor as a function of the frequency for BDS. This current signal is processed in the current domain by a low power current-mode A/D converter. The current signal transducer has a quasi-linear capacitance resolution of 164pA/aF (at 1Ghz) and power consumption of only 30uW in 0.18um TSMC CMOS technology.

Another building block is a low noise front end for feature extraction for gas and nanoparticle detection using Van der Waals sensors. The output of such a sensor consists of particle specific information in the low frequency range from 0 to 100 KHz in the form of stochastic fluctuations. Such detection schemes are termed as fluctuation enhanced sensing, which exploit the statistics of the noise in the low frequency spectrum. The front end consists of a low pass filter bank to process the amplified signal from a low-noise transimpedance amplifier. It handles the noise-like information signal from

the sensor with filters having increasing cut-off frequencies. It is designed to operate at temperature as high as 200C with low leakage currents to maximize the stochastic fluctuation noise generation. The front-end system was fabricated with TSMC 0.18um technology and tested. The gain of the front-end circuit is at least 87dB and its power consumption with one transimpedance amplifier and 10 filters is just 1.1mW. Moreover, the worst-case maximum input current signal is 0.2uApp while satisfying 5% THD and the equivalent input current noise level is under 7nA. The front-end circuit demonstrates the considerably high dynamic range with the low noise input range suitable for applications for sensing using fluctuation enhanced techniques.

ACKNOWLEDGMENTS

The search of knowledge is never ending. It is a journey that leads people to different directions in life. Sometimes the road is long and difficult, but it is the people that you come in contact with that make it all worth while.

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TABLE OF CONTENTS

Page

ABSTRACT iii

ACKNOWLEDGMENTS v

TABLE OF CONTENTS vii

LIST OF FIGURES x

LIST OF TABLES xiv

1. INTRODUCTION 1

1.1 Motivation 1
1.2 Objective of This Thesis 4

2. BACKGROUND 6

2.1 Chemical Sensing with Nanowell Capacitors 6
2.1.1 Fabrication of a Nanowell Capacitor 6
2.1.2 Broadband Dielectric Spectroscopy 9
2.2 Solid State Chemical Sensors 11
2.2.1 History of the Chemical Sensing [12] 11
2.2.2 MOSFET-based Sensor 11
2.2.2.1 Description 11
2.2.2.2 Van der Waals Force Enhanced MOSFET Sensor 13
2.2.2.2.1 Introduction 13
2.2.2.2.2 Motivation 14
2.2.2.2.3 Operational Concept of the Device 15
2.2.3 Thin-film Based Sensor and New Sensing Technique [8] 18
2.2.3.1 Concept of the Film Based Sensor 18
2.2.3.2 New Multiple Type Agents Sensing Technique 19
2.2.4 The Relationship between the Fluctuation Noise and Temperature 20
2.2.5 Summary 21

3. IMPLEMENTATION OF THE CIRCUITS 22

3.1 Nanowell IC Readout Circuit 22
3.1.1 System Description 22
3.1.2 Previous Results of Capacitance Sensing Circuit 23

Page

3.1.3 System Implementation of a Novel Capacitance Sensing Circuit.....24
3.1.3.1 Lock-in Technique.....25
3.1.3.2 Operational Concept of the Capacitance Sensing Circuit.....26
3.1.3.3 Building Block Design.....27
3.1.3.3.1 Common Mode Error Amplifier.....27
3.1.3.3.2 Mixer with the Back-end Amplifier.....30
3.1.3.3.3 OTA-C LPF with the Voltage-Current Converter.....31
3.1.3.3.4 Noise Analysis and Process Variation Problems.....33
3.1.3.4 Simulation Results.....36
3.2 Chemical and Biological Sensing Front-end Using Fluctuation Noise.....40
3.2.1 System Level Implementation.....40
3.2.2 Fully-differential 1st Order OTA-C Filter Design Considerations.....41
3.2.2.1 Resistor.....41
3.2.2.2 First Order Low Pass Filter.....42
3.2.2.3 Constant-gm Biasing.....46
3.2.2.4 High Temperature Compensation.....51
3.2.2.5 Low Frequency Noise Reduction.....56
3.2.3 Final Practical Design Results.....57
3.2.3.1 Whole System.....57
3.2.3.2 Final Design Parameters.....59
3.2.3.2.1 Constant-gm Biasing.....59
3.2.3.2.2 Operational Transconductance Amplifier.....60
3.2.3.2.3 Common Mode Feedback Circuit.....63
3.2.3.3 Simulation Results.....65

4. CHIP PHOTOGRAPHIES AND TEST RESULTS.....70

4.1 Chip Photographies.....70
4.1.1 Nanowell Sensor IC.....70
4.1.2 Van der Waals Sensor IC.....72
4.2 Test Results.....73
4.2.1 Nanowell Sensor IC.....73
4.2.1.1 Test Set-up.....73
4.2.2 Van der Waals Sensor IC.....77
4.2.2.1 Test Set-up.....77
4.2.2.2 Test Results.....84
4.3 Summary.....92

5. CONCLUSION.....93

REFERENCES.....95

Page

APPENDIX 100

VITA 109

LIST OF FIGURES

Page

Figure. 1. The conceptual example of distributed sensing using N redundant. 2

Figure. 2. Fabrication of nanowell capacitors. 7

Figure. 3. SEM photograph of the nanometer pattern mask [4].....8

Figure. 4. Sketch of the frequency variation of the real and imaginary parts of the complex relative permittivity of the material [6]. 10

Figure. 5. The MOSFET-based sensor. 13

Figure. 6. Structure and function of the van der Waals force enhanced MOSFET.....16

Figure. 7. Alternative approach to modulate van der Waals force. 17

Figure. 8. Basic structure of the thin-film sensor [12]. 18

Figure. 9. Demonstration of the usefulness of the new sensor principle. 20

Figure. 10. System level block diagram of the CMOS sensor IC. 22

Figure. 11. The conceptual diagram of the lock-in capacitive sensing. 24

Figure. 12. The spectral representation of the lock-in capacitive sensing system. 25

Figure. 13. The conceptual diagram of the front-end circuit system. 26

Figure. 14. Common mode error amplifier with CMFB. 28

Figure. 15. The mixer stage with the back-end amplifier. 30

Figure. 16. OTA-C filter and voltage-to-current converter (N=10). 33

Figure. 17. The output current vs. the capacitance mismatch plot for 1 GHz 20mV amplitude input VRF signal. 36

Page

Figure. 18. The output current transient response plot with 1fF capacitance mismatch with 20mV input amplitude and 1 GHz frequency. 38

Figure. 19. The Monte Carlo simulation result of the output current with 1 GHz, 20mV input signal and 1fF sensed capacitor....39

Figure. 20. System level block diagram of the CMOS sensing front-end using the fluctuation noise. 40

Figure. 21. A typical implementation of a resistor with a transconductor. 42

Figure. 22. A single-ended voltage-mode gm-C integrator....43

Figure. 23. Single-ended first order gm-C filter....43

Figure. 24. Concept of a differential integrator.....45

Figure. 25. Fully differential integrator.....45

Figure. 26. Conceptual diagram of a conventional resistor-control loop.....46

Figure. 27. Basic fixed transconductance bias circuit. 48

Figure. 28. Concept of an improved fixed transconductance bias circuit. 50

Figure. 29. Circuit implementation of the scheme of fig. 28. 51

Figure. 30. Complete "fixed transconductance bias" circuit. 52

Figure. 31. Drain current characteristics of typical 50-pm/lo-pm p channel MOSFET with temperature as parameter in saturation (VDS = - 6 V) [44].....54

Figure. 32. MOSFET drain and source to body leakage currents and conductances.....55

Figure. 33. Simple leakage current compensation circuit. 56

Page

Figure. 34. The system diagram of the fully differential first order low pass filter with high temperature operation. 58

Figure. 35. Constant gm biasing circuit for a PMOS input stage....59

Figure. 36. Operational transconductance amplifer diagram. 61

Figure. 37. Common mode feedback circuit. 64

Figure. 38. Frequency response plot of the filter array at 200°C. 66

Figure. 39. 3dB point vs. temperature plot of filter #3....67

Figure. 40. Nanowell sensor IC photograph. 70

Figure. 41. Zoomed photo of one front-end channel....71

Figure. 42. Van der Waals sensor IC full photograph. 72

Figure. 43. Nanowell sensor IC test set-up. 73

Figure. 44. Test set-up for Van der Waals sensor IC. 77

Figure. 45. Test board #1 layout. 81

Figure. 46. Photograph of test board #1. 82

Figure. 47. Test board #2 layout. 83

Figure. 48. Test board #2 photograph. 84

Figure. 49. The output transient response of filter #6 with 50mV amplitude (the upper is 1Khz signal and the lower is 5Khz signal). 85

Figure. 50. The conversion gain plot taken from the simulation in Cadence. 86

Figure. 51. The magnitude and phase response of the output of filter #5. 87

Figure. 52. The noise spectrum of the output of filter #5....88

Page

Figure. 53. The signal spectrum of the output of filter #5.....89

Figure. 54. The magnitude and phase response from filter #1.....100

Figure. 55. The magnitude and phase response from filter #2.....101

Figure. 56. The magnitude and phase response from filter #3.....102

Figure. 57. The magnitude and phase response from filter #4.....103

Figure. 58. The magnitude and phase response from filter #5.....104

Figure. 59. The magnitude and phase response from filter #6.....105

Figure. 60. The magnitude and phase response from filter #7.....106

Figure. 61. The magnitude and phase response from filter #9.....107

Figure. 62. The magnitude and phase response from filter #10.....108

LIST OF TABLES

Page

Table 1. Design parameters of the common mode error amplifier. 29

Table 2. Design parameters of the mixer and the back-end amplifier. 31

Table 3. Design parameters of the OTA-C filter and voltage-to-current converter. 32

Table 4. Constant gm bias circuit final design parameters. 60

Table 5. Operational transconductace amplifier design parameters A.....62

Table 6. Operational transconductace amplifier design parameters B.....63

Table 7. Design parameters of the common mode feedback circuit. 64

Table 8. Cut-off frequencies A of the filter array at 200°C(simulation results). 68

Table 9. Cut-off frequencies B of the filter array at 200°C(simulation results).....69

Table 10. Pin description A of Nanowell sensor IC.....75

Table 11. Pin description B of Nanowell sensor IC.....76

Table 12. Pin description A of the Van der Waals sensor IC.....79

Table 13. Pin description B of the Van der Waals sensor IC.....80

Table 14. Filter performance parameters A including TIA of each filter output. 90

Table 15. Filter performance parameters B including TIA of each filter output. 91

1. INTRODUCTION

1.1 Motivation

A wireless sensor network is one of the greatest breakthroughs happening in these times to facilitate truly autonomous, distributed and pervasive computing. Such a network consists of a large numbers of nodes each equipped with front-end circuits and radio devices. Each node of the network monitors its local environment, locally processing and storing the collected data. Network nodes share this information via wireless link between each other and a central base station. Using data fusion, specific features of interest to the end user can be extracted from the information that several nodes collect [1, 2]. For applications ranging from industrial automation to homeland security, distributed wireless ad-hoc sensor networks will make an everlasting impact to improve everyday life. This research focuses on the design of the front-end electronics for two specific sensors used in environment monitoring applications targeted for gas, chemical and molecular sensing.

The design issues for sensor nodes in a wireless sensor network are that of low power and small form factor. Moreover it should be implemented using low cost techniques. The sensors designed in a traditional CMOS technology are desirable due to their low cost, low power consumption, portability and potential advantages in mass production. Also, the state-of-art CMOS technology enables the integration of all the sub-building blocks such as the readout circuit and the signal processing circuitry on a same chip or package as the sensor itself towards "lab-on-a-chip" implementation.

An autonomous node in a sensor network ideally contains a sensor, a readout circuit, a digital signal processing part to process information from the sensor and a RF communication circuit. The central base station which functions as a network controller collects the data from all the sensor nodes and extracts meaningful information of the target material by performing advanced digital signal processing. Fig. 1 demonstrates the conceptual block diagram of the N redundant distributed sensing. As seen, the system

———————

This thesis follows the style of *IEEE Journal of Solid State Circuits.*

has the front-end which converts the raw signal from the sensor to the electrical signal. At the second stage, ADC converts the electrical signals into the digital signals which are much easier to process. The processed digital signals are converted into analog signal in order to be transmitted as the radio frequency signal through Power Amplifier. Also, the control signals from Central Network Controller and that sensor data from neighboring nodes come via the same antenna, the low noise amplifier and the A/D converter.

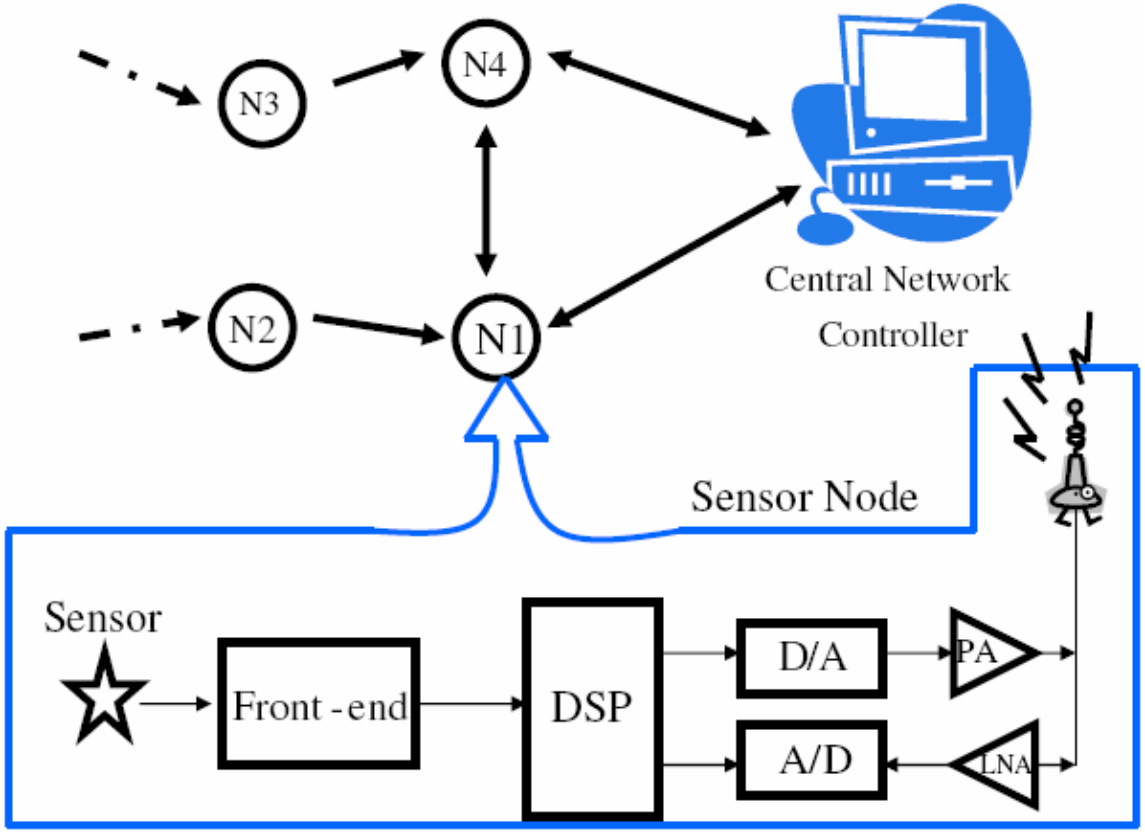

Fig. 1. The conceptual example of distributed sensing using N redundant.

One of the sensor devices used in this research is a nanowell capacitor. The nanowell capacitor was introduced recently [3, 4] by researchers at Texas A&M University using a well-know CMOS process. This nanowell capacitor was postulated for use as a chemical and biological sensor using the technique called Broadband

Dielectric Spectroscopy[5,6], which measures the dielectric constant of the material trapped in the capacitor as a function of the frequency. By capturing the capacitance value change of "nano-size" capacitors on the silicon wafer, the target materials in the capacitor is detected. Its small size is the great advantage in secure environment monitoring applications.

Another device is a Van der Waals MOSFET sensor or a Taguchi sensor, which is fabricated with the CMOS technology. A Van der Waals MOSFET sensor was invented from researchers at Texas A&M University [7]. The trapped molecules on the gate surface modulate the threshold voltage of the MOSFET, resulting in a stochastic fluctuation of drain current which can be used for the identification, quantitative analysis of molecules and their mixtures by the fluctuation-enhanced stochastic analysis method [8]. A Taguchi sensor is one of the typical film-based sensor devices used for gas sensing applications. The operating principle for detection in both these sensors is the use of fluctuation enhanced sensing. The idea of fluctuation enhanced sensing utilizes the statistics of the noise like information signal in the low frequency spectrum to detect target molecules. Our approach to such detection is using a low pass filter bank from 0.1Hz to 100 KHz to extract the information contained therein and processing them individually using advanced pattern matching algorithm [9]. The pattern matching algorithms is not the scope of this research. The low power consumption and s mall size of these sensors (Van der waals and Taguchi) along with their ease of fabrication in traditional CMOS technology makes them suitable candidates for distributed gas sensing applications [10,11].

To use the nanowell capacitors in the sensor network, we need very accurate capacitance sensing circuits which consume ultra low power. Capacitance detection circuit measures the change in the dielectric constant value by measuring the capacitance of the nanowell. The low power consumption of this circuit minimizes the total power consumption of the entire system. We implemented a lock-in sensing technique which can extract both real and imaginary part of the capacitance and hence the dielectric constant of the trapped material with low power consumption.

For the other sensor, we implemented a low power and high gain transimpedance amplifier to amplify the stochastic fluctuation noise current signal from a Van der Waals or Taguchi type sensor. At the next stage of this sensor, extremely low cut-off frequency lowpass filters are used for processing the information located in very low frequency range from 0.1Hz to 100 KHz range [9]. The considerable linear dependency of the fluctuation noise generation of CMOS devices on temperature requires very high temperature operating environment for maximizing the noise-like input current [12]. So, the robustness of the front-end circuit including the amplifier and the filters to the temperature variation(~200℃) is critical and has been addressed in this research.

1.2 Objective of This Thesis

In this thesis, as the building block of front-end circuits using nanowell capacitors, the accurate and low power capacitance sensing circuit is designed. The extremely low cut-off frequency filters, which are very temperature-insensitive, are implemented and tested as one of the building blocks of the front-end circuits using the fluctuation noise current signal from a Van der Waals MOSFET sensor or a Taguchi sensor. The overall layout of the thesis is given below.

First of all, the fundamentals on the fabrications process and the operational concept of nanowell capacitors will be demonstrated. After that, the conceptual background on Broadband Dielectric Spectroscopy will be presented. Next, the background on MOSFET-based sensors is clarified. It covers a Van der Waals sensor and film-based sensors such as a Taguchi sensor. Thirdly, the systematic explanation of the nanowell sensor IC is conducted. The concise description of the previous capacitance sensing circuits will be shown. The need to devise a novel capacitance sensing circuit comes into view while describing them. The novel capacitance value sensing circuit is demonstrated and simulated while displaying the circuit design parameters. Following this discussion, the systematic concept of the Van der Waals Sensor IC is explained. The required characteristics of the building blocks of the IC are clarified. Also, the circuit

topology and technique which enables the circuit to satisfy the requirements are demonstrated and the relevant physical background is attached. Finally, the circuit design parameters are shown and the simulation results are displayed.

The fabrication results of the nanowell sensor IC and the Van der Waals sensor IC are shown with detailed explanation of the test procedures and the test results. Finally, the final conclusion of this thesis is drawn and the future possibilities for exploration are discussed.

2. BACKGROUND

2.1 Chemical Sensing with Nanowell Capacitors

2.1.1 Fabrication of a Nanowell Capacitor

Recently, a novel innovative photo-lithographic method was used to fabricate very large scale nanowell arrays in silicon [4]. In Fig.3, Hashioka's implementation of the array is demonstrated [4]. The lateral dimension of the nanowell (10-100nm) is defined by anodic oxidation of Ti or Si (Fig. 2). The nanowell, 10-50nm wide, 10 – 1000nm long and 60nm deep, is essentially a parallel plate capacitor. The dimension of the capacitor enables trapping of single biomolecules. Trapping of molecules is achieved through positive dielectrophoresis, in which a non-uniform electric field induces a net dipole moment and corresponding attractive force on a polarizable molecule. By tuning the frequency and the voltage applied to the nanowell, the target molecules can be forced in a resonant motion for measurement. Moreover, by changing the frequency and voltage of the applied signal, we can alter the polarizability of the medium and the trapped molecules. It is a very useful technique to release the already trapped molecules from the nanowell to alter the frequency and polarity of the electric field for the future use of the nano-capacitor [5]. Detection of the trapped molecules for its material properties is performed using broadband dielectric spectroscopy (BDS). BDS measures the complex permittivity of the molecule as a function of the frequency. An overview of the BDS technique is provided in the next section.

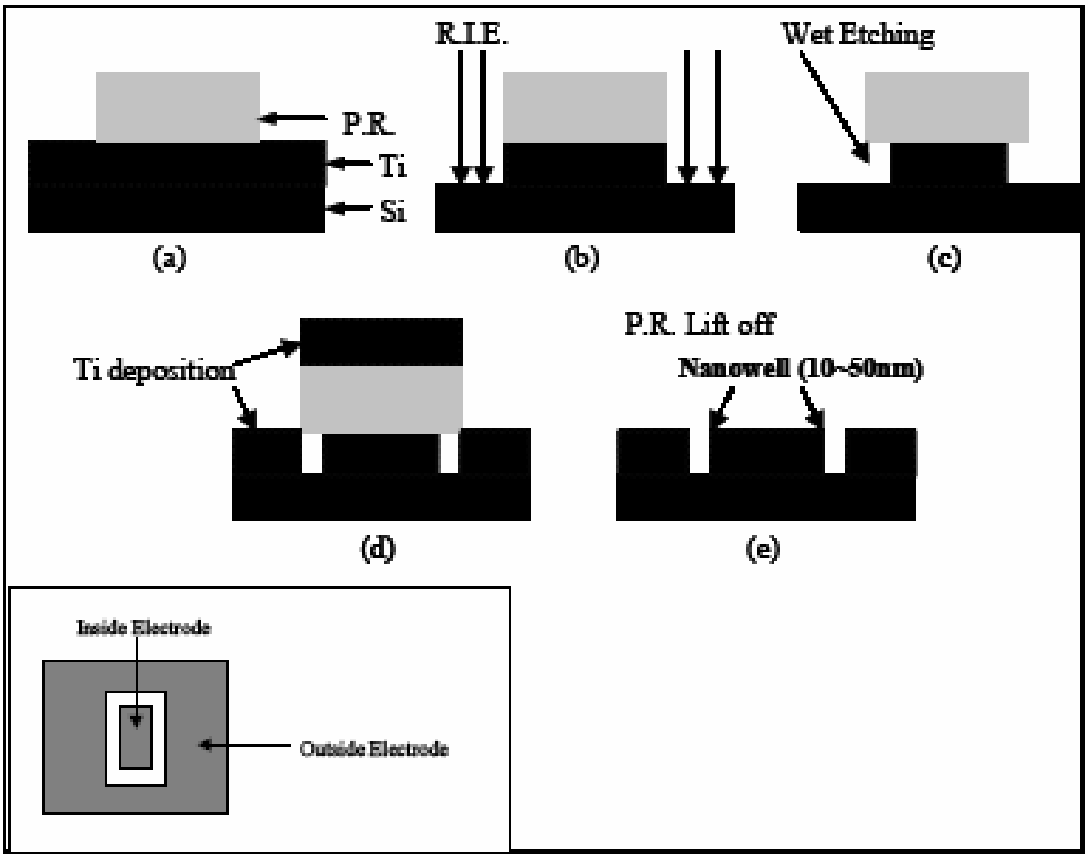

Fig. 2. Fabrication of nanowell capacitors.

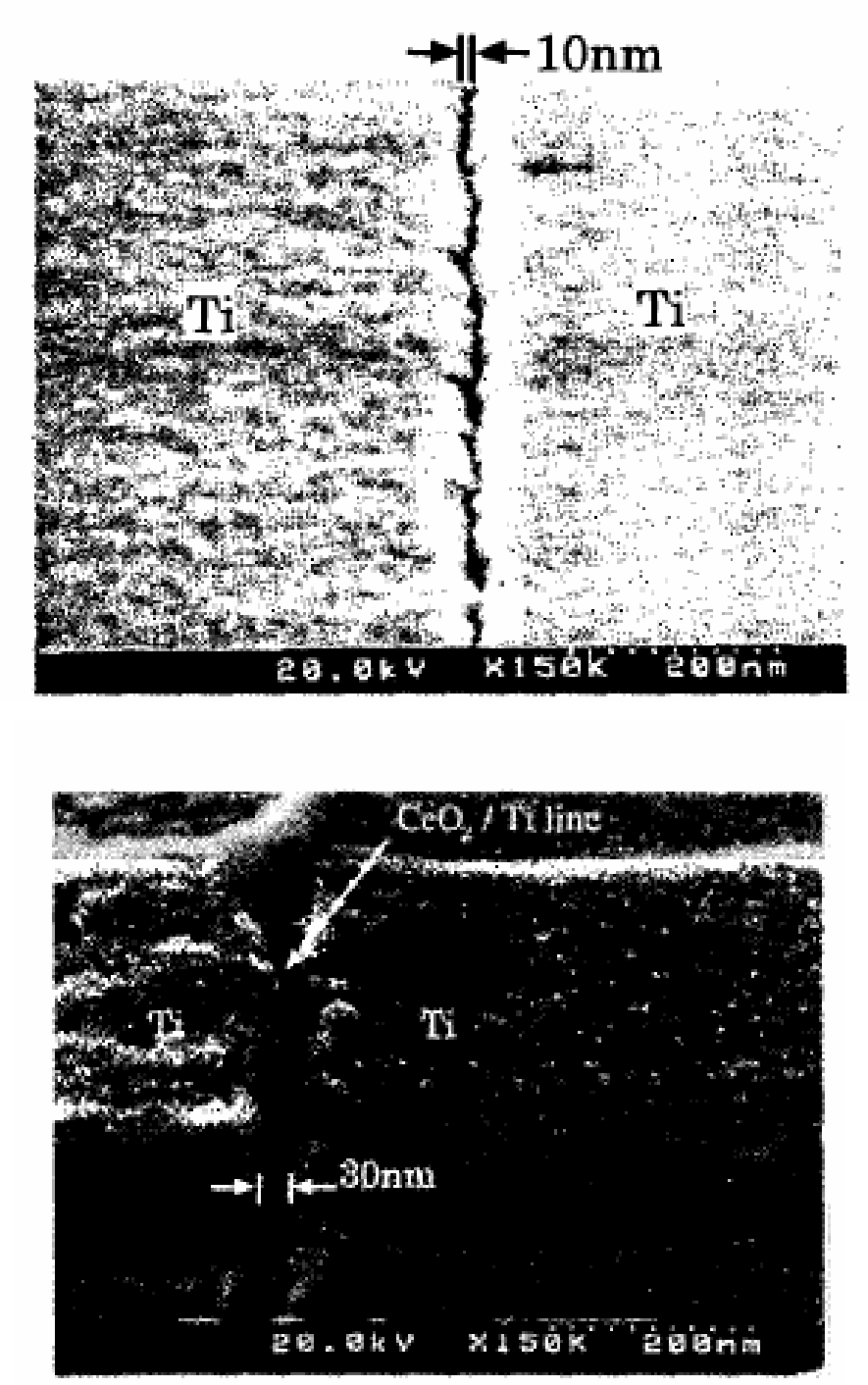

Fig. 3. SEM photograph of the nanometer pattern mask [4].

2.1.2 Broadband Dielectric Spectroscopy

Broadband Dielectric Spectroscopy (BDS) is widely used for investigating the characteristics of a great number of materials. The interaction of electromagnetic (EM) radiation with molecular system induces quantized transitions between the electronic, vibrational and rotational molecular energy states. Those interactions can be observed by UV/visible and infra-red absorption spectroscopies at the high frequency. The dielectric dispersion and absorption phenomena that occur in the wide high frequency range are due to the dipole relaxation arising from the reorientational motions of molecular dipoles and electrical conduction arising from the transitional motions of electric charge [5].

Therefore, these effects can dominantly influence the dielectric properties of the material in the relevant frequency range. At the microelectronics side, the dielectric properties of the material are expressed by the complex electrical impedance. The underlying effects mentioned above and their impact on the impedance can be modeled by a couple of standard models such as Debye, Cole-Cole and Cole-Davison models [3].

$$\varepsilon = \varepsilon^{*} - j\varepsilon^{**} \qquad (2\text{-}1)$$

$$\varepsilon^{*} = \varepsilon_{\infty} + \frac{\varepsilon_s - \varepsilon_{\infty}}{1 + (\omega\tau)^2} \qquad (2\text{-}2)$$

$$\varepsilon^{**} = \frac{\omega\tau(\varepsilon_s - \varepsilon_{\infty})}{1 + \omega^2\tau^2} + \frac{\sigma_{dc}}{\omega\varepsilon_0} \qquad (2\text{-}3)$$

The classical physical behavior of the frequency dependence of the real and imaginary parts of the permittivity was described by Debye [5]. His model can be summarized by (2-1), (2-2) and (2-3), where ε_{∞} is the absolute value of the permittivity at infinite frequency, ε_s is the absolute value of the permittivity at zero frequency, ε_0 is the vacuums permittivity and σ_{dc} is the DC conductivity of the system. Fig. 4 shows us the graphical way of expression of the frequency-dependence of the permittivity of the measured material according to (2-1), (2-2) and (2-3) [5]. BDS measures the real and imaginary part of the capacitance C = C(e,w), where e is the complex permittivity and w is the frequency of the applied electric field. Each molecule or combination thereof

provides a unique signature in the dielectric spectrum as a function of frequency for purpose of detection and analysis.

We also understand that we can fabricate a very tiny value capacitor on the silicon wafer which is used to sense the molecule trapped within itself using the BDS technique. If we can realize the cost-effective dielectric constant sensing CMOS circuitry with that tiny capacitor, we can build up a very good chemical or biological sensing system with the economical CMOS technology. One drawback of the CMOS technology for BDS is the limited frequency range for analysis. However for most molecules, the frequency range (0 ~ 1GHz) provide enough information for selectivity. Therefore, the sensing technique can emerge to be one of the promising sensing solutions with low cost.

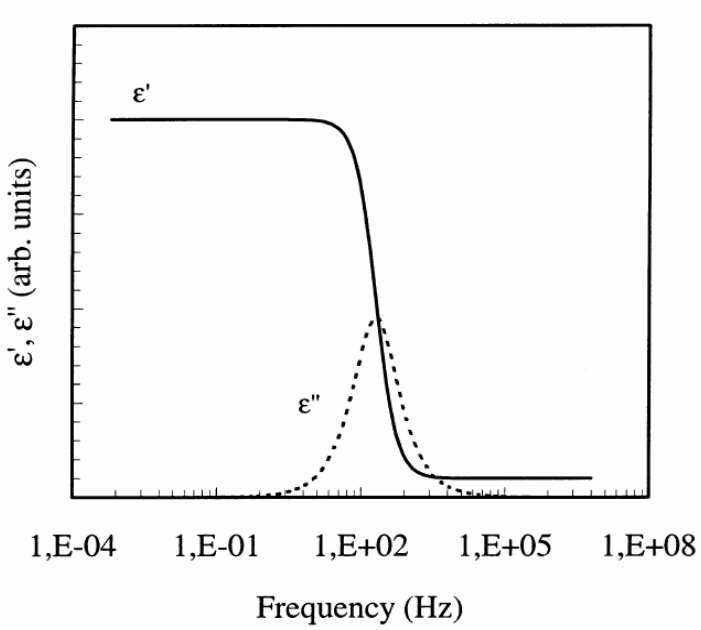

Fig. 4. Sketch of the frequency variation of the real and imaginary parts of the complex relative permittivity of the material [6].

2.2 Solid State Chemical Sensors

2.2.1 History of the Chemical Sensing [12]

Generally speaking, the classical and the current solutions for chemical sensing have been complex like laboratory methods such as gas chromatography and ion-mobility spectroscopy. Even though the methods are accurate for detecting chemical materials and in their ability to perform multi-material detection, they are often very expensive to commercialize for consumer and low-end application. To lower the cost of the chemical sensing system enough to be commercialized in the consumer and low-end market as in distributed sensor network, a new approach to chemical sensing has been created.

To overcome the cost problem of the previous chemical sensing system, miniaturization technique has been used. However, the technique is supposed to sacrifice some of the accuracy of laboratory methods for lower cost, faster response times and greater accessibility. Since the early 1970's, the microelectronic chemical sensor has been investigated as this low-cost, miniaturized alternative to laboratory chemical sensing methods. However, it has been difficult to overcome some of the inherent problems of the miniature chemical sensors such as reproducibility, selectivity, sensitivity, stability and response time while keeping the cost down at a manageable level. After a while, some progress has been made in the research community for realizing the balance between cost and robustness of viable chemical sensing system.

2.2.2 MOSFET-based Sensor

2.2.2.1 Description

MOSFET-based sensors such as ISFET and ChemFET mean the sensor devices using a chemically sensitive insulator or chemically sensitive gate on the gate area of a MOSFET device to sense the chemical material. ISFET was introduced for the first time as an implementation of a MOSFET-based sensor. An ISFET is simply a MOSFET

which has a chemically sensitive insulator membrane instead of a gate. Charge change caused by the sensitive chemicals on the membrane is amplified by operation of the FET device under the membrane [13]. However, vulnerability of the insulator membrane to the external effect and the subsequent transistor breakdown has been the most critical problem in its becoming popular for chemical sensing. Also, the light sensitivity of the insulator has been one of the problems with these devices since no optical shielding exists around the FETs. Therefore, a novel device called "ChemFET" was invented. It has successfully demonstrated more potential for practical chemical sensing. Even though it has less selectivity and chemical sensitivity than ISFET, ChemFET makes use of a standard oxide layer as the insulator and a chemically sensitive metal [14]. The metal gate minimizes light sensitivity problems of ISFETs. Moreover, the physical barrier of the metal gate and the resilience of silicon dioxide can successfully minimize the potential environmental poisoning problems of ISFETs [13]. Also, we can modify the ChemFET to integrate the advantages of two different devices to achieve a better performance. The results are called the "Surface Accessible FET" or "SAFET"[15]. and the "Suspended Gate FET" or "SGFET"[16]. Despite the enhanced selectivity and sensitivity of these devices over the ChemFET, however, they suffer from a short lifetime problem because the exposed oxide layer degrades very fast than other device. Therefore, due to its strong robustness to the environmental degradation, the ChemFET is thought to be the best fit for the MOSFET-based chemical sensing in spite of its relatively low selectivity. The conceptual structures and operational concepts are demonstrated in Fig. 5.

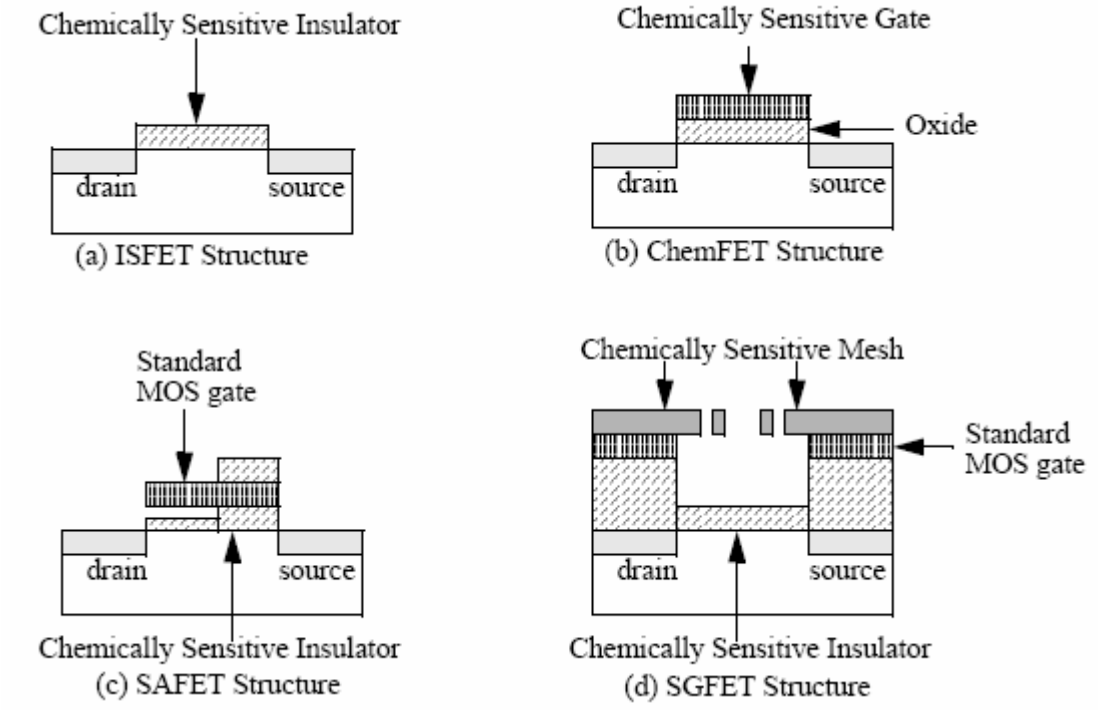

Fig. 5. The MOSFET-based sensor.

2.2.2.2 Van der Waals Force Enhanced MOSFET Sensor

2.2.2.2.1 Introduction

The Van der Waals Force Enhanced MOSFET (VWFE) sensor was proposed by Dr. Mosong Cheng and others [7]. The Van der Waals Forced Enhanced MOSFET sensor manipulates van der Waals force interaction between silicon and molecules by tuning the gate voltage or electrical injection of carriers. The modulation of van der Waals force affects the equilibrium and rate at which molecules on the gate surface are trapped and released. The trapped molecules modulate the threshold voltage of the MOSFET, resulting in a stochastic fluctuation of drain current which can be used for the identification, quantitative analysis of molecules and their mixtures by the fluctuation-enhanced stochastic analysis method. Millions of such devices can be integrated with

CMOS circuitry on a single chip by standard IC processing to construct electronic dog-nose. The sensor is potentially versatile, robust, inexpensive, and would exhibit high sensitivity and selectivity for the analysis of multiple agents. The van der Waals force and electrical excitation can affect the shape and function of trapped molecules. The proposed device, as a molecule/electronics interface, will be explored as a key enabling component of highly parallel, single molecule level "lab-on-a-chip" system[17]. Dr. Mosong Cheng group is working on the fabrication of the first prototype.

2.2.2.2.2 Motivation

Solid-State sensors have been the considerably attractive implementation for the compact, fast and integrated sensor device with the analog/digital electronic circuitry and the potential low-cost sensor device with the mass production possibility. Usually, the sensor is realized by coating an active film (such as oxide, polymer or metal) on the surface of silicon. The sensor is supposed to use the change of physical or chemical property of the coated film, such as mass, dielectric constant, temperature, conductivity, charge, chemical potential, work function or surface potential depending on absorption of target molecules by the film [18, 19, 20, and 21]. In these sensors, the selectivity of target molecules/ion is realized by coating the right material which has the strong sensitivity to target agents and intense insensitivity to the other substances. Therefore, for sensing multiple types of materials, the sensor is necessary to be coated with several different films, which causes excessive processing steps and highly expensive manufacturing cost. Also, the sensor is unable to sense the unexpected yet important molecules (for instance, breaking out of a terrible virus). Also, how to reverse the effect of target material on the film for the future is supposed to limit the availability of those type sensors.

Moreover, the current apparatuses for single molecular detection such as Scanning Probe Microscope (SPM) and Optical Spectroscopy are too bulky and need much time finishing the detection and isolated environment. Also, often, they are pretty incapable of simultaneous multiple type agents sensing. Since the single molecular detection is very essential for revealing information about molecular kinetics and

dynamics which is not currently measurable without some professional devices, the capability of single molecular probing with the solid-state devices has been imperatively demanded in many chemical and biological applications[22].

It is possible that a molecule is embedded between electrodes and performs basic functions of sensing and computation in a very sophisticated experimental condition. However, the cost required to fabricate the complete circuit at the molecular level is still seriously high [23]. Nevertheless, the concept of bioelectronics, aiming to integrate biomolecules and electronics into functional systems, appears to be very attractive as a progressing cross-disciplinary field. Therefore, the implementation of hybrid system that efficiently sense, compute and transform the chemical processes into electric power or signal is emerging to be one of the most promising areas. Additionally, the communication between biomolecules and electronics is the essence of all bioelectronics system.

To address the above needs, a "Van der Waals Force Enhanced MOSFET" sensor as a potentially compact, flexible, and massively parallelable device [11]. It has been intended to have high-selectivity and high-sensitivity for "lab-on-a-chip" analytical system which can sense multiple agents, mostly gaseous substances.

2.2.2.2.3 Operational Concept of the Device

The proposed Van der Waal Enhanced MOSFET sensor manipulates van der Waals force interaction between the silicon and molecules by tuning the gate voltage or injecting carriers to PN junction [11]. The structure of the proposed sensor of NMOS is described in Figure 6. Based on the conventional MOS theory, we can say that if the gate voltage is positive but lower than a threshold voltage VT, the MOSFET works in the depletion region, that is, the free carrier density (mostly holes) in the channel between source and drain is very low, as is depicted in Fig. 6 (a). In this condition, the Van der Waals force between the carriers is negligibly small. However, if the gate voltage is above VT, the MOSFET works in inversion region and the free carrier density (mostly electrons) in the channel is high, as is shown in Fig. 6 (b). The increased free carrier density is supposed to rapidly increase van der Waals force between silicon and

neighboring molecules or ions, therefore many more molecules/ions can be brought to collisions, and therefore trapped, on the surface of silicon, shown in Fig. 6 (b). Additionally, the van der Waals force can be modulated by electrically injecting free carriers into a PN junction under MOSFET as described in Fig. 7.

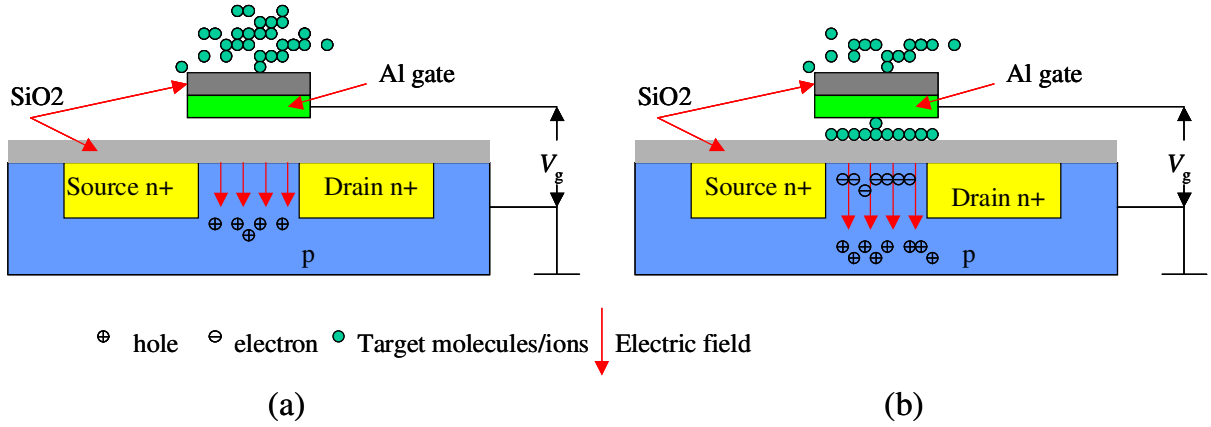

Fig. 6. Structure and function of the van der Waals force enhanced MOSFET.
(a) gate voltage Vg is low, MOSFET is in depletion mode, few carriers exist in the channel, and the van der Waals force is week; (b) Vg>VT, MOSFET is in inversion mode, carrier density in channel is high, the van der Waals force is much stronger and many more molecules are trapped on the gate surface [17].

As explained above, the van der Waals interaction between semiconductor and insulator can intensify due to the increase of the free carrier density. Thus it is possible to modulate van der Waals attraction from silicon by tuning the free carrier density in the channel of a MOSFET with gate voltage. Therefore, according to the change of van der Waals force, the neighboring molecules and ions are supposed to reach a new equilibrium state. Since van der Waals force is a long-range interaction, the temporary external effect does not cause a seriously considerable contamination effect.

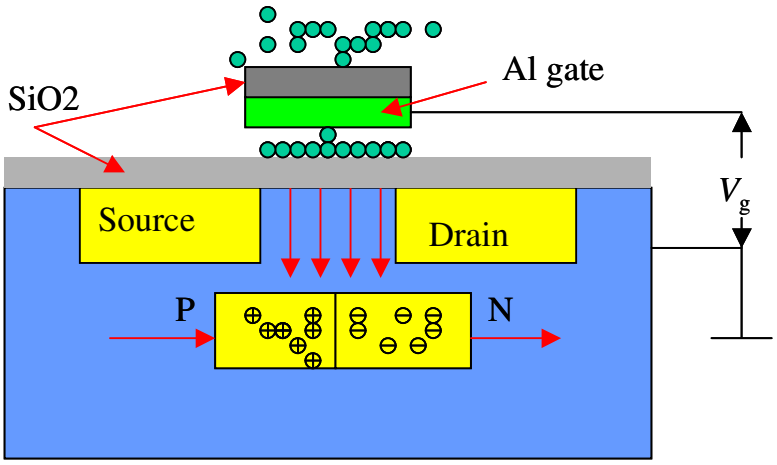

Fig. 7. Alternative approach to modulate van der Waals force.
By applying forward bias, free carriers are injected into the PN junction beneath the MOSFET.

The trapped molecules, with their dipole moment, can change the work function of the insulator, semiconductor or metal. Since the working function is one of the values composing the whole threshold voltage, the changing working function results in a change of VT of the MOSFET. Since the current between source and drain is given by $I_d = C_{ox}\mu\frac{W}{L}\left[(V_g - V_T)V_d - \frac{1}{2}V_d^2\right]$, the change of threshold voltage induces a fluctuation of the drain current I_d. The stochastic fluctuation of drain current can be used for the detection, identification and quantitative analysis of molecules and their mixtures by the stochastic analysis method presented by G. Schmera and L. Kish[21,24], which is probably the most powerful application of fluctuation-enhanced chemical sensing [25,26,27 and 9]. Therefore, by using the device, the MOSFET sensor with multiple type agents sensing capability can be realized. Also, since the sensor is fabricated with the conventional CMOS technology, it is possible that the sensor is integrated with the readout circuitry and amplifier on the same chip to realize the molecular sensor-system-on-chip [17].

2.2.3 Thin-film Based Sensor and New Sensing Technique [8]

2.2.3.1 Concept of the Film Based Sensor

The microelectronic chemical sensor has been recognized as a low-cost alternative to overcome the problems of laboratory chemical sensing methods [12]. Many of the microelectronic sensor technologies are based simply on conductivity changes in a material in response to chemicals in the environment [8]. The simplest of these conductivity-based sensors, the thin-film sensor, was first introduced into the research community in the early 1970's [12]. The thin-film sensor in Fig. 8 is simply a film of chemically sensitive material, such as SnO2, TiO2, or porous silicon [10] whose conductivity changes in response to the neighboring chemicals in the sensing environment. The metal-oxide, thin-film sensors are the only miniaturized chemical sensors which has become popular in the commercial market. The most popular sensor among those sensors is the Taguchi-type sensor. The sensor is composed of tin oxide modified with various catalysts and additive to improve the ability of detecting target materials [10].

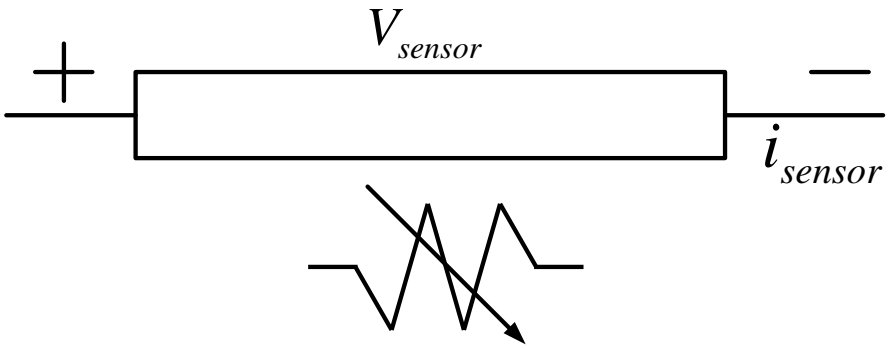

Fig. 8. Basic structure of the thin-film sensor [12].

The reason why thinness is required is because the conductivity change is mainly due to surface interactions. Therefore, to maximize the interaction effect on the conductivity, the film should be made as thin as possible.

Also, since the thin-film sensor device is very compatible with standard integrated circuit fabrication process, it has been possible to integrate these sensors with complex signal processing circuitry on single chip [12]. So, thin-film device can be considered as one of the most promising sensor device for diagnostics and measurement in a "lab-on-chip" system implementation.

2.2.3.2 New Multiple Type Agents Sensing Technique

A conventional film-based sensor however has a serious problem. Since the oxide of the sensor is modified to have a good sensitivity to one target agent, a number of sensors are required to detect various chemical and biological agents. Therefore, it is undesirable to use the conventional type film-based sensor to build a multiple agent sensing sensor. To overcome this problem, Dr. Kish at Texas A&M proposed to use the stochastic fluctuation noise generated by the sensor for realizing the multiple sensing with conventional film-based sensors [8].

The technique is based on sensing the conductance noise caused by each chemical and biological agent when they encounter the sensor layer. The usefulness of the conductivity noise for the sensor application was investigated by Bruschi and coworkers [28,29]. From their research, it is generally recognized that the conductance noise spectrum is very sensitive to the chemical environment. Therefore, if we can measure the noise spectrum which is based on the neighboring chemical environment, we can detect those agents. In Fig.9, the noise spectrum density from four different materials is shown. It shows that the noise density is considerably different from others.

Even though we have much thing to do in order to find the exact origin of the microscopic noise components caused by the neighboring chemical environment, it is absolutely clear that the noise is related to the fluctuation of the carrier mobility and density due to concentration fluctuation and motion of the chemical fragments, originating from the chemical environment. The resultant resistance fluctuations are

supposed to be the source of an ac signal with wide frequency bandwidth, which carries more information than the traditional DC signal [9].

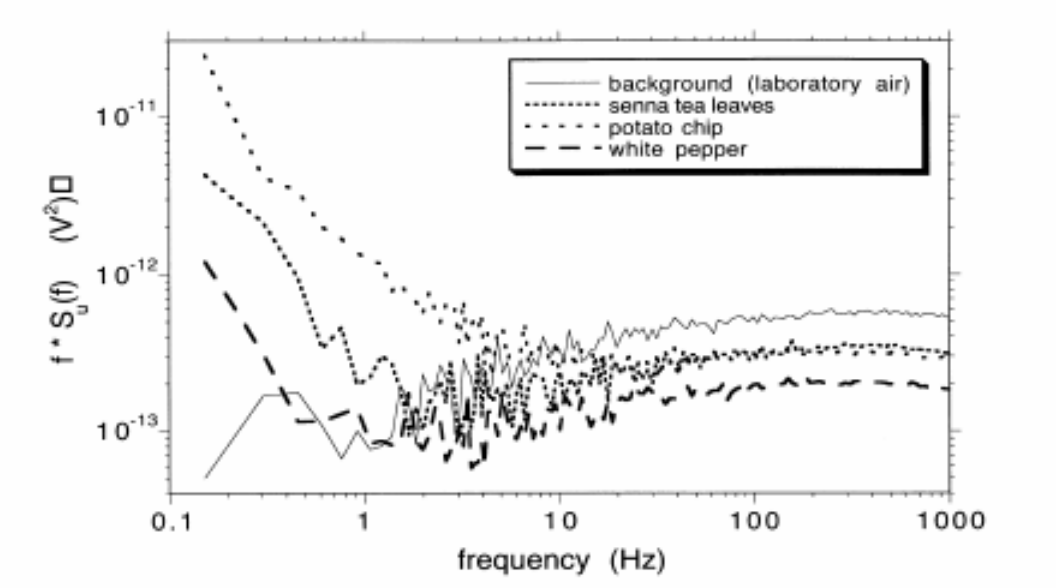

Fig. 9. Demonstration of the usefulness of the new sensor principle.
The voltage noise spectrum Su(f) of the sensor (proportional to the resistance noise spectrum) was measured at a current of 125 mA during exposition of the sensor to different types of natural odors. The differences between the shapes of the spectra should be noticed [9].

2.2.4 The Relationship between the Fluctuation Noise and Temperature

The dominant information of the fluctuation noise current from the sensor devices is located in very low frequency range. The flicker noise is the major contributor to the noise power in low frequency range. Therefore, by investigating the relationship between the flicker noise and temperature, we can find out the dependency of the fluctuation noise generation of CMOS devices on temperature.

In Hung's research, the unified model for flicker noise in MOSFET devices is demonstrated [30]. He formulates the unified flicker noise model like below.

$$S_{id}(f) = \frac{kTI_d^{\,2}}{\gamma f WL}\left(\frac{1}{N} + \alpha\mu\right)^2 N_t(E_{fn}) \qquad (2\text{-}4)$$

k : Boltzmann's constant T : absolute temperature I_d : drain current
γ : trapping time constant N : number of channel carriers per unit area
u : carrier mobility α : fitting constant N_t : distribution of the traps over energy
E_{fn} : quasi Fermi level

The formula (2-4) shows the proportional relationship between the output flicker noise power spectrum density and temperature. It means that the high temperature operating environment is required to maximize the output noise generation of CMOS sensor devices. Although the above expression is true for pure MOSFET devices, its applicability as a general rule of dependence can be extended to other materials.

2.2.5 Summary

In this chapter, we discuss the relevant physical background of the sensor devices used. The two sensor elements discussed were a “nanowell capacitor for molecular sensing” and a “van der waals enhanced MOSFET sensor” for gas sensing. A traditional taguchi sensor can also be used instead of the van der waals sensor and is also discussed.

3. IMPLEMENTATION OF THE CIRCUITS

3.1 Nanowell IC Readout Circuit

3.1.1 System Description

The readout circuit generates the raw signal expressing the dielectric constant variation. Therefore, Analog-to-Digital Converter is used to transform the raw signal into digital signals for the future Digital Signal Processing for better determination. Also, the control circuitry should be integrated to provide the external control functionality to the chip. Therefore, the system in Fig. 10 can be proposed [3].

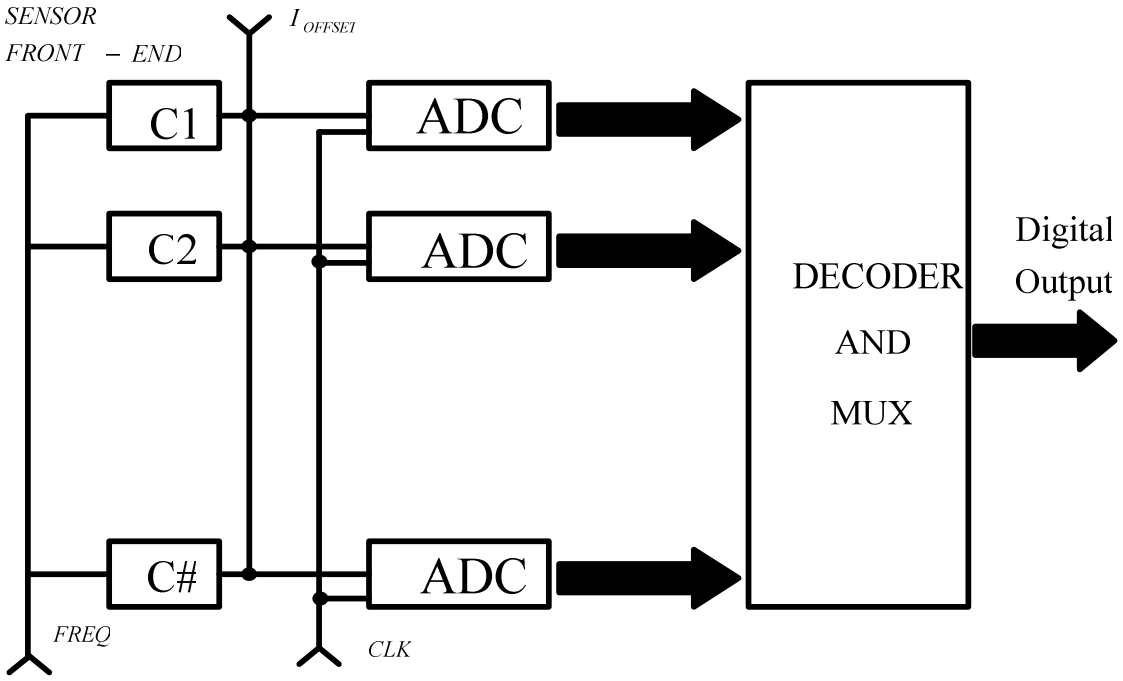

Fig. 10. System level block diagram of the CMOS sensor IC.

In the above system, the readout circuit, the capacitance detection front-end, is expressed as C#. C# provides the signal carrying the information about the dielectric constant change by sensing the change in capacitance value of the capacitor. The analog signal from C# is converted to digital signal through an ADC which is followed by the digital circuitry which controls the data transmission from the sensor IC to a DSP. The basic requirements of the readout circuit C# for the sensor system implementation according to the above system are as follows. First of all, the circuit should process the high frequency signal (~1 GHz) since it detects the capacitance value variation under the influence of the chemical material at the high frequency range. Secondly, power consumption of each readout circuit should be minimized as a number of cells are integrated. Thirdly, the output signal should be current. Finally, the built-in circuit noise should be minimized for increasing the dynamic range of the readout circuit and keeping the output signal power at the low level for minimum power consumption.

3.1.2 Previous Results of Capacitance Sensing Circuit

First of all, Bramani figured out a technique to measure the capacitance variation by measuring the phase shift between voltage and current is a series RLC circuits tuned to a certain resonance [31]. Also, the techniques proposed by Toth and Goes measure the capacitance by forming an oscillator using the sensor capacitor [32, 33]. Additionally, off-the-shelf components were used by Mochizuki in an interface circuit used to measure capacitance ratio [34]. A charge distribution technique was used by Kung [35] for capacitance sensing. Moreover, the IC which uses correlated double sampling (CDS) in combination with delta modulation has been reported by Ranganathan [36]. The CDS circuit acts as a high-pass filter that gets rid of low-frequency noise and interference. However, the available capacitive measuring techniques mentioned above are not appropriate for sensing the change of the dielectric permittivity in the high frequency range for BDS measurement. Even though C. Baltes [37] reported a single-chip gas detection system using the dielectric constant change, it was not adaptable for high frequency application, such as the Ghz range, which is the important regime of BDS. Recently, Sarpeshkar [38] used synchronous demodulation technique adapted in low

noise lock-in architecture for capacitive sensing. His technique has shown some potential for implementing the BDS on the silicon chip because it can vary the frequency of the probing signal. But, the achieved modulating frequency is not high enough for the BDS frequency range and is not designed for low power application. Also, for small-size sensing devices for portable or medical applications, the sensed capacitor size should be minimized and integrated on the silicon chip together with the other part of sensing circuitry. Therefore, the previously reported results are not proper in the BDS application with a very tiny capacitance value fabricated on the silicon.

3.1.3 System Implementation of a Novel Capacitance Sensing Circuit

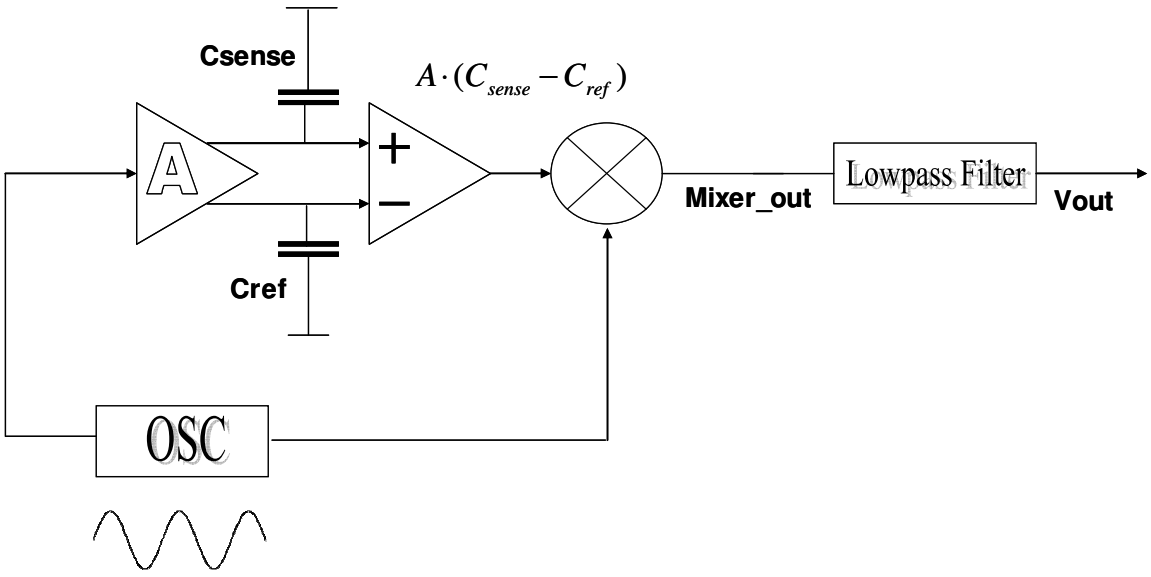

Fig. 11. The conceptual diagram of the lock-in capacitive sensing.

3.1.3.1 Lock-in Technique

The excellent noise performance is very essential for this system. So, the effective technique useful for reducing the amount of noise is required. As one of those techniques, lock-in technique is used in this research.

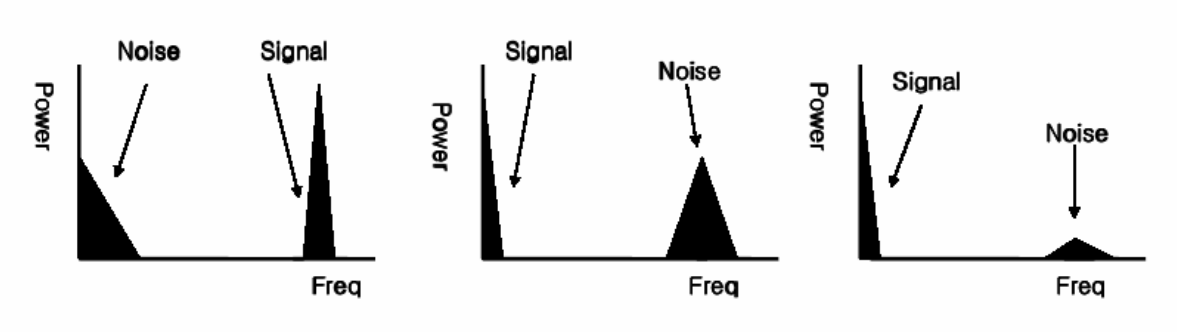

Fig. 12. The spectral representation of the lock-in capacitive sensing system.

The lock-in technique is very useful for implementing a low noise system in sensor electronics. It is because it can attenuate the low frequency noise signal such as 1/f noise and other offset inherent in the device [38].

The common mode Lock-in technique is illustrated in Fig.11 and Fig. 12. Fig 11 demonstrates its systematic modeling and Fig 12 shows the spectral representation of the system. First of all, the differential output of the amplifier "A" in Fig.11 is influenced by the difference of two capacitors, the reference capacitor Cref and the sense capacitor to be measured, Csense. It means that the mismatch between two capacitors is modulated by the applied high frequency signal, generating a signal quasi-linearly proportional to Cref-Csense. After this step, the mixer demodulates the output signal from the antecedent amplifier with the same high frequency signal. The demodulation in the mixer moves the low frequency noise and offset to the high frequency range. Also, the high frequency information signal is transferred into the low frequency range. As a result,

Mixer_out carries the noise at the high frequency range and the information signal at the low frequency range. Finally, a lowpass filter dramatically attenuates the high frequency noise and capture the mismatch information located in the low frequency range. Changing the frequency of the input signal into amplifier "A" enables us to realize wideband BDS measurements.

3.1.3.2 Operational Concept of the Capacitance Sensing Circuit

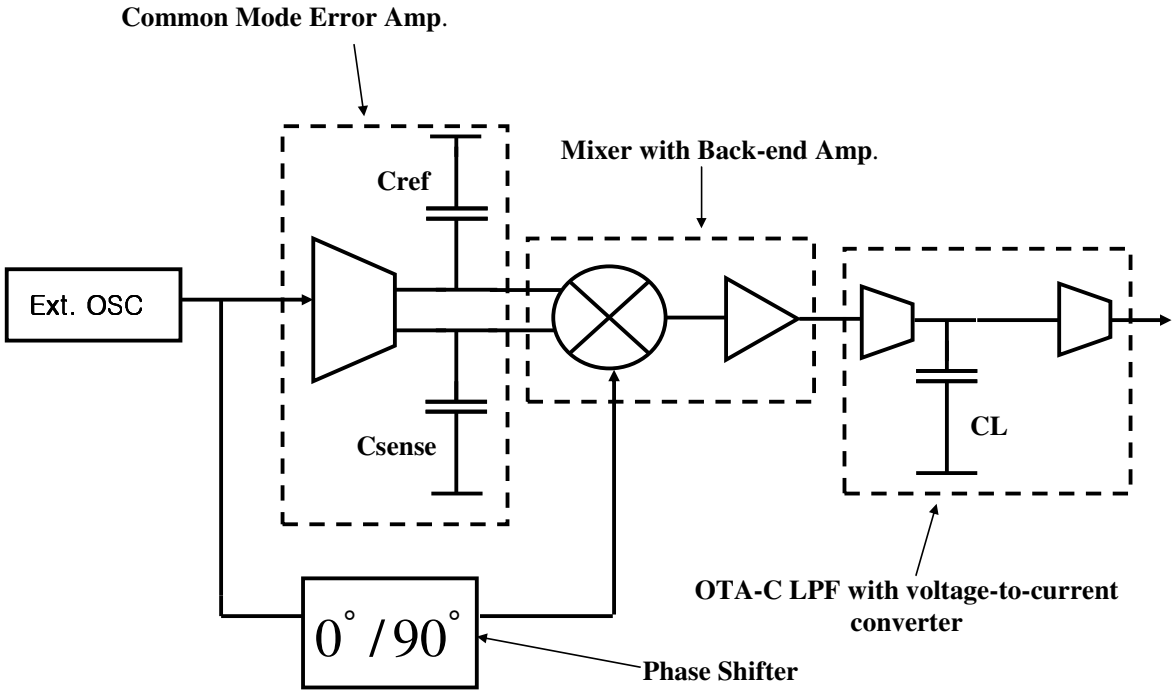

Fig. 13. The conceptual diagram of the front-end circuit system.

The conceptual block diagram of the sensor front-end for BDS measurement is shown in Fig. 13. First of all, a common mode error amplifier modulates and amplifies the mismatch between the reference capacitor value and the sensed capacitor value in the

first stage. Next, the mixer demodulates the signal. The phase shifter is used to measure the amplitude and phase information of the capacitance mismatch by use of quadrature modulation. The back-end amplifier intensifies the weak demodulated signal from the mixer. Finally, the demodulated signal passes through an OTA-C low-pass filter and transforms into current. The current domain output can then be fed to a low-power current-mode ADC for digitization [39, 40].

3.1.3.3 Building Block Design

3.1.3.3.1 Common Mode Error Amplifier

Fig. 14 shows the implementation of the Common Mode Error Amplifier (CMEA).Also, the design parameters are tabulated in Table 1. To amplify the common mode error, the conventional differential gain stage is used. The input VRF to the CMEA is the modulating carrier signal of high frequency. Since each common mode output values are different from each other because of the different capacitance value on each output load, CMEA can be used as a capacitance mismatch detector to measure the difference between a small reference capacitor Cref value and the sense capacitor Csense value (with molecules to be detected via measurement of the change in the dielectric constant), generating the modulated common mode error signal at a non-zero frequency. Also, because the effects of the parasitic capacitance are cancelled at the output stage, assuming that the parasitic capacitance values on each output are same to each other, the circuit can work at the high frequency range. Even if there are mismatches in the parasitic capacitance, it can be easily calibrated externally. In addition, the simple structure of the circuit has the advantage of low power implementation. The additional common mode feedback circuit is attached to stabilize the output common mode signal. The output function of the amplifier is formulated in (3-1) with the capacitive mismatch value in its amplitude. By sensing the value, we can detect the change of the capacitance.

$$V_{out}(s) = \frac{g_{m1,2} R_{out}{}^2 \Delta C \cdot s}{(1 + 2 g_{m1,2} r_{o3})(1 + s/\omega_1)(1 + s/\omega_2)}$$
$$\omega_1 = \frac{1}{R_{out}(C_{sense} + C_p)}, \omega_2 = \frac{1}{R_{out}(C_{ref} + C_p)} \quad (3\text{-}1)$$

Rout value is the output resistance of CMEA and gm1, 2 is the transconductance value of the driving transistors M1 and M2. Also, ro3 means the output resistance of M3 and Cp is the symbol for the parasitic capacitance around the output port. Finally, Δ C means Csense-Cref value.

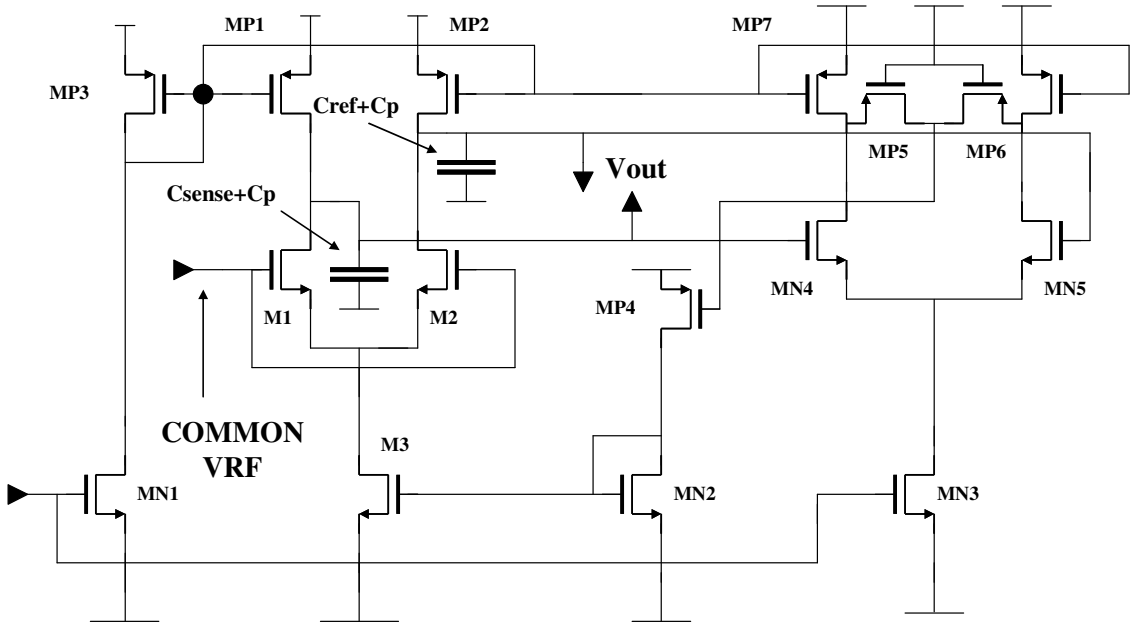

Fig. 14. Common mode error amplifier with CMFB.

Table 1. Design parameters of the common mode error amplifier.

TRANSISORS	SIZE	TRANSISORS	SIZE
M1	**1.62um/0.54um**	**MP1**	**1.98um/1.53um**
M2	**1.62um/0.54um**	**MP2**	**1.98um/1.53um**
M3	**1.44um/0.36um**	**MP3**	**1.8um/0.54um**
MN1	**1.44um/0.36um**	**MP4**	**0.72um/1.215um**
MN2	**1.44um/0.36um**	**MP5**	**0.18um/0.27um**
MN3	**3.015um/360um**	**MP6**	**0.18um/0.27um**
MN4	**0.27um/0.18um**	**MP7**	**0.585um/0.18um**
MN5	**0.27um/0.18um**	**MP8**	**0.585um/0.18um**

3.1.3.3.2 Mixer with the Back-end Amplifier

The single balanced mixer and the back-end amplifier demodulate and amplify the output signal from CMEA. The used topology is shown and the design parameters are tabulated in Table 2.

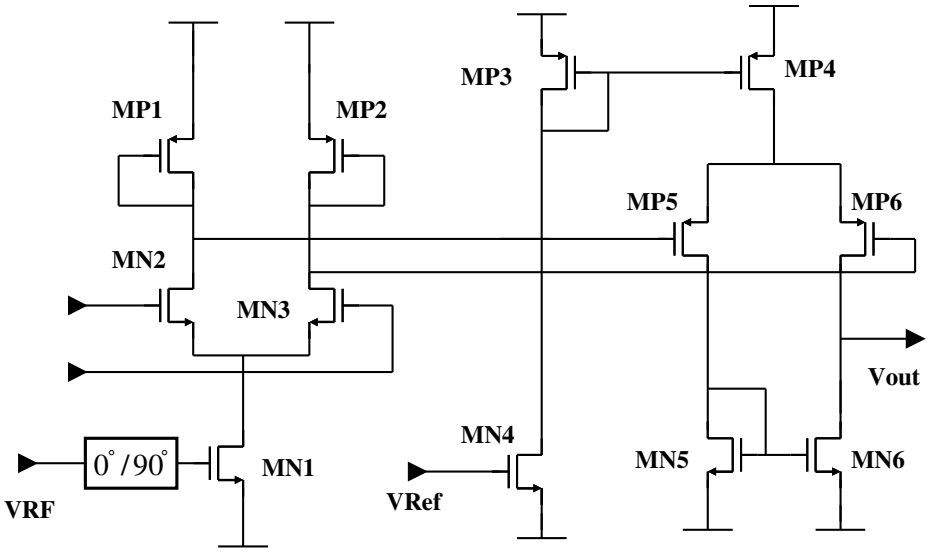

Fig. 15. The mixer stage with the back-end amplifier.

In this stage, the low frequency noise signal transfers into the high frequency range around the carrier frequency. Demodulated signal carrying the capacitance mismatch information transfers into the low frequency range for future low-pass filtering. Minimizing parasitic capacitance of participating transistors is the most important factor for implementing a circuit handling very high frequency signals from CMEA. Therefore, the very conventional single-balanced mixer topology will be proper to be used for achieving minimum parasitic capacitance value. That simple topology is also good for reducing the power consumption at the mixer. Additionally, because the sensed capacitor

value is comparably small with the neighboring parasitic capacitance, the common mode error signal amplified at CMEA is estimated not to have the intense power enough to be directly fed into the current-mode ADC input stage. In other words, an additional amplifier is essential to provide the strong error signal for accurate analog-to-digital conversion in the current-mode ADC converter in the next stage. The conventional OTA amplifies the demodulated signal. As you can assume, a very simple topology was adopted to design an OTA in order to minimize the power consumption.

Table 2. Design parameters of the mixer and the back-end amplifier.

TRANSISORS	SIZE	TRANSISORS	SIZE
MN1	3.015um/0.36um	MP2	0.27um/0.495um
MN2	1.08umum/0.405um	MP3	7.92um/0.36um
MN3	1.08um/0.405um	MP4	7.92um/0.36um
MN4	1.44um/0.36um	MP5	0.81um/0.36um
MN5	1.215um/0.36um	MP6	0.81um/0.36um
MP1	0.27um/0.495um		

3.1.3.3.3 OTA-C LPF with the Voltage-Current Converter

We need a very low cut-off frequency low-pass filter to capture the main signal power located in the low frequency range and attenuate the noise signal power distributed over the high frequency range. OTA-C topology is one of the most popular and efficient ways to realize the integrated filter on the silicon without any external components. However, in order to realize a very small cut-off frequency with OTA-C

topology, a tiny transconductace value is indispensable for minimizing the size of the integrated capacitor and possibly the external capacitor. Among a wide variety of techniques, the current splitting technique [41] is selected to design an OTA with a very small transconductance. The resulting filter is the simple 1st order OTA-C lowpass filter. That's because the future digital signal processing can compensate for the inaccuracy of the 1st order filtering results and the simple circuit is better for low power design. Fig 16. shows the circuit implementation of the filter and voltage-to-current converter. Additionally, the conventional input stage of the current mode ADC [39, 40] is shown in the figure to facilitate the understanding that the output signal is the current. Moreover, the final design parameters are tabulated in Table 3.

Table 3. Design parameters of the OTA-C filter and voltage-to-current converter.

TRANSISORS	SIZE	TRANSISORS	SIZE
MN1	**0.27um/2.115um**	**MP3**	**0.27um/7.2um**
MN2	**0.27um/2.115um**	**MP4**	**0.27um/0.72um**
MN3	**0.27um/2.115um**	**MP5**	**0.27um/3.78um**
MN4	**0.27um/2.115um**	**MP6**	**0.27um/1.8um**
MN5	**0.495um/0.36um**	**MP7**	**0.27um/1.8um**
MP1	**0.27um/0.72um**	**MP8**	**0.27um/3.78um**
MP2	**0.27um/7.2um**	**MP9**	**0.63um/1.35um**

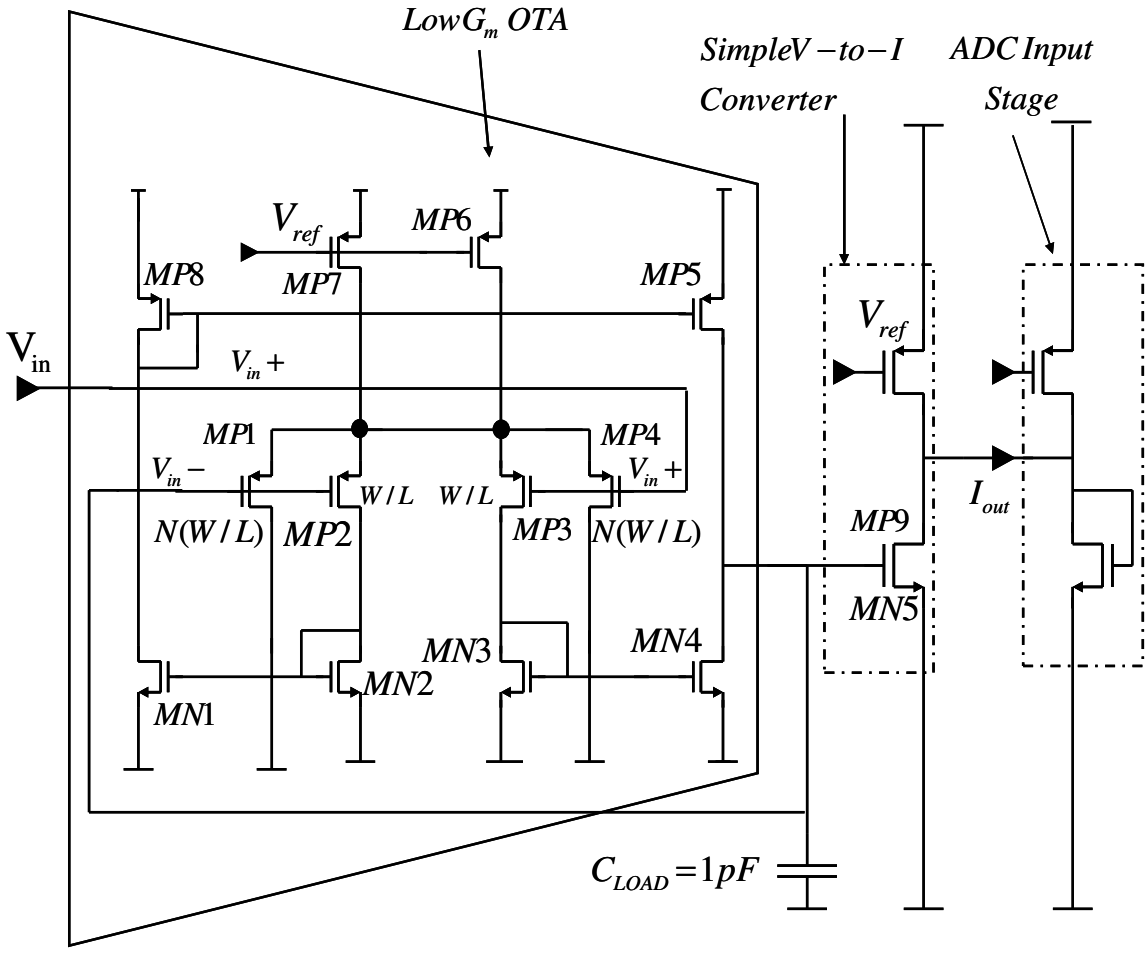

Fig. 16. OTA-C filter and voltage-to-current converter (N=10).

3.1.3.3.4 Noise Analysis and Process Variation Problems

Since this circuit is designed to measure a very small capacitance value change, the error caused by the internal circuit noise and offset would be serious. Therefore, the lock-in technique is used to cancel the low frequency noise and offset. However, the thermal noise of the circuit itself and the low frequency noise and offset of the sensing circuit itself will cause a considerable error at the final value. Therefore, by estimating

the internal error, we can calculate the minimum capacitance value mismatch which this system can sense.

First of all, we can calculate the output noise power spectrum density of CMEA in Fig 14 like (3-2). The current noise signals (in#) in these equations include the flicker noise and thermal noise together.

$$v_{nCMEA}^{\ 2} = i_{nm1}^{\ 2}(r_{om1} \parallel r_{ompl})^2 + i_{nm2}^{\ 2}(r_{om2} \parallel r_{omp2})^2 + \\ + i_{nmp1}^{\ 2}(r_{om1} \parallel r_{ompl})^2 + i_{nmp2}^{\ 2}(r_{om2} \parallel r_{omp2}) \qquad (3\text{-}2)$$

In the mixer in Fig 15, the noise signal from CMEA is multiplied with the mixing signal and the main power of the noise is transferred into the high frequency noise. The noise power spectrum at the output of the single-balanced mixer is formulated like (3-3). GMIXER means the gain of the single-balanced mixer.

$$v^2{}_{nMIXER} = \frac{G_{MIXER}^{\ 2}}{2} v_{nCMEA}^{\ 2} + i_{nmn2}^{\ 2}(1/g_{mp1})^2 + i_{nmn3}^{\ 2}(1/g_{mp2})^2 \qquad (3\text{-}3)$$

The noise signal from the mixer is amplified by the back-end amplifier. Taking the gain of the amplifier and the built-in noise into account, the total noise power spectrum density is formulated in (3-4).

$$v_{nBACK\_END}^{\ 2} = (g_{mp5}(r_{ompl} \parallel r_{omn6}))^2 v_{nMIXER}^{\ 2} + (i_{nmp5}^{\ 2} + i_{nmp6}^{\ 2})(r_{ompl} \parallel r_{omn6})^2 \qquad (3\text{-}4)$$

Finally, the output noise power spectrum density at the output of the lowpass filter in Fig. 16 is.

$$v_{nLOWPASS}^{\ 2} = \left(\frac{g_{mp2,3}}{g_{mp2,3}+sC}\right)^2 v_{nBACK\_END}^{\ 2} + \\ \left(\frac{i_{nmp7}^{\ 2} + i_{nmp6}^{\ 2}}{2N^2} + 2i_{nmp2,3}^{\ 2} + 2i_{nmn2,3}^{\ 2} + 2i_{nm1,4}^{\ 2} + 2i_{nmp8,5}^{\ 2}\right)(r_{omp5} \parallel r_{omn4} \parallel \frac{1}{sC_L})^2 \qquad (3\text{-}5)$$

The Lock-in Technique cancels the low frequency noise and offset, the flicker noise and low frequency offset in $v_{nCMEA}^{\ 2}$. The larger load capacitance of the filter can reduce the thermal noise of the filter itself in the relatively high frequency range. However, the size of the capacitor cannot be increased indefinitely because of the

limited area on the chip for integrated capacitors. Therefore, the optimal capacitance value is found to meet the noise requirement and size limit together. Since the thermal noise of the filter usually is smaller than the amplified low frequency noise of CMEA, it is much inefficient to use a large size integrated capacitor in order to minimize the thermal noise signal.

Moreover, the process variation is one of the most serious problems which make this circuit useless unless the variation is compensated for properly. Even though the stochastically accurate information can be extracted from the data collected in many sensor nodes, the minimization of the effect of the process variation on the circuit performance is required. Monte Carlo simulation is one of the best techniques to check the effect. Therefore, the simulation is the essential step to be conducted before the fabrication.

Also, the parasitic capacitance difference between the two outputs of CMEA can cause serious problem because it assumes the parasitic capacitance of each output has the same value. So, the calibration circuitry is required. The circuit should calibrate the output value of CMEA before the capacitance value is connected to CMEA. Therefore, CMEA can measure only the sensed capacitance value change. The calibration circuit design would be the future work.

3.1.3.4 Simulation Results

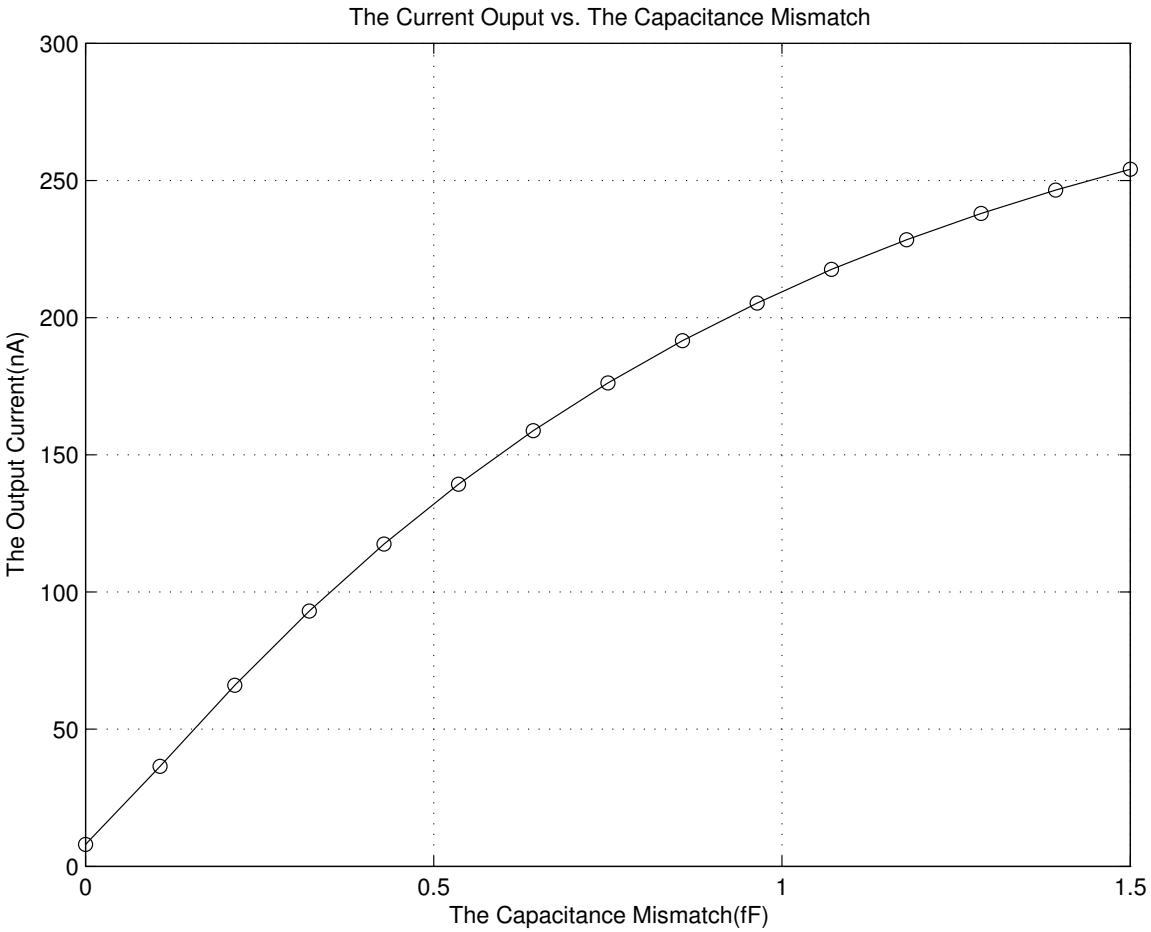

Fig. 17. The output current vs. the capacitance mismatch plot for 1 GHz 20mV amplitude input VRF signal.

The overall circuit was simulated with the low power current-mode ADC input section [39] shown in Fig 16. The reference capacitor and the sensed capacitor have very small capacitor value of few femto farads. It is because this circuit was designed for sensing the very small capacitance of a nano-size silicon structure used for chemical sensing using innovative dense integration technique of the sensed capacitor and the signal sensing circuitry together on the same chip. Due to the recent advancement in semiconductor technology, such a small capacitor can be realized on the silicon with the conventional lithography [4]. The circuit was designed with the conventional 0.18um CMOS technology and ±0.65V power supply. Fig. 17 demonstrates that this circuit has the quasi-linear relationship between the output current and the capacitance mismatch. The dotted line shows that the quasi-linear conversion ratio is about 164pA/aF and the overall power consumption is about 30uW with 1 GHz modulating signal.

Fig. 18 shows the transient response plot of the readout circuit output current. As you see, the output current stabilizes until 10us. Since the high speed response time is not the mandatory requirement for chemical and biological sensors. 10uS response time is fast enough for the sensor application.

Fig 19. shows the Monte Carlo Simulation result of the output current. The simulation is based on the assumption that standard deviation of the threshold voltage and the mobility is about 0.5%. It shows some deviation from the mean value. However, if thousands of sensor nodes are used in order to form an entire sensing system, those deviations are mutually cancelled by averaging effect. Therefore, it is possible that the system has good accuracy.

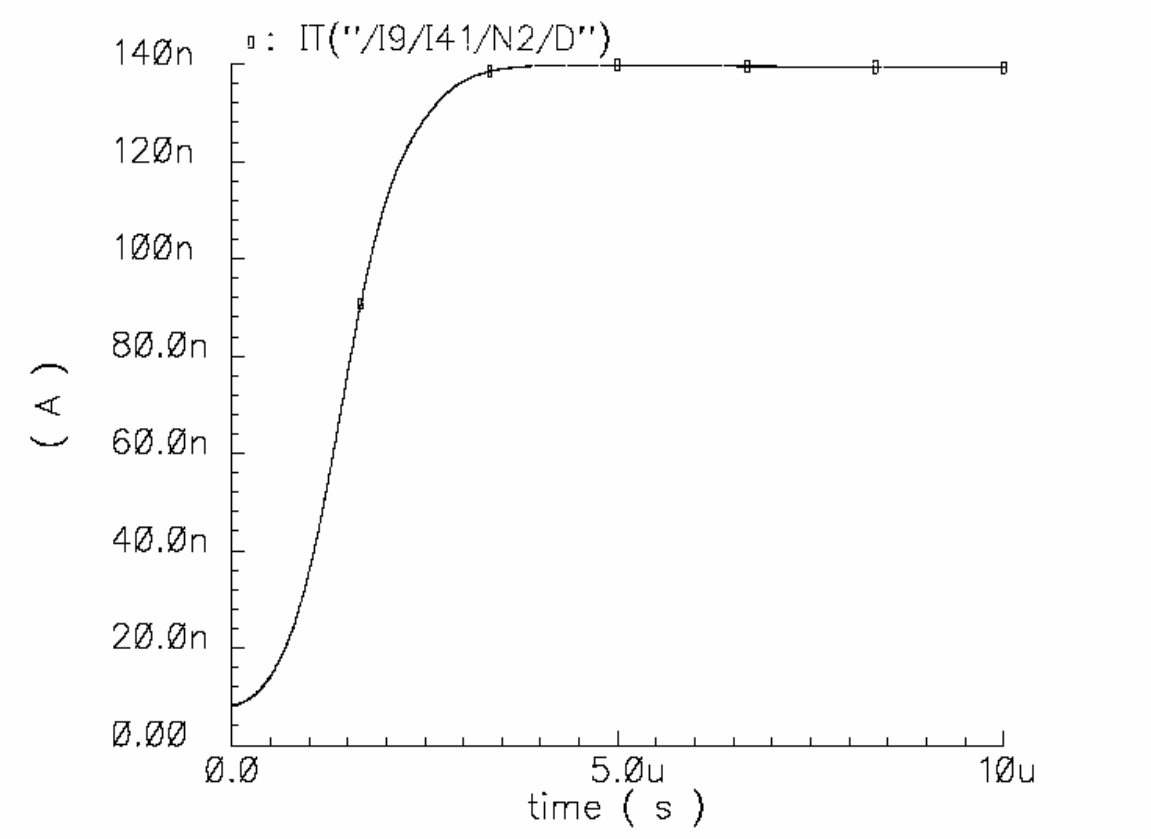

Fig. 18. The output current transient response plot with 1fF capacitance mismatch with 20mV input amplitude and 1 GHz frequency.

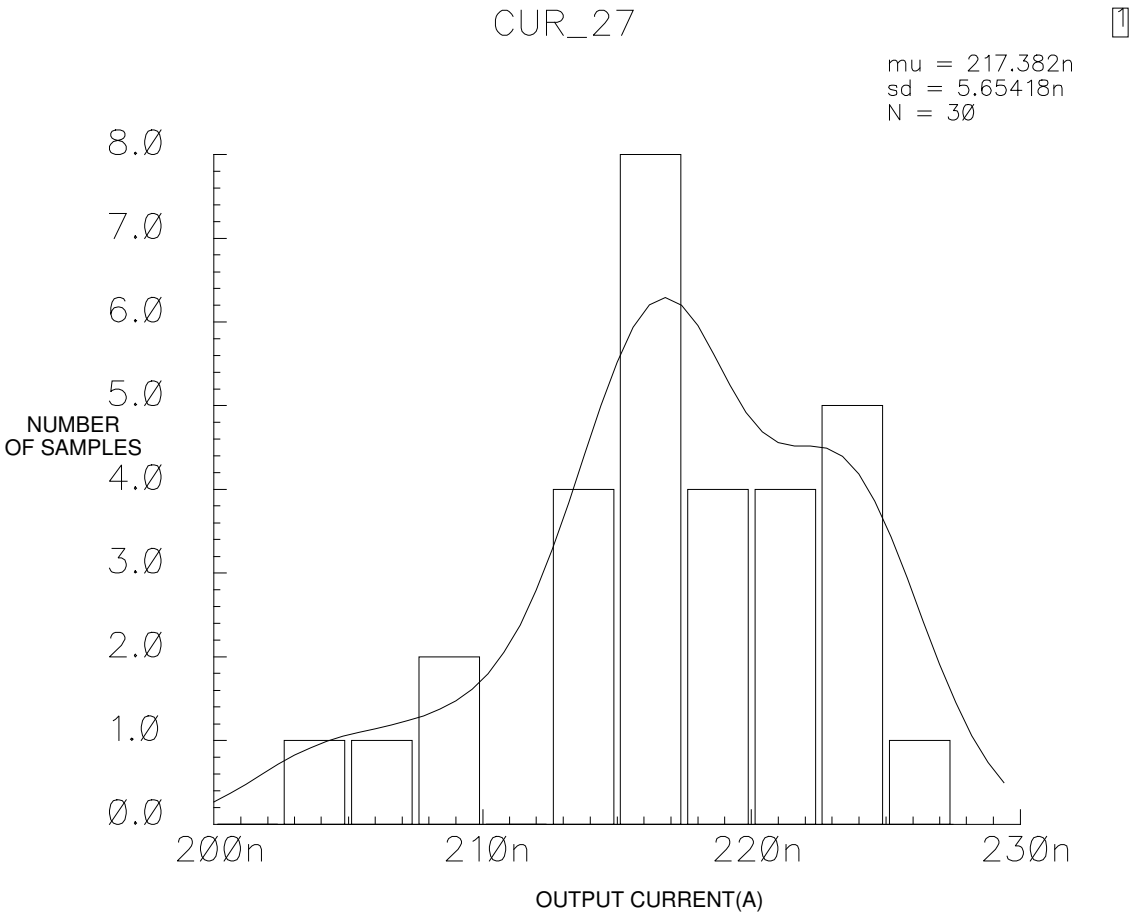

Fig. 19. The Monte Carlo simulation result of the output current with 1 GHz, 20mV input signal and 1fF sensed capacitor. It assumes 0.5% standard deviation of VT and the mobility.

3.2 Chemical and Biological Sensing Front-end Using Fluctuation Noise

3.2.1 System Level Implementation

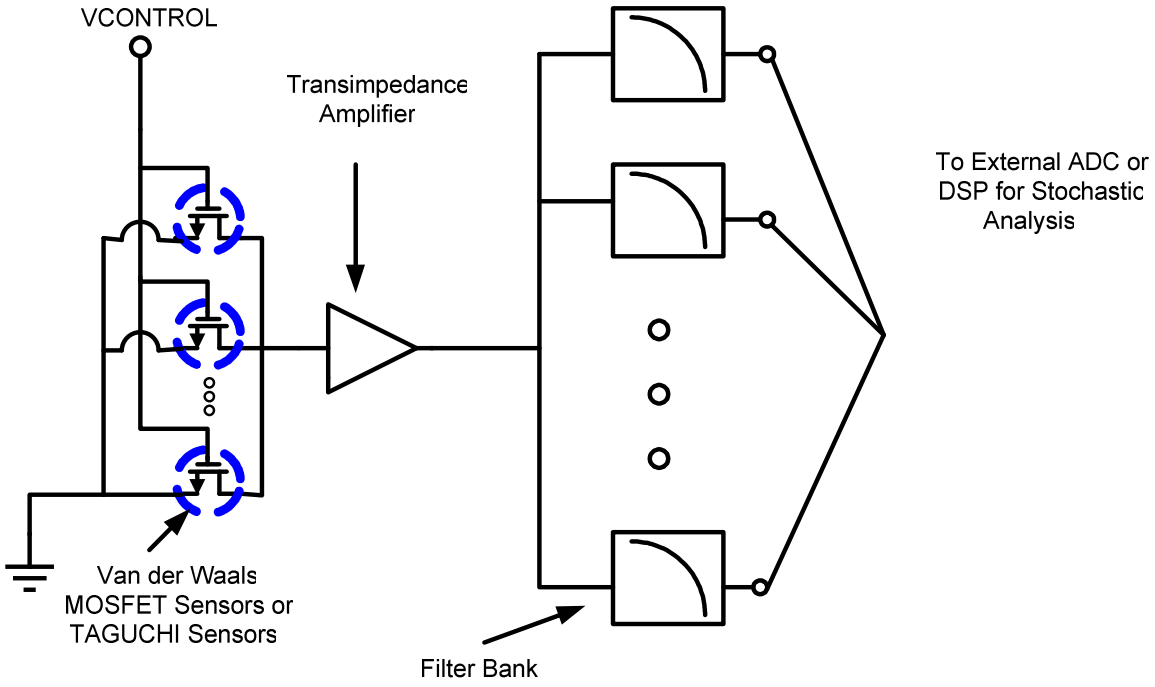

Fig. 20. System level block diagram of the CMOS sensing front-end using the fluctuation noise.

Fig. 20 shows the system diagram of the chemical sensing system using van der Waals MOSFETs or Taguchi type sensors. The transimpedance amplifier accepts the stochastic fluctuation noise current as its input and amplifies it to a considerable voltage signal. The amplified voltage signals become the input signals of the low pass filter array. The lowpass filter array provides a convenient mechanism to monitor "selected" regions in the frequency response of the sensor signal for "distinguishable" features specific to the particle under detection. The filter array provides functionality similar to a

matched filter array in a communication receiver. Higher SNR and higher selectivity is achieved using such an array. The output signal of each filter is fed into an external ADC or DSP for stochastic analysis.

Realizing a very low cut-off frequency in the lowpass filter array is the most important for the system implementation. Moreover, the filters should be designed so that they keep their cut-off frequencies strictly constant over wide range of temperature variation. Most sensors based on thin films exhibit high selectivity and sensitivity at operating temperature in the range of 200℃ or higher. In other words, the additional circuitry which helps an operational transconductance amplifier achieve a constant gm value regardless of the temperature variation is required. Also, the biasing circuitry to compensate for the parameter variations of MOS transistors is the indispensable sub-block in this system. In this chapter, a novel OTA-C filter is designed, which integrates the constant gm biasing circuit and the high temperature compensation circuit together to guarantee the stable high temperature operation with wide temperature variation range.

3.2.2 Fully-differential 1st Order OTA-C Filter Design Considerations

3.2.2.1 Resistor

Basic idea of an OTA-C filter is to realize the resistance value with the transconductance value. Fig. 21 shows the typical implementation of a resistor with a transconductor.

It shows a transconductance with its negative output terminal connected back to its positive input terminal. Since the transconductance input is ideally an open circuit, the input current Ii is equal to the transconductance output current Io=gmVi, thus

$$I_i = I_o = g_m V_i \qquad (3\text{-}2)$$

As a result, the circuit represents a resistor:

$$R = \frac{V_i}{I_i} = \frac{1}{g_m} \qquad (3\text{-}3)$$

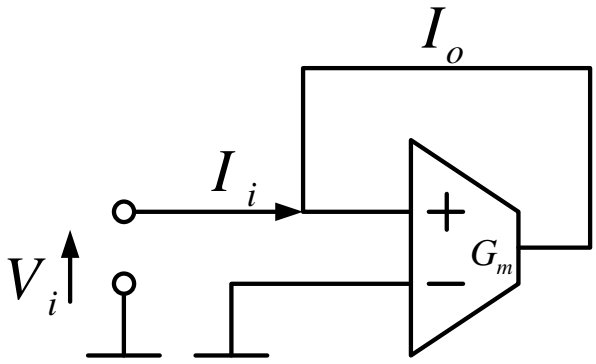

Fig. 21. A typical implementation of a resistor with a transconductor.

Based on the above equation, we can understand that a resistor can be realized with a transconductance value. Using this property, we can replace the external resistor which requires a wide area or an integrated silicon resistor which is very sensitive to the process variation.

3.2.2.2 First Order Low Pass Filter

We understand that we can get the better filtering performance if we use a high order filter at the cost of increased area and high power consumption. In this application, the output signals of each filter are processed by an external digital signal processor. Therefore, the high-level accurate signal processing is not required in the filter. Also, if we use a high order filter on the chip, the limited chip size will be the most serious bottleneck for integrating a great number of sensing nodes. Therefore, in this application, a first order filter (integrator) topology is the best fit. Let's turn our attention to the implementation of an integrator.

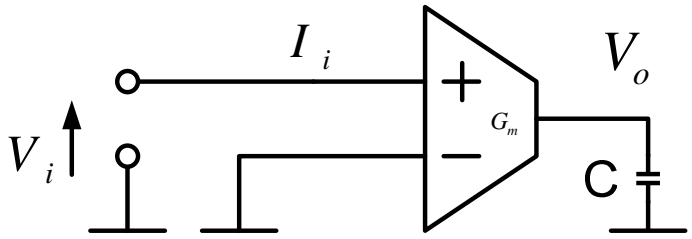

Fig. 22. A single-ended voltage-mode gm-C integrator.

We can see a single-ended voltage-mode gm-C integrator in Fig. 22. The Laplace transfer function of the circuit becomes

$$V_o = \frac{g_m}{sC} \text{ if the transconductor is ideal.} \qquad (3\text{-}4)$$

However, the above topology does not provide any controllability of its cut-off frequency. Therefore, we have to integrate a resistor made by a transconductor to a single-ended voltage-mode integrator illustrated in Fig. 22.

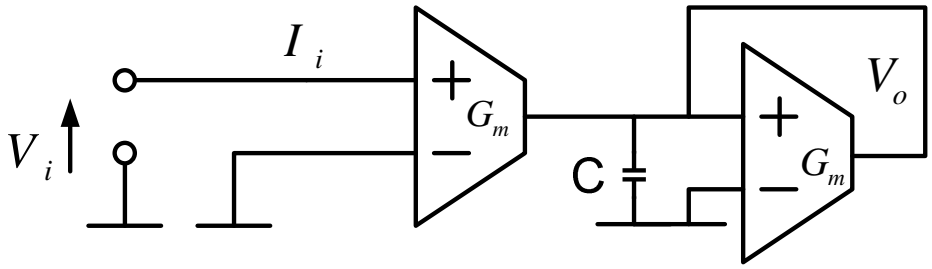

Fig. 23. Single-ended first order gm-C filter.

The circuit in Fig 23. shows a voltage-mode single-ended first order low pass filter. The Laplace transform function of the circuit becomes

$$\frac{V_o}{V_i} = -\frac{g_{m1}}{sC + g_{m2}} \qquad (3\text{-}5)$$

As seen in 3-5, we can change the cut-off frequency of the low pass filter by changing gm2 value.

However, a single-ended filter is not appropriate for low noise application. Fully differential filter is more proper than a single-ended filter for better noise performance. We can realize a fully differential first order filter by merging two single-ended first order filters. Fig. 24 shows the concept of a differential integrator consisting of two single-ended integrators. Since two single-ended integrators are fully symmetric to each other, we can merge the corresponding transconductors in the two paths each into one fully differential transconductor. Fig. 25 shows the resulting fully differential integrator. We have to understand that we doubles their input voltage by merging two transconductors. This means that the output currents are also doubled and we have to double the capacitor. We can find the Laplace transform function by following the steps below.

$$V_o^+ 2sC + (V_i^+ - V_i^-)g_{m1} + (V_o^+ - V_o^-)g_{m2} = 0 \qquad (3\text{-}6)$$

$$V_o^- 2sC + (V_i^+ - V_i^-)g_{m1} + (V_o^+ - V_o^-)g_{m2} = 0 \qquad (3\text{-}7)$$

By subtracting (3-7) from (3-6), we find

$$(V_o^+ - V_o^-)2sC = -2g_{m1}(V_i^+ - V_i^-) - 2g_{m2}(V_o^+ - V_o^-) \qquad (3\text{-}8)$$

Finally, we can find

$$\frac{V_o^+ - V_o^-}{V_i^+ - V_i^-} = -\frac{g_{m1}}{sC + g_{m2}} \qquad (3\text{-}9)$$

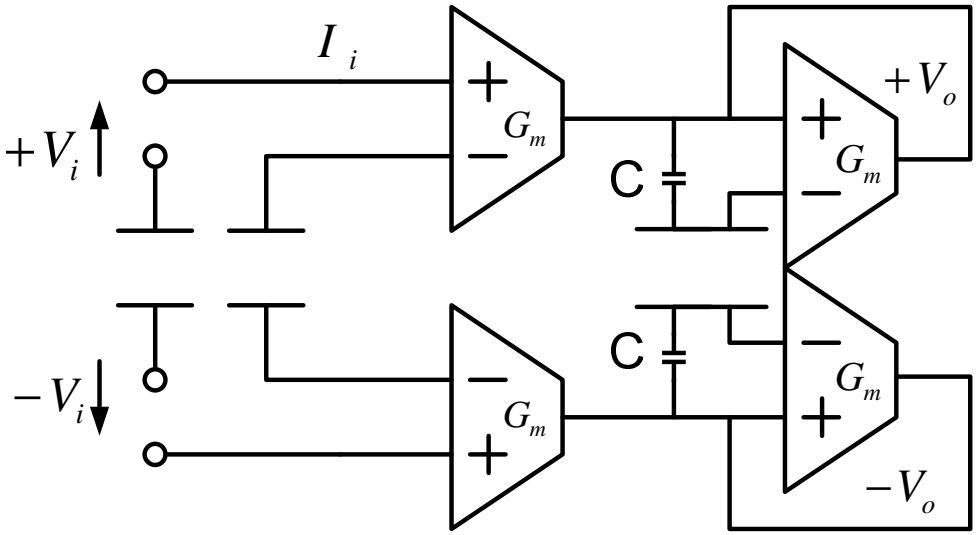

Fig. 24. Concept of a differential integrator.

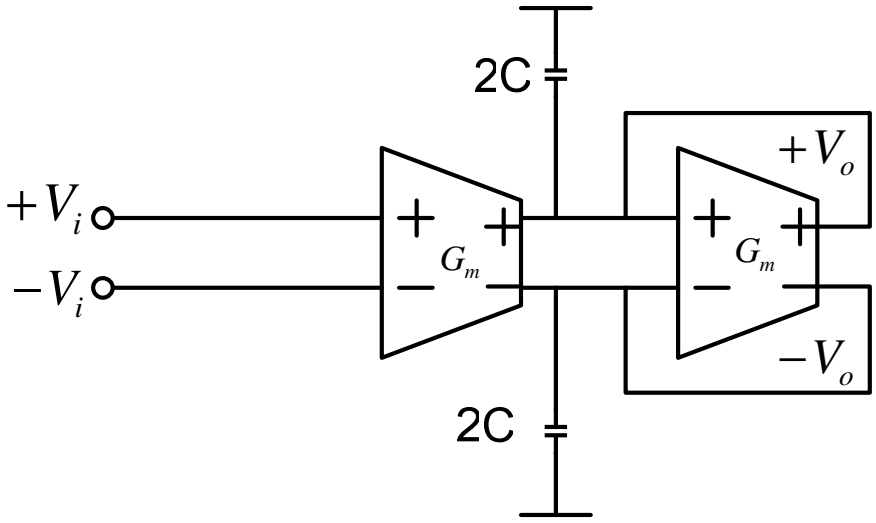

Fig. 25. Fully differential integrator.

3.2.2.3 Constant-gm Biasing

The only active component of an OTA-C filter is a transconductor. Therefore, we have to design a temperature insensitive transconductor in order to realize a temperature-insensitive filter. A great number of techniques have been invented. As one of them, "Fixed Transconductance Bias Circuit" proposed by Pavan [42] is used to design the bias circuit in this research.

In order to keep the transconductance value of a transconductor constant regardless of temperature and process variation, the value should be controlled to a temperature and process insensitive external resistor. This is a relatively simple tuning system in comparison with other complicated techniques. Fig. 26 demonstrates the conceptual schematic of a conventional resistor-control loop.

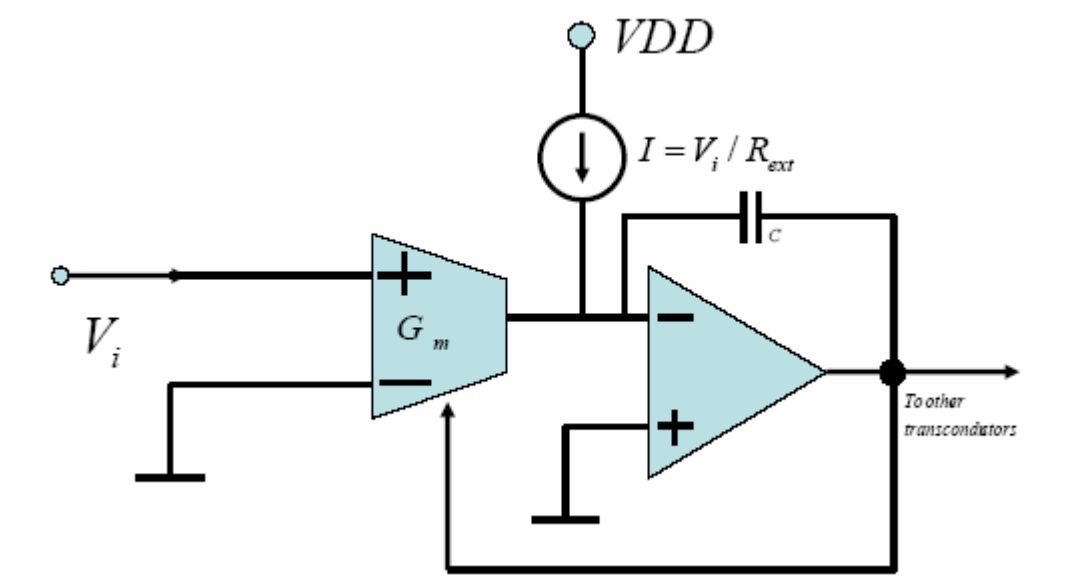

Fig. 26. Conceptual diagram of a conventional resistor-control loop.

The operational mechanism of this circuit is explained as follows. An input voltage Vi is applied to the transconductor, and its output is fed into the input of an

operation amplifier. However, the output is compared with the external current which has Vi/R value. So, only the difference between two current is integrated at the input of the opamp. Due to the negative feedback effect, the opamp output settles to the value which makes the transconductance value locked to 1/Rext. Also, this voltage is shared by the other transconductors.

However, using an additional opamp in this resistor-control loop is so bulky and inefficient. Utilizing the square law characteristics of a MOSFET is a very effective alternative of the traditional resistor-control loop. Let's assume that the MOSFETs work in saturation region and strong inversion. Also, mobility reduction due to gate field, velocity saturation and finite drain conductance are neglected. In this case, we can express the drain current like below.

$$I_{DS} = \frac{u_n C_{OX}}{2\alpha}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \qquad (3\text{-}10)$$

The basis for all the fixed transconductance-bias circuit in this research is based on Zele's paper shown in Fig 27[43]. The basic idea of this bias circuit is that the current generated in the bias circuit is used as the tail current for the differential pair formed by Ma and Mb. Of course, Vref is the common-mode reference for the filter. The current mirror formed by M3 and M4 forces identical currents through M1 and M2. Let me explain that using a couple of equations.

$$I_{M1} = \frac{u_n C_{OX}}{2\alpha}\left(\frac{W}{L}\right)(V_{GS1} - V_T)^2 \qquad (3\text{-}11)$$

$$I_{M2} = \frac{u_n C_{OX}}{2\alpha}\left(\frac{4W}{L}\right)(V_{GS2} - V_T)^2 \qquad (3\text{-}12)$$

$$I_{M1} = I_{M2} = I \qquad (3\text{-}12)$$

$$V_{GS1} - V_{GS2} = IR \qquad (3\text{-}14)$$

From 3-11,3-12,3-13,3-14, we can induce

$$V_{GS1} - V_T = 2(V_{GS2} - V_T) \qquad (3\text{-}15)$$

from 3-14 and 3-15, we can get

$$V_{GS1} - V_T = 2IR \text{ and } g_{m1} = \left(\frac{2I}{V_{GS1} - V_T} \right) = \frac{1}{R} \quad (3\text{-}16)$$

Therefore, we can understand that the circuit stabilizes to a state where the current maintains the transconductance as 1/R, regardless of any VT, u or temperature variation due to the negative feedback effect. However, the biasing condition of Ma and Mb is not same to that of M1 since the source voltage is different from each other. Therefore, we cannot guarantee that the temperature and process variation will be controlled enough.

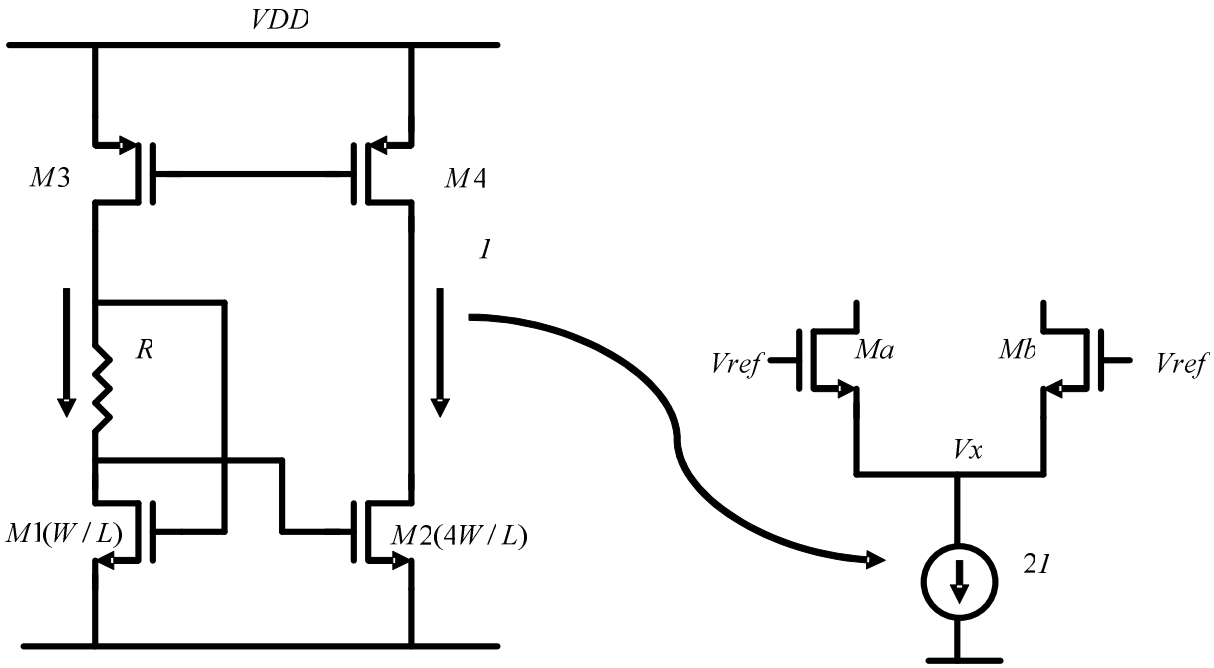

Fig. 27. Basic fixed transconductance bias circuit.

To fix this problem, we have to make the source voltage of M1 to Vx. The conceptual scheme is shown in Fig. 28. The voltage of the source coupled node of Ma-Mb is sensed and the sources of M1 and M2 are modified to have the same value to that of Ma-Mb. By doing so, we can make the operating condition of M1, M2, Ma and Mb same. So, we can take better performance. We can assume that the source of M1 and M2 is connected to a battery which has 2I current through it. The concept can be realized with the scheme in Fig. 29. M5 is used to mirror I flowing through M4. This current is multiplied by 3 in the NMOS mirror formed by M8 and M9. M9 works as a current sink of value 3I. Of this, 2I is supplied by M1 and M2, and I flows through M6 (M6 is of same dimension as Ma in Fig 27).So, it is said that the source voltage of M1 and M2 is Vx.

The more advanced circuit is shown in Fig 30. The output impedance of PMOS mirrors have been enhanced with cascode devices, and the drain of M6 has been tied to the gate (this is because the OTA works with unity feedback condition in OTA-C topology). M7, M10 and M11 operate in order to make the drain-source voltage of M8 and M9 same to each other for a wide range of Vref. Cc is the compensation capacitor to stabilize the loop formed by M7, M8, M10, and M11. Also, the resistor Rb isolates the bias voltage generated at the gate of M8 and M9 from the capacitive load which the circuit sees. Also, it increases the effectiveness of Cc at the high frequency.

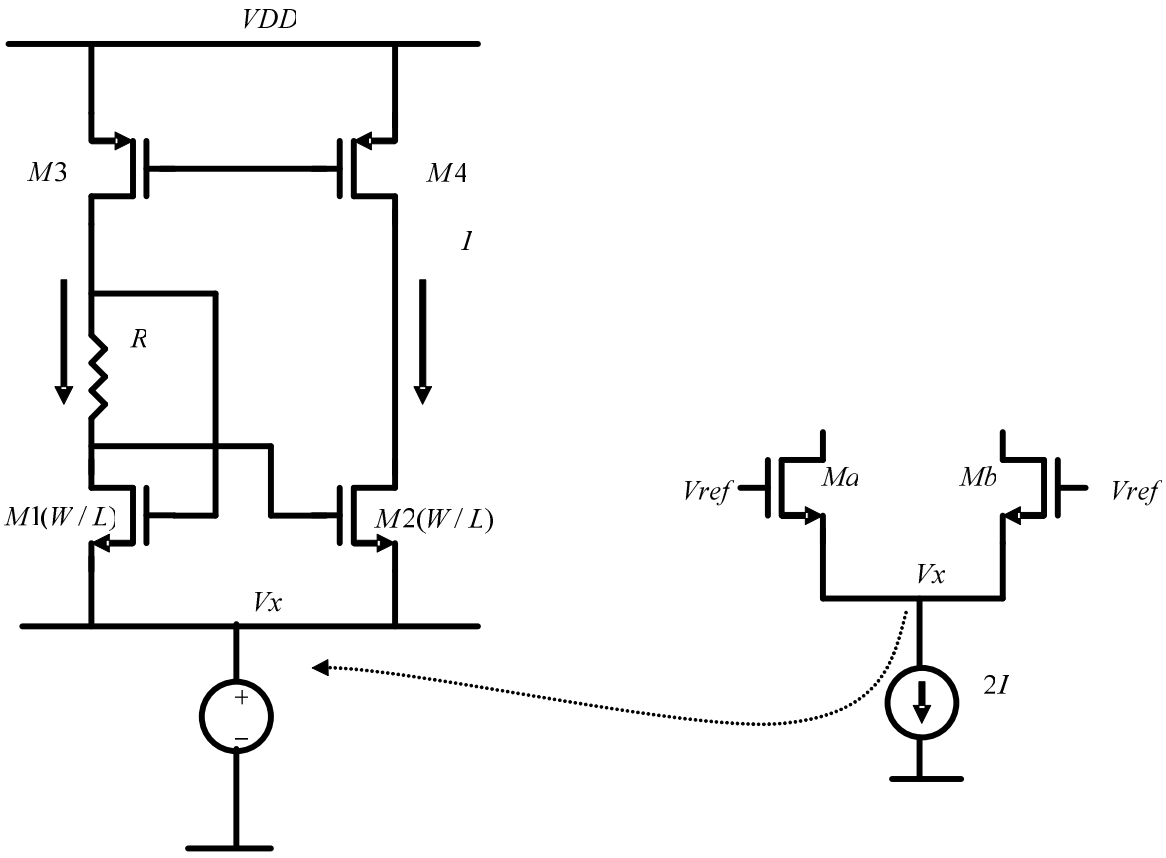

Fig. 28. Concept of an improved fixed transconductance bias circuit.

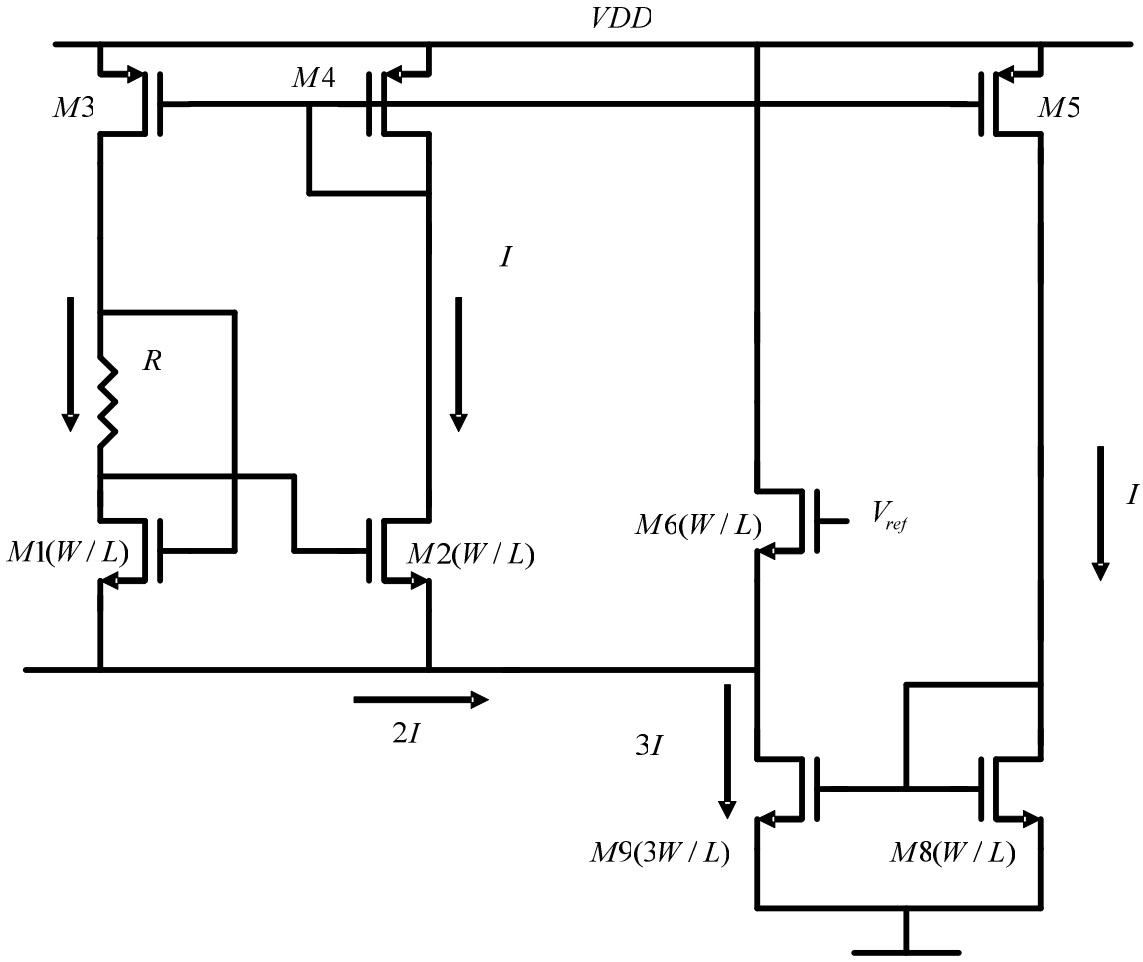

Fig. 29. Circuit implementation of the scheme of fig. 28.

3.2.2.4 High Temperature Compensation

Recently developed advanced CMOS technology demonstrated the ability to realize the high temperature operation(~250°C) of a CMOS device for analog or a digital circuitries[44]. However, the device parameters are truly dependent on temperature variation. The temperature sensitive parameters are Threshold Voltage, Average Effective Mobility, Zero-Temperature-Coefficient Bias Point and Leakage Current [44].

Assuming that we use the constant gm biasing circuit to compensate for the temperature and process variation while operating in the saturation, the influence of the temperature sensitive parameters is minimized. However, the leakage current at the high temperature can cause a serious problem to CMOS device operation.

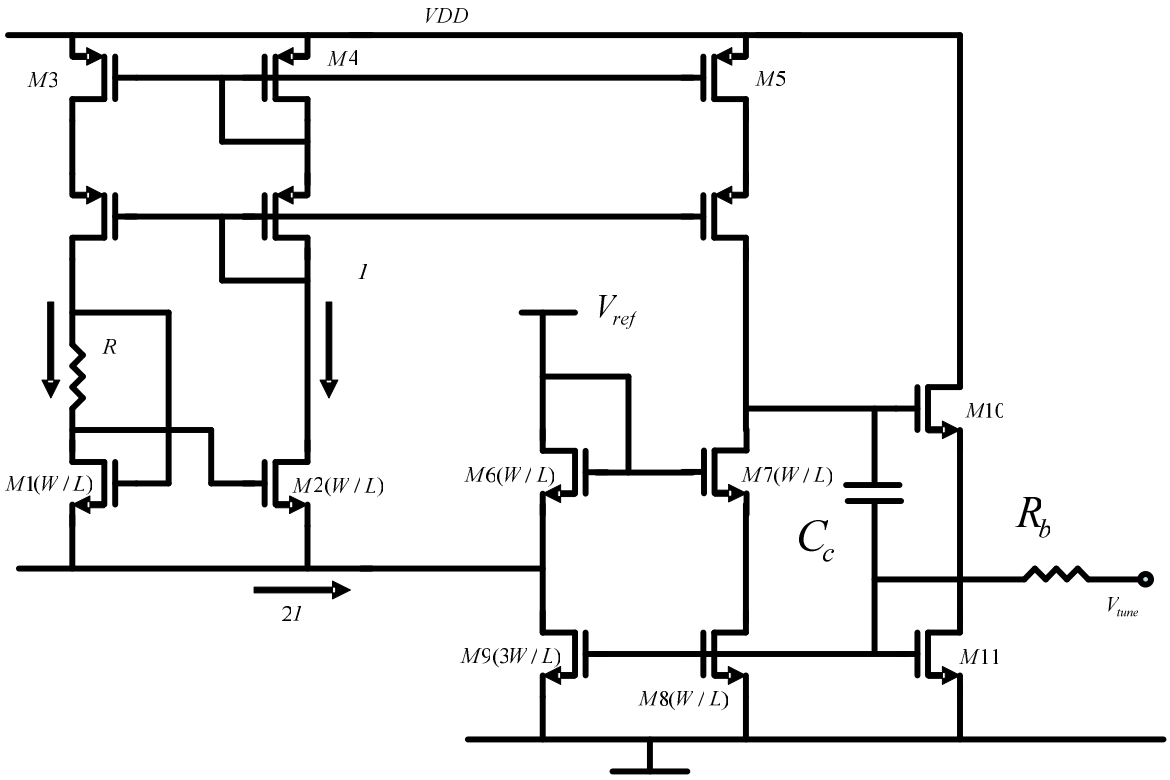

Fig. 30. Complete "fixed transconductance bias" circuit.

That's because of the considerable leakage current mismatch between a NMOS and a PMOS transistor. In Fig. 31 it may be seen that the curves measured at temperature exceeding 250°C exhibit a substantial upward shift along the current axis.

This is because drain (to body) leakage currents have become comparable to drain channel current. Usually, the drain leakage current has the four or five orders of magnitude smaller at 25°C than at 250°C (Fig 32). The drain (or source) junction leakage current is generally dominated by generation-recombination leakage between 25°C and Ttrans and by diffusion leakage between Ttrans and 250°C. Finding the exact value of Ttrans is a seriously difficult job. However, it is generally known to lie in 130-150°C [44]. In Fig. 32, it is shown that the leakage current of a NMOS device after Ttrans is highly more sizable than the PMOS counterpart. The diffusion leakage current of a NMOS device surpassing the PMOS counterpart after Ttrans is the major reason.

Therefore, we have to take into account the considerable leakage current mismatch between PMOS and NMOS devices for the high temperature operation. The effect of other temperature sensitive characteristics of semiconductor devices on the transconductance of a transconductor can be compensated for by the constant gm biasing circuit. However, the huge leakage current can cause the circuit to drift away from the proper biasing point at the high impedance point.

There are a few compensation circuitries proposed in the literature [44]. In this research, a very simple compensation circuit consisting of one "dead" PMOS and one "dead" NMOS transistor in Fig. 33 is used. The leakage current mismatch between two transistors flows into the high impedance point and compensate for its leakage current mismatch.

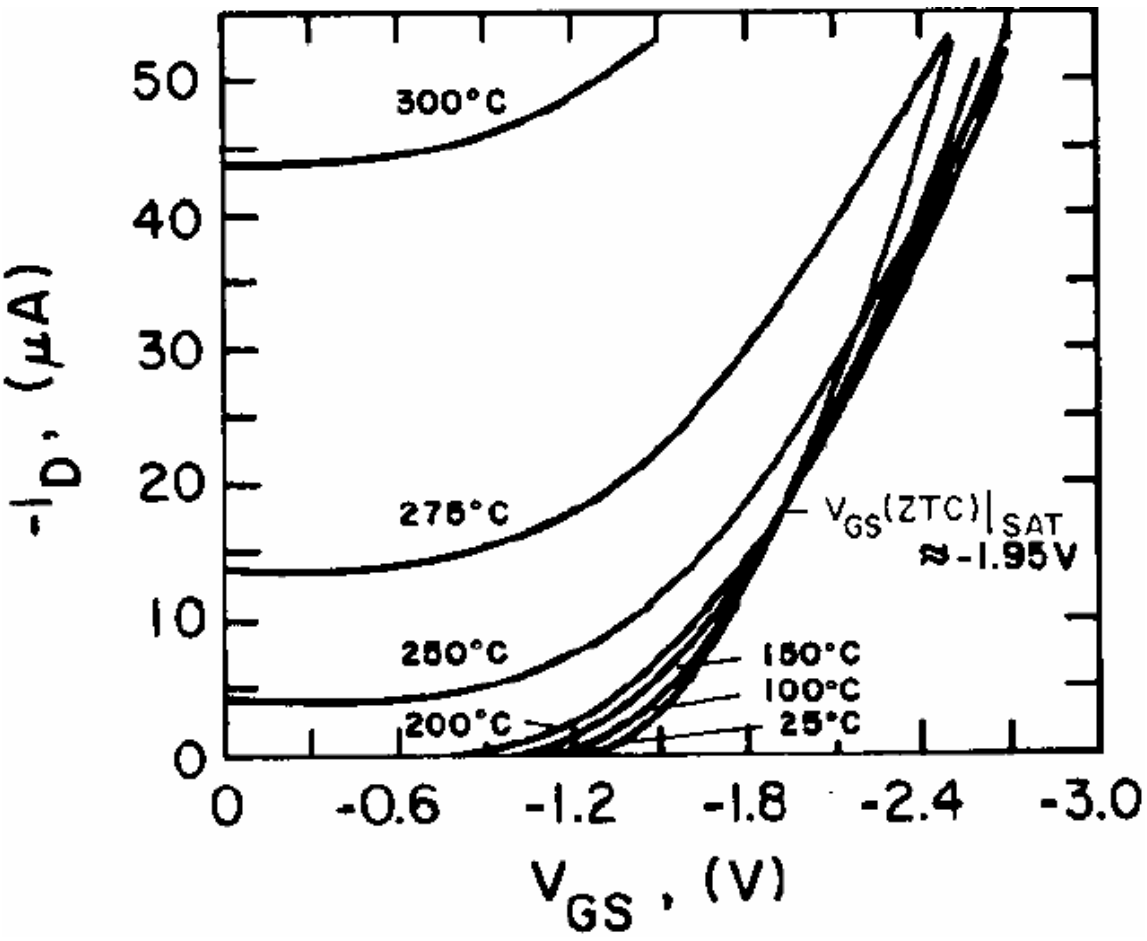

Fig. 31. Drain current characteristics of typical 50-pm/lo-pm p channel MOSFET with temperature as parameter in saturation (VDS = - 6 V) [44].

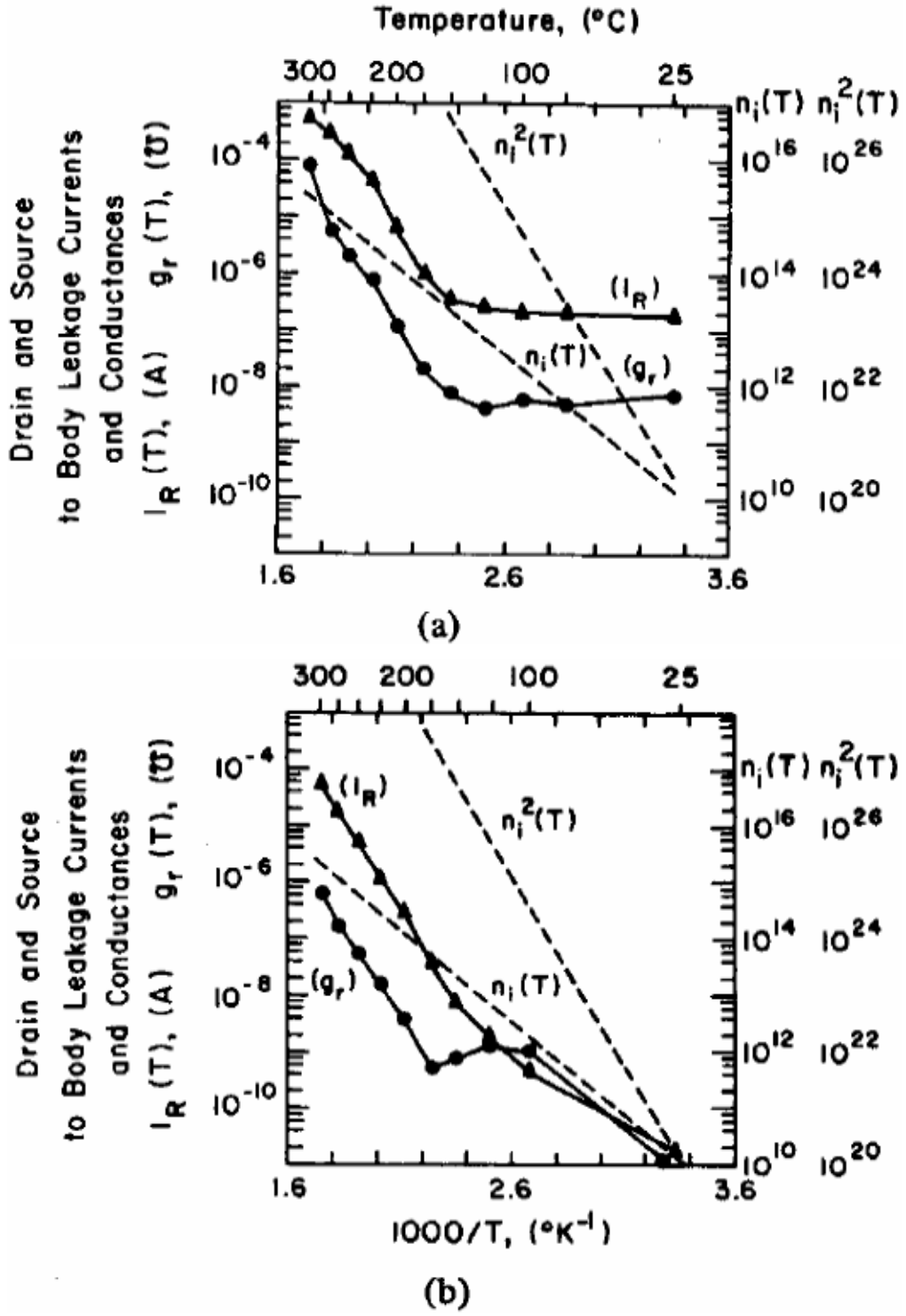

Fig. 32. MOSFET drain and source to body leakage currents and conductances. (a) N channel. (b) P channel [44].

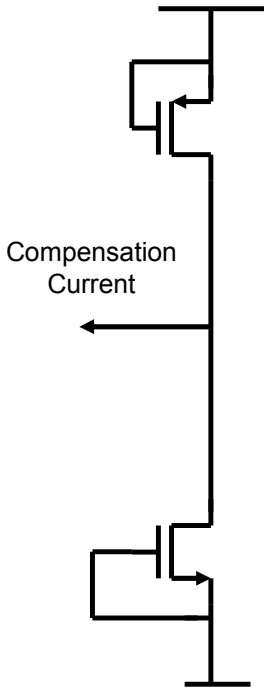

Fig. 33. Simple leakage current compensation circuit.

3.2.2.5 Low Frequency Noise Reduction

The suppression of the low frequency noise to increase SNR is very vital because the target noise signal power is located in the low frequency range. Lock-in technique might be considered as one of good solutions to diminish the low frequency noise power. However, the overlap between the target noise and the unwanted noise prevents the Lock-in technique from extracting pure signal from the mixed signals of the target and unwanted noise. Therefore, we have to figure out another technique.

The two major contributions to CMOS noise are the thermal noise and the flicker noise. The thermal noise is ideally distributed on the entire frequency range with the same power spectrum density. However, the flicker noise is mainly located in the low frequency range.

$$i_d^{\,2} = \frac{8kT}{3} g_m = \left(\frac{8kT}{3}\right)(uC_{OX})\left(\frac{W}{L}\right)(V_{GS} - V_T) \quad (3\text{-}17)$$

$$i_d^{\,2} = \frac{k_F I_{DS}}{C_{OX} L^2 f} \quad (3\text{-}18)$$

$$i_d^{\,2} = \left(\frac{8kT}{3}\right)(uC_{OX})\left(\frac{W}{L}\right)(V_{GS} - V_T) + \frac{k_F I_{DS}}{C_{OX} L^2 f} \quad (3\text{-}19)$$

k_F : *fitting parameter* f : *frequency* I_{DS} = *drain current*

(3-19) means the total noise current from one transistor. As you see, the noise power spectrum density depends on different variables. Therefore, controlling the density is feasible by adjusting them. However, due to the limited design flexibility, we cannot make use of many variables together simultaneously. So, the most dominant controlling factor for low noise should be found. The channel length is included in the thermal noise and flicker noise equation together. Also, the flicker noise at the low frequency is inversely proportional to the square of the channel length. Therefore, increasing the channel length is the most efficient technique to reduce the noise spectrum density, mainly low frequency spectrum density. Therefore, the relatively long channel length is used in this design for minimum noise spectrum density in case of output noise contributing transistors.

3.2.3 Final Practical Design Results

3.2.3.1 Whole System

Based on the design consideration, the whole fully differential first order low pass filter with high temperature operation is design as in Fig. 34. The IC is design with the conventional TSMC 0.18um CMOS technology.

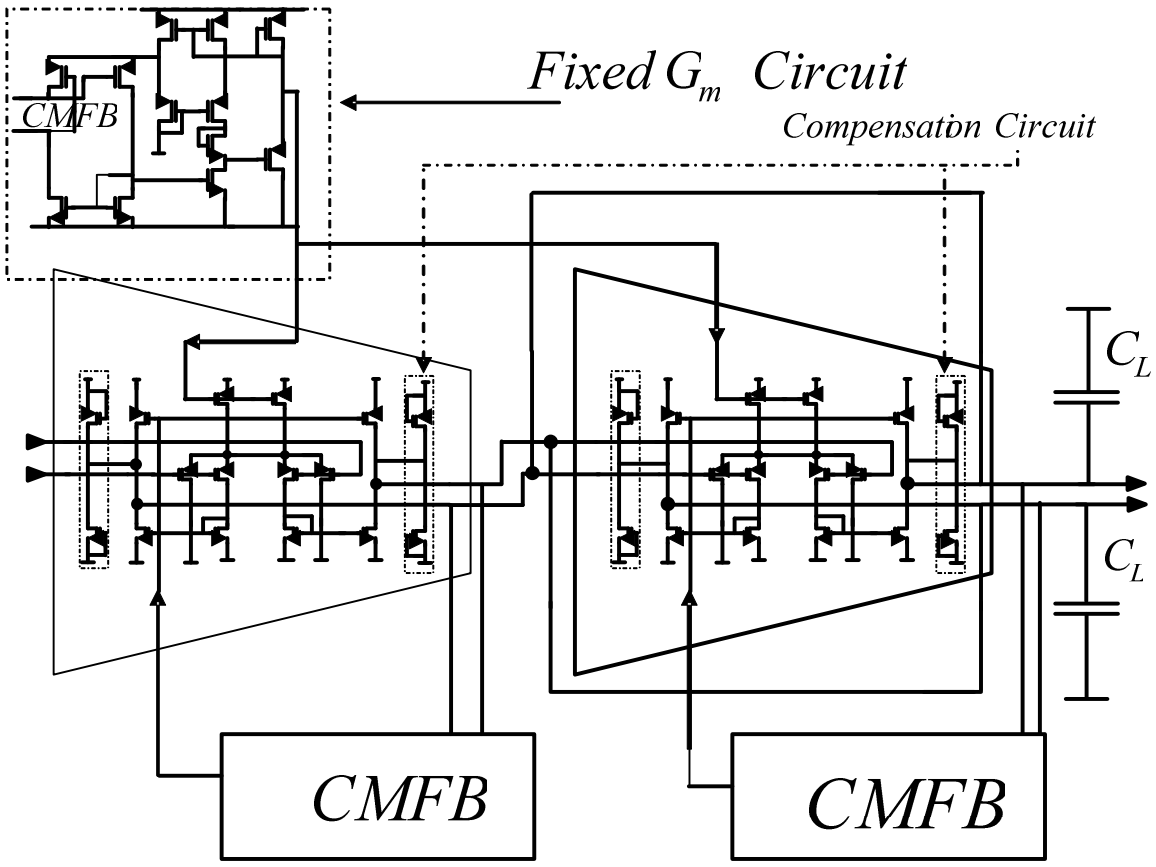

Fig. 34. The system diagram of the fully differential first order low pass filter with high temperature operation.

As explained before, two transconductors are used to build one filter. The current splitting technique [41] is used to achieve a very small transconductance value for extremely low cut-off frequencies. Also, a Common Mode Feedback circuitry is applied to suppress the common mode error and maintain a stable operating point. Moreover, the constant gm biasing circuit provides the adaptive reference voltage to operational transconductance amplifiers for the constant transconductace value over broad range of temperature.

3.2.3.2 Final Design Parameters

3.2.3.2.1 Constant-gm Biasing

The circuit topology illustrated in Fig.30 should be modified for use with the PMOS input differential stages of the transconductors. It is shown in Fig. 35 and the final design parameters are tabulated in Table 4.

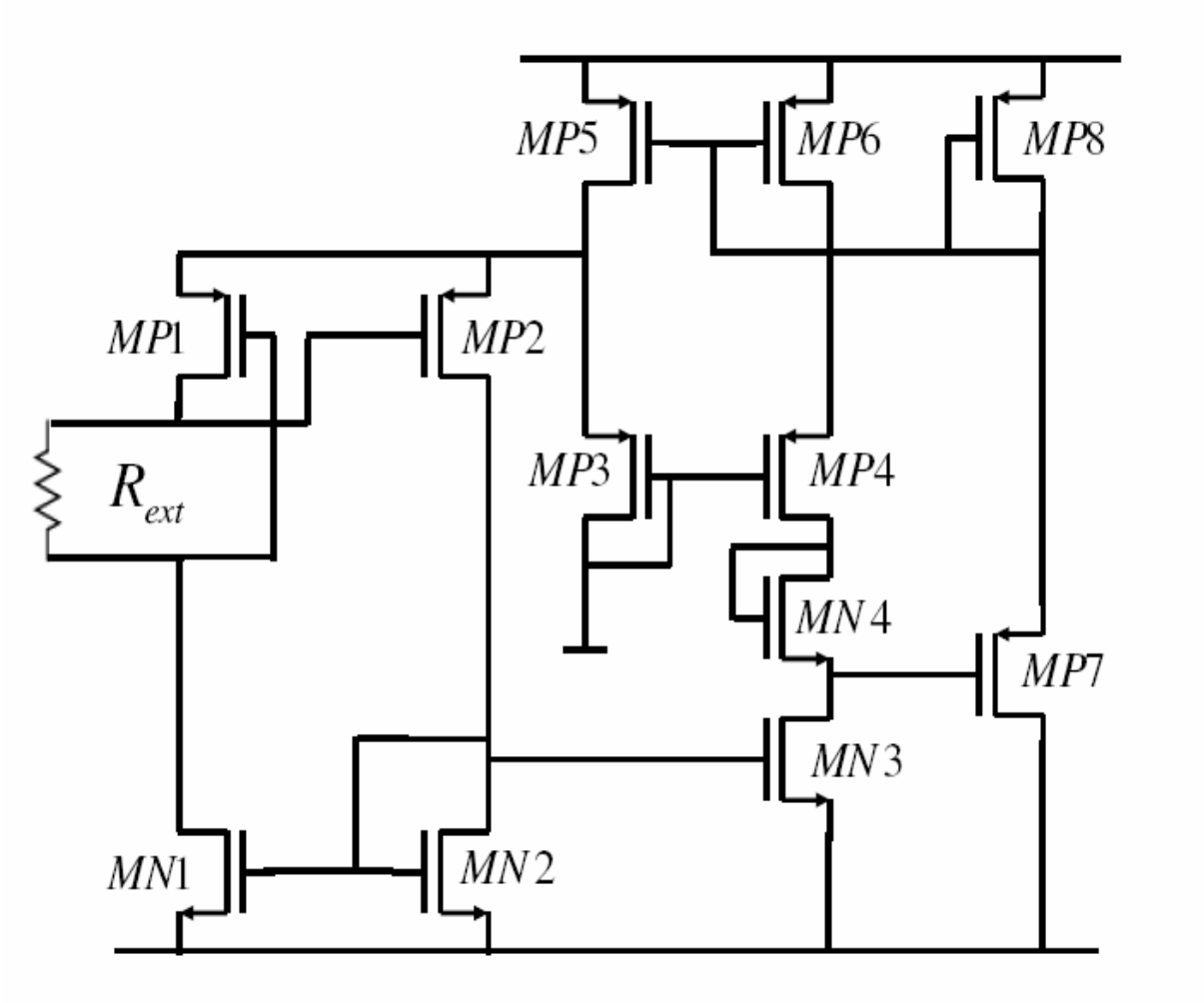

Fig. 35. Constant gm biasing circuit for a PMOS input stage.

Table 4. Constant gm bias circuit final design parameters.

TRANSISORS	SIZE	TRANSISORS	SIZE
MN1	**1.8um/0.945um**	**MP3**	**0.9um/0.945um**
MN2	**1.8um/0.945um**	**MP4**	**0.9um/0.945um**
MN3	**1.8um/0.945um**	**MP5**	**2.7um/0.945um**
MN4	**4.32um/0.18um**	**MP6**	**0.9um/0.945um**
MP1	**0.9um/0.945um**	**MP7**	**0.9um/0.945um**
MP2	**3.6um/0.945um**	**MP8**	**0.9um/0.945um**
Rext	**270K**		

3.2.3.2.2 Operational Transconductance Amplifier

To realize a variety of filters with different cut-off frequencies, four distinctive operational transconductance amplifiers of the same sort are designed with their own transconductance value. The used topology is shown in Fig. 36 and the final design parameters are tabulated in Table 5 and 6.

As you see, the channel of the transistors is very long. The long channel leads to the serious size problem in the integrated sensor system. However, the minimum low frequency noise is required to boost up SNR of the target signal mixed with the low frequency noise. The usage of the long channel length is very effective to realize a very small low frequency noise spectrum. Therefore, the very long channel length is applied in the circuit for the minimum flicker noise spectrum at cost of the size.

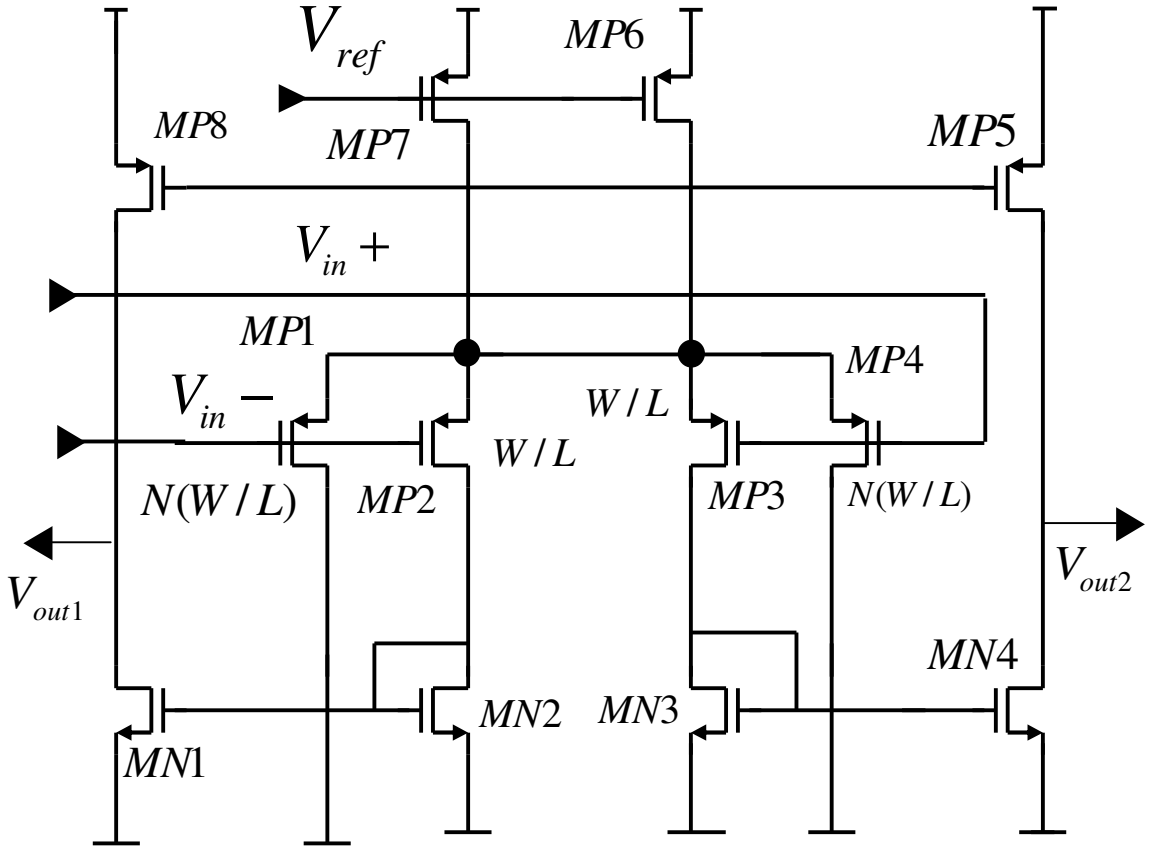

Fig. 36. Operational transconductance amplifer diagram.

Table 5. Operational transconductace amplifier design parameters A

TRANSISTOR	GM=1.8nA/V	GM=15nA/V
MN1	0.27um/360um	0.27um/210um
MN2	0.27um/360um	0.27um/210um
MN3	0.27um/360um	0.27um/210um
MN4	0.27um/360um	0.27um/210um
MP1	0.9um/0.945um	0.27um/0.945um
MP2	0.27um/360um	0.27um/93.24um
MP3	0.27um/360um	0.27um/93.24um
MP4	0.9um/0.945um	0.27um/0.945um
MP5	0.27um/360um	1.215um/210um
MP6	0.63um/1.8um	0.63um/1.8um
MP7	0.63um/1.8um	0.63um/1.8um
MP8	0.27um/360um	1.215um/210um
N	1270	99

Table 6. Operational transconductace amplifier design parameters B

TRANSISTOR	GM=150nA/V	GM=2.2uA/V
MN1	0.27um/21um	0.27um/2.115um
MN2	0.27um/21um	0.27um/2.115um
MN3	0.27um/21um	0.27um/2.115um
MN4	0.27um/21um	0.27um/2.115um
MP1	0.27um/0.945um	
MP2	0.27um/9.225um	0.315um/0.585um
MP3	0.27um/9.225um	0.315um/0.585um
MP4	0.27um/0.945um	
MP5	0.27um/4.5um	3.42um/2.115um
MP6	0.63um/1.8um	0.63um/1.8um
MP7	0.63um/1.8um	0.63um/1.8um
MP8	0.27um/4.5um	3.42um/2.115um
N	10	

3.2.3.2.3 Common Mode Feedback Circuit

Since the OTA is fully differential, CMFB circuit is required. A very conventional CMFB topology is used in Fig. 37 and the final design parameters are tabulated in Table 7.

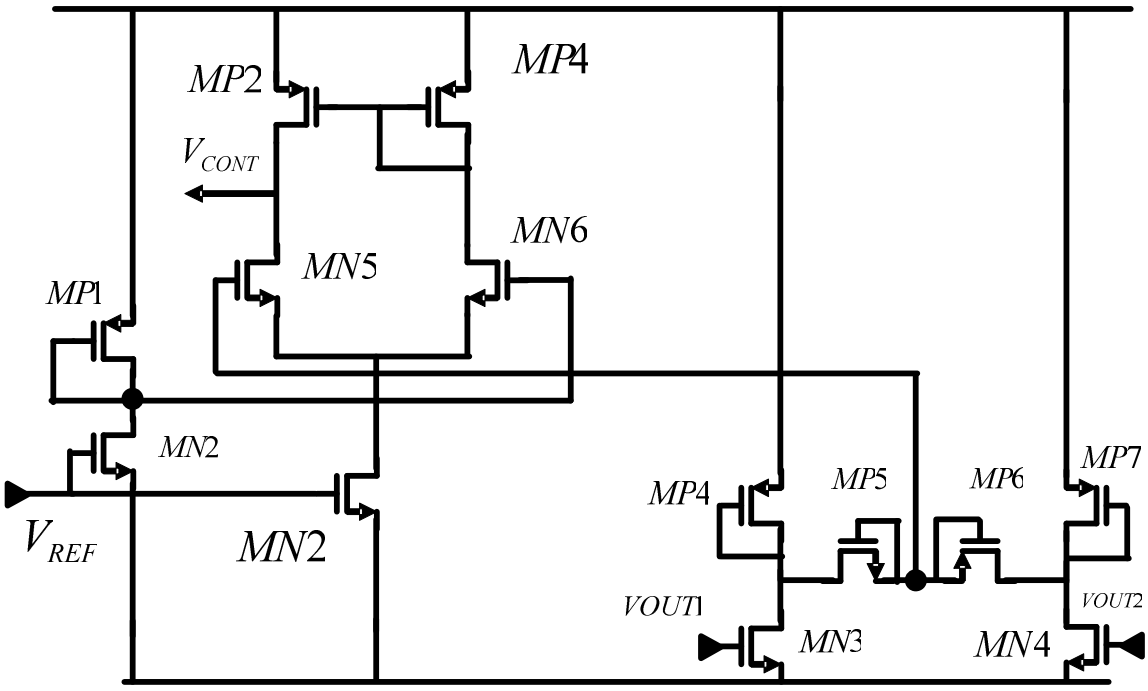

Fig. 37. Common mode feedback circuit.

Table 7. Design parameters of the common mode feedback circuit.

TRANSISORS	SIZE	TRANSISORS	SIZE
MN1	**0.27um/5.4um**	**MP2**	**8.46um/0.18um**
MN2	**0.45um/0.27um**	**MP3**	**8.46um/0.18um**
MN3	**0.27um/5.4um**	**MP4**	**0.315um/0.54um**
MN4	**0.27um/5.4um**	**MP5**	**0.315um/0.18um**
MN5	**0.9um/0.945um**	**MP6**	**0.315um/0.18um**
MN6	**3.6um/0.945um**	**MP7**	**0.315um/0.54um**
MP1	**0.315um/0.54um**		

3.2.3.3 Simulation Results

Fig.38 demonstrates that the filters in the array operate properly at very high, 0dB and the typical lowpass filter frequency response. Moreover, Fig. 39 shows temperature (~200°C). Also, it shows a trivial deviation of the filter gain from the ideal value the very stable variation of 3dB point of Filter #3 in Table 8. As you see, the deviation of the 3dB point is so small that the filter can operate at the high temperature without serious modification. Numerically, for the above case, only 16% of the starting 3dB point value changes from 0°C to 200°C. Therefore, it is concluded that the filter maintains a relatively fixed 3dB point over the wide temperature variation due to the constant gm biasing circuit.

All the filter specifications achieved in the simulation are tabulated in Table 8 and 9. Actually, the filter array and the transimpedance amplifier are fabricated together on the same chip. So, the real independent test of each block is infeasible. However, by performing the independent filter simulation, we can predict the actual filter performance and attain the supporting knowledge for measuring the actual independent filter performance from the real composite test result with the integrated circuit.

Especially, two of the circuit performance parameters draw careful attentions. One is the output noise level inherent in the system. It is the major determinant of the minimum amplitude of the input noise signal into the filter. So, the minimum output noise level is required. Another is Total Harmonic Distortion (THD). It is one of the most dangerous system degrading factors. The system distortion represented by THD will restrict the system dynamic range most seriously. Therefore, the effort to minimize THD is vital.

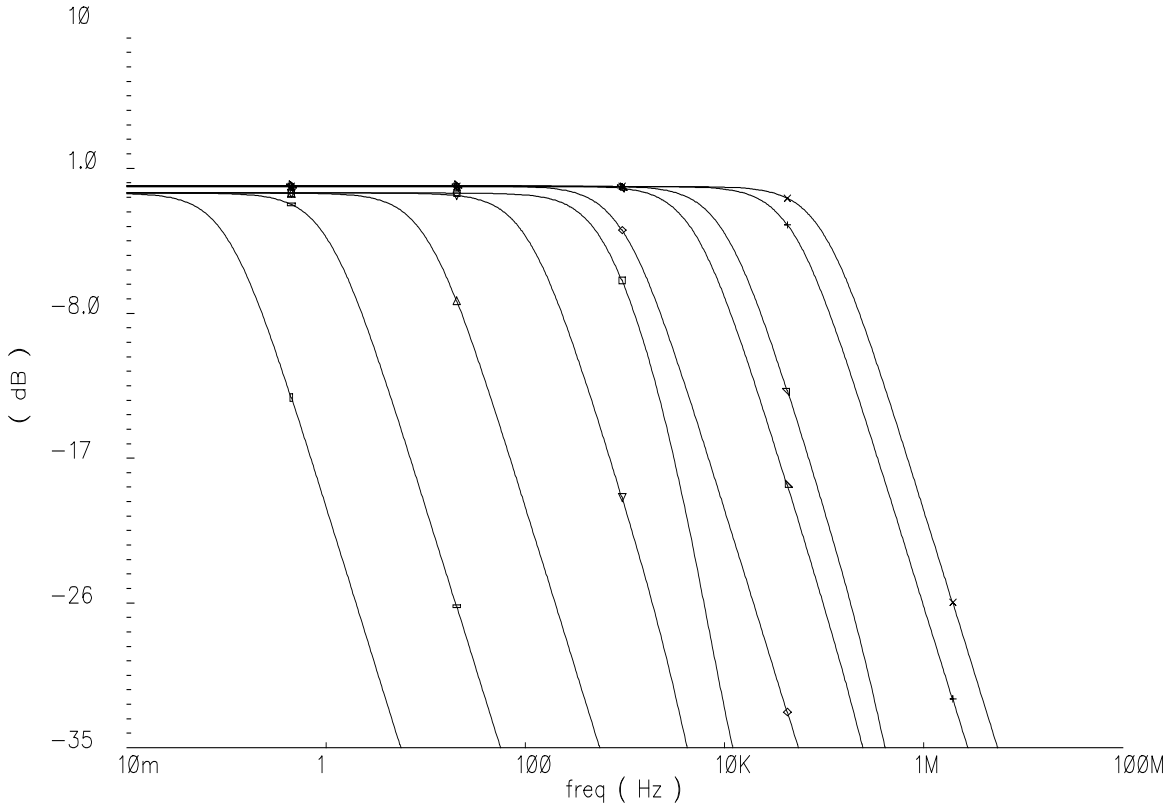

Fig. 38. Frequency response plot of the filter array at 200°C.

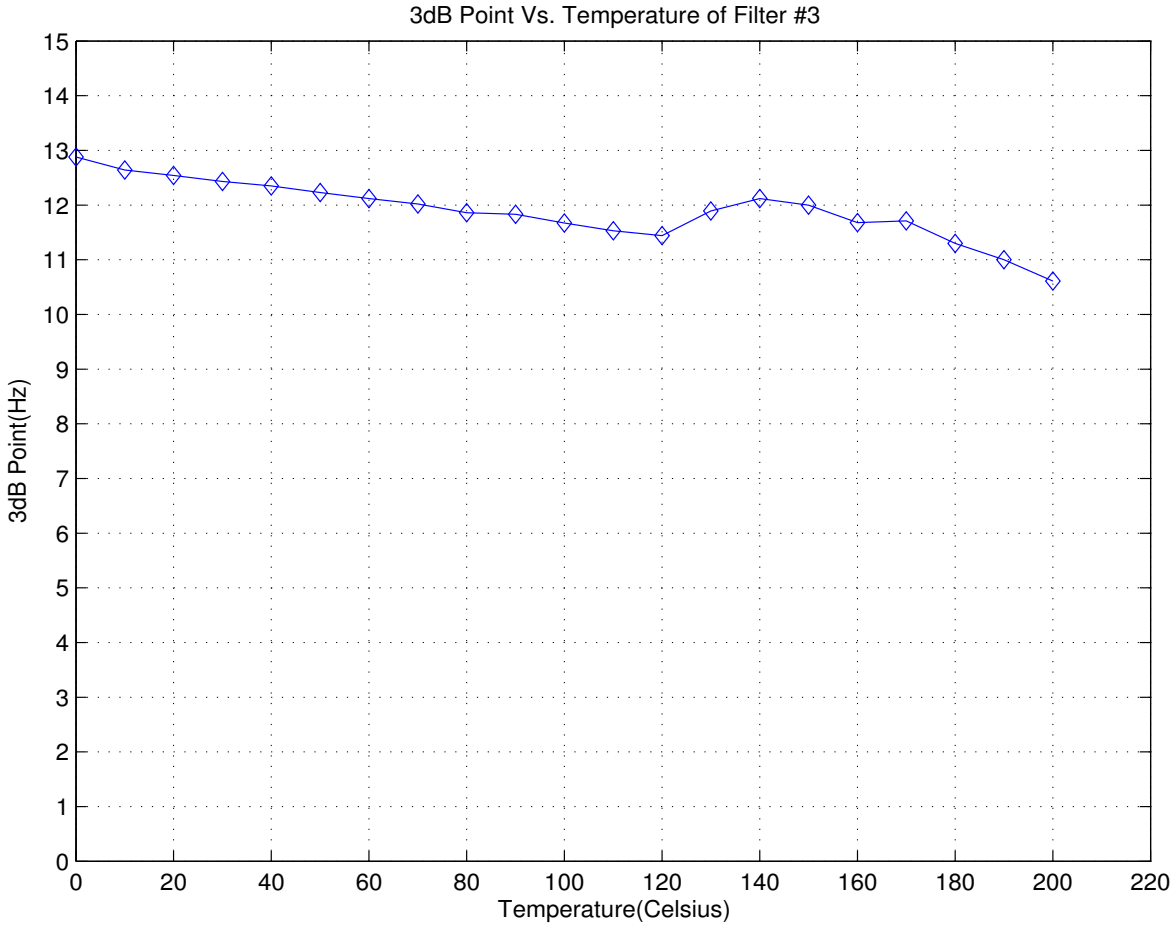

Fig. 39. 3dB point vs. temperature plot of filter #3.

Table 8. Cut-off frequencies A of the filter array at 200°C(simulation results).

	F#1	**F#2**	**F#3**	**F#4**	**F#5**
GAIN(dB)	**2.035**	**2.074**	**2.074**	**2.074**	**2.074**
3dB	**0.11Hz**	**1.07Hz**	**10.72Hz**	**103Hz**	**600Hz**
CMRR(dB)	**40.91**	**40.95**	**40.95**	**40.95**	**40.95**
Output noise level	**4uV**	**12uV**	**39uV**	**124uV**	**299uV**
HD(dB) 50mVpp	**-38.48**	**-38.28**	**-49.1**	**-62.9**	**-59.4**
SNR with 50mVpp	**83.8dB**	**74.6dB**	**64.2dB**	**54.2dB**	**46.5dB**
Dynamic Range (SNDR) with 50mVpp	**40.4dB**	**40.2dB**	**49.3dB**	**52.0dB**	**45.1dB**
Input Signal Amplitude=50mVpp and Frequency is $\frac{1}{2} f_{3dB}$ at 200 Celsius. F#X = Filter #X					

Table 9. Cut-off frequencies B of the filter array at 200°C(simulation results).

	F#6	F#7	F#8	F#9	F#10
GAIN(dB)	**2.451**	**2.451**	**2.451**	**3.711**	**3.711**
3dB	**1Khz**	**5.1Khz**	**10.1Khz**	**51Khz**	**102Khz**
CMRR(dB)	**42.34**	**42.34**	**42.34**	**35.141**	**35.141**
Output noise level	**255uV**	**567uV**	**706uV**	**386uV**	**436uV**
HD(dB) 50mVpp	**-59.2**	**-59.0**	**-59.0**	**-49.4**	**-49.4**
SNR with 50mVpp	**48.3dB**	**41.3dB**	**39.4dB**	**45.9dB**	**44.9dB**
Dynamic Range (SNDR) with 50mVpp	**46.6dB**	**40.5dB**	**38.1dB**	**42.8dB**	**42.4dB**
Input Signal Amplitude=50mVpp and Frequency is $\frac{1}{2}f_{3dB}$ at 200 Celsius. F#X = Filter #X					

4. CHIP PHOTOGRAPHIES AND TEST RESULTS

4.1 Chip Photographies

4.1.1 Nanowell Sensor IC

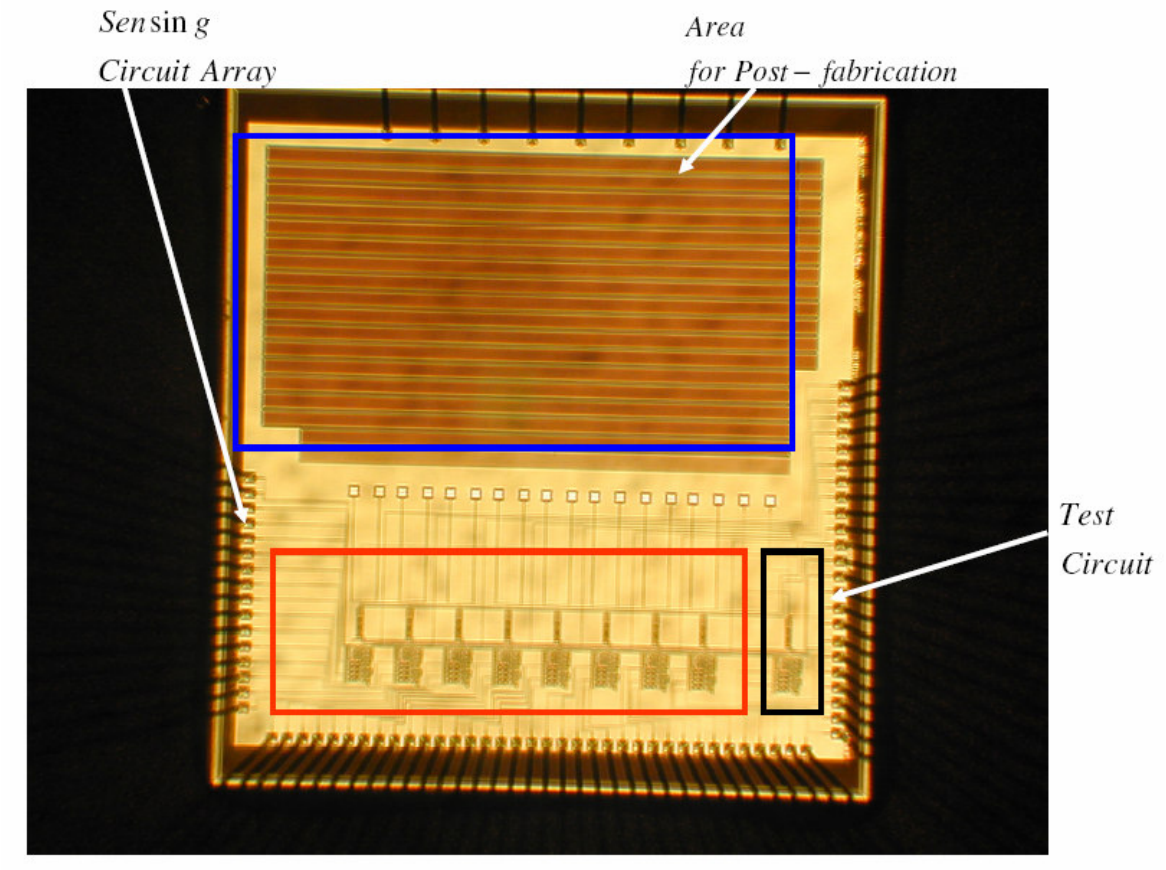

Fig. 40. Nanowell sensor IC photograph.

Fig.40 is the whole top-view photo of Nanowell sensor IC. The size of the chip is 1.6mm by 1.6mm and it was fabricated with TSMC 0.18um CMOS technology and

packaged with PGA145M package. It has 8 channels which integrate one readout circuit and one low power current-mode ADC converter. Also, for future testing, it also has one additional channel for characterization. The wide empty area is reserved for the post-fabrication process of placing a nanowell capacitor.

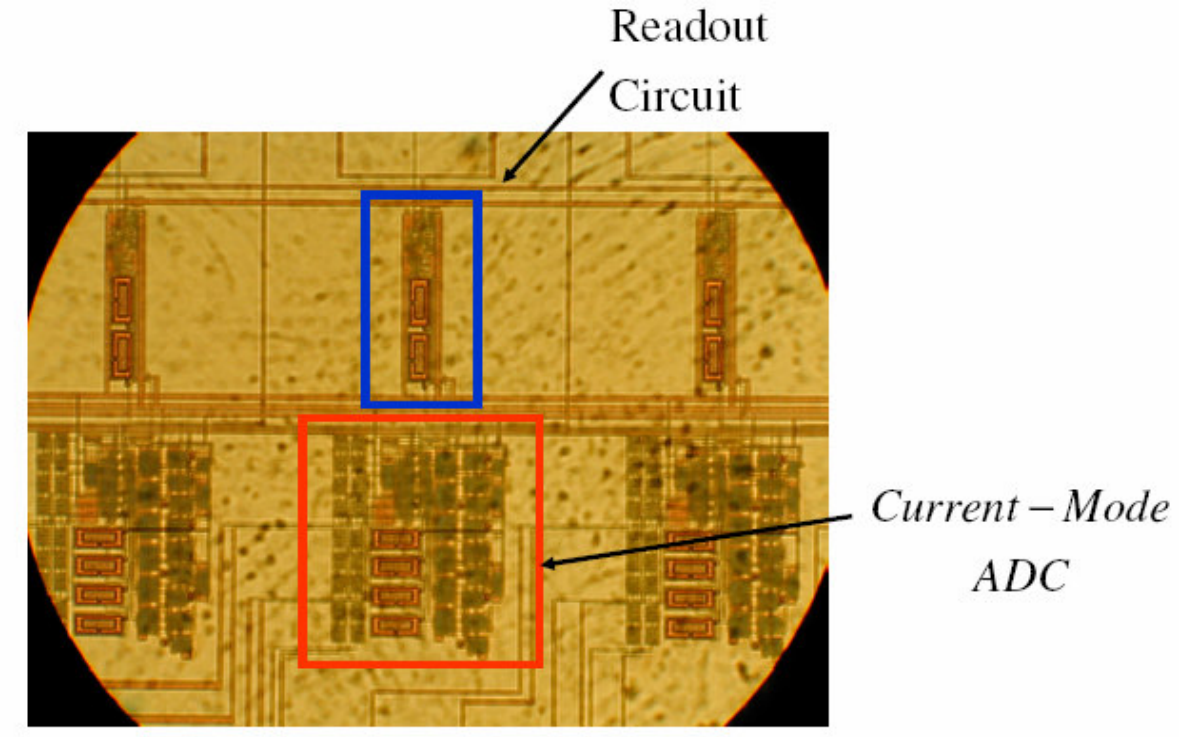

Fig. 41. Zoomed photo of one front-end channel.

Fig. 41 shows the zoomed photography of one front-end channel including one capacitance readout circuit and low-power current-mode ADC [39].

4.1.2 Van der Waals Sensor IC

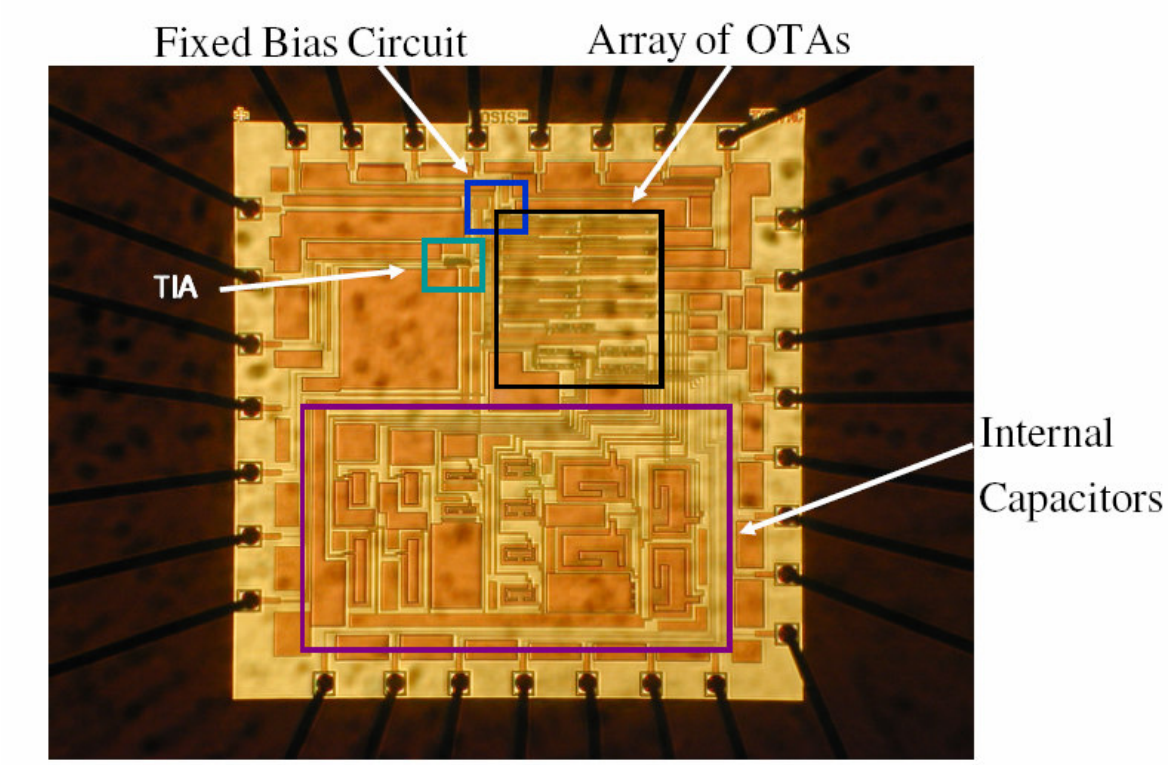

Fig. 42. Van der Waals sensor IC full photograph.

Fig. 42 shows the top-view photography of the Van der Waals Sensor IC. It was also fabricated with TSMC 0.18um CMOS technology and packaged with LCC44 package. The size of the chip itself is 1.6mm by 1.6mm. As explained before, the IC includes one transimpedance amplifier and one filter array consisting of 10 different lowpass filters with the distinctive cut-off frequencies. Also, the internal capacitors used with the transconductance amplifiers to form filters are integrated together. However, in cases of Filter #1, #2 and #3, external capacitors are used on the printed circuit board due to their large size.

4.2 Test Results

4.2.1 Nanowell Sensor IC

4.2.1.1 Test Set-up

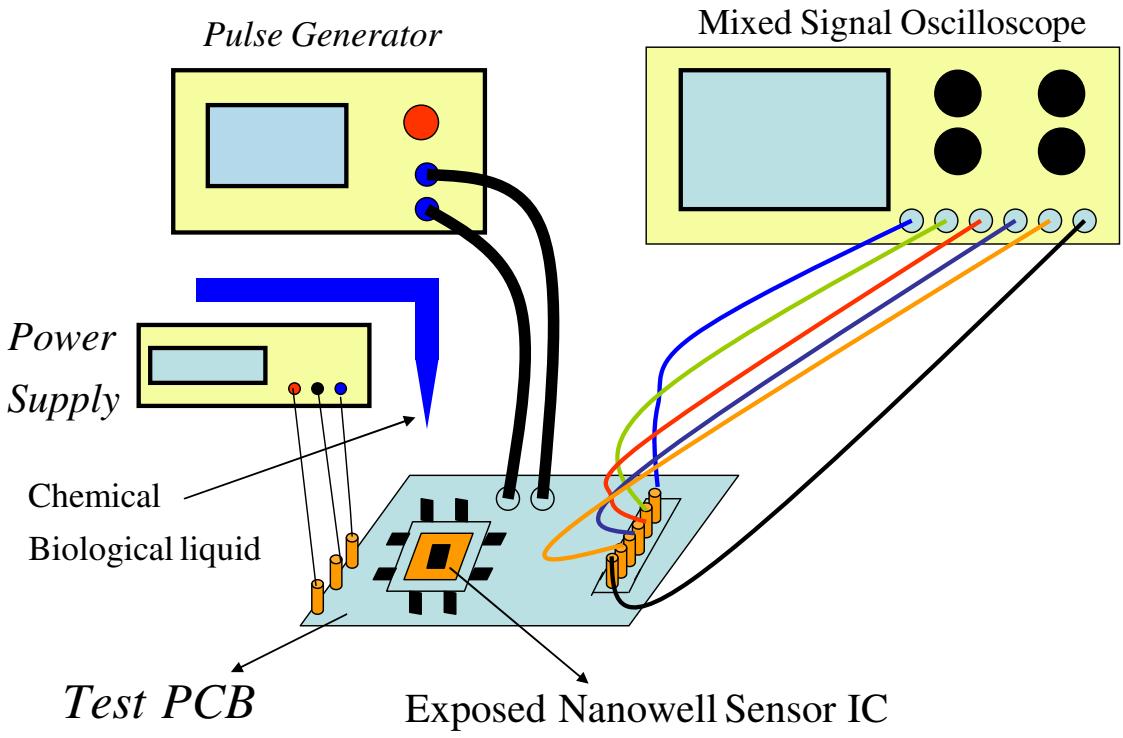

Fig. 43. Nanowell sensor IC test set-up.

Fig. 43 shows the whole test set-up for Nanowell Sensor IC. First of all, the PCB where the chip is placed is designed. Next, the mixed signal oscilloscope is connected to the output ports of the PCB. One function generator provides the circuit with the clock to the digital circuitry and the high frequency common mode signal to the readout circuit. Of course, one power supply is used to provide VDD, VSS and GND power connection. Finally, very precise liquid control equipment is required to drop a very small chemical or biological liquid on the exposed chip to change the dielectric constant of the tiny capacitors placed on the empty area of the chip. The addition of the microfluids will be implemented in the next generation device. Currently, our focus is to test the electronics coupled to the sensor array IC.

The PCB test board should be design to have the external calibration circuitry, output ports, input ports and power supply ports. The pin description summarized in Table 10 and 11 can be used to design a good test PCB. The addition of the microfluids will be implemented in the next generation device. Currently, our focus is to test the electronics coupled to the sensor array IC.

Table 10. Pin description A of Nanowell sensor IC.

PIN NO.	PIN NAME	PIN DESCP.
G1	VRF	MixerInput-125mV DC offset
F1	VIN	Amplifier Input
G3	IREF_EXT_150u	Reference Current 150uA
G2	VSS_WHOLE	VSS=-0.65
E1	VDD_WHOLE	VDD=0.65
F2	GND	`0
F3	IREF_EXT_ TEST_150uA	Reference Current 150uA for Testing
D1	VO_TEST	OUTPUT TESTING(DC)
E2	EXT	External Calibration for Testing Channel
D3,C2,B1,D2,E3, C1	O1,O2,O3,O4, O5,O6	TEST CHANNEL OUTPUT
C12,B13,A14,B12,C11,A13	O1_6, O2_6, O3_6, O4_6, O5_6, O6_6	CHANNEL#6 OUTPUT
B11,A12,C10,B10,A11,B9	O1_5, O2_5, O3_5, O4_5, O5_5, O6_5	CHANNEL#5 OUTPUT

Table 11. Pin description B of Nanowell sensor IC.

PIN NO.	PIN NAME	PIN DESCP.
C9,A10,A9,B8,A8,C8	O1_4,O2_4, O3_4, O4_4,O5_4,O6_4	CHANNEL#4 OUTPUT
C7,A7,A6,B7,B6,C6	O1_3,O2_3,O3_3,O4_3,O5_3, O6_3	CHANNEL#3 OUTPUT
A5,B5,A4,A3,B4,C5	O1_2,O2_2, O3_2, O4_2,O5_2,O6_2	CHANNEL#2 OUTPUT
B3,A2,C4,C3,B2,A1	O1_1,O2_1, O3_1, O4_1,O5_1,O6_1	CHANNEL#1 OUTPUT
F14,F13,E15,E14, D15,C15	O1_7,O2_7,O3_7,O4_7,O5_7, O6_7	CHANNEL#7 OUTPUT
H15,H13,G13,G15, F15,G14	O1_8,O2_8, O3_8, O4_8,O5_8,O6_8	CHANNEL#8 INPUT
J13	GND_DIG	DIGITAL GOUND
K15	VDD_DIG	DIGITAL VDD
J15	CLK	CLOCK+
H14	CLK_M	CLOCK-
H2,H1,H3,J3,J1,K1, J2,K2	EXT1,EXT2,EXT3EXT4,EXT5, EXT6, EXT7, EXT8	External Calibration of each channel

4.2.2 Van der Waals Sensor IC

4.2.2.1 Test Set-up

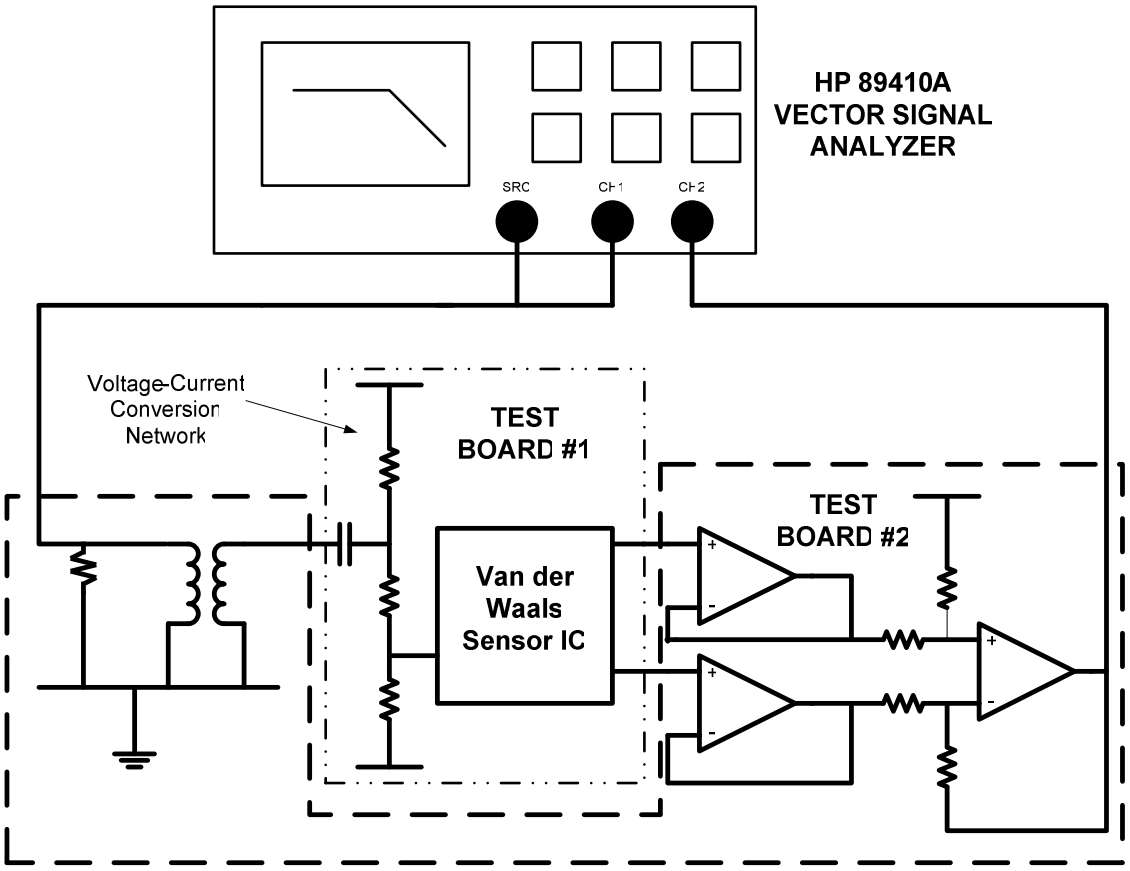

Fig. 44. Test set-up for Van der Waals sensor IC.

Before tested with the real sensor devices, the independent test without sensor devices should be conducted. The test focuses on measuring the basic specifications of the filters. It covers measuring frequency response, noise, harmonic distortion and dynamic range.

Fig. 44 demonstrates the test set-up for the Van der Waals Sensor IC. HP89410A Vector Signal Analyzer is one of the useful measurement equipments especially for the seriously low frequency circuits. The measurable frequency range of HP 89410A is from DC to 10Mhz. It means that 89410A includes the entire frequency range to be measured. To build up the whole test set-up, two PCBs are designed and manufactured. Van der Waals Sensor IC is placed on Test Board #1. The board is equipped with the power supply connection, Voltage-to-Current conversion resistor network, output ports. The buffer circuitry for differential-to-single-ended conversion operates on Test Board #2. Also, it has a transformer which isolates the source output of HP 89410A from the input of Test Board #1.

In the frequency response measurement, the source signal from 89410A passes through the whole test set-up including Van der Waals Sensor IC. Channel #2 accepts the output signal from the buffer circuitry. So, by comparing Channel #2 signal with Channel #1 source signal, HP 89410A can successfully reconstruct the frequency response. However, the frequency response achieved in this set-up is not what we want exactly. That's because this test set-up measures the frequency response from the transformer to the output of the buffer circuitry. Fortunately, because the transformer and the buffer circuitry do not influence the frequency response, the frequency response taken from 89410A is assumed to be the result from Voltage-Current Conversion network to the input of the buffer circuitry. Therefore, by compensating for the effect of the conversion network on the frequency response, we can successfully reconstruct the frequency response of Van der Waals Sensor IC.

Moreover, 89410A has the capability of changing the source signal amplitude and frequency very flexibly and displaying the output signal spectrum. Therefore, by measuring the harmonic distortion of the output spectrum, we can calculate Total Harmonic Distortion (THD). Additionally, 89410A can measure the noise power in the designated bandwidth. As a result, SNR and SNDR (Dynamic Range) can be easily calculated from the test results from 89410A.

Table 12. Pin description A of the Van der Waals sensor IC.

PIN NO.	PIN NAME	PIN DESC.
16	VDD	VDD=0.65
14	EXT_R2	270K OHM CONNECTION
13	EXT_R1	270K OHM CONNECTION
12	V1_P	FILTER #1
11	V1_N	FILTER #1
10	V2_P	FILTER #2
9	V2_N	FILTER #2
5	V3_P	FILTER #3
4	V3_N	FILTER #3
42	V4_P	FILTER #4
43	V4_N	FILTER #4
19	TEST1	TEST PIN #1 for TIA
20	TEST2	TEST PIN #2 for TIA
21	IN	INPUT PORT
38	V5_P	FILTER #5

With reference to the pin description of Van der Waals Sensor IC, Test Board #1 is designed. The pin description is tabulated in Table 12 and 13.

Table 13. Pin description B of the Van der Waals sensor IC.

PIN NO.	PIN NAME	PIN DESC.
3	V6_P	FILTER #6
2	V6_N	FILTER #6
36	V7_P	FILTER #7
35	V7_N	FILTER #7
1	V8_P	FILTER #8
44	V8_N	FILTER #8
32	V9_P	FILTER #9
31	V9_N	FILTER #9
34	V10_P	FILTER #10
33	V10_N	FILTER #10
22	IBIAS2	BIAS CURRENT
24	IBIAS1	BIAS CURRENT
25	GND	
26	VSS=-0.65	
37	V5_N	FILTER #5

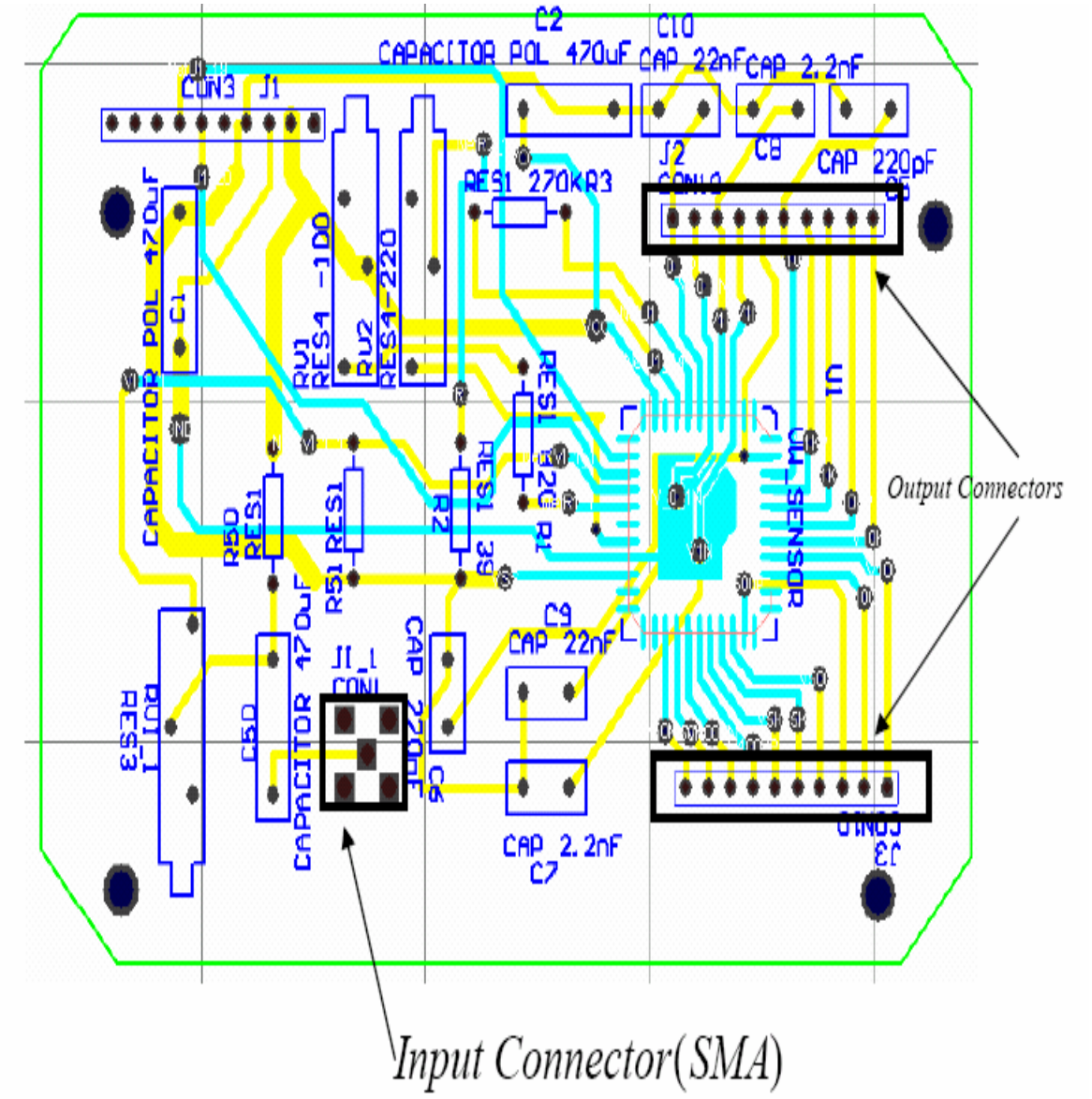

Fig. 45. Test board #1 layout.

Fig 45. and 46. show the PCB layout and photograph of Test Board #1. It has one SMA connector which receives the input signal from the transformer. Also, in front of the input pin of the chip, the conversion network consisting of resistors is attached. Also, it has a few resistors composing the biasing circuitry and capacitors such as external

capacitors of the filters and ample capacitors for better power supply quality. Finally, it has 20 output pins to be connected to Test Board #2 input pins.

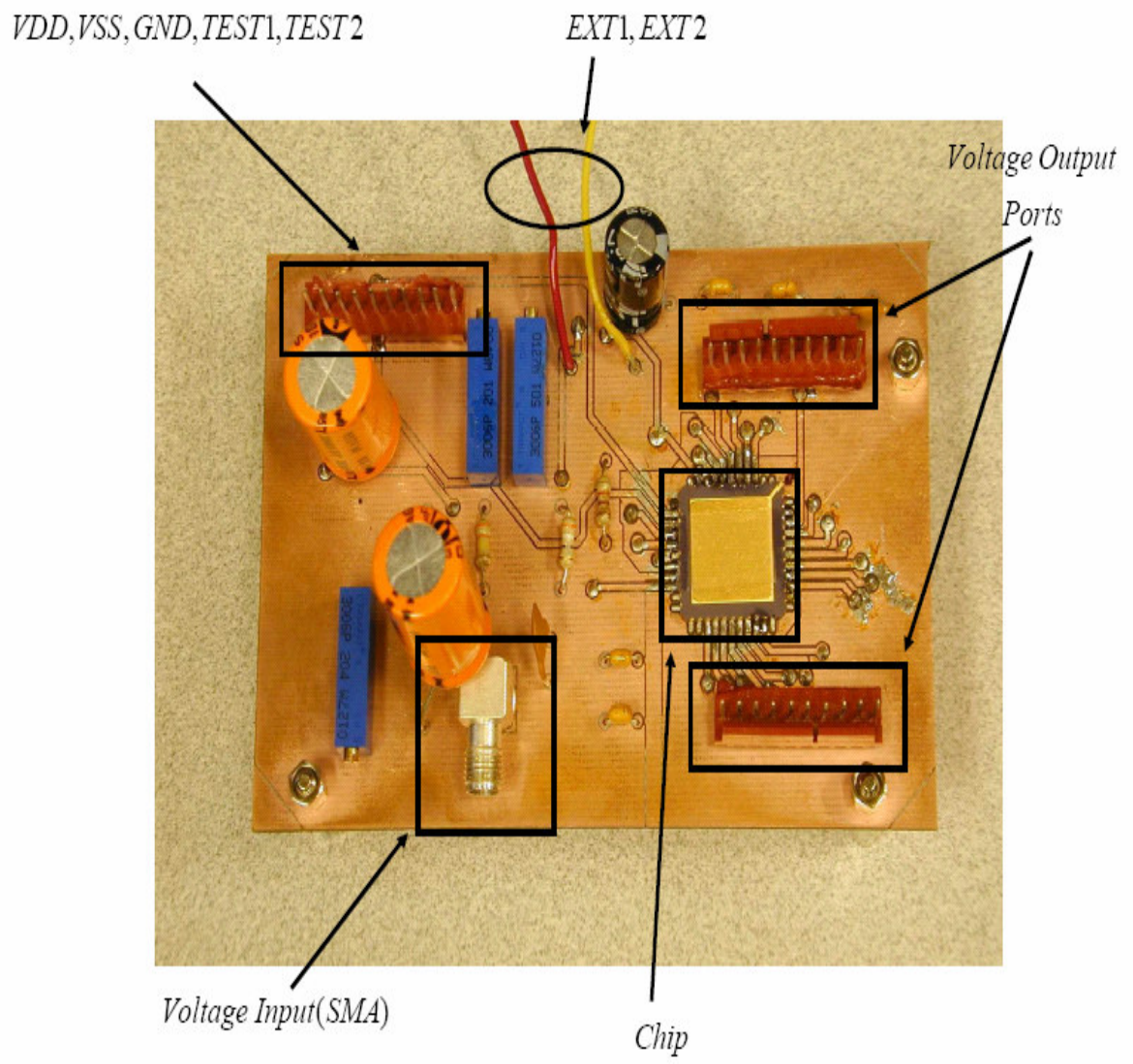

Fig. 46. Photograph of test board #1.

Fig 47. and 48. display the buffer circuitry. Simply, it is composed of a few resistors, two huge capacitors and two TL072 operational amplifier packages. Two

operational amplifiers are used to isolate the output ports of Van der Waals IC from the subtractor inputs as unity-gain buffers. The subtractor made with one operational amplifier and four resistors generates single-ended signals from the differential signals coming out from the unity-gain buffers. The output of the subtractor is connected to Channel #2 of HP 89410A.

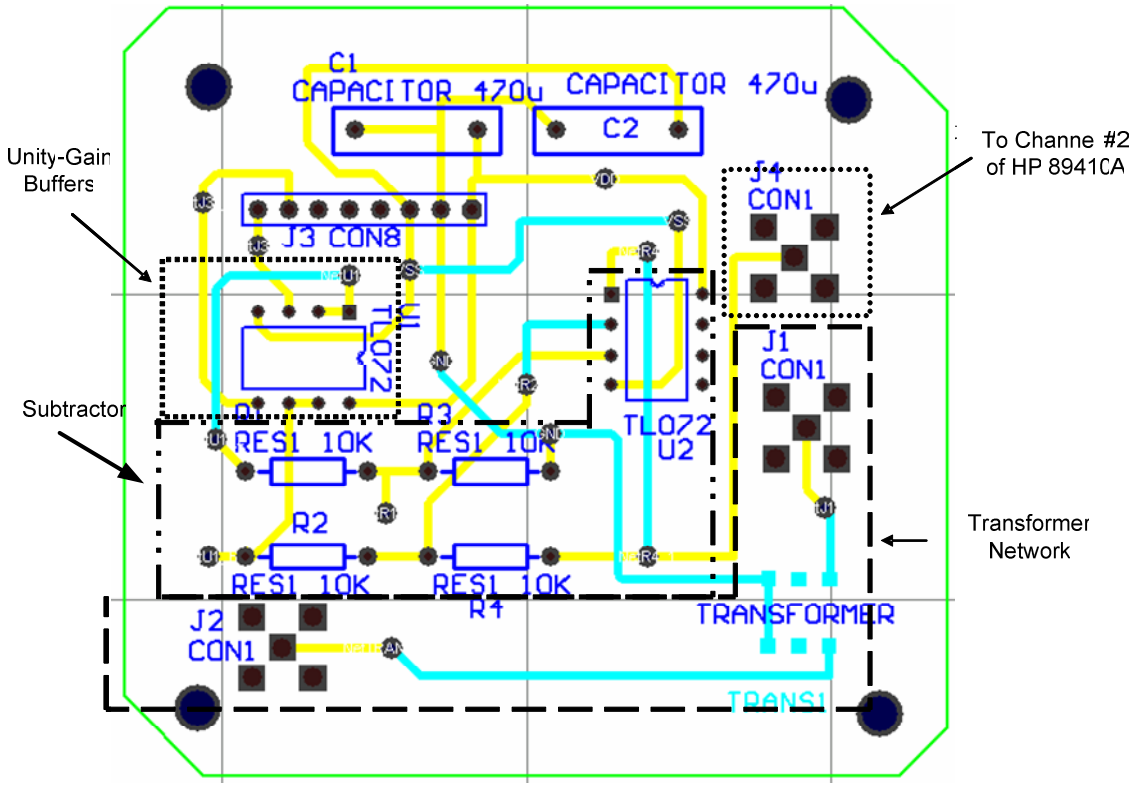

Fig. 47. Test board #2 layout.

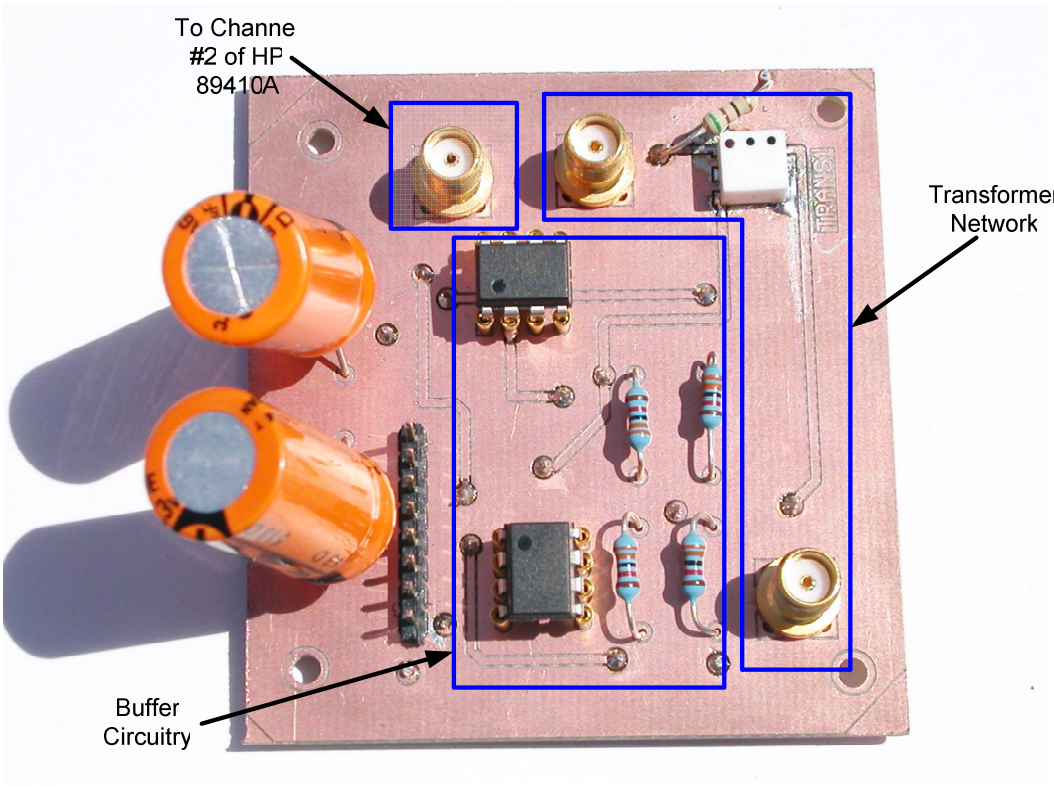

Fig. 48. Test board #2 photograph.

4.2.2.2 Test Results

HP 89410A can provide the test set-up with the transient signal such as sinusoidal signal. By watching the transient output signal with the oscilloscope, we can make sure that the chip works in transient response's point of view. Fig. 49 shows the output transient of one typical filter of the Van der Waals Sensor IC.

First of all, the fact that the frequency response taken from the set-up is not the exact frequency response from the input of Van der Waals Sensor IC to the buffer input should be stressed again. That's because the gain of the conversion network before Van der Waals Sensor IC influences the response. So, in order to recover the frequency

response we want precisely, the conversion gain of the network should be calculated from the simulation. Since the network is composed of passive components, the simulation result is assumed to be same to the real results. Fig. 50. shows the simulated conversion gain of the network. From the plot, we know that the actual gain of Van der Waals Sensor IC should be calculated by adding 91.28dB to the gain of the frequency response taken from the above set-up in Fig. 44.

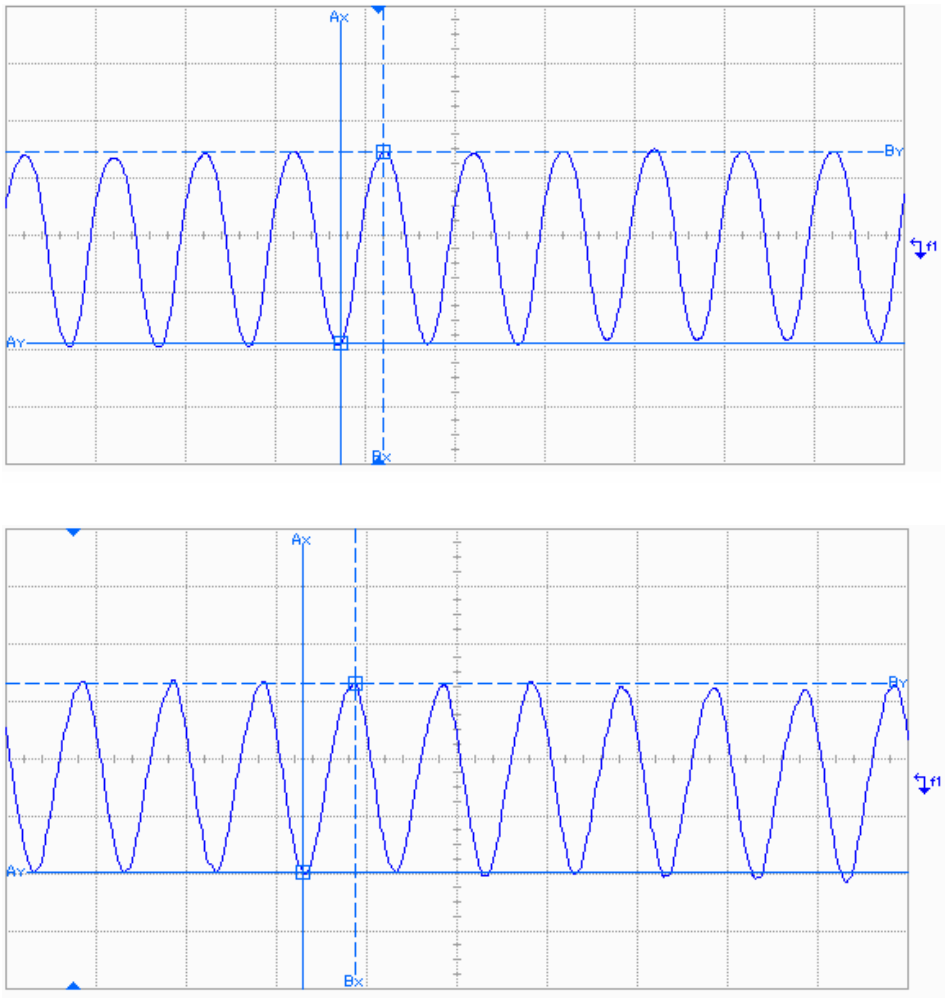

Fig. 49. The output transient response of filter #6 with 50mV amplitude (the upper is 1Khz signal and the lower is 5Khz signal).

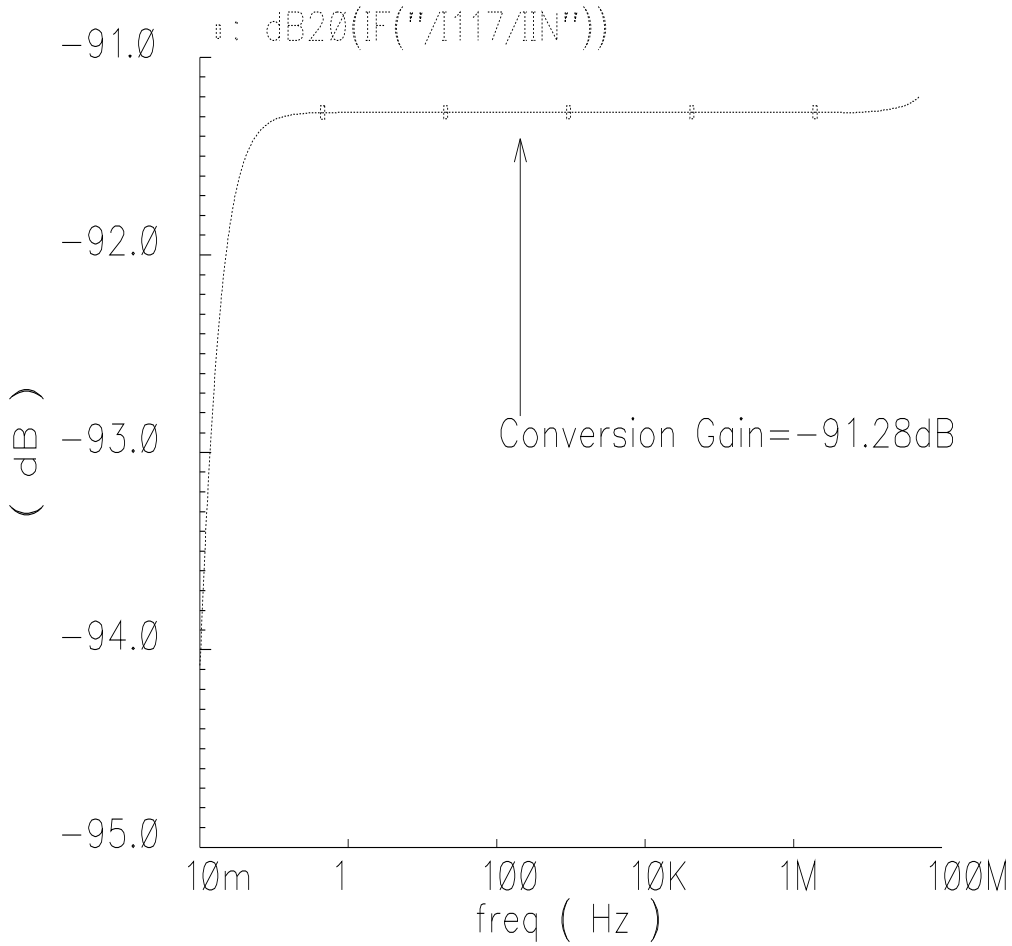

Fig. 50. The conversion gain plot taken from the simulation in Cadence.

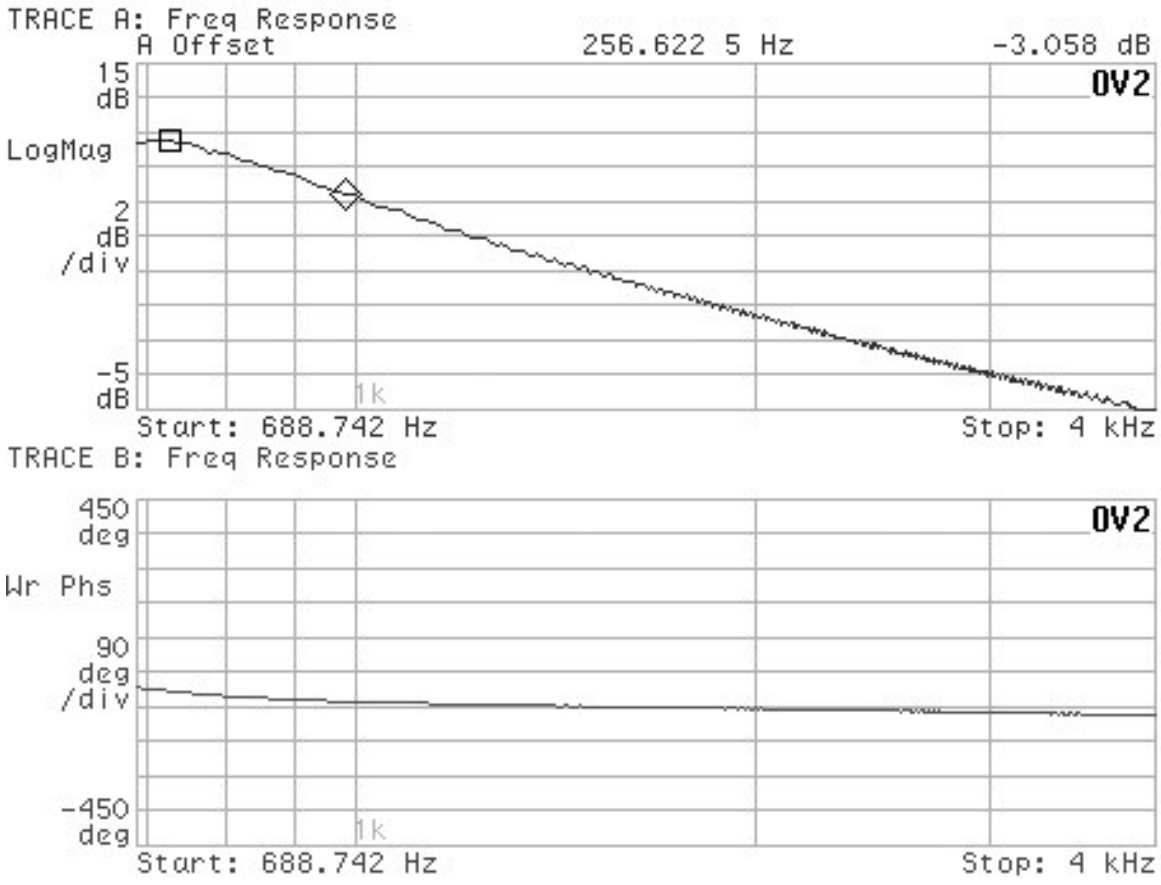

Fig. 51. The magnitude and phase response of the output of filter #5.

[X axis: frequency (Hz), Y axis: noise power density (dBm)]

Fig. 52. The noise spectrum of the output of filter #5.

[X axis: frequency (Hz), Y axis: signal amplitude (uVrms)]

Fig. 53. The signal spectrum of the output of filter #5
with 50mVpp and 470Hz sinusoidal input.

Table 14. Filter performance parameters A including TIA of each filter output.

	F#1	F#2	F#3	F#4	F#5
GAIN (dB) (WHOLE)	**-3.88**	**7.415**	**16**	**0.07**	**10.6**
GAIN (dB) (TIA + Filter)	**87.4**	**98.7**	**107**	**91.3**	**101.9**
3dB	**0.7Hz**	**70Hz**	**103Hz**	**110Hz**	**945Hz**
Output noise level(uV)	**<30**	**<17**	**<21**	**<24**	**<23**
Equivalent Input Current Noise Level(nA)	**<1.28**	**<0.2**	**<0.1**	**<0.7**	**<0.2**
Vpp(mV) (Conversion Network Input)	**100**	**17.4**	**100**	**96**	**50**
Ipp(uA) (Van der Waals IC Input)	**2.7**	**0.5**	**2.7**	**2.6**	**1.4**
THD(dB)	**25%**	**5%**	**5%**	**5%**	**5%**
SNR(dB)	**>60.6**	**>61.6**	**>83.5**	**>66.1**	**>71.3**
Dynamic Range (SNDR)	**12dB**	**25.9dB**	**26dB**	**26dB**	**26dB**
Total Power Consumption (TIA+All Filters)	**1.1mW**				

Table 15. Filter performance parameters B including TIA of each filter output.

	F#6	F#7	F#9	F#10
GAIN (dB) (WHOLE)	**1.89**	**-1.78**	**-3.97**	**-1.63**
GAIN (dB) (TIA + Filter)	**93.2**	**89.5**	**87.3**	**89.7**
3dB	**2360Hz**	**5.5Khz**	**22Khz**	**24Khz**
Output noise level(uV)	**<14**	**<40**	**<163**	**<155**
Equivalent Input Current Noise Level(nA)	**<0.3**	**<1.4**	**<7**	**<5.1**
Vpp(mV) (Conversion Network Input)	**20**	**16**	**8**	**8**
Ipp(uA) (Van der Waals IC Input)	**0.5**	**0.4**	**0.2**	**0.2**
THD(dB)	**5%**	**5%**	**5%**	**5%**
SNR(dB)	**>58.9**	**>44.2**	**>23.8**	**>29.9**
Dynamic Range (SNDR)	**29.3dB**	**25dB**	**18.9dB**	**20.2dB**
Total Power Consumption (TIA+All Filters)	**1.1mW**			

Fig. 51, 52 and 53 show the frequency response, the noise spectrum density and the output spectrum of one typical filter in Van der Waals IC, respectively. The plots include almost all the information needed to calculate the general filter specifications. For each filter output signal, the measurement has been conducted. From the data, the filter specifications have been achieved. The general filter specifications are tabulated in Table 14 and 15.

4.3 Summary

Nanowell Sensor IC and Van der Waals Sensor IC were fabricated with TSMC 0.18um technology. For Nanowell IC, the unavailability of the post-fabrication process prevented the real test from taking places even with the figured-out test set-up. It will be a part of the future work. For Van der Waals Sensor IC, the independent test without the real sensor device has been conducted. The results show the performance parameters of the signal processing system composed of one transimpedance amplifier and the lowpass filters with distinct cut-off frequencies. The measured performance parameters include the gain, 3dB points, noise levels, THD, SNR, Dynamic Range and total power consumption. Currently the experiment was performed at the room temperature. However in the future, we would like to perform high temperature operation to test the feasibility in real life implementations.

The high temperature operation test and the whole system test with a real sensor device will be a part of the future work.

5. CONCLUSION

A wireless sensor network is one of the greatest achievements in the history of wireless network architecture. All the sensor nodes are widely distributed in the network. Each node watches the local environment, locally collecting, processing and storing the data for sharing with other nodes via wireless link. The network extracts the meaningful information to the end user from the data collected from the participating nodes. The Nanowell Sensor device [3] and Van der Waals Sensor [11] or the traditional Taguchi type sensor [45] might be the potential candidates of the novel sensor devices used in the widely distributed sensor network.

To implement the whole system which uses the Nanowell Sensor device for chemical or biological material sensing, a low power and small size capacitance value sensing readout circuit is required. Mainly based on the "Lock-in" technique, t he readout circuit has been designed and fabricated with TSMC 0.18um CMOS technology. Also, it has been integrated together with the back-end low power current-mode ADC on the same chip. In the simulation result, the readout circuit demonstrates its high resolution conversion ratio of 165pA/aF and low power consumption characteristic of 30uW per channel. The chip will be tested as soon as possible after the post-fabrication process is available.

To realize the multiple sensing systems with one type sensor device, the "fluctuation noise" sensing technique proposed by Dr. Kish [9] is used in this research. The fluctuation noise spectrum is used as a "defining" factor to distinguish one agent from another. Therefore, the front-end system amplifying the fluctuation noise signal of the sensor and capturing the signal in the required frequency range with different cut-off frequencies, while maintaining stable operation in the wide range of temperature variation until 200 Celsius is demanded. It was fabricated with TSMC 0.18um technology and tested. The gain of the front-end circuit is at least 87dB and its power consumption with one transimpedance amplifier and 10 filters is just 1.1mW. Moreover, the worst-case maximum input current signal is 0.2uApp while satisfying 5% THD and

the equivalent input current noise level is under 7nA. It clarifies that the front-end circuit demonstrates the considerably high dynamic range with the noise level input signal amplitude. The back-end digital signal processing unit accepts the output signals of the front-end system and extracts considerably meaningful information. . The high temperature operation test and the whole system operation test with the real sensor device will be part of the future work.

REFERENCES

[1] M. Ulema, “Wireless sensor networks: architectures, protocols, and management,” in *Network Operations and Management Symposium*, 2004, vol.1, pp. 931.

[2] C.C. Enz, A. El-Hoiydi, J.-D. Decotignie, V. Peiris, “WiseNET: an ultralow-power wireless sensor network solution,” *Computer* vol. 37, no. 8, pp.62-70, Aug. 2004.

[3] S.R. Sonkusale, M.Cheng, L.Kish, A. Agarwal, Y.Kim, C. Liu, S. Seo, "A CMOS sensor array IC of Nanowell devices for molecular sensing", presented at *the 3rd annual IEEE Conference on Sensors*, Vienna, Austria, Oct. 24-27, 2004.

[4] S. Hashioka, H. Matsumura, “10 nm size fabrication of semiconductor substrate and metal thin lines by conventional photolithography”, *Intl. Micro. and Nano. Conf.*, July, 2000, pp. 184-185.

[5] F. Kremer, A.Schönhals, *Broadband Dielectric Spectroscopy*, Berlin; Springer, 2003.

[6] P.Q. Mantas, “Dielectric response of materials: extension to the Debye model”, J. *the European Ceramic Society*, vol.19, pp. 2079-2086,Oct. 1999.

[7] S.R Sonkusale, L.Kish, M.Cheng, W. Marlow, Y.Kim, A. Agarwal, "A CMOS sensor array IC of Van der Waals enhanced MOSFET and Taguchi type sensors", presented at *the 3rd annual IEEE Conference on Sensors*, Vienna, Austria, Oct. 24-27, 2004.

[8] M. Cheng, W.H. Marlow, L.B. M. Joseowics, J. Janata, “Suspended gate field effect transistor modified with polypyrole as alcohol sensor,” *Anal Chem*, vol. 58, pp. 514-517, Mar.1986.

[9] L.B. Kish, R. Vajtai, C. Granqvist, “Extracting information from the noise spectra of chemical sensors: electronic nose and tongue by one sensor,” *Sensors and Actuators B,* vol. 71, p.55-59, Nov. 2000.

[10] T. Seiyama, A. Kato, K. Fujishi, M. Nagatani, “A new detector for gaseous components using semiconductor thin films”, *Anal Chem*, vol.34, pp. 1502, Oct.1962.

[11] M. Cheng, W.H. Marlow and L.B. Kish, "Van der Waals Force Enhanced MOSFET for Molecular and Particulate Sensing", Patent Disclosure(applied), TAMU, April 20, 2004.

[12] D.M. Wilson, "Analog VLSI architectures for chemical sensing microsystems," Ph.D Dissertation, Dept. EE, Georgia Institute of Technology, Atlanta, 1995.

[13] P. Bergveld, “Development of an ion-sensitive solid-state device for neurophysiological measurements,” *IEEE Trans Biomedical Eng*, vol. 17, pp. 70-71, Jan. 1970.

[14] K.I. Lundstrom, M.S. Shivaraman, C.M. Svenson, “A hydrogen-sensitive Pd gate MOS transistor,” *Journal App Physics*, vol. 46, no. 9, pp. 3876-3881, Sept. 1975.

[15] M. Stenberg, B. Dahlenback, “Surface-accessible FET for gas sensing,” *Sensors and Actuators*, vol. 4, pp. 273-281, May 1983.

[16] M. Joseowics, J. Janata, “Suspended gate field effect transistor modified with polypyrrole as alcohol sensor,” *Anal Chem*, vol. 58, pp. 514-517, May 1986.

[17] M. Cheng, Dept. of EE, Texas A&M University, College Station, “Personal Communication”, Jan. 2004.

[18] P. Bergveld, “Thirty years of ISFETOLOGY, what happened in the past 30 years and what may happen in the next 30 years”, *Sensors and Actuators B*, vol.88, no.1, pp. 1-20, Jan. 2003.

[19] H. Baltes, O. Brand, “Process in CMOS integrated measurement systems,” in *Proc. of the 16th Instrumentation and Measurement Technology Conference*, Venice, Italy , vol. 1, May 1999, p.54-59.

[20] I. Eisele, T. Doll, M. Burgmair, “Low power gas detection with FET sensors,” *Sensors and Actuators B*, vol.78, pp.19-25, Aug.,2001.

[21] G. Schmera, L. B. Kish, “Fluctuation-enhanced gas sensing by surface acoustic wave devices,” *Fluctuation and Noise Letters*, vol.2, pp. 117-123, Jun.,2002.

[22] H. Lu, L. Xun, X. S. Xie, "Single-molecule enzymatic dynamics", *Science*, vol.282, pp.1877-1882, Dec. 1998.

[23] C. Joachim, J. Gimzewski, A. Aviram, "Electronics using hybrid-molecular and mono-molecular devices," *Nature*, vol.408, pp.541-548, Nov. 2000.

[24] G. Schmera, L.B. Kish, "Combinatorial molecule counting by fluctuation-enhanced SAW and MOSFET sensors," in *Proc. SPIE Conference on Smart Electronics, MEMS, BioMEMS, and Nanotechnology*, San Diego, CA, March 3-6, 2003, pp. 120-124.

[25] G. Schmera, L.B. Kish, "Fluctuation Enhanced Chemical Sensing by Surface Acoustic Wave Devices," Patent disclosure under US Navy disclosure, NC 84126, May 2002.

[26] L.B. Kish, C.G. Granqvist, R. Vajtai, "Sampling-and-Hold Chemical Sensing by Noise Measurements for Electronic Nose Applications," Swedish patent Ser. No.: 990409-5. April 1999.

[27] L.B. Kiss, C.G. Granqvist, J. Söderlund, "Detection of chemicals based on resistance fluctuation-spectroscopy," Swedish patent, Ser. No. 9803019-0; Publ. No. 513148, Mar. 1998.

[28] P. Bruschi, A. Nannini, B. Neri, "Vapour and gas sensing by noise measurements on polymeric balanced bridge microstructures," *Sensors & Actuators B* ,vol.25, pp. 429-432, April 1995.

[29] P. Bruschi, F. Cacialli, A. Nannini, B. Neri, "Gas and vapour effects on the resistance fluctuation spectra of conducting polymer thin-film resistors," *Sensors & Actuators B*, vol.19, pp.421-425, April 1994.

[30] K.K. Hung, P.K. Ko, C. Hu, Y.C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol.37,pp. 654-665, Mar. 1990.

[31] Bramani, M., "A high sensitivity measuring technique for capacitive sensor transducer," *IEEE Trans. on Industrial Electronics*, vol.37, no.6. pp. 584-586, Dec. 1990.

[32] F.N. Toth, G.C.M. Meijer, H.M.M. Kerkvliet, "A very accurate system for multielectrode capacitive sensors," *IEEE Trans. on Instrumentation and Measurement*, vol.45, no.2, pp. 531-535, April 1996.

[33] F.M.L.V. Goes, G.C.M. Meijer, "A novel low-cost capacitive sensor interface," *IEEE Trans. on Instrumentation and Measurement*, vol.45, no.2, pp.536-540, April 1996.

[34] K. Mochizuki, T. Masuda, K. Watanabe, "An interface circuit for high-accuracy signal processing of differential capacitance transducer," presented at *the IEEE Instrumentation and Measurement Technology Conference*, Brussels, Belgium, June 4-6, 1996, pp. 1200-1204.

[35] J.T. Kung, R.N. Mills, H.S. Lee, "Digital cancellation of noise and offset for capacitive sensors," *IEEE Trans. on Instrumentation and Measurement*, vol. 42, no.5, pp. 939-942, Oct. 1993.

[36] S. Ranganathan, M. Inerfield, S. Roy, and S.L Garverick, "Sub-Femtofarad capacitive sensing for microfabricated transducers using correlated double sampling and delta modulation," *IEEE Trans. Circuits Sys. –II*, vol. 47, no.11, pp. 1170-76, Nov. 2000.

[37] C. Hagleitner, D. Lange, A. Hierlemann, O. Brand , H. Baltes, "CMOS single-chip gas detection system comprising capacitive, calorimetric and mass-sensitive microsensors," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, Dec. 2002.

[38] M. Tavakoli, R. Sarpeshkar, "An offset-canceling low-noise lock-in architecture for capacitive sensing," *J. Solid-State Circuits*, vol.38, no.2, pp. 244-253, Feb. 2003.

[39] A. Agarwal, Y. B Kim, S. Sonkusale, "Low power current mode ADC for CMOS sensor IC," presented at *ISCAS 2005 Conference*, Kobe, Japan, May 23-26, 2005.

[40] D.G. Nairn, C.A.T. Salama, "Current-mode algorithmic analog-to digital converters," *IEEE. J. Solid-State Circuits*, vol. 25, no. 4, pp. 997-1004, Aug. 1990.

[41] A. Veeravalli, E. Sanchez-Sinencio, J. Silva-Martinez, "Transconductance amplifiers with very small transconductance: a comparative design approach," *IEEE Journal of Solid-State Circuits*, vol. 37 ,no. 6, pp. 770-775, June 2002.

[42] S. Pavan, Y.P. Tsividis, K. Nagaraj, "Widely programmable high-frequency continuous-time filters in digital CMOS technology," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 4, pp. 503-511, April 2000.

[43] R. Zele, D. Allstot, "Low power CMOS continuous-time filters," *IEEE Journal of Solid State Circuits*, vol. 31, no. 2, pp. 157-168, Feb. 1996.

[44] F. S. Shoucair, "Design considerations in high temperature analog CMOS integrated circuits," *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol. CHMT-9, no.3, pp.242-251, Sep. 1986.

[45] N. Taguchi, "Sensor device and method of manufacturing same", U.S. Patent 3,695,848, Oct. 1972.

APPENDIX

In this section, all the plots taken from the test are included.

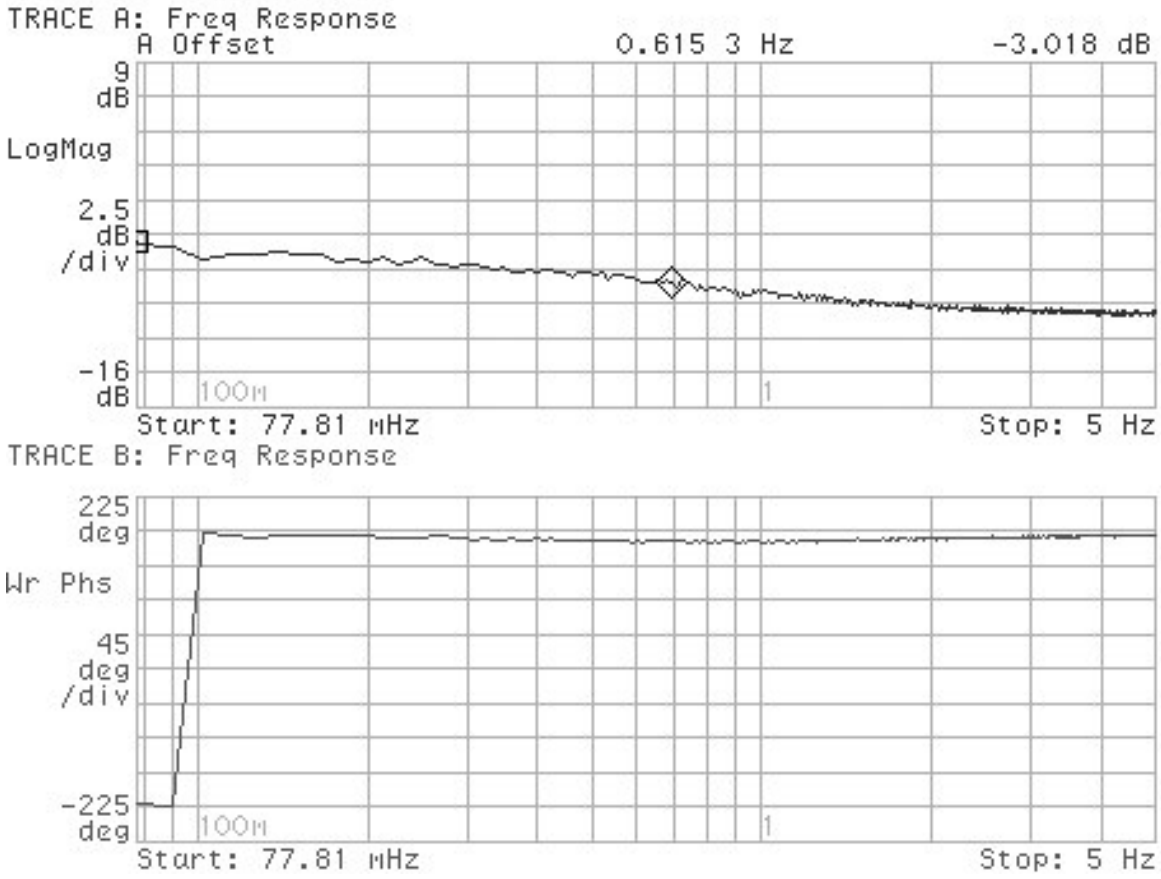

Fig. 54. The magnitude and phase response from filter #1.

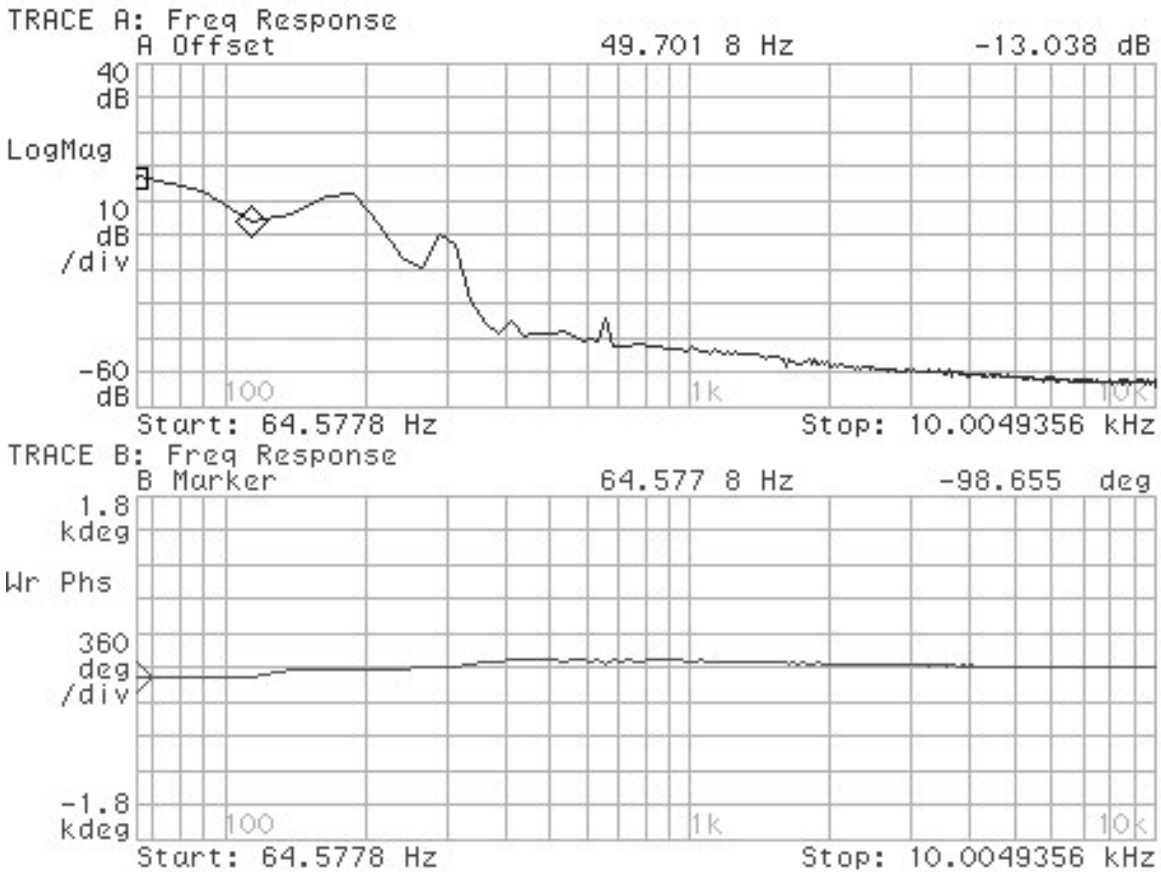

Fig. 55. The magnitude and phase response from filter #2.

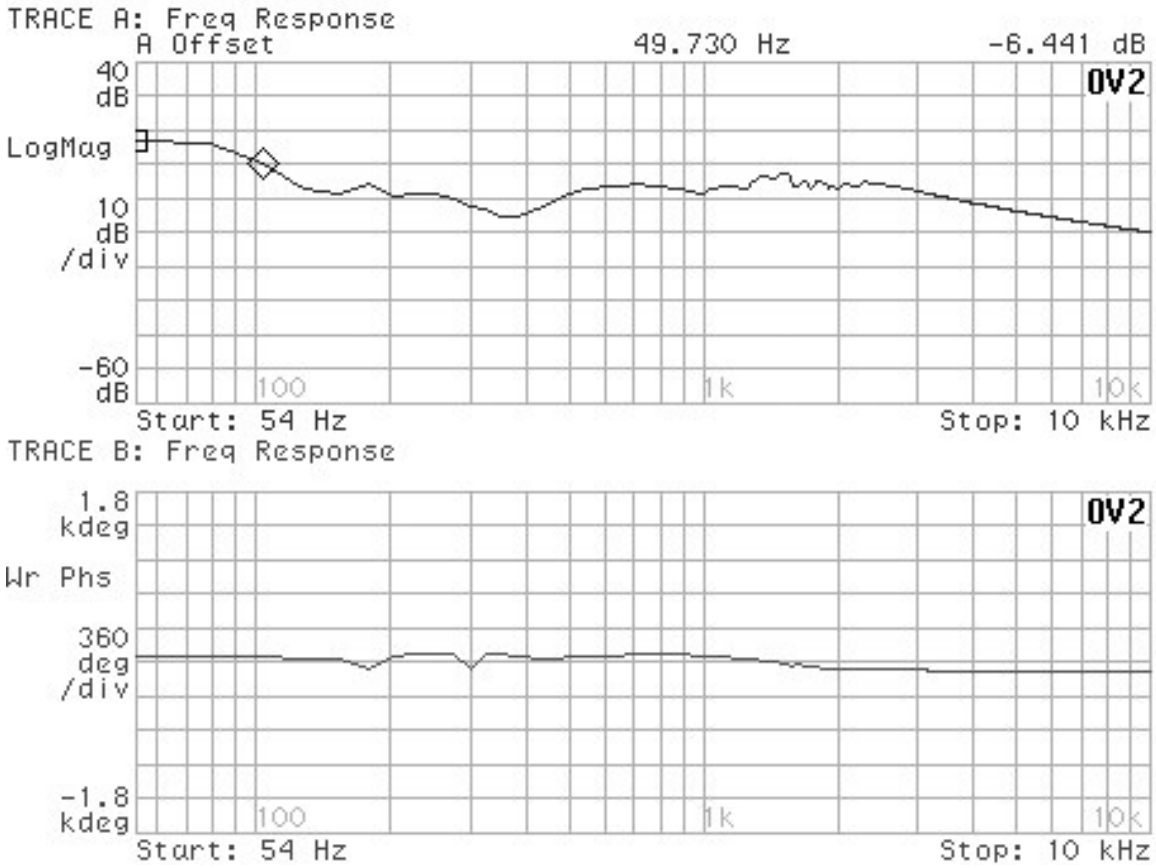

Fig. 56. The magnitude and phase response from filter #3.

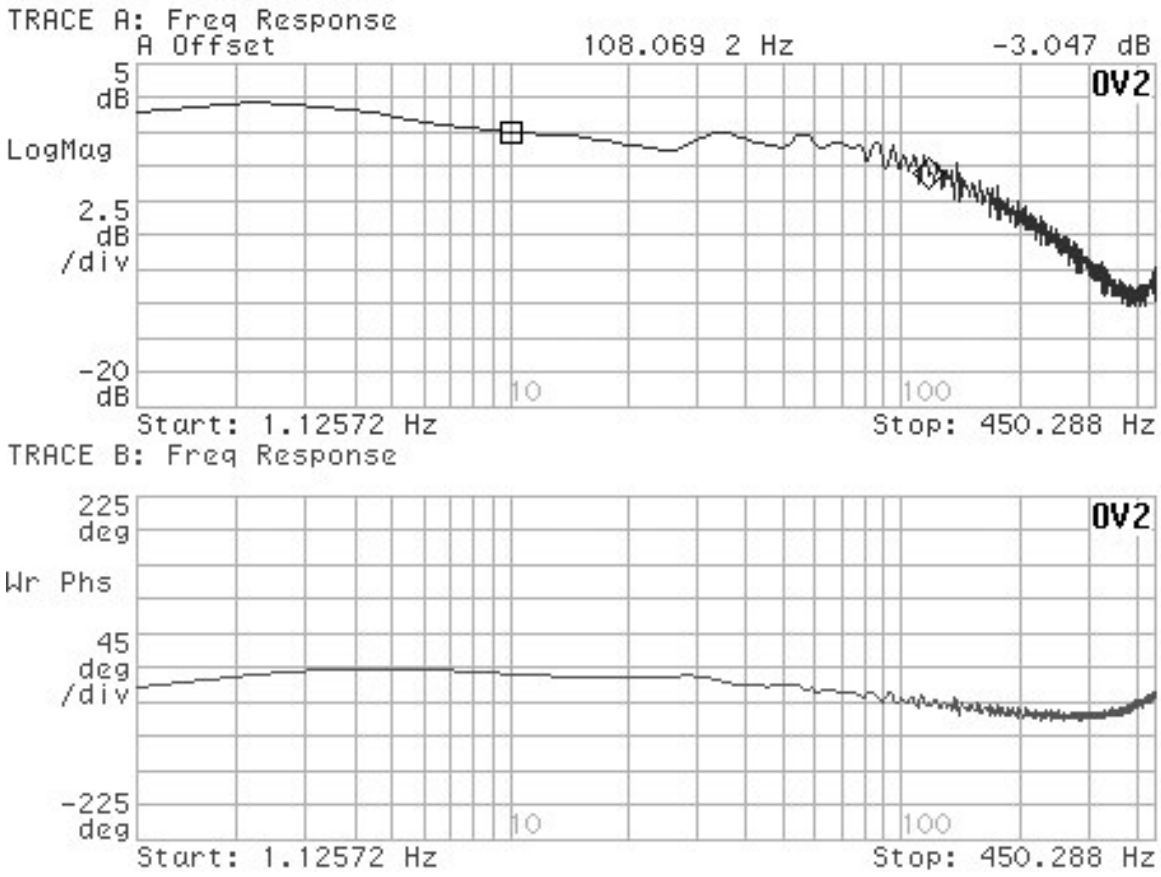

Fig. 57. The magnitude and phase response from filter #4.

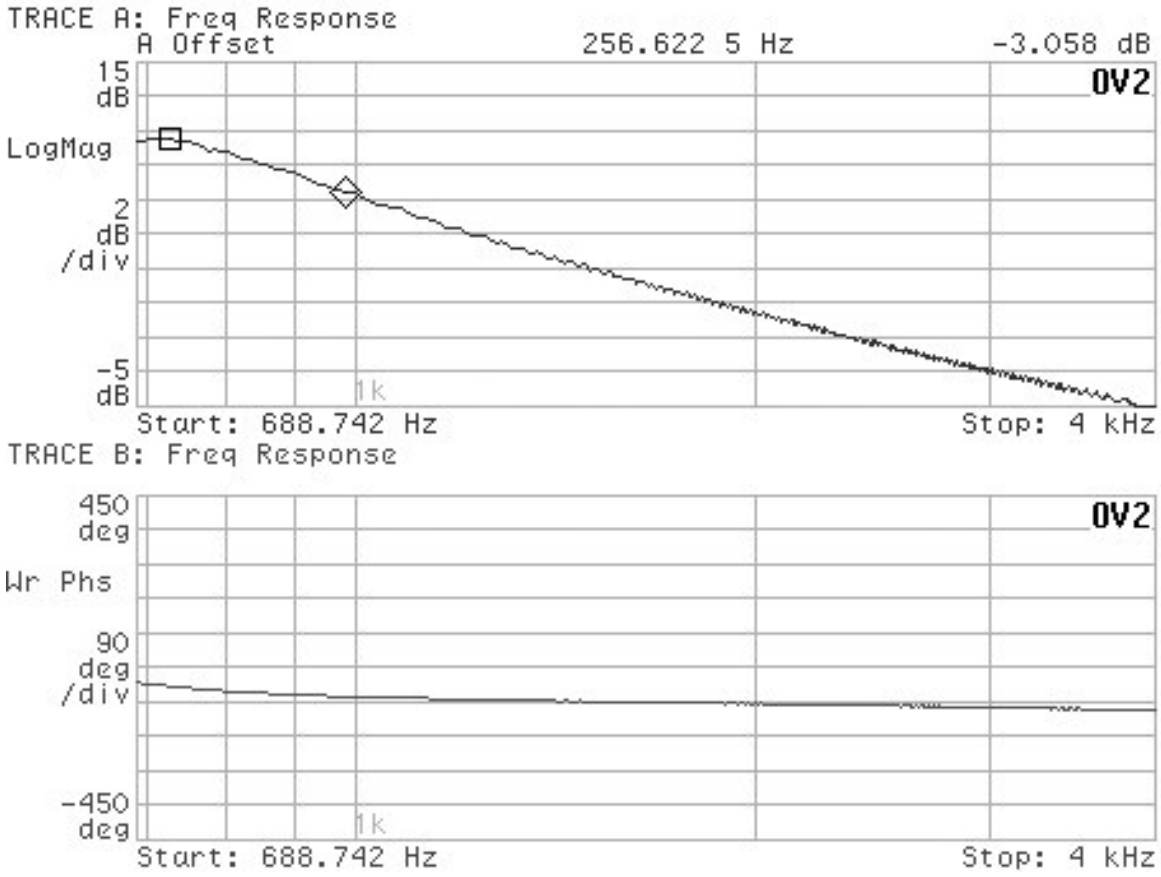

Fig. 58. The magnitude and phase response from filter #5.

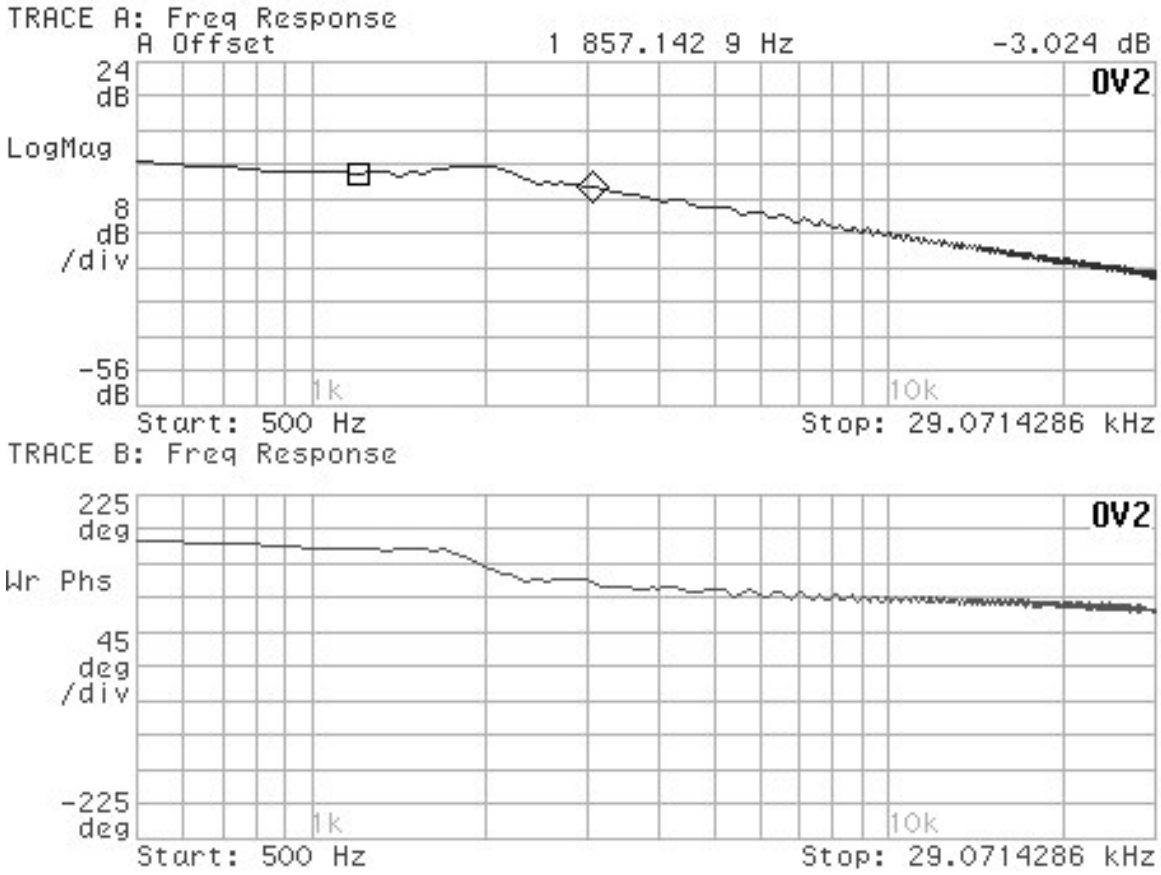

Fig. 59. The magnitude and phase response from filter #6.

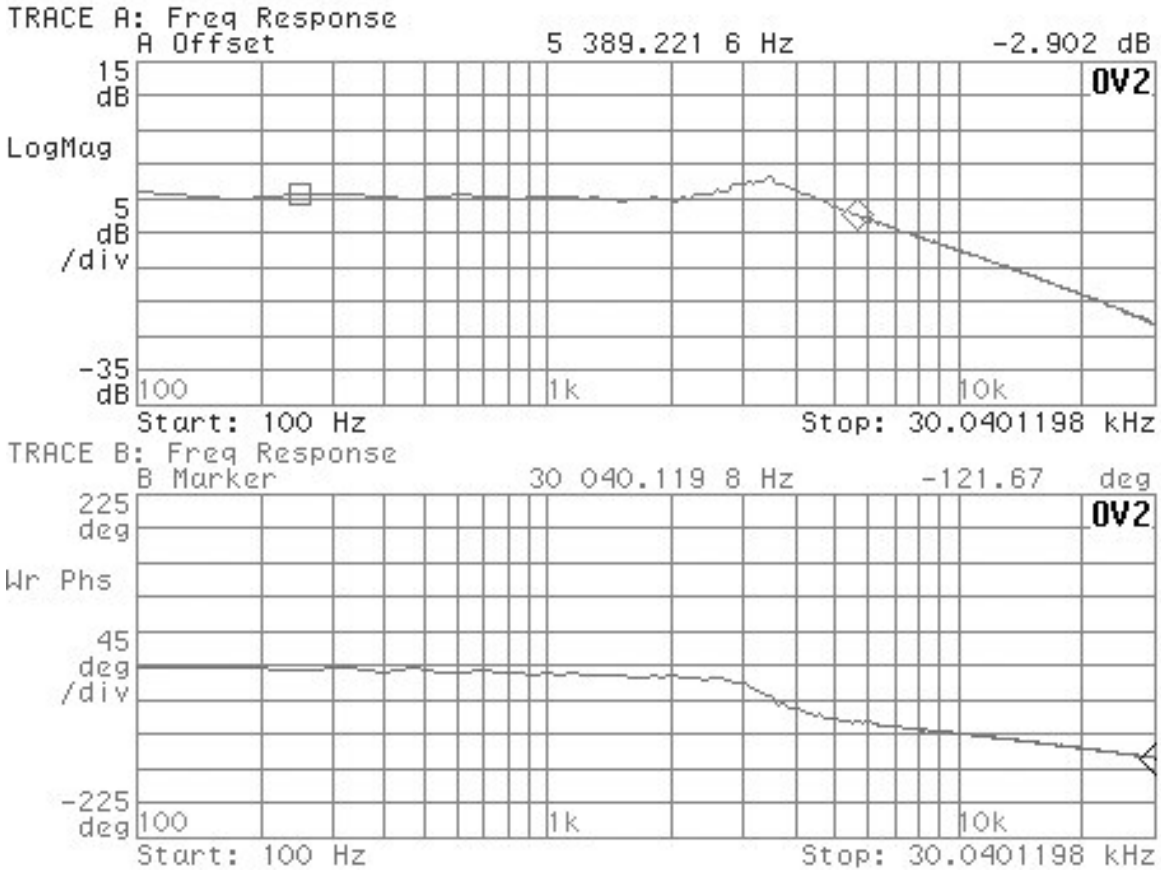

Fig. 60. The magnitude and phase response from filter #7.

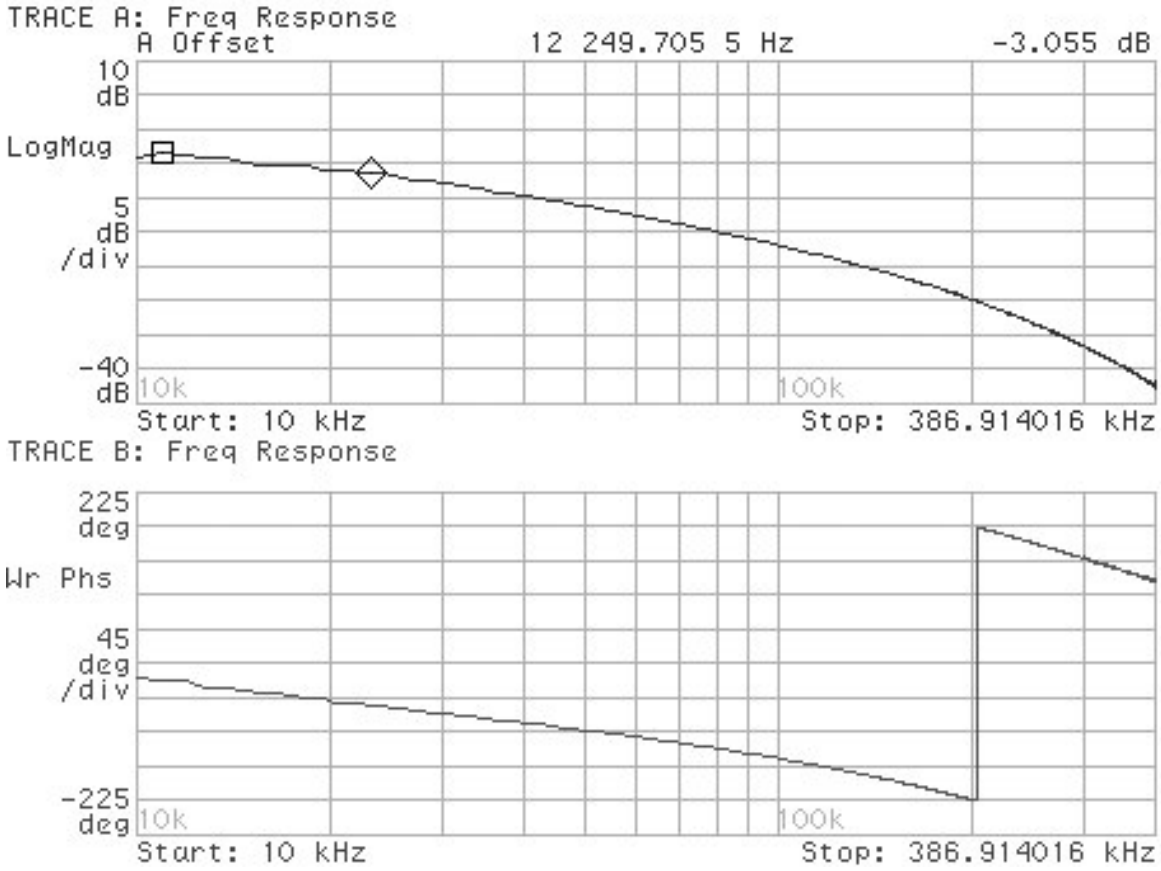

Fig. 61. The magnitude and phase response from filter #9.

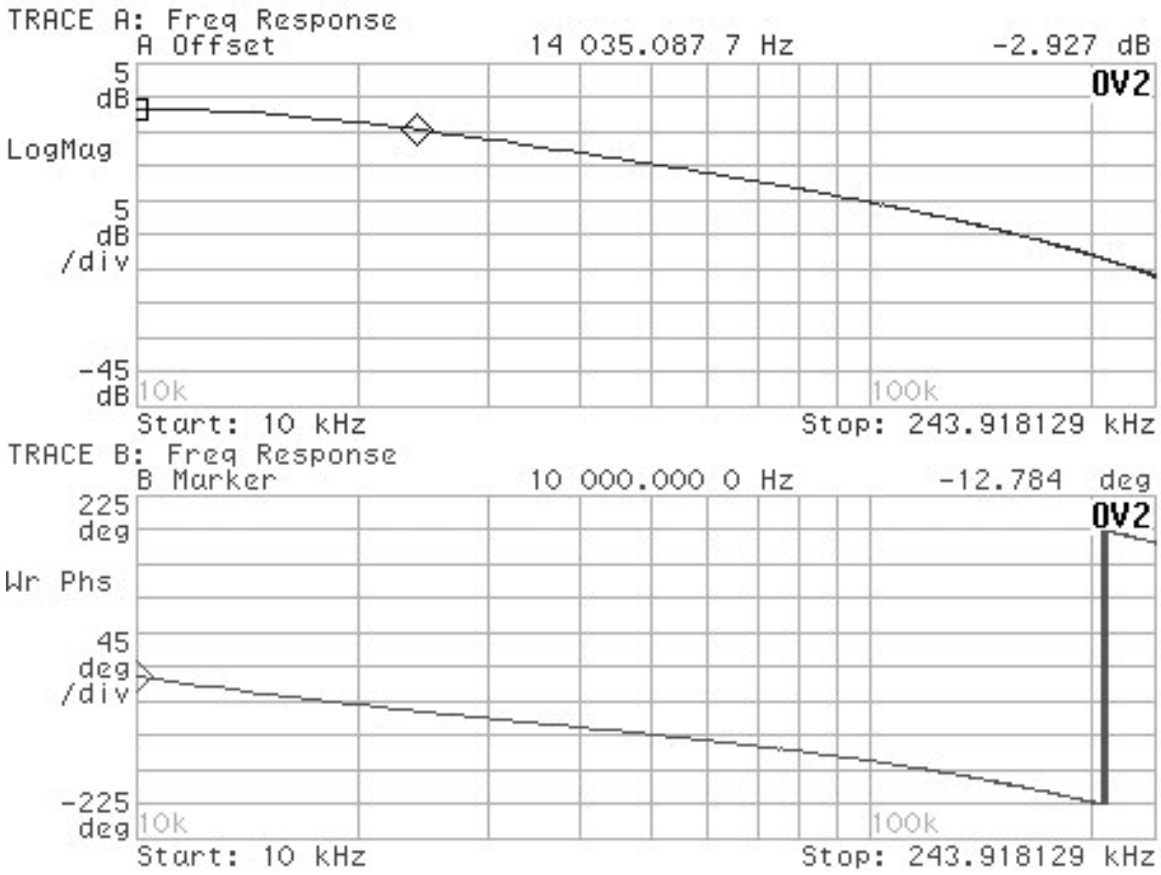

Fig. 62. The magnitude and phase response from filter #10.

VITA

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