MICROCHIP ANALYSIS OF TEMPERATURE AND HUMIDITY'S EFFECT ON THE PERFORMANCE OF SUPPLY VOLTAGE AND AGE

A Thesis

by

JADE ALEXIS CHAPMAN

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Chair of Committee,	Rainer Fink
Co-Chair of Committee	Wei Zhan
Committee Member,	Jeyavijayan Rajendran
Head of Department,	Victor Leon

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ABSTRACT

Semiconductor chips are commonly duplicated overseas and sold on the black market, which causes product failures worldwide and diminishes the reputation of the companies involved in the supply chain. Currently, companies use a burn-in test: this test involves equipment that is used to test and evaluate high power chips, boards, or products. This prevents defective chips from being incorporated into any finished devices. While this method is quite common, the process will never eliminate the possibility of failed chips. Some are random and cannot be traced back to their failure cause. This research aims to determine how temperature and humidity affects a microchip at its different stages of life. This project will use a DOE, Design of Experiments, Analysis to determine the trend between temperature, humidity, VCC, chip-to-chip variation, age and how it affects, VOH, VOL, VIH, VIL, and power consumption. To test the hypothesis that an older chip leads to more failures and particular environment can detect a defective chip based on the input conditions of temperature, humidity, VCC, chip-to-chip variation, and age, this research will design an autonomous environment that will reduce the amount of failed chips that are used in production. The system will adjust and maintain the temperature and humidity of a chamber where the microchip will be tested. The chamber read accurately and precisely as well as the microchip voltage inputs and outputs. These results suggest that all values of VOH, VOL, VIH, VIL, and power consumption can be read, calculated, and recorded

onto a DOE Analysis excel sheet to observe the results and produce the required graphs of temperature and humidity vs VOH, VOL, VIH, VIL, and power consumption.

DEDICATION

This paper is dedicated to Dr. Rainer Fink for pushing myself to become the best engineer. He has always been an inspiration as he always took the time to fulfill my needs when I bothered him about meetings, extra help outside of class, or even just for some advice for my career and future. He continually reminds me of my worth and pushes me to never accept less. In addition, this paper is dedicated to my loving parents, Alex and Brandy Chapman. I never thought I would write or even finish a thesis and they called me almost every day motivating me to write with passion and purpose. I thank all these people for their help and support and can't want to reward them in the future for it.

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NOMENCLATURE

BCS	Bryan/College Station
P	Pressure
T	Time
DUT	Device Under Test
V	Volt
DOE	Design of Experiments
VCC	Supply Voltage
VOH	Voltage Output High
VOL	Voltage Output Low
VIH	Voltage Input High
VIL	Voltage Input Low
EM	Electromigration
IC	Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
AERI	Electronic Components Distributer for Obsolete Electronic Components
UV	Ultra-violet
DNA	Deoxyribonucleic Acid
IDE	Integrated Development Environment
MSET	Master of Science in Engineering Technology

GPIO	General Purpose Input/Output
Vss	Voltage Source Supply
PCB	Printed Circuit Board
IO	Input/Output
COVID	Coronavirus Disease

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CHAPTER I

INTRODUCTION

Semiconductor chips are commonly duplicated overseas and sold on the black market, which causes product failures worldwide and diminishes the reputation of the companies involved in the supply chain. Currently, companies use a burn-in test: this test involves equipment that is used to test and evaluate high power chips, boards, or products. This prevents defective chips from being incorporated into any finished devices. While this method is quite common, the process will never eliminate the possibility of failed chips. Some are random and cannot be traced back to their failure cause. This research aims to determine how temperature and humidity affects a microchip at its different stages of life. This project will use a DOE, Design of Experiments, Analysis to determine the trend between temperature, humidity, VCC, chip-to-chip variation, age and how it affects, VOH, VOL, VIH, VIL, and power consumption.

To test the hypothesis that an older chip leads to more failures and particular environment can detect a defective chip based on the input conditions of temperature, humidity, VCC, chip-to-chip variation, and age, this research will design an autonomous environment that will reduce the amount of failed chips that are used in production. The system will adjust and maintain the temperature and humidity of a chamber where the microchip will be tested. The chamber read accurately and precisely as well as the microchip voltage inputs and outputs. These results suggest that all values of VOH,

VOL, VIH, VIL, and power consumption can be read, calculated, and recorded onto a DOE Analysis excel sheet to observe the results and produce the required graphs of temperature and humidity vs VOH, VOL, VIH, VIL, and power consumption.

Validation of Study

Problem Identification/Statement of Purpose

As technology continues to grow, so does the availability and ability to produce microchips across the globe. With this increase, more and more counterfeit chips are being produced. These chips are being relabeled, replicated and are being sold as legitimate working microchips from a verified manufacturer. Some of these chips are sometimes even recycled from old parts and reproduced and sold as brand new. This project aims to decrease the percent of chips being used in finished products that are counterfeit. Through the use of testing a range of temperature, humidity, and other factors, this test will allow test engineers to configure the testing environment to reflect the best conditions of each chip and whether it's values of VOH, VOL, VIH, VIL, or power consumption are within the proper range after being manufactured and produced in another country. If the specifications of the chip do not meet the required standards, then the test engineer will be able to know if the chip was recycled, remarked, overproduced, defective, cloned, or tampered at any point during production. This will decrease the amount of time and money spent on defective chips as well as reduce the opportunity of ruining a company's reputation for producing and selling a counterfeit chip.

CHAPTER II

RELATED RESEARCH

There are three topics of research that are being investigated, Scan-Based Characterization Through Clock Phase Sweep for Counterfeit Chip Detection, EM-based on-chip aging sensor for detection and prevention of counterfeit and recycled ICs, and An On-Chip Technique to Detect Hardware Trojans and Assist Counterfeit Identification

Scan-Based Characterization Through Clock Phase Sweep

In order contribute to the widespread effort to develop more efficient and cost-effective solutions for detecting deviations in chips, Yu Zheng, Xinmu Wang, and Swarup Bhunia, proposed a method of characterization to identify cloned counterfeit chips. This is, "based on extraction of scan path delay signatures of a chip," by using the "scan chain, a prevalent design-for-testability structure, to create a robust authentication signature [4]. This method has some notable advantages. One of those advantages is that it requires no design or hardware overhead costs because it does not need any additional embedded structure [4]. The second advantage is that it reduces test cost because it alleviates the design house from characterizing each manufactured chip instance [4]. By using clock phase sweep, test engineers can measure the delay of short scan paths with high resolution and observe that over 99% of counterfeit chips can be reliably identified even with large variations [4]. When conducting the research, they emulated 16 counterfeit chips and measured each of their nominal scan path delays based on the

required range. To validate the scan-based characterization through clock phase sweep, they choose 22 scan paths with a 2% difference on the nominal delay [4]. They discovered that the time measured between the authentic chips and the counterfeit chips were different, thus being able to identify the chips properly [4].

EM-based on-chip aging sensor for detection and prevention

This research proposes a lightweight on-chip aging sensor that will detect and prevent recycled integrated circuits by using electromigration induced aging effects [3]. This research aims to improve upon and replace the current aging sensor on IC chips as it is clear they are not as effective as they once were. Their new EM-based aging sensor exploits the natural aging/failure mechanism of interconnect wires to time the aging of the chip [3]. It is more accurate when it comes to predicting the chips usage time compared to the current method. This method is based on a new method pf physics-based stress evolution that can predict EM failure. By understanding this concept, the team was able to interconnect the wire structures based on copper interconnect technology so that the resulting wires will have detectable EM failure at a specific time with sufficient accuracy [3]. One issue they ran into was inherent variations in the metal grain sizes but by defining new wire parameters, they were able to optimize the EM model and produce successful results [3]. The team conducted a statistical and variation analysis that predicts and shows that the aging sensor can accurately predict the targeted failure times with both inherent uncertainties [3]. From their research, this research team

was additional able to prove that more parallel wires will lead to more accurate statistical predications at costs of more areas [3].

An On-Chip Technique to Detect Hardware Trojans and Assist Counterfeit Identification

This method introduces a different solution than the previous research method of detecting counterfeit chips. This method is an embedded solution for detecting hardware trojans and counterfeit integrated chips. This method suggests that hardware trojans are inserted on productions lots and not on a single device [2]. This hypothesis plans to prove that there is a distinct fingerprint of the static distribution of the supply voltage over the whole surface of the integrated chip [2]. In order to measure the fingerprint is done by obtaining and measuring an array of sensors that are sensitive to the local supply voltage [2]. The fingerprint is extracted by using CMOS logic performance which accounts for variations and the impact of the design. This research team validated their technique by basing their method off of cartography with the array of sensors that are sensitive to the supply voltage. When the ICs are at rest, which means they are powered and the clock is active, the fingerprint can be extracted and measured. In doing so, the team was able to detect changed in the supply voltage distribution induced by the hardware trojan's additional logic. In conclusion of their research, they suggested that the proposed technique will decide if the suspected microchip is identical to the reference microchip but does not allow deciding if a microchip is a counterfeit or not.

On-Chip technique is the most like the research being done in this proposal, however, it still leaves questioning on whether a counterfeit chip can be detected or not.

CHAPTER III

BACKGROUND

Chip Shortage of 2021

Due to many revolving issues, the supply chain hit an all-time low in 2021. This was mainly due to the pandemic lockdowns in industrial cities which caused everything from finished goods, foods, raw materials, electronics, parts within electronics and so much more to all come to a halt. During this shortage of parts due to locks downs, the use of electronics devices then increased due to the entire world being stuck inside and finding new ways to entertain themselves. Some manufactures such as MSI are even bringing back outdated electronic parts to keep up with the demand even though they don't perform as well. While this is a great solution, some companies don't have access to old parts building up dust in the back of a warehouse. Smaller companies that saw an opportunity to make money quicker and easier during the pandemic resorted in filling a new market demand with fake goods [6] When these companies had a request, for example, for 5000 parts needed for next week, many bent the rules and surpassed the typical testing process to fulfill the demand.

Most companies don't see a problem with counterfeit chips in the market, as a lot of the times, they won't notice a large impact until months later. Some companies, like AERI, ensure that every device goes through their guide in order to recognize counterfeit components before they are installed on any product. This company focuses on small cavities in certain locations of the chips that counterfeiters tend to forget to add on to the

chip. They often forget to fill them in during sanding and refinishing to make old parts appear new or they make them the wrong size, place components in the wrong place or it even has the wrong shape. Because of these mistakes, indents are caused on the chip and can easily be caught. Physical surface examination is not sufficient to spot fake and real microchips though as it can be time consuming and even destructive at times.

Because of the time and pressure companies face to fulfill orders, counterfeiters are taking advantage of the situation and making manufactures feel desperate to cut corners and surpass the normal supply chain verification process. Its tragic that most companies go through losing, "money now due to idle lines or lose it later due to product replacements, lawsuits, and mass recalls," and that should never be the case [6].

New Problems Arise

Chips are Difficult to Make, and It's Even Harder During Supply Crunch

Chips play a vital role in our everyday lives from controlling the cars, phones, debit and credit cards. There are a limited number of fabrication companies that have the knowledge to manufacture and test these chips and a majority are outside the United States. Currently, like the fabrication plant in Singapore, they are struggling to keep up with the demand. They are having to use every machine in the factory to keep up with the demand.

Chips take about 2-3 months to fabricate for the buyer. At Global Foundries, the chips first go through the process of completing the fabrication of the circuitry followed by testing, packaging, and distributing. Sometimes, it can take as long as 6 months

before chips ever gets into the technology it's being produced for. The chip first begins as a wafer, as seen in Figure 1, which is a skinny disc that can produce 1,000-1,500 individual chips. These wafers are first made with a protective coating. Next, another layer is added on the wafer, which makes it light sensitive, so that it is ready for the most important steps called Lithography. This is where the complex circuit patterns are draw on a photomask made of a large glass plate and then are reduced using ultra-high-performance lenses and then exposed onto the wafer. One lithography machine can cost anywhere from $25 million to $100 million.

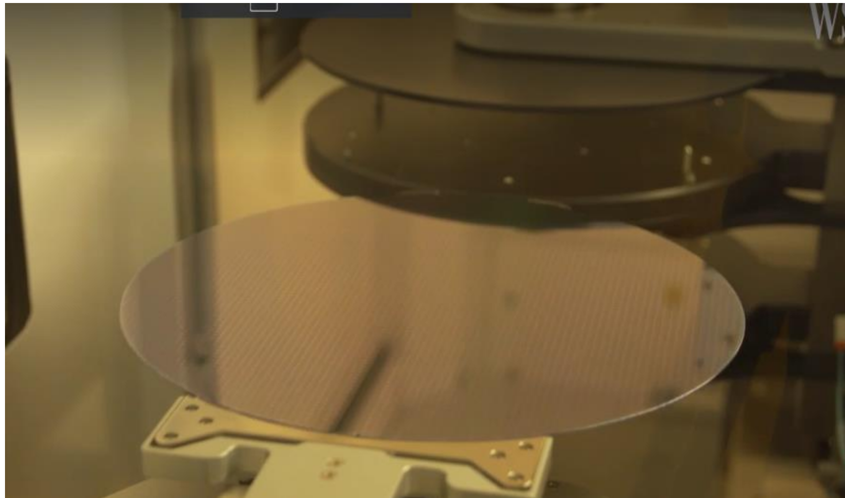

Figure 1: Global Foundries Wafer

The level of complexity of these patterns differ based on the product, such as a 5G chip for your phone versus a credit card chip, and are made with different UV rays. Shorter wavelengths mean you can sketch fine features and create a more complex design. Some of the transistors sketched in these chips are as small as 2 nanometers and can be compared to DNA strands. One the pattern is printed, the wafer is then charged.

To get to the point of charging, some of the orders need to be placed at least a year in advance. Once the wafers are finished, they are tested and then sliced into individual chips. Global Foundries produces around 600,000 wafer annually but with the pandemic, they are pushing out an additional 120,000 wafers a year.

Dangerous Consequences

The Danger of Counterfeit Microchips

Several people are stepping out to speak about the dangers of counterfeit chips as they become more known and more impactful on people's daily lives. Ken Main, a Principal Systems Scientist at the Department of Electrical and Compact Engineering at Carnegie Mellon University mentioned some of the dangers that come along with counterfeit chips. He says there are two types of dangers: benign and harmful. A benign danger is that the product performs less well or is less reliable. A harmful danger is like a charger for a battery of a cell phone or toy that could start a fire or a malicious chip that could steal information.

Counterfeiters are driven by profitability. It is cheaper to recycle or refurbish an old chip versus make a completely new one. Not only is it cheaper, but it is extremely prevalent in our society, and it can be very dangerous. They are even finding counterfeit parts in some of the United States military systems and within the government that cause such great security risks to the United States. Because of this prevalent issue, the government has tried to regulate this issue but the supply chain is so complicated and global that it's almost impossible to try to regulate counterfeit chips. Dr. Mai created

prototype that pulls the information off a chip that includes the VIN number, who manufactured it, and how long it's been on the market. Even with devices like this that can test and find counterfeit chips, the semiconductor industry is not mass enforcing devices like this within their current testing methods. Dr. Mai went on to show two chips side by side. One demonstrated a counterfeit chip and another was a real chip. He explained that they are both the same and you can't really know until you get into the chip. Regulating the mass amounts of chips that are produced is nearly impossible and the dangers are becoming more prevalent now that the pandemic has increased the amount of technology being used worldwide.

CHAPTER IV

DATA COLLECTION

Data Collection

Data collection varied based on the phase of the project. Phase 3 of the research consisted of manually collecting data using Arduino IDE and ramping an analog raw voltage from the Arduino to the target board. With the Arduino, the ramp incremented from 0 to 4096 in steps of 10 and decremented from 4096 to 0 in steps of 10. Phase 4 of the researched consisted of automating the test by collecting the data on the Eagle Tester with the press of a button. This was done by building out code to ramp the analog voltage from the Eagle Tester SPU to the target board. With the tester, the ramp incremented from 0V to 3V in steps of 0.0001V and decremented from 3V to 0V in steps of 0.0001V. The target board is programmed using Code Composer Studio. In the code, Pin 1.1 is configured as an input while Pin 1.2 is configured as an output. The output pin, Pin 1.2, is equal to the inverse of the input pin to find the VOH, VOL, VIH, and VIL. Figures 3.1 and 3.2 reflect the process of gathering data by ramping an analog voltage down and up to find the points of when the output changes from high to low or low to high.

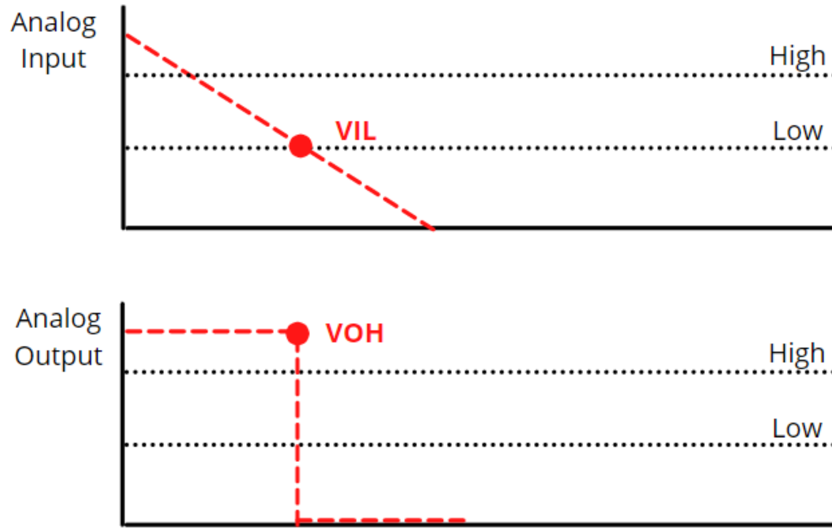

Figure 2: Ramping Down to Gather VIL/VOH

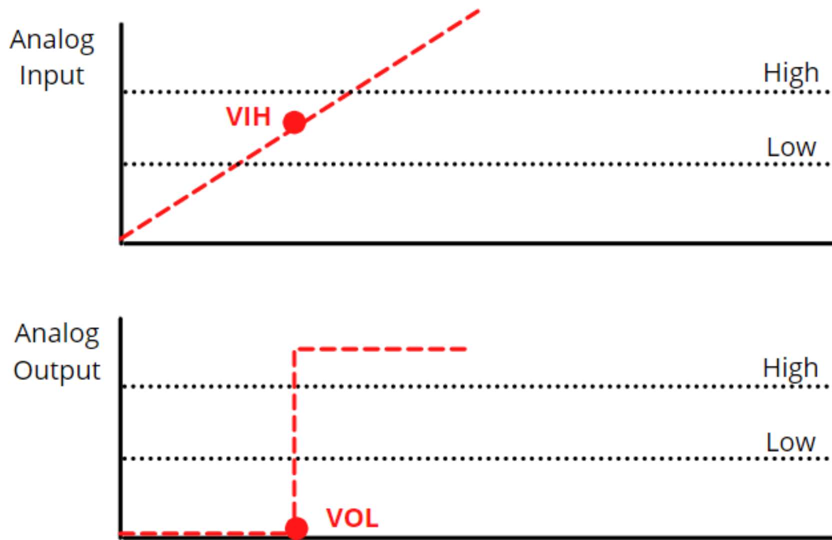

Figure 3: Ramping Up to Gather VIH/VOL

Phase 3 consists of setting the temperature and humidity of the chamber to the desired values and letting them soak for at least an hour. Once this process is done, Arduino IDE is used to run two codes: Ramp Down code and Ramp Up code. The Ramp

Down code consists of ramping the analog voltage out of the Arduino from 3.3V to 0V. Because Arduino uses an analog voltage, the value ramped from 4096 to 0 in increments of 1. Once this code is ran, the user then watches the display and waits for the transition from low to high. Once this value is recorded, it is converted to a digital voltage and recorded to the DOE Analysis Spreadsheet for further analysis. The Ramp Up code consists of ramping the analog voltage out of the Arduino from 0V to 3.3V. Because Arduino uses an analog voltage, the value ramped from 0 to 4096 in increments of 1. Once this code is ran, the user then watches the display and waits for the transition from low to high. Once this value is recorded, it is converted to a digital voltage and recorded to the DOE Analysis Spreadsheet for further analysis. To record the power consumption of the chip, the user must know some more variables. This includes the input power and output power, which must be found by using any of the known power equations. The Arduino device makes finding power consumption a bit more difficult. Voltage is not an issue but resistance and current are. If the user wants to find the current, they need to research and find the resistance between two digital pins. Once the values of resistance, current, or voltage is found at the input and the output, the power consumption can be calculated using power out minus power in. Once all the values are recorded for test 1 and test 2, the research team can analyze the data using a DOE Analysis and determine which factor truly affects the results and how that can be used to identify counterfeit chips.

Phase 4 is very similar to Phase 3 with the difference being that the Eagle Tester is the method of testing. With the Eagle tester, the user can record vast amounts of data

at a much quicker pace. This method starts of by setting the temperature and humidity of the chamber to the desired values and letting them soak for at least an hour. Once this process is done, the Eagle tester is used to run two functions with distinct codes: Ramp Down code and Ramp Up code. The Ramp Down code consists of ramping the analog voltage out of the tester from 3.3V to 0V. The Ramp Up code consists of ramping the analog voltage out of the tester from 0V to 3.3V. These codes will run at once and record the value at which the voltage changes from high to low or low to high. The value is then printed to the screen and recorded by the user on to the DOE Analysis Spreadsheet for further analysis. To record the power consumption of the chip, the user must know some more variables. This includes the input power and output power, which must be found by using any of the known power equations. The Eagle tester makes this much easier to find. The Eagle tester can read current while the Arduino does not. This is a simple code ran to read the analog current. To find resistance, it is also a very simple line of code. Once the values of resistance, current, or voltage is found at the input and the output, the power consumption can be calculated using power out minus power in. Once all the values are recorded for test 1 and test 2, the research team can analyze the data using a DOE Analysis and determine which factor truly affects the results and how that can be used to identify counterfeit chips.

Data Analysis

Design of Experiments

The reason for this choice of data analysis is because DOE helps determine when more than one input factor is suspected of influencing an output. By using this kind of analysis, researchers can determine the effect of multiple input factors and how they can be manipulated to reach the desired output. There are three key concepts when creating a design experiment, which include blocking, randomization, and replication. “When randomizing a factor is impossible or too costly, blocking lets you restrict randomization by carrying out all of the trials with one setting of the factor and then all the trials with the other setting,” [5]. This controls the source of variability which leads to greater accuracy when doing DOE. Researchers often use this to control certain factors to reduce or eliminate the contribution to the error caused by the factors. This method was not used in this research as all of the factors influence the results and the factors don’t need to be blocked to get the desired output. The goal is to see which factor most influences the response of the chip. The next concept is randomization. This concept is the most important for this research. Randomization refers to the order in which the experiments are run. By doing a random sequence, it can help eliminate effects of unknown or uncontrolled variables. This applies when increasing the humidity and temperature in the chamber. If the sequence was in order from cooled positions and then heated positions, the data might be flawed as the chamber might have some remaining humidity and heat. By randomizing the sequences, the results will have only the controllable variables factored into the analysis. The last concept is replications. This

was additionally very important to the outcomes of the research. Repetition of a full experiment aids in being able to observe and verify the values. For this experiment, every full experiment was ran twice to verify the values of VOH, VOL, VIH, VIL, and power consumption.

For the DOE Analysis, there were five input variables and five output variables. The five input variables are temperature, humidity, supply voltage, chip-to-chip variation, and age. The five output variable are VOH, VOL, VIH, VIL, and power consumption. Each of the input variables are noted with a -1 or 1. This represents the minimum and maximum value. Temperature's minimum value was determined to be the room temperature value. This value fluctuates but tends to be in the range of 65-75 degrees. Temperature's maximum value was determined by the amount of heat the chip can handle as well as the chamber and tubing. The original maximum value was 257 degrees Fahrenheit. This melted the heat resistant glue and melted the tubing in the chamber by the end of the first round of testing. For the second round of testing, the value was reduced to 175 degrees Fahrenheit. The humidity minimum value was determined to be the room humidity value. This value fluctuates but tends to be in the range of 8%-20% humid. The humidity maximum value is the maximum possible setting on the humidity chamber. This can cause the chamber to get up to 98% humidity but the team aimed for 95% during most tests. The supply voltage minimum is the lowest possible setting where the chip can still operate and be programmed, which is 2V. The supply voltage maximum is the highest possible setting where the chip can still operate and be programmed, which is 3.6V. Chip-to-chip variation is unique variable. In order to

find the minimum and maximum, the research team had to test all 8 chips to find the highest voltage reading when forcing a high voltage and the lowest voltage reading when forcing a low voltage. The first figure shows when testing with the Arduino. To the left, the values for the low and high voltage were recorded. On the right side, the minimum chip with the lowest voltage readings was determined followed by the maximum chip with the highest voltage. The second figure shows the same thing but the results when using the Eagle Tester.

Chip #	HIGHEST Voltage Reading		LOWEST Voltage Reading						TEST1		TEST2
	Raw ADC	Voltage	Raw ADC	Voltage		Lowest Voltage Output	1.79	V	CHIP 1		CHIP 4
1	419.84	2.05	366.59	1.79		Highest Voltage Input	2.06	V	CHIP 8		CHIP 5
2	419.84	2.05	366.59	1.79							
3	419.84	2.05	366.59	1.79							
4	419.84	2.05	366.59	1.79							
5	421.888	2.06	366.59	1.79							
6	419.84	2.05	366.59	1.79							
7	419.84	2.05	366.59	1.79							
8	421.888	2.06	366.59	1.79							

Table 1: Chip-to-chip Variation Results with Arduino

Chip #	HIGHEST Voltage Reading	LOWEST Voltage Reading					TEST1		TEST2
			Lowest Voltage Output	-0.00540	V		CHIP 7		CHIP 5
	Voltage	Voltage	Highest Voltage Output	3.29639	V		CHIP 1		CHIP 8
1	3.29639	-0.00643							
2	3.29484	-0.00654							
3	3.29580	-0.00574							
4	3.29468	-0.00668							
5	3.29505	-0.00541							
6	3.29509	-0.00556							
7	3.29567	-0.00540							
8	3.29587	-0.00548							

Table 2: Chip-to-chip Variation Results with Eagle

The last input variable is the age. The age minimum is considered to be a brand new chip while the age maximum is an aged chip. For the aged chip, the chips were ran

continuously for 30 days to “age” them over time. Once the chips aged, they were retested with desired conditions. Another variable that is not listed on the DOE because it is constant is the soak time. The soak time consists of soaking the chip for an hour before recording the results.

Once all the input variables minimums and maximums are found, the team conducted a full experiment with the young chips, seen below in Figure 5.

DOE Analysis for Research

RANDOM #	RUN #	A TEMP	B HUMIDITY	C VCC	D C-2-C VAR	E AGE	Y1 VIL	Y2 VIH	Y3 VOL	Y4 VOH	Y5 POWER CONSUMPTION (mW)
18	1	1	-1	-1	-1	1					0
30	2	1	-1	1	1	1					0
23	3	-1	1	1	-1	1					0
7	4	-1	1	1	-1	-1	0.3164	0.3955	2.17	2.38	4.1272
22	5	1	-1	1	-1	1					0
15	6	-1	1	1	1	-1	0.3457	0.3955	2.15	2.38	4.0686
25	7	-1	-1	-1	1	1					0
12	8	1	1	-1	1	-1	0.3457	0.3955	0.00	0.07	-0.5514

Table 3: DOE Analysis with Arduino for Young Chips

This experiment shows Test 1 DOE Analysis using the Arduino to gather the data. For any age maximums, the data was not recorded as the chips will be aged and retested later to fill in the data.

Method Criticism

With any type of method when conducting research, the data analysis being biased or misinterpreted can always be questioned. By giving as many examples as possible and explaining the process of how the data was obtained, the research team hopes to clarify any questions or concerns based on the analysis done. One factor to be considered is the time conducted in between tests. Because the total amount of time to tests the chips spans 32 hours, the data can vary greatly in the industrial world of semiconductor testing. As such, the this should be read with this in mind as time played a huge factor in the results of this thesis.

CHAPTER V

RESULTS

The results from this project are about halfway done due to the research testing still needing to be done. Due to the time it took to gather the vast amount of data, supply chain issues in obtaining parts, and the time it takes to age the microchips, the aging portion of the research was incomplete. The cells with those values are seen in grey. These cells represent the data for the aged chip needing to be tested. This will be continued research for more MSET students. For the results and analysis of this project, a DOE, design of experiments, analysis was used. This was used because of the multiple variables for inputs and outputs that needed to be analyzed. The inputs are temperature, humidity, supply voltage, chip-to-chip variation, and age of a microchip. The outputs are the VIL, VOH, VIH, VOH, and power consumption of a digital pin on the MSP430FG6626. Minitab was used to produce the random run number and the run number. This was done for both Phase 3 and Phase 4 of the project.

Before observing and analyzing the data, it is important to understand the MSP430FG6626 ideal values for VIL, VIH, VOL, VOH, and power consumption. For this research, the current output high (OH) max used was -5mA and the current output low (OL) used was 5 mA. This means that the value for VOL should be Vss+0.25, and VOH should be Vcc-0.25. The values for V_{ss} and V_{cc} are 0V and 3V, respectively. This means that the ideal value for VOL should be ~0.2500 and VOH be ~2.7500. For VIL and VOH, there are no typicals on the MSP430FG6626 datasheet.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)} = -3$ mA[1]	1.8 V	$V_{CC} - 0.25$	V_{CC}	V
		$I_{(OHmax)} = -10$ mA[2]		$V_{CC} - 0.60$	V_{CC}	
		$I_{(OHmax)} = -5$ mA[1]	3 V	$V_{CC} - 0.25$	V_{CC}	
		$I_{(OHmax)} = -15$ mA[2]		$V_{CC} - 0.60$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)} = 3$ mA[1]	1.8 V	V_{SS}	$V_{SS} + 0.25$	V
		$I_{(OLmax)} = 10$ mA[2]		V_{SS}	$V_{SS} + 0.60$	
		$I_{(OLmax)} = 5$ mA[1]	3 V	V_{SS}	$V_{SS} + 0.25$	
		$I_{(OLmax)} = 15$ mA[2]		V_{SS}	$V_{SS} + 0.60$	

Table 4: MSP430FG6626 Output Characteristics of GPIO Pins

After running the experiments for Phase 3, the results were recorded in Table 5 for Test 1 and Table 6 for Test 2. Repeatability is one of the previously mentioned important factors when conducting a DOE Analysis. Due to its importance, each phase of testing was repeated twice, which is why there is a Test 1 and a Test 2 for the manual testing.

DOE Analysis for Research

RANDOM	RUN	A	B	C	D	E	Y2	Y3	Y1	Y4	Y5
#	#	TEMP	HUMIDITY	VCC	C-2-C VAR	AGE	VIL	VIH	VOL	VOH	POWER CONSUMPTION (mW)
18	1	1	-1	-1	-1	1					0
30	2	1	-1	1	1	1					0
23	3	-1	1	1	-1	1					0
7	4	-1	1	1	-1	-1	0.3955	2.17	0.3164	2.38	10.318
22	5	1	-1	1	-1	1					0
15	6	-1	1	1	1	-1	0.3955	2.15	0.3457	2.38	10.1715
25	7	-1	-1	-1	1	1					0
12	8	1	1	-1	1	-1	0.3955	0.00	0.3457	0.07	-1.3785
1	9	-1	-1	-1	-1	-1	0.4248	1.2	0.3164	1.44	5.618
4	10	1	1	-1	-1	-1	0.3955	0.00	0.3457	0.06	-1.4285
2	11	1	-1	-1	-1	-1	0.3955	0.00	0.1655	0.06	-0.5275
6	12	1	-1	1	-1	-1	0.3955	2.18	0.3164	2.39	10.368
27	13	-1	1	-1	1	1					0
10	14	1	-1	-1	1	-1	0.3955	0.00	0.3457	0.07	-1.3785
26	15	1	-1	-1	1	1					0
16	16	1	1	1	1	-1	0.3955	2.18	0.3164	2.38	10.318
31	17	-1	1	1	1	1					0
8	18	1	1	1	-1	-1	0.3955	0.95	0.3457	1.00	3.2715
32	19	1	1	1	1	1					0
3	20	-1	1	-1	-1	-1	0.3955	0.82	0.3457	1.27	4.6215
21	21	-1	-1	1	-1	1					0
14	22	1	-1	1	1	-1	0.3955	2.16	0.3164	2.38	10.318
20	23	1	1	-1	-1	1					0
13	24	-1	-1	1	1	-1	0.3955	2.16	0.3164	2.38	10.318
11	25	-1	1	-1	1	-1	0.3955	0.00	0.375	0.05	-1.625
24	26	1	1	1	-1	1					0
19	27	-1	1	-1	-1	1					0
29	28	-1	-1	1	1	1					0
5	29	-1	-1	1	-1	-1	0.3955	0.98	0.3457	1.00	3.2715
28	30	1	1	-1	1	1					0
9	31	-1	-1	-1	1	-1	0.3955	0.00	0.3457	0.06	-1.4285
17	32	-1	-1	-1	-1	1					0

Table 5: DOE Raw Data for Manual Test 1

DOE Analysis for Research

RANDOM #	RUN #	A TEMP	B HUMIDITY	C VCC	D C-2-C VAR	E AGE	Y2 VIL	Y3 VIH	Y1 VOL	Y4 VOH	Y5 POWER CONSUMPTION
18	1	1	-1	-1	-1	1					0
30	2	1	-1	1	1	1					0
23	3	-1	1	1	-1	1					0
7	4	-1	1	1	-1	-1	0.3955	2.15	0.3164	2.38	10.318
22	5	1	-1	1	-1	1					0
15	6	-1	1	1	1	-1	0.3955	2.15	0.3457	2.38	10.1715
25	7	-1	-1	-1	1	1					0
12	8	1	1	-1	1	-1	0.3955	0.00	0.3457	0.06	-1.4285
1	9	-1	-1	-1	-1	-1	0.3955	1.12	0.3457	1.44	5.4715
4	10	1	1	-1	-1	-1	0.3955	0.00	0.3457	0.06	-1.4285
2	11	1	-1	-1	-1	-1	0.3955	0.00	0.3457	0.06	-1.4285
6	12	1	-1	1	-1	-1	0.3955	2.18	0.3164	2.38	10.318
27	13	-1	1	-1	1	1					0
10	14	1	-1	-1	1	-1	0.3955	0.00	0.3457	0.06	-1.4285
26	15	1	-1	-1	1	1					0
16	16	1	1	1	1	-1	0.3955	2.18	0.3164	2.37	10.268
31	17	-1	1	1	1	1					0
8	18	1	1	1	-1	-1	0.3955	2.16	0.3164	2.37	10.268
32	19	1	1	1	1	1					0
3	20	-1	1	-1	-1	-1	0.3955	1.2	0.3457	1.44	5.4715
21	21	-1	-1	1	-1	1					0
14	22	1	-1	1	1	-1	0.3955	2.16	0.3164	2.38	10.318
20	23	1	1	-1	-1	1					0
13	24	-1	-1	1	1	-1	0.3955	2.18	0.3164	2.38	10.318
11	25	-1	1	-1	1	-1	0.3955	0.99	0.3457	1.09	3.7215
24	26	1	1	1	-1	1					0
19	27	-1	1	-1	-1	1					0
29	28	-1	-1	1	1	1					0
5	29	-1	-1	1	-1	-1	0.3955	0.96	0.3457	0.98	3.1715
28	30	1	1	-1	1	1					0
9	31	-1	-1	-1	1	-1	0.3955	0.94	0.3457	1.05	3.5215
17	32	-1	-1	-1	-1	1					0

Table 6: DOE Raw Data for Manual Test 2

By observing Table 4 and Table 5, it can be observed that the values of VOL and VOH are off compared to their ideal value. After some research, it was determined that the Arduino puts off a different current than what was expected of the analog pins. For the manual testing for Phase 3, the current output high (OH) max assumed is -15mA and the current output low (OL) assumed is 15 mA. This means that the value for VOL should be Vss+0.60, and VOH should be Vcc-0.60. The values for V_{ss} and V_{cc} are 0V and 3V, respectively. This means that the ideal value for VOL should be ~0.6000 and VOH be ~2.4000. This better matches the data but is still not ideal.

After inputting all the data into the DOE Raw Datasheet, the data could then be analyzed on a separate excel sheet. This excel sheet is too large to insert into this document due to the multiple outputs and inputs, but it will be attached with the submission. Below, you can observe the Pareto Plot in Figure 4. The Pareto Plot shows the most effective interaction to be VCC, which is the interaction between the supply voltage to the microchip and the average of the responses of VOH, VIH, VOL, VIL, and power consumption. The next greatest interaction is the interaction between the supply voltage and the chip-to-chip variation. This is interesting because that means that the change in supply voltage and the change in chips (chip 1 and chip 8 specifically) resulted in a variation of data.

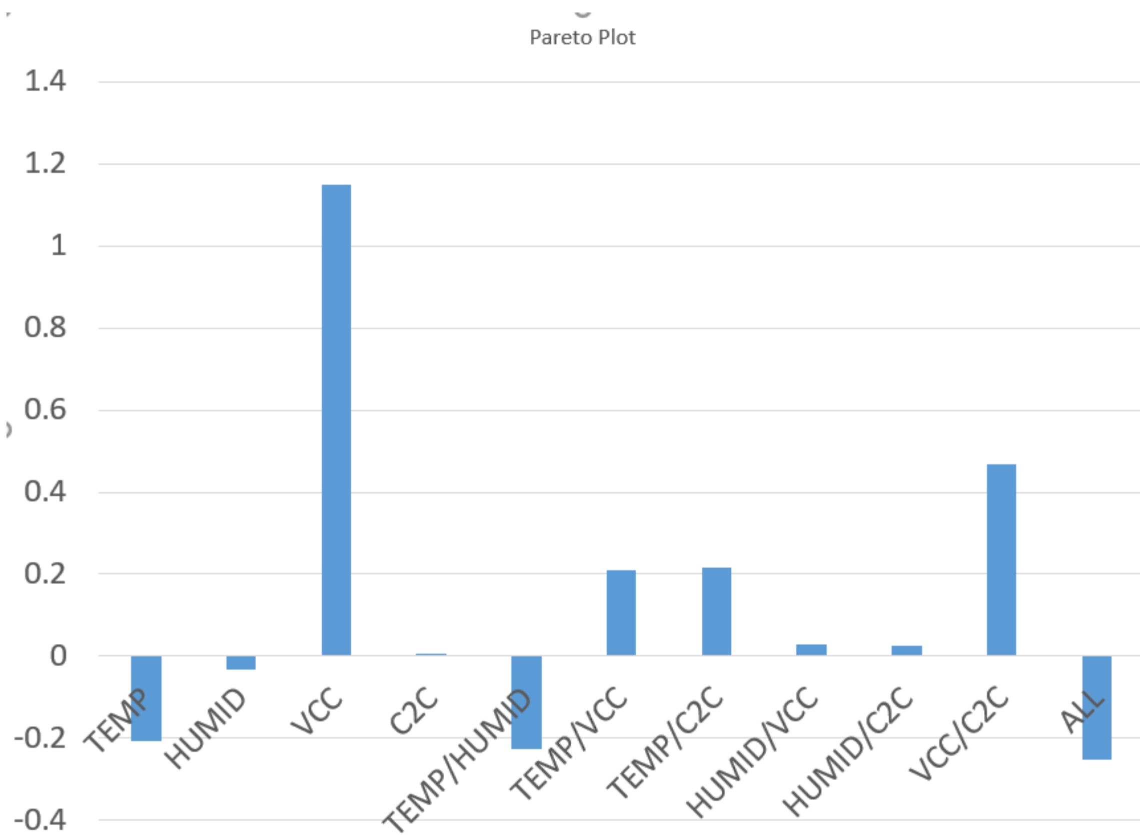

Figure 4: Pareto Plot for Manual Test 1

After obtaining the Pareto Plot for Test 1, Test 2 Pareto chart can be observed in Figure 5. Again, the supply voltage had the greatest interaction for the manual testing. The next greatest interaction is the interaction between the supply voltage and the temperature. This is interesting because it is different than Test 1 but shows why testing twice is important.

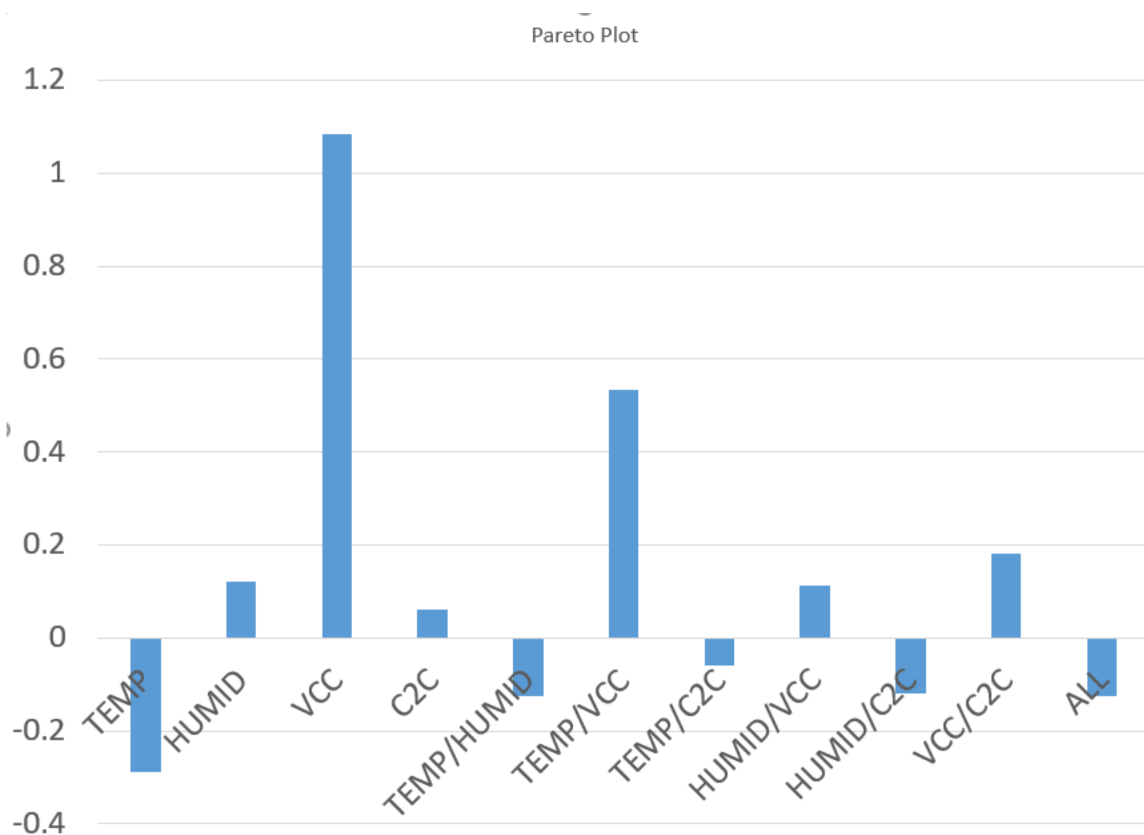

Figure 5: Pareto Plot for Manual Test 2

After Phase 3 was completed and analyzed, Phase 4 testing on the Eagle tester began. After running the experiments for Phase 4, the results were recorded in Table 6 for Test 3 and Table 7 for Test 4. Repeatability is one of the previously mentioned important factors when conducting a DOE Analysis. Due to its importance, each phase of testing was repeated twice, which is why there is a Test 3 and a Test 4 for the Eagle testing.

DOE Analysis for Research

RANDOM #	RUN #	A TEMP	B HUMIDITY	C VCC	D C-2-C VAR	E AGE	Y1 VIL	Y2 VIH	Y3 VOL	Y4 VOH	Y5 POWER CONSUMPTION (mW)
18	1	1	-1	-1	-1	1					0
30	2	1	-1	1	1	1					0
23	3	-1	1	1	-1	1					0
7	4	-1	1	1	-1	-1	0.3529	2.7762	0.2497	2.7503	11.9871
22	5	1	-1	1	-1	1					0.0000
15	6	-1	1	1	1	-1	0.3646	2.7711	0.2498	2.7500	11.9271
25	7	-1	-1	-1	1	1					0.0000
12	8	1	1	-1	1	-1	0.6001	2.4641	0.2499	2.6604	10.3017
1	9	-1	-1	-1	-1	-1	0.6001	2.4536	0.2500	2.6659	10.3289
4	10	1	1	-1	-1	-1	0.6001	2.4000	1.2561	2.6810	10.4047
2	11	1	-1	-1	-1	-1	0.5978	2.4000	0.2443	2.7021	10.4321
6	12	1	-1	1	-1	-1	0.3677	2.7626	0.2500	2.7501	11.9121
27	13	-1	1	-1	1	1					0
10	14	1	-1	-1	1	-1	0.5936	2.5683	0.2497	2.7500	10.7822
26	15	1	-1	-1	1	1					0
16	16	1	1	1	1	-1	0.6001	2.426	0.25	2.61	10.0297
31	17	-1	1	1	1	1					0
8	18	1	1	1	-1	-1	0.5408	2.6006	0.2498	2.75	11.0465
32	19	1	1	1	1	1					0
3	20	-1	1	-1	-1	-1	0.6001	2.442	0.2499	2.6082	10.0405
21	21	-1	-1	1	-1	1					0
14	22	1	-1	1	1	-1	0.5455	2.5768	0.2498	2.7500	10.9712
20	23	1	1	-1	-1	1					0
13	24	-1	-1	1	1	-1	0.5622	2.5861	0.2498	2.7500	10.9392
11	25	-1	1	-1	1	-1	0.6001	2.4151	0.25	2.5836	9.9175
24	26	1	1	1	-1	1					0
19	27	-1	1	-1	-1	1					0
29	28	-1	-1	1	1	1					0
5	29	-1	-1	1	-1	-1	0.4833	2.5202	0.25	2.75	11.3344
28	30	1	1	-1	1	1					0
9	31	-1	-1	-1	1	-1	0.6001	2.4279	0.25	2.5848	9.9233
17	32	-1	-1	-1	-1	1					0

Table 7: DOE Raw Data for Eagle Test 1

DOE Analysis for Research

RANDOM	RUN	A	B	C	D	E	Y1	Y2	Y3	Y4	Y5
#	#	TEMP	HUMIDITY	VCC	C-2-C VAR	AGE	VIL	VIH	VOL	VOH	POWER CONSUMPTION
18	1	1	-1	-1	-1	1					0
30	2	1	-1	1	1	1					0
23	3	-1	1	1	-1	1					0
7	4	-1	1	1	-1	-1	0.3507	2.7769	0.2500	2.7500	11.9966
22	5	1	-1	1	-1	1					0.0000
15	6	-1	1	1	1	-1	0.3648	2.7715	0.2500	2.7501	11.9266
25	7	-1	-1	-1	1	1					0.0000
12	8	1	1	-1	1	-1	0.6001	2.4668	0.2500	2.6639	10.3189
1	9	-1	-1	-1	-1	-1	0.6001	2.4527	0.2500	2.6625	10.3122
4	10	1	1	-1	-1	-1	0.6000	2.4000	0.2500	2.6544	10.2432
2	11	1	-1	-1	-1	-1	0.5998	2.4145	0.2449	2.6332	10.6548
6	12	1	-1	1	-1	-1	0.3674	2.7625	0.2500	2.7501	11.9136
27	13	-1	1	-1	1	1					0.0000
10	14	1	-1	-1	1	-1	0.5988	2.5689	0.2500	2.7501	10.8742
26	15	1	-1	-1	1	1					0.0000
16	16	1	1	1	1	-1	0.6001	2.4341	0.2497	2.6102	10.0923
31	17	-1	1	1	1	1					0.0000
8	18	1	1	1	-1	-1	0.5413	2.6005	0.2499	2.7501	11.0442
32	19	1	1	1	1	1					0.0000
3	20	-1	1	-1	-1	-1	0.6001	2.3345	0.2500	2.7501	11.7845
21	21	-1	-1	1	-1	1					0
14	22	1	-1	1	1	-1	0.5580	2.5867	0.2494	2.7501	10.9605
20	23	1	1	-1	-1	1					0
13	24	-1	-1	1	1	-1	0.5619	2.5859	0.2499	2.7501	10.9411
11	25	-1	1	-1	1	-1	0.6001	2.4163	0.25	2.5849	9.9765
24	26	1	1	1	-1	1					0
19	27	-1	1	-1	-1	1					0
29	28	-1	-1	1	1	1					0
5	29	-1	-1	1	-1	-1	0.4762	2.5209	0.25	2.75	11.3739
28	30	1	1	-1	1	1					0
9	31	-1	-1	-1	1	-1	0.6001	2.4288	0.25	2.5844	9.9214
17	32	-1	-1	-1	-1	1					0

Table 8: DOE Raw Data for Eagle Test 2

By observing Table 6 and Table 7, it can be observed that the values of VOL and VOH are much better compared to their ideal value. This is due to the Eagle Tester being much more accurate due to it's ability to read current precisely.

After inputting all the data into the DOE Raw Datasheet, the data could then be analyzed on a separate excel sheet. This excel sheet is too large to insert into this document due to the multiple outputs and inputs, but it will be attached with the submission. Below, you can observe the Pareto Plot in Figure 6. The Pareto Plot shows the most effective interaction to be VCC, which is the interaction between the supply

voltage to the microchip and the average of the responses of VOH, VIH, VOL, VIL, and power consumption. This is incredible as the data reflected to be about the same for manual and Eagle testing. The next greatest interaction is once again the interaction between the supply voltage and the temperature.

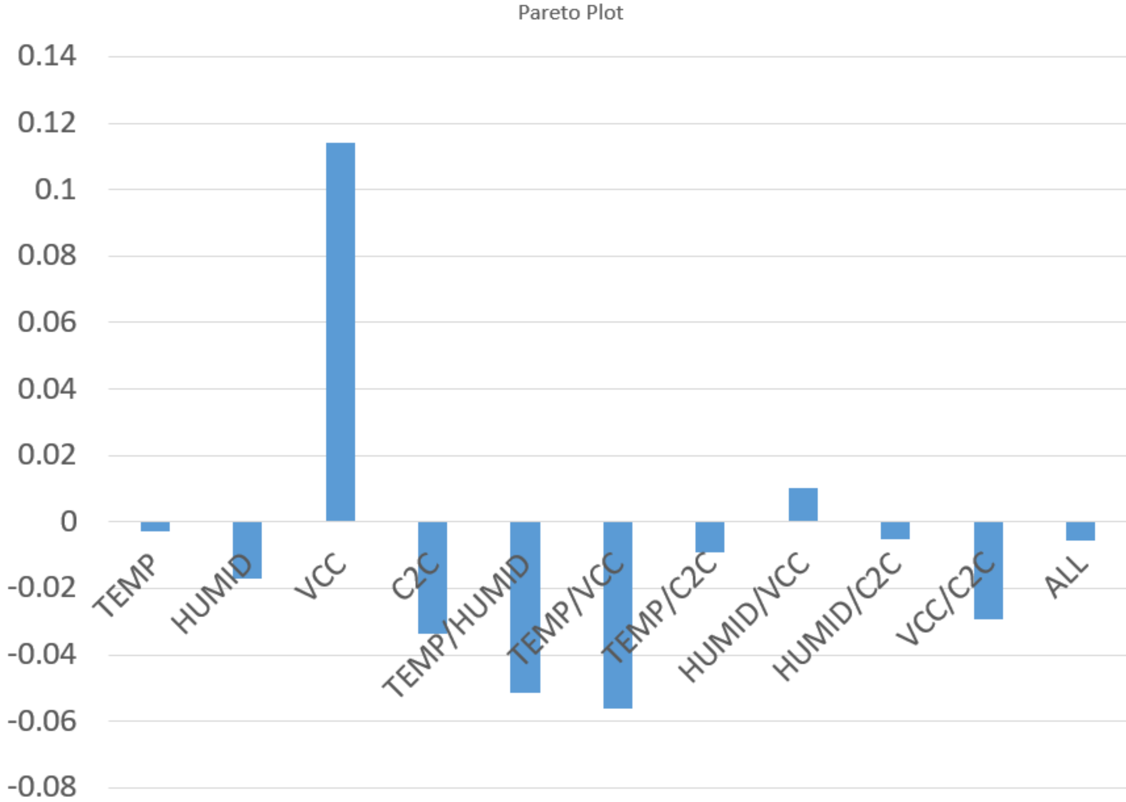

Figure 6: Pareto Plot for Eagle Test 1

After obtaining the Pareto Plot for Test 3, Test 4 Pareto chart can be observed in Figure 7. Again, the supply voltage had the greatest interaction for the Eagle testing. This shows that the data is consistent across the board for the greatest interaction. The next greatest

interaction is the interaction between temperature and humidity. This is even more interesting as humidity had not been a great factor until the final round of testing.

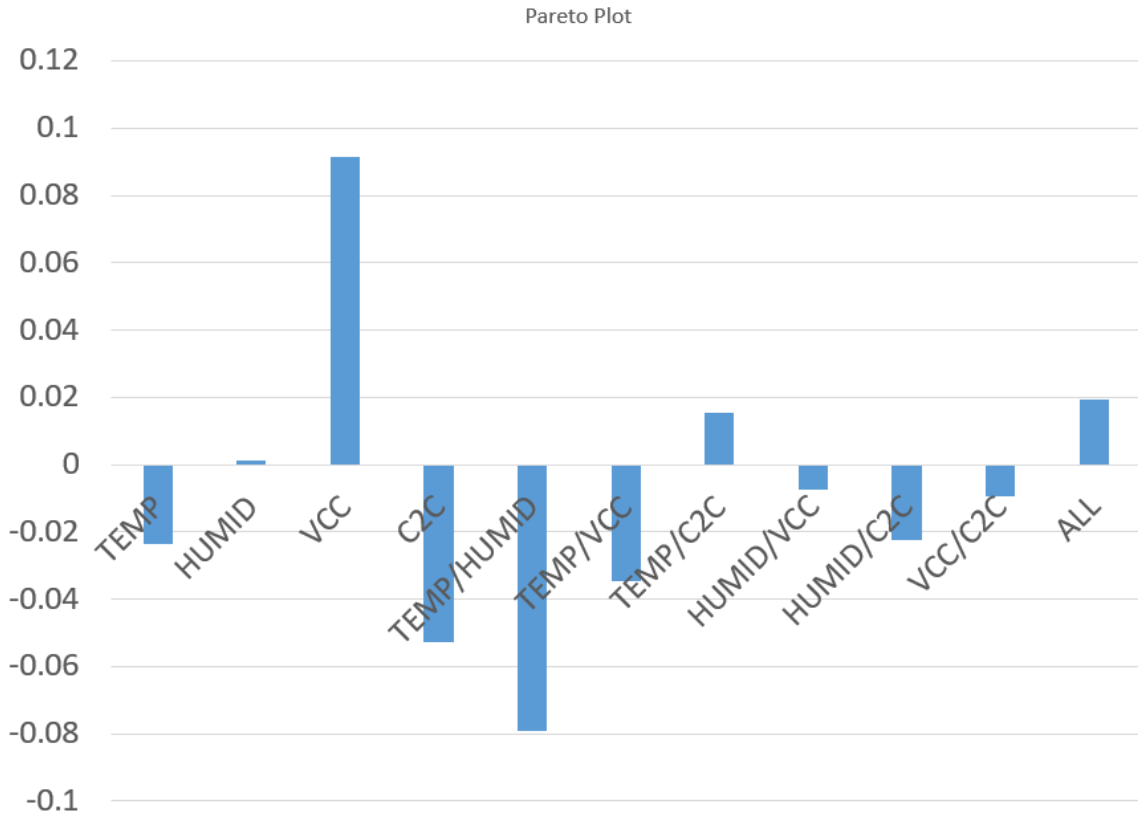

Figure 7: Pareto Plot for Eagle Test 2

CHAPTER VI

DISCUSSION

The results from this research show that the responses recorded have large correlation with the supply voltage to the microchip. The secondary correlation being the interactions between the supply voltage and chip-to-chip variation, temperature, and humidity. From the other previously discussed research, the supply voltage can be the most revealing factor of if a chip is counterfeit or not. This data seconds that and shows that this could be true and can been proven. A way to improve this process is to automate the timing of the soak time. This could be done by putting a time in the code and an array of values that lets the user know that the temperature and humidity is changing and whether they need to switch out the microchip with another one. This process was quite tedious and took over 64 hours to complete. While it took a very long time, it did show that the factor of age in a microchip is extremely important when trying to detect counterfeit chips. While this research took some time, it revealed that supply voltage should be a major factor to observe when detecting counterfeit chips.

Limitations

Some of the limitations this research had was design, product ordering issues, and time. This research project was once an undergraduate senior design project. When the project was taken over, it worked to some extent, but it was not research ready. The first design change was the code. The code was rewritten and simplified as the team

seemed to have tried to build out their own libraries for the stepper motor and temperature-humidity sensor. I added in the already built libraries and replaced lines of code with one function. Once this was done, the project was still not working well. There seemed to be several power issues. This was fixed by completely removing both PCBs the team created as well as the MSP432 that shorted and powering the prototype using a 4 channel relay, Arduino MEGA, and the existing breadboard. Because of the power issues with the chamber PCB as well as the functionality of the PCB not allowing to talk to any digital IOs, the chamber had to be recut and redesigned to test chips. This was done by purchasing a MSP-TS430PZ100AUSB - 100-pin Target Development Board for MSP430FG6x MCUs and MSP-FET MCU Programmer and Debugger. This allowed all 100 pins on the MSP430FG6626 chips to be programmed and debugged for testing. Once the part was installed and the chamber was recut, the prototype was functional and completed. The next limitation was the ordering issues. This was a minor limitation. Texas Instruments did not allow more than three of the target boards to be purchased by one person, which caused delay in receiving product. The last limitation was time. Due to the time dedicated to fixing the undergraduate project, delay in obtaining parts, long testing hours, and catching COVID in February, the second round of testing for the aged chips was not possible. This would be great for a future research project as the next team will be able to retest and analyze new data, which could easily take another two semesters.

CHAPTER VII

CONCLUSIONS

This research project deemed successful after determining from the responses of the VOH, VOL, VIH, VIL, and power consumption that the prototype was able to obtain the values to be recorded and analyzed. It was successful due to the conclusion that the supply voltage is the biggest determining factor on whether a chip will produce the correct or incorrect values of voltage. The process was informative as it proved an earlier hypothesis so that now future work can progress in determining detection of counterfeit chips and their identification register so that chips as such as thrown out and not sold into the public.

Future Research

Significance

The accomplishment of this project's objectives will result in novel methods, procedures, and testing capabilities for Texas Instruments. By implementing this system, this will allow for Texas Instruments test engineers to test microchips using the same equipment and machines they already use but with different parameters. It will require little training and time to implement as Texas Instruments already test the microchips under temperature to verify the specifications. When humidity is incorporated into the current testing methods, test engineers will be able to detect any counterfeit chips regardless of the counterfeiting method. As engineers begin to gain a deeper understanding of how temperature and humidity affect the overall performance of a chip

and how variations in the specifications can lead to detection of counterfeit or damaged chips, integrated chip designers will eventually be able to build and produce the proper sensors to prevent the possibility of anyone counterfeiting microchip for resell. The system will additionally allow for more research in detection solutions as there could be new discoveries with future work.

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