A SINGLE-PHASE GAN TOTEM-POLE BRIDGELESS PFC WITH AN H-BRIDGE

ACTIVE POWER DECOUPLING

A Thesis

by

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ABSTRACT

This research proposes a single-phase power factor correction (PFC) approach employing a GaN Totem-Pole topology with an H-Bridge Active Power Decoupling (APD). The proposed topology assures the achievement of high efficiency with unity power factor and high-power density with minimum losses over a wide range of voltages. Moreover, the GaN Totem-Pole PFC with the H-Bridge APD has shown a significant enhancement on the total energy storage requirement in comparison with the GaN Totem-Pole PFC without the H-Bridge APD. The total energy storage requirement is reduced from 143 J on the Totem-Pole PFC without the H-Bridge APD to around 3.76 J on the Totem-Pole PFC with the H-Bridge APD and the large aluminum electrolytic DC-Link Capacitor (1,880 µF) located at the interface between the converter and the DC load is replaced by the suppressed polypropylene film DC-Link Capacitor (5 µF). The additional H-Bridge APD circuit generates a reactive power that matches and buffers the undesirable low-frequency power ripple caused by the single-phase inherited double-line frequency that exists naturally at the AC side and gets injected into the converter. The topology composes of three GaN high switching frequency legs (100 kHz) and one low (line) frequency leg (60 Hz). The H-Bridge APD circuit consists of two of the high switching frequency legs (100 kHz) with 4 GaN FETs, a decoupling capacitor and an inductor. GaN FETs were used instead of MOSFETs due to their superiorities of having higher switching frequency ensuring lower switching losses, higher efficiency leading to lower conduction losses, lower reverse recovery losses and higher power density.

# DEDICATION

I dedicate this thesis to my wife Nourah, my daughter AlZainah and my son Humoud, for their patience and continuous encouragement. This key academic milestone would never be accomplished without their incessant motivation and support. This thesis is also dedicated to my parents, who kept supporting me along my entire educational path.

# ACKNOWLEDGEMENTS

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**Contributors**

**Funding Sources**

NOMENCLATURE

| | |
|---|---|
| AC | Alternating Current |
| DC | Direct Current |
| EV | Electric Vehicle |
| UPS | Uninterrupted Power Supply |
| LED | Light-Emitting-Diode |
| EMI | Electromagnetic Interference |
| PF | Power Factor |
| PFC | Power Factor Correction |
| THD | Total Harmonic Distortion |
| PPD | Passive Power Decoupling |
| APD | Active Power Decoupling |
| PI | Proportional Integral |
| PWM | Pulse Width Modulation |
| RMS | Root-Mean-Square |
| ESR | Equivalent Series Resistance |
| Si | Silicon |
| SiC | Silicon Carbide |
| MOSFET | Metal–Oxide–Semiconductor Field-Effect Transistor |
| GaN | Gallium Nitride |
| PM | Phase Margin |
| FFT | Fast Fourier Transform |

| | |
|---|---|
| ADC | Analog to Digital Converter |
| CCS | Code Composer Studio |
| DSP | Digital Signal Processor |
| ZVS | Zero Voltage Switching |

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# 1. INTRODUCTION

## 1.1 AC/DC Converter Applications

Data centers have recently become an essential part of advanced computing infrastructures and the backbone of current global economy. Most organizations around the world are utilizing data centers for cloud solutions, compliance assurances and colocation services. This exploitation has increased over the past ten years causing a tremendous rise in the electrical power consumption. U.S. data centers alone consumed more than 90 billion kilowatt-hours of electricity in 2017 and are on track to consume about 140 billion kilowatt-hours of electricity annually by the end of 2020. [1] Therefore, it is crucial to have a very high-power efficiency AC/DC converter (Rectifier) which is the key element used to convert the 220V input AC voltage into 400V DC voltage fed to a DC/DC buck converter that steps down the voltage from 400V to 12V to power up motherboards of the data centers. Furthermore, the resent evolution of numerous DC loads such as Light-Emitting-Diodes (LEDs), Electric Vehicles (EVs), Uninterrupted Power Supplies (UPSs), Telecommunication Equipment has increased the need of having an optimal AC/DC converter with minimum losses.
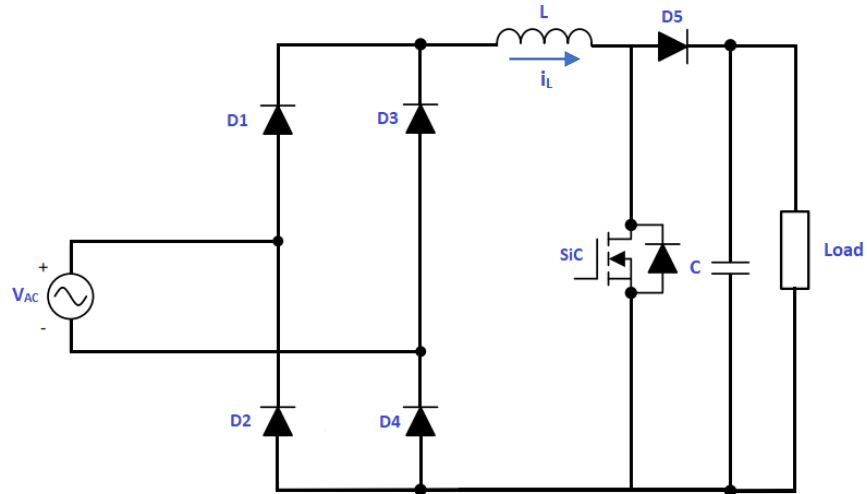
Figure 1. Diode-Bridge Boost PFC
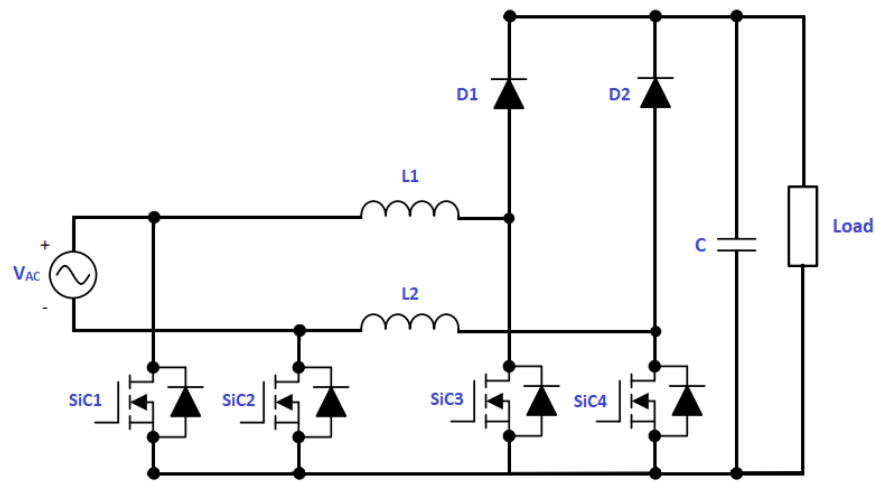


Figure 2. Semi-Bridgeless Dual-Boost PFC

## 1.2 Comparison of PFCs in Literature

Before the evolvement of the wide-band-gap (WBG) devices, the 600V Si super-junction (SJ) MOSFETs were the revolutionary power devices for AC/DC power supplies with low power ranges (few kW) [2]. Negative current state in Si MOSFETs and Si SJ MOSFETs is not favored, because of their meager reverse recovery condition, making the conventional Diode-Bridge Boost Power Factor Corrector (PFC) to be the best topology

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Figure 1. On the other hand, the Semi-Bridgeless Dual-Boost PFC Figure 2 has less conduction loss; however, its utilization of the active and passive components is much inferior in comparison with the classical Boost PFC [3]. Hence, the conventional Boost PFC has become the most convenient single-phase PFC in the past few decades. But then again, its switching frequency is ordinarily below 100 kHz and that is due to its large switching losses. Therefore, it imposes limitations on the reduction of the converter size. The state-of-the-art 600V GaN devices; yet, have brought tremendous improvements to the AC/DC converters due to their low on-resistance, compact packaging, zero reverse recovery loss and fast switching speed [4], [5].
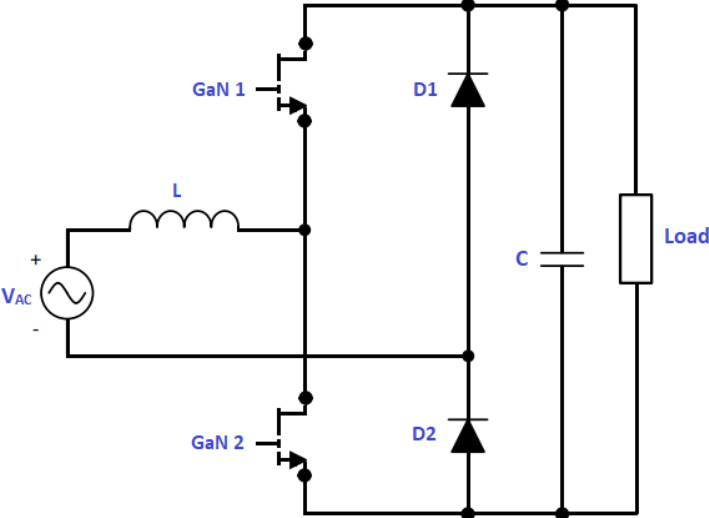


Figure  3. Totem-Pole PFC with Diodes for Line-Rectification
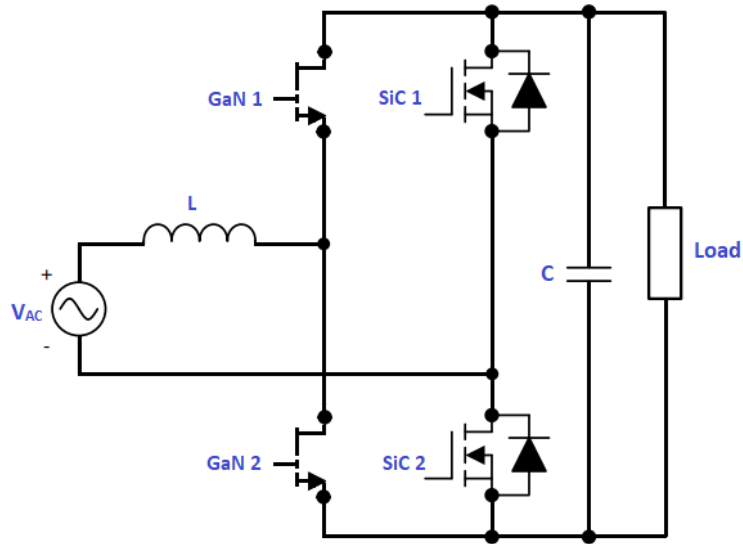
Figure 4. Totem-Pole PFC with MOSFETs for Line-Rectification

The Totem-Pole Bridgeless PFCs with the 600V GaN switches shown in Figures 3 and 4 have revealed surpassing operation on the PFC stage of the AC/DC converters compared to the conventional Diode-Bridge Boost PFC and the Semi-Bridgeless Dual-Boost PFC [6], [7]. Due to the high utilizations of the active and passive components in the GaN totem-pole PFC in addition to its low Electromagnetic Interference (EMI) noise, the GaN totem-pole PFC is capable of achieving minimal conduction losses [7]. Owing to the exclusion of the reverse recovery issue, it has been proven that GaN Totem-Pole PFCs can work perfectly on hard switching mode with an efficiency that can reach up to 99% [2], [7], [8], [9].

Table 1 below illustrates the advantages and disadvantages of the Conventional Diode-Bridge Boost PFC, Semi-Bridgeless Dual-Boost PFC, and the Totem-Pole Bridgeless PFC in terms of EMI performance, Power Density, Efficiency, and Heat Distribution. As shown in the table, the Conventional Diode-Bridge Boost PFC has a good

EMI performance with a moderate power density, low efficiency, no heat distribution and a relatively low cost, while the Semi-Bridgeless Dual-Boost PFC has a good EMI performance as well, but a low power density, moderate efficiency, has a heat distribution and a moderate cost. The Totem-Pole Bridgeless PFC has a high-power density, high efficiency, heat distribution, moderate cost but low EMI performance [10]. Yet, the Totem-Pole Bridgeless PFC stands out in comparison with the other two PFCs.

Table 1. Comparison between Conventional Diode-Bridge PFC, Semi-Bridgeless Dual Boost PFC and Totem-Pole Bridgeless PFC

| Comparison Factors | Conventional Diode-Bridge Boost PFC | Semi-Bridgeless Dual-Boost PFC | Totem-Pole Bridgeless PFC |
|---|---|---|---|
| EMI performance | GOOD | GOOD | LOW |
| Power Density | MODERATE | LOW | HIGH |
| Efficiency | LOW | MODERATE | HIGH |
| Heat Distribution | NO | YES | YES |
| Cost | LOW | MODERATE | MODERATE |

**1.3 Power Decoupling Topologies**

Due to the single-phase inherited double-line frequency power that exists naturally at the AC side and gets injected into the converter and consequently causes an undesirable low-frequency power ripple at the DC load causing fluctuations and reduces the power density, a large aluminum electrolytic DC-Link Capacitor is placed at the interface

between the converter and the load to buffer the power ripple. This Passive Power Decoupling (PPD) approach however, has fundamental disadvantages such as having a short life time and low system reliability caused by the large aluminum electrolytic dc-link capacitor. To avoid the abovementioned drawbacks of the PPD, an Active Power Decoupling (APD) is introduced. A typical APD consists of a buffering circuit that involves passive devices like inductors/ capacitors, and active switches like diodes/ MOSFETs/ GaNs. The load voltage instabilities could be substantially mitigated by transferring the low frequency ripple power to the decoupling circuit [11].

Several APD techniques were introduced and applied on various types of Inverters, Rectifiers, and PFCs [11-17]; nonetheless, they either sacrifice efficiency by having high switching losses, or have a non-unity power factor. In addition, some proposed APD methods consist of complex control topologies with several PI/ PR controllers to control the APD circuit. A simple control method is introduced in [18] and is implemented on a single decoupling leg added to an inverter; however, this topology has not been explored for a PFC rectifier operation. Thus, to achieve high efficiency with unity power factor, high-power density with minimum losses and a suppressed DC-Link Polypropylene Film Capacitor, the GaN Totem-Pole Bridgeless PFC with an H-Bridge APD Topology and a simple yet reliable control methodology is proposed in this research.

## 1.4 Research Objectives

The objective of this research is to replace the bulky aluminum electrolytic DC-link capacitor of an AC/DC boost converter (rectifier) with a suppressed polypropylene film DC-link capacitor. For typical boost power factor correctors, a passive large DC-link capacitor is positioned between the AC/DC boost converter and the load. This capacitor

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is required to filter out the second order harmonic accompanying the dc output power, which accordingly reduces the output power ripple and smoothens the load power waveform. This filter is also needed to absorb any undesirable ripples and noises caused by sudden changes or fluctuations in the ac power supply (grid).

In comparison with the film type capacitor, electrolytic capacitors have several weaknesses such as high equivalent series resistance (ESR), huge leakage current, large tolerance, high heat dissipation, and short lifetime. On the other hand, although having a better performance, better efficiency, and longer lifetime, equivalent film type capacitors are much larger in size compared to electrolytic capacitors with the same specifications. Therefore, it is necessary to find an alternative approach for the passive power decoupling method.

The active power decoupling (APD) technique allows us to merge the advantages of both electrolytic capacitors and film type capacitors by reducing the DC-link capacitance requirement. The active power decoupling circuit provides an additional path for the second order harmonics to pass through and consequently get filtered. Thus, the APD technique leads to a huge reduction in the output power ripple. This circuit primarily consists of a capacitor and an inductor and gets operated through the synchronous switching operation of four GaN/MOSFET switches. Hence, implementing the APD concept on a Totem-Pole PFC with GaN switches will not only assure the replacement of the bulky DC-link capacitor with a suppressed one, but will also assure the achievement of high efficiency, unity power factor, and minimum losses.

A full analysis of the proposed GaN Totem-Pole PFC with an H-Bridge Active Power Decoupling technique will be provided in this study. In addition, a full overview of

the Totem-Pole PFC operation, design, and implementation will be analyzed. The PI controllers design methodology of the proposed approach will be explicitly shared in this research. Furthermore, simulation results and hardware prototype will be examined and documented in this report.

**1.5 Overview**

Section 1 of this thesis starts with an introduction of some applications that uses AC to DC converters and gives a glance of the importance of having very efficient rectifiers. Followed by a comparison of the classical Diode-Bridge Boost PFC, Semi-Bridgeless Dual-Boost PFC, and the Totem-Pole Bridgeless PFC in terms of EMI performance, Power Density, Efficiency, and Heat Distribution. Furthermore, this section provides some literature review of various types of Passive Power Decoupling (PPD) as well as Active Power Decoupling (APD) techniques. The introduction section also covers the research objectives of the thesis and concluded with an overview of the work structure.

Section 2 is a short section describing the Totem-Pole Bridgeless Power Factor Correction principle of operation. A table is provided in this section showing all states of operation as well as the status of the active switches and the passive components.

Section 3 presents the proposed GaN Totem-Pole Bridgeless PFC with the H-Bridge Active Power Decoupling Topology. The principle of operation is also explained in details in this section. In addition, a table showing all states of operation as well as the status of the active switches and the passive components is provided.

The control strategy for the proposed topology is provided in section 4 of this research. This section starts with the control design of the GaN Totem-Pole PFC in the

analog and digital domains, and ends with the calculations and design of the control technique used to control the Active Power Decoupling circuit.

Section 5 demonstrates the design parameters of the Totem-Pole PFC with and without the H-Bridge Active Power Decoupling. System design ratings, active components selections, and passive components sizing for both topologies are provided in this section.

Section 6 comprises a detailed discussion and comparison of all simulation results for the Totem-Pole PFC without the H-Bridge ADP and the Totem-Pole PFC with the H-Bridge ADP. Moreover, this section consists of power loss calculations, simulation waveforms analysis and results of both topologies.
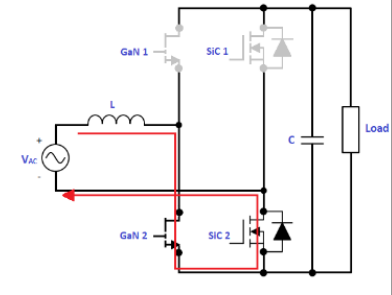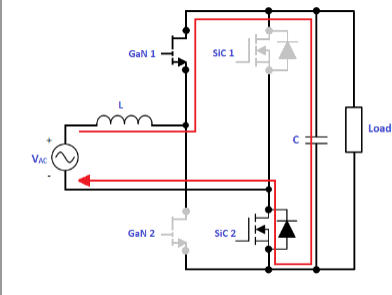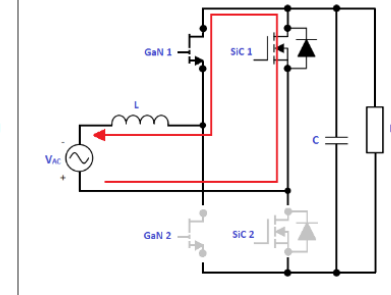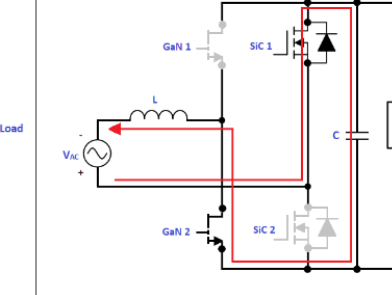
Section 7 shows the hardware design and prototype as well as the hardware experimental results for both topologies. This section also shows the selected hardware components and ratings.

Section 8 of this work contains a conclusion of the overall research results and analysis. Additionally, it consists of the future work that could be applied on the proposed topology for further enhancements.

## 2. TOTEM-POLE BRIDGELESS PFC PRINCIPLE OF OPERATION

The Totem-Pole PFC consists of four switches in total, two GaN FETs in the high frequency leg (100 kHz) and either two diodes or two MOSFETs placed on the low frequency leg. Consequently, it consists of four different states of operation, two in the Positive AC Half Cycle and two in the Negative AC Half Cycle. As illustrated in Table 2, at the positive AC half cycle and for the duration of the duty cycle (T=D), Gan1 and SiC1 will be OFF while GaN2 and SiC2 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. The second state works for a duration of (T= 1-D) at the positive AC half cycle. During this state, GaN2 and SiC1 will be OFF while GaN1 and SiC2 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. Similarly, at the negative AC half cycle and for the duration of the duty cycle (T=D), GaN2 and SiC2 will be OFF while GaN1 and SiC1 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. The fourth state works for a duration of (T= 1-D) at the negative AC half cycle. During this state, GaN1 and SiC2 will be OFF while GaN2 and SiC1 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. The simultaneous synchronous operation of these four states results in boosting and rectifying the sinusoidal input signal maintaining a Unity Power Factor.

Table 2. Totem-Pole Bridgeless PFC States of Operation

| | Positive AC Half Cycle T=D | Positive AC Half Cycle T=1-D | Negative AC Half Cycle T=D | Negative AC Half Cycle T=1-D |
|---|---|---|---|---|
| GaN1 | Synchronous Switch (OFF) | Synchronous Switch (ON) | Control Switch (ON) | Control Switch (OFF) |
| GaN2 | Control Switch (ON) | Control Switch (OFF) | Synchronous Switch (OFF) | Synchronous Switch (ON) |
| SiC1 | OFF | OFF | ON | ON |
| SiC2 | ON | ON | OFF | OFF |
| L | Charging | Discharging | Charging | Discharging |
| C | Discharging | Charging | Discharging | Charging |

## 3. PROPOSED GAN TOTEM-POLE BRIDGELESS PFC WITH AN H-BRIDGE APD

### 3.1 Topology
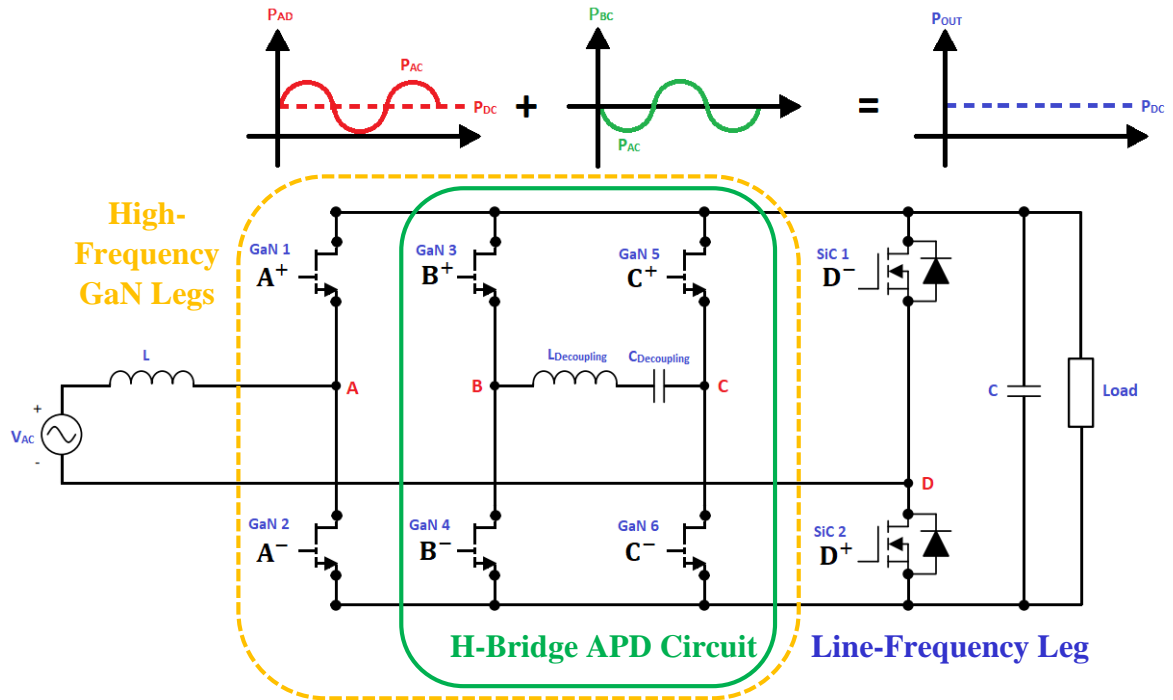


Figure 5. Proposed GaN Totem-Pole Bridgeless PFC with the H-Bridge APD Topology

The GaN Totem-Pole Bridgeless Power Factor Correction (PFC) with an additional H-Bridge Active Power Decoupling (APD) circuit and a simple yet reliable and efficient control topology similar to [18] is proposed in this section. As depicted in Figure 5, the topology contains three high switching frequency legs (100 kHz) and one low (line) frequency leg (60 Hz). The H-Bridge Active Power Decoupling circuit consists of two of the high switching frequency legs (100 kHz) with 4 GaN FET switches, a decoupling capacitor and an inductor. GaN FETs were used instead of MOSFETs due to their

superiorities in having higher switching frequency ensuring lower switching losses, higher efficiency leading to lower conduction losses, lower reverse recovery losses and higher power density. The additional H-Bridge APD circuit aims to cancel out the second order low frequency (120 Hz) harmonics without disturbing the Totem-Pole PFC operation. The additional H-Bridge APD circuit generates a reactive power that matches the undesirable power ripple generated by the Totem-Pole PFC resulting in an optimum DC Power with minimal distortion. The decoupling capacitor is only required to handle the AC voltage and consequently stores minimal energy which needs to match the circulating power ripple. Hence, this topology allows to replace the large aluminum electrolytic DC-link capacitors required to filter out the second order power harmonics with a much smaller polypropylene film capacitor. Film type capacitors have no leakage current, smaller tolerance, much less heat dissipation, and longer lifetime compared to the typical electrolytic capacitors. Furthermore, due to the high switching frequency of the four active switches used in the H-Bridge APD circuit, switching and conduction losses are low relatively. Moreover, using the suppressed DC-link film capacitor reduces the capacitance power loss dramatically. Thanks to the high effective switching frequency of the H-Bridge which allows minimizing the DC-Link filter size as well as the decoupling capacitor size.

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## 3.2 Principle of Operation

Table 3. Proposed GaN Totem-Pole Bridgeless PFC with H-Bridge APD Figures of

Positive AC Half Cycle States

| | States of Operation Figures |
|---|---|
| | **Positive AC Half Cycle T=D** |
| **State 1** |  |
| **State 2** |  |
| | **Positive AC Half Cycle T=1-D** |
| **State 3** |  |
| **State 4** |  |

Table 4. Proposed GaN Totem-Pole Bridgeless PFC with H-Bridge APD Figures of

Negative AC Half Cycle States

| States of Operation Figures | |
|---|---|
| | **Negative AC Half Cycle T=D** |
| **State 5** |  |
| **State 6** |  |
| | **Negative AC Half Cycle T=1-D** |
| **State 7** |  |
| **State 8** |  |

Table 5. Proposed GaN Totem-Pole PFC with H-Bridge APD States of Operation

| | States of Operation | | | |
|---|---|---|---|---|
| | **Positive AC Half Cycle T=D** | | **Positive AC Half Cycle T=1-D** | |
| | **State (1)** | **State (2)** | **State (3)** | **State (4)** |
| GaN1 | Synchronous Switch (OFF) | Synchronous Switch (OFF) | Synchronous Switch (ON) | Synchronous Switch (ON) |
| GaN2 | Control Switch (ON) | Control Switch (ON) | Control Switch (OFF) | Control Switch (OFF) |
| GaN3 | ON | OFF | ON | OFF |
| GaN4 | OFF | ON | OFF | ON |
| GaN5 | OFF | ON | OFF | ON |
| GaN6 | ON | OFF | ON | OFF |
| SiC1 | OFF | OFF | OFF | OFF |
| SiC2 | ON | ON | ON | ON |
| L | Charging | Charging | Discharging | Discharging |
| C | Discharging | Discharging | Charging | Charging |
| | **Negative AC Half Cycle T=D** | | **Negative AC Half Cycle T=1-D** | |
| | **State (5)** | **State (6)** | **State (7)** | **State (8)** |
| GaN1 | Control Switch (ON) | Control Switch (ON) | Control Switch (OFF) | Control Switch (OFF) |
| GaN2 | Synchronous Switch (OFF) | Synchronous Switch (OFF) | Synchronous Switch (ON) | Synchronous Switch (ON) |
| GaN3 | ON | OFF | ON | OFF |
| GaN4 | OFF | ON | OFF | ON |
| GaN5 | OFF | ON | OFF | ON |
| GaN6 | ON | OFF | ON | OFF |
| SiC1 | ON | ON | ON | ON |
| SiC2 | OFF | OFF | OFF | OFF |
| L | Charging | Charging | Discharging | Discharging |
| C | Discharging | Discharging | Charging | Charging |

The Proposed GaN Totem-Pole Bridgeless PFC with the H-Bridge APD consists of eight switches in total, six GaN FETs distributed on three high frequency legs (100 kHz) and two MOSFETs placed in the low frequency leg. Consequently, it consists of eight different states of operation, four in the Positive AC Half Cycle and four in the Negative AC Half Cycle. As illustrated in Tables 3, 4 and 5, at the positive AC half cycle and for the duration of the duty cycle (T=D), we have two states of operation, State (1) and State (2). At State (1), GaN1, GaN4, GaN5, and SiC1 will be OFF while GaN2, GaN3, GaN6 and SiC2 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. At State (2), GaN1, GaN3, GaN6, and SiC1 will be OFF while GaN2, GaN4, GaN5 and SiC2 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. State (3) and State (4) work for a duration of (T= 1-D) at the positive AC half cycle as well. At State (3), GaN2, GaN4, GaN5, and SiC1 will be OFF while GaN1, GaN3, GaN6 and SiC2 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. At State (4), GaN2, GaN3, GaN6, and SiC1 will be OFF while GaN1, GaN4, GaN5 and SiC2 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. Similarly, at the negative AC half cycle and for the duration of the duty cycle (T=D), there are two states of operation, State (5) and State (6). At State (5), GaN2, GaN4, GaN5, and SiC2 will be OFF while GaN1, GaN3, GaN6 and SiC1 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. At State (6), GaN2, GaN3, GaN6, and SiC2 will be OFF while GaN1, GaN4, GaN5 and SiC1 will be ON. At this state, the inductor (L) gets charged while the capacitor (C) gets discharged. State (7) and State (8) work for a duration of (T= 1-D) at the negative AC half cycle as well. At State (7), GaN1,

GaN4, GaN5, and SiC2 will be OFF while GaN2, GaN3, GaN6 and SiC1 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. At State (8), GaN1, GaN3, GaN6, and SiC2 will be OFF while GaN2, GaN4, GaN5 and SiC1 will be ON. At this state, the inductor (L) gets discharged while the capacitor (C) gets charged. The simultaneous synchronous operation of all eight states results in boosting and rectifying the sinusoidal input signal maintaining a Unity Power Factor with the cancelation of the second harmonic power ripple.

# 4. CONTROL STRATEGY FOR THE PROPOSED TOPOLOGY

## 4.1 GaN Totem-Pole Bridgeless PFC Control
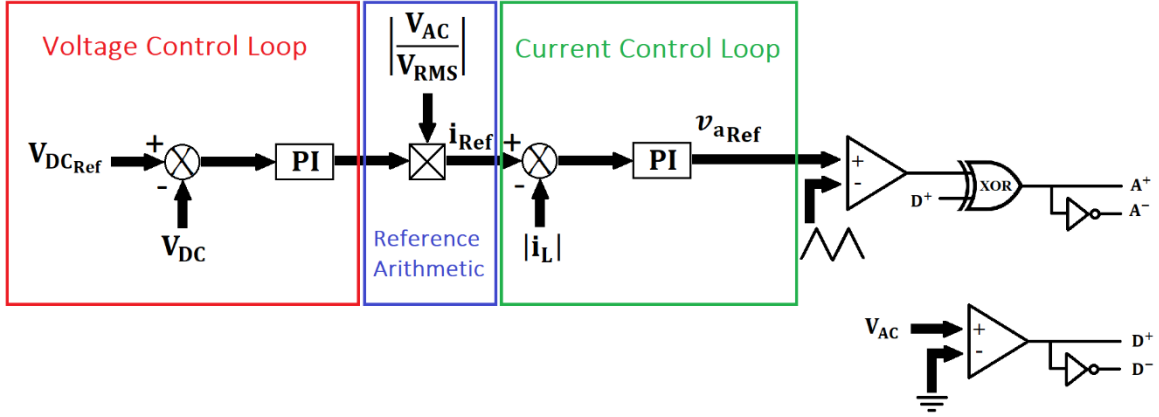


Figure 6. Proposed GaN Totem-Pole Bridgeless PFC Control Scheme

To simplify the control design, hard switching mode is adapted for the GaN Totem-Pole Bridgeless PFC Control. Figure 6 shows the Proposed GaN Totem-Pole Bridgeless PFC Control Scheme, where two PI controllers are used to control the high frequency leg (100 kHz) of the Totem-Pole PFC operation, one for the Inner (Current) Control Loop and one for the Outer (Voltage) Control Loop. The Control topology consists of three sensors, one input current sensor, one output voltage sensor, and one input voltage sensor. The input ac source voltage is sensed and divided by its RMS value to be used as a reference arithmetic for the inner current loop. An XOR Gate is placed at the output of the controller's comparator to make sure that the controller works in a similar manner for both the positive and negative cycles. As for the low frequency leg (60 Hz), a deadtime of 100 ns is introduced to avoid having an overlap between the AC Positive Half Cycle ($D^+$) and the AC Negative Half Cycle ($D^-$), which will eventually cause short circuit.

4.1.1   Analog Domain

This section comprises the design of the Totem-Pole PFC in the Analog domain. After building the Totem-Pole PFC circuit schematic on PSIM, it is set to run on an open loop control with a dc reference voltage and a dc voltage source. The dc reference is scaled from 0 to 1 and gets adjusted till we reach the desired output voltage (390V); it was chosen to be 0.415 in my case. The reference value gets compared with a sawtooth PWM signal with a frequency of 100 kHz through a comparator block. The output of the comparator block then goes to an XOR gate. The second input of the XOR gate is the positive cycle feedback that comes from another comparator that compares the ac source voltage signal with zero. The comparator's output is 1, when the cycle is positive and 0 when the cycle is negative. The positive and negative cycles signals are also used to operate the low (line) frequency MOSFETs. The lower MOSFET turns on during the positive cycle, while the upper one turns on during the negative cycle. Upon the completion of this step, an AC Sweep element is used along with an AC probe that is placed on the input current sensor. The AC Sweep start frequency is chosen to be 10 Hz, the end frequency is 70 kHz, the number of points is 100, the source peak amplitude should be 5-10% of the reference which turns out to be around 0.02075, the number of cycles is 1 and the steady state time of the output voltage and current is 0.08s. Two Bode Plots (Amplitude and Phase) are then generated for the Inner Loop (Current Loop) as shown in Figure 7. To choose the Inner Loop (Current Loop) PI controller parameters, the Bode Plots were exported to the SmartCtrl4.1 Tool. Now, to get a good power factor, the current loop should be able to track the 120 Hz rectified signal (60 Hz $\times$ 2). That is, the closed loop phase response should be close to 0 degrees at 120 Hz. By analyzing the Bode Plots in SmartCtrl,

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maintaining adequate phase margin (PM), cutoff frequency and attenuation ($f_c =$ 23.985 $kHz, PM =$ 57.754, Attenuation $= -15.7912$ dB) the optimum PI parameters were chosen to be ($K_p =$ 1.75934, $T_i(s) =$ 10.6057$\mu$) as shown in Figure 8. Therefore, the PI element is added to the schematic along with a limiter to limit the duty cycles to a sensible range (from 0 to 1).



Figure 7. Analog Domain Inner Loop (Current Loop) Bode Plot

Figure 8. Analog Domain Inner Loop (Current Loop) Controller's PI Parameters Design

Similarly, an AC Sweep element is used for the Outer loop (Voltage Loop) along with an AC probe that is placed on the output voltage sensor. The AC Sweep start frequency is chosen to be 1 Hz, the end frequency is 20 kHz, the number of points is 30, the source peak amplitude should be 5-10% of the reference (1 for the outer loop) which turns out to be around 0.1, the number of cycles is 1 and the steady state time of the output voltage and current is 0.15s. Two Bode Plots (Amplitude and Phase) are then generated for the Outer Loop (Voltage Loop) as shown in Figure 9. To choose the Outer Loop (Voltage Loop) PI controller parameters, the Bode Plots were exported to the SmartCtrl4.1 Tool. Now, to get a good power factor, the voltage loop should be able to attenuate the 120 Hz rectified signal (60 Hz $\times$ 2) with a low Phase Margin (PM). By analyzing the Bode Plots in SmartCtrl, maintaining adequate phase margin, cutoff frequency and attenuation ($f_c = 7.88236\ kHz, PM = 29.9465, \text{Attenuation} = -59.8824$ dB) the optimum PI

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parameters were chosen to be ($K_p = 395.314m, T_i(s) = 1.67593m$) as seen in Figure 10. So, the PI element is added to the schematic along with a limiter to limit the duty cycles to a sensible range (from 0 to 1). After adding both PI controllers and all relevant elements, the simulation was tested and output waveforms were analyzed. Simulation results and analysis are discussed in details in the Results section of this study.
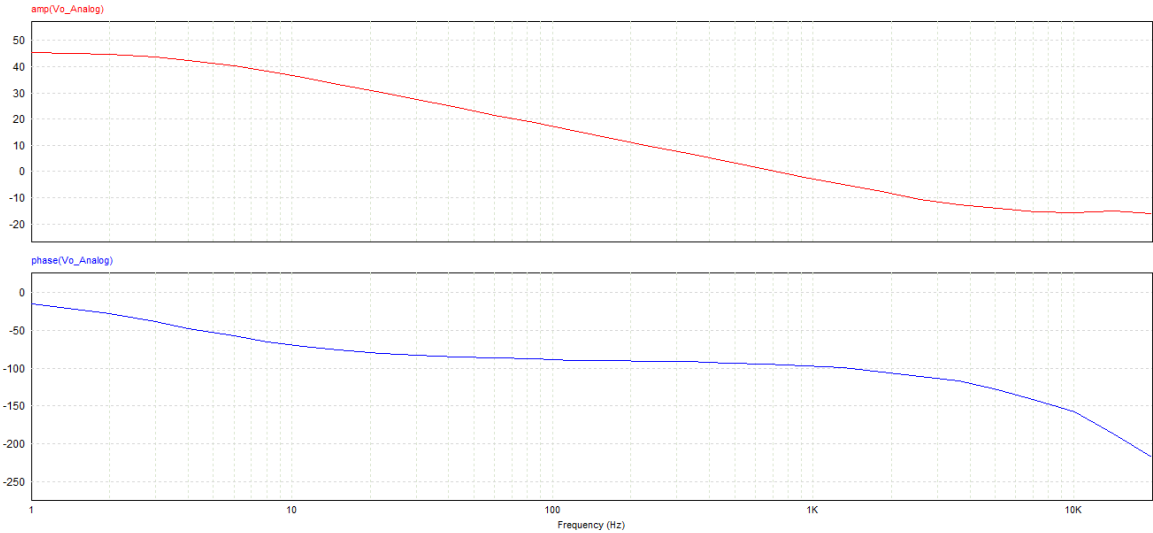


Figure 9. Analog Domain Outer Loop (Voltage Loop) Bode Plot
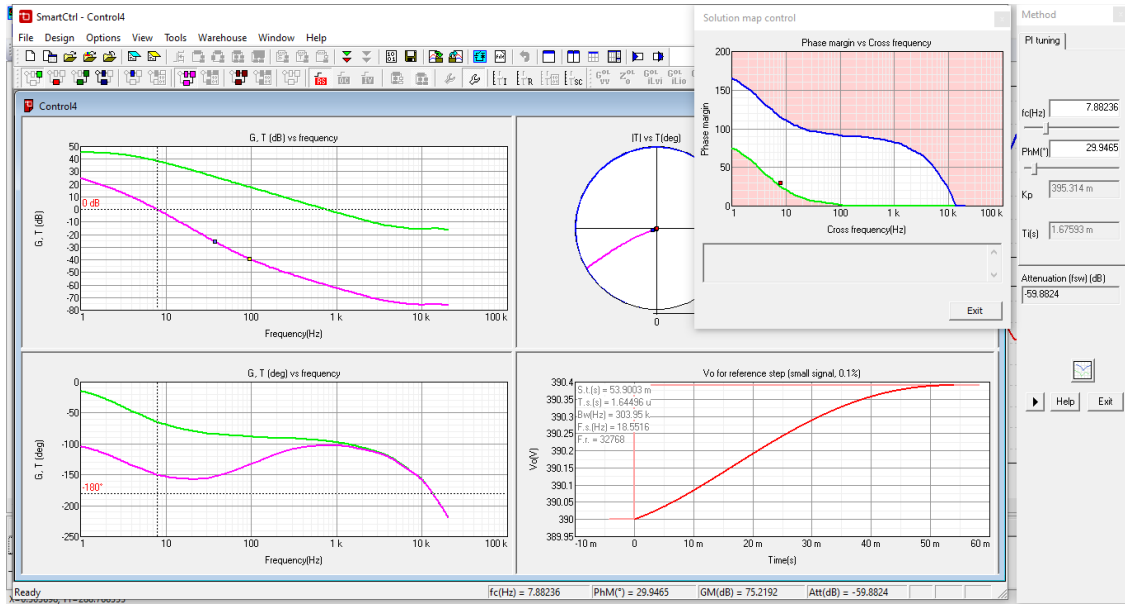
Figure 10. Analog Domain Outer Loop (Voltage Loop) Controller's PI Parameters Design

### 4.1.2    Digital Domain

This section comprises the design of the Totem-Pole PFC in the Digital domain. After building the Totem-Pole PFC circuit schematic on PSIM, a zero-order hold block with a sampling frequency of 100 kHz was added to the outputs of all voltage and current sensors. The simulation is set to run on an open loop control with a dc reference voltage and a dc voltage source. The dc reference is scaled from 0 to 1 and gets adjusted till we reach the desired output voltage (390V); it was chosen to be 0.416 in my case. The reference value first gets delayed by a delay block with a sampling frequency of 100 kHz and then gets compared with a sawtooth PWM signal with a frequency of 100 kHz through a comparator block. The output of the comparator block then goes to an XOR gate. The second input of the XOR gate is the positive cycle feedback that comes from another comparator that compares the ac source voltage signal with zero. The comparator's output

is 1, when the cycle is positive and 0 when the cycle is negative. The positive and negative cycles signals are also used to operate the low (line) frequency MOSFETs. The lower MOSFET turns on during the positive cycle, while the upper one turns on during the negative cycle. Upon the completion of this step, an AC Sweep element is used along with an AC probe that is placed on the input current sensor similar to the analog domain. The AC Sweep start frequency is chosen to be 1 Hz, the end frequency is 25 kHz, the number of points is 100, the source peak amplitude should be 5-10% of the reference which turns out to be around 0.0208, the number of cycles is 1 and the steady state time of the output voltage and current is 0.1s. Two Bode Plots (Amplitude and Phase) are then generated for the Inner Loop (Current Loop) as shown in Figure 11. To choose the Inner Loop (Current Loop) PI controller parameters, the Bode Plots were exported to the SmartCtrl4.1 Tool. Now, to get a good power factor, the current loop should be able to track the 120 Hz rectified signal (60 Hz × 2). That is, the closed loop phase response should be close to 0 degrees at 120 Hz. By analyzing the Bode Plots in SmartCtrl, maintaining adequate phase margin (PM), cutoff frequency and attenuation $(f_c = 7.50551\ kHz, PM = 11.2299, \text{Attenuation} = -25.0389$ dB) the optimum PI parameters were chosen to be $(K_p = 613.81m, T_i(s) = 46.2143\mu)$ as shown in Figure 12. Therefore, the PI element is added to the schematic. The digital version of the PI has its own limiter which is required to limit the duty cycles to a sensible range (from 0 to 1).
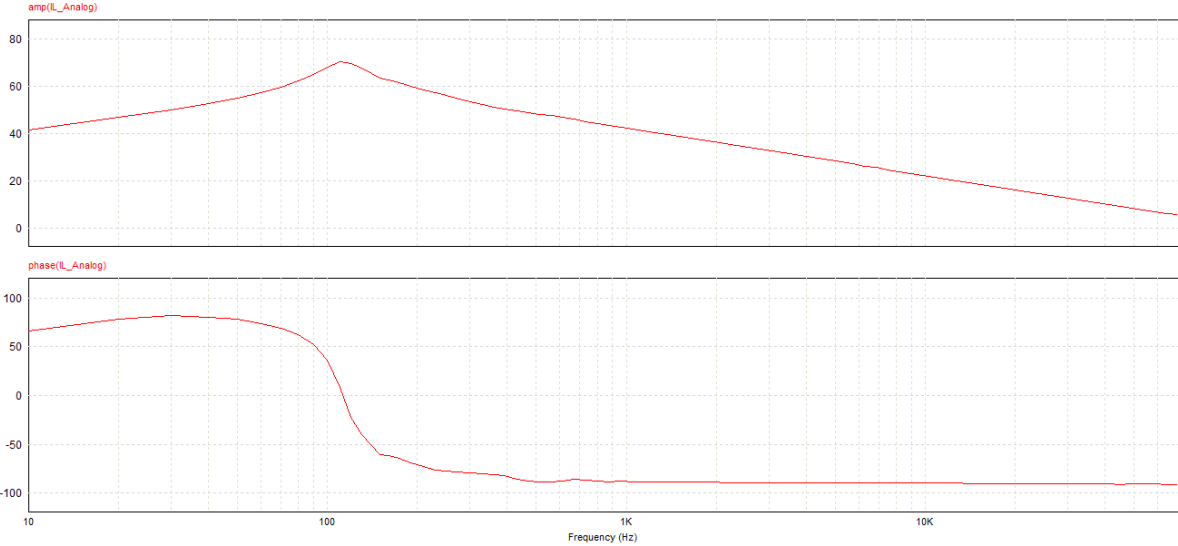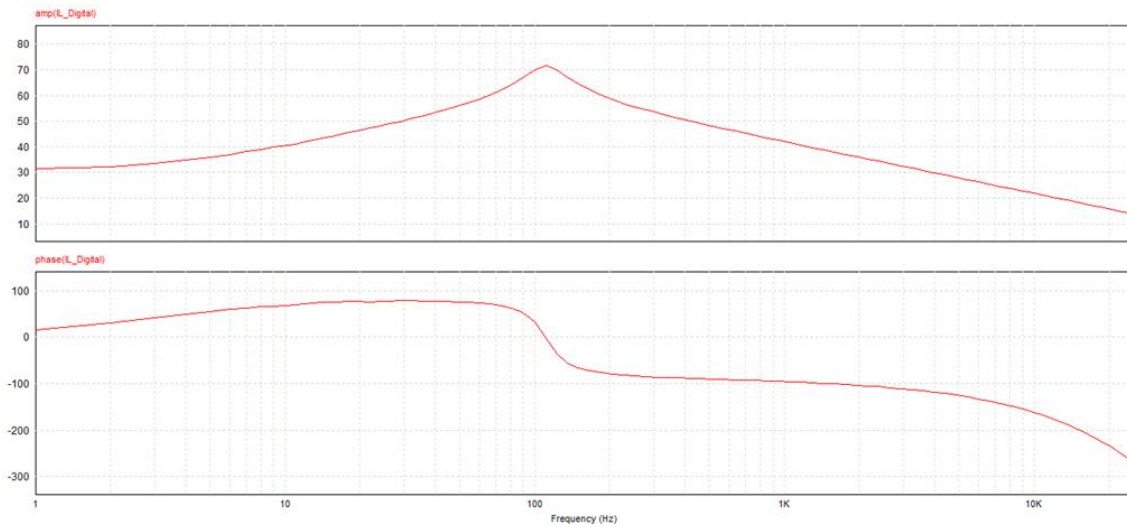
Figure 11. Digital Domain Inner Loop (Current Loop) Bode Plot



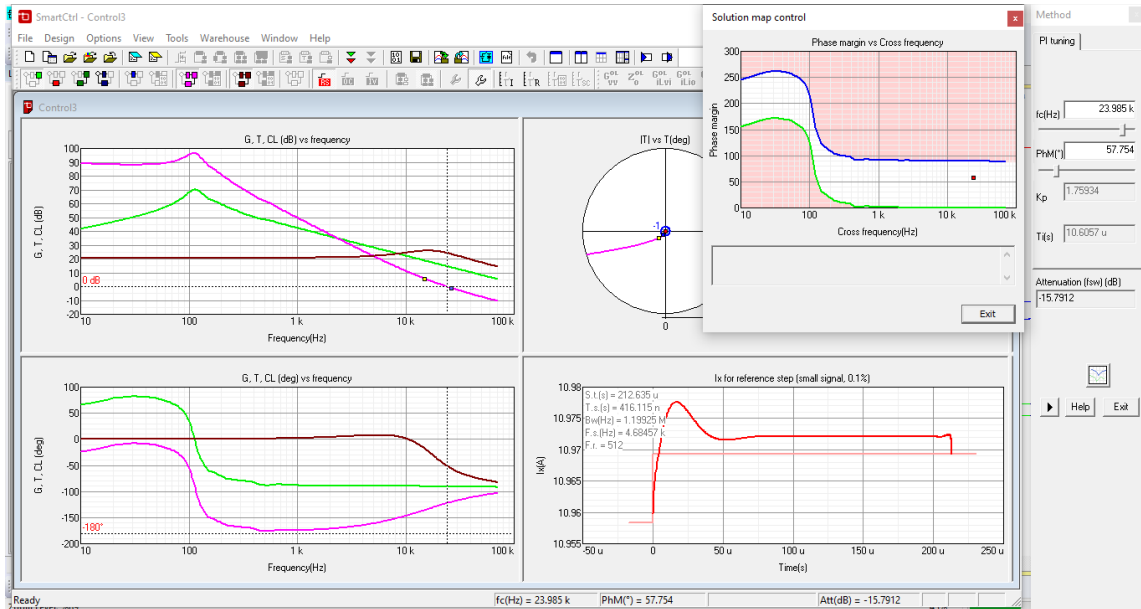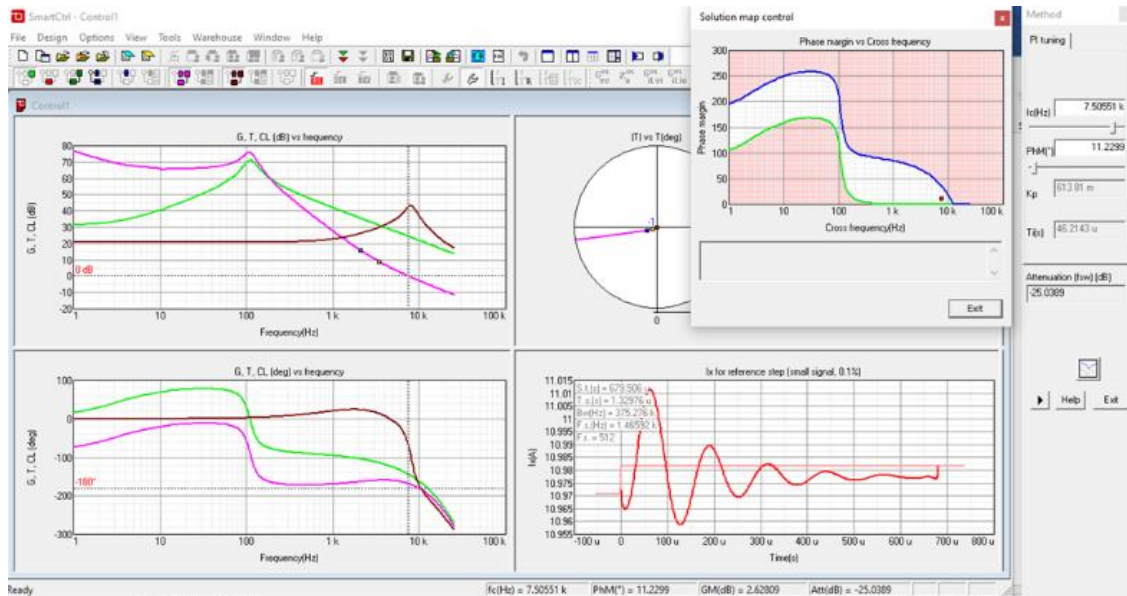Figure 12. Digital Domain Inner Loop (Current Loop) Controller's PI Parameters
Design

Correspondingly, an AC Sweep element is used for the Outer loop (Voltage Loop) along with an AC probe that is placed on the output voltage sensor. The AC Sweep start frequency is chosen to be 1 Hz, the end frequency is 15 kHz, the number of points is 100, the source peak amplitude should be 5-10% of the reference which turns out to be around 0.15, the number of cycles is 1 and the steady state time of the output voltage and current is 0.2s. Two Bode Plots (Amplitude and Phase) are then generated for the Outer Loop (Voltage Loop) as shown in Figure 13. To choose the Outer Loop (Voltage Loop) PI controller parameters, the Bode Plots were exported to the SmartCtrl4.1 Tool. Now, to get a good power factor, the voltage loop should be able to attenuate the 120 Hz rectified signal (60 Hz × 2) with a low Phase Margin (PM). By analyzing the Bode Plots in SmartCtrl, maintaining adequate phase margin, cutoff frequency and attenuation ($f_c =$ 27.7824 $kHz, PM =$ 18.1818, Attenuation $= -49.575$dB) the optimum PI parameters were chosen to be ($K_p =$ 1.29514, $T_i(s) =$ 738.913μ) as seen in Figure 14. So, the PI element is added to the schematic. The digital version of the PI has its own limiter which is required to limit the duty cycles to a sensible range (from 0 to 1). After adding both PI controllers and all relevant elements, the simulation was tested and output waveforms were analyzed. Simulation results and analysis are discussed in details in the Results section of this study.
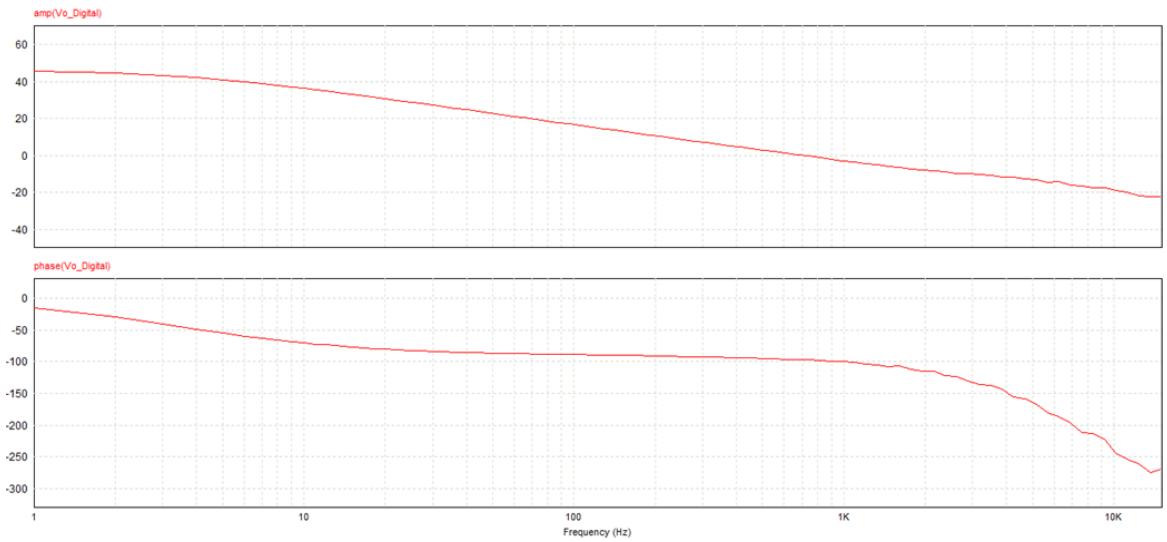
Figure 13. Digital Domain Outer Loop (Voltage Loop) Bode Plot
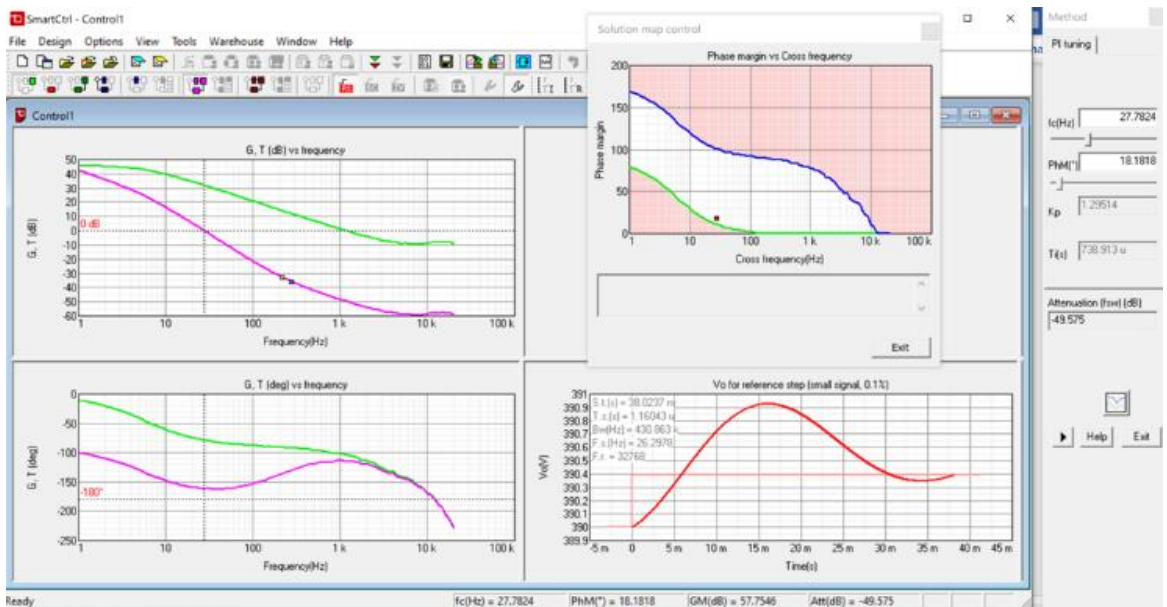


Figure 14. Digital Domain Outer Loop (Voltage Loop) Controller's PI Parameters Design

## 4.2 Proposed H-Bridge APD Control

This section analyzes and investigates the voltage, current and power equations used to derive the required ripple port control references and accordingly generate the PWM gate signals that controls the high frequency active switches. Considering the source voltage $v_{ad}$ to be our reference phase angle

$$v_{ad} = V_{ad,peak} \sin(\omega t) \tag{1}$$

Due to the unity power factor achievement generated by the Totem-Pole PFC, the inductor current $i_L$ and source voltage $v_{ad}$ will be in phase ($i.e\ \theta = 0$), thus the inductor current can be represented by

$$i_L = I_{L,peak} \sin(\omega t) \tag{2}$$

And the input power $P_{ad}(t)$ is

$$P_{ad}(t) = \frac{V_{ad,peak}\ I_{L,peak}}{2} (\cos(0) - \cos(2\omega t)) \tag{3}$$

Knowing that cos (0) is 1, we get the following expression

$$P_{ad}(t) = \frac{V_{ad,peak}\ I_{L,peak}}{2} (1 - \cos(2\omega t)) \tag{4}$$

Thus, the input power $P_{ad}(t)$ consists of a DC part and an AC part as following

$$P_{ad}(t) = P_{ad\,DC} + P_{ad\,AC} \tag{5}$$

It can be clearly seen from (4) and (5) that $P_{ad\,DC}$ is the DC power of $P_{ad}(t)$

$$P_{ad\,DC} = \frac{V_{ab,peak}\ I_{L,peak}}{2} \tag{6}$$

and $P_{ad\,AC}$ is the AC second order harmonic power of $P_{ad}(t)$

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$$P_{ad}(t) = -\frac{V_{ad,peak} I_{L,peak}}{2} \cos(2\omega t) \qquad (7)$$

Similarly, for the H-Bridge Active Power Decoupling circuit, the voltage between leg B and C as shown in Figure 5 of section 3.1 is as following

$$v_{bc} = V_{bc,peak} \sin(\omega t + \theta_1) \qquad (8)$$

And the current passing through the decoupling filter is

$$i_{L_d} = I_{L_d,peak} \sin(\omega t + \theta_2) \qquad (9)$$

Resulting in a decoupling power $P_{bc}(t)$ of

$$P_{bc}(t) = \frac{V_{bc,peak} I_{L_d,peak}}{2} (\cos(\theta_1 - \theta_2) - \cos(2\omega t + \theta_1 + \theta_2)) \qquad (10)$$

At high switching frequency (100 kHz), the impedance ( $j\omega L_{decoupling}$ ) becomes negligible in comparison with the impedance of the decoupling capacitor ($\frac{1}{j\omega C_{decoupling}}$) [18]. Therefore, the following approximations could be made

$$\theta_2 \cong \theta_1 + \frac{\pi}{2} \qquad (11)$$

$$I_{L_d,peak} \cong \omega \, C_{decoupling} \, V_{bc,peak} \qquad (12)$$

Applying (11) and (12) on (10), $P_{bc}$ will be reduced to

$$P_{bc}(t) = -\frac{V_{bc,peak}^2 \, \omega \, C_{decoupling}}{2} \cos(2\omega t + 2\theta_1 + \frac{\pi}{2}) \qquad (13)$$

Therefore, the H-Bridge APD controller should adjust ($v_{bc}$) to generate a reactive power $P_{bc}(t)$ that matches the undesirable power ripple generated by the Totem-Pole PFC ($P_{ad_{AC}}$).

Thus, by matching (13) with (7), we get the following

$$\frac{V_{bc,peak}^2 \, \omega \, c_{decoupling}}{2} \cos\left(2\omega t + 2\theta_1 + \frac{\pi}{2}\right) \approx \frac{V_{ad,peak} \, I_{L,peak}}{2} \cos(2\omega t) \qquad (14)$$

By comparing the magnitudes and phase angles in (14), we can reach the following

conclusion

$$V_{bc,peak} \approx \sqrt{\frac{V_{ad,peak} \, I_{L,peak}}{\omega \, c_{decoupling}}} \qquad (15)$$

$$\theta_1 \approx -\frac{\pi}{4} \qquad (16)$$
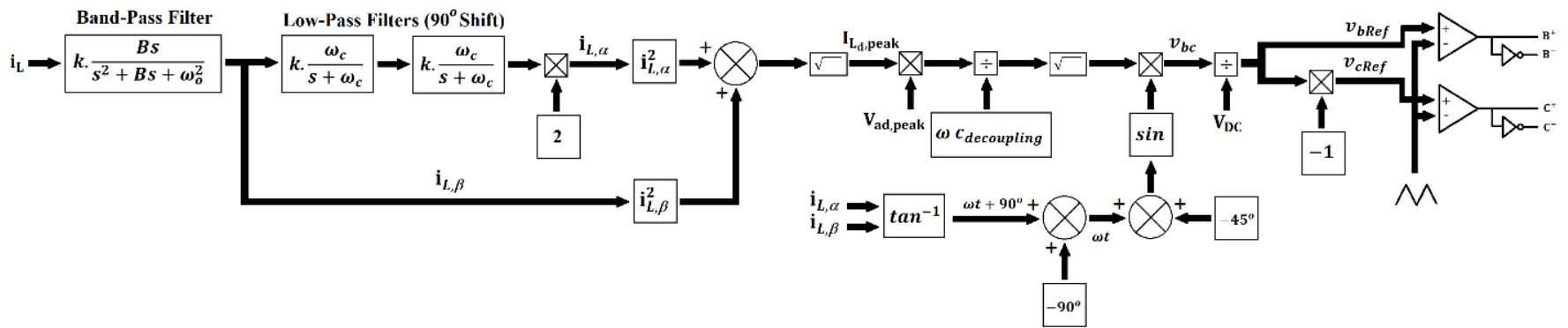
Figure 15. Proposed H-Bridge APD Control Scheme

Figure 15 shows the proposed simple H-Bridge APD control scheme. The proposed methodology requires only one current sensor. Similar to [18] $i_L$ is passed first through a 2nd order Band-Pass-Filter to prevent unwanted harmonics or any possible dc drift and smoothen possible sudden variations in load current. This filter has the following parameters:

Gain

$$k = 1 \qquad (17)$$

Center Frequency

$$f_o = \frac{\omega_o}{2\pi} = 60 \; Hz \qquad (18)$$

Frequency width $f_b$ of the passing band

$$f_b = \frac{B}{2\pi} = 30 \; Hz \qquad (19)$$

The transfer function $G(s)$ is

$$k.\frac{Bs}{s^2 + Bs + \omega_o^2} \qquad (20)$$

The output then is passed through two 1st order Low-Pass-Filters and multiplied by a gain of 2 (to scale back the magnitude to its original value) to generate two orthogonal current components ($i_{L,\alpha}$ and $i_{L,\beta}$ ) which will be used in calculating the magnitude of the current ($I_{L,peak}$) as well as the periodic frequency angle ($\omega t$). The orthogonal current components ($i_{L,\alpha}$ and $i_{L,\beta}$ ) are inserted into a ($\tan^{-1}$) block that outputs the periodic frequency angle ($\omega t$) plus a 90° phase shift caused by the two 1st order Low-Pass-Filters. Thus, a negative offset of 90° is summed to the output of the ($\tan^{-1}$) element to produce the periodic frequency angle ($\omega t$).  The two 1st order Low-Pass-Filters have the following parameters:

Gain

$$k = 1 \tag{21}$$

Cut-Off Frequency

$$f_c = \frac{\omega_c}{2\pi} = 60 \; Hz \tag{22}$$

($\omega t$) is then subtracted by 45° (from equation 16) to generate a sine function that is multiplied by the square-root of the product of the magnitude of the inductor's current ($I_{L_d,peak}$) and the magnitude of the source voltage ($V_{ad,peak}$) divided by the product of the frequency ($\omega$) and the decoupling capacitor as seen in equation 15. Afterward, the voltage reference $v_{bc}$ is generated and gets divided by the output voltage to get scaled and vary in a range of (-1 to 1). This sine wave voltage reference is then used by one comparator with a PWM signal that has the same range of (-1 to 1) and its inverse is used by another identical comparator to generate the active switching gate signals and control the H-Bridge Active Power Decoupling circuit.

Figure 16 below shows the full Control System Overview for the proposed GaN Totem-Pole Bridgeless PFC with the H-Bridge APD. It is clearly noticed that we have only two PI controllers, three sensors (two voltage sensors and one current sensor), three filters (one Band-Pass Filter and two Low-Pass Filters) in the entire control scheme.

Figure 16. Full Control System Overview for the Proposed GaN Totem-Pole Bridgeless PFC with the H-Bridge APD

5.   DESIGN PARAMETERS


This section demonstrates the design parameters of both topologies, the Totem-Pole PFC with and without the H-Bridge Active Power Decoupling. System design ratings are chosen to be the same for both topologies in order to make a rational comparison between the systems. Likewise, active components are selected to have the same specifications and design for both concepts. However, passive components are sized differently due to the fact that they are the main comparison factors.

**5.1 Totem-Pole PFC Design Parameters**

The design parameters subsection includes the system design ratings of the studied case, the active components selection and the passive components sizing.

5.1.1   System Design Ratings

The studied case has system design ratings that are chosen to have reasonable values. The system's frequency is selected to be 60 Hz, the PWM switching frequency is 100 kHz, the AC grid voltage is chosen to be 230 V (RMS). The input voltage is boosted up to deliver an output DC bus voltage of 390 V. Table 6 shows the selected system design ratings:

Table 6. Totem-Pole Bridgeless PFC System Design Ratings

| Input/output specifications | Unit | Totem-Pole PFC |
|:---:|:---:|:---:|
| Grid Frequency | Hz | 60 |
| PWM Switching Frequency | Hz | 100k |
| AC Grid Voltage (rms) | V | 230 |
| DC Bus Voltage | V | 390 |
| Output Power (Pout) | W | 2500 |

### 5.1.2  Active Components Selection

Two fast switching GaN FETs are chosen to be used for the high frequency (100 kHz) switching leg of the Totem-Pole PFC and two MOSFETs are chosen to perform the low frequency (60 Hz) switching of the system. Although diodes can be used instead of MOSFETs, yet to achieve a better performance and lower losses, MOSFETs are selected. The GaN switches are controlled by the PI controllers, while the MOSFETs are controlled by the positive and negative cycles of the operation.

### 5.1.3  Passive Components Sizing

Assuming a maximum inductor current ripple factor ($RF_c$) of 20%, an inductor current peak ($I_{L,peak}$) around 15.6 A, an output DC voltage ($V_{dc}$) of 390 V, and a switching frequency ($f_s$) of 100 kHz, the input side inductor is sized as following:

$$L = \frac{V_d}{4.f_s.RF_c.I_{L,peak}} = \frac{390}{4*100k*0.2*15.6} = 312.5\mu H \qquad (23)$$

Therefore, with an addition of 1.5 safety margin the inductor is selected to be 480 $\mu$H. As for the required DC-link capacitance, assume that $\Delta V_{dc} = 4.5V$, it can be calculated with the following equation:

$$C = \frac{P_o}{2.\,\omega.\,\Delta V_{dc}.\,V_{dc}} = \frac{2500}{2.\,(2.\,\pi.\,60).\,(4.5).\,(390)} = 1.88\ mF \tag{24}$$

Table 7 below shows the input inductor and DC-link capacitor's values for the Totem-Pole PFC.

Table 7. Input inductor and DC-link capacitor sizing

| Design Parameters | Unit | Totem-Pole PFC |
|---|---|---|
| Input Inductance (L) | H | $480\mu$ |
| DC-Link Capacitance (C) | F | 1.88m |

## 5.2 H-Bridge APD Design Parameters

The design parameters subsection includes the system design ratings of the studied case, the active components selection and the passive components sizing.

### 5.2.1   System Design Ratings

The proposed topology has the same system design ratings chosen for the Totem-Pole PFC without the ADP, in order to have a reasonable comparison. The system's frequency is selected to be 60 Hz, the PWM switching frequency is 100 kHz, the AC grid voltage is chosen to be 230 V (RMS). The input voltage is boosted up to deliver an output DC bus voltage of 390 V. Table 8 shows the selected system design ratings:

Table 8. Totem-Pole Bridgeless PFC with the H-Bridge ADP System Design Ratings

| Input/output specifications | Unit | Totem-Pole PFC |
|:---:|:---:|:---:|
| Grid Frequency | Hz | 60 |
| PWM Switching Frequency | Hz | 100k |
| AC Grid Voltage (rms) | V | 230 |
| DC Bus Voltage | V | 390 |
| Output Power (Pout) | W | 2500 |

5.2.2   Active Components Selection

Six fast switching GaN FETs are chosen to be used for the high frequency (100 kHz) switching legs of the Totem-Pole PFC with the H-Bridge ADP and two MOSFETs are chosen to perform the low frequency (60 Hz) switching of the system. Although diodes can be used instead of MOSFETs, yet to achieve a better performance and lower losses, MOSFETs are selected. Two GaN switches are controlled by the PI controllers, and the other four GaN switches are controlled by the additional ADC control, while the MOSFETs are controlled by the positive and negative cycles of the operation.

5.2.3   Passive Components Sizing

Similar to the Totem-Pole PFC without the H-Bridge APD, assuming a maximum inductor current ripple factor ($RF_c$) of 20%, an inductor current peak ($I_{L,peak}$) of around 15.6 A, an output DC voltage ($V_{dc}$) of 390 V, and a switching frequency ($f_s$) of 100 kHz, the input side inductor is sized as following:

$$L = \frac{V_d}{4.f_s.RF_c.I_{L,peak}} = \frac{390}{4*100k*0.2*15.6} = 312.5\mu H \tag{25}$$

Therefore, with an addition of 1.5 safety margin, the inductor is selected to be 480 $\mu$H. As for the required DC-link capacitance, the topology is tested to work perfectly with a suppressed capacitance that could go down to 5$\mu$F.

As for the decoupling passive elements, considering a maximum current ripple factor of 20% of $I_{L,peak}$, the required APD inductance is calculated as:

$$L_{decoupling} = \frac{V_d}{8.f_s.RF_c.I_{L,peak}} = \frac{390}{8*100k*0.2*15.6} = 156.25\mu H \tag{26}$$

Considering

$$V_{bc,peak} = 366.875\ V \tag{27}$$

$$C_{decoupling} \approx \frac{V_{ad,peak}\ I_{L,peak}}{V_{bc,peak}^2 \omega} \approx \frac{(230*\sqrt{2})(15.6)}{(366.875)^2(2\pi60)} \approx 100\mu F \tag{28}$$

Table 9 below shows the input inductor, DC-link capacitor, decoupling inductor and decoupling capacitor's values:

Table 9. Input inductor, DC-link capacitor, decoupling inductor and decoupling capacitor sizing

| Design Parameters | Unit | Totem-Pole PFC |
|---|---|---|
| Input Inductance (L) | H | 480$\mu$ |
| DC-Link Capacitance (C) | F | 5$\mu$ |
| Decoupling Inductor (L$_{decoupling}$) | H | 156.25$\mu$ |
| Decoupling Capacitor (C$_{decoupling}$) | F | 100$\mu$ |

# 6.   SIMULATION RESULTS

All simulation results of the Totem-Pole PFC without the H-Bridge ADP and the Totem-Pole PFC with the H-Bridge ADP are shown and discussed in this section.

## 6.1 Totem-Pole PFC without the H-Bridge APD

This subsection consists of power loss calculations, simulation analysis and results of the Totem-Pole PFC without the H-Bridge ADP.

### 6.1.1   Power Loss Analysis

Two methods were used to find the power losses of the Totem-Pole PFC without the additional H-Bridge APD, by measurement and by calculation.

Firstly, PSIM simulation was used to measure the power losses of the active switches (GaNs and MOSFETs) and the inductors by replacing the ordinary modules with thermal ones. Thermal modules allow to monitor the GaNs/MOSFETs/Inductors thermal conditions and accordingly measure the switching and conduction losses for the switching devices and core and winding losses for the inductors. Thermal module switching devices have one additional node, as seen in Figure 17. The voltage measured at this node represents the case temperature of the device $T_c$ in °C. Therefore, assuming that the ambient temperature is 25 °C, a DC voltage source of 25V was connected to the node as seen in Figure 19 which depicts the thermal equivalent circuit used for each high/low frequency switching leg. The current flowing out of the node represents the heat power flow out of the device which equals the total power losses in the component (in watts). Thus, to measure and display the switching device power losses, an ammeter is connected between the nodes and the ground. The current depends on the component's temperature,

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the ambient temperature and the thermal equivalent circuit of the component. Figure 20 below shows the conduction (2.042W) and switching (5.342W) losses of GaN1, Figure 21 shows the conduction (2.062W) and switching (5.390W) losses of GaN2, Figure 22 shows the conduction (3.158W) and switching losses of MOSFET1, and Figure 23 shows the conduction (3.126W) and switching (8.130W) losses of MOSFET2. Table 10 below contains the breakdown of the conduction and switching losses for the high and low (line) frequency switching leg components. Likewise, the thermal module inductor has two additional nodes, as shown in Figure 18. The current flowing out of the node with a dot represents the core losses of the inductor (0.0631W), while the current flowing out of the other node represents the winding losses (39.4W) as shown in Figure 24. By summing these two power losses, we find the total power losses of the inductor (39.463W). Consequently, to measure and display the losses, an ammeter is connected between the nodes and the ground. To estimate the power losses for the AC side (input) inductor, five series connected $100\mu H$ thermal inductors were used in the simulation. Table 11 below consists the breakdown of the core and winding losses of the equivalent inductor.
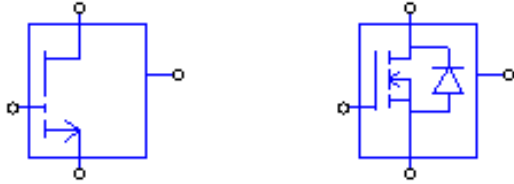


Figure 17. Thermal Module GaN and Thermal Module MOSFET
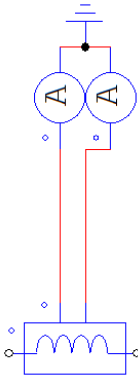


Figure 18. Thermal Module Inductor

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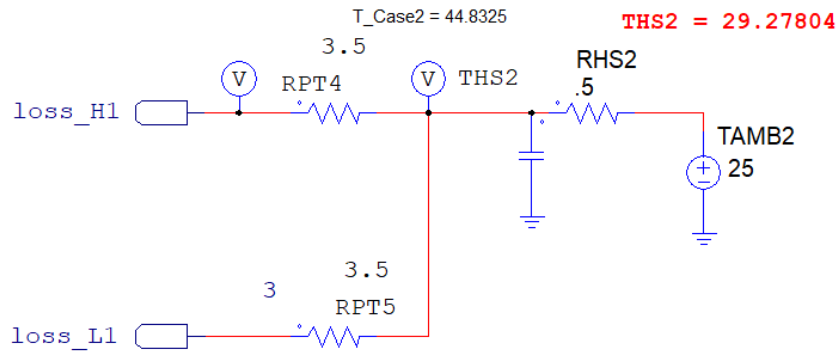
Figure 19. Thermal Equivalent Circuit for High/Low Frequency Switching Legs
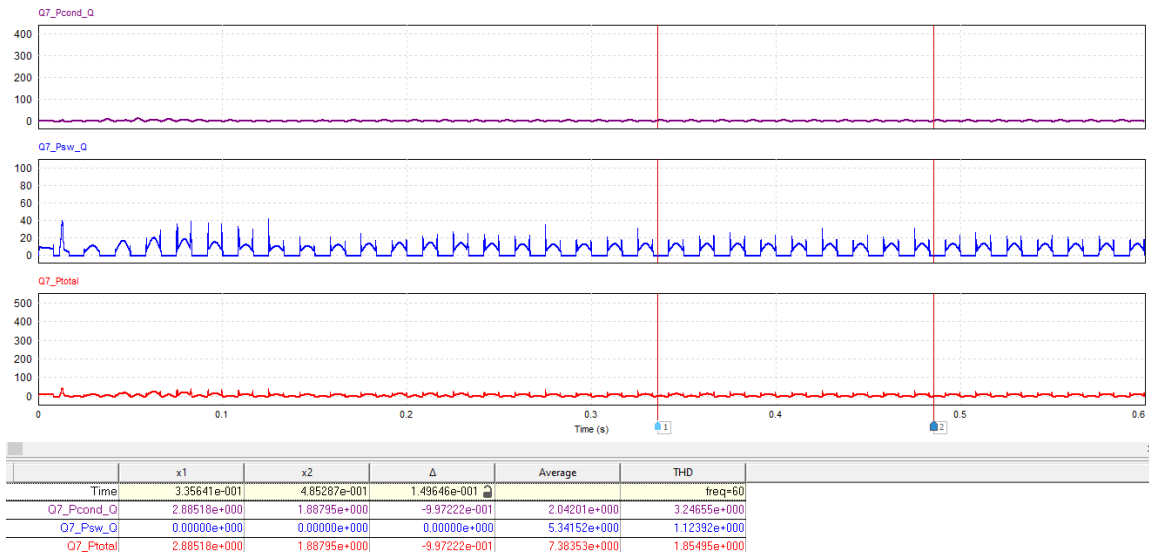


Figure 20. Conduction and Switching Losses for GaN1
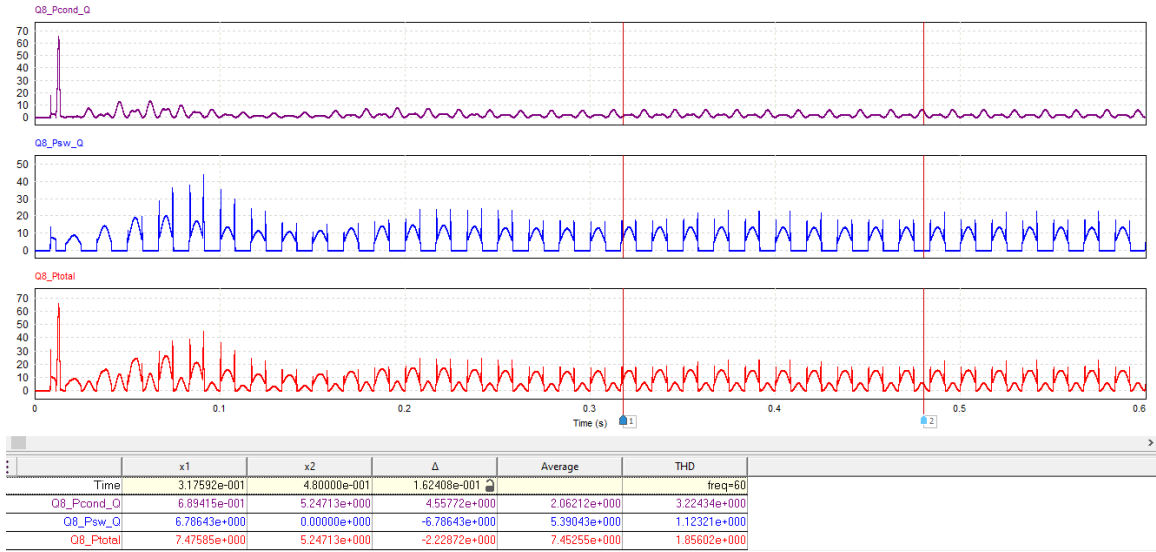
Figure 21. Conduction and Switching Losses for GaN2

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 3.17592e-001 | 4.80000e-001 | 1.62408e-001 | | freq=60 |
| Q8_Pcond_Q | 6.89415e-001 | 5.24713e+000 | 4.55772e+000 | 2.06212e+000 | 3.22434e+000 |
| Q8_Psw_Q | 6.78643e+000 | 0.00000e+000 | -6.78643e+000 | 5.39043e+000 | 1.12321e+000 |
| Q8_Ptotal | 7.47585e+000 | 5.24713e+000 | -2.22872e+000 | 7.45255e+000 | 1.85602e+000 |
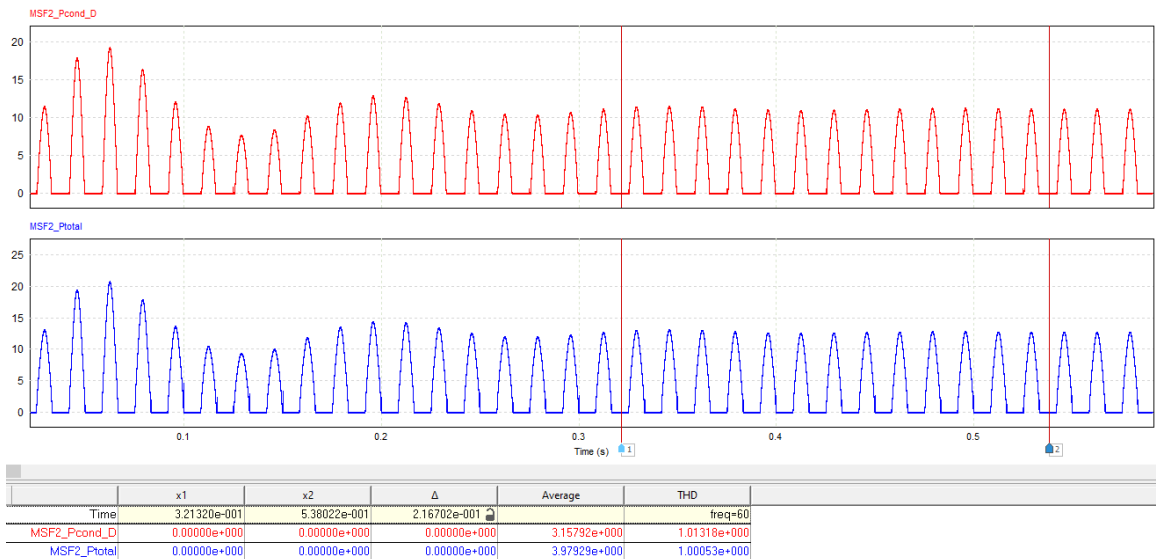


Figure 22. Conduction and Switching Losses for MOSFET1

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 3.21320e-001 | 5.38022e-001 | 2.16702e-001 | | freq=60 |
| MSF2_Pcond_D | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.15792e+000 | 1.01318e+000 |
| MSF2_Ptotal | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.97929e+000 | 1.00053e+000 |

44
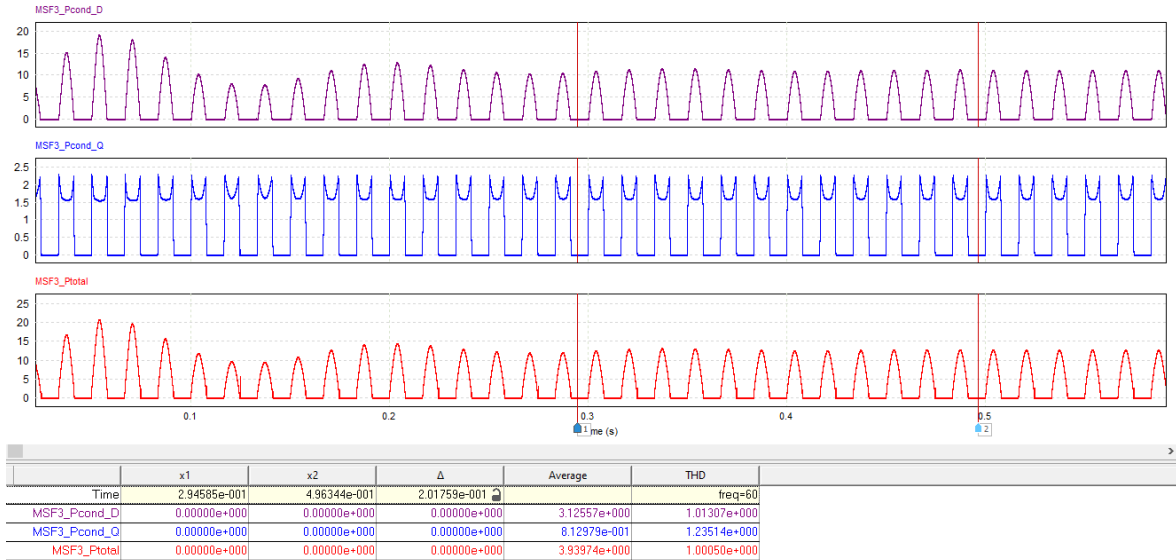
Figure 23. Conduction and Switching Losses for MOSFET2

Table 10. Conduction and Switching Losses for Active Switches

| Switches | Conduction Losses (W) | Switching Losses (W) | Total Losses (W) |
|---|---|---|---|
| GaN1 | 2.042 | 5.342 | 7.384 |
| GaN2 | 2.062 | 5.390 | 7.453 |
| SiC1 | 3.158 | - | 3.979 |
| SiC2 | 3.126 | 8.130 | 3.940 |
| Total Losses (W) | 10.388 | 18.862 | 22.756 |
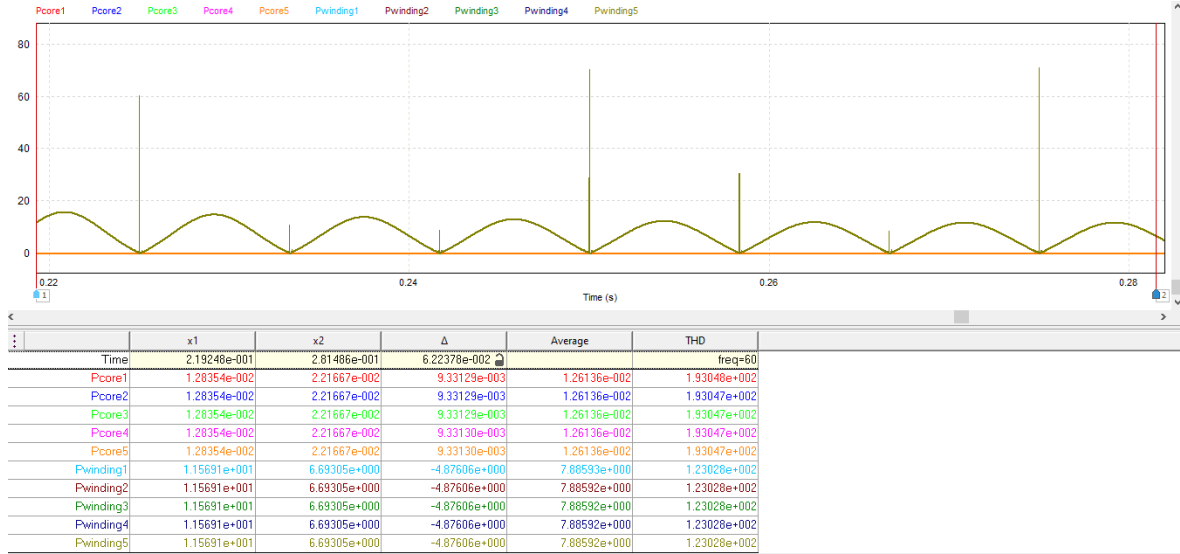
Figure 24. AC Side Inductor Core and Winding Losses

Table 11. Core and Winding Losses for the Input Inductor

| Components | Core Losses (W) | Wining Losses (W) | Total Losses (W) |
|---|---|---|---|
| Input Inductor | 0.0631 | 39.4 | 39.463 |

Secondly, power losses calculation and interpretation for the DC-link capacitor was estimated with a simple mathematical operation. By multiplying the Equivalent Series Resistance (ESR) of the capacitor with the root mean square (RMS) value of the capacitor's current squared, the capacitor's power dissipation is determined. The tested ESR value of Totem-Pole PFC DC-Link capacitor is specified in the datasheet to be 155mΩ for each capacitor [19]. A total number of four $470\mu F$ aluminum electrolytic capacitors were used. Thus, the total capacitor power loss can be calculated as following:

$$P_{loss} = 4 \times ESR \times I_{RMS}^2 = 4 \times 155 \times 10^{-3} \times 6.408^2 = 25.46\,W \tag{29}$$

The total power loss shown in Table 12 below is used in calculating the overall converter's efficiency as seen in the results section.

Table 12. Total Power Losses for the Totem-Pole PFC without the APD

| Components | Total Power losses (W) |
|---|---|
| Active Switches | 22.756 |
| Inductor | 39.463 |
| DC-link Capacitor | 25.46 |
| Total Power Losses (W) | 87.679 |

6.1.2   Simulation Waveforms

This subsection consists of all simulation outputs related to the Totem-Pole PFC without the H-Bridge APD. The circuit is built, simulated, tested, and analyzed using PSIM simulation. The simulation waveforms depicted below include the input voltage, input current, output voltage, output current, input apparent power, the power factor, and the Fast Fourier Transform (FFT) Analysis. Figure 25 below shows the input (AC) voltage source waveform and the scaled ($\times$ 10) input (AC) current waveform. It is clearly noticed that the input voltage and input current are in phase and a unity power factor is achieved as seen in Figure 26.
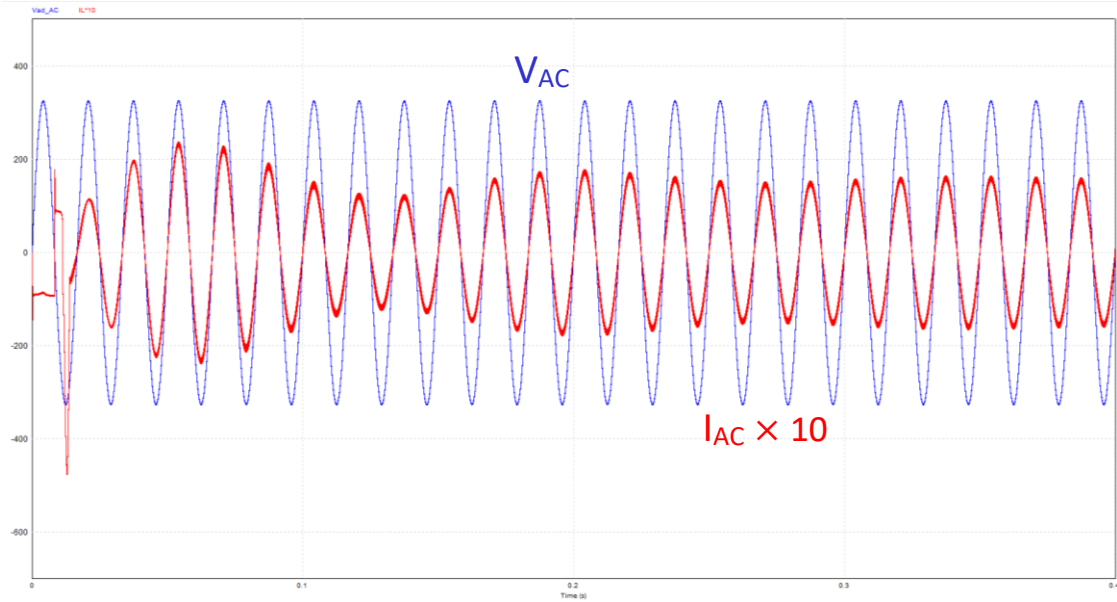
Figure 25. Input (AC) Voltage Source Waveform (in Blue) and Input (AC) Current Waveform (in Red)
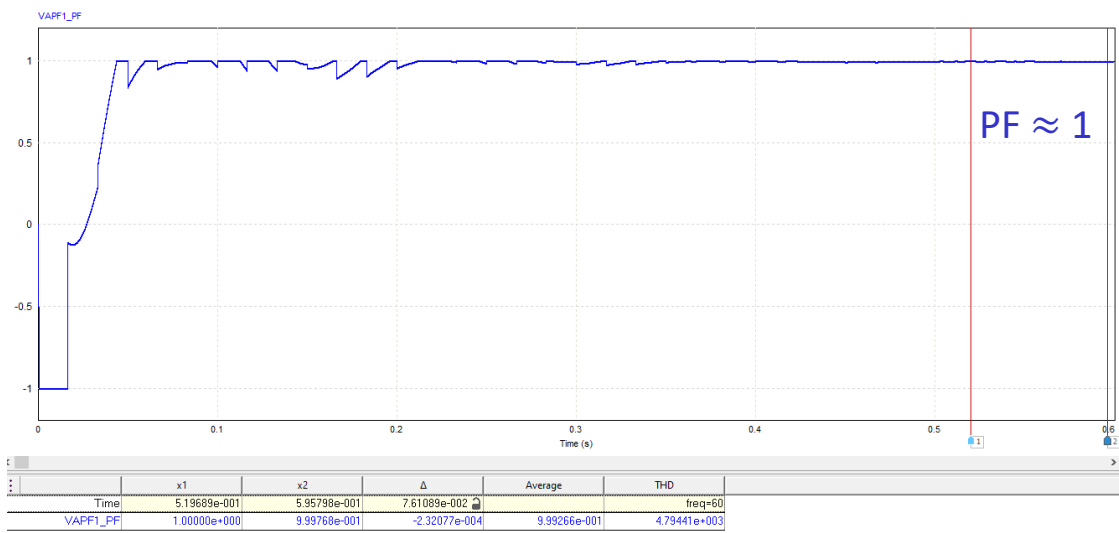


Figure 26. Achieved Unity Power Factor

Figure 27 (a) shows a perfect sinusoidal input current, Figure 27 (b) shows the rippled DC output current, Figure 27 (c) shows the rippled DC output voltage. It can be clearly seen that a stable AC/DC conversion is achieved.
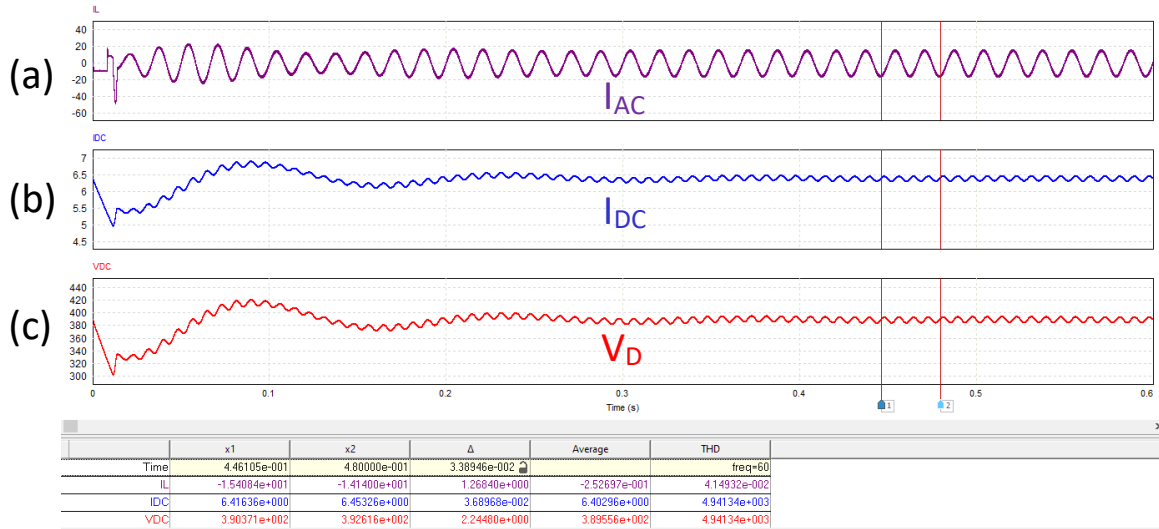


Figure 27. (a) AC Input Current (b) DC Output Current (c) DC Output Voltage

Figure 28 below shows a zoomed view of the DC output voltage ripple, where ΔV is clearly seen to have a value of 9.196V
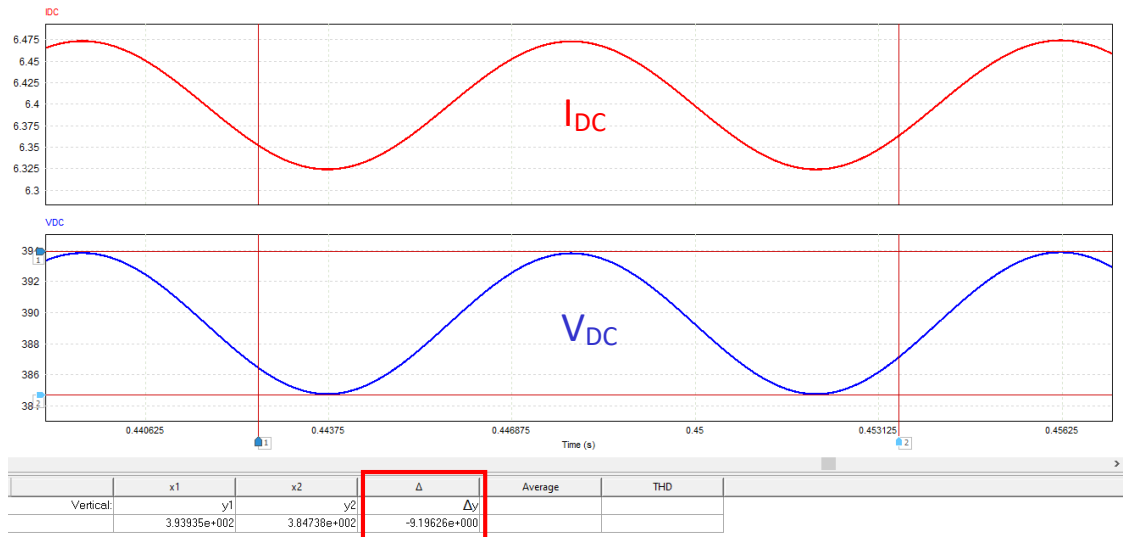


Figure 28. Close-up view of the DC Output Voltage Ripple

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Similarly, Figure 29 shows a zoomed view of the DC output current ripple, where ΔI is clearly seen to have a value of 0.153A
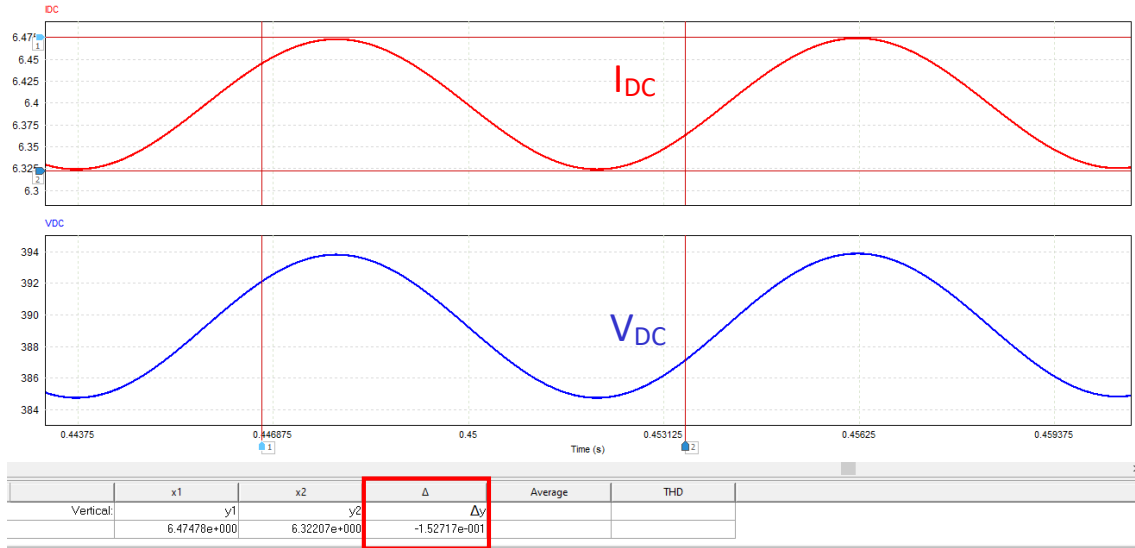


Figure 29. Close-up view of the DC Output Current Ripple

Figure 30 shows the achieved rated input apparent power which is very close to 2.5 kVA
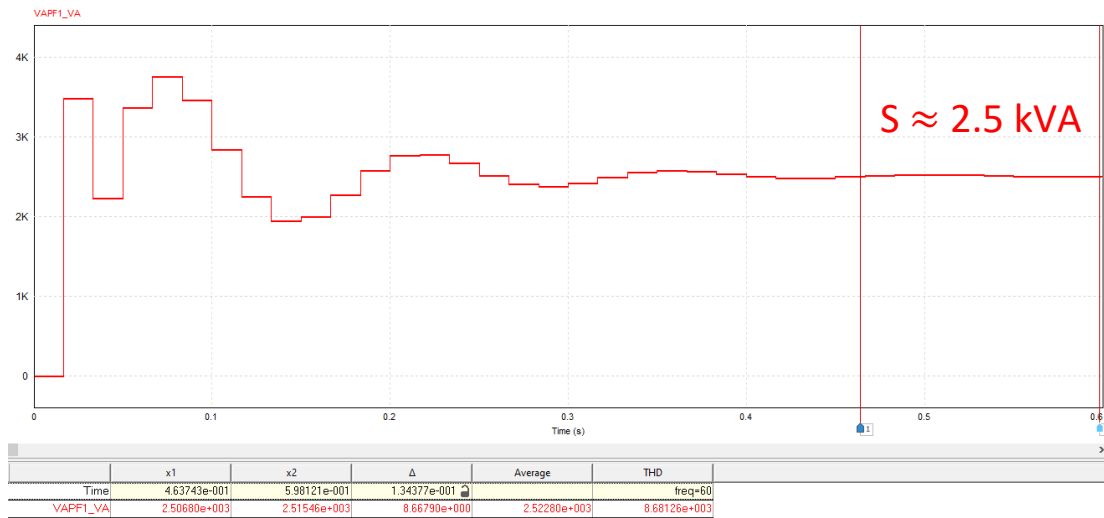


Figure 30. Input Apparent Power

Figure 31 shows the Fast Fourier Transform Analysis for the output current and output voltage without having any passive or active filters. The second order harmonic can be clearly seen at the frequency of 120 Hz. Some higher order harmonics can also be noticed.
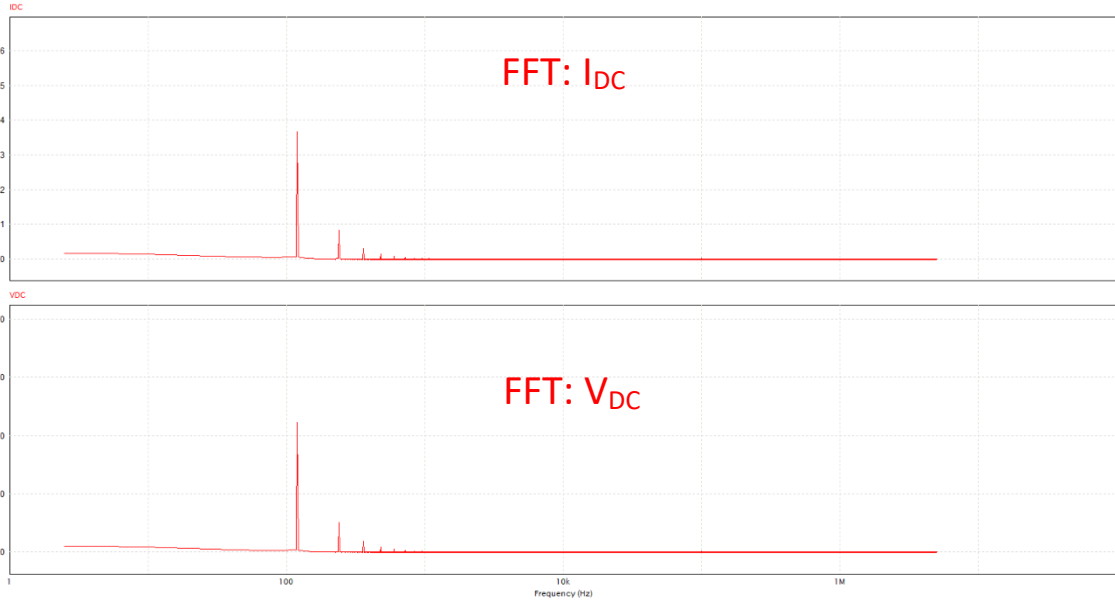


Figure 31. FFT Analysis for the Output Current and Output Voltage with no Filters

Figure 32 shows the Fast Fourier Transform Analysis for the output current and output voltage with the four electrolytic DC-link filters. It can be clearly seen that the second order harmonic is taken care of by the DC-link capacitors. In addition, all higher order harmonics are now negligible as seen below.

FFT: I_DC

FFT: V_DC
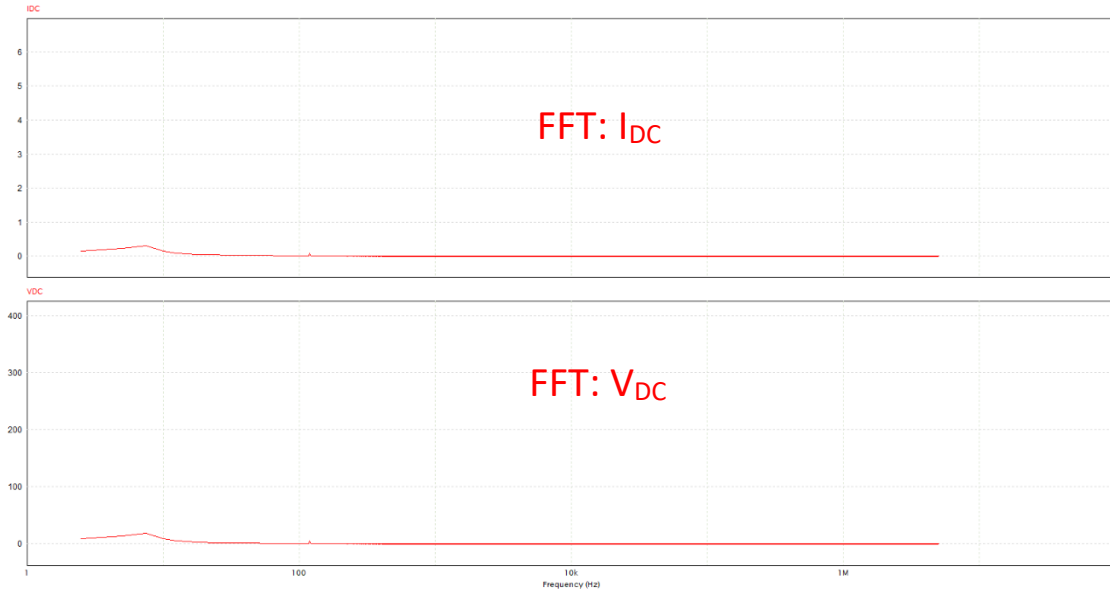
Figure  32. FFT Analysis for the Output Current and Output Voltage with DC-Link Filters

### 6.1.3   Results

This section includes the Totem-Pole PFC without the H-Bridge APD simulation results and measurements in tabular form. Table 13 presents the input voltage, which is 230V (RMS), the input current, which is about 10.5A (RMS), the output voltage, which is about 390V, the output current, which is about 6.41A, the input apparent power, which is about 2.5 kVA, the power factor, which is about 1, the input power, which is about 2.5 kW, the output power, which is about 2.41 kW, the output voltage ripple, which is about 2.3%, the output current ripple, which is about 2.4%, the capacitor's stored energy, which is about 143J, the input current THD, which is as low as 4.15%, and the overall system efficiency of about 96.4%, which is considered to be relatively high.

The output voltage ripple can be calculated as following

$$V_{ripple} = \frac{\Delta V}{V_{average}} \times 100 \tag{30}$$

$$V_{ripple} = \frac{9.2}{390} \times 100 = 2.3\% \tag{31}$$

The output current ripple can be calculated as following

$$I_{ripple} = \frac{\Delta I}{I_{average}} \times 100 \tag{32}$$

$$I_{ripple} = \frac{0.1527}{6.41} \times 100 = 2.38\% \tag{33}$$

Taking all power losses intro consideration, the real output power is

$$P_{out} = V_{out}I_{out} - P_{loss} \tag{34}$$

$$= 389.8 \times 6.408 - 87.7 = 2{,}410.16W \tag{35}$$

The DC-link capacitor's stored energy is

$$E = \frac{1}{2}C\,V^2 \tag{36}$$

$$= \frac{1}{2} \times 1.88 \times 10^{-3} \times 390^2 = 142.97\,J \tag{37}$$

The overall efficiency can then be calculated as following

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{38}$$

$$= \frac{2{,}410.16}{2{,}500} \times 100 = 96.4\% \tag{39}$$

Due to the adapted hard switching technique, the efficiency is a bit lower than 99%. It can be increased to reach up to 99% if we are to use soft switching methodology like Zero Voltage Switching (ZVS).

Table 13. Totem-Pole PFC without H-Bridge APD Results

| Measured Parameters | Unit | Totem-Pole PFC without H-Bridge APD |
|---|---|---|
| Input Voltage (AC) (rms) | V | 230 |
| Input Current (AC) (rms) | A | $\dfrac{14.86}{\sqrt{2}} = 10.508$ |
| Output Voltage (DC) | V | 389.8 |
| Output Current (DC) | A | 6.408 |
| Input Apparent Power (S) | VA | 2,500 |
| Power Factor (PF) | - | 0.999 |
| Input Power (Pin) | W | 2,500 |
| Output Power (Pout) | W | 2,410.16 |
| Output Voltage Ripple | % | 2.3 |
| Output Current Ripple | % | 2.38 |
| Capacitor's Stored Energy | J | 142.97 |
| Input Current (THD) | % | 4.149 |
| Efficiency (η) | % | 96.4 |

## 6.2 Totem-Pole Bridgeless PFC with the H-Bridge APD

This subsection consists of power loss calculations, simulation analysis and results of the Totem-Pole PFC with the additional H-Bridge ADP.

6.2.1   Power Loss Analysis

Similarly, two methods were used to find the power losses of the Totem-Pole PFC with the additional H-Bridge APD, by measurement and by calculation.

Firstly, PSIM simulation was used to measure the power losses of the active switches (GaNs and MOSFETs) and the inductors by replacing the ordinary modules with thermal ones. Thermal modules allow to monitor the GaNs/MOSFETs/Inductors thermal conditions and accordingly measure the switching and conduction losses for the switching devices and core and winding losses for the inductors. Thermal module switching devices have one additional node as shown in the previous section. The voltage measured at this node represents the case temperature of the device $T_c$ in °C. Therefore, assuming that the ambient temperature is 25 °C, a DC voltage source of 25V was connected to the nod which depicts the thermal equivalent circuit used for each high/low frequency switching leg. The current flowing out of the node represents the heat power flow out of the device which equals the total power losses in the component (in watts). Thus, to measure and display the switching device power losses, an ammeter is connected between the nodes and the ground. The current depends on the component's temperature, the ambient temperature and the thermal equivalent circuit of the component. Figure 33 below shows the conduction (2.040W) and switching (5.457W) losses of GaN1, Figure 34 shows the conduction (2.035W) and switching (5.370W) losses of GaN2, Figure 35 shows the conduction (1.790W) and switching (4.540W) losses of GaN3, Figure 36 shows the conduction (1.799W) and switching (4.640W) losses of GaN4, Figure 37 shows the conduction (1.796W) and switching (4.540W) losses of GaN5, Figure 38 shows the conduction (1.791W) and switching (4.484W) losses of GaN6, Figure 39 shows the

conduction (8.237W) and switching (3.169W) losses of MOSFET1, and Figure 40 shows the conduction (3.151W) and switching losses of MOSFET2. Table 14 below contains the breakdown of the conduction and switching losses for the high and low (line) frequency switching leg components. Likewise, the thermal module inductor has two additional nodes, as shown in Figure 18 earlier. The current flowing out of the node with a dot represents the core losses of the AC side inductor (0.061W), while the current flowing out of the other node represents the winding losses (38.5W) as shown in Figure 41. By summing these two power losses, we find the total power losses of the inductor (38.561W). Consequently, to measure and display the losses, an ammeter is connected between the nodes and the ground. To estimate the power losses for the AC side (input) inductor, five series connected $100\mu H$ thermal inductors were used in the simulation. Similarly, a thermal model inductor was used in the H-Bridge APD. The decoupling inductor's core losses (4.45W) and winding losses (1.09W) are shown in Figure 42. By summing these two power losses, we find the total power losses of the decoupling inductor (5.54W). Table 15 below consists of the breakdown of the core and winding losses of the equivalent AC side inductor and the decoupling inductor.

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 2.09695e-001 | 4.80000e-001 | 2.70305e-001 | | freq=60 |
| Q7_Pcond_Q | 1.26244e+000 | 2.01415e+000 | 7.51709e-001 | 2.03986e+000 | 3.20813e+000 |
| Q7_Psw_Q | 8.20622e+000 | 1.29980e+001 | 4.79175e+000 | 5.45684e+000 | 1.15336e+000 |
| Q7_Ptotal | 9.46866e+000 | 1.50121e+001 | 5.54346e+000 | 7.49670e+000 | 1.87638e+000 |
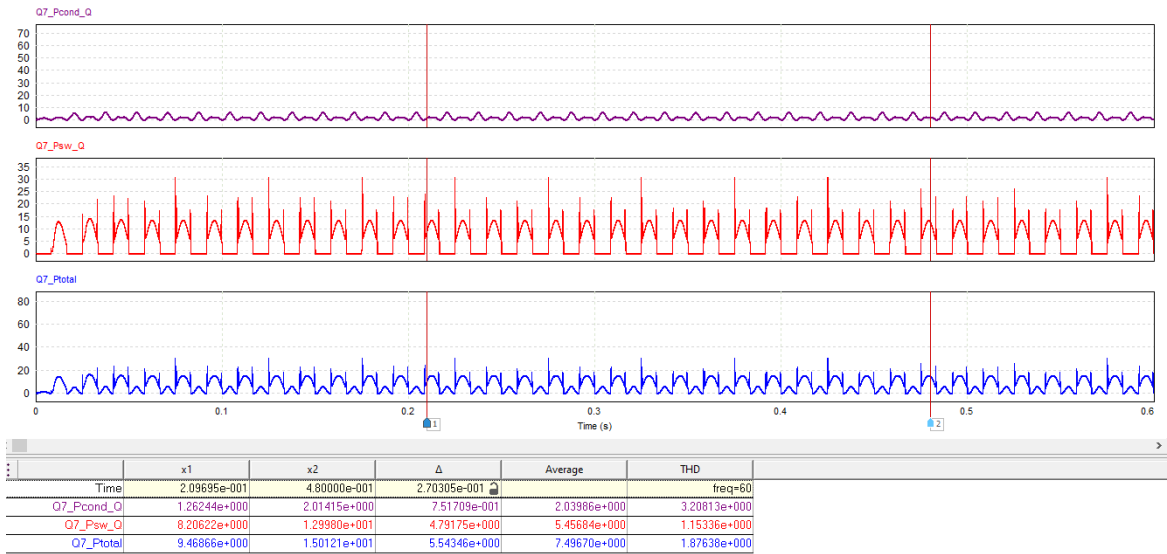
Figure  33. Conduction and Switching Losses for GaN1



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.82017e-001 | 4.80000e-001 | 2.97983e-001 | | freq=60 |
| Q8_Pcond_Q | 7.21625e-001 | 5.27635e+000 | 4.55473e+000 | 2.03511e+000 | 3.20711e+000 |
| Q8_Psw_Q | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 5.36988e+000 | 1.13283e+000 |
| Q8_Ptotal | 7.21625e-001 | 5.27635e+000 | 4.55473e+000 | 7.40499e+000 | 1.85975e+000 |
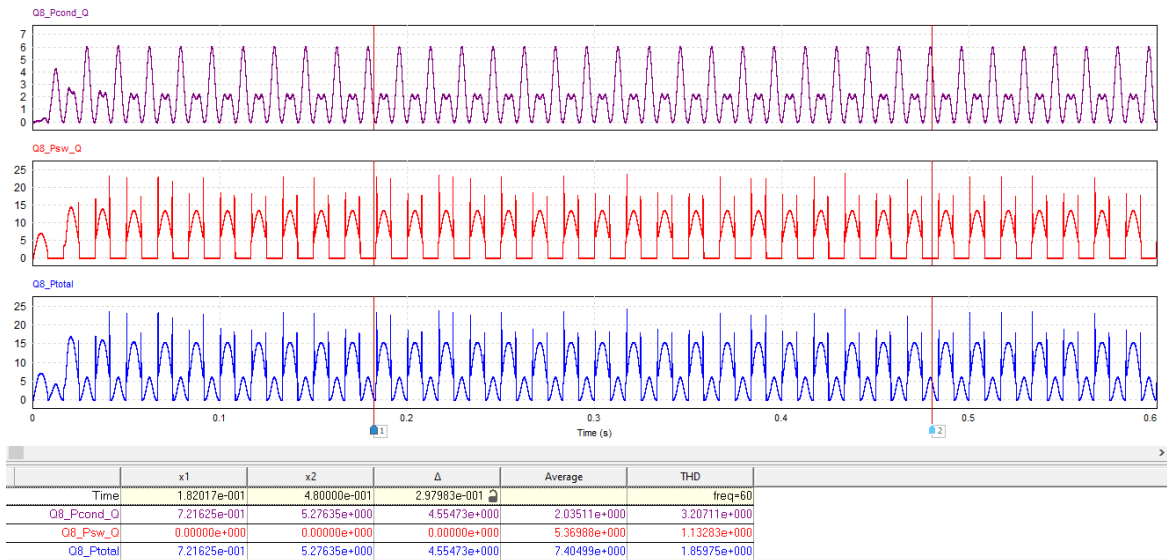
Figure  34. Conduction and Switching Losses for GaN2
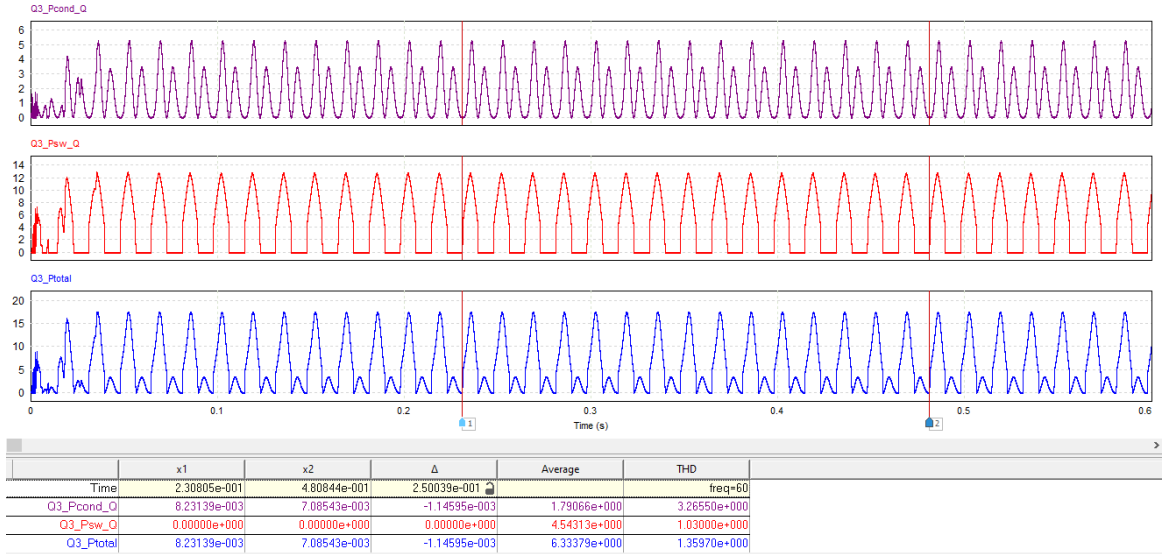
Figure 35. Conduction and Switching Losses for GaN3

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 2.30805e-001 | 4.80844e-001 | 2.50039e-001 | | freq=60 |
| Q3_Pcond_Q | 8.23139e-003 | 7.08543e-003 | -1.14595e-003 | 1.79066e+000 | 3.26550e+000 |
| Q3_Psw_Q | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 4.54313e+000 | 1.03000e+000 |
| Q3_Ptotal | 8.23139e-003 | 7.08543e-003 | -1.14595e-003 | 6.33379e+000 | 1.35970e+000 |
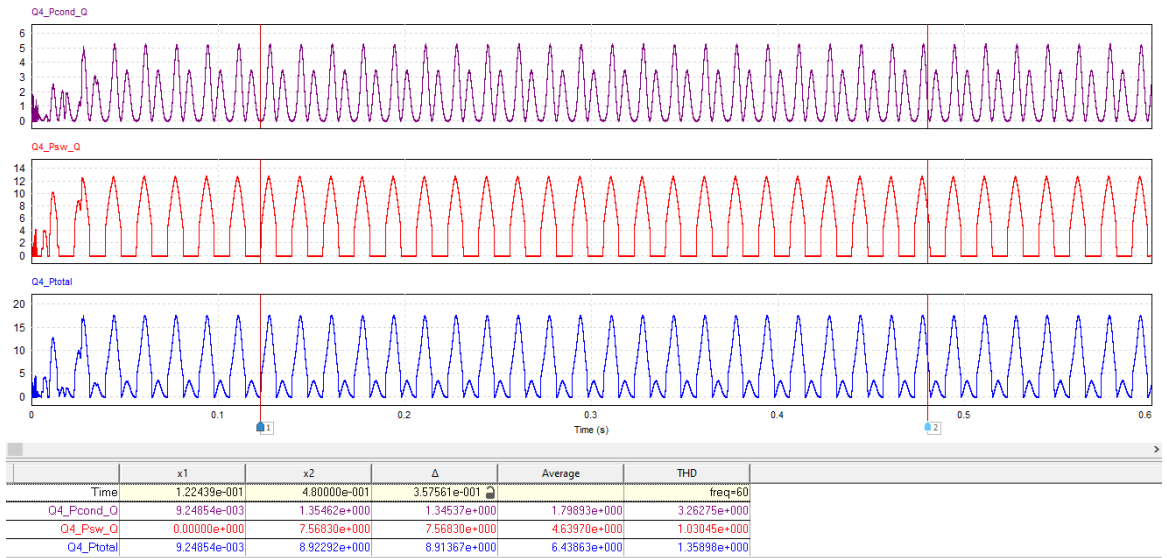


Figure 36. Conduction and Switching Losses for GaN4

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.22439e-001 | 4.80000e-001 | 3.57561e-001 | | freq=60 |
| Q4_Pcond_Q | 9.24854e-003 | 1.35462e+000 | 1.34537e+000 | 1.79893e+000 | 3.26275e+000 |
| Q4_Psw_Q | 0.00000e+000 | 7.56830e+000 | 7.56830e+000 | 4.63970e+000 | 1.03045e+000 |
| Q4_Ptotal | 9.24854e-003 | 8.92292e+000 | 8.91367e+000 | 6.43863e+000 | 1.35898e+000 |

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| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.31353e-001 | 4.80000e-001 | 3.48647e-001 🔒 | | freq=60 |
| Q5_Pcond_Q | 1.62498e-002 | 1.35251e+000 | 1.33626e+000 | 1.79623e+000 | 3.26468e+000 |
| Q5_Psw_Q | 0.00000e+000 | 7.50266e+000 | 7.50266e+000 | 4.54047e+000 | 1.02994e+000 |
| Q5_Ptotal | 1.62498e-002 | 8.85517e+000 | 8.83892e+000 | 6.33670e+000 | 1.35947e+000 |

Figure  37. Conduction and Switching Losses for GaN5



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.59030e-001 | 4.80000e-001 | 3.20970e-001 🔒 | | freq=60 |
| Q6_Pcond_Q | 3.25635e+000 | 1.13849e-001 | -3.14250e+000 | 1.79118e+000 | 3.26247e+000 |
| Q6_Psw_Q | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 4.48404e+000 | 1.03031e+000 |
| Q6_Ptotal | 3.25635e+000 | 1.13849e-001 | -3.14250e+000 | 6.27521e+000 | 1.35887e+000 |
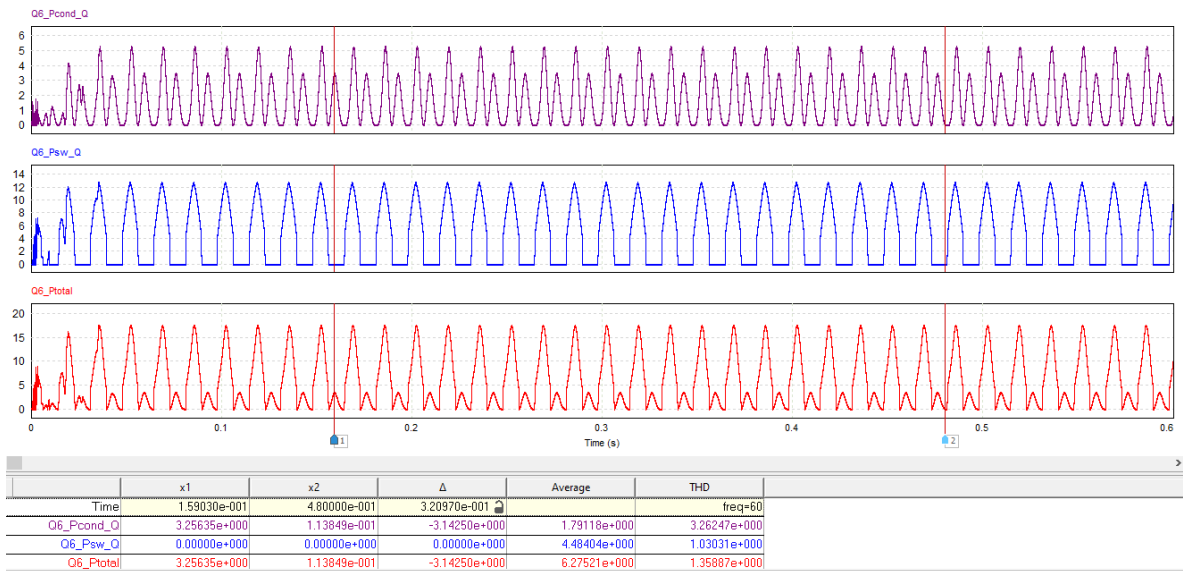
Figure  38. Conduction and Switching Losses for GaN6

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.73323e-001 | 5.21863e-001 | 3.48540e-001 | | freq=60 |
| MSF2_Pcond_Q | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 8.23740e-001 | 1.23506e+000 |
| MSF2_Pcond_D | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.16892e+000 | 1.01282e+000 |
| MSF2_Ptotal | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.99401e+000 | 1.00045e+000 |

Figure  39. Conduction and Switching Losses for MOSFET1



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.79572e-001 | 4.80000e-001 | 3.00428e-001 | | freq=60 |
| MSF3_Pcond_D | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.15080e+000 | 1.01282e+000 |
| MSF3_Ptotal | 0.00000e+000 | 0.00000e+000 | 0.00000e+000 | 3.97105e+000 | 1.00054e+000 |

Figure  40. Conduction and Switching Losses for MOSFET2

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Table 14. Conduction and Switching Losses for Active Switches

| Switches | Conduction Losses (W) | Switching Losses (W) | Total Losses (W) |
|---|---|---|---|
| GaN1 | 2.040 | 5.457 | 7.497 |
| GaN2 | 2.035 | 5.370 | 7.405 |
| GaN3 | 1.790 | 4.540 | 6.334 |
| GaN4 | 1.799 | 4.640 | 6.439 |
| GaN5 | 1.796 | 4.540 | 6.337 |
| GaN6 | 1.791 | 4.484 | 6.275 |
| SiC1 | 8.237 | 3.169 | 3.994 |
| SiC2 | 3.151 | - | 3.971 |
| Total Losses (W) | 22.639 | 32.2 | 48.252 |
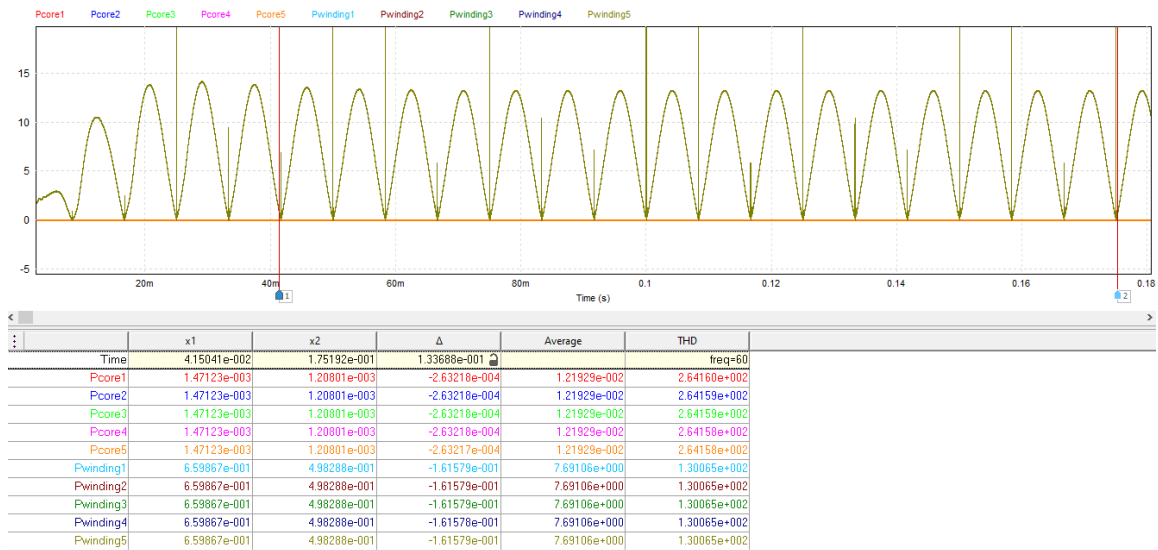


Figure 41. AC Side Inductor Core and Winding Losses
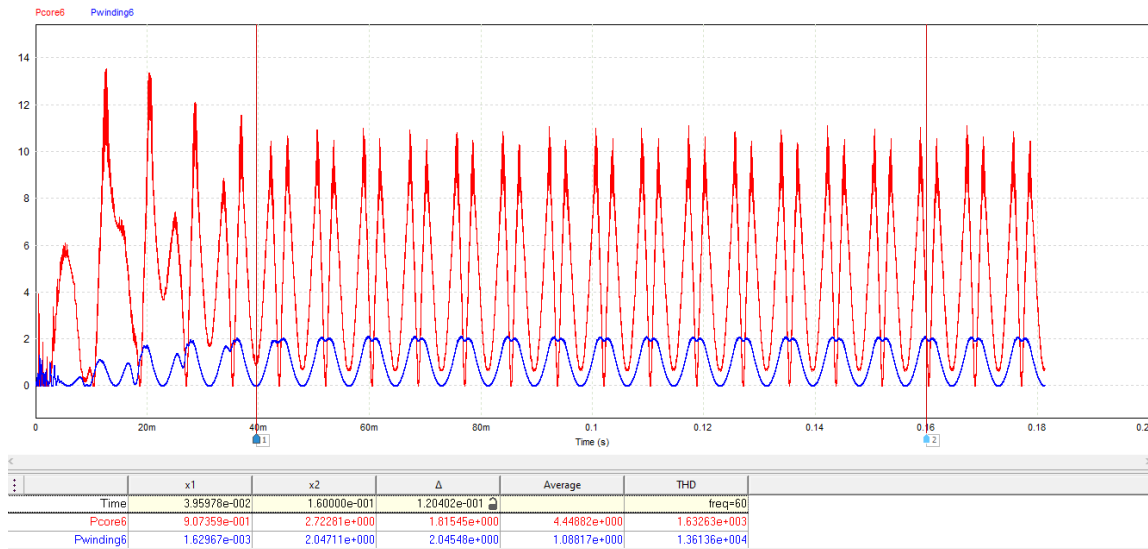
Figure 42. Decoupling Inductor Core and Winding Losses

Table 15. Core and Winding Losses for the Input and Decoupling Inductors

| Components | Core Losses (W) | Wining Losses (W) | Total Losses (W) |
|---|---|---|---|
| Input Inductor | 0.061 | 39.4 | 38.5 |
| Decoupling Inductor | 4.45 | 1.09 | 5.54 |
| Total Losses (W) | 4.511 | 40.49 | 44.04 |

Secondly, power losses calculation and interpretation for the DC-link and the decoupling capacitors is estimated with simple mathematical operations. By multiplying the Equivalent Series Resistance (ESR) of the capacitor with the root mean square (RMS) value of the capacitor's current squared, the capacitor's power dissipation is determined. The tested ESR value of Totem-Pole PFC DC-Link capacitor is specified in the datasheet to be ($ESR_1$= 3.2mΩ) [20] and the tested ESR value of Totem-Pole PFC decoupling capacitors, is specified in the datasheet to be ($ESR_2$= 6.3mΩ) [21]. One $5\mu F$ film capacitor was used as a DC-Link filter and two parallel $50\mu F$ polypropylene film capacitors were

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used in the decoupling H-Bridge. Thus, the total capacitance power loss can be calculated as following:

$$P_{loss} = ESR_1 \times I_{RMS}^2 + ESR_2 \times I_{decoupling\,RMS}^2 \tag{40}$$

$$= 3.2 \times 10^{-3} \times 6.41^2 + 2 \times 6.3 \times 10^{-3} \times \left(\frac{13.8}{\sqrt{2}}\right)^2 = 1.33\ \text{W} \tag{41}$$

The total power loss shown in Table 16 below is used in calculating the overall converter's efficiency as seen in the results section.

Table 16. Total Power Losses for the Totem-Pole PFC with the APD

| Components | Total Power losses (W) |
|---|---|
| Active Switches | 48.252 |
| Inductors | 44.04 |
| Capacitors | 1.33 |
| Total Power Losses (W) | 93.622 |

**Active Components Power Losses Comparison**
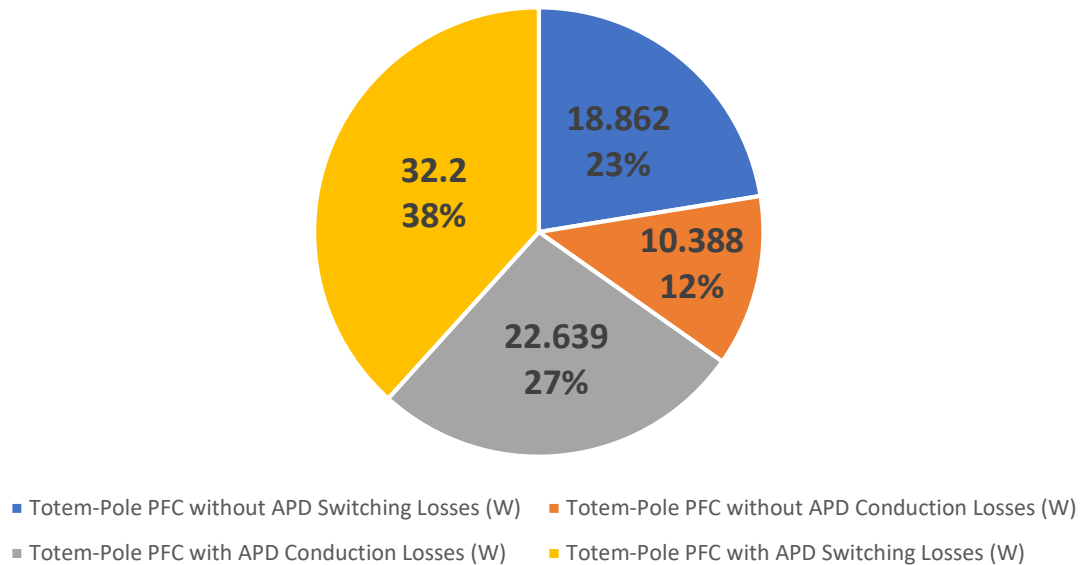


Figure 43. Active Components Power Losses Comparison

The pie-chart in Figure 43 provides a comparison between the Totem-Pole PFC with APD and the Totem-Pole PFC without APD in terms of active components (GaN/MOSFET switches) power losses. We notice that the Totem-Pole PFC without APD has a switching loss of around 23% (18.862W) and a conduction loss of around 12% (10.388W), while the Totem-Pole PFC with APD has a switching loss of around 38% (32.2W) and a conduction loss of around 27% (22.639W). This is duo to the fact that the Totem-Pole PFC with APD has an additional four switches that construct the H-Bridge Active Power Decoupling circuit and this increases the number of active devices from four switches to eight.

## Passive Components Power Losses Comparison
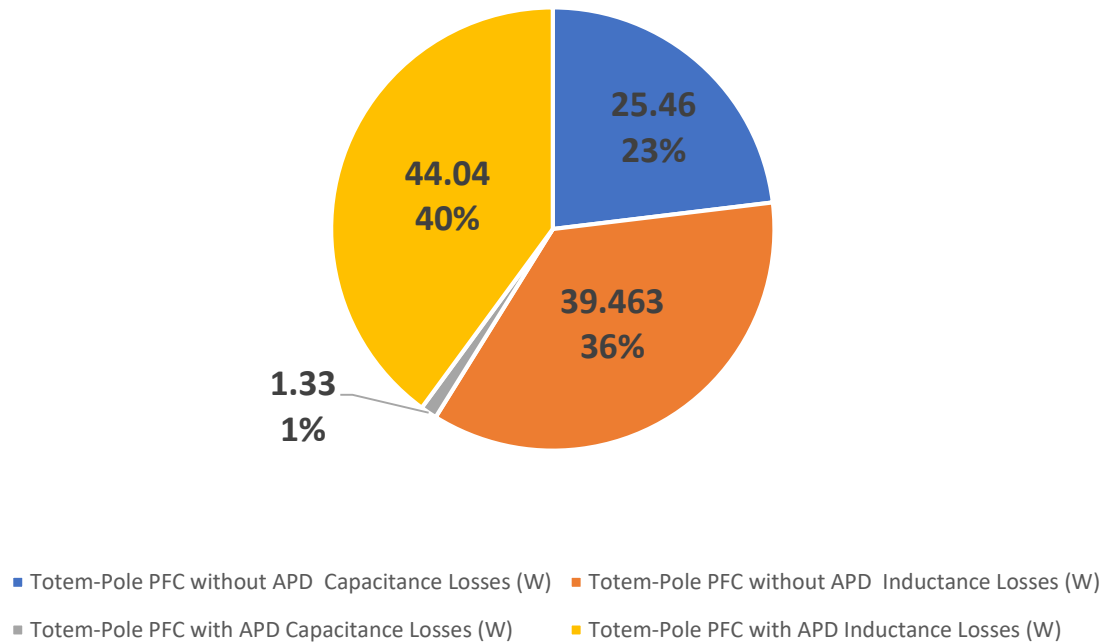


Figure 44. Passive Components Power Losses Comparison

The pie-chart in Figure 44 provides a comparison between the Totem-Pole PFC with APD and the Totem-Pole PFC without APD in terms of passive components (inductors/capacitors) power losses. We notice that the Totem-Pole PFC without APD has a capacitance loss of around 23% (25.46W) and inductance loss of around 36% (39.463W), while the Totem-Pole PFC with APD has a capacitance loss of around 1% (1.33W) and inductance loss of around 40% (44.04W). It is clearly seen that the Totem-Pole PFC with APD has much smaller capacitance loss, although it uses an additional decoupling capacitor, and that is duo to having a significantly much suppressed DC-link capacitor. As for the inductance loss, it is slightly higher in the Totem-Pole PFC with APD due to the additional decoupling inductor used in the APD.

6.2.2    Simulation Waveforms

This subsection consists of all simulation outputs related to the Totem-Pole PFC with the H-Bridge APD. The circuit is built, simulated, tested, and analyzed using PSIM simulation. The simulation waveforms depicted below include the input voltage, input current, output voltage, output current, input apparent power, the power factor, and the Fast Fourier Transform (FFT) Analysis. Figure 45 below shows the input (AC) voltage source waveform and the scaled ($\times$ 10) input (AC) current waveform. It is clearly noticed that the input voltage and input current are in phase and a unity power factor is achieved by the proposed topology as seen in Figure 46.
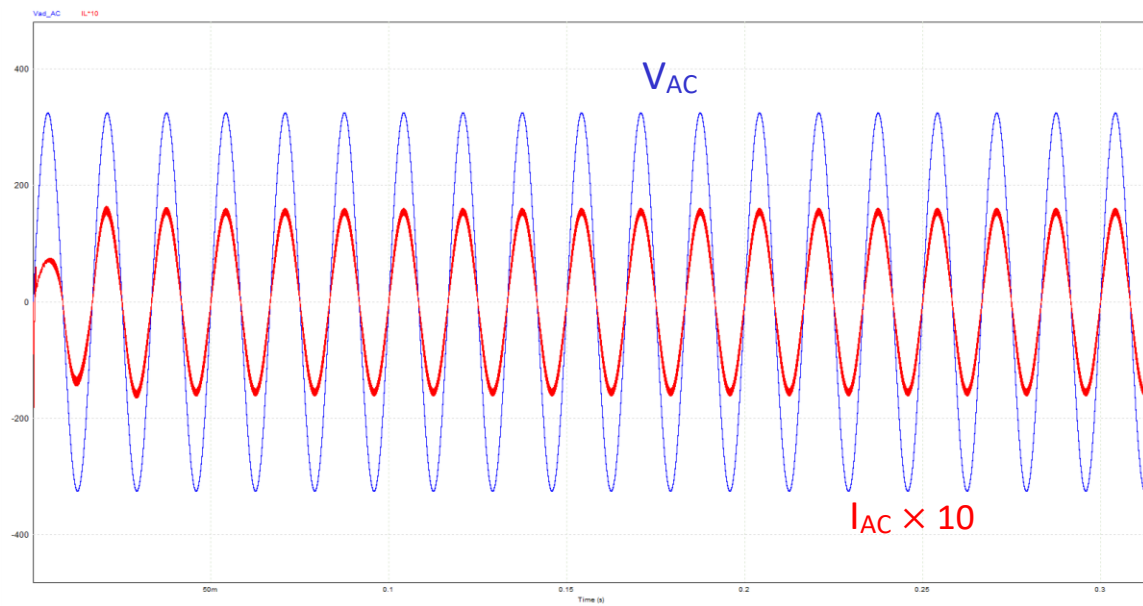


Figure  45. Input (AC) Voltage Source Waveform (in Blue) and Input (AC) Current Waveform (in Red)

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 7.65759e-001 | 9.64202e-001 | 1.98444e-001 | | freq=60 |
| VAPF1_PF | 9.98402e-001 | 9.99035e-001 | 6.32295e-004 | 9.99153e-001 | 1.63318e+006 |

Figure  46. Achieved Unity Power Factor

Figure 47 (a) shows a perfect sinusoidal input current, Figure 47 (b) shows the rippled DC output current, Figure 47 (c) shows the rippled DC output voltage. It can be clearly seen that a stable AC/DC conversion is achieved.



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 7.79006e-001 | 9.12391e-001 | 1.33386e-001 | | freq=60 |
| IL | -1.55493e+001 | -1.59830e+001 | -4.33688e-001 | -7.03023e-003 | 4.13017e-002 |
| IDC | 6.40442e+000 | 6.37678e+000 | -2.76407e-002 | 6.41025e+000 | 2.79541e+005 |
| VDC | 3.89645e+002 | 3.87963e+002 | -1.68166e+000 | 3.90000e+002 | 2.79541e+005 |
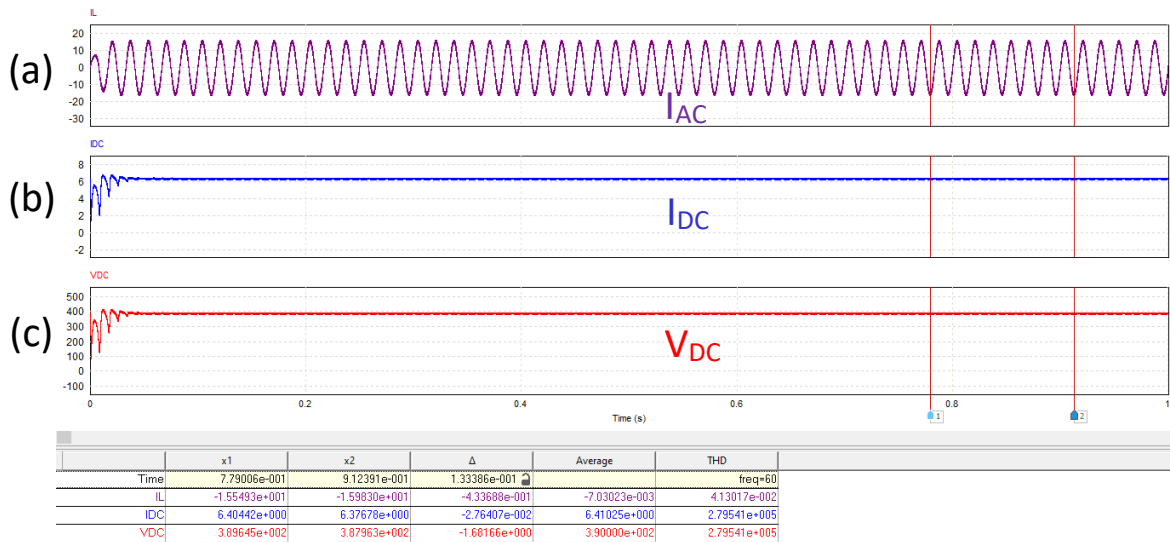
Figure  47. (a) AC Input Current (b) DC Output Current (c) DC Output Voltage

A close-up view of all three waveforms is provided in Figure 48 below.



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 7.79006e-001 | 9.12391e-001 | 1.33386e-001 | | freq=60 |
| IL | -1.55493e+001 | -1.59830e+001 | -4.33688e-001 | -7.03023e-003 | 4.13017e-002 |
| IDC | 6.40442e+000 | 6.37678e+000 | -2.76407e-002 | 6.41025e+000 | 2.79541e+005 |
| VDC | 3.89645e+002 | 3.87963e+002 | -1.68166e+000 | 3.90000e+002 | 2.79541e+005 |
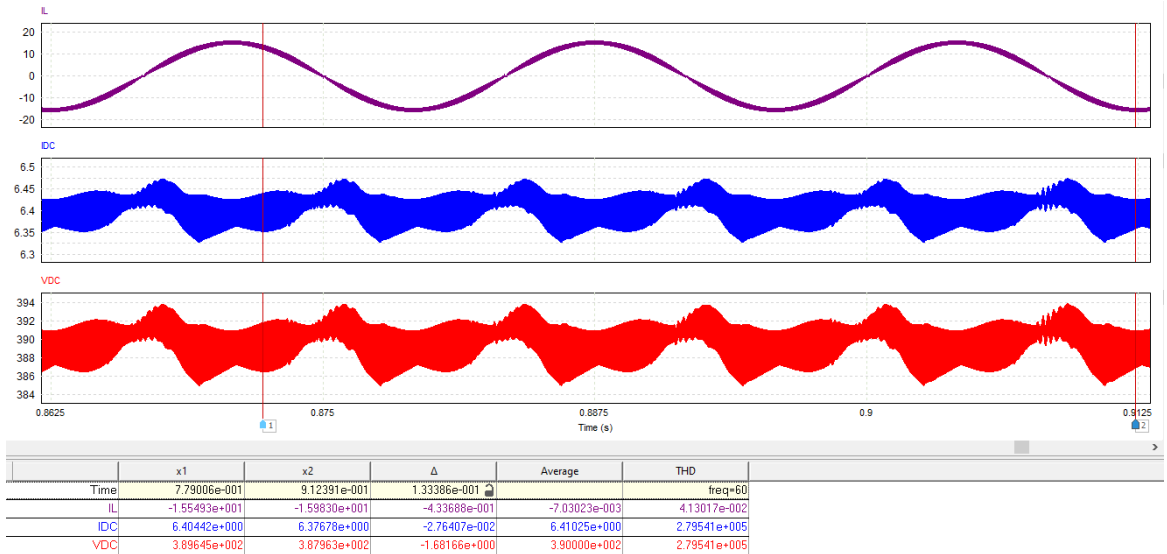
Figure  48. Close-up view of All Three Waveforms

Figure 49 below shows a zoomed view of the DC output voltage ripple, where ΔV

is clearly seen to have a value of 8.748V



| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Vertical: | y1 | y2 | Δy | | |
| | 3.93773e+002 | 3.85025e+002 | -8.74766e+000 | | |
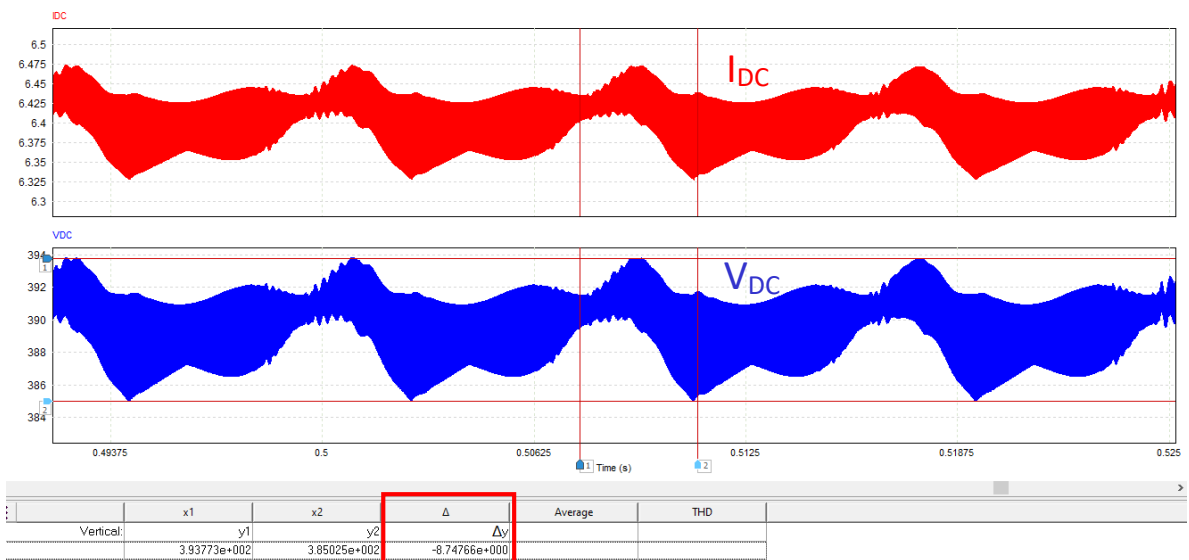
Figure  49. Close-up view of the DC Output Voltage Ripple

Similarly, Figure 50 shows a zoomed view of the DC output current ripple, where ΔI is clearly seen to have a value of 0.147A
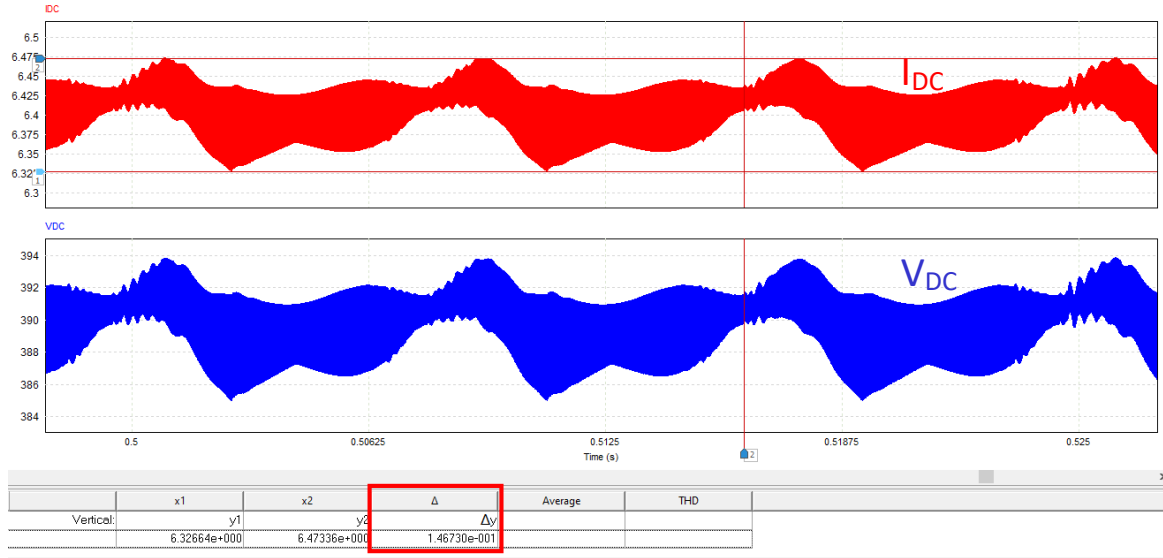


Figure  50. Close-up view of the DC Output Current Ripple

Figure 51 below shows the system's robust response for a load change from 100% (full) load to 67% load.
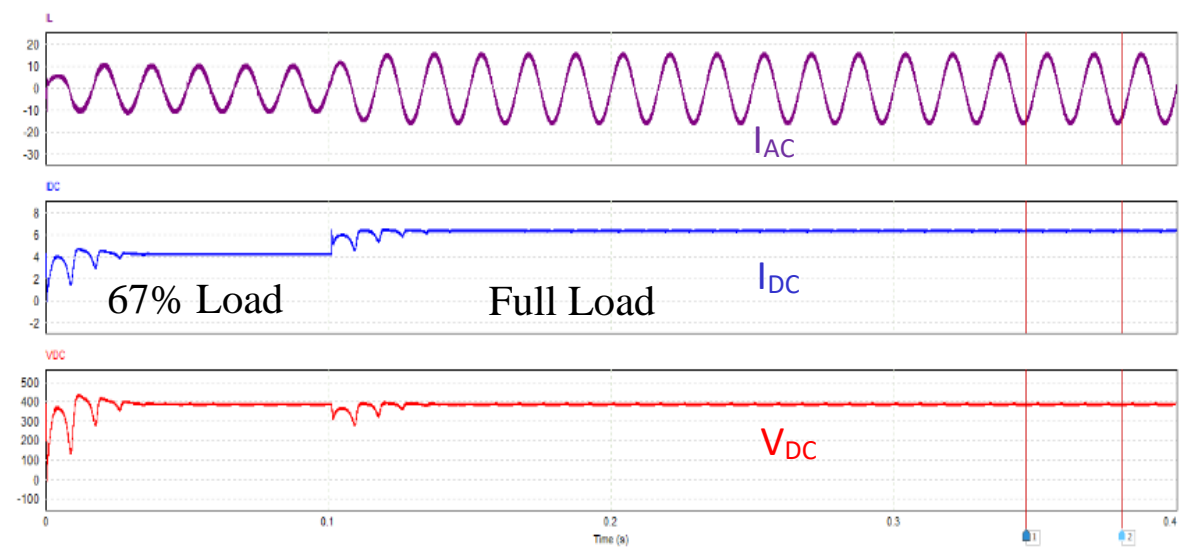


Figure  51. System's Response for Load Changes

Figure 52 shows the achieved rated input apparent power which is very close to 2.5 kVA



Figure 52. Input Apparent Power

Figure 53 shows the Fast Fourier Transform Analysis for the output current and output voltage without having any passive or active filters. The second order harmonic can be clearly seen at the frequency of 120 Hz. Some higher order harmonics can also be noticed.
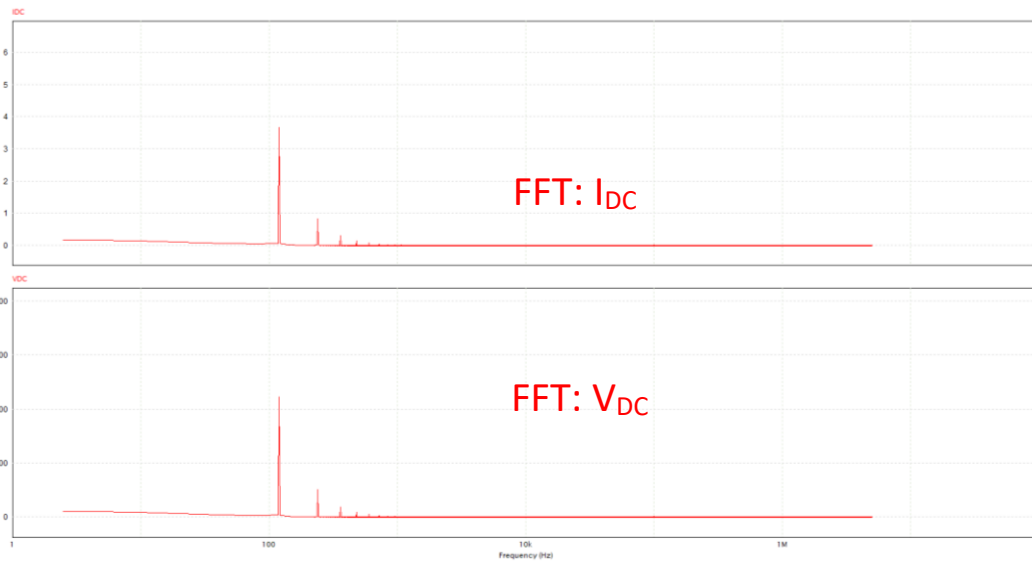


Figure 53. FFT Analysis for the Output Current and Output Voltage with no Filters

Figure 54 shows the Fast Fourier Transform Analysis for the output current and output voltage with the active power decoupling circuit operated. It can be clearly seen that the second order harmonic is taken care of by the APD. In addition, all higher order harmonics are now negligible as seen below
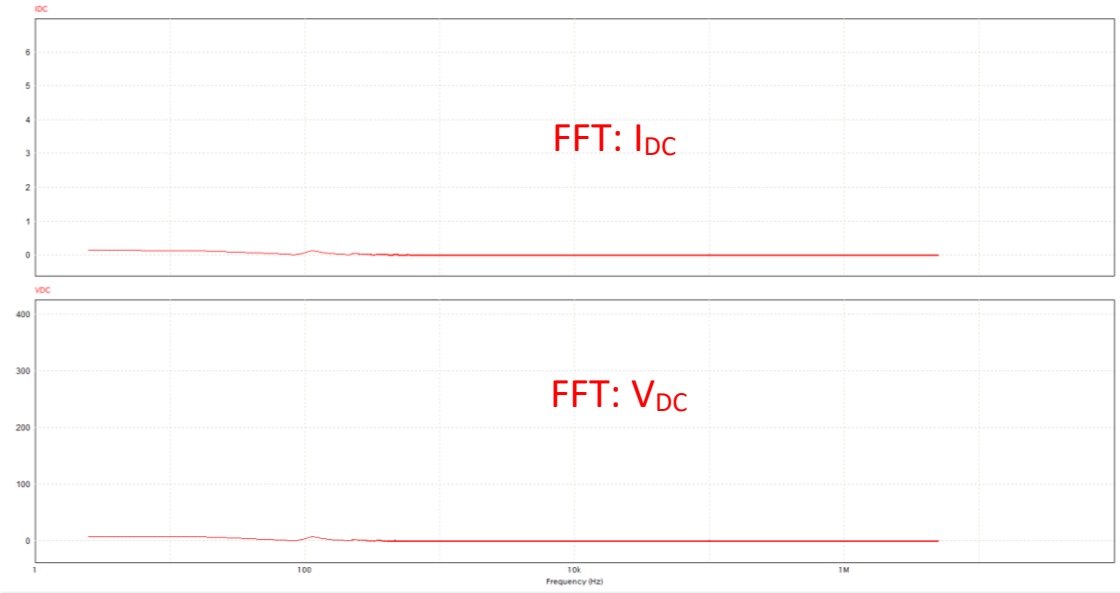


Figure 54. FFT Analysis for the Output Current and Output Voltage with APD

Figure 55 below shows the sinusoidal decoupling current waveform passing through the decoupling inductor and the decoupling capacitor. This current allows generating a reactive power that is used to cancel out the second order harmonic delivered with the output power. It is clearly seen that the peak decoupling inductor current is around 13.8A.

| | x1 | x2 | Δ | Average | THD |
|---|---|---|---|---|---|
| Time | 1.52056e-001 | 3.18697e-001 | 1.66641e-001 | | freq=60 |
| Idecoup | 1.37782e+001 | 1.38361e+001 | 5.79022e-002 | -2.13789e-003 | 6.63180e-002 |
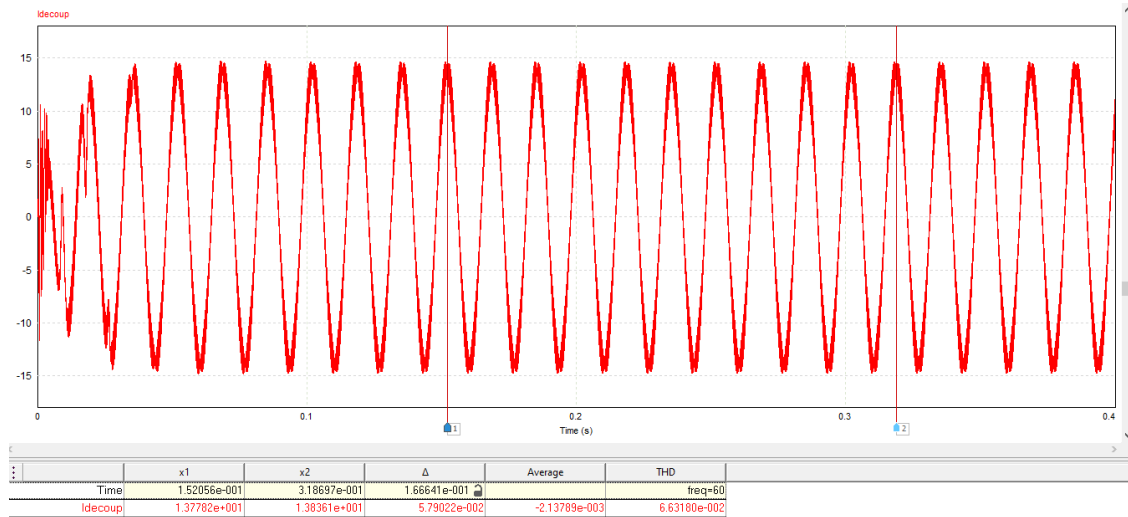
Figure  55. Decoupling Current Waveform

6.2.3   Results

This section includes the Totem-Pole PFC with the H-Bridge APD simulation results and measurements in tabular form. Table 17 presents the input voltage which is 230V (RMS), the input current, which is about 10.87A (RMS), the output voltage, which is about 390V, the output current, which is about 6.41A, the input apparent power, which is about 2.5 kVA, the power factor, which is about 1, the input power, which is about 2.5 kW, the output power, which is about 2.41 kW, the output voltage ripple, which is about 2.2%, the output current ripple, which is about 2.3%, the decoupling inductor's stored energy, which is about 7.44mJ, the decoupling and the DC-link capacitors' stored energy, which sum up to about 3.75J, the input current THD, which is as low as 4.13%, and the overall system efficiency of about 96.3%, which is considered to be relatively high.

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The output voltage ripple can be calculated as following

$$V_{ripple} = \frac{\Delta V}{V_{average}} \times 100 \tag{42}$$

$$V_{ripple} = \frac{8.748}{390} \times 100 = 2.2\% \tag{43}$$

The output current ripple can be calculated as following

$$I_{ripple} = \frac{\Delta I}{I_{average}} \times 100 \tag{44}$$

$$I_{ripple} = \frac{0.1467}{6.41} \times 100 = 2.29\% \tag{45}$$

Taking all power losses intro consideration, the real output power is

$$P_{out} = V_{out}I_{out} - P_{loss} \tag{46}$$

$$= 390 \times 6.41 - 93.622 = 2{,}406.28 \text{ W} \tag{47}$$

The DC-link capacitor's stored energy is

$$E = \frac{1}{2}C\,V^2 \tag{48}$$

$$= \frac{1}{2} \times 5 \times 10^{-6} \times 390^2 = 0.38 \text{ J} \tag{49}$$

The decoupling capacitor's stored energy is

$$E = \frac{1}{2}C\,V^2 \tag{50}$$

$$= \frac{1}{2} \times 100 \times 10^{-6} \times \left(\frac{367}{\sqrt{2}}\right)^2 = 3.367 \text{ J} \tag{51}$$

The decoupling inductor's stored energy is

$$E = \frac{1}{2}L\,i^2 \tag{51}$$

$$= \frac{1}{2} \times 156.25 \times 10^{-6} \times \left(\frac{13.8}{\sqrt{2}}\right)^2 = 7.44 \ mJ \tag{52}$$

It is clearly noticed that the total energy storage requirement in the decoupling inductor, decoupling capacitor and the DC-link capacitor (3.754 J) here is much less than the energy storage requirement of the DC-link capacitor of the Totem-Pole PFC without the ADP (142.97 J).

The overall efficiency can then be calculated as following

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{53}$$

$$= \frac{2,406.28}{2,500} \times 100 = 96.25\% \tag{54}$$

Due to the adapted hard switching technique, the efficiency is a bit lower than 99%. It can be increased to reach up to 99% if we are to use soft switching methodology like Zero Voltage Switching (ZVS).

Table 17. Totem-Pole PFC with the H-Bridge APD Results

| Measured Parameters | Unit | Totem-Pole PFC with H-Bridge APD |
|---|---|---|
| Input Voltage (AC) (rms) | V | 230 |
| Input Current (AC) (rms) | A | $\frac{15.5}{\sqrt{2}} = 10.87$ |
| Output Voltage (DC) | V | 390 |
| Output Current (DC) | A | 6.41 |
| Input Apparent Power (S) | VA | 2,500 |
| Power Factor (PF) | - | 0.999 |
| Input Power (Pin) | W | 2,500 |
| Output Power (Pout) | W | 2,406.28 |
| Output Voltage Ripple | % | 2.2 |
| Output Current Ripple | % | 2.29 |
| Decoupling Inductor's Stored Energy | mJ | 7.44 |
| Total Capacitors' Stored Energy | J | 3.75 |
| Input Current (THD) | % | 4.13 |
| Efficiency ($\eta$) | % | 96.25 |

# 7.  HARDWARE EXPERIMENTAL RESULTS

## 7.1 Hardware Design

After designing and simulating the proposed Totem-Pole PFC with the Active Power Decoupling circuit in PSIM, the circuit schematic was modified with the addition of some hardware elements that are compatible with the code generation stage. All delay elements combined with comparator blocks were replaced by 1-phase PWM blocks (Figure 56). Additionally, an Analog to Digital Convertor (ADC) block (Figure 57) was added and configured to get its inputs from all three sensors used in the topology. The output of the ADC block goes to the PI and decoupling controllers. Furthermore, a hardware configuration block (Figure 58) was used to define how ADC/GPIO ports are used in a specific hardware setting. This block is for users to define the I/O port functions of the specific hardware board that one works with. Thus, all pins were assigned properly to the hardware configuration block. After that, a c code was generated (in the appendix) and exported to the Code Composer Studio (CCS). CCS is used to configure the Digital Signal Processor (DSP) shown in Figure 59 by setting all its parameters and exporting the c code to it. The DSP (TMS320F28379D) is then used to receive all sensor's signals, analyze them, and generate PWM signals to control the switches.
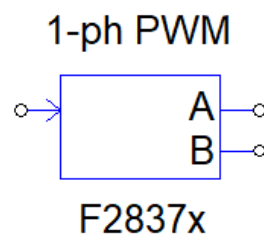
Figure  56. 1-Phase PWM Block
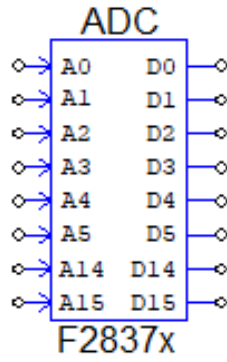
Figure  57. Analog/Digital Converter
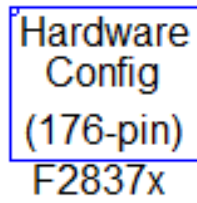


Figure  58. Hardware Configuration Block
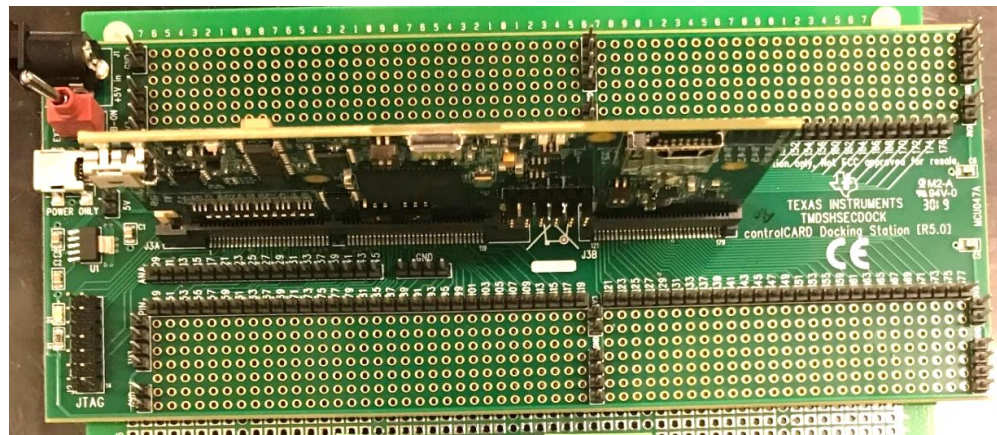


Figure  59. TMS320F28379D Digital Signal Processor

## 7.2 Prototype

Hardware setup preparation has started with the selection of the proper list of hardware components as per the design ratings. As for the Totem-Pole PFC, the TDTTP2500P100: 2.5kW Bridgeless Totem-pole PFC Evaluation Board manufactured by Transphorm [22] was used for examination. Figure 60 below shows the Transphorm Totem-Pole PFC evaluation board with an additional (fourth) 470µF aluminum electrolytic capacitor.
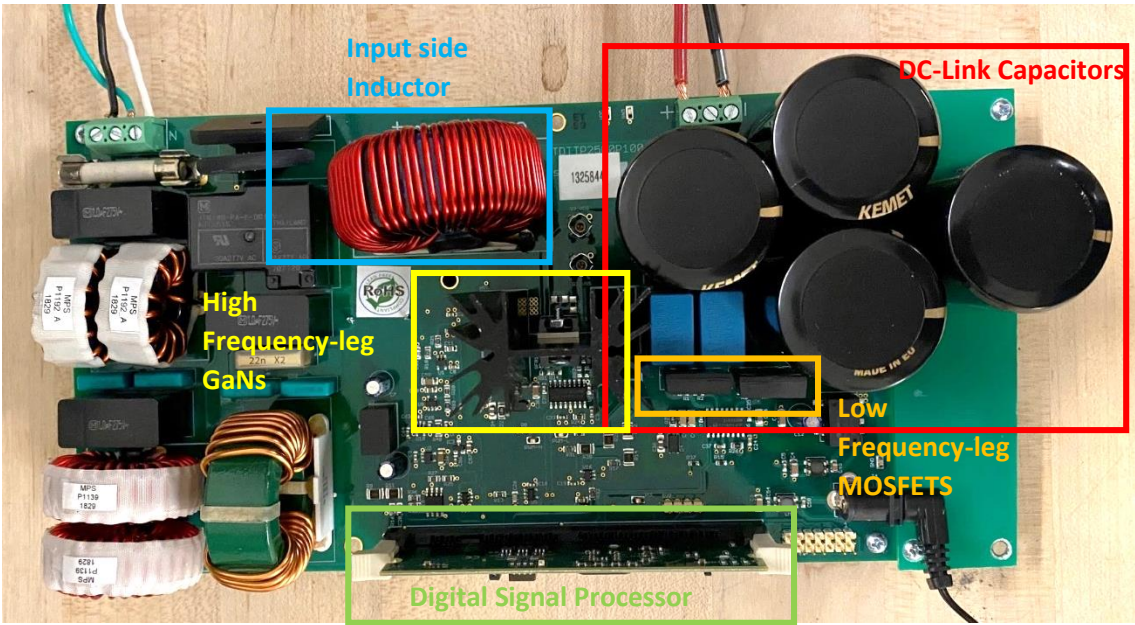


Figure  60. Transphorm Totem-Pole PFC Evaluation Board with the Additional Capacitor

The proposed active power decoupling circuit shown in Figure 61 (version 1) is composed of four GaN switches, one inductor of 152 µH, two 50 µF parallel connected capacitors (with a total capacitance of 100 µF), one current sensor, one DSP to drive the switches, and a breadboard.
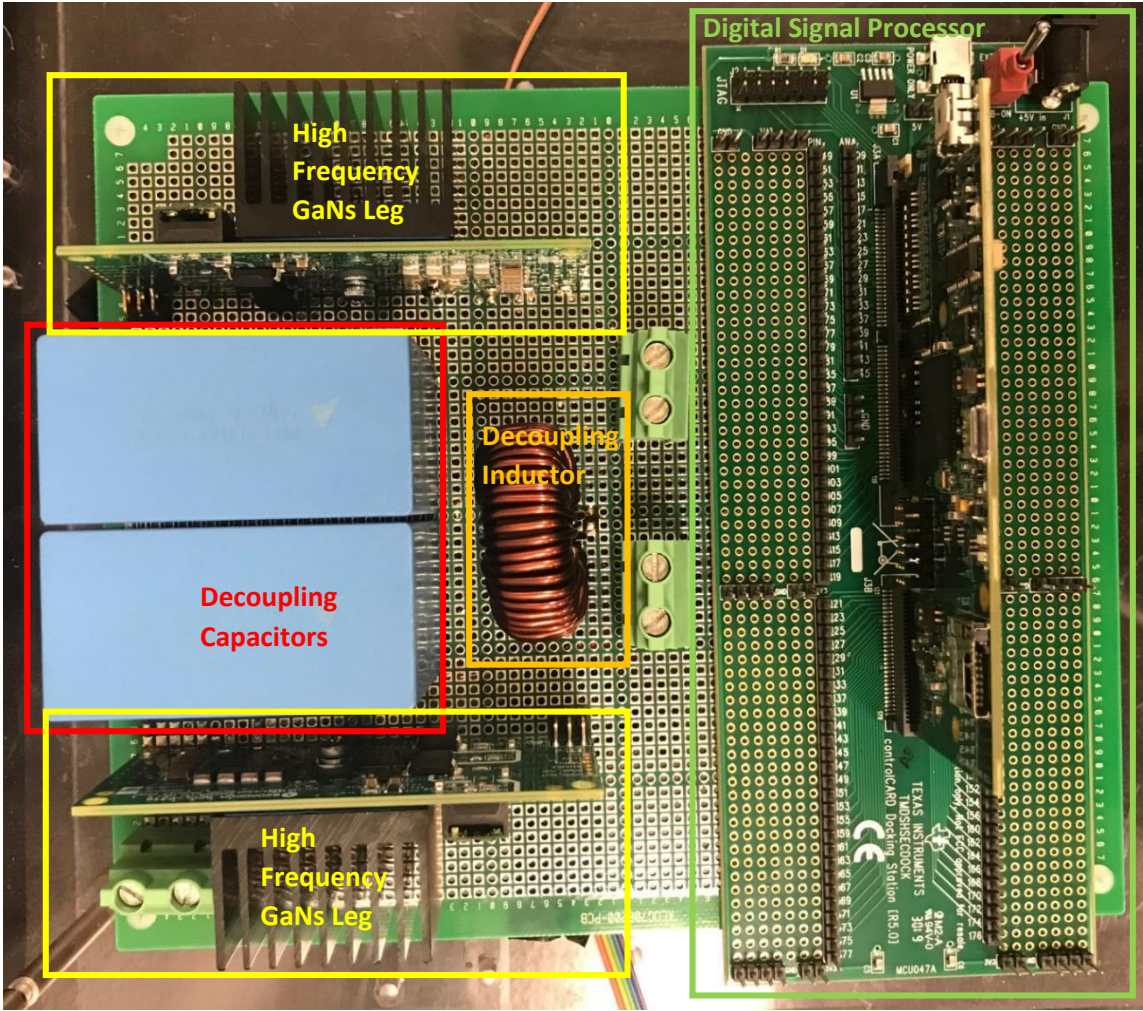


Figure 61. Proposed Active Power Decoupling Prototype (Version 1)

Below is the list of hardware components used to build version 1 of the proposed active power decoupling H-Bridge prototype:

Table 18. List of Hardware Components for the Proposed Topology (Version 1)

| Sr. No. | Part No. | Part Name | Description | Brand |
|---|---|---|---|---|
| 1 | GS66516T-EVBDB2 | 650 V GaN E-HEMT Daughter Board | Power Management IC Development Tools GS66516T Half Bridge Daughter Board | Gan Systems |
| 2 | SHBC20-1R7A0152V | Inductor | KEMET, SHBC, AC Line Filters, Normal Mode, 152 µH, 20% | KEMET |
| 3 | B32778G8506K000 | Capacitor | 50 µF Film Capacitor 800V Polypropylene (PP), Metallized Radial | TDK Electronics Inc. |
| 4 | ACS712ELCTR-20A-T | Current Sensor | Current Sensor 20A 1 Channel Hall Effect, Open Loop Bidirectional 8-SOIC (0.154", 3.90mm Width) | Allegro |
| 5 | TMDSDOCK28379D | DSP | TMS320F28379D Experimenter C2000™, Delfino™ C28x MCU 32-Bit Embedded Evaluation Board | Texas Instruments |
| 6 | EXN-23413-PCB | Breadboard | Breadboard, General Purpose Non-Plated Through Hole (NPTH) Pad Per Hole (Round) 0.100" (2.54mm) | Bud Industries |

Figure 62 shows a modified version (version 2) of the proposed active power decoupling circuit. The newer version model consists of a higher rating inductor used for experimental safety purposes. In addition, some electrolytic and film capacitors were used to terminate all wiring connections to eliminate or mitigate any inductance effect that could occur duo to the usage of long wires. This will also enhance the performance of the circuit. Version 2 is composed of four GaN switches, one inductor of 340 µH, two 50 µF parallel connected capacitors (with a total capacitance of 100 µF), two 470 µF electrolytic capacitors, eight 0.1 µF film capacitors, one current sensor, one DSP to drive the switches, and a breadboard.
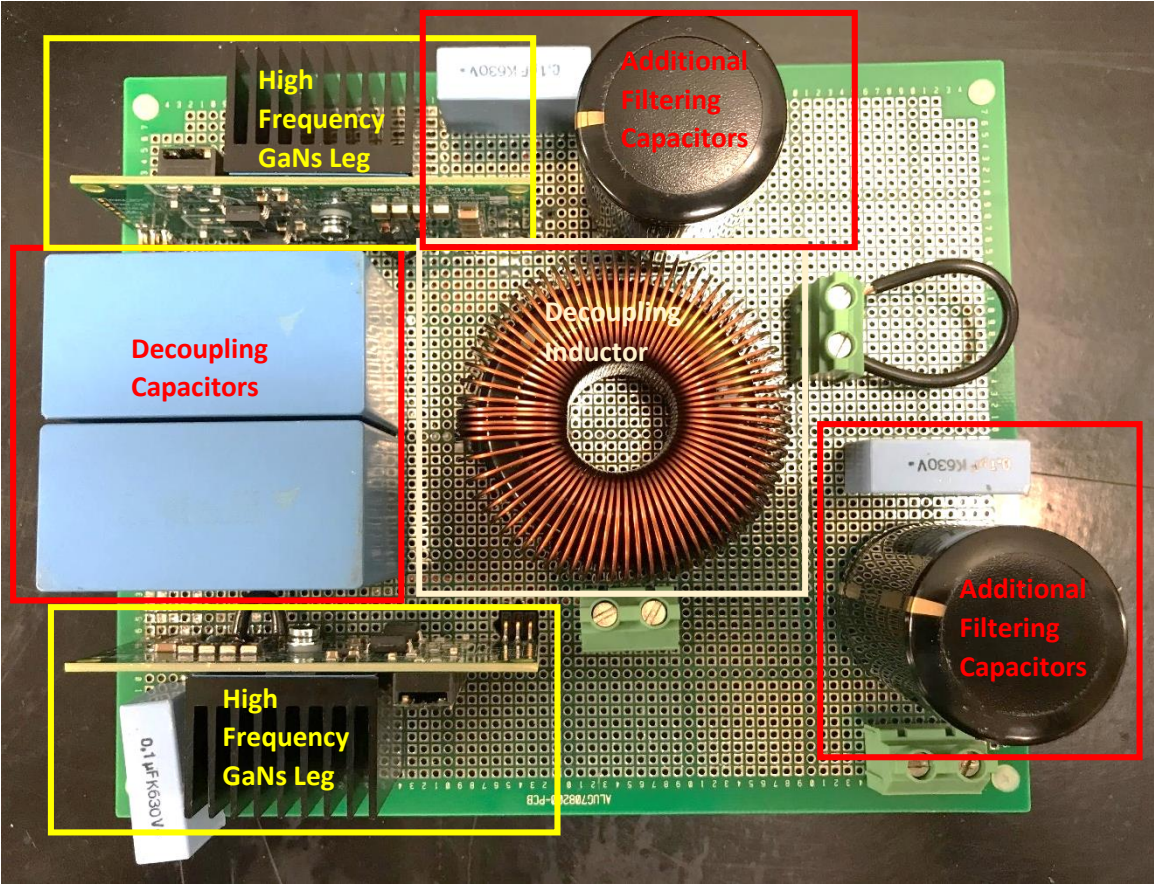


Figure 62. Proposed Active Power Decoupling Prototype (Version 2)

Below is the list of hardware components used to build version 2 of the proposed active power decoupling H-Bridge prototype:

Table 19. List of Hardware Components for the Proposed Topology (Version 2)

| Sr. No. | Part No. | Part Name | Description | Brand |
|---|---|---|---|---|
| 1 | GS66516T-EVBDB2 | 650 V GaN E-HEMT Daughter Board | Power Management IC Development Tools GS66516T Half Bridge Daughter Board | Gan Systems |
| 2 | 750343810 | Inductor | 340µH Unshielded Toroidal Inductor 15A 50mOhm Max Radial, Horizontal (Open) | Würth Elektronik |
| 3 | B32778G8506K000 | Capacitor | 50 µF Film Capacitor 800V Polypropylene (PP), Metallized Radial | TDK Electronics Inc. |
| 4 | ACS712ELCTR-20A-T | Current Sensor | Current Sensor 20A 1 Channel Hall Effect, Open Loop Bidirectional 8-SOIC (0.154", 3.90mm Width) | Allegro |
| 5 | TMDSDOCK28379D | DSP | TMS320F28379D Experimenter C2000™, Delfino™ C28x MCU 32-Bit Embedded Evaluation Board | Texas Instruments |
| 6 | EXN-23413-PCB | Breadboard | Breadboard, General Purpose Non-Plated Through Hole (NPTH) Pad Per Hole (Round) 0.100" (2.54mm) | Bud Industries |
| 7 | ALC10A471DF450 | Capacitor | 470µF 450V Aluminum Electrolytic Capacitors Radial, Can - Snap-In 252mOhm @ 100Hz 15000 Hrs @ 85°C | TDK Electronics Inc. |
| 8 | B32921C3104M000 | Capacitor | Film Capacitor 305V 630V Polypropylene (PP) Radial | TDK Electronics Inc. |

## 7.3 Experimental Results

This subsection includes all experimental results of the Totem-Pole PFC with and without the H-Bridge APD. Several experiments were done with various loads resulting in an output power that ranges from 0.5 W to 1.5 kW. Figure 63 below shows the waveforms of the AC input current (in purple) with a peak value of 10.6 A, the DC output current (in Blue) with a measured value of 3.57 A, and the DC output voltage (in Green) with a measured value of 394 V. An output power of around 1.406 kW is delivered to the load in this case.
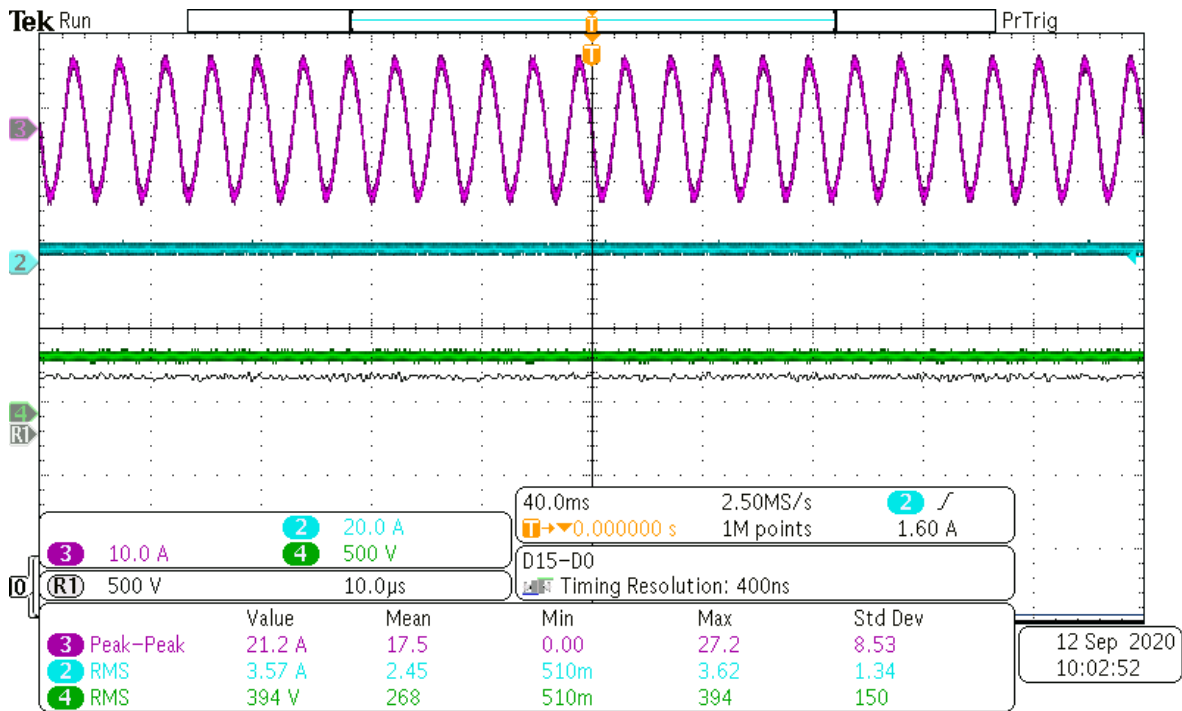


Figure 63. Totem-Pole PFC Waveforms with an Output Power of 1.406 kW

Figure 64 below shows the waveforms of the AC input current (in purple) with a peak value of 6 A, the DC output current (in Blue) with a measured value of 2.49 A, and the DC output voltage (in Green) with a measured value of 381 V. An output power of around 0.948 kW is delivered to the load in this case.



| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 3 RMS | 4.24 A | 4.24 | 4.24 | 4.24 | 0.00 |
| 2 Mean | 2.49 A | ---- | ---- | ---- | ---- |
| 4 Mean | 381 V | 381 | 381 | 381 | 0.00 |
| 1 RMS | 19.3mA | 19.3m | 19.3m | 19.3m | 0.00 |
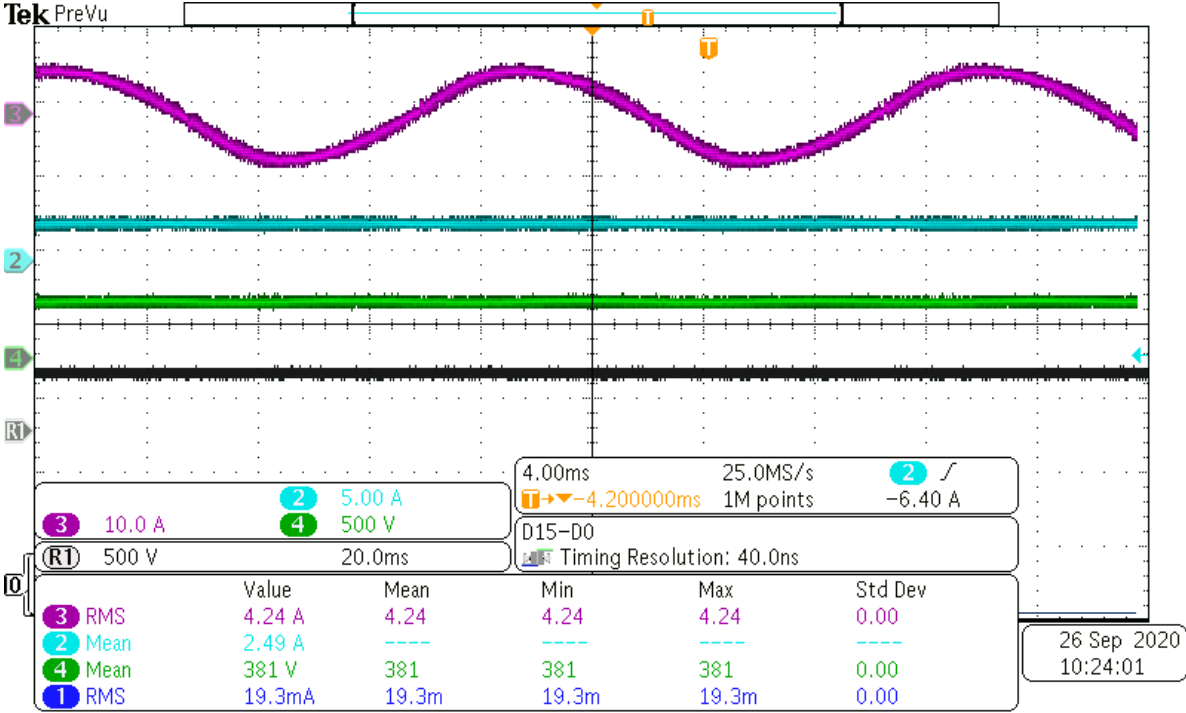
Figure  64. Totem-Pole PFC Waveforms with an Output Power of 0.948 kW

# 8. CONCLUSION

## 8.1 Conclusion

This research presented a GaN Totem-Pole Bridgeless PFC with an embedded H-Bridge Active Power Decoupling Topology with a very efficient and reliable control methodology. In addition, a detailed comparison of the Gan Totem-Pole PFC without the H-Bridge APD and the GaN Totem-Pole PFC with the H-Bridge APD was provided in this work. Moreover, a thorough analysis of the power losses for both topologies was conducted. It is proven that the proposed H-Bridge APD topology has the privilege of delivering high efficiency, unity power factor and high-power density. Furthermore, the H-Bridge APD has shown a significant enhancement on the total energy storage requirement. The total energy storage requirement has reduced from 143 J for the Totem-Pole PFC without the H-Bridge APD to around 3.76 J with the H-Bridge APD, and the bulky aluminum electrolytic DC-Link Capacitor of $1,880\mu$ was replaced by a suppressed $5\mu$ polypropylene film DC-Link Capacitor. The additional H-Bridge APD circuit has also mitigated the undesirable low-frequency power ripple caused by the single-phase inherited double-line frequency that exists naturally at the AC side of the converter. The topology was simulated and inspected on PSIM. A proof of concept and a hardware prototype was provided and the results showed substantial improvements with various ranges of loads.

**8.2 Future Work**

Further improvements could be applied to the proposed Totem-Pole Power Factor Correction Active Power Decoupling topology to include for instance soft switching control methodology. One such effective technique is Zero Voltage Switching (ZVS), which could be utilized to reduce the high frequency switching losses and accordingly enhance the conversion efficiency. That is, using ZVS may increase the overall efficiency of the system to reach up to 99%. Additional work may also include the resizing or reduction of the ac side inductor without affecting the input current shape or ripple to achieve the same marvelous performance.

In regards to the control strategy of the overall system, some more enhancements may be perfumed to the Totem-Pole PI controllers to handle more operating ranges (i.e. input ac voltage source of 85V to 265V). In addition, PI parameters may be improved to achieve better system response that assures the attainment of a robust control. Furthermore, the active power decoupling control may also be enhanced to achieve a stable dynamic performance by utilizing the feedback of the input ac voltage source and use it in the calculation of the active power decoupling voltage reference peak. This will ensure having an independent automatic APD control that does not need to be interfered with every time the input voltage source is changed.

REFERENCES

[1]     Marashi, Ali. "How to Improve Data Center Power Consumption & Energy
        Efficiency." Data Centers and Colocation Services,
        www.vxchnge.com/blog/power-hungry-the-growing-energy-demands-of-data-
        centers.

[2]     Qingyun Huang and Alex Q. Huang, "Review of GaN Totem-Pole Bridgeless PFC",
        CPSS Transactions on Power Electronics and Applications, Vol. 2, No. 3,
        September 2017.

[3]     L. Huber, Y. Jang and M. M. Jovanovic, "Performance Evaluation of Bridgeless
        PFC Boost Rectifiers," IEEE Transactions on Power Electronics, vol. 23, no. 3, pp.
        1381-1390, May 2008.

[4]     A. Q. Huang, "Wide bandgap (WBG) power devices and their Impacts on power
        delivery systems," in 2016 IEEE International Electron Devices Meeting (IEDM),
        San Francisco, CA, 2016, pp. 20.1.1-20.1.4.

[5]     E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power
        devices and GaN Converter design challenges," in IEEE Journal of Emerging and
        Selected Topics in Power Electronics, vol. 4, no. 3, pp. 707-719, Sept. 2016.

[6]     F. C. Lee, Q. Li, Z. Liu, Y. Yang, C. Fei and M. Mu, "Application of GaN devices
        for 1 kW server power supply with integrated magnetics," CPSS Transactions on
        Power Electronics and Applications, vol. 1, no. 1, pp. 3-12, Dec. 2016.

[7]     L. Zhou, Y. Wu, J. Honea, and Z. Wang, "High-efficiency true bridgeless totem pole
        PFC based on GaN HEMT: Design challenges and cost-effective solution," in

Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2015, pp. 1-8.

[8]  E. Persson, "How 600 V GaN transistors improve power supply efficiency and density," Power Electron. Eur., no. 2, pp. 21-24, Mar. 2015.

[9]  E. Persson, "Practical application of 600 V GaN HEMTs in power electronics," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Mar. 2015.

[10] Dusmez, Serkan. "Designing a 99% Efficient Totem Pole PFC with GaN." TI Training, 9 July 2020, training.ti.com/designing-99-efficient-totem-pole-pfc-gan.

[11] K. Ding, Y. Zhang, J. Liu, X. Cheng, P. Zeng and Y. Huang, "Single-Phase AC-DC Buck PFC Converter Based on Flying-Capacitor Topology with Active Power Decoupling Control," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 2885-2889, doi: 10.1109/ECCE.2018.8558365.

[12] Serban, Ioan. (2015). Power Decoupling Method for Single-Phase H-Bridge Inverters With No Additional Power Electronics. IEEE Transactions on Industrial Electronics. 62. 4805-4813. 10.1109/TIE.2015.2399274.

[13] Nguyen, Hoang Vu and Dong-Choon Lee. "Single-phase multifunctional onboard battery chargers with active power decoupling capability." 2018 IEEE Applied Power Electronics Conference and Exposition (APEC) (2018): 3434-3439.

[14] M. Metry, M. Kim and R. S. Balog, "A Hill-Climbing Optimization Approach for Closed-Loop Auto-Tuning of the Grid-Connected Ripple-Port Inverters," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 1-6.

[15]  T. Shimizu, T. Fujita, G. Kimura and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," in IEEE Transactions on Industrial Electronics, vol. 44, no. 4, pp. 447-455, Aug. 1997, doi: 10.1109/41.605618.

[16]  Sun, Yao & Su, Mei & Han, Hua & Wenjing, Xiong & Liu, Yonglu. (2015). Single-phase current source converter with power decoupling capability using a series-connected active buffer. IET Power Electronics. 8. 10.1049/iet-pel.2014.0068.

[17]  Li, Hongbo & Zhang, Kai & Zhao, Hui & Shengfang, Fan & Xiong, Jian. (2013). Active Power Decoupling for High-Power Single-Phase PWM Rectifiers. IEEE Transactions on Power Electronics. 10.1109/TPEL.2012.2208764.

[18]  Morsy, Ahmed & Enjeti, Prasad. (2016). Comparison of Active Power Decoupling Methods for High Power Density Single Phase Inverters Using Wide band Gap FETS for Google Little Box Challenge. IEEE Journal of Emerging and Selected Topics in Power Electronics. 4. 10.1109/JESTPE.2016.2573262.

[19]  "Snap-In Aluminum Electrolytic Capacitors" KEMET, E. (2020). Datasheet. Retrieved 2020, from

https://www.mouser.com/datasheet/2/212/KEM_A4020_ALC10-1103920.pdf

[20]  "Metallized Polypropylene Film Capacitors (MKP) B32754" TDK, E. (2019). Retrieved 2020, from

https://www.tdk-electronics.tdk.com/inf/20/20/ds/MKP_B32754_758.pdf

[21]  "Metallized Polypropylene Film Capacitors (MKP) B32774" TDK, E. (2019). Retrieved 2020, from

https://www.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/MKP_B32774_778.pdf

[22] "GaN Evaluation Board TDTTP2500P100-KIT 2.5kW PFC." Transphorm, 2017,

www.transphormusa.com/en/evaluation-kit/tdttp2500p100-kit/.

APPENDIX


HARDWARE DSP CONFIGURATION WITH CCS C CODE

The c code mentioned in this appendix is generated by PSIM code generation tool. It is used on Code Composer Studio to program and configure the Digital Signal Processor of the hardware components.

```
/*******************************************************************
***********
// This code is created by SimCoder Version 12.0.2 for F2837x Hardware Target
//
// SimCoder is copyright by Powersim Inc., 2009-2019
//
// Date: September 23, 2020 16:28:32
*******************************************************************************
***********/
#include        <math.h>
#include        "PS_bios.h"
#defineGetCurTime() PS_GetSysTimer()
#definePWM_IN_CHECK    // To lower PWM value setting time, comment out this line
if PWM duty cycle values are strictly limited in the range.




interrupt void Task();


#pragma DATA_SECTION(PSK_SysClk, "copysections")
const Uint16 PSK_SysClk = 200;  // MHz
extern  DefaultType    fGblAfter_Filter;
extern  DefaultType    fGblcb_phase1;
extern  DefaultType    fGblVcb_mag1;
extern  DefaultType    fGblVcb_sig;
extern  DefaultType    fGblVab_mag1;
extern  DefaultType    fGblVcb5;
extern  DefaultType    fGblVSVA4;
extern  DefaultType    fGblBefore_Filter;
extern  DefaultType    fGblVSVA12;
extern  DefaultType    fGblAfter_Filter_shift;
extern  DefaultType    fGblV2;
extern  DefaultType    fGblV1;
extern  DefaultType    fGblV5;
extern  DefaultType    fGblV6;
extern  DefaultType    fGblI_angle_1;
```

```
DefaultType    fGblAfter_Filter = 0;
DefaultType    fGblcb_phase1 = 0;
DefaultType    fGblVcb_mag1 = 0;
DefaultType    fGblVcb_sig = 0;
DefaultType    fGblVab_mag1 = 0;
DefaultType    fGblVcb5 = 0;
DefaultType    fGblVSVA4 = 0;
DefaultType    fGblBefore_Filter = 0;
DefaultType    fGblVSVA12 = 0;
DefaultType    fGblAfter_Filter_shift = 0;
DefaultType    fGblV2 = 0;
DefaultType    fGblV1 = 0;
DefaultType    fGblV5 = 0;
DefaultType    fGblV6 = 0;
DefaultType    fGblI_angle_1 = 0;
interrupt void Task()
{
        DefaultType    fMUX21, fCOMP3, fSUM1, fS3, fSUM3, fP3, fABS3, fMULT2,
fABS4;
        DefaultType    fZOH3, fF2837x_ADC1_1, fS2, fSUM4, fZOH2,
fF2837x_ADC1_2, fVCC6;
        DefaultType    fC2, fP1, fP24, fMULT5, fSIN3, fSQ2, fP11, fMULT4, fVad,
fSQ3;
        DefaultType    fSUMP9, fPOW2, fPOW1, fSUMP8, fP16, fATAN22, fP13, fS6,
fS5;
        DefaultType    fBW_30, fP14, fSUM5, foffset1, fZOH1, fF2837x_ADC1, fC15;

        ADC_CLR(0) = 1<<(1-1);
        CPU_PIEACK |= M__INT1;

        fC15 = (-(135.0));
        fF2837x_ADC1 = ADC_RESULT(0, 0) * (1.0 * 3.3 / 4096);
        fZOH1 = fF2837x_ADC1;
        foffset1 = 2.5;
        fSUM5 = fZOH1 - foffset1;
        fP14 = fSUM5 * 12;
        {
                static    DefaultType fIn[2] = {0, 0}, fOut[2] = {0, 0};
                fBW_30 = 0.000942 * fP14 + 0 * fIn[0] - (-(1.998103)) * fOut[0] + (-
(0.000942)) * fIn[1] - 0.998117 * fOut[1];
                fIn[1] = fIn[0];
                fIn[0] = fP14;
                fOut[1] = fOut[0];
                fOut[0] = fBW_30;
```

```
        }
#ifdef _DEBUG
        fGblAfter_Filter = fBW_30;
#endif


        {
                static   DefaultType fOutVal = 0.0;
                const DefaultType b0 =
(1.0*1.0)/100.0E3/(1.0/(2*3.14159*60.0)+1.0/100.0E3);
                const DefaultType a1 = -
1.0/(2*3.14159*60.0)/(1.0/(2*3.14159*60.0)+1.0/100.0E3);
                fS5 = b0 * fBW_30 - a1 * fOutVal;
                fOutVal = fS5;
        }
        {
                static   DefaultType fOutVal = 0.0;
                const DefaultType b0 =
(1.0*1.0)/100.0E3/(1.0/(2*3.14159*60.0)+1.0/100.0E3);
                const DefaultType a1 = -
1.0/(2*3.14159*60.0)/(1.0/(2*3.14159*60.0)+1.0/100.0E3);
                fS6 = b0 * fS5 - a1 * fOutVal;
                fOutVal = fS6;
        }
        fP13 = fS6 * 2;
        fATAN22 = atan2(fP13, fBW_30);
        fP16 = fATAN22 * (180.0/3.14159);
        fSUMP8 = fC15 + fP16;
#ifdef _DEBUG
        fGblcb_phase1 = fSUMP8;
#endif
        fPOW1 = 1 * pow(fP13, 2);
        fPOW2 = 1 * pow(fBW_30, 2);
        fSUMP9 = fPOW1 + fPOW2;
        fSQ3 = sqrt(fSUMP9);
        fVad = sqrt(2.0)*230.0;
        fMULT4 = fSQ3 * fVad;
        fP11 = fMULT4 * (1.0/(((100.0E-6*2.0)*3.14159)*60.0));
        fSQ2 = sqrt(fP11);
#ifdef _DEBUG
        fGblVcb_mag1 = fSQ2;
#endif
        fSIN3 = sin(fSUMP8 * (3.14159265 / 180.));
        fMULT5 = fSQ2 * fSIN3;
#ifdef _DEBUG
        fGblVcb_sig = fMULT5;
#endif
```

```c
#ifdef _DEBUG
        fGblVab_mag1 = fSQ3;
#endif
#ifdef _DEBUG
        fGblVcb5 = fSIN3;
#endif
        fP24 = fMULT5 * (1.0/390.0);
#ifdef _DEBUG
        fGblVSVA4 = fP24;
#endif
#ifdef _DEBUG
        fGblBefore_Filter = fP14;
#endif
        fP1 = -fP24;
#ifdef _DEBUG
        fGblVSVA12 = fP1;
#endif
#ifdef _DEBUG
        fGblAfter_Filter_shift = fP13;
#endif
        fC2 = 1;
        fVCC6 = 1;
        fF2837x_ADC1_2 = ADC_RESULT(0, 2) * (1.0 * 3.3 / 4096);
        fZOH2 = fF2837x_ADC1_2;
        fSUM4 = fVCC6 - fZOH2;
        {       // backward Euler
                static DefaultType out_A = 0.0;
                fS2 = out_A + (1.29514/((738.913E-6)*100000L)) * fSUM4;
                fS2 = (fS2 < (-(10000.0))) ? (-(10000.0)) : ((fS2 > 10000.0) ? 10000.0 :
fS2);
                out_A = fS2;
                fS2 += 1.29514 * fSUM4;
                fS2 = (fS2 < (-(10000.0))) ? (-(10000.0)) : ((fS2 > 10000.0) ? 10000.0 :
fS2);
        }
        fF2837x_ADC1_1 = ADC_RESULT(0, 1) * (1.0 * 3.3 / 4096);
        fZOH3 = fF2837x_ADC1_1;
        fABS4 = fabs(fZOH3);
        fMULT2 = fS2 * fABS4;
        fABS3 = fabs(fZOH1);
        fP3 = fABS3 * (1.0/2.5);
        fSUM3 = fMULT2 - fP3;
        {       // backward Euler
                static DefaultType out_A = 0.0;
                fS3 = out_A + ((613.81E-3)/((46.2143E-6)*100000L)) * fSUM3;
                fS3 = (fS3 < 0.02) ? 0.02 : ((fS3 > 0.98) ? 0.98 : fS3);
```

```c
                out_A = fS3;
                fS3 += (613.81E-3) * fSUM3;
                fS3 = (fS3 < 0.02) ? 0.02 : ((fS3 > 0.98) ? 0.98 : fS3);
        }
#ifdef  _DEBUG
        fGblV2 = fS3;
#endif

        fSUM1 = fC2 - fS3;
#ifdef  _DEBUG
        fGblV1 = fSUM1;
#endif
#ifdef  _DEBUG
        fGblV5 = fF2837x_ADC1;
#endif
#ifdef  _DEBUG
        fGblV6 = fZOH1;
#endif
        fCOMP3 = (fZOH3 > 0) ? 1 : 0;
        fMUX21 = (fCOMP3 > 0.5) ? fSUM1 : fS3;
#ifdef  _DEBUG
        fGblI_angle_1 = fP16;
#endif
        // Start of changing PWM3(1ph) registers
        // Set Duty Cycle
        {
                DefaultType _val = __fsat(fP1, 2 + (-(1.0)), (-(1.0)));
                _val = PWM_TBPRD(3) * ((_val - (-(1.0))) * (1.0 / 2));
                PWM_CMPA(3) = (int)_val;
        }
        // End of changing PWM3(1ph) registers
        // Start of changing PWM2(1ph) registers
        // Set Duty Cycle
        {
                DefaultType _val = __fsat(fP24, 2 + (-(1.0)), (-(1.0)));
                _val = PWM_TBPRD(2) * ((_val - (-(1.0))) * (1.0 / 2));
                PWM_CMPA(2) = (int)_val;
        }
        // End of changing PWM2(1ph) registers
        // Start of changing PWM1(1ph) registers
        // Set Duty Cycle
        {
                DefaultType _val = __fsat(fMUX21, 1 + 0.5, 0.5);
                _val = ((Uint32)(PWM_TBPRD(1))+1) * ((_val - 0.5) * (1.0 / 1));
                PWM_CMPA(1) = (int)_val;
        }
```

```
        // End of changing PWM1(1ph) registers
}


void Initialize(void)
{
        PS_SysInit(2, 20);
        PS_PwmStartStopClock(0);   // Stop Pwm Clock
        PS_TimerInit(0, 0);
        {
          int i, preAdcNo = -1;
          /* PST_AdcAttr: Adc No., Channel No., Soc No., Trig Src,
SampleTime(clock) */
          const PST_AdcAttr aryAdcInit[3] = {
                        {0, 0, 0, ADCTRIG_PWM2, 2000},
                        {0, 1, 1, ADCTRIG_PWM2, 2000},
                        {0, 2, 2, ADCTRIG_PWM2, 2000}};
          const PST_AdcAttr *p = aryAdcInit;
          for (i = 0; i < 3; i++, p++) {
            if (preAdcNo != p->nAdcNo) {
              PS_AdcInit(p->nAdcNo);
              preAdcNo = p->nAdcNo;
            }
            PS_AdcSetChn(p->nAdcNo, p->nChnNo, p->nSocNo, p->nTrigSrc, p-
>nWindSz);
          }
        }

        PS_PwmInit(1, 0, 0, 1.e6/(100000*1.0), ePwmUseA, ePwmStartHigh1,
ePwmComplement, HRPWM_DISABLE);   // pwmNo, pinSel, waveType, period,
outtype, PwmA, PWMB, UseHRPwm
        PS_PwmSetDeadBand(1, 0, 2, 3, 0, 0.1, 0.1);
        PS_PwmSetIntrType(1, ePwmNoAdc, 1, 0);
        PS_PwmSetTripAction(1, eTzHiZ, eTzHiZ);
        PWM_CMPA(1) = (0 - 0.5) / (1.0 * 1) * PWM_TBPRD(1);
        PSM_PwmStart(1);

        PS_PwmInit(2, 0, 1, 1.e6/(100000*1.0), ePwmUseAB, ePwmStartHigh1,
ePwmComplement, HRPWM_DISABLE);   // pwmNo, pinSel, waveType, period,
outtype, PwmA, PWMB, UseHRPwm
        PS_PwmSetDeadBand(2, 0, 2, 3, 0, 0.1, 0.1);
        PS_PwmSetIntrType(2, ePwmIntrAdc, 1, 0);
        PS_AdcSetIntr(0, 1, 2, Task); // AdcNo, IntrNo, SocNo, Interrupt Vector
        PS_PwmSetTripAction(2, eTzHiZ, eTzHiZ);
        PWM_CMPA(2) = (0 - (-(1.0))) / (1.0 * 2) * PWM_TBPRD(2);
        PSM_PwmStart(2);
```

```
        PS_PwmInit(3, 0, 1, 1.e6/(100000*1.0), ePwmUseAB, ePwmStartHigh1,
ePwmComplement, HRPWM_DISABLE);   // pwmNo, pinSel, waveType, period,
outtype, PwmA, PWMB, UseHRPwm
        PS_PwmSetDeadBand(3, 0, 2, 3, 0, 0.1, 0.1);
        PS_PwmSetIntrType(3, ePwmNoAdc, 1, 0);
        PS_PwmSetTripAction(3, eTzHiZ, eTzHiZ);
        PWM_CMPA(3) = (0 - (-(1.0))) / (1.0 * 2) * PWM_TBPRD(3);
        PSM_PwmStart(3);

        PS_PwmStartStopClock(1);   // Start Pwm Clock
}


void main()
{
        Initialize();
        PSM_EnableIntr();   // Enable Global interrupt INTM
        PSM_EnableDbgm();
        for (;;) {
        }
}
```