

MODEL PREDICTIVE CONTROL TECHNIQUE OF MULTILEVEL  
INVERTER FOR PV APPLICATIONS

A Dissertation

by

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## ABSTRACT

Renewable energy sources, such as solar, wind, hydro, and biofuels, continue to gain popularity as alternatives to the conventional generation system. The main unit in the renewable energy system is the power conditioning system (PCS). It is highly desirable to obtain higher efficiency, lower component cost, and high reliability for the PCS to decrease the levelized cost of energy. This suggests a need for new inverter configurations and controls optimization, which can achieve the aforementioned needs. To achieve these goals, this dissertation presents a modified multilevel inverter topology for grid-tied photovoltaic (PV) system to achieve a lower cost and higher efficiency comparing with the existing system. In addition, this dissertation will also focus on model predictive control (MPC) which controls the modified multilevel topology to regulate the injected power to the grid. A major requirement for the PCS is harvesting the maximum power from the PV. By incorporating MPC, the performance of the maximum power point tracking (MPPT) algorithm to accurately extract the maximum power is improved for multilevel DC-DC converter. Finally, this control technique is developed for the quasi-z-source inverter (qZSI) to accurately control the DC link voltage, input current, and produce a high quality grid injected current waveform compared with the conventional techniques.

This dissertation presents a modified symmetrical and asymmetrical multilevel DC-link inverter (MLDCLI) topology with less power switches and gate drivers. In addition, the MPC technique is used to drive the modified and grid connected MLDCLI. The performance of the proposed topology with finite control set model predictive control (FCS-MPC) is verified by simulation and experimentally. Moreover, this dissertation introduces predictive control to achieve maximum power point for grid-tied PV system to quicken the response by predicting the error before the switching signal is applied to the converter. Using the modified technique ensures the

system operates at maximum power point which is more economical. Thus, the proposed MPPT technique can extract more energy compared to the conventional MPPT techniques from the same amount of installed solar panel.

In further detail, this dissertation proposes the FCS-MPC technique for the qZSI in PV system. In order to further improve the performance of the system, FCS-MPC with one step horizon prediction has been implemented and compared with the classical PI controller. The presented work shows the proposed control techniques outperform the ones of the conventional linear controllers for the same application. Finally, a new method of the parallel processing is presented to reduce the time processing for the MPC.

## DEDICATION

To my father's soul.

To my mother.

To my wife (Alaa), my daughter (Lyan), and my son (Hamza).

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# TABLE OF CONTENTS

ABSTRACT.....	ii
DEDICATION.....	iv
ACKNOWLEDGEMENTS.....	v
CONTRIBUTORS AND FUNDING SOURCES.....	vi
TABLE OF CONTENTS.....	vii
LIST OF FIGURES.....	ix
LIST OF TABLES.....	xiv
1. INTRODUCTION.....	1
1.1. Why PV Systems?.....	1
1.2. Multilevel Inverter With Model Predictive Control for PV Applications.....	3
1.3. PV System Configurations.....	4
1.4. Power Conditioning System (PCS) Configuration.....	7
1.5. Dissertation Outline.....	9
2. A MODEL PREDICTIVE CONTROL FOR ASYMMETRIC FOLDED-SWITCHING GRID-CONNECTED MULTILEVEL INVERTER.....	11
2.1. Introduction.....	11
2.2. The Modified Multilevel Inverter Topology.....	14
2.3. A Comparison Between the Proposed Topology and the Conventional Topologies.....	21
2.4. Model Predictive Control Principle.....	29
2.5. Discrete Model of the System.....	30
2.6. Simulation and Experimental Results.....	33
2.7. Conclusion.....	39
3. EFFICIENT MAXIMUM POWER POINT TRACKING USING MODEL PREDICTIVE CONTROL FOR MULTILEVEL DC-DC CONVERTER.....	40
3.1. Modified Maximum Power Point Tracking by Model Predictive Control.....	40
5.1. The Principle of Predictive Model-Based Controller.....	43
5.2. Analysis of Multilevel Boost Converter.....	45
5.3. Voltage Oriented Maximum Power Point Tracking by Model Predictive Control.....	50
5.4. Results & Discussion.....	55
5.5. Efficiency Analysis.....	62
5.6. Conclusion.....	67

4. MAXIMUM POWER POINT TRACKING OF GRID-TIED PHOTOVOLTAIC SYSTEMS .....	69
4.1. Description of the Complete System.....	70
4.2. Model Predictive Control of the System .....	72
4.2.1. Predictive Maximum Power Point Tracking.....	72
4.2.1. Predictive Current Control.....	73
4.3. Results and Discussion.....	75
4.4. Conclusion.....	82
5. HIGH PERFORMANCE PREDICTIVE CONTROL OF QUASI IMPEDANCE SOURCE INVERTER .....	83
5.1. Traditional Feedback Controller for QZSI.....	83
5.2. Operational Principles of QZSI.....	87
5.3. System Modeling and Analysis.....	87
5.4. Proposed Predictive Control for QZSI.....	94
5.5. Simulation Results .....	99
5.6. Experimental Results .....	106
5.7. Conclusion .....	112
6. FPGA-BASED PARALLEL PROCESSING OF MPC FOR QZS SIC INVERTER.....	114
6.1. Introduction .....	115
6.2. MPC Algorithm for QZSI .....	116
6.2.1. Algorithm Brief Description .....	116
6.2.2. Mathematical Framework.....	118
6.2.3. Conventional Sequential Processing .....	119
6.3. Parallel Processing and FPGA Implementation .....	120
6.3.1. Proposed Parallel Processing.....	120
6.3.2. FPGA-Based Digital Design and Implementations .....	121
6.4. Experimental Investigation and Discussion.....	126
6.4.1. Experimental Investigation.....	126
6.4.2. Discussion .....	129
6.5. Conclusion .....	131
7. CONCLUSION AND FUTURE WORK.....	132
7.1. Conclusion .....	132
7.2. Future work.....	133
REFERENCES .....	134



## LIST OF FIGURES

Figure 1: Annual growth rates of electricity production between 1990 and 2016 in OECD countries [6] (Adapted with permission from International Energy Agency [6]).....	1
Figure 2: Cost of onshore wind and PV projects in 58 non-Economic Cooperation & Development (OECD) countries [9].....	2
Figure 3: PV system cost benchmark summary [10] (Adapted with permission from The National Renewable Energy Laboratory [10]).....	3
Figure 4: Three phase grid-tied central inverter .....	5
Figure 5: Single phase grid-tied string inverter .....	6
Figure 6: Single phase grid-tied module inverter .....	6
Figure 7: Three phase multistring inverter.....	7
Figure 8: Traditional PCS for PV system .....	8
Figure 9: Classification of multilevel modulation methods.....	13
Figure 10: Symmetrical or asymmetrical single phase multilevel inverter .....	15
Figure 11: The proposed three phase multilevel topology with (N-1) level generation and one polarity generation per phase .....	17
Figure 12: The proposed single phase multilevel cascaded H-bridge topology with (xN-x) level generation and x polarity generation .....	18
Figure 13: The proposed three phase multilevel cascaded H-bridge topology with (xN-x) level generation and x polarity generation.....	19
Figure 14: States of the switches for seven level output voltage.....	20
Figure 15: Cascaded Multilevel inverter.....	22
Figure 16: Neutral-point clamped multilevel inverter .....	23
Figure 17: Three level flying capacitor multilevel inverters .....	24
Figure 18: Reversing voltage multilevel inverter .....	25
Figure 19: T-type multilevel inverter.....	26
Figure 20: Multilevel module multilevel inverter.....	26

Figure 21: Variation of the number of components with the number of levels for the single phase MLI .....	27
Figure 22: Variation of the number of components with the number of levels for three phase MLI .....	28
Figure 23: Variation of the total stress voltage with the number of levels for the three phase MLI .....	28
Figure 24: Block diagram of the principal MPC .....	30
Figure 25: Schematic illustrating prediction observation for the injected output current .....	33
Figure 26: The simulation results for the injected grid current and the grid voltage with 0.8KW reference power .....	35
Figure 27: The simulation results with a step change in the reference output power from 0.8KW to 1KW .....	36
Figure 28: THD as a function of output power and input voltages with 0.5mH inductor .....	36
Figure 29: THD as a function of output power and inductive filters (Lf) with base input voltage.....	37
Figure 30: Real-time results for multilevel output voltage, output current and grid voltage with a step change in the reference output power from 0.5KW to 1KW .....	38
Figure 31: Zoom of the multilevel output voltage, output current and grid voltage with a step change in the reference output power from 0.5KW to 1KW .....	38
Figure 32: Predictive model-based controller block diagram for maximum power point tracking. ....	45
Figure 33: Multilevel boost converter topology .....	47
Figure 34: Multilevel DC-DC converter when the switch is ON .....	47
Figure 35: Multilevel DC-DC converter when the switch is OFF .....	47
Figure 36: Effect of Equivalent Series Resistance (ESR) of capacitor, inductor, and switch turn on resistance (from top to bottom) on efficiency versus output power .....	51
Figure 37: Maximum power point tracking by MPC.....	52
Figure 38: I-V and P-V characteristics of the array .....	56

Figure 39: PV current Simulation results comparison of the MPC versus INC method under irradiance level change .....	57
Figure 40: PV voltage simulation results comparison of the MPC versus INC method under irradiance level change. ....	58
Figure 41: (From top to bottom) PV power by INC-MPPT, PV power, output voltage of the converter, irradiance level, and duty cycle of the converter switch by MPC-MPPT .	59
Figure 42: Experimental Setup .....	60
Figure 43: PV current, voltage, and power of MPC-MPPT .....	60
Figure 44: Zoomed in plot of PV current, voltage, and power by proposed MPC-MPPT when the step change in irradiance level at time 1.5 s occur.....	60
Figure 45: Output to input voltage ratio using MPC-MPPT.....	61
Figure 46: PV current, voltage, and power of INC-MPPT .....	61
Figure 47: Zoomed in plot of PV current, voltage, and power by proposed INC-MPPT when the step change in irradiance level at time 1.5 s occur.....	61
Figure 48: Output to input voltage ratio using INC-MPPT .....	62
Figure 49: MPC-MPPT control effectiveness, converter efficiency, solar array simulator power, and converter output power for solar irradiance of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> .....	63
Figure 50: INC-MPPT control effectiveness, converter efficiency, solar array simulator power, and converter output power for solar irradiance of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> .....	65
Figure 51: Comparison of INC and MPC control effectiveness and converter efficiency for solar irradiance levels of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> .....	65
Figure 52: Solar array simulator (SAS) voltage and current ripple for solar irradiance of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> .....	66
Figure 53: Output voltage and current ripple for solar irradiance of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> ...	66
Figure 54: The contour plot of the MPC-MPPT control effectiveness versus the disturbances in load for solar irradiance of 100 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> , the 100% load disturbance is the nominal value of the load .....	67
Figure 55: General schematic of the system and proposed model predictive control for grid connected PV system .....	71

Figure 56: Prediction of PV array side current observation .....	73
Figure 57: MPC maximum power point tracking procedure .....	74
Figure 58: Prediction of grid side current observation .....	75
Figure 59: Model predictive control of the multilevel inverter .....	76
Figure 60: I-V and P-V characteristics of the PV array .....	77
Figure 61: Simulation results of MPPT .....	78
Figure 62: Simulation result of grid side .....	80
Figure 63: Experimental validation of the control algorithm by real-time implementation.....	81
Figure 64: Spectrum analysis of grid side current ( $i_{L2}$ ).....	82
Figure 65: Z-source/qZ-source inverter .....	84
Figure 66: The basic three equivalent operation modes for the qZSI.....	88
Figure 67: Voltage vectors for the qZSI .....	89
Figure 68: Illustration of the MPC method predicting the modelled for one-step and two-steps into the future .....	96
Figure 69: Flow chart of the MPC for the qZSI.....	97
Figure 70: Block diagram of the predictive control algorithm for qZSI.....	101
Figure 71: Block diagram of the traditional PI controller for qZSI.....	101
Figure 72: Proposed MPC controller for a step change in the reference output current at instance 200mS; from the top, three-phase output current, input current, DC-link voltage, and harmonic spectrum for the output current .....	103
Figure 73: Conventional PI controller for a step change in the reference output current at instance 200mS; from the top, three-phase output current, input current, DC-link voltage, and harmonic spectrum for the output current .....	104
Figure 74: The THD of the three-phase output current for the proposed MPC and PI controller .....	105
Figure 75: Simulation results for the load voltage van with a step change in the reference output current at instance 200mS.....	105

Figure 76: Simulation results for the effect of the load model error with 50% change reduction in the load inductance and load resistance at instance 200mS .....	105
Figure 77: The prototype of the qZSI inverter.....	107
Figure 78: Proposed MPC block diagram for the qZSI .....	108
Figure 79: The predictive model for the (a) output current, capacitor voltage and inductor current in (b) active state, (c) null state, and (d) shoot-through state. ....	109
Figure 80: Three-phase AC output current .....	110
Figure 81: Input voltage, Capacitor voltage and DC-link voltage.....	111
Figure 82: Input voltage, input current, capacitor voltage and DC-link voltage .....	111
Figure 83: Output current and capacitor voltage for a step-change in the reference output current .....	111
Figure 84: Steady state output current spectrum at 2.3A. The x-axis is harmonic number and the y-axis is percent of fundamental component of the current.....	112
Figure 85: An FPGA-based control scheme of a Quasi-Z-Source inverter .....	116
Figure 86: Locus diagram for prediction and observation of current $i_x$ .....	117
Figure 87: FPGA hardware architecture and drive synthesis flowchart of the proposed parallel-processed MPC algorithm .....	122
Figure 88: Digital design and implementation examples. ....	123
Figure 89: Experimental setup .....	127
Figure 90: Input voltage, capacitor voltage and DC-link voltage and inductor current .....	128
Figure 91: Input voltage, capacitor voltage and DC-link voltage and inductor current (zoomed) .....	128
Figure 92: Input voltage, inductor current, capacitor voltage, inductor current, and output current .....	129

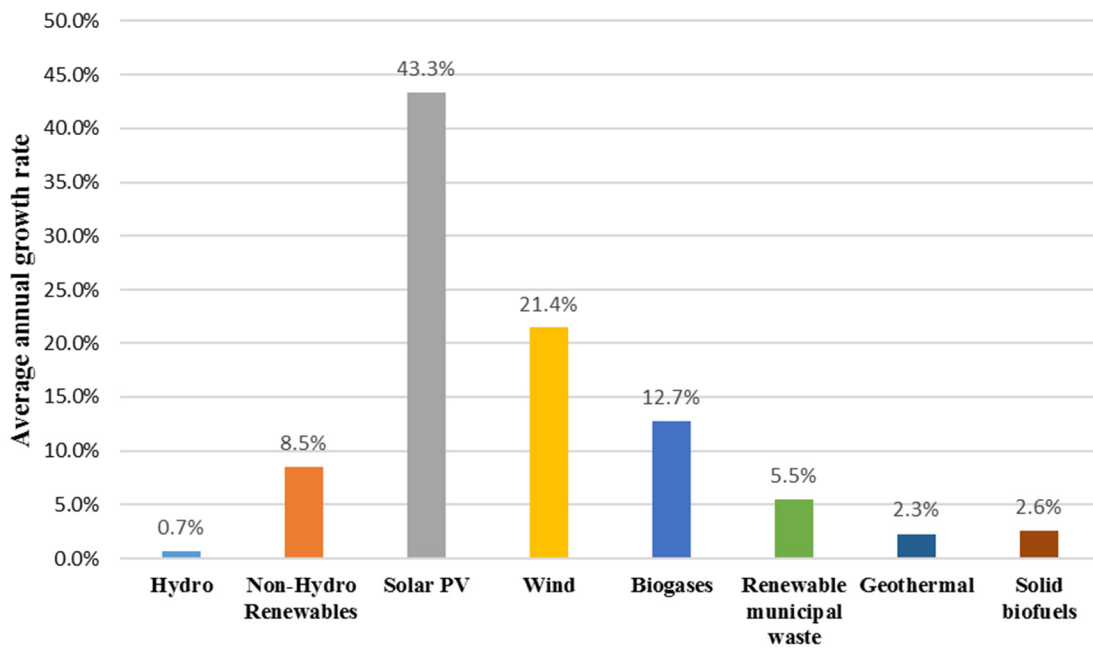
## LIST OF TABLES

Table 1: Switching state of the seven level multilevel output voltage .....	16
Table 2: Comparison of three-phase multilevel inverter .....	27
Table 3. The system parameters.....	34
Table 4. INC-MPPT versus MPC-MPPT comparison of step change dynamic performance (750 W/m <sup>2</sup> to 1000 W/m <sup>2</sup> ) and steady state performance (1000 W/m <sup>2</sup> ) .....	67
Table 5: Summary of output voltage levels as function of switching states.....	71
Table 6: The model-predictive equations of the capacitor voltage and inductor current for the three operating states .....	93
Table 7: qZSI Simulation System Parameters .....	98
Table 8: PI controller parameters.....	98
Table 9: The Overall System Parameters.....	127
Table 10: A number of previously-published FPGA-based implementations of MPC algorithms, compared with proposed work .....	130

# 1. INTRODUCTION

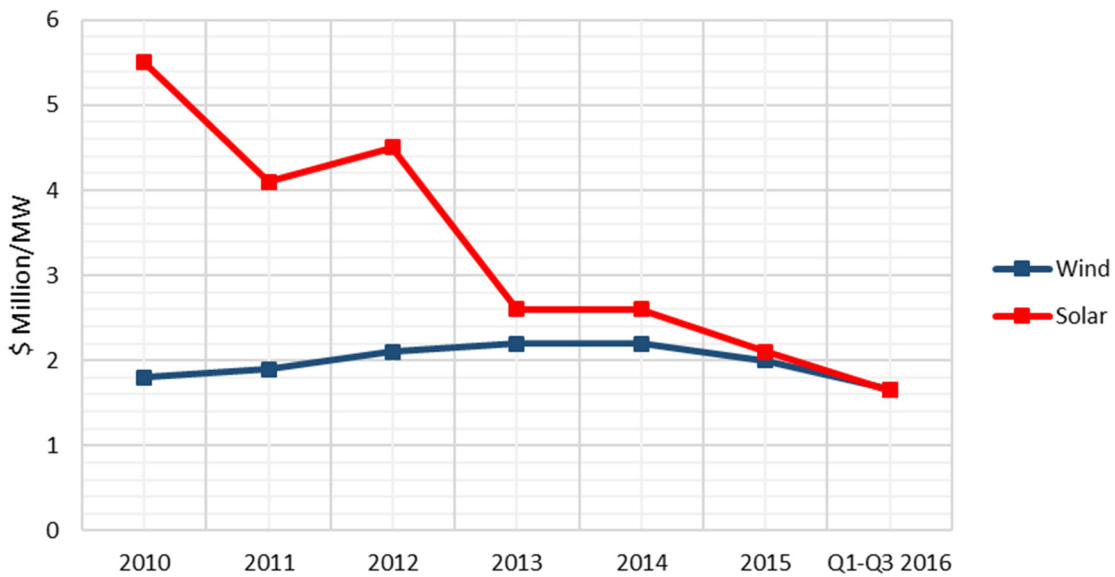
## 1.1. Why PV Systems?

Power generation from renewable energy sources has gained increased acceptance in recent years over the conventional resources like fossil fuels. These conventional resources are one of the leading cause of air pollution and the biggest source for global warming emission [1]. Renewable energy is a clean source, such that electric power can be generated without any impact on the environment [2]. The main types of this clean energy source are solar, wind, hydro, and biofuels [3, 4]. These sources are now well developed, widely used, and cost effective [5]. As shown in Figure 1, the highest average growth rate of electricity production in the organization for economic co-operation and development (OECD) countries is solar PV which increased from 0.0% in 1990 to 43.3% in 2016 [6].



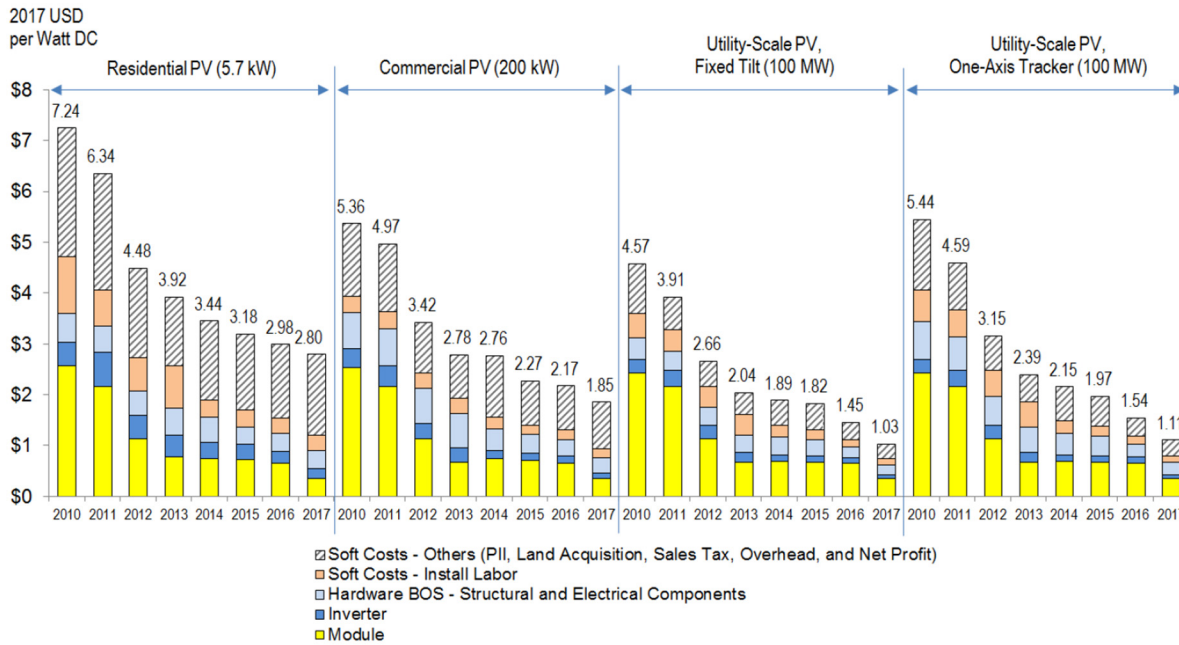
**Figure 1: Annual growth rates of electricity production between 1990 and 2016 in OECD countries [6] (Adapted with permission from International Energy Agency [6])**

Grid connected PV system has been grown during these decades which has led to an increase in the development of the grid-tied inverters. Currently, the main target of the research is to reduce the cost of the system, improve the efficiency, and make the solution more reliable to reduce the levelized cost of energy [7, 8]. In 2016, Bloomberg Technology announced that solar energy overtook wind energy by reducing the price of it to be less than the wind energy [9]. As shown in Figure 2, the cost of the PV project in 2010 was around \$5.5million/MW and reduced to \$1.65 million/MW in 2016. On the other hand, the cost of the wind energy project was \$1.8millions/MW in 2010 and it just decreased to \$1.66 millions/MW in 2016. In addition, Figure 3 shows the PV system cost benchmark summary for the residential, commercial, and utility-scale PV system. For the residential PV system, the cost for a module in 2011 was around \$2/Watt DC (yellow bar), but by 2017 the cost decreased to \$0.3/watt DC. In addition, the cost of the inverter (blue bar) was almost \$0.5/watt DC in 2011 and it decreased to less than \$0.2/watt DC [10].



**Figure 2: Cost of onshore wind and PV projects in 58 non-Economic Cooperation & Development (OECD) countries [9]**





**Figure 3: PV system cost benchmark summary [10] (Adapted with permission from The National Renewable Energy Laboratory [10])**

Figure 2 and Figure 3 show that the cost of the module and the inverter decrease tremendously from 2010 to 2016, which contributes to the decrease in the total cost of the system. Research is one of many reasons for the decrease in cost of PV system.

## 1.2. Multilevel Inverter with Model Predictive Control for PV Applications

DC-AC power converters is a key technology in many setup of conversion, generation, transmission, distribution, and conditioning. However, the converter (DC-DC, DC-AC, and AC-DC converters) is restricted by operational capacities because of limitations in active components from the physical characteristics of the switches in the converter [11-13]. Investigations have been carried out to develop new topologies to reduce the stresses on the components of the converters [14]. The main two aims are to increase the operating voltage and current of the converter. This research introduces new topologies called multilevel inverters. The advantages of multilevel topologies over the traditional inverters include a higher operation voltage than the rating voltage

of the components, staircase output waveforms which provides reduced harmonic profile, and lower the  $dv/dt$ . These advantages led these topologies to play a crucial role in renewable energy interconnection. In the other hand, these topologies greatly increase the number of electronics devices in the circuit [12]. This implies that more research has to be done to reduce the number of components in the system to minimize the cost and improve the efficiency. Nevertheless, these topologies need complex feedback to control the large number of electronic devices on it [15, 16].

Predictive control strategy has been applied on many power electronics converters in general and on multilevel inverter in particular [17-20]. The main advantages of this technique are that the concept is intuitive, supports multivariable case, non-linear model and any constrains can easily be considered. These advantages led this technique to be used in controlling a complex converter like a multilevel inverter [21-24].

### **1.3. PV System Configurations**

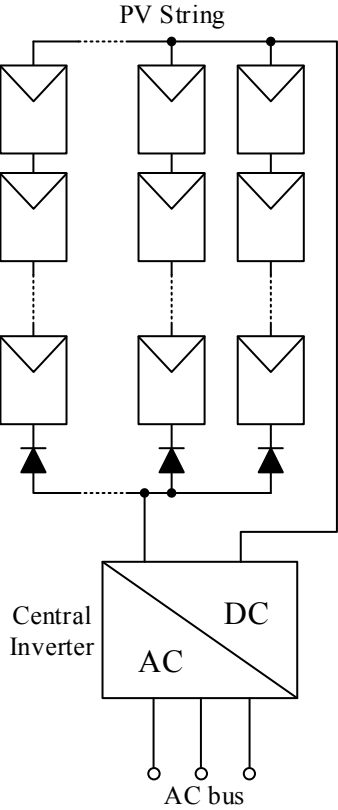
Four main configurations of the PV system families can be defined: (a) central structure, (b) string structure, (c) module structure, and (d) multistring structure [25-29]. Figures 4, 5, 6, and 7 shows these configurations of the PV system.

Figure 4 shows the central structure which is used for power plants where it offers a high efficiency with low cost [30]. The drawbacks of this system are as follows; there are mismatch losses between the PV modules due to the centralized maximum power point tracking (MPPT), losses due to the string diodes, and the reliability is low for this system.

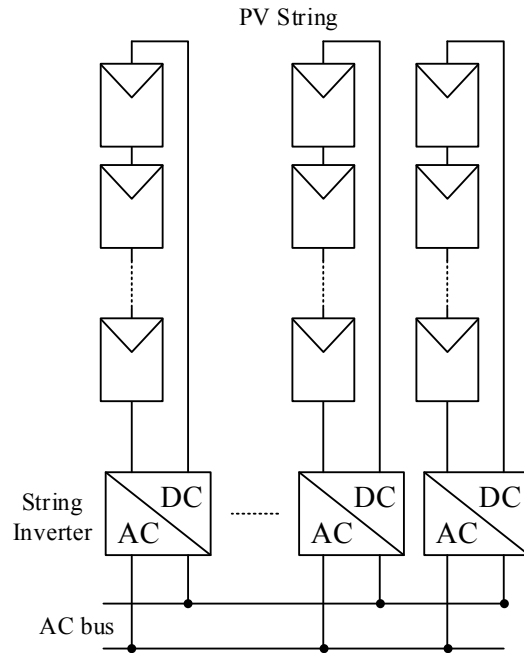
A string structure is designed for a low power range from 1 to 5 KW [31]. The main advantage for this structure is that the MPPT can be applied to each PV string individually [25]. As shown in Figure 5, a string of solar cells have been connected directly to an inverter where it

gives the ability to extract more power. Thus, the overall efficiency of string structure is better when compared with the central structure.

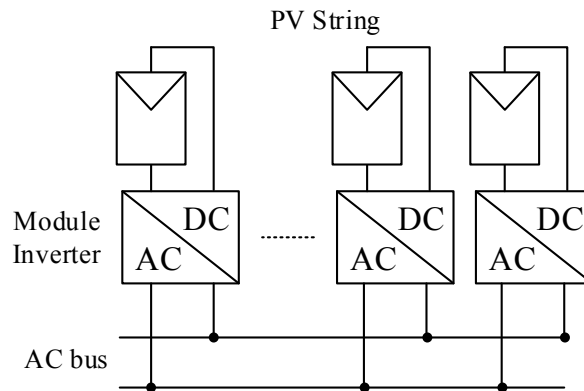
Figure 6 shows the module structure which integrates the inverter and the PV panel into one device. Thus, the module mismatch losses do not exist in this structure and this system can extract the maximum power very easily [32]. However, the module structure has some drawbacks. First, the integrated inverter needs more complex circuit topologies to achieve a high voltage boosting ratio, resulting in a low efficiency and high cost per watt [33, 34]. In addition, integrating the inverter with the PV module in one electrical device requires equal lifetimes for both of them.



**Figure 4: Three phase grid-tied central inverter**



**Figure 5: Single phase grid-tied string inverter**

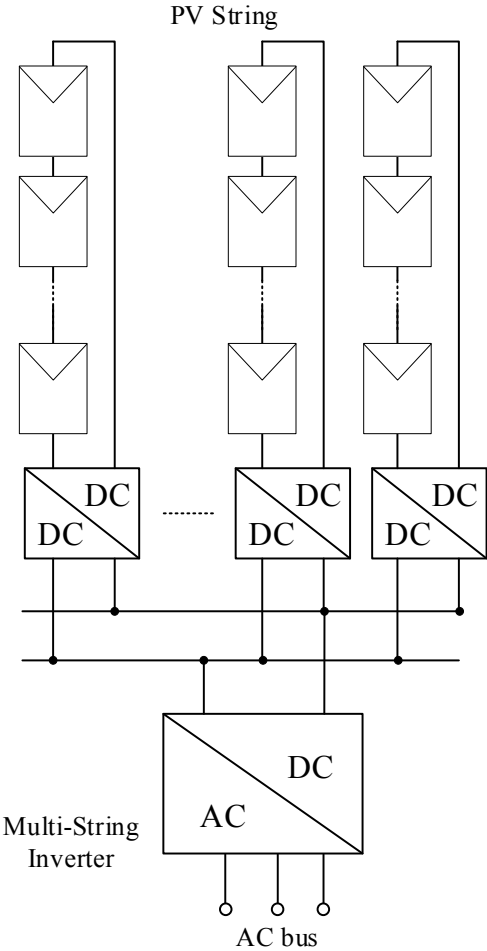


**Figure 6: Single phase grid-tied module inverter**

Unfortunately, the estimated lifespan of solar inverters is fifteen years which is far less than the lifespan of the PV which is around 25 years [35-37]. If the lifetime become equal, this structure will be very interesting because of their ease in use and installation [38].

For a high voltage PV system, multistring structure is preferred to be used. Each PV string has its own DC-DC converter [39, 40]. All these converters are connected in series then connected

to one inverter as shown in Figure 7. This approach combines the aspect of the module structure and the string structure. The main advantages are as following; individual MPPT controller for each string, cheaper and more efficient [41]. Unfortunately, the main disadvantage is that there are two stages in this structure which still limit the efficiency of the system. This existing drawbacks present challenges for controlling these two stages simultaneously [42].

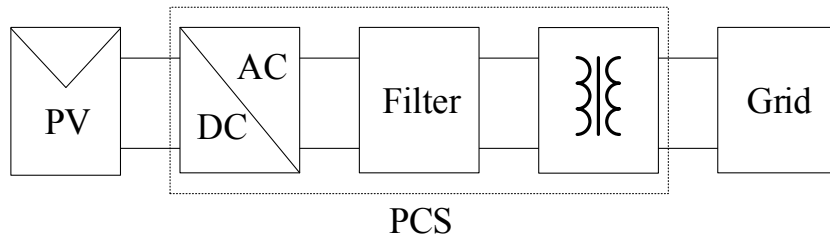


**Figure 7: Three phase multistring inverter**

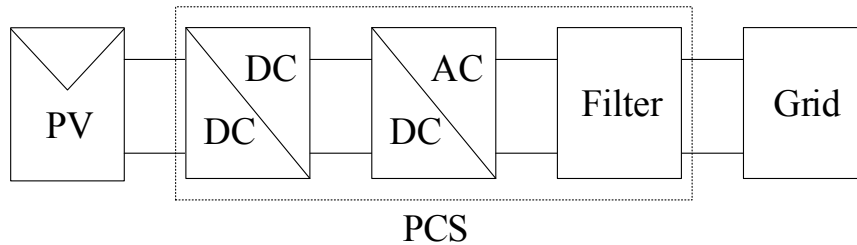
**1.4. Power Conditioning System (PCS) Configuration**

A power conditioning system works as the interface between the solar cell and the grid or the load. It is required to convert the DC output voltage of the solar cell to either AC in case of AC

grid 50/60 Hz or AC load, or DC with different voltage value in case of DC load or DC microgrid. In addition, the PCS should insure maximum power utilization of the PV module to improve the overall efficiency of the system. Figure 8 shows the most common PCS configuration for the PV system. In the system shown in Figure 8(a), a low frequency transformer is used between the inverter and the grid to provide isolation and to step up the output voltage of the inverter. Unfortunately, the low frequency transformer is associated with large volume, high cost and loud acoustic noise [43, 44]. So in order to eliminate the aforementioned drawbacks, a DC-DC converter has been introduced in this system to replace the transformer with it [44, 45]. Unfortunately, the cost of the DC-DC converter is still high [44].



(a) Transformer in the low frequency side to step up the output voltage



(b) DC-DC converter in the input side to step up the PV voltage

**Figure 8: Traditional PCS for PV system**

According to the aforementioned challenges, the work of this dissertation achieved the target of improving the efficiency and reducing the total cost of the PV system by proposing a new multilevel inverter topology. The new topology reduces the number of components in the inverter

and replaces the two stage multistring structure with one stage only. Meanwhile, an improved maximum power point tracking technique using model predictive control is proposed and tested to extract more energy from the PV. In addition, this dissertation proposes model predictive control technique for qZSI which can improve the performance of the system and make the PCS design simple and cost effective.

### **1.5. Dissertation Outline**

According to the strategy discussed in the previous section, the outline for this dissertation is as follows;

Chapter 2 presents a modified multilevel inverter which is used for grid connected PV system. Meanwhile, a comparison between the modified topology and conventional topologies is demonstrated. Moreover, a MPC technique for the new topology is presented in this chapter. Real time implementation is carried out to demonstrate the advantages of this topology.

Chapter 3 presets an efficient MPPT by using MPC for multilevel DC-DC converter which is used to interface with the proposed topology which is presented in chapter 2. This topology is built in the laboratory and the results are presented.

Chapter 4 discusses the combination between the proposed multilevel inverter which is presented in chapter 2 and the multilevel DC-DC converter which is presented in chapter 3. Simulation and experimental results are demonstrated and discussed.

Chapter 5 proposes MPC for qZSI. A complete scheme of the system is presented and explained. In addition, a survey of the conventional techniques is demonstrated and discussed. A comparison between MPC and PI controller is presented in the simulation. Finally, experimental results are presented.

Chapter 6 proposes a solution to reduce the calculation time of MPC by using FPGA board. A parallel processing is investigated and presented. Moreover, a comparison between the proposed technique and the conventional techniques is discussed in this chapter. Then finally, experimental results are presented.

Chapter 7 concludes the work that is done in this dissertation and evaluates the contribution of this work. Possible future work is also described in this section.



## 2. A MODEL PREDICTIVE CONTROL FOR ASYMMETRIC FOLDED-SWITCHING GRID-CONNECTED MULTILEVEL INVERTER\*

The development of renewable energy power generation is expanding. To harness this energy efficiently and convert it to usable form at high quality, highly efficiency and reliable power electronics devices are required. Multilevel inverters can produce high quality sinusoidal waveforms with a small filter size [46-50]. They offer low voltage stress on the components as well as lower harmonic distortion for the output voltage and current. However, conventional multilevel inverters have some disadvantages such as bigger size, higher number of components (switches and sources) and gate drivers, and higher control complexity comparing with the two level inverter [12, 51-53]. To overcome these disadvantages, this chapter explores symmetrical and asymmetrical multilevel DC-link inverter (MLDCLI) topology with reduced number of power semiconductor switches and associated gate drivers. In addition, a Finite Control Set Model Predictive Control (FCS-MPC) is studied and used to drive the grid connected modified MLDCLI. The performance of the modified topology with FCS-MPC is verified by simulation and experimentally. Seven level symmetrical multilevel converter has been tested using dSPACE 1007.

### 2.1. Introduction

Many industrial applications require power electronics converters to process power at the megawatt level. Due to several practical limitations including the lack of high-voltage semiconductor switches and the challenges of passive filters design, the multilevel inverter was

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\* Portions of this chapter have been previously published in M. Mosa, R. S. Balog, and H. Abu-Rub, "A Modified Symmetric and Asymmetric Multilevel Power Inverter with Reduced Number of Power Switches," in IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2017, pp. 488-493, © 2017 IEEE.

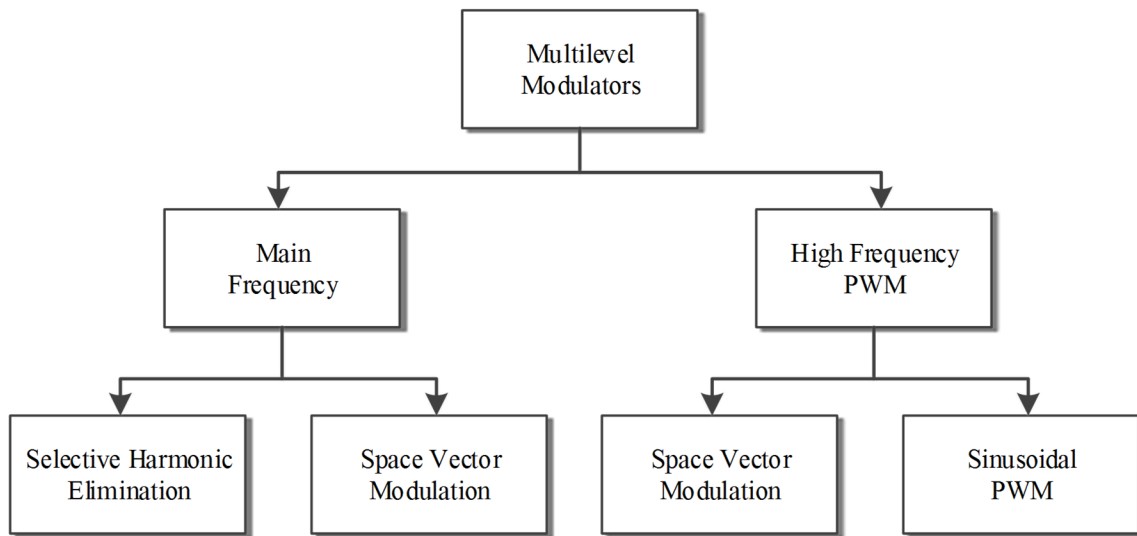
introduced. Multilevel inverters are used in many industrial applications such as AC drives, static reactive power compensation (SVC), HVDC, hybrid vehicle and renewable energy [54-56]. There are several advantages of multilevel topologies over the traditional two level inverters such as the output voltage is higher than the rating voltage for the components, having staircase output waveforms reduces harmonic profile, and alleviating the  $dv/dt$  [57]. Furthermore, multilevel inverters operate at low switching frequency which leads to decrease the overall losses as well as the electromagnetic interference (EMI) comparing to three phase two level inverters [58].

There are three basic topologies of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) inverters [18, 59]. These topologies are used to generate voltage levels which require a high number of active power semiconductor devices, clamping diodes, flying capacitors, and other components. Furthermore, each of those topologies has specific disadvantages. The disadvantage of the CHB is that each H-bridge module needs an isolated source [60]. The NPC cannot maintain voltage balance in the dc-link capacitors for some operating conditions [61, 62]. On the other hand, FC requires excessive number of capacitors when the number of levels increase [63]. Moreover, NPC and FC are not modular which is not preferred for some high power industrial applications.

There are efforts to combine the advantages of the aforementioned topologies such as an eighteen level inverter topology proposed in [64]. The main disadvantage of this topology is that asymmetrical sources are required. Another solution is presented in [65] which utilizes low switching frequency. Although this topology overcomes some previous problems, it generates significant low order current harmonics as well as it does not manipulate the magnitude of the output voltage properly. The topology which is presented in [66] reduced the number of switches and DC sources, but it needs different values of DC sources, different blocking voltage, high stress

current for each switch. One solution has been introduced in [67] which combines the advantages of FC and CHB and use only one isolated dc source. However, to maintain the asymmetrical capacitors' voltage, a very complicated feedback controls have been used.

Several control techniques have been analyzed for the injected current control to the grid such as linear PID controller [68], hysteresis controller [69], and sliding mode control [70]. These controllers, except the hysteresis controller, depend on modulating signals. There are several modulation methods which are used for multilevel topologies which are classified according to switching frequency as shown in Figure 9. The methods which are used for high switching frequency are sinusoidal PWM and space vector modulation (SVM). These methods are used to reduce the harmonics in the output current [54] but unfortunately the switching losses is increased. Moreover, the methods that work with low switching frequency overcome the switching losses but the harmonics are increased [71, 72].



**Figure 9: Classification of multilevel modulation methods**

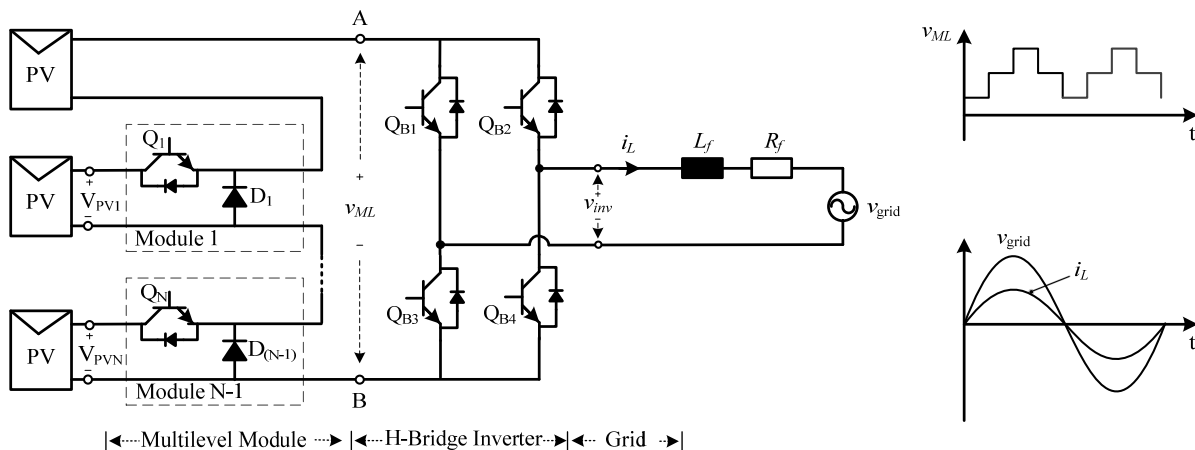
Currently, one of the most important type of closed loop control is model predictive control (MPC) which can be used for current control of the power converters. MPC has several advantages; like fast dynamic response, flexible to include additional system constraints in the controller without adding any additional loop, and can easily include nonlinearities system [71, 73, 74]. MPC considers a model of the system in order to predict the future behavior of the system over a horizon in time. To apply appropriate switching state, a selection criterion must be defined. This criterion consists of a cost function that will be evaluated for the predicted values of the variables to be controlled. Prediction of the future value of these variables is calculated for each possible switching state and then the state that minimizes the cost function is selected. By using MPC, low and high switching frequency, which is demonstrated in Figure 9, can be used for the multilevel inverter which was proposed in [75-77].

This chapter presents an application of MPC for single phase symmetrical multilevel inverter which is suitable for grid connected or standalone application. The overall system consists of multilevel model and single phase H-Bridge inverter to provide a multilevel output voltage to the load [78]. MPC offers high performance injected grid current and reduces the THD. To clarify the advantages of the MPC for the new topology, simulation results for 7-level symmetrical grid connected topology are presented. In addition, implementation results using dSPACE 1103 are provided in this chapter.

## **2.2. The Modified Multilevel Inverter Topology**

This section explains the configuration of the modified multilevel inverter. Figure 10 shows the schematic diagram of the modified inverter, which can be used as symmetrical or asymmetrical multilevel inverter. The inverter consists of two parts, the first one is the multilevel module and the second one is the H-bridge inverter. The multilevel module is comprised of a number of sub-

modules connected in series and every module has a DC source (photovoltaic, fuel cell, or isolated DC source). All of these modules are connected in series with one DC source (upper DC source in Figure 10). Each module is considered as a buck converter in which one diode and one power switch are used to convert the DC voltage to multilevel voltage. The H-bridge module is connected to the sub-modules and inverts the DC multilevel voltage to AC multilevel voltage at main frequency as well as generates the zero state. Different levels of the output voltage can be generated according to the number of DC sources and the switches. In order to increase the number of output voltage levels, it is possible to increase the number of modules that are connected in series. Thus, this work presents a modification for the Multilevel DC Link Inverter (MLDCLI) topology [79] where the bypass switch in each module is replaced with a diode ( $D_1, \dots, D_N$ ). In addition, the upper module is removed completely and only the source is connected directly to the following module. Thus, this modification reduces the number of power switches in the multilevel topology. Since less switches as well as less gate drives are needed in this modified topology which simplifies the control and improves the reliability.



**Figure 10: Symmetrical or asymmetrical single phase multilevel inverter**

For symmetrical modified multilevel inverter, the maximum number of levels  $N_{Levels,max}$  and the maximum output voltage  $v_{inv,max}$  which can be produced, are calculated as following:

$$N_{Levels,max} = 2N + 1 \quad (1)$$

$$v_{inv,max} = N * V_{dc} \quad (2)$$

where  $N$  is the number of sources and  $V_{dc}$  is the DC source in each module. However, for asymmetrical multilevel inverter, the relation between the DC sources (excluding the first source, which it is always  $V_{dc}$ ) can be founded as:

$$V_{dci} = 2^{(i-2)} V_{dc}, \text{ where } i = 2, \dots, N \quad (3)$$

where the maximum number of levels  $N_{Levels,max}$  and the maximum output voltage  $v_{inv,max}$  can be calculated as following:

$$N_{Levels,max} = 2^N + 1 \quad (4)$$

$$v_{inv,max} = 2^{(N-1)} * V_{dc} \quad (5)$$

**Table 1: Switching state of the seven level multilevel output voltage**

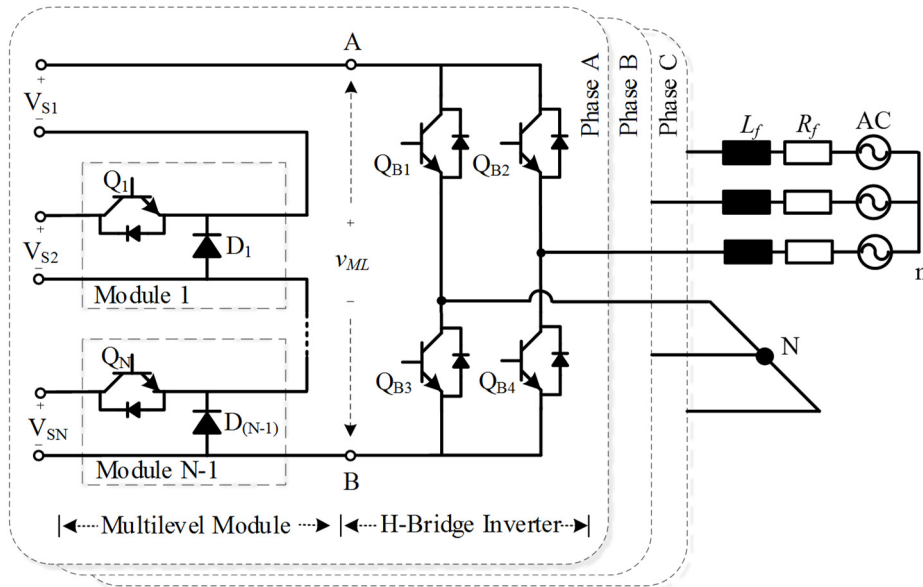
$v_{out}$	$v_{ML}$	Multilevel Module				H-bridge Inverter			
		Q <sub>1</sub>	Q <sub>2</sub>	D <sub>1</sub>	D <sub>2</sub>	Q <sub>B1</sub>	Q <sub>B2</sub>	Q <sub>B3</sub>	Q <sub>B4</sub>
+3V <sub>dc</sub>	+3V <sub>dc</sub>	1	1	0	0	0	1	1	0
+2V <sub>dc</sub>	+2V <sub>dc</sub>	1	0	0	1	0	1	1	0
+V <sub>dc</sub>	+V <sub>dc</sub>	0	0	1	1	0	1	1	0
0	0	0	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	1	1
-V <sub>dc</sub>	+V <sub>dc</sub>	0	0	1	1	0	1	1	0
-2V <sub>dc</sub>	+2V <sub>dc</sub>	1	0	0	1	0	1	1	0
-3V <sub>dc</sub>	+3V <sub>dc</sub>	1	1	0	0	0	1	1	0

In addition, the number of switches  $N_{switches}$  that are needed for the symmetrical modified topology can be calculated as following:

$$N_{switches} = \frac{N_{Levels,max} - 1}{2} + 3 \quad (6)$$

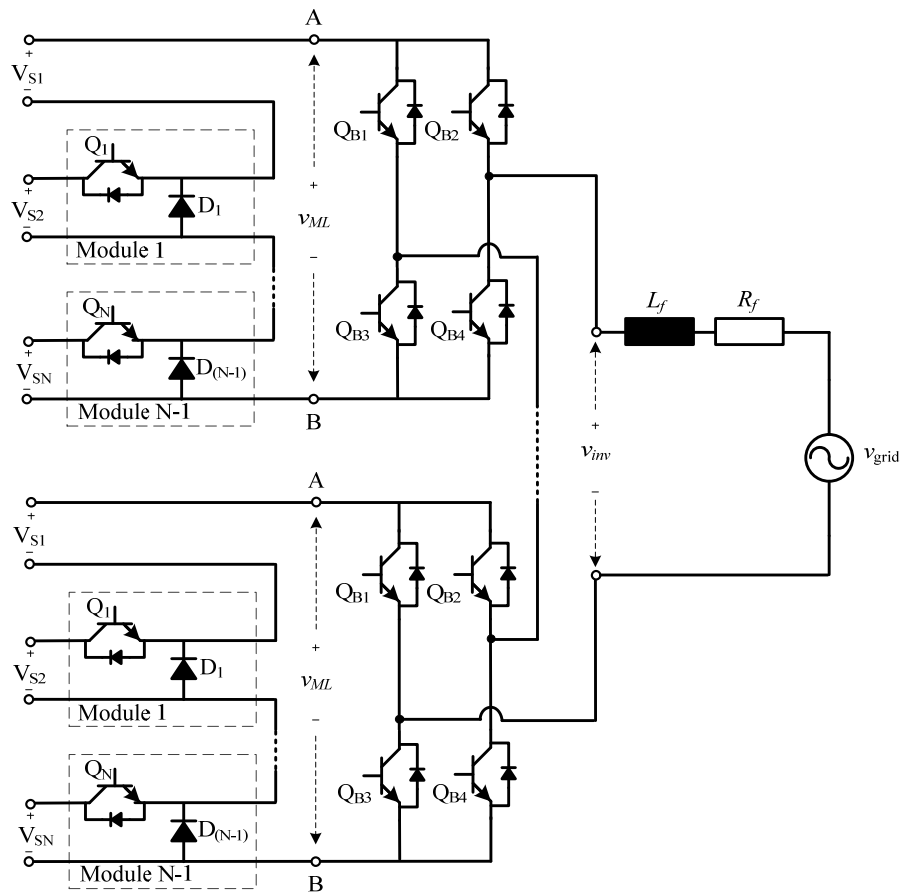
Figure 11 shows the three phase multilevel inverter with N-1 levels and one polarity generation per phase. Figure 12 shows an extension for the single phase modified multilevel inverter in case if the stress voltage on the components on the single module is larger than the maximum voltage of the switches that are available on the market. In Figure 12, x indicates the number of H-bridge per phase. Figure 13 shows the three phase extended multilevel inverter.

The basic operation of the modified multilevel inverter is shown in Figure 14 where three DC sources and two modules are considered. This figure shows the switching configurations for the three positive-voltage states of the 7-level inverter. The DC multilevel module is formed by connecting two modules in series where each module is connected with one DC source. All of these modules are connected in the top terminal with one DC source (upper source). In each module, the switch and the diode operate in a complementary fashion. The module is bypassed



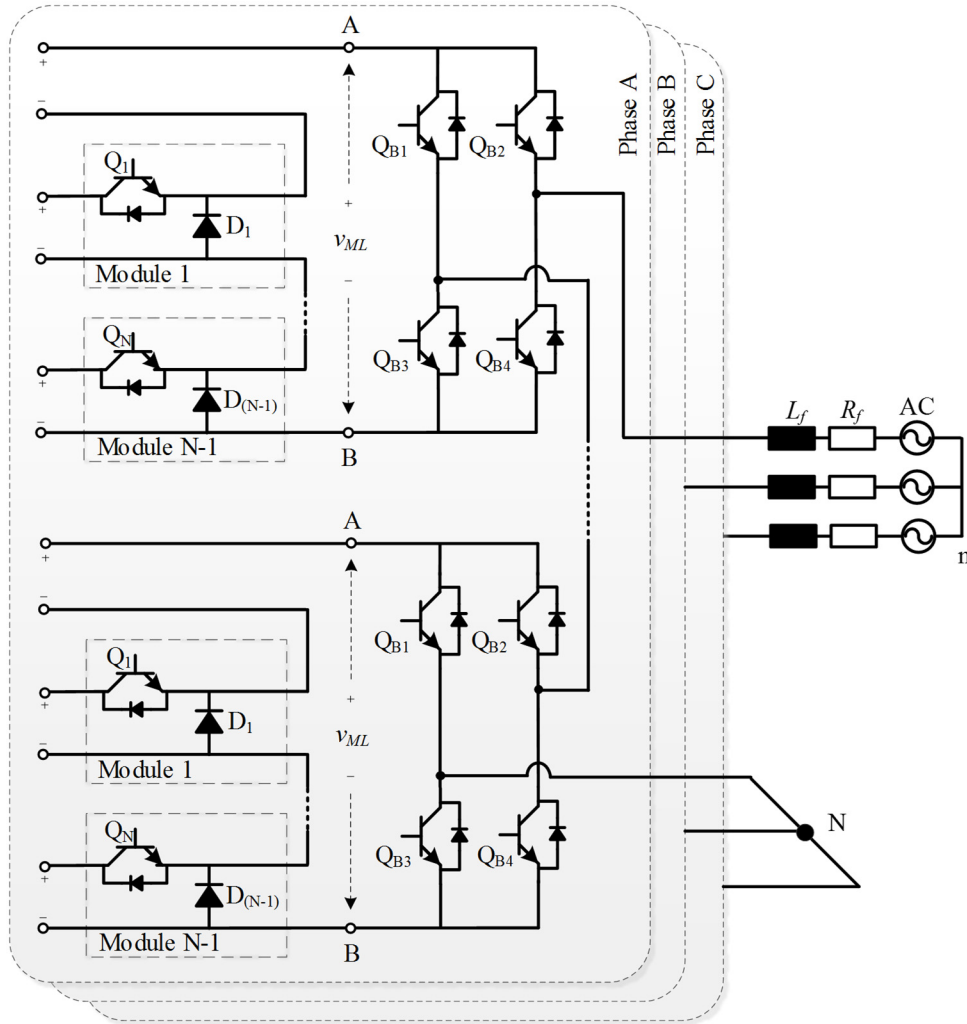
**Figure 11: The proposed three phase multilevel topology with (N-1) level generation and one polarity generation per phase**

when the switch is OFF and the diode is ON. In this work symmetrical system is considered where the three identical DC sources are used so the output voltage is seven level. Table 1 shows the states of the switching for seven level output voltage for the symmetrical multilevel inverter. As shown in Table 1, for zero state, there are two possible switching actions; QB1 and QB2 are turned ON, or QB3 and QB4 are turned ON which create a short circuit on the load side. In addition, for normal operations, there are two possible switching states for H-bridge inverter; positive state where QB1 and QB4 are ON, and negative state where QB2 and QB3 are turned ON, as shown in Table 1. Figure 14(a) shows the multilevel modules where three DC sources are used.



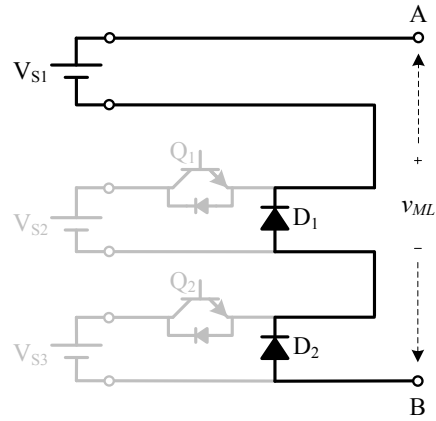
**Figure 12: The proposed single phase multilevel cascaded H-bridge topology with (xN-x) level generation and x polarity generation**



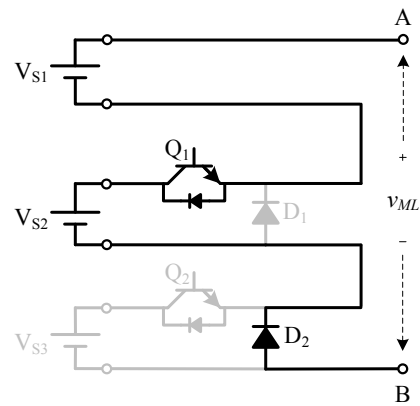


**Figure 13: The proposed three phase multilevel cascaded H-bridge topology with  $(xN-x)$  level generation and  $x$  polarity generation**

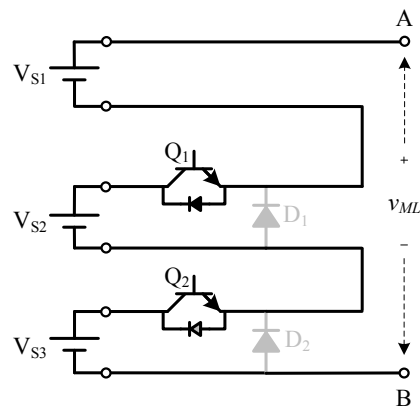
This module can generate three level output voltage in the terminal of the multilevel module. Moreover, Figure 14(b) shows the state of the multilevel module when the output voltage is  $+V_{dc}$ . At this state, only two diodes are ON and each module's switch is turned OFF. Moreover, in Figure 14(c) the output voltage is twice the output voltage from the previous state where  $Q_1$  and  $D_1$  are turned ON. The summation of the previous two states is shown in Figure 14(d) where  $Q_1$  and  $Q_2$  are turned ON.



(a) The multilevel module at  $V_{dc}$



(b) The multilevel module at  $2V_{dc}$



(c) The multilevel module at  $3V_{dc}$

**Figure 14: States of the switches for seven level output voltage**

The power switches used in the multilevel module (Q1 and Q2) are switched at high frequency while the H-bridge switches are operated in a complementary manner except at the zero state. Two switches in H-bridge QB1 and QB4 are kept continuous ON during the positive half cycle of the grid voltage while two switches QB2 and QB3 are kept continuous ON during negative half cycle

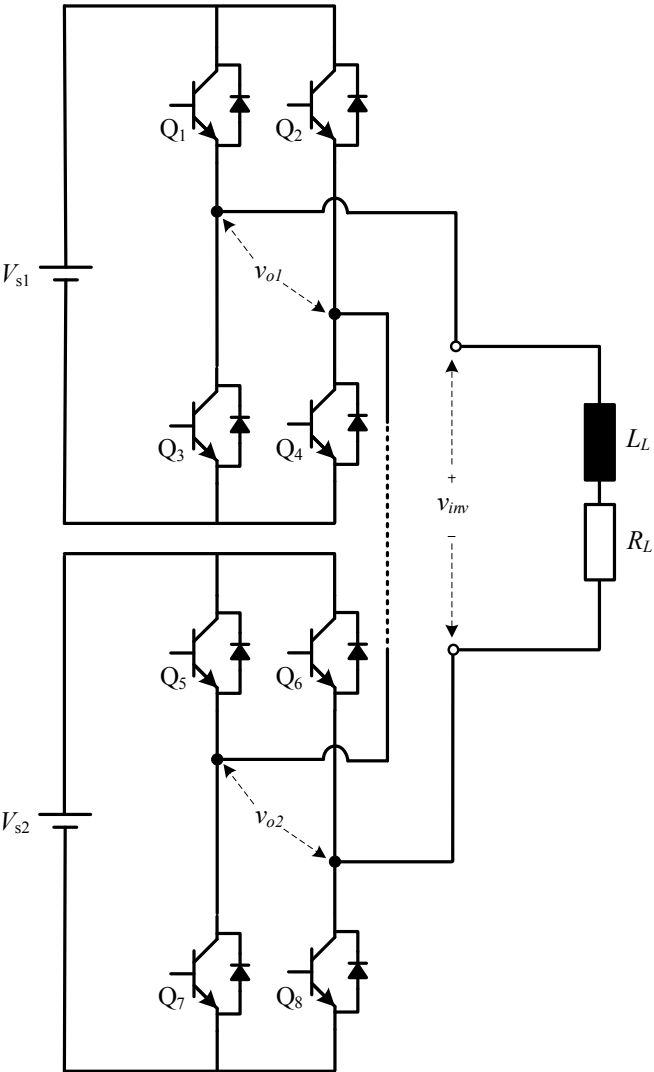
### **2.3. A Comparison between the Proposed Topology and the Conventional Topologies**

These days, there is substantial attention increase in multilevel inverters for different types of high power applications. The most common multilevel inverters are cascade converter as it is shown in Figure 15, neutral-point clamped (NPC) in Figure 16, and flying capacitor inverter in Figure 17. In addition, there are some combinations of the aforementioned topologies such as series combination of a two-level converter with a three-level NPC converter which is called cascaded 3/2 multilevel inverter. Moreover, a series combination of a three level cascaded five level NPC converter which is called cascaded 5/3 multilevel inverter [80]. A topology called reverse voltage (RV) has been proposed in [81, 82] and is shown in Figure 18. Another topologies are presented in Figure 19 and Figure 20; Figure 19 is T-type multilevel inverter [83, 84] and Figure 20 is called multilevel module multilevel inverter (MLM) [85].

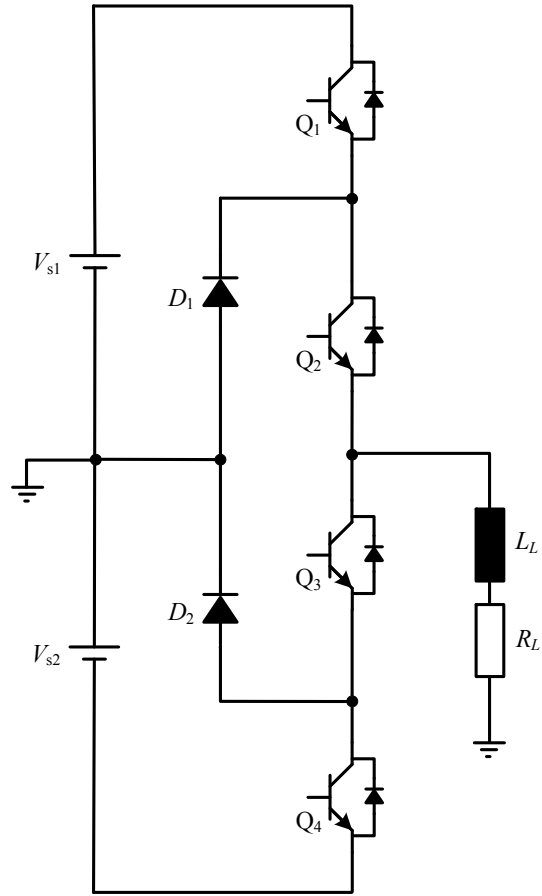
A comparison between the aforementioned topologies regarding to the number of switches has been presented in Table 2. As it is shown in the last row, the modified topology has the lowest number of components after multilevel module multilevel inverter. Unfortunately, multilevel module multilevel inverter has much more stress than the modified topology as it will be demonstrated in the following figures.

Figure 21 and Figure 22 show the comparison between the modified multilevel inverter with the rest of the conventional multilevel inverters for single phase and three phase topologies,

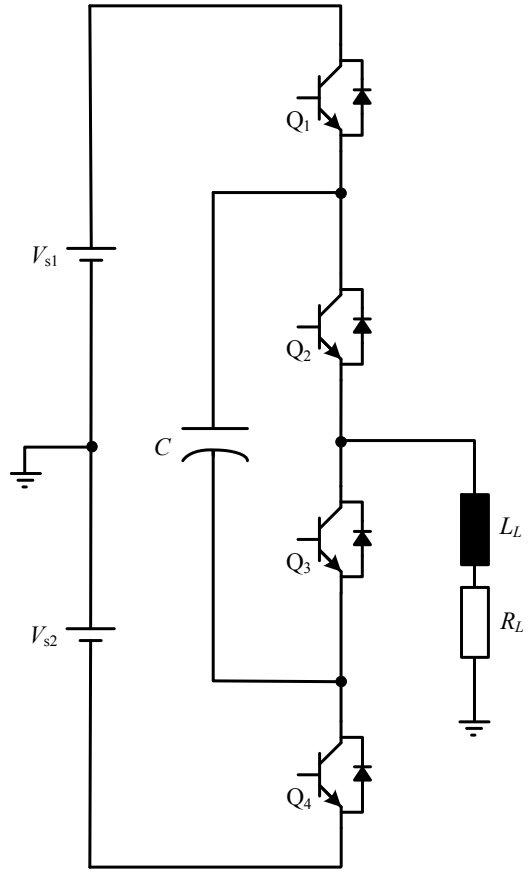
respectively. As it is obvious from this plot, by increasing the number of levels, the modified topology requires less number of switches than other topologies except MLM. Unfortunately, MLM has more stress voltage than the modified multilevel inverter as it is shown in Figure 23.



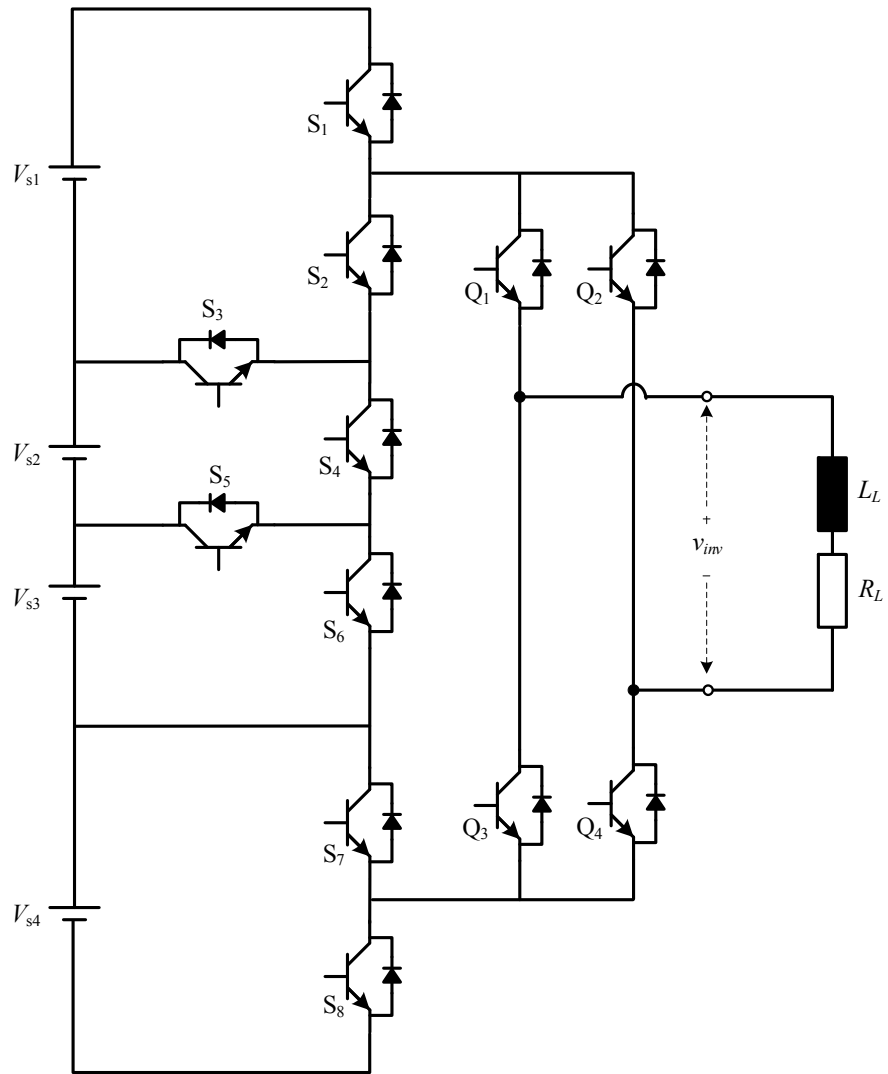
**Figure 15: Cascaded Multilevel inverter**



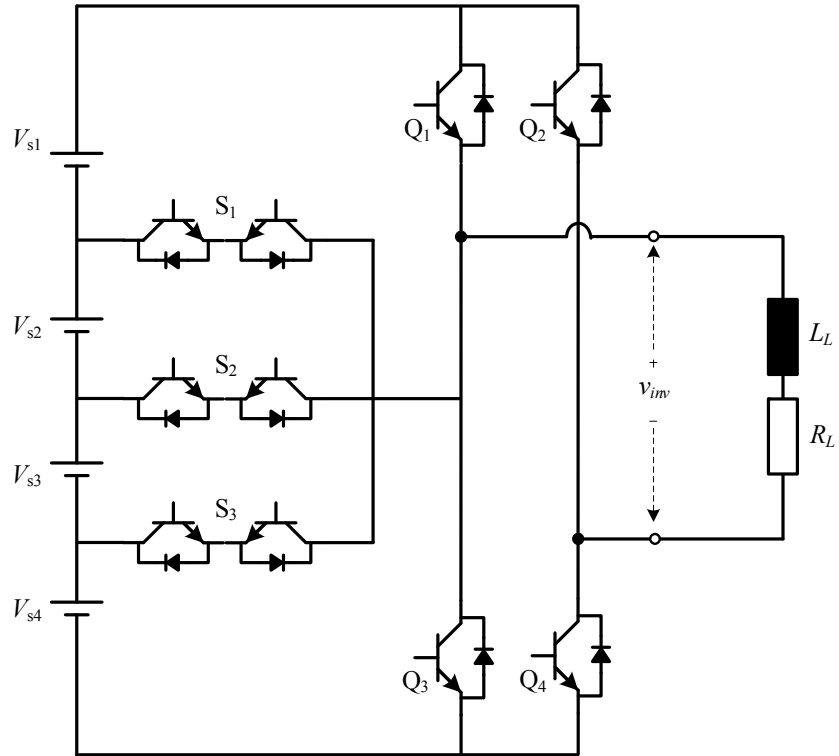
**Figure 16: Neutral-point clamped multilevel inverter**



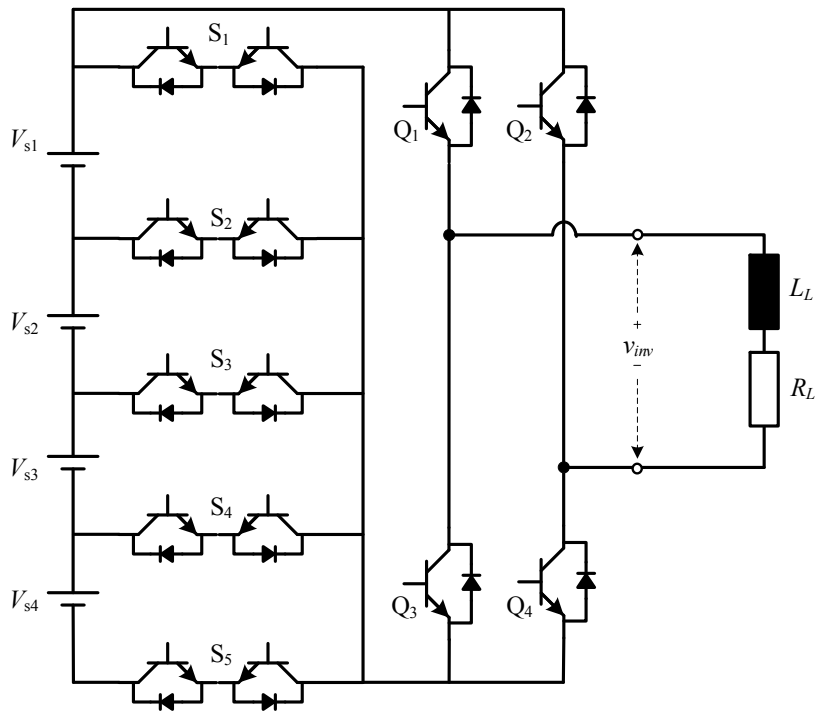
**Figure 17: Three level flying capacitor multilevel inverters**



**Figure 18: Reversing voltage multilevel inverter**



**Figure 19: T-type multilevel inverter**

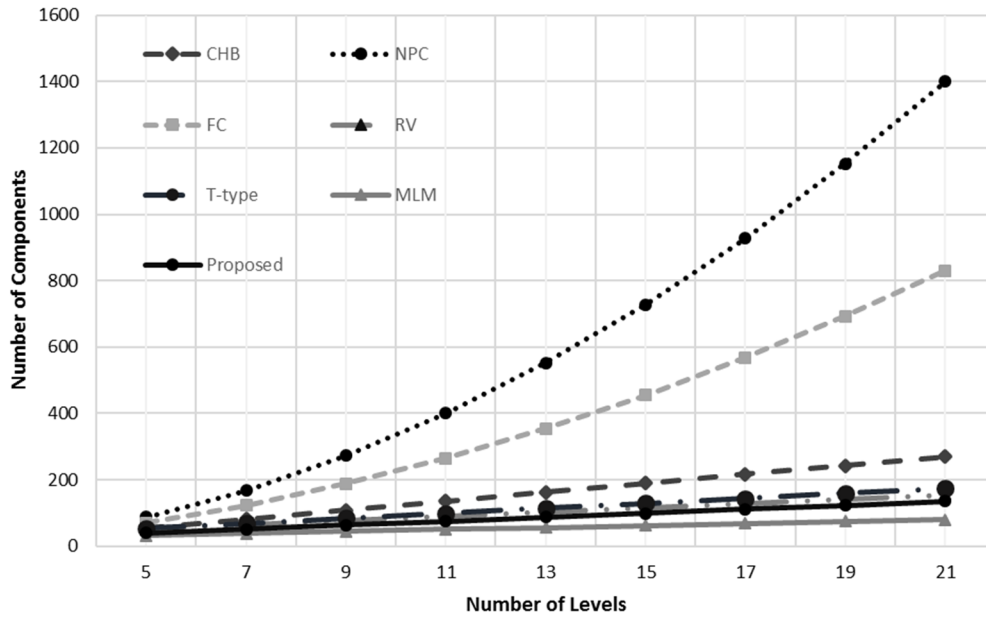


**Figure 20: Multilevel module multilevel inverter**

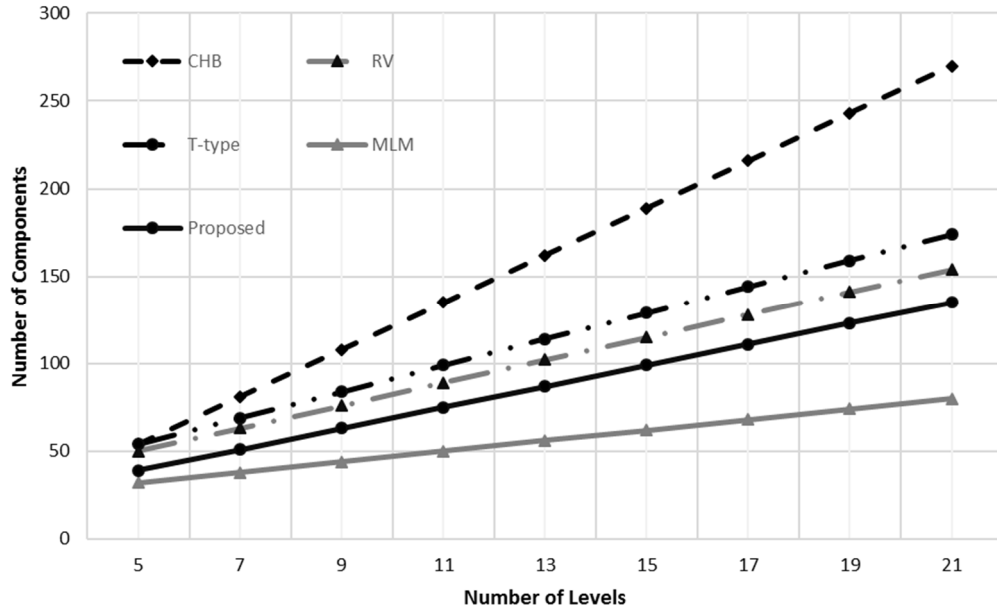


**Table 2: Comparison of three-phase multilevel inverter**

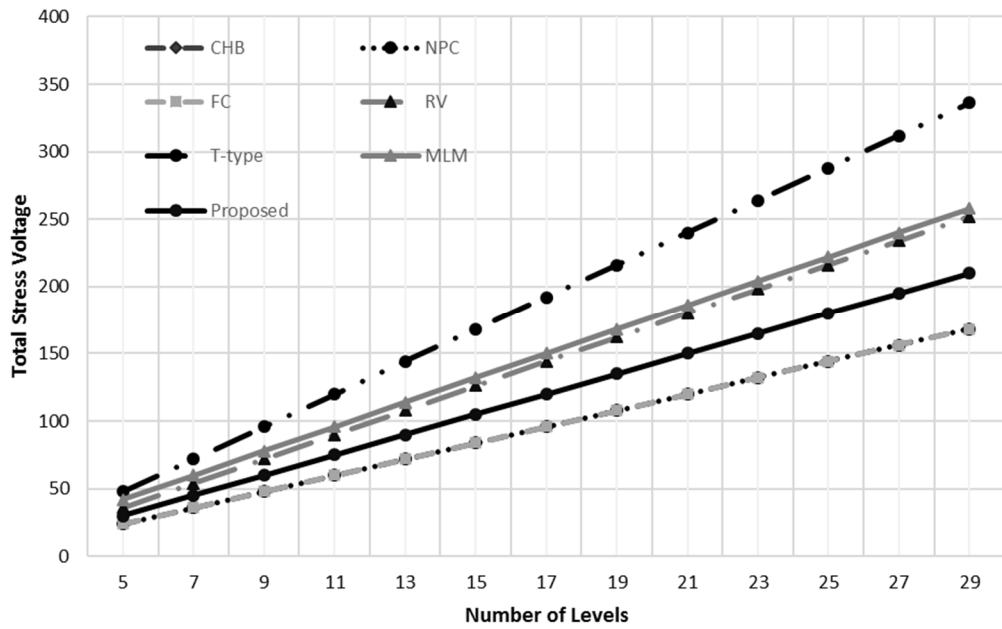
Inverter Type	CHB	NPC	FC	RV	T-Type	MLM	modified topology
Unidirectional switches	$6(n-1)$	$6(n-1)$	$6(n-1)$	$3(n+3)$	12	12	$\frac{3(n+5)}{2}$
Main diodes	$6(n-1)$	$6(n-1)$	$6(n-1)$	$3(n+3)$	$3(n+3)$	$\frac{3(n+9)}{2}$	$3(n+1)$
Bidirectional switches	0	0	0	0	$3(n-1)$	$\frac{3(n+1)}{2}$	0
Clamping diodes	0	$3(n-1)(n-2)$	0	0	0	0	0
Flying capacitors	0	0	$\frac{3(n+1)(n-1)}{2}$	0	0	0	0
DC bus cap/ isolated supplies	$\frac{3(n-1)}{2}$	$n-1$	$n-1$	$\frac{(n-1)}{2}$	$\frac{3(n-1)}{2}$	$\frac{3(n-1)}{2}$	$\frac{3(n-1)}{2}$
Total numbers of devices	$\frac{27(n-1)}{2}$	$(n-1)(3n+7)$	$\frac{(3n+20)(n-1)}{2}$	$\frac{(13n+35)}{2}$	$\frac{(15n+33)}{2}$	$3n+17$	$3(2n+3)$
Total numbers of devices with 5 levels	54	88	70	50	54	32	39



**Figure 21: Variation of the number of components with the number of levels for the single phase MLI**



**Figure 22: Variation of the number of components with the number of levels for three phase MLI**



**Figure 23: Variation of the total stress voltage with the number of levels for the three phase MLI**

## 2.4. Model Predictive Control Principle

The power electronics applications which are controlled by MPC can be found from in 1980s considering high-power systems with low switching frequency [86]. With the development of fast and powerful microprocessors, interest in the application of MPC in power electronics has increased considerably over the last decade [17, 86-88]. Thus, high switching frequency applications with complex calculations can be achieved.

As shown in Figure 24, the main idea of the MPC is predicting a future behavior of the variables (current, voltage,...etc) of the desired system [87]. For the selection of the appropriate switching state to be applied, selection criteria must be defined. The selection criteria is called cost function. The model used for prediction is a discrete-time model of the power converter which can be presented as state space model [89]. The MPC for power electronics converters can be designed using the following steps [87]:

1. Model the power converter which includes all possible switching states and its relation to the input or output voltages or currents.
2. Define a cost function that represents the desired behavior of the system.
3. Obtain discrete-time models that allow one to predict the future behavior of the variables to be controlled.

The discrete time model of the control variables used for prediction can be presented as a state space model as following [89]:

$$x(k + 1) = Ax(k) + Bu(k) \quad (7)$$

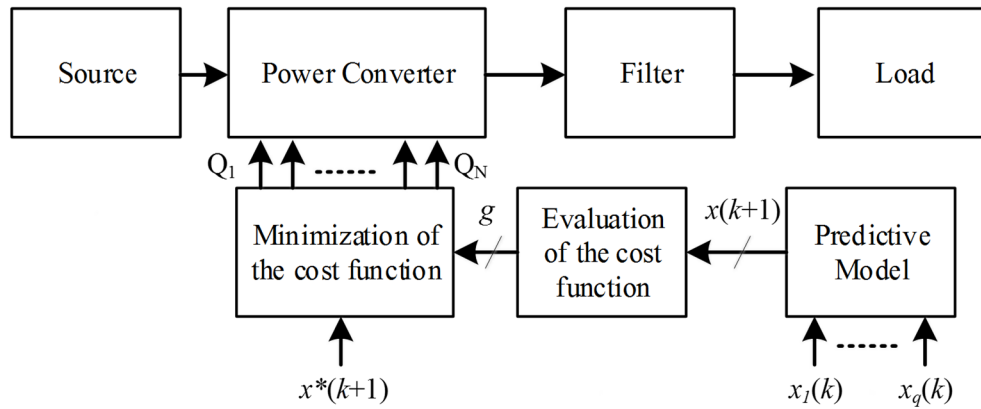
A cost function that takes into consideration the future states, references, and future actuations can

then be defined [89]:

$$g = \lambda_1 |x_1^*(k+1) - x_1(k+1)| + \lambda_2 |x_2^*(k+1) - x_2(k+1)| + \dots + \lambda_n |x_n^*(k+1) - x_n(k+1)| \quad (8)$$

where  $x$  is the controlled variable,  $x^*$  is the controlled reference variable and  $\lambda$  is a weighting factor that allows the level of compromise to be adjusted between reference following and control effort which can be used for multivariable constraints.

The cost function is evaluated in each prediction, then the index value of the voltage vector which minimizes the quality function is stored. At the beginning of the next sampling period, the index value is used to read the table of switching states and generate the corresponding gate signals for the IGBTs.



**Figure 24: Block diagram of the principal MPC**

## 2.5. Discrete Model of the System

As mentioned on the last section, in order to control the overall system by using predictive control, a model of the system should be identified in order to calculate the state variables at the next sample step which is explained in this section. Then after calculating the cost function, the

controller chooses the optimal switching state which minimizes the error between the reference value and the predicted actual value.

Based on the measured value, the load current at  $k+1$  can be predicted according to the following expressions:

$$v_{out} = L \frac{di_L}{dt} + R_f i_L + v_{Grid} \quad (9)$$

$$L \frac{di_L}{dt} = v_{out} - R_f i_L - v_{Grid} \quad (10)$$

A discrete time model of the load current for a sampling time  $T_s$  can be used to predict the next step value of the load current. So by using the forward Euler method, the derivative in (10) can be approximated as

$$\frac{di_L(t)}{dt} \approx \frac{i_L(k+1) - i_L(k)}{T_s} \quad (11)$$

$$i_L(k+1) = \left( 1 - \frac{R_f T_s}{L_f} \right) i_L(k) + \frac{T_s}{L_f} (v(k) - v_{Grid}(k)) \quad (12)$$

where  $i_L$  is the output current,  $i_L(k+1)$  is the predicted value of the output current for the next step,  $T_s$  is the sampling period,  $L_f$  is the inductor value and  $R_f$  is the equivalent series resistance (ESR) for inductor. In addition, the cost function which can force the injected current to follow the reference current can be expressed as follows:

$$g_i = \lambda \left| i_{ref}^*(k+1) - i_L(k+1) \right| \quad (13)$$

where  $i_{ref}^*(k+1)$  is the predicted reference current at this time, which is in phase with the grid voltage and  $\lambda$  is the weighting factor which is equal to one in this case.

Meanwhile, predictive control has the ability to protect the system by define the maximum allowed current which can be injected to the grid by adding one more term in the cost function ( $g_{protection}$ ). This term will be active only when the value of the current exceeds a certain value. In that case, the cost function in all predictive states will be very large. This leads to stop any signals to be applied to multilevel inverters switches.

$$g_{protection} = f(i_{L,max}) \quad (14)$$

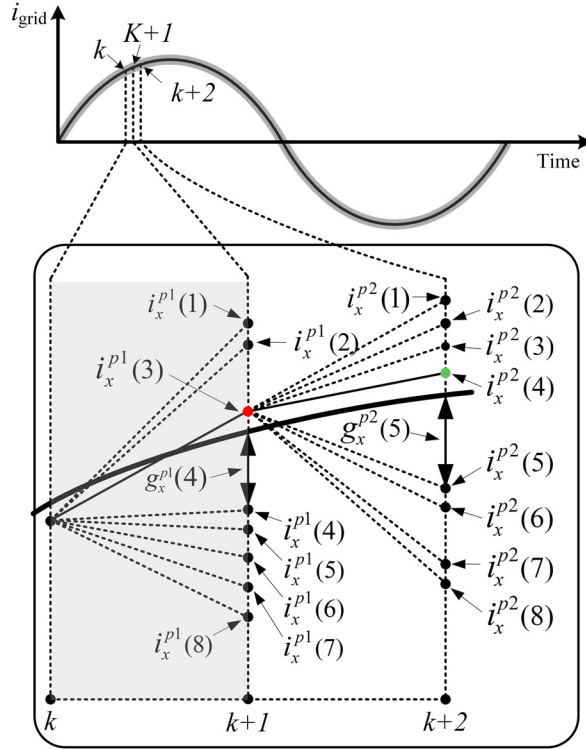
where  $f(i_{L,max})$  is the nonlinear function which depends on the maximum injected current to the grid:

$$f(i_{L,max}) = \begin{cases} \infty & i_L > i_{L,max} \\ 0 & i_L < i_{L,max} \end{cases} \quad (15)$$

Finally, the main cost function consists of two terms; one term for the grid injected current and the second for the protection as follows:

$$g = \lambda \left| i_{ref}^*(k+1) - i_L(k+1) \right| + f(i_{L,max}) \quad (16)$$

The implementation of the control algorithm starts from sensing the variables which in this case is the injected grid current and the grid voltage at a given sample time “ $k$ ” as shown in Figure 24 (considering the load block is a grid). The control calculates the predicted value at next sampling time “ $k+1$ ” for each possible input according to (12). The controller can optimize a defined cost function “ $g$ ” by using the predicted variables and the predicted references with the help of (16). The input which minimizes the cost function is applied in the next sampling time “ $k+1$ ”.



**Figure 25: Schematic illustrating prediction observation for the injected output current**

The strategy of the predictive control is illustrated in Figure 25 for the injected current to the grid assuming that point “ $k$ ” is the current time when the control starts its observation. The controller calculates the next step predictive value for the output current where the sample time “ $k+1$ ”. Then, the optimizer chooses the closest state to the future reference.

## 2.6. Simulation and Experimental Results

In this section, simulation and experimental results are presented to prove the concept. First, simulation results using Matlab/Simulink for the modified topology with FCS-MPC are provided to show the control effectiveness and performance. The experimental results by using ControlDesk with dSPACE 1007 are provided to verify the system performs well. Table 3 shows the parameters values. As the FCS-MPC does not have any modulator, the switching frequency is variable. The average switching frequency of the modified multilevel inverter is calculated by (17)

which in this chapter is 5 kHz. It is worth to mention that the average switching frequency depends on the sampling time. If the sampling time increases, the switching frequency decreases, however if the sampling time decreases, the switching frequency increases.

$$f_{av} = \frac{\sum_0^x f_1 + f_2 + f_3 + f_4 + f_5 + f_6}{6x} \quad (17)$$

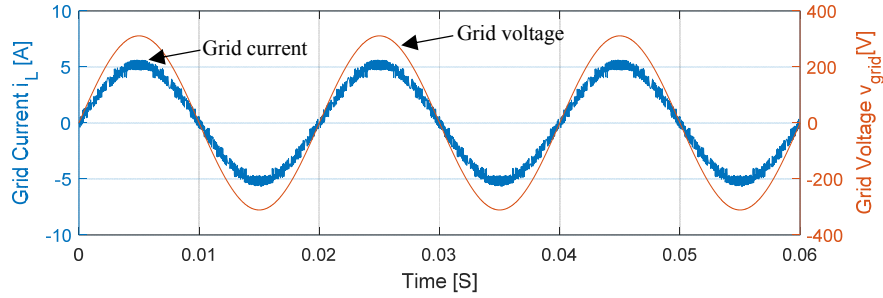
where  $x$  is the number of cycles, which in this work four fundamental cycles are considered. Figure 26 (a) demonstrates the synchronization of the steady state injected grid current and the grid voltage at 0.8 kW. As it is shown, the grid current is in phase with the grid voltage with unity power factor. In addition, Figure 26 (b) shows the high quality seven level output voltage. Besides that, Figure 26 (c) shows the multilevel voltage of the multilevel modules.

The voltage has three levels where the first level is at around 110V, the second level is at 220V, and the third level is at 330V. As it is shown, the frequency of the output voltage modules is 100Hz which is twice the output frequency. It is worth to mention that these modules do not create the zero state, so the controller for the H-bridge has to generate the zero state by its own.

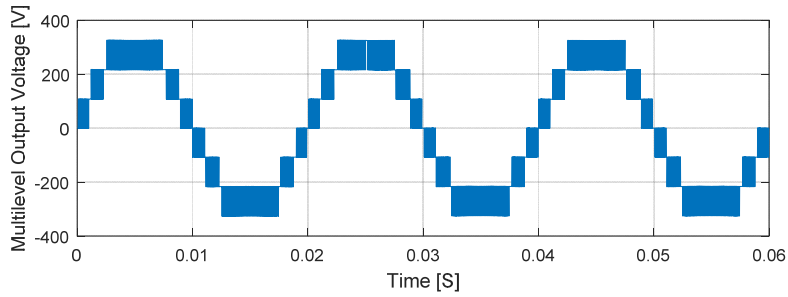
**Table 3. The system parameters**

Parameter	Value
DC Input voltage $V_{pv}$	110V
RMS grid voltage $v_{grid}$	220V
The filter $L_f$	0.5mH
The filter ESR $R_f$	0.5ohm
Sampling time $T_s$	20 $\mu$ S

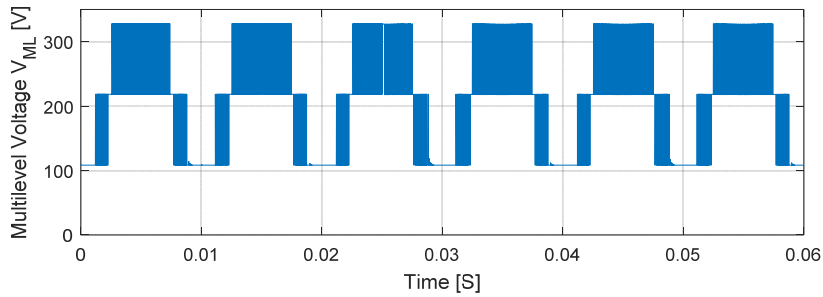




(a) Injected current and grid voltage



(b) Multilevel inverter output voltage

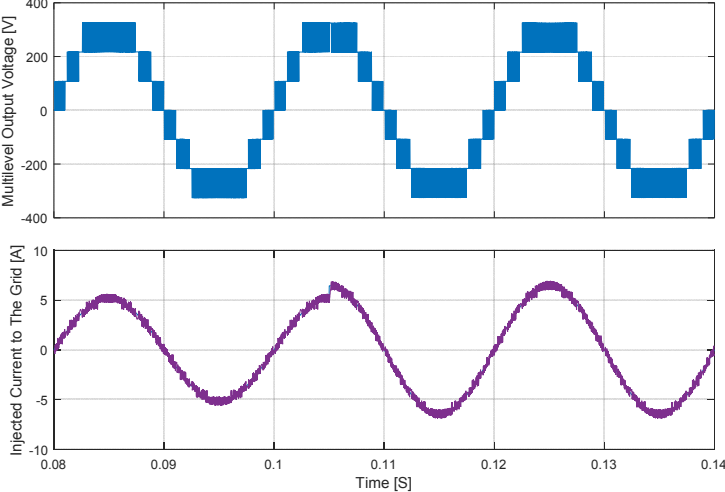


(c) DC-link voltage

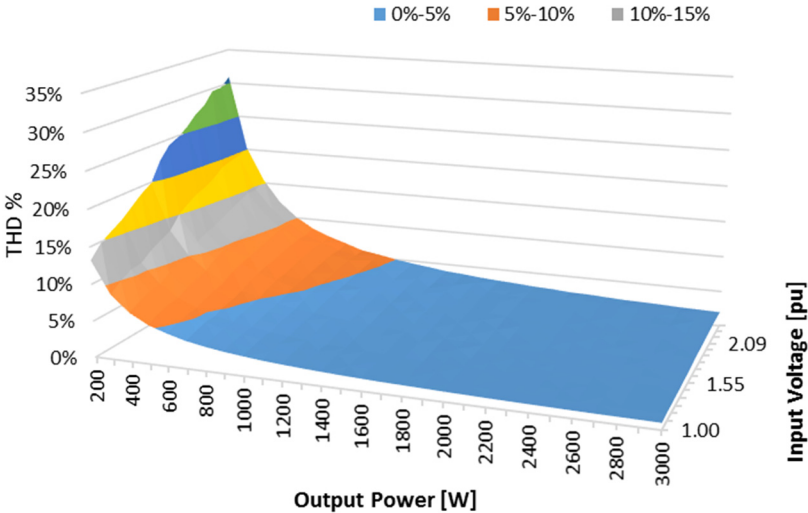
**Figure 26: The simulation results for the injected grid current and the grid voltage with 0.8KW reference power**

A step change in the reference output power is applied on the system from 0.8 kW to 1 kW; Figure 27 shows the multilevel output voltage (the top) and output current (the middle). As shown, the output voltage has seven accurate levels and the quality is still not affected while the output current has near sinusoidal waveform with fast response, which proves the correctness of the modified circuit even at low inductive load. Figure 29 shows the THD for the injected current

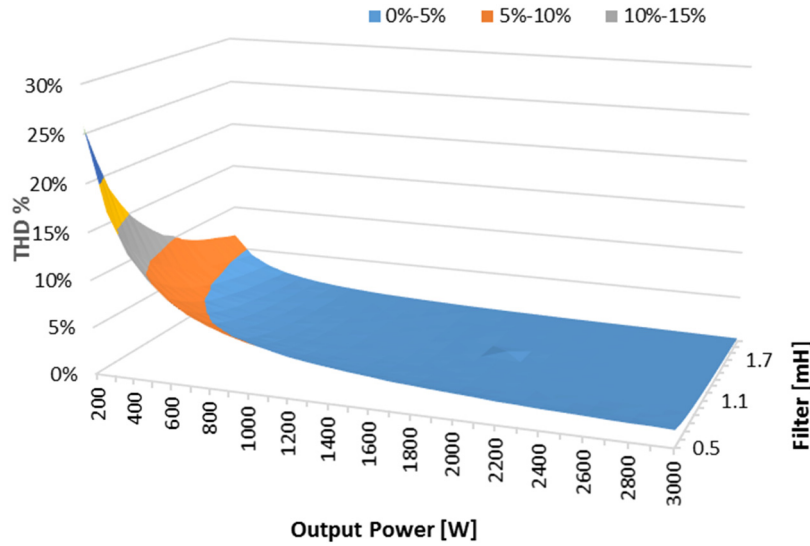
to the grid with various input voltages (pu) and reference output powers. In addition, Figure 29 shows the THD as a function of output power and inductive filter. It is evident that this system with the FCS-MPC has a very low harmonic and complies with the IEEE recommended practice for utility interface of photovoltaic (PV) systems [90] even with low inductor value.



**Figure 27: The simulation results with a step change in the reference output power from 0.8KW to 1KW**



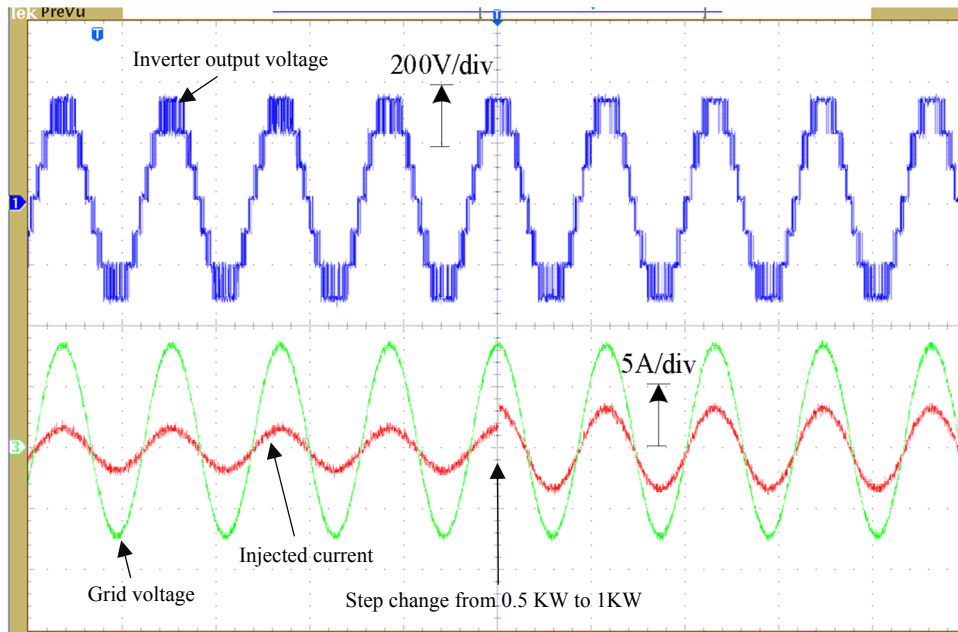
**Figure 28: THD as a function of output power and input voltages with 0.5mH inductor**



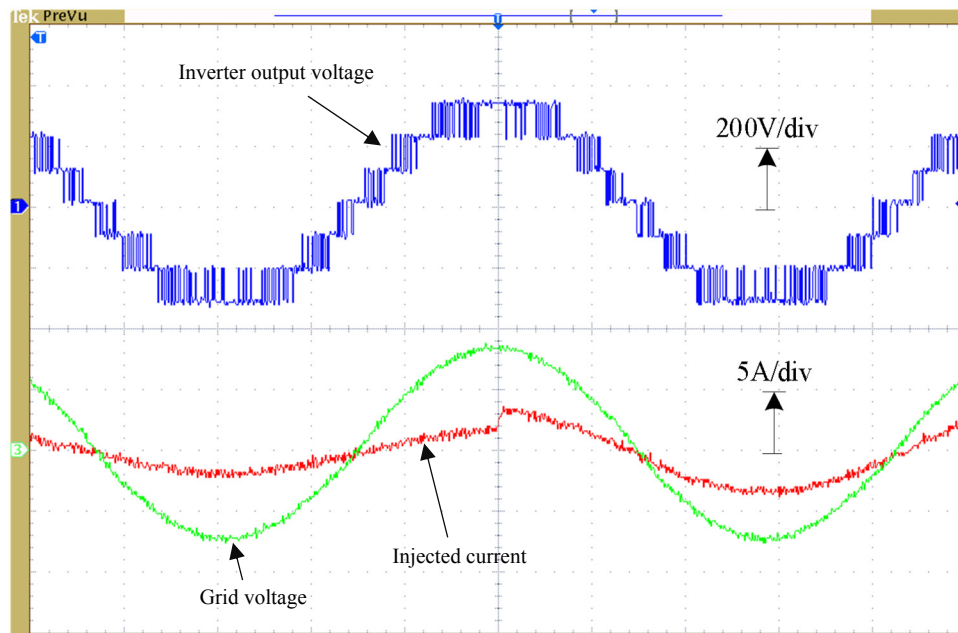
**Figure 29: THD as a function of output power and inductive filters ( $L_f$ ) with base input voltage**

The validity and feasibility of the modified multilevel inverter is confirmed using a test bench implementation with dSPACE 1007. To test the dynamic performance of the grid connected improved MLDCLI with the designed controller, a step change in the reference output power is applied. Thus, the amplitude of the injected current to the grid has been changed from 3.5A to 7A as shown in Figure 30. This figure shows also that the injected current is in phase with the grid voltage (unity power factor).

Moreover, seven levels output voltage has been achieved. Figure 31 shows a zoom on Figure 30, which demonstrates that the performance is fast with high quality output that is achieved by using MPC at the instance of the step change.



**Figure 30: Real-time results for multilevel output voltage, output current and grid voltage with a step change in the reference output power from 0.5KW to 1KW**



**Figure 31: Zoom of the multilevel output voltage, output current and grid voltage with a step change in the reference output power from 0.5KW to 1KW**

## **2.7. Conclusion**

This chapter presented a modified DC link multilevel inverter in which the total number of power switches is reduced comparing with the conventional multilevel inverters. A comparison with other topologies has been presented to confirm that the modified topology can significantly reduce the number of power switches as well as the number of gate drivers with increasing the voltage levels. Moreover, MPC has been designed and implemented for the grid connected modified MLDCLI. Simulation studies with Matlab/Simulink were performed for symmetric seven level inverter based on the modified topology. Experimental verification has been performed using ControlDesk with dSPACE 1007 and has proved the high performance of the modified topology. The presented results showed that the modified multilevel inverter with MPC gives very good performance tracking with fast dynamic response.

### 3. EFFICIENT MAXIMUM POWER POINT TRACKING USING MODEL PREDICTIVE CONTROL FOR MULTILEVEL DC-DC CONVERTER\*

This chapter presents a high efficient Maximum Power Point Tracking (MPPT) of Photovoltaic (PV) system by means of Model Predictive Control (MPC) technique applied to a high-gain DC-DC converter. The high variability and stochastic nature of solar energy requires that the MPPT control continuously adjusts the power converter operating point in order to track the changing maximum power point; a concept well known in the literature. The main contribution of this chapter is introducing a model-predictive based controller with fixed-step that is combined with the traditional Incremental Conductance (INC) method. This technique improves the speed at which the controller can track rapid changes in solar insolation and results in an increase in the overall efficiency of the PV system. The controller speeds up convergence since MPC predicts the error between the commanded and actual converter operation before a switching signal is applied to the high gain multilevel DC-DC converter and thus is able to choose the next switch event to minimize this error. Comparing the proposed technique with the conventional INC method shows substantial improvement in MPPT effectiveness and PV system performance. The performance of the proposed MPC-MPPT is analysed and validated experimentally.

#### **3.1. Modified Maximum Power Point Tracking by Model Predictive Control**

Many MPPT techniques for PV energy harvesting system have been introduced over the past few decades [91-96]; several well-known techniques are discussed in [97]. A critical operating

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\* Portions of this chapter have been previously published in M. Mosa, M. B. Shadmand, R. S. Balog, and H. Abu-Rub "Efficient maximum power point tracking using model predictive control for photovoltaic systems under dynamic weather condition," in IET Renewable Power Generation, 2017, © 2017 IET and M. B. Shadmand, M. Mosa, R. S. Balog, and H. Abu Rub, "An improved MPPT Technique of High Gain DC-DC Converter by Model Predictive Control for Photovoltaic Applications," Applied Power Electronics Conference & Exposition (APEC), March, 2014, © 2014 IEEE.

regime occurs at low solar irradiance; harnessing all of the available solar energy during low solar irradiance periods can significantly improve system operation performance. An MPPT controller and power converter that can effectively track and convert the maximum available solar energy increases the overall conversion efficiency of the PV, without relying on an improvement in the solar cell itself. The MPPT techniques in [97] can be classified into categories that include: Perturb-and-Observe (P&O) [98], Incremental Conductance (INC) [96], Fuzzy Logic Control [99], fractional Open-Circuit Voltage (Voc) [100], Neural Network [92], and Best Fixed Voltage (BFV) [101] where each approach having both advantages and disadvantages.

Recently, efforts have also been made in using model predictive control (MPC) for MPPT of PV systems to improve tracking accuracy and reduce conversion settling time. This is possible thanks to the predictive nature of MPC. Abushaiba et al. proposed a model predictive based MPPT for PV applications [102]. The method proposed in [102] calculates the maximum operating point by considering two possible predicted (future) voltage at sampling time ( $k+1$ ). Then the predicted PV power is calculated by using an observer model based on the equivalent impedance of PV; finally, a modulator is used to generate the switching signals. The MPPT method by MPC in [103] uses three sensors for voltage and current measurements while the performance is verified by simulation only.

The INC technique is well-known with relatively good energy harvesting performance; though the control converges to a limit-cycle around the maximum power point rather than a singular operating point. In addition, INC-MPPT is relatively slow, which limits its capability to track transient solar irradiance [102]. The main contribution of this chapter is to enhance the energy harvesting performance of the well-known INC-MPPT technique by predicting the error one step in the time horizon using MPC framework. The number of the input in the proposed controller is

minimized in comparison to previously proposed MPC based MPPT methods. In the proposed method only two sensors are required to predict the MPP voltage and current. Furthermore, the proposed method doesn't require modulator block and directly manipulates the switching signals by minimizing the developed cost function. The proposed method is shown to have faster dynamic response than conventional INC method by using fixed step size variation of a DC-DC converter duty cycle and it overcomes much of the limitations of the conventional INC approach under rapidly changing atmospheric conditions.

Generally, the overall efficiency of PV systems depends on three main factors: the conversion efficiency of the PV module, the efficiency of the DC-DC conversion stage, and the control effectiveness of the MPPT technique. In this chapter both the control effectiveness and the efficiency of the DC-DC conversion stage of the proposed system are evaluated. The control effectiveness analysis of the proposed predictive control based MPPT shows that it has both fast dynamic response and high tracking efficiency at steady state – properties that should be traded-off in the traditional INC method.

Certainly any algorithm that knows the right answer *a priori* will excel over other algorithms that need to search for the right answer. It is difficult, and expensive (in all senses of the word) to completely characterize the performance of the converter and source for all possible operating points. Instead, the proposed MPC-MPPT knows *a priori* only the structure of the model, but still needs to search for the right answer. This is different than a lookup table built on full knowledge of the system, its operation, and its performance. We chose to compare against the INC method because it is popular, at least in the literature, and both methods use a perturb-and-observe approach to finding the MPP operating point. The preliminary analysis and results of the



proposed technique was published in [104-107], in this chapter more research outcomes, efficiency analysis, and experimental verifications are added.

### 3.2. The Principle of Predictive Model-Based Controller

Application of MPC in power electronics dates back to the 1980's for low switching frequency, high power applications [86, 89]. The implementation of such control for operating power electronic converters at high switching frequencies required much faster computational resources that available, hence widespread its adoption was not feasible at that time. In the past decade, improvements in high speed microprocessors spurred renewed interest in the application of MPC for higher switching frequency power converters [17, 91, 108, 109]. The main feature of MPC is predicting the future behavior of the control variables until a specific time in horizon [89]. The predicted control variables is then used to obtain the optimal switching state by minimizing a cost function. The discrete time model of the control variables is used for prediction, their state space model are [89]:

$$x(k+1) = Ax(k) + Bu(k) \quad (1)$$

$$y(k) = Cx(k) + Du(k) \quad (2)$$

Then the cost function can be defined

$$g = f(x(k), u(k), \dots, u(k+N-1)) \quad (3)$$

The defined cost function  $g$  takes into consideration the future states, references, and future actuation. This cost function should be minimized for a specific step on the time horizon  $N$ ; a sequence of  $N$  optimal actuations, as the controller output  $u(k)$ , will be determined where the controller only applies the first element of sequence:

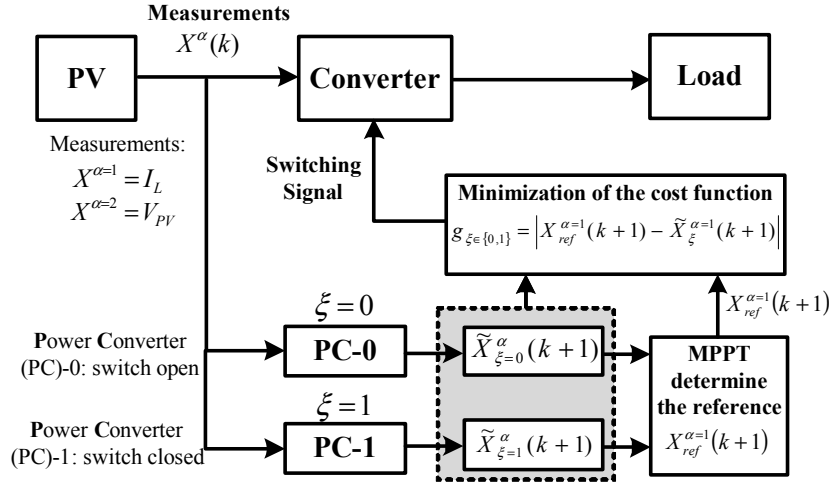
$$u(k) = [1 \quad 0 \quad \dots \quad 0] \arg \min_u g \quad (4)$$

Thus, the control signal  $u(k)$  is sent to the process while the next control signals calculated are rejected. This is due to the fact that the output is already known at the next sampling state [110]. The optimization problem will be solved again at each sampling time by using new set of measured data to obtain a new sequence of optimal actuation. The general form of the cost function,  $g$ , subject to minimization can be formulated as

$$g_\xi = \lambda_1 |X_{ref}^{\alpha=1}(k+1) - \tilde{X}_\xi^{\alpha=1}(k+1)| + \lambda_2 |X_{ref}^{\alpha=2}(k+1) - \tilde{X}_\xi^{\alpha=2}(k+1)| \\ + \dots + \lambda_n |X_{ref}^{\alpha=n}(k+1) - \tilde{X}_\xi^{\alpha=n}(k+1)| \quad (5)$$

where “ $\lambda$ ” is the value or weight factor for each control objective ( $X^\alpha$ ), “ $\alpha$ ” corresponds to the different control variables, and “ $\xi$ ” corresponds to the switching states. In this chapter we use a predictive controller to not just determine switch actuation of the converter, but also to find the maximum power operating point of the PV panel.

The scheme of predictive model-based controller for this application is illustrated in Figure 32. In this block diagram, the measured variables (PV voltage and current in this application),  $X^\alpha(k)$ , are used in the model to estimate predictions,  $X_\xi^\alpha(k+1)$ , of the controlled variables for all of the possible switching state “ $\xi$ ”. Then based on these predictions the reference value of voltage or current to achieve maximum power point operation will be determined. Then the predicted control variable will be evaluated based on the calculated reference control variable in form of a cost function subject to minimization. Finally, the optimal actuation is selected and applied to the converter.



**Figure 32: Predictive model-based controller block diagram for maximum power point tracking.**

The schematic of Figure 32 without loss of generality can be applied to any power converter topology. In this chapter, the multilevel boost converter (MLBC) topology illustrated in Figure 33 has been selected for the proposed MPPT technique, the analysis of this converter topology and its advantages for the application in this chapter are presented in the next section.

### 3.3. Analysis of Multilevel Boost Converter

For residential PV applications, high gain DC-DC converters are typically required to meet the high bus voltage requirements for typical inverters due to low output voltage of the PV modules [111]. However the series connected PV modules is a solution for low output voltage of the PV modules, but this arrangement suffers from the partial shading and mismatch between the series connected modules which significantly decreases the PV array output power [111]. Thus, high gain DC-DC converters for residential PV applications are of high interest. In this chapter a high gain multilevel DC-DC boost converter (MLBC) is used to perform a high efficient PV system [112, 113]. The multilevel boost converter (MLBC) topology for MPPT is illustrated in [114, 115]; the output voltage of the converter is proportional to the number of levels, which can be increased

by adding two additional capacitors and diodes. Since only one switch is used in the selected MLBC topology, the control procedure is simpler than other topologies such as switched capacitor converter with a boost stage [116].

In this chapter MLBC with two levels is used for MPPT. Figure 34 and Figure 35 illustrates the graphical analysis of the converter when the switch is “ON” and “OFF.” As shown in Figure 34 when the switch is turned ON, the inductor conducts and capacitor  $C_1$  keeps charging capacitor  $C_3$  through diode  $D_2$  while voltage of  $C_3$  is smaller than voltage of  $C_1$ . Simultaneously, capacitors  $C_1$  and  $C_2$  supply the load. When the switch is turned OFF, the diode  $D_1$  starts conducting, and the inductor keeps charging capacitor  $C_1$  till its voltage is equal to the summation of the PV module and inductor voltages, Figure 35. Then diode  $D_3$  turns on and the capacitors  $C_1$  and  $C_2$  start charging while the voltage across  $C_1+C_2$  is equal to the summation of PV module, inductor, and capacitor  $C_3$  voltages, Figure 35 [117-120].

The small-ripple approximation, the inductor volt-second balance principle, and capacitor charge balance principle are used to find the steady-state output voltage and inductor current of the MLBC. When the switch is ON in the first subinterval, Figure 34, the inductor’s voltage and capacitor’s current are given by

$$L \frac{di}{dt} = V_{PV} - I_L R_L - R_{on-sw} \left[ I_L + C_3 \frac{dV_{C_3}}{dt} \right] \quad (6)$$

$$C_1 \frac{dV_{C_1}}{dt} = \frac{-V_{C_1} + V_d + V_{C_3}}{R_{C_1}} + C_3 \frac{dV_{C_3}}{dt} + \frac{R_{on-sw}}{R_{C_1}} \left( I_L + C_3 \frac{dV_{C_3}}{dt} \right) \quad (7)$$

$$C_2 \frac{dV_{C_2}}{dt} = \frac{-V_{C_2}}{R_{C_2}} + C_3 \frac{dV_{C_3}}{dt} \quad (8)$$

$$C_3 \frac{dV_{C_3}}{dt} = \frac{V_{C_1} - V_d - V_{C_3} - I_L R_{on-sw} - I_o R_C}{2R_{C_3} + R_{on-sw}} \quad (9)$$

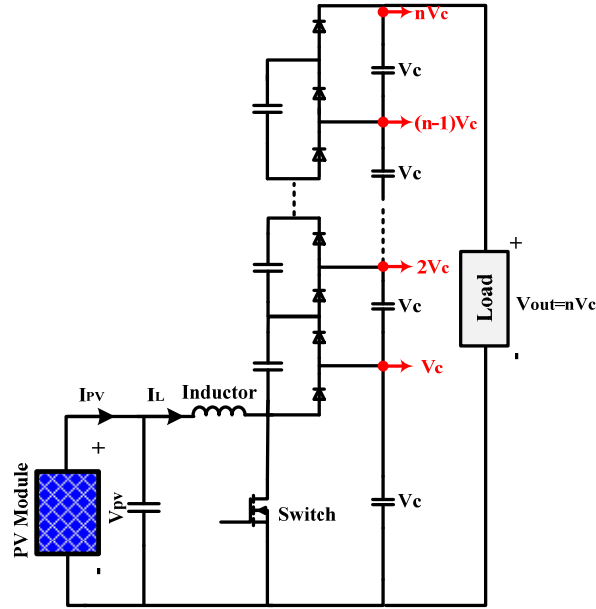


Figure 33: Multilevel boost converter topology

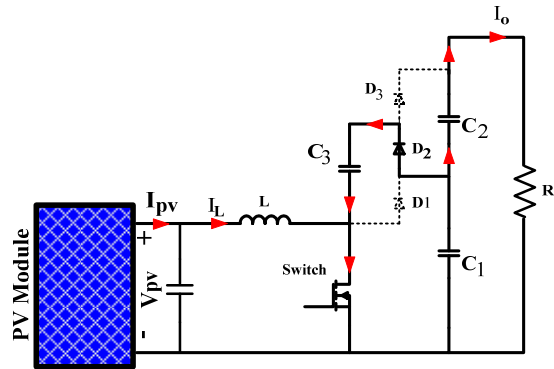


Figure 34: Multilevel DC-DC converter when the switch is ON

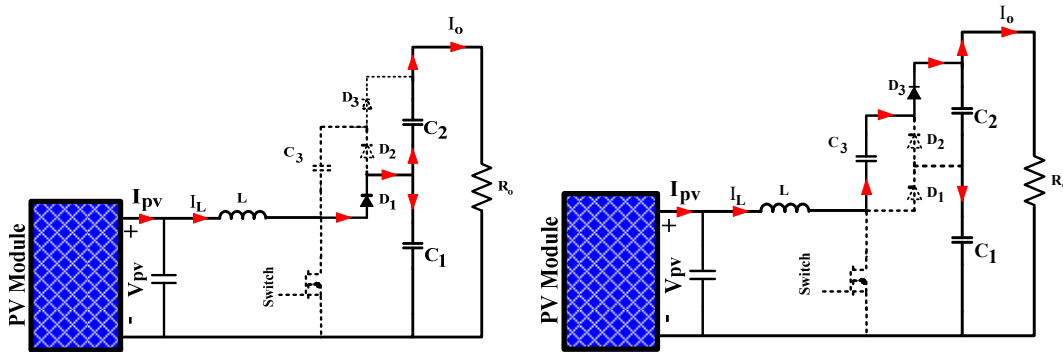


Figure 35: Multilevel DC-DC converter when the switch is OFF

For the next subinterval when switch is OFF, Figure 35, the inductor's voltage and capacitor's current are

$$L \frac{di}{dt} = V_{PV} - I_L R_L - V_d - R_{C_1} C_1 \frac{dV_{C_1}}{dt} \quad (10)$$

$$C_1 \frac{dV_{C_1}}{dt} = I_L - I_o \quad (11)$$

$$C_2 \frac{dV_{C_2}}{dt} = \frac{V_{C_3} - V_{C_1}}{R_{C_2}} + C_3 \frac{dV_{C_3}}{dt} \quad (12)$$

$$C_3 \frac{dV_{C_3}}{dt} = \frac{V_{C_2} - V_{C_3}}{2R_{C_3}} - \frac{I_o}{2} \quad (13)$$

During the first subinterval,  $V_L$  is equal to the dc input voltage. Since, in steady-state, the total volt-seconds applied over one switching period must be zero, negative volt-seconds must be applied during the second subinterval. Therefore, the inductor voltage during the second subinterval must be negative. The volt-seconds and charge balance applied to the inductor and capacitor over one switching period are given by

$$L \frac{di}{dt} = v_{in} - I_l \times A + v_d \left[ \frac{R_{sw}(2D-1) + 2R_c(1-D)}{2R_c + R_{sw}} \right] - R_{sw} D \left[ \frac{v_{c1} - v_{c4} - I_o R_c}{2R_c + R_{sw}} \right] - v_{c1}(1-D) + I_o R_c \quad (14)$$

where A is

$$A = R_l + \frac{2R_c R_{sw}}{2R_c + R_{sw}} + R_c(1-D) \quad (15)$$

$$C_1 \frac{dV_c}{dt} = \frac{V_{pv}}{(1-D)} - I_o \left[ \begin{aligned} & \frac{2R_c}{(1-D)} + \frac{2R_L}{(1-D)^2} + \frac{4R_{sw}R_cD}{(1-D)^2(2R_c + R_{sw})} \\ & + \frac{DR_{sw}}{D(1-D)^2(2R_c + R_{sw})} (R_c(3(1-D)-D)-1 + R_{sw}(1+2D)) \end{aligned} \right] \quad (16)$$

$$C_2 \frac{dV_c}{dt} = \frac{V_{pv}}{(1-D)} - V_d - I_o \left[ \begin{aligned} & \frac{R_c(3+D)}{(1-D)} + \frac{2R_L}{(1-D)^2} + \frac{4R_{sw}R_cD}{(1-D)^2(2R_c + R_{sw})} \\ & + \frac{2R_c(1-D) + R_{sw}}{(2R_c + R_{sw})} \left( \frac{4(1-D)R_c + 2(1+D)R_{sw}}{D(1-D)^2} - \frac{R_{sw} + (2-D)R_c}{D(1-D)} \right) \end{aligned} \right] \quad (17)$$

where  $C$  is the value of the capacitors,  $R_c$  is parasitic dc resistance of the capacitor,  $R_{sw}$  is the ON resistance of the switch,  $V_d$  is the forward voltage of any diodes,  $R_L$  is the dc resistance of the inductor [121, 122].

The DC component of the inductor current is derived by using of the principle of capacitor charge balance. During the first subinterval, the capacitors supply the load current and it is partially discharged. During the second subinterval, the inductor current supplies the load and recharges the capacitors. The output voltage is given by

$$v_o = v_{c1} + v_{c2} = \frac{2V_{pv}}{(1-D)} - V_d - I_o \left[ \begin{aligned} & R_c \left( \frac{5+D}{(1-D)} \right) + \frac{4R_L}{(1-D)} + \frac{8R_{sw}R_cD}{(1-D)^2(2R_c + R_{sw})} \\ & + \frac{DR_{sw}}{D(1-D)^2(2R_c + R_{sw})} (R_c(3(1-D)-1) + R_{sw}(1+2D)) \\ & + \frac{2R_c(1-D) + R_{sw}}{(2R_c + R_{sw})} \left( \frac{4(1-D)R_c + 2(1+D)R_{sw}}{D(1-D)^2} - \frac{R_{sw} + (2-D)R_c}{D(1-D)} \right) \end{aligned} \right] \quad (18)$$

The theoretical analysis in this chapter is based on non-ideal components; therefore it is interesting to see the effect of the Equivalent Series Resistance (ESR) and switch turn on resistance on the efficiency against the output power. As it is illustrated in Figure 36, at high power, efficiency is highly dependent on the capacitor, inductor, and the switch turn on ESRs. As shown, the ESR

of the inductor has the highest effect on the efficiency because the input current is high due to high gain of the converter which is passing through the inductor. This means that the efficiency is more effective by the inductor ESR.

### 3.4. Voltage Oriented Maximum Power Point Tracking by Model Predictive Control

The main characteristic of model predictive control is predicting the future behavior of the desired control variables [87]. The predicted variables are used to obtain the optimal switching state. The proposed MPPT algorithm is illustrated in Figure 37. The inputs to the algorithm are the PV system voltage and inductor current.

The inductor current and PV voltage when the switch is ON ( $\xi = 0$ ) are given by

$$L \frac{dI_L(t)}{dt} = V_{PV}(t) - I_L(t)R_L \quad (19)$$

$$C \frac{dV_{PV}(t)}{dt} = I_{PV}(t) - I_L(t) \quad (20)$$

and when the switch is OFF ( $\xi = 1$ ) are given by

$$L \frac{dI_L(t)}{dt} = V_{PV}(t) - I_L(t)R_L - V_{C1}(t) \quad (21)$$

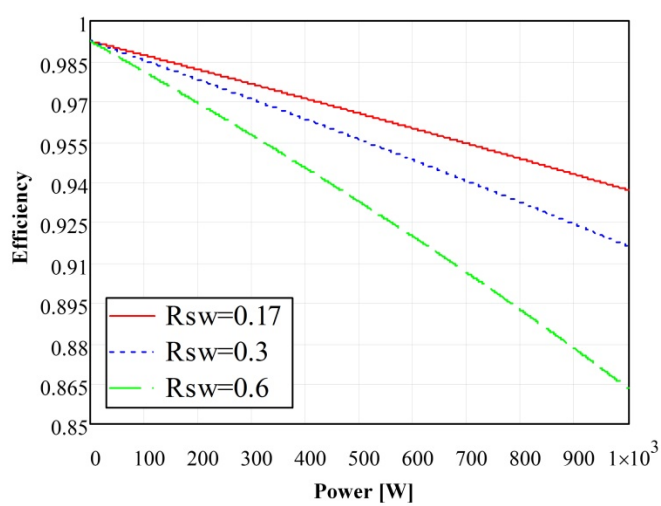
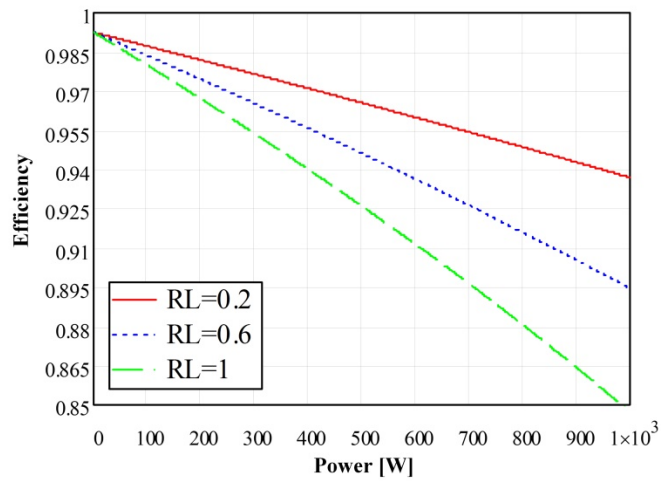
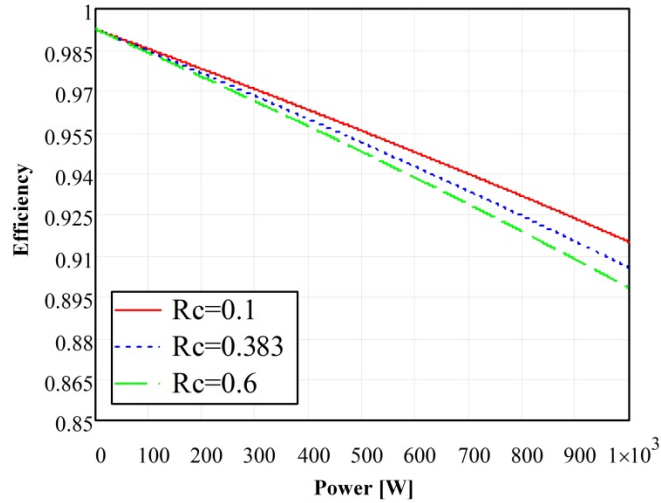
$$C \frac{dV_{PV}(t)}{dt} = I_{PV}(t) - I_L(t) \quad (22)$$

By using the Euler forward method, the derivatives in (19)-(22) can be approximated as

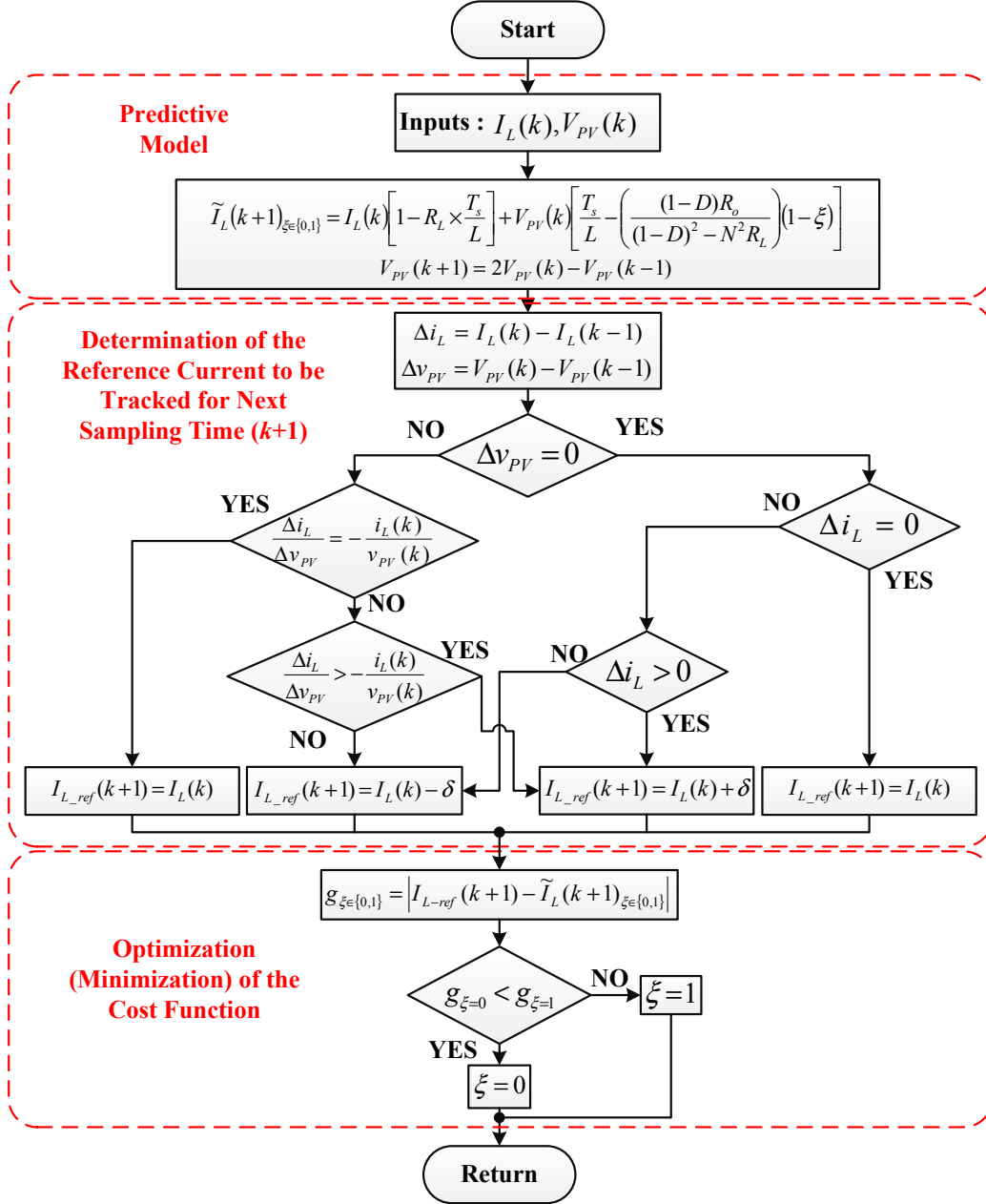
$$\frac{d\psi(t)}{dt} \approx \frac{\psi(k+1) - \psi(k)}{T_s} \quad (23)$$

where  $\psi$  is the parameter for discretization,  $T_s$  is the sampling period and  $k$  is discretized  $t$ .





**Figure 36: Effect of Equivalent Series Resistance (ESR) of capacitor, inductor, and switch turn on resistance (from top to bottom) on efficiency versus output power**



**Figure 37: Maximum power point tracking by MPC**

From the deriving discrete time set of equations, the behavior of control variable can be predicted at next sampling time  $K$ . By using (19)-(22) and (23), the discrete time model of the converter is given by (24)-(27), when the switch is ON ( $\xi = 0$ ):

$$I_L(K+1) = I_L(K) \left[ 1 - R_L \times \frac{T_s}{L} \right] + V_{pv}(K) \times \frac{T_s}{L} \quad (24)$$

$$V_{pv}(K+1) = V_{pv}(K) + [I_{pv}(K) - I_L(K)] \times \frac{T_s}{C} \quad (25)$$

and when the switch is turned OFF ( $\xi = 1$ ):

$$I_L(K+1) = I_L(K) \left[ 1 - R_L \times \frac{T_s}{L} \right] + V_{pv}(K) \times \frac{T_s}{L} - V_{cl}(K) \quad (26)$$

$$V_{pv}(K+1) = V_{pv}(K) + [I_{pv}(K) - I_L(K)] \times \frac{T_s}{C} \quad (27)$$

It can be seen from (24)-(27) that there are four inputs  $I_L$ ,  $V_{pv}$ ,  $I_{pv}$ , and  $V_{cl}$ . In order to reduce the number of required sensors we can rearrange these equations by decreasing the number of input variables. Therefore (25), (26), and (27) can be represented as following

$$V_{pv}(K+1) = 2V_{pv}(K) - V_{pv}(K-1) \quad (28)$$

$$I_L(K+1) = I_L(K) \quad (29)$$

The derived equations can be expressed in matrix form by (30) and (31) when the switch is ON and OFF ( $\xi = \{0,1\}$ ) respectively

$$\begin{bmatrix} I_L(K+1) \\ V_{pv}(K+1) \end{bmatrix} = \begin{bmatrix} 1 - R_L \times \frac{T_s}{L} & \frac{T_s}{L} \\ 0 & 2 \end{bmatrix} \times \begin{bmatrix} I_L(K) \\ V_{pv}(K) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \end{bmatrix} \times V_{pv}(K-1) \quad (30)$$

$$\begin{bmatrix} I_L(K+1) \\ V_{pv}(K+1) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 2 \end{bmatrix} \times \begin{bmatrix} I_L(K) \\ V_{pv}(K) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \end{bmatrix} \times V_{pv}(K-1) \quad (31)$$

The detailed algorithm of the proposed maximum power point tracking methodology using model predictive control is illustrated in Figure 37. The input variables to the algorithm are the  $I_L(k)$  and  $V_{pv}(k)$ , the predicted model of the system are given by (30) and (31). As shown in Figure

37, the predicted value of the inductor current,  $I_L(k+1)$ , is based on contributions from both switch states where  $\xi \in \{0,1\}$  to clearly indicate the two switchings. The MPPT algorithm is based on the fact that the slope of the PV array power curve is zero at the predicted MPP, positive on the left and negative on the right of the predicted MPP. Therefore the voltage and current at MPP can be determined by evaluating the predicted incremental and instantaneous conductance as shown in Figure 37, the increment step of the inductor current at each sampling time is presented by  $(\delta)$  which is added to or subtracted from the  $I_L(k)$  for the determination of the  $I_{L-ref}(k+1)$ . As shown in Figure 37, the  $I_{L-ref}(k+1)$  will be equal to  $I_L(k)$  if

$$\frac{\partial P_{PV}}{\partial v_{PV}} = 0 \quad (32)$$

by using (21):

$$\frac{\partial(i_L v_{PV})}{\partial v_{PV}} = \frac{i_L \partial(v_{PV}) + v_{PV} \partial(i_L)}{\partial v_{PV}} = 0 \quad (33)$$

from (22):

$$i_L + \frac{v_{PV} \partial(i_L)}{\partial v_{PV}} = 0 \quad (34)$$

by using (34), the (35) is determined, if this condition (35) is achieved, the system is operating at MPP and  $I_{L-ref}(k+1)$  will be equal to  $I_L(k)$ :

$$\frac{\Delta i_L}{\Delta v_{PV}} = - \frac{i_L}{v_{PV}} \quad (35)$$

Alternatively, to avoid singularity in (35), the algorithm firstly evaluates  $\Delta v_{PV}$  followed by  $\Delta i_L$ , if  $\Delta v_{PV}$  and  $\Delta i_L$  are zero, the system is operating at MPP and  $I_{L-ref}(k+1)$  will be equal to  $I_L(k)$ . If the slope of the PV array power curve (32) is positive,  $\delta$  will be added to  $I_L(k)$ , and if the slope of the

PV array power curve is negative,  $\delta$  will be subtracted from  $I_L(k)$ . The  $I_{L-ref}(k+1)$  is the current that should be tracked at next sampling time ( $k+1$ ), which is the input for the cost function subject to minimization. The cost function subject minimization is given by

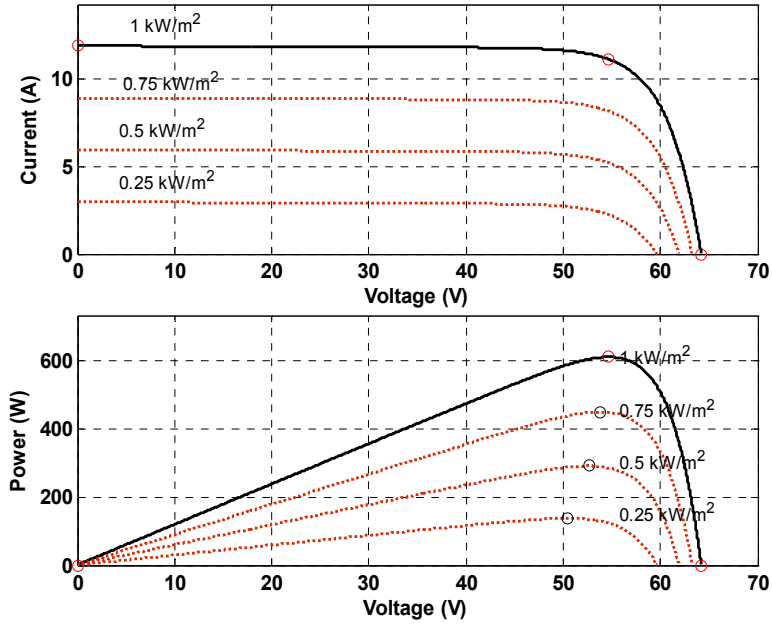
$$g_{\xi \in \{0,1\}} = \left| I_{L-ref}(k+1) - \tilde{I}_L(k+1)_{\xi \in \{0,1\}} \right| \quad (36)$$

The final switching state is the state that minimizes (36); the complete procedure of the controller is summarized in Figure 37.

### 3.5. Results & Discussion

In this chapter the proposed MPC-MPPT is compared to the commonly used INC-MPPT method with fixed variation of the duty cycle of the converter. Directly comparing two control algorithms is challenging to create a fair comparison. However in this chapter, not only the proposed predictive controller technique has faster dynamic response to step change in solar irradiance level, but also it has smaller steady-state ripple power and tracking error. The detail performance comparison of both controllers is presented in this and the following sections.

The I-V and P-V characteristics of the PV system under study for irradiance levels are illustrated in Figure 38. These curves are used as reference to calculate the expected PV side voltage and current at MPP for the experimental efficiency analysis in this chapter. The SUNPOWER SPR-305-WHT is used as PV module type. The PV module characteristics under standard test condition (STC: solar irradiance = 1 kW/m<sup>2</sup>, cell temperature = 25 deg. C) are: open circuit voltage ( $V_{oc}$ ) = 64.2 V, short-circuit current ( $I_{sc}$ ) = 5.96 A, voltage at MPP ( $V_{MP}$ ) = 54.7 V, and current at MPP ( $I_{MP}$ ) = 5.58 A.

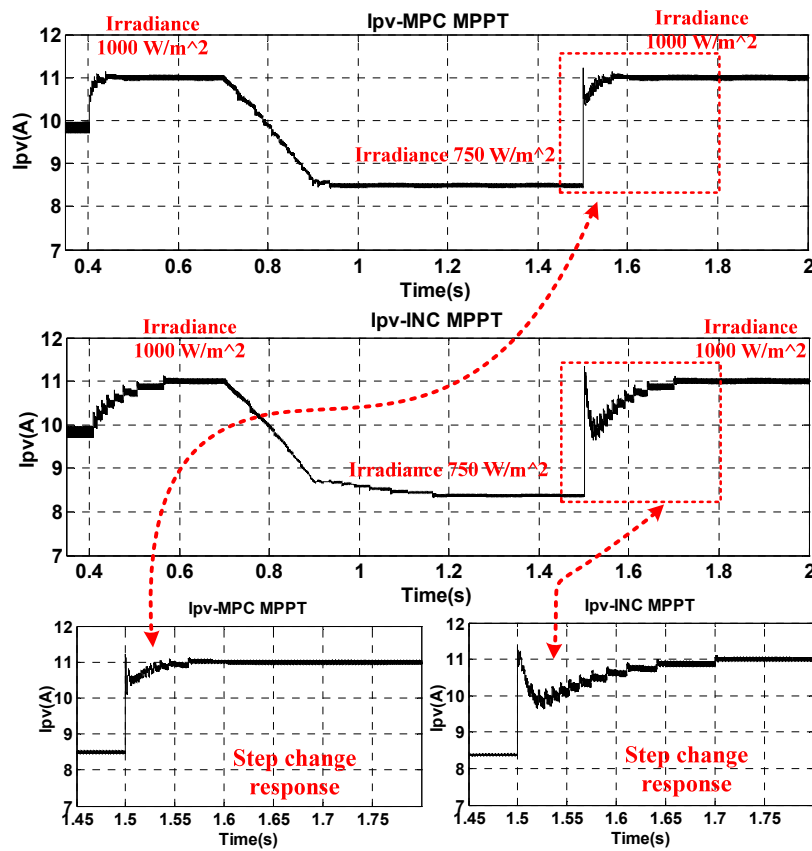


**Figure 38: I-V and P-V characteristics of the array**

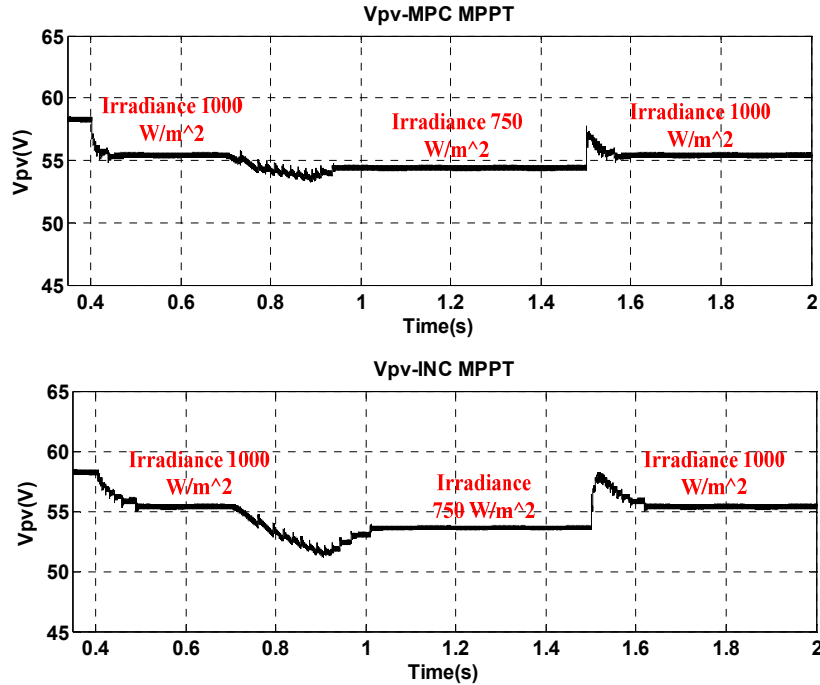
The control algorithm is implemented in Matlab/Simulink; the sampling time  $T_s$  is  $10 \mu s$ . The detail descriptive results are illustrated in Figure 39-Figure 41. By considering continuous operation of the PV systems over the year, the extra amount of energy captured by the proposed MPPT technique is significant, particularly under the cloudy sky condition such as solar irradiance. Combination of the proposed MPPT technique with high efficient inverters can enhance the total efficiency of grid connected PV systems.

Figure 39 and Figure 40 illustrate the simulation results of the proposed MPC and INC method. The MPPT is enabled at  $t=0.4$  s, the system is tested under three irradiance levels changes. The irradiance level of the case study is illustrated in Figure 41. The irradiance was initially  $1000 \text{ W/m}^2$  until time  $0.7$  s, then the irradiance decreases gradually at time  $0.7$  s from  $1000 \text{ W/m}^2$  to  $750 \text{ W/m}^2$ , and finally there is a step change in irradiance level at time  $1.5$  s from  $750 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$ . As shown in Figure 39 the dynamic performance of the MPC method is better than the conventional INC method. More specifically by applying a step change in the irradiance level from

750 W/m<sup>2</sup> to 1000 W/m<sup>2</sup> at time 1.5 s, when using the proposed MPC method the MPP is achieved 0.05 s after the step change. Conversely it is about 0.15 s for conventional INC method, which shows the proposed MPPT technique by MPC is much faster and more efficient than the conventional INC method. The PV power of MPC and INC method are presented in Figure 41, which demonstrates that for approximately similar steady state power value the convergence time to MPP of the proposed MPC method is much smaller comparing to the conventional INC method.



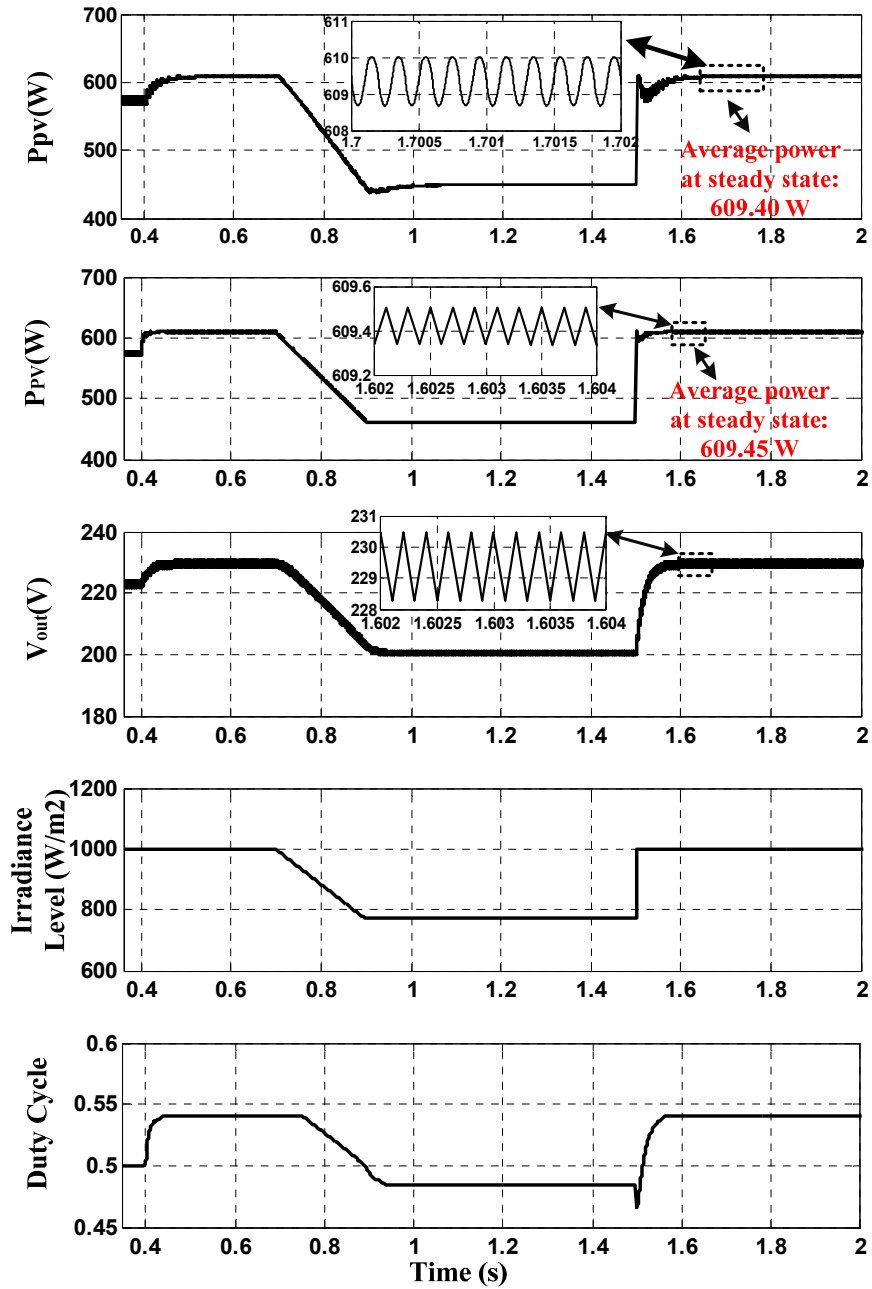
**Figure 39: PV current Simulation results comparison of the MPC versus INC method under irradiance level change**



**Figure 40: PV voltage simulation results comparison of the MPC versus INC method under irradiance level change.**

Agilent E4360A solar array simulator (SAS), Matlab/Simulink, and dSpace DS1103 are used for the experimental results. The control algorithm implemented in Matlab/Simulink and applied to the hardware prototype by using dSpace DS1103 platform. The experimental prototype is illustrated in Figure 42. GeneSiC Semiconductor GA35XCP12-247 used as a switch for the experimental setup. The capacitor and inductor of 470  $\mu$ F and 1 mH are used respectively. The experimental implementation of the MPC-MPPT and INC-MPPT are illustrated in Figure 43-Figure 45 and Figure 46-Figure 48 respectively to validate the simulation results. As it is shown, they confirm the simulation results.





**Figure 41: (From top to bottom) PV power by INC-MPPT, PV power, output voltage of the converter, irradiance level, and duty cycle of the converter switch by MPC-MPPT**

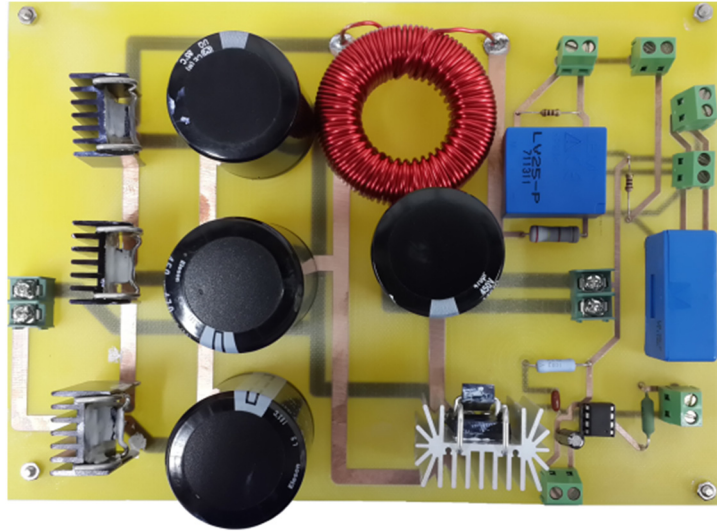


Figure 42: Experimental Setup

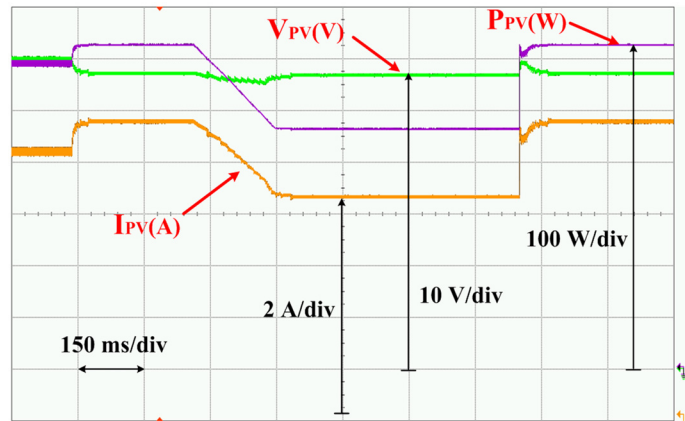


Figure 43: PV current, voltage, and power of MPC-MPPT

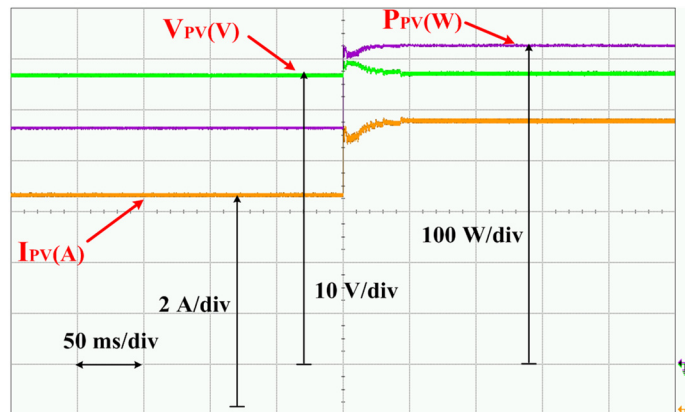


Figure 44: Zoomed in plot of PV current, voltage, and power by proposed MPC-MPPT when the step change in irradiance level at time 1.5 s occur

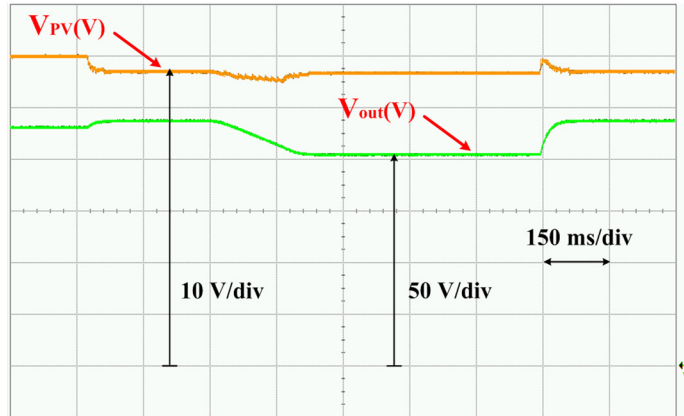


Figure 45: Output to input voltage ratio using MPC-MPPT

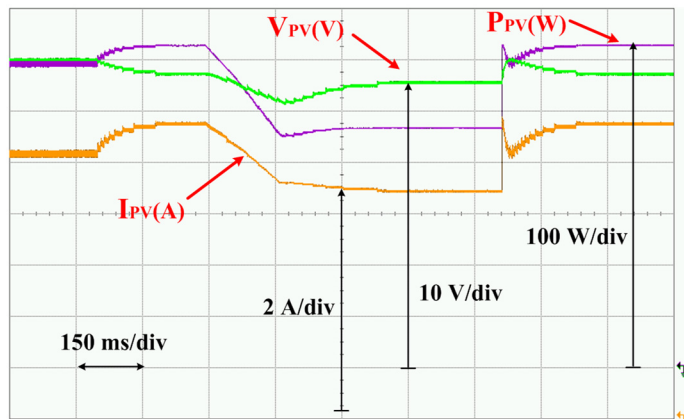


Figure 46: PV current, voltage, and power of INC-MPPT

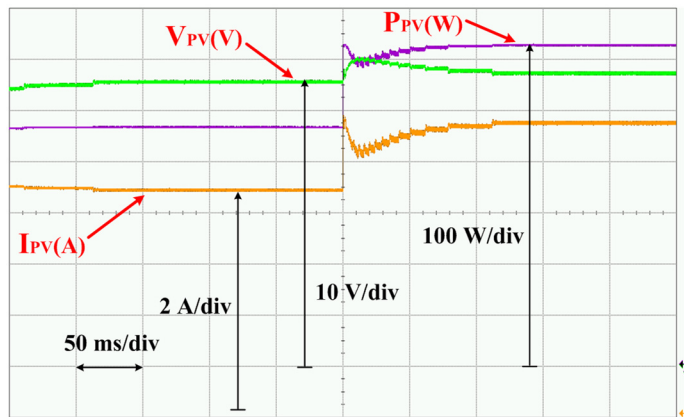
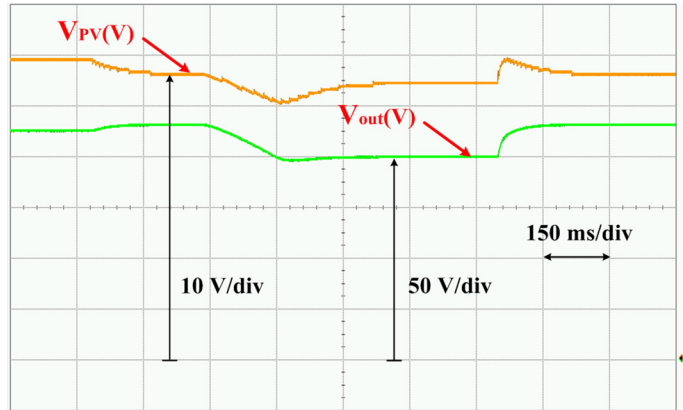


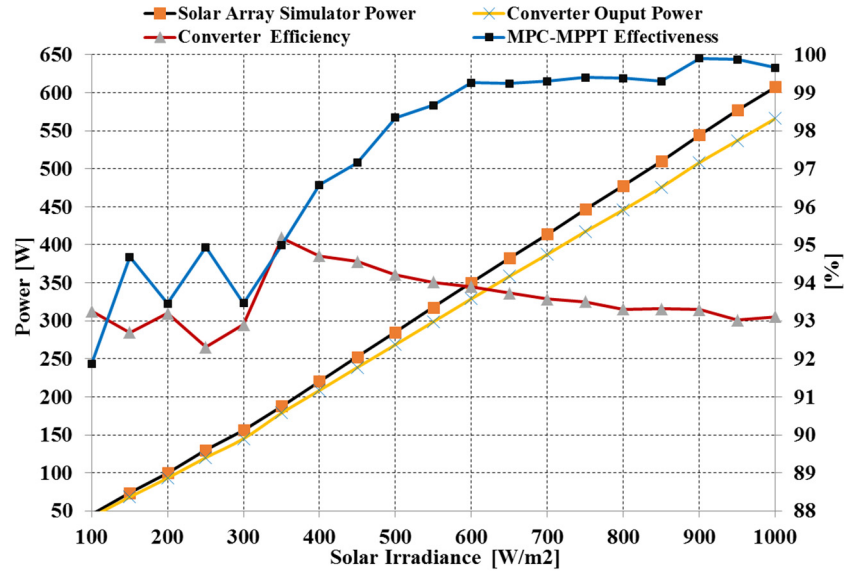
Figure 47: Zoomed in plot of PV current, voltage, and power by proposed INC-MPPT when the step change in irradiance level at time 1.5 s occur



**Figure 48: Output to input voltage ratio using INC-MPPT**

### 3.6. Efficiency analysis

The output power of the Agilent E4360A solar array simulator (converter input power) and the converter output power for solar irradiance levels of  $100 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$  are measured using YOKOGAWA WT1600 digital power meter. The expected power from the solar array simulator at maximum power point is determined using its P-V characteristics curve; these P-V curves for four irradiance levels are illustrated in Figure 38. By using these information, the control effectiveness and converter efficiency of the proposed MPC-MPPT procedure is investigated for solar irradiance levels of  $100 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$ , the results are illustrated in Figure 49. The MPPT control effectiveness is calculated by dividing the measured output power of the solar array simulator by the expected power at MPP from solar array simulator at each solar irradiance level. The converter efficiency is calculated by dividing the measured output power of the converter by the measured output power of the solar array simulator. The results demonstrate that the true maximum power point has been tracked with high efficacy, the worst case scenarios are for the solar irradiance levels of less than  $400 \text{ W/m}^2$  which have control effectiveness of 93%-94%. The output power level of solar array simulator and converter at the corresponding solar irradiance level are also plotted in Figure 49.



**Figure 49: MPC-MPPT control effectiveness, converter efficiency, solar array simulator power, and converter output power for solar irradiance of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>**

Similarly, the efficiency and control effectiveness analysis are done for INC-MPPT method, Figure 50. By comparing the effectiveness of MPC-MPPT to INC-MPPT, it can be observed that the proposed method based on predictive controller is more effective especially at low solar irradiance levels, and the tracked power is closer to the true maximum power point as illustrated in Figure 51. The solar array simulator side voltage and current ripple at MPP are illustrated in Figure 52, this demonstrates that the oscillation around the maximum power point is very small; as a result high effective MPPT is achieved. Also, the converter output voltage and current ripples for solar irradiance levels of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup> are illustrated in Figure 53, the results demonstrate that the ripples are small. Table 4 presents the comparison summary between MPC-MPPT and INC-MPPT. The table shows that the proposed method has smaller maximum percentage of overshoot/undershoot, smaller power oscillation around maximum power point with faster convergence time, and higher control effectiveness. By considering continuous operation of

the proposed PV energy harvesting system over the year, the extra amount of energy harnessed is significant, particularly under the dynamic weather condition.

MPC uses the system parameters model for selecting optimal actuation, therefore analyzing the effect of model parameter mismatch on control effectiveness is of high interest. To investigate the robustness of the proposed MPC-MPPT technique to parameters mismatch, up to  $\pm 30\%$  changes of the nominal load value is assumed as a load ( $R_o$ ) disturbance. The response of the proposed MPC-MPPT to this load disturbance is evaluated by control effectiveness analysis for solar irradiance levels from  $100 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$ , the result is presented by the contour plot of Figure 54. The nominal value of the load is shown as 100% load disturbance in Figure 54 which has the control effectiveness of more than 93% from low to high solar irradiance level. The control effectiveness of the proposed MPC-MPPT with load disturbances of  $\pm 10\%$  shows almost similar to nominal value (with control effectiveness of more than 96%) for solar irradiances of  $400 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$  which demonstrates approximately 100% disturbance rejection. As the load disturbances increased more than  $\pm 10\%$ , the average disturbance rejection achieved is 97% for solar irradiances of  $500 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$ , and 94.5% for irradiance levels of  $100 \text{ W/m}^2$  to  $500 \text{ W/m}^2$ . As it is shown in contour plot of Figure 54, for the highest ( $\pm 30\%$ ) disturbance in the load and low solar irradiance levels (less than  $300 \text{ W/m}^2$ ), the control effectiveness drops to 87% which shows the worst case scenario.

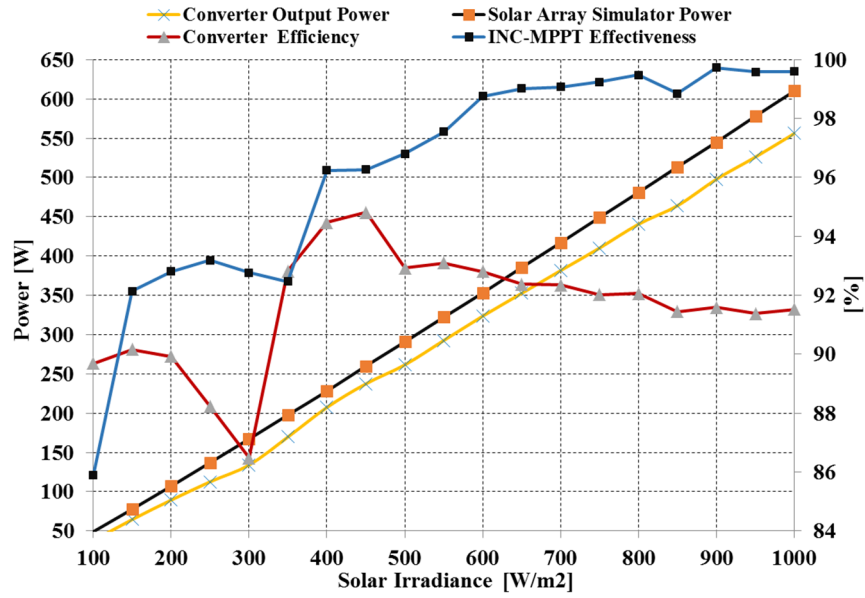


Figure 50: INC-MPPT control effectiveness, converter efficiency, solar array simulator power, and converter output power for solar irradiance of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>

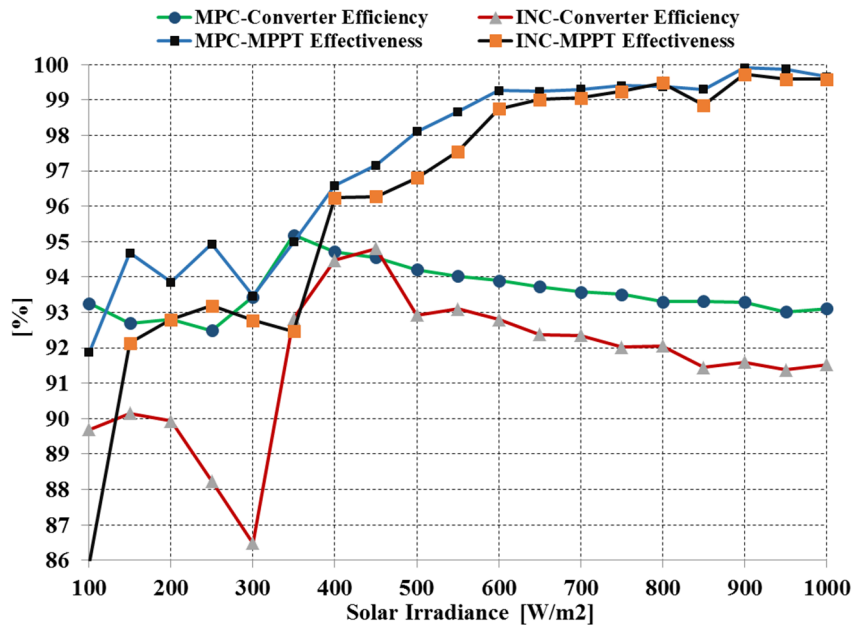


Figure 51: Comparison of INC and MPC control effectiveness and converter efficiency for solar irradiance levels of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>

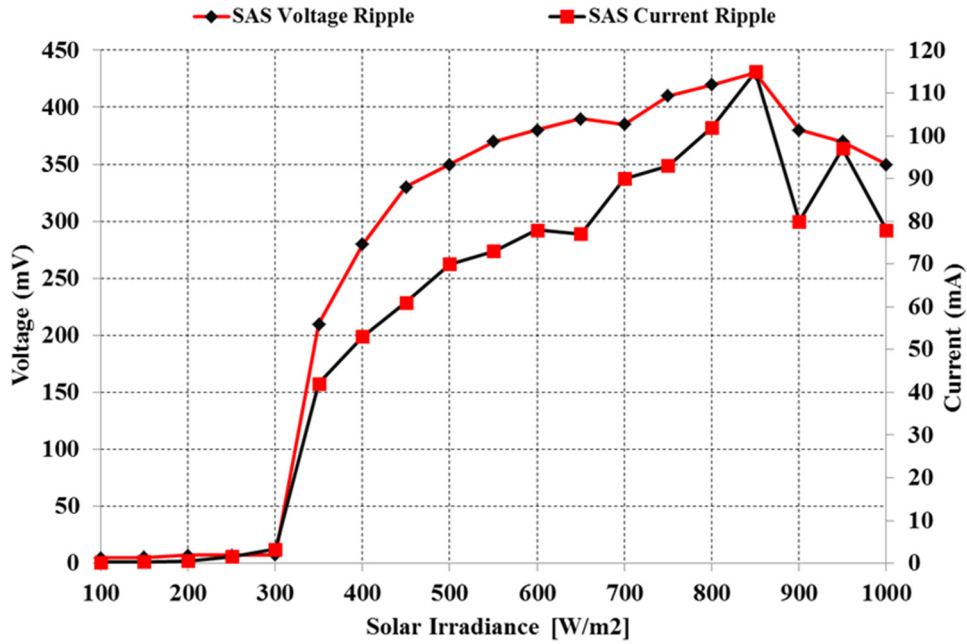


Figure 52: Solar array simulator (SAS) voltage and current ripple for solar irradiance of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>

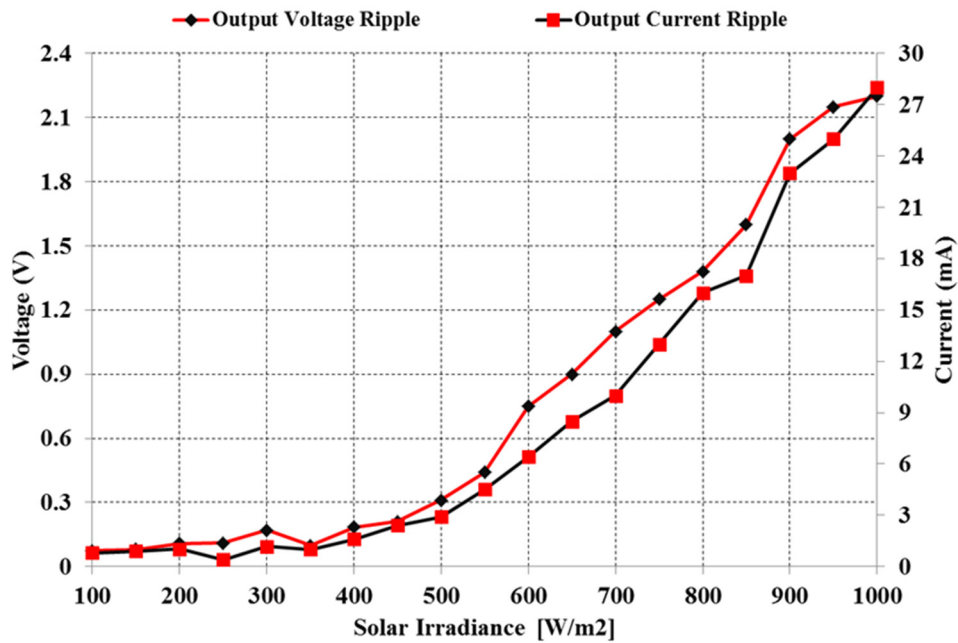
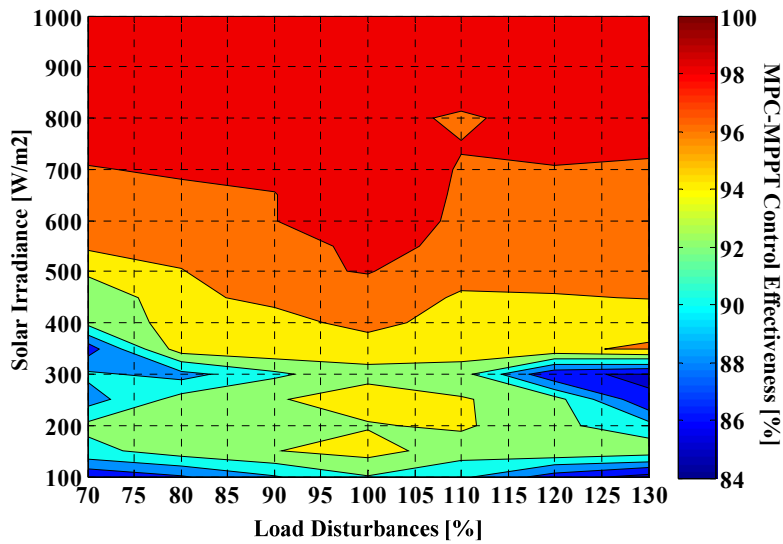


Figure 53: Output voltage and current ripple for solar irradiance of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>



**Table 4. INC-MPPT versus MPC-MPPT comparison of step change dynamic performance (750 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>) and steady state performance (1000 W/m<sup>2</sup>)**

Characteristics	INC-MPPT	MPC-MPPT
% of voltage ripple	0.79%	0.63%
% of current ripple	1.06%	0.72%
Steady state power	609.40 W	609.45 W
PV current overshoot/undershoot	11.07%	9.7%
PV voltage overshoot/undershoot	5.51%	4.78%
Convergence time	0.15 s	0.05 s
Control effectiveness	99.60%	99.65%



**Figure 54: The contour plot of the MPC-MPPT control effectiveness versus the disturbances in load for solar irradiance of 100 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>, the 100% load disturbance is the nominal value of the load**

### 3.7. Conclusion

This chapter presents an effective MPPT technique using the model predictive control framework. The performance of the proposed MPC-MPPT technique is compared to commonly used INC-MPPT method. The results demonstrate that by predicting the error at next sampling time before applying the switching signal when using the proposed MPC method in an elegant, embedded controller has faster dynamic response and higher efficiency at steady state than the

conventional INC technique. This higher performance is achieved under rapidly changing atmospheric condition without requiring expensive sensing and communication equipment and networks to directly measure the changing solar radiation.

## 4. MAXIMUM POWER POINT TRACKING OF GRID-TIED PHOTOVOLTAIC SYSTEMS\*

This chapter presents a maximum power point tracking (MPPT) technique using model predictive control (MPC) for single phase grid connected photovoltaic (PV) systems. The technique exhibits fast convergence, which is ideal for rapidly varying environmental conditions such as changing temperature or insolation or changes in morphology of the PV array itself. The maximum power of the PV system is tracked by a high gain DC-DC converter and is fed to the power grid through a seven-level inverter. Considering the stochastic behavior of the solar energy resources and the low conversion efficiency of PV cells, operation at the maximum possible power point is necessary to make the system economical. The main contribution of this chapter is the development of the incremental conductance (INC) method using a two-step model predictive control. The multilevel inverter controller is based on fixed step current predictive control with small ripples and low total harmonic distortion (THD). The proposed MPC method for the grid connected PV system speeds up the control loop by sampling and predicting the error two steps ahead before the switching signal is applied. As a result, more energy is extracted from the PV system and injected into grid particularly during partially cloudy sky. A comparison of the developed MPPT technique to the conventional INC method shows significant improvement in dynamic performance of the PV system. Implementation of the proposed predictive control is presented using the dSPACE DS1103.

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\* Portions of this chapter have been previously published in M. B. Shadmand, M. Mosa, R. S. Balog, and H. Abu Rub, "Maximum Power Point Tracking of Grid Connected Photovoltaic System Employing Model Predictive Control," Applied Power Electronics Conference & Exposition (APEC), March, 2015, © 2015 IEEE.

#### 4.1. Description of the Complete System

The PV array can feed power to the grid through a DC/DC converter boosting the output voltage and a grid connected inverter [123-130]. The main contribution of this chapter is the development of the INC method using a two-step model predictive control for a multilevel boost DC-DC converter. The boost converter output power is fed to the ac grid through a seven level inverter controlled by model based current predictive method. By predicting the future behavior of the PV system, the proposed MPC method in an elegant, embedded controller that has faster response than the conventional INC technique under rapidly changing atmospheric conditions. The proposed control does not require expensive sensing and communications equipment and networks to directly measure the changing solar insolation.

Figure 55 illustrates the general schematic of the complete grid connected photovoltaic system controlled by predictive methods. As it is shown, the system contains a multilevel DC-DC boost converter to extract the maximum power from the PV arrays and to feed it into the grid through a seven level inverter. Since only one switch is used in the selected multilevel boost DC-DC converter topology, the control procedure is simpler than other topologies such as the switched capacitor converter with a boost stage [116]. The output voltage of the DC-DC converter is proportional to the number of levels, which can be increased by adding two additional capacitors and diodes.

The DC-DC converter in this chapter has three levels. At the dc-link stage of the system, if the average voltage across the capacitor  $C_1$  is  $V_{dc}$ , then the average voltage across capacitors  $C_2$  and  $C_3$  together will be  $2V_{dc}$ . The detail mode of operation of this DC-DC converter with two levels is presented in [104], this concept can be extended for the three levels topology presented in this chapter.

The seven level inverter topology used to feed power to the grid can be divided into two parts: multilevel module and H-bridge inverter. The multilevel module is cascaded with an H-Bridge inverter operating at low switching frequency (120Hz) to reduce the switching losses. Table 5 demonstrates the summary of the output voltage levels as a function of switching states. The state of the switches can be represented by 0 and 1, where state 0 means the switch is OFF, and state 1 means the switch is ON.

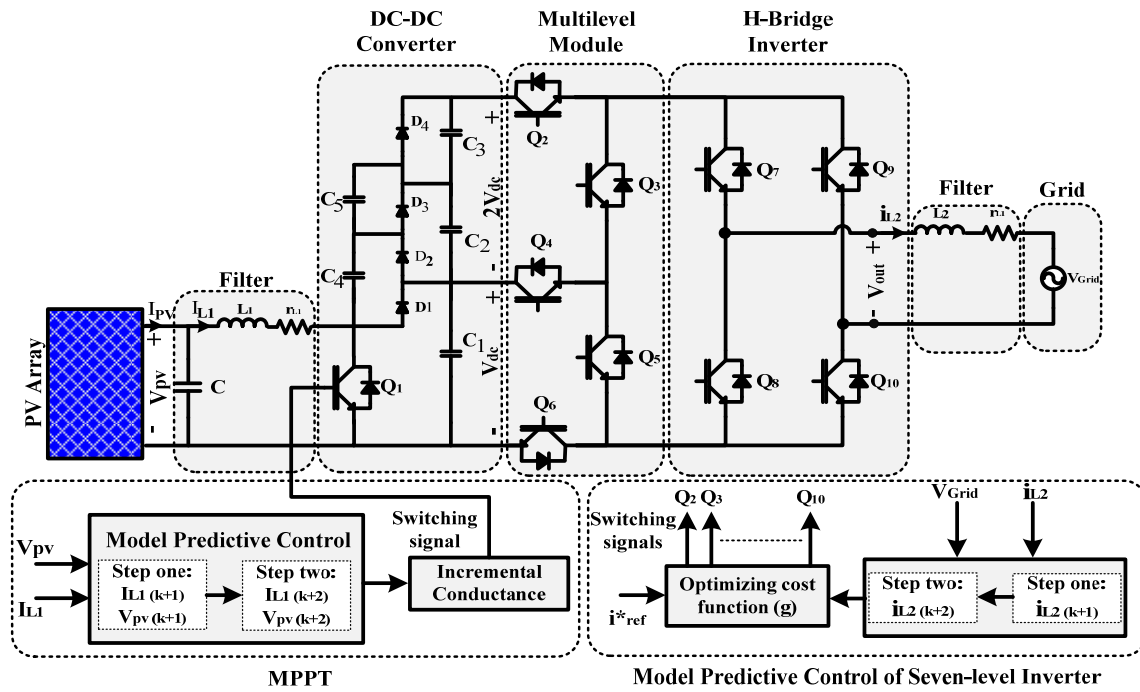


Figure 55: General schematic of the system and proposed model predictive control for grid connected PV system

Table 5: Summary of output voltage levels as function of switching states

Output Voltage ( $V_{out}$ )	Multilevel Inverter Switches States								
	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$Q_7$	$Q_8$	$Q_9$	$Q_{10}$
$+3V_{dc}$	1	0	0	0	1	1	0	0	1
$+2V_{dc}$	1	0	1	1	0	1	0	0	1
$+V_{dc}$	0	1	1	0	1	1	0	0	1
0	0	1	0	1	0	1	0	0	1
$-V_{dc}$	0	1	1	0	1	0	1	1	0
$-2V_{dc}$	1	0	1	1	0	0	1	1	0
$-3V_{dc}$	1	0	0	0	1	0	1	1	0

## 4.2. Model Predictive Control of the System

### 4.2.1. Predictive Maximum Power Point Tracking

The discrete time model of the DC-DC converter is used to determine predicted control variables:

$$I_{L1}(K+n+1) = I_{L1}(K+n) \left[ 1 - r_{L1} \times \frac{T_s}{L_1} \right] + V_{PV}(K) \times \frac{T_s}{L_1} - (1-S) \times V_C(K+n) \quad (1)$$

$$V_{PV}(K+n+1) = V_{PV}(K) + [I_{PV}(K+n) - I_{L1}(K+n)] \times \frac{T_s}{C} \quad (2)$$

where  $n+1$  is the number of steps in the future being predicted at the current  $K^{\text{th}}$  step;  $S$  is 1 when the switch is ON and 0 when the switch is OFF; and  $T_s$  is the sampling time. In this chapter the control variables predicted two steps in horizon. Equations (1) and (2) have four inputs  $I_{L1}$ ,  $V_{PV}$ ,  $I_{PV}$ , and  $V_C$ . In order to reduce the number of sensors, these equations can be rearranged by decreasing the number of input variables. Thus (2) can be represented as

$$V_{PV}(K+2) = 2V_{PV}(K+1) - V_{PV}(K) \quad (3)$$

In order to calculate the value of control variables at time  $K+2$ , the estimated value of the current of the inductor,  $L_1$ , and PV voltage at time  $K+1$  are used. Thus at sampling time  $K+2$ , four values for control variables are predicted and the optimum value will be selected as illustrated graphically in Figure 56. The derived equations can be expressed in matrix form by (4) and (5) when the switch is ON and OFF respectively

$$\begin{bmatrix} I_{L1}(K+2) \\ V_{PV}(K+2) \end{bmatrix} = \begin{bmatrix} 1 - r_{L1} \times \frac{T_s}{L_1} & \frac{T_s}{L_1} \\ 0 & 2 \end{bmatrix} \times \begin{bmatrix} I_{L1}(K+1) \\ V_{PV}(K+1) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \end{bmatrix} \times V_{PV}(K) \quad (4)$$

$$\begin{bmatrix} I_{L1}(K+2) \\ V_{PV}(K+2) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 2 \end{bmatrix} \times \begin{bmatrix} I_{L1}(K+1) \\ V_{PV}(K+1) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \end{bmatrix} \times V_{PV}(K) \quad (5)$$

The summary of the proposed MPPT algorithm is illustrated in Figure 57.

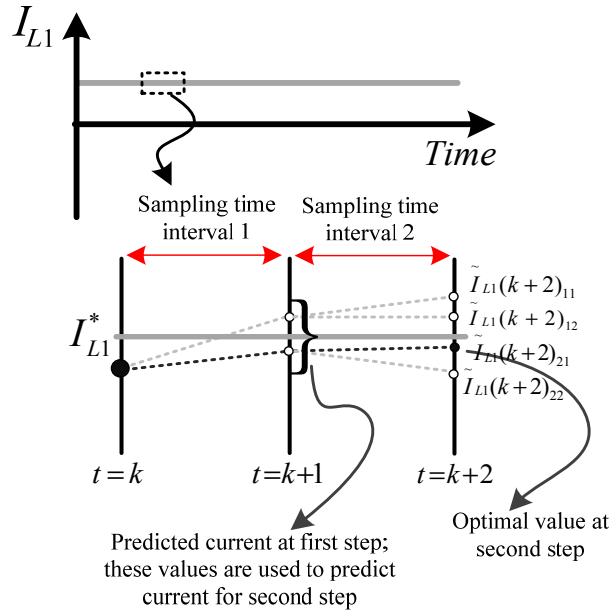
### 4.2.1. Predictive Current Control

The next step is the current predictive control of the multilevel inverter. The load current in continuous form can be determined using the following expression

$$v_{out} = L_2 \frac{di_{L2}}{dt} + r_{L2}i_{L2} + v_{Grid} \quad (6)$$

By using the Euler forward method, the derivative in (6) can be approximately discretize as

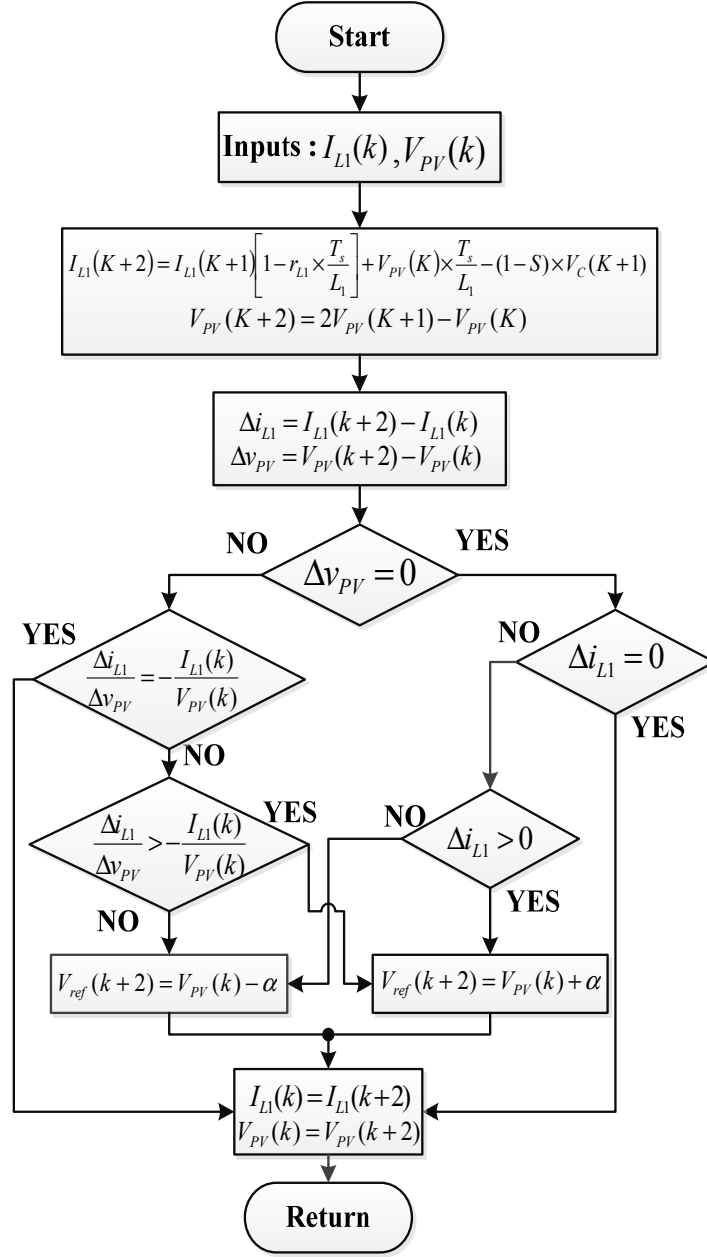
$$L_2 \frac{di_{L2}}{dt} = L_2 \frac{i_{L2}(K+1) - i_{L2}(K)}{T_s} \quad (7)$$



**Figure 56: Prediction of PV array side current observation**

where  $T_s$  is the sampling period. Based on (6) and (7) the load side current can be predicted for  $n$  steps in horizon of time by using

$$i_{L2}(K+n) = \left[ 1 - \frac{r_{L2}T_s}{L_2} \right] i_{L2}(K+n-1) + \frac{T_s}{L_2} (v_{out}(K+n-1) - v_{Grid}(K+n-1)) \quad (8)$$



**Figure 57: MPC maximum power point tracking procedure**

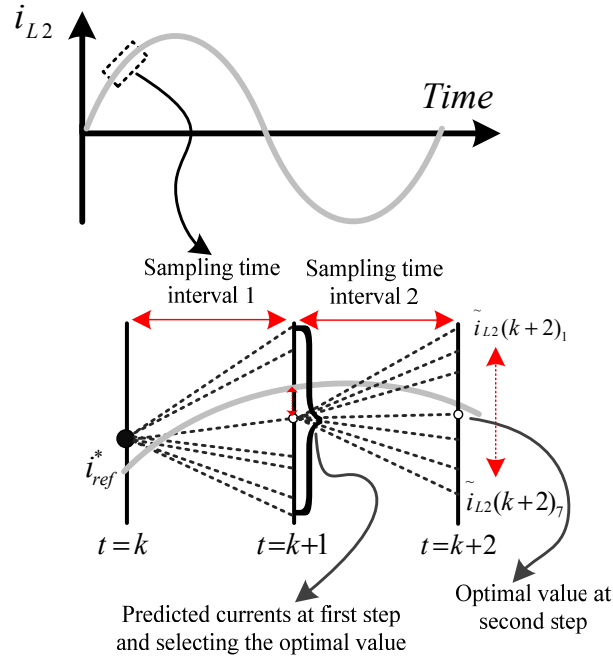
where  $i_{L2}(K+n)$  is the predicted value of the grid side current at time  $K+n$ . In this chapter,  $i_{L2}$  is predicted two steps,  $n=2$ , into the horizon of time as illustrated in Figure 58. The reference current to be tracked and the cost function,  $g$ , are given by



$$i_{ref}^*(K+n) = \frac{2}{220\sqrt{2}} I_{PV}(K+n) \times V_{PV}(K+n) \quad (9)$$

$$g = |i_{ref}^*(K+n) - i_{L2}(K+n)| \quad (10)$$

The cost function needs to be minimized by evaluating all of the possible switching states presented in Table 5 for each step. The summary of optimal switching state selection procedure is illustrated in Figure 59.



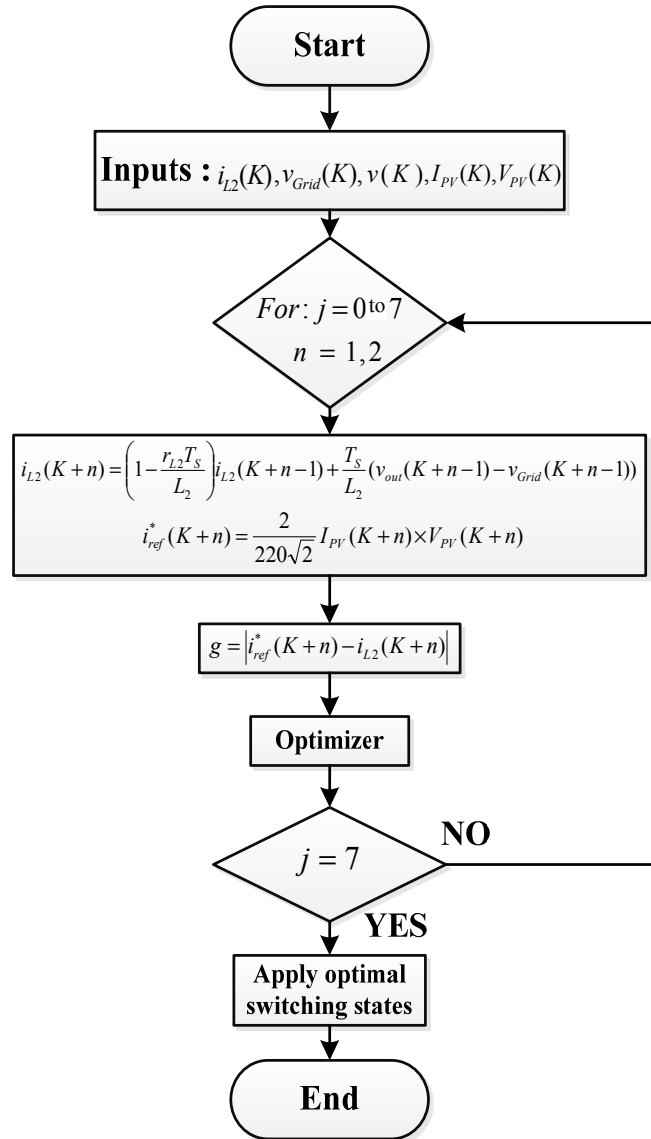
**Figure 58: Prediction of grid side current observation**

### 4.3. Results and Discussion

The proposed controller for the PV system is modeled in MATLAB-Simulink, and implemented in dSPACE DS1103. The I-V and P-V characteristics of the PV system for different irradiance levels are illustrated in Figure 60. The SUNPOWER SPR-305-WHT is used as PV module type. The PV module characteristics under standard test condition (STC: solar irradiance = 1 kW/m<sup>2</sup>, cell temperature = 25 deg. C) are:

- Open circuit voltage (Voc) = 64.2 V

- Short-circuit current ( $I_{sc}$ ) = 5.96 A
- Voltage at MPP ( $V_{MP}$ ) = 54.7 V
- Current at MPP ( $I_{MP}$ ) = 5.58 A



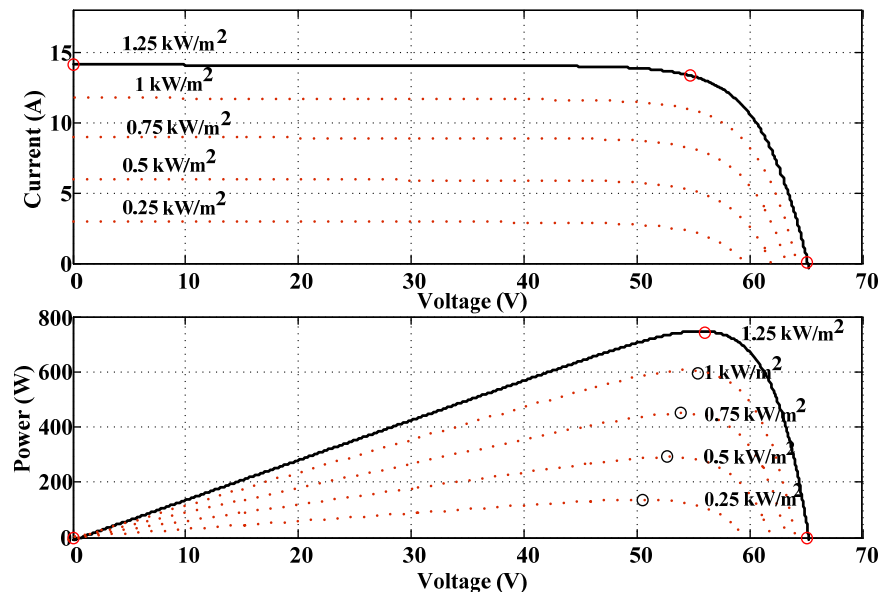
**Figure 59: Model predictive control of the multilevel inverter**

The sampling time,  $T_s$ , is 10  $\mu$ s. In this chapter the MPC for MPPT is compared to the commonly used incremental conductance method. Figure 61 illustrates the simulation results of the proposed MPC and INC method. As it is shown, when the MPPT is enabled at time 0.1 s, the

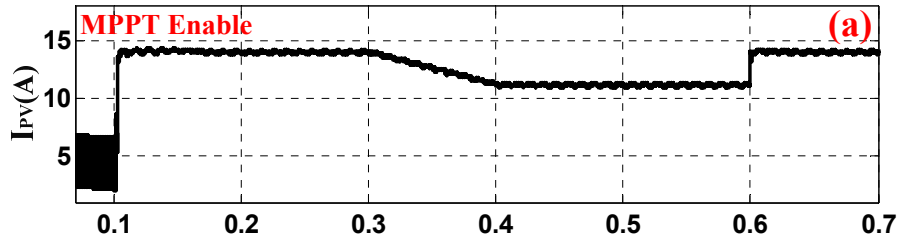
irradiance decreases gradually at time 0.3 s from 1250 W/m<sup>2</sup> to 1000 W/m<sup>2</sup>, and finally there is a step change in irradiance level at time 0.6 s from 1000 W/m<sup>2</sup> to 1250 W/m<sup>2</sup>. By comparing

Figure 61 (d) and (g) to (i) and (h) respectively, it can be noticed that the maximum power is tracked much faster when using two steps in MPC-MPPT than the conventional INC-MPPT method. The maximum power point when using two steps MPC-MPPT is achieved 1 ms after the step change in solar irradiance occurred. Conversely, it is about 4 ms for conventional INC-MPPT. By considering continuous operation of the PV systems over the year, the extra amount of energy captured by the proposed MPPT technique is significant, particularly under the cloudy sky condition such as solar irradiance level.

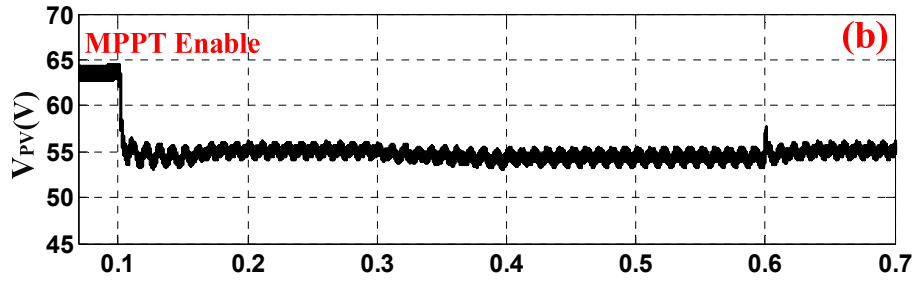
The simulation results of the grid side voltage and current, using MPC for the multilevel inverter, is illustrated in Figure 62. Figure 62 (a) and (c) show that the unity power factor is achieved and that the controller response to the step change in solar irradiance level at time 0.6 s is very fast.



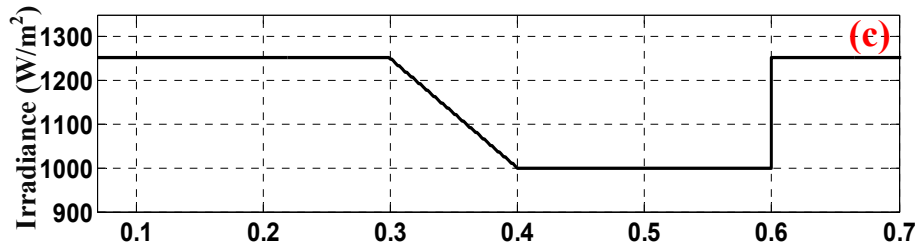
**Figure 60: I-V and P-V characteristics of the PV array**



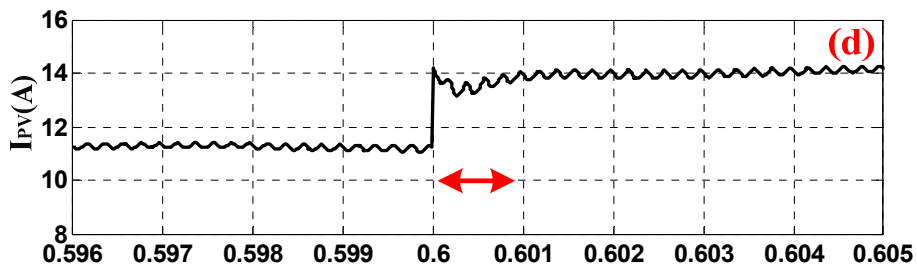
(a) PV current by proposed MPC-MPPT



(b) PV voltage by proposed MPC-MPPT

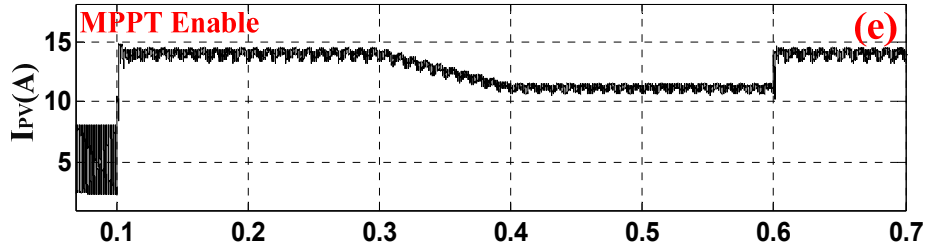


(c) Irradiance level

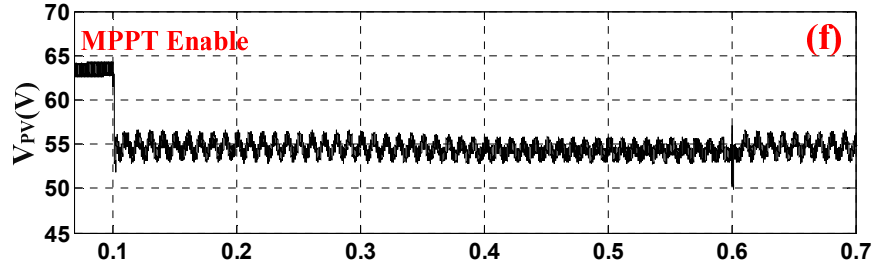


(d) Zoomed in plot of PV current by proposed MPC-MPPT when the step change in irradiance level at time 0.6 s occur

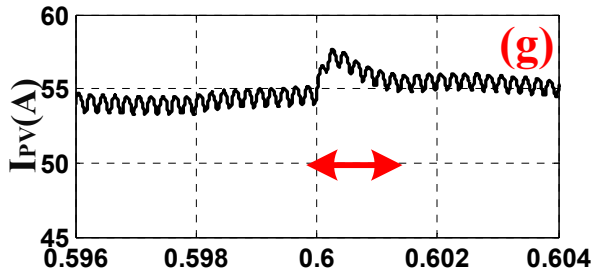
**Figure 61: Simulation results of MPPT**



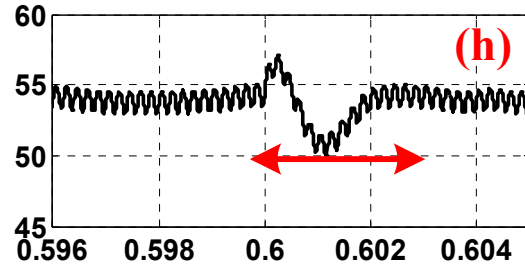
(e) PV current by INC-MPPT



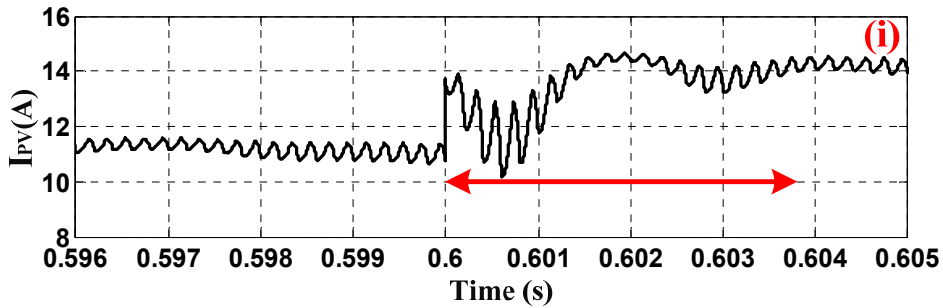
(f) PV voltage by INC-MPPT



(g) Zoomed in plot of PV voltage by MPC-MPPT at time 0.6 s



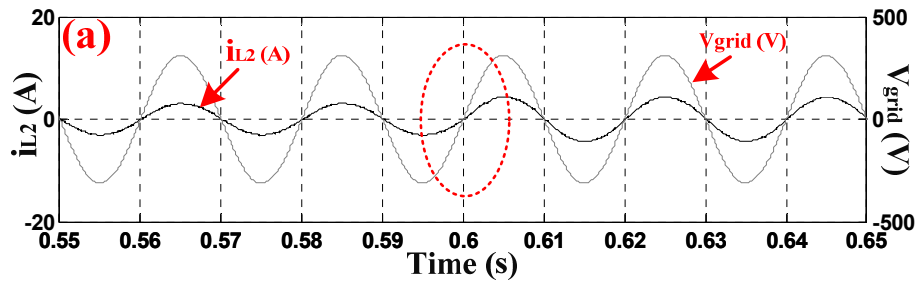
(h) Zoomed in plot of PV voltage by INC-MPPT at time 0.6 s



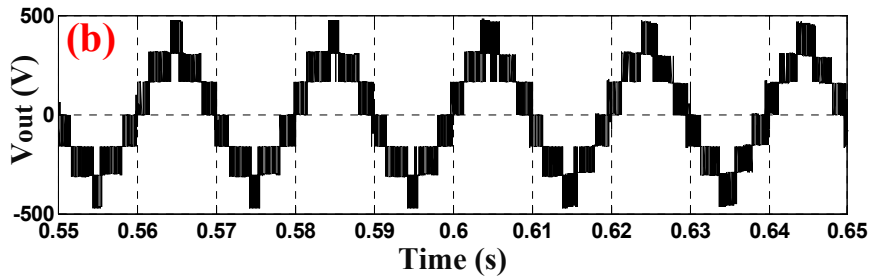
(i) Zoomed in plot of PV current by INC-MPPT at time 0.6 s

**Figure 61: Continued**

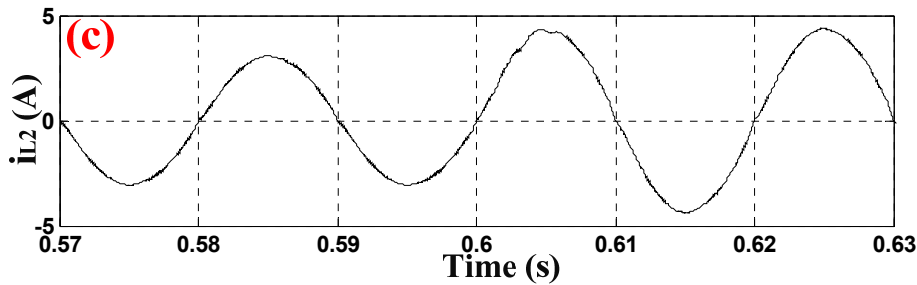
The simulation results are validated experimentally by real-time implementation of the control strategy with dSPACE DS1103. Figure 63 (a) illustrates the PV side voltage and current, the step change response at time 0.6 s is zoomed in. Figure 63 (b) demonstrates the output voltage of the 7 level grid connected inverter. The grid side voltage and current are illustrated in Figure 63 (c) when the step change occurs in solar irradiance at time 0.6 s. As it is illustrated the injected current to the grid has fast dynamic response. The THD of the grid side current is about 1.8% which is within the IEEE-519 standard [131].



(a) Grid side voltage and injected current

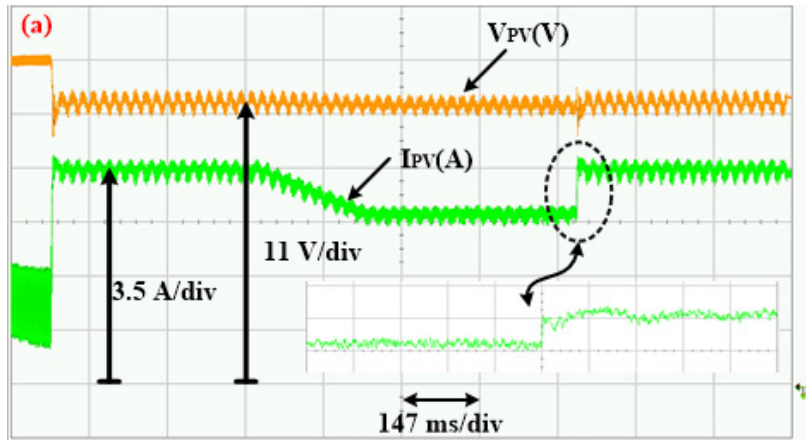


(b) Output voltage of the 7 level inverter

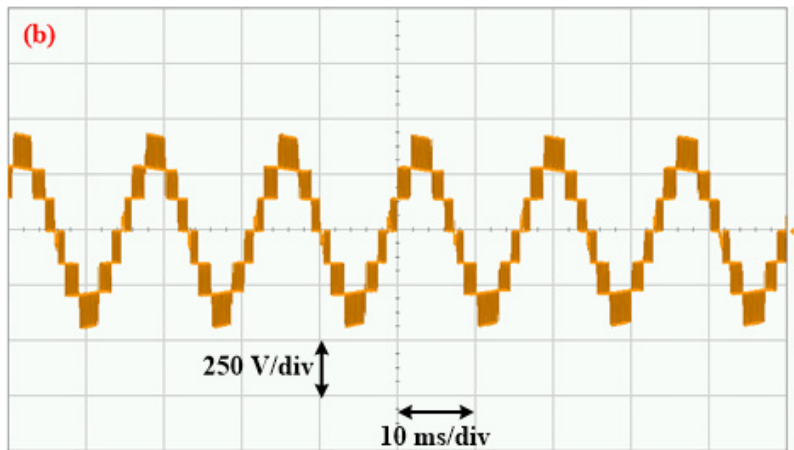


(c) Zoomed in plot of the injected current to the grid by using MPC-MPPT and predictive control of 7 level inverter at time 0.6 s

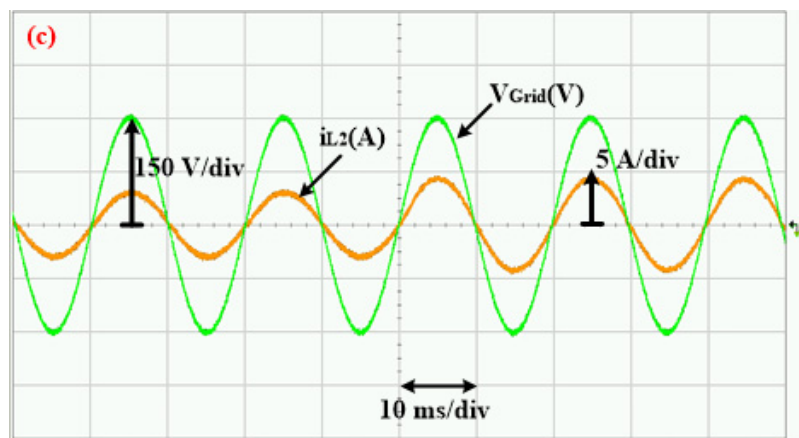
**Figure 62: Simulation result of grid side**



(a) PV voltage and current by proposed MPC-MPPT technique

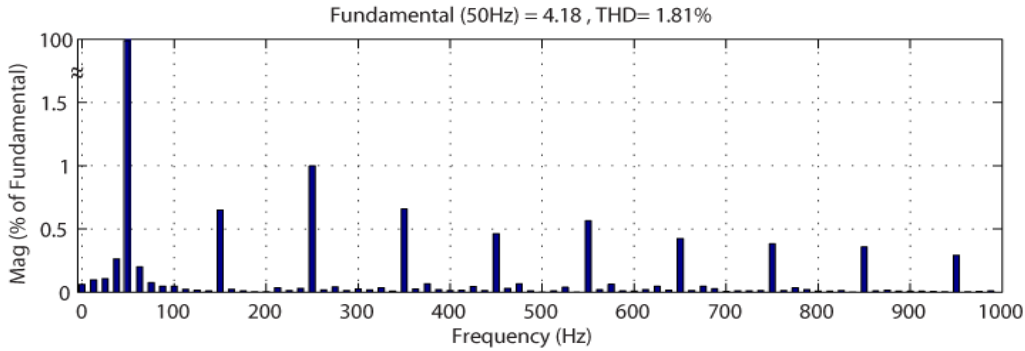


(b) Output voltage of the 7 level grid connected inverter



(c) Grid side voltage and injected current

**Figure 63: Experimental validation of the control algorithm by real-time implementation**



**Figure 64: Spectrum analysis of grid side current ( $i_{L2}$ )**

#### 4.4. Conclusion

This chapter presents an improved MPPT technique using MPC for grid connected photovoltaic systems by predicting the error at the next sampling time before applying the switching signal. The proposed two steps predictive MPPT technique is compared to the commonly used INC method to show improvement in the dynamic performance and efficiency of the MPPT. The technique exhibits fast convergence, which is ideal for rapidly varying environmental conditions such as changing temperature or insolation or changes in morphology of the PV array itself. As a result, more energy will be captured from the PV system and injected into grid particularly during partially cloudy sky without requiring extra sensing and communications equipment and networks to directly measure the changing solar insolation.

The maximized captured energy is fed to the grid through a 7 level inverter controlled by means of predictive control. High quality current, with low THD and in-phase with the grid voltage, is achieved and injected into the grid by using the proposed predictive controller. The dSPACE DS1103 is used for implementing the control technique experimentally.



## 5. HIGH PERFORMANCE PREDICTIVE CONTROL OF QUASI IMPEDANCE SOURCE INVERTER\*

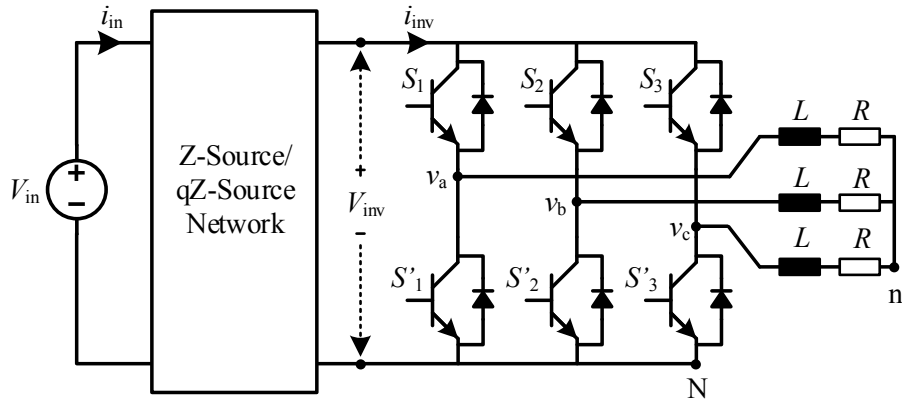
The quasi-Z-source inverter (qZSI) has attracted much attention for motor drives and renewable energy applications due to its capability to boost or buck in a single converter stage. However, this capability is associated with different challenges related to the closed loop control of currents, control the DC capacitor voltage, produce three-phase AC output current with high dynamic performance and obtain continuous and low ripple input current. This chapter presents a predictive control strategy for a three-phase qZSI that fulfills these requirements without adding any additional layers of control loops. The proposed controller implements a discrete-time model of the qZSI to predict the future behavior of the circuit variables for each switching state, along with a set of multi-objective control variables all in one cost function. The quasi impedance network and the AC load are considered together when designing the controller in order to obtain stability of the impedance network with a step change in the output reference. A detailed comparative investigation between the proposed controller and the conventional PI controller is presented to prove the superiority of the proposed method over the conventional control method. Simulation and experimental results are presented.

### 5.1. Traditional Feedback Controller for QZSI

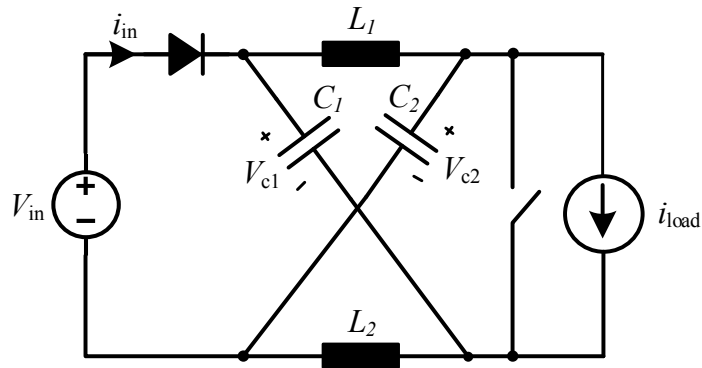
A DC-DC converter is often connected along with a DC-AC inverter to provide well-regulated AC output voltage from a DC source. While this approach decouples the voltage gain from the

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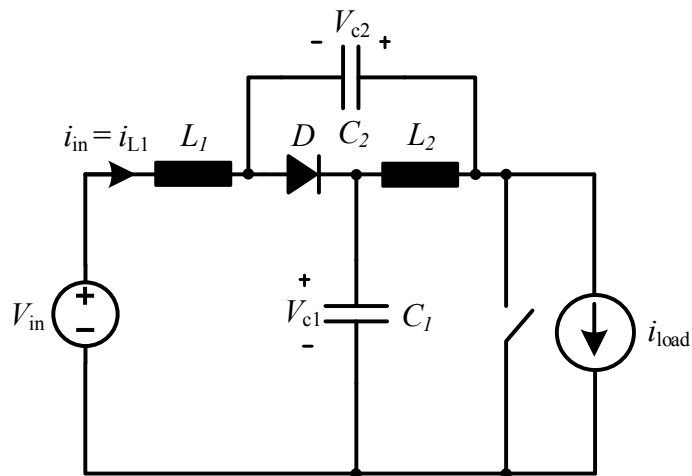
\* Portions of this chapter have been previously published in M. Mosa, R. S. Balog and H. Abu-Rub, "High-Performance Predictive Control of Quasi-Impedance Source Inverter," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 3251-3262, April 2017 © 2017 IEEE.



(a) Three-phase Z-source/qZ-source inverter with RL load



(b) Z-source impedance network with a simplified three-leg inverter



(c) qZ-source impedance network with a simplified three-leg inverter.

**Figure 65: Z-source/qZ-source inverter**

inverter action, the two-stage topology requires more active switches in the path of the power flow, which increases losses and cost. Impedance source inverters are a class of inverter topologies that enable the boost or buck of the input voltage and the ac conversion in a single stage by using a passive network shown in Figure 65(a), which is connected between the source and the active switches [132-138]. Unfortunately, the input current " $i_{in}$ " of the Z-source inverter (ZSI) which is shown in Figure 65(b) is discontinuous because the diode disconnects the Z-network from the source, which may be undesirable for some sources such as solar cells and fuel cells. To overcome this drawback, the qZSI, shown as a combination of the inverter in Figure 65(a) and the network in Figure 65(c), was proposed so that input current  $i_{in}$  would be continuous [139-144]. The additional benefits of the qZSI over the conventional ZSI are that the capacitor ( $C_2$ ) operates with lower voltage stresses and it offers common ground between the source and the DC-link [139].

Without loss of generality, the Z-source and Quasi Z-source networks in Figure 65(b) and Figure 65(c) are shown connected to a three-phase conventional inverter bridge and load in Figure 65(a). To understand the operation of the topology, the three-leg inverter is replaced by a single switch and the load is represented by a current source. The switch represents the overlap-mode of the three-phase inverter during which both the high and the low-side bridge switches are turned on simultaneously, often referred to in the literature as shoot-through mode, which is the mechanism responsible for boosting the input voltage. To regulate the input current, the DC capacitor voltage, and AC output current in the single stage qZSI, complex feedback control techniques have been proposed to optimize the value of the shoot-through duty ratio and the modulation index [145-148].

Other control techniques, like capacitor voltage control method [149-151], are designed using the simplified small signal model in Figure 65 where the load is represented as an ideal

current source [152]. While this model describes the dynamic of the impedance network, it ignores the dynamics of the load. A higher-order model incorporates the load dynamics into the control design at the expense of increasing the control complexity and requires fine-tuning [147],[140, 153-155].

This chapter presents the use of finite-state model predictive control (MPC) for the qZSI. MPC is a class of controller which has emerged as a very powerful method for electrical power converters [140, 156-158] because it is straightforward to implement and has the ability to incorporate variables and constraints without needing structural changes to the main control design [157, 159, 160]. A side-effect of MPC is that without a modulator the switching frequency is not enforced to be constant. However, this may be beneficial since the result of variable-frequency switching is that switching harmonics are distributed across the frequency spectrum which reduces the amplitude of individual harmonic components – similar to adding dither to fixed-frequency switching. Another benefit of MPC is that multiple control objectives are readily incorporated into the cost function – the quality of output waveform and the stability of qZ-network can all be regulated with a suitably formulated qZSI model. These advantages can improve the overall performance and efficiency of qZ-source inverters controlled by MPC.

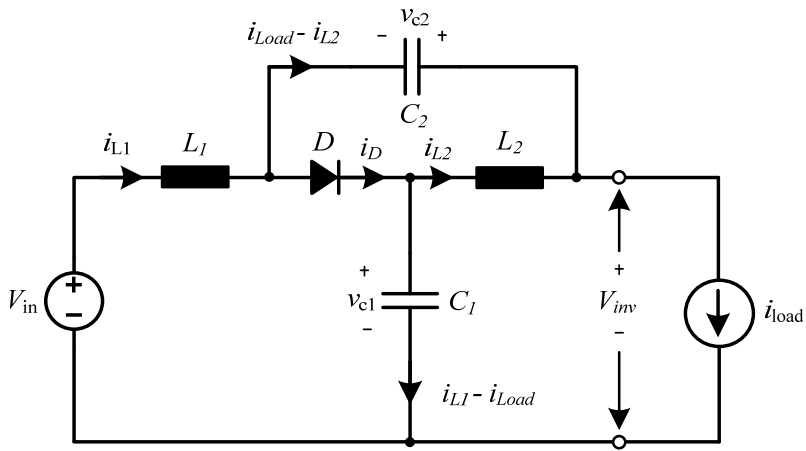
This chapter proposes an extension of the predictive control technique for qZSI which was initially presented by the authors in [161-164]. This paper uses a cost function that includes terms for the qZSI inductor current and capacitor voltage in addition to the three-phase output currents. Including inductor current in the cost function reduces the input current ripple, increases overall performance and stability of the system. In addition, a comparative simulation study of the proposed technique and the conventional PI controller (a commonly used feedback controller) has been provided.

## 5.2. Operational Principles of QZSI

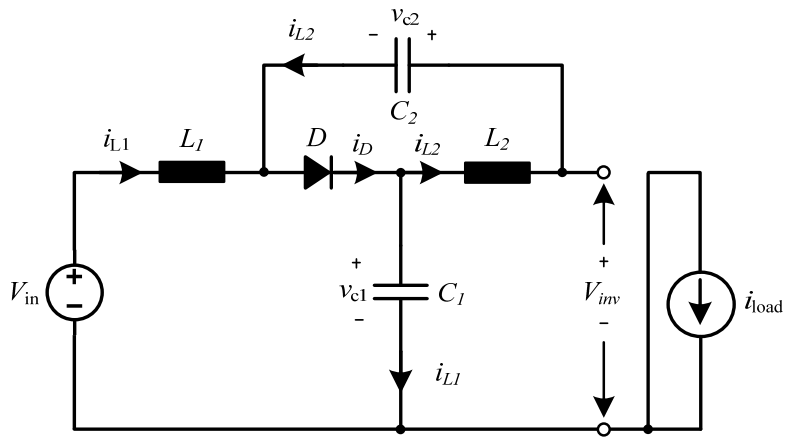
The qZSI topology was first suggested in [139] to provide continuous input current to solve the discontinuous input current problem in the original ZSI. This provides a better interface for DC sources such as fuel cells and solar cells. The qZSI operates in three different modes: active state, null state and shoot-through state, as shown in Figure 66. During the active state, shown in Figure 66(a), the inverter is controlled in the same way as a conventional voltage source inverter only without dead time. On the dc input side, during the active state the diode will turn ON and capacitor  $C_1$  will discharge through inductor  $L_2$ . In the null state, shown in Figure 66(b), all three top switches or bottom switches of the inverter are turned ON which disconnects the inverter output from the input and providing a freewheeling path for the load current. Inductor  $L_2$  current will flow through capacitor  $C_2$  and the diode. Moreover, current flowing in inductor  $L_1$  will charge capacitor  $C_1$  via the diode. Finally, the shoot-through state occurs when both high-side and low-side switches in the same phase leg are turned on simultaneously. During this state, there can be one, two, or all three phase of the inverter short circuited. The inductor  $L_2$  will connect to the capacitor  $C_1$  and the source will connect to the capacitor  $C_2$  through the inductor  $L_1$  as shown in Figure 66(c). Capacitor  $C_1$  transfers the energy to the inductor  $L_2$  and inductor  $L_1$  will be charged from the source and capacitor  $C_2$ .

## 5.3. System Modeling and Analysis

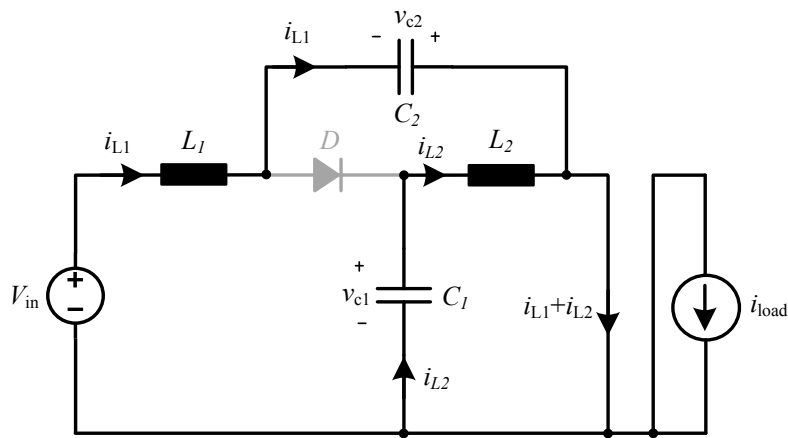
The three-phase inverter has a total of fifteen valid switch configurations. Figure 67 shows the vector diagram for two phases ( $\alpha$ ,  $\beta$ ) where the fifteen states create as six active-states vectors ( $V_1, V_2, \dots, V_6$ ), two null state vectors ( $V_0$ ), and seven shoot-through state vectors ( $V_7$ ) [163, 165-171]. An important observation is that many of these states are redundant as they produce the same output voltage vector: the null states and the shoot-through states can be simplified into one switch



(a) Active state

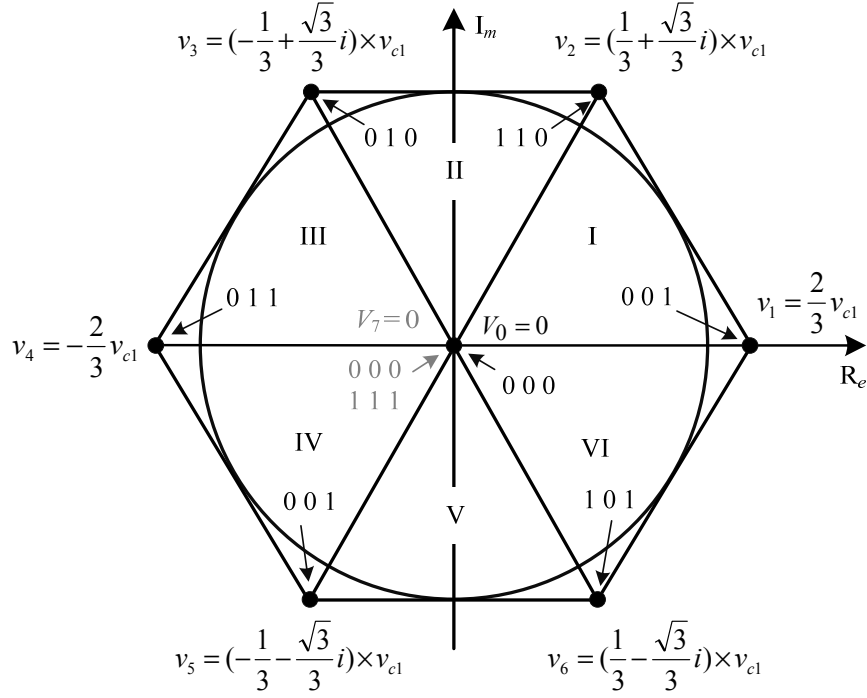


(b) Null state



(c) Shoot-through state

**Figure 66: The basic three equivalent operation modes for the qZSI**



**Figure 67: Voltage vectors for the qZSI**

configuration for each. This reduces controller computation time since less switching configurations need to be evaluated for the selection of the optimal voltage vector. The output voltages can be represented in terms of the space vector as following:

$$v_{out} = \frac{2}{3}(v_{aN} + av_{bN} + a^2v_{cN}) \quad (1)$$

where  $a = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ , and  $v_{aN}$ ,  $v_{bN}$ , and  $v_{cN}$  are the phase leg voltages as shown in Figure 65(a) [89].

Assuming that the inverter load is modelled as a resistor and inductor, shown in Figure 65 (a), the per-phase output voltage equation is:

$$v_{out} = L \frac{di_{out}}{dt} + i_{out\{\alpha, \beta\}} R \quad (2)$$

where  $L$  is the load inductance,  $i_{out}$  is the output current vector, and  $R$  is the load resistance [170].

From (2) the voltage of the inductor is determined by:

$$L \frac{di_{out}}{dt} = v_{out} - i_{out\{\alpha,\beta\}} R \quad (3)$$

In order to find the equations for quasi impedance capacitor voltage and inductor current, all three operational states of the qZSI will be considered: active, null, and shoot-through. Since the controller regulates the voltage on capacitor  $C_1$ , the current through inductor  $L_1$ , and the output current, equations are needed for these variables for the three different modes of operation.

a. Active State:

From Figure 66(a), the capacitor  $C_1$  current and the inductor  $L_1$  voltage can be expressed as follows:

$$C_1 \frac{dv_{c_1}}{dt} = i_{L_1} - i_{inv} \quad (4)$$

$$L_1 \frac{di_{L_1}}{dt} = V_{in} - i_{L_1} R_{L_1} - v_{C_1} \quad (5)$$

where  $i_{inv}$  is the input current to the three-phase inverter which is equal to  $i_{out}$  in this state (instantaneously) as shown in Figure 66(a).

b. Null State:

From Figure 66(b), the inductor  $L_1$  voltage is the same as (5) for the active state. The capacitor  $C_1$  current is given by:

$$C_1 \frac{dv_{c_1}}{dt} = i_{L_1} \quad (6)$$

c. Shoot-through State:

From Figure 66(c), the capacitor current and the inductor voltage are determined from:

$$C_1 \frac{dv_{c_1}}{dt} = -i_{L_1} \quad (7)$$



$$L_1 \frac{di_{L_1}}{dt} = v_{C_1} \quad (8)$$

Using the Euler method the control variables with sampling time  $T_s$  results in the following discrete-time model equations:

$$\left. \begin{aligned} \frac{di_{out}}{dt} &\approx \frac{i_{out}(t) - i_{out}(t - T_s)}{T_s} \\ \frac{dv_{c1}}{dt} &\approx \frac{V_{c1}(t) - V_{c1}(t - T_s)}{T_s} \\ \frac{di_{L_1}}{dt} &\approx \frac{i_{L_1}(t) - i_{L_1}(t - T_s)}{T_s} \end{aligned} \right\} \quad (9)$$

Considering the approximation in (9), the following can be found:

1) From (3), the output load current at time  $t$  is:

$$i_{out}(t)_{\{\alpha,\beta\}} = i_{out}(t - T_s)_{\{\alpha,\beta\}} + \frac{T_s}{L} [v_{out}(t) - R \times i_{out}(t)_{\{\alpha,\beta\}}] \quad (10)$$

Advancing one time-step (from  $t$  to  $t + T_s$ ) the expression for the predicted future output load current is:

$$i_{out}(t + T_s)_{\{\alpha,\beta\}} = \frac{Li_{out}(t)_{\{\alpha,\beta\}} + T_s \times v_{out}(t + T_s)}{L + RT_s} \quad (11)$$

where  $v_{out}(t + T_s)$  is the voltage space vector for the qZSI, illustrated in Figure 67, which can be selectively generated through suitable control of the switches in the circuit.

2) The expressions for the capacitor  $C_1$  voltage in each mode of operation for qZSI are:

a) *Active State*:

$$v_{c_1}(t) = v_{c_1}(t - T_s) + \frac{T_s}{C_1} (i_{L_1}(t) - i_{inv}(t)) \quad (12)$$

To obtain the future value of the capacitor voltage, (12) should shift forward one step (from  $t$  to  $t + T_s$ ).

$$v_{c_1}(t+T_s) = v_{c_1}(t) + \frac{T_s}{C_1}(i_{L_1}(t+T_s) - i_{inv}(t+T_s)) \quad (13)$$

where  $i_{inv}(t+T_s)$  is determined by the switching state  $S_1, S_2, S_3$  and the output load current.

This value can be calculated from the equation as following:

$$i_{inv}(t+T_s) = S_1 i_a(t) + S_2 i_b(t) + S_3 i_c(t) \quad (14)$$

where  $i_a(t), i_b(t)$  and  $i_c(t)$  are the instantaneous phase output current.

b) *Null State:*

$$v_{c_1}(t) = v_{c_1}(t-T_s) + \frac{T_s}{C_1} i_{L_1}(t) \quad (15)$$

In addition to that, the predictive value for capacitor voltage at null state can be expressed

by:

$$v_{c_1}(t+T_s) = v_{c_1}(t) + \frac{T_s}{C_1} i_{L_1}(t+T_s) \quad (16)$$

c) *Shoot-through State:*

$$v_{c_1}(t) = v_{c_1}(t-T_s) - \frac{T_s}{C_1} i_{L_1}(t) \quad (17)$$

The equation below describes the future value of the capacitor voltage at this state:

$$v_{c_1}(t+T_s) = v_{c_1}(t) - \frac{T_s}{C_1} i_{L_1}(t+T_s) \quad (18)$$

3) The expressions for the inductor  $L_1$  current in each mode of operation for qZSI are:

a) *Active State:*

$$i_{L_1}(t) = \frac{L_1 i_{L_1}(t-T_s) + T_s (V_{in} - v_{c_1}(t))}{L_1 + R_{L_1} T_s} \quad (19)$$

and the predictive equation for the inductor current is:

$$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s (V_{in} - v_{c_1}(t+T_s))}{L_1 + R_{L_1} T_s} \quad (20)$$

Equation (20) depends on the predictive value of the capacitor voltage. This value can be considered almost equal to the present capacitor  $C_1$  voltage because the change in capacitor voltage considerably small. Therefore, this equation can be rewritten as:

$$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s (V_{in} - v_{c_1}(t))}{L_1 + R_{L_1} T_s} \quad (21)$$

b) *Null State:*

The equation will be exactly the same as for the active state.

c) *Shoot-through State:*

$$i_{L_1}(t) = \frac{L_1 i_{L_1}(t-T_s) + T_s v_{c_1}(t)}{L_1 + R_{L_1} T_s} \quad (22)$$

For the predictive equation of the inductor current, the future capacitor voltage is presented but the change is small, so the equation can be expressed by:

$$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s v_{c_1}(t)}{L_1 + R_{L_1} T_s} \quad (23)$$

Table 6 shows summarized equations for the predictive capacitor voltage and predictive inductor current for the three states (active, null, and shoot-through state).

**Table 6: The model-predictive equations of the capacitor voltage and inductor current for the three operating states**

	Capacitor voltage $v_{c_1}(t+T_s)$	Inductor current $i_{L_1}(t+T_s)$
Active state	$v_{c_1}(t+T_s) = v_{c_1}(t) + \frac{T_s}{C_1} (i_{L_1}(t+T_s) - i_{inv}(t+T_s))$	$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s (V_{in} - v_{c_1}(t))}{L_1 + R_{L_1} T_s}$
Null state	$v_{c_1}(t+T_s) = v_{c_1}(t) + \frac{T_s}{C_1} i_{L_1}(t+T_s)$	$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s (V_{in} - v_{c_1}(t))}{L_1 + R_{L_1} T_s}$
Shoot-through state	$v_{c_1}(t+T_s) = v_{c_1}(t) - \frac{T_s}{C_1} i_{L_1}(t+T_s)$	$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s v_{c_1}(t)}{L_1 + R_{L_1} T_s}$

#### 5.4. Proposed Predictive Control for QZSI

The general MPC procedure is comprised of three steps. The first is called estimation during which variables like three-phase current, capacitor voltage and inductor current are measured. The second step is the prediction of future value of the variables which are calculated based on the present-time measurements. The third step is the optimization during which the optimal switching state is chosen to minimize the cost-function objectives. The proposed technique uses the qZSI model developed in the previous section to calculate the future behavior of the system (input current (inductor  $L_1$  current), DC capacitor  $C_1$  voltage and three-phase output current) which are summarized in Table 6. Then the control calculates the cost function which is a key factor in selecting the optimal voltage vector in each possible input. Thus the cost function should have all the parameters to be optimized within the imposed constrains. The predictive control can be achieved based on the minimization of the proposed cost function. This leads to the determination of the optimal switching state, which ensures the minimum error between the reference value and the predicted value from (11), (13), (16), (18), (21) and (23).

The MPC cost function used in this chapter is comprised of three weighted cost functions representing the ac output current, capacitor  $C_1$  voltage, and inductor  $L_1$  current. The output current cost function is defined as

$$g_i = \left| i_{\alpha}^*(t+T_s) - i_{\alpha}(t+T_s) \right| + \left| i_{\beta}^*(t+T_s) - i_{\beta}(t+T_s) \right| \quad (24)$$

where  $i_{\alpha}^*(t+T_s), i_{\beta}^*(t+T_s)$  are the real and imaginary parts of the future reference output current, and  $i_{\alpha}(t+T_s), i_{\beta}(t+T_s)$  are the real and imaginary components of the predicted load current. Furthermore the cost function of the capacitor  $C_1$  voltage is defined as

$$g_v = \left| v_{C_1}^*(t+T_s) - v_{C_1}(t+T_s) \right| \quad (25)$$

where  $v_{c1}^*(t+T_s), v_{c1}(t+T_s)$  are the reference and predicted capacitor  $C_1$  voltage. Lastly, the cost function of the inductor  $L_1$  current is defined as

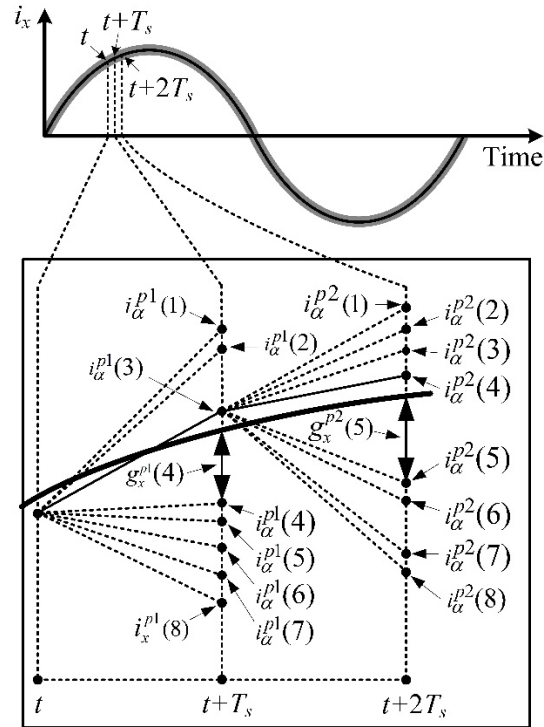
$$g_{i_L} = |i_L^*(t+T_s) - i_L(t+T_s)| \quad (26)$$

where  $i_{L1}^*(t+T_s), i_{L1}(t+T_s)$  are the reference and predicted inductor current, respectively. The complete cost function incorporates (24), (25), (26) into to one function

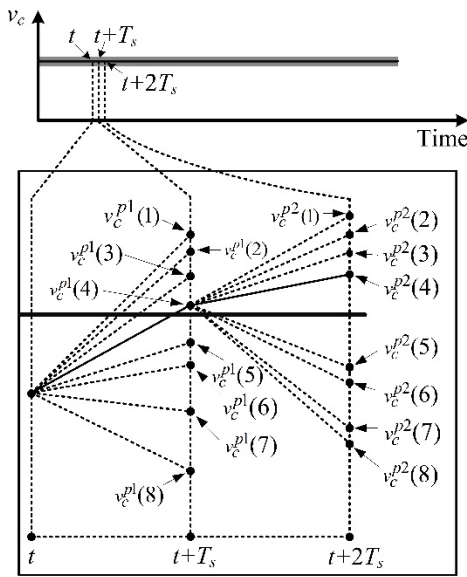
$$g = \lambda_i g_i + \lambda_{v_c} g_{v_c} + \lambda_{i_L} g_{i_L} \quad (27)$$

where  $\lambda_i, \lambda_{v_c}, \lambda_{i_L}$  are the weighting factors for output current and the quasi-Z-sourced capacitor  $C_1$  voltage and inductor  $L_1$  current, respectively. The values of the weighting factor may be selected through heuristic methods since there is no known rigorous mathematical technique for weight factor optimization.

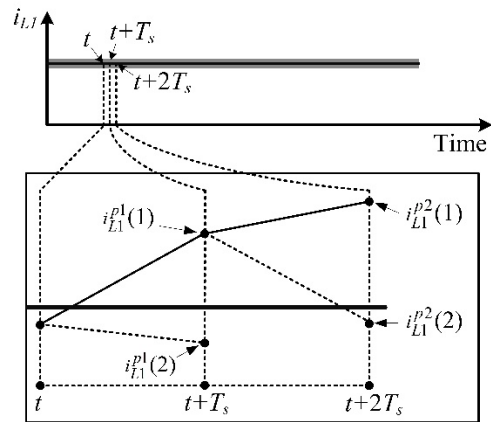
To elaborate on the proposed MPC method, Figure 68 shows the strategy of the predictive control for the AC phase output current, capacitor  $C_1$  voltage and inductor  $L_1$  current. The output load current was converted from three phases (A,B,C) to two phases ( $\alpha, \beta$ ) reference frame then two successive points from this signal were taken. In Figure 68 (a), assuming  $i_x$  is  $i_\alpha$ , from the beginning of the sampling time  $t$ , eight predictive states for the real part of the AC output current ( $i_\alpha^{p1}(1) \dots i_\alpha^{p1}(8)$ ) have been calculated from (11). The numerical difference between any calculated future state and the reference is used to develop the cost function with unity weighting factor ( $g_x^p$ ) where  $x$  is the real component ( $\alpha$ ) or imaginary component ( $\beta$ ) and “p” refer to a prediction. As shown in Figure 68 (a), the optimal calculated future-state of the current which is the nearest point to the reference and minimizes the cost function is  $i_\alpha^{p1}(3)$ . This point can be found from the first term in (24). Thus, the selector will choose this state as an optimal state for the real part of the



(a) Output current

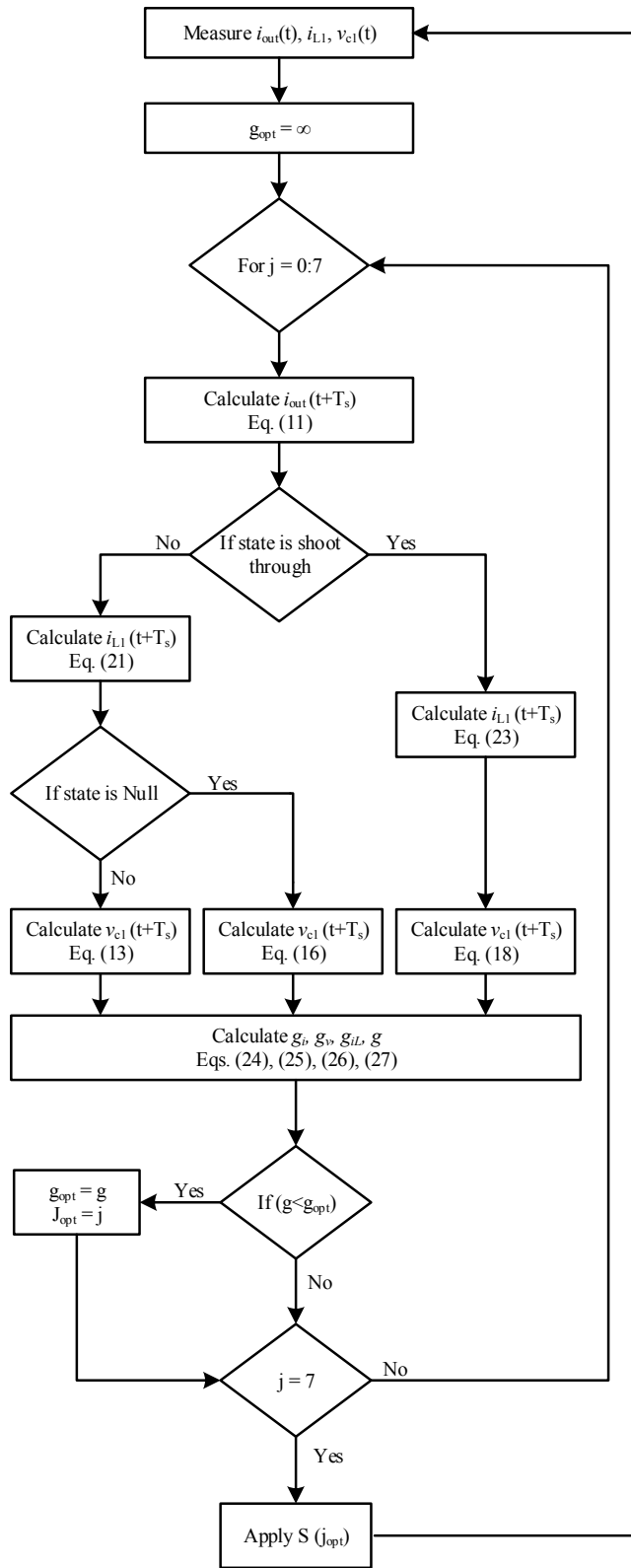


(b) Capacitor voltage



(c) Inductor current.

**Figure 68: Illustration of the MPC method predicting the modelled for one-step and two-steps into the future**



**Figure 69: Flow chart of the MPC for the qZSI**

**Table 7: qZSI Simulation System Parameters**

Parameter	Value
Input DC voltage	50 V
qZSI Inductance	500 $\mu$ H
qZSI Capacitance	470 $\mu$ F
Load inductance	15 mH
Load Resistance	10 $\Omega$
Sample time $T_s$	30 $\mu$ S

**Table 8: PI controller parameters**

Loop type	Parameter	Value
Capacitor voltage loop	$K_p$	0.3
	$K_i$	50
Inductor current loop	$K_p$	1.6
	$K_i$	5
Output current loop	$K_p$	10
	$K_i$	2

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \quad (28)$$

output current. Regarding to the imaginary part ( $i_\beta$ ), it will be calculated also from (11) and the steps will be same like real part ( $i_\alpha$ ). In the other hand, Figure 68 (b) shows the prediction points for the capacitor  $C_1$  voltage which can be calculated from (13), (16), and (18). Through the cost function (25), the optimizer can find the optimal value at  $t+T_s$  which is  $v_c^{p1}(4)$  that is the nearest point to the reference. For the future inductor  $L_1$  current there are only two prediction values which can be calculated from (21), and (23) as shown in Figure 68 (c) (one in active state and one in shoot-through state). The optimal point for the future inductor current is  $i_t^{p1}(2)$  which is minimizing the error. After that, the optimizer will choose the overall optimal state according to (27). Depending



on this selection, the proper switching state will be chosen. Similarly, from  $t + T_s$  to  $t + 2T_s$ , the controller will calculate the future points for the variables and the optimizer will choose the optimal points which is the nearest point to the reference.

The selection process of the optimal switching states in each sampling period is presented in Figure 69. The first step is measuring variables such as three-phase output current, capacitor  $C_1$  voltage and inductor  $L_1$  current. The algorithm transforms the three-phase output current to  $\alpha\beta$  coordination according to Clarke transformation which is in (28). Then the algorithm calculates the predicted output current which is verified in (11). The algorithm is initialized by setting the optimal cost function ( $g_{opt}$ ) to  $\infty$  and then the algorithm enters the loop. The predictive value for the inductor current and capacitor voltage are calculated in all states and for all vectors by the help of the equations mentioned above. The controller starts the optimization by calculating the cost function by using (27). Thus, the selector chooses the optimal switching state (as demonstrated in Figure 68) which give the smallest value of the cost function.

## 5.5. Simulation Results

To verify the proposed control idea, a MATLAB/Simulink program has been used to simulate the full system composed of three-phase qZSI controlled by model predictive control, and three-phase  $RL$  load. A comparison between the proposed MPC and the classical PI controller method (as in [172, 173]) is carried out to assess the performance. Table 7 lists the parameters of the system used in the simulation and experiment. The design equations, used to choose the values of the circuit parameters for the qZSI converter, are from [172]. The value of the parameters for the PI controller, which is used in the simulation, is shown in Table 8. The PWM carrier frequency

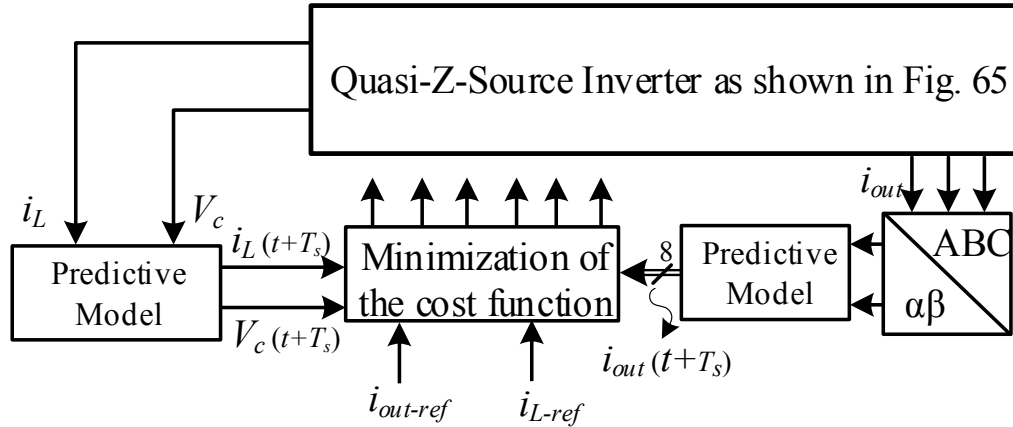
for the conventional PI controller is 10 kHz, whereas the maximum switching frequency of the predictive control is 16 kHz which can be calculated as following:

$$f_{sw,av} = \frac{\sum_0^z \frac{f_{sw,A} + f_{sw,B} + f_{sw,C}}{3}}{z} \quad (29)$$

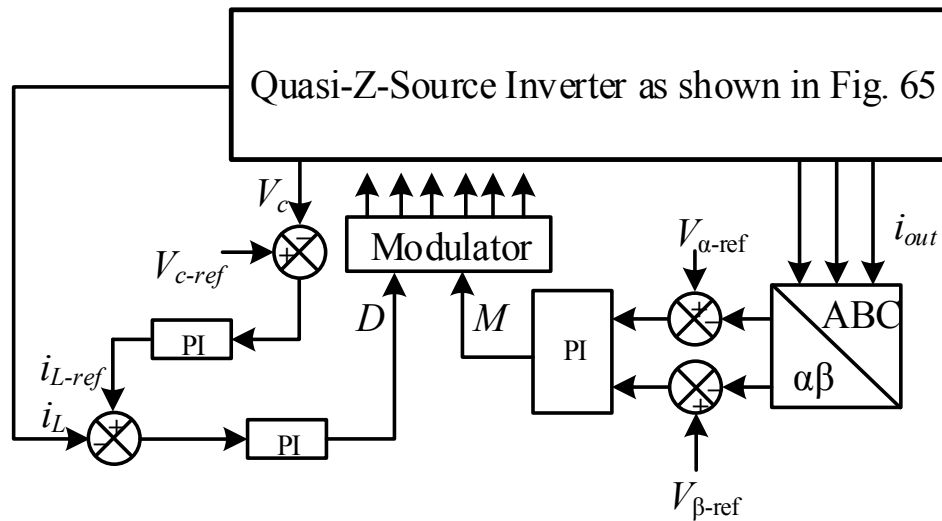
where  $f_{sw,A}$ ,  $f_{sw,B}$ , and  $f_{sw,C}$  are the switching frequencies for the three inverter's legs which are calculated by measuring the number of switching changes in the gating signals. "z" is the number of fundamental cycles which is four in this chapter.

The structure of the MPC controller differs from the PI controller since there is no modulator and no linear controller. Thus, it is easier to design since there is no parameters for the linear controller that must be tuned. The control strategy is evaluated considering the cost function indicated in (27) and with a weighting factor identified using trial and error method as  $\lambda_i=1$ ,  $\lambda_{vc}=0.9$ , and  $\lambda_{iL}=4.6$ .

Figure 70 and Figure 71 show the block diagram of the predictive control algorithm and the traditional PI controller for qZSI respectively. Both controllers are sensing the input current (inductor ( $L_1$ )), the DC capacitor ( $C_1$ ) voltage and the three-phase output current and use them as a feedback. In addition, Figure 72 and Figure 73, show the three-phase load current, input current, DC-link voltage, and harmonic spectrum for the output current for the proposed predictive control, and for the conventional PI controller, respectively, with a step change in the reference output current from 2.1A to 1.35A at instant  $t=200$ ms.



**Figure 70: Block diagram of the predictive control algorithm for qZSI**



**Figure 71: Block diagram of the traditional PI controller for qZSI**

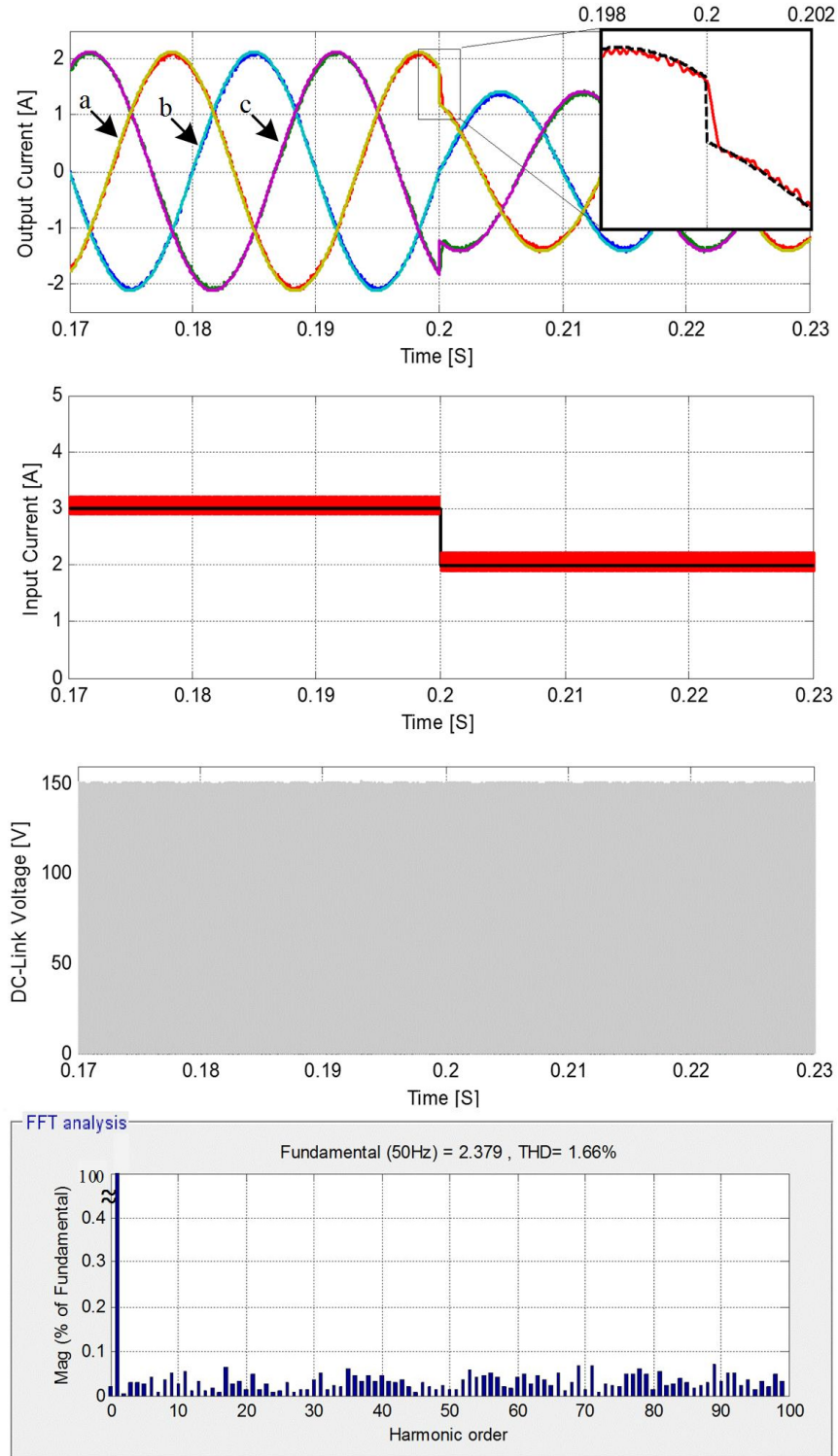
It can be observed that the three-phase output current tracks the sinusoidal references in both cases. However, the proposed predictive controller offers better tracking quality (lower output current ripples and lower DC input current ripples as shown in the middle of Figure 72 and Figure 73). Notice that as mentioned before there are three switching states, so the reason for the increased ripple from the PI controller than the MPC is not because of different switching frequencies but because of the shoot-through state, which effects the output current ripple. MPC chooses the optimal state for the qZSI. In practice, this results has lower ripple at the same effective switching

frequency. This, along with not needing to tune controller parameters, are the main advantages of the MPC over the PI controller for qZSI. In addition, the current THD for the proposed controller is around 1.66%, when it is around 2.33% for the PI controller as shown in the bottom of Figure 72 and Figure 73. Because of the variable switching frequency, a high-quality output current has been produced with lower THD.

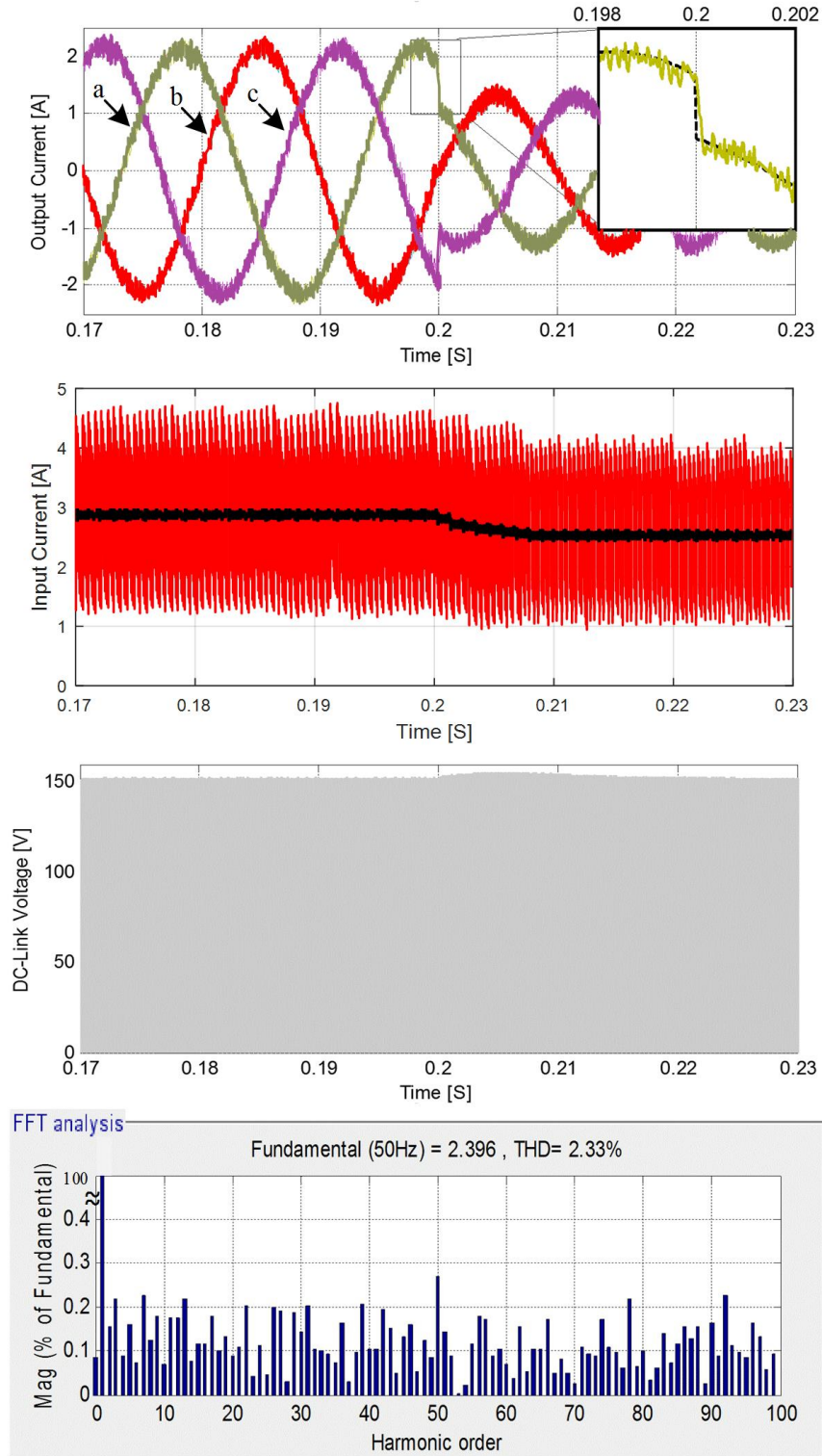
Furthermore, the calculated reference inductor current for the proposed controller is founded from  $i_{L\_ref} = P_{out}/V_{in}$ . This method of calculation is very straightforward, simple, and does not need a long time to calculate the value. However, for the conventional controller, the DC input current is computed according to the inner current loop, which depends on the measured capacitor voltage [173], [174]. This is the reason why the reference input current in the proposed technique changes instantaneously and faster than the conventional PI controller. As shown in the bottom part of Figure 72 and Figure 73, the DC-link voltage for the proposed controller is constant and switched with a step change but there is a slightly change for the conventional techniques.

Figure 74 shows the trade-off between the switching frequency and the THD. This figure shows the superiority of the MPC over the PI controller for low switching frequencies. However, increasing the switching frequency leads to decrease THD in both controller but the reduction in PI controller is much better than MPC. As it is shown, the THD for PI controller becomes less than the MPC at 30 kHz switching frequency or larger.

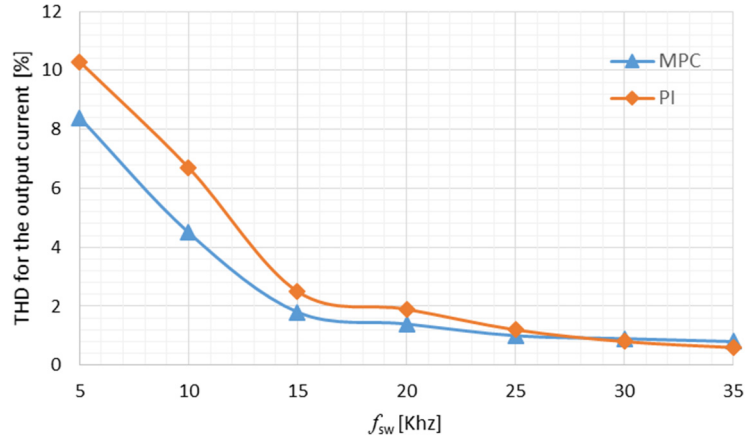
Figure 75 shows the phase load voltage for the predictive control, which is three-level and there is no change with a step change. In addition, Figure 76 shows the quality of the control if there is a load model error by applying a step change in the inductor and resistor of the load from  $L=15$  mH,  $R=10$   $\Omega$  to  $L=7.5$  mH,  $R=5$   $\Omega$  at 200 mS. As shown, the load current is still sinusoidal but the ripple is increased slightly.



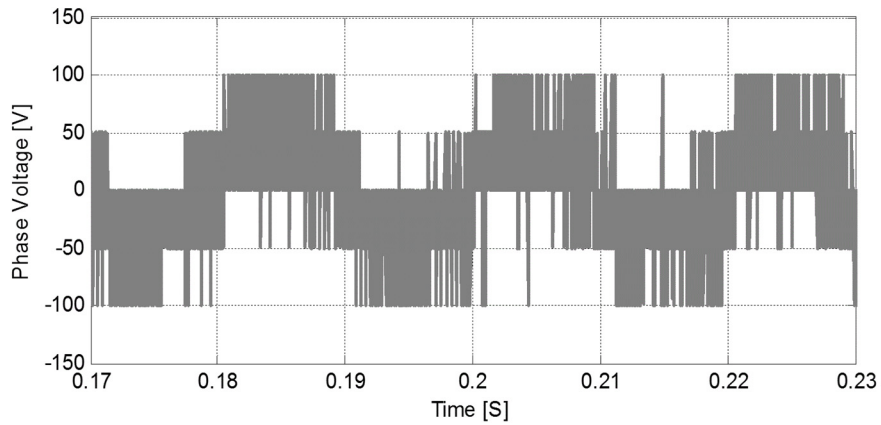
**Figure 72: Proposed MPC controller for a step change in the reference output current at instance 200mS; from the top, three-phase output current, input current, DC-link voltage, and harmonic spectrum for the output current**



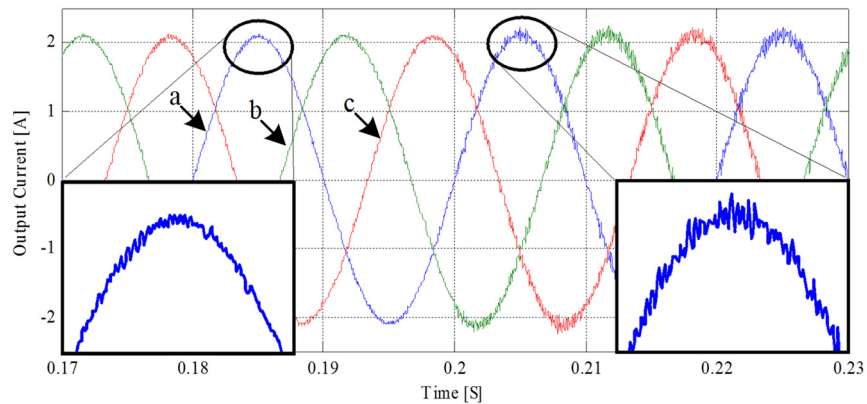
**Figure 73: Conventional PI controller for a step change in the reference output current at instance 200mS; from the top, three-phase output current, input current, DC-link voltage, and harmonic spectrum for the output current**



**Figure 74: The THD of the three-phase output current for the proposed MPC and PI controller**



**Figure 75: Simulation results for the load voltage van with a step change in the reference output current at instance 200ms**



**Figure 76: Simulation results for the effect of the load model error with 50% change reduction in the load inductance and load resistance at instance 200ms**

## 5.6. Experimental Results

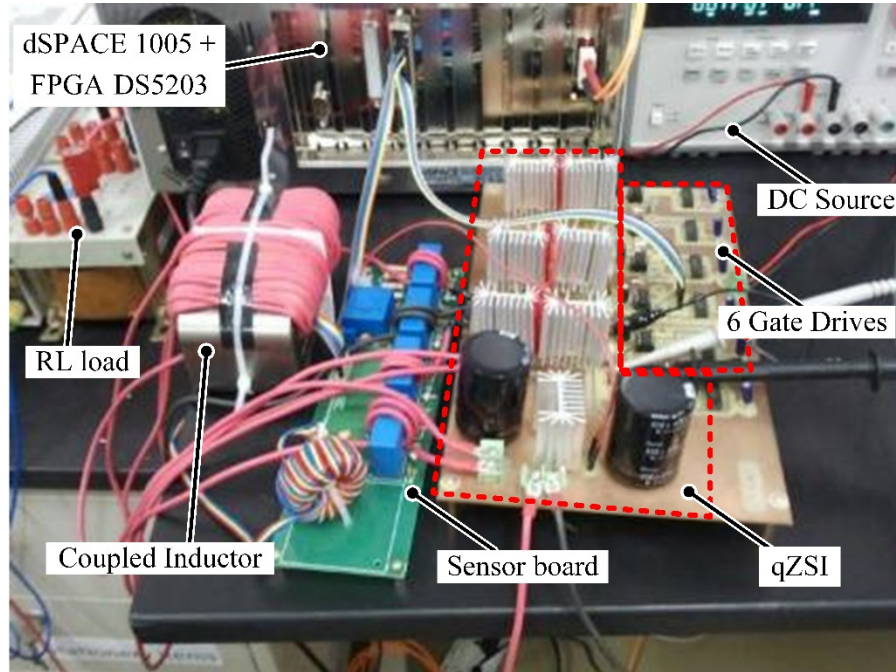
To further validate the concept, an experimental prototype of the qZSI, shown in Figure 77, was built. A dSPACE DS1005 and FPGA DS5203 (Xilinx Virtex<sup>®</sup>5) were used to implement the proposed control. The experimental parameters are shown in Table 7. In the qZSI, two capacitors are EPCOS-B43501A9477M 470 $\mu$ F-400V aluminum electrolytic and the two inductors are built together on one core (AMCC 250 Metglas UU) on common mode to minimize the size and the weight of the inductors [175]. In addition, GA35XCP12-247 IGBT/SiC-diode was used in the three-phase inverter.

In dSPACE, the execution steps of this technique calculate the control action in each sampling period. Figure 78 shows the schematic of the proposed technique applied to the qZSI. As shown in Figure 78, three-phase output current, capacitor voltage and input current were measured and sent to the dSPACE. By using ADC inside the controller, the analog signal is converted to digital form. In the FPGA board, the three-phase current was converted to two phase then to complex equation. Moreover, by using the voltage states mentioned in Figure 67, eight output voltage values can be calculated then sent to the optimizer.

The controller calculates the output power considering the load impedance. In this chapter, a three-phase AC output reference current is 1.9 A and the reference inductor current is 3.0 A. Measured signals are sent to the dSPACE card through the peripheral high-speed bus (PHS). Eight space vector modulation (SVM) signals are generated inside the dSPACE by the help of the capacitor reference voltage (average DC link voltage = capacitor voltage). These signals are supplied to the optimizer, which in turn generates eight vectors and send them to the selector as shown in Figure 78. The selector applies the first element of the optimal control sequence with cost function as smallest one. At the end, the whole procedure is repeated at the next time step.



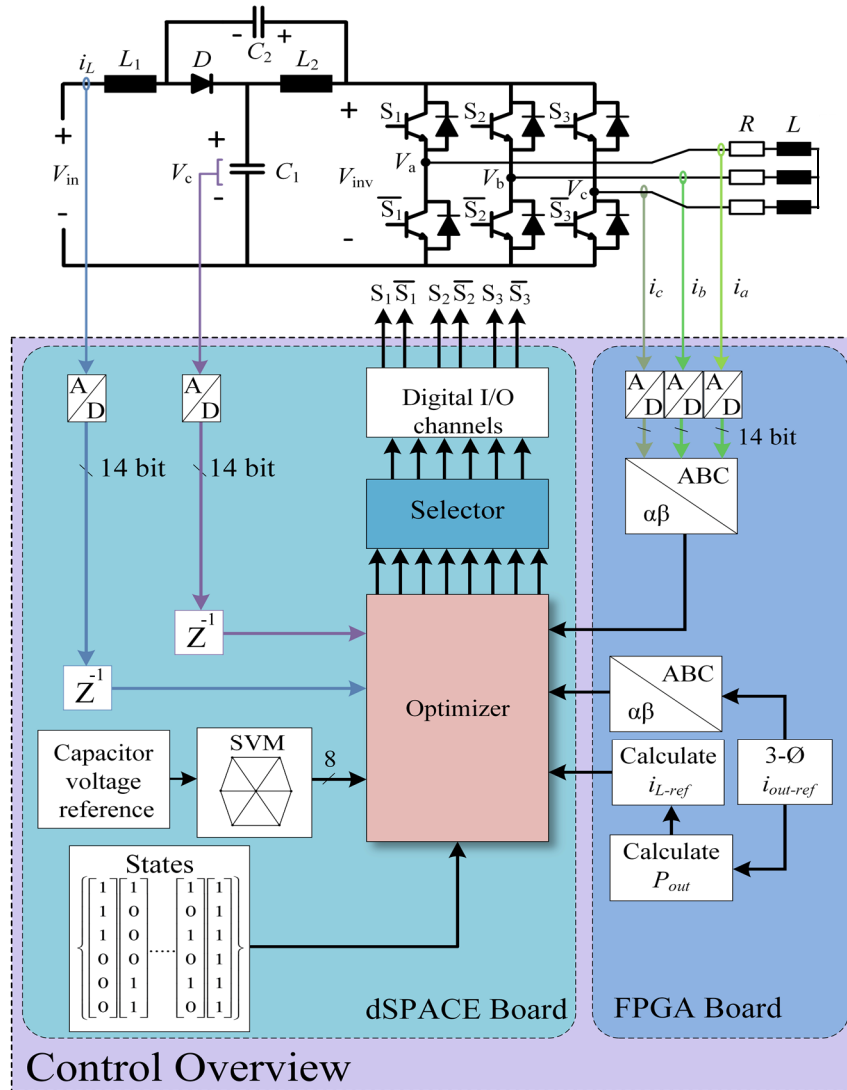
Figure 79(a) shows the predictive model of the output current where it converts the three phase output current to  $\alpha\beta$  vectors, then the prediction of the output current can be calculated.



**Figure 77: The prototype of the qZSI inverter**

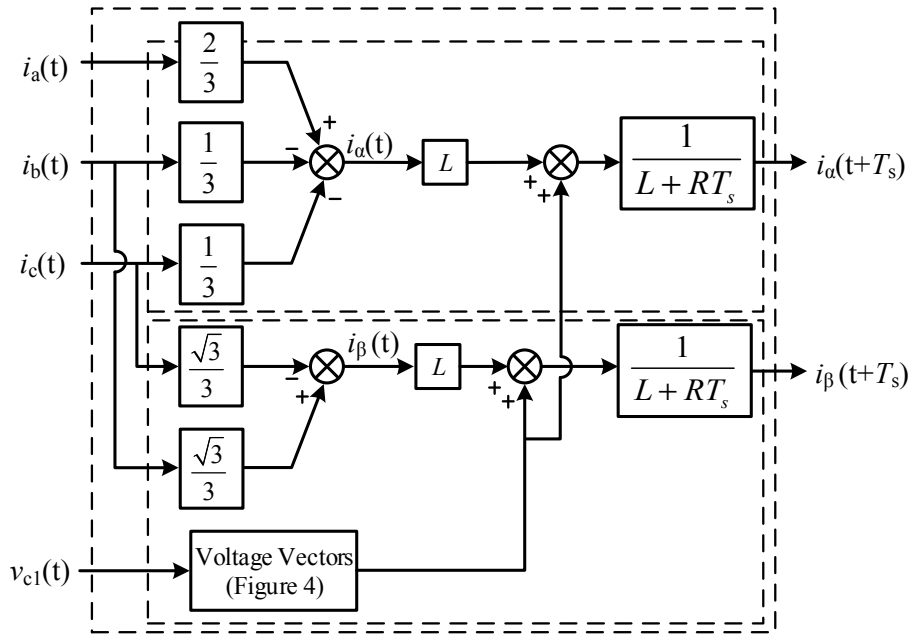
Moreover, Figure 79(b)-(d) show the predictive model for the capacitor voltage and inductor current in the active, null and shoot-through states respectively. These models are depending on (13), (14) and (21) for active state, (16) and (21) for null state, and (18) and (23) for shoot-through state.

Figure 80 shows that the three-phase output currents are sinusoidal and the peak is 1.9 A. In the setup, the input voltage is equal to 50 V, the reference capacitor voltage is equal to 100 V, and the DC-link voltage are shown in Figure 81. In the shoot-through state, the DC-link voltage becomes zero and the inductor stores the energy in this period so the current will increase in this state, as shown in Figure 82. In the normal states, the boosted voltage appears at the DC-link and the inductor current decreases as stored energy is discharged.

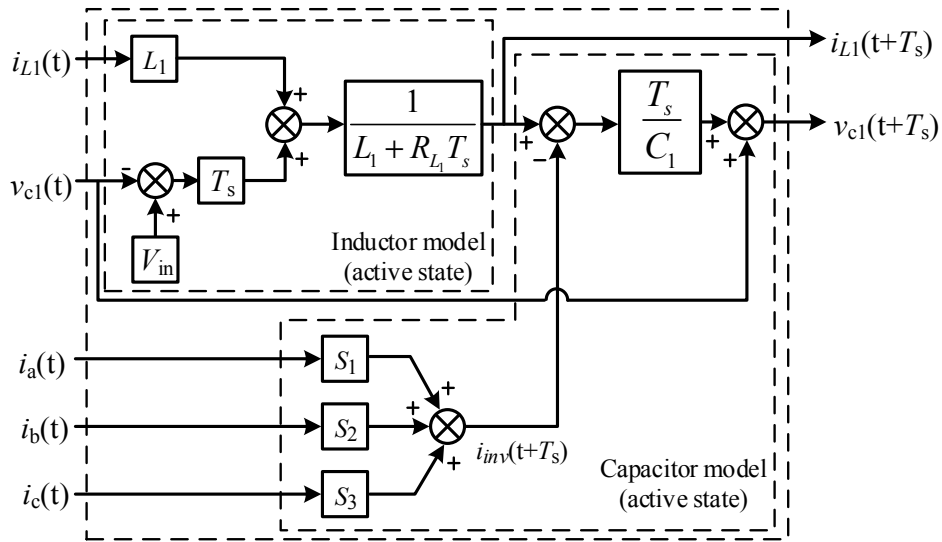


**Figure 78: Proposed MPC block diagram for the qZSI**

To show the excellent tracking capability of the proposed technique, another value of the reference capacitor voltage has been used to be 150V and the reference output current has a step change from 2.7 A to 1.9 A, the output changed from 2.7 A to 1.9 A as shown in Figure 83. It is evident that the control ensures high dynamic response with a step change in the reference output current.

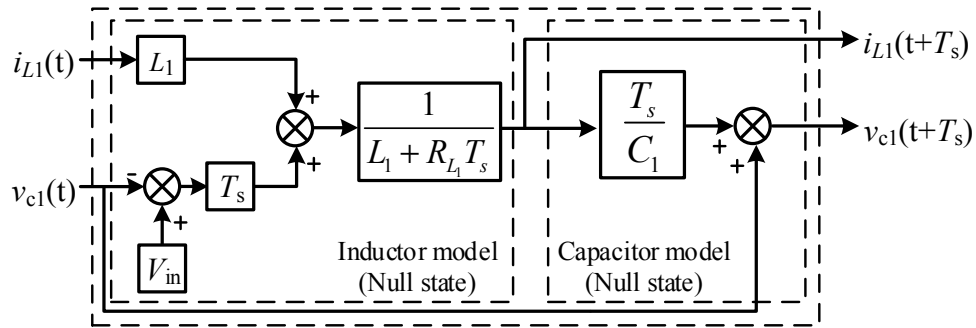


(a) Predictive model for the output current

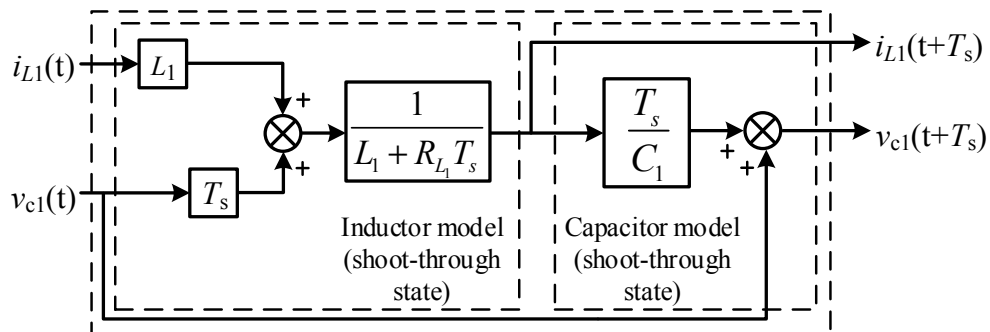


(b) Predictive model for the capacitor voltage and inductor current in active state

**Figure 79: The predictive model for the (a) output current, capacitor voltage and inductor current in (b) active state, (c) null state, and (d) shoot-through state**

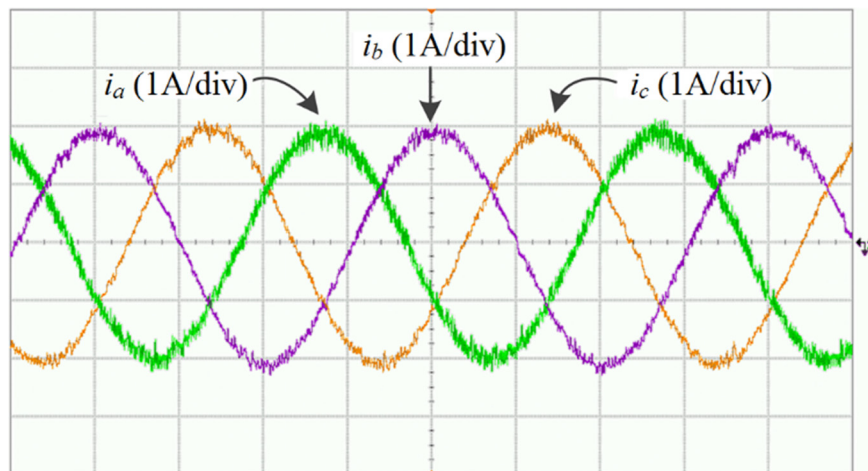


(c) Predictive model for the capacitor voltage and inductor current in null state



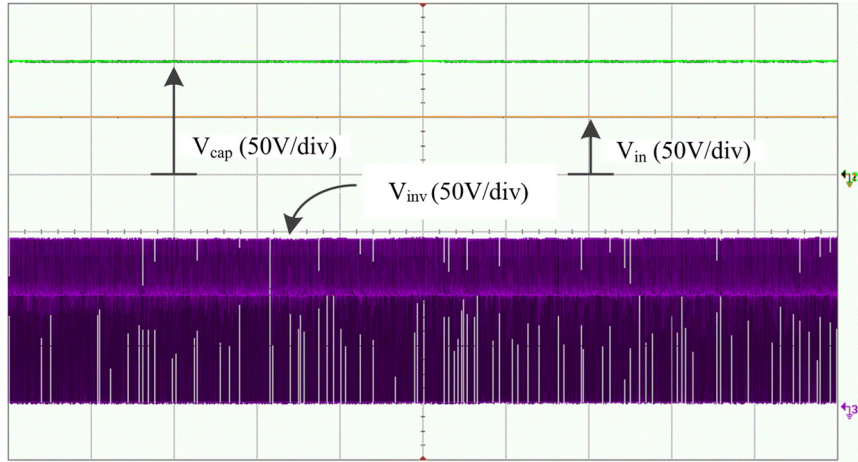
(d) Predictive model for the capacitor voltage and inductor current in shoot-through state

**Figure 79: Continued**

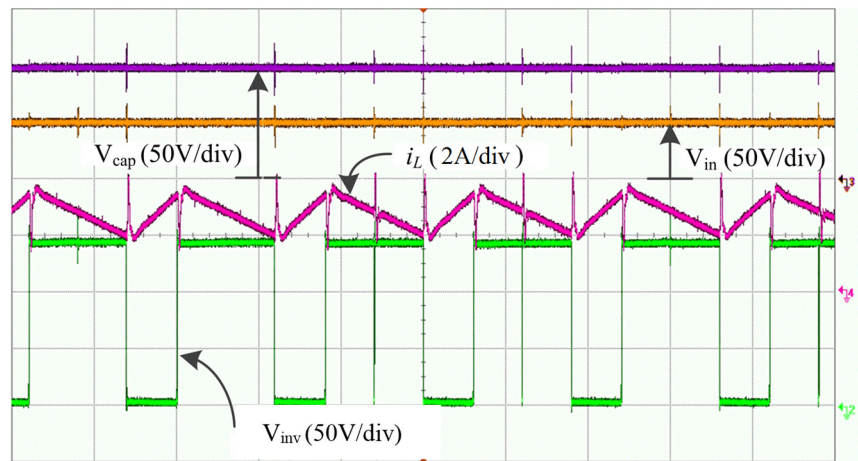


**Figure 80: Three-phase AC output current**

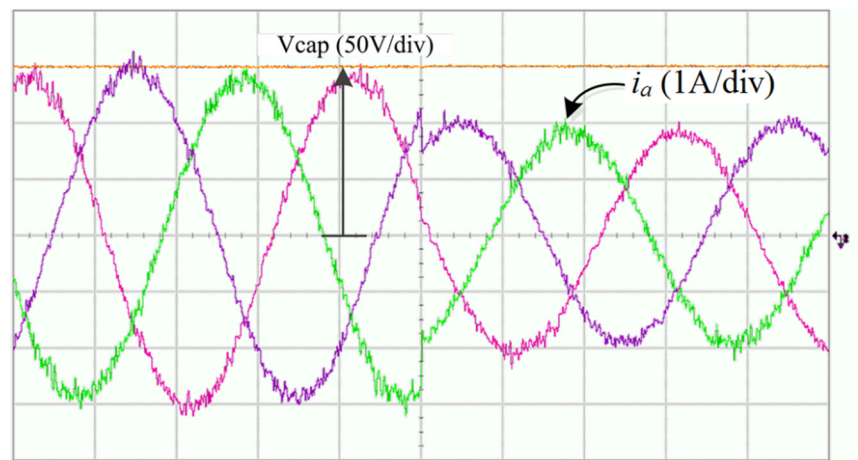
Finally, the harmonic content of the output current at  $T_s = 30 \mu\text{s}$  is presented in Figure 84, which indicates 1.7% THD for 2.3 A fundamental output current. It is confirmed that the presence of fifth and seventh harmonics have little impact on the quality of the output current.



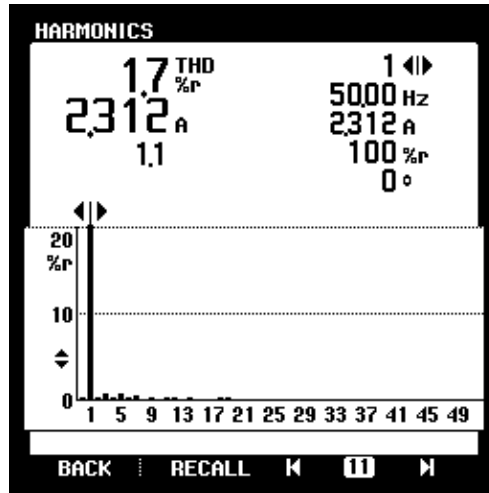
**Figure 81: Input voltage, Capacitor voltage and DC-link voltage**



**Figure 82: Input voltage, input current, capacitor voltage and DC-link voltage**



**Figure 83: Output current and capacitor voltage for a step-change in the reference output current**



**Figure 84: Steady state output current spectrum at 2.3A. The x-axis is harmonic number and the y-axis is percent of fundamental component of the current**

## 5.7. Conclusion

This chapter proposes a model predictive control (MPC) approach for the qZSI. The main aim of this work was to achieve high dynamic performance by controlling the input current (inductor current), the DC capacitor voltage, and three-phase output current. A further aim was to reduce the switching losses, which are generated in the conventional controller due to the modulator. In addition, the proposed control guarantee the stability of the circuit by controlling the DC inductor current and the DC capacitor voltage. A discrete-time model for the qZSI and the implementation of the multi-objective control strategy have been explained in details. Moreover, a comparison between the proposed MPC and the conventional PI controller has been shown.

The results show that this method can ensure constant average capacitor voltage, regulated inductor current, and sinusoidal AC load current better than the conventional PI controller and without the need for tuning control parameters. Moreover, the robustness of the proposed controller to produce low THD in the output current has been demonstrated even when considering error in the load model. Finally, the conducted experimental verification using dSPACE DS1005

and FPGA Xilinx Virtex<sup>®</sup>5 was consistent with simulation results and proved the proposed concept.

## 6. FPGA-BASED PARALLEL PROCESSING OF MPC FOR QZS SIC INVERTER\*

This chapter proposes a novel implementation of a field-programmable gate array (FPGA)-based model predictive control (MPC) for a quasi-z-source inverter (qZSI). To speed-up computations, to satisfy the control requirements, and be able to increase the switching frequency, an MPC algorithm is designed for parallel processing. The parallel-processed implementation targets at short computation time and high accuracy as well. This is suitable for high-sampling/switching frequency operation that enables the use of MPC in fast switching systems such as SiC and GaN based converters. Many innovative digital implementation ideas can be designed, tested, and implemented inside an FPGA-based controller. Thanks to the increasing performance and parallel processing capability of FPGA technology, the implementation of the MPC on SiC based inverter was possible. A theoretical framework for the employed MPC algorithm is provided. Moreover, proposed concepts are simulated in MATLAB Simulink environment and are experimentally validated using a three-phase SiC-based qZSI. Furthermore, the results are compared to a number of close previously-published implementations of other MPC algorithms and a discussion is conducted. Simulation and experimental results show that the use of the proposed FPGA-based controller significantly accelerates the computation process and shorten the calculation time, comparing to that of conventional sequential implementations. As a result, it effectively improves the overall converter's performance to ensure a constant average capacitor voltage, a continuous inductor current, and a smooth sinusoidal load current as well.

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\* Portions of this chapter have been previously published in M. Mosa, G. M. Dousoky, H. Abu-Rub "A Novel FPGA Implementation of a Model Predictive Controller for SiC-Based Quasi-Z-Source Inverters" in IEEE Applied Power Electronics Conference (APEC), pp. 1293-1298, Mar. 2014, © 2014 IEEE.

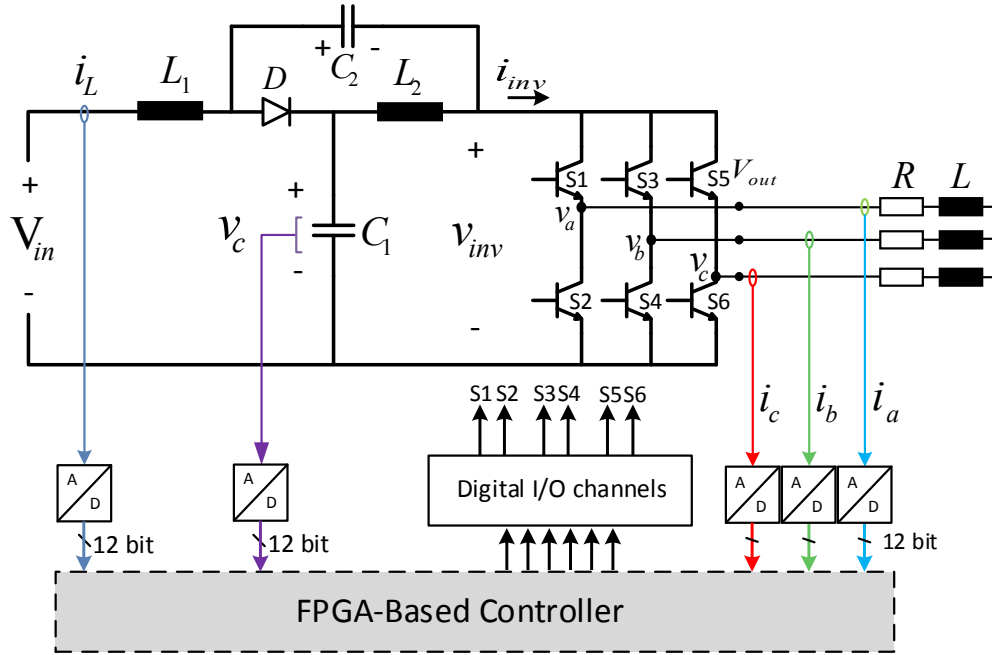


## 6.1. Introduction

Wide-gap semiconductors such as SiC and GaN are very promising materials for high-efficiency switching devices, because of their high breakdown voltage, high switching speed and low on-state resistance [176-178]. Such switches provide an excellent performance and can afford rapid switching at low switching losses; which in turn motivates both industry and academia to do much effort in developing fast controllers to gain the benefits of such promising technology [179, 180], namely, high dynamic performance, low filtering burdens and, therefore, high power density of switching power converters [133].

Model predictive controller (MPC) has emerged as a powerful method for the control of electrical energy [21, 156, 180]. It is very intuitive and makes it easy to apply nonlinearity and constraints [19, 181, 182]. However, a drawback of MPCs is the small sample time required to obtain a proper performance of power converters. In each sampling time, a complicated algorithm chooses the optimum state that should be applied in the next one [183].

Traditionally, the implementation of MPCs has been accomplished using digital sequential processors; where the processes are calculated in a chronological order [21, 184, 185]. On the other hand, to accelerate the computation of MPC and to fulfill most of such control requirements, few publications reported the possibility of parallel computing of MPC algorithms for industrial applications [186-188]. The parallel processing capability of FPGAs, along with its substantial improvements in price and performance, has made the application of many sophisticated control algorithms possible in power electronics field [189-191]. This chapter contribution lies in parallel processing of an MPC algorithm and its innovative implementation using FPGA, as described in Figure 85.



**Figure 85: An FPGA-based control scheme of a Quasi-Z-Source inverter**

A theoretical framework for the employed MPC algorithm has been provided. Moreover, the implementation work has been expanded and addressed more thoroughly in [163]. Furthermore, the literature review has been updated, and the most recent references have been included. In addition to that, the proposed controller's operation has been clarified with new illustrative figures and evaluated by a comparative investigation.

## 6.2. MPC Algorithm for QZSI

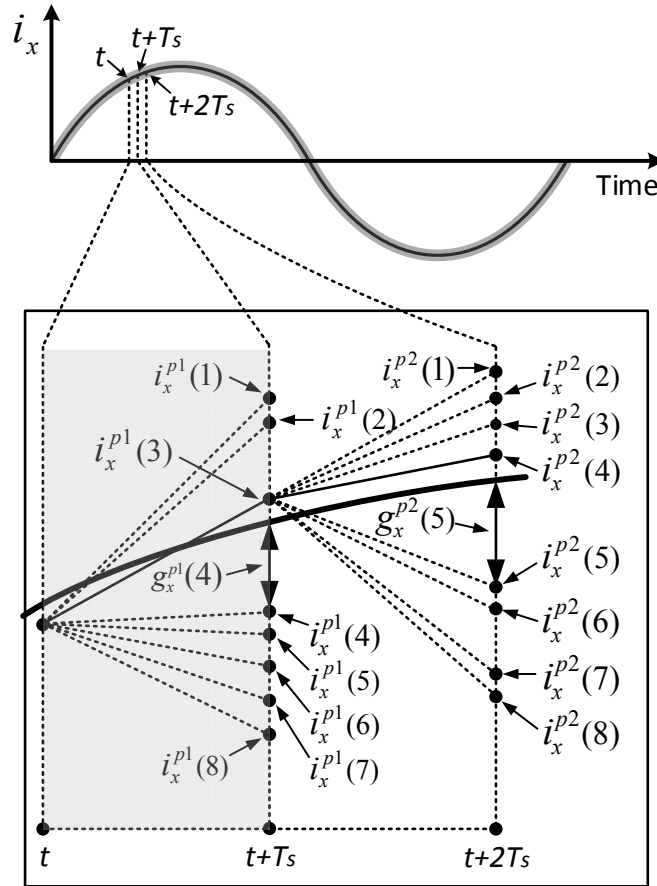
The model of the qZSI is explained in detail in [161]. Moreover, the employed MPC algorithm operation along with its mathematical framework and conventional implementation are briefly described in this section.

### 6.2.1. Algorithm Brief Description

The controller generates the reference inductor current and the reference output currents that fulfill the reference power and the reference capacitor voltage. Furthermore, inductor current,

capacitor voltage and output currents are measured and are processed through the control algorithm, as shown in Figure 85.

Figure 86 shows a locus diagram for prediction and observation of a current ( $i_x$ ). The optimizer identifies the state at which the predicted quantity is located closest to its future reference.



**Figure 86: Locus diagram for prediction and observation of current  $i_x$**

In other words, to move from instant  $t$  to instant  $t+T_s$ , eight future loci exist for the current ( $i_x^{p1}(1) \dots i_x^{p1}(8)$ ), the distance between any locus and the reference is called cost function ( $g_x^{p1}$ ). As shown in Figure 86, the nearest point to the reference is  $i_x^{p1}(3)$ , therefore, the optimizer chooses this case/state as the optimal one. According to this methodology, the proper switching state is applied.

Similarly, to move from instant  $t+T_s$  to instant  $t+2T_s$ , eight future loci exist for the current  $(i_x^{p2}(1)\dots i_x^{p2}(8))$ , the distance between any locus and the reference is  $g_x^{p2}$ , and the optimal point is  $i_x^{p2}(4)$  as shown in Figure 86.

### 6.2.2. Mathematical Framework

Recalling equations from the previous chapter, in qZSI, two states exist: active state and shoot through state. The discrete inductor current and capacitor voltage can be calculated as follows:

i.in active state:

$$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s (V_{in} - V_{c_1}(t))}{L_1 + R_{L_1} T_s} \quad (1)$$

$$V_{c_1}(t+T_s) = V_{c_1}(t) + \frac{T_s}{C_1} (i_{L_1}(t+T_s) - i_{inv}(t+T_s)) \quad (2)$$

ii.in shoot through state:

$$i_{L_1}(t+T_s) = \frac{L_1 i_{L_1}(t) + T_s V_{c_1}(t)}{L_1 + R_{L_1} T_s} \quad (3)$$

$$V_{c_1}(t+T_s) = V_{c_1}(t) - \frac{T_s}{C_1} i_{L_1}(t+T_s) \quad (4)$$

Moreover, the future output current is obtained by:

$$i_{out}(t+T_s) = \frac{L i_{out}(t) + T_s \times V_{out}(t+T_s)}{L + R T_s} \quad (5)$$

where  $L$ ,  $R$  are the load inductance and load resistance,  $i_{out}$  is the output current that flows to the load, and  $V_{out}$  is the inverter output voltage.

The employed cost function includes prediction of the inductor current, capacitor voltage and three phase output current [163] and [159, 192, 193], as follows:

$$g = \left( \left| i_{\alpha\_out}^*(t+T_s) - i_{\alpha\_out}(t+T_s) \right| + \left| i_{\beta\_out}^*(t+T_s) - i_{\beta\_out}(t+T_s) \right| \right) + \lambda_{v_c} \left| v_{c1}^*(t+T_s) - v_{c1}(t+T_s) \right| + \lambda_{i_L} \left| i_{L1}^*(t+T_s) - i_{L1}(t+T_s) \right| \quad (6)$$

where (respectively);  $i_{\alpha\_out}^*(t+T_s), i_{\beta\_out}^*(t+T_s)$  is the real and imaginary components of the reference output current.  $i_{\alpha\_out}(t+T_s), i_{\beta\_out}(t+T_s)$  is the real and imaginary components of the predicted output current.  $v_{c1}^*(t+T_s), i_{L1}^*(t+T_s)$  is the reference capacitor voltage and inductor current.  $\lambda_{v_c}, \lambda_{i_L}$  is the weighting factor of capacitor voltage and inductor current.

Cost function is calculated at all the eight possible switching states and their values are compared to identify the switching state of interest; at which the cost function is minimum. Then, the picked switching state is applied to the power switches, and so forth.

### 6.2.3. Conventional Sequential Processing

To implement the MPC algorithm, explained in the previous section, Microcontrollers and Digital Signal Processors (DSP) are traditional. However, a main drawback of such conventional methods is their sequential nature; where the MPC algorithm is computed in a consecutive way; which takes long time. Accordingly, the sample time has to be longer than desired, even when using a high speed computing clock in GHz; which entirely limits the switching frequency and produces a noticeable ripple in the load current.

The computation and processing of the MPC algorithm every sampling period is sequentially achieved in the following methodology, referring to Figure 86:

1. Three phase output currents, inductor current, and capacitor voltage are measured at instance  $t$ .
2. The reference inductor current is calculated.
3. Calculate  $\alpha$  component of the measured three phase load currents

4. Calculate  $\beta$  component of the measured three phase load currents
5. The reference output currents are calculated.
6. Calculate  $\alpha$  component of the reference three phase load currents
7. Calculate  $\beta$  component of the reference three phase load currents
8. The controller generate the eight vectors of inverter output voltage ( $V_{out}$ ) according to the eight possible switching states.
9. The inductor current is calculated for the next instant ( $t+T_s$ ) using (1) or (3).
10. The capacitor voltage is calculated for next instant ( $t+T_s$ ) using (2) or (4).
11. Predicted output current is calculated by (5).
12. The distance between the predicted output current and the reference output current (cost function) is calculated by (6).
13. Repeat steps from 9 to 12 for every switching state of the eight states.
14. The optimizer identifies the optimal state among the eight states; which has a minimum cost function value.
15. The controller produces the switching signals to drive the power switches.
16. Repeat all the steps for every sample time ( $T_s$ ).

### **6.3. Parallel Processing and FPGA Implementation**

#### **6.3.1. Proposed Parallel Processing**

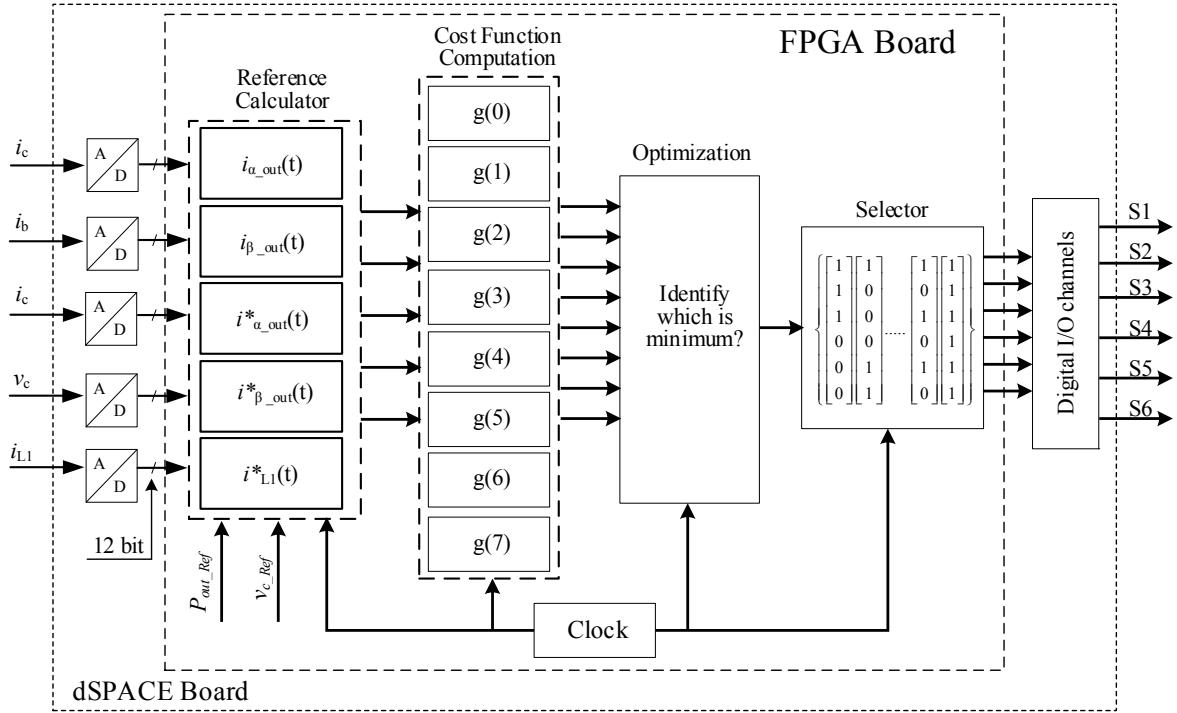
Figure 3 shows the proposed parallel-processed MPC algorithm's drive synthesis flowchart and FPGA hardware architecture. To overcome the above-addressed consecutive-processing drawback, the MPC algorithm is configured for parallel processing with a fixed-point 16-bit arithmetic. Most of the sequential processes are converted into parallel channels. The controller achieves MPC algorithm computations concurrently as follows:

- Inductor current, the capacitor voltage and the three phase output current are sensed and sampled through a set of analog to digital converters (ADCs) in parallel.
- The generation of reference output currents, the conversion of ABC to  $\alpha\beta$  form of the three phase output currents and the three phase reference currents, and calculation of the reference inductor current are computed in parallel.
- The cost function is computed for every switching state of the eight possible states in eight parallel processing computation channels.
- The optimizer identifies the optimal state among the eight states; which has a minimum cost function value.
- The selector produces the switching signals from the stored states inside a ROM, according to the identified optimal state index, to drive the power switches.

### ***6.3.2. FPGA-Based Digital Design and Implementations***

The proposed implementation is developed in MATLAB Simulink environment using System Generator ISE Design Suite 13.4. Then the target Xilinx Virtex-5 LX50T-1C FPGA is programmed using ControlDesk Next Generation 4.3 Software.

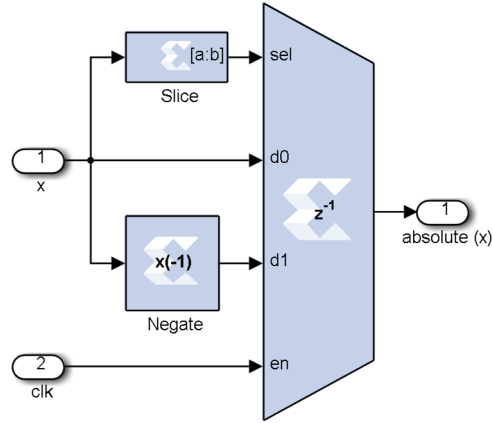
Many innovative digital implementation ideas can be designed, tested, and implemented inside the proposed FPGA-based controller. The parallel-processed implementation targets at short computation time and high accuracy as well. Figure 88 shows a number of these innovative examples; which can be briefly described as follows:



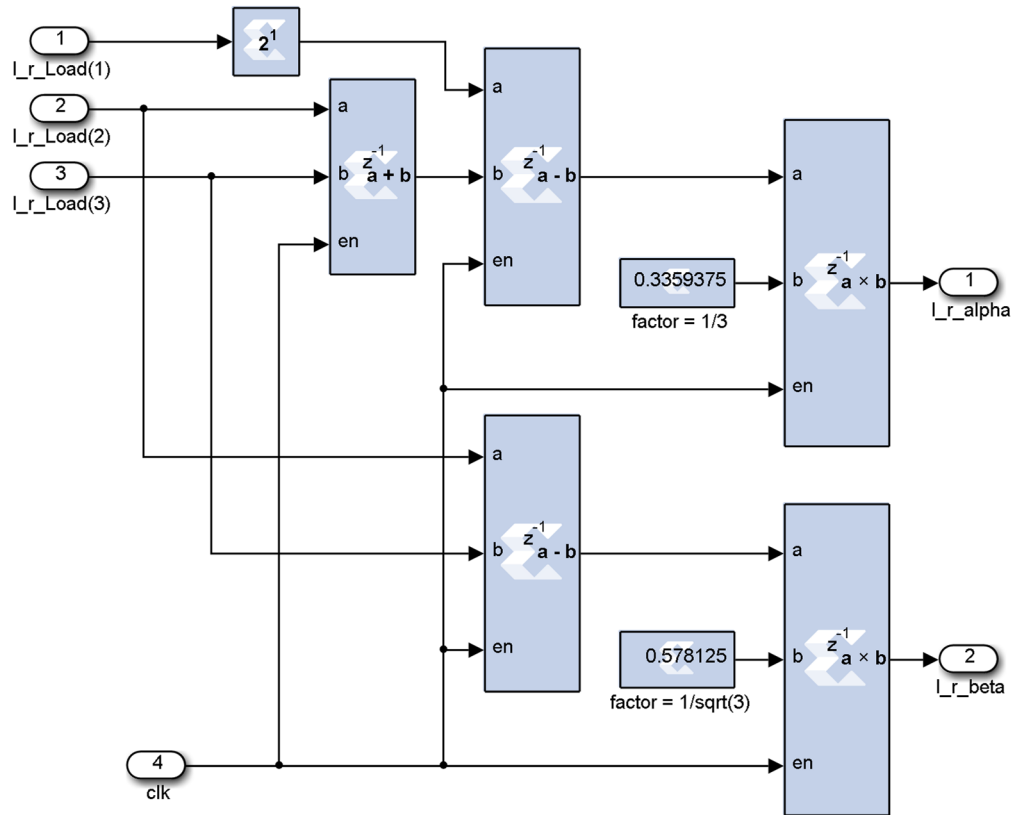
**Figure 87: FPGA hardware architecture and drive synthesis flowchart of the proposed parallel-processed MPC algorithm**

Figure 88(a) shows the absolute function calculation; the sign-assigned digit is sliced and is employed to drive a multiplexer to select the positive quantity whether it is the input quantity or its negation in a very simple and efficient way. Moreover, it consumes one clock only. Figure 88(b) ABC- $\alpha\beta$  transformation; the three phase currents are converted into  $\alpha\beta$  concurrently: both of  $\alpha$  and  $\beta$  components are computed in parallel. It consumes only three clocks. Figure 88(c) *Identify which cost function has a minimum value*; after computing all the eight cases of cost function, every cost function's output value is compared with each of the other seven cost function's outputs of all possible states. The outputs of the comparators are connected to an AND logic gate to decide if the state of interest has the minimum among all other cost functions of other states. Therefore the multiplexer produces the index of such switching state, otherwise the multiplexer holds the state index delivered by the previous stage. Accordingly, seven cascaded



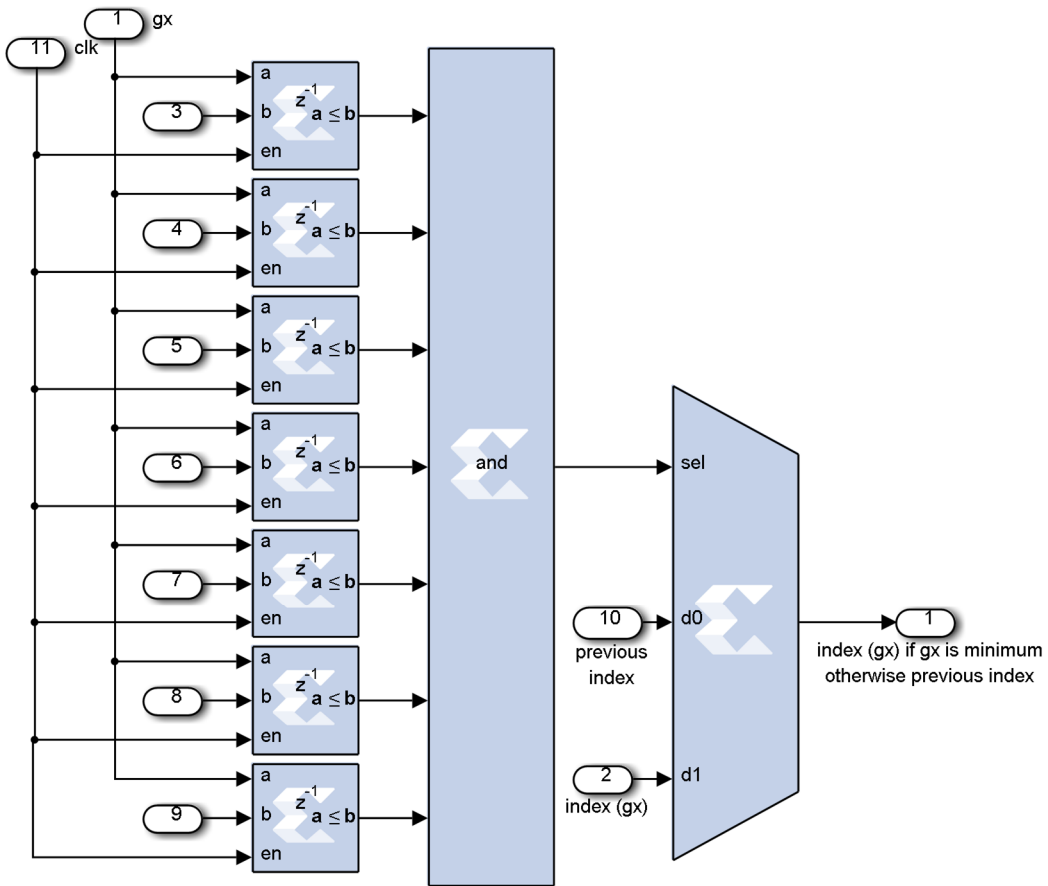


(a) Absolute function calculation



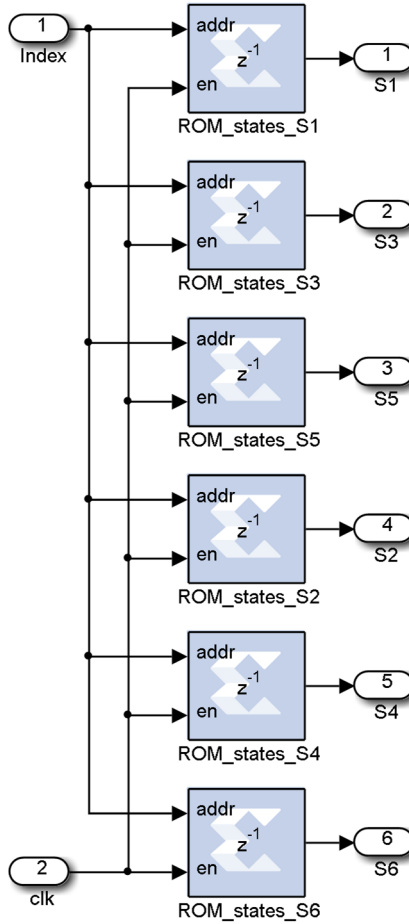
(b) ABC- $\alpha\beta$  transformation

**Figure 88: Digital design and implementation examples**



(c) Compare to identify which cost function has a minimum value (one of seven cascaded stages)

**Figure 88: Continued**



(d) Produce gate signals according to index.

**Figure 88: Continued**

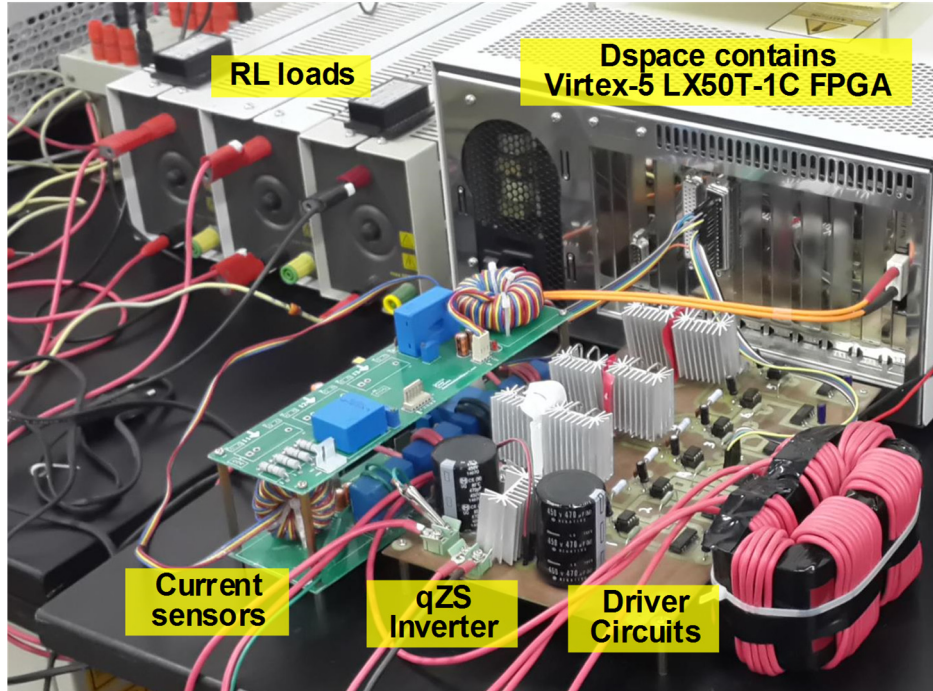
stages are employed in a very systematic and efficient way. They consume only seven clocks. Figure 88(d) produces the gate signals according to index; the selector uses the pointer (identified optimal state index) to handle the switching signals (in form of an array located inside a ROM) and produces it to drive the power switches. It consumes one clock only.

## 6.4. Experimental Investigation and Discussion

### 6.4.1. *Experimental Investigation*

The proposed controller has been experimentally validated. The experimental setup of the built qZSI prototype, controlled by the proposed parallel-processed MPC is shown in Figure 89, according to the overall system parameters addressed in Table 9.

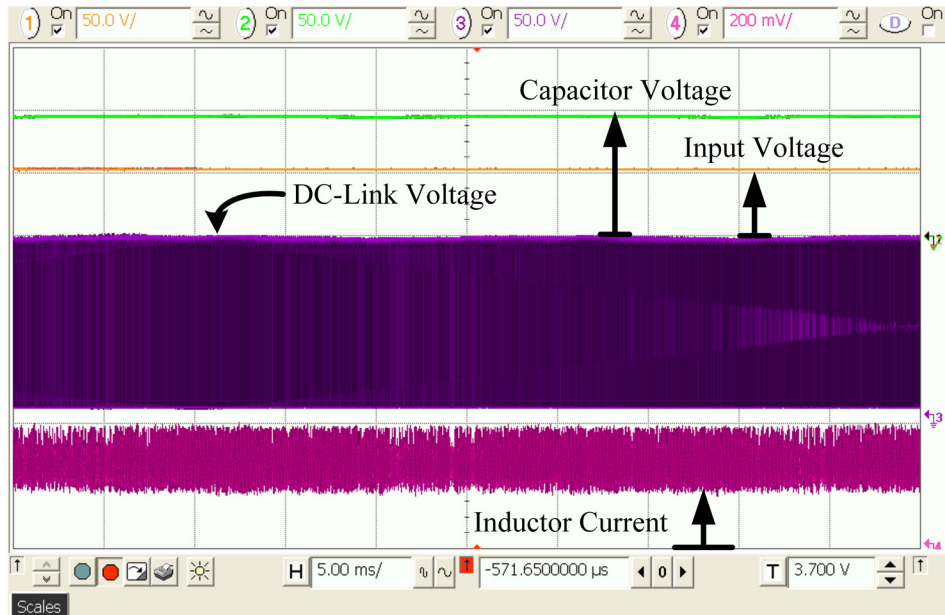
Capacitor type is EPCOS-B43501A9477M 470 $\mu$ F 400V aluminum electrolytic and the core of the inductors is AMCC 250 Metaglas UU core. The three phase qZSI employs GA35XCP12-247 SiC switches. The three-phase output currents, capacitor voltage, and inductor current are sensed and are sent to the controller as shown in Figure 85 and Figure 89. Then, they are converted into 12-bit digital signals by means of ADC inside the controller. The MPC optimizing computations are implemented and are executed in parallel inside a Xilinx Virtex-5 LX50T-1C FPGA board; as described in the previous sections. In the studied case, the three phase AC output reference current peak is 4.3A and the reference inductor current is 6A. Eight Space Vector Modulation (SVM) states are generated inside the FPGA board then one state is chosen and fed to the driver circuit to drive the switches. Figure 90 shows the input voltage (50V dc), the capacitor voltage (about 100V), the DC-link voltage, and the DC inductor current. These waveforms are zoomed and presented in Figure 91, where the DC-link voltage has a pulsated shape: it becomes zero at the shoot through time while the inductor current is charging. Figure 92 shows the input voltage, the capacitor voltage, the inductor current, and the output current.



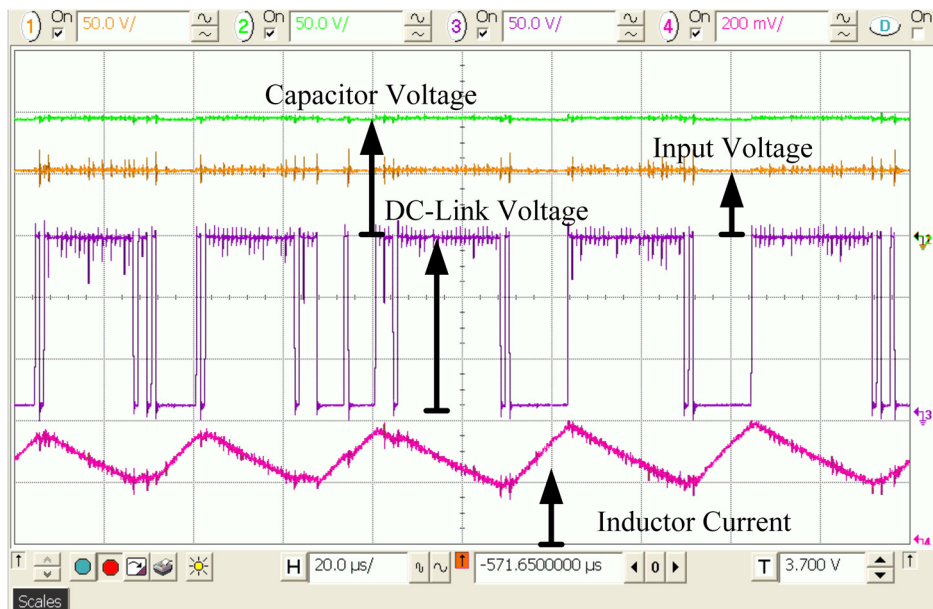
**Figure 89: Experimental setup**

**Table 9: The Overall System Parameters**

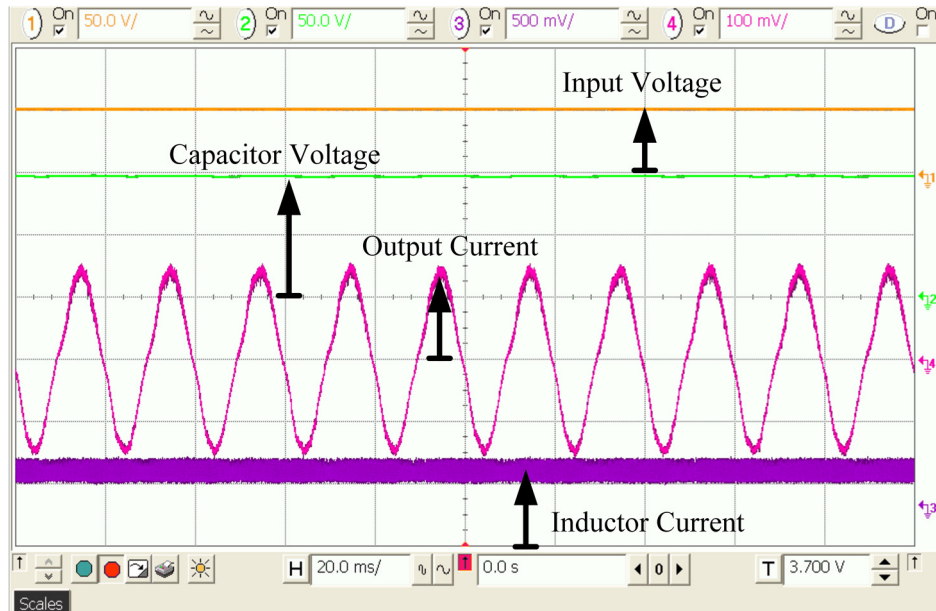
Symbol	Description	Value
$V_{in}$	Input DC voltage	50 V
$L_1, L_2$	qZSI inductance	500 $\mu$ H
$C_1, C_2$	qZSI capacitance	470 $\mu$ F
$F_{sw}$	Switching frequency	$\leq$ 500 kHz
$L$	Load inductance	12 mH
$R$	Load resistance	10 $\Omega$
$T_s$	Sampling time	1 $\mu$ S



**Figure 90: Input voltage, capacitor voltage and DC-link voltage and inductor current**



**Figure 91: Input voltage, capacitor voltage and DC-link voltage and inductor current (zoomed)**



**Figure 92: Input voltage, inductor current, capacitor voltage, inductor current, and output current**

#### 6.4.2. Discussion

The proposed work is compared with a number of close previously-published FPGA-based implementations of MPC algorithms in literature. The comparison is illustrated in Table 10. The most significant features of the proposed work are its short sampling time interval that reflects fast processing speed, which results in its capability to drive high speed SiC-/GaN-based converters, and its compact size due to the use of qZSI.

On the other hand, limitations of the proposed work are that the switches action is updated every two sampling time intervals ( $2T_s$ ), which limits the switching frequency to a maximum of 500 kHz. Further optimization of the employed MPC algorithm may lead to shorter processing time and hence such constraint can be mitigated.

It is clear that model predictive controllers could successfully achieve many sophisticated applications. Furthermore, FPGA design software environments have become more convenient and efficient than ever before, which allows for the use of high-level programming languages (e.g.

Labview-FPGA) or coder generation (e.g. Matlab/Simulink). Thus, it is expected that FPGA techniques will disseminate even more widely in power electronics and drive systems in the near future [188].

**Table 10: A number of previously-published FPGA-based implementations of MPC algorithms, compared with proposed work**

Feature		Previously-published work					Proposed work
		[187]	[186]	[194]	[183]	[188]	
Topologies employed		Two 3ph bridge rectifiers, Basic VSI, dc-dc converter	Three-phase three-level neutral-point-clamped inverter	A diode bridge rectifier and a dc-ac power inverter	Cascaded half bridge converter	Back-to-back power converter	qZSI
System size		Large	Medium	Small	Small	Large	Small
Sensed Parameters		$i_{out(a,b)}, E_{dc}, \theta_m$	$v_{c1}, v_{c2}, i_{grid(a,b,c)}, v_{grid(a,b,c)}$	$i_{out(a,b)}, E_{dc}, \theta_m$	$v_{dc}, i_{grid(a,b,c)}, v_{grid(a,b,c)}$	$v_{dc}, i_{grid(a,b,c)}, i_{load(a,b,c)}$	$i_L, v_c, i_{out(a,b,c)}$
Complexity of control algorithm		High	High	Medium	High	High	High
Implementation Hardware	FPGA	Xilinx Spartan 3 XC3S400PQ208	Xilinx Spartan XC3S500E	Altera Cyclone IV EP4CE55F23C7	Xilinx Spartan XC3S3500E	NI-CRIO system	Xilinx Virtex-5 LX50T-1C
	Clock	50 MHz	50 MHz	50 MHz	50 MHz	40 MHz	100 MHz
Achieved sampling time		100 $\mu$ S	100 $\mu$ S	102.4 $\mu$ S	50 $\mu$ S	50 $\mu$ S	1 $\mu$ S
Constraints/Drawbacks		Not Reported	A fully parallel implementation requires optimization to hardly fit the FPGA resources.	Inappropriate starting of flux-weakening operation is mitigated by reducing the gains of the outer voltage loop, which slow down the loop dynamic performance.	Generating the clock system using counters increases the possibility of failure. Another critical factor is the use of block rams to store rectifier switching function in $dq0$ frames.	Modeling errors and/or ideal efficiency consideration may lead to dc-link voltage steady state errors.	Switches status is updated every two sampling time intervals ( $2T_s$ )
Suitable technology application		Synchronous motor drive	Interface variable-speed wind turbines to the grid.	PM synchronous machine, especially, where flux-weakening operation occurs.	Medium voltage ac drives, multi-cell converters	Drive systems, grid-tied renewable energy interfaces	SiC-/GaN-based converters



## 6.5. Conclusion

This chapter addressed the design and the implementation of FPGA-based parallel-processing of an MPC for fast switching qZS inverter. The main contribution of this work is to benefit of highly-efficient promising switching devices such as SiC and GaN for their high switching speed capability and low on-state resistance by increasing the switching frequency of the inverter. As a result, the size and the ripple of the qZSI are effectively reduced and the dynamic performance is improved.

The novelty of the proposed contribution lies in parallel processing of the MPC algorithm and its innovative implementation using FPGA, which led to a great increase in the processing speed: A 300 times faster computation capability than the conventional sequential implementations was achieved (Parallel- computing:  $T_s=1\mu\text{S}$  with a 100 MHz processing clock, Sequential computing:  $T_s=30\mu\text{S}$  with a 1 GHz processing clock).

The effect of using the proposed parallel-processed MPC on the performance of SiC qZSI has been experimentally investigated using a Xilinx Virtex-5 FPGA-Based controller. The experimental results validate a good functionality of the proposed controller. Moreover, a theoretical framework for the employed MPC algorithm has been provided.

This work may be extended in two aspects, namely, the employed MPC algorithm can be developed to further reduce the processing time, and the proposed concepts can be generalized to be applied to other sophisticated algorithms and/or other fast switching power converters for the same purpose.

## 7. CONCLUSION AND FUTURE WORK

This dissertation focused on two main aspects: modified multilevel inverter and model predictive control of the modified multilevel inverter and qZ-Source inverter.

### 7.1. Conclusion

The *first aspect* is the modified multilevel inverter with less number of components in comparison to the conventional multilevel inverter topologies. The number of components for single and three phase and total voltage stress comparison between the modified topology and six conventional topologies (CHB, NPC, FC, RV, T-Type, and MLMI) are studied. A model predictive control technique has been adopted to control the proposed topology which achieved a high performance in a steady state and during transients. In addition, the use of multilevel DC-DC converter eliminates the challenge of the grounding of the sources in the multilevel inverter. Moreover, maximum power point tracking by using MPC is proposed in this dissertation to improve the performance of the conventional MPPT algorithm.

The *second aspect* is to increase the power density of the Power Conditioning System (PCS) by using a one stage (buck and boost) qZ-Source inverter which replaced the conventional two stages topology. A high efficiency solution has been achieved by controlling simultaneously both sides of the qZSI (ac output current, DC input voltage, and DC input current). Finite Control Set Model Predictive Control technique (FCS-MPC) has been proposed by replacing one null state in the voltage vectors with the shoot-through state. In addition, an accurate predictive modelling of the qZ-Source inverter has been proposed and implemented. The results show that the proposed feedback control when using MPC achieves higher performance and lower total harmonic distortion when compared with the conventional technique.

The main contributions of this dissertation can be listed as following:

- Proposed modified DC-Link multilevel inverter with less power switches for PV application.
- Proposed an MPC technique for maximum power point tracking (MPPT).
- Proposed a robust and accurate MPC for qZSI.
- Reduce a computational time delay by using parallel processing in the FPGA

In sum, the goals which have been mentioned in the introduction chapter, have been fulfilled by simulation and experimental results.

## **7.2. Future Work**

The work in this dissertation has opened new challenges that require more research in the future. The challenges can be listed as following;

- Optimize the proposed multilevel inverter to be suitable for any high power application.
- Modifying the proposed Maximum Power Point Tracking (MPPT) algorithm to be suitable for any partial shading PV system.
- Optimize single phase qZSI components to overcome the problems of the double line frequency.
- Extend the three phase two level qZSI for multilevel qZSI for high power applications.
- Find a numerical method to calculate the weighting factors in the cost function.

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