HARVESTING ULTRA-LOW POWER WIRELESS SIGNALS IN THE GHZ RANGE

An Undergraduate Research Scholars Thesis

by

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ABSTRACT

Harvesting Ultra-low Power Wireless Signals in the GHz Range

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We present methods for harvesting wireless energy as low as -30 dBm (1 μW) from the 2.4 GHz frequency range (e.g. WiFi signals) with discrete components. We have constructed a proof-of-concept device which is capable of operating at -18.8 dBm (13.2 μW) with no onboard power sources, relying solely on the 2.4 GHz energy source. The device is constructed on a PCB and consists of an impedance matching network, a rectifier, and a DC-DC converter. The impedance matching network matches a 2.4 GHz 50 Ω input source to the high impedance rectifier and provides a passive boost. The rectifier converts the AC signal from the impedance matching network to a DC signal. This DC signal feeds into the DC-DC converter subsystem which boosts the voltage from about 45 mV DC to a clean 95 mV DC output.

ACKNOWLEDGMENTS

We would like to sincerely thank Dr. Karsilayan and Dr. Silva-Martinez for their invaluable time and support they provided us during this project. Their continued advice throughout all stages of the project provided us an educational experience that we could never have achieved through any other undergraduate program, covering topics including analog, digital, power, and electromagnetics.

We would also like to thank graduate student Troy Buhr for his help, especially in regards to practical considerations of board design and assembly including assistance in soldering a tiny 0201 SMD diode.

Finally, we would like to thank undergraduate Preston Anthony Parks for his assistance in researching alternative impedance matching networks for the IEEE Circuits and Systems Student Design Contest.

SECTION I

INTRODUCTION AND OVERVIEW

Wireless power will charge the next generation of technology. With commercialized products based on this concept, low power systems such as smoke detectors could have a lifetime limited only by the parts. Mobile sensor networks typically include many battery-powered wireless sensor devices. Replacing batteries for such devices is costly and often impractical. Harvesting power to charge batteries, or completely relying on harvested power for sensor operation, enables deployment of almost maintenance-free low-cost sensors at a large scale. Our research aims to contribute to the development of these future technologies by pushing the lower bound of input power.

Previous research in this field has been able to achieve effective results as low as around -20 dBm input power [1], [2]. Other research has also been able to achieve successful harvesting as low as -25 dBm [3]. Our goal was to expand upon this research to design a circuit capable of harvesting at -30 dBm.

High-level Description

The device is designed to harvest power from WiFi signals (2.4 GHz) at -30 dBm and produce a steady 100 mV DC power output. Commercially available chips can boost a 100 mV output to higher voltages [4]. As shown in Figure 1, the device is subdivided into 3 subsystems: 1) an impedance matching network, 2) a rectifier, and 3) a DC-DC converter which includes an internal oscillator.

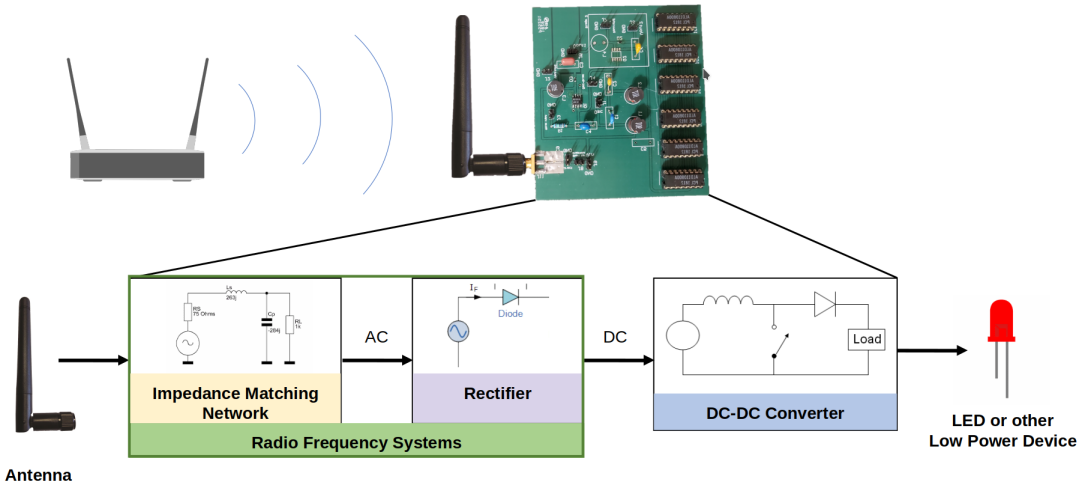

Figure 1: Illustration of the full device and its subsystem breakdown

The Wi-Fi (2.4 GHz) band was chosen since it's an easily accessible spectrum filled with strong signals in most environments. Assuming no path loss, an isotropic radiator, a transmission power of 4 W (which is a typical WiFi router power), a frequency of 2450 MHz, and a received power of -30 dBm, we can calculate the maximum distance from the transmitter that our device can still harvest power from a WiFi router using the following equation.

$$S = \frac{P_t}{4\pi R^2}, P_r = \frac{S\lambda^2}{4\pi} \qquad \text{(Eq. 1)}$$

P_t is equal to power transmitted, P_r is equal to power received, λ is the wavelength of the signal, R is the distance from the transmitter and S is the flux density at the surface of a sphere. So, from Eq. 1, the device has a maximum distance of about 20 m. This number will become larger in the event a directional antenna is used and become smaller for environments with high path loss.

The device is constructed out of purely discrete components. A more aggressive goal is to design an IC. However, using only discrete components decreases production time and cost but also introduces complications at ultra-low voltages since the components are restricted to only those currently available on the market. Figure 2 shows the completed device on a PCB.

Figure 2: Final PCB encompassing the entire device on one board

SECTION II

MICROWAVE FREQUENCY SUBSYSTEMS

Dealing with RF systems and the extremely low input power presents special design challenges. At the input voltages we are expecting, most active components will not work at these low voltage levels. Therefore, the first subsystem is a purely passive boost.

$$\frac{Vout}{Vincident} = \sqrt{\frac{R_{out}}{R_{in}}} \qquad \text{(Eq. 2)}$$

Eq. 2 allows us to calculate the ideal voltage boost of our passive network between the incident voltage on the circuit and the output voltage of the impedance matching network. $Vout$ and $Vincident$ are marked on Figures 3 and 4.

Impedance Matching Network

The RF matching circuit also needs to solve the impedance mismatch between the 50 Ω input and the 2 kΩ load. A perfect impedance match allows 100% of the power to flow from the input to the load with a passive voltage boost of 6.32x as calculated from Eq. 2. We used the voltage standing wave ratio, SWR, as a measure of how well the load is matched. An ideal impedance match has a SWR of 1. The following equation shows how to calculate the SWR from S_{11}. S_{11} measures reflections coming from the input.

$$SWR = \frac{1 + |S_{11}|}{1 - |S_{11}|} \qquad \text{(Eq. 3)}$$

Due to the difficulties of working with RF frequencies, many hours of research and simulations went into designing the matching networks before building them to avoid long debugging in the lab. RF signals are especially susceptible to stray capacitance, inductance, and coupling. Also, the inductors and capacitors become problematic at their self resonant frequencies where the parasitic inductance or capacitance becomes comparable to the built in capacitance or inductance.

This creates a band pass filter in the circuit which is not desirable. The inductors we chose have a self resonant frequency of 4.6 GHz [5].

Multiple circuit layouts were considered and simulated. Of those, we evaluated two matching circuits for the project. The first was an open stub matching circuit as shown in Figure 3. The second was a discrete component matching circuit as shown in Figure 4. In the case of an open stub matching network, the traces had to be designed to carry the 2.4 GHz signal with minimal loss. A special and expensive board material is required to allow the traces to work as reliable transmission lines. For a passive component matching circuit, the traces have to be designed to minimize the parasitic inductance and capacitance. The discrete component circuit was chosen because of lower loss in simulations and the cheaper board cost. Two iterations were made off of this circuit. For the final iteration, the layout was improved to reduce stray inductance and capacitance to achieve a better match at 2.4 GHz.

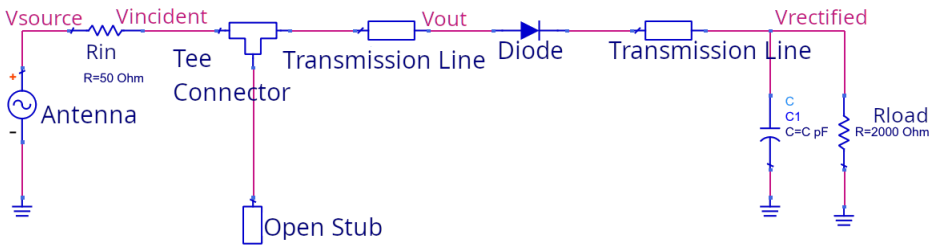

Figure 3: The open stub matching circuit

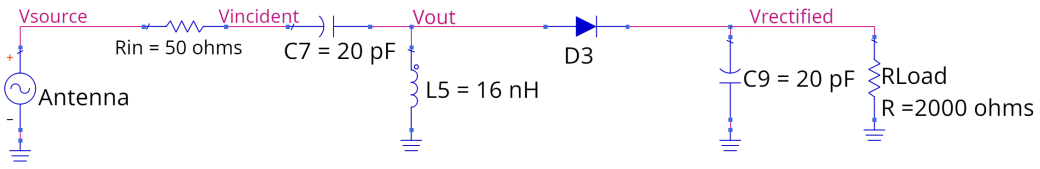

Figure 4: Passive matching network with rectifier

The rectifier for the system consists of a half-wave diode rectifier which converts the 2.4 GHz AC signal to DC. The half-wave design was chosen to keep the DC voltage as high as possible

by reducing the nonidealities of multiple forward diode drops such as with a full wave rectifier. The rectifier circuit integrated with a passive matching network is shown in Figure 4 and the output is shown in Figure 5 with a -30 dBm input.

The SMS7630 family of diodes was chosen for this project. The diode has less than a 60 mV drop below 1 mA of current which is the expected current levels of the circuit [6]. This diode could only be obtained in the 0201 or SC-79 packages, each less than 2 mm in size.

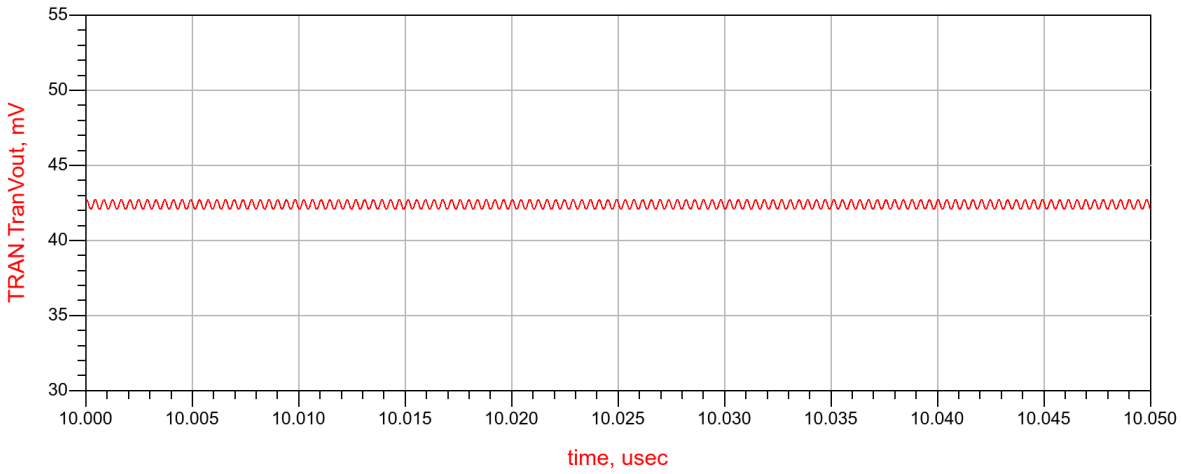

Figure 5: The first iteration rectifier output simulation showing a 45 mV DC output voltage

Microwave Frequency Subsystem Results

The first iteration PCB which included the impedance matching network and rectifier was designed and manufactured. Figure 6 shows the assembled PCB. A screw terminal block was added to the PCB to make changing out connections easier and more reliable. Figure 7 shows the block diagram of the testing configuration and Figure 8 shows the testing configuration with a screw terminal block installed.

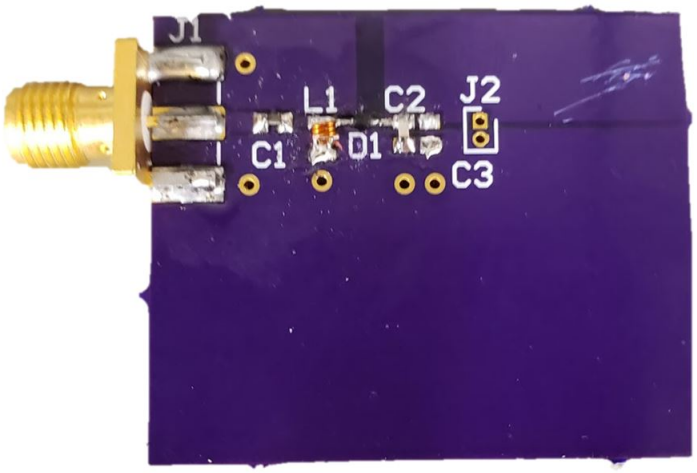

Figure 6: The fully assembled first iteration rectifier and impedance matching network

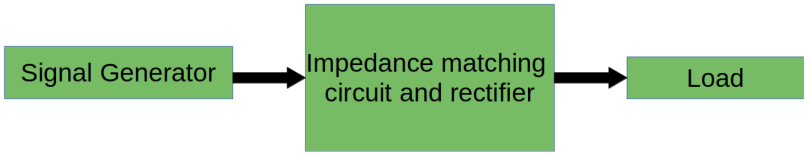

Figure 7: The test setup for the impedance matching circuit and rectifier

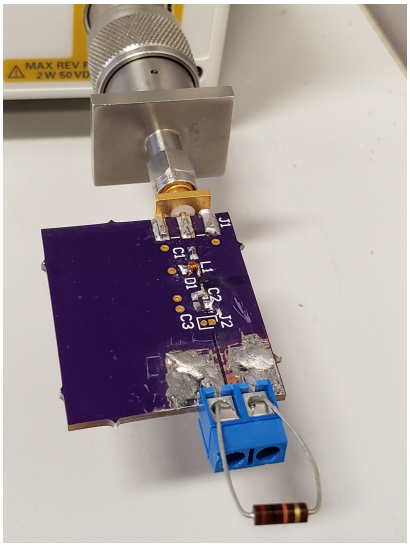

Figure 8: The testing configuration of the PCB with a signal generator with a 20 kΩ load

The first iteration circuit was tested and measured at the AMSC lab at Texas A&M University. Figure 9 shows the output voltage of the rectifier at different input power levels.

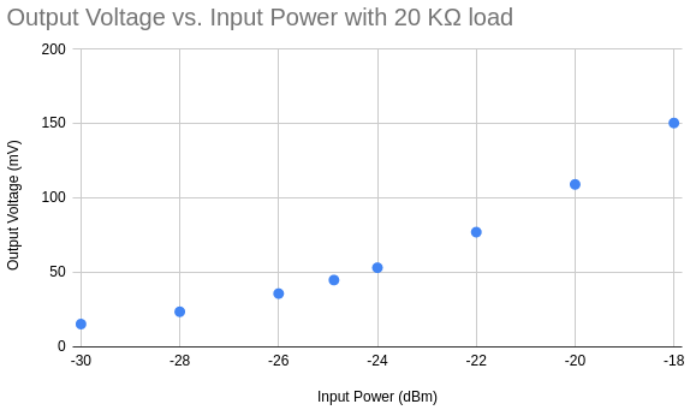

Figure 9: The measured rectified output DC voltage across a 20 kΩ load at different power levels

This first iteration circuit provided 15 mV out at -30 dBm, not meeting our specification of 45 mV. This was to be corrected in the final iteration. The circuit still performed well for the first draft by producing 45 mV DC out at -24.8 dBm. This comes out to passive boost of 2.5x with a 20 kΩ load. The diode is the major factor that cuts down the gain because of the voltage drop.

Measurements were also taken with a network analyzer. Figure 10 shows the simulated reflections on the input and Figure 11 shows the measured S11 output from a network analyzer on the input. The equipment setup is the same as in Figure 7.

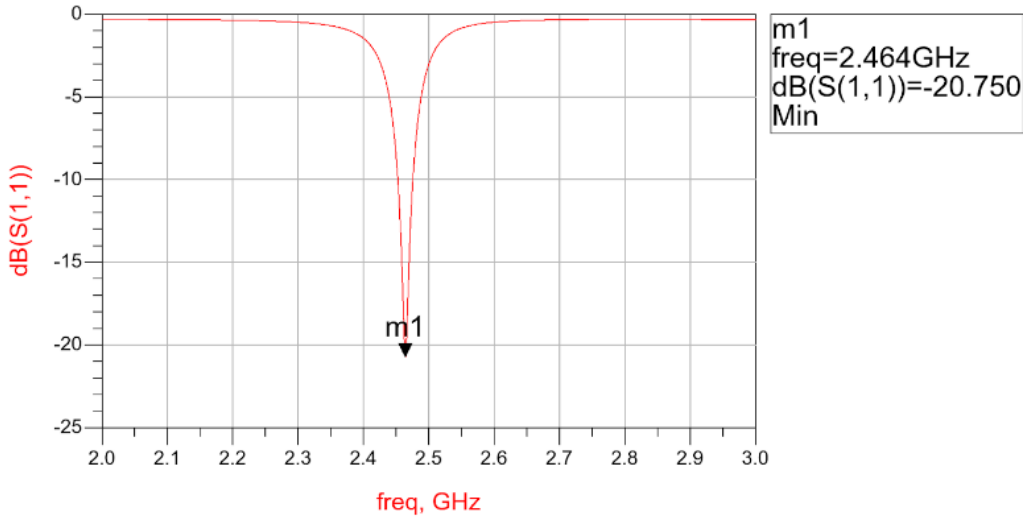

Figure 10: The desired and simulated frequency response of the circuit with reflections coming to a minimum around 2.45 GHz

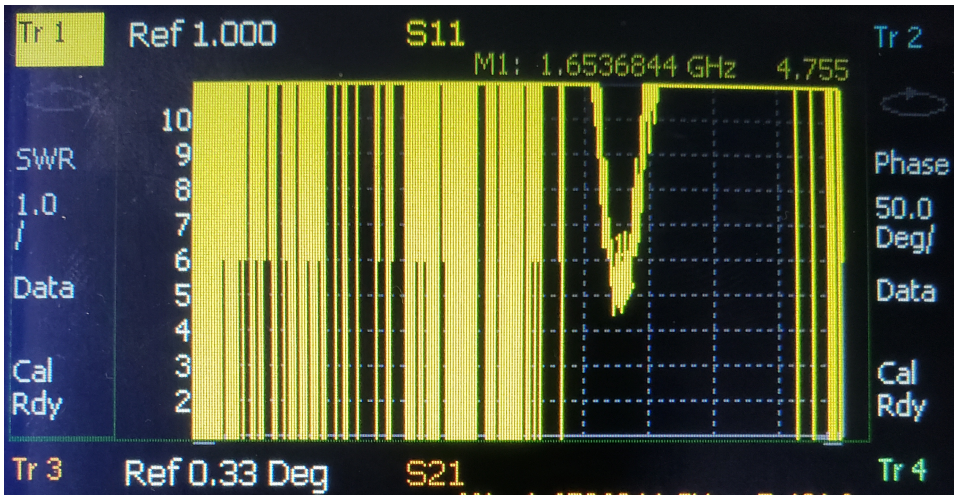

Figure 11: The measured response of the circuit with reflections on the input coming to a minimum around 1.65 GHz

As can be seen, the circuit is working at an offset frequency of 1.65 GHz with moderate reflections. For the final iteration, we produced a PCB that was supposed to improve upon these factors, but we were unable to measure the PCB. Figure 12 shows the Altium model of the final RF circuit section of the board. The ground plane has been expanded and more vias have been drilled to reduce inductance.

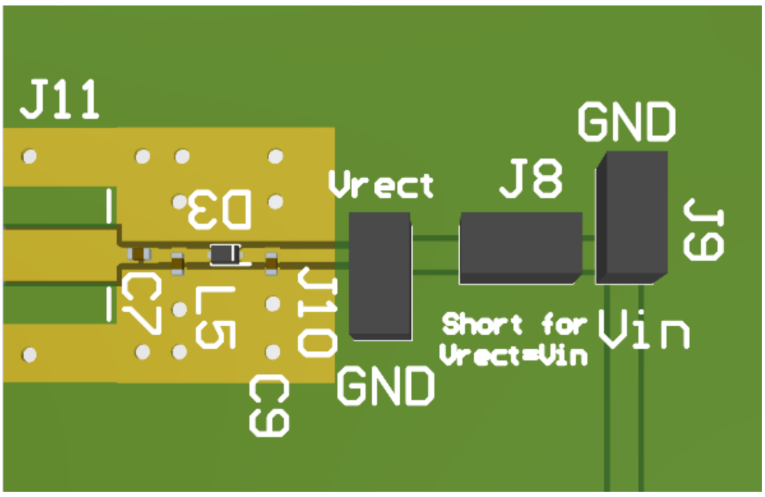

Figure 12: In this final iteration of the RF section, the vias were dramatically improved to lower inductance

SECTION III

DC-DC CONVERTER SUBSYSTEM

The overarching design of the DC-DC Switching Converter subsystem is illustrated in Figure 13. The first stage is a custom designed switching converter which takes as input the voltage from the rectifier, as low as 45 mV, and outputs over 90 mV. Commercially available chips can boost 90mV to higher voltages [4].

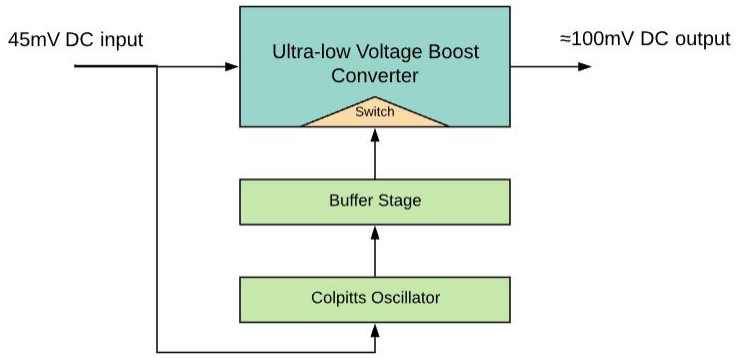

Figure 13: High level block diagram of the DC-DC converter

The boost converter requires an oscillator to drive the switch of the switching converter. This oscillator must be powered solely by the 45 mV input to the subsystem. Two methods for producing these low voltage oscillations were explored.

Ring Oscillator Research

A ring oscillator using three inverters and a buffer stage was characterized and optimized for low voltages. The inverters were built from the ALD110800 and ALD310700 which is the NMOS and PMOS versions, respectively, of the near zero-threshold transistor. These were the best discrete components found available for this design. However, with the schematic from Figure 14, sustained oscillations could only be obtained at voltages above 400 mV. Furthermore, even at

500mV, these oscillations had a peak-to-peak voltage of only 250 mV as shown in Figure 15. Despite efforts to optimize further, the discrete ring oscillator was eventually deemed not practical for use in this project as even with CMOS technology the lowest voltage ring oscillators function above 50 mV [7].

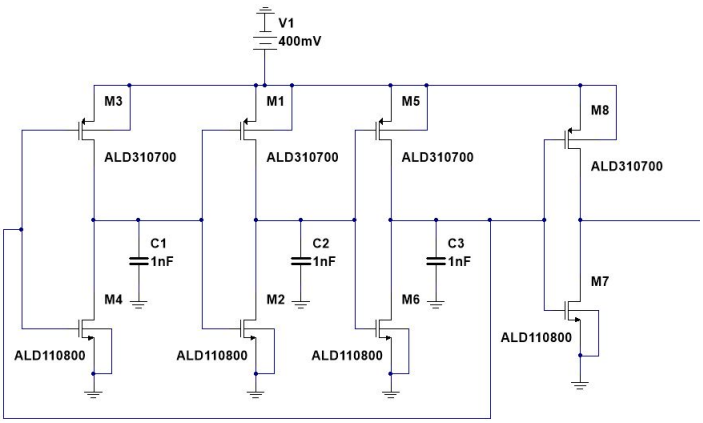

Figure 14: Ring oscillator schematic including buffer stage

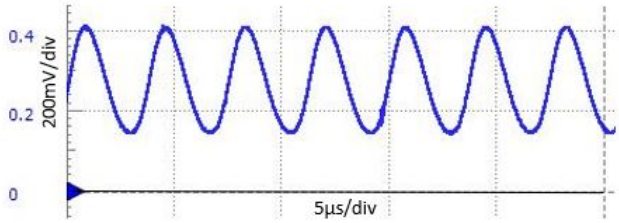

Figure 15: Ring oscillator output at 250 kHz with 500 mV DC input

Colpitts Oscillator

Previous research by [8] on ultra-low voltage oscillators indicated that a Colpitts oscillator produced strong oscillations at voltages above 20 mV. This circuit was adapted and optimized to suit the needs of the wireless power harvesting system. Specifically, the oscillator needs a capacitive load on the output which was not considered in the previous research. The load is about 60 pF as described in the following subsection. To account for the capacitive load and parasitics present, the capacitor values, C1 and C2 as seen in the schematic of Figure 16 for the

Colpitts oscillator, were tweaked until a maximum gain was achieved. These values were re-tweaked between iterations with slight modifications made as seen between the schematics of the next section.

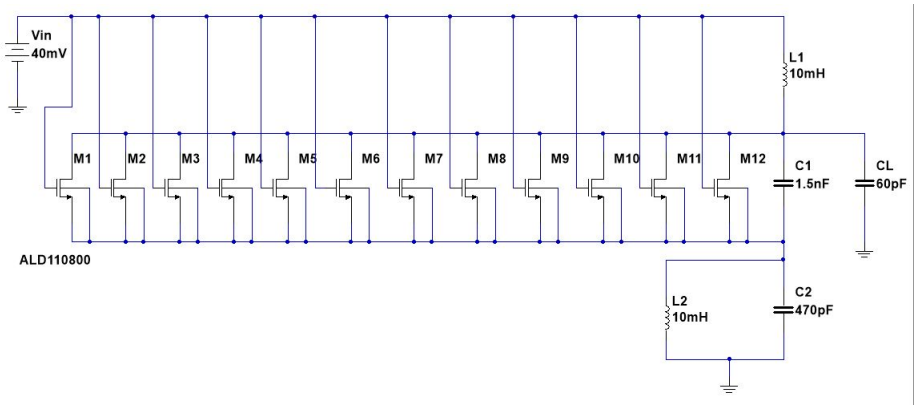

Figure 16: Colpitts oscillator schematic as incorporated in the first revision circuit

$$f_{oscillator} = \frac{1}{2\pi\sqrt{L_1(C_1C_2/(C_1+C_2)+C_L)}} \qquad \text{(Eq. 4)}$$

In measurements, the Colpitts oscillator was demonstrated to generate a high gain at the desired input voltage of 45 mV and produce a frequency around 95 kHz which matches closely with the predicted result of 78 kHz from Eq. 4. As seen in Figure 17, with a 40 mV DC input, the Colpitts circuit generates a sine wave of about 300 mV pk-pk. Table 1 tabulates the amplitude of the Colpitts oscillator at low voltages.

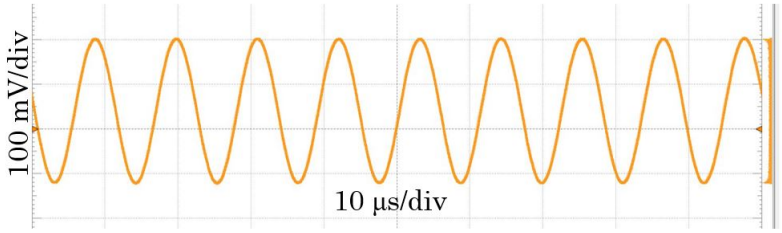

Figure 17: 300 mV pk-pk oscillator output at about 95 kHz produced with only 40 mV DC

Table 1: Results of the Colpitts with two ALD212902 transistors connected as load

DC Input	**Oscillator Pk-Pk**
80 mV	850 mV
50 mV	450 mV
45 mV	400 mV
40 mV	300 mV

Boost Converter

Two ALD212902 transistors in parallel act as the switch for the boost converter and their gates are the previously mentioned capacitive load for the Colpitts oscillator. These transistors have a threshold voltage of $V_{th} = 200 \pm 20$ mV and their gates each have a capacitance of about 30 pF [9]. The large gain of the Colpitts allows transistors with a relatively high threshold voltage to be effectively used as switches. Due to their much higher transconductance, these transistors performed better as switches than the ALD110800s [10]. The inductors used in the design have a self-resonant frequency of 600 kHz and an internal resistance less than 28 Ω which is a quality factor above 200 at the clock oscillation frequency [11].

$$Boost\ Factor = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \qquad \text{(Eq. 5)}$$

The switching duty cycle, D, can be roughly approximated as the fraction of the time that the ALD212902 transistors' gate voltage is above the threshold voltage. The gate voltage is a sine wave produced by the Colpitts oscillator. Higher input voltages increase the amplitude and shift the intrinsic DC bias of the oscillation up increasing the fraction of the time the oscillations are above the threshold voltage and thus increasing D. Therefore, from Eq. 5, the boost factor of the circuit will increase as the input voltage increases. This effect is seen in the following tables of this section and explains why the output voltage of the boost converter is not directly proportional to the input voltage.

$$L \geq \frac{D(1-D)^2 R_{load}}{2f} \qquad \text{(Eq. 6)}$$

$$C \geq \frac{D}{(\Delta V_{out-max}/V_{out}) R_{load} f} \qquad \text{(Eq. 7)}$$

For the design of the boost section of the DC-DC converter, D is estimated to be around 50% at the 45 mV expected input voltage. Thus, from Eq. 5, we should be expecting an output voltage somewhere around 90 mV. Using the oscillator frequency, f, as about 100 kHz and assuming a 8.1 kΩ load (the minimum load for 1 μW of available power at this voltage), Eq. 6 shows the minimum inductor value required to achieve continuous current. For a maximum voltage ripple of 10%, we can also calculate the minimum capacitance from Eq. 7. The minimum values are 5 mH and 6 nF respectively. Using the values of 10 mH and 47 nF, the boost converter schematic is shown in Figure 18 with the Colpitts oscillator directly connected to the switching transistor. This first revision circuit was implemented on the breadboard shown in Figure 19.

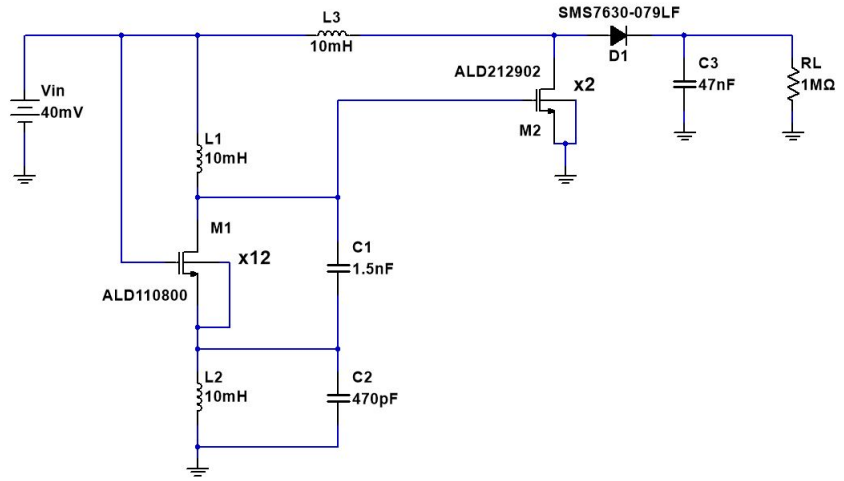

Figure 18: Boost converter schematic as used in the first revision with the Colpitts directly connected to the gate of the switching transistor, M2

Table 2: Measurements of the boost converter with a 1 MΩ load using the schematic in Figure 18

DC Input	DC Output	Boost Factor
80 mV	100 mV	1.25
60 mV	86 mV	1.43
50 mV	53 mV	1.06
40 mV	42 mV	1.05

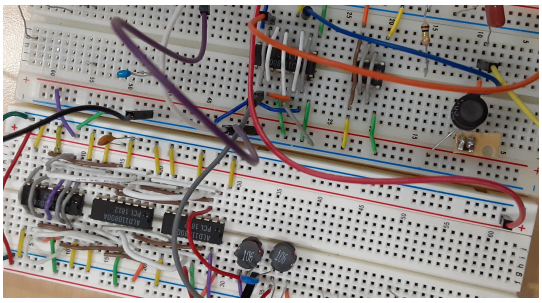

Figure 19: First revision of full boost converter using the schematic in Figure 18 before final PCB

As seen in Table 2, with this circuit structure, the results were far from the expected 2x gain. This is caused by the transistor only partially turning on and thus not applying a large enough potential drop across the inductor in the charging phase of the boost converter. To correct this issue, a 350 mV DC bias was added to the gate of the switching transistor. This addition shifts the midpoint of the oscillation above the threshold voltage of the transistor thus allowing the switch to turn completely on and ground the other side of the inductor during the charging phase. It also had an added benefit of increasing the duty cycle bringing it closer to the 50% approximated value at 45 mV input. Figure 20 shows the updated schematic with the DC bias added as seen in the final design which was implemented on a PCB. In Figure 21, the transistor of the boost converter can be seen to switch fully on demonstrating that the boost converter is operating as anticipated. This circuit achieved remarkable results and met the goals for the first stage.

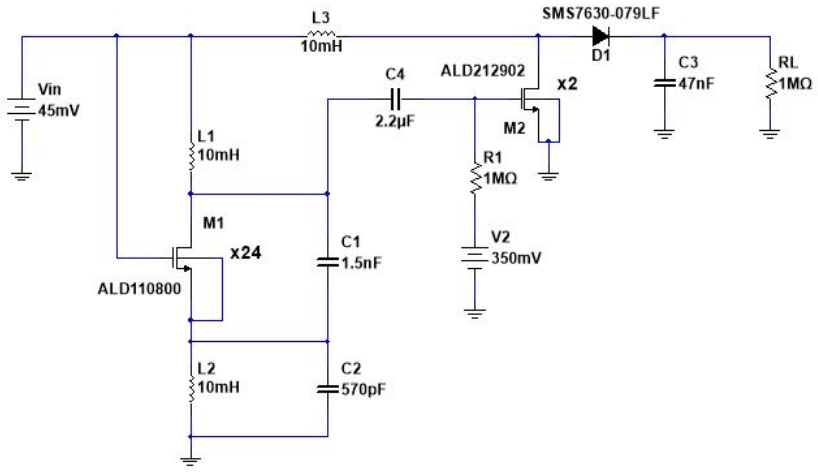

Figure 20: Final PCB design for the DC-DC converter with a 350 mV DC bias added to the switch input (but no power dissipated from the DC bias into the output)

As seen in the schematic of Figure 20, since all of the connections from the voltage source are purely capacitive, it's important to note that the power dissipated from V2 is effectively zero. Any power dissipated would only be in R1 and would be neglible. This ensures the output power is transferred solely from the wireless input source, Vin.

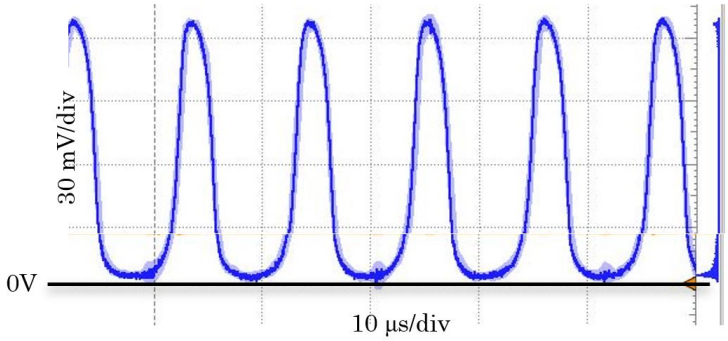

Figure 21: The voltage at the drain of M2 with 300 mV DC bias at 43 mV DC input

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)} \frac{1}{1 + r_L/(R_{load}(1-D)^2)} \qquad \text{(Eq. 8)}$$

$$\eta = \frac{1}{1 + r_L R_{load}(1 - D)^2} \quad \text{(Eq. 9)}$$

One of the largest factors of loss in a nonideal boost converter is the resistance of the inductor. This can decrease output voltage and efficiency as given by Eq. 8 and Eq. 9 respectively. Using r_L = 28 Ω, the manufacturer maximum, and the minimum possible load of 8.1 kΩ at -30 dBm, the loss due to inductor resistance is seen to be negligible; voltage decreases by a factor of 0.986 in the worst case and power by 0.0018% efficiency.

The final results of the boost converter are tabulated in Table 3 and the PCB circuit implementation can be seen in Figure 2. The voltage ripple was measured to be about 2 mV which, as predicted, exceeded our 10% specification. In terms of minimum startup voltage, our discrete DC-DC converter outperformed many other DC-DC converters presented in recent research including ones that used integrated CMOS designs [12], [13], [14]. Very recent publications were able to match our minimum DC-DC startup voltage performance using CMOS technology [15], [16].

Table 3: Measurements of the DC-DC converter on the final PCB with a 1 MΩ load using the schematic in Figure 20 and with the expected operating point highlighted

DC Input	**DC Output**	**Boost Factor**
150 mV	470 mV	3.13
100 mV	267 mV	2.67
60 mV	153 mV	2.55
50 mV	116 mV	2.32
45 mV	***94.2 mV***	***2.09***
40 mV	68.4 mV	1.71
35 mV	40.0 mV	1.14

SECTION IV

CONCLUSION AND RESULTS

For the full circuit in its first revision operating at an input power of -18.8 dBm at 1.66 GHz, we achieved an output voltage of 81 mV DC with a 1 MΩ load. Table 4 summarizes the results obtained by the full circuit. It should be noted that this version of the circuit did not include any DC bias. Thus, it operated solely on the -18.8 dBm input to the circuit.

The final revision of the PCB fully integrated the impedance matching circuit, rectifier, and boost converter onto a single circuit board. In this revision, the impedance matching network load was matched closer to the measured DC-DC converter load which was seen to be about 2.2 kΩ. It was also optimized for a smaller reflection coefficient and more precisely tuned for the desired frequency. Losses in the DC-DC converter were greatly minimized by transferring to a PCB thus improving the overall DC gain by a factor of 0.3x. The closure of the labs due to COVID-19 prevented us from performing measurements on this final improved revision. Despite this, the first iteration of our board performed well and shows promise for our methods of approaching the -30 dBm goal.

Table 4: First revision integration results

Input Power	-18.8 dBm (26 mV RMS at matching network)
Input Frequency	1.66 GHz
Output	81 mV DC

COVID-19 Pandemic Note

Due to the COVID-19 pandemic, we were unable to obtain full measurements on our final PCB design without access to the necessary high frequency equipment. However, parts of the DC-DC subsystem was able to be further characterized as discussed in section III above. The first revision prototype is split between PCB and breadboard as shown in Figure 6 and Figure 19. The

final revision is fully on a PCB as shown in Figure 2.

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