MILLIMETER-WAVE CONCURRENT DUAL-BAND SIGE BICMOS RFIC PHASED-ARRAY TRANSMITTER AND COMPONENTS

A Dissertation

by

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ABSTRACT

A concurrent dual-band phased-array transmitter (TX) and its constituent components are studied in this dissertation. The TX and components are designed for the unlicensed bands, 22–29 and 57–64 GHz, using a 0.18-μm BiCMOS technology. Various studies have been done to design the components, which are suitable for the concurrent dual-band phased-array TX. The designed and developed components in this study are an attenuator, switch, phase shifter, power amplifier and power divider.

Attenuators play a key role in tailoring main beam and side-lobe patterns in a phased-array TX. To perform the function in the concurrent dual-band phased-array TX, a 22–29 and 57–64 GHz concurrent dual-band attenuator with low phase variations is designed.

Signal detection paths are employed at the output of the phased-array TX to monitor the phase and amplitude deviations/errors, which are larger in the high-frequency design. The detected information enables the TX to have an accurate beam tailoring and steering. A 10–67 GHz wide-band attenuator, covering the dual bands, is designed to manipulate the amplitude of the detected signal. New design techniques for an attenuator with a wide attenuation range and improved flatness are proposed. Also, a topology of dual-function circuit, attenuation and switching, is proposed. The switching turns on and off the detection path to minimize the leakages while the path is not used.

Switches are used to minimize the number of components in the phased-array transceiver. With the switches, some of the bi-directional components in the transceiver

such as an attenuator, phase shifter, filter, and antenna can be shared by the TX and receiver (RX) parts. In this dissertation, a high-isolation switch with a band-pass filtering response is proposed. The band-pass filtering response suppresses the undesired harmonics and intermodulation products of the TX.

Phase shifters are used in phased-array TXs to steer the direction of the beam. A 24-GHz phase shifter with low insertion loss variation is designed using a transistor-body-floating technique for our phased-array TX. The low insertion loss variation minimizes the interference in the amplitude control operation (by attenuator or variable gain amplifier) in phased-array systems.

BJTs in a BiCMOS process are characterized across dc to 67 GHz. A novel characterization technique, using on-wafer calibration and EM-based de-embedding both, is proposed and its accuracy at high frequencies is verified. The characterized BJT is used in designing the amplifiers in the phased-array TX.

A concurrent dual-band power amplifier (PA) centered at 24 and 60 GHz is proposed and designed for the dual-band phased-array TX. Since the PA is operating in the dual frequency bands simultaneously, significant linearity issues occur. To resolve the problems, a study to find significant intermodulation (IM) products, which increase the third intermodulation (IM3) products most, has been done. Also, an advanced simulation and measurement methodology using three fundamental tones is proposed.

An 8-way power divider with dual-band frequency response of 22–29 and 57–64 GHz is designed as a constituent component of the phased-array TX.

DEDICATION

To my parents, Mr. Bongjin Bae and Mrs. Jungsim Cho,

my wife, Hyunsuk,

my sister, Joohyun,

and all of those who have inspired me to become what I am today.

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Some chapters in the dissertation are reprints of the paper published. The dissertation author is the primary author of the papers. The reference papers are:

For Chapter III, Juseok Bae and Cam Nguyen, "A novel concurrent 22–29/57–64-GHz dual-band CMOS step attenuator with low phase variations," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 64, no. 6, pp.1867–1875, April 2016.

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CHAPTER I

INTRODUCTION & BACKGROUND

1.1 Silicon-Based Millimeter-Wave RFICs

Wireless communications, sensing, and radar plays an essential role in the life of human being living in a fast-growing information era and are indeed necessary that the world cannot function properly without. Building RF wireless communications, sensing, and radar systems in single chips is no longer a "dream," but becoming a "reality." Silicon (Si)-based Radio-Frequency Integrated Circuits (RFICs), working within the RF/electromagnetic (EM) spectrum, are making this reality possible. RF transceivers and digital control circuits can be integrated on the same chip enabling low-cost, small-size, and high-performance single-chip solution. Advanced RF wireless systems and, in turn, RFICs are relevant not only to commercial and military applications but also to national infrastructures. This importance is even more pronounced as the development of civilian technologies becomes increasingly important to the national economic growth. New applications utilizing RFIC technologies continue to emerge, spanning across the EM spectrum, from ultra-wideband to millimeter-wave and sub-millimeter-wave ultra-high-capacity wireless communications; from sensing abnormal human body condition, diagnosing it and imaging the effect to early detection of cancer and un-attended health monitoring and examination; from sensing for airport security to through-wall imaging and inventory for gas and oil; and from detection and inspection of buried mine, UXO, underground oil and gas pipes to wireless power transmission and data communications

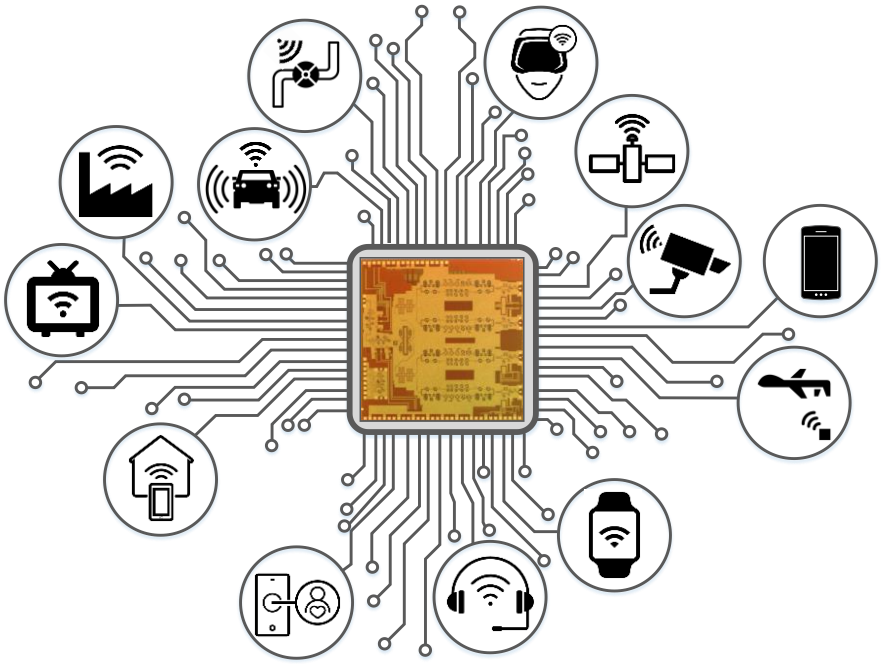


Fig. 1.1. Silicon-based millimeter-wave RFIC single-chip-solution and its applications.

for smart wells, etc. (Fig. 1.1). Research and development of new RFICs and systems are thus vital for both the commercial and defense sectors in a nation. They are particularly important for the development and advancement of wireless communications, sensing and radar technologies.

1.1.1 SiGe BiCMOS Technology

Silicon germanium (SiGe) Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) is the technology of choice for millimeter-wave RFICs due to its various merits. The cross-section of the SiGe BiCMOS process is simply shown in Fig. 1.2, which consists of nMOS and pMOS field effect transistors (FETs), and NPN and PNP bipolar-junction-transistors (BJTs). A SiGe NPN BJT is an advanced technology from Si NPN

BJT. The main difference between them is the material of base of BJT. By using SiGe for the base, the speed, gain, RF and 1/f noises, base resistance and operating frequency of the BJT are improved. In comparison with CMOS, although the BiCMOS process consumes more time and cost, it has a benefit of having available BJTs and CMOS FETs on the same substrate. The two types of transistors enable enhanced system performances, integration, and functionalities. The BJT has higher speed and better high-frequency characteristics ($f_t \approx$200 GHz) than CMOS. Also, it provides a larger current capability, which means more output power, and higher transconductance (g_m) and lower RF noise. So, the BJT is considered better for active circuits such as power amplifier (PA), low noise amplifier (LNA), and gain amplifier (GA) in RFIC systems. On the other hand, CMOS has lower cost and can be used more than BJT for passive or digital circuits such as an attenuator, phase shifter, switch, DC control circuit, etc., since CMOS has lower static power dissipation without DC current at gate, and higher yield capability (passive-type circuits usually needs bigger transistor size.)

1.2 RFIC Phased-Array System

The first phased-array systems were proposed in the 1950's [1-1]. Since then, they have broadly used in radar and communication applications due to their high directivity, beam-tailoring/steering ability, fast beam scanning/tracking response, etc. [1-2, 1-3]. In spite of their attractive properties, they were expensive, and applications had been limited only to high-cost and big-size systems such as airplane radar, military missile warning/tracking, space surveillance, etc. because of the plenty of constituent circuits. In

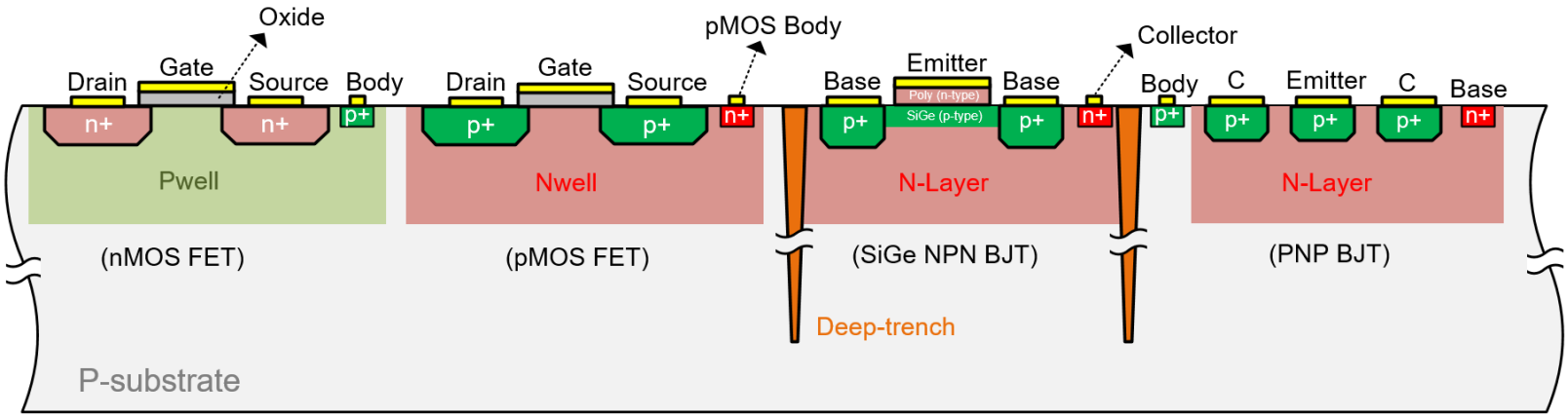


Fig. 1.2. Cross section of SiGe BiCMOS containing nMOS and pMOS FETs, and SiGe NPN and PNP BJTs.

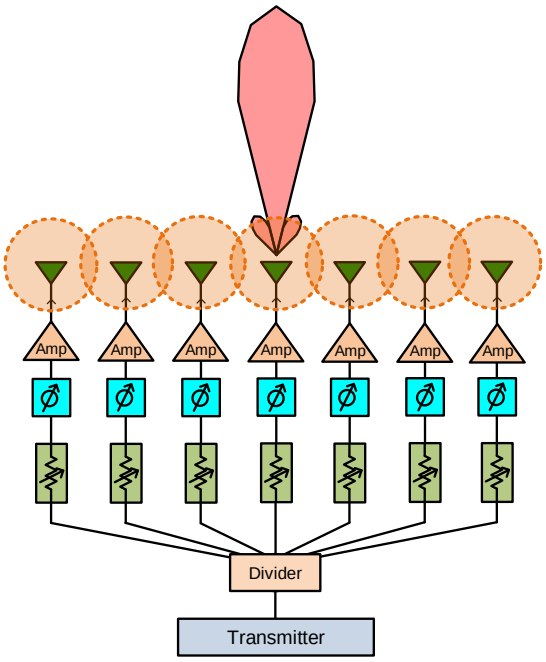


Fig. 1.3. Phased-array transmitter and its high-gain beam.

2007, the first fully integrated phased-array RFIC receiver is demonstrated with a SiGe BiCMOS technology in [1-4] achieving significant reductions in cost, weight and power consumption. It is an appropriate design for the modern economic systems such as radars for human-driven/autonomous cars, personal health monitoring devices and wearable/mobile devices requiring high data-rate communications. There have been researching efforts in the last ten years to realize millimeter-wave phased-array systems in silicon-based RFIC processes for a higher integration (on-chip antenna) and wider bandwidth [5th generation (5G) wireless communication].

The intrinsic transistors in RFIC are not able to handle high power due to low current density, breakdown voltage, and lossy substrate. These drawbacks can be remedied with phased arrays. As shown in Fig. 1.3, the low-gain beams radiated by the single array

antennas are spatially combined on the space building the high-gain array beam. The effective isotropic power (EIRP) of a phased-array system is the sum of the output power, antenna gain and array gain ($EIRP=P_{out}+G_{ant}+G_{Array}$). So, a 7-channel phased-array transmitter has 8.5-dB array gain more than a single antenna transmitter.

1.2.1 Phased-Array Beam Steering with Varying Phases

In phased-array systems, the individual antenna beams at each of the channels construct a high gain beam as mentioned previously. The constructed beam can be steered in the desired direction by varying the phase of the signal at each channel, which is called beam-steering. Fig. 1.4 show the beam direction/range, θ, of a phased-array transmitter which consists of antennas, amplifiers, phase shifters, attenuators, and a divider. The phase shifters are employed to adjust the phase/delay of the signal at each channel, ϕ, for having the high gain beam pointing in the desired direction. For the beam direction in Fig. 1.4, the phases are normally $\phi_1 > \phi_2 > \phi_3 > \phi_4 > \phi_5 > \phi_7 > \phi_7$. The array factors (AF) of the steered beam are plotted in Fig. 1.5, which are calculated with

$$AF = \sum_{n=1}^{N} A_n e^{j(\phi_n + \varepsilon_n)} \ . \tag{1.1}$$

The steering range of the phased-array system is practically limited by the phase shift range of the constituent phase shifters. For example, a 4-bit phase shifter with 22.5º least significant bit (LSB) and 0–337.5º phase shift range is employed at each channel of a 24-GHz 7-channel phased-array system. The maximum phase difference ($\Delta\phi_{max}$) between the channels is chosen as 55º since the total phase difference over the seven

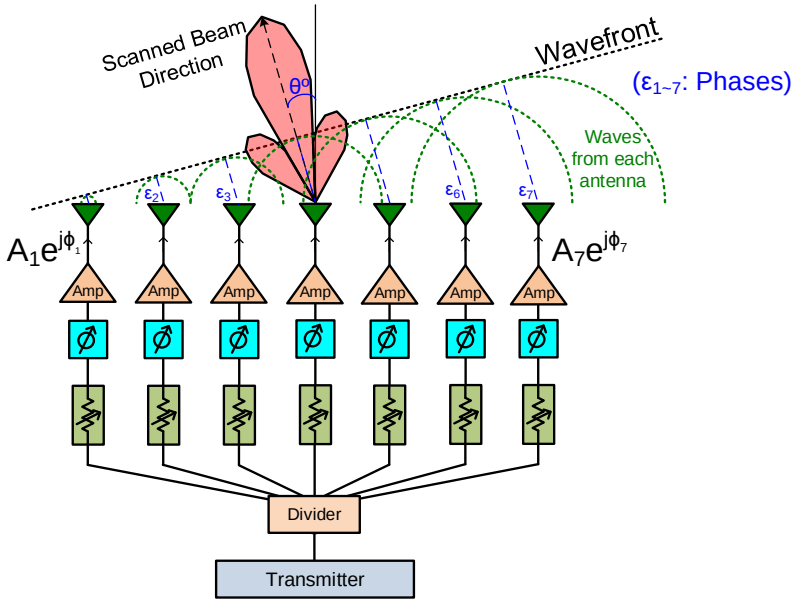


Fig. 1.4. 7-channel phased-array transmitter and beam steering.

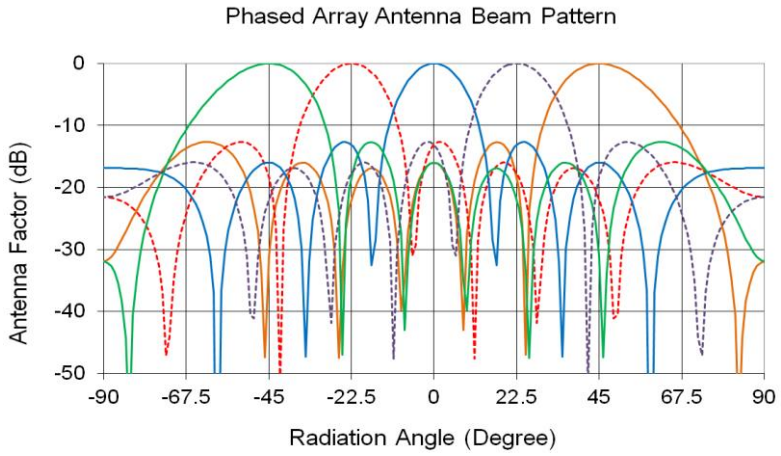


Fig. 1.5. Antenna factor of the steered beam with the varied phases, $\phi_{1\sim7}$.

channels should be smaller than the maximum phase shift ($55^{o} \times 6 = 330^{o} < 337.5^{o}$) as shown in Fig. 1.6. If the spacing between the array antennas (d) is assumed as 0.44 cm, the steering range (θ), $\pm 26^{o}$, can be calculated with

$$|\theta| = \sin^{-1} \frac{\Delta\phi_{\max} \cdot \lambda}{360 \cdot d}. \quad (1.2)$$

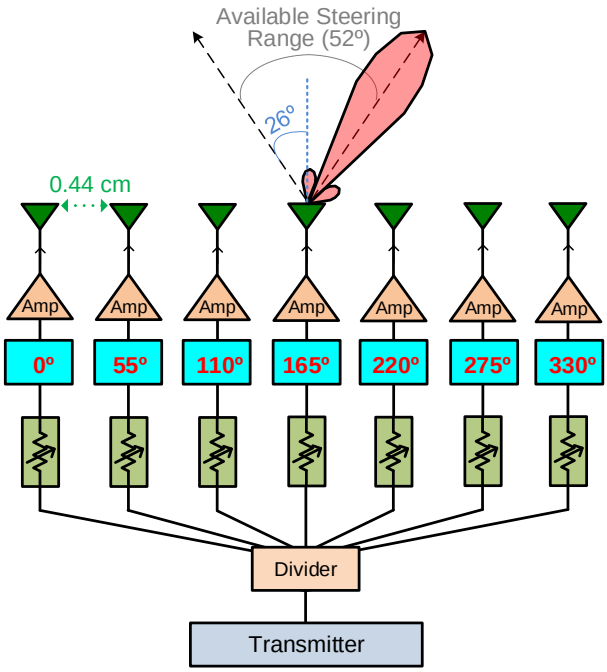
The total steering range calculated is 52º from the left to right direction as shown in Fig. 1.6. The assumption of the 0.44-cm spacing (d) can be verified with the maximum antenna spacing ($d_{\max}$) calculated with

$$d_{\max} = \frac{\lambda}{1+\sin\theta}. \quad (1.3)$$

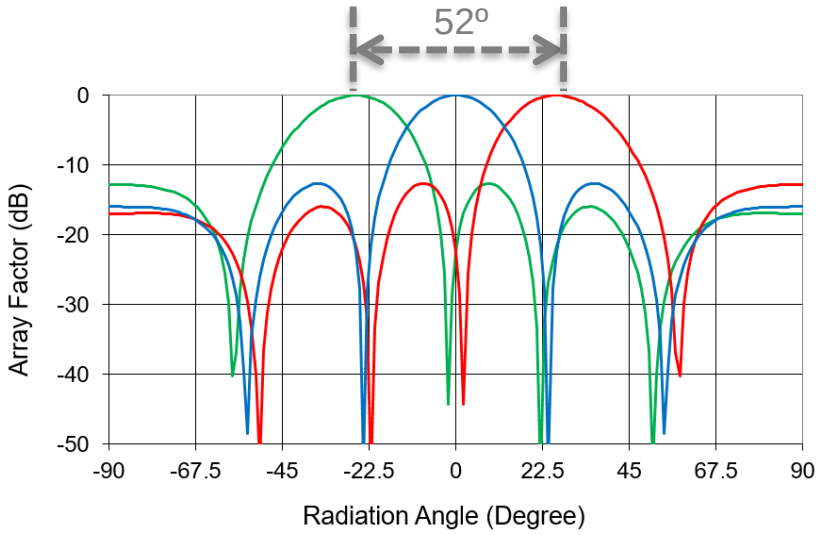
The spacing between antennas should be smaller than $d_{\max}$ in the arrays to facilitate the decent beam combining on space. The 0.44-cm array spacing assumed is acceptable based on the $d_{\max}$ of 0.73 cm calculated. There are several ways to increase the steering range. Firstly, we reduce the antenna spacing or the number of arrays/channels, but the directivity of the beam is degraded. Secondly, we also increase the phase shifting range of the phase shifters, but more phase shifters are needed at the cost of insertion loss and size.

1.2.2 Phased-Array Beam Tailoring with Amplitude Varied

The beam steering function with the phase shifters is introduced in the previous chapter. As another remarkable function of a phased-array system, the high gain beam can be shaped as desired, which is caller beam tailoring. The attenuators in the phased-array transmitter in Fig. 1.7 are used to control the amplitude of the signal at each channel. By changing the amplitude in specific ways, we can reduce the side lobe to a certain degree, which means the interference signal at certain degree can be reduced. Fig. 1.8 shows the reduced side lobes at ±22.5º in red dotted line, which are calculated with the varying amplitudes, A_1=1.3, A_2=0.8, A_3=1.6, A_4=1.6, A_5=0.8, A_6=0.4, and A_7=0.5.



(a)



(b)

Fig. 1.6. (a) Phase shifting and array antenna spacing of the 24-GHz 7-channel phased-array transmitter for the 26º steering direction, and (b) its array factors showing 52º steering range.

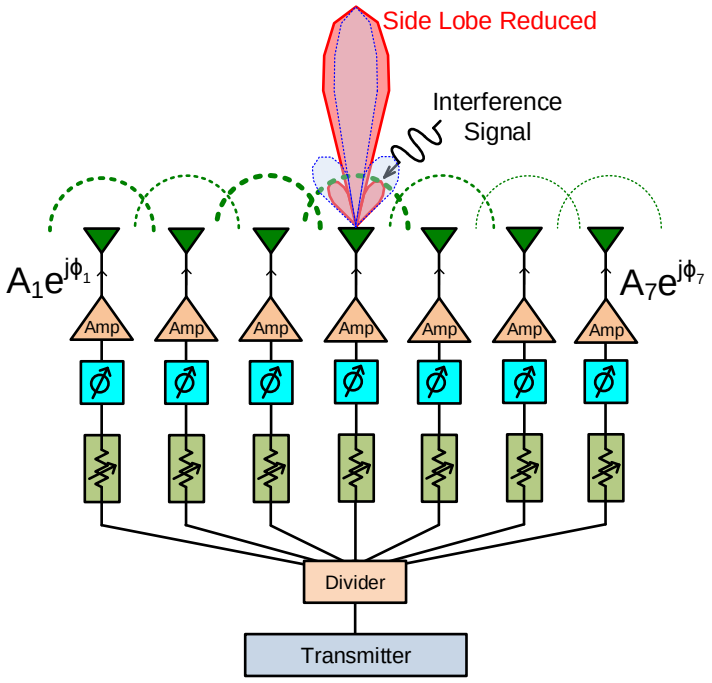


Fig. 1.7. 7-channel phased-array transmitter with beam tailored.

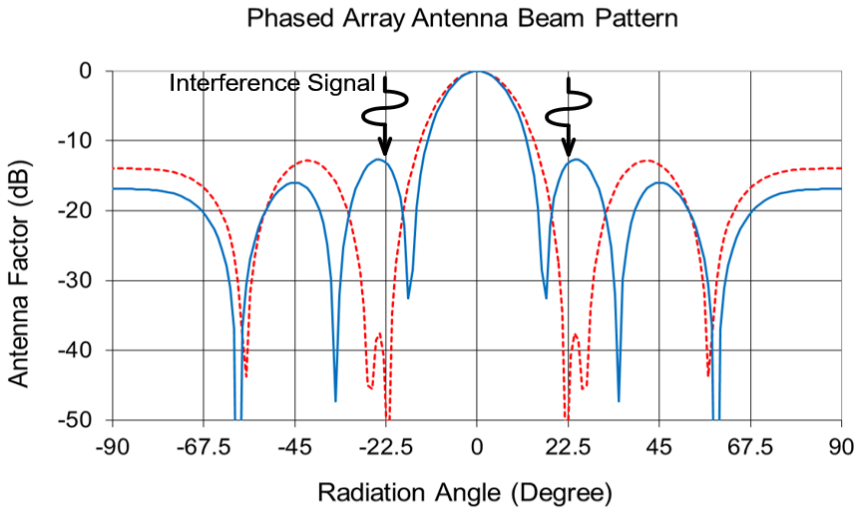


Fig. 1.8. Antenna factor of the tailored beam with varied amplitudes, $A_{1\sim7}$.

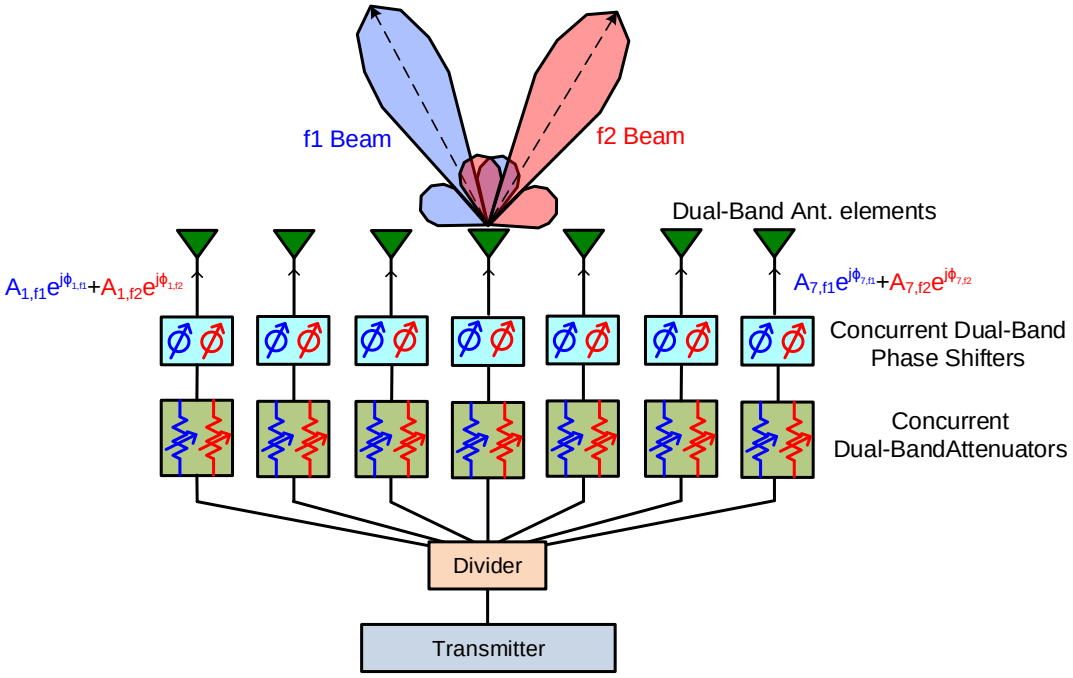


Fig. 1.9. 7-channel concurrent dual-band phased-array transmitter with dual independent beams.

1.2.3 Concurrent Dual-Band Phased-Array System

Dual-band communication and radar systems, particularly those that can work in different bands at the same time, have become attractive in addressing increasing demands of military and industry applications. Accordingly, phased-array systems working concurrently over multiple bands are needed to push the wireless communications and sensing to the next level with its numerous advantages. Concurrent dual-band phased-array systems bring the inherent strengths of phased arrays, such as high directivity, beam-tailoring/steering ability, fast beam scanning/tracking response, etc., in different bands together into a single system. Consequently, dual-band phased-array systems are capable of forming and steering multiple electronic beams in different frequency bands

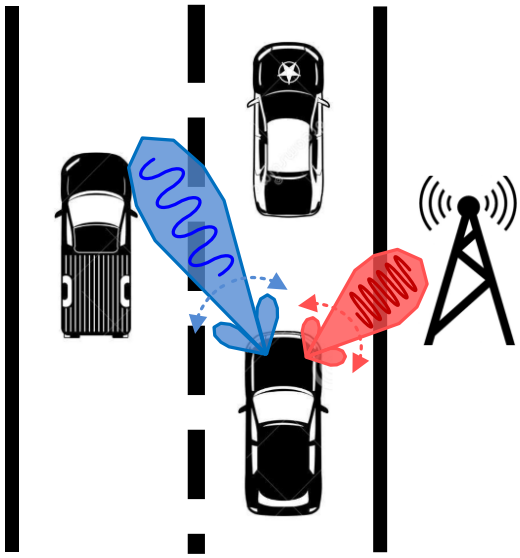


Fig. 1.10. Concurrent dual-band phased-array automotive radar with independent beams.

simultaneously, which significantly improve the systems' diversity, ability, reliability, and performance. The higher frequencies of a dual-band system enable a high-data-rate communication and a high-detection-sensitivity radar, but at the cost of increased noise and propagation loss. On the other hand, the lower frequencies minimize noise and propagation loss. Fig. 1.9 shows the concurrent dual-band phased-array transmitter for f_1 and f_2 frequencies. The single constituent components, concurrent dual-band phase shifters and attenuators, are able to operate at the dual bands individually without interference in another band, which enable the control of the dual array beams. The dual-band phased-array transmitter/receiver can be employed in various systems such as an automotive radar enabling dual-target tracking, dual-point communication, simultaneous tracking/sensing, etc, as shown in Fig. 1.10.

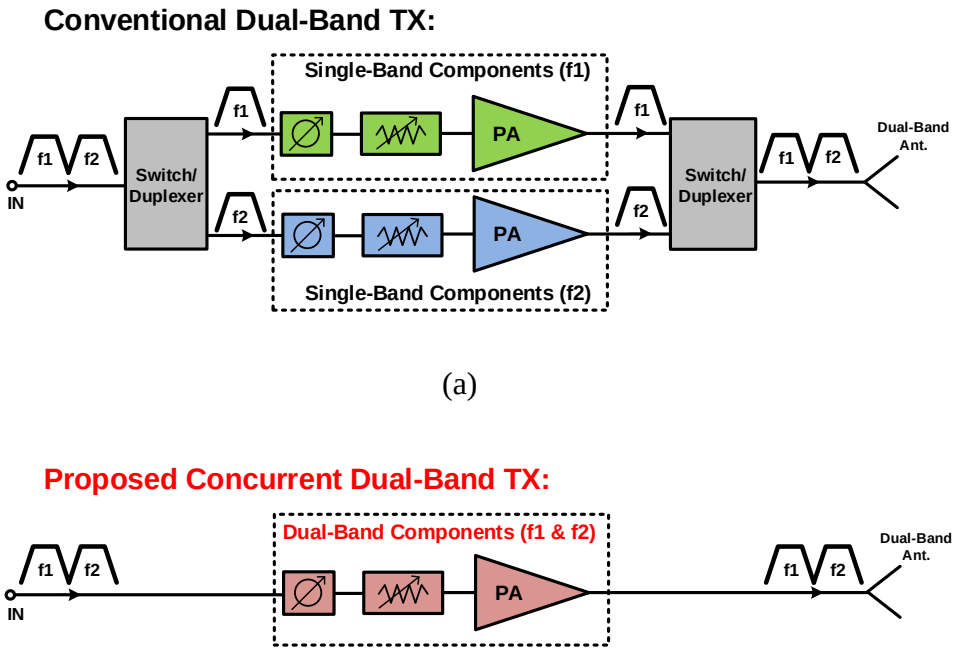


Fig. 1.11. (a) Conventional and (b) proposed concurrent dual-band transmitter.

Conventionally, the concurrent dual-band transmitters are designed with two separate paths with switches or duplexers as shown in Fig. 1.11(a). We propose the transmitter shown in Fig. 1.11(b) to reduce the number of components, loss, power consumption, size, and cost. The proposed concurrent dual-band transmitter consists of the concurrent dual-band constituent components, which would have more linearity issues compared to the single-band components because the dual frequencies are simultaneously processed. This approach is more challenging but deserves significant attention, as it enables fully integrated dual-band transceiver in a single unit, bringing more cost-effective and better-performance systems to both military and commercial sectors.

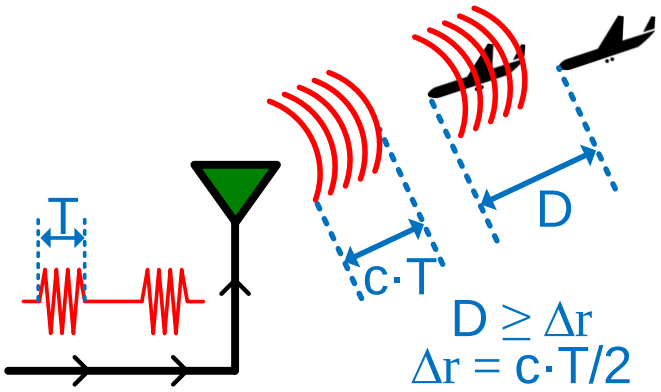


Fig. 1.12. Radar range resolution (Δr) to discriminate the objects close to each other.

1.3 Frequency Band Planning

For our phased-array design, two unlicensed bands of 22–29 and 57–64 GHz are chosen. The high frequencies enable a compact design of the phased-array system. Also, for radar application, it can have broad bandwidth, which leads to high data rate and low range resolution (Δr) based on

$$FBW = \frac{f_2 - f_1}{f_C} \tag{1.4}$$

and

$$\Delta r = \frac{c \cdot T}{2} = \frac{c}{2 \cdot BW}. \tag{1.5}$$

Fig. 1.12 shows why a low range resolution is needed for the radar system. The low range resolution enables us to discriminate the objects located closely apart. On the other hand, the high frequencies degrade the radar detection range (R_{max}),

$$R_{\max} = \sqrt[4]{\frac{P_t G^2 c^2 \sigma}{f_0^2 (4\pi)^3 P_{\min}}} \tag{1.6}$$

, but it can be compensated with the array structure. The high-frequency design also increases the gain of the beam, which is good for discriminating multiple targets in radar. The correlation between the gain of beam and operating frequency is expressed as

$$G = \frac{4\pi A_e f_0^2}{c^2}. \tag{1.7}$$

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CHAPTER II

CONCURRENT DUAL-BAND PHASED-ARRAY TRANSCEIVER

2.1 24/60-GHz Concurrent Dual-Band Phased-Array Transceiver/Transmitter

Fig. 2.1 shows an n-channel concurrent dual-band phased-array transceiver, which consists of power amplifiers (PAs), low noise amplifiers (LNAs), gain amplifiers (GAs), attenuators, phase shifters, switches, and a divider/combiner. The constituent components are designed for the concurrent dual-band frequency response at 24 and 60 GHz, which enable the concurrent dual-beam operation as mentioned in Sec. 1.2.3. The transmitting part of the transceiver is shown in Fig. 2.2. The constituent components in the transmitter have been studied in this dissertation. The sequent chapters show how the components are designed and developed. The input/output power, gain, and insertion loss (IL) are estimated as shown in Fig. 2.2, which are used to decide the specifications of the components. The output powers entering into antenna are 12 and 0 dBm at 24 and 60 GHz, respectively, assuming 0-dBm input power. The output power is too small to use the transmitter for mid-range radar and communications. So, if we use 8-channel array (9-dB array gain) and assume the single-antenna gain is 12 and 8 dB at 24 and 60 GHz respectively, the EIRPs are increased to 33 and 17 dBm at 24 and 60 GHz, respectively. Assuming RCS (radar cross section, σ) is 4 m^2 and minimum power (P_{min}) is -60 dBm for both frequencies, the radar detection range is calculated with (1.4) as 7 and 2 meters at 24 and 60 GHz, respectively. The range can be easily increased with more transmitting RF

power and/or by extending the number of arrays using more RFIC chip sets, which do not cost much.

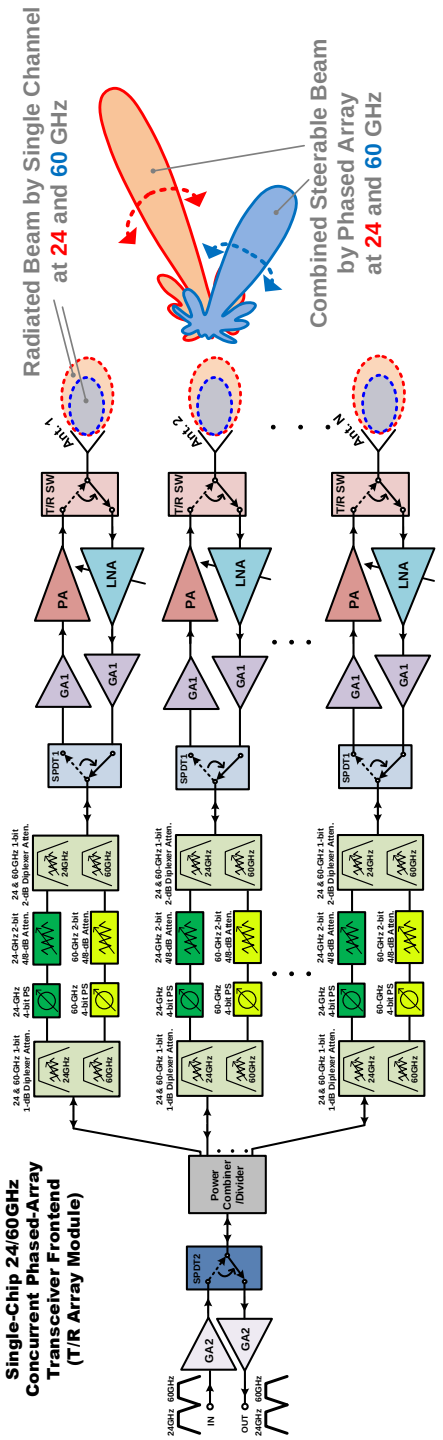


Fig. 2.1. 24/60-GHz concurrent dual-band phased-array transceiver.

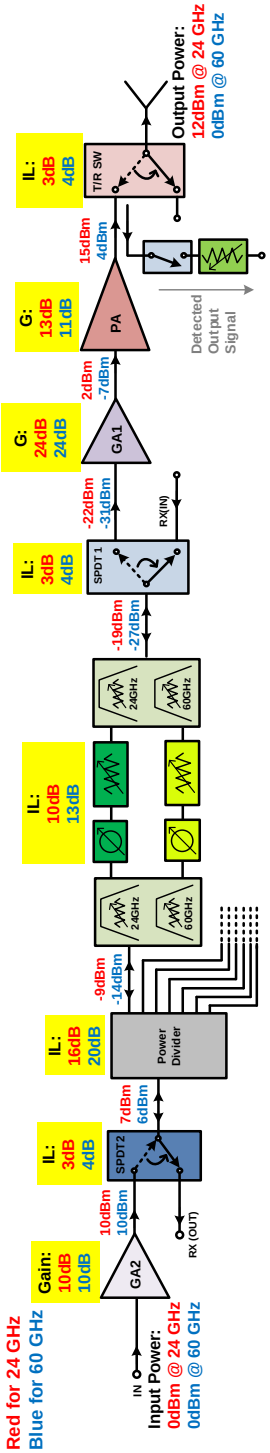


Fig. 2.2. 24/60-GHz concurrent dual-band phased-array transmitter and its estimated input/output power.

CHAPTER III

CONCURRENT 22–29/57–64-GHZ DUAL-BAND CMOS STEP ATTENUATOR WITH LOW PHASE VARIATIONS*

Concurrent dual-band phased-array systems bring the inherent strengths of phased arrays, such as high directivity, beam-tailoring/steering ability, fast beam scanning/tracking response, etc. [3-1], [3-2], in different bands together into a single system. Consequently, dual-band phased-array systems are capable of forming and steering multiple electronic beams in different frequency bands simultaneously, which significantly improve the systems' diversity, ability and performance.

Amplitude-controllable circuits, which play a key role in tailoring beam patterns and side-lobe levels, are important components in phased-array systems. For amplitude control, step attenuators are preferable to variable gain amplifiers and analog attenuators in terms of power consumption, linearity, temperature dependency, control complexity, and phase variation. However, typical step attenuators have relatively large circuit size and high insertion loss, causing possible shortcomings for implementation in phased arrays. These problems are particularly troublesome for phased arrays employing silicon-based CMOS/BiCMOS radio frequency integrated circuits (RFICs) whose real estate is expensive and insertion loss is relatively high due to lossy silicon substrates. Therefore,

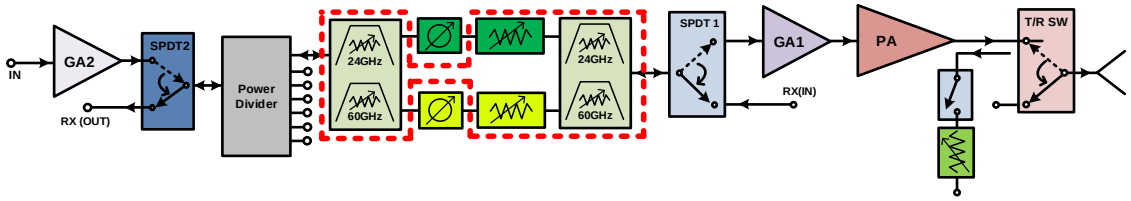


Fig. 3.1. Concurrenut dual-band attenuator in the phased-array transmitter (in the dotted boxes)

design techniques to reduce the size and loss of step attenuators are needed, especially for RFIC design. The need of these techniques is more pronounced in multi-band step attenuators since multi-band attenuators typically have a larger size and higher insertion loss compared to their single-band counterparts due to the possible use of separate single-band attenuators and associated multiplexers. Attenuators are also required to have less transmission-phase variation during the amplitude control to minimize the interference in the phase shifter operation in the phased-array system. This helps avoid steering/tracking error and additional calibration process for the system. Various single-band step attenuators with low phase variations have been developed, e.g. [3-3], [3-4], [3-5].

This paper presents a novel 4-bit step attenuator that can work concurrently in two unlicensed bands of 22–29 and 57–64 GHz with low phase variations. It is fabricated on CMOS using a 0.18-μm BiCMOS technology. New dual-function band-pass attenuator having both attenuating and band-pass filtering and integrated diplexer-attenuator with dual-function of diplexer and attenuation, which constitute the concurrent 22–29 and 57–64 GHz dual-band attenuator, is proposed along with their design formulas. The proposed dual-band attenuator is capable of controlling the amplitudes of signals operating at different frequency bands independently and simultaneously, enabling concurrent tailor

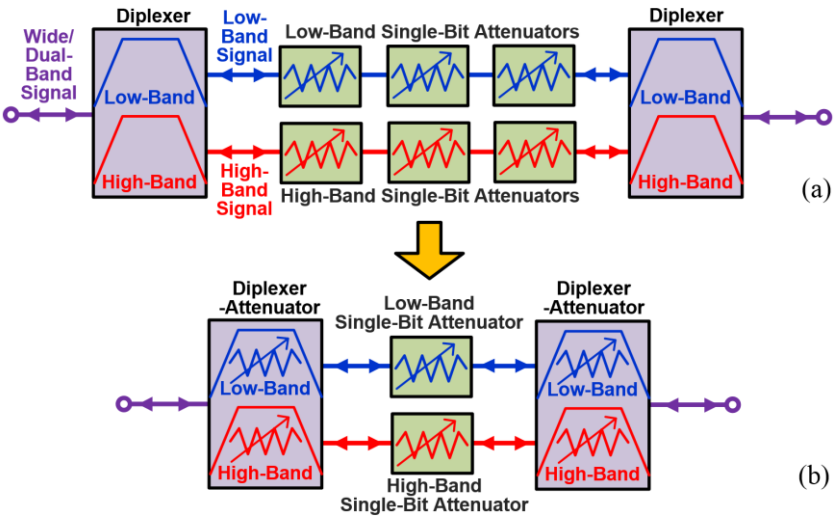


Fig. 3.2. (a) Conventional concurrent dual-band attenuator realized with separate diplexers and attenuators. (b) Proposed concurrent dual-band attenuator implementing attenuators and integrated diplexer-attenuators having dual functions of diplexer and attenuation.

of dual electronic beams independently without any significant effects on each other's beam shapes and phase errors. A new distributed attenuator with minimum phase variation, which is part of the concurrent 22–29 and 57–64 GHz dual-band attenuator, is also proposed.

The designed concurrent dual-band attenuator is employed for the phased-array transmitter as shown in the dotted box in Fig. 3.1.

3.1 Concurrent Dual-Band and Low-Phase-Variation Attenuators

A conventional approach to design concurrent dual-band attenuators is shown in Fig. 3.2(a). It consists of two branches of separate diplexers and single-bit attenuators, each designed in a single band, and operates as follows. A wide or dual-band signal injected through the input of the first diplexer splits into the low- and high-band signal

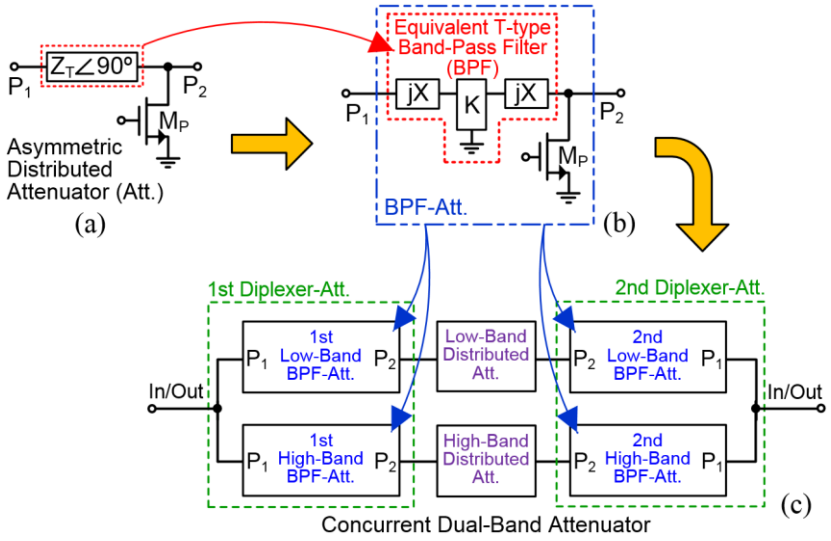


Fig. 3.3. Design process of the proposed concurrent dual-band attenuator.

paths; the amplitudes of these separate signals are then controlled by the low- and high-band attenuators, respectively; and finally these signals are combined by the subsequent diplexer, yielding a concurrent dual-band output signal having controlled amplitude. The attenuator is bidirectional and can be used in both receive and transmit paths in systems. As can be seen, this approach results in large size and high insertion loss. To overcome these problems, we propose a new concurrent dual-band attenuator as shown in Fig. 3.2(b). The proposed attenuator employs integrated diplexer-attenuators having dual-function of diplexer and attenuation, hence enabling a reduction in the overall circuit size and insertion loss.

Fig. 3.3 illustrates the design process of the proposed concurrent dual-band attenuator showing how the concept is realized. The design starts with an asymmetric distributed attenuator consisting of a $\lambda/4$ transmission line and a shunt transistor M_P as shown in Fig. 3.3(a). The $\lambda/4$ transmission line is replaced with a T-type equivalent

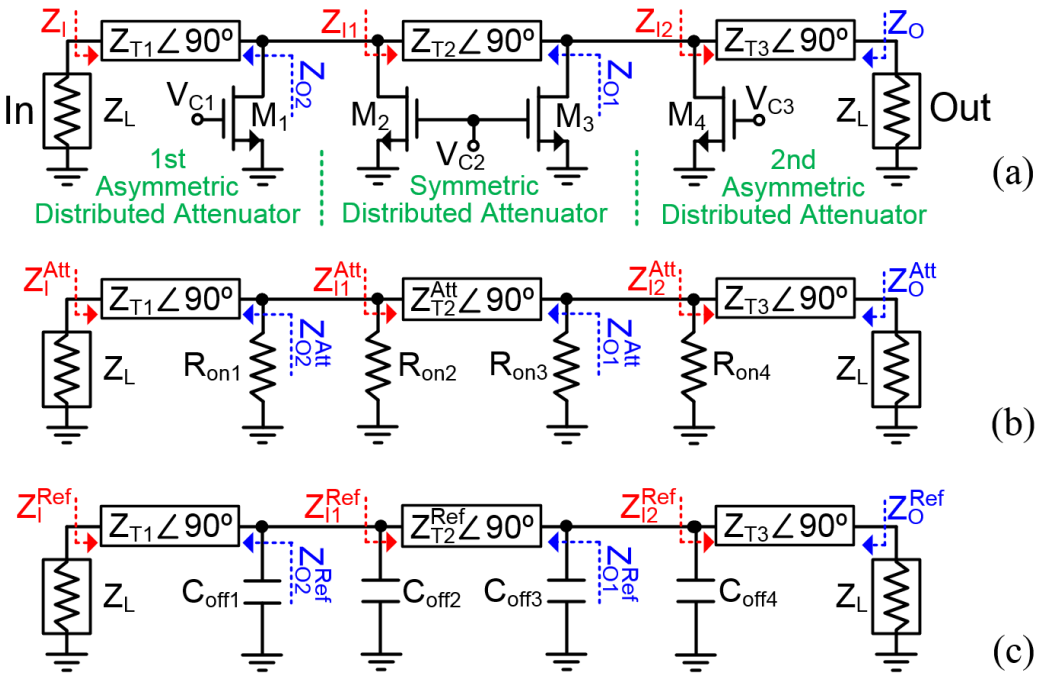


Fig. 3.4. Core attenuator of the concurrent dual-band attenuator: topology (a) and equivalent circuits at maximum attenuation state (b) and reference state (c).

network configured to behave as a band-pass filter (BPF) to produce a BPF-attenuator as shown in Fig. 3.3(b), which will be discussed in Sec. II.B. Two BPF-attenuators are then designed to cover the low and high-frequency bands of interest. They constitute the integrated diplexer-attenuators as shown in Fig. 3.3(c). These diplexer-attenuators are finally combined with the low- and high-band distributed attenuators to form the concurrent dual-band attenuator in Fig. 3.3(c). The low- and high-band distributed attenuators are employed for both impedance transformation and additional attenuation bits, which will be discussed in details in Sec. II.A. It is noted that the asymmetric structure and T-type BPF, instead of a conventional symmetric attenuator and a Pi-type BPF, are chosen for the BPF-attenuator in Fig. 3.3(b) to avoid possible problems of deviation from

the desired performance. A conventional symmetric attenuator and a Pi-type BPF contain a shunt transistor and shunt passive elements (inductor and capacitor) at their input terminals (P_1 in Fig. 3.3(b)), respectively [3-6], which cause deviations from the designed attenuation and frequency response when combined at the input of the diplexer-attenuator.

3.1.1 Core Attenuator Topology

Each path of the new concurrent dual-band attenuator in Figs. 3.2(b) and 3.3(c) constitutes its "core" attenuator. Fig. 3.4 shows the core attenuator, which consists of two asymmetric distributed attenuators and a symmetric distributed attenuator as mentioned earlier. The shunt nMOS transistors of the core attenuator are digitally controlled and are represented by the on-resistance or off-capacitance in the on or off state, respectively. Specific topologies of the low- and high-band BPF-attenuators of the asymmetric distributed attenuators that produce the dual-function low- and high-band band-pass filtering-attenuation characteristics will be presented in Sec. II.B, while that of the symmetric distributed attenuator having low phase variation will be discussed in Sec. II.C. At the maximum attenuation state where all transistors are on as shown in Fig. 3.4(b), the characteristic impedance of the $\lambda/4$ transmission line Z_{T1} and the on-resistance R_{on1} in the 1st asymmetric distributed attenuator can be derived based on its *ABCD*-parameters as

$$Z_{T1}=\sqrt{\frac{Z_L^2 R_{on1}}{Z_L+R_{on1}}} \tag{3.1}$$

$$R_{on1}=\frac{Z_L 10^{-A_1/10}}{1-10^{-A_1/10}} \tag{3.2}$$

where A_1 denotes the attenuation of the 1st asymmetric distributed attenuator in dB, Z_L represents the termination impedance at the input and output of the attenuator, and $Z_I^{Att}=Z_{I1}^{Att}=Z_L$ is assumed for the input matching. Similarly, the design formulas for the 2nd asymmetric attenuator are derived as

$$Z_{T3}=\sqrt{\frac{Z_L^2 R_{on4}}{Z_L+R_{on4}}} \tag{3.3}$$

$$R_{on4}=\frac{Z_L 10^{-A_3/10}}{1-10^{-A_3/10}}\,. \tag{3.4}$$

The asymmetric distributed attenuators have $Z_{O2}^{Att}\neq Z_L$, $Z_{I2}^{Att}\neq Z_L$ and $Z_{O2}^{Att}\neq Z_{I2}^{Att}$ at the maximum attenuation state, necessitating an impedance transformer between the asymmetric attenuators for the input and output matching. The symmetric distributed attenuator provides such impedance transformation as well as enables increased total attenuation bit and range. The symmetric distributed attenuator can be designed based on Z_{O2}^{Att} and Z_{I2}^{Att} expressed as

$$Z_{O2}^{Att}=\frac{R_{on1}Z_{T1}^2}{R_{on1}Z_L+Z_{T1}^2} \tag{3.5}$$

$$Z_{I2}^{Att}=\frac{R_{on4}Z_{T3}^2}{R_{on4}Z_L+Z_{T3}^2}\,. \tag{3.6}$$

By assuming $Z_{I1}^{Att}=Z_L$ and $Z_{O1}^{Att}=Z_L$, the on-resistances R_{on2} and R_{on3} of the transistors M_2 and M_3 can be derived as

$$R_{on2}=\frac{R_{on3}Z_L+(T+1)Z_L Z_{I2}^{Att}}{R_{on3}+Z_{I2}^{Att}} \tag{3.7}$$

$$R_{on3}=\frac{R_{on2}Z_L+(T+1)Z_L Z_{O2}^{Att}}{R_{on2}+Z_{O2}^{Att}} \tag{3.8}$$

where $T=(4\times10^{A_2/10})/(10^{A_2/10}-1)^2$ with A_2 denoting the attenuation of the symmetric distributed attenuator in dB. Substituting R_{on3} from (3.8) into (3.7) gives

$$R_{on2}^2(Z_L+Z_{I2}^{Att})+R_{on2}\{(T+1)(Z_{O2}^{Att}-Z_{I2}^{Att})Z_L+Z_{I2}^{Att}Z_{O2}^{Att}-Z_L^2\}-(T+1)(Z_L+Z_{I2}^{Att})Z_LZ_{O2}^{Att}=0 \quad (3.9)$$

from which R_{on2} can be calculated and then used for determining R_{on3} from (3.8). The characteristic impedance Z_{T2}^{Att} is expressed, using the design formulas of conventional distributed attenuator in [3-7], as

$$Z_{T2}^{Att}=\frac{(10^{A_2/10}-1)}{2}\sqrt{\frac{R_{on2}R_{on3}}{10^{A/10}}}. \quad (3.10)$$

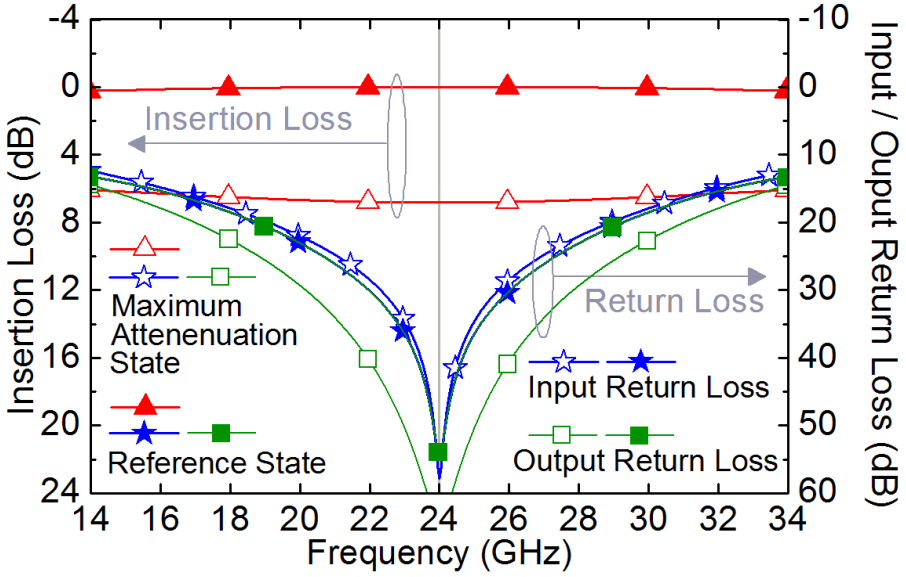
These derived formulas allow the values of the elements for the maximum attenuation state shown in Fig. 3.4(b) to be calculated.

For the reference state of the core attenuator where all transistors are turned off as shown in Fig. 3.4(c), the characteristic impedance of the second transmission line Z_{T2}^{Ref} is derived as

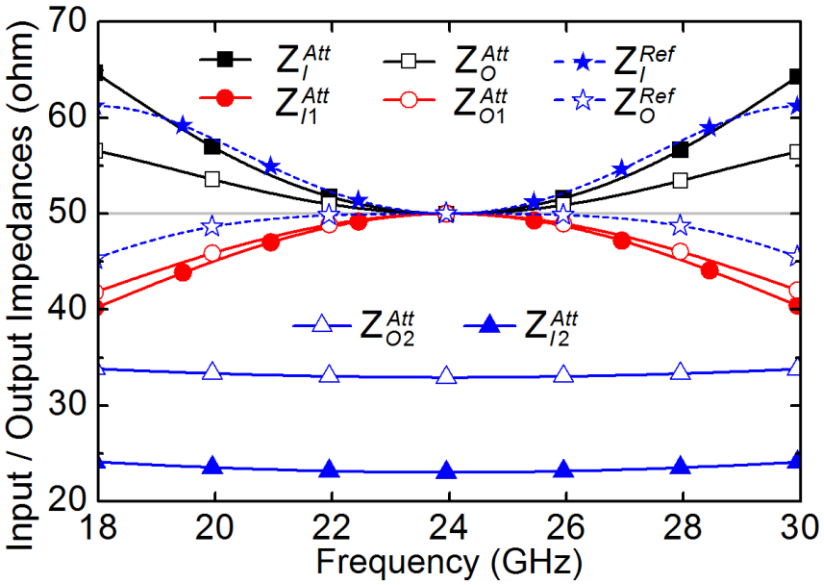
$$Z_{T2}^{Ref}=\frac{Z_{T1}Z_{T3}}{Z_L} \quad (3.11)$$

assuming $Z_I^{Ref}=Z_L$ or $Z_O^{Ref}=Z_L$for the input and output matching and the shunt transistors M_1–M_4 have ideal off-switching conditions with the off-capacitances C_{off1}–C_{off4} ignored.

To verify the design formulas derived for the core attenuator in Fig. 3.4(a), a 7-dB step attenuator, which consists of 1-and 2-dB asymmetric distributed attenuators and 4-dB symmetric distributed attenuator, is designed. The elements' values at the maximum attenuation state are calculated with (3.1)–(3.4) and (3.8)–(3.10), while (3.1), (3.3) and (3.11) are used for the reference state. Also, the center frequency of 24 GHz and input and



(a)



(b)

Fig. 3.5. Simulated (a) insertion and input/output return losses, and (b) constituent attenuators' input/output impedances of the 7-dB step attenuator at the maximum attenuation and reference states.

output load impedance of 50 Ω are employed for the design. Consequently, it yields

R_{on1}=193.1 Ω, R_{on2} = 88.1 Ω, R_{on3} = 109.8 Ω, R_{on4} = 85.5 Ω, Z_{T1} = 44.5 Ω, Z_{T3} = 39.7 Ω, Z_{T2}^{Att}

= 46.9 Ω and Z_{T2}^{Ref} = 35.4 Ω. The simulations of the designed 7-dB step attenuator at the maximum attenuation and reference states are shown in Fig. 3.5. The 0-dB insertion loss, 7-dB attenuation and well-matched input and output at the center frequency, 24 GHz, are confirmed in Fig. 3.5(a) as designed. Also, $Z_I^{Att}=Z_{I1}^{Att}=Z_O^{Att}=Z_{O1}^{Att}=Z_I^{Ref}=Z_O^{Ref}$ =50 Ω, Z_{I2}^{Att} =23 Ω and Z_{O2}^{Att}=33 Ω at 24 GHz are shown in Fig. 3.5(b), verifying the derived formulas. The above results show that, in practical designs, the characteristic impedances of the $\lambda/4$ lines and the sizes of the shunt transistors in the core attenuator can be determined based on the derived formulas. Particularly, an optimum value for the characteristic impedance of the second transmission line Z_{T2} is found from (3.10) and (3.11) considering acceptable attenuations and matching conditions at both attenuation and reference states.

It is noted that our (single-band) core attenuator implements a single-stage attenuation approach, which results in minimum numbers of transmission lines and shunt transistors. This approach is different from that proposed in [3-4], which employs a multi-stage distributed attenuator.

3.1.2 Integrated Diplexer-Attenuator and Constituent Low- and High-Band Band-Pass-Filter-Attenuators

By configuring the transmission lines in the constituent 1st and 2nd asymmetric distributed attenuators of the core attenuators in Fig. 3.5(a) to behave as BPFs, we can realize the low- and high-band BPF-attenuators, which constitute the integrated diplexer-attenuators as seen in Fig. 3.3(c).

Fig. 3.6 shows the equivalences between transmission lines and 2nd-order BPFs with C-

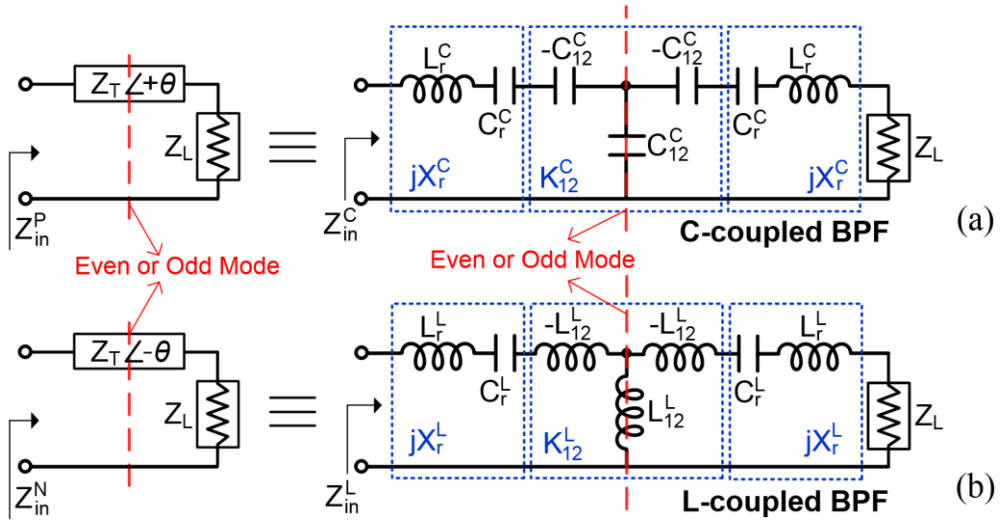


Fig. 3.6. Equivalences between $\pm\theta$ transmission lines and 2nd-order K-inverter BPFs with (a) C-coupled and (b) L-coupled networks.

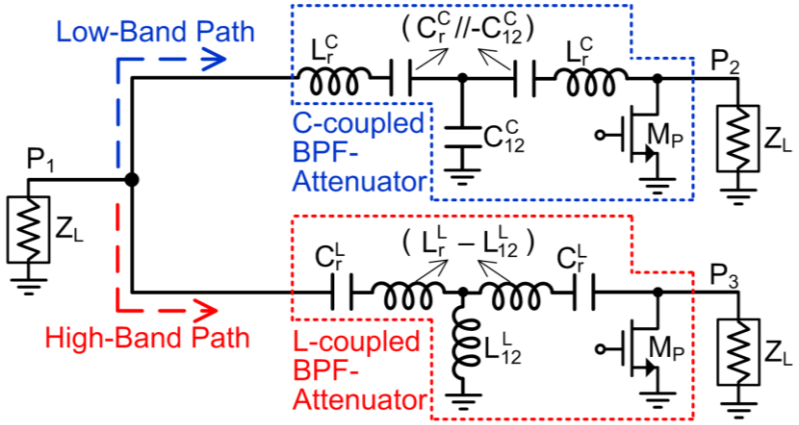


Fig. 3.7. Integrated diplexer-attenuator consisting of the C- and L-coupled BPF-attenuators constituting the low- and high-band BPF-attenuators, respectively.

and L-coupled impedance inverters (K-inverters) terminated with Z_L. The transmission lines with positive ($+\theta$) and negative ($-\theta$) electrical length are equated to the C- and the L-coupled BPFs, respectively, due to the corresponding image phase shift of the C- and

L-coupled networks. The even- and odd-mode correspond to the open and short circuits at the dashed line, respectively. The input impedances of the transmission line and C-coupled BPF in Fig. 3.6(a) for the even- and odd-mode can be expressed as

$$Z_{in\text{-}even}^{P} = -jZ_T \cot\frac{\theta}{2} \tag{3.12}$$

$$Z_{in\text{-}odd}^{P} = jZ_T \tan\frac{\theta}{2} \tag{3.13}$$

$$Z_{in\text{-}even}^{C} = -j\left(\frac{1}{\omega C_r^C} + \frac{1}{\omega C_{12}^C} - \omega L_r^C\right) \tag{3.14}$$

$$Z_{in\text{-}odd}^{C} = j\left(\omega L_r^C - \frac{1}{\omega C_r^C} + \frac{1}{\omega C_{12}^C}\right) \tag{3.15}$$

where Z_T is the characteristic impedance of the transmission line. By equating the corresponding even- and odd-mode input impedances ($Z_{in\text{-}even}^{P}=Z_{in\text{-}even}^{C}$ and $Z_{in\text{-}odd}^{P}=Z_{in\text{-}odd}^{C}$), C_{12}^C is derived as

$$C_{12}^C = \frac{\sin\theta}{Z_T \omega_0} \tag{3.16}$$

where ω_0 is the center frequency of the BPF. Equating Z_{in}^{P} and Z_{in}^{C} yields the impedance of the inverter as

$$K_{12}^C = Z_T \csc\theta \,. \tag{3.17}$$

The series inductance and capacitance in the C-coupled BPF can be obtained, following the low-pass to band-pass mapping [3-8], as

$$L_r^C = \frac{K_{12}^C \sqrt{g_1 g_2}}{\omega_0 W} \tag{3.18}$$

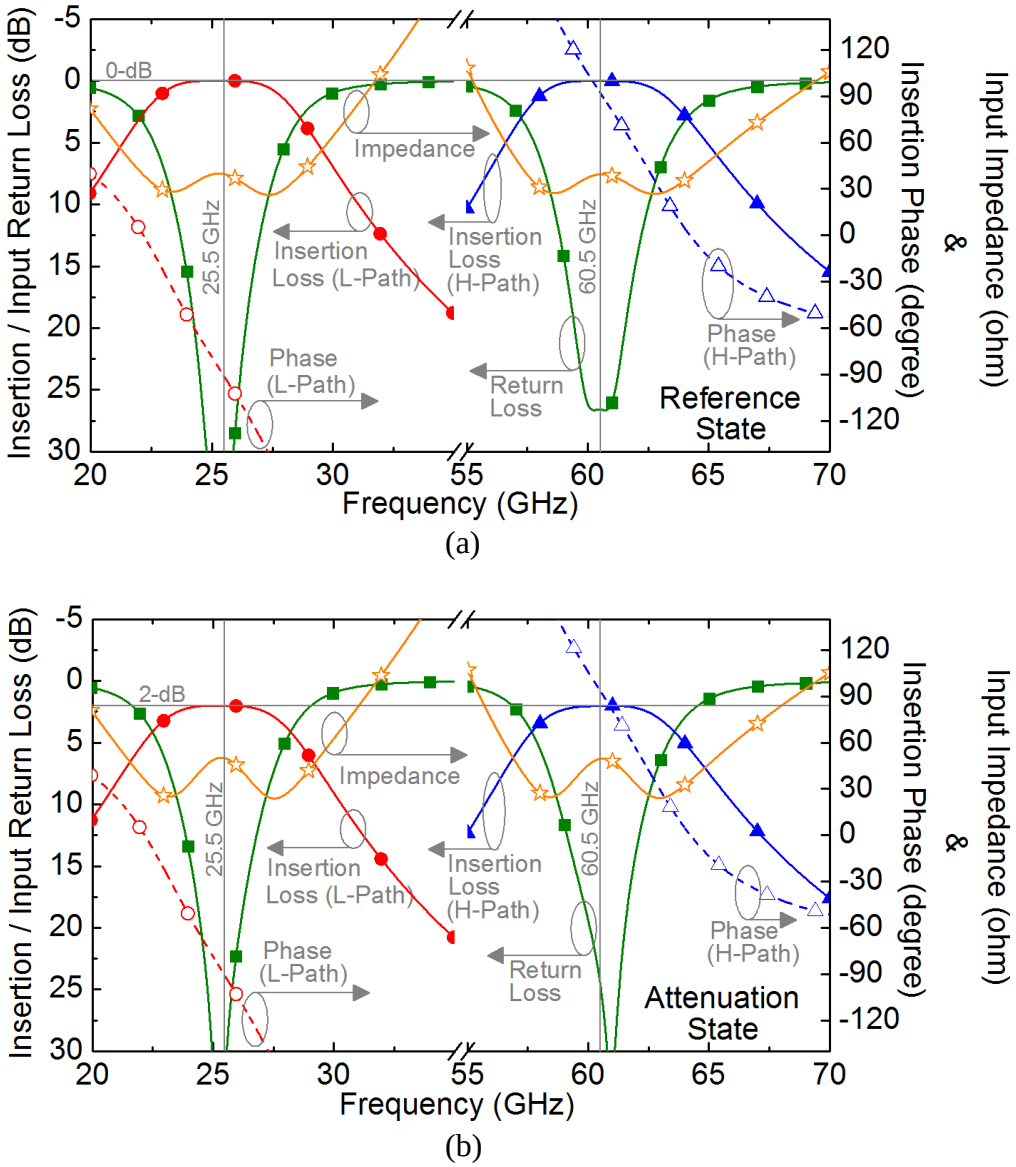


Fig. 3.8. Simulations of the 2-dB integrated diplexer-attenuator at (a) reference and (b) attenuation states. L-path: low-band path and H-path: high-band path.

$$C_r^C = \frac{1}{\omega_0(\omega_0 L_r^C - Z_T \cot\theta)} \tag{3.19}$$

where g_1 and g_2 are the values of the 1st and 2nd elements of the low-pass prototype filter, respectively, $W = (\omega_2 / \omega_0) - (\omega_0 / \omega_2)$, and ω_2 is the upper-pass-band cut-off frequency of

the BPF. Similarly, the equivalent formulas of the L-coupled BPF in Fig. 3.6(b) can also be derived as

$$L_{12}^{L}=\frac{Z_T \csc\theta}{\omega_0} \tag{3.20}$$

$$K_{12}^{L}=K_{12}^{C} \tag{3.21}$$

$$L_r^{L}=L_r^{C} \tag{3.22}$$

$$C_r^{L}=C_r^{C}. \tag{3.23}$$

With these equivalent C-coupled and L-coupled BPFs, the corresponding low- and high-band BPF-attenuators can be designed as shown in the integrated diplexer-attenuator in Fig. 3.7. It is noted that, in the integrated diplexer-attenuator, the equivalent C-coupled and L-coupled BPFs are utilized for the low- and high-band paths, respectively, due to their weighted filter responses toward low-pass (C-coupled BPF) and high-pass (L-coupled BPF).

As an example to verify the formulas derived for the equivalent transmission lines and BPFs, the integrated diplexer-attenuator in Fig. 3.7 is designed for 2-dB attenuation in each path (low- or high-band path). 2nd-order Butterworth filter responses with 22–29 GHz and 57–64 GHz pass-bands are chosen. Eqs. (3.1), (3.2) and (3.16)–(3.19) are used to design the constituent C-coupled-BPF attenuator, while (3.1), (3.2) and (3.20)–(3.23) are used for the L-coupled BPF-attenuator. Consequently, we obtain Z_T = 39.7 Ω, R_{on} = 85.5 Ω, C_{12}^{C} = 157 fF, L_{12}^{L} = 105 pH, C_r^{C} = C_r^{L} = 28.7 fF, and L_r^{C} = L_r^{L} = 1.36 nH. The simulations of the designed integrated diplexer-attenuator at the reference and attenuation states are shown in Figs. 3.8(a) and (b), respectively. For the reference-state simulations,

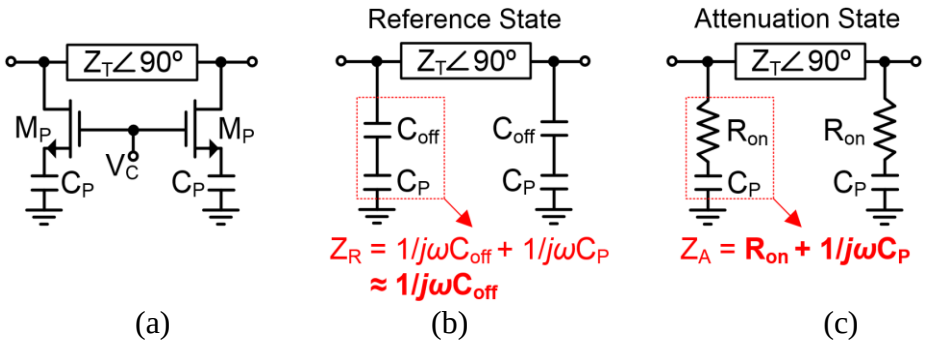


Fig. 3.9. Low-phase-variation attenuator (a) and its equivalent circuits at reference (b) and attenuation (c) states.

the off-capacitances of M_Ps are disregarded. Also, the 39.7- and 50-Ω load impedances are employed for the reference- and attenuation-state simulations, respectively. The simulated results in Figs. 3.8 (a) and (b) show that, at the design frequencies of 25.5 and 60.5 GHz, the integrated diplexer-attenuator has 0-dB insertion loss, 39.7-Ω input impedances and 90° phase delays at the reference state, and 2-dB attenuation and 50-Ω input impedance at the attenuation state, which demonstrate the validity of the derived formulas (3.16)–(3.23).

3.1.3 Low-Phase-Variation Attenuator

The symmetric distributed attenuator of the core attenuator seen in Fig. 3.4(a) is implemented for low phase variation as shown in Fig. 3.9(a), and its equivalent circuits at reference and attenuation states are shown in Figs. 3.9(b) and (c), respectively. For low phase variation, a large capacitor C_P is inserted in series with the transistor M_P. C_P affects the phase delay at the attenuation state while it is negligible at the reference state due to the relatively very small off-capacitance C_{off}. The relations of C_P to C_{off} and R_{on} are

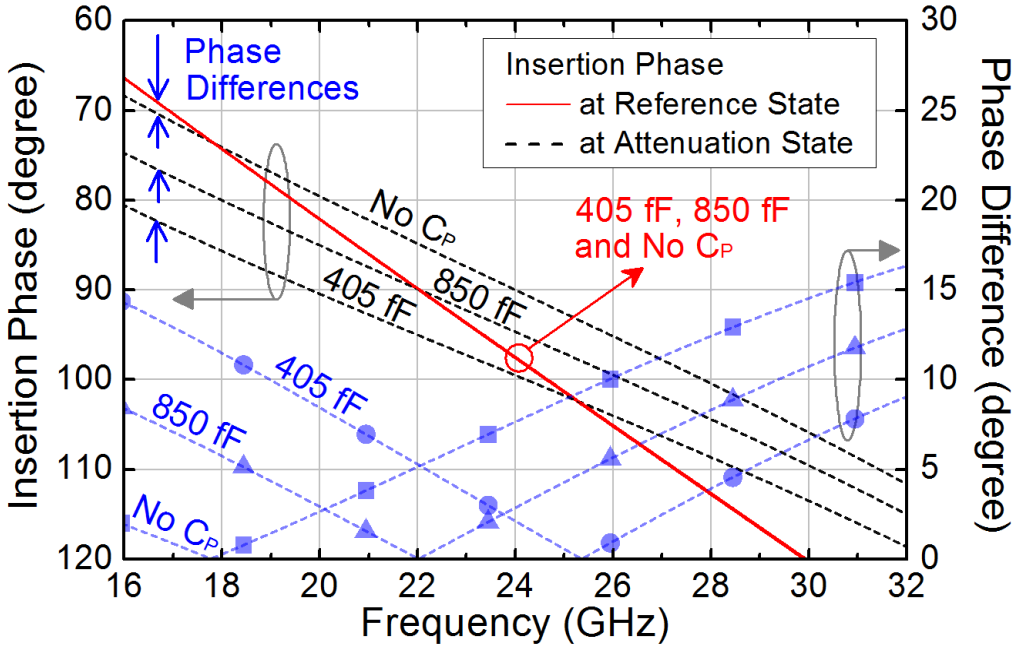


Fig. 3.10. Simulated (a) insertion phase and (b) phase difference of the low-phase-variation attenuator with C_P of 405- and 850-fF and without C_P.

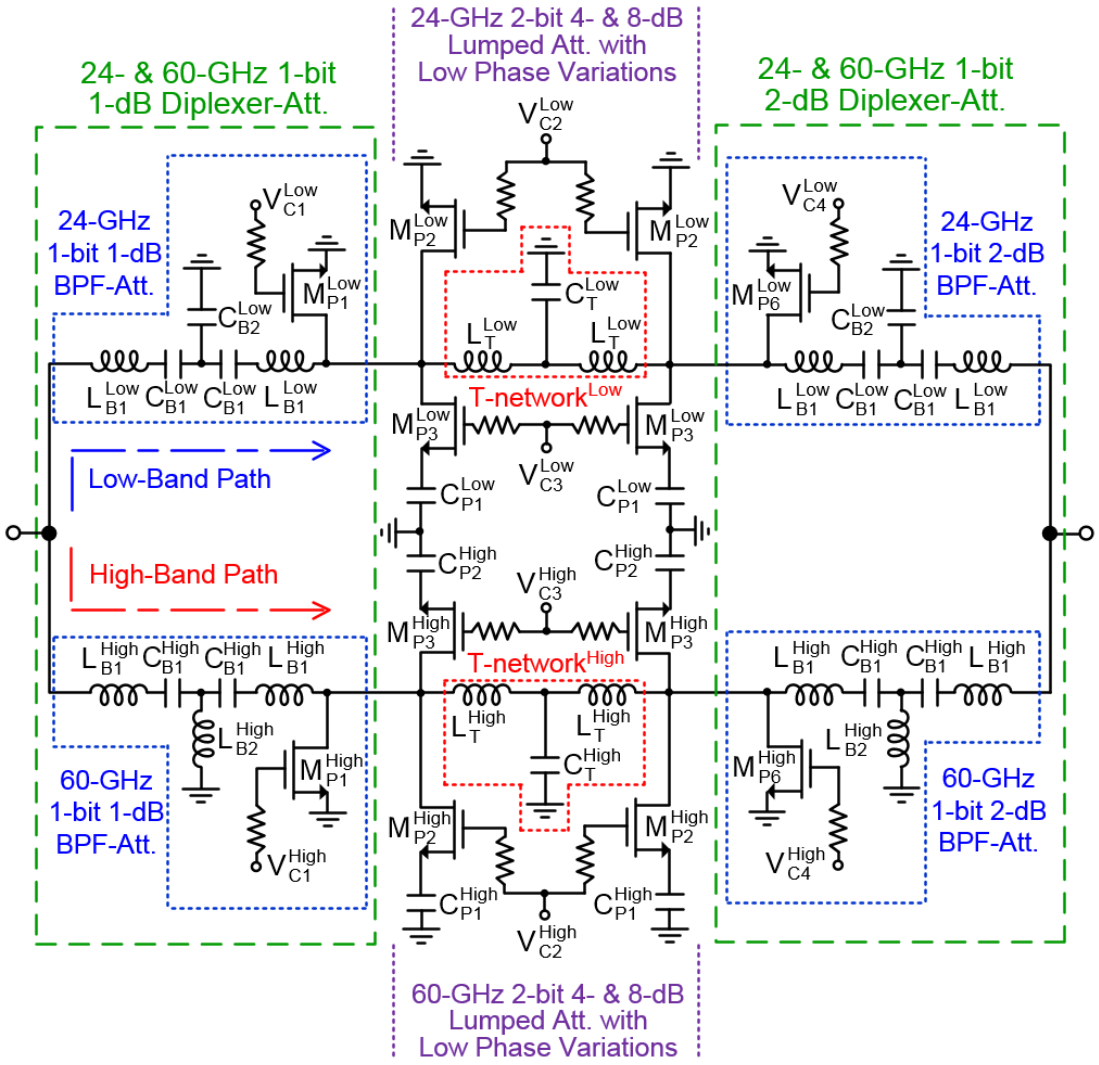
described with the impedance expressions (Z_R and Z_A) in Figs. 3.9(b) and (c), respectively. Hence, the insertion phase at the attenuation state can be adjusted without any significant effect on the phase at the reference state. To verify this design concept, a 24-GHz 8-dB distributed attenuator, which consists of 72.8-Ω shunt resistors and 68.8-Ω transmission line, is designed based on the proposed structure in Fig. 3.9(a). For the design, the shunt nMOS transistor M_P, having 0.18-μm gate-length and 12-μm gate-width, which has approximate 72.8-Ω on-resistance and 13-fF off-capacitance, is employed. Fig. 3.10 shows the simulated insertion phase and phase difference of the designed symmetric distributed attenuator with C_P of 405- or 850-fF or without C_P. The simulations show that the insertion phase at the reference state (solid lines) changes very slightly for different

values of C_P, while that at the attenuation state (dashed lines) decreases significantly with decreasing C_P. Therefore, an optimum phase difference/variation over the desired frequency band can be found by adjusting the value of C_P in the proposed symmetric distributed attenuator. Over 22–29 GHz, the simulations show that the attenuator with 405-fF C_P leads to the lowest phase difference, 0–5.3°, when compared with those, 0–9.5° and 5.1–13.5°, by the attenuator with 850-fF C_P and without C_P, respectively. It also shows that the phase variation can be reduced without any significant size increase by adding the large capacitors on the shunt path. It is noted that a distributed attenuator inherently has lower phase variation during the attenuation control compared to other types of attenuators, such as Pi-, T- and bridged-attenuator reported in [3-3], [3-5] and [3-9], due to the absence of large-size series transistors. This virtue is also reflected in the proposed symmetric distributed attenuator. In [3-4], the phase variation of the multi-stage distributed attenuator is reduced by adding shunt inductors. However, for the single-stage distributed attenuator in Fig. 3.9(a), adding inductors increases the insertion phase, making the phase variation worse. In [3-5], a shunt capacitor is added into a T-type lumped attenuator to offset the impact of the series off-capacitance at the attenuation, resulting in reduced phase variation. This phase-variation reduction is different from our approach utilizing the relations of elements as described earlier.

3.2 Concurrent Dual-Band Attenuator with Low Phase Variations

3.2.1 Design and Fabrication

Fig. 3.11 shows the schematic of the new 4-bit 24/60-GHz step attenuator with concurrent dual pass-bands and low phase variations designed based on the discussions of the concurrent dual-band attenuator and the low-phase-variation attenuator in Sec. II. Fig. 3.11 also includes the sizes of the transistors and values of the inductors and capacitors used in the attenuator. The 4-bit 24/60-GHz concurrent dual-band step attenuator consists of 1-bit 1- and 2-dB integrated diplexer-attenuators and 2-bit 4- and 8-dB low-phase-variation lumped-element attenuators, and can control the amplitude with a 1-dB step over 16 states (4 bit) in each pass-band (22–29 or 57–64 GHz). The integrated diplexer-attenuator, consisting of the low-band 24- and high-band 60-GHz BPF-attenuators, is placed at the input and output for splitting and combining the input and output signals, respectively, which enables independent amplitude control in each pass-band. It is noted that this diplexer-attenuator is different from that designed for the dual-band of 22–29 and 57–64 GHz simulated in Fig. 3.8. In this design, the 2nd pass-band of the attenuator is wider than 57–64 GHz to obtain more practical capacitances and inductances to facilitate realization in the BiCMOS process. This will result in a wider second passband for the concurrent dual-band attenuator as will be seen in the measurement results. The lumped attenuators are initially designed as distributed attenuators mentioned in Sec. II, and then the constituent $\lambda/4$ lines are substituted with the equivalent T-networks as shown in Fig. 3.11 for compactness. The lumped attenuators' sizes are also reduced by sharing the T-networks for the 4- and 8-dB attenuations on both paths. Specifically, as shown on the



Low-Band Path

L_{B1}^{Low}=635 pH C_{B1}^{Low}=109 fF C_{B2}^{Low}=123 fF L_{T}^{Low}=180 pH C_{T}^{Low}=170 fF
M_{P1}^{Low}=2.9 μm × 5 M_{P2}^{Low}=2.9 μm × 5 M_{P3}^{Low}=3.8 μm × 8 M_{P4}^{Low}=3.0 μm × 5 C_{P1}^{Low}=1.2 pF

High-Band Path

L_{B1}^{High}=150 pH C_{B1}^{High}=30 fF L_{B2}^{High}=180 pH L_{T}^{High}=73 pH C_{T}^{High}=40 fF
M_{P1}^{High}=2.5 μm × 4 M_{P2}^{High}=3.1 μm × 4 M_{P3}^{High}=3.4 μm × 8 M_{P4}^{High}=2.6 μm × 4
C_{P1}^{High}=C_{P2}^{High}=160 fF

Fig. 3.11. Schematic of the 4-bit 24/60-GHz concurrent dual-band step attenuator with low phase variations.

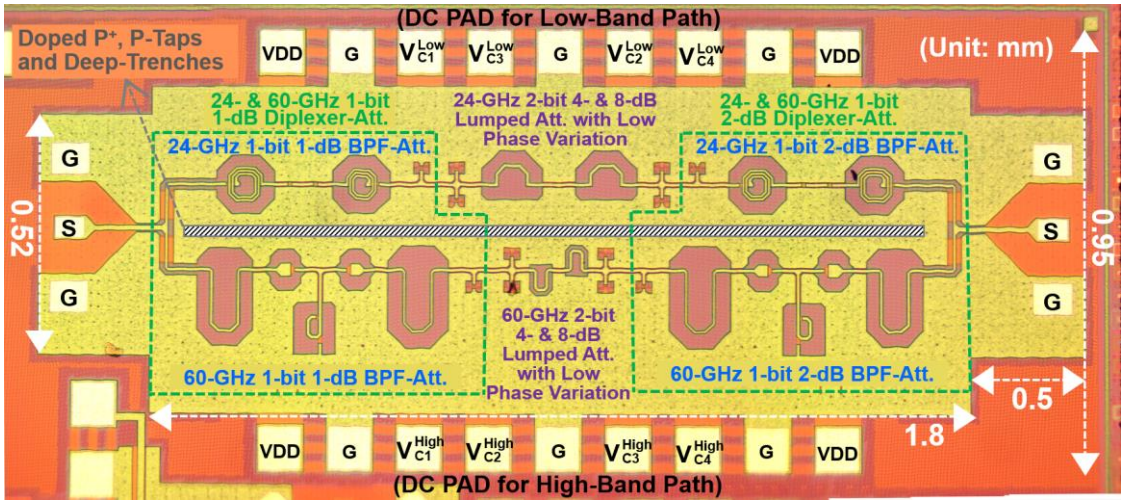


Fig. 3.12. Micrograph of the 4-bit 24/60-GHz concurrent dual-band step attenuator with low phase variations. Chip size (core part): 1.8 × 0.52 mm^2.

low-band path in Fig. 3.11, the shunt transistors for the 4-dB attenuation (M_{P2}^{Low}) and 8-dB attenuation (M_{P3}^{Low}) share the *T-network*^{Low} in the 24-GHz 2-bit lumped attenuator. The 60-GHz 2-bit lumped attenuator on the high-band path is similarly designed. The characteristic impedances of the equivalent $\lambda/4$ lines of the T-networks for the 4- and 8-dB attenuations are calculated with (3.10) as 46.9 and 67 Ω, respectively. For sharing the T-network, the optimum impedances can be found between the calculated values. To achieve low phase variations, the capacitors C_{P1}^{Low}, C_{P1}^{High} and C_{P2}^{High} are inserted into the 8-dB lumped-element attenuator on the low-band path and 4-, 8-dB lumped-element attenuators on the high-band path, respectively. This is necessary since, without C_P, these attenuators lead to relatively high phase variations as compared to the other lower-attenuation attenuators in the concurrent dual-band attenuator. The control voltages (V_{C1}^{Low}–V_{C4}^{Low} and V_{C1}^{High}–V_{C4}^{High}) at the gates of the transistors are digitally controlled with 0 and 1.8 V

Table 3.1 Design parameters of the BPFs and attenuators composing the concurrent dual-band attenuator

		Low-Band Path	**High-Band Path**
BPFs (in 1- and 2-dB Diplexer Attenuators)	Center Frequency	24 GHz	60 GHz
	Number of Resonators	2	
	Filter Response	Butterworth	
	K-Inverter Type	C-coupled	L-coupled
Attenuators	Topology	Multi-bit single-stage distributed attenuator	
	Control Type	Digital (0 V for reference state and 1.8 V for attenuation state)	
	Attenuation Step	1 dB	
	Attenuation Bit	4 bit (16 states)	
	Attenuation Range	16 dB	

through large resistors (15 kΩ) to prevent RF signals from leaking through the dc bias lines [3-9], [3-10]. The design parameters of the BPFs and attenuators, used in the concurrent dual-band attenuator are shown in Table 3.1.

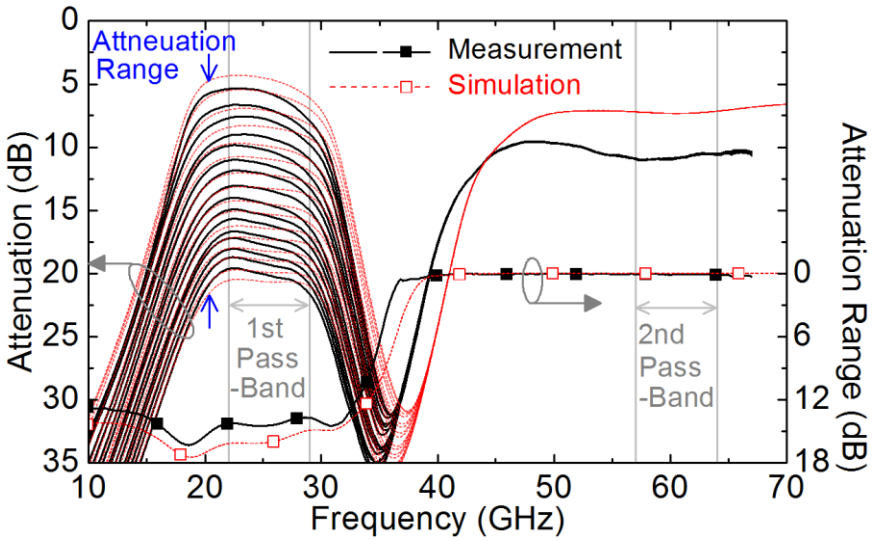
The 4-bit 24/60-GHz concurrent dual-band step attenuator is fabricated using CMOS in TowerJazz 0.18-μm BiCMOS process and its photograph is shown in Fig. 3.12. It occupies 1.8×0.52 mm^2 excluding on-wafer RF and dc pads. Transistors laid out typically contain shunt parasitic capacitances and resistances, which could cause a shift in the frequency response and increase the insertion loss of the attenuator, respectively. In particular, the filtering response of the developed attenuator is degraded easily by the parasitic capacitances as compared to wide-band circuits. To minimize the resistive and capacitive parasitics, the body-floating technique in [3-9] is employed for the design of the shunt

transistors. All interconnections in the attenuator are laid out using coplanar waveguide (CPW) structure and all spiral inductors are laid out inside the CPW structure to minimize the electric fields penetrating into the substrate and the mutual coupling between adjacent components, which facilitates low insertion loss and compact size, respectively. For the capacitors, metal-insulator-metal (MiM) structure is employed due to the compactness, reliability and high Q-factor in the design frequency ranges, except the series capacitors in the 60-GHz 1-bit 1- and 2-dB BPF-attenuators. These capacitors are implemented with a metal-oxide (SiO_2)-metal (MOM) structure due to their small values. The inductors, interconnects and MOM capacitors in the attenuator are simulated with the EM-simulator IE3D (HyperLynx 3D EM, Mentor Graphics) for the post-layout simulations. The doped P^+, P-taps and deep-trenches are placed between the low- and high-band paths as seen in Fig. 3.12 to minimize the crosstalk coupling through the conductive substrate (8 Ω·cm).

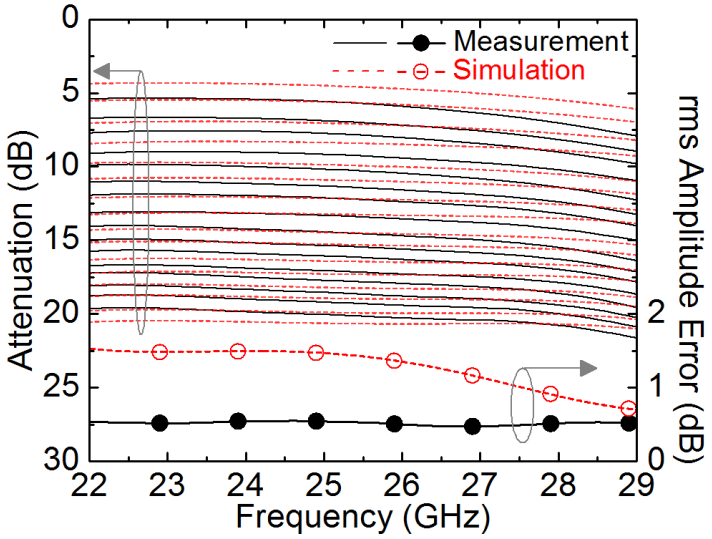
3.2.2 Simulations and Measurements

Figs. 3.13–17 show the post-layout simulations and measurements of the 24/60-GHz concurrent dual-band and low-phase-variation step attenuator. For the simulations, the amplitude at each pass-band is controlled individually. For instance, during the control of the attenuations in the 1st pass-band (22–29 GHz) over 16 states, the amplitude in the 2nd pass-band (57–64 GHz) is fixed at its reference state. However, the attenuator is designed to allow control in both bands simultaneously.

In the 1st pass-band, the measured insertion loss, attenuation range and RMS amplitude error, as seen in Figs. 3.13(a) and (b), are 5.4–7.9, 13.7–14.5 and 0.51–0.54 dB,



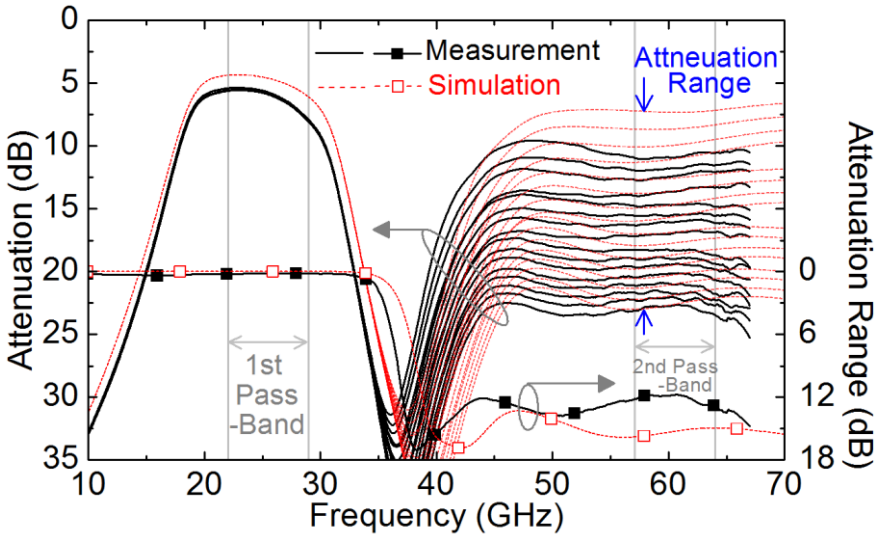
(a)



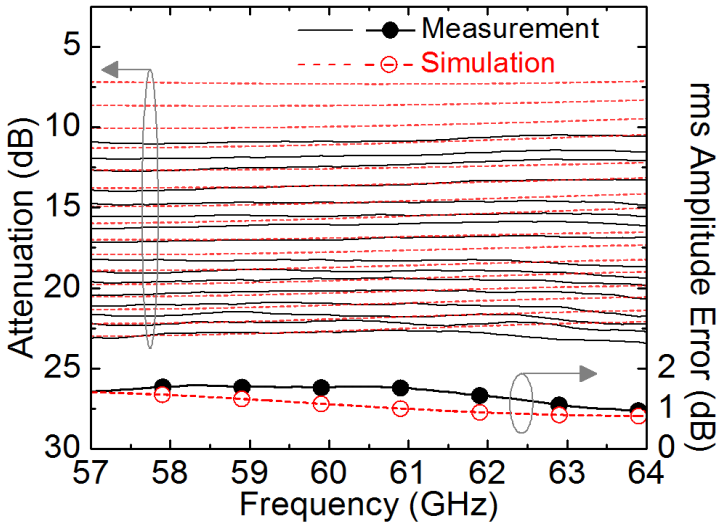
(b)

Fig. 3.13. Simulated and measured (a) attenuation and attenuation range, and (b) zoomed-in attenuation and rms amplitude error during the 16-state amplitude control in the 1st pass-band.

respectively. The measured insertion loss at 24 GHz is 1 dB higher than the simulation. Figs. 3.14(a) and (b) show that the measured insertion loss, attenuation range and RMS amplitude error in the 2nd pass-band are 10.5–11, 11.8–12.9 and 0.93–1.54 dB,



(a)



(b)

Fig. 3.14. Simulated and measured (a) attenuation and attenuation range, and (b) zoomed-in attenuation and rms amplitude error during the 16-state amplitude control at the 2nd pass-band.

respectively. The measured insertion loss at 60 GHz is 3.6 dB higher than the simulation. The insertion loss difference is mainly caused by the accuracy of the parasitic extraction (RCX) simulation used for the transistors at high frequencies and the parasitic

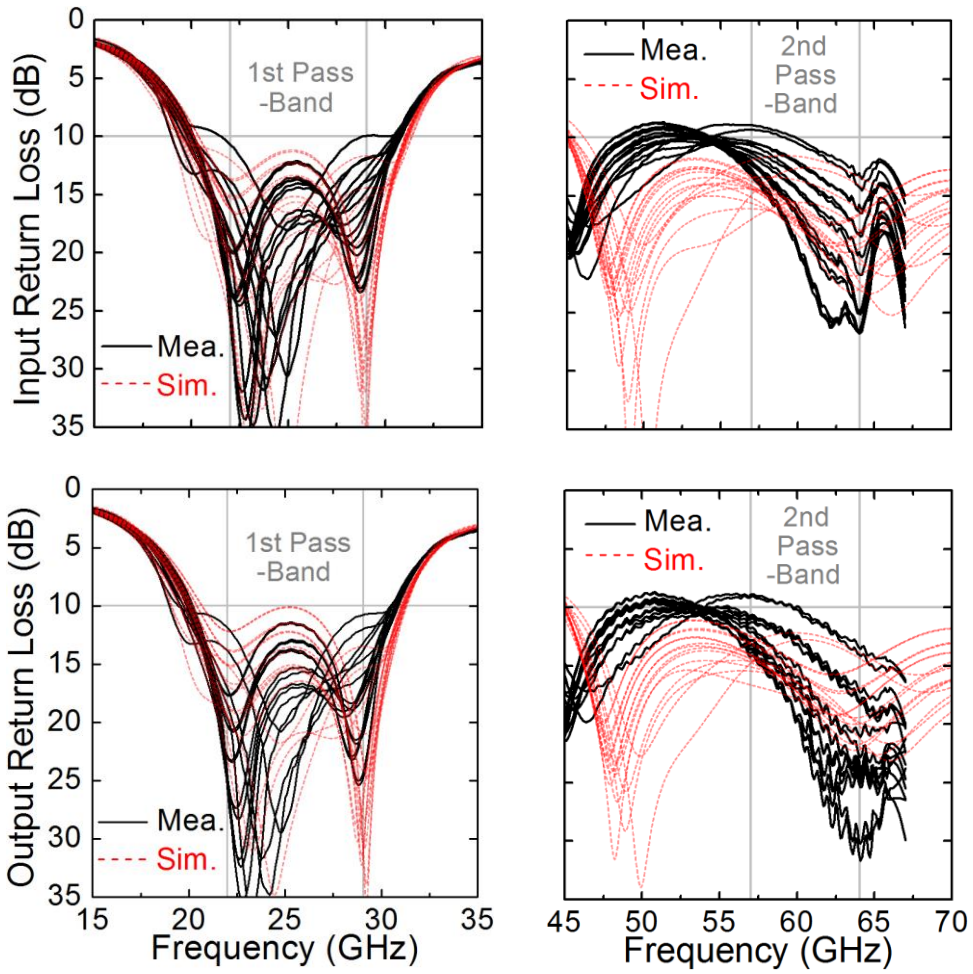
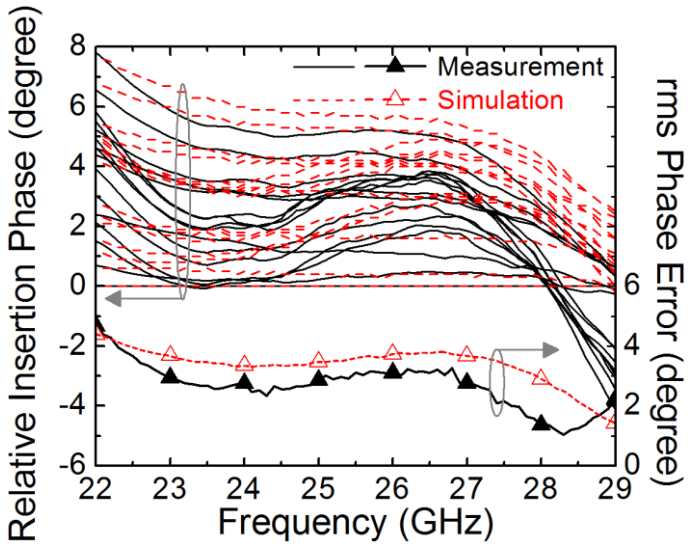
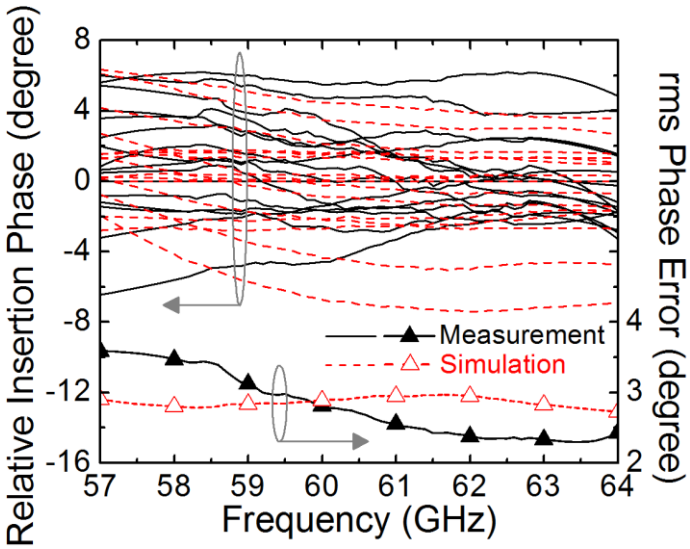


Fig. 3.15. Simulated and measured input and output return losses corresponding to the plots in Figs. 3.13 and 14.

capacitances, which could not be extracted. In Figs. 3.13(a) and 3.14(a), the measured rejections over 16 states at 12 and 36 GHz in the stop-bands are high than 28 and 31 dB, respectively. It is noted that the intermodulation products at 12 and 36 GHz are significant for the developed attenuator having the dual center frequencies, 24 GHz (f_1) and 60 GHz (f_2), because $f_2 - 2f_1 = 12$ GHz and $f_2 - f_1 = 36$ GHz. It is observed in Figs. 3.13(a) and 3.14(a) that the 16-state amplitude control in each pass-band barely affects the amplitude in the



(a)



(b)

Fig. 3.16. Simulated and measured relative insertion phases and rms phase errors during the 16-state amplitude control in (a) the 1st pass-band and (b) the 2nd pass-band.

other pass-band, which reflects the fact that the constituent integrated diplexer-attenuators have high isolations between the low- and high-band paths, and hence good dual-band functionality is attained for the developed attenuator. Fig. 3.15 shows the simulated and

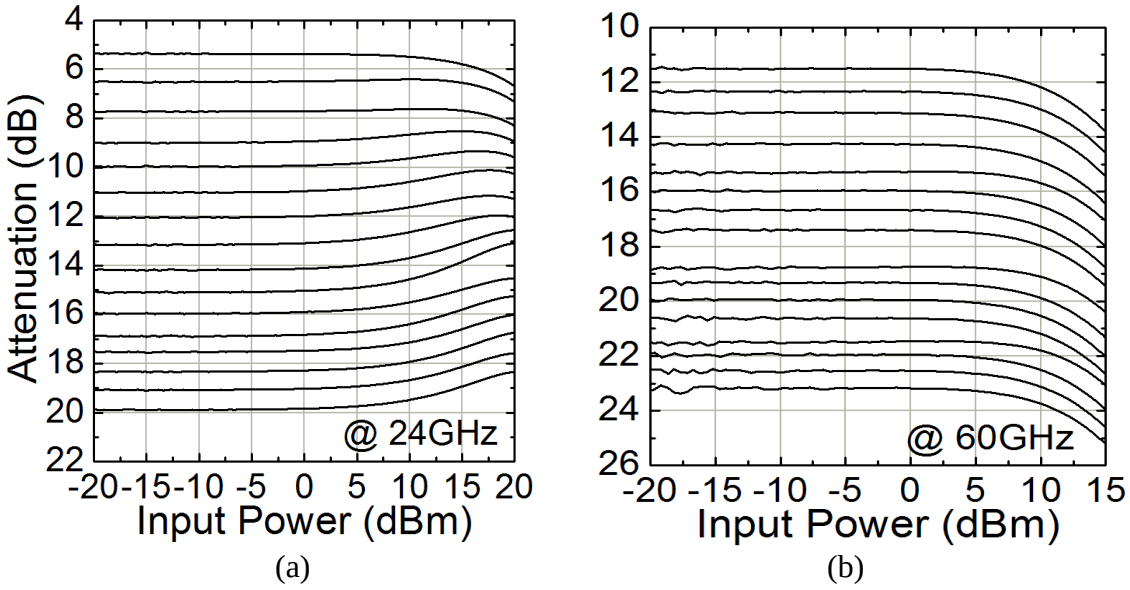


Fig. 3.17. Measured power handling over 16 states at (a) 24 GHz and (b) 60 GHz.

measured input and output return losses during the 1st- or 2nd pass-band amplitude control. The measured input and output return losses are more than 9.9 and 8.9 dB in the 1st and 2nd pass-band over the 16 different states, respectively, which show the developed attenuator is bidirectional. In Fig. 3.16 shows relative insertion phases and RMS phase errors of the attenuator. The measured RMS phase errors in the 1st and 2nd pass-band shown in Figs. 3.16(a) and (b) are 1–4.7° and 2.3–3.6°, respectively. The measured attenuation versus input power seen in Fig. 3.17 shows that the input P1dB is higher than 13.7 and 11.4 dBm at 24 and 60 GHz over all states. Although the insertion loss at 60 GHz is higher than that at 24 GHz, the P1dB at 60 GHz is lower than that at 24 GHz. This is primarily due to the inherently lower power handling capability of the transistors as the frequency is increased, especially when it increases significantly and into the millimeter-

Table 3.2 Comparison of step CMOS attenuators

	Freq. (GHz)	Insertion Loss (dB)	Number of States	Desired Step (dB)	RMS Phase Error (degree)	RMS Amplitude Error (dB)	Input P1dB (dBm)	Size (mm^2) *	Process	Freq. Band Selectivity
[3]	dc–14 (Type 1)	3.7–10	64	0.5	< 4.2	< 0.5	15 (at 10 GHz)	1.25× 0.4	0.18-μm CMOS	No
[4]	10–50	2-3	11	1	0.9–2.9	Not Available	4 (at 35 GHz)	0.75× 0.2	CMOS in 0.12-μm BiCMOS	No
[6]	36–52	4.4–5.9	8	1	1.9–6.7	0.8–1.4	> 20 (at 44 GHz)	0.61× 0.36	CMOS in 0.18-μm BiCMOS	Yes (Single Pass-Band)
[9]	10–67	8.4–15.2	16	3	Not Available	Not Available	> 14 (at 25 GHz) > 10 (at 60 GHz)	1.45× 0.53	CMOS in 0.18-μm BiCMOS	No
This Work	22–29	5.4–7.9	16	1	1–4.7	0.49–0.51	> 14 (at 24 GHz)	1.8× 0.52	CMOS in 0.18-μm BiCMOS	Yes (Dual Pass-Band)
	57–64	10.5–11.1			2.3–3.6	0.93–1.5	> 11 (at 60 GHz)			

* The chip sizes exclude RF and dc pads

wave regime. Fig. 3.17 shows that the attenuation increases as the input power is increased. This is due to the fact that the forward resistance of the shunt transistor's junction diodes between the drain and body becomes smaller when the input power is increased, leading to more signal leakage to the body. In Table 3.2, the performance of the developed attenuator is compared with those of reported CMOS step attenuators in [3-3], [3-4], [3-6] and [3- 9]. The proposed attenuator in this work is the only attenuator that is capable of a concurrent dual-band amplitude control. Moreover, the obtained RMS phase error in each pass-band is comparable with those of the attenuators reported in [3-3] and [3-4], which are designed with particular design techniques to minimize the phase variations for the single band.

3.3 Conclusion

A novel concurrent 22–29/57–64-GHz dual-band 4-bit step attenuator having small phase variations has been developed using a 0.18-μm BiCMOS technology for the first time. The low insertion loss and compact size are achieved by implementing dual-functional elements. The small phase variation is obtained by adding shunt capacitors, which do not impact the attenuator's size and insertion loss much. The design theory of the proposed concurrent dual-band attenuator is validated with the derived formulas and simulation and measurement results. The measured results show low RMS phase errors, low RMS amplitude errors, and high P1dB in both pass bands of 22–29 and 57–64 GHz. Moreover, it is also confirmed that the signal amplitude of the developed attenuator can be controlled independently in each pass-band without any significant effect on the amplitude in the other pass-band, which enables tailoring dual electronic beams independently or concurrently in dual-band phased-array systems. The developed attenuator is attractive for silicon-based concurrent dual-band phased arrays, especially for those demanding a compact size, low insertion loss and minimum tracking/steering error.

3.4 References

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CHAPTER IV

10–67-GHZ CMOS DUAL-FUNCTION SWITCHING ATTENUATOR WITH IMPROVED FLATNESS AND ATTENUATION RANGE*

Attenuators are extensively employed as an amplitude control circuit in communication and radar systems. Their primary purpose is to reduce the signal level without distorting its waveform. In this chapter, a wide-band CMOS attenuator covering 10 to 67 GHz with large attenuation range, improved insertion-loss flatness, and switching function is studied. The attenuator is used for the output signal detection in the phased-array transmitter as shown in Fig. 4.1. The output signal of the PA is detected with the directional coupler and then the attenuator adjusts the signal level as desired. The large attenuation range and improved flatness of the attenuator enable to handle the high power output signal over a broad frequency band. The embedded switching function in the attenuator is to turn on and off the detection path to minimizing the leakages. The collected information of the output signal, the amplitude and phase, can be employed to fix the amplitude/phase errors in the phased-array transmitter.

Attenuators are typically classified as step (or digital) or linear (or analog) type [4-1]–[4-5]. Step attenuators are preferred for systems demanding high linearity, power efficiency, and simplicity [4-1], [4-2], [4-4]. Conventional Pi-, T- [4-1], [4-4]–[4-8] and

distributed [4-3], [4-9] attenuators as shown in Fig. 4.2 are the basic topologies for most attenuators and can provide step attenuation by digitally controlling the gate voltages.

The flatness of attenuation levels, attenuation range, and bandwidth are typical specifications in attenuator design. The attenuation flatness particularly affects the linear distortion of signals (or signal amplitude fidelity) and signal level across operating frequencies which might cause problems for subsequent components in systems. High attenuation levels are necessary to handle high-power systems or circuits. Ultra-wide bandwidth is typically desired for attenuators. The Pi- and T-attenuators have the virtue of compactness, while the distributed attenuators have low insertion loss and relatively flat transmission performance over wide frequency ranges. The Pi- and T-attenuators, however, are substantially affected by the switching performance of transistors; thereby, it is hard to obtain optimum attenuation flatness, range, and bandwidth with CMOS transistors due to the fact that CMOS transistors have poorer switching performance at microwave frequencies than GaAs transistors [4-10]. On the other hand, the distributed attenuator is not proper for large attenuation ranges as it demands many transmission lines and hence a large chip area [4-1], [4-3], [4-9].

In RF systems, switching is normally needed at various places to achieve certain functions and/or improve system performance. These switching functions are typically

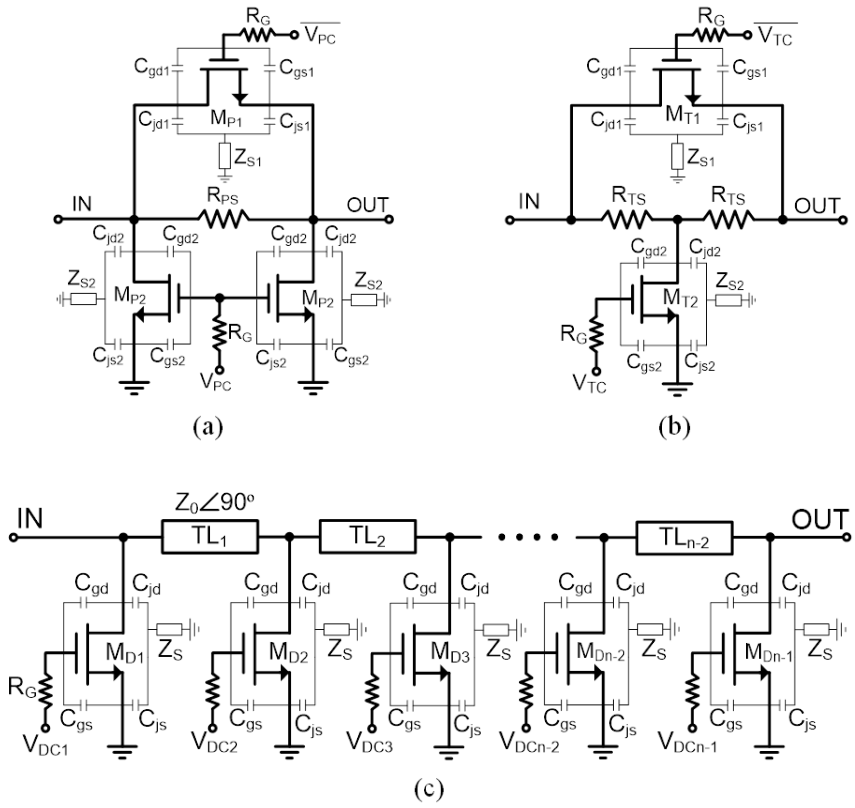


Fig. 4.2. Conventional attenuator topologies: (a) 1-bit Pi-, (b) 1-bit T-, and (c) n-state distributed attenuators.

executed by individual switches. However, in order to improve system performance, size and cost, multifunction components are needed. To that end, dual-function attenuators possessing both attenuation and switching functions in the same circuit is highly desired. In spite of their usefulness, the dual-function switching attenuators have not been reported.

This paper reports a new CMOS dual-function 4-bit step attenuator capable of switching and large attenuation ranges with improved flatness over an ultra-wide bandwidth from 10–67 GHz. This attenuator was briefly reported in [4-11]. A new attenuator design method is proposed and implemented using a cascade of the Pi- or/and T-attenuator and distributed attenuator to improve the attenuation flatness, range, and

bandwidth. The new design exploits the inherent nature of the slopes of the insertion loss responses of the Pi- and T-attenuator, which increase as the frequency is increased at certain attenuation states, and that of the distributed resonator with shortened transmission lines that decreases with frequency. These two opposite slopes compensate each other, resulting in good attenuation flatness and large attenuation range across wide frequency ranges. The body-floating technique for transistors implemented for switches in [4-12]-[4-15] is also employed for the attenuator design to help minimize the effect of the low-resistivity silicon substrate. It is found that the use of the body-floating technique can also improve the flatness and transmission performance in CMOS attenuators. The reflective switching function for the attenuator is accomplished by implementing a switchable attenuating unit for the first and last stage of the 4-bit attenuator that results in good off-state isolation.

4.1 Analysis of Conventional Attenuators

Fig. 4.2 shows the conventional Pi-, T- and distributed attenuators that contain series resistances (R_{PS}, R_{TS}), transistors' significant parasitic elements affecting the performance of attenuators including junction capacitances at the drain (C_{jd1}, C_{jd2}, C_{jd}) and the source (C_{js1}, C_{js2}, C_{js}), gate-drain capacitances (C_{gd1}, C_{gd2}, C_{gd}) and gate-source capacitances (C_{gs1}, C_{gs2}, C_{gs}), and the substrate impedances from the source/drain junctions to ground (Z_{S1}, Z_{S2}, and Z_S). A large resistance, R_G, is used at the gate of each transistor to

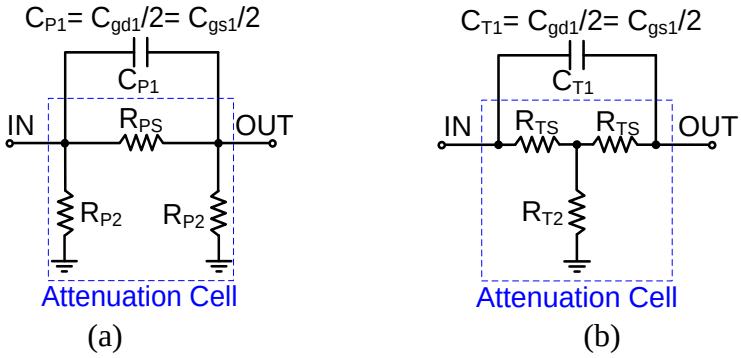


Fig. 4.3. Equivalent circuits at an attenuation state of the Pi-attenuator (a) and T-attenuator (b).

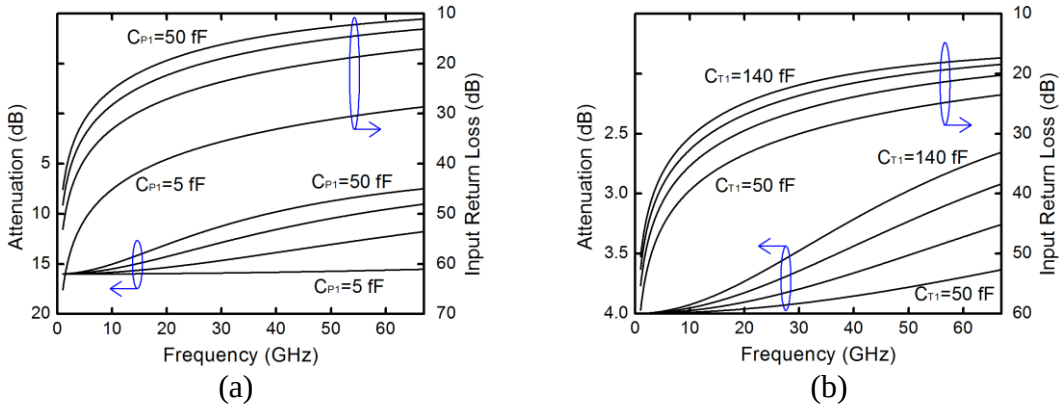


Fig. 4.4. Attenuation and input return loss of (a) 16-dB Pi-attenuator for C_{P1} from 5 to 50 fF in 15-fF steps and (b) 4-dB T-attenuator for C_{T1} from 50 to 140 fF in 30-fF steps.

prevent RF signal from leaking through the DC bias line and to decrease the fluctuations of the gate-drain and gate-source voltages in the attenuators, which may cause breakdown [4-16].

4.1.1 Pi- and T-Attenuator

Fig. 4.3 represents the equivalent circuits of the Pi- and T-attenuator for an attenuation state, ignoring the junction capacitances and substrate impedances for

simplicity. The series and shunt transistors (M_{P1}, M_{P2}, M_{T1} and M_{T2}), as seen in Fig. 4.2, act as switches in the attenuators. In the attenuation state, M_{P2} and M_{T2} are turned on and represented by on-resistance R_{P2} and R_{T2}, respectively, whereas M_{P1} and M_{T1} are switched off with off-capacitance C_{P1} and C_{T1}, respectively. R_{P2} and R_{T2} together with R_{PS} and $R_{TS,}$ respectively, act as attenuation cells. These resistances can be expressed as [4-17]:

$$R_{P2}=Z_0(1+10^{-L/20})/(1-10^{-L/20}), \tag{4.1}$$

$$R_{PS}=2R_{P2}/\{(R_{P2}/Z_0)^2-1\}, \tag{4.2}$$

$$R_{TS}=Z_0(1-10^{-L/20})/(1+10^{-L/20}), \tag{4.3}$$

$$R_{T2}=(Z_0^2-R_{TS}^2)/2R_{TS} \tag{4.4}$$

where L denotes the attenuation value of the attenuation cell in dB and Z_0 represents the terminating impedance at the input and output ports. Assuming $C_{gd1}=C_{gs1}$ leads to $C_{P1}=C_{T1}=C_{gd1}/2=C_{gs1}/2$. The attenuation ($S_{21}$) of the circuit in Fig. 4.3(a) can be derived from the ABCD matrix as

$$S_{21}^{PA}=\sqrt{\frac{4R_{P2}^4(1+\omega^4C_{P1}^4R_{PS}^4+2\omega^2C_{P1}^2R_{PS}^2)}{S_{PA}+T_{PA}+\omega^4C_{P1}^4U_{PA}^2+\omega^2C_{P1}^2W_{PA}}}, \tag{4.5}$$

where $Y_0=1/Z_0$, $S_{PA}=4R_{P2}^4(1+2Y_0^2R_{PS}^2)$, $T_{PA}=8Y_0R_{PS}R_{P2}^3(R_{PS}+R_{P2})$, $U_{PA}=2R_{PS}^2R_{P2}(R_{P2}+Z_0)$, $V_{PA}=8R_{P2}^3(Z_0+R_{P2}+2R_{PS})$ and $W_{PA}=R_{PS}^2\{T_{PA}+V_{PA}+R_{PS}^2(Y_0^2R_{P2}^4+6R_{P2}^2+Z_0^2)\}$. The corresponding reflection coefficient S11 can be obtained from

$$S_{11}=(Z_{in}-Z_0)/(Z_{in}+Z_0) \tag{4.6}$$

where Zin is the input impedance. The input impedance of the circuit in Fig. 4.3(a) can be derived as

$$Z_{in}^{PA}=\frac{Z_0 X_{PA}+j\omega C_{P1}Z_0 R_{PS}R_{P2}^2}{X_{PA}+j\omega C_{P1}R_{PS}R_{P2}(R_{P2}+2Z_0)} \tag{4.7}$$

where $X_{PA}=R_{P2}(2Z_0+R_{PS}+R_{P2})+Z_0R_{PS}$. Similarly, the attenuation and input impedance of the circuit in Fig. 4.3(b) are obtained as

$$S_{21}^{TA}=\sqrt{\frac{R_{T2}^2S_{TA}^2+Z_0^4\omega^4C_{T1}^4T_{TA}^2+\omega^2C_{T1}^2U_{TA}}{S_{TA}^4+\omega^4C_{T1}^4T_{TA}^4+2\omega^2C_{T1}^2S_{TA}^2T_{TA}^2}} \tag{4.8}$$

$$Z_{in}^{TA}=\frac{Z_0S_{TA}+j\omega C_{T1}Z_0^3}{S_{TA}+j\omega C_{T1}(Z_0^2+2Z_0R_{TS})} \tag{4.9}$$

where $S_{TA}=Z_0+R_{TS}+R_{T2}$, $T_{TA}=Z_0(R_{TS}+Z_0)$ and $U_{TA}=Z_0^2(2Z_0^3S_{TA}+2R_{T2}^2T_{TA}+R_{TS}^2R_{T2}^2)$.

The attenuation flatness for the Pi-attenuator (F_{PA}) and T-attenuator (F_{TA}) between two frequencies ω_1 and ω_2 can be expressed as the ratio between the attenuations at ω_1 and ω_2 which, upon using (4.5) and (4.8), yields

$$\begin{aligned}&\{\omega_1^4\omega_2^4R_{PS}^4U_{PA}^2(F_{PA}-1)\}C_{PA}^4+\{\omega_1^2\omega_2^2R_{PS}^4W_{PA}(\omega_1^2F_{PA}-\omega_2^2)\\&+2\omega_1^2\omega_2^2R_{PS}^2U_{PA}^2(\omega_2^2F_{PA}-\omega_1^2)\}C_{PA}^3+\{U_{PA}^2(\omega_2^4F_{PA}-\omega_1^4)\\&+R_{PS}^4Y_{PA}(\omega_1^4F_{PA}-\omega_2^4)+2\omega_1^2\omega_2^2R_{PS}^2W_{PA}(F_{PA}-1)\}C_{PA}^2\\&+(W_{PA}(\omega_2^2F_{PA}-\omega_1^2)+2R_{PS}^2Y_{PA}(\omega_1^2F_{PA}-\omega_2^2))C_{PA}\\&+\{Y_{PA}(F_{PA}-1)\}=0\end{aligned} \tag{4.10}$$

$$\begin{aligned}&\{\omega_1^4\omega_2^4Z_0^4T_{TA}^6(F_{TA}-1)\}C_{TA}^4+\{2\omega_1^2\omega_2^2Z_0^4S_{TA}^2T_{TA}^4(\omega_2^2F_{TA}-\omega_1^2)\\&+\omega_1^2\omega_2^2T_{TA}^4U_{TA}(\omega_1^2F_{TA}-\omega_2^2)\}C_{TA}^3+\{R_{T2}^2S_{TA}^2T_{TA}^4(\omega_1^4F_{TA}-\omega_2^4)\\&+Z_0^4S_{TA}^4T_{TA}^2(\omega_2^4F_{TA}-\omega_1^4)+2\omega_1^2\omega_2^2C_{T1}^4S_{TA}^2T_{TA}^2U_{TA}(F_{TA}-1)\}C_{TA}^2\\&+\{2R_{T2}^2S_{TA}^4T_{TA}^2(\omega_1^2F_{TA}-\omega_2^2)+S_{TA}^4U_{TA}(\omega_2^2F_{TA}-\omega_1^2)\}C_{TA}\\&+\{R_{T2}^2S_{TA}^6(F_{TA}-1)\}=0\end{aligned} \tag{4.11}$$

for the Pi- and T-attenuator, respectively, where $Y_{PA}=S_{PA}+T_{PA}$, $C_{PA}=C_{P1}^2$ and $C_{TA}=C_{T1}^2$. Eqs.

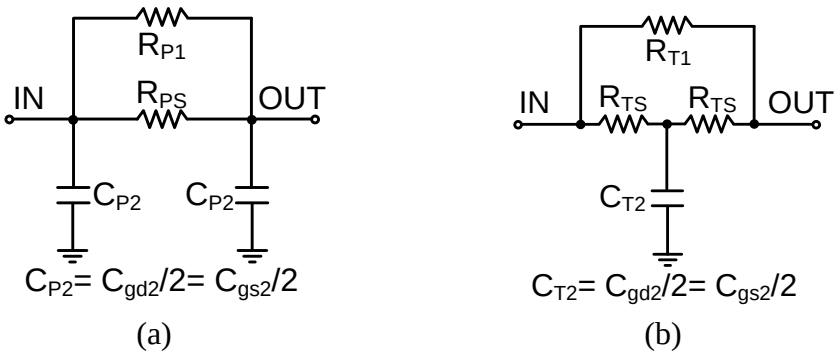


Fig. 4.5. Equivalent circuits at a reference state of (a) the Pi-attenuator and (b) the T-attenuator.

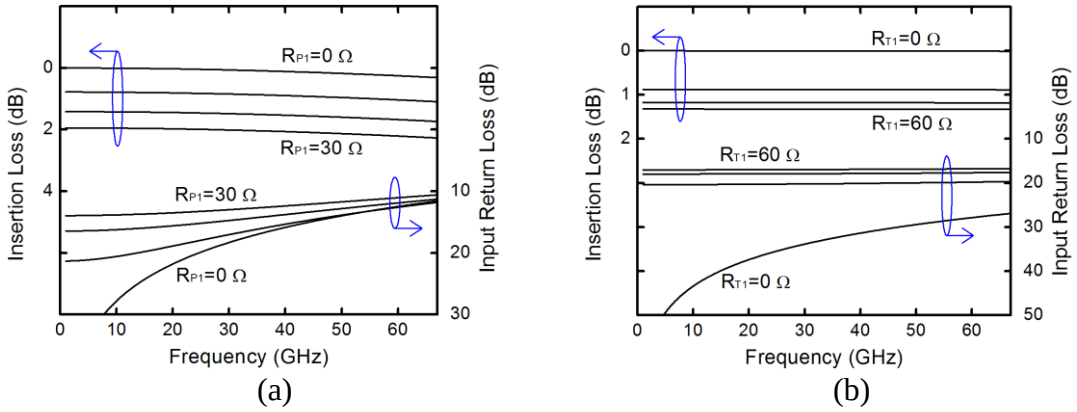


Fig. 4.6. Insertion loss and input return loss at a reference state of (a) 16-dB Pi-attenuator for R_{P1} from 30 to 0 Ω in 10-Ω steps, and (b) 4-dB T-attenuator for R_{T1} from 60 to 0 Ω in 20-Ω steps.

(4.10) and (4.11) enable the sizes of the series transistors M_{P1} and M_{T1} in Fig. 4.2 to be chosen from their off-capacitances C_{P1} and C_{T1} calculated for given frequencies and flatness. As discussed later, the attenuation variation over the desired frequency range could be compensated by using proper transistor sizes and lengths for the transmission lines in the Pi-/T-attenuator and distributed attenuator, respectively.

The ideal 0-dB attenuation flatness for the attenuators in Figs. 4.3(a) and (b) is obtained

when C_{P1}=0 and C_{T1}=0, respectively. Under this ideal condition, perfect matching is also obtained for the attenuators as can be calculated from (4.1), (4.2), (4.6), (4.7) and (4.3), (4.4), (4.6), (4.9) for the Pi- and T-attenuator, respectively. This ideal condition, however, never occurs in practice since the capacitances C_{P1} and C_{T1} always exist in attenuators and hence need to be considered in the attenuator design. As examples to show the significance of C_{P1} and C_{T1} in the Pi- and T-attenuator, we consider a one-bit 16-dB Pi- and 4-dB T-attenuator whose equivalent circuits are given in Fig. 4.3. For the 16-dB Pi-attenuator, R_{PS}=153.78 Ω and R_{P2}=68.83 Ω as calculated from (4.1) and (4.2). Fig. 4.4(a) shows the attenuation and input return loss of this 16-dB Pi-attenuator calculated from (4.5)–(4.7) as C_{P1} is changed from 5 to 50 fF in 15-fF steps. For the 4-dB T-attenuator, R_{TS}=11.31 Ω and R_{T2}= 104.83 Ω as calculated from (4.3) and (4.4). Fig. 4.4(b) shows the attenuation and input return loss of the 4-dB T-attenuator calculated from (4.6), (4.8), and (4.9) with C_{T1} varied from 50 to 140 fF in 30-fF steps. We can see, as expected, that the flatness of the attenuation and the return loss are exacerbated by increasing C_{P1} and C_{T1}. The reason is the off-capacitances C_{P1} and C_{T1} act as leakage paths and some input signals make a detour without passing through the attenuation cell.

In contrast with the attenuators in attenuation states, the transistors M_{P1} and M_{T1} are on while M_{P2} and M_{T2} are off when the attenuators are in reference states. Fig. 4.5 shows the equivalent circuits of the Pi- and T-attenuator at a reference state, in which R_{P1}, R_{T1} and C_{P2}, C_{T2} represent the on-resistances of M_{P1}, M_{T1} and off-capacitances of M_{P2}, M_{T2}, respectively. The insertion loss and the input impedance of the equivalent circuit in Fig. 4.5(a) are derived as

$$S_{21}^{PR}=\sqrt{\frac{4Z_0^2}{(Z_{S1}+2Z_0)^2+\left(Z_{S1}Z_0^2\omega^2C_{P2}^2\right)^2+\omega^2C_{P2}^2S_{PR}}} \tag{4.12}$$

$$Z_{in}^{PR}=\frac{Z_0+Z_{S1}+j\omega C_{P2}Z_0Z_{S1}}{1-Z_0Z_{S1}\omega^2C_{P2}^2+j\omega C_{P2}(2Z_0+Z_{S1})} \tag{4.13}$$

where $Z_{S1}=R_{P1}R_{PS}/(R_{P1}+R_{PS})$ and $S_{PR}=2Z_0^2(Z_{S1}^2+2Z_0^2+2Z_{S1}Z_0)$. For the equivalent circuit in Fig. 4.5(b), the insertion loss and input impedance are obtained as

$$S_{21}^{TR}=\frac{\sqrt{(4Y_0^2T_{TR}-\omega^2C_{T2}^2S_{TR})^2+4Y_0^2\omega^2C_{T2}^2U_{TR}^2}}{(4Y_0^2+\omega^2C_{T2}^2)U_{TR}} \tag{4.14}$$

$$Z_{in}^{TR}=\frac{\frac{R_{TS}}{T_{TR}}(3R_{TS}R_{T1}+3Z_0R_{TS}+2Z_0R_{T1})\omega C_{T2}-j(Z_0+Z_{S2})}{\left(Z_{S2}+Z_0+\frac{3R_{TS}^2}{T_{TR}}\right)\omega C_{T2}-j(1-Z_0R_{TS}\omega^2C_{T2}^2)} \tag{4.15}$$

where $S_{TR}=Y_0R_{TS}R_{T1}$, $T_{TR}=R_{T1}+2R_{TS}$, $U_{TR}=S_{TR}+T_{TR}$ and $Z_{S2}=2R_{TS}\ R_{T1}/T_{TR}$, making use of $(\omega C_{T2}R_{TS})^2<<1$ due to very small C_{T2} typically used in the attenuator design. Equations (4.12)–(4.15) show that the transmission and reflection performance of the Pi- and T-attenuator in Fig. 4.5 can be improved by reducing R_{P1} or C_{P2}, and R_{T1} or C_{T2}, respectively. However, C_{P2} and C_{T2} are not adjustable; these off-capacitances are predetermined by the size of M_{P2} and M_{T2}, which are chosen for the desired on-resistances corresponding to the attenuation state as discussed earlier, and hence are fixed. Consequently, in order to improve the transmission and reflection performance at the reference state, small R_{P1} and R_{T1} are used, which can be realized by employing large width for M_{P1} and M_{T1}, respectively. As examples illustrating the effect of R_{P1} and R_{T1}, we consider the same one-bit 16-dB Pi-attenuator with R_{PS}= 153.78 Ω and one-bit 4-dB T-attenuator with R_{TS}= 11.31

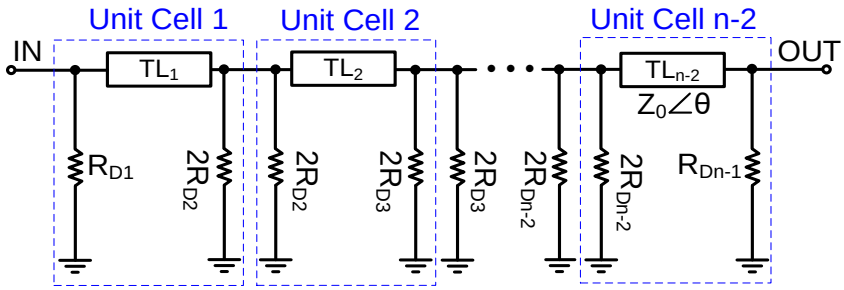


Fig.4.7. Equivalent circuit for the highest attenuation state of the n-state distributed attenuator.

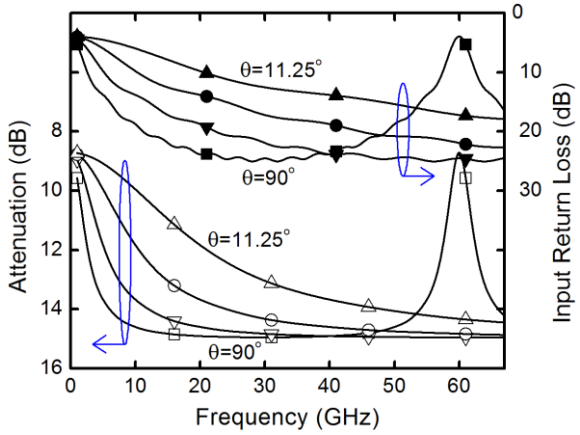


Fig. 4.8. Attenuation and input return loss at the highest attenuation state of a 4-bit distributed attenuator for transmission-line electrical length θ at 30 GHz of 90°, 45°, 22.5°, and 11.25°.

Ω used previously, and use 0.18-μm nMOS transistors of 12-μm and 6-μm gate-width for M_{P2} and M_{T2}, respectively. The off-capacitances C_{P2} and C_{T2} of these transistors are 13 fF and 4.3 fF, respectively. These transistors have on-resistances of around 68.83 Ω (R_{P2}) and 104.83 Ω (R_{T2}), respectively, which are the same as those used for calculations in Fig. 4.4. Fig. 4.6(a) shows the insertion loss and input return loss of the Pi-attenuator represented by the equivalent circuit in Fig. 4.5(a) calculated from (4.2), (4.6), (4.12), and (4.13) as R_{P1} is decreased from 30 to 0 Ω in 10-Ω steps. Fig. 4.6(b) shows the insertion loss and

input return loss of the T-attenuator represented by the equivalent circuit in Fig. 4.5(b) obtained from (4.3), (4.6), (4.14) and (4.15) for R_{T1} varied from 60 to 0 Ω in 20-Ω steps. Fig. 4.6 shows that small on-resistance R_{P1} and R_{T1} are necessary for low insertion loss and high return loss in the conventional Pi- or T-attenuator design. However, these small on-resistances correspond to large off-capacitances for transistors, which cause poor attenuation flatness for the attenuators. Therefore, the performance of the conventional attenuators is always limited by a tradeoff between the insertion/return loss and attenuation flatness, which prevents their optimum design. Moreover, there is also a tradeoff between the attenuation level and flatness in the conventional attenuator design. For high attenuation, large R_{PS} and R_{TS} are needed as seen from (4.1)-(4.3). Large R_{PS} and R_{TS}, however, cause poor transmission and reflection performance in the reference state. This effect can be compensated for with small on-resistances R_{P1} and R_{T1}; yet also leading to large off-capacitances which exacerbates the attenuation flatness. The equations derived in this section help facilitate the analysis of the Pi- and T-attenuator.

4.1.2 Distributed Attenuator

Fig. 4.2(c) shows the conventional n-state distributed attenuator consisting of multiple shunt nMOS transistor switches spaced apart by λ/4 transmission lines. The transmission lines help to maintain matched input and output conditions at all attenuation states. Various attenuation states can be obtained by turning on proper transistors. Fig. 4.7 depicts the attenuator's equivalent circuit for the highest attenuation state when all transistors are switched on, neglecting the parasitic elements indicated in Fig. 4.2(c). We

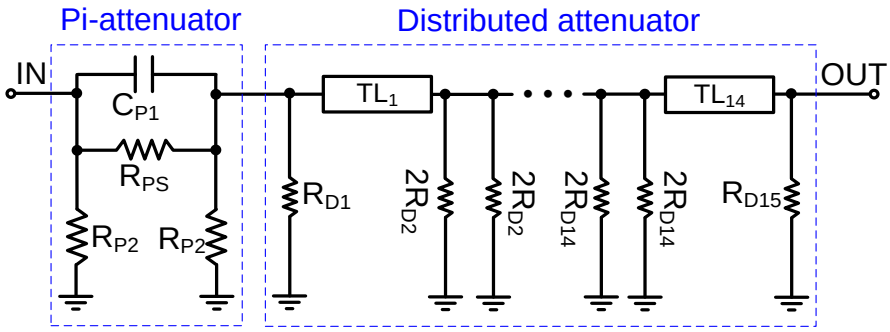


Fig. 4.9. Equivalent circuit of Pi-distributed attenuator consisting of 1-bit Pi- and 4-bit distributed attenuators at an attenuation state.

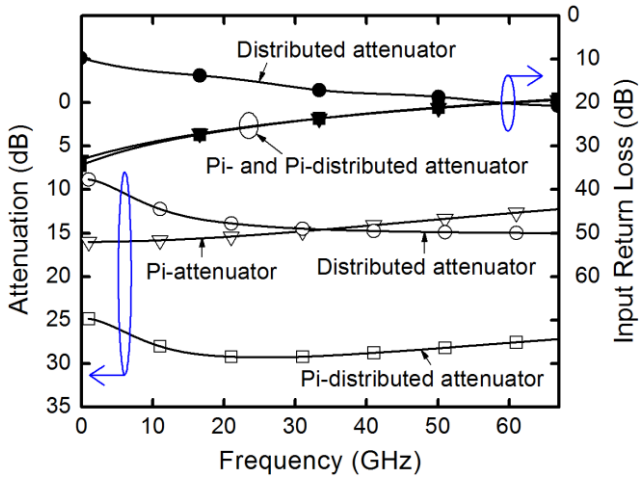


Fig. 4.10. Attenuations and input return losses of the Pi-distributed attenuator, and Pi- and distributed attenuator constituents.

consider identical attenuation steps and correspondingly the values of all the transistors' on-resistances are assumed to be equal ($R_{Dn-1}=R_D$, n=2, 3, …).

To examine the effect of the transmission-line length, we plot in Fig. 4.8 the attenuation and return loss of a (4-bit) 16-state distributed attenuator for the highest 16-dB attenuation state, calculated using the *ABCD* matrix of the distributed attenuator shown in Fig. 4.7, as the electrical length θ of the transmission lines at 30 GHz is varied from 90°

to 11.25° in four steps (90°, 45°, 22.5° and 11.25°). R_D=217 Ω, and Z_0=50 Ω are used for obtaining the 15-dB attenuation. As can be seen in Fig. 4.8, the attenuation flatness becomes worse with shorter transmission lines from 10–50 GHz because the 30-GHz center frequency is shifted to a higher frequency. We also see that the slopes of the attenuation curves corresponding to shorter transmission lines are opposite to those corresponding to larger capacitances for the Pi- and T-attenuator as seen in Fig. 4.4.

4.2 Proposed Attenuator Architecture

4.2.1 Attenuator Topology for Improved Attenuation Flatness and Range

The foregoing analysis reveals that, in general, the slopes of the attenuation responses of the Pi- and T-attenuator are opposite to that of the distributed resonator with reduced transmission-line length as the frequency is increased. A new attenuator with small attenuation fluctuation and large attenuation range is proposed exploiting these inherent characteristics. Specifically, the new attenuator is realized by employing the Pi-attenuator (or/and T-attenuator) and the distributed attenuator with short transmission lines in a cascade connection, which is hereafter referred to as "Pi/T-distributed attenuator."

Fig. 4.9 shows an equivalent circuit of the new Pi-distributed attenuator that consists of a 1-bit Pi-attenuator and a 4-bit distributed attenuator. Fig. 4.10 shows the attenuation and input return loss of the Pi-distributed attenuator calculated using the *ABCD* matrix. Those of the constituent Pi- and distributed attenuators of the Pi-distributed attenuator are also plotted in the same figure for comparison. For the plot in Fig. 4.10, the Pi- and distributed attenuators are respectively designed to have 16-dB and 15-dB

Table 4.1 Summary of the calculations in Fig. 4.10

	Pi-Distributed Attenuator (θ=18° at 30 GHz, C_{P1}=23 fF)	Pi-Attenuator (C_{P1}=23 fF)	Distributed Attenuator (θ=18° at 30 GHz)
S21 at 10 GHz	- 27.7 dB (Magnitude: 0.0412)	- 15.8 dB (0.162)	- 11.9 dB (0.254)
S21 at 30 GHz	- 29.2 dB (0.0347)	- 14.9 dB (0.18)	- 14.4 dB (0.191)
S21 at 67 GHz	- 27.16 dB (0.0439)	- 12.2 dB (0.245)	- 15 dB (0.178)
Flatness (10-67 GHz)	2.05 dB (0.00092)	3.6 dB (0.083)	3.1 dB (0.076)

attenuation with R_{PS}=153.8 Ω, R_{P2}=68.8 Ω, C_{P1}=23 fF, R_D=217 Ω, and Z_0= 50 Ω. A 6-finger nMOS transistor of 4-μm width having off-capacitance (C_{P1}) of 23 fF and on-resistance of about 21 Ω is chosen to compromise between the insertion loss and the attenuation flatness of the 15-dB Pi-attenuator constituent. A short electrical length (θ) of 18° (at 30 GHz) is chosen for the transmission lines in the distributed attenuator to obtain an opposite attenuation slope to that of the Pi-attenuator, hence compensating for the attenuation variation. Table 4.1 summarizes the attenuation and flatness performance in Fig. 4.10. The attenuation flatness and range are improved to 2.05 dB (over 10–67 GHz) and 29.2 dB (at 30 GHz), respectively, for the Pi-distributed attenuator. It is noted that the increased attenuation of the Pi-distributed attenuator is the sum of the attenuations of the Pi-attenuator (14.9 dB) and distributed attenuator (14.4 dB) at 30 GHz.

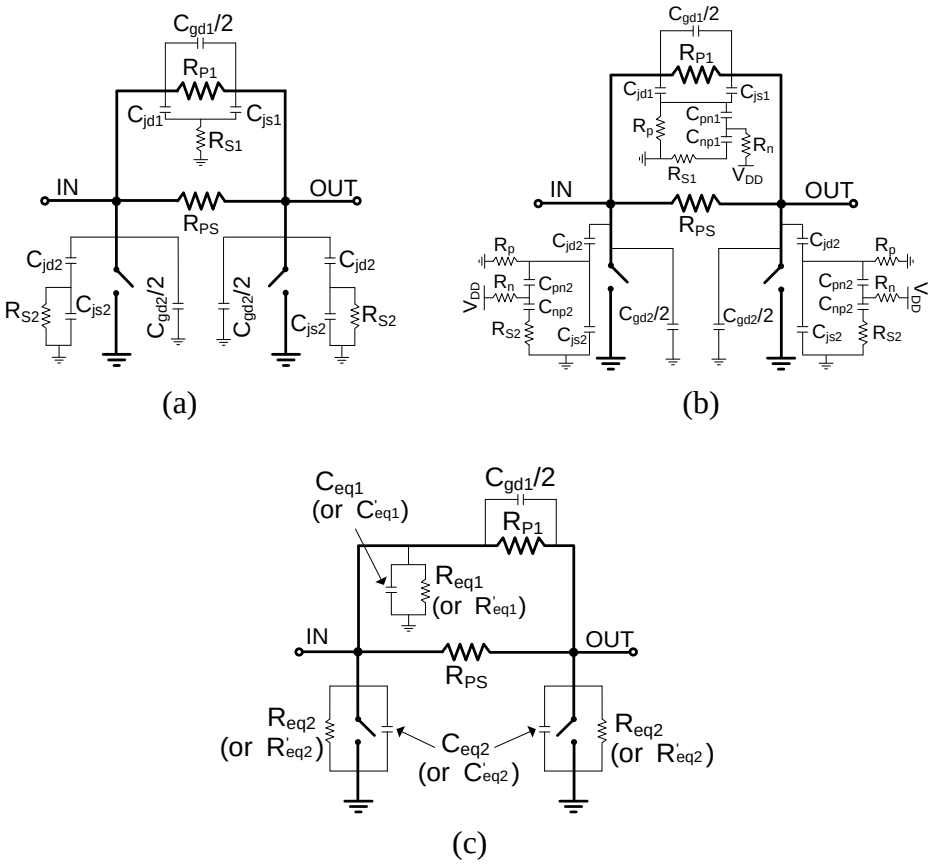


Fig. 4.11. Equivalent circuits at a reference state of the Pi-attenuator consisting of (a) normal transistors and (b) transistors designed by body-floating technique. (c) An approximate equivalent circuit of (a) or (b). $R_{eq1,2}$ and $C_{eq1,2}$ are for normal transistors, while $R'_{eq1,2}$ and $C'_{eq1,2}$ are for body-floated transistors.

4.2.2 Body-Floating Technique for Improved Attenuation Flatness and Transmission Performance

Figs. 4.11 (a) and (b) show equivalent circuits of the conventional Pi-attenuator, including parasitic elements, at a reference state employing normal transistors and deep n-type well (DNW) transistors with body floated, respectively. DNW transistors and body-floating technique have been used in the design of switches [4-12]-[4-15]. The use of body floating for transistors can also improve the power handling capability in attenuators [4-

18]. DNW transistors and body-floating technique, however, have not been implemented for improving the flatness and transmission performance of attenuators. The isolated p-well and DNW are biased with V_{SS} and V_{DD} through large resistors, R_p (15 kΩ) and R_n (15 kΩ), respectively, as seen in Fig. 4.11(b). R_{S1} and R_{S2} in Fig. 4.11 denote the substrate resistances. $C_{pn1,2}$ and $C_{np1,2}$ in Fig. 4.11(b) denote the p-n and n-p junction capacitances, respectively. On the assumption that the on-resistance R_{P1} is very small compared with the other parasitic impedances of the series transistor, we can approximately separate the parasitic elements into a series part (consisting of R_{P1} and $C_{gd1}/2$) and a shunt part (consisting of R_{eq1} and C_{eq1} or R'_{eq1} and C'_{eq1}) as seen in Fig. 4.11(c), as done in [4-16]. In Fig. 4.11(c), $C_{eq1,2}$ and $R_{eq1,2}$ denote the sum of the shunt parasitic capacitances and resistances of the equivalent circuit in Fig. 4.11(a), respectively. Similarly, $C'_{eq1,2}$ and $R'_{eq1,2}$ denote corresponding elements of the equivalent circuit in Fig. 4.11(b).

The equivalent shunt parasitic elements of the series transistor in on-state and the shunt transistor in off-state in Fig. 4.11(c), assuming R_p and R_n are infinite, can be expressed as

$$R_{eq1}=(1+4R_{S1}^2\omega^2C_{jd1}^2)/(4R_{S1}\omega^2C_{jd1}^2) \tag{4.16}$$

$$C_{eq1}=2C_{jd1}/(1+4R_{S1}^2\omega^2C_{jd1}^2) \tag{4.17}$$

$$R_{eq2}=(1+4R_{S2}^2\omega^2C_{jd2}^2)/(R_{S2}\omega^2C_{jd2}^2) \tag{4.18}$$

$$C_{eq2}=\{(2R_{S2}^2\omega^2C_{jd2}^3+C_{jd2})/(1+4R_{S2}^2\omega^2C_{jd2}^2)\}+(C_{gd2}/2) \tag{4.19}$$

$$R'_{eq1}=\frac{(1+4\omega^2R_{S1}^2C_{jd1}^2)\omega^2C_{pn1}^2+(16C_{jd1}+8C_{pn1})\omega^2C_{jd1}}{4R_{S1}\omega^4C_{jd1}^2C_{pn1}^2} \tag{4.20}$$

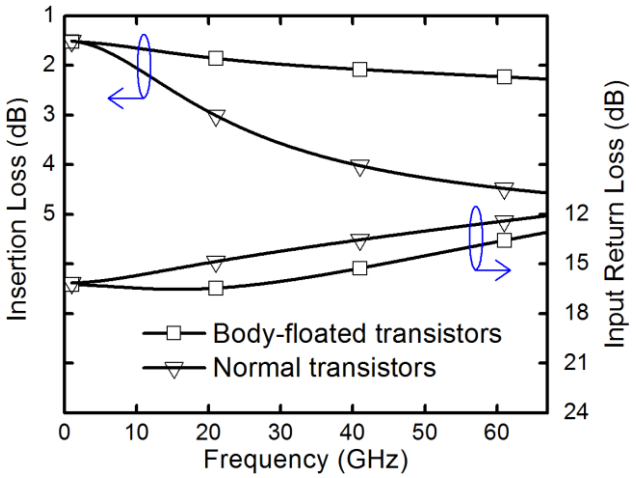


Fig. 4.12. Simulated insertion loss and return loss at a reference state of the Pi-attenuator with normal and body-floated transistors.

$$C'_{eq1}=\frac{2C_{jd1}\left(4\omega^2C_{pn1}C_{jd1}+\omega^2C_{pn1}^2\right)}{\left(1+4\omega^2R_{S1}^2C_{jd1}^2\right)\omega^2C_{pn1}^2+\left(16C_{jd1}+8C_{pn1}\right)\omega^2C_{jd1}} \tag{4.21}$$

$$R'_{eq2}=\frac{\left(1+4R_{S2}^2\omega^2C_{jd2}^2\right)+\frac{8C_{jd2}}{C_{pn2}}\left(1+\frac{2C_{jd2}}{C_{pn2}}\right)}{R_{S2}\omega^2C_{jd2}^2} \tag{4.22}$$

$$C'_{eq2}=\frac{2R_{S2}^2\omega^2C_{jd2}^3+C_{jd2}+\frac{2C_{jd2}^2}{C_{pn2}}\left(3+\frac{4C_{jd2}}{C_{pn2}}\right)}{1+4R_{S2}^2\omega^2C_{jd2}^2+\frac{8C_{jd2}}{C_{pn2}}\left(1+\frac{2C_{jd2}}{C_{pn2}}\right)}+\frac{C_{gd2}}{2} \tag{4.23}$$

where $C_{jd1}=C_{js1}$, $C_{jd2}=C_{js2}$, $C_{pn1}=C_{np1}$, $C_{pn2}=C_{np2}$ and $C_{gd2}=C_{gs2}$. In typical transistors used for attenuators, $(2\omega R_{S1}C_{jd1})^2<1$ and $(2\omega R_{S2}C_{jd2})^2<1$ which, upon using, leads to $R'_{eq1}>R_{eq1}$, $R'_{eq2}>R_{eq2}$, $C_{eq1}>C'_{eq1}$ and $C_{eq2}>C'_{eq2}$. It is then straightforward to see that the attenuator containing the body-floated transistors has both lower insertion loss (from

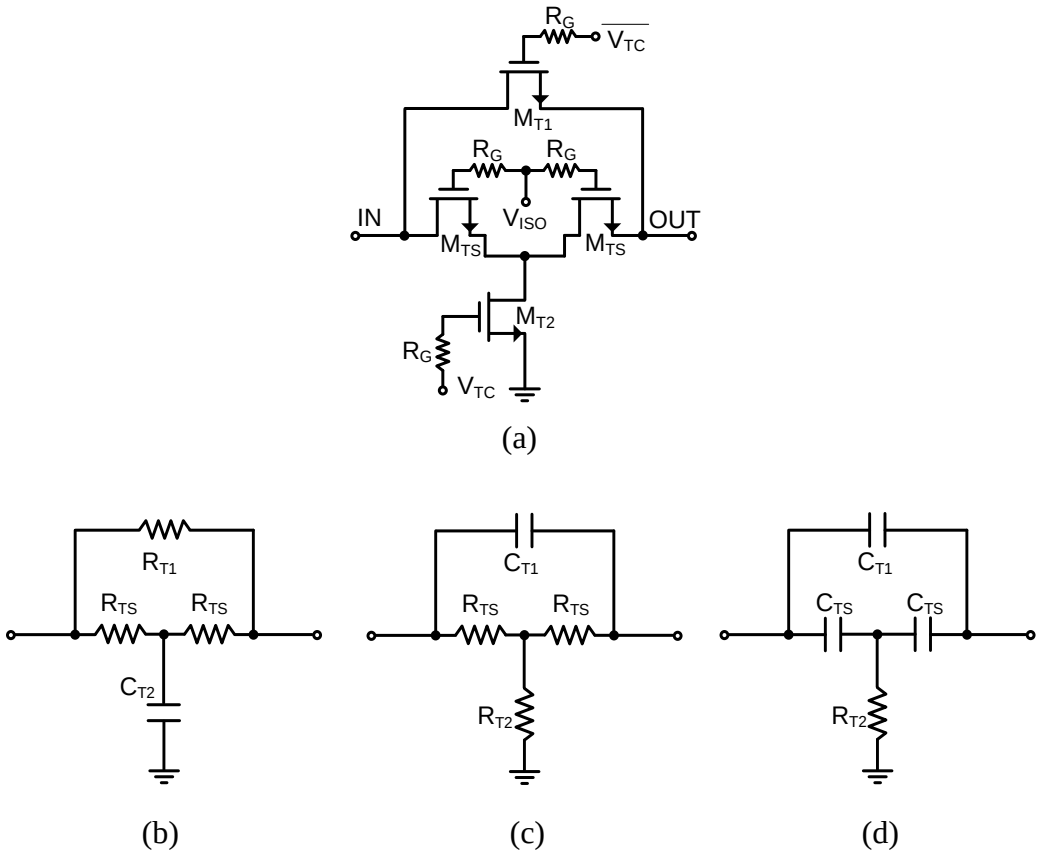


Fig. 4.13. (a) A switching 1-bit T-attenuator and its equivalent circuit at (a) a reference/switching-on, (b) attenuation, and (c) isolation/switching-off state.

$R'_{eq1}>R_{eq1}$ and $R'_{eq2}>R_{eq2}$) and better flatness (from $C_{eq1}>C'_{eq1}$ and $C_{eq2}>C'_{eq2}$) than that containing the normal transistors. To verify this, two 16-dB Pi-attenuators at a reference state, one with normal and another with body-floated transistors, are simulated and shown in Fig. 4.12. As can be seen, the attenuator designed with the body-floating technique has the flatness of 0.6 dB over 10–67 GHz and insertion loss of 2 dB at 30 GHz, while that using normal transistors has 2.5-dB flatness and 3.6-dB insertion loss at 30 GHz. This is a significant improvement in attenuator design. Similar improvement in other attenuator

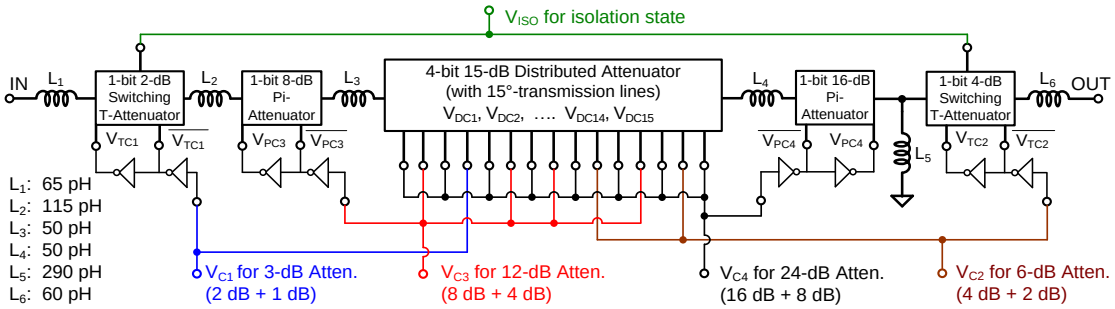


Fig. 4.14. Diagram of the 4-bit switching Pi/T-distributed attenuator.

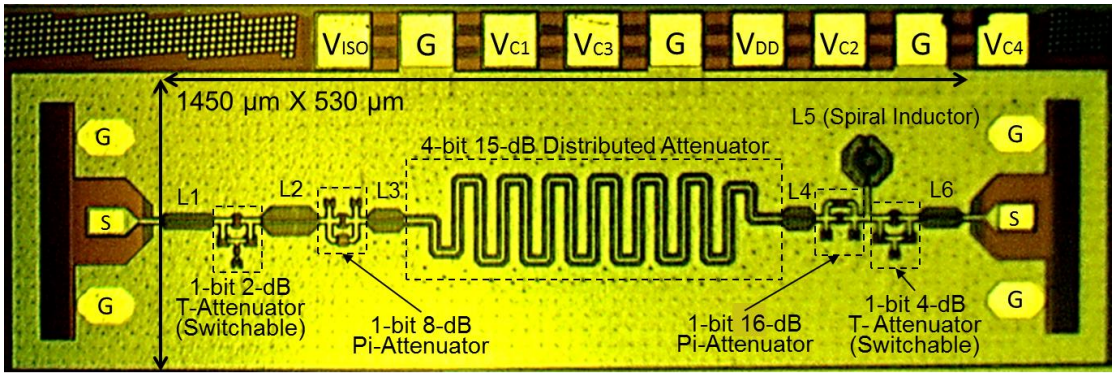


Fig. 4.15. Micrograph of the 4-bit switching Pi/T-distributed attenuator.

designs such as T-, distributed, and Pi/T-distributed attenuators can also be achieved by implementing the body-floating technique.

4.2.3 Dual-Function of Attenuating and Switching

Fig. 4.13(a) shows a schematic of a switching T-attenuator that can perform both attenuation and switching. Fig. 4.13(b)-(d) shows its equivalent circuit at a reference (switching-on), attenuation, and isolation (switching-off) state. The switching function is achieved by simply replacing the series resistor (R_{TS}) of the conventional T-attenuator with

a transistor (M_{TS}) and biasing V_{ISO} through a large resistor (R_G). The size of M_{TS} is determined by the on-resistance chosen for the desired attenuation performance. A similar approach can be used to achieve the dual function of switching and attenuating for other attenuator types. It is noted that the use of a switching function superimposed on an attenuation function enables the reflective switching required in our design, as opposed to the absorptive switching using the maximum attenuation.

4.3 Pi/T-Distributed Attenuator Design

Fig. 4.14 shows the diagram of the new 4-bit switching Pi/T-distributed attenuator designed based on the discussion in Section III. It consists of two 1-bit T-attenuators (2- and 4-dB), two 1-bit Pi-attenuators (8- and 16-dB), and a 4-bit 15-dB distributed attenuator having short transmission lines of 15° (at 30 GHz) in cascade. The constituent distributed attenuator and the Pi-attenuator (or/and T-attenuator) can be actuated simultaneously at each attenuation state to achieve improved flatness and attenuation range across a wide frequency range as mentioned in Section III-A. It is recalled that the attenuation-flatness compensation is achieved through opposite slopes of the attenuation curves for the Pi-/T-attenuator and distributed attenuator. These slopes are mainly controlled by the sizes of the series transistors in the Pi-/T-attenuator and the lengths of the transmission lines in the distributed attenuator. As the compensation ultimately depends on the slope cancellation between these attenuators, it is very difficult to derive an analytical solution enabling both the transistor sizes and transmission-line lengths to be determined. The most effective way, as far as design is concerned, is to conduct a numerical analysis/simulation on the

Pi/T-distributed attenuator to select proper transistor sizes and transmission-line lengths that lead to optimum attenuation flatness over frequency. This can be done relatively easy during the design process. Particularly, the 2- and 4-dB T-attenuators are used at the first and last stage of the switching Pi/T-distributed attenuator to attain the switching function mentioned in Section III-C. The control voltages of the attenuator constituents are linked in particular ways for V_{C1}, V_{C2}, V_{C3}, and V_{C4} corresponding to 3, 6, 12, and 24-dB attenuation, respectively, as shown in Fig. 4.14. Specifically, the control voltages of the distributed attenuator constituent are combined and selected to make the electrical length gradually shorter as the attenuation state is increased. This leads to not only opposite attenuation slopes to those of the Pi-/T-attenuator as seen in Figs. 4.16(a) and (b), but also gradual flatness degradation as the attenuation state is increased as shown in Fig. 4.16(b), ultimately leading to improved flatness and attenuation range for the Pi/T-distributed attenuator. The series/shunt inductors (L_1–L_6) are used for matching purpose, and their approximate values are listed in Fig. 4.14. The series inductors (L_1–L_4 and L_6) cause more resistance and hence more loss, especially at high frequencies. These inductors degrade the flatness at low attenuation states while, at high attenuation states, they help improve the flatness due to the increasing loss with frequency. The shunt inductor (L_5) causes more rejection of the low-frequency signals while not affecting much the high-frequency signals, thereby resulting in better flatness, especially in the low-frequency region. DC inverters are also employed to digitally control the voltages of the Pi- and T-attenuator. Table 4.2 shows the targeted attenuations and corresponding control voltages of the attenuator for all attenuation states. In the table, the 4-bit Pi/T-attenuator signifies the two

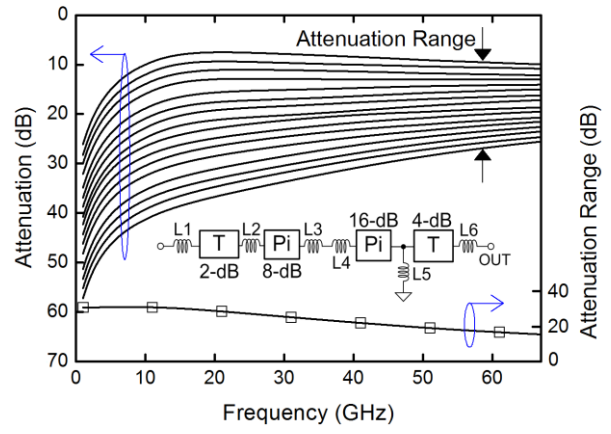
Table 4.2 Control voltages and target attenuations at all states.

States	V_{C1}	V_{C2}	V_{C3}	V_{C4}	V_{ISO}	Attenuation [dB]		
						Combined Pi- and T-attenuator (4-bit)	Distributed attenuator (4-bit)	Switching Pi/T-distributed attenuator (4-bit)
1	X	X	X	X	O	0	0	0
2	O	X	X	X	O	2	1	3
3	X	O	X	X	O	4	2	6
4	O	O	X	X	O	6	3	9
5	X	X	O	X	O	8	4	12
6	O	X	O	X	O	10	5	15
7	X	O	O	X	O	12	6	18
8	O	O	O	X	O	14	7	21
9	X	X	X	O	O	16	8	24
10	O	X	X	O	O	18	9	27
11	X	O	X	O	O	20	10	30
12	O	O	X	O	O	22	11	33
13	X	X	O	O	O	24	12	36
14	O	X	O	O	O	26	13	39
15	X	O	O	O	O	28	14	42
16	O	O	O	O	O	30	15	45
Isolation	O	O	O	O	X	N/A	N/A	N/A

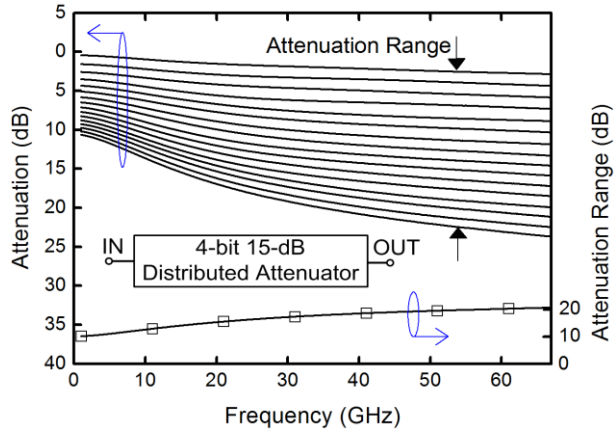
[O: ON (= 1.8 V) and X: OFF (= 0 V)]

Pi-attenuators and the two switching T-attenuators in cascade as indicated in Figs. 4.14 and 4.16(a).

Fig. 4.15 shows the photomicrograph of the CMOS 4-bit switching Pi/T-distributed attenuator fabricated with TowerJazz 0.18-μm BiCMOS technology [4-19]. The attenuator occupies 1450 μm×530 μm excluding on-wafer pads. All transistors in the attenuator are designed with DNW and body floating. The area of the DNW in the layout is drawn as small as possible within the design rule/restriction. This is necessary because the p-n and n-p junction capacitances are proportional to the area, and large junction capacitances lead to more RF leakages through the substrate which cause large attenuation fluctuation and



(a)



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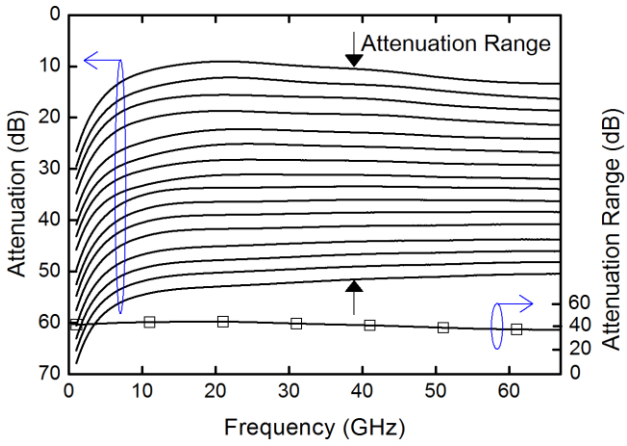


(c)

Fig. 4.16. Simulated attenuation and attenuation range of the combined 4-bit 30-dB Pi- and T-attenuator (a), 4-bit 15-dB distributed attenuator (b), and 4-bit 45-dB switching Pi/T-distributed attenuator (c).

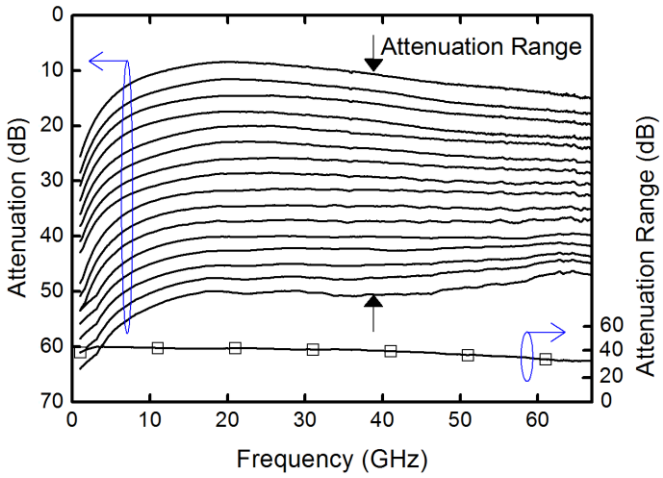


Fig. 4.17. Measured attenuation and attenuation range of the 4-bit switching Pi/T-distributed attenuator.

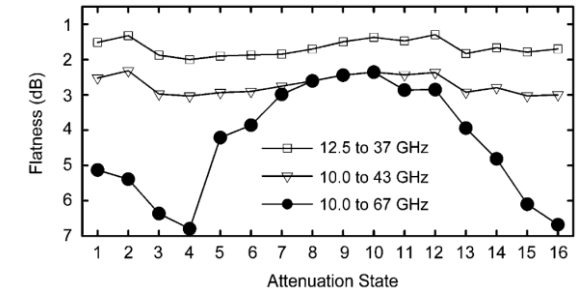
high insertion loss. Furthermore, the attenuator is laid out using coplanar waveguide (CPW) structure to confine the fields within the Oxide layers, hence reducing the penetration of the electric fields into the substrate which effectively reduces the substrate loss, and hence improved quality factor (Q), and mutual coupling between adjacent components. Well-defined ground planes are also implemented in the layout to minimize the interference among adjacent elements. All matching inductors, except L_5, are designed with CPW transmission lines considering size and Q factor.

All inductors and interconnections in the 4-bit switching Pi/T-distributed attenuator were simulated with the EM simulator IE3D [4-20].

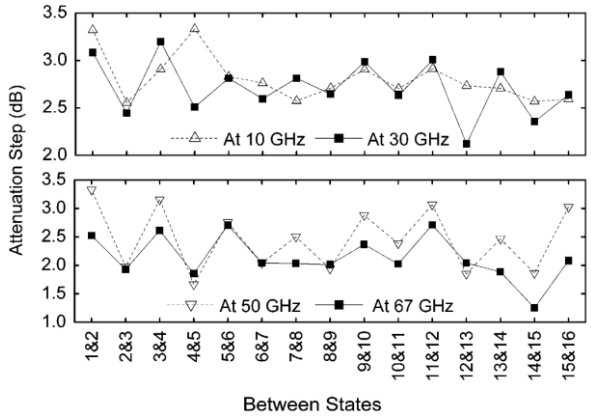
4.4 Simulated and Measured Results

Fig. 4.16 shows the simulated attenuations and attenuation ranges of the combined Pi- and T-attenuators, distributed attenuator, and switching Pi/T-distributed attenuator.

The attenuation range of the combined Pi- and T-attenuator decreases at higher frequencies, as seen in Fig. 4.16(a), due to the fact that the impedances of its series off-capacitances and shunt off-capacitances become smaller at higher frequencies, forcing some signals to go through these instead of the attenuation cell (at high attenuation states) and the resistors in the Pi- and T-attenuator shown in Fig. 4.5 (at low attenuation states). On the other hand, the attenuation range of the distributed attenuator as shown in Fig. 4.16(b) increases as frequency is increased since the electrical distance between the shunt transistors become closer to 90º at higher frequencies in the frequency band from 0 to 67 GHz. The increased attenuation range of the distributed attenuator also results from the fact that, as the attenuation state is increased, the electrical distance reduces, causing increasing slope for the attenuation curve. It is also observed that the attenuation curves at lower attenuation states are flatter than those at higher attenuation states as seen in Figs. 4.16(a) and (b). For the combined Pi- and T-attenuator, there is less number of series off-capacitances at lower attenuation states, which leads to less leakage through these capacitances and more signals going through the attenuation cells. The series off-capacitance (C_{T1}) in the T-attenuator is typically larger than that (C_{P1}) in the Pi-attenuator for the same attenuation. In our attenuator design, however, we use the T-attenuator for lower attenuations (2 and 4 dB) and Pi-attenuator for larger attenuations (8 and 16 dB). Lower attenuation requires smaller series resistance and hence smaller-size transistor, which also has smaller off-capacitance. On the other hand, larger attenuation requires large series resistance and hence larger transistor which has larger off-capacitance. As a result,



(a)



(b)

Fig. 4.18. Measured (a) flatness and (b) attenuation step of the 4-bit switching Pi/T-distributed attenuator.

the difference between C_{T1} (for small attenuation) and C_{P1} (for large attenuation) becomes small. The less number of series capacitances coupled with a small difference between C_{T1} and C_{P1} hence lead to slightly increased or flat attenuation as can be seen in Fig. 4.16(a) for the first three attenuation states of the combined Pi- and T-attenuator. For the distributed attenuator, it is noted that the use of small-size shunt transistors (3.5 μm) in the design allows the influence of the shunt off-capacitances to be ignored, and hence for the lower attenuation states of the distributed attenuator with proper locations for on-transistors, the transmission lines between the shunt on-resistances can be combined as

one long transmission line approaching 90 degrees, thereby resulting in better attenuation flatness, as seen in Fig. 4.16(b), and matching. As the opposite attenuation-range slopes, as displayed in Figs. 4.16(a) and (b), are combined in the switching Pi/T-distributed attenuator, flatter attenuation and larger attenuation range are expectedly achieved as seen in Fig. 4.16(c). It is noted that the combined Pi- and T-attenuators are designed to have larger attenuation range than the distributed attenuator as seen in Fig. 4.16(a), (b) and Table 4.2. Such design is preferred because, for high attenuation range, the size of the Pi/T-attenuator remains essentially the same, whereas that of the distributed attenuator increases substantially due to the need of more transmission lines. Fig. 4.16(b) also shows that the insertion loss of the distributed attenuator is 1.8 dB at 30 GHz, which is much smaller than that of the Pi/T-attenuator. This low insertion loss is due to the absence of series transistors or resistors. The shorter transmission lines also contribute to the lower loss.

The 4-bit switching Pi/T-distributed attenuator was measured on-wafer. Fig. 4.17 shows the measured attenuation and attenuation range of the switching Pi/T-distributed attenuator. The insertion loss is 9.3 dB at 30 GHz, and the maximum and minimum attenuation ranges over 10–67 GHz are 42 dB and 32 dB, respectively. The measured attenuation and attenuation range agree reasonably well with the simulation results in Fig. 4.16(c). Smaller measured attenuation range above 50 GHz is due to unexpected parasitics at high frequencies. The measured flatness and attenuation step as a function of the attenuation state and between states are plotted in Fig. 4.18, respectively. As can be seen in Fig. 4.18(a), the flatness over 10–67 GHz is 2.4–6.8 dB, while over 12.5–37 GHz and

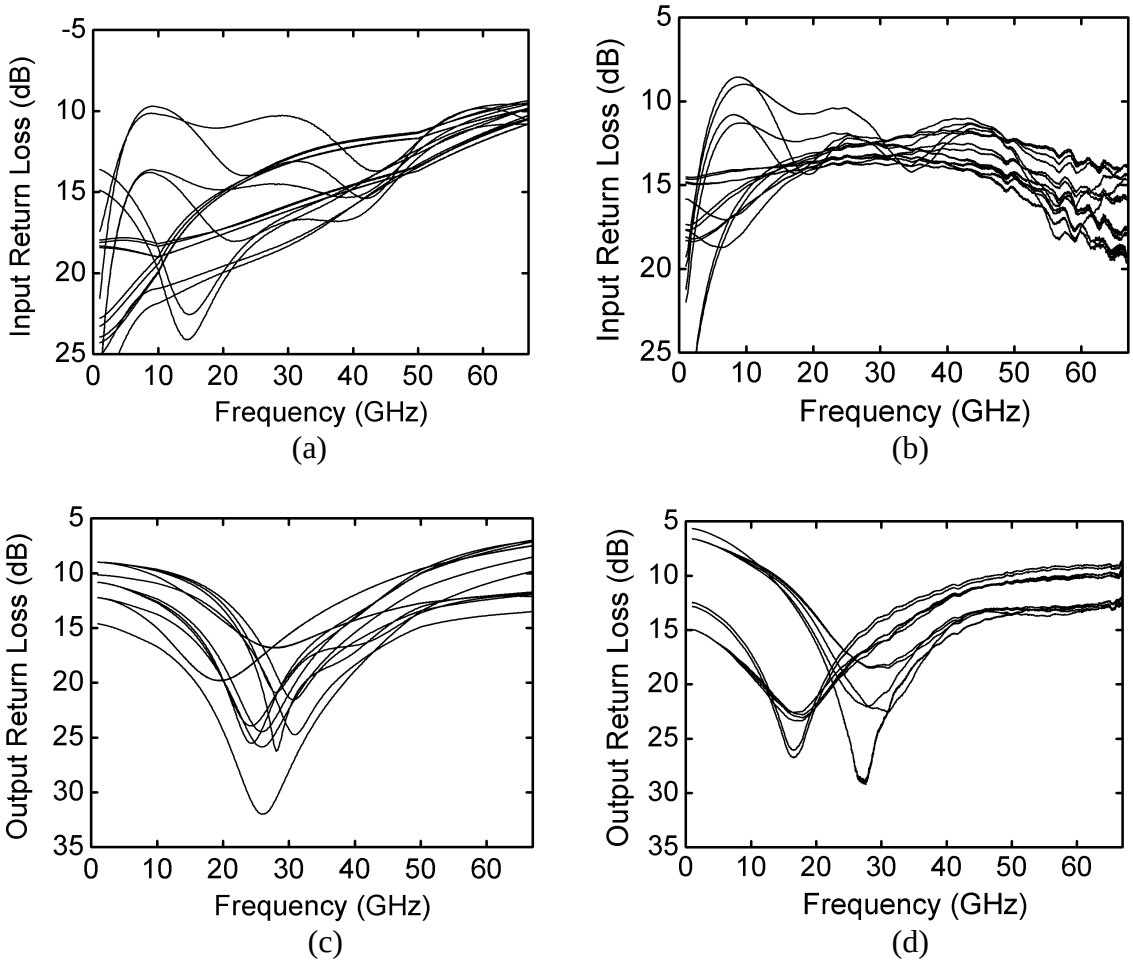


Fig. 4.19. Input (S11) and output (S22) return losses of the 4-bit switching Pi/T-distributed attenuator: (a) Simulated S11, (b) measured S11, (c) simulated S22, and (d) measured S22.

10–43 GHz, only 2- and 3-dB flatness are achieved, respectively. The design attenuation step is 3 dB as indicated in Table 4.2. The measured results in Fig. 4.18(b) show that the attenuation steps at 50 and 67 GHz are smaller than 3 dB on average, and those at 10 and 30 GHz are 2.95±0.35 dB and 2.65±0.55 dB, respectively. It is noted that, although 1-dB attenuation step could be made possible with proper control voltages, it was not done in the designed attenuator to enable us to utilize both the Pi/T and distributed constituents

together to compensate for the attenuation variations over frequency. Fig. 4.19 shows the simulated and the measured input and output return losses for the 16 attenuation states. The worst measured input and output return losses over 10–67 GHz are 8.7 and 8.5 dB, respectively. The isolation in the isolation (switching-off) state of the switching Pi/T-distributed attenuator is shown in Fig. 4.20, indicating reasonably good agreement between the measured and simulated results over 10–67 GHz with measured isolation from 43 to 67 dB. It is observed in Figs. 4.17 and 4.20 that, while the isolation from DC to 15 GHz is higher than the maximum attenuation, they are almost the same after 15 GHz. This is due to the fact that the impedances of the off-capacitance C_{TS} and the on-resistance R_{TS} of the series transistors M_{TS} as shown in Fig. 4.13(b) are almost the same after 15 GHz. It is, however, not desired to use the maximum attenuation state as the isolation state since the switch is designed to function as a reflective instead of an absorptive switch as mentioned in Section IIIC. Fig. 4.21 shows the measured and simulated attenuation for the 1st, 2nd, 4th, 8th, 10th, 12th, 14th, and 16th attenuation states versus input power at 40 GHz which match reasonably well to each other. The worst measured 1-dB power compression point (P1dB) is 14 dBm at the 1st attenuation state. It is particularly noted that, as compared to [4-9], the designed attenuator provides very constant attenuations and hence constant maximum attenuation range over a large input power range for all attenuation states. This phenomenon is due to two reasons. The first reason is the use of the DNW transistors and body-floating technique which enhance the power handling capability. The second reason, which is the primary reason, is the use of the 2-dB T- and 8-dB Pi-attenuators in front of the distributed attenuator, which attenuate the input power,

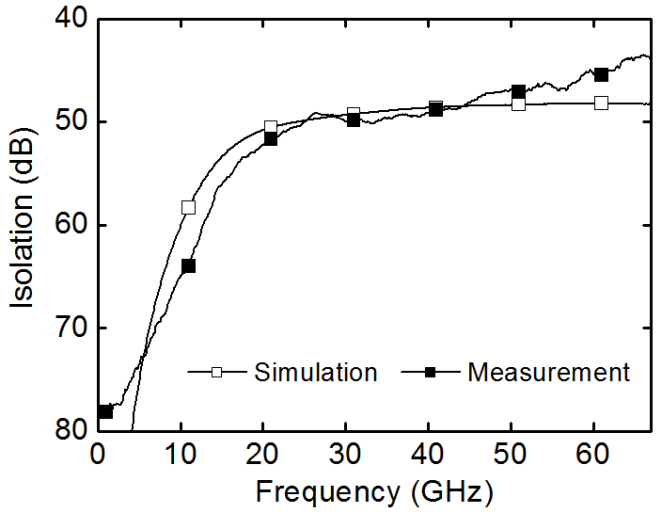
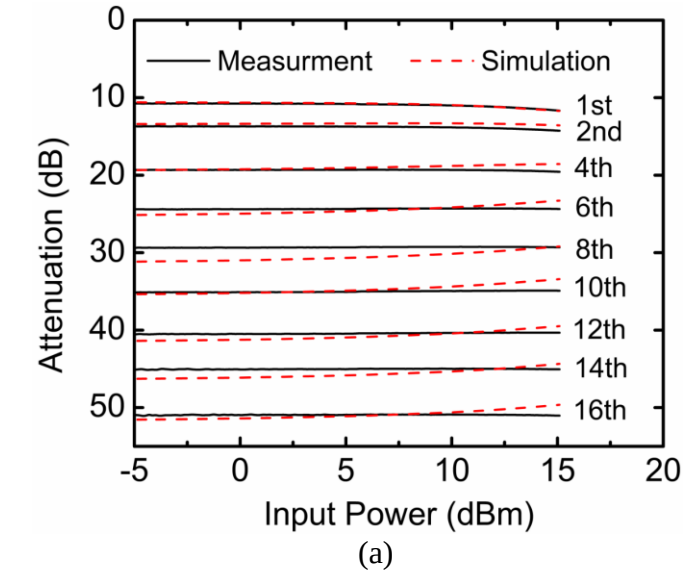


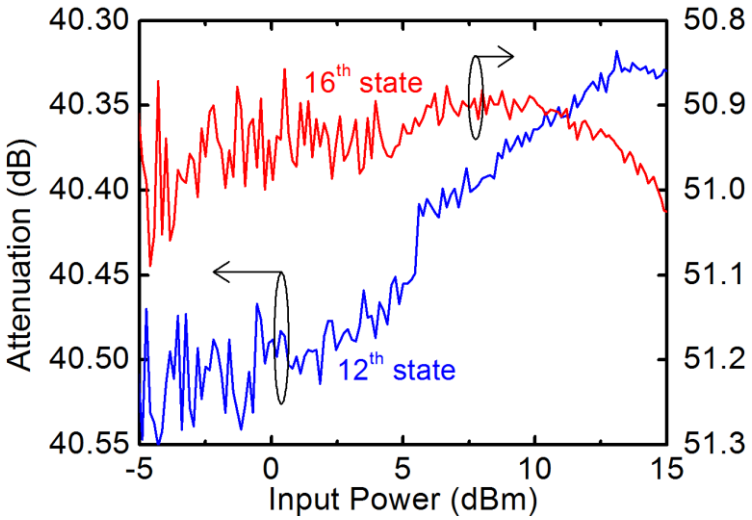
Fig. 4.20. Simulated and measured isolations of the 4-bit switching Pi/T-distributed attenuator in isolation state.

hence resulting in a small input power to the subsequent distributed attenuator. Consequently, the linearity of the Pi/T-distributed attenuator depends mostly on the 2-dB T-and 8-dB Pi-attenuator which have much higher power handling capability than the distributed attenuator as confirmed by our simulations. Ultimately, the power handling of the Pi/T-distributed attenuator is higher than that of the distributed attenuator, which leads to constant attenuation and hence constant maximum attenuation range across a wide input power range as seen in Fig. 4.21. We have also measured the power handling at different frequencies. At 20, 25, 35, and 60 GHz, the worst measured P1dB are 13, 14, 15, and 10 dBm, respectively.

It is noted that, while the phase deviation of attenuators and, in general, of any other components is important in phase-sensitive systems such as phased arrays. The designed attenuator, however, is not intended for these applications; it is designed for



(a)



(b)

Fig. 4.21. Simulated and measured power handling for different attenuation states at 40 GHz. (a) and expansion of the measured results for the 12th and 16th attenuation state (b).

amplitude control of signals across an ultra-wide bandwidth without considering the phase performance.

Table 4.3 compares the performance of the designed attenuator to those of reported

CMOS/BiCMOS attenuators. The designed attenuator demonstrates the best performance in terms of attenuation flatness, bandwidth, attenuation range, and power handling across 10-67 GHz. It is also the only attenuator that is capable of reflective switching across 10-67 GHz.

4.5 Conclusion

A new design is proposed for attenuators to achieve improved attenuation flatness and range as well as switching functionality. The new design exploits the inherently opposite frequency-response slopes of the attenuation of the conventional Pi-, T- and distributed attenuators. Additionally, the body-floating technique for transistors is also studied and implemented to further improve the attenuation flatness and transmission performance through reduction of the substrate influence. The CMOS dual-function switching 4-bit attenuator consisting of cascaded Pi-, T- and distributed attenuators with DNW transistors having body floated is realized using a 0.18-μm BiCMOS technology and works well across 10-67 GHz in both attenuation and switching functions as designed. The developed attenuator is attractive for signal amplitude control in wideband microwave and millimeter-wave communication and radar systems, especially those requiring switching together with attenuation.

Table 4.3 Comparison of CMOS/BiCMOS attenuators

Ref.	Freq. (GHz)	Flatness (dB)	Atten. Range (dB)	Insertion Loss (dB)	Return Loss (dB)	Number of States	Step (dB)	Reflective Switching	Input P1dB (dBm)	Process
[1]	8–12 (Type 1)	< 1.2	30–31.5	8–9.3	> 10	64 (6-bit)	0.5	None	15 (at 10 GHz)	0.18-μm CMOS
	DC–14 (Type 1)	< 6.5		3.7–10	> 9			None		
	8–12 (Type 2)	< 1.5		9.8–11.3	> 11			None	13 (at 10 GHz)	
[9]	10–50	< 5	8.2–11	2-3	> 9.1	11	0.9± 0.25	None	4 (at 35 GHz)	0.12-μm BiCMOS
[18]	0.4–3.7	< 2.6	30–33	0.96–2.91	> 9	8 (3-bit)	3±2	None	> 7.5 (at 1.95 GHz) > 7 (at 1GHz) > 6 (at 700 MHz)	0.18-μm CMOS
[21]	DC–2.5	2.6 (at Max. Atten. State)	39–42	0.9–3.5	> 8.2	Not Available (N/A)	N/A	None	2.5	0.13-μm CMOS
This Work	10–67	< 2 (12.5–43 GHz) < 3 (10–43 GHz) < 6.8 (10–67 GHz)	32–43	8.4–15.2	> 8.7	16 (4-bit)	2.9± 0.1	43–67 dB Isolation (10–67 GHz)	> 13 (at 20 GHz) > 14 (at 25 GHz) > 15 (at 35 GHz) > 14 (at 40 GHz) > 10 (at 60 GHz)	0.18-μm BiCMOS

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CHAPTER V

CMOS HIGH-ISOLATION SPDT SWITCH WITH BAND-PASS-FILTER RESPONSE

A CMOS high-isolation single-pole-double-throw (SPDT) switch with a band-pass filtering response is designed for the phased-array transmitter in Fig. 5.1. By shortening the channel length of the CMOS transistor, we can improve the overall RF switch performances. However, the inherent low electron mobility of the silicon-based transistors still leads to poorer switch performances in comparison with the III-V semiconductor-based transistors, especially at high frequencies. High isolation and low insertion loss are primary performances for the RF switch design. However, there is an inherent trade-off between them in general switch design. Fig. 5.2 shows the trade-off of a shunt RF switch (a series switch also has the similar trade-off.) For example, to improve the isolation, we can increase the size of the transistor but it leads to large off-capacitance (C_{off}), which causes more insertion loss especially at higher frequencies. So, intuitively we know that the trade-off can be eliminated by removing the effect of C_{off} at the switching-on state, which is realized by employing a band-pass filter (BPF) topology. Various techniques for designing CMOS switches have been investigated [5-1]–[5-4]. In [5-1] and [5-2], the leakage cancellation techniques are employed for the high isolation without significant insertion loss increase, but it demands additional phase shift circuits. In [5-3], the insertion loss and isolation are both improved by increasing the substrate impedance, but the effect is insignificant. In [5-4], a low insertion loss is achieved by using minimum

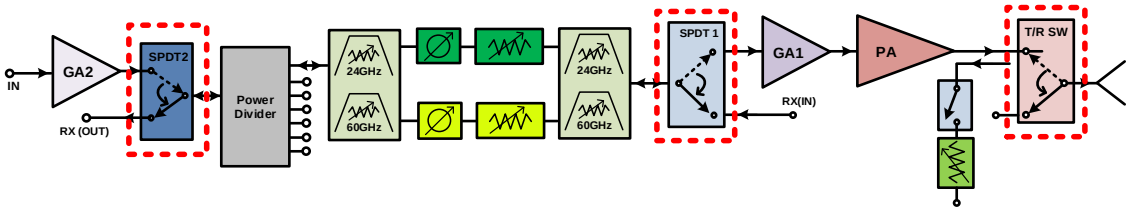


Fig. 5.1. Switches in the phased-array transmitter (in the dotted boxes).

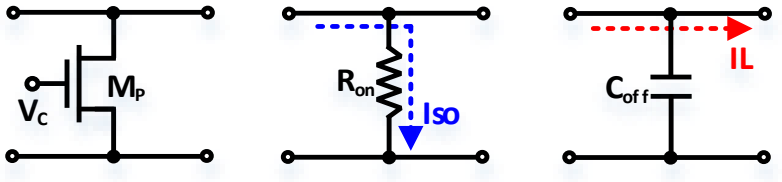


Fig. 5.2. Shunt RF switch and its switching-off and switching-on states.

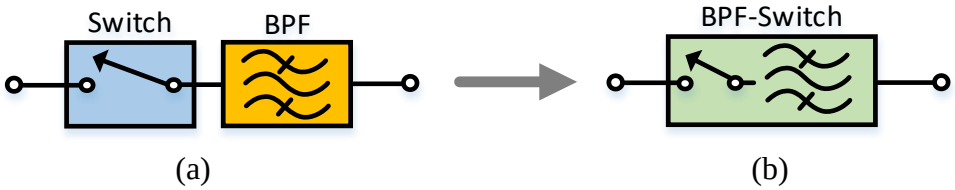


Fig. 5.3. Band-pass filtering and switching functions realized with (a) cascaded switch and BPF and (b) switch having dual-function of switching and band-pass filtering.

shunt transistors without a series transistor, but the topology used is not suitable for the high-isolation switch design.

This chapter presents a new high-isolation single-pole-single-throw/single-pole-double-throw (SPST/SPDT) switch, which is designed based on a BPF topology. The proposed design significantly mitigates the trade-off between the isolation and insertion loss because a large shunt off-capacitance, which is occurred from the large size of transistor used for a high-isolation performance, is absorbed into the constituent BPF without increasing the insertion loss especially at high frequencies. Also, the proposed

switch contains band-pass filtering response as a dual-function circuit, which is named BPF switch. Fig. 5.3(a) and (b) show a conventional BPF and switch connected in cascade and the proposed BPF switch, respectively. The proposed BPF switch has a smaller size, lower insertion loss, and higher isolation than the conventional counterpart. The filtering function added will suppress the undesired harmonics and intermodulation products in the phased-array transmitter.

5.1 Design

5.1.1 Band-pass filter topology for high-isolation SPST switch design

Fig. 5.4 shows an n-order J-inverter BPFs consisting of J-inverters and shunt susceptances (β). Inductive J-inverter is used in Fig. 5.4(a), and the elements are derived as

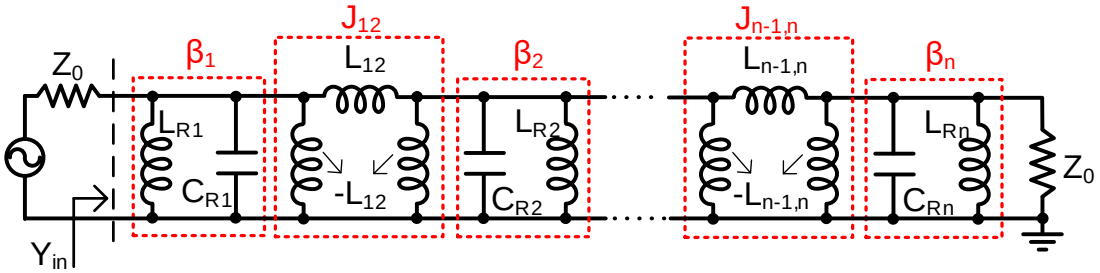
$$C_{Rj} = \frac{\omega'_1 g_0 g_1}{Z_0 \omega_0 W} \tag{5.1}$$

$$L_{Rj} = \frac{1}{C_{Rj} \omega_0^2} \tag{5.2}$$

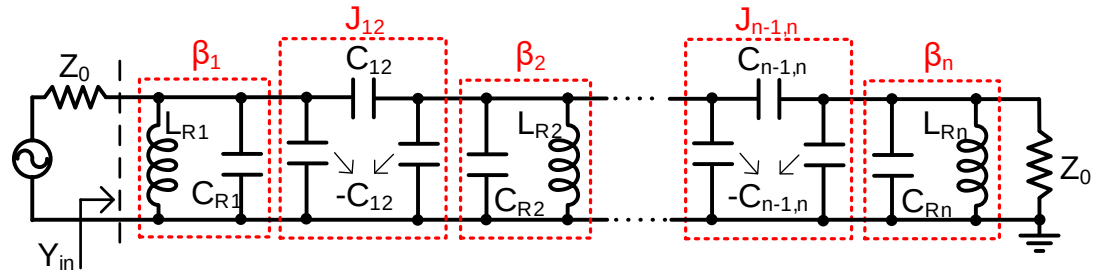
$$J_{k-1,k} = \frac{W}{\omega'_1 \omega_0} \sqrt{\frac{1}{g_{k-1} g_k L_{Rk-1} L_{Rk}}} \tag{5.3}$$

$$L_{j-1,j} = \frac{1}{\omega_0 J_{j-1,j}} \tag{5.4}$$

where j=1, 2, 3, … n-1, n and k= 2, 3, … n-2, n-1. g_0–g_{n+1} are the parameters of the low-pass prototype filter. n, Z_0, ω_0 and ω_2 denote the number of order, terminating impedance, center frequency, and upper-pass-band cut-off frequency of the BPF, respectively. W represents the bandwidth of the BPF. ω'_1 is the upper-pass-band cut-off frequency of the



(a)



(b)

Fig. 5.4. *n*-order BPF with (a) inductive and (b) capacitive J-inverter Pi-networks.

low-pass prototype filter and $\omega'_1=1$ is assumed. The adjacent shunt inductors (L_{R1} and L_{12}) are merged. Similarly, the BPF with capacitive J-inverters in Fig. 5.4(b) can be calculated with

$$C_{Rj}=\frac{\omega'_1 g_0 g_1}{Z_0 \omega_0 W} \tag{5.5}$$

$$L_{Rj}=\frac{1}{C_{Rj}\omega_0^2} \tag{5.6}$$

$$J_{k-1,k}=\frac{\omega_0 W}{\omega'_1}\sqrt{\frac{C_{Rk-1}C_{Rk}}{g_{k-1}g_k}} \tag{5.7}$$

$$C_{j-1,j}=\frac{J_{j-1,j}}{\omega_0} \tag{5.8}$$

The adjacent shunt capacitors in the BPF in Fig. 5.4(b) are merged and can be expressed as

$$C_{P1} = C_{R1} - C_{12} = \left(\frac{1}{W} - \sqrt{\frac{1}{g_1 g_2}} \right) \frac{g_0 g_1}{Z_0 \omega_0} \tag{5.5}$$

$$C_{Pn} = C_{Rn} - C_{n-1,n} = \left(\frac{1}{W} - \sqrt{\frac{1}{g_{n-1} g_n}} \right) \frac{g_0 g_1}{Z_0 \omega_0} \tag{5.6}$$

$$C_{Pk} = C_{Rk} - C_{k-1,k} - C_{k,k+1} = \left(\frac{1}{W} - \sqrt{\frac{1}{g_{k-1} g_k}} - \sqrt{\frac{1}{g_k g_{k+1}}} \right) \frac{g_0 g_1}{Z_0 \omega_0} . \tag{5.7}$$

From (5.1) and (5.5)–(5.7), it is noted that the shunt capacitances in the BPFs are increased when the bandwidth of the BPF (W) is reduced. By replacing the shunt capacitors with nMOS transistors (M_{P1}, M_{P2}, … M_{Pn}) as shown in Fig. 5.5(a) and (b), the proposed SPST switches with a band-pass filtering response are designed. The transistors are turned off and on with the control voltage, V_C, at the on and off states of the SPST switches, respectively. The off-capacitances of the transistors substitute for the shunt capacitors at the on-state of the switch, while the on-resistances act as the drain paths at the off state for the isolation increase. The gate-widths of the transistors are determined by the calculated capacitances with (5.1) and (5.5)–(5.7). So, it is intuitively expected that by reducing the bandwidth, we can have a wide gate-width, which leads to a small on-resistance in the switch design, and hence increasing the isolation of the switches in Fig. 5.5. In typical switch topologies [5-1], [5-3], [5-4], the shunt off-capacitances are considered as undesired parasitics and compensated for by adding shunt/series inductors, which lead to increased insertion loss. However, in our design, the off-capacitances act as parts of the switches providing the band-pass filtering response without any insertion-loss increase.

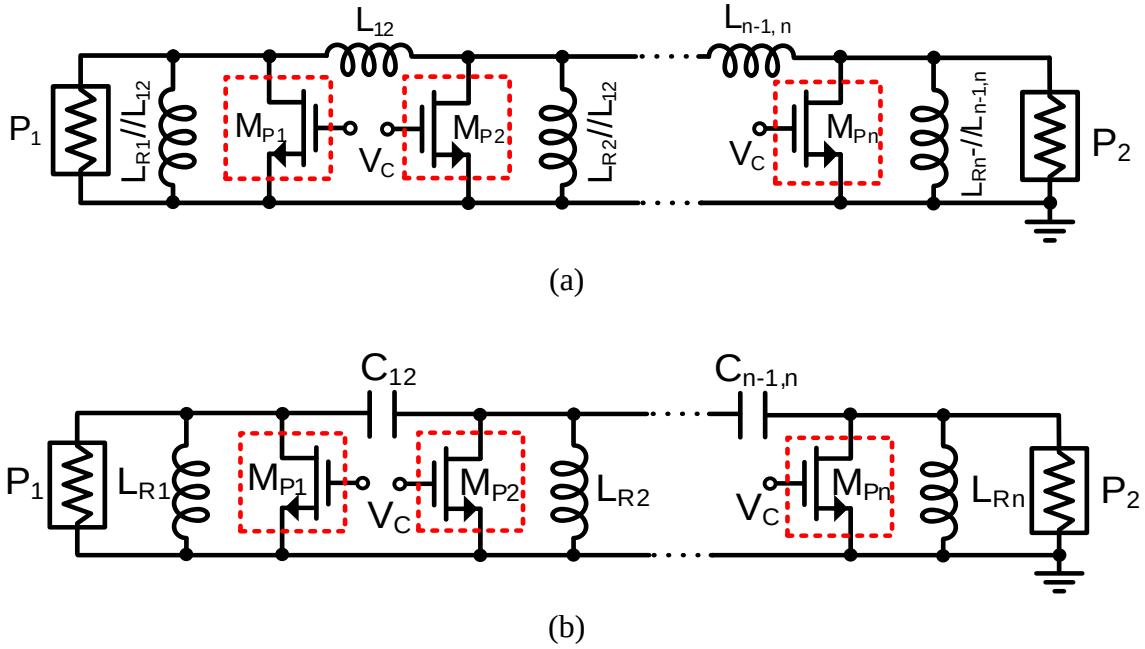
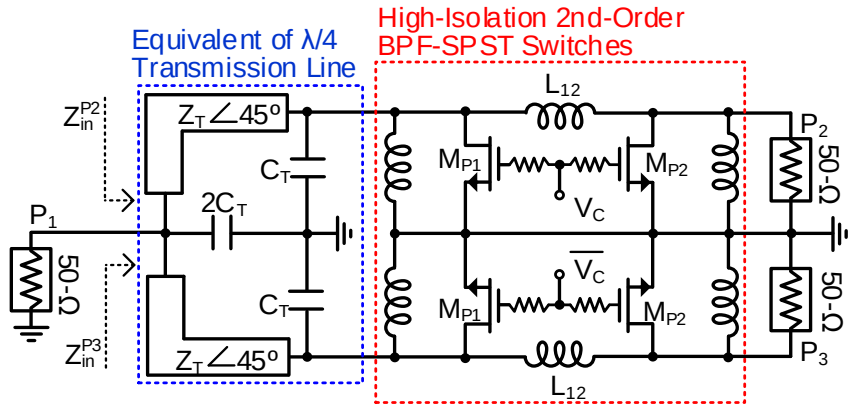


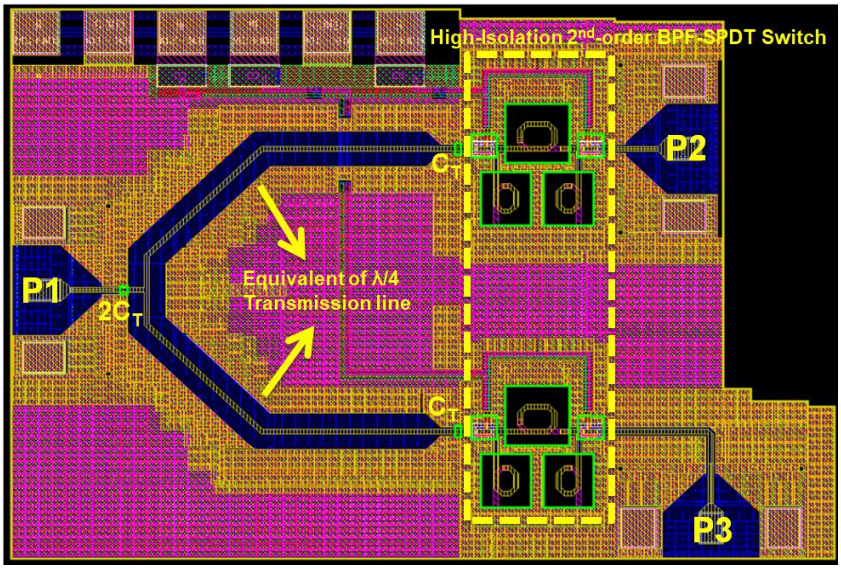
Fig. 5.5. SPST switch with band-pass filtering response whose isolation is increased by reducing the bandwidth.

5.1.2 High-isolation SPDT switch with band-pass filtering response

With the proposed SPST switch in the previous chapter, the high-isolation SPDT switch with the band-pass filtering response shown in Fig. 5.6(a) is designed using TowerJazz 0.18-μm BiCMOS technology [5-6]. The BPF-switch is designed with the inductive J-inverter as shown in Fig. 5.5(a). The switch consists of a network equivalent to the λ/4 transmission line at the common input and the high-isolation band-pass SPST switches at the outputs. The equivalent network transforms the input impedance (Z_{in}^{P2} or Z_{in}^{P3}) at the common node into almost 50 Ω or very high (approximately 700 Ω) at the on or off state of the SPDT switch, respectively. For the constituent SPST switches, a 2nd-order



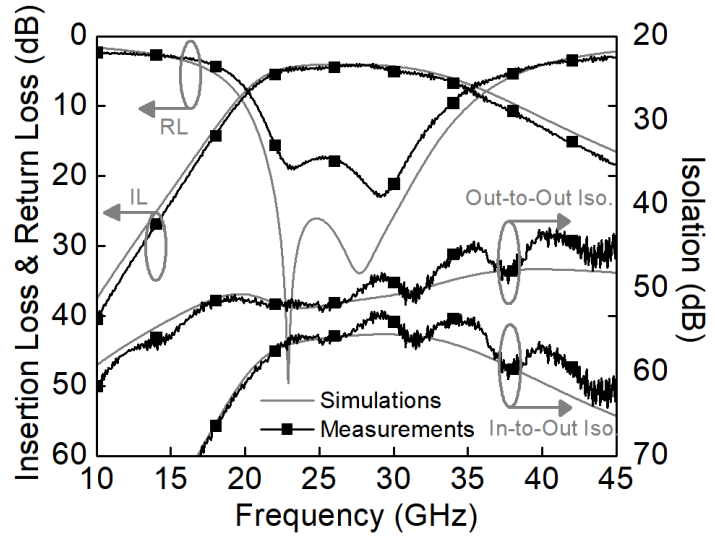
(a)



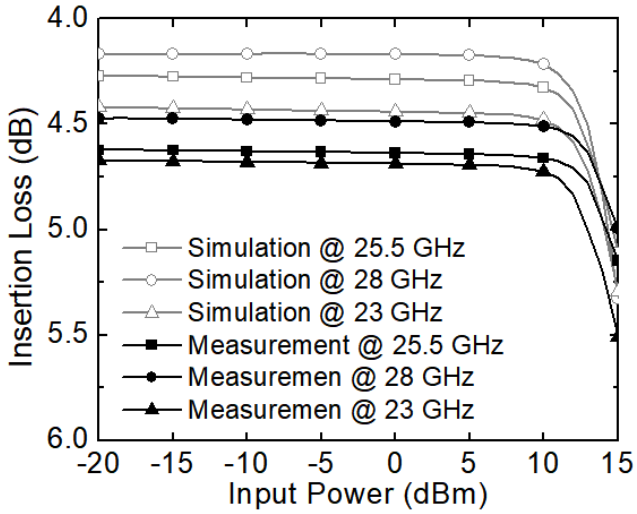
(b)

Fig. 5.6. High-isolation band-pass SPDT switch consisting of equivalents of λ/4 transmission line and high-isolation band-pass SPST switches: (a) schematic and (b) layout. Chip size (core part): 520×600 μm^2.

BPF topology is employed considering the overall isolation, insertion loss, and size. For the control voltage, V_C, 0 and 1.8 V is used to turn the transistors off and on, respectively. The layout of the SPDT switch is shown in Fig. 5.6(b). A 2nd-order 0.01-dB ripple band-



(a)



(b)

Fig. 5.7. Simulations and measurements: (a) insertion loss, return loss and isolations, and (b) power handling at 23, 25.5 and 28 GHz.

pass SPST switch covering 23–28 GHz is employed. Fig. 5.7 shows the post-layout simulations in which the inductors and interconnects are simulated with the EM-simulator IE3D [5-7], and the measured results. Over 23–28 GHz, the measured isolations from

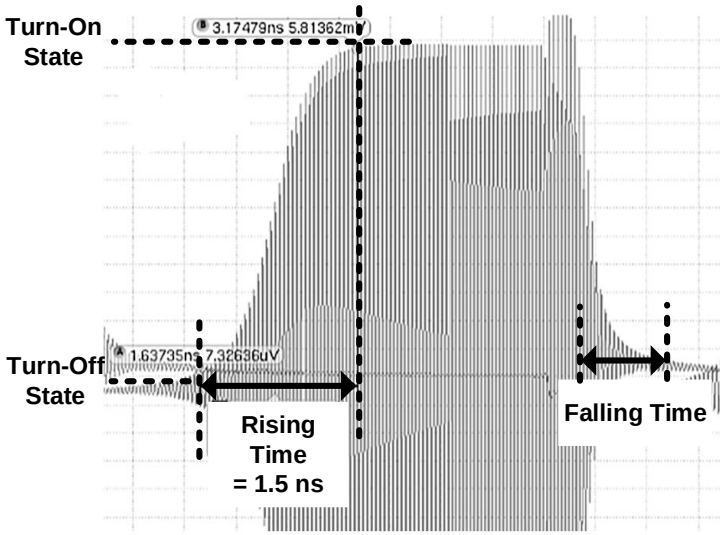


Fig. 5.8. Simulation of switch rising time (turn-on time).

input-to-output and output-to-output, as seen in Fig. 5.7(a), are more than 48 dB and 52 dB, respectively. The measured insertion and return losses are less than 4.7 dB and higher than18 dB over the same band-width, respectively. At 15 and 45 GHz in the stop-band, the measured rejections relative to the insertion loss at the band-edge frequencies (23 and 28 GHz) are 17 and 12 dB, respectively. The measured insertion losses versus input power at 23, 25.5, and 28 GHz seen in Fig. 5.7(b) show that the P1dBs are higher than 15 dBm. Fig. 5.8 shows a rising switching time of the SPDT switch in the simulation. The rising and falling time is faster than 1.5 ns.

5.2 Conclusion

A new high-isolation SPDT switch having band-pass filtering response is proposed. The switch is designed from 23-28 GHz using CMOS devices. The idea for high-isolation and multi-functional filtering response in the switch is validated with the

derived design formulas of the constituent BPF, and simulation and measurement results. The proposed band-pass SPDT switch is attractive for RF/microwave and millimeter-wave communication and radar systems, especially for those demanding both signal switching control and band-pass filtering in a simple single component providing very high isolation performance.

5.3 References

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CHAPTER VI

DESIGN OF CMOS PHASE SHIFTERS WITH SMALL INSERTION-LOSS VARIATION FOR PHASED ARRAYS AND ITS VALIDATION AT 24 GHZ*

Phase shifters are generally employed as a transmission phase control circuit in various communication and radar systems. Phased arrays especially have become an important application of phase shifters in the last few decades. Fig. 6.1 shows the phase shifters in the phased-array transmitter we are designing. The phase shifters in phased array systems play a key role in steering an electronic beam. Low insertion-loss variation of phase shifters across different states is an important requirement in the phased array system design. The low insertion-loss variation helps reduce the variation of a signal controlled by the attenuator used in shaping the amplitude distribution in phased arrays. Phase shifters having low insertion losses also make it possible to design phased arrays without additional attenuators/variable gain amplifiers, which have fine attenuation/gain steps to compensate for the fluctuating insertion loss caused by the phase shifters. Some techniques have been proposed to reduce the insertion-loss variation of phase shifters [6-1]–[6-2]. These designs, however, have relatively large size due to the use of hybrid couplers and hence are not attractive for radio frequency integrated circuits (RFICs) due to expensive silicon real estate.

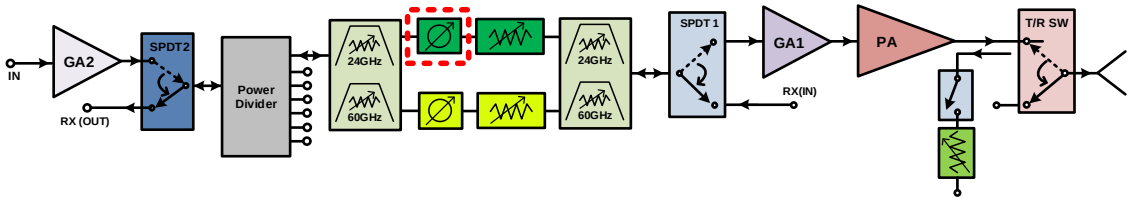


Fig. 6.1. A 24-GHz phase shifter in the phased-array transmitter (in the dotted box)

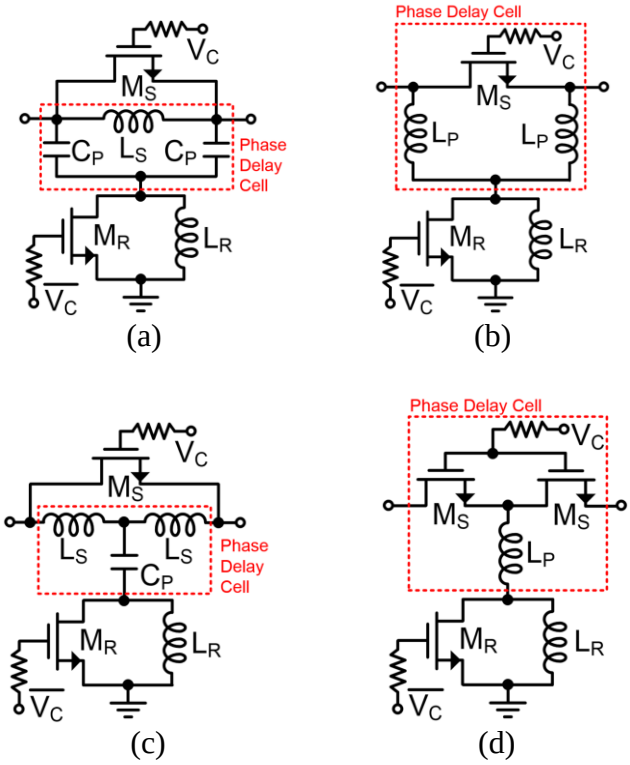


Fig. 6.2. 1-bit phase shifter topologies based on conventional (a) low-pass Pi-, (b) high-pass Pi-, (c) low-pass T-, and (d) high-pass T-type phase delay networks.

A body-floating technique with a deep-nwell layer in CMOS/BiCMOS technology has been used for purposes such as improved insertion loss and its flatness in attenuators [6-3] and enhanced power capability in switches [6-4]–[6-5], etc. The technique is basically used to reduce the undesired influence of the substrate in n-type metal-oxide-semiconductor (nMOS) transistors. It is useful and effective especially in silicon-based

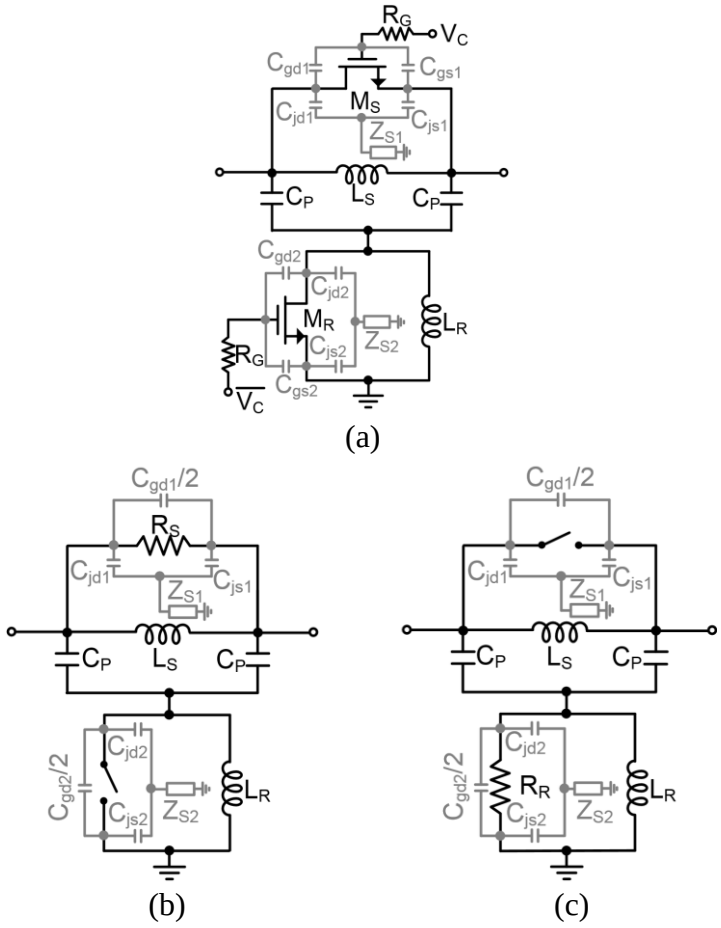


Fig. 6.3. (a) A 1-bit low-pass Pi-type phase shifter with parasitic elements in nMOS transistors, and its equivalent circuits (b) at bypass and (c) phase delay states.

CMOS/BiCMOS transistors, which accompany a lossy substrate. A study of the body-floating technique shows that it could be used to reduce the insertion-loss variation in circuits including phase shifters. Moreover, small insertion-loss variation for phase shifters can also be achieved by optimizing the size of nMOS transistors.

In this chapter, we present an expanded investigation of the body-floating technique and optimum nMOS transistor size for minimizing the insertion-loss variation of phase shifters

[6-6]. The validity of the investigation is confirmed through the performance of a CMOS 4-bit digital phase shifter designed and fabricated using a 0.18-μm BiCMOS technology at 24 GHz. The measurements show an insertion-loss variation of only 13±2.5 dB, root mean square (RMS) amplitude error of 1.7 dB, and input 1-dB power compression (P1dB) greater than 12.5 dBm across different phase states at 24 GHz. The measured input/output return loss greater than 10 dB and RMS phase error lower than 26° over 21 to 27 GHz are also obtained.

6.1 Phase Shifter Design

Fig. 6.2 shows the models of 1-bit phase shifters using switchable nMOS transistors (M_S and M_R) and shunt inductors (L_R). The topologies are based on conventional phase delay networks consisting of low-pass Pi, high-pass Pi, low-pass T and high-pass T. The inductances (L_S and L_P), capacitances (C_P) and off-capacitances of M_S in the phase delay cells in the dotted red boxes in Fig. 6.2 can be calculated with the desired phase delay (θ), operation frequency (f_0), and input/output terminating impedance (Z_0) or admittance (Y_0) for different filter types as

Low-pass Pi-type: $$L_S = \frac{Z_0 \sin\theta}{2\pi f_0} \qquad C_P = \frac{\tan(\theta/2)}{Z_0 2\pi f_0} \tag{6.1}$$

High-pass Pi-type: $$L_P = \frac{Z_0}{2\pi f_0 \tan(\theta/2)} \qquad C_{off} = \frac{\tan\theta}{Z_0 2\pi f_0} \tag{6.2}$$

Low-pass T-type: $$L_S = \frac{\tan(\theta/2)}{Y_0 2\pi f_0} \qquad C_P = \frac{\sin\theta}{Z_0 2\pi f_0} \tag{6.3}$$

High-pass T-type: $$L_P = \frac{Z_0}{2\pi f_0 \sin\theta} \qquad C_{off} = \frac{Y_0}{2\pi f_0 \tan(\theta/2)} \tag{6.4}$$

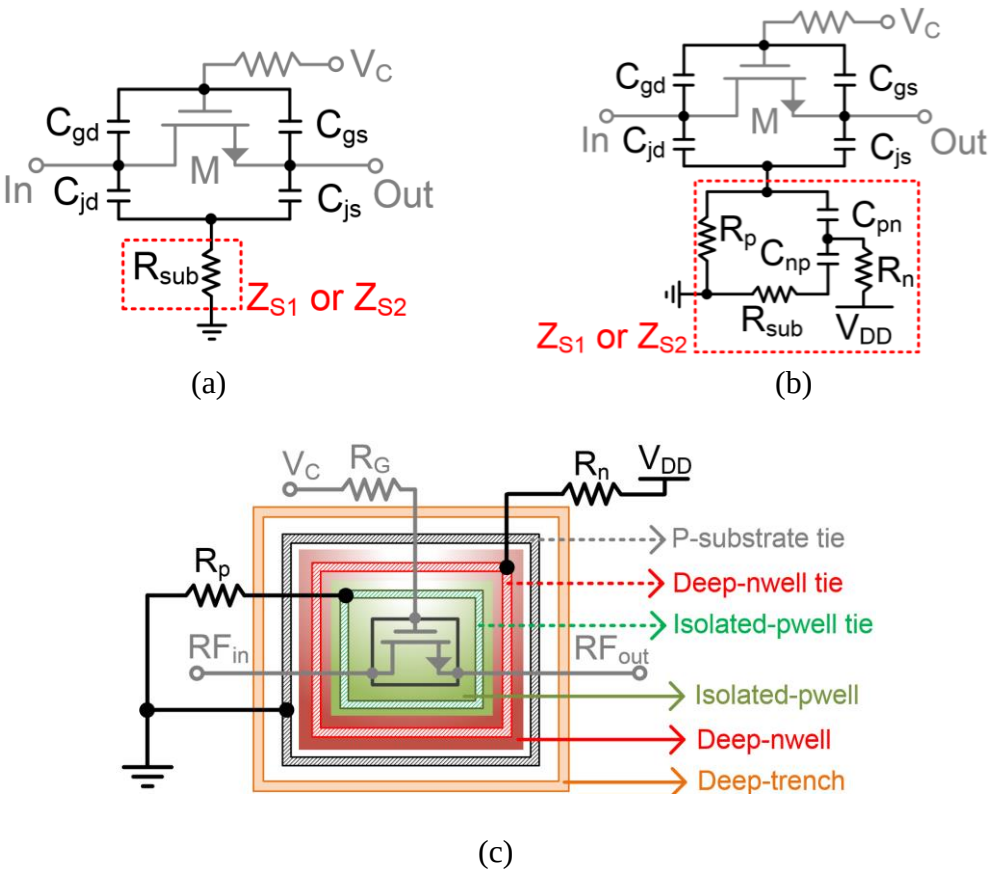


Fig. 6.4. Parasitic elements in an nMOS transistor (a) without floating body and (b) with floating body, and (c) a top view of the nMOS transistor with floating body. Z_{S1} and Z_{S2} are shown in Fig. 6.3.

The inductances (L_R) and the size of the transistors outside the phase delay cells can be determined based on a trade-off among insertion/return loss, bandwidth, etc. The low-pass Pi-type topology in Fig. 6.2(a) has a virtue of compact size with less number of inductors (than those of high-pass Pi- and low-pass T-type) and low insertion loss with fewer series inductors and the added transistor in parallel with L_S, M_S, (than those of high-pass Pi-, low-pass T- and high-pass T-type). These are particularly desirable for SiGe CMOS/BiCMOS RFICs whose real estate is expensive and insertion loss is relatively high

resulting from the low electron mobility transistors and the lossy silicon substrates.

Fig. 6.3 shows the low-pass Pi-type phase shifter and its equivalent models at bypass and phase delay states, where V_C is digitally controlled, that contain transistors' (M_S's and M_R's) significant parasitic elements affecting the performance of phase shifter, including junction capacitances at the drain (C_{jd1} and C_{jd2}) and the source (C_{js1} and C_{js2}), gate-drain capacitances (C_{gd1} and C_{gd2}), gate-source capacitances (C_{gs1} and C_{gs2}), and substrate impedances from source/drain junctions to a RF ground (Z_{S1} and Z_{S2}). A large resistance, R_G (=15 kΩ), is used at the gate of each transistor to prevent RF signal from leaking through the DC bias line and to decrease the fluctuations of the gate-drain and gate-source voltages in the phase shifters, which may cause breakdown [6-7]. In the bypass state shown in Fig. 6.3(b), M_S and M_R are turned on and off and the on- and off-state are represented by the on-resistance (R_S) and off-capacitance (C_{gd2}/2), respectively, assuming C_{gd2}=C_{gs2}. R_S forms a through-path along with the L_S and C_P, while the parallel resonator consisting of C_{gd2}/2 and L_R resonates at the operation frequency of the phase shifter. In the phase delay state shown in Fig. 6.3(c), M_s is turned off to create an approximate open, while M_R is turned on to make a connection to the ground through the on-resistance (R_R) and inductance (L_R).

6.1.1 Body-Floating Technique on Phase Shifter Design

A nMOS transistor and their parasitic elements without and with the body-floating technique are shown in Figs. 6.4(a) and (b), respectively. The body-floating technique changes the condition of the substrate impedance (Z_{S1} or Z_{S2}) in Fig. 6.3 from R_{sub} in Fig.

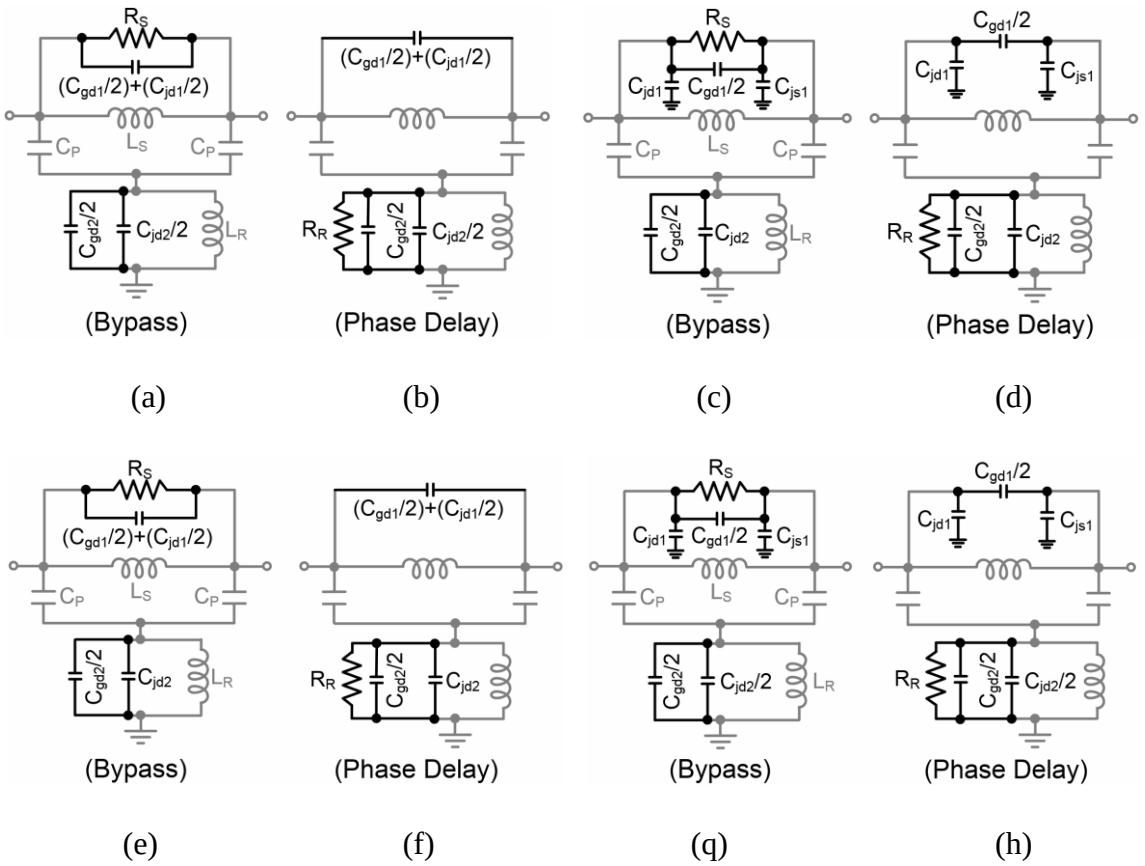


Fig. 6.5. Simplified equivalent circuits at bypass and phase delay states of the 1-bit low-pass Pi-type phase shifter in Fig. 2 consisting of: series and shunt transistors with floating body (a, b), series and shunt transistors without floating body (c, d), series transistor with floating body and shunt transistor without floating body (e, f), series transistor without floating body and shunt transistor with floating body (g, h).

3(a) to $\{1/(j\omega C_{pn}// j\omega C_{np})\}+R_{sub}$ in Fig. 5.4(b), where R_p (=15 kΩ) and R_n (=15 kΩ) are assumed to be infinite. A deep-nwell layer can be employed to implement the body-floating technique in a CMOS/BiCMOS process, whose simplified top view is shown in Fig. 5.4(c). In the deep-nwell body-floating transistor in Fig. 5.4(c), the connections for R_p and R_n, from the isolated-pwell tie and deep-nwell tie, respectively, should be short, and the ground plane connected to the p-substrate tie should be firm and well-defined in

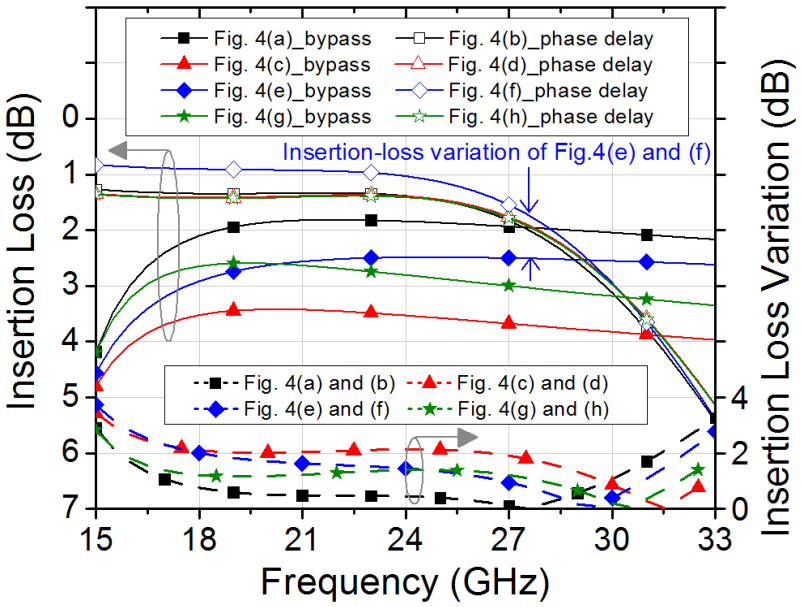


Fig. 6.6. Simulated insertion losses and insertion-loss variations of a 1-bit phase shifter based on the equivalent circuits in Fig. 4.

order to minimize any other parasitics, which are not depicted in Fig. 5.4(b). The junction capacitances (C_{pn} and C_{np}) can also be reduced, hence approaching closer to the ideal body-floating condition, by minimizing the size of isolated-pwell and deep-nwell within the limits of the required design rules/restrictions in a process. The deep-trench surrounding the transistor decreases the interference from other elements.

Fig. 6.5 shows the simplified equivalent circuits of the 1-bit phase shifter with or without the body-floating technique for bypass and phase delay states, where the body condition of the transistor without floating body is assumed to be short (with the small substrate impedance of R_{sub}) and the transistor with floating body is open (with the large substrate impedance of $\{1/(j\omega C_{pn}//j\omega C_{np})\}+R_{sub}$), and $C_{jd1}=C_{js1}$ and $C_{jd2}=C_{js2}$. The junction capacitances of the series transistor without floating body (C_{jd1} and C_{js1}) shown in Figs.

6.5(c) and (g) act as leakage paths causing more insertion loss in a bypass state, which does not happen with the body-floating series transistors in Figs. 6.5(a) and (e). On the other hand, in a phase delay state, the junction capacitance of the shunt transistor without floating body (C_{jd2}) shown in Figs. 6.5(d) and (f) is larger than the capacitance of the body-floating transistor ($C_{jd2}/2$) in Figs. 6.5(b) and (h), leading to better input/output matching condition. This is due to the fact that the on-state impedance of the transistor (M_R) without floating body, $2R_R/(2+j\omega C_{gd2}R_R +2j\omega C_{jd2}R_R)$, is lower than that with floating body, $2R_R/(2+j\omega C_{gd2}R_R+j\omega C_{jd2}R_R)$. So, it is intuitively expected that the equivalent circuits in Figs. 6.5(a) and (f) would have the lowest insertion loss performance in the bypass and phase delay states, respectively.

As an example to verify the body-floating technique in a phase shifter design, a 90° phase shifter centered at 24 GHz with transistor M_S having 8 fingers of 5 μm each, M_R having 12 fingers of 10 μm each, L_S=290 pH, L_R=477 pH, and C_P=130 fF is simulated as shown in Fig. 6.6 based on the equivalent circuits in Fig. 6.5. The lowest insertion-loss variation of 0.54±0.54 dB over 18 to 30 GHz is obtained with the phase shifter using the body-floating technique on both the series and shunt transistors in Fig. 6.5(a) and (b). The worst insertion-loss variation of 1.5±0.62 dB, however, is obtained by the phase shifter designed based on the equivalent circuits in Fig. 6.5(c) and (d), which uses the transistors without floating body.

Fig. 6.7 shows a cross-sectional view of the body-floating series and shunt transistors in a 1-bit low-pass Pi-type phase shifter. R_{SS} is substrate resistance between the series and shunt nMOS transistors, which also shows an isolation/interference between the

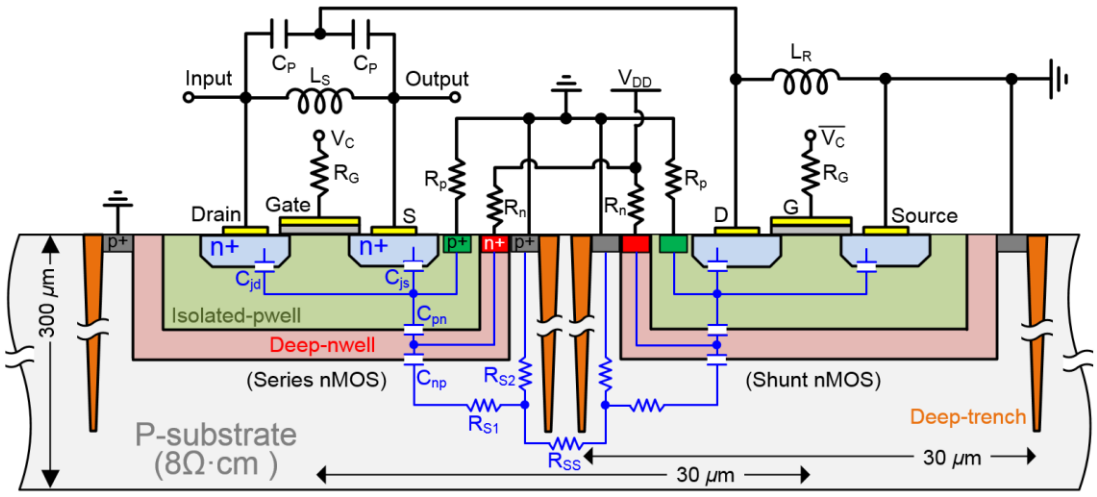


Fig. 6.7. A cross section of a low-pass Pi-type 1-bit phase shifter with a deep-nwell body-floating technique. The transistors are simplified with a single-finger gate.

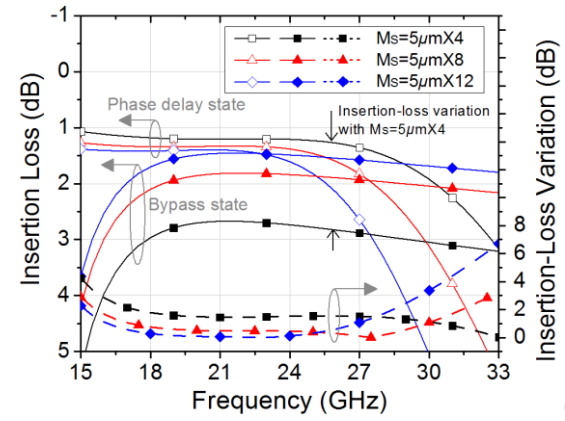
transistors, and the resistance (isolation) can be increased by placing deep-trenches around the transistors as shown, which help reduce the size of the circuit as well. It is noted that the isolation can also be improved by reducing the substrate resistance, R_{S2}, to the p-substrate tie.

6.1.2 Optimization of Transistor's Size

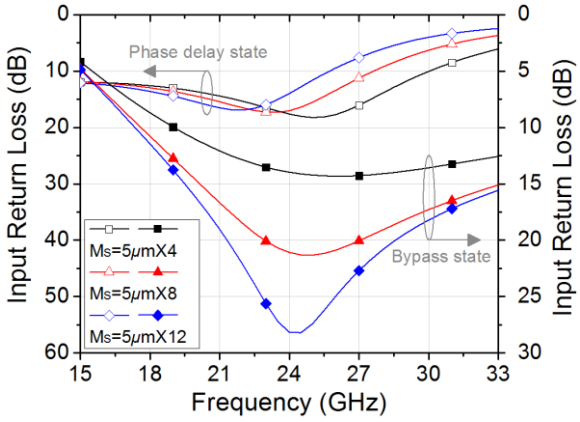
Optimizing the size of transistors is one of the effective ways to minimize the insertion-loss variation of phase shifters. For example, the insertion losses at the bypass and phase delay states are decreased and increased by increasing the size of the series transistor (M_S) in Fig. 6.3(a), respectively. These are due to the decreased on-resistance and increased off-capacitance at the bypass and phase delay states, respectively. Consequently, the insertion-loss variation in the phase shifters can be adjusted and optimized accordingly. Fig. 6.8 shows the simulated insertion loss, insertion-loss variation,

input return loss, and phase delay for the bypass and phase delay states for different gate fingers of M_S in the 90° phase shifter employed for the simulation in Fig. 6.6. The number of the transistor's fingers is changed from 4 to 12 in three steps with a constant 5-μm gate width. In Fig. 6.8(a), it is shown that the insertion-loss variation with 4, 8 and 12 fingers are 1.5±0.03 (worst), 0.3±0.19 and 0.56±0.5 dB over 21 to 27 GHz, respectively. The return losses in Fig. 6.8(b) vary in different states with varying M_S size, which should be considered during the optimization of the transistor size. Moreover, Fig. 6.8(c) shows that the phase delays are 84°, 94° and 103° at 24 GHz with the 4, 8 and 12 fingers, respectively, demonstrating that a larger size of M_S leads to more phase delay, which is due to larger off-capacitance.

The shunt nMOS transistor (M_R) in Fig. 6.3(a) also has an influence on the insertion-loss variation. For instance, a larger transistor M_R, corresponding to a smaller on-resistance, causes low return and insertion losses at a phase delay state with a well-defined RF ground; but its larger off-capacitance leads to narrow bandwidth with a smaller L_R at a bypass state, then leading to worse insertion-loss variation in a wide-band phase shifter design. So, the size of M_R is determined mainly considering the phase shifter's size (through the size of L_R), bandwidth, insertion loss, and insertion-loss variation. Fig. 6.9 shows the simulations of the insertion loss, insertion-loss variation, input return loss and phase delay for the bypass and phase delay states of the 90° phase shifter for different sizes of M_R (10μm×9, 10μm×12 and 10μm×18) and corresponding inductances of L_R (650, 477 and 340 pH). As seen in Figs. 6.9(a) and (b), the phase shifter has narrower bandwidth



(a)



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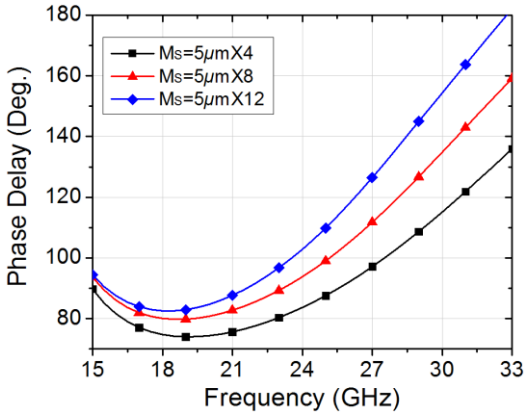
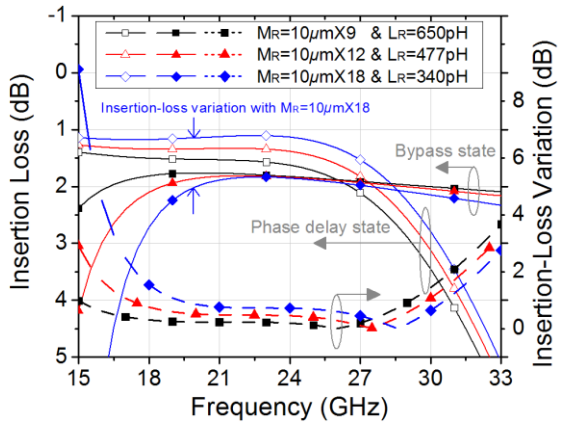
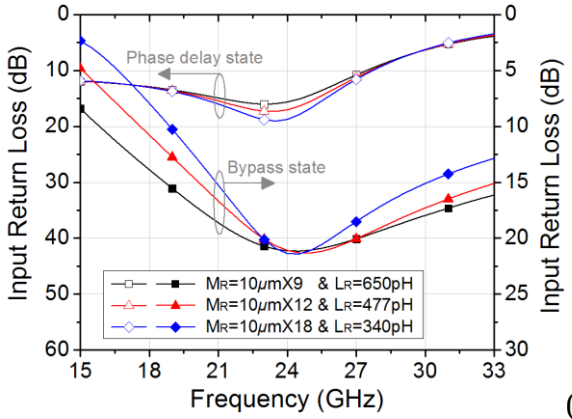


(c)

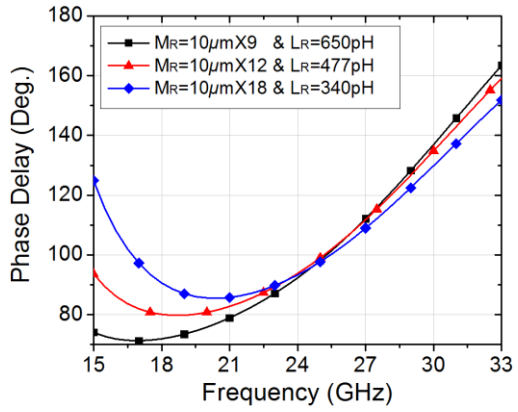
Fig. 6.8. Simulations of the 90° phase shifter with different M_S (5μm×4, 5μm×8 or 5μm×12) for bypass and phase delay states: (a) insertion loss and insertion-loss variation, (b) input return loss, and (c) phase delay representing the phase difference between the bypass and phase delay states.



(a)



(b)



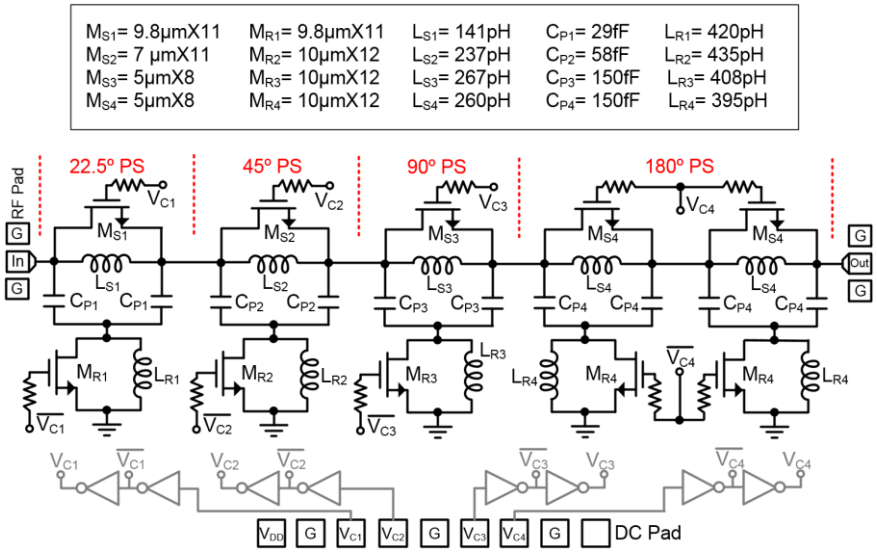
(c)

Fig. 6.9. Simulations of the 90° phase shifter with different M_R (10μm×9, 10μm×12 or 10μm×18) for bypass and phase delay states: (a) insertion loss and insertion-loss variation, (b) input return loss, and (c) phase delay representing the phase difference between the bypass and phase delay states.

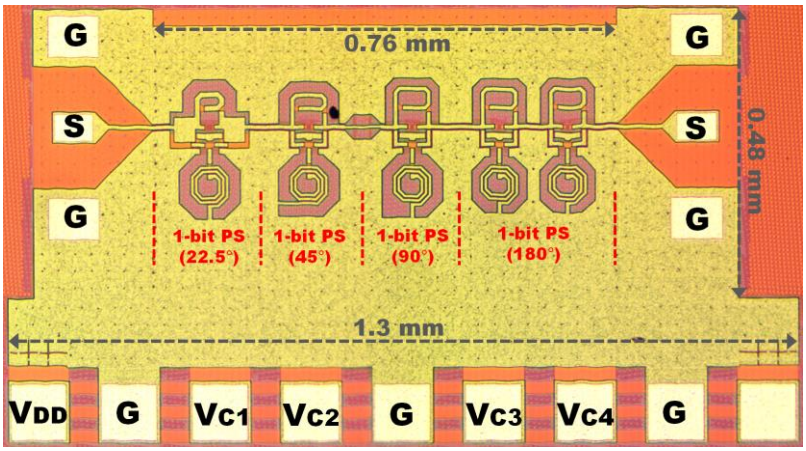
at the bypass state and lower insertion loss at the phase delay state with the larger M_R (10μm×18) and the corresponding L_R (340 pH) than with the smaller M_R and larger L_R. The insertion-loss variation with the 18-finger M_R and 340-pH L_R is 0.61±0.15 dB over 21 to 27 GHz, which is higher than the variation of 0.12±0.12 dB obtained with the 9-finger M_R and 650-pH L_R. Fig. 6.9(c) shows the varying slope of the phase delay by different sizes of the transistor and the corresponding inductors.

6.1.3 Design of a 4-Bit Phase Shifter with Body-Floating Technique

A 4-bit CMOS phase shifter is designed and fabricated with TowerJazz 0.18-μm BiCMOS technology [6-8] as shown in Fig. 6.10, which occupies 760 × 480 μm^2 excluding the on-wafer pads. The phase shifter consists of four individual 1-bit digital phase shifters (for 22.5°, 45°, 90° and 180° phase delays) designed based on the body-floating technique and transistor-size optimization to control the phase delay with 22.5° steps over 16 states. The phase shifter is generally laid out using coplanar waveguide (CPW) structure to confine the fields within the oxide layers, hence reducing their penetration into the silicon substrate, which effectively reduces not only the substrate loss and hence improving the Q-factor, but also the mutual coupling between adjacent components. Well-defined ground planes are also implemented in the layout to minimize the interference among adjacent elements, which facilitates designing the compact phase shifter circuit. All the inductors are designed with CPW considering their size and Q-factor, and metal-insulator-metal (MIM) capacitors are employed for compactness, reliability and high Q-factor in the design frequency range, except C_{P1} in the 22.5° section. C_{P1} is



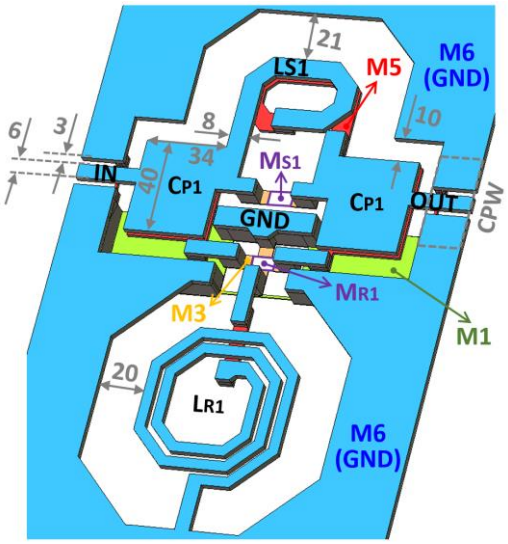
(a)



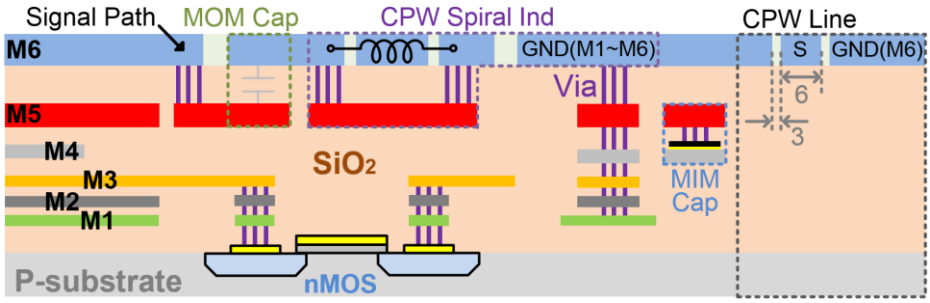
(b)

Fig. 6.10. A 4-bit CMOS digital phase shifter: (a) schematic and (b) microphotograph. Chip size (core part): 760 × 480 μm^2.

implemented with a metal-oxide (SiO_2)-metal (MOM) structure and EM-simulated with IE3D [6-9]. Figs. 6.11(a) and (b) respectively show the 3-dimensional (3-D) view of the 22.5° section and its simplified cross-section view of metal and substrate layers. The 22.5° section contains the MOM capacitors (C_{P1}s), CPW inductors (L_{S1} and L_{R1}), and CPW



(a)



(b)

Fig. 6.11. (a) 3-D view of the 22.5° section in the 4-bit phase shifter and (b) cross section view of metal and substrate layers. For the metal layers, the same colors are used in (a) and (b). Unit is μm.

interconnects. The capacitors are formed in the SiO_2 layer between the 5th (M5) and 6th (M6) metal layers as shown in Fig. 6.11(b). Since M5 and M6 are thicker than M1–M4, a high Q-factor MOM capacitor can be designed. Moreover, the metal layers (M5 and M6) and the p-substrate are placed sufficiently apart, which minimizes the shunt parasitic capacitances of the MOM capacitor. For the same reasons, the CPW inductors and interconnects are also designed with M5 and M6. The CPW interconnect in the M6 layer

has 3-μm gaps and 6-μm width as shown in Fig. 6.11, for the 50-Ω characteristic impedance at the desired band (21–27 GHz). Fig. 6.12 shows the simulated and measured results of the CMOS 4-bit digital phase shifter, in which the measured insertion-loss variations (RMS amplitude errors) are 11±1.2 dB (0.8 dB), 13±2.6 dB (1.7 dB) and 16±5.2 dB (3.2 dB) at 21, 24 and 27 GHz, respectively. The simulated and measured RMS phase errors are 0.5–18° and 2.4–26° over 21 to 27 GHz, respectively. For all 16 states, the measured input/output return losses are greater than 10 dB over 21 to 27 GHz and the measured input P1dB is greater than 12.5 dBm at 24 GHz.

6.2 Conclusion

A body-floating technique and transistor-size optimization have been investigated for low insertion-loss variation of the phase shifter. The simulations verify that the insertion-loss variation is reduced by using the body-floating technique accompanying the deep-nwell layer for the series and shunt transistors and optimizing the transistors' size. A 24-GHz CMOS 4-bit phase shifter is designed on a 0.18-μm BiCMOS process implementing transistors with the body-floating technique and transistor-size optimization. The measured results across 21 to 27 GHz show small insertion-loss variation and RMS amplitude error with good input/output return loss. The proposed design techniques especially do not cause any increase in size and cost, which is preferred for RFIC design. The developed phase shifter along with the body-floating technique and transistor's size optimization for low loss variation is attractive for microwave and millimeter-wave phased array design.

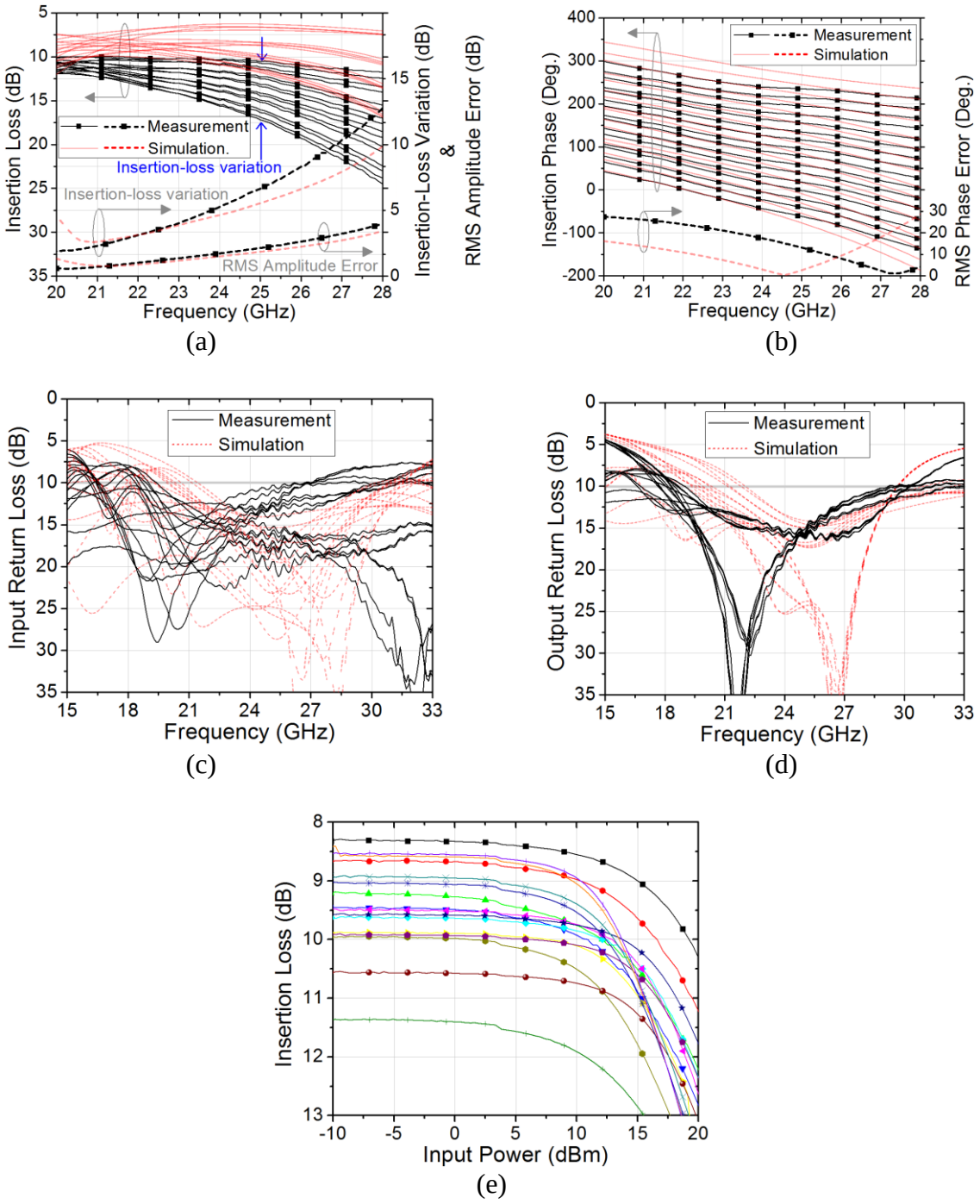


Fig. 6.12. Simulated and measured (a) insertion loss, insertion-loss variation and RMS amplitude error, (b) insertion phase and RMS phase error, (c) input return loss, (d) output return loss over 16 states of the 4-bit CMOS digital phase shifter. (e) Measured power handling of the phase shifter over 16 states at 24 GHz.

6.3 References

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CHAPTER VII

57–64 GHZ CMOS 4-BIT PHASE SHIFTER WITH SMALL INSERTION-LOSS VARIATION

As mentioned in Chapter VI, a small insertion-loss variation is required in a phase shifter design to minimize the damages to the operations of amplitude control circuits such as attenuators and variable gain amplifiers which are used for beam tailoring in the phased-array system. In this chapter, a phase shifter covering 57 to 64 GHz with small insertion-loss variation is designed for the phased-array transmitter as shown in Fig. 7.1. A novel phase shifter topology with an additional shunt inductor is proposed to reduce the insertion-loss variation. The validity of the proposed topology is confirmed through the performance of a CMOS 4-bit digital phase shifter designed and fabricated using a 0.18-μm BiCMOS technology over 57 to 64 GHz.

7.1 Design, Simulation, and Measurement

A new 4-bit phase shifter with small insertion-loss variation is shown in Fig. 7.2. It is designed based on the conventional high-pass Pi- and T-topologies in Figs. 6.2(b) and (d). In Fig. 7.2, the shunt inductors (L_{A1}, L_{A3}, and L_{A4}) are added to the conventional topologies to reduce the resonance inductors (L_{R1}, L_{R3}, and L_{R4}), which lead to low insertion loss at the phase delay state of the phase shifters. On the other hand, the added inductors hardly affect the insertion loss at the reference state because the defined resonance frequency by the resonance inductor (L_{R1}, L_{R3}, or L_{R4}) and off-capacitance (by

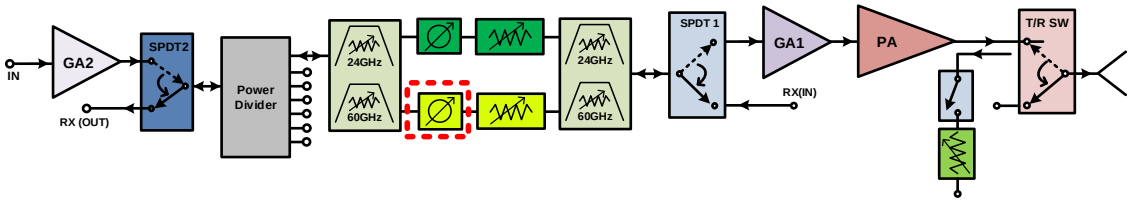


Fig. 7.1. A 57–64 GHz phase shifter in the phased-array transmitter (in the dotted box).

M_{R1}, M_{R3}, or M_{R4}) is the same as that of the conventional phase shifter's counterparts. So, the difference between the insertion losses at reference and phase delay states is significantly reduced. The phase shifter is fabricated with TowerJazz 0.18-μm BiCMOS technology as shown in Fig. 7.3, which occupies 960 × 480 μm^2 excluding the on-wafer pads. The phase shifter consists of four individual 1-bit digital phase shifters (for 22.5°, 45°, 90° and 180° phase delays) to control the phase delay with 22.5° steps over 16 states. The phase shifter is generally laid out using coplanar waveguide (CPW) structure to confine the fields within the oxide layers, hence reducing their penetration into the silicon substrate, which effectively reduces not only the substrate loss and hence improving the Q-factor, but also the mutual coupling between adjacent components. Well-defined ground planes are also implemented in the layout to minimize the interference among adjacent elements, which facilitates designing the compact phase shifter circuit. All the inductors are designed with CPW considering their size and Q-factor and EM-simulated.

Fig. 7.4 shows the simulated and measured results of the CMOS 4-bit digital phase shifter, in which the measured insertion-loss variations are 13±3 dB, 12±3 dB, and 11.3±1.3 dB at 57, 60 and 64 GHz, respectively. The simulated and measured RMS phase errors are 2.7–3.9° and 4.3–10.8° over 57 to 64 GHz, respectively. For all 16 states, the measured input/output return losses are greater than 10 dB over 57 to 64 GHz.

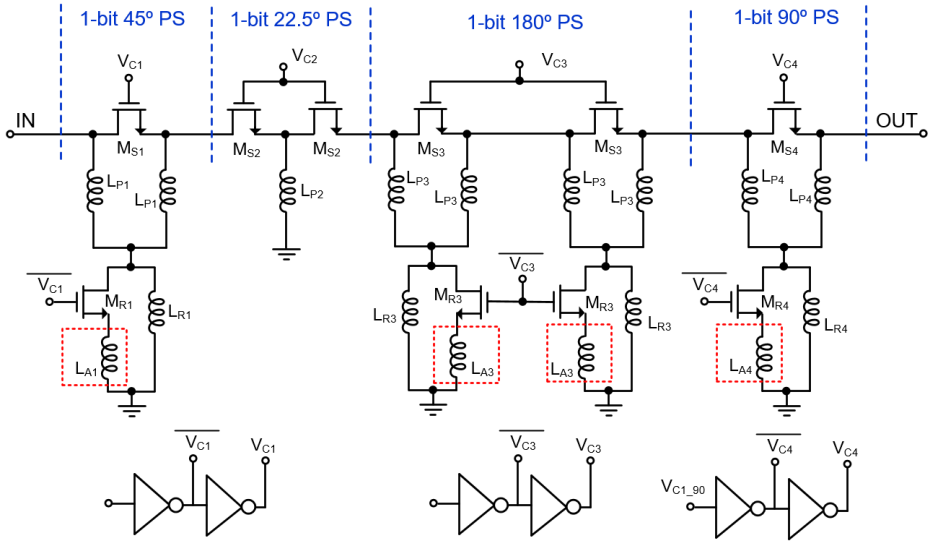


Fig. 7.2. A proposed 57–64 GHz 4-bit phase shifter topology with additional shunt inductors (L_{A1}, L_{A3}, and L_{A4}) designed based on conventional high-pass Pi- and high-pass T-type phase delay networks.

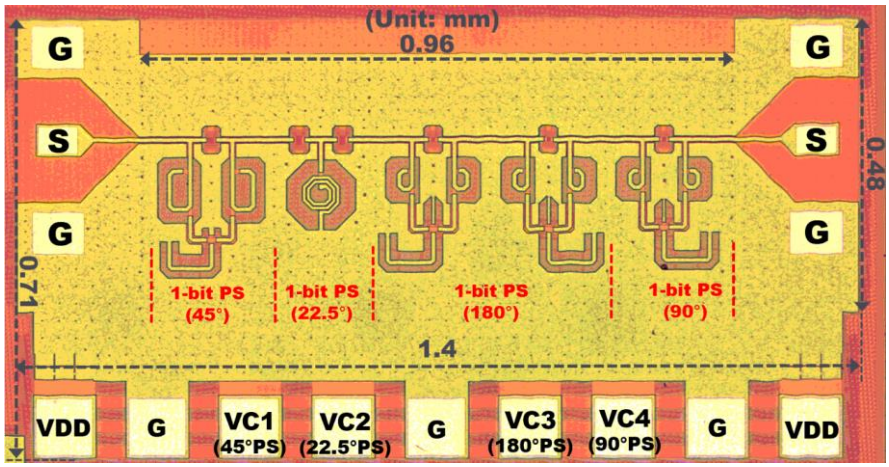


Fig. 7.3. A microphotograph of the 57–64 GHz 4-bit CMOS digital phase shifter.

7.2 Conclusion

A 57–64 GHz CMOS 4-bit phase shifter is designed using a 0.18-μm BiCMOS process based on the proposed topology with the added shunt inductors. The measured results across 57 to 64 GHz show small insertion-loss variation and low RMS phase error with good input/output return loss. The developed phase shifter for low loss variation is attractive for microwave and millimeter-wave phased array design.

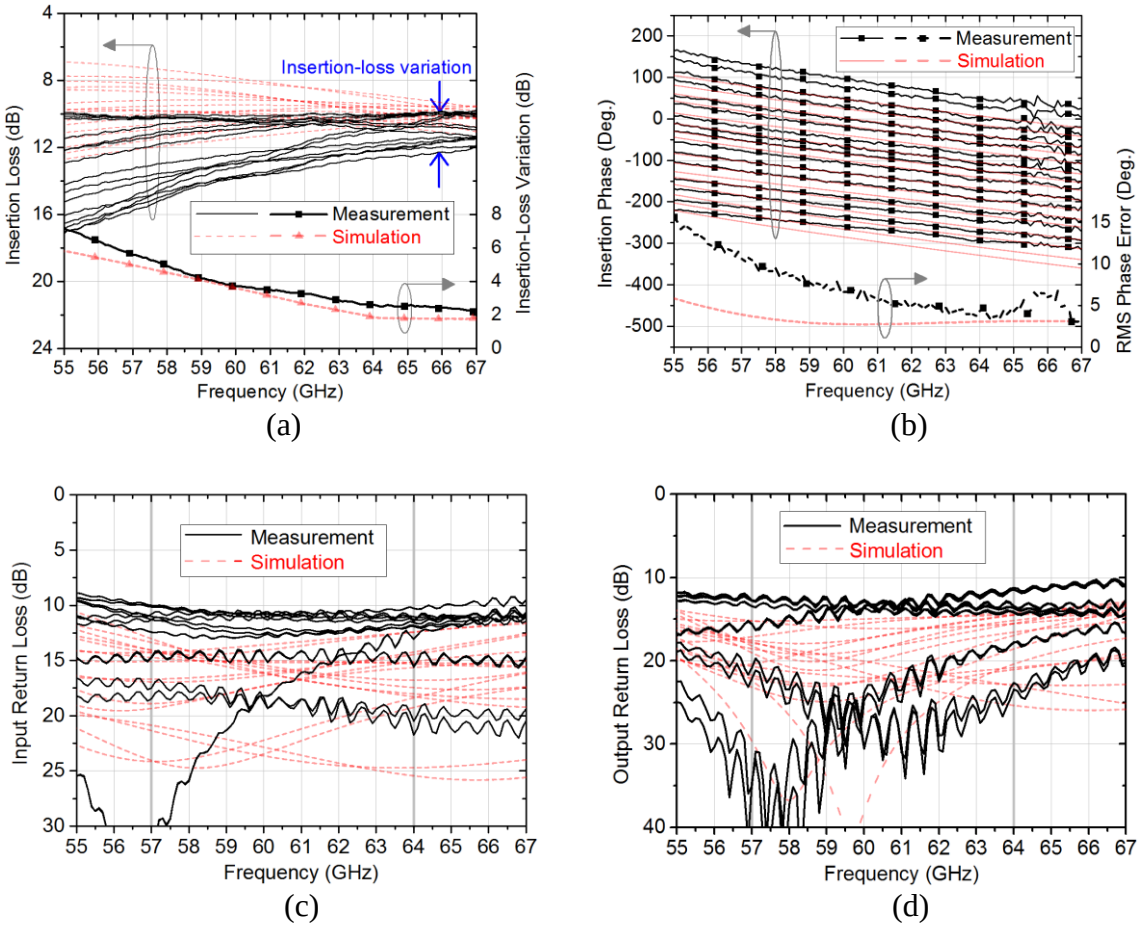


Fig. 7.4. Simulated and measured (a) insertion loss and insertion-loss variation, (b) insertion phase and RMS phase error, (c) input return loss, (d) output return loss over 16 states of the 4-bit CMOS digital phase shifter.

CHAPTER VIII

DC-TO-67 GHZ HIGH-SPEED BICMOS BJT CHARACTERIZATION WITH ON-WAFER CALIBRATION AND EM-BASED DE-EMBEDDING*

In the BiCMOS process, bipolar junction transistors (BJTs), npn and pnp, and metal-oxide-semiconductor field-effect transistors (MOSFET), nmos and pmos, are available on the same silicon-based substrate. BJT has higher gain and lower RF noise at high frequencies. Also, it is capable of generating more power with the large current density capability. The strengths of BJTs show that the transistor is better for the active circuit design in the phased-array transmitter in comparison with the CMOS transistors. Fig. 8.1 shows the amplifiers which are designed with BJTs in the dotted boxes. Other than that, the passive circuits are designed with CMOS transistors. Before using the BJTs in the amplifier design, we have characterized the transistors from DC to 67 GHz. Since 67 GHz is too high to use conventional de-embedding or on-wafer calibration techniques, we in this chapter propose a novel technique for characterizing BJTs up to the high frequencies.

Small- and large-signal models of active devices are needed for the design of radio-frequency integrated circuits (RFICs). These models can be classified into "physics-based" models and "measurement-based" (or "empirical") models. A physics-based

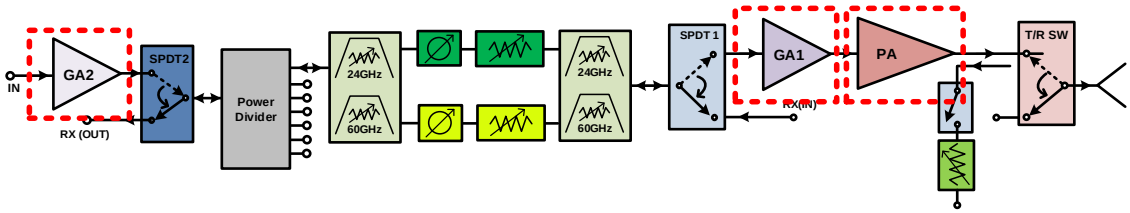


Fig. 8.1. Amplifiers designed with bipolar junction transistors (BJTs) in the phased-array transmitter.

model provides a direct relationship between the electrical performance and the geometry and physical parameters of devices and is, thus, very useful for device design and understanding of device operation. These models are, however, extremely difficult to be derived accurately at millimeter-wave (mm-wave) frequencies, mainly due to the lack of accurate analysis methods and difficulty in the formulation process. Moreover, the computation time in using these models for circuit design, especially complex RFICs containing many active devices operating over a wide frequency range, is prohibitively extensive. These models have limited use in CAD programs for mm-wave RFIC design. Empirical models can be derived using numerical results obtained from physics-based models and/or measurements of devices under dc and RF operations at different bias voltages and across interested frequencies. Practical empirical models, however, are typically measurement-based, in which measured data and simple closed-form equations are used together to develop the models. The empirical models do not need the physics and geometries of devices, yet, if properly obtained, can describe accurately the actual device electrical performance due to a direct relation between the models and measured performance of the devices. Measured scattering (S) parameters over interested frequencies are the most important part in the development of these models.

As the complementary metal oxide semiconductor (CMOS) and bipolar-complementary metal oxide semiconductor (BiCMOS) technologies and device performance have advanced into the mm-wave regime, accurate S-parameters of CMOS and BiCMOS devices at mm-wave frequencies are needed for the mm-wave RFIC design. The accuracy of these S-parameters is absolutely essential for extracting accurately the device parameters and small- and large-signal models.

A quick and convenient way (and hence becoming increasingly typical) for extracting the device S-parameters from an on-wafer measurement is using the calibration kit on an impedance standard substrate (ISS) as described in [8-1]. With the ISS-calibration, the effects of the cables between the vector network analyzer (VNA) and the on-wafer probes, and the probes are calibrated out up to the ends of the probe tips. To remove the effects of the on-wafer RF pads and interconnects associated with the device, a de-embedding procedure is utilized afterward. ISS-based calibrations were implemented along with de-embedding methods for transistor characterization [8-2], [8-3]. These de-embedding methods involve many calculations and multiple fabricated dummy test structures. The use of multiple dummies likely causes more measurement errors, especially at mm-wave frequencies and across wide frequency ranges.

While using the ISS for on-wafer calibration is sufficient for circuit measurements, especially for amplitudes such as insertion loss and return loss, it is not very accurate for measurements involving phase, such as S-parameters, due to the simple fact that the ISS does not provide the same environment in which an on-wafer device is embedded. On-wafer calibration techniques implementing calibration standards fabricated on the same

wafer together with the device under test (DUT) are more accurate in characterizing the device's S-parameters. These on-wafer calibration standards use the same RF pads and interconnects for the DUT, and hence can accurately mimic the responses of the RF pads and interconnects in the DUT's test structure, thus leading to more accurate calibration results and DUT's S-parameters, especially over wide frequency ranges and at high frequencies such as those in the mm-wave regime. However, as compared to the ISS-calibration technique, implementing an on-wafer calibration over a wide frequency range covering mm-wave frequencies poses challenges. In on-wafer calibrations, the ends of the interconnects for the open and load standards are typically very close to each other, hence causing a significant gap and open-end fringing capacitances, which could lead to substantial undesired effects for device characterization at mm-wave frequencies if not properly taken into account. These capacitances need to be determined accurately and input to a VNA for accurate calibration. Moreover, in the bipolar junction transistor (BJT) characterization as reported here, the gaps between the closely spaced interconnects needed to provide connections to the BJT's terminals, that define the reference planes, are about the same as the spacing between the base (or collector) and emitter (about 0.25 μm), making it impossible to place resistors at the reference planes within such narrow gaps for the load-standard design. In a previous work on on-wafer calibration [8-4], some interconnects including vias, used for interfacing with a transistor were excluded, hence inadvertently ignoring the parameters of these interconnects. Even if the excluded interconnects in the calibration structures were very small compared to other parts of the calibration structures, it is still not a preferable approach for device characterization at

Table 8.1 Size and configuration of BJTs

	Emitter's size and finger (width [μm]× length [μm]× no. of finger)	Configuration (no. of emitter, base and collector)
BJT1	0.15×10.16×1	1, 2, 2
BJT2	0.15×4.52×1	1, 2, 2
BJT3	0.15×10.16×1	2, 3, 2

mm-wave frequencies and over wide bands due to possibly significant effects otherwise occur at these frequencies.

In this chapter, on-wafer calibration and electromagnetic (EM) based de-embedding procedures are implemented to accurately characterize the S-parameters of BJTs in 0.18-μm SiGe BiCMOS technology across an extremely wide frequency range up to 67 GHz. The EM-based de-embedding specifically resolves the problem of non-calibrated parts, consisting of a part of the interconnects including the vias and the spacing between the closely spaced interconnects, encountered in typical on-wafer calibrations, hence leading to accurate device characterization at mm-wave frequencies.

8.1 On-Wafer Calibration and EM-based De-embedding

8.1.1 On-wafer Calibration Structures and Issues

Table 8.1 summarizes the size and configuration of three BJTs that are characterized on-wafer. Figs. 8.2 and 8.3 show photographs of the on-wafer calibration standards used in the short-open-load-thru (SOLT) calibration method [8-1] and test structure for BJT1, configured as a common-emitter amplifier, fabricated with TowerJazz

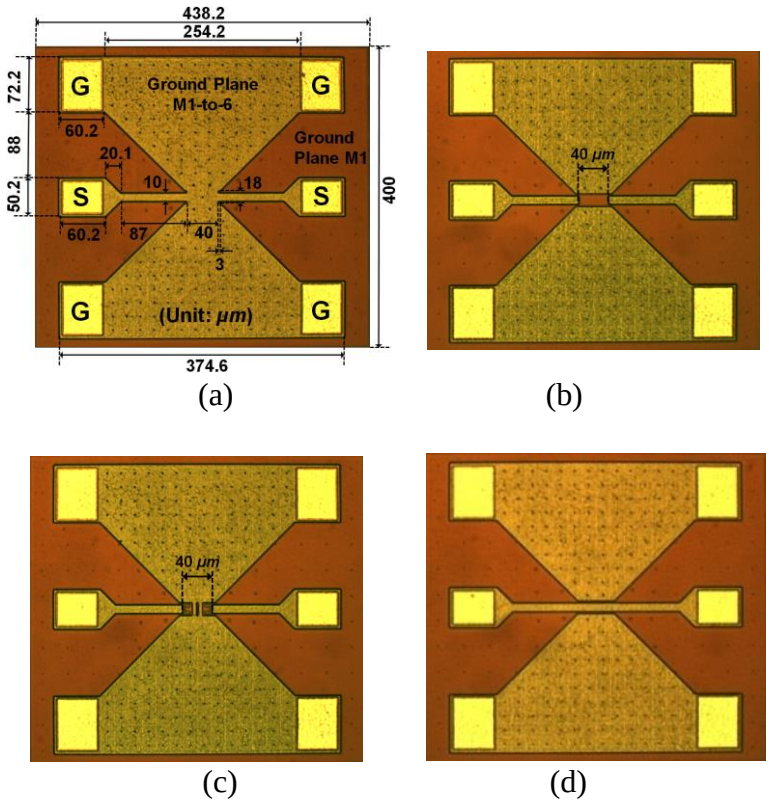
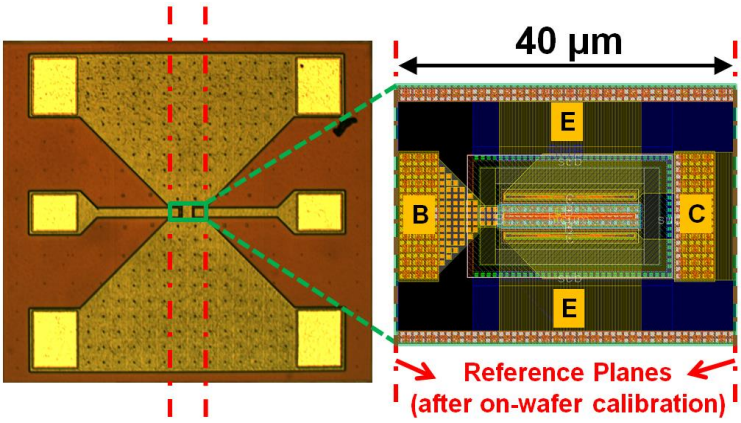


Fig. 8.2. Photographs of fabricated on-wafer calibration standards: (a) short, (b) open, (c) load, and (d) thru.

0.18-μm SiGe BiCMOS technology [8-5]. They are designed based on a coplanar waveguide with grounded back conductor (CPWG), which not only minimizes the length of the interconnect from the BJT to the ground plane, but also minimizes the influence of the low-resistive silicon substrate to the BJT. The structures in Figs. 8.2 and 8.3 have the same size of 438.2×400 μm^2 and contain identical RF pads and interconnects, enabling the same environment and hence accurate calibration results. The top metal (M6) with the thickest thickness, and hence lowest loss, is used for the RF pads and interconnects, while the lower metal (M1 or M2) is utilized for the interconnects around BJTs for ease of

connection. 50-Ω titanium nitride (TiN) metal resistors are used for the loads in Fig. 8.2(c). In Fig. 8.3, the vertical dotted lines represent the reference planes after the on-wafer calibration, and the zoomed view shows the interconnects for the BJT, beyond the reference planes, that connect the base (B), collector (C), and emitter (E) to the input, output, and (coplanar) ground planes, respectively. It is noted that the test structures for BJT2 and BJT3 are essentially the same as that for BJT1 in Fig. 8.3, with some minor differences depending on the BJT's size and configuration as indicated in Table 8.1.

The design of reliable calibration standards for on-wafer calibration is challenging, requiring careful layout and analysis. As shown in Fig. 8.2, the standards contain not only RF pads, but also interconnects, unlike typical ISS calibration standards in [8-1] which contain no interconnects. The closely spaced open ends of the interconnects in the open and load standards, seen in Figs. 8.2(b) and (c), cause a significant gap and open-end fringing capacitances, which could obstruct the design of reliable standards if not properly accounted for. However, there is no analytical equation that can calculate these parasitic capacitances accurately for use in on-wafer calibrations, especially at mm-wave frequencies. To obtain accurate results for these parasitics, an extra complex extraction procedure is required before the on-wafer calibration is conducted, and this should be done for every fabrication due to possible variations of the fabrication processes. Moreover, sufficient gap needs to be used to enable placement of two 50-Ω resistors, each constituting the load standard. To provide a small gap that is sufficiently large to accommodate two 50-Ω resistors and has a minimum gap and fringing capacitances, the EM simulator IE3D [8-6] was used for simulating the effects of different gaps, and a gap



(a) (b)

Fig. 8.3. (a) Photograph of fabricated test structure for BJT1 configured as a common-emitter amplifier and (b) zoomed view showing the layout of the extra interconnects for the base (B), collector (C) and emitter (E) within the 40-µm gap.

of 40 μm was selected for all the structures in Figs. 8.2 and 8.3.

As seen in Fig. 8.3(b) and elaborated in Fig. 8.4, there are extra interconnects, which include vias, beyond the reference planes established by the on-wafer calibration. These interconnects are needed to facilitate connections to the transistor's terminals. As will be further elaborated in the following Figs. 8.5 and 8.6, these interconnects to the base, collector and emitter are too close to each other (around 0.25 μm) to enable placement of a 50-Ω resistor needed for the load-standard design, hence further complicating the characterization process. The effects of these interconnects need to be removed for accurate device characterization. However, they cannot be calibrated out through typical on-wafer calibrations. To alleviate this issue, these non-calibrated parts are extracted through an EM-based de-embedding procedure to be described in the following section.

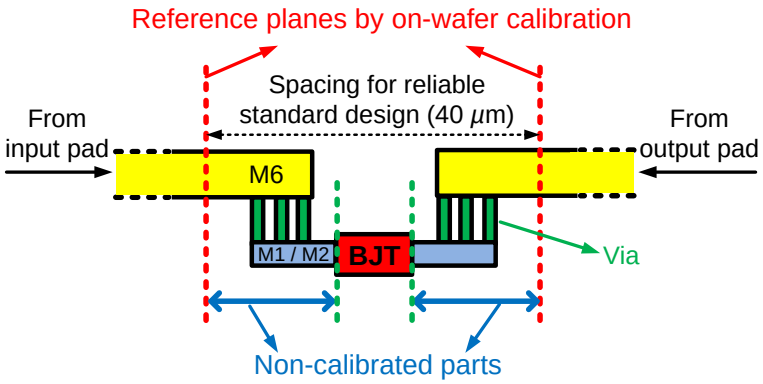


Fig. 8.4. A simplified cross-sectional view of the BJT-test structure showing the reference planes by the on-wafer calibration and the non-calibrated parts.

8.1.2 EM-based De-Embedding Procedure

The foregoing analysis reveals that there are still parts of the interconnects, as shown in Fig. 8.4, that cannot be calibrated through measurement even after the on-wafer calibration is executed. In order to extract these remaining non-calibrated elements, a two-step de-embedding procedure in [8-7] is conducted with EM simulations, which is fast and convenient, yet giving accurate results as will be seen later. The EM-based two-step de-embedding technique, which is based only on two dummies (open and short), is relatively simple and accurate at high frequencies. To perform the EM-based de-embedding, the layouts of the open and short dummies are created in IE3D as shown in Fig. 8.5. Since these dummies are only used for calculating the parameters of the non-calibrated part in Fig. 8.4, the RF pads and interconnects, which are already calibrated out in the on-wafer calibration, are excluded in these layouts. Consequently, the reference planes in Fig. 8.5 after the on-wafer calibration are the same as the beginning and end of the dummies. There are three separate interconnects for B, C, and E on the open dummy in Fig. 8.5(a), while

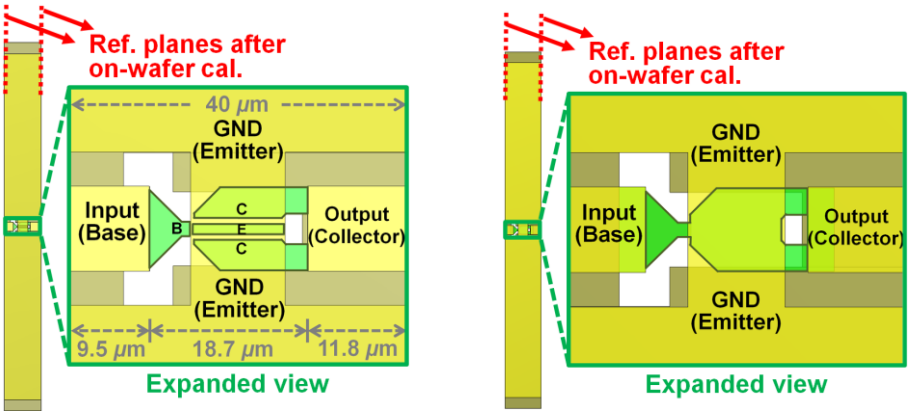


Fig. 8.5. Layouts of open (a) and short (b) dummies used in EM-simulations for BJT1 de-embedding and their expanded views. The dimensions for the short dummy are the same as those for the open dummy.

on the short dummy in Fig. 8.5(b), these interconnects are combined together and connected to the emitter ground (GND). Fig. 8.6 shows the 3-dimensional (D) view of the open-dummy pattern shown in Fig. 8.5(a). The metals from M1 to M6 are stacked together to form the ground plane (GND). The base and collector are at M6 and connected to M1 and M2 separately through vias, which define the corresponding references planes for the base and collector. The emitter at M6 is connected to GND and then to M2 through vias which define the reference plane for the emitter. This reference, although grounded, behaves as a distributed ground, not an ideal ground, and hence causing effects at high frequencies that need to be taken into account properly. It is recalled that the BJT is connected as a common-emitter amplifier. It is particularly noted that, in Figs. 8.5 and 8.6, the BJT is not part of these layouts, and the entire structures, which consist of all the metals including vias, are external to the BJT. The vacant part on M1 (denoted as M1 GND in

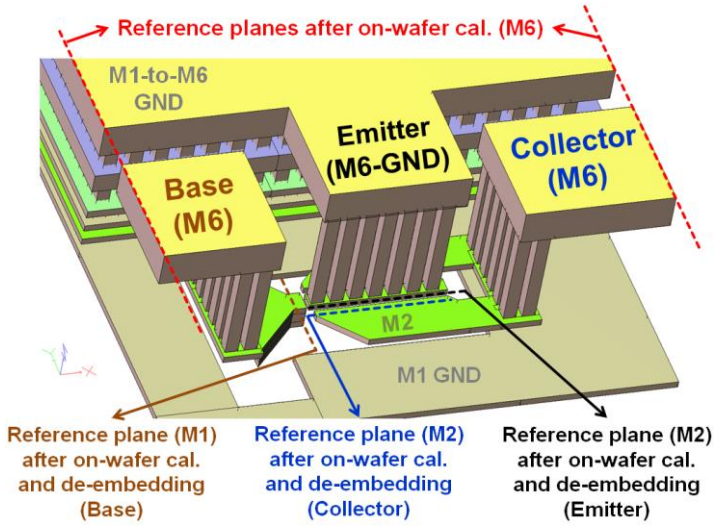


Fig. 8.6. 3-D view of the open dummy for BJT1 characterization. For better visibility, only one emitter connection and ground plane are shown.

Fig. 8.6) is used for the BJT. The reference planes on M6 are obtained after the on-wafer calibration, while the three reference planes on M1 or M2 are obtained after the following three steps are performed: SOLT on-wafer calibration, BJT-test structure measurement, and EM-based two-step de-embedding. The dummies for the other two transistors BJT2 and BJT3 are basically the same as those for BJT1 shown in Figs. 8.5 and 8.6. In order to properly perform the SOLT calibration, (load) resistors need to be placed at the reference planes on M1 for the base and M2 for the collector terminals seen in Fig. 8.6. The distance from the collector and base references to the emitter (GND) is around 0.25 μm, making it impossible to place a resistor. Furthermore, the resistor at the collector reference would need to be connected vertically from M2 to M6, which is impossible to do with the current technology. While the resistor at the base can be connected to the ground from the side of the base through a larger available space on M1, it is not desired to do so since this will

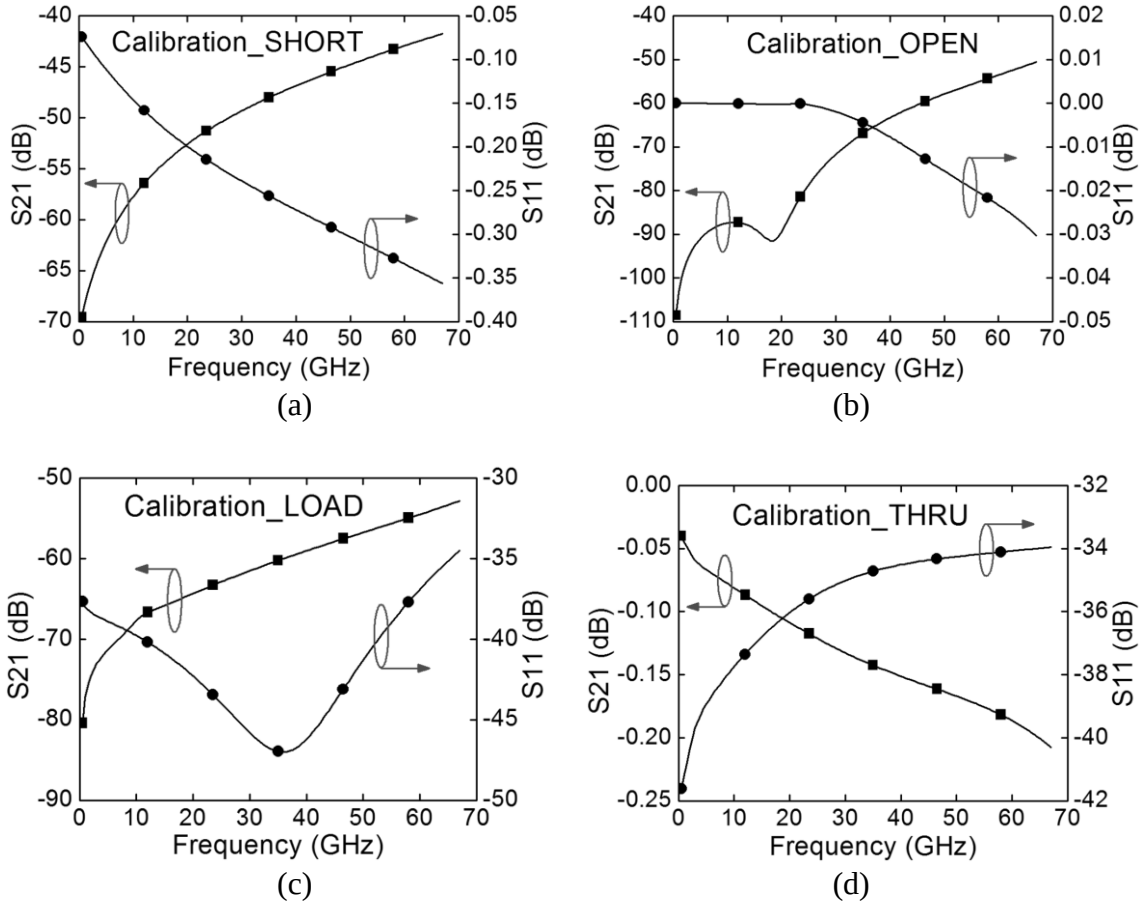


Fig. 8.7. EM-simulated results of the on-wafer calibration standards: short (a), open (b), load (c), and thru (d).

alter the reference plane. Consequently, it is virtually impossible to fabricate these structures with (load) resistors needed for performing the SOLT calibration. The proposed EM-based de-embedding avoids actual fabrication of these structures, hence overcoming the problem and simplifying the process, while making possible accurate device characterization.

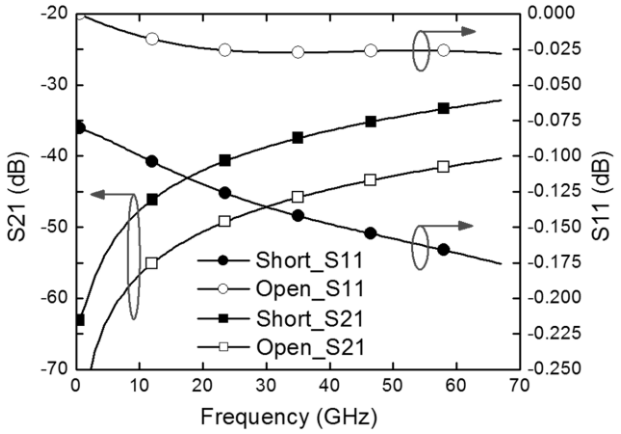


Fig. 8.8. EM-simulated results of the de-embedding dummies for BJT1: open (a) and short (b).

8.2 Simulated and Measured Results

Fig. 8.7 shows the EM-simulated results of the on-wafer calibration standards shown in Fig. 8.2. The insertion losses of the open and load standards in Figs. 8.7(b) and (c) are very high (> 50 dB) over a wide frequency range from DC to 67 GHz. These insertion losses are achieved with a 40-μm gap between the ends of the interconnects and are sufficient for the open and load standards. Although higher insertion losses can be achieved by increasing the gap, it is not necessary, and a larger gap would result in a larger part of the interconnects not taken into account during the on-wafer calibration which is undesirable. The open and short dummies for BJT1 in Fig. 8.5 are also EM-simulated, and the results are shown in Fig. 8.8. The EM-simulated results for the dummies of BJT2 and BJT3 are similar to those for BJT1 shown in Fig. 8.8.

As mentioned earlier, the BJT-test structures such as that in Fig. 8.3 are designed as common-emitter amplifiers. The simulations show that these structures can generate

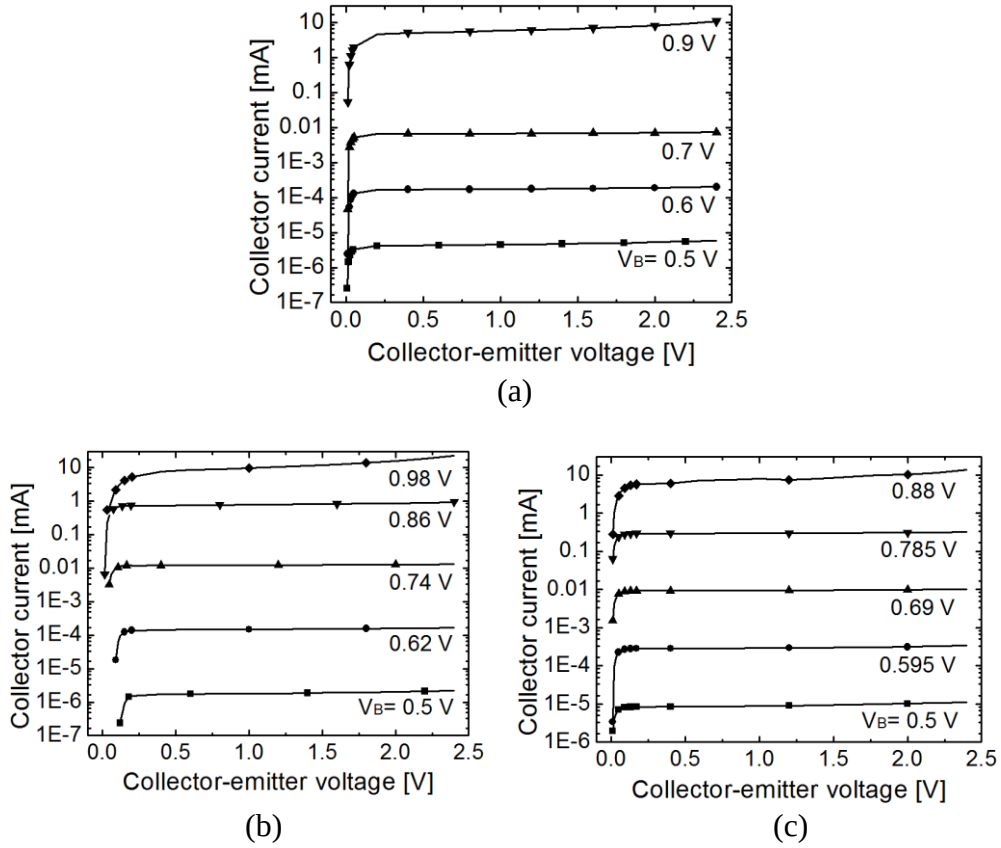
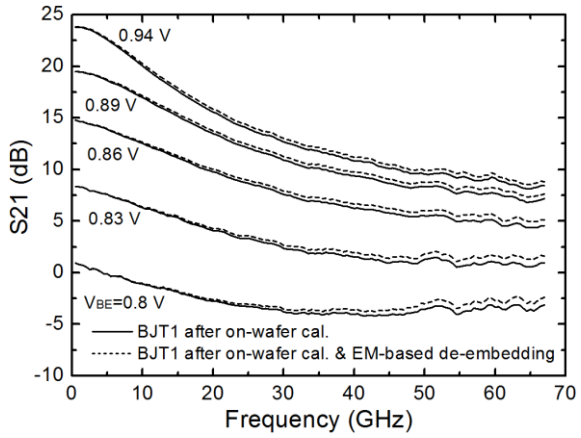
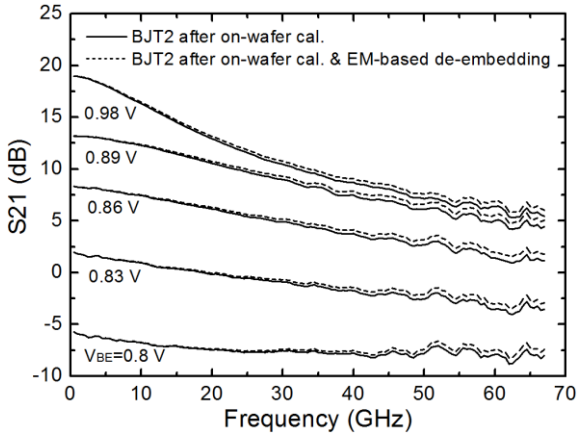


Fig. 8.9. Measured I-V curves of (a) BJT1, (b) BJT2 and (c) BJT3.

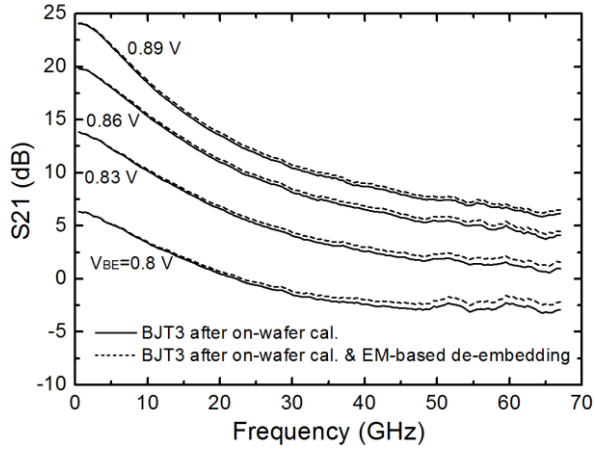
decent gains when the collector current (I_C) is about 10 mA. In order to estimate the bias voltages for the BJTs in the BJT-test structures, the collector currents versus collector-emitter voltage (V_{CE}) of the three BJTs for different base-emitter voltages (V_{BE}) were measured using an HP4145 semiconductor parameter analyzer as shown in Fig. 8.9. All the S-parameter measurements up to 67 GHz were then done with V_{CE} fixed at 1.5 V as V_{BE} was varied based on the DC test results in Fig. 8.9. Figs. 8.10 and 8.11 show the measured magnitudes and phases of S21 for the BJTs, respectively. The results corresponding to the solid lines were obtained after the SOLT on-wafer calibration, while



(a)

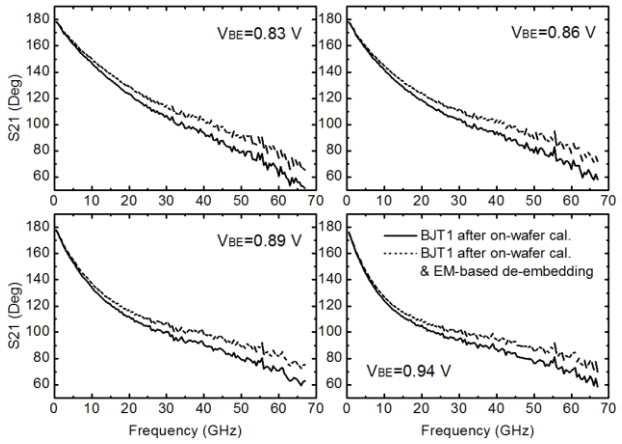


(b)

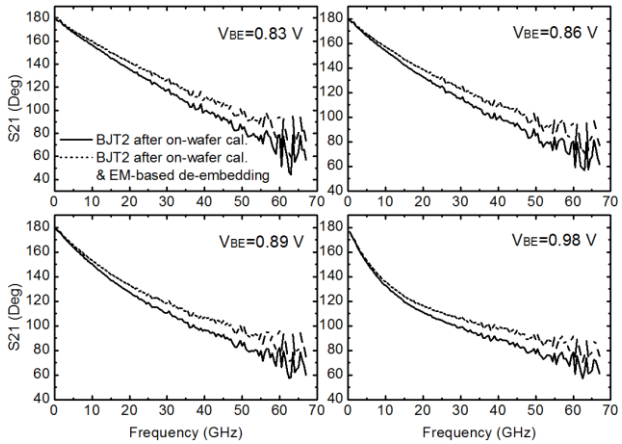


(c)

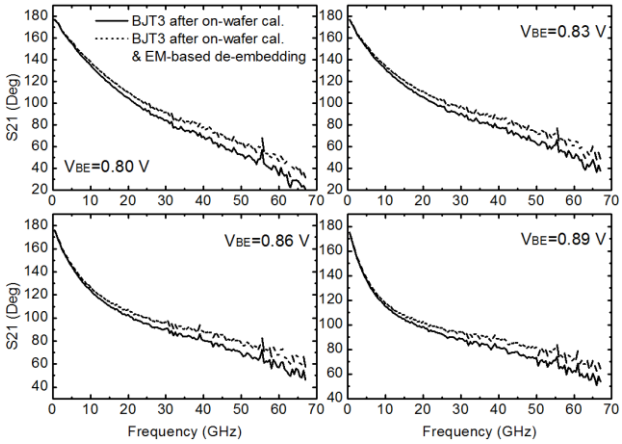
Fig. 8.10. Measured S21 magnitude versus frequency of (a) BJT1, (b) BJT2 and (c) BJT3 for different V_{BE}.



(a)



(b)



(c)

Fig. 8.11. Measured S21 phase versus frequency of (a) BJT1, (b) BJT2 and (c) BJT3 for different V_{BE}.

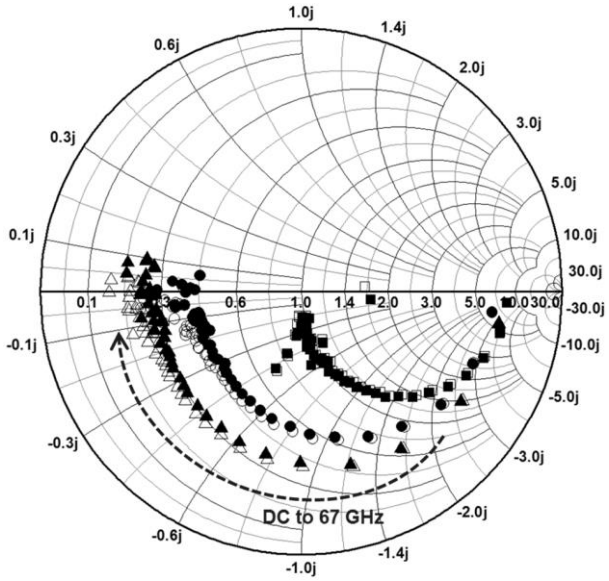


Fig. 8.12. Measured input reflection coefficients for BJT1, BJT2 and BJT3. Filled and non-filled symbols show results after on-wafer cal. and after on-wafer cal. and EM-based de-embedding, respectively. ●○ BJT1 at V_{BE}=0.94 V; ■□ BJT2 at V_{BE}=0.98 V; ▲△ BJT3 at V_{BE}=0.89 V.

those on the dotted lines were obtained after further performing the EM-based de-embedding on the results on the solid lines. The de-embedding was done by extracting the non-calibrated part calculated using the EM-simulations of the open and short dummies. Fig. 8.12 shows the measured input reflection coefficients of the BJTs after the on-wafer calibration only, and after both on-wafer calibration and EM-based de-embedding. The reduction in the insertion loss and phase in S21 up to 67 GHz, obtained by removing the non-calibrated parts through the de-embedding process, are clearly seen from the solid and dotted lines in Figs. 8.10 and 8.11 as expected. The insertion-loss and phase differences between the removal and non-removal of the non-calibrated parts are approximately less

than 2 dB and 15 deg. to 67 GHz, respectively, showing substantial differences (with respect to device characterization and modeling) at mm-wave frequencies. The results in Fig. 8.12 for BJT1, BJT2 and BJT3 were measured at V_{BE}= 0.94, 0.98 and 0.89 V, respectively, with V_{CE}=1.5 V. The results in Figs. 8.10–12 demonstrate that, while the BJTs could be characterized and modeled without the EM-based de-embedding at low frequencies, they should be characterized and modeled with the EM-based de-embedding at mm-wave frequencies, even over a narrow frequency range

8.3 Conclusion

An EM-based de-embedding method used along with the on-wafer calibration can resolve the issue of non-calibrated parts consisting of interconnects including vias within the spacing between the two ends of closely spaced interconnects typically encountered in on-wafer calibration standards. Specifically, the EM de-embedding enables the removal of the non-calibrated parts in the device characterization which are not taken into account in typical device characterization using on-wafer calibrations. The measured results of three BJTs embedded on test structures using on-wafer calibration standards fabricated in TowerJazz 0.18-μm SiGe BiCMOS technology up to 67 GHz confirm the effects of the non-calibrated parts and demonstrate the usefulness of the proposed method for accurate device characterization at mm-wave frequencies.

8.4 References

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CHAPTER IX

24/60–GHZ CONCURRENT DUAL-BAND POWER AMPLIFIER

Advanced communication and radar systems working "concurrently" over multiple bands provide numerous advantages and have more capabilities as compared to their single-band counterparts for communications and sensing. However, multi-band circuits and systems have many intermodulation (IM) products and harmonics due to many main tones, which significantly decrease their performances such as linearity, efficiency, etc. Multi-band power amplifier (PA) is the component suffered the most from these IM products due to its highly nonlinear nature. Various multi-band PAs have been developed, e.g., [9-1] and [9-2].

In this chapter, we report a concurrent dual-band PA centered at 24 and 60 GHz designed on a 0.18-μm BiCMOS process. As shown in Fig. 9.1, the power amplifier is used as the last amplifier in the phased-array transmitter, which facilitates high output power handling with a decent efficiency. The resonators having a dual-passband at 24 (f_1) and 60 (f_2) GHz and a single stop band at 42 GHz are employed in the PA design so that its input and output impedances are matched in the dual bands for high gain and output power, respectively. The single stop band at 42 GHz is selected to minimize the 2nd IM (f_2-f_1) and the 2nd harmonic ($2f_1$), which significantly affect the third-order IM (IM3) product. For more accurate linearity simulations for a concurrent dual-band PA, a technique using three tones is proposed and investigated.

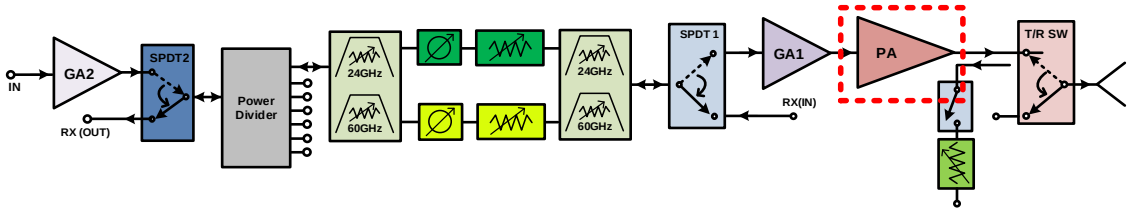


Fig. 9.1. Power amplifier in the phased-array transmitter (as shown in the dotted box).

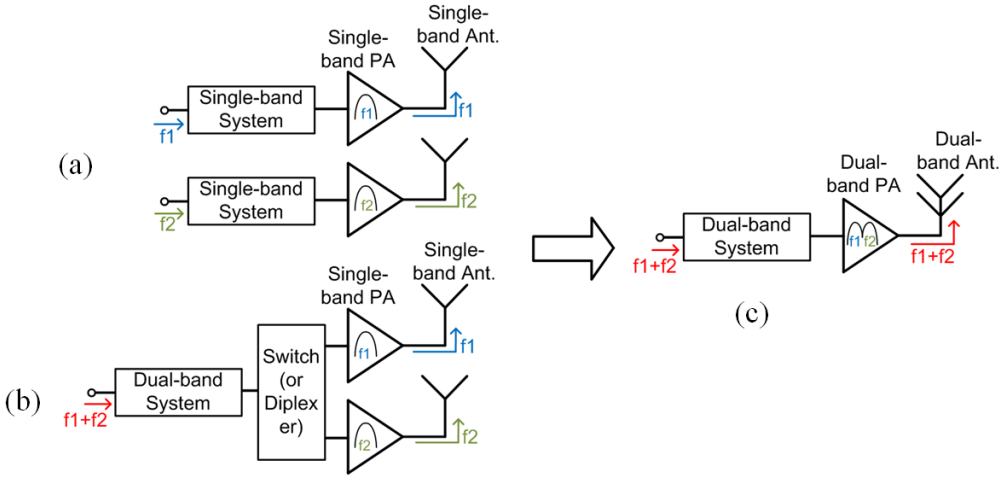


Fig. 9.2. Conventional (a) multi-path and (b) selectable/diplexing dual-band transmitters. (c) Proposed concurrent dual-band transmitter.

9.1 Concurrent Dual-Band Power Amplifier

9.1.1 Proposed Topology and Design Challenge

Figs. 9.2(a) and (b) show the block diagram of the conventional dual-band transmitters consisting of two PAs, antennas, etc. Fig. 9.2(c) shows a simpler transmitter architecture that combines two single-band PAs into a concurrent dual-band PA, which enables reduced size, insertion loss (better efficiency), and power consumption. The concurrent dual-band PA, however, has more IM products and harmonics as compared to its single-band counterparts due to the dual main tones injected as shown in Fig. 9.3(a). It

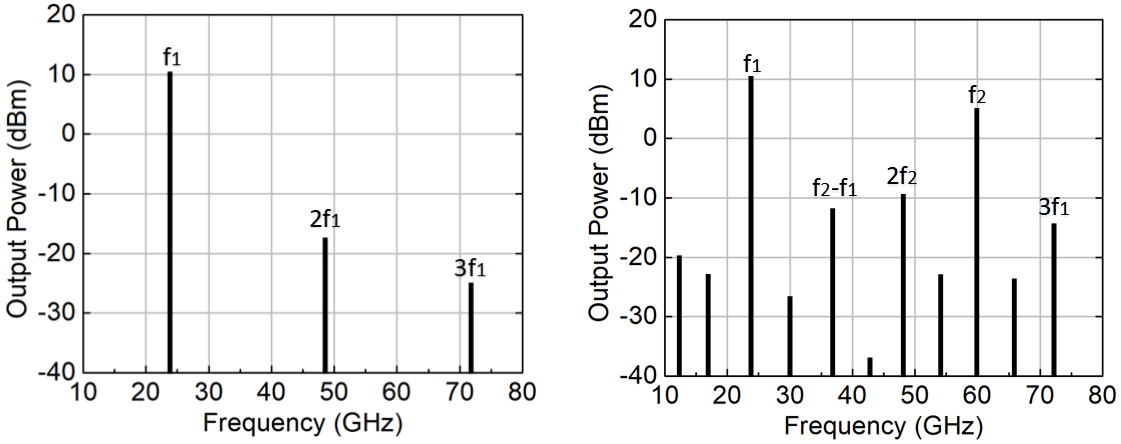


Fig. 9.3. (a) Harmonics by the single main tone at f_1 in a conventional single-band PA, and (b) IM products and harmonics caused by the dual main tones at f_1 and f_2 in the concurrent dual-band PA.

is desirable to filter out all of the IM products and harmonics to improve the linearity of PA. However, the more filtering functions lead to the more insertion loss by the LC elements. In Sec. 9.1.3, we investigate the interferences, which are most significant to the linearity. Eliminating these interferences only would minimize the rejection filtering and hence effectively improving the linearity of a concurrent dual-band PA.

A two-tone test in [9-1] is widely used to verify the IM3 products and the linearity of amplifiers. However, the two-tone test is only usable for single-band amplifiers but not concurrent dual-band amplifiers. So, an advanced method to verify the IM3 products of the concurrent dual-band amplifiers/PAs is proposed in Sec. 9.1.2, which is named three-tone test.

A concurrent PA operates at two different bands simultaneously. So, the input and output should be concurrently matched at two different frequencies. As shown in Fig. 9.4,

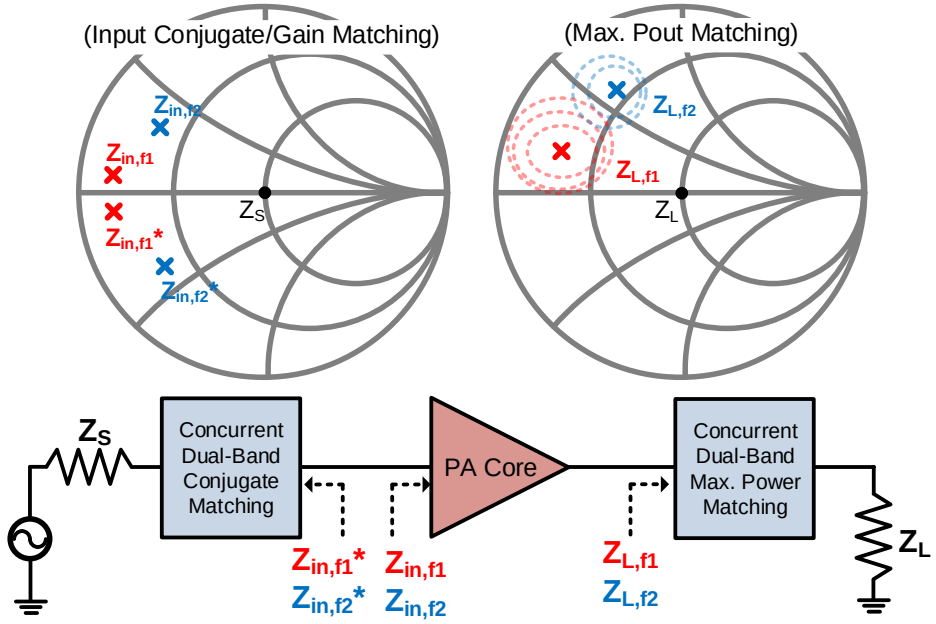


Fig. 9.4. Dual-point input/output matching in a concurrent dual-band PA design

the input is matched for the high gain and the output is matched for the high output power at the two frequency points, respectively. To realize the dual-point matching, dual-band resonators should be used for the matching networks, which will be introduced in Sec. 9.1.4.

9.1.2 Three-Tone Test for Concurrent Dual-Band Power Amplifiers

A two-tone test is used to verify the linearity of single-band PAs based on the IM3 products. However, it is not usable for concurrent dual-band PAs or amplifiers. The concurrent dual-band PA should be tested taking the two frequency bands into account simultaneously. So, we propose a three-tone test as an alternative.

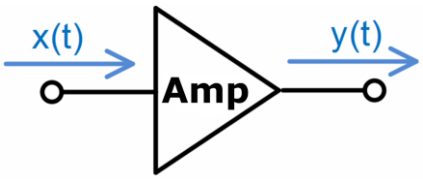
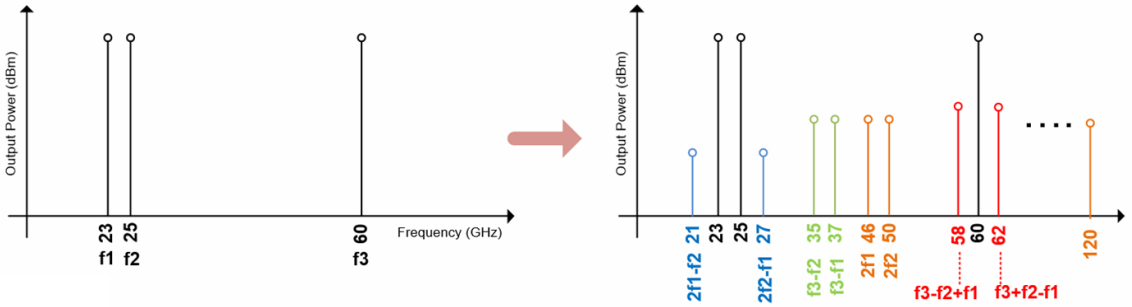
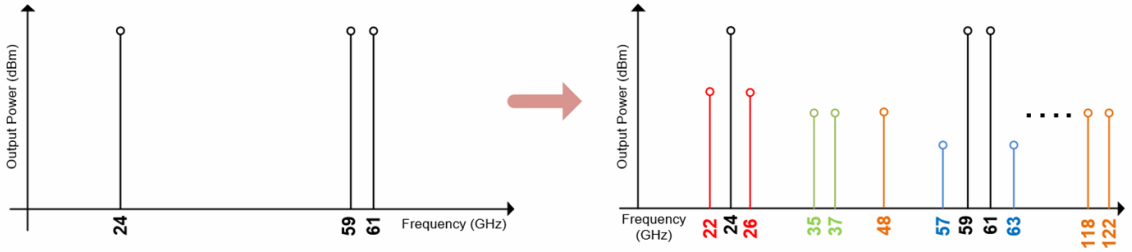


Fig. 9.5. Nonlinear amplifier with the three-tone injected signal.



(a)



(b)

Fig. 9.6. The three tones injected (a) at 23, 25 and 60 GHz and (b) 24, 59, and 61 GHz, and their IMD products and harmonics.

The concept of the three-tone test for the concurrent dual-band amplifiers is similar to the two-tone test for the single-band amplifiers. Both are used to verify the linearity of amplifiers based on the magnitude of the IM3 products located at nearby fundamentals. The IM3 products are too close to be filtered out and they are growing three times faster than the fundamentals.

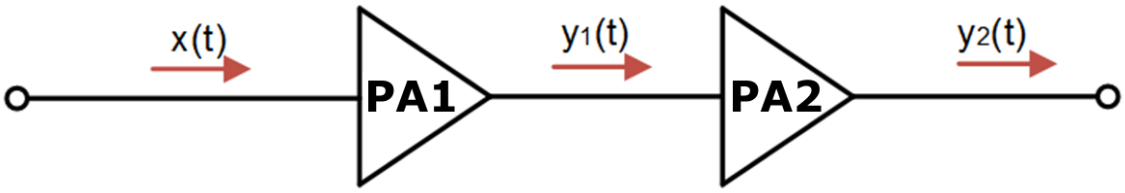


Fig. 9.7. Cascaded 2-stage PA with the three-tone input signal.

If we assume the input signal of an amplifier in Fig. 9.6 as

$$x(t)=A\cos\theta_1+A\cos\theta_2+A\cos\theta_3 \tag{9.1}$$

where $\theta=\omega t$, the output signal is obtained as

$$\begin{aligned} y(t)\approx&\left(\alpha_1+\frac{15}{4}\alpha_3A^2\right)A\cos\theta_1+\left(\alpha_1+\frac{15}{4}\alpha_3A^2\right)A\cos\theta_2+\left(\alpha_1+\frac{15}{4}\alpha_3A^2\right)A\cos\theta_3\\ &+\alpha_2A^2\left\{\frac{1}{2}\cos2\theta_1+\frac{1}{2}\cos2\theta_2+\frac{1}{2}\cos2\theta_3+\cos(\theta_3-\theta_1)+\cos(\theta_3-\theta_2)+....\right\}\\ &+\alpha_3A^3\left\{\frac{3}{4}\cos(2\theta_2-\theta_1)+\frac{3}{4}\cos(2\theta_1-\theta_2)+\frac{3}{2}\cos(\theta_2+\theta_3-\theta_1)+\frac{3}{2}\cos(\theta_1+\theta_3-\theta_2)+.....\right\} \end{aligned} \tag{9.2}$$

The third term in (9.2) contains the conventional IM3 products ($2\omega_2-\omega_1$ and $2\omega_1-\omega_2$) and newly generated IM3 products ($\omega_2+\omega_3-\omega_1$ and $\omega_1+\omega_3-\omega_2$) by the three tones. It is noted that the magnitudes of the new IM3 products are bigger than the conventional IM3. The three tones can be injected in two different ways, in order to verify the linearity of concurrent dual-band amplifiers. Fig. 9.6 conceptually shows the two ways of injection for a 24/60-GHz concurrent dual-band PA or amplifier. Fig. 9.6(a) shows the IM3 products at $2\omega_2-\omega_1$, $2\omega_1-\omega_2$, $\omega_2+\omega_3-\omega_1$, and $\omega_1+\omega_3-\omega_2$, which are derived from (9.2). They are located close to the fundamental tones at 23, 24, and 60 GHz, which should be small for a high-linear PA design. Similarly, the second three-tone test in Fig. 9.6(b) has the IM3

products close to the main tones. We investigate the first way of the three-tone test in Fig. 9.6(a) only since the analyses of those in Fig. 9.6 are the same.

9.1.3 Cascaded PA with Three-Tone Test and Significant IM Products

The three-tone test is proposed in the previous chapter, and the more IM3 products are observed in the concurrent dual-band amplifier. In this section, we investigate it to minimize the IM3 products in the cascaded 2-stage PA as shown in Fig. 9.7. Similar to the dual-tone results in [9-1], the output signal of the PA by the three-tone input signal is expressed as

$$\begin{aligned} y_2(t) = {} & \alpha_1\beta_1 A(\cos\omega_1 t+\cos\omega_2 t+\cos\omega_3 t) \\ & +\left(\frac{3\alpha_3\beta_1}{4}+\frac{3\alpha_1\alpha_2\beta_2}{2}+\frac{3\alpha_1^3\beta_3}{4}\right)A^3\{\cos(2\omega_1-\omega_2)t+\cos(2\omega_2-\omega_1)t\} \\ & +\left(\frac{3\alpha_3\beta_1}{2}+3\alpha_1\alpha_2\beta_2+\frac{3\alpha_1^3\beta_3}{2}\right)A^3\{\cos(\theta_2+\theta_3-\theta_1)+\cos(\theta_1+\theta_3-\theta_2)\}+..... \end{aligned} \quad . \qquad (9.3)$$

With (9.2) and (9.3), we can make the following observations. Firstly, the fundamental input tones are amplified by α_1 in the 1st stage (PA1) and β_1 in the 2nd stage (PA2). Thus the output fundamentals are $\alpha_1\beta_1 A(\cos\omega_1 t+\cos\omega_2 t+\cos\omega_3 t)$. Secondly, the IM3 products generated by PA1 are amplified by β_1. Thus, the output IM3 products are $(3\alpha_3\beta_1/2)A^3\{\cos(\theta_2+\theta_3-\theta_1)+\cos(\theta_1+\theta_3-\theta_2)\}$. Thirdly, the PA2 senses $\alpha_1 A(\cos\omega_1 t+\cos\omega_2 t+\cos\omega_3 t)$ at its input and IM3 products are $\beta_3\alpha_1 A^3\{(3/2)\cos(\theta_2+\theta_3-\theta_1)+(3/2)\cos(\theta_1+\theta_3-\theta_2)\}$. Lastly, the 2nd order-nonlinearity in $y_1(t)$ generates components at $\theta_2+\theta_3$, $\theta_1-\theta_2$, $\theta_3-\theta_1$, $\theta_1+\theta_3$, and $\theta_3-\theta_2$. Upon experiencing a

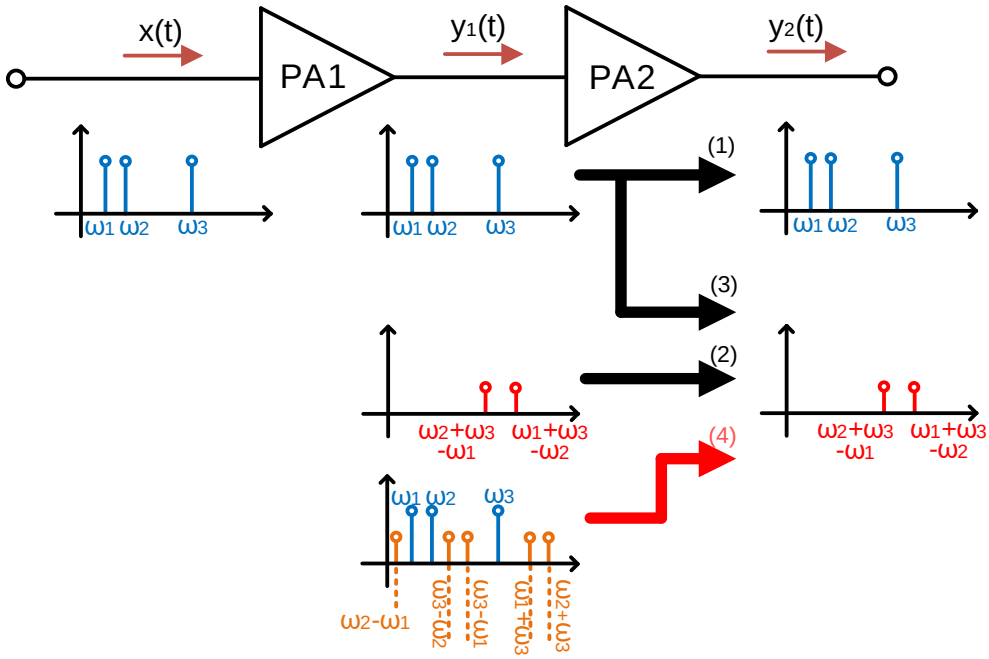


Fig. 9.8. Intermodulation mechanisms in cascade of two PAs with a three-tone input injection.

similar nonlinearity in the 2nd stage, such components are translated to $\theta_2+\theta_3-\theta_1$ and $\theta_1+\theta_3-\theta_2$. More specifically, $y_2(t)$ contains the terms such as

$$2\beta_1\{A^2\alpha_2\cos(\theta_2+\theta_3)\times A\alpha_1(\theta_1)\}$$
$$2\beta_1\{A\alpha_1(\theta_3)\times A^2\alpha_2\cos(\theta_2-\theta_1)\}$$
$$2\beta_1\{A^2\alpha_2\cos(\theta_3-\theta_1)\times A\alpha_1(\theta_2)\}$$

for the IM3 at $\theta_2+\theta_3-\theta_1$, and

$$2\beta_1\{A^2\alpha_2\cos(\theta_1+\theta_3)\times A\alpha_1(\theta_2)\}$$
$$2\beta_1\{A\alpha_1(\theta_3)\times A^2\alpha_2\cos(\theta_2-\theta_1)\}$$
$$2\beta_1\{A^2\alpha_2\cos(\theta_3-\theta_2)\times A\alpha_1(\theta_1)\}$$

for the IM3 at $\theta_1+\theta_3-\theta_2$. The resulting IM3 products can be expressed as $3\alpha_1\alpha_2\beta_1A^3\{\cos(\theta_2+\theta_3-\theta_1)+\cos(\theta_1+\theta_3-\theta_2)\}$. Based on these observations, a figure of IM mechanisms is drawn as shown in Fig. 9.8. The interferences at $\omega_2-\omega_1$, $\omega_3-\omega_2$, $\omega_3-\omega_1$,

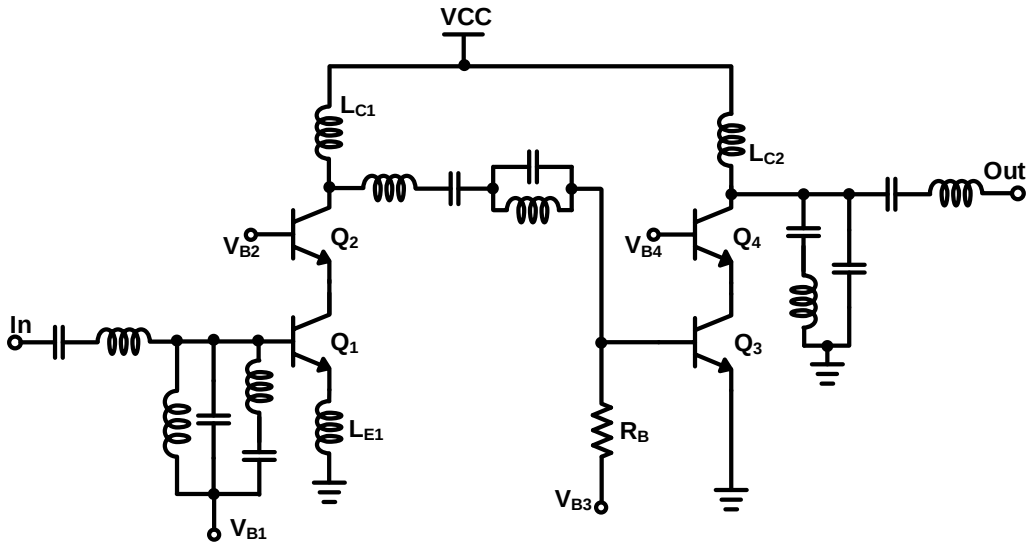


Fig. 9.9. 24/60-GHz concurrent dual-band 2-stage PA for low IM3 products.

$\omega_1+\omega_3$, and $\omega_2+\omega_3$ are mixed with fundamentals, which increases IM3 products at $\omega_2+\omega_3-\omega_1$ and $\omega_1+\omega_3-\omega_2$. So, the IM3 products can be reduced by filtering out the interferers in a multi-stage PA/amplifier design. In addition, the conventional IM3 products at $2f_1$-f_2 and $2f_2$-f_1 can be reduced by filtering out the 2nd harmonics at $2f_1$, $2f_2$, and $2f_3$ as discussed in [9-1].

9.1.4 Concurrent Dual-Band Power Amplifier Design & Simulation

Based on the foregoing studies, a 24/60-GHz concurrent dual-band PA is designed with TowerJazz 0.18-μm BiCMOS technology [9-2] as shown in Fig. 9.9. For the concurrent dual-band input/inter-stage/output matching, the dual-band matching networks are employed. As discussed in Sec. 9.1.3, the interferences at f_2-f_1 (2 GHz), f_3-f_2 (35 GHz), f_3-f_1 (37 GHz), f_1+f_3 (48 GHz), f_2+f_3 (85 GHz), $2f_1$ (46 GHz), $2f_2$ (50 GHz), and $2f_3$ (120

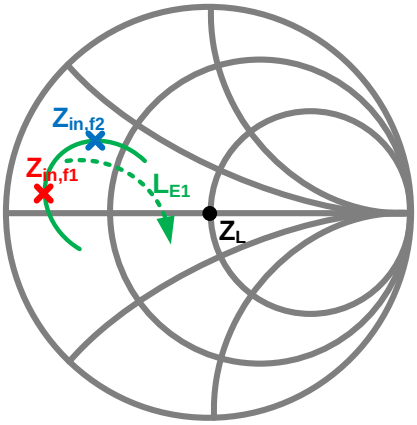


Fig. 9.10. Input matching with an inductive degeneration (L_{E1}).

GHz) should be minimized to reduced IM3 products at $f_2+f_3-f_1$ (62 GHz), $f_1+f_3-f_2$ (61 GHz), $2f_1-f_2$ (21 GHz), and $2f_2-f_1$ (27 GHz). For the PA, the dual-band matching networks are designed to have the suppression point at 42 GHz to filter out the interferences at 35, 37, 46, 48, 50 GHz overall. The remaining interferences at 2, 85, and 120 GHz are negligible since the intrinsic filtering response of the PA can suppress them sufficiently. The 1st and 2nd stages are designed for Class A and B operations, respectively, in order to have high efficiency. The inductive degeneration (L_{E1}) is used for the stability and input matching purposes. The matching effect is shown in Fig. 9.10 on Smith Chart. Both stages have the cascode structure, which increases the isolation from output to input, hence minimizing the miller effect. Also, the cascade structure allows more voltage headroom which is very attractive for our low-voltage transistor design.

The simulated gain (S21) and input (S11) and output (S22) return losses of the 2-stage PA are shown in Fig. 9.11(a). As discussed previously, the stop band between the

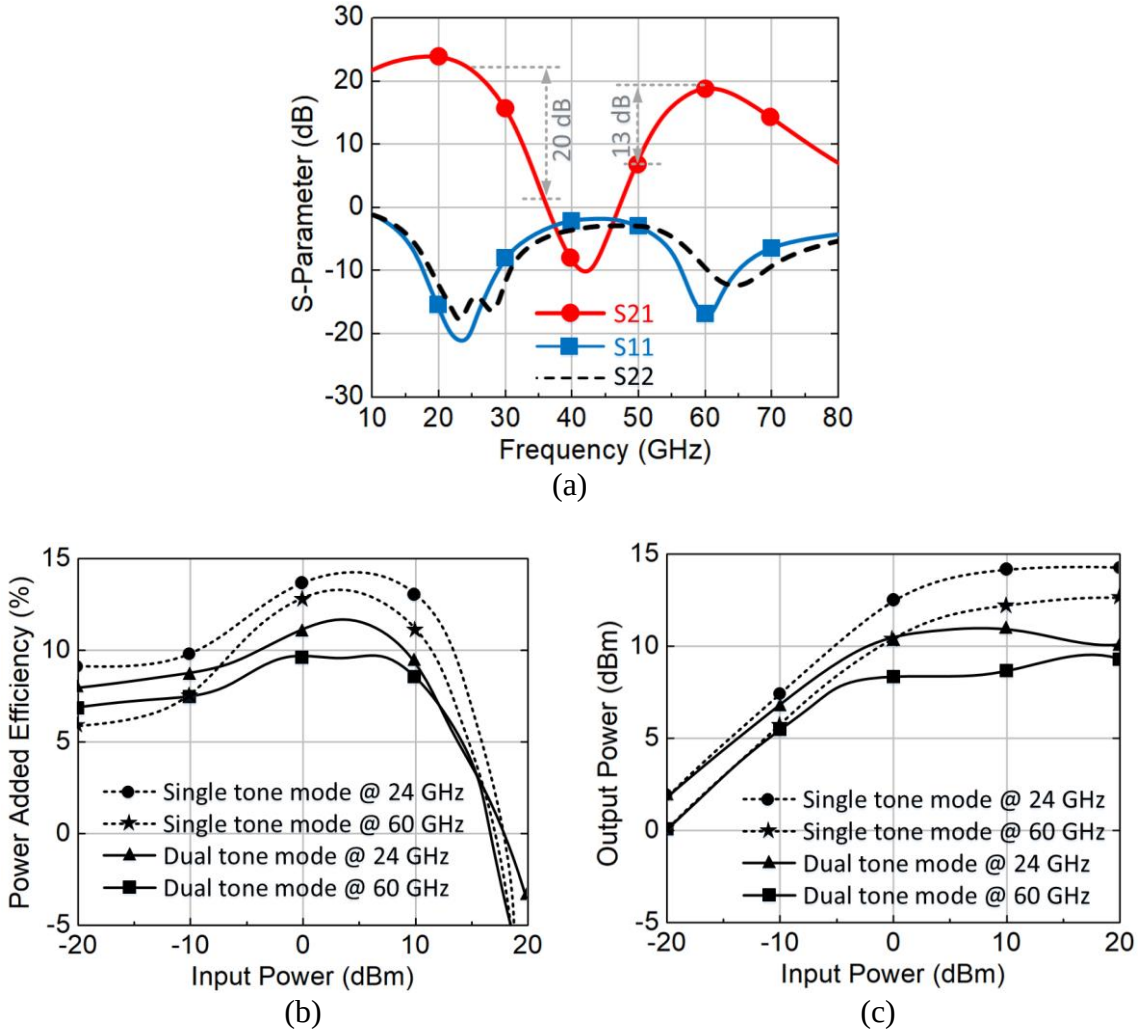


Fig. 9.11. Simulations of the concurrent dual-band PA: (a) Gain, and input/output return loss, (b) power added efficiency, and (c) output P1dB for the single- and dual-tone modes.

dual bands is located at around 42 GHz to suppress the spreading interferences from 35 to 50 GHz.

For the power added efficiency (PAE) and the output 1-dB compression point (OP1dB) simulations shown in Figs. 9.11(b) and (c), two injection modes (single-tone and dual-tone modes) are employed. For the single-tone mode, only one main tone such as 24-

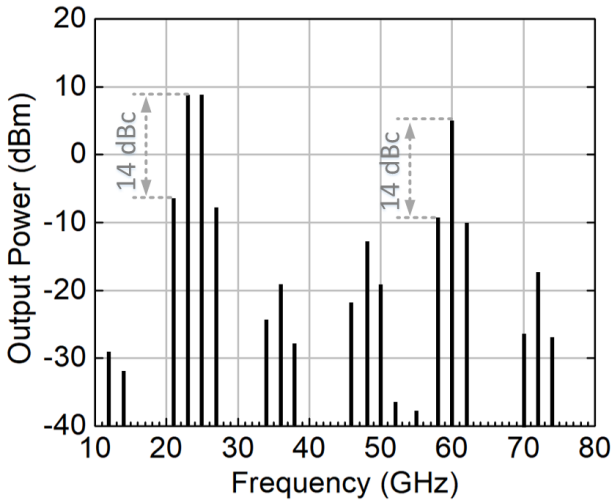


Fig. 9.12. Frequency specturm by the three-tone test with -15, -15, and -13-dBm inputs at 23, 25 and 60 GHz, respectively.

Table 9.1
Simulations of the concurrent dual-band PA with single-tone and dual-tone modes

Performance \ Mode	Single-tone mode		Dual-tone mode	
Freq. (GHz)	24	60	24	60
Gain (dB)	22	19	22	19
Input Return Loss (dB)	20	17	20	17
Output Return Loss (dB)	18	10	18	10
OP1dB (dBm)	13	10	9	7
PAE_{max} (%)	14	13	12	9.5

or 60-GHz tone is individually injected into the PA while the two main tones are simultaneously injected in the dual-tone mode simulation. As shown in Fig. 9.3, the dual-tone mode should be used for accurate P1dB simulations in a concurrent dual-band PA design.

Table 9.1 compares the simulations for the dual-tone mode to those for the single-tone modes. As expected, from the more IM products and harmonics incurred, the dual-tone mode simulation leads to lower OP1dB and PAE at each center frequency, which are more reliable than the results obtained in the conventional single-tone modes. Fig. 9.12 shows a simulated output spectrum with -15, -15, and -13-dBm input powers at 23, 25 and 60 GHz, respectively (three-tone test). It shows that the output power of the fundamental tones at 23, 25, and 60 GHz are 9, 9, and 5 dBm, respectively. The IM3 products are 14-dBc smaller than the fundamentals. The interferences from 35 to 50 GHz are suppressed under –10 dBm. Table 9.1 compares the simulations for the dual-tone mode to those for the single-tone modes. As expected, from the more IM products and harmonics incurred, the dual-tone mode simulation leads to lower OP1dB and PAE at each center frequency, which are more accurate than the results obtained in the conventional single-tone modes.

9.2 Conclusion

A 0.18-μm SiGe BiCMOS 24/60 GHz concurrent dual-band PA with a dual-band resonator having an interference rejection response is designed. The results show that the PA's input impedances are well matched in the dual pass bands, and the significant IM products and the 2nd harmonic are sufficiently filtered out in the stop band. The dual main tones employed for the PAE and OP1dB simulations show more accurate results than those using the conventional single-tone modes, demonstrating that the dual- or multi-tone mode simulation and measurement are necessary for the multi-band circuit and system design for more accurate characterization. The proposed technique of filtering out the

undesired IM products and harmonics is attractive for the design of the multi-band circuits and systems with high linearity.

9.3 References

[9-1] K. Kim and C. Nguyen, "A concurrent Ku/K/Ka tri-band distributed power amplifier with negative-resistance active notch using SiGe BiCMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 1, pp. 125–136, Jan. 2014.

[9-2] C. Huynh and C. Nguyen, "New technique for synthesizing concurrent dual-band impedance-matching filtering networks and 0.18-μm SiGe BiCMOS 25.5/37-GHz concurrent dual-band power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 11, pp. 3927–3939, Nov. 2013.

CHAPTER X

24/60-GHZ DUAL-BAND 8-WAY POWER DIVIDER

A divider has a role to separate the signal of the upconversion mixer and transfer to the multiple array channels in phased-array transmitters. An 8-way power divider is needed to facilitate multiple channels in the phased-array transmitter as shown in Fig. 10.1. In this chapter, an 8-way power divider with concurrent dual-band response centered at 24 and 60 GHz is designed. The 8-way power divider can be used for the 7-channel phased-array transmitter by terminating one of the output ports with a 50-ohm resistor.

10.1 Dual-Band Power Divider Design and Simulations

Fig. 10.2 shows a conventional Wilkinson power divider, which is widely used due to its simplicity, decent isolation, input/output matching condition, etc. The transmission line in the power divider can be expressed as a pi-type network as shown in Fig. 10.3, and the parameters of the network are calculated with

$$Z_e = \frac{Z_0}{\sin\theta_e} \tag{10.1}$$

$$\theta_e = \sin^{-1}\left(\frac{Z_0}{Z_e}\right) \tag{10.2}$$

$$B_e = \frac{\cos\theta_0}{Z_e \sin\theta_e} \, . \tag{10.3}$$

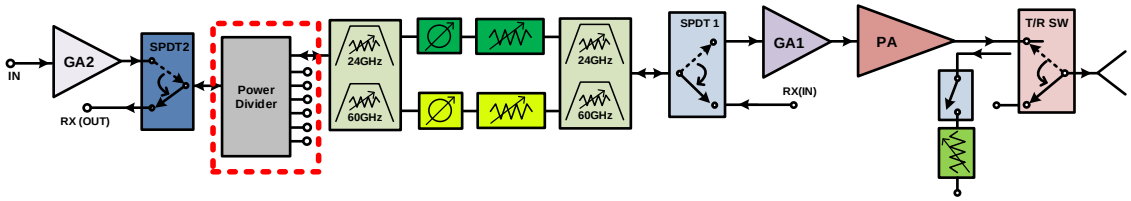


Fig. 10.1. 8-way power divider in the phased-array transmitter (in the dotted box).

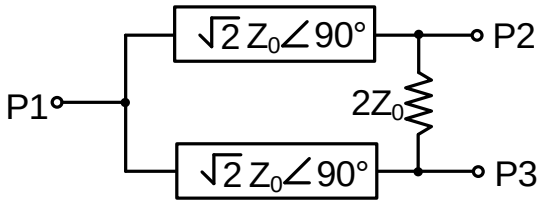


Fig. 10.2. Conventional Wilkinson power divider.

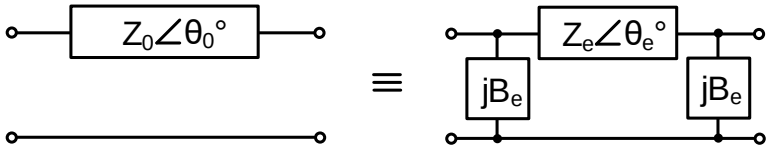


Fig. 10.3. Transmission line and its equivalent pi-type network.

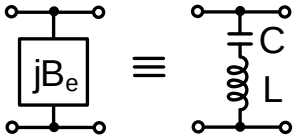


Fig. 10.4. Shunt susceptance and its equivalent LC resonator.

To design a concurrent dual-band divider, the shunt susceptance (β_e) can be replaced with the equivalent LC resonator in Fig. 10.4. The capacitance and inductance in the resonator can be expressed as

$$L=\frac{1}{\omega_0\beta_e\left(\frac{\omega_0}{\omega}-\frac{\omega}{\omega_0}\right)} \tag{10.4}$$

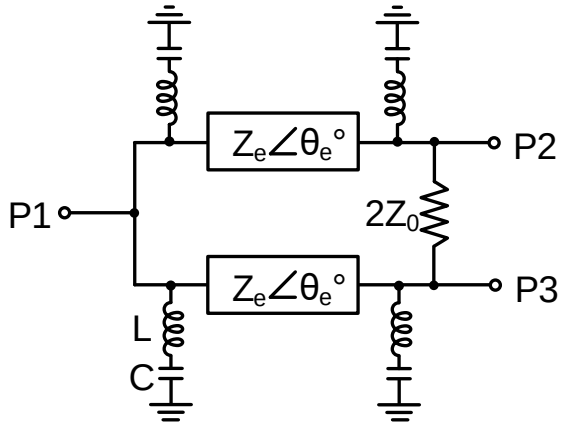


Fig. 10.5. Dual-band divider with equivalent transmission lines and resonators.

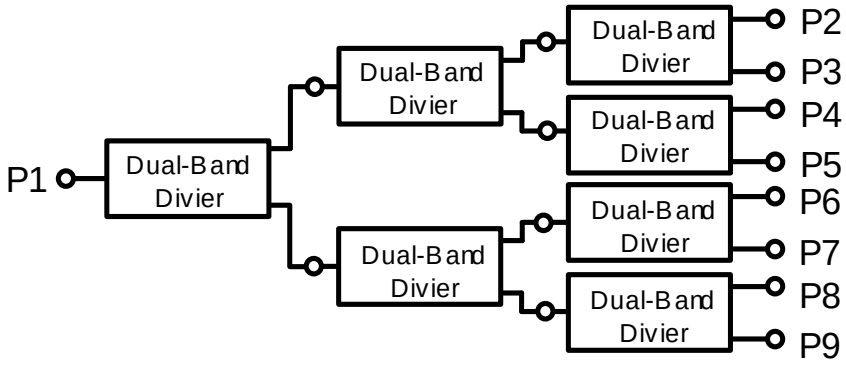


Fig. 10.6. 8-way dual-band divider consisting of the divider in Fig. 10.5.

$$C=\frac{1}{\omega_0^2 L} \tag{10.5}$$

$$\omega_0=\sqrt{\omega_1\omega_2}\ . \tag{10.6}$$

So, the dual-band divider can be designed as shown in Fig. 10.5, and it can be extended to 8-way outputs as shown in Fig. 10.6. The 8-way dual-band is simulated and the results are shown in Fig. 10.7. At 24 GHz, the insertion loss (S21), return loss (S11), and isolation

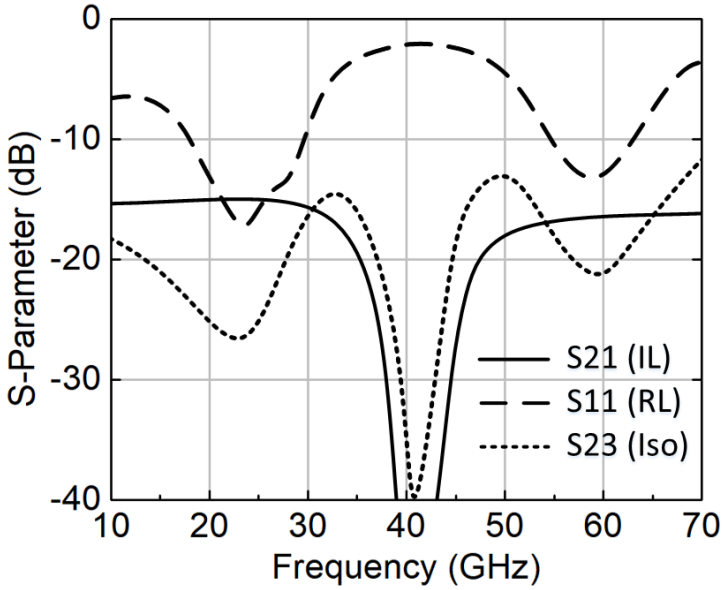


Fig. 10.7. Simulations of the 8-way dual-band divider in Fig. 10.6.

(S23) at 24 GHz are 15, 16, and 25 dB, respectively, and 16, 12, and 21 dB at 60 GHz, respectively.

APPENDIX A

44-GHZ CMOS RFIC DUAL-FUNCTION ATTENUATOR WITH BAND-PASS-FILTER RESPONSE*

Attenuators and band-pass filters (BPFs) are widely employed in communication and radar systems as amplitude controllable and frequency selective circuits, respectively. To achieve both band-pass filtering and attenuating responses in systems, BPF and wideband attenuator are typically cascaded together as depicted in Fig. A.1(a). This conventional approach, integrating two individual components, leads to an overall large circuit size and high insertion loss. To alleviate this problem, a dual-function attenuator incorporating an embedded band-pass filtering function as part of the attenuation circuitry could be employed as described in Fig. A.1(b). Similar design concepts incorporating frequency selectivity into a non-filtering circuit have been investigated for Wilkinson power divider [A-1] and 90-deg hybrid coupler [A-2]. An attenuator was designed using a BPF topology to absorb the parasitic capacitances, which affect the bandwidth [A-3]. However, the design does not display a band-pass filtering function with distinguished pass-band and stop-band responses. Moreover, its attenuation shape is directly affected by the adjusted resistance for various attenuation levels. An adaptive method for designing an attenuator that behaves explicitly as a BPF has not yet been developed despite their

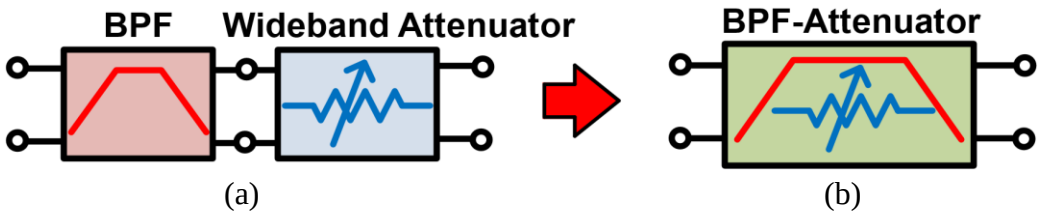


Fig. A.1. Band-pass filtering and attenuating responses realized with (a) cascaded BPF and attenuator and (b) attenuator having dual-function of attenuation and band-pass filtering.

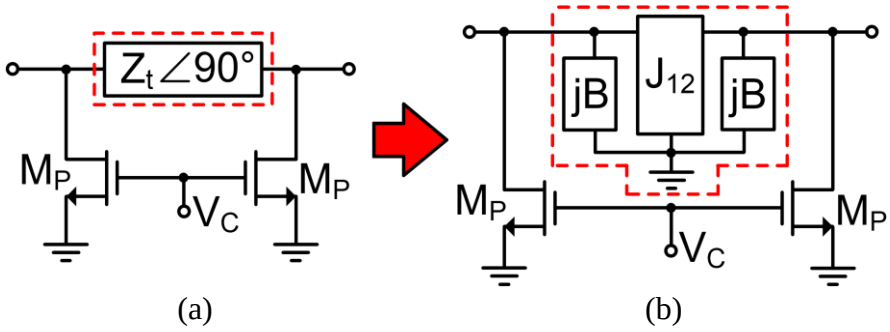


Fig. A.2. Attenuator employing (a) a quarter-wavelength line and (b) a 2nd-order J-inverter BPF (shown inside the dashed boxes).

usefulness for microwave and millimeter wave systems, particularly those employing silicon-based CMOS/BiCMOS radio frequency integrated circuits (RFICs) whose real estate is expensive and insertion loss is relatively high due to lossy silicon substrates.

This paper presents a new attenuator architecture having both attenuating and band-pass filtering functions along with the design formulas. A 3-bit CMOS dual-function band-pass step attenuator is designed and fabricated using a 0.18-μm BiCMOS technology and achieves measured insertion loss of 4.5 dB, RMS amplitude error of 0.85 dB, RMS phase error of 2.8° and input P1dB greater than 20 dBm at 44 GHz, and stop-band rejections greater than 18 dB at 24 and 64 GHz.

A.1 Circuit Design

Fig. A.2(a) shows a conventional wideband attenuator employing a $\lambda/4$ transmission line of characteristic impedance Z_t. The $\lambda/4$ transmission line could be substituted by an equivalent lumped-element Pi- or T-network for size reduction, which is useful for RFIC design. Using a Pi/T lumped-element network for the attenuator, however, generally leads to a low-pass filter response. In order to tailor the low-pass response to achieve certain specifications such as desired cutoff frequency, selectivity, etc., further design techniques need to be employed. On the other hand, configuring the $\lambda/4$ transmission line so that it behaves as a BPF itself could simplify the design of the attenuator with desired frequency responses.

We consider a 2^{nd}-order BPF employing an admittance inverter (J-inverter) as shown in the dashed box of Fig. A.2(b). The J-inverter theoretically functions like a $\lambda/4$ transmission line of characteristic admittance J_{12} (mho) at all frequencies [A-4] and the susceptance B is zero at the BPF's center frequency. It is intuitively expected, from the response of the considered 2^{nd}-order BPF, that it could be used to replace the $\lambda/4$ transmission line in the conventional attenuator for the design of the dual-function band-pass attenuator illustrated in Fig. A.1(b). This results in the dual-function band-pass attenuator topology as shown in Fig. A.2(b).

A.1.1 Design Formulas

The characteristic impedance Z_t of the $\lambda/4$ transmission line and the on-resistance R_{on} of the transistor M_P in Fig. A.2(a) can be expressed as

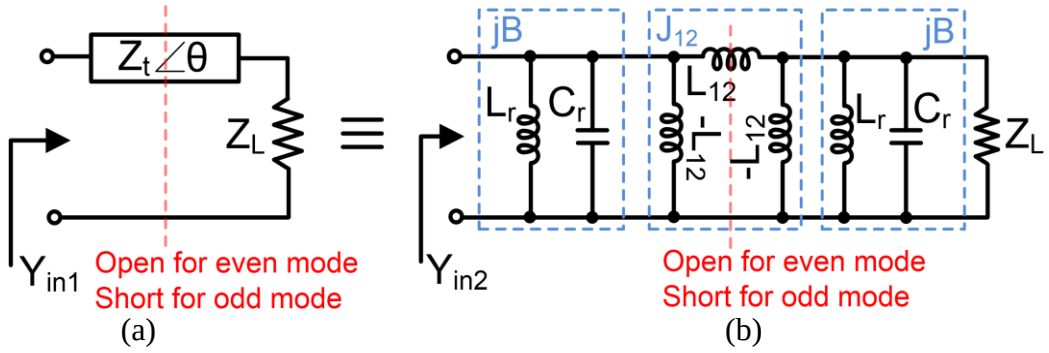


Fig. A.3. Equivalence between (a) a transmission line and (b) a 2nd-order J-inverter BPF.

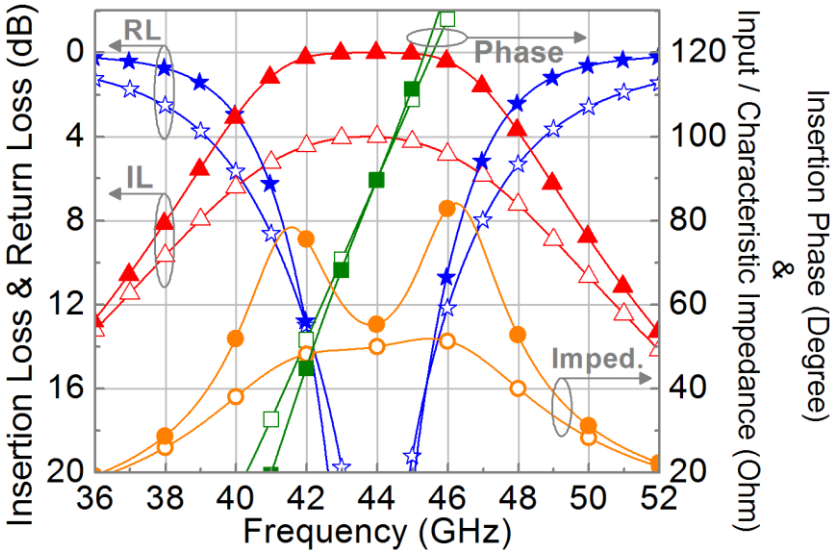


Fig. A.4. Simulation results for the constituent BPF (filled symbol) and 1-bit 4-dB dual-function band-pass attenuator (non-filled symbol). Input impedance: Z_{in2}. Characteristic impedance: Z_t.

$$Z_t = \frac{Z_L(10^{-A/10}+1)}{2\sqrt{10^{-A/10}}} \tag{1}$$

$$R_{on} = \frac{Z_L(10^{-A/10}+1)}{10^{-A/10}-1} \tag{2}$$

where A denotes the attenuation in dB and Z_L represents the termination impedance at the

input and output of the attenuator [A-5]. The size of M_P is determined based on the on-resistance calculated from (2).

The design formulas for the dual-function band-pass attenuator can be derived by enforcing the equality between the $\lambda/4$ transmission line and the 2nd-order J-inverter BPF. The formulation is facilitated by applying the even- and odd-mode excitations at the input and output ports of the attenuator in Fig. A.2, which are made possible from the inherent symmetry of the attenuator. Fig. A.3 shows the equivalence between a transmission line and a 2nd-order J-inverter BPF, terminated with Z_L, in which an L-coupled Pi-network is employed for J_{12} and B consists of L_r and C_r. The transmission line and BPF has an open or short circuit at the dotted red line corresponding to the even- or odd-mode excitation, respectively. By equating the even- and odd-mode input admittances of the corresponding transmission line and BPF, L_{12} can be derived as

$$L_{12} = Z_t \sin\theta / \omega_0 \tag{3}$$

where Z_t and θ are the characteristic impedance and electrical length of the transmission line, respectively, and ω_0 is the center frequency of the BPF. Equating Y_{in1} and Y_{in2} yields the admittance of the inverter

$$J_{12} = \sqrt{\left\{Y_{in1} - jY_t\left(\tan\frac{\theta}{2} - \csc\theta\right)\right\}\left\{Y_L + jY_t\left(\tan\frac{\theta}{2} - \csc\theta\right)\right\}} \ . \tag{4}$$

The shunt capacitance and inductance of the 2nd-order J-inverter BPF can be obtained, following the low-pass to band-pass mapping [A-6], as

$$C_r = \frac{J_{12}\sqrt{g_1 g_2}}{\omega_0\left(\frac{\omega_2}{\omega_0} - \frac{\omega_0}{\omega_2}\right)} \tag{5}$$

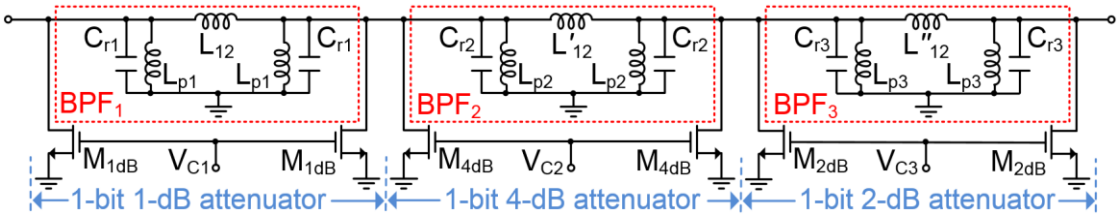
$$L_r = \frac{1}{\omega_0^2 C_r - \omega_0 Y_t \left(\tan\frac{\theta}{2} - \csc\theta \right)} \tag{6}$$

where g_1 and g_2 are the values of the 1st and 2nd elements of the low-pass prototype filter, respectively, and ω_2 is the upper-pass-band cut-off frequency of the BPF.

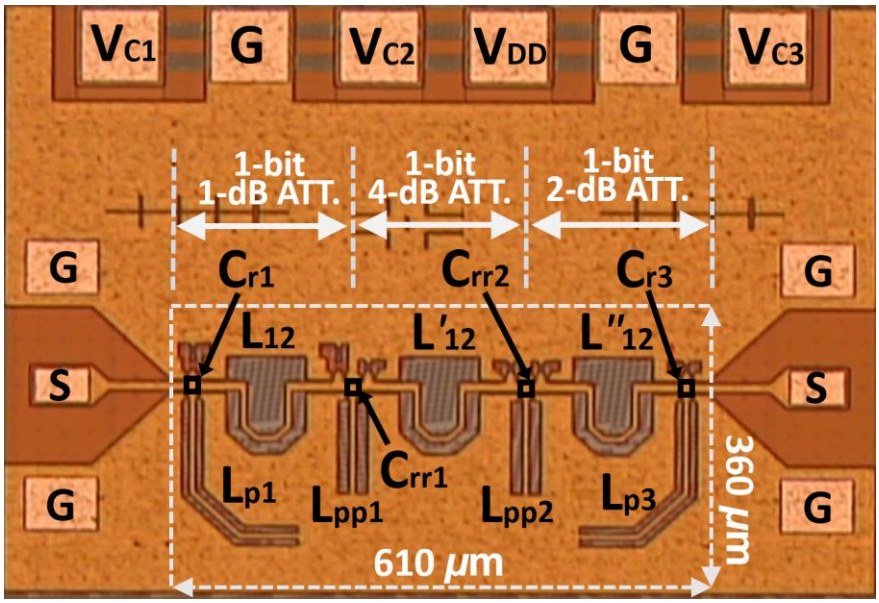
As an example to verify the design formulas derived for the dual-function band-pass attenuator, (1)–(6) are used to design a dual-function band-pass attenuator having 4-dB attenuation, 40–48 GHz pass-band, and Butterworth response, yielding Z_t = 55.4 Ω, R_{on} = 116 Ω, L_{12} = 200 pH, C_r = 530 fF, and L_r = 24.7 pH. The simulations of the dual-function band-pass attenuator and the (constituent) BPF, with the yielded values, are shown in Fig. A.4. The dual-function band-pass attenuator and BPF are simulated with load impedances of 50 and 55.4 Ω, respectively. The simulated results in Fig. A.4 shows that, at the design center frequency of 44 GHz, the BPF has Z_t = 55.4 Ω and electrical length of 90°, and the dual-function band-pass attenuator has Z_{in2} = 50 Ω, 90° electrical length and 4-dB attenuation, which demonstrate the validity of the derived formulas (3)–(6).

A.1.2 Design of 3-bit CMOS Dual-Function Band-Pass Attenuator

A 3-bit CMOS dual-function band-pass step attenuator is designed and fabricated with TowerJazz 0.18-μm BiCMOS technology [A-7] as shown in Fig. A.5. The band-pass attenuator consists of three individual 1-bit attenuators (1-, 2- and 4-dB) designed based on the formulas derived in Sect. II-A to control the amplitude with a 1-dB step over 8 states. The adjacent shunt elements are combined together as $L_{pp1} = L_{p1} // L_{p2}$, $L_{pp2} = L_{p2} // L_{p3}$, $C_{rr1} = C_{r1} + C_{r2}$, and $C_{rr2} = C_{r2} + C_{r3}$ as shown in Fig. A.5(b). It is particularly noted that the



(a)



(b)

Fig. A.5. 3-bit CMOS dual-function band-pass step attenuator: (a) schematic and (b) microphotograph. Chip size (core part): 610 × 360 μm^2.

device parasitic capacitances are added to the shunt capacitances of the constituent BPFs and would shift the BPF responses to lower frequencies. The device parasitic shunt resistances, which could be large, also increase the insertion loss of the individual attenuators as investigated in [A-8]. To overcome these problems, the body-floating technique implemented for attenuators in [A-8] is employed for the design of the shunt transistors (M_{1dB}, M_{2dB} and M_{4dB}) to minimize the effects of the parasitics. All inductors

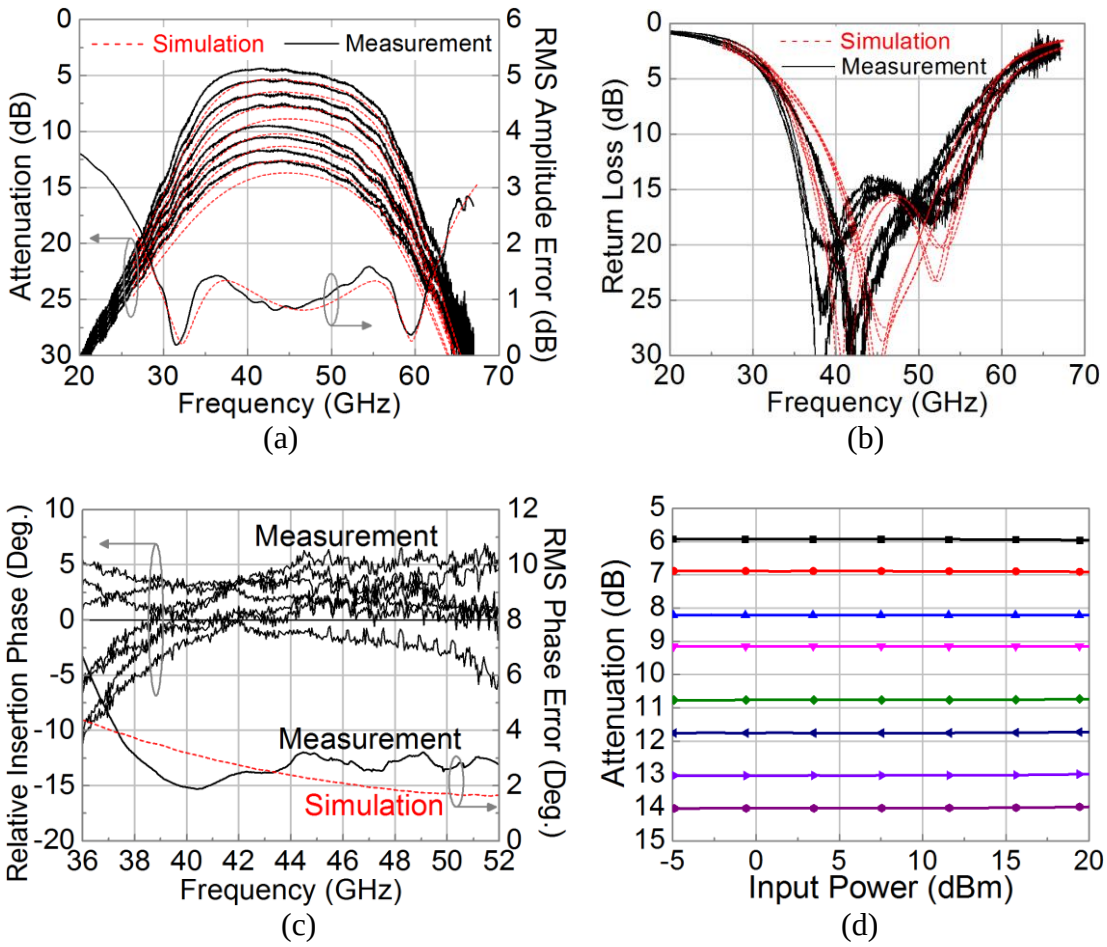


Fig. A.6. Simulated and measured (a) insertion loss and RMS attenuation error, (b) return loss, and (c) relative insertion phase and RMS phase error over 8 states of the 3-bit CMOS dual-function band-pass step attenuator. (d) Measured power handling over 8 states at 44 GHz.

are designed with coplanar waveguide considering their size and Q-factor, and MIM capacitors are employed for compactness, reliability and high Q-factor.

Figure A.6 shows the simulated and measured results of the 3-bit CMOS dual-function band-pass step attenuator. Over 36–52 GHz, the measured insertion loss and RMS amplitude error, as seen in Fig. A.6(a), are 4.4–5.9 and 0.8–1.4 dB, respectively. At

Table A.1 Comparison of CMOS attenuators

Parameter \ Ref.	[8]	[9]	[10]	[11]	This Work
Freq. (GHz)	10–67	DC–14	0.4–3.7	10–50	36–52
IL (dB)	8.4–15.2	3.7–10	0.96–2.91	2–3	4.4–5.9
No. of States	16	64	8	11	8
Desired Step (dB)	3 (digital type)	0.5 (digital type)	3±2 (analog type)	1 (digital type)	1 (digital type)
IP1dB (dBm)	> 15 (at 35GHz)	15 (at 10GHz)	> 7 (at 1GHz)	4 (at 35GHz)	> 20 (at 44 GHz)
RMS Amplitude Error (dB)	Not Available	< 0.5	Not Available	Not Available	0.8–1.4
RMS Phase Error (Deg.)	Not Available	< 4.2	Not Available	0.9–2.9	1.9–6.7
Size (mm^2)	1.45×0.53	1.25×0.4	0.75×0.37*	0.75×0.2	0.61×0.36
Process	CMOS in 0.18-μm BiCMOS	0.18-μm CMOS	0.18-μm CMOS	CMOS in 0.12-μm BiCMOS	CMOS in 0.18-μm BiCMOS
Freq. Band Selectivity	No	No	No	No	Yes (band-pass)

*This chip size includes DC and RF pads

24 and 64 GHz in the stop-band, the measured rejection relative to the insertion loss at the band-edge frequencies (36 and 52 GHz) are 19 and 18 dB, respectively, for the first attenuation state. The measured input return loss displayed in Fig. A.6(b) is more than 9.7 dB over 36–52 GHz at all attenuation states. The measured relative insertion phase and RMS phase error are 3.6–16.3° and 1.9–6.7° over 36–52 GHz, respectively, as seen Fig. A.6(c). Compared to the conventional Pi-, T- and bridged-attenuator reported in [A-9], the conventional attenuator employing $\lambda/4$ transmission line leads to lower phase deviation during the attenuation control due to the absence of large-size series transistors, which is

desired especially for phase-sensitive systems such as phased arrays. This virtue is also reflected in the developed dual-function band-pass attenuator as evidenced by the achieved RMS phase error. The measured attenuation versus input power at 44 GHz seen in Fig. A.6(d) shows that the input P1dB is higher than 20 dBm in all states. Table A.1 compares the performance of the developed dual-function band-pass attenuator to those of reported CMOS attenuators. The proposed attenuator is the only attenuator that is capable of both amplitude control and frequency-band selection.

A.2 Conclusion

A new attenuator topology having band-pass filtering response is developed and implemented at millimeter-wave frequencies centered at 44 GHz. The derived design formulas and dual-function band-pass attenuation theory are validated. The measured results of the 44-GHz CMOS 3-bit dual-function band-pass step attenuator show that the attenuator performs well in both attenuation and pass-band selection as designed with high P1dB. The developed dual-function band-pass attenuator is attractive for microwave and millimeter-wave communication and radar systems, especially for those demanding both signal amplitude control and band-pass filtering in a single component. It is particularly noted that the derived formulas could be employed not only for the proposed dual-function attenuator, but also for other multifunction components with a band-pass response, which contain $\lambda/4$ transmission lines, such as quadrature hybrids, directional couplers, power dividers, etc.

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APPENDIX B

NEW DUAL-BAND BAND-PASS FILTER DESIGN WITH ENHANCED DUAL-BAND SKIRT CHARACTERISTICS*

Frequency transformation from low-pass filter prototypes is widely used for filter design [B-1]. The conventional frequency transformation in [B-1], however, suffers from poor skirt selectivity in the high-frequency stop-band of band-pass filters (BPF), which is undesirable in modern communication and radar systems. This inferior selectivity, which causes asymmetric skirt selectivity between the low-frequency and high-frequency stop-bands, results because the conventional frequency transformation has an asymmetric frequency-mapping relation. Although more resonators can be employed in BPFs to improve the skirt characteristic, this also leads to increased insertion loss and circuit size [B-2]–[B-4]. To overcome the disadvantage of unsymmetrical stop-band responses, a novel frequency transformation concept has been proposed in [B-5].

In this chapter, a new technique for improving the stop-band response in dual-band BPFs is presented and a new dual-band BPF is demonstrated. The technique extends the single-band BPF concept [B-5] for dual-band BPFs and achieves enhanced skirt characteristics with good symmetry between the low- and high-frequency stop-bands in dual-band BPFs. The proposed dual-band concept incorporates an extra frequency

parameter into the conventional frequency transformation to provide additional suppression in the frequency domain. Modified dual-band series and shunt resonators are also proposed, analyzed, and implemented to realize the dual-band BPF.

B.1 Design Theory

B.1.1 Conventional frequency transformation method

Fig. B.1 shows the conventional frequency transformation of a low-pass response to a dual band-pass response. In the method, $-\omega_1'$ or ω_1' is transformed to ω_{11} and ω_{21} or ω_{12} and ω_{22}, respectively. ω_{r1} is the rejection frequency that makes the dual-band response possible. As shown in Fig. B.1, the rejection skirt at the high-frequency stop-band is looser than that at the low-frequency stop-band because the negative infinity point (frequency) on ω' axis is transformed to the zero point of ω axis, while the positive infinity point on ω' is transformed to the positive infinity point of ω. Such asymmetrical relation in the frequency transformation leads to a skirt imbalance and degraded BPF's selectivity. Moreover, the asymmetric skirt characteristic increases when the bandwidth is increased, and hence the conventional frequency transformation method is inappropriate for wideband and high-selectivity dual-band BPF design.

B.1.2 Proposed frequency transformation method and dual-band BPF design

Figure B.2 shows the proposed dual-pass-band frequency transformation. The enhanced selectivity at the high-frequency stop-band is achieved by adding an extra frequency parameter ω_{r2} in the high-frequency stop-band.

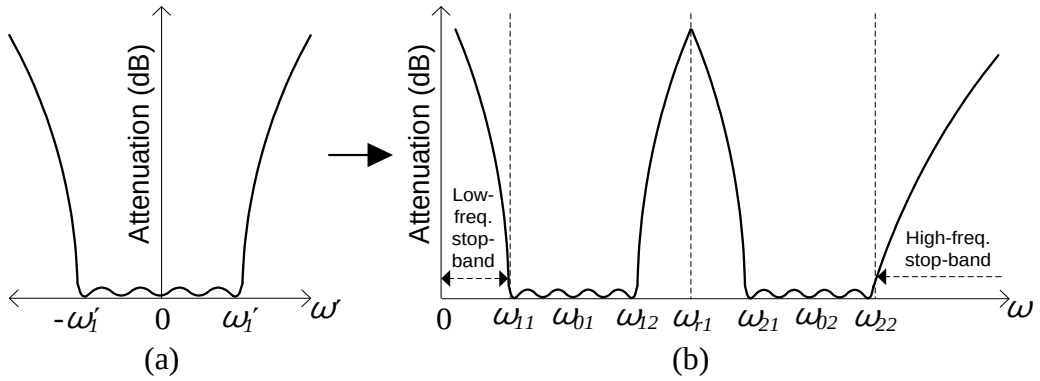


Fig. B.1. Frequency transformation from a low-pass response (a) to a dual band-pass response (b), leading to poor skirt selectivity at the high-frequency stop-band.

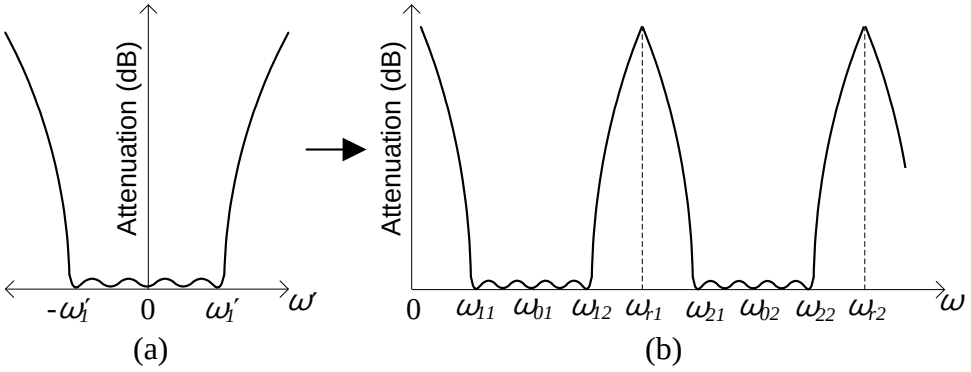


Fig. B.2. Proposed frequency transformation from a low-pass response (a) to a dual band-pass response (b) with a frequency parameter (ω_{r2}) added for improved symmetrical stop-band response.

Figures B.3(a) and (b) represent the series and parallel resonators that constitute the conventional dual-band BPF, respectively. The input reactance and susceptance of the series and shunt resonators are given as

$$jX_s = j\omega L_{ss} + \frac{1}{j\omega C_{ss}} + \frac{j\omega L_s}{1-\omega^2 L_s C_s} \tag{B.1}$$

$$jB_p = j\omega C_{pp} + \frac{1}{j\omega L_{pp}} + \frac{j\omega C_p}{1-\omega^2 L_p C_p} \tag{B.2}$$

respectively. Letting ω approaching ∞, (B.1) and (B.2) can be expressed as $X_s \approx \omega L_{ss}$ and $B_p \approx \omega C_{pp}$, which imply that the filter response at high frequencies is mainly determined by L_{ss} and C_{pp}. This leads to an idea to obtain another rejection point in the high-frequency stop-band by adding a capacitor (C_{s2k}) in parallel and inductor (L_{p2k}) in series with the series inductor (L_{s2k}) and shunt capacitor (C_{p2k}) in the conventional series and shunt resonators, respectively. The input reactance and susceptance of the resonators in Fig. B.4 are derived as

$$X_{sk} = \frac{\omega\omega_{r1}^2 L_{s1k}}{\omega_{r1}^2 - \omega^2} + \frac{\omega\omega_{r2}^2 L_{s2k}}{\omega_{r2}^2 - \omega^2} - \frac{1}{\omega C_{ssk}} \tag{B.3}$$

$$B_{pk} = \frac{\omega\omega_{r1}^2 C_{s1k}}{\omega_{r1}^2 - \omega^2} + \frac{\omega\omega_{r2}^2 C_{s2k}}{\omega_{r2}^2 - \omega^2} - \frac{1}{\omega L_{ppk}} \tag{B.4}$$

where k stands for the number of filter's order, $\omega_{r1} = 1/\sqrt{L_{s1k}C_{s1k}}$, and $\omega_{r2} = 1/\sqrt{L_{s2k}C_{s2k}}$. The center frequencies of the series resonator in Fig. B.4(a) are obtained, considering the relation $X_{sk}(\omega_{01}) = X_{sk}(\omega_{02}) = 0$, as

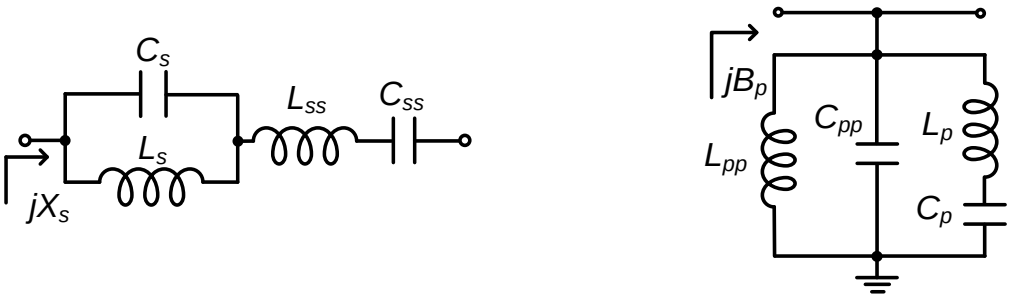
$$\omega_{01} = \sqrt{\frac{C_{T4} - \sqrt{C_{T4}^2 - 4C_{T3}\omega_{r1}^2\omega_{r2}^2}}{2C_{T3}}} \tag{B.5}$$

$$\omega_{02} = \sqrt{\frac{C_{T4} + \sqrt{C_{T4}^2 - 4C_{T3}\omega_{r1}^2\omega_{r2}^2}}{2C_{T3}}} \tag{B.6}$$

where $C_{T1k} = 1 + C_{ssk}/C_{s1k}$, $C_{T2k} = 1 + C_{ssk}/C_{s2k}$, $C_{T3k} = C_{T1k} + C_{ssk}/C_{s2k}$, and $C_{T4k} = C_{T1k}\omega_{r1}^2 + C_{T1k}\omega_{r2}^2$. The reactance relations for the series resonators in the dual-band BPF can be expressed as

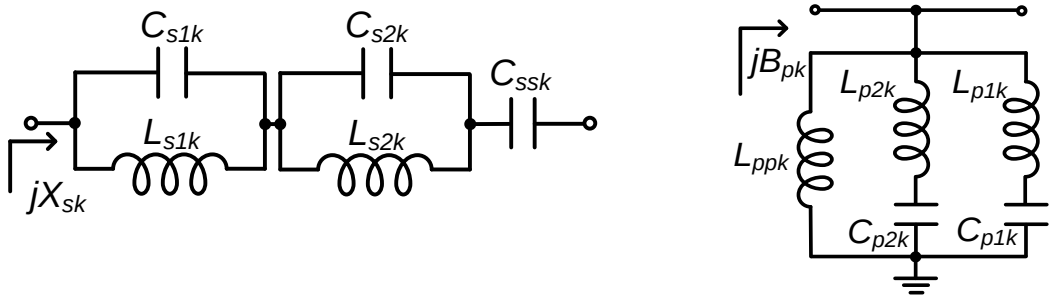
$$X_{sk}(\omega_{11}) + X_{sk}(\omega_{12}) = -\omega_1' g_k + \omega_1' g_k = 0 \tag{B.7}$$

$$X_{sk}(\omega_{21}) + X_{sk}(\omega_{22}) = -\omega_1' g_k + \omega_1' g_k = 0 \tag{B.8}$$



(a) (b)

Fig. B.3. (a) Series and (b) shunt resonators for realizing the conventional frequency transformation technique and used in the conventional dual-band BPF design.



(a) (b)

Fig. B.4. (a) Series and (b) shunt resonators for realizing the proposed frequency transformation technique and used in the proposed dual-band BPF.

$$X_{sk}(\omega_{11}) = X_{sk}(\omega_{21}) \rightarrow -\omega_1' g_k = -\omega_1' g_k \tag{B.9}$$

$$X_{sk}(\omega_{12}) = X_{sk}(\omega_{22}) \rightarrow \omega_1' g_k = \omega_1' g_k \tag{B.10}$$

where g_k indicates the k^{th} element value of the low-pass prototype filter [B-1]. Applying (B.7)–(B.10), the inductors and capacitors of the series resonator in Fig. B.4(a) can be obtained as

$$L_{s1k} = \frac{g_k}{B_{12} - (A_{12}/\alpha)} \tag{B.11}$$

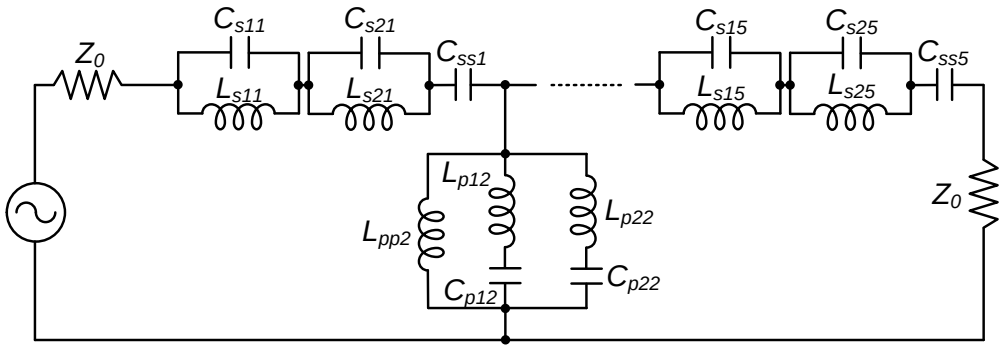


Fig. B.5. Proposed five-element dual-band BPF.

$$C_{ssk} = \alpha / L_{s1k} \tag{B.12}$$

$$C_{s1k} = 1/\left(L_{s1k}\omega_{r1}^2\right) \tag{B.13}$$

$$L_{s2k} = \frac{1}{C_{ssk}}\left(\frac{1}{\omega_{x2}^2} - \frac{1}{\omega_{r2}^2}\right) \tag{B.14}$$

$$C_{s2k} = 1/\left(L_{s2k}\omega_{r2}^2\right) \tag{B.15}$$

where $A_{nn}=\{\omega_{r2}(\omega_{x2}/\omega_{nn}-\omega_{nn}/\omega_{x2})\}/\{\omega_{nn}\omega_{x2}(\omega_{r2}/\omega_{nn}-\omega_{nn}/\omega_{r2})\}$ and $B_{nn}=\omega_{r1}/(\omega_{r1}/\omega_{nn}-\omega_{nn}/\omega_{r1})$ with n=1 or 2, $\omega_{x2}=1/\sqrt{L_{s2k}(C_{ssk}+C_{s2k})}$ and $L_{s1k}C_{ssk}=\alpha=(A_{11}+A_{12})/(B_{11}+B_{12})=(A_{21}+A_{22})/(B_{21}+B_{22})=(A_{11}-A_{21})/(B_{11}-B_{21})=(A_{12}-A_{22})/(B_{12}-B_{22})$. The susceptance relations and the inductors, capacitors for the shunt resonator in Fig. B.4 (b) can also be derived in a similar fashion.

$$C_{p1k} = \frac{g_k}{B_{12} - \left(A_{12}/\beta\right)} \tag{B.16}$$

$$L_{ppk} = \beta / C_{p1k} \tag{B.17}$$

$$L_{p1k} = 1/\left(C_{p1k}\omega_{r1}^2\right) \tag{B.18}$$

$$C_{p2k} = \frac{1}{L_{ppk}}\left(\frac{1}{\omega_{x2}^2} - \frac{1}{\omega_{r2}^2}\right) \tag{B.19}$$

$$L_{p2k} = 1/\left(C_{p2k}\omega_{r2}^2\right) \tag{B.20}$$

B.2 Simulation and Measurement

To verify the proposed technique and design concept, and the derived formulae in the previous section, a dual-band BPF is designed with the following specifications:

- Input/output impedance: 50 Ω
- Number of resonators: 5
- Filter response: Tchebyscheff
- Passband ripple: 0.05 dB
- Dual bandwidth: 70–155 MHz and 255–340 MHz
- f_{r1} and f_{r2}: 200 and 400 MHz

Fig. B.5 shows the schematic of the new dual-band BPF which contains three series and two shunt resonators, and Fig. B.6 shows its simulated results. The dual-band BPF is fabricated with surface-mount (SM) capacitors and coil-inductors on a PCB board. The measured insertion loss and return loss are shown in Fig. B.7. The insertion loss and return loss at 110 and 300 MHz are 0.36 and 21.8 dB and 1.34 and 14.6 dB, respectively. More insertion loss occurs in the second pass-band due to more lossy elements (SM-capacitor and coil-inductor) at a higher frequency. The rejection performance at 200 and 400 MHz

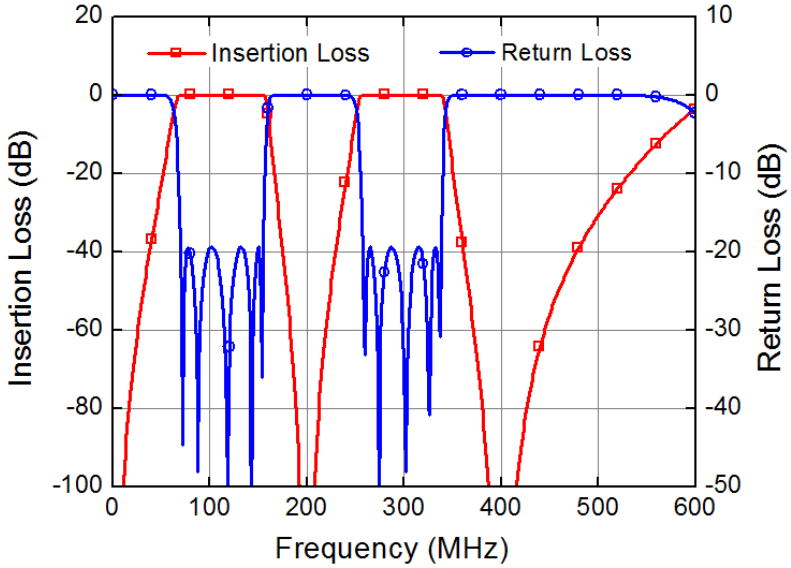


Fig. B.6. Simulated insertion loss and return loss of the proposed dual-band BPF.

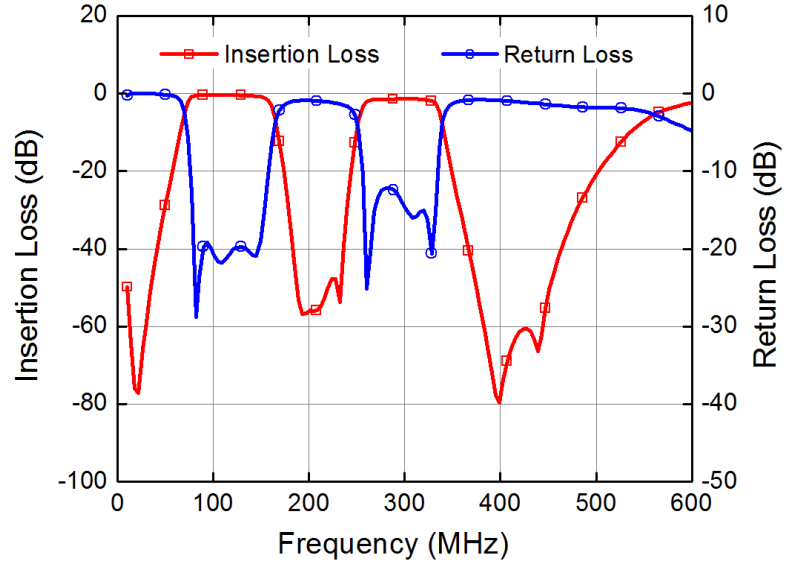


Fig. B.7. Measured insertion loss and return loss of the proposed dual-band BPF.

are 58 and 79 dB, respectively. As can be seen, good symmetrical skirt selectivity between the low- and high-frequency stop-bands is achieved. Also, the simulated and measured results agree well.

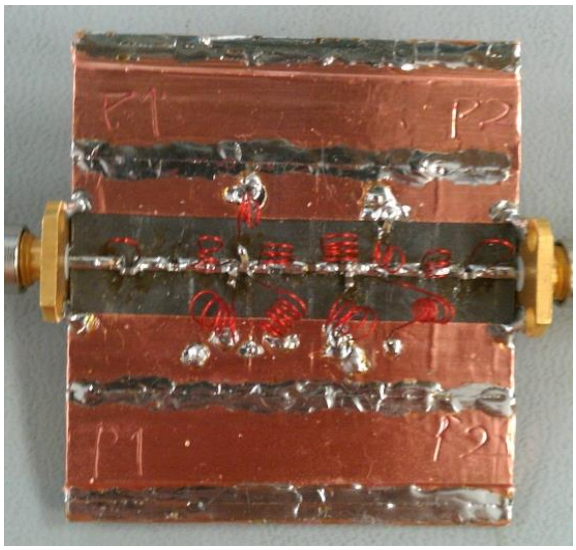


Fig. B.8. Photograph of the proposed dual-band BPF.

B.3 Conclusion

This paper presents a new technique for improved stop-band response in dual-band BPFs and a new dual-band BPF with enhanced skirt characteristics at the high-frequency stop-band that produce well symmetry between the stop-bands of the first and second bands. The idea has been verified through simulations and measurements. The derived formulae enable simple and accurate design for the proposed dual-band BPF. Moreover, these formulas also help adjust the second rejection frequency, f_{r2}, as desired without using any extra tuning procedure. The proposed technique has an advantage over the conventional design method in that it maintains the improved skirt characteristic with the fixed suppression point f_{r2} even if the bandwidth of the pass-band is extended. This unique property makes the proposed design technique attractive for multi-band broadband wireless communication and sensing designs.

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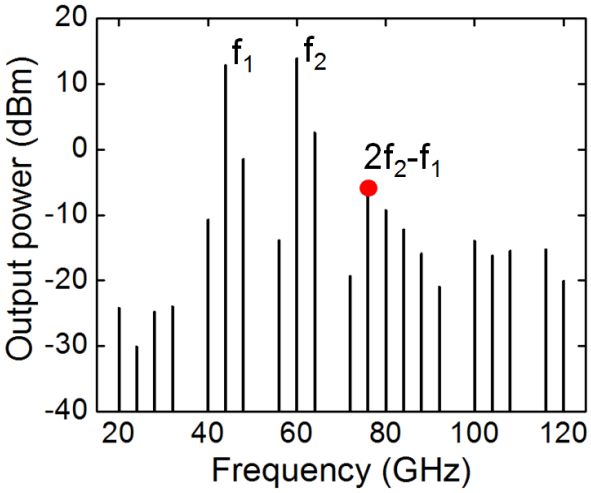
APPENDIX C

44/60-GHZ CONCURRENT DUAL-BAND 0.18-μm BICMOS POWER AMPLIFIER

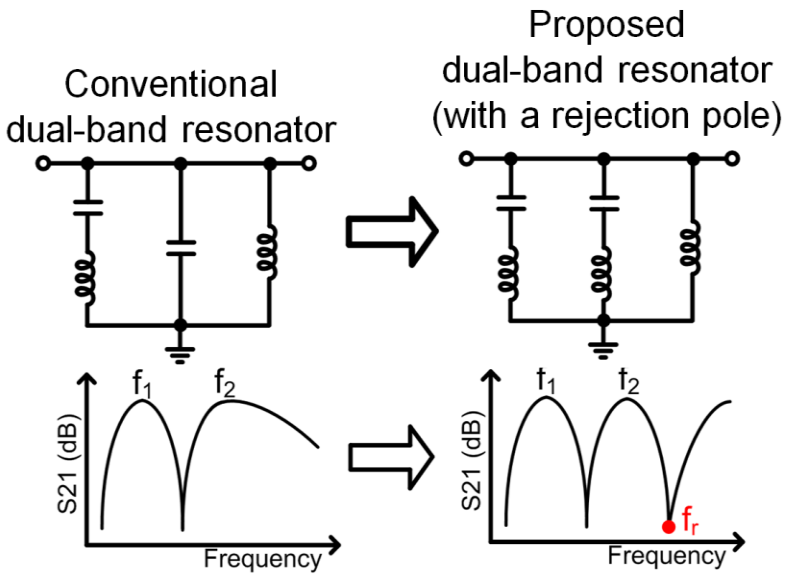
In this chapter, we report a concurrent dual-band power amplifier (PA) centered at 44 and 60 GHz designed on a 0.18-μm BiCMOS process. A shunt resonator having a dual-passband at 44 and 60 GHz and a single stop band at 76 GHz is employed in the PA design so that its input impedance is matched in the dual bands and the significant third-order intermodulation (IM3) product is filtered out in the stop band. Some part of this chapter, contents/figures, are previously published in [C-1].

C.1 Circuit Design

A concurrent dual-band PA has more IM products and harmonics as compared to its single-band counterparts due to the dual main tones injected as shown in Fig. C.1(a). Especially, in the 44/60GHz frequency plan, the main tones at 44 (f_1) and 60 GHz (f_2) lead to the significant IM3 product at 76 GHz ($2f_2$-f_1), which is only 23.5 % away from the 2nd main tone with relatively high power. It is desired to filter out the IM3 product for improving the reliability of the PA and its associated system. To that end, the dual-band resonator having a rejection pole shown in Fig. C.1(b) is proposed and utilized in the PA design as shown in Fig. C.2 for filtering out the IM3 product. The PA has 3 stages and the proposed resonators are placed in the input and output matching networks. On the other



(a)



(b)

Fig. C.1. (a) IM products and harmonics caused by the dual main tones at f_1 and f_2 in the concurrent dual-band PA. (b) Conventinoal dual-passband and proposed dual-passband and single-stopband resonators.

hand, the conventional resonator in Fig. C.1(b) is not suitable for the IM3 filtering due to the poor rejection performance in the higher frequency stop band.

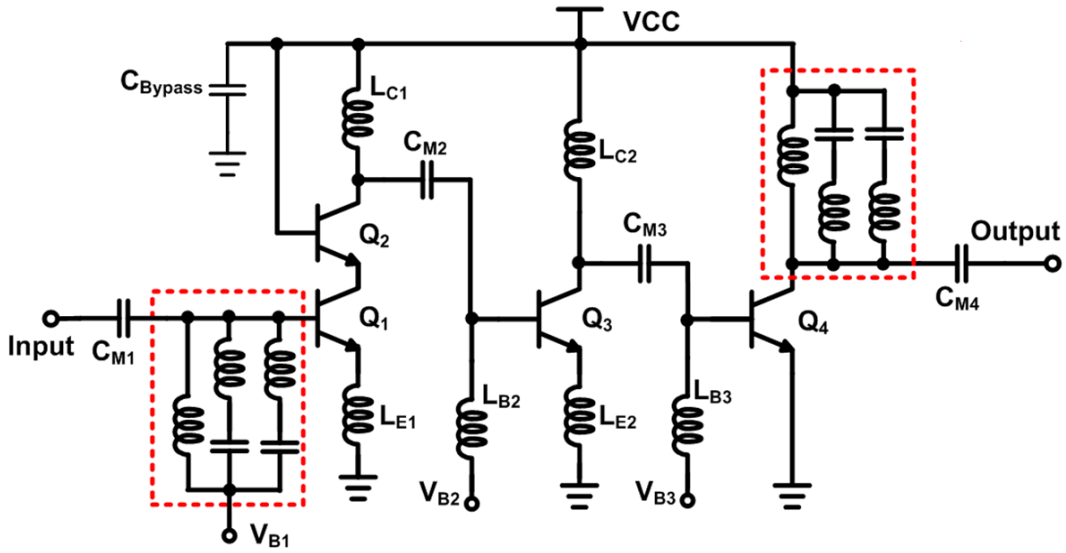


Fig. C.2. 3-stage concurrent dual-band PA with the proposed dual-band resonators.

C.2 Performance

The 44/60 GHz concurrent dual-band PA is designed with TowerJazz 0.18-μm BiCMOS technology [C-2] based on the circuit topology shown in Fig. C.2. Fig. C.3(a) shows the simulated gain (S21) and input (S11) and output (S22) return losses. The gain response shows the dual pass bands centered at 44 and 60 GHz and the stop band at the IM3 frequency of 76 GHz. For the PAE and OP1dB simulations shown in Figs. C.3(b) and (c), two injection modes (single-tone and dual-tone modes) are employed. For the single-tone mode, only one main tone such as 44- or 60-GHz tone is injected into the PA while the two main tones are simultaneously injected in the dual-tone mode simulation. Table C.1 compares the simulations for the dual-tone mode to those for the single-tone modes. As expected, from the more IM products and harmonics incurred, the dual-tone

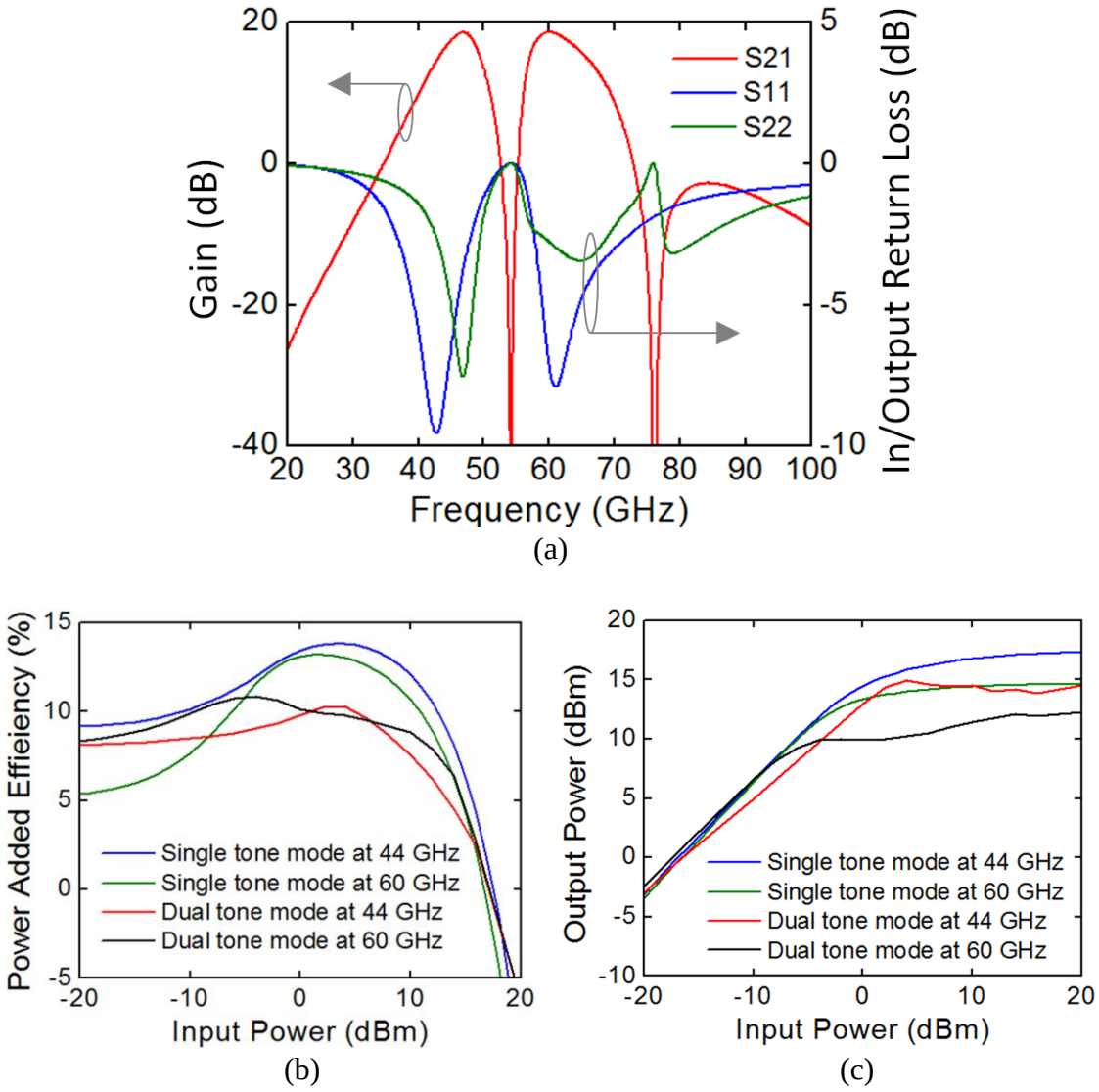


Fig. C.3. Simulations of the concurrent dual-band PA: (a) Gain, and input/output return loss, (b) power added efficiency, and (c) output P1dB for the single- and dual-tone modes.

mode simulation leads to lower OP1dB and PAE at each center frequency, which are more accurate than the results obtained in the conventional single-tone modes.

Table C.1 Simulations of the concurrent dual-band PA with single-tone and dual-tone modes

Mode / Performance	Single-tone mode		Dual-tone mode	
Freq. (GHz)	44	60	44	60
Gain (dB)	18.5	18.1	18.5	18.1
Input Return Loss (dB)	8.4	7.1	8.4	7.1
Output Return Loss (dB)	3.6	2.8	3.6	2.8
3-dB Bandwidth (GHz)	5.8	7.7	5.8	7.7
OP1dB (dBm)	11	11.6	4.5	8
PAE (%)	13.8	13	10.3	10.7

C.3 Conclusion

A 0.18-μm SiGe BiCMOS 44/60 GHz concurrent dual-band PA with a dual-band resonator having an IM3 rejection response is designed. The results show that the PA's input impedances are well matched in the dual pass bands and the IM3 products are sufficiently filtered out in the stop band. The dual main tones employed for the PAE and OP1dB simulations show more accurate results than those using the conventional single-tone modes, demonstrating that the dual- or multi-tone mode simulation and measurement are necessary for the multi-band circuit and system design for more accurate

characterization. The proposed technique of filtering out the undesired IM products or harmonics is attractive for the design of multi-band circuits and systems.

C.4 References

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APPENDIX D

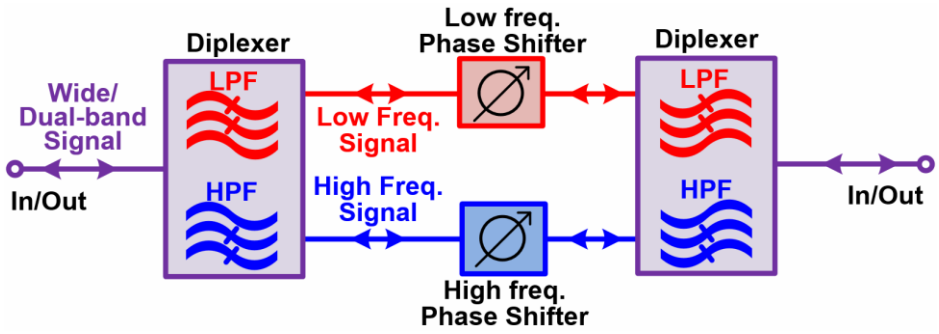
44/60 GHZ DUAL-BAND 0.18-µm CMOS PHASE SHIFTER

Multi-band wireless communication and radar systems have become attractive in addressing increasing demands of applications. Specifically, multi-band phased-array systems are important. Various phase shifters working in single bands have been developed, e.g. [D-1]-[D-2].

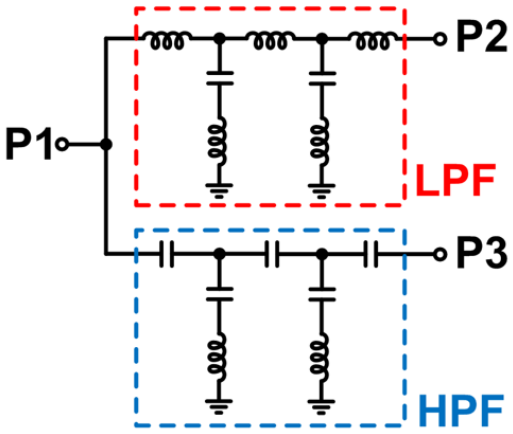
In this chapter, a 4-bit dual-band phase shifter, having the pass-bands of 40–46 GHz and 54–66 GHz and consisting of diplexers and single-band phase shifters, is designed using a 0.18-µm BiCMOS/CMOS technology. Due to the adjacent pass bands with only 15% spacing from 46 to 54 GHz, high-isolation diplexers are employed for the dual-band phase shifter design. Consequently, the dual-band phase shifter can be controlled in each frequency band individually without significant effects between the bands. Some part of this chapter, contents/figures, are previously published in [D-3].

D.1 Circuit Design

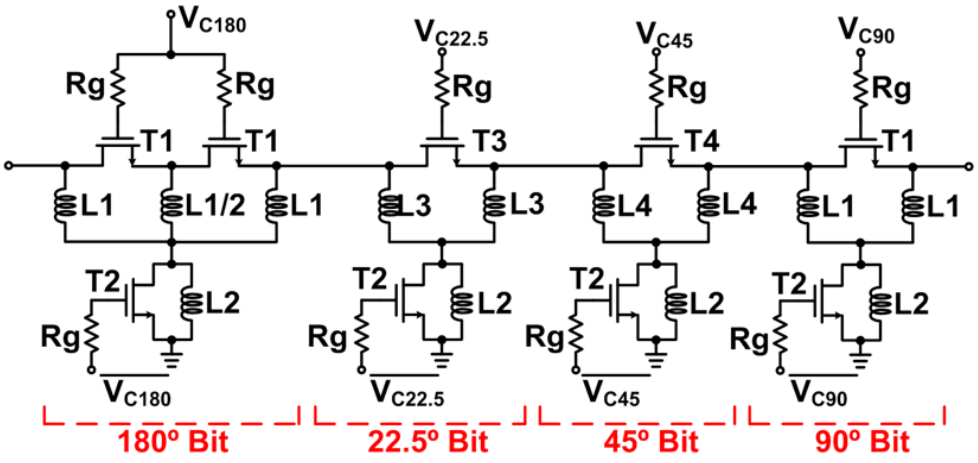
Fig. D.1(a) shows the block diagram of the proposed bidirectional dual-band phase shifter consisting of two diplexers and single-band phase shifters. It operates as follows. A wide- or dual-band signal injected through the input of the first diplexer splits into the low-frequency and high-frequency signal paths; the phase delays of these separate signals are then controlled by the low- and high-frequency single-band phase shifters, respectively; and then finally the signals are combined by the second diplexer yielding a dual-band



(a)



(b)



(c)

Fig. D.1. (a) Block diagram of the dual-band phase shifter, (b) its constituent diplexer consisting of high-pass and low-pass filters, and (c) 4-bit sigle-band phase shifer.

phase-controlled output signal. In order to be able to control the phase in the low- and high-frequency paths independently, high-isolation diplexers are necessary for the dual-band phase shifter – otherwise, the phase control on one path would inadvertently affect the phase on the other path, hence rendering the dual-band functionality ineffective. To that end, as shown in Fig. D.1(b), the constituent diplexer is designed with Elliptic low-pass and high-pass filters, which have rejection poles outside the pass bands. Fig. D.1(c) shows the topology of the constituent single-band phase shifters. The single-band phase shifters are designed base on the high-pass Pi-type phase delay network and the gate voltages are digitally controlled for 16 phase delay states.

D.2 Performance

A 4-bit CMOS dual-band phase shifter centered at 44 and 60 GHz is designed with TowerJazz 0.18-μm SiGe BiCMOS technology [D-4] based on the block diagram and circuit topologies in Fig. D.1. Its simulation results shown in Fig. D.2 are obtained by controlling the 44-GHz phase shifter on the low-frequency path over 16 states while the 60 GHz phase shifter on the high-frequency path is fixed to the first phase delay state. The zoomed-out insertion loss and phase in Figs. D.2(a) and (b) show that the phase delay in the 1st band (40 to 46 GHz) can be controlled independently without causing significant effects on the 2nd band (54 to 66 GHz). In Fig. D.2, the RMS amplitude error, RMS phase error and in/output return loss are less than 0.9 dB, 12^{o} and 7.6 dB across 40 to 46 GHz, respectively. Also, the insertion loss and input P1dB at 44 GHz over the 16 states are 4.2±1.3 dB and higher than 10.5 dBm, respectively. The constituent 4-bit 60-GHz phase

shifter of the dual-band phase shifter is controlled similarly and its simulations are shown in Fig. D.3. As shown in the zoomed-out insertion loss and phase in Figs. D.3(a) and (b), no significant effects occur in the 1st band during the 16-states phase shift in the 2nd band. In Fig. D.3, the RMS amplitude error, RMS phase error and in/output return loss are less than 1.2 dB, 7.2º and 7.7 dB across 54 to 66 GHz, respectively. Also, the insertion loss and input P1dB at 60 GHz over the 16 states are 5.4±1.8 dB and higher than 9.5 dBm, respectively. It is noted that the phases in the 1st and 2nd pass-bands are individually adjusted in the simulations shown in Figs. D.2 and 3, but the designed dual-band phase shifter basically enables to control the phases at the both pass-bands concurrently without any significant effect on the other band.

D.3 Conclusion

A 44/60 GHz dual-band phase shifter consisting of high-isolation diplexers and 4-bit single-band phase shifters is designed in a 0.18-μm BiCMOS/CMOS process. It is verified that the dual-band phase shifter works in the 44 or 60 GHz frequency band independently without any significant effect to each other, which is a crucial and desired characteristic in multi-band phase-control circuits and systems such as phased-array radar and communication systems.

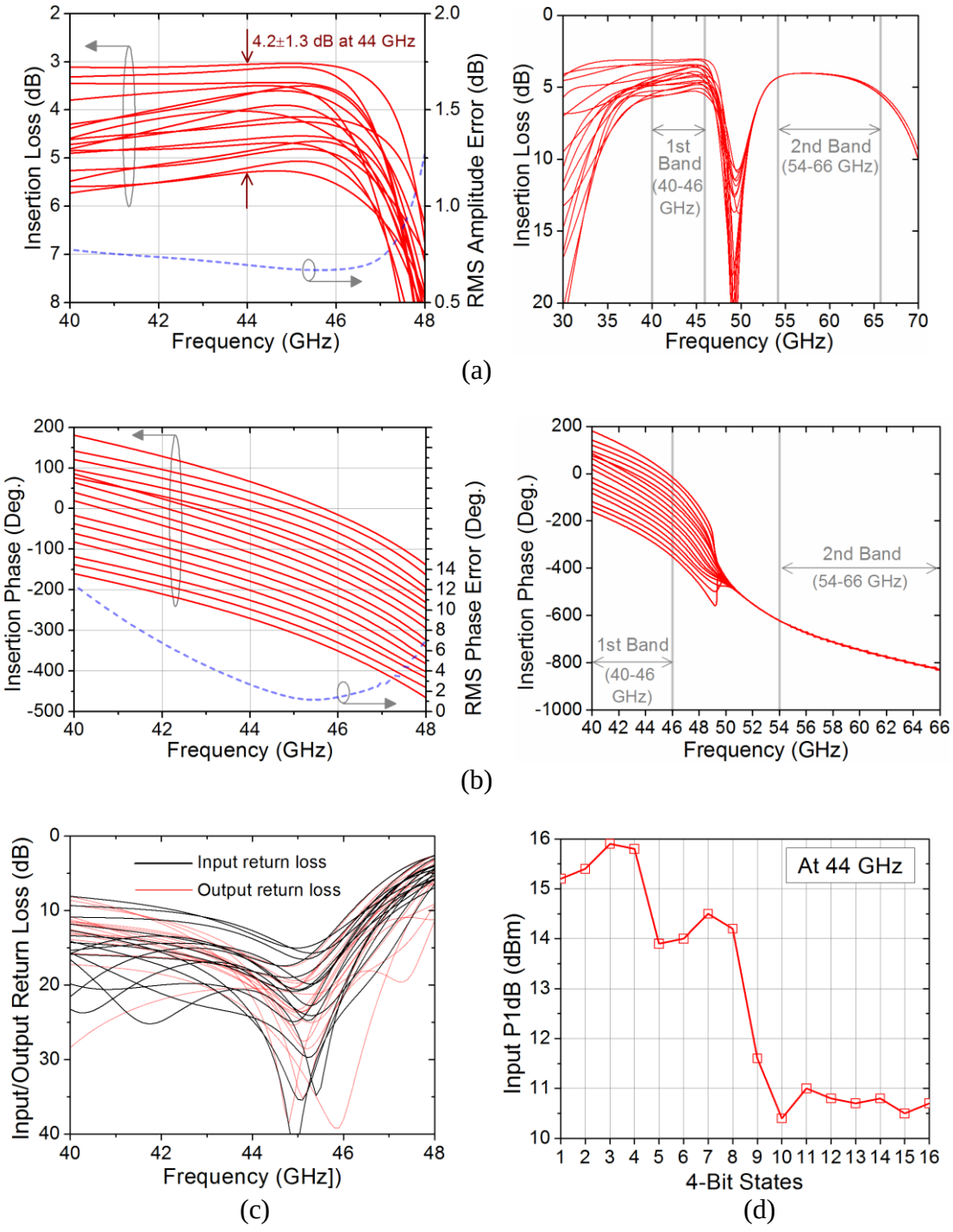


Fig. D.2. Simulations of the dual-band phase shifter over 16 states during the operation of the 44-GHz phase shifter: (a) insertion loss and RMS amplitude error zoomed in and out, (b) insertion phase and RMS phase error zoomed in and out, (c) input and output return loss, and (d) input P1dB.

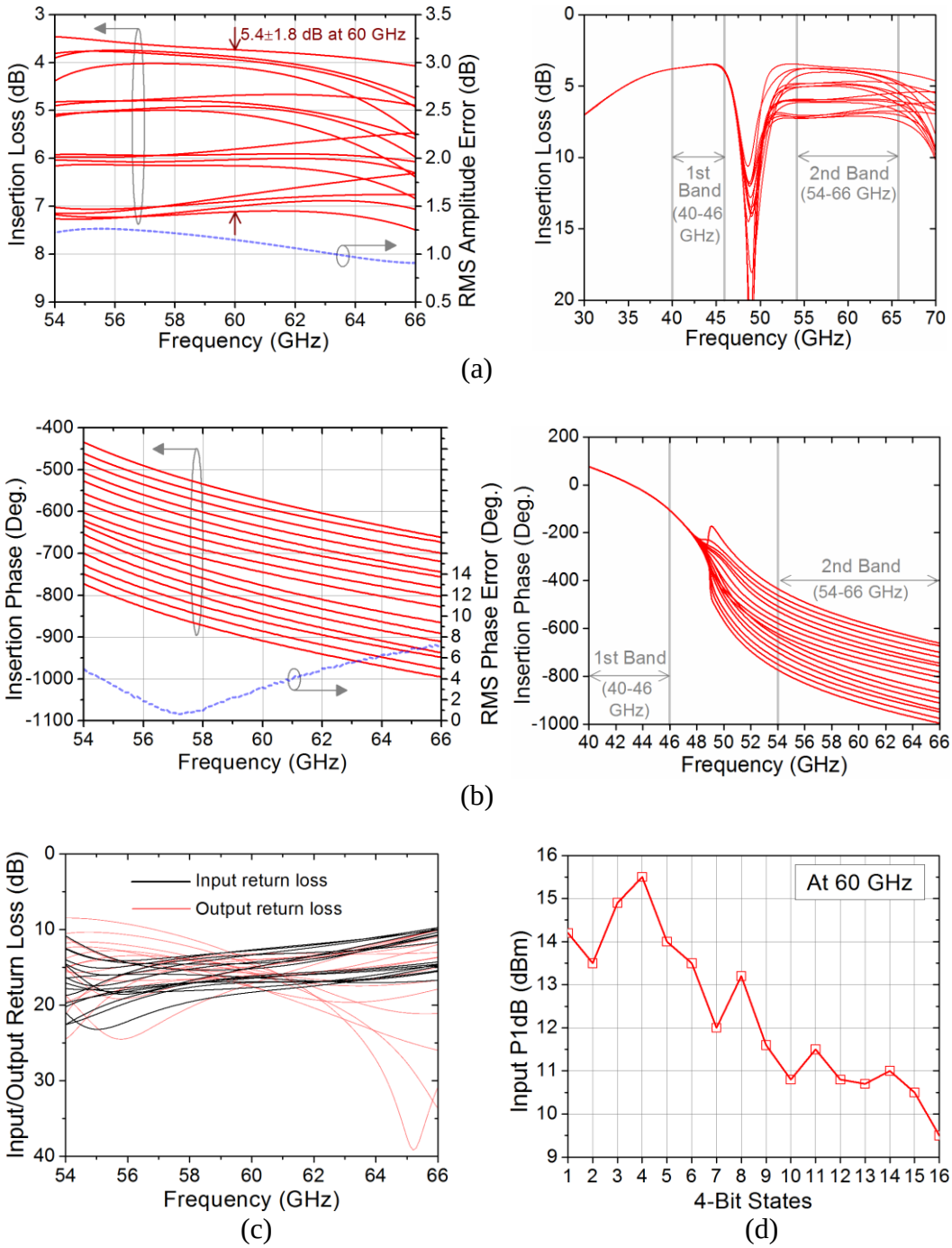


Fig. D.3. Simulations of the dual-band phase shifter over 16 states during the operation of the 60-GHz phase shifter: (a) insertion loss and RMS amplitude error zoomed in and out, (b) insertion phase and RMS phase error zoomed in and out, (c) input and output return loss, and (d) input P1dB.

D.4 References

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