

LOW-POWER SLEW-RATE BOOSTING BASED 12-BIT PIPELINE ADC
UTILIZING FORECASTING TECHNIQUE IN THE SUB-ADCS

A Dissertation

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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May 2019

Major Subject: Electrical Engineering

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ABSTRACT

The dissertation presents architecture and circuit solutions to improve the power efficiency of high-speed 12-bit pipelined ADCs in advanced CMOS technologies. First, the 4.5bit algorithmic pipelined front-end stage is proposed. It is shown that the algorithmic pipelined ADC requires a simpler sub-ADC and shows lower sensitivity to the Multiplying DAC (MDAC) errors and smaller area and power dissipation in comparison to the conventional multi-bit per stage pipelined ADC. Also, it is shown that the algorithmic pipelined architecture is more tolerant to capacitive mismatch for the same input-referred thermal noise than the conventional multi-bit per stage architecture. To take full advantage of these properties, a modified residue curve for the pipelined ADC is proposed. This concept introduces better linearity compared with the conventional residue curve of the pipelined ADC; this approach is particularly attractive for the digitization of signals with large peak to average ratio such as OFDM coded signals.

Moreover, the minimum total required transconductance for the different architectures of the 12-bit pipelined ADC are computed. This helps the pipelined ADC designers to find the most power-efficient architecture between different topologies based on the same input-referred thermal noise. By employing this calculation, the most power efficient architecture for realizing the 12-bit pipelined ADC is selected.

Then, a technique for slew-rate (SR) boosting in switched-capacitor circuits is proposed in the order to be utilized in the proposed 12-bit pipelined ADC. This technique makes use of a class-B auxiliary amplifier that generates a compensating current only

when high slew-rate is demanded by large input signal. The proposed architecture employs simple circuitry to detect the need of injecting current at the output load by implementing a Pre-Amp followed by a class-B amplifier, embedded with a pre-defined hysteresis, in parallel with the main amplifier to boost its slew phase. The proposed solution requires small static power since it does not need high dc-current at the output stage of the main amplifier. The proposed technique is suitable for high-speed low-power multi-bit/stage pipelined ADC applications. Both transistor-level simulations and experimental results in TSMC 40nm technology reduces the slew-time for more than 45% and shorts the 1% settling time by 28% when used in a 4.5bit/stage pipelined ADC; power consumption increases by 20%.

In addition, the technique of inactivating and disconnecting of the sub-ADC's comparators by forecasting the sign of the sampled input voltage is proposed in the order to reduce the dynamic power consumption of the sub-ADCs in the proposed 12-bit pipelined ADC. This technique reduces the total dynamic power consumption more than 46%. The implemented 12-bit pipelined ADC achieves an SNDR/SFDR of 65.9/82.3 dB at low input frequencies and a 64.1/75.5 dB near Nyquist frequency while running at 500 MS/s. The pipelined ADC prototype occupies an active area of 0.9 mm² and consumes 18.16 mW from a 1.1 V supply, resulting in a figure of merit (FOM) of 22.4 and a 27.7 fJ/conversion-step at low-frequency and Nyquist frequency, respectively.

DEDICATION

To my parents and Sima

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere appreciation to my advisor, Dr. Jose Silva-Martinez. Without his supports, my research and dissertation will not be possible. During my research and study, he is always patient and supportive when I have problems. I have learnt from him, not just limited to technical aspect, but also from his personality. He is an extremely nice person and also a wonderful friend.

I would like to thank Dr. Kamran Entesari, Dr. Peng Li, and Dr. Jay Porter for their critical comments on my research. I would also like to thank Eric G. Soenen and Martin Kinyua for fruitful discussions on my projects. I would like to thank Dongwon Seo and Shahin Mehdizad Taleie for mentoring me during my intern experience at Qualcomm.

I would like to thank Alexander Edward, Carlos Briseno-Vidrios, Negar Rashidi, Qiyuan Liu, Chulhyun Park, Suraj Prakash, and Venkatraman Natarajan as supportive teammates and great friends collaborating on research projects.

I would like to express deep appreciation to my family, particularly my parents and brother, thank you for your love, support, and unwavering belief in me. Without you, I would not be the person I am today.

Above all, I would like to thank my wife Sima for her love and constant support, for all the late nights and early mornings, and for keeping me sane over the past years. Thank you for being my muse, editor, proofreader, and sounding board. But most of all, thank you for being my best friend. I owe you everything.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a dissertation committee consisting of Professors Jose Silva-Martinez, Kamran Entesari, and Peng Li of the Department of Electrical and Computer Engineering and Professor Jay Porter of the Department of Engineering Technology and Industrial Distribution.

The work for the Section II, III, IV, and V of the dissertation was completed by the student, in collaboration with Suraj Prakash, and Chulhyun Park under the advisement of Dr. Jose Silva-Martinez of the Department of Electrical and Computer Engineering together with Dr. Martin Kinyua and Dr. Eric G. Soenen from TSMC Technology, Inc.

The rest part of the dissertation was completed by the student, under the advisement of Dr. Jose Silva-Martinez of the Department of Electrical and Computer Engineering.

Funding Sources

Graduate study was supported by Texas Instrument Excellence Fellowship, Broadcom Corporation Fellowship, and National Science Foundation.

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1. INTRODUCTION

1.1. Motivation

The wireless communication industry has experienced exceptional growth in the past decade, which has resulted in handheld devices with multi-purpose functionality. Fig. 1.1 shows the number of worldwide smartphone users in the seven consecutive years which is growing rapidly. The low-cost, low-power digital computing required by these systems is facilitated by process scaling and it is expected to continue. It is anticipated that the main issues in these systems will be the co-existence of multiple services; excessive power consumption is especially critical for mobile devices. High-performance audio and video standards demand over 11 effective number of bits (ENOB), while signal bandwidth varies by more than an order of magnitude. The challenge is to develop ADC architectures that can be efficiently reconfigured for multiple applications while maintaining performance and power consumption comparable to the optimal standalone solution for each standard. ADC power optimization is one of the key areas of current areas of research.

Pipelined analog-to-digital converters (ADCs) have been utilized to achieve high-speed high-resolution in Nyquist-rate data converters. Pipelined ADCs with sampling rates in the range of several hundreds of MS/s are widely used in broadband communication receivers, radar systems, digital wireless, and wired communication systems, including fifth-generation mobile networks (5G) and data-over-cable service interface specifications (DOCSIS) [1]–[13]. As it is shown in the Fig. 1.2, although

pipelined ADCs offer high sampling rates and high bandwidths, they usually demand high power consumption, which results in limited power efficiency [3], [7], [10], [14]. Conventionally, pipelined ADC is the most popular choice in the communication application and RF sampling due to its high-speed range capability and simple digital output bits. However, there is still high-power consumption issue demanding new techniques to handle.

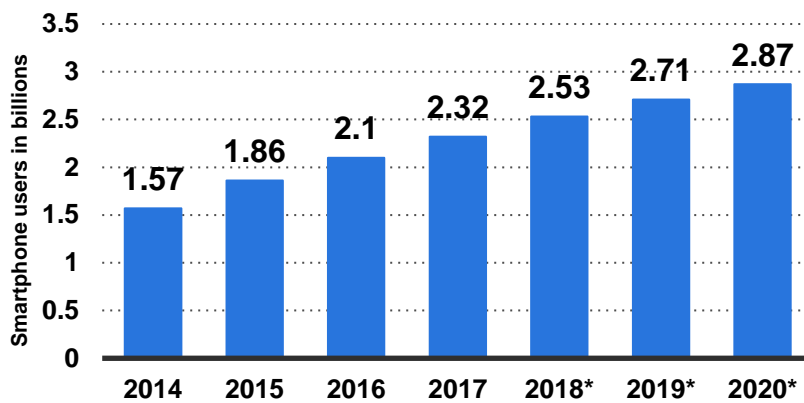


Fig. 1.1 Number of smartphone users worldwide from 2014 to 2020 (in billions).

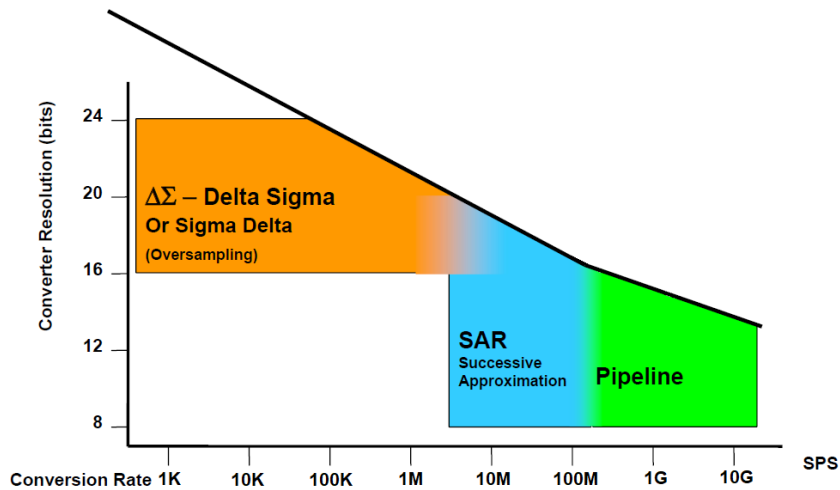


Fig. 1.2. Quantization noise ADC.

1.2. Research Contribution

The dissertation presents system and circuit solutions to improve the power efficiency of high-speed 12-bit pipelined ADCs in advanced CMOS technologies.

In this dissertation, the minimum total required transconductance for the different architectures of the pipeline ADC are computed. These calculations are performed for different capacitive scaling ratios between consecutive pipeline stages and considering the minimum unit capacitance in pipeline stage to avoid mismatch. This study helps the pipeline ADC designers to find the most power-efficient architecture between different topologies for the same input-referred thermal noise. In this dissertation, it is shown that a proposed algorithmic pipeline ADC is very competitive and requires a simpler sub-ADC and shows lower sensitivity to the Multiplying DAC (MDAC) errors as well as smaller area and power dissipation in comparison to the conventional multi-bit per stage pipeline ADC. Also, the algorithmic pipeline architecture is more tolerant to capacitive mismatch for the same input-referred thermal noise than multi-bit per stage architectures. To take full advantage of these properties, a modified residue curve for the pipeline ADC is proposed. This approach is particularly attractive for the digitization of signals with large peak to average ratio such as OFDM coded signals.

For high-performance switched-capacitor circuits like multi-bit/stage pipelined ADC, this dissertation presents a technique for slew rate (SR) boosting. The proposed technique makes use of a class-B auxiliary amplifier that generates a compensating current only when high slew-rate is demanded by large signals. The proposed architecture employs simple circuitry to detect the need for a large output current by employing a highly

sensitive pre-amplifier followed by a class-B amplifier. The functionality of the class-B transconductance amplifier is dictated by a predefined hysteresis, and operates in parallel with the main amplifier. The proposed solution demands small static power (under 20% of main amplifier power) due to its class-B nature. The experimental results in a 40 nm CMOS technology show more than 45% reduction in slew time, and a 28% shorter slew time for 1% settling time when used in a typical 4.5 bit/stage block commonly used in pipelined ADCs. Compared with the core amplifier, its third harmonic distortion (HD3) at 500 MHz reduces by more than 10 dB when the slew-rate boosting circuit is activated.

In addition, this dissertation presents a forecasting technique in the sub-ADC, which reduces the number of active comparators during the sub-ADC's conversion phase. The sign of the incoming signal is detected, and then the number of active comparators in each conversion cycle reduces by half, which leads to a more than 46% dynamic power savings from the sub-ADCs. The 12-bit 500 MS/s pipelined ADC fabricated in the 40 nm TSMC technology utilizing the proposed concepts achieves an SNDR/SFDR of 65.9/82.3 dB at low input frequencies and a 64.1/75.5 dB near Nyquist frequency while running at 500 MS/s. The pipelined ADC prototype occupies an active area of 0.9 mm² and consumes 18.16 mW from a 1.1 V supply, resulting in a figure of merit (FOM) of 22.4 and a 27.7 fJ/conversion-step at low-frequency and Nyquist frequency, respectively.

1.3. Dissertation Organization

The dissertation is organized as follows: Chapter 2 presents 4.5-bit algorithmic-pipelined ADC with a modified residue curve for better linearity topology. Chapter 3

discusses minimum total required transconductance for the different architectures for 12-bit pipelined ADC. Chapter 4 introduces the proposed operational transconductance amplifier with class-B slew-rate boosting topology for fast high-performance switched-capacitor circuits. Chapter 5 presents a 27.7 fJ/conv-step at Nyquist 500 MS/s 12-Bit pipelined ADC with slew boosted amplifiers and sub-ADC forecasting. Chapter 6 concludes the dissertation and proposes recommendations for future works.

2. 4.5-BIT ALGORITHMIC-PIPELINED ADC WITH A MODIFIED RESIDUE CURVE*

2.1. Introduction

A common practice to save power in ADC is to extend its input signal swing to relax the noise level specifications at the expense of a more demanding linearity constraint [15]-[19]. Also, this strategy is not feasible in the low supply voltage systems where the preceding stage cannot provide such a highly linear and large input signal swing to the ADC [20]-[23]. Another method for saving power is utilizing conventional multi-bit quantizer used in each stage of the pipelined ADC. But this technique shows limited linearity due to the multiple input signal segmentations. Thus, an extra calibration circuit must be employed in order to correct the static errors [24]-[27]. As a result, it would reduce the Figure of Merit (FOM) of the total pipelined ADC when the power dissipation of the calibration scheme would be taken into account.

In this section, we propose using a 4.5bit algorithmic front-end stage with a $V_{ref}/3$ residue curve that makes the architecture less sensitive to MDAC errors while achieving an unmatched power-linearity-resolution trade-off. By comparing the 4.5-bit algorithmic pipelined front-end stage to the conventional multi-bit front-end stage pipelined ADC, it would be shown that the algorithmic-pipelined front-end stage is one the competitive stage

* Reprinted with permission from “Algorithmic-pipelined ADC with a modified residue curve for better linearity” by M. H. Naderi and J. Silva-Martinez, 2017. 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1446-1449, Copyright 2017 by IEEE.

when the power consumption of the Sub-ADC is evaluated. The proposed 4.5-bit algorithmic stage needs dramatically smaller number of comparators, simpler DAC, and better linearity than the conventional 4.5-bit front-end pipelined stage. Also, the proposed novel residue curve that achieves better linearity in the pipelined stage is proposed in this section. It would be shown that the proposed residue curve shows 5 dB better linearity in comparison to the conventional residue curve.

2.2. Proposed 4.5-Bit Algorithmic Pipelined Front-End Stage

A conventional 4.5-bit front-end stage is shown in the Fig. 2.1. A design issue in the conventional 4.5-bit front-end stage is the sensitivity to 5-bit MDAC errors that result in limited linearity. The more bits are allocated in the first stage the smaller the voltage difference among segments is and the larger the effects of the MDAC errors are even for signals with small power. Thus, a complex calibration scheme is demanded in order to correct for those errors. The idea of an algorithmic 4.5-bit front-end is shown in the Fig. 2.2. The comparators are permanently connected to one of the plates of C1 and through a high-swing switch the circuit samples the input signal during phase ϕ_{s1} . C2 samples the input signal during the first clock phase, while the amplifier's input and output are short circuited to the common mode voltage. During the first evaluation phase, C2 is connected to the MUX and then the stage residue is computed. The amplifier's output is sampled again during the following phase ϕ_1 , and the evaluation process is then repeated. The 4.5bit/stage operation is completed after 4 clock cycles. Only at the end of the last iteration, the OpAmp is loaded by the next stage to process the following bits.

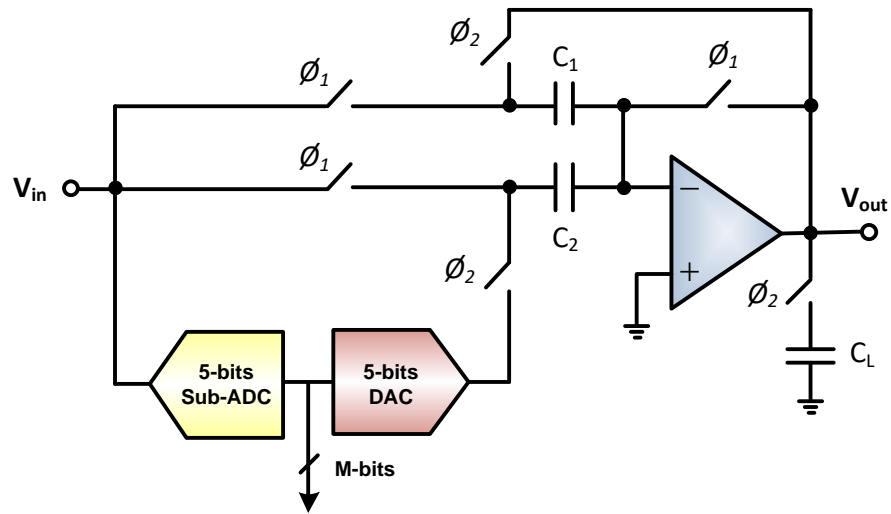


Fig. 2.1. The conventional 4.5bit pipelined front-end stage.

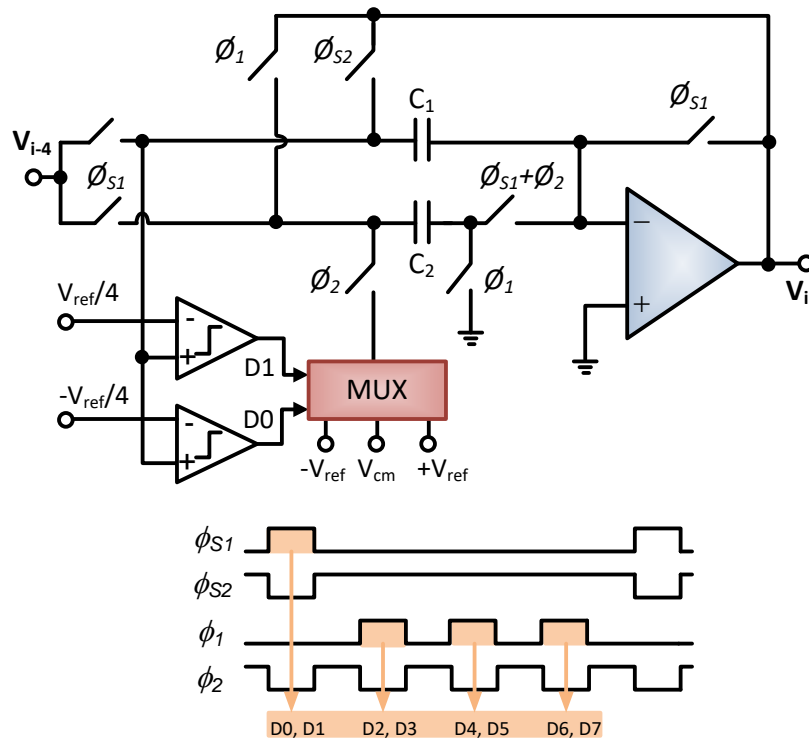


Fig. 2.2. Implementation of the proposed 4.5-bit algorithmic pipelined front-end stage.

This topology retains the segmentation properties of the 1.5-bit stage and then it shows lower sensitivity to MDAC errors such as capacitive and gain mismatches; the bits during the four iterations re-use the capacitors and same OpAmp. Although running four times faster than the conventional architectures, the amplifier is not loaded by the following stage when resolving first three most significant bits which relaxes the required transconductance of the residue amplifier. In addition, the feedback factor is maintained at $1/2$ instead of the factor $1/16$ required by the realization of a conventional 4.5bits/stage design. In a first approximation, reducing the evaluation time by 4 and reducing the feedback factor by 8 and relaxing the loading during 3 out of the 4 clock cycles result in a more power efficient solution.

Since the proposed topology needs only two capacitors compared to sixteen capacitors in the conventional 4.5-bit pipelined stage, less number of switch capacitor are needed, but notice that faster clocks are required. The proposed design needs only two bootstrap switches while the conventional design needs sixteen bootstrap switches for sampling the input signal at the first stage of the pipelined ADC. As a result, the proposed 4.5-bit algorithmic pipelined stage demands smaller area, simpler analog input layout routing, and less power but the clocks run four times faster.

Another remarkable difference is that only two comparators are needed compared to thirty comparators in the sub-ADC of the conventional 4.5-bit pipelined stage; again, the comparators in the algorithmic solution runs four time faster. As a result, much simpler MDAC with remarkable less number of gates are demanded.

2.3. Proposed Novel Residue Curve

Instead of using the conventional 1.5bit/stage block segmenting the residue curve at $\pm V_{\text{ref}}/4$, it is proposed to use $\pm V_{\text{ref}}/3$ as depicted in Fig. 2.3. The input range can be as large as $\pm V_{\text{ref}}$, while the output of the first stage and signal swing for the following stages is limited to $\pm 2V_{\text{ref}}/3$. Also, the signal swing when at the middle region of the residue curve can be as large as $\pm V_{\text{ref}}/3$ which is -9 dBFS while it corresponds to -12 dBFS for the conventional case. Since the main reason for non-linearity is due to gain and offset errors, it is expected to achieve better linearity figures when employing the proposed approach, especially when using coding schemes with large peak-to-average ratio (PAR) like the OFDM signals; e.g. PAR > 12 dB; most of time the signals will be processed without any segmentation when processing the MSBs. Only when signals are very large the other far left and far right segments are necessary for resolving the MSB.

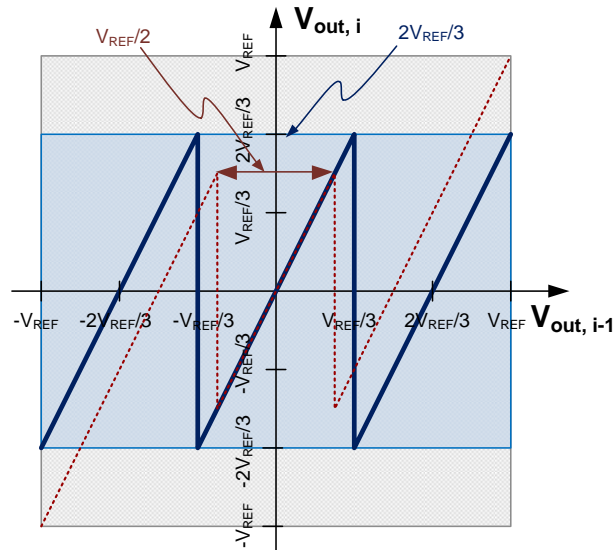


Fig. 2.3. Proposed residue curve for the 1.5 bit/stage architecture.

In the proposed scheme, most of the time the signal is within the middle range of the residue curve which make it insensitive to DAC errors for the most significant bit. Another remarkable advantage of the proposed scheme is that the signal swing in all remaining stages is within the range of $\pm 2V_{ref}/3$ as it is shown in the Fig. 2.4, which relaxes the output linear range of the amplifiers and switches. In addition, since IM3 and HD3 are proportional to the square of the input signal, then linearity for following stages will improve by 6 dB.

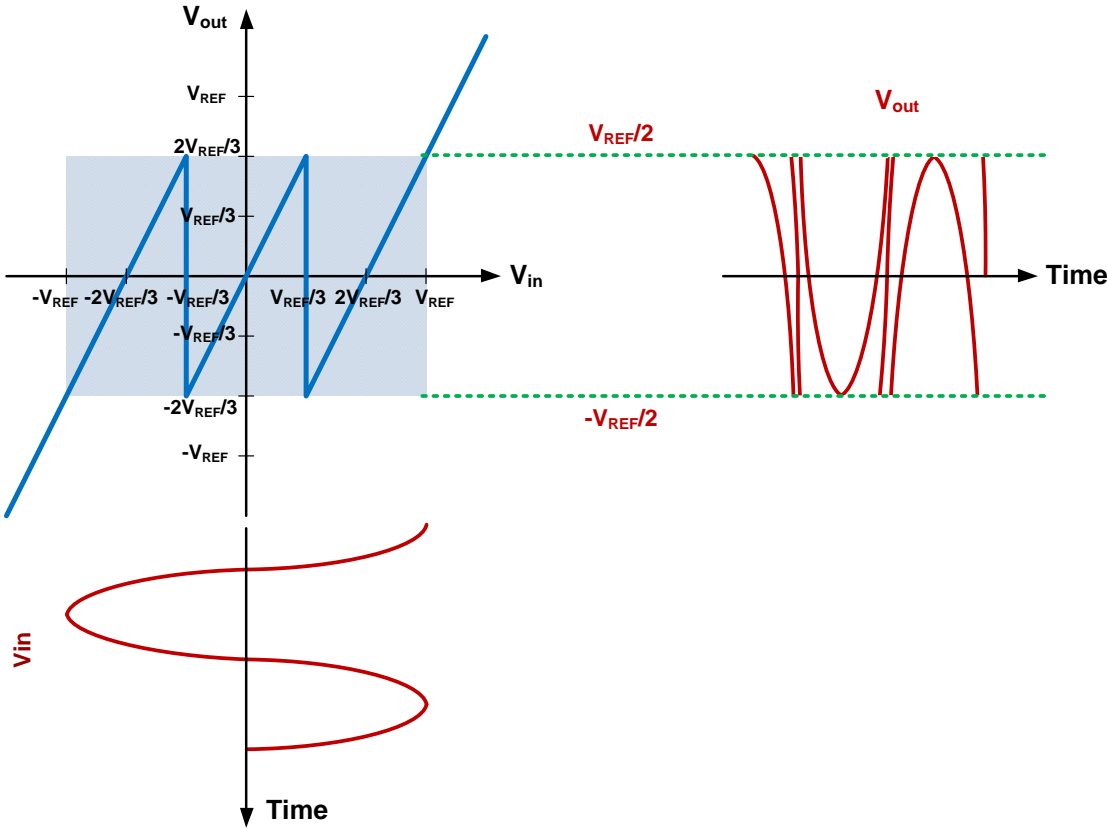


Fig. 2.4. The input and output ranges of the proposed residue curve for the 1.5 bit/stage architecture.

The realization of the 4.5-bit/stage algorithmic-pipelined ADC with a modified residue curve is presented in the Fig. 2.5. As it can be seen in this figure, the only required modification is scaling the reference voltages. In the proposed scheme, the reference voltages are set at $\pm V_{ref}/3$ for the sub-ADC and $\pm 4V_{ref}/3$ for the MDAC.

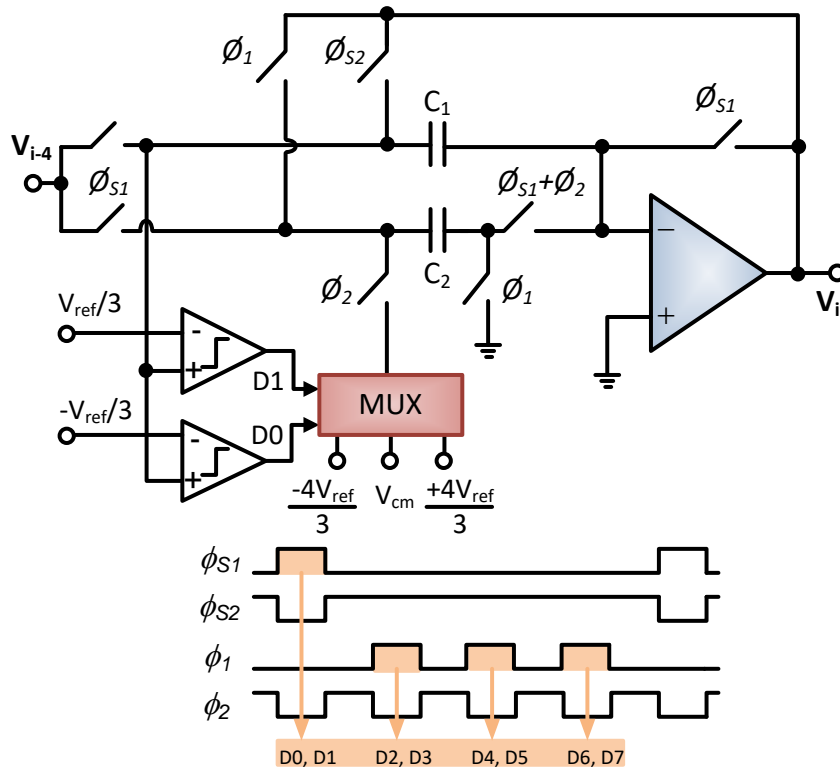


Fig. 2.5. Realization of 4.5-bit/Stage algorithmic-pipelined ADC with a modified residue curve.

2.4. Implementation and Simulation Results

To compare the performance of the 4.5-bit algorithmic pipelined stage versus the conventional 3.5-bit and 4.5-bit pipelined stages, we implemented three 100MS/s 12-bits

pipelined ADCs realized by cascading of 3.5-bit stages, 4.5-bit stages, and proposed 4.5-bit algorithmic stages in the TSMC 40 nm CMOS process using core devices with a nominal power supply voltage of 1.1 V. The residue amplifiers are designed based on the minimum total required G_m in each stage. A capacitor mismatch of 1% is considered for tracking immunity of the different architectures to MDAC errors. Then, a 1 V_{p-p} 9.6 MHz sinusoidal signal is applied at the input of all three ADCs to study the capacitor mismatch performance by running the Monte-Carlo simulation and measuring the mean values of the SNDR in each architecture.

Table 2.1 shows a comparison between the proposed 4.5-bit algorithmic stage and conventional 3.5-bit and 4.5-bit pipeline stages. As it can be seen in this Table, the algorithmic pipeline topology, compared with the conventional architectures, shows at least 7.5 dB better SNDR which demonstrate its properties such as lower sensitivity to MDAC errors.

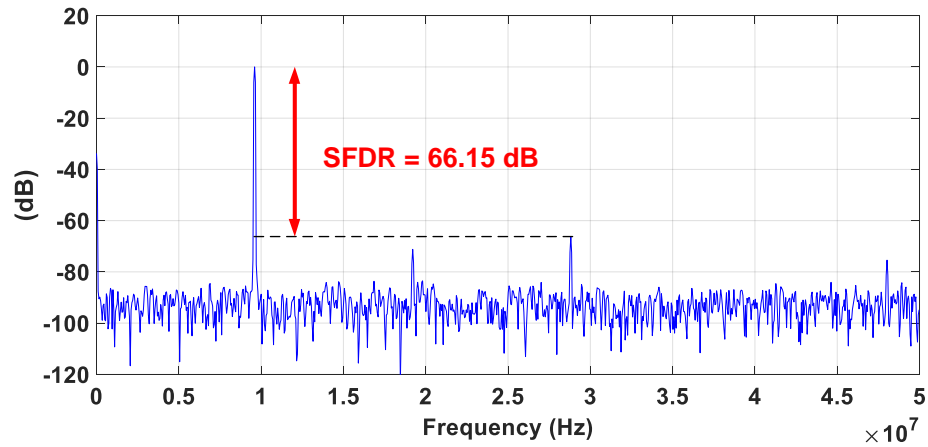
Table 2.1: Performance summary and comparison of different 12-bit pipelined ADCs under 1% capacitor mismatch

Architecture	Cascading of 3.5-bit Stages	Cascading of 4.5-bit Stages	Cascading of 4.5-bit Algorithmic Stages
SNDR	56.3 dB	53.1 dB	63.8 dB
Analog Power Consumption	5.5 mW	5.9 mW	6.3 mW
Digital Power Consumption	2.3 mW	4.8 mW	1.05 mW
Overall Power Consumption	7.8 mW	10.7 mW	7.35 mW
FOM (fJ/conv.step)	146.23	289.87	58.30

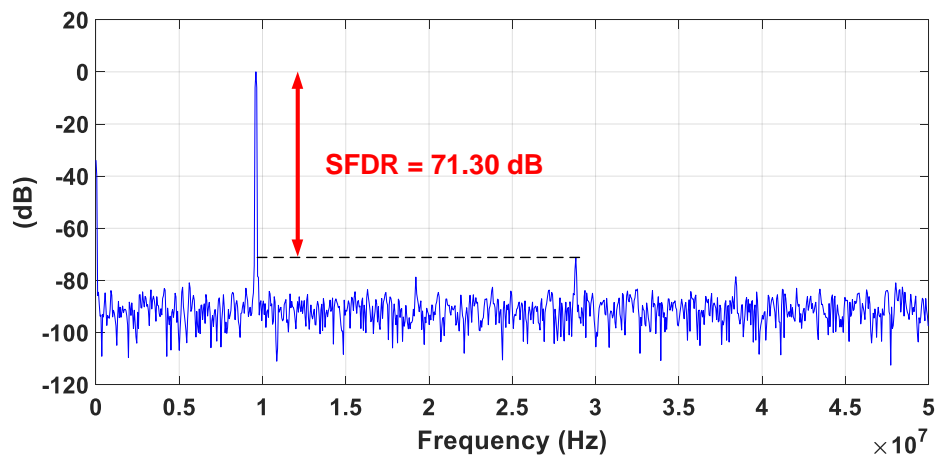
Table 2.1 shows that the algorithmic architecture demands 14% more analog power consumption from its residue amplifiers mainly due to the fact that it is running four times faster than the conventional solutions inside the pipeline stage. On the other hand, algorithmic architecture needs 54% and 78% less power dissipation from its sub-ADC and digital circuitry compared to the conventional 3.5-bit and 4.5-bit pipeline architectures, respectively. This superior advantage is mainly because of the fewer number of comparators with the less required accuracy and simpler MDAC in the algorithmic topology. Table 2.1 illustrates that the proposed 4.5-bit algorithmic architecture demands 5% and 31% less overall power consumption compared to 3.5-bit and 4.5-bit pipeline architectures for building a 100 MS/s 12-bit pipeline ADC while it presents better immunity to the capacitor mismatch.

The linearity performance of proposed 4.5-bit algorithmic pipeline stage with a novel residue curve is compared with the conventional residue curve in the Fig. 2.6. As it can be seen in this figure, the 4.5-bit algorithmic pipeline with $V_{ref}/3$ exhibits 5 dB better SFDR; better linearity, since the analog output voltage of the residue amplifiers is limited to 66% of the conventional output signal swing.

Although proposed algorithmic pipeline architecture offers better power consumption, linearity, and area, it would not be able to operate under very high sampling rate. Because of its cyclic architecture, its sampling frequency would be limited. For example, for 1 GS/s operation, the proposed algorithmic pipeline must operate at 5 GS/s which may be limited by the technology bandwidth.



(a)



(b)

Fig. 2.6. Frequency spectrum of 12-bit pipeline ADC by cascading 4.5-bit algorithmic pipeline stages with reference voltages: a) $\pm V_{\text{ref}}/4$, SFDR=66.15 dB b) $\pm V_{\text{ref}}/3$, SFDR=71.30 dB.

2.5. Conclusion

A new 4.5bit algorithmic front-end pipeline stage with a $V_{\text{ref}}/3$ residue curve is proposed in this section. It is shown that the algorithmic-pipeline topology presents very

competitive power efficiencies and low sensitivity to the MDAC errors while requires less area and less power dissipation in the sub-ADC. It is shown that cascading of the 4.5-bit algorithmic architecture offers most power efficiency for constructing a 12-bit pipeline ADC while it is more tolerant to the capacitive mismatch. A novel residue curve for the pipeline ADC is proposed that introduces better linearity specially for coding schemes with large peak-to-average ratio like the OFDM signals. The proposed 4.5-bit algorithmic-pipeline topology with a novel residue curve offers a power efficient alternative to conventional pipeline ADC architectures.

3. MINIMUM TOTAL REQUIRED TRANSCONDUCTANCE FOR THE DIFFERENT ARCHITECTURES FOR 12-BIT PIPELINED ADC*

3.1. Introduction

There are different available architectures for realizing a 12-bit pipelined ADC. As it is illustrated in the Fig. 3.1, a 12-bit pipelined ADC can be realized by series of 1.5-bit/stage, 2.5-bit/stage, 3.5-bit/stage, or 4.5-bit/stage pipelined stages. Moreover, a 12-bit pipelined ADC can be realized by mixing of these $M+0.5$ -bit/stages like 4.5-bit as the first stage and 3.5-bit as the second stage and etc. In this section, we propose the calculation of minimum total required transconductance for the different architectures of 12-bit pipelined ADC and the most power-efficient 12-bit pipelined architecture would be found.

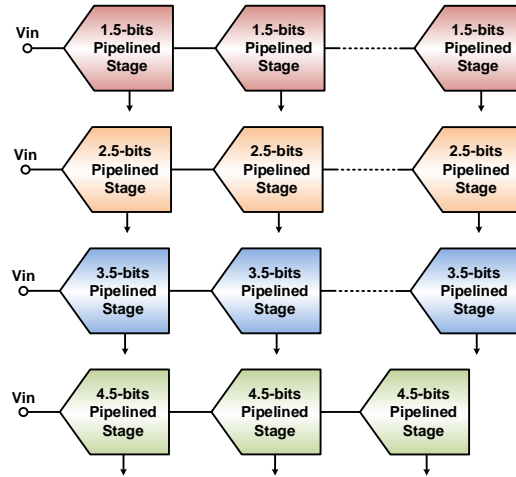


Fig. 3.1. Different available architectures for realizing a 12-bit pipelined ADC.

* Reprinted with permission from “Algorithmic-pipelined ADC with a modified residue curve for better linearity” by M. H. Naderi and J. Silva-Martinez, 2017. 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1446-1449, Copyright 2017 by IEEE.

bit/stage are computed as follows:

$$C_{T1} = \frac{C_1 C_2}{C_1 + C_2} + C_L; \quad \beta_1 = \frac{C_1}{C_1 + C_2} = \frac{1}{2}; \quad (3.1)$$

$$\text{Loop Gain} = \frac{G_{m1} R_{01}}{1 + s R_{01} C_{T1}} \cdot \beta_1 \quad (3.2)$$

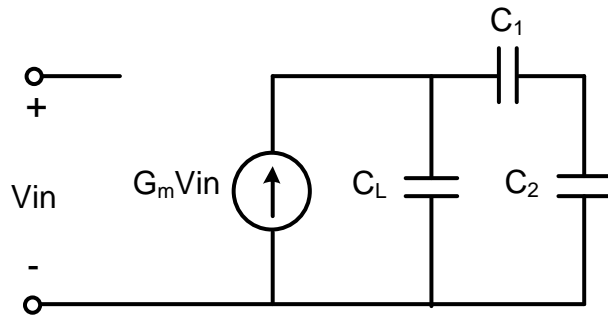


Fig. 3.3. Small-signal model of an OTA in the pipeline stage.

Where R_{01} is the amplifier's output resistance. The transient response of the closed loop operation, ignoring the effects of the additional parasitic poles, is determined by the unity gain frequency $\omega_u \cong GBW$ of the system's loop gain. The loop's gain unity gain frequency is then approximated as follows:

$$GBW \cong \frac{G_{m1}}{C_{T1}} \cdot \beta_1 \quad (3.3)$$

In the case that the next stage is not loading the OTA, then loop's unity gain frequency can be approximated as

$$GBW \cong \frac{G_{m1}}{C_1} \quad (3.4)$$

For a first order system, usually when the residue amplifier significant pole located at its output node, it is well known that the linear settling error is an exponential decaying function of the GBW. Thus, for N bits accuracy needed for the following sub-ADC, the settling error \mathcal{E} must be under $1/2^N$, therefore

$$GBW \cdot \tau_{residue} \geq \ln\left(\frac{1}{\mathcal{E}}\right) = N \cdot \ln(2) = 0.69 \cdot N \quad (3.5)$$

where $\tau_{residue}$ is the time allocated for residue computation. It is more appropriated to use N+1 instead of N in the previous equation to maintain the settling error within 1/2LSB; in the rest of the analysis we will use equation 4. If the capacitance of the 1.5-bit/stage used to satisfy noise considerations is fixed at $C_1=C_u$, the transconductance's requirement for the first stage amplifier can be found as follows:

$$G_{m1} \geq 0.69 \cdot (N) \cdot \left(\frac{C_{T1}}{\tau_{residue}}\right) \cdot \left(\frac{1}{\beta_1}\right) \quad (3.6)$$

According to this result, the required next stage bit's accuracy N, overall load capacitance C_{T1} , time allocated for the OpAmp to settle, $\tau_{residue}$, and the feedback factor β , are all equally relevant to optimize amplifier's settling time.

The cascade of N blocks with 1.5-bit/stage whose capacitors are scaled down by four

in succeeding stages leads to an input referred noise power that is N-times the noise power of the first stage. Now lets us consider the general case of M+0.5 bits per stage in the front-end. The number of switched capacitors needed in the MDAC is 2^M ; that generates an stage input referred integrated noise power equivalent to

$$v_n^2 = \frac{KT}{2^M \cdot C_{uM}} \quad (3.6)$$

Where C_{uM} is the unit capacitance used in the stage. Computing the overall capacitance in the stage and the feedback factor allow us to compute G_{m1} from (5) and compare the different architectures.

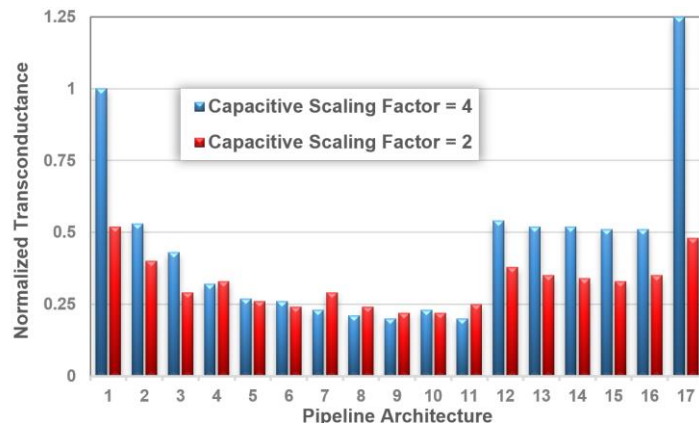
The total G_m (defined as the addition of the G_m values required by all the stages for the implementation of the entire ADC) required by different architectures for the realization of a 12-bit pipeline ADC is compared in Fig. 3.4. In all cases the capacitors are properly scaled to maintain the overall thermal noise at the same level for all architectures. Capacitive scaling factors that lead to 50% power noise in the following stage (in red) and same noise power in all stages (in blue) are used. The total transconductance required in every realization is normalized to the overall G_m required by the 1.5-bit/stages solution. OpAmp noise is not included in these results, it is assumed that noise is dominated by kT/C components. Thermal noise due to OpAmp noise increases more for the solutions with lower G_m in the first stage, then slightly reducing the difference among the architectures shown in Fig. 3.4.

As it can be seen from Fig. 3.4, cascading the 4.5-bit stages topology for realizing a

12-bit pipeline ADC is the most power efficient solution. But there are some other considerations that make this architecture less competitive. In the Fig. 3.4, the minimum unit capacitor for satisfying the capacitive mismatch requirement in pipeline stages was not considered. For example, the realization of the 4.5-bit first stage requires using a total capacitance of around 1.6 pF for 16 6-fF-unit capacitors in the second stage if scaled according with the square of residue amplifier gain. However, utilizing these small unit capacitors requires deploying mismatch calibration, which results in extra circuitry, extra power dissipation, and lengthy start-up time. According to Cadence simulations for the 40nm technology, the minimum unit capacitor demanded for the pipelined stages to perform a mismatch calibration-free 12-bit conversion is 20 fF.

Case #	1st Stage	2nd Stage	3rd to the Last Stages
1	1.5-bit	1.5-bit	1.5-bit
2	2.5-bit	1.5-bit	1.5-bit
3	2.5-bit	2.5-bit	2.5-bit
4	3.5-bit	1.5-bit	1.5-bit
5	3.5-bit	2.5-bit	1.5-bit
6	3.5-bit	3.5-bit	3.5-bit
7	4.5-bit	1.5-bit	1.5-bit
8	4.5-bit	2.5-bit	1.5-bit
9	4.5-bit	3.5-bit	1.5-bit
10	4.5-bit	4.5-bit	4.5-bit
11	4.5-bit	4.5-bit Alg	4.5-bit Alg
12	4.5-bit Alg	1.5-bit	1.5-bit
13	4.5-bit Alg	2.5-bit	1.5-bit
14	4.5-bit Alg	3.5-bit	1.5-bit
15	4.5-bit Alg	4.5-bit	4.5-bit
16	4.5-bit Alg	4.5-bit Alg	4.5-bit Alg
17	1.5-bit	4.5-bit Alg	1.5-bit

(a)



(b)

Fig. 3.4. Comparison of the overall transconductance required by the different architectures for implementing the 12-bit pipeline ADC: a) architectures considered and b) overall transconductance required for each case.

By considering the minimum unit capacitor of 20 fF, the load capacitance from the second 4.5-bit stage to the first stage residue amplifier increases from 96 fF (16×6 fF) to 320 fF (16×20 fF). This additional load requires much more transconductance from the first residue amplifier when the cascading 4.5-bit/stage leads to limited power efficiency. The total Gm required by different architectures for the realization of the 12-bit pipelined ADC is recalculated by considering the minimum unit capacitor of 20 fF as shown in Fig. 3.5 (in bricked red). The cascade of 3.5-bit pipelined stage shows the best analog power efficiency when implementing a 12-bit mismatch calibration-free pipelined ADC among different architectures.

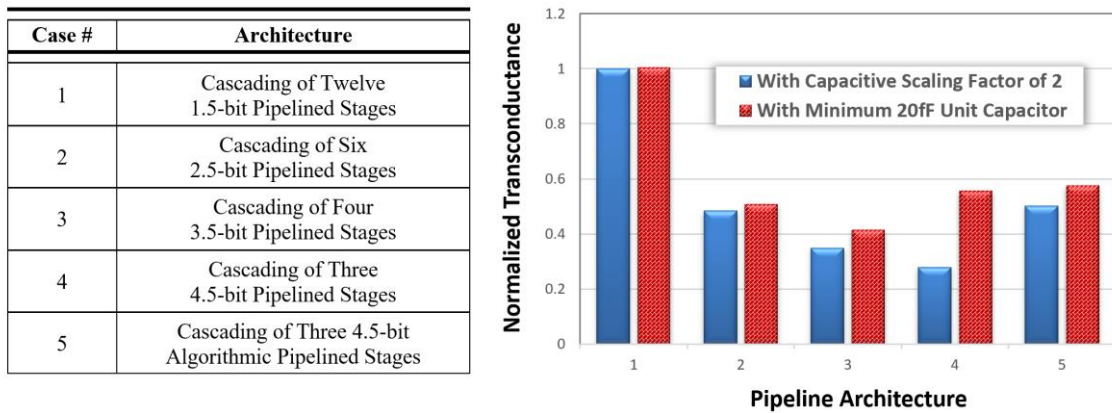


Fig. 3.5. Comparison of the overall transconductance required by the different architectures for implementing the 12-bit pipelined ADC.

Moreover, the 4.5-bit pipelined stage needs complicated sub-ADC design which requires about two times of comparators in the sub-ADC of the 3.5-bit pipelined stage. In addition, each comparator requires 2x finer accuracy in compare to a comparator in the 3.5-bit pipelined stage. As a result, in the 4.5-bit pipelined stage, the sub-ADC power

consumption would be much more than the sub-ADC in the 3.5-bit pipelined stage. Overall, when the power consumption of the sub-ADC, MDAC, and output encoder are taken into account, the cascading of 3.5-bit pipelined ADC shows superior power efficiency. Thus, Fig. 3.6 shows the most power-optimized architecture for realizing the 12-bit ADC.

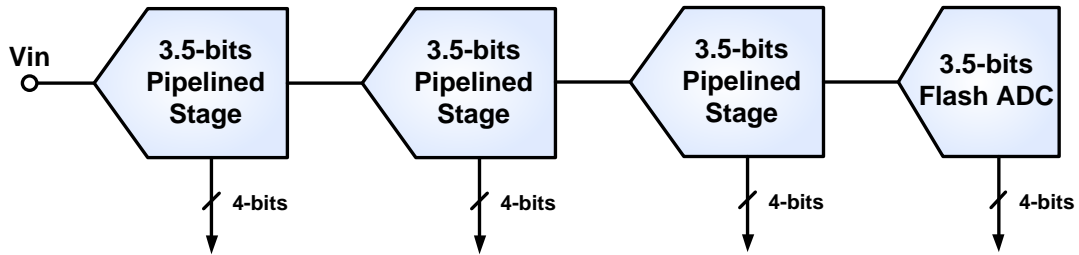


Fig. 3.6. Most power efficient 12-bit pipelined ADC architecture by considering the all components power consumption.

3.3. Conclusion

In this section, the calculation of minimum total required transconductance for the different architectures of 12-bit pipelined ADC is proposed. These calculations were based of evaluating the required G_m for different multi-bit pipeline stages for realizing a 12-bit pipeline stage. Many design factors like unit capacitor for each architecture, feedback factor, capacitor ratio, thermal noise, and minimum unit capacitor for each stage are considered in the calculation. It is found that cascading the 4.5-bit stages topology for realizing a 12-bit pipeline ADC is the most power efficient solution. But if the minimum unit capacitor of 20 fF is considered for all stages, the cascading of 3.5-bit pipelined ADC

shows superior power efficiency. This architecture would be utilized to implement a low power 12-bit 500-MS/s pipelined ADC in Chapter 5.

4. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH CLASS-B SLEW-RATE BOOSTING TOPOLOGY FOR FAST HIGH-PERFORMANCE SWITCHED-CAPACITOR CIRCUITS*

4.1. Introduction

Most analog-to-digital converters (ADCs) like pipelined ADCs and discrete-time delta sigma modulators as well as high performance filters in the audio and video systems are based on switched-capacitor (SC) techniques [28]–[41]. For high-speed and large signal swing applications, the operational amplifier must settle into its final value within a time frame, which is a fraction of the main clock period, i.e., around 45% in the case of conventional two-phase SC circuits, which is usually in the range of nanoseconds for more than 100 MS/s (mega-samples per second) applications. For large signals, the settling process consists of two phases: slewing and linear settling. The slew phase does not require high precision, but a large amount of current is needed to more quickly move the output voltage from its initial condition closer to its final voltage value.

Decreasing the slewing time allow us to allocate more time for the linear settling phase, which is dictated by loop bandwidth properties, e.g., gain-bandwidth products of the operational amplifier, loading conditions, feedback factor, and location of poles and zeros.

Usually, reducing the slewing time requires a large static current available at the amplifier's output to efficiently drive the feedback and load networks. The high current

* Reprinted with permission from “Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched-Capacitor Circuits” by M. H. Naderi, S. Prakash, and J. Silva-Martinez, 2018. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, pp. 3769-3779, Copyright 2018 by IEEE.

requirement at the output stage of a class-A amplifier must satisfy the high slew-rate needs, which drastically increases the amplifier's power consumption [42]–[46]. Current amplification has been used that is relying on increasing the tail-current efficiency by mirroring and amplifying the differential's input stage current [47]–[54]. In SC circuits, the differential current is produced by a differential voltage step at the beginning of the settling phase that turns one of the differential input transistors OFF and another input transistor ON [55]–[57]; this is especially noticeable in the presence of large input steps. The differential current, which is dictated by the input stage tail current, is mirrored and amplified and then delivered to the loading impedance. As a result, a high slew-rate is achieved at the expense of higher power consumption.

There are additional limitations in the case of low supply voltage deep sub-micron technologies. By reducing the full-scale voltage in pipeline ADCs, the voltage step across the differential input transistor is relatively small and may not exceed the input stage's overdrive voltage. This effect is often present when large number of bits per stage are used; the input voltage is reduced to be the ADC's full-scale value divided by 2^N ; N being the number of bits resolved in that stage. Thus, only a small portion of the tail current used in the amplifier's input stage is processed, then resulting in slower settling time. Therefore, in order to maintain faster settling time, large amount of dc bias current is needed. Moreover, the extensive use of class-A circuits will limit solution's power efficiency.

The slew rate can be boosted by utilizing class-AB stages [58, 59]. In [59], a class-AB stage provides high dynamic current when demanded, but the bias current is relatively small. For switched-capacitor circuits, large current values can be generated by utilizing a

class-AB stage; however, the quiescent current has to be maintained at level such that the required linear settling requirements are satisfied. Settling errors are dictated by small signal parameters such as overall transconductance gain, bandwidth and low-frequency loop gain. Enhancing the slew rate utilizing a hybrid dynamic amplifier was proposed in [60]. However, the hybrid amplifier requires optimization of its different building blocks for slew rate, phase margin, stability, and accuracy. Also, since the initial step voltage in the pipelined stages decreases when increasing the number of bits per stage, the class-AB alone amplifier in [60] might not be able to perform well for the case of higher number of bits per stage. Therefore, only 2.5-bit pipelined stages are utilized which is not the most power efficient solution due to the required transconductance for the different pipelined ADC architectures [61]. Table 4.1 summarizes the properties of available architectures as well as the proposed slew-rate boosting technique.

Table 4.1: Advantages and drawbacks of available slew-rate boosting solutions

Technique	Current Amplification [56]	Class-AB Stage [60]	The Proposed Technique
SR correlated with Tail-Current	No	Yes	Yes
Functional for Low Supply Voltage	No	No	Yes
Fully functional for Multi-Bit (>3) Pipelined Stage	No	No	Yes
Required Optimization Between Different Building Blocks	No	Yes	No

In this section, we propose a slew-rate boosting technique based on the generation of high dynamic current when fast response is demanded. The proposed concept relies on

monitoring the amplifier's input stage, employing a low-power single-stage ultra-fast preamplifier to detect the need for a higher current to boost the amplifier's slew-rate. Preamplifier output is used to drive a class-B amplifier with controlled hysteresis that can generate up to three times the current delivered by the main amplifier. Static power overhead is no more than 20%, and the noise level increases by 1dB; effects on input capacitance are negligible. The auxiliary circuit extends the frequency range of a 4.5 bit/stage residue amplifier from 400 MHz (core bandwidth) up to 780 MHz while maintaining the third harmonic distortion around -48 dB.

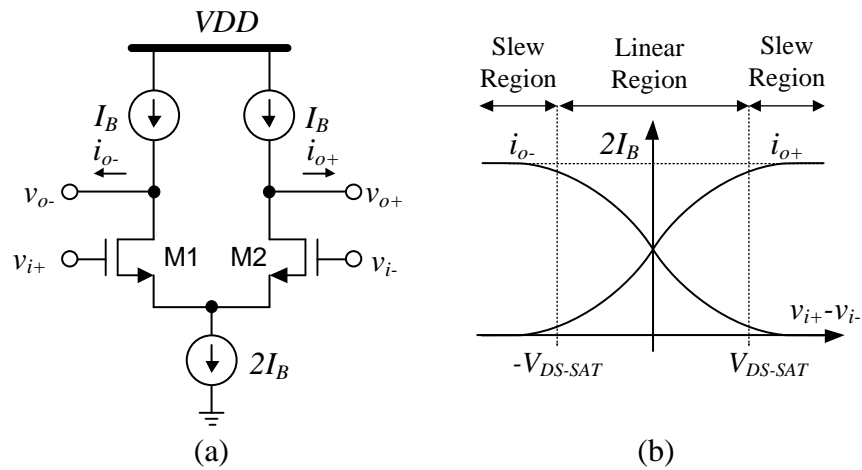


Fig. 4.1. a) Differential pair and b) output current versus the voltage across the input transistors in a simple OTA.

4.2. Slew-Rate Function of an OTA Based SC Circuit

The output current versus the voltage across the gate of the input transistors in the

simplest OTA is depicted in Fig. 4.1. The OTA's output current shows two different regions, the linear region and the slewing (saturation) region. When the input voltage across the differential pair is less than the overdrive voltage $V_{ds,sat}$, the transistors operate in their saturation regime, and in a first approximation the current is proportional to the differential input voltage. For input voltages larger than $V_{ds,sat}$, the current at differential pair outputs remain constant; either one zero or $2I_B$.

4.2.1. Unloaded Switched-Capacitor Circuit

Let us consider the step response of a capacitive amplifier, commonly found in switched-capacitor circuits. Assuming zero initial conditions in the capacitors, when a large input step voltage is applied to the unloaded switched capacitor gain stage, the OTA acts as a constant DC-current source, as shown in Fig. 4.2. Right after the input step is applied, the voltage at the inverting terminal is identical to the input signal, which leads to

$$V_x = V_i = V_o \quad \text{at } t = t_{0+}. \quad (4.1)$$

If V_x is close or exceeds the overdrive voltage $V_{DS,sat}$, the OTA operates in the slew regime. The OTA generates the maximum possible current at its output and returns V_x towards ground as shown in the Fig. 4.3; V_x and the output voltage is estimated as follows.

$$V_x = V_i - \frac{I_B}{C_1} \cdot (t - t_0). \quad (4.2)$$

$$V_o(t) = V_i - I_B \cdot \left(\frac{1}{C_1} + \frac{1}{C_2} \right) \cdot (t - t_0). \quad (4.3)$$

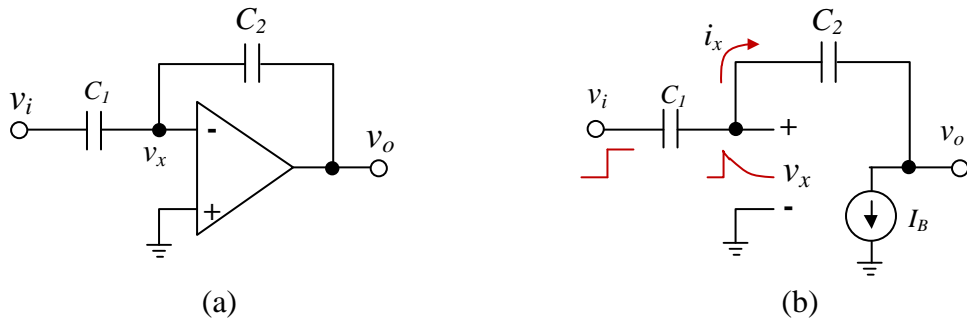


Fig. 4.2. Operation of the OTA when slewing in the switched capacitor gain stage without loading at the output stage.

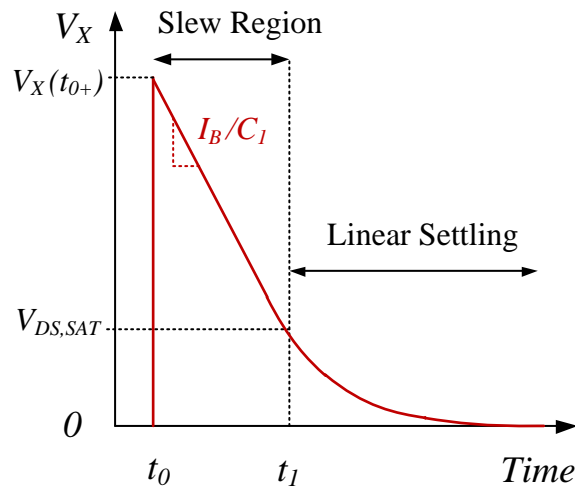


Fig. 4.3. Operational transconductance amplifier (OTA) waveform input voltage when slewing in the switched capacitor gain stage without loading at the output stage.

The output slew rate is a function of the I_B/C ratio and its boosting requires larger amount of current and/or use of smaller capacitors. Unfortunately, the capacitors cannot be reduced since the thermal kT/C noise level must be maintained at a low level; hence, a large amount of power is needed for highly demanding systems that requires fast response and high resolution.

In most practical cases, the capacitors are pre-charged from a previous phase. In the worst case, the voltage variation at the amplifier's input would be even larger than expected. Right after the circuit is reconfigured as shown in Fig. 4.2. Based on the capacitor's initial conditions, the amplifier's input voltage is estimated after the capacitors are rearranged. This process can be shown through the following equation and is obtained using charge recombination techniques.

$$V_x(t_{0+}) = \frac{C_1(V_i(t_{0+}) - V_{c1}(t_0)) - C_2V_{c2}(t_0)}{C_1 + C_2}. \quad (4.4)$$

$V_{c1}(t_0)$ and $V_{c2}(t_0)$ in (4.4) correspond to the initial conditions in C_1 and C_2 , respectively. Equation (4.4) shows that the initial voltage variation at the inverting terminal of the amplifier, $V_x(t_{0+})$, occurs after the connection of the capacitors. According to this equation, large excursions at the amplifier's input will occur when $V_{c1,2}(t_0)$ and the input voltage $V_i(t_{0+})$ have opposite polarity; this is the worst case for a slew-rate and slew may occur even if $V_i(t_{0+})$ does not exceed $V_{ds,sat}$.

The initial amplifier's input voltage $V_x(t_{0+})$ after the input pulse is applied is returned to its steady state value according to the slope of I_B/C_1 over time, as illustrated in Fig. 4.3.

This constant current condition is maintained until the voltage across the input differential pair reaches the overdrive voltage; then, the amplifier's input stage will operate in a linear regime.

4.2.2. Loaded Switched-Capacitor Circuit

Fig. 4.4 shows the operation of the amplifier slewing when loaded by C_L ; the parasitic capacitor C_P present at amplifier input is also included. The output capacitor C_L is usually pre-charged to a voltage before the charge recombination phase; this charge is a function of the operation of the following stage during the previous clock phase. The initial charge stored in all capacitors determines the instantaneous voltage at the amplifier's input after the capacitors are reconnected; V_x is then computed as

$$V_x(t_{0+}) = \frac{C_1(V_i(t_{0+}) - V_{C1}(t_0)) - C_P V_{CP}(t_0)}{C_1 + C_P + \frac{C_2 C_L}{C_2 + C_L}} + \frac{\left(\frac{C_2 C_L}{C_2 + C_L}\right)(V_{CL}(t_0) - V_{C2}(t_0))}{C_1 + C_P + \frac{C_2 C_L}{C_2 + C_L}}. \quad (4.5)$$

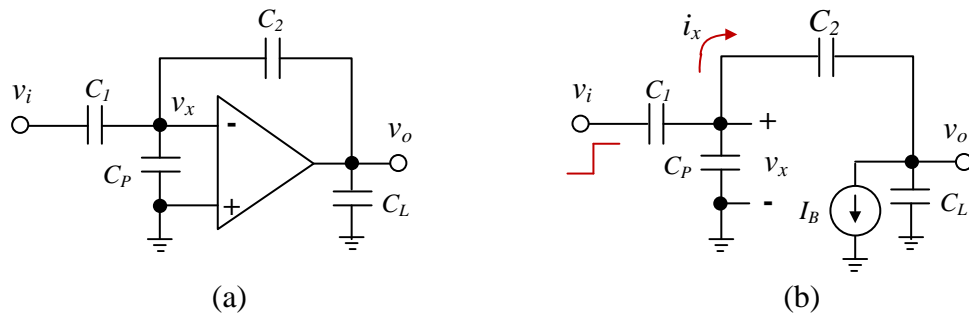


Fig. 4.4. OTA operation when slewing in the switched capacitor gain stage by considering the load capacitor.

In (4.5), $V_{CL}(t_0)$ represents the initial voltage at C_L , and $V_i(t_{0+})$ corresponds to the input voltage right after the input pulse is applied. Usually $V_{CP}(t_0)$ is small compared with the other terms and can be safely ignored for a sake of simplification in the analysis. It is worth mentioning that the amount of current that discharges $V_x(t_{0+})$ is smaller than the maximum amplifier output current, I_B , since there is a current divider effect due to the presence of C_L . The amplifier's input voltage $V_x(t)$ returns to its steady state according to:

$$V_x(t) = V_x(t_0) - \left(\frac{I_B}{1 + C_L \left(\frac{1}{C_2} + \frac{1}{C_1 + C_P} \right)} \right) \cdot \left(\frac{t - t_0}{C_1 + C_P} \right) \quad \text{if } |V_x(t)| \geq V_{dsat}. \quad (4.6)$$

The rate of variation of amplifier's input voltage V_x is then dictated by

$$SR_{V_x} = - \left(\frac{I_B}{1 + C_L \left(\frac{1}{C_2} + \frac{1}{C_1 + C_P} \right)} \right) \cdot \left(\frac{1}{C_1 + C_P} \right). \quad (4.7)$$

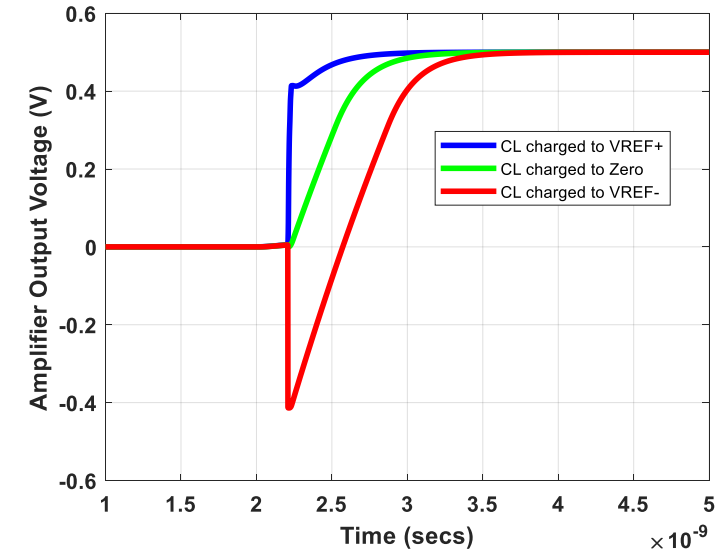
Equation (4.7) shows the (dis)charging feedback current is a portion of the maximum output current I_B . The slew-rate is determined by the current divider gain between C_L and the series of C_2 and the parallel of C_1 and C_p ; the portion of the current flowing through C_2 is then integrated by $C_1 + C_p$ and determines the speed of the variation at node V_x . The larger the load capacitor C_L is, the smaller the slew-rate. In a first approximation, the slew time is then computed as follows:

$$T_{slew} = (V_x(t_{0+}) - V_{ds_sat}) \left(\frac{C_1 + C_P + C_L \left(1 + \frac{C_1 + C_P}{C_2} \right)}{I_B} \right). \quad (4.8)$$

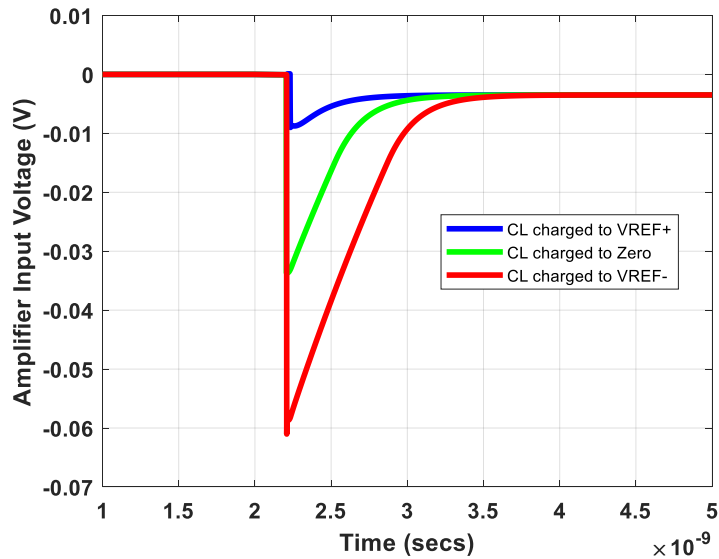
According to (4.5) and (4.8), slew time is a function of the capacitor's initial conditions as well as the amplitude of the $V_x(t_0)$. The slew-time increases with large capacitors C_L , C_1 and C_P ; it also increases when reducing C_2 . This results in the switched capacitor trade-off; larger capacitors reduce thermal noise power but increase settling-time.

To get more insight on the design trade-offs, let us consider the case of a residue amplifier used in a 4.5-bit pipelined stage. For this case, assume that the feedback factor $\beta = \frac{C_2}{C_1 + C_2} = 1/16$, amplifier's gain-bandwidth product $GBW = 4.5 \text{ GHz}$, $C_1 = 825 \text{ fF}$, $C_2 = 55 \text{ fF}$, $C_L = 420 \text{ fF}$, Amplifier $DC \text{ Gain} = 43 \text{ dB}$, and sampling frequency $F_s = 400 \text{ MHz}$. The C_1 and C_2 values were based on the maximum total allowed input referred noise limit to satisfy the thermal noise requirement for the first 4.5-bit pipelined stage in a 12-bit pipelined ADC. The C_L value was based on minimum unit capacitance for satisfying the mismatch requirement, input referred noise, and considering 100 fF parasitic capacitance from sub-ADC in the second 4.5-bit pipelined stage of a 12-bit pipelined ADC. The target is to achieve a settling error under 0.25% in $T_s/2$ secs (1.25 nsecs). Fig. 4.5 displays the amplifier's transient response for three different initial conditions on the load capacitor. According to these results, it is evident that we have to consider the very worst case when computing the required settling time. The 0.25% settling time for each one of these cases is 0.8 nsecs, 1.25 nsecs and 1.75 nsecs,

respectively. The worst-case condition takes more than twice the settling time of the best case.



(a)



(b)

Fig. 4.5. Different slewing-time of the class-A residue amplifier based on the initial stored-voltage on the load capacitor: a) differential amplifier input voltage V_x and b) amplifier's output voltage. The 0.25% settling time for each case is 0.8 nsecs, 1.25 nsecs and 1.75

nsecs, respectively.

According to equation (4.8), the slew time can be reduced by increasing V_{ds_sat} ; this approach, however, is not advisable since linear settling time will be affected and results in a limitation on voltage headroom. Although the quadratic equation is not accurate for short channel devices, it can help us to get some intuition on the amplifier's design tradeoffs; the transistor's small signal transconductance of a differential pair is approximated as $g_m \approx 2I_B/V_{ds_sat}$. The larger the saturation voltage, the smaller the transconductance for constant current. On the other hand, decreasing further the overdrive voltage of the differential pair has a negative impact on the slew time since the transistor may enter into a subthreshold region, thereby reducing its current driving capability. Optimizing V_{ds_sat} is recommended for best bandwidth and required noise level; usually, a good compromise is to keep its value in a range between 80 mV and 200 mV for the TSMC 40nm technology under 1.1V supply voltage. The proposed design strategy is to make the design procedure independent for the best possible slew rate and faster linear settling.

4.3. Slew-Rate Boosting Employing an Auxiliary Class-B Amplifier

For high-gain broadband amplifiers, class-AB solutions are desirable to save power. The output stage must be optimized for both small signal performance and high GBW for linear settling; this last parameter usually demands significant power consumption that limits the power efficiency of the class-AB topology. Usually the class-AB amplifier suffers from crossover distortion, which limits its linearity and increases its design

complexity. Also, in the two-stage class-AB stage, the first stage must be very fast and must provide high gain at the same time; these two requirements conflict with each other. In the proposed topology, two amplifiers work in parallel where the main amplifier is solely optimized for a linear settling, while the auxiliary two-stage amplifier operates for slew rate boosting. The architecture utilizes a low-power high speed pre-amp in cascade with a class-B stage that allows boosting main amplifier's slew-rate. Unlike the conventional slew-rate boosting that relies on the tail-current, in the proposed topology, the slew rate is based on the injection of a highly dynamic current, which is available on demand from the class-B auxiliary amplifier. Thus, the main amplifier is designed to satisfy the required linear settling and DC gain while the auxiliary amplifier determines architecture's slew rate when driving large voltage variations.

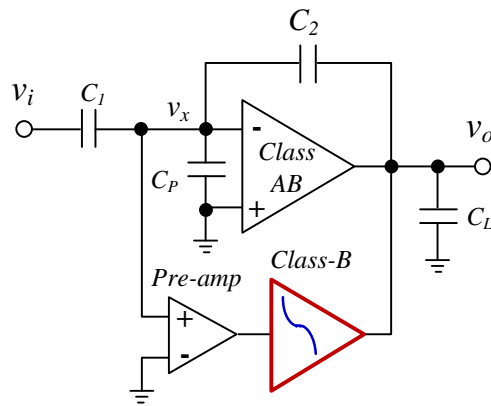


Fig. 4.6. Simplified schematic of the proposed amplifier aided with an auxiliary pre-amp followed by a class-B amplifier to boost its overall slew rate.

The proposed topology employs a high-speed, low-power pre-amplifier followed by a low-power class-B auxiliary amplifier as displayed in Fig. 4.6. The class-B amplifier turns

on when the main amplifier's input voltage exceeds the threshold voltage (16 mV in this case) differential signal swing. When activated, the class-B amplifier delivers most of the current demanded by the load and feedback capacitor. When the amplifier's input voltage is reduced, the class-B amplifier is less effective, and the linear settling is dominated by the action of the primary amplifier. The auxiliary circuit is OFF when processing small signals. Thus, the AC response of the overall circuit would be almost the same as the one of the main amplifier; some small parasitics are the difference. Linear settling behavior of the overall circuit would be same as linear settling behavior of the main amplifier.

The primary amplifier consists of the cascade of a class-A pre-amp and a class-AB output stage. The main amplifier is optimized for linear settling by satisfying the minimum required DC gain and small signal transconductance while the class-B amplifier shows a large current capability when activated.

4.3.1. Main Amplifier

A two-stage pseudo class AB (class A cascaded with class AB) amplifier was chosen as the main amplifier as shown in Fig. 4.7. The first stage, composed by transistors M1–M8, achieves high gain due to the cascode nature of its components. Resistors R1 and R2 are used to set the bias point without the need of a CMFB circuit. The first stage is DC connected to the P-type output (transistors M9 and M10) and the AC is also coupled to the N-type amplifier realized through transistors M11 and M12. The AC connection through CB boost the high frequency AC transconductance by 6 dB. This high-frequency signal path enables the architecture to operate as a true class AB amplifier with the ability

Then, a small dc-current (0.5 mA) is set as the output stage current to provide enough small signal transconductance since the output resistance of the first stage is high. Then, Miller compensation through C_z and R_z is used. Thus, the dominant pole is placed at the output node of the amplifier's first stage. An external resistor is used for the generation of the reference DC current, and weighted current mirrors are employed to generate the bias current needed in each stage. Table 4.2 shows the amplifier device sizes including dimensions and bias conditions for the relevant transistors and component values. Total amplifier's power consumption is 2.75 mW. Simulated results show that 0.25% settling time is under 1.8 nsecs, while the DC gain is over 49 dB.

Table 4.2: Amplifier device sizes

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)	Drain Current (μA)
M1-M2	20/0.08	750
M3-M4	15/0.12	750
M5-M6	30/0.08	750
M7-M8	30/0.12	750
M9-M10	16/0.06	400
M11-M12	8/0.06	400
Component		Value
R_B		20 k Ω
C_B		200 fF
R_Z		400 Ω
C_Z		100 fF

4.3.2. Slew-Rate Booster

The proposed slew rate boosting auxiliary circuit employs simple circuitry to detect the need for injecting high-dynamic current at the output load by implementing a pre-amp

followed by a class-AB amplifier. The simplified schematic is shown in the Fig. 4.8. The high-speed pre-amp amplifies the error signal present at the input of the main amplifier and then increases the sensitivity of the class-B output stage (MN1-MN2 and MP1-MP2). The class-B output stage operates in a subthreshold region to reduce power consumption; it also enables slew-rate booster circuit operation with a defined hysteresis around 16 mV. For that purpose, VBN and VBP voltages are properly set. The transistors are computed such that MP1, MP2, MN1, and MN2, can provide up to five times of the main amplifier output current in the slew mode and in the presence of large signals. Although the disadvantage of the class-B amplifiers is the cross-over distortion, our proposed technique does not suffer from this effect because the proposed class-B amplifier is activated if and only if the signal swing at the input of the main amplifier exceeds 16 mV, and that happen when the signal is large; this stage remains OFF during small signal operation. The value of 16 mV threshold voltage is set based on adjusting 65 mV sub-threshold bias voltage for MP1, MP2, MN1, and MN2 and considering the gain voltage of 4 V/V for the pre-amp first stage.

The tail current of the pre-amp in the slew-rate booster is 0.4 mA; this current is smaller than the 1.5 mA tail current of the main amplifier's first stage. The in-band gain of the front-end amplifier is 8 V/V, and the -3dB bandwidth is as high as 1 GHz. Also, the input capacitance of the pre-amp is around 15 fF, which is small compared to the 65 fF of the input capacitance of the main amplifier. This additional capacitance does not have a major effect on either the loop gain or the amplifier's settling time of the main amplifier. Table 4.3 displays the device sizes including dimensions and bias conditions for the

relevant transistors and component values. The overhead power consumption is 0.55 mW after utilizing this auxiliary circuit, which is only 20% of the main amplifier power consumption.

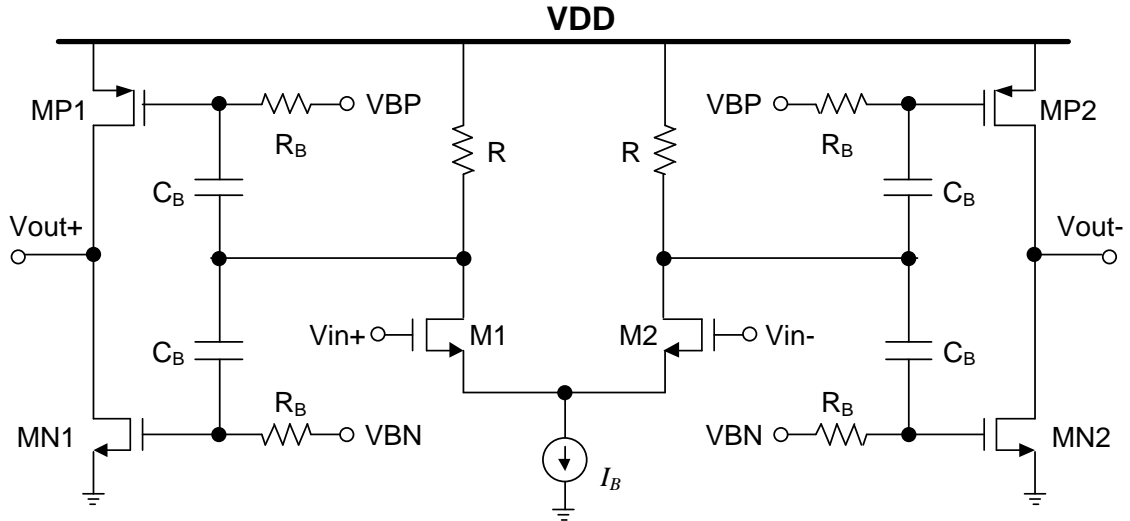


Fig. 4.8. The proposed auxiliary circuit for boosting main amplifier's slew rate.

Table 4.3: Slew-rate booster device sizes

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)	Drain Current (μA)
M1-M2	5/0.08	200
MN1-MN2	20/0.06	50
MP1-MP2	40/0.06	50
Component		Value
R_1		2.25 k Ω
C_B		500 fF
R_B		20 k Ω
I_{drain} (MN1, MP1)		0.15mA

The small signal model of the preamplifier and coupling network to the class-B output stage (see Fig. 4.8) used in the proposed slew-rate booster circuit is shown in the Fig. 4.9.

The transfer function would be derived as

$$H(s) = gm_1 \times \frac{R_1 R_B C_B s}{[(R_1 R_B C_{p1} C_{p2} + R_1 R_B C_B (C_{p1} + C_{p2}))]s^2 + [R_1 C_{p1} + R_B C_{p2} + (R_1 + R_B) C_B]s + 1} \quad (4.9)$$

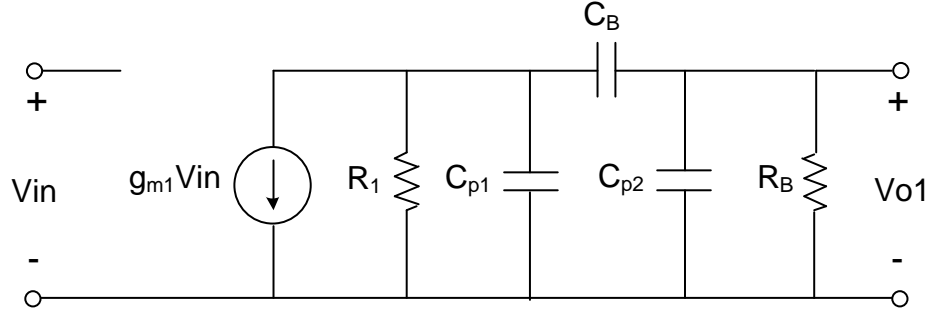


Fig. 4.9. Small-signal model of the pre-amplifier and coupling network including C_B and R_B .

In (9), C_{p1} and C_{p2} are the parasitic capacitances at the drain of the M1 and gate of the MP1/MN1, respectively. Since the parasitic capacitances are much smaller than C_B , equation (9) can be simplified as

$$H(s) = \frac{gm_1 R_1 R_B C_B s}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})} \quad (4.10)$$

where $\omega_{p1} \cong \frac{1}{R_B C_B}$ and $\omega_{p2} \cong \frac{1}{R_1(C_{p1} + C_{p2})}$. The dominant pole ω_{p1} is placed at low frequency, while the non-dominant pole ω_{p2} is placed at the highest possible frequency. At intermediate frequencies, the voltage gain is flat and dominated by $gm_1 R_1$ if $R_B \gg R_1$. Although the small signal analysis is interesting, it is not very useful since this circuit is not active for small signals. More interesting is the large signal analysis of its impulse and pulse response.

It can be shown that when enabled, the unity impulse response of the 2nd order function represented by (4.10), follows the behavior determined by

$$v_{o1}(t) \cong (v_{o1}|_{t=0}) \left(e^{-\omega_{p2}t} - \left(\frac{\omega_{p1}}{\omega_{p2}} \right) e^{-\omega_{p1}t} \right). \quad (4.11)$$

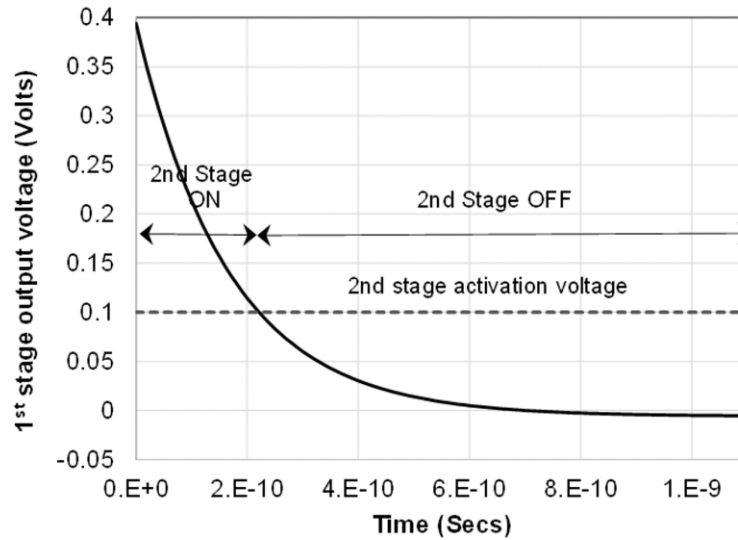


Fig. 4.10. Impulse response of a 2nd order amplifier (eqn. 11) showing the activation voltage for the amplifier’s second stage (dashed line).

Significant slow components may result from this circuit unless $\omega_{p2} \gg \omega_{p1}$. For this case, ω_{p1} is set at 100 Mrad/sec while ω_{p2} is set around 6 Grad/sec. Thus, the peak value of the slow component is 60 times smaller than the component lumped to the fast exponential component in equation (4.11). This equation is plot in Fig. 4.10; the dash line shows the activation voltage set at 100 mV for the class B (second-stage) amplifier, which correspond to a threshold voltage of around 16 mV at first amplifier input. The first part of the transient is dominated by the term $e^{-\omega_{p2}t}$; after 1% settling time, the behavior is dominated by the slow component $e^{-\omega_{p1}t}$. Notice in this figure that the slow settling component does not play a major role on the operation of the class-B amplifier; even 10% settling is enough for the proper functionality of the architecture. The speed of the overall circuit is dominated by the fast exponential component. Fig. 4.11 shows the main amplifier's frequency response versus the main amplifier with SR boosting frequency response. Since the auxiliary circuit is OFF when processing small signals, the AC response of the overall circuit would be almost the same as the one of the main amplifier; some small parasitics are the difference.

Fig. 4.12 shows the differential output current (from Cadence) versus the input voltage for both the main amplifier and the auxiliary amplifier. The auxiliary amplifier is turned OFF when the main amplifier's input voltage is less than 16 mV. For small signal variations, the slew phase is not critical; hence, the final settling time is determined by the parameters of the main amplifier. When the input step voltage exceeds the threshold voltage, the auxiliary amplifier delivers a high dynamic current—more than triple of main amplifier's output current and over 10 times greater than class-B amplifier bias current.

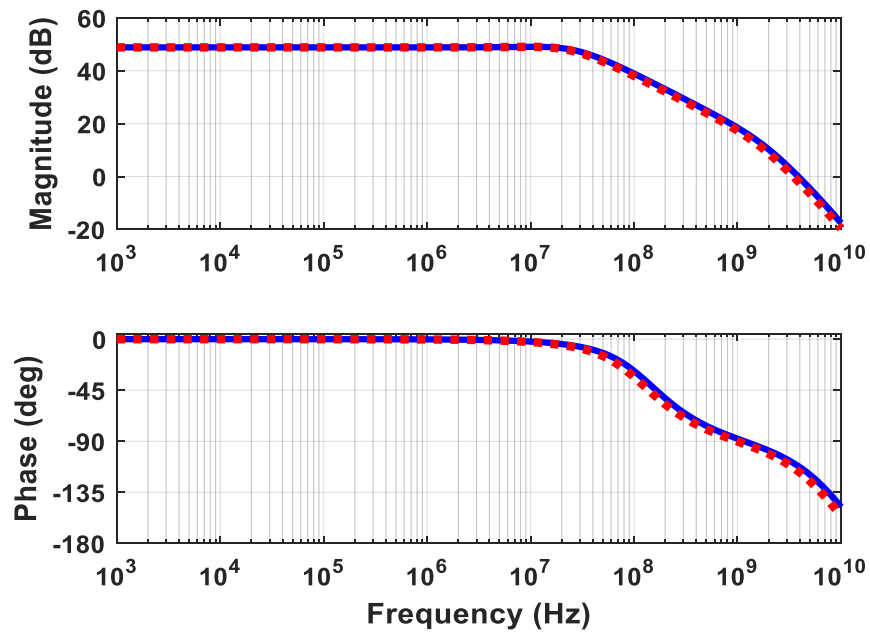


Fig. 4.11. Main amplifier's (solid line) and the main amplifier's with SR boosting (dotted line) frequency response: a) magnitude and b) phase.

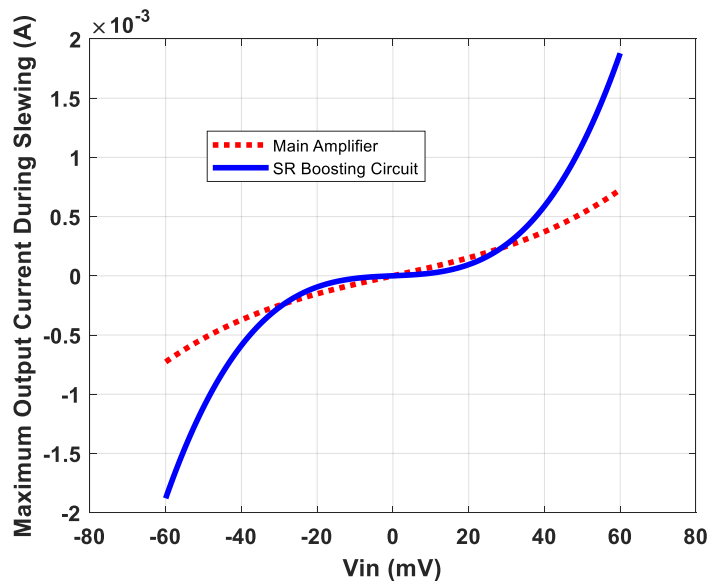


Fig. 4.12. Differential output current versus the input voltage for both the main amplifier (dotted line) and the auxiliary amplifier (solid line); cadence results.

To compare the current capability of the current booster, a differential narrow input pulse with 1 nsec width and 60 mV amplitude was used. For this simulation, amplifier's output was connected to a small resistor to measure the time delay and amount of current delivered by the amplifier components. Fig. 4.13 shows the results. The auxiliary class-B amplifier takes less 300 psecs delay to deliver/sink more than 1.7 mA and takes around 700 psecs for 1% settling; main amplifier delivers around 0.7 mA and settles (1%) in around 1500 psecs.

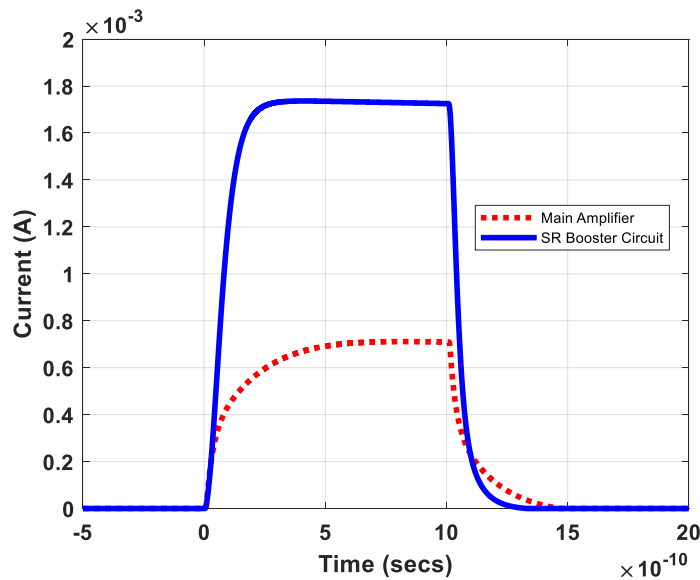


Fig. 4.13. Pulse response current of the main amplifier (dotted line) and slew-rate booster circuit (solid line): output current.

To verify the circuit behavior under a practical case, a 4.5-bit stage used in pipelined ADCs was used as a testbed; the very small feedback factor $\beta = 1/16$ [32]. The input capacitance ($C_1 = 16C_2$ in Fig. 4.6) was set at 880 fF while the feedback capacitor was set

at $C_2=55$ fF; capacitive amplification factor is 16. The capacitors were fully discharged, and the input signal was pulsed from zero to 62.5 mV. Fig. 4.14 shows the differential output current when the auxiliary amplifier is enabled and for the case of the standalone amplifier. The peak current of the enhanced architecture surpasses the one of the conventional one by a factor of 240%. For the proposed architecture, the current's peak value is reached in 180 psecs compared to 380 psecs when the main amplifier was operating alone. The superior performance of the proposed amplifier is more evident if we consider the slew time for the capacitive amplifier: 400 psecs for the proposed amplifier with slew boosting technique vs. 1050 psecs required for the conventional architecture.

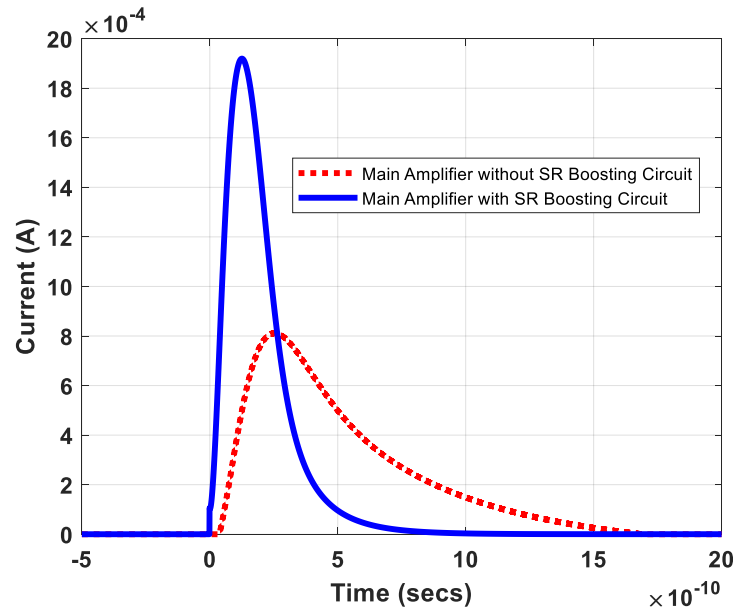


Fig. 4.14. Differential output current for the standalone amplifier (dotted line) and for the main amplifier with auxiliary amplifier enabled (solid line).

4.4. Experimental Results

The amplifier along with the slew-rate boosting auxiliary circuit was fabricated in the TSMC 40 nm CMOS process using core devices with a nominal value of 1.1 V. Fig. 4.15 shows the die photo of the amplifier along with the slew-rate boosting auxiliary circuit, where the core occupies 0.05 mm^2 . The single-ended test setup used to characterize the performance of the amplifiers in the 4.5-bit/stage pipelined stage prototype is shown in Fig. 4.16. The actual chip is fully differential. An Agilent E8267D PSG vector signal generator was used to supply the input signal and the output was captured using the Agilent Infiniium DSA91304A oscilloscope. To preserve the high output impedance of the amplifiers and set the DC value at the amplifier's input, R was set to be $5 \text{ M}\Omega$. As for C_1 and C_2 they were set to 880 fF and 55 fF , respectively, to resemble the operation of a capacitive amplifier of 16 V/V . The capacitor values were based on the maximum total allowed input referred noise limit to satisfy the thermal noise requirement for the first 4.5-bit pipelined stage for a 12-bit pipelined ADC. The load impedance from the bond wire, pads, and equipment was driven by an extra buffer placed at the output of the gain stage. The buffer's input capacitance is around 180 fF , which introduces an additional load to the gain stage amplifiers.

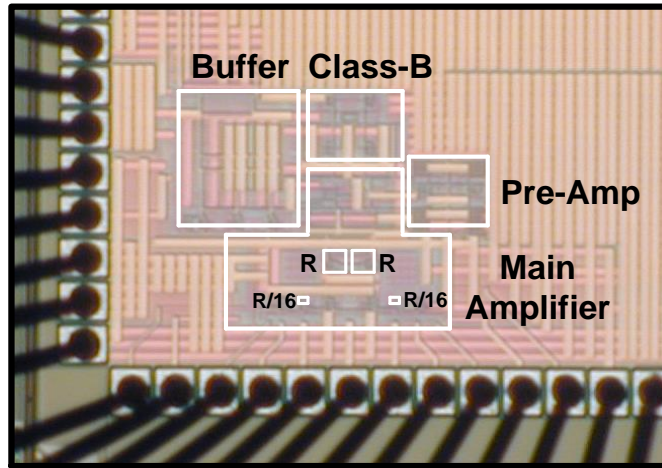


Fig. 4.15. Chip micrograph.

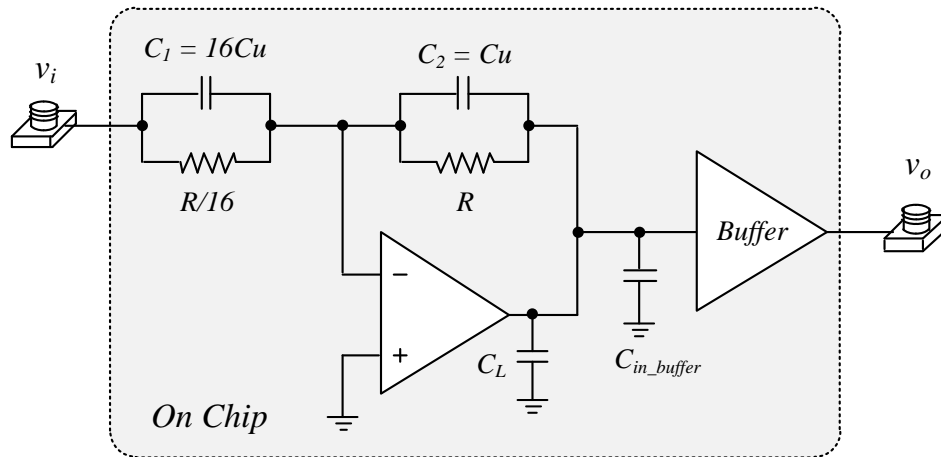


Fig. 4.16. Simplified (single-ended) version of the amplifier characterization setup used to measure the performance of the slew-rate boosting technique.

A 62.5 mVpp input step voltage was applied to generate a 1Vpp output step variation. The measured output waveform results were compared to the amplifier without the slew-rate booster in Fig. 4.17. The proposed architecture shows a 0.8 nsecs shorter slew time

(45% smaller than the amplifier without SR boosting) and 0.7 nsecs shorter 1% settling time, which is 28% smaller than the conventional solution. These results include the effect of the on-chip buffer, bondwire inductance and input impedance of the test equipment; 1% settling time is around 1.8 nsecs but simulation results show that standalone amplifier's 1% settling time is around 1 nsec.

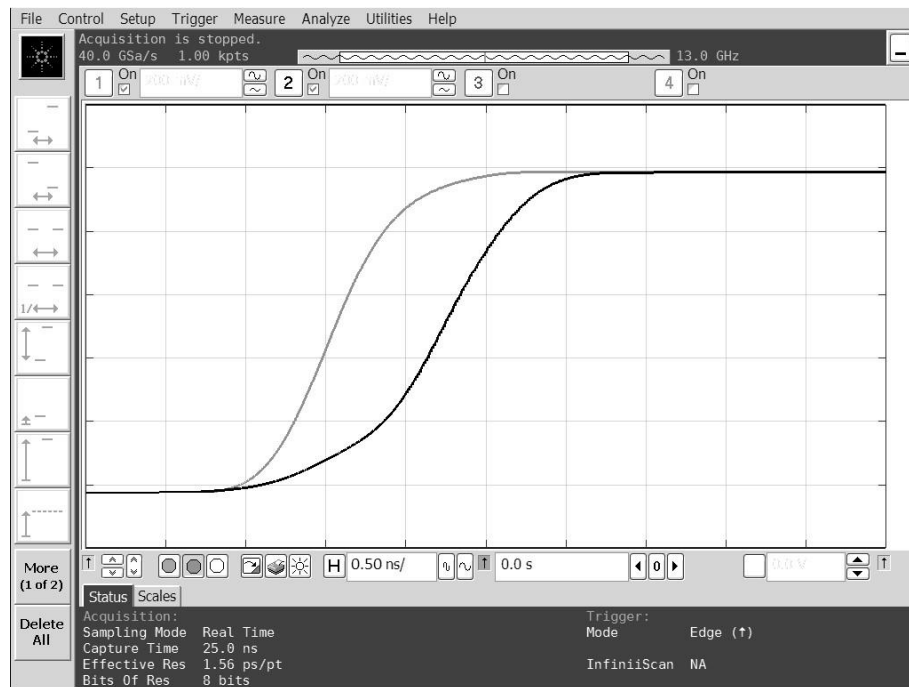


Fig. 4.17. Measurement results of a large input step voltage for the pseudo class-AB amplifier with SR boosted technique and the conventional pseudo class-AB amplifier in the prototype of a 4.5-bit/stage pipelined ADC.

The linearity of the x16 capacitive amplifier was characterized as well. Fig. 4.18 shows the output harmonic components for both circuits with a 500 MHz input signal and

62.5 mVpp amplitude. High frequency large signals demand a larger amplifier slew-rate to follow the fast signal variations. According to these results, the proposed architecture surpasses the linearity of the conventional amplifier by more than 10 dB. The linearity of both amplifiers was compared for different frequencies in the range of 100 MHz to 500 MHz. The results are plotted in Fig. 4.19. The third harmonic distortion of the two amplifiers is similar for low frequency conditions since signal variation is not very slew demanding. Table 4.4 compares the measured results for the class-AB amplifier with and without boosted SR technique. For the same loading and same core amplifier, the proposed architecture shows an improvement of 100% in slew-rate and a reduction of 28% in the 1% settling time. The proposed architecture's HD3 is maintained under -48 dB (8 bits resolution) up to 780 MHz, while the conventional amplifier can only operate properly until 400 MHz. The cost of these benefits represents an increase in power consumption of 20% and a 1 dB increase in noise level that comes from pre-amp circuit in auxiliary path.

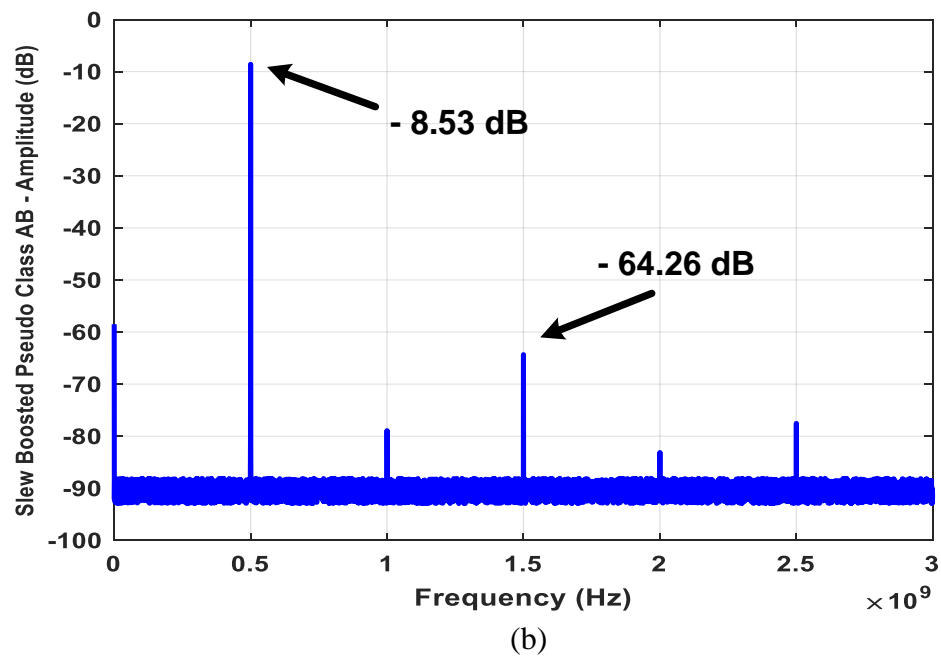
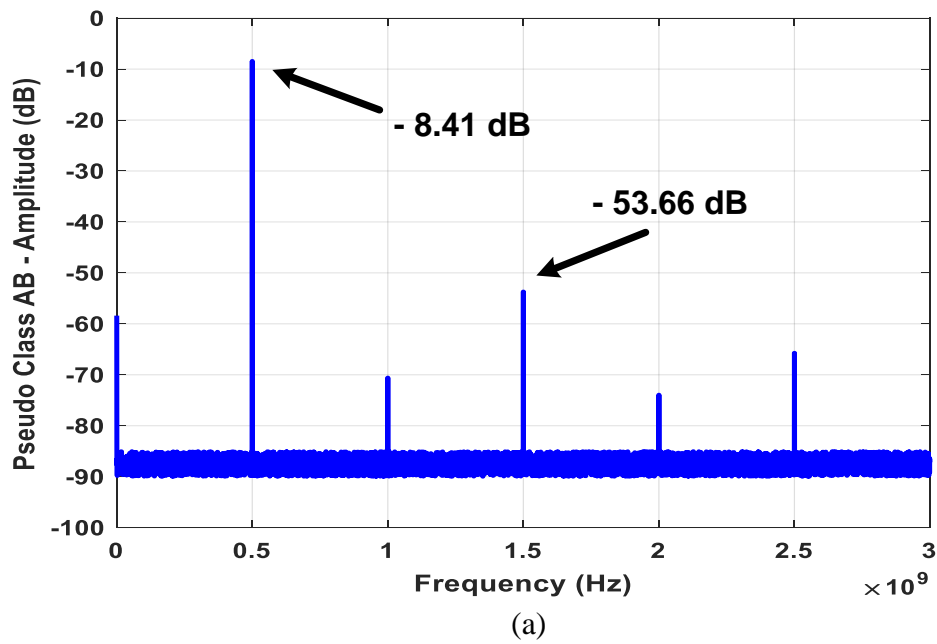


Fig. 4.18. Measured spectrums for a 500 MHz tone for a) stand-alone amplifier and b) an amplifier with the SR boosting SR technique enabled.

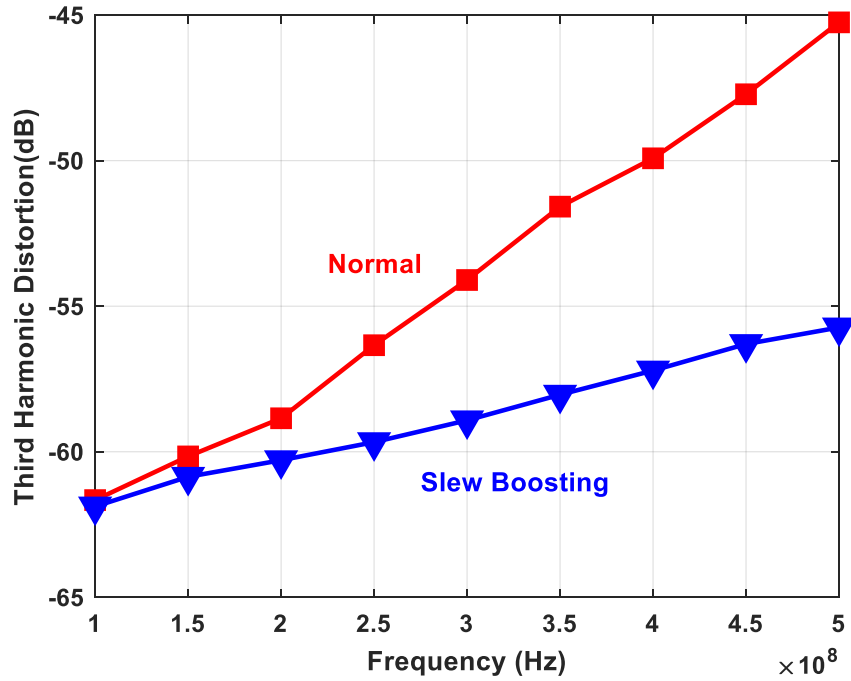


Fig. 4.19. Measured spectrums for a 500 MHz tone for a) stand-alone amplifier and b) an amplifier with the SR boosting SR technique enabled.

4.5. Conclusion

A new technique for slew-rate boosting based on high injection of the dynamic current only when the high slew-rate is demanded is proposed in this section. The proposed technique makes use of a high-speed pre-amp followed by a class-B auxiliary amplifier that delivers high output current only when high slew-rate is demanded when large input signals arise.

The proposed technique is suitable for high-speed, low-supply voltage low-power multi-bit/stage pipelined ADC applications. Measurement results for the proposed

architecture demonstrate that the proposed scheme shortens by 28% the amplifier's 1% settling time. Also, utilizing this technique provided more than 10 dB better linearity for a 500 MHz input signal, while only a 20% power consumption overhead is reported due to the extra circuitry.

Table 4.4: Comparison of experimental results

Parameter	[55]	Pseudo Class-AB Amplifier	Pseudo Class-AB Amplifier with SR Boosting [62]
Technology	0.18 μm CMOS	TSMC 40 nm	TSMC 40 nm
Supply Voltage	1.8	1.1 V	1.1 V
Static Current	0.194 mA	2.5 mA	3 mA
DC Gain	60 dB	49 dB	49 dB
Small signal GBW	160 MHz	3.6 GHz	3.6 GHz
Open Loop PM*	75 degrees	65 degrees	65 degrees
Capacitive Load	1750 fF	500 fF	500 fF
Slew Rate (average)	26.7 [V/ μs]	625 [V/ μs]	1250 [V/ μs]
Input Referred Noise* (1Hz – 250 MHz)	N/A	36.2 μV_{rms}	40.8 μV_{rms}
1% Settling Time	\cong 100 ns	2.5 ns	1.8 ns
HD3 (Fin = 500 MHz) Vout = 1V _{pk-pk}	N/A	- 45.25 dB	- 55.73 dB
Max Frequency Providing the 8-bit Output Linearity	\cong 40 MHz	400 MHz	780 MHz
FoM ((V/ μs)pF/mA)	137.6	125	208.33

* Simulation Results

5. A LOW-POWER SLEW-RATE BOOSTING BASED 12-BIT PIPELINED ADC UTILIZING FORECASTING TECHNIQUE IN THE SUB-ADCS

5.1. Introduction

Pipelined analog-to-digital converters (ADCs) have been utilized to achieve high-speed high-resolution in Nyquist-rate data converters. Pipelined ADCs with sampling rates in the range of several hundreds of MS/s are widely used in broadband communication receivers, radar systems, digital wireless, and wired communication systems, including fifth-generation mobile networks (5G) and data-over-cable service interface specifications (DOCSIS). Although pipelined ADCs offer high sampling rates and high bandwidths, they usually demand high power consumption, which results in limited power efficiency.

There has been a trend for high resolution ADCs to use the SAR-assisted pipelined architecture to achieve better power efficiency. This architecture combines two moderate-resolution successive approximation register (SAR) ADCs with an inter-stage residue amplifier [63]–[68]. Thus, it benefits from employing a high-energy efficient SAR ADC as the sub-ADC in the pipelined stages. This architecture allows a higher first-stage resolution by utilizing only one comparator instead of implementing $2^{(M+1)}-2$ comparators per stage used in the conventional $M+0.5$ bits pipelined stage. However, this architecture suffers from a limited sampling speed due to its slow sub-ADC, which is an inherent cyclic SAR ADC. To alleviate this issue, a greater portion of the clock period time is devoted to the sub-ADC conversion phase [65]–[69]. On the other hand, a smaller portion of clock

period time remains for the sampling and settling phase, which results in more design constraints and a higher power consumption for both the preceding filter and the residue amplifier inside the stage. Although time-interleaved SAR-assisted pipelined ADCs with higher sampling rates have been reported recently [68]–[72] the gain and offset mismatches and the time skews among each sub-ADC, especially close to the Nyquist frequency, are still technologically challenging for designers. To alleviate this problem, a large differential input swing about two times larger than the supply voltage was applied to the SAR-assisted pipelined ADC [63], [65], and [67]. But this strategy is not feasible for low supply voltage systems where the preceding stage cannot provide such a highly linear and large input signal swing to the ADC. Also, implementing small unit capacitor demands for deploying mismatch calibration schemes result in extra circuitry, extra power, and lengthy start-up time. Furthermore, SAR-assisted pipelined architecture requires several clock phase signals with a frequency that is many times greater than the ADC sampling frequency which leads to a complex clock signal generator circuitry with considerable power dissipation.

Utilizing the fastest flash ADC as the sub-ADC in the pipelined stages, minimizes the devoted sub-ADC's conversion time and enables implementing high-resolution and high-sampling-rate pipelined ADCs [7], [10]. However, this architecture offers a poor figure of merit (FOM) if based on one conversion bit per stage because of residue amplifiers' high-power consumption [4], [73], [74]. If minimum total required transconductance for realizing a set number of bits for the pipelined ADC is considered, the multi-bits pipelined stage would show better power efficiency when the number of conversion bits per stage

increases [61]. On the other hand, conventional multi-bit ($M+0.5$ bits) for a pipelined stage requires $2^{(M+1)}-2$ comparators in its sub-ADC that drastically increases the power consumption and area, especially when $M > 3$. Also, by increasing the number of bits per stage, each comparator is required to increase its accuracy, which leads to higher power and a higher area. In addition, the residue amplifier used in the high-speed multi-bits pipelined stage needs to satisfy a high slew rate in order to decrease the slewing time and allocate more time for the linear settling phase. Under regular conditions, increasing the slew-rate requires a large static current available at the amplifier's output to efficiently drive the feedback and load capacitance from the next pipelined stage. The high output current demanded by the residue amplifier drastically increases ADC's static power consumption.

In this section, we propose a low-power, high-speed, 12-bit pipelined ADC architecture based on a class-B slew-rate boosting technique in the class-AB residue amplifiers to reduce static power, and a forecasting technique in the sub-ADC to minimize static power consumption. First, this work compares the most power-efficient 12-bit pipelined architectures based on the required transconductance gain for different architectures considering the minimum unit capacitor for avoiding capacitive mismatch calibration. Moreover, to achieve high-speed operation with a low-power residue amplifier, a class-B slew-rate boosting technique that generates high dynamic current is introduced. This concept decreases the residue amplifier's static power consumption by more than 38%. In addition, the novel forecasting technique in the sub-ADC reduces the number of active comparison cells during the sub-ADC conversion phase without

reducing the portion of the sampling and settling phase in the timing diagram of the pipelined stage. By employing this technique, the sub-ADC's power dissipation is reduced by more than 40% compared to the conventional sub-ADC implementation. The prototyped pipelined ADC was implemented in the 40 nm TSMC CMOS technology and achieves a Walden FOM of 27.7 fJ/conversion-step when operating around the Nyquist rate at a 500 MS/s sampling rate.

5.2. Forecasting Technique for Reducing the Number of Active Comparison in Pipelined Stages

The settling phase in the switched capacitor circuits consists of two parts, the slewing phase and linear settling phase as shown in Fig. 5.1. These two phases can be considered as coarse settling and fine settling phases. Notice that the sign of the amplifier's output can be detected after its coarse settling as shown in Fig. 5.1. The proposed forecasting technique exploits the settling behavior of SC circuits. The detection of the sign of the amplifier's residue is determined around the middle of the evaluation phase. Once the sign of the signal is identified, the signal is then routed to the group of comparators that process either the positive or the negative signals. As a result, half of the total dynamic power consumption is saved since half of the comparators are turned OFF during each comparison cycle; these concepts are illustrated in the Fig. 5.2, 5.3, and 5.4. No extra time is needed for the sub-ADC phase because: i) the loading during the first half of the evaluation phase is drastically reduced since only the sign comparator is connected, and ii) once the signal sign is identified, only 50% of the comparators are connected to the

amplifier's output.

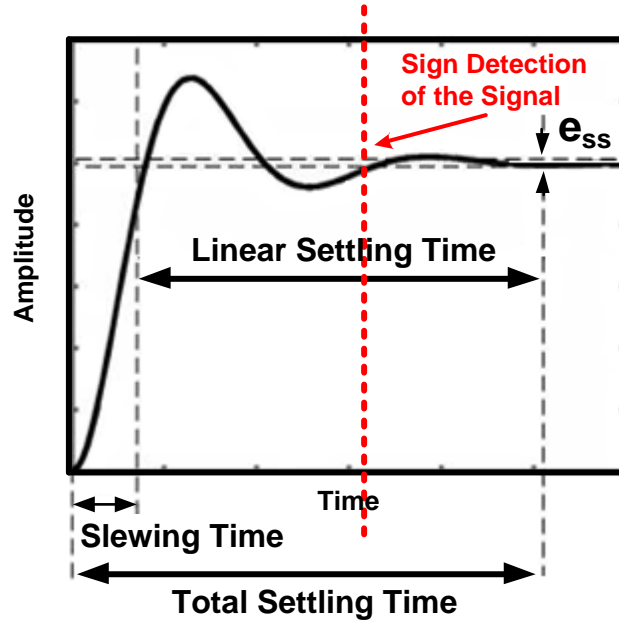


Fig. 5.1. Typical pulse response of the second order system detecting the sign of the output signal at the middle of the settling of the SC circuits in the proposed forecasting technique.

To implement the proposed concept, an extra comparator was employed to detect the sign of the input signal at the middle of the settling phase of the preceding stage's residue amplifier. If the sign comparator's output is high, all the comparators connected to the negative voltage references are not connected to the amplifier's output. On the other hand, if the sign comparator's output is negative, all the comparators attached to the positive reference voltages are disabled. Fig. 5.4 shows the details of the implementation of this forecasting technique. The sign detection is performed by an extra comparator during the settling phase of the residue amplifier. The sign detector output is ready before the end of

the linear settling phase and is driving by phase PHIX. Once the sign is detected, the clock that drives the dynamic comparators is enabled for the set of comparators that complete the analog-to-digital conversion.

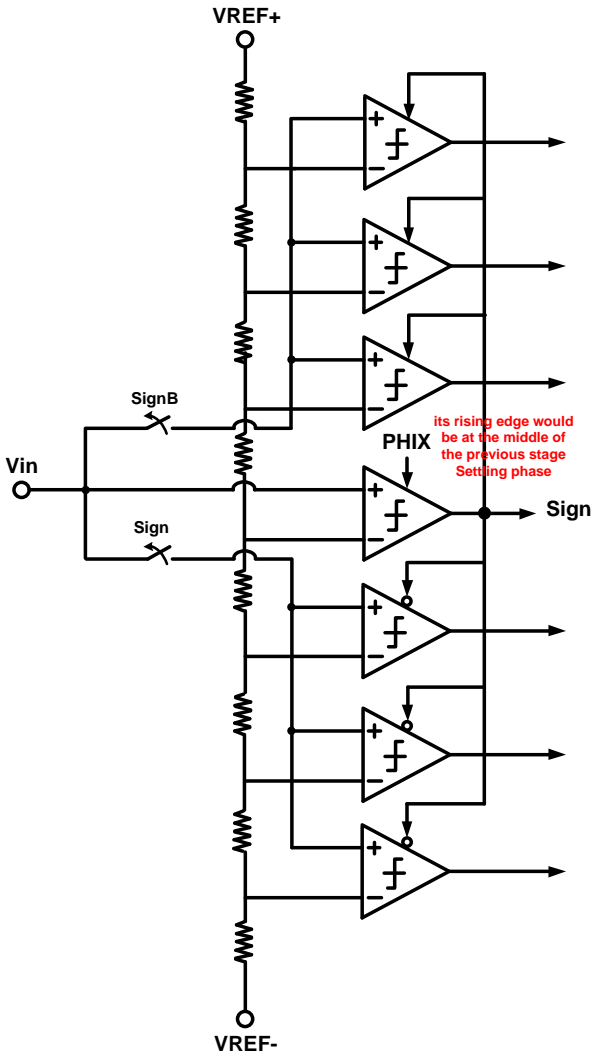


Fig. 5.2. Implementation of activation of required the Sub-ADC's comparators by forecasting the sign of the sampled input voltage by utilizing the nature of settling waveforms in SC residue amplifiers.

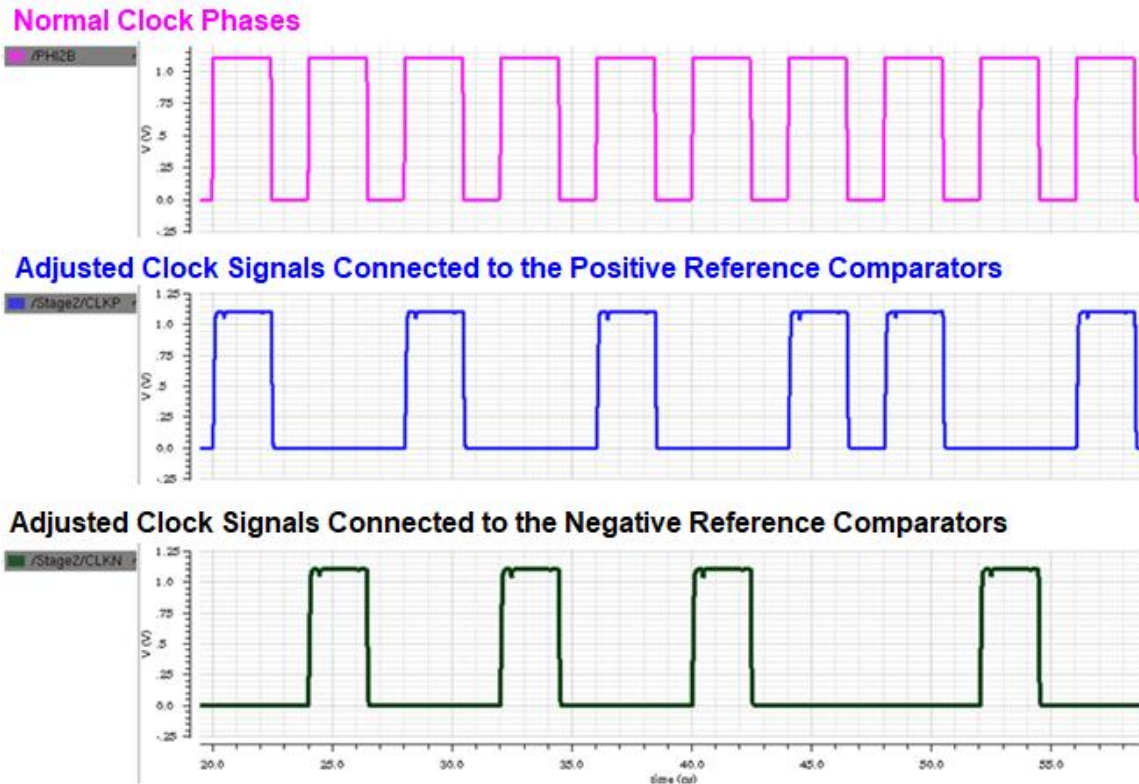


Fig. 5.3. Adjusted clock signals for negative/positive reference voltage connected comparators based on the sign of the input signal.

Notice that the residue amplifier drives the next stage unit capacitors and the load capacitance due to the next stage sub-ADC. The conventional $M+0.5$ -bits pipelined stage requires $2^{(M+1)}-2$ comparators in its sub-ADC, which drastically increases the load capacitance from the sub-ADC to the preceding pipelined stage. The forecasting technique mitigates this issue and decreases the load capacitance from the next stage's sub-ADC. Therefore, dynamic power is saved since the loading for previous residue amplifier design is relaxed.

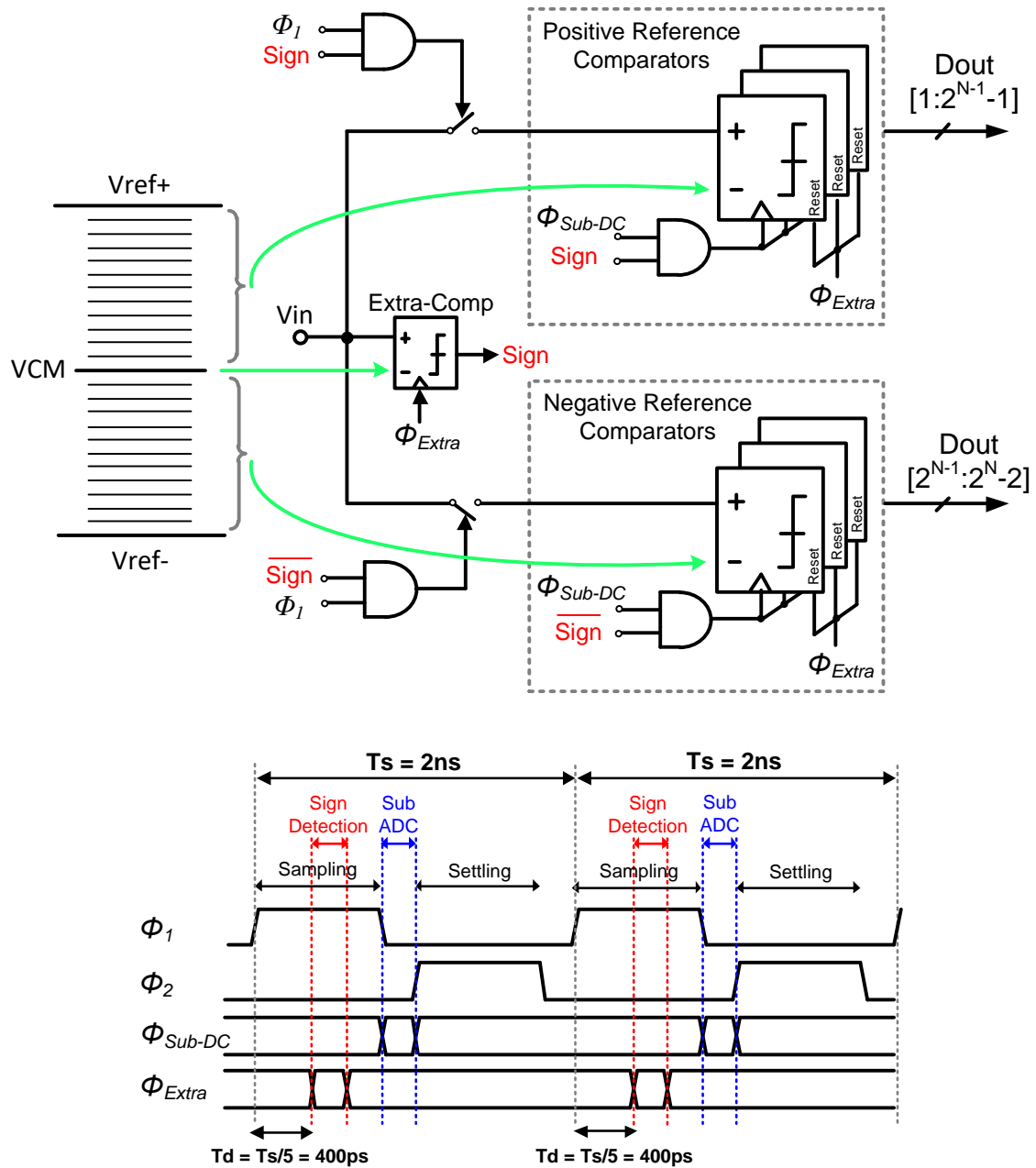


Fig. 5.4. Implementation of the proposed forecasting technique in the sub-ADC for the case of N bits pipelined stage.

5.3. Circuit Implementation

5.3.1. Proposed Architecture

As mentioned in section 3, the cascade connection of the 3.5-bit pipelined stages is one of the most power-efficient architectures when implementing high performance mismatch calibration-free pipelined ADC. The overall power consumption is further optimized by cascading two 3.5-bit pipelined stages followed by a 6-bit Flash ADC, which employs the forecasting technique; Fig. 5.5 shows the proposed architecture. In this architecture, almost half of the comparators remain disabled during each comparison cycle, which leads to power savings of almost 50% in the design of the flash ADC.

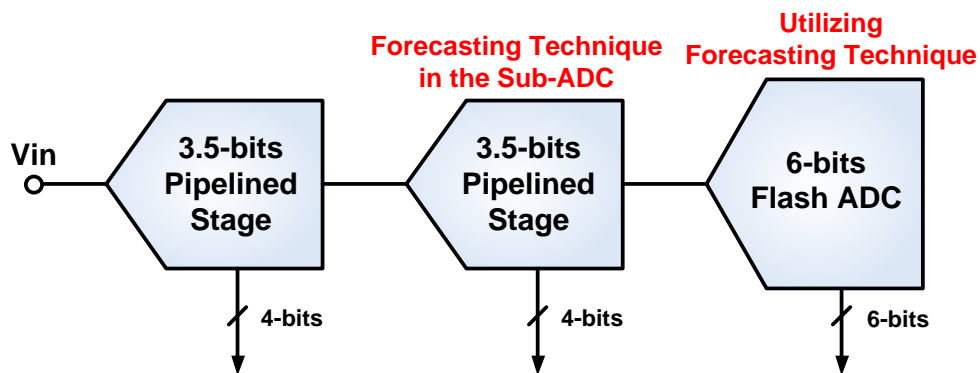


Fig. 5.5. Proposed power efficient high speed 12-bit pipelined ADC employing two 3.5-bit/stage pipeline stages and a 6-bit flash.

5.3.2. Residue Amplifier

To achieve superior static power efficiency, single-stage op-amps with low dc-gain

are employed in [75] and [76]. Since the $M+0.5$ -bits pipelined stage is utilized as the 1st stage in [75] and [76], the first stage output swing shrinks as follows.

$$V_{OUT} = \frac{\frac{1}{\beta}}{1 + \frac{1}{\beta A}} V_{IN} \quad (5.1)$$

where A is the gain of the residue amplifier and β is the feedback factor of the $M+0.5$ -bits pipelined stage, which is equal to $\frac{1}{2^M}$. Therefore, the expression for the gain stage can be computed as follows:

$$V_{OUT} = \left(\frac{2^M}{1 + \frac{2^M}{A}} \right) V_{IN} = \left(1 - \frac{\frac{2^M}{A}}{1 + \frac{2^M}{A}} \right) (2^M \cdot V_{IN}) \quad (5.2)$$

$$Error = \frac{\frac{2^M}{A}}{1 + \frac{2^M}{A}} \quad (5.3)$$

Eq. (5.2) demonstrates that more conversion bits in a pipelined stage requires a higher gain from the residue amplifier to maintain the residue amplifier's accuracy. From (5.2), we can conclude that the gain stage is drastically affected when loop gain $A/2^M$ is limited [75], [76]. Even if corrected in the digital form, the analog residue output reduces to half while the thermal noise is kept at the same level. This results in a reduction of the signal power-to-thermal noise power ratio. In addition, more conversion bits per pipelined stage

requires a higher loop gain from the residue amplifier to maintain the required accuracy and linearity. Loop gain reduces drastically (even close to unity) in the case of single-stage amplifiers in multi-bits stage; e.g., $M = 4$ (feedback factor = -24 dB) and amplifier gain ($A=30$ dB) leads to a loop gain of only 6 dB. As a result, the architecture does not take full advantage of the properties of linear feedback systems; e.g., large linearity, high accuracy and immunity to nonlinear parasitic capacitors. Even if the magnitude errors are corrected in the digital domain, pipelined ADC linearity is drastically affected due to the limited loop gain. Eq. (5.3) represents the relative error due to the finite residue amplifier gain in a $M+0.5$ -bits pipelined stage. Furthermore, finite residue amplifier dc-gain results in non-virtual ground at the amplifier's input nodes which leads to high sensitivity to nonlinear parasitic capacitors. Table 5.1 shows the amount of error in percent for a residue amplifier with the different finite gain of 30 dB and 60 dB in a $M+0.5$ -bits pipelined stage.

Table 5.1: Error in percent for a residue amplifier with different finite gain in a $M+0.5$ -bits pipelined stage

Amplifier DC-Gain	M	Error
60 dB	1	0.199%
	2	0.398%
	3	0.793%
	4	1.574%
30 dB	1	5.948%
	2	11.229%
	3	20.191%
	4	33.598%

For large loop gain, the telescopic architecture is also attractive, but it may not be suitable for high resolution ADCs realized in deep submicron technologies due to the significant voltage headroom needed for the operation of five transistors allocated between the VDD and ground and operating in a linear regime. In this design a two-stage pseudo class AB amplifier (class-A cascaded with class-AB) was chosen as the main amplifier; the amplifier is shown in Fig. 5.6. The first stage, composed of transistors M1, M3, M5, and M7, achieves high gain due to the cascode nature of its components; this is indeed a first stage cascode amplifier. R1 resistors are used to set the bias point without the need of a CMFB circuit. The first stage is DC coupled to the P-type second stage (transistors M9), while AC is coupled to the N-type amplifier, which is realized through transistor M11. The AC connection through C_B boosts the high-frequency AC transconductance by around 6 dB. This signal path enables the architecture to operate as a true class-AB amplifier with ability to sink and deliver large amounts of output current improving its power efficiency.

The amplifier's targeted specifications are: DC gain > 48 dB and GBW > 3.6 GHz. The transconductance requirement can be satisfied by delivering enough current at the input transistor's small signal behavior; thus, 2.5 mA at the tail current in the first stage is employed. The output stage of the main amplifier is designed to provide the maximum signal swing; then, cascode transistors are not used. Modest dc-current (0.5 mA) is used at the output stage just to provide enough small signal transconductance; its class-AB nature can deliver large amounts of dynamic current. Miller compensation through C_z and R_z is used. Thus, the dominant pole is placed at the amplifier's first stage output node. Table 5.2 shows the amplifier device sizes including dimensions and bias conditions.

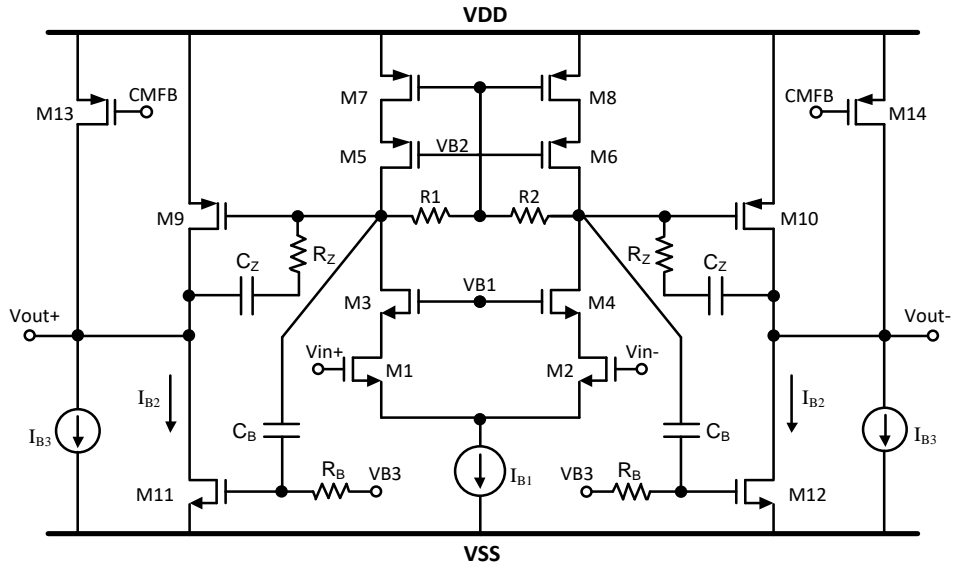


Fig. 5.6. The low-power, high-performance pseudo Class AB architecture utilized as the residue amplifier in the 3.5-bit pipelined stage.

Table 5.2: Residue amplifier device sizes

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)	Drain Current (μA)
M1-M2	60/0.08	1250
M3-M4	45/0.12	1250
M5-M6	90/0.08	1250
M7-M8	90/0.12	1250
M9-M10	32/0.06	500
M11-M12	14/0.06	500
Component		Value
R_B		20 K Ω
C_B		200 fF
R_Z		500 Ω
C_Z		100 fF

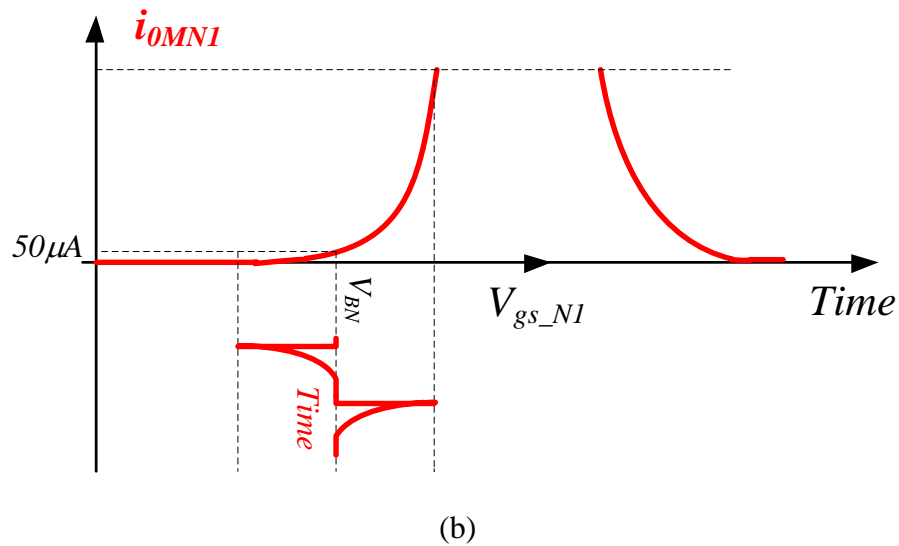
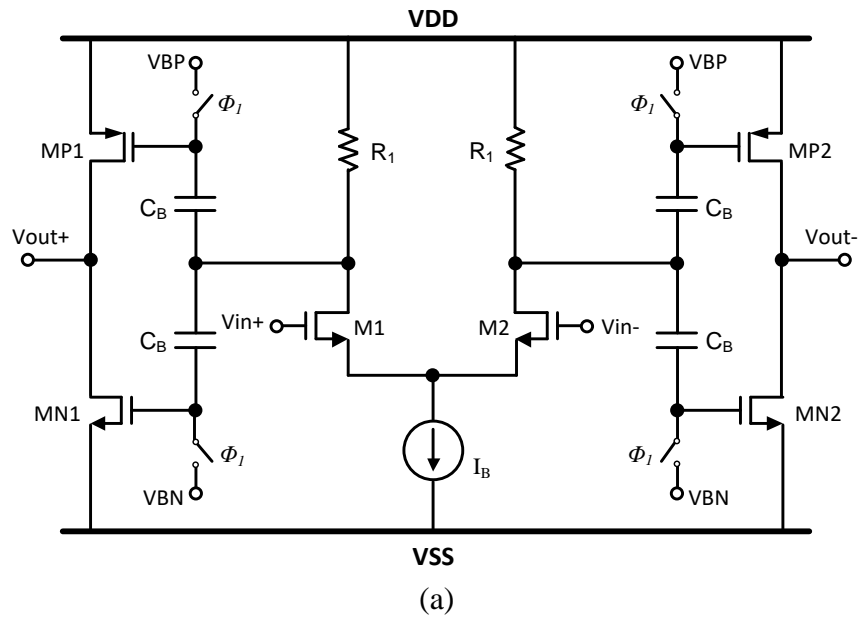


Fig. 5.7. Auxiliary circuit for boosting the slew rate in the 3.5-bit pipelined stage: a) simplified schematic and b) operating point and functionality of Class B output stage: drain current of transistor MN1.

5.3.3. Slew-Rate Booster

The slew rate boosting auxiliary circuit employs simple circuitry to detect the need for injecting high-dynamic current at the output load by implementing a pre-amp followed by a Class-B amplifier, as the simplified schematic is shown in Figure 5.7a. A high-speed pre-amp amplifies the error signal present at the input of the main amplifier during the settling phase and then increases the sensitivity of the class-B output stage (MN1 and MP1); this circuit is designed to give an exceptionally fast performance, with a -3 dB frequency over 1 GHz. The class-B output stage operates in a subthreshold region to reduce power consumption during the sampling phase by connecting the gate of the MN1 and MP1 transistors to the reference voltages VBN and VBP, respectively. The C_B capacitors are precharged during the main amplifier's sampling phase (ϕ_1) to set the output stage bias conditions. The bias voltages VBN and VBP are set to enable the slew-rate booster circuit operation when the differential input signal is higher than 20 mV; this scenario is illustrated in Fig. 5.7b for the case of transistor MN1. It is bias at the onset of its subthreshold region, but it can provide up to five times the main amplifier output current when operating in slew mode and in the presence of large signal excursions. The tail current of the pre-amp in the slew-rate booster is set at 0.4 mA; this current is relatively small when compared to the 2.5 mA DC current used in the main amplifier's first stage.

In Fig. 5.7a, the in-band gain of the first stage is set at 8V/V, and the -3 dB bandwidth is over 1 GHz; then, it settles within an error under 0.2% in less than 1 nsec; therefore, settling time is not limited by the internal pole of the slew-rate booster. The input capacitance of the pre-amp is around 15 fF, which is small compared to the main

amplifier's 65 fF input capacitance. This additional capacitance does not have a major effect on loop-gain bandwidth or on the main amplifier's settling time. Table 5.3 displays the dimensions and bias conditions for the relevant transistors and component values. The overhead power consumption is 0.55 mW due to this auxiliary circuit, which is only 20% of the main amplifier power consumption.

Table 5.3: Slew-rate booster device sizes

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)	Drain Current (μA)
M1-M2	6.4/0.08	200
MN1-MN2	20/0.06	50
MP1-MP2	40/0.06	50
Component		Value
R_1		2.25 k Ω
C_B		500 fF

5.3.4. Comparator

Fig. 5.8 shows a double tail sense amplifier [77] that employed as comparator in the sub-ADC design. This comparator utilizes one tail for the input stage and another tail for the latching stage [77]. In comparison to strong-arm comparator design, this architecture offers less transistor stacking [77]. Therefore, it can operate very well under low supply voltages. In addition, while the input transistors biased with small current for achieving low offset, large current can be employed in the latching stage in the order to reach fast

latching independent of input transistor bias current or common mode voltage [77]. As a result, the double tail sense amplifier in Fig 5.8 enables the comparator design to have more degrees of freedom in optimizing speed, offset, power consumption, and common-mode voltage [77].

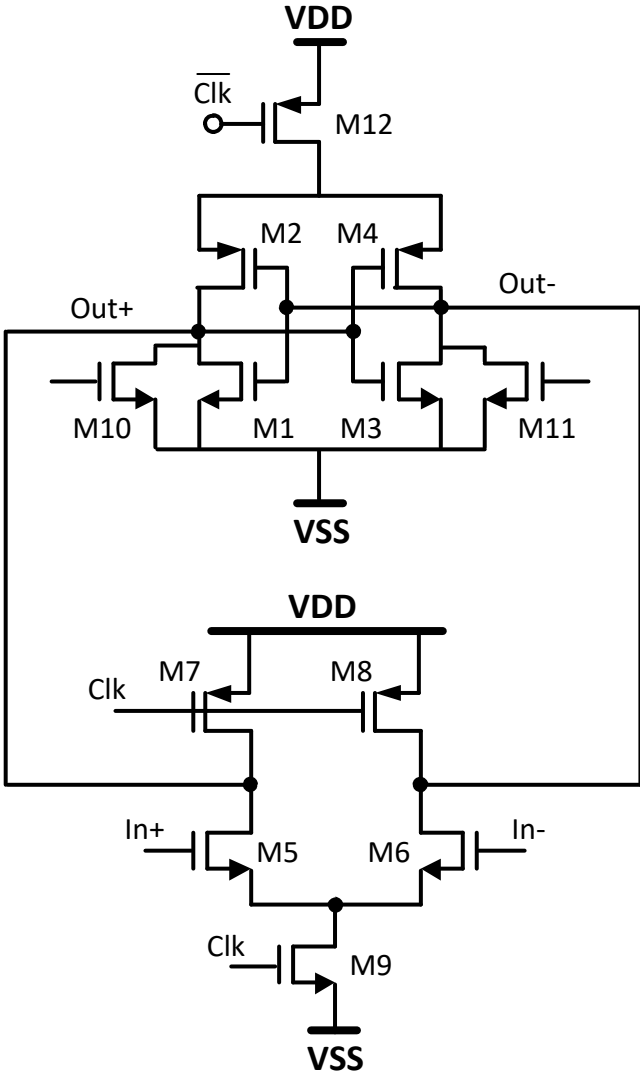


Fig. 5.8. Double-tail sense amplifier utilized as comparator in sub-ADC [77].

5.4. Experimental Results

The proposed 12-bit pipelined ADC is fabricated in the TSMC 40 nm CMOS process using core devices with a nominal DC supply of 1.1 V. Fig. 5.9 shows the die photo of the ADC, where the core occupies 0.9 mm². Every four digital output bits of each sub-ADC output were combined on-chip and captured by a fast oscilloscope. An Agilent E8267D PSG vector signal generator was used to supply the input signal and the output codes were captured using an Agilent Infiniium DSA91304A oscilloscope. The output codes were then imported into MATLAB where the first-order gain calibration process was performed as it is shown in Fig. 5.10. This first-order calibration was based on multiplying the output of each stage with a coefficient that represents the finite gain calibration for the preceding stages' residue amplifiers of as follows.

$$D_{i,cal} = D_i \times \prod_{j=1}^{i-1} \left(1 + \frac{2^{M_j}}{A_j}\right) \quad (5.4)$$

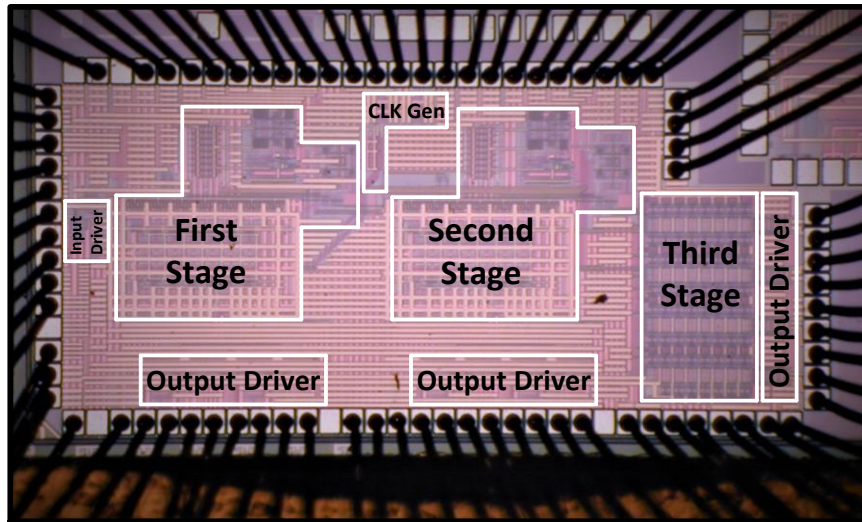


Fig. 5.9. Chip micrograph.

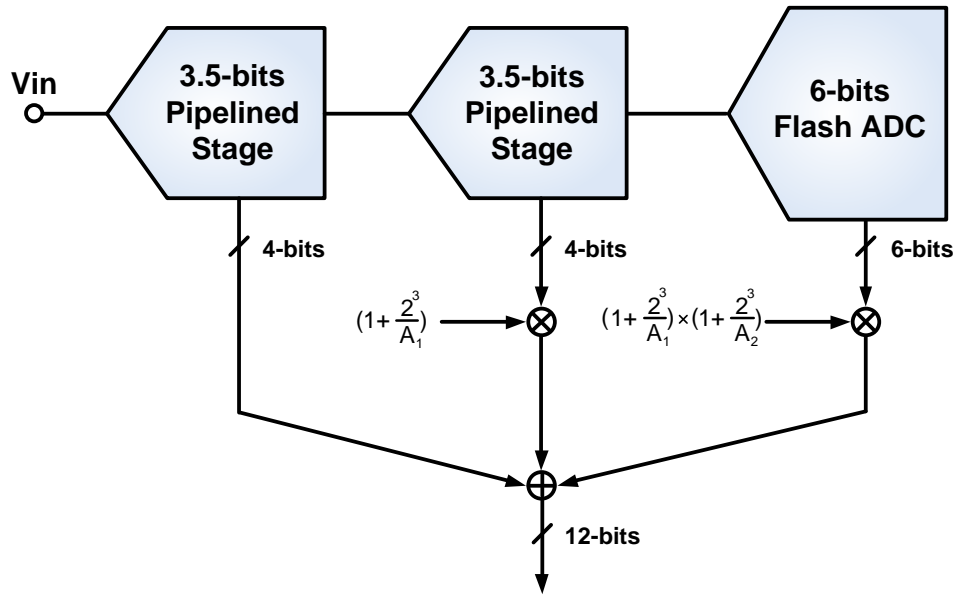


Fig. 5.10. Calibration scheme.

where D_i corresponds to the output code of each stage; M_j and A_j represent the number of converted bits per stage and the finite residue amplifier gain of the i_{th} stage, respectively. Bootstrap switches are utilized in the first two pipelined stages to keep constant the switch resistance and to minimize the input-signal-dependent sampling nonlinearities. Large on-chip bypass capacitors are used to stabilize the supply and reference voltages.

Fig. 5.11 shows the measured spectra of ADC output before and after gain calibration; these results were obtained for an input tone set at 24.95 MHz. The inter-stage gains errors due to the finite gain of the amplifiers, and capacitor mismatches generate several harmonic distortion components that limit the ADC's SNDR and SFDR to 51.51 dB and 54.15 dB, respectively. After calibration the measured SNDR and SFDR were 65.31 dB

and 75.59 dB, respectively. The power of the third harmonic distortion component is under -75 dB, and a reduction of close to 20 dB was obtained after calibration.

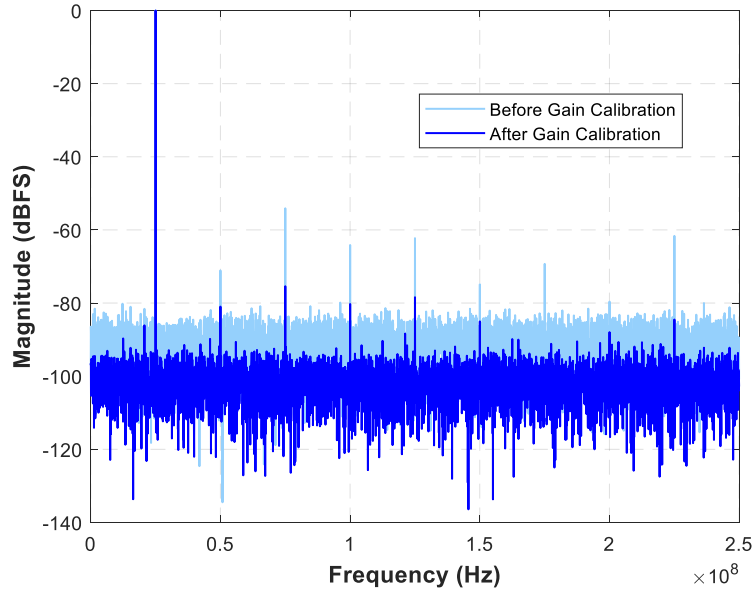


Fig. 5.11. Measured spectra with sinusoidal input at 24.95 MHz before and after gain calibration.

Fig. 5.12 shows the dynamic performance of the pipelined ADC versus the frequency of the single tone input signal; the sampling frequency is set at 500 MHz and 10k samples were recorded. The SNDR is around 65.5 dB when measured at low-frequency, and it decreased to 64.5 dB when measured close to the Nyquist frequency. The SFDR is over 75 dB for the entire ADC band. The sampling frequency was swept up to 600 MHz maintaining the frequency of the input tone at 4.15 MHz; the results are shown in Fig. 5.13. The SNDR is over 65dB until 500 MS/sec and drops down to 64 dB near 600 MS/sec.

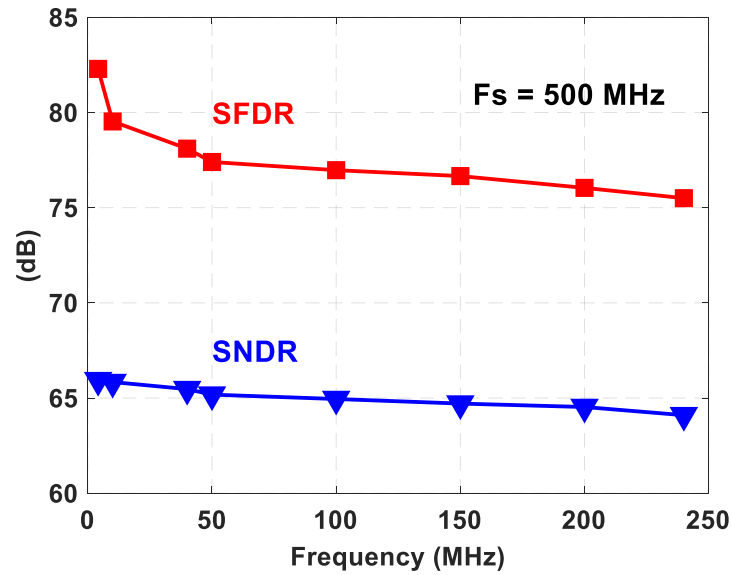


Fig. 5.12. SNDR and SFDR as function of the input frequency measured with a sampling frequency set at 500 MHz.

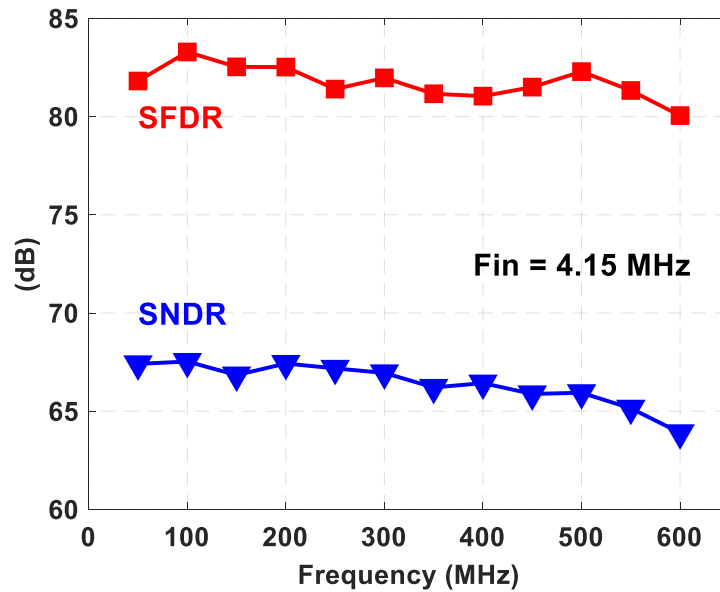


Fig. 5.13. SNDR and SFDR versus sampling frequency when the frequency of the input signal is set at 4.15 MHz.

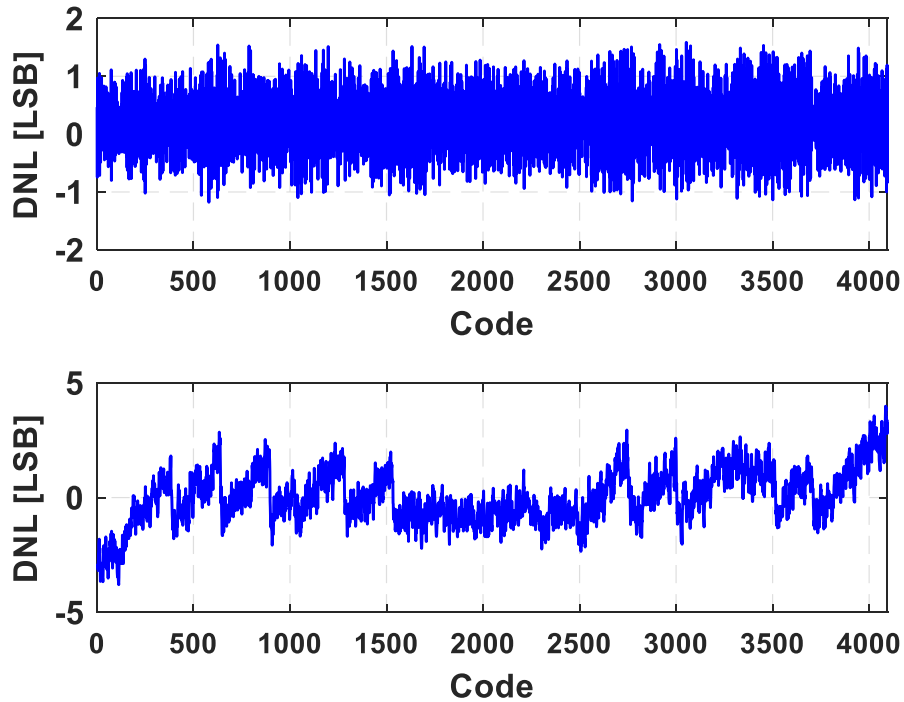


Fig. 5.14. Measured DNL and INL before gain calibration.

Fig. 5.14 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) profiles before calibration, which are $+1.58/-1.17$ LSB and $+3.97/-3.79$ LSB, respectively. The INL exhibits a slope pattern indicating that the intrinsic conversion nonlinearity depends on the finite gain of residue amplifiers. Fig. 5.15 illustrates the DNL and INL after gain calibration in the digital domain. The DNL is now limited to $+0.41/-0.42$ LSB, and the INL reduces to $+0.82/-0.73$ LSB.

Table 5.4 shows the power consumption breakdown of the proposed 12-bit pipelined ADC and that of a conventional 12-bit pipelined ADC, both running at a 500 MS/s conversion rate. The proposed amplifier with slew-rate boosting reduces the total power

consumption by more than 40%. Also, utilizing the forecasting technique decreases the power consumption of the 6-bit flash ADC by around 46%. At 500 MS/s, the overall measured power consumption of the proposed ADC is 18.16 mW; 51% of the total power is consumed by the residue amplifiers. Table 5.5 shows a comparison between the prototype ADC and other pipelines as well as the pipelined-SAR ADCs. The proposed architecture achieves high resolution and background calibration-free operation simultaneously even under process, temperature and power supply variations. The proposed ADC architecture shows competitive power efficiency, even though it is not implemented in the most advanced technology node.

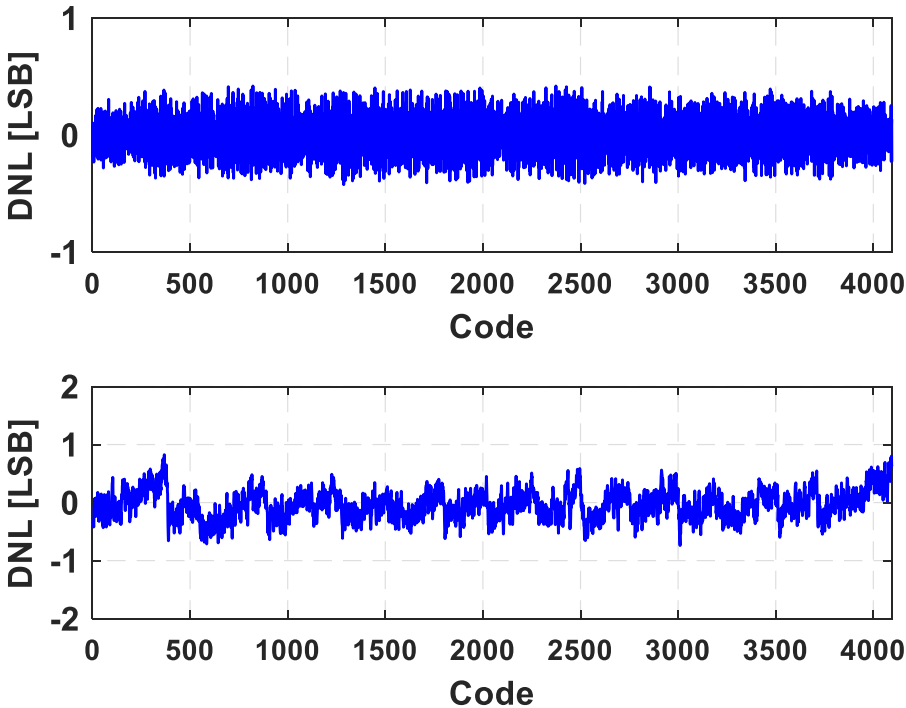


Fig. 5.15. Measured DNL and INL after gain calibration.

Table 5.4: Power consumption breakdown of the presented 12-bit pipelined ADC

ADC Type	1 st Stage Residue Amplifier	1 st Stage sub-ADC	2 nd Stage Residue Amplifier	2 nd Stage sub-ADC	3 rd Stage 6-bit Flash ADC	Total Power Consumption
Conventional Design	8.25 mW	2.32 mW	7.5 mW	2.49 mW	8.25 mW	28.81 mW
Proposed Techniques	5.63 mW	2.32 mW	3.77 mW	2.01 mW	4.42 mW	18.15 mW

According to Table 5.5 and Table 5.6, this design achieves a very competitive conversion accuracy and FOM among the most efficient reported pipelined ADCs. The SAR architectures show the lowest power consumption; however, usually their performance without calibration is not quite competitive; e.g. DNL and INL over 40 LSBs and 100 LSBs, respectively, are reported in [68]. The proposed architecture achieved the second best FOM and the best SNDR achieved due to proper selection of ADC architecture and because of the proposed techniques aimed to reduce the power consumption of the residue amplifier and sub-ADC.

5.5. Conclusion

A 12-bit 500-MS/s pipelined ADC fabricated in the 40-nm TSMC technology is presented in this section. The power-efficient 12-bit pipelined architecture was chosen based on the minimum total required transconductance among different architectures. The presented ADC employs a novel class-B slew-rate boosting technique to save power in the residue amplifiers, and still provides superior slew-rate performance. Also, a forecasting technique in the sub-ADC is proposed which reduces the number of active

comparison cells during the sub-ADC's evaluation phase without affecting the sampling/settling phase of the pipelined stage. The proposed concepts help to reduce the static current of the residue amplifiers by more than 40% and reduced the dynamic power dissipation of the sub-ADCs by more than 46%. Measured results reveal an SNDR/SFDR of 65.94 dB and 82.29 dB for a 4.15 MHz sinusoidal input 64.10 dB and 75.51 dB close to the Nyquist rate. In both cases, the ADC operated at 500 MS/sec. The ADC core occupies a 0.9 mm² chip area and a consumption power of 18.16 mW. The proposed ADC architecture achieves an FOM of 27.7 fJ/conversion-step when measured at Nyquist frequency.

Table 5.5: Performance summary and comparison I

	This Work	[1]	[2]	[10]	[11]	[66]	[68]
Architecture	Pipelined	Pipelined Current Mode MDAC	Pipelined Ring-Amp Based RA	Pipelined Charge-Steering RA	Pipelined Ring-Amp Based RA	Pipelined SAR	Pipelined SAR
Technology (nm)	40	40	28	65	65	28	65
Resolution (bit)	12	13	12	10	10.5	10	12
Sampling Rate (MS/s)	500	200	600	800	100	500	180
Supply Voltage (V)	1.1	1/1.8	0.9	1	0.75/1.2	1.0	1.2
Power (mW)	18.15	8.4	14.2	19	2.46	6	6
SNDR@Low Freq (dB)	65.94	58.4	58.1	56.9	57.9	56.7	63.8
SFDR@ Low Freq (dB)	82.29	75	67.5	N/A	71.9	73.1	76.3
SNDR@Nyquist (dB)	64.10	57.6	56.3	52.2	56.6	56.6	60.92
SFDR@Nyquist (dB)	75.51	72	69.2	N/A	64.7	69.2	67
FOM @ Low freq (fJ/conv.step)	22.41	61.82	36.04	53	38.4	21.47	26.3
FOM@Nyquist (fJ/conv.step)	27.71	64	44.3	71	44.5	21.7	36.7
Area (mm ²)	0.9	0.23	0.62	0.18	0.097	0.015	0.068

Table 5.6: Performance summary and comparison II

	This Work	[4]	[14]	[78]	[79]	[80]
Architecture	Pipelined	Pipelined Integrating-Amp Based RA	Pipelined SAR	Pipelined Ring-Amp Pipelined SAR	Pipelined Combining Flash and TDC	Pipelined Ring-Amp Based RA
Technology (nm)	40	28	65	28	28	28
Resolution (bit)	12	14	11	12	8	12
Sampling Rate (MS/s)	500	280	1000	800	900	1000
Supply Voltage (V)	1.1	1	1.2/2	1	1	0.9
Power (mW)	18.15	13.0	230	20.2	3.5	24.8
SNDR@Low Freq (dB)	65.94	65.50	59.1	63.03	43.3	57.1
SFDR@ Low Freq (dB)	82.29	81.0	67.0	79.0	51.6	74.6
SNDR@Nyquist (dB)	64.10	64.0	56.0	61.4	41.9	56.6
SFDR@Nyquist (dB)	75.51	77.0	60.5	75.2	49.5	73.1
FOM @ Low freq (fJ/conv.step)	22.41	30.3	312.4	21.88	32.0	42.46
FOM@Nyquist (fJ/conv.step)	27.71	35.8	449.2	26.40	37.0	45.0
Area (mm ²)	0.9	0.22	2.5	0.175	0.029	0.54

6. CONCLUSION AND RECOMMENDATION FOR FUTURE WORKS

In this dissertation, power-efficient architectures and circuit solutions to improve the power efficiency of high-speed 12-bit pipelined ADCs in advanced CMOS technologies are presented. The 4.5-bit algorithmic pipelined front-end stage is proposed. It is shown that the algorithmic-pipeline topology presents very competitive power efficiencies and low sensitivity to the MDAC errors while requires less area and less power dissipation in the sub-ADC. Also, the calculation for the minimum total required transconductance for the different architectures of 12-bit pipelined ADC is proposed. These calculations are performed for different capacitive scaling ratios between consecutive pipelined stages and considering the minimum unit capacitance in pipelined stage to avoid mismatch. This study helped us to find the most power-efficient 12-bit pipelined architecture between different topologies for the same input-referred thermal noise.

A slew-rate boosting technique based on the generation of high dynamic current when fast response is demanded is presented. The proposed concept relies on monitoring the amplifier's input stage, employing a low-power single-stage ultra-fast preamplifier to detect the need for a higher current to boost the amplifier's slew-rate. Preamplifier output is used to drive a class-B amplifier with controlled hysteresis that can generate up to three times the current delivered by the main amplifier. Static power overhead is no more than 20%, and the noise level increases by 1dB; effects on input capacitance are negligible. The auxiliary circuit extends the frequency range of a 4.5 bit/stage residue amplifier from 400 MHz (core bandwidth) up to 780 MHz while maintaining the third harmonic distortion

around -48 dB.

By employing the above ideas, a 27.7 fJ/conv-step at Nyquist 500 MS/s 12 -bit pipelined ADC based on a class-B slew-rate boosting technique in the residue amplifiers to reduce static power, and a forecasting technique in the sub-ADC to minimize static power consumption is designed and implemented. A novel forecasting technique in the sub-ADC is proposed, which reduces the number of active comparison cells during the sub-ADC conversion phase without reducing the portion of the sampling and settling phase in the timing diagram of the pipelined stage. By employing this technique, the sub-ADC's power dissipation is reduced by more than 40% compared to the conventional sub-ADC implementation. The prototyped pipelined ADC achieves an SNDR/SFDR of $65.9/82.3$ dB at low input frequencies and a $64.1/75.5$ dB near Nyquist frequency while running at 500 MS/s. The pipelined ADC prototype occupies an active area of 0.9 mm² and consumes 18.16 mW from a 1.1 V supply, resulting in a figure of merit (FOM) of 22.4 and a 27.7 fJ/conversion-step at low-frequency and Nyquist frequency, respectively.

Although different new techniques are proposed which reduced the total power consumption of implemented 12 -bit pipeline ADC, new technique can be utilized to reduce the total area of the pipeline ADC. In this prototype, instead of inactivating and disconnecting the sub-ADC's comparators by forecasting the sign of the sampled input voltage in pipeline stages, a new sub-ADC can be employed which contains half number of required comparators inside a conventional M -bit sub-ADC that sweeps their reference voltages by output of the sign detection. In this solution, reference voltages of the comparators would have negative or positive orientation based on the sign bit. As a result,

not only about 50% power saving would be reached inside the sub-ADC, but also area shrinking about 50% would be achieved by utilizing the proposed technique.

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