ENERGY EFFICIENT WIRELESS CIRCUITS FOR IOT IN CMOS TECHNOLOGY

A Dissertation

by

OMAR ABDULMONEM MOHAMED ELSAYED

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Kamran Entesari
	Sunil Khatri
	Mahmoud El-Halwagi
Head of Department,	Miroslav M. Begovic

May 2019

Major Subject: Electrical Engineering

ABSTRACT

The demand for efficient and reliable wireless communication equipment is increasing at a rapid pace. The demand and need vary between different technologies including 5G and IoT. The Radio Frequency Integrated Circuits (RFIC) designers face challenges to achieve higher performance with lower power resources. Although advances in Complementary Metal-Oxide-Semiconductor (CMOS) technology has help designers, challenges still exist. Thus, novel and new ideas are welcome in RFIC design. In this dissertation, many ideas are introduced to improve efficiency and linearity for wireless receivers dedicated to IoT applications.

A low-power wireless RF receiver for wireless sensor networks (WSN) is introduced. The receiver has improved linearity with incorporated current-mode circuits and high-selectivity filtering. The receiver operates at a 900 MHz industrial, scientific and medical (ISM) band and is implemented in 130 nm CMOS technology. The receiver has a frequency multiplication mixer, which uses a 300 MHz clock from a local oscillator (LO). The local oscillator is implemented using vertical delay cells to reduce power consumption. The receiver conversion gain is 40 dB and the receiver noise figure (NF) is 14 dB. The receiver IIP3 is -6 dBm and the total power consumption is 1.16 mW.

A wireless RF receiver system suitable for Internet-of-Things (IoT) applications is presented. The system can simultaneously harvest energy from out-of-band (OB) blockers with normal receiver operation; thus, the battery life for IoT applications can be extended. The system has only a single antenna for simultaneous RF energy harvesting and wireless reception. The receiver is a mixer-first quadrature receiver designed to tolerate large unavoidable blockers. The system is implemented in 180 nm CMOS technology and operates at 900 MHz industrial, scientific and medical (ISM) band. The receiver gain is

41.5 dB. Operating from a 1 V supply, the receiver core consumes 430 μW. This power can be reduced to 220 μW in the presence of a large blocker ($\approx$ 0 dBm) by the power provided by the blocker RF energy harvesting where the power conversion efficiency (PCE) is 30%.

Finally, a highly linear energy efficient wireless receiver is introduced. The receiver architecture is a mixer-first receiver with a Voltage Controlled Oscillator (VCO) based amplifier incorporated as baseband amplifier. The receiver benefits from the high linearity of this amplifier. Moreover, novel clock recycling techniques are applied to make use of the amplifier's VCOs to clock the mixer circuit and to improve power consumption. The system is implemented in 130 nm CMOS technology and operates at 900 MHz ISM band. The receiver conversion gain is 42 dB and the power consumption is 2.9 mW. The out-of-band IIP3 is 6 dBm.

All presented systems and circuits in this dissertation are validated and published in various IEEE journals and conferences.

DEDICATION

To my mother, father, brothers, sister and beloved son, Yahya.

ACKNOWLEDGMENTS

First, I am thanking Allah the Almighty, the First, the Last and the capable over everything. Without his blessings and mercies, nothing can be done.

I am thankful for my advisor Prof. Edgar Sánchez-Sinencio, who helped and guided me throughout my work on this Ph.D. work. His knowledge, respect, vision, and encouragement were very essential and critical during my Ph.D. journey. I am really grateful for his support.

I am thankful to my Ph.D. committee members, Prof. Kamran Entesari, Prof. Sunil Khatri and Prof. Mahmoud El-Halwagi. Their help and suggestions are very appreciated.

I would like to thank my father and mother who are always standing behind me and supporting me. I ask Allah to give them the best in this world and hereafter. I would like also to thank my brothers and sister for their encouragement and support during my Ph.D. studies. I am thankful to my grandmother for her prayers and support. I am thankful to my little angel Yahya whose birth lightened and colored my life. I ask Allah to give him the best in this world and hereafter. To the memory of my grandparents.

I would like to thank my friends and work colleagues Mohamed Abouzied and Hatem Osman for their valuable discussion, comments and input.

I would like to thank my friends and colleagues at Texas A&M University in College Station. I would like to thank Ahmed Abdelraouf, Ahmed Bashirah, Ahmed Elsayed, Ahmed Rabea, Ahmed Salah, Amr Abuellil, Ayman Shafik, Bahaa Hafez, Bassem Zaki, Jorge Zarate, Joseph Riad, Mahmoud Elsabahy, Mohamed Elkholy, Mostafa Mosa, Osama Elhadidy, Sherif Shakib and Tarek Elgohary.

I would like also to thank my close friends Khaled Yehia, Mohamed Shehata and Omar Abdalla for their encouragement and support.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supported by a dissertation committee consisting of Professors Edgar Sánchez-Sinencio [advisor], Kamran Entesari, and Sunil Khatri of the Department of Electrical Engineering and Professor Mahmoud El-Halwagi of the Department of Chemical Engineering.

Part of the research in Section 2 was made by Jorge Edgar Zarate of the Department of Electrical Engineering. Part of the research in Section 3 was made by Mohamed Ali Abouzied of the Department of Electrical Engineering. The analysis depicted in Section 4 was made by Hatem Osman of the Department of Electrical Engineering.

All other work conducted for the dissertation was completed by the student independently.

Funding Sources

Graduate study was supported by a fellowship from Silicon Laboratories and Texas Instruments.

NOMENCLATURE

2G	Second-generation cellular technology
5G	Fifth-generation cellular technology
WiFi	Wireless Fidelity
IoT	Internet of Things
LNA	Low Noise Amplifier
VCO	Voltage Controlled Oscillator
OTA	Operational Transconductance Amplifier
ISM	Industrial, Scientific and Medical
WSN	Wireless Sensor Network
NF	Noise Figure
LPF	Low Pass Filter
TIA	Transimpedance Amplifier
k	Boltzmann Constant
γ	Excess Noise Factor
HD3	Third Harmonic Distortion
IM3	Third-Order Intermodulation
CMOS	Complementary Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
FSK	Frequency Shift Keying
IIP3	Input Third-Order Intercept Point

OIP3	Output Third-Order Intercept Point
RF	Radio Frequency
FoM	Figure of Merits
λ	Wavelength
SNR	Signal to Noise Ratio
BER	Bit Error Rate
QAM	Quadrature Amplitude Modulation
GSM	Global System for Mobile
LO	Local Oscillator
PSRR	Power Supply Rejection Ratio
LDO	Low-Dropout
PCE	Power Conversion Efficiency
DR	Dynamic Range
EH	Energy Harvesting
CCO	Current Controlled Oscillator
PI	Phase Interpolator

TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

LIST OF TABLES

TABLE Page

1. INTRODUCTION

The world is witnessing a radio revolution. From the initial impetus for improved mobile communication and a high data demand, a trend has emerged toward the continual development of many radio frequency (RF) technologies starting with 2G to the current much-improved 5G network technology. Between these two technologies, the access data rate has increased drastically. On the other hand, for local area communication, WiFi and Bluetooth technologies' generational development have been accompanied by improved data rates, latency, and more efficient power consumption.

The recent other trend is to make any thing we have and use in our life smart. Making it smart requires information analysis and sharing. The former can be achieved with a processor, while the latter can be achieved with radio communication. The technology that adopts the communication between all the smart objects we have in the world is called the Internet of Things (IoT) or Internet of Everything (IoE). The fact that an IoT unit needs processing and communication adds stress on the power budget for the whole system because they are considered the most power hungry functions. IoT nodes are typically equipped with a battery so it can provide the needed power for the systems; however, some of these nodes are placed in remote places that make it hard to replace the battery or to provide the power needed all the time. This has urged researchers to explore ideas and techniques to make use of all the energy sources available. Developers have integrated an Energy Harvesting (EH) system with the IoT node. The role of the EH system is to provide energy to the IoT node to extend its battery life of to make it self-sustainable. The EH system is designed to harvest energy from different sources; e.g. Radio Frequency (RF), solar and thermal.

The typical trade-off exists when there is a need for more processing power and more

battery life. Complementary Metal–Oxide–Semiconductor (CMOS) technology scaling helps to reduce the power consumption; nevertheless, the need for more processing power drains the battery. The other drawback is the Lithium–ion (Li–ion) battery technology. This common battery technology used for electronic devices does not scale at the same rate as CMOS scaling, resulting in a reduction in the area consumed by the system chips and an increase in the area consumed by the battery.

From the previous discussion, we can summarize that there are two recent trend in developing radio systems: i) targeting high data rate (like in 5G and WiFi) and ii) achieving ultra-low power consumption (like in IoT).

1.1 IoT and Spectrum Congestion

As previously mentioned, IoT is a network that can provide communication between any smart thing. The IoT is initially started with sensors and Radio Frequency Identification (RFID) tags; then, it widened to include more objects and things [1]. Fig. 1.1 shows a diagram for the IoT network. It connects all aspects of transportation, smart home devices, factories, power transmission lines and healthcare systems. On the other hand, having network that shares all these information poses threats for cyber security especially for sensitive information such that found in healthcare or for logistic control for the power grid. Cyber security is especially dependent on software and hardware level innovation.

One of the recent issues for radio communication is spectrum congestion. Whether it is high-performance mobile communication or energy efficient IoT radio, spectrum congestion become an issue for both licensed and unlicensed band. However, licensed spectrum is more organized. To overcome spectrum congestion problem and to improve the data rates, standards have explored new bands for licensed and unlicensed bands. For example, a 5 GHz band is allocated for WiFi and 60 GHz band represents a future plan,

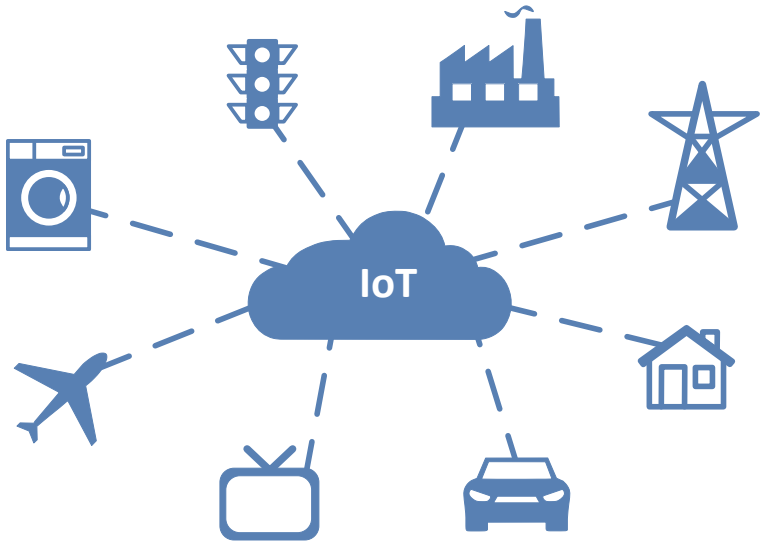


Figure 1.1: IoT network.

while 28 GHz is allocated for 5G cellular technology.

The reason for spectrum congestion is the increased number of standards and number of connected devices. For example, Fig. 1.2 shows the growth of the number of connected devices to IoT network [2] which is expected to be 20 billions by 2020. When the number of connected devices increases, the number of blockers also increases. That means the linearity requirement for the wireless systems become more stringent, which adds power budget stress on any system with limited energy resources.

1.2 Radio for IoT

To get insights about the radio for IoT, we need to consider the whole IoT node. Fig. 1.3 shows the IoT node block diagram [3]. The IoT radio consists of a transmitter and receiver with a T/R switch. The node also includes a microprocessor or data conversion unit for sensing. It has a clock generation unit that can be used for different blocks and memory for data storage. The unit includes energy harvesting and a power management

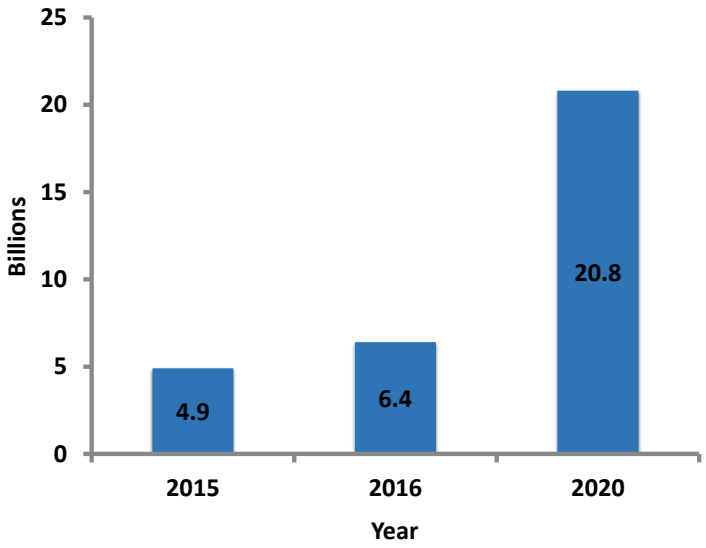


Figure 1.2: Growth in number of connected devices to the IoT network.

unit. The role of this unit is to harvest energy from different sources, to regulate the voltage, and to supply the power need for the unit. The ultimate goal for designing the unit is to make it self-sustainable. Radio for IoT must be designed with the consideration of energy limitation in the unit and IoT requirements.

1.3 Goals and Organization of the Dissertation

The goal for this dissertation is to present novel ideas for IoT radios with validation by chip testing. The dissertation contains four sections in addition to the introduction. The sections are organized as follows. Section 2 presents a highly linear low power wireless receiver for WSN. Current re-use of a transconductance low noise amplifier (LNA) is presented to reduce the power consumption along with a frequency multiplication mixer. The receiver baseband filter features a notch in the stop band to improve selectivity and linearity. In Section 3, an ultra-low power RF wireless receiver with RF blocker energy recycling is introduced. The system consists of a low power receiver and an RF energy

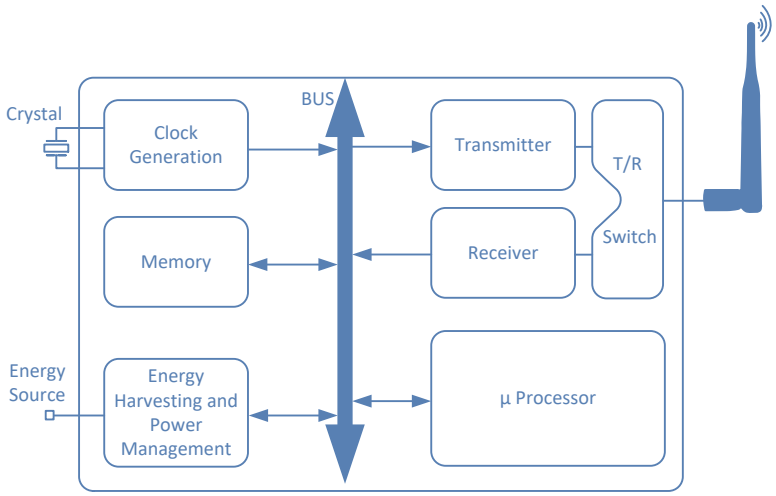


Figure 1.3: IoT node block diagram

harvesting unit. The system makes use of out-of-band blockers and recycle its energy to supply partial power need for the wireless receiver. In certain case, the core power consumption of the wireless receiver can be reduced by 49%. Section 4 presents a highly linear energy efficient wireless receiver using VCO-based OTA and clock recycling. The system employs mixer-first architecture with VCO-based OTA in the baseband due to its high linearity. The system also recycles the clock from the OTA's VCO to save power consumption. Finally, Section 5 summarizes conclusions about the research presented in this dissertation on radio for IoT as well as plans for future work.

2. HIGHLY LINEAR LOW POWER WIRELESS RF RECEIVER FOR WSN[1]

2.1 Introduction

Wireless circuits operating in the ISM band are under focus nowadays. This focus arises from an increased interest in the wireless sensor network (WSN) and short range wireless devices as the Internet of Things (IoT) continues to evolve at a rapid pace. However, the growth in the wireless communication sector and an increasing number of wirelessly connected devices causes spectrum congestion. This congestion is manipulated by moving wireless communication to other frequency bands, nonetheless, the congestion problem still exists. A review of IoT and WSN specifications shows that devices can tolerate a large noise figure (NF) [4]; however, device power consumption should be minimized to extend the battery life. This makes low power consumption a vital design target. In addition, the wireless system should have adequate linearity to overcome the increased number of blockers as the number of the connected devices is increased. Moreover, designing the wireless system to operate on a wide range of frequencies would make it more cost effective.

On the other hand, the WSN or IoT transceiver is typically accompanied with an energy harvesting unit [5, 6] from multiple sources. The dependence on energy supplied from the energy harvesting sources varies between partial dependence and full dependence with storage capability techniques to maximize the use of energy over time. In case of a self-sustainable WSN node, it would help to be able to use the wireless transceiver with programmability in power consumption based on the energy availability. However, the transceiver performance needs to be assessed carefully to count for system limitations.

[1] ©2019 IEEE. Part of this section is reprinted with permission from "Highly Linear Low Power Wireless RF Receiver for WSN," by O. Elsayed, J. Zarate-Roldan, A. Abuellil, F. Hussien, A. Eladawy, and E. Sánchez-Sinencio, 2019. IEEE Trans. Very Large Scale Integ. Syst.

Examining prior art, [4, 7] introduce low power receivers with lower NF; however, the former achieves high linearity with low gain while the latter achieves low linearity with high gain. [8] presents a short range low power wireless receiver with a Gilbert active mixer-first architecture; however, the receiver suffers from high NF, which limits the receiver sensitivity and has poor linearity. [9] presents an ISM band receiver; however, it suffers from high power consumption. [10, 11, 12, 13, 14, 15, 16] have introduced low power wireless receivers with different techniques to reduce the NF.

In this section [17], we introduce a low power highly linear wireless receiver for WSN. The receiver employs current-mode circuits starting with a current-reuse low-noise transconductance amplifier (LNTA). The receiver has a current-mode filter with high selectivity to improve the receiver linearity. The receiver has a frequency multiplication mixer to be clocked from a lower frequency local oscillator operating at 300 MHz to reduce the power consumption. The receiver operates at 900 MHz ISM band and is implemented in 130 nm CMOS technology. The receiver total power consumption is 1.16 mW. The receiver is designed with aim of improving linearity while minimizing the NF and power consumption. The linearity is improved as the receiver adopts current-mode architecture for the LNTA and the baseband filter. The linearity is furtherly improved by using notch at the stop band of the baseband filter. The power consumption is reduced in every receiver block. For the LNTA, transistors stacking and current re-use is applied while for the mixer, frequency multiplication mixer is used.

The section is organized as follows: Subsection 2.2 has the proposed RF system architecture. Subsection 2.3 presents the receiver building blocks and brief analysis. Subsection 2.5 presents the experimental results while Subsection 2.6 summarizes the main points in a conclusion.

2.2 Proposed RF Wireless System

Wireless receiver architectures have been developed based on specifications and requirements. Early RF receiver architectures usually consist of separate blocks (low-noise amplifier (LNA), mixer and filter) with voltage signal processing and either single or dual down conversion [18]. Later, more advanced receiver architectures were introduced with higher efficiency by integrating different functions in the same block with a mixture of voltage and current modes; e.g. the Blixer (a wideband balun-LNA-I/Q mixer) [19]. Recently, a mixer-first receiver architecture was introduced as a solution to tolerate large blockers [20]; nevertheless, it suffered from high NF, which led to the introduction of a noise-canceling mixer-first architecture [21].

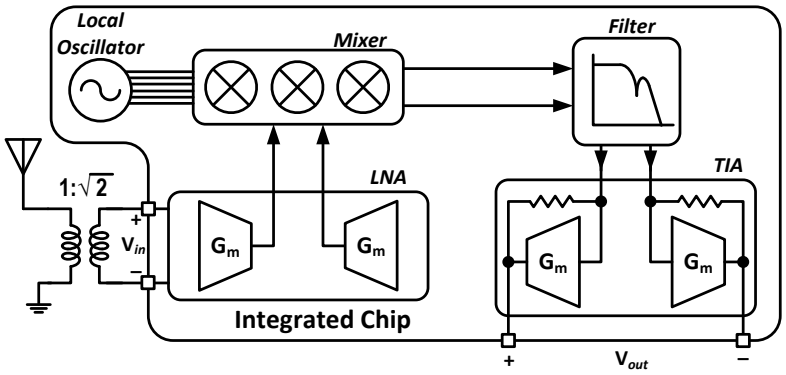


Figure 2.1: Proposed RF wireless receiver.

Fig. 2.1 shows the building blocks for the proposed receiver. The receiver operates at 900 MHz ISM band. Right after the antenna, a balun is there to convert the single-ended signal to a differential signal. The balun is followed by an LNA, which is a transconductance that transforms the RF voltage signal to an RF current signal. A passive mixer downconvertes the RF current signal at 900 MHz to the baseband using a six-phase low-

power ring oscillator running at 300 MHz [22]. The local oscillator is implemented using ring oscillator operating at 300 MHz to reduce the power consumption. After the mixer, the downconverted ac signal goes to a current-mode low pass filter. The filter is a second order low pass filter (LPF) with two zeros in the stop band to sharpen the roll-off. The ac baseband signal goes from the mixer output to the filter input. Finally, there is a transimpedance amplifier (TIA) to transfer the current signal to a voltage signal and to provide the required amplification. In each block, multiple techniques are utilized to reduce the power consumption and improve the performance while the receiver current-mode architecture improves the linearity. These techniques will be discussed in detail in Subsection 2.3. Compared to mixer-first architecture, which its mixer typically operates in voltage mode, the implemented receiver architecture operates the mixer in current mode as the output impedance of the LNTA is high while the baseband input impedance is low. Current mode circuit nodes are low impedance, which make the voltage swing minimal. As a result, linearity is improved.

2.3 Receiver Building Blocks

2.3.1 Transconductance LNA

The transconductance LNA has two roles: First, it has to convert the input voltage signal to an output current signal while introducing minimum noise. Second, it should provide input matching. As a survey for the prior art, Fig. 2.2 compares the transconductance LNA topologies [23, 24]. Common source LNA is shown in Fig. 2.2a. It provides reasonable transconductance while it doesn't provide input matching. Common source LNA with inductive degeneration is shown in Fig. 2.2b. Its G_m doesn't depend on transistor transconductance while it provides narrow band matching. Fig. 2.2c shows the single ended common gate LNA. It provides wide band matching; however, the transistor g_m should be large enough to provide the matching. Fig. 2.2d shows the

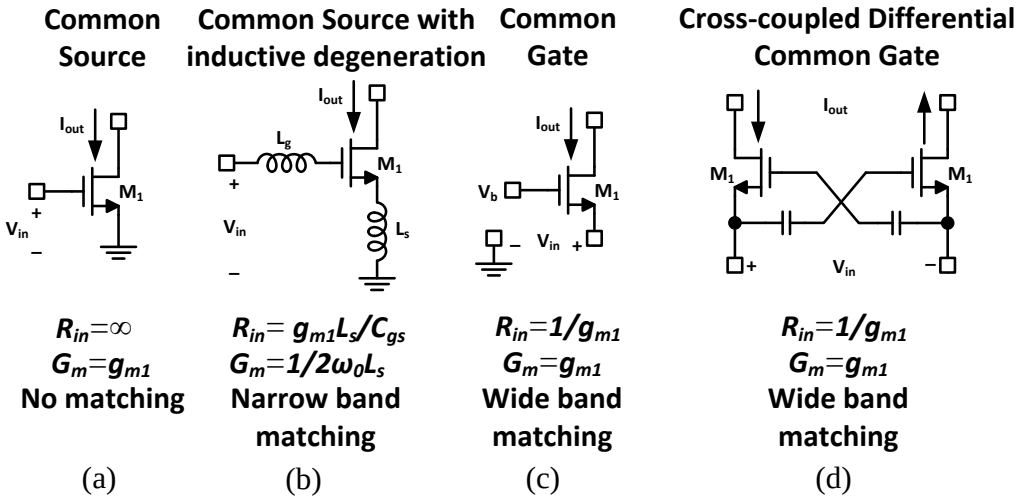


Figure 2.2: Transconductance LNA topologies. (a) common source, (b) common source with inductive degeneration, (c) single ended common gate, (d) cross-coupled differential common gate.

cross-coupled differential common gate LNA [25]. It provides wide band matching and the cross-coupling boosts the transistors g_m. The drawback of a common gate LNA is that it requires a large current to provide input matching. As a solution, Fig. 2.3 shows the basic concept of the proposed transconductance LNA. Unlike [25], complementary CMOS transistors (M_2 and M_3) are used to provide input matching. Both transistors have the input voltage (negative input voltage) applied at the gate (source) of the transistor to boost the transconductance by a factor of two. Additionally, M_1 and M_4 are added to increase the total transconductance. Current i_1 is given by:

$$i_1 = g_{m1}v_{in} + 2 \times g_{m2}v_{in}, \tag{2.1}$$

while i_2 is given by:

$$i_2 = g_{m4}v_{in} + 2 \times g_{m3}v_{in}. \tag{2.2}$$

The output currents can be summed together and the total output current will be:

$$i_{out} = i_1 + i_2 = \big(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4}\big)v_{in}. \tag{2.3}$$

Assuming $g_{m1} = g_{m3} = g_{mn}$ and $g_{m2} = g_{m4} = g_{mp}$, the total transconductance is given by:

$$G_m = \frac{i_{out}}{v_{in}} = 3\big(g_{mn} + g_{mp}\big). \tag{2.4}$$

The input current is given by:

$$i_{in} = 2\big(g_{mn} + g_{mp}\big)v_{in}, \tag{2.5}$$

and the input impedance becomes:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{2\big(g_{mn} + g_{mp}\big)}. \tag{2.6}$$

To provide matching, the following condition should be satisfied:

$$R_S = Z_{in} = \frac{1}{2\big(g_{mn} + g_{mp}\big)}, \tag{2.7}$$

where R_S is the source impedance (antenna impedance). By stacking four transistors, matching can be achieved with lower power consumption and total transconductance can be increased by added transistors.

Fig. 2.4 shows the differential and full implementation of the proposed transconductance LNA. Capacitors are used for ac coupling at input and to combine the output currents at output. As shown in Fig. 2.1, the LNTA is then followed by passive mixer. Equations (2.22)-(2.7) can be used to model the proposed LNTA in Fig. 2.4 ideally. Nev-

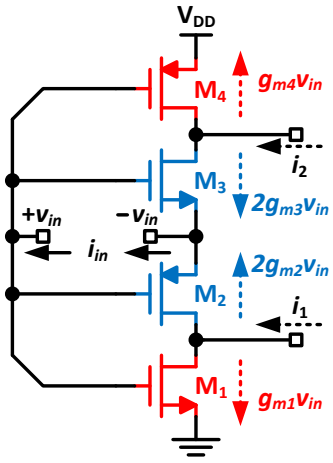


Figure 2.3: Proposed transconductance LNA concept.

ertheless, the nonidealities in the implementation seems to demand that we provide an expression for the input impedance with nonidealities. The input impedance is given as:

$$Z_{in,non-ideal} = 2 \times \frac{1 + (\beta_2 + \beta_4)/sC_C}{\beta_1 + \beta_2 + \beta_3 + \beta_4} \Big|\Big| \frac{1}{sC_{par}}, \tag{2.8}$$

where C_C is the ac coupling capacitor, C_{par} is the total parasitic capacitor seen at the LNTA input from all transistors gate capacitance, β_1 is given by:

$$\beta_1 = \frac{r_{ds2}}{2Z_{mix} \parallel r_{ds1} + r_{ds2}} g_{m2} + \left(\frac{r_{ds2}}{2Z_{mix} \parallel r_{ds1} + r_{ds2}} - 1 \right) g_{m1}, \tag{2.9}$$

where r_{ds1} and r_{ds2} are the drain to source impedance for transistors M_1 and M_2, respectively. $Z_{in,mixer}$ is the impedance seen at the mixer input. β_2 is given by:

$$\beta_2 = \frac{r_{ds2}}{2Z_{mix} \parallel r_{ds1} + r_{ds2}} \left(g_{m2} + 1/r_{ds2} \right). \tag{2.10}$$

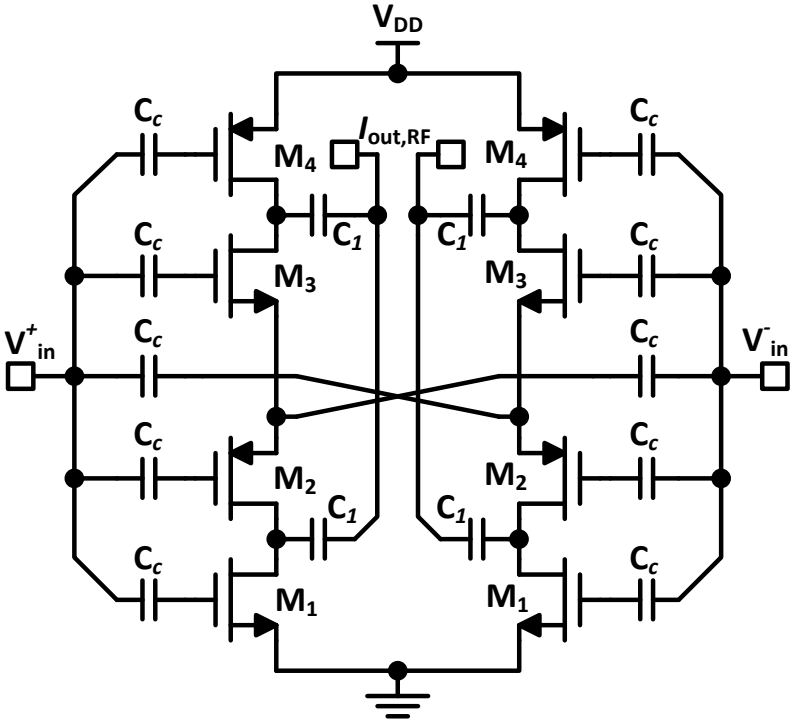


Figure 2.4: Fully differential implementation of the proposed transconductance LNA.

β_3 is given by:

$$\beta_3 = \frac{r_{ds3}}{2Z_{mix} \parallel r_{ds4} + r_{ds3}} g_{m3} + \left(\frac{r_{ds3}}{2Z_{mix} \parallel r_{ds4} + r_{ds3}} - 1 \right) g_{m4}, \quad (2.11)$$

where r_{ds3} and r_{ds4} are the drain to the source impedance for transistors M_3 and M_4, respectively. β_4 is given by:

$$\beta_4 = \frac{r_{ds3}}{2Z_{mix} \parallel r_{ds4} + r_{ds3}} \left(g_{m3} + 1/r_{ds3} \right). \quad (2.12)$$

From (2.8), we can see that the transconductance used for matching (g_{m2} and g_{m3}) is slightly reduced by g_{m1} and g_{m4} with a factor due to nonidealities. That would result in

an increase in $Z_{in,non-ideal}$ and higher power consumption is needed for better matching. For the transconductance LNA, S_{11} is given by:

$$S_{11} = \frac{Z_{in,non-ideal} - R_S}{Z_{in,non-ideal} + R_S}. \tag{2.13}$$

To verify (2.8) and (2.13), analytical $|S_{11}|$ is compared with simulated one in Fig. 2.5. The figure shows a good agreement between simulation and analysis.

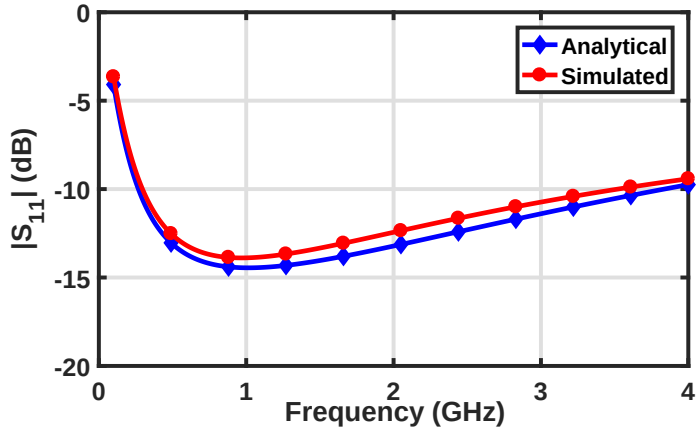


Figure 2.5: Simulated and analytical $|S_{11}|$ for transconductance LNA.

For the noise calculation, the total output noise from the circuit is given by:

$$\overline{i^2_{n,out}} = \overline{i^2_{n,M1}} + \overline{i^2_{n,M2}}/4 + \overline{i^2_{n,M3}}/4 + \overline{i^2_{n,M4}} = 4kT\gamma\big(g_{m1} + g_{m2}/4 + g_{m3}/4 + g_{m4}\big) \tag{2.14}$$

where k is Boltzmann constant, T is the temperature in Kelvin degrees and γ is the excess noise factor. The noise from M_1 and M_4 appear directly at the output while part of noise

current from M_2 and M_3 go to the output. The output noise from R_S is given by:

$$\overline{i^2_{n,R_S}} = 2 \times kTR_S \times \left(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4}\right)^2. \tag{2.15}$$

The NF is given by:

$$\mathrm{NF} = 1 + \frac{2\gamma}{R_S} \frac{g_{m1} + g_{m2}/4 + g_{m3}/4 + g_{m4}}{(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4})^2}. \tag{2.16}$$

If $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$ and using matching condition $R_S = 1/4g_m$, NF will be simplified to $\mathrm{NF} \approx 1 + \frac{10}{9}\gamma$. From (2.16), $\mathrm{NF} = 4.8$ dB while $\mathrm{NF} = 4$ dB from simulation. NF from the LNTA will affect the total receiver NF along the NF from mixer, baseband filter and TIA.

In this design, we have stacked four transistors to share the bias current and save the power consumption from nominal supply voltage (1.5 V). The transistors are biased in sub-threshold, as a consequence, the linearity is affected. A tradeoff between power and linearity takes place. The dc current in the stack is controlled by a current mirror circuit connected to M_1. In dc, M_2 and M_4 are diode connected transistors with large resistance. M_3 is biased via large resistance.

2.3.2 Mixer and LO Generation

Fig. 2.6 shows the block diagram for the clock generation. It employs the ring oscillator proposed in [22]. The ring oscillator is based on vertical delay cells to recycle the charge and reduce the power consumption. The oscillator consists of three differential stages. The oscillator operates at 300 MHz to reduce the power consumption and produces six phases shifted $T_{LO}/6$ apart. In order to downconvert the signal at 900 MHz with 300 MHz, two steps should be implemented: i) oscillator phases should be combined to generate 3 times higher clock phases and ii) the mixer should switch every $T_{LO}/3$. The

later can be implemented by having three mixers in parallel with one mixer active every $T_{LO}/3$. The former can be implemented by AND process between the six clock phases. The full schematic of the mixer is shown in Fig. 2.7. It consists of three double balanced mixers in parallel. Each mixer is active every T_{LO} so the RF input signal sees one active mixer every $T_{LO}/3$. The mixer uses the six clock phases from the oscillator $\phi_1 : \phi_6$. Each mixer, enlarged at top of Fig. 2.7, has four clock inputs. The mixer has two transistors in series to perform the AND process between the oscillator phases without consuming power. The mixer can be clocked from an external clock as well.

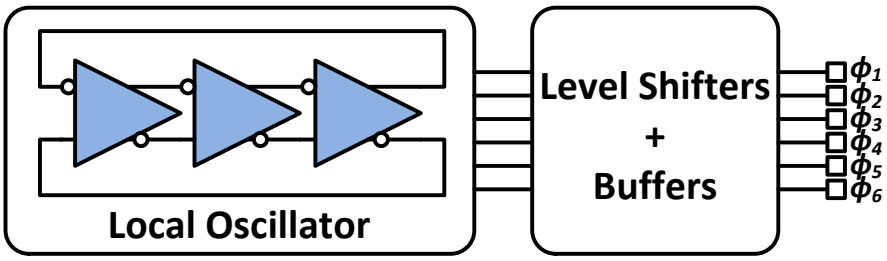


Figure 2.6: Block diagram for clock generation.

Analysis for the current-driven passive mixer is presented in [26, 27, 28, 29]. The current gain for the fundamental frequency for a mixer with a 50% duty cycle clock is $A_{I,mixer} = 2/\pi$. The mixer input impedance including the frequency translated impedance is given by:

$$Z_{in,mixer}(\omega) \cong 4R_{SW} + \frac{4}{\pi^2}\big[Z_{in,F}(\omega - \omega_{LO}) + Z_{in,F}(\omega + \omega_{LO})\big], \tag{2.17}$$

where R_{SW} is the switch resistance of transistor M_5 and $Z_{in,F}(\omega)$ is the baseband input impedance of the filter.

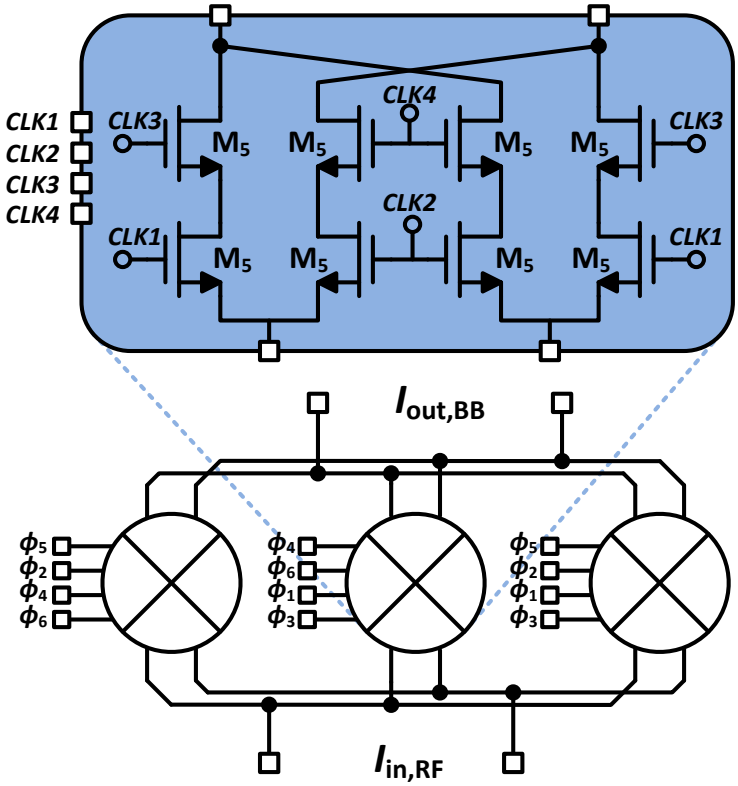


Figure 2.7: Proposed mixer schematic.

2.3.3 Baseband Filtering

The filter has important role in the receiver design to provide the selectivity for the signal of interest and to limit the noise. There is always a trade-off in the design of the filter. Power, linearity, noise and selectivity are the key parameters in designing the baseband filter. In this receiver, the used filter is a second order low pass current-mode filter. To sharpen the filter selectivity, shunt series resonance is added at the input of the filter to provide notch in the stopband. The model of the filter is shown in Fig. 2.8. The second order LPF is implemented with L_2, R and C_2 while the notch is implemented with L_1 and C_4. For implementation, Fig. 2.9 shows the implementation of the filter. Active inductor [30] is used to emulate inductance. The inductor for the shunt series resonance is

enlarged in the right side of the figure. M_8 transistors and C_5 are used to emulate inductor L_1 while M_7 provides negative resistance to cancel the inductor resistance. Inductor L_1 and L_2 are given by $L_1 = 4C_5/g_{m8}^2$ and $L_2 = 4C_3/g_{m6}^2$, respectively. In simulation, lowest Q for L_1 in bandwidth of 30% of notch frequency is 27. The power consumption for L_1 is 185 μW. Adding L_1 doesn't degrade receiver in-band noise performance as the noise products from L_1 active transistors appear at baseband output only at the vicinity of notch frequency. The total transfer function for the filter is given by:

$$A_{I,filter} = \frac{i_{out}}{i_{in}} = \frac{(g_{m6}^2/4C_2C_3)(2C_5/g_{m8}^2 s^2 + 1/C_4)}{\frac{2C_5}{g_{m8}^2}s^4 + \frac{g_{m6}}{C_2} \times \frac{C_5}{g_{m8}^2}s^3 + \left(\frac{1}{2C_2} + \frac{1}{C_4} + \frac{C_5 g_{m6}^2}{2C_2C_3g_{m8}^2}\right)s^2 + \frac{g_{m6}}{2C_2C_4}s + \frac{g_{m6}^2}{4C_2C_3C_4}}. \quad (2.18)$$

It is calculated under the condition that $g_{m7} = g_{m8}$. The single side filter input impedance is given by:

$$Z_{in,F}(s) = \frac{s/2C_2}{s^2 + (g_{m6}/2C_2)s + g_{m6}^2/(4C_2C_3)} \parallel \left(2C_5/g_{m8}^2 s + 1/sC_4\right). \quad (2.19)$$

The power per pole is 60 μW. Active inductor is sensitive to PVT and bias variations especially when the active inductor is used to implement a notch in the stop band. In order to study the impact of those variations, Fig. 2.10 shows the Monte Carlo simulation for the notch rejection. In the simulation, process and mismatch variations are applied with 100 samples. While the rejection varies with process and mismatch, the rejection is still good for most of the samples. Fig. 2.11 the Monte Carlo simulation for frequency of the notch. The plot shows that the notch frequency doesn't have large variation (standard deviation=155 kHz) with the process and mismatch variations.

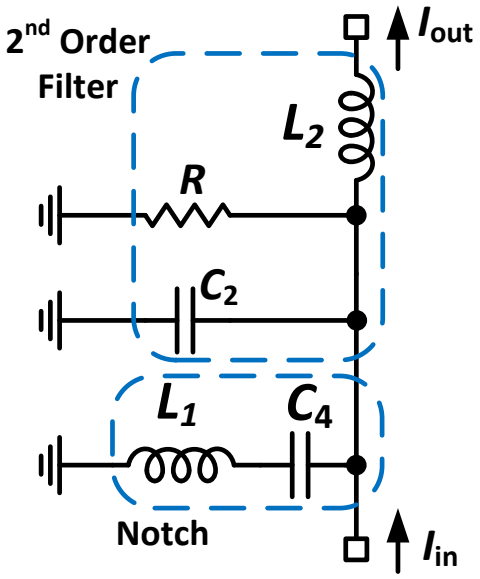


Figure 2.8: Filter model.

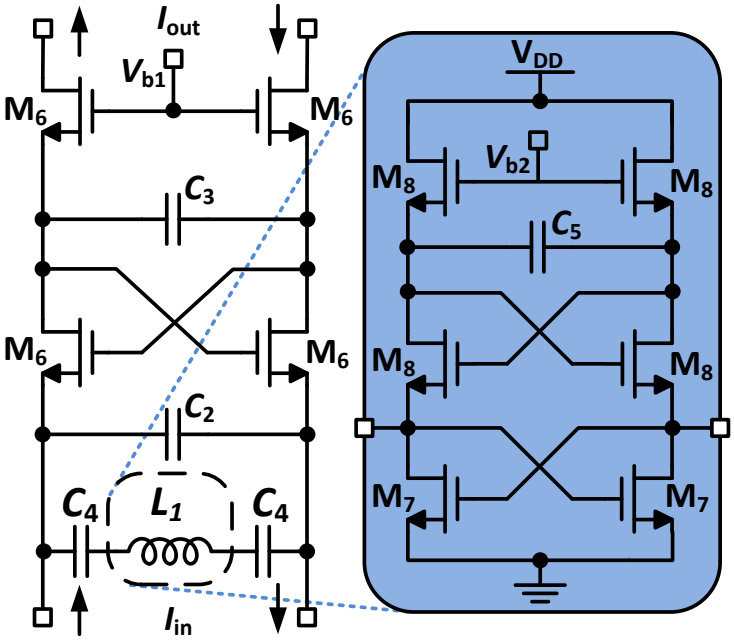


Figure 2.9: Filter schematic.

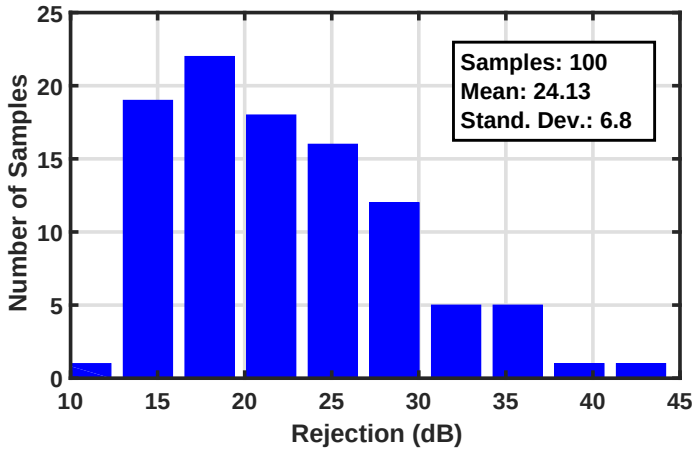


Figure 2.10: Monte Carlo simulation for notch rejection.

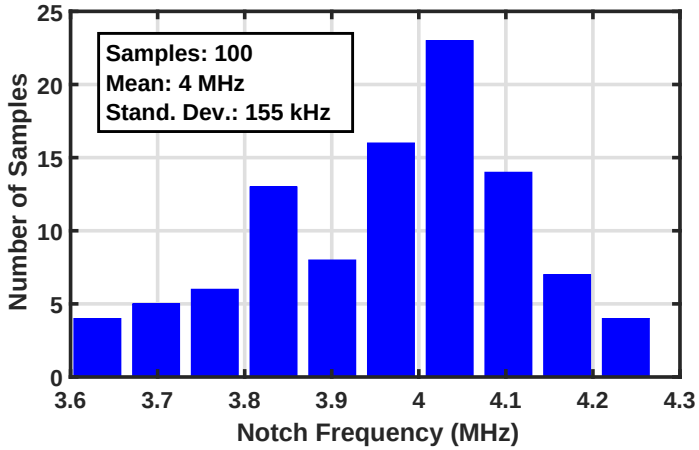


Figure 2.11: Monte Carlo simulation for notch frequency.

2.3.4 Transimpedance Amplifier

The transimpedance amplifier (TIA) role is to convert the current signal to voltage signal. The schematic of the TIA is shown in Fig. 2.12. It consists of a complementary

CMOS to reduce the power consumption. Capacitor (C_6) is added to improve the filtering. The transimpedance transfer function is given by:

$$A_{T,TIA} = \frac{v_{out}}{i_{in}} = -\frac{(g_{m9} + g_{m10})R_1 - 1}{g_{m9} + g_{m10} + 2C_6 s}. \tag{2.20}$$

The transfer function has pole at $(g_{m9} + g_{m10})/2C_6$.

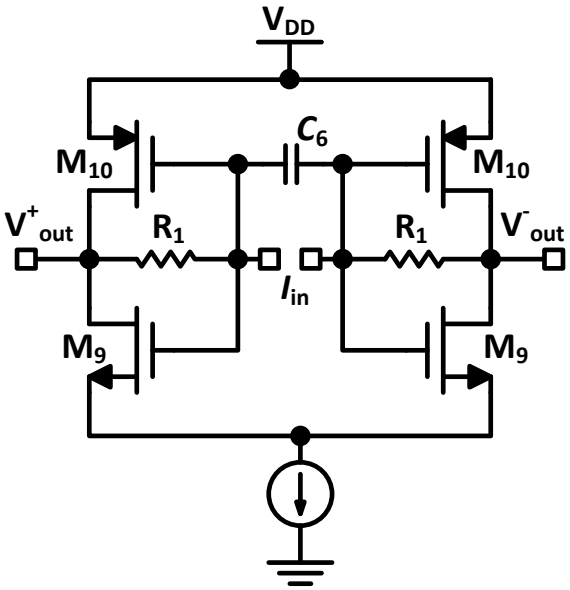


Figure 2.12: TIA schematic.

2.3.5 Receiver Conversion Gain and Linearity

The total receiver voltage gain is given by:

$$A_{Rx} = G_{m,LNTA} \times \frac{Z_{o,LNTA}}{Z_{o,LNTA} + Z_{in,mixer}} \times A_{I,mixer} \times A_{I,filter} \times \frac{Z_{o,filter}}{Z_{o,filter} + Z_{in,TIA}} \times A_{T,TIA} \tag{2.21}$$

where $G_{m,LNTA}$ is the LNTA transconductance, $Z_{o,LNTA}$ is the output impedance of the LNTA, $Z_{o,filter}$ is the output impedance of the filter and $Z_{in,TIA}$ is the input impedance of the TIA. To verify (2.21) along with (2.18), Fig. 2.13 shows a comparison between the simulated and analytical receiver conversion gain. The figure shows a good agreement between the simulation and calculation. The notch in the filter transfer function helps to sharpen the selectivity and improves in-band linearity. For the out-of-band linearity, the LNTA and mixer dominate the nonlinearity since the large capacitor at the input of the filter absorbs the large blocker at out-of-band frequencies.

Fig. 2.14 shows the third harmonic distortion (HD3) at each output of the blocks and at the receiver output. The linearity at the LNTA output doesn't change with the frequency whileit changes at other blocks' output. At low frequency, the linearity degrades as the signal travels through the receiver blocks. From (2.19), we can see that the input impedance of the filter has its maximum value at the cut-off frequency. That would degrade the linearity at the cut-off frequency of the filter. At high frequency, the HD3 is improved for baseband blocks.

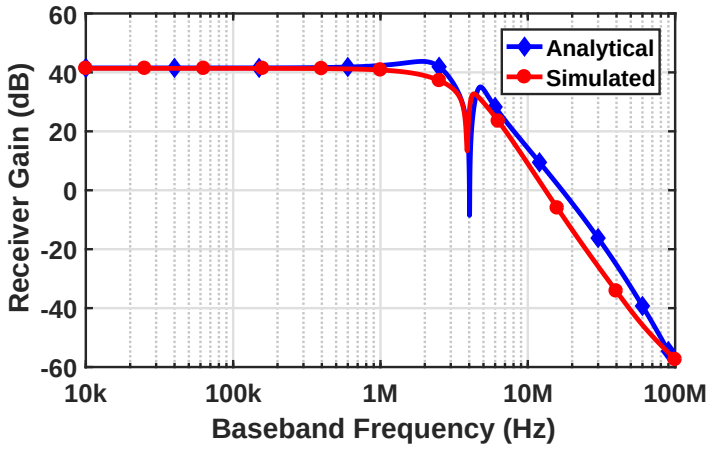


Figure 2.13: Simulated and analytical receiver gain.

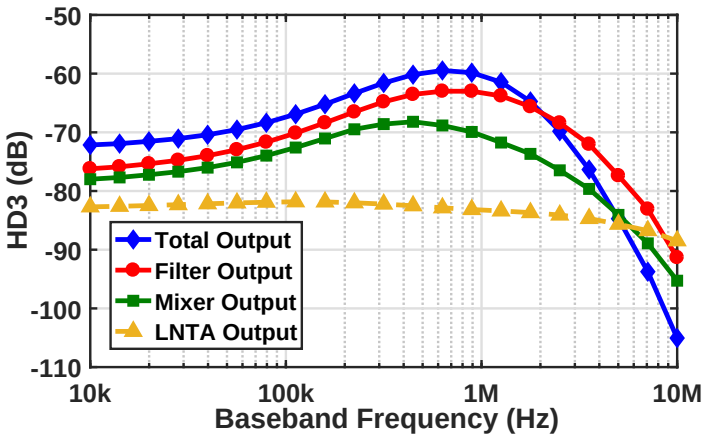


Figure 2.14: Simulated HD3 for receiver blocks.

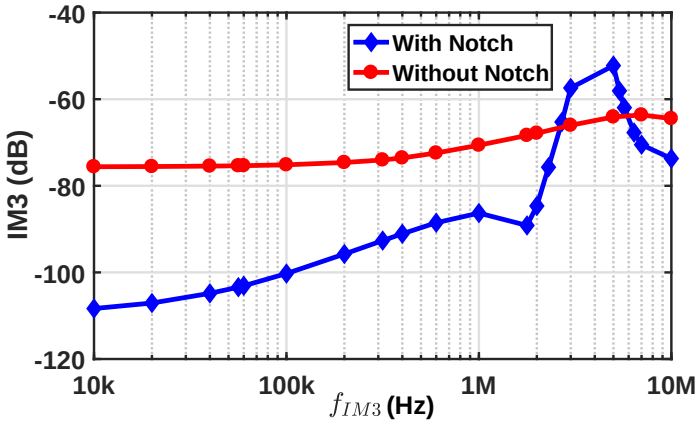


Figure 2.15: Simulated IM3 for the receiver.

Fig. 2.15 shows the simulated third intermod (IM3) for the receiver versus the third intermod frequency (f_{IM3}). It is simulated by applying two tones at the receiver input with frequencies $f_{LO} + 1/2 f_{AC} + 1/2 f_{IM3}$ and $f_{LO} + f_{AC}$ where f_{AC} is the frequency of the adjacent channel and equals $f_{AC} = 4$ MHz. Fig. 2.15 shows a comparison for the IM3

with and without the existence of the notch at the stop band. The figure shows that the filter with the notch has better linearity especially at low frequency. The linearity starts to degrade as we approach the cut-off frequency of the filter. The receiver with the notch circuit has worst linearity at 4 MHz. The reason for that is at this frequency, the two tones lies in the notch band where the active circuitry of the notch introduce its nonlinearity. However, the frequency of the intermod lies outside our band of interest.

2.4 Design Procedure

To start designing the whole system, we need to design each block and see how they interact with each other. Starting with the LNTA, to achieve the matching, we can use (2.7) to determine the value of g_{m2} and g_{m3} based on the available source resistance R_S that is typically 50 Ω. Then, we can use (2.3) to get the value of g_{m1} and g_{m4}. However, we need to define or assume the value of $G_{m,LNTA}$. In order to obtain that, we need to use (2.21) and define the LNTA contribution to the total receiver gain along with $A_{T,TIA}$ as $A_{I,mixer} = 2/\pi$ and $A_{I,filter} \approx 1$. On the other hand, the value of g_{m1} and g_{m4} cannot be too large as it will reduce the LNTA output resistance and its ability to drive the following stage. After calculating the g_m values, the dc current can be defined and the transistor sizing can be calculated.

For the mixer, the design parameter would be the switch sizing. The sizing of the switch affects the power consumption of the clock buffer and the driving ability of the LNTA to the baseband filter. The larger (smaller) the switch size, the higher (lower) power consumption at the clock buffer, while the driving capability of the LNTA to the baseband filter will be higher (lower). There is a trade-off here. Generally, $Z_{O,LNTA} \gg Z_{in,mixer}$ must be satisfied to achieve good driving ability for the LNTA.

For the filter, we should consider many parameters. First, the maximum input impeda-

nce of the filter happens at the cut-off frequency. The single side input impedance is

$$Z_{in,F}(\omega_\circ) = \frac{1}{g_{m6}} \tag{2.22}$$

at the cut-off frequency. On the other hand, filter input impedance needs to be low so the LNTA can drive the mixer and filter with low loss. However, making the filter input impedance small means consuming larger current in the filter. There is a tradeoff here. After selecting g_{m6} based on maximum tolerable input impedance and power consumption, the filter capacitor can be calculated based on (2.18) after selecting the required cut-off frequency. The notch circuit can be designed based on the required notch location in the stop band.

For the TIA, R_1 is selected based on the required TIA gain. g_{m9} and g_{m10} should be maximized, however, power consumption will be the limit.

2.5 Experimental Results

A test chip for the wireless receiver is fabricated in 130 nm CMOS technology. The receiver operates at the 900 MHz ISM band. Fig. 2.16 shows the measured and simulated $|S_{11}|$ for the receiver. It shows the matching for 200 MHz. The matching bandwidth is limited due to the bond wires and PCB traces. Fig. 2.17 shows the measured and simulated receiver conversion gain. The gain is 40 dB and the $3-$dB bandwidth is 1.6 MHz. In measurement, external clock is used to locate the notch in the stop band. Fig. 2.18 shows the receiver measured and simulated NF. The NF is 14 dB and the flicker noise corner frequency is 160 kHz. Fig. 2.19 shows the measured receiver in-band IIP3. The IIP3 is -6 dBm as the linearity is improved from sharp selectivity. The linearity achieved in the receiver is better than the WSN receiver can tolerate [31], however, the concept can be used in different applications and standards. To elaborate more on the receiver

performance versus the power consumption, Fig. 2.20 shows the measured receiver in-band OIP3 and NF versus receiver power consumption. In this measurement, the power is reduced from LNTA, filter and TIA while the other circuitry power consumption remains the same. As the power consumption increases, the linearity and NF improve. To verify the operation of the wireless receiver, the receiver is tested with Silicon Labs transceiver module (Si4463). The module is used as transmitter with FSK modulation and transmits PRBS9 signal. The testing setup is shown in Fig. 2.21. Fig. 2.22 shows photograph for measurement setup. Fig. 2.23 shows the received data at baseband of the receiver in the upper trace while the lower trace shows the de-modulated data.

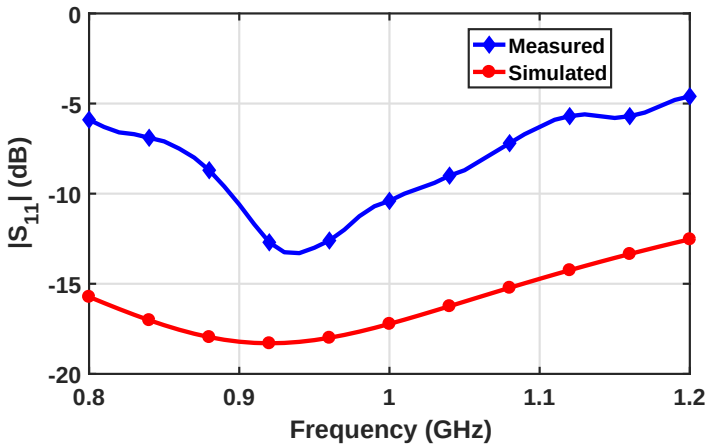


Figure 2.16: Measured and simulated receiver $|S_{11}|$.

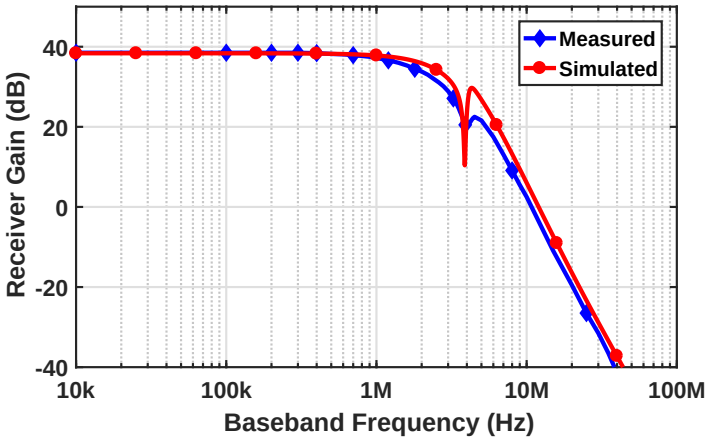


Figure 2.17: Measured and simulated receiver conversion gain.

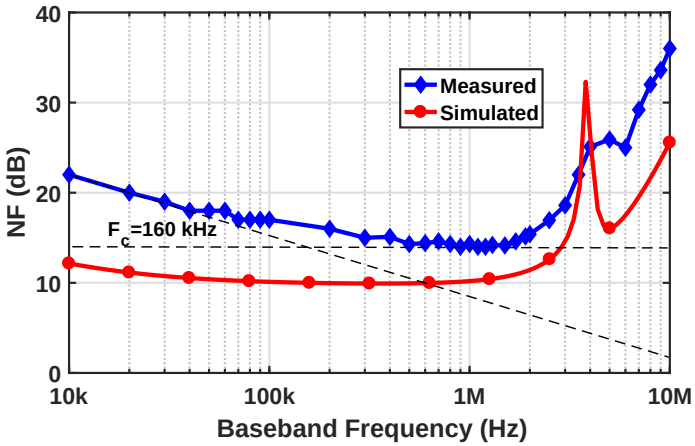


Figure 2.18: Measured and simulated receiver NF.

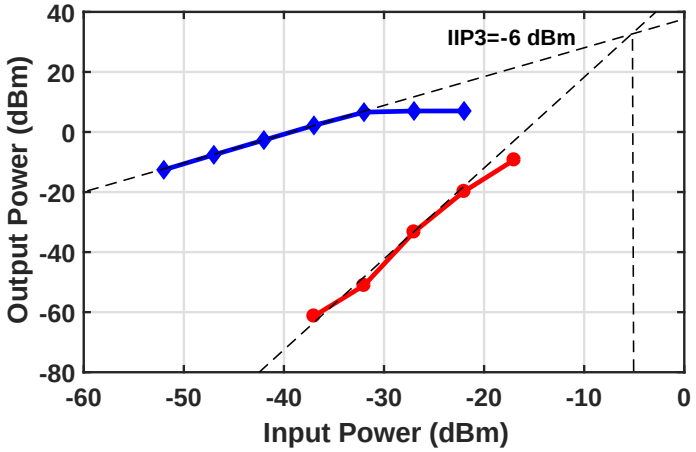


Figure 2.19: Measured receiver in-band IIP3.

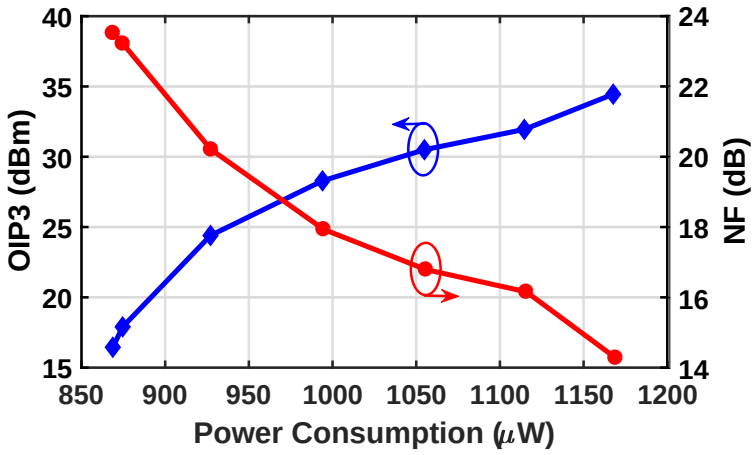


Figure 2.20: Measured receiver in-band linearity and NF versus power consumption.

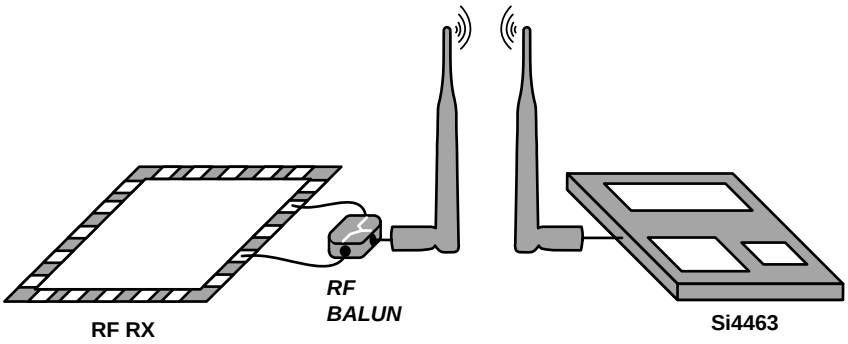


Figure 2.21: Receiver test setup with Si4463 module.

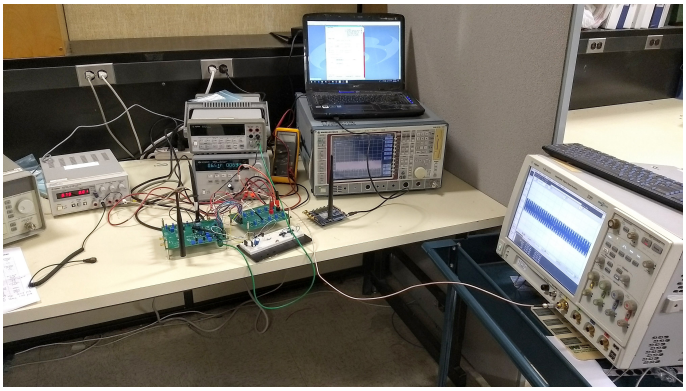


Figure 2.22: Photograph for measurement setup.

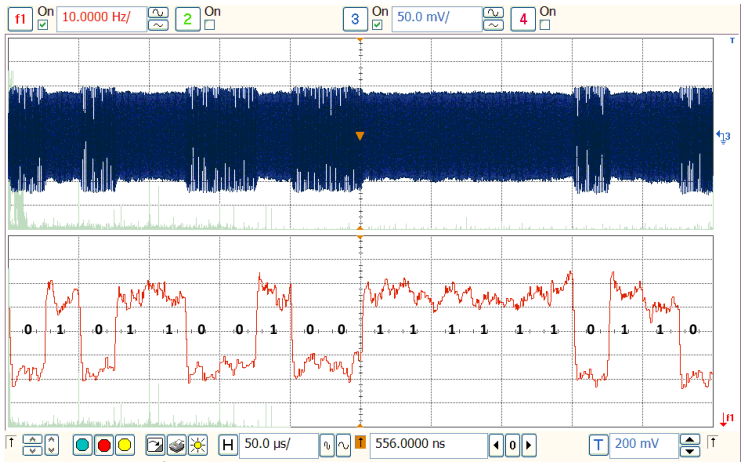


Figure 2.23: Received and de-modulated FSK data from Si4463 module.

A micrograph for the chip die is shown in Fig. 2.24. Fig. 2.25 shows the receiver power distribution. Finally, Table 2.1 gives a performance summary and comparison with the state-of-the-art systems. The receiver shows its competitiveness among other designs especially in the linearity while keeping the NF low. Comparison table has two Figure of Merits (FoM). FoM_1 is given by:

$$\mathrm{FoM}_1 = 10\times \log\left(\frac{\mathrm{IIP3(Linear)} \times \mathrm{RF\ Freq.(MHz)} \times \mathrm{Tech.(nm)}}{\mathrm{NF(Linear)} \times \mathrm{Power(mW)}}\right) \tag{2.23}$$

and FoM_2 is given by:

$$\mathrm{FoM}_2 = -\mathrm{RX}_{\mathrm{Sensitivity}} - 10 \times \log\big(\mathrm{Power(mW)}\big). \tag{2.24}$$

Our work tops other designs for FoM_1 and shows its competitiveness for FoM_2.

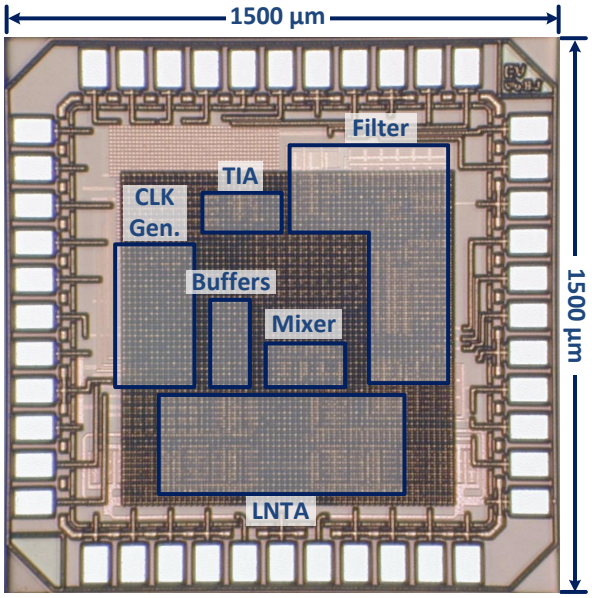


Figure 2.24: Die micrograph for test chip in 130 nm CMOS.

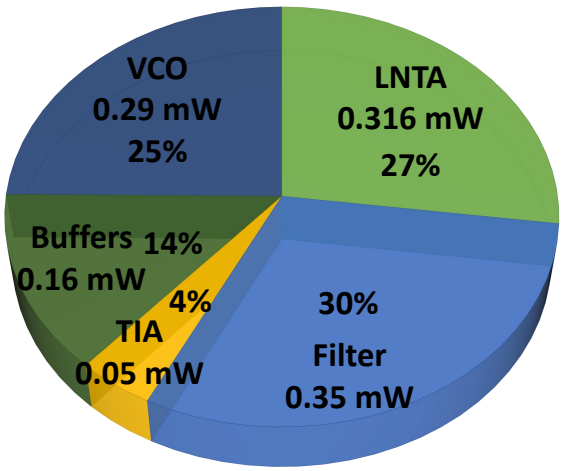


Figure 2.25: Receiver power distribution.

2.6 Conclusions

A highly linear low power wireless RF receiver suitable for WSN is introduced. The receiver has improved linearity due to high selectivity of the baseband filter and current-mode blocks. The power consumption is minimized by using current re-use in the LNTA and frequency multiplication in the mixer design. The receiver operates at 900 MHz ISM band and is implemented in 130 nm CMOS technology. The receiver power consumption is 1.16 mW and the IIP3 is -6 dBm. The receiver performance make it a good candidate for WSN and IoT applications.

Table 2.1: Performance Summary and Comparison with the State-of-the-Art Systems

	Masuch [4]	**Cruz [7]**	**Khan [8]**	**Balankutty [9]**	**Lee [10]**	**Selvakumar [11]**	**Wang [12]**	**Lin [13]**	**Sano [14]**	**This Work**
Architecture	Mixer-First	Low-IF Current-Bleeding	Gilbert Active Mixer-First	Zero-IF /Low-IF	Mixer-First	QLNA	Sliding-IF	RF-to-BB Recycled Front-End	Sliding-IF	LNTA+ CM Filter
RF Frequency (MHz)	2400	400	2400	2400	2400	2400	2400	900	2400	900
Gain (dB)	13†	30	37	67	55	55.8	57.8	48	NA	40
NF (dB)	16	13.2	28	16	13.6	15.5	15.7	8.7	6.5	14
Channel BW (MHz)	1	0.3	1	1	2.2	1	1	1	1	1.6
In-Band IIP3 (dBm)	NA	-17	-35	-10.5	NA	-16	-18.5	-20.5	NA	-6
Power (mW)	1.1	1.3	0.87◇	32.5	0.97◇	0.6	1.78	1.15	6.3	1.16
CMOS Technology	130 nm	180 nm	65 nm	90 nm	28 nm	130 nm	65 nm	65 nm	40 nm	130 nm
FoM_1	-	17.23	-10.4	11.7	-	25.6	15.2	17.8	-	30
FoM_2	84.6	91.9	73.6	69.9	84.1	87.7	82.8	91.7	86.5	84.3

† Estimated ◇ Excluding clock generation

3. AN ULTRA-LOW POWER RF WIRELESS RECEIVER WITH RF BLOCKER ENERGY RECYCLING FOR IOT APPLICATIONS[1]

3.1 Introduction

The number of connected things to Internet of Things (IoT) network is expected to be 20 billion by 2020 [2]. This huge growth in the number of connected devices, up from 6 billion at 2016, should be accompanied by extensive research on wireless transceivers. The wireless sensor network (WSN) node is a very popular application as an IoT device. This device can be deployed in wearables, cars, street light lamps, electricity meters, forests, volcanoes and so on. Once deployed [32], this device needs to stay there as long as possible without costly maintenance such as that found in battery replacement. Therefore, the ultimate goal is to make this device self-sustainable. As a consequence, the power consumption for the RF transceiver, which is one of the most power hungry blocks in the entire system, should be minimized. Yet, the crowded spectrum is extremely challenging. Too many transceivers in a limited spectrum are like too many people sitting in a confined room–the more people talk, the more noise is generated, and the fewer words people hear and understand. In this situation, some people start to raise their voice to convey their messages. By analogy, transmitters start to send signals with a higher power which means larger blockers. From this discussion, we can summarize the requirement for IoT wireless receivers as: i) insusceptibility to large blockers and ii) ultra low power consumption.

As a survey for prior art, blocker resilient wireless receivers were implemented in

[1] ©2018 IEEE. Part of this section is reprinted with permission from "An Ultralow-Power RF Wireless Receiver With RF Blocker Energy Recycling for IoT Applications," by O. Elsayed, M. Abouzied, V. Vaidya, K. Ravichandran, and E. Sánchez-Sinencio, Nov. 2018. IEEE Trans. Microw. Theory Techn., vol. 66, no. 11, pp. 4927−4942.

[33, 20, 21, 34, 35, 36] with different techniques to improve the linearity and to reduce the noise figure (NF), but the receivers suffered from high power consumption. Other designs [37, 38, 39, 8, 40] were able to reduce the power consumption to a lower limit, but it is still high power for sustainable operation. [41] introduced low power transceiver with integrated RF energy harvesting, but the harvester is not able to operate concurrently with the transceiver at high power levels. In [42], low energy wake-up receiver is introduced with multiple sources of energy harvesting including RF. In [43], low voltage transconductance mixer with mutual noise-cancellation technique is introduced. In [44, 45], ultra-low power wake-up receivers are presented. In [46], ultra-low power transceiver for biomedical applications is presented with integrated RF energy harvesting system.

From another point of view, energy harvesting is expected to be integrated in IoT standards to enable green operation where required power from the IoT nodes is scavenged from ambient sources. Specifically, RF energy harvesting converts the RF ambient electromagnetic waves to useful dc energy. A minimum input signal [47] is a characteristic of these systems and has been analyzed in [48] for integrated CMOS designs with on-chip and off-chip matching networks where charging capacitors take a considerable amount of time at the sensitivity levels. In [49], RF energy harvesting co-designed with custom antennas were demonstrated. However, in the presence of large RF blockers, the input signal is large enough to operate the system in a more efficient way [50, 51, 52, 53, 54, 55, 56, 57].

In this section, we present an energy efficient wireless receiver system that is suitable for IoT applications [54, 58]. It is a mixer-first based receiver with current mode operation to withstand large blockers. The wireless receiver system is not only unaffected by large blockers, it is also able to harvest energy from out-of-band blockers for further battery power consumption reduction. As a result, the battery life for IoT applications can be

extended. The receiver system, that has I and Q paths and an RF energy harvesting front end, is implemented in 180 nm CMOS technology and operates at 900 MHz ISM band. The receiver system power consumption is about 0.43 mW, and it can be reduced to 0.22 mW in the presence of a large blocker ($\approx$ 0 dBm) [18, 59].

In this section [54, 58], analysis is introduced for link budget and for the receiver's building blocks along with receiver's NF analysis. Analysis and trade-offs of the RF rectifier design are presented. Interfacing and interaction between the receiver and the RF rectifier are discussed. Supplementary measurement results for in-band linearity and RF rectifier performance are presented.

The section is organized as follows: subsection 3.2 has the link budget analysis and the proposed RF system architecture. Subsection 3.3 discusses the receiver building blocks and the circuit design and analysis. subsection 3.4 discusses the design and analysis for the proposed RF rectifier. subsection 3.6 has the measurement results. Finally, subsection 3.7 gives conclusions.

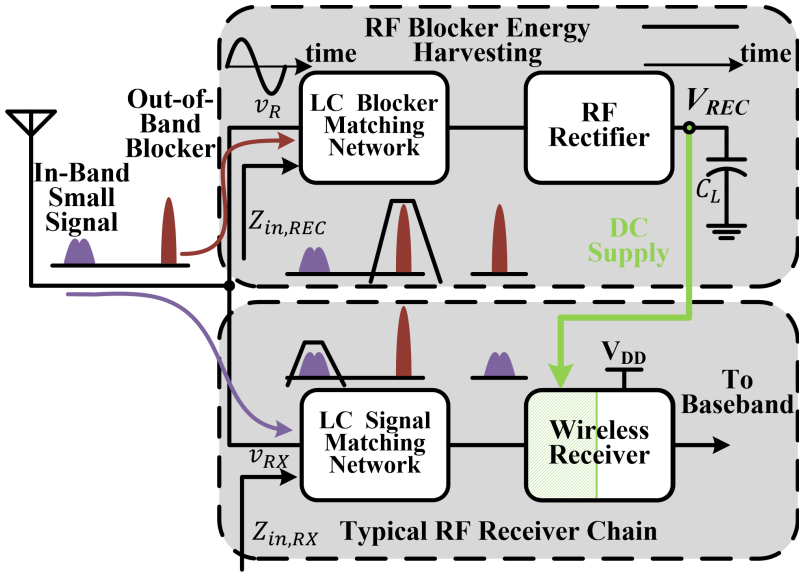


Figure 3.1: Proposed RF wireless receiver system.

3.2 Link Budget Analysis and Proposed RF System Architecture

To analyze the link budget of a wireless communication between transmitter and receiver, we start with the well known link budget equation [60]

$$P_{RX} = \frac{P_{TX} G_{TX} G_{RX}}{L_{fs}}, \tag{3.1}$$

where P_{RX}, P_{TX}, G_{TX} and G_{RX} are the received power, transmitted power, transmitter antenna gain and receiver antenna gain, respectively. L_{fs} is the free-space path loss and given by:

$$L_{fs} = \left(\frac{4\pi d}{\lambda}\right)^2, \tag{3.2}$$

where d is the distance between the transmitter and receiver and λ is the carrier wavelength in the free space. Assuming 0 dBm transmitted power (P_{TX}) from the transmitter, 2 dBi transmitter and receiver antenna gain (G_{TX} and G_{RX}), 500 m distance and 900 MHz carrier frequency, the received power will be $P_{RX} = -81.5$ dBm.

For a wireless receiver, the sensitivity is given by [23]

$$P_{sens} = 10\log(kT) + 10\log(\mathrm{B}) + \mathrm{NF} + \mathrm{SNR} + \mathrm{MAR}, \tag{3.3}$$

where k, T, B, NF, SNR, MAR are the Boltzmann constant, temperature, receiver's bandwidth, receiver's NF, required SNR for demodulation and a certain margin, respectively. Assuming $P_{sens} = P_{RX} = -81.5$ dBm, $T = 300$ K, B$= 500$ kHz, SNR$= 11.5$ dB for 16-QAM with bit error rate (BER) of 10^{-3} [61] and margin of 3 dB, the required receiver's NF will be 21 dB. Also from [4, 11], NF for IoT applications can be relaxed to 19 dB.

The proposed wireless receiver architecture is shown in Fig. 3.1. The antenna receives in-band small signals and large out-of-band blockers. The typical RF receiver chain is

shown at the bottom where an LC matching network is used for impedance transformation and another role of the matching network is to attenuate the out-of-band blockers. The proposed system introduces another path, shown in the top of Fig. 3.1, for the blocker signal flow where an RF rectifier is used for ac to dc conversion of the blocker RF power. An LC matching network is used to transform the input impedance of the wireless receiver block to the antenna impedance (assume $50\ \Omega$) for maximum power transfer and blocker signal selection due to the band pass nature of the input impedance $Z_{in,REC}$. The ripple on the rectifier output voltage V_{REC} is filtered by the load capacitor C_L, and V_{REC} is used to partially supply the wireless receiver with dc power as a recycling process of the RF blocker. Thus, although the RF blockers are traditionally considered non-desirable signals for their effects on the traditional receivers, in the proposed system, they can be used to lower its effective power consumption or even achieve batteryless design as an ultimate goal. The same antenna is used for concurrent reception of both signals: the receiver and blocker signals. In GSM standard, wireless systems may receive blockers as large as 0 dBm at 980 MHz [18, 59] which is 80 MHz away from our band of interest. The idea of the receiver system can be applied at different frequency bands as well.

A more detailed block diagram for the wireless receiver system is shown in Fig. 3.2. The system consists of an RF wireless receiver and an RF rectifier with series inductors to adjust the impedance levels. The used antenna can be any omni or directional antenna that works at 900 MHz. After the antenna, there is a balun with voltage ratio of $1{:}\sqrt{2}$ to provide 50 Ω impedance at all terminals. The balun part number is "B0430J50100AHF". The wireless receiver is a current-mode mixer-first receiver with a passive mixer. The mixer is followed by a current-mode baseband low pass filter (LPF). At the end, there is a transimpedance amplifier (TIA) to convert the current signal to a voltage signal and to provide the adequate gain. The baseband filter has two power supplies, main supply

(V_{DD}) and auxiliary supply (V_{AUX}). Main supply (V_{DD}) is always connected to the system battery. The system operation and auxiliary supply (V_{AUX}) behavior is described as follows: If there is no blocker or there is a blocker with low power, V_{AUX} will be connected to the main supply (V_{DD}). If there is a large blocker ($\approx$ 0 dBm), V_{AUX} will be automatically connected to V_{REC}. In this case, the filter will be partially powered up from the RF rectifier. As a result, the power consumption of the wireless receiver from the battery is reduced. L_1 is implemented off-chip to add degree of freedom for the design; however, for mass production, L_1 can be easily integrated to reduce cost. The off-chip Q is 60 while the on-chip Q is 11.

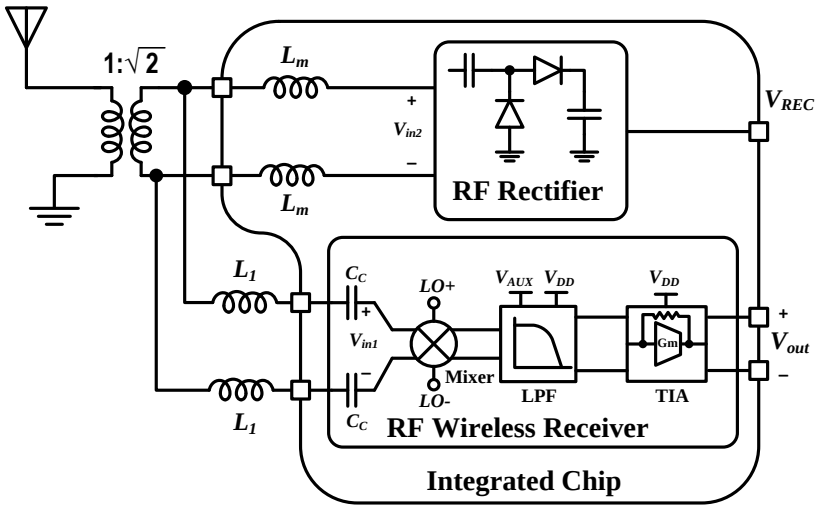


Figure 3.2: Proposed RF wireless receiver system block diagram.

3.3 Receiver Blocks Implementation and Circuit Design

Fig. 3.3 shows the detailed I/Q design of the RF wireless receiver. Each arm consists of a passive mixer, baseband low pass filter and transimpedance amplifier. As the filter dominates the power budget, the auxiliary supply (V_{AUX}) is connected only to the filter.

There is a switch that controls whether V_{AUX} is connected to V_{REC} or V_{DD}. The switch is controlled by the supply control that has the rectifier output voltage (V_{REC}) as input. A clock generation circuit is implemented to generate 25% duty cycle 4 phases from an external RF source with frequency of $2f_{LO}$ (1.8 GHz). In the following subsection, we will discuss all the blocks in detail.

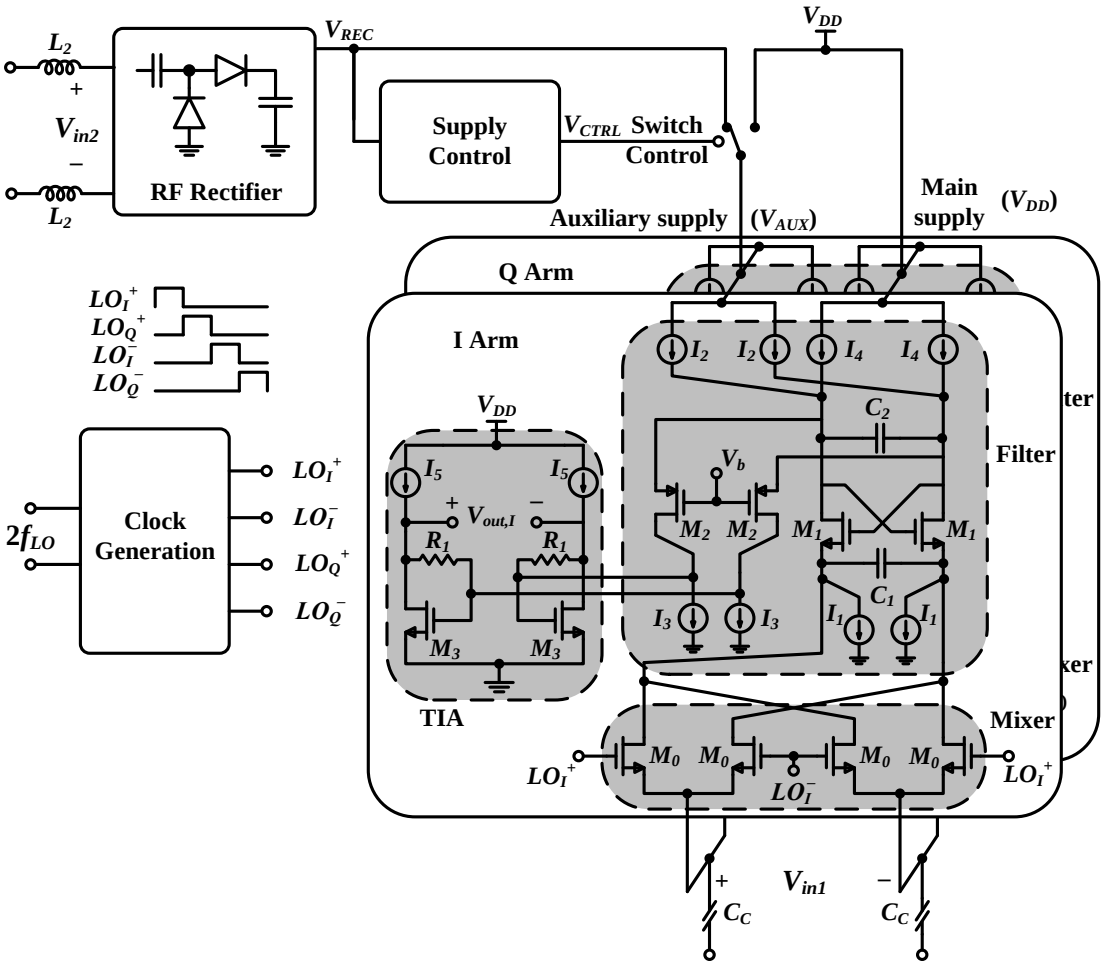


Figure 3.3: Detailed schematic for the wireless receiver.

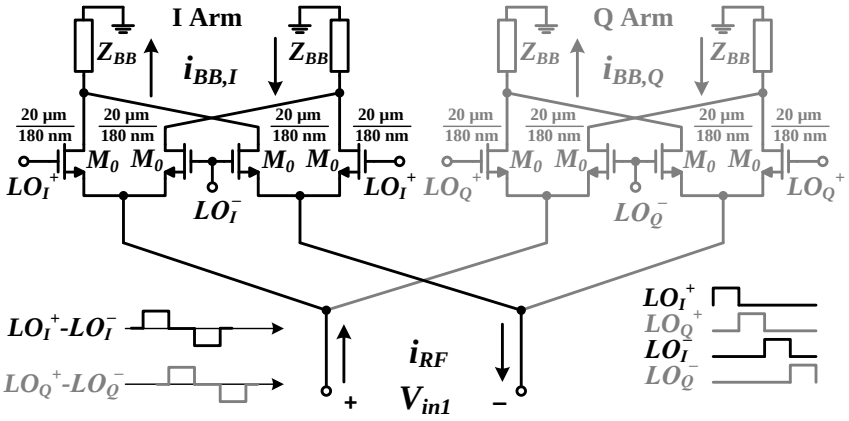


Figure 3.4: Receiver's passive mixer with baseband loads.

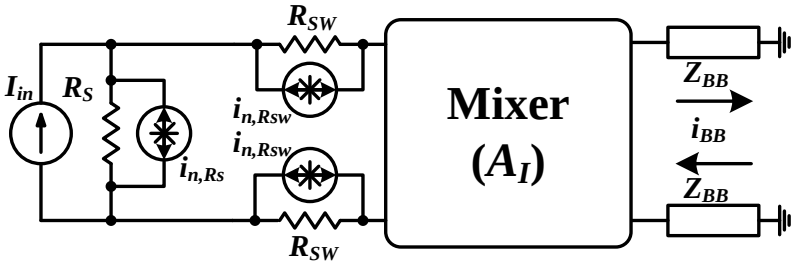
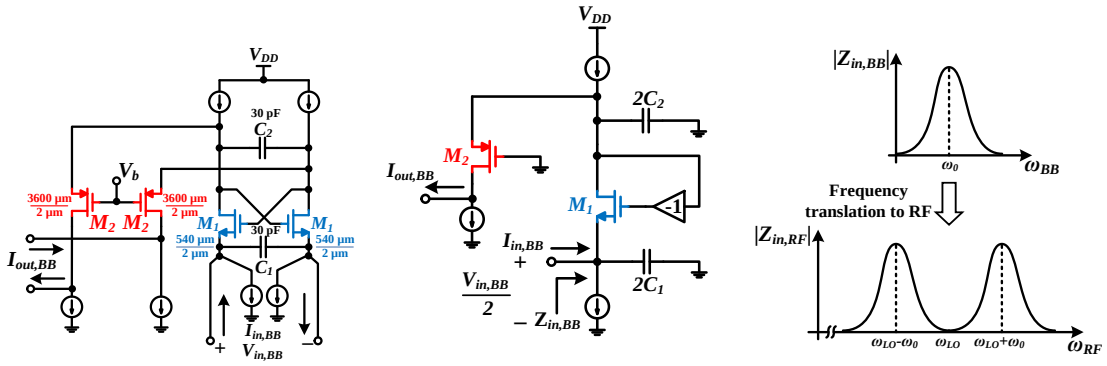


Figure 3.5: Simplified mixer noise model.

3.3.1 Passive Mixer Analysis and Design

Fig. 3.4 shows the receiver's passive mixer with I and Q baseband loads. The baseband impedance seen from the mixer (Z_{BB}) is the input impedance of the baseband filter. The mixer is clocked from 25% duty cycled four clocks shifted with $T_{LO}/4$ apart . We can consider that this passive mixer is current-driven as the input impedance of the baseband filter is relatively low (will be revisited later). Each mixer is effectively clocked by $LO_I^+ - LO_I^-$(or $LO_Q^+ - LO_Q^-$) signal shown in Fig. 3.4. Analysis of the current-driven passive-mixer is presented in [62, 63, 64, 20, 39, 26, 27, 28, 29]. Generally, the magnitude



(a) (b) (c)

Figure 3.6: Baseband low pass filter: a) schematic, b) half circuit, and c) baseband and RF input impedance.

of the I and Q baseband current is given by

$$i_{BB,I}(\omega_{BB})| = |i_{BB,Q}(\omega_{BB})| = \sum_{n=0}^{\infty} |\text{sinc}((2n+1)\pi d) \times i_{RF}((2n+1)\omega_{LO})|, \quad (3.4)$$

where i_{BB} is the current at baseband, i_{RF} is the current at RF and d is the duty cycle of the clock. For $d = 0.25$, (3.4) can be expanded to:

$$|i_{BB,I}(\omega_{BB})| = |i_{BB,Q}(\omega_{BB})| = A_{I,1}\left[i_{RF}(\omega_{LO}) + \frac{1}{3}i_{RF}(3\omega_{LO}) + \frac{1}{5}i_{RF}(5\omega_{LO}) + \cdots\right], \quad (3.5)$$

where $A_{I,1}$ is the current gain for the fundamental frequency (ω_{LO}) and equals $A_{I,1} = 2\sqrt{2}/\pi$. From (3.5), we can conclude that the current gain for the fundamental frequency is $2\sqrt{2}/\pi$ while the higher odd harmonics current gain is attenuated by $1/n$, where n is the number of the harmonic.

For the input impedance seen from V_{in1} at RF ($Z_{in}(\omega) = V_{in1}(\omega)/i_{RF}(\omega)$) and by

neglecting higher frequency harmonics, it is given by [39]:

$$Z_{in,RF}(\omega) \cong 2R_{SW} + \frac{8}{\pi^2}\big[Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})\big], \tag{3.6}$$

where R_{SW} is the on resistance for the mixer transistor.

From (3.6), we can conclude that the input impedance seen from V_{in1} at RF domain is the frequency-translated impedance from the baseband plus the switch's resistance ($2R_{SW}$).

For noise analysis, Fig. 3.5 shows a simplified model for the mixer noise. From [63, 39, 62], the output noise current from the mixer switches is given by:

$$\overline{i^2_{n,out,mixer}} = \frac{4kT \times 2R_{SW}}{(R_S + 2R_{SW})^2} A^2_{I,1} + \frac{4kT}{2R_{SW}} A^2_{I,1}\big(\frac{\pi^2}{8} - 1\big). \tag{3.7}$$

where R_S is the source impedance. (3.7) is derived under the assumption that $R_{SW} > 0$ and R_S can be neglected at higher harmonics ($\omega > \omega_{LO}$).

3.3.2 Baseband Filter Analysis and Design

In a mixer-first receiver architecture, the design of the baseband filter is a crucial task. The filter is the first active block in the receiver chain, and there is no significant gain preceding it. As a consequence, both the filter and the mixer dominates the generated noise from the receiver. However, the filter has higher flexibility in design and specifications than the mixer. The filter also should reject the out-of-band blockers to provide adequate linearity. For the previously stated reasons, the filter dominates the receiver's power budget.

Fig. 3.6a shows the filter schematic. It is a current-mode active biquad filter [30] that is implemented in a folded cascode architecture to support operation from low voltage supply (1 V) and to provide better linearity. Current-mode active biquad topology

is selected over passive RC filter because it has better selectivity and rejection without jeopardizing the linearity. The filter consists of a capacitor (C_1) and an active inductor. The cross coupled transistor M_1 implements an active inductor with C_2. Transistors M_2 are used as a current buffer. The bias current and the sizing of transistors M_1 and M_2 are designed to make $g_{m1} = g_{m2} = g_m$. The filter half circuit is shown in Fig. 3.6b. The filter has two complex poles. The filter transfer function, neglecting g_{ds} of transistors, becomes:

$$A_{I,filter} = \frac{i_{out,BB}}{i_{in,BB}} = \frac{g_m^2/(4C_1C_2)}{s^2 + (g_m/2C_1)s + g_m^2/(4C_1C_2)}. \tag{3.8}$$

The filter has $\omega_0 = g_m/\sqrt{4C_1C_2}$ and $Q = \sqrt{C_1/C_2}$. The filter response has complex poles if $Q > 1/2$ where $C_2 > 4C_1$. The simulated transfer function of the filter is shown in Fig. 3.7.

The single side input impedance of the filter, shown in Fig. 3.6b, is determined by:

$$Z_{in,BB}(s) = \frac{v_{in,BB}}{2 \times i_{in,BB}} = \frac{s/2C_1}{s^2 + (g_m/2C_1)s + g_m^2/(4C_1C_2)}. \tag{3.9}$$

The filter input impedance has an inherently bandpass response. The input impedance of the filter is shown in Fig. 3.6c along with the frequency translated impedance at RF presented in (3.6).

A simplified noise model for the filter is shown in Fig. 3.8. $R_{S,F}$ is the source impedance of the filter, and it is the output resistance of the mixer at the baseband. The

total output current noise is expressed from all thermal noise sources is given by:

$$\overline{i^2_{n,out,F}}(\omega) \cong$$

$$\overbrace{\frac{\omega^2 \times 4C_1^2/g_m^2 + 1/(g_m^2 R_{S,F}^2)}{\left(1-\omega^2 \times 4C_1C_2/g_m^2\right)^2 + \omega^2 \times 4C_2^2/g_m^2} \times 4kT\gamma g_m}^{due\ to\ M_1} +$$

$$\overbrace{\underbrace{\frac{1}{\left(1-\omega^2 \times 4C_1C_2/g_m^2\right)^2 + \omega^2 \times 4C_2^2/g_m^2} \times \overline{i^2_{n,B1}}}_{due\ to\ I_{B1}} + \underbrace{\frac{1+\omega^2 \times 4C_1^2/g_m^2}{\left(1-\omega^2 \times 4C_1C_2/g_m^2\right)^2 + \omega^2 \times 4C_2^2/g_m^2} \times \overline{i^2_{n,B2}}}_{due\ to\ I_{B2}} +}$$

$$\underbrace{\frac{\omega^2 \times \left[\omega^2 \times 16C_1^2C_2^2/g_m^4 + 4/g_m^4 \times (C_2-C_1)^2\right]}{\left(1-\omega^2 \times 4C_1C_2/g_m^2\right)^2 + \omega^2 \times 4C_2^2/g_m^2} \times 4kT\gamma g_m}_{due\ to\ M_2} + \underbrace{\overline{i^2_{n,B3}} \times \frac{|Z_{out,F}|}{|Z_{out,F}| + Z_{in,TIA}}}_{due\ to\ I_{B3}}. \tag{3.10}$$

The expression is calculated with the assumption that $g_m > 1/R_{S,F}$ and can be minimized by increasing g_m. γ is the excess noise factor, $Z_{in,TIA}$ is the input impedance for the TIA and is given by $Z_{in,TIA} = R_1/(1+g_{m3}R_1)$. $Z_{out,F}$ is the output impedance of the filter and given by $Z_{out,F} = r_{ds,M2}(1 + g_m Z_{s,M2} + Z_{s,M2}/r_{ds,M2})//(1/sC_{p,M2})$ where $r_{ds,M2}$ is the drain source resistance of M_2, $Z_{s,M2}$ is the impedance seen from the source of M_2, $C_{p,M2}$ is the parasitic capacitance at M_2. $Z_{s,M2}$ is given by

$$Z_{s,M2} = \frac{1 + Z_{s,M1}(1/r_{ds,M1} + g_m)}{1/r_{ds,M1} - g_m} // \frac{1}{2 \times sC_2} \tag{3.11}$$

where $r_{ds,M1}$ is the drain source resistance of M_1, $Z_{s,M1}$is the impedance seen from the source of M_1 and is given by $Z_{s,M1} = R_{S,F}//(1/2sC_1)$.

To summarize the filtering in the receiver chain, first, matching network is used to

pass the in-band signal and reject the out-of-band one. Second, a passive mixer is used followed by large capacitor, like typical mixer-first receiver, provides enough rejection for the out-of-band signal. Finally, the second order filter in the baseband provides additional filtering. Regarding linearity, the active filter dominates the in-band non-linearity while the passive mixer dominates the out-of-band non-linearity.

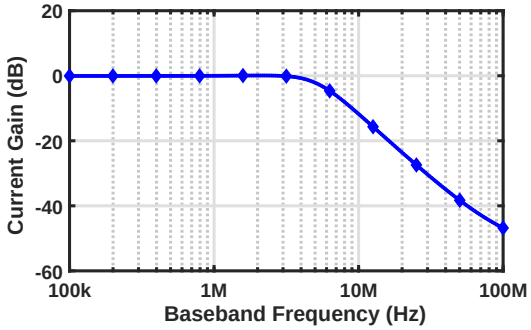


Figure 3.7: Filter simulated current gain.

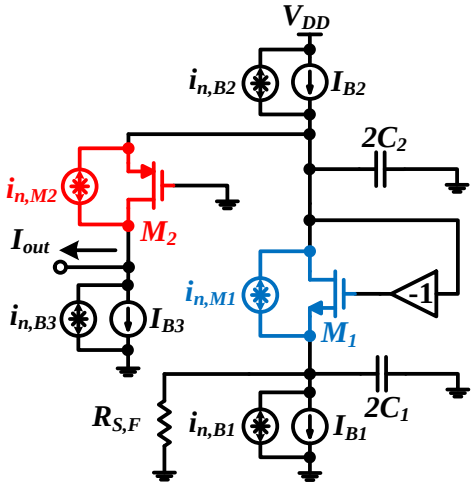


Figure 3.8: Simplified filter noise model.

3.3.3 TIA Analysis and Design

The TIA role is to convert the current signal to a voltage signal and to provide the required gain. It consists of a transistor (M_3) with a feedback resistor (R_1) as shown in Fig. 3.9. The input impedance is given by $Z_{in,TIA} = v_{in,TIA}/i_{in,TIA} = 2/g_{m3}$, and the transimpedance gain (A_T) is given by:

$$A_T = \frac{v_{out,TIA}}{i_{in,TIA}} = -2 \times \frac{g_{m3}R_1 - 1}{g_{m3}}. \tag{3.12}$$

For the noise analysis, and by assuming that R_1 is smaller than the filter output resistance, the noise from R_1 can be neglected. The total output voltage noise is given by:

$$\overline{v^2_{n,out,TIA}} \cong \frac{2}{g^2_{m3}} \times 4kT\gamma g_{m3} + \frac{2}{g^2_{m3}} \times \overline{i^2_{n,B4}}, \tag{3.13}$$

where $\overline{i^2_{n,B4}}$ is the noise generated from the bias current of the TIA.

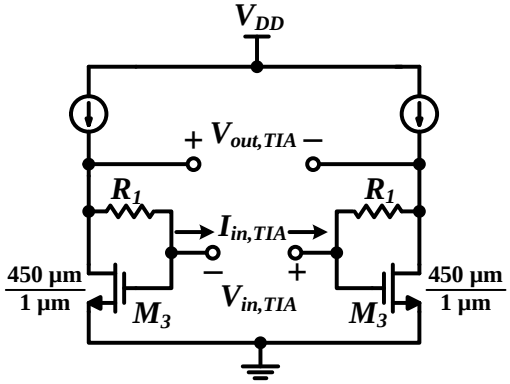


Figure 3.9: Schematic of the TIA.

3.3.4 Receiver's NF Analysis

In order to calculate the NF for the receiver's I and Q arms, we define the following current and transimpedance gains: For the mixer, the magnitude of the current gain for the fundamental frequency (ω_{LO}) is given by $|A_{I,mixer}| = R_S/(R_S + 2R_{SW}) \times 2\sqrt{2}/\pi$. The magnitude of the filter current gain yields:

$$|A_{I,filter}| = \frac{g_m^2/(4C_1C_2)}{\sqrt{\left(g_m^2/(4C_1C_2) - \omega_{BB}^2\right)^2 + \omega_{BB}^2 \times g_m^2/(4C_1^2)}}. \tag{3.14}$$

The magnitude of the transimpedance gain of the TIA is given by $|A_{T,TIA}| = 2 \times (g_{m3}R_1 - 1)/g_{m3}$.

Using these defined gains and (3.7), (3.10) and (3.13), we can get an expression for the receiver's NF and it is given by:

$$\mathrm{NF}(\omega_{BB}) = 1 + \frac{\overbrace{\overline{i_{n,out,mixer}^2} \times |A_{I,filter}|^2|A_{T,TIA}|^2}^{Mixer} + \overbrace{\overline{i_{n,out,F}^2} \times |A_{T,TIA}|^2}^{Filter} + \overbrace{\overline{v_{n,out,TIA}^2}}^{TIA}}{\underbrace{4kT/R_S \times |A_{I,mixer}|^2|A_{I,filter}|^2|A_{T,TIA}|^2}_{Output\ noise\ due\ to\ R_S}} \tag{3.15}$$

To verify the expression in (3.15), a comparison between analytical NF and simulated one is shown in Fig. 3.10. In analytical and simulated NF, noise from current sources is omitted and thermal noise is the only noise type presented. The comparison shows a good agreement between the simulated and analytical NF.

To get insight about the system blocks contribution to the NF from (3.15), mixer contribution is 61%, filter contribution is 38% and TIA contribution is < 1%. Mixer noise is primarily from switch resistance noise. In order to reduce it, we have to either use LNA

before the mixer or implement noise canceling architectures [21, 35]. Filter noise is from its active transistors and current sources.

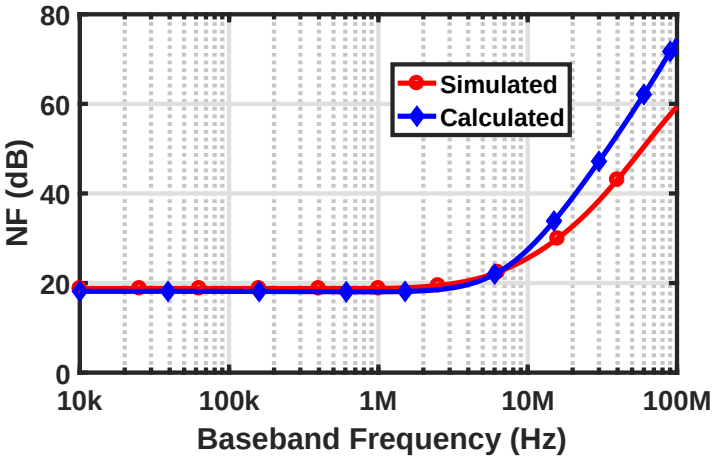


Figure 3.10: Simulated and analytical receiver's NF due to thermal noise.

3.3.5 Clock Phases Generation Circuit

A clock phases generation circuit, shown in Fig. 3.11, is implemented to generate four clocks with 25% duty cycle to test the receiver. The clocks are shifted $T_{LO}/4$ apart. Two latches are used to build the divider. After that, logic gates are used to generate the four clocks. The circuits are all implemented by static CMOS logic. The phase noise from the clock generation circuit should be minimized, especially if the receiver deals with large blockers. For this reason, the clock generation circuit is designed based on the design in [65] rather than the conventional design. Instead of combining the four outputs of the divider with each other, the design combines them with CLK and $\overline{CLK}$ as they have less jitter. Using this design approach results in better receiver's noise performance especially at large blockers where the NF can be improved by 2-3 dB. The power consumption for

the clock generation is 2.44 mW while the power consumption for the buffer is 1 mW. The area of the clock generation is 0.005 mm^2. The LO leakage at the RF input is -88 dBm.

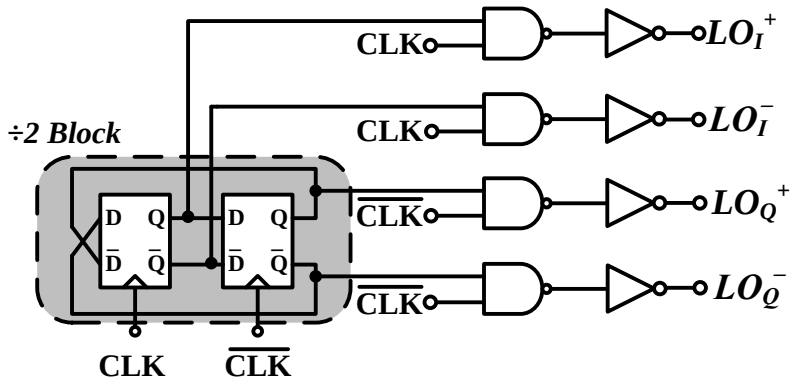


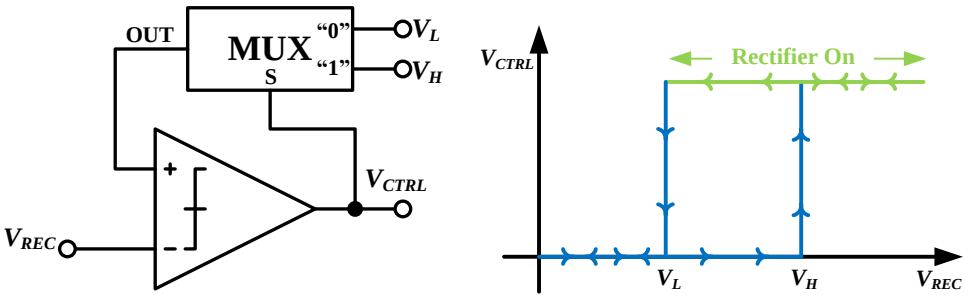
Figure 3.11: Clock generation circuit.

3.3.6 Supply Control and RF Rectifier Interaction with the Receiver

The role of the supply control is to automatically determine whether the existing blocker is able to partially supply the receiver or not. If the RF rectifier is not loaded, its output voltage increases fast with an increase in the blocker power. In this case, if it reaches the targeted supply voltage (1 V), the output voltage of the rectifier will drop less than 1 V with a load current. That means the rectifier needs to go higher than 1 V with no load to be able to support a load current and maintain a supply voltage of 1 V. In addition to that, the supply control shouldn't perform unnecessary toggle between the two modes of operation. Based on this discussion, hysteresis should be implemented in the supply control. Fig. 3.12a shows the block diagram for the supply control. It consists of a comparator and a multiplexer. The hysteresis behavior for the supply control is shown in Fig. 3.12b. The light lines represent when the receiver system partially depends on the

power harvested from the rectifier.

To further understand supply control's mechanism, top of Fig. 3.13 shows the rectifier output voltage (V_{REC}), total V_{DD} current and the current driven from the rectifier versus time. Initially, the blocker power $P_{blk} = -2$ dBm and $V_{REC} < 1.6$ V (T_H). That means that this blocker power is not able to support the load current at 1 V. At 1 μs, the blocker power is increased to -1 dBm, V_{REC} exceeds T_H, current load is connected to V_{REC}, V_{REC} is maintained at 1 V, total V_{DD} current is reduced from 430 μA to 218 μA and the current driven from the rectifier is increased from 0 μA to 212 μA. At 3 μs, the blocker power is reduced back to -2 dBm, load current is disconnected from V_{REC} and connected to V_{DD}, total V_{DD} current is increased to 430 μA, the current driven from the rectifier is reduced to 0 μA and V_{REC} is increased to 1.55 V. To elaborate more on blocker power reduction from -1 dBm to -2 dBm, the transition is zoomed in the bottom of Fig. 3.13. At blocker power P_{blk}=-1 dBm, V_{REC} is maintained at 1 V. At 3 μs, blocker power is reduced to -2 dBm. This blocker power isn't able to support the load current at 1 V, as a result, the voltage will reduce until it reaches the lower hysteresis level ($T_L \approx 0.95$ V), the load current is disconnected from V_{REC} and connected to V_{DD}. V_{REC} is increased again after the load current is disconnected. As the capacitor connected to V_{REC} is large and switching between the two mode takes around 20 ns, there is no long sequence going to be missed. The discharging time for V_{REC} is larger than the switching time and the system will switch to the other mode to maintain the supply. In case of the presence of fast large blocker, switching will not happen as the blocker needs time to charge V_{REC} to reach T_H. The value of the filter bias current from V_{REC} can be manually set along with T_L and T_H based on the available blocker power. For blocker power ≈ 0 dBm, the filter bias current from V_{REC} is set just that $V_{REC} = 1$ V. As a result, wireless receiver filter parameters will be almost the same in the two modes.



(a) (b)

Figure 3.12: Supply control: a) block diagram and b) hysteresis response.

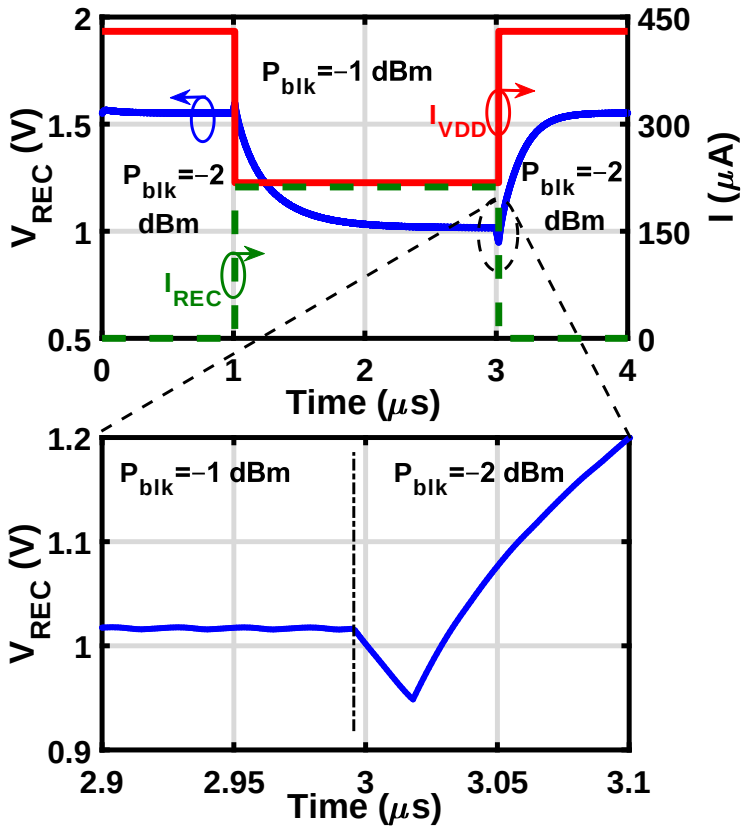


Figure 3.13: Top: V_{REC}, total V_{DD} current (solid) and the current driven from the rectifier (dashed) versus time with a change in the blocker power. Bottom: Zoomed version.

The filter dominates the power budget for the receiver core. V_{AUX} is only connected to the filter supply. The connection of the main supply and the auxiliary supply to the filter supply is shown in Fig. 3.14. If there is no large blocker, V_{REC} will be less than V_H and V_{AUX} is connected to V_{DD} as shown in Fig. 3.14a. If there is large blocker, V_{REC} will be higher than V_H and V_{AUX} is connected to V_{REC} as shown in Fig. 3.14b. In this case, the power consumption from the main V_{DD} is reduced. V_{AUX} will be connected back to V_{DD} if V_{REC} become less than V_L. V_L is determined by specifying the lower supply voltage the circuit can operate from which is typically less than 100 mV lower than the supply voltage. In this design, we made it 50 mV less than the supply voltage which is 0.95 V. V_H is determined by evaluating the output voltage of the RF rectifier V_{REC} in unloading condition with input blocker power large enough to supply the circuit need, which is -1 dBm in this design. The turn-on power of the RF rectifier, which is -1 dBm in this design, can be controlled by V_H. The turn-on power of the RF rectifier, which is -1 dBm in this design, can be controlled by V_H. There is a trade-off in selecting the turn-on point for the RF rectifier. Selecting low (high) blocker power level for turn on will result in lower (higher) RF rectifier efficiency but with higher (lower) blocker availability. The simulated power supply rejection ratio (PSRR) is 60 dB. Adding an LDO to the system will provide clean supply for the filter; however, it will reduce the power conversion efficiency as there will be power consumed due to the drop out voltage of the LDO.

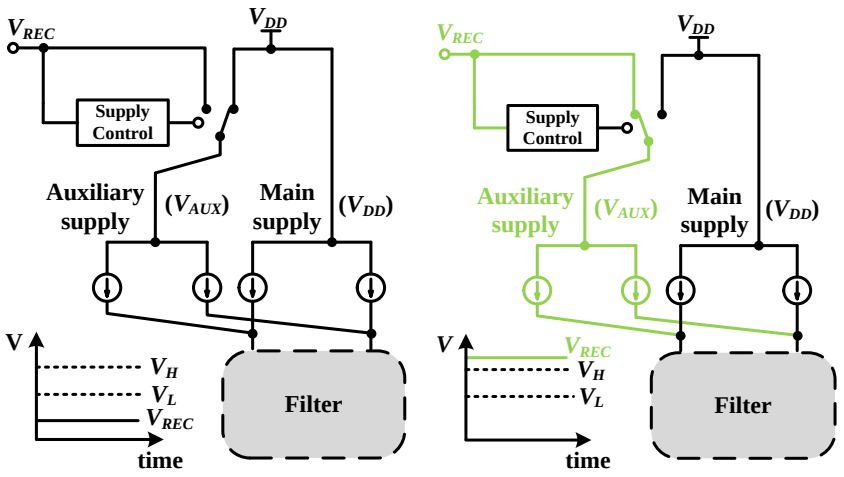


Figure 3.14: Filter supply connection with V_{DD}, V_{AUX} and V_{REC}: a) in case of no large blocker and b) in case of large blocker.

3.4 Proposed Differential RF Rectifier with Integrated Passives

RF energy harvesting consists of an on-chip matching network and a differential cross-coupled [66] two-stage RF rectifier as shown in Fig. 3.15. Two series inductors, as shown in Fig. 3.15, are used to match the RF rectifier to the out-of-band frequency range. Differential design is chosen due to the balanced nature of the wireless receiver design. The RF energy harvesting should present high input impedance for in-band signals (not to affect the matching of the receiver and Noise Figure) and 50 Ω input impedance for the out-of-band frequency range of the blockers. As a result, the RF rectifier can work simultaneously with the receiver without hugely affecting its characteristics. In simulation, adding the RF rectifier to the wireless system reduces the gain by 0.6 dB and increases the NF by 1.4 dB.

To elaborate more on the co-integration of the RF rectifier and the receiver, Fig. 3.16 shows the frequency response at the input of the receiver and the RF rectifier. At signal

band, most of the signal goes to the receiver while in the blocker band most of the blocker goes to the RF rectifier. At blocker band, L_1 & C_C form a high impedance even if the translated input impedance of the mixer approaches R_{SW} at blocker band. On the other hand, L_m & C_m form a low impedance so most of the blocker signal goes to the RF rectifier.

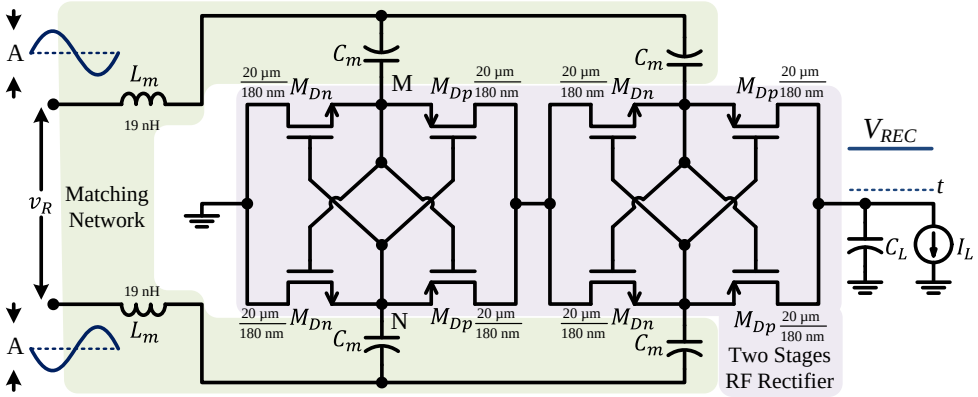


Figure 3.15: Proposed RF energy harvesting front end comprised of matching network and RF rectifier.

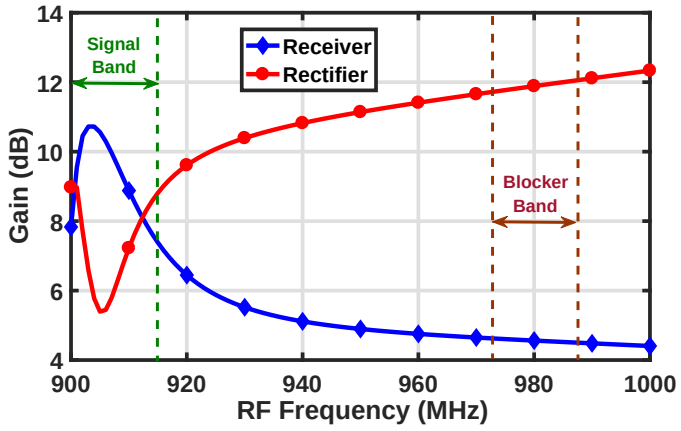


Figure 3.16: RF gain at the input of the receiver and the rectifier.

3.5 Design Procedure

To start the design of the wireless system, we need to identify the signal band blocker band to harvest the energy from. The blocker band should be at least 40 MHz away from the signal band not to affect the receiver performance. After selecting the bands, the matching network for the signal and blocker band can be designed.

The next step is to design the mixer. The sizing of the mixer is critical. Ideally, the mixer switches should be large enough to support a low switching resistance; however, a large mixer switch would result in high clock buffer power consumption. The mixer should be designed so that the sum of the filter input impedance and the mixer switch should be $< 50\ \Omega$. The filter is designed by selecting the baseband filter cut-off frequency and then using (3.8) to calculate g_m and C values. g_m can be designed based on the power consumption budget and the noise requirement. Finally, TIA can be designed based on the required amount of gain.

3.6 Experimental Results

The receiver system is implemented in 180 nm CMOS technology. The receiver operates at 900 MHz. A die micrograph for the chip is shown in Fig. 3.17. The die area is $5.3\ \mathrm{mm}^2$ and the effective receiver system area with passives is $1\ \mathrm{mm}^2$. The receiver system is designed to harvest energy from out-of-band blocker 80 MHz away from the wanted signal. 80 MHz frequency separation is selected as a trade-off between filter blocker rejection and the ability of operating the receiver and the RF rectifier from the same antenna at 900 MHz band. The rectifier is also able to harvest from blockers 60 MHz away where the downlink for GSM exists. In addition to that, if the receiver operates at 1.99 GHz, we will find blockers, as large as 0 dBm, 80 MHz away from operating frequency [18, 59]. However, in this case, the matching network should be slightly modified. All measure-

ment results are for the receiver characterization with the RF rectifier. The testing setup is shown in Fig. 3.18 and the test board is shown in Fig. 3.19. Two RF sources are applied at the RF input, RF source applied at the clock input and the output is connected to spectrum analyzer. Fig. 3.20 shows the measured, simulated and analytical receiver $|S_{11}|$. It shows the matching at 900 MHz for the signal of interest and also the matching at 980 MHz to harvest energy from the out-of-band blockers. For small signal characterizations of the receiver, Fig. 3.21 shows the measured and simulated conversion gain of the receiver versus the baseband frequency. The receiver gain is 41.5 dB and the $3-$dB cut-off frequency is 500 kHz. The attenuation at 80 MHz is 78 dB. Fig. 3.22 shows the measured and simulated receiver NF. The receiver NF is 19.5 dB. Measurement for the receiver's linearity performance is shown in Fig. 3.23. Fig. 3.23a shows the measured in-band IIP3. It is measured by applying two tones at 900.8 MHz and 901.3 MHz. The in-band IIP3 is -11 dBm. The measured out-of-band IIP3 is shown in Fig. 3.23b. It is measured by applying two tones out-of-band and sweep the offset frequency up to 100 MHz. The out-of-band IIP3 is $+5$ dBm at 100 MHz offset. The two tones input power is -43 dBm at 1 MHz separation and -33 dBm at 100 MHz separation. Higher IIP3 can be obtained by increasing the receiver power consumption.

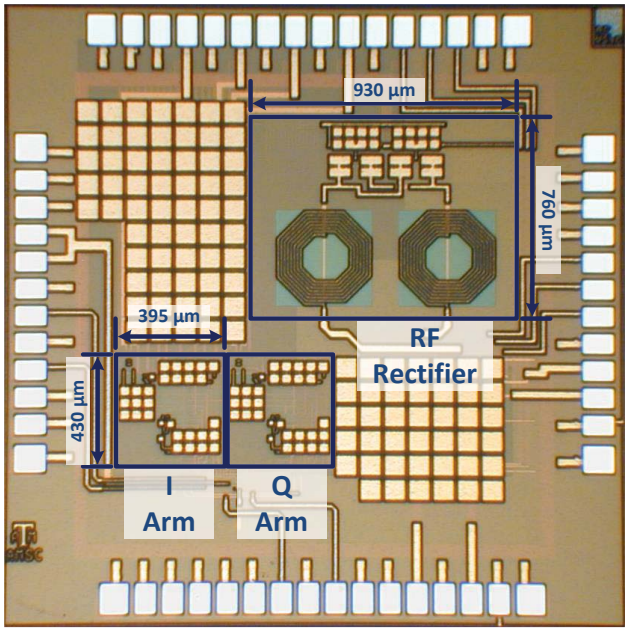


Figure 3.17: Die micrograph.

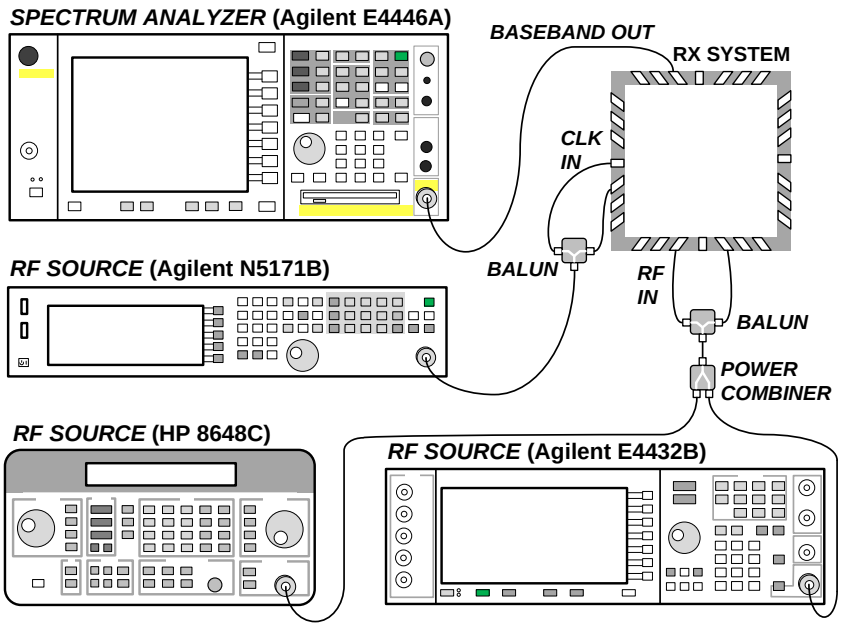


Figure 3.18: Wireless receiver system testing setup.

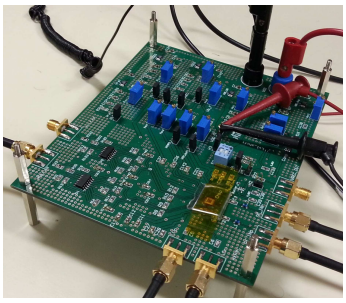


Figure 3.19: Testing board.

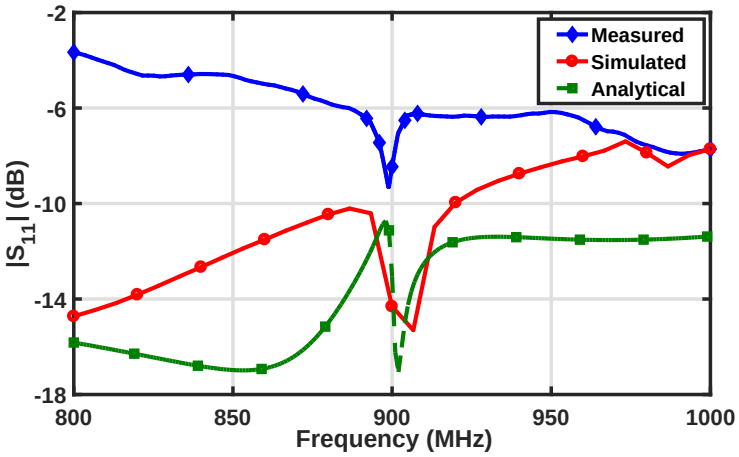


Figure 3.20: Measured, simulated and analytical receiver $|S_{11}|$.

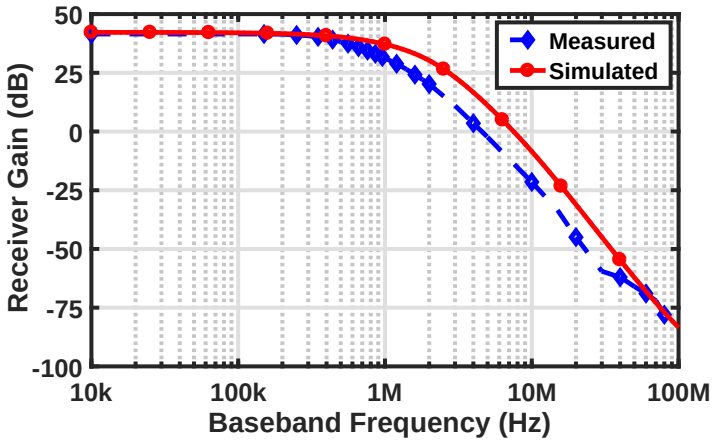


Figure 3.21: Measured and simulated receiver voltage gain.

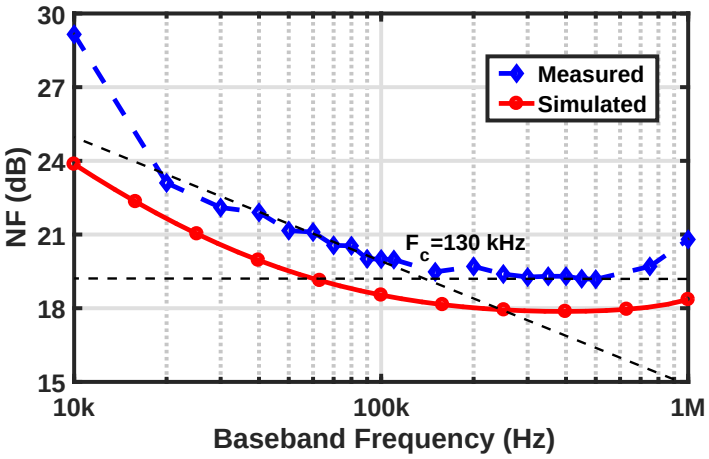
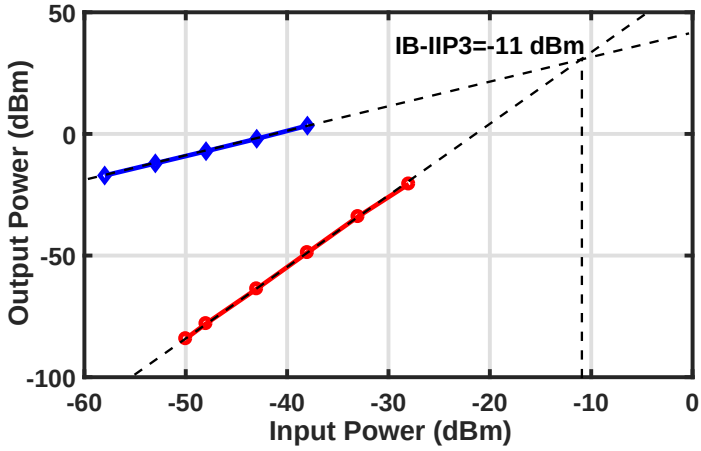
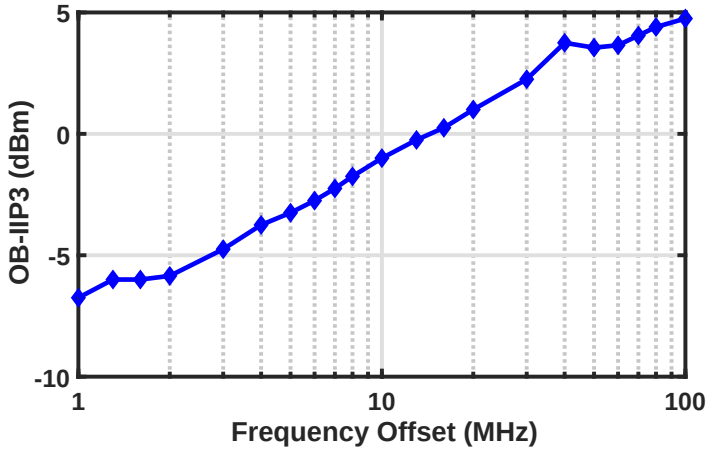


Figure 3.22: Measured and simulated receiver NF.



(a)



(b)

Figure 3.23: Measured linearity performance for the receiver a) in-band (IB) IIP3 and b) out-of-band (OB) IIP3.

As a complete characterization for the receiver system, measurements are given for the system response for large blockers, from which the receiver can harvest energy. Fig. 3.24 shows the measured and simulated receiver gain versus the blocker power. The gain drops from 41.5 dB to 38 dB at 0 dBm blocker 80 MHz away from the signal of interest. Fig. 3.25 shows the measured and simulated receiver NF versus the blocker power. The

NF increases from 19.5 dB to 22 dB at 0 dBm blocker. The reason for the NF increase is the gain compression and the reciprocal-mixing where the large blocker mixes with the LO divider's output phase noise. In simulation, using clock with reasonable on-chip LO performance would further degrade the NF by 0.6 dB in the existence of 0 dBm blocker. The highest blocker power we have applied to the receiver system is 3 dBm. Fig. 3.26 shows the output power from the RF rectifier at 1 V and PCE of the rectifier versus blocker power. The RF rectifier is able to harvest 212 μW at -1 dBm blocker. The ripples on RF rectifier output is filtered by on and off chip capacitors. The on-chip capacitor is 50 pF and the off-chip capacitor is 1.1 nF. The ripples on V_{REC} due to two tones at 0 dBm with 20 MHz frequency separation, in simulation, is 4.8 mV. Fig. 3.27 shows the measured RF rectifier output voltage (V_{REC}), total V_{DD} current and the current driven from the rectifier versus the blocker power. The plot shows how the voltage is developed on the output rectifier and shows the power saving mode starts at -1 dBm. In this work, with the available input power and the dc output current requirements, if the dc output voltage is not sufficient for the receiver's filter to operate, around 1 V, the rectifier don't provide dc current and the receiver entirely operate from battery. An adaptive control for the dc current extracted from the RF rectifier can be incorporated to utilize power from lower input power levels. This can be a future extension to this work.

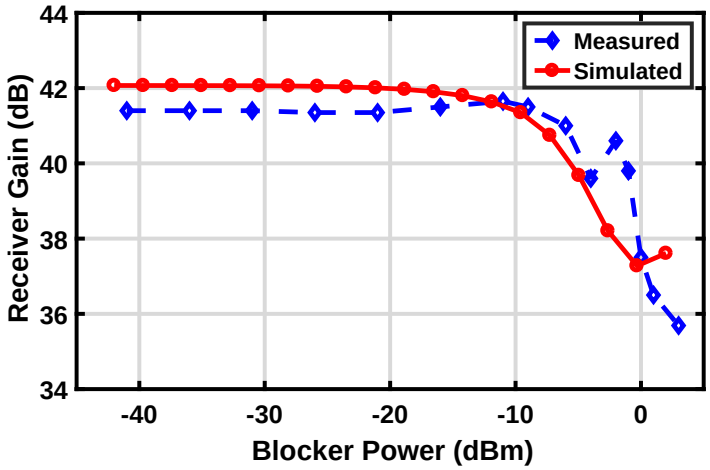


Figure 3.24: Measured and simulated receiver gain versus blocker power.

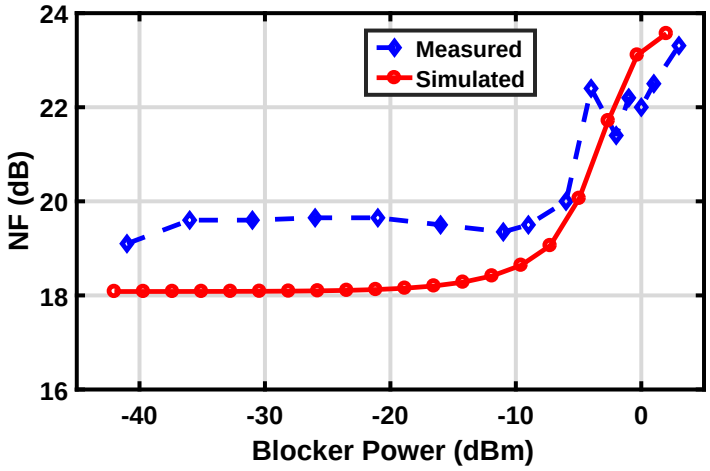


Figure 3.25: Measured and simulated receiver NF versus blocker power.

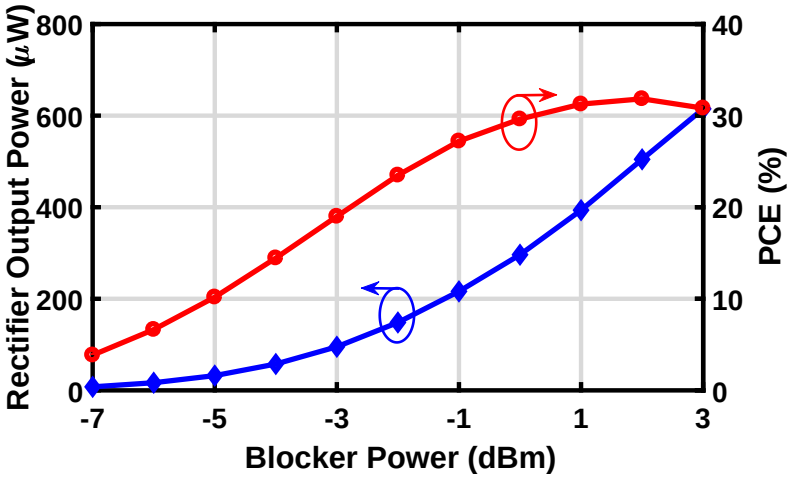


Figure 3.26: Measured rectifier output power and PCE versus blocker power.

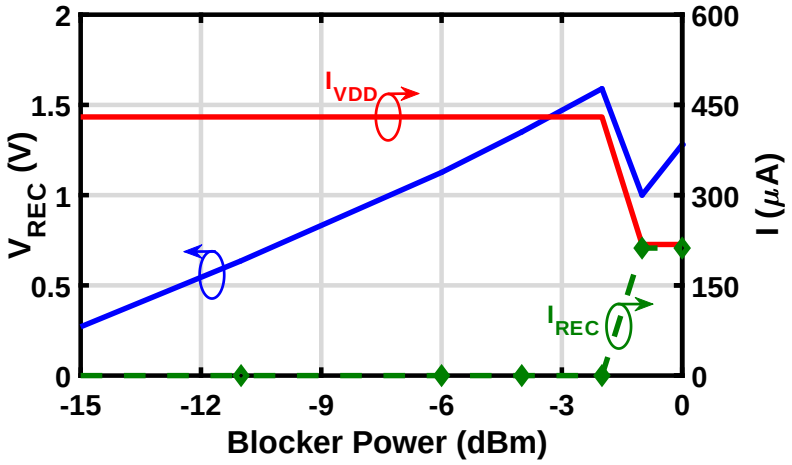


Figure 3.27: Measured V_{REC}, total V_{DD} current (solid) and the current driven from the rectifier (dashed) versus blocker power.

The receiver core (mixer, filter and TIA) power consumption is 430 μW from 1 V supply. In the presence of -1 dBm blocker, the RF rectifier is able to harvest 212 μW. In

this case, the power consumed from the main V_{DD} will drop to 218 μW. That means 49% reduction in the power budget. Fig. 3.28 shows the power distribution for the receiver core on a pie chart. In case of a -1 dBm blocker, the left part of the chart (Filter V_{AUX}) can be saved. Table 3.1 shows receiver blocks noise contribution.

The receiver is tested with Silicon Labs transceiver module (Si4463) for modulated signal reception. The Silicon Labs module operates as transmitter with FSK modulation. Fig. 3.29 shows the received signal at the baseband (upper trace) with the demodulated stream of data in the lower trace. The receiver is used to verify the operation of the energy harvesting combiner in [67]. The receiver sensitivity is -87 dBm while the receiver gain drops $3-$dB when the input power is 0 dBm. The receiver dynamic range (DR) is 87 dB.

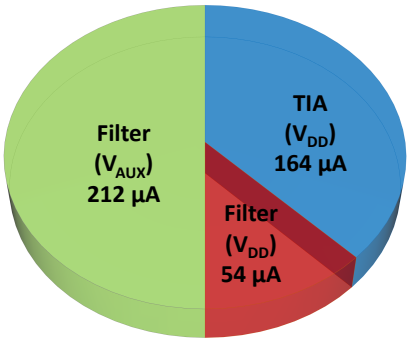


Figure 3.28: Receiver's core power distribution.

Table 3.1: Receiver Blocks Noise Contribution

	R_s	Mixer	Filter	TIA
Noise Contribution (%)	5.3	4.6	82.8	7.3

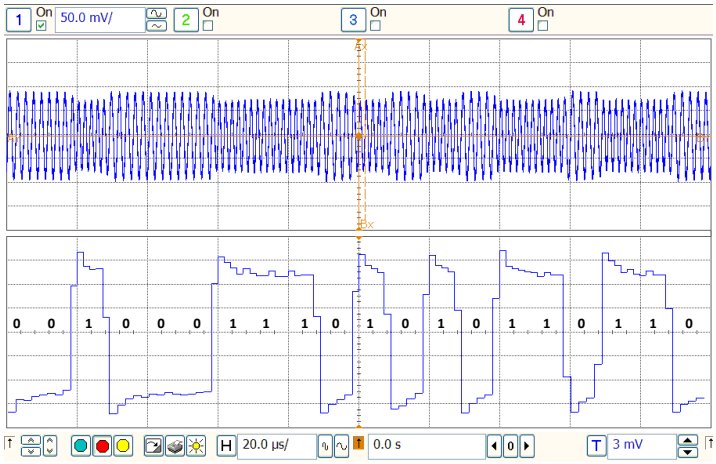


Figure 3.29: Demodulation of FSK data transmitted from Si4463.

Table 3.2 summarizes the performance comparison for the RF rectifier with the state-of-the-art designs. The RF rectifier performance shows its competitiveness while it is implemented on the largest feature size technology. A performance summary and comparison for the whole system with the state-of-the-art designs is shown in Table 3.3. The proposed receiver system is uniquely able to harvest energy from the blocker during the normal receiver operation and from the same antenna. The receiver core has the lowest power consumption especially in the presence of -1 dBm blocker. On the other hand, the NF is high but that can be tolerated for the sake of ultra low power consumption as in IoT applications.

Table 3.2: RF Rectifier Performance Summary and Comparison with the State-of-the-Art

	Masuch [41]	Rajavi [46]	Abouzied [48]	Wang [55]	Moghaddam [56]	Kang [57]	This Work
RF Frequency (MHz)	2400	1800	915	900	953	2400	900
Peak PCE @ Power Level	15.9% @ 0 dBm	11%† @ 9 dBm	27% @ -2 dBm	47% @ 0 dBm	70% @ 5 dBm	37% @ -23 dBm	32% @ 2 dBm
CMOS Technology	130 nm	40 nm	180 nm	40 nm	130 nm	65 nm	180 nm
Sensitivity (dBm)	-12.6	-	-14.8	-15	-	-30.7	-1

† Estimated

3.7 Conclusion

An ultra low power RF wireless receiver with an RF blocker energy harvesting aid is presented. The receiver operates at 900 MHz ISM band. Using the same antenna and during the normal operation, the receiver system is able to harvest energy from a large blocker 80 MHz away from the band of interest. The receiver is implemented in 180 nm CMOS technology and is operating from 1 V supply. In the presence of a large blocker, the receiver power consumption is reduced by 49%. The maximum PCE for the RF energy harvesting is 32% while the input is shared between the receiver and the harvesting unit. To the best of authors' knowledge, this is the first RF wireless receiver that is able to harvest energy from out-of-band blockers simultaneously with in-band signal reception using the same antenna for all power levels. Due to its ultra low power consumption, the receiver is very attractive for IoT applications.

Table 3.3: Performance Summary and Comparison with the State-of-the-Art

	Khan [8]	**Selvakumar [11]**	**Lin [37]**	**Lin [38]**	**Homayoun [39]**	**Masuch [41]**	**Rahman [43]**	**Alpman [44]**	**Salazar [45]**	**This Work**
Architecture	Gilbert Active Mixer-First	QLNA	RF-to-BB-Recycled Front-End	Gain-Boosted Mixer-First	Transformer + Mixer-First	Mixer-First+ RF EH	FT+ M. Noise-Canc.	Mixer-First Wake-Up Rx	Dual Uncertain-IF	Mixer-First+ Blocker-Harvesting
RF Frequency (MHz)	2400	2400	900	1500	5000	2400	2400	2400	2400	900
Gain (dB)	37	55.8	48	38	48	18.7	20.6	37	70	41.5
NF (dB)	28	15.5	8.7	2.9	5.3	16.25	6.55	27$^{\beta}$	27	19.5
0 dBm Blocker NF @ Freq. Offset	NA	NA	NA	13.5 @ 80 MHz	NA	NA	NA	NA	NA	22 @ 80 MHz
OB-IIP3 @ Freq. Offset	NA	NA	-20.5 @ 10 MHz	+13 @ 100 MHz	+2.6 @ NA	NA	NA	NA	NA	+5 @ 100 MHz
RF Energy Harvester	✗	✗	✗	✗	✗	✓	✗	✗	✗	✓
Concurrent E.H. Operation	NA	NA	NA	NA	NA	✓ Only for low power	NA	NA	NA	✓ For all power levels
PCE @ Power Level	NA	NA	NA	NA	NA	15.9% @ 0 dBm	NA	NA	NA	30% @ 0 dBm 32% @ 2 dBm
Supply (V)	1	0.8	0.5	0.7, 1.2	1	1	0.7	0.95	0.5	1
Power (mW)	0.87	0.6†	1.15†	11	11.6	0.42	0.194$^{\Delta}$	0.095	0.099	0.22$^{\diamond}$/0.43*+ 3.44 CLK Gen.
CMOS Technology	65 nm	130 nm	65 nm	65 nm	65 nm	130 nm	65 nm	14 nm	65 nm	180 nm

† Including VCO $^{\Delta}$ Mixer Power $^{\beta}$ Estimated $^{\diamond}$ Receiver core (Mixer+Filter+TIA) power in the presence of -1 dBm blocker

* Receiver core (Mixer+Filter+TIA) power if there is no large blocker

4. HIGHLY LINEAR ENERGY EFFICIENT WIRELESS RECEIVER USING VCO-BASED AMPLIFIER AND CLOCK RECYCLING

4.1 Introduction

Recent trends in wireless connectivity shows the need to design and implement highly linear wireless systems due to increased spectrum congestion as the number of connected devices increase. On the transmitter side, non-linearity deteriorates the performance and increases spectral regrowth. This make it hard for the system to pass the spectral mask requirement. On the receiver side, non-linearity results in gain desensitization and compression. Researchers in this area [8, 14, 12, 9] have recently investigated many techniques to reduce power consumption for the wireless receiver while maintaining reasonable noise performance and linearity. Nevertheless, novel ideas need more exploration so the linearity can be improved.

Notably, VCO-based amplifiers have caught designers' attention recently. In [68], a fourth-order low pass filter is implemented using Current Controlled Oscillators (CCO) to replace the integrator. The power supply can be reduced as a benefit of using a CCO as an integrator. In [69], active Unity-Gain Bandwidth fourth−order filter is introduced by using a VCO-based amplifier. These designs show the ease of implementing the amplifier with zero compensation. [70] presents design procedures on how to optimize the charge pump design in a VCO-based amplifier.

In this section, a low power wireless receiver is implemented using a VCO-based amplifier. Although the design incorporates VCOs for amplifiers, it also recycles the clock from those VCOs to clock the RF mixer circuit.

This section is organized as follows: Subsection 4.2 has background information about VCO-based amplifiers. Subsection 4.3 presents the receiver architecture and the

proposed clock recycling technique with analysis. Subsection 4.4 introduces the receiver building blocks. Subsection 4.6 presents the results. Finally, Subsection 4.7 summarizes the major achievements with concluding remarks.

4.2 Background: VCO-Based Amplifiers

The implementation and use of a VCO-based amplifier and OTA have been explored recently [68, 69, 70]. The main idea that the VCO-based amplifier leverages the large gain (ideally infinite at DC) between the VCO output phase and input voltage. The relation is given by:

$$\frac{\phi_{out}(s)}{v_{in}(s)} = \frac{\mathrm{K_{VCO}}}{s}, \tag{4.1}$$

where $\mathrm{K_{VCO}}$ is the VCO constant. From (4.1), we can observe that the VCO can be used as an amplifier with infinite gain at DC and at a unity gain frequency of $\mathrm{K_{VCO}}$. However, in order to use it as amplifier, the output phase needs to be converted to voltage. This can be done by using the phase detector (PD) followed by a charge pump (CP). Differential implementation for the VCO-based amplifier is shown in Fig. 4.1. It consists of two VCOs followed by phase detector that compares the output from the two VCOs with different polarities. Finally, there is a charge pump with load capacitance $\mathrm{C_L}$. The system has two poles at zero, one from the VCO and the other one from the charge pump. In order to make the system stable at the closed loop, zero is added using $\mathrm{R_C}$ and $\mathrm{C_C}$. The open loop transfer function is given by:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{4\pi \mathrm{K_{VCO}K_{PD}I_{CP}}\big(1 + s\mathrm{R_C C_C}\big)}{s^2\mathrm{C_C}\big(1 + s\mathrm{R_C C_L}\big)}, \tag{4.2}$$

where $\mathrm{K_{PD}}$ is the phase detector gain and $\mathrm{I_{CP}}$ is the charge pump gain. The amplifier behaves as Type-II 3^{rd}-order phase-locked loop with unity feedback.

The VCO-based amplifier has advantages. It moves the processing from voltage do-

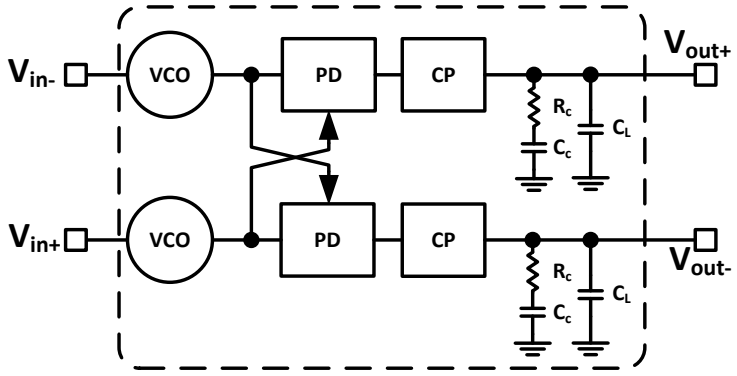


Figure 4.1: Implementation of VCO-based amplifier.

main to time domain with rail to rail operation. That means a higher dynamic range with better linearity especially at deep sub micron CMOS technology. The compensation can be implemented easily with zero using $\mathrm{R_C}$ and $\mathrm{C_C}$.

4.3 Proposed Receiver Architecture and Clock Recycling Technique

Fig. 4.2 shows the block diagram for the wireless receiver. In order to achieve high linearity, a mixer-first architecture is used. In the mixer-first architecture, the mixer is a passive device with a rail to rail clock. This makes the linearity of the baseband amplifier affects the total receiver linearity. As a solution, the VCO-based amplifier is used in the baseband due to its high linearity. The receiver has capacitors at the baseband input ($\mathrm{C_{IN}}$) right after the mixer to filter large out-of-band blockers. The receiver has a clock recycling block. Its role is to generate the required clock for the mixer circuit. Because the receiver features a VCO-based amplifier, VCOs in the baseband amplifier can be used to clock the mixer circuit. However, processing should be applied to the clocks before it can be used. The VCO can operate at the RF frequency of the receiver because the VCO frequency is independent of the amplifier unity gain frequency. The block is named clock recycling since it recycles the clocks from the baseband amplifier VCOs. This clock

recycling reduces the power consumption for the whole receiver; thus, it is unnecessary to to implement a separate VCO to clock the mixer circuit. The following subsection will discuss the idea and implementation of clock recycling.

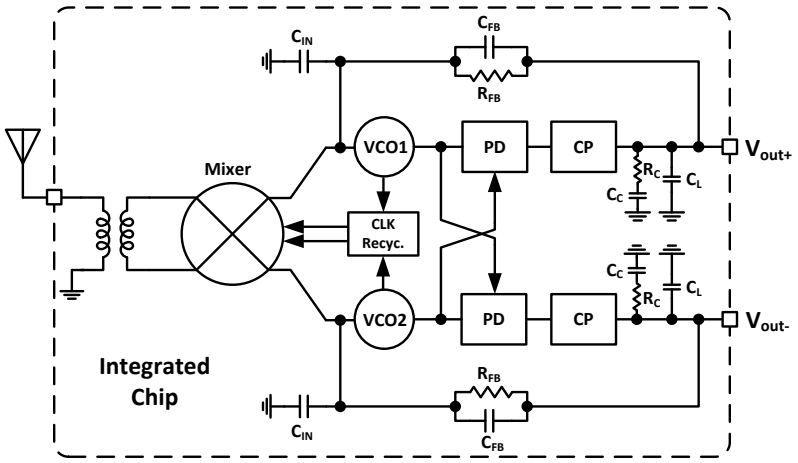


Figure 4.2: Proposed receiver architecture.

4.3.1 Clock Recycling Idea

In the VCO-based amplifier, the VCO frequency can be selected freely as long as it satisfies $f_{VCO} > 10 \times f_u$. That means it needs to be 10 times higher than the amplifier unity gain frequency. Because the VCO-based amplifier operates like phase locked loop (PLL), the two VCOs will be locked to each other when there is no input signal applied and they will have the same operation frequency, which is the nominal frequency. However, when an input signal applied is to the amplifier, the frequency of the two VCOs start to change. Fig. 4.3 shows the two VCO frequencies when a sinusoidal signal is applied at the input. The oscillators' frequencies start to deviate from the nominal frequency which is 920 MHz in this case. However, the average of the two oscillation frequencies remain

the same as the nominal frequency at all times. Because the two oscillation frequencies change with time, they cannot be used to clock the mixer circuit. On the other hand, if we can generate a signal with the average of the two frequencies, this signal can be used to clock the mixer circuit.

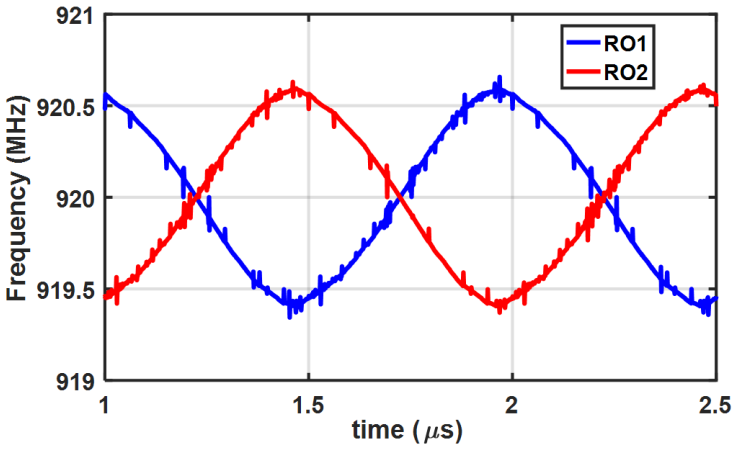


Figure 4.3: Amplifier's VCO frequencies versus time when sinusoidal signal is applied at the input.

To elaborate more on the idea, Fig. 4.4 shows the clocks for the two oscillators in different cases. The graph shows the case where VCO1 is leading and the other case where VCO2 is leading. The bottom green line of the figure shows the targeted frequency average signal that needs to be generated to clock the mixer circuit. One method to generate the average frequency is the phase interpolator (PI) [71], which can generate the targeted average frequency signal; nevertheless, using a phase interpolator has its drawbacks. First, the phase interpolator will not operate properly if the phase difference between the two clocks varies with time. Second, the phase interpolator circuit has different weights for the two clocks depending on which one is leading. This means the phase interpolator

will not operate if the two clocks exchange the lead. This can be solved by adding extra circuitry; however, the complexity will be higher, and the power consumption will increase.

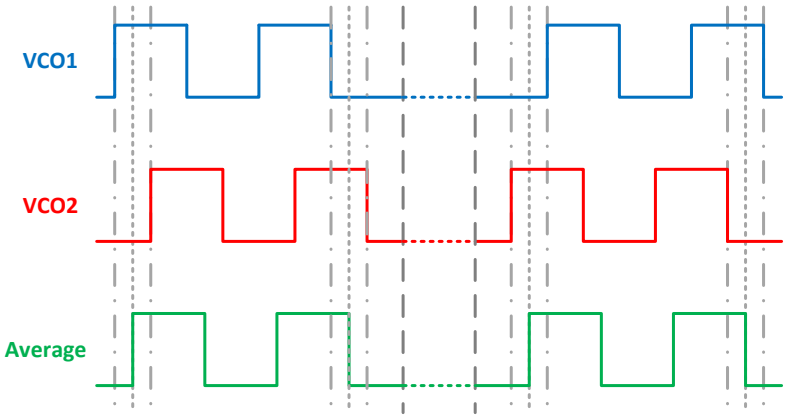


Figure 4.4: VCOs clocks waveform in different cases and the targeted frequency average signal.

To overcome the previous drawbacks, the proposed solution is to use an AND gate between the two clocks. This approach results in a response much like the response for the targeted average frequency signal. It also can be implemented with a simple circuit and low power consumption. The following subsection will elaborate more on this idea and its analysis.

4.3.2 Clock Recycling Implementation and Analysis

As mentioned, generation of a clock with a frequency that is the average of two VCO clocks can be implemented using an AND gate. For two VCOs, when the input voltage is zero, the VCOs will oscillate at the nominal oscillation frequency. We can consider the output phase from both VCOs in this case as $\phi_\circ$. If there is an input signal applied, it will

be applied differentially to the two VCOs. In this case, we can consider the output phase for VCO1 and VCO2 as ϕ_1 and ϕ_2, respectively. ϕ_1 is given by:

$$\phi_1 = \phi_\circ + {}^{\Delta\phi}/_{2}, \tag{4.3}$$

and ϕ_2 is given:

$$\phi_1 = \phi_\circ - {}^{\Delta\phi}/_{2}, \tag{4.4}$$

where $\Delta\phi$ is the differential phase difference that results from an applied differential signal. Fig. 4.5 shows ϕ_1, ϕ_2, $\phi_\circ$ and ϕ_{AND} which is the AND output from ϕ_1 and ϕ_2. From the waveform, the rising edge is always at:

$$\phi_\circ - \frac{|\Delta\phi|}{2} = 2k\pi, \tag{4.5}$$

while the falling edge is always at:

$$\phi_\circ + \frac{|\Delta\phi|}{2} = (2k+1)\pi. \tag{4.6}$$

A function that has an abrupt transition at $(2k+1)\pi$ is the saw tooth function, which can be expressed as:

$$\mathrm{St}(\theta) = \frac{j}{\pi} \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \frac{1}{m} e^{jm(\theta+\pi)}. \tag{4.7}$$

The output of the AND gate can be expressed as:

$$\phi_{AND} = \mathrm{St}\left(\phi_\circ + \frac{|\Delta\phi|}{2}\right) - \mathrm{St}\left(\phi_\circ - \frac{|\Delta\phi|}{2} + \pi\right) - \frac{|\Delta\phi|}{\pi}. \tag{4.8}$$

By substituting with (4.7) in (4.8), we get:

$$\phi_{AND} = \frac{j}{\pi} \sum_{\substack{m=-\infty \\ m \neq 0}}^{\infty} \left(\frac{1}{m} e^{jm(\phi_\circ + |\Delta\phi|/2)} - \frac{1}{m} e^{jm(\phi_\circ - |\Delta\phi|/2 + \pi)} \right) - \frac{|\Delta\phi|}{\pi}, \tag{4.9}$$

which can be simplified to:

$$\phi_{AND} = \frac{2}{\pi} \sum_{\substack{m=-\infty \\ m \neq 0}}^{\infty} \left(\frac{1}{m} e^{jm(\phi_\circ + \pi/2)} \times \sin\left(\frac{m\pi}{2}(1 - \frac{|\Delta\phi|}{\pi})\right) \right) - \frac{|\Delta\phi|}{\pi}. \tag{4.10}$$

At fundamental frequency, (4.10) can be simplified to:

$$\phi_{AND}(f_{LO}) = \frac{4}{\pi} \sin(\phi_\circ) \cos(\frac{|\Delta\phi|}{2}). \tag{4.11}$$

If $\Delta\phi$ is small, we will get:

$$\phi_{AND}(f_{LO}) = \frac{4}{\pi} \sin(\phi_\circ). \tag{4.12}$$

That means that the output from the AND gate will approach the nominal oscillation frequency if the output phase variation ($\Delta\phi$) is small.

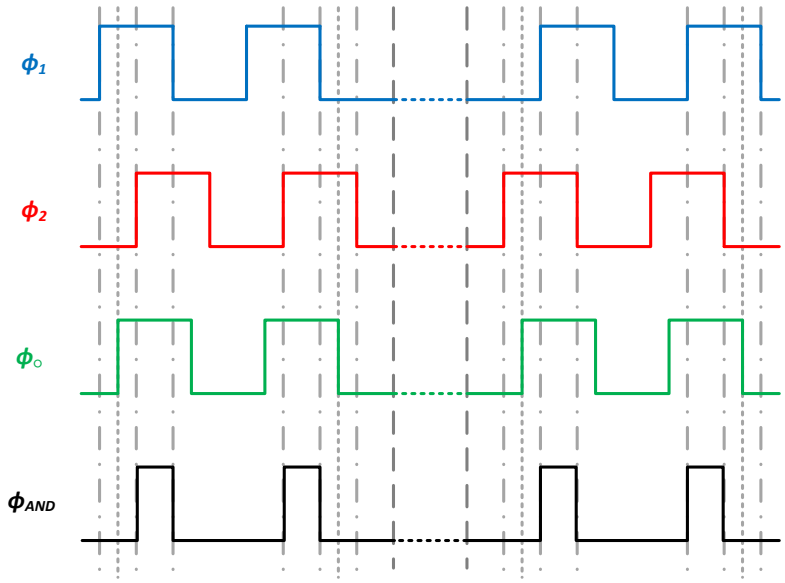
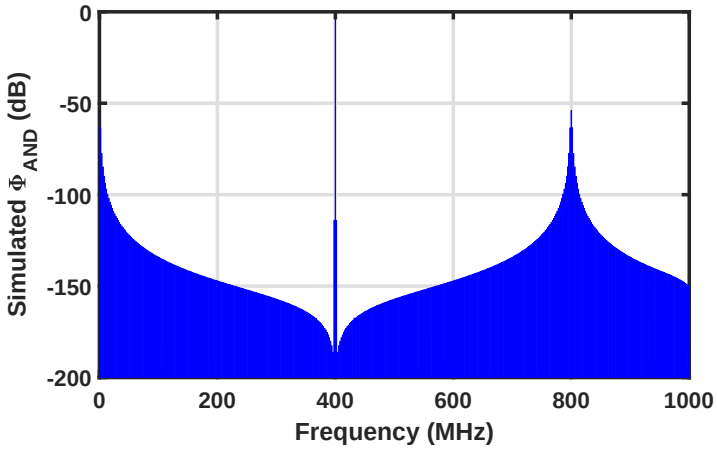
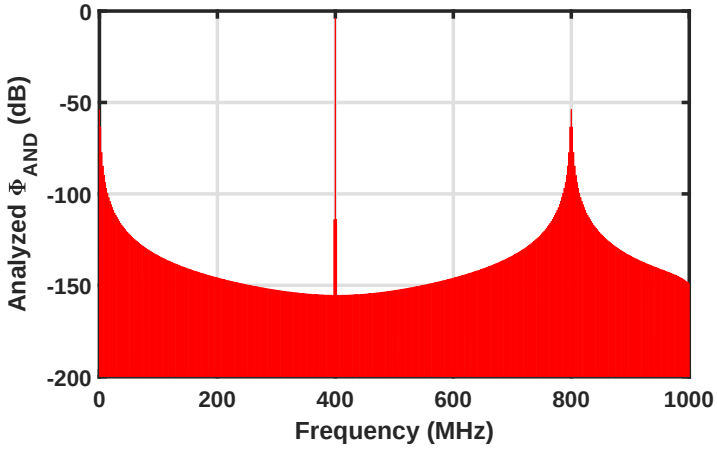


Figure 4.5: VCO clock waveform and proposed AND signal.

To verify expression in (4.12), Fig. 4.6 shows a comparison between the simulated ϕ_{AND} in the 4.6a and the analyzed one in 4.6b. In this comparison, the nominal VCO frequency is 400 MHz. The comparison shows good agreement between the simulated and analyzed ϕ_{AND}. The comparison shows that the response of ϕ_{AND} approaches the response of $\phi_{\circ}$; hence, it can be used to clock the mixer circuit.



(a)



(b)

Figure 4.6: Simulated and analyzed frequency response for ϕ_{AND}.

4.4 Receiver Building Blocks

4.4.1 RF Mixer and Clock Generation

Fig. 4.7a shows the mixer circuit. It is a double-balanced mixer. The current gain for the RF fundamental frequency and for a mixer with with a 50% duty cycle clock is given

by [26, 27, 28, 29]:

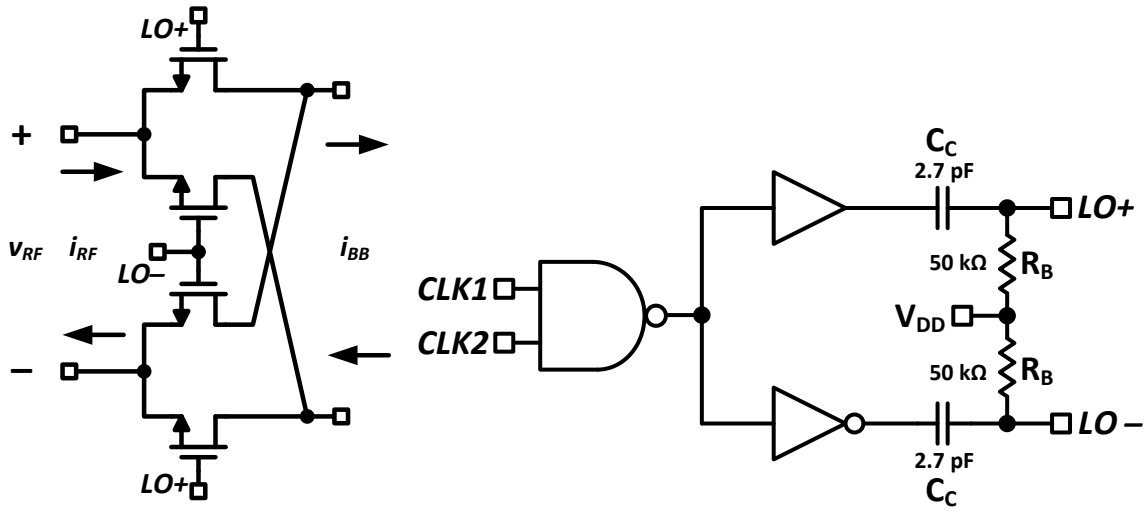
$$A_{I,mixer} = \frac{i_{BB}}{v_{RF}} = \frac{2}{\pi}. \tag{4.13}$$

The mixer input impedance at RF is given by:

$$Z_{in,mixer}(\omega) \cong 4R_{SW} + \frac{4}{\pi^2}\big[Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})\big], \tag{4.14}$$

where Z_{BB} is the baseband input impedance and R_{SW} is mixer switch resistance.

Fig. 4.7b shows the clock generation circuit from the amplifier VCO clock. It consists of AND the gate followed by an inverter and delay cell. DC bias is applied with $\mathrm{V_{DD}}$ so the mixer can switch properly as the baseband side of the mixer dc value is $\mathrm{V_{DD}}/2$.



(a) (b)

Figure 4.7: Receiver's a) RF mixer, and b) clock generation circuit.

4.4.2 Baseband Amplifier

Fig. 4.8 shows a detailed implementation for the baseband amplifier. The amplifier consists of two ring oscillators. Each ring oscillator has a control knob to set the nominal frequency of oscillation. The amplifier has a single phase frequency detector with UP and DOWN outputs. Finally, two charge pumps are used. As the phase frequency detector compares the clock from the two oscillators, a common mode feedback circuit needs to be added to set the common mode level for the amplifier. The following subsections will discuss the implementation for each block.

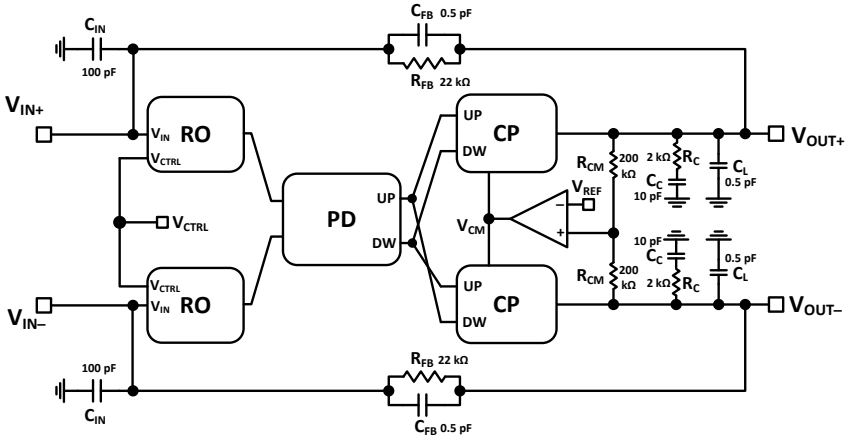


Figure 4.8: Detailed implementation of the baseband amplifier.

4.4.3 Ring Oscillator

Fig. 4.9 shows the implementation of the ring oscillator VCO. It consists of six differential inverters. The VCO has two controls, one for differential input ($\mathrm{V_{IN}}$) and the other one for setting the nominal frequency for both VCOs ($\mathrm{V_{CTRL}}$). Fig. 4.10 shows the $\mathrm{K_{VCO}}$ for the oscillators versus the input voltage. For a supply voltage of 1 V, the dc value of

V_{IN} will be 0.5 V and the effective K_{VCO} will be -700 MHz/V.

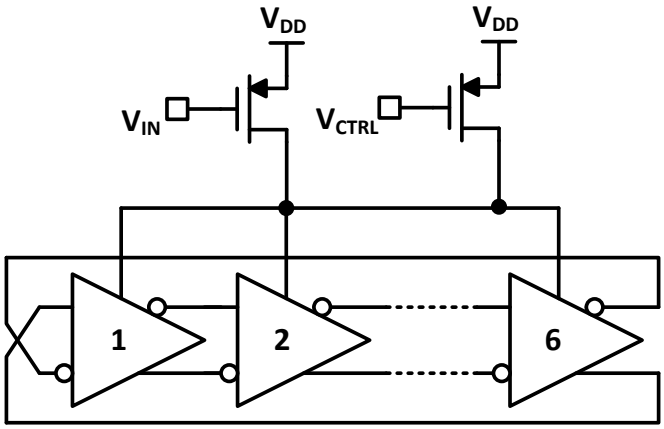


Figure 4.9: Ring oscillator implementation.

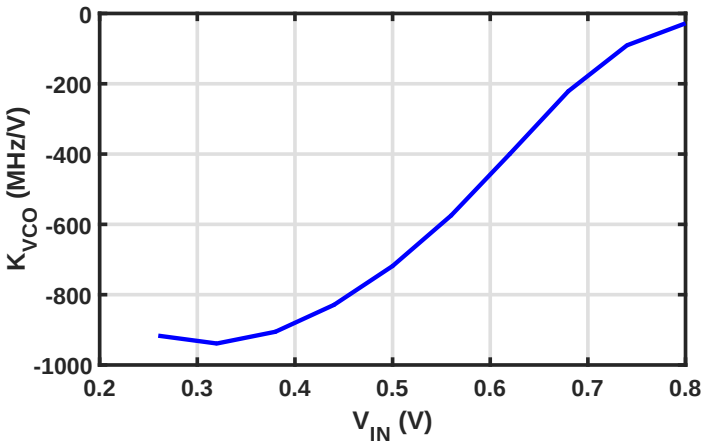


Figure 4.10: $\mathrm{K_{VCO}}$ for the oscillator versus input voltage.

4.4.4 Phase Frequency Detector

Fig. 4.11 shows the implementation for the phase frequency detector. It is designed to optimize the speed and to reduce the minimum pulse width as it affects the linearity and the dynamic range for the amplifier.

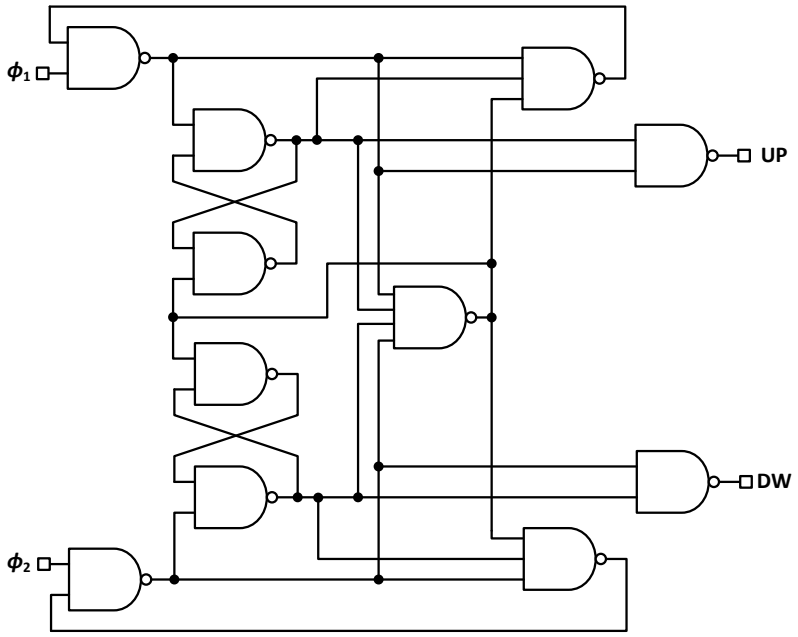


Figure 4.11: Phase frequency detector implementation.

4.4.5 Charge Pump

Fig. 4.12 shows the implementation for the charge pump. It consists of source and tail current sources from $\mathrm{V_{DD}}$ and GND, respectively. Dummy switches are used to connect the current sources to the point with a value of $\mathrm{V_{DD}}/2$ to maintain the operation of the current source to improve linearity. Cascode transistors ($\mathrm{M_2}$ and $\mathrm{M_3}$) are added to improve the output resistance and, hence, the linearity.

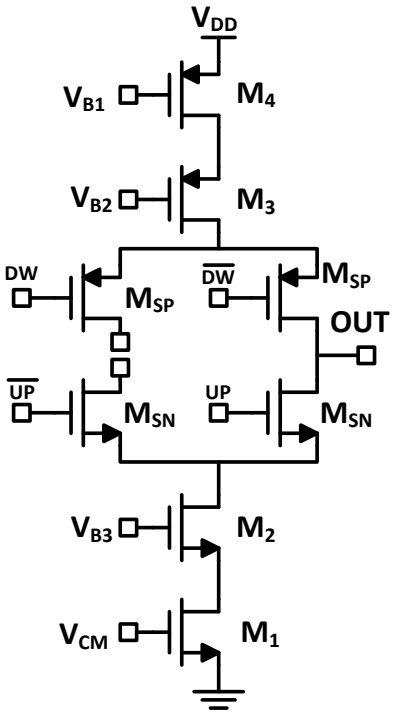


Figure 4.12: Charge pump implementation.

4.5 Design Procedure

To start the design of the system, we will need to have a look at the whole system design. First, the system is simply a mixer followed by an amplifier with a negative feedback resistor and capacitor. To provide matching, the input impedance seen at RF should be equal to 50 Ω. At the clock frequency, the input impedance is given by:

$$Z_{in}(f_{LO}) \cong 4R_{SW} + \frac{8}{\pi^2}\frac{R_{FB}}{A}, \tag{4.15}$$

where R_{SW} is the mixer switch resistance, R_{FB} is amplifier feedback resistance, and A is the amplifier gain. The mixer switch size, amplifier dc gain, feedback resistance and the chain gain should be designed and selected while satisfying (4.15). The chain gain is

given by $A_{RX} \cong R_{FB}/R_{SW}$. The mixer switch should be minimized to reduce the loss in the switch; however, the bigger switch will result in higher power consumption in the buffer circuitry.

To design the VCO based amplifier, the unity gain frequency needs to be specified and it should be $\omega_{\mathrm{UG}} > 10 \times \omega_{3-\mathrm{dB}}$ where $\omega_{3-\mathrm{dB}}$ can be set by R_{FB} and C_{FB}. The unity gain frequency is given by $\omega_{\mathrm{UG}} \cong 4\pi \times K_{VCO}K_{PD}I_{CP}R_C$ [69]. For stability, the zero $\omega_Z = 1/(R_C C_C)$ should be less than ω_{UG}. Also, the VCO oscillation frequency should be $\omega_{osc} \gg \omega_{\mathrm{UG}}$.

4.6 Experimental Results

The wireless receiver is implemented in 130 nm CMOS technology. The receiver operates at the 900 MHz ISM band. Fig. 4.13 shows the die micrograph for the implemented chip. Fig. 4.14 shows the measured $|\mathrm{S}_{11}|$ for the receiver. It also shows the matching at 900 MHz. Fig. 4.15 shows the measured conversion gain for the receiver. The receiver gain is 42 dB and the $3-$dB cut off frequency is 2.7 MHz. Fig. 4.16 shows the measured NF for the receiver. The NF is 21. In simulation, the OB-IIP3 is 6 dBm. The total power consumption for the receiver is 2.9 mW. Fig. 4.17 shows a pie chart for power distribution. Performance summary and comparison with recent art is shown in Table 4.1. The receiver shows its competitiveness except in noise figure which is high due to using ring oscillators right after the mixer.

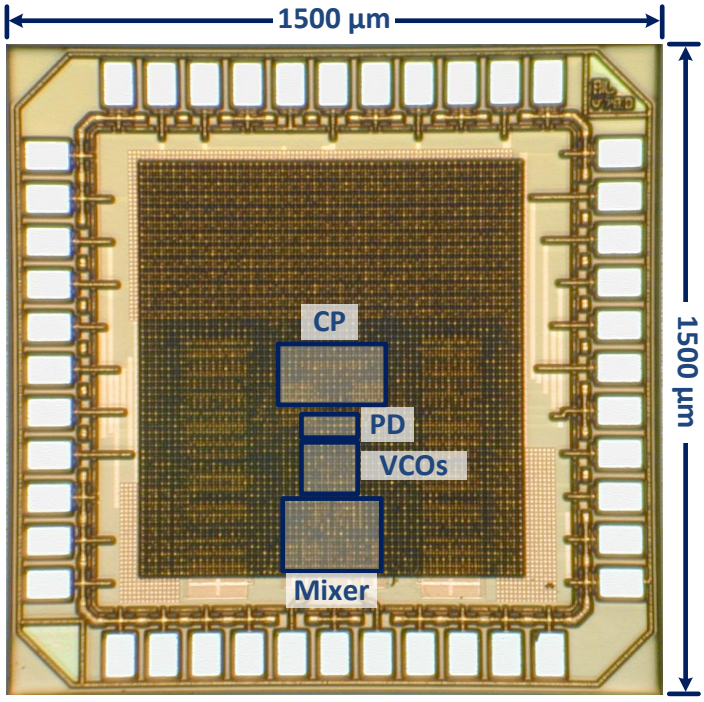


Figure 4.13: Die micrograph.

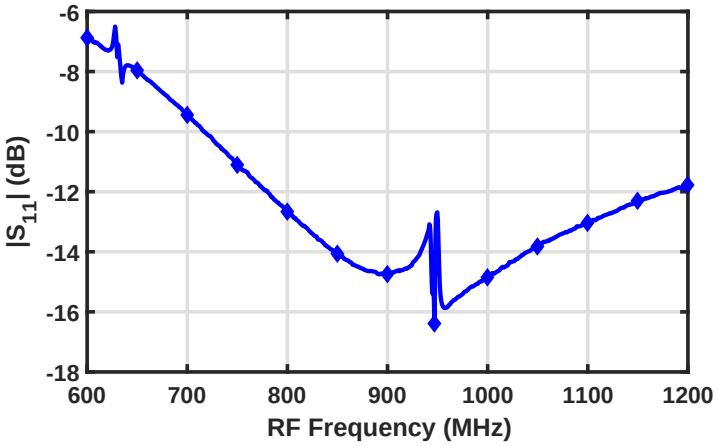


Figure 4.14: Measured receiver $|S_{11}|$.

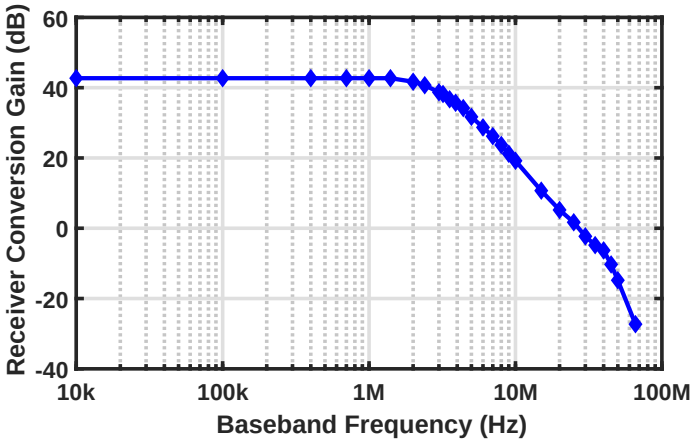


Figure 4.15: Measured receiver conversion gain.

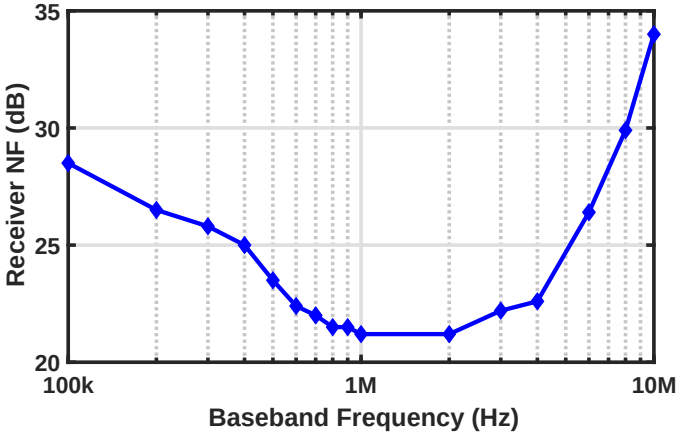


Figure 4.16: Measured receiver NF.

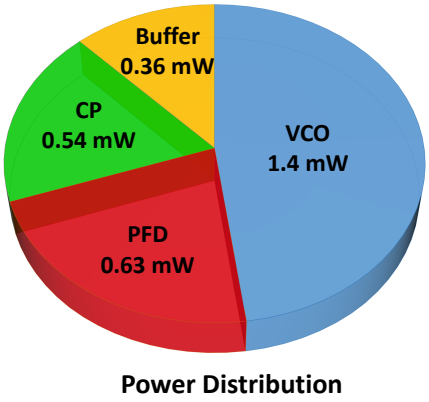


Figure 4.17: Pie chart for power distribution.

Table 4.1: Performance Summary and Comparison with Recent Art

	Khan [8]	Balankutty [9]	Wang [12]	Lin [13]	Sano [14]	Homayoun [39]	This Work
Architecture	Gilbert Active Mixer-First	Zero-IF /Low-IF	Sliding-IF	RF-to-BB Recycling	Sliding-IF	Transformer +Mixer-First	VCO-Based Amplifier +CLK Recycling
RF Frequency (MHz)	2400	2400	2400	900	2400	5000	900
Gain (dB)	37	67	57.8	48	NA	48	49
NF (dB)	28	16	15.7	8.7	6.5	5.3	24
Out-of-Band IIP3 (dBm)	NA	NA	NA	−20.5	NA	+2.6	+6
Power (mW)	0.87◇	32.5	1.78	1.15	6.3	11.6	2.45
CMOS Technology	65 nm	90 nm	65 nm	65 nm	40 nm	65 nm	130 nm

◇ Excluding clock generation

4.7 Conclusions

A highly linear low power wireless receiver is presented. The receiver incorporates a VCO-based amplifier as baseband amplifier to achieve high linearity. Moreover, it saves

power by recycling the VCO clocks to be used in the mixer circuit by using a novel clock recycling technique. The system is implemented in 130nm CMOS technology and operates at an ISM 900 MHz band. The receiver gain is 42 dB. The power consumption is 2.9 mW and the out-of-band IIP3 is 6 dBm. The noise figure is 21 dB. Although the noise figure is high, the novel idea of clock recycling has various applications.

5. SUMMARY AND CONCLUSIONS

In this dissertation, various ideas are introduced to improve the linearity and reduce the power consumption for wireless radio systems.

In Section 2, a low-power RF wireless receiver for WSN is presented. The receiver leverages current-mode topology and a high selective filter to achieve high linearity. The receiver has a frequency multiplication mixer to clock the mixer circuit from a lower frequency oscillator to reduce the power consumption. The receiver gain is 40 dB, NF is 14 dB, in-band IIP3 is -6 dBm and the power consumption is 1.16 mW.

In Section 3, an ultra-low power consumption is introduced that is able to harvest energy from an RF blocker while receiving the signal of interest. The receiver features a single antenna for both operations. The receiver gain is 41.5 dB, and the NF is 19.5 dB. The receiver core power consumption is 430 μW. This power can be reduced by 49% in the presence of a large blocker.

In Section 4, a highly linear energy efficient wireless receiver is presented. The receiver features a VCO-based amplifier in the baseband to improve the linearity with the mixer-first architecture. The system features a novel clock recycling idea to reuse the amplifier's VCOs to clock the mixer circuit and to save power consumption. The receiver conversion gain is 42 dB, the out-of-band IIP3 is 6 dBm and the power consumption is 2.9 mW.

5.1 Future Work

In Section 2, future work can be done by introducing tunability to the notch in the baseband filter. That would make the receiver more immune to nearby blockers. For Section 3, future work can be implemented by adding a complete power management

system to save the power to a battery and make use of the power based on need and availability. Finally, in Section 4, future work can be to investigate the high NF and to reduce it without jeopardizing the linearity.

REFERENCES

[1] L. Atzori, A. Iera, and G. Morabito, "The Internet of Things: A Survey," *Comput. Netw.*, vol. 54, pp. 2787–2805, Oct. 2010.

[2] I. Gartner, "Gartner Says 6.4 Billion Connected "Things" Will Be in Use in 2016, Up 30 Percent From 2015." http://www.gartner.com/newsroom/id/3165317, Nov. 2015. Online; accessed July 2016.

[3] A. Roy, A. Klinefelter, F. B. Yahya, X. Chen, L. P. Gonzalez-Guerrero, C. J. Lukas, D. A. Kamakshi, J. Boley, K. Craig, M. Faisal, S. Oh, N. E. Roberts, Y. Shakhsheer, A. Shrivastava, D. P. Vasudevan, D. D. Wentzloff, and B. H. Calhoun, "A 6.45 μW Self-Powered SoC With Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems," *IEEE Trans. Biomed. Circuits Syst*, vol. 9, pp. 862–874, Dec. 2015.

[4] J. Masuch and M. Delgado-Restituto, "A 1.1-mW-RX -81.4-dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy," *IEEE Trans. Microw. Theory Techn.*, vol. 61, pp. 1660–1673, Apr. 2013.

[5] D. Niyato, E. Hossain, M. M. Rashid, and V. K. Bhargava, "Wireless sensor networks with energy harvesting technologies: a game-theoretic approach to optimal energy management," *IEEE Wireless Comm.*, vol. 14, pp. 90–96, Aug. 2007.

[6] X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, "A Switched Capacitor Energy Harvester Based on a Single-Cycle Criterion for MPPT to Eliminate Storage Capacitor," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 65, pp. 793–803, Feb. 2018.

[7] H. Cruz, H. Y. Huang, S. Y. Lee, and C. H. Luo, "A 1.3 mW Low-IF, Current-Reuse, and Current-Bleeding RF Front-End for the MICS Band with Sensitivity of -97 dBm," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 62, pp. 1627–1636, June 2015.

[8] O. U. Khan and D. D. Wentzloff, "8.1 nJ/b 2.4 GHz Short-Range Communication Receiver in 65 nm CMOS," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 62, pp. 1854–1862, Jul. 2015.

[9] A. Balankutty, S. A. Yu, Y. Feng, and P. R. Kinget, "A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications," *IEEE J. Solid-State Circuits*, vol. 45, pp. 538–553, Mar. 2010.

[10] S. Lee, I. Choi, H. Kim, and B. Kim, "A Sub-mW Fully Integrated Wide-Band Receiver for Wireless Sensor Network," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, pp. 319–321, May 2015.

[11] A. Selvakumar, M. Zargham, and A. Liscidini, "A 600μW Bluetooth low-energy front-end receiver in 0.13μm CMOS technology," in *IEEE ISSCC Dig. Tech. Papers*, pp. 1–3, Feb. 2015.

[12] K. Wang, J. Koo, R. Ruby, and B. Otis, "21.7 A 1.8mW PLL-free channelized 2.4GHz ZigBee receiver utilizing fixed-LO temperature-compensated FBAR resonator," in *IEEE ISSCC Dig. Tech. Papers*, pp. 372–373, Feb. 2014.

[13] Z. Lin, P. I. Mak, and R. P. Martins, "A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications," *IEEE J. Solid-State Circuits*, vol. 49, pp. 2990–3004, Dec. 2014.

[14] T. Sano, M. Mizokami, H. Matsui, K. Ueda, K. Shibata, K. Toyota, T. Saitou, H. Sato, K. Yahagi, and Y. Hayashi, "13.4 A 6.3mW BLE transceiver embedded RX

image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network," in *IEEE ISSCC Dig. Tech. Papers*, pp. 1–3, Feb. 2015.

[15] J. Prummel, M. Papamichail, M. Ancis, J. Willms, R. Todi, W. Aartsen, W. Kruiskamp, J. Haanstra, E. Opbroek, S. Rievers, P. Seesink, H. Woering, and C. Smit, "13.3 A 10mW Bluetooth Low-Energy transceiver with on-chip matching," in *IEEE ISSCC Dig. Tech. Papers*, pp. 1–3, Feb. 2015.

[16] F. Zhang, Y. Miyahara, and B. P. Otis, "Design of a 300-mV 2.4-GHz Receiver Using Transformer-Coupled Techniques," *IEEE J. Solid-State Circuits*, vol. 48, pp. 3190–3205, Dec. 2013.

[17] O. Elsayed, J. Zarate-Roldan, A. Abuellil, F. Hussien, A. Eladawy, and E. Sánchez-Sinencio, "Highly Linear Low Power Wireless RF Receiver for WSN," *IEEE Trans. Very Large Scale Integ. Syst.*, 2019.

[18] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, "A 900-MHz Dual-Conversion Low-IF GSM Receiver in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1992–2002, Dec. 2001.

[19] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The Blixer, a Wideband Balun-LNA-I/Q-Mixer Topology," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2706–2715, Dec. 2008.

[20] C. Andrews and A. C. Molnar, "A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface," *IEEE J. Solid-State Circuits*, vol. 45, pp. 2696–2708, Dec. 2010.

[21] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. C. F. Chang, "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wide-

band Wireless Applications," *IEEE J. Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec. 2012.

[22] J. Zarate-Roldan, A. Abuellil, M. Mansour, O. Elsayed, F. A. L. Hussien, A. Eladawy, and E. Sánchez-Sinencio, "0.2-nJ/b Fast Start-Up Ultralow Power Wireless Transmitter for IoT Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, pp. 259–272, Jan. 2018.

[23] B. Razavi, *RF Microelectronics, Second Edition*. Prentice-Hall, 2011.

[24] H. Zhang and E. Sánchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 58, pp. 22–36, Jan. 2011.

[25] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio, "A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 52, pp. 875–879, Dec 2005.

[26] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and Optimization of Current-Driven Passive Mixers in Narrowband Direct-Conversion Receivers," *IEEE J. Solid-State Circuits*, vol. 44, pp. 2678–2688, Oct. 2009.

[27] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan, "A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, pp. 718–739, Mar. 2009.

[28] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural Evolution of Integrated M-Phase High-Q Bandpass Filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, pp. 52–65, Jan. 2012.

[29] H. Osman, A. Emira, A. N. Mohieldin, M. Abouzied, and A. Soliman, "On-chip high-Q bandpass filtering using N-phase current driven passive mixers," in *ECCTD*, pp. 206–209, Aug. 2011.

[30] A. Pirola, A. Liscidini, and R. Castello, "Current-Mode, WCDMA Channel Filter With In-Band Noise Shaping," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1770–1780, Sept. 2010.

[31] E. Kargaran, D. Manstretta, and R. Castello, "Design and Analysis of 2.4 GHz 30 μW CMOS LNAs for Wearable WSN Applications," *IEEE Trans. Circuits and Syst. I: Reg. Papers*, vol. 65, pp. 891–903, Mar. 2018.

[32] G. Werner-Allen, K. Lorincz, M. Ruiz, O. Marcillo, J. Johnson, J. Lees, and M. Welsh, "Deploying a wireless sensor network on an active volcano," *IEEE Internet Computing*, vol. 10, pp. 18–25, Mar. 2006.

[33] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3359–3375, Dec. 2009.

[34] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, B. Verbruggen, and J. Craninckx, "A 40 nm CMOS 0.4-6 GHz Receiver Resilient to Out-of-Band Blockers," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1659–1671, Jul. 2011.

[35] H. Hedayati, W. F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF Blocker-Filtering Noise-Canceling Wideband Receiver With Shared TIA in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, pp. 1148–1164, May 2015.

[36] C. Wu, Y. Wang, B. Nikolić, and C. Hull, "An Interference-Resilient Wideband Mixer-First Receiver With LO Leakage Suppression and I/Q Correlated Orthogonal

Calibration," *IEEE Trans. Microw. Theory Techn.*, vol. 64, pp. 1088–1101, Apr. 2016.

[37] Z. Lin, P. I. Mak, and R. Martins, "9.4 A 0.5V 1.15mW 0.2mm2 Sub-GHz ZigBee receiver supporting 433/860/915/960MHz ISM bands with zero external components," in *IEEE ISSCC Dig. Tech. Papers*, pp. 164–165, Feb. 2014.

[38] Z. Lin, P. l. Mak, and R. P. Martins, "2.4 A 0.028mm2 11mW single-mixing blocker-tolerant receiver with double-RF N-path filtering, S11 centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF," in *IEEE ISSCC Dig. Tech. Papers*, pp. 1–3, Feb. 2015.

[39] A. Homayoun and B. Razavi, "A Low-Power CMOS Receiver for 5 GHz WLAN," *IEEE J. Solid-State Circuits*, vol. 50, pp. 630–643, Mar. 2015.

[40] Y. Liu and W. A. Serdijn, "Analysis and Design of a Passive Receiver Front-End Using an Inductive Antenna Impedance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, pp. 733–744, Feb. 2018.

[41] J. Masuch, M. Delgado-Restituto, D. Milosevic, and P. Baltus, "Co-Integration of an RF Energy Harvester Into a 2.4 GHz Transceiver," *IEEE J. Solid-State Circuits*, vol. 48, pp. 1565–1574, Jul. 2013.

[42] N. E. Roberts, K. Craig, A. Shrivastava, S. N. Wooters, Y. Shakhsheer, B. H. Calhoun, and D. D. Wentzloff, "26.8 A 236nW -56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 450–451, Jan. 2016.

[43] M. Rahman and R. Harjani, "A Sub-1-V 194- μW 31-dB FOM 2.3-2.5-GHz Mixer-First Receiver Frontend for WBAN With Mutual Noise Cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, pp. 1102–1109, Apr. 2016.

[44] E. Alpman, A. Khairi, M. Park, V. S. Somayazulu, J. R. Foerster, A. Ravi, and S. Pellerano, "95 μW 802.11g/n compliant fully-integrated wake-up receiver with -72dBm sensitivity in 14nm FinFET CMOS," in *IEEE RFIC Symp.*, pp. 172–175, Jun. 2017.

[45] C. Salazar, A. Cathelin, A. Kaiser, and J. Rabaey, "A 2.4 GHz Interferer-Resilient Wake-Up Receiver Using A Dual-IF Multi-Stage N-Path Architecture," *IEEE J. Solid-State Circuits*, vol. 51, pp. 2091–2105, Sep. 2016.

[46] Y. Rajavi, M. Taghivand, K. Aggarwal, A. Ma, and A. S. Y. Poon, "An RF-Powered FDD Radio for Neural Microimplants," *IEEE J. Solid-State Circuits*, vol. 52, pp. 1221–1229, May 2017.

[47] S. Oh and D. D. Wentzloff, "A -32dBm sensitivity RF power harvester in 130nm CMOS," in *IEEE RFIC Symp.*, pp. 483–486, Jun. 2012.

[48] M. Abouzied and E. Sánchez-Sinencio, "Low-Input Power-Level CMOS RF Energy-Harvesting Front End," *IEEE Trans. Microw. Theory Techn.*, vol. 63, pp. 3794–3805, Nov. 2015.

[49] T. Le, K. Mayaram, and T. Fiez, "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1287–1302, May 2008.

[50] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1985 –1997, Sept. 2011.

[51] M. Stoopman, S. Keyrouz, H. Visser, K. Philips, and W. Serdijn, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE J. Solid-State Circuits*, vol. 49, pp. 622–634, Mar. 2014.

[52] Z. Hameed and K. Moez, "A 3.2 V -15 dBm Adaptive Threshold-Voltage Compensated RF Energy Harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, pp. 948–956, Apr. 2015.

[53] M. A. Abouzied, K. Ravichandran, and E. Sánchez-Sinencio, "A Fully Integrated Reconfigurable Self-Startup RF Energy-Harvesting System With Storage Capability," *IEEE J. Solid-State Circuits*, vol. 52, pp. 704–719, Mar. 2017.

[54] O. Elsayed, M. Abouzied, and E. Sánchez-Sinencio, "A 540 μW RF wireless receiver assisted by RF blocker energy harvesting for IoT applications with +18 dBm OB-IIP3," in *IEEE RFIC Symp.*, pp. 230–233, May 2016.

[55] J. Wang *et al.*, "A 900 MHz RF energy harvesting system in 40 nm CMOS technology with efficiency peaking at 47% and higher than 30% over a 22dB wide input power range," in *Proc. IEEE 43rd Eur. Solid-State Circuits Conf. (ESSCIRC)*, pp. 299–302, Sep. 2017.

[56] A. K. Moghaddam *et al.*, "A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, pp. 992–1002, Apr. 2017.

[57] J. Kang, S. Rao, P. Chiang, and A. Natarajan, "Design and Optimization of Area-Constrained Wirelessly Powered CMOS UWB SoC for Localization Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 64, pp. 1042–1054, Apr. 2016.

[58] O. Elsayed, M. Abouzied, V. Vaidya, K. Ravichandran, and E. Sánchez-Sinencio, "An Ultralow-Power RF Wireless Receiver With RF Blocker Energy Recycling for IoT Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, pp. 4927–4942, Nov. 2018.

[59] H. Darabi, "A Blocker Filtering Technique for SAW-Less Wireless Receivers," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2766–2773, Dec. 2007.

[60] G. Barué, *Microwave Engineering: Land & Space Radiocommunications*. Wiley-Interscience, 2008.

[61] M. Pischella and D. L. Ruyet, *Digital Communications 2: Digital Modulations*. John Wiley & Sons, 2015.

[62] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and Optimization of Direct-Conversion Receivers With 25Mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, pp. 2353–2366, Sept. 2010.

[63] C. Andrews and A. C. Molnar, "Implications of Passive Mixer Transparency for Impedance Matching and Noise Figure in Passive Mixer-First Receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, pp. 3092–3103, Dec. 2010.

[64] A. Mirzaei and H. Darabi, "Analysis of Imperfections on Performance of 4-Phase Passive-Mixer-Based High-Q Bandpass Filters in SAW-Less Receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, pp. 879–892, May 2011.

[65] X. He and J. van Sinderen, "A Low-Power, Low-EVM, SAW-Less WCDMA Transmitter Using Direct Quadrature Voltage Modulation," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3448–3458, Dec. 2009.

[66] K. Kotani, A. Sasaki, and T. Ito, "High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3011–3018, Nov. 2009.

[67] M. A. Abouzied, H. Osman, V. Vaidya, K. Ravichandran, and E. Sánchez-Sinencio, "An Integrated Concurrent Multiple-Input Self-Startup Energy Harvest-

ing Capacitive-Based DC Adder Combiner," *IEEE Trans. Ind. Electron.*, vol. 65, pp. 6281–6290, Aug. 2018.

[68] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," *IEEE J. Solid-State Circuits*, vol. 47, pp. 3120–3129, Dec. 2012.

[69] C. Hsu and P. R. Kinget, "A 40MHz 4th-order active-UGB-RC filter using VCO-based amplifiers with zero compensation," in *Proc. IEEE 40th Eur. Solid-State Circuits Conf. (ESSCIRC)*, pp. 359–362, Sep. 2014.

[70] S. Kalani, S. S. Nagam, and P. R. Kinget, "Charge pump optimization and output spur reduction in VCO-based OTAs for active-RC analog filters," in *Proc. IEEE Inter. Symp. Circuits Syst. (ISCAS)*, pp. 822–825, May 2016.

[71] D. K. Weinlader, *Precision CMOS Receivers for VLSI Testing Applications*. PhD thesis, Dept. Elect. Eng., Stanford University, Stanford, CA, 2001.