HIGH SPEED RECONFIGURABLE NRZ/PAM4 TRANSCEIVER DESIGN TECHNIQUES

A Dissertation

by

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ABSTRACT

While the majority of wireline standards use simple binary non-return-to-zero (NRZ) signaling, four-level pulse-amplitude modulation (PAM4) standards are emerging to increase bandwidth density. This dissertation efficient implementations for high speed NRZ/PAM4 transceivers. The first prototype includes a dual-mode NRZ/PAM4 serial I/O transmitter which can support both modulations with minimum power and hardware overhead. A source-series-terminated (SST) transmitter achieves 1.2Vpp output swing and employs lookup table (LUT) control of a 31-segment output digital-to-analog converter (DAC) to implement 4/2-tap feed-forward equalization (FFE) in NRZ/PAM4 modes, respectively. Transmitter power is improved with low-overhead analog impedance control in the DAC cells and a quarter-rate serializer based on a tri-state inverter-based mux with dynamic pre-driver gates. The transmitter is designed to work with a receiver that implements an NRZ/PAM4 decision feedback equalizer (DFE) that employs 1 finite impulse response (FIR) and 2 infinite impulse response (IIR) taps for first post-cursor and long-tail ISI cancellation, respectively. Fabricated in GP 65-nm CMOS, the transmitter occupies 0.060mm2 area and achieves 16Gb/s NRZ and 32Gb/s PAM4 operation at 10.4 and 4.9 mW/Gb/s while operating over channels with 27.6 and 13.5dB loss at Nyquist, respectively. The second prototype presents a 56Gb/s four-level pulse amplitude modulation (PAM4) quarter-rate wireline receiver which is implemented in a 65nm CMOS process. The frontend utilize a single stage continuous time linear equalizer (CTLE) to boost the main cursor and relax the pre-cursor cancelation requirement,

requiring only a 2-tap pre-cursor feed-forward equalization (FFE) on the transmitter side. A 2-tap decision feedback equalizer (DFE) with one finite impulse response (FIR) tap and one infinite impulse response (IIR) tap is employed to cancel first post-cursor and long-tail inter-symbol interference (ISI). The FIR tap direct feedback is implemented inside the CML slicers to relax the critical timing of DFE and maximize the achievable data-rate. In addition to the per-slice main 3 data samplers, an error sampler is utilized for background threshold control and an edge-based sampler performs both PLL-based CDR phase detection and generates information for background DFE tap adaptation. The receiver consumes 4.63mW/Gb/s and compensates for up to 20.8dB loss when operated with a 2-tap FFE transmitter. The experimental results and comparison with state-of-the-art shows superior power efficiency of the presented prototypes for similar data-rate and channel loss. The usage of proposed design techniques are not limited to these specific prototypes and can be applied for any wireline transceiver with different modulation, data-rate and CMOS technology.

To my mother and father,

Soheila and Manouchehr.

My inspiration, my motivation, my joy

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Contributors

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1. INTRODUCTION

While most of household and personal devices are moving towards using wireless networks and transceivers [1-12], optical interconnects [13-20] and wireline transceivers [21-25] provide higher data-rate, lower latency and more power efficient solution for many applications. Data centers networks is the most prominent example of such applications where growing zettabyte range traffic of them requires ultra-high speed, low power transceivers.

New standards and application are emerging every year for wireline applications. The industry demand is always towards higher data-rate communications. Due to limited number of input-output (IO) pins on commercial packages and density constraints, high-speed links, often serialize the data on the transmitter side before sending it on channel. The data will be de-serialized back on the receiver side [21].

The power efficiency and circuit bandwidth are benefiting from advances in CMOS process. However, wireline communication channels' bandwidth have not followed the same trend. Thus, channel impairments such as dielectric loss, skin effect, reflections and cross-talk have become more prominent affecting quality of communication. This results in bit errors in communication if no measure is taken.

Equalization is employed on both receiver and transmitter side to compensate for the channel impairments. Transceivers can be implemented utilizing fully digital equalizers with digital-to-analog (DAC) based transmitters [22] and analog-to-digital (ADC) based receivers [23-25]. This allows for easy implementation of complex equalizers in digital domain which are prone to process variations can compensate for significant channel loss.

However, DAC based and ADC based designs along with digital signal processors (DPS), required to implement equalization, can be very power hungry. On the contrary, mixed signal transceivers can provide a more power efficient solution for low to medium loss channels.

This research targets the design of efficient mixed signal transmitter and receivers operating at >32Gb/s data-rates with focus on four-level pulse amplitude modulation (PAM4). While the design are done for specific data-rates using a certain process node, the proposed techniques can be extended to higher data-rates. Most of the proposed techniques can benefit from CMOS scaling as well.

This dissertation is organized as follows. Section 2 discusses challenges associated with system level and circuit level high speed mixed-signal transceiver design. The system level considerations and trade-offs have been discussed in this section. The rest of the section, explains design topologies and trade-offs for some critical transmitter and receiver circuit blocks. A reconfigurable dual-mode 16/32 Gb/s NRZ/PAM4 transmitter design is detailed in section 3. A 56 Gb/s PAM4 receiver design details has been discussed in section 4. Details of clock and recovery circuit (CDR) is discussed in this section. PAM4 threshold and DFE adaptations are implemented and discussed in details in this section. Finally, section 5 concludes this dissertation.

2. BACKGROUND ON MIXED SIGNAL TRANSCEIVERS*

2.1 Introduction

This section briefly explains challenges and trade-offs in wireline transceiver design. Section 2.1 discusses the system level design challenges and solutions. Section 2.3 focuses on trade-offs and circuit level solutions for critical blocks in transmitter design which includes the final serializer and the output driver. Section 2.4 compares different circuit implementation for critical receiver circuits including continuous time linear equalizers (CTLE) and samplers. The main target of this section is to provide the reader with background information about mixed signal transceiver design, required for understanding the remainder of this dissertation.

2.2 Transceiver Architectures

The main target of wireline transceiver design is achieve bit error free transmission over a channel with limited bandwidth, such as the one shown in Fig. 2.1, while consuming as low power as possible. The most common modulation used for wireline applications is non-return-to-zero (NRZ) modulation. This is achieved by sending a positive voltage at the output for a one symbol and a negative voltage for a zero, sending on bit at a time.

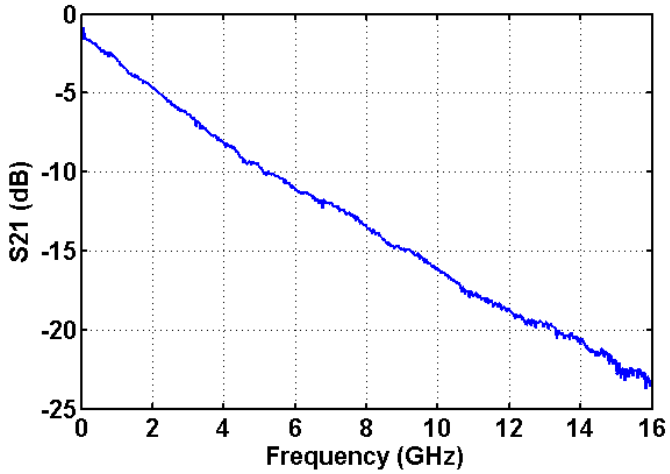

Figure 2.1: Insertion loss of a sample back-plane wireline channel.

The Skin effect, dielectric loss and reflection causes by impedance discontinuities in the channel, results in dispersion of data while traveling through the channel. In order to characterize this, pulse response of the channel is often used as depicted in Fig. 2.2. The one bit period (T_b) long input pulse will spread over multiple bit periods. This results in reduced peak at the output of channel and transmitted single bit at the input of channel will affect multiple of bits at the output of the channel. This will cause inter-symbol-interference (ISI) at the output of channel, resulting in detection errors at the receiver side.

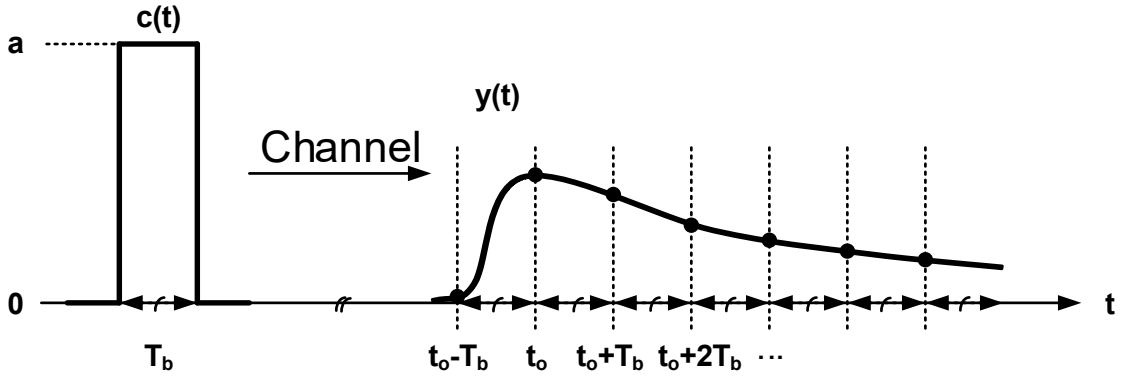

Figure 2.2: Channel pulse response.

To overcome ISI in wireline systems, equalization is used at transmitter and receiver sides. On transmitter side feed-forward equalization (FFE) is often used to cancel out the post-cursor and pre-cursor ISI [26-29]. Fig. 2.3 shows the block diagram of such equalizer. FFE equalizer cancels the channel distortion by pre-distorting the signal before the channel. As the input data is a digital signal, digital delay units (flip-flops) can be engaged to generate the taps. Due to supply voltage limitations, FFE equalization is done by attenuating the main cursor. This limits effectiveness of FFE equalizers when number of taps increase.

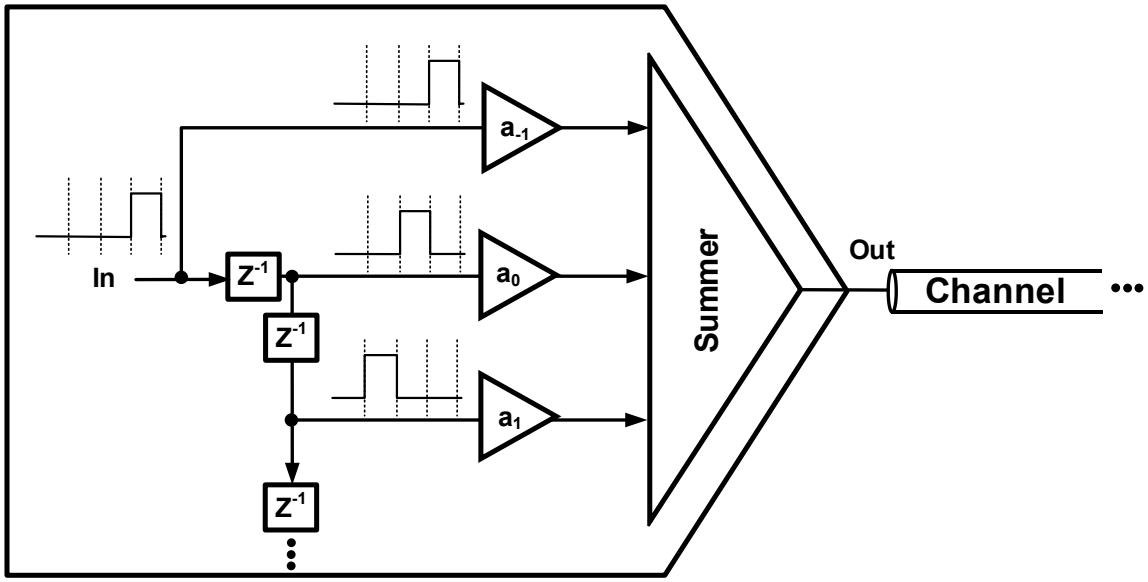

Figure 2.3: Transmitter FFE equalization.

FFE equalization can also be achieved at receiver side [30-33] as depicted in Fig. 2.4. As the signal is already attenuated by the channel, the dynamic range would be enough to implement high pass filtering by amplifying high frequency contents rather that attenuating low frequency contents. However, implementing FFE equalization at receiver side can be quite challenging as delay elements should be implemented in an analog manner rather than simple digital delays.

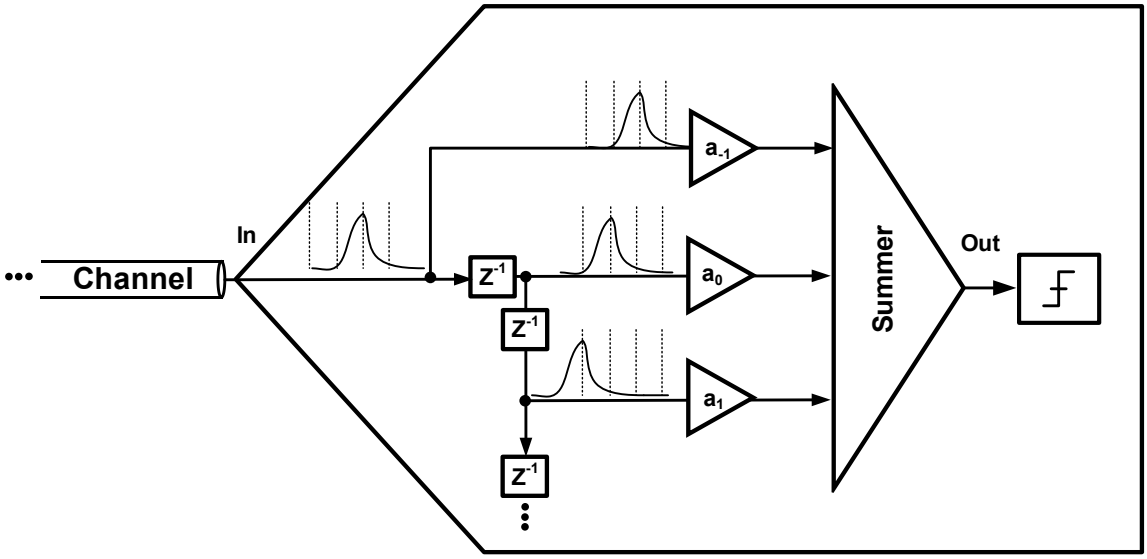

Figure 2.4: Receiver FFE equalization.

To implement receiver side equalization using only digital delay elements, the decision feed-back equalizer (DFE) is engaged [34-37]. Fig. 2.5 shows block diagram of such equalizer. DFE equalizers can efficiently cancel post-cursor ISI without noise and crosstalk amplification. However, they cannot cancel pre-cursor ISI and the loop should settle in 1 unit interval (UI), which can be very challenging at high data-rates. Loop-unrolling can be utilized to relax critical timing of a DFE [38], [39]. This will increases the number of samplers by a factor of 2 if only the first tap in unrolled. Two or more number of taps can be unrolled which will cause exponential increase in number of slicers and can be prohibitive in terms of power and area.

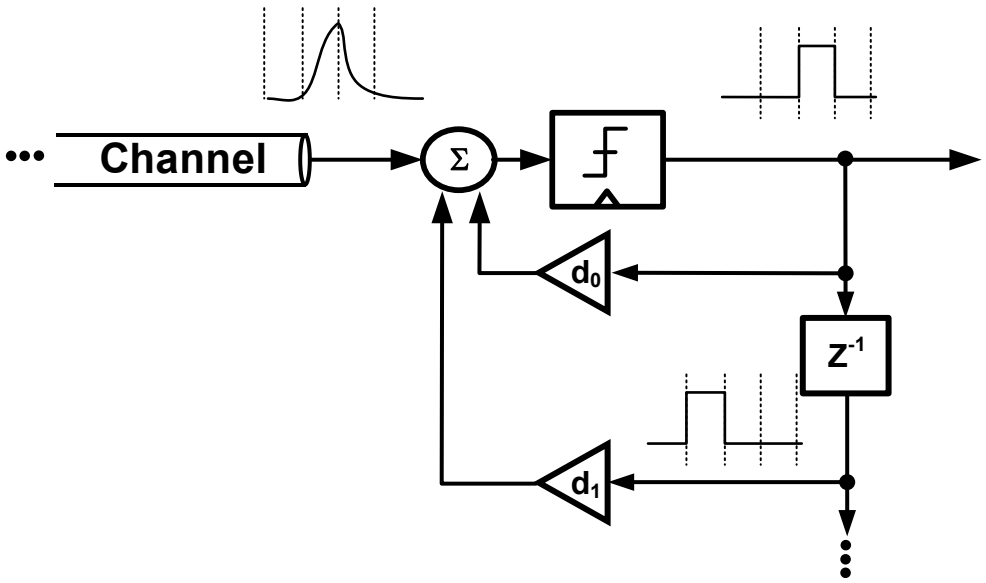

Figure 2.5: Receiver DFE equalization.

Each DFE finite impulse response (FIR) tap could cancels only one post-cursor ISI. Thus, multiple FIR taps are required to compensate for high loss channels with multiple significant post-cursor ISI terms. Alternatively, infinite impulse response (IIR) taps can be utilized to cancel multiple ISI terms [40], [41]. A continuous time linear equalizer (CTLE) can also be utilized at receiver side to compensate for the long-tail ISI. CTLE implementations are discussed in more details in section 2.4.

Another method to reduce the effect of low frequency channel response is to use more advance modulation. four-level pulse amplitude modulation (PAM4) signaling is the most popular alternative for conventional NRZ signaling which has been proposed for very high data-rates in new standards [42], [43]. It allows 2 bits per symbol transmission reducing the system bandwidth by a factor of 2. However, multiple challenges are associated with PAM4 signaling. PAM4 transceivers require more stringent circuit linearity, equalizers which can implement multi-level inter-symbol interference (ISI) cancellation, and

improved sensitivity. While PAM4 modulation allows for a longer unit interval (UI) time, the reduced voltage margins necessitate increased comparator sensitivity. Moreover, PAM4 modulation is more sensitive to residual ISI. Thus, multiple taps of equalizer is required to minimize the residual ISI.

While pessimistic from a BER perspective, peak distortion analysis [44] provides a rapid approach to find the worst-case eye opening and is utilized to highlight the differences in ISI sensitivity between NRZ and PAM4 modulation at the same symbol rate. Fig. 2.2 shows a conceptual pulse response $y(t)$ produced by sending an ideal pulse $c(t)$ with duration T_b across a channel. This pulse response has the cursor value at $t = t_0$ and ISI terms at T_b offsets before and after this cursor instant.

First consider the NRZ modulation case, where there are two symbols, $y_1 = y(t)$ and $y_0 = -y(t)$. Assuming linearity, the worst case high and low levels, v_1 and v_0 respectively, of the eye diagram at the sampling point, t_o, are calculated by

$$v_1 = y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_0 = -y(t_o) + \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|. \tag{2.1}$$

Thus, the NRZ PDA eye height, shown in Fig. 24(a), is

$$A_{NRZ} = v_1 - v_0 = 2(y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|). \tag{2.2}$$

Note that the $\sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|$ term equals the sum of the absolute value of all post- and pre-cursor ISI values determined from the pulse response. This represents the maximum amount of ISI that can be added or subtracted from a symbol with the worst-

case symbol sequence. In the common case where all ISI values are positive, a lone-pulse sequence of a single 1 preceded and followed by all 0s is the worst-case pattern that sets the minimum high level.

Now consider the PAM4 case, where there are four symbols, $y_{11} = y(t)$, $y_{10} = 1/3\ y(t)$, $y_{01} = -1/3\ y(t)$ and $y_{00} = -y(t)$. As shown in Fig. 2.6(b), assuming linearity this results in three eyes that are bounded by six levels which can be calculated by

$$v_{11} = y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_{10h} = \frac{1}{3}y(t_o) + \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_{10l} = \frac{1}{3}y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_{01h} = -\frac{1}{3}y(t_o) + \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_{01l} = -\frac{1}{3}y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|,$$

$$v_{00} = -y(t_o) + \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|. \qquad (2.3)$$

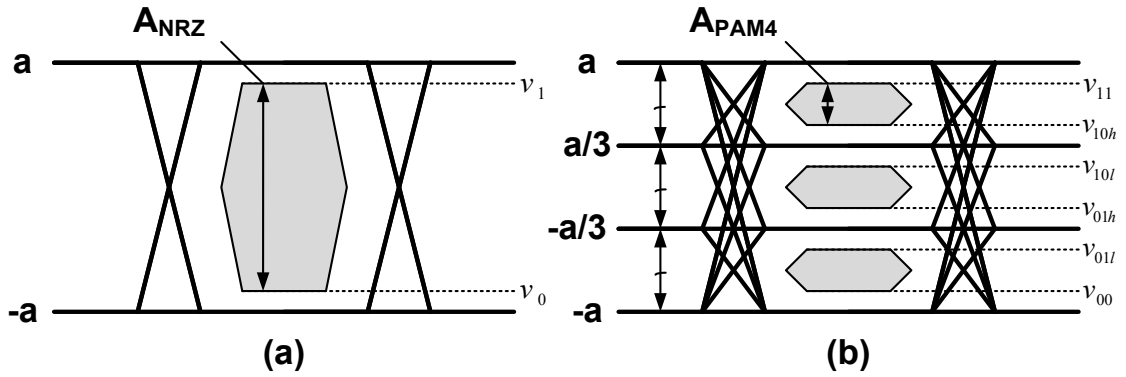

Figure. 2.6: Eye diagrams with (a) NRZ and (b) PAM4 data.

Thus, the PAM4 PDA eye heights are

$$A_{PAM4} = v_{11} - v_{10h} = v_{10l} - v_{10h} = v_{10l} - v_{00}$$
$$= 2\left(\frac{1}{3}y(t_o) - \sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty} |y(t_o - iT_b)|\right). \quad (2.4)$$

Note that although the ideal voltage margin with PAM4 modulation is 1/3 the ideal voltage margin with NRZ modulation, the PAM4 symbols suffer from the same amount of ISI $\sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty}|y(t_o - iT_b)|$. While for the same data rate a PAM4 pulse response will often be much better than its NRZ counterpart for typical wireline channels, it is worth noting that this heightened PAM4 ISI sensitivity necessitates an increased level of ISI cancellation. This confirms, while PAM4 has better spectral efficiency relative to NRZ signaling, this doesn't make it the superior modulation option for all systems. The optimal modulation is a function of the target data rate, channel loss profile. Power and circuit constraints should also be considered while choosing optimal modulation.

Overall, in order to design a mixed signal transceiver for a certain application, factors including, standard requirements, channel profile, circuit constrains, power efficiency

should be taken into account. This will lead to selection of appropriate modulation and type and complexity of equalization at transmitter and receiver side.

Statistical analysis is a convenient method to plan the architecture, based on system requirements. Statistical analysis along with an estimation of how circuit level complexity can translates into power consumption can provides us a metric to make architectural decisions. The system design procedure described in system analysis subsection of section 3 and 4 are based on this approach.

2.3 Transmitter Circuits

In this section some key circuit blocks of a transmitter will be discussed. Different implementations of these key blocks are investigated and trade-offs will be discussed to for choosing the optimal structure for a certain architecture.

2.3.1 Serializer

The final serializer is one of the most critical blocks in a transmitter, as it must maintain enough bandwidth to support the full-rate output. Fig. 2.7 shows a CMOS 2:1 transmission gate (T-gate) based serializer [45]. The CMOS serializer suffers from stacking at the output full-rate node which reduces the driving power. Both NMOS and PMOS transistors are required to transfer zeros and ones. Thus both switches are turned on at the same time. However, essentially, only one of them are required to turn on depending on the polarity of the input data which translates into extra switching power consumption.

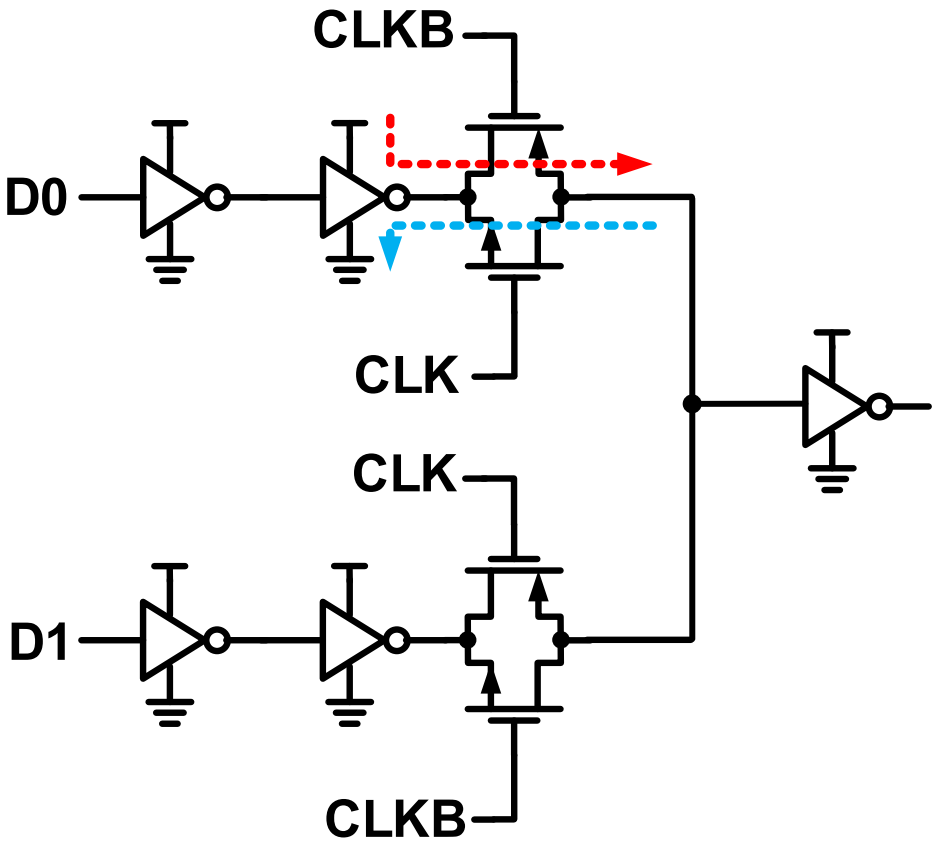

Figure. 2.7: A CMOS 2:1 T-gate based serializer.

A tri-state inverter based 2:1 serializer is proposed in [46] to overcome stacking at the output node and reduce the switching power as illustrated in Fig. 2.8

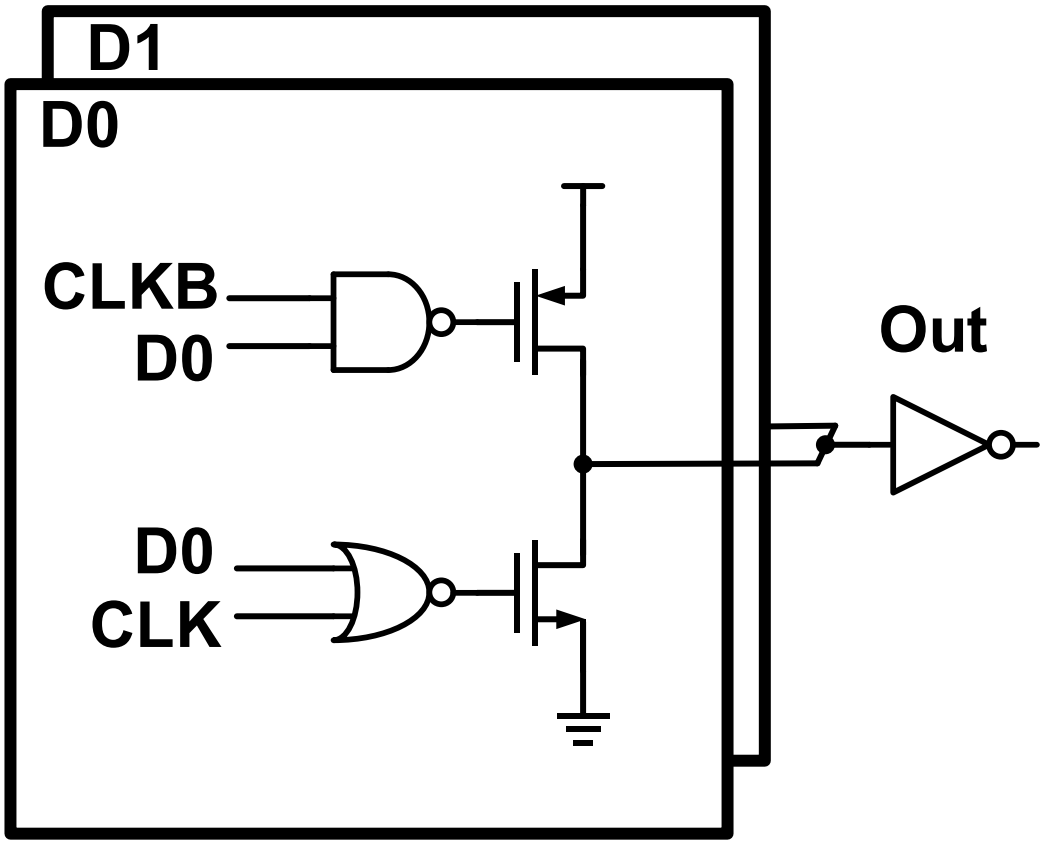

Figure. 2.8: A tri-state based 2:1 serializer.

The serializer requires half-rate differential clock. Using 2:1 serializer requires half-rate flip-flops to retime the data and half-rate clock distribution. This could be very challenging and power hungry when trying to transmit very high data-rates.

In many high data-rate applications, instead, a quarter-rate architecture is used where the final stage of serialization involves a 4:1 serializer. This allows engaging only quarter-rate flip-flops for retiming and quarter-rate clock distribution which can reduce power consumption of the system. Fig. 2.9 shows a 4:1 CMOS T-gate based serializer.

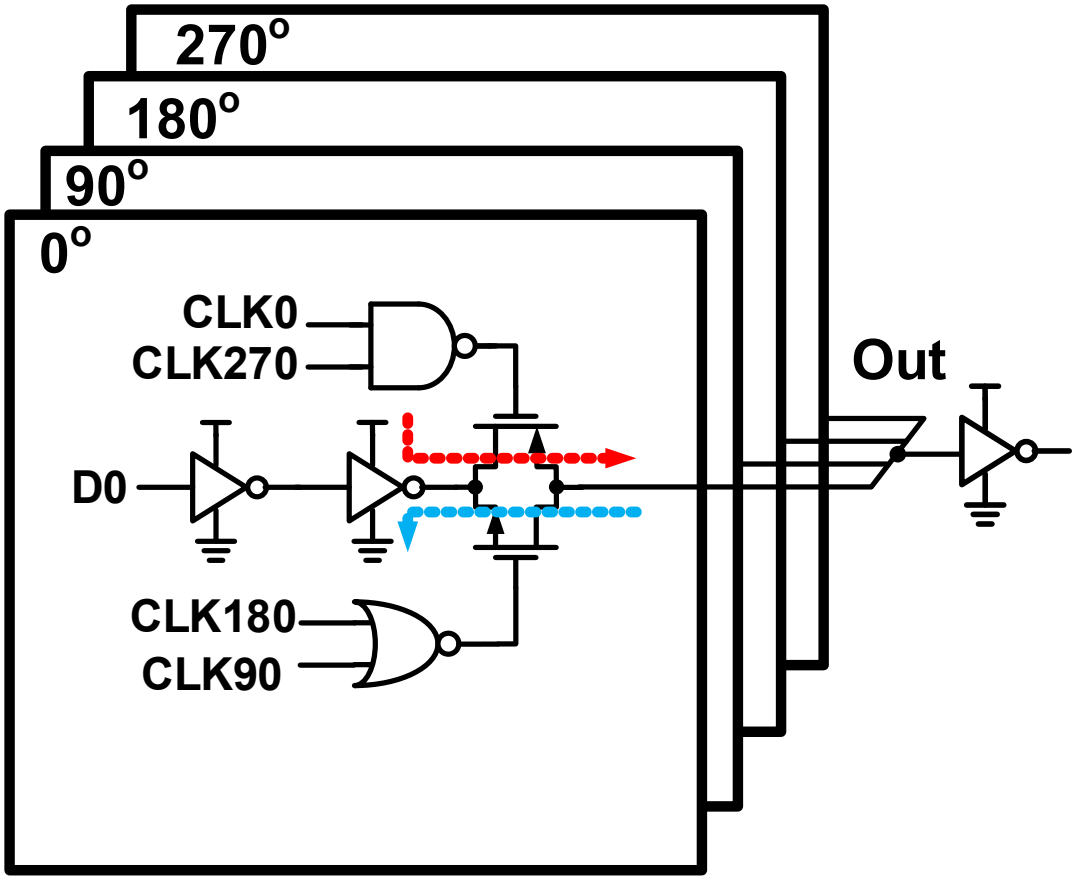

Figure. 2.9: A CMOS 4:1 T-gate based serializer.

In addition to stacking at the output full-rate node, the serializer suffers from significant self-loading caused by 4 parallel branches connected to the output node.

Current mode serializers can also be used instead of CMOS serializers [47] as depicted in Fig. 2.10. This will reduce self-loading of the serializer and achieve higher bandwidth. The disadvantage is that current mode serializers consume static current which is independent of the data-rate.

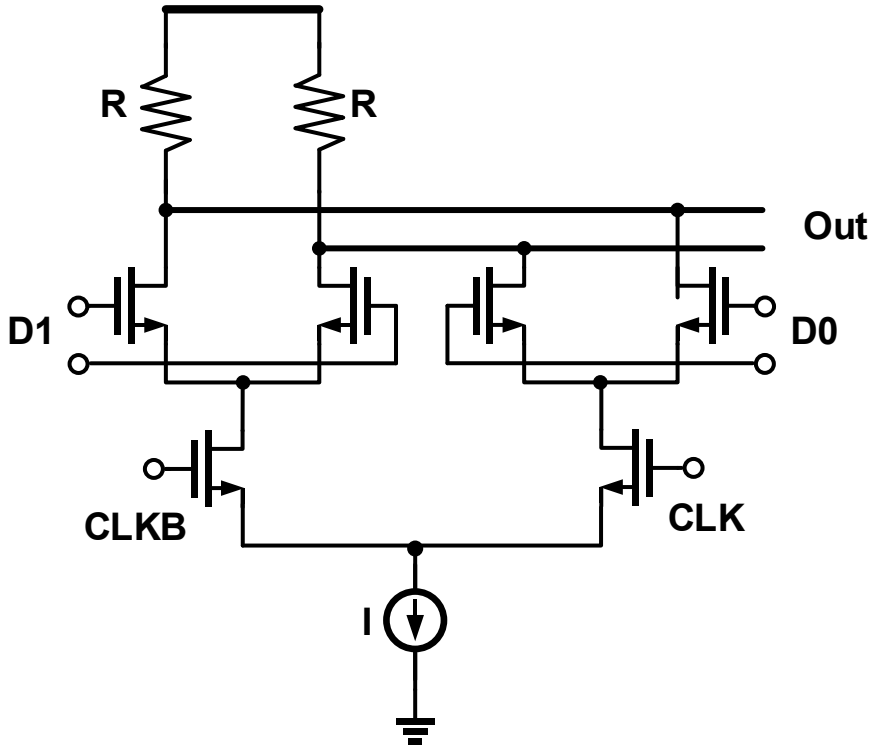

Figure. 2.10: A current mode 2:1 serializer.

2.3.2 Output Driver

Output driver is the last stage of a transmitter, connecting the transmitter to the channel. Since the output driver should provide the current to drive the channel, termination load, and pads capacitive parasitic, it could be a power hungry block especially in very low power applications.

Fig. 2.11 shows schematic of a current mode output driver [48]. Here Rc resistance, the parallel termination, is set to match the channel impedance to minimize reflections. In order to ensure good channel matching in presence of fabrication tolerances, a resistor DAC is often used to tune the output termination. It should be noted as a passive resistor is used as the termination, the output resistance is relatively independent of the output

voltage. Having a fixed matched resistance in the drain, the output swing of the driver is set by the tail current. The output swing of the current mode drivers can be quite large as each side can go all the way up to supply voltage and the limitation on low minimum voltage is set by compliance voltage of tail current plus drain-source voltage of the differential pair transistors in triode region which can be very low. This allows for maximum peak to peak differential output swing of slightly less than twice the supply voltage.

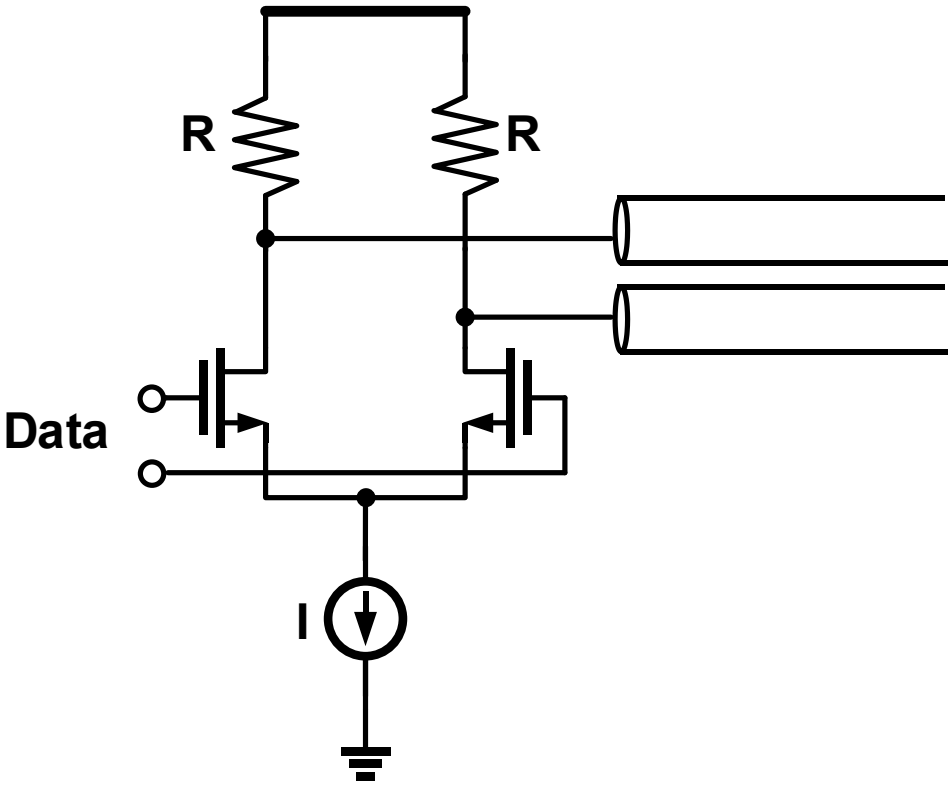

Figure. 2.11: A current mode output driver.

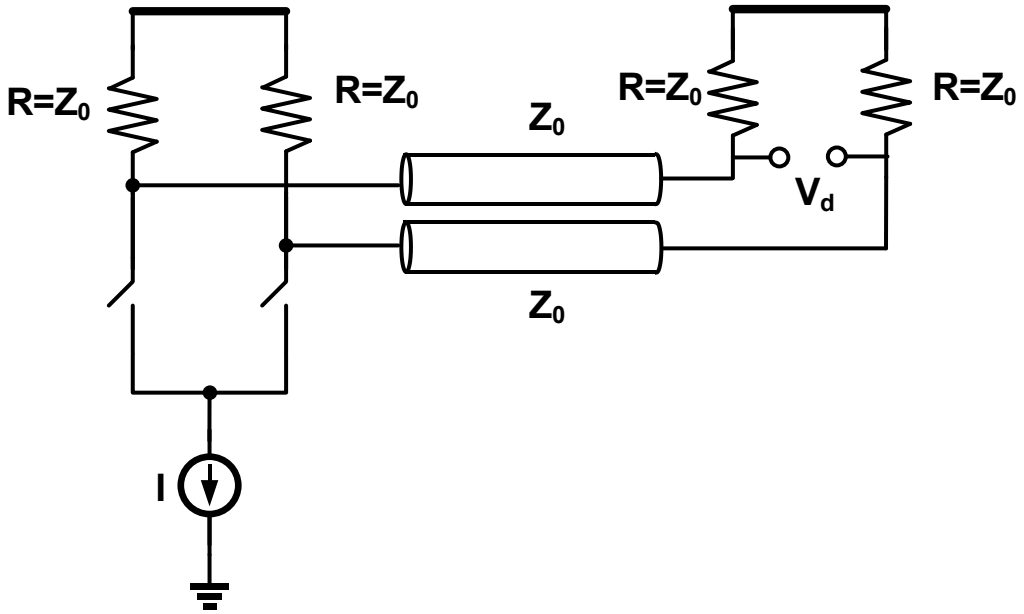

Figure. 2.12: A single-ended terminated current mode driver.

Fig. 2.12 shows a current mode driver while connected to the channel with single-ended termination on the receiver side. Writing the voltage and current equations we have:

$$V_{d,1} = \left(\frac{I}{2}\right) R \tag{2.5}$$

$$V_{d,0} = -\left(\frac{I}{2}\right) R \tag{2.6}$$

$$V_{d,pp} = IR \tag{2.7}$$

$$I = \frac{V_{d,pp}}{R} \tag{2.8}$$

Where $V_{d,1}$ is the differential voltage at the receiver side when transmitting a one, $V_{d,0}$ is the same when transmitting a zero, $V_{d,pp}$ is the peak-to-peak differential received signal amplitude and I is the driver tail current.

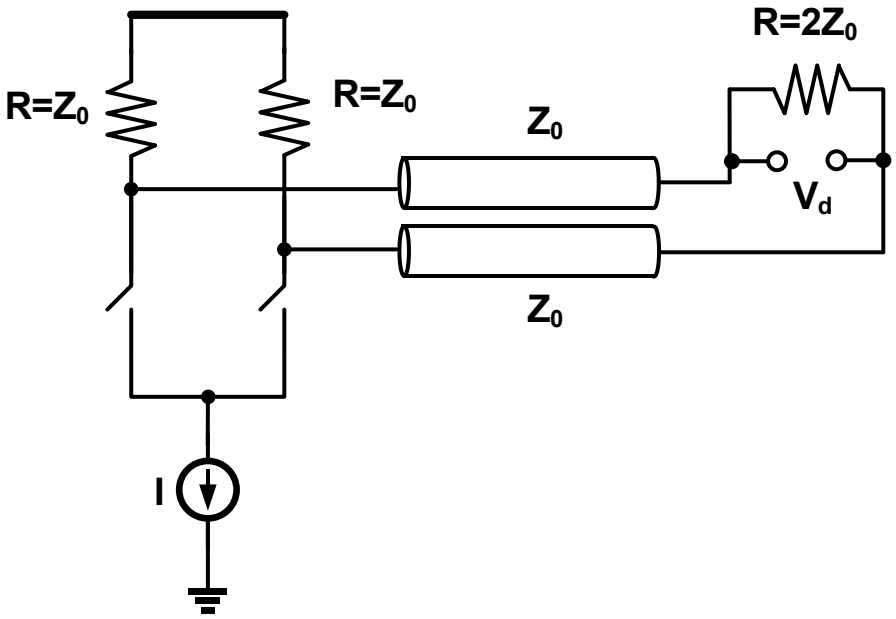

Figure. 2.13: A differentially terminated current mode driver.

Fig. 2.13 shows the same driver when terminated differentially on the receiver side after the channel. Writing voltage and current equations for we have:

$$V_{d,1} = \left(\frac{I}{4}\right)(2R) \tag{2.9}$$

$$V_{d,0} = -\left(\frac{I}{4}\right)(2R) \tag{2.10}$$

$$V_{d,pp} = IR \tag{2.11}$$

$$I = \frac{V_{d,pp}}{R} \tag{2.12}$$

Implementing feed-forward equalization (FFE) can be easily achieved in current mode drivers by adding extra parallel differential pairs connected to the output [49] as illustrated in Fig. 2.13. It should be noted that the middle level generation associated with FFE does not affect the driver's termination matching. Another good characteristic of current mode

drivers is that the current they drain from supply voltage is independent of the current transmitted symbol and previous symbols, in case of FFE equalization.

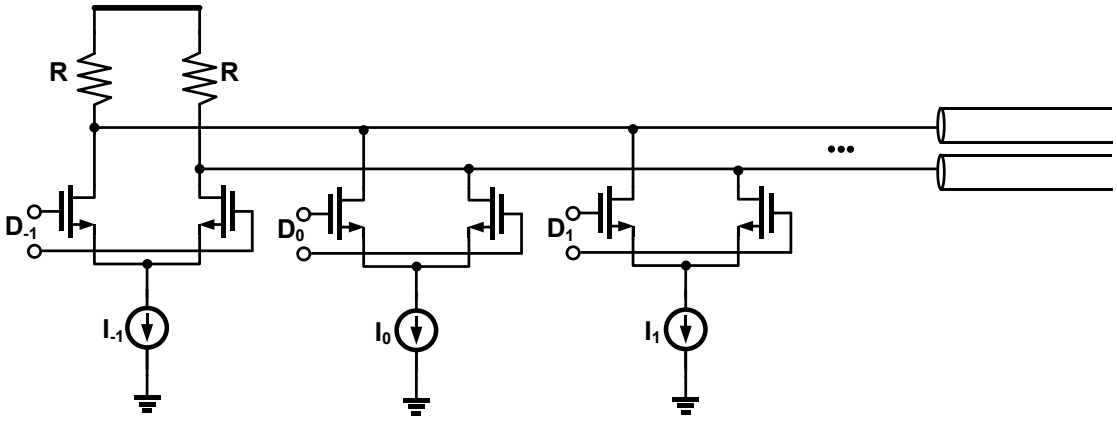

Fig. 2.14: FFE implementation in a current mode driver.

Figure. 2.14 shows schematic of a voltage mode driver. Here, a series combination of Rc passive resistor and triode resistance of the switch provides a source series termination (SST) and matching to the channel.

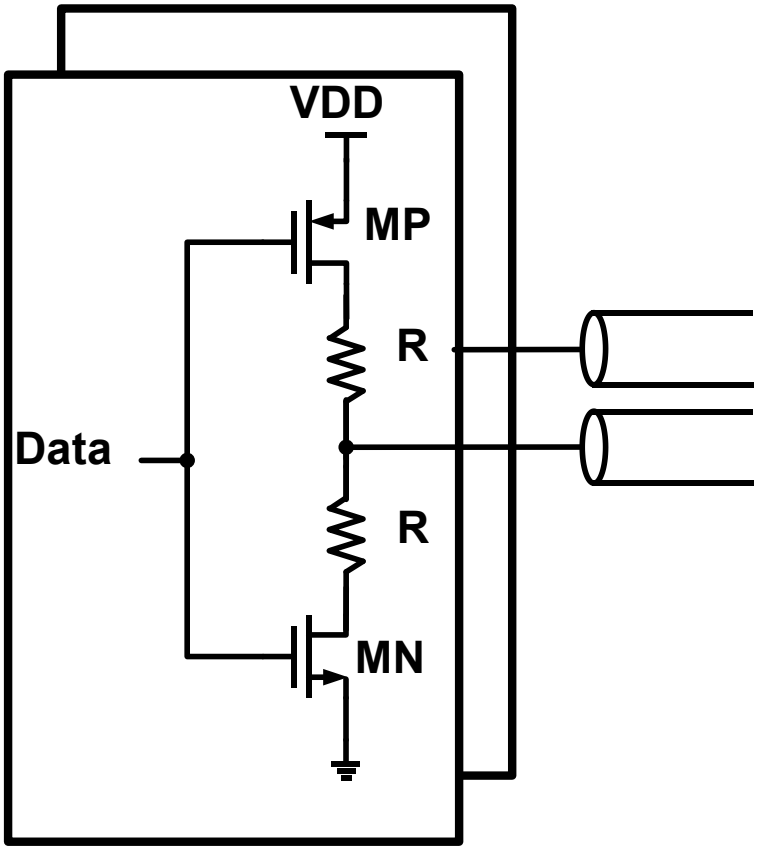

Figure. 2.15: A high swing voltage mode driver.

In simple voltage mode SST drivers, the supply voltage of the driver sets the output swing. The differential peak to peak output swing of the driver is equal to supply voltage in a voltage mode driver. The minimum supply voltage of the driver in Fig. 2.15 is equal to:

$$V_s = |V_{THP}| + V_{ODP} \tag{2.13}$$

To ensure PMOS transistors will turn on while their gate is pulled down to ground. As this minimum voltage can be quite high, for very low power applications, this type of driver is often referred to as a high swing voltage mode driver [50], [51].

An alternative to using NMOS and PMOS transistors as switches, is to use an all NMOS structure [52] as shown in Fig. 2.16.

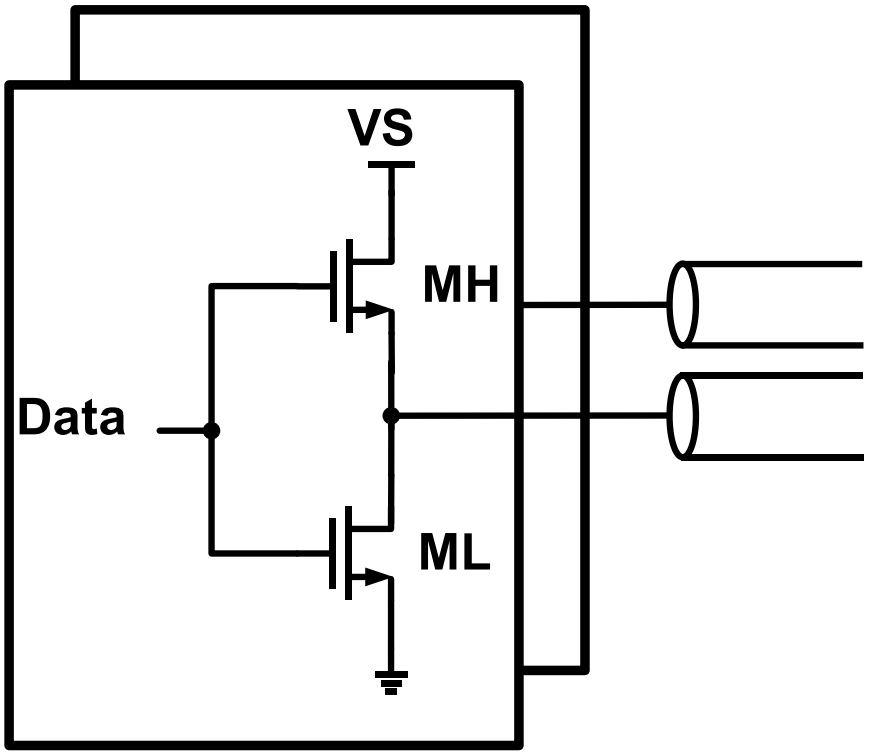

Figure. 2.16: A low swing voltage mode driver.

Here as both top and bottom switches are NMOS transistors, the top transistors can turn on even with very low supply voltages. However, engaging an all NMOS structure enforcers a maximum supply voltage to ensure triode operation of top transistors. It can be shown that the maximum supply voltage is equal to:

$$V_s = \frac{4}{3}(VDD - V_{THH} - V_{ODH}) \tag{2.14}$$

When differential termination is engaged on the receiver side, while this will increase to:

$$V_s = 2(VDD - V_{THH} - V_{ODH}) \tag{2.15}$$

When single-ended termination is used at the receiver side. As this limits the maximum driver output swing, for high performance applications, this driver is often referred to as a low swing driver.

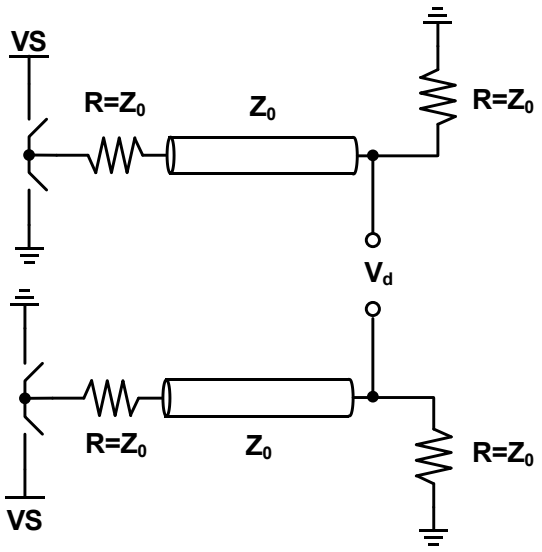

Figure. 2.17: A single-ended terminated voltage mode driver.

Fig. 2.17 shows a voltage mode driver when connected to a channel and terminated in a single-ended manner at the receiver side. Writing voltage and current equations for we have:

$$V_{d,1} = \frac{V_S}{2} \tag{2.16}$$

$$V_{d,0} = -\frac{V_S}{2} \tag{2.17}$$

$$V_{d,pp} = V_S \tag{2.18}$$

$$I = \frac{V_S}{2R} \tag{2.19}$$

$$I = \frac{V_{d,pp}}{2R} \tag{2.20}$$

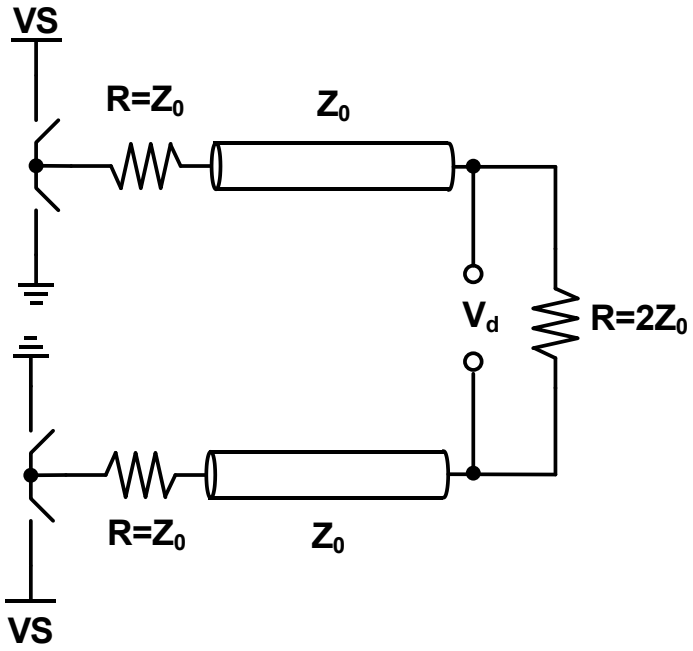

Figure. 2.18: A differentially terminated voltage mode driver.

Fig. 2.18 shows the same voltage mode driver when terminated differentially at the receiver side. Writing voltage and current equations for we have:

$$V_{d,1} = \frac{V_S}{2} \tag{2.21}$$

$$V_{d,0} = -\frac{V_S}{2} \tag{2.22}$$

$$V_{d,pp} = V_S \tag{2.23}$$

$$I = \frac{V_S}{4R} \tag{2.24}$$

$$I = \frac{V_{d,pp}}{4R} \tag{2.25}$$

Compared to a current mode driver, for a similar voltage swing, the single-ended terminated voltage mode driver consumes half the current. This is while the differentially terminated voltage mode driver consumes a quarter current compared to the current mode counterpart for the similar output swing.

FFE equalization is more challenging to implement in voltage mode drivers compared to current mode drivers due to the fact that voltage mode drivers are terminated in a series manner. The driver should be modified to generate the extra levels associated with FFE equalization while maintaining the channel matching. One popular approach to implement FFE equalizer is to divide the output driver to a multi-segment driver [50]. Segments will provide and overall termination to match the channel. However, each segment can be connected to the current or one of the previous symbols (Fig. 2.19). Here, the middle levels will be generated by shunting the current from positive output port to ground and from supply voltage to the negative output port. The tap weights will be set by the number of segments assigned to each tap. Redundant segments are often employed for impedance matching which can be enabled or disabled.

It should be noted that implementing segmentation at the output driver requires complex logic in the pre-driver which results in increased power consumption of the pre-driver. The shunt current required when shunting current for middle level voltages will cause variation in current from supply that will cause fluctuation on the supply voltage.

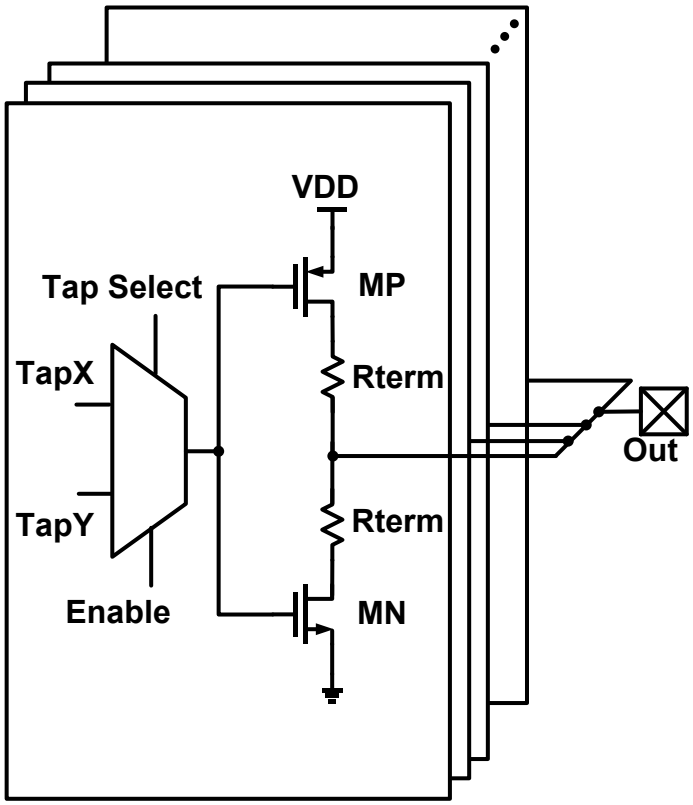

Figure. 2.19: A segmented voltage mode driver.

The tap selection and enabling and disabling of the segments is often implemented by tap select MUXes preceding the SST segments. This allows for flexible tap weight assignment and convenient impedance matching. However, similar to a T-gate serializers, tap select MUXes causes stacking in the full-rate path which reduces the system bandwidth and increase the power consumption to achieve similar driving strength.

2.4 Receiver Circuits

In this section some key circuit blocks of a receiver will be discussed. Different implementations of these key blocks are investigated and trade-offs will be discussed to for choosing the optimal structure for a certain architecture.

2.4.1 CTLE

CTLE is a linear equalizer often used in the receiver frontend as the first stage of equalization. Their purpose is create a high pass filter to compensate the low pass profile of the channel, creating close to flat frequency response. CTLEs can be in a passive manner as depicted in Fig. 2.20.

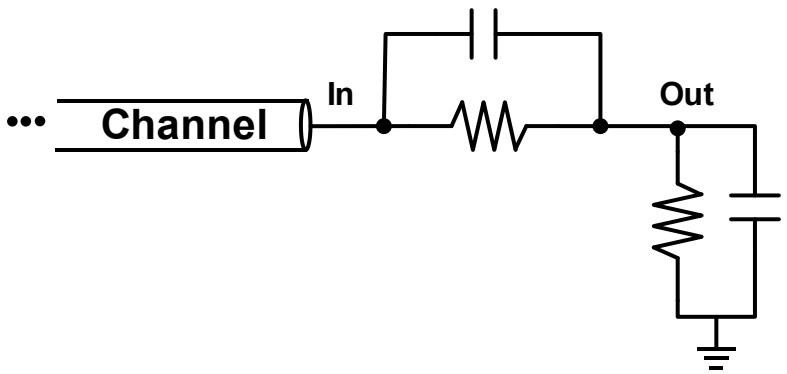

Figure. 2.20: A passive CTLE block diagram.

Passive CTLEs are very linear and easy to implement as they only require passive elements. But they cannot provide any gain at Nyquist. Resistor and capacitor DACs are used to tune the low frequency gain and high frequency peaking to match the target channel profile.

Active CTLEs [53] are more popular as they can provide gain ay Nyquist as illustrated in Fig. 2.21. This, however, limits the linear range of the equalizer. Here Rd along with load capacitance sets the bandwidth. The low frequency gain (and input linear range) is set by Rs resistor DAC while the high frequency peaking can be controlled by Cs capacitor DAC.

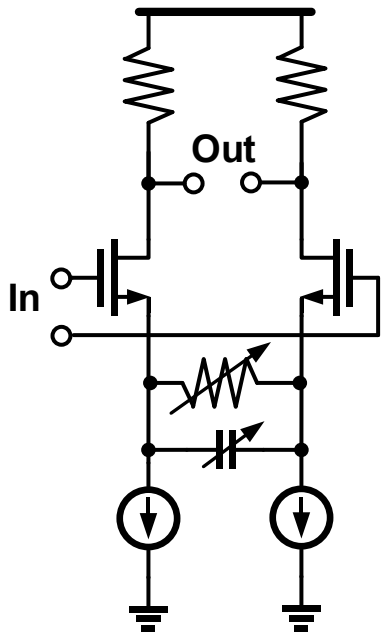

Figure. 2.21: An active CTLE block diagram.

As maintaining bandwidth while providing sufficient gain might be challenging when dealing with very high data-rates, shunt peaking is often employed in active CTLEs to increase the equalizer bandwidth [37]. However, due to usage of inductors this implementation consumes significant area. As channel losses might exceed the viable peaking of a single stage CTLE and the channel loss profile often doesn't match simple R-C type profile, multi-stages of CTLE is often engaged to compensate for medium to

high loss channels. These CTLEs occupies significant chip areas and can consume significant amount of power.

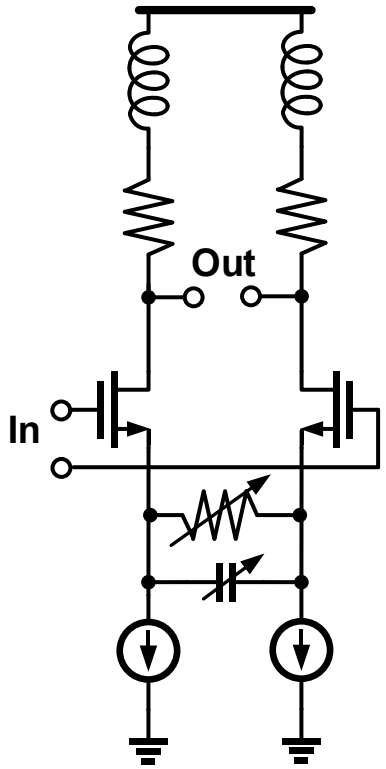

Figure. 2.22: An active CTLE with shunt peaking.

2.4.2 Sampler

Sampler is one of the most critical blocks in the receiver design. Their decision time limits the maximum data-rate that the receiver can operate at. Their gain and noise performance is a significant contributor is overall system sensitivity and the maximum channel loss the receiver can handle without bit errors.

The single stage dynamic amplifier of Fig. 2.22 can be used as a sampler [54]. While the single stage implementation can provide a high bandwidth, it suffers from low gain.

This will result in poor sensitivity. The output swing will also be dependent on the input amplitude.

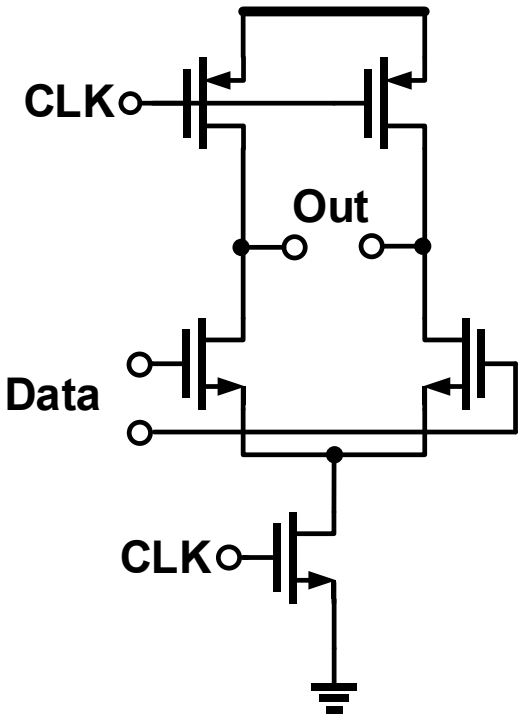

Figure. 2.22: A single stage dynamic amplifier sampler.

Strong-arm sampler of Fig. 2.23 is one of the most popular structures used in high speed receivers [55]. It can provide relatively high bandwidth while the regenerative NMOS and PMOS pairs can provide a high gain. They provide rail-to-rail output without consuming static power. Only single-ended clock is required for clocking the strong-arm sampler.

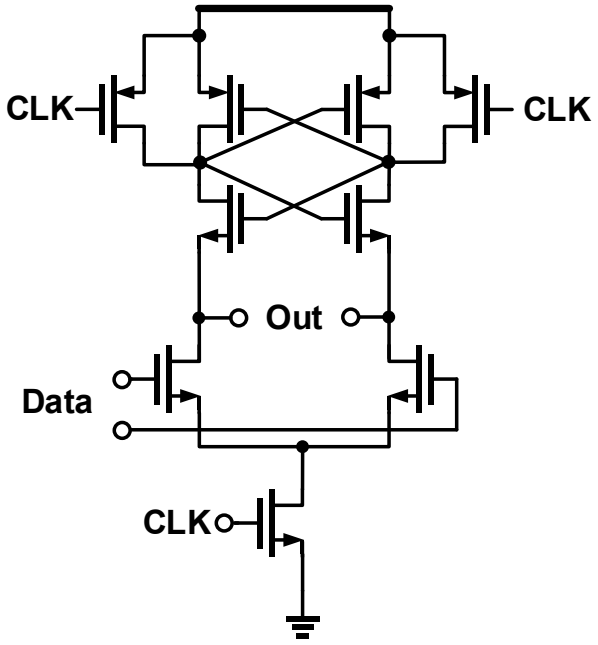

Figure. 2.23: A strong-arm sampler.

Due to stacking in strong-arm samplers, the supply voltage scaling in advanced processes negatively affect their performance. The modified two-stage double tail implementation of [56] reduces stacking and illustrated in Fig. 2.24. However, complimentary clocks are required in first and second stage which can be sensitive to differential clock misalignment.

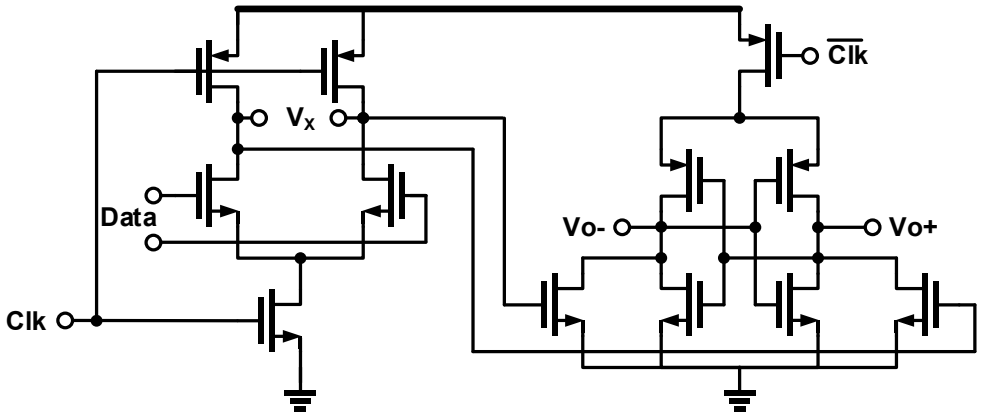

Figure. 2.24: Two-stage double tail sampler block diagram.

An alternative implementation is presented in [57] and depicted in Fig. 2.25. It utilizes a two stage dynamic amplifier along with a regenerative NMOS and PMOS pair in parallel with the final stage to achieve high gain and rail-to-rail output swing. Similar to a strong-arm sampler, this sampler requires only a single-ended clock.

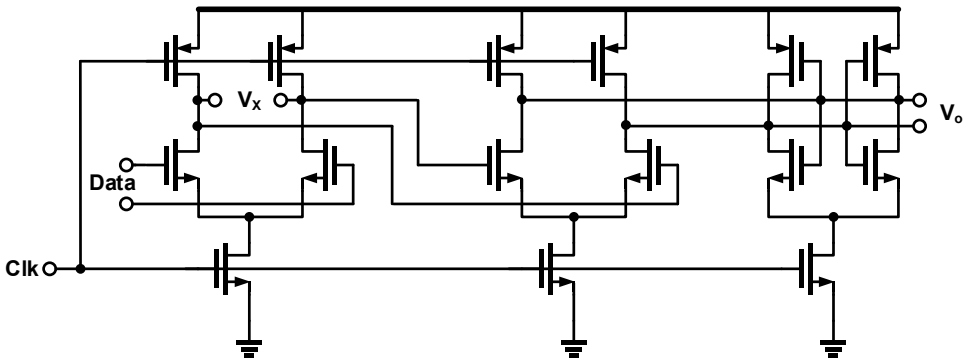

Fig. 2.25: A two-stage dynamic amplifier with regeneration.

Samplers can also be implemented in a current mode manner [58] as depicted in Fig. 2.26. Here, by setting the Rd resistance a compromise between gain and bandwidth can be achieved. It should be noted that the current mode sampler can potentially provide higher bandwidth than strong-arm and two-stage counterparts due to single stage implementation. However, it suffers from static power consumption which is independent of the data-rate.

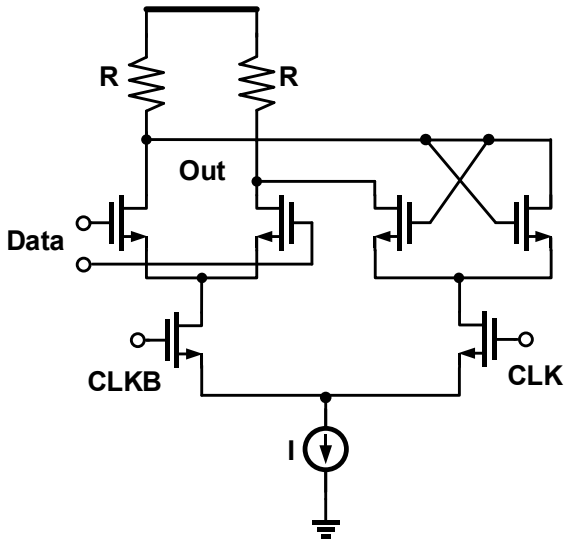

Figure. 2.26: A current mode sampler block diagram.

2.5 Conclusion

This section has summarized the key challenges associated with system and circuit design in wireline mixed-signal transceivers. Effect of frequency dependent channel loss on data transmission has been discussed. Equalization approaches at transmitter and receiver side are explained to overcome ISI caused by limited channel bandwidth. A short summary of critical circuit blocks of transmitter and receiver has been given. Different implementation approaches and trade-offs have been discussed.

3. DUAL-MODE 16/32 GB/S NRZ/PAM4 TRANSMITTER*

3.1 Introduction

Improvements in high-speed serial I/O bandwidth density and energy efficiency are necessary to support the dramatic growth in global IP traffic, which is projected to reach 2 zettabytes per year by 2019 [59]. While high-performance I/O circuitry can leverage technology improvements, unfortunately the bandwidth of the electrical channels used for inter-chip communication has not scaled in the same manner. This merits serious consideration of four-level pulse amplitude modulation (PAM4) which, relative to simple binary non-return-to-zero (NRZ) signaling, offers higher spectral efficiency, lower loss at the Nyquist frequency, and relaxed clock speeds. These advantages have led to implementation of PAM4 modulation in various high-speed I/O standards [42, 43]. In order to support PAM4 modulation, there has been recent developments in current-mode [22, 49, 60, 61], voltage-mode [62], and hybrid transmitters [63], and both analog-to-digital converter (ADC)-based [61, 64, 65], and mixed-signal receivers [49, 60, 66]. Relative to NRZ-based systems, PAM4 transceivers require more stringent circuit linearity, equalizers which can implement multi-level inter-symbol interference (ISI) cancellation, and improved sensitivity.

On the transmitter side, source-series-terminated (SST) voltage-mode drivers enable the high output swing required for PAM4 modulation with high linearity achieved up to

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differential output swings equal to the nominal output stage supply [39]. Further improvements in output swing are possible with advanced hybrid drivers employing current boosting [63]. Voltage mode drivers also offer reduced static power consumption relative to current-mode drivers. Although, at higher data-rates this static power advantage becomes a smaller percentage of the total transmitter power consumption. Key reasons for this include large clocking power and that these voltage-mode drivers often use output-stage segmentation to achieve equalization setting and impedance control. The presence of equalization tap-select muxes that must pass the full-rate signal in the output segments [39] can introduce on-chip ISI and including digitally-controlled redundant segments for impedance control [50] results in increased output stage area and power. Another key transmitter bottleneck is the final serializer, where efforts have been made to minimize power consumption in both current-mode [67] and voltage-mode [68] implementations.

Equalization is often also implemented at the receiver to support higher channel loss, with the most common blocks employed being a continuous-time linear equalizer (CTLE) and a decision feedback equalizer (DFE). Continuous time linear equalization is effective at cancelling both pre-cursor and long-tail ISI. However, CTLE amplifiers must be designed with sufficient bandwidth to support the full rate signal and linearity to support PAM4 modulation. Decision feedback equalization is often used due to the effectiveness of cancelling ISI without amplifying noise or crosstalk [69]. However, a key challenge associated with DFE architectures involves optimizing the critical feedback path to allow for ISI cancellation beginning at the first post-cursor. While PAM4 modulation allows for a longer unit interval (UI) time, the reduced voltage margins necessitate increased

comparator gain to achieve a symbol decision in one UI. Another issue is that DFEs which employ common FIR feedback filters can require a large tap count (>10) to cancel long-tail ISI [70]. An efficient solution for this is to employ IIR feedback filters which can cancel smooth exponentially decaying ISI with a minimal number of taps [41, 57, 68, 71], in a manner similar to a continuous time equalizer. Finally, a PAM4 DFE must implement the necessary hardware with the required linearity to support multi-level ISI subtraction.

While PAM4 has better spectral efficiency relative to NRZ signaling, this doesn't make it the superior modulation option for all systems. The optimal modulation is a function of the target data rate, channel loss profile, and process technology, with the majority of standards utilizing simple binary non-return-to-zero (NRZ) signaling. As serial I/O transceivers are often designed to support different channels and standards, this motivates dual-mode transceivers with flexible equalization (Fig. 3.1) to seamlessly support both NRZ and PAM4 modulation with minimal hardware and power overhead.

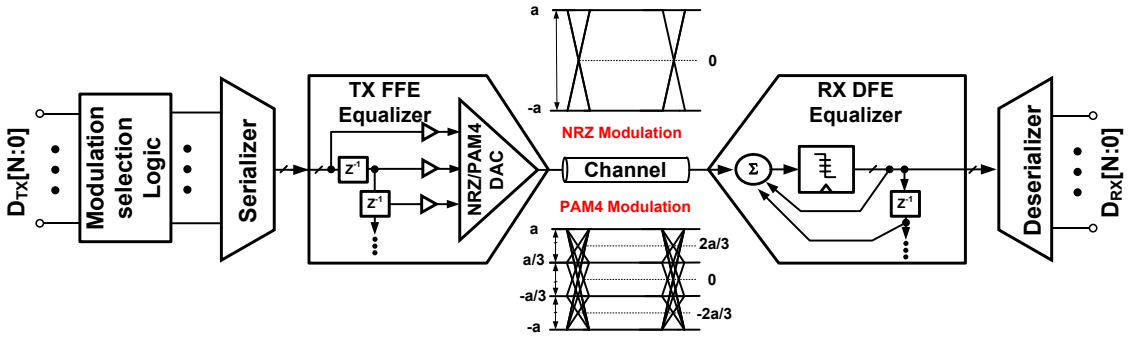


Figure. 3.1: Conceptual dual-mode NRZ/PAM4 transceiver architecture with TX FFE and RX DFE equalizers.

This section presents a quarter-rate 16/32Gb/s dual-mode NRZ/PAM4 SerDes datapath which can be configured to work in both modes with minimal hardware overhead [52]. Section 3.2 investigates the equalization requirements of the proposed transceiver with statistical bit error rate (BER) modeling results of transmit-side FFE used with receive-side DFE structures with either FIR or IIR feedback taps. The high-swing voltage-mode SST transmitter which utilizes an efficient tri-state inverter-based mux with dynamic pre-driver gates, a lookup table (LUT) controlled 31-segment output DAC to implement FFE without any full-rate tap-select muxes, and low-overhead analog impedance control is detailed in Section 3.3. Section 3.4 discusses the receiver that saves power with a quarter-rate DFE that directly samples the input from the termination and achieves efficient equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation [39]. Experimental results from a general purpose (GP) 65nm CMOS prototype are presented in Section 3.5. Finally, Section 3.6 concludes this section.

3.2 System Architecture

High-speed link signal integrity suffers from ISI caused by channel skin effect, dielectric loss, and reflections. The proposed transceiver is designed to support refined electrical channels with minimal performance degradation due to reflections, such as the one shown in Fig. 3.2(a) which displays a smooth low-pass frequency response and 13.5 dB loss at 8GHz. This causes attenuation and dispersion of a 16GS/s data pulse at the channel output. The resultant time-domain ISI in Fig. 3.2(b) is well characterized by a fast rising side with only one significant pre-cursor ISI term, a fast-decaying short-tail ISI term that dominates

through the third post-cursor, and a slow-decaying long-tail ISI term that continues out to higher post cursor locations [41, 69, 71, 72]. While the first pre-cursor ISI term is small, it can significantly degrade performance in PAM4 systems due to this modulation being more sensitive to residual ISI, as further quantified in the Appendix. Thus, transmitter FFE should be utilized to cancel this pre-cursor term and RX DFE can compensate for the post-cursor terms.

The slow-decaying long-tail ISI can have a large impact and necessitate a large tap count in DFEs with conventional FIR feedback filters [70]. Utilizing the 16GS/s pulse response in a statistical BER simulator, the 32Gb/s PAM4 timing margin is compared in Fig. 3.2(c) assuming a 2-tap TX FFE for pre-cursor cancellation and various configurations of RX DFE feedback filters. While 4 FIR DFE taps can achieve a BER<10^{-12}, 9 FIR DFE taps are required to achieve an eye opening close to 10% at this BER. DFEs with IIR taps have been shown to efficiently cancel smooth exponentially decaying ISI, with only one IIR-tap utilized for signaling over an RC-limited on-chip channel [73]. However, a major issue with DFE IIR feedback taps is that the comparator regeneration can limit the time available for the IIR filter output to reach the required amplitude to cancel the large first-post cursor ISI term. This motivates hybrid DFE architectures which employ one FIR feedback tap for the first post-cursor ISI and subsequent IIR taps for long-tail ISI cancellation [71, 74]. Fig. 2(c) shows that by employing one FIR and one IIR feedback tap, a performance better than 5 FIR taps is achieved with 32Gb/s PAM4 modulation. Multiple IIR feedback taps provide more flexibility to tailor the tap time constants and post-cursor location to better match a given PCB channel [69, 75], with close to 10% eye opening at BER=10^{-12}

achieved by employing one FIR and two IIR taps. The pulses responses of Fig. 3.2(d) also confirm that this equalization configuration is effective in cancelling both pre-cursor and post-cursor ISI.

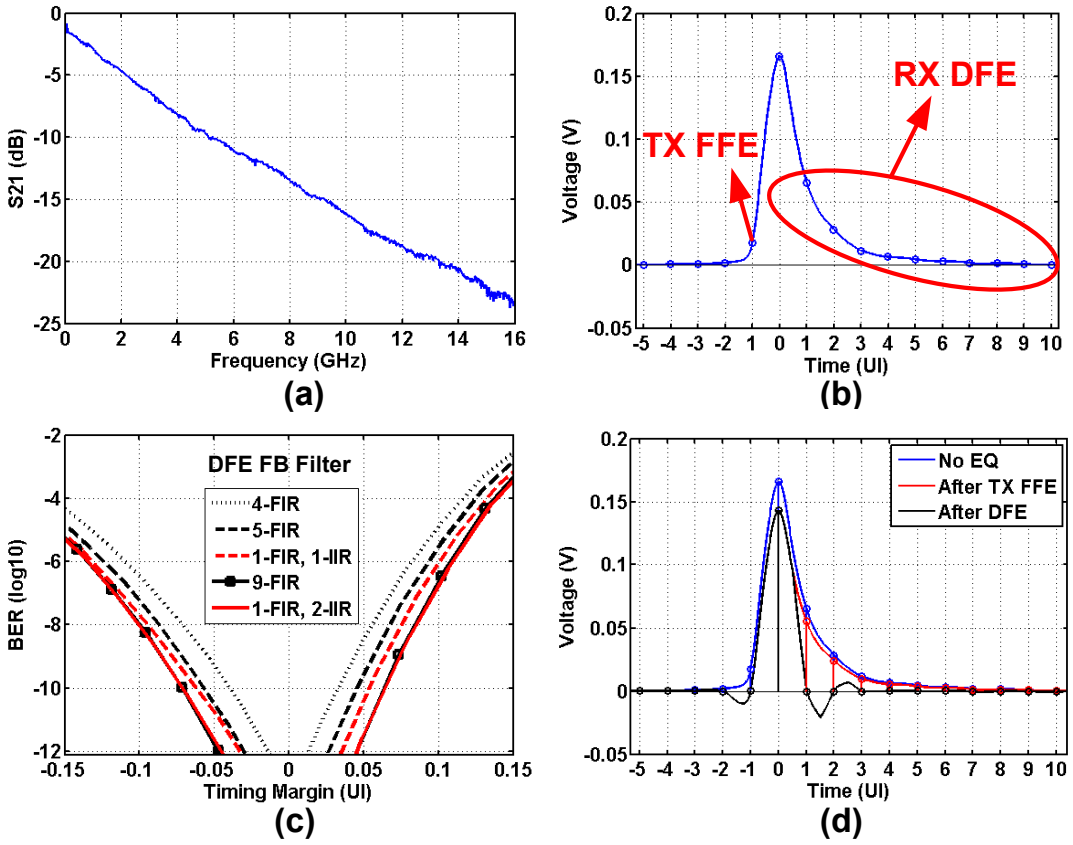


Figure. 3.2: Refined electrical channel (a) S21 response, (b) 16GS/s pulse response, (c) 32Gb/s PAM4 timing margin with 2-tap pre-cursor TX FFE and various RX DFE feedback filter configurations, (d) and 16GS/s pulse response with 2-tap TX FFE and RX DFE with 1-FIR and 2-IIR feedback taps.

Fig. 3.3 shows the proposed dual-mode NRZ/PAM4 transceiver architecture. At the transmitter side, a modulation mode signal selects either a 1/16th or 1/8th symbol-rate

clock to control the 16-bit wide PRBS15 pattern generator and initial serialization stages in NRZ and PAM4 mode, respectively, to generate four sets of four-bit patterns which address the LUT equalizer that controls the 31-segment high-swing SST output stage. This allows the realization of a 4/2-tap FFE in NRZ/PAM4 mode, respectively. At the receiver side, a quarter-rate 3-tap NRZ/PAM4 DFE is utilized with 1 FIR and 2 IIR feedback taps. The three output bits per quarter-rate slice, which are all the same value for NRZ and thermometer-code for PAM4, are converted to binary and buffered out of the chip for BER testing.

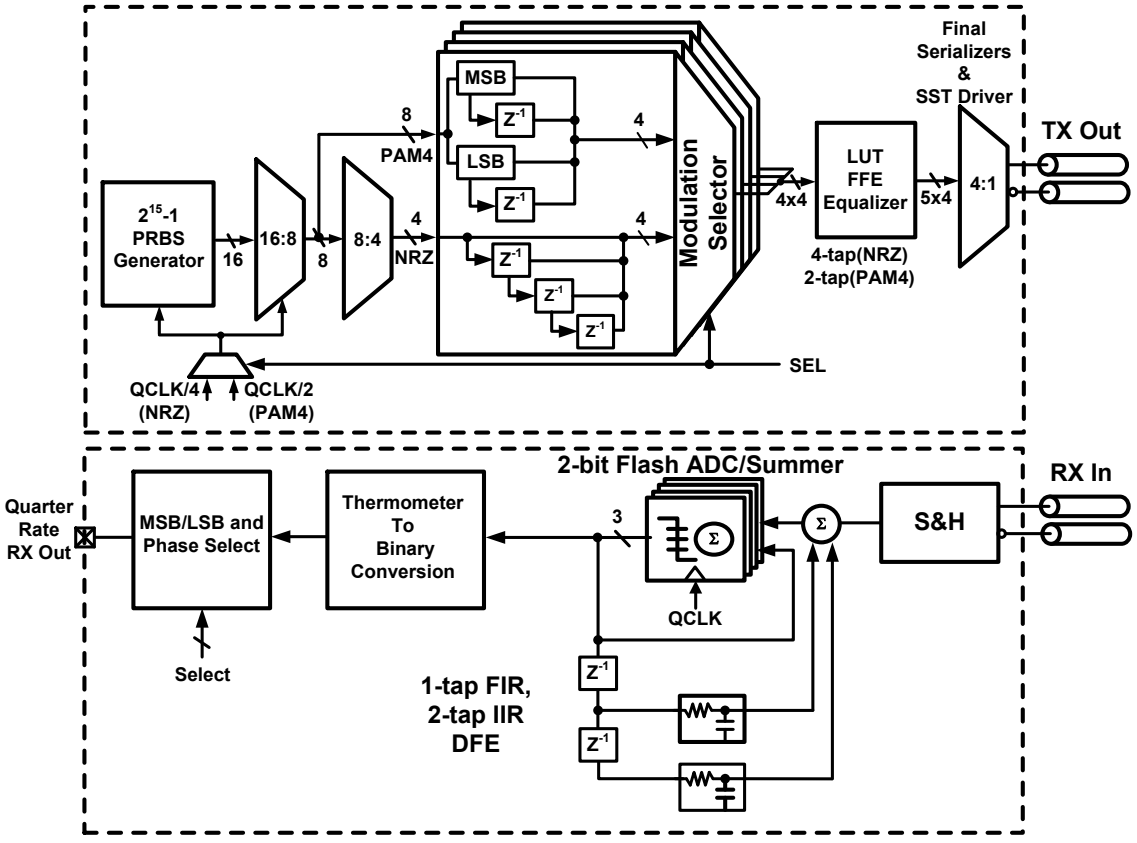


Figure. 3.3: Dual-mode NRZ/PAM4 transceiver architecture.

3.3 Transmitter Architecture

Fig. 3.4 shows the detailed transmitter block diagram. The quarter-rate architecture uses four sets of four-bit patterns from the on-chip PRBS15 generator to address the 16x5 element LUT equalizer by controlling four 5-bit 16-to-1 muxes. This allows the realization of a 4-tap FFE in NRZ mode, with a main cursor and up to three pre/post cursor taps, and a 2-tap FFE in PAM4 mode, with a main cursor and either one pre/post cursor tap for the MSB and LSB bits. The LUT provides for 5-bit resolution in the output stage level generation, eliminates any full-rate tap-select muxes in the output segments [39], and also allows for potential non-linear equalization. After a retiming stage, a final quarter-rate dynamic tri-state inverter-based 4-to-1 stage serializes the 5-bit resolution LUT output to full rate to drive the 31-segment high-swing SST output stage. Finally, the driver output impedance is efficiently set to near 50 Ω with a pseudo-analog control loop. In order to compensate for phase mismatches in the critical serialization clocks, per-phase digitally-controlled delay lines with adjustable duty cycle and delay are inserted in the clock distribution network. While not implemented in this prototype, a calibration scheme can be utilized similar to [52] to automatically correct phase mismatches and provide uniform output eyes.

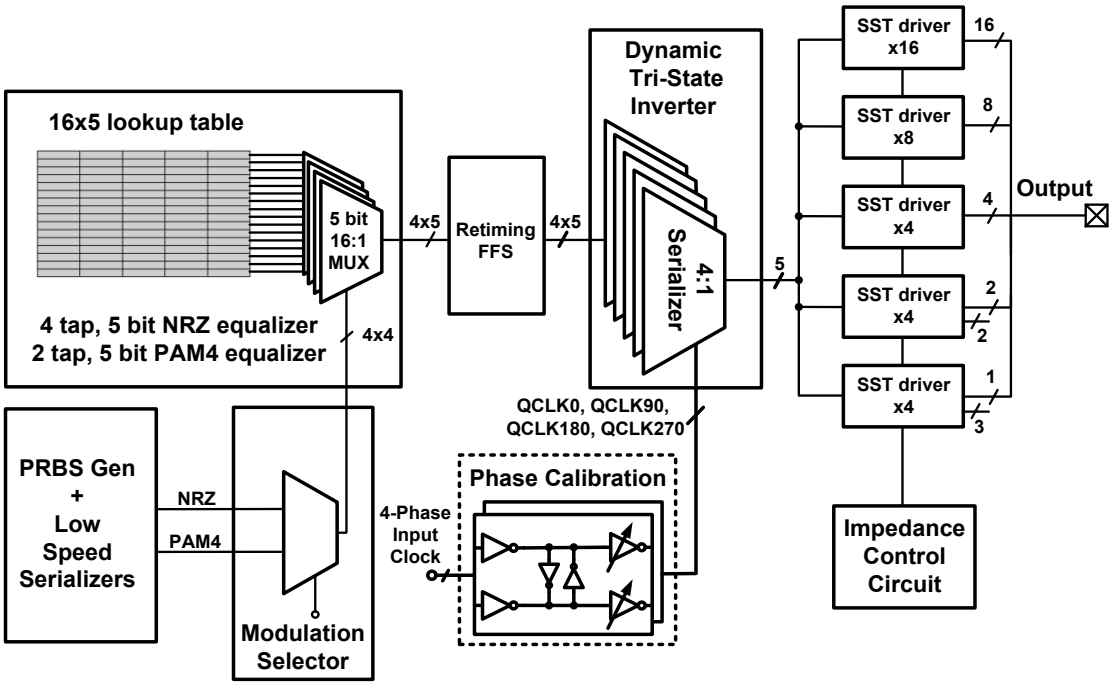


Figure. 3.4: NRZ/PAM4 transmitter with lookup table-based FFE equalizer and pseudo-analog impedance control.

3.3.1 4-to-1 Serializer

The final 4-to-1 serializer is one of the most critical blocks in a quarter-rate transmitter, as it must maintain enough bandwidth to support the full-rate output. However, this can be difficult to achieve with conventional pass-gate serializers which suffer from reduced drive strength due to the effective transistor stacking at the high self-loading output node. This transmitter extends the 2-to-1 tri-state inverter-based mux design proposed in [46] to perform 4-to-1 serialization and further improves power efficiency by utilizing dynamic NAND pre-drivers (Fig. 3.5(a)). Fig. 3.5(b) shows the serializer's PMOS-path timing diagram, with similar waveforms present in the NMOS-path. The dynamic NAND

predriver gates utilize the input data to qualify a pulse defined by adjacent quarter-rate clock edges. This allows the tri-state inverter-based mux to drive the full-rate output node through only a single transistor, similar to a simple inverter, with the input data activating one of the PMOS/NMOS devices. Dummy gates are present in both the PMOS and NMOS paths to enable a uniform eye diagram at the full-rate serializer output. As shown in the post-layout simulation results of Fig. 3.5(c), the proposed dynamic tri-state inverter-based design has significantly faster transition times relative to a conventional pass-gate serializer designed with equal power consumption. Overall, the minimal transistor stacking allows the proposed serializer to achieve the same level of deterministic jitter with a 40% power reduction relative to a conventional pass-gate design.

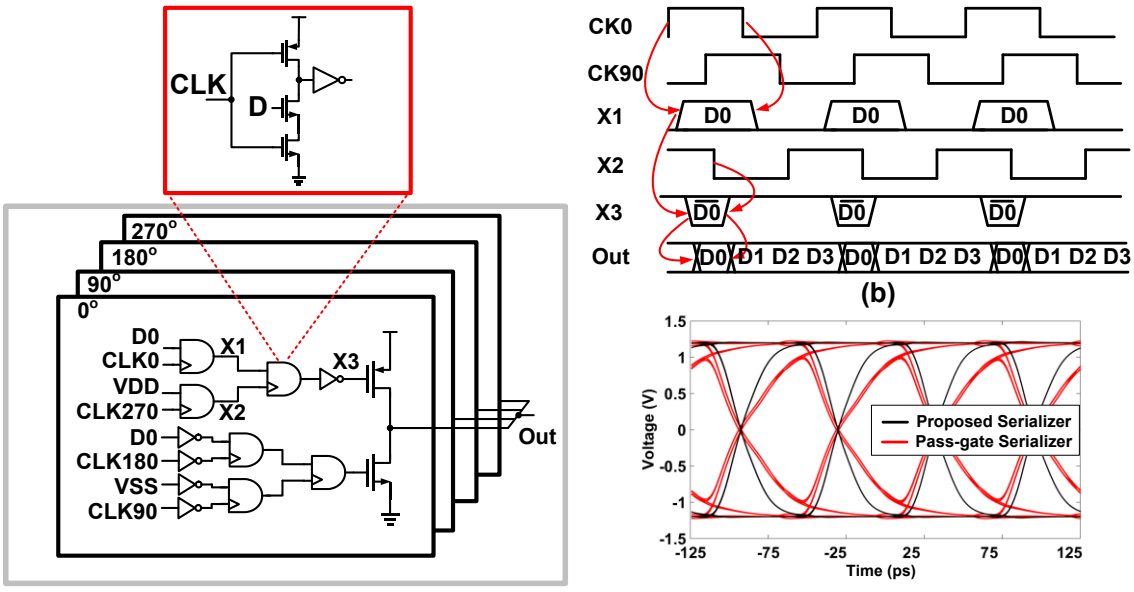


Figure. 3.5: Dynamic tri-state inverter-based 4-to-1 serializer: (a) schematic, (b) timing diagram (PMOS path), and (c) simulated performance comparison with a conventional pass-gate design.

3.3.2 Pseudo-Analog-Controlled Output Driver

Fig. 3.6(a) shows a single segment of a conventional high-swing source-series-terminated output driver. The segment's output impedance is set by the series combination of the passive resistor, Rterm, and the transistor's triode resistance. As shown in the simulation results of Fig. 3.6(c), both of the elements are affected by process variations and can cause deviations in the driver output impedance without any compensation (No comp). A straight-forward technique to control the output impedance of a high-swing voltage-mode driver involves implementing redundant segments that can be digitally activated to match the channel impedance [50]. However, the presence of these redundant stages results in increased output stage area and pre-driver power.

This design proposes pseudo-analog control to compensate for large statistical variations in driver output impedance. Fig. 3.6(b) shows a schematic of the voltage-mode SST driver segments which supports a 1.2 Vpp output swing. Here the main MP and MN switch transistors and Rterm resistors are sized to always yield greater than 50 Ω output impedance over corners, and two analog-controlled paths are added for impedance tuning via the GP/N gate voltages. While conceivably one additional analog-controlled branch is sufficient for impedance control, a trade-off exists in choosing RP and RN values. As shown in Fig. 3.6(c), selecting a relatively small RP and RN value to yield near 50 Ω under a +3σ variation case (Single leg comp1) results in low overdrive voltages for the MRP and MRN transistors under a nominal impedance corner. This causes a large positive deviation from the desired 50 Ω value due to the transistors entering the saturation region with a small-signal output impedance higher than the large-signal value set by a conventional

analog control loop. Conversely, selecting a relatively high RP and RN value to yield near 50 Ω under a nominal variation case (Single leg comp2) results in insufficient overdrive voltage range and a large positive deviation under a +3σ impedance corner. Thus, in order to break this trade-off, a two branch compensation approach with both analog-controlled low-impedance path 1 and high-impedance path 2 are added which are replica-biased by the FSM-controlled pseudo-analog loop.

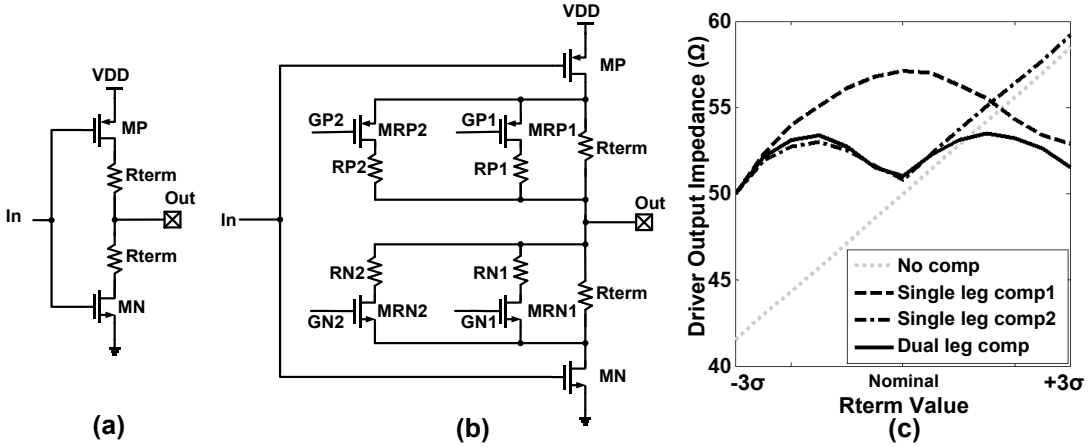


Figure. 3.6: (a) Conventional SST output driver segment. (b) Proposed output driver segment with pseudo-analog impedance control. (c) Simulated output impedance vs. process corners.

Fig. 3.7 shows the output driver impedance controller that produces the output voltages, GP1, GN1, GP2, and GN2, that control the low/high-impedance paths' pull-up and pull-down resistances. The impedance controller consists of a replica transmitter stage with a precision off-chip 100 Ω resistor load that is placed in two feedback loops. Depending on the control-loop mode, the top loop sets the MRP1/2 transistors' gate voltage with either the analog control signal VOP or in a digital fashion to be fully-on (VSS) or full-off (VDD)

in order to force a value of (3/4)*VDD at the replica transmitter positive output. The bottom loop works in a similar manner to force a value of (1/4)*VDD at the replica transmitter negative output. For corners with low output resistance, the impedance tuning circuitry operates with the lower-impedance path 1 in the feedback loops to set analog voltages GP1/GN1 with VOP/VON to yield a 50 Ω match, while the higher-impedance path 2 is disabled (Mode 1). In Mode 1, both the replica driver and the main output driver segments share the same control signals. For corners with high output resistance, path 1 switches from analog to digital control and is turned fully on, while the higher-impedance path 2 is now in the feedback loops to set analog voltages GP2/GN2 with VOP/VON to yield a 50 Ω match (Mode 3). In Mode 3, again both the replica driver and the main output driver segments share the same control signals. For corners with close-to-nominal output resistance, the main output driver is designed to operate with path 1 simply set fully on and path 2 disabled, while the replica loop controls either the low- or high-impedance path depending on the previous state (Mode 2A/B). Switching between the modes in the replica loop without dithering the control signals presented to the main output driver is achieved by an asynchronous FSM that monitors the VON voltage. As shown in the Fig. 3.7 flowchart, in the nominal impedance case the replica driver will be continuously switching between the low-impedance (Mode 2A) and high-impedance (Mode 2B) modes without disturbing the output driver segments. In Mode 2A with the low-impedance path in feedback, the loop checks whether VON is less than a high threshold VH, corresponding to deep triode operation of MRN1, minus some margin before transitioning to Mode 1 with analog control of the low-impedance path 1 in the main output stage segments. In

Mode 2B with the low-impedance path fully on and the high-impedance path in feedback, the loop checks whether VON is greater than a low threshold VL, corresponding to a minimum conductance level from MRN2, plus some margin before transitioning to Mode 3 with analog control of the high-impedance path 2 and the low-impedance path 1 fully on in the main output stage segments. The margin introduced in transitioning between Modes 1/2 and 2/3 introduces hysteresis which, along with the extra Mode 2 state, prevents dithering in the main output segment impedance control signals.

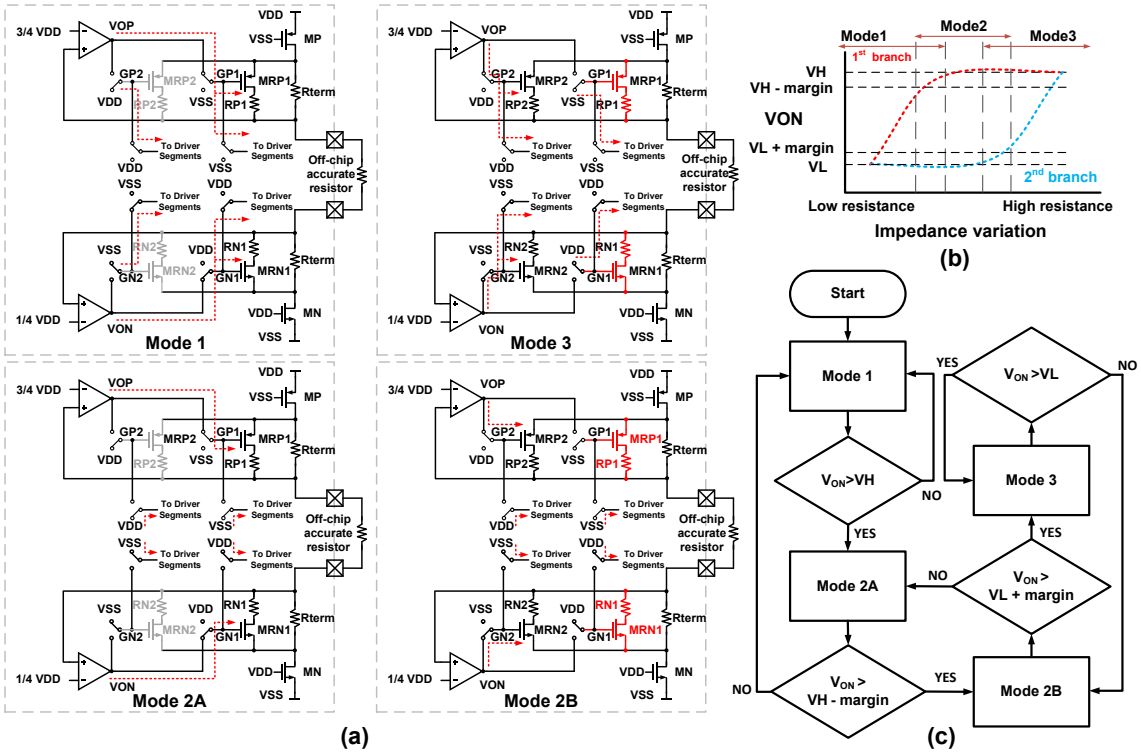


Figure. 3.7: Impedance control loop: (a) different operation modes, (b) NMOS control OTA output voltage VON in different modes, and (c) FSM flow chart.

Robust operation of the replica bias impedance control scheme in the presence of mismatch is ensured since the analog-controlled MRP and MRN transistors are always

biased in the triode region with a large overdrive voltage. In order to quantify the effect of both process variation and mismatch between the replica and output driver segments, the output driver's post-layout simulated return loss plot is shown in Fig. 3.8 with ±3σ error bars. While there is some slight variation over the process corners, the small error bars indicate that the mismatch-induced variation for a given corner is minimal. Overall, the simulation results show a worst-case return loss of -27.4 dB and -10.5 dB at 500 MHz and 8 GHz, respectively.

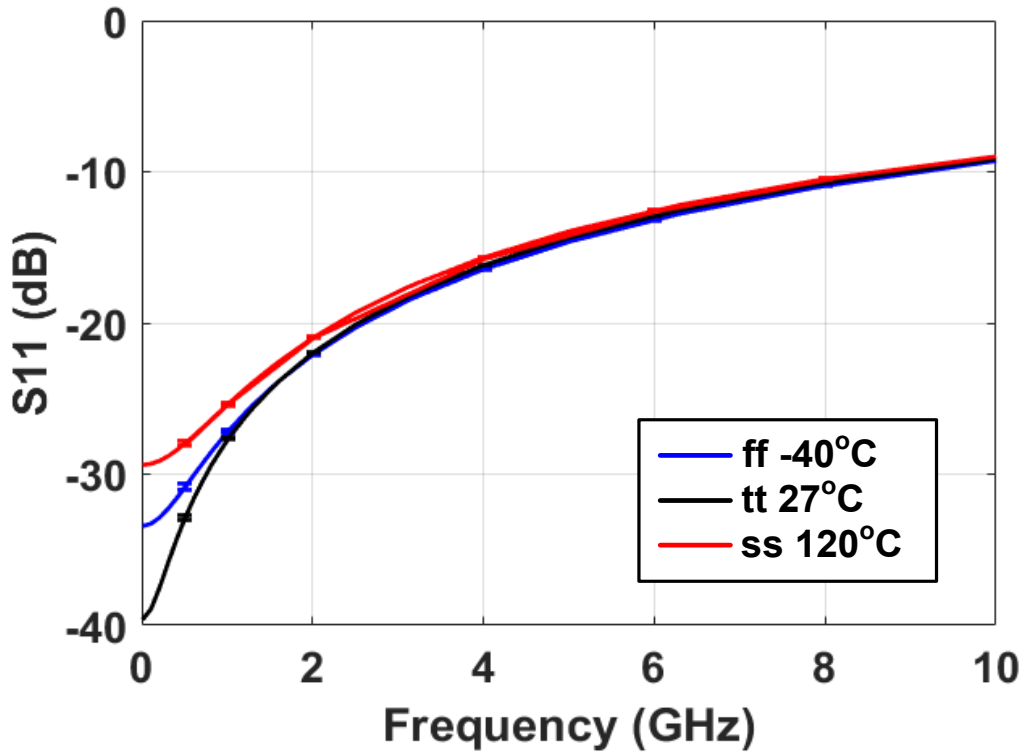


Figure. 3.8: Monte Carlo simulations of the output driver S11 for different process corners with ±3σ error bars for mismatch at a given corner included.

3.4 Experimental Results

The dual-mode NRZ/PAM4 SerDes was fabricated in a 65-nm CMOS general purpose process. As shown in the die micrographs of Fig. 3.9, the total active area for the transmitter is 0.06 mm2 and the DFE receiver core is 0.014 mm2. The four phase clocks for the quarter-rate SerDes is generated on both chips by passing a half-rate differential input clock through on-chip CML divide-by-2 blocks followed by CML-to-CMOS converters and local clock buffers.

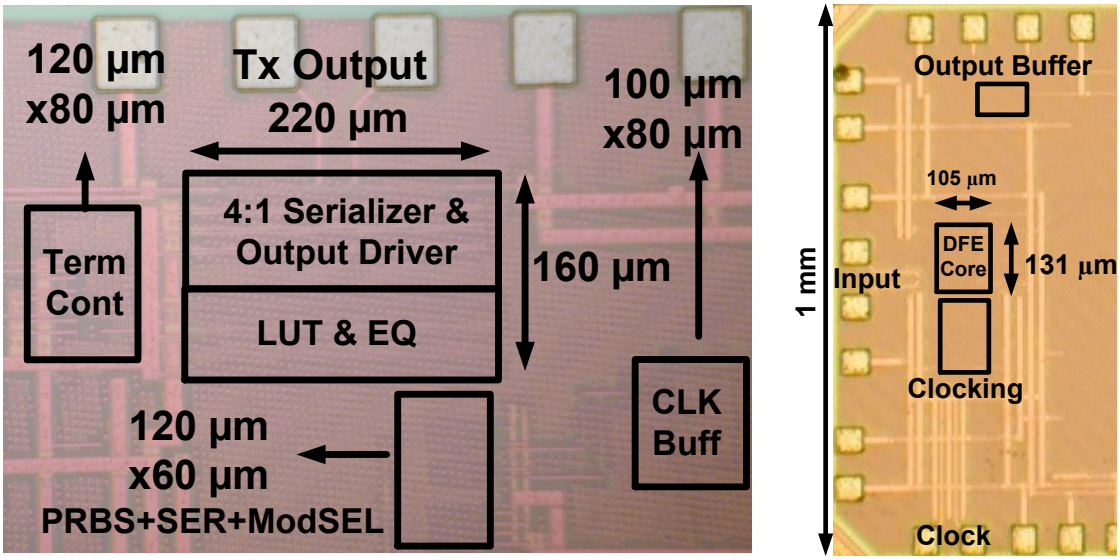


Figure. 3.9: Chip micrograph of (a) transmitter and (b) receiver.

Fig. 3.10 shows measurement results of the transmitter positive and negative output pin impedance versus output differential voltage for 5 different transmitter chips. The impedance control loop ensures that the output stage maintains near a 50 Ω output impedance over the entire 1.2 Vpp range for both nominal samples (1-4) which operate in

Mode 2 and the high-impedance variation sample 5 which operates in the analog-controlled Mode 3. Fig. 3.11 shows level separation mismatch ratio (RLM) measurements which highlight the utility of the LUT-based transmitter. Utilizing the default PAM4 settings results in a 93% RLM, with the third level being somewhat low in this sample. Optimizing the LUT settings allows for an improved 96.7% RLM and more uniform level spacing.

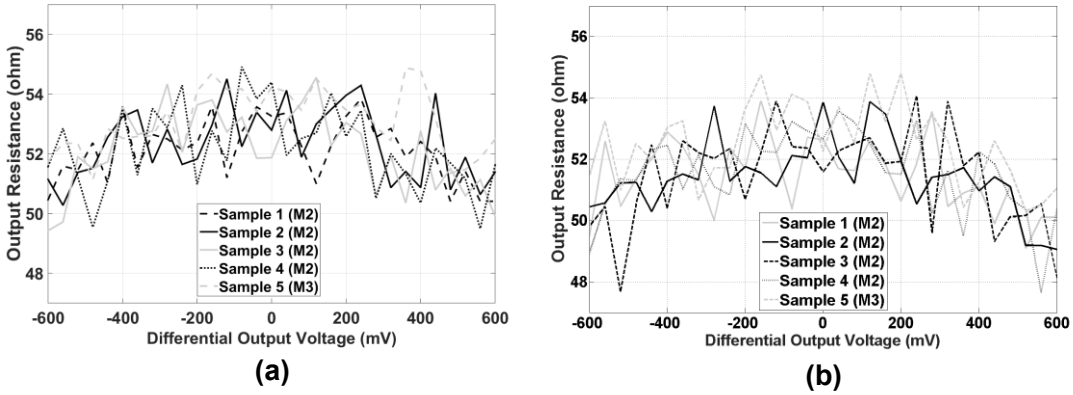


Figure. 3.10: Measured transmitter output impedance versus differential output voltage for (a) positive output pin and (b) negative output pin.

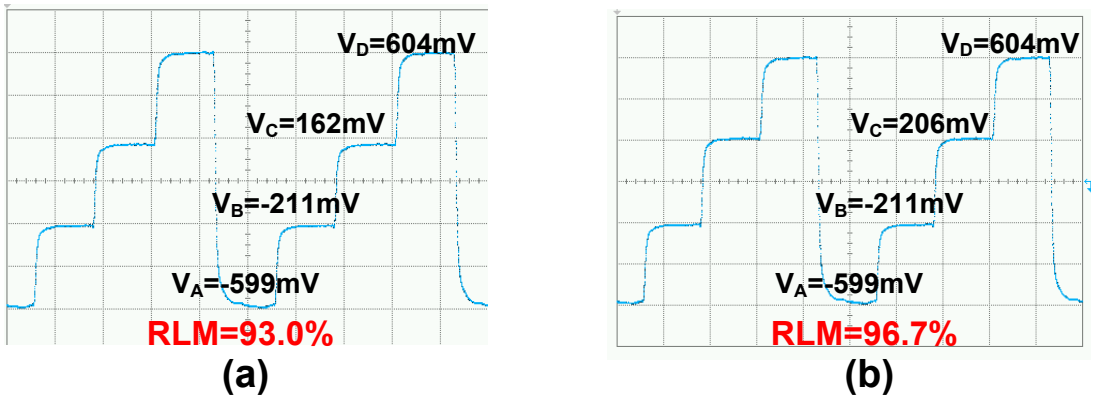


Figure. 3.11: Level separation mismatch ratio (RLM) measurement results for (a) nominal PAM4 level settings and (b) optimized PAM4 level settings.

A block diagram of the link BER test setup and measurements of the two test channels' insertion loss is shown in Fig. 3.12. Eye diagrams are captured at the output of the test channels, excluding the RX PCB loss of about 3 dB at 8 GHz, utilizing a high-bandwidth sampling scope to characterize the transmitter. Full link testing is performed with two synchronized sources to generate the transmitter and receiver clocks. A programmable phase shifter is inserted in the receive-side path to manually adjust the phase and generate BER bathtub curves. This receive-side clock is also used to clock the BERT. In PAM4 mode, the on-die quarter-rate data MUX at the receiver output allows for independent verification of the MSB or LSB outputs. These results are then combined to produce the receiver BER bathtub curves in PAM4 mode.

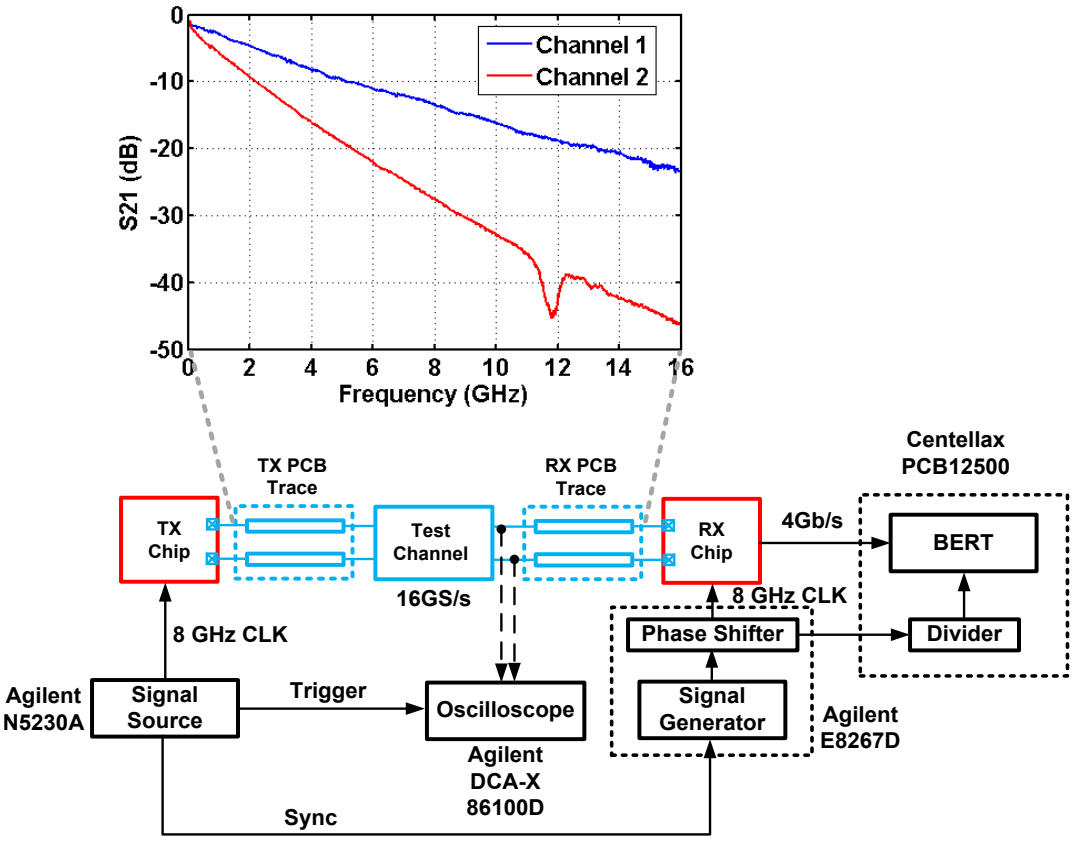


Figure. 3.12: Dual-mode NRZ/PAM4 transceiver test setup.

The transmitter eye diagrams at the channels' outputs and the full-link BER timing margin bathtub curves are shown in Fig. 15 and Fig. 16, respectively. Fig. 16 also includes the utilized TX and RX equalizer settings, with initial values obtained using the statistical simulation model discussed in Section 3.2 and further manual fine tuning employed to achieve the lowest BER. 32 Gb/s PAM4 operation is achieved over channel 1, which has 13.5 dB loss at the 8GHz Nyquist frequency. The left half of Fig. 3.13 shows that without any transmit equalization the output eye diagram is completely closed. As shown in Fig. 3.14(a), utilizing only RX equalization in this case allows for only a BER near 10^{-10}. While

only optimizing the PAM4 2-tap TX FFE allows for open eyes at the channel output before the RX PCB, the additional board loss results in only 0.02UI timing margin at a BER=10^{-12} without any receiver equalization. Co-optimizing the 2-tap TX FFE for pre-cursor ISI cancellation with the RX DFE for post-cursor cancellation allows this timing margin to increase to 0.06UI. Note that in this co-optimized condition the eye diagram at the RX PCB input is completely closed, as shown in Fig. 3.13(c). 16 Gb/s NRZ operation is achieved over channel 2, which has 27.6 dB loss at the 8 GHz Nyquist frequency. The right half of Fig. 3.13 shows that without any transmit equalization the output eye diagram is completely closed. As shown in Fig. 3.14(b), utilizing only RX equalization in this case allows for only a BER near 10^{-8}. Optimizing the NRZ 4-tap TX FFE allows for open eyes at the channel output before the RX PCB, as depicted in Fig. 3.13(e). Jitter decomposition of this eye yields 34.3 ps of deterministic jitter, with 31.2 ps of residual ISI being the main contributor. The random jitter is measured at 830 fsrms using a clock source with 750 fsrms random jitter. A timing margin of 0.08UI at a BER=10^{-12} is achieved without any receiver equalization. This timing margin is improved to 0.18UI with co-optimization of the 4-tap TX FFE and RX DFE. As in the PAM4 case, in this co-optimized NRZ condition the eye diagram at the RX PCB input is completely closed, as shown in Fig. 3.13(f).

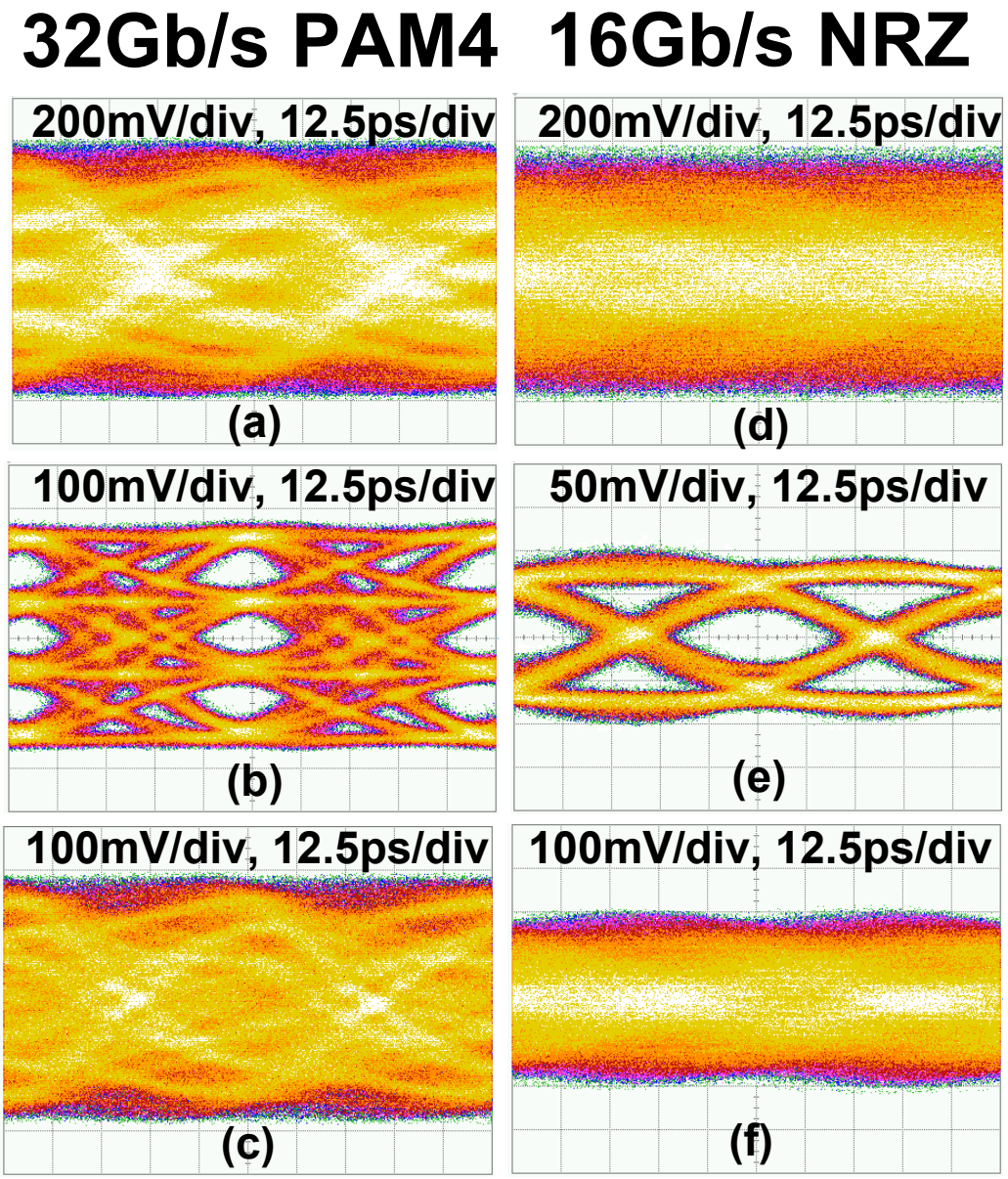


Figure. 3.13: 32Gb/s PAM4 eye diagrams over channel 1: (a) without TX equalization, (b) with optimal 2-tap TX-only FFE settings, and (c) with the 2-tap TX FFE settings co-optimized with the RX DFE to yield maximum timing margin. 16Gb/s NRZ eye diagrams over channel 2: (d) without TX equalization, (e) with optimal 4-tap TX-only FFE settings, and (f) with the 4-tap TX FFE settings co-optimized with the RX DFE to yield maximum timing margin.

Equalizer Settings			TX Only	RX Only	TRX
TX FFE Coefficients		a_{-1}	-	-	-0.1
		a_0	0.7	1	0.9
		a_1	-0.3	-	-
RX DFE Settings	FIR Weight (mV)	FIR	-	52	71
	IIR Amplitude (mV)	IIR1	-	24	24
		IIR2	-	-4	8
	IIR Time Constant (UI)	IIR1	-	2	0.5
		IIR2	-	3	3

Equalizer Settings			TX Only	RX Only	TRX
TX FFE Coefficients		a_{-2}	-	-	0.04
		a_{-1}	-0.06	-	-0.18
		a_0	0.51	1	0.62
		a_1	-0.36	-	-0.16
		a_2	0.07	-	-
RX DFE Settings	FIR Weight (mV)	FIR	-	27	30
	IIR Amplitude (mV)	IIR1	-	18	10
		IIR2	-	8	4
	IIR Time Constant (UI)	IIR1	-	1.5	1
		IIR2	-	5	4

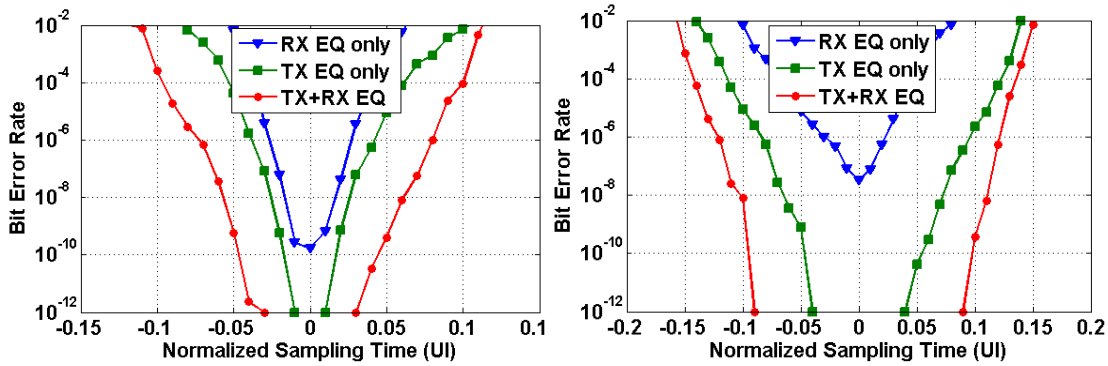


Figure. 3.14: Transceiver equalizer settings and bathtub curves for (a) channel 1 at 32 Gb/s PAM4 and (b) channel 2 at 16 Gb/s NRZ.

Table 3.1 summarizes the multi-mode transceiver performance and compares this work against other dedicated NRZ and PAM4 designs. Relative to the mixed-signal PAM4 designs of [60] and [49], the presented transceiver's additional equalization functionality allow for compensation of higher channel loss. Better power efficiency and significant area reduction is also achieved relative to a 16-nm ADC-based PAM4 transceiver [76]. Comparing against NRZ designs, the presented dual-mode transceiver achieves a higher 32 Gb/s data rate in PAM4 mode at a better power efficiency than a 28-nm design operating at 28 Gb/s NRZ [39]. Also, superior power efficiency in NRZ operation is

achieved relative to the 16 Gb/s 40-nm design which utilizes a DFE with 14 FIR feedback taps [49]. Fig. 3.15 shows the 32 Gb/s power breakdown. The transmitter consumes 158.6 mW of power, with the 4-to-1 serializer and local clock buffers having the most contribution. Only 17.7 mW is consumed at the receiver, with the local clock buffers and comparators dominating.

Table 3.1: Transceiver Performance Summary

References	This Work		[60]	[49]	[76]	[39]	[67]
Data Rate	32 Gb/s	16 Gb/s	20 Gb/s	56 Gb/s	56 Gb/s	28 Gb/s	16 Gb/s
Equalization	2-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	4-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	3-tap TX FFE	3-tap TX FFE + 1-tap RX DFE	3-tap TX FFE + RX CTLE + ADC based RX 24-tap FEE, 1-tap DFE	5-tap TX FFE + RX CTLE + 14-tap RX DFE	3-tap TX FFE + RX CTLE + 14-tap RX DFE
Modulation	PAM4	NRZ	PAM4	PAM4	PAM4	NRZ	NRZ
Total Loss @ Nyquist	13.5 dB	27.6 dB	5 dB	2 dB	25dB	40 dB for 25.78 Gb/s	34 dB
Eye Width BER	6% 10^{-12}	18% 10^{-12}	- 10^{-12}	- 10^{-12}	- 10^{-8}	23% 10^{-12}	- 10^{-15}
Supply (V)	1.2 TX, 1 RX		1.8	1.2	0.9 digital, 1.2 analog, 1.8 auxiliary	1 TX & RX, 1.25 TX driver	1/1.5 TX, 0.9 RX
Power (mW) (mW/Gbps)	176.3 5.5	173.7 10.9	408 20.4	475 8.5	550* 9.8	295* 10.5	235* 14.7
Area (mm^2)	0.074		0.43	2.74	1.4	0.62	2.15
Technology	65-nm		90-nm	65-nm TX, 40-nm RX	16-nm FinFET	28-nm	40-nm

*Clock generation and CDR power included

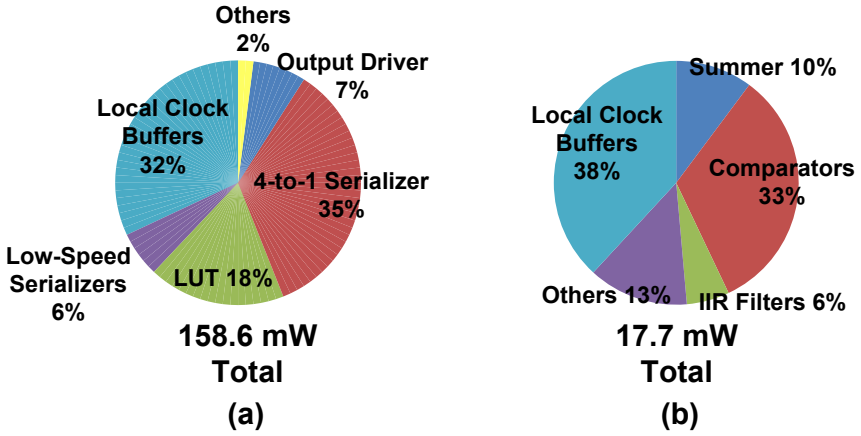


Figure. 3.15: 32 Gb/s power breakdown of (a) transmitter and (b) receiver.

3.5 Conclusion

This section has presented a 16/32 Gb/s dual-mode NRZ/PAM4 SerDes which can be configured to work in both modes with minimal hardware overhead. The SST transmitter achieves 1.2 Vpp output swing and employs lookup table control of a 31-segment output DAC to implement 4/2-tap FFE in NRZ/PAM4 modes, respectively. Power efficiency is improved in the transmitter with an optimized quarter-rate serializer and a new low-overhead analog impedance control scheme is employed in the output stage to obviate additional impedance control segments. The presented DFE receiver utilizes a new single-clock phase two-stage regenerative comparator in the 2-bit flash ADCs to allow sufficient gain to support PAM4 DFE. Improved sensitivity is achieved in the direct feedback design with the multi-level first post-cursor ISI subtracted in the comparators and the remaining ISI cancelled in a preceding current integration summer. Overall, leveraging the proposed dual-mode SerDes architecture allows the support of multiple channel conditions and variable data rates with a single design solution.

4. PAM4 56 GB/S RECEIVER WITH THRESHOLD AND DFE ADAPTATION

4.1 Introduction

Supporting the increasing demand for higher bandwidth in datacenters and telecommunication infrastructure requires increased data-rate per lane for electrical interfaces. While I/O circuit bandwidth and power efficiency can leverage technology improvements, as upgrading the current infrastructure require major investment, channel bandwidths have remained constant prohibiting reliable communication beyond 50Gb/s in traditional non-return-to-zero (NRZ) signaling due to excessive channel loss and reflections. This has motivated employing PAM4 signaling in new high-speed I/O standards owing to higher spectral efficiency it provides [42, 43].

Adoption of PAM4 signaling, however, increase complexity of system both at transmitter and receiver sides. The inherent multi-level signaling increases the complexity of transmitter FFE by a factor of 2, making many-tap equalizers prohibitive in terms of power. The receiver is required to make multi-level decisions and implement equalizers that can cancel long-tail multi-level ISI while maintaining linearity and power efficiency. Fig. 4.1 shows block diagram of such a system. The focus of this work is on the receiver side while trying to minimize the equalization requirement on the transmitter side.

While ADC-based receivers are well suited for PAM4 signaling [77], due to inherent multi-level detection and possibility of implementing robust many-tap DFE and FFE equalizers in digital domain, they generally consume high power. This motivates a power-efficient mixed-signal receiver front-end solution for these applications. However, several challenges are faced in a mixed-signal PAM4 receiver design. Increased sensitivity of

PAM4 to noise and residual ISI enforce stringent ISI cancellation requirements. This can lead to increased tap counts in transmitter side FFE equalization, multi-stage power hungry receiver side CTLE equalization [77-79], and receiver side DFEs that have large tap counts when implemented with FIR feedback filters [78]. While CTLE is effective in canceling the long-tail ISI, the linear amplifiers must be designed with sufficient bandwidth to support the full rate signal and linearity to support PAM4 modulation and enough peaking to compensate for the target channel loss. This often results in multi-stage CTLE implementations with excessive area overhead due to inductive peaking required to maintain the bandwidth at high data-rates. An alternative to using CTLE and many-tap DFEs is to utilize DFEs which combine FIR and IIR feedback filters [57, 69]. However, due to main cursor loss, supporting channels with over 15dB of loss at Nyquist requires excessive slicer sensitivity in the frontend [29].

Similar to an NRZ system, DFE taps should be adaptively tuned for robust operation. The extra challenge associated with PAM4 operation is multi-level channel and equalization dependent thresholds which also require to be adaptively tuned. These adaptations should be done with minimal hardware overhead and offer compatibility with clock recovery architectures that support PAM4 modulation. A PAM4 threshold

adaptation based on difference between input data and summation of input data and positive and negative thresholds is proposed in [80]. In addition to high speed summer and slicer overhead, the proposed method relies heavily on equal spacing of PAM4 levels which is sensitive to non-linearity of both transmitter and receiver frontend.

This section presents a 56 Gb/s mixed-signal PAM-4 quarter-rate receiver with background threshold and DFE adaptation which utilizes phase locked loop (PLL) based clock and data recovery (CDR). Section 4.2 investigates the optimal equalization solution to achieve successful transmission over the target channel using statistical bit error rate (BER) modeling. The PAM4 receiver architecture employing a single-stage CTLE and a 1 FIR and 1 IIR-tap DFE to efficiently cancel long-tail ISI and utilizing a bang-bang phase detector (BBPD) PLL-based CDR recover the clock using only one per-slice edge sampler is detailed in section 4.3. Section 4.4 discusses a background sampler threshold adaptation scheme which doesn't rely on equal level spacing of PAM4 levels using only an additional single per-slice sampler that periodically scans the top and bottom of PAM4 eyes as well as the DFE adaptation scheme of [71] is extended for PAM4 operation with independent per-slice tap values for mismatch robustness utilizing the same edge slicers used in CDR. Experimental results from a general purpose (GP) 65nm CMOS prototype is presented in section 4.5. Finally, section 4.6 concludes the section.

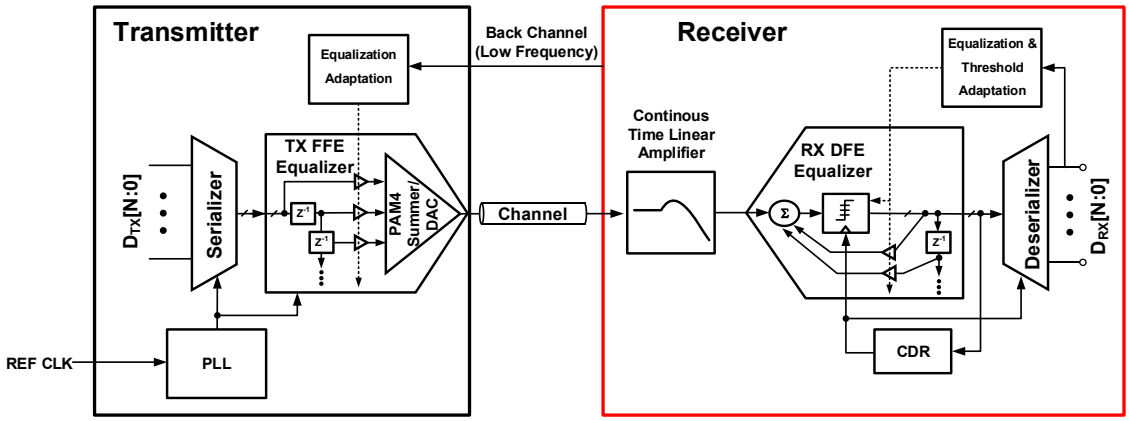


Figure. 4.1: Conceptual block diagram of a PAM4 transceiver with transmitter and receiver side equalization, equalizer and threshold adaptation, and clock recovery circuit.

4.2 System Analysis

The proposed receiver is designed to support PAM4 transmission over refined electrical channels with minimal performance degradation due to reflections. Fig. 4.2(a) shows the frequency response of such a channel with 20.8dB of loss at 14GHz. ISI caused by skin effect and dielectric loss with results in attenuation and dispersion of input pulses at the output of the channel. This results in pulse response of Fig. 2(b) (blue curve) which can be well characterized by a fast rising side with one significant pre-cursor ISI term, and a slow-decaying long-tail ISI on the other side with significant ISI terms up to tenth post-cursor. Due to increased sensitivity of PAM4 to ISI compared to NRZ, an appropriate cancellation of all these terms should be done in order to have error free transmission over this channel. A 3-tap DFE with 1-FIR and 2-IIR taps [29] can cancels out the post-cursor terms appropriately as illustrated in pulse response of Fig. 4.2(b) (green curve) while avoiding any CTLE. However, due to significant pre-cursor term minimum BER will be higher than 10^{-3} as depicted in voltage and bathtub curves of Fig. 4.2(c) and (d). A 2-tap

transmitter side FFE equalizer can be used to cancel the large pre-cursor tap as illustrated in Fig. 4.2(b) (red curve) while using the same 3-tap DFE on the receiver side [72]. This plot shows the pulse response with optimal transmitter and receiver equalizer settings. It can be noted from the pulse response that the 2-tap FFE equalizer with optimal settings won't cancel out the pre-cursor sufficiently. The reason is that by increasing the pre-cursor coefficient beyond this point, the second pre-cursor ISI term will become larger while the main cursor becomes smaller and overall BER of the system will degrade. As depicted in bathtub curves of Fig. 2(c) and (d), this will result in BER of worse than 10^{-10}. In order to achieve better pre-cursor cancellation, more pre-cursor taps are required at the transmitter side. While CTLE has relatively similar behavior to DFE IIR-tap, it has some advantages and disadvantages in comparison. As discussed in section 4.1 relying solely on CTLE for long-tail ISI cancellation can be area hungry due to required peaking. One advantage of CTLE over IIR tap is that while the domain of effect for both is in the post-cursors, an active CTLE boost the main cursor reducing the system sensitivity to residual ISI. By replacing one of the DFE IIR taps with a single stage CTLE with a feasible 6dB of high frequency peaking we can break the trade-off between using CTLE and DFE IIR taps. Fig. 4.2 (b) (black curve) shows the pulse response of such a system with a single stag CTLE, 1-tap FIR and 1-tap IIR DFE along with the same 2-tap transmitter FFE. As depicted, although similar pre-cursor ISI cancellation is achieved the boost in the main cursor makes the system performance less susceptible to the residual ISI. The resultant bathtub curves of Fig. 4.2(c) and (d) show BER of better than 10^{-12} with timing and voltage margins of better than 0.2UI and 18mV for this BER. In order to achieve similar performance by 1-

tap FIR, 2-tap IIR DFE without engaging CTLE peaking, a 4-tap transmitter side FFE is required which could be prohibitive in terms of power and area considering the PAM4 complexity.

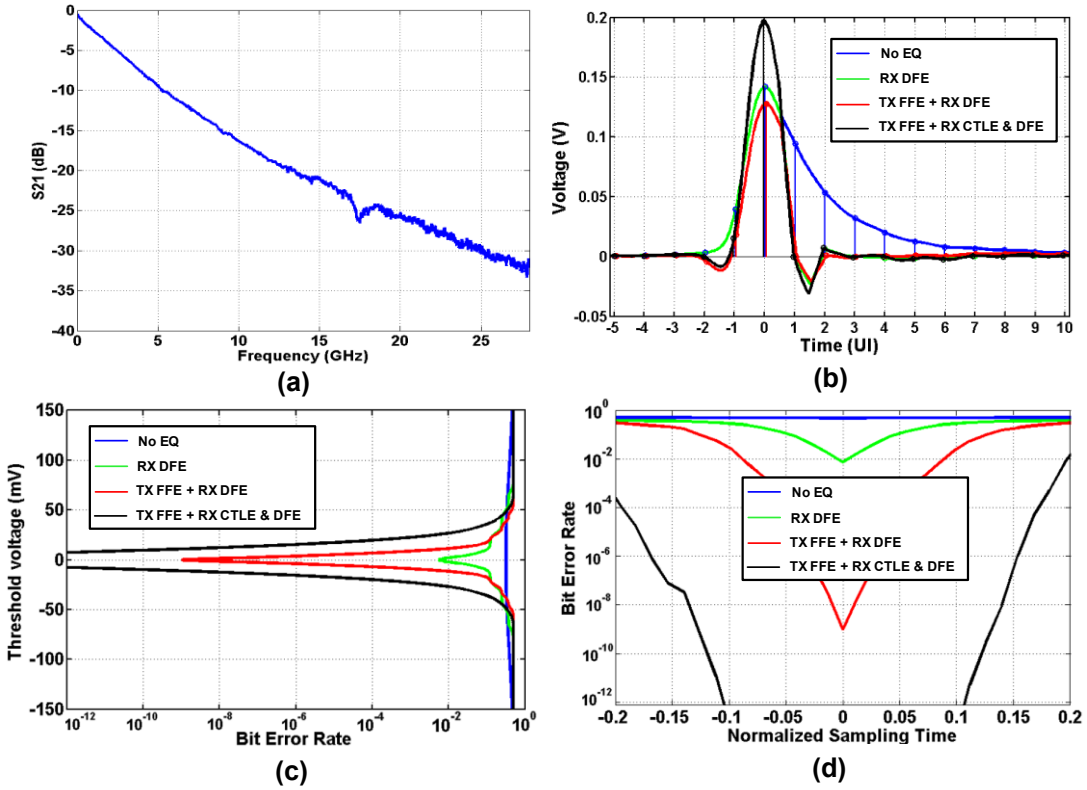


Figure. 4.2: Refined electrical channel. (a) S21 response. (b) 28GS/s pulse responses with various equalizer configurations, (c) 56 Gb/s PAM4 voltage margin, and (d) 56 Gb/s PAM4 timing margin with 2-tap pre-cursor TX FFE and various RX equalizer configurations.

4.3 Receiver Architecture

Based on system analysis of Section 4.2, a PAM4 receiver with a single stage CTLE and a 1-tap FIR, 1-tap IIR DFE is proposed as shown in Fig. 4.3. The CTLE output is connected to the quarter-rate DFE with slices that consists of 5 samplers. Three data samplers implement a 2-bit flash ADC for PAM4 symbol detection, 1 error sampler

periodically scans the top and bottom eyes for threshold tuning, and 1 edge sampler provides information for CDR phase locking and DFE tap adaptation. The outputs of the 4 receiver slices are first deserialized to 1/8 symbol rate, with the data and edge samples driving the CDR's PAM4 BBPD. At this point the data samples are also probed out for external BER testing. All the data, error, and edge samples are then further deserialized to 1/32 symbol rate for processing by the DFE tap and threshold adaptation logic.

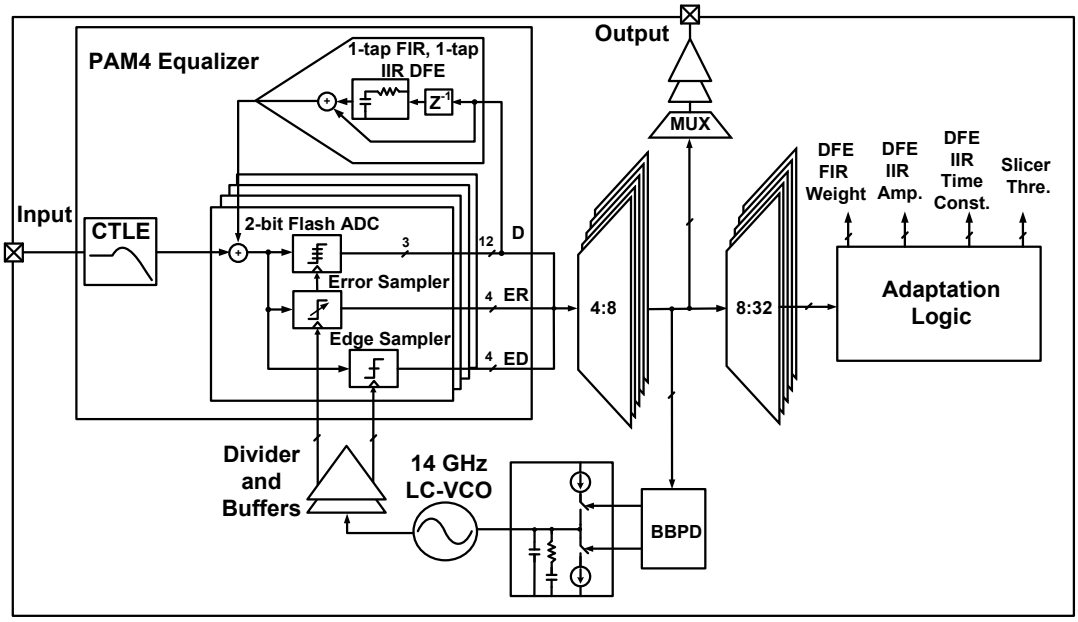


Figure. 4.3: 56Gb/s PAM4 receiver with threshold and DFE tap adaptation.

A detailed block diagram of the equalizer data-path is shown in Fig. 4.4. The quarter-rate architecture reduces the clocking power and relaxes timing of CML slicers by giving them extra time to recover from previous decision in sampling phase. Eight phase clocks are used for data and edge detection. The three data samplers implement a 2-bit flash ADC for PAM4 level detection. The middle data slicer threshold will be set to zero while the

top and bottom slicers' threshold will be set to ±2/3 the post-equalized amplitude of the received signal by the threshold adaptation circuit. The error slicer is used for threshold tuning and its threshold will be set by the adaptation circuit. The edge sampler is used for timing recovery and DFE adaptation with the threshold set to zero. An FIR tap is utilized to cancel the first post-cursor ISI. This multi-level FIR tap is efficiently realized by feeding back the data samplers' 3-bit thermometer-coded output bits directly to three equally weighted summer inputs embedded in data, edge and error comparator to minimize FIR tap critical delay and meet the 1-UI stringent timing. Long-tail ISI is efficiently cancelled with the IIR tap, starting from the second post-cursor. In order to minimize the comparator's internal loading, these IIR tap is subtracted from the input with CML summers that precedes the comparators. The quarter-rate data samplers' outputs are serialized to full-rate and filtered to generate the IIR tap signal.

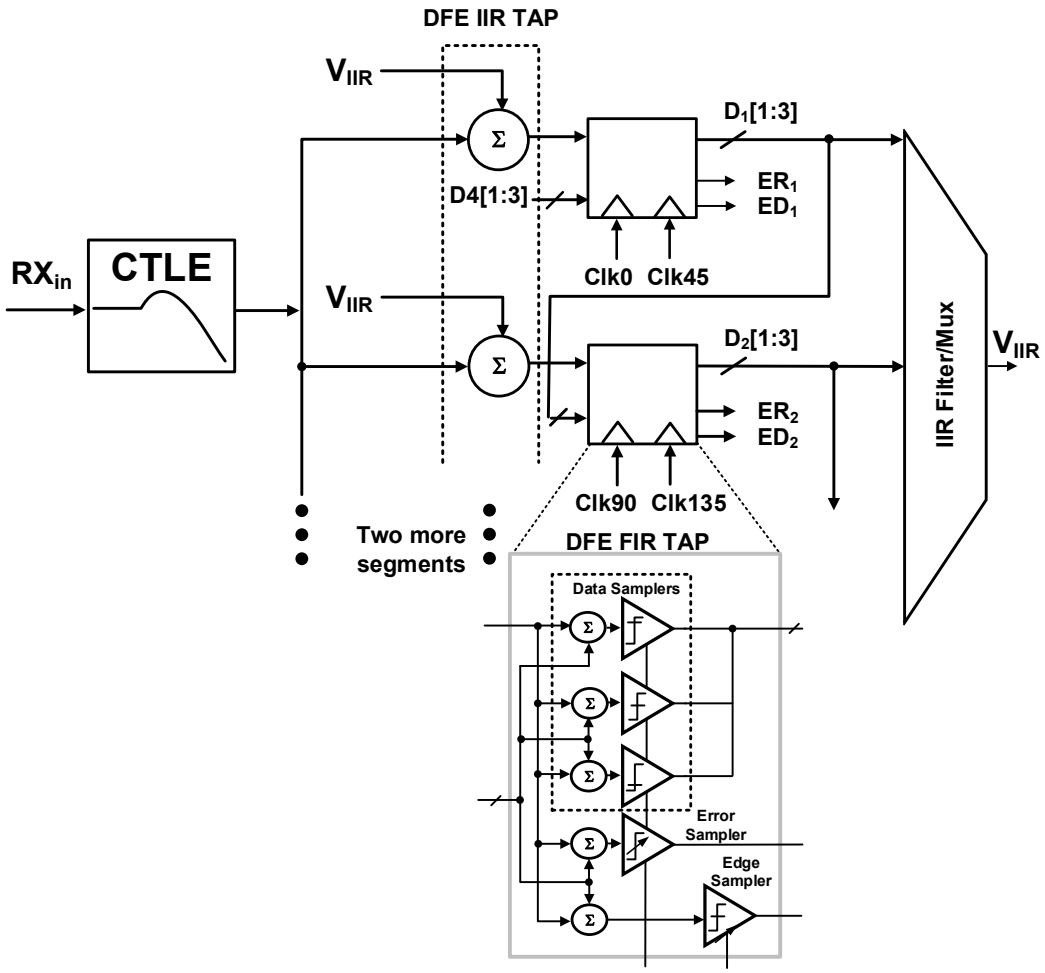


Figure. 4.4: Equalizer data-path.

Fig. 4.5 (a) shows the single-stage CTLE with tunable degeneration resistor and capacitor to tune the high frequency peaking and low frequency gain. The high frequency peaking is set by the capacitor DAC while the low frequency gain is set by the resistor DAC both of which having 3-bit resolution and providing 0 to 6 dB of range as illustrated in frequency response of Fig. 4.5 (b) and (c), respectively, for different settings.

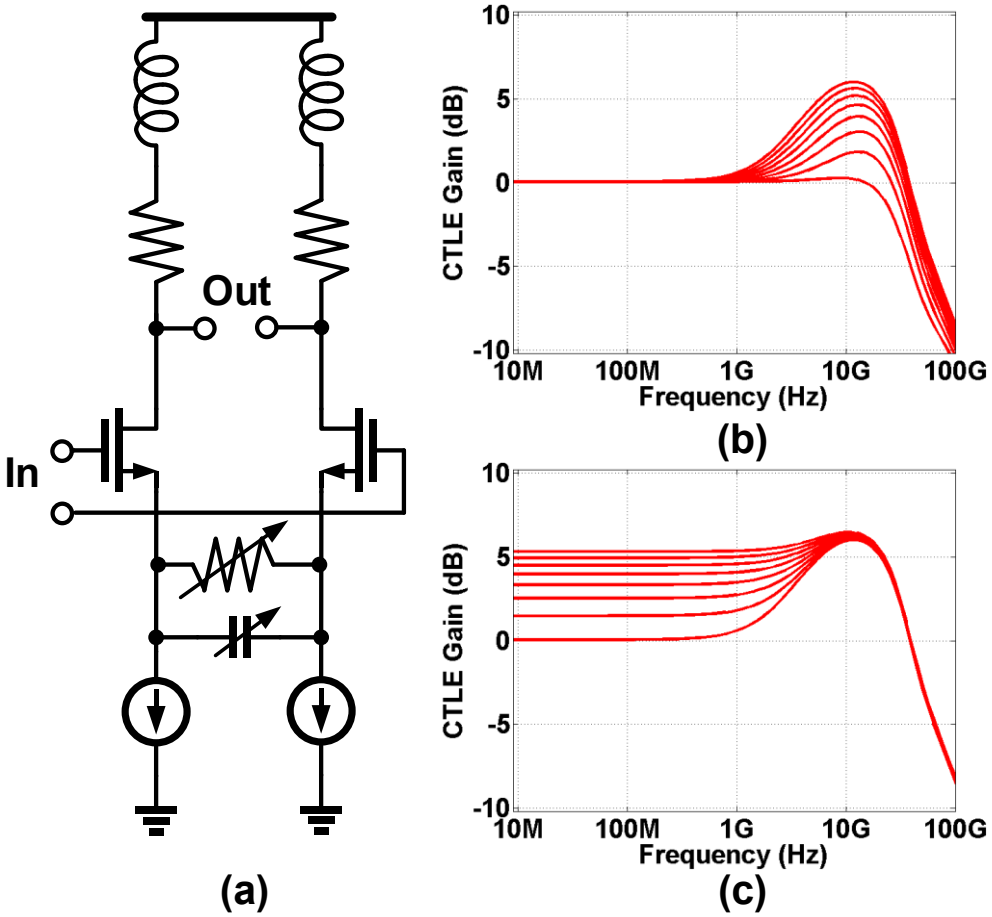
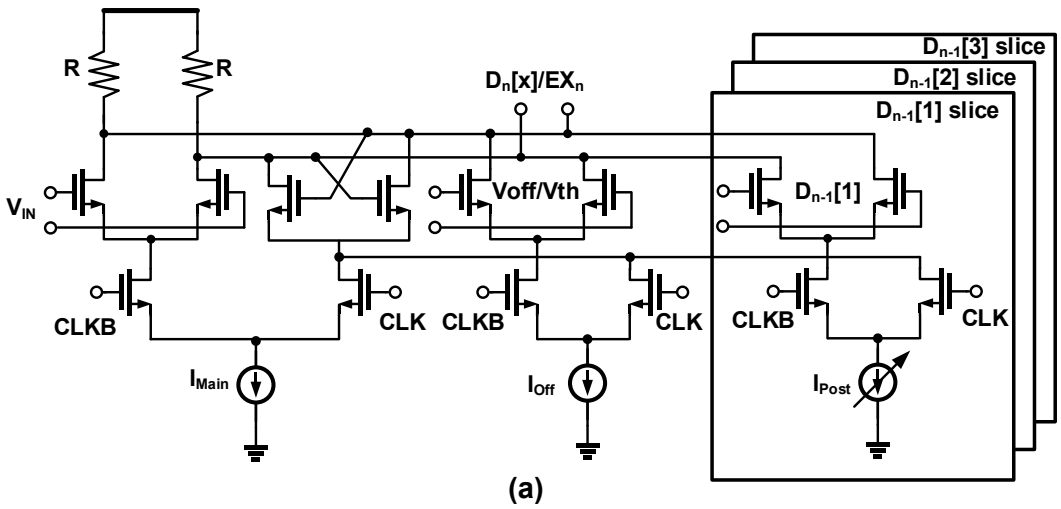


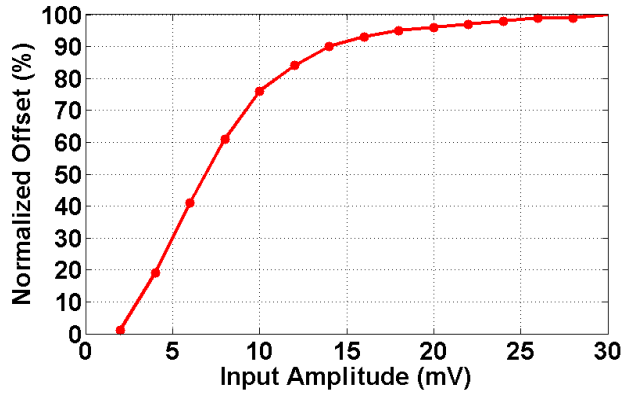
Figure. 4.5: Single stage CTLE (a) block diagram and frequency response with different (b) capacitor DAC settings, and (c) resistor DAC settings.

While strong-arm comparators [76], and modified double-tail versions [73], have advantages that include no dc power, small aperture time, high gain, and CMOS-level outputs, due to their multi-stage implementation, they often suffer from reduced bandwidth and large delay. The single stage CML slicers [58], on the other hand, provide higher bandwidth while suffering from reduced gain and static power consumption. Fig. 4.6 (a) shows the schematic of such slicer with embedded FIR taps and threshold/offset control pairs. In order for the feedback loop to operate as a through DFE, avoiding noise

propagation in the loop, [54] the input data should be sufficiently large to clip the feedback pairs. A differential input amplitude of ~14mV is required to achieve 90% maximum DFE weight at 56Gb/s as depicted in Fig. 4.6 (b). Thus the minimum sensitivity of the DFE loop is equal to 28mVppd. Samplers' threshold and offset is controlled through the DAC-generated Voff/Vth voltage with 7-bit (1-bit sign, 6-bit amplitude) resolution with a maximum range of more than 250mV as illustrated in Fig. 4.7 (a). Independent DFE FIR-tap weights are used to set the tail currents with 6-bit resolution on a per-slice basis to compensate for mismatch between the receiver slices achieving more than 150mV of range as depicted in Fig. 4.7 (b). The single IIR MUX of Fig. 4.8 combines the thermometer quarter-rate data from all the slices and serializes it to full-rate using a current-mode architecture. A tunable RC load filter implements the IIR filter, with the time constant controlled through tunable 3-bit resistor DAC for coarse tuning and tunable 3-bit tunable capacitor DAC for fine tuning. Fig. 4.9 shows how the time constant can be tuned by changing the resistor and capacitor DAC codes. The IIR amplitude is controlled by the tunable tail current. The IIR summation is done in the CML summer as shown in Fig. 4.8. The input pair is degenerated to achieve required linear range to support input signal swing. The gain and linear range of the input pair can be set by the tunable degeneration resistor. As the IIR tap cancelation domain starts from 2nd post cursor, the IIR taps doesn't require degeneration due to smaller amplitude requirements.

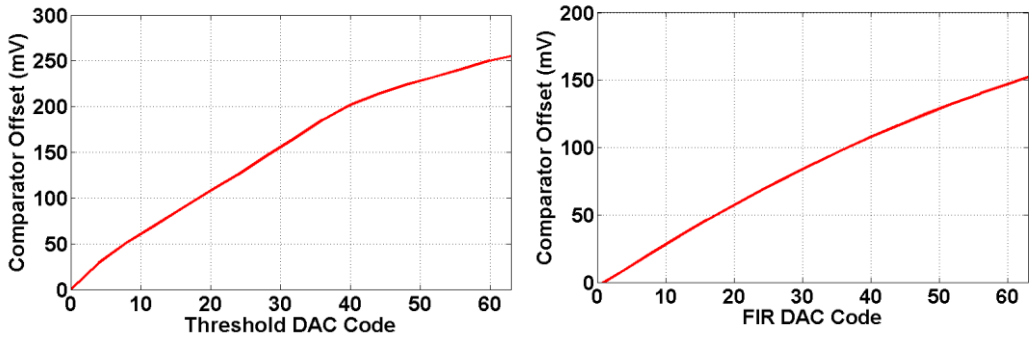


(a)



(b)

Figure. 4.6: (a) CML buffer with DFE FIR-tap and threshold control. (b) Simulated normalized FIR-tap offset weight versus differential input amplitude.



(a) (b)

Figure. 4.7: (a) Simulated comparator offset versus threshold DAC code, (b) simulated FIR weight vs FIR DAC code.

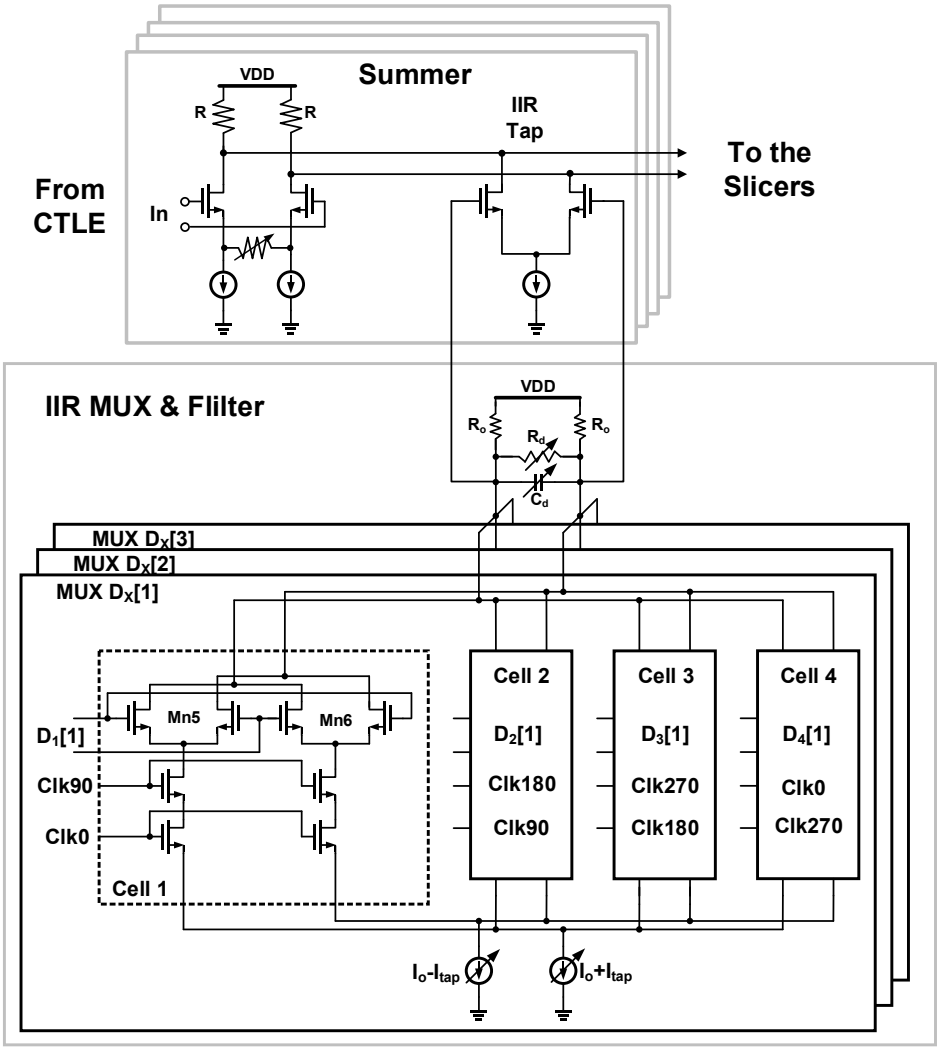


Figure. 4.8: Block diagram of IIR MUX, filter and summer.

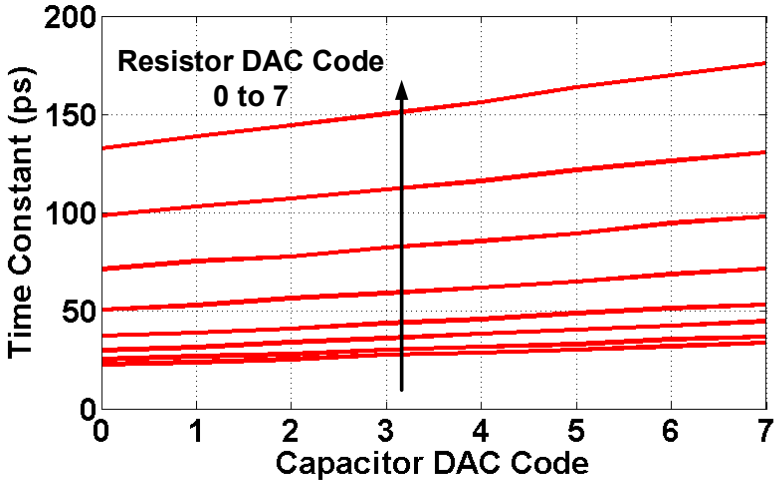


Figure. 4.9: IIR time-constant versus resistor and capacitor DAC settings.

Fig. 4.10 shows the PLL-based CDR block diagram. The BBPD receives the 1/8-rate data and edge samples and filters out all but the symmetric transitions to avoid asymmetric PAM4 transition-induced jitter. In order to reduce loop latency, the BBPD works with 8 parallel Early/Late signals controlling an 8-segment charge pump. This parallel charge pump drives the loop filter to produce the control voltage for a 14GHz LC oscillator [81]. In addition to the primary resonator tank, oscillator phase noise is reduced with tanks also in the source of both cross-coupled transistor pairs [82]. Quarter-rate clocks are generated by a CML divide-by-two and then converted to CMOS level. Static CMOS phase interpolators efficiently generate the 8 clock phases for the quarter-rate data and edge samplers. Per-phase skew calibration is achieved with tunable delay buffers preceding the samplers.

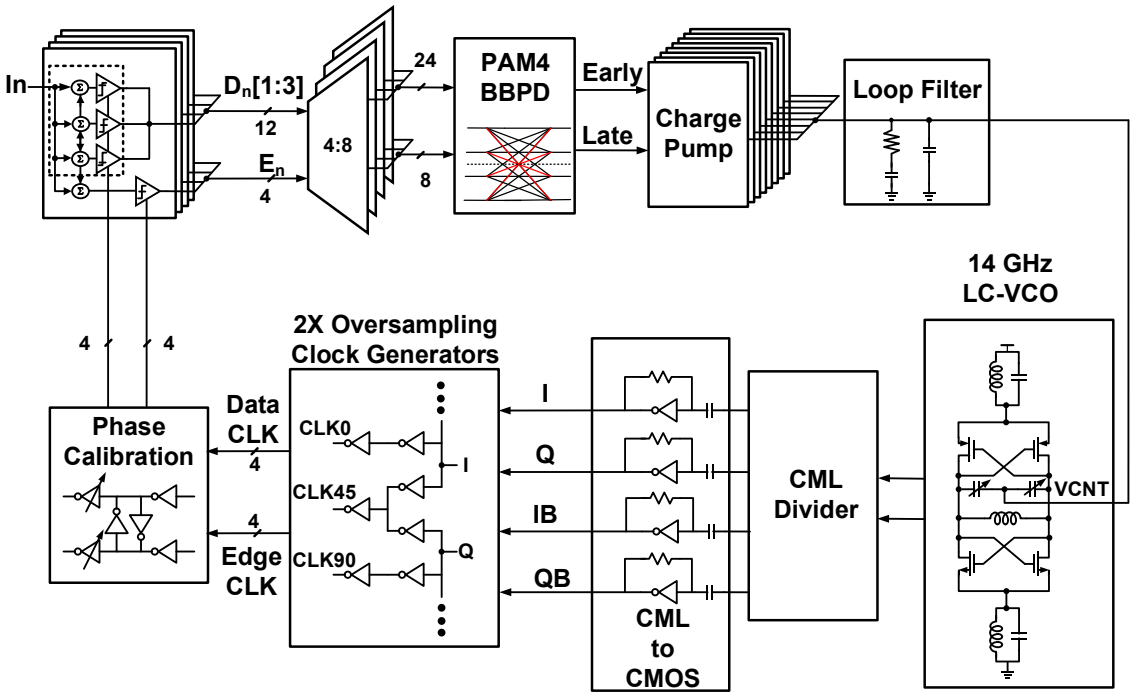


Figure. 4.10: PAM4 PLL-based CDR.

4.4 Threshold and DFE Tap Adaptation

Background sampler threshold adaptation is achieved with an additional error sampler to periodically estimate the top/bottom eye height and place the thresholds in the middle. An initial foreground calibration step is performed where all 20 samplers are set to zero offset/threshold by shorting the input to the common mode and adjusting the per-sampler Voff/Vth DAC codes. On a per-slice basis, the top sampler's threshold (highlighted in green) is then incremented up by 1LSB (error offset 1) to come to the initial condition shown in Fig. 4.11. The initial coarse adaptation steps are based on uniform symbol statistics, with both the top sampler and error thresholds (highlighted by red) increased until a 25% one detection probability is achieved by the error sampler. Also, in parallel

the bottom sampler (highlighted by blue) is stepped at the same rate in an open-loop manner to improve convergence speed. At the end of state 1, the error sampler is residing at the bottom of the top eye and the top sampler is sampling only 1 threshold LSB inside the eye. Next, the polarity of the error sampler threshold is inverted and then fine-tuned to converge to the top of the bottom eye based on 25% zero detection criteria, while the bottom sampler will follow the error sampler by -1 LSB difference (State 2). The independent top and bottom threshold tuning eliminates errors caused by PAM4 asymmetry and level spacing mismatch. In order not to rely on uniform statistics, the process then transitions to monitoring the relative values of the error samplers and the bottom/top samplers to track the eye edges in States 3 and 4. It should be noted that at the end of state 4, the top and bottom slicers are in a sub-optimal position inside the eye. While ideally the top and bottom samplers should be following the error sampler with ± half the eye-height respectively in States 4 and 3, due to lack of eye-height estimation at this point, they are following it with only ± 1 LSB (the minimum possible estimation).

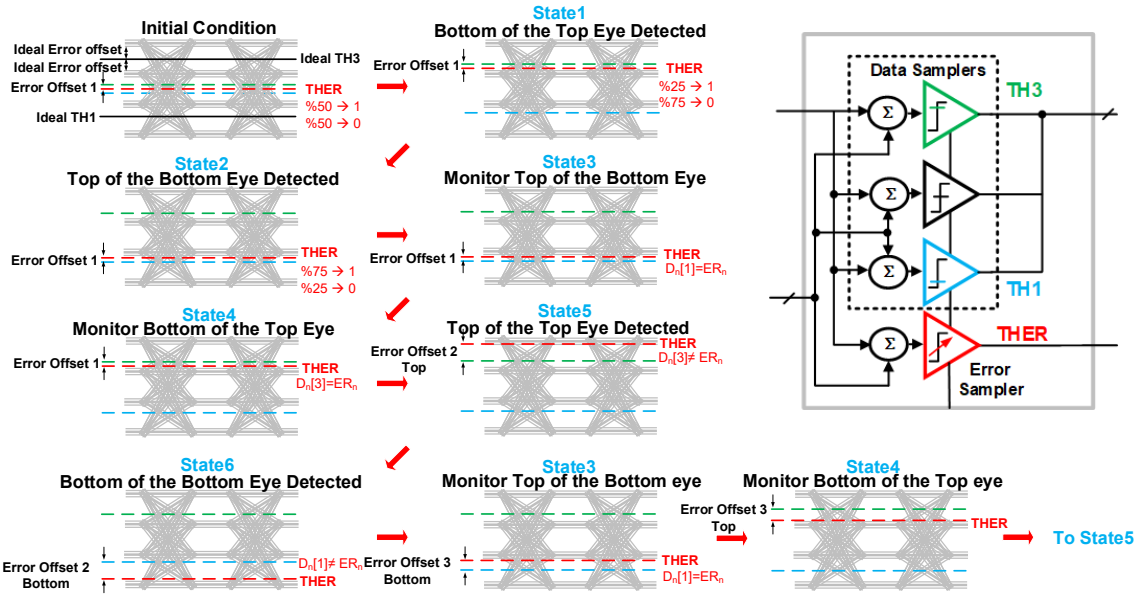


Figure. 4.11: Background sampler threshold adaptation algorithm.

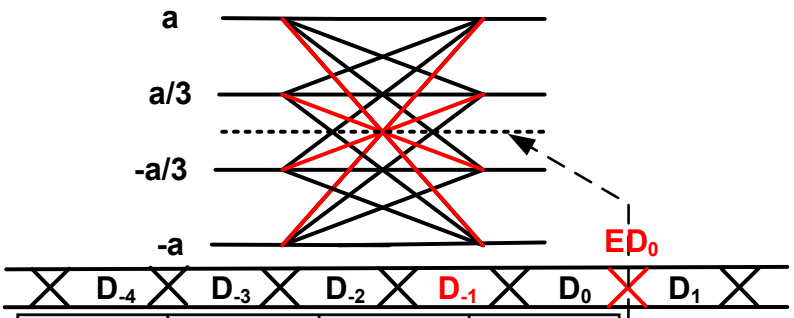
Next, in order to get an estimation of eye-height, the data samplers' thresholds are fixed and the error sampler threshold is increased until discrepancy is detected between error and the top outputs, implying the error sampler has reached the top edge of the top eye (State 5) resulting in threshold code difference of error offset 3 with top sampler. This is repeated to find the bottom of the bottom eye (State 6). At this point, the top and bottom eye heights are found and the eye-height can be estimated precisely for top and bottom eyes independently. The error offset will be updated to be:

$$error\ offset = \frac{error\ offset\ 1 + error\ offset\ 2}{2}. \tag{4.1}$$

Next, the bottom/top thresholds are placed in the middle of the corresponding eye when the process goes back to State 3 and 4 for monitoring of the top of the bottom eye

and bottom of the top eye, respectively. The algorithm then periodically rotates between States 3-6 to track eye-height and optimal threshold position.

The edge-based DFE tap background adaptation logic tables are shown in Fig. 4.12, which is modified from [71] to allow for PAM4 operation and independent per-slice DFE FIR-tap control. Similar to the BBPD logic, the DFE tap adaptation works with symmetric PAM4 data transitions in order to improve convergence. When a symmetric transition is detected, the correlation between the edge sample and the sign of the previous symbols determines the residual ISI polarity from the corresponding symbol. As the DFE FIR-tap cancels the first post-cursor, if the D_{-1} symbol polarity matches the edge sample ISI polarity, this implies that the tap value is too small and the FIR-tap counter is incremented and vice-versa. As PAM4 receivers require improved sensitivity, independent per-slice adaptation is implemented for the DFE FIR-taps to compensate for mismatch in the 4 receiver slices. The DFE IIR-tap amplitude is set in a similar manner utilizing the D_{-2} polarity, as this IIR tap compensates for long-tail ISI after the first post cursor. IIR-tap time constant is set with the correlation from either D_{-3} or D_{-4} and the edge sample. The use of one common DFE IIR-tap mux allows for the adaptation of only a single set of IIR values.



FIR Weight	D_{-1}	ED_0	D_1
INC	a(a/3)	+1	$-D_0$
DEC	-a(-a/3)	+1	$-D_0$
DEC	a(a/3)	-1	$-D_0$
INC	-a(-a/3)	-1	$-D_0$

IIR Amplitude	D_{-2}	ED_0	D_1
INC	a(a/3)	+1	$-D_0$
DEC	-a(-a/3)	+1	$-D_0$
DEC	a(a/3)	-1	$-D_0$
INC	-a(-a/3)	-1	$-D_0$

IIR Time Constant	D_{-4}	D_{-3}	ED_0	D_1
INC	a(a/3)	a(a/3)	+1	$-D_0$
DEC	-a(-a/3)	-a(-a/3)	+1	$-D_0$
DEC	a(a/3)	a(a/3)	-1	$-D_0$
INC	-a(-a/3)	-a(-a/3)	-1	$-D_0$

Figure. 4.12. PAM4 DFE FIR and IIR-tap adaptation logic tables.

4.5 Experimental Results

The PAM4 receiver is fabricated in GP 65nm process, occupying a total active area of 0.51mm2 as shown in chip micrograph of Fig. 4.13. The receiver BER test setup and measured insertion loss of the two test channels' are shown in Fig. 4.14. A PAM4 pattern generator with 1-main and 1-pre-cursor FFE taps generates PRBS15 data which then pass

through channel 1 and channel 2 with 16.1 dB and 20.8 dB of loss at 14GHz respectively. The on-die 1/8 rate data MUX at the receiver output allows for independent verification of the MSB or LSB outputs which are tested using an NRZ pattern checker. In order to measure the timing bathtub curves of the receiver, the CDR is bypassed and receiver is clocked through an external clock. In this mode, the half-rate clock is generated by pattern generator with phase shift capability to capture BER at different sampling times.

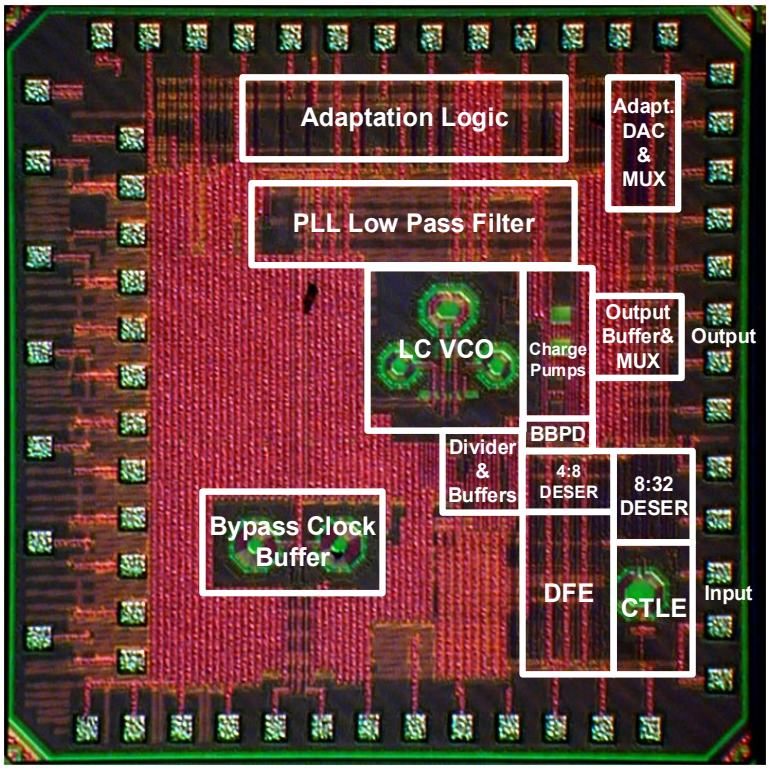


Figure. 4.13: Chip micrograph of 56Gb/s PAM4 receiver.

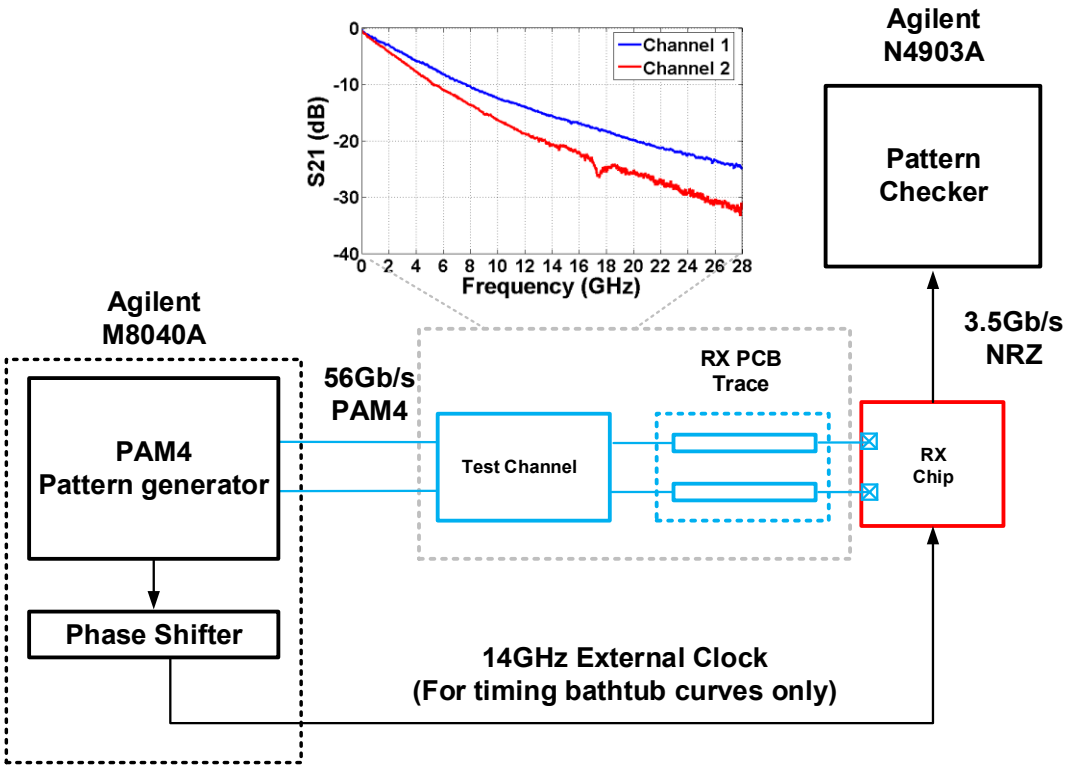


Figure. 4.14: High speed PAM4 receiver test setup.

Fig. 4.15 (a) shows the transmitter PAM4 pre-channel eye diagram without any equalization with 600 mVppd swing. Co-optimizing the 2-tap pre-cursor FFE with the receiver equalization results in a completely closed eye at the output of channel 2 (Fig. 4.15 (b)).

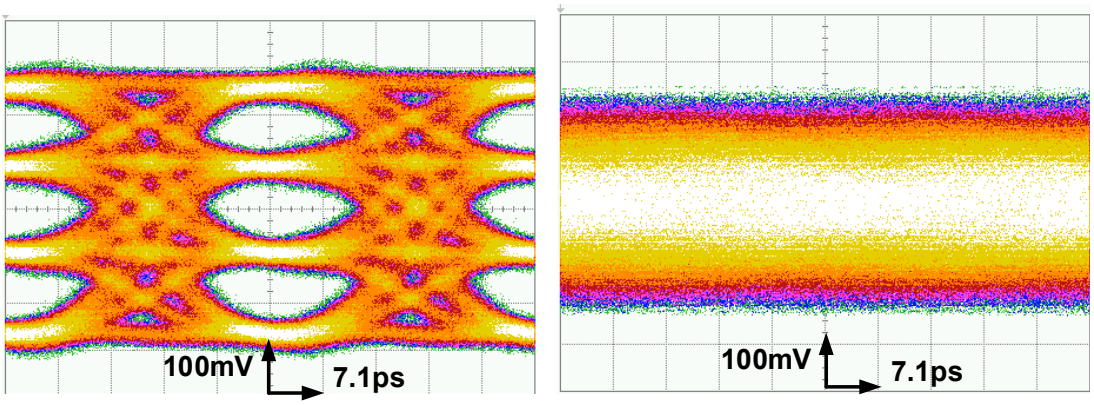


Figure. 4.15: (a) 56 Gb/s eye-diagram before channel 2 without equalization and (b) after channel 2 with 2-tap pre-cursor FFE.

An on-chip DAC monitors DFE tap coefficients and the sampler thresholds convergence. Fig. 4.16 (a) and (b) show the DFE taps convergance for channel 1 and channel 2 respectively. In both cases all taps converge within 2µs. The threshold convergence for channel 1 and channel 2 is illustrated in Fig. 4.16 (c) and (d). The initial threshold procedure completes within 16µs in for both channels. The combined MSB/LSB BER timing bathtub curves of receiver is measured using the bypass CDR mode with 2-tap pre-cursor transmitter FFE and different number of DFE taps enabled as depicted in Fig. 4.17 (a) and (b) for channel 1 and channel 2, respectively. While an optimized combination of CTLE and DFE FIR tap allows BER of better than 10^{-7} for channel 1, due to significant ISI from 2nd post cursor and beyond BER is worse than 10^{-2} for channel 2 using this equalization setting. Adding the IIR DFE tap allows for efficient higher post-cursor cancellation achieving 0.22UI and 0.19UI of timing margin at BER=10^{-12} for channel 1 and channel 2 respectively. The voltage bathtub curves of Fig. 4.17 (c) and (d) are measured with all taps enabled while the CDR is locked and by changing the threshold

code for the top, middle, and bottom samplers from their ideal position. Voltage margins of 23mV and 14mV are achieved at BER=10^{-12} for channel 1 and channel 2 respectively.

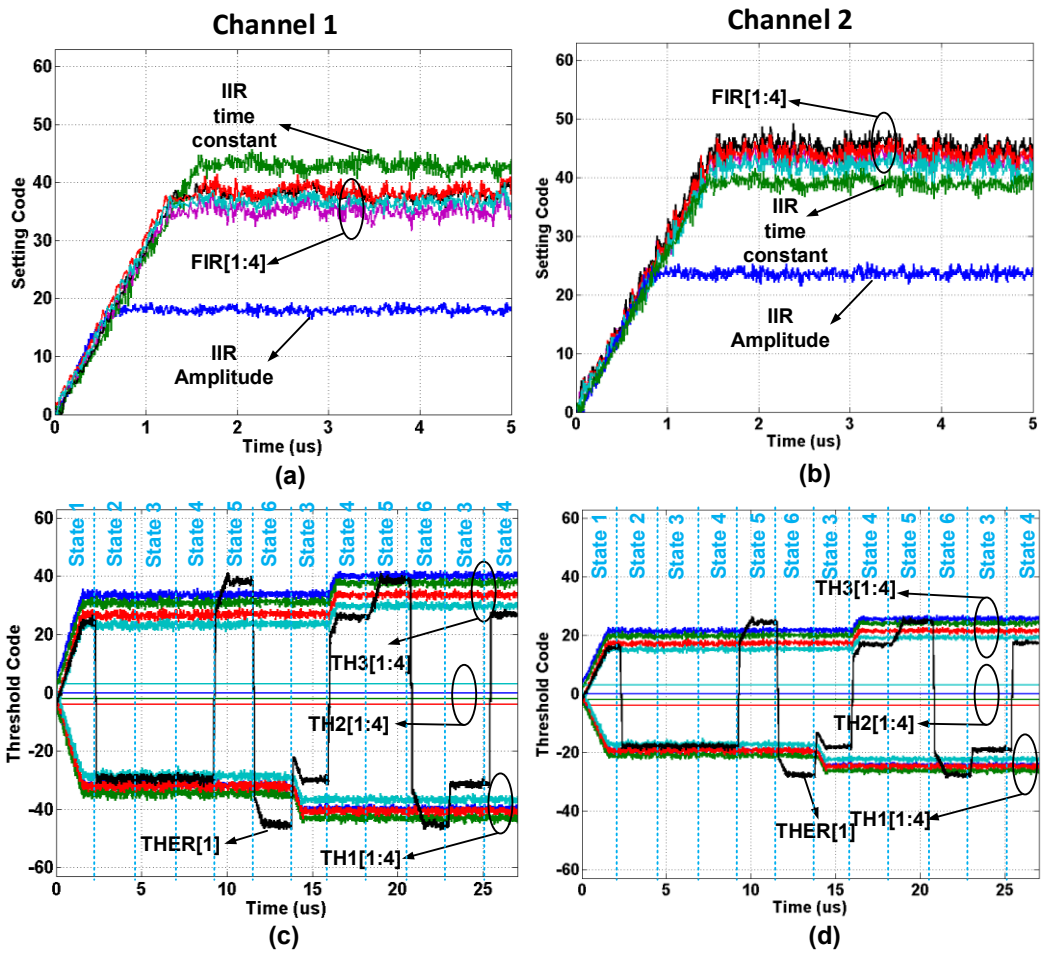


Figure. 4.16: Measured DFE tap adaptation working over (a) channel 1 and (b) channel 2, and measured sampler threshold adaptation working over (c) channel 1 and (d) channel 2. Note, edge sampler values are omitted and only error sampler#1 is shown for clarity.

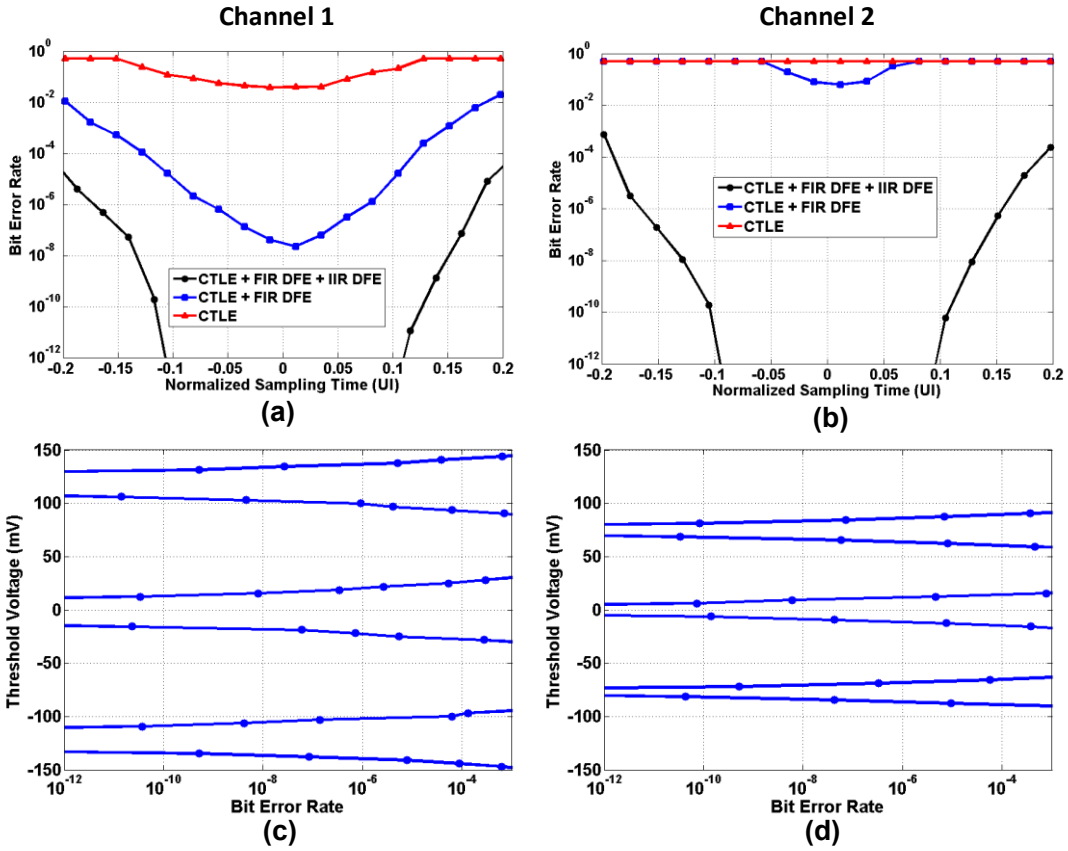


Figure. 4.17: Measured 56Gb/s receiver timing bathtub curves working over (a) channel 1, and (b) channel 2, and receiver voltage bathtub curves working over (c) channel 1, and (d) channel 2.

Fig. 4.18 shows the jitter tolerance of the receiver while working over channel 2 for BER=10^{-9}. CDR shows more than 6 MHz of bandwidth with 0.12UI of high frequency jitter tolerance exceeding CEI-56G-VSR requirements. It should also be noted that CEI-56G-VSR spec only requires a BER=10^{-6}.

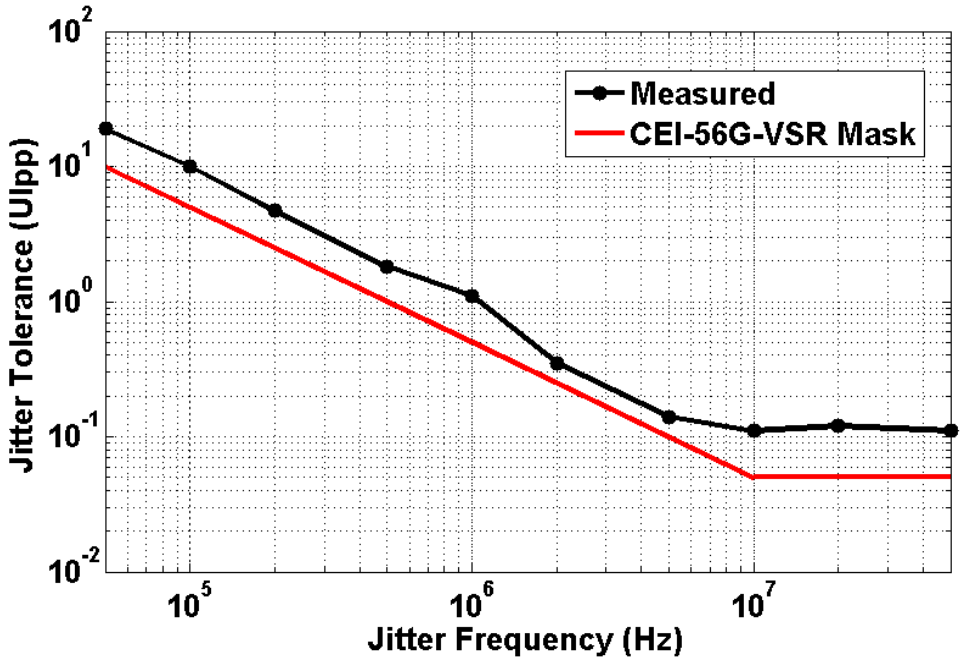


Figure. 4.18: Measured PAM4 jitter tolerance working over channel 2.

Fig. 4.19 shows the 56 Gb/s power breakdown of the receiver. The receiver consumes 259 mW of power, with CML comparators and clocking circuits having the most contribution. Table 4.1 summarizes the receiver performance [83] and compares it with other PAM4 receivers operating near 56Gb/s. The receiver achieves a power efficiency of 4.63mW/Gb/s, which is superior to the ADC-based design of [77] and the mixed-signal front-end of [79] which utilizes a 2-stage CTLE and an additional TX FFE tap. Employing the DFE IIR-tap allows for a reduction in the total tap count relative to [78], while also extending the maximum supported channel loss.

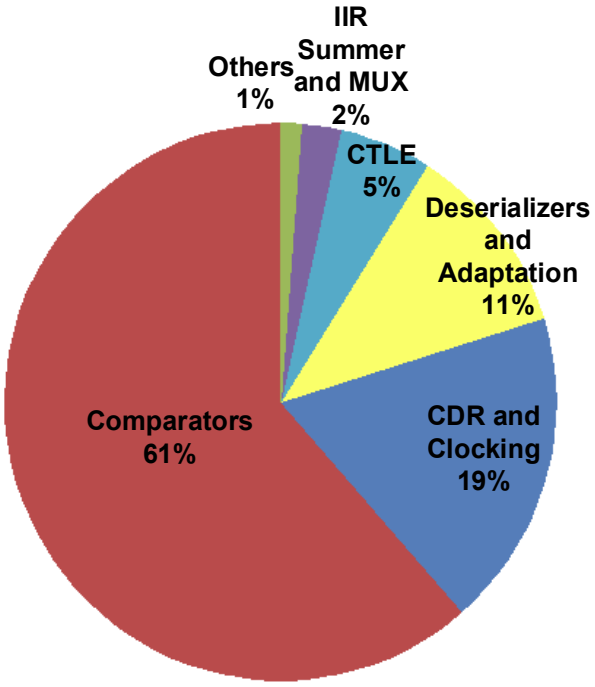


Figure. 4.19: 56Gb/s power breakdown of the receiver.

Table 4.1: Performance Summary

References	[77]	[78]	[79]	This Work
Technology	CMOS 16nm FinFET	CMOS 16nm FinFET	40nm CMOS	65nm CMOS
Data-Rate	56Gb/s	40-56Gb/s	56Gb/s	56Gb/s
Data Format	PAM4	PAM4	PAM4	PAM4
Equalization	CTLE ADC based DFE & FFE	CTLE 10-tap DFE	CTLE 3-tap DFE	CTLE 1-tap FIR & 1-tap IIR DFE
Maximum CTLE Peaking	2-stage 14dB	2-stage 16 dB	2-stage 9 dB	1-Stage 6 dB
Channel-Loss	31dB[1]	10dB[2]	24dB[1]	20.8dB[2]
Area	2.8mm^2 (2 TX/RX)	0.364mm^2	1.26mm^2	0.51mm^2
Supply	0.9V/1.2V/1.8V (digital/analog/aux)	0.9V/1.2V/1.8V (digital/analog/aux)	1V	1.2V
Power Consumption	370mW (RX excl. DSP)	230mW	382mW	259mW
Power Efficiency	6.6mW/Gb/s	4.1mW/Gb/s	6.82mW/Gb/s	4.63mW/Gb/s

[1] Including 3-tap TX FFE equalization
[2] Including 2-tap TX FFE equalization

4.6 Conclusion

Section 4 presented a 56Gb/s PAM4 quarter-rate receiver which employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-taps. In addition to main three samplers for PAM4 data detection, one edge sampler per slice is utilized for PLL based CDR phase detection and DFE tap adaptation with independent per-slice values for required PAM4 sensitivity, and one error sampler is utilized that periodically scans the top and bottom of the PAM4 eyes. Overall, the proposed PAM4 receiver architecture enables transmission over channels with up to 20dB of loss at Nyquist requiring only a 2-tap pre-cursor transmitter side FFE while improving the power efficiency compared to state-of-the-art receivers operating at similar data-rates over channels with comparable channel loss.

5. CONCLUSION

Mixed signal transceivers can provide low power solutions compared to ADC based counterparts. However, additional complexities associated with PAM4 modulation including linearity, sensitivity, and multi-level ISI cancellation issues can results in significant reduction in transceiver power efficiency. This requires serious consideration of different aspects of system level and circuit level design. This dissertation proposes design techniques for power efficient >32Gb/s mixed signal transceivers. One PAM4 transmitter and one receiver prototype have been designed, fabricated as a part of this research.

The first prototype includes a dual-mode NRZ/PAM4 serial I/O transmitter achieving 16Gb/s NRZ and 32Gb/s PAM4 operation at 10.4 and 4.9 mW/Gb/s while operating over channels with 27.6 and 13.5dB loss at Nyquist, respectively. The source-series-terminated (SST) transmitter utilizes lookup table (LUT) based digital-to-analog converter (DAC) to implement 4/2-tap feed-forward equalization (FFE) in NRZ/PAM4 modes, respectively. A low-overhead analog impedance control is proposed along with a quarter-rate serializer based on a tri-state inverter-based mux with dynamic pre-driver gates. The transmitter is fabricated in GP 65-nm CMOS, the transmitter occupies 0.060mm2 area.

The second prototype presents a 56Gb/s four-level pulse amplitude modulation (PAM4) quarter-rate wireline receiver achieving 4.63 mW/Gb/s power efficiency while operating over a channel with 20.8dB, implemented in a 65nm CMOS process. The proposed receiver utilizes a single stage continuous time linear equalizer (CTLE) along with a 2-tap decision feedback equalizer (DFE) with one finite impulse response (FIR) tap and one

infinite impulse response (IIR) taps. The FIR tap direct feedback is implemented inside the CML slicers to relax the critical timing of DFE and maximize the achievable data-rate. The prototype utilize only one error sampler and one edge sampler in addition to 3 main samplers to implement PLL-based CDR phase detection, threshold adaptation and DFE tap adaptation. A novel threshold adaptation is employed in this design, while the edge based adaptation of [71] is extended for PAM4 modulation.

Leveraging the proposed architectures and design techniques, PAM4 transceivers can be implemented to compensate for more than 20dB of channel loss, while achieving low power efficiency.

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