WIDE-DYNAMIC RANGE IMAGE SENSOR PROTOTYPE BASED ON DIGITAL READOUT INTEGRATED CIRCUIT

A Thesis

by

ROBIN GUPTA

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Chair of Committee,	Samuel Palermo
Co-Chair of Committee,	Sebastian Hoyos
Committee Members,	Roozbeh Jafari
	Laszlo Kish
Head of Department,	Miroslav M. Begovic

December 2017

Major Subject: Electrical Engineering

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ABSTRACT

Emerging infrared and visible imaging applications require higher sensitivity, larger pixel array, larger contrast ratio (dynamic range), very low power consumption and faster data readout rate operations all at the same time. Some of these applications are camera surveillance used both in day/night (very bright and dark conditions), medical diagnostics, weather forecasting, and aerial search & rescue operations etc. The digital-pixel focal plane array (DFPA) implemented in this thesis has the capabilities to capture a wide dynamic range of more than 120dB in a single global shutter without saturating the pixels at a huge frame rate of more than 500Hz. An adaptive Integration Window technique has been developed which ensures that we are able to measure such a huge dynamic range using a counter of only 10 bits (this helps us lower the power consumption of the design). This proposed image sensor has been designed, fabricated and tested in 65nm CMOS technology. It has 16 x 16-pixel array with 16 x 9 pixels with an inbuilt Silicon APD for optical testing and 16 x 7 dummy pixels for electrical testing. Our design proposes an off-chip digital calibration technique to cut down the burden on the analog circuitry. The sensor design achieved more than 128dB+ of dynamic range with a DNL/INL of 0.65/1.65 respectively with a power consumption of only 0.58 uW/pixel. The digital calibration scheme successfully cuts down the pixel-pixel variation standard deviations by a factor of 4. The proposed image sensor design should be able to address most of the short-comings of conventional FPAs and provides a one-shot solution to the design of high performance CMOS image sensors.

DEDICATION

To my beloved family

ACKNOWLEDGEMENTS

I am enormously grateful for the people who have helped me accomplish the work presented in this thesis. I thank my advisor, Dr. Samuel Palermo, for his knowledge, advice, and support throughout my studies at Texas A&M University.

I would like to thank my committee members, Dr. Sebastian Hoyos, Dr. Laszlo Kish, and Dr. Roozbeh Jafari for their guidance and support throughout the course of the research.

Thanks also go to my friends and colleagues and the department faculty and staff for making my time at Texas A&M University a great experience.

Finally, thanks to my mother and father for their encouragement, patience and love.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a thesis (or) dissertation committee consisting of Professors Samuel Palermo, Sebastian Hoyos and Laszlo Kish of the Department of Electrical & Computer Engineering and Professor Roozbeh Jafari of the Department of Biomedical Engineering.

All other work conducted for the thesis (or) dissertation was completed by the student independently.

Funding Sources

There are no outside funding contributions to acknowledge related to the research and compilation of this document.

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1. INTRODUCTION

Electrical-optical photo-detectors helps us in measuring or sensing the radiation reflected by the respective objects if falling in the detector's spatial observation view. Detectors operating passively, work without any object illumination by the imaging solution, they rely solely on the objects self-luminance or the reflection-transmission of light present in the environment. Whereas in active systems, the scene is irradiated (as in the flash of a camera) with the radiation of interest and then the information is captured [1]. Imaging is done using a 2-D array of photo-detectors which are placed in a grid like format to capture the spatial variation of the incident light intensity. These are placed at the focus point of the optical lens system. The incident optical light falling on the photo-diode get converted to photo-current which is directly corelated with incident light's intensity. Post detection, the read-out circuit (ROIC) captures the incoming current where it is processed, and is sent over a serial link, and/or stored locally or in a remote location [1]. ROIC and the detector array are the focus of our thesis work where the ever-growing emerging trends in sensing applications demand large contrast ratio, large sensitivity, larger pixel array, low power consumption, and a faster read-out.

1.1 SPECTRAL RANGES

Over the time, many indices have been employed to designate each of the spectral region. There has been significant overlap between the regions and the transitions are not sharply well defined. Electromagnetic sensors cover the entire region of electromagnetic spectrum starting all the way from 200nm till 20um and even beyond.

Table 1.1 [1] lists the definition of different spectral regions along with the physical significance of each spectral region. Figure 1.1 shows graphically of how exactly the electromagnetic spectrum is divided into different spectral regions.

Table 1-1: Definition of Spectral Regions [1]

Region	Wavelength Band (um)	Physical Significance
Solar Bind Ultra-violet	0.21 – 0.27	
Ultra-violet	0.27-0.41	Atmospheric transparency
Visible Region	0.405-0.75	Maxima of Solar region
NIR	0.68-1.1	silicon detectors Cut-off.
Short-wave Infrared	1.0-2.8	
MWIR	2.7-6.3	
LWIR	6.1-15.2	
VLWIR	15.0-20.5	

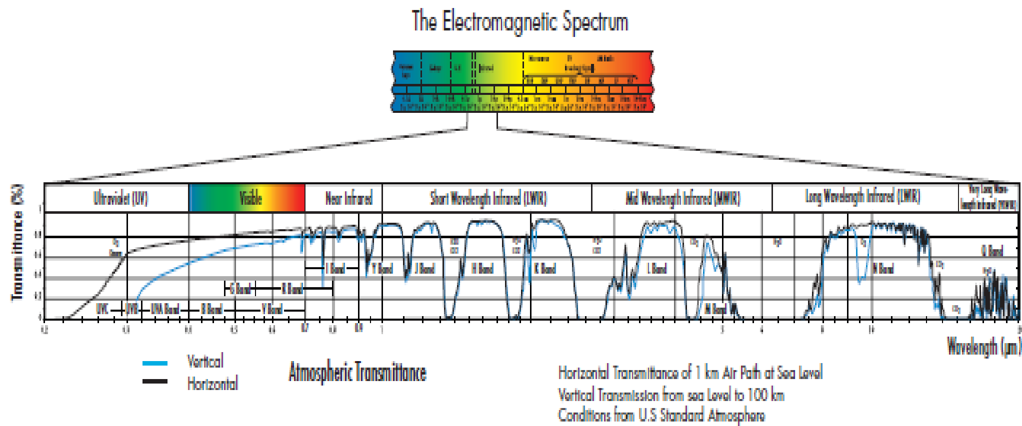


Figure 1-1: Display of spectral bands & wavelength distribution. Reprinted from [1]

1.2 INFRARED SPECTRUM

Infrared (IR) portion of electromagnetic radiation is invisible to the human eye. It's spectral content spreads all the way from the visible region on one side and radio waves on the other. Its wavelength extends all the way from 700nm till 1mm (the

boundary of the visible spectrum to radio waves) which equates to a huge frequency range spanning all the way from 300GHz to 400 THz. Figure 1.2 details the spread of infrared radiation [3].

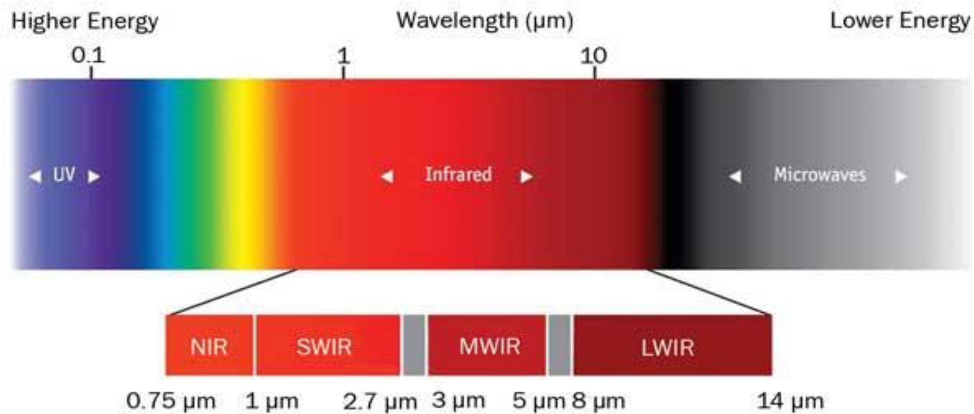


Figure 1-2: Infrared Spectrum region. Reprinted from [3]

The infrared electromagnetic radiation spectrum is further cut-down to near-wave infrared (NIR), mid-wave infrared (MWIR), long-wave infrared (LWIR) and far-wave IR. Every spectral region carries its own properties. Near infrared is closer to the ambient light (visible spectrum) whereas far infrared is far from that [3].

Today, Infrared imaging is an emerging area of interest due to their abundant applications in all the fields which range anywhere from diagnosis of a medical situation, surveillance to assistance in patrolling the borders, search and rescue, to military applications etc. [4]. For example, these can assist in various scenarios such as rescue operations during a disaster by providing read time camera feed, night vision goggles for patrolling the borders looking for enemies, forecasting the weather, diagnosing a medical problem, and also consumer applications like mobile phone for

face recognition etc. [4] Section 1.3 details about some of the applications for the Infrared Imaging.

1.3 APPLICATIONS OF INFRARED IMAGING

Safety and Law Enforcement: It helps in seeing the hidden thief's or track someone escaping a crime area. The infrared cameras are very widely used in Military and defense area in a range of applications starting from aerial drones, border patrol and security etc. Please see the example in figure 1.3 [4]

Night Vision: They are an excellent tool for night vision imaging. They detect things even in the absence of illumination and can capture image even when there is no illumination at all (during very dark nights) and can even see through smoke, foggy or rainy weather conditions. These are used in the surveillance networks, and also assisting in aircrafts during the night. Please see the example in figure 1.4 [4]

Figure 1-3: Infrared Image capture of an area, where a thief is hiding behind the car and also during a disaster rescuing. Reprinted from [4]

Figure 1-4: Military and Border Patrol Surveillance. Reprinted from [4]

Weather Forecasting, Medicine and Building Diagnostics: Satellite mounted with the Infrared Cameras helps in predicting the weather patterns on earth, and distinguish between changing seasons, rain, heat waves etc. Similarly, it also has huge applications in the field of Medicine and Building Diagnostics [8]. See figure 1-5 for the same.

1.4 TYPES OF INFRARED DETECTORS

Thermal Detectors: In thermal detectors, absorbing of the photon leads to a certain variation in the detector's temperature, which can be sensed by a device whose property changes with change in temperature such as a temp. dependent resistor whose value changes with temperature. They are quite advantageous as their frequency response is pretty broadband in nature; but a bigger disadvantage is that it is very challenging to make a material that has quantifiable variation in the temperature for very low strength signals. But we can have larger capturing time for detecting weaker signals, at cost of higher response time [5] [1].

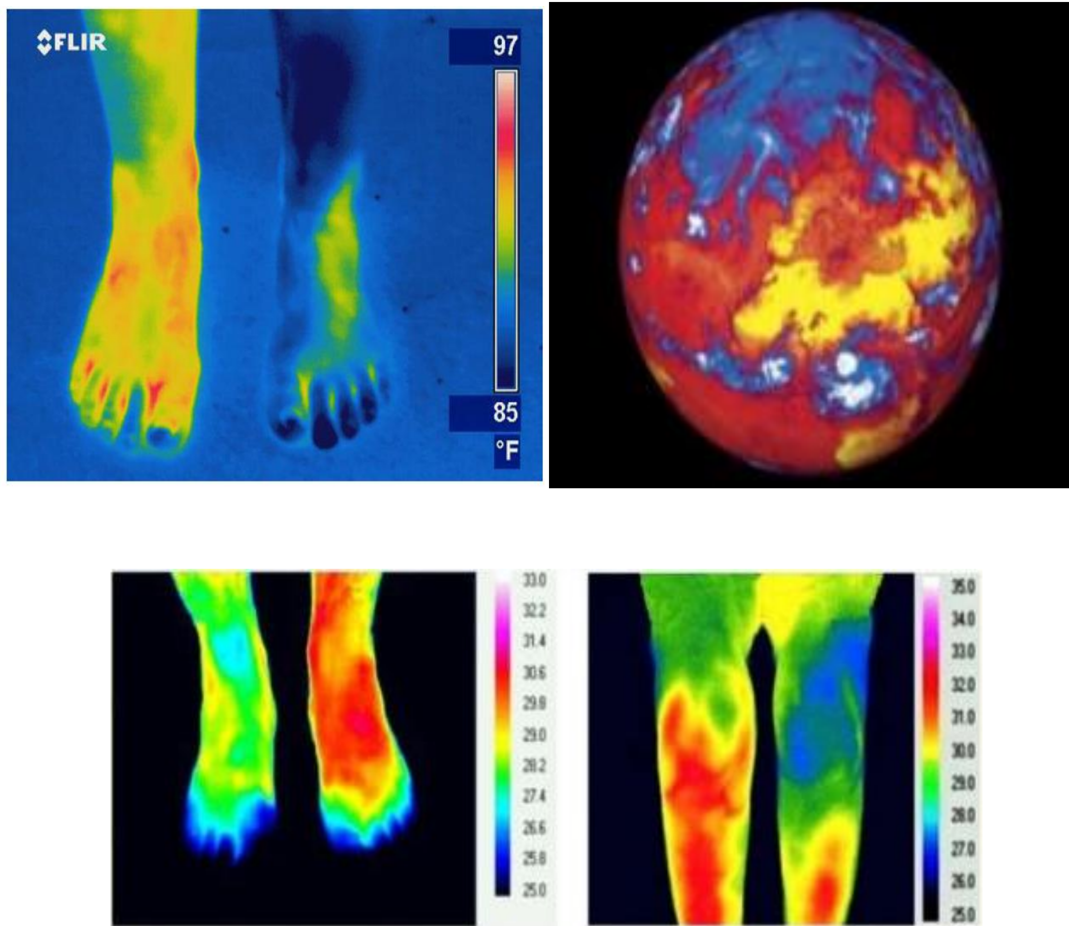


Figure 1-5: Blood Circulation flow in the leg, Infrared image of the Sahara Desert, Inflammation in the leg. Reprinted from [4]

Photon Detectors: Quantum or photon detectors, are typically the semiconductor devices with the band gap of the material very near to the incident optical energy. Absorption of light usually lead to the generation of electron and hole in pairs. There are three different categories of photon detectors namely photovoltaic, photo-conductive and photo-emissive [6][7].

Photovoltaic Photon Detectors: This is designed with a junction fabricated in a semiconductor material. A region where it’s the electrons which are conducting and a

region where conductivity is because of the holes (called p-n junction). As the light falls on the photo-detectors, its either the current or voltage signal produced. [6][7]

Photovoltaic Photon Detectors: In these detectors, the incoming photons changes the electrical conductivity of the detector. As the light intensity falling on the detector changes so does its conductivity. The material often produces currents corresponding to the incident light. These are also designed using silicon based material. [6][7]

Photo-emissive: In these detectors, free electrons are generated upon the reception of the incident light. They are based on the photo-electric effect. The free electrons can then be captured by the readout electronic circuits. [6]

Our work in this thesis will rely upon the photo-emissive based photo-detectors for the optical sensing. We will cover this in more details in sections 2 and section 3 of the thesis.

1.5 SCHEMATIC REPRESENTATION OF THE TYPICAL INFRARED IMAGING SYSTEM

Figure 1.6 presents the schematic of the generic infrared imaging system having an infrared light emitting source on the left followed by a transmitting medium which is usually air (atmosphere) in most of our use cases. This is followed by a system of lens (optical system) to focus the incoming light on the detector array. It is followed by the read-out Integrated Circuits which digitizes the incoming electrical signal from the detector array and transmits it to further downstream devices for further processing, display or storage [1]. Figure 1.7 is the block diagram of each component. Our thesis focusses on the implementation of the detector array and the read-out integrated circuits.

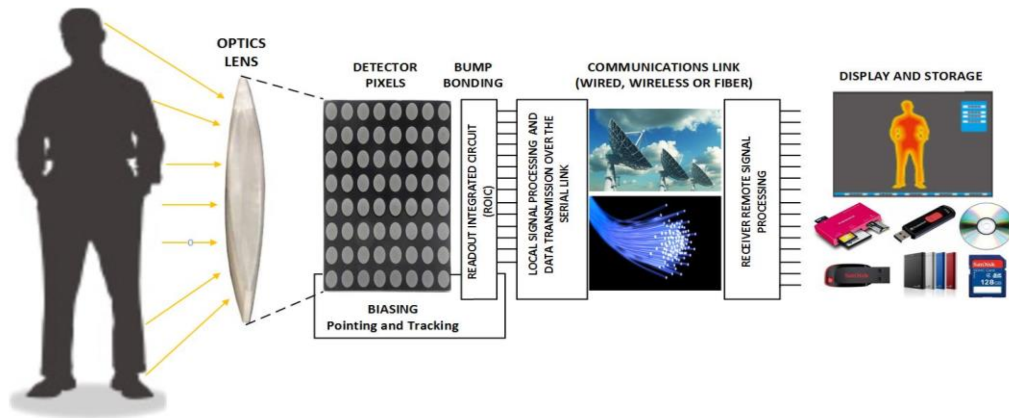


Figure 1-6: Schematic representation of a typical Infrared Imaging system

Figure 1-7: Block diagram of a typical Infrared Imaging system

1.6 FOCAL PLANE ARRAY

A focal plane array is an image capturing unit where individual photo-detectors (each element) are placed in an array like structure. Detector arrays are usually referred as pixel arrays. Focal plane arrays (FPA) are used mainly for imaging purposes but are not limited to them. They are also used for non-imaging purposes like spectrometry, LiDAR etc. In the infrared imaging systems, FPA refers to the element which converts the incoming infrared light into the electrical charges. The method of designing a pixel array is way more difficult as to design an individual element [1]. For infrared detectors, as the detecting element can't be fabricated in silicon (this is usually a different substrate material, a common material is InGaAs), the focal plane array need to be designed

separately from the read out integrated circuit and then bonded together. Each detector element (pixel) is bonded to a silicon based circuit with the help of bumps made using indium [1]. We will discuss more about the focal plane array design for infrared detectors in section 2.

1.7 READ OUT INTEGRATED CIRCUIT

The readout circuit is a silicon based cell whose main function is convert the incoming photo-diode current to respective analog value which can be digitized and further processed. The readout cell is a medium to connect the detector array and digital signal processing unit. The photo detector current produced by the IR detector is digitized in the readout integrated circuit using a unit cell on a per pixel basis.

1.8 ORGANIZATION OF THESIS

In this thesis we are proposing an infrared image sensor prototype based upon the digital focal plane array which can accomplish the wide dynamic range while still consuming as little power as possible. The thesis is divided into seven sections, the first one been the introduction. Below is the description of each chapter in detail.

In chapter 2, we discuss an overview and background of the infrared image sensor. We initiate the chapter by discussing the different methods of designing the infrared detector arrays (like detector materials, material absorption length) and route that we have taken as part of this prototype design. Post description of the detector arrays, we concentrate on the readout integrated circuits. We provide a literature survey of the present-day methods of designing the front end of the image sensors, different

specification using which the performance of the readout integrated circuits can be characterized and the different ADC designs for converting the incoming photocurrent into the digital code. After explaining in detail, the design constraints on the readout integrated circuits, we introduce the concept of dynamic range in image sensor and how it is measured. We also mention some of the techniques that have been used in the past to increase the imaging sensors dynamic range.

In chapter 3, we describe in detail the design of photo-diode which has been implemented as part of the optical testing in the prototype build in the thesis. In the start, we describe the different performance metrics through which photo-diodes are characterized (quantum efficiency, bandwidth, dark current etc.) and the physics behind the working operation of the photo-didoes. Then, we introduce different types of photo-diodes which can be designed in CMOS process which were feasible for our design (N-well / p-substrate, N+/ p- substrate, P+/N-well/p-substrate, T-well/N-well/p-substrate). We mention the photo-diode design approach that we have taken in this work and the layout techniques used for the photo-diode. In the end of the chapter, we table the different layers that were used in the photo-diode layout and the step by step guide of how the photo-diode has been laid out.

In chapter 4, we introduce the circuit and system level specifications of the targeted image sensor and then describe the readout integrated circuit that we have designed in the prototype and explain in detail the working operation of the used techniques. After this we introduce the method of dynamic integration time control where the integration window is automatically adjusted based upon the incident light

intensity. We demonstrate how the integration time control techniques helps us reduce the counter size and thereby the power consumption. Next, we introduce the digital calibration scheme and showcase how it assist in cutting down the fixed pattern noise.

In chapter 5, we describe in detail the design of each block of the proposed image sensor. We commence by showing a top level architectural block diagram of the sensor with all the critical blocks (pixel arrays, timing and control block, scan chain, biasing circuitry, FPGA readout block etc.). There are total 256 pixels broken down into 16 rows of 16 pixels each. Out of the 256 pixels, there are 16 x 7 showing the electrical performance of the chip whereas the rest of them have an APD inside for showing the optical performance. Each Pixel cell has a Pixel ADC which contains the photo-diode (PD), calibration current source for digital calibration, photo-diode biasing circuitry, comparator, and fixed pulse and reset control, 10-bit counter cum shift register, timing and control signal buffers, dynamic integration control circuitry etc. After describing the pixel ADC from top level and its operation, each component of the ADC is discussed in detail one after the other along with their respective explanation. Post the pixel ADC, the other blocks in the chip are discussed in detailed and their corresponding operation.

In chapter 6, we show the micrograph of the proposed image sensor chip. We describe in detail the packaging, bonding and assembling procedure of the chip. After that we provide a description of the lab setup that has been used for testing of the chip which includes bias board, scan chain programmer through lab-view, ML604 FPGA board programming and data capturing through chip-scope. Then, we show the different metrics tested on the chip and the corresponding procedures. Firstly, we tested the

dynamic range performance of the sensor using the in-built test pixels with a given frame and readout rate. Then we showcase the performance of the digital calibration scheme implemented in the design and how it reduces the fixed pattern noise in the pixel array. We also capture how the scheme works over all the 1023 codes. Then, we show the linearity performance of the pixel in terms of linearity plot across all the codes and, also DNL/INL. Lastly, we show a performance comparison table against the infrared references available on internet.

In section 7, a summary of the work is given, conclusions are made and the nature and scope of future work in this thesis is discussed.

2. OVERVIEW AND BACKGROUND OF THE INFRARED SENSOR

2.1 DETECTOR ARRAY

The first and one of the most critical blocks in the complete signal chain of the optical imaging solution is the focal plane array. It is a grid of photo-diodes which converts the incoming light into electrical charges. Photo-diodes are often characterized based upon these three specifications namely dark current, quantum efficiency (responsivity) and rise time (bandwidth). The silicon based p-n/pin diodes have maximum optical sensitivity (amount of incident light converted into electrical current), around an incident wavelength around 800-850nm. Silicon has very large absorption length, hence its device structure needs to be very precisely optimized to support the Infrared detection. Apart from Silicon based photo-diodes, a lot of other detector compositions have been studied in the past which might be more suitable for the Infrared spectrum [9]. Please refer to figure 2.1 [9] comparing the spectral sensitivity of various semiconductor photo-diodes in several materials structures spanning all the way from UV (>200nm) region to LWIR (>1400nm).

In Figure 2.2 [9], absorption length is plotted for different semiconductors. For a visible spectrum ranging from 600-850nm, the light penetration depth is larger than 6um but less than 10um which means a very little fraction of light is absorbed in the junctions and walls, while most of it is absorbed in the substrate.

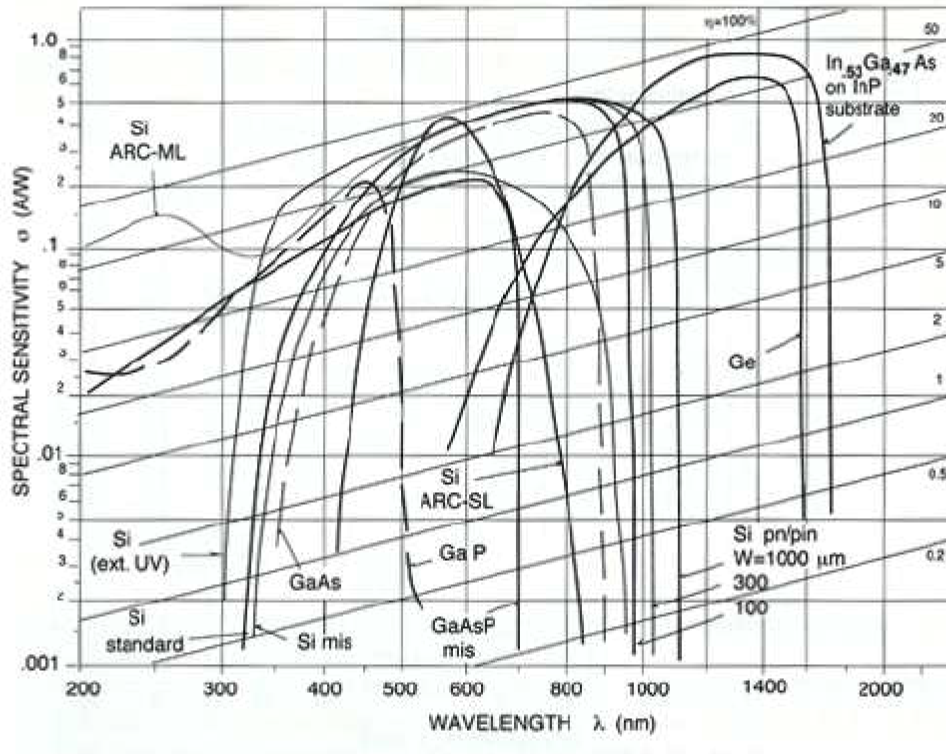


Figure 2-1: Spectral sensitivity of different photodiodes. Reprinted from [9]

Our end application targeted is Infrared Imaging Solution, but Silicon doesn't absorb a wavelength more than 800-850nm (for higher wavelength, the penetration depth is very high for silicon), hence its sensitivity reduces dramatically as the wavelength increases. For Infrared solutions, InGaAs is an optimal choice but that cannot be fabricated in the silicon. Hence a hybrid solution (multi-chip module, flip chip bonding using Indium bump pads etc.) as shown in figure 2.3 [11] [20] needs to be designed which was not feasible for the extent of our project. Hence, we decided to showcase the performance of our read-out Integrated circuit with a silicon photo-diode

operating in visible spectrum rather than infrared region. A detailed description of the silicon based photodiodes designed for the thesis work has been given in section 3.

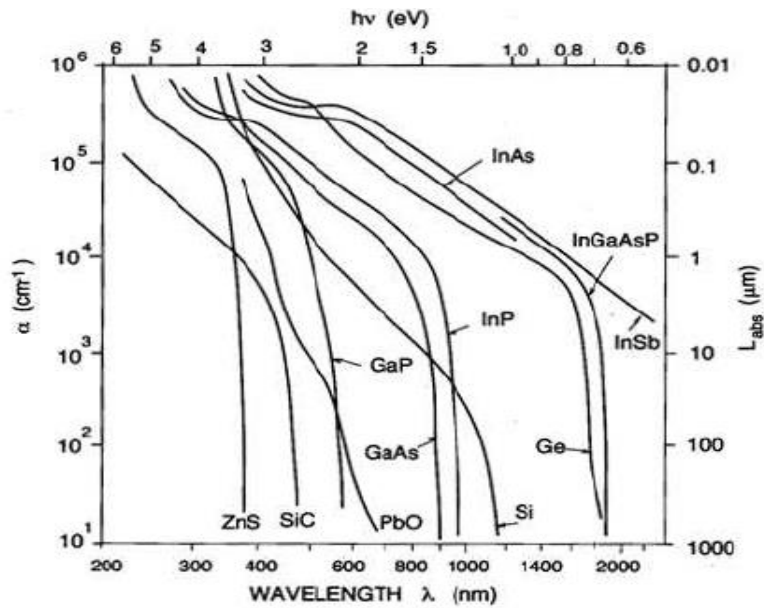


Figure 2-2: Absorption length of various photo-diodes. Reprinted from [9]

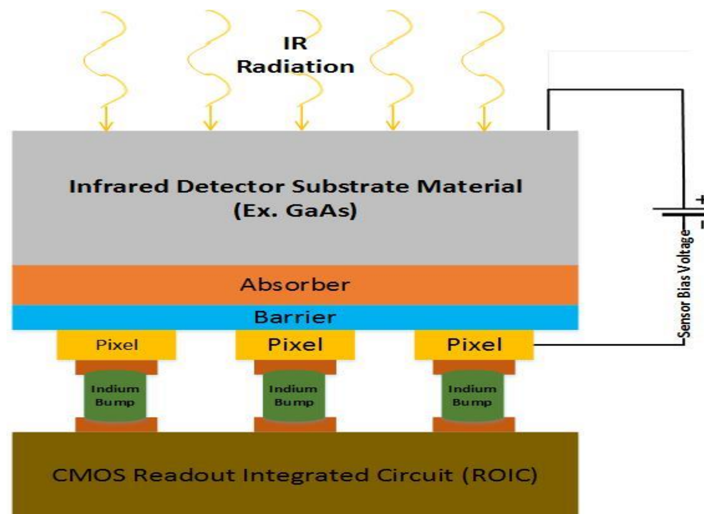


Figure 2-3: Generic Infrared pixel detector

2.2 READOUT INTEGRATED CIRCUITS (ROIC)

The detector array used in the FPA outputs the signal in the form of the current. As shown in the figure 2.4, the current from the photodiode (due to excitation) is fed into the read-out cell, there it integrates onto the integration capacitor and gets converted to voltage which can be digitized and processed further [10] [12]. So, therefore the readout cell has a very important function of extracting out the information from the incoming photo-diode current and convert it into a form which can readily be used by ADC's to convert it into digital form. Simultaneously, the read-out cell also biases the photo-diode for its operation in the region of interest [12].

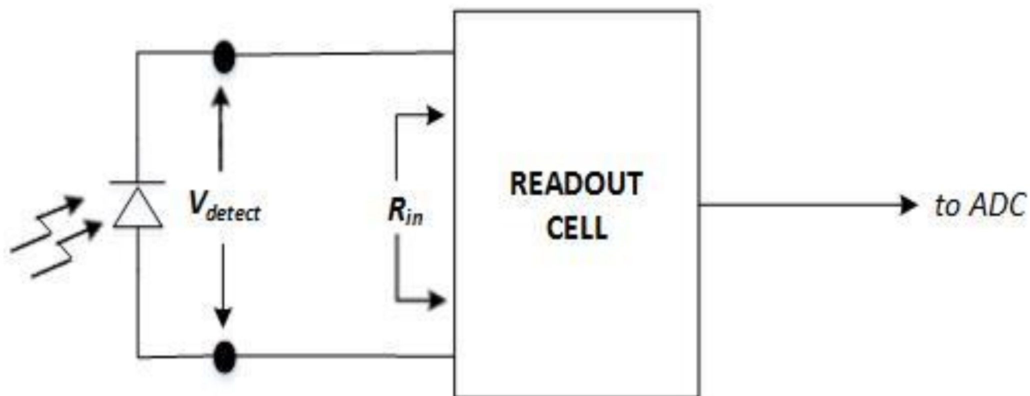


Figure 2-4: Readout Cell Schematic Description

2.3 IMPORTANT SPECIFICATIONS OF THE ROIC

As ROIC serves as an interface between the photo-diode array and the ADCs, it is an important block and plays a very considerable role for the overall system design. The photo-current generated by the photo-diode is partially shunted by the photo-diode resistance as shown in figure 2.5 and reduces the photocurrent transferred to the readout

circuit. There is a terminology used to define the amount of photo-current transferred to the readout circuit from the photo-diode current, it's called as injection efficiency.

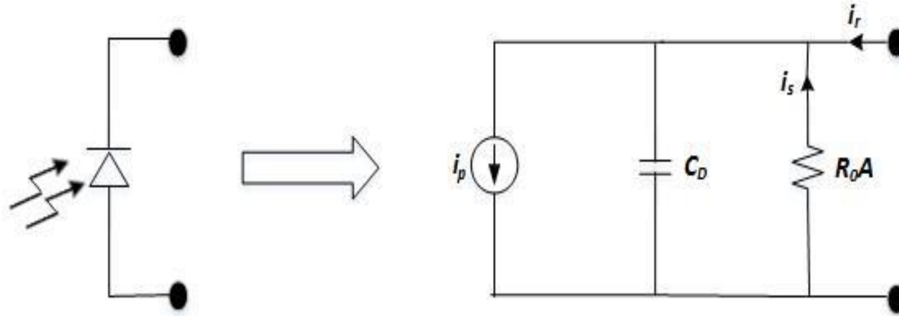


Figure 2-5: Equivalent Photo-diode Circuit

$$n_i = \frac{i_r}{i_p} = \frac{R_o A}{R_{in}}$$

Where the injection efficiency n_i is given by the above equation.

Apart from the injection efficiency, the parasitic capacitance C_D limits the bandwidth of the circuit. Therefore, to increase the effective bandwidth, the cell ideally should have as little resistance as possible. As the frame rate for the imaging solutions are usually lower, the bandwidth usually comes out to be lot larger than that. So, in a general scenario, to increase the performance (bandwidth) of the imager, a very high output resistor and small output capacitance is desired for the photo-diode (PD). But certainly, that the output resistance can't be increased beyond a certain limit due to the device structure and imperfections, the input resistance of the cell should be even lesser for a sufficiently good imager performance.

The responsivity, dark current and shot noise generated by PDs are all dependent upon the bias voltage which should be very stable and should not change as the voltage at the integrating cap changes. The biasing voltage circuitry should be optimized to provide a very stable biasing supply to the photodiode.

Another important performance metric for the readout integrated circuit is the dynamic range/sensitivity that the cell can capture. From the application view-point, it must be as high as possible so that we can capture both high illumination images and low illumination images at the same time. Hence the dark current, the size of the integrating capacitor determines the dynamic range that a readout cell can capture. In practice, a higher value of integrating capacitor is required to capture large dynamic range which in turn increases its size.

Size of the readout element is another critical parameter which needs to be considered while designing the readout cell. Ideally the readout cell should be smaller than the detector array pitch so that they can be easily bonded to each other without any hassles. The more advanced technology nodes help us in cutting down the pixel size and packing more circuitry in the same pixel pitch as earlier.

Frame Readout rate also needs to be seriously taken into consideration as more dynamic patterns need to be captured. The frame rate is affected by the integrating capacitor time, pixel array time, ADC conversion time, readout time etc. Out of these the integrating time is usually the dominant limiter of the frame readout rate. Hence it needs to be taken into consideration while designing.

Lastly, the power consumed by the readout element is a very important metric and especially given that in the latest systems the size of the pixel array is continuously increasing. The total power consumed by the entire readout array usually increases with the size of the array and hence places a very heavy reliance on the cooling-down system.

2.4 CONVENTIONAL READOUT CELL CIRCUITS

In the conventional analog ROIC's (Read-out Integrated Circuit), the photocurrent generated in the detector is integrated onto an integration capacitor which is then further multiplexed with many pixels and then digitized using an ADC which can either a pixel/column level ADC. The dynamic range for these conventional structures is often constrained on both the lower and higher side of illumination due to maximum charge storage capacity of the integration cap on the higher side and dark current/noise on the lower side. A generic structure of the unit element (pixel) is presented in Figure 2.6 [13]. In conventional readout cells, the maximum well capacity is often limited to 10's of million electrons. This is usually achieved by 1pF of Integration capacitor which if implemented in 65nm using a MIM capacitor will occupy 400um^2 of area. This is more than 60% of the pixel area. Plus, still the maximum well size is still limited to 15-25Me-. Given that pixel saturates at higher illumination and is not able to capture the lower brightness due to minimum limit posed on the frame rate, the maximum dynamic range that it can capture is often limited.

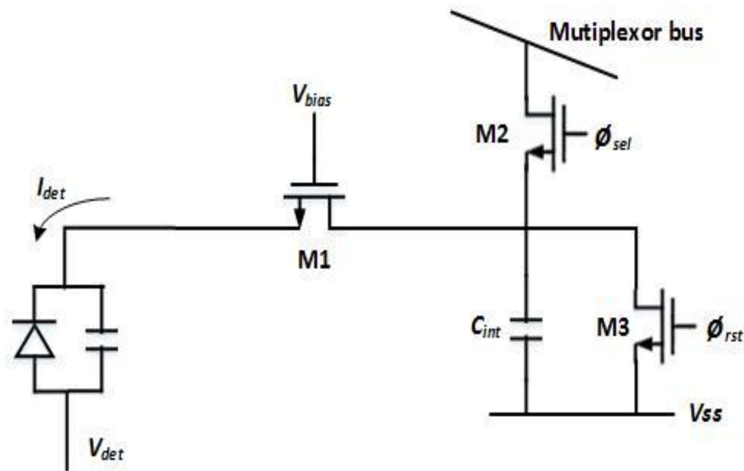


Figure 2-6: Conventional ROIC – Direct Injection

There are many other architectures available in the literature for the ROIC like Buffered direct injected cell, Gate modulated input (GMI) cell etc. But all of them poses serious constraints on the dynamic range, readout frame rate, power consumption and pixel size. These challenges necessitate a need to develop a more robust wide dynamic range and high-speed read-out rate read out integrated circuit which should be easily scalable to accommodate large pixel array format. This is where Digital focal plane array comes to rescue and provides a much more beneficial solution to all the above challenges.

2.5 DIFFERENT ADC ARCHITECTURES

The readout cell outputs an analog voltage signal. For infrared and visible imaging applications and in general for most of the imaging applications, the voltage output will need to be digitized using an ADC for image signal processing, display and storage etc. It would be ideal if we are able to convert the signal directly to digital data

inside the ROIC as it would reduce the noise coupling and thereby increase the SNR. The main attributes for the on-chip ADC is that it should consume very low power, should have high sensitivity with sufficient precision, lower conversion time, lower noise and higher sampling rate etc.

Global ADC: Global ADC topology implements one single ADC to resolve the whole pixel array data. The conversion rate is typically around 10MS/s to 100MS/s, according to pixel array size and frame rate requirement. Please refer to figure 2.7 for one of the examples of Global ADC architectures as implemented in literature. The typical ADC architecture in here is pipelined-ADC or SAR-ADC. Since all pixel data is converted through the same ADC, any distortion within the conversion will be common-mode background noise and does not cause fix-pattern-noise (FPN). Single ADC also reduce the complexity of digital background calibration. However, as pixel size increases, the ADC conversion rate needs to be increased too. For example, from 1MP to 2MP pixel array, ADC conversion rate needs to be increased by two times. Two time-interleaved ADCs are usually utilized to support high conversion rate and consumes very high power. Typically, global ADC architecture is used in pixel array smaller than 1MP.

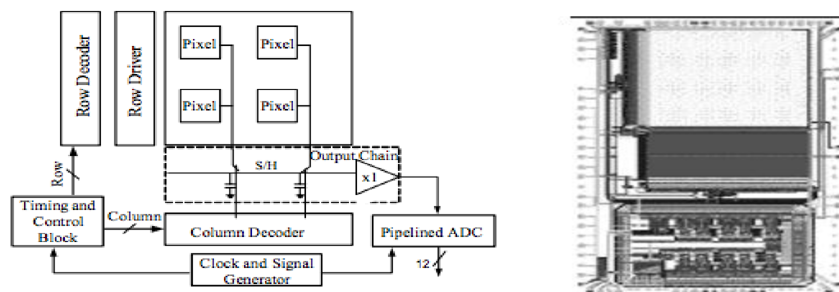


Figure 2-7: Global ADC architecture. Reprinted from [14]

Column ADC: Column ADC topology is to utilize a low-power ADC in each column to speed up the conversion rate. The most well-known ADC design for column ADC is “single-slope ADC.” In the design, a ramp signal is used to compare with CDS output (pixel output). A digital counter is synchronous with that ramp signal. As the ramp signal is larger than CDS output, the counter output is latched and the digital value is:

$$DN = V_{CDS} / (slope\ of\ ramp)$$

Since it is a low ramping, the ramping and counter signals can be generated globally (Fig. 2.8) and the rest of parts implemented inside columns are low-power circuits such as the comparator and time register. Therefore, the power of each column circuit can be greatly reduced. Since the power of column ADC is less sensitive to array size than that in global ADC, column version can support large pixel array. The challenge of column ADC is the mismatch (gain error, and offset) in each column. The mismatch can come from process variation and circuitry design. A background column FPN (CFPN) calibration is needed.

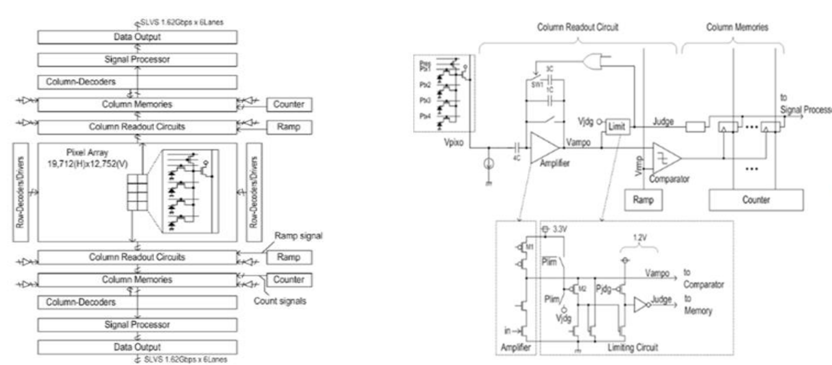


Figure 2-8: Column ADC Architecture. Reprinted from [15]

2.6 DIGITAL READOUT INTEGRATED CIRCUIT WITH BUILT-IN ADC

DROIC overcomes the limitations of traditional readout cells by doing analog to digital conversion inside the pixel. The DROIC leads to a very large sensitivity due to much lesser noise, and can perform a lot of on the chip signal conditioning digitally. The basic DROIC unit-cell circuit [13] is presented in the figure 2.9.

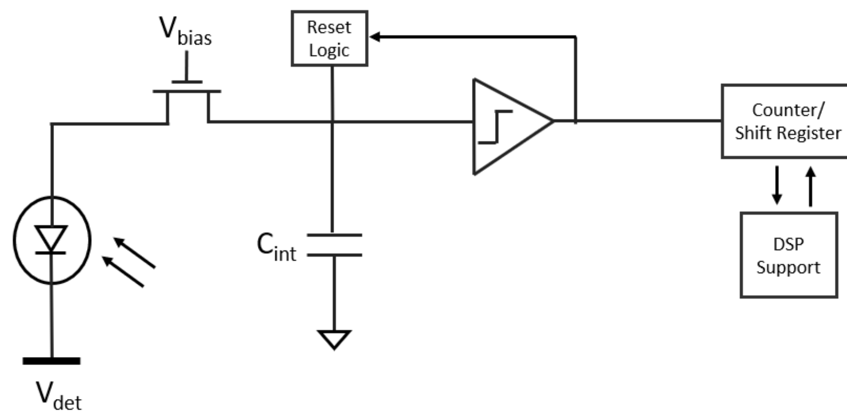


Figure 2-9: DROIC Unit Cell

The basic building blocks of a DROIC are direct injection pre-amplifier, integration capacitor, reset circuit, a comparator (I to F converter) and a counter. Finally, the data need to be serialized and read out. Here since the integrating capacitor gets reset each time the comparator trips, the maximum well capacity is not limited by the capacitor size but rather by the counter resolution. Similar on the lower current side given that the integration capacitor is very small, we will not be limited by the very low frame rate to capture very small currents. Hence DROIC can certainly extend the dynamic range without much system/circuit design constraints. Since the integrating

capacitor size is drastically reduced, the overall pixel pitch can be reduced. All the major blocks used in the pixel are digitally implemented, hence the read noise will be of a very small order.

2.7 DYNAMIC RANGE OF THE PIXEL SENSOR

Pixel's dynamic range (DR) is its ability to capture the scene information both under very bright condition (broad day sun light) and also under very dark conditions (night) without saturating the pixel for higher brightness and under-utilizing the pixel resolution for lower brightness.

$$\text{Dynamic Range (DR)} = 20\ log_{10} \frac{i_{max}}{i_{min}}$$

The higher side of the DR is constrained because of the maximum charge holding capacity of the integrating capacitor whereas on the lower side it is constrained by the maximum possible integration time for a given noise current.

Therefore, if the dynamic range need to be increased, we have to either increase the i_{max} and/or reduce the i_{min}. There are several available methods in the literature [36] [37] [38] for extending doing the same, some of them have been listed below.

Multiple Capture Scheme: This method increases the DR of the readout cell by capturing the information from a pixel with different integration times and then combining them in post processing using an algorithm in DSP [16] as shown in Figure 2.10. The algorithm to run efficiently, will require an on-chip memory bank to store different capture values and also good hardware signal processing capability [17]. The dominant blocks which consumes power are the on-chip memory, the signal processor and also the readout. As the number of captures can be significantly large for small

photo-diode currents, this scheme will increase the memory size drastically and reduce the readout time as the photo-diode current reduces.

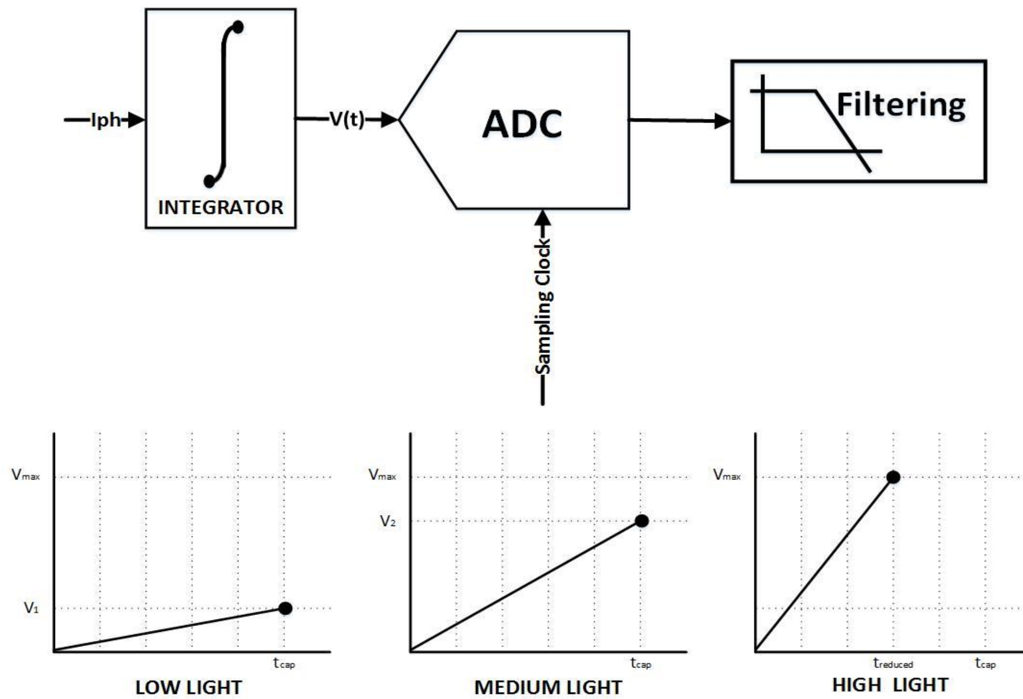


Figure 2-10: Multiple Capture Scheme

Logarithmic Sensor: In logarithmic readout cell, the voltage signal is directly generated by the readout cell rather than integration unto an integration capacitor [18] [19], using the non-linear response curve of the MOSFET in the sub threshold region as shown in figure 2.11. Up to 4-5 decades of input signal can be fit into a small voltage range (based upon the V_t of the transistor and number of series transistors). There is usually a lot of variation in the transistor characteristics in sub threshold region. And the also the succeeding circuitry need to be extremely precise so that it can make use of the dynamic range that we have packed into such a small voltage range. The non-integrating

nature of the sensor also usually leads to higher noise and other non-idealities, hence should be accounted for.

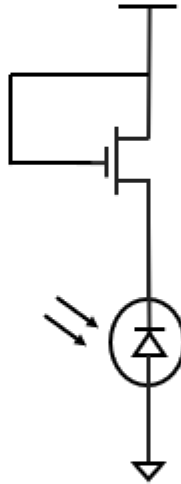


Figure 2-11: Logarithmic compression technique in Sensor

$$v_{out} = k \; ln \frac{i_{ph}}{I_o}$$

So, all the present architectures have some challenges either in the terms of design, complexity, read-out rate or precision to meet the wide dynamic range requirement of the pixels. In this thesis, we are trying to demonstrate a new method through which the DR of the pixel sensor is increased without sacrificing the readout rate, design complexity, precision or other variables.

3. PHOTODIODE DESIGN

3.1 INTRODUCTION TO THE PHOTODIODES

A photo-diode transforms the incident light into the current. In optical-electronic systems such as cameras, telescopes etc., photo-diodes are the first and the basic component of front end electronics of a camera. In this research work, the incident light reflected from the surfaces will be sensed by the silicon photo-diodes and afterwards the electrical signals produced by the photo-diodes will be converted to digital domain using a read-out integrated circuit (ROIC) for post processing.

There are four major specifications associated with the photo-diodes, namely their responsivity, optical bandwidth, dark current and their parasitic capacitance. These are heavily dependent on the geometry of the photo-diode, junctions used to design them, process node, and on the material which are used in fabrication process. Silicon photo-diodes are solid-state devices exploiting the internal photoelectric effect, as opposed to the photoemission effect. It stands out to be a good material for photo-detection purposes mainly because it has high mobility of charge carriers (defines the speed/bandwidth of the photo-diode), low dark current (increases the sensitivity of the photo-diodes) and the pre-dominance of electron-hole pair generation compared to phonon generation or single carrier excitation (leads to higher quantum efficiency/responsivity) [22]. Junction photo-diodes are the most common semiconductor photodiodes due to their generally good performance and low cost [21].

When incident photons carry energy larger than silicon's bandgap, pairs of electron and holes are created as light fall on a reversely biased p-n junction. This exact phenomenon happens inside a p-n junction photo-diode (inside the depletion created in between the type junctions) as shown in Fig. 3.1 [23]. Now, because of the strong unidirectional electric field, as soon as the electron-hole pair are created, they are swept away towards their majority carriers. The sweeping of the majority carriers leads to drift current. On the other hand, photons absorbed inside the neutral region, diffuses in the all possible directions. Some of them reaches the depletion region, and thereby are pulled by the majority carrier region. In total three are 2 diffusion currents (created in both the neutral regions) and one drift current [23].

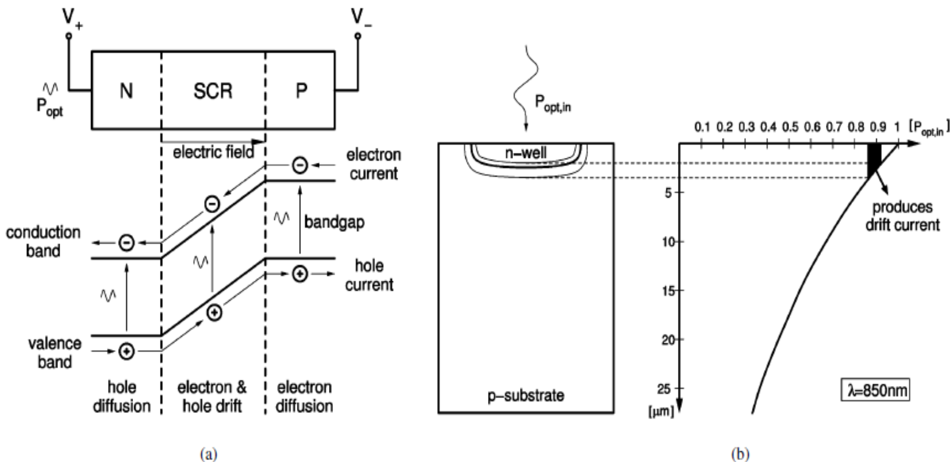


Figure 3-1: (a) Carrier generation in reverse biased p-n jun. (b) Relation between junction dimensions and the penetration depth. Reprinted from [23].

The useful photocurrent generated by the photo-electric emission can be written as [24]:

$$I_{op} = q \times go_p \times A\ (W + L_n + L_p) \qquad (1)$$

where W denotes the width of depleted region, go_p is the rate at which pairs of electron-hole are generated, q the electronic charge, L_p the diffusion length of holes, L_n the diffusion length of electrons, and total junction area with side and bottom-walls is denoted by A [24]. The depletion width is a function of the doping purity of the p-n type materials of which the diode is made and also the reverse bias voltage which is applied across the diode.

In addition to the p-n junction design, doping concentrations etc., its spatial location also determines the responsivity we get from the photo-diode. For instance, if the junction is shallow, it is possible that a lot of electron-hole pairs generated might not contribute to the actual current as compare to a deeper junction whereas owing to better collection efficiency the overall quantum efficiency might be higher. Over-all the junction depth, doping concentration, wavelength of light captured all have a great influence on the sensitivity of the photo-diode and should be seriously taken into consideration. [25]

Other than the responsivity of the photo-diode, other photo-diode specifications like dark current (photo-diode output in the absence of the incoming light), thermal noise are heavily dependent on the composition of the diode and its physical design. Dark current is produced where is there no optical light falling, due to the random thermal

motion. It is one of the major contributor to noise under low light conditions and often determines the dynamic range performance on the lower side of the illumination. [26].

Above analysis proves that the various characteristics of the photo-diodes designed using p-n junction depends on the junction used for the diode, and various properties of the PD material. With CMOS process, multiple methods are present for designing a p-n diode. For deciding on the most suitable photo-diode structure, different types of photo-diodes are investigated and listed with their characteristics and difference in the following section 3.2. Types of Photo-diodes; and in section 3.3 we will discuss the layout of the Photodiode as it is implemented in our design with specific layers used.

3.2 TYPES OF PHOTO-DIODES

In standard CMOS processes, different kinds of photodiodes can be implemented using basic layers. Since in the over-all pixel design only a fraction of area is reserved for photodiodes, the highest possible photo-current value is desired to obtain from this limited area, i.e. highest quantum efficiency/responsivity is aimed from the photo-diodes.

In this section, various kind of photodiode structures are studied and compared against with each other, by keeping in mind the three major specifications characterizing them (optical bandwidth, responsivity, and dark current) figure 3.2 [27] [28]:

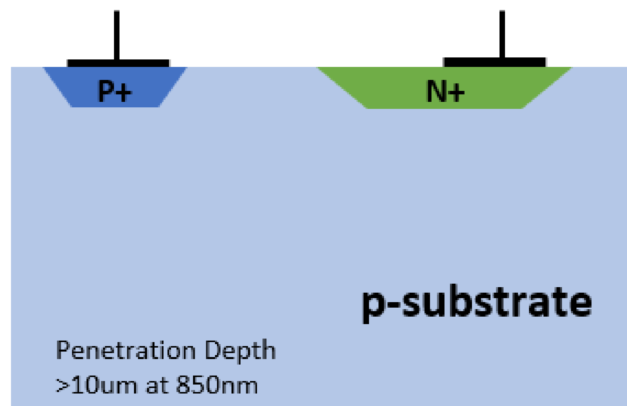
- N-well / p-substrate
- N+/ p- substrate
- P+/N-well/p-substrate

- T-well/N-well/p-substrate

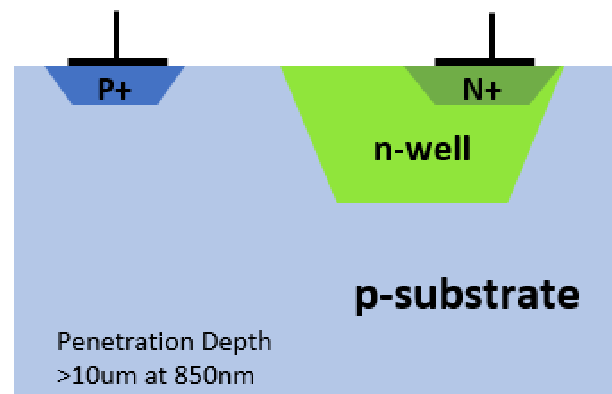
For different types of photo-diodes we also considered the fingered structures. Fingered structures are used for increasing the area of the junction for fixed width stripes. However, it was learned that a default process layer called shallow trench isolation (STI) prevents current flow between the layers, which annihilates the positive effect of fingering. For avoiding this process extra masks are needed, which costs additional money. [28] Thus, fingered structures were not further considered.

3.2.1 N-well/P-substrate Photodiodes

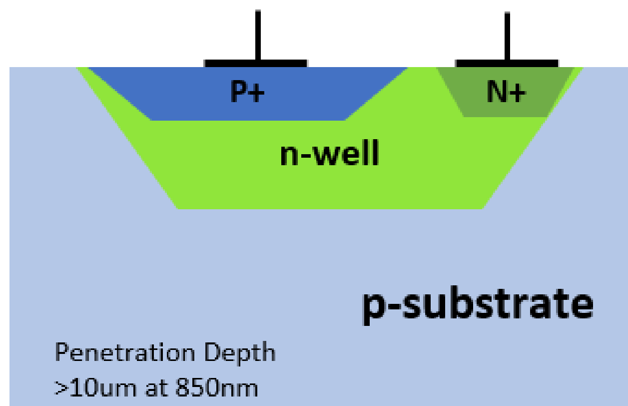
The most common photodiode is designed using n-well / p-substrate. Its depletion region is very lightly doped. As doping concentration is smaller for n-well as compare to the higher n+ diffusion layer, the depletion width is larger. The increase in depletion width considerably cuts down the junction capacitance. As the depletion region's width is larger, it should better help us in improving the photo-diode responsivity as its collection efficiency should be higher [25] [22]. The smaller junction capacitance of the diode also improves the Q-to-V conversion. Wider the depletion region, higher the probability of photon absorption becomes. The p-n junction is located deeper in the substrate; thus, this photo-diode is suitable for high penetration depths. [25] [22].



(a)



(b)



(c)

Figure 3-2: a) N-well/P-substrate b) N+/P-substrate c) P+/N-well/P-substrate

3.2.2 N+/P-substrate Photodiodes

This type of photo-diode introduces one diffusion layer in between, n+ implant layer/p-substrate region instead of using a n-well directly. It is a kind of scaled down version of the N-well & p-substrate based photo-diode having a higher doped n-region (N+, instead of lightly doped N region). As per design rules, this structure can be made more compact (as there are restrictions on the minimum n-well spacing/size from p-substrate for n-well and p-substrate photodiode etc.). But since N+ ions are used instead of lightly doped n-well, junction is formed relatively close. This causes a degradation in the responsivity of the photodiode. This structure is more suitable for the smaller wavelength as compare to higher [25] [22].

3.2.3 P+/N-well/P-substrate Photodiodes

This photo-diode is very much like N-well & p-substrate based photo-diode but adds another implant of p+ diffusion layer above the n-well diffusion. This has two-fold advantage. The first advantage is that in similar junction area, 2 diodes are in parallel (p+/N-well, N-well/P-substrate), hence our depletion region widens. This leads to higher quantum efficiency. Overall this creates a depletion width even much larger than the n-well/p-substrate type photodiode. Secondly, it is expected for this photo-diode to have much smaller dark current as compare to basic photo-diode. It is known the un-occupied interface states due to lattice deformities at the surface leads to dark current, but because of p+ implant, there should be more free charge carriers at/near the surface. Hence the photodiode is expected to have lower dark current and lesser noise [25] [22].

3.2.4 Designed Photodiode Approach

In this research, a different photo-diode design methodology has been taken to improve the photo-diodes sensitivity and make them better useable for our application. Instead of N-well/P-substrate junction, the p+/n-well/p-substrate junction has been used which assists in removing the ultra-slow diffusion carriers associated with the p-substrate. To increase the photo-detection efficiency further, the reverse biased junction (p+/n-well) will be controlled from the external supply which in turns control the photo-diode avalanche gain. Hence an Avalanche photo-diode is designed out of this 3-layer structure [28] [29].

3.3 LAYOUT OF THE PHOTO-DIODES

The p+/n-well/p-substrate type photo-diode has been found to be the most convenient for this project. There are several ways to layout a photo-diode like area version or finger version [22]. There also need to be special attention given while laying out the photo-diode.

- Metal layers usage should be kept to minimum within the active region. As most of the metal layers are opaque to the incoming light. We need to make sure that metal layers are removed from the top of the active diffusion area. Otherwise the light will not reach the photo-diode, and the photo-sensitivity of the diode will reduce dramatically.
- There is a trade-off between the contact resistance and the parasitic capacitance. You want to minimize the contact resistance by having more number of the

connections with the p+/n-well/p-substrate regions but also don't want to aggravate the parasitic capacitance.

- The area apart from the active diffusion region of the photo-diode should be made opaque, so that photons don't get scattered in the circuitry other than photo-diode. This can otherwise cause leakages and optical coupling etc.
- Another layer which doesn't let the light pass through and is opaque in nature are silicide's. Make sure that the layout doesn't have the silicide layer on top of the active region. In this way, you can make sure that light does reach the photo-diode active region.
- Another thing to look for laying out the photo-diode is metal dummy layers; usually metal dummy layers get inserted during the metal fill in the final stages of the layout. As most of them opaque, we need to make sure that we use dummy block layers on top of the active diffusion region of the photo-diode so that the normal operation doesn't get hurt.

3.3.1 Fingered Photo-diode Layout

Fingers are a critical component which can further improve the sensitivity and bandwidth of the photo-diode. Efficiency will be increased mainly because there are more sidewall junctions with a compromise of less bottom junction. Increasing the junction area through side-wall should give a boost to the responsivity and bandwidth. Thus, using fingers instead of area layout photo-diode can be a better proposition for larger bandwidth and higher sensitivity. The problem with the fingered structure is that a

default process called as shallow trench isolation (STI) prevents side-walls to contribute to the photo-sensitivity. To make a mask avoiding STI is costly, thus fingered structure is not a good option for this work.

3.3.2 Area Photo-diode Layout

The area layouts are much simpler and easy to design as compare to fingered structures [30]. We designed a square shaped photo-diode with basic diffusion layers present in 65nm CMOS. The size of the optical window is 10um x 10um and the whole photo-diode has the size of 15um x 15um. Figure 3.3 shows the full layout of the photo-diode including all the layers (including the diffusion layers, metallization, silicide block layer, dummy metal layers) etc. Table 3.1 gives a description of all the layers used in the photo-diode layout. Figure 3.4 deals with the step by step guide of how each layer of the APD layout is done step by step. The final APD layout has been used in 16 x 9 pixels for optical testing where the reverse bias voltage will be optimized for controlling the APD gain and thereby sensitivity.

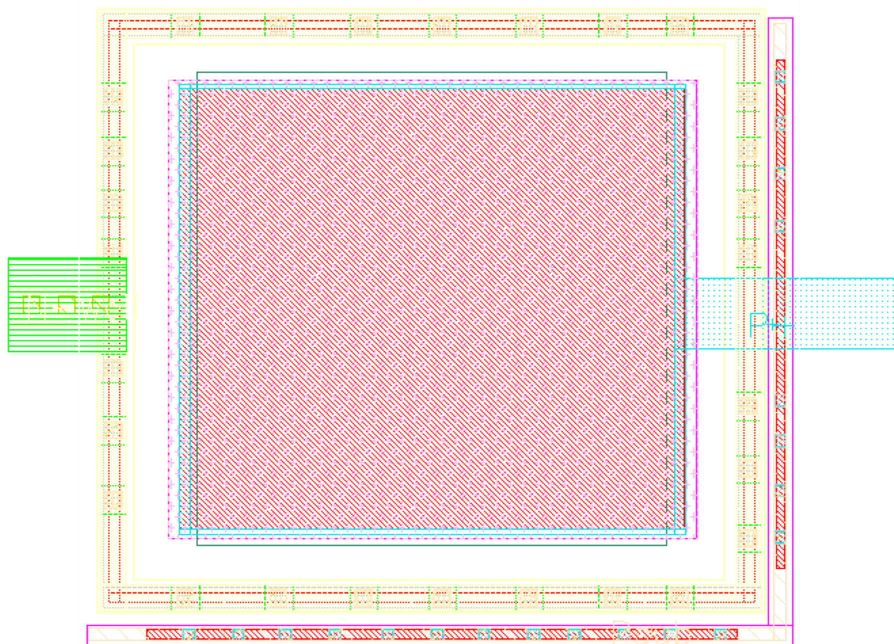


Figure 3-3: Photodiode Layout

Table 3-1: Layers used in the photo-diode layout and description

Layer/s Name	Description
OD	Active Diffusion for 1V devices
NP	N+ Implant
PP	P+ Implant
N-well	Lightly Doped N well
M1-M8	Metallization
RPO and RH Layers	Silicide Block Layers
DM1-DM9, POBLK, ODBLK, DMEXCL	Dummy Block Layers

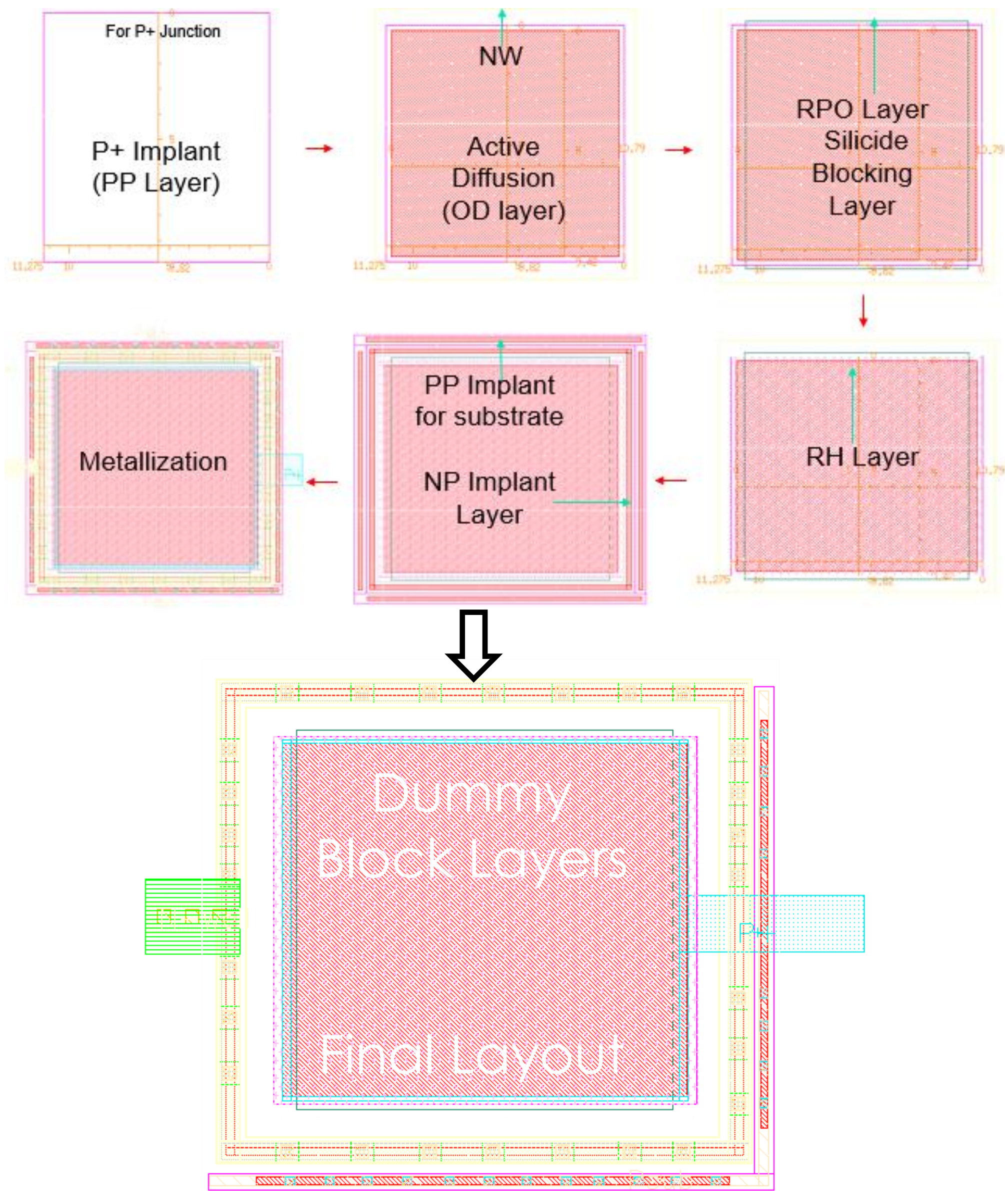


Figure 3-4: Step by Step Guide to final photo-diode layout

4. IMAGE SENSOR DESIGN SPECIFICATIONS

4.1 CIRCUIT AND SYSTEM LEVEL SPECIFICATIONS

Table 4-1: Circuit and System Image Sensor Specifications

Specification	Value	Comments
Minimum Photo-diode Current to be captured by the Image Sensor	20pA	This can be even lower, depends on the receiver BW, photodiode responsivity and application
Maximum Photo-diode Current to be captured by the Image Sensor	20uA	This can be even lower, depends on the application etc.
Maximum Integration time for the photo-diode current	500us – 1ms	This is mainly decided by the maximum frame rate and minimum photodiode current
Dynamic Range	>= 120dB	Will cover well both the high and low illumination regions
Photo-diode Responsivity	0.3-0.4 A/W	
Counter Size	10-12 bits	Cut down the counter size to reduce the power consumption
Readout Frame Rate	100Hz- 500Hz	Should be user Controllable
Pixel Array Size	16 x 16	
Fixed Pattern Noise (FPN) Calibration	Digital/Analog	Preferably Digital Method
Power Consumption	Ultra-low Power	
Digital Interface	FPGA-Compatible	

4.2 DIGITAL READ-OUT INTEGRATED CIRCUIT (DROIC)

In this work, we have implemented DROIC as it overcomes the limitations of conventional readout cells by performing analog to digital conversion inside the pixel.

The DROIC leads to a very larger dynamic range, much lesser additive noise, and a lot of on-chip signal processing.

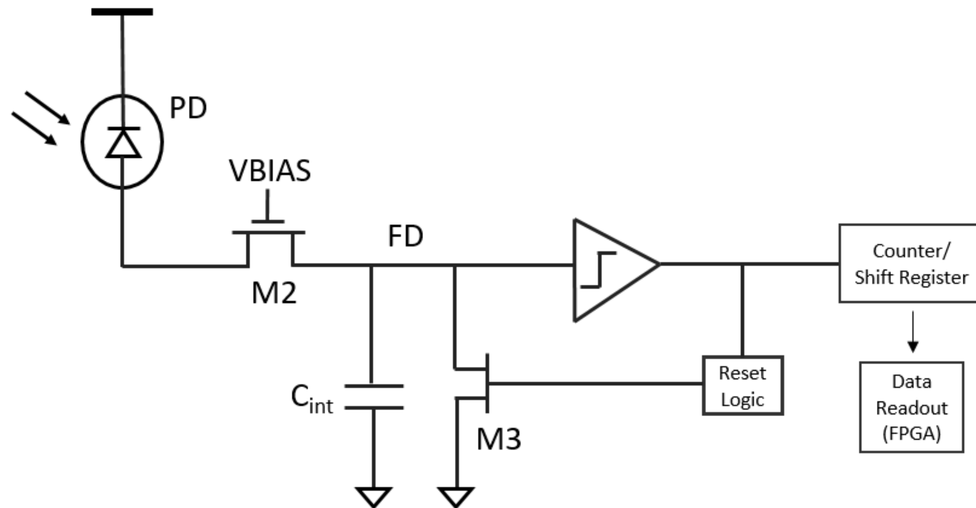


Figure 4-1: Digital Read-out Integrated Circuit (DROIC) Unit Cell

The basic building blocks of a DROIC are direct injection pre-amplifier, integration capacitor, reset circuit, a comparator (I to F converter) and a counter. Finally, the data need to be serialized and read out. Here since the integrating capacitor gets reset each time the comparator trips, the maximum well capacity is not limited by the capacitor size but rather by the counter resolution. Similar on the lower current side given that the integration capacitor is very small, we will not be limited by the very low frame rate to capture very small currents. Hence DROIC, without any design constraints can certainly extend the dynamic range. Since the value/size of integrating capacitor is drastically reduced, the overall pixel pitch can be reduced. All the major blocks used in the pixel are digitally implemented, hence the read noise will be of a very small order.

The working operation of the DROIC has been presented in the next section of the unit cell description.

4.3 WORKING OPERATION OF DIGITAL READOUT INTEGRATED CIRCUIT (DROIC)

The working operating of the DROIC is explained by refereeing to figure 4.1. At the beginning of integration, the infrared photo-diode captures the photon energy and converts it into a photocurrent (Iph) based upon its optical responsivity that charges the integration capacitor (Cint) on floating node (FD). A pixel comparator is utilized to sense the voltage level of FD. Once the FD crosses the trip point of pixel comparator, it will trigger a pulse signal and reset FD through the reset device (M3). FD will recharge again till it crosses trip point and trigger the next reset pulse. Therefore, a linear relationship between photocurrent and frequency of pixel reset can be obtained if an ideal (delta) pulse signal is applied:

$$frst = Iph / (Cint*Vtrip) \tag{1}$$

where *Cint* is integration capacitor, *Vtrip* is the trip point of comparator, and *frst* is the frequency of pixel reset. In ADC part, a counter, counts the number of times pixel resets the floating node (FD).

For a limited integration time (Tint), the counter output is:

$$Cout=frst*Tint \tag{2}$$

replacing the first with (1), we can get:

$$Cout = [Tint / (Cint*Vtrip)] * Iph \tag{3}$$

Thus, the counter output is a digitized photocurrent value times a linear gain Tint / (Cint*Vtrip), and the LSB photocurrent for the ADC is:

$$LSB\ (A) = (Cint*Vtrip)/Tint \tag{4}$$

According to (4), we can notice that the LSB is related to the integration time of pixel. At longer integration time, we can achieve higher resolution for the ADC but lower measurement range due to the fixed dynamic range (let's say if we use a 10-b ADC in this case), while at shorter integration time, we can achieve larger measurement range but lower resolution.

Thus, the integration time will need to be made adaptive based on the illuminance condition: at strong illuminance, the resolution of brightness is not critical so we can use longer integration time to extend measurement range. At low illuminance, the resolution of brightness is critical due to the low contrast ratio in the dark image, and a short integration time can be used. To cover the bright region and dark region in one image frame, multiple lengths of integration time are used. In this method, multiple frames that are captured with different integration time are merged together in image signal processor either using Digital Signal Processor or FPGA. The merged image preserves the high brightness value in the frames of short integration window and the high resolution in the frames of longer window. As the technique relies on a powerful image signal processor to merge the different images captured during lower and higher integration time conditions, it consumes the extra power and chip area and is often tedious to implement. In this research, we implemented an automatically adapting

integration time control at pixel-level that doesn't require a background signal processor. This is explained in the next section.

4.4 ADAPTIVE INTEGRATION TIME CONTROL

To capture the six-fold of dynamic range (>120dB), we would ideally need more than 20 bits of ADC. But implementing a 20Db is not feasible practically from the power consumption, performance and area point of view. Hence, we need to devise a low power scheme with which we shall be able to capture this wide dynamic range using a smaller bit ADCs, something like 10 or 12 bits. In our case the best way to meet the wide dynamic range is through control of the Integration time but to remove the big, bulky image signal processor (as it consumes large amount of chip area, power etc.), we need to make the Integration time adaptive in our system.

Fig. 4.2 shows the trade-off between Full-signal-range (FSR) and LSB of ADC versus pixel integration time. Shorter integration time achieves large FSR and LSB. It is suitable for strong illuminance condition since we need a wide FSR to cover the input signal amplitude. The LSB is not critical in strong illuminance. This is because the retina in human eye cannot identify the small brightness change at high illuminance. On the other side, long integration time achieves small FSR and LSB and suitable for low illuminance condition. FSR is not critical here because of the low input signal amplitude. The resolution, however, need to be high since a slight change of brightness in dark condition can be detected by human eyes. For covering both high and low illuminance, we proposed a new adaptive integration time control that doesn't require back-end digital circuitry.

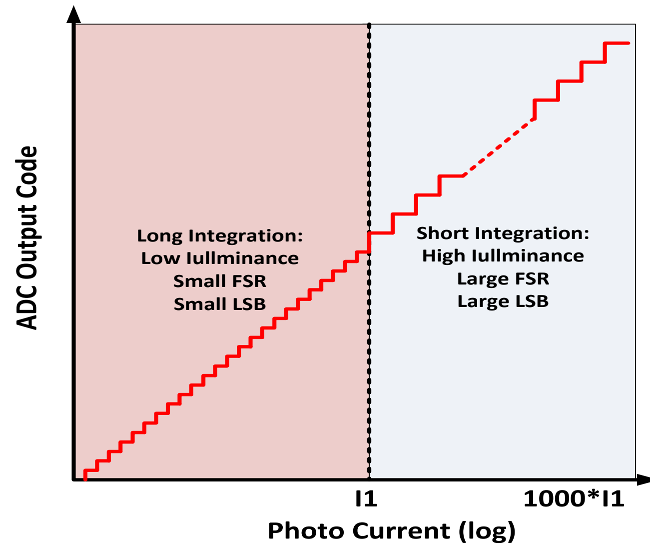


Figure 4-2: Integration Time vs. Full-signal-range (FSR) and LSB

The concept of adaptive integration time can be illustrated by the pixel integration timing diagram as shown in Fig. 4.3. Let's assume, that each pixel starts the integration of the photo-diode current after the GLOBAL_RESET pulse is pulled low. Due to the integration of photo-diode current, the FD node will rise and reset low repeatedly. Now let's take two cases. In case 1, the photo-diode is illuminated under high brightness, means it generates large photo-diode current. Now, because this pixel is illuminated strongly (i.e. PIX1), T1 is used as the integration time, the ADC counter stop integration after end of T1. On the other side, for the case 2 let's assume that photo-diode is illuminated under very low light conditions. Now, because the pixel (PIX2 in this case) receives low illuminance, it will not trigger the counter even once during the T1 integration time hence the pixel Integration period is automatically increased to more than T1 till T2. But because the integration time is larger, the resolution (LSB size) will be lower. Let's assume that the T2 integration time is self-adaptively increased to

1000*T1 to achieve higher ADC resolution. The ADCs (let's assume that the counter size is 10 bits) output value will be resolved as:

$$D_{out} = CNT\ [9{:}0]\ {*}1000\ (if\ Tint{=}T1)$$

$$D_{out} = CNT\ [9{:}0]\ (if\ Tint{=}T2)$$

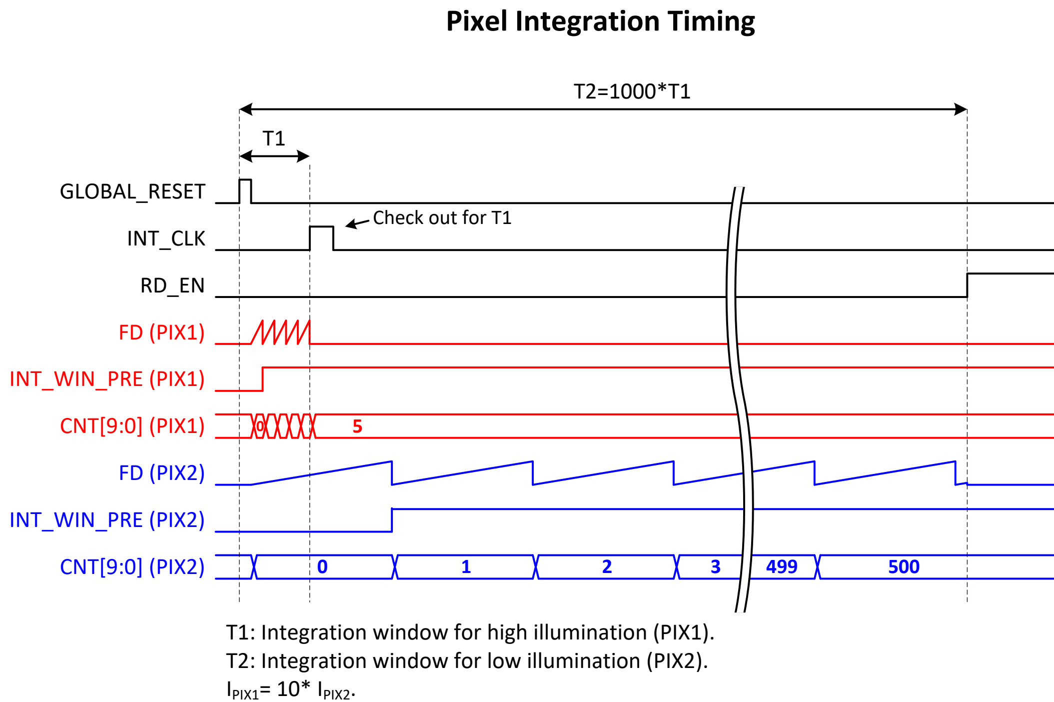


Figure 4-3: Timing Diagram of Pixel Integration Time

The technique allows to not only the sense the low-level illuminance pixels but also extend the dynamic range by 1000 for high illuminance pixels but still using a counter size of only 10 bits (as used in the above example). Hence the power consumption and size of the pixel is still very small but we can meet the wider dynamic range requirement. The circuit implementation of this technique has been detailed in the section 5.

4.5 DIGITAL CALIBRATION TO OVERCOME FIXED PATTER NOISE

As the integrating capacitor value and threshold voltage of the comparator changes from pixel to pixel, different counter values were observed over the Monte Carlo Analysis. This variation from the Pixel to Pixel is called fixed pattern noise. Its known as fixed pattern noise, because it doesn't change over time or the noise component which is not random in nature. Usually in the image sensors this fixed pattern noise is corrected by some form of Analog plus digital Calibration techniques. Here we propose a digital Calibration based on which the Fixed Pattern Noise can be reduced significantly.

Method: We provide a same reference (current) to all the pixels and capture the counter values across the pixels. Ideally, without the fixed pattern noise all the pixels digital counter value should be same but given that each pixel will have different comparator threshold voltage, and integrating capacitance, we will observe different values from pixel to pixel. Our calibration scheme works by storing all the pixels values in the memory. After we store the values, we take an average of all the pixels counter values and then run a calibration routine where we find out the variation in the counter value from the average value for each pixel and store that variation for each pixel. We don't need the original counter values now, so they can be removed from memory but we will need to store the original average counter value.

Once we have captured the variation in $\Delta(CV)$ across all the pixels then, we can use that information to calibrate the actual frequency points by scaling the variation to the ratio of the new counter value to the average of the reference current and subtracting

it from the actual point. Figure 4.4 is flow-chart of calibration routine currently implemented in excel for 96 pixels which will be implemented inside the DSP core or FPGA for an actual system. This calibration routine can be extended easily to an array of 256 x 256 or even larger depending upon the need.

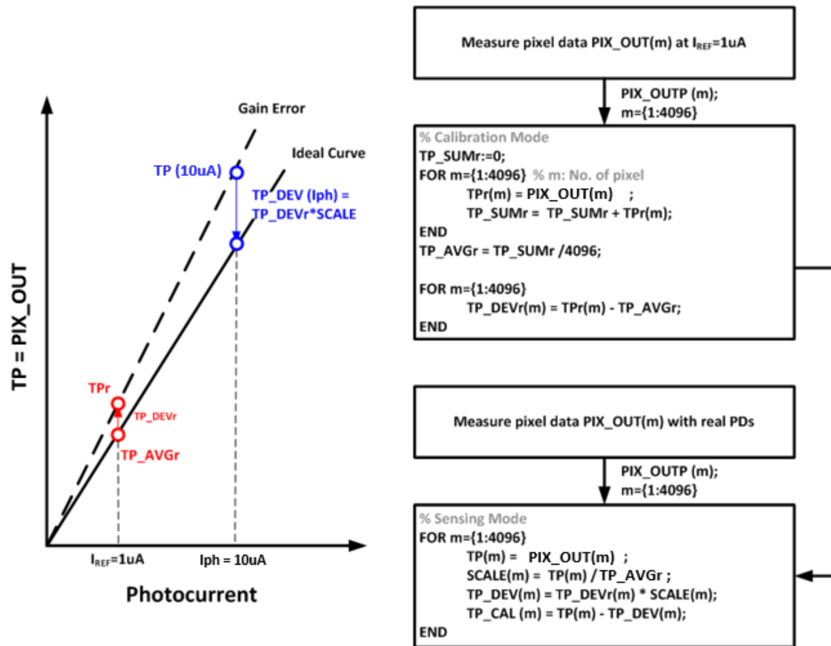


Figure 4-4: Digital Calibration Scheme Flow Chart

The further details on the implementation of the digital calibration scheme can be found in section 5 along with the simulation results. In the section 6 we have provided a rough estimate of the memory that will be required to run the calibration scheme for a 256 x 256 pixels array.

5. IMAGE SENSOR CIRCUIT DESIGN

5.1 TOP LEVEL ARCHITECTURE

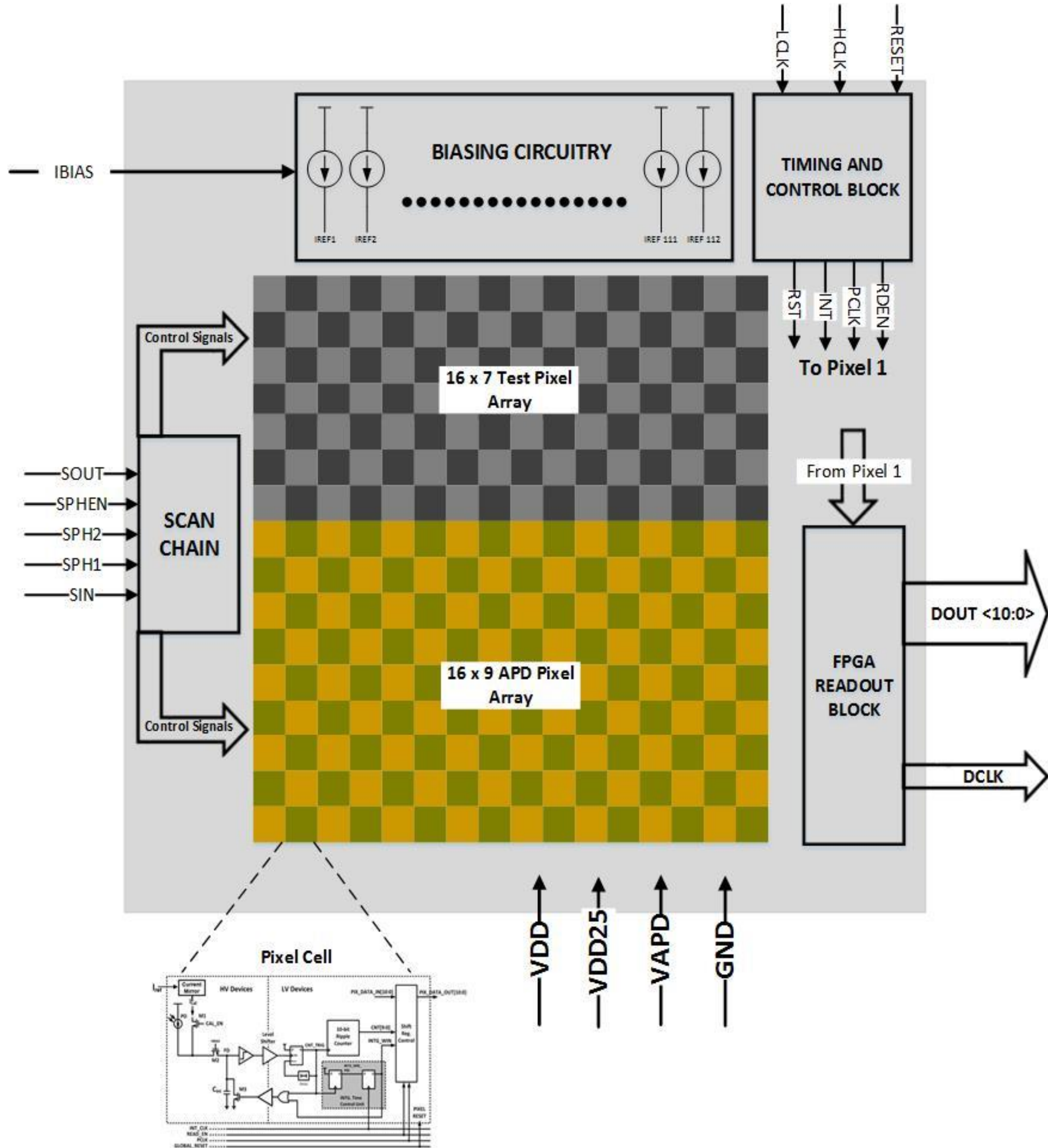


Figure 5-1: Top level Image Sensor Chip Architecture

Figure 5-1 details the block diagram of image sensor chip that we designed. For our chip, we have total 256 Pixels in a 16 x 16 Pixel array. Of these 16 x 7 Pixels (112 Pixels) are used for showing the electrical performances of the chip with the appropriate electrical test circuitries which can quantify the chip's electrical performance. The remaining 16 x 9 Pixels (144) have a photo-diode (APD) fabricated on chip inside them for the optical testing, for capturing the optical performance of the chip. This chip has been designed in TSMC 65 nm CMOS process.

Apart from the 16 x16 Pixel array, the other blocks inside the chip are Timing and Control Block which provides the required timing and control signals to the whole pixel array for integration, readout and dynamic integration window control etc. This block takes three inputs in the form of two clocks signals HCLK (High Clock Frequency), LCLK (Low Clock Frequency) and RESET. There is also a FPGA read-out block which interfaces the chip digital data with the FPGA, makes it compatible with it and provides the required clocking, sync and 11-bit parallel data to be read out by the FPGA. The output signals will need to be level shifted based on the FPGA requirements. There is also a SCAN Chain block which helps in providing a fixed register setting to the chip at the startup which are user controlled externally. We will discuss in detail each section of the chip along with the appropriate explanation.

5.2 PIXEL CELL

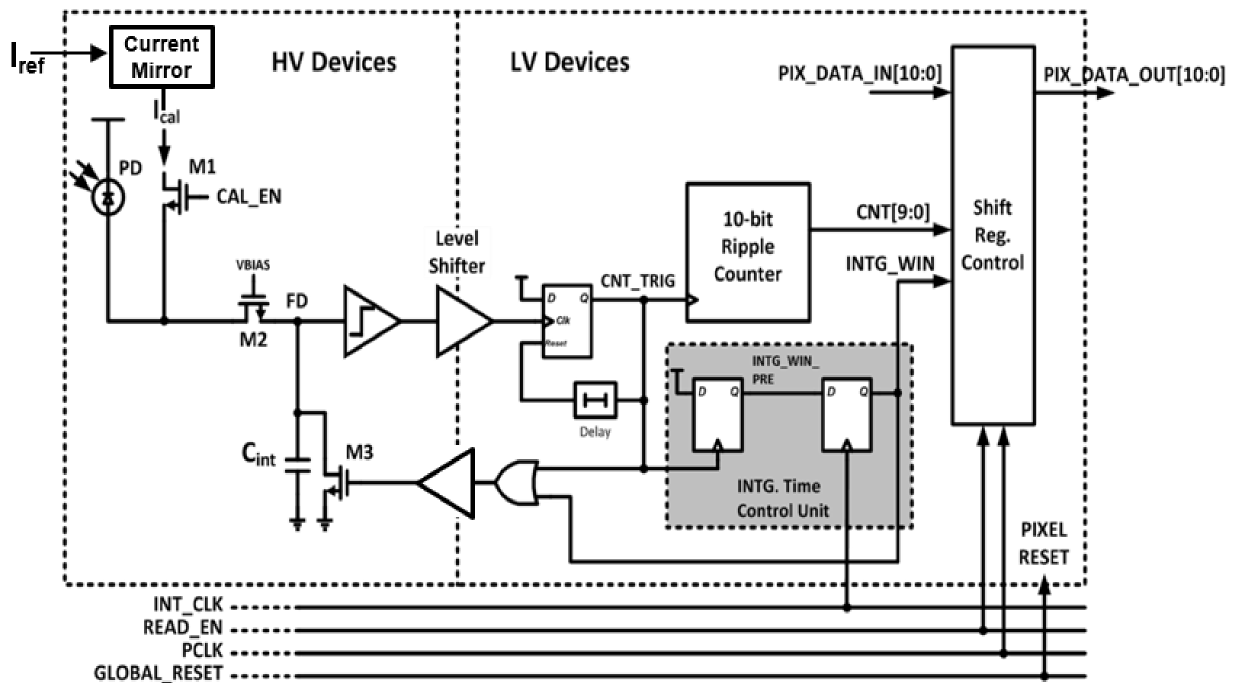


Figure 5-2: Pixel Cell

Fig. 5-2 depicts the internal circuit blocks of the unit pixel circuit that contains one infrared photodiode pixel (IR-PD), integration time control unit (ITCU) and the pixel-level ADC.

5.3 HV AND LV SECTIONS

The whole Pixel level ADC is divided into sections. One using 2.5 Volts HV (high voltage) devices and the other using minimum length transistors with 1.0 Volts LV (low voltage) devices. In the front end of the pixel, where the photo-diode current integrates onto the integration capacitor, the leakage current of the comparator, reset circuit and calibration circuit should be very low as we are going to be capturing very

small magnitudes of current (of the order of few pAs). During simulations, we found that in the minimum length devices which are available in 65nm CMOS, they have sufficiently large gate-drain, gate-source and drain to source leakage which was dumping the current onto the integrating cap even when there was no external excitation. This causes unnecessary trip of the counter even in the event there is not photo-diode current. Hence, we need to use the HV devices the front-end. These are all 2.5 Volts devices with 280nm Length and VT is larger as compare to the 65nm devices. Once the front-end operation is bit wise digitized by the comparator, we translate into the low voltage devices regime through a level shifter, this helps us in implementing the rest of the circuitry in the minimum length devices with lower supply voltage as compare to 2.5 Volts to save power and area.

5.4 DIGITAL CALIBRATION SCHEME DESIGN

As discussed previously in section 4.5, we have implemented a digital calibration scheme which helps in reducing the fixed pattern noise of the Pixel array. This is implemented using CAL_EN, PD_EN switches and the low voltage Cascode current mirror. To enable the calibration, CAL_EN is pulled high and PD_EN is pulled low. Once the appropriate switches are pulled low/high, the FD node start receiving the calibration current for integration rather than the PD current. Each pixel coverts the incoming calibration to the respective digital code and is readout during the FPGA readout mode. The pixel-pixel variations are captured through the variations in the digital code and calibration route is run in the post analysis to reduce the standard deviation. The important point to consider is that the digital calibration scheme relies on

the fact that we have a fixed calibration current source (I_{cal}) inside each pixel whose value shouldn't change from pixel to pixel. There are many possible ways to provide this calibration current inside each pixel but there is an important design consideration which needs to be kept in mind while implementing. As the FD node is connected to the I_{cal} current source through a MOSFET switch, any extra capacitive loading of the node supplying the calibration current will automatically load the integrating node (FD node) and will hinder the normal operation of the pixel (as the PVT variations of this parasitic capacitance will limit the performance of the digital calibration scheme). Therefore, we need to make sure that we reduce the loading of the node supplying the calibration current source. To ensure this, we must locally mirror the current inside the pixel so that routing parasitic to each pixel doesn't come into picture if a single current source is used to supply current to each pixel. But given that we would need to use a mirror locally inside each pixel, there will be fluctuations in the mirroring current from one pixel to another (because of mismatch, arbitrary fluctuations in the mirroring ratio from the pixel to pixel). To ensure that the random variation from pixel to pixel is small a large transistor (W x L) need to be selected so that the V_t mismatch in the mirrors can be reduced. But if the large transistor is placed right at the node supplying the calibration current, we will again load the FD node through the switch. Hence a low voltage Cascode has been used for this purpose with smaller M3 & M4 and larger M1 and M2 devices. Low- Voltage Cascode also has better mismatch performance as compare to simple current mirror and it also helps reduce the loading of the node by using very

small M3 and M4 devices. Please refer to the figure 5.3, showing the design of the low-voltage Cascode used for the mirroring.

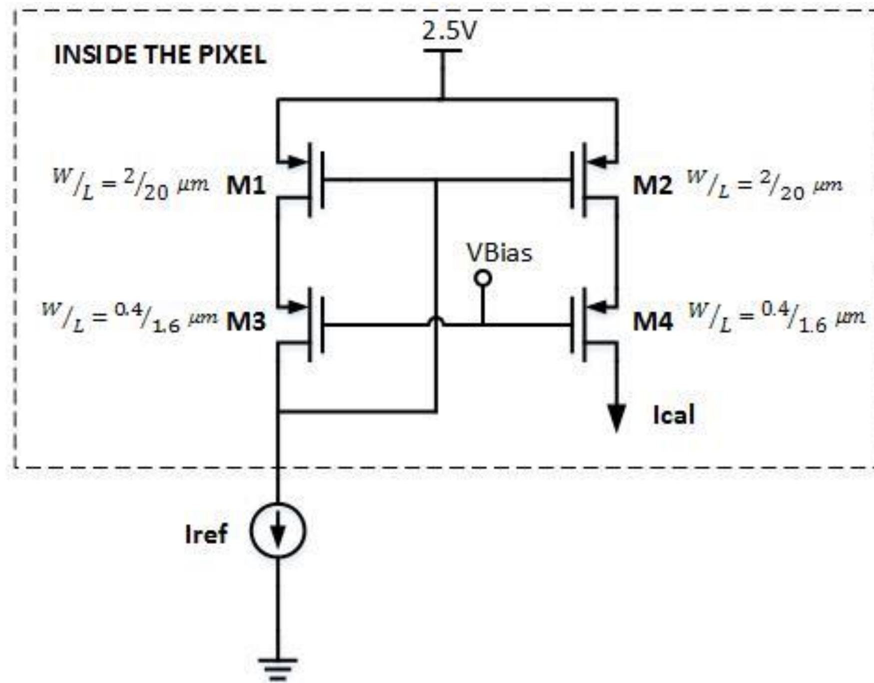


Figure 5-3: Low Voltage Cascode Current Mirror used for the Digital Calibration

To check the effectiveness of the digital calibration scheme, MONTE CARLO simulations were performed. As in the simulation test bench we didn't have actual photo-diodes and neither the optical setup. We used a calibration current of 1uA. We included the current mirror also in these simulations and the whole pixel front end to capture the effect of variations in the pixel. After capturing the pixels information with 1uA calibration current, we calibrated 2uA of excitation current (instead of PD current) across 100 pixels. Figure 5.4 shows the results that we received from this calibration.

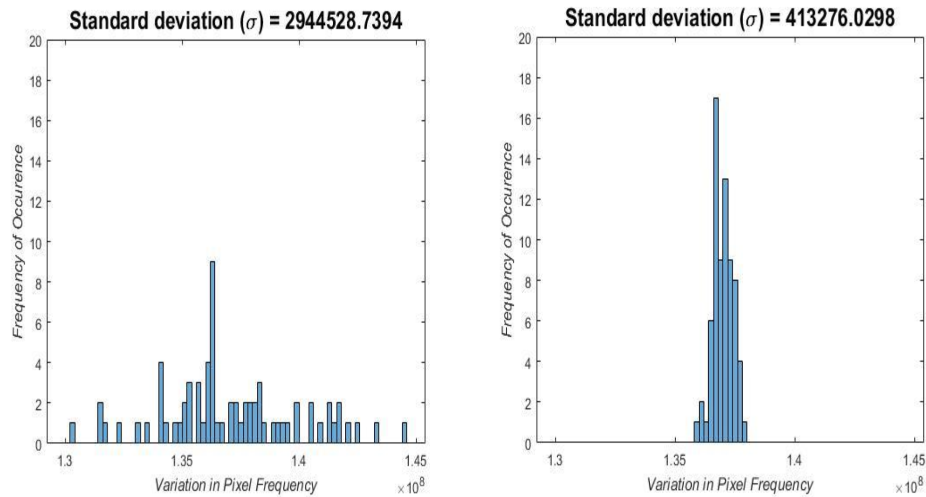


Figure 5-4: Standard Deviation of Un-calibrated and Calibrated Pixels

In the figure 5.4, graph on the left shows the standard deviation in the frequency obtained across all the pixels when 2uA was fed to each one of them. The average frequency value across the pixels is roughly 137 Mhz. Graph on the right side shows the standard deviation in the across after the calibration. So clearly, we can see that the standard deviation across the pixels which is observed to be roughly 2.15% before calibration has been cut-down to a factor of 0.3% which is about 86% improvement. To test this scheme in the actual chip scenario, we will be using in total 96 pixels where instead of the PD, a second excitation current of 2uA is generated along with the calibration current using the current mirrors instead of one as per the figure 5.5.

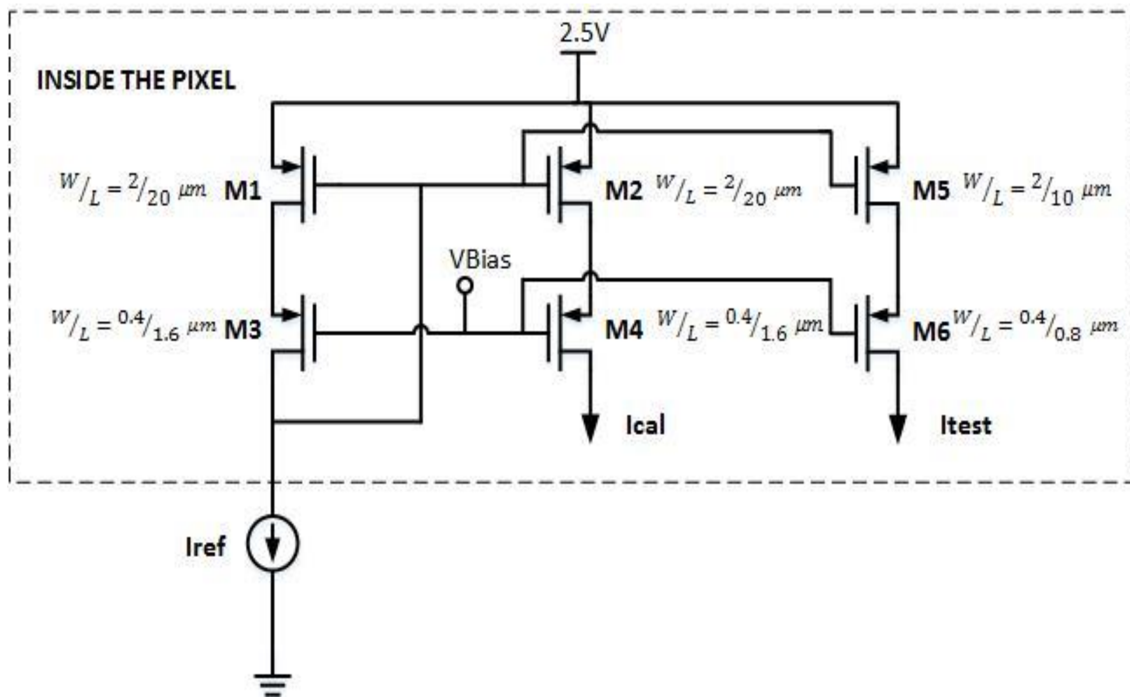


Figure 5-5: Pixels front end used for digital calibration

5.5 COMPARATOR DESIGN

As already discussed in the working operation of the pixel at the beginning of integration, the IR-PD captures photon energy and converts it into a photocurrent (Iph) that charges the integration capacitor (Cint) on floating node (FD). A pixel comparator is utilized to sense the voltage level of FD. Once the FD crosses the trip point of pixel comparator, it will trigger a pulse signal and reset FD through the reset device (M3). FD will recharge again till it crosses trip point and trigger the next reset pulse. Hence an Ultra-low power comparator is required inside each pixel to sense the trip point and therefore provide a pulse to the counter. The comparator design that we have implemented has four back-back CMOS inverters as shown in 5.6. [32] [33] The comparator's threshold level gets set by the first inverter, which is tunable using the

voltage transfer characteristics of the inverter which is controlled by the sizing of the transistors. The comparator's trip point is set as per the equation (1) [31] [33]

$$V_{th} = \frac{V_{dd} - |V_{tp}| + V_{tn}\sqrt{\frac{K_n}{K_p}}}{1+\sqrt{\frac{K_n}{K_p}}} \qquad (1)$$

Where V_{dd} is supply voltage used in the inverter, V_{th} is the threshold voltage of the comparator, K_p & K_n are the functions of mobility, size, and capacitance for PMOS and NMOS, respectively, V_{tp} and V_{tn} are the threshold voltages for the PMOS, NMOS transistors respectively [33].

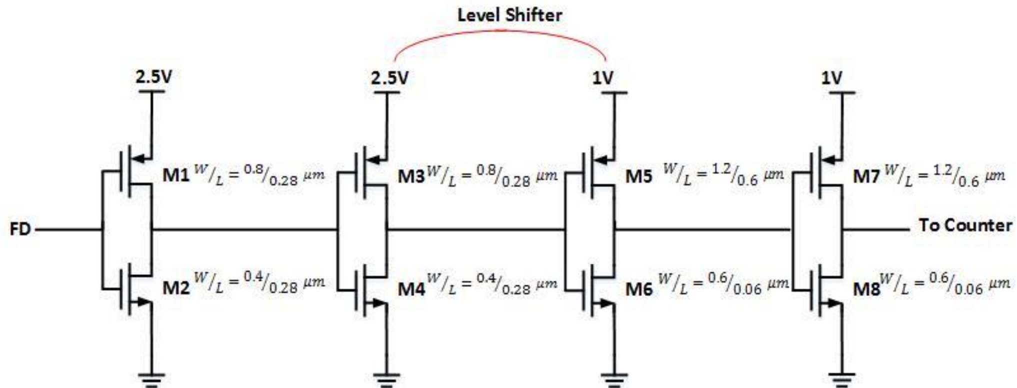


Figure 5-6: Comparator Design of four cascaded Inverters

Four inverters were planned for the design as they increase the comparator gain which helps in generating a sharp pulse each time the comparator trips. The second inverter design should ideally match the first stage so that the crossover point is maintained throughout. This assists in making the rising and falling of the pulse signal generated more symmetrical in nature. [33] [34]

The above comparator design has advantages, it's a very simple design and can operate with a very low conversion time (gate delays control the conversion time) as opposed to many others like static amplifier based designs, plus its doesn't consume any static current but only dynamic power which automatically scales with the frequency of operation. There are couple of disadvantages of the above designed comparator. Firstly, the comparators trip point V_{th} is prone to PVT variations, which will be calibrated by the digital calibration scheme implemented in the design. As per Eq. (1), the transistor's threshold voltage and mobility are dependent on temperature. Therefore, the threshold voltage also changes with temperature. A calibration scheme need to designed which can compensate for pixel-pixel variation at the power on. Also, the inverters are quite sensitive to the noise coming from power supply. This noise needs to be bypassed to ground using a big capacitor. [33] Now, the inverter delay is majorly a function of the device size. First inverter in the comparator chain loads the integration capacitor, hence first stage should not be very big. A minimum device size transistor is chosen for the first inverter. Now, as discussed earlier we would like to keep the dimensions for each subsequent inverter stage to be same, so that we can keep it symmetrical. This leads to a much simpler inverter delay control equation which can be tuned just by controlling the inverter supply and the length of the device used in inverter stage, the inverter delay when added together for this design comes out to be approximately 60 ps. [33] [35]

$$Inverter\ Delay \propto \frac{L^2}{V_{dd}} \quad (2)$$

Comparator generates a pulse of fixed width every-time it gets triggered which is further fed to the counter. The third stage in the comparator also acts as a bridge between

the high voltage and low voltage devices and performs level shifting operation from 2.5 Volts to 1Volts. This ensures that a seam less transition is observed in the regions.

5.6 RESET CIRCUITRY AND PULSE GENERATOR

Usually the counter requires a minimum pulse width to be applied before it can increment correctly. In our case for the counter design, this minimum pulse width was found to be around 200-240ps. Hence the pulse generated by the comparator can't be applied directly to the reset circuit because in that case, the comparator will trip back to being low within its propagation delay (~60ps) which is much lesser than what is required by the counter. Hence a delay needs to be introduced in the signal path in such a way, that a minimum pulse width of roughly 300ps (by keeping some safety margins) is being provided to the counter each time the comparator trips. This is done by the asynchronous set-reset flop. Each time the comparator trips, it generates a pulse which sets the D-Flipflop, which after passing through the multiple buffers delay resets the flip-flop back to low stage. This same pulse also keeps the pixel in reset stage and releases the reset as soon as the flip flop gets reset.

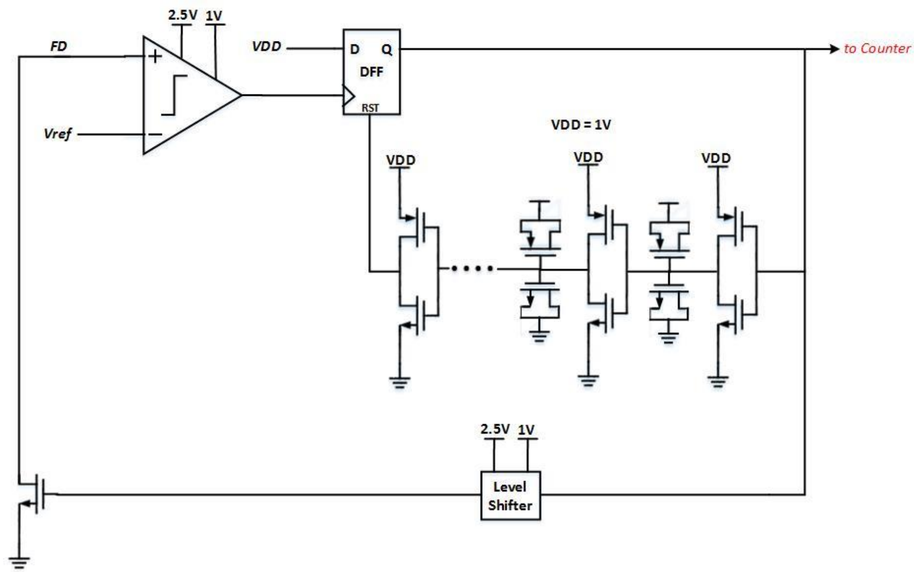


Figure 5-7: Fixed Pulse Generator and Reset Circuitry

5.7 INTEGRATION TIME CONTROL UNIT (ITCU)

The adaptive integration time control unit as discussed in section 4.4, helps us dynamically control the integration time based upon the received photo-current signal. This is implemented as shown in the figure 5.2 using a 1-b latch. It is utilized to latch value-1 once the trigger signal (CNT_TRIG) occurs which occurs when the comparator trips. The output of 1-b latch (INT_WIN_PRE) is checked at the end of T1 which is defined by the rising edge of INT_CLK. If INT_WIN_PRE- is 1 at end of T1, meaning that counter value is larger than zero, and T1 will be used as integration time. This also shuts down the further pixel integration and ensures that pixel value is intact till the integration time T2 is over and we readout the data. If INT_WIN_PRE- is 0 at end of T1, meaning the resolution is too low for the input signal, and the integration time is

extended to T2. Please refer to figure 5.8 for the timing diagram illustration of the Integration Time Control Unit.

The technique allows to not only the sense the low-level illuminance pixels but also extend the dynamic range by 1000 for high illuminance pixels. The occurrence of the INT_CLK is user dependent and can be externally controlled. All the pixels are readout together at the end of T2, independent of their integration time. This ensures that there is no discrepancy in the readout data. In the event if we are receiving the high intensity for all the pixels, it might be helpful to limit the integration time to just T1 and increase the frame rate to even few MHz's.

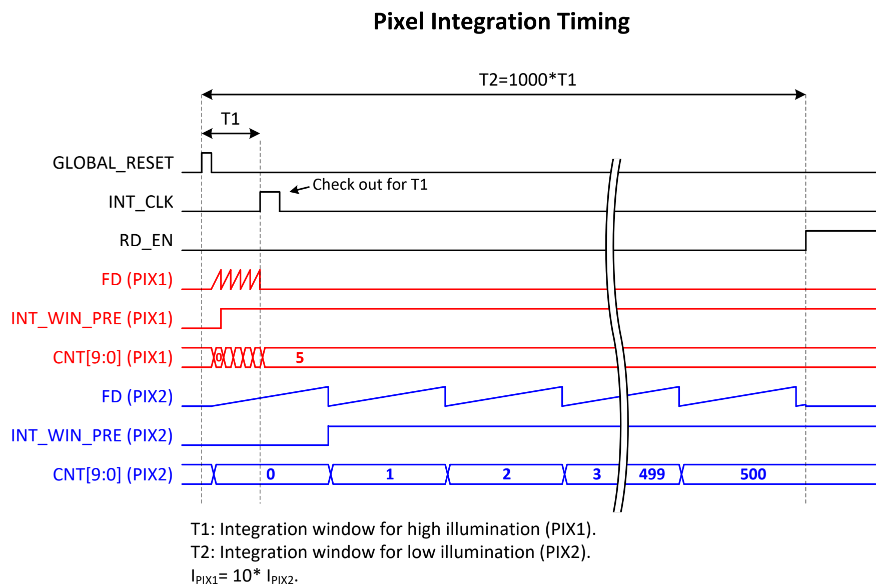


Figure 5-8: Pixel Integration Timing

5.8 COUNTER AND SHIFT REGISTER

For the counter design, 10-bit ripple counter is utilized to digitize the comparator tripping cycles. Each time the comparator trips, as we know the fixed pulse generator circuitry generates a pulse, whose rising-edge triggers the flip flop (DFF) which is basic unit cell of the shift register. To minimize the pixel circuitry, the counter is designed to support 10-bit rising counting and shift register readout scheme (Fig. 5.9) both at the same time. The same counter shifts to counting mode during integration and changes to shift register during data readout mode. To start counting mode, READ_EN is equal to 0. The 10-b DFFs are cascaded where the output Q_bar is feedback connect to input D, and the clock is triggered by the output Q of previous unit.

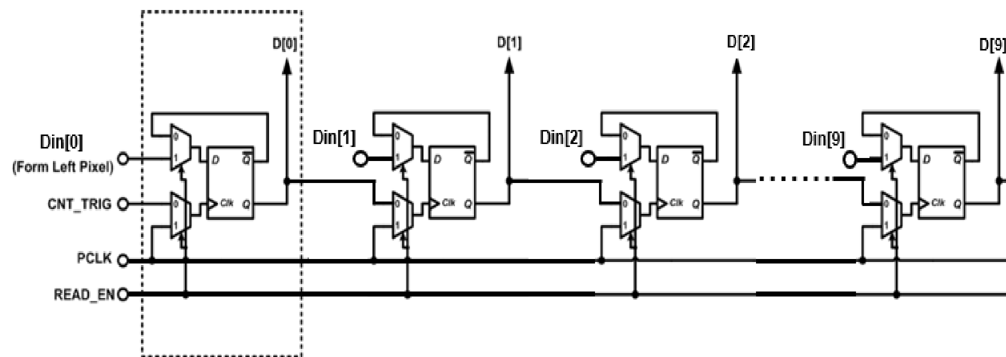


Figure 5-9: Counter and Shift Register

The counter gets triggered from the CNT_TRIG signal which is generated by the fixed pulse width generator. As the pixel integration time is over, circuits will enter readout-mode by connect READ_EN to 1. In readout-mode, the counter circuitry will be reconfigured as shift registers: all registers are synchronous with PCLK, and the input D

of all the flip flops is connected to the output Q of respective previous pixels. The overall shift register chain is connected from most left pixel to most right pixel so that the counting value can be transferred from pixel to pixel. As shown in Fig. 5.9, the 1-bit data from left-hand side pixel is shifted into the unit counter circuitry from Din, and shifted out to right-hand side pixel through Dout. All the pixels get connected in the series chain and at every rising edge of PCLK (pixel clock) starts shifting the data out. This is explained in detail along with the timing diagram in the next section. The Pixel clock can go as high as 10's of MHz depending upon the maximum driving strength of the CMOS driver and FPGA readout rate and related power consumption.

5.9 DATA READOUT MODE

In the data Readout mode, all the pixels get connected in series one after another. The figure 5.10 shows how the pixels gets connected to each other in this mode. The 11bit data (10-bit counter + 1-bit integration window output) from the last left pixel gets connected to the input of the right pixel. The data starts to shift out at the rising edge of the PCLK after the READ_EN goes high.

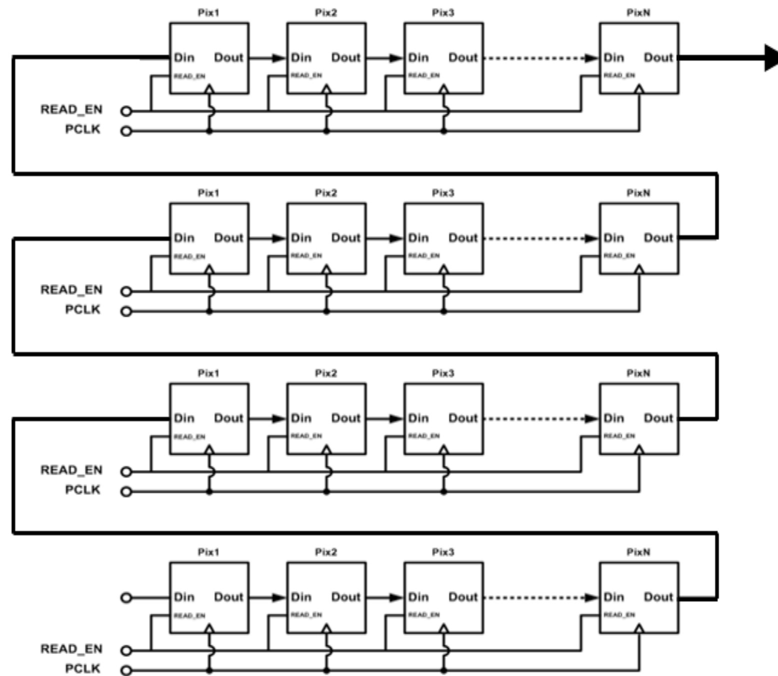


Figure 5-10: Pixel Configuration in Read-Out Mode

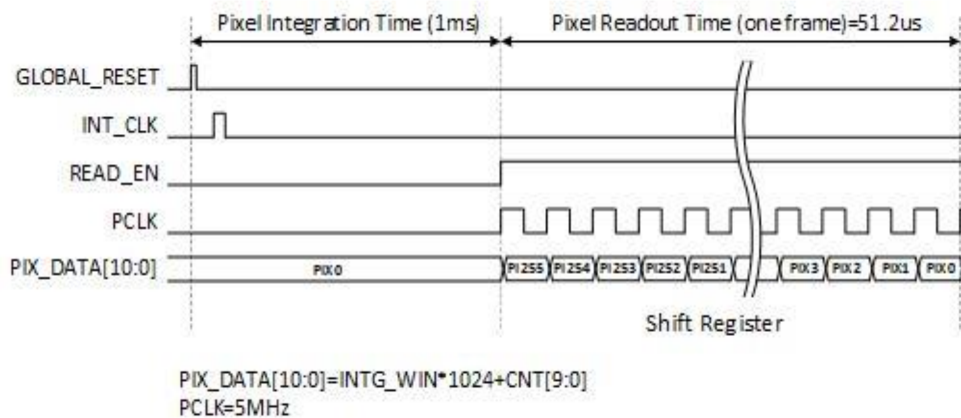


Figure 5-11: Pixel Readout Timing

Figure 5.11 gives the top-level pixel timing diagram. The frame rate for the sensor is given by the equation 3.

$$Frame\ Rate = \frac{1}{Integration\ Time\ (IT) + Readout\ Time\ (RT)} \qquad (3)$$

Let's say the maximum integration time we are targeting is 1ms and PCLK used to readout data has a rate of 5MHz. Then the frame rate will be given as below:

$$Readout\ Time\ (RT) = 256\ x\ 0.2\ us = 51.2us$$

$$Frame\ Rate\ (FR) = \frac{1}{1ms + 51.2\ us} = 950Hz$$

Therefore, the maximum Frame Rate possible with the above integration time comes out to be of the order of 950Hz. This can be certainly increased beyond this in the event we start with smaller integration time.

5.10 TIMING AND CONTROL BLOCK (TCBLK)

As shown in the figure 5.11 we would need four timing and control signal inside each pixel for the operation of the pixel. These signals are GLOBAL_RESET, INT_CLK, RD_EN and PCLK. Global Reset resets the pixel each time its triggered high and makes sure that once it is released the pixel starts the integration. INT CLK is the integration window control signal, which distinguishes between the high and low integration region and comes at a fixed time interval after the reset is released. RD_EN is the signal which when pulled high puts the pixel in the readout mode and pixel stops the integration. PCLK is the clock which is used to shift out the data from the pixels.

All the four signals in the chip are generated from two clocks. One is a high clock frequency (HCLK) and another is a lower clock frequency (LCLK). The lower

clock frequency is used to set the frame rate of the image sensor. At the rising edge of the LCLK, the device is reset.

Timing and control block generates the reset pulse for a fixed unit interval controlled by the delay cell in the feedback path of the flip flop. After the reset is pulled low, the pixel starts integration which continues until the INT_CLK is pulled high for the dynamic integration control. This is generated by the timing and control block with the help of reset signal and HCLK. A counter is incremented each time the HCLK is triggered and compared digitally in a comparator with the user input external count value. After the counter has incremented to the user input count value, the INT_CLK pulse is generated.

At the falling edge of the LCLK, RD_EN is enabled and shifts the chip from the Integration mode to Readout mode. This also defines the higher integration limit for the pixel. After the RD_EN is pulled high, pixel clock is also supplied along with it to serially shift the data out from the pixel array. A description of the implemented circuitry is shown in the figure 5.12

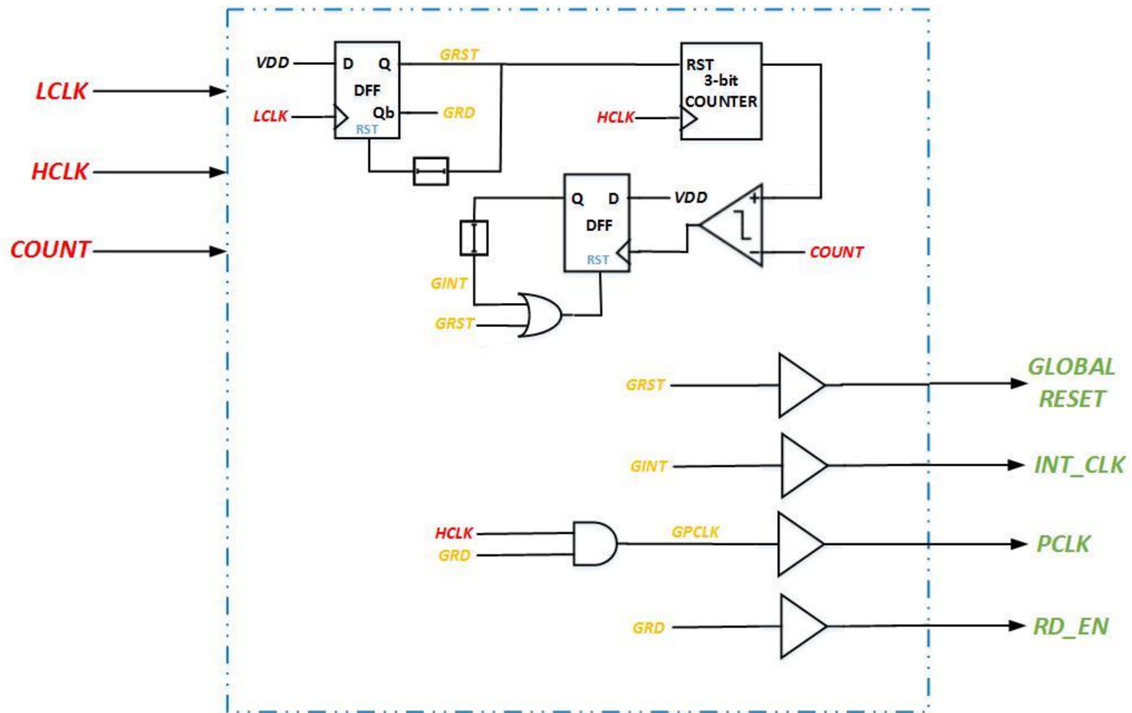


Figure 5-12: Timing and Control Block

This may not be the best way to implement the required timing and control signals, but it sufficed the need for our test chip. Typically, the LCLK and HCLK were of the range 100Hz – 15KHz whereas the HCLK from 500KHz – 15MHz.

5.11 TIMING AND CONTROL SIGNALS ROUTING

All the pixels need the four timing and control signals and their relative timing should not be disturbed. The first pixel receives the four timing and control signal directly from the timing and control blocks. It uses the four signals for its operation and buffers them out for the next pixel. This trend is continued down till the last pixel. The present pixel uses the timing and control signals and buffers them out to the next pixel. In this manner, the four signals are never overly loaded by routing and placement plus

their relative timing mismatch is also considerably lesser, it is of the order of magnitude 10's of ps which doesn't impact the performance and fixed pattern noise of the pixels. The figure 5.13 shows how the above methodology is implemented in the pixel array.

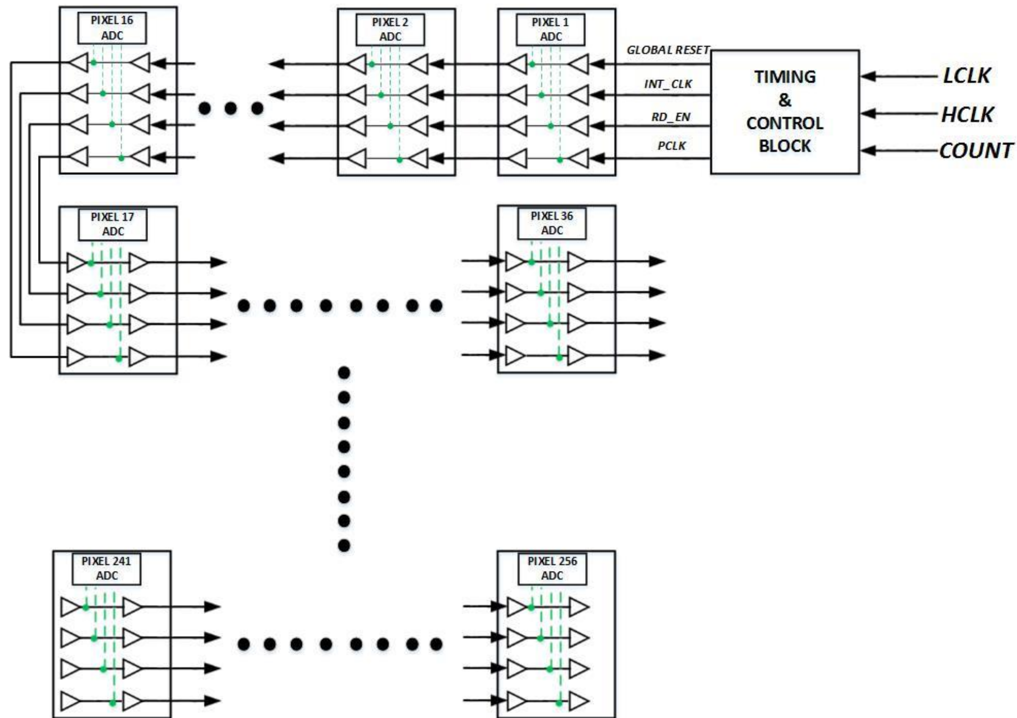


Figure 5-13: Routing of Timing and Control Signals

5.12 FPGA READOUT BLOCK

The serial data coming out of the pixels goes to the FPGA Readout Block which re-samples the data again with the falling edge of Pixel Clock to make sure that the data is well aligned with the clock. It also outputs a buffer copy of the last flip flop sampling clock which can be used by the FPGA to sample the incoming data. The FPGA Readout block also features a test-mode where it outputs a fixed pattern of 2047 (decimal)

followed by 0 at each edge of PCLK. This test-mode helps in interfacing the FPGA readout block with the FPGA and to remove any wiring phase delay etc. Please refer to figure 5.15 which shows the implementation of the FPGA readout block.

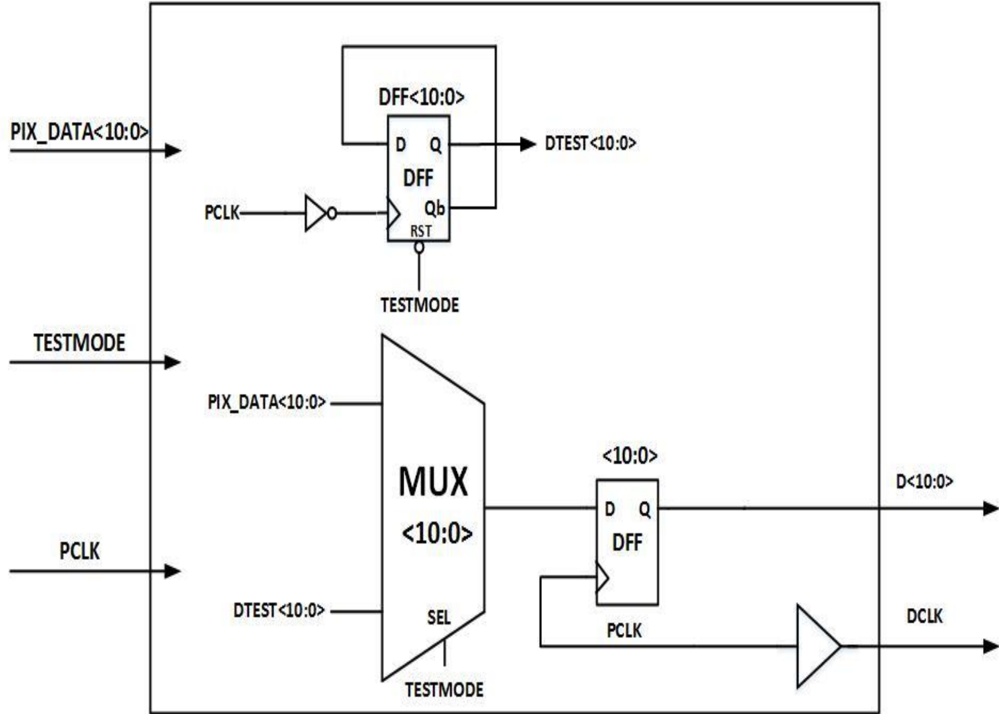


Figure 5-14: FPGA Readout Block

6. EXPERIMENTAL RESULTS

6.1 IMAGE SENSOR SOC DESIGN

The figure 6.1 portrays the photo micrograph of the designed imaging solution SoC (System on Chip). The chip has in total 256 Pixel (16 x 16 Pixel Array). Out of which the first 6 rows of pixels (in total 16 x 6 pixels) are for showing the performance of digital calibration. The next 16 pixels (one row) are the test pixels for showing the electrical performance and remaining 9 rows of 16x9 pixels (144 pixels) are with APDs and for measuring the optical performance. The chip also has timing and control block, scan chain, de-coupling capacitors on all the supply lanes, input/output buffers on all the input/output pads and the biasing circuitry. The chip has in total 36 pads and has dimension of 1.04mm x 1.04mm.

The die was bonded using ball bonding with a 5mm x 5mm QFN40 package. Figure 6.2 shows the picture of bonded die in the QFN40 packages. The extra 4 pads in the package apart from the 36 used in the chip were shorted to the GND. A PCB board was designed to test the SoC with all the required other devices. After the packaging and bonding, the chip was assembled onto the Sensor PCB board for testing in the lab. The chip requires two power supplies of 1V (for the smaller channel length devices) , 2.5 Volts (for long channel length devices) and one more for APD which can range anywhere from 2.5-6 Volts for their operation (we are yet sure of the supply requirements for APDs)

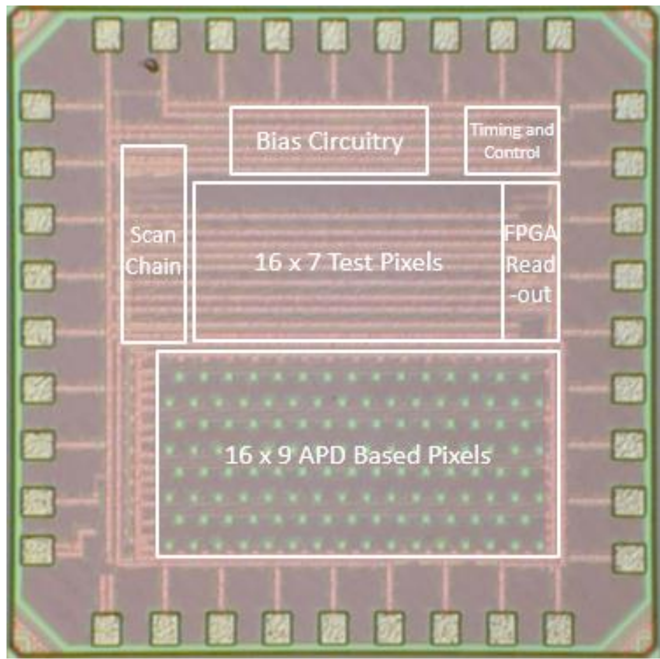


Figure 6-1: Image Sensor SoC Micrograph

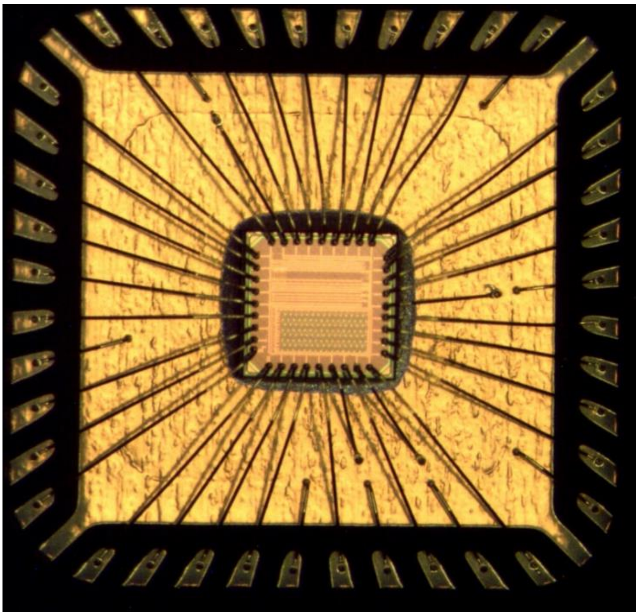


Figure 6-2: Bonded Image Sensor Chip Micrograph

6.2 LAB SETUP FOR TESTING THE CHIP

The chip is powered from the DC bias board which provides all the necessary supply outputs and biasing current for the bias circuitry. The chip also requires two clock signals named as LCLK and HCLK. The LCLK is a low frequency 1V CMOS level square wave signal. The frequency of the signal can range anywhere from few 100Hz's to 15-20KHz. The HCLK is a high frequency 1V CMOS level square wave signal. The frequency for the HCLK can range anywhere from 100KHz to 20-25 MHz's. The digital data coming out from the chip passes through a level shifter and is read through the ML605 (Virtex-6) evaluation board. Chip-scope is used inside the ISE Design Suite to read the incoming data and store it. Figure 6.3 shows how the above setup is done in the lab.

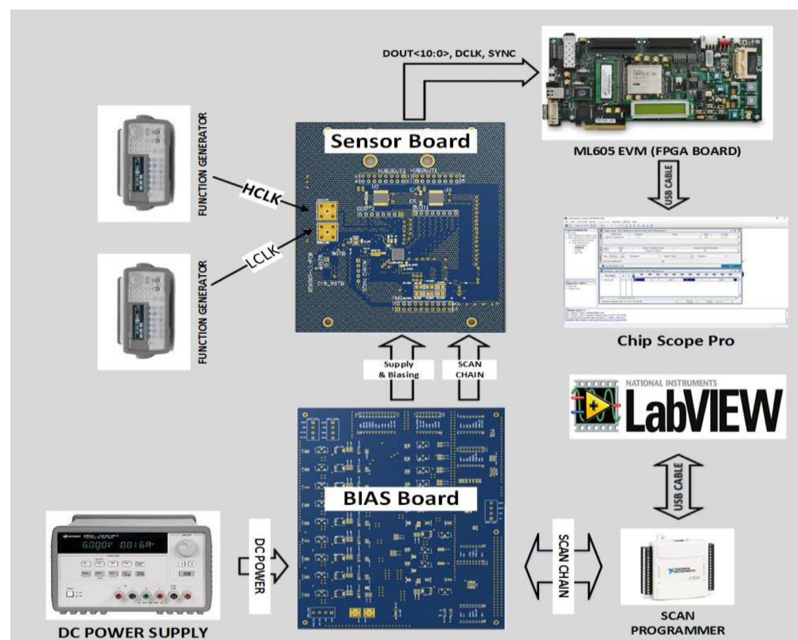


Figure 6-3: Lab Setup for testing the performance Chip

6.3 DYNAMIC RANGE TESTING

There are total 14 test pixels inside the chip which are used for dynamic range measurements. A bias current of 10uA flows inside the chip which after passing through the bias circuitry produces 1uA reference current for each of the test pixel. Test Pixels internally have current Mirrors which can both multiply this current and in parallel also divide the reference current to be measured by the chip. A Frame rate of 250Hz (LCLK frequency) and Readout rate of 2MHz (HCLK frequency) was used to capture the dynamic range performance.

$$Frame\ Rate\ \ (FR) = 250Hz$$
$$Frame\ Read\ Time = 4ms$$
$$Larger\ Integration\ Time\ Window = 2ms$$
$$Readout\ Clock\ Rate = 2MHz$$
$$Smaller\ Integration\ Time\ Window = 2us$$

The smaller integration time window has been set to 1000 times smaller than the larger integration time. This ensures that we have divided down the total integration time into two regions as previously discussed. Table 6.1ists down the digital code received from the chip corresponding to the different currents which were fed to the ADC inside each pixel. The table has total 15 values. We have linearly scaled down the last value to the digital code of 1 to receive the full dynamic range that sensor can support with the above conditions.

Table 6-1: Test Current vs. Digital Code

Digital Code Obtained From FPGA	Current	20-bit Scaled Digital Code (if Digital Code >1024) then (Code-1024) *1024
1	7.7505E-12	1
31	2.4027E-10	31
45	3.4877E-10	45
66	5.1153E-10	66
130	1.0076E-09	130
1026	1.5873E-08	2048
1028	3.1746E-08	4096
1032	6.3492E-08	8192
1039	1.1905E-07	15360
1110	6.8254E-07	88064
1150	1.00E-06	129024
1245	2.00E-06	226304
1427	4.00E-06	412672
1746	1.00E-05	739328
2011	2.00E-05	1010688

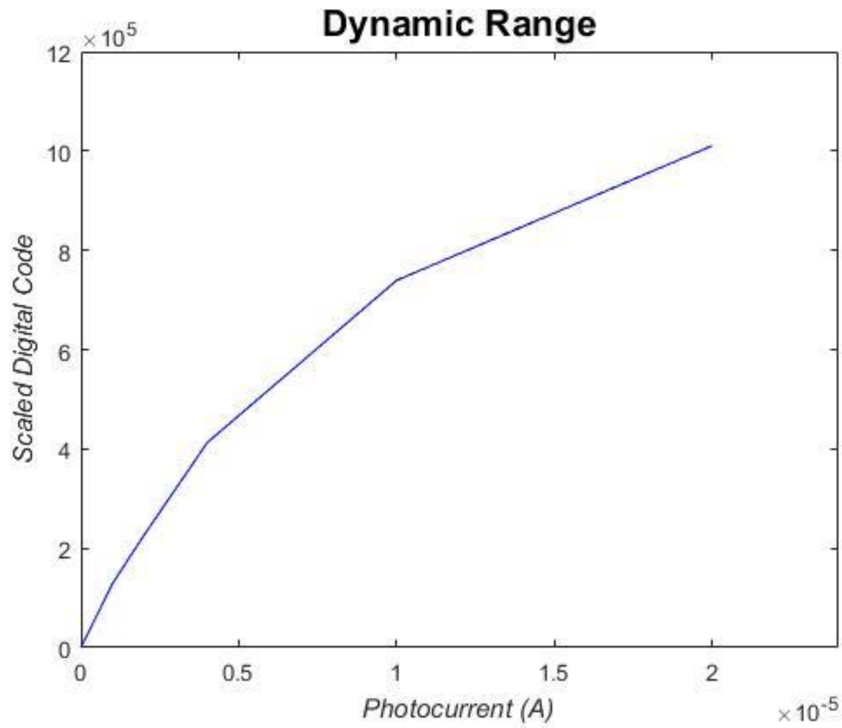


Figure 6-4: 20-bit scaled Digital Code vs. Test Current

$$Dynamic\ Range = 20 \times \log \frac{I_{max}}{I_{min}}$$
$$= 20 \times \log \frac{2 \times e^{-5}}{7.75 \times e^{-12}} = 128.75dB$$

Hence, the total dynamic range achieved with the design is about 128.75dB. This can be extended further by changing the lower and the higher clock frequency.

6.4 DIGITAL CALIBRATION TESTING

In our chip there are total 96 pixels for testing the performance of the digital calibration. We supply the required 10uA bias current to the chip from the DC board and internally to each pixel two reference current of 1uA and 2uA are generated inside each pixel. Firstly, the digital code values are captured across the 96 pixels with 1uA

reference current and then with 2uA. The digital codes captured with the first reference current are used to calibrate the second reference current. Figure 6.5 shows the variation in the code value obtained without 2uA current without calibration across the 96 pixels. The average Code Value is 807. The standard deviation obtained is 11.456 codes across all the pixels. This is 1.42% variation in the code value.

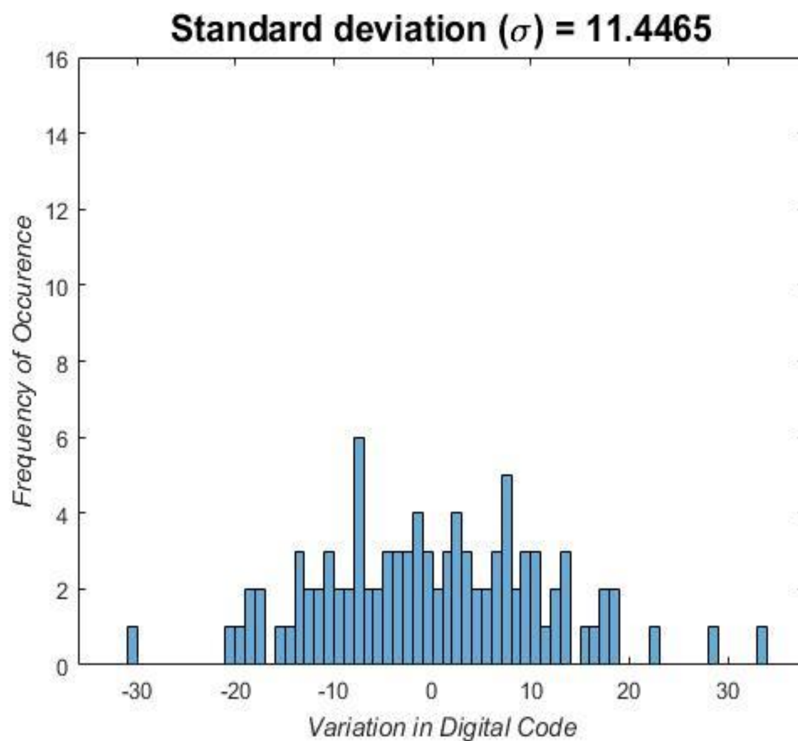


Figure 6-5: Standard deviation in the code value before calibration

After this the pixels are calibrated using the reference current information we have captured at 1uA. Figure 6.6 shows the standard deviation in the code obtained after calibration. The average code value after the calibration is still 807, and the standard deviation is reduced to 3 codes which is 0.38% of the actual code value. The original

standard deviation has been cut down by a factor of 4 and roughly an improvement of 75%

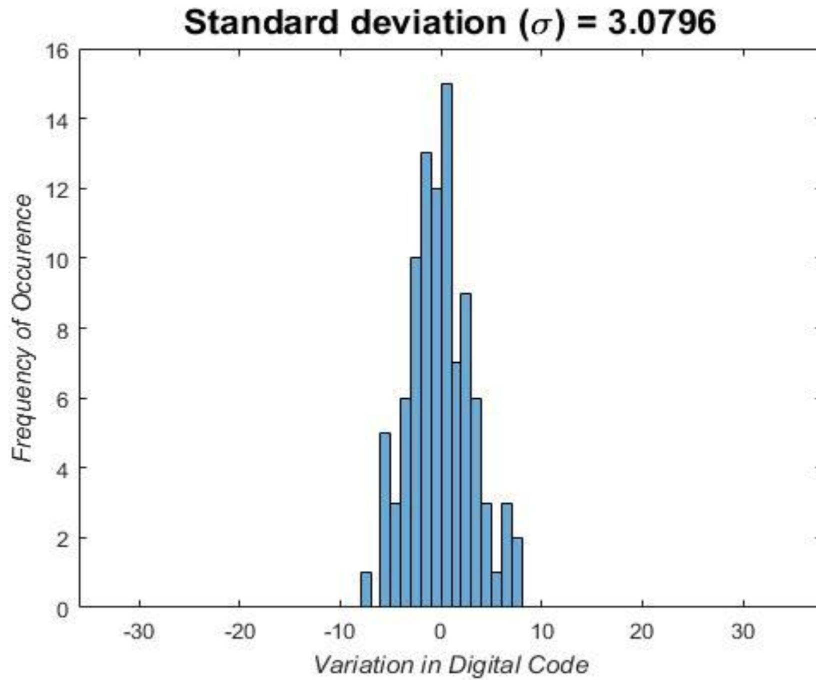


Figure 6-6: Standard deviation in the code value after calibration

We also tested the calibration scheme for 54 pixels (the middle ones) by removing the corner pixels of the top, bottom and side pixels. The assumption here is that the layout environment observed by the middle pixels should be more common as compare to the corner pixels. Figure 6.6 shows the standard deviation in the code obtained for just 54 pixels. The standard deviation is about 2.89 codes which is roughly 0.357% of the code value.

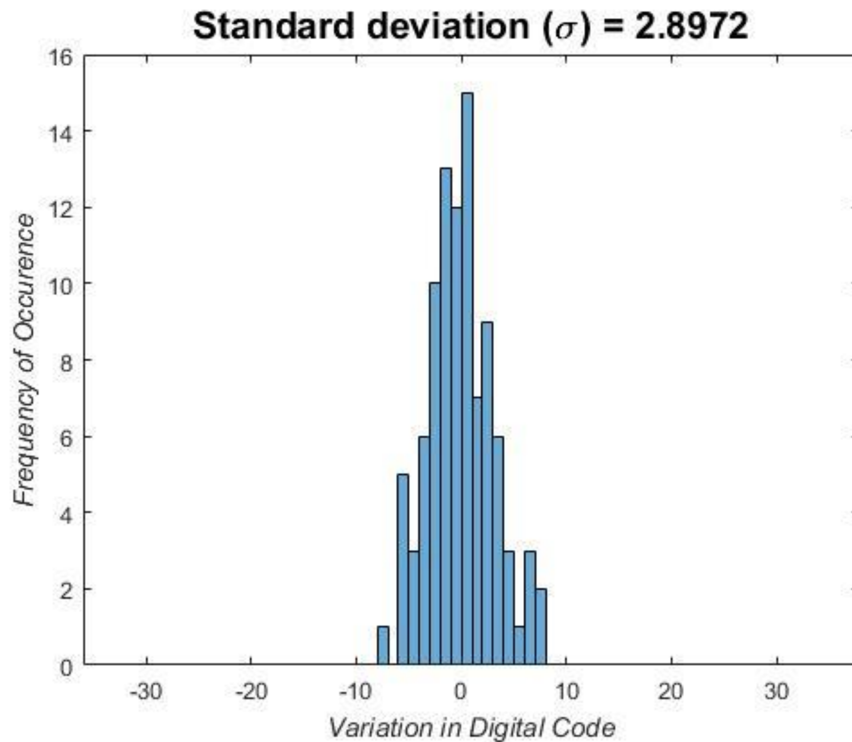


Figure 6-7: Standard deviation in the code value after calibration for 54 Pixels

Therefore, there is not a huge difference between the standard deviation of 54 and 96 Pixels. After this we ran digital calibration for all the 1023 codes (1-1023) to see if our scheme works for all the digital codes and the performance that we can achieve. Figure 6.7 shows the standard deviation in the code value before and after calibration for all the 1023 codes. It seems that our calibration scheme maintains its performance across the 1023 codes and can cut down the variation by a factor 3-4.5 across all the codes. The calibration schemes require a certain memory size for its implementation to store the value of the variation across the pixels. For a pixel array of 256 x 256, the memory size should be of the order of 450kbits.

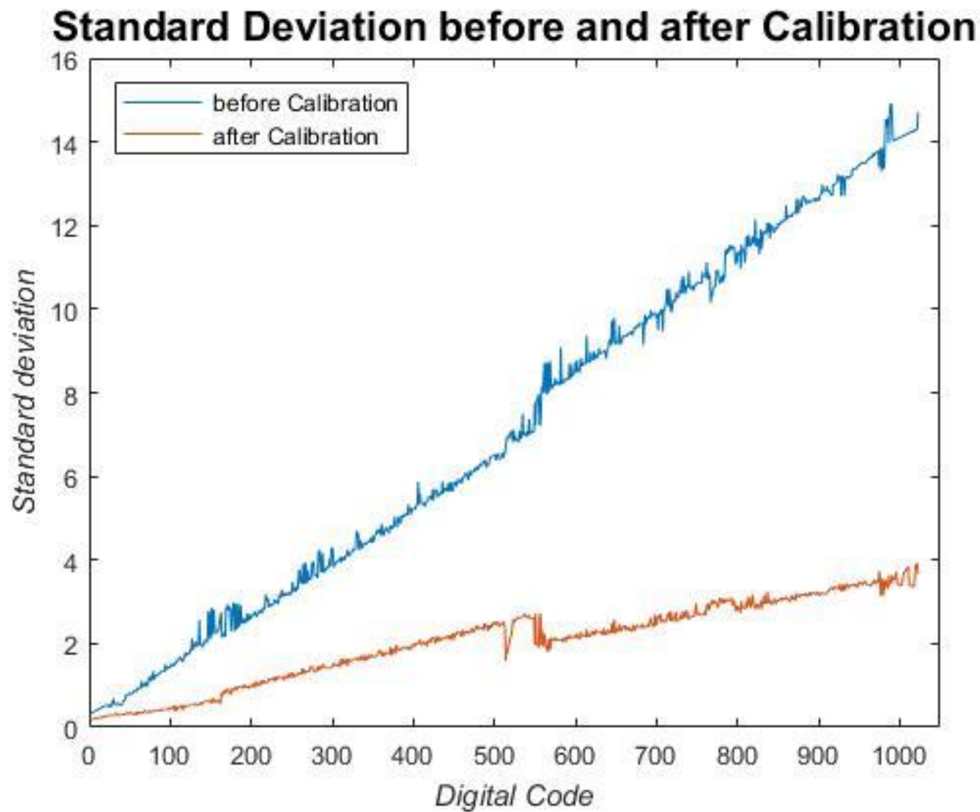


Figure 6-8: Standard deviation in the code value across the 96 pixels before and after the calibration for all the 1023 code values.

6.5 LINEARITY TESTING

The linearity performance of the pixel ADC is measured using the non-linearity parameters of Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). For the first test pixel the integration time window is swept from 2us – 16ms in steps of 2us, this let the pixel pass through all the 1024 codes and thereby the measure the linearity performance. Figure 6.8 shows the linearity plot of the pixel digital output code with the pixel integration time. Figure 6.9 and Figure 6.10 shows the DNL and INL observed

over the length of digital codes. The maximum DNL is 0.65 LSB and INL is 1.65 LSB over the complete length of 1024 codes.

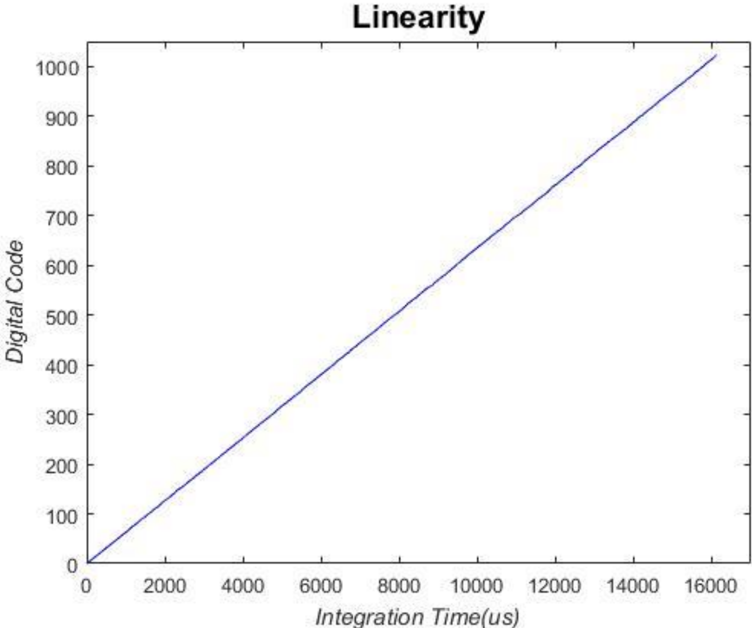


Figure 6-9: Digital Code vs. Integration Time (us)

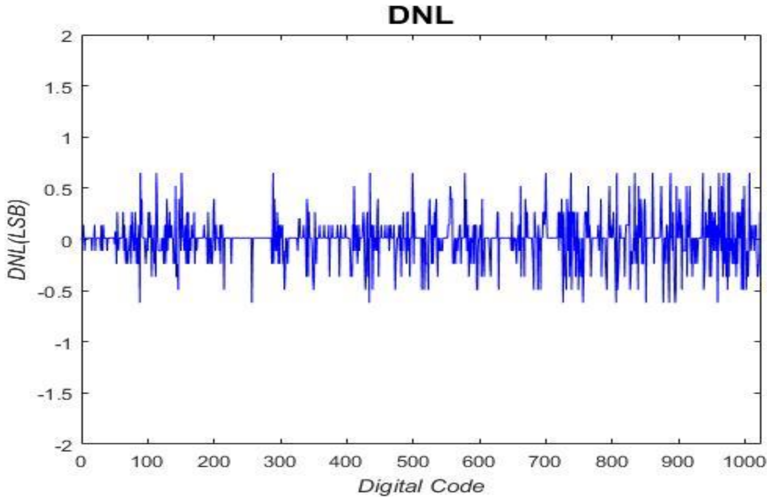


Figure 6-10: DNL (LSB's) vs. Digital Code

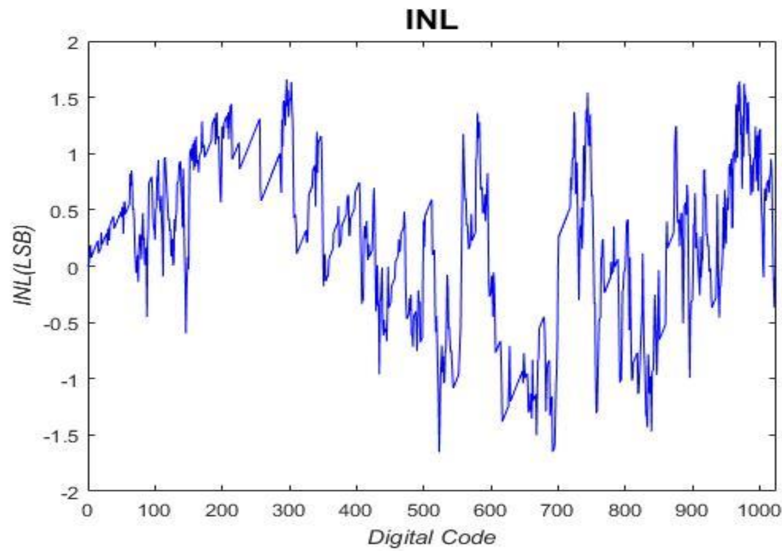


Figure 6-11: INL (LSB's) vs. Digital Code

Table 6-2: Performance comparison against the latest references

Specification	Ref [39]	Ref [40]	Ref [41]	Ref [42]	This work
ROIC Type	Analog	Analog	Digital	Digital	Digital
Detector Type	LWIR	LWIR	SWIR-LWIR	SWIR-LWIR	NIR/ CMOS
Technology Node	350nm	600nm	90nm	90nm	65nm
Frame Rate	NA	NA	Not tested	10KHz	10KHz
Maximum Readout Speed	2MHz	5MHz	NA	NA	20MHz
Format	32 x 4	576 x 6	256 x 256	256 x 256	16 x 16
Pixel Pitch	30um x 30um	56um x 43um	30um x 30um	30um x 30um	30um x 30um
Dynamic Range (dB)	77	79	100	112	128
Power Consumption (uW/pixel)	781	28.93	1.22	0.9	0.58

7. SUMMARY AND CONCLUSION

`Certainly DROIC (Digital Read-out Integrated Circuit) based image sensor implemented in the thesis has a lot more advantages over the traditional analog and digital architectures. It can overcome the fundamental limitations of lower side and higher side photo current integration limits due to much higher well capacity and easily extend the dynamic range as displayed in this case well over 125dB. The design achieves a very low power consumption of about 0.58uW/pixel as compared to the other reference designs, mainly because of the novel dynamic integration control technique implemented in the design. The power consumption is reduced because of two main reasons. Firstly, if the photocurrent is higher, the integration is automatically switched off after a fixed duration and, it also lets us use a much smaller counter size (of only 10 bits + 1-bit of integration control). There was Fixed Pattern Noise observed from one pixel to another owing to variation in the front-end comparator gain, threshold and offset, and the integration capacitor. This was compensated in the digital domain with gain and offset correction. We have implemented a digital calibration scheme in the post processing mode which cuts down the standard deviation (of the pixel-pixel variation) by almost 75%. The imager also shows a good linearity performance of 0.65LSB/1.65LSB DNL/INL respectively. All the circuits were implemented in 65nm TSMC CMOS technology process node. The lower process node helps us push the readout frequency to as high as 20MHz (the last tested frequency). Overall, the imaging

solution proposed has shown very promising performance and should serve the emerging needs of infrared and visible sensing applications.

Future work involves testing of the APDs implemented in the design and verifying their performance across the six folds of optical signal's intensity given to the APDs. This involves de-encapsulation of the chip's QFN package to remove the lid from the top of the chip so that light can fall on the APDs. Then PCB should be mounted on the optical test-bench, and it needs to be fed with the intensity varying light source through an optical lens (for focusing the light), and showcase that we are able to capture that wide dynamic range using the imaging solution.

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