POWER MANAGEMENT CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

A Dissertation

by

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ABSTRACT

Energy harvesting is the process of converting ambient available energy into usable electrical energy. Multiple types of sources are can be used to harness environmental energy: solar cells, kinetic transducers, thermal energy, and electromagnetic waves.

This dissertation proposal focuses on the design of high efficiency, ultra-low power, power management units for DC energy harvesting sources. New architectures and design techniques are introduced to achieve high efficiency and performance while achieving maximum power extraction from the sources. The first part of the dissertation focuses on the application of inductive switching regulators and their use in energy harvesting applications. The second implements capacitive switching regulators to minimize the use of external components and present a minimal footprint solution for energy harvesting power management. Analysis and theoretical background for all switching regulators and linear regulators are described in detail.

Both solutions demonstrate how low power, high efficiency design allows for a self-sustaining, operational device which can tackle the two main concerns for energy harvesting: maximum power extraction and voltage regulation. Furthermore, a practical demonstration with an Internet of Things type node is tested and positive results shown by a fully powered device from harvested energy. All systems were designed, implemented and tested to demonstrate proof-of-concept prototypes.

DEDICATION

Para mis padres Salvador y Marisa, cuyo apoyo y ejemplo me han fortalecido cuando lo necesitaba.

Para mi esposa Pilar, que estuvo conmigo todo el camino sin yo darme cuenta.

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CHAPTER I

INTRODUCTION

Energy harvesting

As power demands continue to grow for integrated solutions, new ways to extend device lifetime must be developed to maintain high energy dense solutions plausible. And even though battery technology has shown unprecedented growth and application [1, 2], compact solutions with limited area real-estate still show lagging power when compared to transistor power density [3]. Fig. 1 shows a comparison between battery power density improvements over the course of 20 years compared to the processing power of integrated solution over the same time frame.

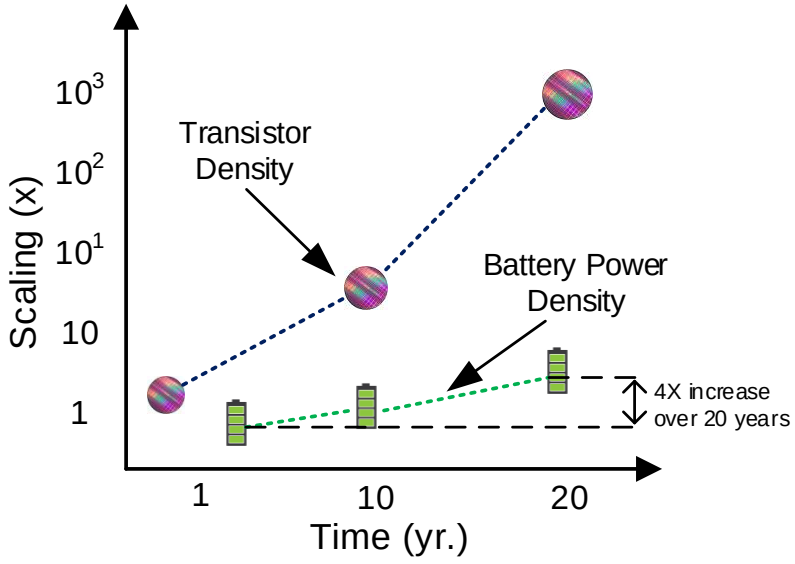

Fig. 1. Power density comparison of battery density improvement over time vs. processing power density improvement over time.

As the figure shows, battery technology deeply lags behind processing power, and there is only a 2X improvement shown every 10 years [4].

This leads to a very real need to enhance battery life for small, portable applications in order to allow wireless sensor technologies a real shot of being implemented. Among the possible solutions to enhance operational lifetime, or even disregard the need for battery technology all-together, of wireless sensors is energy harvesting. Energy harvesting is the process of scavenging energy that is readily and freely available in the environment, into electrical energy [5, 6]. Similar to large scale energy farms seen with photovoltaic solar cells, energy harvesting targets the available energy in one form to convert to electrical and utilize it to power small devices/systems.

The only difference lies in the scale of the targeted power to be harvested. Whereas macro-harvesting systems are related to energy conversion in the range of kilowatts to Megawatts, energy harvesting is limited to harvesting power in the range of nanowatts to milliwatts. Even at these low power levels, much can be accomplished through smart, low-power electronic design through the implementation of environmental sensors [7], healthcare monitoring nodes [8], and data networking for large-scale operations [9].

Applications and need for power management

Applications such as Wireless sensor nodes (WSN) or Internet of Things (IoT) [10-12] arrangements allows for a distributed approach to power consumption duties. Whereas several nodes in a mesh configuration may perform the sensing operation of the

network, only a select few of nodes within the mesh hold the responsibility of transmitting the power over long distances to the central processing unit [12]. These types of approaches focus more on delegating responsibilities and lightening the load on a single node, redistributing it throughout the network. Alternate approaches focus on dealing with power limited designs through intelligent package transmission [13-15]. These methods limit packet size transmission to minimize the use of the system power amplifier (PA), which is the most power hungry and inefficient block in transmitter circuits. Efforts on efficiently utilizing power resources can be extended further by employing energy harvesting technology. Utilizing energy harvesting technology is not without its own caveats: the possible power to be harvested is limited to both amount and availability. TABLE 1 shows the power densities per area/volume for commonly used energy harvesting sources.

TABLE 1. Energy harvesting estimates in μW per unit of area [16].

ENERGY SOURCE	HARVESTED POWER
Kinetic Vibration	
Human	10s of $\mu Ws/cm^2$
Industrial setting	100s of $\mu Ws/cm^2$
Temperature Gradient	
Human	10s of $\mu Ws/cm^2$
Industrial setting	10s of mWs/cm^2
Light	
Human	10s of $\mu Ws/cm^2$
Industrial setting	10s of mWs/cm^2
Radiofrequency	
GSM	100s of nWs/cm^2
AM	10s of pWs/cm^2
Wi-Fi	1000s of pWs/cm^2
Biomass (MFCs)	
240 mL (air)	600 μW

All available power densities from EH sources in TABLE 1, go from 10s of mWs and below. These power densities would be available for sensor applications if the implemented systems in charge of the power conversion were 100% efficient, which is never the case. The power converter's own energy consumption and losses are the main limitations in delivering all of the available power to the load. Current research efforts are being done on both ends, improved EH transducers and high efficiency power converters.

Due to both the limitation and variability of the power sources in energy harvesting, a power management units (PMU) are required to store and utilize the harvested energy in the best way possible. As shown in Fig. 2, the PMU extracts power from the EH source and delivers an adequate voltage level to the subsequent blocks in the wireless sensor node.

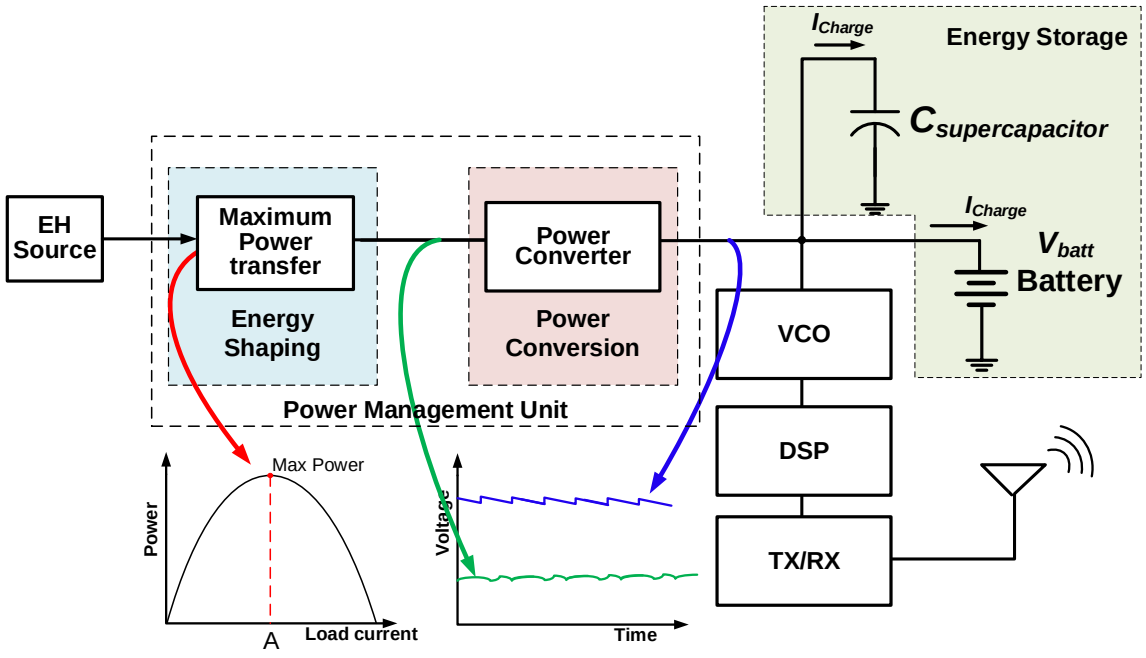

Fig. 2. Overview of wireless sensor node with power management unit highlighted.

The two main blocks which make up the PMU are shown: the Energy Shaping block and the Power Conversion block. The Energy Shaping block is in charge of extracting maximum power from the source in order to enhance efficiency and avoid any additional strain on the PMU when harvesting from low power scenarios. The Power Conversion's duties are to take the maximum available power and efficiently convert it to the required voltage rating required by the system. This can be performed through up-conversion [17], rectification [18], down-conversion [19] or a combination of several of the aforementioned techniques [20]. Fig. 2 highlights the operation of both blocks with the colored lines. Red shows the maximum power transfer operation from the Energy Shaping block allowing maximum energy to be extracted from the source. Green and

Blue show the input and output voltages of the Power Conversion block. An up-conversion operation takes place increasing the available voltage at the input to workable voltage levels for the later sensor nodes (VCO, DSP and TX/RX blocks), as well as delivering charging current to the battery on board.

The remainder of the chapter will focus on the principle of operation of the EH sources, as well as the available power converter blocks found in literature and application.

Energy harvesting sources

Harvesting energy from multiple different natural phenomena, be it thermal, solar, kinetic, or electromagnetic waves; require specialized transducers capable of harnessing and converting one type of energy to another. This section will delve into the fundamental operation of the currently available transducers which are used in EH applications.

Thermoelectric generators

Heat loss is a common occurrence in mostly all mechanical and electrical systems used worldwide. Be it from vehicle waste heat to geothermal underground sources, it is one of the most prevalent sources of potential untapped power today. Thermoelectric generators focus on converting temperature gradients into electrical energy through three different thermoelectric effects: the Seebeck effect, the Peltier effect, and the Thomson Effect. Each one of these effects takes advantage of the surrounding natural temperature gradient through materials special properties.

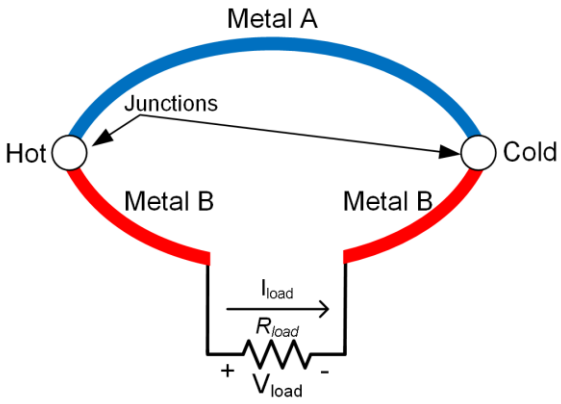

Fig. 3. Seebeck effect principle between two different metals.

The Seebeck effect is described as the phenomena which occur when two dissimilar metals or semiconductors are joined together and a temperate difference across their junctions is applied.

Fig. 3 shows the Seebeck effect principle and the generated voltage (V_{load}) from the temperature difference across the junctions of Metal A and Metal B. This leads to a voltage dependent on the temperature difference across the junctions given by:

$$V_{load} = \alpha_{AB} \Delta T \tag{1}$$

where the variables α_{AB} and ΔT are the Seebeck coefficient and temperature difference between hot and cold junctions, respectively. As shown in (1), the Seebeck coefficient for a particular pair of metals can be extracted from the voltage difference across the junctions over a variety of temperatures the surfaces may be subjected to. The units for α_{AB} are defined as $V \cdot K^{-1}$, and can achieve both positive or negative coefficient values.

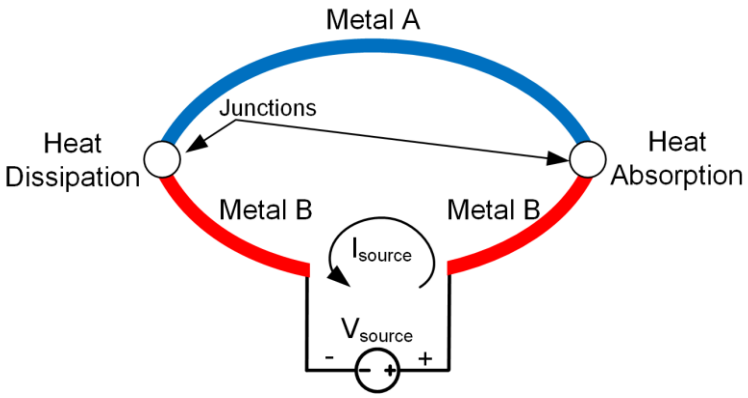

Fig. 4. Peltier effect principle through applied voltage source.

Usual ranges can vary in the tens of $\mu V \cdot K^{-1}$ for metals and metal alloys, and showing values up to $mV \cdot K^{-1}$ in semiconductors [21]. The Peltier effect is somewhat of a reverse Seebeck effect, in that a voltage is applied to the metal junction configuration and a heat absorption and heat dissipation phenomena will occur at the junctions of the metals. Fig. 4 shows how the junctions dissipate or absorb heat due to the applied V_{source} voltage. The heating and cooling effect depend on the polarity of the voltage applied, and may reverse the effects of cooling or heating if V_{source} were to be reconnected in reverse polarity.

The amount of heat removed by the junctions is given by:

$$Q = \pi_{AB} \cdot I_{source} \tag{2}$$

where Q is heat transferred by conduction from the system, π_{AB} the Peltier coefficient between the two metals A and B, and I_{source} is the electrical current in the circuit.

As with the Seebeck coefficient, the Peltier coefficient (π_{AB}) depends on the materials used in the junctions and amount of current flowing through the junctions. The unit for the π_{AB} is given by $W \cdot I^{-1}$, equivalent to volts. Thermoelectric generators used under the Peltier mode operate as cooling systems.

Finally, the Thomson Effect takes into account the thermal properties of a single metal with no junctions, subjected to varying temperatures across its terminals as well as a current established by an external voltage source. This causes the metal to absorb or dissipate heat. Fig. 5 shows the manner in which the Thomson effect causes absorption or dissipation of heat over a single type of material.

The amount of heat which the absorbed or dissipated is given by the following equation:

$$Q = \beta \cdot I_{source} \cdot \Delta T \tag{3}$$

where β is the Thomson coefficient and the units defined for it are $W \cdot I^{-1}K^{-1}$. Under sufficiently high temperatures, thermoelectric generators can begin to see the effects of the Thomson coefficient.

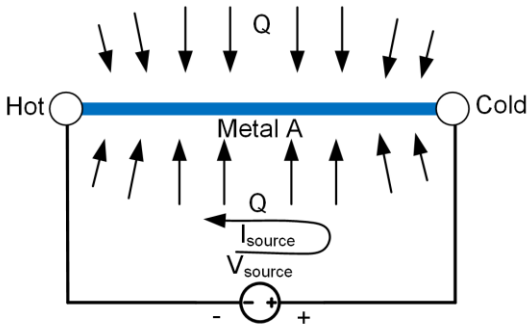

Fig. 5. Thomson effect showing absorption or dissipation by a single type of material with both temperature difference and current passed through it.

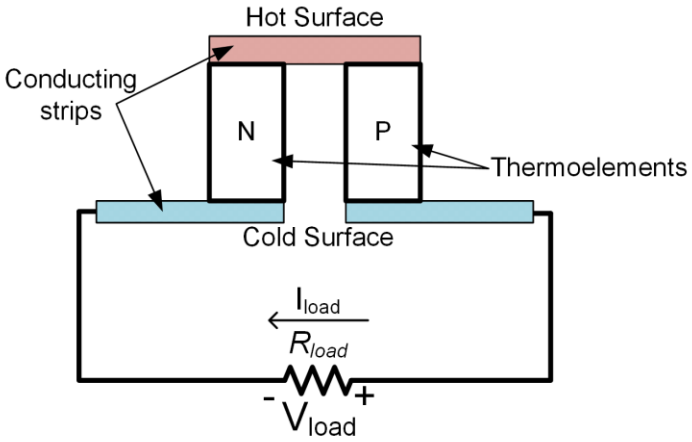

Fig. 6. Basic TEG building block consisting of n- and p-type semiconductor elements.

Due to the fact that most semiconductor materials are nonconductile crystalline solids, thermocouple implementations are difficult to implement. Rather than using intrinsic semiconductor materials, doped semiconductors are implemented in order to perform the thermocouple structure. Fig. 6 shows the N- and P-type materials connected in series through conducting strips (performed through aluminum or copper connections), and being subjected to a temperature gradient akin to the structure shown in Fig. 3.

The building block shown in Fig. 6 serves as the foundation over which the Thermoelectric generator (TEG) module is constructed. The TEG module is comprised of a matrix of unit building blocks to enhance the conversion efficiency and power output of the device. Both power output and conversion efficiency are decisive parameters in the TEG module performance. In order to correctly assess the capabilities of a TEG module, a figure of merit has been developed for device parameters:

$$Z = \frac{\alpha_{np}^2}{R \cdot K} \tag{4}$$

where α_{np}, R, and K are the material properties coefficient, interface properties value, and geometrical influence. If an assumption can be made in which the n- and p- type materials both possess similar values for electrical resistivity ($\rho_n = \rho_p$), similar thermal conductivity ($\lambda_n = \lambda_p$), opposite Seebeck coefficients ($\alpha_n = -\alpha_p$), and identical ratio of cross-section lengths to area, the TEG figure of merit (Z) can be simplified to:

$$Z = \frac{\alpha^2 \cdot \sigma}{\lambda} \tag{5}$$

where σ is electrical conductivity ($1/\rho$). The unit for Z is K^{-1}. From (4) and (5) it can be seen that in order for large values of Z to be available, two materials with individual values of high Z are needed, as well as opposite Seebeck coefficients.

Since the value of Z is K^{-1}, a dimensionless figure of merit would be $Z \cdot T$. The plot in Fig. 7 shows the figure of merit for a number of different thermoelectric materials currently available. As can be seen, the figure of merit for Bismuth Telluride (Bi_2Te_3) reaches approximately unity at 300 K, making it a suitable material for room temperature applications.

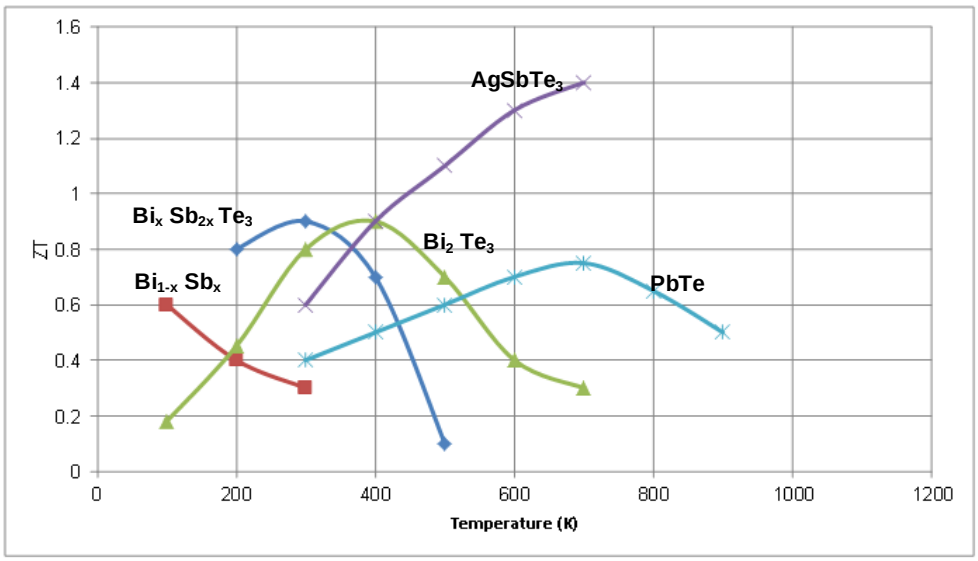

Fig. 7. Figure of merit (ZT) for current TEG materials (Adapted with permission from Ref. [22]).

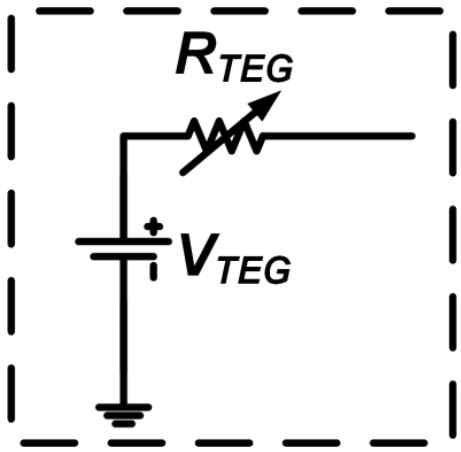

Fig. 8. TEG module's electrical equivalent.

Finally, as the TEG module will interact with electrical circuits there is a need for an electrical equivalent with which the design of the power management can be performed.

Fig. 8 shows that the TEG module may be modeled as a battery, where the voltage is proportional to the Seebeck voltage of the material ($V_{TEG} = \alpha_{np}\Delta T$), and the series resistance, R_{TEG}, is given by the total series resistances of the N- and P-type materials. Chapter III will delve into the design of power conditioning circuits which take both the Seebeck voltage and internal resistance deeply into consideration.

Photovoltaic cells

Among the more ubiquitous power sources used in energy harvesting technology are the photovoltaic solar cells. The conversion of light energy to electrical energy was first developed into silicon through a photovoltaic cell in 1954 in Bell Labs. Ever since this breakthrough, more and more development in these cells towards higher conversion efficiency has been the key parameter for this technologies push into mainstream applications. The photovoltaic cells operating principle comes down to semiconductor basics: electron-hole pair generation through light absorption, charge carrier separation and extraction of charge carriers through an electrical circuit.

As photons in sunlight hit the photoconductive material and are absorbed, electrons are knocked loose from their respective atoms and flow to produce a current.

This phenomenon only momentarily increases the semiconductor's conductivity, but over time the semiconductor returns to its previous state with the electron losing its energy recombining into a hole. Single doped type materials are functional photodetectors; in order to allow for light to produce electricity in usable quantities, a p-n junction semiconductor with separate electrons in the conduction band and holes in the valence band are required. Due to the structure of the photoconductive material p-n junction, comprised of silicon, the minimum amount of energy required for the electrons to come loose from the valence band must be greater than that of the bandgap energy [21]. This electron jumps to the conduction band allowing free movement in the crystal lattice, leaving behind a hole in the valence band. Fig. 9 shows the band-diagram of a p-n junction shows this occurrence.

This hole left in the valence band by the energized electron, causes other electrons to move into this new hole position; propagating holes throughout the lattice by diffusion.

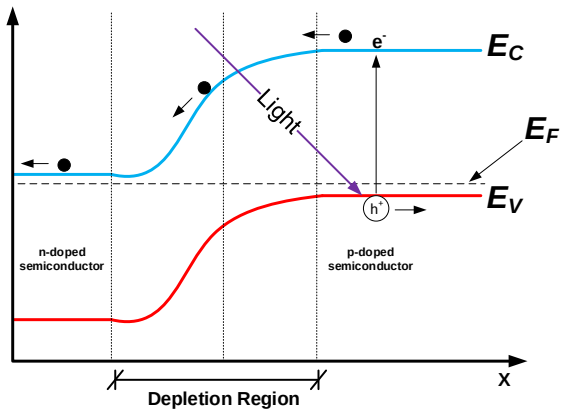

Fig. 9. Band diagram of p-n junction showing diffusion directions and electron drift.

Due to the power density of the solar light, this process occurs in greatly high numbers, allowing for current to be extracted from the p-n junction. As more and more electrons are pushed toward the conduction band of the junction, a depletion region begins to form and drift of carriers leads to an equilibrium within the junction. The depletion region also ends ups forming an electrostatic field and a built-in voltage across the junction.

The building up of charge on either side of the junction creates a diode like operation, promoting charge flow. This leads to the generation of the equivalent model for the photovoltaic cell [22] as shown in Fig. 10.

The model describes the light dependent operation by modeling the current delivering capability of the cell through photogeneration current source, I_{PV}, in parallel with a diode D_{PV}. Shunt and series resistances are also added, R_{sh} and R_s, to take into account non-idealities of the cell.

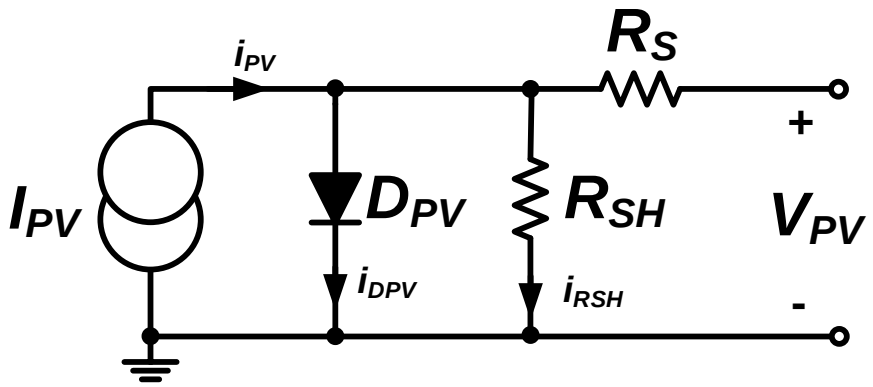

Fig. 10. Equivalent circuit of photovoltaic cell.

From Fig. 10, we can see that the amount of current available at the output node of the cell (V_{PV}), is limited by the diode current and shunt resistors.

$$i_S = i_{PV} - i_{DPV} - i_{RSH} \tag{6}$$

where I_S is the total output current, I_{PV} is the current produced by the illuminated current source, I_{DPV} the diode current, and I_{RSH} the shunt resistor current. Both the diode and shut resistor currents may be quantified through:

$$i_{DPV} = I_0\left(e^{\frac{qV_{be}}{nkT}-1}\right) \tag{7}$$

$$i_{RSH} = \frac{V_{be}}{R_{SH}} \tag{8}$$

where I_0 is the reverse saturation current, q the elementary charge of an electron, V_{be} voltage across the p-n junction (diode), n diode ideality factor, k Boltzmann's constant, and T the absolute temperature in K.

Assuming a small valued series resistor R_s, the overall output current to be expressed as:

$$i_s = i_{PV} - I_0\left(e^{\frac{qV_{be}}{nkT}-1}\right) - \frac{V_{be}}{R_{SH}} \tag{9}$$

All of these variables depend on size, but mostly material. As photovoltaic cells have been around for over 50 years, multiple different types of materials and configurations have been researched [21]. Configurations ranging from single-junction to multiple-junction silicon photovoltaic cells [23] have allowed for increased conversion efficiencies and application specific deployment, i.e. space solar harvesting.

Silicon in different presentations has been widely explored and has shown multiple breakthroughs throughout the years.

While silicon has been the predominant and cheapest implementation for photovoltaic cells, new materials such as Cadmium Telluride and Copper indium Gallium Selenide have also shown promise [24, 25]. TABLE 2 shows the overall efficiencies of current solar harvesting technologies [26].

Chapter VI in this dissertation will present a solution to harvesting maximum power for small photovoltaic cells aimed at low-power, wireless sensor node applications.

TABLE 2. Solar efficiency tables for multiple photovoltaic cell materials

Maximum Conversion Efficiency % for multiple Photovoltaic cell technologies	
Mono Crystalline Silicon	26.0%
Multi Crystalline Silicon	21.1%
CdTe	18.0%
Organic Solar Cells	10.0%
CIGS	20.1%

Radiofrequency harvesting

The capability of transferring power wirelessly has been a goal which has been aimed for since the beginning of electrical power. Pioneers such as Nikola Tesla envisioned the transmission of electrical power wirelessly as a means for global reconciliation [27]. Power transmission through electromagnetic waves would allow a near unlimited source of available power from the environment. This would allow for applications which could potentially do completely without an on-board battery [28]. Applications in various fields can be reached: display technology, biomedical sensors, and wireless networks would allow for both complex and compact electronic solutions to become commonplace in everyday lives.

Previous works on near-field magnetic resonance [29] and inductive coupling [30] solutions are considered near-field solutions. Far-field power transmission through RF/microwave energy transmission presents itself as the viable option to fulfill the power transmission challenge; with solutions combining solar harvesting in space and then converting harvested power to microwaves beamed down to earth [31, 32] to low power radiofrequency ID (RFID) tags working with μW of power [33].

Fig. 11 shows an overall radiofrequency (RF) energy harvesting system. The system is made up of a Power Transmitter which generates the power to be transmitted, efficiency and power to be transmitted stand out as the main limitations in this block. Depending on the application, antennas are chosen which meet directionality and polarization.

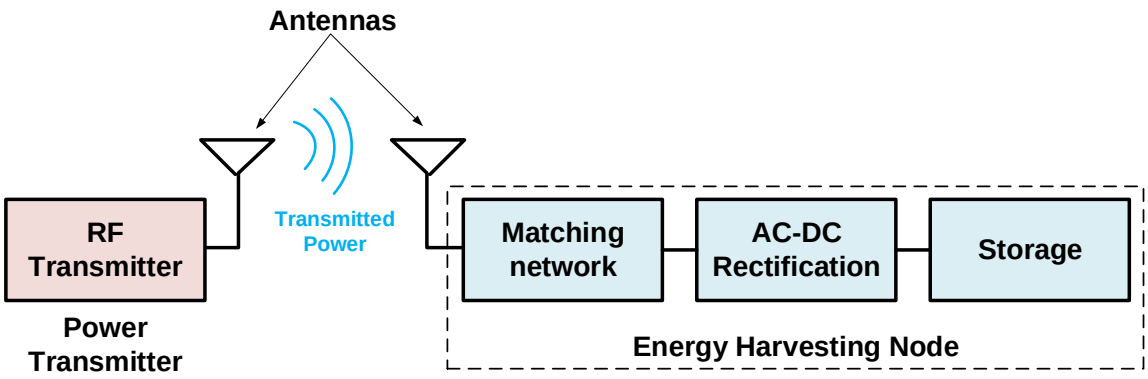

Fig. 11. RF energy harvesting system.

Once the power is transmitted through the medium, the RF energy harvesting node takes the available RF power and converts it to stored power.

As RF harvesting is aimed at far-field applications, power must be extracted from the air at increasingly low power densities. This is due to the propagation energy dropping off rapidly as distance from the source increase [34]. In free space both electric field and power densities drop off at a rate of $1/d^2$, with d being the distance from the power transmitting source. This signifies that 6 dBs of power are lost for every doubling of the distance from transmitter, causing serious strain on the receiving energy harvesting node block.

The components making up the node are: receiving antenna, matching network, AC-DC rectification block, and finally a Storage block [18]. As shown in Fig. 11, the antenna picks up the radiated power from the power transmitter, the matching network operates to ensure maximum power is transferred to the system, the AC-DC rectification converts the incoming RF signal to a DC voltage while performing a DC voltage gain,

and finally the Storage block comprised of a storage element such as capacitor or battery.

Implementation of the matching network is usually performed with off-chip inductors and capacitors, ensuring high quality factors (Q) and low parasitic resistance values. A drawback of having a high valued Q is the limitation in harvested bandwidth over which the system may operate as shown:

$$Q = \omega \cdot \left(\frac{Energy\ Stored}{Average\ Power\ Dissipated}\right) \rightarrow Q = \frac{f_c}{\Delta f} \tag{10}$$

where ω is the tuned frequency of the matching network, f_c the center frequency of operation and Δf the system bandwidth.

Both the antenna impedance matched to the input impedance of the rectifier circuit will allow for best operational performance for the system. Matching allows for passive amplification of the signal to reduce stress on the AC-DC block.

Fig. 12 shows an individual AC-DC rectification block. As RF power enters the rectifier, it is rectified and delivered to the DC output node during the positive half-cycle. While at the negative half-cycle, the voltage is clamped through the input capacitor C_{in} to the maximum voltage achieved during the positive half-cycle. Fig. 13 shows the aforementioned operation of the rectifying block.

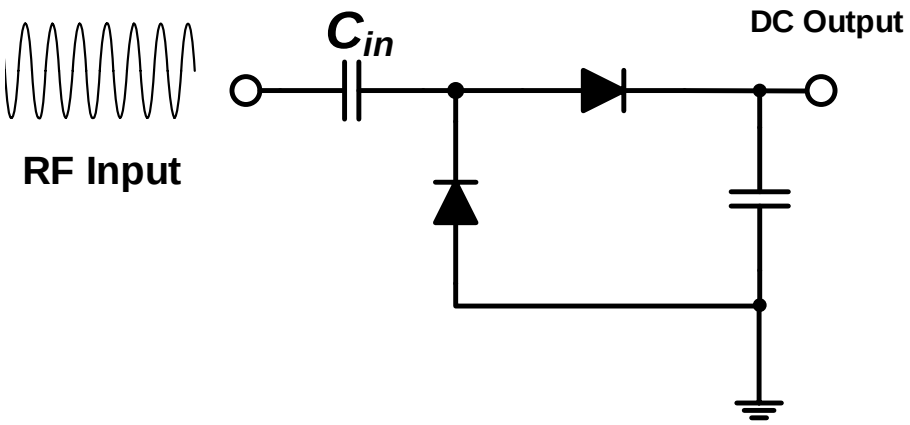

Fig. 12. AC-DC rectifier.

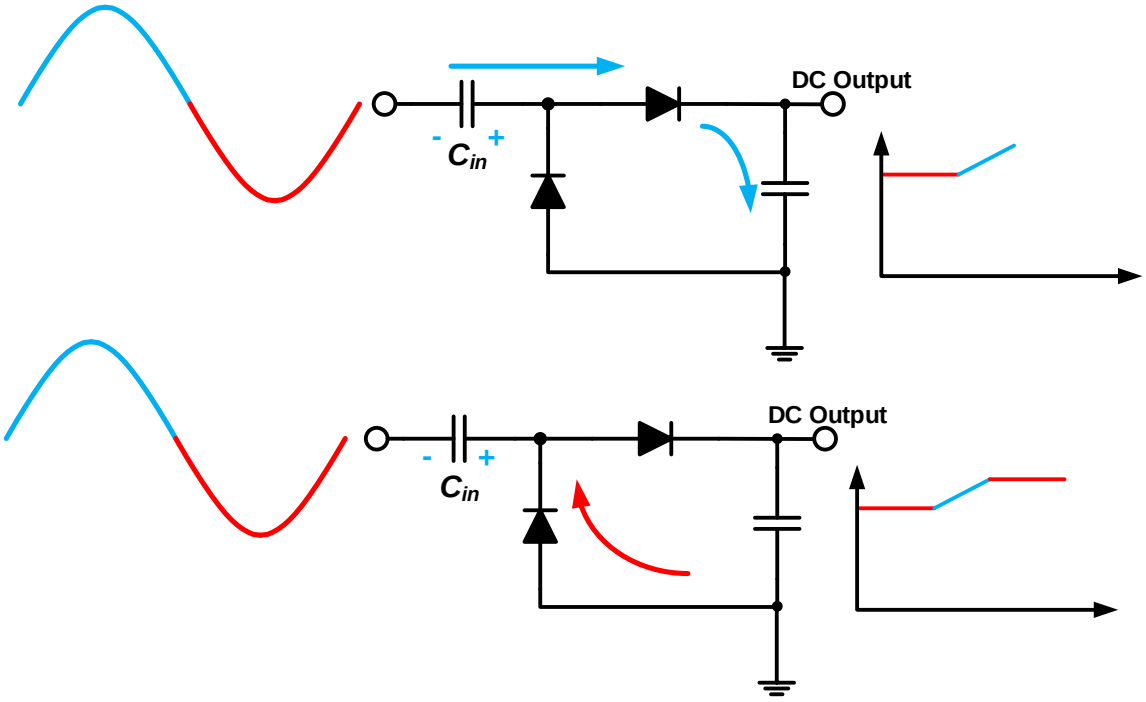

Fig. 13. Positive and negative half-cycle performance for RF AC-DC rectifier.

As a single stage can theoretically deliver a maximum of 2X the input voltage peak, a series of cascaded rectifier blocks can potentially lead to an ever increasing output voltage value as shown in (11).

$$V_{out} = n_{stage} V_{in,peak} - \frac{n_{stage} - 1}{f_c \cdot C_{out}} I_{Load} \tag{11}$$

where n_{stage} is the number of stages in the rectifier block, $V_{in,peak}$ is the peak input voltage of the incoming RF signal, f_c the RF signal frequency, C_{out} the output capacitor at the DC output node, and I_{load} the output load at the DC output node. From (11) we see that for a power limited input signal, a finite output voltage can be achieved for a set output current I_{load}. Fig. 14 shows an N-stage AC-DC rectifier block by implementing multiple cascaded rectifier blocks.

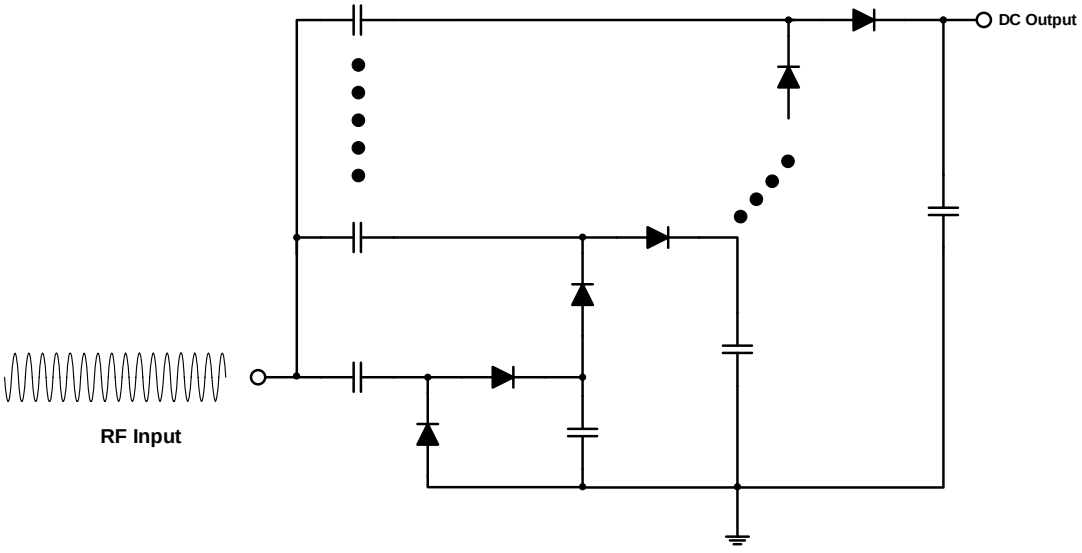

Fig. 14. N-stage AC-DC rectifier block for RF energy harvesting.

It should be noted that (11) does not take into account the forward bias voltage drops of the diodes in the rectifier. This reduces overall efficiency of the harvester by limiting the delivered power at the output node (DC output).

Implementing CMOS transistors as diodes helps alleviate the forward bias drop issue to an extent [18, 35], but are still a major bottleneck in RF harvesting technology and the minimum power needed for scavenging purposes; Fig. 15 shows both implementations.

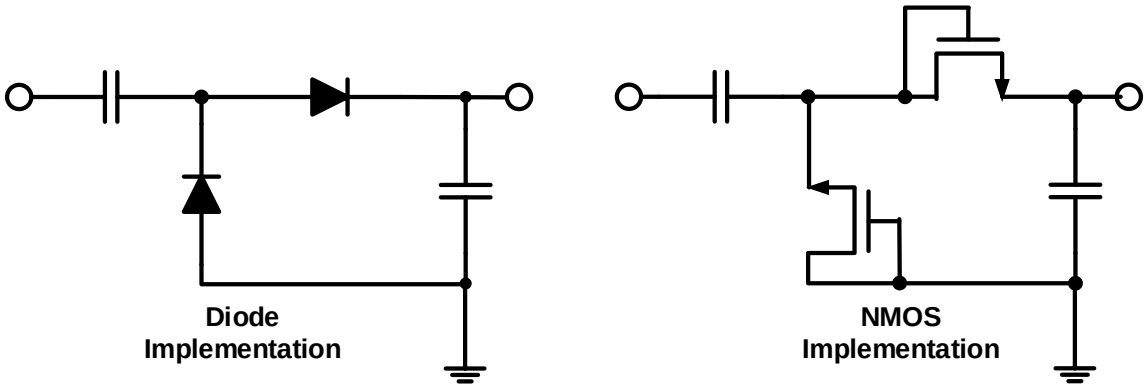

Fig. 15. Diode and NMOS implementation of AC-DC rectifier block for RF harvesting.

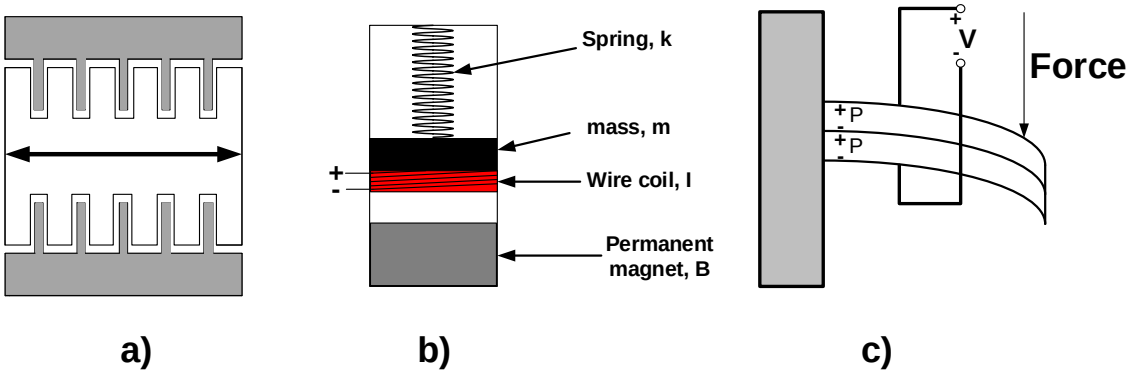

Fig. 16. Schematic of three types of electromechanical transducers a) electrostatic b) electromagnetic and c) piezoelectric.

Current limits for state-of-the-art harvesting sensitivity are ~ 25 dBm of input power for a 1.3 GHz RF frequency [36].

Kinetic energy harvesting

Focusing on the vibration energy available, we can see that vibration sources are generally ubiquitous and can be readily found in accessible locations such as air ducts and building structures. There are generally three types of electromechanical transducers that can convert vibration energy to electrical energy, these are: electrostatic, electromagnetic and piezoelectric and are shown in the figure below.

Out of the three different option for harvesting kinetic energy it is the piezoelectric device the one that has been more extensively studied and presents many advantages over the other two mechanisms, such as: simple configuration, high conversion efficiency and better control.

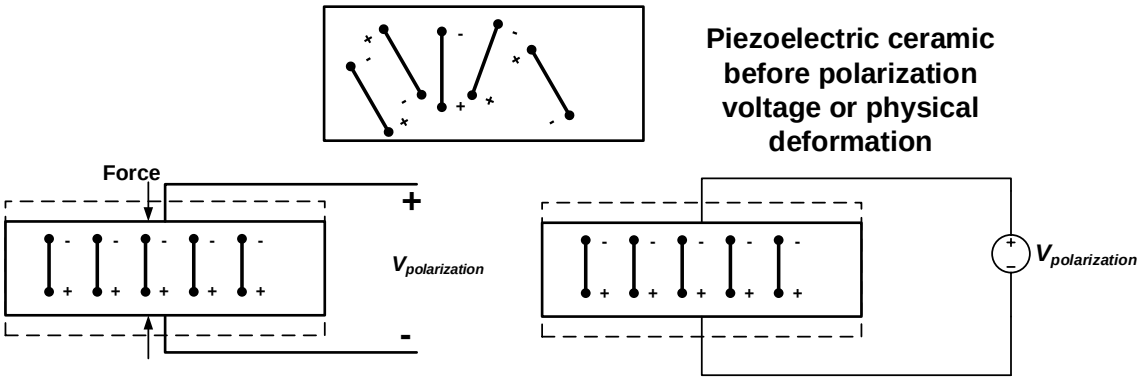

Fig. 17. Piezoelectric effect showing ceramic cation and anion reconfiguration with both external polarization voltage and deformation forces applied.

The manner in which piezoelectric materials operate is that they become electrically polarized, or undergo a change in polarization in their structure, when subjected to mechanical deformation (stress or changes in its original dimensions). This results in a variation in bond lengths between cations and anions, this may cause a flow of energy to occur if a closed circuit system is implemented [37]. Fig. 17 illustrates the aforementioned occurrence.

This phenomenon was discovered on many crystals, for instance, tourmaline, topaz, quartz, Rochelle salt, and cane sugar, by Jacques and Pierre Curie brothers in 1880, and named as piezoelectricity or piezoelectric effect, which describes a relationship between stress and voltage. Conversely, a piezoelectric material will have a change in dimension when it is exposed in an electric field. This inverse mechanism is called electrostriction (Fig. 17). Those devices utilizing the piezoelectric effect to

convert mechanical strain into electricity are called transducers, which can be used in sensing applications, such as sensors, microphones, and strain gages.

While those devices utilizing the inverse piezoelectric effect to generate a dimension change by adding an electric field are called actuators and used in actuation application, such as positioning control devices, and frequency selective device.

Among the important parameters to understand for a given piezoelectric material are those referring to the electric displacement component (C/m^2) which is a measure of charge storage or polarization at a given electric field. The charge generated is proportional to the applied pressure. This proportionality can be expressed in matrix notation in terms of dielectric displacement *D* (charge, *Q*, per unit area; Coulomb/meter^2-C/m^2), which is a measure of charge storage or polarization at a given electric field:

$$D_i = d_{ij}\sigma_j \quad (i = 1-3 \; and \; j = 1-6) \tag{12}$$

where *dij* are the piezoelectric coefficients (*C/N*), also called charge coefficients, and σ_j are the stress (N/m^2) components.

Among the commercially available materials used in piezoelectric devices Lead Zirconate Titanate (PZT) based ceramics are the most commonly used due to their excellent piezoelectric properties and high coefficient variable values. It is important to note that the piezoelectric coefficients dictate the energy harvester's performance, the main parameter to focus on for energy harvesting applications is the piezoelectric voltage coefficient g_{33}, these coefficients relate the electric field to the applied stress by the following equation:

$$g_{33} = \frac{d_{33}}{\varepsilon_o \cdot K_3} \tag{13}$$

where ε_o is the permittivity of free space and K_3 is the relative dielectric constant of the material. Higher *g33* values yield higher output voltages. This coefficient is low for bulk PZT ceramics due to their high *K3*. However, *g33* can be increased by incorporating the PZT ceramic as continuous parallel rods in an inactive polymer matrix.

The application of an external force, σ, to a piezo material creates an Electric field, E, proportional to the voltage coefficient, g. This is expressed by the following equation:

$$E = g \cdot \sigma \tag{14}$$

Considering that the electric field is given by $E = \frac{V}{L}$ and $\sigma = \frac{F}{A}$, we can assume that the output voltage due to the applied force on the piezoelectric material is given by:

$$V = \frac{g \cdot F \cdot L}{A} \tag{15}$$

where V is the voltage, F is the applied force, L and A are the length and cross section of the device. From this equation we can see that for larger voltage coefficients, force and length, along with small cross section gives us the best results in terms of output voltage. Accordingly piezoelectric fibers give off higher voltages from high L/A ratios. Hence a tradeoff is seen in terms of area and length, but it is the voltage coefficient which is the main restriction in terms of good power conversion.

A second important factor in piezoelectric converters is the resonant frequency, which limits the range of operational frequency the transducer possesses. Depending on resonant frequency, a particular application driven design may be achieved.

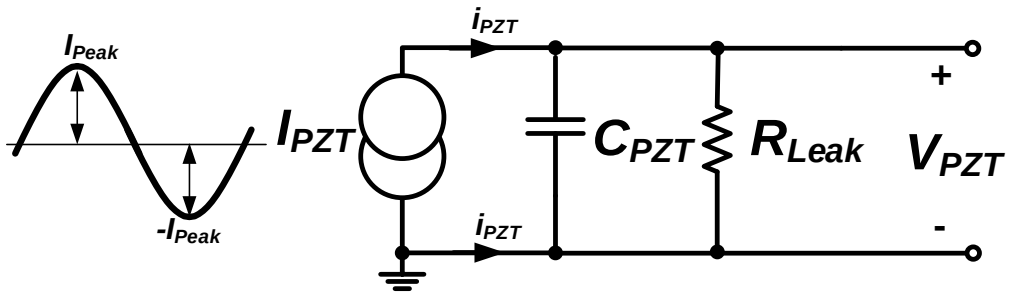

Fig. 18. Piezoelectric energy harvester electrical model.

A first approach to the calculation of the resonant frequency is given by:

$$f_r = \frac{\omega}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{K}{m_e}} \tag{16}$$

where *fr* is the resonant frequency; ω is the angular frequency; *K* is the spring constant at the tip of the cantilever, *me* is the effective mass of the cantilever. It can be easily seen that for higher value of masses i.e. area, we can expect a much lower resonant frequency for the device.

As the piezoelectric transducer bends in both directions during mechanical stress, the electrical equivalent model behaves as an AC current source (I_{PZT}) which charges and discharges a capacitance across the material surface (C_{PZT}). A leakage resistor is also considered, R_{Leak}, causing some loss in the delivered charge.

This dissertation does not deal with the power generated from kinetic energy harvesting sources.

Alternative energy harvesting sources

Alternative approaches to generate power have been continuously researched in hopes to reduce the dependency on fossil fuels. As mentioned throughout this chapter, many of the energy harvesting technologies have the potential of reducing the carbon footprint of humans. Taking an approach which considers biological substances as potential sources of power is not entirely new; in the late 1700s, Luigi Galvani noted that living beings possessed a capacity to generate electrical charges within the body. This would lead researchers to look at microscopic sources for power: bacteria.

In 1911, the first paper published on the power generation capabilities of bacteria were first reported [38]. This would lead to implementing groups of bacteria into cells to better harness their power generation capacity. This led to the breakthrough of Microbial Fuel Cells (MFC).

MFCs are a bioelectrochemical technology that converts chemical energy into electrical energy by producing electricity directly from biodegradable substrates such as wastewater; Fig. 19 shows a simplified schematic of the MFC. In MFCs, exoelectrogenic bacteria break down the carbon substrates while producing electrons, which are then transferred to the anode [39]; these electrons flow to the cathode through an external load, and then combine with protons and oxygen to form water, thus completing a full circuit and producing electricity.

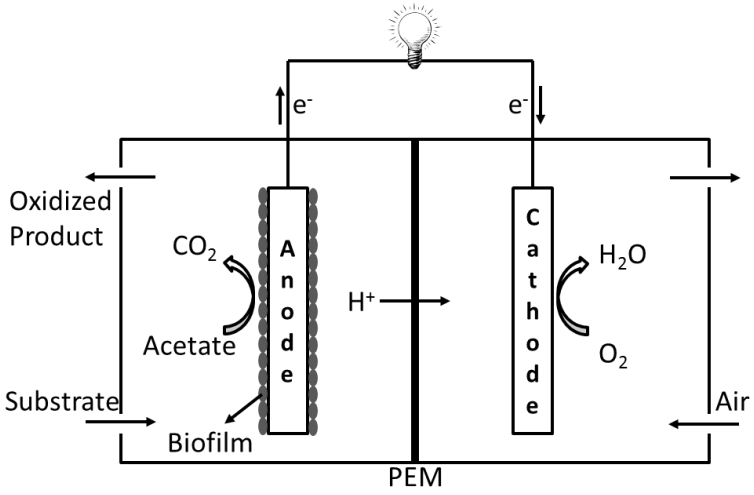

Fig. 19. Microbial fuel cell two-chamber schematic.

The operating principle with MFCs is through the digestion of sugars by micro-organisms in aerobic conditions. These conditions allow for sugar to breakdown into carbon dioxide and water. Whenever oxygen is not present in the reaction, the byproducts of digestion leave carbon dioxide, protons, and electrons.

$$C_{12}H_{22}O_{11} + 13H_2O \rightarrow 12CO_2 + 48H^+ + 48e^- \quad (17)$$

MFCs use these byproducts and funnel the protons through the Proton Exchange Membrane (PEM) in Fig. 19. Causing a potential difference across the chambers and allowing for a built-in potential to develop and manifest at the anode-cathode connections set externally.

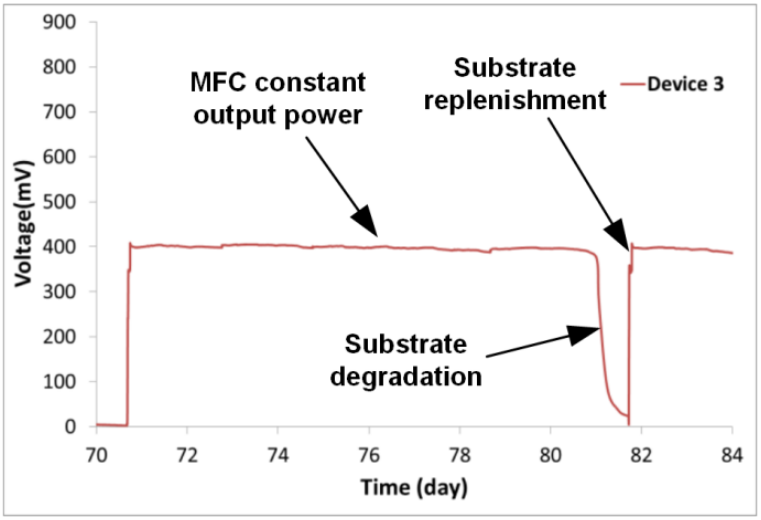

Fig. 20. Output voltage of MFC vs. time.

The device must also possess the ability to oxidize the substrate being injected into the chamber, through either an intermittent or continuous mechanism; otherwise the system falls into the biobattery category. The defining characteristic of the MFC lies in the catalyzed electron liberation at the anode and subsequent electron consumption at the cathode, in a sustainable fashion.

Since the MFC technology is dependent on biological variables, non-linearity is to be expected. As the substrate is completely consumed by the bacteria within the anode chamber of the MFC, the exoelectrogenic activity within the chamber reduces. This causes an output power degradation; thus, both the measured voltage and current are reduced. Fig. 20 shows the tested performance for a two chamber MFC, with 240 mL volume. It can be seen from this plot that on the 81st day, the output voltage abruptly drops, until substrate replenishment is performed.

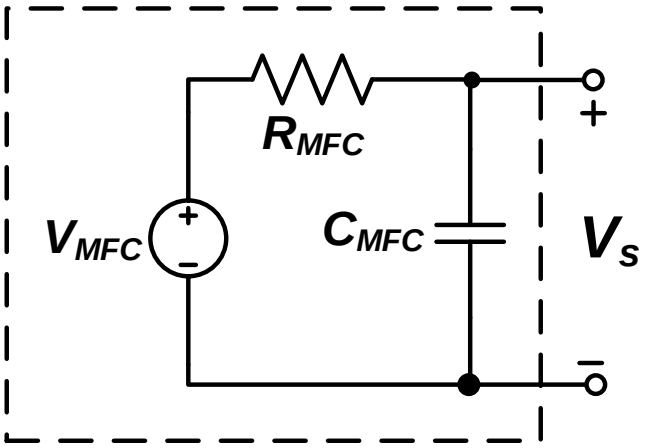

Fig. 21. Microbial fuel cell simplified electrical equivalent model.

This sets a limit to the applications in which the MFC technology can aid, a common thread in all energy harvesting technology. Nevertheless, given the right conditions and constant substrate replenishment application (water treatment plants), MFCs can potentially lead to helpful power generation to reduce overall power demand and load of a system.

A simplified electrical equivalent model of the MFCs is constructed in Fig. 21. This first order model possesses a dynamic and steady-state power component. By implementing the series resistor, R_{MFC}, a maximum power capability is determined in the MFC model. While the parasitic capacitor, C_{MFC}, is used to model the dynamic behavior of the MFC whenever a charging/discharging scenario is presented.

More complete electrical equivalent models consider multiple variables [40], i.e. pH, temperature, and concentration. Nonetheless, for first order approximation electrical model, from Fig. 21, offers sufficient information for proper PMU design. Chapters IV,

V and VI in this dissertation will present a solution to harvesting maximum power for MFCs aimed at low-power, wireless sensor node applications.

Voltage regulators

As the energy harvesting transducers offer unregulated voltage, the need for regulators is a must. Since the power produced by the transducers is non-continuous and at times extremely sparse. The need for power conditioners capable of storing and later delivering the stored energy to electrical loads on demand becomes apparent.

The implemented regulators must be highly efficient, as well as low-power in order to deliver the vast majority of the harvested power to the load. This is shown as:

$$\eta_{eff} = \frac{P_{Load} - P_{losses} - P_{consumed}}{P_{input}} \tag{18}$$

From (18) we see that the overall efficiency depends on both losses and consumed regulator power, this becomes a major issue when the input power, P_{in} is extremely small to begin with. Two major topologies of power converters will be briefly described and overviewed to better understand the major benefits and drawbacks with each topology: switching regulators and linear regulators.

Inductive switching regulators

Switching regulators are a category of regulator that implement magnetic-based components (inductor) to draw, store, and then release charge to an electronic load. This is achieved by temporarily energizing and de-energizing inductors in alternating cycles.

As see in Fig. 22, the input inductor, L_{in}, draws current from the input source by connecting L_{in} to the input source, V_{in}, to one terminal and the second terminal to a lower potential. This causes the inductor current, i_{Lin}, to increase in a proportional manner as the waveform in Fig. 22b shows (blue). The almost linear current increase is due to the inductor voltage is determined by:

$$V_{Lin} = L_{in}\frac{di_{Lin}}{dt} = V_{in} \tag{19}$$

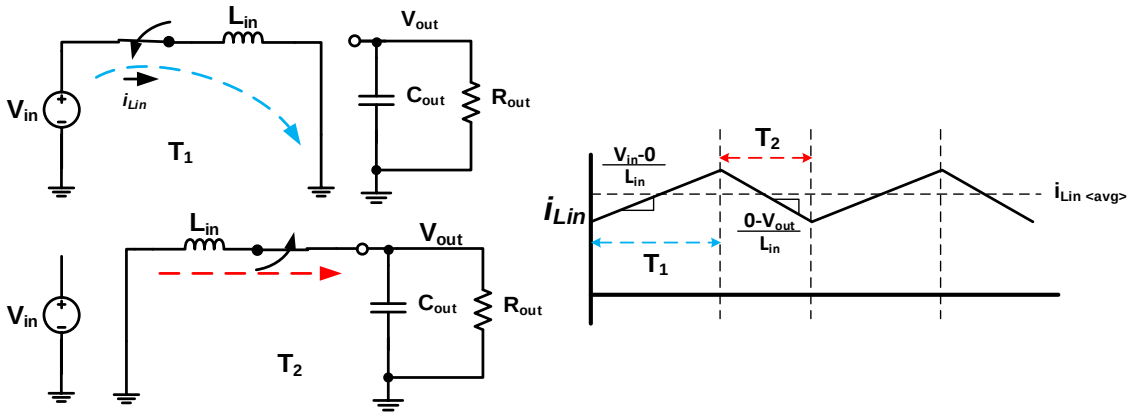

Fig. 22. A) Switching phases and B) inductor current waveform of an inductive switching regulator.

During the complementary cycle V_{Lin} is subjected to the output voltage, V_{out}, which effectively causes a reverse polarity across L_{in}. This causes the inductor to release energy which was received in the first cycle (Fig. 22B).

Since V_{out} is usually regulated to a set level, the output voltage is usually constant and well defined. This causes L_{in} to discharge at a rate of $-V_{out}/L_{in}$. Both the

input and output voltage define the inductor current ripple and amount of energy delivered to the load.

Since the output current to be delivered should be continuous, the inductor ripple current sits above a steady-state averaged DC current value given by $i_{Lin<avg>}$. Depending on the load demands, the inductor ripple current may ride on a high valued steady-state value, or the current ripple may reach zero amps during the discharging cycle, before the next charging cycle. The value of the inductor ripple current prior to the next charging cycle defines whether the switching converter operates in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). Both of these modes of operation are further discussed in Chapter II.

A second feature which is integral to inductive switching converters is the ability to produce a higher (boost) or lower (buck) voltages. These higher or lower voltages can be achieved as long as the charging and discharging cycles of L_{in} remain positive and negative, respectively. This since in order for L_{in} to release the stored charge to the load, requires the differences across its terminals for correct charging/discharging.

The inductors used in switching regulators allow for continuous current by instantly varying its voltage until an adequate supply or load is found for its stored charge. Any switch resistance or inductor DC resistance, R_{series}, exhibited in the converter will drop a root-mean-square voltage, dissipating the following expression:

$$P_R = I_{Lin(rms)}^2 \cdot R_{series} \tag{20}$$

Since the associated DC resistances are usually low, inductive switching converter offer high values of efficiency. The conduction losses (P_R) while low are not zero, and are proportional to the input current squared. Increasing this current will also increase the amount of power burnt on these resistors, increasing conduction losses.

Capacitive switching regulators

The capacitive switching regulator, or more commonly known Charge Pump, implements the same principle as the inductive switching regulator but instead of using a magnetic component for charge storage, a capacitor is used. Both buck and boost operations are possible with charge pumps.

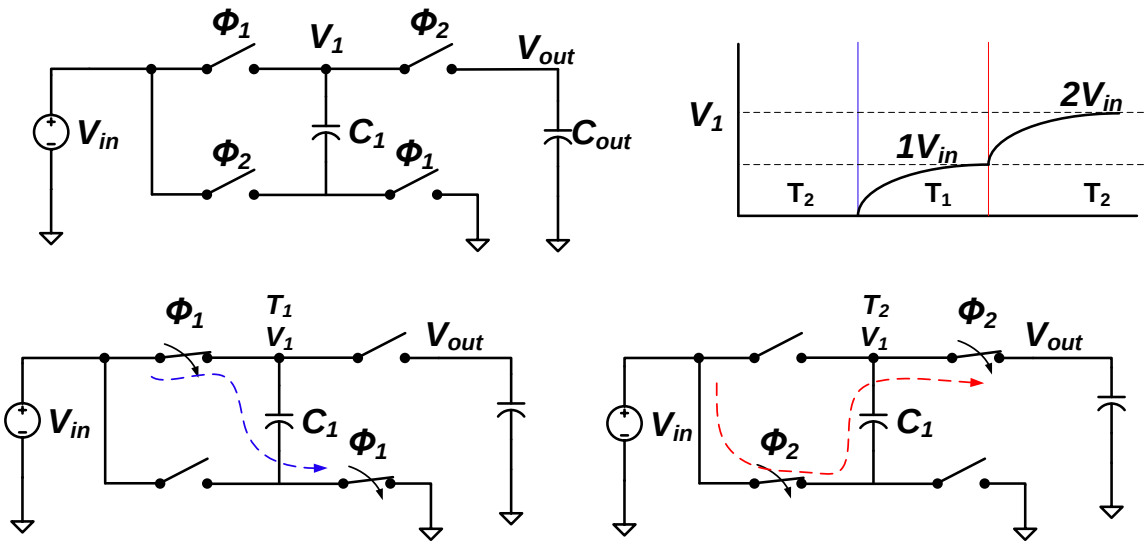

Fig. 23. Operation and switching waveforms for a simple voltage doubler.

Compared with inductive switching regulators, charge pumps offer an alternative to designs where the use of magnetic components is not desired. Offering a fully integrated approach is also an added bonus to using charge pumps as voltage regulators for applications. Fig. 23 shows the operation and waveform of the intermediate node in a simple voltage doubler topology.

During ϕ_1 the "flying" capacitor C_1 is charged up to V_{in}, while the output voltage V_{out} in capacitor C_{out} remains static.

$$Q_{C1} = V_{in} \cdot C_1 \tag{21}$$

During ϕ_2, the flying capacitor is placed in series with V_{in}, and the addition of both these voltages delivers a 2X increment to V_{out} (now in parallel with the series C_1 and V_{in}).

$$Q_{C1} = (V_{out} - V_{in}) \cdot C_1 = V_{in} \cdot C_1 \rightarrow V_{out} = 2 \cdot V_{in} \tag{22}$$

Multiple topologies can be implemented with the flying capacitor topologies [41], going from parallel-series (Fig. 23) for step-up operations, as well as series-parallel for step-down voltages.

Nonetheless, the main limitations of charge pumps are the required area for the desired application, capacitor density areas in integrated CMOS processes are low and lossy (high ESR and leakage) compared to discrete components, output noise due to constant switching of capacitors, and output current delivering capability [41]. For higher current delivering densities (low output resistance of charge pump) a higher capacitance value is required [42]:

$$R_{out} = \frac{N}{C_{stage} \cdot f_{switching}} \tag{23}$$

where N is the number of stages in the charge pump topology, C_{stage} is the flying capacitance value, and $f_{switching}$ is the switching frequency of the charge pump. Due to these limitations, charge pumps are widely used in internal CPU memories and solid-state drives which require high-voltage pulses to program and erase data. Other applications for charge pumps are found in LED drivers, where high voltages are required while sacrificing minimum area.

Linear regulators

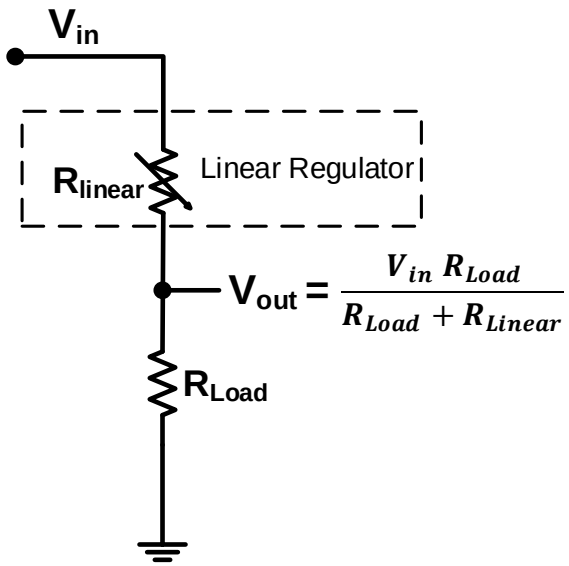

Fig. 24. Linear regulator simplified schematic.

The linear regulator is, at its name dictates, a linearly dependent variable that delivers a constant output voltage from a higher input voltage. Fig. 24 shows a simplified representation of the operational principle of linear regulators. As V_{in} or R_{Load} change, the variable resistor R_{linear} varies its value in order to maintain V_{out} constant.

The implementation of R_{linear} is usually implemented through a semiconductor transistor, who's conductance is modulated through a control loop to maintain V_{out} constant. Due to the low number of transistors in the overall implementation of the regulator, it is able to react quickly to load demands as well as having limited quiescent power consumption. This circuit generates minimum noise to the output load (not counting thermal noise) since it is not periodically switching between fully on and off stages [43].

The main limitation in this type of approach to regulation is voltage flexibility. For a linear regulator V_{in} will always be greater than V_{out}, a case which is not so in inductive or capacitive switching regulators. Also, the energy harvesting transducer and output storage (capacitor) set the voltage across R_{in}, which means that the power lost in the linearly variable resistor rises linearly with input current. This sets maximum efficiency of the regulator as a function of the dropout voltage (voltage drop across R_{in}).

$$\eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{Loss}} = \frac{V_{out} \cdot I_{out}}{V_{out} \cdot I_{out} + (V_{in} - V_{out}) \cdot I_{out}} = \frac{V_{out}}{V_{in}} \tag{24}$$

From (24), if the input voltage were to be 15 V and the output 2.5 V, the overall regulator efficiency would fall to ~17%. This would mean that approximately 83% of the input power is spent on R_{in}. This also signifies that the linear regulator is extremely highly efficient for V_{out} values close to V_{in}. Also, linear regulators possess superior noise rejection, mainly due to the lack of switching components when compared to the switching regulator counterparts.

Energy storage elements

Having a place to store the harvested power from the energy harvesting sources is a critical component in any power management solution. Solutions range from batteries, to temporary storage units such as capacitors.

Breakthroughs are performed at a rapid rate in both battery technology [44, 45] and capacitor technology in the form of supercapacitors/ultracapacitors [46, 47]. Although both components offer their respective benefits to temporary storage, the main difference between both technologies is the power/energy density availability. Whereas capacitor technologies possess a much higher power delivery density, delivering high current values in an instantaneous fashion; battery technology offers a more energy dense solutions, capable of delivering steady amounts of energy over longer periods of time. Fig. 25 shows a conceptual comparison between both power and energy densities.

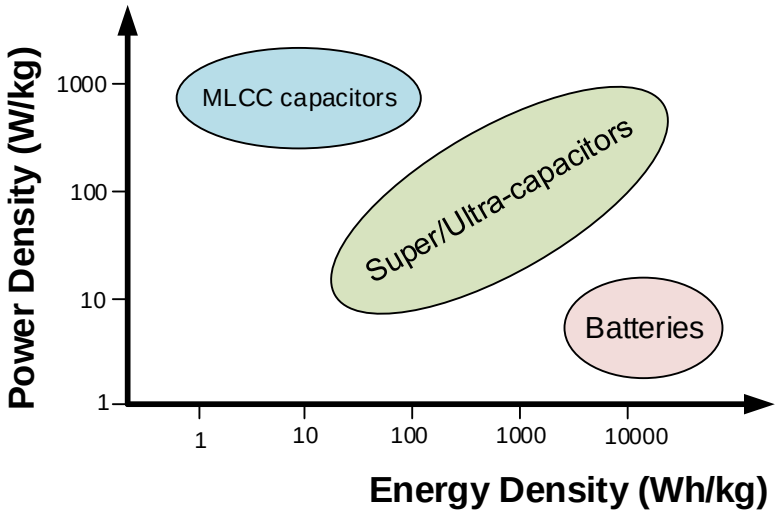

Fig. 25. Comparison of power density vs. energy density in batteries and super/ultra-capacitors.

Power management's significance on energy harvesting technology

Due to the non-continuous nature of energy harvesting power sources, a smart and efficient power management block is needed to shape the available power and deliver it to a storage/electronic load.

New applications in the field of wireless sensor network require multiple sensor networks, which can number in the hundreds [48-50], require a power source capable of operating over long periods of time. And even with longer lasting power sources on-board, whenever these sources were to run out, the operation of changing batteries on hundreds of sensors nodes becomes a tedious and impractical task.

Energy harvesting technology would potentially increase the power availability with sensor networks ad infinitum. By continuously extracting power from the environment and maintaining an ultra-low-power operation, overall operational lifetime would increase immensely.

Proposed solution

This dissertation presents four unique power management solutions Energy Harvesting sources. Implementing inductive, capacitive and linear regulator approaches; the focus of extracting maximum power as well as delivering a regulated load are tackled in the proposed approaches.

The first part of the dissertation focuses on the application of inductive switching regulators and their use in energy harvesting applications. In the first work, a built-in input matching technique capable of handling a wide variation of multi-array TEG impedances ranging two decades, from 10s to 1000s of ohms is presented. Maximum power point tracking (MPPT) control for a boost converter (BC) are performed to assure maximum power transfer. A prototype was fabricated in 0.5 μm CMOS with the achieved goal of maximum measured efficiency of over 60% for an R_{TEG}=33.33Ω, and quiescent power consumption under 1μW. Fig. 26 shows the conceptual solution of the harvesting unit.

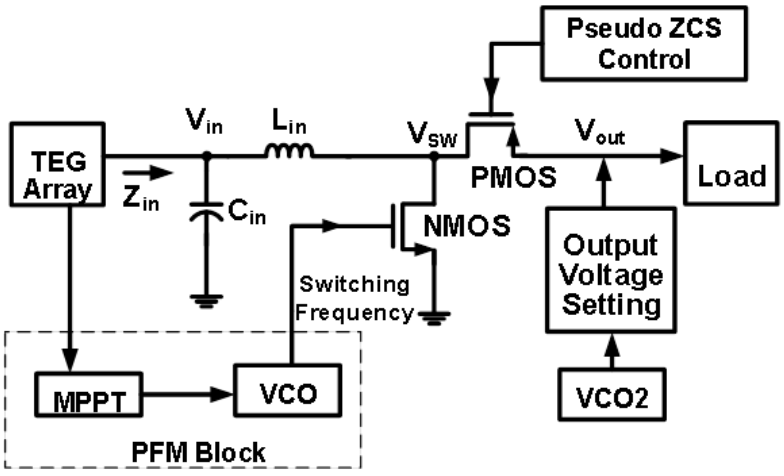

Fig. 26. Proposed solution for TEG array impedance matching and energy harvesting.

The second work focuses on extracting maximum power from MFCs. Due to the MFC's low power and voltage production, a power management system (PMS) is required to process the MFC power to a more readily usable level. For this application a monolithic PMS with an integrated maximum power extraction algorithm (MPEA) is presented. The MPEA will allow for quick and accurate pin-pointing of the matching conditions for maximum power transfer from the MFC to the PMS. The PMS was fabricated and tested in 0.5 μm CMOS technology. The maximum dynamic efficiency was measured at ~58%. Fig. 27 shows the conceptual solution of the harvesting unit.

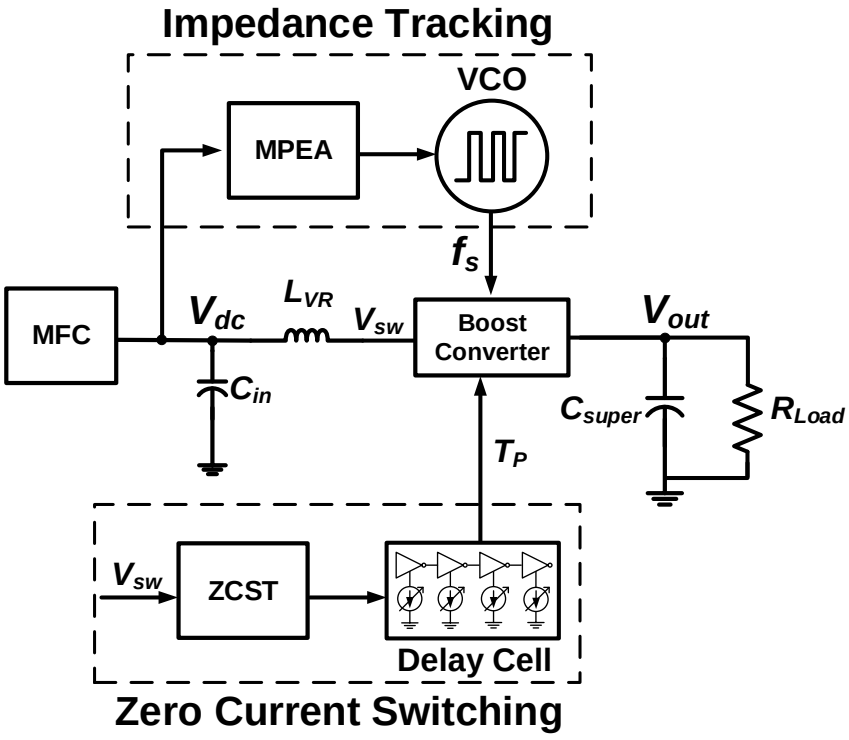

Fig. 27. Proposed solution for MFC source impedance matching and energy harvesting.

The second part of the proposal focuses on a more fully integrated approach by implementing switched capacitor regulators. A second solution targeted for MFC applications is presented via an inductorless DC-DC (I-DCDC) converter for an energy-aware power management unit (EA-PMU). The system is capable of performing a DC step-up gain of up to 10X and achieving MPPT efficiently. The converter is a key building block for an EA-PMU capable of identifying the best candidate for energy harvesting from an array of MFCs.

Due to the MFC's varying power profile over time, identifying and selecting the best MFC from an array enhances efficiency and overall power delivery. MPPT is achieved through wide variety of impedance scenarios from the MFC array while maintaining low power consumption. The converter was designed, fabricated, and tested in 0.18 µm CMOS process and achieved a maximum efficiency of 65%. Fig. 28 shows the conceptual solution of the harvesting unit.

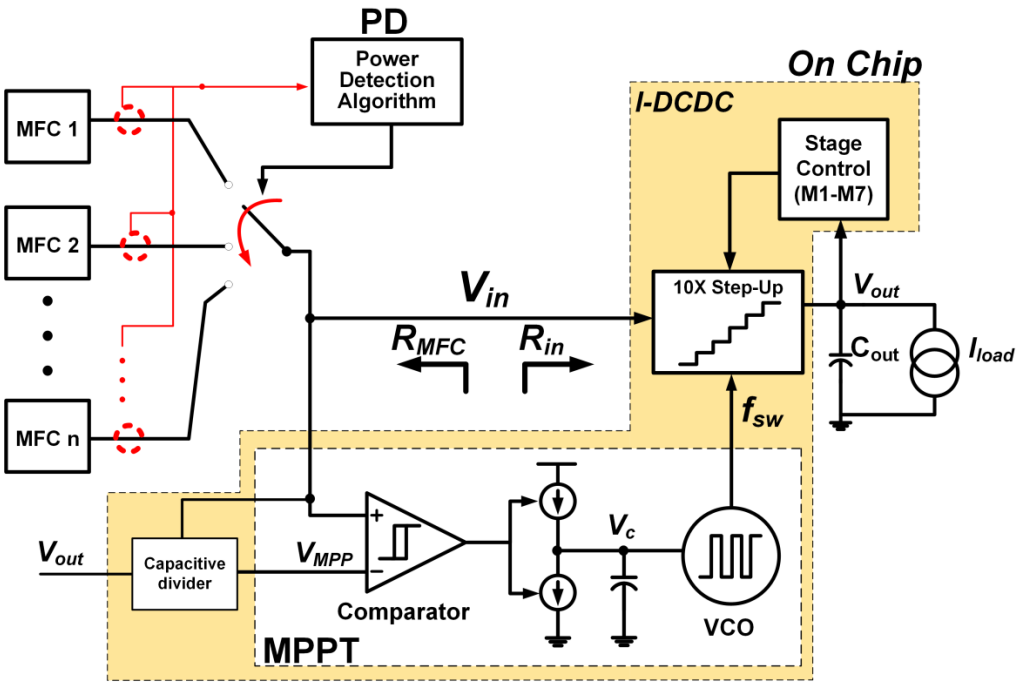

Fig. 28. Proposed solution for MFC array impedance matching and energy harvesting.

Finally an autonomous, fully integrated, Energy Harvesting power management unit (PMU) with digital regulation for Internet of Things (IoT) applications is presented.

The main focus of this work is targeted for wireless sensor node applications, and focus on performing maximum power extraction and storing harvested power. Efforts on delivering a regulated supply to noise sensitive blocks have yet to be fully achieved with current solutions. The presented PMU achieves full autonomous operation able to perform maximum power point tracking (MPPT) for DC type energy harvesting sources (solar, thermal, biomass), startup operation with the available power from the harvesting source, and deliver a regulated output voltage through a digital Low dropout (LDO) regulator. The system was fabricated in 0.18 μm CMOS process and maximum end-to-end efficiency was measured to be at 57 % with 1.75 mW of input power. Fig. 29 shows the conceptual solution of the autonomous power management unit.

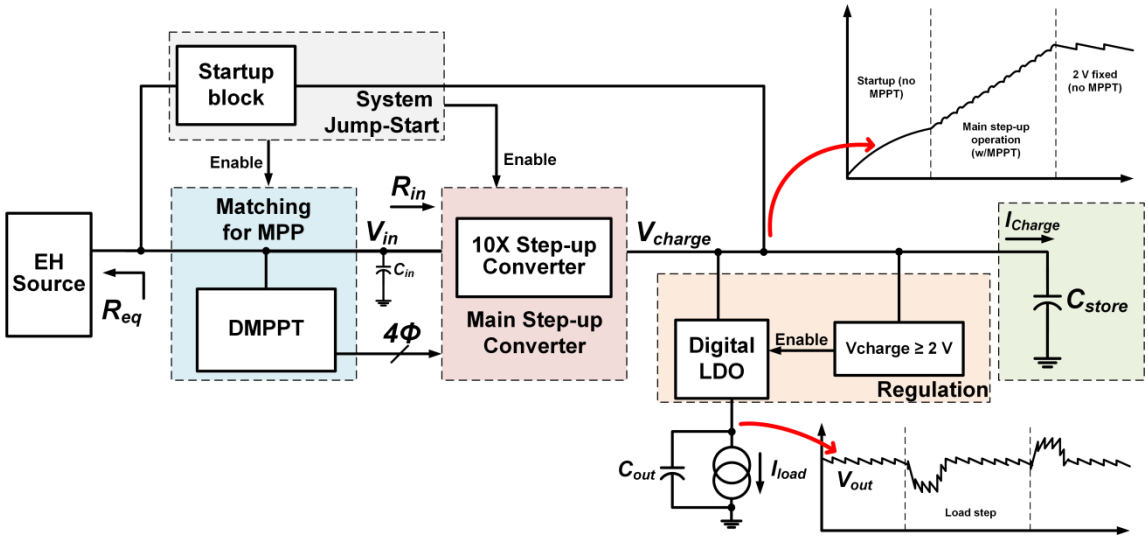

Fig. 29. Proposed solution for DC energy harvesting autonomous power management unit.

CHAPTER II

FUNDAMENTALS OF POWER MANAGEMENT SYSTEMS FOR ENERGY HARVESTING

Introduction

Nowadays, commercially available consumer electronics possess a wide variety of voltage/current level requirements that cannot be met with a single battery. Implementing each and every one of the voltage domains would require the same number of batteries, making the solution impractical. The answer lies in power processing circuits capable of delivering multiple voltage/current domains with a single source. As can be seen in Fig. 30, the main focus of these power processing circuits is to convert one power domain, usually input voltage/current levels incompatible with the required levels, to other more compatible voltage/current levels for the required application.

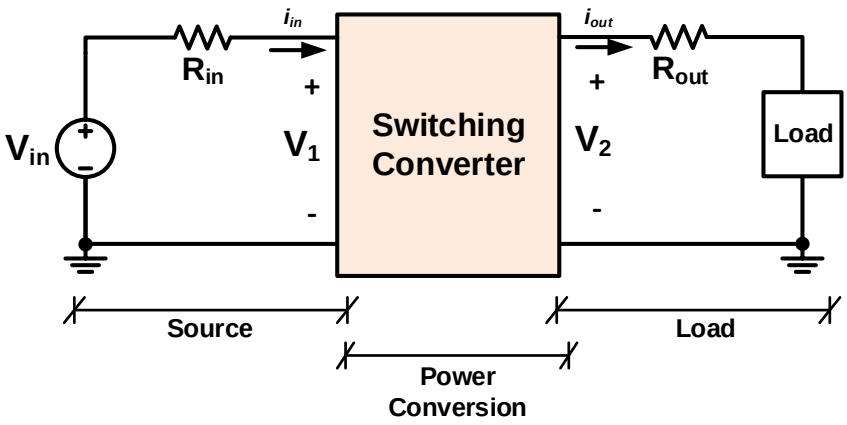

Fig. 30. Switching converter power conversion illustration.

A key component in these types of conversions is the switching converter. The switching converter operates by storing the input energy temporarily in magnetic field storage components (inductive, transformers) or electric field storage components (capacitors), then delivering the stored energy to the output load of the converter. This stored/deliver cycle is repeated multiple times to achieve the required output voltage level.

Akin to the switching converter, an alternative exists in the linear regulator. The linear regulator operates as a variable resistor, as shown in Fig. 31; the resistor varies its value in order to maintain a constant output voltage at V_{out} when load demands vary. Whereas the switching converter possesses a great flexibility in terms of load power delivery, the linear regulator is a more limited topology since it can only deliver output voltages below that of the input. Nonetheless, while the switching converter does possess a high degree of freedom in terms of output power delivery the required controller is higher in complexity when compared to the linear regulator.

When the variable resistor is implemented via an active device, i.e. a transistor, a special type of linear regulator is implemented, named a Low Dropout Regulator due to the low voltage drop across the Drain-Source (Collector-Emitter) terminals of the device.

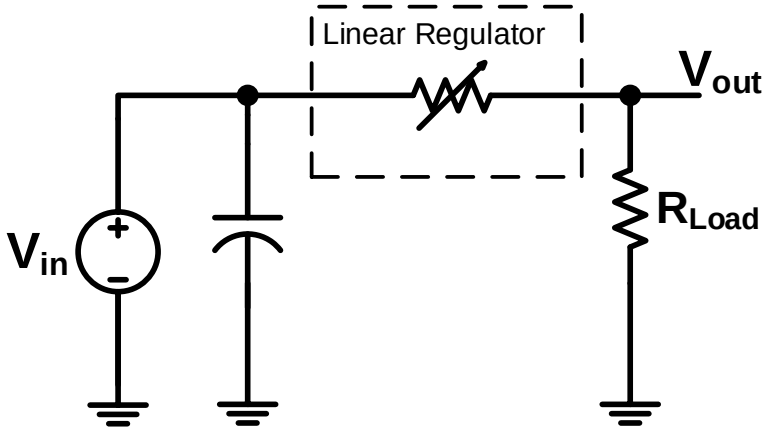

Fig. 31. Illustrative example of linear regulator.

In energy harvesting applications, due to the low power nature of the transducer sources, switching converters are implemented to step-up the delivered voltage levels of the transducers to usable voltage/current levels for the system. The present chapter of this dissertation will delve into the fundamentals of two main switching converter topologies: the boost converter and the charge pump (also known as switched capacitor regulator). The boost converter stores the input energy into a magnetic field storage component, an inductor; while the charge pump performs the energy storage through an electric field storage component, the capacitor. Linear regulators will also be described, mainly focusing on Low dropout regulators.

Switching converter fundamentals

Step-up (boost converter)

As mentioned previously, the switching converter categorized as a boost converter performs a step-up operation of the input voltage by storing energy through a magnetic element (an inductor) in one phase, then delivering the stored energy to the output in a complementary phase. Fig. 32 shows an illustrative boost converter schematic, where the input inductor, L_{in}, performs the energy storage, the power stage made up of two main switches S1 and S2, an output capacitor to stabilize and filter the output voltage, C_{out}, and finally the input and output voltages V_{in} and V_{out}.

As shown in Fig. 33, the inductor stores energy during one phase of the switching period, $D_1 = D \cdot T_{sw}$, with D being the duty cycle (percentage of the period) the switch S1 operates during this first phase to charge L_{in}.

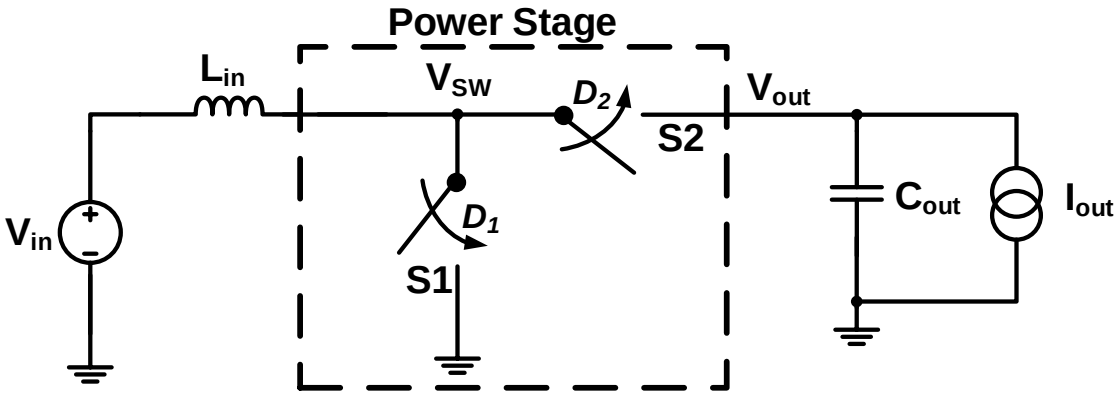

Fig. 32. Boost converter schematic.

Once the phase duration ends, S1 shuts off and S2 switches on, causing L_{in} to deliver the stored energy from the first phase to load. This secondary phase, $D_2 = (1 - D) \cdot T_{sw}$, sees the delivered energy to the output load and once D_2 is over, D_1 begins anew and the cycle repeats.

Both switches S1 and S2 are implemented through active components. Shown in Fig. 34 is a simplified schematic of the boost converter power stage with two different switch implementations: Asynchronous and Synchronous. For the asynchronous case, Fig. 34A, the switch network implemented via a transistor and diode: an NMOS transistor for S1, and an output diode S_D for S2. For the synchronous case, Fig. 34B, both switches are implemented via transistors: an NMOS transistor for S1, and a PMOS transistor for S2.

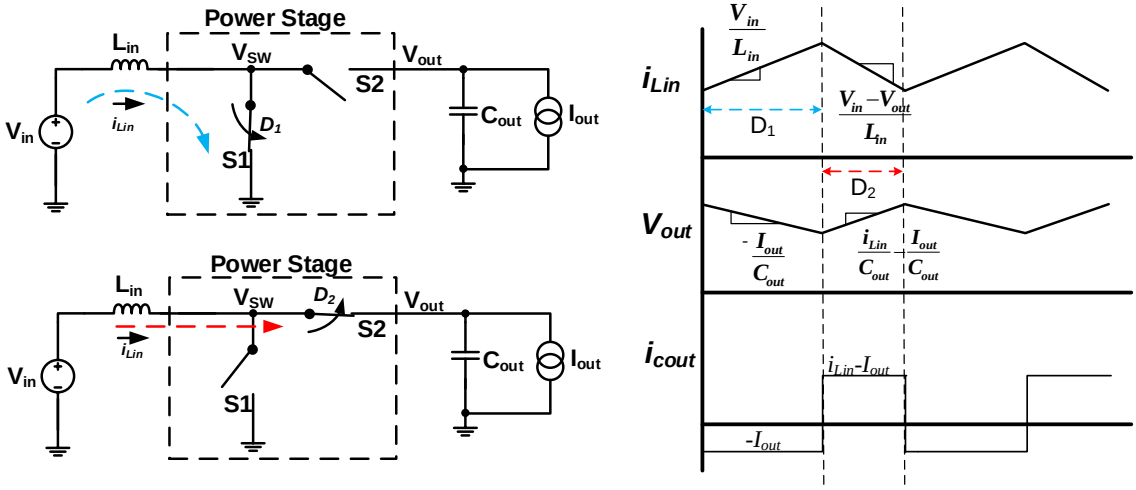

Fig. 33. Boost converter complementary phase operation.

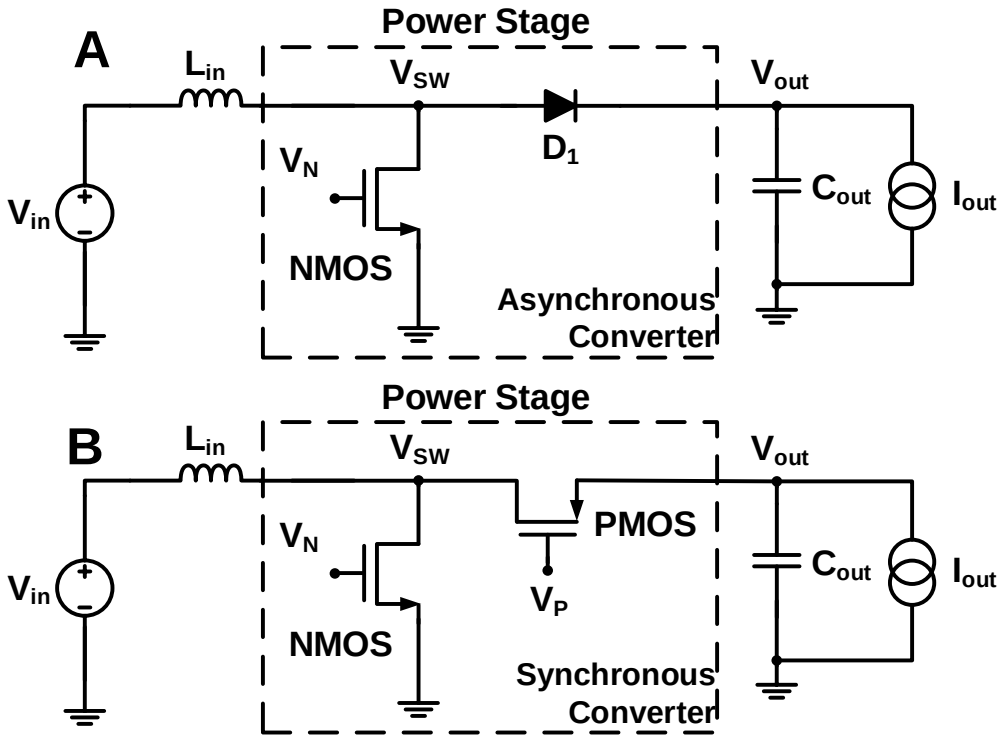

Fig. 34. A) Asynchronous boost converter schematic and B) synchronous boost converter schematic.

As asynchronous converters suffer from the forward bias drop of the diode, S_D, they have an inherent reduced overall efficiency. The synchronous converters possess a much higher efficiency due to the transistor voltage drop being much less than that of the diode, but require a much more complex control in order to avoid having the S2 switch on for too long, causing a backflow of current to the input.

Depending on load demands, the boost converter is able to operate under two different modes: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). CCM applications are usually implemented for heavy-load currents at the output voltage, whereas DCM applications are intended for more light-load applications.

Due to the load demand at the output, each operating mode has a distinctive current shape passing through L_{in}. While as in CCM mode the inductor current never reaches 0 A due to the high demand at the output, in DCM mode the inductor current falls to 0 A before or at the end of each period. Fig. 35 highlights both operating modes and the voltage nodes associated to the boost converter. A more detailed description of each operating mode will follow.

Independent of the type of power stage implemented (asynchronous or synchronous), or operation mode (CCM or DCM) design insights for steady state dynamics are needed for correct modeling of the converter for voltage regulation applications. The following section presents the modeling method for the converter based on the Pulse Width Modulation (PWM) switch design.

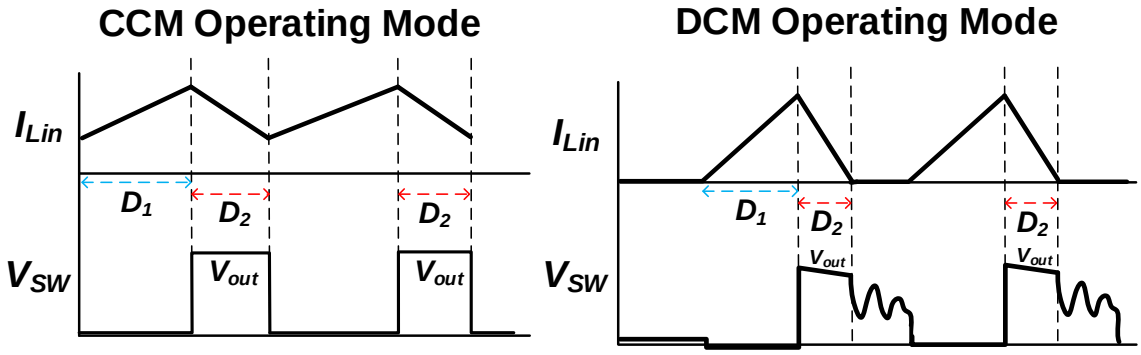

Fig. 35. Boost converter CCM and DCM inductor current waveforms.

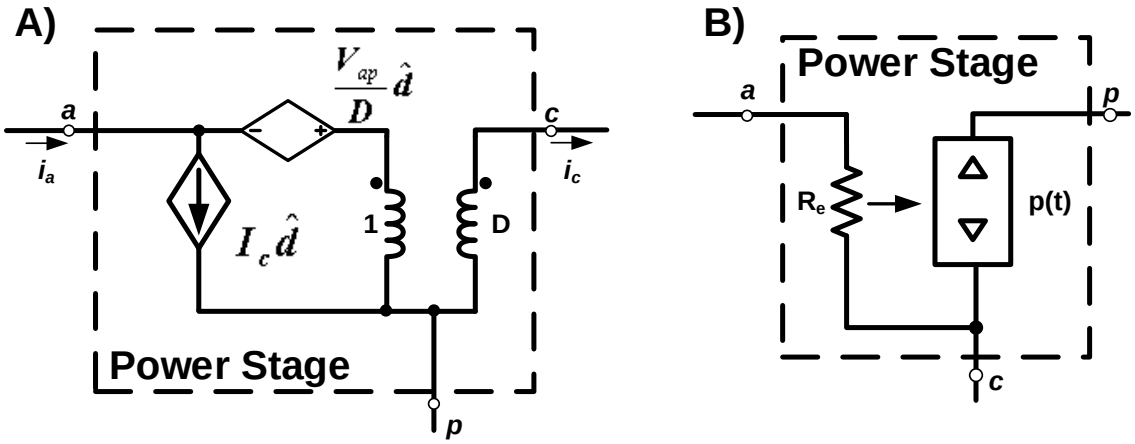

Fig. 36. DC and small signal models for CCM and DCM PWM switch implementations.

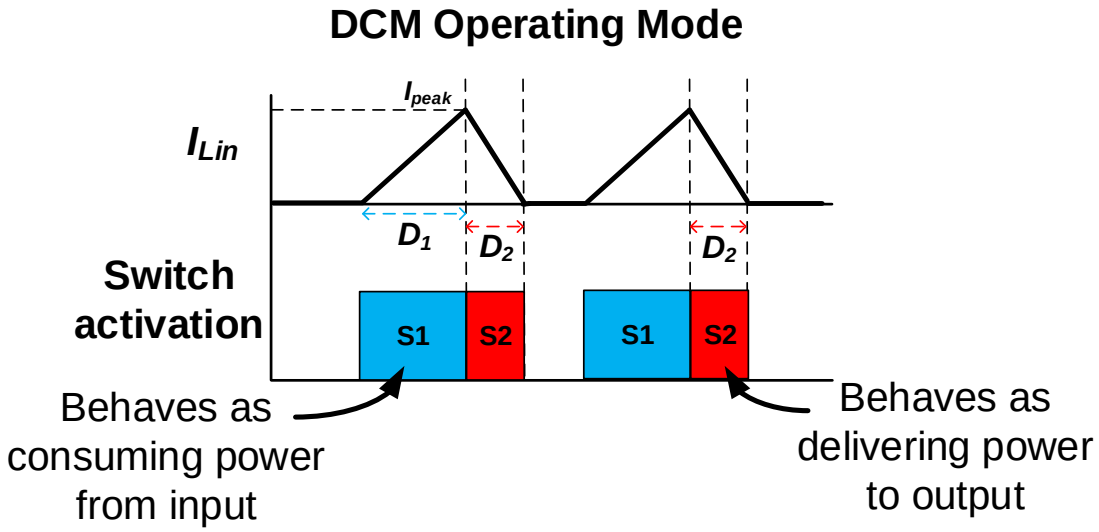

Fig. 37.DCM operating mode view of switch activation and behavior during each cycle.

Operating modes

A Pulse Width Modulation (PWM) switch model for each operating mode [51] allows for a simplified design approach while maintaining the system's characteristics. Fig. 36 shows the PWM equivalent model for both CCM (Fig. 36A) and DCM (Fig. 36B) operating modes for the boost converter. Both S1 and S2 switches from Fig. 32 are encompassed within the Power Stage dashed-line box and are replaced by a three terminal block. The terminals are labeled as *a* (active) connects to the S1 switch, *p* (passive) connects to the S2 switch, and *c* (common) is common node to both switches.

For the CCM operating mode variable *D* represents the steady-state duty cycle, $\hat{d}$ represents small AC variations of the duty cycle, and $\hat{d}$ represents the complete duty cycle including any DC component and AC variations. For the DCM operating mode the averaged switch waveforms (Fig. 37) obey Ohm's law, and are modeled by an effective resistance R_e and a power source *p(t)* delivering the dissipated power through R_e to the output. The averaged waveforms for S2 follow a power source characteristic, equal to the power effectively dissipated in R_e:

$$R_e = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\frac{I_{peak}}{2} D_1 \cdot T_{switching}} = \frac{2 \cdot V_{in}}{I_{peak} \cdot D_1 \cdot T_{switching}} = \frac{2 \cdot L_{in}}{D_1^2 \cdot T_{switching}} \tag{25}$$

Both operating mode models are inserted into the converter's power stage in order to model the converter dynamics and interaction with a control loop. Fig. 38 shows

the connection scheme with which the PWM model would be connected in a boost converter configuration independently of CCM or DCM operation.

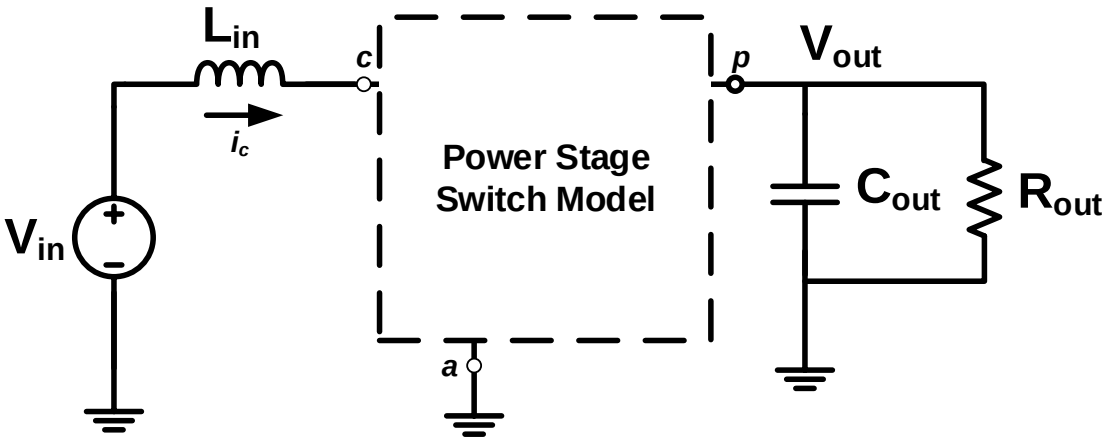

Fig. 38. Boost power stage with connection structure for PWM model.

Implementing The PWM model allows for simple DC and AC analysis of the converter. Due to the dependency of the AC analysis on DC parameters, the DC analysis should be performed prior to small-signal AC analysis.

For the CCM steady-state DC analysis the small-signal variables $\hat{d}$ is assumed zero, L_{in} is shorted, and C_{out} behaves as an open circuit.

$$-V_{in} + V_{cp} + V_{out} = 0 \tag{26}$$

$$i_c = \frac{V_{out}}{R_{out}} \cdot \frac{1}{1-D} \tag{27}$$

$$V_{cp} = V_{ap} \cdot D = -V_{out} \cdot D \tag{28}$$

Substituting the relationship between V_{CP} and i_c from (27) and (28) leads to the DC voltage gain expression in CCM:

$$\frac{V_{out}}{V_{in}} = M = \frac{1}{1-D} \tag{29}$$

Once all DC voltages are determined, the control-to-output transfer function can be determined. Since the analysis has been performed utilizing the PWM switch model, the control-to-input transfer function will contemplate duty cycle to output voltage control.

The control-to-output transfer function, given by $G_{vd}(s) = \hat{v}_{out}(s)/\hat{d}(s)$, is found by assuming a clean input voltage source (causing AC ground at this node), and then solving the equivalent circuit model for $\hat{v}_{out}(s)$ as a function of $\hat{d}$:

$$G_{vd}(s) = \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{K_{dc}\left(1-\frac{s}{\omega_{RHP}}\right)}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{30}$$

where K_{dc} is the DC gain of the converter and is given by:

$$K_{dc} = \frac{V_{out}}{(1-D)^2} \tag{31}$$

The system zero is set by:

$$\omega_{RHP} = \frac{(1-D)^2 R_{out}}{L_{in}} \tag{32}$$

And the resonant frequency and system Q are given by:

$$\omega_o = \frac{1}{\sqrt{L_{in}C_{out}}} \cdot \sqrt{(1-D)^2} \tag{33}$$

$$Q = C_{out}R_{out} \cdot \omega_o \tag{34}$$

The main problem with the CCM operation, is presented in its RHP zero (32). This will cause a phase shift of -90º while having the traditional effect of a zero on the magnitude (increase in magnitude). This is the cause of instability in the system and is reason why a control loop design that is capable of dealing with this system must not be taken lightly. It should be noted no inductance DCR or capacitor ESR are assumed in this model analysis.

In order to illustrate the DCM operating mode's steady-state analysis using the PWM switch model Fig. 36B, the DC steady-state operation will be detailed first. As with the CCM mode, the switch model is substituted into the power stage. The inductor is treated as a short circuit and the capacitor is treated as an open circuit. To obtain the DC operating voltages in steady-state two calculations are required: determine the power dissipated by the dependent power source, *p(t)* and match this value to the power consumed by R_e:

$$P_{pt} = P_{Re} = \frac{V_{in}^2}{R_e} = (V_{out} - V_{in}) \cdot I_{out} = \frac{(V_{out} - V_{in})(V_{out})}{R_{out}} \tag{35}$$

Rearranging for the conversion gain, V_{out}/V_{in}, and solving the quadratic equation yields:

$$M = \frac{V_{out}}{V_{in}} \approx \frac{1 + \sqrt{1 + \frac{2 \cdot D_1^2 \cdot R_{out}}{L_{in} \cdot f_{switching}}}}{2} \tag{36}$$

The obtained sets the DC operating point with which the AC small-signal control-to-output transfer function can be acquired.

From the large-signal averaged model in DCM (Fig. 36B), a small signal perturbation is introduced. The perturbation is implemented to linearize the operation of the converter at a particular operating point (found with the DC steady-state equations) [52]. Each large-signal and small-signal perturbations are added into a single variables given by (37). From (37), the small signal perturbations variables are used to determine the input and output currents going into the power stage ports.

$$\begin{gathered} d(t) = D + \hat{d} \\ \langle v_{in}(t) \rangle_{Tswitching} = V_{in} + \hat{v}_{in} \\ \langle i_{in}(t) \rangle_{Tswitching} = I_{in} + \hat{\imath}_{in} \\ \langle v_{out}(t) \rangle_{Tswitching} = V_{out} + \hat{v}_{out} \\ \langle i_{out}(t) \rangle_{Tswitching} = I_{out} + \hat{\imath}_{out} \end{gathered} \tag{37}$$

From the perturbation variables, the input and output current are determined to be:

$$\langle i_{in}(t) \rangle_{Tswitching} = \frac{d_1^2(t) \cdot T_{switching}}{2 \cdot L_{in}} \langle v_{in}(t) \rangle_{Tswitching} \tag{38}$$

$$\langle i_{in}(t) \rangle_{Tswitching} = \frac{d_1^2(t) \cdot T_{switching}}{2 \cdot L_{in}} \frac{\langle v_{in}(t) \rangle^2{}_{Tswitching}}{\langle v_{out}(t) \rangle_{Tswitching}} \tag{39}$$

With the non-linear equations (38) and (39), the current expressions are expanded in three-dimensional Taylor series over the quiescent point (DC steady-state), and obtain the following expression:

$$\begin{aligned}\langle i_{in}(t)\rangle_{Tswitching} &= \frac{\langle v_{in}(t)\rangle_{Tswitching}}{R_e(d(t))} \\ &= f_1\big(\langle v_{in}(t)\rangle_{Tswitching}, \langle v_{out}(t)\rangle_{Tswitching}, d(t)\big)\end{aligned} \tag{40}$$

$$\begin{aligned}I_{in} + \hat{\imath}_{in} = f_1(V_{in}, V_{out}, D_1) &+ \hat{v}_{in} \cdot \frac{df_1(\hat{v}_{in}, V_{out}, D_1)}{d\hat{v}_{in}}\bigg|_{\hat{v}_{in}=V_{in}} \\ &+ \hat{v}_{out} \frac{df_1(V_{in}, \hat{v}_{out}, D_1)}{d\hat{v}_{out}}\bigg|_{\hat{v}_{out}=V_{out}} \\ &+ \hat{d} \frac{df_1\big(V_{in}, V_{out}, \hat{d}\big)}{d\hat{d}}\bigg|_{\hat{d}=D_1}\end{aligned} \tag{41}$$

From (41), the higher-order nonlinear terms are eliminated under the assumption that the small-signal perturbations are extremely small compared to the large-signal DC steady-state values [52].

$$\begin{aligned}\hat{\imath}_{in} = \hat{v}_{in} \cdot \frac{df_1(\hat{v}_{in}, V_{out}, D_1)}{d\hat{v}_{in}}\bigg|_{\hat{v}_{in}=V_{in}} &+ \hat{v}_{out} \frac{df_1(V_{in}, \hat{v}_{out}, D_1)}{d\hat{v}_{out}}\bigg|_{\hat{v}_{out}=V_{out}} \\ &+ \hat{d} \frac{df_1\big(V_{in}, V_{out}, \hat{d}\big)}{d\hat{d}}\bigg|_{\hat{d}=D_1}\end{aligned} \tag{42}$$

$$\hat{\imath}_{in} = \hat{v}_{in} \cdot \frac{1}{r_1} + \hat{v}_{out} \cdot g_1 + \hat{d} \cdot j_1 \tag{43}$$

$$\hat{\imath}_{out} = \hat{v}_{out} \cdot -\frac{1}{r_1} + \hat{v}_{in} \cdot g_2 + \hat{d} \cdot j_2 \tag{44}$$

By separating the small-signal values, an averaged switch model in DCM can be constructed as seen in (43) and (44). Fig. 39 shows the constructed model with the AC small-signal parameters. The Taylor series values are shown in TABLE 3.

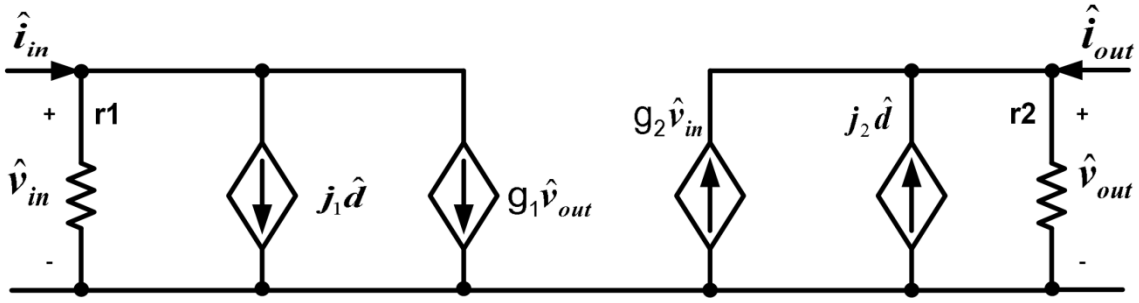

Fig. 39. AC small-signal averaged switch network model in DCM.

TABLE 3. Small-signal DCM switch model parameters

g_1	j_1	r_1	g_2	j_2	r_2
$\frac{1}{(M-1)^2 R_e}$	$\frac{2MV_{in}}{D_1(M-1)R_e}$	$\frac{(M-1)^2}{M^2}R_e$	$\frac{2(M-1)}{(M-1)^2 R_e}$	$\frac{2V_{in}}{D_1(M-1)R_e}$	$(M-1)^2 R_e$

This allows for the control-to-output transfer function to be evaluated for the converter; the transfer function is yields:

$$G_{vd}(s) = \frac{v_{out}(s)}{\hat{d}(s)}\bigg|_{\hat{v}in=0} = \frac{K_{dc}}{1 + \frac{s}{\omega_p}} \tag{45}$$

where K_{dc} is the DC gain of the converter and is given by:

$$K_{dc} = \frac{2V_{in}}{D_1(M-1)R_e} \cdot \frac{(R_{out} \cdot [(M-1)^2 R_e])}{R_{out} + [(M-1)^2 R_e]} \tag{46}$$

The system pole is set by:

$$\omega_p = \frac{R_{out} + (M-1)^2 R_e}{(R_{out} \cdot (M-1)^2 R_e) \cdot C_{out}} \tag{47}$$

The transfer function of boost converter operating in DCM exhibits a single dominant low-frequency pole. As inductor dynamics in this operating mode push an additional pole, and possibly a zero, to high frequencies, stability issues are not a main concern in DCM operating boost converters.

Fig. 40 shows the complete control loop for the inductive switching regulator scheme. It is comprised of the switching converter block (boost converter), along with a feedback factor, summation node, compensation block, and modulation block. The implementation of the feedback factor is usually performed through resistor dividers [53]. Whereas the summation and compensation blocks are implemented through a opamp-feedback arrangement [53]. Finally, the modulation block converts the compensated error signal to the driving signals needed by the converter.

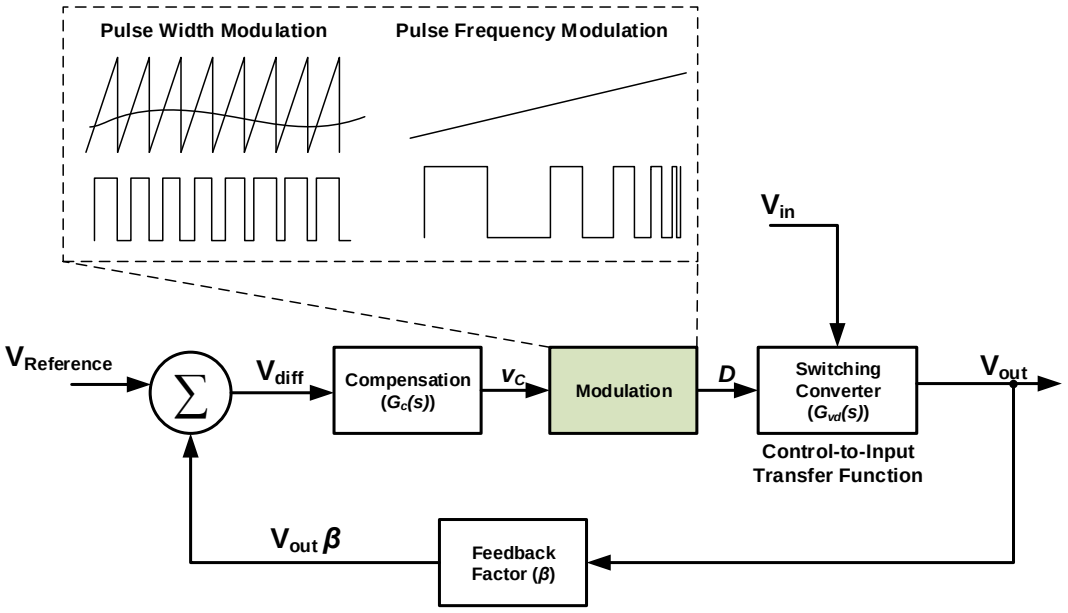

Fig. 40. Complete control loop for switching converter regulator with two different modulation implementation options: PWM and PFM.

Two major modulation schemes are shown within the modulation block: Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). Each will be described in the following sections.

Boost converter control loop for pulse width modulation

The main function of the PWM block is to produce a digital set of signals which are proportional to the analog output from the compensation block. The PWM block performs this conversion by delivering a constant frequency, variable duty cycle signal which drives the S1 and S2 switches for the switching converter (Fig. 32).

Fig. 41 shows a simplified schematic for a PWM implementation. A saw-tooth waveform generator delivers the V_{Ramp} voltage, with amplitude given by V_{pp}. The switching converter's switching frequency is determined by the V_{Ramp} signal, since this signal when compared to the compensation (v_c), sets the switching period for the driving signal D. The comparator produces a logical high level output when v_c is greater than V_{Ramp}, otherwise it is a low level output signal.

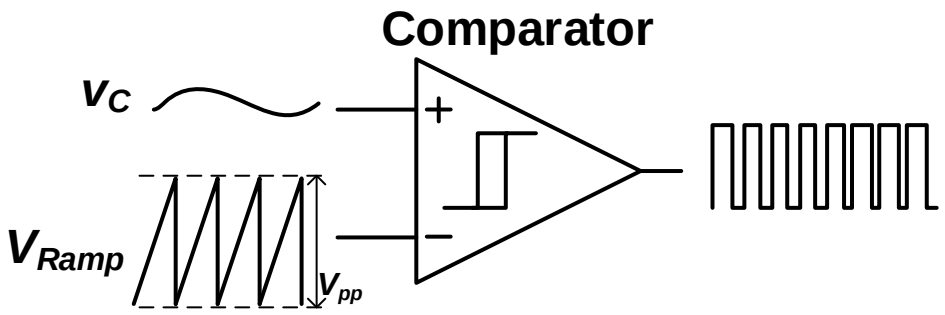

Fig. 41. Implementation of PWM scheme.

If over a switching period, V_{Ramp} varies linearly over time, and if v_c falls within the values of V_{pp}, the duty cycle signal d will be a linear function of v_c given by:

$$d(t) = \frac{v_C}{V_{pp}} \rightarrow for\ 0 \leq v_c \leq V_{pp} \tag{48}$$

Boost converter control loop for pulse frequency modulation

The implementation of PFM utilizes the same analog signal, v_c, from the compensation block but then uses this signal as a control voltage for a Voltage

Controlled Oscillator (VCO). The VCO's delivered frequency varies with the input v_c voltage [54]. The VCO, for small-signal analysis, can assume a relatively small frequency variation to v_c, so a linear gain can be safely presumed. This allows for a linear VCO model dependent on control voltage:

$$K_{VCO} = \frac{f_{switching}}{v_c} \tag{49}$$

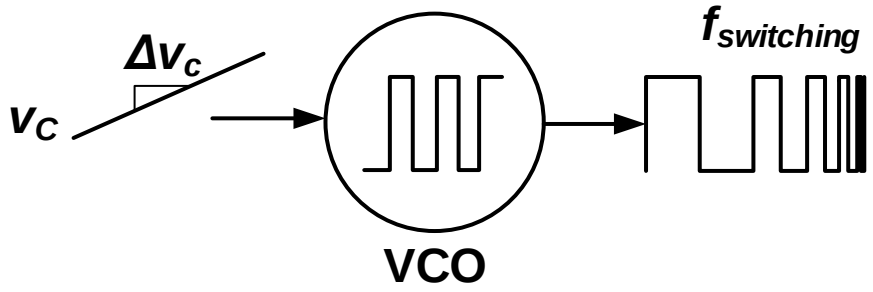

Fig. 42. Implementation of PFM scheme.

This modifies the switching converter dynamics to depend solely on $f_{switching}$ instead of duty cycle, d [55]. Due to the increased noise profile at the output voltage from the varying switching frequency, PFM is usually left for light-load applications (DCM implementations [56]). Taking into account the VCO's small-signal linear gain, new small-signal parameters are also needed to correctly model the converter with its dependency on $f_{switching}$, the variable definitions are shown in Fig. 43 and TABLE 4.

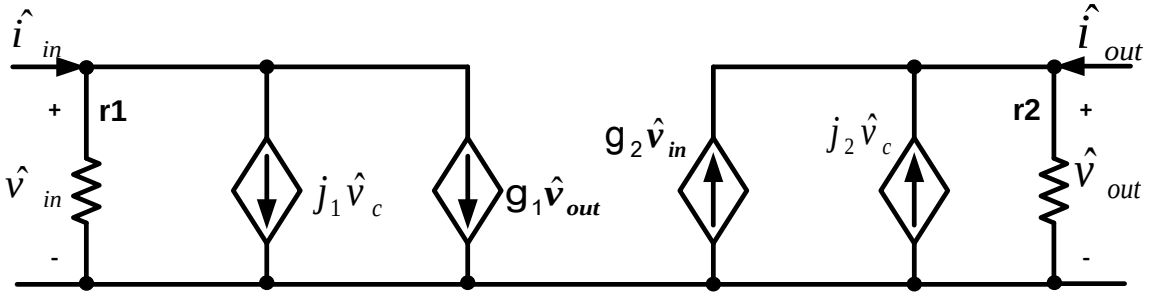

Fig. 43. AC small-signal averaged switch network model in DCM un PFM.

TABLE 4. Small-signal model parameters for boost converter in DCM under PFM.

g_1	j_1	r_1	g_2	j_2	r_2
$\frac{1}{(M-1)^2R_e}$	$\frac{MV_{in}\,K_{VCO}}{f_{sw}(M-1)R_e}$	$\frac{(M-1)^2}{M^2}R_e$	$\frac{2(M-1)}{(M-1)^2R_e}$	$\frac{K_{VCO}V_{in}}{f_{sw}(M-1)R_e}$	$(M-1)^2R_e$

$f_{sw} = f_{switching}$

From TABLE 4, a control-to-output transfer function is elaborated:

$$G_{vc}(s) = \frac{v_{out}(s)}{v_c(s)}\Big|_{\hat{v}in=0} = \frac{K_{fc}}{1+\frac{s}{\omega_p}} \tag{50}$$

where K_{dc} is the DC gain of the converter and is given by:

$$K_{fc} = \frac{V_{out}K_{Vco}}{f_{switching}} \cdot \frac{(M-1)}{(2M-1)} \tag{51}$$

The system pole is set by:

$$\omega_p = \frac{(2M-1)}{R_{out}C_{out}(M-1)} \tag{52}$$

Step-up (switched capacitor)

Due to their compact size and full integration, capacitive switching regulators (charge pumps) have found widespread application in areas such as smart phones, memories, operational amplifiers, regulators, and LCD drivers [41].

As mentioned in Chapter I, the charge pump regulator can perform step-up or step-down operation without the use of inductors to do so. Due to their implementation, charge pump applications range from fully capacitive loads to electronic loads demanding high current densities.

As shown in Fig. 23, the regulator operates in two cycles: ϕ_1 (charging of series-parallel flying capacitors) and ϕ_2 (discharging stored capacitor to output load). In order to maintain a regulated voltage at the output of the charge pump a modulation of the amount of charge being pumped from the input source is needed.

For a single stage (only 1 flying capacitor) Fig. 44 shows the dynamic behavior of the charge pump after the initial voltage step-up operation (Fig. 23) and a 50% duty cycle between ϕ_1 and ϕ_2 is assumed for the converter. During the first period, ϕ_1, the flying capacitor C_1 is connected in parallel to V_{in}. This causes C_1 to charge up to V_{in}, while the output capacitor C_{out} is discharged at a rate of $I_{out} \cdot T/2$, where T is the switching period for the converter.

$$\Delta Q_1 = C_1(V_{in} - V_1) \tag{53}$$

During ϕ_2 the switches change states and now V_{in} is connected in series to the flying capacitor, allowing for part of the charge stored in C_1 to be transferred to the output load (C_{out} and I_{out}). Depending on the demand of output current (I_{out}), the output voltage will rise sequentially through a series of charge steps until a steady-state operational value is achieved [41] yielding:

$$\Delta Q_2 = I_{out}T \tag{54}$$

or:

$$V_{out,st-st} = 2V_{in} - \frac{I_{out}T}{C_1} \tag{55}$$

The expression in (55) can be further extended to *N* number of stages in the charge pump.

$$V_{out,st-st} = (N+1)V_{in} - N\frac{I_{out}T}{C_1} \tag{56}$$

As the charge pump must deliver the same packet of charge throughout the entire charge chain to maintain an average DC output voltage, the same amount of charge consumed at the output ($I_{out}T$) during one phase must be supplied by the complementary phase. Due to this output voltage increase and decrease due to I_{out}, an output voltage ripple V_r is seen.

$$V_r = \frac{I_{out}T}{C_{out}} \tag{57}$$

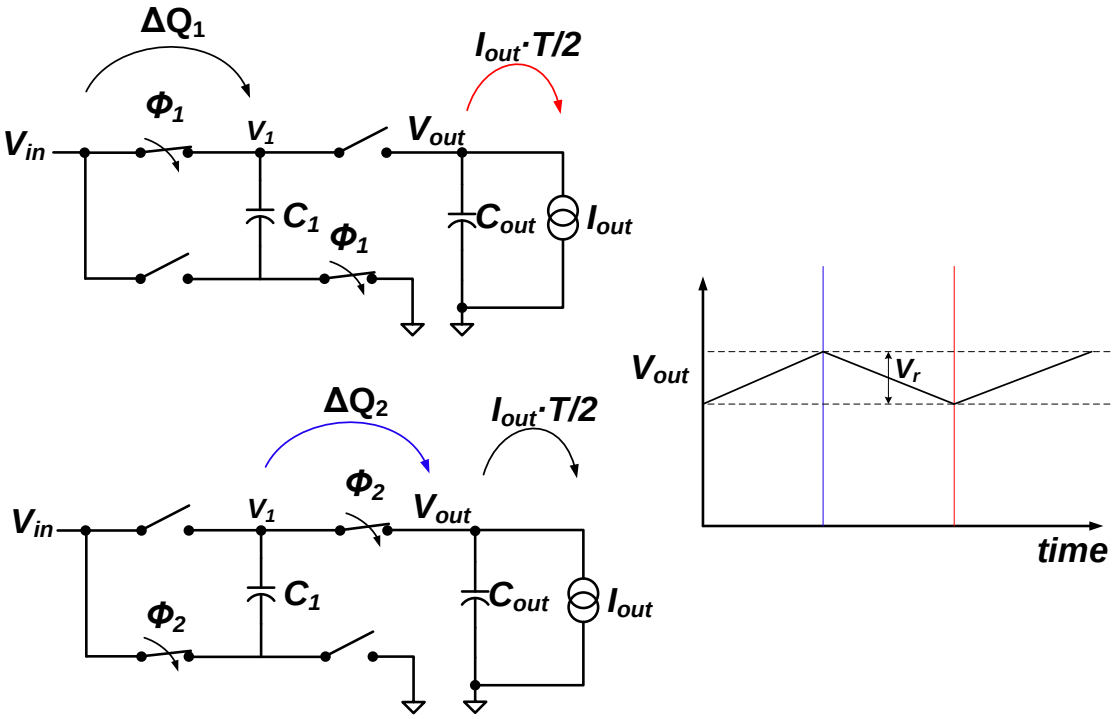

Fig. 44. Dynamic behavior of charge pump.

Switch implementation have ranged from diodes to MOSFETs connected as diode fashion [57, 58] as technology processes have matured. Nonetheless, these approaches were limited to the forward bias drop of the diode and voltage drop in the diode connected MOSFET; increasing the required charge to be transferred to the output load with each cycle. Bootstrap switch implementations can also be implemented in order to minimize the voltage drop across the switches [59], improving overall efficiency. Fig. 45 shows both implementations with diodes, MOSFETS, and bootstrapped switches in the capacitive switching regulator.

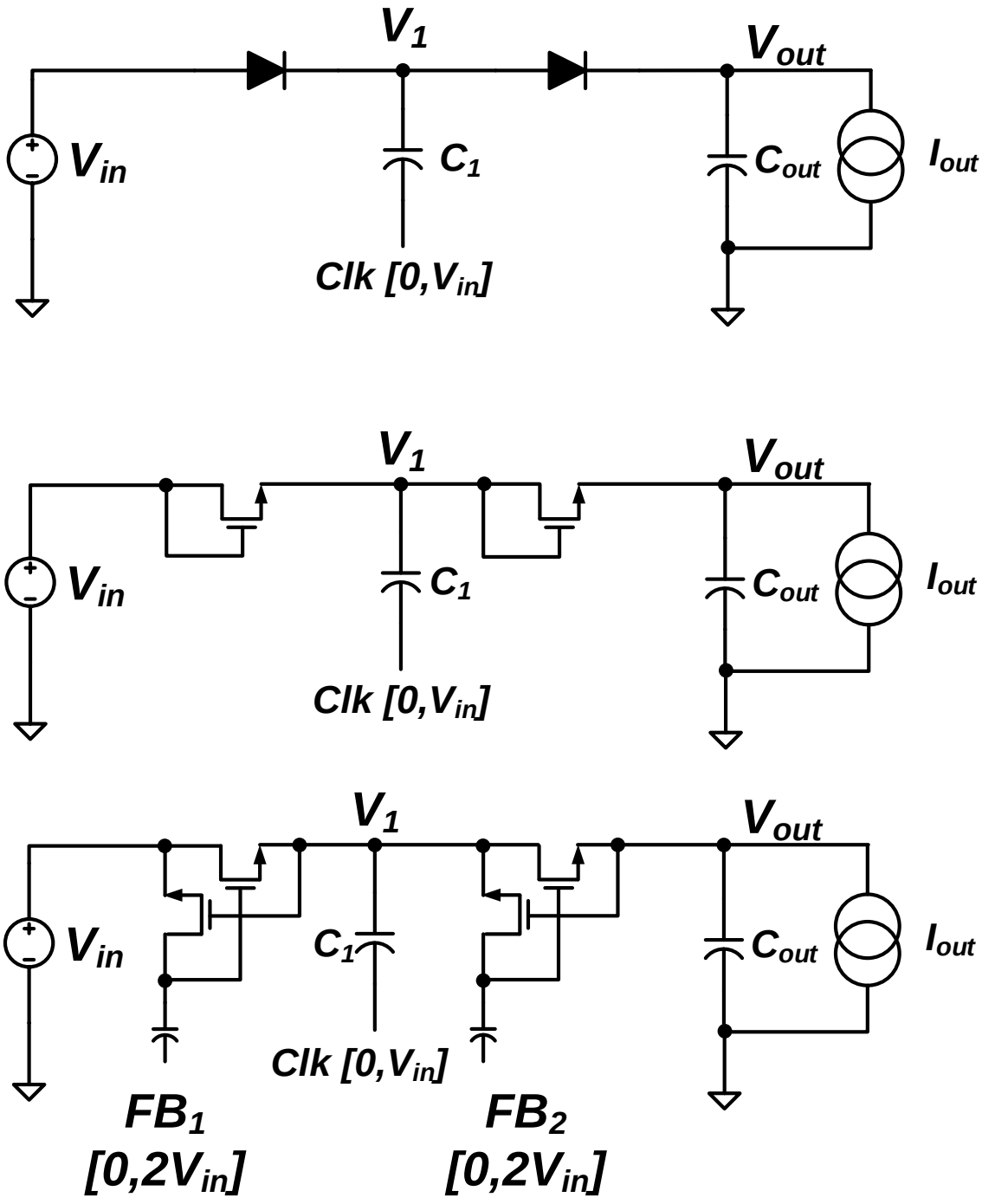

Fig. 45. Diode, MOSFET, and bootstrap switch schemes for charge pump implementations.

Small-signal AC transfer functions for the charge pumps are required for proper regulation. Both duty cycle and switching frequency dependent control variable analysis can be performed. Although the analysis presented in [60] is for a LC based switching converter, its application to other topologies is equally valid as it is a derivation of the classical approach of state-space averaging [61]. From Fig. 46, the transfer function is obtained by solving for the time domain transient response in both the charging and discharging phases taking into account the on-resistances of the switches. From both charging and discharging equations, an averaged model is obtained:

$$C_{out}\frac{d\mathrm{V_{out}}}{dt} = \left(-\frac{V_{out}}{R_{out}}\right)(\mathrm{T_{on}\ F_{sw}}) + \left(\frac{V_{in}+V_1-V_{out}}{R_{on}} - \frac{V_{out}}{R_{out}}\right)(\mathrm{T_{off}\ F_{sw}}) \tag{58}$$

For duty cycle control, (58) can be made to match $\hat{d}$ as the control variable:

$$C_{out}\frac{d\mathrm{V_{out}}}{dt} = \left(-\frac{V_{out}}{R_{out}}\right)(D_1) + \left(\frac{V_{in}+V_1-V_{out}}{R_{on}} - \frac{V_{out}}{R_{out}}\right)(D_2) \tag{59}$$

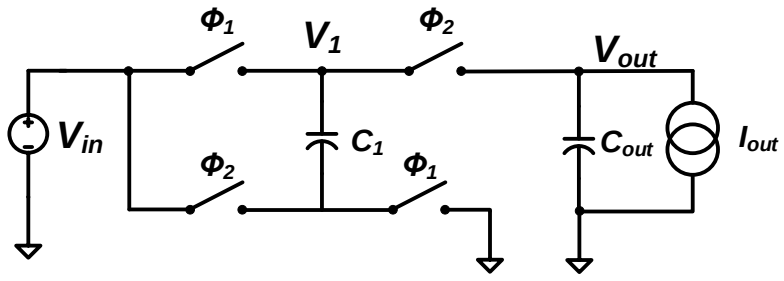

Fig. 46. Single stage switched capacitor converter with associated capacitor voltages.

By assuming a 50% duty cycle, i.e. $\phi_1 = \phi_2$ ($D_1 = D_2$), the DC solution is obtained from the steady-state DC equations for frequency modulation:

$$\begin{aligned} C_{out}\frac{d(V_{out}+\hat{v}_{out})}{dt} &= 0 \\ &= \left(-\frac{V_{out}+\hat{v}_{out}}{R_{out}}\right)\left(T_{on}(F_{sw}+f_{sw})\right) \\ &+ \left(\frac{V_{in}+(V_1+\hat{v}_1)-(V_{out}+\hat{v}_{out})}{R_{on}}\right. \\ &\left.-\frac{V_{out}+\hat{v}_{out}}{R_{out}}\right)\left(T_{off}\ (F_{sw}+f_{sw})\right) \end{aligned} \tag{60}$$

As well as duty cycle modulation:

$$\begin{aligned} C_{out}\frac{d(V_{out}+\hat{v}_{out})}{dt} &= 0 \\ &= \left(-\frac{V_{out}+\hat{v}_{out}}{R_{out}}\right)\left(D+\hat{d}\right) \\ &+ \left(\frac{V_{in}+(V_1+\hat{v}_1)-(V_{out}+\hat{v}_{out})}{R_{on}}\right. \\ &\left.-\frac{V_{out}+\hat{v}_{out}}{R_{out}}\right)\left(D+\hat{d}\right) \end{aligned} \tag{61}$$

Eliminating both DC and nonlinear terms (second order effects), as well as setting the input voltage to AC ground greatly simplifies analysis and the acquisition of the effect of both the switching frequency and duty cycle on the control-to-output voltage transfer function after including the effect of the oscillator linear gain.

$$G_{vd}(s) = \frac{v_{out}(s)}{d(s)}\Big|_{\hat{v}in=0} = \frac{-2V_{out}R_{on}}{s(C_{out}R_{out}R_{on}) + D(R_{out})} \tag{62}$$

$$G_{vc}(s) = \frac{v_{out}(s)}{v_c(s)}\Big|_{\hat{v}in=0} = \frac{-V_{out}R_{on} \cdot K_{VCO}}{s(C_{out}R_{out}R_{on}) + (R_{out})} \tag{63}$$

Switched capacitor control loop for pulse width modulation

Following the same control loop shown in Fig. 40, the same modulation methods are available for the switched capacitor regulator. In order for the implementation of a PWM control scheme a charging profile is implemented by varying the duty cycle of one of the phase switches $\phi_{1,2}$. Fig. 47 shows how the secondary switch for the ϕ_1 cycle modulates the amount of current being pulled from the input source; hence, limiting the charge being transferred from the input source to the output load.

While modifying the duty cycle of the charge being dumped into C_1 allows for a degree of control, it is limited to a maximum duty cycle of 50% [62]. Any increase in duty cycle for ϕ_1 beyond 50% negatively affects the charge delivering capability of the system as not unbalanced charge transfer takes place in the converter, further complicating linearizing dynamics.

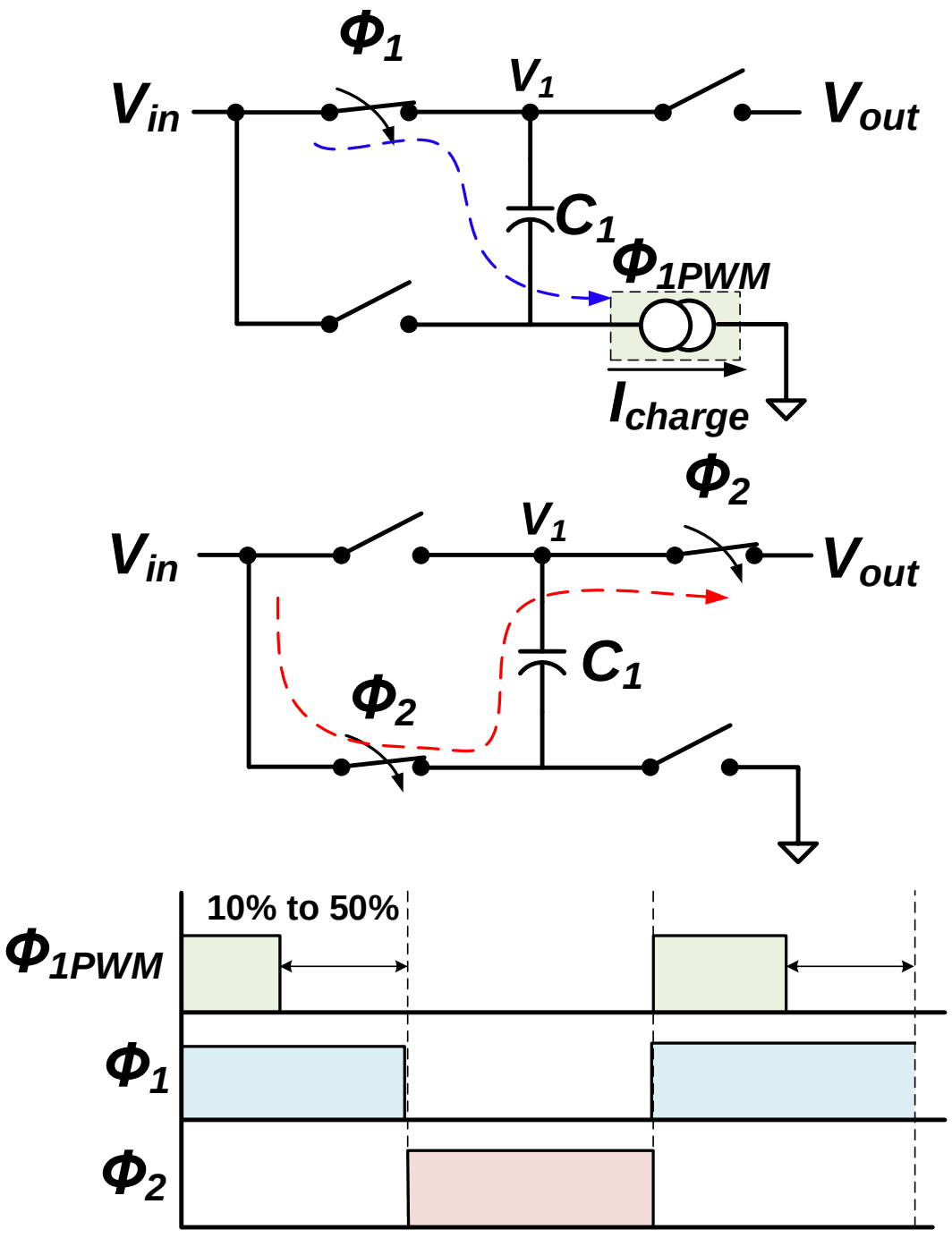

Fig. 47. Charge pump PWM implementation.

If the requirements of the load fall within the regulators capabilities with duty cycle modulation, the PWM control loop can improve both speed (bandwidth) and accuracy through the compensation block implemented (Fig. 40). The implementation of the variable duty cycle block is the same as the one implemented for the inductive switching regulator (boost converter).

Switched capacitor control loop for pulse frequency modulation

The implementation of variable control frequency in PFM is a commonly used method in switched capacitive regulators [63-65]. The variable switching frequency allows for a rapid and accurate voltage regulation mechanism, within the limits of the output resistance of the regulator, expressed in (23) in Chapter I.

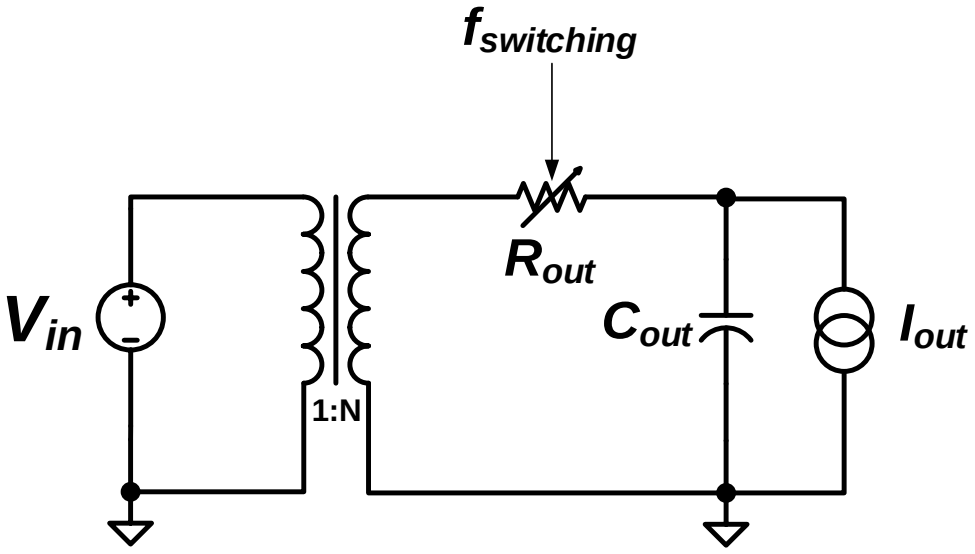

Fig. 48. PFM behavioral model for step-up operation.

Fig. 48 represents the PFM behavioral model of the charge pump. Implementations utilizing bootstrapped switches usually require and additional number of phases (4 phase non-overlapping clock) to synchronize the turning on-off of the bootstrap switches prior to the main switches.

Fig. 49 shows the output resistance variations with both number of stages and switching frequency of the regulator. The output capacitor, C_{out}, is set to 1 μF. As the plot shows, as the number of stages increases (N) the range over which the output resistance can vary is reduced. Causing load current variations to be limited to number of stages if any one particular frequency is to be set.

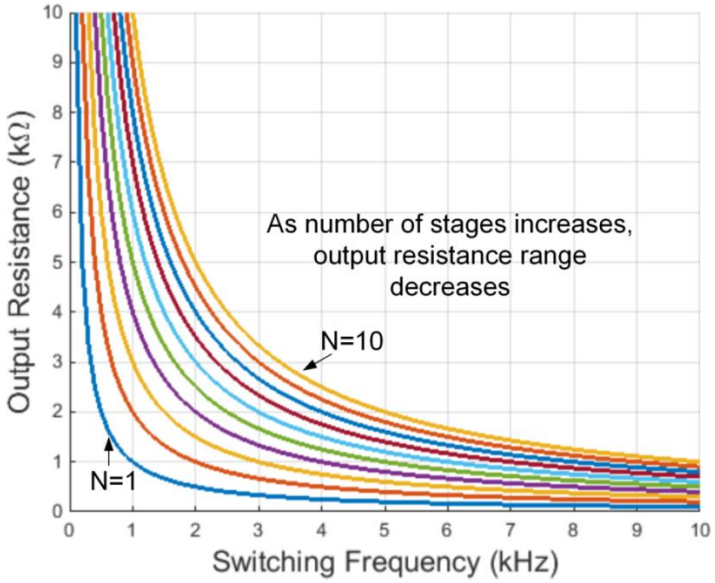

Fig. 49. Output resistance with variable switching frequency and number of stages.

Performance comparison

As both topologies offer their own benefits and disadvantages, a comparison between both regulator types is presented.

Voltage gain ratio

As presented in both Chapters I and II, the voltage gain capabilities for inductive and capacitive are performed via the storing and delivering of energy through complementary cycles. The stored energy is kept in reactive components, allowing for variable amounts of charge to be deposited.

As the capacitive switching regulator is limited by both frequency and number of stages, and the applications for which both regulators will be applied for are in energy harvesting approaches, light-load conditions for both converters will be assumed.

For the inductive regulator the DCM operation is assumed, setting the voltage gain to be given by (36). And for the capacitive regulator, since the voltage gain is mainly limited by both load current and number of stages, the ratio is determined by (56).

Fig. 50 shows how both converters' voltage gain is varied with duty cycle and number of stages for the boost converter and charge pump, respectively. Both converters were set to a switching frequency of 1 MHz, and an input voltage of 1 V. The boost converter was also set with an input inductance of 100 μH, whereas the charge pump was set to have 200 pF capacitors per stage.

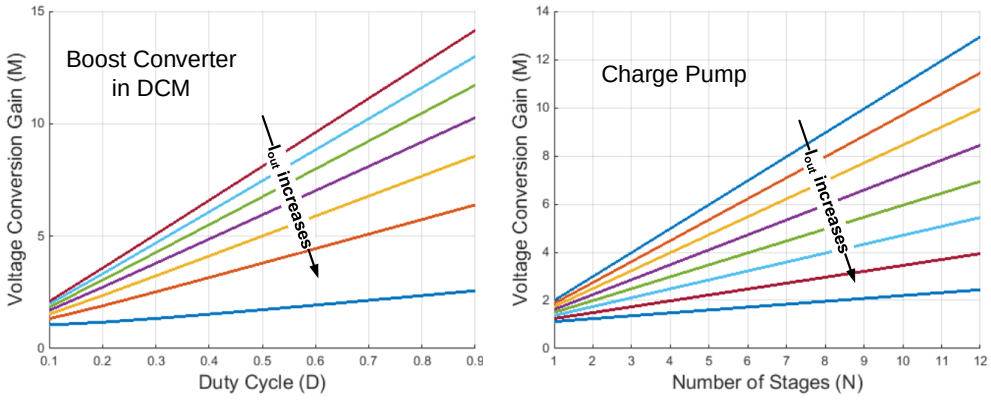

Fig. 50. Voltage conversion ratio for both regulators under light-load conditions.

As can be seen, the main limitation in terms of voltage gain for both topologies lies in output current demands. As increases in load current will cause the boost converter to begin operating in CCM/DCM boundary, and the voltage gain drops, the same occurs with the charge pump as the output current demand increases.

In order to increase M for both regulators with high I_{out} demands, the boost converter will need to a lower valued inductor and the charge pump a higher valued flying capacitor per stage.

Power efficiency

Both regulators possess competitive efficiencies under the light-load regime. The boost converter's efficiency is mainly limited to the conduction losses present in the on-resistance of both switches and input inductor as the light-load specification allows for smaller MOSFET switches to be implemented, reducing the overall switching losses $(^1/_2 \cdot C_{gate} \cdot V_{drive}^2 \cdot f_{sw})$.

The efficiency expression is then given by:

$$\eta_{Boost} = \frac{P_{input} - (P_{NMOS} + P_{PMOS} + P_{inductor})}{P_{input}} \tag{64}$$

where

$$P_{NMOS} = R_{NMOS} \cdot D_1 \cdot \left(\frac{I_{out}}{1 - D_1}\right)^2 \tag{65}$$

$$P_{PMOS} = R_{PMOS} \cdot D_2 \cdot \left(\frac{I_{out}}{1 - D_2}\right)^2 \tag{66}$$

$$P_{inductor} = R_{Lin} \cdot \left(\frac{I_{out}}{1 - D_1}\right)^2 \tag{67}$$

Assuming low valued DC resistance for the inductor, the switches become the main efficiency limitation for DCM boost converter topologies.

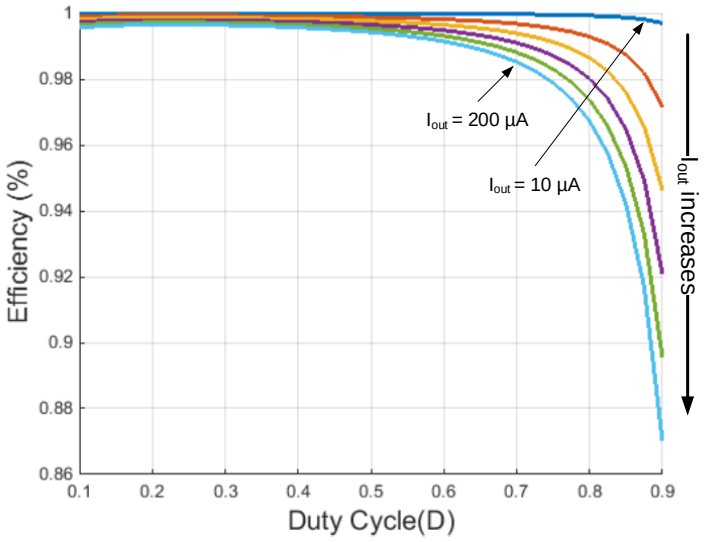

Fig. 51. Power efficiency for boost converter with variable duty cycle and increasing output load current in DCM.

For the charge pump's efficiency several assumptions can be made. Whenever diodes or MOSFET connected diodes are replaced by active switching, the main loss factor in charge pumps become the parasitic capacitance of the used flying capacitors [66]. This leaves the following expression for overall efficiency of the converter:

$$\eta_{charge} = \frac{V_{in} \cdot I_{out} \cdot (N+1) - \frac{N\, I_{out}^2}{f_{sw} \cdot C_{stage}}}{V_{in} \cdot I_{out} \cdot (N+1) + \alpha \cdot C_{stage} \cdot f_{sw} \cdot V_{in}^2} \tag{68}$$

where α is the parasitic to main capacitance value ratio for each stage flying capacitors [67].

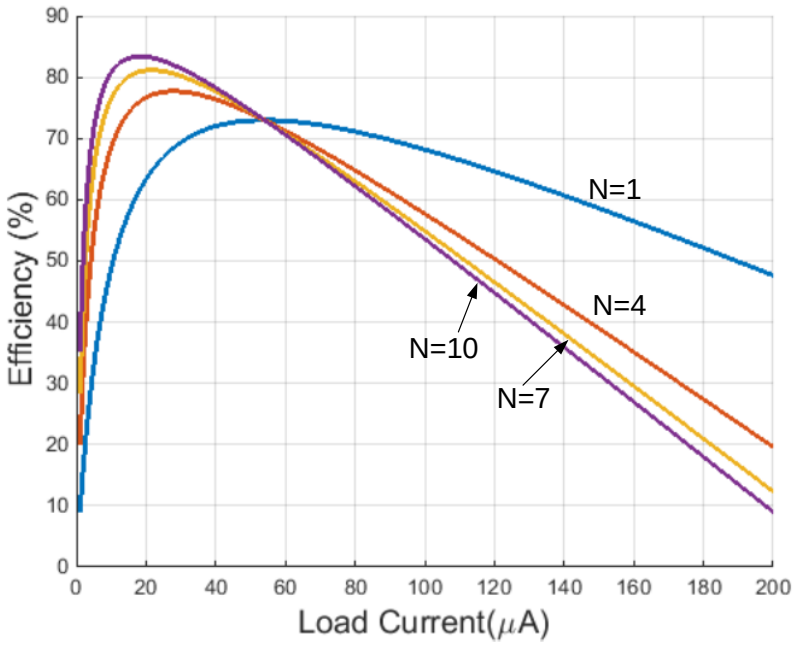

Fig. 52. Power efficiency for charge pump with variable load current and increasing number of stages.

Both regulator topologies offer benefits at low and high current load demands and integration capability; where the boost converter displays overall better efficiency, but limited integration options.

Integration

It is in this aspect where the capacitive switching regulator allows for a fully monolithic approach. Current technology processes allow for high capacitance density per area (F/μm^2) where flying capacitors above 150 pF are achievable [42, 68]. Nonetheless, as expressed in (68), the efficiency is affected by the capacitance ratio of the parasitic capacitance to implemented capacitor ($\alpha = C_{parasitic}/C_{stage}$). Fig. 53 shows a cross section of the implementation of Metal-Insulator-Metal (MIM) capacitor.

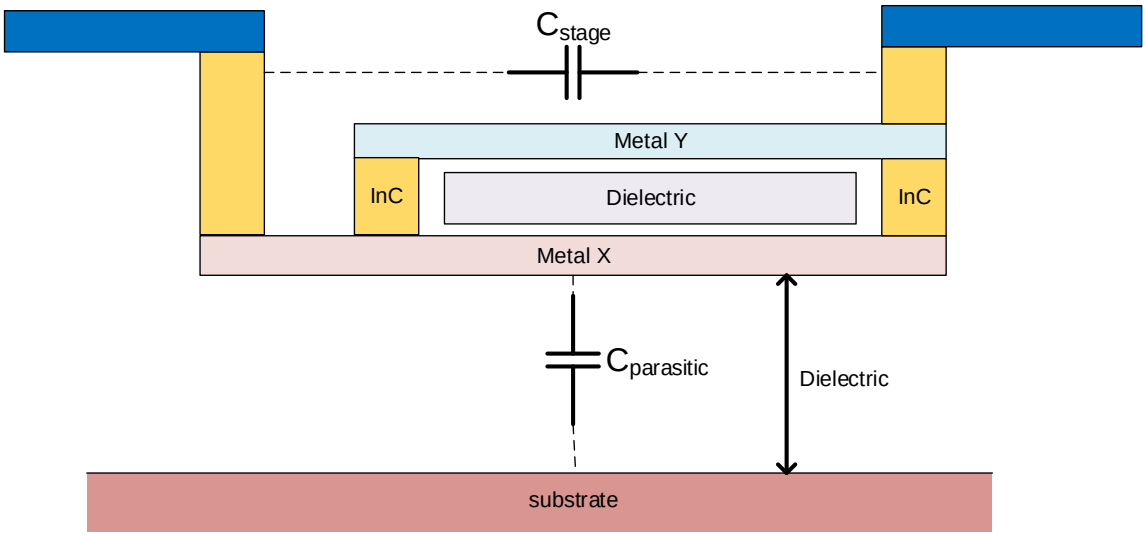

Fig. 53. Parasitic capacitance for on-chip capacitors implemented for charge pumps.

The main capacitor is formed with metals Y and X for C_{stage}; the issue arises with the $C_{parasitic}$ element from Metal X to the substrate. The more distance between the bottom plates (Metal X) to the substrate the lower the value for parasitic capacitances.

Other capacitor creation methods for on-chip processes have also been explored: on-chip trench capacitors [69] or metal finger capacitors [70]. These implementations are limited to special process technologies which are able to offer such types of capacitors.

For the boost converter the main focus is to minimize the off-chip inductance by integrating the magnetic component on-chip. Although efforts to present integrated inductors through top metal coils on-chip of use of bond-wire for inductor purposes [71-74], they are limited to low quality factor designs for light-load demands and require high switching frequencies to take full advantage of the storing capabilities of the inductor.

Trade-offs

As has been shown throughout this chapter, both regulator topologies offer a voltage regulation capability to the output. Where the switched capacitor regulator offers higher integration capability, the switched inductive regulator possesses inherently higher efficiency and higher power delivery capabilities. TABLE 5 shows a comparative view of both regulator topologies.

TABLE 5. Comparison table for both regulator topologies presented.

	Switched Capacitive Regulator	Switched Inductive Regulator
Topology Complexity	High (for multistage regulators)	Low
Control Implementation	Medium	Medium
Footprint	Small	Large (due to off chip inductor)
Efficiency	Low (At high current demands)	High
Output current	Low	High

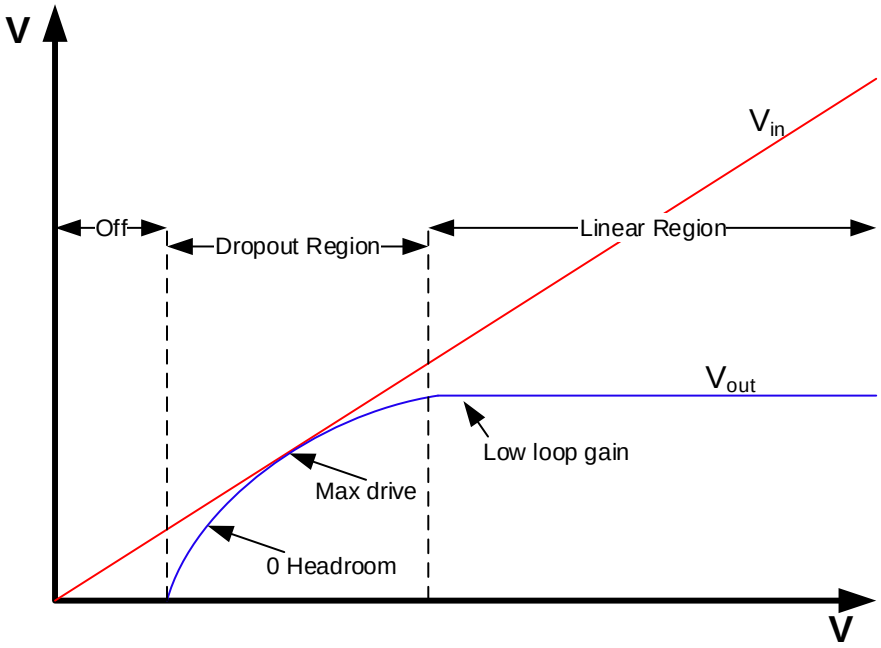

Fig. 54. Input-output voltage characteristic of Linear regulator.

Linear regulators

As mentioned in Chapter I, linear regulators achieve DC-DC voltage conversion by dissipating excess power into a resistive element; essentially making these regulators resistive dividers. Utilizing active devices as the dissipating element, the output voltage is set through a control loop which varies the active devices on resistance. A linear regulator has three operational regions: off, dropout region, and linear operation, Fig. 54 illustrates presents the regions and their typical characteristics.

It is during the linear region where the regulator operates and fixes the output voltage with a finite and non-zero loop gain. Decreasing V_{in} causes the pass device to enter its linear (MOSFET) or saturation (BJT) region in which the gain of the active pass device is low. The regulator still operates, although with minimum loop gain, causing DC errors in the regulated value of V_{out}.

Decreasing V_{in} even further causes the system to enter the dropout region, which is where the regulator operates at its driving limit. The pass device still supplies as much current in order to keep V_{out} regulated. Additional decreases in V_{in} forces the regulator to be unable to maintain regulation at all.

Low dropout regulators

Low dropout regulators (LDO) are made up of a control loop which senses the output voltage in order to maintain the output voltage constant, within a specific tolerance level. They appear in two different topologies: source-follower/common-collector and common-source/common-emitter.

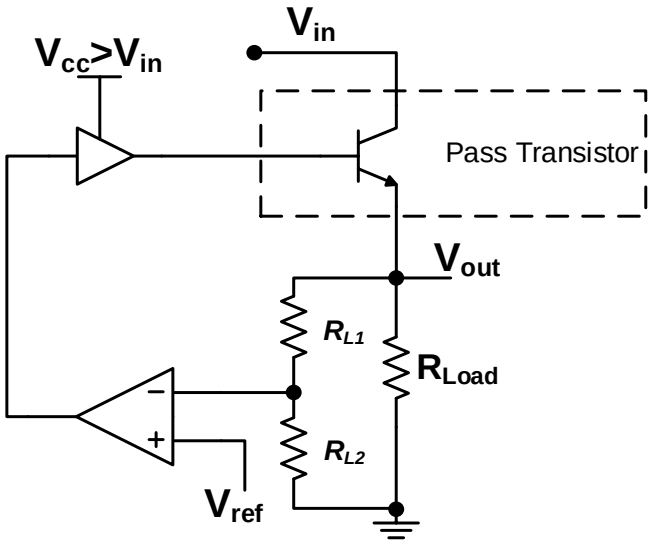

Fig. 55. Common-collector LDO topology with NPN active device.

Fig. 55 illustrated a block level composition of a common-collector LDO topology with NPN transistor as the pass device. This type of regulator requires base driving voltages in excess of the input voltage in order to fully drive the device for high current demands. The common-collector topologies are present in low-voltage applications [75], but require the implementation of charge pump converters to deliver the appropriate base driver levels. The main common-collector topology efficiency under ideal conditions yields:

$$\eta_{LDO} = \frac{V_{in} - V_{out}}{V_{in}} = \frac{V_{dropout}}{V_{in}} = 1 - \frac{V_{out}}{V_{in}} \tag{69}$$

It is the common-source/common-emitter voltage regulator topology that overcomes the high gate voltage requirements from the source-follower regulator; by setting the V_{DS}/V_{CE} voltage of the active device as the main parameter that limits the

regulator operation. In the MOSFET instance, it is the dropout voltage (V_{DSAT}) which limits the output current and size of the pass device.

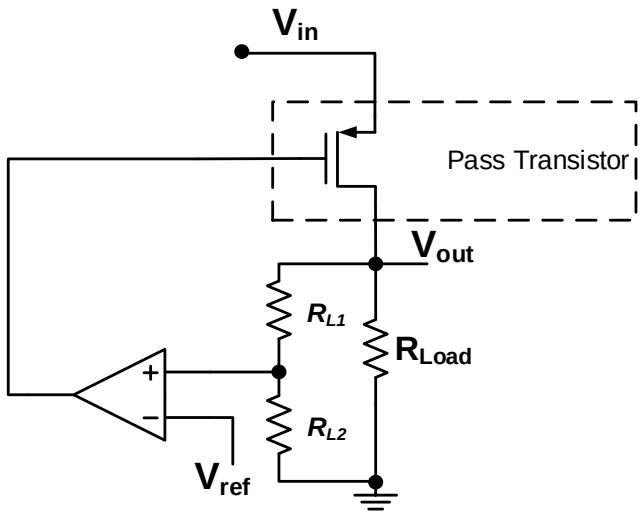

Fig. 56. Common-source LDO topology with NMOS active device.

Fig. 56 shows the common-source topology of the LDO. The main difference between the PNP and PMOS implementation of this topology is the use of much reduced quiescent current by the PMOS, which in turn increases the drive portability, battery operation, and overall reduced power consumption [76].

Principles

The LDO is fully comprised of a voltage reference, error amplifier, a pass transistor, and a feedback network (Fig. 55 and Fig. 56). The feedback network senses the output voltage, delivering a fraction of the output voltage the error amplifier. The

error amplifier then compares and generates an error signal that drives the pass device and regulates the output voltage.

The output voltage of the regulator is set through both the reference voltage and ratio of feedback resistors. This is determined for an ideal error amplifier as:

$$V_{out} = \left(1 + \frac{R_{L1}}{R_{L2}}\right) V_{ref} \tag{70}$$

A second critical aspect in the regulator design is the pass device dimensions. The dimensions set the maximum amount of current the regulator can deliver to the load. The pass device dimensions are usually large in order to deliver enough current for the application:

$$\frac{W}{L}_{PASS} = \frac{2 \cdot I_{Pass}}{\mu_X C_{OX} (V_{GS} - V_T)^2} \tag{71}$$

where I_{Pass} is the current through the pass device, μ_x the mobility of electrons/holes, C_{OX} the oxide capacitance, V_{GS} the gate to source voltage difference and V_T the threshold voltage.

The main downside of having a large pass device is the associated parasitic capacitances. These parasitic capacitances cause an unwanted time delay whenever load event occurs, charging-discharging these capacitances requires additional charge to fully enhance the depletion channel generated by the pass device.

Each pass device topology has their associated stability requirements. While the source-follower/common-collector topology possesses an inherently stable response, due to its low output impedance; only two poles are within the bandwidth of interest: the dominant P_1 generated by the error amplifier driving stage's output impedance ($\omega_{p1} = 1/(R_{out}C_{pass})$), and the secondary pole P_2 generated with the load impedance and emitter/source impedance. Fig. 57 shows the typical small-signal response for this topology.

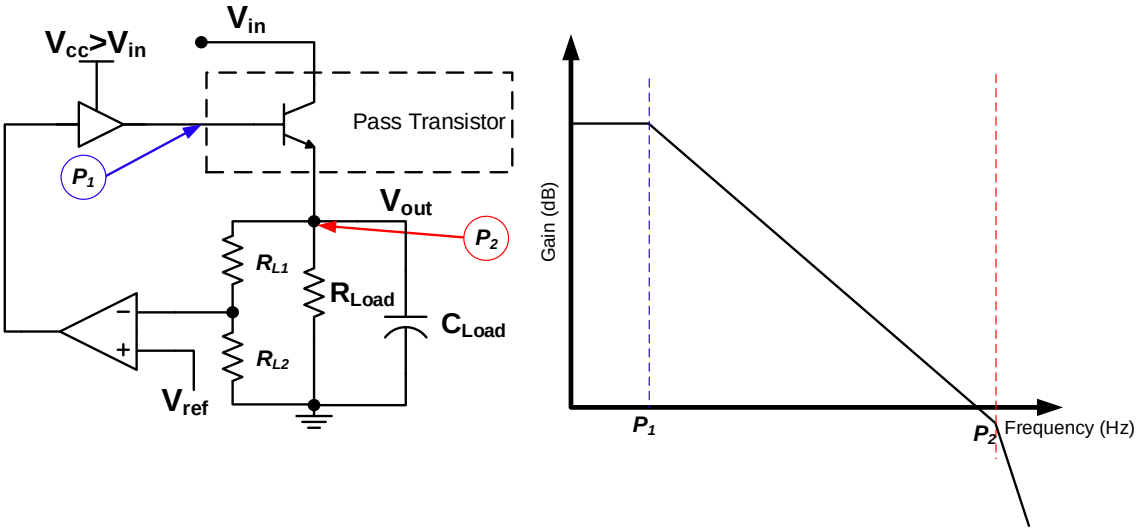

Fig. 57. Small-signal pole locations for source-follower topology.

For the common-source/collector topology stability is a prime concern as the output capacitor and high output impedance of the pass device set the dominant pole of the regulator at the output node.

This causes the dominant pole P_1 ($\omega_{p1} = 1/(R_{out}C_{pass})$) to come in close proximity to the pole located at the output of the error amplifier P_2 ($\omega_{p2} = 1/(R_{Load}C_{Load})$). This requires external or internal compensation of the regulator in order to correctly operate. Fig. 58 shows the typical small-signal response for this topology.

Different approaches have been sought out to stabilize this topology ranging from taking advantage of the load capacitor's ESR, external or internal creation of small-signal zero responses, or eliminating the external capacitor altogether through multiple loop configuration to ensure stability over wide current and capacitance loads [77, 78].

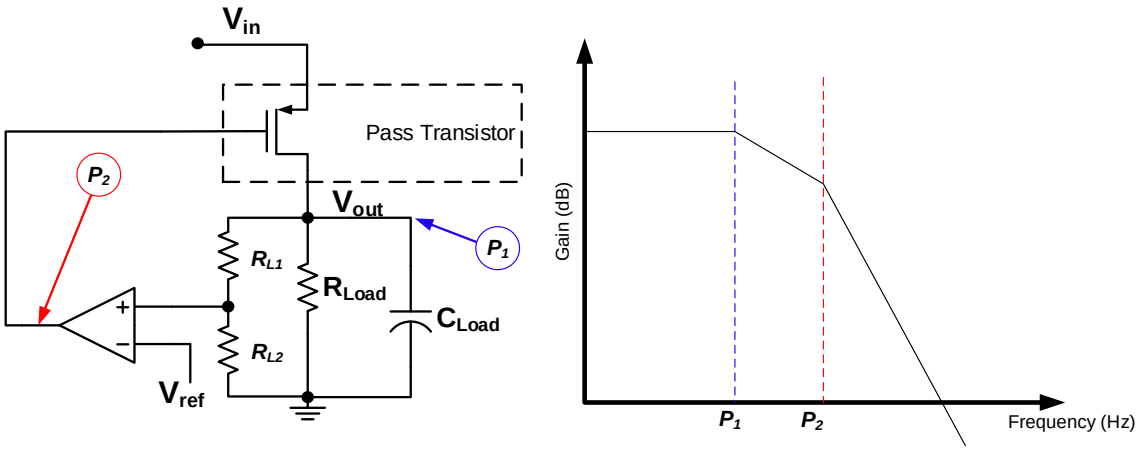

Fig. 58. Small-signal pole locations for common-source topology.

Digital LDO approach

So far the presented solutions have shown the behavior of LDO regulators with analog approaches. The same implementation can be taken into the digital domain and perform the regulation qualities through fully digital means.

Going back to the principle of operation of a linear regulator, we can see that the main purpose of the system is akin to a resistive divider. In an analog LDO, this is performed by modifying an active device's transconductance to achieve the required output voltage over load current demands. Stability, power consumption, and speed are a major set of concerns for analog LDOs. The same regulating properties can be achieved by digital means as well. As the dropout voltage for a device is dependent on pass device dimensions, a fragmented pass device into multiple single units can also mimic the effect of an analog voltage driving a single large device, this is better shown as follows:

$$I_{Di} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_i \left(V_{gs} - V_{th}\right)^2 \tag{72}$$

It is through the $\left(\frac{W}{L}\right)_i$ ratio that the current load demand is met and voltage regulation achieved. Fig. 59 shows an overall view of a Digital LDO implementation with multiple pass devices making up the single pass device from the analog LDO approach.

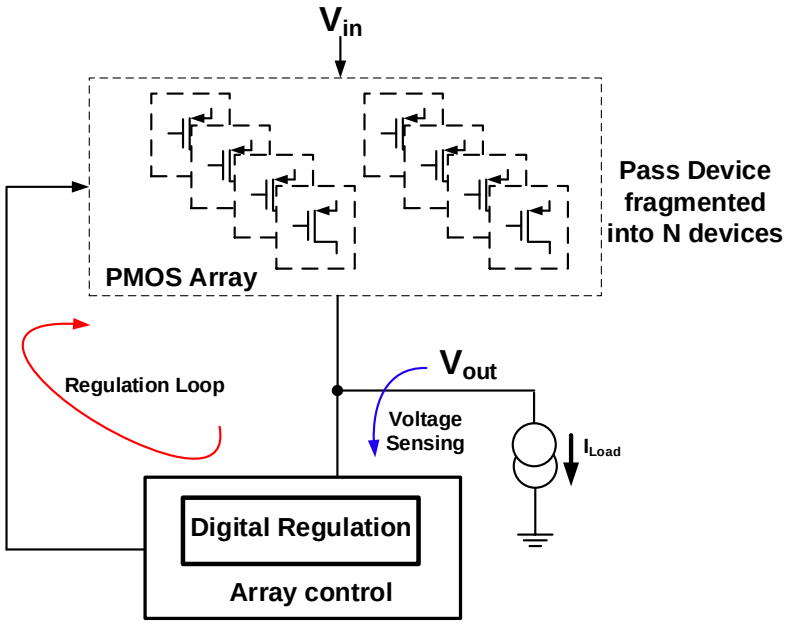

Fig. 59. Digital LDO implementation with PMOS array for pass devices.

The means by which the digital LDO approach is achieved is through a digital control loop implemented in the voltage domain. Fig. 60 shows a simple implementation for a digital LDO controller in voltage domain. The controller is comprised of a comparator, up/down counter, and N-bit decoder [79]. The decoder number of bits is dependent on the number of fragmented pass device units. As a load current demand occurs, the output voltage would fall due to the insufficient driving current from the pass device. This would make the comparator trigger the event and increase the number of pass devices turned on, increasing the driving current to the load. The opposite effect would occur (decrease number of units in pass device) whenever less current is required.

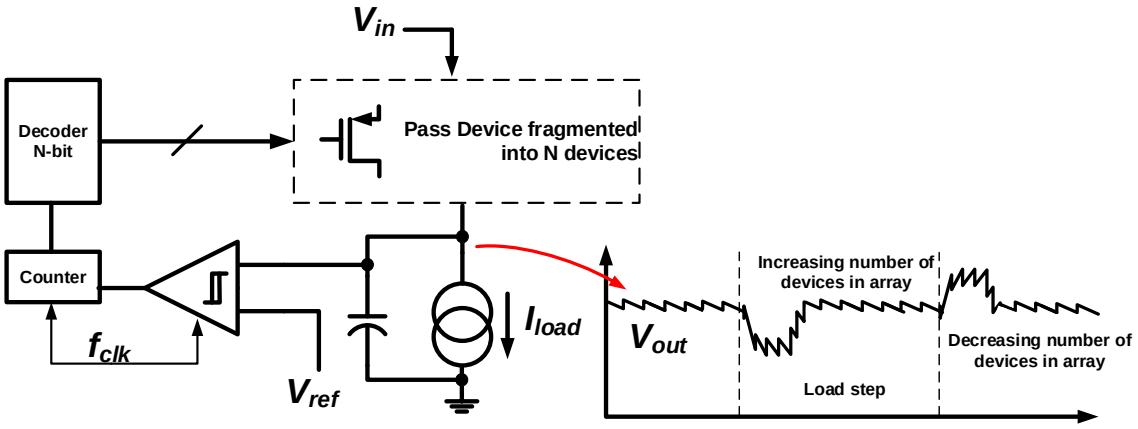

Fig. 60. Voltage domain controller for digital LDO implementation.

This topology also has an additional clocked signal to synchronize the entire operation between the counter and decoder. This makes the clock frequency, f_{clk}, the main performance variable to optimize the system performance. Low f_{clk} allows for a much improved efficiency, reducing dynamic power consumption, but causing higher load regulation errors. This is caused by the reaction time between the comparator and counter to load current events. Higher f_{clk} reduces the load regulation error, but increases the amount of power consumed by the system. A careful trade-off between load error and system efficiency exist in digital LDO implementations.

Performance comparison and state-of-the-art

Digital LDO implementations were sought after as a solution to power management in deep submicron technology; processes where dynamic power consumption were minimal due to small size devices. Although not as robust as an analog LDO implementation, the digital counterpart offers lower power consumption, and almost synthesizable approach to design.

TABLE 6 presents current state-of-the-art design implementing digital LDO systems for voltage regulation. Due to the switching nature of the digital LDO (adding and subtracting pass device units), Power Supply Rejection (PSR) is not a parameter included in most designs.

TABLE 6. Comparison table with state-of-the-art digital LDO implementations.

	[79]	[80]	[81]	[82]
Technology	40 nm	90 nm	65 nm	40 nm
Minimum V_{in}	0.9 V	2.4 V	0.5 V	1.34 V
V_{out}	1 V	1.2 V	0.45 V	1.2 V
Minimum Dropout voltage	100 mV	1.2 V	50 mV	1.4 V
Output Capacitor	None	None	None	None
Current Consumption	50 nA	25.7 mA	2.7 μA	130-100 nA
Active area	0.08 mm^2	0.03 mm^2	0.042 mm^2	0.057 mm^2
Efficiency	99.90%	97.50%	98.70%	96-99.9 %

As technology continues to decrease in size and multiple voltage domains will be required on-chip, smaller and more power efficient voltage regulators will be required. Digital LDOs offer a solution for this dilemma by offering a quick and robust regulator with minimum variable components. Combinations of types of converters can be used to operate together and deliver multiple voltage domains for a full System on Chip (SoC) operation.

CHAPTER III

A BOOST CONVERTER WITH DYNAMIC INPUT IMPEDANCE MATCHING FOR DC ENERGY HARVESTING SOURCES*

Introduction

One of the most critical aspects in wireless sensor nodes is the limited available energy on the system from onboard batteries. As systems continue to increase in power density, battery life lags behind these needs. One possible solution lies in energy harvesting (EH), which presents itself as a means of increasing battery life and sustaining up-time for the wireless sensor node to a theoretical never-ending power supply [18, 83-87]. Energy processing circuits designed to work at ultra-low power levels have been developed for a variety of energy sources such as vibrational, solar, radio frequency, and thermal. A thermoelectric generator (TEG) delivers a voltage, V_{TEG}, that is proportional to the difference of the temperatures applied to each side of the device. The resulting voltage output magnitude varies over a wide range as a function of the temperature gradients applied.

Previous reports on EH power management units (PMU) for TEGs [17, 20, 88-90] have focused on harvesting energy from single TEG units utilizing boost converters (BC). Although these reported systems have shown good efficiency for single units, no efforts have been made to utilize TEGs placed in a multiple array fashion. A recent

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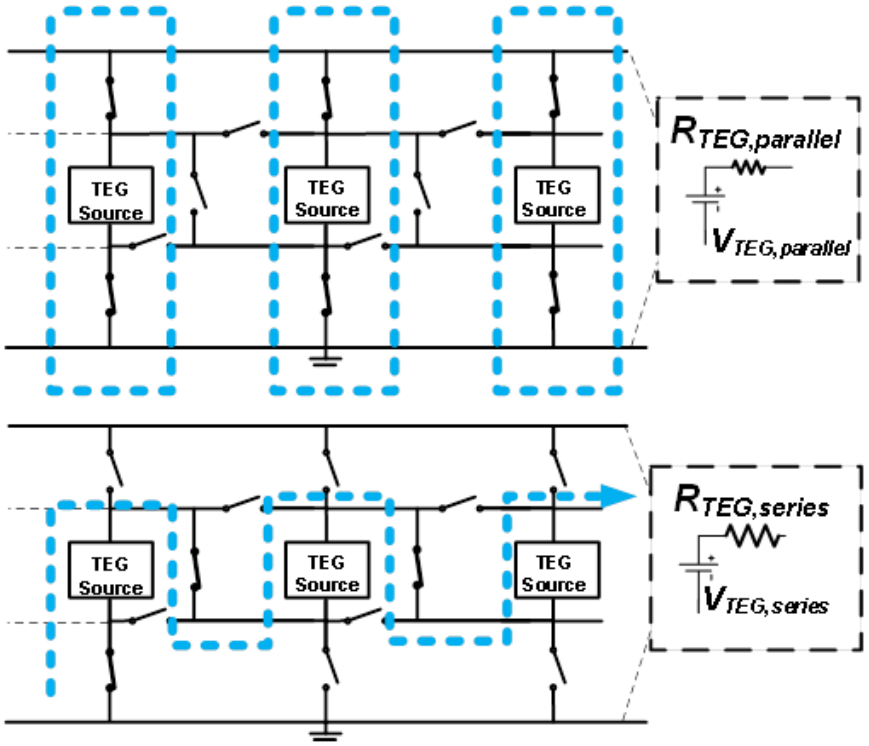

Fig. 61. Multi-array TEG grid parallel (top), series (bottom) configuration.

publication [86] has also shown how sub-micron technologies allow for lower startup voltages and improved efficiency; however, it does not deal with on-chip built-in impedance matching schemes.

If multiple TEG units are placed in an array fashion, a higher power density becomes available to the load system. The control scheme required to handle the dynamic connection for the TEG array, implemented through a state machine, would be capable of changing the manner in which individual TEG units are connected within the array. This reconfiguration would be based on the available temperature gradients. The state-machine implementation is not within the scope of the present work. Fig. 61

illustrates two possible ways in which the TEG units would be interconnecting their terminals to maximize temperature gradients power. For example, for low temperature gradients, the TEG units would be placed in series as shown in the bottom configuration of Fig. 61. Resulting in an equivalent V_{TEG} with an internal resistance $R_{TEG} = R \cdot n$, where R is the internal resistance of one TEG unit, and n is the number of units. To maximize efficiency, the input impedance of the PMU used for thermal EH of such a multi-array TEG must change dynamically along with the array. This internal resistance R_{TEG} will vary dynamically depending on the temperature gradient. If the internal resistance is not matched by the PMU, maximum power transfer will not occur. Wide varying impedance variations, due to TEG grid reconfiguration, are a key issue not addressed by previous EH solutions in literature.

The PMU presented in this dissertation is a step-up switching converter system, capable of tracking these impedance matching changes and delivering maximum power at all times. The maximum power point tracking (MPPT) system is proposed and applied to a BC operating in a discontinuous conduction mode (DCM) with pulse frequency modulation (PFM). Furthermore, a pseudo-zero current switching (P-ZCS) scheme is also implemented to achieve a high efficiency. Fig. 62 illustrates the topology of a BC implementing independent controls for the NMOS and PMOS switch controls (V_{CN} and V_{CP}) through their respective duty cycles (D_{NMOS} and D_{PMOS}). Based on this topology, a MPPT scheme is proposed having independent control over the two MOS switches.

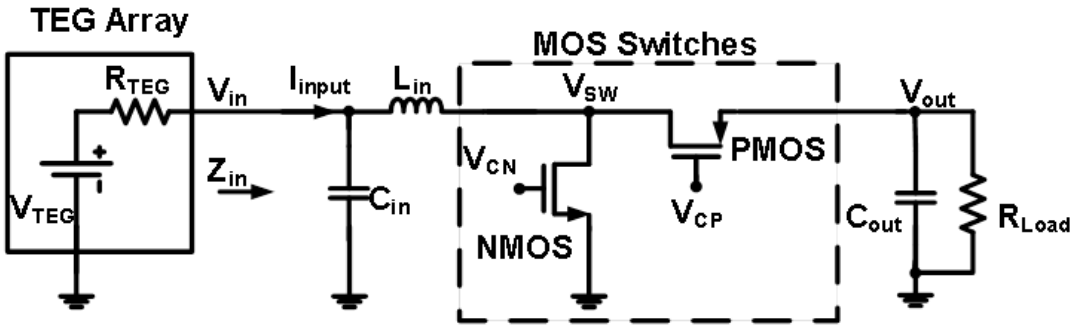

Fig. 62. Schematic of BC with synchronous rectification.

Maximum power point tracking

The critical factor for achieving maximum power transfer from a TEG EH source is to match the TEG array impedance ($\boldsymbol{R_{TEG}}$) with the input impedance ($\boldsymbol{Z_{in}}$) of BC. Once both impedances are matched the voltage at the input of the BC becomes the TEG source ($\boldsymbol{V_{TEG}}$) divided by two. To achieve maximum power point (MPP) state, it is critical to determine the internal impedance range of the TEG array to know the input impedance range. For commercially available TEG sources [91-94], it is known that the internal impedances can range from Ωs to kΩs. From [94], the fixed output electrical impedance for a single 10 mm^2 unit is approximately 300 Ω. Depending on the connection type for the individual TEG units (parallel, series, or a combination), $\boldsymbol{R_{TEG}}$ would not be fixed and would require tuning the input impedance of the switching converter to fully reach MPP operation.

In [20], $\boldsymbol{Z_{in}}$ is approximated as a function of the inductor current charge and discharge, yielding:

$$Z_{in} = \frac{V_{in}}{I_{input}} = \frac{2 \cdot L_{in}}{t_{NMOS}^2 \cdot f_s}\left(1 + \frac{t_{PMOS}}{t_{NMOS}}\right)^{-1} \quad (73)$$

where V_{in} is the input voltage of the BC, I_{input} is the input current going through the inductor, L_{in} is the storage inductor for the BC, f_s is the switching frequency, t_{NMOS} and t_{PMOS} are the NMOS and PMOS on times, respectively. Both t_{NMOS} and t_{PMOS} are related to the duty cycle by $t_{NMOS,PMOS} = D_{NMOS,PMOS} \cdot T_s$, where $D_{NMOS,PMOS}$ is the duty cycle for the NMOS and PMOS switches, respectively, and T_s is the period.

This research's design was structured to directly work with a small grid application to prove the capabilities of matching variable impedances. The proof of concept prototype involves the system design for a 3x3 TEG grid composed of units with variable connections in parallel and series.

One of many possible applications for the system lies in wearable medical applications where a minimum temperature difference is obtained from the skin-environment interface. With temperature differences ranging from 0.4° C to 2° C, the TEG grid would be reconfigured to deliver the highest amount of power directly into the BC. TABLE 7 shows the design specifications for the converter presented in this dissertation. From the reconfigurable TEG grid design, the design presents two different impedance extreme scenarios: a 2.7 kΩ R_{TEG} from the TEG grid where the units are all connected in series and a 33.33 Ω R_{TEG} where the units are all connected in parallel.

TABLE 7. Design specification for converter.

SPECIFICATION	VALUE
$\boldsymbol{V_{in}}$	20 mV→150 mV
$\boldsymbol{V_{out}}$	1.8 V→2.5 V
Maximum efficiency	>60%
Impedance Matching Range	33.33Ω→2.7kΩ
Quiescent Power Consumption	<1 μW

Proposed dynamic matching for boost converter

For the present design the DCM mode of operation was selected for the system design in order to keep power consumption to a minimum due to the low power density of EH sources. PFM modulation was also implemented in order to reduce losses at light loads and improve efficiency [55].

A relationship between (73) and [55] can be made and (73) is rewritten as follows:

$$Z_{in} \approx \frac{R_e \cdot (M-1)}{M} \tag{74}$$

where R_e is defined as the effective impedance seen through the input port of the BC (V_{in}) in Fig. 62, and M is the conversion gain of the BC.

$$R_e = \frac{2 \cdot L_{in} \cdot f_s}{D_{NMOS}^2} \tag{75}$$

$$M \approx 1 + \frac{t_{NMOS}}{t_{PMOS}} = 1 + \frac{D_{NMOS}}{D_{PMOS}} \tag{76}$$

Assuming that $t_{NMOS} \gg t_{PMOS}$, (74) effectively becomes equal to (75). For the PFM scheme used in the proposed system, a constant duty cycle of 50% is established for the NMOS switch. This decision to keep D_{NMOS} fixed was due to the quadratic nature of the relationship between input impedance and the NMOS duty cycle (75). The value of (75) would change at a much faster rate than when varying the switching frequency. The issues that arise by this possible implementation are the available resolution with which the duty cycle of the NMOS would be controlled. Implementing a traditional PWM scheme would hinder the overall system efficiency, and implementing a digital PWM would require additional system blocks which could also limit the efficiency of the converter. Hence, this leaves the values for (75) dependent on f_s and L_{in} of the converter. Fig. 63shows the effect of varying f_s along with L_{in} for Z_{in}.

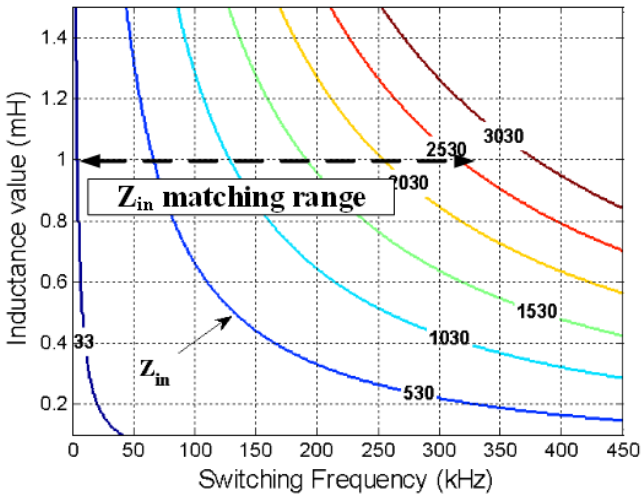

Fig. 63. Contour plots of input resistance variation with L_{in} and f_s.

Selecting an inductor value that is too small may cause a much more stringent requirement on the system's f_s to effectively cover the entire Z_{in} variation. Likewise, setting an inductor value that is too large becomes impractical due to the amount of inductor resistance (DCR) included as well as size. For the presented design, a fixed on-time PFM with 50% duty cycle was implemented using a 1mH inductor with a low DCR of 370 mΩ and small footprint (5.6 mm x 7.1 mm).

From Fig. 63, selecting L_{in} to 1 mH bounds the control range for f_s for nearly a decade that is between 4.2 kHz and 337.5 kHz. This frequency range allows for the implementation of a low power VCO. Depending on the technology, the target application and range of impedances to match, smaller values for the inductor can be selected to optimize the design.

Fig. 64 presents the overall block diagram of the proposed MPPT system. The matching is achieved through the MPPT control via a PFM modulator. By varying f_s of the BC through a voltage control oscillator (VCO), Z_{in} is varied by f_s to adjust the input voltage of the BC and achieve MPPT.

Block diagram for dynamic MPPT

Analogous to a Phase Locked Loop (PLL) which possesses a capture range, the MPPT scheme possesses a matching range for which it can achieve maximum power point with a harvesting transducer. The system implemented in Fig. 64 allows the design to lock and match for abrupt impedance changes because of the ample bandwidth.

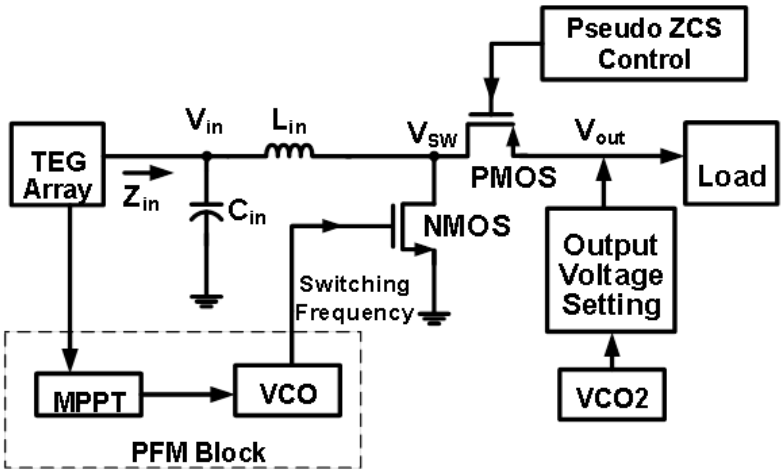

Fig. 64. Block diagram of proposed MPPT system.

This is performed in a similar fashion in which a PLL locks on to different channels in a short period. Note that the system present in [90], assuming a single capacitor filter (with limited bandwidth), would not be able to "lock" to the sudden and large impedance variations under a rapid conditions that would appear due to the TEG rearrangement process due to its limited stability parameters for the matching loop.

For the linear model of the MPPT system, the open circuit voltage (V_{oc}), that arises from the open circuit voltage of the TEG grid, will be used as the input variable. The block diagram in Fig. 65 shows the components of the MPPT system implemented and Fig. 66 shows the small signal linearized equivalency used to track its dynamic behavior.

The source V_{oc} is divided by 2 and compared to the input voltage (V_{in}) seen by the BC. From the linearized model of the MPPT implementation in Fig. 66, the open loop transfer function becomes:

$$TF_{OL} = K_P \cdot K_{CP} \cdot F(s) \cdot H_{c-in}(s) \tag{77}$$

where K_p is the comparator gain, K_{CP} is the gain due to the charge pump, $F(s)$ is the transfer function for the filter, and $H_{c-in}(s)$ is the BC control-to-input voltage transfer function.

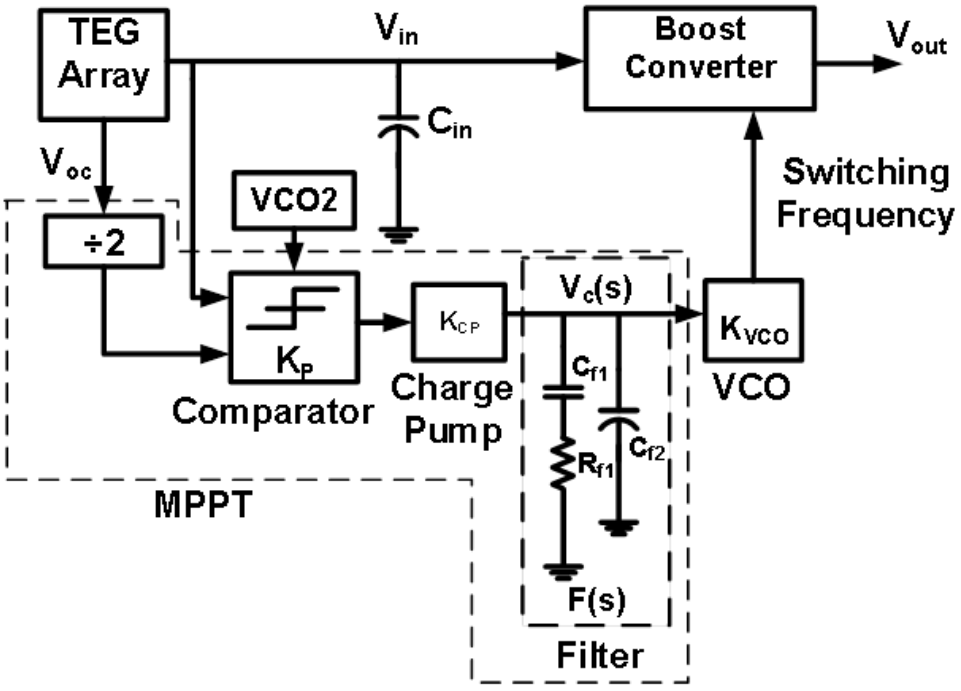

Fig. 65. Block diagram for MPPT implementation.

To minimize power consumption, the charge pump quiescent power is reduced by limiting the bias current; this leaves the filter as the one factor in the design with allowance for performance improvement.

The filter allows for an improved phase margin as well as extended bandwidth for the system. Depending on the implementation, this can permit faster locking time and minimize ringing due to sudden impedance changes. It is the implementation of the filter within the MPPT control loop which allows for the broad impedance matching.

To obtain the effect that the input voltage has in relation to the control signal V_C, the system behavior is approximated by linearizing the BC around an operating point.

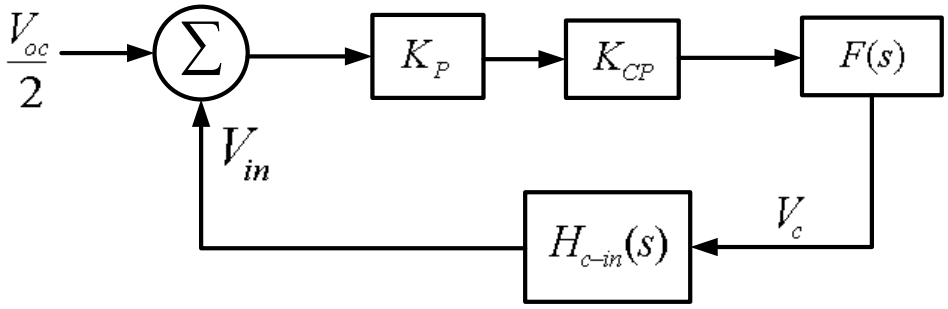

Fig. 66. Small-signal linear model of MPPT block.

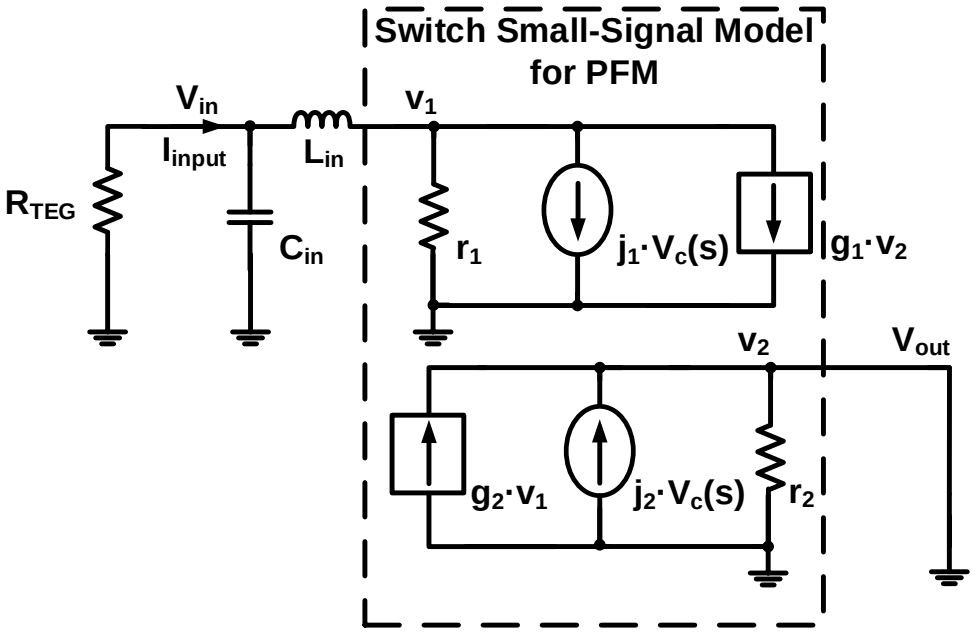

Fig. 67. Control-to-input voltage transfer function model of boost converter.

Assuming the output voltage reaches a steady state DC voltage via the regulating mechanisms (P-ZCS and comparator); both the output and input voltage sources are assumed to behave as AC grounds in small signal as shown in Fig. 7. In [55], a small signal model for the BC operating under a PFM scheme was presented. Fig. 67 represents the aforementioned small signal model, where the parameters j_x, r_x, and g_x are obtained via three dimensional Taylor series expansions of the average input and output voltages and duty cycle [95]. The variable $V_c(s)$, seen in Fig. 67, is the VCO control voltage coming in from the filter block (Fig. 65).

Thus the control-to-input voltage transfer function $H_{c-in}(s)$ can be obtained. Following the small signal model from [55], the PFM control-to-input voltage transfer

function is acquired, which includes the effects of f_s as well as the gain of the VCO block.

$$H_{c-in}(s) = \frac{V_{in}(s)}{V_c(s)} = \frac{\frac{j_1 r_1}{L_{in} C_{in}}}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{78}$$

where

$$\omega_o = \sqrt{\frac{R_{TEG} + r_1}{L_{in} C_{in} R_{TEG}}}$$

$$\xi = \frac{(L_{in} + C_{in} R_{TEG} r_1)}{2\sqrt{(C_{in} L_{in} R_{TEG})(R_{TEG} + r_1)}}$$

As can be seen from (78), the analytical transfer function for the control-to-input voltage in PFM would closely resemble its Pulse Width Modulation (PWM) counterpart [95]. The disparity lies in the magnitude of the transfer function due to the addition of the VCO gain (K_{vco}) and f_s terms in the j_1 small signal parameter.

For the presented design, a VCO with K_{VCO} of $550\ kHz/V$ was used; this VCO gain selection is justified in Section IV. Fig. 68 shows the Bode plot comparison between (78) and the simulated one when f_s is set at 100 kHz. Agreement between both analytical and simulated results is shown with 9% error in magnitude at DC; the gain mismatch for the magnitude is from the VCO gain and nonlinearity of the block.

As in PLLs, different compensation schemes can be implemented to extend bandwidth and minimize ringing. Using the initial assumption that the filter $F(s)$ is comprised only of a single storage capacitor given by C_f [90], taking (78) and expanding from (77) yields the open loop transfer function:

$$TF_{OL} = \frac{K_p \cdot K_{CP}}{sC_f} \cdot H_{c-in}(s)_{PFM} \tag{79}$$

This open loop transfer function allows for an insight on the parameters affecting fast changing series impedances and the requirements to achieve MPPT. Assuming a value of $V_{in,DC}$ of 100 mV, 1 µF for C_f, a $K_P \approx 90$dB, and K_{CP} can be approximated as the static current consumed by the charge pump [96] or 0.5 µA in Fig. 65.

The frequency response for the entire open loop system for the mid-range value of $R_{TEG} = 1.366\ k\Omega$; results in a phase margin (PM) of 16° and unity gain frequency of 82.4 Hz. This presents a conditionally stable system but with an ample amount of ringing and a limited bandwidth that will react slowly to drastic impedance changes from the TEG grid.

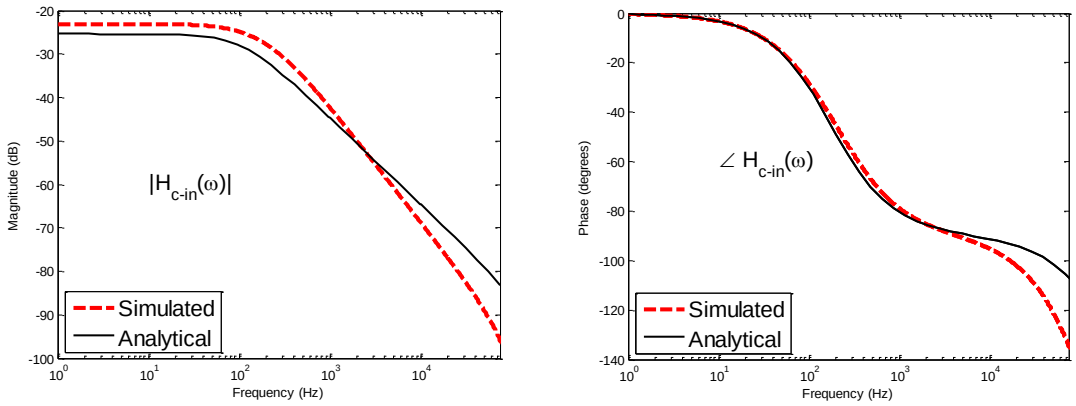

Fig. 68. Analytical (5) vs. simulated results: (left) magnitude, (right) phase.

This limited range approach would not be able to cope with the sharp impedance variations which would take place with the TEG array reconfiguration. Implementing a different filter configuration would allow for a much faster, and overall stable response from the system (increased bandwidth), while maintaining good PM.

A type II filter [54], illustrated as $F(s)$ in Fig. 65, was implemented to obtain a unity gain frequency was driven to 2.24 kHz and a PM of 89.2°. This implemented filter allows for the system to be stable under the abrupt impedance changes presented by the TEG grid. Section IV further elaborates on the implementation.

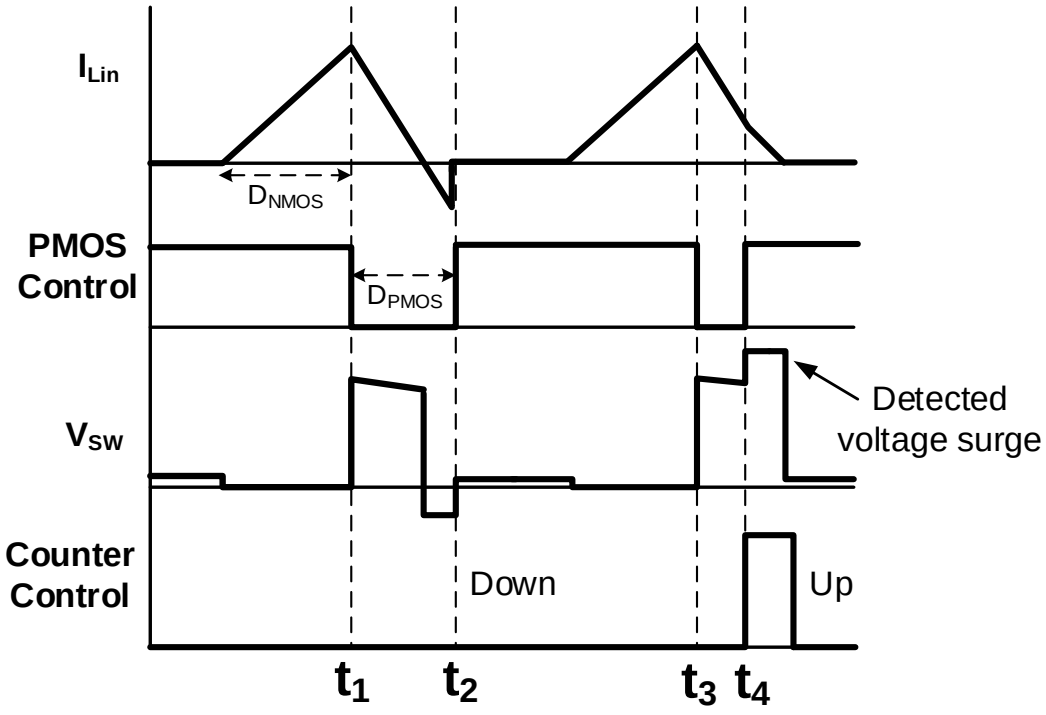

Fig. 69. Inductor current behavior for P-ZCS scheme.

Algorithm for pseudo zero current switching

In order to minimize component stress and increase efficiency, a zero current switching (ZCS) technique is employed. The P-ZCS is implemented to minimize the inductor current losses through the PMOS switch. The P-ZCS is performed via a skewed voltage peak detector in the V_{SW} node (Fig. 62).

Fig. 69 shows the overall current and voltages associated with the P-ZCS algorithm. At time interval t_1-t_2, considering the inductor is completely discharged when the PMOS switch is turned off, no voltage peaking should be discernible at the V_{SW} node since the inductor current reverses direction. As noted by [88], this drains the parasitic capacitors associated with the V_{SW} node before turning on the drain-bulk diode of the NMOS switch.

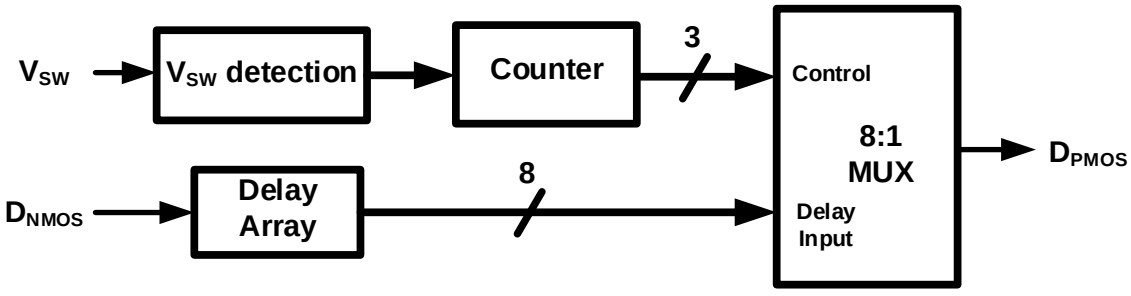

Fig. 70. Pseudo-ZCS control algorithm.

During time interval t_3-t_4, the current in the inductor has not completely been discharged; this causes the parasitic diode across the PMOS switch to turn on and is associated with a voltage surge at V_{SW}.

By sampling the high/low state of V_{SW} shortly after the PMOS is switched off, it can be determined whether the PMOS switch was turned off before or after the current falls to zero. From Fig. 4 the implementation of the P-ZCS in Fig. 70 shows the PMOS ON-OFF selection scheme implementation.

The ON-OFF time for the PMOS is selected via an UP-DOWN Counter that detects the voltage levels at the V_{SW} node and signals a MUX to choose the PMOS ON time from a set of delay signals. In steady-state operation, the system toggles between two different D_{PMOS} values: one where the inductor current falls below zero and one where the inductor current does not reach the zero value.

Output voltage setting

In order to achieve the set output voltage for the system, from (79) the values of D_{PMOS} are set to be much smaller than D_{NMOS}. This sets the system's conversion gain high and achieves the required output voltage.

The output voltage setting block, illustrated in Fig. 64, is employed to set V_{out} to a predefined value. A clocked comparator driven by a dedicated oscillator VCO2 verifies that V_{out} does not exceed a set external voltage reference (V_{REF}). If V_{out} exceeds V_{REF}, the primary VCO within the PFM block is disabled and the BC ends operation.

Once the system reaches an operational steady state, V_{out} can be set as the internal supply source for the system (V_{DD}). It should be noted that VCO2's clock signal, for the comparators in the system, is never disengaged. This allows continuous monitoring of input and output voltages. As VCO2 maintains operation even when V_{out} exceeds V_{REF}, on average V_{out} is never more than a few cycles of VCO2 over V_{REF}. Furthermore, C_{in} and C_{out} are both fairly large valued (10μF); these capacitors maintain both the input and output voltage comparatively constant when compared to both the switching frequencies of VCO and VCO2.

Typically EH power management systems disengage the source after the desired output voltage is reached [17, 86, 89, 97]. However, different configurations can be implemented with the BC in order to minimize the time the system is disabled: i) A more demanding variable load at the output; ii) multiple BC units could potentially be placed in an array fashion in order to continuously harvest energy from the TEG array, and finally iii) multiple storage capacitors could also be considered in order to allow the BC to continuously charge up.

Building block circuit implementation

Divider (extraction of $V_{oc}/2$)

The implemented capacitive divider [89], samples the input voltage and divides it by two by saving the open circuit voltage in storage capacitors C_1 and C_2, as shown in Fig. 71. The dual phase nature of the block samples the open circuit voltage, V_{oc}, and effectively obtains the open circuit voltage of the TEG divided by two (i.e. $V_{oc}/2$) by

channeling the stored charge into two storage capacitors ($C_{1,2}$). Once the desired voltage is stored, it is compared with the input voltage (V_{in}) of the BC (Fig. 65).

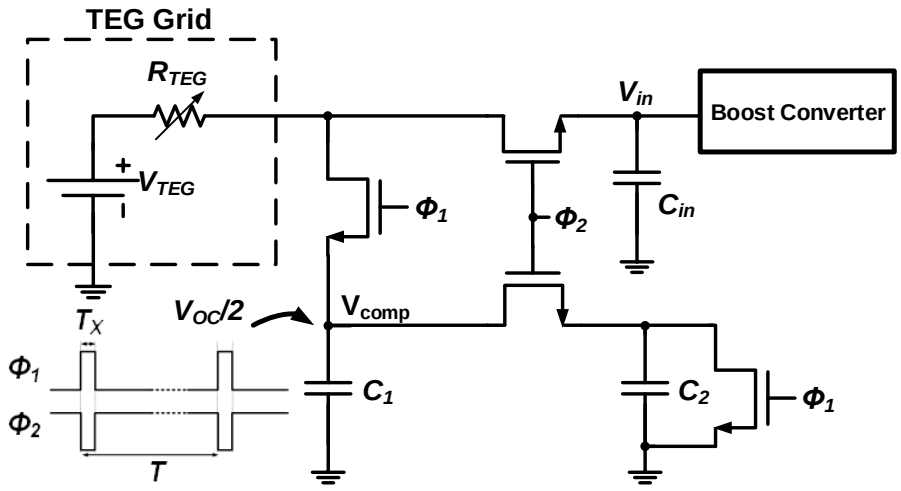

Fig. 71. Divider circuit implemented [89]

Comparators (K_P) and charge pump (K_{CP})

Two clocked comparators [96] were implemented for the system. The first clocked comparator evaluates the difference between the input voltage of the BC (V_{in}) and the targeted value of $V_{oc}/2$. The second comparator is used to set the level of V_{out}. Both comparators operate utilizing a dedicated VCO, designated as VCO2, operating at approximately 200 kHz.

For the K_P gain used in (5), the comparator was assumed to operate quasi-linearly since the rate at which the nodes V_{in} and V_{out} change is much lower than the

switching speed of the comparator [98]. For the charge pump, a conventional current steering design [54] was implemented consuming a static current of 0.5μA.

Voltage controlled oscillator

The VCOs implemented in the PFM block are based on [99]. A low-frequency full-swing ring oscillator topology was employed through the use of controllable resistances (R_G) between each inverting stage of the VCO implemented with transmission gates. This allowed for a controlled delay and full swing oscillations. The switching frequency becomes:

$$f_s = \frac{g_m}{2N_{stages}C_{gate}(1 + g_m R_G)} \tag{80}$$

where the frequency is dependent on the transconductance (g_m) of the transistors in the inverter device, the parasitic capacitances at the input of the next stages (C_{gate}), and the number of inverter stages in the VCO (N_{stages}). The VCO varies its frequency only by varying R_G. Implementing the VCO with a low K_{vco} was done in order to maintain power at a minimum while setting the required f_s to achieve MPPT.

For the secondary oscillator VCO2, an externally controlled ring oscillator was implemented running at approximately 200 kHz.

Filter

Due to the nature of EH systems, low power is a major design factor; a passive filter is the most appropriate. As discussed previously, implementing a filter with only a

capacitor will not achieve stable MPPT with the unavoidable sudden TEG grid impedance variations.

Through a type II filter [54], it is possible to achieve a high gain at low frequencies as well as controlled bandwidth increase and improved phase margin through the zero and high frequency pole given by the series resistance R_{f1} and capacitor C_{f1} (Fig. 65). Bandwidth increase would enhance the speed at which the loop would respond to impedance changes, and increased phase margin would allow for a stable response from the system when facing rapid impedance changes from the TEG grid. This approach would assure stability within the design parameters of the TEG array. The transfer function for the implemented filter in Fig. 65 yields.

$$F(s) = \frac{K_{DC}\left(sR_{f1}C_{f1} + 1\right)}{s\left(s\frac{R_{f1}C_{f1}C_{f2}}{C_{f1} + C_{f2}} + 1\right)} \tag{81}$$

where

$$K_{DC} = \frac{R_{f1}C_{f1}C_{f2}}{C_{f2}\left(C_{f1} + C_{f2}\right)\left(R_{f1}C_{f1}\right)}$$

The obtained unity gain frequency was 2.24 kHz and the phase margin was 89.2°. The values of the used components were: $C_{f1} = 0.1\mu F$, $C_{f2} = 10pF$, and $R_{f1} = 500\Omega$. The filter was implemented with off-chip components for this proof of concept; further implementations can potentially integrate most, if not all, of the filter components.

Pseudo zero current switching

Due to the low power requirements for an EH PMU system, the P-ZCS algorithm is implemented with minimal components. By following a similar topology as [100], but by directly sensing the V_{SW} node, the inductor current is closely inspected to avoid its value from becoming negative. After the detection of the V_{SW} voltage by a skewed inverter (Fig. 62), a flip-flop samples the binary state of the V_{SW} node shortly after the rising edge of the D_{PMOS} signal.

The sampled state then informs a counter to either count up (decrease the delay period) or count down (increase the delay period). Thus, the counter acts as an integrator in a feedback loop; if the sampled state is high, then the counter increments and D_{PMOS} increases for the next switching cycle. If the V_{SW} state is low, then the counter decrements, causing D_{PMOS} to decrease for the next cycle. As a result, in steady state, the current will toggle above and below the target value. This allows implementing a programmable delay that will be controlled by the residual inductor current after turning OFF the PMOS switch.

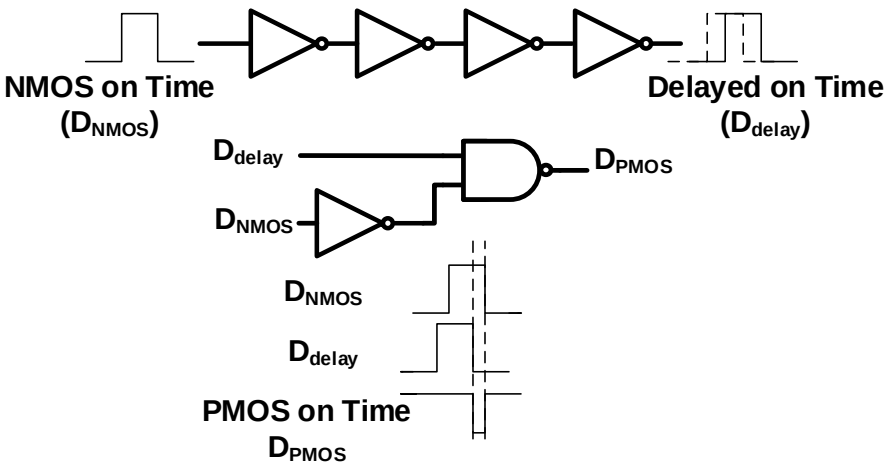

Fig. 72. Implementation of delay array for PMOS on/off time.

The implementation of the P-ZCS scheme was realized by establishing a set of values for D_{PMOS} that assures a sufficiently high conversion ratio (75). By duplicating and delaying the D_{NMOS} signal, and implementing gate logic as shown in Fig. 72, the D_{PMOS} is obtained to quickly turn on/off the PMOS transistor to transfer charge to the output. A total of eight controllable delay cells were implemented. Depending on the inductor current, a different delay would be selected, which would then be applied to the PMOS control signal.

Startup

The system allows for a self-sustaining operation once it achieves steady state. The initial startup voltage requirements are usually not met by EH sources. The boost converter presented in this dissertation requires an external precharge of the load

capacitor to begin operation. A precharge voltage of 900 mV at the output capacitor is required for the boost converter to begin operation.

Experimental results

The proposed system was fabricated in 0.5 µm CMOS process. Fig. 73 shows the die microphotograph of the design. The active area occupied by the chip was approximately 0.735 mm^2. The values for C_{in} and C_{out} (see Fig. 62) were both 10 µF, and the inductor used was a 1 mH inductor with a DCR of 370 mΩ and a footprint of 5.6 mm x 7.1 mm.

The design was tested simulating the 3x3 Micropelt TEG via a power supply with an impedance array. The impedance array connected all of its elements in series or parallel through discrete MOS switches controlled by an external clock.

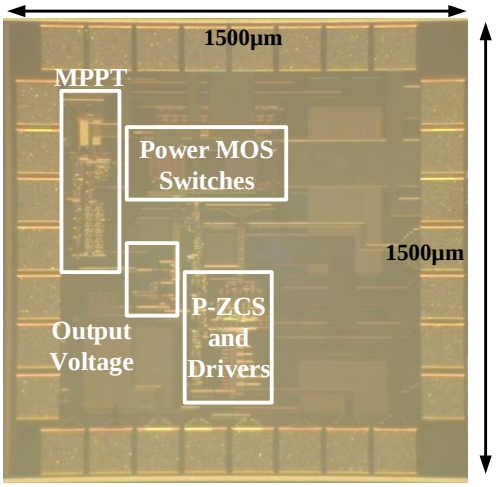

Fig. 73. Die microphotograph

MPPT impedance tracking

In Fig. 74, the V_{in} node is operating with a TEG voltage of 200 mV and applied variations in the TEG. The node shows locking at 100 mV, which is the maximum power point, R_{TEG} is initially set at 2.7 kΩ. An abrupt change in R_{TEG} to 33.33 Ω is applied. The MPPT system follows the change in TEG impedance and maintains the $V_{oc}/2$ condition at the input. A voltage dip of 60 mV is present when going from 33.33 Ω to 2.7k Ω due to the time response the system takes to increase f_s to match the new impedance.

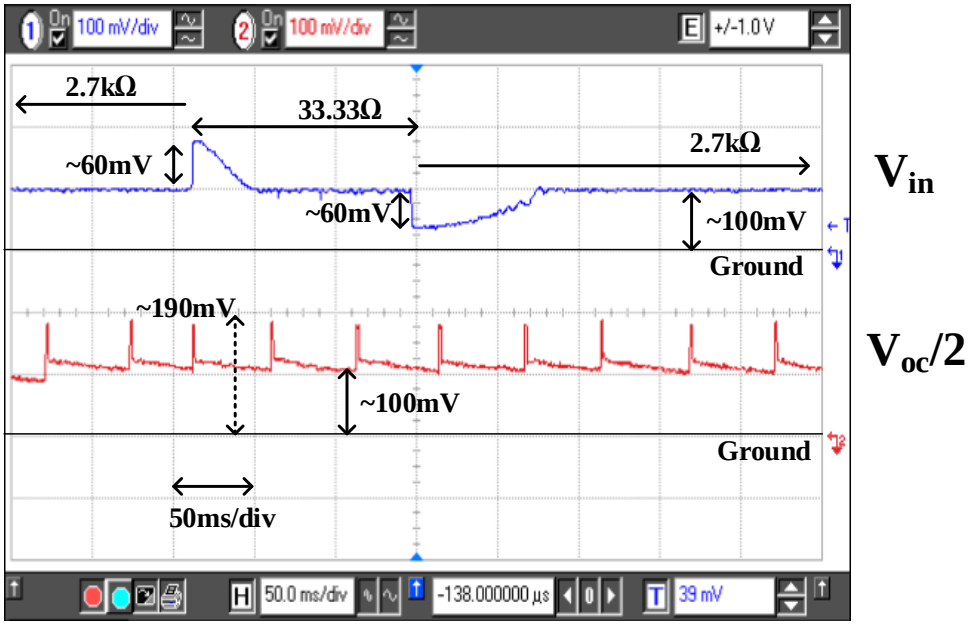

Fig. 74. Input voltage regulation maintaining MPPT under large variations of R_{TEG} (V_{OC}=200 mV).

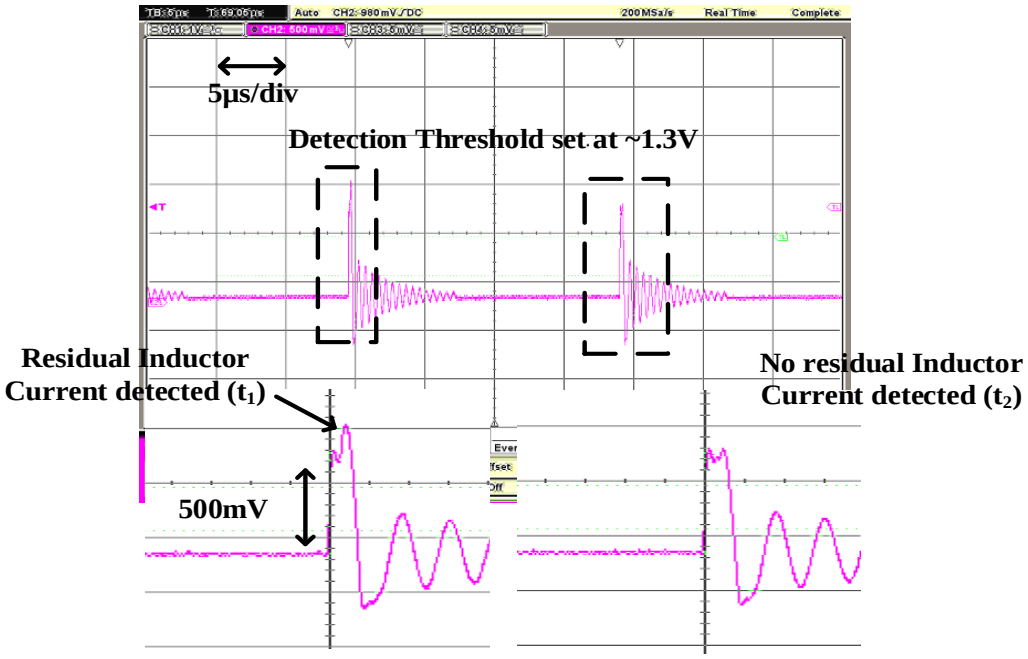

Fig. 75. P-ZCS scheme implementing variable D_{PMOS} duty cycles to minimize inductor losses.

For the negative step of 2.7kΩ to 33.33Ω, a voltage surge of 60 mV takes place due to the time the system requires to stabilize back to the maximum power point.

P-ZCS waveforms

As mentioned in Section IV, the P-ZCS varies the D_{PMOS} signal to minimize the amount of losses due to inductor current flowing negative. Fig. 75 shows the waveforms of node V_{SW} for the two varying D_{PMOS} lengths that are toggled once the system reaches a steady state. These two states for D_{PMOS} are the ones with which the system achieves the minimum amount of losses for the inductor current. For t_1 the D_{PMOS} on time is too short; hence, a voltage surge at V_{SW} is detected. For t_2 the voltage spike is not present and causes D_{PMOS} to revert back to the duration of t_1. The waveforms in Fig. 14 were

obtained for $V_{in} = 150\,mV$ and $R_{TEG} = 300\,\Omega$ and show expected behavior for V_{SW} node.

Efficiency measurements

Fig. 76 shows the measured efficiencies for the system. Measurements were performed using V_{out} as the internal supply for the system. Output node V_{out} is set to 2.5 V for R_{TEG} values of 33.33Ω to 300Ω, while it is set to 1.8 V for R_{TEG} values of 600 Ω to 2.7 kΩ. Each R_{TEG} efficiency value was measured with a constant resistor load at the output.

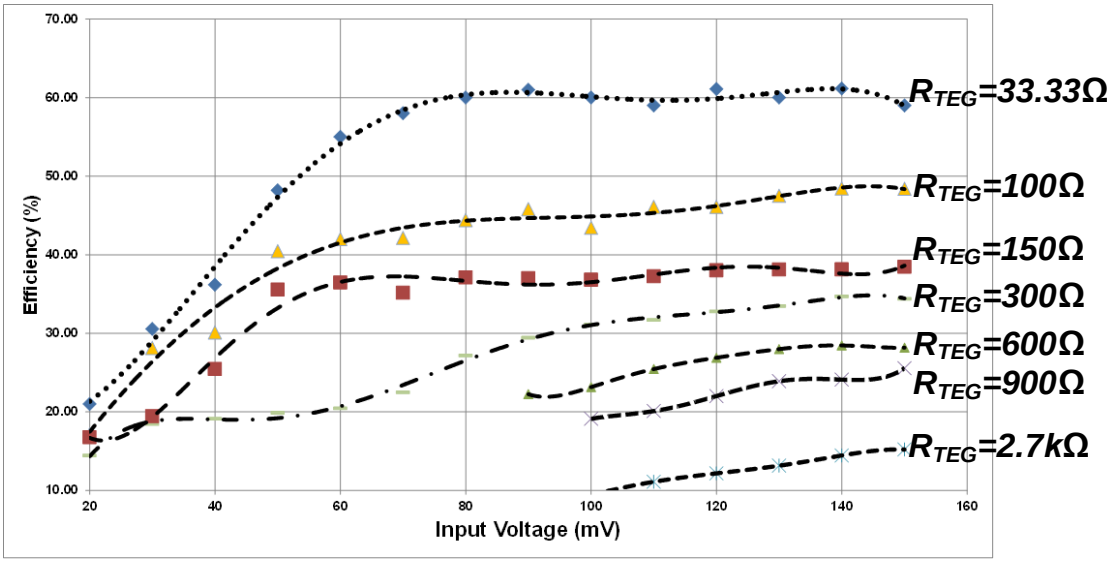

Fig. 76. Measured efficiency for system under varying R_{TEG} values for R_{TEG} =[33.33Ω to 300Ω] I_{load}≈14μA,for R_{TEG} =[600Ω to 2.7kΩ] I_{load} =1μA.

Maximum efficiency measured was 61.15% at 140 mV input voltage and R_{TEG} of 33.33Ω; delivering an output power of $\sim 359\ \mu W$. It should be noted that improved efficiency could be achieved by reducing the value of R_{TEG} from the TEG. TABLE 8 summarizes the performance of this work and compares it with previously reported state-of-the-art works. Notice that the work presented possesses a much broader matching range than any of the previous reported solutions while having a large output range.

Conclusions

This chapter presents a solution for the impedance matching between a low power boost converter and a wide varying impedance range from a TEG array using a practical and novel MPPT technique. Design methodology and trade-offs are provided to solve general arbitrary EH sources where a varying resistance range is to be matched to a boost converter.

TABLE 8. Performance summary

SPECIFICATION	[86] †	[17]	[89]	[20]‡	[90]	[97]†	[101]†	THIS WORK
Input Voltage Range	30mV-200mV	20mV-250mV	40mV-300mV	20mV-160mV	70mV-600mV	120mV	12mv (380mV for self-startup)	20mV-150mV
Output Voltage	1.2V	1V	2V	1.88V	3V-5.8V	1.2V	0.66V-3.3V	1.8V-2.5V
Quiescent Power Consumption	-	1.1μW	-	-	-	-	-	<1μW
MPPT	No	No	Yes	Yes	Yes	No	No	Yes
Impedance Matching Range	-	-	5Ω	4.1Ω-13Ω	8Ω (with 10% variation tolerance)	-	-	33.33Ω-2.7kΩ
Max. Efficiency	73%	75%	[1]61%	[2]64%	[3]72.2%	30%	[5]82%	[4]61.15%
Technology	65nm	0.13μm	0.13μm	0.35μm	0.35μm	0.18μm	0.13μm	0.5μm

‡ Values given only for thermoelectric input
† Design requires no external voltages to startup system
1.$R_{TEG} = 5\Omega$
2.$R_{TEG} = 10\Omega$
3.$R_{TEG} = 8\Omega$
4.$R_{TEG} = 33.33\Omega$
5.Output Power of 12mW (Input power ≈14.6mW)

CHAPTER IV

POWER MANAGEMENT SYSTEM WITH INTEGRATED MAXIMUM POWER EXTRACTION ALGORITHM FOR MICROBIAL FUEL CELLS*

Introduction

Microbial fuel cells (MFCs) are an emerging bioelectrochemical technology that converts chemical energy into electrical energy by producing electricity directly from biodegradable substrates such as wastewater. In MFCs, exoelectrogenic bacteria break down the carbon substrates such as glucose and acetate while producing electrons, which are then transferred to the anode. These electrons flow to the cathode through an external load, and then combine with protons and oxygen to form water, thus completing a full circuit and producing electricity [39].

However due to the low power production of the current MFC technology [6, 102-110], significant improvement in overall system performance is needed for MFC technology to become a viable renewable energy technology. Developments in the MFC field have mainly focused on development of new electrode materials, improvement of the design, and development of efficient membranes, all to improve the power production from MFCs. However, there has been limited focus in methods to extract maximum power from the MFCs in an efficient way as well as to up-convert the low voltages and power to a usable level [111].

* Reprinted with permission from "Power Management System With Integrated Maximum Power Extraction Algorithm for Microbial Fuel Cells" by S. Carreon-Bautista, C. Erbay, A. Han, and E. Sanchez-Sinencio, 2014. IEEE Trans. On Energy Conversion, vol. 30, no. 1, pp. 262-272, March 2015 © 2015 IEEE

Current power management systems (PMSs) for MFCs typically utilize discrete component implementations of DC-DC converters emphasizing efficiency[106], with some method implemented for maximum power point tracking [105]. The main drawback of these implementations are the quiescent power consumption of the DC-DC converter's controller itself and lack of integrated impedance matching schemes dedicated for MFCs to run at maximum power point. Improved methods of harvesting power from MFCs are needed to address both of these issues for MFCs to be used in practice.

Specific dedicated PMS solutions [112] for other harvesting sources would not offer a solution to the MFC characteristics due to the reactive behavior within the MFC. The previous implemented maximum power point (MPP) acquisition technique would not allow the system enough time to reach MPP, thus extracting significantly less power. Due to the lower power extraction, a larger error on the Pseudo-Zero Current Switching scheme will occur due to the toggling nature of the digital control. The aforementioned PMS [8], if applied to the MFC power conditions, would suffer from at least a 15% overall efficiency decrease from faulty MPP and severe inductor current losses. Hence, this solution would not meet the MFC requirements for maximum power extraction.

The project presented in this dissertation is a suitable PMS solution to handle the MFC power profile optimally. This proposed PMS has two unique characteristics: i) an accurate maximum power extraction algorithm (MPEA) capable of dealing efficiently with the MFC time constant, and ii) A Zero Current Switching Tracking (ZCST) loop, to maximize efficiency power conversion by reducing losses from the inductor current.

This proposed PMS offers a tailored solution for the MFC power profile. The MPEA scheme was integrated into the PMS to harvest maximum power from the MFC under all conditions. MPEA is a key block in the operation of the PMS as the power from the MFC is very low. The MPEA also continuously monitor and adapts to power variations from the MFC. Note that the ZCST loop is performed in order to minimize losses from inductor current by modulating the PMOS on/off time (T_p). This reduces negative inductor current and improves efficiency. Thus, the overall system efficiency of the PMS and charging time to operate electronic applications can be improved with the proposed MPEA and ZCST scheme presented here.

MFC and power management system specifications

The design presented is composed of an MFC controlled through the developed PMS to deliver sufficient power to a resistive load as a demonstration of the PMS. This section describes the design and characterization of the MFC, as well as the system specifications of the PMS.

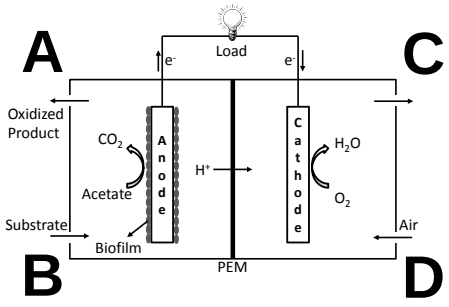

Fig. 77. Schematic of conventional two-chamber MFC.

MFC construction and characterization

A two-chamber MFC was constructed from plastic (acrylic) anode and cathode chambers (total volume: 240mL). The anode was made from a3 cm x 4 cm carbon felt (Morgan, UK) and the cathode was made from a 3cm x 4cm carbon cloth containing 0.5 mg/cm^2 of Pt catalyst on one side (ElectroChem, Inc). Proton exchange membrane (PEM) (Nafion 117^{TM}, Ion Power Inc.) was used to separate the anode and cathode compartments from each other, while selectively allowing proton generated in the anode chamber to cross over to the cathode chamber. Both anode and cathode were connected to titanium wire and a 1kΩ load resistor was placed between the electrodes.

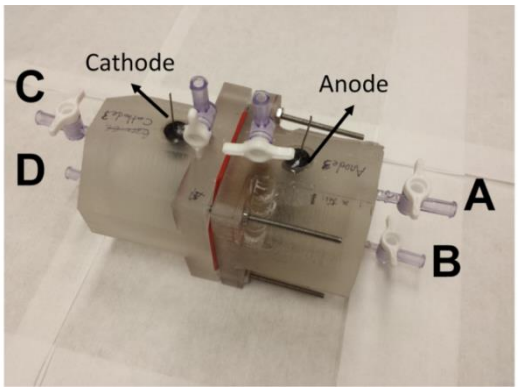

Fig. 78. The 240 mL two-chamber MFC constructed and used for the PMS characterization, connections follow Fig. 77.

Fig. 77 shows the overall schematic diagram of the MFC. The MFC was inoculated with anaerobic activated sludge collected from the Austin Wastewater Treatment Plant. The anode chamber was refilled with fresh wastewater daily for the

first 3 days of startup. As anode growth medium, acetate (1.0g/L) in nutrient/mineral/buffer (NMB) solution was used (10mL/L mineral base 1, 10mL/L mineral base 2 and 1mL/L nutrient base) [113]. The anode chamber was refilled each time with the NMB solution with acetate when the voltage across the load resistor dropped below50mV (batch mode feeding). The constructed two-chamber MFC is shown in Fig. 78 (overall dimension: 5 cm x 5 cm x 12 cm, W x H x L).

The MFC voltage was recorded by using a digital multimeter through a multiplexer (National Instruments) and monitored via LabView^{TM} (National Instruments) [114-116]. Once the voltage was stabilized, maximum power and voltage curves were obtained by varying the load resistor value between the electrodes (Fig. 79).

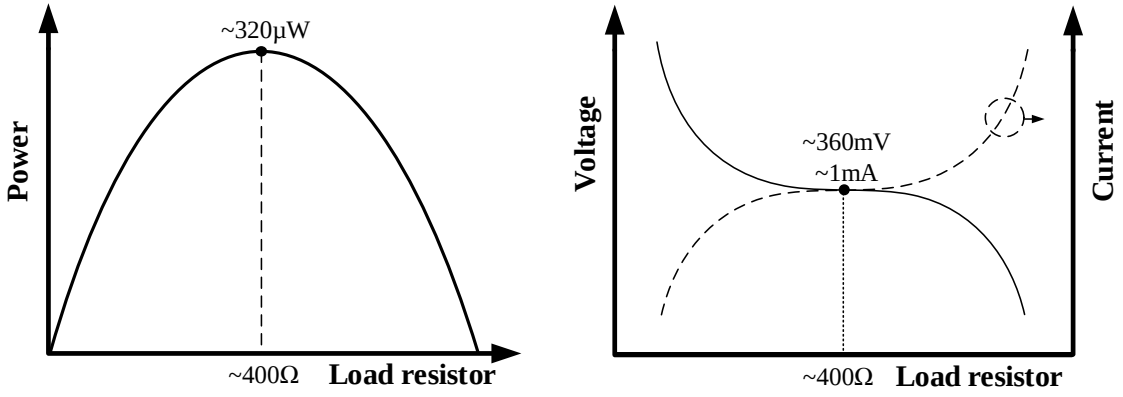

Fig. 79. Power-resistance and voltage-resistance characteristics of the MFC.

MFC electrical equivalent modeling

The MFC is modeled, in a first-order approximation, as a voltage source with a high series resistance, which limits the amount of available current to be delivered. Fig. 80 shows both the steady state and dynamic simplified electrical equivalent models of an MFC. V_{dc} represents steady-state (DC) voltage delivered by the MFC and V_s represents the dynamic voltage that takes into account the time constant (τ_{MFC}) due to the parasitic capacitance C_{MFC} inherent in an MFC.

The value of R_{MFC} is considered to be the internal resistance made up of several different components (anodic resistance, cathodic resistance, membrane resistance, and electrolyte resistance) [117]. The value V_{MFC} is the MFC's thermodynamic voltage which varies nonlinearly depending on multiple variables, such as solution pH, temperature, and substrate concentration in the anode chamber [118].

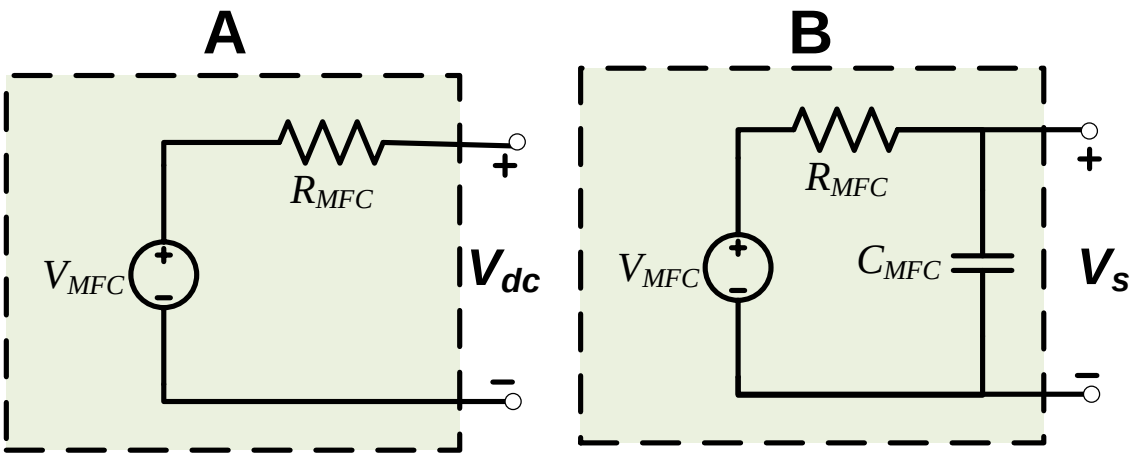

Fig. 80. A) Stead-state electrical mode (V_{dc}) and B) dynamic model (V_s) of the MFC.

Several different electrical models of an MFC have been presented throughout literature [6, 104-107], and most use a simple voltage-resistor model (Fig. 4A). Based on the maximum power transfer theorem, in order to obtain the maximum power from the MFC, the impedance seen at V_{dc} (V_s), for a DC source would have to be equal toR_{MFC}. This steady state equivalent (V_{dc}) circuit (Fig. 80A) however does not take into account the effective parasitic capacitor, since at DC this would not appear. Fig. 80B presents a more realistic model that includes the parasitic capacitance, similar to that presented by [106], and was the base with which the MPEA was designed. Note that from Fig. 79, the value of $R_{MFC} = 400\ \Omega$ is obtained.

The design of the MPEA implemented for the PMS takes into account C_{MFC} and its effect under dynamic conditions (V_s). The time constant (τ_{MFC}) was obtained by shorting the output then opening the MFC connection and measuring the time the output voltage requires to reach nominal V_{MFC}.This method allowed for estimation of C_{MFC} from the characterized device. The PMS requires only range of τ_{MFC} and associated R_{MFC}in order to operate due to the adaptive MPEA scheme. The use of the time constant variable employed in the MPEA system will be further discussed in the following section III-C.

System specifications

MFCs typically generate voltages below 1 V, at which even low-power devices and systems cannot be directly powered.

The PMS implemented for the MFC was designed to deliver a higher and regulated voltage supply to be able to directly power low-power applications. Two key features required for a PMS for low-power energy harvesting systems are low power consumption by the PMS itself and maximum efficiency. Since efficiency is a critical factor in the design, a boost converter was selected due to its inherent higher efficiency at lower power profiles [119]. The specifications for the design are presented in TABLE 9. Due to the low-power nature of the application, an efficient boost converter was set to discontinuous conduction mode (DCM) to minimize losses and reduce power consumption by the controller.

TABLE 9. MFC PMS system specifications.

SPECIFICATION	VALUE
$\boldsymbol{V_{in}}$	360mV (MPP)
$\boldsymbol{V_{out}}$	2.5V
Max efficiency	>55%
Impedance to match	R_{MFC} = 400Ω

Adaptable maximum power extraction algorithm

Current state-of-the-art

The usual manner in which MPP is obtained in reported MFC power management units is through prior testing to find the maximum operating point by using multiple load resistor values [102, 103, 106, 107]. This is usually a very time consuming

approach, since each operating point is obtained by varying different load resistances connected directly to the MFC. A valuable tool for the MFC field would lie in the automatic detection of the MPP, reducing overall testing time to detect the MPP.

The approach to reach MPP automatically has only been explored in [6] implementing a hysteretic controller to reach MPP. However the main drawback in aforementioned approach is the requirement for multiple external and discrete components to locate the optimal operating point, resulting in a high power consuming solution and poor efficiency. This type of solution is not practical, nor accurate, for low power energy harvesting systems such as MFCs since the power required to drive the PMS is comparable or even higher than the actual power that can be extracted. Another solution obtains automatic maximum power extraction for thermoelectric generator arrays [8], but this solution does not take into account the MFC complex impedance source behavior. This complex MFC impedance would result in faulty MPP due to the τ_{MFC} associated with the fuel cell. This would effectively reduce overall power extraction and system efficiency.

The approach presented in this chapter allows for dynamic tracking of the MPP while consuming low power through a custom monolithic integrated circuit.

Overview of the proposed MPEA system

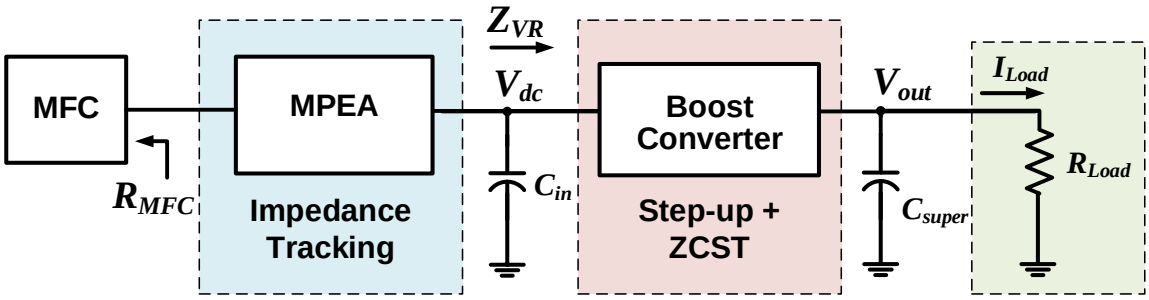

Fig. 81. Conceptual representation of the proposed power management system.

For the adaptable MPEA scheme proposed here, two complementing operations should take place: 1) locating the required operating point to achieve MPP and 2) setting the input impedance for the boost converter to match that of R_{MFC}. Fig. 81 highlights the top level structure of the PMS, with both resistance matching through the MPEA and voltage regulation through the boost converter and ZCST. It should be noted that the PMS in [8] cannot implement the above two operations for an MFC.

A quick mechanism is employed that samples the open circuit voltage of the MFC (V_{MFC}) and divides this value by two to locate the required operating point to achieve MPP. This operating point becomes the reference voltage, which would appear at the input node, (V_{dc}), if the input impedance of the boost converter is equal to R_{MFC}.Since the MFC behaves as a DC voltage source, where variations occurring on the DC voltage of the MFC can be considered negligible i.e. low frequency, the maximum power transfer theorem states [120] that maximum power is transferred when

a DC source (V_{MFC}) with fixed source resistance (R_{MFC}) is connected to a load resistance (Z_{VR}) of equal value to the source resistance. This is justified next.

$$P_{load} = I_{load}^2 Z_{VR} = \left(\frac{V_{MFC}}{R_{MFC} + Z_{VR}}\right)^2 Z_{VR} \tag{82}$$

In order to obtain the maximum power condition, the derivative of P_{LOAD} with respect to R_{MFC} is taken (i.e. $\frac{dP_{load}}{dR_{MFC}} = 0$) yielding $Z_{VR} = R_{MFC}$, this result implies:

$$max\ P_{load} = V_{max} I_{max} = \frac{V_{MFC}}{2} \cdot \frac{V_{MFC}}{2R_{MFC}} \tag{83}$$

Once the operating point is found, the PMS input impedance matching is modulated by means of varying the switching frequency. The relationship between switching frequency and input impedance will be further detailed in section IV-A.

Operating point for impedance tracking

The manner in which the MPP is extracted from the MFC is through a rapid sampling of the open circuit voltage (OCV), followed by a halving process [121]. This halving of OCV sets the target value the input voltage of the PMS (V_{dc}) must reach to assure maximum power transfer. This method presents limitations when applying to a source with associated capacitance as the MFC possesses; this causes the OCV additional time to correctly reach nominal V_{MFC}. This additional time is directly related to the time constant associated to the MFC sources, τ_{MFC}. Solutions not considering this time constant would potentially miss reaching correct nominal V_{MFC} [8] due to the small amount of time allowed for the MFC to reach nominal V_{MFC}.

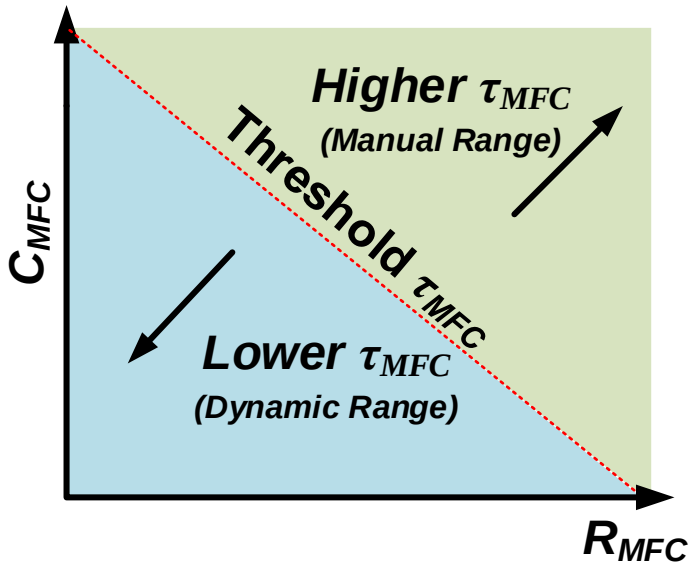

Fig. 82. Obtaining MPP voltage (V_{comp}) from the MFC through MPEA.

From the equivalent model (Fig. 80B),experimental time constant ($\tau_{MFC} = R_{MFC} \cdot C_{MFC}$) can be obtained. Variable τ_{MFC} provides information on the power delivering capabilities of the MFC. By acquiring the time constant value two different operational methods for maximum power extraction are obtained: a dynamic range and manual range of MPEA operation.

Fig. 82 shows the threshold boundary set by τ_{MFC} between manual and dynamic range. The dynamic range is defined by high power delivering capabilities (small product of R_{MFC} and C_{MFC}), allowing for the system to correctly reach MPP quickly and accurate through the OCV sampling method. The manual range is determined through large values of τ_{MFC} requiring larger sampling periods of the OCV to correctly reach nominal V_{MFC}. The threshold, τ_{MFC}, is set by design as the appropriate time required for

the MFC to reach nominal V_{MFC} from MPP ($V_{MFC}/2$). For this IC implementation the threshold τ_{MFC} is set between 25-50 ms. Large values of the τ_{MFC} threshold become impractical to implement in a fully integrated approach; thus manual range of operation is set. This is the reasoning of implementing the pre-charging scheme from the output voltage.

For the proposed PMS, the characterized MFC possesses large values for τ_{MFC}, above the determined range for integration; pushing the system into the manual range of operation. Both R_{MFC} and τ_{MFC} need not be determined with high accuracy since the PMS is capable of achieving both matching and correct MPP acquisition through correct range setting (dynamic or manual).

Since the sampling method requires disconnection of the source to the PMS in order to measure the OCV, power delivery to the output is disrupted. To avoid this disruption in power delivery, a pre-charging scheme is employed in order for the system to accurately capture the correct OCV.

MPEA and ZCST loops

Fig. 83 shows the overall block diagram of the PMS with both MPEA and ZCST loops. Once the correct value of OCV is sampled, then halved, the reference for the MPEA Impedance Tracking loop is defined (V_{comp}). This defined reference serves as the target V_{dc} is to be settled at through frequency modulation. As $V_{dc}$is continuously compared with V_{comp}, high/low signals are sent to a current-steering charge pump that

generates a control voltage. This control voltage modulates a voltage controlled oscillator (VCO) in order to have V_{dc}reach V_{comp}, assuring MPP.

The ZCST loop is implemented by monitoring the switching node V_{sw} in order to minimize losses from inductor current by modulating T_P. As the PMOS switch goes off, and the inductor current has not reached zero, an associated voltage surge is perceived at the switching node; an external reference sets the threshold for which V_{sw} can increase. The goal of this loop is to minimize the residual inductor current and move as much stored charge to the output node.

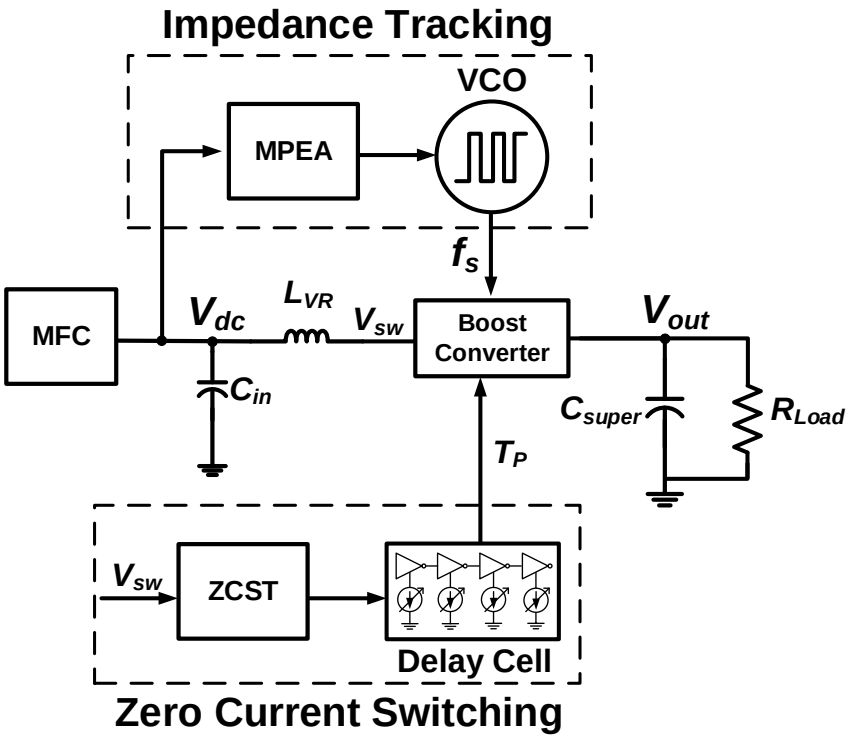

Fig. 83. Overview of the proposed PMS with the MPEA section highlighted.

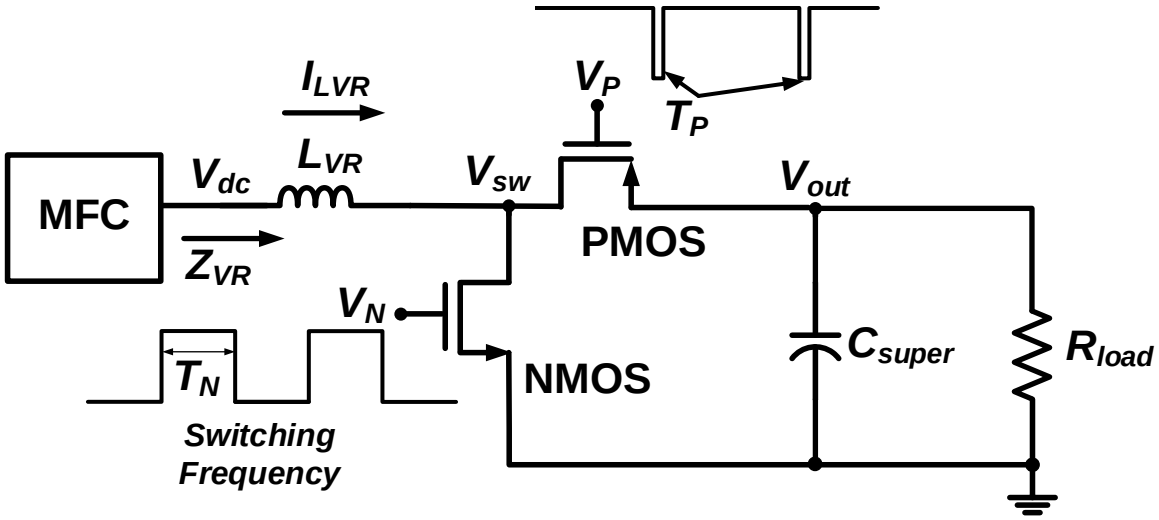

Fig. 84. Fundamental schematic of the boost converter used here as part of the PMS circuit.

The Experimental Results and Discussion section in this chapter present circuit details and voltage references on both MPEA and ZCST loop implementations.

Circuit implementation for PMS

The boost converter in Fig. 84 is a voltage step-up converter capable of increasing a DC voltage from the input (V_{dc}) to a higher DC output voltage value (V_{out}). Output current load and input power are the main limitations in terms of how much gain (V_{out}/V_{dc}) the converter can achieve.

The parameter utilized to modify the input impedance of the boost converter is the switching frequency ($1/T_s$). As the converter operates in DCM, the input impedance is derived from the averaged inductor current [8]. The expression of the input impedance can be approximated as:

$$Z_{VR} \approx \frac{2 \cdot L_{VR} \cdot T_s}{T_N^2} = \frac{2\ L_{VR}}{D_{utycycle}^2 T_s} \tag{84}$$

where L_{VR} is the converter inductor, $T_N$is the on-time for the NMOS switch, and $D_{utycycle}$ is the NMOS switch duty cycle. By defining the duty cycle for the NMOS switch to be 50% of the period (T_S), (84) yields:

$$T_N = D_{utycycle} \cdot T_s = 0.5 \cdot T_s \tag{85}$$

$$Z_{VR} \approx \frac{2\ L_{VR}}{0.5^2 T_s} = 8\ L_{VR}\ f_s \tag{86}$$

This allows the input resistance of the boost converter to vary in a linear fashion to fulfill the needs of MPP for the MFC. This permitted the implementation of a frequency-controlled input resistance of the PMS. From the system characterization and specifications in the previous section (Adaptable Maximum Power Extraction Algorithm), the input resistance to match is R_{MFC} =400Ω. Thus,L_{VR} was selected to be 1.5 mH, setting the switching frequency to 66kHz.Broad resistance matching ranges can be obtained through different inductor and switching frequency values.

The PMS also possesses the capabilities of extracting power from much lower producing MFCs. This lower power production is translated as an electrical equivalent MFC source with larger R_{MFC}. As shown in (4), the input resistance would modulate to extract maximum power matching Z_{VR} and R_{MFC}.

Operating point for impedance tracking implementation

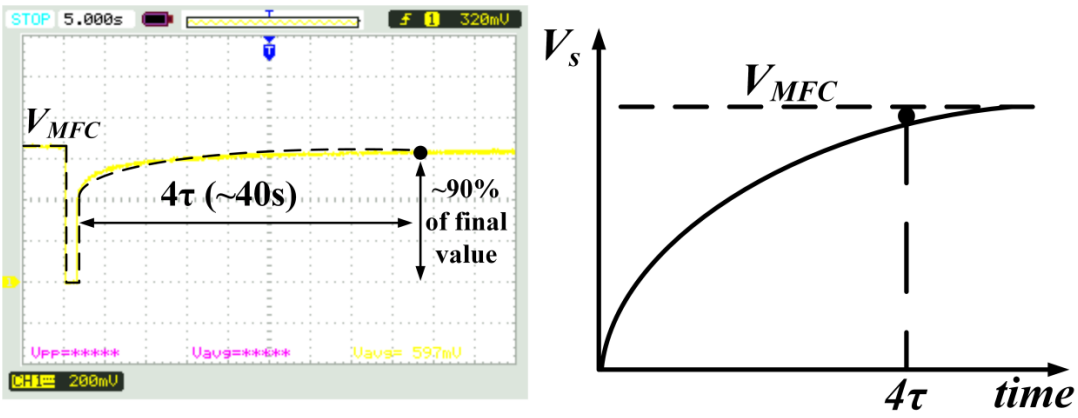

Fig. 85. (Left) Measured RC time constant (τ_{MFC}) of the MFC device and (right) illustration of time needed to charge the capacitor C_1 to read the open circuit voltage V_{MFC}.

As mentioned in the previous Section (Adaptable Maximum Power Extraction Algorithm), variable τ_{MFC} is measured and shown in Fig. 85. As with any RC circuit, τ_{MFC} is the time required to charge C_{MFC} through resistor R_{MFC} to ~63% of its final value. It can be seen that the time it takes for the RC system to reach approximately 99% of its final value is 40 seconds. This information, along with the characterized value of R_{MFC} allows an estimation of C_{MFC}:

$$\tau_{MFC} = C_{MFC} R_{MFC} = 10\ s \tag{87}$$

From (87), for an $R_{MFC} = 400\Omega$, C_{MFC} is approximately 25 mF. Note that under circumstances where no R_{MFC} is known through characterization, τ_{MFC} from testing alone can function as an indicator of MFC health, i.e. $\tau_{MFC} \gg 10s$ is an indication of

weak MFC power production. The τ_{MFC} parameter serves as a strong indicator on the MFC power delivery capabilities and PMS MPP method (Manual or Dynamic) needed in order to achieve maximum power extraction. In summary, the MFCs time constant sets the operation range of the PMS's MPP method (Manual or Dynamic).

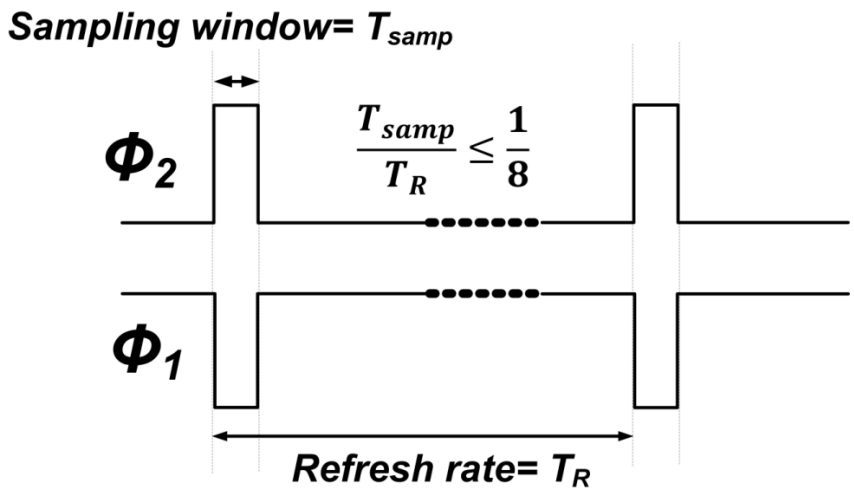

Fig. 86. Relationship between ϕ_2 and ϕ_1.

Fig. 86 illustrates the comparison between both clock phases ϕ_2 and ϕ_1. For the characterized MFC and measurements the required time for the MFC to reach nominal V_{MFC} is too large to be implemented practically in an integrated solution. For the proposed PMS, a good rule of design is to minimize the sampling window (T_{samp}) compared to the refresh rate (T_R), since T_{samp} effectively disengages the MFC from the PMS disrupting power delivery. Non-integrated solutions could potentially allow longer T_{samp} avoiding manual range operation.

The OCV sampling window is performed by phase ϕ_2 with duration T_s, and the refresh rate is performed by phase ϕ_1 with duration T_R. A 1/8th maximum T_s value with respect to T_R for the PMS is suggested to minimize power disruption. For larger values of τ_{MFC}, longer $T_{samp}$is required; hence longer values forT_R. This requires high capacity sampling capacitors ($C_1$and C_2) with low ESR to minimize leakage between each sampling window in order to minimize MPP error. This assures limited power disruption to the PMS, while correct MPP.

With the implemented approach of 1/8 ratio limit between sampling window to sampling period careful considerations should be taken when sizing $C_1$and C_2. As C_1 is placed in parallel to the MFC, this would effectively increase the associated capacitance with τ_{MFC} to be C_{MFC}+ C_1. Therefore, C_1should always be sized much smaller than C_{MFC} to avoid increasing τ_{MFC} beyond the 1/8 limit for fully monolithic approaches.

In Fig. 82, for values of τ_{MFC} lower than the time constant threshold, the dynamic range is externally set. Fig. 87 shows the sampling structure for this mode of operation; which allows for quick and dynamic OCV monitoring through two non-overlapping control signals (Fig. 86) for the sampling switches.

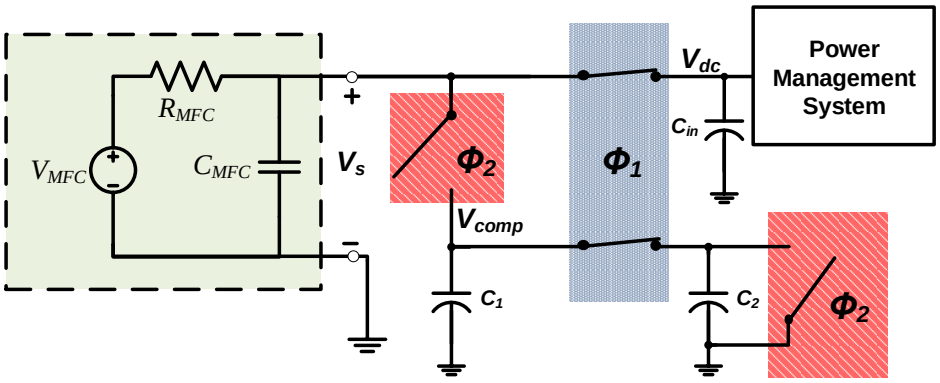

Fig. 87. Operating point tracking for dynamic range, phase ϕ_2 sampling of V_{MFC} and phase ϕ_2 dividing V_{MFC} by two.

During ϕ_2 the open circuit voltage V_{MFC} is stored in C_1 (Fig. 87). During ϕ_1, the charge stored in C_1 is shared with C_2 through the associated controlled switches. Since both capacitors have the same value, the voltage at node V_{comp} becomes equal to $V_{MFC}/2$ due to charge redistribution between the two capacitors. Phaseϕ_2 pulse duration, T_{samp}, needs to be at least equal to $4\tau_{MFC}$ (Fig. 85) in order for C_1 to be charged to a value close to V_{MFC}. The timing is achieved through a dedicated one-shot circuit with external tuning to achieve the required sampling window for ϕ_2. Fig. 88 shows experimental correct MPP being achieved under electrical equivalent circuit for a high powered MFC ($\tau_{MFC} = 5$ ms).

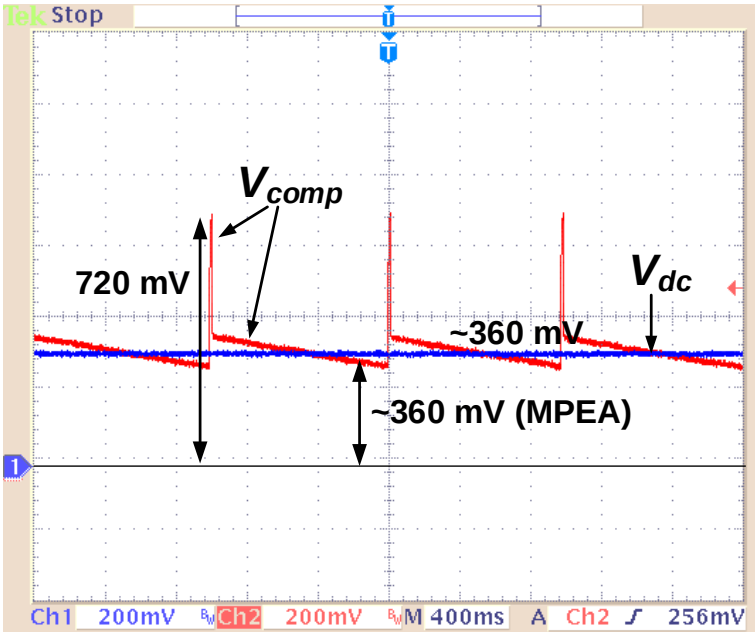

Fig. 88. Dynamic range showing correct MPP.

For the measured MFC, with large value τ_{MFC}, the manual range is externally set. In order for the MPP be achieved without large power disruption to the PMS, a pre-charging scheme for the sampling capacitors ($C_1$and C_2) is employed. This eliminates the need to disengage the PMS from the MFC required to sample the open circuit voltage ($V_{MFC} = V_s$). Fig. 89 shows the manner in which the manual range achieves the characterized 720 mV of the MFC. The pre-charging scheme is implemented through a similar sampling approach as the dynamic range, but without sensing the MFC's OCV, through a resistor divider from V_{out}. Since the output voltage node is set to a fixed value (2.5 V), the MPP can be obtained via a divider network. The same sampling phases, $\phi_2$and ϕ_1, are used to obtain V_{comp}.

The threshold, τ_{MFC}, for the dynamic/manual range is set to 25 ms. This allows a sampling window of 100 ms (4 τ_{MFC}) to be applied with a 800ms value for T. From (88), solving for R_{tune} sets this resistor value to 404 kΩ, with a 1 MΩ value for R_x, to achieve 720 mV from the 2.5 V at the output node.

$$V_{comp} = V_{out} \frac{R_{tune}}{R_x + R_{tune}} \tag{88}$$

Fig. 90 shows the correct MPP being achieved for the system tested in Fig. 85 through the pre-charging scheme proposed for the PMS. A note of importance is to consider capacitance values capable of maintaining correct charged voltage over the entirety of T_R. Issues such as leakage must be carefully accounted for otherwise voltage V_{comp} will negatively affect the MPEA loop.

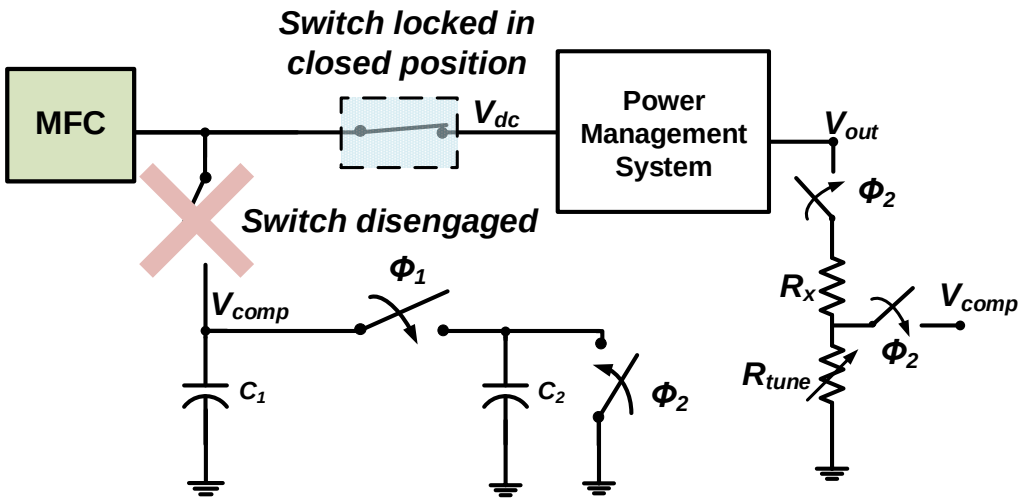

Fig. 89. Operating point tracking for manual range, (ϕ_2) sampling of V_{out} and (ϕ_1) dividing V_{comp} by two.

The proposed MPP acquisition effectively reduces the required time for the PMS to locate and operate at MPP compared to conventional polarization curve approaches [39].

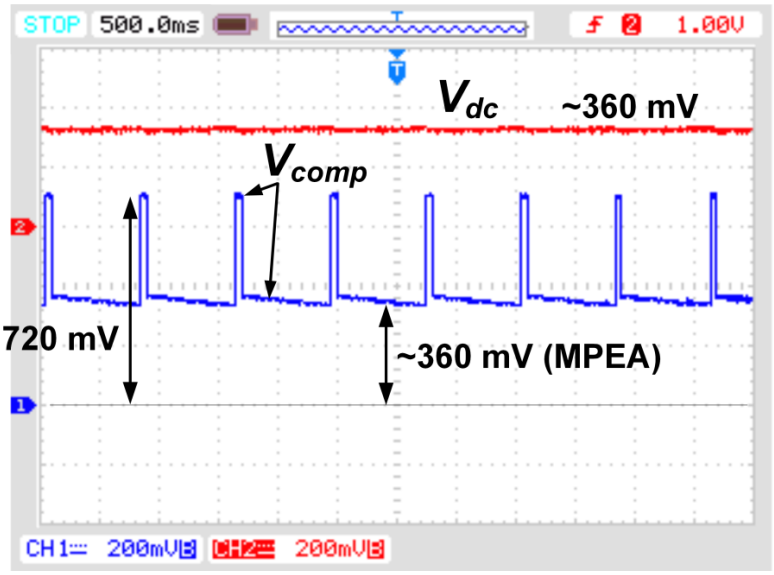

Fig. 90. Manual range showing correct MPP.

It should be noted that if the OCV were to drastically change from the set MPP voltage through the resistive divider, maximum power extraction would not be achieved. A possibility would be to reset the resistive divider to recalibrate to MPP. Nonetheless, it is well documented [122, 123] that MFC OCV does not vary significantly over long periods of time.

MPEA implementation

Fig. 91 present the main blocks which make up the dynamic MPEA. Once the desired operating point is stored in C_1 (V_{comp} from Fig. 87, Fig. 89), this is compared to the value at the input of the boost converter (V_{dc}).

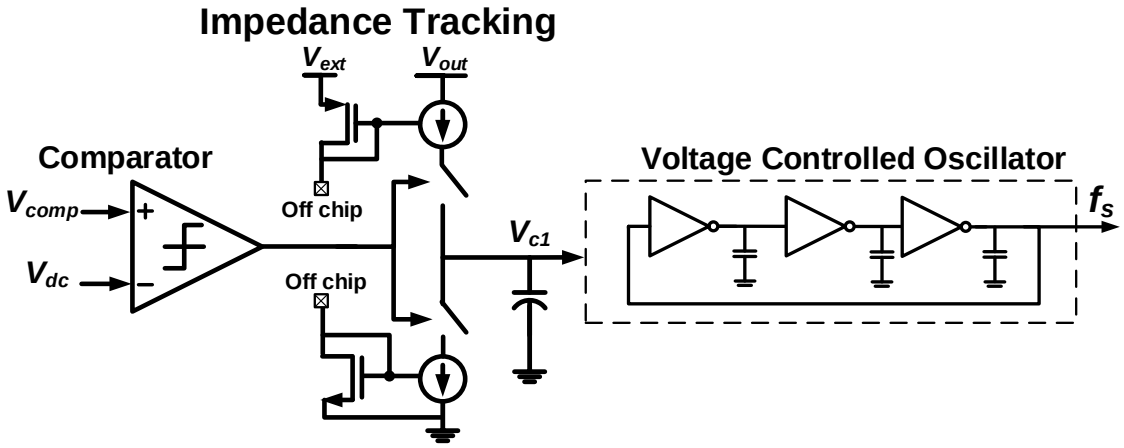

Fig. 91. Impedance tracking scheme for MPEA.

Depending on the voltage level of V_{dc}, a comparator sets a control voltage for a VCO, implemented by a ring-oscillator, in order to modify the input impedance of the boost converter and match R_{MFC}.

The implemented charge pump injects packets of charge into the control voltage node (V_{C1}) through externally biased switched current sources.

Zero current switching tracking loop

A critical component regarding efficiency is the duration of T_P (PMOS on-time duration). Previous methods have proposed setting a fixed period [17] or toggling values to reduce reverse inductor current losses [8]. While these efforts improve on synchronous switching they still lack fine tuning capabilities to minimize losses due to inductor current achieving negative values.

As previously explored in [8, 17], when the PMOS switch switches off, and the inductor current has not reached zero, an associated voltage surge is perceived at the switching node (V_{sw} Fig. 83) of a boost converter. This voltage surge, shown in Fig. 92, is proportional to the rate of change of the remaining current in the inductor when the PMOS switches off. Ideally the inductor current would fall to zero before the PMOS is switched off, thus, reducing any losses associated with this switch (Fig. 92). The proposed solution to minimizing these potential losses associated with negative inductor current is through a dynamic Zero Current Switching Tracking (ZCST) loop.

Fig. 93 shows how the tuning of the T_P parameter is tuned via the ZCST loop. The process behaves in the reverse manner when the inductor current falls below zero.

As with the Impedance Tracking loop, the ZCST loop requires externally biased current sources in order to deliver a V_{c2} to the inverter delay cells. The V_{sw} node surge upper limit is determined through an external reference,V_{zref}, tuned to minimize inductor current losses.

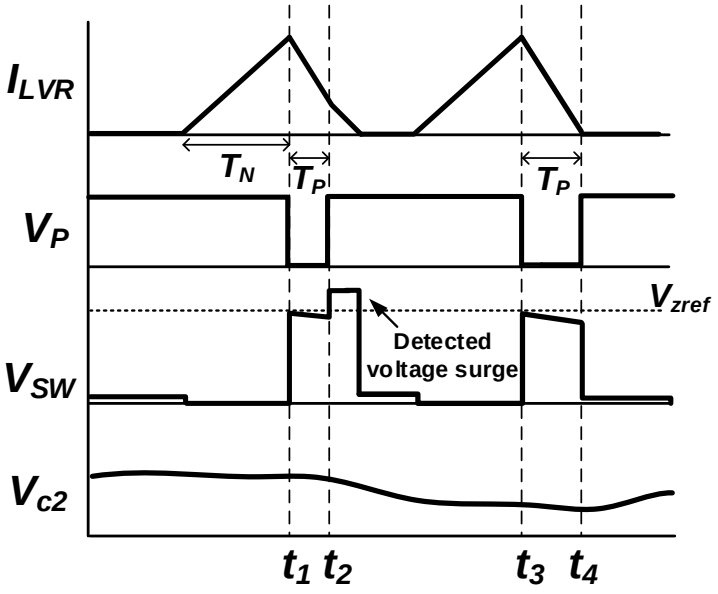

Fig. 92. Inductor current and ZCST parameters.

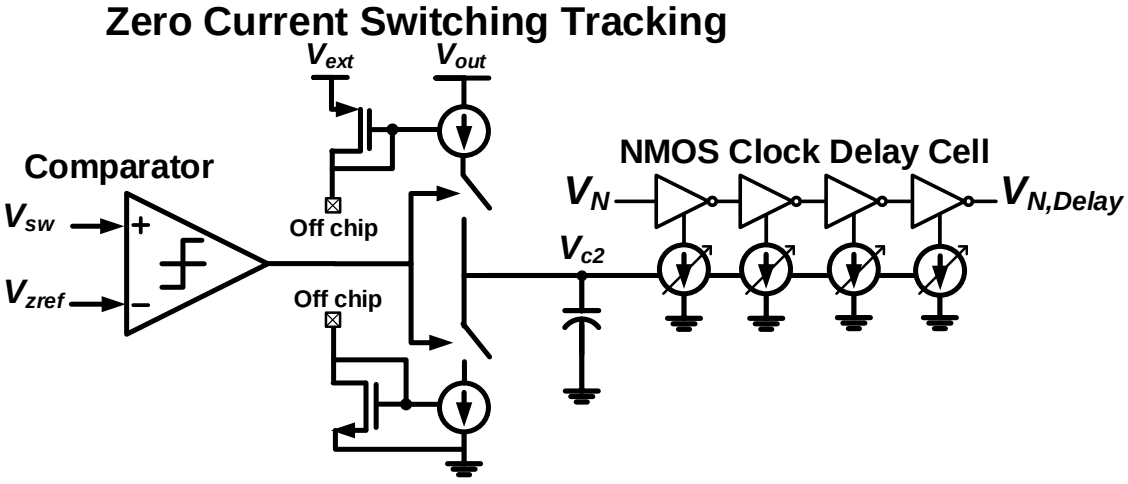

Fig. 93. Zero current switching tracking loop for T_p time control.

The ZCST loop minimizes the losses from the inductor current by setting T_P time through an adaptive inverter delay cell controlled by the comparison of the voltage surge from V_{sw} and V_{zref}. Whenever the voltage surge exceeds V_{zref}, the control voltage V_{c2} starves the delay cell of available current, effectively slowing down the signal $V_{N,Delay}$ used to generate the PMOS signal (T_P) [8]. V_P determination is next discussed.

Output voltage setting

The output node voltage, V_{out}, is constantly monitored by a secondary comparator that turns the entire PMS on or off depending on the reference voltage level, V_{REF}; if V_{out} exceeds the set reference voltage, the system automatically stops operating and waits until V_{out}drops below the reference level. This is common practice in energy harvesting power management systems [17, 86, 97, 121]. To assure that enough conversion gain is achieved by the boost converter, T_P is set much smaller than the T_N. Fig. 77 shows how the T_P (V_P) signal is obtained from the $V_{N,Delay}$ signal (ZCST) and logic gate approach (Fig. 94).

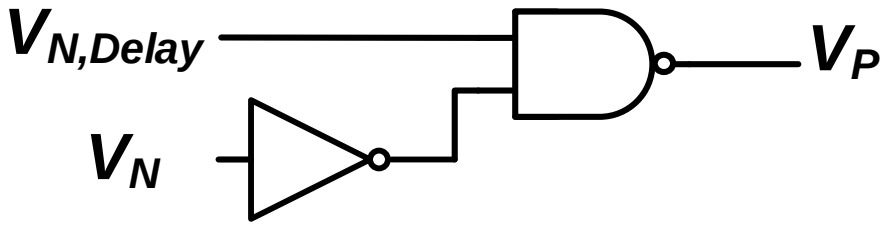

Fig. 94. V_P generation for T_P signal.

The small value of $T_P$assures enough conversion gain as stated by the conversion gain equation [20]:

$$V_{out} \approx \left(1 + \frac{T_N}{T_P}\right) \cdot V_{in} \tag{89}$$

Setting a high value for $\left(1 + \frac{T_N}{T_P}\right)$ always assures to be enough to achieve 2.5 V at the output. The conversion gain (V_{out}/V_{in}) is always maximized through the ZCST loop, minimizing inductor current losses.

Fig. 95 shows how the output voltage setting is performed. In order to fix the output voltage, a global enable is employed through a division of V_{out} and comparing it to a 1.25 V reference.

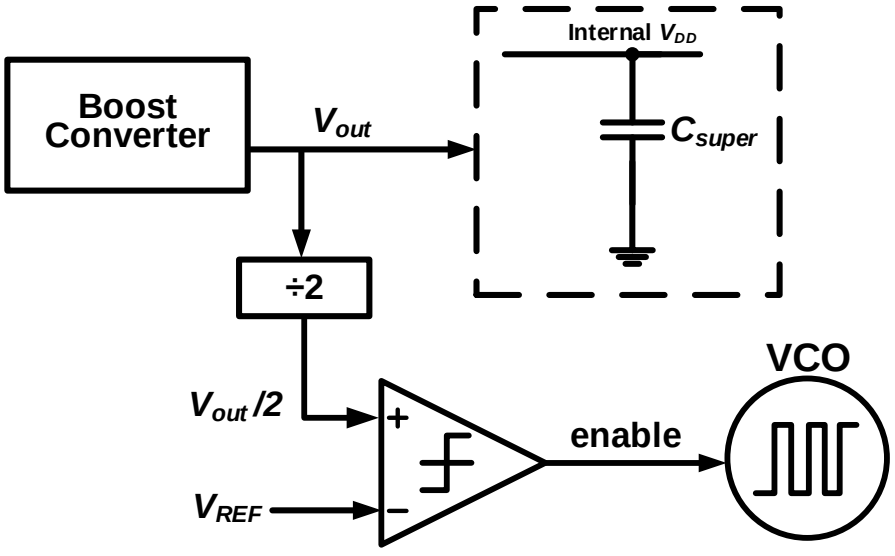

Fig. 95. Internal voltage supply for controller and driver acquisition fromV_{out}.

Power management system startup

As the output voltage level of the MFC is not high enough to allow for self-starting operation from the PMS. An external one-time pre-charging of the output capacitor to 900 mV is required to begin controller operation. Multiple different approaches may be taken to startup the system [88, 124].

Once the system begins extracting energy from the MFC, there is no longer need for an external power source to power the PMS.

Experimental results and discussion

Fig. 96 showcases the testing setup for the complete PMS. The complete PMS was fabricated in 0.5 μm CMOS technology with an active area of 0.8mm^2, die photograph is shown in Fig. 97. The measurements were performed with a storage capacitor C_{in} of 10mF, a super-capacitor C_{super} of 0.1 F, and external biasing and references.

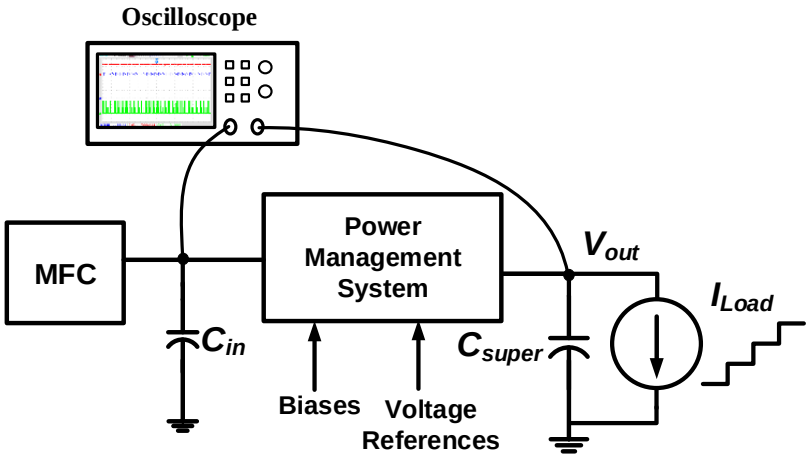

Fig. 96. Overall testing setup to characterize the PMS controlling the MFC.

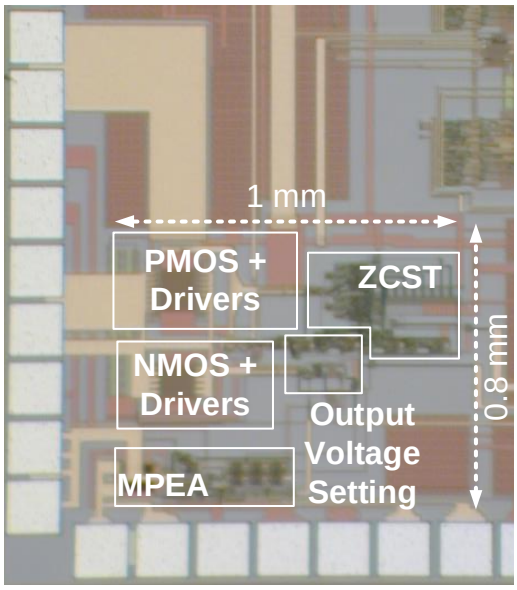

Fig. 97. Die microphotograph.

To begin testing the steps taken are the following: i) biases for both MPEA and ZCST are set externally through off-chip supplies, ii) the output voltage reference of 1.25 V is set for the Output Voltage Setting block, iii) Reference V_{zref} set to 625 mV for the ZCST block, iv) the manual range is set, for the presented MFC, through an external pin set to the lowest potential (not shown in Fig. 20), and finally v) testing is performed by an external initial pre-charge on C_{super} to 900 mV. The pre-charge allows the control circuit to being switching operation and extraction from the MFC follows.

Maximum power extraction algorithm

Fig. 98 showcases the MPEA correctly achieving MPP at 360 mV with a switching frequency of approximately 65 kHz. Measurements were performed by pre-charging the output capacitor, C_{out}, to 900 mV to allow the system to begin operating.

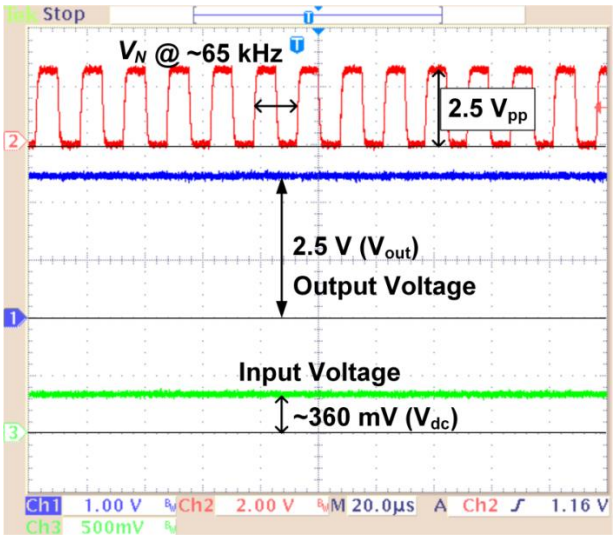

Fig. 98. Input and output voltage profiles at steady state with ~75µA load.

The manual range was externally set with R_{tune} sets to 404 kΩ, with a 1 MΩ value for R_x, to achieve 720 mV from the 2.5 V at the output node

It should be noted that frequency variations are to be expected due to the continuous comparison between V_s and V_{comp} that results in dynamic toggling of the control voltage V_{c1} (Fig. 93) to vary slightly around the correct operating point. The output voltage value of approximately 2.5 V was successfully achieved with a load of ~75 µA.

Zero current switching tracking

Fig. 99 shows the ZCST loop minimizing the voltage surge from the early PMOS off time. V_{zref}limits the voltage surge related to V_{sw} (Fig. 83).

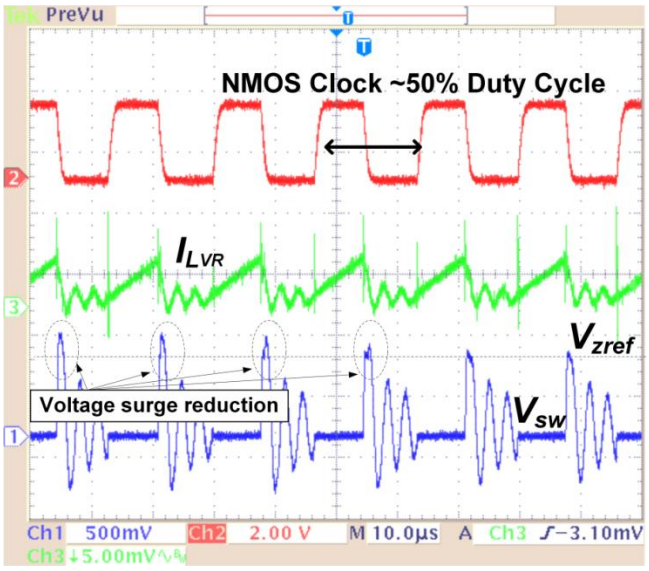

Fig. 99. ZCST loop minimizing losses from inductor current switching.

The external reference V_{zref} was set to 625 mV as the threshold for the voltage surge detection at node V_{sw}. Voltage surges detected at V_{sw}can be seen effectively decrease as the ZCST loop increases T_P to minimize residual inductor current.

Total power consumption and efficiency

Fig. 100 shows overall power consumption for both static (quiescent) and dynamic; total power consumed is 13.16µW.

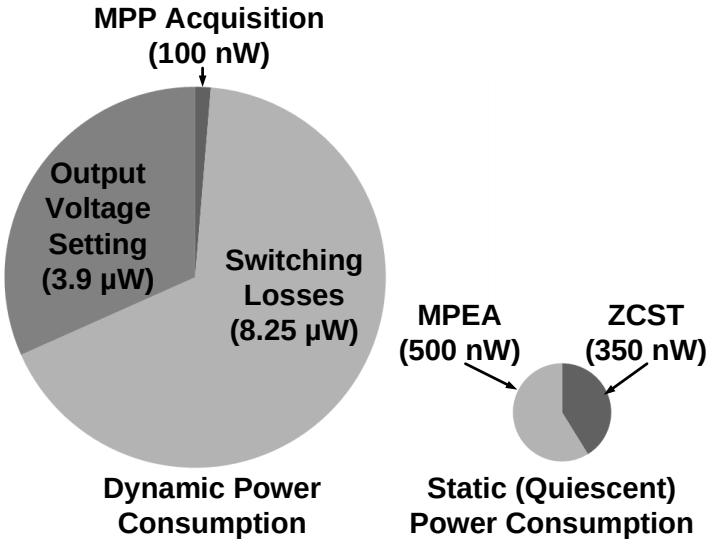

Fig. 100. Overall PMS power consumption breakdown.

Fig. 101 shows the efficiency profile. The efficiency of the PMS was measured for varying loads. Maximum efficiency was recorded at ~58% with a load of ~250 µW. TABLE 10 summarizes and compares the presented solution to previously reported systems. It should be noted that the proposed solution is the only system possessing quiescent power consumption below 1 µW, as well as taking circuit dynamic power consumption into account in the efficiency measurements. Efficiency is considered dynamic as it does not take into account the effects of the 1 µW quiescent; this is performed in the same fashion as references in TABLE 10. Thus, the presented PMS achieves a significantly higher efficiency compared to previously reported PMSs for MFCs.

TABLE 10. Comparison of MFC power management units.

SPECIFICATION	[102]	[125]	[6]	[126]	[107]	THIS WORK
Input Voltage Range	300mV	300mV* 180mV**	300mV	300mV (startup at 140mV)	300mV	300mV-720mV
Output Voltage	1.8V	3.3V	2.5V	1V	3.3V	2.5V
Inductor	2μH	7.5μH** (primary winding transformer)	110mH	326.7μH (primary winding)	1:20 transformer	1.5mH
Output Capacitor	47μF	0.25F* 1.5F** (supercapacitors)	1F (supercapacitors)	8μF	680μF 0.4F (supercapacitor)	0.1 F (supercapacitor)
Maximum Power Extraction	-	-	Hysteresis Control	-	-	Adaptable MPEA tracking
Max. Efficiency	-	5.33%* 4.29%**	-	73%†	53%†	58%‡
Implementation Approach	Discrete Components	Discrete Components	Discrete Components	Discrete Components	Discrete Components	Custom IC

*Charge Pump + Boost converter topology
**Transformer + Boost converter topology
†Does not take into account system power consumption
‡ PMS operates with <1μW of quiescent power consumption

Comparison between similar CMOS implementations focused on extracting maximum power from energy harvesting sources, other than MFCs, would require higher power for the MPP control) [20, 127-129] compared to the proposed MPEA presented (~600 nW for only the MPEA control). It should be noted that switching losses, comprising the majority of the circuits' power consumption, can potentially be reduced if the system were to be implemented in a smaller technology, i.e. 180 nm CMOS process or smaller.

Discussion

While the use of the pre-charging scheme for the proposed PMS is implemented, an alternative approach would be to directly power from a battery at V_{batt}, as seen in Fig. 102. While the battery is needed to start the system and deliver the appropriate biases and references at startup, once the system begins extracting power from the MFC, it can then store the extracted energy back into the battery.

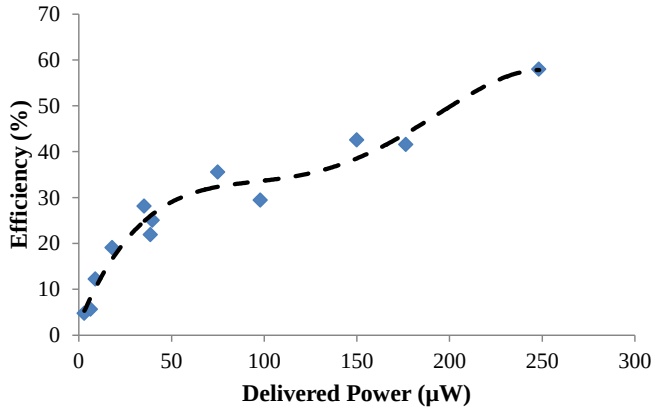

Fig. 101. Measured efficiency vs. delivered power.

Both references and biases, used in the ZCST and MPEA, would potentially be generated internally through low-power integrated temperature stable reference consuming sub-µWs of power [130, 131] (bandgap voltage references). Due to the low power extracted from the MFC (~320 µW) a rechargeable battery can be directly charged from the PMS output with the assurance no damage to the chemistry will occur.

This scenario would be plausible with MFCs delivering power over 13.6 µW (dynamic power of 12.25 µW +static power of 0.85 µW) plus the additional reference power requirements from the temperature stable references. This possible scheme would enable a much longer up-time operation for the wireless sensor. A small amount of invested power to increase the system's operational lifetime would be the requirement.

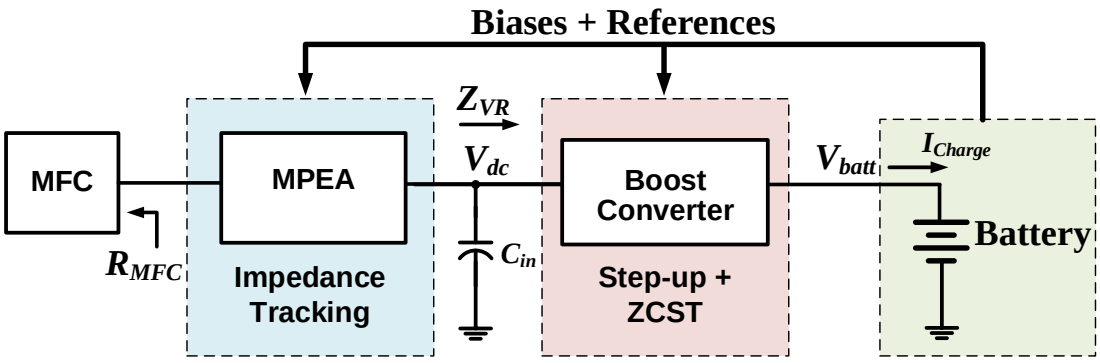

Fig. 102. Possible implementation with presented PMS for battery extending operation.

Conclusions

MFCs can generate renewable energy from waste organic substrates such as wastewater and other biomass by using the metabolic process of electrochemically active bacteria. Due to their inherently low power and voltage profiles however, power management systems are required to process the MFC power to a usable voltage levels such as CMOS compatible voltage. This chapter presents a singular dynamic MPEA DC-DC converter IC chip for efficiently managing power outputs of MFCs.

The presented monolithic boost converter is capable of sampling and locating the MPP and setting the input resistance to match that of the internal MFC resistance, hence continuously operating the system at MPP. Previous works cannot accomplish this with the MFC's complex impedance. This proposed solution presents a quicker approach to MPP compared to conventional MFC characterization through polarization curve approaches. The MPEA is capable of dynamically matching the impedances of the MFC that continuously changes over time. The MPEA also continuously extracts maximum power from the MFC even when its power level changes over time. In order to reduce inductor current losses by modulating T_P time duration a ZCST loop is introduced. The PMS was fabricated using a 0.5μm CMOS technology and demonstrated a maximum dynamic efficiency of ~58% for a load of ~250μW.

CHAPTER V

AN INDUCTORLESS DC-DC CONVERTER FOR AN ENERGY AWARE POWER MANAGEMENT UNIT FOR MICROBIAL FUEL CELLS[*]

Introduction

The research behind novel renewable energy sources has always been a critical and major driving force in technological innovation. One of the breakthroughs in renewable energy technologies has been the development of new and highly efficient power management units (PMU) for energy harvesting (EH) systems. EH-PMUs are focused on two major tasks: 1) extract maximum power from the renewable source, and 2) offer an acceptable and well-regulated voltage/current profile for the power delivery chain.

Major results have been accomplished for several different EH sources, i.e., solar, kinetic, RF, and thermoelectric [132-135]. However, fully integrated solutions where biomass is used as a source are still few, and PMU solutions have yet to tackle extreme low power producing systems such as microbial fuel cells (MFC) [136]. Due to their inherent low power production, power extraction from MFCs requires extremely efficient and low power PMUs.

The power profile of an MFC varies with pH level, temperature, and amount/type of substrate in the anode chamber [118, 137]. Over time, these aforementioned effects

[*] Reprinted with permission from "An Inductorless DC-DC Converter for an Energy Aware Power Management Unit Aimed at Microbial Fuel Cell Arrays" by S. Carreon-Bautista, C. Erbay, A. Han, and E. Sanchez-Sinencio, 2015. IEEE J. of Emerging and Selected Topics in Power Electronics, Early Access Article, 2015, © 2015 IEEE

compound and reduce the maximum power delivered by the MFC. This overall power degradation or fluctuation limits the potential of applying a single MFC for a continuous load demanding system for any long up-time operation, and an MFC system would require careful monitoring of the MFC health. A possible solution lies in implementing a large volume MFC in order to maintain up-time for as long as possible [102] or intermittent operation of PMUs [138]. Efforts of placing multiple devices in series or parallel configuration are possible in order to improve either output voltage (series connection increases equivalent output voltage), or reduce internal equivalent resistance (parallel connection increases current delivering capability). However, due to the nonlinear effects of the bacteria in MFC, variations in power production between devices leads to unequal voltage drop when placed in an array fashion and hence, limiting the overall power delivered by the array [139]. In fact, no current solution truly tackles the low power density and wide range MFC parameters over time.

The proposed solution is to perform a time multiplexing harvesting approach, where MFCs are harvested individually at MPP to avoid the issue of voltage reversal, yet benefiting from an a higher power density achieved from an array configuration. The present chapter presents an inductorless DC-DC converter (I-DCDC) which allows for dynamic tracking of the optimum point for maximum power extraction from an MFC array. The I-DCDC is part of an Energy Aware Power Management Unit (EA-PMU), comprised of a power sensing and aforementioned I-DCDC converter. The I-DCDC is implemented with a Charge Pump Dickson topology [57]. The EA-PMU performs a power detection (PD) algorithm that locates the optimum MFC within the MFC array for

power extraction. Once the best MFC is located, the I-DCDC begins harvesting from the selected MFC through a rewiring process, achieving maximum power point tracking (MPPT) via a frequency modulation scheme (FMS). The proposed system is a novel approach towards tackling MFC power profile degradation due to MFC internal variations and towards effectively increasing power extraction by implementing a multiplexing harvesting of MFC arrays.

MFC array and power extraction methodology

An MFC possesses nonlinear behavior when mapped to an equivalent electrical circuit with initial approximations showing the effects of non-idealities [117, 118]. As power is being extracted from an MFC, its performance degrades over time and delivers less power if not replenished with a feeding solution. Another set of factors affecting power performance of an MFC are: size, pH, temperature, and substrate concentration in the anode chamber [118]. This causes challenges in maintaining a certain level of power and voltage for the load.

For the proposed application, an MFC array is established from which maximum power can be extracted from individual cells, maximizing the overall system efficiency. Under this scheme, power from an individual MFC is harvested without the need of previously knowing the optimum point of power extraction, contrary to previous solutions implementing [140] multiple MFCs, the proposed converter can achieve MPP power extraction at all times. The MPPT scheme locates and dynamically adjusts the system parameters for the power converter to achieve a maximum power extraction.

The power detection of MFCs is performed in order to quickly switch between the healthiest cells within the array. Once the healthiest MFC is selected, the PD algorithm continues monitoring the rest of the array for a set period of time and selects the best available candidate. The PD algorithm can be implemented in a variety of ways such as: a microcontroller or a fully-integrated Finite-State-Machine (FSM).

State-of-the-art

Current power management solutions implementing MFCs as their power source are limited in application and require large external components (inductor) [102, 136, 141], or suffer from complex implementation [142]. The issue of power degradation and functional array implementation of MFCs has yet to be tackled in an efficient and automated manner.

Previous efforts aimed at placing harvesting sources in an array fashion [112] consider only resistive components when achieving MPP. Since the impedance the MFC yields both resistive and reactive components, any array type approach where rapid reconnection occurs between the DC-DC converter and the MFCs must tackle stability issues in a more stringent fashion. Another multi-source approach with an LC switching converter, which differs from the dynamics of a fully integrated capacitive DC-DC converter, has also been presented [112]. The proposed implementation via a fully capacitive DC-DC converter alone requires new understanding on the I-DCDC's particular interaction with the MPPT control loop.

Thus, this type of approach requires a sound implementation in order to tackle the different MFC power profiles, and to show how energy harvesting MPPT control loop dynamics are affected by it.

MFC construction and operation

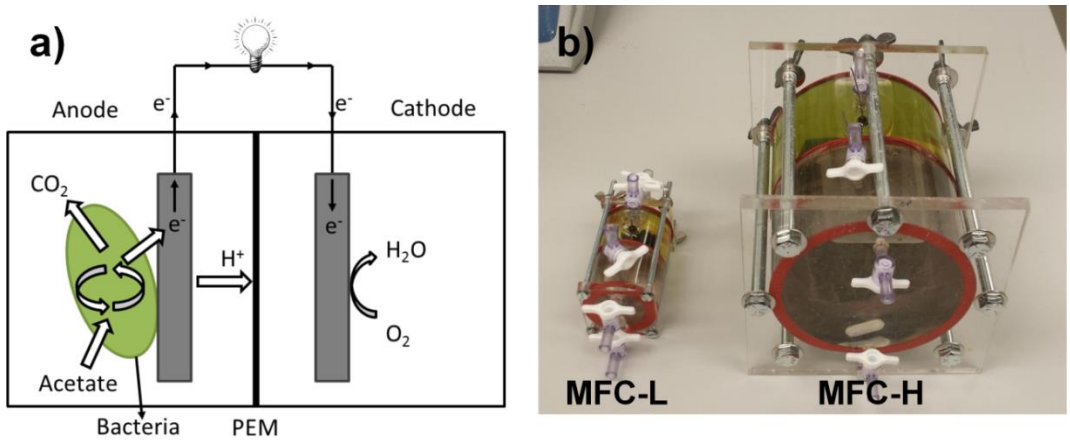

Fig. 103. a) Schematic of a two chamber microbial fuel cell. b) The small (MFC-L) and large (MFC-H) devices used with I-DCDC.

MFCs are bio-electrochemical, energy-producing devices that convert chemical energy into electrical power by the catalytic activity of living bacteria. MFCs are similar to other fuel cells, consisting of anode and cathode chambers separated by a proton exchange membrane (PEM) as shown in Fig. 103a. In the anode chamber, fuel is oxidized by the bacteria, generating CO_2, electrons and hydrogen atoms. The electrodes in each chamber connected through a resistor load and generated electrons are

transferred to the cathode electrodes, while protons are moved to the cathode chamber through the membrane.

The MFCs were assembled by connecting two acrylic chambers separated with a PEM (Nafion 117^{TM}, Ion Power Inc.). Carbon felt (Morgan, UK) was used as the anode and carbon cloth with Pt catalyst on one side (10wt% Pt/C, 0.5 mg Pt/cm^2, ElectroChem, Inc.) was used as the cathode. Anaerobic activated sludge (Austin Wastewater Plant) was used as the inoculum. The anode chamber was filled with wastewater, containing 1 g/L acetate and autoclaved anaerobic nutrient mineral buffer (NMB, pH 7.0) solution [113]. Two different size MFC configurations were used to test the EA-PMU. The larger MFC (MFC-H) had 1 L total volume with 100 cm^2 anode and 50 cm^2 cathode electrode areas. The smaller MFC (MFC-L) had 20 mL total volume with 2 cm^2 anode and 1 cm^2 cathode electrode areas, both MFC devices can be seen in Fig. 103b. The cathode chambers were filled with potassium ferricyanide (100 mM). During the startup phase, the MFC was connected with an external resistor (1 kΩ), and the voltage across the resistor was monitored through a multiplexer (National Instruments) for continuous voltage measurements via a LabVIEW^{TM} (National Instruments) interface [114, 115, 143] and additional acetate was fed intermittently when the voltage generation was lower than 50 mV. A polarization curve was obtained by varying the load resistances (10 Ω-50 kΩ).

MFC electrical equivalent circuit

Power profile tests were performed on multiple MFCs, showing that ranges for series resistances (R_{MFC}) varied from 100 Ω to 8 kΩs, with open circuit voltages ranging from 600 mV to 800 mV. A second critical issue regarding the electrical equivalent circuit for an MFC is the parasitic capacitance associated with the MFC (C_{MFC}) ranging from 6.5 μF to 2.5 mF. Both associated components (R_{MFC} and C_{MFC}) seen in Fig. 104 affect the maximum power extraction parameters for a power conversion system.

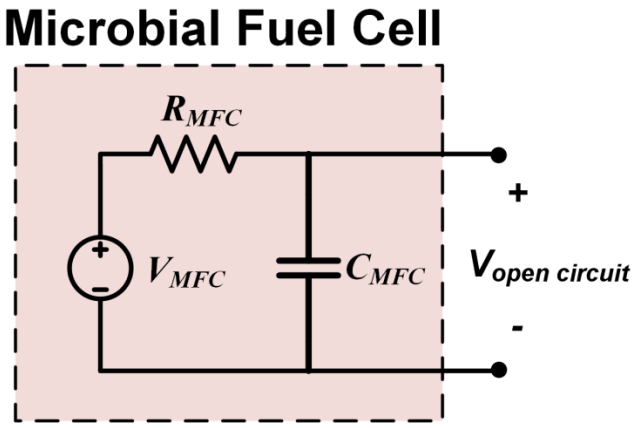

Fig. 104. Simplified electrical equivalent circuit for an MFC device.

Multiple characterization trials were performed on the MFC devices within the array in order to quantify both associated components. TABLE 11 summarizes upper and lower values obtained through the characterization process for the 20 mL MFC (MFC-L) and 1 L MFC (MFC-H).

Obtaining these parameters for high/low power MFCs is critical in the design of the I-DCDC converter in order to assure MPPT stability ranges after reconnection between cells.

TABLE 11. Microbial fuel cell parameters

SPECIFICATION	VALUE RANGE
$\boldsymbol{R_{MFC}}$	$0.1\ k\Omega - 8\ k\Omega$
$\boldsymbol{C_{MFC}}$	$6.5\mu F - 2.5mF$
$\boldsymbol{V_{MFC}}$	$600mV - 800mV$

Inductorless DC-DC converter

Fig. 105 presents the proposed overall structure of the EA-PMU with the I-DCDC block being featured in this article. Section IV-C further elaborates on the design and specifications of the converter. The I-DCDC converter is comprised of a variable stage, 10X Dickson charge pump (CP) capable of dynamically achieving MPPT over a wide range of MFC impedance scenarios. The number of stages in the CP is automatically set depending on input voltage and load current conditions of the converter through a stage control loop monitoring the output voltage node. Likewise, a frequency modulation scheme (FMS) is also implemented in order to achieve automatic input resistance matching through an MPPT loop, between the converter and the MFC input resistance (R_{MFC}). MFCs behave as DC voltage sources, where variations occurring on the DC voltage of the MFC can be considered negligible i.e. low frequency,

the maximum power transfer theorem states [120] that maximum power is transferred when a DC source (V_{MFC}) with fixed source resistance (R_{MFC}) is connected to a load resistance (R_{in}) of equal value to the source resistance, causing the input voltage to be $V_{MFC}/2$ (V_{MPP} in Fig. 105). A capacitive divider is implemented to obtain the correct reference of V_{MPP}. As the PD algorithm switches within the MFC array, the MPPT control loop must assure that the I-DCDC converter reaches MPP in a fast and stable manner. Since MFCs are selected based on their power availability, it is possible that this can result in switching between a low-power (*high valued* R_{MFC} *and* C_{MFC}) cell to a high-power (*low valued* R_{MFC} *and* C_{MFC}) cell.

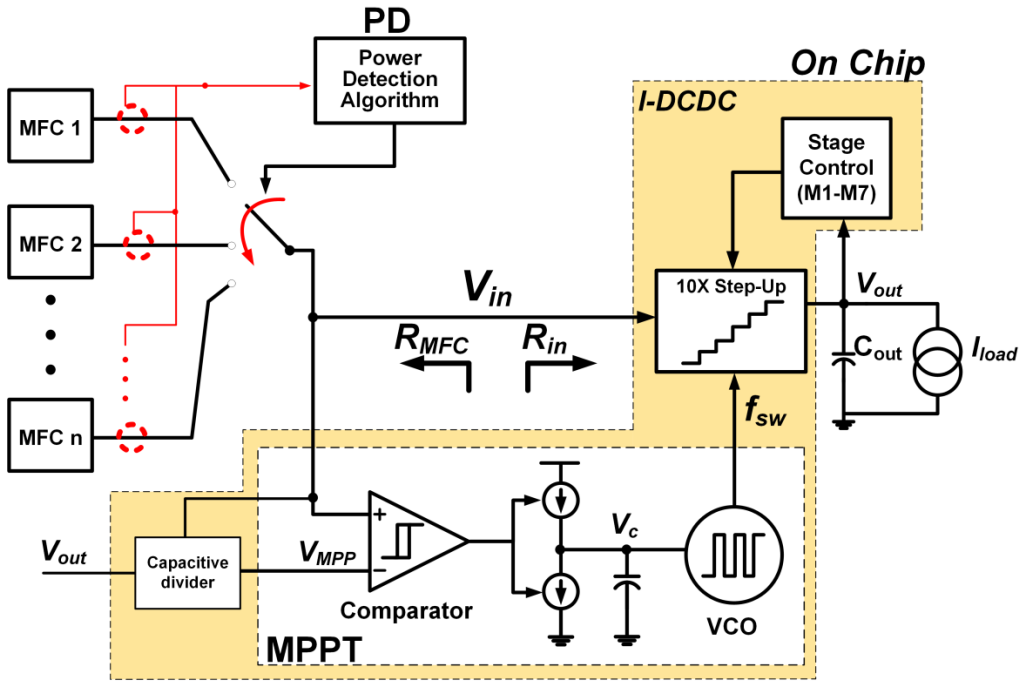

Fig. 105. Proposed structure of the energy aware-power management unit.

Since the process of extracting power from the MFCs follows a time interleaved approach, the reconnection scenario can potentially result in a faulty and unstable MPP acquisition due to the strong effect of switching between low- and high-power producing MFCs (small and large values of R_{MFC} and C_{MFC}). Stability considerations will be further discussed in the following section titled: Maximum Power Extraction for MFC Arrays.

Maximum power extraction for MFC array

The main goal of the MPPT control loop is to achieve resistive matching, between R_{MFC} and R_{in}, in order to ensure maximum power transfer from any individual MFCs within the MFC array by modulating the switching frequency. Frequency modulation is commonly used in low-power applications where efficiency at light loads and low power consumption of control circuitry are critical [55]. FMS was selected for the control method since traditional approaches, which have variable duty cycles have a limited effective control range over which regulation may be applied on capacitive DC-DC converters [62, 144]. The downside of the FMS approach is that the noise spectrum and EMI for successive blocks in the power chain is increased. Since the proposed EA-PMU application is intended for intermittently operating sensor nodes, a large storage capacitor at the output of the converter offers significant noise suppression.

As with most energy harvesting applications, the main focus of the EA-PMU is to deliver as much power from the harvesting source to the load at the appropriate voltage levels.

Once the voltage levels are attained, the controller is disengaged to minimize power consumption. Two main operating conditions are determined: storage efficiency and current demanding load scenario. For the first condition, multiple storage capacitors can be sequentially charged in order to keep the PMU operating for long periods of time. For the second condition, a load demand proportional to the input power from the MFC requires the system to maintain operation in order to achieve the required output voltage. The output voltage regulation aspect of the converter is achieved by fixing the output voltage to a predefined level by always extracting maximum power from the input source. Any load demand beyond the available input power (operating at MPP), would result in a voltage drop at the output of the any converter.

Input resistance for I-DC DC

As mentioned in the previous section, the source resistance range of the MFCs characterized were between 100 Ω to 8 kΩs. This indicates that the proposed converter must be capable of matching these values to its own input resistance. In order to calculate for the input resistance of the converter, the procedure established in [145, 146] allows for quantification of the input resistance with averaged values for input and output voltages. For the step-up Dickson CP topology, assuming ideal charge transfer switches, the expression for the input resistance is:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{N}{A_{Ideal}\, C_i\, f_{sw}\, \Delta A_{gain}} \tag{90}$$

where the components in N, C_i, f_{sw}, A_{Ideal}, and ΔA_{gain} are the number of stages, capacitance per stage, switching frequency of the converter, ideal voltage gain expression ($A_{Ideal} = N + 1$), and difference between actual voltage gain expression ($A_V = V_{out}/V_{in}$) and the ideal gain ($\Delta A_{gain} = A_{ideal} - A_V$). A_V calculated assuming ideal charge transfer switches yields:

$$A_V = (N+1) \cdot \left(\frac{1}{1 + \frac{N}{C_i \, f_{sw} \, R_{Load}}} \right) \tag{91}$$

$$\Delta A_{gain} = \frac{N+1}{1 + \frac{C_i \, f_{sw} \, R_{Load}}{N}} \tag{92}$$

The first term of A_V, $(N + 1)$, is the ideal voltage gain of the converter and the second term makes up the efficiency of the system and how it is affected by number of stages (N), frequency, and load. A more elaborate efficiency expression, including effect of parasitic capacitances, is found in [67]. As stages increase, both input resistance and overall efficiency decrease.

Fig. 106 presents the variable input resistance range of the I-DCDC for an increasing number of stages (N) [42], and switching frequencies for the converter. As the number of stages is reduced the equivalent input resistance range for a given switching frequency is also decreased, requiring higher switching frequencies to match low R_{MFC} values.

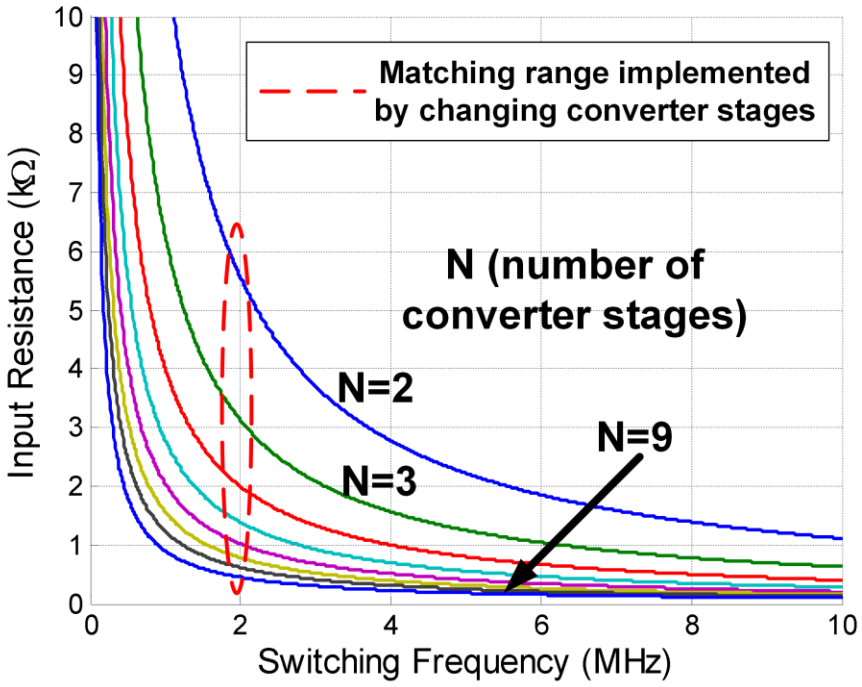

Fig. 106. Input resistance variation for inductorless DC-DC converter.

From (90) the input resistance is inversely proportional to capacitance per stage (C_i) and switching frequency (f_{sw}) as would be expected from a switched capacitor circuit. A value of ~200 pF for each stage capacitance was selected in order to maintain switching frequency to a minimum range allowing for system-wide low power consumption. The main tradeoff with this approach is area cost due to the capacitance density offered by the process used (4.1 fF/μm^2 in 0.18 μm CMOS process) and the high switching frequency required for high power MFCs (low R_{MFC} values).

Previous efforts [42] implementing stage addition/subtraction as the main mechanism for maximum power extraction show a limited range over which matching

can be performed when compared to the wider matching range offered by sweeping the switching frequency and stage management offered by the proposed solution. Fig. 3 highlights the flexibility offered by the EA-PMU compared to the approach proposed by [42].

For maximum power transfer to occur, the I-DCDC's input resistance must equal R_{MFC}. Once the input voltage of the converter equals to half of the MFC's open circuit voltage, the maximum power transfer [120] condition occurs. Since MPP is achieved through a control loop dependent on input impedance, stability issues are vital to the correct operation of the system once reconnection between MFCs occurs. Switching between different MFCs will cause impedance variations at V_{in} of the I-DCDC, requiring the system to modulate its input resistance to correctly achieve MPP. Fig. 107 shows the small-signal model of the MPPT system. With each reconnection of an MFC, a new impedance profile is presented to the PMU, requiring quick and accurate matching

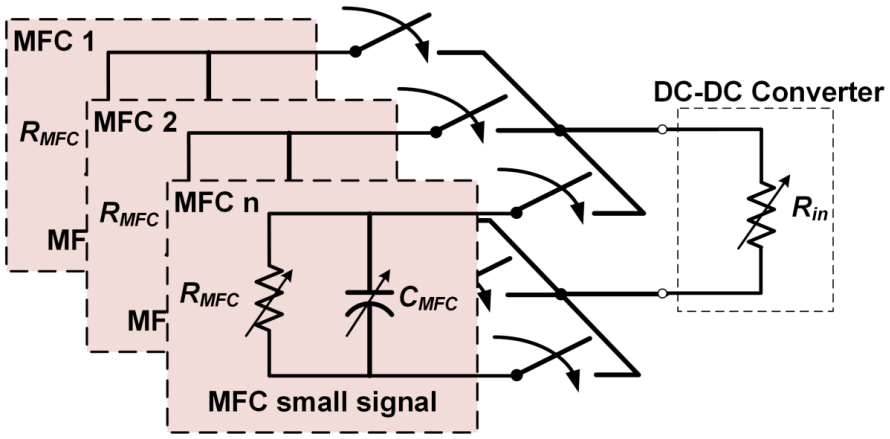

Fig. 107. Small-signal equivalent MFC source impedance for control-to-input transfer function.

within as short amount of time as possible. The proposed PMU is unique in this aspect, since modification of the input source modifies the control loop parameters demanding the PMU's MPPT loop to possess a stable response under all conditions it may face from the MFCs within the array.

I-DCDC stability with reconnection

In order to take frequency behavior into consideration for stability concerns of the MPPT loop, a small-signal model for the switching converter is elaborated. Contrary to the work presented in [112], the switching frequency is inversely proportional to the input resistance of the I-DCDC converter, nor is there an associated internal parasitic capacitance found in TEG sources. State-space averaging following [60] was performed to obtain the control-to-input (C-to-I) transfer function, where individual variables for the on and off (T_{on} and T_{off}) time for a switching converter are implemented. Through analysis, the C-to-I transfer function for the converter yields:

$$\frac{V_{in}(s)}{V_c(s)} = \frac{G_{do}}{s+\omega_p} K_{cco}$$

$$\approx \frac{\frac{T_{on}}{R_{on}\, C_{MFC}}\left(\mathrm{V_{out,DC}} - (N+1)\mathrm{V_{in,DC}}\right)}{s + \left(\frac{1}{R_{MFC}\, C_{MFC}} + \frac{\left((N+1)T_{on}F_{sw}\right)}{R_{on}\, C_{MFC}}\right)} K_{cco} \tag{93}$$

$$\omega_p \approx \frac{R_{on} + R_{MFC}((N+1)\cdot T_{on}F_{sw})}{C_{MFC}\cdot R_{MFC}R_{on}} \tag{94}$$

where N, K_{cco}, R_{par}, and C_{MFC} are the number of stages in the converter, the oscillator linear gain, the equivalent parallel resistance ($R_{par} = R_{MFC}||R_{on}$) of the MFC's series resistance and switches' on resistance, and parasitic capacitance, respectively. T_{on} and T_{sw} are the on-time duration of a switching period and switching period times, and finally, $V_{in,DC}$ and $V_{out,DC}$ from (92) are the steady-state DC voltages at the input and output of the converter and are obtained from the state-space DC averaging (see Appendix). Equation (93) shows the pole location given by the C_{MFC} value and resistances R_{MFC} and R_{on}. Equation (92) behaves as a single pole system below the switching frequency of the converter. From here, it is clear to see that the pole is dominated mainly by the MFC parasitic electrical equivalents, which vary over a large range (TABLE 11). Fig. 108 shows both simulated and analytical expressions in good agreement between obtained transfer function and its simulated performance.

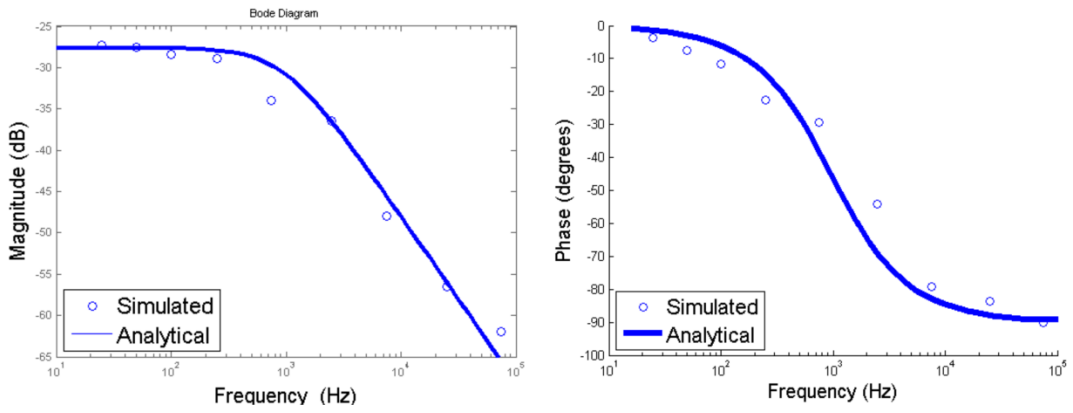

Fig. 108. Control-to-input simulated and analytical comparison.

The small signal equivalent model for the MPPT loop (Fig. 105) is shown in Fig. 109, where the open loop transfer function, $T_{ol}(s)$, is given by:

$$T_{ol}(s) = B(s)\, K_p\, K_{cp}\, F(s) \tag{95}$$

where K_p, K_{cp}, $F(s)$, and $B(s)$ are the comparator gain, current steering charge pump gain, filter transfer function, and the C-to-I transfer function of the converter. As was the case in [112], loop performance can be enhanced through the implementation of a filter block, $F(s)$.

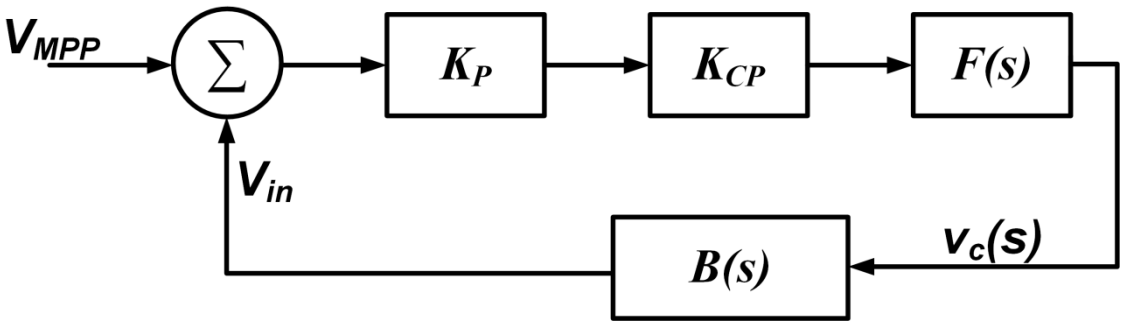

Fig. 109. Small-signal stability model for PMU MPPT scheme.

The open loop transfer function without considering an optimized filter ($F(s)$ implemented with a 10 nF capacitor), with K_{cp} of 100 nA quiescent current and K_p of 100 dB provides a gain bandwidth product (GBP) of 9 kHz and 718 Hz, with phase margin values of 2.36° and 0° for the high-power (MFC-H) and low-power MFC (MFC-L) electrical circuit equivalents, respectively.

By implementing F(s) as a Type-II filter [54] an improvement in phase margin and GBP is performed. GBP is increased to 74 kHz and 47° phase margin for MFC-H (MFC-HOpt), and for MFC-L, the GBP and phase margin are 150 Hz with 87° of improvement (MFC-LOpt).

The main limitation for loop dynamics fall directly on the state of the MFC cells, as lower power production translates to higher parasitic internal elements (R_{MFC} and C_{MFC}). Previous works [112] implementing dynamic MPPT schemes for large ranges of varying source resistances did not consider stability issues in both parasitic components or in their analysis. This issue has the potential of de-stabilizing the frequency response of the MPPT loop. To the best of the authors' knowledge, this is the first presented work which considers the input source's power production state into the control dynamics. Section IV-B describes the realization of the MPPT control loop in more detail.

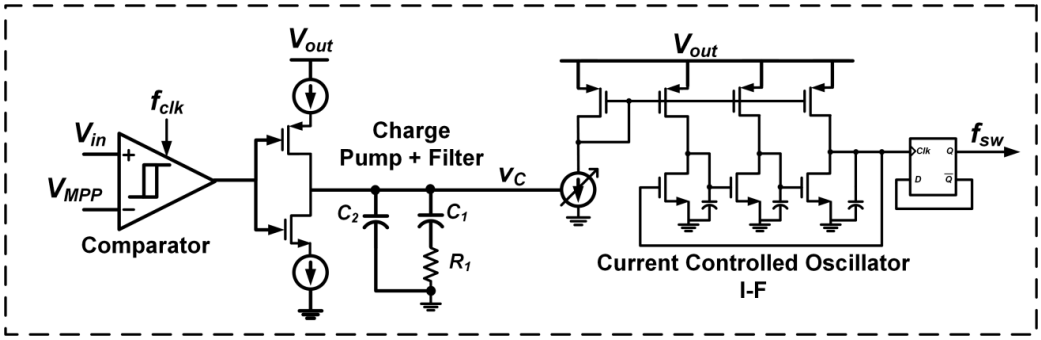

Fig. 110. Implemented MPPT scheme through frequency modulation scheme.

I-DCDC implemented circuit blocks

The MPPT building block, indicated in Fig. 105, is shown in detail in Fig. 110. Among the main contributions of the proposed approach differing from [112] are the MFC MPP acquisition (V_{MFC} /2) through a precharging scheme, and the higher linearity oscillator which allows for a broader matching range over multiple MFC power profiles. These features make the presented solution ideal for low-power time-varying energy harvesting sources.

Maximum power point and comparator blocks

The MPP acquisition, performed by the capacitive divider block (Fig. 105), can be performed by two separate means: through a precharging scheme, which consisted of taking the output voltage and using a dynamic resistive divider network; or by the open circuit voltage method [19]; thus, the MPP can be obtained. Fig. 111 shows the manner in which both the precharging scheme, and open circuit voltage method are performed.

The precharging scheme is required due to the large parasitic components associated with the MFC (R_{MFC} and C_{MFC}). Applying the same approach as [112] would produce an incorrect MPP due to the amount of time required for the MFC to reach nominal open circuit voltage (OCV) during a single sampling period. However, when

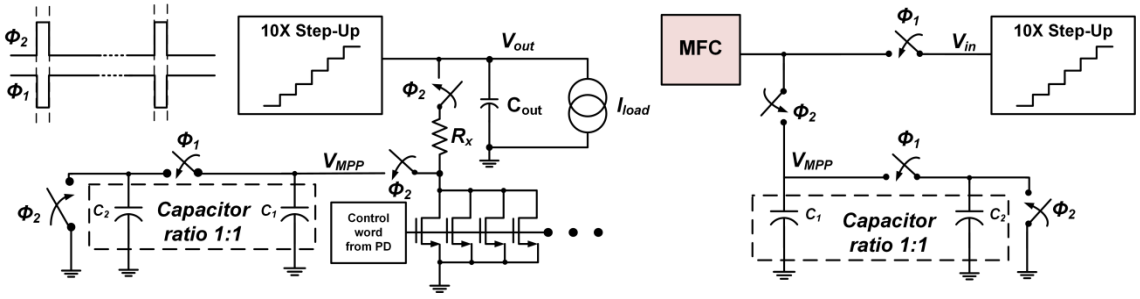

Fig. 111. Capacitive divider for MPP acquisition from output voltage (left) and directly from input voltage (right).

small values of associated parasitics can be obtained from the MFC, the open circuit voltage method can be used and allows for a stand-alone solution to obtain MPP for the MFC devices.

For the precharging scheme the output voltage is quickly sampled through a pair of switches controlled by nonoverlapping clock phases ϕ_1 and ϕ_2. The resistive divider is composed of resistor R_x and a variable resistor implemented with multiple NMOS devices in parallel. The PD algorithm selectively turns on the required number of NMOS devices in order to correctly achieve nominal OCV from the selected MFC.

A lookup table, within the PD algorithm controller, would allow the correct setting of the required division factor and would give the operator an opportunity to sample this value to C_1 during phase ϕ_2. Afterwards the stored charge in C_1 would be divided between C_1 and C_2 to achieve the required MPP.

The open circuit voltage method briefly disconnects the MFC from the I-DCDC converter to sample the open circuit voltage during ϕ_2, where capacitor C_1 stores the open circuit voltage of the MFC (V_{MFC}). During ϕ_1, the MFC is reconnected to

converter, while the charge stored in C_1 is again divided between both C_1 and C_2, to achieve MPP.

Both methods can achieve accurate MPP for MFC, but the open circuit voltage method is limited in the time constant value of the MFC's R_{MFC} and C_{MFC} for it to reach nominal V_{MFC}.

If the time constant is restrictively large, the capacitive divider would need to disconnect the MFC from the I-DCDC converter for prohibitively large periods of time, making it unsuitable for power harvesting from the MFC.

Once the MPP acquisition is completed, a comparator evaluates differences between the desired reference and the input voltage for the CP (V_{in}). As the compared voltages are DC values and V_{in} varies at a slower than a single comparator clock period, the behavior can be approximated as continuous. The comparator topology implemented [96] operates with a dedicated clock tuned at 100 kHz and characterized with a gain of 100 dB.

Charge pump and filter

The charge pump employed was that of a conventional current steering design with a static current consumption of 100 nA. For the filter, a Type-II filter topology commonly used in Phase-Locked Loops was realized due to the low power nature of the system. The optimization of the control loop was mainly focused on improving performance for the worst case MFC-L: R_{MFC} of 8 kΩ and C_{MFC} of 2.5 mF.

In order to improve phase margin under the already limited system parameters offered by MFC-L, the zero frequency was placed at low frequencies, i.e., ~8 Hz. The secondary pole, ω_{p2}, was placed considering stability for the best case MFC (MFC-H). Since GBP is much better than MFC-L, the only limitation was adequate phase margin.

The pole was positioned at ~80 kHz and improved both GBP and PM to 73.6 kHz and 45.7°, respectively. Values for the filter implemented were: R_1= 20 kΩ, C_1 = 1 μF, and C_2= 10 pF; the filter was implemented with external components.

Current controlled oscillator

The current controlled oscillator (CCO) implemented for the MPPT scheme was a wide tuning range and a three-stage ring oscillator topology [147]. The tuning range was selected by the required frequency range for the SC input resistance (Fig. 106). The implemented topology of the CCO offered a much broader linear range and only one control voltage (V_c) compared to the approach presented in [112], where control voltage for both PMOS and NMOS in the transmission gate resistance had be considered. The implemented CCO was designed for a linear tuning range (see (90)) from 10 kHz to 10 MHz with a gain of 10 MHz/V (K_{cco}) in order to cover the required values of f_{sw} for impedance matching purposes.

10X step-up charge pump

Fig. 112 shows the DC-DC converter topology, where by monitoring the output voltage the number of stages varies on load conditions. The implemented step-up converter was composed of a 9-stage, 10X gain, 4-phase Dickson Charge Pump [57];

responsible for stepping up the MFC voltage to usable CMOS levels. This topology was selected due to its inherent higher efficiency for lower power profiles [148, 149].

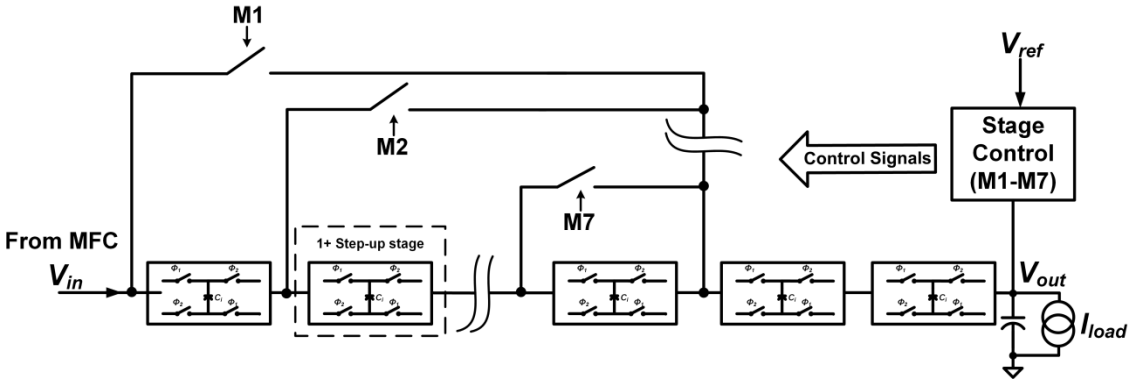

Fig. 112. 10X charge pump topology.

The switch design implemented a bootstrapped approach in order to minimize R_{on} values throughout the entire converter. Fig. 113 shows the implemented technique where each stage is activated via the M_x control bit. Both Φ_A and Φ_B were delivered from a 4-phase nonoverlapping clock generator; previous and next stage block used the remaining two phases for their own clock control. The bootstrapping effect through phase ϕ_A precharges the capacitor C_{bt} to the voltage at the V_s node, then during ϕ_B and additional potential is added to the bottom plate of C_{bt} of approximately V_{out}. This allows for the overall overdrive voltage across the switching transistors to remain constant throughout the entire step-up chain.

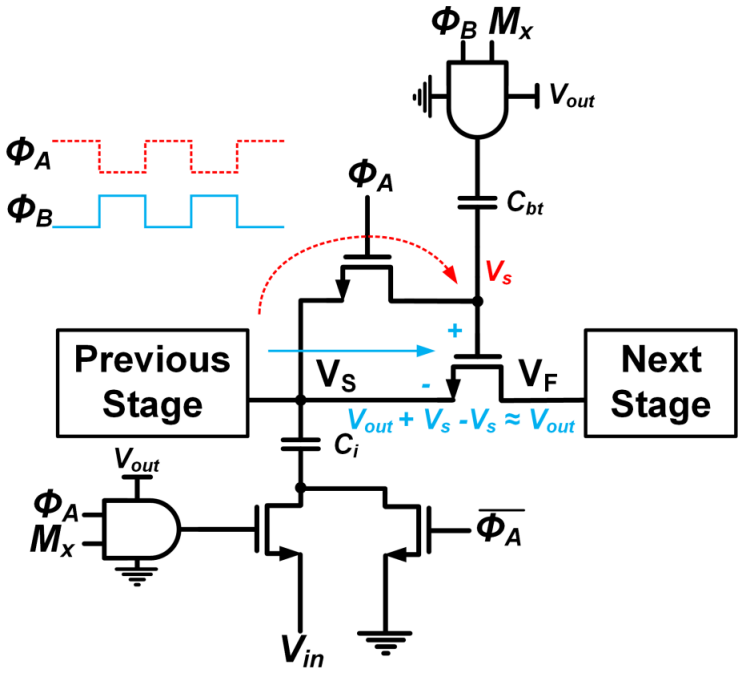

Fig. 113. Bootstrap technique for CP stage.

As shown in Fig. 105, the output voltage was continuously monitored by a clocked comparator in charge of reducing the number of stages in the step-up converter if the output voltage exceeded the required reference (M1-M7) (Fig. 114). As the output voltage exceeded the external reference, stages are bypassed until the output voltage falls below the reference voltage.

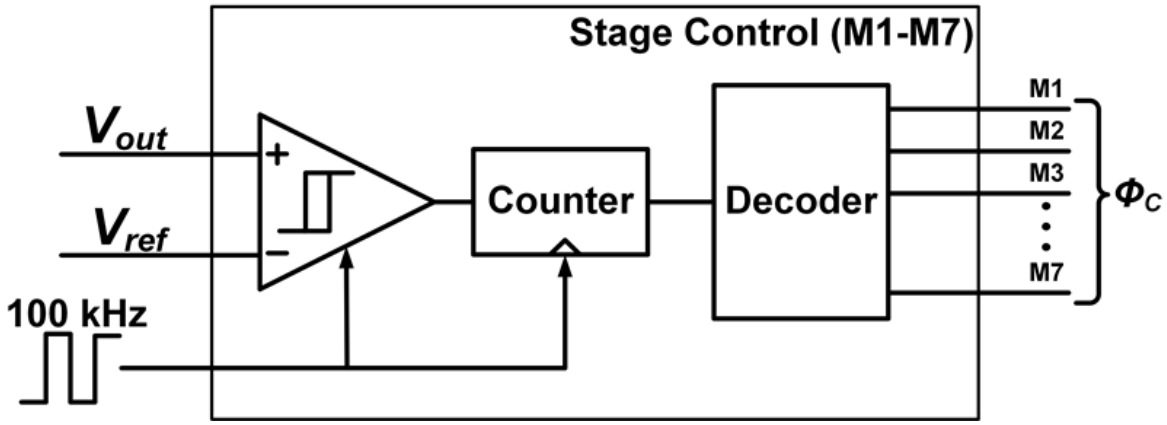

Fig. 114. Stage control block for output voltage monitoring.

Fig. 114 shows the overall structure of the Stage Control block. Only two stages are permanently set in the power path due to the maximum voltage delivered by the MFC, which is characterized to be 800 mV. If all programmable stages are bypassed and the output voltage still exceeds the external voltage reference, the main oscillator clock is disengaged, but maintains a secondary oscillator to drive both the MPP acquisition block and Stage Control blocks (output and input comparators) of the PMU. The main oscillator clock is re-engaged once the output voltage falls below the reference. By extracting MPP during all operational up-time, regulation can be achieved as long as the load does not demand more power than what is available at the input source; this is the main limitation in all energy harvesting systems. Current demands within the system's capabilities will maintain the converter operating at MPP through the MPPT scheme, sustaining the required output voltage.

I-DCDC system startup

The voltage delivered by the MFC does not allow for a self-starting operation from the converter. An external one-time precharging of the output capacitor to 600 mV is required to begin controller operation. Multiple different approaches may be taken to start up the system [88, 124].

Once the system begins extracting energy from the MFC, there is no longer a need for an external power source to power the I-DCDC.

Measurement results

The PMU system was fabricated in 0.18 μm CMOS process with an active area of 1.8 mm^2. Fig. 115 shows the die microphotograph of the PMU with the value for output capacitor, C_{out}, being 100 mF.

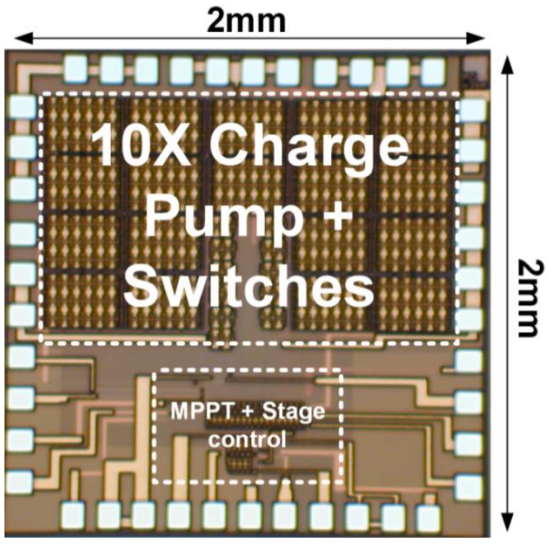

Fig. 115. Die microphotograph of implemented I-DCDC and test bench.

For the MFCs, Fig. 116 shows the polarization curves for the 240 mL (MFC-L) device obtained after eight months of operation, showing a maximum power output of 11.2 µW at a voltage of 300 mV (open circuit voltage of 600 mV). The maximum power from the 1 L (MFC-H) device was 1.6 mW at a voltage of 400 mV (open circuit voltage of 800 mV) (Fig. 14). This is in line with a typical two-chamber MFC power performance when using wastewater inoculum and acetate as the carbon substrate. These two MFCs were used to test how the developed I-DCDC performs at two different MFC voltage and power levels.

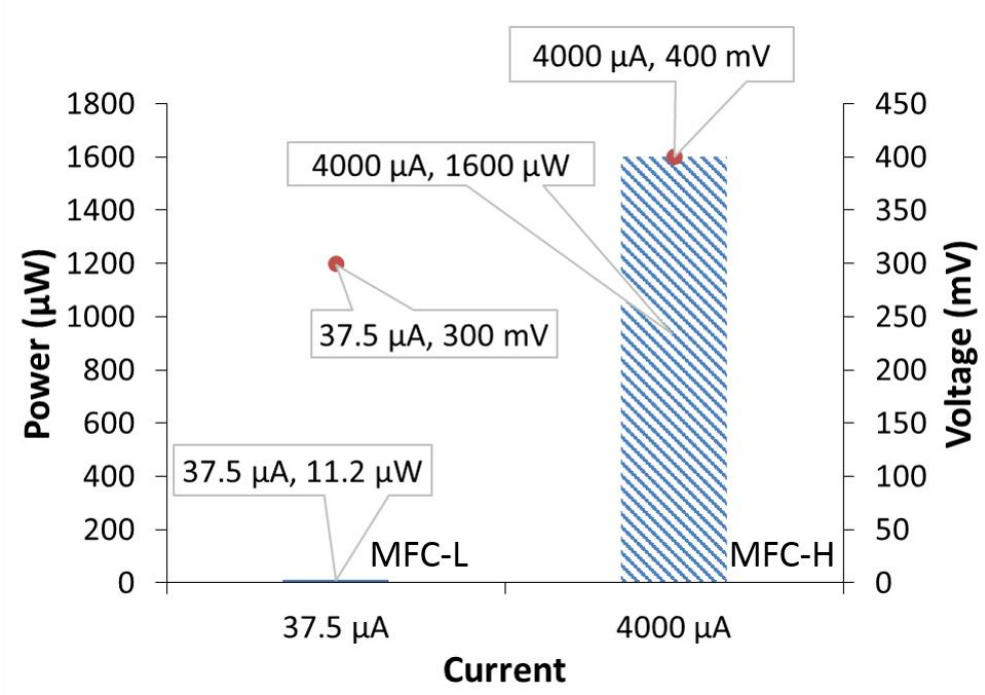

Fig. 116. Power production of MFC-L (low power) and MFC-H (high power).

Maximum power point tracking

Fig. 117 shows correct MPPT extracted through the PMU by performing rapid changes between the best and worst case condition MFC sources; both conditions modified the operating point for MPPT ($V_{MFC}/2$) as well as the pole location (ω_p) for the control loop. The change between MFCs was performed to simulate the effect of the PD algorithm when selecting within the MFC array between 'best' and 'worst' conditions. The aforementioned variables were correctly dealt with by the PMU. As it was calculated in section titled I-DCDC Implemented Circuit Blocks-Maximum Power Point and Comparator Blocks, the GBP and PM for both cases was so drastically different that settling time between MFC-H and MFC-L varied between ~100 ms for MFC-H and ~3 s for MFC-L.

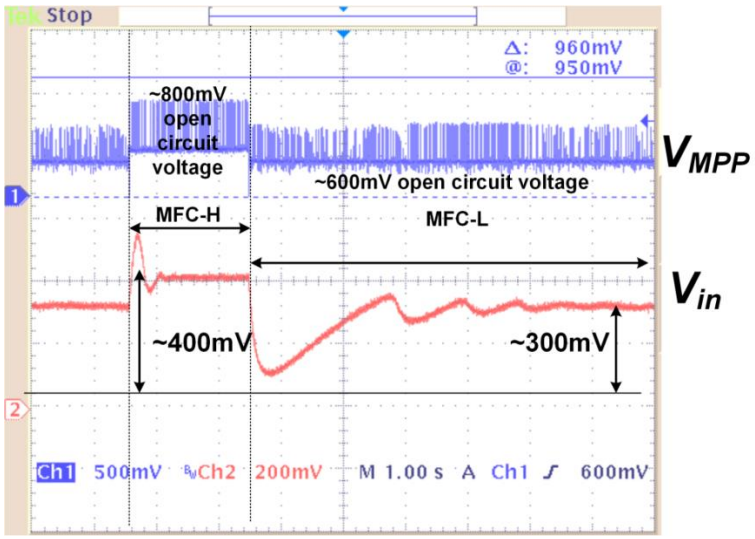

Fig. 117. The MPPT control loop correctly identifying MPP for extreme condition MFC-H and MFC-L.

Voltage regulation

Fig. 118 shows output voltage regulation capabilities for the converter for 1.6 mW of input power and load current step from 100 µA to 400 µA and back. A 50 mV drop at the output voltage is seen at V_{out} as well as a 150 mV overshoot when load is stepped down from 400 µA to 100 µA. The system is able to maintain regulation by maintaining MPP throughout varying load current demands (extracting maximum power from the source at all times). Whenever load current exceeds the input available power, regulation cannot be maintained and the output voltage will drop.

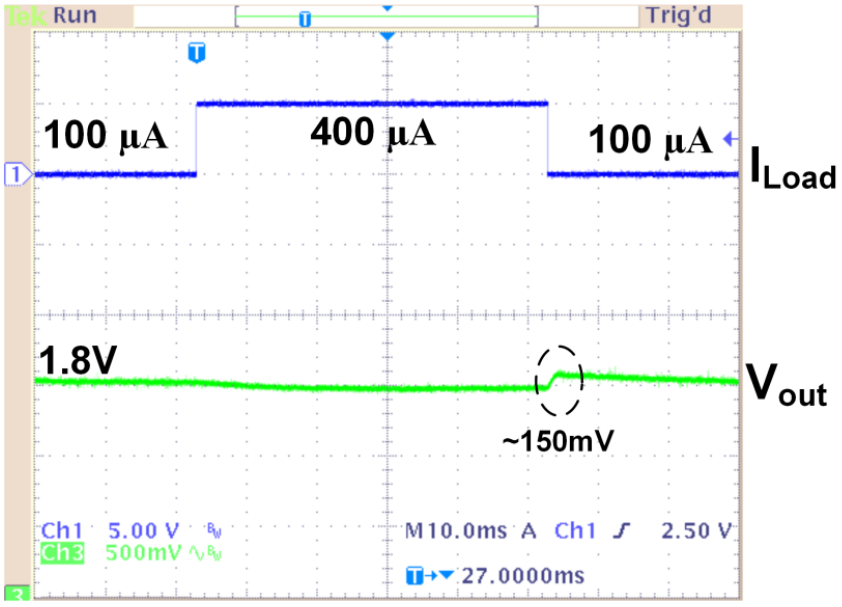

Fig. 118. Output voltage load regulation test with load current variation for 1.6 mW of input power.

Efficiency measurement

Fig. 119 shows the measured efficiency of the system when operating at the full 10X gain. Measurements were performed using V_{out} as the internal control supply, with the exception of the current steering charge pump bias in the MPPT control loop. Maximum efficiency from MFC-L was measured to be at 46% for an output power of 3.6 µW and for MFC-H maximum efficiency of 65 % for 1 mW output power. TABLE 12 summarizes the performance of the EA-PMU and compares with previously reported state-of-the-art works.

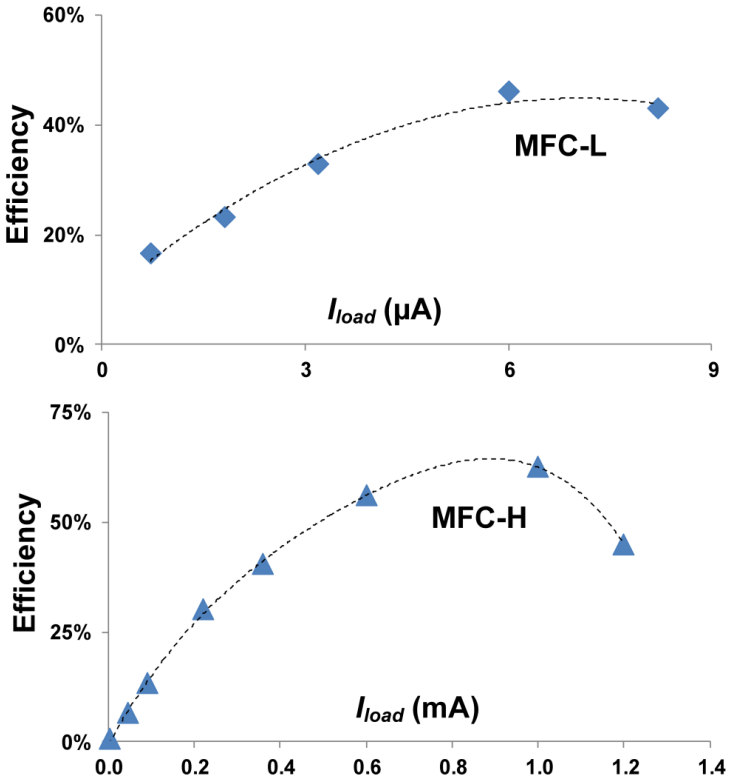

Fig. 119. Efficiency measurements for CP with variable loads.

Results from [42] show a higher efficiency due to lower number of stages in the charge pump being used. The presented system is the only fully integrated PMU capable of achieving both a broad range of matching and improved efficiency for energy harvesting solutions operating below 1 V input voltage. Power consumption for the proposed I-DCDC converter totals approximately 4.7 μW between static and dynamic power consumed. It should be noted that higher power consumption was derived from the increased number of stages of the I-DCDC.

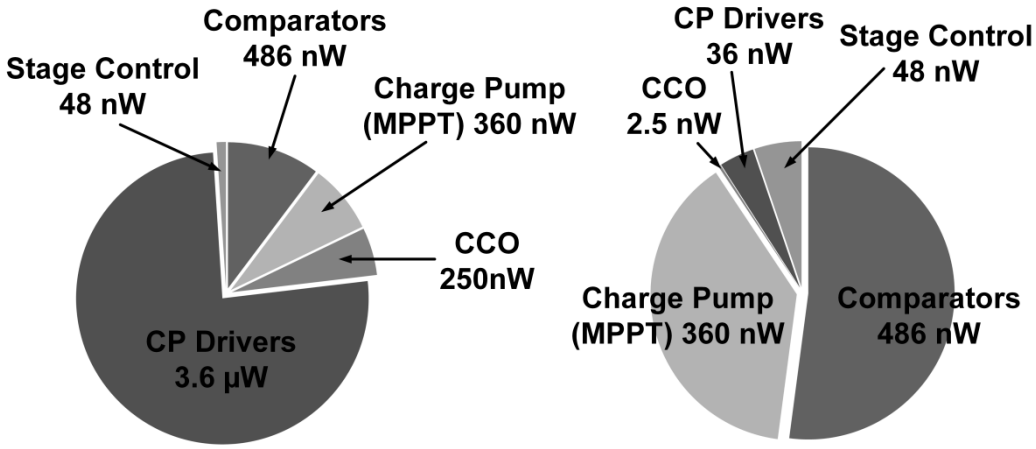

Fig. 120. Power consumption for I-DCDC @ 1 MHz f_{sw} (left) and 10 kHz f_{sw} (right).

Fig. 120 breaks down the power consumed by dynamic and quiescent for 1 MHz f_{sw}. Power consumption will automatically set depending on the power availability at the input MFC source. With high MFC power profiles, the I-DCDC will require higher f_{sw} to achieve MPP, i.e., at 5 MHz the power consumption is 20 μW, but the power extracted from the MFC was much higher.

TABLE 12. Summary of performance for MFC power management units.

SPECIFICATION	[150]	[42]	[104]	[136]	[102]	[151]	THIS WORK
Input Voltage Range	350 mV–480 mV	1V–5 V	315 mV	320 mV	~ 0.66 V	> 0.6 V	300 mV-400 mV @ MPP
Output Voltage	1.4 V	2 V	~ 1.1 V	5 V	1.8 V Charge pump 3.3 V Boost converter	0.9 V–1.2 V	1.6 V–2 V
Power Consumption	2.62 µW ‡	2.11 µW @ 60 kHz f_{sw}	NA	NA	NA	1 µW @ 1 MHz f_{sw}	933 nW @ 10 kHz f_{sw} 36.4 µW @ 10 MHz f_{sw}
MPPT	No	Yes	Yes	Yes	No	No	Yes
Impedance Matching Range	-	100 kΩ	NA	NA	-	-	100 Ω–8 kΩ *(6.5 µF–2.5mF)*
Input Source	Photovoltaic or Thermoelectric generator (TEG)	TEG	MFC	MFC	MFC	MFC	MFC or TEG
Max. Efficiency	65%	58%	~ 90 % at 0.7 V output voltage	45.21%	21.6%	85% at 0.9 V output voltage	64.88% with MFC-HIGH at 1.8 V output voltage
Topology	Charge Pump	Charge Pump	Boost Converter	Boost Converter	Charge Pump and Boost Converter	Boost Converter	Charge Pump
Technology	0.13 µm	0.35 µm	Discrete	Discrete	Discrete	0.18 µm	0.18 µm

‡f_{sw} for this power not reported

Conclusions

This chapter presents a fully integrated, I-DCDC converter for an EA-PMU aimed at managing power of MFC arrays, through a time multiplexing harvesting approach in order to overcome the voltage reversal issue in MFC arrays power harvesting. MPPT and efficient DC step-up gain were performed through a FMS and dynamic stage selection. It also showcases a novel MPPT design procedure, for capacitive DC-DC converters and the stability considerations to be taken to achieve MPP. The converter can achieve MPPT for a broad range of MFC power profiles, ranging from 7.8 µW ($R_{MFC} = 8k\Omega$) to 1.6 mW ($R_{MFC} = 100\ \Omega$) as well as taking into account parasitic capacitances from the MFCs (6 µF to 2.5 mF). The maximum measured efficiency was of 65 % for 1.6 mW of input power and a 1 mA load current.

CHAPTER VI

AN AUTONOMOUS FULLY INTEGRATED ENERGY HARVESTING POWER MANAGEMENT UNIT WITH DIGITAL REGULATION FOR IOT APPLICATIONS

Introduction

The research behind novel renewable energy sources has always been a critical and major driving force in technological innovation. One of the breakthroughs in renewable energy technologies has been the development of new and highly efficient power management units (PMU) for energy harvesting (EH) systems. EH-PMUs are focused on two major tasks: 1) Extract maximum power from the source, and 2) provide a regulated output voltage. Major results have been accomplished for solar, kinetic, RF, and thermoelectric sources [124, 152]. Advances in Internet of Things (IoT) devices have allowed for complex and task specific solutions to become the new norm. Complete PMUs are becoming a standard and the same can be seen in energy harvesting [124, 152, 153]. The main challenges behind the design and implementation are the stringent power constraints inherent in EH technology; for which dedicated PMU design must overcome by becoming both low power, and high efficiency.

Providing both maximum power point tracking (MPPT), as well as output voltage regulation is still an issue to be fully resolved. State-of-the-art solutions are capable of performing maximum power point tracking and/or charging capabilities with DC EH sources [154-156].

Nonetheless, delivering a regulated supply to a noise sensitive load (e.g. voltage controlled oscillator) can potentially be an issue for current solutions. The need for a PMU capable of performing both charging function, as well as load regulation, will allow for a new set of functions for PMU with EH sources. These solutions can lead to more robust IoTs and wireless sensor applications where efficiency and power storage are critical for practical employment.

This chapter proposes an ultra-low power, fully integrated, autonomous PMU capable of performing MPPT for dc EH sources, as well as performing both a charging operation and output voltage regulation for noise sensitive blocks. The PMU is comprised of a 10X step up charge pump with two-dimensional articulation for MPPT, and a digital Low Dropout (LDO) regulator with input power sense capabilities. The PMU does not require any additional external biasing or references, and can startup autonomously with a minimum of 350 mV at the input of the converter. The proposed PMU presents a solution for both the maximum power extraction from EH dc sources, as well as offering both storage and regulation capabilities to different types of loads.

The chapter is divided up in the following sections: Section II presents the overall proposed PMU with an overview of the main blocks comprising it, Section III describes the building block implementation of the PMU, and Section IV discusses the obtained measurements from a PMU prototype. Finally, Section V concludes the paper.

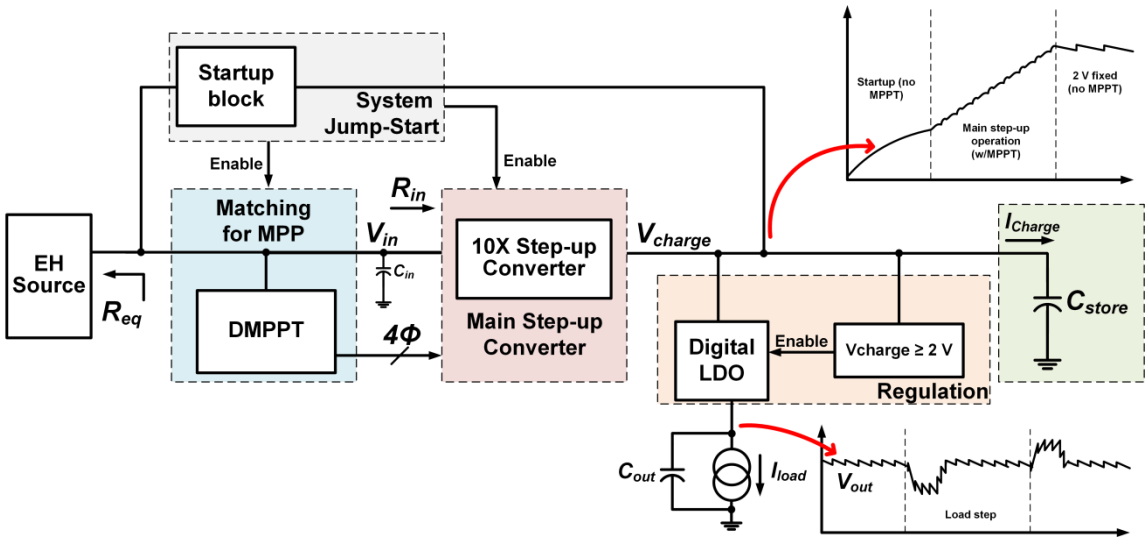

Fig. 121. Proposed block diagram of the power management unit.

Proposed power management unit

Fig. 121 shows the full system proposed for the PMU. The presented system is comprised of 4 main blocks: 1) the startup block (system jump-start), 2) digital MPPT, 3) main converter (charge pump), and 4) the digital LDO. Each block of the PMU requires no external references or external biasing in order for operation of the system. With a fully enclosed operational capability, the proposed PMU can augment battery life of wireless sensor systems; as well as deliver a regulated supply to sensitive systems, e.g. voltage controlled oscillators. The system begins operation by sequentially enabling each block depending on the availability of EH transducer power. A minimum of 350 mV is required to jump-start the system and begin preliminary power extraction through the startup scheme.

A preset delay timer is designed into the startup scheme in order to assure enough power is delivered to the storage capacitor. Once the timer runs out, the main converter is engaged and startup disengaged. The main converter then begins the harvesting operation along with step-up and maximum power extraction process. The main converter steps up the dc EH transducer voltage to 2 V (V_{charge}), allowing for a charging/storage operation at the output of the converter through C_{charge} . Once the 2 V are achieved at the output of the converter, the digital LDO is activated to deliver a regulated output voltage of 1.8 V through a secondary output node, V_{out}.

Startup block

The startup scheme is employed whenever there is no usable stored charge at the V_{charge} node. This would require the converter to begin operation from whatever power the harvesting source can deliver, which can vary significantly over a wide range of values. To circumvent the low voltage nature of the energy harvesting sources used, and enable autonomous operation of the PMU, the startup block shown in Fig. 122 is included to jump-start the PMU to being operation. The startup block is composed of a Dickson-based charge pump with a 3X voltage gain and a dedicated low frequency voltage controlled ring oscillator (VCO), as well as an Enable timer block which enables the main converter + digital LDO blocks while disengaging the startup block.

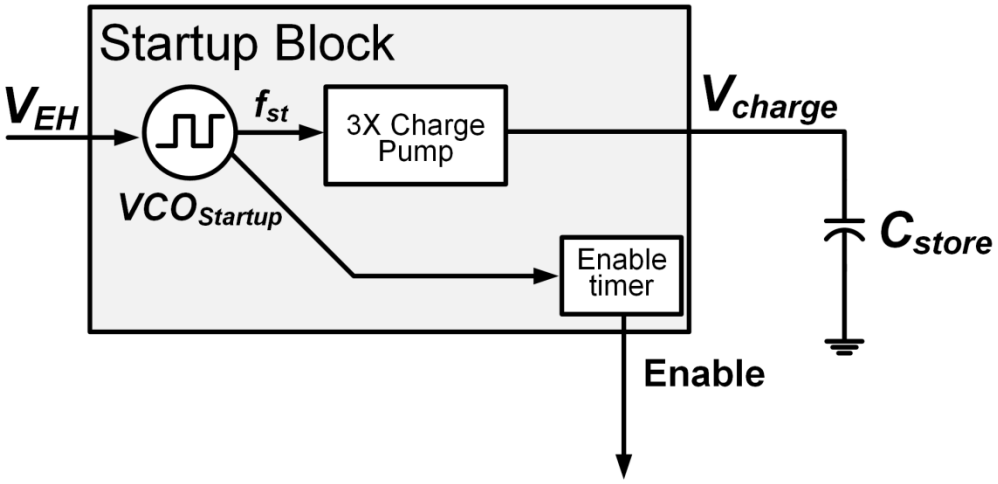

Fig. 122. Startup scheme generating a supply rail for the main converter to begin operation.

Main converter charge pump

Once the hand-off between the startup block and main converter is enabled, the main converter takes over and begins the primary harvesting effort for the PMU. Powered from the V_{charge} node, the main DC-DC converter in the PMU begins maximum power extraction from the EH source. The main converter topology is a 9-stage, step-up converter, based on a Dickson charge pump topology [41]. The converter manages maximum power extraction for the system by implementing a digital maximum power point tracking (DMPPT) scheme via a frequency modulation (FM) through a digitally controlled oscillator (DCO).

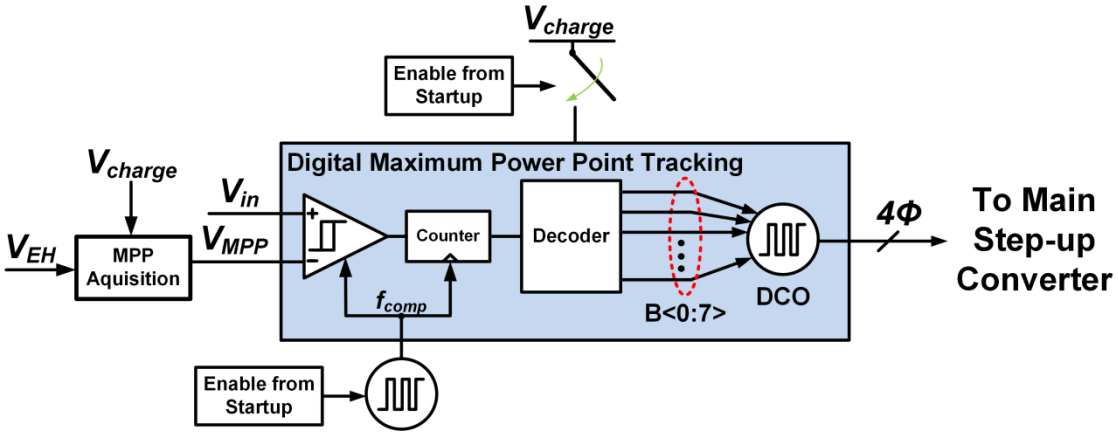

Fig. 123. Digital maximum power point tracking with maximum power point acquisition block for main converter.

The DMPPT, Fig. 123, scheme allows the converter to harvest the highest energy from dc EH sources, by modulating the current being drawn by the PMU to reach maximum power extraction conditions through varying the switching frequency, f_{sw}, of the main converter. The converter also possesses individual control over the 9-stages involved in the step-up process (Fig. 124); this control permits the system to bypass any unnecessary step-up stages to reach the goal voltage. Thus, the two functions of the main converter are summarized as: extract maximum power from the EH source, and to step-up the input voltage from the EH source to 2 V. The main converter has an internal voltage reference powered directly from V_{charge}, permitting the system to operate autonomously. Section III-B and C further describe the system implementation.

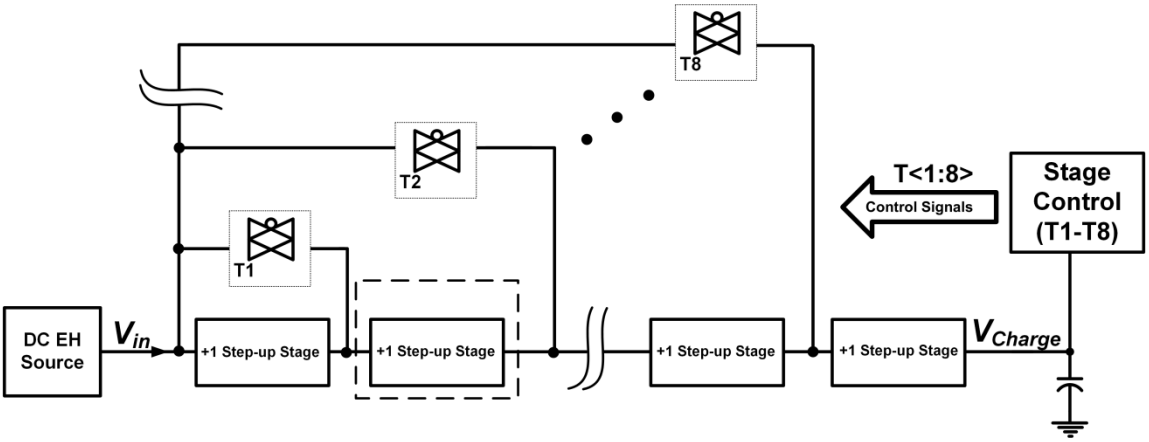

Fig. 124. Main converter (10x) showing bypassing capabilities through stage control block.

Low power digital LDO

Among the chief concerns with power converters focused on EH technology, are the regulation capabilities of a harvesting system. Efforts have been mainly focused on maximum power extraction for storage/charging applications [150, 157, 158], and while there are a few solutions that offer voltage regulation [8, 42, 159], they still require external references and/or external inductors to implement. The proposed approach with the PMU implements the regulation block through a digital LDO, shown in Fig. 125, capable of adapting the pass-device through two main control means: a coarse tuning method that selects the pass-device array to maximize efficiency, and a fine tuning method to regulate the output voltage to the required reference.

The pass-device fragmentation (fine tuning) is a common practice and has shown positive results for sub-micron processes [79, 160], but for EH solutions the variability of the input sources power may limit delivered power to the output load. By utilizing the power density information from the main converter and DMPPT blocks a coarse tuning approach is implemented, which selects a pass-device array from a device bank, according to the available power from the EH source. Three main array banks were implemented which can handle 10s of μWs to 10s of mWs in power range to maximize efficiency by reducing switching losses inherent in larger device geometries. The digital LDO requires no additional external references or biases; it directly draws power from the V_{charge} node for all of the block's needs. This allows for a fully autonomous operation from the digital LDO. The next section describes the design implementation in further detail.

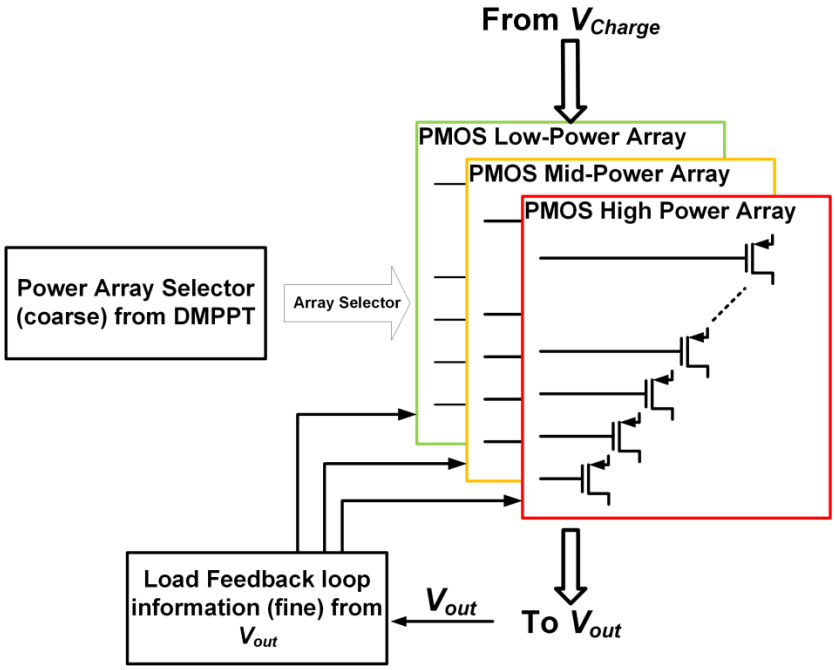

Fig. 125. Digital LDO regulation scheme.

Circuit block implementation

The proposed PMU presents a dc energy harvester with the capability for full autonomous operation. The system has the potential of being deployed along with remote sensor nodes to enhance and extend battery lifetime of the device. The present section elaborates on the PMU block implementations.

Startup block

The startup block enables operation from voltages down to 350 mV, Fig. 126. The entire startup scheme is powered directly from the harvesting source's open circuit voltage, and once the VCO starts, it drives a 4-phase non-overlapping clock for the 3X

charge pump. A dedicated counter sets a time limit on the startup by dividing the VCO startup switching frequency (f_{sw}) by 2^{22} ($f_{sw}/2^{22}$). Operating at 350 mV, the startup VCO delivers a f_{sw} of ~75 kHz, for a roughly 1 minute-long starting-up time. This ensures that the startup build up a high enough voltage for the main DC-DC converter for proper operation. The startup block ends up delivering ~650 mV for the main DC-DC converter, at the V_{charge} node.

Once the main converter begins harvesting energy from the dc source, the startup circuit is disengaged and does not become operational again until the entire system is shut down and reset through complete power deprivation. A set timer of ~ 1 minute was set as variable conditions on EH sources may allow the system to operate under non-optimal conditions, i.e. extreme low power availability. Although the startup block is set to a 1 minute hold period for the PMU to hand-off to the main converter, this can potentially be modified to a lower hold period through bypassing several clock dividers

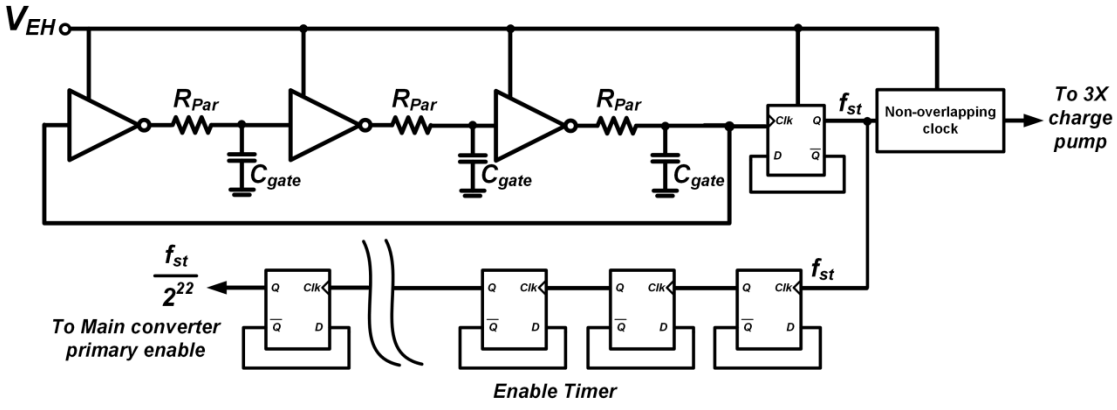

Fig. 126. Startup scheme clock generation and enable timer block.

depending on availability of power from the EH source. Furthermore, since the startup scheme is only operational during initial system settling it is a one-time operational block, and does not negatively impact the overall performance if a steady EH source is present.

Digital maximum power point tracking

In order to extract maximum power from the EH source a MPPT scheme must be set to guarantee this. Depending on the type of EH source, maximum power can be achieved through a resistive matching or/and through power detection algorithms [161, 162]. Both schemes can be implemented in a variety of ways ranging in complexity and power consumption [8, 163, 164]. The DMPPT is implemented to assure the converter extract maximum power, Fig. 123 presents the components comprising the DMPPT: dynamic comparator, up/down counter, decoder, and DCO. Fig. 127 also shows the MPP acquisition block used to obtain the reference for the DMPPT, V_{MPP}.

The overall function of the DMPPT is to drive the V_{in} node to match the V_{MPP} reference by increasing/decreasing the switching frequency of the main converter through the use of the up/down counter and decoder to set the switching frequency of the DCO. The V_{MPP} reference sets the MPP for the EH sources and is divided into 3 different operating modes: for thermoelectric generators (TEG), for solar cells (SC), and for microbial fuel cell (MFC) sources.

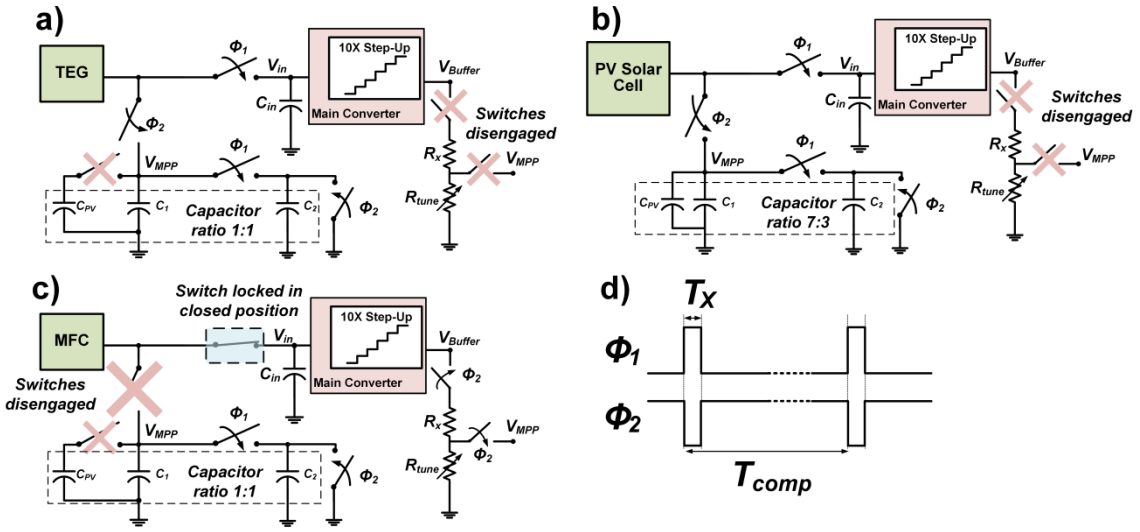

Fig. 127. Maximum power point acquisition scheme for difference dc EH sources a) thermoelectric generators, b) PV solar cells, c) Microbial fuel cells (MFCs), and d) the timing diagrams for both switching phases.

Fig. 127 presents the 3 varying methods with which the V_{MPP} for the needed EH source is achieved. Fig. 127a illustrates the manner in which harvesting efforts with TEGs the DMPPT samples the open circuit voltage and divides it by two using a capacitive voltage divider to set the maximum power point (MPP) condition for the PMU:

$$V_{MPP} = V_{OCV}\left(\frac{R_{TEG}}{R_{TEG}+R_{in}}\right) = \frac{V_{OCV}}{2} \tag{96}$$

Once the V_{MPP} value is correctly obtained, the input voltage of the converter, V_{in}, is driven to match the MPP condition.

For the SCs, an additional capacitor, C_{PV}, is placed next to C_1 (Fig. 127b) to increase the effective value of C_1 and set the maximum power condition to 70-80% of the open circuit voltage (OCV) (V_{MPP} = 70-80% V_{OCV}) [163, 164], approximate MPP condition for SCs. The capacitive divider approach, while not as accurate as other MPP algorithms, is a straightforward implementation and is lower in power consumption. This lends itself for small solar cell dimensions for which the MPP algorithm is accurate (no partial shading conditions). For the MFCs, a biomass power generation systems [165] (Fig. 127c), a resistor ratio is placed on V_{charge} and the value of V_{MPP} is set to OCV divided by two:

$$V_{MPP} = V_{Charge}\left(\frac{R_{Tune}}{R_X + R_{Tune}}\right) = \frac{V_{OCV}}{2} \tag{97}$$

The same method used by the TEG sources would not properly achieve MPP due to the internal parasitic capacitance of the source, requiring long times ($\Phi_2 >> \Phi_1$) of sampling to correctly reach OCV [165] (Fig. 127d), making both sampling capacitors and input capacitor connected at V_{in} prohibitively large. The clock periods shown in Fig. 127d are set by a dedicated oscillator, f_{comp}, free running at ~100 kHz, this sets the sampling times for ϕ_1 and ϕ_2 to $T_{comp}/10$ and T_{comp} respectively. The low frequency sampling of the OCV voltage (~ 1μs), assures that the EH source is only briefly disconnected from the PMU and the sampled OCV voltage value is refreshed in the sampling capacitors.

Once the reference, V_{MPP}, is correctly obtained, the dynamic comparator speeds up or slows down the DCO through an up/down counter with decoded thermometric

output to modulate the input resistance of the main converter to achieve maximum power transfer. The input resistance of the capacitive DC-DC converter is approximated as:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{\alpha\, C_i\, f_{sw}\, N\, R_{charge} + (N+1)\, A_V}{\alpha\, C_i\, f_{sw}\, N\, (N+1)\, A_V} \tag{98}$$

where the variables in α, R_{charge}, N, C_i, f_{sw}, and A_V are the ratio of parasitic capacitance to stage capacitance, charging equivalent resistance (V_{charge}/I_{charge}) seen at C_{charge}, number of stages, capacitance per stage, switching frequency of the converter, and the voltage gain for the charge pump given by:

$$A_V = (N+1) \cdot \left(\frac{1}{1 + \frac{N}{C_i\, f_{sw}\, R_{Load}}} \right) \tag{99}$$

The expression (98) sets the limits for which input resistance can be varied through both number of stages in the converter, voltage gain, and switching frequency. For the main converter design, emphasis was placed on switching frequency as main control method to accurately achieve a wide range of MPPs. The FMS implements a DCO with wide operating range to correctly extract maximum power from most EH sources. The DCO provides rail to rail oscillation and uses a coarse (capacitive) and fine (resistor) tuning schemes to vary switching frequency through a CMOS inverter delay cell configuration, Fig. 128. A digital word of 8 bits (FF in hexadecimal) is used to tune both capacitor and resistor banks to achieve the correct value for f_{sw} at MPP. The capacitor bank unit cell value for C_D is ~2 pF, and the resistor bank unit cell value for

R_D is ~ 10 kΩ. Careful attention is spent on layout efforts to minimize mismatch between resistor and capacitors within their respective bank values.

Fig. 129 the varying switching frequency achieved with different DCO code values in hexadecimal format, XY h, with X values signifying the capacitor bank code, and Y the resistor bank code. The output of the DCO is then sent to the 4-phase non-overlapping clock generator to later transmit to the main converter switches.

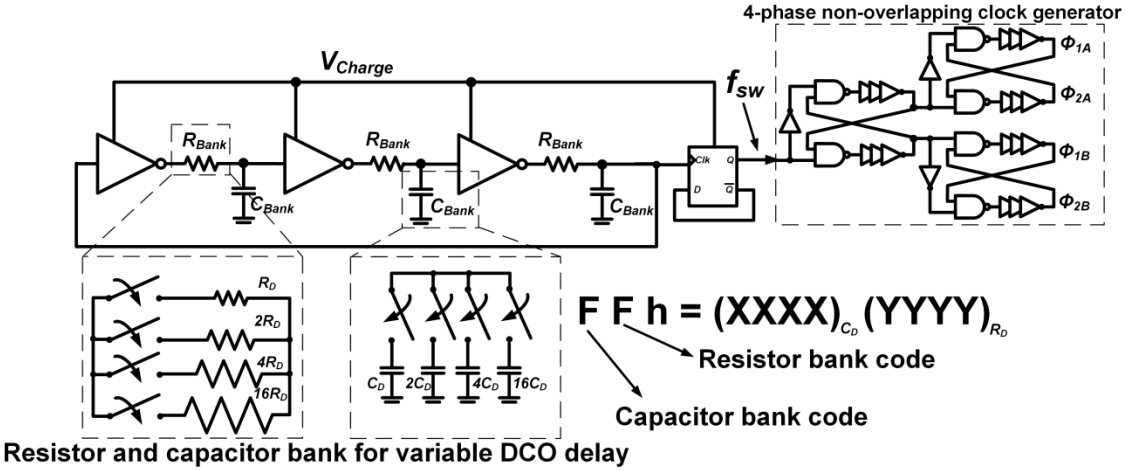

Fig. 128. Digital controlled oscillator implementation for DMPPT.

With the varying frequency and variable number of stages of the main converter, the input resistance, R_{in}, of the PMU can effectively be adapted to achieve the required input voltage condition (V_{in}) to meet MPP ($V_{in} = V_{MPP}$). Fig. 130a shows the range over which the R_{in} of the PMU is tuned over switching frequency and charge pump number of stages to meet the MPP condition.

Notice how R_{in} is inversely proportional to high values of f_{sw} and number of stages. This sets the limit over which the MPP condition can be met by the PMU; for high values of dc gain from the PMU (low input voltage EH source) more stages will be required to achieve the goal output voltage of 2 V, limiting the resistance range over which MPP can be met.

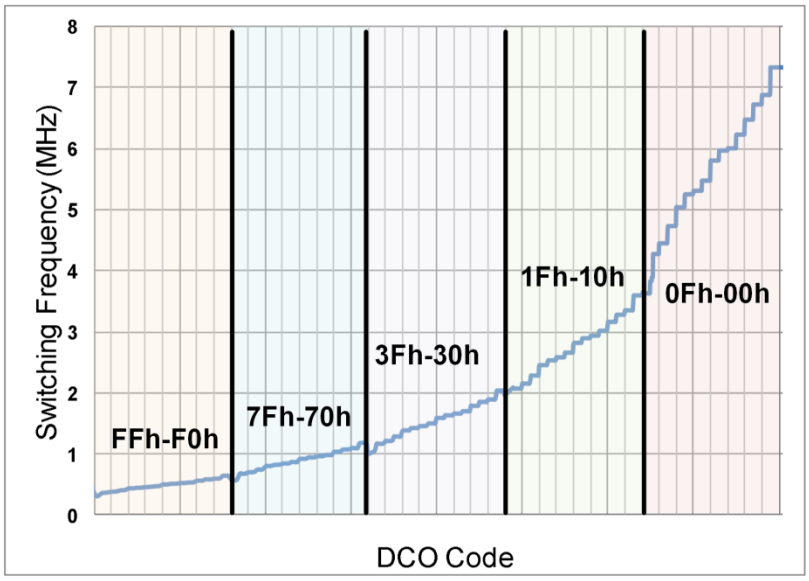

Fig. 129. Digitally controlled oscillator frequency range and code word in hexadecimal format.

For lower values of dc gain (high input voltage EH source), the number of stages can be decreased and the range over which the R_{in} of the PMU can change increases at the cost of higher valued f_{sw} to meet lower resistance values. A second variable to consider is the output voltage value, V_{charge}, Fig. 130b shows how output voltage values also affect R_{in}. Differences between 1 stage and 9 stage implementations show the

limitation of values for R_{in} for which the PMU can achieve. All three variables, f_{sw}, output voltage, and number of stages, must be considered when designing a MPPT scheme for a charge pump, these variables are the inherent limitation on the topology over which R_{in} values can be accomplished.

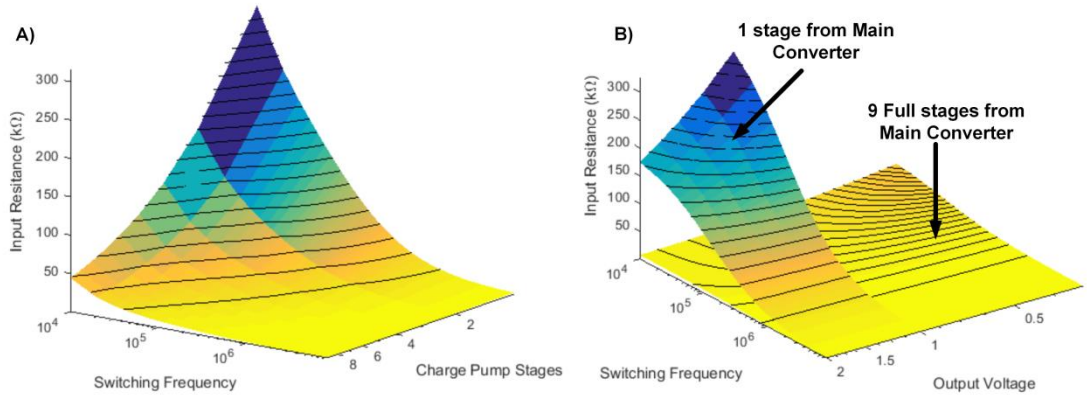

Fig. 130. Input resistance range capabilities for proposed PMU with a) varying charge pumps stages v. f_{sw} and b) varying output voltages v. f_{sw}.

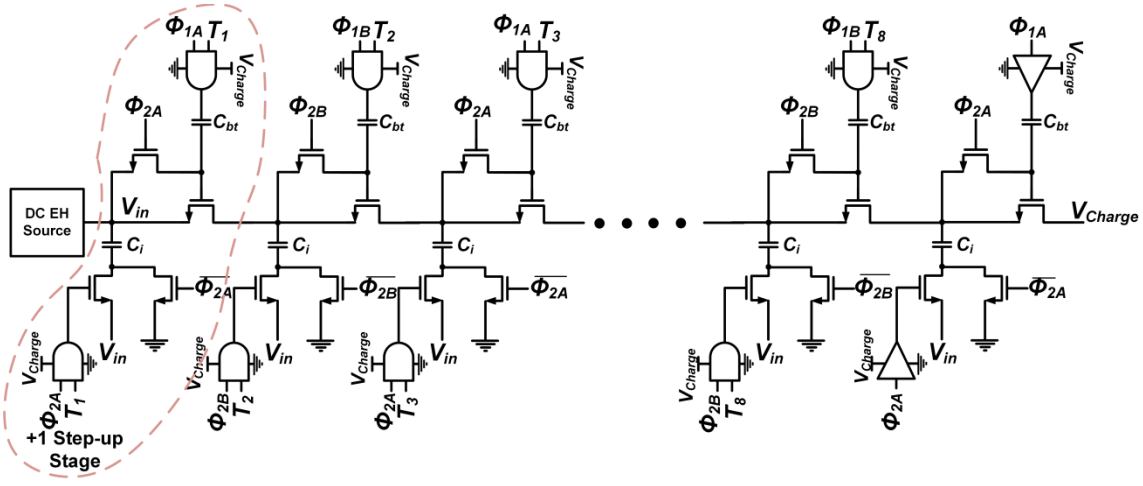

Fig. 131. Full schematic of 10X main converter with variable stage selection.

Main converter charge pump

The main converter charge pump is comprised of 9 step-up stages to achieve the required output voltage at the output of the converter. The number of stages are not fixed and allow for increasing/decreasing depending on the voltage delivered by the EH source. Fig. 131 shows the full schematic of the step-up main converter. Each individual stage, +1 Step-up Stage, receives both its clock signals from the DCO and stage enabling/disabling signals from the Stage Control block.

The switch design implemented a bootstrapped approach in order to minimize R_{on} values throughout the entire converter, where each stage is activated via the T_{1-8} control bits. Both $\phi_{1A,B}$ and $\phi_{2A,B}$ (Fig. 131) are delivered from the 4-phase non-overlapping clock generator. The bootstrapping effect through phase $\phi_{2A,B}$ precharges the capacitor C_{bt} to the voltage stored in capacitors C_i, then during $\phi_{1A,B}$ and additional potential is added to the bottom plate of C_{bt} of approximately V_{charge}. This allows for the overdrive voltage across the switching transistors to remain constant throughout the entire step-up chain.

As mentioned previously, the main converter has a variable stage control in order to reduce the number of stages T_{1-8} when high enough voltage is available from the harvesting sources. Stages can potentially be reduced to a minimum of one when the input voltage provided from the EH source is 1V. The Stage Control block is shown in Fig. 132 comprised of a CMOS reference, capacitive divider, comparator, counter, and decoder. The reference implemented is a CMOS subthreshold reference [166], powered directly from V_{Charge} node delivering a voltage of approximately 200 mV with a power

consumption of ~7 μWs for 2 V at the V_{charge} node. The capacitive divider performs a series-parallel step-down operation, with the same clock phases used in the MPP acquisition block, to obtain the $V_{Div/10}$ voltage ($V_{Div/10} = V_{charge}/10$); this voltage is used in the Stage Control loop to add or reduce stages in the main converter by triggering the comparator high or low, thus increasing or reducing the up/down counter. The counter output is then sent to the decoder block, which performs the enabling/disabling operation of the main converter (Fig. 124).

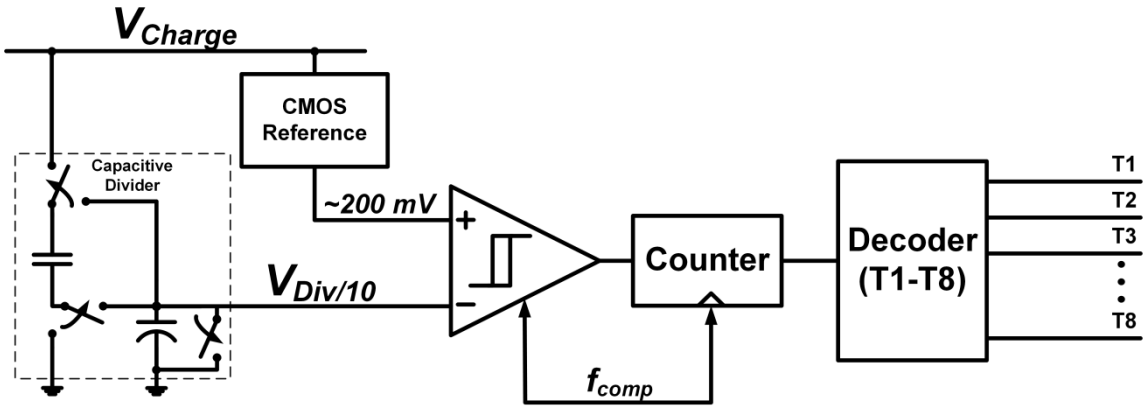

Fig. 132. Stage control block with low power reference schematic.

With each additional stage added to the main converter, efficiency decays. So the addition of more stages to the main converter comes at a price on overall system efficiency. From [167] the efficiency expression (5) shows the relationship between number of stages (*N*), switching frequency, (f_{sw}), ideal voltage gain ($A_{Ideal} = N + 1$), and ratio of stage and parasitic capacitances (α):

$$\eta = \frac{A_V}{(A_{Ideal}) + \alpha \frac{N^2}{(A_{Ideal}) - A_V}} \tag{100}$$

From (100) each additional stage increase (*N*), increases the value of the second term in the denominator and reduces the overall efficiency of the system. As stated in [42], efficiency limitations on capacitive DC-DC converter are heavily driven by α ratio inherent in the process. This shows the intrinsic limitations with any capacitive DC-DC converter and viability of implementation with each process.

Digital low dropout regulator

Regulation is among the key building block for any system which requires a regulated supply voltage to supply noise-sensitive blocks [168]. The implemented digital LDO allows for a regulated output voltage through an energy aware scheme which emphasizes overall efficiency by minimizing switching losses in the switched pass device. As previously mentioned in Section II, there are two main variables that allow for efficient regulation in the PMU: the power array selector loop, and the load feedback loop information.

Since with any EH system power is limited to what is available from the source, so having a one-size fits all solution can limit the range of applications over which the system can be applied to. The implemented digital LDO takes power level information from the DMPPT block and Stage Control Block, Fig. 133, and selects the best suited PMOS pass device to deal with load demand, while minimizing power consumption required in driving the device.

The load feedback loop performs the required fine tuning of the pass device once the best suited array is selected. Each array is broken up into multiple individually driven pass devices which comprise the equivalent full pass device. It is this load feedback loop which performs the required control for load regulation.

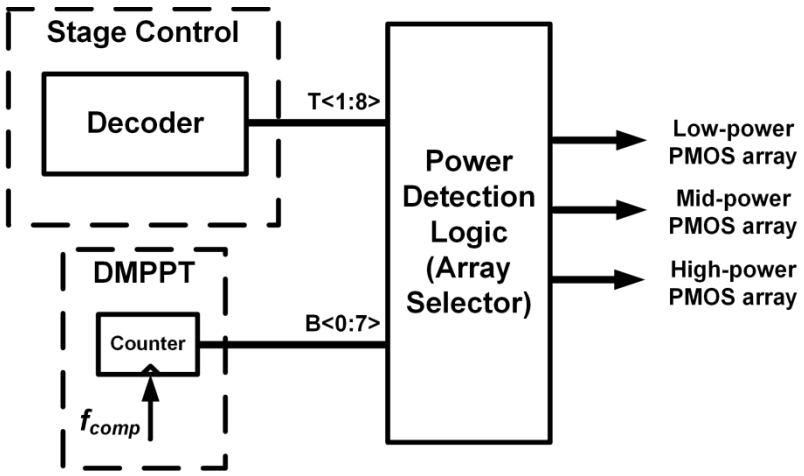

Fig. 133. LDO pass device array selector.

Fig. 134 presents the digital LDO structure; comprised of a resistive divider, comparator, counter, decoder, and 3 banks of pass device arrays. The decision to implement a resistive divider for the LDO instead of a capacitive divider is due to the need for a steady and ripple-free supply. This produces a quiescent current being consumed (~80 nA), but allows the generation of the LDO voltage reference, V_{ref}. TABLE 13 shows the combination, of both DCO code and number of stages from the main converter (N), which enable the LDO pass device arrays as well as the equivalent input power coming in from the EH source.

It should be noted that for high values of f_{sw}, the number of stages are irrelevant due to the high detected power profile from the DMPPT (low R_{IN}).

The voltage regulation loop continuously compares the output voltage, V_{out}, with V_{ref}, depending on load current demand V_{out} may exceed or go below V_{ref}, this triggers the comparator high or low which in turn increases/decreases the 5-bit counter, leading to an increase or decrease in the number of individually driven

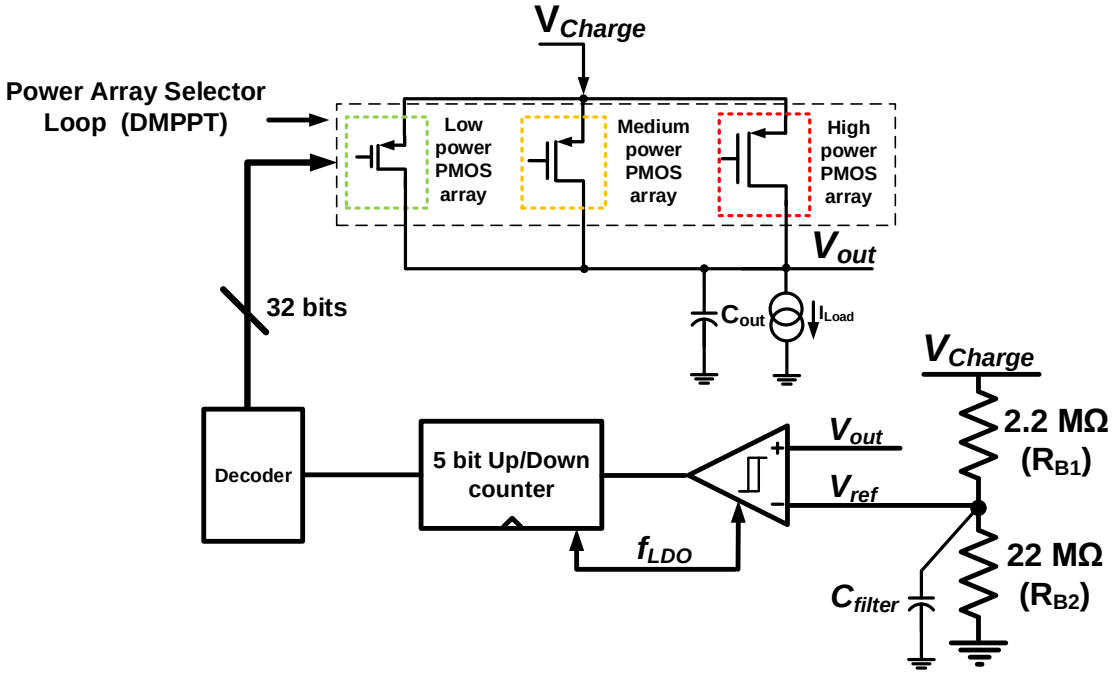

Fig. 134. Digital LDO implementation.

devices by the decoder. The digital LDO structure possesses a dedicated clock free running at ~ 1 MHz, f_{LDO}. Each array is divided up into 32 separate transistor fingers which are individually enabled through a load feedback loop.

Where

$$V_{ref} = \frac{V_{charge}\, R_{B2}}{R_{B2} + R_{B1}} \tag{101}$$

Thus;

$$V_{out} = \frac{V_{charge}}{1 + \frac{R_{B1}}{R_{B2}}} \tag{102}$$

TABLE 13. Power detection logic parameters for LDO array selector.

POWER SPECIFICATION	DCO CODE	NUMBER OF STAGES (MAIN CONVERTER)	INPUT POWER LEVEL
High Power Array	0H-FH	ALL STAGES	From 250 μW to 2 mW
Mid Power Array	30H-3FH 10H-1FH	3-5 STAGES	From 50 μW to 249 μW
Low Power Array	F0H-FFH 70H-7FH	6-9 STAGES	From 12 μW to 49 μW

As with any regulator, efficiency is crucial in the design of the PMU. This becomes even more so in EH systems. Due to the switching nature of the digital LDO, efficiency calculations were performed to set the ideal size for the pass device of the regulator, for the power levels expected at the input of the PMU. Fig. 134 shows the equivalent model of the digital LDO.

As shown in (2), each transistor array is sized to handle a particular power domain (Low, Mid, and High), that is available from the EH source.

$$\frac{W}{L}_{Array} = \frac{2I_{load}}{V_{drop}K_p\left(V_{charge} - V_t\right)} \tag{103}$$

Following the power ranges from TABLE 13, transistor array sizes were determined to maintain the 200 mV drop (V_{drop}) and expected load current for said power domain. Finally the arrays were divided up into the 32 segments for each array to be individually controlled by a 5 bit decoder. The sizing allows a reduction in switching losses associated with the transistor capacitances, thus improving efficiency for a power limited system without the need of a more complex digital controller.

Measurement results

The PMU was design and implemented in 180 nm CMOS process. Fig. 135 shows the prototype converter PCB and die photo. The PCB dimensions are 3cm x 3cm, and die has 2 mm x 2mm dimensions. The PMU works for input voltages (once startup sequence has run its course) ranging from 250 mV to 1.1 V for the main converter. The storage capacitor C_{charge}, was set at 1 mF, and output capacitor (output of digital LDO) set at 10 µF. The external capacitors used for MPP acquisition are set at 100 pF, 100 pF and 33 nF for C_1, C_2, and C_{PV} respectively. The capacitive divider for the Stage Control block was performed with 10 µF external capacitors. Finally, the resistive divider for the digital LDO control loop was implemented with 2 external resistors of 2.2 MΩ and 22 MΩ to set the reference. V_{REF}, at 1.8 V.

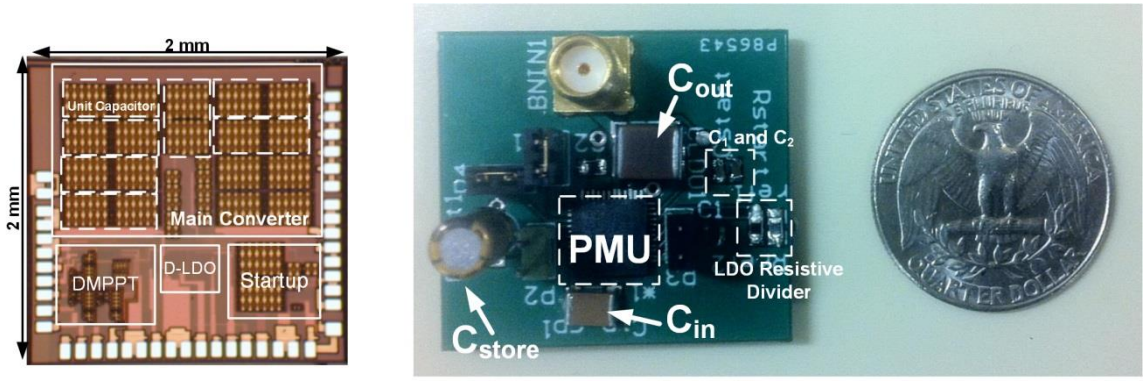

Fig. 135. a) Die microphotograph and b) PCB footprint comparison to US quarter.

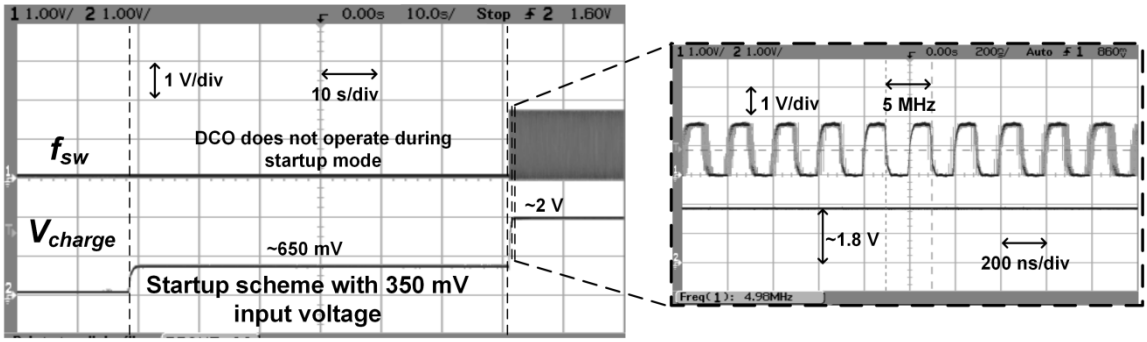

Fig. 136. Startup scheme with handoff operation to main converter.

Startup scheme

Fig. 136 shows the startup operation as well as the handoff to the main converter. The input voltage is set to 350 mV, which deliver ~650 mV at V_{charge}. The main DCO operating frequency is also shown and how it begins operating only once handoff has occurred. The V_{charge} node increases from 650 mV at startup to 2 V after handoff. Stage

control is also shown in Fig. 136, highlighting the stage decrease to meet the required output voltage, no load conditions were set for this test.

Digital maximum power point tracking

Multiple tests were performed on the PMU to surmise MPPT efficiency with the different EH sources. Fig. 137 shows the MPPT efficiency of the presented PMU. As expected, the OCV method proves reliable for both MFC and TEG sources, with >95 % tracking efficiency for input powers < 100 μWs. The error at higher input powers translates to lower internal resistances from the MFC and TEG sources; hence, higher switching frequencies are required from the DCO. As can be seen from Fig. 137, the resolution for switching frequencies is diminished at higher frequencies, causing the error in MPPT tracking efficiency.

The results for the SC source show a lower MPPT efficiency, maximum at 87%; this is due to the nonlinear nature of the SC source, and the implementation of the OCV method. Although the MPPT efficiency is lower than previously reported literature, the overall control power consumption + capacitive divider is minimal when compared (~580 nW) to other reported works [159, 169].

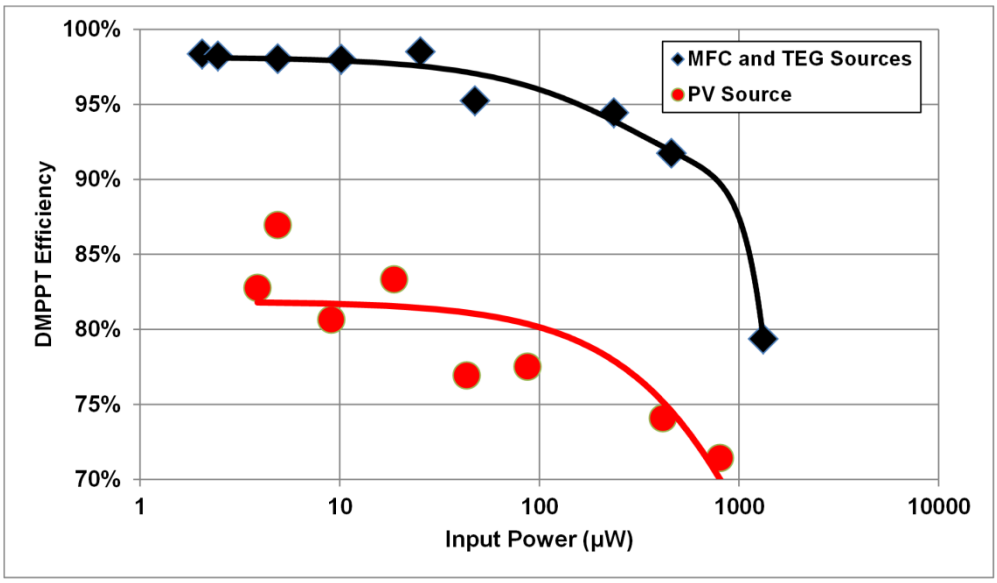

Fig. 137. Digital maximum power point tracking efficiency for MFC, TEG, and PV solar cells.

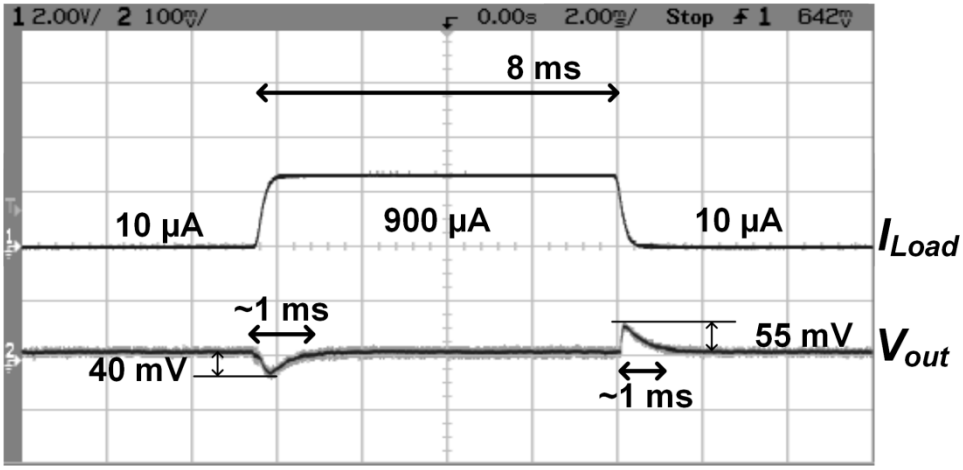

Fig. 138. Digital low-dropout regulator load regulation test for 1.75 mW of input power and a 900 µA step load current.

Voltage regulation (digital LDO)

Fig. 138 shows the load test response of the system for a step of ~900 μA. Output voltage (V_{out}) is regulated at 1.8 V from the 2 V stored at V_{charge}. A maximum voltage overshoot of 55 mV can be seen, with a settling time of ~ 1 ms for both step cases.

Wireless sensor node temperature sensor testing

Additional tests of the PMU powering a wireless sensor were also performed to showcase the PMU's power delivering capabilities. The PMU was powered by Laird Technologies thermoelectric module, showing a 550 mV OCV and equivalent internal resistance of ~10 Ω ($P_{in} = 30\ mW$).

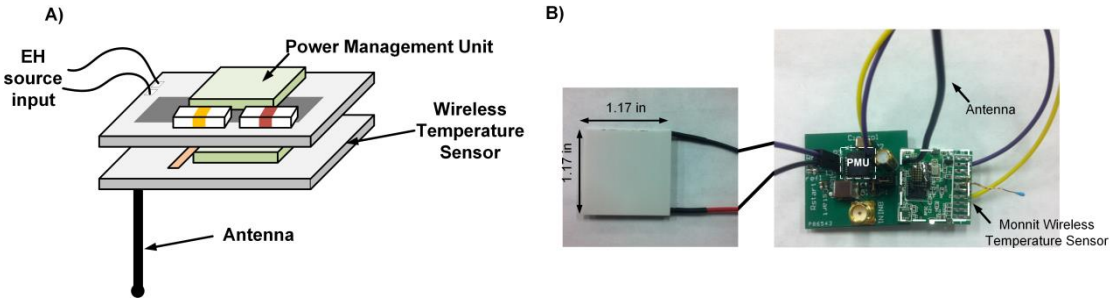

Fig. 139. Internet of Things (IoT) testing configuration A) illustration of power management unit with temperature sensor and B) unfolded implementation for IoT configuration with thermoelectric generator unit.

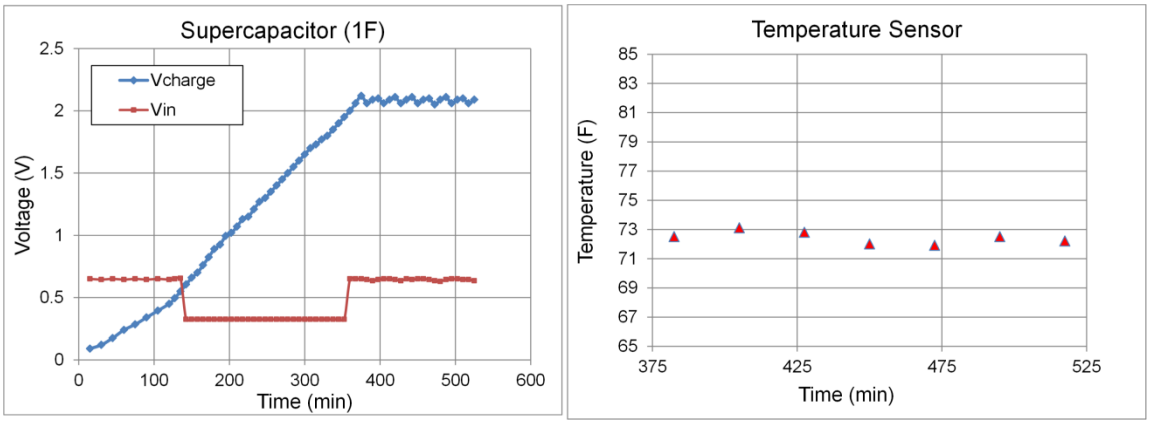

Fig. 140. Wireless sensor node testing voltage profile A) with 1F supercapacitor at C_{store} and B) temperature sensor transmitted results.

A 1 F supercapacitor was placed as C_{store} for the testing procedures, and the wireless sensor used was a Monnit Wireless Temperature Sensor [170]. Fig. 139A shows an illustration of the implemented PMU with sensor node, and Fig. 139B shows the implemented sensor with PMU in an unfolded configuration as well as the utilized TEG unit.

The sensor was powered with an operating voltage of ~2 V at V_{charge} (900 MHz operating frequency for wireless transmission). Power of 85 mW is consumed during each sense and transmit event. Fig. 140 shows A) the voltage charging profile at V_{charge}, as well as the input voltage through the startup, MPPT, and 2 V output voltage setting; B) shows the registered temperature transmitted by the sensor.

Power consumption and efficiency

Fig. 141 breaks down the power consumed by both 500 kHz and 5 MHz f_{sw}. Power consumption will automatically set depending on the power availability at the input MFC source, i.e. higher input power requires higher f_{sw} to decrease R_{in} and increase input extracted current, while lower input power requires lower f_{sw} to increase R_{in} and decrease input extracted current.

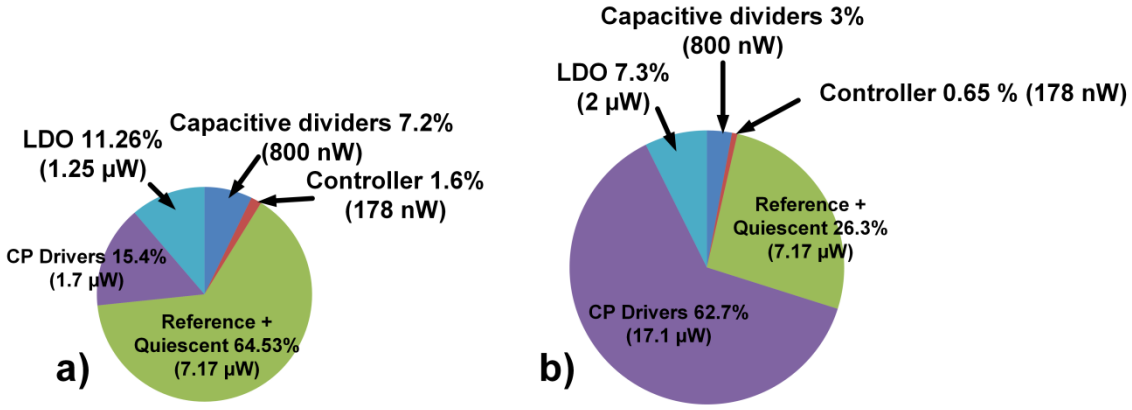

Fig. 141. Power consumption by block for PMU at a) 500 kHz f_{sw} and b) 5 MHz f_{sw}.

Maximum end-to-end efficiency was measured to be at 57 % with 1.75 mW of input power, Fig. 142 shows efficiency results for different input power profiles. Minimal bias current is consumed from the system (from reference for Stage Control and resistive divider in LDO) and the presented design is capable of delivering both MPP tracking and output voltage regulation with minimal power consumption. TABLE 14 summarizes results and compares to previously reported solutions.

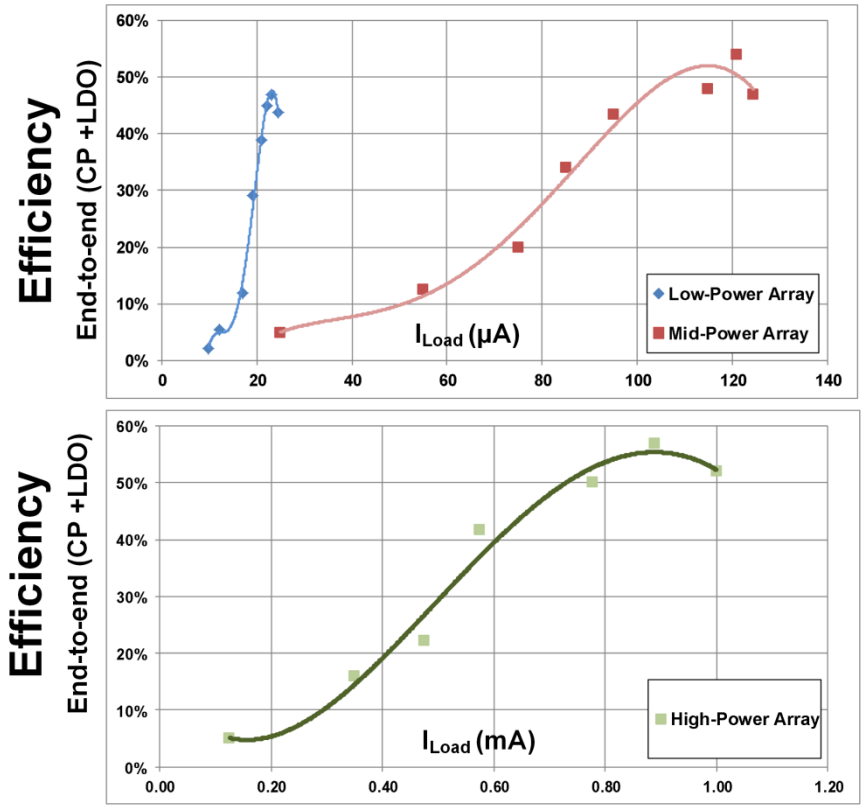

Fig. 142. End-to-end efficiency for 9 stage enabled (10X gain) main converter and digital LDO.

TABLE 14. Performance summary

SPECIFICATION	[150]	[42]	[171]	THIS WORK
Input Voltage Range	350 mV– 480 mV	1 V – 5 V	320 mV – 600 mV	250 mV – 1.1 V (for main converter)
Output Voltage	1.4 V (regulated)	2 V (un-regulated) 1.508 V (regulated)	2.04 V – 3.7 V (un-regulated)	2 V (un-regulated) 1.8 V (regulated)
Power Consumption	3 µW (Quiescent only)	2.11 µW (Controller only Driver power not included)	Not reported (startup scheme only)	1.18 µW controller @ 500 kHz f_{sw} 11 µW with driver power consumption @ 500 kHz f_{sw}
Startup	270 mV (unregulated output voltage) 400 mV (regulated output voltage)	-	320 mV	350 mV (regulated output voltage)
MPPT	No	Yes	No	Yes
Autonomous	Yes	No	Yes	Yes
Impedance Matching Range	NA	100 kΩ	NA	>300 kΩ to <10 Ω (discrete steps)
Regulation	No	Yes (external reference)	No	Yes @ 1.8 V
Input Source	Solar Cell/ Thermoelectric generator (TEG)	TEG	Microbial Fuel Cells (MFC)/TEG/Solar Cells	MFC/TEG/Solar Cells
Max. Efficiency	65% (for 4 stage CP)	82% (For 1 stage charge pump)	89% (capacitive load, no current demand)	90% w/o regulation (1 Stage for Charge Pump) 81% w/D-LDO (1 Stage for Charge Pump)
Technology	0.13 µm	0.35 µm	0.18 µm	0.18 µm

Conclusions

This chapter presents a PMU able to perform startup operation, maximum power extraction for DC type EH sources (solar, thermal, biomass), and deliver a regulated output voltage through a digital LDO regulator, presenting a solution to the regulation and maximum power extraction dilemma present in current PMU solutions aimed at EH sources. The PMU operates in a complete autonomous fashion, with charging/regulation capabilities with minimum power consumption, and allows operation from voltages as low as 350 mV through the startup block. Maximum power extraction is performed through a fully digital MPPT scheme, allowing for minimal quiescent consumption with minimum power overhead cost. Information about the source-power density availability from the DMPPT and number of stages implemented from the Stage Control is passed on to the digital LDO, which uses this information to increase or decrease the pass transistor size. This allows for an overall power consumption decrease by reducing the gate driving losses associated with large pass transistor devices and enhance efficiency while delivering a regulated voltage to noise sensitive blocks. The PMU possesses the capability of internal reference generation through capacitive, and resistive dividers, as well as an internal voltage reference allowing for true autonomous operation. The system was fabricated in 180 nm CMOS process and maximum end-to-end efficiency was measured to be at 57 % with 1.75 mW of input power

CHAPTER VIII

SUMMARY AND FUTURE WORK

The design and implementation of inductive, capacitive and linear regulators for energy harvesting technology has been presented. Solutions for thermoelectric generators, microbial fuel cells, and photovoltaic energy harvesting sources have been fabricated and tested.

Chapter III showed a solution for a thermoelectric generator array intended for medical applications. The implemented inductive switching regulator is capable of achieving maximum power transfer through a frequency modulation tracking loop, while maintaining high efficiency through a Pseudo-Zero Current Switching scheme. Results obtained show comparable to state-of-the-art solutions with a wider matching range by the presented regulator.

Chapter IV showed a solution for microbial fuel cells through a self-powered, inductive switching regulator. A new maximum power point tracking scheme was implemented in order to manage the internal parasitic capacitance of the fuel cell and correctly achieve matching between the fuel cell and regulator. A true Zero Current Switching scheme is also implemented to enhance overall efficiency of the solution by over 40% compared to the results obtained from the proposed PMU in chapter III.

Chapter V presents a capacitive switching regulator capable of handling arrays of microbial fuel cells or thermoelectric generators. The regulator utilizes a frequency modulation control in order to match the internal impedance of the fuel cells with its own internal impedance to ensure maximum power transfer. The regulator also

possesses a programmable stage control to allow for a level of output voltage regulation while maintaining minimum power consumption. Overall results show comparable results to state-of-the-art solutions, with improved matching and power extraction dynamics.

Finally, chapter VI presents a fully autonomous, capacitive switching regulator with a digital Low Dropout regulator for a full power management unit aimed at Internet of Things applications. The capacitive regulator is capable of performing maximum power transfer from any DC type energy harvesting sources. The power management unit also performs a start-up operation without the need of additional power from batteries or charged capacitors. Regulation is performed by communication between the main regulator and dropout regulator in order to enhance pass device size, thus improving power efficiency.

The common denominator is the need for further research into simultaneous multiple input energy harvesting regulators can be potentially explored to present a truly stand-alone solution capable of dealing with multiple availability conditions of the energy harvesting transducers. This multiple source harvesting implementation is recommended if energy harvesting is to be adopted by mainstream applications.

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APPENDIX

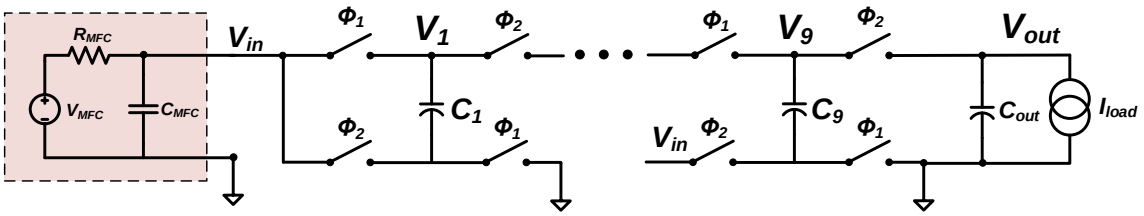

Fig. 143. 9 stage I-DCDC converter with associated capacitor voltages.

Small-signal control-to-input transfer function

The following appendix will demonstrate how the small-signal used in the MPPT control loop was obtained.

The transfer function is obtained by solving for the time domain transient response in both charging and discharging phases (Fig. 143). Once the time domain behavior equations are acquired, an averaged value solution follows:

$$C_{MFC} \cdot \frac{d\mathrm{V_{in}}}{dt} = (A_{MFC\Phi 1})\left(\mathrm{T_{on}}\ (\mathrm{F_{sw}})\right) + (A_{MFC\Phi 2})\left(\mathrm{T_{off}}(\mathrm{F_{sw}})\right) \tag{104}$$

$$C_i \cdot \frac{d\mathrm{V_i}}{dt} = \left(A_{C_i\phi 1}) + A_{C_{i+1}\phi 1}\right)\left(\mathrm{T_{on}}\ (\mathrm{F_{sw}})\right) + \left(A_{C_i\phi 2} + A_{C_{i+1}\phi 2}\right)\left(\mathrm{T_{off}}(\mathrm{F_{sw}})\right) \tag{105}$$

where $A_{MFC\Phi 1}$, $A_{MFC\Phi 2}$, $(A_{C_i\phi 1}) + (A_{C_{i+1}\phi 1})$, and $(A_{C_i\phi 2}) + (A_{C_{i+1}\phi 2})$ are the associated time capacitor charging currents referred to each particular stage capacitor, the term T_{on} and T_{off} is the on and off time for each phase (50% of the period for charge-discharge phases), and F_{sw} is the steady stage value of the switching frequency.

$$C_{MFC} \cdot \frac{d(V_{in} + v_{in})}{dt} = (A_{MFC\Phi 1} + a_{MFC\Phi 1})\left(T_{on}\,(F_{sw} + f_{sw})\right) + (A_{MFC\Phi 2} + a_{MFC\Phi 2})\left(T_{off}(F_{sw} + f_{sw})\right) \tag{106}$$

$$C_i \cdot \frac{d(V_i + v_i)}{dt} = \left((A_{C_i\phi 1} + a_{C_i\phi 1}) + (A_{C_{i+1}\phi 1} + a_{C_{i+1}\phi 1})\right)\left(T_{on}\,(F_{sw} + f_{sw})\right) + \left((A_{C_i\phi 2} + a_{C_i\phi 2}) + (A_{C_{i+1}\phi 2} + a_{C_{i+1}\phi 2})\right)\left(T_{off}(F_{sw} + f_{sw})\right) \tag{107}$$

As shown in Chapter II, a small signal perturbation is introduced to obtain the control to input transfer function. Once second order terms (non-linear) and DC terms (no perturbation) are discarded, the linearized (steady-state) transfer function is obtained. where $a_{MFC\Phi 1}$, $a_{MFC\Phi 2}$, $a_{C_i\phi 1} + a_{C_{i+1}\phi 1}$, and $a_{C_i\phi 2} + a_{C_{i+1}\phi 2}$ are the small signal perturbation induced to each particular stage capacitor and f_{sw} the small signal perturbation of the switching frequency. For the following design the postulation is made that the output node (V_{out}) is under light load with a large valued output capacitor (100

mF) causing AC ground at this node [112]. This greatly simplifies analysis and the acquisition of the C-to-I transfer function.

Stability analysis for MPPT loop

The following appendix section will illustrate how the stability of the MPPT affects correct MPP attainment. The stability parameters for the complete MPPT are enhanced through the implementation of the Type II filter. Fig. 2 below shows the open loop bode plots for both MFC-H and MFC-L input, with GBP is increased to 74 kHz and 47° phase margin for MFC-H (MFC-HOpt), and for MFC-L, the GBP and phase margin are 150 Hz with 87° of improvement (MFC-LOpt).

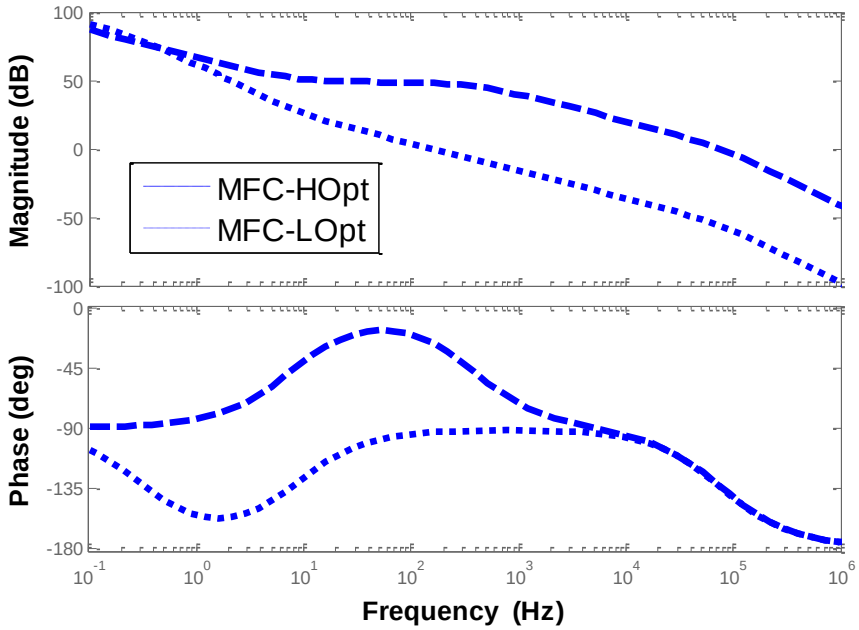

Fig. 144. Open loop gain and phase margin with optimized filter design.

By not optimizing loop stability parameters in the full MPPT open loop, whenever a switch between sources occurs, a faulty MPP will occur. The simulation in Fig. 145 shows this behavior when implementing a 1 nF capacitor as the filter, F(s), for the MPPT control loop.

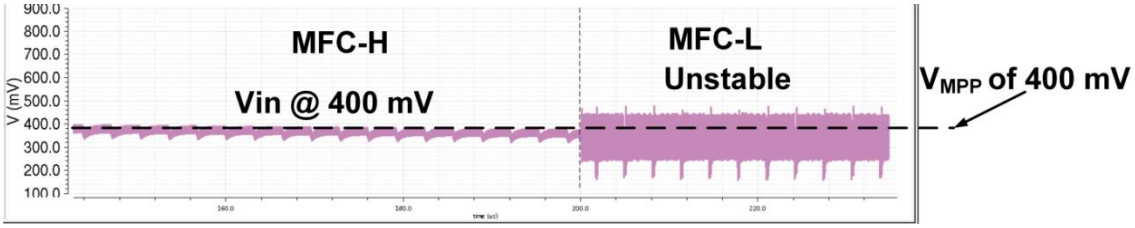

Fig. 145. Effect of stability in MPPT when switching between MFCs (MFC-H to MFC-L) and unstable response.