RF POWER TRANSFER, ENERGY HARVESTING, AND POWER MANAGEMENT STRATEGIES

A Dissertation

by

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ABSTRACT

Energy harvesting is the way to capture green energy. This can be thought of as a recycling process where energy is converted from one form (here, non-electrical) to another (here, electrical). This is done on the large energy scale as well as low energy scale. The former can enable sustainable operation of facilities, while the latter can have a significant impact on the problems of energy constrained portable applications. Different energy sources can be complementary to one another and combining multiple-source is of great importance. In particular, RF energy harvesting is a natural choice for the portable applications. There are many advantages, such as cordless operation and light-weight. Moreover, the needed infra-structure can possibly be incorporated with wearable and portable devices. RF energy harvesting is an enabling key player for Internet of Things technology. The RF energy harvesting systems consist of external antennas, LC matching networks, RF rectifiers for ac to dc conversion, and sometimes power management. Moreover, combining different energy harvesting sources is essential for robustness and sustainability.

Wireless power transfer has recently been applied for battery charging of portable devices. This charging process impacts the daily experience of every human who uses electronic applications. Instead of having many types of cumbersome cords and many different standards while the users are responsible to connect periodically to ac outlets, the new approach is to have the transmitters ready in the near region and can transfer power wirelessly to the devices whenever needed. Wireless power transfer consists of a dc to ac conversion transmitter, coupled inductors between transmitter and receiver, and an ac to dc conversion receiver. Alternative far field operation is still tested for health issues. So, the focus in this study is on near field.

The goals of this study are to investigate the possibilities of RF energy harvesting from

various sources in the far field, dc energy combining, wireless power transfer in the near field, the underlying power management strategies, and the integration on silicon. This integration is the ultimate goal for cheap solutions to enable the technology for broader use. All systems were designed, implemented and tested to demonstrate proof-of-concept prototypes.

DEDICATION

To the Creator,

To my mother, father, and brothers

To my wife, and daughter

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In this life, everything is destined and I was happy with everything that happened to me during the graduate study in Texas A&M University. I got to understand, discover, and digest many aspects in this life, not just the academic ones. Firstly, I thank ALLAH for help during my life. I would like to acknowledge my advisor, Prof. Edgar Sánchez-Sinencio, for his help and support. I have learned a lot from his academic and life experience. He guided me through the past five years and I appreciate everything he did with me. He pushed me hard to extract the best from me that I didn't imagine that I can do so. All my other committee members, Prasad Enjeti, Mahmoud El-Halwagi, and Sam Palermo are among the best people I have met. I learned a lot from their knowledge and during coursework, especially Enjeti whose character and knowledge inspired me in many aspects. I would like to thank my college friends, Hatem Osman, Ahmed Rabie, Ahmed Salah, Ayman Shafik, Hasan Tahir Abbas, Omar Abdel Monem, Mostafa Mousa, Bahaa Hafez, Tarek Elgohary, Mohamed Elkhouly, Amr Abouelil, Sherif Shakib, Alexander Edward, and many others who my memory can't help me with. Even though not all of them work in the same lab with me, everyone contributed to my life and success through advice and help. Furthermore, I would like to thank my lab friends who graduated and will be graduating—Salvador Carreon-Bautista, Johan Estrada, Chao-Hsiuan Tsay, Roland Rebiero, Xiaosen Liu, Sungjun Yoon, Kyoohyun Noh, Judy Amanor Boadu, Alireza Saghati, Ashkan Zamir, Minglei Zhang.

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power converters and how technology can be used to the teacher's advantage. The course of MRI hardware with Steven Wright and Mary McDougall opened a new area of thoughts in biomedical engineering and they are really good teachers. Furthermore, Wright gave me the opportunity to attend his course in phased array, where I learned that science is all connected together. Ultra sound course with Raffaella Righetti was a continuum to this world of biomedical interfaces. Many thanks to Scott Miller who allowed me to audit his course in wireless communications where I learned that if my field was not circuit design, definitely, it would have been wireless communications. Thanks to Kamran Entesari for his rigorous power amplifiers course. Lastly, but not least, my advisor, Edgar Sánchez-Sinencio, taught one of the best courses in analog filter design, where I learned a lot from his experience. Thanks to all of the aforementioned professors for their knowledge that gave me a big push in my research career.

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Contributors

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All other work conducted for the dissertation was completed by the student independently.

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1. INTRODUCTION

1.1 Internet of Things (IoT)

The IoT term was first coined by Kevin Ashton in 1998 and later defined as "The Internet of Things allows people and things to be connected Anytime, Anyplace, with Anything and Anyone, ideally using Any path/network and Any service" [1]. Fig. 1.1 summarizes the IoT technology. According to [2], the fundamental technologies for IoT are Radio-Frequency Identification Device (RFID) and Wireless Sensor Network (WSN) that appeared from 1980s and 1990s respectively. The former is associated with automatically identifying and tracking while the latter address intelligent sensor networks, health-care monitoring, industrial monitoring, environment monitoring. In addition, many other technologies such as bar-codes, smart phones, social networks, cloud computing are supporting the rise of IoT technology. According to [1], the expected functionalities of IoT solutions can be identified under five categories: smart wearable devices, smart home: platforms., virtual assistance, smart objects and digital relationships, smart city: smart traffic, platforms, resource management and activity monitoring, smart environment: air quality, water quality and natural disaster monitoring, smart farming and smart enterprise: transportation and logistics, infrastructure and safety, energy and production and resources management.

The available technologies for powering IoT devices [3] are: non-rechargeable batteries, rechargeable batteries, printable batteries, solid-state batteries, super capacitors, and energy harvesting.

1.2 RF Energy Harvesting

RF energy is used for wireless communications and it could be found almost everywhere. The power density of the transmitted signals depends on both frequency and time

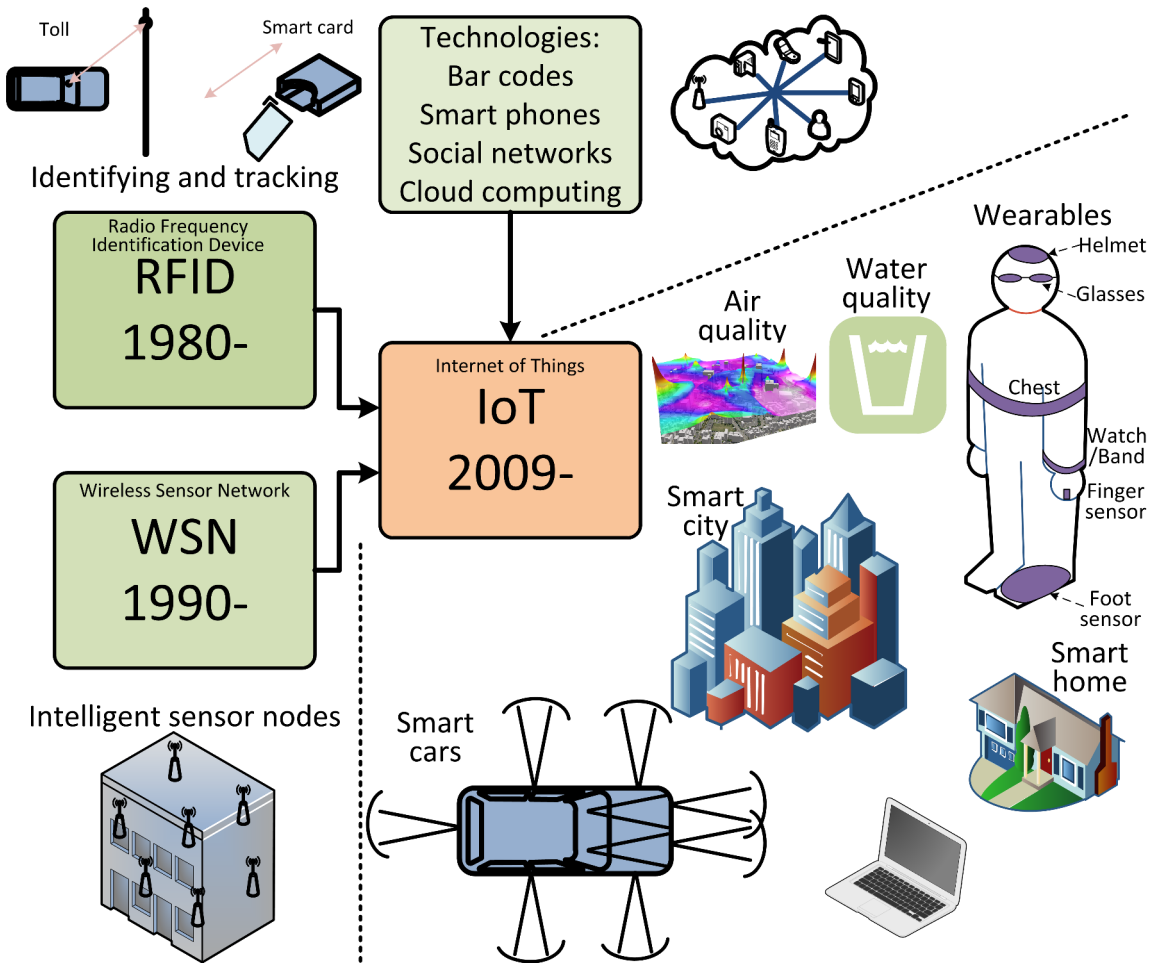


Figure 1.1: IoT: Hardware point of view.

[4] as shown in Fig. 1.2 and is sinusoidal in nature. It can be received through an antenna and converted to dc power through a rectifier. The process of RF power rectification to dc power has gained a lot of attention in many disciplines especially for RFIDs [5, 6]. The rectifier could be implemented using charge pumps which are a cascade of passive voltage doublers. Moreover, impedance matching is needed between the antenna interface and the rectifier input impedance to ensure maximum power transfer. In order to have estimates for the available RF power, the spectrum measurements are needed and this can vary between city to city in the world. Fortunately, there is a new observatory program hosted by Microsoft® [7] that allows any organization to deploy its RF measurement equipment, data can be logged over time and this can be published.

As an example, Fig. 1.3 shows the measured spectrum of the University of Santa Barbra observatory station for the period of one day. From the shown measurements, the RF power is localized in bands. Also, the power levels are not too high and all RF rectifiers have a minimum detectable signal (sensitivity ~ -24dBm) below which no power can be sensed [8]. There are standards that allocate the RF spectrum as shown in Fig. 1.4. This shows the various frequency bands of wireless standards. The AM channels are located at the lowest frequency range from 535-1605 kHz. The traditional FM is between 88-108 MHz. The TV channels are allocated in subgroups, 54-72 MHz, 76-88 MHz, 174-216 MHz, 512-608 MHz, and 614-698 MHz. The GSM is located between 824-849 MHz and between 869-894 MHz. ISM bands spans from 902-928 MHz and from 2400-2500 MHz. The DCS is located in two sub-bands, 1710-1755 MHz and 2110-2155 MHz. Finally, the GSM 1900 (4G) is from 1850-1910 MHz and 1930-1990 MHz. The ultimate goal is to harvest power from all these bands but there are always trade-offs between losses associated with multi-band design and the power gained from this technique. The generalized Friis transmission equation, that governs the far-field wireless links and shown in Fig. 1.5, is given by:

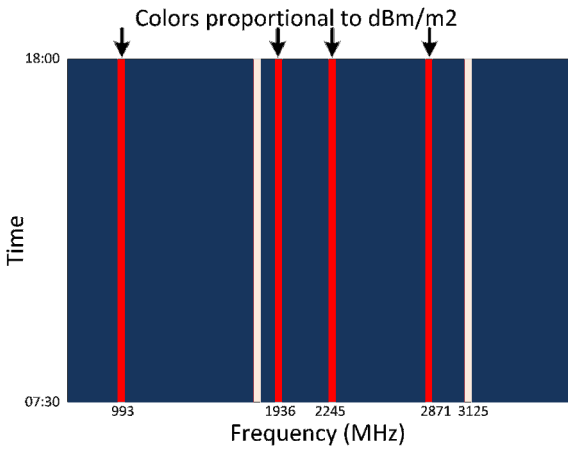


Figure 1.2: Frequency and time dependence of ambient RF power.

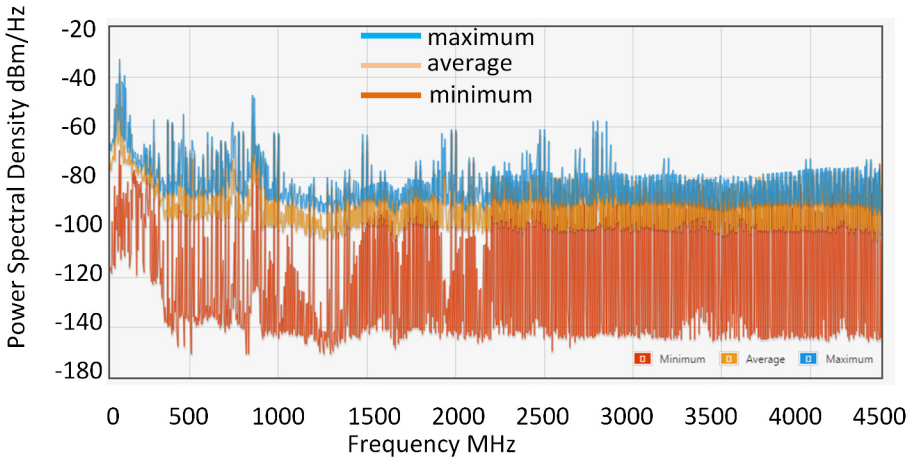


Figure 1.3: Average power spectral density over time.

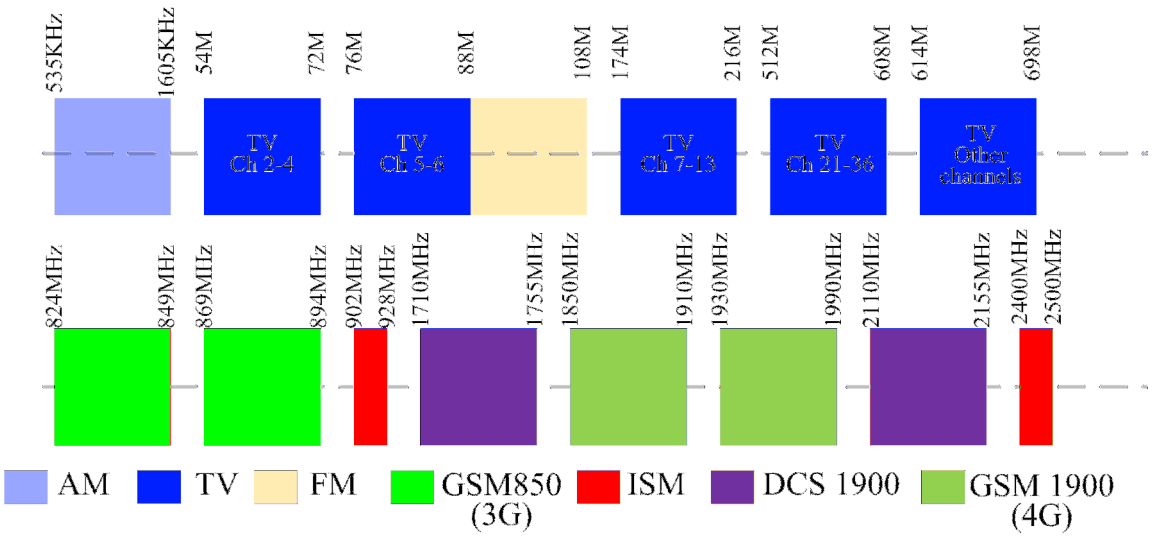


Figure 1.4: RF spectrum according to FCC standards.

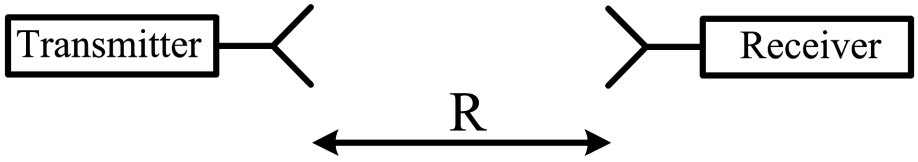


Figure 1.5: RF wireless far-field link.

$$P_r = P_t \frac{G_t G_r \lambda^2}{(4\pi R)^2} pq, \tag{1.1}$$

where P_r is the power at the receiving antenna, P_t is the output power of transmitting antenna, G_t and G_r are the gains of the transmitting and receiving antennas respectively, λ is the wavelength, R is the distance between the antennas, p is the polarization efficiency (polarization mismatch factor), and q is the impedance mismatch factor. The received power is dependent on all of these factors; particularly the received power is quadratically inversely proportional to the distance between transmitter and receiver which results in weak signals at the receivers.

A typical RF energy harvesting system is shown in Fig. 1.6. The antenna is a sensor that acquires the Electromagnetic waves in the space and converts them into a time-varying signal. In order to maximize the transferred power from the antenna to the next RF block, a loss-less (ideally) matching network is needed to transform the impedance to the antenna impedance, which is usually 50 Ω (to be discussed later). The rectifier/charge pump circuit is responsible for the conversion of the ac to dc signal which is composed of a group of capacitors and diodes. The realization of the diodes is done in several ways in the literature as shown in Fig. 1.7 where NMOS and PMOS realizations can be used. During forward bias, the diode experiences a drop V_T and this can be compensated by introducing a voltage difference (effective battery) V_C between the gate (drain) and the drain (gate) for the NMOS (PMOS). In the reverse region of the diode, the diode is supposed to be completely off. The introduced voltage difference can affect the reverse current since the effective gate-source voltage is now higher than the original case. So, an optimum between the forward bias loss and the reverse bias loss can be achieved by the choice of the value of V_C. To implement the effective voltage difference, a pre-charged capacitor [9] can be used. Dynamic bootstrapping where a capacitor is periodically charged and then applied to the gate-drain as was reported in [10]. Static bootstrapping with feedback from the output to

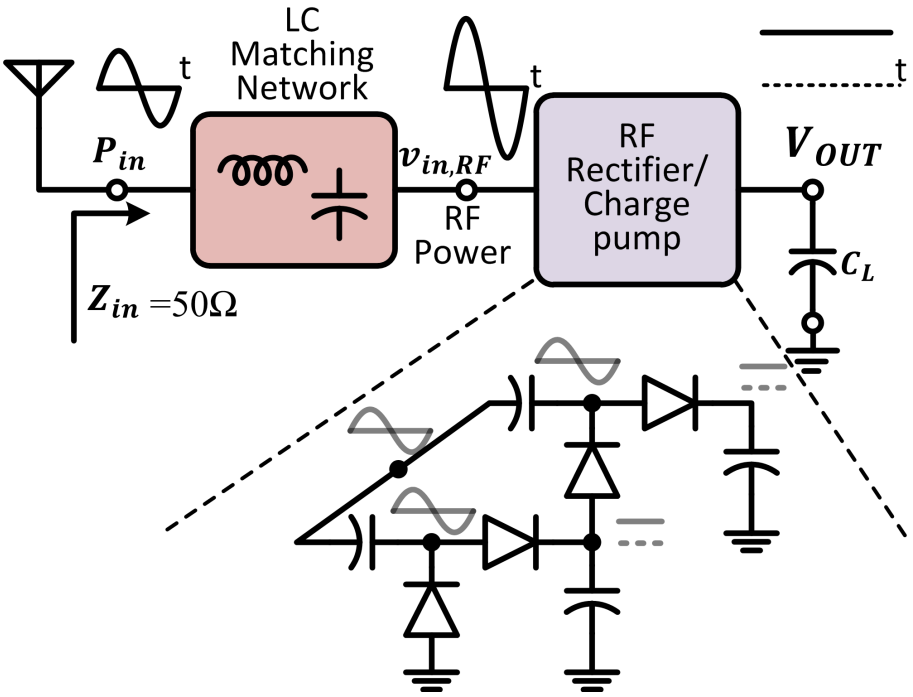


Figure 1.6: An RF energy harvesting front end.

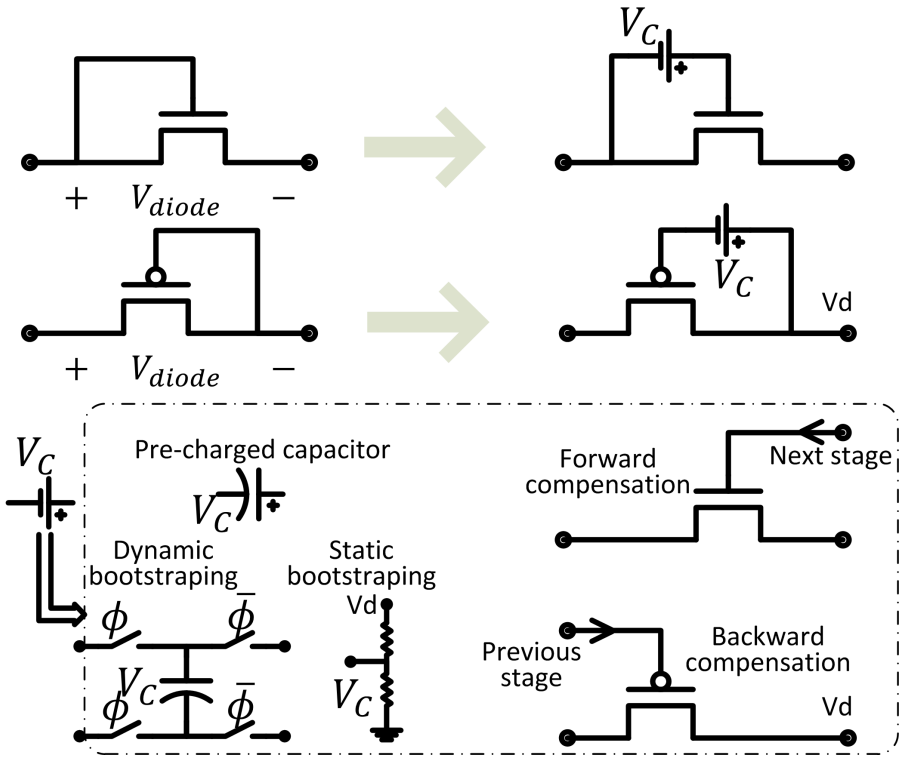


Figure 1.7: Realization of diodes.

generate the required voltage V_C can be used. Forward and backward compensation [11] can be used for NMOS and PMOS -based charge pumps respectively. The idea is that in forward (backward) compensation, the voltage waveforms from the next (previous) stages is the same nature of the current stage except for a higher (lower) dc shift which can be used to generate the required voltage.

Finally, the use of different energy harvesting sources is vital to provide robustness and sustainability. As shown in Fig. 1.8, the source IN and the sources $Source\,1...n$ can be combined to provide a final output OUT for possible IoT applications. When one or more sources fail, the others can still share the required load. Since the different sources are expected to have different voltages, a series connection is better than a parallel connection, although the latter can be better for more output current capability. High gain dc-dc converters are more suitable for energy harvesting sources that have a low voltage voltage across the transducer terminals. Inductive based dc-dc converters [12, 13] need extra off-chip inductors which raise the cost of the total solution; however, more integrated friendly converters are needed with low power operation.

1.3 Concept of Energy Use

Table 1.1 [14] illustrates the harvested power from an isotropic RF transmitter, TX91501 Powercast transmitter, and a KING-TV tower. The received power is in the microwatt range and strongly dependent on the distance between the source and the receiver as discussed earlier. Although the transmitted power in the TV band is the largest, the distance is usually long which resulted in the same microwatt range. The microwatt harvested power is a typical case for portable energy harvesting applications such as RF, vibration, thermal, solar ... Illustrated in Fig. 1.9, the harvested small dc energy can be stored in a large energy reservoir such as a big buffer capacitor. It is the duality to using a small bucket, fill it with water from the source, e.g. a river, dump it into a large reservoir, and keep

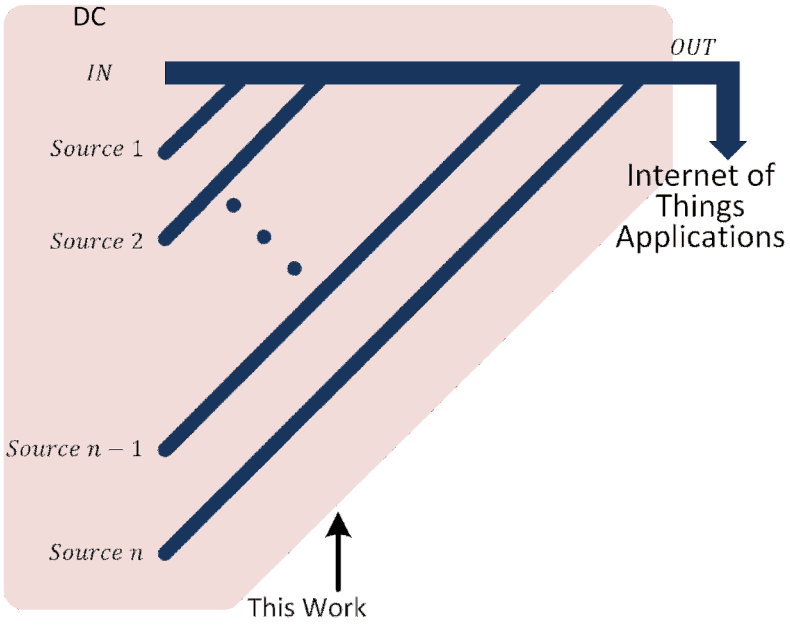


Figure 1.8: DC energy combining from different sources.

Table 1.1: Examples of RF harvested power rates.

RF Source	TX Power P_t	Frequency $\propto \frac{1}{\lambda}$	Distance R	Power Harvested Rate
Isotropic RF transmitter	4W	902-928MHz	15m	5.5μW
	1.78W	868MHz	25m	2.3μW
	1.78W	868MHz	27m	2μW
TX91501 Powercast transmitter	3W	915MHZ	5m	189μW
	3W	915MHz	11m	1μW
KING-TV tower	960kW	674-680MHz	4.1km	60μW

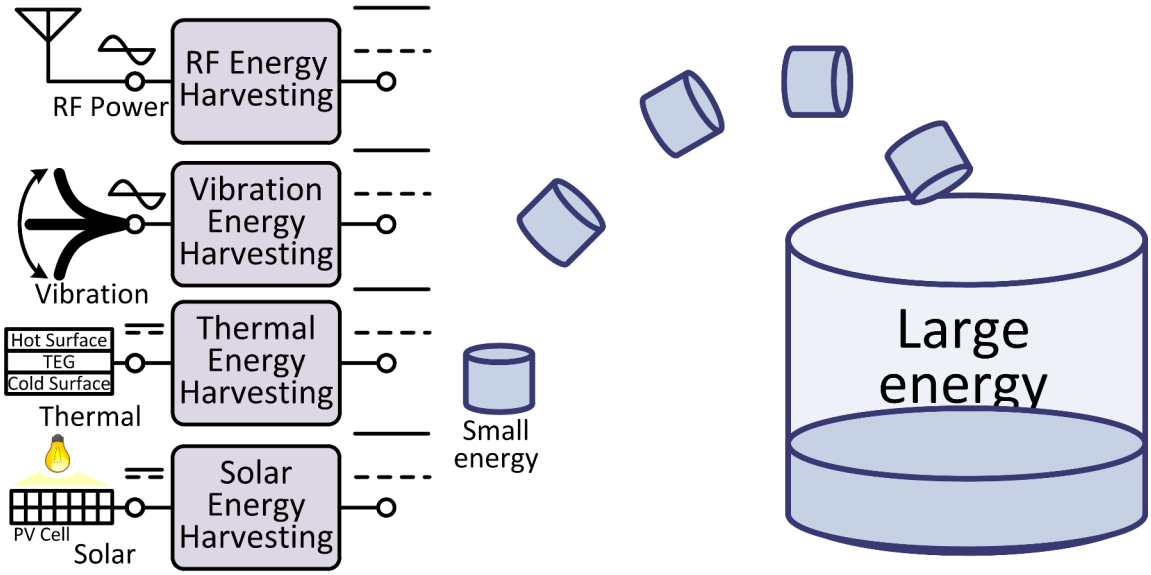


Figure 1.9: Different harvesting units viewed as small energy providers.

doing that. At the end, the large reservoir can be filled and used later for high demand usage. So, the required amount of energy can be harvested given that sufficient wait time is elapsed. Fig. 1.10 (a) shows a Thevenin equivalent circuit to model the energy harvesting (EH) front end at the dc output terminal, a buffer capacitor C_L to store energy, and a switch with control signal ϕ to control the duty cycle of the operation of the load. The equivalent circuit of the EH is a variable source voltage V_{EH} and resistance R_{EH} correspond to the change of the power flow due to the change of the input power. Fig. 1.10 (b) shows charging-discharging effects on the ripple of the voltage of the capacitor V_X which is explained shortly. The capacitor C_L is charged with a current I_{ramp}, where the output voltage V_X is given by:

$$V_X = V_{EH}\left(1 - \exp^{-t/R_{EH}C_L}\right), \tag{1.2}$$

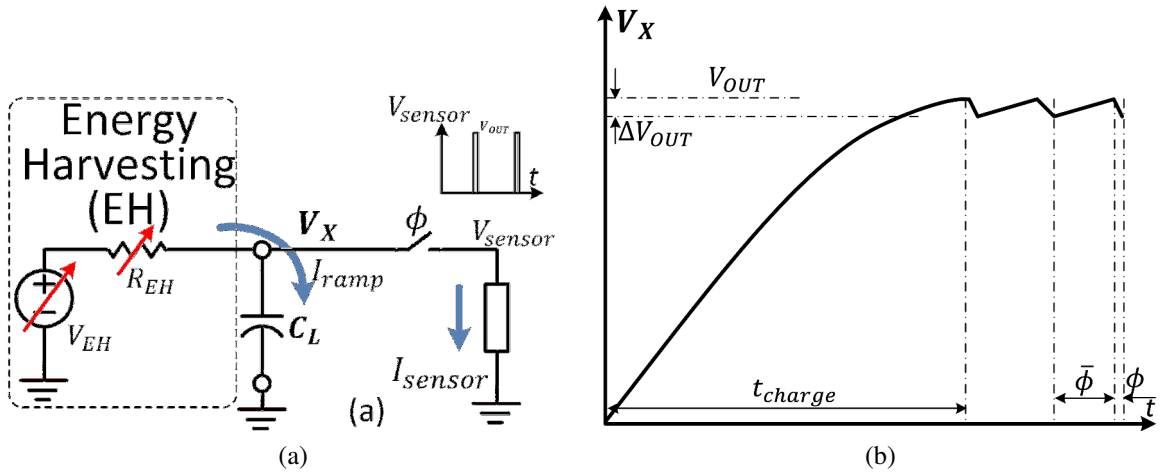


Figure 1.10: Using capacitor C_L as a buffer capacitor, large reservoir: (a) circuit implementation and (b) charging-discharging effects on the ripple of the voltage of the capacitor V_X.

and for the initial time period, the output voltage V_X can be approximated as linearly increasing with time as:

$$V_X = \frac{I_{ramp}}{C_L} t_{charge}, \tag{1.3}$$

where t_{charge} is the charging time from 0 voltage to V_{OUT} value and $I_{ramp} = V_{EH}/R_{EH}$. Thus, the stored energy in C_L is:

$$\text{Energy} = \frac{1}{2} C_L V_X^2 = \frac{1}{2} \frac{I_{ramp}^2}{C_L} t_{charge}^2, \tag{1.4}$$

where the output voltage and energy versus time are shown in Fig. 1.11. The charging of the buffer capacitor is shown in Fig. 1.12 (a). The possible applications/sensors that can be powered by energy harvesting can be modeled as a current demand I_{sensor} as shown in Fig. 1.12 (b). The capacitor C_L can be used to provide the required amount of power through discharging process during time Δt (during ϕ) and the output voltage V_{OUT} will decrease with time. The charging-discharging effects on the output voltage V_X is shown

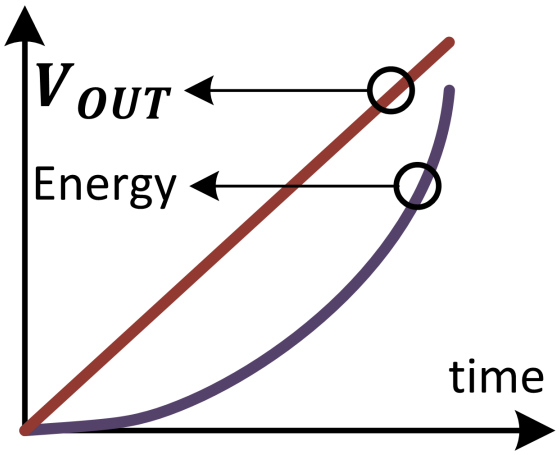


Figure 1.11: The output voltage V_{OUT} and stored energy versus time during charging.

in Fig. 1.13. The ripple voltage ΔV_{OUT} is a critical parameter where this can be specified by the requirements of the load sensor circuit design. This can be expressed as:

$$\Delta V_{OUT} = \frac{I_{sensor}}{C_L}\Delta t. \tag{1.5}$$

For a given sensor with a demand current to operate I_{sensor}, a required nominal voltage V_{OUT}, an allowed ripple voltage ΔV_{OUT}, and a required time Δt to operate to collect data, the minimum capacitor C_L to be used can be derived from (1.5) as:

$$C_L(\text{min}) = \frac{I_{sensor}}{\Delta V_{OUT}}\Delta t, \tag{1.6}$$

and assuming that the dc current supplied by the energy harvesting source is I_{ramp}, (1.4) and (1.5) are combined to estimate the time to wait for charging as:

$$t_{charge}(\text{min}) = \frac{C_L V_{OUT}}{I_{ramp}}\frac{1}{60} = \frac{V_{OUT}}{\Delta V_{OUT}}\frac{I_{sensor}}{I_{ramp}}\frac{\Delta t}{60}, \tag{1.7}$$

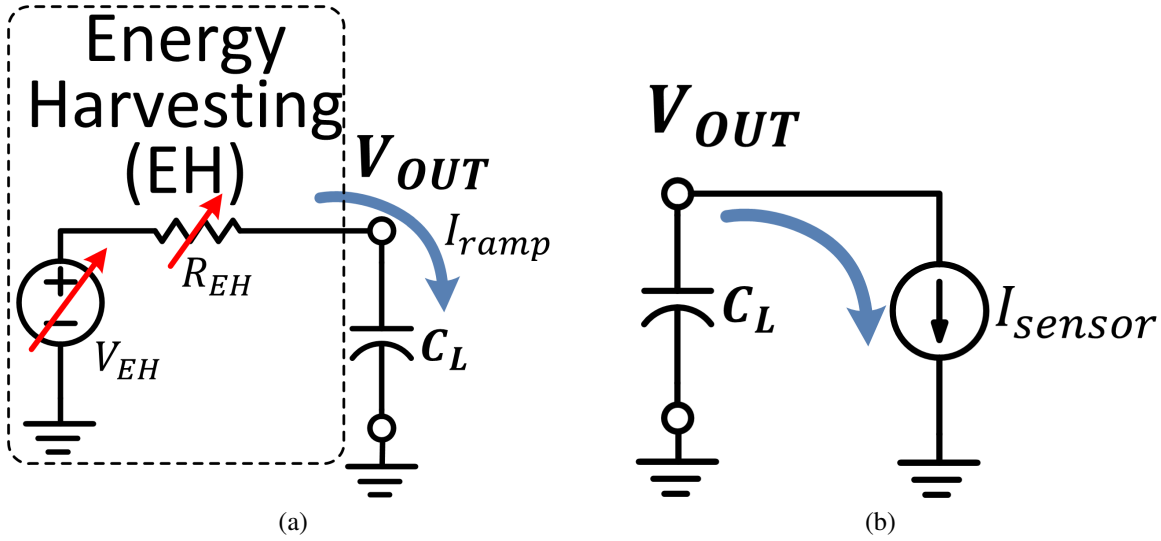


Figure 1.12: Using capacitor C_L as a buffer capacitor, large reservoir: (a) during charging phase, (b) during discharging phase.

assuming an initial condition of 0 voltage on the capacitor. Design examples for a commercial CO_2, a 12-bit ADC, and a transmitter that is designed in TAMU are shown in Table 1.2. This shows that a diverse variety of loads can be supported by the weak energy harvesting sources with providing the appropriate load capacitor and waiting the sufficient time. In the steady-state operation, during $\bar{\phi}$, the capacitor is charged from an initial value that is ΔV_{OUT} below the final value and ΔV_{OUT} can be used in (1.3) instead of V_{OUT}.

Table 1.2: Design examples for the wait time and required capacitor.

	I_{sensor}	C_L	t_{charge} (time to wait)
CO2 sensor	3.5 mA	35 µF	17.5 min.
ADC 12 bits	350 µA	3.5 µF	1.55 min.
TX, TAMU	620 µA	6.2 µF	3.1 min.

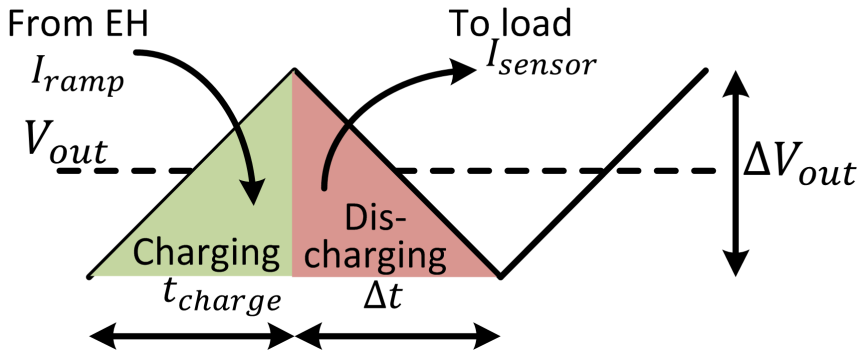


Figure 1.13: Zoom-in for steady-state charging-discharging of the capacitor voltage V_X.

Thus, the estimated time to wait for charging as:

$$t_{charge,ss}(\text{min}) = \frac{C_L \Delta V_{OUT}}{I_{ramp}} \frac{1}{60} = \frac{I_{sensor}}{I_{ramp}} \frac{\Delta t}{60}. \tag{1.8}$$

It should be pointed out that the direct discharging of the load capacitor C_L doesn't fully use all the energy stored in the capacitor. The utilization of the capacitor C_L can be defined as the used energy divided by the total stored energy. Thus,

$$\text{Utilization} = \frac{\frac{1}{2} C_L \Delta V_{OUT} \left(2V_{OUT} - \Delta V_{OUT}\right)}{\frac{1}{2} C_L V_{OUT}^2} \approx \frac{2\Delta V_{OUT}}{V_{OUT}}. \tag{1.9}$$

If an extra boost (inductive-based converter) or a reconfigurable charge pump is used between the capacitor $C_{L,BC}$ and the load, as shown in Fig. 1.14, the voltage on the capacitor V_Y is allowed to reach smaller values (during discharging phase ϕ) while the intermediate converter delivers a regulated output voltage (V_{sensor}) to the load. The extra converter in the power-flow path can degrade the efficiency due to its loss and the required power for controller. A maximum conversion of 2 can maintain good converter efficiency (not including the controller power consumption). For that, the capacitor voltage V_Y is allowed to reach 1/2 of its maximum value and the allowed ripple on the capacitor ΔV_{OUT}

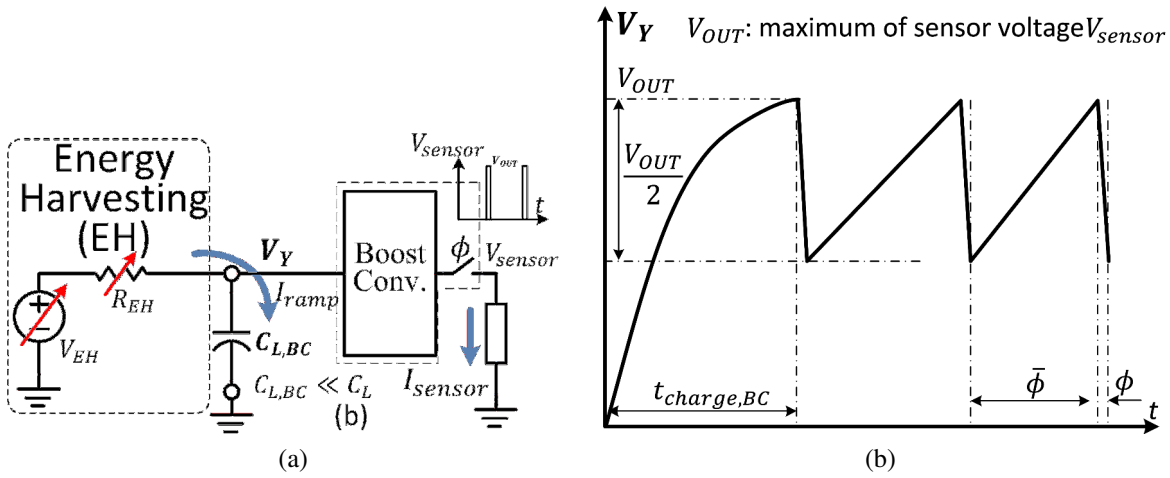


Figure 1.14: Using capacitor C_{LB} as a buffer capacitor and an intermediate boost converter: (a) circuit implementation and (b) charging-discharging effects on the ripple of the voltage of the capacitor V_Y.

is $V_{OUT}/2$. During discharging and assuming a 100% efficient intermediate converter, the energy balance between the input and output is given by:

$$V_{OUT} I_{sensor} \Delta t = \frac{1}{2} C_{L,BC} \left(V_{OUT}^2 - \left[\frac{V_{OUT}}{2} \right]^2 \right), \tag{1.10}$$

and the minimum capacitor $C_{L,BC}$ to be used can be derived as:

$$C_{L,BC}(\text{min}) = \frac{I_{sensor}}{(3/8)\,\text{x} V_{OUT}} \Delta t, \tag{1.11}$$

which is smaller than (1.6). Assuming an initial value of 0 voltage, the time to wait for charging is:

$$t_{charge,BC}(\text{min}) = \frac{C_L V_{OUT}}{I_{ramp}} \frac{1}{60} = \frac{8}{3} \frac{I_{sensor}}{I_{ramp}} \frac{\Delta t}{60}, \tag{1.12}$$

which is again smaller than (1.7) due to smaller capacitor used. This shows faster initialization time for this setup compared direct interaction between capacitor C_L and the load.

However, in the steady-state operation, the capacitor is charged from an initial value of $V_{OUT}/2$ and the time to wait is given by:

$$t_{charge,BCss}(\text{min}) = \frac{C_{L,BC}V_{OUT}}{2I_{ramp}}\frac{1}{60} = \frac{4}{3}\frac{I_{sensor}}{I_{ramp}}\frac{\Delta t}{60}, \tag{1.13}$$

which is the larger than (1.8) and the utilization of the capacitor $C_{L,BC}$ is given by:

$$\text{Utilization} = \frac{\frac{1}{2}C_{L,BC}\text{x}\frac{3}{4}V_{OUT}^2}{\frac{1}{2}C_{L,BC}V_{OUT}^2} = \frac{3}{4}, \tag{1.14}$$

where the actual factor $3/4$ is dependent on the boosting capability of the intermediate converter. Again, this analysis assumed 100% efficiency for the intermediate converter and no power overhead for its controller whiles its operation. If this operation has an efficiency of 50%, the required energy during discharging is doubled which will double the steady-state charging time $t_{charge,BCss}$ in (1.13). So, initialization versus steady-state operation is the trade-off between the two approaches. Table 1.3 summarizes these findings. Finally, the maximum voltage of both sensors is V_{OUT}, the output voltages of both sensors V_{sensor} are comparable (dc voltage around V_{OUT} with ripple), and the governing equations for both cases can be derived to demonstrate the aforementioned arguments. Moreover, in both cases, when the energy harvesting source is weaker, this translates to longer waiting times. The extreme case of no energy coming from the source will lead to infinite time

Table 1.3: Compare direct discharging with intermediate converter discharging.

	Direct capacitor	Intermediate converter
Charging from 0 V (initialization)	Longer	Smaller (by orders of magnitude)
Steady-state charging	Less charging time	More charging time
Efficiency of power delivery	Better	worse

of wait and during this time, leakage in capacitors will be taking effect, although leakage resistance in modern capacitors in the range of GΩ.

1.4 Wireless Power Transfer (WPT)

WPT is intended to replace the use of cords for different applications spanning from portable gadgets to high power electric vehicles. Moreover, most existing implanted applications used that technology to avoid unnecessary after-implantation surgeries. As shown in Fig. 1.15, a wall adapter (an external regulated rectifier) is connected between the ac outlet permanent source and the transmitter. Two questions arises: since the input is ac, why not to use that alternative current to drive the transmitter and the other, what type of transmitting element should we use? The frequency of ac outlet is $50-60$ Hz which is chosen for an efficient power-line transmission for high voltage operation. When that is needed to be transmitted for WPT, a very large transmitting element is needed for efficient transmission, as the dimensions of elements decreases with respect to the electrical length, the efficiency decreases. As a consequence, higher frequency is needed which is in the range of MHz. The other question is related to the type of transmission. As will be shown in Section 6, near-field inductive WPT with MHz frequency range is preferred due to efficiency and safety issues. This leads to the use of transmitting (and receiving) coils. In Fig. 1.15, a power amplifier, or more generally a dc to ac converter, is needed to drive the transmitting coil. The near-field transmission is dependent on linking the transmitted magnetic field to a receiving area, coil. This magnetostatic linkage transfers the electrical power efficiently to the different gadgets.

1.5 Goals and Objectives of the Dissertation

The objectives are a) to propose integrated circuits for RF energy harvesting, wireless power transfer and power management, b) to study the sensitivity of the RF energy harvesting integrated circuits and build mathematical models to describe that, c) to study the

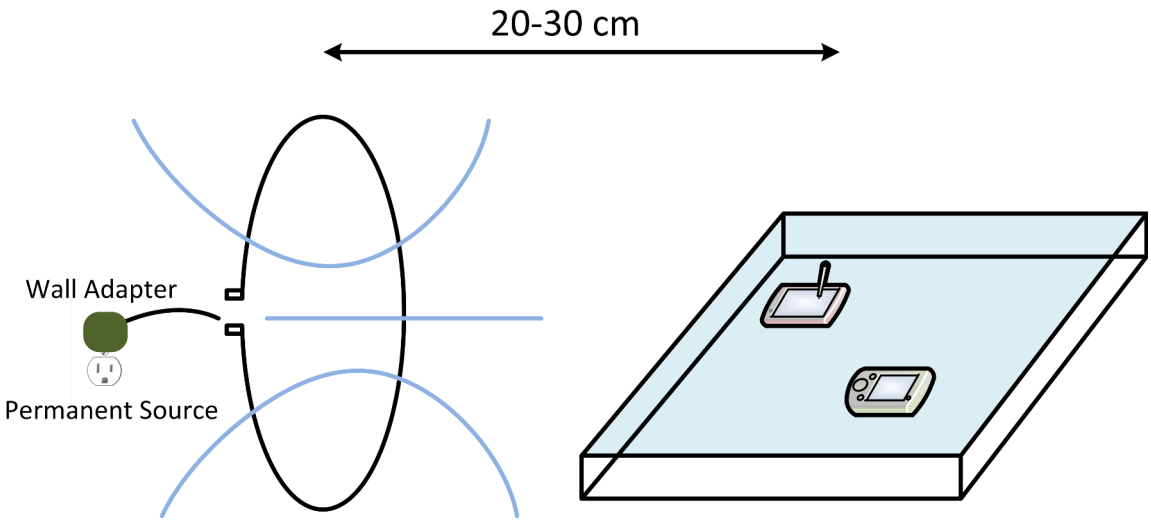


Figure 1.15: Wireless power transmitter to transfer power to different gadgets.

start-up issues of circuits at ultra-low power operation, d) to use ultra-low power circuits for power management, e) to analyze RF rectifiers as large signal circuits e) to propose self-sustainable architectures, investigate power-assisted solutions, and compare between them in terms of performance, f) to propose reconfigurable structures that are suitable for the variable nature of the both RF energy harvesting and wireless power transfer, g) to integrate and test the RF energy harvesting with wireless receivers, h) to propose a fully integrated watt-level wireless power transmitter through multi-level inverters operating in the MHz range suitable for emerging standards, i) to use high voltage supply to enhance the efficiency of the transmitter while taking care of the reliability of the integrated devices, and j) to propose a multiple input switched capacitor combiner suitable for ultra-low power energy harvesting sources with self-startup capability though the use of cross-coupling techniques. Fig. 1.16 summarizes the proposed designs.

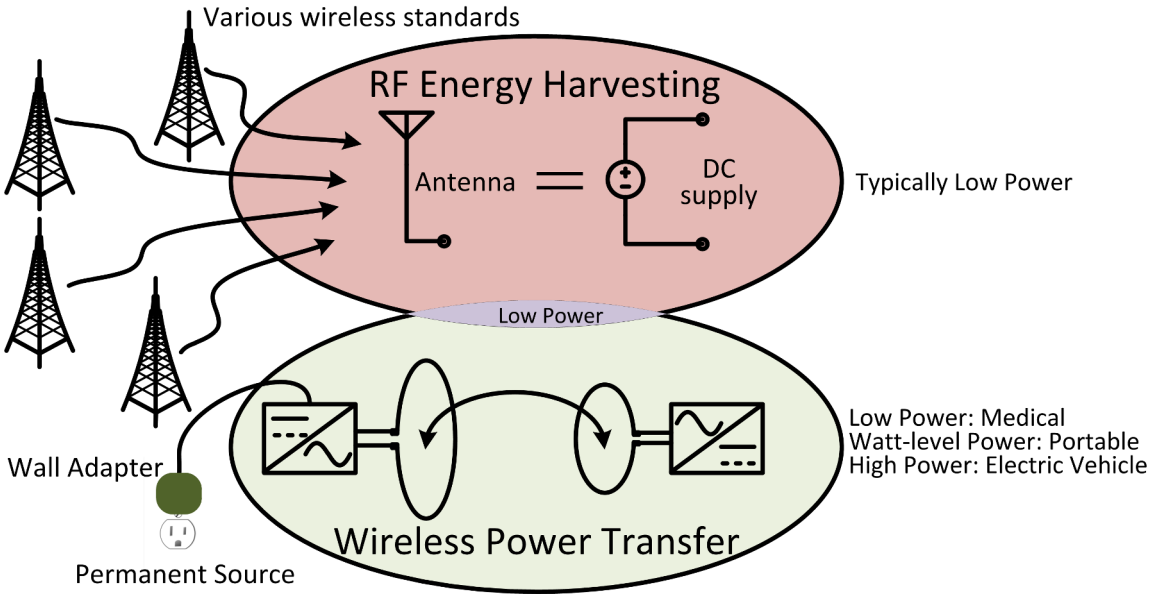


Figure 1.16: Proposed work.

1.6 Organization of the Dissertation

The dissertation contains seven sections, besides the introduction section and an appendix, organized as follows:

Section 2 is organized as follows: Section 2.1 gives a brief introduction about RF energy harvesting in the literature. Section 2.2 discusses the diode-connected MOS model used and will compare the model to a foundry supplied model and how the model can be used to predict the required voltage amplitude, at the input of the RF rectifier, for a specific required output. Also, the application of the analysis for multistage rectifiers is presented. Section 2.3 shows how the losses of a matching network can affect the sensitivity of the RF front end. Section 2.4 discusses the experimental results for the two designs. They share the same design of the RF rectifier. One of them uses an off-chip matching network and the other integrates an on-chip matching network. It is shown that the matching network has tremendous effect on the performance of the RF energy harvesting front end. It is

the main loss mechanism in the RF harvesting front ends. That is why the expressions of the matching network conversion should include specifically the loss (ordinary matching network design just assumes quality factors are large enough). The limited quality factor affects both the voltage gain as well as choosing the matching network values.

Section 3 is organized as follows: Section 3.2 describes the proposed RF energy harvesting system and the main building blocks where priority to the load demand, duty cycle control for low input powers to satisfy the load requirements except for limited intervals and the potential benefits of storing extra energy in the external capacitor through the secondary path. The control circuitry takes the decisions based on trying to keep the voltage limited at the output of the reconfigurable RF rectifier. Section 3.3 shows the circuit implementation for the main building blocks. The RF rectifier is presented and how modular the design is. The power management controller, incorporating digital control to control the main and secondary paths, is shown. The control scheme for the switches in the reconfigurable RF rectifier is presented along with required logic levels. The circuits of the voltage reference, tunable ring oscillator and the non-overlapping clock generation are discussed and how they can affect the design. Non-overlapping level-shifters are discussed and shown to mitigate the problem of clock overlapping and as a result, shoot through power loss is minimized while generating level-shifted non-overlapping clocks. Section 3.4 models the RF rectifier and the matching network, and shows the effect of the reconfiguration on the parameters of the RF front end. Furthermore, it discusses the RF rectifier and the matching network and shows the effect of the reconfiguration on the parameters of the RF front end. The dependences of the output delivered power and the input impedance of the rectifier on the input power and the output dc voltage (or the dc current) are derived. The classical diode equation is used where the generalization for level-m compensation is discussed to modify the obtained results and how they affect the location of the maximum point of power conversion efficiency (PCE). Section 4.5 shows the measurement results

for the RF energy harvesting systems. Finally, Section 2.5 discusses the conclusions.

Section 4 is organized as follows: Section 4.2 describes the proposed RF system architecture where a single antenna is proposed to capture the in-band and out-band signals. The former carries the actual data of the wireless receiver while the latter is scavenged through RF energy harvesting. Section 4.3 presents the proposed differential RF rectifier with integrated passives where a two-stage rectifier is used. The steady-state analysis of the differential RF rectifiers through the use of the nonlinear equations of the devices is shown. Output dc voltage for different loads, input impedance and power conversion efficiency (PCE) are derived. A comparison between cross-coupled and non-cross coupled devices is conducted. Section 4.4 presents the top level large signal simulations to characterize the interaction between the RF rectifier and the wireless receiver. Section 4.5 shows the experimental results for the proposed test chip. Finally, Section 4.6 discusses the conclusions.

Section 5 is organized as follows: Section 5.2 discuss the different antenna parameters such as antenna impedance, radiation pattern, directivity, gain, polarization, and bandwidth. Then, Section 5.3 shows the components of the RF energy harvesting system and possible implementation of each block. The design of the antenna is shown and the realization of the diodes in the RF rectifier is discussed. Section 5.4 shows the experimental results for the test chip. Section 5.5 discusses the conclusions.

Section 6 is organized as follows: Section 6.2 discuss the near field and far field wireless power transmission and how each system has different characteristics in terms of path loss, the transmitting/receiving elements, what is the boundary between the distances of the two systems, and the effect of different technologies on the performance. Section 6.3 introduces a thorough analysis to the inductive wireless power link as a resonant dc-dc converter. Section 6.4 discusses the optimization of Litz wire coils used in this work, how different models can lead to different results, and which EM simulators type should the

designer use. Section 6.5 introduces the different types of multi-level inverters and how the use of a multi-level inverter can give advantage in terms of device reliability and total harmonic distortion (THD). Different modulation schemes are discussed along with the most suitable for the diode-clamped inverters that will be used. Section 6.6 shows the implementation of the proposed integrated wireless power transmitter. Then, Sections 6.7 and 6.8 show the simulation results and the proposed test setup for the experimental results, respectively. Finally, Section 6.9 discusses the conclusions.

Section 7 is organized as follows: Section 7.2 shows the different power gain definitions and the relation to microwave amplifier design. The input matching, output matching, and intrinsic losses are three important parameters that affect the power flow through the power converter. Thus, different efficiency definitions are introduced. Then, Section 7.3 presents a proposed novel multiple-input self-startup switched capacitor circuit that can be used for energy harvesting. Different differential thyristor-based based tunable oscillators are used in the switched converter to generate non-overlapping clocks and they are powered from the input sources. Section 7.4 shows the experimental results for the proposed test chip. Finally, Section 7.5 discusses the conclusions.

Section 8 concludes the discussion about energy harvesting, wireless power transfer, and power management techniques with proposed plans for future work. Furthermore, the Appendix includes some of the derivations used in Section 3.

2. LOW INPUT POWER LEVEL CMOS RF ENERGY HARVESTING FRONT END[1]

2.1 Introduction

Energy harvesting is a renewable source of energy. This can be thought as a recycling process where energy is converted from one form (here, non-electrical) to another (here, electrical). The same holds true for RF, Solar, Thermoelectric, and Kinetic Energy Harvesting [15, 16, 17, 6, 5, 8, 18, 19, 20, 21, 22, 23, 24]. Although all communication transfer information from one location to another, their standards vary depending on the specifications of the transmitters and types of receivers used. Some of them have low transmitted energy and large area coverage requirements. Consequently, a highly sensitive receiver is needed (for example, GPS systems). On the other hand, others may have a higher transmitted power, but their coverage is limited to the area surrounding the transmitter such as WIFI, GSM, LTE, *etc*. The advantage of the latter systems is a low complexity power consumption of the used receiver. A main difference between wireless standards is the used digital modulation schemes and how this affects their capacity and bandwidth. The RF energy discussed previously can be a useful source when the energy harvesting device is used to capture that from different wireless standards. In this situation, the target is now the RF energy itself and the modulated information does not have any useful significance. The main objective of the energy harvesting system is to capture the RF time-varying energy and convert it to a dc energy and charge an output capacitor over time and/or deliver dc current to electrical loads. In the case of the charged capacitor, which is used in this work, it can provide different electrical circuits with dc voltage until the charges stored in the capacitor vanish. If the harvested dc energy is sufficient to operate the load circuits

[1]Part of this section is reprinted, with permission, from M. Abouzied and E. Sánchez-Sinencio, "Low-Input Power-Level CMOS RF Energy-Harvesting Front End," IEEE Trans. Microw. Theory Techn., vol. 63, no. 11, Nov. 2015. ©2015 IEEE.

and there is no need for power to operate the energy harvester itself, the energy harvesting system can replace the battery. But in some cases [10], there could be an intermediate stage where a battery and the energy harvesting system is a secondary source of dc energy. This is similar to the semi-passive radio-frequency identification (RFID) technology [25, 26]. Fig. 2.1 shows an RF energy harvesting system. The antenna is a sensor that acquires the Electromagnetic waves in the space and converts them into a time-varying signal. In order to maximize the transferred power from the antenna to the next RF block, a loss-less (ideally) matching network is needed to transform the impedance to the antenna impedance, which is usually 50 Ω (to be discussed later). The rectifier/charge pump circuit is responsible for the conversion of the ac to dc signal. There are many variations of this circuitry [15, 16, 6, 5, 8], but since the input voltage amplitude is usually small, an accumulating process is used to boost the value of the output dc voltage. That is why it may be called a charge pump where the clock input is the RF signal itself and the dc input is zero. RF energy harvesting is a challenging system since the harvested energy is small and the efficiency of the circuits degrades due to high frequency operation. This means that there is a required sensitivity at the input of the energy harvesting system. Below this limit, there is no energy obtained. From an analysis point of view, RF rectifiers are analyzed in [16, 27, 28]. [16] used the classical exponential diode equation to analyze that. [27, 28] used the MOS equation in sub-threshold for the analysis and this is the same starting point in the present work. The former took channel length modulation λ_{sub}, used waveform approximations to reach to compact equations and identified two operating regions of the devices used while the latter neglected λ_{sub} and made reasonable approximation to the MOS equation and that led to the classical exponential diode equation. From a design point of view, many references used various techniques to lower this minimum detectable signal. In [5], differential rectifiers were used but not clearly detailed (the matching network is not mentioned). In [8], threshold voltage cancellation for diodes

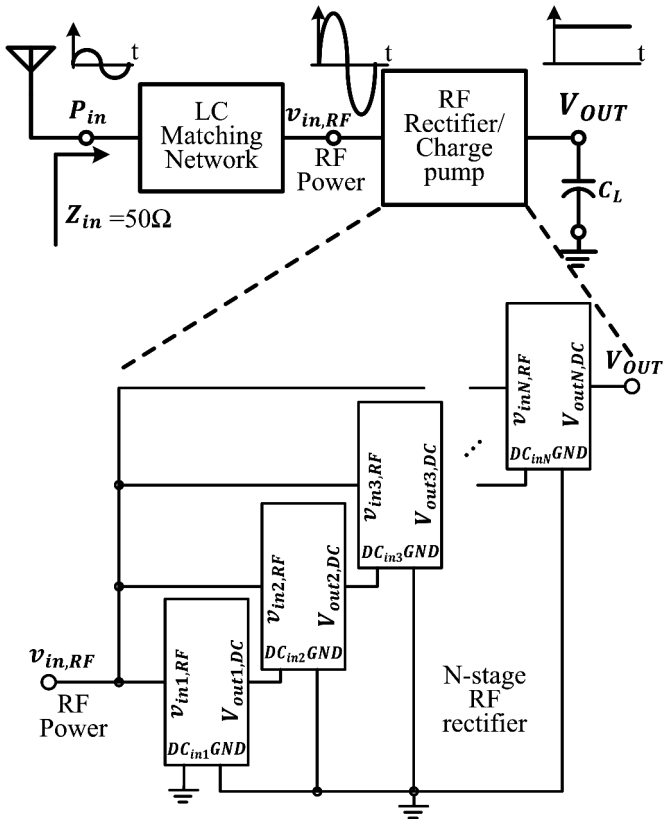


Figure 2.1: An RF Energy Harvesting rectifier preceded by a matching network.

was investigated. This technique used higher dc voltages from upcoming stages, a better CMOS technology resulted in a performance advantage. In [10], active threshold voltage cancellation for diodes was utilized. The main drawback was the overhead dc energy to assist the RF rectifier. The required energy, to start up the circuit, scales up with frequency, and this additional energy would limit the sensitivity of the RF harvesting system. In [9], an RFID system was discussed, which included an antenna and an RF harvester. Initially, a precharge phase was needed due to the use of the floating-gate technique. In [29], an antenna rectifier co-design was performed and an external control loop including a microcontroller was used which demands dc power to operate properly.

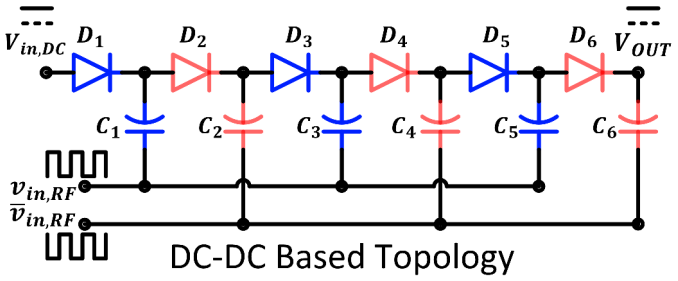
This Section 2 presents a steady state analysis of the RF front end including both the

RF rectifier and the lossy matching network. Topics will include the sensitivity of the RF energy harvesting front ends, the main loss mechanisms associated with the front ends and how they affect the minimum detectable power and the expected input impedance of the RF rectifier at the sensitivity limits. Exact equations governing the sensitivity are derived at this limit.

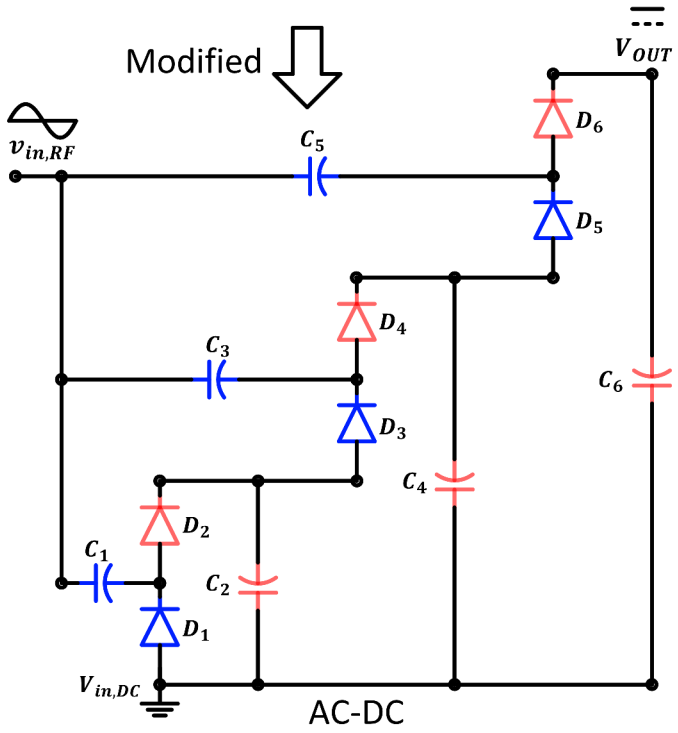
2.2 Analysis of the RF Rectifier

Ac to dc conversion and dc voltage accumulation can be obtained by using charge pumps. The charge pumps are commonly used for dc to dc converters and by the redefinition of inputs, it can be used for ac to dc conversion. The early used charge pump was Croft-Walton charge pump and Dickson modified it to reach a better charge pump suitable for integrated circuit applications [30]. This new structure helps to overcome the bottom plate capacitance of the capacitors (and more generally, the parasitic capacitance at the intermediate nodes) used in the Croft-Walton charge pump and this is the reason why this structure is used for the integrated circuit implementation in this work. Also, the use of more sophisticated versions of the charge pumps discussed previously lead to more parasitic capacitance at the intermediate nodes. Fig. 2.2 shows how a six-stage Dickson charge pump can be converted to a three-stage RF rectifier. The clock ϕ is the RF signal and it is ac coupled to each stage. The clock $\bar{\phi}$ is the RF ground from the antenna. Inside the rectifier, the dc output of each rectifier stage is dc coupled to the next stage. Fig. 2.3 shows how a six-stage Croft-Walton charge pump can be viewed as a three-stage RF rectifier. It should be noted that they share the same basic structure but the RF signal in Dickson charge pump is directly fed to each stage (the concept of stages will be explained later).

In this Section 2, the ideal diode clamper and half wave rectifier are discussed briefly, which will be used throughout the analysis. Then, a quantitative analysis of the RF rectifier, the governing equation of the diodes is applied to one of the RF rectifier stages. In

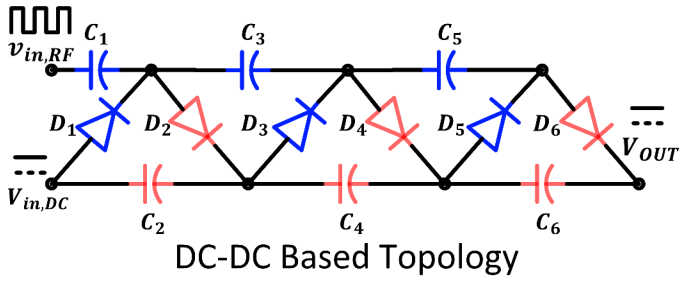


(a)

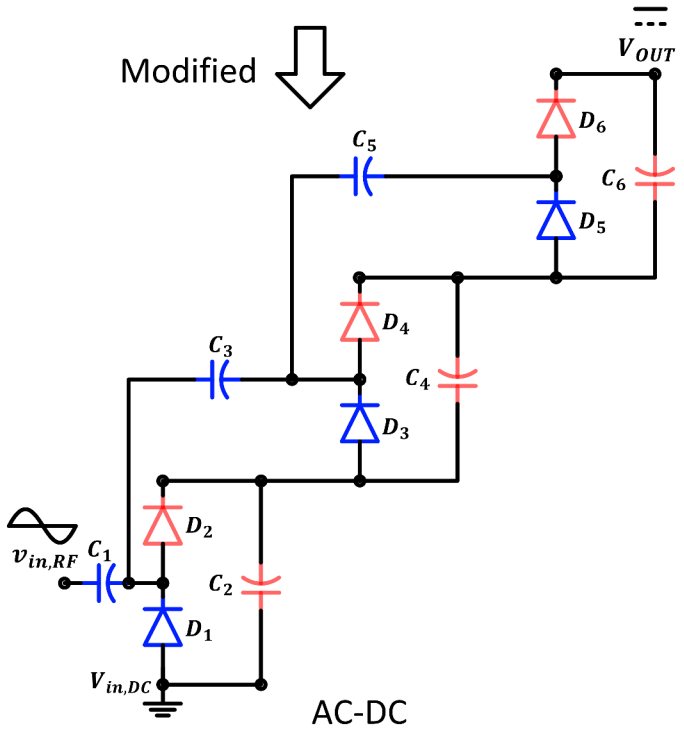


(b)

Figure 2.2: Three-stage RF rectifier: (a) six-stage Dickson charge pump and (b) a three-stage RF rectifier equivalent to (a).



(a)



(b)

Figure 2.3: Three-stage RF rectifier: (a) six-stage Croft Walton charge pump and (b) a three-stage RF rectifier equivalent to (a).

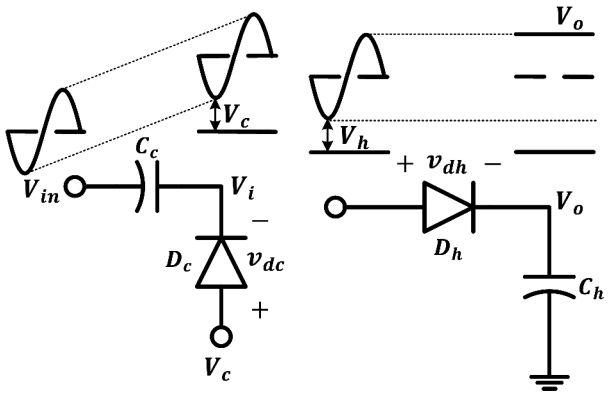
this analysis, the ripple at the output capacitor is neglected. This enabled a steady state solution of the RF rectifier stage. The sensitivity and input impedance of each stage are related to the physical parameters of the diodes. Finally, a generalization of the results for multistage design is discussed.

2.2.1 Diode Clamper and Half Wave Rectifier

Fig. 2.4a shows the diode clamper, which consists of a capacitor C_c and a diode D_c. The input V_{in} at the capacitor C_c is sinusoidal, and the positive terminal of the diode D_c is connected to a constant voltage V_c. The diode D_c will turn on if the voltage v_{dc}, across it, is above zero. Hence, the capacitor C_c starts to accumulate charges until the voltage v_{dc} is no longer below the zero voltage. Since the capacitor is a short circuit at RF frequencies, the output voltage V_i will be a shifted version of the input sinusoidal with a shift equal to the input amplitude plus the constant voltage V_c.

The half wave rectifier is also shown in Fig. 2.4b where a capacitor C_h and a diode D_h are used. In general, the input V_i at the diode D_h is sinusoidal with a constant voltage component V_h and the capacitor C_h can filter the ripples at the output. Again, the diode D_h will turn on if the voltage v_{dh}, across it, attempts to go above zero. As a result, the capacitor C_h starts to accumulate charges until the voltage v_{dh} is no longer below the zero voltage for any value of the input voltage. As a result, the output voltage V_o will be the maximum of the input voltage which is the input amplitude plus the constant voltage V_h neglecting the ripples.

In reality, the dc shift is always less than the ideal value due to the current that follows to the next stages.



(a) (b)

Figure 2.4: Basic building blocks: (a) voltage clamper and (b) half wave rectifier.

2.2.2 Diode-Connected MOS Equation-Based Model

To find the input output governing equations of the diode-connected transistor, the starting point is the equation of weak-inversion NMOS [31]:

$$I_{DS} = \mu_n C_{ox} \phi_t^2 \frac{W}{L} \exp\left(\frac{(V_{GS} - V_T)}{n\phi_t}\right) \left\{1 - \exp\left(-\frac{V_{DS}}{\phi_t}\right)\right\}, \tag{2.1}$$

where I_{DS} is the current through the channel of the transistor with its positive direction from drain to source, μ_n is the mobility of the carriers, C_{ox} is the capacitance of the oxide layer per unit area, W is the channel width, L is the channel length, ϕ_t is the thermal voltage ($\phi_t = KT/q$) and equals to 26 mV at room temperature, n is the slope factor, V_T is the threshold voltage, V_{GS} is the gate-source voltage or the control voltage of the channel and V_{DS} is the drain-source voltage or the voltage across the channel with the direction of the current. In deep weak-inversion [31], the slope factor n is related to the sub-threshold slope S by:

$$S = 2.3\phi_t n. \tag{2.2}$$

Typical values of S range from 70 to 100 mV/decade (this gives a range from 1.17 to 1.67 for n) at room temperature, and are directly proportional to temperature.

With the constraint of $V_G = V_D$ for the diode-connected transistor, the equation becomes:

$$I_{DS} = \mu_n C_{ox} \phi_t^2 \exp\left(\frac{-V_T}{n\phi_t}\right) \left(\frac{W}{L}\right) \left\{\exp\left(\frac{V_{DS}}{n\phi_t}\right) - \exp\left(-\frac{(n-1)\,V_{DS}}{n\phi_t}\right)\right\}. \quad (2.3)$$

The term $\mu_n C_{ox} \phi_t^2 \exp\left(-V_T/n\phi_t\right)$ is process dependent and will be called I_B, current factor. μ_n (and μ_p for PMOS) varies from die-to-die, the term is strongly (exponentially) dependent on temperature due to the thermal voltage ϕ_t, V_T is dependent on the process as well as the source-to-body voltage and n , ϕ_t, C_{ox} are constants for a specific process. Also, V_{DS} can be written V_d such that the equation can be used for the PMOS as well where the source and drain are interchanged but the V_d is from the positive to the negative sides of the diode-connected transistor:

$$I_d = I_B \left(\frac{W}{L}\right) \left\{\exp\left(\frac{V_d}{n\phi_t}\right) - \exp\left(-\frac{(n-1)\,V_d}{n\phi_t}\right)\right\}. \quad (2.4)$$

I_B and n are process dependent and can be extracted. For the 0.18 µm technology, nominal temperature and typical corner, Fig. 2.5 shows the simulated current-voltage relationship for the actual PMOS transistor foundry-supplied model and the proposed equation-based model. It also shows the diode-connected PMOS and its equivalent diode device. The absolute value of the current is plotted. The actual sign of the current follows the sign of the diode voltage. As the voltage gets higher, the results do not match since the transistor leaves the weak-inversion region and enters the strong-inversion region where the governing equations are completely different. However, the sensitivity analysis shows the

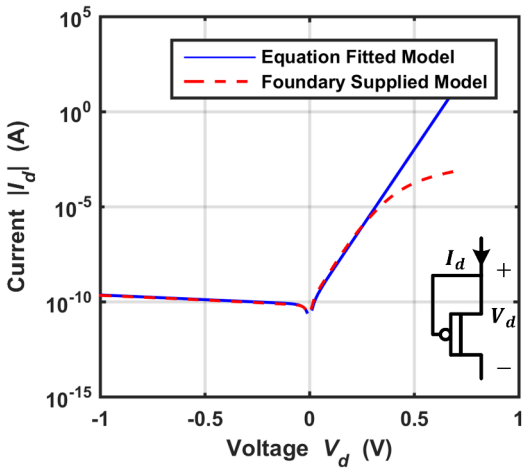


Figure 2.5: Comparison between the used equation fitted model (blue-solid) and the real diode-connected PMOS model supplied by the foundry (red-dashed). Magnitude of the current of the device is plotted versus voltage across the device.

amplitude to be small and indicates that transistor is operating in the weak-inversion.

2.2.3 Modified Bessel Function $\mathrm{I_m}\,(x)$

Modified Bessel Function $\mathrm{I_m}\,(x)$ is discussed in [32],

$$e^{\pm x\cos(\omega_o t)} = \mathrm{I_o}\,(\pm x) + 2\sum_{m=1}^{\infty} \mathrm{I_m}\,(\pm x)\cos\,(m\omega_o t)\,, \tag{2.5}$$

which corresponds to a constant dc value and harmonics of the original sinusoidal waveform in the exponent. One important symmetry property of this function that relates the negative argument to the positive argument:

$$\mathrm{I_m}\,(-x) = (-1)^m\,\mathrm{I_m}\,(x)\,. \tag{2.6}$$

Starting from (2.15), the RF input current i_{RF} can be expressed as:

$$i_{RF} = 2I_B \left(\frac{W}{L}\right) \exp\left(-\frac{A}{n\phi_t}\right) \left\{\sinh\left(A_I \cos\left(\omega_o t\right)\right) + \exp\left(\frac{A}{\phi_t}\right) \sinh\left(\frac{(n-1)}{n\phi_t} A_I \cos\left(\omega_o t\right)\right)\right\}, \quad (2.7)$$

which is an odd function in the function $\cos(\omega_o t)$, $i.e.$ it contains only odd harmonics.

2.2.4 Minimum Amplitude Sensitivity and Input Impedance of the RF Rectifier

The rectifier stage consists of two diode-connected MOS transistors and two capacitors as shown in Fig. 2.6a. For simplicity, the diode-connected transistors will be called diodes. The first capacitor C_c - diode D_c pair is a diode clamper which assures that the minimum voltage at its output (v_{inter}) is around the dc voltage at the positive node of the diode DC_{in}, effectively, achieving a positive dc shift to the input sinusoidal voltage $v_{in,RF}$. This is followed by the other diode D_h - capacitor C_h pair working as a half wave rectifier. The output is a dc voltage $V_{out,DC}$ with some ripples that are minimized by the filtering of the output capacitor and ignored in this analysis. So, the intermediate node v_{inter} is a dc+ac voltage while the output node $V_{out,DC}$ is dc voltage.

Before getting into the analysis details, the expected waveforms are discussed and shown in Fig. 2.6b. The input ac signal $v_{in,RF}$ is assumed to be $A_{RF} \cos(\omega_o t)$ where A_{RF} is the amplitude of the sinusoidal wave and ω_o is the frequency. The input capacitor C_c can pass the ac sinusoidal signal and blocks the dc signal. The voltage v_{inter} is permitted to go below the voltage DC_{in}. During this interval, the current i_{dc} of the diode D_c is supplied to the load and shown in blue. Also, the voltage v_{inter} can go higher than the output dc voltage $V_{out,DC}$ in order to supply current i_{dh} to the load during this interval. During the intervals of supplying current from both diodes, the voltage waveform v_{inter} is expected to deviate from sinusoidal which gives rise to harmonics and is shown in red (exaggerated to

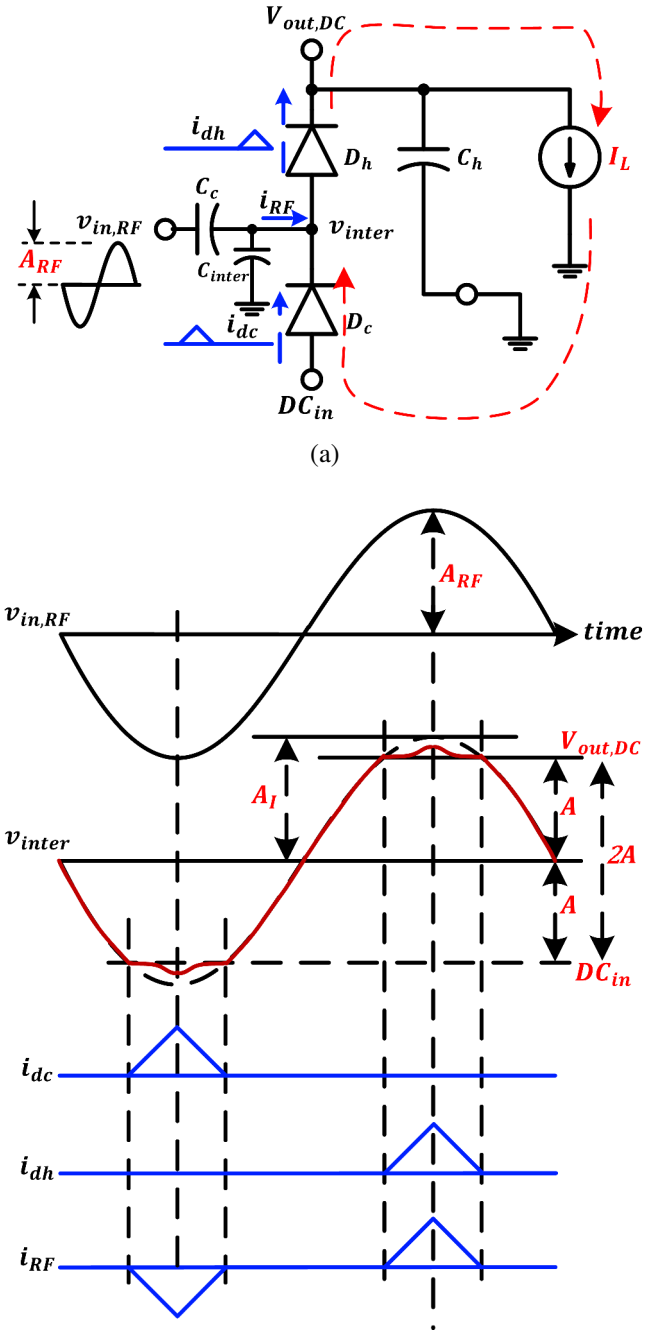


Figure 2.6: Analysis of one stage of the RF rectifier: (a) implementation with voltage and current illustrations and (b) waveforms for various signals.

show the effect although in practice, this deviation is small). In this Section 2, it is assumed that these are neglected and the voltage waveform v_{inter} is composed of a dc value plus a pure sinusoidal waveform.

The dc output current path is shown as a dotted red arrow in Fig. 2.6a. The dc value is only delivered to the next stage, and the harmonics are filtered out by the output capacitor C_h. Since the capacitor C_c - diode D_c pair form a voltage clamper, the voltage v_{inter} has the form of:

$$v_{inter} = DC_{in} + A + A_I \cos(\omega_o t), \tag{2.8}$$

where A is the dc voltage shift associated with diode clamper stage as well as the half wave rectifier stage, and A_I is assumed to be the sinusoidal amplitude at the intermediate node. Since this signal is periodic, it can be cosine or sine. Here, cosine is used assuming that in the steady state, diode D_h is acting first then diode D_c.

A_I is obtained by a capacitive divider between the ac coupling capacitor C_c and the parasitic capacitance associated with the intermediate node C_{inter}:

$$A_I = \frac{C_c}{C_c + C_{inter}} A_{RF}. \tag{2.9}$$

C_{inter} is composed of the diodes parasitic capacitance, wire capacitance and bottom plate capacitance. Since diode D_h - capacitor C_h pair acts as a half wave rectifier, the dc output voltage $V_{out,DC}$ is:

$$V_{out,DC} = 2A + DC_{in}. \tag{2.10}$$

The output voltage is twice the value of A. This output voltage is composed of the input dc voltage plus twice a dc shift voltage A associated with the two diodes D_c and D_h used. Due to symmetry, both intervals should be the same (neglecting body effect). The difference

between the negative peak voltage and zero is the same as the difference between the positive peak voltage and output voltage and the voltage across diode D_c is the same as the voltage across diode D_h.

At the intervals where the diodes are conducting current, the current is filtered and the dc component is passed to the load while the ac component contributes to the input RF current i_{RF}. The input RF current waveform has an odd symmetry and reach in harmonics. So, either diode D_c or diode D_h can be analyzed. Diode D_c is arbitrarily chosen. For diode D_c, the voltage across the diode terminal v_d can be expressed as:

$$v_d = -\left(A + A_I \cos\left(\omega_o t\right)\right). \tag{2.11}$$

So, using (2.4), and using the modified Bessel functions $\mathrm{I_m}\left(x\right)$ (see Section 2.2.3) to find the dc term of the $\exp\left(\pm x \cos\left(\omega_o t\right)\right)$ function, the load dc current I_L can be expressed as:

$$I_L = I_B \left(\frac{W}{L}\right) \exp\left(\frac{-A}{n\phi_t}\right) \left\{ \mathrm{I_o}\left(\frac{A_I}{n\phi_t}\right) - \exp\left(\frac{A}{\phi_t}\right) \mathrm{I_o}\left(\frac{\left(n-1\right)A_I}{n\phi_t}\right) \right\}. \tag{2.12}$$

The minimum amplitude will correspond to the condition of no load current (I_L=0), i.e., the input should be sufficient to overcome the losses in the rectifier. At no load current,

$$\mathrm{I_o}\left(\frac{A_I}{n\phi_t}\right) = \exp\left(\frac{A}{\phi_t}\right) \mathrm{I_o}\left(\frac{\left(n-1\right)A_I}{n\phi_t}\right). \tag{2.13}$$

The amplitude voltage A_I required for each dc voltage value A is governed by (2.13) and plotted in Fig. 2.7. It is important to note that the sensitivity results subject to a required dc shift A is independent of the transistor dimensions if C_c used is large enough to reduce the effect of the capacitive divider on A_I (see (2.9)) where A_I is reduced to approximately A_{RF}. At the beginning, A is almost zero as A_I increases and after A_I

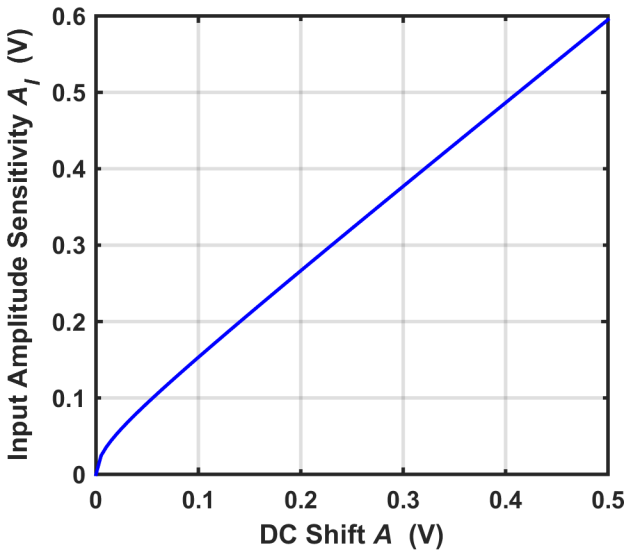


Figure 2.7: Amplitude voltage at the intermediate node v_{inter} required to obtain a specific dc shift at load-free conditions.

reaches a certain value, A starts to increase. The more input amplitude A_I is available, the more output dc voltage A (this was stated previously by [28]) but after that limit is reached. This limit is important to be known to show how low the output voltage can be which in turn put specifications on the possible low voltage circuitry that can be potentially powered by the rectifier. Moreover, the slope factor n is the only process parameter that affects the relationship between A and A_I. The above condition changes slightly when the channel length modulation is taken into consideration as shown in Section 2.2.5. As a conclusion, from a design perspective, if the output dc voltage A of the stage is required to be of a certain value, the RF amplitude A_I is known which affects the minimum input amplitude.

In reality, the intermediate capacitance C_{inter} is dependent on the size of the diode used as well as the value of the capacitance C_c. As a result, A_I deviates a bit from A_{RF} according to (2.9). This can make the choices of these parameters affect a little bit the

sensitivity. For the most optimal sensitivity, the iterative approach should be adapted from this initial step. The complete expression, after substitution from (2.9), would be:

$$\mathrm{I_o}\left(\frac{C_c}{C_c+C_{inter}}\frac{A_{RF}}{n\phi_t}\right)=\exp\left(\frac{A}{\phi_t}\right)\ \mathrm{I_o}\left(\frac{C_c}{C_c+C_{inter}}\frac{(n-1)\,A_{RF}}{n\phi_t}\right). \tag{2.14}$$

The input impedance is a parallel RC equivalent circuit. To reach these expressions, we began by the RF input current (using (2.4) and applying KCL at the intermediate node):

$$i_{RF}=\mathbf{I_d}(-A+A_I\cos(\omega_o t))-\mathbf{I_d}(-A-A_I\cos(\omega_o t)), \tag{2.15}$$

which is an odd function in the variable $\cos(\omega_o t)$ as shown in Section 2.2.3. That suggests that there is no even harmonics in this single ended structure. But in the presence of channel length modulation, there exists even harmonics as proved in Section 2.2.5.

Using the expansion of $\mathrm{I_m}(x)$ in Section 2.2.3 and taking only the fundamental component leads to the input impedance. The real part of the input conductance is given by:

$$G_{stage}=\frac{4I_B\left(\frac{W}{L}\right)}{A_I}\exp\left(\frac{-A}{n\phi_t}\right)\left\{\mathrm{I_1}\left(\frac{A_I}{n\phi_t}\right)+\exp\left(\frac{A}{\phi_t}\right)\ \mathrm{I_1}\left(\frac{(n-1)\,A_I}{n\phi_t}\right)\right\}. \tag{2.16}$$

where A_I is assumed to be equal to A_{RF}. In other words, the ac coupling capacitors C_c are assumed to be much larger than the parasitic capacitance at the v_{inter} node.

The input impedance changes for different conditions so, the use of a tunable matching network can track these changes to obtain better matching. When channel length modulation is taken into account, extra terms appear as shown in Section 2.2.5.

The imaginary part of the input conductance is capacitive and the capacitance is due to the parasitic capacitance due to bottom plate capacitance C_{bottom} of C_c, and equivalent

gate capacitance C_B of the diodes used. The gate capacitance $C_B \approx C_{ox}WL$. Thus,

$$C_{stage} \approx C_{inter} \approx 2C_B + C_{bottom} \approx 2C_{ox}WL + C_{bottom} \approx 2C_{ox}WL. \tag{2.17}$$

The capacitance C_c is carefully chosen such that it is not too large to reduce C_{bottom} and not too small to avoid reducing A_I with respect to A_{RF}. The quality factor of the RC parallel equivalent circuit is given by $Q_{stage} = \omega_o C_{stage}/G_{stage}$. The intermediate capacitance C_{inter} can create an RF path for the RF current harmonics to go through in case of a high impedance (for the harmonics) condition imposed by the matching network; hence, only the fundamental component will remain.

The lower the length of the transistors, the lower the quality factor. The equivalent parallel resistance of the rectifier is much larger than the source impedance, which is assumed to be $50\ \Omega$. Alternatively, the input series equivalent impedance is almost capacitive with a very small resistive part.

2.2.5 Take the Effect of Lambda Into Account

Again starting from (2.4) and adding the dependency term of channel length modulation as [27]:

$$I_d = I_B \left(\frac{W}{L}\right)(1 + \lambda_{sub} V_d)\left\{\exp\left(\frac{V_d}{n\phi_t}\right) - \exp\left(-\frac{(n-1)\,V_d}{n\phi_t}\right)\right\}, \tag{2.18}$$

where λ_{sub} is the sub-threshold region channel-length modulation parameter.

For diode D_c in Fig. 2.6a, the voltage across the diode terminal v_d is expressed as (2.11). Again, using the modified Bessel functions $\mathrm{I_m}\,(x)$(see Section 2.2.3) to find the dc term of the $\exp\left(\pm x\cos\left(\omega_o t\right)\right)$ function, the load dc current I_L can be expressed as:

$$I_L = I_B \left(\frac{W}{L}\right) \left(1 - \lambda_{sub} A + \lambda_{sub} A_I \cos\left(\omega_o t\right)\right) \exp\left(\frac{-A}{n\phi_t}\right) \left\{ \mathrm{I_o}\left(\frac{A_I}{n\phi_t}\right) - \exp\left(\frac{A}{\phi_t}\right) \mathrm{I_o}\left(\frac{(n-1)\,A_I}{n\phi_t}\right) \right\}. \quad (2.19)$$

The minimum amplitude is at no load current (I_L=0) which leads to the same expression in (2.13):

$$\left(1 - \lambda_{sub} A\right) \left\{ \mathrm{I_o}\left(\frac{A_I}{n\phi_t}\right) - \exp\left(\frac{A}{\phi_t}\right) \mathrm{I_o}\left(\frac{(n-1)\,A_I}{n\phi_t}\right) \right\} = \lambda_{sub} A_I \left\{ \mathrm{I_1}\left(\frac{A_I}{n\phi_t}\right) - \exp\left(\frac{A}{\phi_t}\right) \mathrm{I_1}\left(\frac{(n-1)\,A_I}{n\phi_t}\right) \right\}. \quad (2.20)$$

To find the input impedance, the RF input current i_{RF} can be expressed as shown below:

$$i_{RF} = 2I_B \left(\frac{W}{L}\right) \exp\left(-\frac{A}{n\phi_t}\right) \{ \left(1 - \lambda_{sub} A + \lambda_{sub} A_I \cos\left(\omega_o t\right)\right) \sinh\left(A_I \cos\left(\omega_o t\right)\right) + \exp\left(\frac{A}{\phi_t}\right) \left(1 - \lambda_{sub} A + \lambda_{sub} A_I \cos\left(\omega_o t\right)\right) \sinh\left(\frac{(n-1)}{n\phi_t} A_I \cos\left(\omega_o t\right)\right) \}, \quad (2.21)$$

which is a mix between odd and even functions in the variable $\cos\left(\omega_o t\right)$ (unlike the case where the channel length modulation was neglected in the analysis here). The fundamental component leads to the real part of the input conductance which is given by:

$$G_{stage} = \frac{4I_B\left(\frac{W}{L}\right)}{A_I}\left(1-\lambda_{sub}A\right)\exp\left(\frac{-A}{n\phi_t}\right)\left\{\mathrm{I}_1\left(\frac{A_I}{n\phi_t}\right)\right.$$
$$\left. + \exp\left(\frac{A}{\phi_t}\right)\ \mathrm{I}_1\left(\frac{\left(n-1\right)A_I}{n\phi_t}\right)\right\}. \quad (2.22)$$

2.2.6 Multistage Analysis

The dc output voltage $V_{out,dc}$ of each stage is dc coupled to the voltage clamper of the next stage. If the number of stages is N, this will boost the dc output voltage V_{out}:

$$V_{OUT} = 2NA. \quad (2.23)$$

It should be noted that as N increases, the output voltage V_{OUT} increases. With the use of (2.13), V_{OUT} will be almost zero for values of RF input amplitude below a certain limit and as N increases, this effect will be more significant (practically, although this limit is small in Fig. 2.7 but when it multiplied by the value of N, its value is higher).

The output node of each stage can be considered an ac ground. This leads to the fact that the stages can be considered in parallel where the rectifier is represented by a parallel combination of a conductance $G_{rec}(1/R_{rec})$ and a capacitance C_{rec}, which have the form:

$$G_{rec} = \sum_N G_{stage} = NG_{stage}, \quad (2.24)$$

$$C_{rec} = \sum_N C_{stage} = NC_{stage}. \quad (2.25)$$

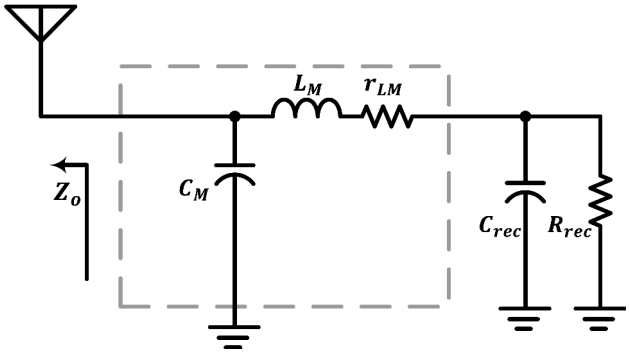
2.3 Analysis of the Matching Network

The antenna impedance is usually 50 Ω, which is a compromise between cable loss and power handling [33]. The matching network should provide the complex conjugate of the antenna impedance for maximum power transfer from the antenna to the front end. The use of a series inductor in the matching network will act as a high impedance and the current harmonics will pass through the rectifier capacitance C_{rec} which will be filtered by this act. As a consequence, the fundamental current and voltage will only appear at the terminals of the rectifier. Also, at the low power levels, antenna impedance is much less than the rectifier's input impedance i.e. the transformation ratio is high and therefore the matching network is narrow-band. So, the fundamental input impedance is taken into account in the following calculations and two matching networks will be discussed. Since the value of the input impedance changes as shown in (2.16), this affects the matching elements. The choice of the values of the matching elements should change according to the input power levels as well as the output voltage levels.

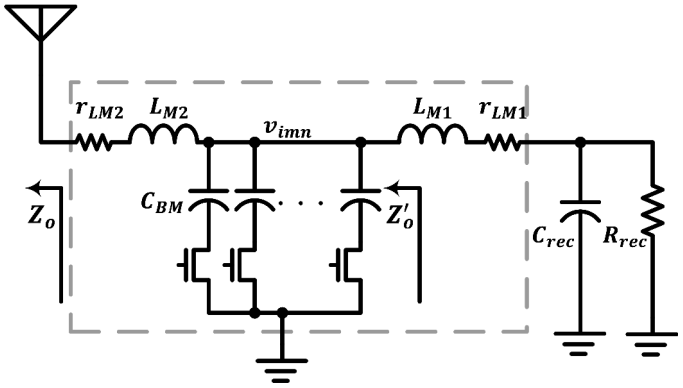
2.3.1 Off-Chip Matching Network

The rectifier was previously shown to be a parallel RC equivalent circuit with high impedance values. The off-chip components should be placed as close as possible to the chip in order to minimize the losses. The width of the wires should be the lowered in order to lessen the radiation losses of the PCB and the parasitic capacitance at the input node of the rectifier. This is important to get the highest voltage gain as will be seen shortly. The off-chip components will enable a 50 Ω input impedance. After this, a 50 Ω transmission line is designed.

The off-chip matching network is shown in Fig. 2.8a with two matching elements. The loss resistance r_{LM} is used to reflect both PCB loss at this node and the inductor L_M



(a)



(b)

Figure 2.8: Matching network between the antenna sensor and the RF rectifier: (a) off-chip and (b) on-chip tunable implementations.

losses. The series equivalent circuit of the rectifier equivalent impedance is composed of:

$$R_{rec,series} = \frac{1}{G_{rec}\left(1+Q_{rec}^2\right)} \approx \frac{1}{G_{rec}Q_{rec}^2}, \tag{2.26}$$

$$C_{rec,series} = C_{rec}\left(1+1/Q_{rec}^2\right) \approx C_{rec}. \tag{2.27}$$

At the minimum sensitivity conditions, the values of the $R_{rec,series}$ is too small to be ignored in this analysis and $C_{rec,series}$ is approximately C_{rec}. The values of inductor L_M and capacitance C_M can be calculated as can be seen in Section 2.3.3, (2.36),

$$C_M = \frac{1}{\omega_o Z_o}\sqrt{\frac{Z_o}{r_{LM}}-1} \approx \frac{1}{\omega_o\sqrt{Z_o r_{LM}}}, \tag{2.28}$$

$$L_M = C_M\, r_{LM} Z_o + \frac{1}{\omega_o^2 C_{rec}} \approx \frac{1}{\omega_o}\left\{\sqrt{Z_o r_{LM}} + \frac{1}{\omega_o C_{rec}}\right\}. \tag{2.29}$$

The voltage gain of the matching network after substitution of L_M and C_M in Section 2.3.3, (2.39),

$$A_{v,offchip} = \frac{1}{2\sqrt{Z_o r_{LM}}\,\omega_o C_{rec}}. \tag{2.30}$$

The higher the value of C_{rec}, the lower the voltage gain obtained. The same applies for the losses. Fig. 2.9, solid, shows how the matching network transforms the impedance using the Smith chart.

2.3.2 On-Chip Matching Network

The proposed matching network is shown in Fig. 2.8b. It is an LC ladder where the load impedance is gradually down-converted to the source impedance which is assumed to be 50 Ω. The more elements, especially inductors, added, the worse is the matching net-

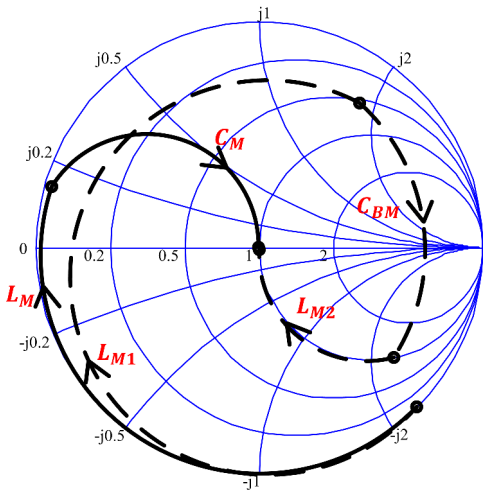


Figure 2.9: Matching network impedance transformation on smith chart: off-chip implementation (solid) and on-chip tunable implementation (dashed).

work's transmission coefficient and the higher the matching network loss. In this design, two LC ladder stages are used with two inductors and one tunable capacitor (to tune the operating frequency). The reason for the use of this structure is that the capacitance of the first stage does already exists in the rectifier equivalent impedance and a programmable intermediate capacitance is used. This can lead to programmable rectifier front ends over different frequencies. Moreover, the value of a one series inductor would be large and separating this into two inductors is beneficial.

The matching network should boost the antenna impedance in two stages. The first part consists of the rectifier capacitance C_{rec}, inductance L_{M1} with associated loss resistance r_{LM1} and a fraction of the capacitance C_{BM}, which is called C_1. This is similar to the off-chip matching network discussed previously with the exception of matching to $Z_o^{'}$, which is the intermediate impedance at the node v_{imn}.

The second part which consists of the remainder of the capacitance C_{BM} which is called C_2 ($C_1 + C_2 = C_{BM}$) and the inductance L_{M2} with associated loss resistance r_{LM2}. This part should boost the antenna impedance Z_o to its local load impedance $Z_o^{'}$. The

quality factor of the parallel combination of C_2 and $Z_o^{'}$ is:

$$Q_c = \omega_o C_2 Z_o^{'}. \tag{2.31}$$

The value of the capacitance C_2 can be calculated from:

$$C_2 = \frac{1}{\omega_o Z_o^{'}} \sqrt{\frac{Z_o^{'}}{Z_o} - 1}. \tag{2.32}$$

where the quality factor of the second section is $\sqrt{\frac{Z_o^{'}}{Z_o} - 1}$ [34] and r_{LM2} is neglected since the impedance level now is small (50 Ω). The value of inductance L_{M2} is chosen to tune out the capacitance C_2 and is given by:

$$L_{M2} = \frac{1}{\omega_o^2 C_2}. \tag{2.33}$$

The input impedance is due to the losses and process dependent. Also, the addition of the on-chip components increases the losses of the matching network, which eventually makes the sensitivity worse. But at the same time, this offers a compact integrated solution that is cheap and easier to tune.

The voltage gain of the last section can be done like the first section in Section 2.3.3. As a result, the voltage gain of the matching network would be the multiplication of the gain of both sections and given by:

$$A_{v,onchip} = \frac{1}{2\sqrt{r_{LM1}}\,\omega_o C_{rec}} \cdot \sqrt{\frac{1}{Z_o} - \frac{1}{Z_o^{'}}}. \tag{2.34}$$

The loss of the matching network can be considered the minimum input power that can produce the desired output voltage after the rectifier. Fig. 2.9, dashed, shows how the matching network transforms the impedance using the Smith chart. A two-step network is realized with the addition of each passive element (here, the capacitance C_{BM} is consid-

ered one element).

2.3.3 Derivation of the Input Admittance Y_{in}

The input admittance Y_{in} for the off-chip design is:

$$Y_{in} = j\omega C_M + \frac{j\omega C_{rec}}{1 - \omega^2 L_M C_{rec} + j\omega C_{rec} r_{LM}}, \tag{2.35}$$

$$Y_{in} = j\omega \left\{ \frac{C_M + C_{rec} - \omega^2 L_M C_M C_{rec} + j\omega C_M C_{rec} r_L}{1 - \omega^2 L_M C_{rec} + j\omega C_{rec} r_{LM}} \right\} = \frac{1}{Z_o}, \tag{2.36}$$

where the input impedance is expected to be real and equal to Z_o for matching purposes. Equating both the real and the imaginary parts gives the two sets of equations that govern C_M (2.28) and L_M (2.29).

Assuming a 50 Ω source resistance, the voltage at the antenna interface should be 1/2 of the source voltage resulting in a total voltage gain of:

$$A_{v,complex} = \frac{1}{2} \frac{1}{1 - \omega^2 L_M C_{rec} + j\omega C_{rec} r_{LM}}, \tag{2.37}$$

which should be related to the value of Z_o as:

$$A_{v,complex} = \frac{1/Z_o - j\omega C_M}{j\omega C_{rec}}. \tag{2.38}$$

The magnitude of the voltage gain is:

$$A_v = \frac{1}{2} \frac{\sqrt{(1/Z_o)^2 + \omega^2 C_M^2}}{\omega^2 C_{rec}^2}. \tag{2.39}$$

Substitution by the value of C_M from (2.28), (2.30) can now be obtained.

2.4 Experimental Results

Two RF energy harvesting front ends were designed and fabricated on CMOS 0.18 µm technology. The first features an off-chip matching network with two matching elements and a rectifier while the second is fully integrated. The die photo is shown in Fig. 2.10. The rectifier takes a 180x90 µm^2 die area and two off-chip high quality components which takes extra 7.28 mm^2 PCB area. The fully integrated on-chip design has a 820x450 µm^2 die area including two matching inductors and a digitally tunable capacitance. Table 2.1 shows the estimated values from simulations for both off-chip and on-chip matching networks. The rectifier input capacitance is estimated to be 200 fF without the pads and metal capacitance.

The test setup is shown in Fig. 2.11. The RF energy harvesting front end is used to charge a ceramic capacitor of a 2.2 nF value. The rectifier consists of six stages. For an output voltage of 1 V, the required dc voltage shift A should be 83.33 mV (1 V/ (6x2)). Using Fig. 2.7, about amplitude A_{RF} of 150 mV is required at the rectifier input. The sensitivity for the off-chip matching design is -27.3 dBm which means that the off-chip matching network voltage gain is around 10 (V/V). For the on-chip matching design, the voltage gain is less by a factor of 2, i.e. the off-chip inductors have a quality factor four times better than the on-chip ones, which leads to a sensitivity of -21.7 dBm. The charging time for an output voltage of 1 V is 1.3 seconds for both of the designs. The charging time is defined as the time to charge a capacitor until 63% (1-e^{-1})) of its final value. Fig. 2.12

Table 2.1: Values of the matching elements used for illustration.

	L_M	r_{LM}	C_{LM}	L_{M1}	r_{LM1}	L_{M2}	r_{LM2}	C_{BM}
Value	47 nH	4 Ω	1.2 PF	73 nH	36 Ω	5 nH	3.5 Ω	0 to 4 pF

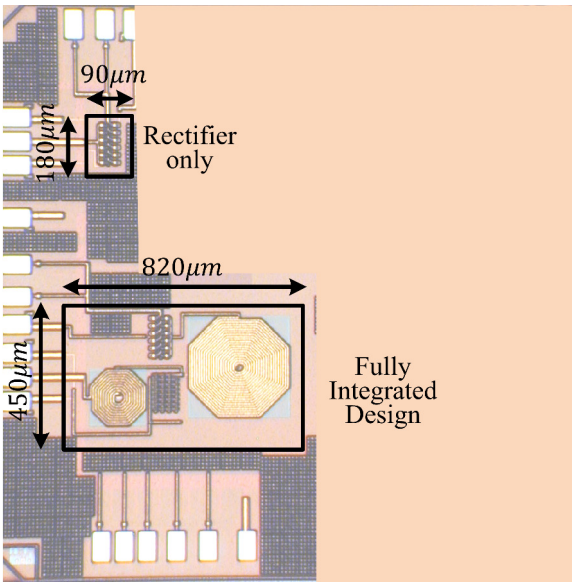


Figure 2.10: Micrograph of the CMOS RF energy harvesting front end.

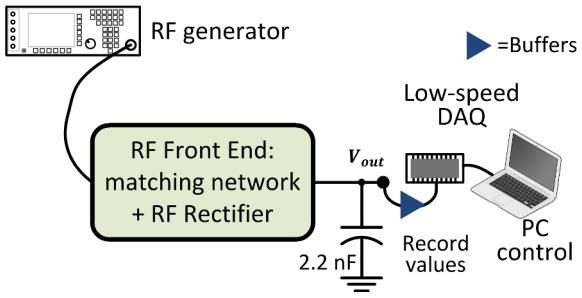


Figure 2.11: Test setup for the RF front end.

shows the output voltage V_{OUT} versus the input power levels. When the voltage amplitude at the rectifier input A_{RF} is below a certain limit, the dc voltage shift is almost zero. As the input increases beyond this limit, the output voltage starts to increase rapidly as explained previously. Here, the values of the elements of the matching network are not tuned for different input power levels which affect the input impedance as shown in (2.16).

According to the values of the off-chip matching elements, the frequency of the input impedance matching is obtained. Fig. 2.13a shows the frequency response of the off-chip implementation. It is matched around 781-798 MHz. It is noted that the reflection coefficient is almost about -12 dB which shows poor matching which suggests that the conjugate match and the power (or source-line) match points, which takes into account the devices physical limits into account, are not the same. It is like the load-pull in power amplifiers where the output conjugate match is different from the output power (load-line) match, which takes into account the physical limits of the devices used, are not the same [35]. This technique in the RF rectifier can be referred as source-pull.

Fig. 2.13b shows how the matching frequency can be tuned over a wide range from 850-1200 MHz. The tuning is done by a 5-bit digital capacitor bank.

The difference between the two designs is the value of the amplitude A_{RF} that is obtained from different matching networks and the main reason for the poor sensitivity of the on-chip matching version is the poor quality factors [34] of the on-chip inductors compared to off-chip ones which benefit from special low-loss processes. This leads to more loss in the matching network. Also, it should be noted that a wide-band matching is obtained in the case of on-chip matching which lead potentially to more harvested energy in the case of wide-band signals.

Table 2.2 shows how the design is compared to other designs in the literature. The sensitivity is reported as the available power at the antenna interface whether it is a $50\ \Omega$ interface or other impedance. Newer technologies have smaller lengths which results in

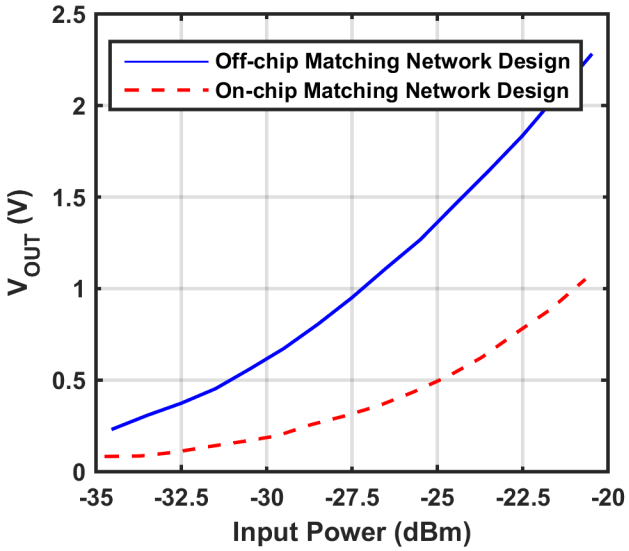
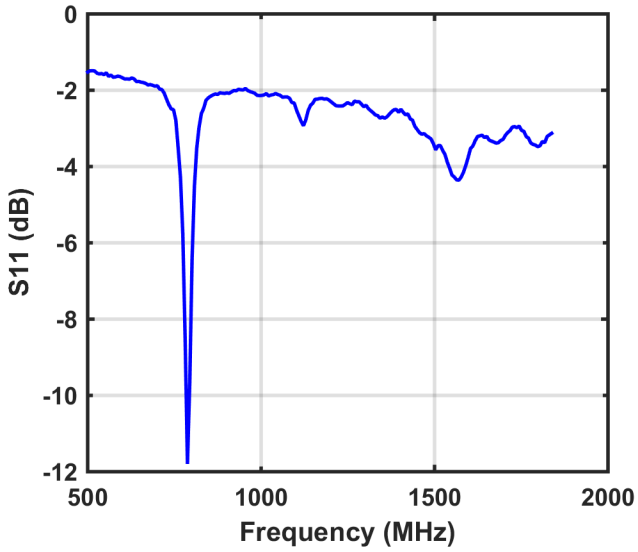


Figure 2.12: The output voltage versus input power at load-free conditions and charging a 2.2 nF capacitor.

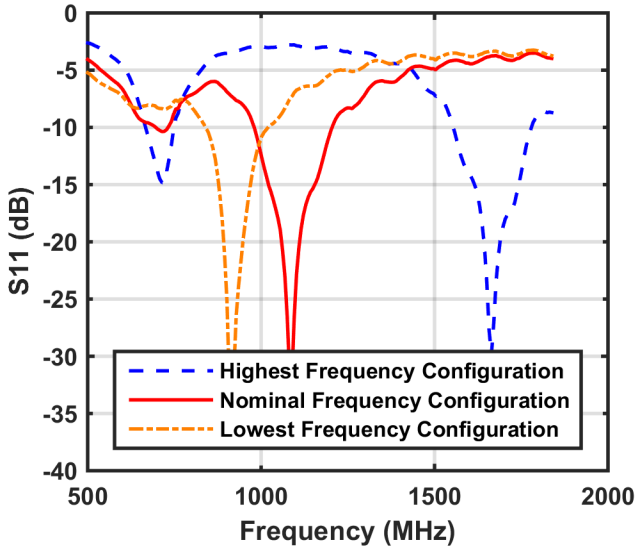
smaller device capacitance (i.e., C_{inter} see (2.9)), the device capacitance is quadratically proportional to the length. As a consequence, the rectifier input capacitance C_{rec} is lower which leads to higher voltage gain in the matching network as shown in (2.30) and (2.34). This justifies the performance advantage of newer technologies compared to old ones. Differential designs can offer a 3 dB improvement since the voltage gain A_v of the matching network is inversely proportional to loss in the inductors as shown in (2.30) and (2.34) and the differential inductors have higher quality factor due to the elimination of the substrate loss effect in the differential excitation [34].

2.5 Summary

A comparative study between an on-chip matching network and an off-chip matching network was conducted. This Section 2 also examined the sensitivity effect of each design strategy. The RF rectifier at the sensitivity limit was analyzed and the input-output relationship was quantified. The input impedance of the RF rectifier proved to be mainly



(a)



(b)

Figure 2.13: Reflection coefficient of the proposed RF energy harvesting front end at load-free conditions: (a) off-chip and (b) on-chip tunable implementations.

Table 2.2: Comparison between the proposed RF system and other works.

	Kotani [5]	Papotto [6]	Umeda [14]	Ho [8]		Le [17]	Stoopman [18]	This work	
								on chip matching	off chip matching
Technology	0.18 µm	**90 nm**	0.3 µm	0.13 µm		0.25 µm	90 nm	**180 nm**	**180 nm**
Input method	External antenna+ matching	External 50Ω interface	Probing	External antenna+ matching		External not 50 Ω antenna	External not 50Ω antenna	External 50Ω interface	External antenna+ matching
Die area	n.a.	0.1900 mm²	0.6400 mm² *	0.03 mm² ***	0.3 mm² ***	0.4000 mm²	0.0290 mm²	0.3690 mm²	0.0162 mm²
Requirements	Deep n-well	Deep n-well	Auxiliary Battery	n.a.	**LVT**	External pre-charge	Control Loop (dc power)	-	-
Architecture	Differential	Single-ended	Single ended	Single ended		Single-ended	Differential	Single ended	Single ended
Operating frequency	953 MHz	915 MHz	950 MHz	915 MHz		906 MHz	868 MHz	850 MHz	798 MHz
Sensitivity	n.a.	**-22.44 dBm Vout = 1 V**	-14 dBm ** ,Vout = 1.5 V	-22.6 dBm	**-32.1 dBm**	-22.6 dBm ,Vout = 2 V	-27 dBm ,Vout = 1 V	**-21.7 dBm ,Vout = 1 V**	**-27.3 dBm ,Vout = 1 V**

*: including PAD ring. **: reported for a load current of 0.4 µA. ***: estimated.

capacitive. It has been confirmed that the on-chip matching network offers a flexibility of tuning as well as integration for a more robust design. On the other hand, the off-chip matching network gave a better sensitivity along with higher cost due to bulky off-chip matching elements.

This work shows that better matching elements will lead to the success of RF energy harvesting to harvest from very low levels of the incoming signals. Also, it shows how the integrated CMOS RF energy harvesting systems can be analyzed and the limits of the system.

3. A FULLY INTEGRATED RECONFIGURABLE SELF-STARTUP RF ENERGY HARVESTING SYSTEM WITH STORAGE CAPABILITY[1]

3.1 Introduction

Developing a green Internet of Things (IoT) technology based on harvesting energy [2, 36] from naturally available sources is one of the current research trends that avoids the use of external batteries and/or connection to a wired permanent power source. However, this technology is not yet mature enough for commercial use. Among the energy harvesting sources, RF energy harvesting is a promising renewable energy source with the prime advantages of flexibility and portability with respect to other sources. The system consists of a receiving antenna and an RF rectifier to convert the RF energy to dc energy. The dc energy can be used by resistive demand loads or stored for later use in capacitors and/or rechargeable batteries. Power management is needed to control the energy flow mandates of a self-startup feature that can provide the control circuits with the needed dc power without any power overhead from external sources. The needed dc load power defines the sensitivity of the RF harvesting system, and it is lower when only one capacitive load (open circuit) is charged. The RF energy is reported to have the lowest average power density [3]. Moreover, for a specific frequency band, the RF power varies dynamically according to three parameters: the change of transmitted power, the distance between the transmitter and the receiver, and the RF wireless link.

In order to tackle the variable nature of the input power, [37] proposed a dual-mode reconfigurable RF rectifier to widen the operating power range. The reported sensitivity was obtained for open circuit loads with no control circuits. From a top level point of view,

[1]Part of this section is reprinted, with permission, from M. A. Abouzied, K. Ravichandran, and E. Sánchez-Sinencio, "A Fully Integrated Reconfigurable Self-Startup RF Energy-Harvesting System With Storage Capability," IEEE J. of Solid-State Circuits, vol. PP, no. 99, Jan. 2017. ©2017 IEEE.

[38, 39, 40] describe harvesting systems in which the power management is incorporated and only resistive loads are supported by the RF energy harvesting front ends. In [38], an off-chip matching network and a differential RF single stage rectifier with a cascaded boost converter are used. The harvested power is delivered to a resistive load, and the boost converter presents an adaptive resistive load for the rectifier. In [39], RF harvesting was used to kick-start both the control and the boost converter for thermoelectric and solar energy harvesting. Even though the RF energy harvesting does not provide a demand load with dc power, it provides power to the control of the chip in the vicinity of other sources. In [40], RF harvesting is incorporated to provide the control circuits with the needed dc power. This enables the thermoelectric harvesting to operate at lower voltages with higher power conversion efficiency (PCE).

Therefore, for variable input power, a reconfigurable system architecture is important to accommodate the different RF power conditions, while the extra harvested energy can be stored in external storage elements. For the RF energy harvesting systems, full integration and self-startup are key attributes.In this work, an RF energy harvesting system is proposed and the contributions of this work are as follows: 1) a fully integrated system with an RF matching network, RF rectifier and power management/control circuitry, 2) a self-startup operation while minimizing the dc power overhead from the controller with $66-157$ nA current consumption, 3) a reconfigurable system to increase the available output power with the different input power levels with an RF rectifier with a modular design for a general number of stages N, while using all sub-blocks at the same time; specifically, the implementation of one-two-four-eight-stage configurations, 4) a proposed hardware solution to deliver the harvested power to different paths, such that a demand resistive load with duty cycle capability and a storage capacitor for extra power are simultaneously supported with priority to the resistive load, 5) proposed non-overlapping input/output level shifters to minimize the shoot-through power loss, and 6) and 8) a math-

ematical modeling for the operation of low-input power and high-input power rectifiers. The sensitivity of the total system is -14.8 dBm at a 1 V dc output.

In this work, an RF energy harvesting system is proposed where all required components are incorporated: RF matching network, RF rectifier and power management/control circuitry. The system is self-startup and harvests the dc power requirements of the controller. Moreover, it delivers the harvested power to a demand resistive load as well as a storage capacitor. This makes the system a hybrid green solution [36]. The priority is given to the main path: demand resistive load but in the case of excess available energy, the extra energy is stored in the external capacitor which is a secondary path for the energy flow. In the conditions of low input power and the load is demanding high current, the system adapts itself to deliver the required current in bursts where duty cycle control is used. This can be considered as a hardware solution and the decision is made according to the power management unit. With the last two attributes, the proposed system takes into account the variable nature of the energy harvesting paradigm and it has an impact on the processing capability of the IoT node. The proposed RF rectifier is reconfigurable with modular design for general N number of stages. In addition, it incorporates level-1 compensation for threshold voltage compensation [11].

3.2 Description of the RF Energy Harvesting System

The proposed system is shown in Fig. 3.1. It integrates the RF circuits, the controllers and the power management. The RF energy is received by an off-chip antenna tuned at the band of interest, which is 915 MHz. The antenna converts the electromagnetic energy, which propagates through the space, into electric energy. For maximum power transfer from the antenna, an LC matching network is inserted between the antenna and an RF reconfigurable rectifier. The RF reconfigurable rectifier is an ac to dc converter, which can be reconfigured to enhance the overall system efficiency as a function of the input

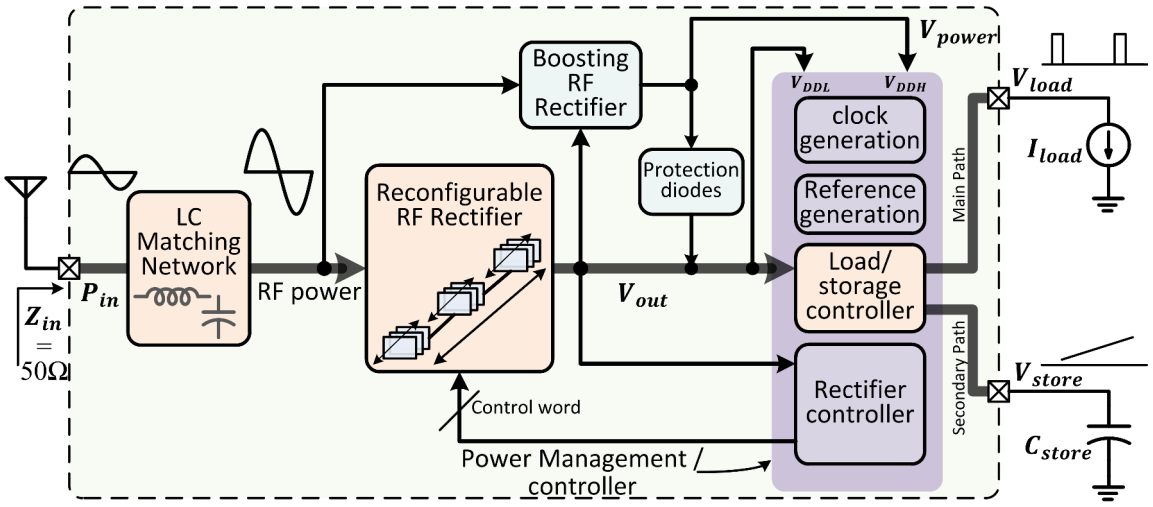


Figure 3.1: Reconfigurable RF energy harvesting system level with power management controller.

power. The nominal output voltage V_{out} is used for dc energy delivery to the main load I_{load} and the storage capacitor C_{store} for the extra power through the main and secondary paths, respectively. Moreover, V_{out} acts as a low supply V_{DDL} for the power management/controller block. An auxiliary boosting rectifier is used to generate a voltage V_{power} higher than the nominal voltage V_{out}. The voltage V_{power} is the voltage V_{DDH} for the power management/controller block and is used for high voltage control. Protection diodes are used between the voltage V_{power} and the voltage V_{out} to limit the maximum value of V_{power} without affecting the reliability of the devices. The power management/controller has four main ultra-low power blocks: the clock generation, the voltage reference generation, the load/storage controller, and the rectifier controller. The clock generation is used by all digital logic circuits. The reference generation is used to generate a constant voltage V_{BG} that is robust with variation in supply voltage, temperature and process. This is the only analog block contributing to the overall static power. The load/storage controller is responsible for delivering the dc energy to both the load I_{load} and the storage capacitor C_{store}. It has latched comparators as well as digital logic to take the appropriate decisions to control the

system. Lastly, depending on the estimation of the open circuit value of the output voltage V_{out}, the rectifier controller sends a binary control word to the RF reconfigurable rectifier in order to choose the state of the rectifier (number of stages) yielding the desired output voltage. The flow of extra power is limited by the secondary path maximum extraction capability which suggests that multiple secondary paths could be used in the future for handling larger input power.

In the next sections, the reconfigurable RF rectifier is presented along with illustrations on how to generalize for N number of stages while using all sub-blocks. Then, the energy delivery through the main and secondary paths is discussed.

3.2.1 Reconfigurable RF Rectifier

The reconfigurable rectifier is shown in Fig. 3.2 where the number of sub-blocks N is kept constant for all different configurations. The typical configuration consists of N number of stages in a series as shown in Fig. 3.2a. Each stage/sub-block takes a sinusoidal input v_{RF}, rectifies it to a dc output voltage, and places it in series with the output voltage DC_{in} of the previous stage. Thus, the final output voltage V_{out} is proportional to N. The first stage is connected to the reference ground and all stages are connected to the RF input v_{RF}. As the input amplitude of v_{RF} increases, the required number of stages can be lowered to maintain the same output voltage V_{out}, while increasing the supported maximum output current. This last property means that the diodes/switches or the stage sizing should be larger. If $N/2$ number of stages in series and two sub-blocks in parallel are used, as shown in Fig. 3.2b, the stages are rearranged, such that the sizing of each stage is doubled, compared to the typical configuration in Fig. 3.2a. The higher the input amplitude of v_{RF}, the fewer stages appear in series, and the more sub-blocks appear in parallel, the larger each stage becomes. This can increase the available output power as will be shown in the measurements. Fig. 3.2c and Fig. 3.2d show the case where two stages and one stage are

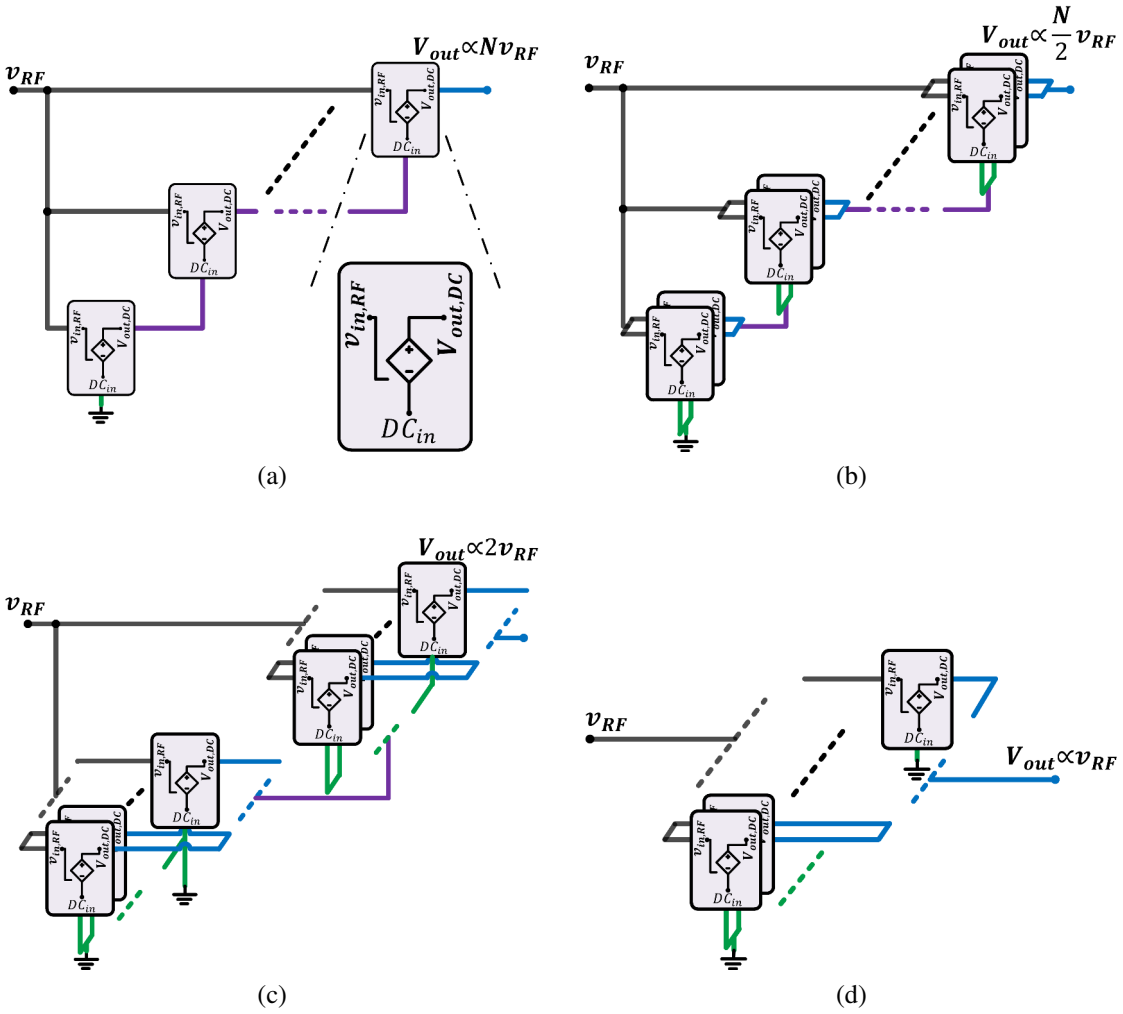


Figure 3.2: Conceptual reconfigurable RF rectifier with total number of sub-blocks N: (a) N number of stages in series, (b) $N/2$ number of stages in series with 2 parallel sub-blocks for each, (c) 2 stages in series with $N/2$ parallel sub-blocks for each, and (d) 1 stage with N parallel sub-blocks for each.

obtained with the reconfiguration of the same rectifier, respectively.

The proposed scheme reconfigures the number of stages of the RF rectifier while using all sub-blocks that are already connected to the RF port. Additionally, as shown in Section 3.3, the reconfiguration can be done on the dc side of the RF rectifier to avoid the losses on the RF side. In general, using N number of sub-blocks, the number of configurations is up to floor $\{log_2(N)\} + 1$ where floor $\{\}$ is the integer of the argument. The preferred choice of N is from the geometric sequence $\{1, 2, 4, 8, 16, ...\}$[2]. The circuit of the reconfigurable RF rectifier is shown in Section 3.3.

3.2.2 Load/Storage Control Scheme

The reconfigurable RF rectifier, as shown in Fig. 3.2, is represented by its Thevenin equivalent circuit: an open circuit voltage source V_{th} and a series resistance R_{th}. The energy flow from the rectifier to the main load demand R_L and the remaining power to charge the storage capacitor C_{store} is controlled through the main and the secondary paths, respectively. Fig. 3.3 shows how the two power flow paths interact. For maximum power transfer between the rectifier and the subsequent blocks, assume the desired output voltage from the rectifier is V_{OUT} equal $V_{dc,desired}$:

$$R_{PM} = R_{th}, \tag{3.1}$$

$$V_{th} = NV_{th,stage} = 2V_{dc,desired}, \tag{3.2}$$

where R_{PM} is the parallel input resistance of the subsequent blocks and $V_{th,stage}$ is the Thevenin voltage of any stage. The V_{th} can be estimated for an open circuit condition and

[2]In order to get the minimum transition between the minimum number of stage configurations and the next configuration, a base-2 log is used which results in a transition from 1 to 2. If a base-3 log was used, this transition would have been from 1 to 3 and N would have been preferably chosen from the geometric series $\{1, 3, 9, ...\}$.

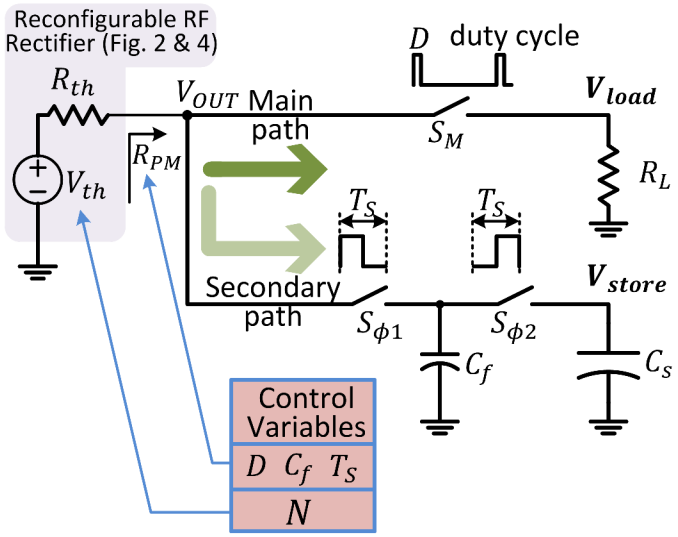


Figure 3.3: The scheme used to control the power flow to the load demand and the storage capacitor.

used to control the number of stages of the RF rectifier.

Now, we consider how to control the value of R_{PM}. The main path always has the higher priority to deliver energy to the resistive load. In the case of extra energy, the secondary path can take the remaining energy, while conditions (3.1) and (3.2) are satisfied. The first situation is when the available energy from the RF rectifier is less than the load demands, and the ratio of R_L/R_{th} is less than one, where the load demand is characterized by a specific R_L. In order to increase the equivalent input resistance R_{PM}, the duty cycle control scheme is utilized to satisfy the $V_{dc,desired}$ and the load demand simultaneously with a duty cycle less than 100%. The second situation occurs when there is more available energy than the load demands and the ratio of R_L/R_{th} is greater than one; hence, the secondary path is activated to satisfy (3.1). One possible implementation of the secondary path is shown in Fig. 3.3. The secondary path charges the capacitor C_f for half of the period, and for the other half, the charge of the capacitor C_f is dumped to the storage capacitor C_{store}. Thus, using this scheme, the parallel input resistance can be expressed as:

$$R_{PM} = \frac{R_L}{D} /\!\!/ R_{second} = \frac{R_L}{D} /\!\!/ \frac{T_s}{C_f}, \tag{3.3}$$

where R_{second} is the equivalent input resistance of the secondary path, D is the duty cycle from 0% to 100% and $/\!\!/$ indicates the parallel equivalent resistance. For the specific implementation of the secondary path, the switched capacitor circuit [41] has an input resistance R_{second} that is inversely proportional to the capacitance value C_f and the operating frequency f_s (proportional to period T_s) of the two phases, ϕ_1 and ϕ_2. Therefore, these signals are used to tune R_{second}. Finally, in the proposed architecture, there is no specific relationship between the frequencies of the signals, $S_{\phi 1}$ ($S_{\phi 2}$) and S_M. The circuit implementation of the control circuit may impose some relationship between both as will be mentioned in the next section.

3.3 Circuit Implementation of the Proposed System

Fig. 3.4 shows the proposed reconfigurable RF front end. The LC matching network consists of two stages with digitally tunable capacitors to support different bands. The reconfigurable RF rectifier provides the dc energy to the load (resistive) and capacitive storage. As shown, an auxiliary boosting rectifier generates a second dc voltage V_{power}. Thus, there are two supplies: a nominal output voltage $V_{DDL} = V_{out}$ and a higher voltage $V_{DDH} = V_{power}$. Protection diodes are used between V_{power} and V_{out} in order to prevent the voltage difference from going beyond a certain limit to comply with the reliability of the devices and provide the extra current to the load so as not to waste it. There is a trade-off in the design of the stack of protection diodes: the more diodes used, the less effect on low voltage differences at the output (and this will affect the voltage difference of the boosting RF rectifier at the low voltage range, which is proportional to the open circuit voltage, as will be shown), but higher protection voltage is imposed (in the order of the number of diodes x 0.7 V). For the current design, only two diodes are used for extra

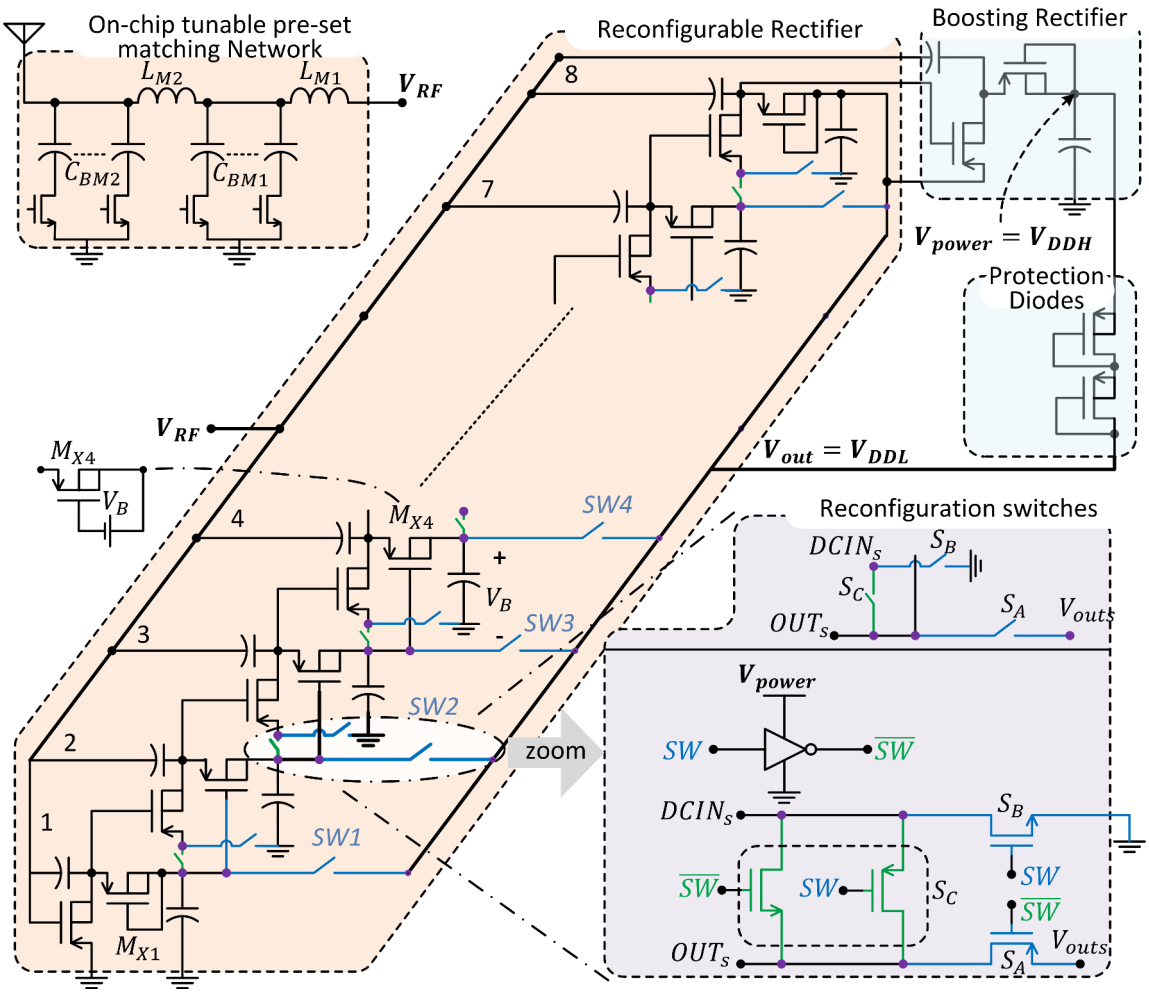


Figure 3.4: Reconfigurable eight-stage level-one compensated RF rectifier and cascaded one stage with limiting/protection diodes.

protection of the devices. A reconfigurable eight-stage (extendable to more, if needed) RF rectifier is utilized. PMOS devices are used for compatibility with standard CMOS technology. The nature of the voltages of each stage is: ac with no dc shift at the RF input side, an ac superimposed on a 1X dc shift at the intermediate node, and 2X shifted dc with no ac at the output node. Moreover, level-one compensation [11] is incorporated. In the conventional diode-connected realization of diodes, the gate and the drain are tied together as in [42] and device M_{X1} in Fig. 3.4. Introducing a positive (negative) voltage difference between these two nodes for NMOS (PMOS) device can mitigate the threshold voltage constraint of the devices. In order to realize this floating voltage V_B, as shown in Fig. 3.4, the connection between the gate of the NMOS (PMOS, for example M_{X4}) device in the current stage and the drain of the similar NMOS (PMOS) device in the next (previous) stage is used. Hence, the value of V_B is the dc shift from each stage to the next. The connection should be between nodes of the same voltage nature. If the connection is taken from m-stages away from the current stage, this is called level-m compensation [11].

The reconfiguration switches are also shown in the lower right side of Fig. 3.4 where an SW signal controls the state of each sub-block either in series or in parallel. Each switch network consists of three switches: PMOS switch S_A, NMOS switch S_B, and a transmission gate S_C. This scheme reconfigures the number of stages of the RF rectifier while using all sub-blocks that are already connected to the RF port. Moreover, it is implemented completely on the dc side of the RF rectifier where the reconfiguration switches are not affecting the parasitic capacitance on the RF side. Since the switches are on the dc side, the conduction loss is dominant and the switching loss is expected to be small. The on-resistance R_{on} is inversely proportional to theV_{GS} of the switch. However, the current flow I_{load} is small, and therefore, the conduction loss is $I_{load}^2 R_{on}$, and can be made small. As the input power increases, the value of R_{on} decreases quickly with the increase of V_{power} where the conduction loss is once again small. Unlike [43] where stages are

skipped (which is only acceptable for low frequency operation); here, all existing sub-blocks are used in an efficient way. This way, the available output power from the RF rectifier is increased.

Fig. 3.5 shows the power management block, which is part of Fig. 3.1, except for the controller of the RF rectifier, which will be discussed in the section of implementation. It consists of a clock generation circuit, a voltage reference circuit [44], and the load/storage controller. V_{DDL} is connected to the reference generation blocks, all the digital circuitry, and the latched comparators, while V_{DDH} is connected to the reference generation block and the level shifters (LS1, LS2, and LS3). The level shifters (LS1 and LS2) are used to control the switches in both the reconfigurable RF rectifier and the main and secondary paths of the dc energy delivery to I_{load} and C_{store}, respectively. The proposed non-overlapping level shifter (LS3) to shift the clock signals will be discussed. The main path has latched comparators as well as digital logic to reconfigure the system for different input power levels. The secondary path transfers the remaining power to C_{store} through a tunable capacitor C_f, as shown in Fig. 3.5, and the switches M_2 and M_3, which operate at a frequency f_s. The higher the value of f_s and C_f, the more energy is transferred through the secondary path.

To control the *main path*, half of the output voltage V_{out} is compared with V_{BG}. The comparison is done through two comparators with ϕ_1 and ϕ_2 (see also Fig. 3.3) to effectively operate twice as fast, compared to a single comparator. When V_{load}, which is the same as V_{out}, and I_{load} are specified and the output power of the RF rectifier is not capable of yielding the load power demand, the duty cycle operation is activated. Hence, the delivered power to the load is lowered by the value of the duty cycle while meeting the load requirements for specific periods. To control the power flow to the load, the gate of device M_1 at top of Fig. 3.5 is switched through a level shifter. As the available output power is high enough, signal A_1 is sensed for being high for a period of time, specified here by a

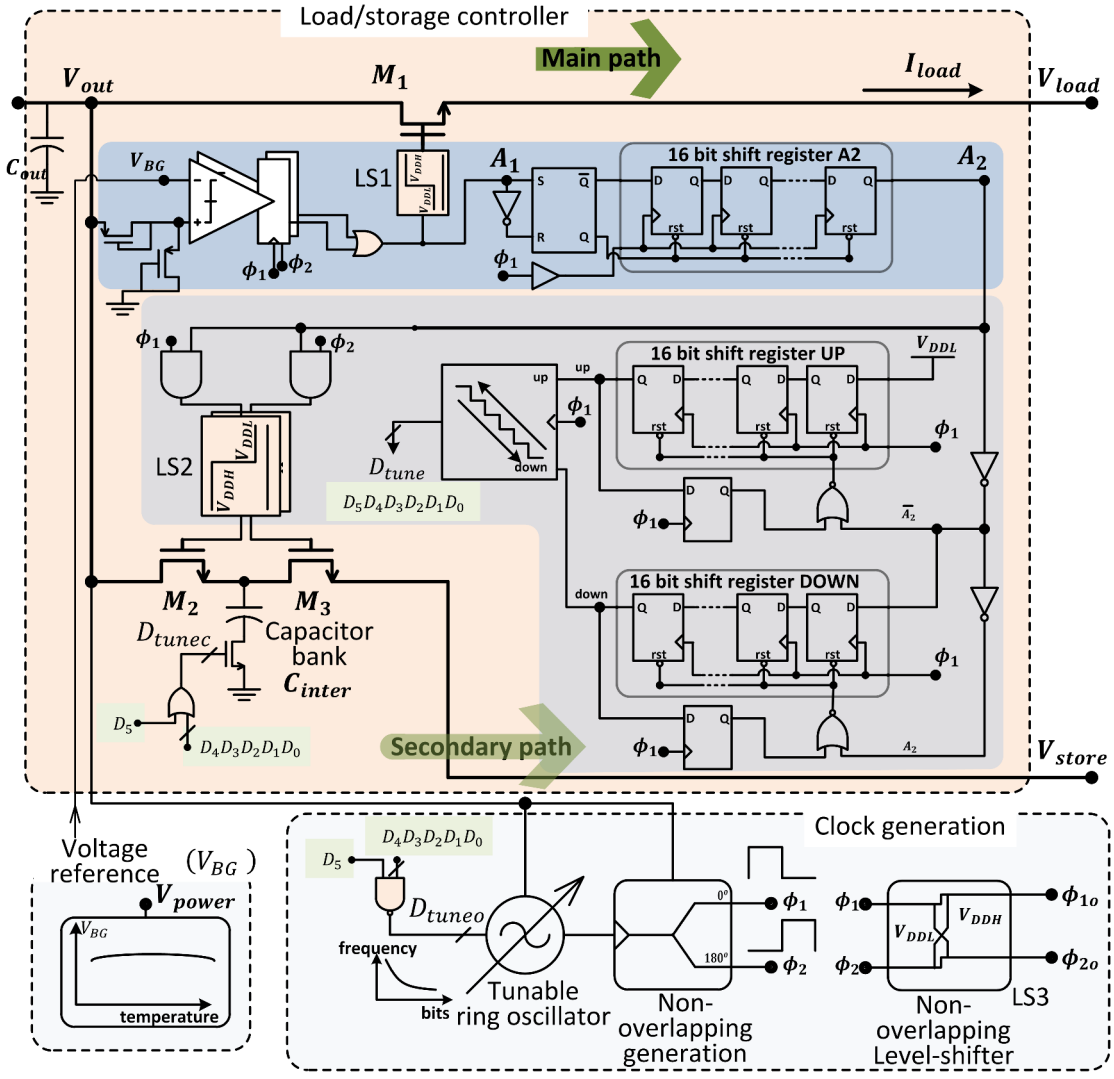


Figure 3.5: Power management/controller: clock generation, voltage reference and power storage controller.

16-bit shift register A2. As a result, signal A_2 goes to high, which activates the *secondary path*. If the value of A_1 drops to zero, a reset is used for the shift registers, and the system waits again to raise the signal A_2. If the signal A_2 is high, the delay of the 16-bit shift register UP is used to check that A_2 is being high for this time. After that delay, the signal *up* goes to high; otherwise, a reset to the shift register UP is used. When the signal A_2 is low, the delay of the 16-bit shift register DOWN is used to make sure that A_2 is being low during this time. Then, the signal *down* goes to high; otherwise, a reset to the shift register DOWN is used. The *up* and *down* signals control a 6-bit binary counter that is implemented with maximum-minimum limiter logics. The control output word D_{tune} (at the middle of Fig. 3.5) of the counter is used to generate the control word D_{tuneo} and D_{tunec} to control the oscillator frequency and the value of C_{inter}, respectively (at the bottom left of Fig. 3.5). The frequency of the oscillator is inversely proportional to the equivalent digital number of the control bits; hence, a NAND gate is used to invert the logic signals. When D_5 is low, the capacitor C_{inter} is proportional to the value of the vector $D_4D_3D_2D_1D_0$, and the minimum frequency is used. When D_5 is high, the maximum capacitance is used while the frequency is tuned with a frequency proportional to the value of the same vector. In Fig. 3.6, the voltage reference [44] is shown, which is all-CMOS design. Moreover, it is the only analog block, which consumes static power (half of the total power consumption of the design). $M_{11}, M_{12}, M_{33-35}$ are used for startup, and the remaining devices are the core circuit of the reference generator. The reference voltage output V_{BG} is 0.52 V where the load capacitance at the output will affect the startup time which is critical from a system point-of-view. This design was optimized for low power consumption with 40 nA current consumption. Other implementations can be used for better accuracy at the expense of consuming more power.

A tunable ultra-low power current-starved ring oscillator is shown in Fig. 3.7. The oscillator frequency is tuned through the digital capacitor bank $C_1 - C_7$. The voltage of

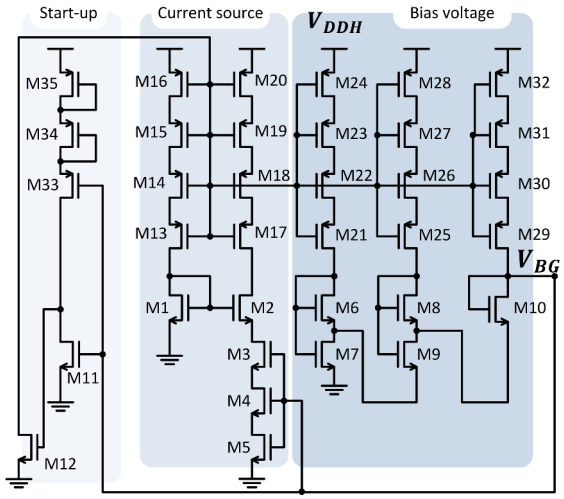


Figure 3.6: Voltage reference generation.

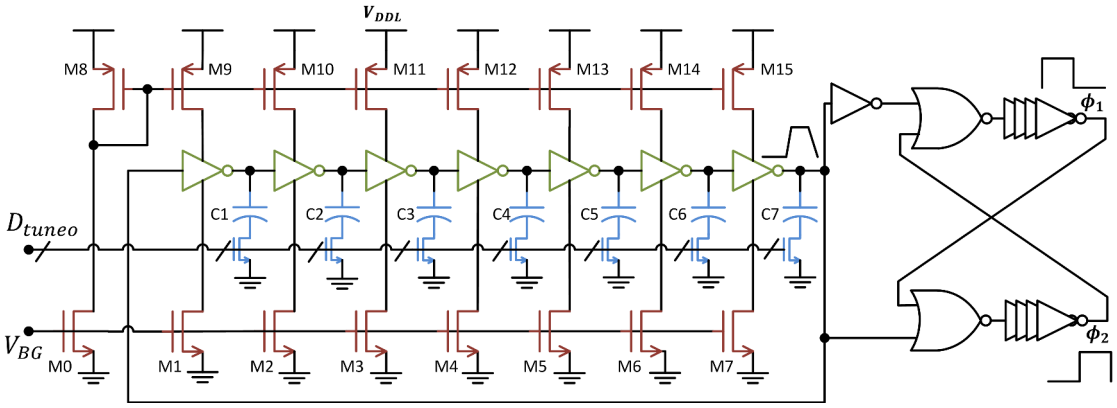


Figure 3.7: Tunable ring oscillator and non-overlapping clock generation.

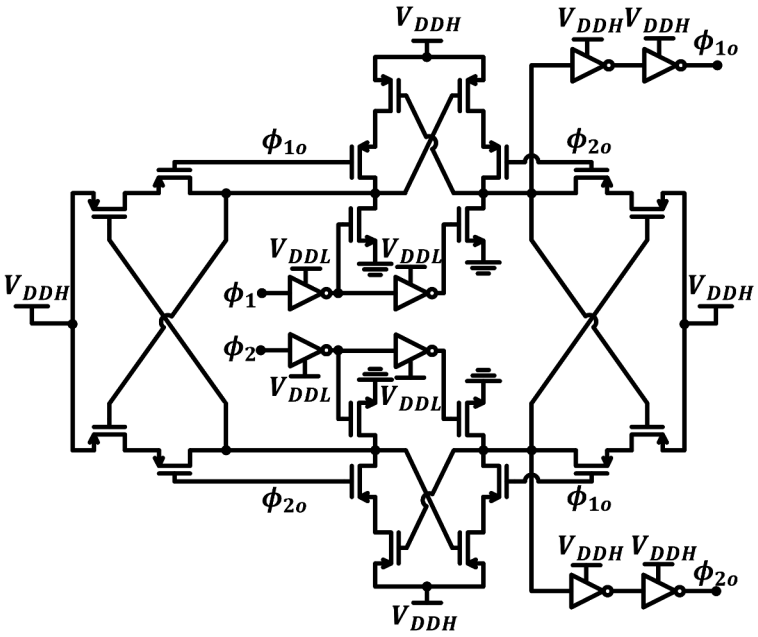
the current-starved devices, $M_1 - M_7$ and $M_9 - M_{15}$, is obtained from the V_{BG} which is low when the available output power is small, and the oscillator takes less-current at startup. The oscillator feeds a non-overlapping clock generation block that produces two phases, ϕ_1 and ϕ_2. The clock generation chain with the oscillator consumes 26 nA and 117 nA for the lowest and highest frequencies, respectively. Fig. 3.8a depicts the proposed non-overlapping level shifter (LS3) to shift ϕ_1 and ϕ_2 to ϕ_{1o} and ϕ_{2o}, respectively. The block

takes non-overlapping input signals and produces level-shifted versions as shown in Fig. 3.5. The implementation is done through cross-coupling of the two level shifters. The use of two regular level shifters cannot guarantee the non-overlapping operation of the output clocks, which is important to minimize the losses in the digital circuits. Simulation results for the non-overlapping behavior are shown in Fig. 3.8b. The non-overlapped high voltage signals ϕ_{1o} and ϕ_{2o} are used for the implementation of the controller of the RF rectifier as will be shown.

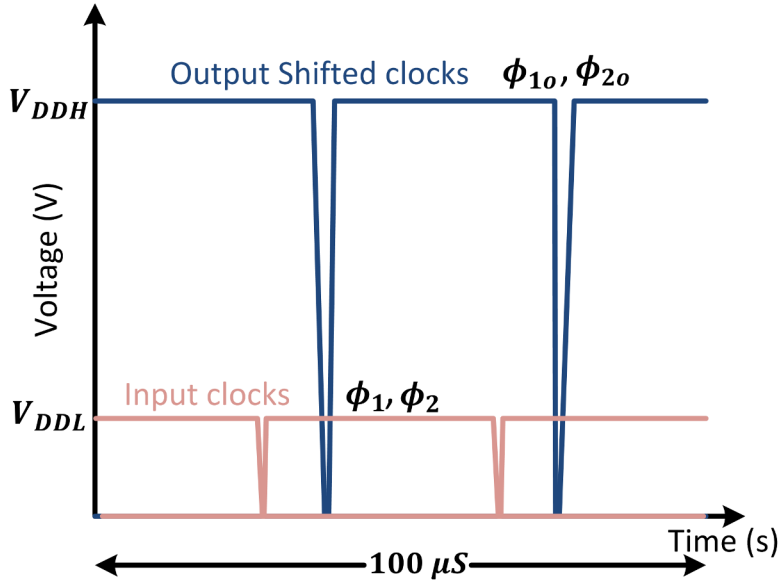
Table 3.1 shows the truth table for the signals of the control switches of the reconfigurable RF rectifier. A one bit per sub-block SW(1-2 ... 7), illustrated in Fig. 3.4 in the lower right side, is needed. The bits are generated by three independent signal controls, N_0, N_1 and N_3. Signal N_3 is used, instead of N_2, to highlight that N_2 will be redundant and is equal to N_0. The implementation of the controller of the RF rectifier circuit is shown in Fig. 3.9. The controller of the RF rectifier senses the voltage of the last non-reconfigurable stage $V_{th,stage}$, which is proportional to the open circuit voltage of one stage and then, compares it to different threshold levels. As the available output power and the value of $V_{th,stage}$ increase, fewer stages are used to obtain better efficiency. The value of V_{BG} is designed to be 1/4 of the desired open circuit voltage V_{th}, for this $N = 8$ design, where scaling is used between the values of $V_{th,stage}$ and V_{BG} in order to maintain low

Table 3.1: Truth table for the control signals of the reconfigurable RF rectifier.

Switch Signals (in Fig. 4) →		SW7	SW6	SW5	SW4	SW3	SW2	SW1
Control bits →		N_0	N_1	N_0	N_3	N_0	N_1	N_0
	8	0	0	0	0	0	0	0
	4	0	0	0	1	0	0	0
N	2	0	1	0	1	0	1	0
	1	1	1	1	1	1	1	1



(a)



(b)

Figure 3.8: Proposed non-overlapping cross-coupled level shifter: (a) circuit. (b) simulation with exaggerated rise/fall times for illustration.

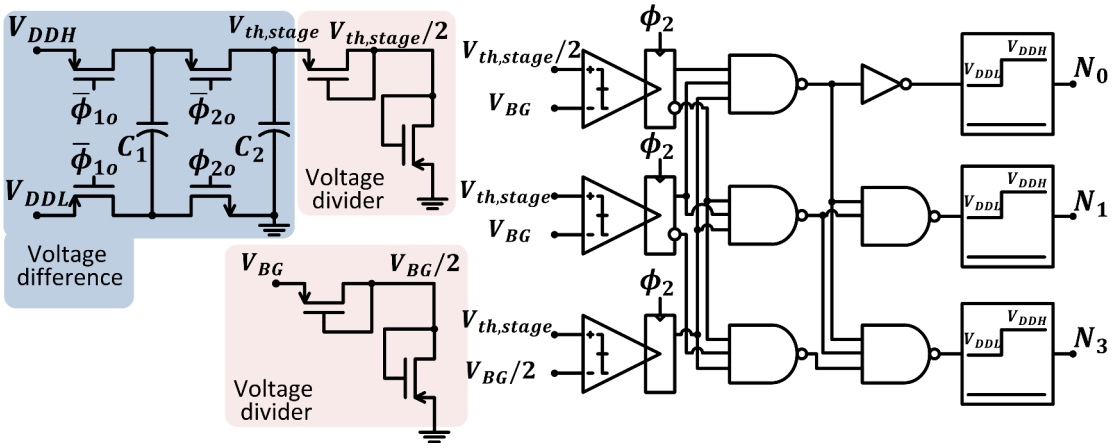


Figure 3.9: Controller of the RF rectifier circuit implementation.

voltage operation. The estimation of V_{th} by a multiple value of $V_{th,stage}$ is valid, given that the loading current from the auxiliary RF rectifier is small, compared to the current supplied by the main RF rectifier. The switching signals SW1, SW3, SW5, and SW7 are the same since all odd stages shall be either connected to the output or to the next stage. For the switching signals connected to even stages, there should be symmetry in control signals between the beginning and ending of the reconfigurable RF rectifier; hence, SW2 and SW6 have the same signals. A switched capacitor C_1 voltage difference circuit is used to measure the voltage $V_{th,stage}$ periodically, and a deep-subthreshold voltage divider is used to get $V_{th,stage}/2$ and $V_{BG}/2$. High voltage clocks are needed for sampling, and the non-overlapping level shifted signals ϕ_{1o} and ϕ_{2o} are used. This prevents the shoot-through current loss. Moreover, latched comparators, logic circuits and shifters generate the required control bits to decide the number of stages. There is no direct interaction between the controller of the RF rectifier and the power management/controller, as shown in Fig. 3.5. However, the former circuit, with a fast path, directly controls the final open circuit voltage of the RF rectifier, which indirectly affects the signals of the latter. The loop of the control of the RF rectifier has a faster response by having less delay than the

loop of the power management/controller.

3.4 Modeling of the RF Rectifier

The RF rectifier is composed of a cascade of a multiple of ac to dc conversion stages. Each stage converts the ac input and feeds its dc output V_{DC} to the next stage [42]. The dc voltage is accumulated from one stage to the next. The final dc output voltage V_{out} is related to the number of series stages N by the relation: $V_{out} = NV_{DC}$.

The main parameters of the RF rectifier are:

1. Harmonic content
2. Input impedance (Z_{in})
3. Output dc current (I_{DC})
4. Power Conversion Efficiency (PCE)

The input impedance is considered as the parallel combination of a resistive part $R_{rect} = 1/G_{in}$ and a reactive part $X_{rect} = 1/B_{in}$. The value of R_{rect} is related to V_{in} and I_{in}, which are the fundamental amplitudes of the input ac voltage and current, respectively. Here, R_{rect} is analyzed using the nonlinear operation of the diodes. The nonlinear voltage-dependent capacitance of the pn junctions, which is part of the diode-connected devices, contributes to the input capacitance of the RF rectifier. The average value of the nonlinear varactor, as was discussed in [16], is dependent on the voltage swing, and the power levels, across the pn junctions. This will affect the matching network performance and introduces mismatch. In [29], an automatic tuning feedback loop was introduced. Here, the matching network is preset for the low input power levels and the variation of the input impedance, with different input power levels, will be partially compensated by the reconfigurable operation of the RF rectifier, as will be discussed in subsection 3.4.4. The power conversion

efficiency is given by:

$$PCE = \frac{P_{DC,out}}{P_{in,fundamental}}. \tag{3.4}$$

In these models, the classical equation current-voltage relation of the diode:

$$i_d = I_S \left(\exp \left(v_{diode} / V_T \right) - 1 \right), \tag{3.5}$$

is used where I_S is the saturation current, v_{diode} is the voltage across the diode, V_T is the thermal voltage and equals to KT/q (26 mV in room temperature), and i_d is the diode current. Although (3.5) is not accurate for deep submicron technologies, where the slope factor n is different than 1 [42], it is used to get closed form expressions of the rectifier parameters. Here, I_{SN} is the total I_S current for all sub-diodes and equals to NI_S. Moreover, the total input resistance of the N-stage RF rectifier is the parallel combination of the resistance of each stage [42].

At low-input power, both the RF current and voltages, at the input terminal of the RF rectifier, are sinusoidal. As the input power increases, while the current is approximately sinusoidal, the voltage waveform starts to deviate from the sinusoidal behavior. Other than that, Harmonic Balance should be used where nonlinearities of both currents and voltages appear dominant. Thus, the rectifier can operate in two modes [45]: the voltage-mode and the current-mode, which are equivalent to low-input power and high-input power modes, respectively. The modeling of the RF rectifier is carried out in the appendices, only the highlights are discussed here in this section. A fixed output voltage V_{DC} is assumed, and the parameters are derived according to this V_{DC} constraint and the input condition.

3.4.1 Low-Input Power RF Rectifier

In this mode, the input of the RF rectifier is assumed to be a sinusoidal voltage as shown in Fig. 3.10. In any configuration of the LC matching that guarantees the input resistance

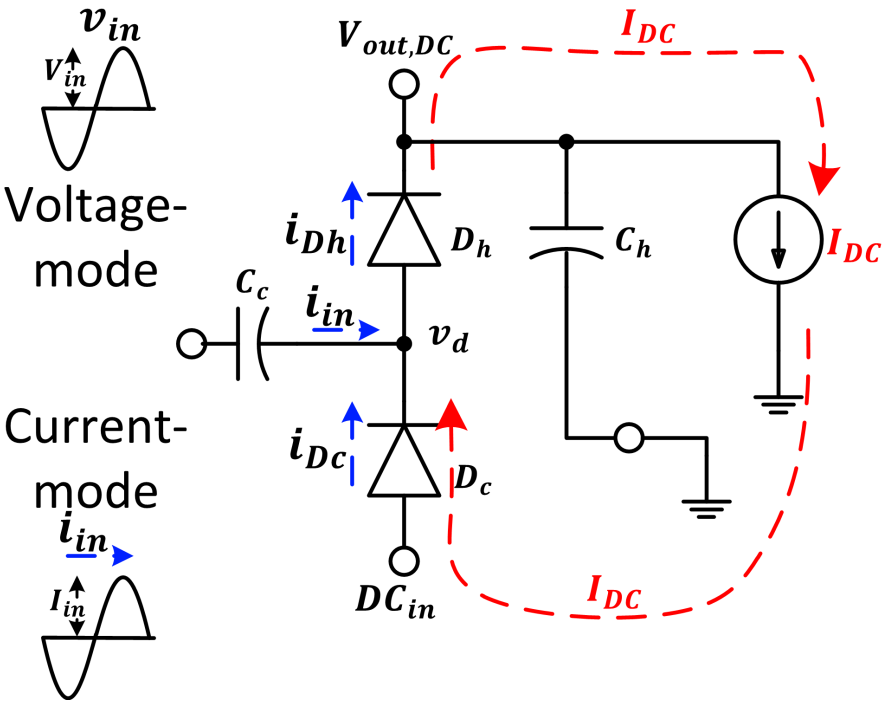


Figure 3.10: One-stage RF rectifier for illustration with voltage-mode or current-mode excitation.

is much higher than the source resistance, the rectifier is said to be in the voltage-mode.

Assuming the input voltage is sinusoidal:

$$v_{in} = V_{in} \cos(\omega_o t) . \tag{3.6}$$

The harmonics in the input current are given by:

$$i_{in}[n, odd] = 2I_S \, \mathrm{e}^{-V_{DC}/2V_T} \, \mathrm{I_n}\left(\frac{V_{in}}{V_T}\right) . \tag{3.7}$$

Moreover, the expression of the input resistance (for N stages), becomes:

$$R_{rect} = \frac{V_{in} N \, \mathrm{e}^{V_{out}/2NV_T}}{2I_{SN} \, \mathrm{I}_1 \left(\frac{V_{in}}{V_T}\right)}. \tag{3.8}$$

The output dc current yields:

$$I_{DC} = \frac{I_{SN}}{N} \left(\mathrm{e}^{-V_{out}/2NV_T} \, \mathrm{I}_0 \left(\frac{V_{in}}{V_T}\right) - 1 \right), \tag{3.9}$$

and the power conversion efficiency (for N stages) is:

$$PCE = \frac{V_{out} I_{SN} \left(\mathrm{e}^{-V_{out}/2NV_T} \, \mathrm{I}_0 \left(\frac{V_{in}}{V_T}\right) - 1 \right)}{N \; P_{in,fundamental}}. \tag{3.10}$$

3.4.2 High-Input Power RF Rectifier

In this mode, the input of the RF rectifier is assumed to be a sinusoidal current as shown in Fig. 3.10. In any configuration of the LC matching that guarantees the input resistance is much lower than the source resistance, the rectifier is said to be in the current-mode. Assuming the input current is sinusoidal:

$$i_{in} = I_{in} \cos\left(\omega_o t\right), \tag{3.11}$$

The third harmonic in the intermediate voltage v_d, which is the same as the input voltage since the input capacitor is short circuit at high frequencies, is given by:

$$v_d[3] = \frac{4\left(1+P^2\right)^{3/2} V_T}{3\pi P^3} \left\{ \left(\frac{8P^2}{1+P^2} - 2 \right) \mathrm{K}\left(\frac{P}{\sqrt{1+P^2}} \right) - \left(2 + \frac{7P^2}{1+P^2} \right) \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}} \right) \right\}, \tag{3.12}$$

where $P = \frac{I_{in}}{I_{SN}} N \, \mathrm{e}^{V_{out}/2NV_T}$. The expression of the input resistance yields:

$$R_{rect} = \frac{\frac{4\sqrt{1+P^2}}{\pi P} V_T \left\{ \mathrm{K}\left(\frac{P}{\sqrt{1+P^2}}\right) - \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}}\right) \right\}}{I_{in}}, \tag{3.13}$$

The output dc current is given by:

$$I_{DC} = \frac{I_{SN}}{N} \left(\frac{2}{\pi} \, \mathrm{e}^{V_{out}/2NV_T} \, \sqrt{1+P^2} \, \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}}\right) - 1 \right), \tag{3.14}$$

and the power conversion efficiency is:

$$PCE = \frac{V_{out} I_{SN} \left(\frac{2}{\pi} \, \mathrm{e}^{V_{out}/2NV_T} \, \sqrt{1+P^2} \, \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}}\right) - 1 \right)}{N \, P_{in,fundamental}}. \tag{3.15}$$

3.4.3 Level-m Compensation Effect on the RF Rectifier Relationships

As derived in Appendix, all previous equations where I_S is encountered shall be replaced by $I_S' = I_S \exp\left(\frac{mV_{DC}}{\phi_t}\right)$. From (3.10), in the low-input power operation, the PCE of the rectifier is independent of the saturation current I_S, and the compensation will have no effect on the PCE in this regime. However, the input impedance, from (3.8), is affected and decreased where the rectifier starts to leave that mode of operation. The I_S affects all the characteristics of the high-input power mode.

3.4.4 Number of Stages and Input Amplitude Effects

As shown in Fig. 3.11, a large signal S-parameter transistor level simulation is plotted for different stage configurations. The return loss S_{11} of the RF front end is plotted while sweeping input power, maintaining a constant output voltage of 1 V and using a preset configuration for the matching network. The system shows that the input matching can be maintained over a wider input range compared to a single configuration. For example, at

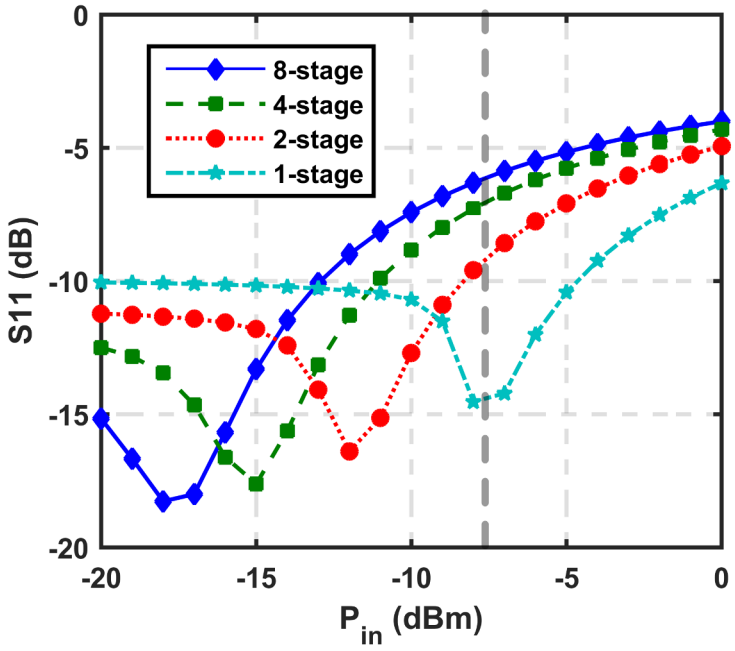


Figure 3.11: Large signal S-parameter simulation while input power is varied.

$P_{in} = -7.5$ dBm, the use of an eight-stage configuration yields a return loss of -6 dB, which results in a reflection loss of 1.26 dB, while the use of a one-stage configuration yields a reflection loss of 0.14 dB. This directly affects the efficiency of the RF front end with percentages of 86.5% for the former case and 98.4% for the latter case. Thus, reconfiguration can maintain the input matching conditions and reduce reflection loss. We concluded that automatic tuning of the matching network does not satisfy the overhead and, thus, can be omitted.

The PCE increases (or decreases) as the number of stages decreases (or increases) while using all sub-blocks. It is desirable to have the lowest number of stages in order to increase the available output power. On the other hand, a minimum number of stages must be used to get sufficient dc output voltage for small inputs. Thus, as the input amplitude increases (or decreases), the number of stages should decrease (or increase) and the

rectifier is required to have more (or less) stages to generate a required dc output voltage.

3.4.5 Matching Network Design

The tunable matching network can be considered as a cascade of three L matching sections [34], as shown in Fig. 3.4 at the top right side: the first section is composed of the input capacitance C_{rect} of the rectifier and L_{M1}, while the second section is represented by C_{BM1} and L_{M2}. The third section consists of C_{BM2} and the bonding wire with any parasitic inductance to the source. The objective of the matching network is to transform the source (antenna) impedance, which is 50 Ω, to the rectifier input resistance R_{rect}, while absorbing the value of C_{rect} into the design. The desired impedance to each L section is R_s. Moreover, each L section is loaded by R_p, where R_p is the input impedance of the next L section, and the loaded quality factor is Q_i. Hence, the design equations [34] are:

$$R_p = \left(1 + Q_i^2\right) R_s, \tag{3.16}$$

$$Q_i = \frac{\omega_o L_{Mi}}{R_s}, \tag{3.17}$$

$$L_{Mi} C_{Mi} = \omega_o^2, \tag{3.18}$$

where ω_o is the operating frequency (900 MHz is used), C_{Mi} and L_{Mi} are the capacitance and inductance of each section, respectively and i=1, 2, ... n. The total efficiency is the product of the efficiencies of the individual sections. Due to the limited quality factor Q_L of the on-chip inductors, which are typically between 6 to 7, [46] showed that in order to maximize the total efficiency, the values of Q_i should be equal. This imposes a constraint

on the interface impedance between the sections. Thus, Q_i will be:

$$Q_i = \sqrt{\left(\frac{R_{rect}}{R_{s,50}}\right)^{1/n} - 1}, \tag{3.19}$$

and the overall efficiency would be:

$$\eta = 1 - \frac{n}{Q_L}\sqrt{\left(\frac{R_{rect}}{R_{s,50}}\right)^{1/n} - 1}, \tag{3.20}$$

where here, n=3 and the first section, composed of L_{M1} and C_{rect} is not fully controllable since C_{rect} is defined by the input capacitance of the RF rectifier. The expected voltage boosting of the matching network is given by $\sqrt{R_{rect}/R_{s,50}}$.

3.5 Experimental Results

The proposed RF energy harvesting system was designed and fabricated using 0.18 μm CMOS technology. The die photo is shown in Fig. 3.12, the active chip area is 1.08 mm^2 where the area of the reconfigurable RF front end is 0.756x0.624 mm^2, and the power management/controller takes 1.084x0.56 mm^2.

The RF front end consists of the LC matching network and the reconfigurable RF rectifier. The values of L_{M1} and L_{M2} are respectively 12.6 nH and 30 nH with chip areas of 260x260 μm^2 and 360x360 μm^2. On the antenna side, the loaded quality factor is small, which permits the use of lower quality factor with a higher inductance value L_{M2} to achieve the input matching. On the other hand, the loaded quality factor on the input of the rectifier is high, so L_{M1} is chosen for maximum quality factor Q_L (about 8). The maximum values of the tunable capacitors C_{BM1} and C_{BM2} are 300 fF and 5.7 pF, respectively, excluding the parasitic capacitance at the inductor terminals. The test setup for the RF front end is shown in Fig. 3.13 (a). Moreover, Fig. 3.13 (b) shows the test setup for the total system, which will be described shortly. A data acquisition (DAQ) card is used

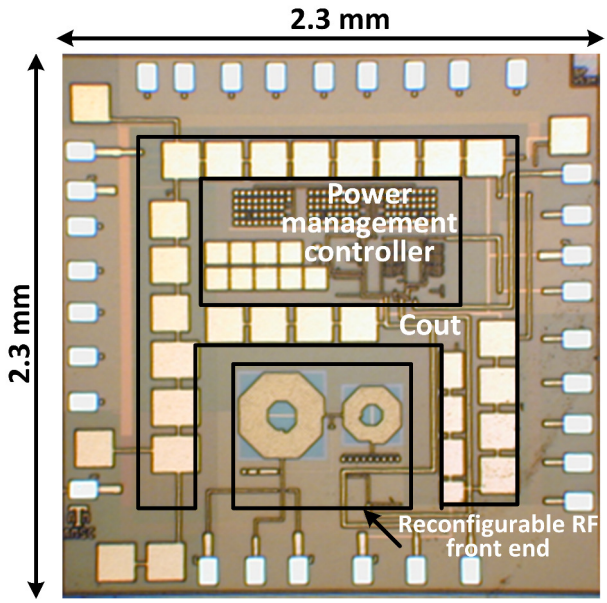


Figure 3.12: Micrograph of the RF energy harvesting system prototype IC.

to control the input power sweep of the RF generator and to record values of the output voltages. The RF front end is measured for all configurations of the RF rectifier in Fig. 3.14. Note that the right vertical axes have ranges that are different for the sub-figures. Output voltage versus input power for different load currents is plotted. This test measurement was conducted for a range of load resistances from 2 kΩ to 10 MΩ. It was done with external switching signals with a 1.8 V supply level. In Fig. 3.14a, an eight-stage configuration is used. When $P_{in} = -18$ dBm, the RF front end will provide a 1 V dc output voltage for a load resistance of 10 MΩ. Note that the delivered current range is from 0 to 120 μA for the input power range from-25 dBm to 2.5 dBm. In Fig. 3.14b, with the use of four-stage configuration, the delivered current range extends from 0 to 220 μA for the same input power range while delivering an output voltage of 1 V at higher input power range than shown in Fig. 3.14a. The use of two-stage and one-stage in Figs. 3.14c and 3.14d respectively widens the current delivery to ranges between 0 and 380 μA and

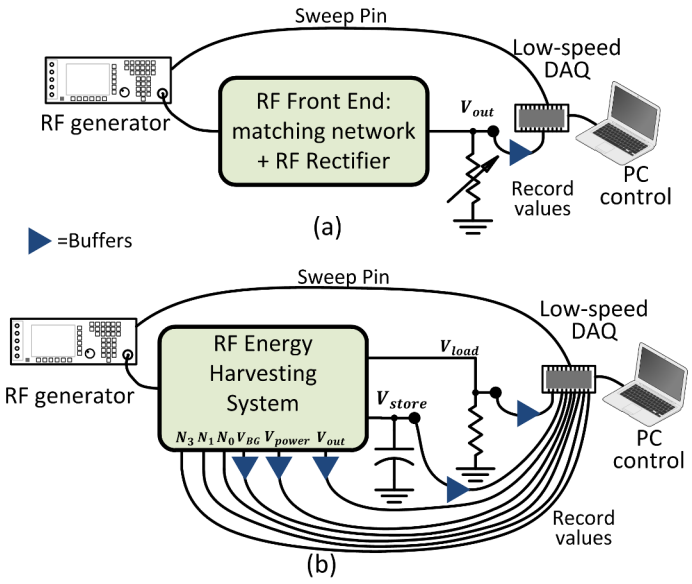


Figure 3.13: Test setup for: (a) RF front end, (b) RF energy harvesting system.

between 0 and 500 μA, while delivering an output voltage of 1 V for the high input power ranges. At the lowest load and high power delivery, the switching signals at the gate of the switches are not high anymore with respect to the source/drain, and that is why the output voltage is almost unchanged. With ideal switches, the output voltage of the RF rectifier is expected to rise monotonically, as the number of stages increases despite maintenance of the same input power, which raises reliability issues of the fabricated chip. For non-ideal switches, the voltage output voltage is decreased by the values of the voltage drop across the switches which is proportional to $I_{out}R_{on}$ and the configured number of stages (one, two, four, or eight).

It is appropriate here to consider the PCE of the main load path compared to previous results. But when the two paths are considered, due to non-ideal losses, the PCE is degraded (as will be shown). The PCE versus input power, considering only the main path, is shown in Fig. 3.15 where the PCE is plotted for output voltage greater than 1 V. This constraint on the output voltage is arbitrary, and depends on the system design of the power

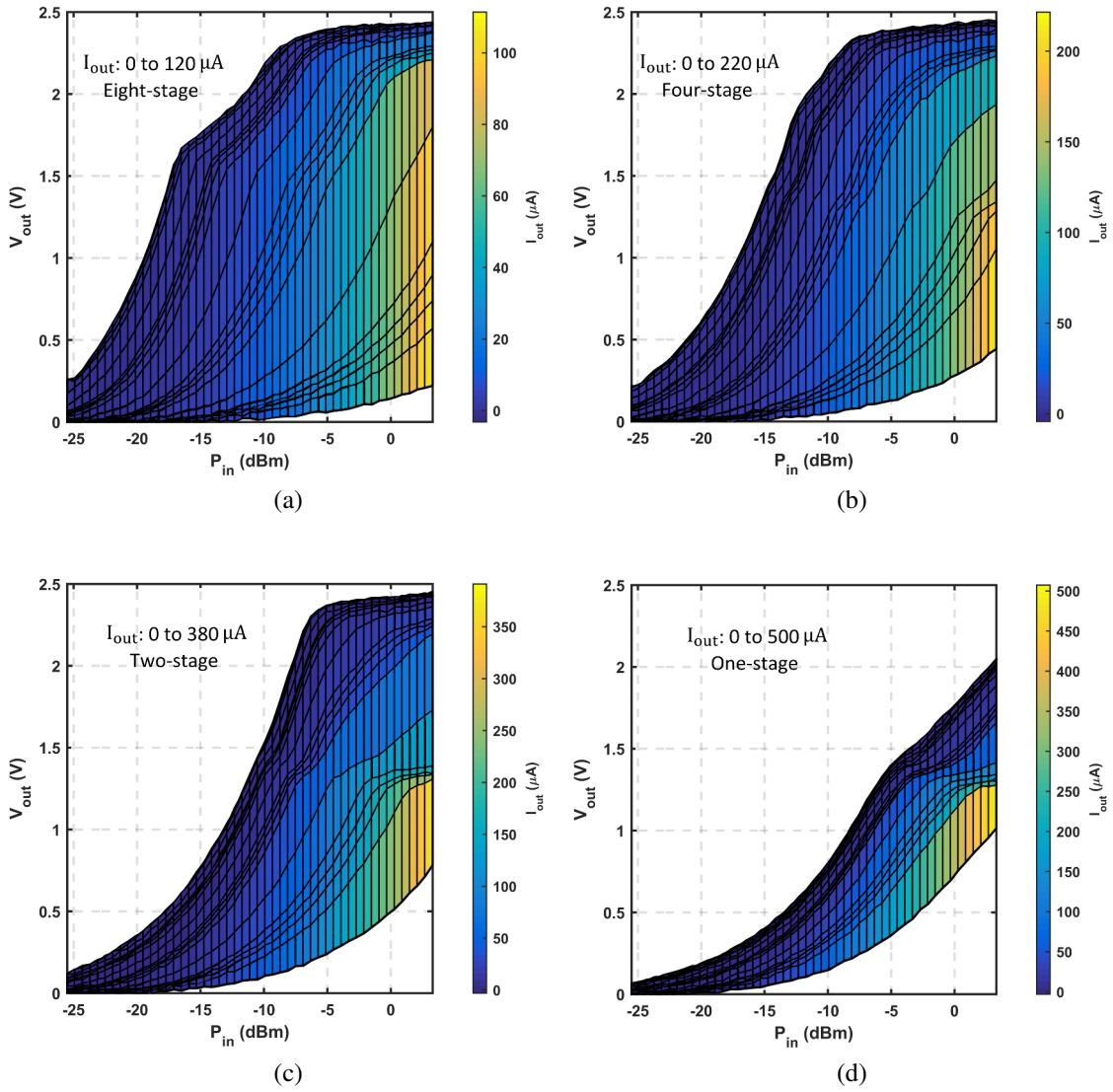


Figure 3.14: Steady-state measurements of the output voltage for the cascade of the reconfigurable RF rectifier and the on-chip matching network versus the input power P_{in} for different output currents I_{out} (more current obtained for fewer stages): (a) eight-stage, (b) four-stage, (c) two-stage, and (d) one-stage.

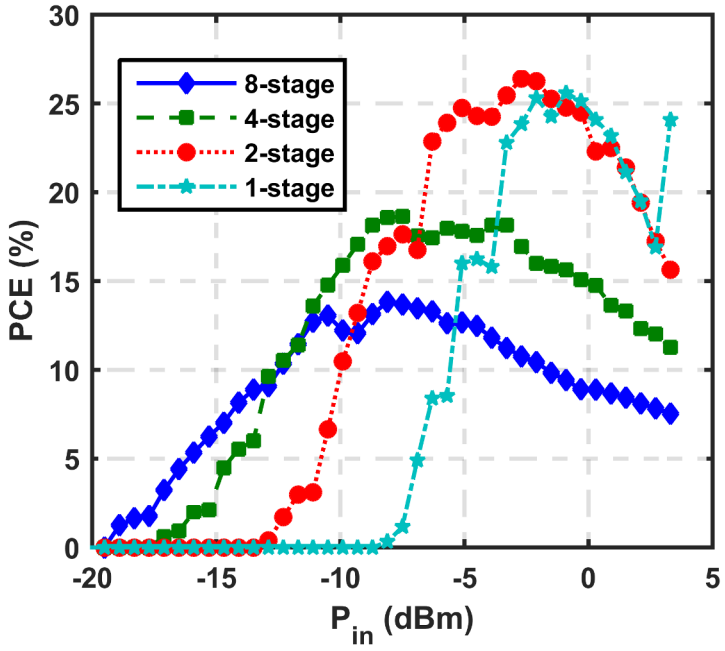


Figure 3.15: Power conversion efficiency, including the matching network and the RF rectifier, versus input power P_{in} for different stage configurations for output voltage greater than 1 V.

management circuit succeeding the RF rectifier. When the output voltage is less than 1 V, the PCE is plotted as zero. The plot shows that at low input power, a higher number of stages is required to get the sufficient output voltage. As the input power increases, fewer stages are needed. Moreover, each configuration of the RF rectifier has an input power range where the PCE is maximal. The total PCE is defined as:

$$\text{PCE} = \eta_{matching} PCE_{rect}, \tag{3.21}$$

where $\eta_{matching}$ is the efficiency of the matching network and PCE_{rect} is the power conversion efficiency of the RF rectifier. $\eta_{matching}$ is dependent on the quality factor of the matching elements where off-chip equivalent elements for a non 50 Ω antenna/rectifier interface [29] and potential system-in-package elements [47] give an advantage. On the

other hand, PCE_{rect} is process dependent where the characteristics of the diodes, mainly the threshold voltage and leakage current, affect this number. Different processes like silicon-on-insulator (SOI) and high performance customized processes [47] gives performance advantage where similar results for RF power amplifiers are published in the literature. The product [47] has a higher PCE with a large package of 0.625x0.53 inch^2, and the details of the design and the fabrication technology are not published. Therefore, it is difficult to compare to the proposed design.

In addition to that, the reconfiguration of the number of stages of the RF rectifier introduces ohmic losses on the dc side of the rectifier which should be, by careful design of the reconfiguration switches, small; however, they eventually contribute to the losses of the RF rectifier.

The total RF energy harvesting system is measured at startup conditions to show the duty cycling capability of the system as shown in Fig. 3.16 where the load voltage V_{load} starts from 0% duty cycle to 100% at a sufficient input power. The steady-state duty cycle is plotted versus the input power. The test setup for the RF energy harvesting system is shown in Fig. 3.13 (b). The DAQ card is used for recording values of different signals, and sending control signals to the RF generator. Then, the transient measurement results of the system are shown in Fig. 3.17 for different wider ranges P_{in} with a demand current of 1 μA represented by 1 MΩ resistance and a C_{store} of value 100 µF. The measurement results are obtained by sweeping input power in 2.5 dB steps from -19.2 dBm to 0.8 dBm, where each lasts for 10 seconds. At low power, the controller circuit powers up, and the sensitivity for that is measured at -14.8 dBm, when the load begins to receive the duty cycled current. As P_{in} increases, the number of stages decreases. The voltage reference is constant with V_{power} except for supplies exceeding 3 V. V_{load}, the storage capacitor voltage V_{store}, V_{out} and V_{power} are shown in Fig. 3.17. At low input power and low available output power, the load current is duty cycled and no power is delivered to C_{store}. As the

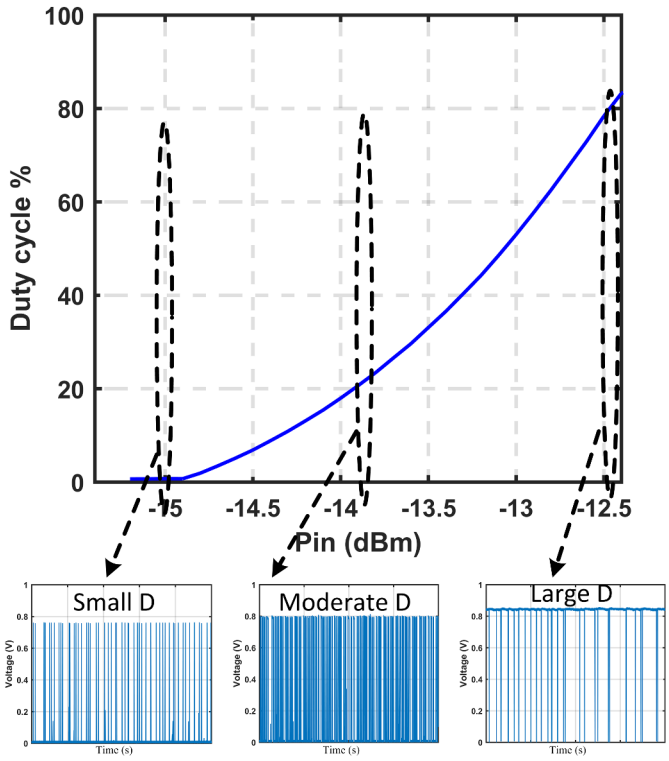


Figure 3.16: Measurements of the startup of the system versus input power with small steps to show the duty cycling feature (duty cycle D) of the system.

input power increases, the load current is continuous, the output voltage is designed to be regulated to twice V_{BG} and charges are transferred to C_{store}, where the secondary path is used to absorb the extra energy. The values of the maximum frequency f_s and maximum capacitance C_f limit the maximum extra absorbed energy where in simulations, larger C_f capacitance helps to maintain the regulation at high input power levels. For the current design of the secondary path, the power extraction through this path is bounded to a value proportional to $\frac{1}{2}C_f f_s V_{sout}^2$ and the energy flow through this path saturates when the maximum C_f and f_s are used. So, the extra power needs to go somewhere which is shown here to be a higher value of V_{out} voltage than 1 V and $P_{out} = V_{out}I_{load}$. The increase of V_{load} also affects the efficiency of the RF rectifier (the reported PCE in Fig. 3.15 is for specific

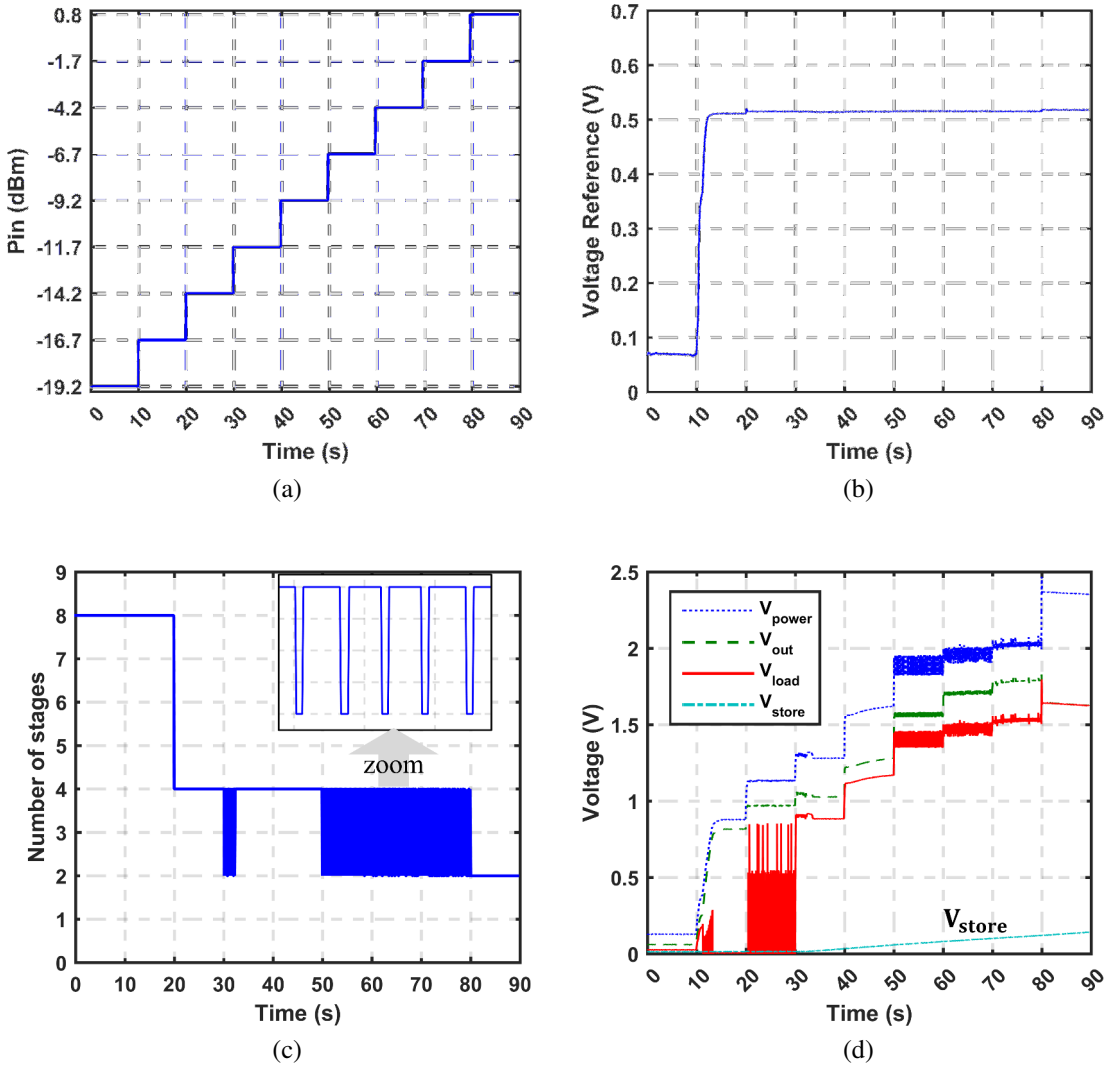


Figure 3.17: Transient measurement results for sweeping input power in 2.5 dB steps from −19.2 dBm to 0.8 dBm, where each lasts for 10 seconds: (a) sweep of the input power. (b) the startup of the reference voltage, (c) the change of the number of stages, and (d) the different dc output voltages.

loads) which will affect the end-to-end efficiency. A potential solution is to cascade a low dropout regulator (LDO) to filter any variation since the maximum capability of the secondary path will be reached when the maximum power extraction capability is reached. This will be at the expense of more complexity and power consumption. For simplicity, no LDOs were used in the current implementation. At very high input power, higher than 0.8 dB, the secondary path reaches a higher voltage than its maximum capability, and the dc voltages start to increase; particularly, the reference voltage, which causes all the other voltages to increase at the same rate. This is a typical case for non-reconfigurable RF rectifiers, where the output voltage increases as the input power increases. But here, this is prevented from happening until a very high input power is reached, where higher maximum values of operating frequency and/or C_{store} should be used to further improve the design. The RF rectifier switches back and forth between two-stage and four-stage configurations when the input power is between -6.7 dBm and -1.7 dBm. The difference between V_{power} and V_{load} is around 0.5 V. The loading effect of the protection diodes introduces some error in the estimation of the open circuit voltage. This switching action increases the ripples on the output voltages of the system in these regions of operation and the efficiency is degraded from the optimal value due to this estimation. More protection diodes in series will decrease this toggling error, but since a standard CMOS process, with no high voltage devices, was used, the number of series protection diodes was limited to only two, which prevented the value of V_{power} to reach high voltage. The effect of the error, due to the protection diodes, was to shift the decision points of the number of stages to be used. According to our simulations, when protection diodes are omitted (or the use of more stack of diodes), the $(V_{power} - V_{out})$ can go to twice Vout. Table 3.2 shows an estimation of the amount of harvested energy and energy consumption (power multiplied by duration) of the main building blocks at different input power levels, assuming a 10 second period. The consumption of the level shifters is not taken into account since it is negligible

Table 3.2: Harvested energy and consumption in μJoule for 10 seconds duration.

Pin,dBm	-15	-12.5	-10	-7.5	-5	-2.5	0
Bandgap	0.48	0.52	0.64	0.76	0.8	0.8	0.92
clock gen	0.66	0.726	0.96	1.4	1.755	1.755	1.872
harvested	6.4	8.5	11.2	16.4	25.3	26.1	30.0

provided that nonoverlap clocking is guaranteed. The harvested energy is calculated for both the load I_{load} and the storage capacitor C_{store}. To the best of the authors' knowledge, the proposed work is the first work to harvest the extra power in an RF energy harvesting system. For the case of a fixed load shown here as 1 MΩ, about 3X power is extracted at 0 dBm with respect to the fixed load. The limited value of $(V_{power} - V_{out})$ will introduce losses in the switches and especially the switches near the end. So, the performance of the switches suffers resulting in a poor efficiency. Also, higher values of V_{out} will degrade the RF energy harvesting front end. The I-V curve of the rectifier has the maximum efficiency at the point where the voltage starts to decrease, and maximum current can be obtained. The maximum capability of the secondary path limits the extracted power of this path. More extracted energy can be obtained at high input power with the use of larger values of C_f in the secondary path or multiple secondary paths.

If the input power becomes low or is absent, storage capacitor C_{store}, after some charging time passes, can be used to feed the demand current, which is represented by the 1 MΩ. The off-chip capacitor C_{store}, which is an aluminum electrolyte with a value of 100 μF, is switched with an external switching circuit for the purposes of proof of concept. A low leakage switch, with leakage in the range of 1-2 nA, is also used. Fig. 3.18 shows the different time loading cases for eight hours. First, no power is delivered to the load and leakage effects are observed. After 8 hours, the voltage across the storage capacitor

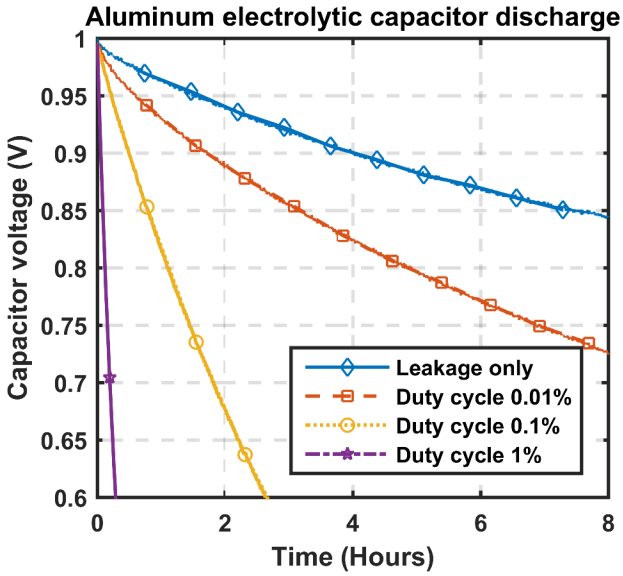


Figure 3.18: Experimental results for storage capacitor delivering power to load.

is reduced by 15%. For a 10 seconds periodic time and duty cycles of the 0.01%, 0.1%, and 1%, the storage capacitor is able to support the demand of the load with different lifetimes. The lifetime will be dependent on how low voltage the load can operate with. For instance, for 0.01% duty cycle, the voltage is reduced by 20% after nearly 5 hours. Using lower leakage capacitors such as film capacitors or super-capacitors can prolong the operation of the system.

Table 3.3 shows how the design is compared to other designs in the literature. The proposed design is reported to be self starting, incorporates power management and delivers power to a load where previous works used RF energy harvesting either to startup or deliver power to a load. Simultaneous delivery of power to the load and a storage capacitor with two different paths is a unique practical feature. This can allow the separate optimization of the two paths, where the former is real-time, and the latter is slow and used for long-term operation. The output dc voltage is bounded, and the design is reconfigurable to maximize the PCE. No extra off-chip inductors are used, and the passives are

Table 3.3: Comparison table with other energy harvesting systems.

	ESSCIRC2012[4]	TCAI2013[5]	JSSC2015[6]	JSSC2013[7]	This Work
Power output usage	Load	Start-up, load	Start-up	Start-up, control	**Start-up, power management, load**
Simultaneous capacitor charging and load powering	No	No	No	No	**Yes for extra power**
Bounded output voltage	No	N.A.	No	N.A.	Yes*
Frequency	915 MHz	830 MHz	915 MHz	433 MHz	915 MHz
Matching network	Off-chip	Off-chip	No matching	Off-chip	**On-chip and tunable**
Extra off-chip inductors	Yes	Yes	No	Yes	**No**
Number of stages of the RF rectifier	1-2	1**	30	6	**1-2-4-8**
Control to handle different loads	No	Yes	No	No	Yes
Sensitivity	−17 dBm @ 1.8 V (capacitive load)	−17 dBm @ 0.5 V*** (1 MΩ load)	−14.5 dBm @ 0.55 V (capacitive load)	−10 dBm @ 1.35 V (capacitive load)	**−14.8 dBm @ 1 V (1 MΩ load)**
Maximum PCE of RF rectifier+matching network	40%, 60% **** (@ -12, -2 dBm)	53% **** (@ -15 dBm)	-	-	**14, 18, 25, 25% (@ -11, -8, -5, 0 dBm)**
Current consumption	-	1560 nA	300 nA	N.A.	**66-157 nA**
CMOS technology	130 nm	180 nm	130 nm,ZVT*****	130 nm	180 nm

*: Valid below 0.8 dBm input power.
**: Differential stage and uses a boost converter (with another external power inductor) in cascade.
***: Measurement reported @ -10 dBm & dc voltage at the output of the rectifier.
****: Only RF rectifier with off-chip matching
*****:Zero Threshold Voltage devices.

integrated on-chip with tuning capability. The process is a standard 0.18 µm CMOS, and the reported sensitivity is for a 1 V output voltage where the system startup happened and the controller is operating and taking a very low current of 66 nA for low oscillator frequency operation and it increases to 157 nA for the highest oscillator frequency. Lower voltage operation and newer technologies, with lower channel length or lower threshold voltage devices, enable better sensitivity.

3.6 Conclusions

A fully integrated system with an LC matching network, RF rectifier, clock generation, voltage reference and power management/control circuitry is presented in this Section 3, yet the system features a self-startup operation with no external supply help. The full integration of all functionalities on a single CMOS chip proves to be a promising low-cost solution. In order to increase the available output power, a novel reconfigurable modu-

lar RF rectifier circuit is presented. The dc power is delivered to the load only, when the voltage on the load can reach the desired voltage; otherwise, the power management waits until this condition is satisfied and delivered power is duty cycled. Moreover, the extra available output power can be stored for future usage. This two-path power delivery scheme enables the support of real-time loads, increases the extracted power from the RF front end, and stores the extra power in external storage elements. For the proof of concept, only one secondary path is used, but multiple secondary paths can be incorporated to enhance the extraction capability of the extra available power at the expense of more complex logic circuits. Finally, a new circuit for non-overlapping level shifters is proposed and used in the design to overcome shoot-through power loss.

4. RF ENERGY HARVESTING FROM OUT-OF-BAND BLOCKERS OF WIRELESS RECEIVERS[1]

4.1 Introduction

Wireless transceivers are a key-enabling building block for Internet of Things (IoT) technology to establish communications between different systems, geographic, vendors, and industries. Due to the expected increase in the number of installed devices for consumer and industrial applications, [48], low-power energy-efficient designs are expected while tolerance of out-of-band blockers should be taken into account. Out-of-band blockers can be large enough, like the GSM communications where an out-of-band 0 dBm blocker is expected to present at a spacing of 80 MHz, to saturate the RF receiver, lower the gain, and increase the Noise Figure (NF).

From another point of view, energy harvesting is expected to be integrated in IoT standards to enable green operation where required power from the IoT nodes is scavenged from ambient sources. Specifically, RF energy harvesting converts the RF ambient electromagnetic waves to useful dc energy. A minimum input signal is a characteristic of these systems and has been analyzed in [42] and Section 2 for integrated CMOS designs with on-chip and off-chip matching networks where charging capacitors take a considerable amount of time at the sensitivity levels. However, in the presence of large RF blockers, the input signal is large enough to operate the system in a more efficient way [8, 29].

In this work, an energy efficient RF wireless receiver system that not only tolerates but leverages the blocker is presented. RF energy harvesting is incorporated by using the high RF power from the blockers and provides demand dc power of the receiver (partially).

[1]Part of this section is reprinted, with permission, from O. Elsayed, M. Abouzied, and E. Sánchez-Sinencio, "A 540 W RF wireless receiver assisted by RF blocker energy harvesting for IoT applications with +18 dBm OB-IIP3," in IEEE Radio Freq. Integr. Circuits Symp. (RFIC), May 2016, pp. 230– 233. ©2016 IEEE.

Thus, the effective power consumption is even lower and the RF receivers can benefit from the available energy of the large blockers.

4.2 Proposed RF System Architecture

The proposed RF system architecture is shown in Fig. 4.1. The antenna receives in-band small signals and large out-of-band blockers. The typical RF receiver chain is shown at the bottom where an LC matching network is used for impedance transformation and . Another rule of the matching network is to filter out to some extent the out-of-band blockers. The proposed system introduces another path for the blocker signal flow where an RF rectifier is used for ac to dc conversion of the RF power. An LC matching network is used to transform the input impedance of the wireless receiver block to the antenna impedance (assume $50\ \Omega$) for maximum power transfer and blocker signal selection due to the bandpass nature of the input impedance $Z_{in,REC}$. The ripple on the output voltage V_{OUT} is filtered by an off-chip capacitor C_L, and V_{OUT} is used to supply the wireless receiver with dc power as a recycling process of the RF blocker. Thus, although the RF blockers are considered non-desirable signals for their effects on the traditional receivers, they can be used in the proposed system to assist the wireless receiver, lower it effective power consumption or even going batteryless design as an ultimate goal. The same antenna is used for concurrent reception of both signals: the receiver and blocker signals.

4.3 Proposed Differential RF Rectifier with Integrated Passives

RF energy harvesting consists of an on-chip matching network and a differential cross-coupled [5] two-stage RF rectifier as shown in Fig. 4.2. The analysis part will focus on the cross coupled stage and derive the equations for the output dc voltage versus the input swing for different output currents, the input impedance $Z_{in,stage}$, and the power conversion efficiency (PCE) which is defined as the output dc power divided by the input fundamental ac power.

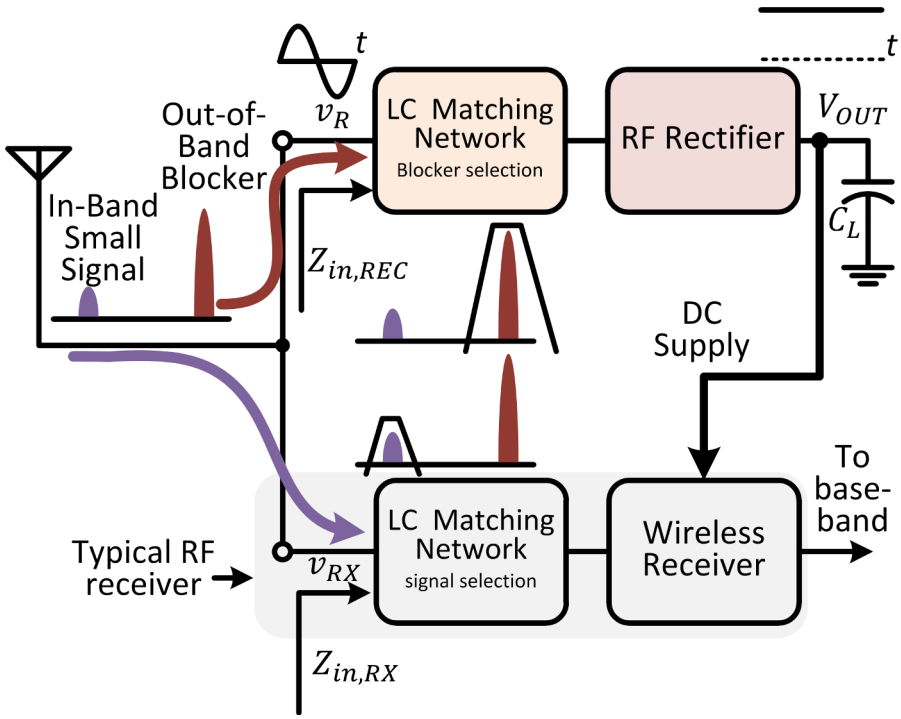


Figure 4.1: Proposed RF system comprising of RF receiver assisted with out-of-band blocker RF energy harvesting.

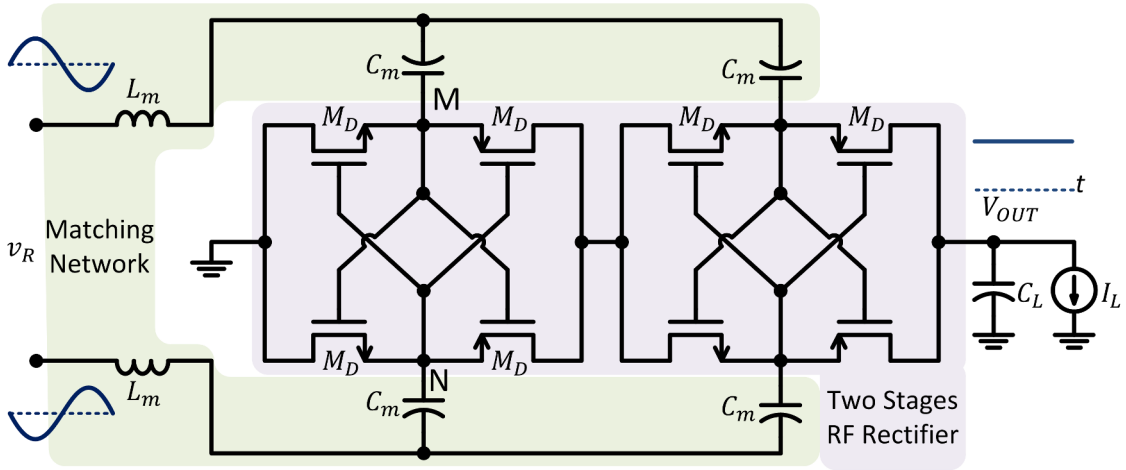


Figure 4.2: Proposed RF energy harvesting front end comprising of matching network and RF rectifier.

4.3.1 Architecture of the RF Energy Harvesting Front End

Two series inductors are used to match the RF rectifier to the out-of-band frequency range. Differential design is chosen due to the balanced nature of the wireless receiver design. The RF energy harvesting should present high input impedance for in-band signals (not to affect the matching of the receiver and Noise Figure) and an input impedance of 50 Ωfor the out-of-band frequency range of the blockers as shown in Fig. 4.3a. As illustrated on the Smith chart of Fig. 4.3b, for the in-band frequency range which is marked with circle markers, the input impedance of the wireless receiver $Z_{in,RX}$ is $50\ \Omega$ while the input impedance of the RF rectifier $Z_{in,REC}$ is high impedance, and it is capacitive by nature as will be explained in Section 4.3.2. For the out-of-band frequency range which is marked with square markers, $Z_{in,RX}$ is now high impedance, and inductive according to our simulations, and $Z_{in,REC}$ is matched for maximum power transfer.

The RF rectifier does ac to dc conversion of the out-of-band blockers. It is a two-stage design in order to maximize the PCE. However, this affects the minimum detectable signal of the rectifier. The analysis of each stage is shown in the next Section 4.3.2.

4.3.2 Analysis of the Differential RF Rectifier

The cross-coupled structure, as shown in Fig. 4.4a, is composed of: two parallel voltage clampers and two half-wave rectifiers. The former consists of capacitor, C_m, and device, M_{D1}, and the latter consists of capacitor, C_m, and device, M_{D2}, with output signals, M and N, respectively. The capacitors, C_m, works as a short for high frequency and opens for dc values. Assuming an input voltage waveform $v_{in} = A\cos(\omega_B t)$, the signals, M and N, have a dc shift and sinusoidal parts superimposed on that dc shift which are out of phase. The two half-wave rectifiers are: devices, M_{D3} and M_{D4}, and capacitor, C_{out}. They work as ac to dc converters with out-of-phase operation as well. The output voltage V_{REC} is dc voltage with ripple at twice the operation frequency ω_B. Due to symmetry, the

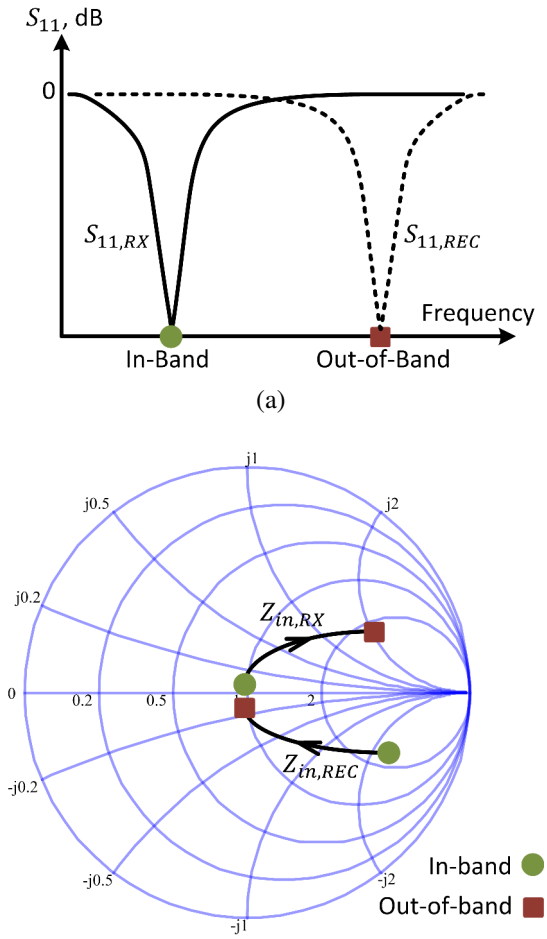
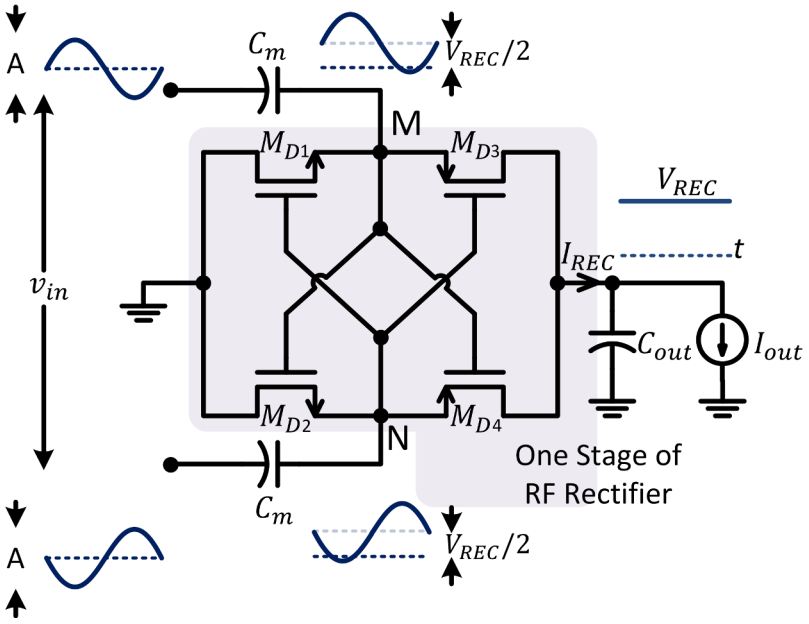
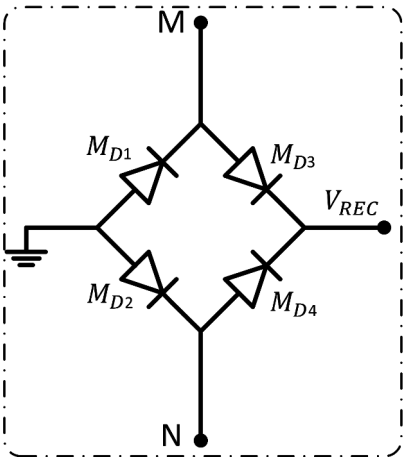


Figure 4.3: In-band and out-of-band input interface: (a) desired reflection coefficient S_{11} for the receiver and the rectifier at different bands and (b) smith chart different input impedance for different frequencies.



(a)



(b)

Figure 4.4: One stage of the RF rectifier: (a) CMOS realization and (b) typical full bridge diode implementation.

dc shift at M and N is $V_{REC}/2$.

The arrangement of the devices M_{D1}, M_{D2},M_{D3}, and M_{D4} can be viewed as the typical full bridge rectifier [49], as shown in Fig. 4.4b. Instead of connecting the gate to the drain of each device, in the diode implementation of the full ridge circuit, cross-coupling between the nodes M and N is used. If device M_{D3} is considered, the gate voltage N is out of phase from the source voltage M. So, when the device is conducting (not conducting), the voltage M is the highest (lowest) while the voltage N is the lowest (highest) voltage, which helps to create a better on (off) resistance of the switch. That way, the cross-coupling is thought to introduce better switches/diodes.

In this part, the analysis of this structure is done assuming a sinusoidal voltage at the input of the RF rectifier. This is done for the sake of deriving behavioral trends for the operation although the correct way to analyze this structure in the case of the high power operation, which is the intended mode of operation in this work, is to assume sinusoidal current and the voltage waveform will deviate from the sinusoidal operation. To find the input/output governing equations of the devices, the starting point is the equation of weak-inversion NMOS [31]:

$$I_{DSn} = \mu_n C_{ox} \phi_t^2 \frac{W}{L} \exp\left(\frac{(V_{GS} - V_T)}{n\phi_t}\right) \left\{1 - \exp\left(-\frac{V_{DS}}{\phi_t}\right)\right\}, \tag{4.1}$$

where I_{DSn} is the current through the channel of the transistor with its positive direction from drain to source; μ_n is the mobility of the carriers; C_{ox} is the capacitance of the oxide layer per unit area; W is the channel width; L is the channel length, and ϕ_t is the thermal voltage ($\phi_t = KT/q$), which equals to 26 mV at room temperature. n is the slope factor; V_T is the threshold voltage; V_{GS} is the gate-source voltage or the control voltage of the channel, and V_{DS} is the drain-source voltage (the voltage across the channel with the direction of the current). Although the slope factor deviates from the value 1 as was

discussed in [42], Section 2, for the sake of simplicity here, it is assumed to be 1. Thus,

$$I_{DSn} = I_B \left\{ \exp\left(\frac{V_{GS}}{\phi_t}\right) - \exp\left(\frac{V_{GD}}{\phi_t}\right) \right\}, \tag{4.2}$$

where $I_B = \mu_n C_{ox} \phi_t^2 \frac{W}{L} \exp\left(-V_T/n\phi_t\right)$, and it is the design parameter for the device with the proper choice of W/L. For a PMOS, the equation should be:

$$I_{DSp} = I_B \left\{ \exp\left(\frac{V_{SG}}{\phi_t}\right) - \exp\left(\frac{V_{DG}}{\phi_t}\right) \right\}. \tag{4.3}$$

4.3.3 Derivation of the Output Voltage V_{REC} (DC operation)

The currents that follow through the devices M_{D3} and M_{D4} are:

$$I_{DS3} = I_B \left\{ \exp\left(\frac{A}{\phi_t}\cos\left(\omega_B t\right)\right) - \exp\left(\frac{V_{REC}}{2\phi_t}\right) \exp\left(\frac{A}{2\phi_t}\cos\left(\omega_B t\right)\right) \right\}, \tag{4.4}$$

$$I_{DS4} = I_B \left\{ \exp\left(\frac{-A}{\phi_t}\cos\left(\omega_B t\right)\right) - \exp\left(\frac{V_{REC}}{2\phi_t}\right) \exp\left(\frac{-A}{2\phi_t}\cos\left(\omega_B t\right)\right) \right\}. \tag{4.5}$$

Writing KCL at the output node yields:

$$I_{REC} = 2I_B \left\{ \cosh\left(\frac{A}{\phi_t}\cos\left(\omega_B t\right)\right) - \exp\left(\frac{V_{REC}}{2\phi_t}\right) \cosh\left(\frac{A}{2\phi_t}\cos\left(\omega_B t\right)\right) \right\}, \tag{4.6}$$

where the dc component corresponds the output current I_{out}. Using modified Bessel functions $\mathrm{I_m}\left(x\right)$ which are discussed in [32],

$$e^{\pm x\cos(\omega_0 t)} = \mathrm{I_0}\left(\pm x\right) + 2\sum_{n=1}^{\infty} \mathrm{I_n}\left(\pm x\right)\cos\left(n\omega_0 t\right), \tag{4.7}$$

and the relationship in [32]:

$$\cosh\left(x\cos\left(\omega_0 t\right)\right) = \mathrm{I}_0\left(x\right) + 2\sum_{n=even}^{\infty}\mathrm{I}_\mathrm{n}\left(x\right)\cos\left(n\omega_0 t\right). \tag{4.8}$$

Thus, using (4.8) and substitute in (4.6) yields,

$$V_{REC} = 2\phi_t \ln\left(\frac{\mathrm{I}_0\left(\frac{A}{\phi_t}\right) - \frac{I_{out}}{2I_B}}{\mathrm{I}_0\left(\frac{A}{2\phi_t}\right)}\right). \tag{4.9}$$

4.3.4 Derivation of the Input Impedance Z_{stage} and PCE (AC operation)

The input ac impedance can be modeled as a parallel R-C network where the parallel resistance is R_{stage}, the admittance B_{stage} and the parallel capacitance is C_{stage}. The capacitance is due to bottom plate capacitance C_{bottom} of C_c, and to the equivalent gate capacitance C_B of the devices used. The gate capacitance $C_B \approx C_{ox}WL$. Thus,

$$C_{stage} \approx C_{inter} \approx 2C_B + C_{bottom} \approx 2C_{ox}WL + C_{bottom} \approx 2C_{ox}WL. \tag{4.10}$$

The currents that follow through the devices M_{D1} is:

$$I_{DS1} = I_{DS4}, \tag{4.11}$$

Writing KCL at the either of intermediate nodes, here chosen to be M, yields,

$$i_{in} = 2I_B\left\{\sinh\left(\frac{A}{\phi_t}\cos\left(\omega_B t\right)\right) - \exp\left(\frac{V_{REC}}{2\phi_t}\right)\sinh\left(\frac{A}{2\phi_t}\cos\left(\omega_B t\right)\right)\right\}, \tag{4.12}$$

where the fundamental component corresponds the fundamental input current i_{in}. Using the relationship in [32]:

$$\sinh\left(x\cos\left(\omega_0 t\right)\right) = 2\sum_{n=odd}^{\infty} \mathrm{I_n}\left(x\right)\cos\left(n\omega_0 t\right), \tag{4.13}$$

and substitute in (4.12) yields the following expression for the input admittance,

$$B_{stage} = \frac{2I_B}{A}\left\{\mathrm{I_1}\left(\frac{A}{\phi_t}\right) - \exp\left(\frac{V_{REC}}{2\phi_t}\right)\mathrm{I_1}\left(\frac{A}{2\phi_t}\right)\right\}. \tag{4.14}$$

Fig. 4.5 shows the plots of the output voltage V_{REC} and the input resistance $1/B_{stage}$ versus the normalized current I_{out}/I_B for different values of input amplitude A. For the evaluation of B_{stage}, the value of I_B is chosen to be 1 nA. The quality factor can be expressed by:

$$Q_{stage} = \frac{\omega_B C_{stage}}{B_{stage}}. \tag{4.15}$$

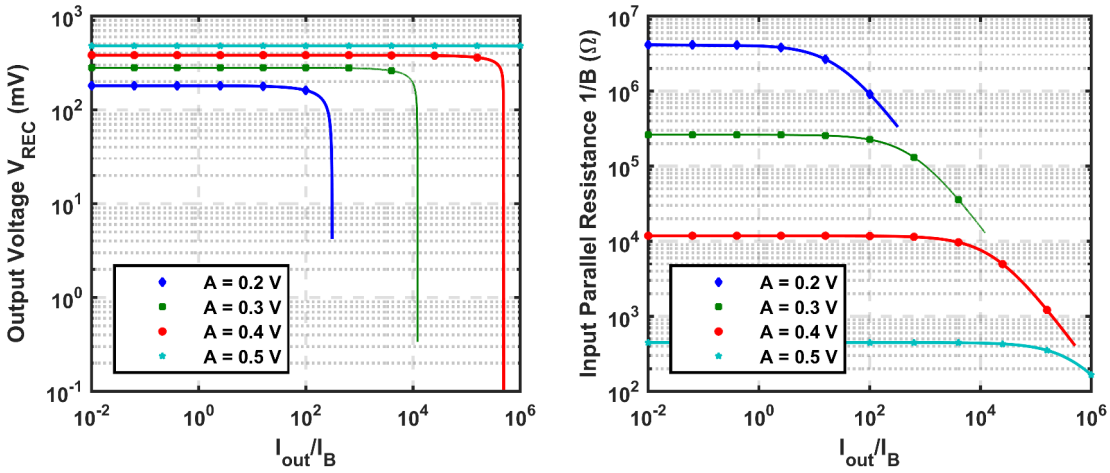
The PCE can be derived using (4.9) and (4.14):

$$PCE = \frac{V_{REC} I_{REC}}{A^2 B_{stage}}. \tag{4.16}$$

4.3.5 Compare to Diode-Connected Devices (no Crosscoupling)

Repeating the above procedure to obtain the dc operation shows that the first term in 4.6, which has the form of$\cosh\left(\frac{A}{\phi_t}\cos\left(\omega_B t\right)\right)$, yields 1 and

$$I_{REC,diodes} = 2I_B\left\{\exp\left(\frac{-V_{REC}}{2\phi_t}\right)\cosh\left(\frac{A}{2\phi_t}\cos\left(\omega_B t\right)\right) - 1\right\}, \tag{4.17}$$



(a) (b)

Figure 4.5: Model results for one-stage of the cross-coupled RF rectifier versus the normalized current I_{out}/I_B for different input amplitudes A where (a) is the output voltage V_{REC} and (b) is the input resistance $1/B_{stage}$.

Thus, using (4.8) and substitute in (4.17) yields,

$$V_{REC,diodes} = 2\phi_t \ln\left(\frac{\mathrm{I}_0\left(\frac{A}{2\phi_t}\right)}{1+\frac{I_{out}}{2I_B}}\right). \tag{4.18}$$

Repeating the above procedure to obtain the ac operation shows that the first term in 4.12, which issinh $\left(\frac{A}{\phi_t}\cos\left(\omega_B t\right)\right)$, vanishes and

$$i_{in} = 2I_B \exp\left(\frac{-V_{REC}}{2\phi_t}\right)\sinh\left(\frac{A}{2\phi_t}\cos\left(\omega_B t\right)\right), \tag{4.19}$$

which yields the following expression for the input admittance,

$$B_{stage,diode} = \frac{2I_B}{A}\exp\left(\frac{-V_{REC}}{2\phi_t}\right)\mathrm{I}_1\left(\frac{A}{2\phi_t}\right). \tag{4.20}$$

When the values of $V_{REC,diodes}$ from (4.18) are evaluated, they are always less than V_{REC} for the same diodes and same output current I_{out}. Also, the input resistance $1/B_{stage,diode}$ is always higher than $1/B_{stage}$. There fore, the cross-coupled differential RF rectifier is used in this work.

4.4 Top-Level System Simulations

The overall system is simulated using harmonic balance to characterize the system before sending the design for fabrication. Fig. 4.6 shows the gain G and NF of the receiver, the reflection coefficient S_{11}at the antenna port, and the harvested power $P_{harvest}$ while sweeping the out-of-band blocker power. The reflection coefficient S_{11} is simulated at the in-band signal which shows a good match across the different blocker powers. The following discussion compares the characteristics when there is no blocker and in the presence of 0 dBm blocker. The gain G is reduced by 3 dB due to the compression of the chain of the receiver. As noted, while the blocker power increases, the gain drops then, it increases and decreases again. This effect is due to the operation of the RF rectifier, at this power range, the rectifier starts to supply current to the receiver where the output voltage is initially below the intended supply voltage and introduces gain expansion. The NF degrades with the presence of the large blockers by 4 dB due to large signal operation and gain compression as well. The RF rectifier can supply 300μW in the case of 0 dBm blocker.

4.5 Experimental Results

The design was fabricated on CMOS 180 nm technology and the die photo is shown in Fig. 4.7. The RF energy harvesting front end takes 930x760 μm^2. This area include the LC matching network area. The system is first tested with a small signal input at the receiver band. Then, the system is tested with a small signal input at the receiver band (900MHz) and a large signal blocker with variable power level at the blocker frequency (80 MHz

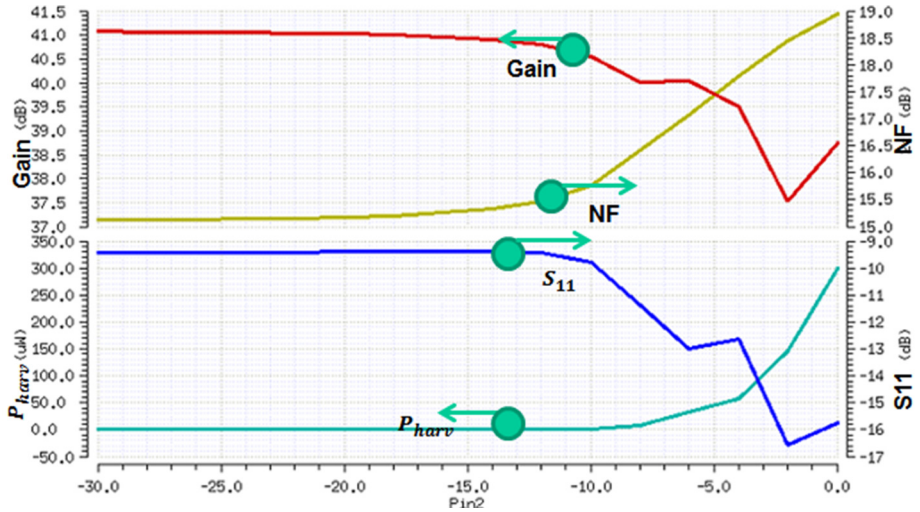


Figure 4.6: Proposed system simulations for different out-of-band blocker levels.

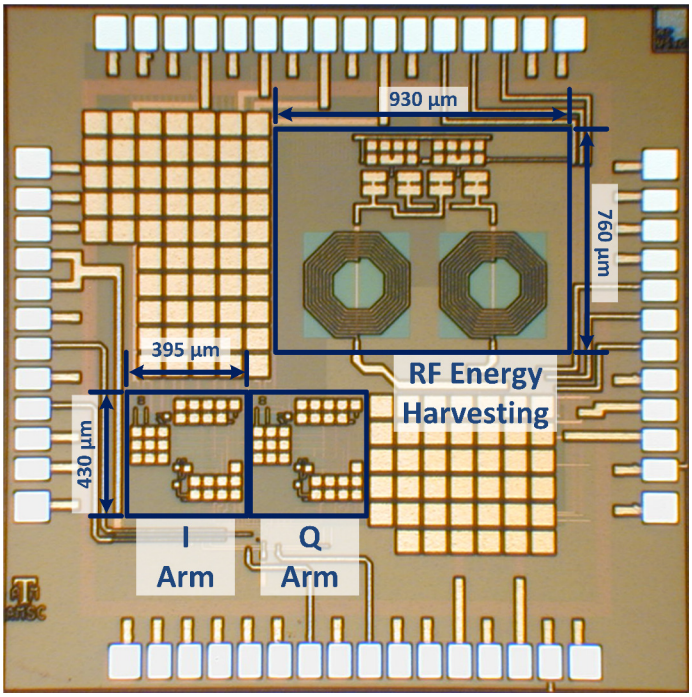


Figure 4.7: Chip micrograph of the proposed RF system.

offset). The gain of the receiver drops by 2 dB at 0 dBm blocker. The NF is 18.5 dB at low/no blocker power case and increases to 34 dB at 0 dBm blocker. Due to spur mixing of the receiver, the NF at large blockers increases as expected. The output harvested dc power of the RF rectifier versus blocker power is shown in Fig. 4.8. For low blocker levels, the control of the system (not shown here and published in [50]) doesn't take power from the RF rectifier. When the output voltage is sufficient for the receiver operation, reaches 1V, while providing a minimum current, in the range of hundreds of μA, the control starts to enable the dc power flow from the RF rectifier to supply the wireless receiver. The RF rectifier can provide 246 μW at 1.7 dBm blocker.

The reflection coefficient S_{11} of the total system at the antenna interface is shown in Fig. 4.9. Two matching frequencies can be observed one at 900 MHz which is the signal band while another match at 980 MHz is used for the blocker band which is present due to the insertion of the RF energy harvesting front end.

The supply voltage for the wireless receiver is 1 V and the receiver core (mixer, filter and TIA) power consumption is 534 μW. In the presence of 1.7 dBm blocker, the output dc power of the RF rectifier (P_{REC}) is 246 μW (46% of the power requirement of the receiver core) so the power consumption from the main supply of the receiver is reduced to 288 μW.

4.6 Summary

The proposed system introduces a wireless receiver with RF energy harvesting and proves the possibility of the co-existence between two systems, yet using the same antenna source. The RF energy harvesting from out-of-band blockers is a way to recycle the high power to be used for powering-up the wireless receiver itself. The interaction between both subsystems should be taken into account and each should have minimal effect on the operation of the other in each band of interest. Finally, in the presence of 1.7 dBm

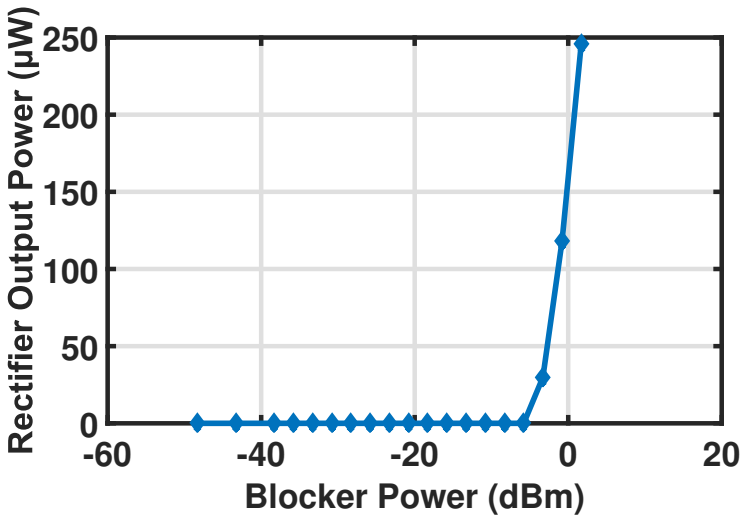


Figure 4.8: Measured rectifier output power versus blocker power

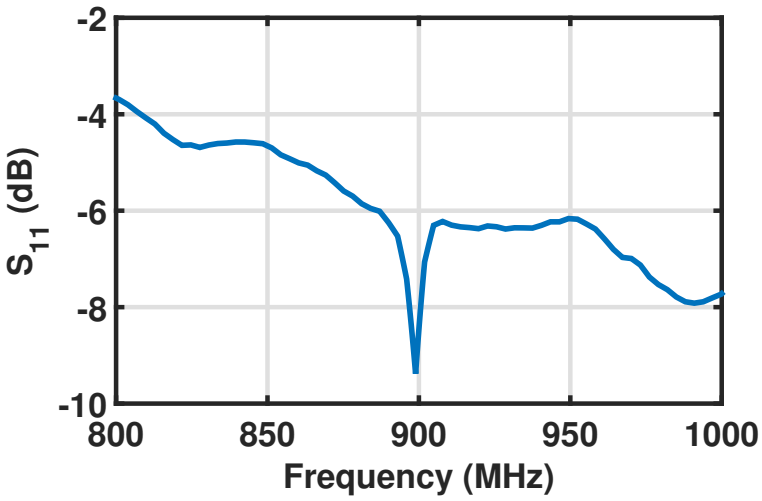


Figure 4.9: Measured receiver S_{11}

blockers, the measurements shows that 46% of the power of the core receiver is supplied by the RF energy harvesting and the ultimate goal is to design batteryless designs in the future.

5. BATTERY-ASSISTED RF ENERGY HARVESTING UNIT WITH A NEW ANTENNA

5.1 Introduction

A typical RF energy harvesting system is shown in Fig. 5.1. An off-chip antenna

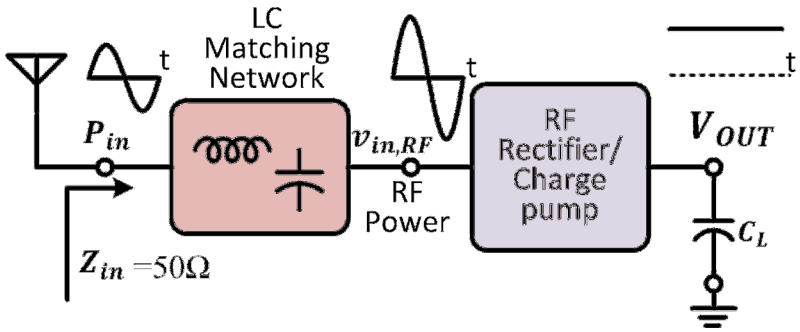


Figure 5.1: A general RF energy harvesting system incorporating antenna.

captures the RF electromagnetic signals and converts these signals to electrical ac signals. The available power from the antenna is P_{in}. The ac signals $v_{in,RF}$ are rectified with the use of a RF rectifier/charge pump to an output dc output V_{OUT}. Maximum power extraction from the antenna is achieved with the use of an intermediate LC matching network. The antenna interface is typically chosen to be $50\,\Omega$ which is a balance between maximum efficiency and maximum bandwidth (BW).

The nature of the input impedance of the RF rectifier is a series RC, the real part is very small (using a parallel RC with the real part is very large). Thus, the transformation ratio of the matching network would be very high and the matching network introduces losses. Eliminating the use of matching networks can potentially boost the efficiency of the total system. In [29], co-design of a CMOS rectifier with a small loop antenna is done.

Moreover, for the CMOS rectifier, the performance is highly dependent in the threshold voltage of the diode-connected transistors used. In order to compensate for this voltage drop, assistance from external batteries is needed or the use of internal feedback.

Here, in this work, RF energy harvesting with direct conjugate match between antenna and RF rectifier is investigated as shown in Fig. 5.2. A new antenna suitable for RF energy

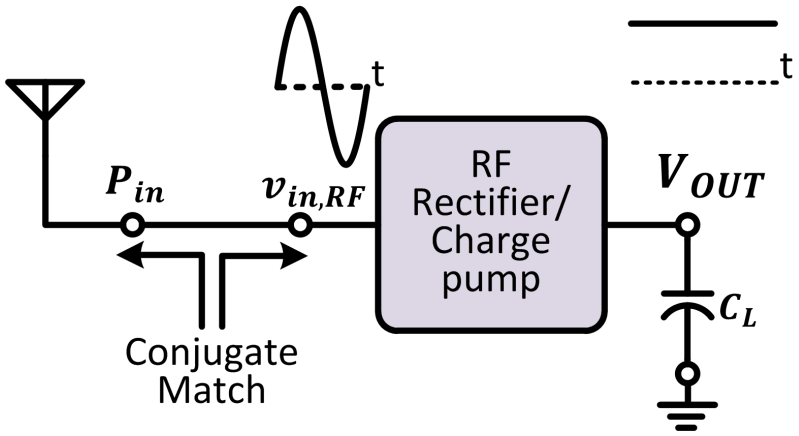


Figure 5.2: Proposed direct matching RF energy harvesting system.

harvesting is proposed with low series resistance and high inductive part through the use of T-match design. The RF rectifier is statically compensated with the assistance of external battery source.

Moreover, a typical design with an on-chip matching network with the same parameters and a $50\,\Omega$ termination is investigated and compared.

5.2 Antenna Performance Parameters

Antennas are critical elements in RF energy harvesting. In the transmitting mode, a desired current distribution is excited at the antenna surface and from that, wave propagation occurs (due to the principle of duality, the opposite happens in the receiving mode and

either modes can be used to analyze antennas according to ease of use). To characterize the antennas, different parameters are used and shown in Fig. 5.3 [51]. There are circuit

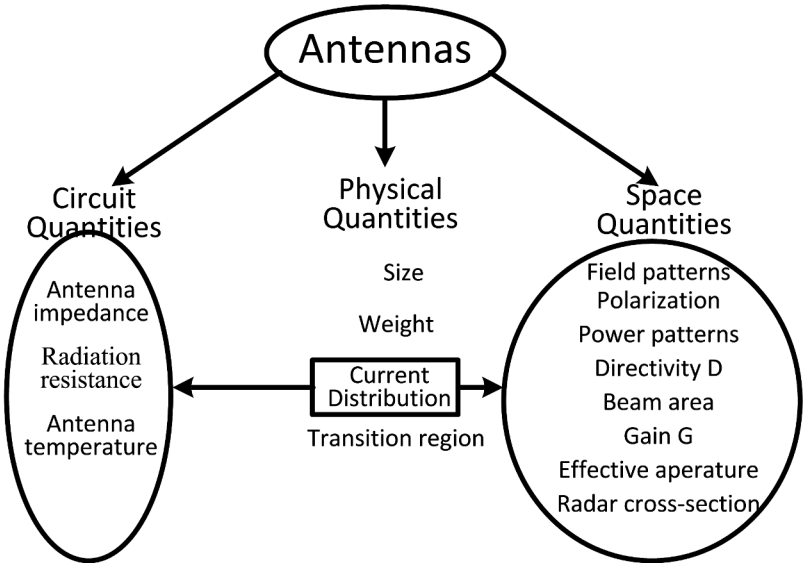


Figure 5.3: Antenna performance parameters.

quantities related to the antenna interface to the feed lines with are connected to different circuits (in our case, an RF rectifier). Also, there are spatial quantities that define the distributions of the propagated waves in space. Finally, physical quantities of the antenna that are visible by human eye and these are the antenna parameters that can be changed to achieve certain circuit and spatial quantities.

- Antenna Impedance Z_A: The input impedance at the antenna terminals:

$$Z_A = R_A + jX_A = R_r + R_o + jX_A, \tag{5.1}$$

where R_A is the real part of the total antenna impedance, X_A is the imaginary part of the total antenna impedance, R_r is the radiation resistance which is the good

resistance that transform electric power to electromagnetic propagation, andR_o is the losses, ohmic resistance, associated with the antenna structure. The antenna efficiency is defined as:

$$e_r = R_r/(R_r + R_o) = R_r/R_A. \tag{5.2}$$

- Radiation Pattern $F(\theta, \phi)$: Angular variation of radiation around the antenna

$$F(\theta, \phi) = \frac{E_\theta}{E_\theta(\text{max})}, \tag{5.3}$$

$$F(\theta, \phi) = g(\theta, \phi) f(\theta, \phi), \tag{5.4}$$

where $g(\theta, \phi)$ is the element factor and $f(\theta, \phi)$ is the pattern factor. The pattern factor is the integration over the current and is strictly due to the distribution of current in space. The element factor is the pattern of an infinitesimal current element in the current distribution. Finally, the power pattern $P(\theta, \phi)$ is:

$$P(\theta, \phi) = |F(\theta, \phi)|^2 . \tag{5.5}$$

- Directivity D: Ratio of power density in the direction of pattern peak to the average power density at the same distance from the antenna.

- Gain G: is defined as

$$G = e_r.D, \tag{5.6}$$

which is the value of directivity reduced by the losses of the antenna.

- Polarization: the instantaneous direction of the electric field vector associated with

the radiation from an antenna when transmitting. There are linear, circular, and elliptical polarizations. The factor p is the polarization mismatch between the polarization of the transmitting and receiving antennas in the wireless link. For a two linearly polarized (LP) antennas, $p = \cos^2(\Delta\tau)$. For two circularly polarized (CP) antennas with the same sense and different senses, $p = 1$ and $p = 0$ respectively. Finally, for a LP antenna with a CP antenna, $p = 1/2$.

- Bandwidth: range of frequencies over which important performance parameters are acceptable.

5.3 RF Energy Harvesting System

5.3.1 Antenna Design

The design of the antenna is based on a folded dipole. A simple $\lambda/2$ dipole has a radiation resistance of 70 Ω. With folding that dipole, i.e. using another parallel $\lambda/2$ dipole near to the original one, a folded dipole is formed and the radiation resistances higher and approaches 300 Ω. A folded dipole is shown in Fig. 5.4 with a gamma match

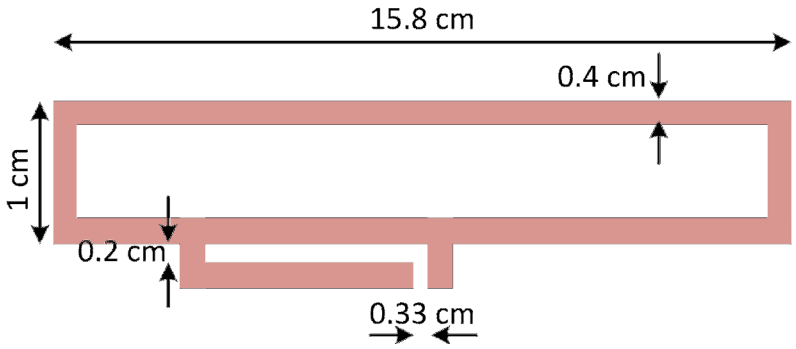


Figure 5.4: Proposed antenna design.

[51, 52]. A folded dipole is a balanced structure where differential signals shall be used to

eliminate unwanted imbalance current. Using single ended signaling (since the rectifier is a single ended design) needs the use of a Balun for unbalanced to balanced transformation. A gamma match is suitable for that.

To analyze the folded dipole, it can be decomposed into a transmission line (even) mode and an antenna (odd) mode. Fig. 5.5 shows the currents of the two modes. An input

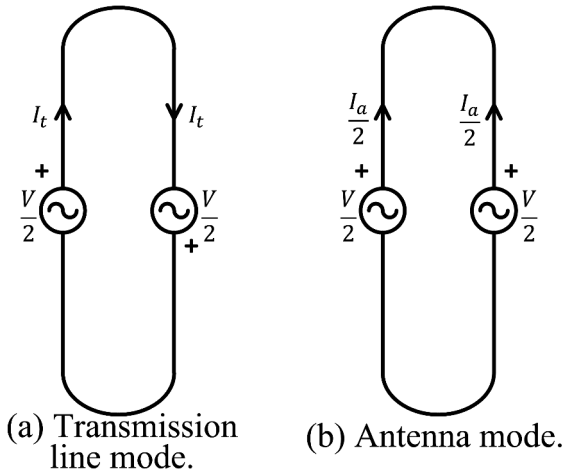


Figure 5.5: Decomposition of the excitation into two modes.

voltage difference V excitation can be decomposed into $+V/2$ and $+V/2$ for the first dipole . For the parallel dipole, no explicit excitation there, so $+V/2$ and $-V/2$ cancels each other. On the first dipole and the parallel dipole, $+V/2$ and $+V/2$ ($-V/2$) contributes to the transmission line (antenna) mode respectively where the principle of superposition has been used in this decomposition. The input impedance for the transmission line mode for each dipole is the input impedance of a short-circuit transmission line which is given by:

$$Z_t = jZ_o \tan\left(\beta \frac{L}{2}\right), \tag{5.7}$$

where Z_o is the characteristic impedance of the transmission line, $\beta = \frac{2\pi}{\lambda}$, λ is the wave-

length in the medium of the transmission line, and L is the length of the dipole. In the far field, the two dipoles are parallel where each has the antenna mode input impedance Z_d for a typical dipole of the same length. Thus for the transmission line mode,

$$I_t = \frac{V}{2Z_t}, \tag{5.8}$$

and for the antenna mode,

$$I_a = \frac{V}{2Z_d}. \tag{5.9}$$

Thus, the input impedance of the folded dipole at the excitation point is given by:

$$Z_A = \frac{V}{I_t + \frac{1}{2}I_a} = \frac{4Z_tZ_d}{Z_t + 2Z_d} = \frac{2}{\frac{1}{2Z_d} + \frac{1}{Z_t}}. \tag{5.10}$$

For a half-wavelength folded dipole, $Z_t = \infty$ and (5.10) reduces to:

$$Z_A = 4Z_d \ \left(L = \frac{\lambda}{2}\right). \tag{5.11}$$

Since Z_A is complex as in (5.10), the use of less than $\lambda/2$ dipole gives an inductive part. This inductive part can be tuned for the required input impedance.

5.3.2 RF Rectifier

An N-stage RF rectifier is shown in Fig. 5.6. The ac input power is rectified through each stage and the dc output of each is fed to the next one. Each stage is composed of a clamper and a half wave rectifier. The output of the clamper is V_{inter} which is shifted by dc voltage proportional to the input amplitude and the value of DC_{in} and inversely proportional to the output dc current. The output of the half-wave rectifier is a dc voltage $V_{out,DC}$ with a small ripple. Assuming ideal diodes, Fig. 5.7 shows the expected waveforms at different nodes. The voltage drop V_d for actual diodes will affect the output voltage as

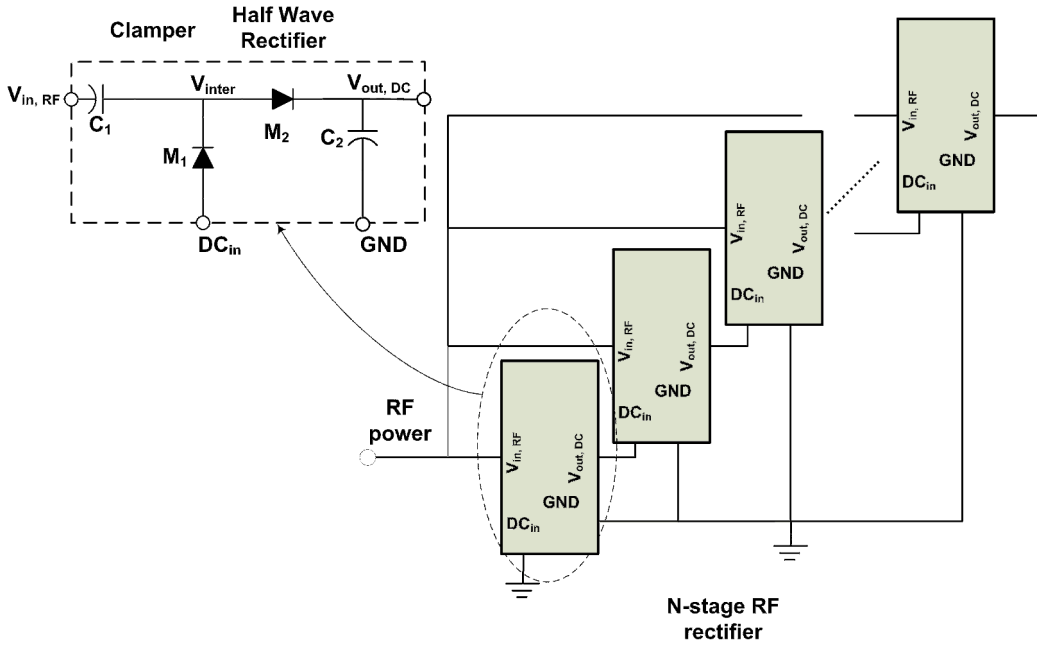


Figure 5.6: RF rectifier as a cascade of N-stages.

shown in Fig. 5.8. The proposed static bootstrapping technique is demonstrated in Fig. 5.9. The body is connected to the drain for the following reasons: during forward biasing, the objective is to reduce conduction losses. When M1 (same argument for M2) is forward biased, the source of the MOS is as indicated (V_{inter} node) and V_{inter}should be less than the DC_{in}voltage by the threshold voltage. So, the body is not tied to the source, but tied to a higher voltage. So, the body to source junction is biased and the threshold voltage is lowered from V_{TH0} and the threshold voltage expression:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{5.12}$$

where V_{SB} is the is the source body substrate bias, $2\phi_F$ is the surface potential, V_{TH0} is threshold voltage for zero substrate bias, and $\gamma = (t_{ox}/\epsilon_{ox})\sqrt{2q\epsilon_{si}N_A}$ is the body effect parameter, t_{ox} is oxide thickness, ϵ_{ox} is oxide permittivity, ϵ_{si} is the permittivity of silicon,

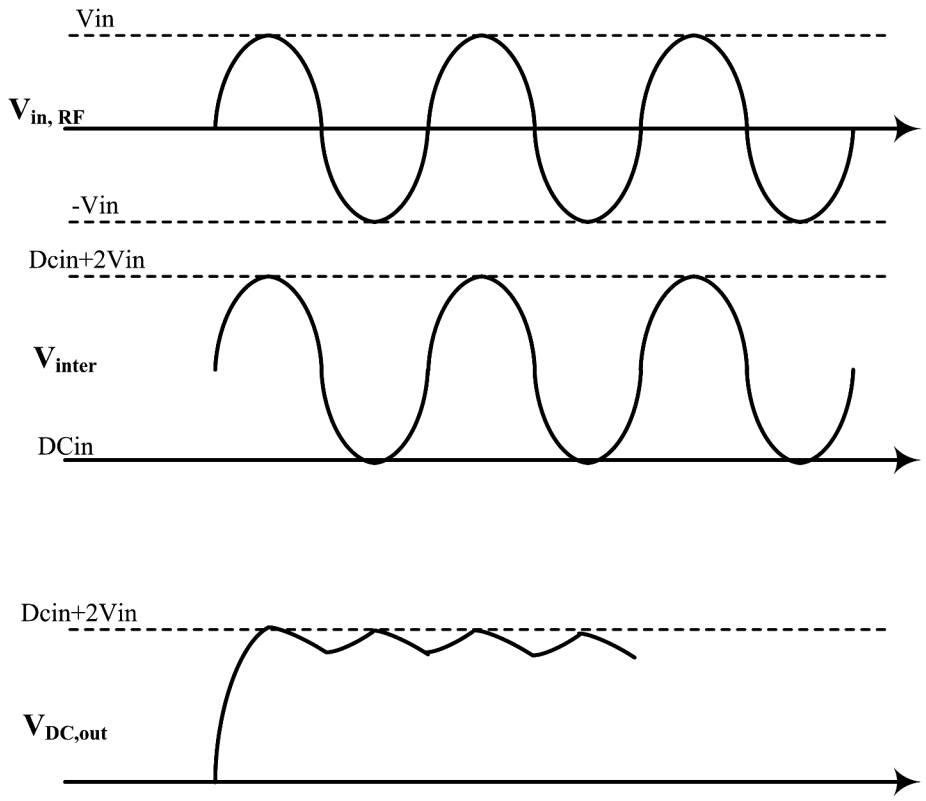


Figure 5.7: Waveforms at different nodes for ideal diodes.

N_A is a doping concentration, and q is the charge of an electron. During reverse biasing, the objective is to reduce leakage losses which are the second reason. When M1 (same argument for M2) is reverse biased, i.e. V_{inter} is higher than DC_{in}, the source and drain nodes are interchanged and the source should be the node DC_{in}. In this phase, the body is connected to the source which is the lowest voltage across the MOS M1, so the threshold voltage should be V_{TH0} which is high. This would enhance the reverse blocking of current. Diode connected transistors suffer from the conduction loss which mandates a minimum sensitivity on the received power to be used for harvesting. This can be understood by the fact that the diodes have a threshold voltage drop which is in the range of 0.5V according to the process. Using diode connected zero threshold transistors can solve the problem

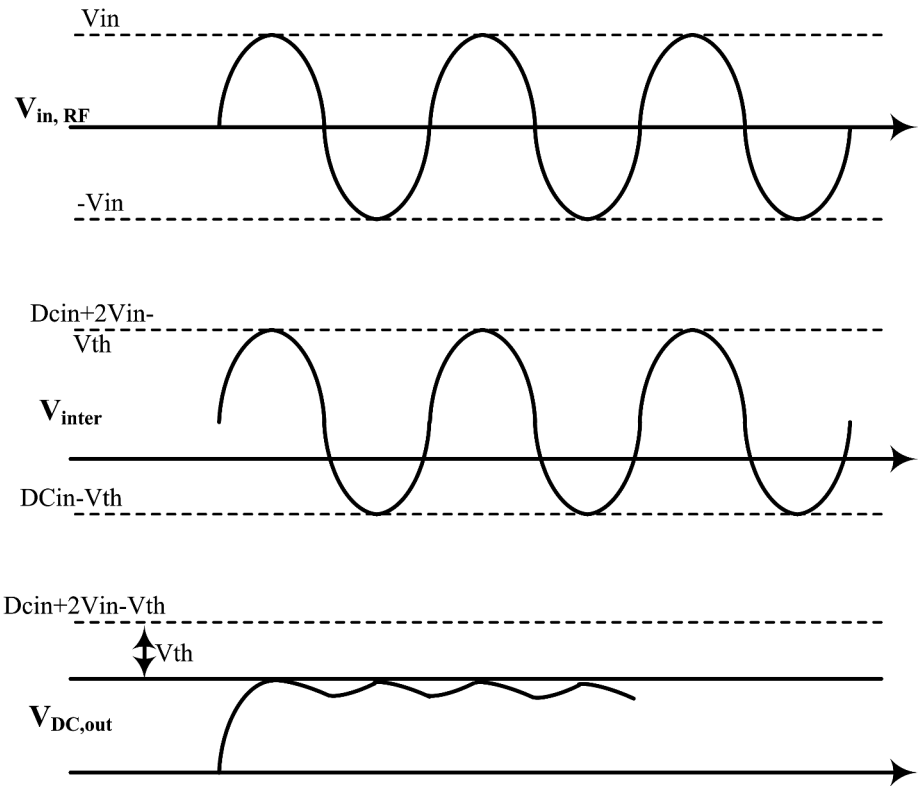


Figure 5.8: Waveforms at different nodes for actual diodes with a predefined V_{TH}.

of conduction loss. But on the other hand, reverse leakage currents exist which increases the losses in the charge pump. This will lead to degraded power efficiency. Thus, using an optimal voltage difference (battery) between the gate and the drain is a solution to the reverse losses while conducting at low powers (of course, a little higher than zero threshold transistors). The effective threshold voltage is tuned by the effective battery. To generate this voltage difference, Fig. 5.9 shows another diode-connected transistor with an external small current that can generate the required voltage difference. Tuning can be done by the value of the external current. A capacitor is needed to stabilize the dc voltage. The usage of NMOS and PMOS in this way minimizes the stray capacitance at the intermediate node. The body is tied to the node that connected to the gate.

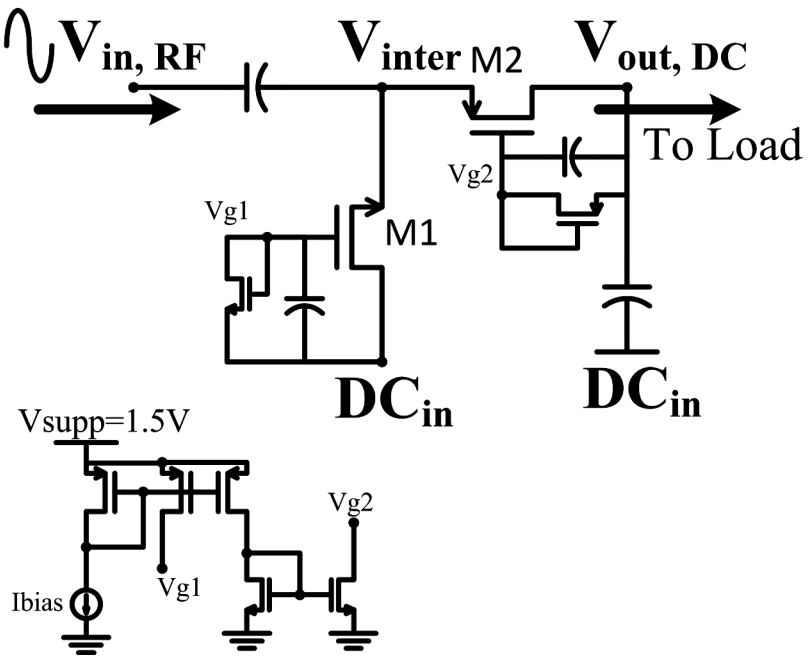


Figure 5.9: Proposed static bootstrapped diodes in one stage of the RF rectifier.

5.3.3 Matching Network for the Typical Design

In order to match the highly capacitive input impedance of the RF rectifier to the antenna impedance, a matching network is shown in Fig. 5.10. The inductance L_{M1} is at a low quality factor node where the quality factor of L_{M1} can be low. However, the opposite is for inductor L_{M2} and a high quality factor is important for this component. The values of L_{M1} and L_{M2} are 11.88 nH and 35 nH respectively. The tunable capacitors C_{BM1} and C_{BM2} are 0.8$-$5.68 pF and 100$-$300 fF respectively.

5.4 Experimental Results

The proposed RF energy harvesting front ends were designed and fabricated using 0.18 μm CMOS technology. The die photo is shown in Fig. 5.11, the chip area is 1.5x1.5 mm^2. Two designs are tested: Design1 uses an external antenna with conjugate match and Design2 has an integrated matching network, shown in Fig. 5.10, with a 50 Ω termination.

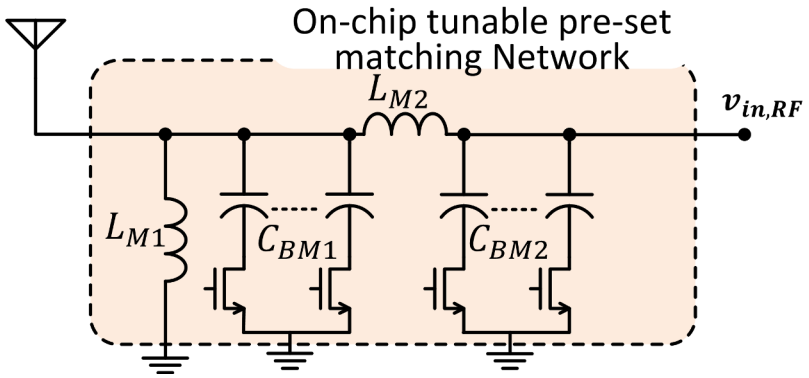


Figure 5.10: On-chip matching network for a typical RF energy harvesting system.

For testing purposes, the nominal load presented to the RF rectifier should be regulated to 1 V by the proper load resistance. In order to present that load, shunt regulators (current sink regulators) can be used. However, the available regulators are intended for higher voltages and currents. Moreover, they lack the ability to measure current. The circuit shown in Fig. 5.12a uses an amplifier in unity feedback and depends on the output stage of the amplifier to sink current., but no current measurement can be achieved. The proposed load in Fig. 5.12b incorporates a transistor (here, BJT, although MOS can be used) in the feedback loop. By tapping the nodeV_m to another matched device, the current can be measured independently using NI DAQ. For wide-range current measurements, a dedicated current log-amplifier, such as LOG114 [53], may be used. The proposed test setups for Design1, Design2, and the available power at the receiver are shown in Fig. 5.13. If the transmitted power is 20 dBm and two 50 Ω antennas, MSC-AT50-XXX, are used, the available power of the receiver, while changing the distance d_3 between the transmitter and receiver, was done in the lab and is shown in Fig. 5.14. The dc rectified voltage after the RF rectifier is shown in Fig. 5.15. As the distance increases, the rectified voltage decreases since the available power decreases. A nonlinear behavior for this indoor measurement is observed which can be attributed to fading and scattering from other metal objects in the lab. The

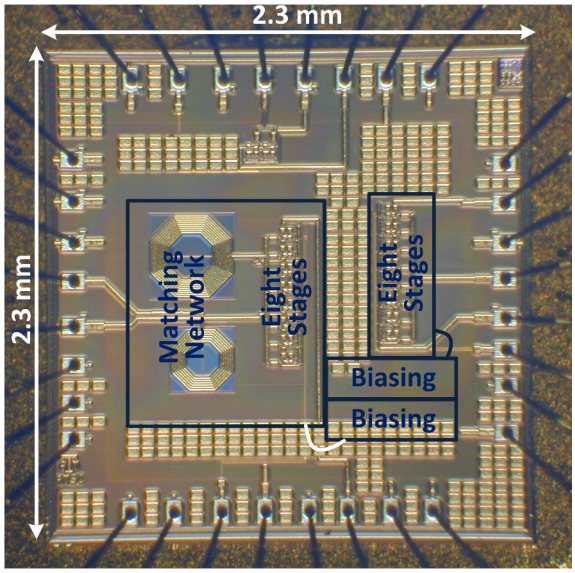


Figure 5.11: Micrograph of the different RF energy harvesting systems.

last design of the proposed antenna structure revealed worse results than shown in Fig. 5.15 due to mismatch between antenna and RF rectifier impedances and possible modeling issues.

5.5 Summary

RF energy harvesting system is composed of antennas, RF rectifiers, and matching elements. The lack of using matching elements leads to high sensitivities to parasitics and modeling errors. The path loss of the transmitted power affects the received power and the high gain antenna structures are important to counteract this effect. The received power shows a nonlinear behavior due to indoor conditions. Using inherit Balun structures in the antenna design can be done for differential to single ended conversion while keeping the losses as small as possible.

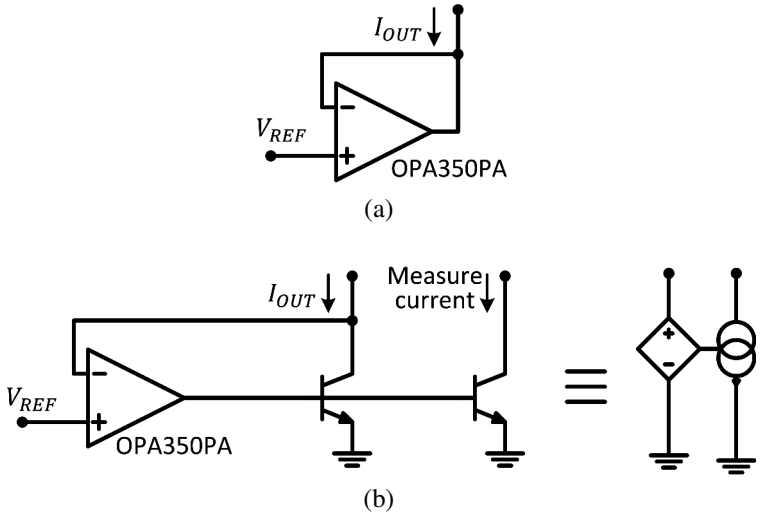


Figure 5.12: Load implementation using instrumentation amplifiers: (a) no current sensing capability and (b) added current sensing capability (used in this work).

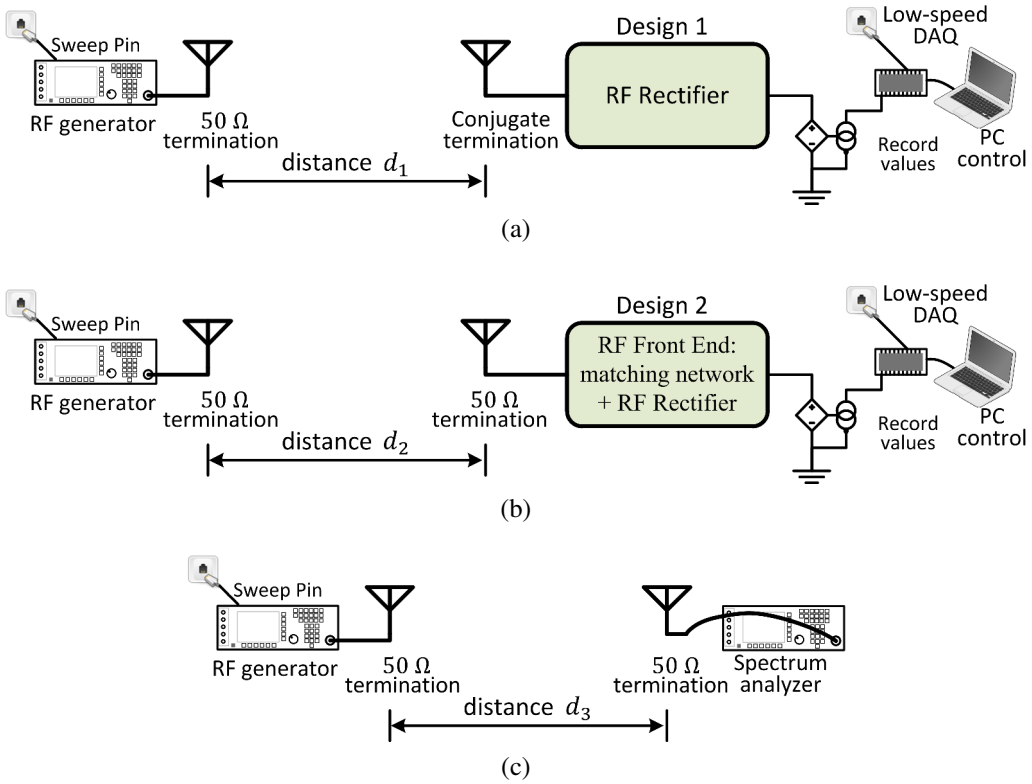


Figure 5.13: Test setup for the RF energy harvesting system: (a) testing Design1 with the proposed antenna, (b) testing Design2 with a 50 Ω antenna, and (c) measurement of the available power at the receiver.

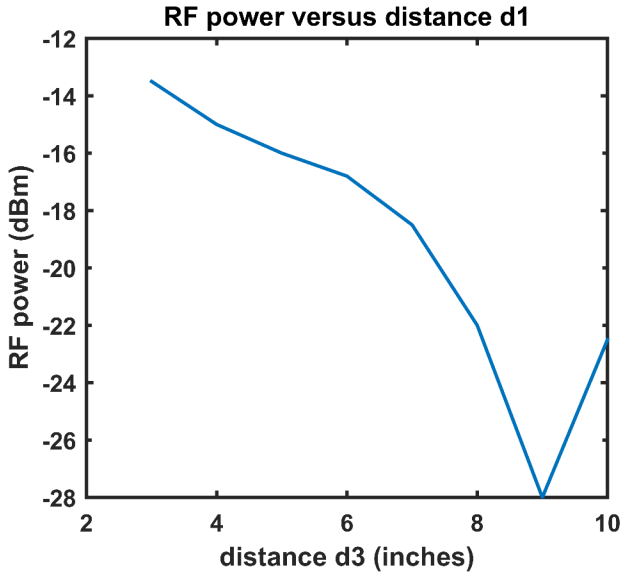


Figure 5.14: Available RF power at the receiving antenna while changing the wireless link distance d_3.

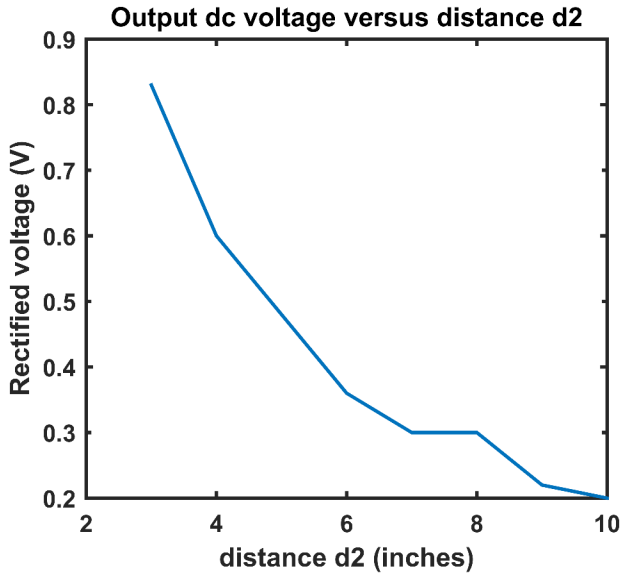


Figure 5.15: Rectified dc voltage for open circuit conditions while changing the wireless link distance d_2.

6. AN INTEGRATED RECONFIGURABLE WATT-LEVEL WIRELESS POWER TRANSFER H-BRIDGE TRANSMITTER WITH SINUSOIDAL PWM MODULATION

6.1 Introduction

Cutting the last wire through wireless power transfer is the current demand for portable consumers. A typical near field system is shown in Fig. 6.1. The dc ac converter (power inverter/amplifier) converts the dc supply to an alternating signal that drives the primary (transmitting) coil L_p. Due to coupling between the primary and the secondary (receiving) L_s coils, the magnetic energy is transferred to the secondary. The final ac to dc converter (power rectifier) delivers dc supply to the final load R_L which, for example, can be a battery to be charged. This system can be seen as a resonant dc-dc converter which is discussed extensively in [49]. There are emerging standards for the near field transmission, Qi [54] and AirFuel Alliance [55] are competing for this market. The Qi standard focuses on the near field transmission in the 100 kHz range with short distances to enable highly efficient power transfer with lots of reference designs [56]. The AirFuel Alliance is a merge between the Power Matters Alliance (PMA) and Alliance for Wireless Power's (A4WP) Rezence. It is expected to cover power-mats, inductive, resonant, far-field, ultrasound, and laser power beaming. The traditional resonant operating frequency of A4WP is 13.56 MHz where resonance can be utilized with realizable passive values to enable longer distances. The resonant primary side is composed of the coil L_p and, here, a series resonant capacitor C_p (where parallel resonance could have been utilized instead). Moreover, the resonant secondary side is composed of the coil L_s and, here, a parallel resonant capacitor C_s (where series resonance could have been utilized instead). For far field operation, the primary and secondary interfaces are replaced with resonance antennas operating

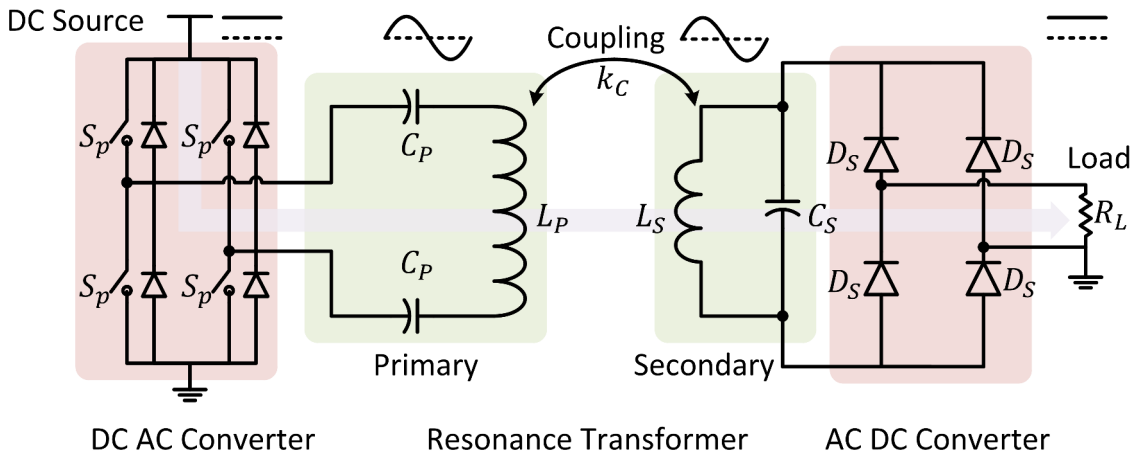


Figure 6.1: Wireless power transmission system from dc source to final dc load.

at high frequency with much longer distances. Respectively, Ossia and Energous provide the products Cota and WattUp, with the transmitter/receiver chipsets [57] and Energous, have already explored the far field wireless power transmission for WIFI frequencies 2.4 GHz and 5.8 GHz with claims of distances up to 30 feet, and power handling up to 10 Watts. They both utilize phase antenna arrays for beam forming to enhance power transfer efficiency and avoid health issues associated with high frequency/high power operation.

In this work, a fully integrated wireless power transmitter is proposed using CMOS technologies. The contributions of this work are: 1) a fully integrated watt-level transmitter with efficient operation, reliability of low-voltage CMOS process, and low electromagnetic interference (EMI), 2) a proposed efficient operation for different output powers through segmentation, 3) proposed segmentation architecture for high light load efficiency and 4) new design equations for the wireless power transfer resonant link taking into consideration the reliability of the process.

6.2 Near Field Versus Far Field Transmission

Nicola Tesla started WPT using resonant transformers (small distances) with the air as the gap or core. Then, researchers started to use far-field transmission for longer distances to power space-crafts. After that, the focus changed to near field operation [58] and recently far field operation is revived again, as was discussed in the introduction. Assuming a virtual sphere with the transmitter at the center, the region interior to the far field region is divided into the reactive near field and the radiating near field regions. The distinction between different regions comes from the dominant terms in the general solution of the electric field of an ideal dipole [52]. In the far field, the power density is real and radially directed outward from the antenna, while in the reactive near field, it is pure imaginary with no time-average radial power flow, which corresponds to a standing wave, not a traveling wave. In the radiating near field region, the power density is a complex number which is a mix between standing wave and traveling wave. For electrically small antennas, the reactive near field extends to $\lambda/2\pi$ and the boundary between radiating near field and the far field is at 5λ distance to the antenna, where λ is the wavelength related to the frequency f with c/f and c is the speed of light. This situation changes for large antennas (and phase arrays which usually have high gain), where the reactive near field extension is $0.62\sqrt{D^3/\lambda}$ and the previous boundary changes to $2D^2/\lambda$ where $D > 2.5\lambda$ is effective length of the large antenna.

When there is a receiver in the reactive near field region, inductive coupling, with a loosely coupled transformer, is the mechanism for power transfer. As the distance between the transmitter and receiver increases, the coupling and the efficiency of power transfer decrease. On the other hand, two issues related to high frequency operation (and consequently radiating fields operation) are: human safety and efficiency of power transfer [58]. For safe human exposure to electromagnetic waves, the wireless power transfer de-

vices need to comply with the IEEE C95.1-2005 standard for public environment [59] with recommended practice for Radio Frequency Safety Programs [60], shown in Fig. 6.2. The masks for low frequency operation allow high values of exposure to magnetic and electric fields and as the frequency increases, the limits get tight. Between 100 MHz and 400 MHz is the most tight in terms of power density and this maximum seems to relax to 10 $\mathrm{W/m^2}$. But actually the effective area of the antennas sizes gets smaller as the frequency increases where the actual power transfer decreases and the use of phased arrays is important for better directivity of the beams to deliver the required power. The other issue of efficient operation of circuits and transfer links at higher frequency. The latter can be seen from Friis transmission equation for Far field operation as was discussed in Section 1. The former is due to the inherited switching loss of circuits specially the low cost CMOS designs. More advanced processes such as Gallium Nitride (GaN) and Gallium Arsenide (GaAs) can be used for high frequency operation.

6.3 Analysis of the Resonant DC-DC Converter

Resonant converters are proposed in the dc-dc power conversion for their reduced switching loss. The zero voltage switching (ZVS) is known to mitigate the switching loss associated with the parasitic capacitance and reverse recovery of diodes and MOSFETs, i.e. reduced EMI and avoids ringing. On the other hand, the resonant converters are sensitive to the load conditions seen by the dc ac inverter, which changes with both the load R_L and the coupling factor k_c of the inductive link. At light load, the conduction loss should be controlled and minimized. Moreover, zero-voltage switching is obtained over a wide range of load currents and k_c. Lastly, the converter dynamic range is compatible with the load i–v characteristic. These can be controlled by the proper choice of the values of the tank elements [49]. In general, zero voltage (current) switching can occur when the resonant tank presents an effective inductive (capacitive) load to the switches, so that

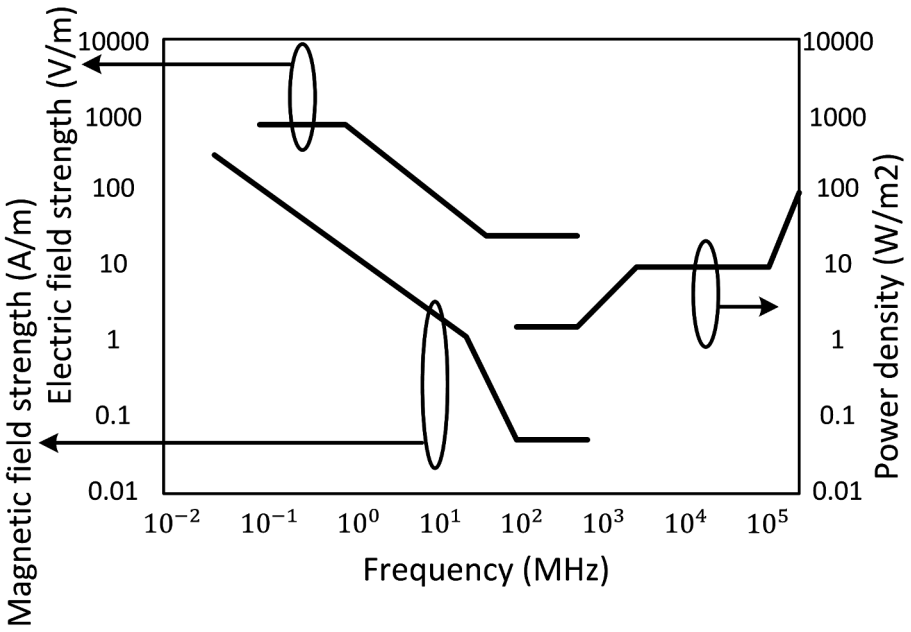


Figure 6.2: Maximum permissible human exposure to radio-frequency electromagnetic fields specified in IEEE C95.1-2005.

the switch voltage (current) zero crossings occur before the switch current (voltage) zero crossings. The following analysis assumes a high loaded quality factor for the tank circuit which will filter out harmonics and sinusoidal analysis can be utilized. For more general cases, state-plane analysis should be used.

To maintain ZVS operation for the resonant inverter, the input current to the tank (output current of the inverter) lags the input voltage to the tank (output voltage of the inverter) where the input impedance $Z_i(j\omega)$ of the tank circuit is inductive. Using the model of the tank network as shown in Fig. 6.3 where $H_\infty(j\omega_s)$ is the open circuit transfer function of the tank network, $H_\infty(j\omega_s) = \frac{v(j\omega)}{v_s(j\omega)}\Big|_{R\to\infty}$, $Z_{o0}(j\omega_s)$ and $Z_{o\infty}(j\omega_s)$ are the output impedance, determined when the source $v_s(j\omega)$ is short circuited or open circuited respectively, and $v(j\omega)$ and $i(j\omega)$ are the load (output from the tank network) voltage and current respectively. The zero current switching condition happens when $Z_i(j\omega)$ is capacitive. The inverter output characteristic, that is, the relationship between $\|v(j\omega)\|^2$ and

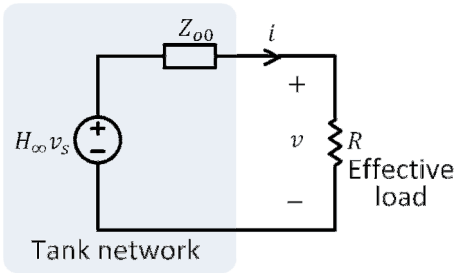


Figure 6.3: Tank model for fundamental harmonic analysis of high-Q resonant dc-dc converter.

$\|i(j\omega)\|^2$ is elliptical with the relationship:

$$\frac{\|v(j\omega)\|^2}{V_{oc}^2} + \frac{\|i(j\omega)\|^2}{I_{sc}^2} = 1, \tag{6.1}$$

which is plotted in Fig. 6.4. The open circuit voltage V_{oc} and the short circuit current I_{sc} are given by:

$$\begin{aligned} V_{oc} &= \|H_\infty(j\omega_s)\| \, \|v_s(j\omega_s)\|, \\ I_{sc} &= \frac{V_{oc}}{Z_{o0}(j\omega_s)}, \end{aligned} \tag{6.2}$$

where ω_s is the switching frequency and$v_s(j\omega)$ is the fundamental sinusoidal voltage at the input of the tank circuit. For a matched load condition, $R = \|Z_{o0}(j\omega_s)\|$, which results in an operating voltage and current $\|v(j\omega_s)\| = V_{oc}/\sqrt{2}$ and $\|i(j\omega_s)\| = I_{sc}/\sqrt{2}$ respectively. In order to see the effect of load conditions on the input impedance $Z_i(j\omega)$ of the tank on the inverter operation, $Z_i(j\omega)$ is sketched for different loads. Extreme cases for an open circuit $R \to \infty$ and short circuit $R \to 0$ are $Z_{i\infty}(j\omega_s)$ and $Z_{i0}(j\omega_s)$ respectively. It is desirable to have $\|Z_{i\infty}(j\omega_s)\| > \|Z_{i0}(j\omega_s)\|$ such that the no load current is maintained less than the short circuit current which corresponds to high light load efficiency. For lossless tank networks, the input impedance $Z_i(j\omega)$ is a monotonic

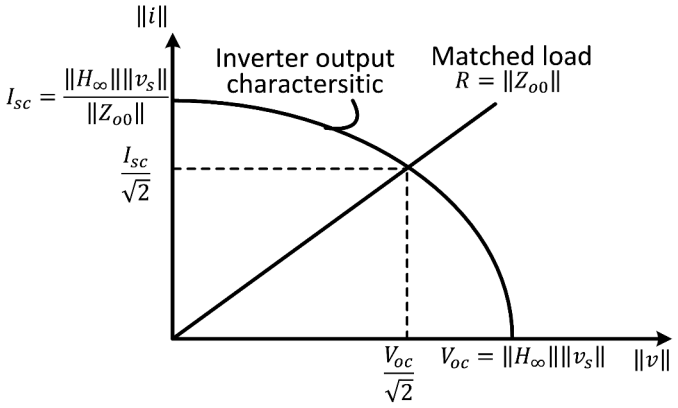


Figure 6.4: I-V elliptic characteristics of resonant inverters where a resistive matched load is also presented and assuming lossless tank operation.

function of the load resistance R [49] and given by:

$$Z_i(j\omega) = Z_{i0}(j\omega)\frac{\left(1+\frac{R}{Z_{o0}(j\omega)}\right)}{\left(1+\frac{R}{Z_{o\infty}(j\omega)}\right)} = Z_{i\infty}(j\omega)\frac{\left(1+\frac{Z_{o0}(j\omega)}{R}\right)}{\left(1+\frac{Z_{o\infty}(j\omega)}{R}\right)}, \tag{6.3}$$

which is derived through the use of Middlebrook's Extra Element Theorem [61]. The intersection between $Z_{i\infty}(j\omega)$ and $Z_{i0}(j\omega)$ occurs at the frequency f_m. At this frequency, the relationship between the two impedance values changes where it is desirable to operate with $\|Z_{i\infty}(j\omega_s)\| > \|Z_{i0}(j\omega_s)\|$ where the short circuit current is higher than the open circuit current.

Also, it is necessary to determine the critical resistance $R = R_{crit}$ at the boundary between ZVS and ZCS. This boundary can also be expressed as a function of the impedances $Z_{i\infty}$ and Z_{i0}. For lossless tank network, the boundary between zero-current switching and zero-voltage switching occurs when the load resistance $R = R_{crit}$ where:

$$R_{crit} = \sqrt{Z_{o0}Z_{o\infty}} = \|Z_{o0}\|\sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}, \tag{6.4}$$

where this conditions is satisfied when $Z_i(j\omega) = 0$. For $R < R_{crit}$, ZVS operation is maintained. For a typical converter, this occurs for frequencies $f > f_0$. So to satisfy both light load high efficiency and ZVS, the operating frequency should be in the range $f_0 < f_s < f_m$ where load resistance R above R_{crit} losses ZVS but maintain the light load efficiency through low conduction loss (small currents).

In order to analyze the resonant dc-dc converter, shown in Fig. 6.1, and the relevant circuit model for the transformer, shown in Fig. 6.5, the open circuit voltageV_{oc} and the nominal output voltage V and current I are known. The value of V_{oc} corresponds to the maximum voltage that the ac dc rectifier can withstand which is imposed by the technology used for this circuit. For matched operation, the relationship $V_{oc} = \sqrt{2}V$ should hold. The expression for $H_\infty(j\omega_s)$ is given by:

$$H_\infty(j\omega_s) = \frac{j\omega_s M}{(j\omega_s L_p + 1/j\omega_s C_p)}, \tag{6.5}$$

where the transformer is analyzed as an impedance inverter [62, 63] and $M = k_C L_p L_s$. The expressions for the output impedance $Z_{o0}(j\omega_s)$ is:

$$Z_{o0}(j\omega_s) = \frac{\omega_s^2 M^2}{(j\omega_s L_p + 1/j\omega_s C_p)} + (j\omega_s L_s + 1/j\omega_s C_s), \tag{6.6}$$

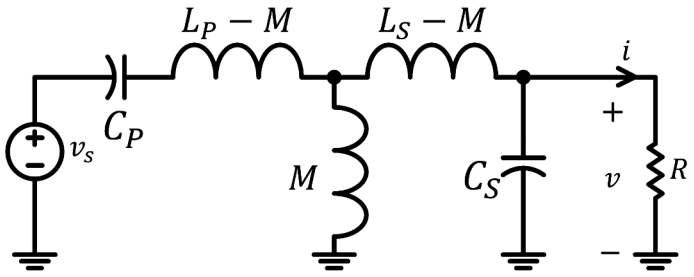


Figure 6.5: Circuit model for the wireless power transfer tank.

and the input impedances at open and short circuits are:

$$Z_{i\infty}\left(j\omega_s\right) = \left.Z_i\left(j\omega_s\right)\right|_{R\to\infty} = \left(j\omega_s L_p + 1/j\omega_s C_p\right), \tag{6.7}$$

$$Z_{i0}\left(j\omega_s\right) = \left.Z_i\left(j\omega_s\right)\right|_{R\to 0} = \frac{\omega_s^2 M^2}{\left(j\omega_s L_s + 1/j\omega_s C_s\right)} + \left(j\omega_s L_p + 1/j\omega_s C_p\right). \tag{6.8}$$

The bode plots of these equations are shown in Fig. 6.6 and the intersection frequency f_m is given by:

$$f_{m1,2} = \frac{1}{2\pi\sqrt{2L_pL_s\left(1-k^2/2\right)}} \sqrt{\left(\frac{L_p}{C_s}+\frac{L_s}{C_p}\right) \pm \sqrt{\left(\frac{L_p}{C_s}+\frac{L_s}{C_p}\right)^2 - \frac{4L_sL_p\left(1-k^2/2\right)}{C_pC_s}}}, \tag{6.9}$$

and the equation for f_0 is the same as (6.9) except for modifying the $k^2/2$ to only k^2. The operation the operating frequency should be in the range $f_0 < f_s < f_m$ and the expression for R_{crit} is given by:

$$R_{crit} = \sqrt{\left(1-k^2\right)L_pL_s\omega_s^2 + \left(\frac{L_p}{C_s}+\frac{L_s}{C_p}\right) - \frac{1}{C_pC_s\omega_s^2}}, \tag{6.10}$$

where the ZVS operation is guaranteed when $R < R_{crit}$.

6.4 Optimization of Inductive Link Coils

The losses of the coils directly impacts the range and efficiency of the wireless power transfer system [64, 65, 66, 67, 68]. There are two common types of coils: PCB [69] and Litz wire [70, 71] coils where the later is used in this work for higher quality factor. As the coupling factor k decreases, as the distance between the transmitter and receiver increases, the reflected load resistance at the transmitter side decreases and this mandates

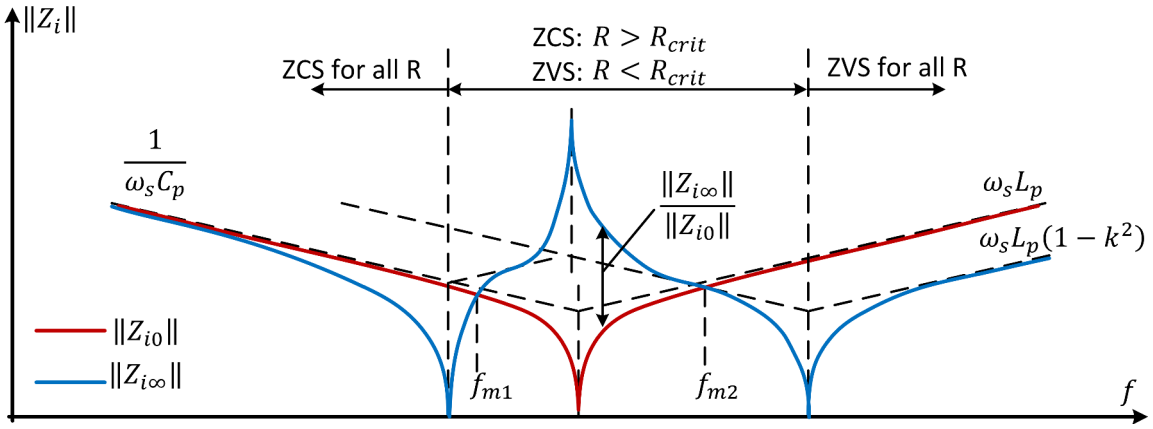


Figure 6.6: how to determine the ZVS and ZCS regions using the open/short circuit input impedances $\|Z_{i\infty}(j\omega_s)\|$ and $\|Z_{i0}(j\omega_s)\|$.

the use of high quality factor Q_p and Q_s in the primary and the secondary of the wireless link (lower losses with respect to the reflected load resistance). According to the previous literature, the value efficiency at resonance increases as the term kQ_p and kQ_s increases (or $k^2_{coupling}Q_{primary}Q_{secondary}$). In the previous analysis, the tank is assumed to be lossless which is achieved by the maximum attainable quality factors. Towards this goal, the values of the self-inductances L_p and L_s need to be calculated and also the losses in the coils. After that, the quality factor Q_p and Q_s can be estimated and maximized for different geometries. The equations of self-inductance are accurate and most of them can be found in [72]. However, the loss resistance analytic expressions are more complicated. At low frequency, the conduction loss resistance is the dominant factor. As the frequency increases, the current passes through outer surface of the conductor in a thickness δ called penetration depth. This assumes a wire carrying current at high frequency. But there is interaction between the different turns of the Litz coil which gives rise to proximity effects and these can introduce significant resistance values compared to the δ model at high frequency. Thus, expressions of the ac resistance of the Litz coil should take into account this effect. In [71], the expressions of δ model were compared to the measurements which

showed too much discrepancy (as commented by the authors) at tight pitch distances between the turns of the coils and this was also observed by the use of Ansys Maxwell® simulator [73] which only takes the penetration depth effect. Here, Ansoft HFSS® [74] is used to take into account the proximity effects. A spiral Litz wire coil is shown in Fig. 6.7 which is simulated while varying the pitch p for different number of turns N for a diameter of 60 mm^2.

On the other hand, coupling coefficient can be estimated from the expressions of the mutual inductance. HFSS® setup is shown in Fig. 6.8 and the EM simulation results for the quality factor, self-inductance, coupling factor $k_{coupling}$, and efficiency factor $k^2_{coupling}Q_{primary}Q_{secondary}$ are shown in Figs. 6.9, 6.10, 6.11, and 6.12, respectively. The simulation setup is done for two concentric coils, each having 48 mm outer radius, 0.512 mm cross-section radius of the wires, and the distance is varied. The pitch distance was chosen to be 2.524 mm to reach maximum quality factor based on a similar simulation varying the pitch distance. The quality factor of the primary and secondary is shown to be maximum when the number of turns is 6 and the efficiency factor is also maximized for that value. No change versus distance for both self-inductance and quality factor which give confidence to the simulation results.

Finally, the mutual inductance M is defined as:

$$M = \frac{\mu_0}{4\pi} \oint \oint \frac{dl_p.dl_s}{r_{ps}}, \tag{6.11}$$

where dl_p and dl_s are the line segments of the primary and secondary coils respectively and r_{ps} is the distance between the segments. For concentric loop coils with radii a and b and distance d [75], the expression is:

$$M = \mu_0 \sqrt{ab} \left\{ \left(\frac{2}{k} - k \right) \mathrm{K}(k) - \frac{2}{k} \mathrm{E}(k) \right\}, \tag{6.12}$$

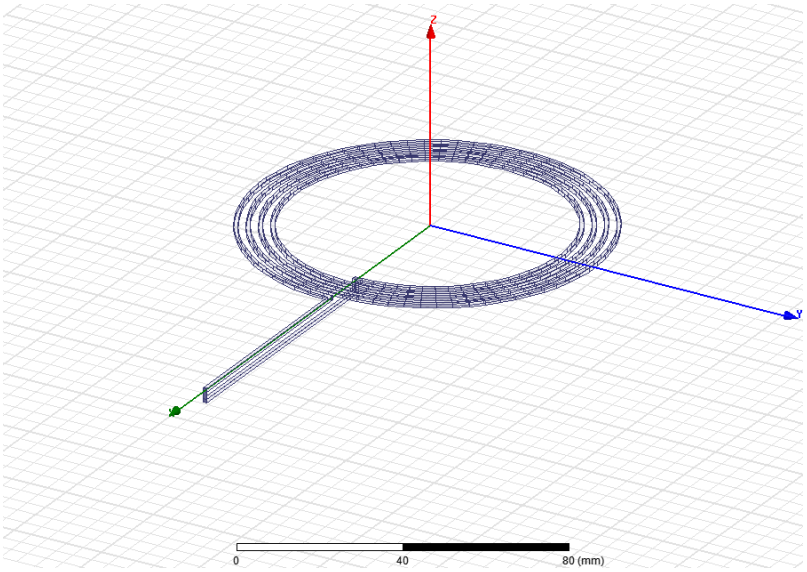


Figure 6.7: Litz wire coil drawn in HFSS® with excitation and de-embedding.

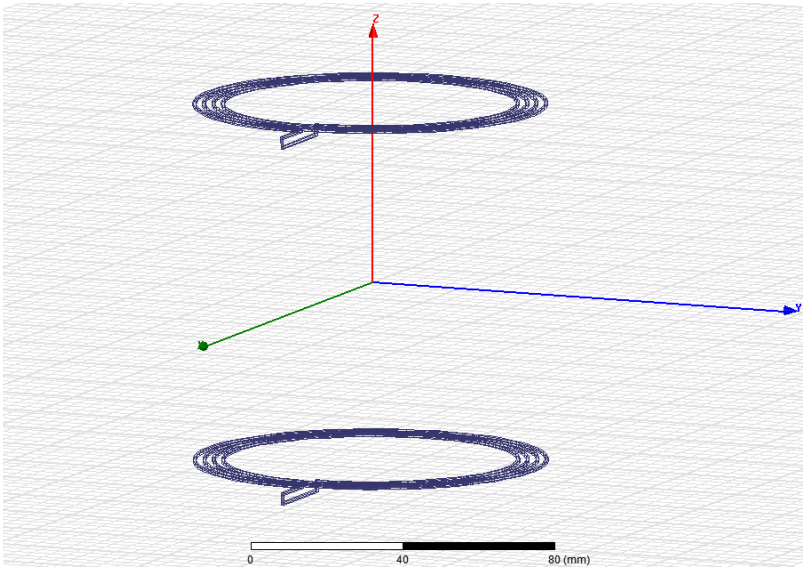


Figure 6.8: Mutual inductance EM setup in HFSS® solver.

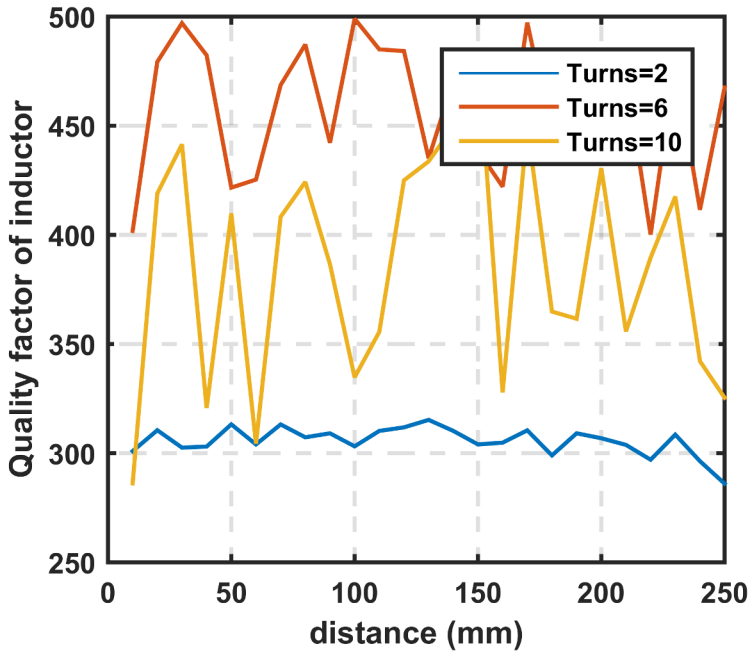


Figure 6.9: Quality factor is invariant from distance and dependent on the number of turns.

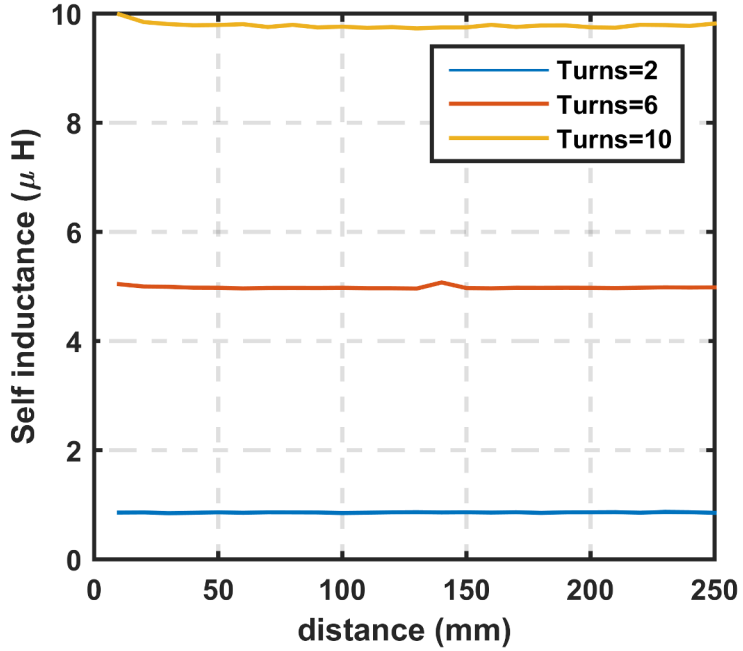


Figure 6.10: Self-inductance is invariant from distance and dependent on the number of turns.

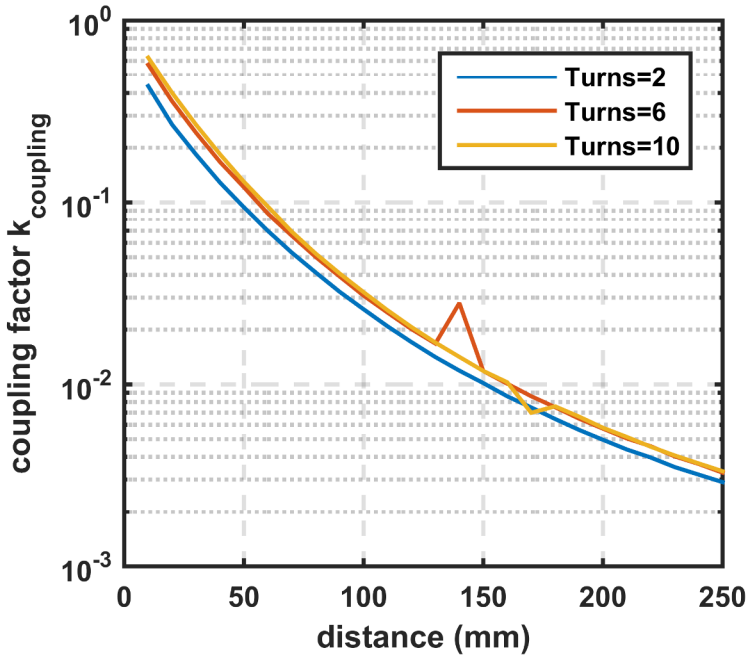


Figure 6.11: Coupling factor k_{couple} versus distance for different number of turns.

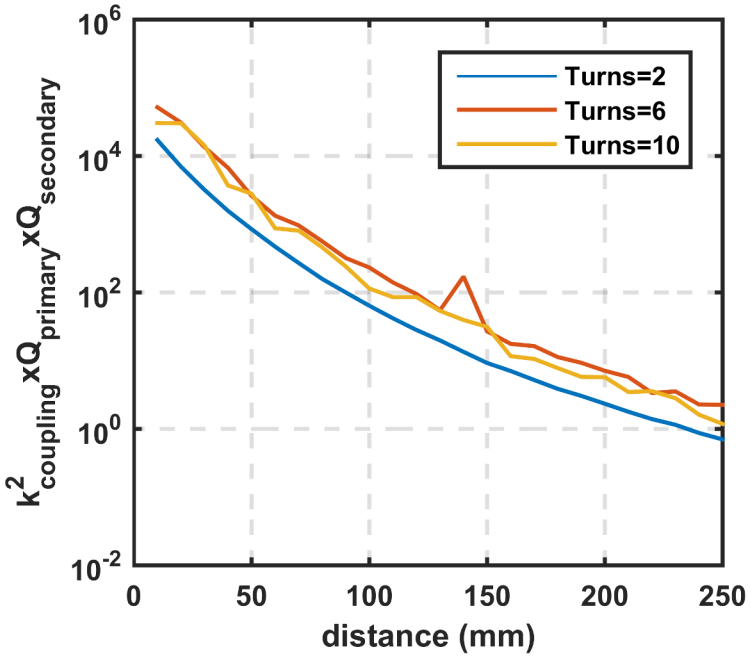


Figure 6.12: Efficiency factor $k^2_{coupling}Q_{primary}Q_{secondary}$ versus distance for different number of turns.

$$k = \sqrt{\frac{4ab}{(a+b)^2 + d^2}}, \tag{6.13}$$

where $\mathrm{K}(k)$ is the complete elliptic integral of the first kind and is given by:

$$\mathrm{K}(k) = \int_0^{\pi/2} \frac{1}{\sqrt{1 - k^2 \sin^2\theta}} d\theta, \tag{6.14}$$

and $\mathrm{E}(k)$ is the complete elliptic integral of the second kind given by:

$$\mathrm{E}(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2\theta} d\theta. \tag{6.15}$$

In the cases of misalignment and angular coils configurations, no analytic formula for the mutual inductance exists and the coupling factor changes and this was analyzed in [75].

6.5 Multi-Level Inverter and Modulation Strategies

In order to design a dc to ac power inverter, there are many alternatives. Among which multi-level inverters are chosen in this work. Multilevel inverters offer the ability to raise the supply voltage while using standard low voltage devices through proper stacking. Thus, the load resistance can be high while the output power is high as well which provide immunity against the losses in the inductors. Also, the inverter can operate at lower frequency with smaller switching loss [76]. Moreover, the structure of the multi-level inverters allows for low total harmonic distortion (THD) which leads to low EMI. The common topologies are: diode clamped and capacitor clamped (flying capacitor) converters [76, 77] where five-level examples are shown in Figs. 6.13a and 6.13b respectively. The output voltages v_{diode} and v_{cap} has four states, 0, $V_{supply}/4$, $V_{supply}/2$, $3V_{supply}/4$ and V_{supply}. For the diode clamped case, the extra diodes provide paths for the

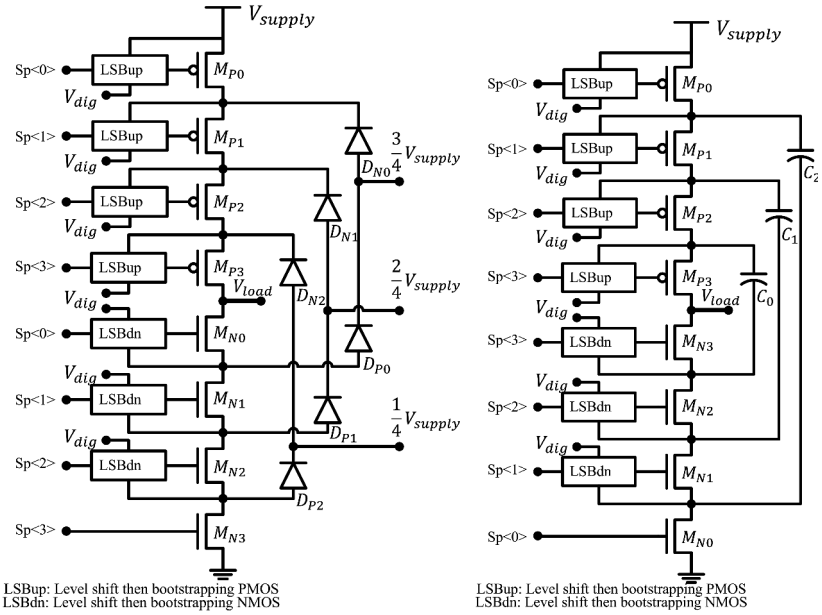


Figure 6.13: Five-level multi-level inverters (a) diode clamped and (b) capacitor clamped (flying capacitor).

intermediate voltages while in the capacitor clamped, the flying capacitors are assumed to be precharged (and charged during the multi-level inverter cycle) such that the output voltage can obtain the intermediate nodes. In these proposed structures, PMOS is used for the high side of the inverter which offers flexibility and lower loss for drivers. Moreover, the output current is ac where the current can flow toward (from) the load though the high (low) side. To determine the required signaling for each inverter, the different states of the both topologies are summarized in Figs. 6.14, 6.15, 6.16, 6.17, and 6.18.

6.5.1 Diode Clamped Topology

In order to get $V_{load} = 0$, shown in Fig. 6.14a, all device $M_{N0...3}$ are conducting while the device $M_{p0...3}$ are off. In order to maintain a suitable low voltage across each device (here, this is $V_{supply}/4$), diodes $D_{N0...2}$ are conducting such that the internal node voltages

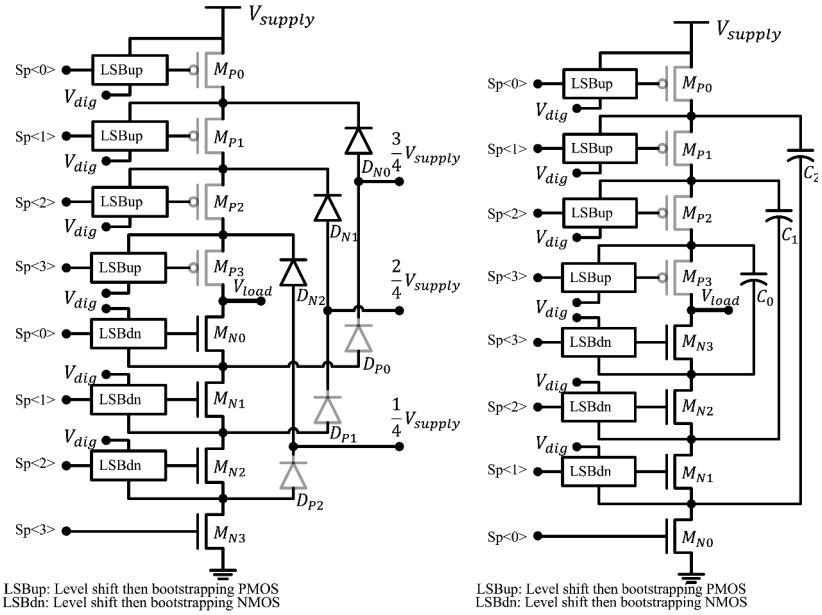


Figure 6.14: State $V_{load} = 0$ (a) diode clamped and (b) capacitor clamped which is called (flying capacitor).

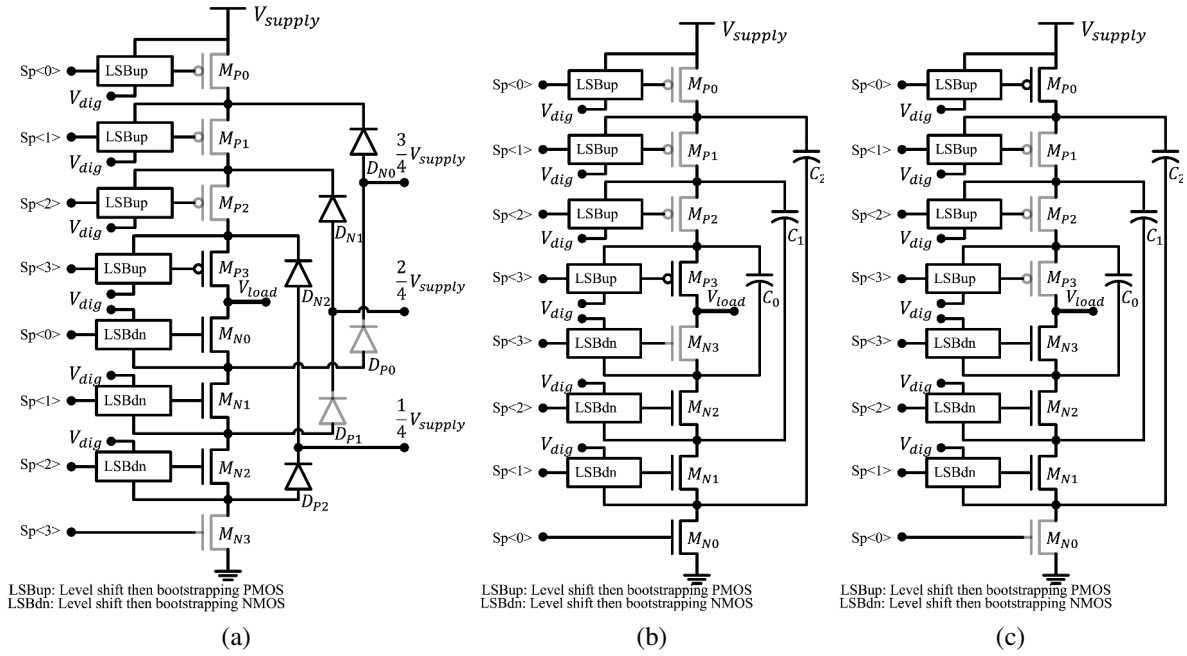


Figure 6.15: State $V_{load} = V_{supply}/4$ (a) diode clamped and (b) and (c) capacitor clamped (flying capacitor) and its redundant state.

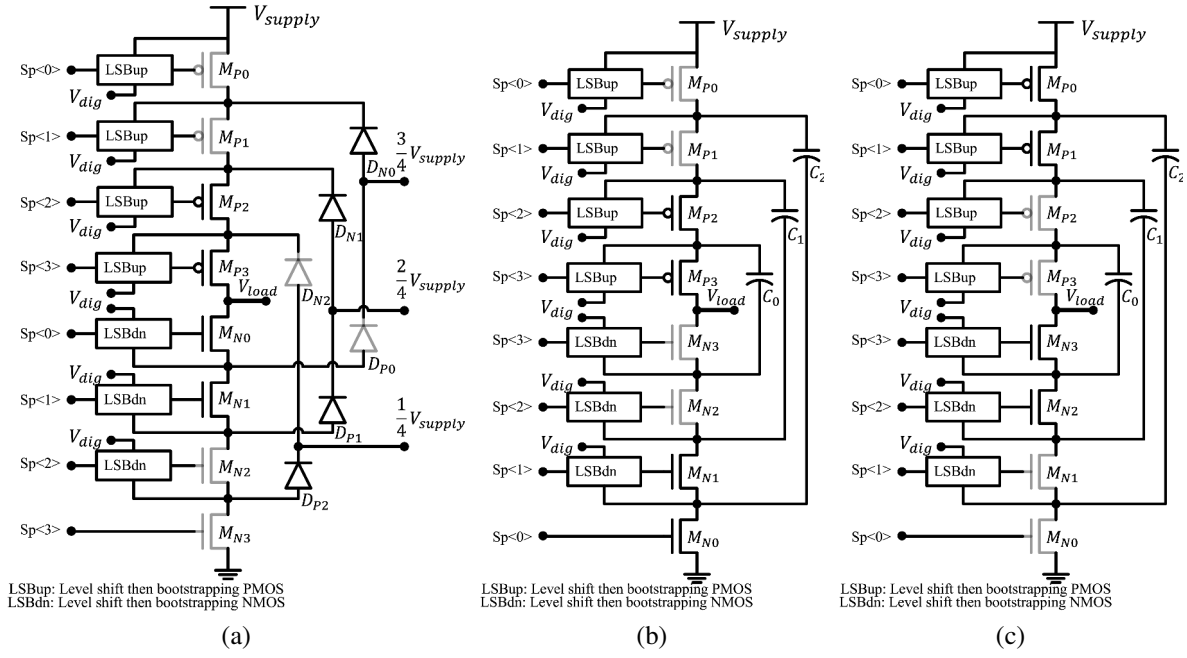


Figure 6.16: State $V_{load} = V_{supply}/2$ (a) diode clamped and (b) and (c) capacitor clamped (flying capacitor) and its redundant state.

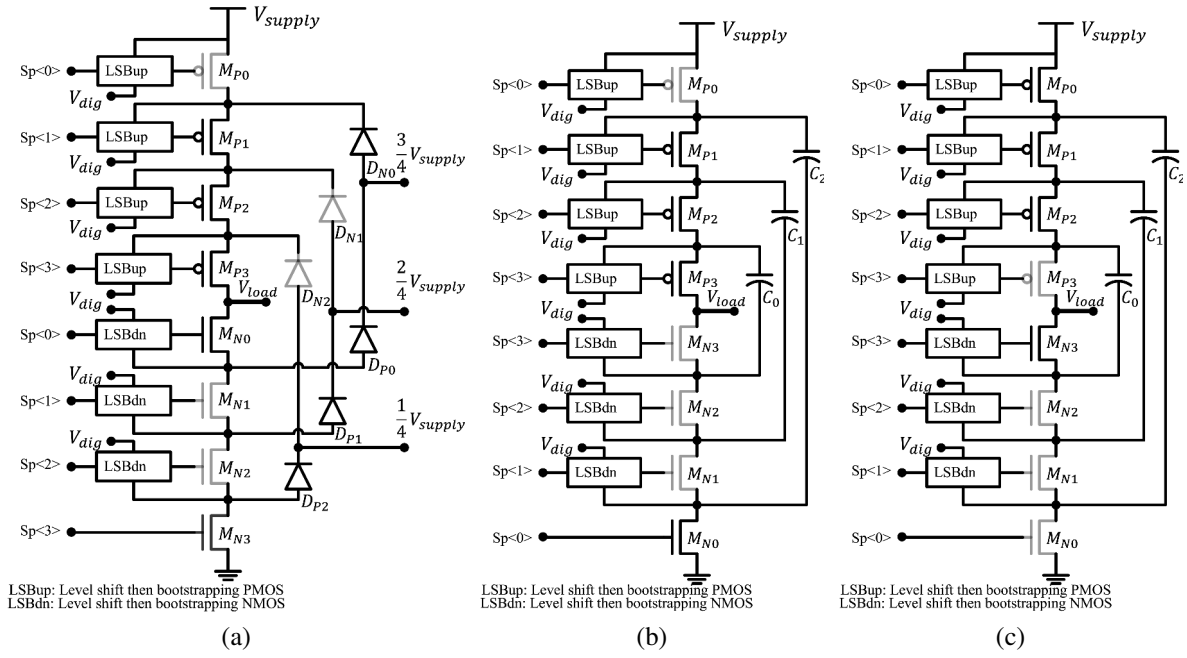


Figure 6.17: State $V_{load} = 3V_{supply}/4$ (a) diode clamped and (b) and (c) capacitor clamped (flying capacitor) and its redundant state.

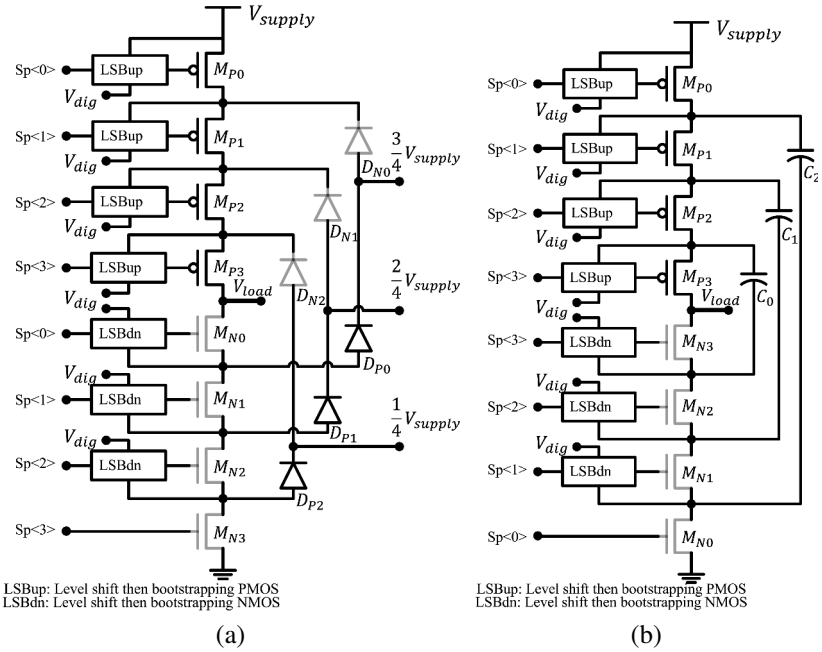


Figure 6.18: State $V_{load} = V_{supply}$ (a) diode clamped and (b) capacitor clamped (flying capacitor).

are defined. For the state $V_{load} = V_{supply}/4$, shown in Fig. 6.15a, diodes D_{P2} and D_{N2} are conducting to support ac current for the load. Moreover, the devices $M_{N0...2}$ and $M_{P0,1}$ are conducting, while diodes $D_{N0,1}$ and also D_{P2} provide the appropriate internal node voltage. Similarly, states $V_{load} = V_{supply}/2$, $V_{load} = 3V_{supply}/4$, and $V_{load} = V_{supply}$ can be deduced as shown in Figs. 6.16a, 6.17a, and 6.18a respectively.

6.5.2 Capacitor Clamped (Flying Capacitor) Topology

For this topologies, the assumption that the capacitors C_0, C_1, and C_2 are precharged to $V_{supply}/4$, $V_{supply}/2$, and $3V_{supply}/4$, respectively for each cycle and this voltage difference can be used as a source while discharging. redundant states are important for this charging/discharging mechanism. In order to get $V_{load} = 0$, shown in Fig. 6.14b, all device $M_{N0...3}$ are conducting while the device $M_{p0...3}$ are off. The capacitors $C_{0,1,2}$ provide

the appropriate internal node voltages where each device of $M_{P0...3}$ have a reverse voltage drop as $V_{supply}/4$. The state $V_{load} = V_{supply}/4$ is discussed in Fig. 6.15b. Device M_{P3}, capacitor C_0, and M_{N0} enforces the value of output voltage, again provided that capacitor C_0 is already precharged. Similarly, states $V_{load} = V_{supply}/2$, $V_{load} = 3V_{supply}/4$, and $V_{load} = V_{supply}$ can be deduced as shown in Figs. 6.16b, 6.17b, and 6.18b respectively. Lastly, redundant states are shown in Figs. 6.15c, 6.16c, and 6.17c which can be used to charge the capacitors $C_{0,1,2}$.

Since the output of the inverter is time varying, sinusoidal pulse width modulation (SPWM) is used where the reference signal is a sinusoidal signal is compared to a high frequency triangular signal. Alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) are shown in Fig. 6.19. Carriers of APOD modulation are shifted by 180 degrees in adjacent bands with peak-to-peak voltage V_{dig}. Carriers of POD modulation above the reference $V_{dig}/2$ line are out of phase with these below zero by 180 degrees, each shifted by $V_{dig}/4$ and peak-to-peak voltage is $V_{dig}/4$. Finally the carrier of PD modulation is the same as POD except for all carriers are in phase across all bands and PD modulation is reported to offer the lowest THD [78]. Also, from our analysis of the two multi-level inverters topologies, the PD modulation is suitable for diode clamped inverter while POD modulation is suitable for capacitor clamped inverters. Other modulation schemes such as space-vector modulation and selective harmonic elimination modulation [78] can be used for more sophisticated designs.

In this work, capacitor clamped inverters are not used due to problems associated with converter initialization, regulation of the capacitor voltages under normal operation, and higher capacitor rating to block the high dc voltages. On the other hand, the problems of the diode clamped inverters are the diode stress which may lead to the use of more diodes in series and consequently more area/loss. In CMOS processes, the well diodes are known to withstand more reverse voltage than the standard devices.

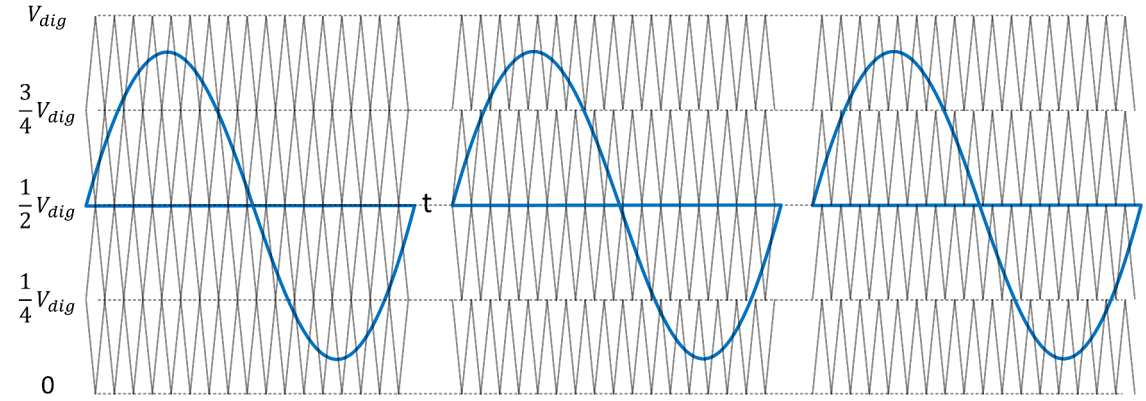


Figure 6.19: Carrier based Sinusoidal PWM: left: alternative phase opposition disposition (APOD), middle: phase opposition disposition (POD), and right phase disposition (PD).

Finally, the previous descriptions are for unbalanced (single-ended) designs. H-bridge configurations can be used, as will be shown, to enable differential (balanced) operation where two-phases are used to drive the load, which is the primary inductor.

6.6 Proposed Transmitter System

The proposed transmitter system is shown in Fig. 6.20 with the two-phase outputs out_p and out_n. An external modulation signal at frequency f_{mod} and carrier sinusoidal signal at

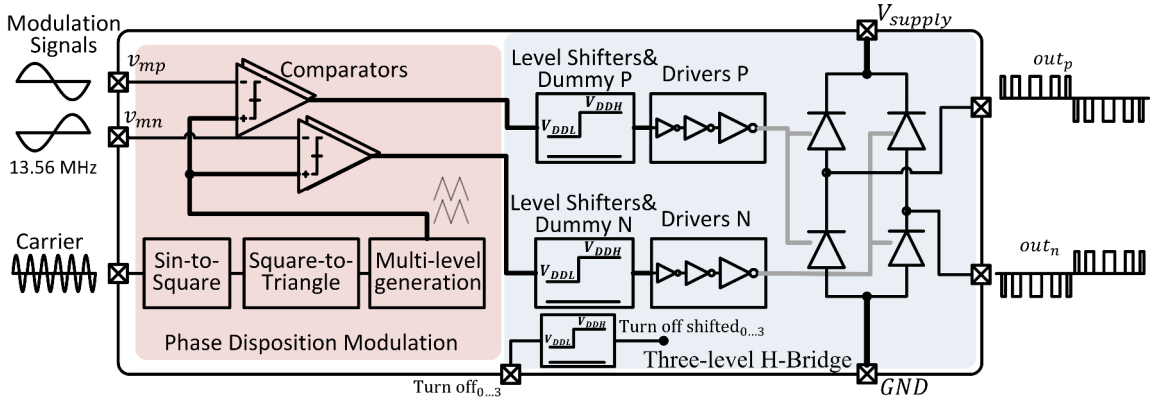


Figure 6.20: Proposed design of the wireless power transmitter.

$f_{carrier} \gg f_{mod}$ are the reference sinusoidal and the carrier signals. The carrier signal is converted to square and then a triangular signal. In a typical SPWM, the triangular signal is compared with the modulating signal to generate pulse with a density proportional to the signal. Here, shifted versions of the triangular signal is used to generate pulses for the multi-level inverter, specifically, PD is used as discussed in the previous Section 6.5. High-speed rail-to-rail comparator [79] are used in this design. The modulated signals, with the logic '0' and '1' are in the digital domain and need power to drive the power transistors in the multi-level inverter. The logic signals are level shifted according to the appropriate values. Dummy level shifters are used to equalize the delay between all paths when no level shifting is needed. A segmented power drivers are used to enable better efficiency while delivering less power. The signals $\mathrm{Turn\ off}_{0...3}$ and the shifted versions $\mathrm{Turn\ off\ shifted}_{0...3}$ are used for that. The chain of inverters in the driver circuit is a fan-out-four (FO4) as a compromise between speed and power consumption [80]. The H-bridge, two-phase multi-level inverter is driving the primary coil in the wireless power transfer system. The circuit blocks of the SPWM generation are shown in Fig. 6.21. The resistor $R_b = 50\ \Omega$ is used to provide external matching and prevent reflections for the high frequency carrier signal. Inverter INV_0 with the feedback resistor R_0 are used for square signals generation. A charge pump with externally tuned currents I_P and I_N integrates the square signal to obtain a triangular waveform OUT. In order to control the dc level to $V_{dig}/2$ for maximum linearity of the integrator, the negative feedback loop incorporating the amplifier A_1 (a typical one-stage differential amplifier [81]) is used. High-pass filters with capacitorsC_H and C_L, resistors R_H and R_L, and dc biasing $V_{dig}/4$ and $3V_{dig}/4$ are used to generate the multi-level triangular signals, T_H and T_L, respectively. In order to control the peak to peak values of the triangular signals, the peak of the signal OUT is detected as shown in Fig. 6.22. The capacitor C_p and the diode-connected device D_p are the typical peak detector circuits where amplifier $A_2$is used to prevent loading on the signal OUT . A reset peak

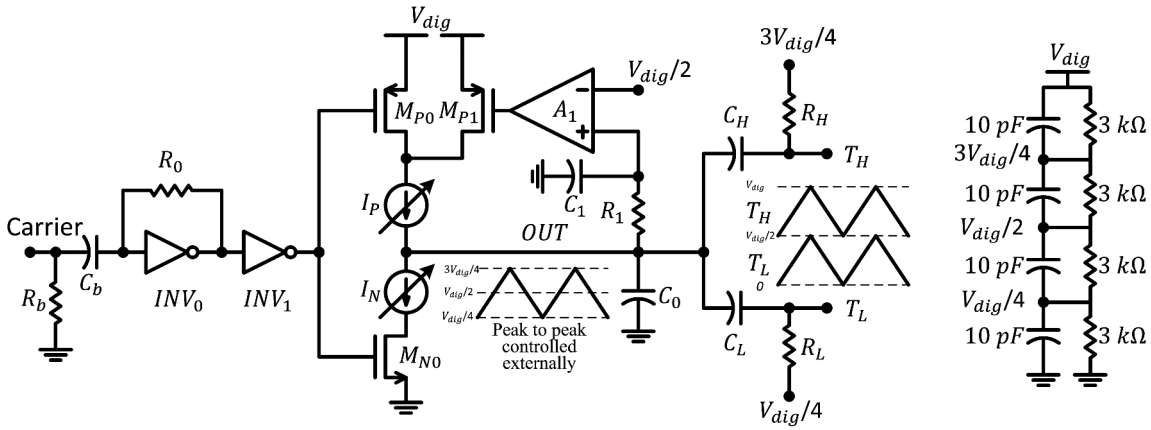


Figure 6.21: Three-level sinusoidal pulse width signals for pulse disposition modulation.

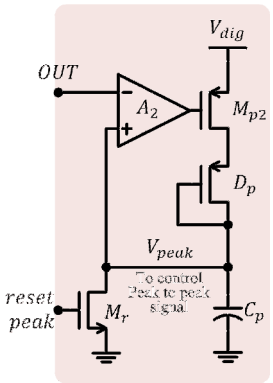


Figure 6.22: Peak detector used to detect the peak of the output triangular wave.

signal is externally applied as a pulse to reset the voltage V_{peak} to zero before whenever the peak is evaluated. A one-phase of H-bridge multi-level inverter with the appropriate signals is shown in Fig. 6.23. The diode clamped inverter is composed of the low side switches $MN_{3\,0\ldots3}$ and $MN_{2\,0\ldots3}$; and the high switches $MN_{1\,0\ldots3}$ and $MN_{0\,0\ldots3}$; and the controlled diodes DN_{03} and DN_{33}. Fig. 6.24 shows the different states and the required signal levels for each switch. The diode DN_{03} (DN_{33}) is on when $MN_{0\,0\ldots3}$ ($MN_{3\,0\ldots3}$) are off, which results in taking the same switch control signals between both. The rules of the controlled diodes are to provide biasing for intermediate nodes when switches are off connected to these nodes and provide current path, in both directions from the load and to the load, for the load to obtain the state $V_{supply}/2$. Regarding the low side and high side switches, the signal levels for the switches $MN_{3\,0\ldots3}$ and $MN_{1\,0\ldots3}$ are between 0 and $V_{supply}/2$ The signal levels for the switches $MN_{3\,0\ldots3}$ and $MN_{1\,0\ldots3}$ are between 0 and $V_{supply}/2$. The signal levels for the switches $MN_{3\,0\ldots3}$ and $MN_{1\,0\ldots3}$ are between 0 and $V_{supply}/2$ while the signal levels for the switches $MN_{2\,0\ldots3}$ and $MN_{0\,0\ldots3}$ are between $V_{ssupply}/2$ and V_{supply}. During the disconnect state where one (or more) segments are required to be disconnected, the low side and high side switches are all off with the shown gating signals and the controlled diodes enable the biasing at the intermediate nodes. In Fig. 6.23, the triangular signals T_H and T_L are compared to the sinusoidal modulation signal v_{mn} to generate the control signals CTR_H and CTR_L. Level shifters and dummy level shifters are used for different switches and controlled power drivers are used. The rails for the inverters of the drivers depend on the required signaling for each switch in the bridge inverter as shown in the figure. To control the drivers to enable control over the different segments of the multi-level inverter, the first inverter in the driver chain has extra signals and switches as shown in Fig. 6.25. When the value of the $\mathrm{turn\,off} =' 1'$, the segment is disconnected with applying logic $'0'$ to the low side and high side switches, where the actual voltage value of the logic $'0'$ is different and the appropriate values are

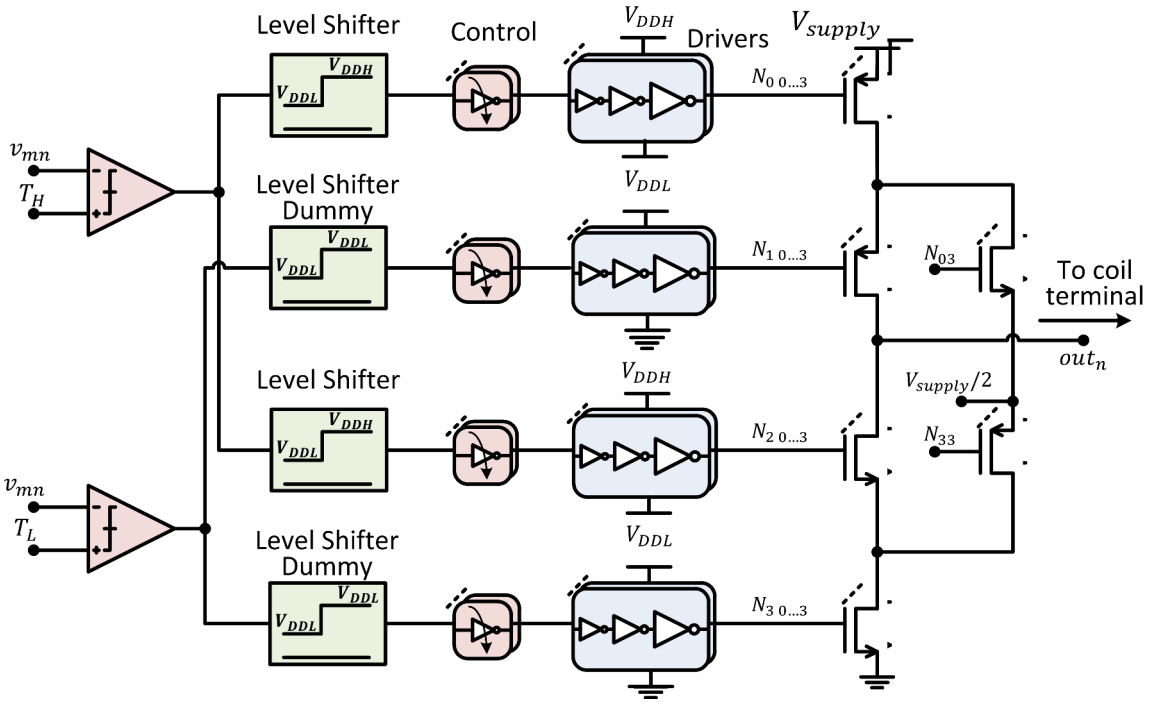


Figure 6.23: One-phase of H-bridge with segmentation for the power transistors and the drivers and the different signals.

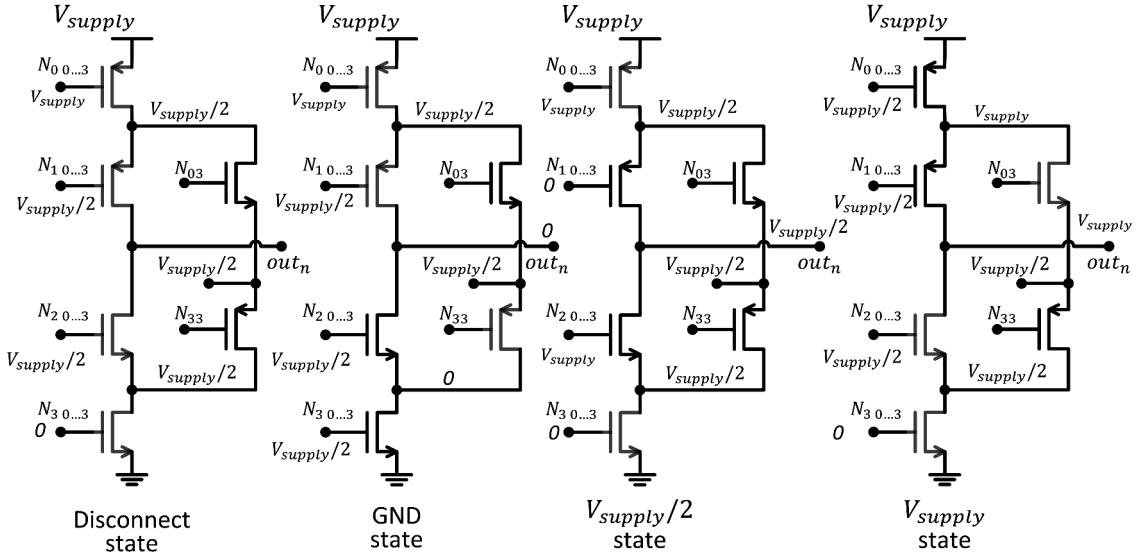
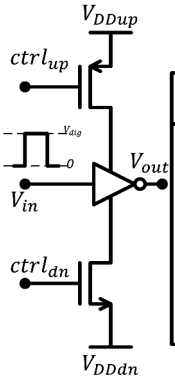


Figure 6.24: Proposed three-level inverter with different states.



See Fig.	$ctrl_{up}$	$ctrl_{dn}$	V_{DDup}	V_{DDdn}
	Turn off shifted	V_{DDH}	V_{DDH}	V_{DDL}
	Turn off	V_{DDL}	V_{DDL}	0
	V_{DDL}	(Turn off Shifted)'	V_{DDH}	V_{DDL}
	0	(Turn off)'	V_{DDL}	0

Figure 6.25: How to control the segments of the drivers.

used. There are three types of level-shifters used in this work, shown in Figs. 6.26, 6.27, and 6.28. A contention mitigated level shifter design was presented in [82] and the low-speed level shifter, here Fig. 6.26, is based on that design. In the SPWM signal path, high speed level-shifter design is needed for the driver chain, which is shown in Fig. 6.27. The capacitor and the forward inverter allow for faster operation. The cascode NMOS and PMOS transistors are used to ensure the reliability of low-voltage devices, which are used in this work. The signal after the cross coupled pair is between V_{DDL} and V_{DDH} and the rails of the next PMOS-NMOS inverter is between these values. It should be noted that the well diodes can withstand more voltage than the gate-source, gate-drain, and drain-source voltages. Finally, for the equalization of delays in the driver chain, a dummy version of the high speed level shifter is used as shown in Fig. 6.28. The capacitor and the forward inverter are omitted since no high voltage is needed and the biasing of the cascode devices is changed such that they are always passing signals. In order to control the segments of the drivers, the first inverter stage is controlled with the digital word $\mathrm{Turn\ off}_{0...3}$.

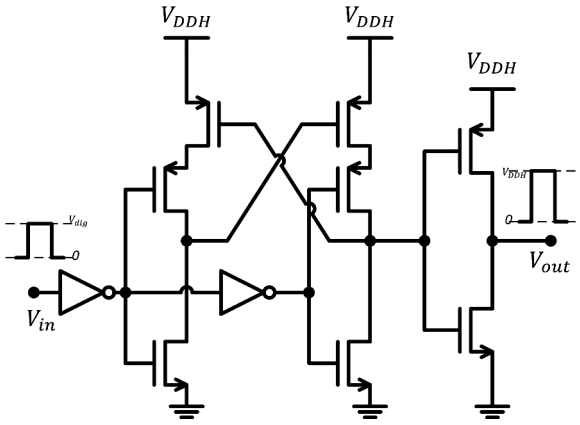


Figure 6.26: Basic low speed level shifter used for control signals $Turn\ off_{0...3}$.

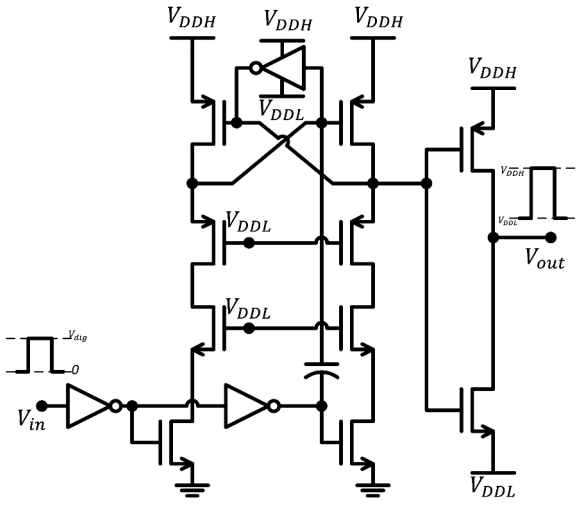


Figure 6.27: High speed level shifter used for SPWM signals.

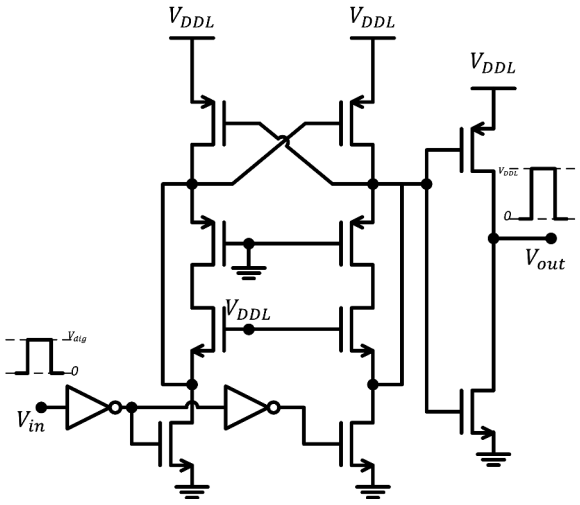


Figure 6.28: Dummy level shifter used for SPWM signals to equalize delays between paths.

6.7 Simulation Results

The design is simulated with a model for the wireless link as a transmitting coil, a receiving coil, and coupling factor k_{couple} between them. For a load $R_L$of 2 Ω, k_{couple} of 0.06, and supply voltage of 3 V, the output current at the terminals out_p and out_n is sinusoidal as shown in Fig. 6.29. Furthermore, the differential output voltage $out_p - out_n$ is indeed multi-level with observed five levels as shown in Fig. 6.30. The total harmonic

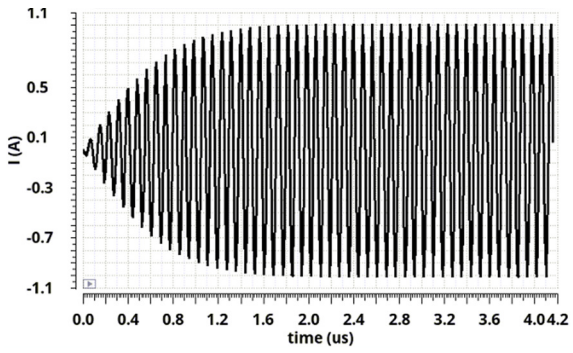


Figure 6.29: Transient time of the output current of the H-bridge circuit.

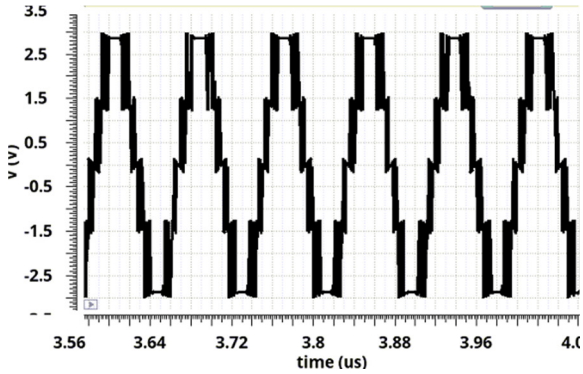


Figure 6.30: Transient response of the differential output voltage of the H-bridge circuit.

distortion was measured to be 2.8% for this differential output. The delivered output power to R_L is 1.137 W with efficiency of 50.6%.

To observe the performance of the system over different conditions, Figs. 6.31 and 6.32 show the contour plots of the delivered power to load and efficiency for different loads and coupling factors. As the coupling factor increases, the delivered power increases; however, the efficiency increases when the input-referred resistance of the transformer circuit is greater than the losses of the coils.

Different load resistances are used for the coupling factor of 0.06 while changing the setting of the number of segments. Fig. 6.33 shows an enhancement in efficiency as more segments are turned off since less power is consumed in the drivers; however, delivered output power is less as plotted in Fig. 6.34.

6.8 Experimental Setup

The proposed wireless power transmitter system was designed and fabricated using 0.13 μm CMOS technology. The die photo is shown in Fig. 6.35, the chip area is 1.5x1.5 mm^2 where the area of the power transistors, the drivers for both sides of the H-bridge, and the modulator/level-shifters/logics/comparators are 0.6x0.54 mm^2, 1.05x0.42 mm^2, and 0.61x0.28 mm^2 respectively. The proposed setup for the chip testing is shown in

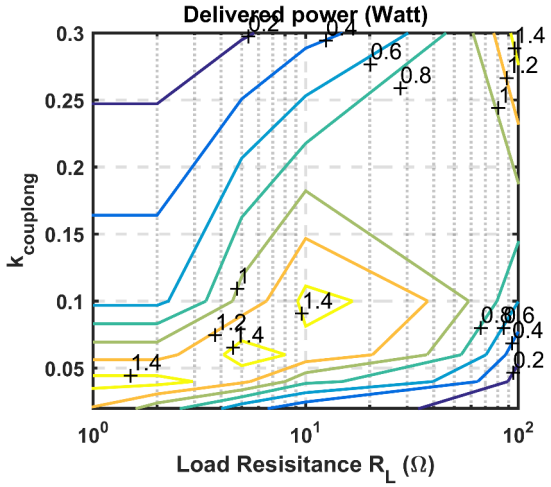


Figure 6.31: Delivered power to the load for different load resistances R_L and coupling factors k_{couple}.

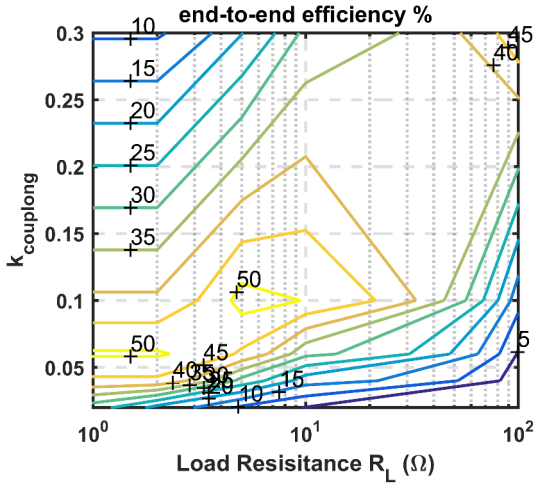


Figure 6.32: System end-to-end efficiency for different load resistances R_L and coupling factors k_{couple}.

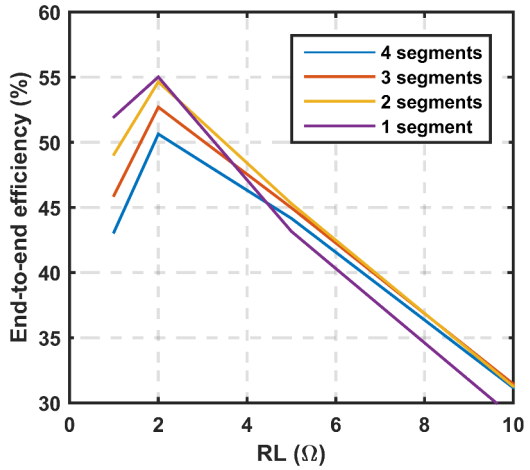


Figure 6.33: System end-to-end efficiency versus load resistance R_L for different segmentation settings.

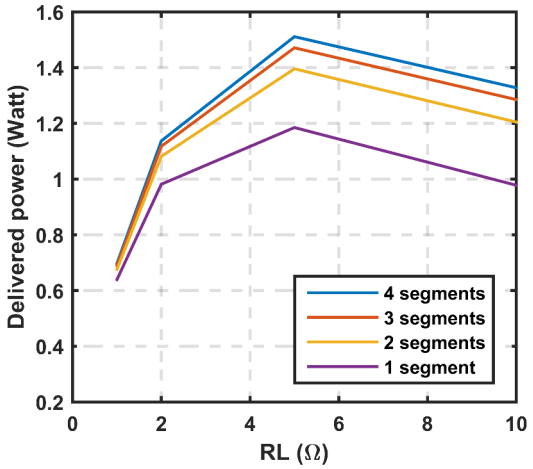


Figure 6.34: Delivered load power versus load resistance R_L for different segmentation settings.

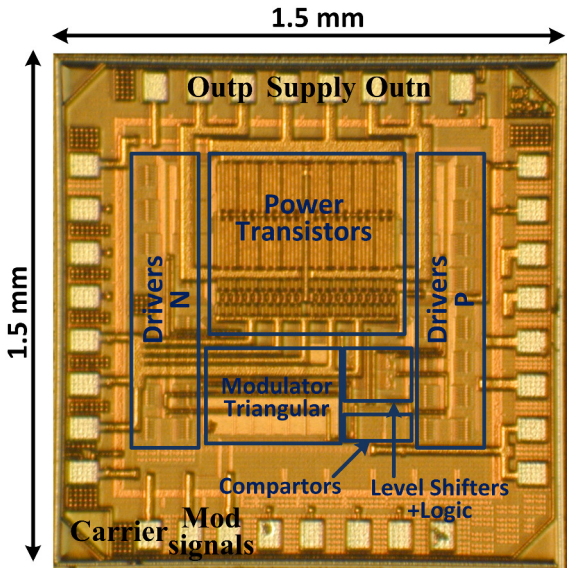


Figure 6.35: Micrograph of the wireless power transmitter prototype IC.

Fig. 6.36. Two Agilent 33120A waveform generators should be synchronized (from the back for the same reference and same trigger), one of them phase shifted, and both have a voltage offset of $V_{supply}/2$ to generate two out-of-phase sinusoidal reference signals. An RF signal generator with -10 dBm signal is used to generate the sinusoidal carrier signal (which will be processed by the chip to generate the required triangular signals). The differential output is either connected to an oscilloscope with a 50 Ω termination for

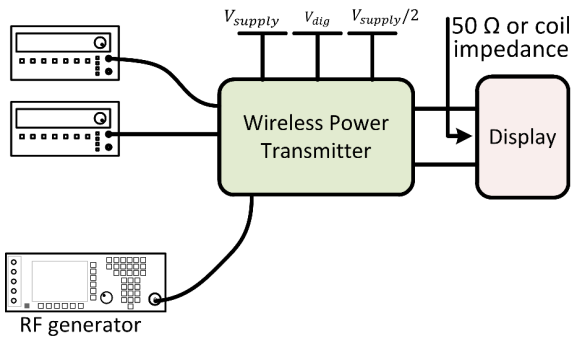


Figure 6.36: Test setup for the transmitter circuit.

waveform testing or the actual coil of the transmitter. Three supplies are needed.

6.9 Conclusion

An integrated friendly architecture for watt-level wireless power transmitters is proposed. A multi-level diode clamped inverter is used as the core dc to ac converter. The stress on each device is maintained for standard CMOS technology with a fundamental output voltage that is proportional to the number of levels, or series devices, used. Analysis of wireless inductive link as a resonant dc-dc converter is used where the performance with different loads is conducted. The design of Litz wire coils proofs to obtain good quality factors that directly affect the end-to-end efficiency of the system. The transmitter system is implemented on standard CMOS 0.13 μm technology which can enable the use of the same architecture in more submicron technologies that can be integrated with more advanced digital circuitry and processors.

7. AN INTEGRATED MULTIPLE-INPUT SELF-STARTUP ENERGY HARVESTING CAPACITIVE-BASED DC COMBINER

7.1 Introduction

Energy harvesting sources are environment−dependent which impose tough conditions on the loads, among them the different internet of things (IoT) applications. Different sources, such as solar, thermal, Piezo, RF, ... [83, 84, 85, 86, 42] have different energy densities [87] but they can be combined together to enable robust operation. For example, solar energy harvesting is reported to provide huge amounts of power provided the availability of light, or sun. With indoor conditions [88, 89], the harvested power is lower. When the source is not present due to shading, or raining, no power can be extracted and other energy harvesting sources, such as thermal energy harvesting [85, 88] can have important roles. The same is applied for other sources. Particularly, RF energy is reported to be the lowest energy density yet its robustness against environment change is a key advantage. In [90, 40, 91, 92, 93, 94], different approaches are used for multiple-source energy combining. In [90], more than two sources are harvested using time-interleaving and one external inductor. No concurrent harvesting is allowed where the strong source is utilized and the remaining available power from other sources are not used. Also, when none of the energy sources are available, it can be reconfigured as a reverse buck/boost converter to use the battery to power the load. Maximum power extraction is utilized by controlling the input impedance seen by each source. In [40], RF and thermal sources are used with circuits utilizing a separate RF rectifier and a boost converter for each, respectively and two dc outputs are obtained. Direct connection of the dc outputs is used where reverse currents from the combined output to any of the sources can degrade the performance. Matching at the RF source is done by external LC matching and maximum power point

tracking (MPPT) is used for the thermal source. Using low frequency inductive wireless power transfer and GaAs flexible solar cells in [91], the former is rectified and the latter is used for start-up or combined directly with the previous rectified dc output with no dedicated MPPT operation for the solar source. One switched capacitor circuit is used for the combination and an external inductor is used to deliver a boosted voltage to the final dc load. In [92], thermal and Piezo sources are used with a full-bridge and a half-bridge rectifier respectively. The full-bridge rectifier is used to enable positive-negative voltage inputs from the thermal generator. Then, the power path of the thermal source is connected through a super-diode to the power path of the impulsive Piezo source. The combined output is connected to a low dropout regulator (LDO) to provide regulated output to the load. This design utilizes forward-super-diodes in the power-paths to provide reverse isolation between the two sources, yet needs external power to provide the super−diodes with the required power consumption. In [93], parallel connection of the dc regulated outputs of the energy harvesting units are connected together to increase the total current capability, but the input voltage of each needs to be high enough to overcome the sensitivity of the harvesting circuits.

Self-startup is a crucial property for energy harvesting systems[95]. Switching-based energy harvesting needs oscillators for clock generation where ultra-low power [96] is important to enable high efficiency of the conversion and defines the minimum power/supply (sensitivity) needed from the source to operate the oscillator (in case of self-startup systems). Moreover, low voltage operation is important for the dc to dc converters[97]. Thyristor-based oscillators, composed of a number of cascaded delay cells, can be used for their inherited low-power high speed operation, yet operating with low supply voltage. The basic differential thyristor-based cell was introduced in [98], [99] proposed a single-ended version, and finally [100] proposed tuning for the single-ended design.

In this work, an integrated approach is proposed to combine dc power from different

sources. When one of the sources is ac, such as RF, it is assumed that a rectifier is used before the combiner circuit to convert to dc. The proposed system is shown in Fig. 7.1. Switched capacitor approach without any external passives is shown to be feasible for combining three sources ($Source_{IN}$, $Source_1$, and $Source_2$) extendable to more sources. The basic concept is to convert one of the dc inputs to ac (dc to ac conversion), superimpose this waveform on the other dc input, and then do ac to dc conversion. The contributions of this work are: 1) a modular approach for capacitive-based dc energy combining suitable for self-startup operation, dealing with weak and strong sources simultaneously, and boosting up the final load voltage, 2) a proposed thyristor-based differential tunable oscillator to enable maximum power extraction and at the same time, input impedance tuning at the interfaces of the harvesting sources, and 3) different definitions for power conversion efficiencies are discussed and how they are related to traditional microwave amplifier design with the goal of differentiating between input matching, dc-dc converter losses, and output matching.

7.2 Different Power Gain Definitions and Relation to Microwave Amplifier Design

In microwave amplifier design, different power gain definitions are used. Consider an arbitrary two$-$port network, connected to source and load resistances R_S and R_L, respectively, as shown in Fig. 7.2 (Here, we have used real parts only). There are three types of power gains[62]: Power gain $= G = P_L/P_{in}$ is the ratio of power dissipated in the load R_L to the power delivered to the input of the two-port network. This gain is independent of R_S and assumes that there is matching (conjugate matching in the case of high frequency amplifiers) between the source R_S and the input resistance of the network. The input power is calculated by simply not taking the source into account. Thus, the value G takes into account the mismatch at the output of the network and assumes matching at the input. Secondly, the available power gain $= G_A = P_{avn}/P_{avs}$ is the ratio of the power

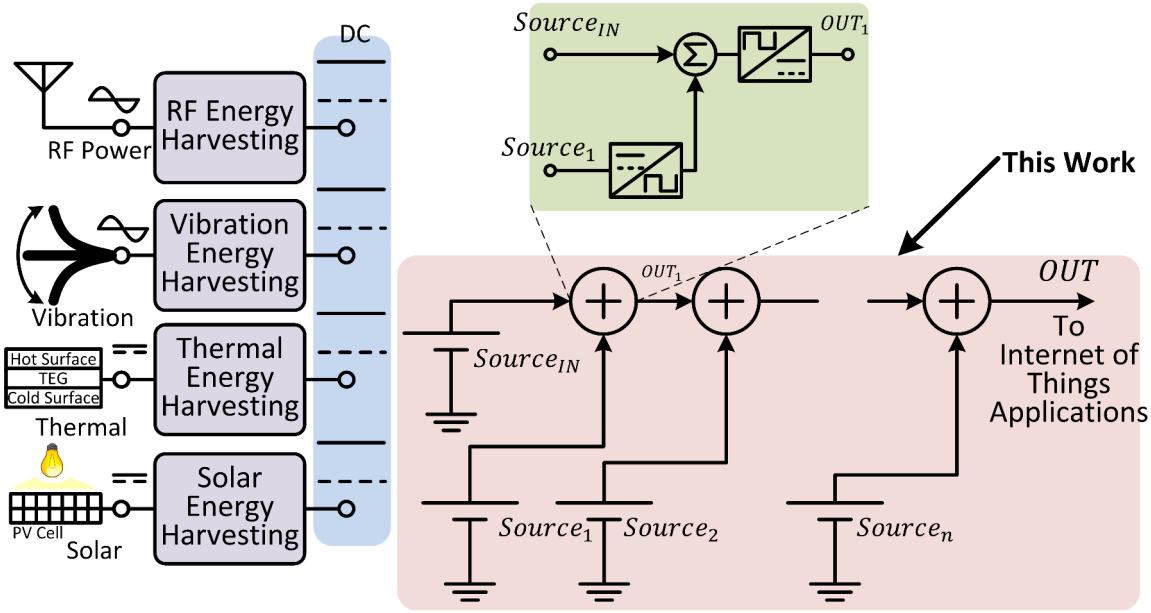


Figure 7.1: Proposed multi-input energy harvesting combiner and the energy flow to the possible applications.

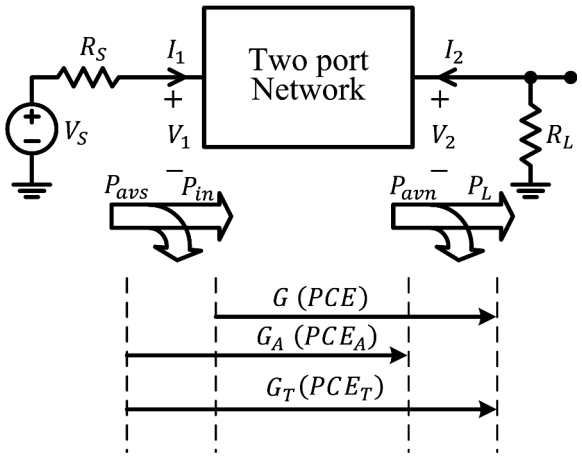


Figure 7.2: Two-port network with various definitions of power gains.

available from the two-port network to the power available from the source. This assumes matching of the load, the source resistance can take any arbitrary value, and depends on R_S, but not R_L. The available power from the source P_{avs} is calculated for the case as if there is matching at the input which gives the maximum power to be extracted from the source although this condition is not imposed in the calculation of the output available power. Thus, the value G_A takes into account the mismatch at the input of the network and assumes matching at the output. Thirdly, the transducer power gain $= G_T = P_L/P_{avs}$ is the ratio of the power delivered to the load to the power available from the source. This depends on both R_S and R_L and the value of G_T accounts for both source and load mismatch. With simultaneous input/output matching, maximum transducer gain $G_{T,max}$ is obtained and there could be some concerns for stability.

In dc-dc converters, power conversion efficiency (PCE) is the term used for power gain. So, the previous three power gains are renamed: PCE, available PCE (PCE_A), and transducer PCE (PCE_T). Sometimes, the term PCE_T is referred to as the end-to-end efficiency which is maximized when simultaneous matching for the source and load is achieved with low loss converter. In this work, the focus is on switched capacitor dc-dc converter while the above definitions are suitable for any dc-dc converter.

In [101, 41], the steady-state dc behavior of a switched capacitor dc-dc converter is modeled as an ideal transformer with $1 : A$ where A is the ratio between the output voltage V_2 and the input voltage V_1 (V_2/V_1) when the load is open-circuit. An output resistance R_o is added to model the losses of the converter which is frequency f and architecture dependent. At low frequencies, $R_o \propto 1/f$ and this is called slow switching limit and at high frequencies, the value of R_o is constant and this is the fast switching limit. The highest efficiency is obtained at low frequency while the lowest area of the converter is achieved at high frequencies. As a consequence, the transition point between the two limits is considered the best compromise.

The previous model fails to predict the input impedance at light load (the load is open circuit). In [102], a parallel resistive element $R_i = 1/G_i$ at the input is proposed. It represents the input resistance (losses) when the load is open circuit. Moreover, dependent voltage and current sources are used between the source and the load which can be shown to be equivalent to the traditional ideal transformer model in [101, 41]. So, the proposed model for the switched capacitor circuit is shown in Fig. 7.3 where the inverse hybrid two-port equations are:

$$\begin{pmatrix} I_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} G_i & -A \\ A & R_o \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix}, \tag{7.1}$$

where A is the open circuit conversion ratio, G_i is the input conductance when the load is open circuit, and R_o is the output resistance when the input is short circuit. This is a steady−state model that is valid in the slow switching limit [102]. It should be mentioned that conversion to ABCD parameters can be utilized to enable general expressions for the cascade of dc-dc converters. It can be derived that the PCE, which assumes input matching (no effect from the source resistance), is given by:

$$PCE = \frac{A^2}{(R_L + R_o)^2} \frac{R_L}{\left(G_i + \frac{A^2}{(R_o + R_L)}\right)}, \tag{7.2}$$

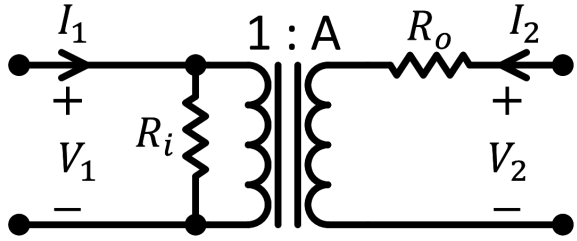


Figure 7.3: Steady-state slow switching limit model for switched capacitor dc-dc converters.

and the expression for PCE_A, which assumes output matching, is:

$$PCE_A = \frac{A^2 G_S}{(G_i + G_S)^2 \left(R_o + \frac{A^2}{(G_i+G_S)}\right)}, \tag{7.3}$$

where $G_S = 1/R_S$ is the source conductance and when no matching is assumed at the input nor the output, the transducer efficiency PCE_T is:

$$PCE_T = \frac{4A^2 R_o G_S}{\{(G_i + G_S)(R_o + R_L) + A^2\}^2}. \tag{7.4}$$

Fig. 7.2 illustrates the difference between the definitions of the power conversion efficiencies. When there are simultaneous input/output matching conditions, the PCE_T can be maximized which is given by:

$$PCE_{T,max} = K - \sqrt{K^2 - 1}, \tag{7.5}$$

$$K = \frac{2G_S R_o}{A^2} + 1 > 1. \tag{7.6}$$

Finally, for multiple-input dc-dc converter, a generalized circuit model, shown in Fig. 7.4, is proposed.

For a fixed voltage at input, i.e. no input matching effects, the reported efficiency is PCE or $PCE_{T,max}$ when maximum power point tracking is used. However, when actual energy harvesting sources with finite source impedances are used and the output power is sensed for maximum power extraction i.e. output matching, the reported efficiency can be either $PCE_{T,max}$ or PCE_A depending on the input matching is forced by a different loop or not.

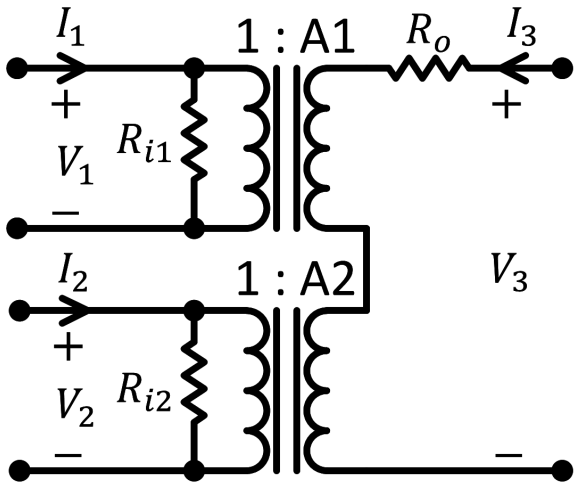


Figure 7.4: Steady-state slow switching limit model for multiple-input switched capacitor dc-dc converters.

7.3 Circuit Implementation

The proposed basic circuit to combine two dc sources ($Source_{IN}$ and $Source_1$) is shown in Fig. 7.5. Two-phase structure is used to overcome the use of bootstrapping circuits for switch control [103]. Single-phase switched capacitor circuits can be transformed to two-phase cross-coupled structures [104] where this is only one example. The dc source $Source_1$ is converted to ac through the use of the oscillator I_o with two out-of-phase signals that drive the drivers I_1 and I_2. The capacitors C_1 and C_2 act as short-circuit at ac and open-circuit at dc, so the intermediate signals v_{i1} and v_{i2} have a peak to peak voltage approximately as the signal after the drivers while the dc shift can be defined from another path. The path composed of the pair of devices M_1 and M_2 defines the dc values at the intermediate nodes. The pair of devices M_3 and M_4acts as a full wave rectifier and the dc signal OUT_i is smoothed with an output capacitor (not shown here). A three input, $Source_{IN}$, $Source_1$, and $Source_2$ combiner circuit is shown in Fig. 7.6. The sources $Source_{IN}$ and $Source_1$ are combined as was shown in Fig. 7.5 and the resultant is com-

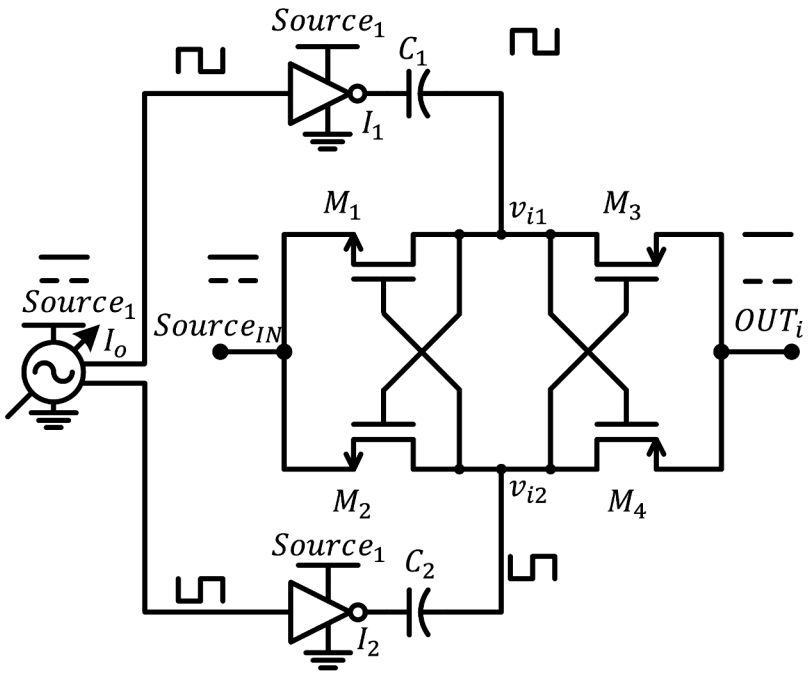


Figure 7.5: Proposed two-source combiner derived from traditional voltage doublers.

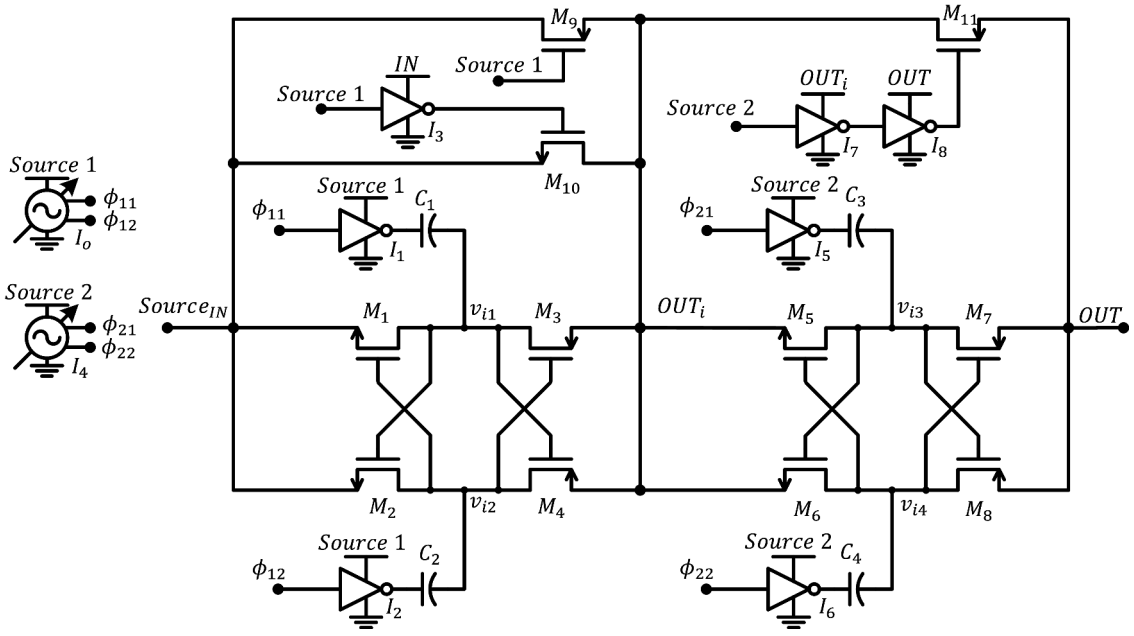


Figure 7.6: Proposed three-input doubler-based dc energy combiner.

bined in series with input $Source_2$ in the same manner. Two oscillators are needed for dc to ac conversion from each source and different frequencies are needed since the source resistance R_S is not the same for the two sources. The input impedance seen by each source can be tuned to be matched to the source resistance by either capacitor tuning [83] or frequency tuning where the latter is used here to obtain better efficiency both at light load and heavy load. In the case that voltage of $Source_1$ ($Source_2$) is low such that the oscillator I_0 (I_1) is not working, the devices M_1, M_2, M_3, and M_4 (M_5, M_6, M_7, and M_8) are bypassed by the transmission gate M_9 and M_{10} (device M_{11}). If the voltage at OUT_i is low, i.e. sources $Source_{IN}$ and $Source_1$ are weak, device M_{11} is ON when output OUT is low. Also, device M_{11} is OFF when signal OUT is high and signal OUT can ramp up if $Source_2$ is present. The implemented voltage controlled oscillator (VCO) is shown in Fig. 7.7. The two differential delay cells D_1 and D_2 are in a positive feedback. To ensure non-overlapping output signals ϕ_1 and ϕ_2 and duty cycle correction, the standard circuit composed of the NAND gates I_1 and I_2, drivers P and N, and buffer inverters I_3 and I_4 is implemented for the differential outputs O_1 and O_2. The proposed tunable thyristor-based delay cell is shown in Fig. 7.8. The first thyristor is composed of M_1, M_2, M_3, and M_4 while the complementary thyristor consists of M_6, M_7, M_8, and M_9. This internal positive

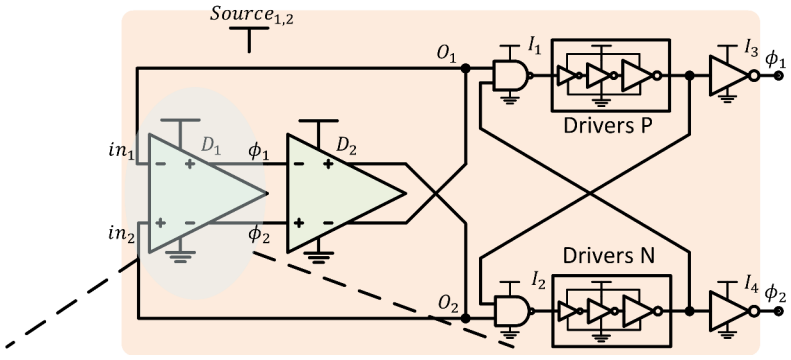


Figure 7.7: Two-stage differential voltage controlled oscillator with extra non-overlap protection in cascade.

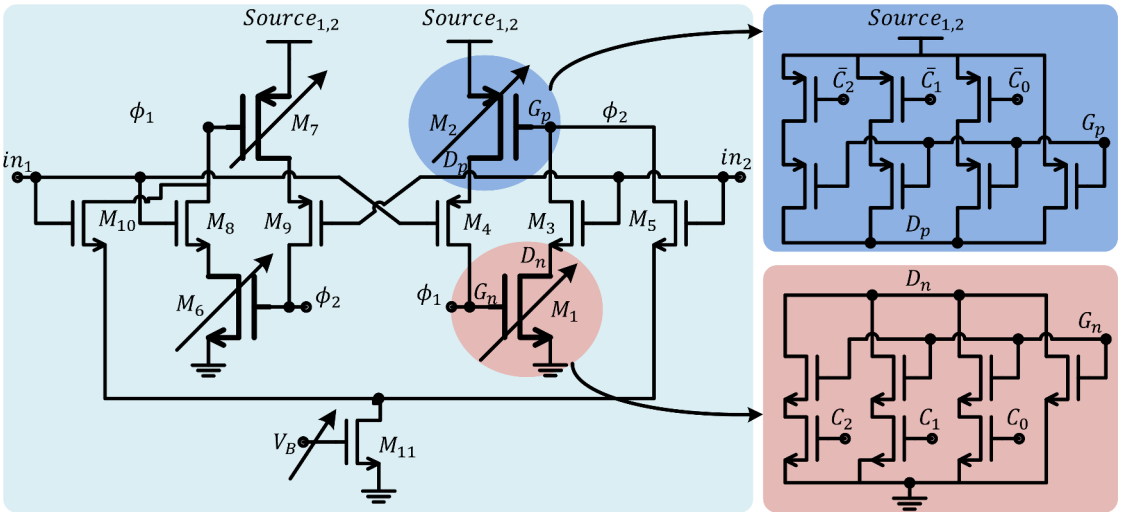


Figure 7.8: Proposed tunable differential delay cell based on the thyristor concept.

feedback ensures sharp edges when the output signal raises above the threshold voltage of the thyristor. This can reduce the shot-through currents [100] which reduces the power consumption of oscillator yet operating at high frequencies and lower supply voltages. The differential pair M_5 and M_{10} sets the initial condition for the thyristor blocks. The delay of the delay cell depends on the current of the differential pair as well as the equivalent area of the Thyristors, i.e. the size of devices $M_1 - M_6$ and $M_2 - M_7$. Tuning both as proposed is an effective way to tune the delay cell and the corresponding oscillator shown in Fig. 7.7.

7.4 Experimental Results

The proposed dc energy combiner system was designed and fabricated using 0.13 µm CMOS technology. The die photo is shown in Fig. 7.9 with an area of 1.5x1.5 mm^2. This includes the actives switches, the MIM capacitors, and the oscillators. The oscillation frequency of the integrated oscillator is measured while varying the analog and digital controls for different input voltages, i.e. different supply voltages V_{DD} shown in Fig. 7.7. The test results are shown in Fig. 7.10. To show the effectiveness of the digital control,

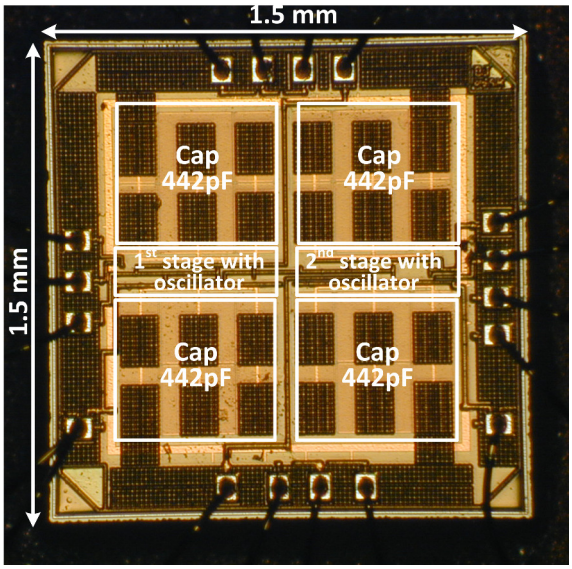


Figure 7.9: Micrograph of the three-input dc power combiner prototype IC.

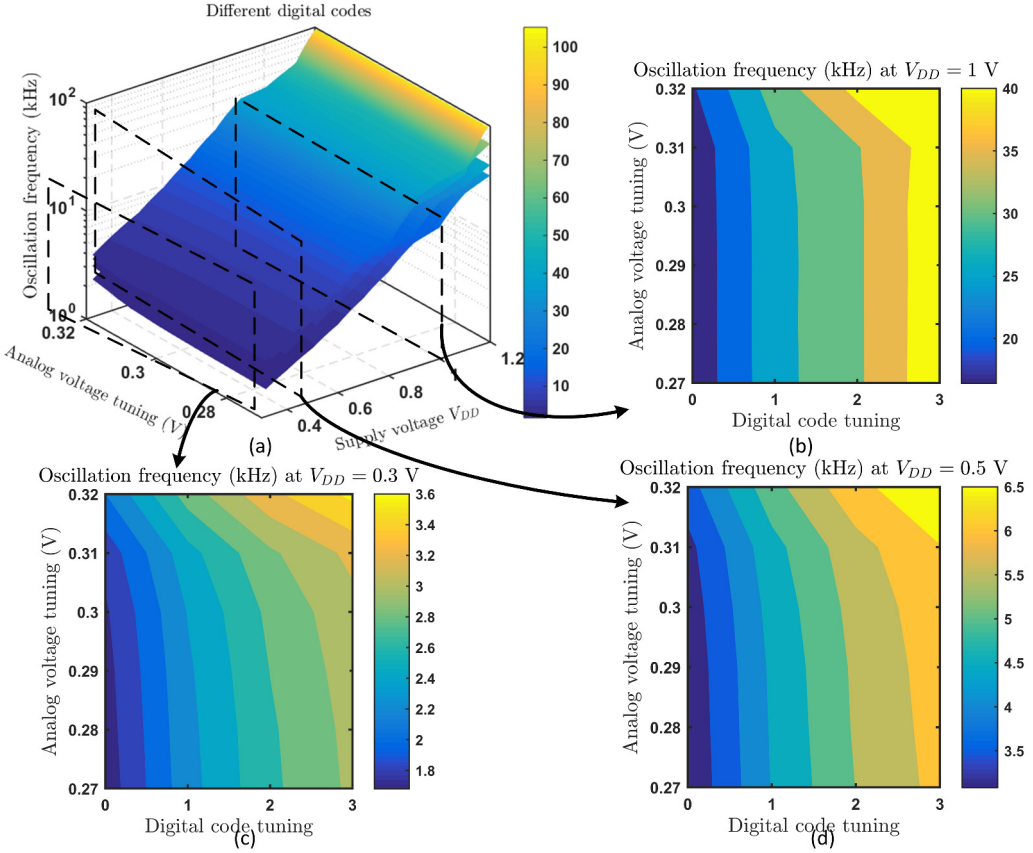


Figure 7.10: Measurement results of the tunable oscillator.

cross sections of the 3D plot at $V_{DD} = 0.3, 0.5$, and 1 V are shown as well. The analog control is obtained by an external peaking current mirror, shown in Fig. 7.11 in order to maintain adequate current, in the range of μA on the printed circuit board control, but the input current can be in the range of nA. The digital control extends the operating frequency of the oscillators by 2X.

Then, the test setup to characterize the proposed chip is shown in Fig. 7.12. Each input of the three inputs $Source_{IN}$, $Source_1$, $Source_2$ is tested separately. The output power and efficiency are measured for different loads R_{load} and different input voltages as shown in Figs. 7.13a, 7.13b, and 7.13c. When $Source_{IN}$ is tested, it doesn't matter the condition of either $Source_1$ or $Source_2$ to be open-circuit or short-circuit. However, when $Source_1$ ($Source_2$) is tested, $Source_{IN}$ should be grounded since the dc current flow depends on this condition and the condition of $Source_2$ ($Source_1$) can be open-circuit or short-circuit. The best performance is obtained from $Source_{IN}$ since the other sources $Source_1$ and $Source_2$ involve dc-ac and ac-dc conversions. Moreover, the minimum voltage required for the oscillator operation is measured to be 0.26 V (the input voltage needs to reach 0.6 V or higher to start the oscillation and the oscillator can sustain oscillation for any input higher than 0.26 V). For $Source_{IN}$, the PCE is higher than 90% for the different inputs and loads and the peak throughput power is 1.84 mW obtained at heavy load and maximum tolerable voltage 1.5 V by the CMOS process. The throughput power obtained from $Source_1$is better than the ones obtained by $Source_2$. The power consumption of the oscillator is added as a power loss factor which is different between both sources. The frequency is tuned such that maximum power is obtained at the output. The higher operating frequency, the more power consumption with more efficient operation. That is why it is preferable to operate at low frequency as light loads. The maximum efficiencies when $Source_1$ and $Source_2$ are present are comparable which are 56.1% and 58%.

The test results using two active sources at a time are shown in Figs. 7.14a, 7.14b, and

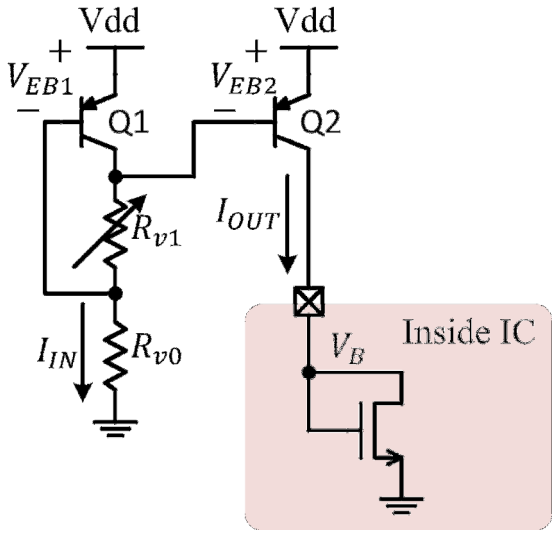


Figure 7.11: Peaking current mirror to obtain a large ratio between currents.

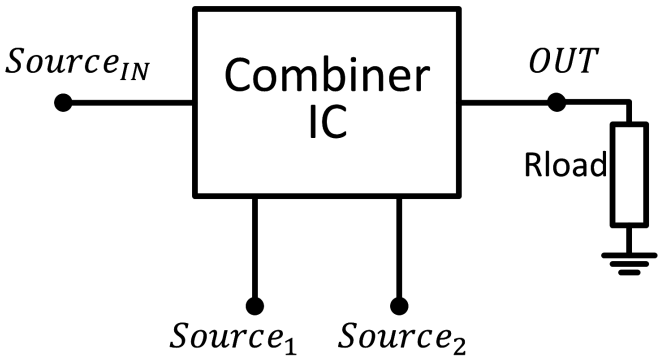
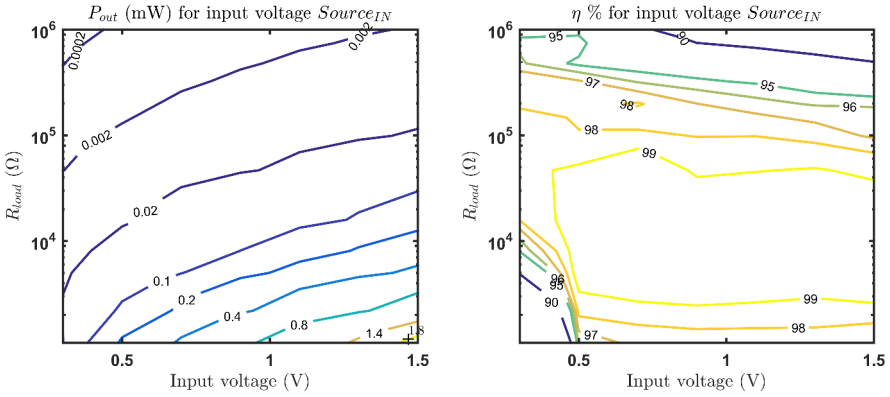
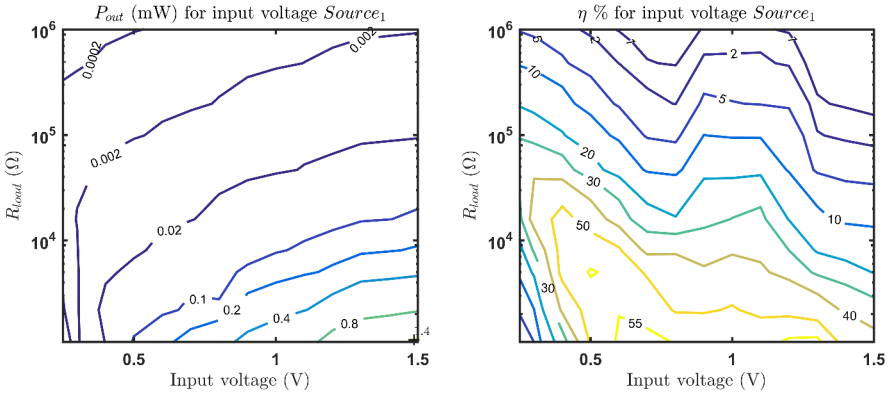


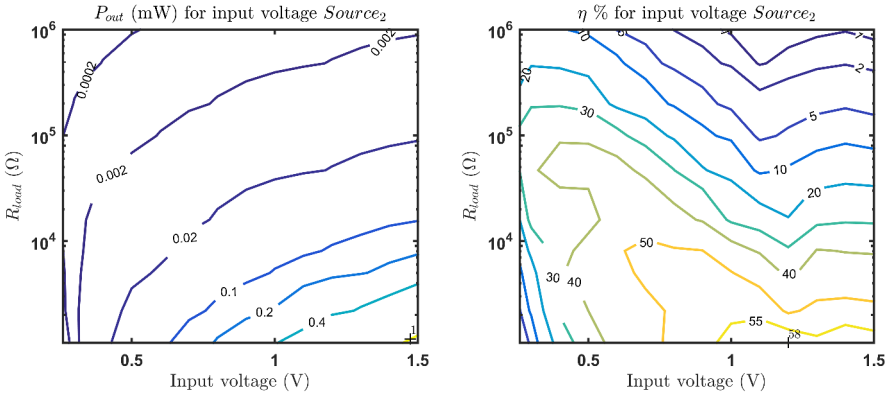
Figure 7.12: Test setup for chip characterization.



(a)



(b)



(c)

Figure 7.13: Measurement results of the output power and efficiency for different loads R_{load} and the input source: (a) $Source_{IN}$, (b) $Source_1$, and (c) $Source_2$.

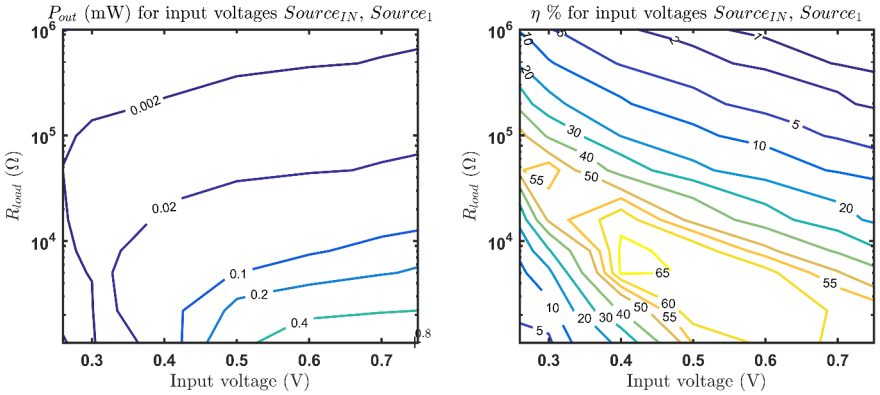
7.14c. The proposed topology adds power from two sources and the light load efficiency is improved with the use of frequency modulation. The maximum voltage is limited to 0.75 V for reliability of the CMOS devices. The efficiency is calculated as the output power divided by the total input power. The curves show clearly the difference between peak throughput power and peak efficiency operating points. When $Source_{in}$ is used with other source, the peak efficiency is higher (66% and 76% with $Source_1$and $Source_2$ respectively), near to 100 μW output power at an input voltage of 0.45 V, and a load resistance of 10 kΩ. When all sources are applied, as shown in Fig. 7.15, the total power throughput is higher. Again, the peak efficiencies depend on the frequency of operation of the oscillators and which inputs are applied.

In order to test the energy combiner with actual energy harvesting sources, three different solar cells are used for that and the test setup is shown in Fig. 7.16. Two parallel solar cells of the type SLMD121H09L are connected to source $Source_{IN}$. A small solar cell, SS13-70x65, is connected to source $Source_2$. Finally, a flexible solar cell, PowerFilm, is connected to source $Source_2$. The testing is conducted in the lab with typical indoor conditions at 12:00 PM where the load R_{load} is varied. The test setup for the three solar cells along with the proposed test chip is shown in Fig. . The output voltage versus load current is plotted in Fig. 7.17a which shows an open circuit voltage around 1.4 V and a short circuit current of 160 μA. The output power is recorded and plotted in Fig. 7.17b where the peak power is measured to be 70 μW at a load of 10 kΩ.

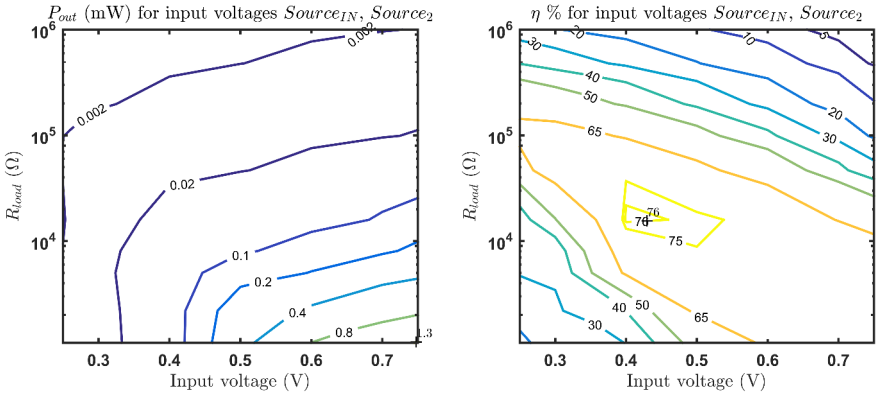
Table 7.1 includes a performance summary for the energy harvesting unit. Table 7.2 shows a comparison table with other energy harvesting systems.

7.5 Summary

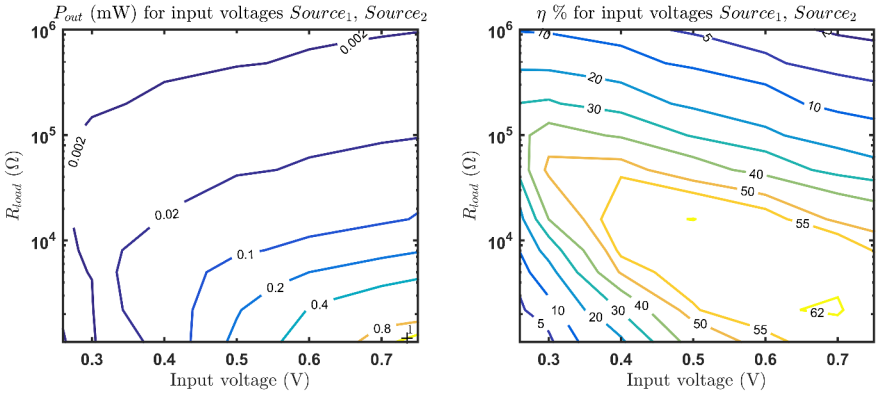
Using a linear steady-state model for the switched converters and the knowledge of different gain definitions of microwave amplifiers, input matching, dc-dc converter losses,



(a)



(b)



(c)

Figure 7.14: Measurement results of the output power and efficiency for different loads R_{load} and the input source: (a) $Source_{IN}$ and $Source_1$, (b) $Source_{IN}$ and $Source_2$, and (c) $Source_1$ and $Source_2$.

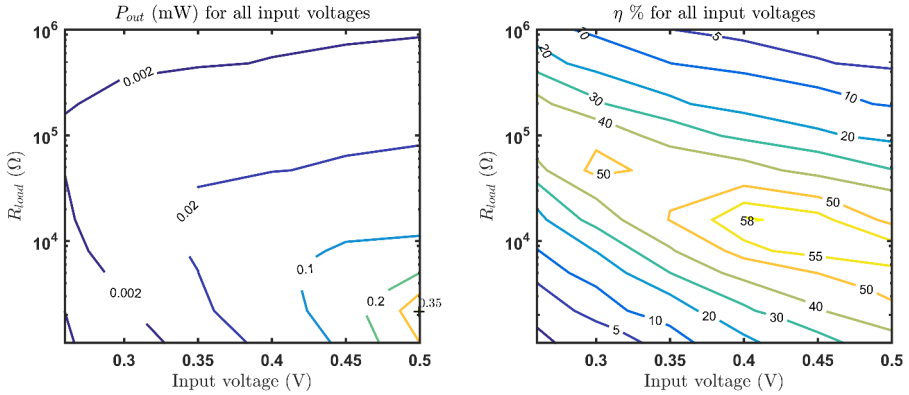


Figure 7.15: Measurement results of the output power and efficiency for different loads R_{load} and input voltages $Source_{IN}$, $Source_1$, and $Source_2$.

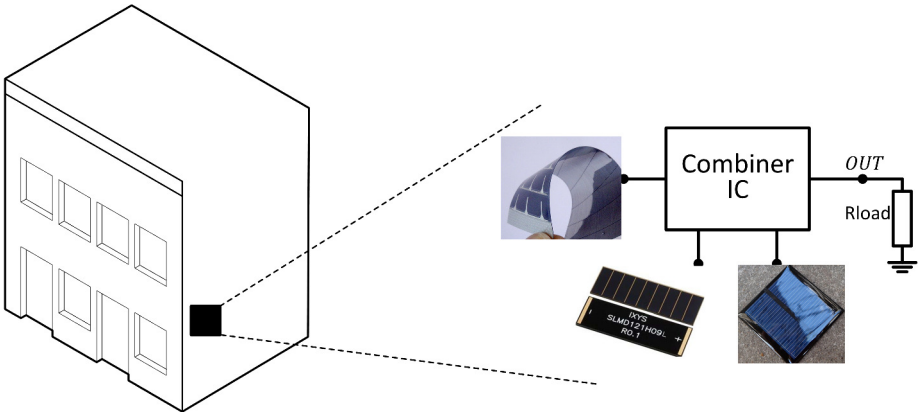
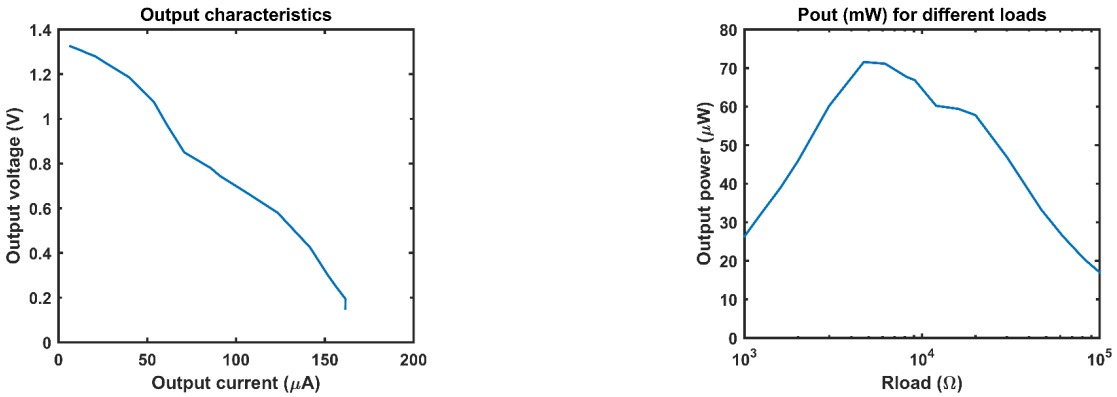


Figure 7.16: Test setup for three different solar cells.



(a) (b)

Figure 7.17: Measurement results using three different indoor solar cells for (a) output voltage versus output current and (b) output power for different load R_{load}.

Table 7.1: Performance summary for the dc combiner.

	Input voltage range (V)	Maximum output power (μW)	Maximum PCE (%)
$Source_{IN}$	0.26-1.5	1840	99.9
$Source_1$	0.26-1.5	1461.1	56.1
$Source_2$	0.26-1.5	1086	58
$Source_{IN}$&$Source_1$	0.26-0.75	810.6	66
$Source_{IN}$&$Source_2$	0.26-0.75	1321.1	76.4
$Source_1$&$Source_2$	0.26-0.75	1090	62.6
All sources	0.26-0.5	354.4	58.4

Table 7.2: Comparison with other multiple-input energy harvesting systems.

	JSSC,16 [1]	JSSC,14 [2]	TIE,14 [3]	JSSC,13 [10]	JSSC,14 [11]	TIE,12 [17]	This Work
Architecture	Capacitive	Capacitive	Inductive	Inductive	Inductive+ capacitive	Inductive	**Capacitive**
Number of inputs	1	1	1*	2	2	1	**3**
MPPT control	Frequency + capacitance, auto	Frequency, manual	Frequency, auto	–	Frequency, auto	–	Frequency, manual
Input voltage range	450-3000 mV	140-500 mV	20-150 mV	30 mV	N.A.	100-500 mV	**260-500 mV****
Maximum output power	**50**	5 μW	359 μW	397 μW	943 μW	286 μW	**354.4 μW****
Maximum PCE	81%	50%	61%	38%	72%	30%	**58.4%****
CMOS technology	180 nm, IO devices	180 nm	500 nm, high voltage	130 nm	180 nm	180 nm, Low threshold	130 nm, standard

*: An external impedance array connected all of its elements in series or parallel through discrete MOS switches controlled by an external clock

**: input voltage is limited by the device reliability of the process. For single input, this goes up to 1.5 V

and output matching can be differentiated. A multiple-input self-startup switched capacitor topology is proposed for N-inputs. A fabricated chip for 3-inputs, where more inputs can be incorporated in future designs, is measured and tested. Thyristor-based oscillators are used for robust and low power/voltage operation. The system showed that the output power is combined from the different input sources and delivered to the load. Automatic MPPT algorithms can be incorporated for future designs for optimal and robust performance.

8. SUMMARY AND FUTURE WORK

This work is focusing on RF energy harvesting, multiple-input dc energy combining, and wireless power transfer from integrated circuits point of view. Modeling and understanding the issues associated with these technologies are primary objectives of this study. From that basis, solutions are proposed to tackle the associated barriers and enhance performance. Ultra-low power and high power watt-level circuits are investigated and shown to be feasible for standard CMOS technologies to enable cheap solutions. The RF energy can be harvested and either stored in a buffer capacitor or used directly by dc loads. New materials with high quality factors can enable harvesting from lower input powers than -30 dBm but the bandwidth will be very narrow. Integration versus robustness was demonstrated. The concept of energy is vital in dealing with energy harvesting world where time is needed to collect energy which can be used instantaneously to power high demand loads such as wireless transmitters.

Section 2 showed a comparative study between an on-chip matching network and an off-chip matching network. It also examined the sensitivity effect of each design strategy. The RF rectifier at the sensitivity limit was analyzed and the input-output relationship was quantified. The input impedance of the RF rectifier proved to be mainly capacitive. It has been confirmed that the on-chip matching network offers a flexibility of tuning as well as integration for a more robust design. On the other hand, the off-chip matching network gave a better sensitivity along with higher cost due to bulky off-chip matching elements. This work shows that better matching elements will lead to the success of RF energy harvesting to harvest from very low levels of the incoming signals. Also, it shows how the integrated CMOS RF energy harvesting systems can be analyzed and the limits of the system.

Section 3 presented a fully integrated system with an LC matching network, RF rectifier, clock generation, voltage reference and power management/control circuitry, yet the system features a self-startup operation with no external supply help. The full integration of all functionalities on a single CMOS chip proves to be a promising low-cost solution. In order to increase the available output power, a novel reconfigurable modular RF rectifier circuit is presented. The dc power is delivered to the load only, when the voltage on the load can reach the desired voltage; otherwise, the power management waits until this condition is satisfied and delivered power is duty cycled. Moreover, the extra available output power can be stored for future usage. This two-path power delivery scheme enables the support of real-time loads, increases the extracted power from the RF front end, and stores the extra power in external storage elements. For the proof of concept, only one secondary path is used, but multiple secondary paths can be incorporated to enhance the extraction capability of the extra available power at the expense of more complex logic circuits. Finally, a new circuit for non-overlapping level shifters is proposed and used in the design to overcome shoot-through power loss.

Section 4 introduced the use of RF energy harvesting with a wireless receiver where out-of-band blockers are harvested and used to power-up the receiver. The design demonstrated that using the same antenna is feasible. The ultimate goal is to design batteryless designs in the future. Furthermore, decreasing the noise and nonlinearity effects introduced by the harvesting unit is of great importance.

Section 5 introduced the different antenna parameters and how this can affect the design of RF energy harvesting. Furthermore, differential to single ended conversion is shown to make it possible to use differential antennas with single ended RF rectifiers.

Section 6 showed a watt-level wireless power transmitter and digital modulator where both are integrated on the same chip. Analysis of the wireless link is done that shows how the values of the passive elements affect the performance of the system specifically

efficiency across different loads. Furthermore, segmentation is used to improve the light load efficiency. Multi-level diode-clamped inverters are used for low total harmonic distortion (THD). Guidelines for the design of Litz wire coils are obtained and how properly simulate these elements.

Section 7 introduced a novel switched capacitor self-startup topology for multiple input energy harvesting systems. If one or more of the sources are weak, the load still gets the combined power from all sources. A new framework for different efficiency definitions was introduced to assist energy harvesting system designer. Finally, a new tuning methodology for differential thyristor-based oscillator was introduced.

8.1 Future Work

8.1.1 Synergic Design of Antennas and Power Management for RF Energy Harvesting

For wireless transmission and reception, antennas are used to convert electrical signals to electromagnetic signals and vice versa according to the principle of duality. A receiving antenna followed by an ac to dc conversion is used for RF energy harvesting. The available technologies to power-up Internet of Things (IoT) devices are: non-rechargeable batteries, rechargeable batteries, printable batteries, solid-state batteries, super capacitors, and energy harvesting. Developing a green IoT technology based on harvesting energy from naturally available sources is one of the current research trends that avoid the use of external batteries and/or connection to a wired permanent power source. However, this technology is not yet mature enough for commercial use.

The sensitivity of the RF energy harvesting system is limited by the design of the antennas and the various types of losses. Losses of the matching network, inserted between the antenna and the RF rectifier circuit, and the RF rectifier switches are limited by the available technology. On the other hand, antenna gain plays an important rule to

enable highly-sensitive RF energy harvesting. Highly directive antennas along with high efficiency can enable harvesting from lower available RF powers, -40 dBm and below. These levels and below are the typical maximum power for the RF wireless communications, provided that the transmitting tower location is not known. High directivity comes with the narrow beam-width for reception where the antenna can harvest only from certain limited directions. Furthermore, the use of antenna arrays enables more harvested power. When arrays are used, power combining loss is an issue which adds to the aforementioned losses. The antenna element can have many variant and multi-band is of interest, yet resonance should be the case for the best area efficiency. With all the above trade-off in mind, it is proposed portable multi-band RF energy harvesting antenna array with the RF front-end and power management circuits in the size of a computer tablet. The RF front-end and the power management will be integrated on the same die for low cost and robust solutions. Two approaches will be investigated as shown in Fig. 8.1: RF power combining and the use of one RF rectifier chip versus the use of multiple RF rectifier chips and one dc power combining. The former suffers from feeding/combining network loss and area waste but the received power from antennas are higher at the input of the RF rectifier which can enable operation above the sensitivity of the RF rectifier. The properties of the latter are the exact opposite of the former. The target is to harvest RF input powers below -40 dBm range where each topology will be investigated and the trade-offs to achieve that tough requirement will be demonstrated.

In principle, an array of N identical elements yields a factor of N in the antenna gain (and the received power is proportional to effective antenna gain). If the received power from one antenna is P_a, the ideal received power from the array is NP_a. However, the losses in the combining structure can lower this multiplication factor and increases with the number of elements to be combined. Our target is to keep this loss below 70 such that the total received power is in the order of $0.7NP_a$.

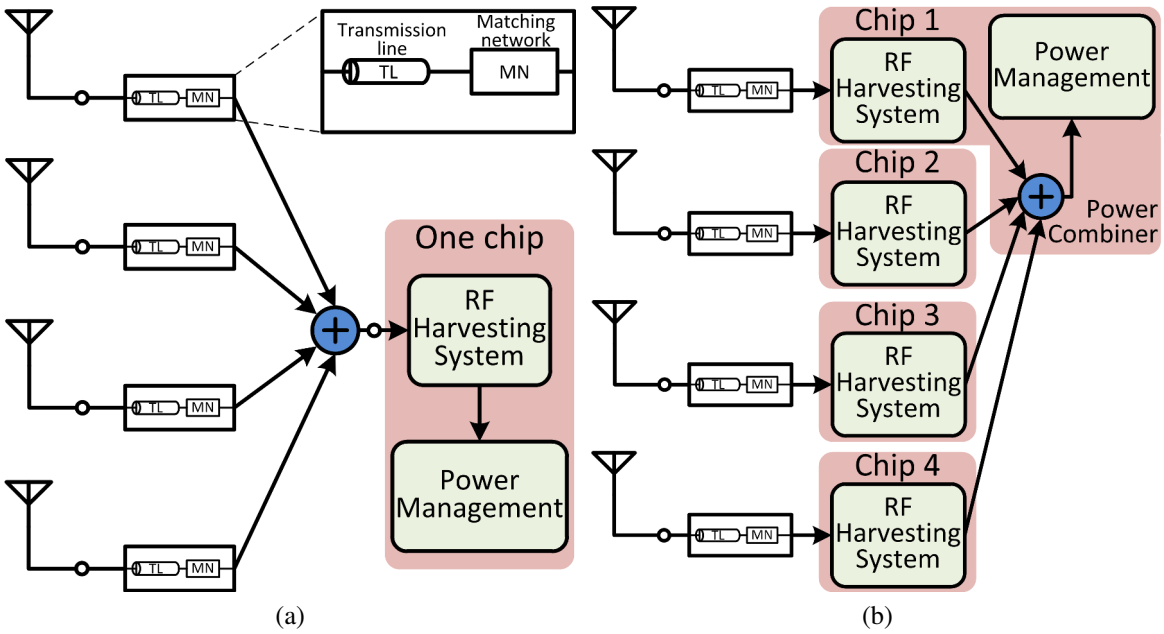


Figure 8.1: Proposed designs for RF energy harvesting system: a) one chip: adding power then rectify, and b) multiple chips: rectify then combine dc powers.

The literature of RF energy harvesting is diverse which is traced back to the far-field wireless power transmission experiments by Nicola Tesla and later Radio Frequency Identification Device (RFID) technology. Both of these are harvesting from a known source with expected direction and received power levels. In the recent applications, the source could be weaker than it used to be and more area can be used for the purpose of enabling the technology (RFID cards have limited area which impose a trade-off on the antenna design). In the literature, off the shelf high performance RF devices with arrays, known as Rectennas, can be used but they are costly, designed for high power throughput, and sensitive to environment changes. On the other hand, integrated RF front ends were shown to be an optimal customized and cheap solution although not as highly sensitive as the high-end devices. Lastly, ultra-low power management for use of RF energy harvesting is lacking where performance of the circuit can be traded-off with power consumption.

So, here in this work, arrays with integrated RF front ends and power management are designed together to get the benefits of integration yet collecting more power and enabling highly sensitive operation. In summary, what is proposed is mainly different from previous work on targeting low power portable applications which needs portable antenna arrays and ultra-low power custom designed management circuits.

8.1.2 Wireless Power Transmitter

Wireless power transmitter is responsible for dc to ac conversion of electrical power. The proposed design as shown in Fig. 8.2 is a differential class D architecture with high efficiency 80% and fully integrated solution. In order to control the switched amplifier, sinusoidal pulse width modulation (SPWM) is used where a sinusoidal signal f_o is modulated by a fixed frequency f_c triangular carrier. The output is a square-wave like signal which has odd harmonics at $3f_c$, $5f_c \ldots$ with the a relative ratio to the fundamental equals to $1/3$, $1/5 \ldots$ In order to lower the total harmonic distortion (THD) at the output, spread spectrum for the carrier clock is used. Spread spectrum generally makes use of a sequential noise-like signal structure to spread the normally narrow-band information signal over a relatively wide-band (radio) band of frequencies. Feedback is introduced to reconfigure the control signals to adapt the transmitter with variable nature of the wireless inductive link. Integration of the switching amplifier, digital control, and sensing circuits is the aim of this work which demonstrates the possibility of using CMOS 0.18 μm high voltage technology for this task.

Finally, the previous descriptions are for unbalanced (single-ended) designs. H-bridge configurations can be used, as will be shown, to enable differential (balanced) operation where two-phases are used to drive the load, which is the primary inductor. Multi-phase inverters can be used to drive more inductors for phased arrays.

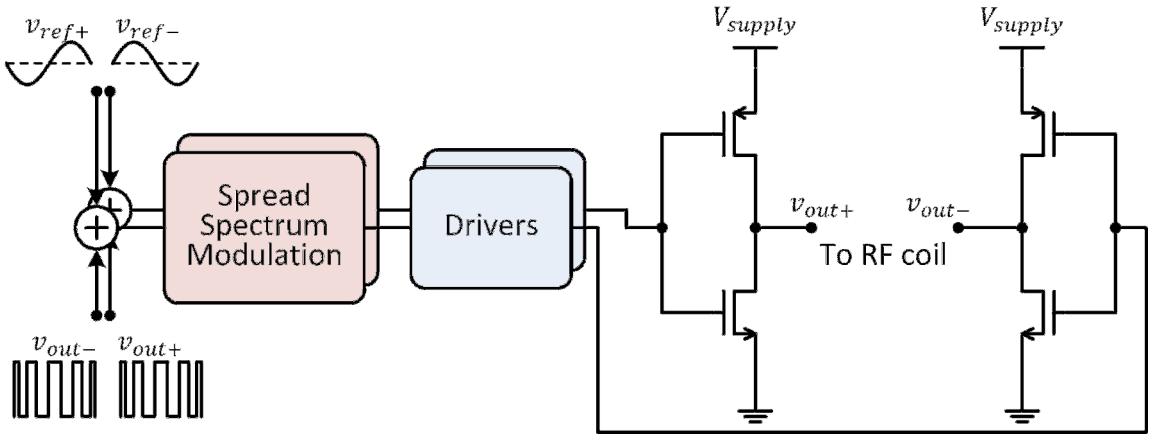


Figure 8.2: Proposed fully integrated class D wireless power transmitter, digital control, and feedback.

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APPENDIX

ANALYSIS OF RF RECTIFIER

A.1 Low-Input Power One-Stage RF Rectifier Analysis

Assuming the input voltage is sinusoidal as in (3.6), the intermediate voltage v_d is given by:

$$v_d = V_{in} \cos(\omega_o t) + V_{DC}/2. \tag{A.1}$$

Writing the KCL equation at the intermediate node and substitution from (A.1):

$$i_{in} = i_{Dh} - i_{Dc} = I_S \, \mathrm{e}^{-V_{DC}/2V_T} \sinh\left(\frac{V_{in} \cos(\omega_o t)}{V_T}\right). \tag{A.2}$$

Using modified Bessel functions $\mathrm{I_m}(x)$ which are discussed in [32],

$$e^{\pm x \cos(\omega_o t)} = \mathrm{I_o}(\pm x) + 2\sum_{n=1}^{\infty} \mathrm{I_n}(\pm x) \cos(n\omega_o t), \tag{A.3}$$

Using the relationship in [32]:

$$\sinh(x \cos(\omega_o t)) = 2 \sum_{n=1,odd}^{\infty} \mathrm{I_n}(x) \cos(n\omega_o t). \tag{A.4}$$

The harmonic n of the input current i_{in} is given by:

$$i_{in}[n, odd] = 2I_S \, \mathrm{e}^{-V_{DC}/2V_T} \, \mathrm{I_n}\left(\frac{V_{in}}{V_T}\right). \tag{A.5}$$

The expression of the input resistance of the RF rectifier is given by:

$$R_{rect} = \frac{V_{in}\, \mathrm{e}^{V_{DC}/2V_T}}{2I_S\, \mathrm{I}_1\left(\frac{V_{in}}{V_T}\right)}. \tag{A.6}$$

The diode current is expressed by:

$$i_d = I_S\left(\mathrm{e}^{-V_{DC}/2V_T}\, \mathrm{e}^{-V_{in}/V_T\, \cos(\omega_o t)} - 1\right). \tag{A.7}$$

The dc component of the load current, which is the diode current [42], is given by:

$$I_{DC} = I_S\left(\mathrm{e}^{-V_{DC}/2V_T}\, \mathrm{I}_0\left(\frac{V_{in}}{V_T}\right) - 1\right). \tag{A.8}$$

A.2 High-Input Power One-Stage RF Rectifier Analysis

Assuming the input current is sinusoidal as in (3.11). Rewriting the KCL equation at the intermediate node with substitution from (3.11):

$$i_{in} = I_{in}\cos(\omega_o t) = I_S\, \mathrm{e}^{-V_{DC}/2V_T}\left\{\mathrm{e}^{((v_d - V_{DC}/2)/V_T)} - \mathrm{e}^{(-(v_d - V_{DC}/2)/V_T)}\right\}, \tag{A.9}$$

which results in:

$$\frac{I_{in}}{I_S}\, \mathrm{e}^{V_{DC}/2V_T}\cos(\omega_o t) = \sinh\left(\frac{(v_d - V_{DC}/2)}{V_T}\right), \tag{A.10}$$

and the intermediate voltage v_d is given by:

$$\frac{v_d}{V_T} = \frac{V_{DC}}{2V_T} + \sinh^{-1}\left(\frac{I_{in}}{I_S}\, \mathrm{e}^{V_{DC}/2V_T}\cos(\omega_o t)\right), \tag{A.11}$$

where from now on we define:

$$P = \frac{I_{in}}{I_S} \, \mathrm{e}^{V_{DC}/2V_T} \, . \tag{A.12}$$

The expression of the intermediate voltage v_d is given as:

$$v_d = v_d \left[0\right] + \sum_{n=0}^{\infty} v_d \left[n\right] \cos \left(n\omega_o t\right) . \tag{A.13}$$

The dc component is:

$$v_d \left[0\right] = \frac{V_{DC}}{2}, \tag{A.14}$$

and the fundamental and third harmonics are evaluated in Appendix (A.4). The expression of the input resistance, using (A.26) and (3.11), is:

$$R_{rect} = \frac{\frac{4\sqrt{1+P^2}}{\pi P} V_T \left\{ \mathrm{K} \left(\frac{P}{\sqrt{1+P^2}} \right) - \mathrm{E} \left(\frac{P}{\sqrt{1+P^2}} \right) \right\}}{I_{in}}, \tag{A.15}$$

The diode current after substitution from (3.5) is expressed by:

$$i_d = I_S \left(\exp \left(-v_d / V_T \right) - 1 \right) . \tag{A.16}$$

Using the relationship of the inverse hyperbolic function and the logarithmic function:

$$\exp \left(\sinh^{-1} \left(x \right) \right) = \exp \left(\ln \left(x + \sqrt{1 + x^2} \right) \right) = x + \sqrt{1 + x^2}, \tag{A.17}$$

the dc component of the load current, which is the diode current, is given by:

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_S \left(\mathrm{e}^{V_{DC}/2V_T} \left(P \cos \left(\theta \right) + \sqrt{1 + P^2 \cos^2 \left(\theta \right)} \right) - 1 \right) d\theta, \tag{A.18}$$

which gives the expression (3.14), where $\mathrm{E}(k)$ is the complete elliptic integral of the second kind given by:

$$\mathrm{E}(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2\theta} d\theta, \tag{A.19}$$

$$\int_0^{\pi/2} \sqrt{1 + P^2 \cos^2\theta} d\theta = \sqrt{1+P^2}\ \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}}\right), \tag{A.20}$$

where $\cos^2(\theta) = 1 - \sin^2(\theta)$ and the elliptic equation (A.19) are used.

A.3 Level-m Compensation Effect on the RF Rectifier Relationships

In order to understand the effect of the level-m compensation, the starting point is the equation of weak-inversion NMOS [31, 42], which is expressed as:

$$i_d = \mu_n C_{ox} \phi_t^2 \frac{W}{L} \exp\left(\frac{(V_{GS} - V_T)}{n\phi_t}\right) \left\{1 - \exp\left(-\frac{V_{DS}}{\phi_t}\right)\right\}, \tag{A.21}$$

with the constraint of $V_G = V_D + mV_{DC}$ where m is level of compensation. If the compensation gate signal is taken from the next/previous stage, m=1, and if it is taken from a distance of 2 stages after/before the current stage, m=2, ... Under these assumptions, the equation becomes:

$$i_d = \mu_n C_{ox} \phi_t^2 \exp\left(\frac{-V_T}{n\phi_t}\right) \exp\left(\frac{mV_{DC}}{n\phi_t}\right) \left(\frac{W}{L}\right) \left\{\exp\left(\frac{V_{DS}}{n\phi_t}\right) - \exp\left(\frac{(1-n)V_{DS}}{n\phi_t}\right)\right\} \tag{A.22}$$

Assuming $n = 1$ for simple calculations (not very good for deep submicron technologies [42]), this results in:

$$i_d = \mu_n C_{ox} \phi_t^2 \exp\left(\frac{-V_T}{\phi_t}\right) \left(\frac{W}{L}\right) \exp\left(\frac{mV_{DC}}{\phi_t}\right) \left\{\exp\left(\frac{v_d}{\phi_t}\right) - 1\right\}, \tag{A.23}$$

where $I_S = \mu_n C_{ox} \phi_t^2 \exp\left(\frac{-V_T}{\phi_t}\right)\left(\frac{W}{L}\right)\exp\left(\frac{mV_{DC}}{\phi_t}\right)$. It is not a constant but has a feedback factor from the output dc voltage V_{DC} and depends on the level of compensation m. Thus, all previous equations where I_S is encountered can be replaced by $I_S^{'} = I_S \exp\left(\frac{mV_{DC}}{\phi_t}\right)$.

A.4 Integral Solution

The function $f(\theta) = \sinh^{-1}(P\cos\theta)$ is an even function $f(\theta) = f(-\theta)$ and half-wave symmetric $f(\theta) = -f(\theta + T/2)$:

$$I[n, odd] = \frac{1}{\pi}\int_0^{2\pi} \sinh^{-1}(P\cos\theta)\cos(n\theta)\,d\theta = \frac{4}{\pi}\int_0^{\pi/2} \sinh^{-1}(P\cos\theta)\cos(n\theta)\,d\theta. \tag{A.24}$$

Doing integration by parts yields:

$$I[n, odd] = \frac{4P}{\pi n\sqrt{1+P^2}}\int_0^{\pi/2} \frac{\sin(n\theta)\sin(\theta)}{\sqrt{1-\frac{P^2}{1+P^2}\sin^2\theta}}d\theta. \tag{A.25}$$

For $n = 1$, the numerator of the integrand is $\sin^2(\theta)$ which yields the following (using [105]):

$$I[1] = \frac{4\sqrt{1+P^2}}{\pi P}\left\{\mathrm{K}\left(\frac{P}{\sqrt{1+P^2}}\right) - \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}}\right)\right\}, \tag{A.26}$$

where $\mathrm{F}(k)$ is the complete elliptic integral of the first kind and is given by:

$$\mathrm{K}(k) = \int_0^{\pi/2} \frac{1}{\sqrt{1-k^2\sin^2\theta}}d\theta, \tag{A.27}$$

For $n = 3$, the numerator of the integrand is $3\sin^2(\theta) - 4\sin^4(\theta)$ which yields the following (using [105] and substitution from (A.26)):

$$I[3] = \frac{4\left(1+P^2\right)^{3/2}}{3\pi P^3} \left\{ \left(\frac{8P^2}{1+P^2} - 2 \right) \mathrm{K}\left(\frac{P}{\sqrt{1+P^2}} \right) - \left(2 + \frac{7P^2}{1+P^2} \right) \mathrm{E}\left(\frac{P}{\sqrt{1+P^2}} \right) \right\}. \quad \text{(A.28)}$$