DESIGN TECHNIQUES FOR HIGH PERFORMANCE SERIAL LINK TRANSCEIVERS

A Dissertation

by

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ABSTRACT

Increasing data rates over electrical channels with significant frequency-dependent loss is difficult due to excessive inter-symbol interference (ISI). In order to achieve sufficient link margins at high rates, I/O system designers implement equalization in the transmitters and are motivated to consider more spectrally-efficient modulation formats relative to the common PAM-2 scheme, such as PAM-4 and duobinary.

The first work, reviews when to consider PAM-4 and duobinary formats, as the modulation scheme which yields the highest system margins at a given data rate is a function of the channel loss profile, and presents a 20Gb/s triple-mode transmitter capable of efficiently implementing these three modulation schemes and three-tap feed-forward equalization. A statistical link modeling tool, which models ISI, crosstalk, random noise, and timing jitter, is developed to compare the three common modulation formats operating on electrical backplane channel models. In order to improve duobinary modulation efficiency, a low-power quarter-rate duobinary precoder circuit is proposed which provides significant timing margin improvement relative to full-rate precoders.

Also as serial I/O data rates scale above 10 Gb/s, crosstalk between neighboring channels degrades system bit-error rate (BER) performance. The next work presents receive-side circuitry which merges the cancellation of both near-end and far-end crosstalk (NEXT/FEXT) and can automatically adapt to different channel environments and variations in process, voltage, and temperature.

NEXT cancellation is realized with a novel 3-tap FIR filter which combines two traditional FIR filter taps and a continuous-time band-pass filter IIR tap for efficient crosstalk cancellation, with all filter tap coefficients automatically determined via an on-die sign-sign least-mean-square (SS-LMS) adaptation engine. FEXT cancellation is realized by coupling the aggressor signal through a differentiator circuit whose gain is automatically adjusted with a power-detection-based adaptation loop.

In conclusion, the proposed architectures in the transmitter side and receiver side together are to be good solution in the high speed I/O serial links to improve the performance by overcome the physical channel loss and adjacent channel noise as the system becomes complicated.

DEDICATION

To my parents, brother, sister and parents-in-law, and
to my dearest wife, Jina, and adorable daughter and son,
Boyoung and Seungchan

I dedicate my dissertation work to my family and many friends. Especially, I am grateful to my lovely wife and two children, Jina, Boyoung, and Seungchan for their love, encouragement, patience and sacrifice during the challenges of graduate school and life. I am truly thankful for having you in my life. This work is also dedicated to my loving parents, Eui-Sik and Sae-geun, who have always loved me unconditionally. I would not have successively finished this long journey without them.

ACKNOWLEDGMENTS

I would like to express my gratitude to my advisor, Dr. Samuel Palermo, whose expertise, understanding, and patience, added considerably to my graduate experience. I appreciate his vast knowledge and skills in analog and mixed circuit and system design in serial link I/O, and his assistance in writing papers. I also want to thank my PhD committee members, Dr. Kish, Dr. Peter, and Dr. Duncan M Walker, for agreeing to serve on my committee and for taking time out from their busy schedule.

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I would also like to thank my family for the support they provided me through my entire life and in particular, my wife, Jina, Kids Boyoung and Seungchan for giving me strength to work and live. I owe them especial thank for their patience and love to keep me staying on this journey. I would like to dedicate this thesis to them.

NOMENCLATURE

CMOS	Complementary Metal Oxide Semiconductor
I/O	Input and Output
ISI	Inter-Symbol Interference
MUX	Multiplexing
DMUX	De-Multiplexing
CML	Current Mode Logic
DJ	Deterministic Jitter
RJ	Random Jitter
PAM	Pulse-amplitude modulation
CTLE	Continuous Time Linear Equalization
UI	Unit Interval
BER	Bit Error Rate
FFE	Feed-forward equalization
TX	Transmitter
RX	Receiver
PRBS	Pseudo-Random Binary Sequency
FIR	Finite Impulse Response
PCB	Printed Circuit Board
DAC	Digital-to-Analog Converter
NEXT	Near-end crosstalk

FEXT	Far-end crosstalk
FIR	Finite impulse response
IIR	Infinite impulse response
Serdes	Serilaizer/Deserializer
PJ	Periodic jitter
DDJ	Data dependent jitter
DCD	duty cycle jitter
ZFE	Zero forcing equalizer
LMS	Least mean square
DFE	Decision feedback equalization
MSLE	Maximum likelihood sequence estimator

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I. INTRODUCTION

I.1. Motivation

Inter-chip communication at high data rates over standard electrical channels is challenging due to excessive frequency-dependent channel attenuation which causes large amounts of inter-symbol interference (ISI). Transmitters with feed-forward equalization (FFE) are often employed in order to operate reliably over such channels at high data rates [1], [2]. However, due to transmit peak-power limitations imposed by shrinking CMOS power supplies, only incremental performance improvement is achieved by increasing transmitter equalization complexity past two or three taps [3]. This motivates I/O system designers to consider modulation techniques which provide spectral efficiencies higher than simple binary PAM2 signaling in order to increase data rates over band-limited channels, with the most commonly proposed modulation schemes being PAM4 and duobinary. However, again due to transmit peak-power limitations, the optimal modulation which yields the best system margins is a function of the channel loss profile and the desired data rate. Examples of high-speed serial I/O transmitters which implement these different modulation formats include [2], [4], [5].

The work of [2], [4] implements a transmitter which is compatible with PAM2 and PAM4 modulation, but does not support duobinary due to the absence of the precoder necessary to avoid error propagation. Custom designed transmitters for each modulation scheme are compared in [5], which implements the duobinary transmitter with a full-rate precoder. A transmitter which could efficiently support all three of these modulation formats would provide a high degree of flexibility to support different channel

environments and, for a given platform, the ability to scale to high data rate during periods of peak I/O bandwidth demand.

In addition, at data rates at or above 10 Gb/s, both intersymbol interference (ISI) due to channel frequency-dependent loss and crosstalk interference due to multi-channel coupling must be considered in order to ensure adequate system bit-error rate (BER). While equalizers are effective in cancelling ISI, topologies such as receive-side FIR filters and continuous-time linear equalizers (CTLE) don't improve the signal-to-crosstalk ratio, motivating the use of dedicated circuitry to cancel both near-end crosstalk (NEXT) and far-end crosstalk (FEXT).

An effective approach to cancel NEXT involves passing the known aggressor transmit data through an FIR filter to sum with the incoming signal at the victim receiver. One key limitation of this approach is that the NEXT signal is only canceled out to the span of the FIR filter, leading to relatively long 5-7 tap implementations [1], [2]. At the receiver side, efficient cancellation of FEXT is possible by passing the aggressor signal through a high-pass filter which acts as a differentiator to emulate the FEXT signal [3]-[5]. With these crosstalk cancellation schemes, in order to seamlessly support operation with different channels and allow for robustness to variations in process, voltage, and temperature, adaptive tuning of all the filter coefficients is required.

The main purpose of this dissertation was to understand both the achievements and limitations of previous works and to develop new design techniques for overcoming channel loss from transmitter side, and ISI from the receiver side.

I.2 Dissertation Organization

This dissertation starts with the overview of serial link transceiver architectures in order to understand how the serial I/O transceivers can be implemented both systemically and in circuitry to overcome the physical channel loss and noise sources in Section II.

Section III discusses the modulation techniques to overcome the physical channel loss in the transmitter side. The proposed transmitter, which to the authors' knowledge, is the first to implement a triple mode (NRZ,PAM-4, and Duobinary)-supported architecture in one transmitter and it is detailed in this section.

Also, it discusses the use of precoder design, which has been shown in previous work [5] as an efficient technique to generate Duobinary data format. In addition, this section presents how the triple mode is implemented in an architecture using mode selection. Statistical analysis is included in order to understand and analyze each modes according to various physical channels. The transmitter experimental results from GP 90nm process are presented and summary is included.

Section IV presents a receive-side near-end and far-end crosstalk cancellation circuitry, which reduces both crosstalks, allowing for a significant reduction in clock distribution circuitry complexity and power. The proposed next architecture utilizes low frequency clock to save power and circuit complexity, which are presented comparing with the previous work. In addition, the newly proposed fext architecture shows the RC components are adaptively found in the feedback loop comparing to the previous works. Also, experimental results from GP 65 nm CMOS prototype are presented.

Finally, Section V summarizes the contributions of this dissertation and proposes suggestions for future works.

II. BACKGROUND [1]

II.1. Transceiver Design Consideration

Increasing data rates over electrical channels with significant frequency dependent loss is difficult due to excessive inter-symbol interference (ISI) in the transceiver architecture like Fig. 2.1. In order to achieve sufficient link margins at high rates, I/O system designers implement equalization in the transmitters and are motivated to consider more spectrally-efficient modulation formats relative to the common PAM2 scheme, such as PAM4 and duobinary. Inter-chip communication at high data rates over standard electrical channels is challenging due to excessive frequency-dependent channel attenuation which causes large amounts of inter-symbol interference (ISI).

Transmitters with feed-forward equalization (FFE) are often employed in order to operate reliably over such channels at high data rates [1], [2]. However, due to transmit peak-power limitations imposed by shrinking CMOS power supplies, only incremental performance improvement is achieved by increasing transmitter equalization complexity past two or three taps [3]. This motivates I/O system designers to consider modulation techniques which provide spectral efficiencies higher than simple binary PAM2 signaling in order to increase data rates over band-limited channels, with the most commonly proposed modulation schemes being PAM4 and duobinary. However, again due to transmit peak-power limitations, the optimal modulation which yields the best system margins is a function of the channel loss profile and the desired data rate.

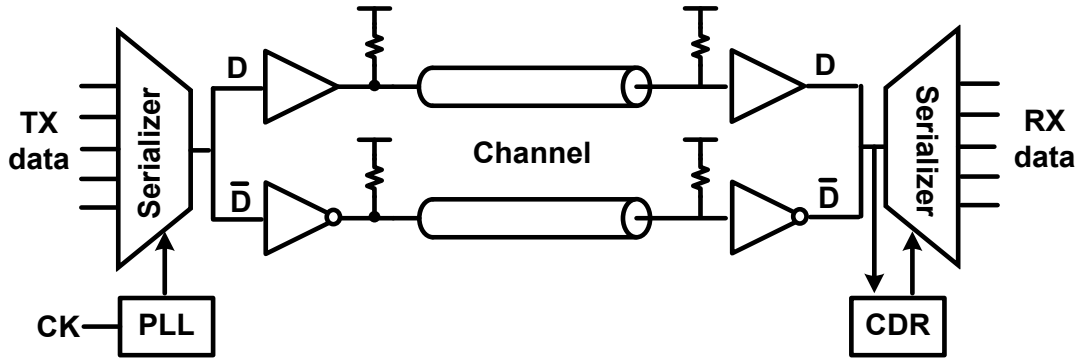


Fig. 2.1. Block diagram of the Serdes transceiver.

Also at data rates at or above 10 Gb/s, crosstalk interference due to multi-channel coupling must be considered in order to ensure adequate system bit-error rate (BER). While equalizers are effective in cancelling ISI, topologies such as receive-side FIR filters and continuous-time linear equalizers (CTLE) don't improve the signal-to-crosstalk ratio, motivating the use of dedicated circuitry to cancel both near-end crosstalk (NEXT) and far-end crosstalk (FEXT). An effective approach to cancel NEXT involves passing the known aggressor transmit data through an FIR filter to sum with the incoming signal at the victim receiver. One key limitation of this approach is that the NEXT signal is only canceled out to the span of the FIR filter, leading to relatively long 5-7 tap implementations [6], [7]. At the receiver side, efficient cancellation of FEXT is possible by passing the aggressor signal through a high-pass filter which acts as a differentiator to emulate the FEXT signal [8]-[10]. With these crosstalk cancellation schemes, in order to seamlessly support operation with different channels and allow for

robustness to variations in process, voltage, and temperature, adaptive tuning of all the filter coefficients is required.

II.1.1. Channel

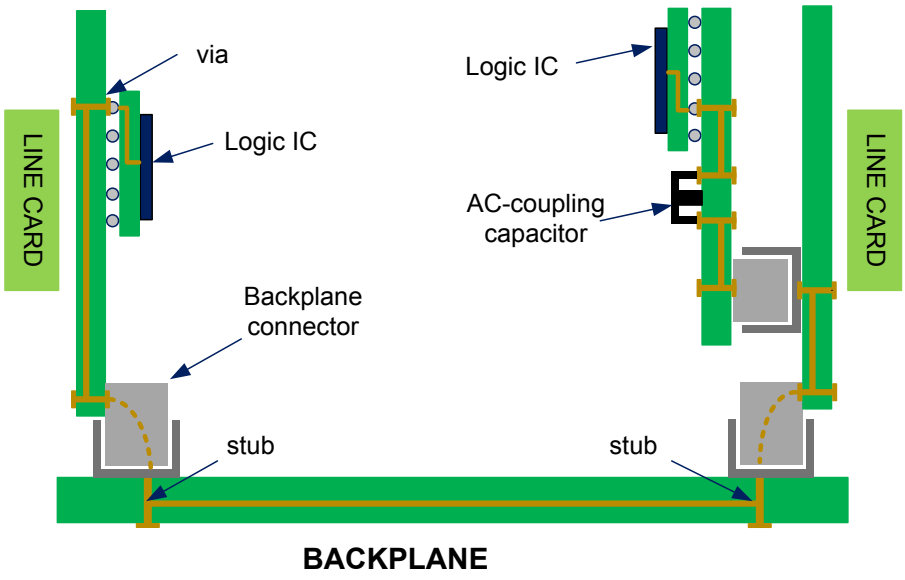
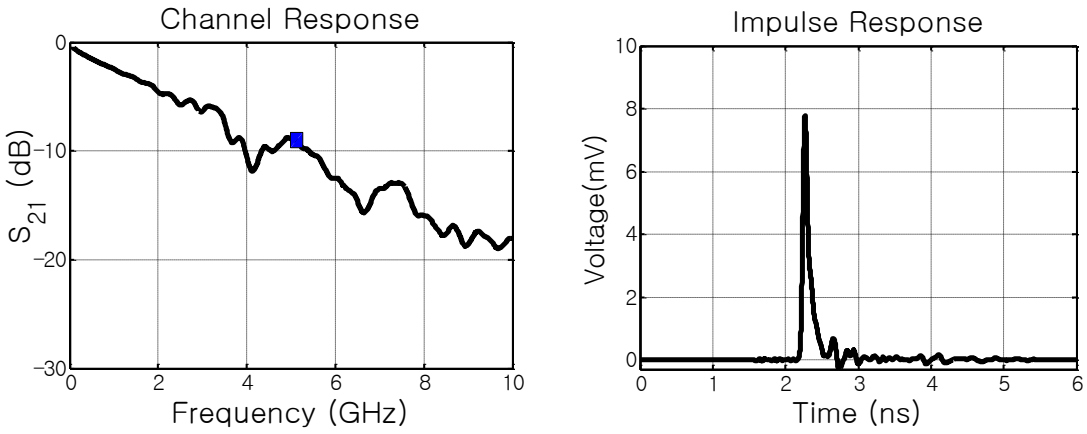


Fig. 2.2. Backplane channel.

A traditional backplane implementation is shown in Fig. 2.2. For backplane channel, the issues of impedance, losses, via stubs, lumped parasitics have decreased system performance. As data rates have risen, the aforementioned defects are to be deleterious significantly, and I/O circuit design complexity increases. The device-to-package solder bump and package-to-board (line card) solder ball interfaces are high impedance signal path that cannot be controlled easily. Also backplane connector and stub can cause the impedance discontinuity.



(a) (b)

Fig. 2.3. (a) Channel response, (b) Impulse response

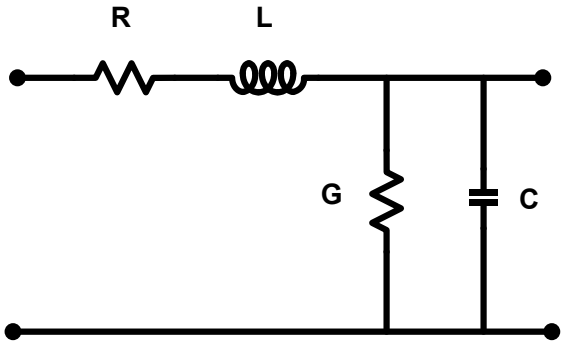


Fig. 2.4. RLGC network

As shown in Fig. 2.3 (a), the channel frequency response has low-pass filter characteristic as the attenuation increases with distance, and it generates nulls in frequency response due to impedance discontinuity by via-stub or impedance mismatching. In addition, the impulse response will disperse in a general low-pass nature in Fig. 2.3. This causes inter-symbol interference (ISI) which creates the pre-

cursors and post-cursors. As pre-cursors interfere with previously sent bits, while post-cursors interfere with the following bits, ISI from multiple bits reduces timing and voltage margin in receiver.

II.1.2. Channel Loss

Skin effect is the tendency of an alternating electric current (AC) to become distributed within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductor. The electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. The skin effect causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller, thus reducing the effective cross-section of the conductor [10], [11], [12].

The cause of the skin effect is electromagnetic induction. A magnetic field is accompanied by an induced electric field, which in turn creates secondary currents and a secondary magnetic field. Consequently, both the total magnetic field and induced currents inside conductors are reduced when compared with the dc case. The skin effect and the dielectric loss can be analyzed with all the RLGC parameters in Fig. 2.4.

II.1.2.1 Propagation Constant

Lossy copper transmission line is given by:

$$H(j\omega) = e^{-\gamma l} \tag{2-1}$$

where l is the length of the cable, and H(jw) is defined as the ratio between the output and input voltages of the cable (V_{out} and V_{in} respectively):

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} \tag{2-2}$$

The complex propagation constant γ is defined in [10], [11], [12].

$$\gamma = \sqrt{(R + j\omega l)(G + j\omega C)} = \alpha + j\,\beta \tag{2-3}$$

where R is the distributed series resistance (Ω/m), L is the distributed inductance (H/m), G the distributed parallel conductance (S/m), C the distributed capacitance (F/m), α the attenuation constant, and β the phase constant.

Losses in transmission lines are categorized into at least four elements such as metal loss, dielectric loss, conductivity loss, and loss due to radiation [11], [12].

$$\alpha = \alpha_c + \alpha_D + \alpha_G + \alpha_R \tag{2-4}$$

where α_c is metal loss, α_D dielectric loss, α_G conductivity loss, and α_R loss due to radiation.

II.1.2.1.1 Loss due to Metal Conductivity

The metal loss is the most dominant one in the transmission lines. This element is proportional to$\sqrt{f}$. So the frequency goes higher, it will dominate overall loss. The sheet resistance is calculated as:

$$R_{SHEET} = \left(\frac{\pi f \mu_0 \mu_R}{\sigma}\right)^{1/2} \quad (2\text{-}5)$$

where Sigma (σ) is the metal's conductivity, μ0 permittivity in the air, and μR permittivity in the resistance.

$$\alpha_c = \frac{R'}{2Z_0} \quad (2\text{-}6)$$

R' is converted from R_{SHEET}, and Z_0 is the characteristic impedance of the conductor.

$$R' = 0.8 * \frac{R_{SHEET}}{W} + 0.2 * \frac{R_{SHEET}}{W} = \frac{R_{SHEET}}{W} \quad (2\text{-}7)$$

where W is the width of the conductor. The first term is from the top of the strip, and the second one is from the bottom of the strip [11], [12].

II.1.2.1.2 Loss due to Dielectric Loss Tangent

The loss due to dielectric loss tangent is one of important losses at high speed data rate. It is shown in a printed circuit board (PCB) design option as dissipation factor, "DF" as an abbreviation. This term is proportional to frequency; therefore it can be dominant factor in the total loss [11], [12].

$$\alpha_D = \tan(\delta)\frac{\omega C' Z_0}{2} \quad \left(\frac{Nepers}{meter}\right) \quad (2\text{-}8)$$

where C' is Farads/meter. In this equation, tan(δ) is expressed like the below.

$$\text{Permittivity} : \varepsilon = \varepsilon' - j\varepsilon'' \tag{2-9}$$

$$\text{Loss tangent} : \tan(\delta) = {}^{\varepsilon'}/_{\varepsilon''} \tag{2-10}$$

II.1.2.1.3 Loss due to conductivity of dielectric

$$\alpha_G = \frac{G' \cdot Z_0}{2} \quad (\frac{Nepers}{meter}) \tag{2-11}$$

where G' is siemens/meter.

The loss due to substrate conductivity term is often ignored because it's very small due to low conductivity [11], [12]. However silicon has relatively poor electrical insulating properties, so it should be considered in the total loss.

II.1.2.1.4 Loss due to Radiation

This is another attenuation mechanism that has a very small effect. It's more or less a leakage loss. It's hard to explain in the transmission line model, therefore 3D electromagnetic simulator is needed [12].

II.1.3. Crosstalks

Crosstalk is the unwanted coupling of energy between two or more adjacent channels [10], [13]. It occurs when energy is coupled capacitively or inductively during data transition between them. Aggressor channel causes the crosstalk into the adjacent channel called the victim channel. As it is shown in the Fig. 2.5, there are two kinds of crosstalks such as near-end and far-end ones.

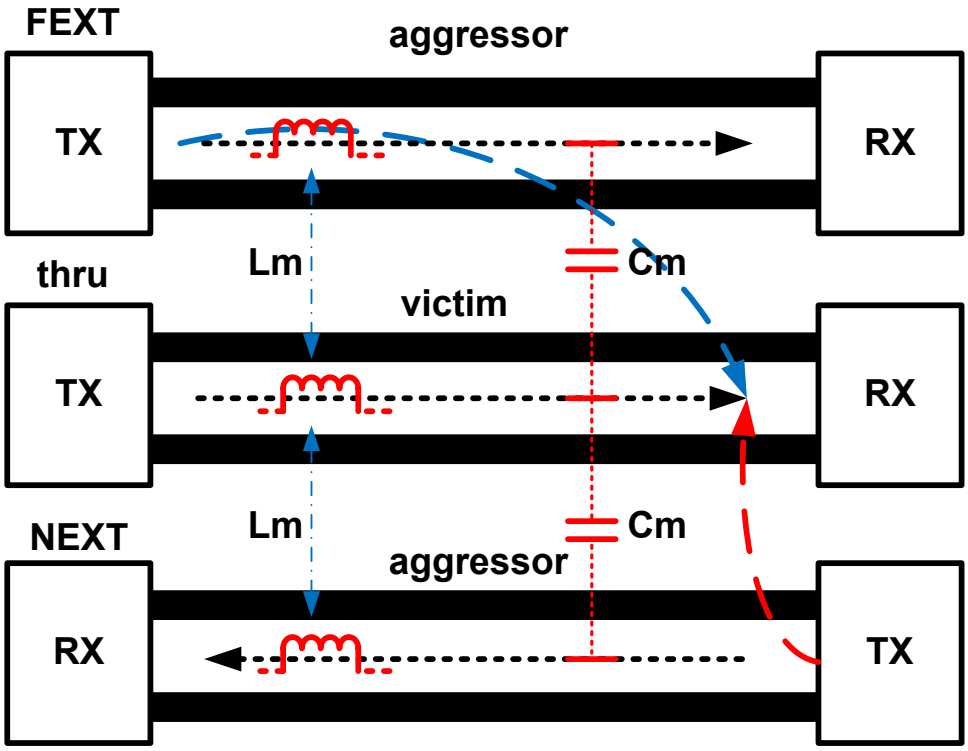
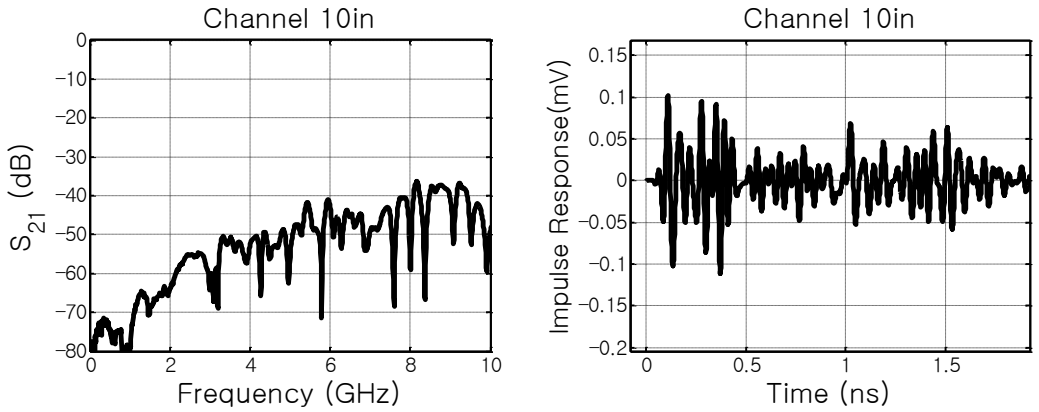


Fig. 2.5. Block diagram of crosstalk noise

II.1.3.1 Near-end Crosstalk

The energy coupled from the active signal line, the aggressor, onto a quiet passive victim line is transferred to the end of the victim line. This is known as near-end crosstalk in Fig. 2.6, which shows next channel response and next impulse response respectively. The frequency response has high-pass filter characteristic as it is shown in Fig. 2.6 (a).



(a) (b)

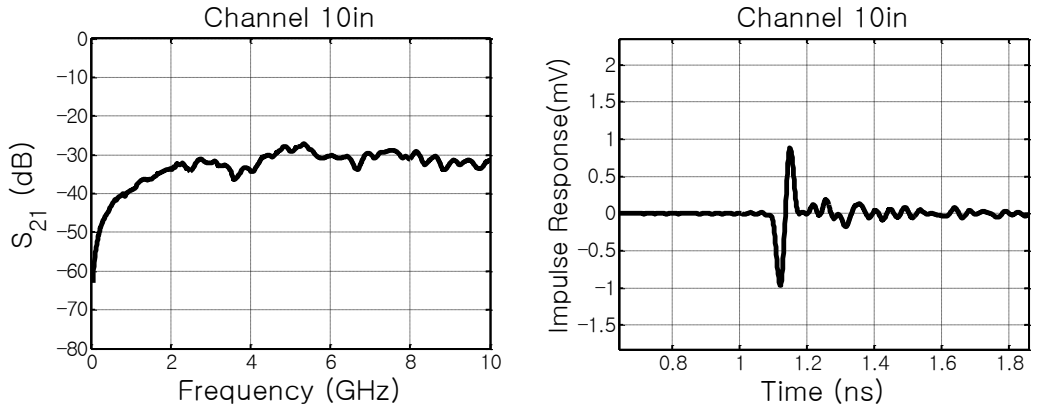
Fig. 2.6. (a) Next channel, (b) Next impulse response

The magnitude of it is dependent on the mutual capacitance (Cm) and inductance (Lm) between the adjacent lines.

$$Next = \frac{1}{4}\left(\frac{C_m}{C} + \frac{L_m}{L}\right) \tag{2-12}$$

where Cm is the mutual capacitance between lines per unit length, Lm is the mutual inductance between lines per unit length, C is the capacitance per unit length, and L is the inductor per unit length of line.

II.1.3.2 Far-end Crosstalk



(a) (b)

Fig. 2.7. (a) Fext channel, (b) Fext impulse response

The coupled energy from the aggressor onto the victim line is travelling forward to the end of the victim line. It is called far-end crosstalk. Its magnitude is dependent on the Cm and –Lm between the adjacent lines.

$$Fext = \frac{1}{4}\left(\frac{C_m}{C} + \frac{-L_m}{L}\right) \tag{2-13}$$

where Cm is the mutual capacitance between lines per unit length, Lm is the mutual inductance between lines per unit length, C is the capacitance per unit length, and L is the inductor per unit length of line. Fig. 2.7 shows fext channel response and fext impulse response respectively, which shows fext channel response and fext impulse response respectively. The frequency response has band-pass filter characteristic as it is shown in Fig. 2.7 (a).

II.1.4. Jitter

Jitter is the deviation from true periodicity of a presumed periodic signal, often in relation to a reference clock source [10], [13], [14]. Jitter falls into two broad categories: random jitter and deterministic jitter which consists of data dependent jitter and periodic jitter. It can be described as a variation in the period of the signal. If we have a sine wave clock, it can be written like the below.

$$Clock = \sin(w * t) \tag{2-14}$$

which is a perfect clock without jitter.

Then jittery clock can be described like the below.

$$Clcok = \sin(w * t + j(t)) \tag{2-15}$$

where j(t) is a function of the jitter.

II.1.4.1 Random Jitter (RJ)

This jitter is timing noise that cannot be predicted, because it's not caused by specific patterns. This is random process, so it is assumed to have a Gaussian distribution for the modeling. This results from differential and common mode stochastic noise processes such as power supply noise and thermal noise [15].

II.1.4.2 Deterministic Jitter (DJ)

This jitter is also timing jitter that is repeatable and predictable. It is attributable to specific patterns or events. It's from sources such as rise/fall times, ISI, power supply feed through, oscillator wand, and cross-talk from other signals [13], [14], [15].

This consists of periodic jitter (PJ), data dependent jitter (DDJ), and duty cycle Jitter (DCD).

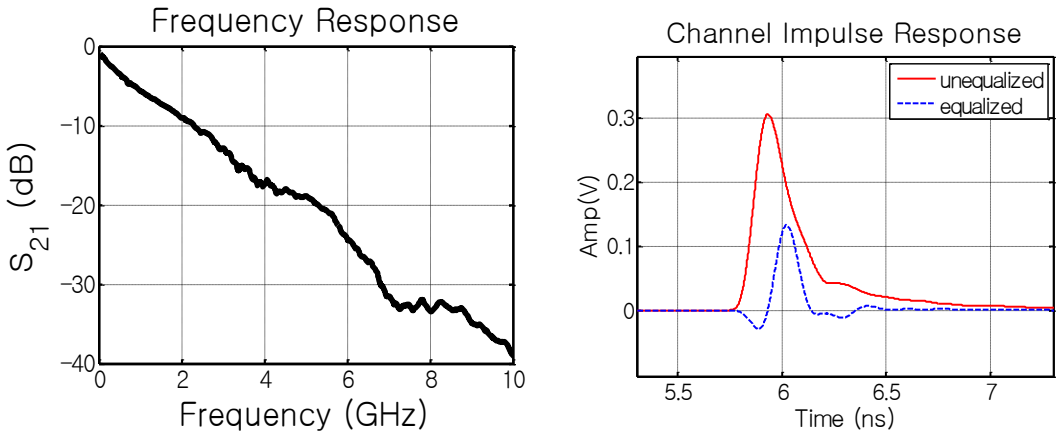
PJ repeats in a cycle fashion. Since any periodic waveform can be decomposed into a Fourier series of harmonic sinusoids, so it is called sinusoidal jitter. It's typically caused by external deterministic noise sources coupling into a system, such as switching power supply noise or a strong local RF carrier. It may also be caused by an unstable clock-recovery PLL [14].

DDJ is correlated with the bit sequence in a data stream. And it is often caused by the frequency response of a channel. It's also known as ISI [15].

DCD is predicted based on whether the associated edge is rising or falling. These are two common causes of DCD [14]. The one is the slew rate for the rising edges are different from the falling edges. The other is the decision threshold for a waveform is higher or lower than it should be.

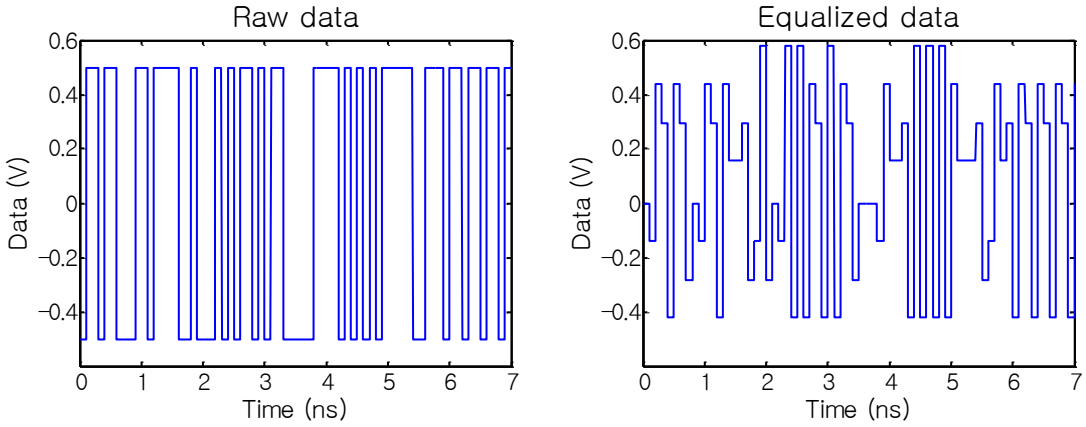
II.2. Transmitter Design Consideration

II.2.1.Transmitter Equalization Techniques



(a) (b)

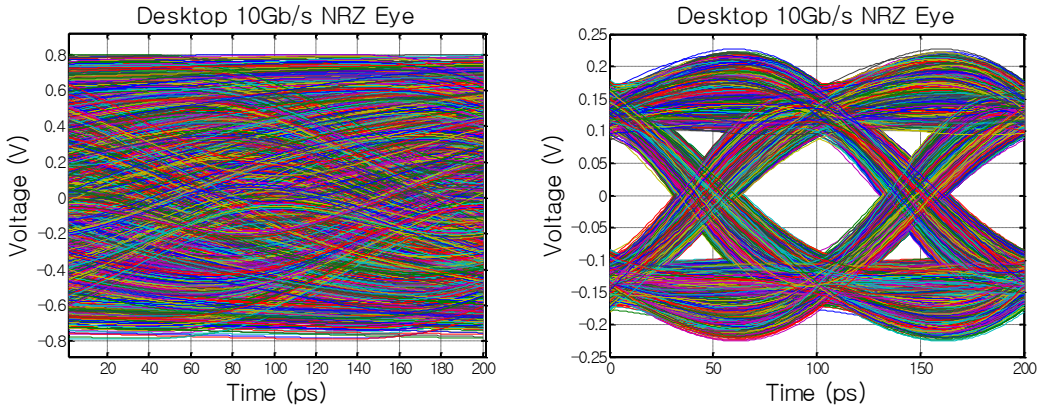
Fig. 2.8. (a) Channel response, (b) Unequalized and equalized impulse response



(a) (b)

Fig. 2.9. (a) Raw data, (b) 3-tap Equalized data

A high-speed signal travelling through an electrical channel is subject to high-frequency losses such as skin effect and dielectric losses as mentioned before. Fig. 2.8 shows a channel response in frequency domain and pulse responses with and without equalization techniques in time domain. The equalized data is made up with 3 taps as shown in Fig. 2.9. The channel losses can severely degrade and attenuate the high-frequency content of the signal, making it difficult for the receiver to detect the signal without error. Therefore transmitter equalizer technique improves the high-speed signal quality. Fig. 2.10 (a) shows that data through lossy channel become dispersive, and eye-diagram is totally closed. But equalized data overcome the ISI effects, and make the eye wide open in Fig. 2.10 (b).



(a) (b)

Fig. 2.10. (a) Unequalized eye-diagram, (b) Equalized eye-diagram

II.2.1.1. Linear Transmitter Equalizer

An ideal signal for a receiver without ISI completes the transition within a symbol interval. However, when the signal travels through a lossy channel, the transition expands to adjacent intervals. This effect is called as inter-symbol interference (ISI). The purpose of pre-cursor and post-cursor emphasis is to apply delays and inversions to the signal and add them back to the original signal with the proper weight.

In case of three tap equalizer implementation [16], the feed-forward equalization is implemented by spreading the symbol's energy over three bit periods, one pre-cursor, one main-cursor, and one post-cursor tap, with the tap weights. Two main techniques for formulating the filter coefficients are Zero forcing equalizer (ZFE) and Least mean square (LMS) equalizer.

II.2.1.1.1. Zero Force Equalizer (ZFE)

It is computationally efficient method of forming an inverse filter. A training signal is transmitted over the channel in order to formulate a set of FIR inverse filter coefficients. A set of coefficients can be determined by solving a set of equations based on the received sample values, and force all but the center tap of the filtered response to 0.

$$C_i = \sum_{n=-K}^{K} e_n u_{i-n} \tag{2-13}$$

$$C_k = \begin{cases} 1, & k = 0 \\ 0, & k \neq 0 \end{cases} \tag{2-14}$$

$$\begin{bmatrix} u(-k) & 0 & 0 \\ u(-k+1) & u(-k) & 0 \\ 0 & \cdots & 0 \\ 0 & 0 & \cdots \end{bmatrix} \begin{bmatrix} u(k) \\ \vdots \\ \vdots \\ e_k \end{bmatrix} = \begin{bmatrix} e_{-k} \\ \vdots \\ \vdots \\ C_{2k} \end{bmatrix} \tag{2-15}$$

This means the N-1 samples around the center tap does not contribute to ISI. The main advantage of this technique is that the solution to the set of equations is reduced to a simple matrix inversion. But the major drawback is that since ZFE is simply an inverse filter, it applies high gain to the high frequencies, which tends to amplify noise [16], [17].

II.2.1.1.2. Least Mean Square (LMS) Equalizer

The least mean squared equalizer is a more general approach to automatic system. Instead of solving a set of N equations as was done in the ZFE, the coefficients are gradually adjusted to minimize the error between the equalized signal and the reference. The LMS equalizer [18] is shown to have better noise performance than the ZFE.

Equalization coefficients for all data formats are acquired with a minimum-mean-square-error algorithm.

$$\begin{bmatrix} y(0) \\ y(1) \\ \cdots \\ y(l+k-2) \end{bmatrix} = \begin{bmatrix} p(0) & 0 & 0 & \cdots & 0 & 0 \\ p(1) & p(0) & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & p(k-1) & p(k-2) & \\ 0 & 0 & \cdots & 0 & p(k-1) & \end{bmatrix} \begin{bmatrix} h(0) \\ h(1) \\ \cdots \\ h(l-1) \end{bmatrix} \tag{2-16}$$

$$H_{ls} = (P^T P)^{-1} P^T Y_{des} \tag{2-17}$$

where here *y* is the desired pulse response with an *l*-tap equalizer, *h*, and *p* is the un-equalized pulse response with *k* samples.

II.2.1.2 Non-Linear Transmitter Equalizer

These techniques are used in applications where the channel distortion is too severe. We assume that the channel is linear time-invariant, then ISI can be described as a deterministic superposition of time-shifted dispersive pulses.

II.2.1.2.1. Decision Feedback Equalization (DFE)

DFE is based on the principle that once you have determined the value of the current transmitted symbol, ISI contribution of that symbol to future received symbols can be exactly removed by estimating and substracting out before detection of subsequent symbols. This postcursor ISI removal is accomplished by the use of filter. The details are descripted in the receiver side. DFE can only remove post-cursor ISI, or ISI introduced by future bits. In order to eliminate pre-cursor ISI, FFE must be utilized [19].

II.2.1.2.2. Maximum Likelihood Sequence Estimator (MLSE)

The optimal equalizer, in the sense that it with the highest probability correctly detects the transmitted sequence, is the maximum-likelihood sequence estimator (MLSE) in Fig. 2.11. MLSE tests all possible data sequences, and choose the data sequence with the maximum probability as the output. MLSE is used like in the below architecture to find out noise-free received data with a matched filter [20].

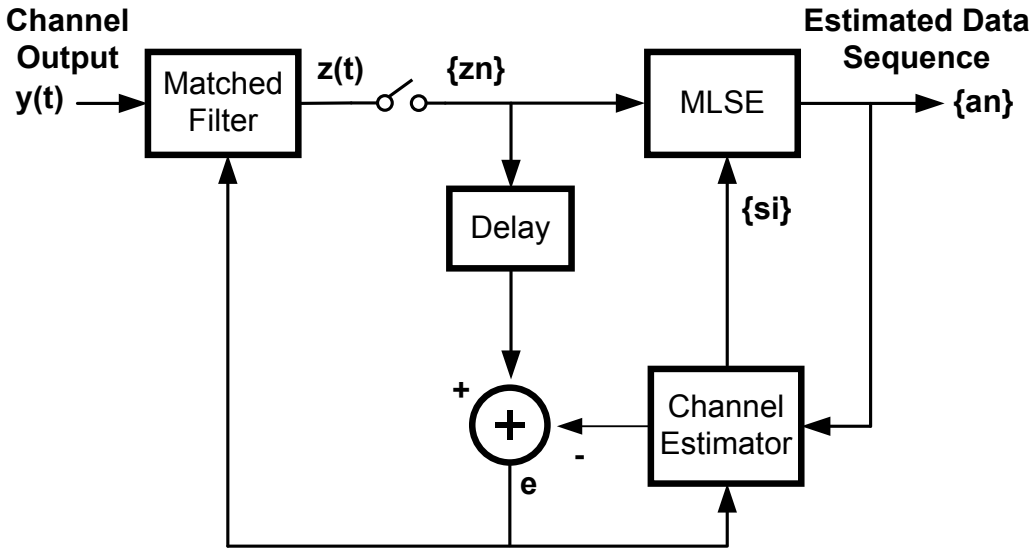


Fig. 2.11. The structure of a maximum likelihood sequence equalizer (MLSE) with an adaptive matched filter

II.2.2. Transmitter Modulation Technique

Increasing data rates over electrical channels with significant frequency dependent loss is difficult due to excessive inter-symbol interference (ISI). In order to achieve sufficient link margins at high rates, I/O system designers implement equalization in the transmitters and are motivated to consider more spectrally-efficient modulation formats relative to the common PAM2 scheme, such as PAM4 and duobinary in Fig. 2.12. Examples of high-speed serial I/O transmitters which implement these different modulation formats include [2], [4], [5]. The work of [2], [4] implements a transmitter which is compatible with PAM2 and PAM4 modulation, but does not support duobinary due to the absence of the precoder necessary to avoid error propagation. Custom designed transmitters for each modulation scheme are compared in [5], which

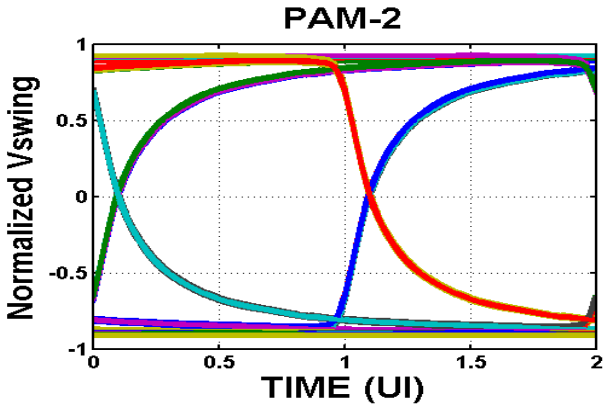
implements the duobinary transmitter with a full-rate precoder. A transmitter which could efficiently support all three of these modulation formats would provide a high degree of flexibility to support different channel environments and, for a given platform, the ability to scale to high data rate during periods of peak I/O bandwidth demand.

In order to consider when a certain modulation format will yield higher link margins, it is possible to compare the channel loss at an effective Nyquist frequency. As PAM4 sends two bits/symbol, the symbol period is twice as long as the PAM2 symbol or bit period, T_b. Thus, relative to the PAM2 Nyquist frequency of $1/(2T_b)$ and for the same data rate, the PAM4 Nyquist frequency is at one-half this value or $1/(4T_b)$.

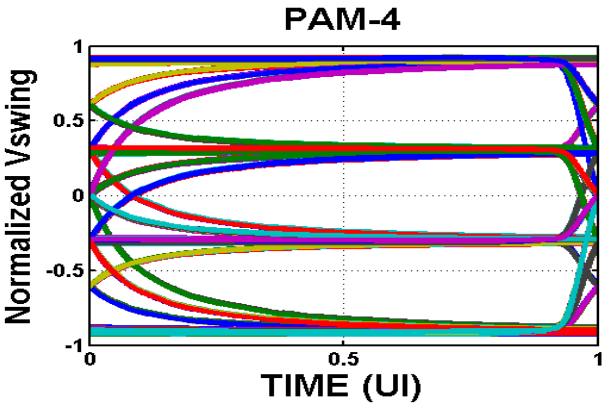
However, due to the transmitter's peak-power limit, the voltage margin between symbols is 3x (9.5dB) lower with PAM4 versus simple binary PAM2 signaling. The signal at the output of a linear channel can be represented as

$$y(t) = \sum_{k=-\infty}^{n} (b_k - b_{k-1}) S(t - kT) \tag{2-18}$$

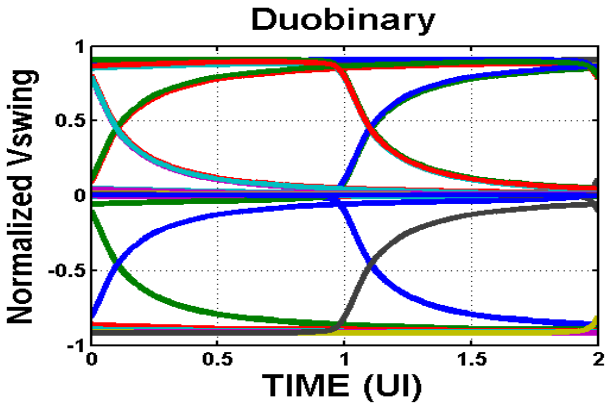
where T - symbol interval, bk , bk-1 are symbol values which are {-1,+1} for NRZ and {-1, - 1/3, 1/3, 1} for PAM4; S(t) is the channels' step response. Encoding more data into the same timeframe can be done using different signaling levels. Such multi-level signaling (MLS) or pulse amplitude modulation (PAM) can have multiple distinct levels. Actually, NRZ is a two-level MLS or PAM-2 system. PAM-4 has four distinct levels to encode two bits of data, essentially doubling the bandwidth of a connection. Generating or decoding more than two levels is typically more difficult, and often requires better or more complex hardware.



(a)



(b)



(c)

Fig. 2.12. Eye diagrams of the three common modulation formats (a) PAM-2, (b) PAM-4, (c) duobinary

Likewise, for high-speed signals, random and induced noise becomes a significant factor. In this scheme there are three slicers to detect each of the 4 logic levels: symbol 0 for 00 bit pattern; symbol 1 for a 01 bit pattern; symbol 2 for a 11 bit pattern and symbol 3 for a 10 bit pattern. This means more complex receiver circuitry and reduction of voltage margin/eye height in the eye diagram for a given bit rate. However less equalization is needed for a given bit rate, since the required speed is only half the bit rate. High-speed link designs have started using PAM4 instead of binary (PAM2) signaling in an attempt to make better use of the high signal-to noise ratio in the available bandwidth of the low-pass high-speed link channel.

Duobinary modulation in [5] allows for a controlled amount of ISI, such that the received signal at time *n* is

$$y_n = x_n + x_{n-1} \tag{2-19}$$

Ideally, this produces a three-level waveform at the receiver which has an effective Nyquist frequency of $1/(3T_b)$ at the cost of a 2x reduction in voltage margin (6dB) relative to PAM2 signaling. Thus, as shown in Table 1, if the PAM2 Nyquist frequency channel loss is greater than 6dB relative to the effective duobinary Nyquist frequency channel loss, β_1, then duobinary can potentially offer higher SNR. In comparing duobinary versus PAM4, if the channel loss profile is not overly steep, such that there is less than 3.54dB of loss at β_1 relative to the PAM4 Nyquist frequency loss, β_0, then duobinary should provide an advantage over PAM4. If the channel loss profile is steep and displays more than 9.54dB separation between β_2 and β_0, then PAM4 has the potential to offer the most margin in Fig. 2. 13. When the modulation is used jointly with

equalization, the total receiver signal magnitude depends on the highest channel attenuation in the Nyquist band. Since the modulation with higher Nyquist links channels are predominantly low-pass, this means that Nyquist frequency (for example PAM2 over PAM4, for same bit rate) will incur more loss. On the other hand, due to the peak-power constraint, the multi-level PAM has to fit all the signal levels within the same headroom thereby decreasing the distance between the signal levels and therefore the received eye opening.

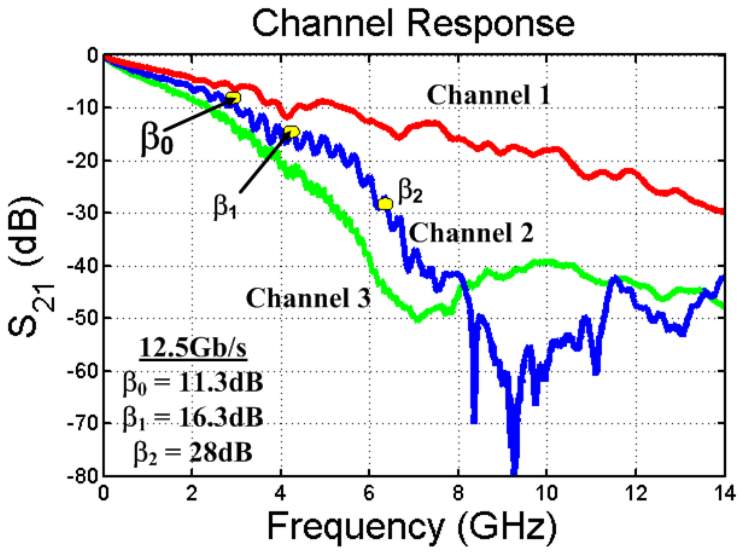


Fig. 2.13. Frequency response of three backplane channels.

II.3. Receiver Design Consideration

II.3.1. Continuous-Time Linear Equalizer

CTLE is another signal equalizer to overcome high-frequency losses through an electrical channel. It acts as a bandpass filter, which boosts the components inside a band

of frequencies and attenuates both the low and high frequency components outside. A continuous-time linear equalizer (CTLE) as shown in Fig. 2.14 is utilized after the crosstalk interferences are removed to reduce the inter-symbol interference (ISI) caused by channel loss and boost high-frequency components [21].

The transfer function of CTLE is

$$H(S) = \frac{A_p(s + w_z)}{(s + w_{p1})(s + w_{p2})} \tag{2-20}$$

where

$$A_p = {g_m}/{C_D}$$

$$w_z = {1}/{R_s C_s}$$

$$w_{p1} = (1 + g_m R_s/2)/R_s C_s$$

$$w_{p2} = {1}/{R_D C_D}$$

R_s and C_s are source degeneration resistor and capacitor, and R_D and C_D are loading resistor and capacitor respectively. g_m is the transconductance of the input transistor, and A_p is the DC gain of the CTLE stage in Fig. 2.15.

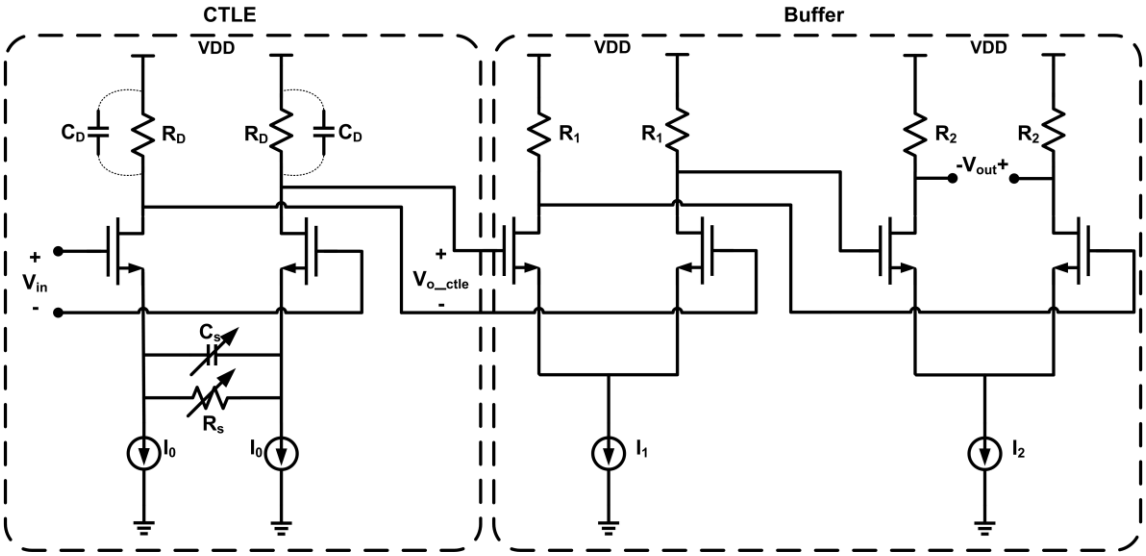


Fig. 2.14. CTLE & Buffer schematic

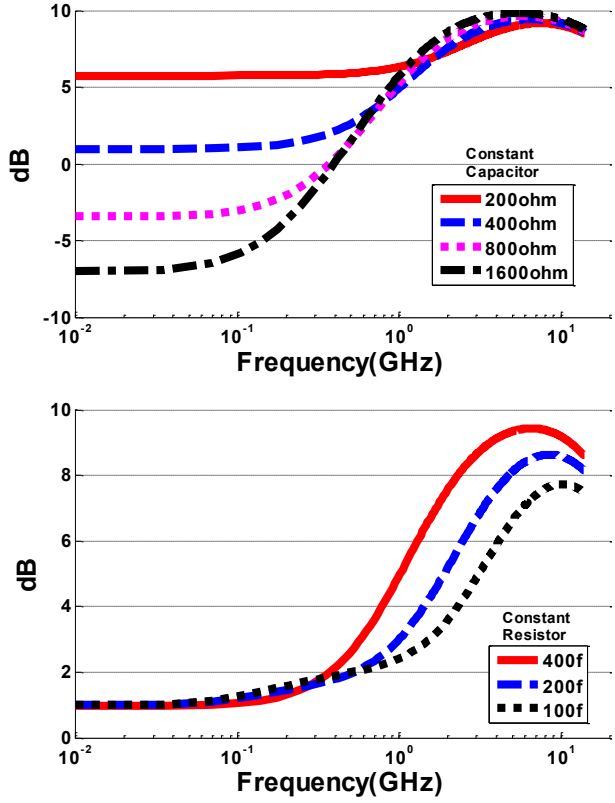


Fig. 2.15. CTLE simulation results

II.3.2. Non- Linear Equalizer (Decision Feedback Equalizer)

The nonlinear adaptive equalizer called decision feedback equalizer (DFE) in Fig. 2.16 is based on the principle that once it has determined the value of the present symbol, it can remove the ISI contribution of that symbol to future received symbols [19]. The nonlinear feature is due to the latch used in the decision period, which attempts to determine which signals of discrete levels were transmitted. Once the present symbol has been determined, the following structure can calculate the ISI effect that it would be added to the following data. This postcursor ISI removal is accomplished by the use of feedback structure like the figure.

II.3.2.1. Full-rate DFE

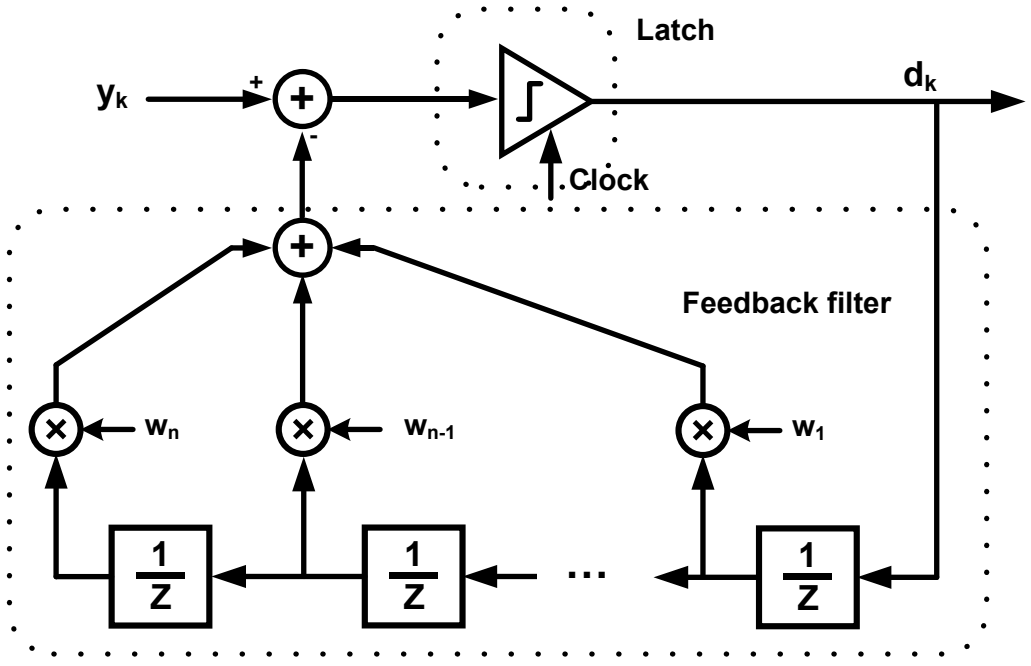


Fig 2.16. Full-rate Decision Feedback Equalizer

The requirements on the latch setup and hold times, and for the settling time of the feedback signals at the summer output in Fig. 2.16 is

$$\boldsymbol{t_{CK2Q} + t_{pd,w1-wn} + t_{summer} + t_{setup} < 1\ U.I.} \quad (2\text{-}21)$$

where t_{CK2Q} is the clock-to-Q delay of the flip-flop, $t_{pd,w1\text{-}wn}$ is the propagation delay through the tap (w1-wn), t_{sumner} is the summer propagation delay, and t_{setup} is the flip-flop setup time [22].

II.3.2.2. Half-rate DFE

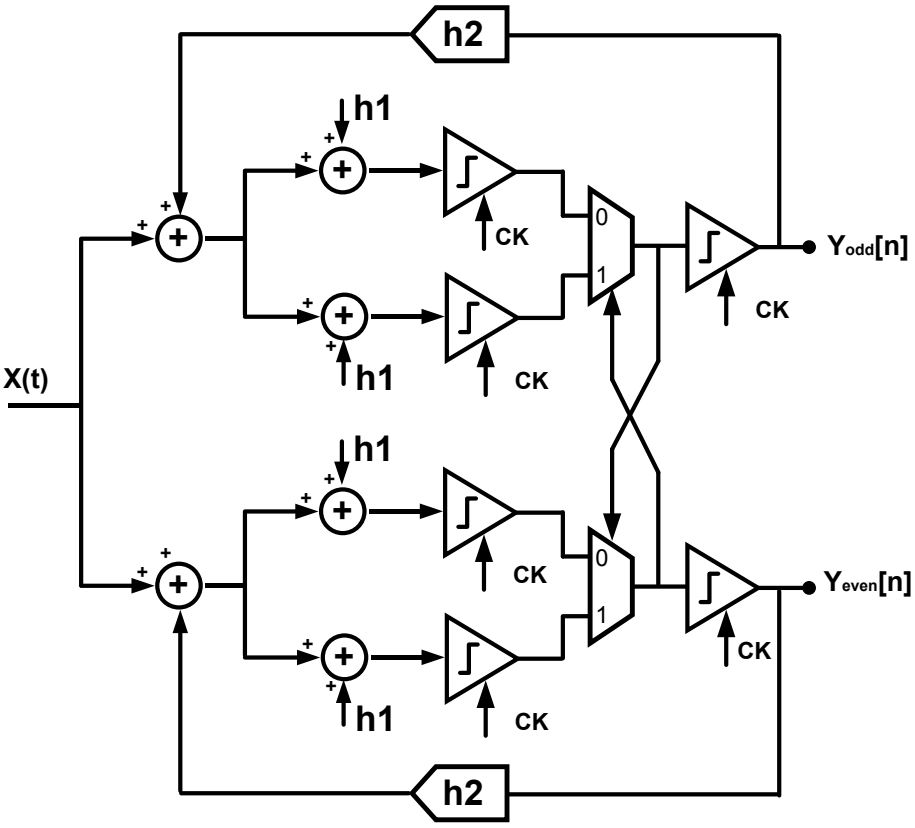


Fig 2.17. Half-rate Decision Feedback Equalizer

The requirements on the latch setup and hold times, and for the settling time of the feedback signals at the summer output in Fig. 2.17 is

$$\boldsymbol{t_{CK2Q} + t_{pd,h2} + t_{mux} + t_{summer} + t_{setup} < 1\ U.I.} \quad (2\text{-}22)$$

where t_{CK2Q} is the clock-to-Q delay of the flip-flop, $t_{pd,h2}$ is the propagation delay through the tap, t_{mux} is the mux propagation delay, t_{sumner} is the summer propagation delay, and t_{setup} is the flip-flop setup time [23], [24].

III. TRANSMITTER DESIGN [2]

III.1. Introduction

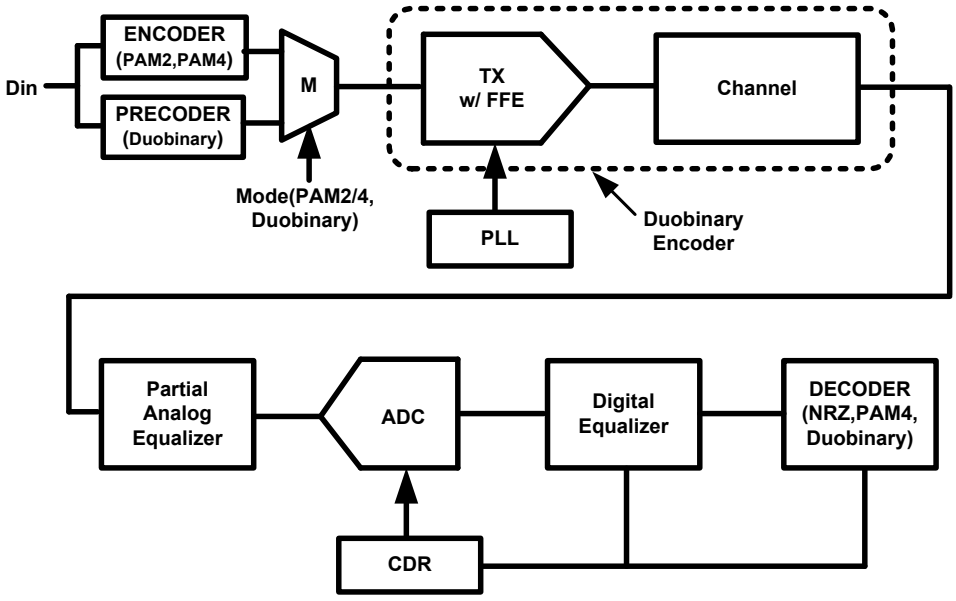


Fig. 3.1. High-Speed link block diagram with triple-mode transmitter and ADC-based receiver.

High-performance computing applications require I/O data rates to scale well past 10Gb/s to meet the demand of future systems. However, inter-chip communication at high data rates over standard electrical channels is challenging due to excessive frequency-dependent channel attenuation which causes large amounts of inter-symbol interference (ISI).

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2 . Reprinted with permission from "10 Gb/s Adaptive Receive-Side Near-End and Far-End Crosstalk Cancellation Circuitry" by Byungho Min, Noah Hae-Woong Yang, Samuel Palermo, 2014, IEEE International Midwest Symposium on Circuits and Systems, pp. 77-80, Copyright 2014 IEEE

In order to scale data rates, high-performance I/Os are evolving into sophisticated communication links, as shown in Fig. 3.1. Transmitters with feed-forward equalization (FFE) are often employed [1], [2]. However, due to transmit peak-power limitations imposed by shrinking CMOS power supplies, only incremental performance improvement is achieved by increasing transmitter equalization complexity past two or three taps [3]. This motivates I/O system designers to consider modulation techniques which provide spectral efficiencies higher than simple binary PAM-2 signaling in order to increase data rates over band-limited channels, with the most commonly proposed modulation schemes being PAM-4 and duobinary. At the receiver, analog equalization with continuous-time linear equalizers or FIR filters can also help mitigate ISI. The use of an ADC-based front-end allows for additional equalization in the digital domain and the support of multiple modulation formats. However, again due to transmit peak-power limitations, the optimal modulation which yields the best system margins is a function of the channel loss profile and the desired data rate.

For applications such as data centers, storage, and computer networking, high-speed links must typically achieve a bit-error rate (BER) from 10^{-12} to 10^{-15} for acceptable system performance. Under this low BER requirement, empirical analysis is impractical due to current hardware performance limitations. However, simple worst-case analysis techniques, such as peak-distortion analysis, yield highly pessimistic performance estimations which map to inefficient designs that consume excessive power and chip area [4]. This has lead to the development of statistical analysis methods [4], [5], [25],

[26], which utilize the statistical properties of noise and distortion to rapidly estimate link performance and trade-offs in equalization complexity and modulation format.

Examples of high-speed serial I/O transmitters which implement different modulation formats include [2], [28], [30]. The work of [2], [28] implements a transmitter which is compatible with PAM-2 and PAM-4 modulation, but does not support duobinary due to the absence of the precoder necessary to avoid error propagation. Custom designed transmitters for each modulation scheme are compared in [27], [29], [30], which implements the duobinary transmitter with a full-rate precoder. A transmitter which could efficiently support all three of these modulation formats would provide a high degree of flexibility to support different channel environments and, for a given platform, the ability to scale to high data rates during periods of peak I/O bandwidth demand.

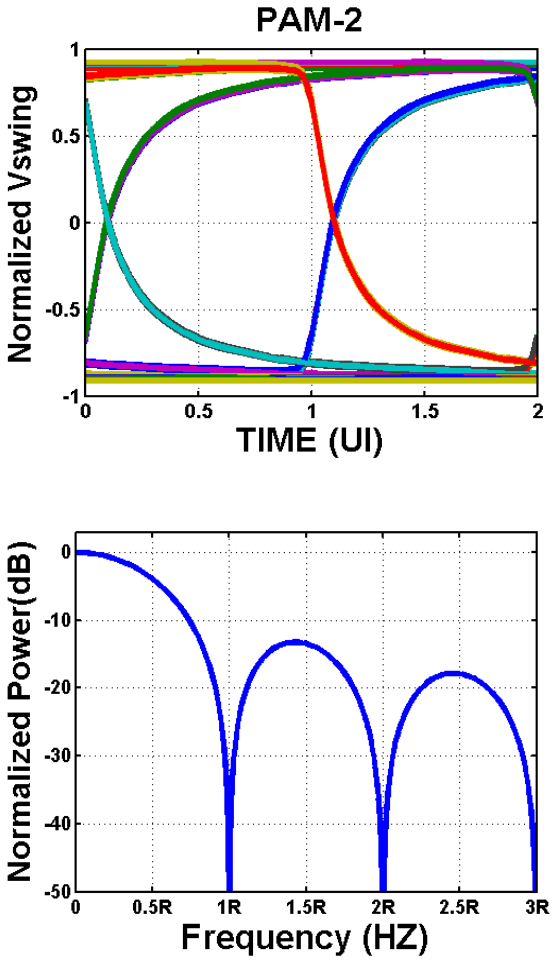
III.2. Modulation Techniques

III.2.1. Overview of PAM-2, PAM-4, and Duobinary Signaling

Fig. 3.2 compares random data eye diagrams and frequency spectrums for the three common modulation formats. PAM-2 or binary signaling is the simplest to implement at both the transmitter and receiver, and thus is the most commonly used modulation format. Here the binary bits are directly transmitted over the channel, requiring only a single comparator at the receiver to recover the data. The PAM-2 random data power-spectral density can be expressed as

$$S_{PAM2} = T_b sinc^2(T_b f), \tag{3-1}$$

where T_b is the bit period equal to the inverse of the data rate, R. Here, more than 95% of the cumulative signal power is contained in a bandwidth R [27].



(a)

Fig. 3.2. Eye diagrams and power-spectral density of the three common modulation formats of PAM-2

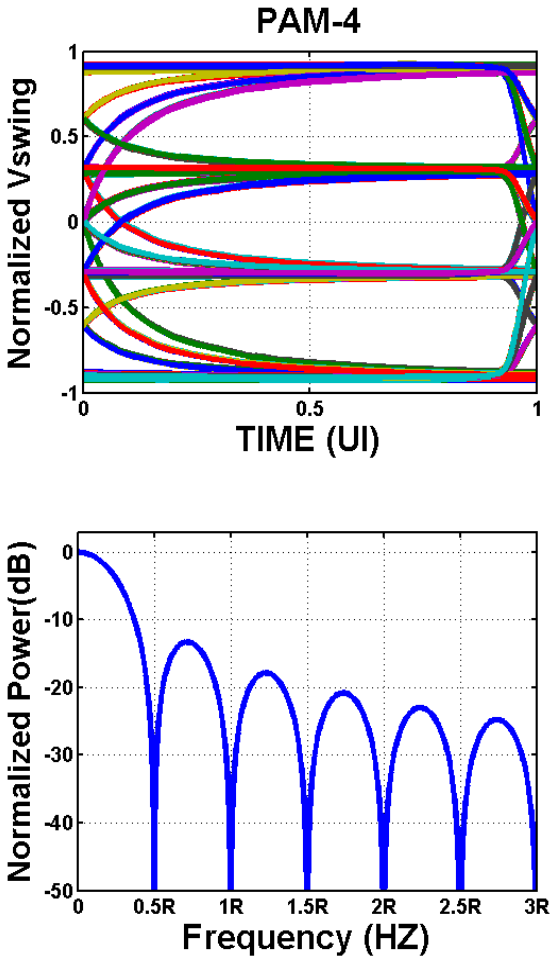


Fig. 3.3. Eye diagrams and power-spectral density of the three common modulation formats of PAM-4

PAM-4 modulation in Fig. 3.3 transmits two-bits per symbol by utilizing four signal levels, reducing the baud rate by a factor of two. This increases the complexity of the receiver to a two-bit ADC, which is typically implemented with three comparators. The reduced baud rate modifies the PAM-4 random data power-spectral density to

$$S_{PAM4} = (10/9)\, T_b sinc^2(2T_b f), \tag{3-2}$$

with the majority of the cumulative signal power contained in half the bandwidth relative to PAM-2 modulation.

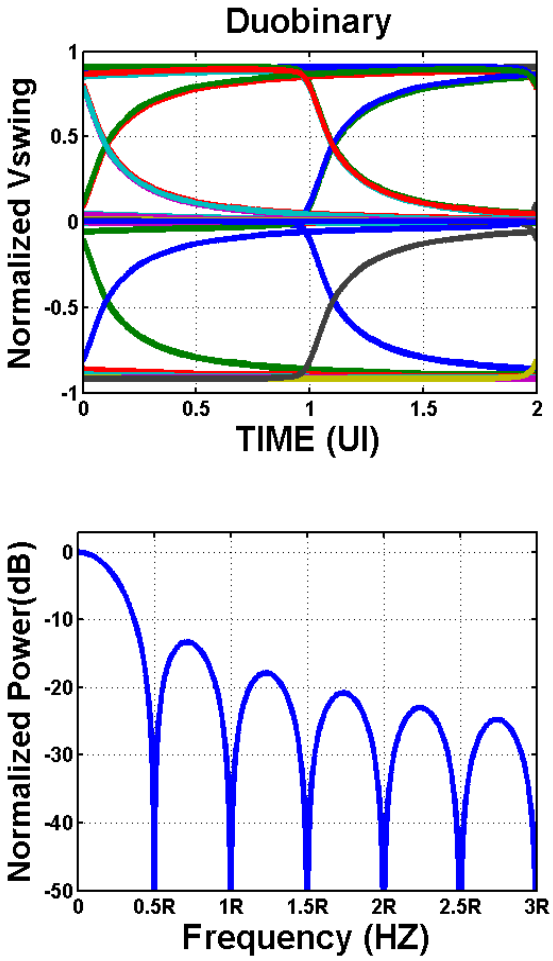


Fig. 3.4. Eye diagrams and power-spectral density of the three common modulation formats of duobinary

Duobinary modulation in Fig. 3.4 uses the same PAM-2 baud rate equal to the bit rate, but allows for a controlled amount of ISI, such that the received signal at time *n* is

$$y_n = x_n + x_{n-1}. \tag{3-3}$$

where x_n is the transmitted signal which is a one-to-one mapping of the data d_n. Here, the duobinary encoding is implemented by leveraging the channel response to provide a portion of this ISI, along with the transmit equalizer. This ideally produces a three-level waveform at the receiver, requiring two comparators at the receiver to decode the data using the previous decision. In order to prevent error propagation at the receiver, often data precoding is implemented in the transmitter, with a modified transmitted signal of

$$x_n = d_n \oplus x_{n-1}. \tag{3-4}$$

After this precoded signal experiences the duobinary encoding, the receiver decoding no longer requires the previous decision, with the mapping

$$\hat{d}_n = \begin{cases} 1 \ if \ y_n = 0 \\ 0 \ if \ y_n = -1,1 \end{cases} \tag{3-5}$$

This controlled ISI results in a duobinary random data power-spectral density of

$$S_{duo} = T_b sinc^2(T_b f) * cos^2(\pi T_b f) = T_b sinc^2(2T_b f) \tag{3-6}$$

which for a given data rate provides the same factor of two signal bandwidth reduction as PAM-4 modulation.

III.2.2 Modulation Selection

In order to consider when a certain modulation format will yield higher link margins, it is possible to compare the channel loss at an effective Nyquist frequency. As PAM-4 sends two bits/symbol, the symbol period is twice as long as the PAM-2 symbol or bit period, T_b. Thus, relative to the PAM-2 Nyquist frequency of $1/(2T_b)$ and for the same

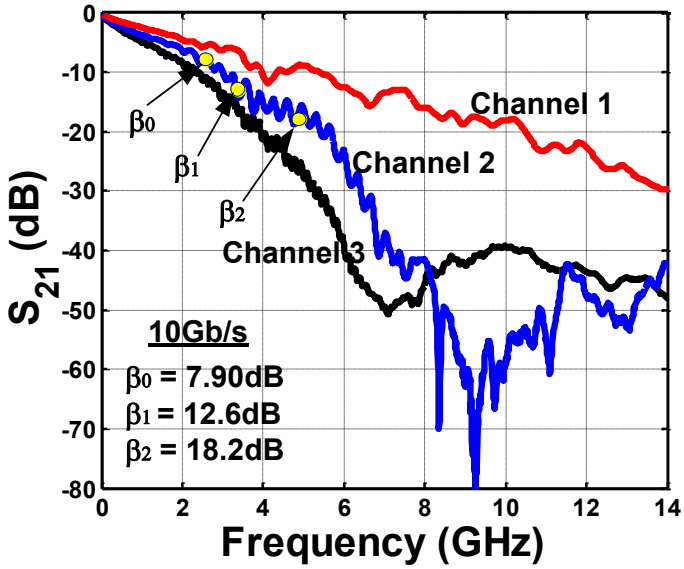


Fig. 3.5. Frequency response of three backplane channels.

data rate, the PAM-4 Nyquist frequency is at one-half this value or $1/(4T_b)$. However, due to the transmitter's peak-power limit, the voltage margin between symbols is 3x (9.54dB) lower with PAM-4 versus simple binary PAM-2 signaling. While duobinary modulation has the same baud rate as PAM-2, the introduction of controlled ISI reduces the effective Nyquist frequency to $1/(3T_b)$ at the cost of a 2x reduction in voltage margin (6dB) due to the three-level waveform at the receiver [5]. Thus, as shown in Table 1, if the PAM-2 Nyquist frequency channel loss, β_2 , is greater than 6dB relative to the effective duobinary Nyquist frequency channel loss, β_1, then duobinary can potentially offer higher SNR. In comparing duobinary versus PAM-4, if the channel loss profile is not overly steep, such that there is less than 3.54dB of loss at β_1 relative to the PAM-4

Nyquist frequency loss, β_0, then duobinary should provide an advantage over PAM-4. If the channel loss profile is steep and displays more than 9.54dB separation between β_2 and β_0, then PAM-4 has the potential to offer the most margin.

The frequency responses of the three backplane channels considered in this work are shown in Fig. 3.5. Channel 1, consisting of ~5" (12.7cm) of traces on line cards and only 1" (2.54cm) on the backplane board, displays the lowest frequency-dependent loss due to both its short length and the use of the bottom backplane signaling layer to minimize impedance discontinuities. The impact of channel length is evident in the increased loss of channel 2, which has ~6" (15.24cm) of traces on line cards and 10" (25.4cm) on the top layer of the backplane board. The backplane via stubs associated with signaling on the top layer introduce a capacitive impedance discontinuity that causes severe loss in this channel near 9GHz. Channel 3 is the longest channel, with ~6" (15cm) line card traces and 20" (50.8cm) of top-layer backplane traces. It also displays a resonant null in the frequency response near 7GHz.

An example of applying the Table 1 modulation selection methodology is shown in Fig. 3.5 for channel 2 at 10Gb/s. The loss at β_2, β_1, and β_0 is 18.2, 12.6, and 7.9dB, respectively. Using Table 1 predicts that PAM-4 will provide the maximum link margin. This will be verified in the simulation results of Section 3. Note, it should be mentioned here that the modulation selection guide provides an initial check as to whether a modulation other than PAM-2 should be considered. Other system considerations, such as cross-talk sources and receiver CDR complexity, should also be considered for the final modulation choice.

III.3. Statistical BER Modeling

While the channel loss-slope parameters of Table. 3.1 serve as an initial guide in modulation choice, other link system effects, such as sensitivity to crosstalk and jitter should be considered. In order to accurately estimate the system BER, a link modeling tool which statistically models voltage and timing noise and ISI and crosstalk distortion is utilized. Both far-end crosstalk (FEXT) and near-end crosstalk (NEXT) models are included for the three backplane channels under consideration, as shown in Fig. 5(a), 6(a) and 7(a).

Table. 3.1. Modulation selection.

$\beta_2 - \beta_1 > 6$dB	$\beta_2 - \beta_1 < 6$dB
$\beta_1 - \beta_0 < 3.54$dB **→Duobinary**	$\beta_2 - \beta_0 > 9.54$dB **→PAM-4**
$\beta_1 - \beta_0 > 3.54$dB **→PAM-4**	$\beta_2 - \beta_0 < 9.54$dB **→PAM-2**
β_0 : PAM-4 Nyquist frequency(1/(2Tb)) channel loss β_1 : Effective duobinary Nyquist frequency(1/(3Tb)) channel loss β_2 : PAM-2 Nyquist frequency(1/(4Tb)) channel loss	

The "thru" and crosstalk channels are assumed as linear time-invariant (LTI) [25] and the received signal y_k is described in the PAM-2 and PAM-4 case as,

$$y_k = I_{k,THRU} h_{k,THRU} + \sum_{i \neq k}^{N} I_{i,THRU} h_{i,THRU} + \sum_{m}^{N} I_{m,FEXT} g_{i,FEXT}$$

$$+\sum_{m}^{N} I_{m,NEXT} g_{i,NEXT} + Z_k \tag{3-7}$$

where k is the cursor index, $I_{i,THRU}$, $I_{i,FEXT}$ and $I_{i,NEXT}$ are the transmitting symbols through corresponding channels, $h_{i,THRU}$, $g_{i,FEXT}$ and $g_{i,NEXT}$ are the sampled pulse responses of N-tap equalized thru, FEXT, and NEXT channels, respectively, and Z_k is a random noise component. Since (7) consists of a linear combination of independent random variables, the received signal PDF is obtained by convolving the independent random variables PDFs. In the duobinary case, as both the cursor and first post-cursor are utilized for a decision, the received signal expression is modified to,

$$\begin{aligned} y_k = \pm I_{k,THRU} h_{k,THRU} \pm I_{k-1,THRU} h_{k-1,THRU} + \sum_{i \neq k,k-1}^{N} I_{i,THRU} h_{i,THRU} \\ + \sum_{m}^{N} I_{m,FEXT} g_{i,FEXT} + \sum_{m}^{N} I_{m,NEXT} g_{i,NEXT} + Z_k \end{aligned} \tag{3-8}$$

where $\pm I_k h_k \pm I_{k-1} h_{k-1}$ are four possible cursor values to represent three symbols(-2, 0, 2) [29]. Timing jitter is introduced with a dual-Dirac receiver-side jitter model, which modifies the received signal PDF as

$$p(v,t) = p(v|t)p(t) \tag{3-9}$$

where *p(t)* is the time-domain jitter probability model and *p(v|t)* is the received signal PDFs at a given sampling time *t* [26].

This statistical link modeling tool can be utilized to rapidly explore trade-offs in modulation schemes and equalization partitioning and complexity. Fig. 4 shows that the maximum achievable data rate versus TX equalization taps for channel 3 (Fig 7(a)), with

the system modeling parameters of $1mV_{rms}$ random noise, 1% bit (T_b) deterministic jitter (DJ) and σ=1% T_b random jitter (RJ). Also, the transmitter equalization taps are optimized in a minimum mean-squared error manner, the transmit signal dynamic range is constrained to $1V_{ppd}$, and a minimum receiver eye height margin of 10mV at a BER=10^{-12} is used to set the maximum data rate.

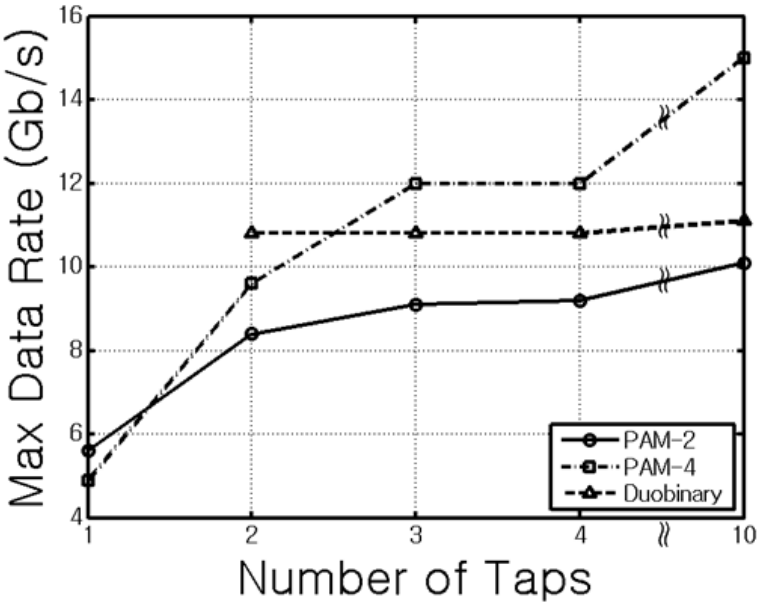


Fig. 3.6. Maximum achievable data rate with channel 3 based on the number of TX-FFE taps for the three modulation schemes.

Table 3.2. 10Gb/s FFE coefficients and link margin with channel 1.

	a_{-1}	a_0	a_1	BER=10^{-12}	
				H(mV)	W(ps)
PAM2	-0.0492	0.7177	-0.2331	220.4	56
PAM4	-0.0179	0.8824	-0.0997	117.8	80
DUO	0.4951	0.3273	-0.1776	154.7	57

For the PAM-2 and PAM-4 cases of Fig. 3.6, significant improvements in data rate are achieved by including transmit equalization with two taps. While scaling to three taps provides some additional performance benefits, improvements with four or more taps is somewhat incremental. As doubinary modulation includes ISI by definition, a two-tap equalizer is necessary. While duobinary achieves the highest data rate with two-taps of equalization, adding more taps doesn't dramatically improve the achievable data rate.

Simulations are performed with the three backplane channels to illustrate the relative performance of the three modulation formats with the inclusion of a three-tap transmit equalizer with a pre-cursor tap, α_{-1}, cursor tap, α_0, and post-cursor tap, α_1. Two crosstalk aggressor channels, one FEXT and one NEXT, are included with the same input power as the main "thru" transmitted signal. Fig. 3.7 (b)-(d) shows 10Gb/s transient random 1k-bit eye diagrams and the BER=10^{-12} eye contour from the statistical link model with channel number 1, where the loss profile is 4.5, 6.8, and 9.1dB for β_0, β_1, and β_2, respectively. Table 3.2 confirms that PAM2 modulation yields the largest voltage margin,

Table 3.3. 10Gb/s FFE coefficients and link margin with channel 2.

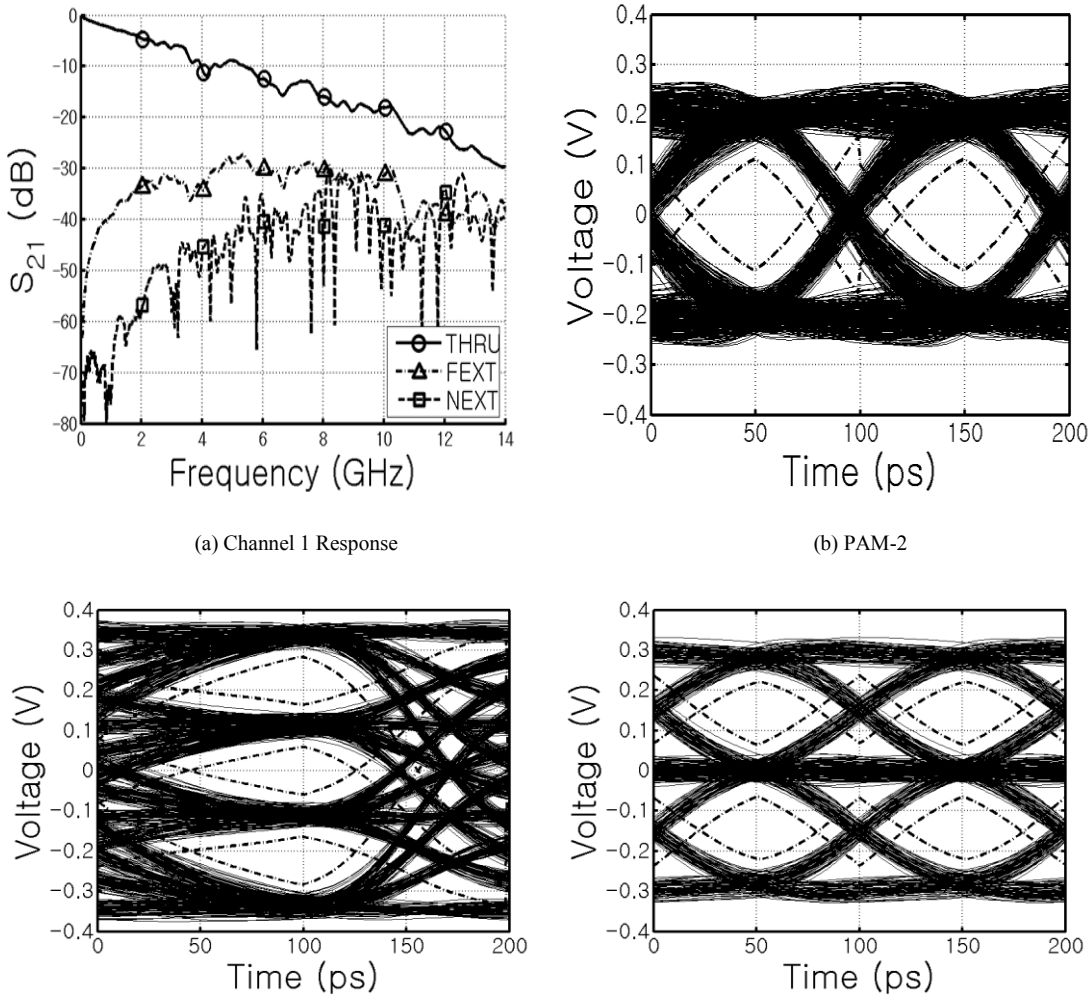
	a_{-1}	a_0	a_1	BER=10^{-12}	
				H(mV)	W(ps)
PAM2	-0.1669	0.5994	-0.2337	14.2	13
PAM4	-0.0470	0.7972	-0.1559	44.4	36
DUO	0.7246	-0.2669	0.0086	8.3	7

Table 3.4. 8Gb/s FFE coefficients and link margin with channel 3.

	a_{-1}	a_0	a_1	BER=10^{-12}	
				H(mV)	W(ps)
PAM2	-0.1685	0.5917	-0.2398	54.2	41.25
PAM4	-0.0459	0.7767	-0.1774	58.4	65
DUO	0.7302	-0.2297	-0.0401	62	47.5

as expected with this low loss channel. Note the performance degradation from the 1k-bit transient simulation to the BER=10^{-12} eye contour. The statistical link model allows rapid performance analysis to this low error rate with the consideration of the different link system effects, something that is not feasible with transient simulations. Fig. 3.8 (b)-(d) shows 10Gb/s results with channel number 2, where the loss profile is 7.9, 12.6, and 18.2dB for β_0, β_1, and β_2, respectively. Table 3.3 confirms that PAM4 modulation yields the largest voltage and also timing margin, as expected with this high loss channel with a steep loss slope around this data rate.

In order to illustrate a scenario where duobinary modulation provides superior voltage margin, 8Gb/s operation over channel 3 is considered. Channel 3 has overall high loss, but relatively moderate loss slope around this data rate, with a loss profile of 8.5, 11.5, and 21.5dB for β_0, β_1, and β_2, respectively. Fig. 3.9 (b)-(d) shows the 8Gb/s results and Table 3.4 confirms that duobinary modulation yields the largest voltage margin.



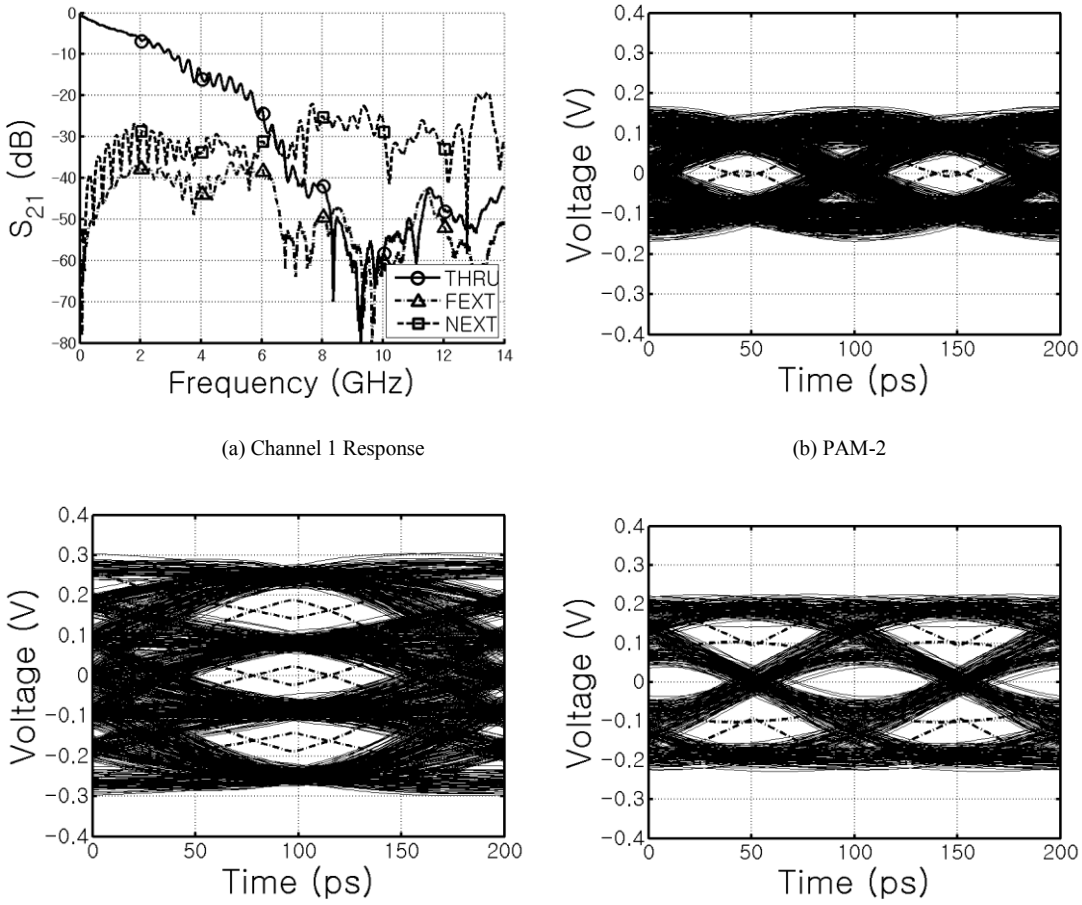
(a) Channel 1 Response

(b) PAM-2

(c) PAM-4

(d) Duobinary

Fig. 3.7. 10Gb/s eye diagrams with channel 1. Solid lines are transient 1k-bit simulations and dashed lines are BER=10^{-12} contours obtained from the statistical link model.



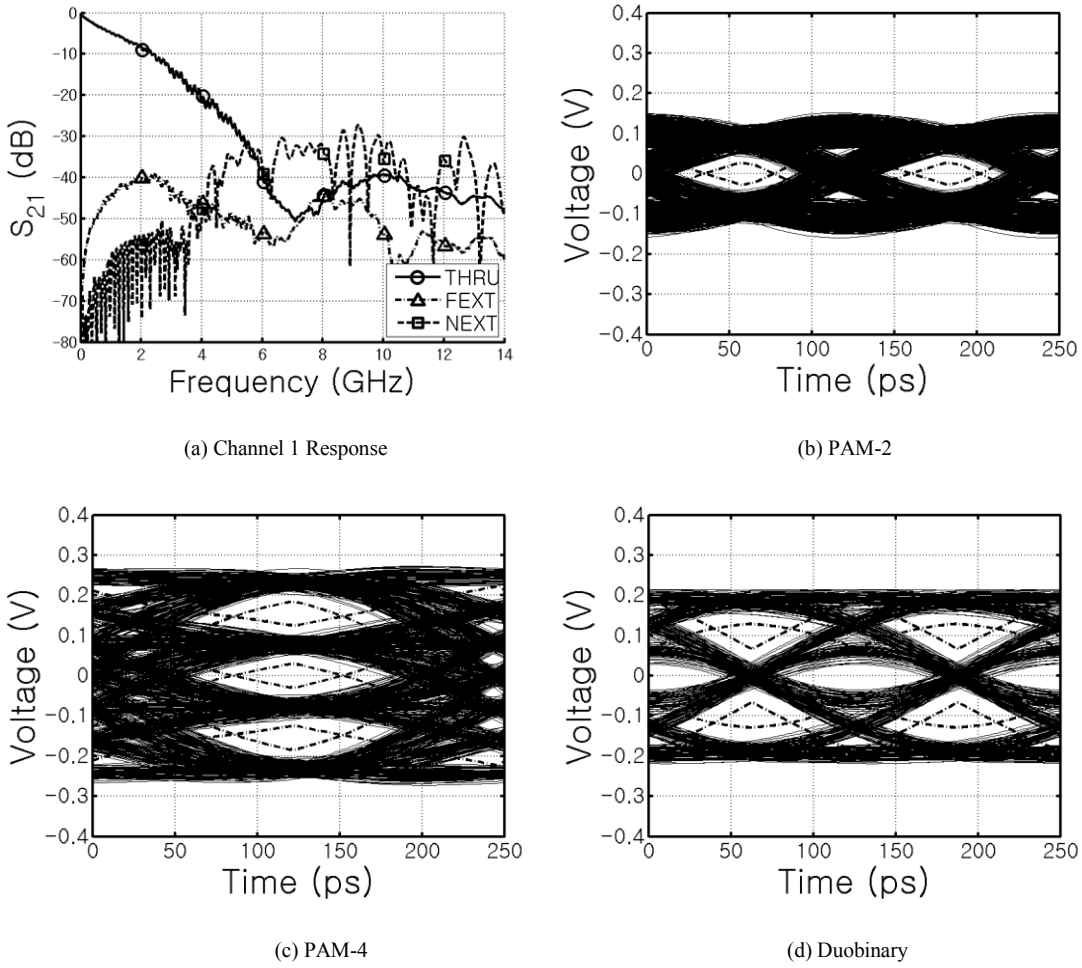
(a) Channel 1 Response

(b) PAM-2

(c) PAM-4

(d) Duobinary

Fig. 3.8. 10Gb/s eye diagrams with channel 2. Solid lines are transient 1k-bit simulations and dashed lines are BER=10^{-12} contours obtained from the statistical link model.



(a) Channel 1 Response

(b) PAM-2

(c) PAM-4

(d) Duobinary

Fig. 3.9. 8Gb/s eye diagrams with channel 3. Solid lines are transient 1k-bit simulations and dashed lines are BER=10^{-12} contours obtained from the statistical link model.

Sensitivity to crosstalk and timing jitter are important considerations in the selection of the modulation format. In order to gain intuition on these effects, the distortion variance due to ISI and crosstalk is derived for the three modulation formats. Assuming PAM-2 symbols with value 1,-1, the distortion variance is

$$\sigma_{\mathrm{PAM2}}^2 = \sum_{\mathrm{i}\neq\mathrm{k}}^{\mathrm{N}}\left\{\frac{1}{2}\left(1\cdot \mathrm{h_{i,PAM2}}\right)^2 + \frac{1}{2}\left(-1\cdot \mathrm{h_{i,PAM2}}\right)^2\right\}$$
$$+ \sum_{\mathrm{i}}^{\mathrm{M\cdot N}}\left\{\frac{1}{2}\left(1\cdot \mathrm{g_{i,PAM2}}\right)^2 + \frac{1}{2}\left(-1\cdot \mathrm{g_{i,PAM2}}\right)^2\right\} \quad (3\text{-}10)$$
$$= \sum_{\mathrm{i}\neq\mathrm{k}}^{\mathrm{N}} \mathrm{h_{i,PAM2}^2} + \sum_{\mathrm{i}}^{\mathrm{M\cdot N}} \mathrm{g_{i,PAM2}^2}$$

where N is the channel length, M is the number of crosstalk channels, $h_{i,PAM2}$ are the equalized and sampled thru channel pulse response and $g_{i,PAM2}$ are the sampled crosstalk pulse responses filtered by a transmitted FIR equalizer.

Likewise, with the same peak signal level, the distortion variance for duobinary modulation is

$$\sigma_{\mathrm{DUO}}^2 = \left(\left|\mathrm{h_{k,DUO}}\right| - \left|\mathrm{h_{k-1,DUO}}\right|\right)^2 + \sum_{\mathrm{i}\neq\mathrm{k,k-1}}^{\mathrm{N}} \mathrm{h_{i,DUO}^2} + \sum_{\mathrm{i}}^{\mathrm{M\cdot N}} \mathrm{g_{i,DUO}^2}, \quad (3\text{-}11)$$

where the first term is due to mismatch between cursor and precursor.

For PAM-4,

$$\sigma_{\mathrm{PAM4}}^2 = \sum_{\mathrm{i}\neq\mathrm{k}}^{\mathrm{N}}\left\{\frac{1}{4}\left(1\cdot \mathrm{h_{i,PAM4}}\right)^2 + \frac{1}{4}\left(\frac{1}{3}\cdot \mathrm{h_{i,PAM4}}\right)^2 + \frac{1}{4}\left(-\frac{1}{3}\cdot \mathrm{h_{i,PAM4}}\right)^2\right.$$
$$\left. + \frac{1}{4}\left(-1\cdot \mathrm{h_{i,PAM4}}\right)^2\right\}$$
$$+ \sum_{\mathrm{i}\neq\mathrm{k}}^{\mathrm{N}}\left\{\frac{1}{4}\left(1\cdot \mathrm{g_{i,PAM4}}\right)^2 + \frac{1}{4}\left(\frac{1}{3}\cdot \mathrm{g_{i,PAM4}}\right)^2 + \frac{1}{4}\left(-\frac{1}{3}\cdot \mathrm{g_{i,PAM4}}\right)^2\right. \quad (3\text{-}12)$$
$$\left. + \frac{1}{4}\left(-1\cdot \mathrm{g_{i,PAM4}}\right)^2\right\}$$

$$= \frac{5}{9}\sum_{i\neq k}^{N} h_{i,PAM4}^2 + \frac{5}{9}\sum_{i}^{M\cdot N} g_{i,PAM4}^2$$

Interestingly, the PAM-4 distortion variance crosstalk term is smaller relative to the PAM-2 and duobinary cases, implying that PAM-4 will display less sensitivity to increased levels of crosstalk. In order to illustrate this, the statistical link modeling tool is utilized to simulate 8Gb/s operating over channel 3 with the three modulation formats and crosstalk levels ranging from none, one FEXT and one NEXT aggressor from Fig. 3.9 (a), and with these crosstalk channels boosted by 6dB. The eye height results of Fig. 3.10 confirm that relative to the no crosstalk case, PAM-4 displays the least amount of degradation due to increased levels of crosstalk. While duobinary modulation displays the most eye height with no and normal crosstalk, when the crosstalk is boosted by 6dB PAM-4 achieves superior eye height.

The longer symbol period of PAM-4 also allows for reduced jitter sensitivity, as illustrated in Fig. 3.11. While the nominal 1% DJ and σ=1% RJ assumptions result in duobinary displaying the most 8Gb/s eye height, when jitter is increased PAM-2 and duobinary performance degrades at a similar rate that is more severe than the PAM-4 reduction. When jitter levels are increased to near σ=2% RJ, PAM-4 displays superior eye height.

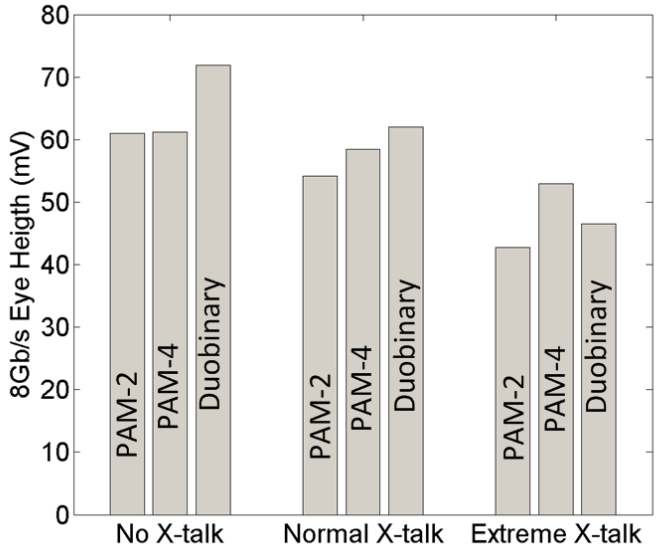


Fig. 3.10. 8Gb/s eye height degradation with crosstalk for channel 3.

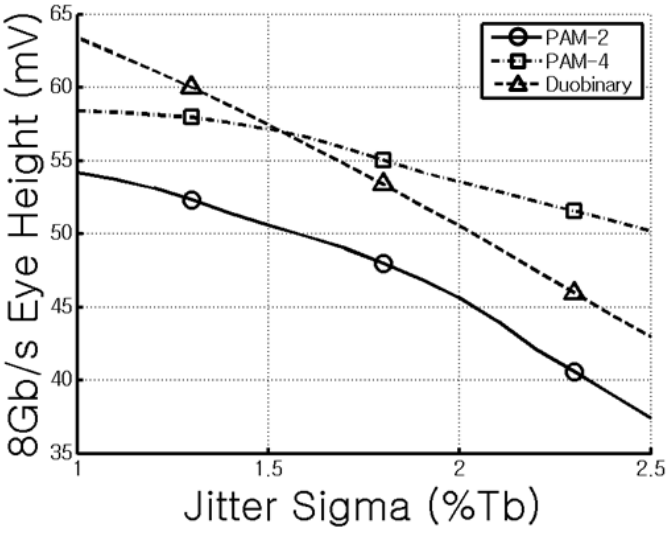


Fig. 3.11. 8Gb/s eye degradation vs. random jitter for channel 3.

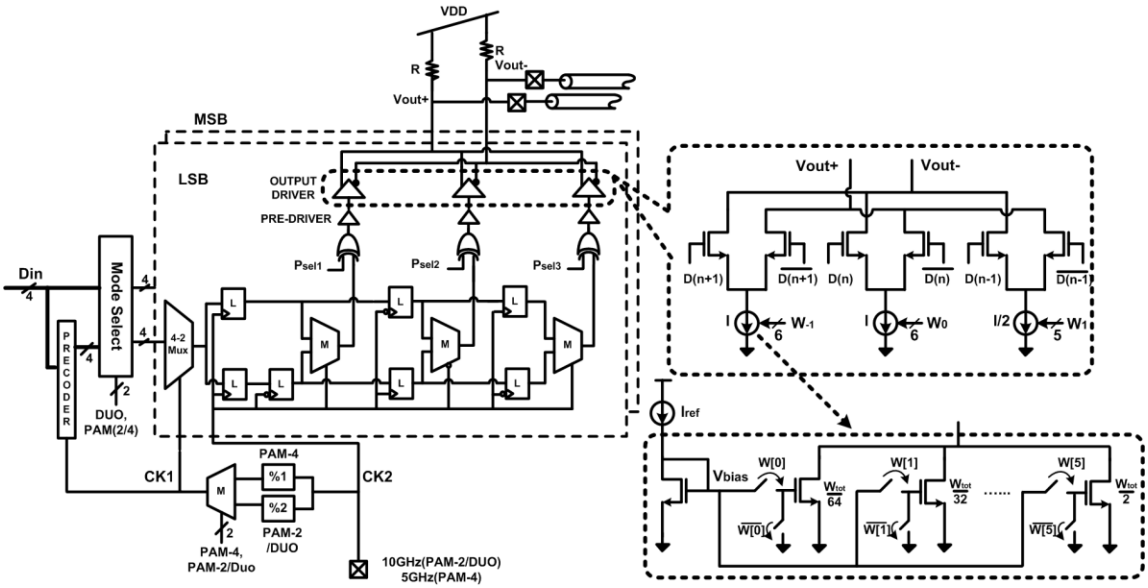


Fig. 3.12. Triple-mode transmitter architecture.

III.4. Transmitter Design

III.2 and III.3 detailed how the optimal modulation format for maximum eye margins is a function of the channel loss profile, crosstalk, random noise, and jitter. This section discusses the design of a transmitter which can efficiently support all three of these modulation formats, providing a high degree of flexibility to support different channel environments and, for a given platform, the ability to scale to high data rates during periods of peak I/O bandwidth demand.

III.4.1 System Architecture

Fig. 3.12 shows a block diagram of the half-rate transmitter which efficiently supports PAM-2, PAM-4, and duobinary modulation. The transmitter's input consists of four parallel input data bits at the quarter-rate clock, 5Ghz at 20Gb/s. Depending on the

selected modulation, a CMOS mode select block either chooses the raw input data for PAM-2 and PAM-4 mode or data which passes through the power-efficient quarter-rate CMOS precoder for duobinary mode. This data is then routed to the CML output stage which performs serialization and implements a three-tap feed-forward equalizer. The output stage has been segmented into an MSB and LSB path, with the MSB path sized for double the current output capability of the LSB path. In PAM-2 and duobinary mode, the mode select block routes the four data bits to both the MSB and LSB block for serialization with two cascaded mux stages clocked with the quarter-rate and half-rate clock, respectively.

In PAM-4 mode, the mode select block routes the two even bits to the MSB segment and the two odd bits to the LSB segment. Power savings are achieved in PAM-4 mode by clocking both mux stages by the quarter-rate or half-symbol-rate clock (5GHz for 20Gb/s); with only the second mux stage actually switching. The feed-forward equalization is implemented by spreading the symbol's energy over three bit periods, one pre-cursor, one main-cursor, and one post-cursor tap, with the tap weights set by current-mode DACs which controls the three parallel current-mode output stages. For the pre-, main-, and post-cursor taps, respectively, the FFE taps weights are sized to maximum relative weights of 1, 1, and 0.5 at a resolution of 64, 64, and 32 steps for equal LSB weight. Note, the pre-cursor tap has the same maximum range as the main-cursor to support duobinary modulation. Equalization coefficients for all data formats are acquired with a minimum-mean-square-error algorithm [32]

$$\begin{bmatrix} y(0) \\ y(1) \\ \cdots \\ y(l+k-2) \end{bmatrix} = \begin{bmatrix} p(0) & 0 & 0 & \cdots & 0 & 0 \\ p(1) & p(0) & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & p(k-1) & p(k-2) & \\ 0 & 0 & \cdots & 0 & p(k-1) & \end{bmatrix} \begin{bmatrix} h(0) \\ h(1) \\ \cdots \\ h(l-1) \end{bmatrix} \tag{3-13}$$

$$H_{ls} = (P^T P)^{-1} P^T Y_{des} \tag{3-14}$$

where here y is the desired pulse response with an l-tap equalizer, h, and p is the un-equalized pulse response with k samples.

The ability to choose the appropriate modulation for a given channel response and data rate, coupled with the efficient duobinary precoder described next, allows the flexibility to support a wide range of operating conditions.

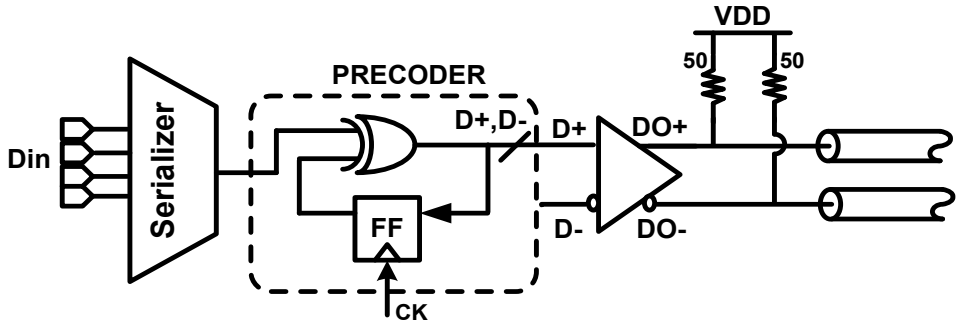
III.4.2 Duobinary Precoder Design

As discussed in III.2, systems which implement duobinary modulation often employ precoding to avoid error propagation at the receiver. While the precoder is often implemented after serialization [5] (Fig. 3.13(a)), this requires a full-rate clock signal and careful design to meet the tight timing margin. High-power CML logic is generally necessary for the full-rate precoders of Fig. 3.14 and Fig. 3.15. The critical path of the Fig. 3.14 implementation is

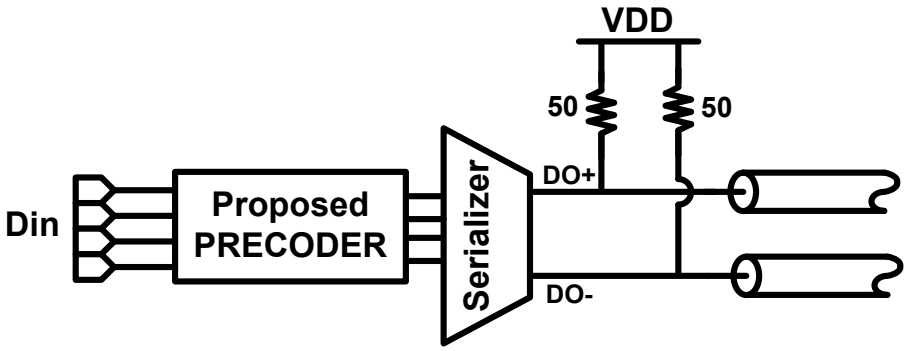
$$T_b - \left(T_{xor} + T_{D \to Q}\right) > T_{setup} \tag{3-15}$$

while for Fig. 3.15 it is

$$0 < T_{margin} < T_b/2 \tag{3-16}$$



(a)



(b)

Fig. 3.13. Precoder implementations. (a) Full-rate architecture. (b) Proposed parallel quarter-rate architecture.

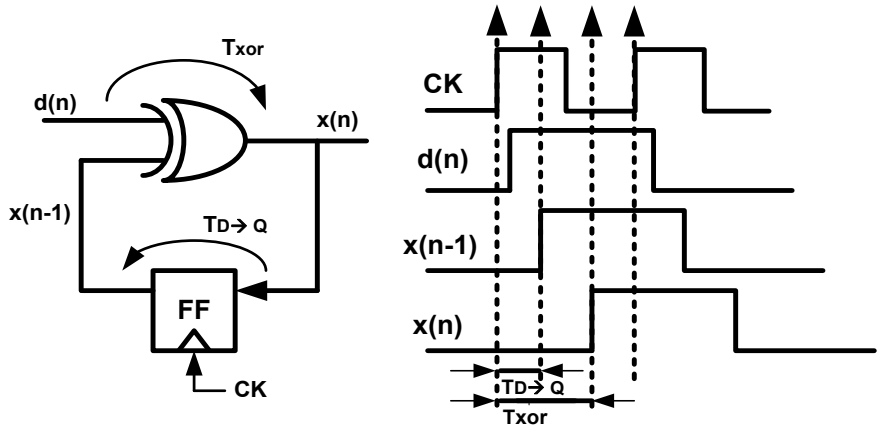


Fig. 3.14. General full-rate precoder timing diagram.

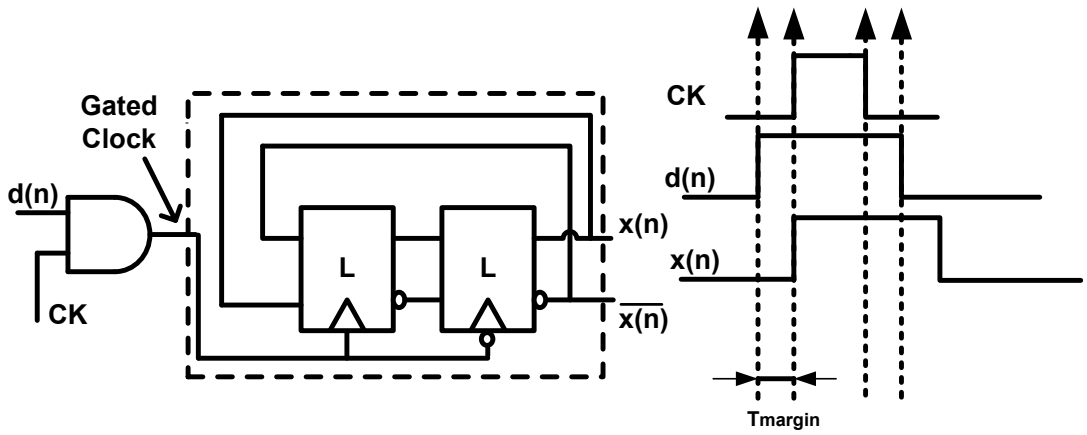


Fig. 3.15. Modified full-rate precoder timing diagram [5].

This thesis proposes computation of the precoder operation in parallel before serialization at the quarter-rate clock cycle time (Fig. 3.13(b)). This allows the use of static CMOS circuitry, with power that dynamically scales with data rate.

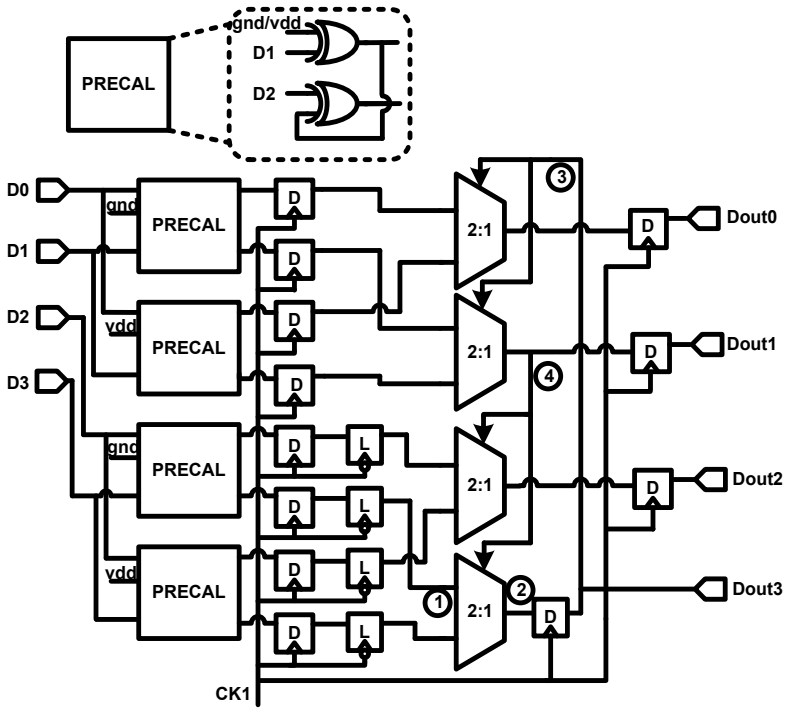


Fig. 3.16. Parallel quarter-rate precoder circuit.

The proposed parallel precoder is shown in Fig. 3.16. In order to improve the precoder timing margin, the input data is speculatively computed with the two possible previous precoded values of *VDD* or *GND* in a PRECAL block comprised of 2 XOR gates. These precomputed values are then stored in flip-flops and passed to a mux controlled by the previous cycle's output data to select the appropriate pre-computed value. For example, D_{out3} from the previous cycle selects between the computation of

$$D_0 \oplus 0 \;\; OR \;\; D_0 \oplus 1 \tag{3-17}$$

to produce the next D_{out0} signal and

$$D_1 \oplus (D_0 \oplus 0) \;\; OR \;\; D_1 \oplus (D_0 \oplus 1) \tag{3-18}$$

to produce the next D_{out1} signal.

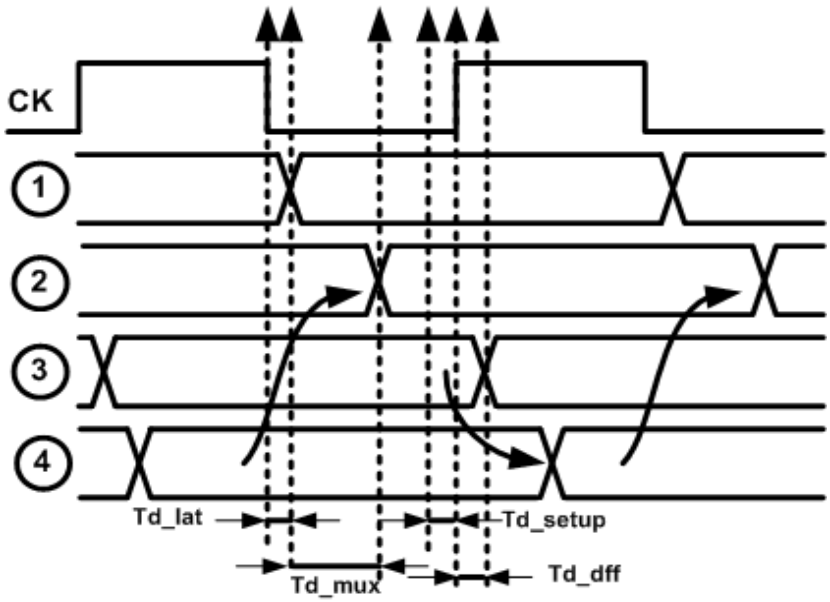


Fig. 3.17. Parallel quarter-rate precoder timing diagram.

The timing diagram of the proposed quarter-rate precoder is shown in Fig. 3.17. The circuit's critical path is set by the half-cycle path from node 1 to D_{out3}

$$\frac{T_{qclk}}{2} = 2T_b > T_{d\_lat} + T_{d\_mux} + T_{setup}, \tag{3-19}$$

assuming that node 4 has settled in a half-cycle, or the full-cycle path starting and ending at node 2 given by

$$T_{qclk} = 4T_b > T_{d\_dff} + 2T_{d\_mux} + T_{setup}. \tag{3-20}$$

The simulation results of Fig. 16, performed in a GP 90nm CMOS process, verify the duobinary precoder operation at 5GHz. The four parallel incoming data bits are correctly precoded according to (4). Executing the precoding in parallel at the quarter-rate clock

frequency allows for the use of an all-CMOS design that operates at the nominal 1V supply.

III.5. Experimental Results

The 20Gb/s triple-mode transmitter was designed in a GP 1V 90nm CMOS process, with the chip layout and chip photo shown in Fig. 3.19 and Fig. 3.20. Significant area savings are achieved through the use of the all-CMOS precoder, with the total transmitter occupying an area of $0.17mm^2$.

Post-layout simulations are performed with the three backplane channels in Fig. 3.5 to verify the different modulation capabilities and which modulation provides the most margin for a given channel and data rate. Fig. 3.21, 3.22, and 3.23 repeat the simulation results presented in III.3 with the actual transmitter.

As expected, for the low-loss channel 1 PAM-2 modulation provides the most eye height, while PAM-4 provides the most 12.5Gb/s eye height for the steep loss slope channel 2, and duobinary provides the most 8Gb/s eye height for the more gradual slope channel 3. Table 3.5 summarizes these simulation results. Relative to the ideal transmitter modeled in Section 3, the designed transmitter suffers some eye margin degradation due to finite pre-driver transition times and additional pad parasitics.

Fig. 3.24 shows eye diagrams with an ideal channel to confirm 20Gb/s operation. Table 3.6 summarizes the 20Gb/s transmitter performance and compares the design with other recent high-speed serial I/O transmitters.

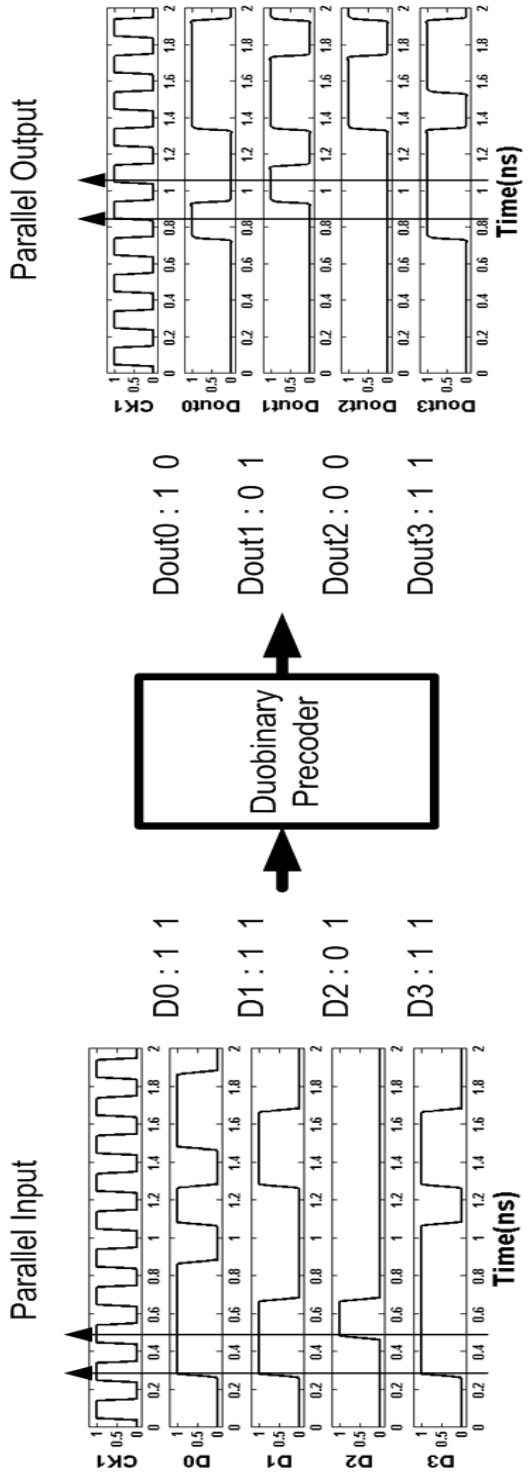


Fig. 3.18. Duobinary precoder simulation at 5GHz.

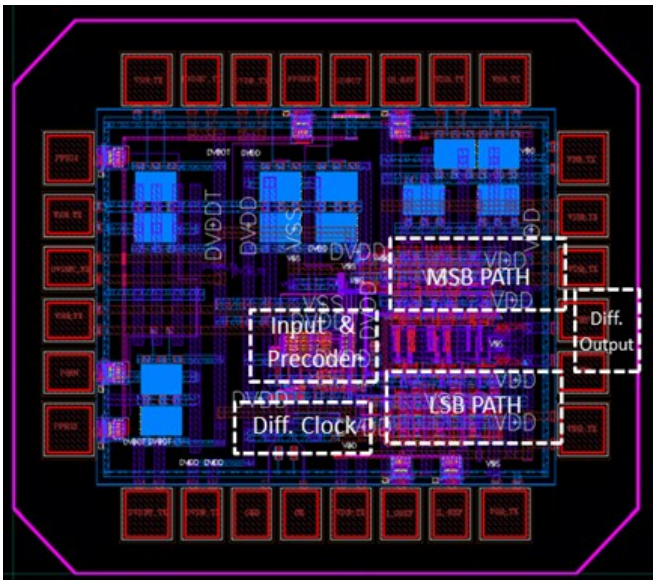


Fig. 3.19. Triple-mode transmitter chip layout.

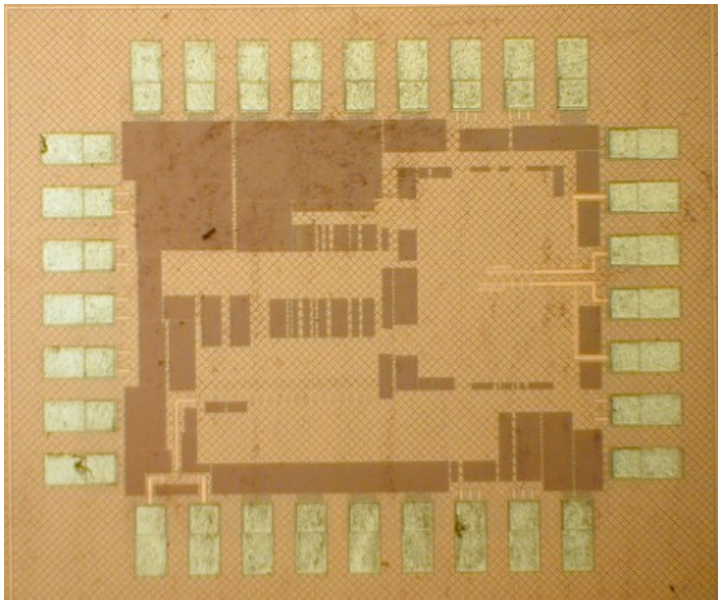


Fig. 3.20. Microphotograph of chip

Table 3.5. Summary of results.

Channel	Data Rate (Gbps)	Selected Mode	Macromodel Simulation with #1K bit.		Transistor-level Simulation with #1K bit	
			H(mV)	W(ps)	H(mV)	W(ps)
1	10	PAM-2	275.6	81	268.2	80
2	10	PAM-4	110.6	86	100.1	83
3	8	Duo	129.5	87.5	104.2	76

Table 3.6. Transmitter comparison.

	[5] (P-2,P-4,duo) (Separate Designs)	[28]	[30]	[31]	This Work (P-2,P-4,duo) (Single Design)
Process Technology(nm)	90	90	130	180	90
Supply Voltage(V)	1.5, 1.8, 1.5	1.2	1.2	1.8	1
Power(mW)	100, 150, 120	133	165	32	114,103,122
Swing(mV_{pp})	200,400,200	N.A	400	600	1000
# of Taps	3	5	2	No TX Equalizer	3
Area(mm^2)	P-2 : 0.224 P-4 : 0.156 duo: 0.228	duo : 0.18	P-2 : 0.228	duo : N.A	0.17
Max Data Rate(Gb/s)	20	12	20	8	20

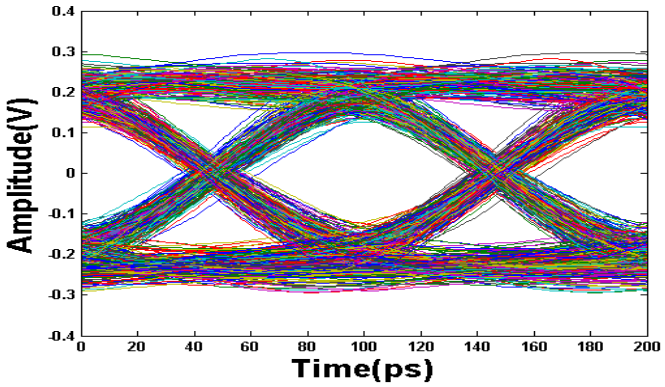


Fig. 3.21. 10Gb/s PAM-2 eye diagram from designed transmitter operating with channel 1.

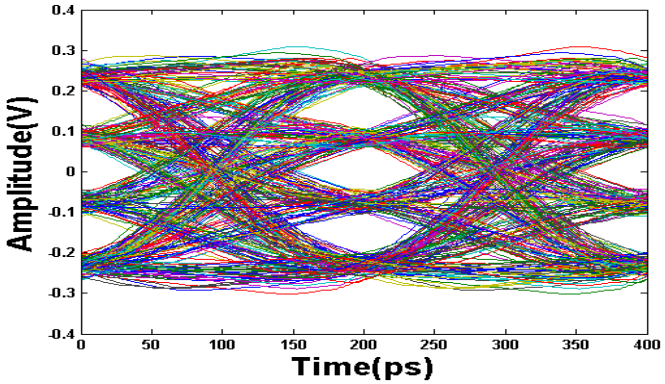


Fig. 3.22. 10Gb/s PAM-4 eye diagram from designed transmitter operating with channel 2.

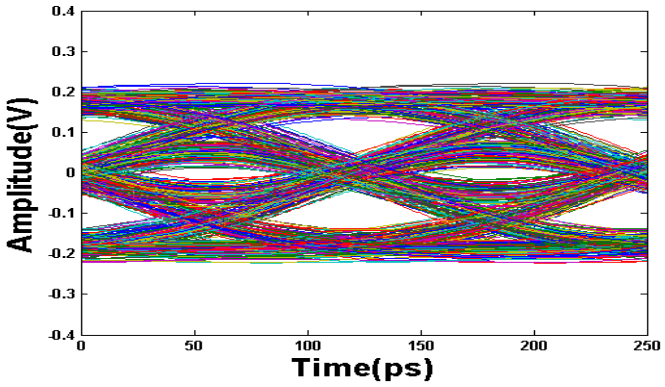
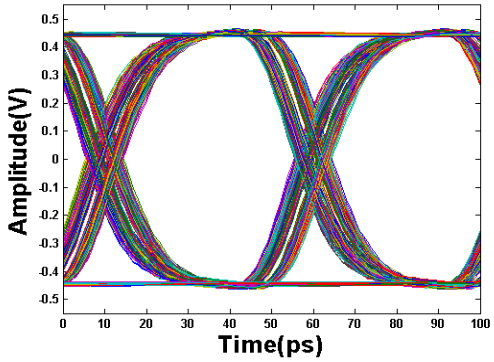
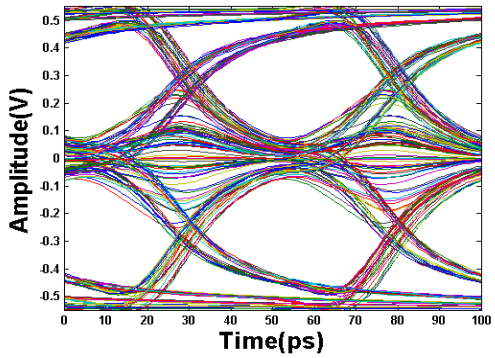


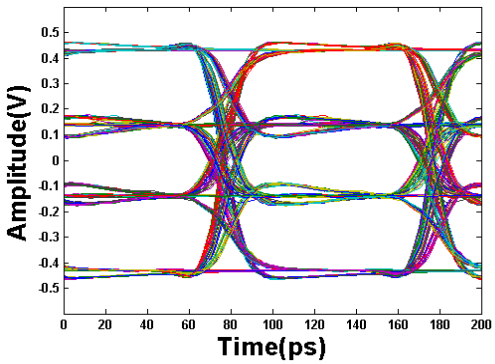
Fig. 3.23. 8Gb/s duobinary eye diagram from designed transmitter operating with channel 3.



(a) PAM-2



(b) Duobinary



(c) PAM-4

Fig. 3.24. 20Gb/s eye diagrams from designed transmitter operating with an ideal channel.

The Fig. 3.35 shows PCB board mounted with a chip of a triple-mode supported transmitter. It has two pairs of microstrip lines for differential clock and output to support high-speed clock and data. Also high-speed supported SMA connectors are used to reduce the gain loss of a regular SMA. NI-DAQ equipment from National Instrument is used for setting the control registers in the chip. The Fig. 3.26 shows measurement setup for testing the chip-on-board.

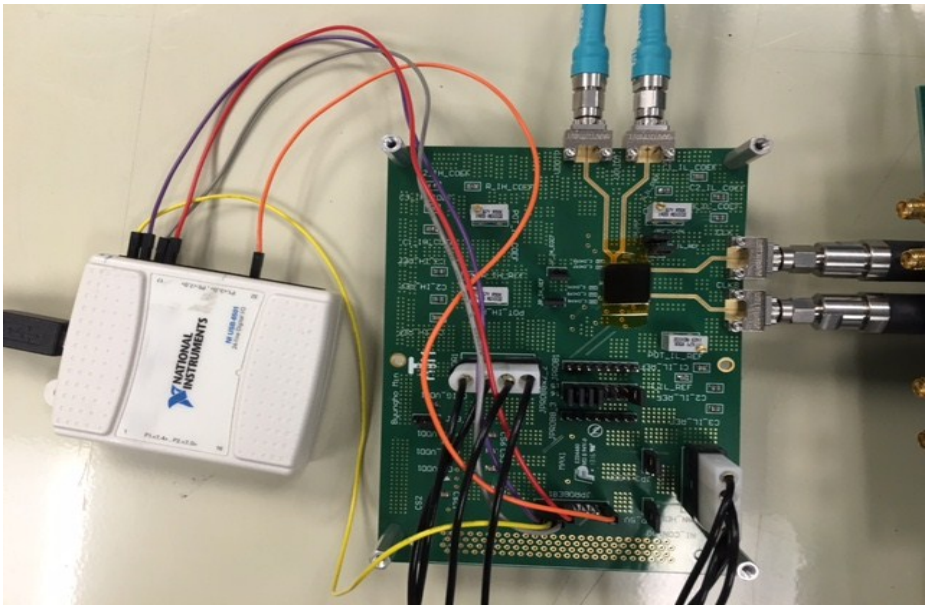


Fig. 3.25. Testing PCB board

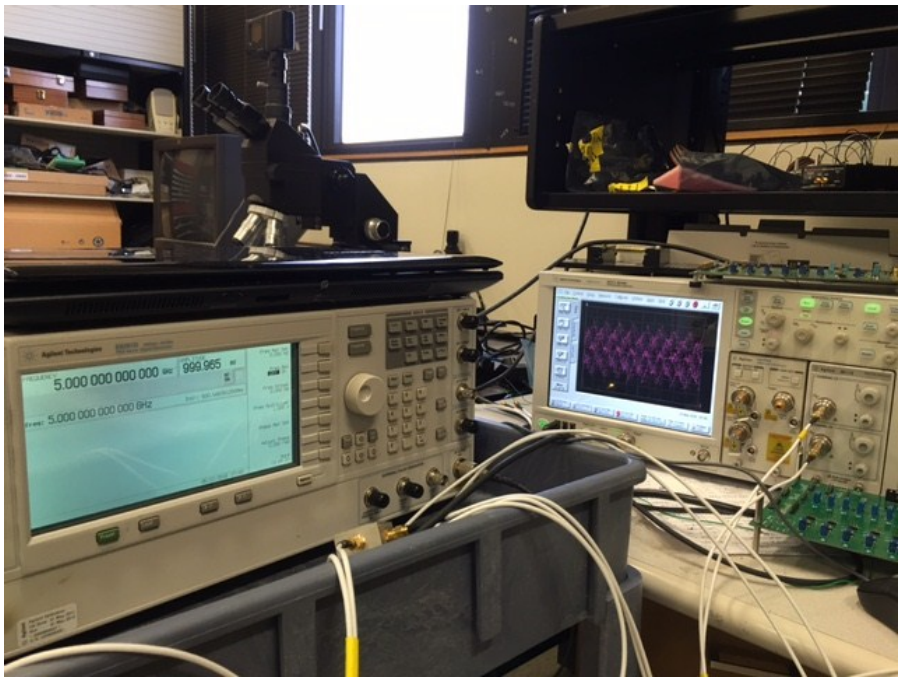


Fig. 3.26. Measurement setup

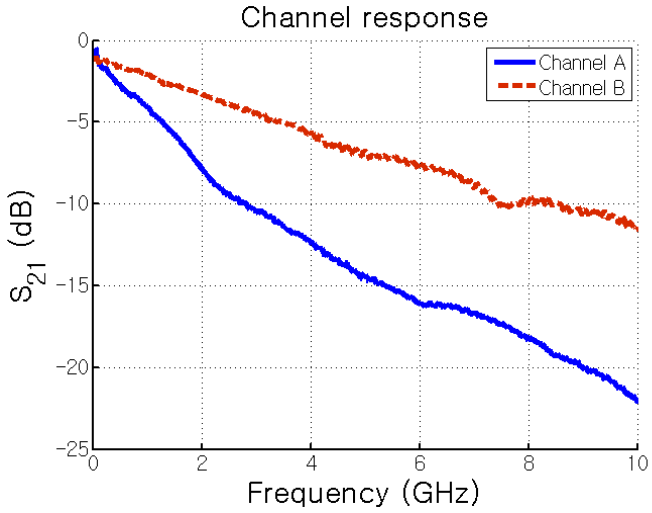


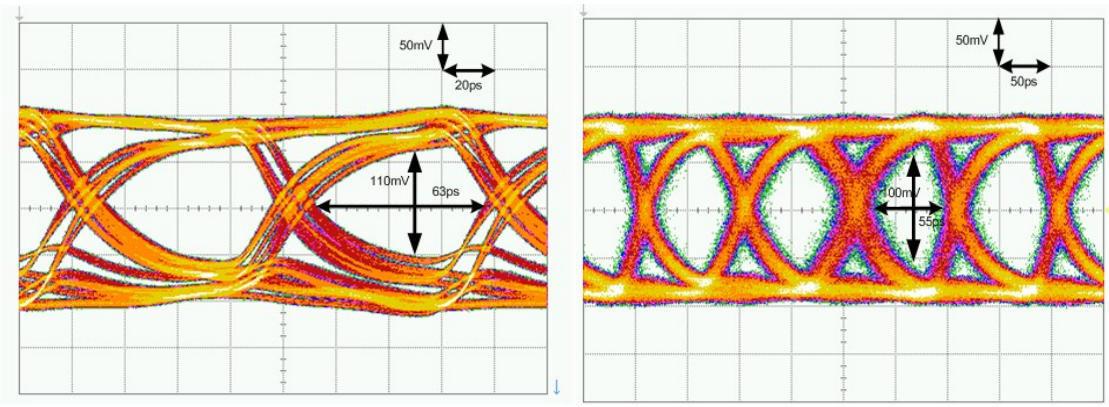
Fig. 3.27. Channel response (a) short channel (Channel A), and (b) long channel (Channel B)

The Fig. 3.27 shows channel responses of channels that are used in the test. Channel A (short channel) and Channel B (long channel) are approximately 4.5 and 14 inch long respectively. Both channels are not steep, and kind of smooth characteristic.

A chip-on-board test setup is utilized, with the die directly wire-bonded to the FR4 board as shown in Fig 3.26. In order to demonstrate the transmitter functionality, the eye diagrams of Fig. 3.28~3.30 are produced with a short 4.5" and a long 14" channel. In order to demonstrate transmitter operation, the transmitter coefficients are acquired by optimization technique at a given data rate to achieve maximum eye height and width at the channel output in both cases. Table 3.7 shows optimized 3-tap coefficients for transmitter. As it is mentioned before, if the channel loss profile is not overly steep, such that there is less than 3.54dB of loss at β_1 relative to the PAM-4 Nyquist frequency loss, β_0, then duobinary should provide an advantage over PAM-4. Also if the PAM-2 Nyquist frequency channel loss is less than 6dB relative to the effective duobinary Nyquist frequency channel loss, β_1, then duobinary can potentially offer lower SNR. Also if we apply this rule to the first testing with short channel, then we can acquire these relationships : $\beta_2 - \beta_1 < 6$ dB, $\beta_1 - \beta_0 < 3.54$ dB and $\beta_2 - \beta_0 < 9.54$ dB. It means we predict that PAM-2 will provide the maximum link margin. Also the results show that the eye opening of PAM-2 is the largest among them as shown in Table 3.7.

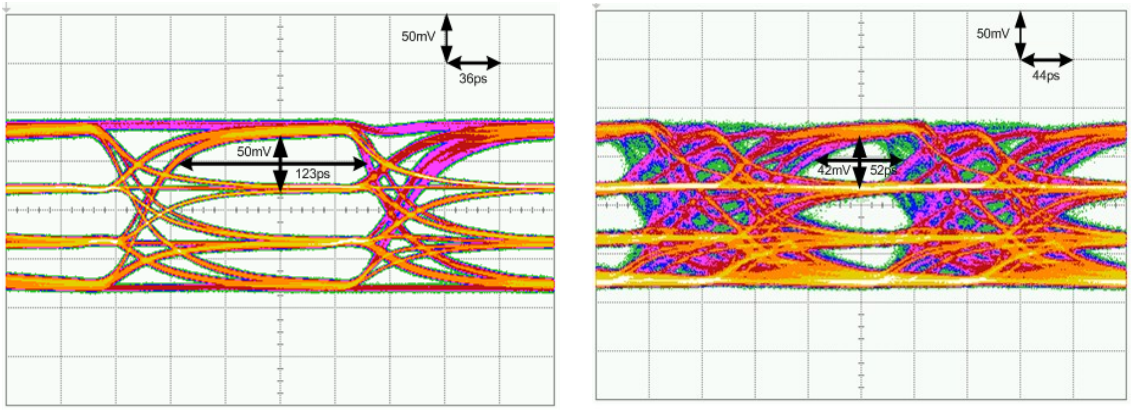
Also in the long channel case, the relationships between those losses are like this: $\beta_2 - \beta_1 < 6$ dB, $\beta_1 - \beta_0 < 3.54$ dB and $\beta_2 - \beta_0 < 9.54$ dB. Therefore the eye opening margin of PAM-2 is the best, and Duobinary and PAM-4 follows in this order. This results are not surprised at all, because the used channel losses are not overly steep and

linear. Therefore it is expected that PAM-2 provides an advantage over Duobinary and PAM-4 modulations.



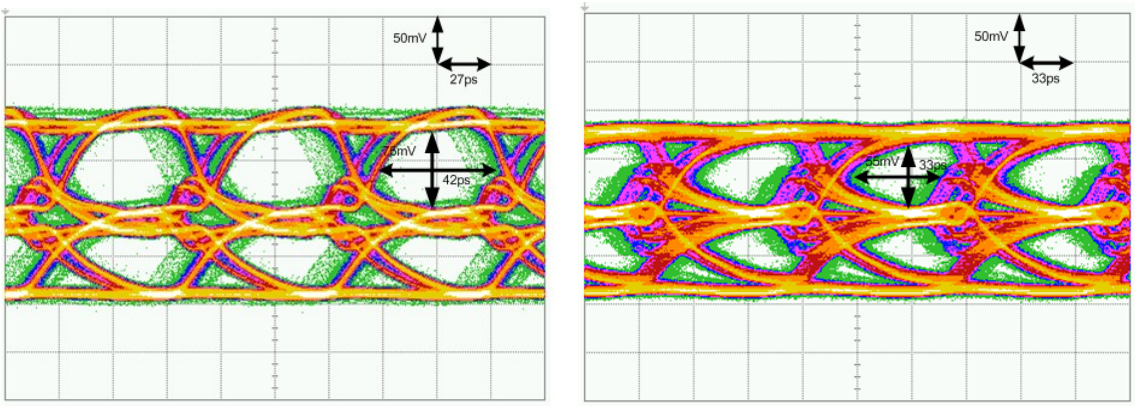
(a) (b)

Fig. 3.28. (a) 12.5Gb/s PAM-2 eye diagram with short channel, and (b) 10Gb/s PAM-2 eye diagram with long channel



(a) (b)

Fig. 3.29. (a) 12.5Gb/s PAM-4 eye diagram with short channel, and (b) 10Gb/s PAM-4 eye diagram with long channel



(a) (b)

Fig. 3.30. (a) 12.5Gb/s Duobinary eye diagram with short channel, and (b) 10Gb/s Duobinary eye diagram with long channel

Relative to the work of [7], which implemented three separate transmitters to compare the different modulation schemes, the presented work allows for the efficient implementation of the three modulation schemes in a single design. While there is some additional power overhead in the presented PAM-2 design relative to a design optimized only for PAM-2, significant power savings are achieved in PAM-4 mode due to the reduced clock speed. When comparing the duobinary-only transmitters of [5], [28] with the presented triple-mode work, the efficient quarter-rate precoder implementation allows for low voltage operation and comparable performance to the 20Gb/s design of [5] and improved power efficiency relative to the 12Gb/s design of [28]. Implementing this triple-mode design in a 1V 90nm process allows for lower power relative to the PAM-2 only design of [30] which was implemented in a 0.13µm process.

Table 3.7. Test results.

Short channel (4.5”) 12.5Gbps	Long channel (14”) 10Gbps
PAM-2 [apre,amain,apost] = [-0.0406 0.8041 -0.1553] [E_Width, E_Height] = [63ps, 110mV] β_2 = 7.6 at 6.25G	PAM-2 [apre,amain,apost] = [-0.029 0.7823 -0.1887] [E_Width, E_Height] = [55ps, 100mV] β_2 = 14.6 at 5G
Duobianry [apre,amain,apost] = [0.4971 0.3546 -0.148] [E_Width, E_Height] = [42ps, 75mV] β_1 = 6.22 at 4.17G	Duobinary [apre,amain,apost] = [0.5015 0.3624 -0.1362] [E_Width , H_Hight] = [33ps, 55mV] β_1 = 12.2 at 3.3G
PAM-4 [apre,amain,apost] = [-0.0285 0.924 -0.0475] [E_Width, E_Height] = [123ps, 50mV] β_0 = 4.8 at 3.125G	PAM-4 [apre,amain,apost] = [-0.0227 0.9141 -0.0632] [E_Width, E_Height] = [52ps, 42mV] β_0 = 9.7 at 2.5G
$\beta_2 - \beta_1 < 6$ dB $\beta_1 - \beta_0 < 3.54$ dB $\beta_2 - \beta_0 < 9.54$ dB	$\beta_2 - \beta_1 < 6$ dB $\beta_1 - \beta_0 < 3.54$ dB $\beta_2 - \beta_0 < 9.54$ dB

III.6. Summary

This chapter has reviewed the three common high-speed serial I/O modulation formats and discussed a triple-mode transmitter capable of efficiently implementing them up to 20Gb/s. The optimal modulation format for maximum eye margins is a function of the channel loss profile, crosstalk, random noise, and jitter. Comparing the modulation schemes at an effective Nyquist frequency predicts that for best eye height, PAM-2 should be used for low-loss channels, PAM-4 for high-loss channels with a steep

loss slope, and duobinary for high-loss channels with more gradual slopes. As transient simulations are not feasible to accurately predict link performance at the necessary low system bit-error rates, a statistical link model is developed to compare the three modulation formats. This statistical model confirms the channel loss profile guidelines and also allows for rapid exploration of trade-offs in equalization complexity and sensitivity to crosstalk and jitter. The presented triple-mode transmitter utilizes a quarter-rate duobinary precoder circuit that allows for improved timing margin, which translates into reduced power consumption at a low 1V supply.

This transmitter provides a high degree of flexibility to support different channel environments and, for a given platform, the ability to scale to high data rates during periods of peak I/O bandwidth demand.

IV. RECEIVE-SIDE NEAR-END AND FAR-END CROSSTALK CANCELLATION CIRCUITRY [3]

IV.1. Introduction

Serial I/O data rates are currently surging in order to support the increase in mobile communication and cloud computing bandwidth requirements. At data rates at or above 10Gb/s, both intersymbol interference (ISI) due to channel frequency-dependent loss and crosstalk interference due to multi-channel coupling must be considered in order to ensure adequate system bit-error rate (BER) [33], [34]. While equalizers are effective in cancelling ISI, topologies such as receive-side FIR filters [35, 36] and continuous-time linear equalizers (CLTLE) [37], [38] don't improve the signal-to-crosstalk ratio, motivating the use of dedicated crosstalk cancellation circuitry.

As shown in Fig. 4.1, crosstalk is typically classified as near-end crosstalk (NEXT), where an aggressor signal couples to a victim signal on the same channel side, and as far-end crosstalk (FEXT), where an aggressor signal couples to a victim signal traveling in the same direction to the far side of the channel. Both NEXT and FEXT occur at points along the channel where isolation is degraded, such as the chip packages and connectors between boards [39], [40]. In addition, FEXT also occurs due to high-density parallel routing of multiple channels between chips [41].

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3 . Reprinted with permission from "10 Gb/s Adaptive Receive-Side Near-End and Far-End Crosstalk Cancellation Circuitry" by Byungho Min, Noah HaeWoong Yang, Samuel Palermo, 2014, IEEE International Midwest Symposium on Circuits and Systems, pp. 77-80, Copyright 2014 IEEE

An effective approach to cancel NEXT involves passing the known aggressor transmit data through an FIR filter to sum with the incoming signal at the victim receiver, with both analog [6], [7] and digital FIR implementations reported previously [56]. One key limitation of this approach is that the NEXT signal is only canceled out to the span of the FIR filter, leading to relatively long 5-7 tap implementations [6], [7], [56]. In order to cancel additional long-tail NEXT, [7] introduced a parallel continuous-time pole-zero filter which was manually tuned to match a given channel environment. However, in order to seamlessly support operation with different channels and allow for robustness to variations in process, voltage, and temperature, adaptive tuning of all the filter coefficients, both FIR and continuous-time, is required.

It is possible to cancel FEXT at the transmit-side where both the aggressor and victim data is known, with approaches being proposed that include utilizing digital filters to generate inverse pulses [43]-[46], signal mode detection for delay adjustment [47], [48], and channel delay staggering with eye-center glitch cancellation [49]. However, one limitation of transmit-side FEXT cancellation is that the crosstalk impact at the victim receiver is not directly known, which necessitates the overhead of a back-channel to implement adaptive tuning schemes [46]. At the receiver side, FEXT cancellation schemes include passing the aggressor signal through a high-pass filter which acts as a differentiator to emulate the FEXT signal [9], [24], [50], [57] and signal mode detection for lumped coupling capacitance adjustment [51]. With receive-side cancellation, the FEXT impact can be directly detected at the victim receiver and used to adapt the

crosstalk cancellation circuitry, with mode-detection clock-and-data recovery [51] and power detection schemes being proposed [46].

For systems where both NEXT and FEXT exist, efficient merged NEXT/FEXT cancellation schemes are required which allow for simultaneous operation and independent adaptation to ensure robust operation. This paper presents receive-side circuitry which merges the cancellation of NEXT and FEXT and can automatically adapt to different channel environments and variations in process, voltage, and temperature [52]. Chapter IV.2 gives an overview of the proposed receive-side adaptive NEXT/FEXT cancellation circuitry, which also includes a continuous-time linear equalizer to compensate for channel loss without masking the crosstalk cancellation impact. The adaptive NEXT cancellation scheme, which utilizes a novel 3-tap FIR filter which combines two traditional FIR filter taps and a continuous-time band-pass filter IIR tap for efficient long-tail crosstalk cancellation, is detailed in chapter IV.3. Chapter IV.4 discusses the FEXT cancellation scheme which couples the aggressor signal through a differentiator circuit whose gain is automatically adjusted with a power-detection-based adaptation loop. Experimental results of the merged crosstalk cancellation system, fabricated in a GP 65nm CMOS process, are shown in Chapter IV.5. Finally, chapter IV.6 concludes the chapter.

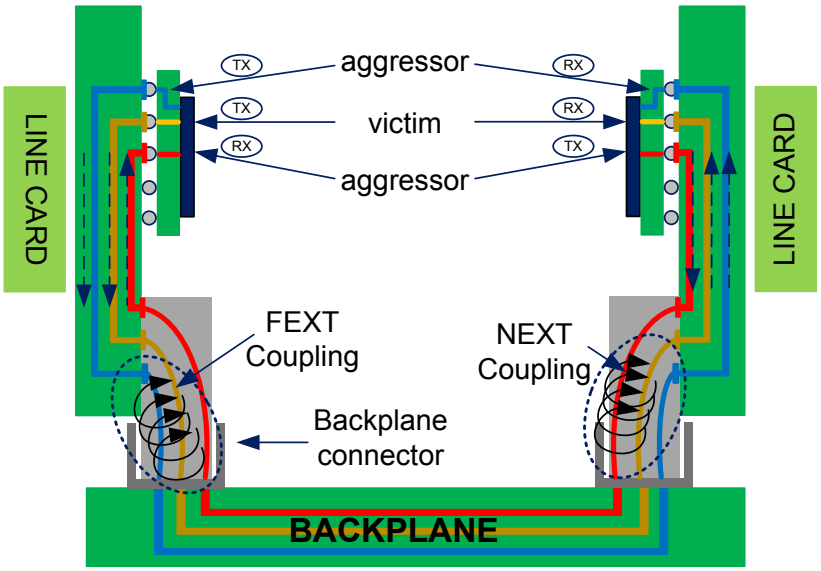


Fig. 4.1. NEXT and FEXT crosstalk in a backplane channel environment.

IV.2. NEXT/FEXT Cancellation System Architecture

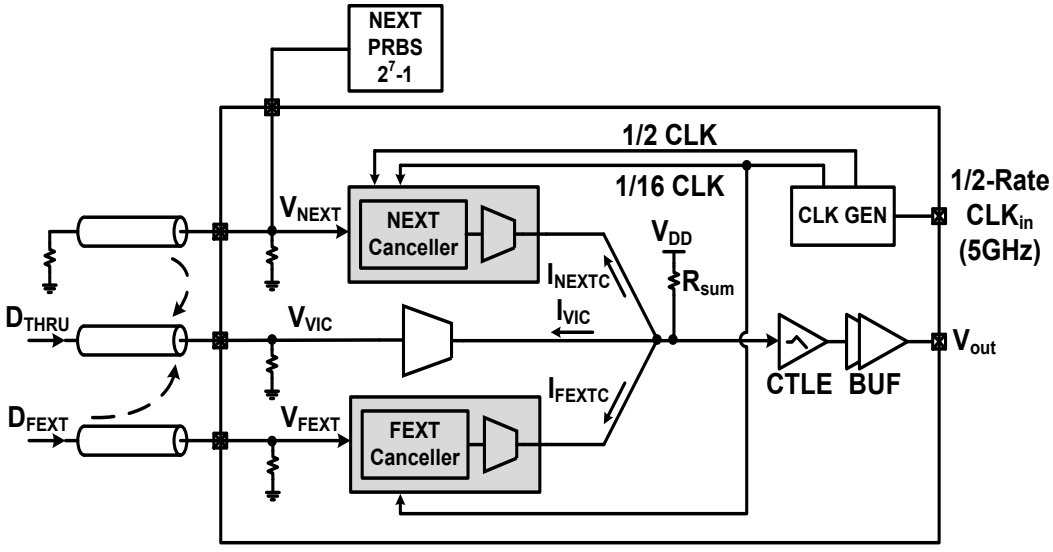


Fig. 4.2. Receive-side adaptive NEXT and FEXT cancellation circuitry.

Fig. 4.2 shows a block diagram of the proposed receive-side adaptive NEXT and

FEXT cancellation circuitry. The victim data signal, V_{VIC}, which includes both FEXT and NEXT coupled from adjacent channels, passes through a transconductance buffer stage that feeds a current-mode summer where both NEXT and FEXT are cancelled. In order to generate the NEXT cancellation current, the known aggressor transmitter data passes through a novel 3-tap FIR filter which combines two traditional FIR filter taps and a continuous-time band-pass filter IIR tap for efficient long-tail crosstalk cancellation. FEXT cancellation is generated by passing the parallel received FEXT signal, V_{FEXT}, through an un-clocked adaptive-gain differentiator circuit. The adaptation of the NEXT and FEXT filters is performed at a rate equal to 1/16 the 10Gb/s data rate, with the 625MHz clocks produced by a clock generation block that divides an external 5GHz half-rate clock by eight. This 5GHz clock is also buffered and used to synchronize the 10Gb/s aggressor data passing through the NEXT filter. In a complete transceiver system, this half-rate 5GHz clock would be supplied by the local NEXT aggressor transmitter. Note that this does not require the NEXT and FEXT aggressors to be synchronous, as the 1/16-rate clock is only used for FEXT filter adaptation and during normal operation the FEXT cancellation filter is not clocked. A CTLE follows to cancel the through-channel ISI without distorting the effectiveness of the cross-talk cancellation circuitry. Finally, a 50Ω output buffer drives the equalized signal off-chip.

The crosstalk-cancellation circuitry has two modes of operation, data transfer and crosstalk cancellation adaptation mode [24], [42], [46]. During crosstalk cancellation adaptation mode, the NEXT and FEXT cancellation circuitry are tuned sequentially. The NEXT cancellation filter is first calibrated by activating the aggressor transmitter to

drive data onto the channel, while both the victim and FEXT signals are deactivated. Sampling the summer output under this condition provides information to drive a sign-sign least-mean squared (LMS) adaptation loop that sets both the FIR and continuous-time NEXT filter tap coefficients. The FEXT cancellation filter is then calibrated by activating the aggressor transmitter at the far-end to drive data onto the channel, while both the victim and NEXT signals are deactivated. Under this condition, a rectifying power detector circuit compares the victim signal with the FEXT aggressor signal passed through a passive RC differentiator, which emulates the FEXT obtained along the channel. The obtained error signal is used to adjust a digitally-controlled capacitor bank to set the powers of the FEXT emulation signal equal to the FEXT coupled onto the victim signal. Data transfer mode is activated after the crosstalk cancellation circuitry has been calibrated, with the NEXT and FEXT cancellation control codes frozen. Note that, as the crosstalk cancellation adaptation is done in the foreground, both the NEXT and FEXT cancellation filter settings must be periodically retrained to compensate for temperature and voltage variations. Thus, it is important that the adaptation procedure quickly converge. Adapting at a 1/16 clock rate provides a reasonable balance between convergence time and power and area consumption of the adaptation logic.

IV.2.1. Channel Model

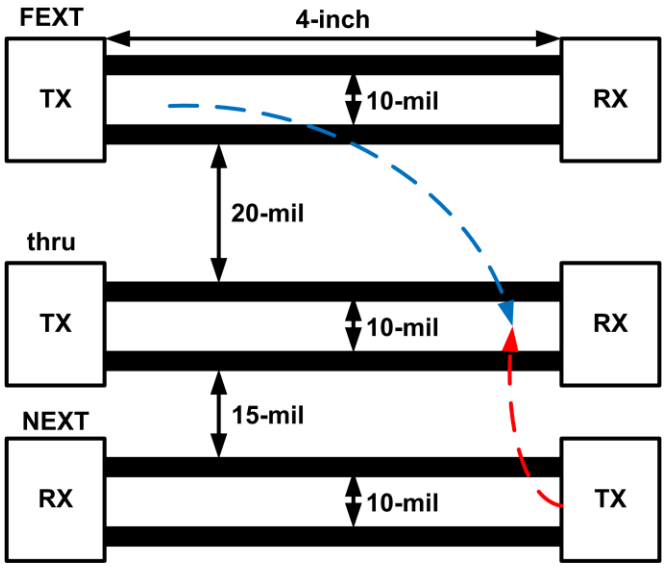


Fig. 4.3. Channel environment

Fig. 4.3 shows the differential channel environment which is fabricated on FR4 PCB. The thru, NEXT, and FEXT channel responses are shown in Fig. 4.4. The thru channel is 4-inch long copper lane, and spacing is 10-mil, which has 7.3dB loss at 5GHz.

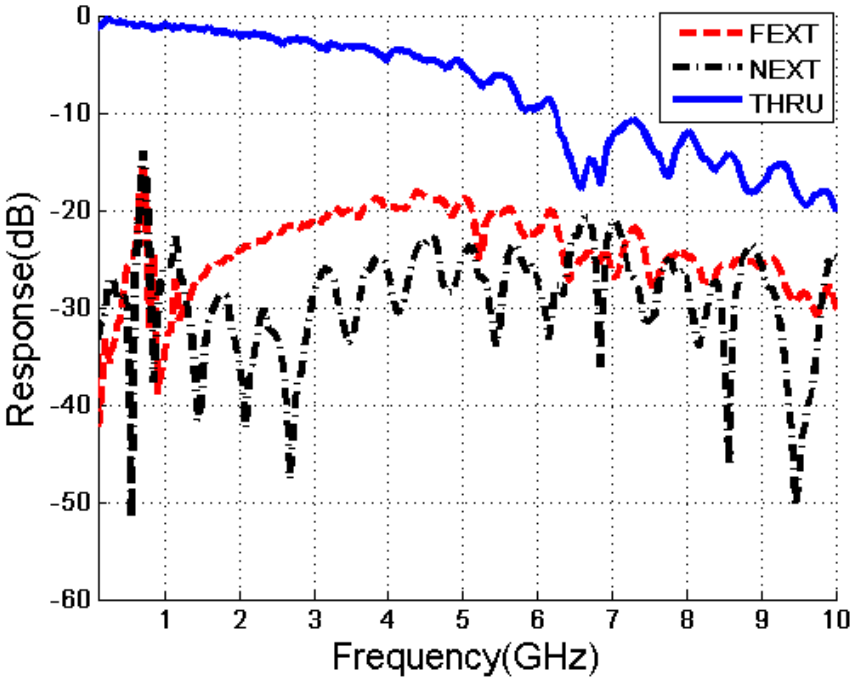


Fig. 4.4. Channel response

The NEXT channel is 15-mil away from the thru channel, and has 27.7dB loss at 5GHz. The FEXT channel is 20-mil away from the thru channel, and has 21dB loss at 5GHz. A single channel is 5.8-mil wide to be matched to 50-ohm in this FR4 PCB dielectric material. The thru channel response shows the large dip around 6~7GHz, because the thru channel has strong coupling with two adjacent channels, which loses whole energy in the thru channel to the adjacent channels in this frequency range.

IV.2.2. Clock Distribution

Fig. 4.5 shows the clock distribution network. It consists of input clock network and clock delay parts to make various clocks. Differential clock inputs are applied to the

CML-to-CMOS clock buffer circuitry, and this clock is connected to two clock networks for NEXT and FEXT canceller blocks. As mentioned earlier, clock division factors of 1

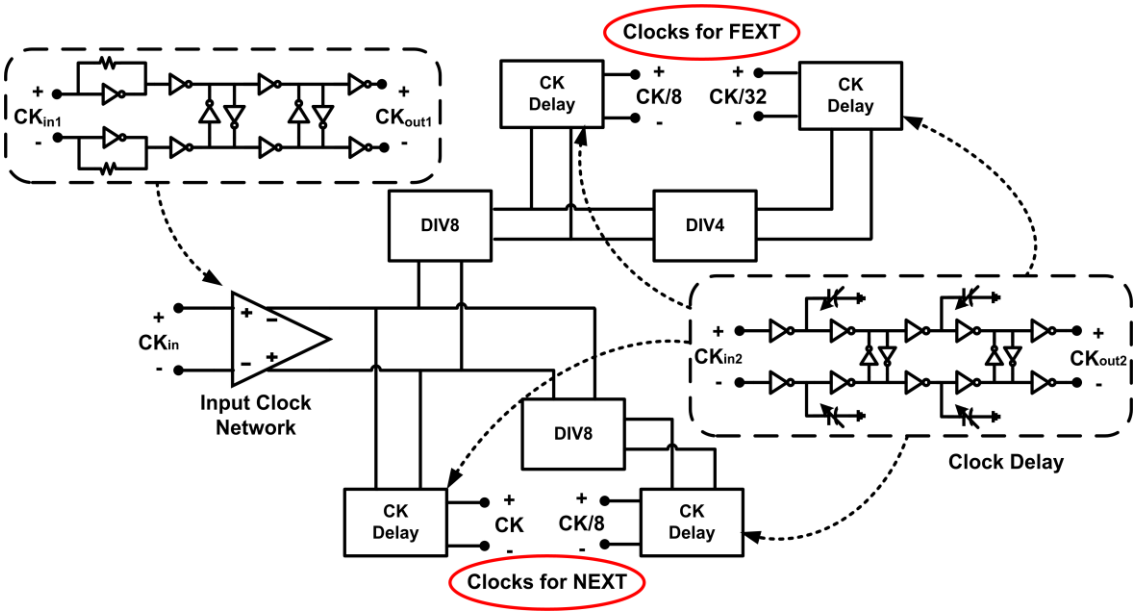


Fig. 4.5. Clock distribution

and 8 for the NEXT canceller, and factors of 8 and 32 for FEXT canceller are required. Each clock delay block can control the time delay relative to input clock CK using two 2-bit capacitor banks.

IV.2.3. CTLE & Buffer

Fig. 4.6 (a) shows the continuous-time linear equalizer and output buffer stages used to compensate for channel loss and drive the controlled impedance output channel for high-speed eye diagram measurements. A CTLE is chosen as the sole equalizer block because it provides the same transfer function to the desired signal and the crosstalk

aggressors, thus enabling an accurate characterization of the crosstalk cancellation circuitry's effectiveness. This is in contrast to a decision-feedback equalizer (DFE) [24], [57], which will only cancel ISI and not propagate any crosstalk signal if a correct decision is made. The CTLE provides a zero-pole response, along with a secondary output pole, in order to implement high-frequency peaking up to the 5GHz Nyquist frequency. The transfer function of CTLE is

$$H(S) = \frac{A_p(s + w_z)}{(s + w_{p1})(s + w_{p2})} \tag{4-1}$$

where

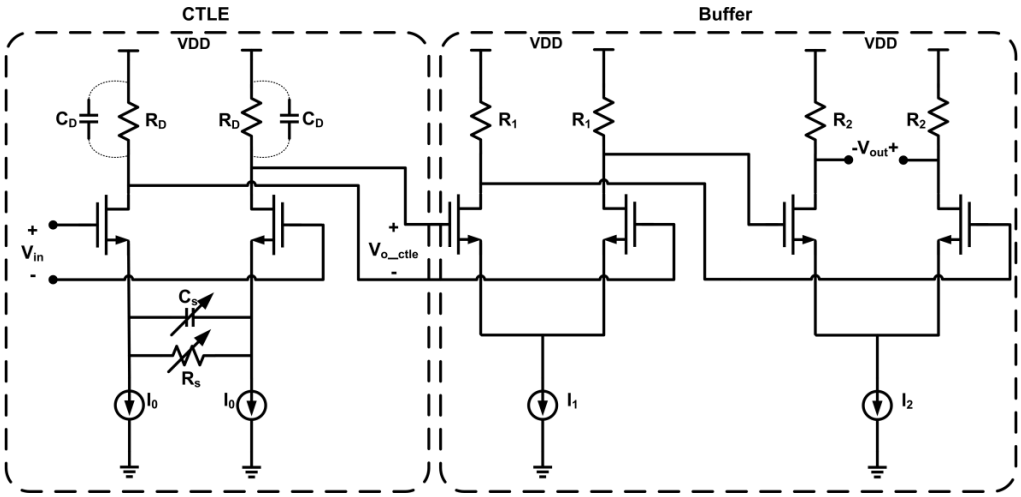
$$A_p = {g_m}/{C_D}$$

$$w_z = {1}/{R_s C_s}$$

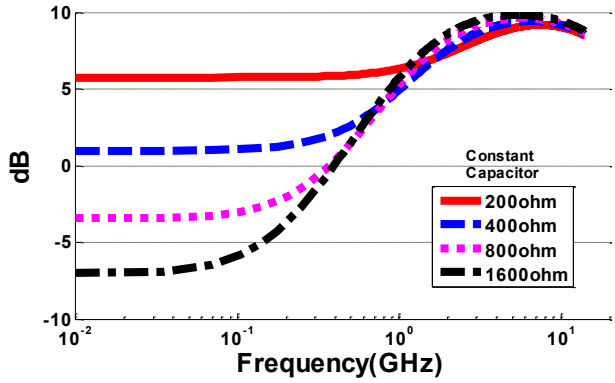
$$w_{p1} = (1 + g_m R_s/2)/R_s C_s$$

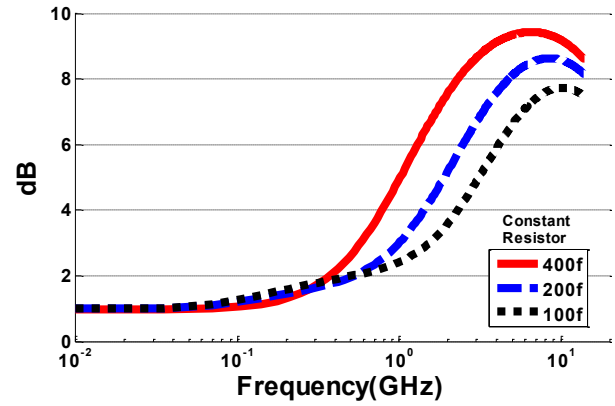
$$w_{p2} = {1}/{R_D C_D}$$

R_s and C_s are source degeneration resistor and capacitor, and R_D and C_D are loading resistor and capacitor respectively. g_m is the transconductance of the input transistor, and



(a)





(b)

Fig. 4.6. (a) CTLE & Buffer schematic, and (b) CTLE simulation results

A_p is the DC gain of the CTLE stage [1]. It is designed to compensate high frequency loss of thru channel at 5GHz (~7dB). The CTLE stage provides wide selective bandwidth of (~3.85 GHz) and various gains from -7.3dB to 10.5dB according to the R and C values shown in Fig. 4.6 (b). The CML buffer with 400mV_{pp} output swing is followed, which consists of two cascaded CML-based inverters, where the last inverter has 50 ohm load for matching to the output load.

IV.3. Proposed NEXT Architecture

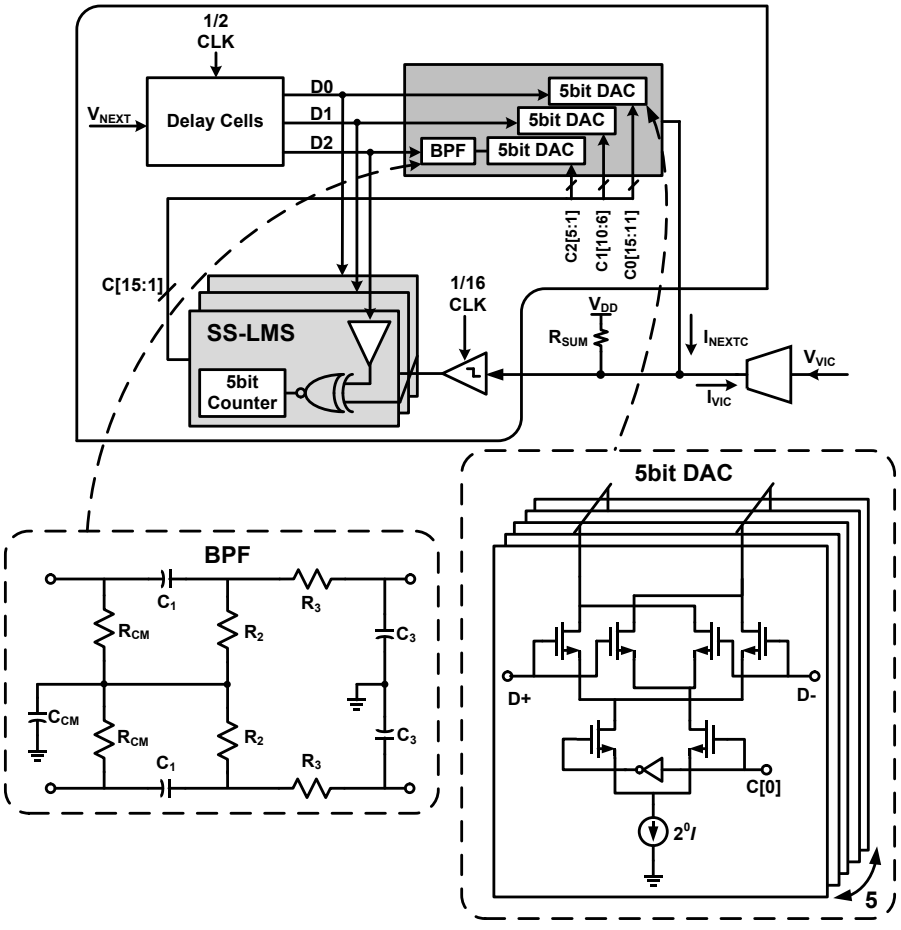


Fig. 4.7. Adaptive NEXT cancellation filter.

NEXT cancellation is achieved with the 3-tap FIR filter shown in Fig. 4.7. In the implemented prototype, 10Gb/s NEXT aggressor data is generated with an external transmitter module. As mentioned previously, the NEXT canceller has two operating modes: 1) adaptation to interference mode, and 2) data transfer mode. In the adaptation mode, the current and delayed data are applied to the SS-LMS block operating at CK/8 to calculate FIR coefficients using three 5-bit digital-to-analog converters (DACs). SS-LMS algorithm is based on the following equations [18].

$$y(n) = D_{NEXT}(n)w(n) \tag{4-2}$$

$$e(n) = d(n) - y(n) \tag{4-3}$$

$$w(n+1) = w(n) + \mu \cdot u(n) \cdot e(n) \tag{4-4}$$

where $D_{NEXT}(n)$ is the input data to cause NEXT interference into the adjacent channel, d(n) is the NEXT interference, y(n) is the emulated output, e(n) is the difference between interference and emulated output, μ is the step size, and w(n) is the filter coefficients. All coefficients are proper arrays based on these equations.

The SS-LMS block operating at CK/8 clock is implemented as shown in Fig. 4.7. Three data inputs, $D_{NEXT}(n)$, $D_{NEXT}(n-1)$ and $D_{NEXT}(n-2)$, are captured at the falling edge of CK/8. The d(n)-y(n) is also captured at the same falling edge as shown in Fig. 4.8, and it is decided whether d(n) or y(n) is larger. Then, new coefficients are updated at the next rising edge of CK/8 for the three DACs. Therefore CK/8 can be used in this work instead of a full data rate clock [2xCK], and hence the power consumption of the NEXT canceller can be dramatically reduced with this modification [1].

During the calibration step, the NEXT canceller keeps trying to find coefficients which make the difference between the NEXT interference and the mimicked interference close to zero. After the calibration step, the operating mode changes into the data transfer mode manually. The mimicked signal is negatively summed at the current-mode summer with thru-data including the NEXT interference, which results in the cancellation of the NEXT interference.

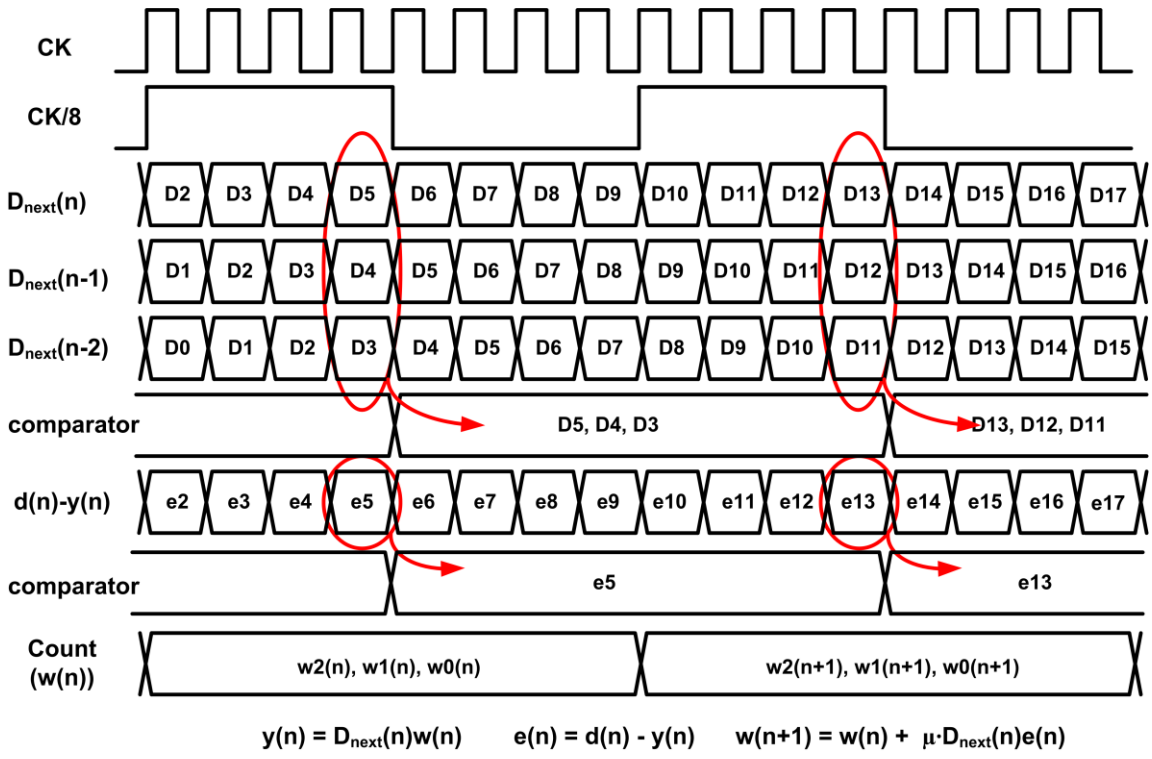


Fig. 4.8. Timing Diagram for SS-LMS algorithm

IV.3.1. Input Delay Cell

Input block which has 4-current-mode-logic (CML) latches and 2-muxes in Fig. 4.9 operates at half-data rate frequency clock to capture data instead of using full-data rate frequency clock to save power consumption and relax the complexity of hardware. With using input data denoted by $D_{NEXT}[n]$, it generates $D_{NEXT}[n-1]$ and $D_{NEXT}[n-2]$ which are one- and two-clock delayed NEXT data respectively. These data are applied to the counter and the DAC to mimic the NEXT interference.

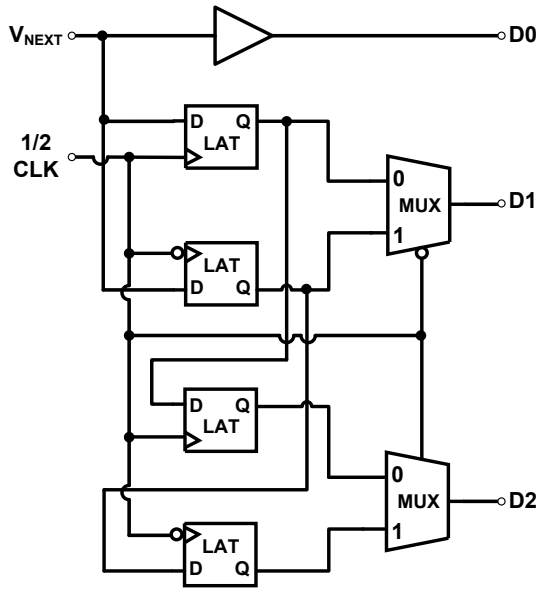


Fig. 4.9. NEXT cancellation filter input retiming block.

IV.3.2. DAC & Band Pass Filter

Three 5bit-dac and band-pass filter (BPF) in Fig. 4.7 are designed to closely emulate

the NEXT interference. The mimicked signal is directly fed back to the output node of the summer to avoid the non-linear summation at the summer, where thru-data including NEXT interference is applied as it is shown in Fig. 4.7. Three 5bit coefficients are converged after being calibrated in Fig. 4.10. The simulation results show that the three filter taps converge within 2000 iterations or 3.2μs for 10Gb/s operation.

Fifteen coefficients from the counter are connected to each DAC to control the amount of currents, and 5bits of them respond to one coefficient of data such as $D_{NEXT}[n]$, $D_{NEXT}[n-1]$, and $D_{NEXT}[n-2]$. The DAC is binary-weighted current-steering structure which is Gilbert-cell topology. The first and second data from the previous block are directly connected to the DACs, but the last input $D_{NEXT}[n-2]$ is connected through band- pass filter (BPF) which has quality factor (~2.4), center frequency

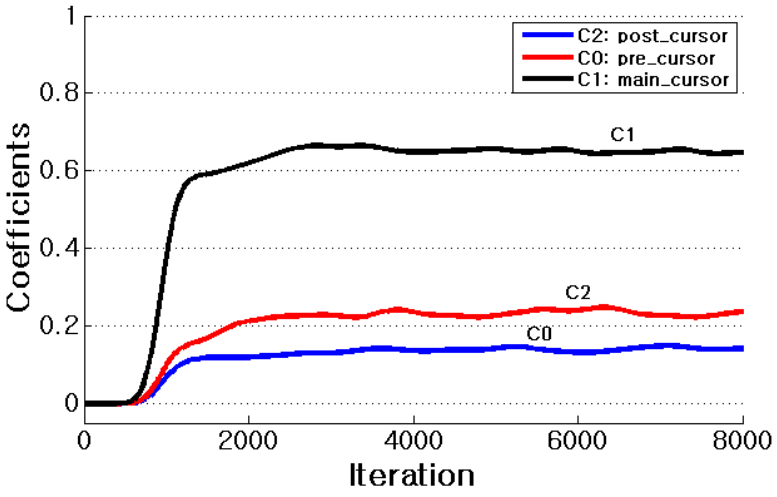
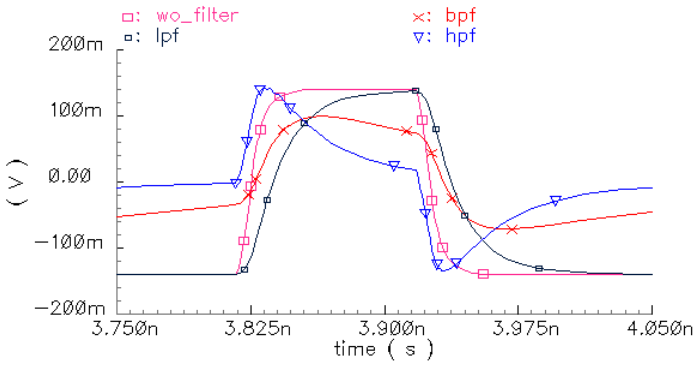


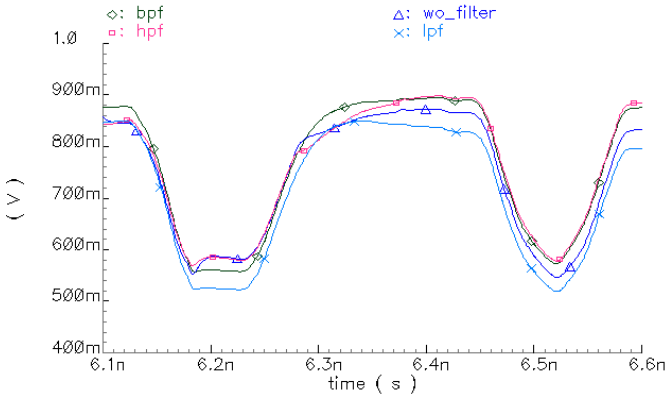
Fig. 4.10. NEXT cancellation filter coefficients convergence behavior with the SS-LMS adaptation loop.

(~4.8GHz) and bandwidth (~2GHz) to easily adapt the NEXT characteristic that is band-pass filter . The BPF is designed with LPF and HPF serially connected based on the basic filter concept in Fig. 9. The simulations with other cases such as LPF, HPF, and without a filter are shown in Fig. 4.11. Fig. 4.11(a) shows the inputs to the DAC using various filters in order to reshape them to emulate the NEXT interference closely. Each input has different rise time, and different shapes according to the filters. The rise time is 12ps with HPF, 17ps with BPF, 22ps with LPF, and 15ps with wo_filter, and these reshaped signals drive the DAC. As it is shown in Fig. 4.11(b), the output signal using BPF is the horizontally and vertically widest and flattest after the NEXT interference is cancelled. But the simulation results using HPF show more slanted output because the reshaped input signal has mostly high frequency components.

In case of LPF, the output has also slope which makes the eye-diagram smaller, because the input signal has the largest rise time fall time. The case without any filters makes output the smallest one vertically and horizontally, because both rise and fall times are too steep to emulate the NEXT interference comparing to other cases. Fig. 4.12 shows the eye-diagrams of all cases. It shows [H,W] is [359mV, 55ps] without using any filter, [H,W] = [426mV, 63ps] for using BPF, [H,W] = [369mV, 61ps] for using HFP, and [H,W] = [367mV, 53ps] for using LFP. Therefore, when the shaped signal using BPF drives one of DACs, it can make a healthy eye-diagram as shown in Fig. 4.12.



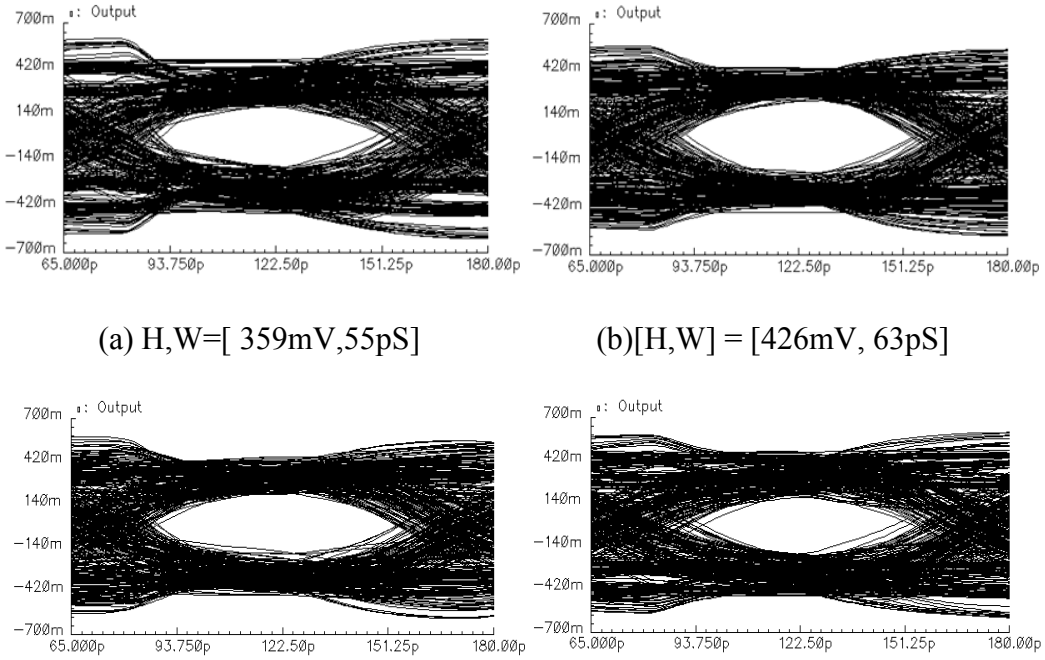
(a)



(b)

Fig. 4.11. (a) Inputs to DAC, and (b) Outputs after noise cancellation

Eye-Height is increased by 18.6%, and eye-width is increased by 14.5% comparing to the wo_filter case. These results coincide with the simulation results in Fig. 4.11. Relative to a simple symbol-spaced 3-tap FIR filter, including the bandpass filter in the third tap allows for a more complex pulse response with a longer tail to better compensate for NEXT crosstalk after the third tap.



(a) H,W=[359mV,55pS] (b)[H,W] = [426mV, 63pS]

(c)[H,W] = [369mV, 61pS] (d)[H,W] = [367mV, 53pS]

Fig. 4.12. Eye diagram of (a) without filter, (b) with BPF, (c) with HFP, and (d) with LFP

The 10Gb/s simulation results of Fig. 4.13, which utilize measured s-parameter models of the NEXT/FEXT testbench consisting of three 4" differential channels that is used in the experimental results of Chapter IV.5, show that employing the band-pass IIR tap offers 12% eye height and a slight eye width improvement relative to a traditional 3-tap FIR filter implementation. Also, the band-pass IIR tap performs superior to potential low-pass and high-pass IIR tap implementations.

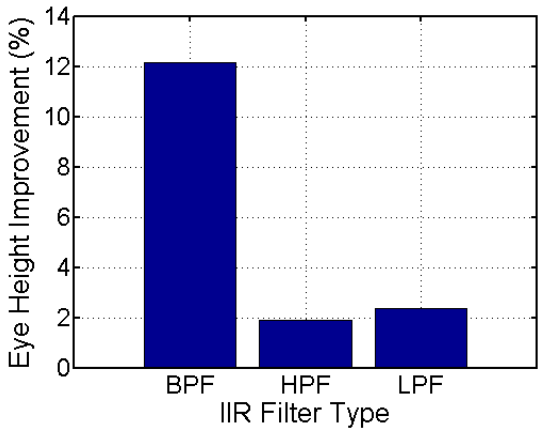


Fig. 4.13. 10Gb/s eye height improvement, relative to a traditional 3-tap FIR filter, by including an IIR tap.

IV.3.3. Comparator Block

Comparator block has 4 comparators and 3 xnors in Fig. 4.14. Each Comparator is low voltage strong arm latch structure [58]. The sense amplifier is connected to another latch to store the data firmly. All inputs, $D_{NEXT}(n)$, $D_{NEXT}(n-1)$, $D_{NEXT}(n-2)$ and feedback outputs, are connected to each comparator. The outputs of comparators regarding to $D_{NEXT}(n)$, $D_{NEXT}(n-1)$, and $D_{NEXT}(n-2)$ are xnored with the output of comparator regarding to *output(n)* like the below.

$$\overline{comp\left(D_{NEXT}(n)\right) \oplus comp(output(n))} \tag{4-5}$$

$$\overline{comp\left(D_{NEXT}(n-1)\right) \oplus comp(output(n))} \tag{4-6}$$

$$\overline{comp\left(D_{NEXT}(n-2)\right) \oplus comp(output(n))} \tag{4-7}$$

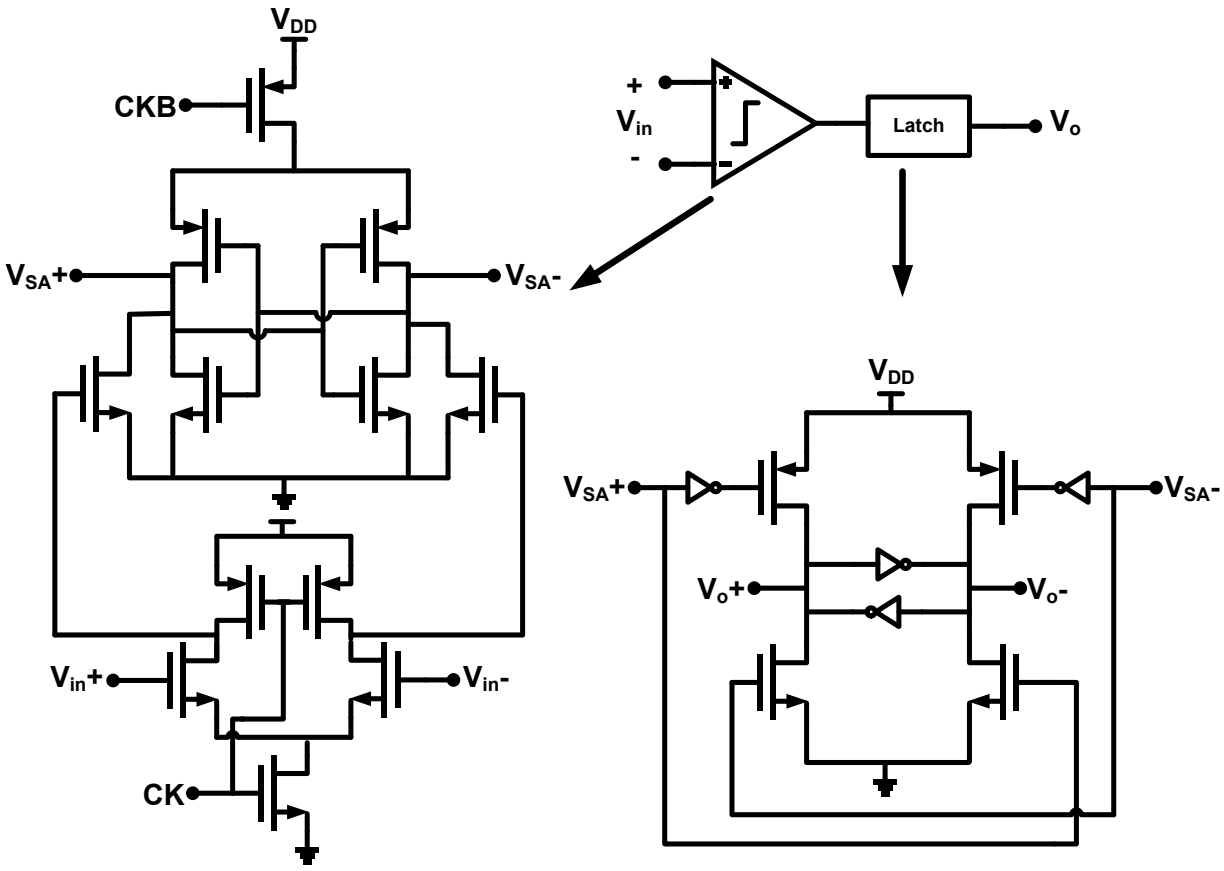


Fig. 4.14. Low-power dynamic comparator used in the NEXT and FEXT adaptation loop.

These signals control 5bit up-down counter respectively. If the signal is high, then the counter increases, and vice versa.

IV.3.4. Counter Block

Three 5bit counters are designed to handle the DACs as it is shown in Fig. 4.15. It can be reset at the beginning of the start, and the up-down signal decides the up-down direction of the counter according to the signal status of the previous block. This block is

designed with CMOS logic operating at CK/8, therefore it is relieved from timing margin and circuit complexity.

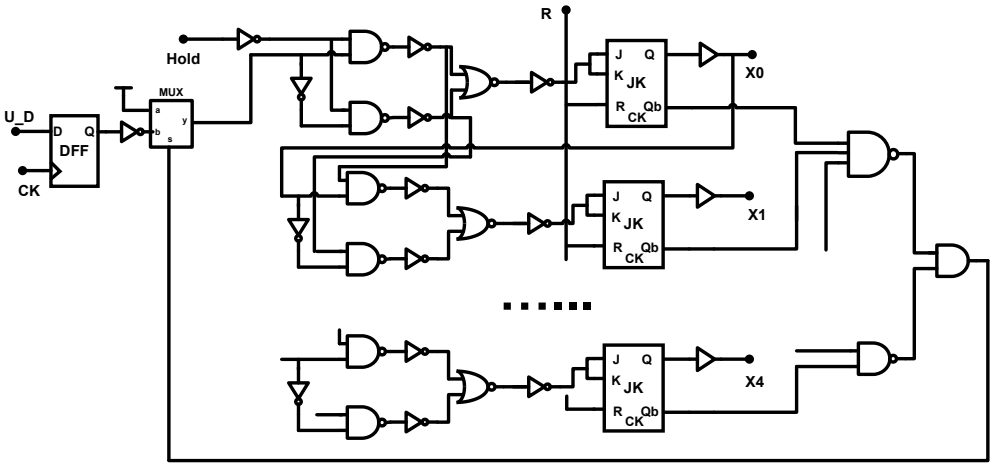


Fig. 4.15. 5bit counter

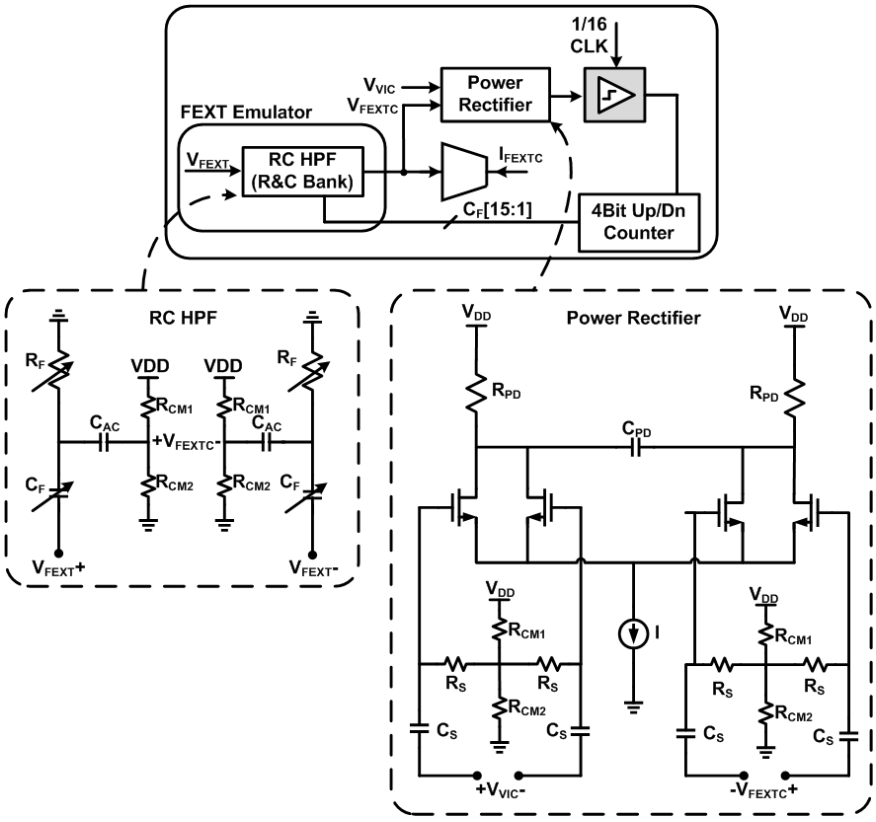


Fig. 4.16. FEXT canceller

IV.4. Proposed FEXT Architecture

Fig. 4.16 shows the FEXT cancellation circuitry, where the FEXT aggressor is passed through a tunable RC-highpass filter which acts as an adaptive-gain differentiator circuit to emulate the coupling that occurs on the victim channel. The high-pass filter pole frequency is adjustable from 2.7GHz to near 20GHz, with a 3-bit manually-controlled band-select resistor bank and a 4-bit adaptively-controlled capacitor bank. This emulated FEXT signal is AC-coupled to drive a current-mode output stage which is connected to

the shared crosstalk cancellation summer.

Adaptation of the FEXT cancellation filter is achieved by activating the aggressor transmitter at the far-end to drive data onto the channel, while both the victim and NEXT signals are deactivated. Under this condition, a rectifying power detector circuit compares the victim signal with the FEXT aggressor signal passed through the passive RC differentiator [21[, [46]. Similar to the NEXT cancellation, the power rectifier output is sampled with a 1/16-rate clock and the obtained error signal controls a 4-bit counter to adjust the digitally-controlled capacitor bank to set the powers of the FEXT emulation signal equal to the FEXT coupled onto the victim signal. Relative to tuning the differentiator gain in the current-mode [46], this method of tuning the RC values to adjust the FEXT emulation signal gain saves power and offers a more stable output common-mode for the shared crosstalk cancellation summer.

IV.4.1. RC Bank

RC Bank in Fig. 4.16 is designed for mimicking the FEXT interference [9]. RC bank can provide 105 different combinations of cutoff frequency from 2.65GHz to 19.8GHz with 170MHz resolution to cover the wideband frequency. The adaptive mechanism is to change the capacitor values according to the feedback signal from the power rectifier and comparison block. If the present signal power is greater than the previous, then C value decreases, and vice versa.

IV.4.2. Power Rectifier & Comparator

The emulated signal and FEXT interference are applied to the power comparison

block in Fig. 4.16 to compare each other and gives out the information about which one is greater. It extracts power of each signal through the high-pass filter structure (f_c > 3MHz), because FEXT interference has most of power in high frequency area. The Comparator following this power extraction block gives out the information about how closely the emulated FEXT follows the real FEXT interference controlling the following 4bit counter. When the FEXT interference and emulated FEXT get closer, comparator output will keep toggling around one point.

IV.4.3. Counter Block

The up-down signal of the preceding comparator controls the 4bit up-down counter in Fig. 4.17, and 4bit signals are decoded into 15bit thermometer codes in Fig. 4.18. These 15bit signals make the capacitors in the RC bank connect or disconnect to the V_{FEXT} data path with emulating the FEXT interference according to the up-down signal. When the two signals are coming closer, the counter keeps toggling around one point, which means that calibration is done in Fig. 4.19.

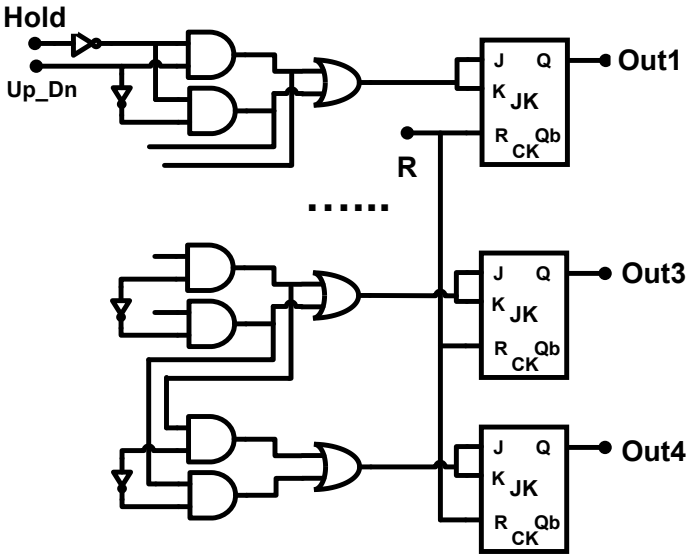


Fig. 4.17. 4bit counter

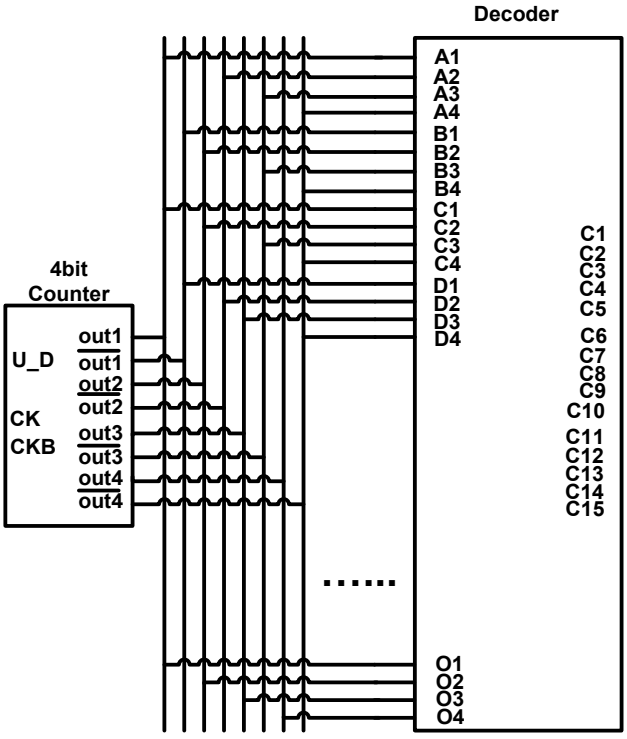


Fig. 4.18. Thermometer decoder

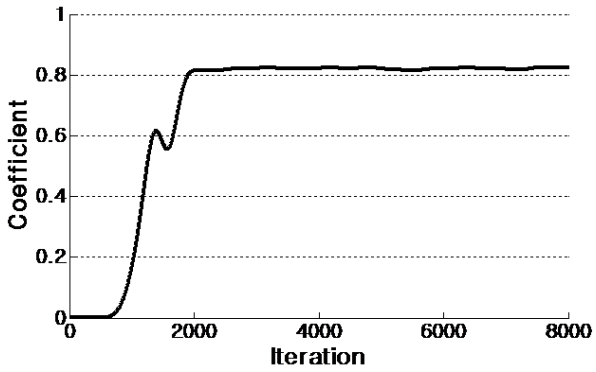


Fig. 4.19. FEXT cancellation filter digitally-controlled capacitor bank convergence behavior with the power-detection-based adaptation loop.

Utilizing the Fig. 4.16 testbench, the simulation results of Fig. 4.19 show that the capacitor code converges within 2000 iterations or 3.2μs for 10Gb/s operation. This allows for a potential sub-10μs retraining time for the combined NEXT and FEXT crosstalk cancellation filter settings.

IV.5. Experimental Results

Fig. 4.20 shows 10Gb/s 2^7-1 PRBS eye-diagrams with the 400mV$_{pp}$ driver output according to the functional modes of the cancellers. The eye-diagrams with before and after the calibration process are shown. The left two columns of Fig. 4.20 are the cases when cancellers are all turned off. In this case the eye height (H) and width (W) are [18mV, 23ps] and [4mV, 6ps] for NEXT and FEXT interferences respectively. The eyes are almost closed due to each interference. After the calibration process, the eye-diagrams are to be [88mV, 62ps] and [84mV, 60ps] due to the removal of interferences in the right two columns in Fig. 20. We can see that the NEXT and FEXT cancellers

improve the height and the width by [70mV, 39ps] and [80mV, 54ps] respectively. After each calibration, converged coefficients for each filter are acquired by each canceller's engine. When both cancellers are turned on, the eye-diagram is improved from [N.A, N.A] to [92mv, 58ps] in Fig. 4.20(c) with these converged coefficients. It clearly shows

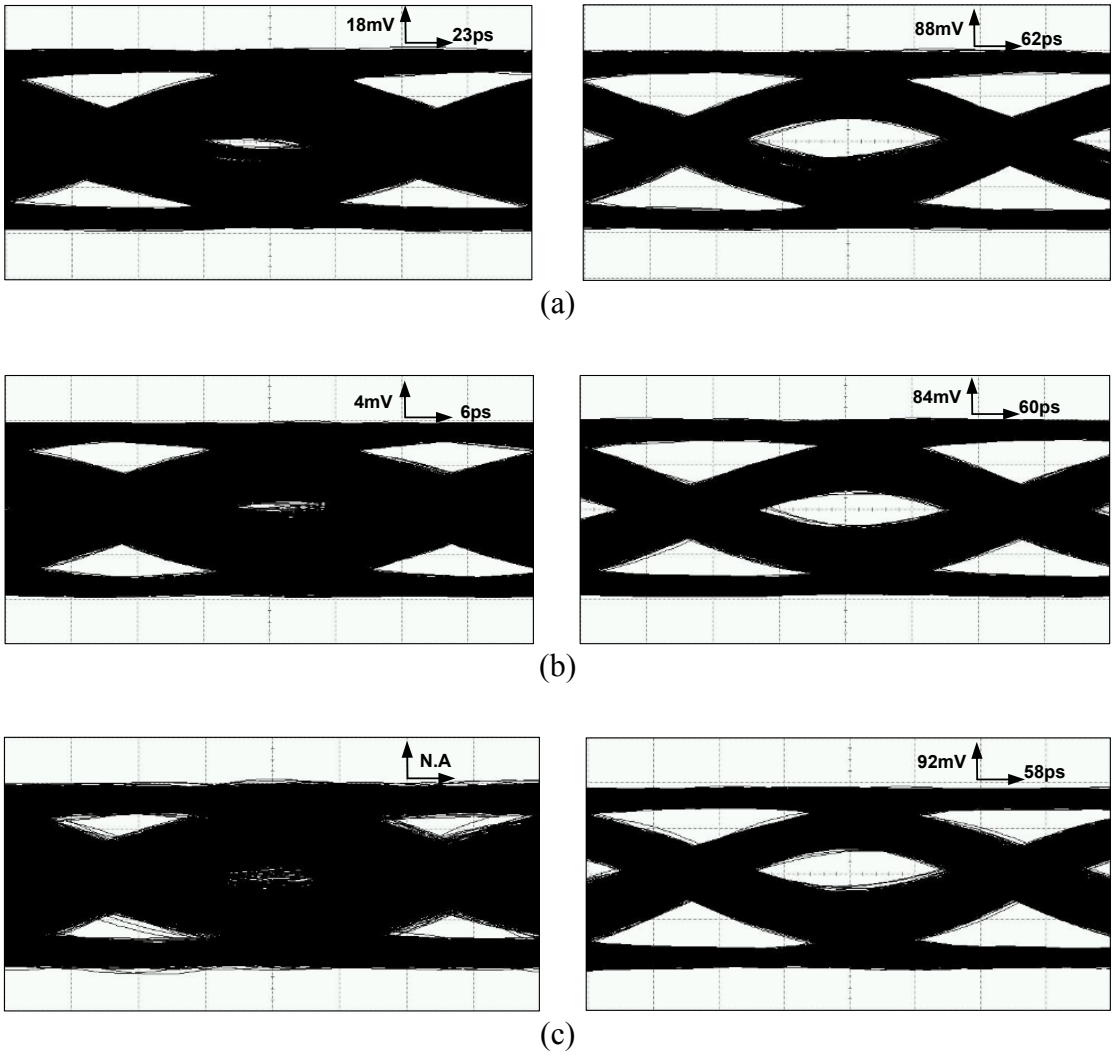


Fig. 4.20. Eye-diagrams of (a) NEXT canceller off vs. on (b) FEXT canceller off vs. on (c)Both cancellers off vs. on

that the eye-diagram is almost closed with turning the cancellers off, but enabling the NEXT and FEXT cancellers allows for a healthy eye-diagram close to the one without interferences. Fig. 4.21 shows bath-tub diagram according to three cases. When the noise cancellers are turned off, measured bathtubs touches at most up to 10e-2 at 10Gb/s. On the other hand, when the noise cancellers are turned on, it allows almost 0.2UI at 10e-10 BER. In case of No Crosstalks, it opens almost 0.3UI at 10e-10 BER.

The NEXT and FEXT canceller is fabricated in GP 65nm CMOS process in Fig. 4.22. Chip area including ESD diodes and decoupling capacitors is 0.84mm^2. If diodes and decoupling capacitors are not considered, the area is 0.3mm^2.

Performance summary is in the Table 4.1 and 4.2. The operating power of both NEXT and FEXT cancellers consumed to reduce both interferences and transfer thru data is 34.6mW. This value is the least one comparing to other distinguished papers. The general NEXT canceller is power hungry, but new architecture is designed to reduce power by utilizing half data rate clock [CK/2]. In the power breakdown of Table II, the NEXT canceller consumes most power due to the input delay block which is designed with CML structure.

In general NEXT canceller [56] has a feedback loop to adaptively calculate filter coefficients, but FEXT canceller [9] does not have it for adaptation. On the other hand this architecture has two feedback loops for adaptation techniques, which means this architecture can adapt unknown channels efficiently. It is the first paper which removes both interferences in one structure to the best of my knowledge.

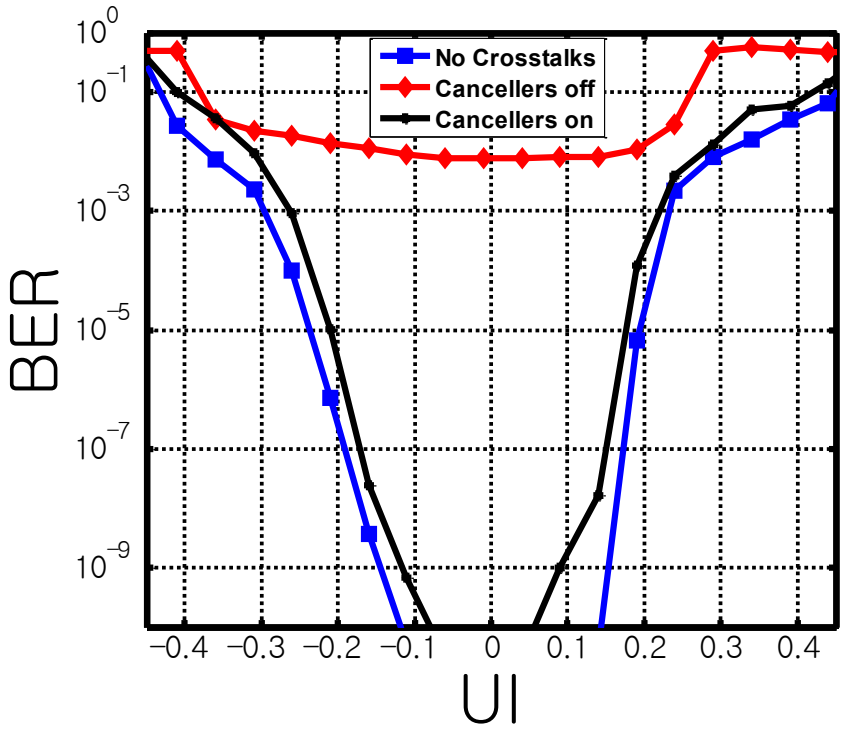


Fig. 4.21. Bath-tub plot

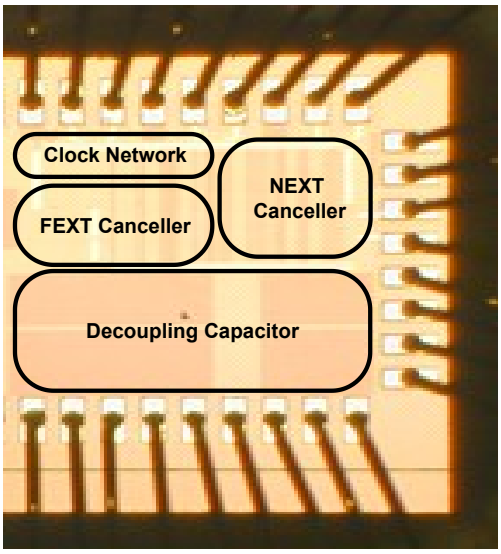


Fig. 4.22. Microphotograph of chip

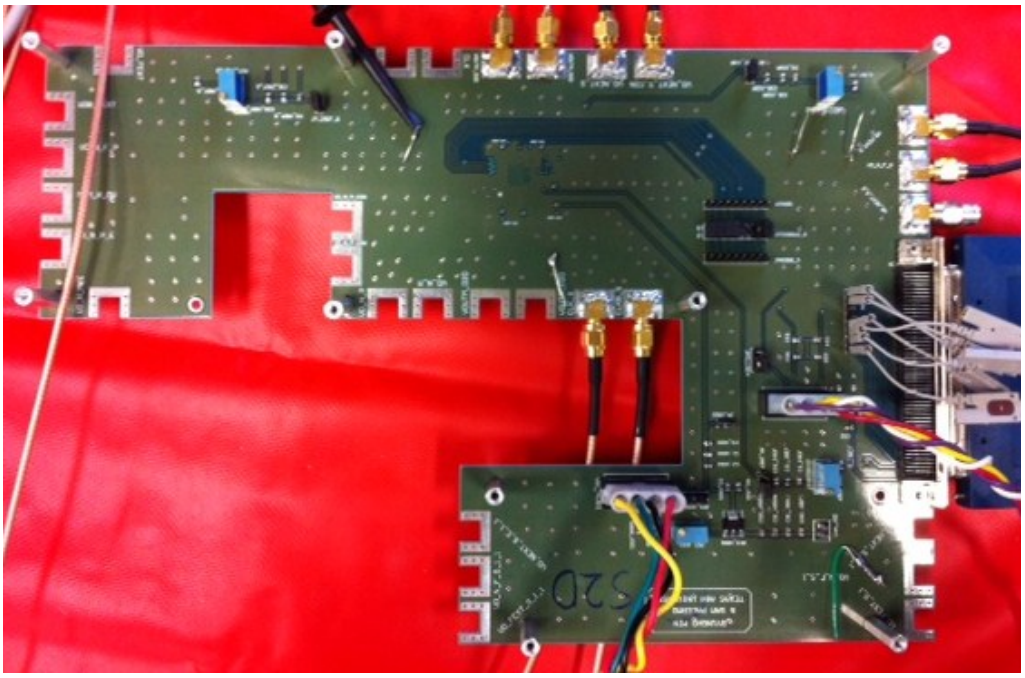


Fig. 4.23. PCB board

IV.6. Summary

This chapter presented a merged adaptive NEXT and FEXT canceller design technique. In the multi-channel link which experiences NEXT and FEXT interferences, both of them need to be dealt together. The NEXT and FEXT cancellers together are merged in one structure in order to reduce both NEXT and FEXT interferences. It is demonstrated that the NEXT canceller with BPF gives the healthiest eye-diagram comparing to other cases. Also it is power efficiently designed using a half-rate clock at input stage. The FEXT canceller also utilizes a feedback loop to adaptively accustom to unknown channels, which is designed with passive components. Therefore, this architecture can work in NEXT and FEXT interference environment.

Table 4.1. Performance comparison

	[1]		[4]		This Work		
Technology(nm)	130		130		65		
Supply Voltage(V)	1.2		1.1		1.1		
Data Rate(Gb/s)	5		12		10		
Channel Type(FR4)	·10 & 20 inch ·Width : 5-mil ·Spacing : 7-mil		·11 inch ·Width : 120-mil ·Spacing : 240-mil		·4 inch ·Width : 5.8-mil ·Spacing : 15&20-mil		
Channel Loss(dB)	Thru	NEXT	Thru	FEXT	Thru	NEXT	FEXT
	-11	-25	-11	-25	-7.3	-27.68	-21
Area(mm^2)	0.426		0.144		0.84		
Output Swing(mV_{pp})	400		500		400		
Power(mW)	177		46		34.64		
Adaptation	NEXT canceller		No		Both		
BER	10e-12		10e-9		10e-9		
Signaling	Differential		Single		Differential		

Table 4.2. CHIP Power Breakdown

RX Power Breakdown(10Gb/s)	
NEXT Canceller	16.4mW(Delay Cell)+2.1mW(Core)
FEXT Canceller	1.54mW
Clock Distribution	6.8mW
CTLE	1.29mW
Buffer	6.51mW
Total Power	34.64mW

The chip is fabricated in GP 65nm CMOS process, and the area including ESD diodes and decoupling capacitors is 0.84mm^2 (core : 0.3mm^2), and consumes about 34.6mW. For testing, the differential channels with 4-inch long microstrip line are fabricated on the FR4 PCB in Fig. 4.23 with 5.8-mil width and 15-mil space for NEXT channel, and with 5.8-mil width and 20-mil space for FEXT channel to thru Channel.

V. CONCLUSION AND FUTURE WORK

V.1. Conclusion

We can see that it is hard to overcome the electrical channel loss and other channel defects losses without using modulation techniques and equalizer techniques in the transmitter side, or cross-talk canceller, and CTLE techniques in the receiver side in serial links. This dissertation has represented and developed various techniques for conquering channel limitation to meet proper BER in the high-speed IO design.

The first work is that the 20Gb/s transmitter was designed in a 1V GP 90nm CMOS process. Simulations are performed with the three backplane channels in Fig. 3.5 to verify the different modulation capabilities and verify which modulation provides the most margin for a given channel and data rate. Fig. 3.1 shows 10Gb/s eye diagrams with channel number 1, where the loss profile is 4.5, 6.8, and 9.1dB for β0, β1, and β2, respectively. Table 3.2 confirms that PAM2 modulation yields the largest voltage margin, as expected with this low loss channel. Fig. 3.22 shows 12.5Gb/s eye diagrams with channel number 2, where the loss profile is 11.3, 16.3, and 28dB for β0, β1, and β2, respectively. Table 3.3 confirms that PAM4 modulation yields the largest voltage and also timing margin, as expected with this high loss channel with a steep loss slope around this data rate. Fig. 3.24 shows 8Gb/s eye diagrams with channel number 3, where the loss profile is 8.5, 11.5, and 21.5dB for β0, β1, and β2, respectively. Table 3.4 confirms that duobinary modulation yields the largest voltage margin, as expected with this high loss channel with a moderate loss slope around this data rate. Finally, Fig. 3.24 shows eye diagrams with an ideal channel to confirm 20Gb/s operation. Table 3.5

summarizes the 20Gb/s transmitter performance and compares the design relative to other high-speed serial I/O transmitters. The efficient quarter-rate precoder implementation allows for reduced power consumption and low voltage operation.

The second work is that it presented receive-side circuitry which merges the cancellation of NEXT and FEXT and can automatically adapt to different channel environments and variations in process, voltage, and temperature. Efficient NEXT cancellation is achieved with only three filter taps through the inclusion of a continuous-time band-pass filter IIR tap in the NEXT cancellation filter. Utilizing independent SS-LMS and power-equalizing loops for NEXT and FEXT adaptation, respectively, allows for the optimization of both cancellation filters. Overall, the proposed circuits provide the potential for increased robustness to crosstalk in systems where both NEXT and FEXT exist. Table 4.1 summarizes the performance of the prototype receive-side crosstalk cancellation circuitry and compares it to other recent designs. Relative to the work of [21] and [56], which only considered one type of crosstalk, the proposed design is able to efficiently cancel both NEXT and FEXT with the ability to adapt the cancellation filter parameters. Table 4.2 shows the measured power breakdown at 10 Gb/s, with a total power of 34.6 mW or 3.46 pJ/b. The majority of power is consumed in the NEXT canceller due to the CML latches employed in the FIR filter, suggesting that further improvements in power are possible by moving to a CMOS implementation.

In conclusion, the proposed architectures in the transmitter side and receiver side together are to be good solution in the high speed I/O serial links to improve the

performance by overcome the physical channel loss and adjacent channel noise as the system becomes complicated.

V.2. Recommendations For Future Work

As the operating frequency increases, and various protocols are requested, the number of pins for chips are increased and the space between them is getting problematic for crosstalks. Therefore the PCB design to mount the chips is also getting sophisticated and complicated. The congestion of signals is necessary to be solved making lots of signal paths through various layers by vias. Generally in FR4 pcb, one via causes less than 1.5 db loss [70]. It means that two or three vias can cause 3 or 4.5 db loss more in the pcb. It can exasperate transceiver jitter budget or loss budget, so it's hard to meet them without modulation techniques, channel equalization techniques or noise cancellation techniques. Firstly, the modulation techniques can help the user to have less burden on the bandwidth of channel loss like half and third over fourth as in PAM4 and Duobinary modulation respectively. Of course they need decoder circuits in the receiver side, but it's worth adopting this techniques. Secondly, the equalization techniques such as FFE in the transmitter side and CTLE and DFE in the receiver side can overcome the loss in the electrical channel. CTLE is generally used in the linear loss channel, but DFE is better in the bumpy channel [69].And thirdly, the noise canceller is helpful in case of close signal lines which affect each other from the near-end or far-end side. In case of near-end crosstalk, NEXT is used, but it's hard to be implemented with active components beyond 10Gbps, because MOSFET's non-linearity and RC time constants for current's summation to remove the near-end crosstalk. Therefore the proposed adaptive NEXT

operating at half data rate frequency can be modified at higher data rate application. Also the adaptive FEXT is able to be applied to remove far-end crosstalk interference. The FEXT is easier to be implemented by passive components, RC, comparing to the NEXT.

Finally, the proposed transmitter architecture including FFE and modulation techniques in the transmitter side and the noise canceller in the receiver side can be variously combined according to the channel characteristic. As the date rate increases, PAM4 modulation technique can be strongly recommended in the serdes design combining FFE, CTLE and DFE.

REFERENCES

[1] R. Payne et al., "A 6.25-Gb/s binary transceiver in 0.13-um CMOS for serial data transmission across high loss legacy backplane channels," IEEE Journal of Solid-State Circuits, 40, (12), (2005), pp. 2646–2657.

[2] J. L. Zerbe et al., "Equalization and clock recovery for a 2.5-10Gb/s 2-PAM/4-PAM backplane transceiver cell," IEEE Journal of Solid-State Circuits, 38, (12), (2003), pp. 2121–2130.

[3] B. Casper et al., "A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS," in: IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2006, pp. 263-272.

[4] V. Stojanovic et al., "Adaptive equalization and data recovery in a dual-Mode (PAM2/4) serial link transceiver," in VLSI Circuits Symp. Dig. Tech. Papers, Jun. 2004, pp. 348–351.

[5] J. Lee et al., "Design and comparison of three 20-Gb/s backplane transceivers for duobinary, PAM4, and NRZ data," IEEE Journal of Solid-State Circuits, 43, (9), (2008), pp. 2120-2133.

[6] Pelard, E. Gebara, A. Kim, M. Vrazel, F. Bien, Y. Hur, M. Maeng, S. Chandramouli, C. Chun, S. Bajekal, S. Ralph, B. Schmukler, V. Hietala, and J. Laskar, "Realization of multigigabit channel equalization and crosstalk cancellation integrated circuits," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1659–1670, Oct. 2004.

[7] Y. Hur, M. Maeng, C. Chun, F. Bien, H. Kim, S. Chandramouli, E. Gebara, and J. Laskar, "Equalization and near-end crosstalk (NEXT) noise cancellation for 20-Gb/s 4-PAM backplane serial I/O interconnections," *IEEE Trans. On Microwave Theory and Tech.*, vol. 53, no. 1, pp. 246–255, Jan. 2005.

[8] M. Nazari and A. Emami-Neyestanak, "A 15-Gb/s 0.5-mW/Gbps two-tap DFE receiver with far-end crosstalk cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2420–2432, Oct. 2012.

[9] T. Oh and R. Harjani, "A 12-Gb/s multichannel I/O using MIMO crosstalk cancellation and signal reutilization in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1383–1397, June 2013.

[10] Wikipedia. [Online]. Available: https://en.wikipedia.org/wiki/Crosstalk

[11] "Microwaves101.com" [Online]. Available: http://www.microwaves101.com/encyclopedias

[12] "RF Cafe" [Online]. Available: http://www.rfcafe.com/references/electrical/skin-depth.htm

[13] Eric Bogatin, "Signal and Power Integrity-Simplified", Second Edition, pp. 143-158.

[14] National Instruments, "Understanding and Characterizing Timing Jitter", pp 2-8.

[15] Mike Resso, Eric Bogatin, "Signal Integrity Characterization Techniques", pp. 68-88.

[16] David Smalley, "Equalization Concepts: A Tutorial", pp. 4-8.

[17] Samueli, H., Daneshrad, B., Joshi, R., Wong, B., and Nicholas, H., "A 64-Tap CMOS Echo Canceller/Decision Feedback Equalizer for 2B1Q HDSL Transceivers," IEEE Journal on Selected Areas in Communications, Vol. 9, August 1991, pp. 839–847.

[18] Simon S. Haykin, Bernard Widrow (Editor): *Least-Mean-Square Adaptive Filters,* Wiley, 2003

[19] K. Parhi, "Design of Multigigabit Multiplexer-Loop-Based Decision Feedback Equalizers," IEEE Transactions On Very Large Scale Integration (VLSI) systems, Vol. 13, No.4, April 2005

[20] W. U. Lee and F. S. Hill. A Maximum-likelihood Sequence Estimator with Decision-feedback Equalization. IEEE Trans. Commun., 25:971-979, 1977.

[21] J. Lee, "A 20-Gb/s adaptive equalizer in 0.13-μm CMOS technology," IEEE J.Solid-State Circuits,vol.41,no.9,pp.20582066, Sep.2006

[22] Shahramian, S., Yasotharan, H., Carusone, A.: "Decision feedback equalizer architectures with multiple continuous-time infinite impulse response filters," IEEE Trans. Circuits Syst. II, 2012, 59, (6), pp. 226–230

[23] Payne, R., Bhakta, B., Ramaswamy, S., et al.: "A 6.25 Gb/s binary adaptive DFE with first post-cursor tap cancellation for serial backplane communications," IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers, 2005, pp. 68–69

[24] S.-Y. Kao and S.-I. Liu, "A 10-Gb/s adaptive parallel receiver with joint XTC and DFE using power detection," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2815–2826, Nov. 2013.

[25] G. Balamurugan et al., "Modeling and analysis of high-speed I/O links," IEEE Transactions on Advanced Packaging, 32, (2), (2009), pp. 237-247.

[26] Stateye. [Online]. Available: http://www.stateye.org.

[27] J. Proakis and M. Salehi, *Communication Systems Engineering*. Upper Saddle River, NJ: Prentice Hall, 1994.

[28] K. Yamaguchi et al., "12Gb/s Duobinary Signaling with ×2 Oversampled Edge Equalization," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2005, pp. 70-71.

[29] K. Hu, L. Wu, and P. Chiang, "A comparative study of 20-Gb/s NRZ and duobinary signaling using statistical analysis," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (2011)

[30] P. Chiang et al., "A 20Gb/s 0.13um CMOS serial link transmitter using an LC-PLL to directly drive the output multiplexer," IEEE Journal of Solid-State Circuits, 40, (4), (2005), pp. 1004-1011.

[31] Vijaya Sankara Rao et al., "High-Speed Low-Current Duobinary Signaling Over Active Terminated Chip-to-Chip Interconnect," IEEE Computer Society Annual Symposium on Very Large Scale Integration(VLSI), May.2009, pp. 73-78.

[32] Simon Haykin, "Adaptive Filter Theory," Prentice Hall, 2001

[33] G. Balamurugan, B. Casper, J. Jaussi, M. Mansuri, F. O'Mahony, and J. Kennedy, "Modeling and analysis of high-speed I/O links," *IEEE Trans. On Adv. Packaging*, vol. 32, no. 2, pp. 237–247, May 2009.

[34] M. Li, M. Shimanouchi, and H. Wu, "Advancements in high-speed link modeling and simulation," in *IEEE Custom Integrated Circuits Conference*, pp. 1-8, Sept. 2013.

[35] Momtaz and M. Green, "An 80mW 40Gb/s 7-tap T/2-spaced feed-forward equalizer in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 629–639, Mar. 2010.

[36] M.-S. Chen, Y.-N. Shih, C.-L. Lin, H.-W. Hung, and J. Lee, "A fully-integrated 40-Gb/s transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 627–640, Mar. 2012.

[37] J. Bulzacchelli, C. Menolfi, T. Beukema, D. Storaska, J. Hertle, D. Hanson, P.-H. Hsieh, S. Rylov, D. Furrer, D. Gardellini, A. Prati, T. Morf, V. Sharma, R. Kelkar, H. Ainspan, W. Kelly, L. Chieco, G. Ritter, J. Sorice, J. Garlett, R. Callan, M. Brandli, P. Buchmann, M. Kossel, T. Toifl, D. Friedman, "A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3232–3248, Dec. 2012.

[38] M. Mansuri, J. Jaussi, J. Kennedy, T.-C. Hsieh, S. Shekhar, G. Balamurugan, F. O'Mahony, C. Roberts, R. Mooney, and B. Casper, "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3229–3242, Dec. 2013.

[39] K. Lee, H.-K. Jung, J.-Y. Sim, and H.-J. Park, "Reduction of transient far-end crosstalk voltage and jitter in DIMM connectors for DRAM interface," *IEEE Microwave and Wireless Comp. Letters*, vol. 19, no. 1, pp. 15–17, Jan. 2009.

[40] M. Kotzev, R. Frech, H. Harrer, D. Kaller, A. Huber, T.-M. Winkel, H.-D. Bruns, and C. Schuster, "Crosstalk analysis in high density connector via pin fields for digital backplane applications using a 12-port vector network analyzer," in *IEEE Electronic System-Integration Tech. Conference*, pp. 13-16, Sept. 2010.

[41] Deutsch, "Electrical characteristics of interconnections for high-performance systems," *Proc. IEEE*, vol. 86, no. 2, pp. 315–355, Feb. 1998.

[42] J.-H. Lu and S.-I. Liu, "A merged CMOS digital near-end crosstalk canceller and analog equalizer for multi-lane serial-link receivers," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 433–446, Feb. 2010.

[43] J. Zerbe, P. Chau, C. Werner, W. Stonecypher, H. Liaw, G. Yeh, T. Thrush, S. Best, and K. Donnelly, "A 2Gb/s/pin 4-PAM parallel bus interface with transmit crosstalk cancellation, equalization, and integrating receivers," in *IEEE Int. Solid-State Circuits Conference*, pp. 66-67, Feb. 2001.

[44] S.-J. Bae, Y.-S. Sohn, T.-Y. Oh, S.-H. Kim, Y.-S. Yang, D.-H. Kim, S.-H. Kwak, H.-S. Seol, C.-H. Shin, M.-S. Park, G.-H. Han, B.-C. Kim, Y.-K. Cho, H.-R. Kim, S.-Y. Doo, Y.-S. Kim, D.-S. Kang, Y.-R. Choi, S.-Y. Bang, S.-Y. Park, Y.-J. Shin, G.-S. Moon, C.-G. Park, W.-S. Kim, H.-J. Yang, J.-D. Lim, K.-I. Park, J Choi, and Y.-H. Jun, "A 40nm 2Gb 7Gb/s/pin GDDR5 SDRAM with a programmable DQ ordering crosstalk equalizer and adjustable clock-tracking BW," in *IEEE Int. Solid-State Circuits Conference*, pp. 498-499, Feb. 2011.

[45] H.-K. Jung, I.-M. Yi, S.-M. Lee, J.-Y. Sim, and H.-J. Park, "A transmitter to compensate for crosstalk-induced jitter by subtracting a rectangular crosstalk waveform from data signal during the data transition time in coupled microstrip lines," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2068–2079, Sept. 2012.

[46] S.-Y. Kao and S.-I. Liu, "A 7.5-Gb/s one-tap-FFE transmitter with adaptive far-end crosstalk cancellation using duty cycle detection," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 391–404, Feb. 2013.

[47] J. Buckwalter and A. Hajimiri, "Cancellation of crosstalk-induced jitter," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 621–632, Mar. 2006.

[48] H.-K. Jung, K. Lee, J.-S. Kim, J.-J. Lee, J.-Y. Sim, and H.-J. Park, "A 4 Gb/s 3-bit parallel transmitter with the crosstalk-induced jitter compensation using TX data timing control," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2891–2900, Nov. 2009.

[49] K.-I. Oh, L.-S. Kim, K.-I. Park, Y.-H. Jun, J. Choi, and K. Kim, "A 5-Gb/s/pin transceiver for DDR memory interface with a crosstalk suppression scheme," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2222–2232, Aug. 2009.

[50] T. Oh and R. Harjani, "A 6-Gb/s MIMO crosstalk cancellation scheme for high-speed I/Os," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1843–1856, Aug. 2011.

[51] S.-K. Lee, B. Kim, H.-J. Park, and J.-Y. Sim, "A 5 Gb/s single-ended parallel receiver with adaptive crosstalk-induced jitter cancellation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2118–2127, Sept. 2013.

[52] B. Min, N. Yang, and S. Palermo, "10 Gb/s adaptive receive-side near-end and far-end crosstalk cancellation circuitry," in *IEEE Int. Midwest Symp. On Circuits and Systems*, pp. 77-80, Aug. 2014.

[53] H. Cirit and M. Loinaz, "A 10Gb/s half-UI IIR-tap transmitter in 40nm CMOS," in *IEEE Int. Solid-State Circuits Conference*, pp. 448-449, Feb. 2011.

[54] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *IEEE Int. Solid-State Circuits Conference*, pp. 314-315, Feb. 2007.

[55] J. Lee, "A 20-Gb/s adaptive equalizer in 0.13-µm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2058–2066, Sept. 2006.

[56] J.-H. Lu and S.-I. Liu, "A merged CMOS digital near-end crosstalk canceller and analog equalizer for multi-lane serial-link receivers," *IEEE JSSC*, vol. 45, no. 2, pp. 433-446, Feb. 2010

[57] M. Nazari and A. Emami-Neyestanak, "A 15-Gb/s 0.5-mW/Gbps two-tap DFE receiver with far-end crosstalk cancellation," *IEEE JSSC*, vol. 47, no. 10, pp. 2420-2432, Oct. 2012.

[58] RAZAVI, B., WOOLEY, B. A. "Design techniques for high-speed, high-resolution comparators," IEEE Journal of Solid-State Circuits, 1992, vol. 27, no. 12, p. 1916 - 1926

[59] M. Meghelli, *et al*., "A 10Gb/s 5-Tap-DFE/4-Tap FFE Transceiver in 90nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 213-222, Feb. 2006.

[60] K. Wong, *et al*., "A Serial-Link Transceiver with Transition Equalization," in *IEEE ISSCC Dig. Tech. Papers*, pp. 223-232, Feb. 2006.

[61] B. Casper, *et al*., "A 20Gb/s Forwarded Clock Trasnceiver in 90nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 263-272, Feb. 2006

[62] R. Palmer, *et al*., "A 14mW 6.25Gb/s Transceiver 9n 90nm CMOS for Serial Chip-to-Chip Communications," in *IEEE ISSCC Dig. Tech. Papers*, pp. 440-614, Feb. 2007.

[63] Y. Hidaka, *et al*., "A 4-Channel 3.1/10.3Gb/s Transceiver Macro with a Pattern-Tolerant Adaptive Equalizer," in *IEEE ISSCC Dig. Tech. Papers*, pp. 442-443, Feb. 2007.

[64] J.-K. Kim, *et al.,* "A 40-Gb/s Transceiver in 0.13-μm CMOS Technology," *IEEE Symp. on VLSI Circuits*, pp. 196-197, June. 2008.

[65] Y. Hidaka, *et al*., "A 4-Channel 10.3Gb/s Backplane Transceiver Macro with 35dB Equalizer and Sign-Based Zero-Forcing Adaptive Control," in *IEEE ISSCC Dig. Tech. Papers*, pp. 188-189a, Feb. 2009.

[66] A. Agrawal, *et al*., "A 19Gb/s Serial Link Receiver with Both 4-Tap FFE and 5-Tap DFE Functions in 45nm SOI CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 134-135, Feb. 2012.

[67] W. Dally, *et al*., "*Digital Systems Engineering*," Cambridge, U.K.: Cambridge University Press, 1998.

[68] "Understanding and Characterizing Timing Jitter" [Online]. Available: http://www.ni.com/white-paper/14227/en/#toc3

[69] Ransom Stephens, "Optimize equalization for FFE, CTLE, DFE, and crosstalk," EDN NETWORK

[70] Mike Resso, et al., "Signal Integrity Characterization Techniques", International Engineering Consortium.