ANALYSIS OF LIGHTNING ARRESTER OVERLOADING IN FUTURE DISTRIBUTION SYSTEMS WITH DISTRIBUTED GENERATION

A Thesis

by

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ABSTRACT

The objective of this thesis is to address an issue that arises from the increasing penetration of distributed energy resources in future power systems: the design and analysis of protective devices with more complex topology and power flow patterns. In particular, this thesis investigates lightning arrester overloading and failure from fault-induced overvoltages. Currently, in existing literature and industry practice, there does not exist a readily practical and sufficiently accurate method to determine the magnitude of a fault-induced overvoltage. Thus, the length of time from the fault inception until the lightning arresters fail is unknown, forcing utility companies to assume the worst case scenario and install more costly and complex protection schemes than otherwise needed.

In this thesis, the Thevenin Equivalent Impedance method is proposed to analyze a distributed generation (DG) source's effect on the transformer high side voltage. After examining the voltage transients and determining the magnitude of the overvoltage, an optimal and cost-effective protective relaying strategy is developed and implemented. To complete this study, various types of DG sources were modeled and simulated using two test systems. Finally, the implementation of the suggested solution of intentional islanding operation of the distribution system is discussed. This solution allows the DG source to continue to supply a portion of the distribution system's load, thereby increasing the reliability of the system.

ACKNOWLEDGEMENTS

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NOMENCLATURE

ATP	Alternative Transients Program
EMTP	Electromagnetic Transient Program
DG	Distributed Generation
MCOV	Maximum Continuous Operating Voltage
POI	Point of Interconnection
PQ Bus	Bus Real Power (P), Reactive Power (Q) specified
PV Bus	Bus Power and Voltage specified
TOV	Temporary Overvoltage
VT	Voltage Transformer

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1 INTRODUCTION

One of the major challenges facing the world today is that of global climate change and the resulting effects on the environment. In response, there have been efforts to decrease greenhouse gas emissions by installing new renewable energy sources to eventually replace fossil-fuel based generation [1]. Many distributed generation (DG) resources, such as photovoltaic panels or wind turbines, are integrated directly into distribution systems. DG resources pose fundamental challenges in today's control and protection framework of distribution systems, since the traditional design philosophy is based on the premise of unidirectional power flow from transmission down to the distribution systems. While there are numerous challenges to overcome when integrating DG into future or existing energy systems, the focus of this thesis is to model, analyze, and design a coordinated protection scheme for a class of protection devices: the lightning arresters.

If a distribution system with adequate distributed generation is connected to the transmission grid through a delta-wye substation transformer, a permanent line-to-ground fault that causes the distribution grid to inadvertently island will cause at worst a line-to-line voltage drop across the lightning arresters, thus quickly overloading the arresters. Without an analysis method to determine the possibility and severity of these overvoltages, utility companies are forced to assume the worst case scenario, and must implement a protection scheme that is potentially much more complex and costly than

otherwise required. Thus, a simpler method to analyze the voltage profile of a distribution system with integrated DG is of great need.

1.1 Contributions from this Thesis

This project was motivated by a summer project by the author with a Texas utility that was facing the aforementioned problem. In response to this issue, research was conducted on using a simple, but sufficiently accurate model of the distribution system to determine the overvoltage that results from the installation of a given DG source in to a distribution grid. By determining the severity of the overvoltage, a more proper protective relaying scheme may be utilized, preventing a utility company from implementing an overly conservative and costly scheme. Utilizing the Thevenin Equivalent Method suggested in this paper could potentially save utility companies numerous hours in conducting a more complicated and detailed system study. Also, implementing the protective relaying schemes suggested in this thesis can potentially save tens to hundreds of thousands of dollars on costly protection equipment. Additionally, if islanding schemes are utilized, the DG source can continue to operate during a transmission-level fault, increasing reliability of the distribution grid by supplying a portion of the distribution system load.

The outline of this thesis is as follows: Sections 2 and 3 present an overview of the lightning arrester overvoltage problem, as well as the current solutions used by utility companies. Sections 4 and 5 give an overview of the existing academic literature on lightning arrester overloading, and lists the shortcomings of the current analysis and solutions presented. The cause of the overvoltage conditions is more fully examined in

section 6, and the impact on lightning arresters is discussed in section 7, along with additional background information on lightning arresters. The Thevenin Equivalent solution method is explained in section 8, and test systems are introduced in section 9. The results of the transient voltage analysis as well as the steady state voltage levels are given in section 10. In section 11, protective relaying strategies are presented and successful islanding operation of the distribution grid is discussed. Finally, sections 12 and 13 present areas for future research, as well as summarize the research in this thesis.

2 PROBLEM OVERVIEW

An increasing amount of distributed generation, such as wind and solar, is being integrated into distributions systems. Though there are many problems that such installations pose, one such issue is the risk of a transformer high-side overvoltage contingency when a substation is connected at a single point to a high-voltage transmission line via delta-wye step-up transformer, as shown in Figure 2.1

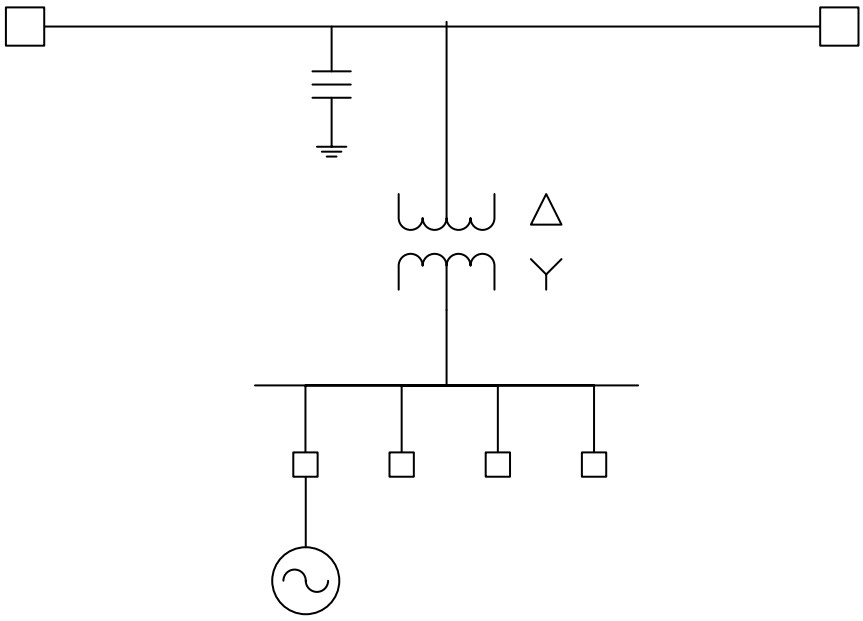


Figure 2.1: Distribution System One-Line with DG

The lightning arrestors are connected to the transmission line directly from each conductor to ground, as shown in Figure 2.2, thus nominally experiencing line-to-ground voltages.

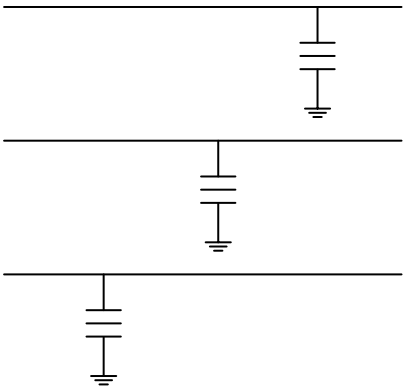


Figure 2.2: Lightning Arrester Connections to Transmission Lines

However, for normal transmission lines, voltages are given in line-to-line quantities, thus a 138kV transmission line would have a line to neutral voltage of approximately 80kV (precisely 79.67kV). Thus, for normal operation, a lightning arrestor would experience a line to neutral (or ground) voltage drop.

In the case of a line to ground fault (shown in Figure 2.3), the transmission level line-end breakers will open (near) instantaneously, assuming there is a communication scheme between the line-end relays. Once the line-end breakers have opened, the DG source will be connected to the transmission grid via an ungrounded delta transformer, until the DG or distribution substation breaker trips. During this period (10-20 cycles, or

longer), the lightning arrestors on the non-faulted phases will experience a line-to-line voltage drop instead of the customary line-to-neutral voltage drop, as explained in further sections. If the overvoltage is severe enough, and the DG source isn't tripped within 2-3 cycles, then this overvoltage condition will cause the semiconductor-based lightning arrestors to fail. However, as explained later in this thesis, the delta transformer creates a break in the zero-sequence transformer impedance, thus no fault current flows, making fault detection much more difficult since traditional overcurrent relays cannot be used.

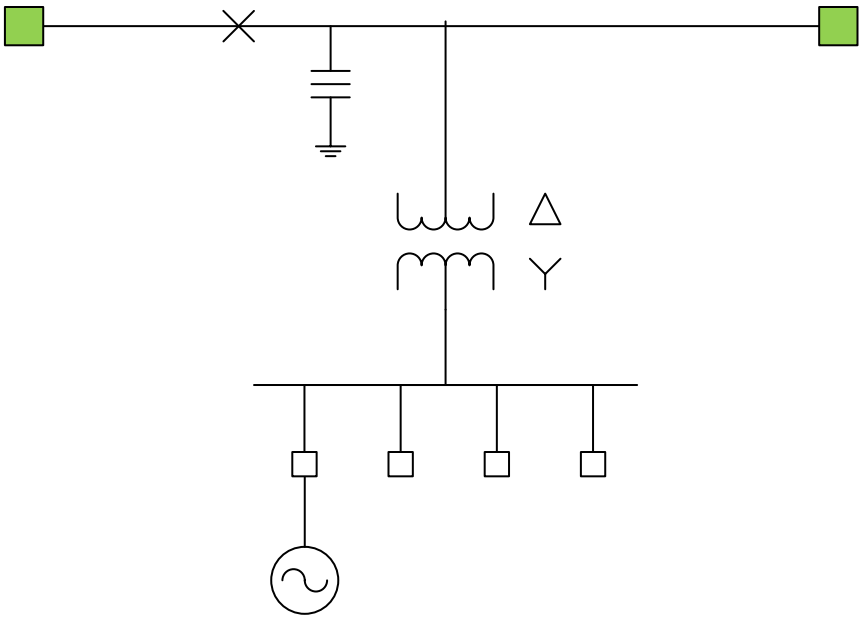


Figure 2.3: System One-Line after Line-End Breakers Opened

Currently, protection engineers mitigate this risk by installing a transmission-level undervoltage relaying scheme with a direct transfer trip signal to the DG source's main breaker. This transfer trip command could initiate from the remote substation relays, or a relay on the high side of the local substation transformer. While this approach is robust and reliable, it causes over-tripping of the DG source for every transmission line fault, including temporary faults. This means the DG source must wait a set amount of time before reconnecting to the transmission grid, and must go through the resynchronization process before connecting to the grid. This results in lost revenue for the DG, and increased wear and tear on the DG interconnection breaker. Also, there is currently no analysis process to determine if the DG source is sufficient to cause overvoltages capable of damaging the lightning arresters, or if the distribution system load causes sufficient voltage drop to mitigate the problem. Therefore, the worst case scenario is assumed, and the undervoltage relaying with direct transfer trip is implemented for all cases of distribution level interconnected DG. Thus, a simple, but sufficiently accurate method of determining the overvoltage conditions resulting from the line-to-ground fault needs to be developed, as will be explained in subsequent sections.

3 CURRENT INDUSTRY PRACTICE

In the Electric Reliability Council of Texas (ERCOT) grid, due to deregulation, there is a limited amount of information that can be shared between generation companies, transmission/distribution companies, and the retail electric providers. Thus, if a generation company, or an independent power producer, wants to connect a new power source to the distribution or transmission grid, the system operator or transmission company needs to conduct a feasibility study to make sure that the new generation can be safely and properly connected [2].

For both cases, the generation company must supply the needed information to the transmission company regarding the details and capacity of the generation to be connected, the point of interconnection, and any other information required to complete the study. Thus, the generation company supplies only one proposed location, and this location is used for the interconnection study, regardless of whether this is the optimal interconnection location or not. However, this results in an easier feasibility study, since the generation capacity and interconnection location are already known.

Since the DG source to be integrated is only proposed and not actually installed, this is a worst-case analysis study. Thus, the worst-case DG source levels and system loading conditions are used to determine the highest possible voltage across the lightning arresters. This occurs when the DG source is producing its rated power output (e.g. at noon on a sunny day for a solar photovoltaic installation), and the load is at its lightest (e.g. a mild spring day where little air conditioning is running). Thus, the generation and

load quantities are conservative estimates and create factors of safety in the system. Also, in typical utility distribution voltage studies of this type, unbalanced operation is not considered, however, for the purpose of this paper, unbalanced load and asymmetrical distribution lines are considered.

Currently, there is no good method of determining if the proposed DG capacity will result in lightning arrester overload conditions. Consequently, utility protection engineers assume the worst-case scenario and design the protection schemes such that they trip the DG source for any transmission-level fault. However, this results in unnecessary tripping of the DG for temporary faults, as well as interconnections where the DG source capacity isn't high enough to cause lightning arrester overloads.

One method that has been proposed is the sequence network analysis method, but as discussed later in this paper, the asymmetrical distribution lines and unbalanced distribution loads substantially complicate the symmetrical component analysis by making the sequence networks no longer decoupled and independent. Thus, a simpler analysis method must be developed to determine if the proposed DG will operate safely, or if additional and more complicated analysis methods are required.

The conclusion is that using the Thevenin impedance method results in a first-order approximation of the transformer high-side voltages. If these calculated voltages are below the threshold where the lightning arresters will be overloaded, then simpler protective relaying strategies may be used, saving time and money. If the calculated voltages are above the threshold voltage range, then islanding schemes may be implemented, depending on the DG capacity.

For a more robust solution, adaptive relaying strategies may be implemented that take the current load and DG source capacities into account when determining whether to island the system, trip the DG, or allow existing protection schemes to work.

4 LITERATURE REVIEW

Several other sources have theorized about the line-to-line overvoltage across the lightning arresters and documented the potential problems that this overvoltage condition would create. In [3], it is shown that an ungrounded wye system could experience up to a 1.73 per unit overvoltage on the unfaulted phases for a single-line to ground fault. [4] indicates that a 1.73 overvoltage can also occur from an open phase fault. [5] introduces the idea of cogeneration (DG) connected to a distribution system, and presents the same problem as addressed in this paper: a distribution-level DG source is interconnected to the transmission grid through a delta-wye transformer. According to [5], during a ground fault, the line-end breakers will open, but the DG breaker will not open due to the delta connection preventing fault current from flowing. Until the DG breaker trips on underfrequency or undervoltage, the line section between the transformer and the line-end breakers will operate at as a 3-wire system, and the unfaulted phases "may reach 1.73 P.U. This overvoltage may have no effect on gapped arresters, but the metal oxide arresters on this feeder will conduct current on the overvoltage. If the overvoltage is high, the metal oxide arresters will fail unless the duration of the overvoltage is short." [5]

While all of these papers explain that the neutral shift overvoltages can occur in theory, none of them ran any simulations to illustrate or prove this point. Additionally, none of the sources mention islanding the distribution grid as a possible solution for the overloads. However, later in this paper, the line-to-ground fault on an ungrounded

(delta) system cause of the neutral shift overvoltage will be examined, and simulations will verify that this condition does indeed result in an overvoltage of approximately 1.73 pu voltage on the unfaulted phases.

4.1 Currently Suggested Solutions in Literature

One solution described by [3] is to make the lightning arresters less sensitive to overvoltages, and if an arrester does overload, making sure that the arrester fails in an acceptable manner. According to [4], this can be accomplished by placing a disconnector in series after the lightning arrester, which disconnects after the arrester has failed to remove the short circuit from the transmission line.

4.1.1 Gapped Lightning Arresters

According to [4] and [6], an efficient way to prevent the lightning arresters from being overloaded is to introduce gapped silicon-carbide arresters in series with the MOV arresters. The withstand voltage of the gapped arresters is approximately 2.34 pu, which is above the maximum overvoltage experienced by the arresters [4]. The problem is that most proposed DG integrations are into existing distribution networks with existing transmission infrastructure already in place. Thus, all of the lightning arresters on the connected transmission lines would need to be replaced, at great cost to the DG owner or transmission grid operator. Another problem is that the higher withstand voltage of a gapped arrester also means that the arrester has a higher flashover voltage, thus offering less protection to connected equipment in the event of transient overvoltages and switching surges [3]. Thus, a method that allows the current system configuration to remain unchanged is needed.

5 ALTERNATE ANALYSIS METHODS

Next, two existing methods of voltage analysis, load flow and sequence network analysis, are explored. It is shown that both of these methods have disadvantages, and a simpler, first step approach is needed to determine the substation voltage levels for the proposed DG installation.

5.1 Distribution Load Flow

Load flow is a method that uses the network impedance matrix and three different types of busses to determine the voltage magnitudes and phase angles at each bus, as well as the real and reactive power flows along each line connecting the busses. As detailed by [7], load flow calculations use the voltage equations shown below in Figure 5.1. There is one bus, the slack or reference bus, where the voltage magnitude and phase angle is known. All other busses on the system are either load (PQ busses where the real and reactive power injection is specified) or generator (PV busses where the real power and voltage magnitude are specified) busses.

$$\mathbf{V}_k = \frac{1}{\mathbf{Y}_{kk}} \left(\frac{P_k - jQ_k}{\mathbf{V}_k^*} - \sum_{j \neq k} \mathbf{Y}_{jk} \mathbf{V}_j \right)$$

Figure 5.1: Network Bus Voltages

As detailed by [8], distribution load flow takes into account asymmetrical distribution lines and unbalanced loading conditions. The method presented in [8] utilizes the Zbus Gauss solution approach which takes advantage of the sparse bifactored Ybus matrix, and treats unbalanced loads as current injections into or from the network. Another paper, [9] uses the Newton-Raphson method and calculates the effect of distributed generation in the distribution network by modeling the generators as PV busses.

The limitation with using distribution load flow is that there must be a slack bus to establish the voltage phase angle reference, as well as meet any power mismatch not supplied by the generation busses. However, islanded distribution systems inherently do not meet this criteria, since the utility grid can no longer be considered the slack bus. Also, as in the cases explored later in this thesis, the DG generation capacity is below the load levels, and the substation voltage must be computed to examine the effect on lightning arrester overloading. This short time scale voltage profile is present before the load shedding relays will operate, thus removing the possibility of using distribution level load flow for this analysis.

Finally, distribution load flow requires a full system model of the distribution system with precise load locations, and as detailed in section 3, the load levels and locations are not precisely known for the purpose of determining if lightning arresters will overload. Thus, an analysis method that allows for mismatch between generation and load, as well as accommodates uncertainty in the load placement and levels, is needed.

5.2 Sequence Network Approach

As detailed in Appendix A [10], symmetrical components is a method that is utilized to change an unbalanced set of voltage or current phasors into three sets of balanced phasors: positive, negative and zero sequence. This analysis method is utilized to compute voltages and currents for inherently unbalanced systems, such as line-to-ground fault conditions.

However, as shown later in this paper, distribution systems have unbalanced loads and asymmetrical distribution lines by nature, thus significantly complicating the sequence network analysis. For example, the load at node 675 on the IEEE 13 node feeder test case is shown in Table 5.1 below.

Node	Load Model	Ph-1 kW	Ph-1 kVAr	Ph-2 kW	Ph-2 kVAr	Ph-3 kW	Ph-3 kVAr
675	Y-PQ	485	190	68	60	290	212

Table 5.1: IEEE 13 Node System Load for Node 675

The phase impedance matrix, Z_{abc} is given below. Then, the impedance is transformed to the sequence domain using the transformation described in Appendix A, and the result, Z_{012} is given below in Figure 5.2. Notice that the sequence matrix is far from diagonal, with significant cross coupling existing between most of the sequence networks.

```
Zabc =
       30.934 -     12.119i            0 +          0i            0 +          0i
            0 +          0i       143.09 -     126.26i            0 +          0i
            0 +          0i            0 +          0i       38.891 -     28.431i
Z012 =
       57.559 -      3.704i      -73.613 +     84.607i        6.749 +     62.672i
      -32.506 -     2.1161i       98.414 -     142.95i      -32.758 -      54.64i
       5.8812 -     6.2984i       6.1332 +     46.225i       56.943 -     20.151i
```

Figure 5.2: Phase and Sequence Impedance Matrices for Load at Node 675

Also, the line impedance between node 675 and the adjacent node 692 is shown below. Notice that since the line is more symmetrical than the load above, the sequence matrix is closer to being diagonal, with the exception of the cross coupling shown in the first row of the matrix.

```
ZLineabc =
       0.7982 +     0.4463i       0.3192 +     0.0328i       0.2849 -     0.0143i
       0.3192 +     0.0328i       0.7891 +     0.4041i       0.3192 +     0.0328i
       0.2849 -     0.0143i       0.3192 +     0.0328i       0.7982 +     0.4463i
ZLine012 =
       1.4033 +    0.46872i    -0.074081 +     1.7557i      0.12942 +     1.7271i
   -0.0028137 -  0.0045366i      0.47616 +    0.37439i    0.0031053 +   0.027711i
    0.0018292 + 0.00061591i      0.03021 +   0.015469i      0.50605 +    0.45359i
```

Figure 5.3: Phase and Sequence Impedance Matrices for Line from Node 675 to Node 692

Thus, when unbalanced loads are considered in a distribution system, sequence matrix analysis is not the best method to pursue when a simplified approach is desired. Thus, the Thevenin equivalent network method will be considered. Although this

method makes certain assumptions and simplifications, the results can be shown to be accurate within a desired tolerance, and will provide an excellent first-order approximation to determine whether additional studies are needed.

6 OVERVOLTAGE CONDITIONS

As more distributed generation is integrated into distribution systems, the issue of lightning arrester overloading will become more significant and important. Thus, a simple analysis method to determine a range of voltages that the DG source can create on the distribution system is an excellent method to determine if the proposed DG will operate safely, or if an additional in-depth study or special protection scheme is needed.

To illustrate the problem, the examples explained in [2] will be summarized. First, the example of a simple, 3-bus power system is given below. The utility source (S), is connected to a distribution load bus (L) through a line connected to a delta-wye transformer (T). The sequence networks are given below in Figure 6.1 (left side). Notice that as explained in the symmetrical components overview in Appendix A, there is an open circuit in the zero-sequence network at the delta connection of the transformer. In the event of a single-line to ground fault as shown in Figure 6.1 (right side), the sequence networks become connected in series. Since the load is significantly higher resistance than the source and transmission line impedance, the vast majority of the fault current flows through the source and line, and thus the current through the load can be neglected, as is typical in fault most fault analysis studies.

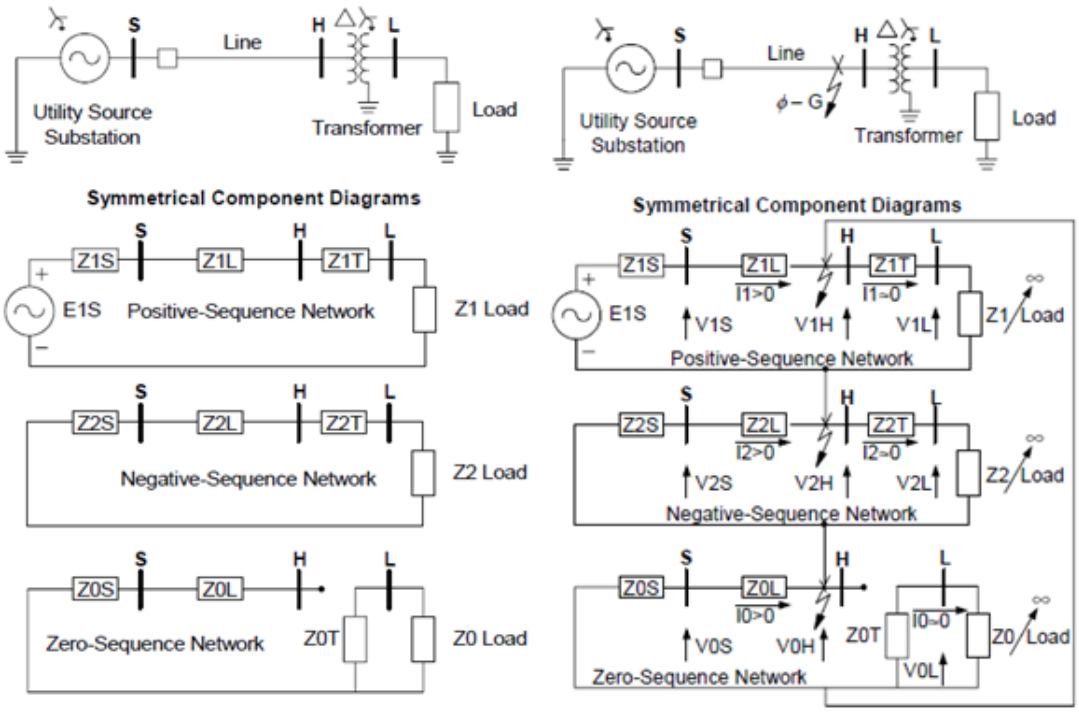


Figure 6.1: Sequence Network Connections Pre-Fault and for Single Line to Ground Fault (Reprinted with Permission from [2])

Thus, when the utility source breaker opens, the fault path becomes interrupted, thus no current can flow, as shown in Figure 6.2 (left side). However, when a DG source is introduced into the distribution system, as shown in Figure 6.2 (right side), there is still a source connected to the fault, even when the utility breaker (S) opens. However, even though the DG is still connected to the fault, no fault current flows, since the zero sequence network impedance has an open circuit from the delta winding in the transformer. However, positive sequence current still flows through the load, since it still has a return path to the source through the load grounding.

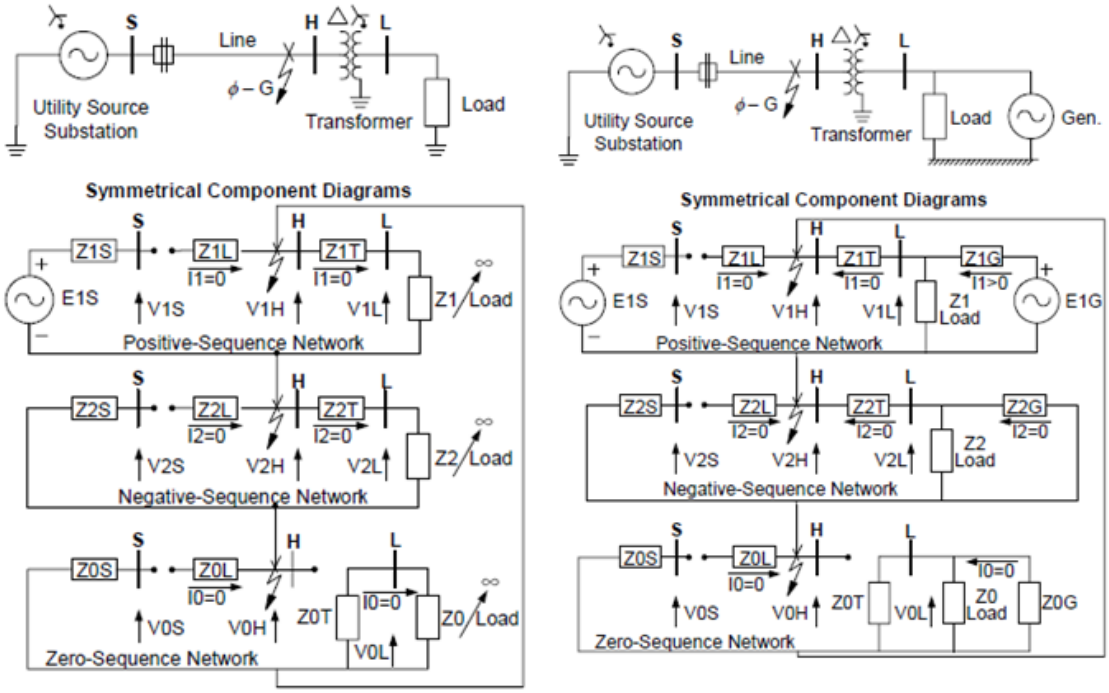


Figure 6.2: Sequence Network Connections after Utility Breaker Opens, Without and With DG Source (Reprinted with Permission from [2])

What is not shown in the figures above is the voltages on the unfaulted phases. During normal operation, the generator and y-grounded winding of the transformer provide a reference to ground for the system. Thus, the neutral point of the delta winding is in the center of the delta voltage triangle, as shown in Figure 6.3 (a). When there is a solidly-bolted fault on the system, the voltage of the faulted phase (in this case phase A), collapses to 0, and the utility grid holds the voltage of the unfaulted phases near the nominal unfaulted voltage values, as shown in Figure 6.3 (b). Once the utility breaker opens, the fault current ceases to flow, as explained above. If the fault is an arcing fault, the fault will clear, and the line will remain energized. However, if the fault

is permanent, with the worst case being a bolted fault, the apparent neutral shifts, as shown in Figure 6.3 (c). In this case, phase A is directly connected to ground, becoming the new ground reference point for the system. However, since no fault current is flowing, the phase-to-phase voltages are still maintained, so V_{ab}, V_{bc}, and V_{ca} are still their nominal values. Since phase A is the new neutral reference point, phase B and C now have line-to-line voltages across any line-to-ground connected equipment, such as arresters, or single-phase transformers. In the case of a solidly connected fault, this voltage can rise to approximately 1.73 times the normal phase-to-ground voltage, causing damage to equipment such as lightning arresters [2].

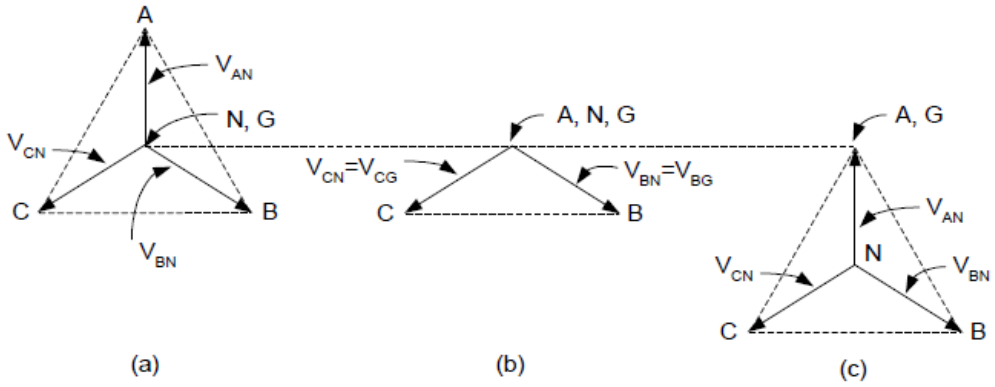


Figure 6.3: (a) Normal Phasor diagram, (b) Line-to-Line Fault, (c) Apparent Neutral Shift (Reprinted with Permission from [2])

7 LIGHTNING ARRESTER OVERVIEW

In order to protect against transient voltage spikes and surges, lightning or surge arresters are installed in numerous locations around power systems, such as on transformers, near critical loads, and on transmission towers. The lightning arresters that are of primary concern in the analysis presented in this paper are the arresters on the high side of the substation transformer, as well as the arresters on the transmission towers that are between the substation breaker and transmission line-end breakers. In particular, the arresters closer to the substation will experience higher voltage if there are additional loads tapped off the transmission line before the line-end breakers. The worst case scenario is considered: analyzing the high-side voltage assuming little to no current is flowing in the transmission line, resulting in little to no voltage drop across the transformer. Thus, the low side voltages can be used, and scaled to line-to-line voltages by multiplying by $\frac{\sqrt{3}}{2}$.

There are two main types of surge arresters installed in power systems, gapped and gapless types. Gapless, the most common arresters, are typically MOV, or Metal Oxide Varistors. These are typically made of a bulk semiconductor, such as zinc oxide, that can conduct significant current when the voltage across the arrester is above its rated voltage [11]. Unfortunately, most MOVs fail closed, i.e. when they break, they create a permanent fault on the system. MOVs can be protected by installing a series thermal fuse to prevent thermal runaway and catastrophic failure of the MOV.

Gapped arresters are the simplest and oldest overvoltage protective device, and are still found in telephone circuits today. The size of the gap determines the flashover voltage. However, since the ambient air is the dielectric material, the performance and spark voltage varies with atmospheric conditions, such as humidity. Also due to the physical presence of a spark or arc on the transmission line, gapped arresters are not used as commonly as MOV arresters.

Surge arresters are designed to protect against surge voltages associated with: lightning strikes as well as switching capacitor and equipment insulation failure. When lightning first strikes a transmission line, it quickly travels away from the point of stroke origin in both directions. The voltage magnitude of a lightning surge is typically very high, but the surge has a short duration, with typical durations of 1 to 20 microseconds, and the crest of the wave can be from 5 to 20 times the normal system voltage [12].

The rating of a piece of electrical equipment or surge protective device is call the Basic Insulation Level, or BIL. The BIL is determined by applying an impulse test and determining the crest value of the voltage wave.

The current industry practice is to select the surge arrester with the lowest conduction voltage to protect the desired equipment, while still having a satisfactory service life when connected to the power system [12]. For example, by examining Table 1 in [12], a design engineer could select a 108 kV or 120 kV MCOV (Maximum Continuous Operating Voltage) rated surge arrester for a 138kV transmission system, which would be 1.36 pu and 1.50pu, respectively, of line-to-neutral voltage.

Thus, an obvious solution to the lightning arrester overvoltage problem is to select lightning arresters that have an MCOV of 1.73pu or higher. This is the current industry practice for high impedance grounded or ungrounded systems, as shown in [12]. For example, the 138kV circuit examined before has the options of a 132kV and 144kV arrester, which is near or above the rated line-to-line voltage. If such an arrester were selected for a substation design, an islanded distribution system with DG would not overload these arresters. The drawbacks to this method is that this leaves the protected equipment more vulnerable to switching surges. Additionally, for existing distribution systems the surge arresters are already installed, and upgrading the arresters to higher MCOV ratings would be expensive and time consuming [3].

Thus, a better approach must be developed that allows the current industry arrester selection process to be continued, but still allows DG integration into distribution systems without incurring the significant additional cost of specialty protection systems for cases in which islanding is not needed or desired.

7.1 Temporary Overvoltages

Temporary overvoltages (TOV) are caused by numerous sources, but for the sake of this paper, distribution systems with connected DG sources are examined to be the cause of the temporary overvoltage. As discussed previously, a permanent line to ground fault on the high side of a delta-wye distribution transformer can cause a TOV of up to 1.73 pu of line-to-neutral voltage, corresponding to nominal line-to-line voltage.

As detailed in [13] and [14], a lightning arrester has four voltage transient stages that it must withstand: impulse or fast-front overvoltages, switching surges or slow-front

overvoltages, temporary overvoltages, and the highest system operating voltage. Industry practice is to clear a transmission-level fault within 20 cycles, with a backup clearing time of 30 to 60 cycles [15]. Thus, a TOV withstand of 1 second is used for the analysis in this paper. According to [12], the maximum withstand rating for a 1 second TOV event is 1.43 to 1.57 per unit of MCOV, depending on the type of lightning arrester. Thus, a distribution system voltage drop of 16% to 30% from nominal in needed to ensure that the lightning arresters are not overloaded. This voltage is taken at the high side of the distribution transformer when just the DG source is supplying the load, and the DG must be disconnected within 1 second to avoid damaging the lightning arresters. However, if the voltage drop on the distribution system is higher when the distribution grid is inadvertently islanded, then the distribution system can remain connected to the transmission system for a longer duration without damaging the lightning arresters. However, it is still advantageous to disconnect the distribution system from the faulted transmission system to avoid other damage to the grid, as well as prevent injury to line workers who may try and repair or remove the cause of the fault.

8 SOLUTION METHODOLOGY

Given the drawbacks to the current methods available to analyze the high-side transformer voltage to determine if the transmission line lightning arresters will be overloaded, a simpler, first-level approach must be developed and tested. After discussion and deliberation, it was decided to create an equivalent network model with the substation as the output node. This allows for a simple calculation of the substation voltages using ohm's law and doesn't require the use of sequence networks, load flow calculations, or differential equations.

The benefits of using the Thevenin's Equivalent Circuit approach is that it is less dependent on the exact load placement locations in the system. Since the exact system load placement is unknown, as explained in section 3, the Thevenin equivalent method is a better choice for the analysis of this problem.

8.1 Equivalent System Impedance

Two methods were used to calculate Thevenin's Equivalent Impedance of the distribution circuit.

8.1.1 Test Current Injection

The first and primary method used to measure the equivalent circuit impedance was injecting a test current and measuring the resultant voltage [16]. The method is as follows: first deactivate the sources by setting their values to zero. This results in a short (zero voltage) for voltage sources, and an open circuit (zero current) for current sources. Then, a test current source is connected to the output node, and the voltage drop from

node one to node two of the current source is measured. Using ohm's law, the system impedance is calculated by dividing the measured voltage by the test injected current.

8.1.2 Voc/Isc

As an alternative method, the open circuit voltage and short circuit current method was used to calculate the system impedance. Instead of deactivating the system sources, they were left connected and set to their nominal values. First, the steady-state system voltage was measured at the output node (the substation). Then, the output node was connected to ground, and the short circuit current was measured. Finally, ohm's law was again used to calculate the system impedance by dividing the open circuit voltage by the short circuit current.

8.2 Voltage Computation

Once the system impedance is calculated, the source voltage and a test load is used to compute the voltage at the output node, i.e. the substation. As shown in later in this thesis, several factors complicate the analysis and prevent an exact implementation of the methods described above. However, modifications are made as described in subsequent sections, and these changes allow for successful implementation and testing of the substation voltage using Thevenin's equivalent circuit method.

9 TEST SYSTEMS

9.1 IEEE 4 Node Test Feeder

The first step in testing the validity of the Thevenin equivalent circuit approach was to examine the transient voltage waveforms to determine if they had significant impact on the voltages seen across the lightning arresters. To verify this, the IEEE 4 node test feeder [17] was modeled and tested in the EMTP transient program, ATP. This model is shown in Figure 9.1 The IEEE 4 node case is a small distribution system consisting of an infinite bus representing the transmission grid, a delta-wye transformer, and two short, nearly symmetrical distribution lines. The main purpose of this distribution system is to test simulation models of transformers when there is an unbalanced load on the distribution system. However, this system worked well to examine the transient voltages caused by a line-to-ground fault on the high side of a delta-wye transformer, as well validate the line-to-line overvoltage on the lightning arresters, as described in section 6.

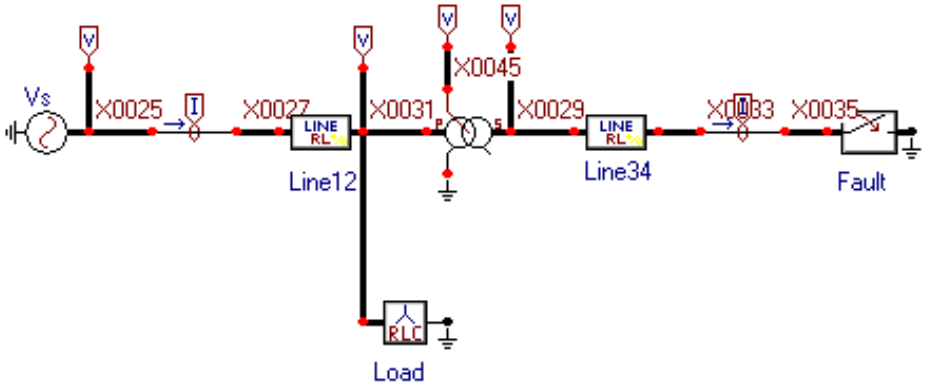


Figure 9.1: ATP Simulation of IEEE 4 Node System Model

Several modifications were made to the system to make it compatible with the desired outcome. First, a DG source was connected on the low side of the distribution transformer and the load was connected to the low side of the transformer, as shown in Figure 9.1. As mentioned in Appendix B, the DG source was first simulated using an ideal voltage source with no source impedance to establish a worst-case post fault transformer high side voltage. During later simulations as summarized in, the ideal voltage source was replaced by a synchronous generator that used all of the default ATP parameter settings, except the voltage was changed to 12.47 kV (line-to-line) and the power rating to 6 MVA to match the power rating of the transformer. The results from these simulations are summarized in section 10.1.1 and detailed in Appendix B.

9.2 IEEE 13 Node Test Feeder

After the transient and steady state voltages were examined using the IEEE 4 node feeder, a larger system, the IEEE 13 node test feeder, was utilized to examine the

effect of DG placement and load values on the substation voltage. The characteristics of the IEEE 13 node feeder [18] are that the system is operated at 4.16kV, the lines are short and relatively highly loaded, and the system has unbalanced loads and shunt capacitor banks. A Simulink model of the IEEE 13 node test feeder is shown in Figure 9.2.

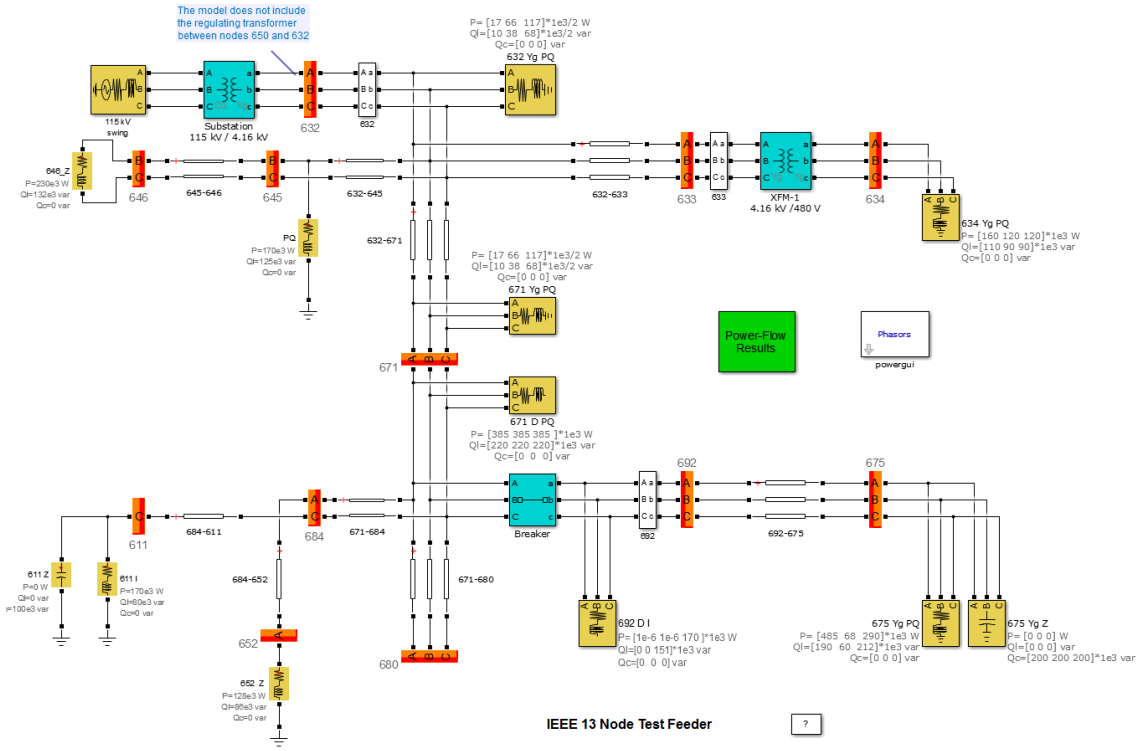


Figure 9.2: Simulink Simulation of the IEEE 13 Node Feeder System

9.3 Solar and Wind SG Source Models

Once the test systems were established, a simple model of power electronic interfaced DG sources was developed. Current industry practice is to model such sources as current-limited (to 1.5 pu) voltage sources to reflect the regulating effect of the power electronics. Thus, a simple model of these sources is a constant power source, since the power electronic interfaces can only supply a maximum amount of power to the system.

Since the distribution system loads in Simulink are modeled as constant impedance loads, a constant power source is created using the following approach: Using the measured current as feedback, a Simulink controlled voltage source is varied to supply constant power to the system. A Simulink model of the proposed system is shown below in Figure 9.3. Since two quantities are fixed, the load impedance Z and the power output of the source, there need to be two degrees of freedom to satisfy Ohm's law and the electrical power equation. Thus, these two equations, P=IV and V=IZ are used to calculate the voltage and current produced by the power-limited DG source. Then, these voltages and currents can be used to determine the voltage drop across the network and thus the voltage at the substation.

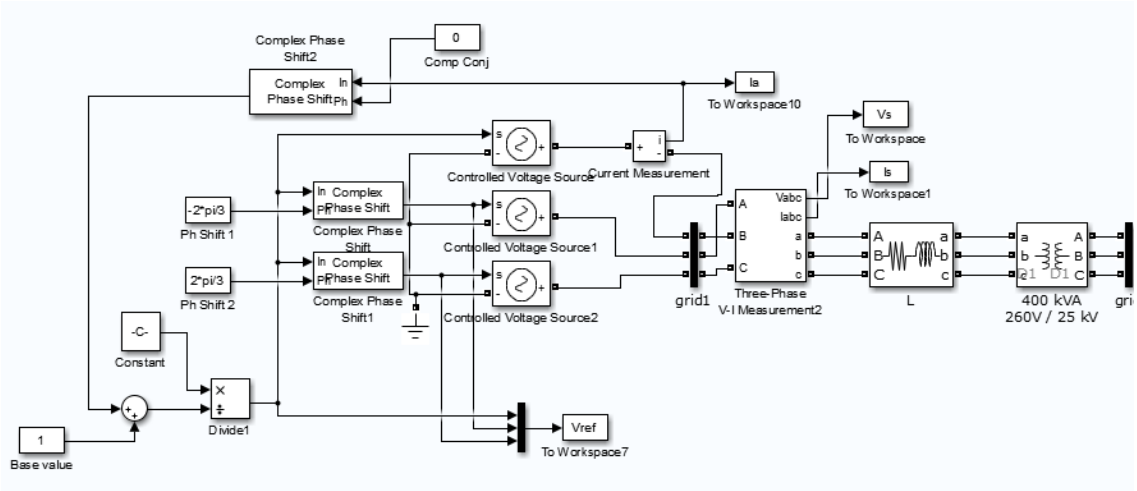


Figure 9.3: Simulink Constant Power Model of Power Electronically Interfaced Generation

9.4 Load Shedding Simulations

Once the substation voltage has been determined for the worst-case scenario of DG generation levels and load levels, the proper protective relaying scheme is selected to properly island the distribution system. This is further discussed in section 11.1. If the load levels are greater than the current DG maximum capacity, load shedding must be utilized to properly match generation and load. This is done using simulated power-frequency droop control for power electronic interfaced generation, and underfrequency relays for loads as further detailed in 11.2.1. Since power electronic interfaced generation has a very fast response time compared to traditional rotating machine based generation [19], a modified load-shedding simulation needed to be created, with a reduced equivalent "inertia" to properly simulate the implemented droop control. Thus, a small synchronous machine example in Simulink was used that has a low inertia, as

shown in Figure 9.4. A phase locked loop was used to determine the system frequency, and once it dropped below a pre-established threshold, the feeder breakers were tripped one at a time until the system frequency stabilized. The results of this simulation are shown in Appendix D.

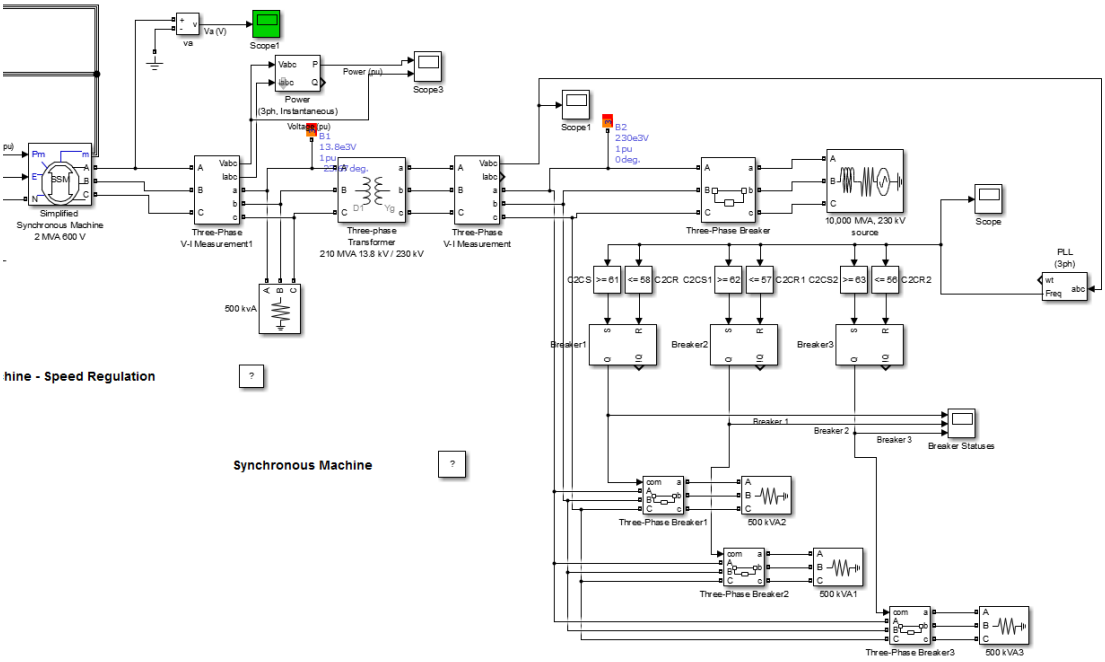


Figure 9.4: Under Frequency Load Shedding Simulation in Simulink

10 RESULTS

First, the voltage transients were examined to determine if they were insignificant enough for a steady-state analysis to fully characterize the system. Then, the Thevenin's equivalent circuit method was used to calculate the substation voltages, and the results are tabulated in this section.

10.1 Voltage Transients

10.1.1 IEEE 4 Node Test Feeder

As discussed in section 9.1, the IEEE 4 node test feeder was used to verify the transient and steady state voltage levels. First, a base case was established for the balanced load specified in [17] by simulating a single-phase to ground fault on the high side of the transformer. The voltage at the high side of the transformer is shown below in Figure 10.1. To aid in viewing the results, I set the peak voltage value of the DG source to be the nominal line-to-line voltage. Thus, the pre-fault voltage seen across the lightning arresters (connected line to neutral) is 24.83 kV, and the post fault voltage is 43 kV, corresponding to the line-to-line voltage of the pre-fault condition. This validates the assertions from [3], [4] that a bolted line to ground fault on an ungrounded (delta) system results in an approximately 1.73 pu (line-to-line voltage) overvoltage to be seen on the non-faulted phases.

Also, the transient voltage spikes in Figure 10.1 are noticeably insignificant, thus showing that a steady-state post fault voltage fully characterizes the behavior of the system. As seen below, there is no overshoot or significant ramping from the pre-fault

to post-fault voltage levels on the system. This is most likely because no fault current flows in the system, as explained in section 6.

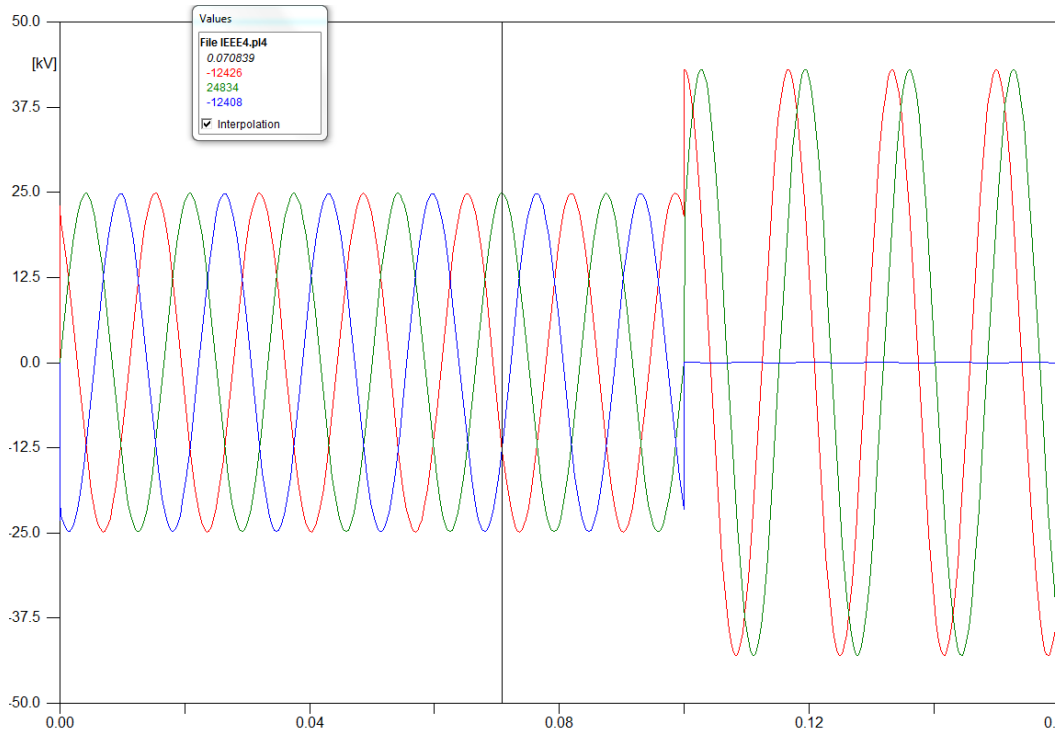


Figure 10.1: Voltage Transients for Single Line to Ground Fault

After this base case was established, several additional simulations were run with varying levels of unbalanced load. As detailed in Appendix A, adding additional load to the system reduced the high side voltage by causing a voltage drop across the distribution lines and the transformer, thus validating that there exists a certain load level or DG source amount that reduces the high side voltage so that the lightning arresters are

no longer overloaded in under 1 second, thus allowing time for the substation breaker to trip and the distribution system to be islanded.

10.1.2 Simulink Verification

The IEEE 4 node feeder was also modeled and simulated in Simulink's Simscape Power Systems. Figure 10.2 below shows the system along with the voltage measurements. The duplicated load configuration from Appendix A was utilized, and a single-line to ground fault was simulated on the high side of the transformer.

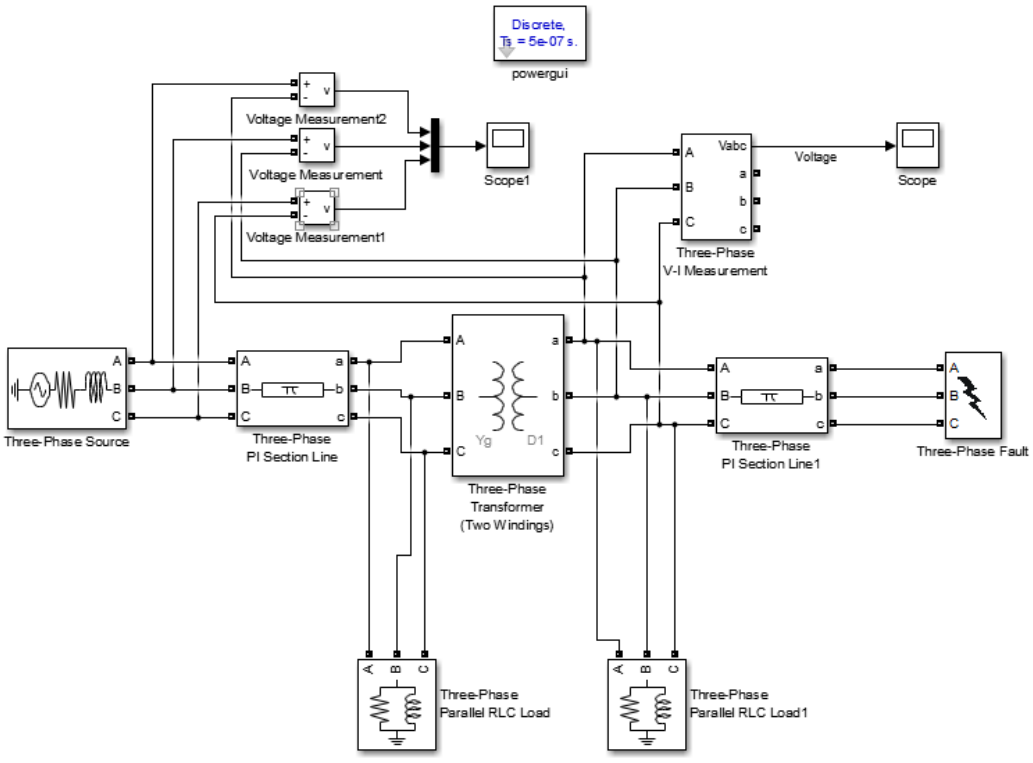


Figure 10.2: Simulink Model of IEEE 4 Node System

10.1.3 IEEE 13 Node Test Feeder

The IEEE 13 node test feeder was utilized to determine the voltage levels at the substation when different types of DG (solar, wind, microturbine) were placed at different locations on the distribution grid. The results for several case studies were tabulated below, however, the application is that a utility company can successfully create a simple model of their distribution systems and analyze the voltage impact of a proposed DG interconnection.

The following observations were made: for a system such as the IEEE 13 node case where the line impedance is several of orders of magnitude below the load impedance, the exact placement of the load on the system is less important than accurately estimating the worst case load levels and amount of imbalance. Also, the asymmetrical distribution lines along with the mutual coupling create problems for the Thevenin equivalent network analysis, but this can be remedied by techniques explained later.

First, the transient voltage waveforms were observed as in the IEEE 4 node system. A single-line to ground fault was simulated on the high side of the substation transformer, and the voltage waveforms for are shown below in Figure 10.3. This verified that the transient voltage spikes are negligible, and established that the steady state voltage values can be utilized to determine the highest voltage seen across the lightning arresters.

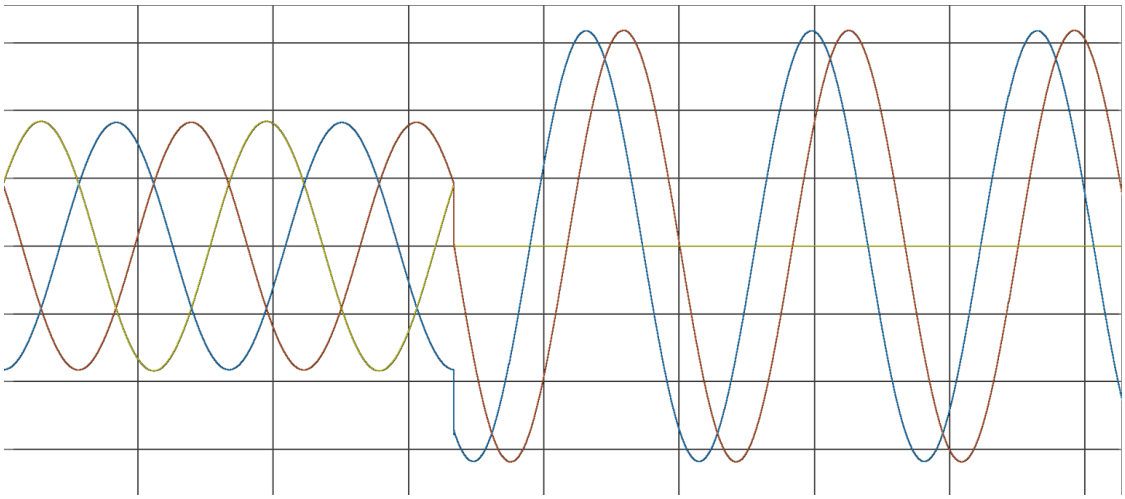


Figure 10.3: Simulink Voltage Transients for Single Line to Ground Fault, IEEE 13 Node System

10.2 Thevenin's Equivalent Circuit

After it was determined that the voltage transients were negligible, the equivalent circuit impedance was determined for the distribution system, and the substation voltages were calculated to determine if the Thevenin Equivalent would produce sufficiently accurate voltages for a first-order approximation of the distribution system voltages. The transformer low-side voltage was calculated, which can be multiplied by $\sqrt{3}$ to get the high side voltage in the case of a high side single line-to-ground fault. This is further explained in section 6.

10.2.1 Test Current Injection: Simulink Approach

To implement the test current injection method described in section 8.1.1, Simulink's Simscape Power Systems impedance measurement block was used. It uses a two-input block with current source Iz connected internally between the two inputs. The

terminals of the impedance to be measured were externally connected between the two inputs, and a 60 Hz test current was injected into the impedance network. When calculating the impedance, the impedance measurement block automatically deactivates the sources as described in section 8.1.1, then divides the voltage measured across the impedance network.

For the IEEE 13 node distribution system, one terminal of the impedance measurement block was connected to the output node (the substation, node 632), and the other terminal was connected to ground, thus measuring the impedance of the distribution system from the reference output node of the substation, "looking into" the distribution network, as shown in Figure 10.4.

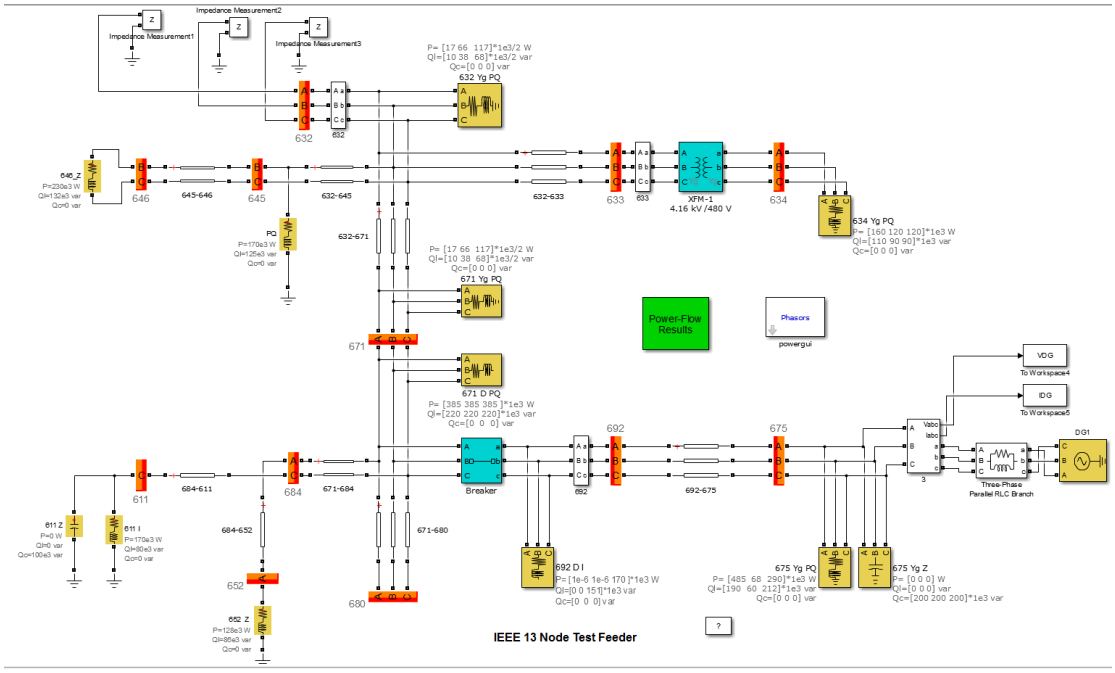


Figure 10.4: System Impedance Measurements of IEEE 13 Node System

However, the impedance measurement block doesn't properly take mutual coupling into account. This was seen when the impedance of only A-phase of the distribution network was measured independently, then three impedance measurement blocks were connected simultaneously to the system. In both cases, the impedance was the same to 13 digits, i.e. when the DG source was connected to node 675, the system impedance in both cases was 0.2352606557 + 0.4431160283i. When there was a substantial imbalanced between the phase load levels, this resulted in inaccuracies in the voltage levels as calculated using the equivalent circuit impedances, which can be remedied, as shown later in the paper.

10.2.2 Voc/Isc: Simulink Simulations

To implement the Voc/Isc method as described in section 8.1.2, a Simulink model was constructed with an example shown in Figure 10.5. The DG source (in this case, a simple model of a microturbine) was left connected to a distribution node, and a 3-phase to ground fault with negligible fault resistance was triggered on the substation node at t= 3 cycles. The Simulink powergui simulation block was set to run in phasor mode, and voltage and current measurement blocks were connected at the substation. The open circuit voltage was recorded from the pre-fault values, and the short circuit current values were measured during the fault period. Because in some cases the current and voltage values had an angle difference of more than 90 degrees, the calculated resistance was negative, i.e. had an angle of more than 90 degrees. As shown later in the results section, this resulted in higher voltage values calculated using the equivalent network approach.

For example, the Simulink model of the IEEE 4 node feeder in section 9.1 gave a calculated impedance of -4.1 + j12.24 ohms. This was because the open circuit voltage was $24.825\angle -0.149$ kV, and the short circuit current was $1924\angle -108.5475$ amps, yielding an impedance angle of 108.39 degrees.

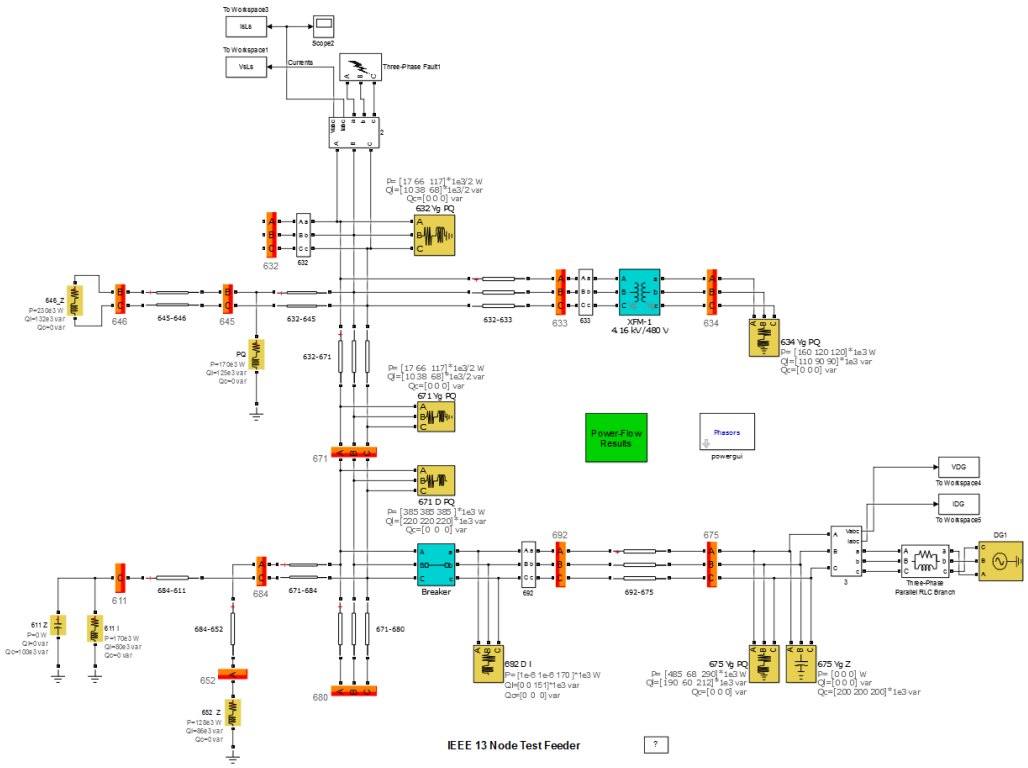


Figure 10.5: Voc/Isc Equivalent Network Measurement Model

10.2.3 Assumptions and Simplifications

The benefit of using the Thevenin's Equivalent method is that it created 3 simple, single-phase, decoupled systems that could be analyzed separately. However, the mutual coupling between distribution lines was computed at one particular instant, and the result was lumped into the phase impedances of each line. For the test current injection method, this resulted in a lower system impedance, as verified by the results later in this paper. This is because the test current method didn't take the mutual coupling into account, as shown in section 10.2.1. Also, for the Voc/Isc method, the mutual coupling was computed for one instant during the 3-phase to ground fault, and thus was not properly considered. However, as shown later in this paper, variations in the load are used to correct for these assumptions and create a more accurate voltage profile.

10.3 Substation Voltages

The IEEE 13 node system is used to test and measure the low-side substation voltages. For the simulations, a 5 kVA microturbine is used as the DG source to match the power rating of the transformer. Based on typical values from [20], the reactance X was set to be 0.17 pu and the X/R ratio is 25. This DG source was connected to nodes 675, 680 and 633, respectively, and the substation voltages are listed in following subsections. Since the sum of the 3 phase total system load, (real load and reactive load minus shunt capacitors) was only 3.74 kVA, the substation voltages are fairly close to 1 pu.

Thus, to further test the effect of the system load being greater than the DG source capacity, the IEEE 13 system was duplicated in both series and parallel to approximate a larger system. For the series duplication, the substation (node 632) of a copy of the IEEE 13 node system was connected to node 680 of the original system, as shown in Figure 10.6.

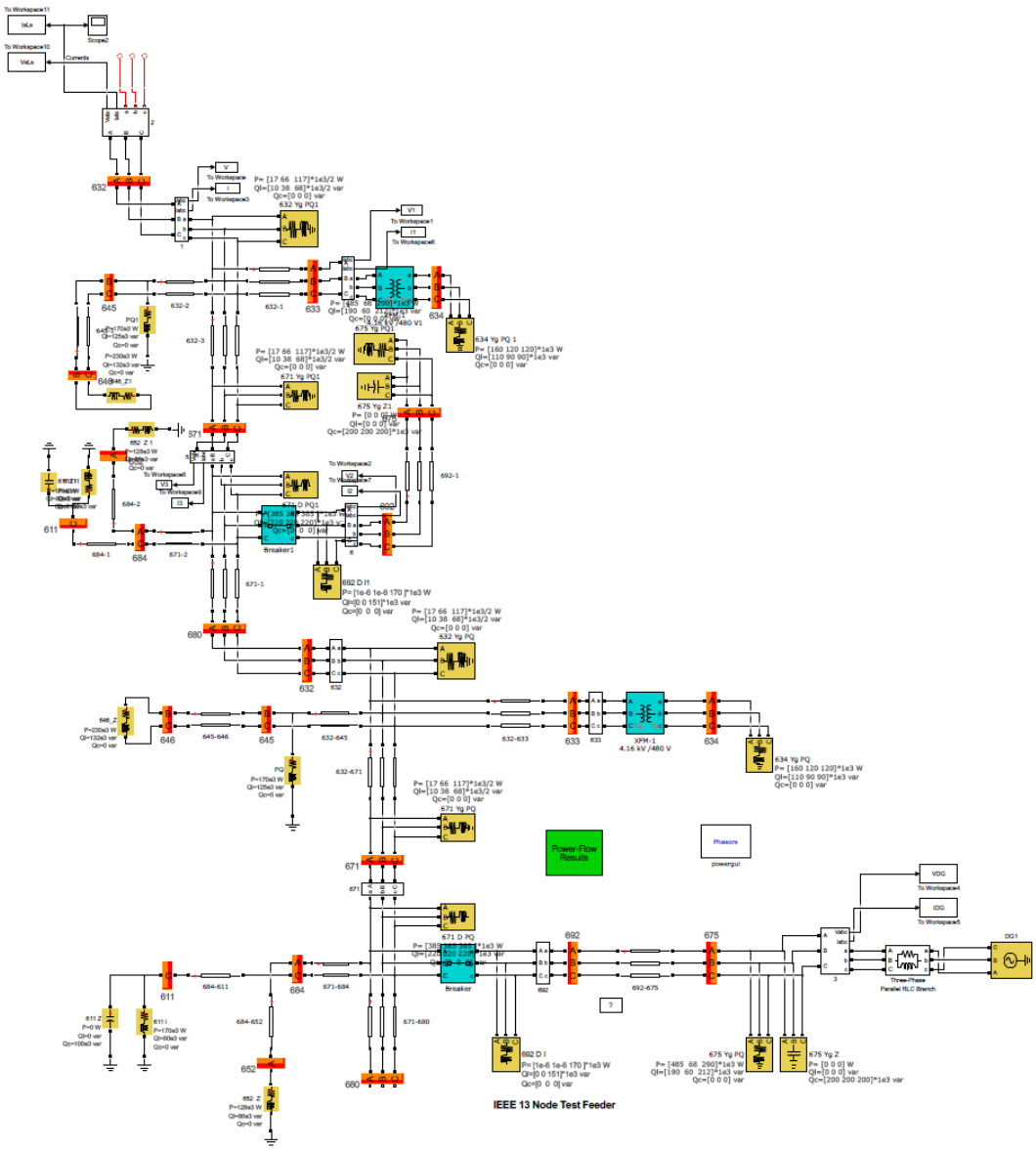


Figure 10.6: IEEE 13 Node System, Series Configuration

The parallel duplication took a copy of the IEEE 13 node system and connected the two substations (node 632) together, thus creating two parallel systems. Since the DG was only connected to the original distribution system, the second parallel system

was treated as a parallel adjacent feeder. For the Thevenin equivalent calculations, the impedance of the parallel system (feeder) was measured using the Simulink impedance measurement tool, and is recorded below in Table 10.1. Also, if such an impedance were connected to the original system's substation, the equivalent power value of the corresponding constant impedance load is also given. Notice the substantial imbalanced between the equivalent powers of phases A and C, and phase B, as will be discussed later in this paper.

IEEE 13 node system	**Phase A**	**Phase B**	**Phase C**
Impedance Without DG	5.0095+1.8523i	7.7655+2.7371i	5.2413+1.8498i
Equivalent Power	3039+1124i	1982+699i	2936+1036i

Table 10.1: IEEE 13 Node System Equivalent Impedances

Another interesting result from the equivalent network approach is the nearly negligible impact of the load location on the feeder with DG on the calculated substation voltage, as detailed later in this paper. This is because the total load per phase is on the order of 12 ohms (magnitude), whereas the phase impedance of the distribution network (with the DG source connected to node 675) is on the order of 0.5 ohms magnitude. The effect of the system load on the measured network impedances can be further observed in Table C.1 in Appendix C. However, this effect is very beneficial and desirable, because the exact locations of the worst-case loads for the actual distribution system to

be simulated are difficult to determine, and thus approximations and combined loads must be used.

To verify the Thevenin equivalent method, an excel spreadsheet was created to calculate the substation voltages for several different DG placement locations, system configurations and load levels. Thevenin's equivalent circuit, shown in Figure 10.7, was simulated, and Ohm's law was utilized to calculate the voltages at the substation. The network impedance was calculated using the methods described in section 8.1, and an equivalent load for the different system configurations was calculated as described below.

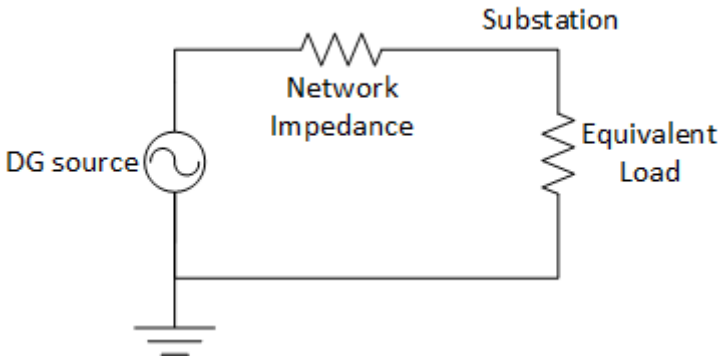


Figure 10.7: Thevenin Equivalent Network Model

For the first 3 test cases, the normal IEEE 13 node system configuration was utilized (Figure 9.2), with the DG source connected to three different nodes, 633, 675

and 680, respectively. The results are shown in the tables of results below. Several values for the equivalent load were used, as summarized in Table 10.2 below.

To compare the accuracy of the Thevenin's equivalent circuit voltages, a complete voltage simulation of the IEEE 13 node system was conducted in Matlab's Simscape Power Systems. The phasor analysis was utilized with the default solver parameters set from the IEEE 13 node system. The results from these simulations are listed in the Measured Voltage columns of the tables of results below.

Equivalent Load values for first 3 cases	**Base Load Configuration (without caps)**	**Base Load Configuration (with caps)**	**Base + Test Load**	**Test Load only**
A-Phase	1175+606i	1175+416i	2675-1016i	1500+600i
B-Phase	1039+627i	1039+465i	2539-1065i	1500+600i
C-Phase	1252+753i	1252+521i	2752-1121i	1500+600i

Table 10.2: IEEE 13 Node System Load Levels for Various Configurations

10.3.1 Original IEEE 13 Node System Configuration

For the first 3 tables (Table 10.3, Table 10.4 and Table 10.5), the first three columns are the calculated voltages when only an equivalent lumped system load was used as the equivalent load in Figure 10.7. The base load configuration was computed by taking the sum of the IEEE 13 node system loads as specified in [18] and connecting them directly to the substation node as part of the Equivalent Load in Figure 10.7. Two different configurations were used: one subtracting the connected shunt capacitor values

from the total reactive power load (with caps), and the other load configuration did not consider the effects of the connected capacitors on the system (without caps).

Then, a balanced test load (last column of Table 10.2) was connected to the substation and added to the equivalent load, and the measured network impedance was used as the network impedance. The results are listed in the last 3 columns of the tables of results.

The results were inconclusive as to whether the system load with or without the connected capacitors yielded a more accurate result, as seen from the error percentages in the first 3 tables. However, since the total system load (3.74 kVA) was below the DG maximum capacity (5 kVA) and the total including the test load (8.59 kVA) was only 1.72 pu of the DG capacity, the substation voltage for the most extreme scenario experience a 5% maximum drop. These results indicate that the lightning arrestors would be overloaded in less than 1 second, so more advanced protective relaying strategies would be needed to ensure the distribution system is islanded quickly to avoid overloading the lightning arresters, as detailed in section 11.1.

Also, there exists a slight imbalance in the system loads as seen in Table 10.2. However, since the maximum imbalance is between phases B and C, and is only 250 VA (18%), the voltage difference between the three phases is fairly small. However, once the load imbalance becomes more pronounced, the discrepancies between the measured and calculated voltages become greater.

Thus, for a system without a large magnitude of load imbalances such as the IEEE 13 node system with load impedances much greater than line impedances, the

Thevenin equivalent method is an excellent approximation for determining the substation voltages. This saves time and resources since a full sequence network model or transient model doesn't need to be constructed.

Calculated Substation Voltage	**Base Load Config-uration (without caps)**	**Base Load Config-uration (w/ caps)**	**Measured Voltage (no test load)**	**Base + Test Load**	**Test Load only**	**Meas-ured Voltage**
A-Phase	0.990	0.991	*0.981*	0.982	0.988	0.972
B-Phase	0.991	0.992	*0.989*	0.983	0.989	0.980
C-Phase	0.988	0.990	*0.974*	0.977	0.988	0.964
Error						
A-Phase	0.85%	0.98%		0.96%	1.57%	
B-Phase	0.22%	0.32%		0.28%	0.87%	
C-Phase	1.44%	1.60%		1.32%	2.44%	

Table 10.3: DG Source Connected to Node 633

Calculated Substation Voltage	**Base Load Config-uration (without caps)**	**Base Load Config-uration (w/ caps)**	**Measured Voltage (no test load)**	**Base + Test Load**	**Test Load only**	**Measured Voltage (test load)**
A-Phase	0.969	0.974	*0.978*	0.940	0.965	*0.956*
B-Phase	0.972	0.976	*0.969*	0.943	0.967	*0.952*
C-Phase	0.966	0.972	*0.973*	0.940	0.967	*0.951*
Error						
A-Phase	0.92%	0.46%		1.62%	1.00%	
B-Phase	0.25%	0.63%		0.91%	1.54%	
C-Phase	0.65%	0.11%		1.19%	1.65%	

Table 10.4: DG Source Connected to Node 675

Calculated Substation Voltage	**Base Load Config-uration (without caps)**	**Base Load Config-uration (w/ caps)**	**Measured Voltage (no test load)**	**Base + Test Load**	**Test Load only**	**Measured Voltage**
A-Phase	0.964	0.970	*0.967*	0.931	0.960	*0.942*
B-Phase	0.967	0.972	*0.975*	0.934	0.962	*0.956*
C-Phase	0.961	0.968	*0.961*	0.931	0.962	*0.938*
Error						
A-Phase	0.33%	0.30%		1.18%	1.89%	
B-Phase	0.80%	0.29%		2.21%	0.63%	
C-Phase	0.01%	0.71%		0.70%	2.61%	

Table 10.5: DG Source Connected to node 680

10.3.2 Expanded IEEE 13 Node System Configurations

After the normal IEEE 13 node system was tested, the system was expanded to determine the effect of having load values greater than the DG supply capacity, as well as examining the effects of a larger system on the substation voltages. For the remaining scenarios, the DG source is connected to node 675, and the systems are connected in series and/or parallel as described in the beginning of this section.

For the next 5 system configuration cases, first the base load configuration was tested and displayed in the second and third columns. The base load configuration included the combined lump system load connected directly to the substation (i.e. modeled as the equivalent load in Figure 10.7) plus the equivalent impedance/power of any connected duplicated parallel IEEE 13 node systems (adjacent feeders). For example, for the Series Parallel 2 configuration, there are two IEEE 13 node systems connected in series, and two additional systems connected in parallel to the main

substation. Thus, the base load configuration would be two times the combined load of the IEEE 13 node system, added to two times the equivalent impedance/power of the IEEE 13 node systems connected in parallel at the substation. A complete table of the equivalent power values for each configuration case is given in Appendix C.

As can be seen in the tables of results below, there are non-negligible errors between the calculated voltages using the base load configurations and the Simulink measured voltages. This is because of the larger system load imbalances combined with the fact that the Thevenin Equivalent method does not properly account for the mutual coupling, as explained in section 10.2. The worst case is the Series Parallel 2 case in Table 10.10, which has a load imbalance of 2.46 kVA between phases B and C, which is a 32% imbalance. Using only the impedance of the series system, this results in a phase B voltage error of 9%.

To observe a trend in these errors, additional simulations were conducted by varying the value of the equivalent load impedance in the Thevenin equivalent circuit. The results are displayed in the following 6 tables below (Table 10.6, Table 10.7, Table 10.8, Table 10.9, Table 10.10 and Table 10.11). The load values were decreased by either removing a copy of the lump load (lump load -1), or removing one of the connected parallel IEEE 13 system impedances (equivalent system -1). This was performed in successive iterations until the B-phase voltage had overshot the measured value. For example, in the Series Parallel 2 configuration, Table 10.10, first one, then a second equivalent lump load were removed from the Thevenin load value and the calculated voltages were recorded in columns 3 and 4, respectively. Then, beginning

with the regular base system, first one, then the second parallel IEEE 13 system equivalent impedance was removed from the Thevenin load, and the calculated voltages were recorded in columns 5 and 6. Finally, the substation voltage was calculated for only one IEEE 13 lump load and one parallel adjacent feeder connected to the substation, and the result was recorded in column 7.

Calculated Substation Voltage	**Base Load Config. (with caps)**	**Equivalent System (lump load -1)**	**Measured Voltage (no test load)**	**Base + Equiv. Sys + Test load**	**Equiv. Sys + Test Load**	**Measured Voltage (test load)**
A-Phase	0.909	0.933	*0.920*	0.878	0.901	*0.899*
B-Phase	0.935	0.958	*0.950*	0.905	0.927	*0.932*
C-Phase	0.913	0.939	*0.911*	0.884	0.909	*0.892*
Error						
A-Phase	1.18%	1.42%		2.28%	0.25%	
B-Phase	1.52%	0.91%		2.88%	0.53%	
C-Phase	0.27%	3.13%		0.89%	1.89%	

Table 10.6: Parallel 1 Configuration, DG Connected to Node 675

Calculated Substation Voltage	**Base Load Config. (without caps)**	**Base Load Config. (with caps)**	**Lump load -1 (w/o caps)**	**Lump load -1 (w/caps)**	**Measured Voltage (no test load)**
A-Phase	0.882	0.897	0.938	0.947	*0.895*
B-Phase	0.891	0.904	0.943	0.951	*0.929*
C-Phase	0.873	0.891	0.933	0.943	*0.880*
Error					
A-Phase	1.44%	0.30%	4.84%	5.84%	
B-Phase	4.03%	2.60%	1.55%	2.36%	
C-Phase	0.79%	1.24%	6.04%	7.22%	

Table 10.7: Series System Configuration, no Test Load

Calculated Substation Voltage	**Base (w/caps) + Test Load**	**Base (w/o caps) + Test Load**	**Test Load only**	**Measured Voltage (test load)**
A-Phase	0.837	0.824	0.930	*0.854*
B-Phase	0.846	0.817	0.933	*0.894*
C-Phase	0.834	0.819	0.933	*0.843*
Error				
A-Phase	2.00%	3.54%	8.89%	
B-Phase	5.35%	8.60%	4.35%	
C-Phase	1.08%	2.89%	10.73%	

Table 10.8: Series System Configuration, with Test Load

Calculated Substation Voltage	**Base Load Config. (without caps)**	**Base Load Config. (w/ caps)**	**Lump load -1**	**Lump load -2**	**Equivalent System -1**	**Measured Voltage (no test load)**
A-Phase	0.773	0.784	0.824	0.868	0.897	*0.79127*
B-Phase	0.821	0.832	0.872	0.916	0.904	*0.88873*
C-Phase	0.775	0.789	0.833	0.880	0.891	*0.77364*
Error						
A-Phase	2.36%	0.95%	4.18%	9.72%	13.42%	
B-Phase	7.63%	6.42%	1.83%	3.12%	1.77%	
C-Phase	0.23%	1.94%	7.61%	13.80%	15.11%	

Table 10.9: Series Parallel 1 System, Using Measured Impedance of the Series System

Calculated Substation Voltage	**Base Load (with caps)**	**Lump load -1**	**Lump load -2**	**Equiv. System -1**	**Equiv. System -2**	**Lump load -1 Equiv. System -1**	**Measured Voltage (no test load)**
A-Phase	0.691	0.720	0.760	0.784	0.897	0.824	*0.704*
B-Phase	0.767	0.798	0.842	0.832	0.904	0.872	*0.844*
C-Phase	0.704	0.734	0.780	0.789	0.891	0.833	*0.688*
Error							
A-Phase	1.81%	2.22%	7.94%	11.30%	27.45%	17.06%	
B-Phase	9.15%	5.48%	0.31%	1.50%	7.12%	3.33%	
C-Phase	2.21%	6.66%	13.24%	14.56%	29.36%	20.93%	

Table 10.10: Series Parallel 2 Configuration, Using Measured Impedance of the Series System

Calculated Substation Voltage	**Base Load (with caps)**	**Lump load -1**	**Lump load -2**	**Equiv. System -1**	**Equiv. System -2**	**Lump load -1 Equiv. System -1**	**Measured Voltage (no test load)**
A-Phase	0.730	0.756	0.791	0.811	0.910	0.846	*0.704*
B-Phase	0.786	0.815	0.854	0.845	0.912	0.882	*0.844*
C-Phase	0.736	0.764	0.803	0.812	0.903	0.851	*0.688*
Error							
A-Phase	3.66%	7.32%	12.26%	15.18%	29.20%	20.20%	
B-Phase	6.92%	3.52%	1.09%	0.10%	8.05%	4.49%	
C-Phase	6.96%	11.02%	16.71%	17.98%	31.14%	23.58%	

Table 10.11: Series Parallel 2 Configuration, Using Measured Impedance of the Series Parallel 2 System

Once the amount of load is varied following the method described above, an interesting pattern emerges: when each phase load is decreased by the amount of imbalanced between phases B and C in the base case, the resulting B-phase voltage is almost identical to the calculated voltage. For example, in the Series Parallel 2 case, the imbalance between phase B and C is 2.46 kVA, which is approximately 32%. Thus, the lump load -2 case (removing the equivalent lump load from the Series portion of the IEEE 13 node feeder) is examined, since the load on each phase is reduced by approximately 2.4 kVA. In this case, the B-phase voltage error is only 0.31%. This correlation holds true for all cases except series 2, since the reductions in load didn't properly match with the imbalance between phases. The results for the load reduction method are shown below in Table 10.12.

Configuration	Base Case B-C Imbalance (mag)	Error	Load reduction amount	New Error
Parallel 1	1230.57	1.52%	1135.84	0.91%
Series Parallel 1	-1368.21	7.63%	1267.82	1.77%
Series Parallel 2	2460.58	9.15%	2272.26	0.31%

Table 10.12: Results of the Load Reduction Method

Thus, the base loading case is used to determine the voltage of the phases that are the most heavily loaded, since for all cases except for the Series Parallel 2 configuration, the base loading case results in a voltage error of less than 2%. To determine the voltage of the lightest loaded phase, the method described above, the equivalent load reduction method, is utilized.

From the results in the tables above, the lowest phase-B voltage is the Series Parallel 2 case, at 0.84 pu. This is only a voltage drop of 16%, which is not above the upper range of the safe voltage drop of 30%, thus the lightning arresters for this system might be overloaded in under one second, which still would require a more advanced protective relaying strategy with faster islanding times. However, if the DG source was changed from a microturbine to a power electronic interfaced generation source such as PV or wind, the voltage results would change substantially, since the equivalent load is 24.4 kVA for the three phases combined. This is because the power electronically interfaced generation is limited to 1.5 pu of the maximum power rating of the inverters, and only for a short duration.

In this case, instead of using a fixed voltage value for the Thevenin equivalent circuit, a fixed power source of 1.5 times the rated DG source can be used. The voltage

and current of the DG source is calculated per the method in section 9.3, then these values are used to calculate the substation voltage using Ohm's law and basic circuit analysis.

10.3.3 Error vs. Imbalance

To quantify the analysis above, two different graphs were created, load magnitude vs. error and load imbalance vs. error. Figure 10.8 shows the load magnitude and the effect on error for phases A and C, while Figure 10.9 shows the graph for phase B. As seen from the first figure, at lower loading levels of phase C, there is no clear correlation between increasing load and calculated voltage error. For phase A, there is a fairly clear upward trend in the error % as the load increases. However, for phase B, once the load increases beyond 3pu (3 phase base load is 5 kVA, so single phase base load is 1.67 kVA), the error increases and stays higher. Also, as seen from Figure 10.8, the calculated voltage error is below 2.5% for all cases, and this is most likely due to the low imbalance between phases A and C, as seen in Figure 10.11.

Figure 10.8: Per Phase Load vs. Error % for Phases A and C

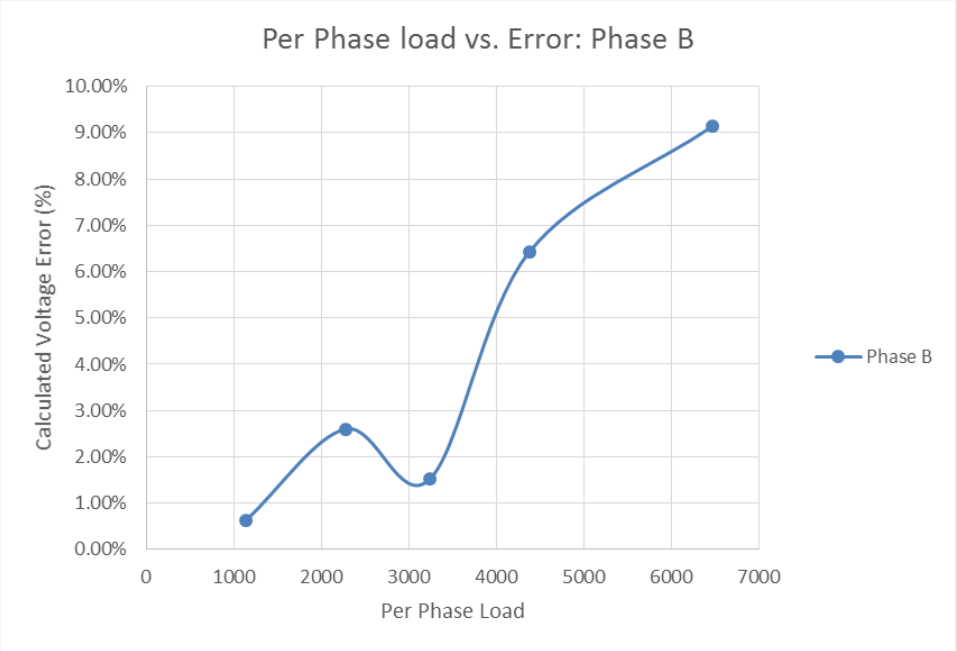


Figure 10.9: Per Phase Load vs. Error % for Phase B

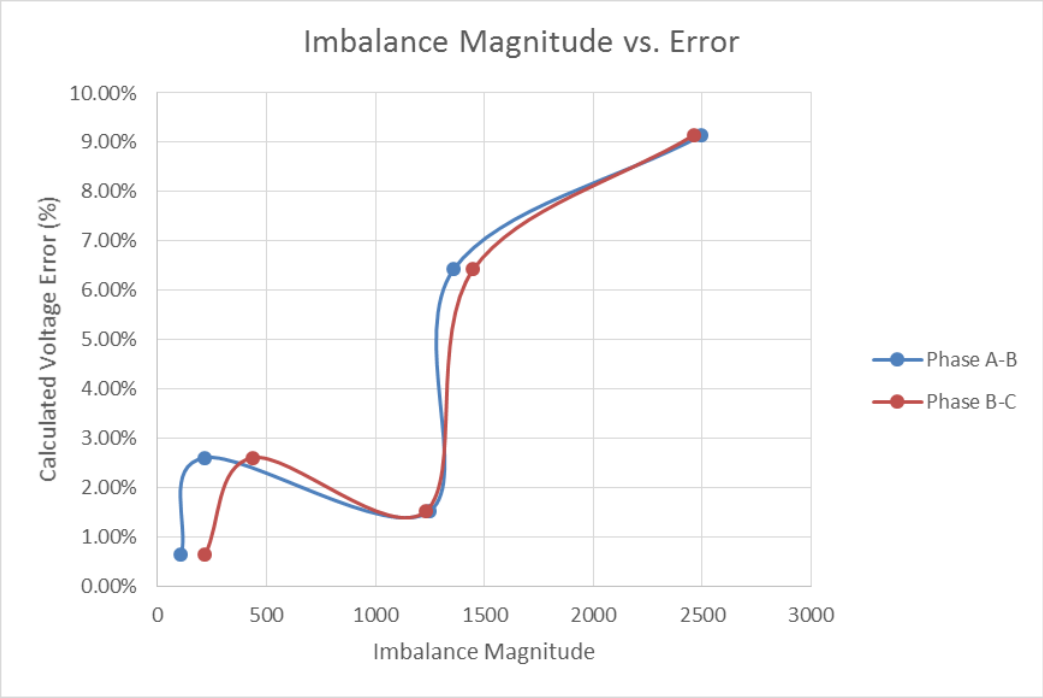


Figure 10.10: Imbalanced Magnitude vs. Error % for Phases A-B and B-C

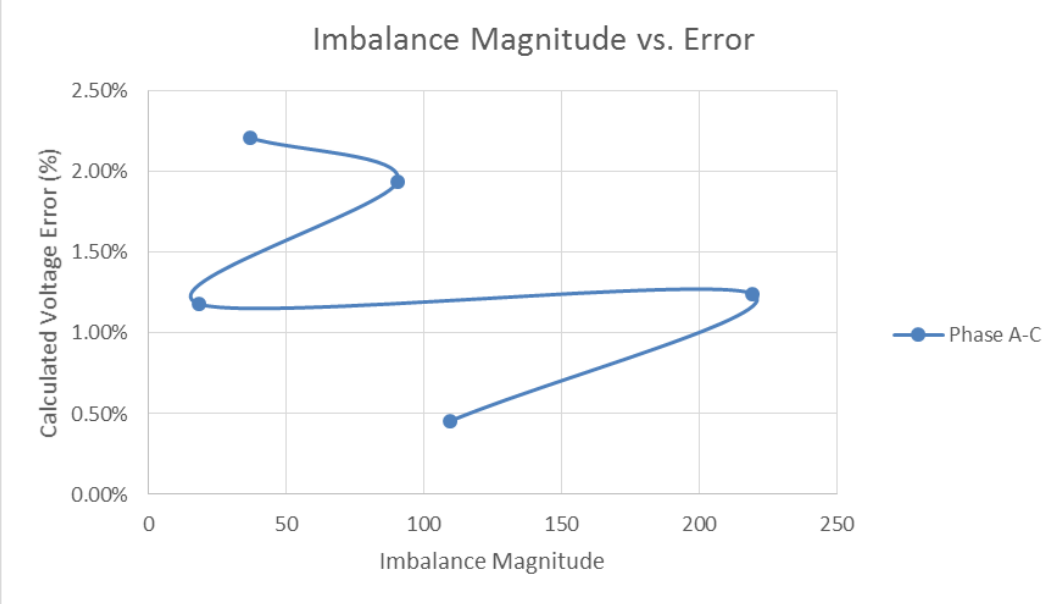


Figure 10.11: Imbalanced Magnitude vs. Error % for Phase A-C

Thus, for the first 5 test cases, it is fairly clear that the lightning arresters would overload in less than one second, thus the faster protective relaying scheme would be necessary. However, the last 2 test cases, Series Parallel 1 and Series Parallel 2, are not as conclusive, since they fall within the 10-21% voltage drop range. Also, as indicated by the figures above, these cases have a higher error percentage than the other cases, due to the high system load and imbalance. Thus, a more in-depth system study would need to be performed for these cases, or the faster relaying scheme could also be used.

11 PROBLEM SOLUTIONS

For a proposed DG capacity level and worst case load estimate, the Thevenin's equivalent method above will determine the worst-case substation voltage, which can be used to determine the transformer high-side voltages. This will indicate the worst-case overvoltage that the lightning arresters will experience. If the magnitude of the overvoltage is above the withstand rating of the particular arresters, a faster protection scheme will need to be used to island the distribution grid, as detailed below. However, if the DG and load levels result in a low enough substation voltage, then a simple overvoltage relay may be used to detect the fault, and island the distribution grid, as detailed below. This will not require many modifications to the distribution system protection settings, since many substation relaying schemes already include over or under voltage protection.

11.1 Protective Relaying Strategies

According to [2], there are three proposed strategies to successfully disconnect the distributed generation from the distribution system when there is a single line to ground fault present.

- "Wait for the utility source breaker to open, and trip generation with islanding protection at the point of interconnection.
- Apply fault detecting protection at the distributed generation point of interconnection to trip generation, or the interconnection breaker, for line faults.

- Transfer trip the distributed generation from the utility source substation via a communications link."

11.1.1 Using Communication Channel to Transfer Trip DG Source

One method currently used in industry is to install a high-speed communication channel between the substation and the DG source for successful high-speed tripping of the DG. This is shown below in Figure 11.1 [2]. The undervoltage fault detection method described in section 11.1.3 is utilized to detect the initial transmission line fault before the line-end breakers open. However, rather than island the distribution system as proposed in section 11.2, the undervoltage relay in the substation issues a direct transfer trip command to the DG interconnection breaker. This trips the DG source for all transmission-level faults, regardless of whether the fault is temporary or permanent. Also, as explained in section 3, there is currently no method implemented to determine whether the proposed DG will overload the lightning arresters, thus the transfer trip signal is issued regardless of the DG capacity. Another problem with this method is that the additional communication channel can be expensive, especially if the DG source is located at a substantial distance from the substation.

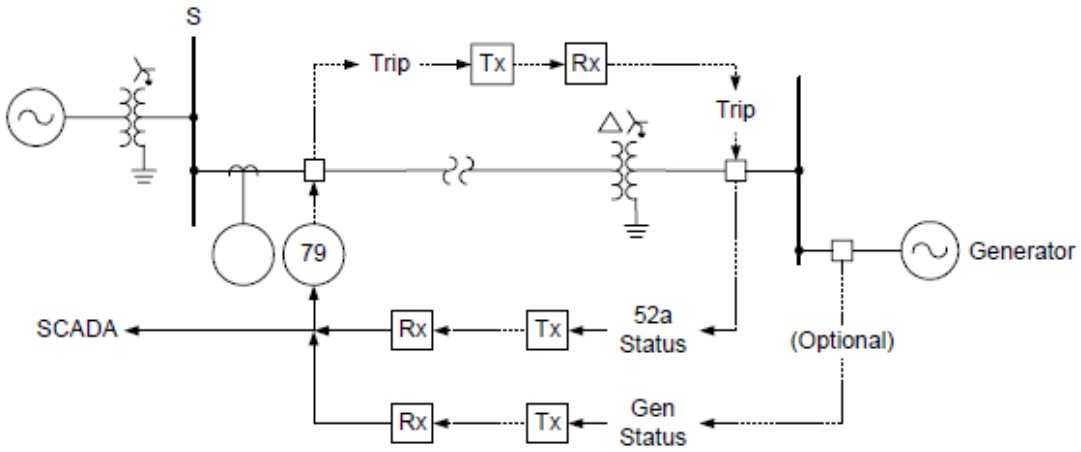


Figure 11.1: Tripping DG Using Communication Channel (Reprinted with Permission from [2])

11.1.2 Use Existing Anti-Islanding Protection

Another possible method of protecting the lightning arresters is to rely on the DG source's anti-islanding relaying schemes. This usually relies on a large mismatch between the distributed generation output and the distribution grid load, and uses an under or over frequency relay to trip the DG source. The clearing times for frequency deviations are detailed in Table 8 in [21]. Also, reverse power relays may be added to supplement the under/overfrequency and voltage relays [2].

One problem with this method are that it makes it impossible to achieve the desired goal of islanding the distribution grid to increase reliability and decrease unnecessary DG tripping. Another problem is that this method doesn't work for distributed generation that exports power to the distribution or transmission grid. Finally, the clearing time of 0.16 seconds is not fast enough to prevent the lightning

arresters from overloading as detailed in sections 7 and 7.1. Thus, another method will need to be considered.

11.1.3 Fault Detection at the Point of Interconnection

As detailed in [2] and shown in Figure 11.2 below, fault detection may be placed at the point of interconnection (POI), and may include overcurrent relays, phase current unbalance, phase voltage unbalance, phase undervoltage, or phase overvoltage. As detailed below, this method will be utilized to detect the presence of the fault. However, instead of directly tripping the DG source as suggested by [2] or as currently implemented in industry practice, the distribution grid will be islanded, as detailed in section 11.2.

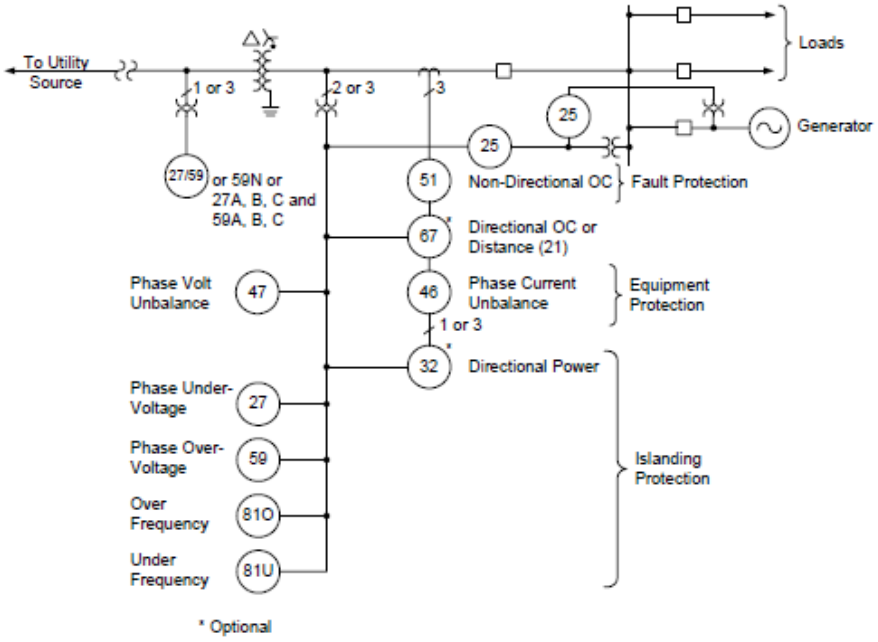
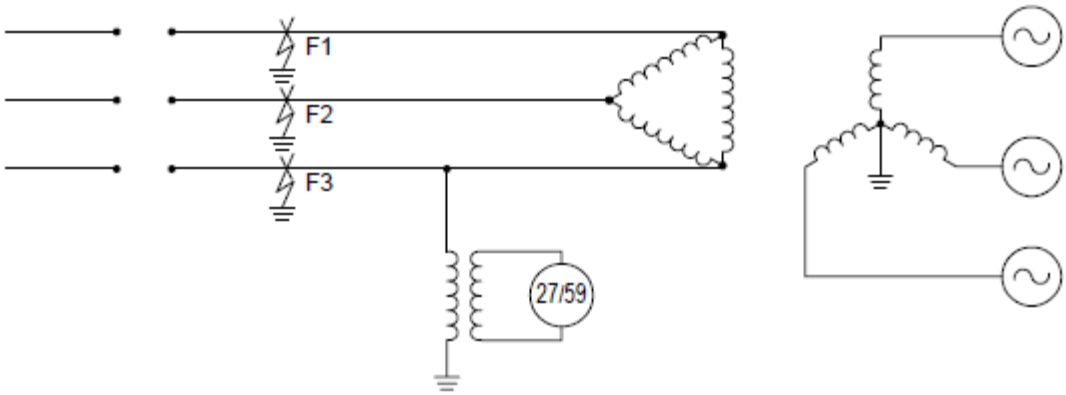


Figure 11.2: Fault Detection Relaying One-Line (Reprinted with Permission from [2])

To properly detect the line to ground fault, over/under voltage relays are installed on the high side of the delta-wye transformer. One example is to install a single voltage transformer, as shown in Figure 11.3. To detect the onset of the fault, an undervoltage threshold (an example of 50 % is used in [2]) is set. Thus, before the transmission line-end breakers open, the transmission line fault voltage will drop below this threshold. For proposed DG installations that result in lightning arrester overload in under 1 second, the distribution grid is islanded when the transmission fault is initially detected, before the line-end breakers trip. This will keep the lightning arresters from overloading, since they would fail within a few cycles of the line-end breakers opening. As detailed in section 11.2, the distribution grid will island, then load shedding schemes will be utilized to properly balance the DG supply and the load levels.



	27	59
No Fault	—	—
F1	—	X
F2	—	X
F3	X	—

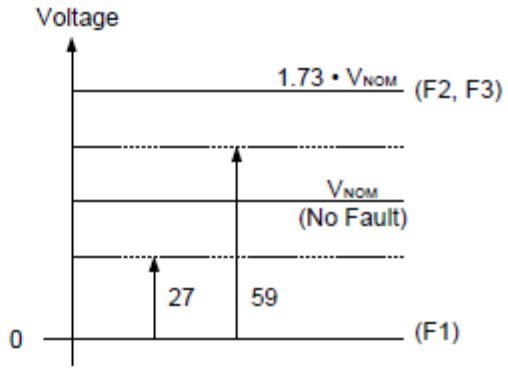


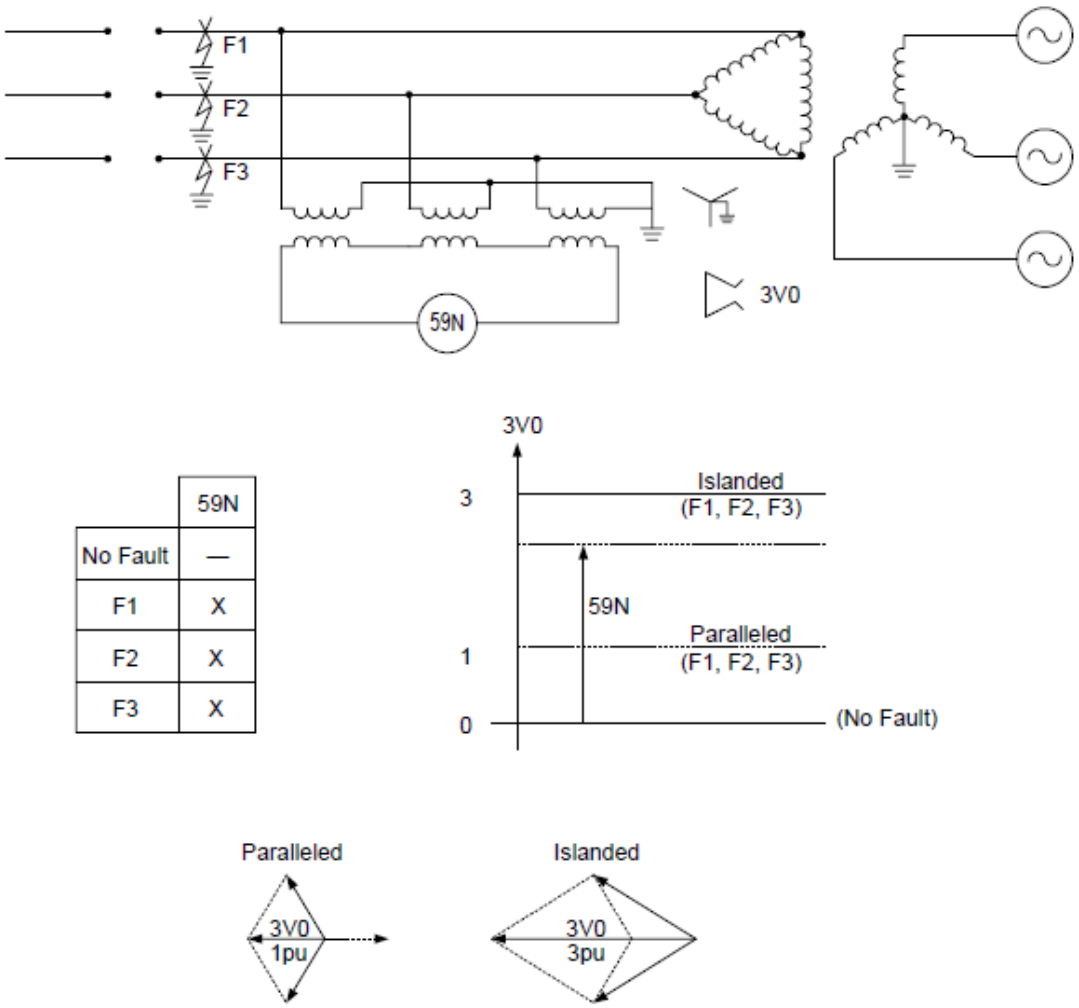
Figure 11.3: Fault Detection Using a Single Voltage Relay (Reprinted with Permission from [2])

For DG capacity levels that result in lightning arrester overloading times of greater than 1 second, or don't overload the lightning arresters at all, an overvoltage threshold (for example 130% in [2]) is set. Once the line-end breakers open, the voltage on the high side of the transformer will rise to the level calculated by the Thevenin equivalent method. This overvoltage will be detected by the relay, and the substation breaker will trip, islanding the distribution system and protecting the lightning arresters. A time delay will be implemented to allow temporary faults to clear and the transmission

line-end breakers to reclose before attempting to island the distribution system. For a permanent fault, even if the lightning arresters won't overload for any finite amount of time, the distribution grid should still be islanded to disconnect the distribution system and DG from the faulted transmission line. This will allow line workers to safely repair the fault without the DG still being connected to the transmission line.

However, the problem with using only one VT connected to the high side of the transformer is that initial fault detection is only possible for the phase with the connected VT, and the overvoltage is only detected if a phase without the VT is faulted. There are several solutions to this problem, including installing 3 separate VTs, or using 3 VTs connected in a broken delta configuration as shown in Figure 11.4 and described in [2]

The benefits of the proposed method are that it doesn't require the installation of a high-speed communication channel to transfer trip the DG, and that temporary faults will at most island the distribution grid instead of tripping the DG. This will allow the distribution grid to continue to operate with the DG supplying part to all of the connected load, increasing the reliability of the system.



	59N
No Fault	—
F1	X
F2	X
F3	X

Figure 11.4: Fault Detection Strategy Using Multiple Voltage Relays (Reprinted with Permission from [2])

11.2 Islanding Strategies

Currently, the IEEE standard 1547 prohibits distribution system islanding [21], thus a revision to the standard would be necessary before a full distribution system islanding approach to lightning arrester overloading could be implemented. This could prove difficult, since the revision and approval process for IEEE 1547 is long and

difficult, and the original standard itself almost wasn't approved. In the case where islanding is not desired, the Thevenin equivalent analysis method can still be used to determine the appropriate protective relaying strategy for protecting the lightning arresters, preventing utility companies from installing overly expensive equipment, as discussed in sections 2 and 3. Then, instead of islanding the distribution system, the DG source could be either tripped via a transfer trip signal, or allowed to trip using its own anti-islanding protection, as described in section 11.1.

However, if distribution system islanding is permitted and desired, once the substation voltage for a proposed DG source integration has been determined and the proper protective relaying scheme has been selected, a sufficient islanding strategy must be implemented. In order to successfully island the distribution grid and operate independently from the transmission grid, the following procedure needs to be followed. First, the substation breaker needs to be tripped quickly enough to not overload the lightning arresters as detailed in section 11.1. Then, the generation and load need to be balanced in order to keep the frequency within the region specified by [21]. This is commonly realized by load shedding. Finally, the DG source needs to be controlled such that the output set point tracks with the load and continues to match the load levels. Each of these steps are described in subsequent sections.

11.2.1 Load Shedding

Since the distribution grid will most likely not have electrical storage such as batteries, the islanded distribution grid will not be a full microgrid as defined in [22]. However, as detailed in [23], a microgrid can operate without storage provided that the

DG sources are dispatchable and capable of meeting the distribution grid load. This is true for the cases of DG sources such as microturbines, fuel cells, or solar or wind with adequate storage. However, for the case where there is only power electronically interfaced generation that is not dispatchable, load shedding techniques such as the ones described in [19] can be utilized.

As simulated in section 9.4 and Appendix D, a basic load shedding algorithm is utilized as follows. An underfrequency and/or undervoltage relays are utilized to determine when there is a mismatch between generation and load. If the frequency goes below a certain threshold, loads are tripped at the recloser or feeder breaker level to reduce the mismatch between generation and load. However, there still remains a small power mismatch, and the generation control algorithms described in section 11.2.2 will fully restore the balance between generation and load.

More sophisticated load shedding techniques have been proposed by various authors, and some of these techniques could be utilized depending on the DG source, distribution grid configuration, availability of communication channels, and number of installed distribution level PMUs.

For example, [24] suggests using the slope of the voltage amplitude and Idpu to determine the imbalance between the DG source and the load. However, this paper only discusses intentional islanding, and it is unclear if this method would work for distribution grids that have already inadvertently islanded.

If distribution level PMUs are installed in the distribution grid, [25] suggest using the high-resolution data from the PMUs to determine the rate of change of frequency to

determine the load and generation power mismatch. First, a stability assessment is conducted to determine if the distribution grid can be safely operated in islanded mode, as well as to aid in determining the proper amount and locations of the load to be shed.

However, this method relies on using a centralized control center to conduct the stability assessments and issue the load shedding commands and the communication channels and computation delays of this control center may be inadequate to keep the distribution system stable during islanded operation. If a centralized control method was desired, [26] provides additional background on centralized control methods as well as information on how to properly select the communication channel.

The method that appears most promising is suggested in [27], which combines underfrequency and undervoltage relaying for increased reliability and precision of load shedding. Additionally, continuous load monitoring is suggested to optimize the load shedding, and may be performed at a central location, or locally at the underfrequency/voltage relays.

As a supplement to this method, if a centralized approach is used, the historical DG supply levels before islanding may be used along with short and long-term estimates of the capacity if the DG is a renewable source. This information could be used to properly determine the DG operating margin, and when combined with the measured load levels, could be used to optimize the selection of load shedding.

11.2.2 Frequency-Droop Control

Before the distribution grid islands, the DG source is operating at its maximum power output to maximize the revenue generated from selling power to the grid. Any

power imbalance between the DG source and distribution grid load is supplied or absorbed by the transmission grid. However, when the distribution grid islands, this imbalance needs to be corrected. As detailed above, load shedding is utilized to resolve the large mismatches between generation and load, especially when the DG supply levels are below the load levels. However, once the load shedding schemes finishes operating, the control of the DG source needs to be changed from maximum PQ output to a voltage control mode [24] so the DG source can match the load.

For synchronous generators that already include voltage regulation and frequency control, this load and generation matching is automatically performed, assuming the constraints on ramp rate and maximum and minimum generation levels are met. For a combined heat and power (CHP) plant in [28], an automatic voltage regulator is used to adjust the rotor field excitation current to properly control the output voltage of the generator. However, since CHP plants operate at constant power factor mode, frequency control will need to be used, which is implemented through a turbine governor.

The basics of a turbine governor are as follows: when the load power increases, the rotational speed of the generator slows down to maintain conservation of power, since$P_m = T\omega = I\alpha$. Thus, the rotational frequency of the generator, and thus the output voltage frequency, decreases. The turbine governor senses this decrease in frequency and increases the power set point of the generator to return the frequency to a steady state 60 Hz.

For power electronically interfaced generation, the output frequency can be controlled to mimic the frequency-droop characteristic of a conventional inertial

generator such as a gas turbine with a synchronous generator. This is explained in detail in [22], [23], [29]. For the voltage regulation, a voltage vs. reactive power droop controller is utilized. As the output current of the power electronically interfaced DG source becomes more capacitive, the DG set point voltage is decreased. The converse is also true, if the output current becomes more inductive, the DG set point voltage is increased [22].

Frequency regulation is achieved through a power vs. frequency droop controller. As the frequency decreases, the power set point of the DG source increases. The converse is also true, as the frequency increases, the power set point of the DG source decreases. However, to restore the frequency to its nominal value, a restoration function must be included in each frequency droop controller [22].

Thus, to successfully operating in islanded mode, all DG source types need to be run below their maximum power output, thus leaving a preset margin amount to successfully implement the frequency droop control. If the load continues to increase beyond the margin level and the DG source is operating at the max power output, the frequency will drop and the load shedding relays will reduce the load to a level that the DG source can supply.

12 FURTHER RESEARCH

Further research is needed on creating a more detailed model of the system frequency response in islanded operation to allow for better balancing of the generation and loads. Additionally, the IEEE 34 node test feeder could be utilized to further test assumptions and conclusions from the Thevenin's equivalent circuit approach. This is because the IEEE 34 node feeder is characterized by long and lightly loaded lines, while the IEEE 13 node feeder has short lines that are more heavily loaded. Also, a system with an equal amount of imbalanced between the three phases could be examined to determine if the equivalent load reduction method is still effective to determine the voltages of the lighter-loaded phases. For increased accuracy, transmission line impedances, transformers, and additional loads connected to the transmission line before the line-end breakers may be included, however, for the sake of this study, they were omitted.

13 SUMMARY

This thesis examines future design and analysis of protective relays in distribution systems with integrated distributed generators. Specifically, when examining the impacts of interconnecting new distributed generation (DG) sources into an existing or new distribution grid, studies must be performed to ensure that lightning arresters on the high side of a delta-wye distribution substation transformer will not fail from a temporary overvoltage. This overvoltage condition can happen when a permanent single line to ground fault occurs on the high side of the distribution transformer, increasing the voltage of the unfaulted phases to a maximum of 1.73 pu volts. In this thesis, the Thevenin Equivalent Impedance method was used to calculate the magnitude of the overvoltage, which determined the proper protective relaying strategy to be implemented.

First, an equivalent network impedance was determined for the feeder containing the DG source. Next, a worst case estimate for the lightest system loading conditions was calculated, and a single equivalent load impedance was modeled. Then, Ohm's Law was used to determine the voltage at the substation node of this equivalent circuit consisting of the DG source, the system impedance, and the load impedance.

To successfully island the distribution system by tripping the substation breaker, under/over voltage and under/over frequency relays are utilized. If the calculated voltage does not result in lightning arrester failure within one second, an overvoltage or over/under frequency relay trips the substation breaker after a time delay to allow the

transmission line breakers to reclose first. If the lightning arresters fail before one second, undervoltage relays are used to trip the substation breaker at the inception of the transmission-level fault to protect the lightning arresters.

After the distribution grid successfully islands, the load shedding relays balance the DG generation capacity and the load. Then, the DG source is switched to droop control mode in order to match small changes in the load power. After the transmission level fault has been completely cleared, the distribution system is resynchronized and reconnected to the transmission grid following the procedure described in [2].

The benefit of the proposed Thevenin Equivalent Impedance method is that it provides a practical and straightforward method to determine whether a given DG capacity level will overload the lightning arresters. This method is a significant improvement over the current approach which always that the lightning arresters will overload and unnecessarily trips the DG source for every fault. Additionally, by islanding the distribution grid instead of always tripping the DG source, the DG source may supply a portion to all of the distribution system load, thus increasing the reliability of the distribution grid, and reducing lost revenue for the DG owners.

This thesis provides the initial phase of a full systematic framework of co-designing transmission and distribution protection systems. Future research areas include conducting stability studies to analyze the effects of large mismatches between the DG capacity and load levels when the system islands, in addition to studies to improve DG and grid synchronization and reconnection.

REFERENCES

[1] Electric Reliability Council of Texas, “ERCOT Analysis of the Impacts of the Clean Power Plan,” Oct 2015.

[2] K. Behrendt, “Protection for Unexpected Delta Sources,” 29th Annual Western Protective Relay Conference, Atlanta, Oct 2002.

[3] A. Mansoor and F. Martzloff, "The dilemma of surge protection vs. overvoltage scenarios: implications for low-voltage surge-protective devices," in Harmonics and Quality of Power Proceedings, 8th International Conference, Athens, pp. 964-969 vol.2. Oct 1998.

[4] R. Walling, R. Hartana and W. Ros, "Self-generated overvoltages due to open-phasing of ungrounded-wye delta transformer banks," in IEEE Transactions on Power Delivery, vol. 10, no. 1, pp. 526-533, Jan 1995.

[5] E. Sakshaug, J. Burke and J. Kresge, "Metal oxide arresters on distribution systems: fundamental considerations," in IEEE Transactions on Power Delivery, vol. 4, no. 4, pp. 2076-2089, Oct 1989.

[6] D. Gonzales, J. Bonner and K. Argiropoulos, "Benefits of gapped MOV arrester to improve system reliability and extend equipment life," in Electricity Distribution, 12th International Conference, Birmingham, pp. 2.14/1-2.14/5 vol.2. May 1993.

[7] J. Kirtley Jr, (2011) *Introduction to Load Flow*. MIT Open Courseware. [Online]. Accessed Apr 2016. Available: http://ocw.mit.edu/courses/electrical-engineering-

and-computer-science/6-061-introduction-to-electric-power-systems-spring-2011/readings/MIT6_061S11_ch5.pdf

[8] T. Chen, M. Chen, K. Hwang, P. Kotas and E. Chebli, "Distribution system power flow analysis-a rigid approach," in IEEE Transactions on Power Delivery, vol. 6, no. 3, pp. 1146-1152, Jul 1991.

[9] A. Abur, H. Singh, H. Liu and W. Klingensmith, "Three Phase Power Flow for Distribution Systems with Dispersed Generation", in Power Systems Computation Conference, Sevilla, Session 11, Paper 3, Page 1, Jun 2002.

[10] H. Zmuda, (2013). *Symmetrical Components and Sequence Networks*. University of Florida. [Online]. Accessed May 2016 Available: http://www.zmuda.ece.ufl.edu/Fall_2013_Power_Systems/6-Symmetrical_Components.pdf

[11] K. Steinfeld, *Design of Metal-Oxide Surge Arresters with Polymeric Housings*, Siemens AG, Berlin, Germany. [Online]. Accessed Apr 2016. Available: http://www.energy.siemens.com/ru/pool/hq/power-transmission/high-voltage-products/surge-arresters-and-limiters/publications/design-mo--1400142.pdf

[12] L. Pryor, (2008). *The Application and Selection of Lightning Arresters*, GE Industrial, [Online]. Accessed May 2016. Available: http://apps.geindustrial.com/publibrary/checkout/Arresters?TNR=White%20Papers|Arresters|generic

[13] W. Goch, (2012). *Surge Arrester Lead Length Revisited*. [Online]. Accessed Apr 2016 Available: http://classicconnectors.com/surge-arrester-lead-length-revisited/

[14] V. Hinrichsen, (2012) *Metal-Oxide Surge Arresters in High-Voltage Power Systems*. Siemens AG. [Online]. Accessed May 2016. Available: http://www.energy.siemens.com/hq/pool/hq/power-transmission/high-voltage-products/surge-arresters-and-limiters/Arrester_Book_Ed%20_3_en_2012.pdf

[15] J Ciufo, J Sykes, M. McDonald, W. Miller, J. Roberts, et. al. (2008). *Protection System Reliability: Redundancy of Protection System Elements*. North American Electric Reliability Corporation. [Online] Accessed Apr 2016 Available: http://www.nerc.com/docs/pc/spctf/Redundancy_Tech_Ref_1-14-09.pdf

[16] J. Nilsso and S. Riedel, *Electric Circuits,* 10th ed. Upper Saddle River, New Jersey, Pearson Education Inc., 2015, pp. 113-119.

[17] M. Baughman, C. Liu, E. Liu, S. Carneiro, D. Niebur, et. al. (2006). *IEEE 4 Node Test Feeder*, IEEE Power Engineering Society, Distribution System Analysis Subcommittee. [Online]. Accessed May 2016. Available: http://ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html

[18] M. Baughman, C. Liu, E. Liu, S. Carneiro, D. Niebur, et. al. (2004). *IEEE 13 Node Test Feeder*, IEEE Power Engineering Society, Distribution System Analysis Subcommittee. [Online]. Accessed May 2016. Available: http://ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html

[19] S. Rostamirad, K. Wang and J. Marti, "Power management in disasters: Application of loadshedding and wind turbine controller," in Electrical and Computer Engineering (CCECE), 24th Canadian Conference, Niagara Falls, pp. 001511-001514, May 2011

[20] J. Peqqueña Suni, E. Ruppert and F. Fajoni, "A guide for synchronous generator parameters determination using dynamic simulations based on IEEE standards," in Electrical Machines (ICEM), XIX International Conference, Rome, pp. 1-6, Sept 2010

[21] IEEE Application Guide for IEEE Std 1547(TM), IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," in IEEE Std 1547.2-2008 , vol., no., pp.1-217, Apr 2009.

[22] R. Lasseter, "MicroGrids," Power Engineering Society Winter Meeting. IEEE, pp. 305-308 vol.1, Jan 2002.

[23] F. Katiraei and M. Iravani, "Power Management Strategies for a Microgrid With Multiple Distributed Generation Units," in IEEE Transactions on Power Systems, vol. 21, no. 4, pp. 1821-1831, Nov. 2006.

[24] I. Balaguer, Q. Lei, S. Yang, U. Supatti and F. Peng, "Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation," in IEEE Transactions on Industrial Electronics, vol. 58, no. 1, pp. 147-157, Jan. 2011.

[25] J. Tang, J. Liu, F. Ponci and A. Monti, "Adaptive load shedding based on combined frequency and voltage stability assessment using synchrophasor measurements," in IEEE Transactions on Power Systems, vol. 28, no. 2, pp. 2035-2047, May 2013.

[26] H. Seyedi and M. Sanaye-Pasand, "New centralised adaptive load-shedding algorithms to mitigate power system blackouts," in IET Generation, Transmission & Distribution, vol. 3, no. 1, pp. 99-114, Jan 2009.

[27] A. Apostolov and M. Sforna, "Load-shedding in distribution systems during wide area disturbances," in Electricity Distribution, CIRED, 18th International Conference and Exhibition, Turin, pp. 1-4, Jun 2005.

[28] R. de Groot, P. Karaliolios, J. Slootweg and W. Kling, "The effect of advanced load shedding in the formation of islanded MV grids," Innovative Smart Grid Technologies (ISGT Europe), in 2nd IEEE PES International Conference and Exhibition, Manchester, pp. 1-7, Dec 2011.

[29] S. Barsali, M. Ceraolo, P. Pelacchi and D. Poli, "Control techniques of Dispersed Generators to improve the continuity of electricity supply," in Power Engineering Society Winter Meeting. IEEE, pp. 789-794 vol.2, Jan 2002

APPENDIX A

OVERVIEW OF SYMMETRICAL COMPONENTS

Fundamental power system analysis operates on the principle of balanced operation, i.e. the three phase voltages and currents are equal in magnitude, and equally spaced 120° apart. However, for unbalanced operation, such as for a fault or imbalanced loading condition, the voltages and phases no longer have equal magnitude and phase angle spacing. In this case, the phasors can be transformed into 3 sets of balanced phasors, called sequence phasors. The positive-sequence is a balanced set of phasors with equal magnitude and displaced by 120° and having the same phase rotation sequence as the original unbalanced system. The negative sequence is a set of balanced phasors, but rotating in the opposite phase sequence from the original system. The zero-sequence is three phasors of equal magnitude that all have a 0O displacement from each other. A graphical representation of the three sequences is seen below in Figure A.1.

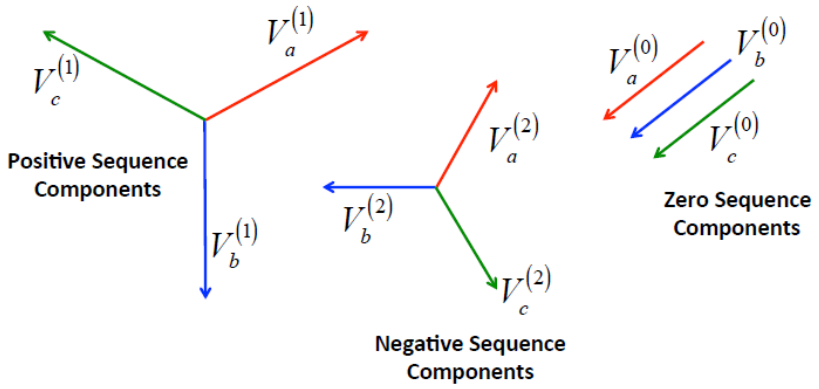


Figure A.1: Sequence Phasor Diagram (Reprinted with Permission from [10])

By definition, the original unbalanced phasors are the sum of the three sequence components, as shown below in Figure A.2.

$$V_a = V_a^{(0)} + V_a^{(1)} + V_a^{(2)}$$
$$V_b = V_b^{(0)} + V_b^{(1)} + V_b^{(2)}$$
$$V_c = V_c^{(0)} + V_c^{(1)} + V_c^{(2)}$$

Figure A.2: Sequnce to Phase Conversion (Reprinted with Permission from [10])

Using the relationship above, one can derive the following transformation:

$V_{abc} = AV_{012}$ where $A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$ $V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$ $V_{012} = \begin{bmatrix} V_a^0 \\ V_a^1 \\ V_a^2 \end{bmatrix}$ $a = 1\angle 120°$

The derivation is shown below in Figure A.3. Also, using the relationships shown above, one can derive the sequence impedances as $Z_{012} = A^{-1}Z_{abc}A$

This is because $V_{abc} = Z_{abc}I_{abc}$ and $AV_{012} = Z_{abc}AI_{012}$ So therefore, $V_{012} = A^{-1}Z_{abc}AI_{012}$ And the term Z_{012} can be defined as shown above [10].

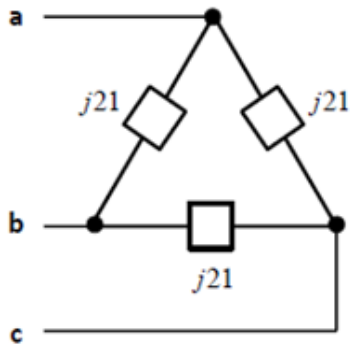
$$V_a = V_a^{(0)} + V_a^{(1)} + V_a^{(2)}$$
$$V_b = V_b^{(0)} + V_b^{(1)} + V_b^{(2)} = V_a^{(0)} + V_a^{(1)} e^{j240°} + V_a^{(2)} e^{j120°}$$
$$V_c = V_c^{(0)} + V_c^{(1)} + V_c^{(2)} = V_a^{(0)} + V_a^{(1)} e^{j120°} + V_a^{(2)} e^{j240°}$$

Let: $a = e^{j120°}$

$$V_a = V_a^{(0)} + V_a^{(1)} + V_a^{(2)}$$
$$V_b = V_a^{(0)} + a^2 V_a^{(1)} + a V_a^{(2)}$$
$$V_c = V_a^{(0)} + a V_a^{(1)} + a^2 V_a^{(2)}$$

Figure A.3: Derivation of Sequence Conversion (Reprinted with Permission from [10])

For a balanced load or transmission line with no mutual coupling, the sequence impedances are the same as the phase impedances as shown below in Figure A.4.



$$\mathrm{A}\begin{bmatrix} V_{ab}^{(0)} \\ V_{ab}^{(1)} \\ V_{ab}^{(2)} \end{bmatrix} = \begin{bmatrix} j21 & 0 & 0 \\ 0 & j21 & 0 \\ 0 & 0 & j21 \end{bmatrix} \mathrm{A}\begin{bmatrix} I_{ab}^{(0)} \\ I_{ab}^{(1)} \\ I_{ab}^{(2)} \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} V_{ab}^{(0)} \\ V_{ab}^{(1)} \\ V_{ab}^{(2)} \end{bmatrix} = j21\mathrm{A}^{-1}\mathrm{A}\begin{bmatrix} I_{ab}^{(0)} \\ I_{ab}^{(1)} \\ I_{ab}^{(2)} \end{bmatrix} = \begin{bmatrix} j21 & 0 & 0 \\ 0 & j21 & 0 \\ 0 & 0 & j21 \end{bmatrix} \begin{bmatrix} I_{ab}^{(0)} \\ I_{ab}^{(1)} \\ I_{ab}^{(2)} \end{bmatrix}$$

Figure A.4: Sequnce Impedance Calcuations (Reprinted with Permission from [10])

However, for a delta connected load or transformer, there is no path for the zero sequence current to flow, so in the sequence network domain, the zero sequence impedance network is drawn with an open circuit, as shown below in Figure A.5. This is further explained below in Figure A.6 and further explanation is given below.

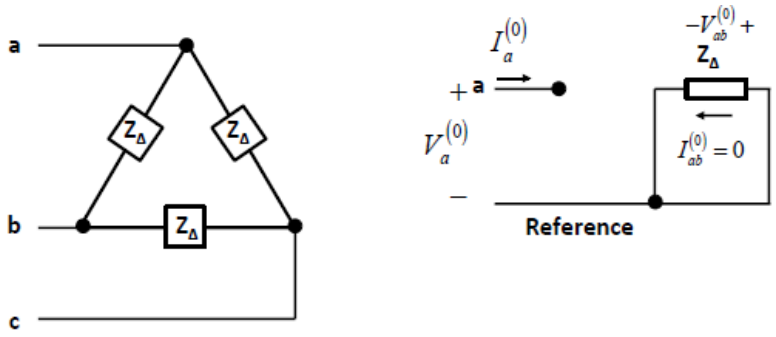


Figure A.5: Zero Sequence Network Connection for Delta Circuit (Reprinted with Permission from [10])

For a balanced three phase system, there is no zero-sequence current flowing into a delta circuit. However, if there is a nonzero value of circulating current flowing in the delta connected load, the current cannot be determined from the line currents alone, as shown in the equations below. This is because there is not return path for the zero-sequence current, as explained later in this appendix.

$$I_a = I_{ab} - I_{ca}$$
$$\Rightarrow I_a^{(1)} + I_a^{(2)} = \left(I_{ab}^{(0)} + I_{ab}^{(1)} + I_{ab}^{(2)}\right) - \left(I_{ca}^{(0)} + I_{ca}^{(1)} + I_{ca}^{(2)}\right)$$
$$= \underbrace{\left(I_{ab}^{(0)} - I_{ca}^{(0)}\right)}_{=0} + \left(I_{ab}^{(1)} - I_{ca}^{(1)}\right) + \left(I_{ab}^{(2)} - I_{ca}^{(2)}\right)$$
$$I_a^{(1)} + I_a^{(2)} = \underbrace{\left(I_{ab}^{(0)} - I_{ca}^{(0)}\right)}_{=0} + \left(I_{ab}^{(1)} - I_{ca}^{(1)}\right) + \left(I_{ab}^{(2)} - I_{ca}^{(2)}\right)$$

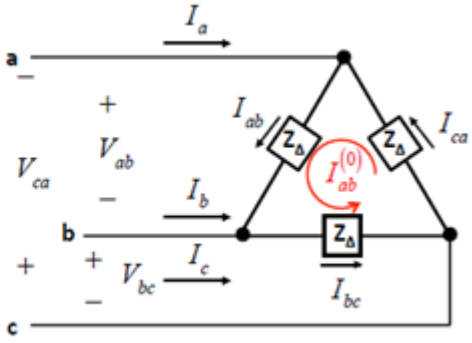
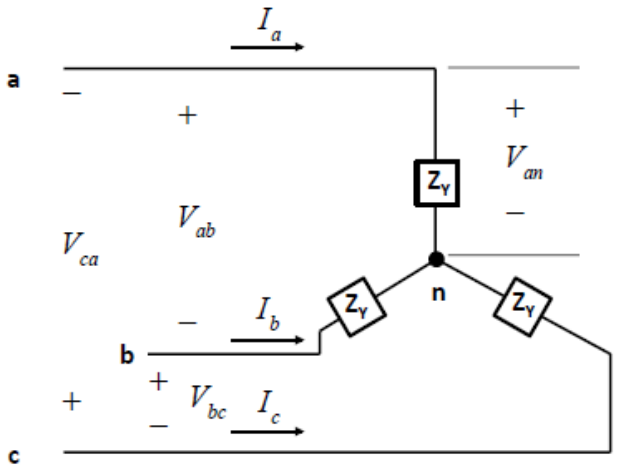


Figure A.6: Derivation of Zero Sequence Delta Connections (Reprinted with Permission from [10])

For a Y-ungrounded load connected below in Figure A.7, at the neutral point n, the positive and negative sequence currents and voltages separately sum to zero, respectively. However, since there is no path for the zero sequence return current, the zero sequence network is shown as an open circuit, as in Figure A.5.



$$V_{ab} = V_{an} - V_{bn}$$
$$V_{bc} = V_{bn} - V_{cn}$$
$$V_{ca} = V_{cn} - V_{an}$$

Figure A.7: Ungrounded Y-Connected Load (Reprinted with Permission from [10])

However, if a neutral return path is added to the circuit, there is now a return path for the zero-sequence currents. Using Kirchhoff's Current law at point n, one gets that $I_n = I_a + I_b + I_c$ However, since the positive sequence current and negative sequence current both separately sum to zero at point n, since both are sets of balanced phasors, there is no positive or negative sequence current flowing in the neutral return path. From the equations below in Figure A.8, it is shown that the neutral current is the sum of the three zero sequence currents. However, since the zero sequence currents are the same magnitude and have 0O angle separation, the neutral current is $3I_a^0$.

$$
\begin{aligned}
I_n &= \left(I_a^{(0)} + I_a^{(1)} + I_a^{(2)}\right) + \left(I_b^{(0)} + I_b^{(1)} + I_b^{(2)}\right) + \left(I_c^{(0)} + I_c^{(1)} + I_c^{(2)}\right) \\
&= \left(I_a^{(0)} + I_b^{(0)} + I_c^{(0)}\right) + \underbrace{\left(I_a^{(1)} + I_b^{(1)} + I_c^{(1)}\right)}_{=0} + \underbrace{\left(I_a^{(2)} + I_b^{(2)} + I_c^{(2)}\right)}_{=0} \\
&= 3I_a^{(0)}
\end{aligned}
$$

Figure A.8: Neutral Current derivation (Reprinted with Permission from [10])

The presence of the neutral resistance Z_n causes a $\frac{3I_n^0}{Z_n}$ voltage drop between the neutral point n and ground. Using sequence network analysis, the following voltages can be established. A full derivation of this result is found in [10].

$$V_a^{(0)} = \left(Z_Y + 3Z_n\right) I_a^{(0)} = Z_0 I_a^{(0)}$$
$$V_a^{(1)} = Z_Y I_a^{(1)} = Z_1 I_a^{(1)}$$
$$V_a^{(2)} = Z_Y I_a^{(2)} = Z_2 I_a^{(2)}$$

Figure A.9: Voltage Computations (Reprinted with Permission from [10])

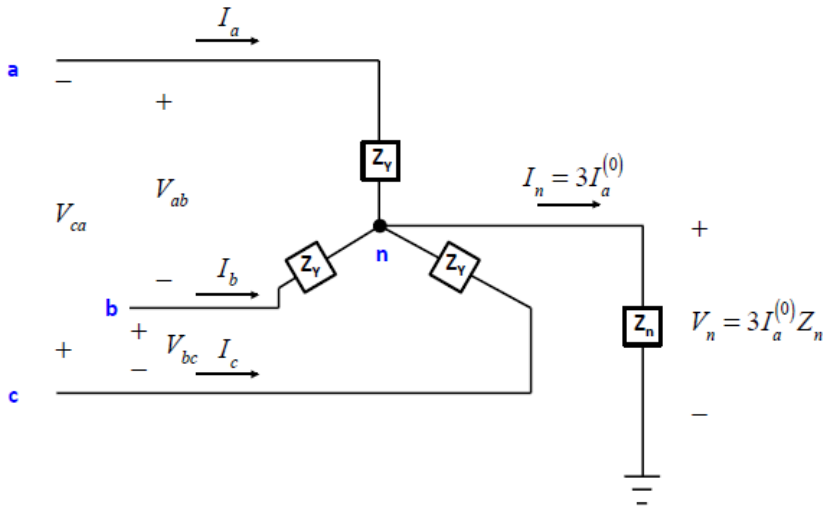


Figure A.10: Unbalanced Voltage Operation (Reprinted with Permission from [10])

Using the results from Figure A.9, the following sequence network connections can be established in Figure A.11. Thus, for the unbalanced voltage operation shown in Figure A.10, the three sequence networks are independent, and thus can be decoupled into three separate networks, as shown below in Figure A.11.

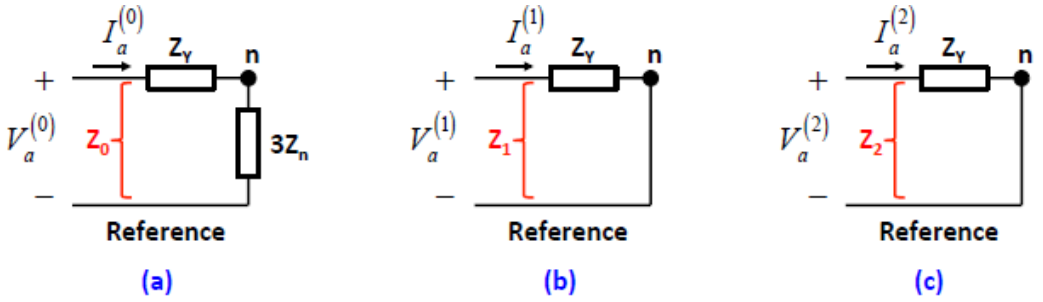


Figure A.11: Sequence Impedances (Reprinted with Permission from [10])

Using Figure A.11(a) above, one can see that an ungrounded Y configuration, as shown below in Figure A.12, is the same as making Z_n infinite. In this case, the zero sequence network shows and open circuit, as shown below for Figure A.12, confirming the assertion made earlier in this section. The delta connected load has no return path, so it is also shown with an open circuit in the zero sequence network.

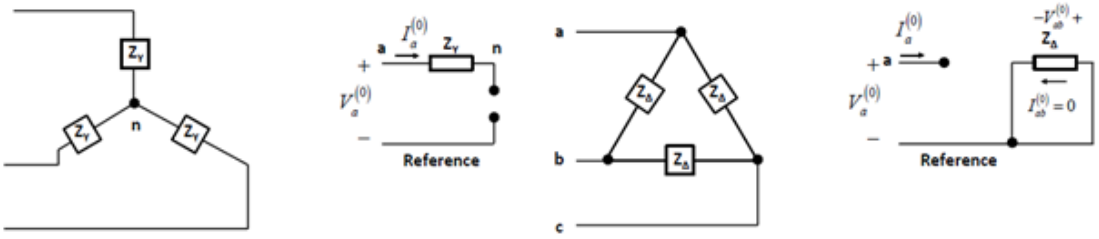


Figure A.12: Zero Sequence Connections for Delta and Ungrounded Wye Circuits (Reprinted with Permission from [10])

APPENDIX B

ADDITIONAL IEEE 4 NODE RESULTS

After establishing the base case in section 10.1.1, an additional load was added at the end of the second distribution line, as shown in Figure B.1. Also, the unbalanced loads were implemented from the IEEE 4 node feeder case, but to further increase the voltage drop on the system, the specified load value was replicated at each load location.

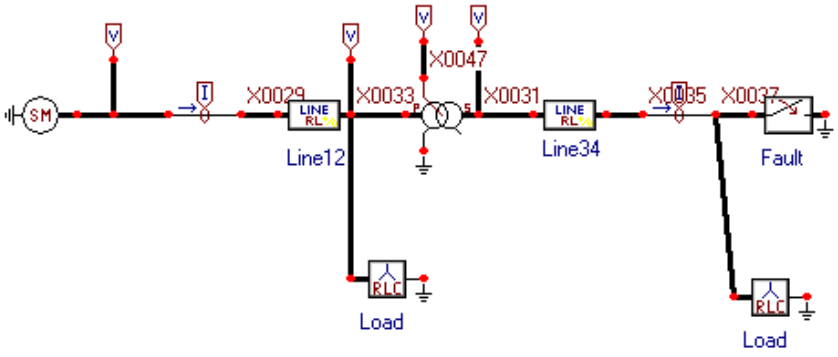


Figure B.1: IEEE 4 Node Network, Modified

Figure B.2 below shows the result when the specified unbalanced load was connected to both the high and low sides of the transformer. B phase voltages are reported since they are the largest value of the high-side voltage post-fault. The pre-fault B-phase voltage is 22.7 kV and the post fault voltage is 39.5kV, which is an 8.1% voltage drop from the base case voltage of 43 kV.

Running the same scenario with the synchronous generator instead of the ideal voltage source gave a pre-fault B-phase voltage of 23.4 kV and post fault voltage of 37.6kV, which is voltage drop of 12.6%

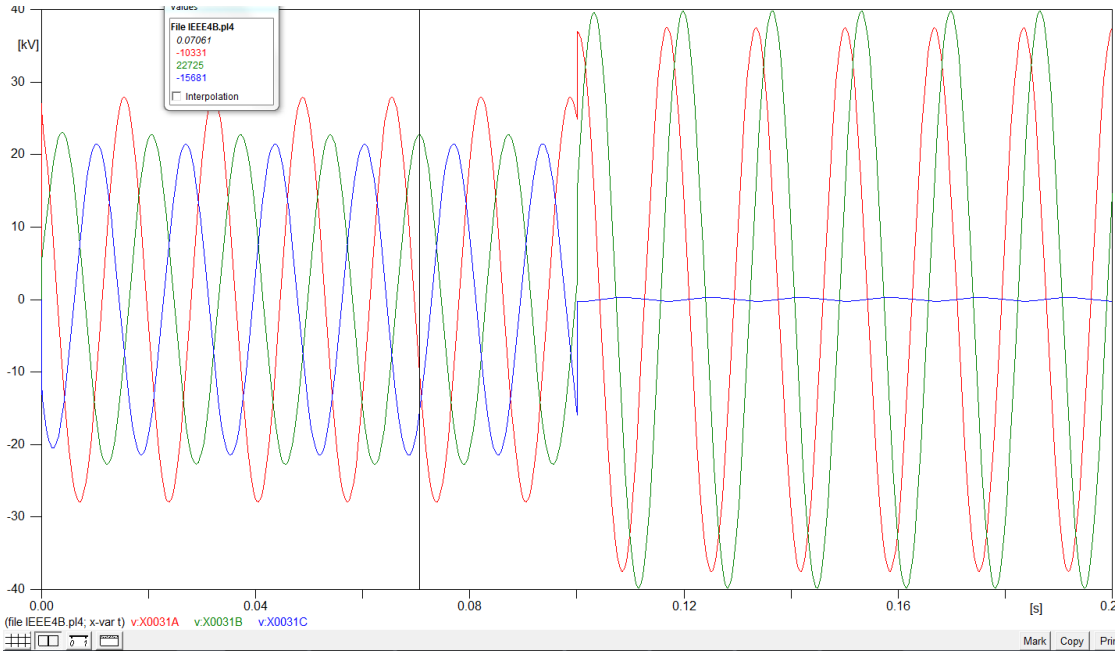


Figure B.2: Voltage Results From Modified IEEE 4 Node System

Next, the load values were tripled, and the simulation was run again, with the results shown below in Figure B.3. The pre-fault voltage was 21 kV, and the post fault voltage was 33.5 kV, which is a 22% voltage drop. For the synchronous machine case, the post-fault voltage was 28.3 kV, which is a 34.2% voltage drop.

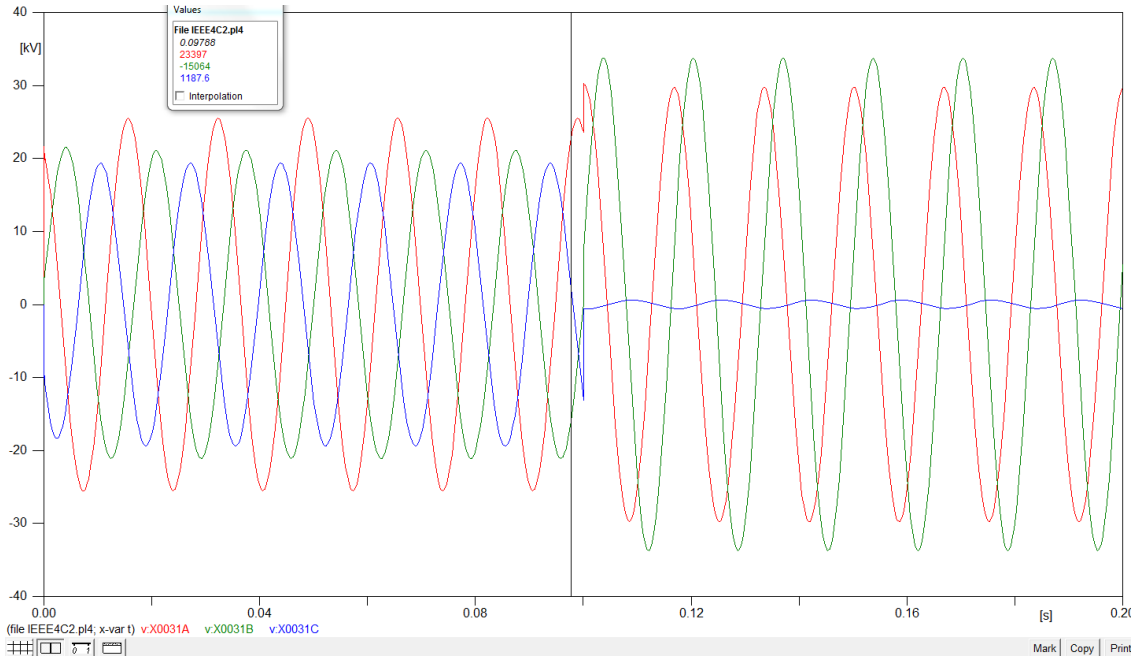


Figure B.3: Voltage Results with Load Trippled

The voltage drop from the second case meets the upper bound requirement from Section 7.1 (16% to 30%) for the DG source to remain connected during the line to ground fault without the lightning arresters overloading for 1 second. This gives the protective relaying the necessary time to island the distribution system without overloading the lightning arresters. For the case of less than 6 times the base load, the distribution network would need to be tripped more quickly to prevent the lightning arresters from being overloaded.

APPENDIX C

ADDITIONAL IEEE 13 NODE RESULTS

DG node:	Phase A	Phase B	Phase C
633 With Load	0.0978+0.1118i	0.0895+0.1098i	0.0961+0.1135i
633 Without Load	0.0982+0.1151i	0.0895+0.1117i	0.0964+0.1168i
675 without load	0.2387+0.4484i	0.2307+0.4351i	0.2265+0.4289i
675 with load	0.2353+0.4431i	0.2251+0.4219i	0.223+0.4229i
680 with load	0.2374+0.5934i	0.2246+0.5691i	0.2189+0.5654i
680 without load	0.2288+0.6214i	0.2147+0.6025i	0.2103+0.5917i

Table C.1: Measured System Impedances with the DG Source Connected to the Given Node, with and without the Connected System Load

System Configuration	Phase A	Phase B	Phase C
Series system w/load	0.473+0.9388i	0.4444+0.9114i	0.4412+0.901i
Series system w/o load	0.4414+1.0767i	0.4169+1.0428i	0.4107+1.0272i
Series Parallel 1 w/load	0.5052+0.7577i	0.4743+0.7886i	0.4755+0.7419i
Series Parallel 2 w/load	0.4994+0.619i	0.4809+0.6869i	0.4761+0.6161i

Table C.2: Impedances of the Series and Parallel Configurations of the IEEE 13 Node System

DG Node or Configuration	A-Phase	B-Phase	C-Phase
Node 633	0.0547+0.1676i	0.0442+0.1754i	0.0733+0.1779i
Node 675	0.0203+0.5257i	-0.0526+0.4904i	-0.0325+0.5557i
Node 680	0.0491+0.6294i	0.1376+0.5894i	0.1026+0.6682i
Parallel 2	0.0334+0.5018i	-0.0278+0.4723i	-0.0092+0.5236i
Series System	-0.0279+1.0931i	-0.1578+1.0148i	-0.1225+1.138i

Table C.3: Voc/Isc Measured Impedances of Various System Configurations

Results with calculated impedances:

Calculated Substation Voltage	Base Load Configuration (without caps)	Base Load Configuration (with caps)	Measured Voltage (no test load)	Base + Test Load	Test Load only	Measured Voltage
A-Phase	0.990	0.992	0.981	0.979	0.989	0.972
B-Phase	0.991	0.993	0.989	0.980	0.990	0.980
C-Phase	0.987	0.989	0.974	0.978	0.988	0.964
Error						
A-Phase	0.95%	1.13%		0.64%	1.75%	
B-Phase	0.25%	0.41%		0.05%	1.03%	
C-Phase	1.33%	1.56%		1.40%	2.41%	

Table C.4: Substation Voltages with DG Connected to Node 633, Voc/Isc Calculated Impedance

Calculated Substation Voltage	Base Load Configuration (without caps)	Base Load Configuration (with caps)	Measured Voltage (no test load)	Base + Test Load	Test Load only	Measured Voltage
A-Phase	0.980	0.986	*0.978*	0.964	0.979	*0.956*
B-Phase	0.985	0.990	*0.969*	0.975	0.987	*0.952*
C-Phase	0.978	0.985	*0.973*	0.966	0.983	*0.951*
Error						
A-Phase	0.18%	0.75%		0.91%	2.51%	
B-Phase	1.62%	2.08%		2.46%	3.66%	
C-Phase	0.52%	1.26%		1.61%	3.32%	

Table C.5: Substation Voltages with DG Connected to Node 675, Voc/Isc Calculated Impedance

Calculated Substation Voltage	Base Load Configuration (without caps)	Base Load Configuration (with caps)	Measured Voltage (no test load)	Base + Test Load	Test Load only	Measured Voltage
A-Phase	0.974	0.981	0.967	0.953	0.973	0.942
B-Phase	0.971	0.976	0.975	0.944	0.968	0.956
C-Phase	0.964	0.972	0.961	0.940	0.968	0.938
Error						
A-Phase	0.76%	1.44%		1.23%	3.33%	
B-Phase	0.38%	0.15%		1.20%	1.27%	
C-Phase	0.32%	1.19%		0.22%	3.20%	

Table C.6: Substation Voltages with DG Connected to Node 680, Voc/Isc Calculated Impedance

Calculated Substation Voltage	Base Load Configuration (without caps)	Base Load Configuration (with caps)	Lump load -1 (w/o caps)	Lump load -1 (w/caps)	Measured Voltage (no test load)
A-Phase	0.923	0.944	0.962	0.974	0.895
B-Phase	0.941	0.958	0.971	0.981	0.929
C-Phase	0.913	0.939	0.958	0.972	0.880
Error					
A-Phase	3.17%	5.49%	7.55%	8.81%	
B-Phase	1.31%	3.17%	4.61%	5.59%	
C-Phase	3.78%	6.77%	8.86%	10.48%	

Table C.7: Substation Voltages of Series System Configuration, no Test Load, Voc/Isc Calculated Impedance

Calculated Substation Voltage	Base (w/caps) + Test Load	Base (w/o caps) + Test Load	Test Load only	Measured Voltage (test load)
A-Phase	0.900	0.881	0.962	0.854
B-Phase	0.925	0.896	0.975	0.894
C-Phase	0.898	0.874	0.967	0.843
Error				
A-Phase	5.34%	3.16%	12.62%	
B-Phase	3.53%	0.21%	9.05%	
C-Phase	6.48%	3.65%	14.73%	

Table C.8: Substation Voltages of Series System Configuration, Test Load, Voc/Isc Calculated Impedance

Calculated Substation Voltage	Base Load Config (with caps)	Equiv System	Measured Voltage (no test load)	Base + Equiv. Sys + Test load	Equiv. Sys + Test Load	Measured Voltage (test load)
A-Phase	0.944	0.960	0.920	0.922	0.938	0.899
B-Phase	0.971	0.983	0.950	0.954	0.967	0.932
C-Phase	0.950	0.967	0.911	0.929	0.947	0.892
Error						
A-Phase	2.61%	4.33%		2.52%	4.32%	
B-Phase	2.20%	3.50%		2.37%	3.76%	
C-Phase	4.31%	6.23%		4.19%	6.21%	

Table C.9: Substation Voltages of Parallel 1 System Configuration, Voc/Isc Calculated Impedance

Equivalent Load for each configuration	Base Load Configuration (with caps)	Equivalent System (lump load -1)	Base + Equiv. Sys + Test load	Equiv. Sys + Test Load
A-Phase	4214+1540i	3039+1124i	5714+2140i	4539+1724i
B-Phase	3021+1164i	1982+699i	4521+1764i	3482+1299i
C-Phase	4188+1557i	2936+1036i	5688+2157i	4436+1636i

Table C.10: Equivalent Loads for Parallel 1 Configurations

Equivalent Load per configuration	Base Load (without caps)	Base Load (with caps)	Lump load - 1 (w/o caps)	Lump load - 1 (w/caps)
A-Phase	2350+1212i	2350+832i	1175+606i	1175+416i
B-Phase	2078+1254i	2078+930i	1039+627i	1039+465i
C-Phase	2504+1506i	2504+1042i	1252+753i	1252+521i

Table C.11: Equivalent Loads for Series Configurations, Part 1

Equivalent Load per configuration	Base (w/caps) + Test Load	Base (w/o caps) + Test Load	Test Load only
A-Phase	3850+1432i	3850+1812i	1500+600i
B-Phase	3578+1530i	3578+1854i	1500+600i
C-Phase	4004+1642i	4004+2106i	1500+600i

Table C.12: Equivalent Loads for Series Configurations, Part 2

Equivalent Load per Config	**Base Load Config (without caps)**	**Base Load Configuration (with caps)**	**Lump load -1**	**Lump load -2**	**Equivalent System -1**
A-Phase	5389+2336i	5389+1956i	4214+1540i	3039+1124i	2350+832i
B-Phase	4060+1953i	4060+1629i	3021+1164i	1982+699i	2078+930i
C-Phase	5440+2542i	5440+2078i	4188+1557i	2936+1036i	2504+1042i

Table C.13: Equivalent Loads for Series Parallel 1 Configurations

Equivalent Load per Config	Base Load (with caps)	Lump load -1	Lump load -2	Equiv System -1	Equivalent System -2	Lump load -1 Equivalent System -1
A-Phase	8428+3079i	7253+2853i	6078+2248i	5389+1956i	2350+832i	4214+1540i
B-Phase	6043+2327i	5004+2024i	3964+1398i	4060+1629i	2078+930i	3021+1164i
C-Phase	8376+3114i	7124+2825i	5872+2072i	5440+2078i	2504+1042i	4188+1557i

Table C.14: Equivalent Loads for Series Parallel 2 Configurations

APPENDIX D

UNDER FREQUENCY LOAD SHEDDING RESULTS

To test the system described in section 9.4, a 2 MVA, 600V synchronous machine was connected to a simulated distribution grid with a total of 2 MVA of load. 500 kVA of simulated "auxiliary load" was connected to the low side of a 2 MVA, 600 V/ 4160 V transformer, and 3, 500 kVA loads were connected to the 4160V high side of the transformer via 3-phase breakers. These three breakers had underfrequency thresholds of 58, 57 and 56 Hz, respectively before the breakers tripped. This system was connected to a simulated "grid source" via another 3-phase breaker. This allowed the synchronous machine to reach a steady state operating condition before the breaker was tripped, simulating an islanding event. The resulting system frequency, generator behavior, and load breaker statuses are shown below in the following 3 figures, respectively. Figure D.3 shows the 3 breaker statuses, with 1 being closed and 0 being open. Notice that at 1.5 seconds (corresponding to the grid interconnection breaker opening), the system frequency begins to drop, because the system load combined with the losses in the transformer were greater than the generation capability of the synchronous generator. The frequency drops until it hits 58 Hz, when breaker 1 opens. The frequency quickly recovers and due to the generator speed control, it settles down to the steady state frequency of 60 Hz. To properly model the system response of a microgrid with power electronic interfaced generation, the speed control and the inertia

of the synchronous machine model can be tuned to properly match the corresponding p-f droop control and DC bus capacitance of the power electronic interfaced generation.

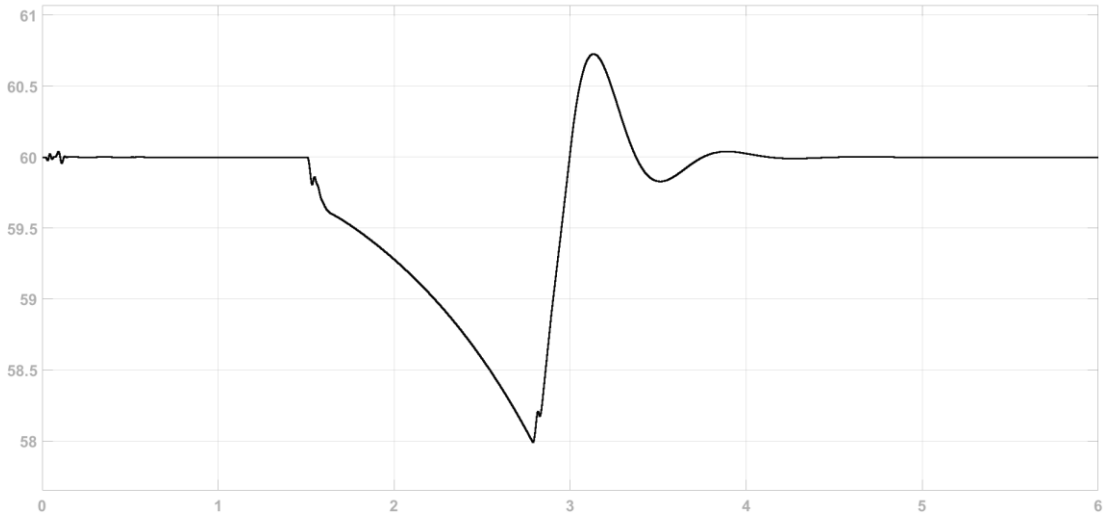


Figure D.1: Graph of System Frequency (Hz) vs. Time (s)

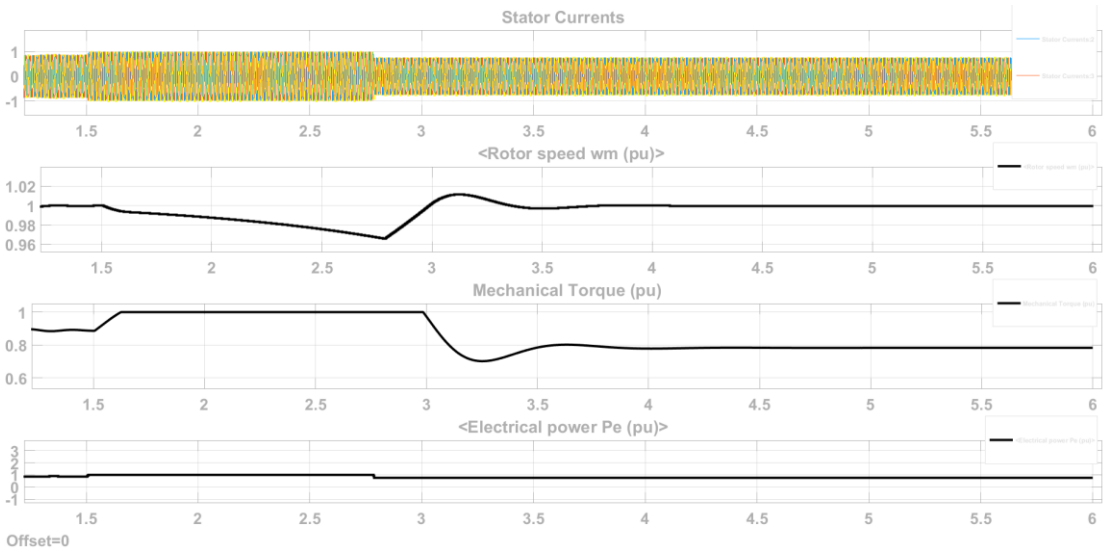


Figure D.2: Electrical Power and Rotor Angle vs. Time

Figure D.3: Breaker Status (open/closed) vs. Time (s)