LOW POWER, HIGH PSR CMOS VOLTAGE REFERENCES

A Thesis

by

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ABSTRACT

With integration of various functional modules such as radio frequency (RF) circuits, power management, and high frequency digital and analog circuits into one system on chip (SoC) in recent applications, power supply noise can cause significant system performance deterioration. This makes supply noise rejection of the embedded voltage reference crucial in modern SoC applications. Also the use of resistors in bandgap voltage references makes them less suitable for modern low power and portable applications.

This thesis introduces two resistorless sub-1 V, all MOSFET references. The goal is to achieve a high power supply rejection (PSR) over a wide bandwidth not achieved in previous works. This high PSR over wide bandwidth is achieved by using a combination of a feedback technique and an innovative compact MOSFET low pass filter. The two references were fabricated in a standard 0.18 μm CMOS process.

The first reference uses a composite transistor in subthreshold to produce a proportional-to-absolute temperature (PTAT) voltage which is converted to a current used to thermally compensate the threshold voltage of a MOSFET in saturation. The second references uses *dynamic-threshold voltage MOSFET* (DTMOS) to produce a PTAT voltage which is converted to a current used to thermally compensate the threshold voltage of a MOSFET in saturation.

The measurement shows that both references consumes a sub-1 μW power across their entire operating temperatures. The first reference achieves a PSR better than 50 dB for frequencies of up to 70 MHz and a 20 ppm/°C temperature coefficient (TC) for

temperatures from -35 °C — 80 °C. It has a compact area of 0.0180 mm^2 and operates on a supply of 1.2 V — 2.3 V.

The second reference achieves a PSR better than 50 dB for frequencies of up to 60 MHz. This reference achieves a TC of 9.33 ppm/°C after trimming for temperatures from -30 °C — 110 °C and a line regulation of 0.076 %/V for a step from 0.8 V to 2 V supply voltage with 360 nW power consumption at room temperature. It has a compact area of 0.0143 mm^2.

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TABLE OF CONTENTS

Page

ABSTRACT ii

ACKNOWLEDGEMENTS iv

TABLE OF CONTENTS v

LIST OF FIGURES viii

LIST OF TABLES xii

1. INTRODUCTION TO VOLTAGE AND CURRENT REFERENCES 1

1.1 Semiconductor Basics 1
1.1.1 Basic Semiconductor Effects 2
1.1.2 Threshold Voltage 6
1.1.3 Carrier Mobility 10
1.2 Current References 11
1.2.1 PTAT Current References 12
1.2.2 CTAT Current References 14
1.2.3 Temperature-Independent Current References 16
1.2.4 $PTAT^2$ Current References 18
1.3 Voltage References 21
1.3.1 Types of Voltage References 21
1.3.2 Curvature-Correction Techniques 25
1.4 Definitions and Metrics 31
1.4.1 Initial Accuracy 31
1.4.2 Temperature Coefficient (TC) 32
1.4.3 Thermal Hysteresis 33
1.4.4 Long-Term Stability 34
1.4.5 Power Supply Rejection (PSR) 34
1.4.6 Line regulation 35

2. CMOS BANDGAP VOLTAGE REFERENCES 36

2.1 Bipolar Transistors (BJT) in CMOS 36
2.2 VEB Temperature Characteristics 38
2.3 Commercial Voltage Reference ICs 40
2.4 The Classical CMOS Bandgap Reference 44
2.5 Design of Sub-1 V CMOS Bandgap Reference 46
2.5.1 Circuit Overview 46

2.5.2 Curvature Compensation 47
2.5.3 PSR Improvement 50
2.5.4 Op-Amp 52
2.5.5 Startup 54
2.5.6 Experimental Results 55

3. AN ALL-MOSFET VOLTAGE REFERENCE WITH -50 DB PSR @ 80 MHZ FOR LOW POWER SOC DESIGN 58

3.1 Motivation and Overview 58
3.2 Architecture and Design 59
3.2.1 PTAT Voltage Generator 62
3.2.2 Self-Biased Current Source 63
3.2.3 Loop Compensation 66
3.2.4 Reference Generator 66
3.2.5 PSR Improvement 69
3.2.6 Trimming Circuit 69
3.3 Design Considerations 70
3.3.1 Channel Length Modulation 70
3.3.2 Process Variation 71
3.3.3 Dynamic Range 72
3.4 Temperature Compensation 72
3.5 Design of the Proposed Voltage Reference 73
3.6 Simulation Results 75

4. AN ALL-MOSFET SUB-1 V VOLTAGE REFERENCE WITH A -51 dB PSR UP TO 60 MHz DESIGN 81

4.1 Motivation and Overview 81
4.2 Proposed Reference Voltage Architecture 83
4.2.1 Conceptual Block Diagram 83
4.2.2 PTAT Voltage Generator 84
4.2.3 Self-Biased Current Source 88
4.2.4 Startup Circuit 91
4.2.5 Reference Generator and Leakage Compensation 91
4.2.6 PSR Improvement 93
4.2.7 Compact MOSFET Low Pass Filter (LPF) 97
4.3 Design Considerations 100
4.3.1 Channel Length Modulation 100
4.3.2 Process Variation 100
4.3.3 Dynamic Range 101
4.4 Temperature Compensation 102
4.5 Simulation Results 103

5. EXPERIMENTAL RESULTS 108

5.1 Setup for Testing the VRs 108
5.2 Experimental Results An All-Mosfet Voltage Reference With -50 dB PSR @ 80 Mhz For Low Power Soc Design 112
5.3 Experimental for the All-MOSFET Sub-1 V Voltage Reference with a -51 dB PSR up to 60 MHz 116

6. CONCLUSIONS 122

REFERENCES 124

APPENDIX 131

LIST OF FIGURES

Page

Figure 1.1: Band-gap of Silicon Dependence on Temperature 3

Figure 1.2: a) Temperature Dependence of Electron Concentration n_0 in n-type Si for four values of net doping. Also shown is the Temperature Dependence of *ni*. b) Temperature Dependence of Normalised Electron Concerntration n_0/N_D 5

Figure 1.3: a) Temperature Dependence of Threshold Voltage of NMOS (L=2) 10

Figure 1.4: PTAT Current Generator 14

Figure 1.5: CTAT Current Generator using V_{BE} 15

Figure 1.6: Temperature-Independent Current Reference a) Concept and b) Implementation 17

Figure 1.7: CMOS $PTAT^2$ Current Reference 20

Figure 1.8: Categories of Voltage References 22

Figure 1.9: Zener Diode References a) Zener Diode as Shunt Regulator b) Thermally Compensated Breakdown Zener Diode 24

Figure 1.10: Conceptual Implementation of a First-Order Reference a) Voltage-Mode b) Current-Mode 27

Figure 1.11: Squared PTAT Curvature-Correction a) Typical Temperature Dependence b) Implementation Concept 29

Figure 1.12: Temperature Dependence of Piecewise-Linear Curvature Corrected Bandgap 30

Figure 1.13: Different Methods for TC Calculation 33

Figure 2.1: CMOS BJTs a) Lateral NPN b) Vertical PNP 38

Figure 2.2: Types of Commercial Monolithic Voltage References 41

Figure 2.3: A CMOS Bandgap Reference (*The Brokaw Cell*) 45

Figure 2.4 BGR Curvature Compensation a) Concept b) Implementation 49

Figure 2.5: The Proposed Bandgap Reference (BGR) 50

Figure 2.6: PSR Improvement Concept 53

Figure 2.7: Op-Amp for BGR 54

Figure 2.8: Measured Temperature Dependence of the Proposed BGR 56

Figure 2.9: Measured PSR of Output BGR 56

Figure 3.1: The Conceptual Bock Diagram of the Proposed VR Circuit 61

Figure 3.2: Composite Transistor PTAT Voltage Generator 63

*Fig*ure 3.3: V_{PTAT} across Process Corners 63

Figure 3.4: Self-Biased Current Source 64

Figure 3.5: Temperature Dependence of I_{BIAS} across Process Corners 65

Figure 3.6: Proposed VR Circuit 68

Figure 3.7: Trimming Circuit 70

Figure 3.8: Simulation of V_{REF} for Various Supply Voltages 76

Figure 3.9: Monte Carlo Simulation for Untrimmed Reference for -20 °C to 100 °C 76

Figure 3.10: Monte Carlo Simulation @27 °C a) Untrimmed b) Trimmed 77

Figure 3.11: Startup Simulation 78

Figure 3.12: a) Accuracy of Reference Voltage vs. Area at Different Power Levels and b) the area of MP6 and Corresponding Power for 3.15% Accuracy and 19 ppm. 79

Figure 3.13: Simulated PSR of Output VR 80

Figure 4.1: The Basic Concept of the Proposed VR 85

Figure 4.2: Cross Section of a DTMOS Transistor and Schematic Connection b) PTAT Generation from DTMOS c) Simulated Temperature Characteristics of DTMOS and Corresponding PTAT Voltage 87

Figure 4.3: Proposed VR circuit 90

Figure 4.4: Leakage Compensation Configuration a) Low Temperature and b) High Temperature 94

Figure 4.5: Power Supply noise Paths at (a) and Small Signal Diagram for PSR at (b) 97

Figure 4.6: The compact MOSFET LPF and Equivalent RC Model along with b) the MOSFET LPF and Equivalent RC Model Response 99

Figure 4.7: Simulation of V_{REF} for Various Supply Voltages 104

Figure 4.8: Monte Carlo Simulation for V_{REF} a) Untrimmed VREF @ 27 °C and b) Trimmed VREF @ 27 °C 105

Figure 4.9: Simulation Results for Start-Up of the VR 106

Figure 4.10: Reference Voltage v.s. Power Supply Voltage 106

Figure 4.11: Simulated PSR of Output VR 107

Figure 5.1: DC Power Supply for VR 108

Figure 5.2: The Laboratory Setup for Testing 110

Figure 5.3: PSR and Temperature Stability Measurement Setup 111

Figure 5.4: Chip Micrograph of the Proposed VR1 113

Figure 5.5: Measured Temperature Dependence of the Proposed VR1 114

Figure 5.6: Measured Temperature Dependence of Five Trimmed Samples 114

Figure 5.7: Supply dependence of V_{REF} 115

Figure 5.8: Measured PSR of VR1 115

Figure 5.9: Chip Micrograph of the Proposed VR2 117

Figure 5.10: Measured Temperature Dependence of the Output Voltage (V_{REF}) of the Proposed VR 118

Figure 5.11: a) Supply Dependence of V_{REF} b) Quiescent Current of the VR2 119

Figure 5.12: Measured PSR of Output Reference Voltage 120

Figure A.1: Calibration Concept 132

Figure A.2: Block Diagram of the Proposed Auto-calibration Bandgap Reference System 133

Figure A.3: Temperature Sensor 135

Figure A.4: ADC Output Code vs. Temperature 135

Figure A.5: Monte-Carlo Simulation a) VPTAT and b) Slope of VPTAT 136

Figure A.6: Piecewise Nonlinear 2nd Order Bandgap Reference 138

Figure A.7: Curvature of Proposed 2nd Order Bandgap 139

Figure A.8: Folded Cascode Op-amp with Chopping Scheme 141

Figure A.9: Modular and Non-overlap Clock 143

Figure A.10: Temperature Dependence of 2nd Order BGR Output Voltage 144

Figure A.11: Noise Spectrum of V_{REF} from 1 Hz to 500 kHz 144

Figure A.12: Monte Carlo Simulation a) Without Chopper and b) With Chopper 145

Figure A.13: Chip Floor Plan which has 12 Sensors and 4 Heaters 147

Figure A.14: Flowchart for Reference Voltage Sampling 148

Figure A.15: $F(V)_{12}$ Contour as well as the Optimal Solution (x,y) of the Calibration Engine 150

Figure A.16: $F(V)_{23}$ Contour as well as the Optimal Solution (x,y,z) of the Calibration Engine 150

LIST OF TABLES

Page

Table 2.1: Popular Proprietary Bandgap Based Voltage Reference Products 42

Table 2.2: Performance Comparison of Selected Bandgap References in Today's Market.....43

Table 2.3: Performance Comparison of Sub-1 V BGR with Previous Works.....57

Table 5.1: Performance Summary and Comparison with Previous Works.....121

Table 6.1: Main Difference Between the two Proposed VRs 123

1. INTRODUCTION TO VOLTAGE AND CURRENT REFERENCES

A crucial part in the design of analog integrated circuits is the creation of reliable and well-defined voltage and current references. A reference in a circuit establishes a stable point which is used by other sub-circuits to generate predictable and repeatable results. It is essential that this reference point does not change significantly under various operating conditions. Temperature is an important parameter which affects the performance of references. To successfully design a CMOS current or voltage reference, one must have thorough understanding of the temperature behavior of MOS transistors.

Therefore, in this section, the temperature dependency of some basic semiconductor physical properties and the effects of temperature on MOS transistor parameters such as threshold voltage and carrier mobility are described. The equations which are generally used to describe the temperature behavior of the CMOS threshold voltage and mobility are presented. This section will further explore the design of different types of current and voltage references and their performance metrics.

1.1 Semiconductor Basics

This section considers some basic properties of semiconductor materials with emphasis on the temperature dependencies of these properties. This is followed by the discussion of the temperature dependency of the threshold voltage and the carrier mobility in a MOS transistor.

1.1.1 Basic Semiconductor Effects

In this section, we review the temperature dependencies of some basic properties of semiconductor materials.

Band-gap

The difference in energy between the valence band and the conduction band is called the band-gap and is denoted by E_g. The temperature dependence of E_g for silicon expressed [1].

$$E_g(T) = 1.170 - \frac{4.73\ x\ 10^{-4}T^2}{T + 636}\ eV \tag{1.1}$$

where T is the temperature in kelvin (K).

Above 250 K, E_g can be approximated by the simpler straight-line [1] expression.

$$E_g = 1.206 - 2.73\ x\ 10^{-4}T\ eV \tag{1.2}$$

Figure 1.1 shows the temperature dependency of the silicon band-gap energy (solid line) and its first degree approximation (dashed line). As can be seen, even for the relatively broad military temperature range of -55℃ to 125℃ (218 K – 398 K), the first degree approximation can be applied.

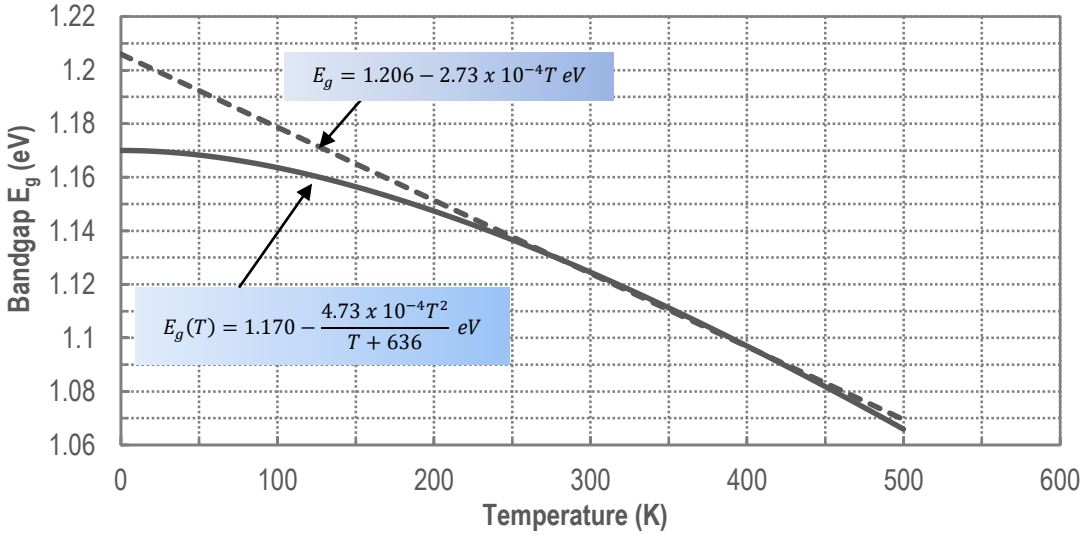


Figure 1.1: Band-gap of Silicon Dependence on Temperature

Intrinsic Carrier Concentration

The intrinsic concentration, n_i of electrons and holes depends on the amount of energy needed to break a bond (e.g., the energy band-gap) and on the amount of energy available (e.g., the thermal energy as characterized by the temperature). For silicon, n_i can be expressed as [2].

$$n_i = \sqrt{1.5x10^{33}T^3 e^{-\left(\frac{E_g}{kT}\right)}}\ cm^{-3} \tag{1.3}$$

where k is the Boltzmann's constant. At higher temperatures, thermally generated carriers can contribute to concentration of majority carriers.

Carrier Concentration

When impurity atoms are added and at relatively elevated temperature, most donors and acceptors are ionized. Employing the space charge neutrality and assuming equilibrium condition, carrier concentration, n_c, can be expressed as [1]

$$n_c = \begin{cases} \frac{N_D - N_A}{2} + \left[\left(\frac{N_D - N_A}{2}\right)^2 + n_i^2\right]^{\frac{1}{2}} & (nondegenerate\ n-type) \\ \frac{N_A - N_D}{2} + \left[\left(\frac{N_A - N_D}{2}\right)^2 + n_i^2\right]^{\frac{1}{2}} & (nondegenerate\ p-type) \end{cases} \quad (1.4)$$

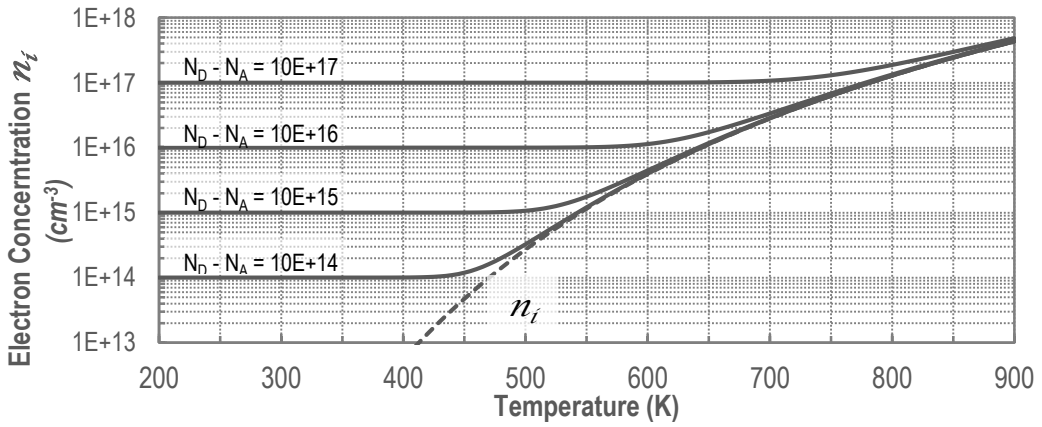
Where N_D and N_A are donor and acceptor concentration, respectively. As long as the magnitude of the net impurity concentration $|N_D - N_A|$ is much larger than n_i, the carrier concentration will be approximately equal to the substrate doping concentration, i.e. ($N_D - N_A$) for the n-type and ($N_A - N_D$) for the p-type.

Figure 1.2a shows the variation of electron concentration for an n-type (n_0) with temperature, with net doping as a parameter, above 200 K, where complete ionization is a good approximation. It can be seen that for n_i greater than about 20% of ($N_D - N_A$), n_0 increases appreciably with increasing temperature.

Figure 1.2b shows the carrier concentration in Si as a function of temperature for a donor concentration of $N_D = 10^{16} cm^{-3}$. When the temperature is low, the thermal energy is not sufficient to ionize all the impurities and so the carrier density is less than the donor concentration. This region is known as freeze-out region. As the temperature increases, all impurities are ionized and $n_c = N_D$. This condition will remain over a wide temperature range and is known as extrinsic region.

However, as the temperature increases further, the intrinsic carrier concentration, n_i, also increases to a point where the intrinsic carrier concentration becomes comparable to N_D. The temperature at which the intrinsic carrier concentration becomes equal to N_D, is called the intrinsic temperature. It is apparent that the intrinsic temperature can be delayed by increasing the impurity density.

a)



b)

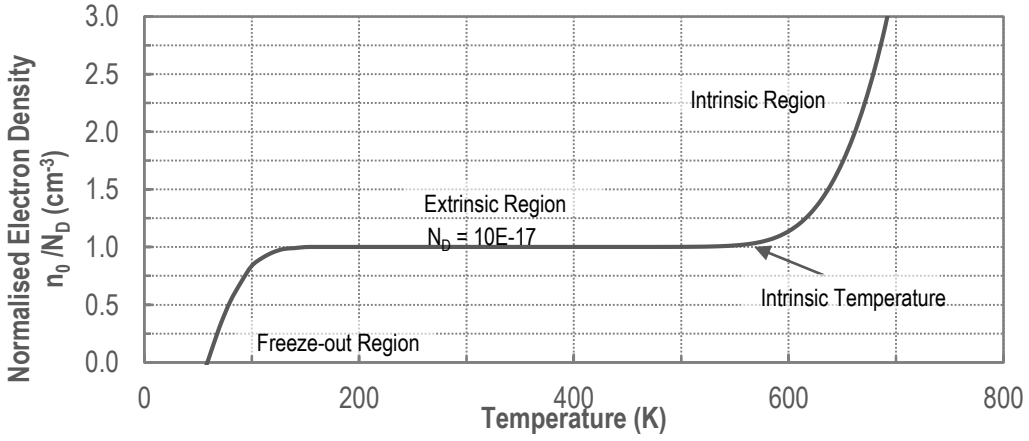


Figure 1.2: a) Temperature Dependence of Electron Concentration n_0 in n-type Si for four values of net doping. Also shown is the Temperature Dependence of *ni*. b) Temperature Dependence of Normalised Electron Concerntration n_0/N_D

Fermi Level

For an intrinsic semiconductor, the Fermi level lies about midway between the valence and conduction bands. The Fermi level in n-type materials is closer to the conduction band while for p-type material it is closer to the valence band. The value of the Fermi level depends on temperature due to the temperature dependence of n_i and the thermal voltage, $V_T = \frac{kT}{q}$, and is expressed by

$$\phi_F(T) = \pm V_T \ln\left(\frac{n_c}{n_i(T)}\right) \tag{1.5}$$

where the positive or negative sign refers to n-type or p-type semiconductors, respectively.

1.1.2 Threshold Voltage

For all known types of MOSFET devices the threshold voltage relation can be expressed in the general form [3]

$$V_{TH} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \pm 2\phi_F + \Delta V_{TH}(N_i) \pm \gamma(N_s, t_{ox}, L, W)(|V_{SB}| + 2\phi_F + V_o)^{\frac{1}{2}} \tag{1.6}$$

where the + and – sign refers to n-channel and p-channel devices, respectively.

In the above equation: ϕ_{ms} is the metal-silicon work function difference, ϕ_F is the Fermi potential of the substrate, Q_{ox} is the surface-state charge density per unit area, C_{ox} is the gate-oxide capacitance per unit $\Delta V_{TH}(N_i)$ is the threshold shift owing to a channel

implant N_i, with depth d_i, V_{SB} is the source-substrate bias, γ is the substrate body-bias factor, which depends on the substrate doping N_s, the gate insulator thickness t_{ox}, and the channel length L and width W, $V_o(N_i, N_s, d_i)$ is a correction term owing to the threshold shift implant. For enhancement devices with a ΔV_{TH} implant of the same type as the substrate, V_o has a sign opposite to that of $2\phi_F$.

The main contributors to the variation of threshold voltage with temperature are Fermi potential, ϕ_F, and the gate-semiconductor work function difference, ϕ_{ms}. The other contributors to the variation of threshold voltage with temperature are the variation in oxide capacitance, as well as the ionization of surface states. For a first-order approximation, these effects are very small and can be safely ignored [4].

For a Si-gate doped oppositely to the substrate, the contact potential is essentially determined by the pn product. Therefore, for an n-type doped gate, the gate-semiconductor work function is expressed as [4],

$$\phi_{ms} = \begin{cases} -V_T \ln\left(\frac{N_s N_p}{n_i^2}\right) & NMOS \\ -V_T \ln\left(\frac{N_s}{N_p}\right) & PMOS \end{cases} \tag{1.7}$$

where N_p is the carrier concentration in the polysilicon gate. As apparent from equation (1.7) the temperature dependence of ϕ_{ms} is determined by temperature dependence of the intrinsic carrier concentration, n_i, and of the thermal voltage, V_T.

As a first order approximation, the V_{TH} decreases linearly with temperature as given by [5]:

$$V_{TH}(T) = V_{TH0} - \alpha_{V_{TH}}(T - T_0) \tag{1.8}$$

where V_{TH0} is the threshold at temperature T_0, and $\alpha_{V_{TH}} = \frac{\partial V_{TH}}{\partial T}\Big|_{T=T_0}$.

It is apparent from Figure 1.3a that the temperature dependency of threshold voltage can be closely approximated as a linear function of temperature as shown in the equation (1.8). The temperature coefficient of V_{TH}, $\alpha_{V_{TH}}$, is obtained by differentiating equation (1.6) with respect to temperature. Noting that ϕ_{ms} and ϕ_F are the main factors which may cause a temperature dependence in the threshold voltage, $\alpha_{V_{TH}}$ is given by

$$\alpha_{V_{TH}} = \left|\frac{\partial V_{TH}}{\partial T}\right| = \left|\frac{\partial \phi_{ms}}{\partial T} + 2\frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{|V_{SB}| + 2\phi_F + V_o}}\frac{\partial \phi_F}{\partial T}\right| \tag{1.9}$$

Assuming from (1.3), where $\frac{E_{G0}}{q} = 1.21V$ is the extrapolated zero-degree band gap, it can be determined that for an n-type doped gate

$$\frac{\partial \phi_{ms}}{\partial T} = \frac{1}{T}\left[\phi_{ms} + \frac{E_{G0}}{q} + \frac{3kT}{q}\right]. \tag{1.10}$$

From equation (1.5), the temperature coefficient of ϕ_F is given by

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T}\left[\phi_F - \left(\frac{E_{G0}}{2q} + \frac{3kT}{2q}\right)\right] \tag{1.11}$$

Therefore, the $\alpha_{V_{TH}}$ becomes

$$\alpha_{V_{TH}} = \left|\frac{\partial V_{TH}}{\partial T}\right| = \left|\frac{\phi_{ms}}{T} + 2\frac{\phi_F}{T} + \frac{\gamma(N_s, t_{ox}, L, W)}{\sqrt{|V_{SB}| + 2\phi_F + V_o}}\right| \frac{\partial \phi_F}{\partial T} \quad (1.12)$$

Although the value of $\alpha_{V_{TH}}$ is assumed to be constant, there are a number of factors which affect its value. As equation (1.12) shows, the transistor length affects the value of $\alpha_{V_{TH}}$. For a short channel transistor, the depletion charge associated with channel formation is depleted from source and drain rather than from the gate. Generally this effect leads to a reduction of the substrate body-bias factor γ [3]. As a result according to equation (1.12) $\alpha_{V_{TH}}$ should decrease with decreasing channel length. Figure 1.3b shows the variation of $\alpha_{V_{TH}}$ with channel length. It show also be noted that, $\alpha_{V_{TH}}$ is independent of the width as shown by Figure 1.3b. As seen in the Figure 1.3b, $\alpha_{V_{TH}}$ can only be considered constant for lengths above 2µm. $|V_{SB}|$ is also affects the value $\alpha_{V_{TH}}$, higher body biases leads to a smaller value of $\alpha_{V_{TH}}$.

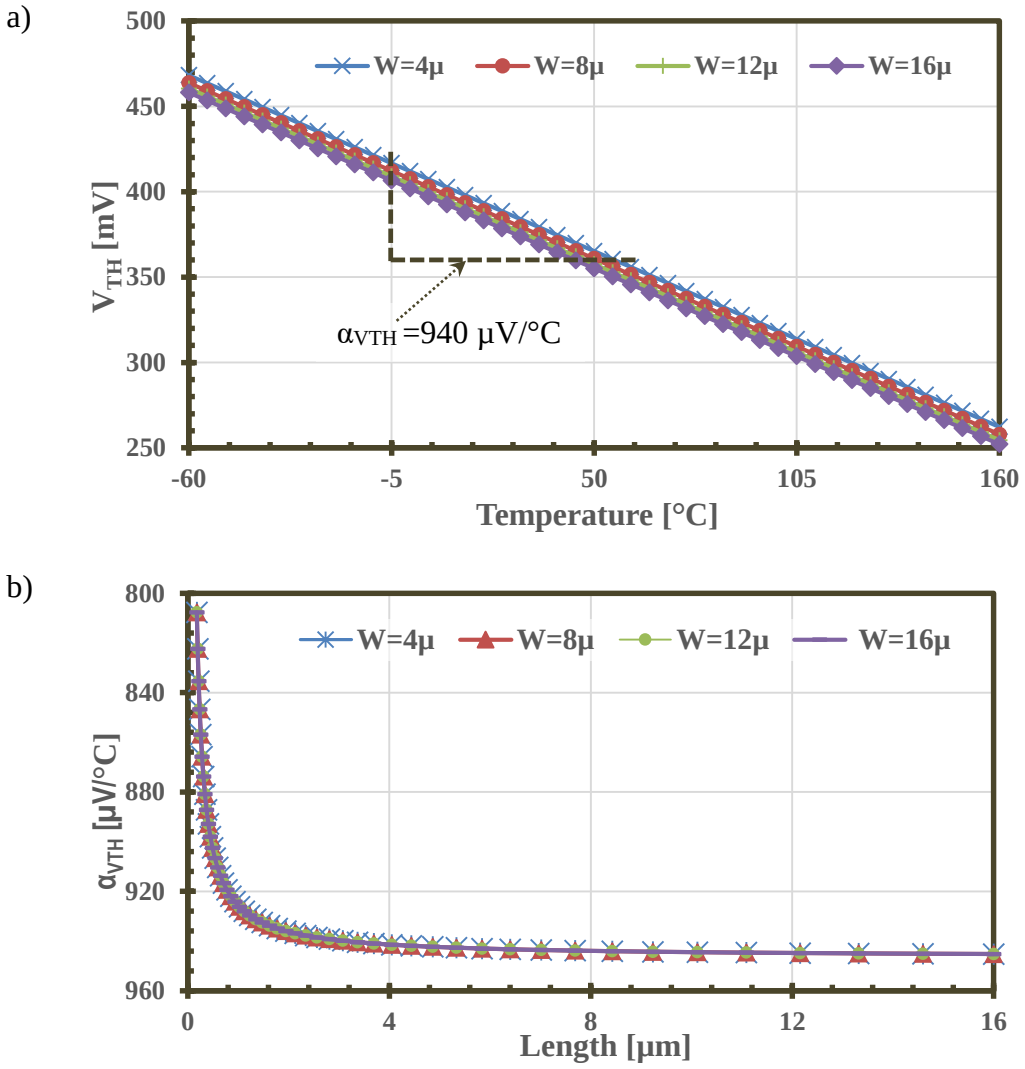


Figure 1.3: a) Temperature Dependence of Threshold Voltage of NMOS (L=2)
b) Change of $\alpha_{V_{TH}}$ with the Length of NMOS

1.1.3 Carrier Mobility

The electron and hole mobility are dependent on the impurity concentrations of donors and acceptors, on temperature and on whether the carriers are minority or majority carriers [1]. With increasing temperature, the carrier mobility due to lattice scattering decreases

because the increased phonon concentration causes increased scattering. For silicon, the mobility due to lattice scattering varies as $T^{-2.6}$ for electrons and as $T^{-2.3}$ for holes [1].

The effect of ionized impurity scattering, however, decreases with increasing temperature because the average thermal speeds of the carriers are increased [1]. Thus, the carriers spend less time near ionized impurity as they pass and the mobility due ionized impurity scattering increases with increasing temperature.

The above two effects operate concurrently on the carriers. Hence, the mobility depends on temperature as in [5]

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{1.13}$$

where μ_0 is the mobility at temperature T_0, and α_μ is the mobility temperature exponent.

1.2 Current References

Current references are essential part of most integrated circuits, since most fundamental blocks such as amplifiers, phase-locked loops (PLLs) and oscillators are dependent on a current reference. Voltage references in particular are usually derived from and are dependent on current references. It should be noted that a current reference does not have to be temperature-independent; however, its temperature dependence should be well characterized and controlled.

The processing and distribution of current signals are done more easily and faster than voltage signals and, therefore, for a given technology, the circuits designed using current-mode approach operate faster than their voltage-mode counterparts. Additionally, the current controls the transconductance of transistors, which in turns affects the static and

dynamic circuits' characteristics. Ultimately, the current sources influences the power consumption of many circuits.

A current linearly proportional to temperature, usually referred to as a proportional-to-absolute temperature (PTAT) current, is the most commonly used reference current. The popularity of PTAT currents is due to the practical, predictable and linear nature of PTAT relation. The other three commonly used current references are complementary-to-absolute temperature (CTAT), temperature-independent and squared PTAT ($PTAT^2$) current references. These currents references are explained in the next few sections.

1.2.1 PTAT Current References

A PTAT current reference generates a current which increases as temperature increases. The difference of the base-emitter voltage of two bipolar transistors is proportional to the temperature and are used for the design of PTAT current references. For an pnp bipolar transistor (BJT), the base-emitter voltage [6], V_{EB}, is given by

$$V_{EB} = V_T \ln\left(\frac{I_C}{J_S A}\right) \tag{1.14}$$

where I_C is collector current, A is the emitter area and J_s is the saturation current density.

Using equation (1.14), the difference of the base-emitter voltages of two BJT transistors, Q_1 and Q_2, can is given by

$$V_{EB2} - V_{EB1} = V_T \ln\left(\frac{I_{C1}}{J_S A_2}\frac{J_S A_1}{I_{C2}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_2}\frac{A_1}{I_{C2}}\right) \tag{1.15}$$

I_{C1} and I_{C2} are the collector currents of Q_1 and Q_2, respectively. As apparent from equation (1.15) the difference of two base-emitter voltages is proportional to the absolute temperature.

Figure 1.4 shows a PTAT current reference circuit using the difference of two base-emitter voltages [6]. Transistors M_1 and M_2 form a current mirror, developing equal currents for transistors Q_1 and Q_2, i.e., $I_{C1} = I_{C2}$. From Kirchhoff's voltage law and applying (1.15),

$$I_{C1}R = V_{EB2} - V_{EB1} = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_2}\frac{A_1}{I_{C2}}\right) \tag{1.16}$$

The current, I_{PTAT}, will then be

$$I_{PTAT} = I_{C1} = \frac{kT}{qR}\ln(n) \tag{1.17}$$

$n = \frac{A_1}{A_2}$ is the is the emitter-area ratio of Q_1 to Q_2.

The transistors M_1 and M_2 are the same size and must be laid out to match well. The channel length of these two transistors must be large enough to minimize channel length modulation errors on the PTAT current. It should be noted that the circuit has two stable points; when $I_{C1} = I_{C2}$ is the desired operating current and when it is zero current. A start-up circuit [6] is required to eliminate the possible zero current condition by injecting current at a suitable node and force the circuit to move from the zero state to the correct point of operation.

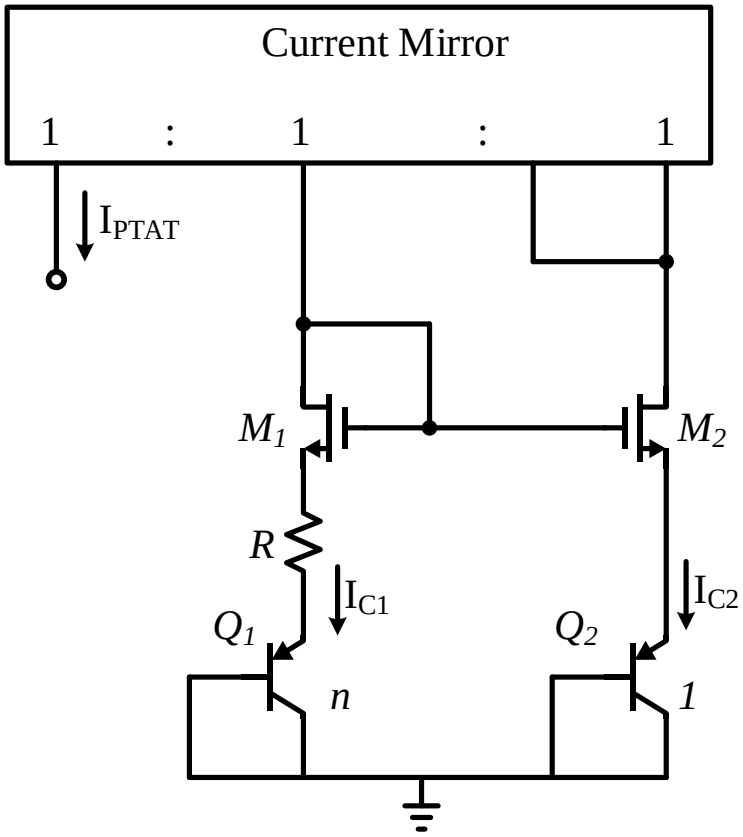


Figure 1.4: PTAT Current Generator

1.2.2 CTAT Current References

Another important current reference is a reference that generates a current which is complementary-to-absolute temperature (CTAT), the current decreases linearly with increasing temperature (the complement of PTAT). A CTAT dependence are often used for second-order voltage references as well as for first-order current references [6]. The threshold voltage of a MOSFET and the base-emitter voltage of a BJT both have a negative temperature coefficients and thus used for generating CTAT currents.

In the Figure 1.5, the base-emitter voltage is forced across the resistor (R) using the Op-amp. By mirroring the current flowing through the resistor elsewhere in the circuit a CTAT current is obtained. The CTAT is therefore given by

$$I_{CTAT} = \frac{V_{EB1}}{R} \tag{1.18}$$

From (2.6) as shown in section 2.2, the TC of the base-emitter voltage is assumed as -2.2 mV/°C at room temperature [6]. The temperature coefficient of the resistor is considered negligible, hence current shows a negative temperature dependence.

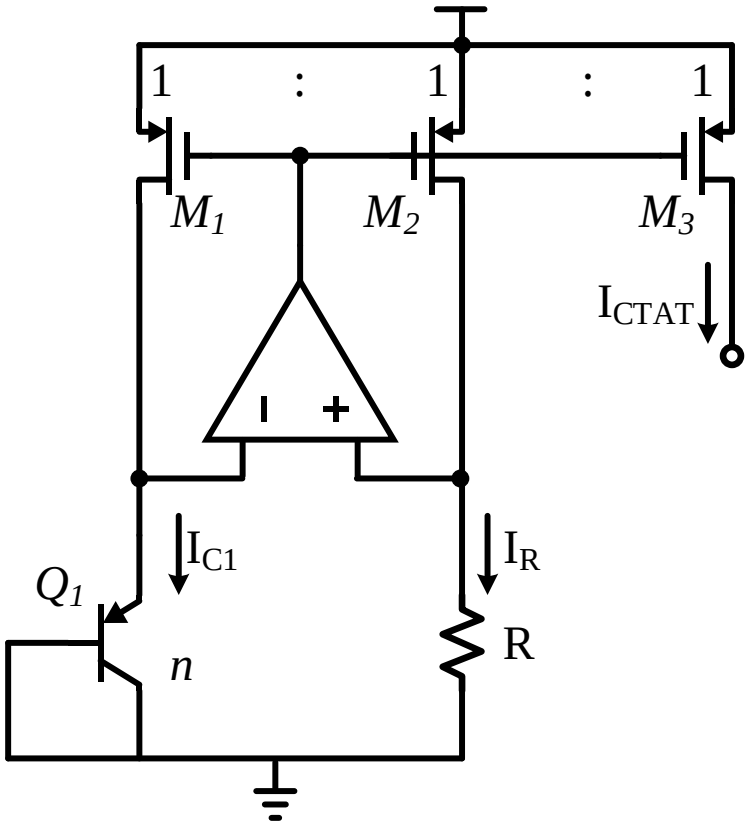


Figure 1.5: CTAT Current Generator using V_{BE}

1.2.3 Temperature-Independent Current References

Temperature-independent current generators are usually used in the design of temperature-independent voltage references. They also find applications in the biasing of circuits which require a fixed current across an operating temperature range. The simplest way to obtain a temperature-independent current is summing PTAT and CTAT currents in appropriate proportion [6]. These summation usually leads to first-order temperature-independent (quasi-temperature-independent) current.

Figure 1.6 illustrates one possible design for summing the PTAT and CTAT currents. In this circuit, I_{PTAT} is generated by the loop consisting of transistors Q_1 and Q_2 and resistor R_1 and the CTAT current is created by forcing the V_{EB} of transistor Q_1 across the two R_2 resistors. It is again assumed that the temperature coefficients of the resistors are very low. The Op-amp is so controlled that the voltages at node a and b are equalized [7], hence:

$$I_{PTAT}R_1 = V_{EB1} - V_{EB2} = \frac{kT}{q} ln(\, n) \tag{1.19}$$

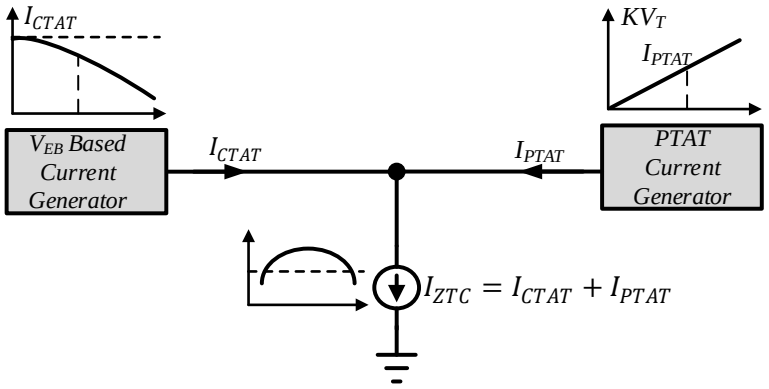
$$I_{PTAT} = \frac{kT}{qR_1}\ln(n) \tag{1.20}$$

$$I_{CTAT} = \frac{V_{EB1}}{R_2} \tag{1.21}$$

Since, the gates of M_1, M_2, and M_3 are connected to a common node the current I_1, I_2, and I_{OUT} becomes the same value due to the current mirror. Henceforth:

$$I_{OUT} = I_2 = I_1 = I_{PTAT} + I_{CTAT} = \frac{kT}{qR_1}\ln(n) + \frac{V_{EB1}}{R_2} \tag{1.22}$$

a)



b)

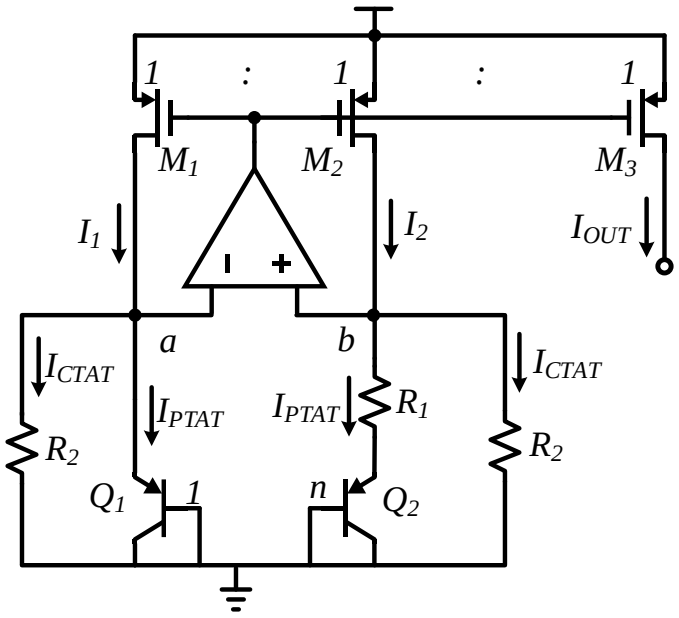


Figure 1.6: Temperature-Independent Current Reference a) Concept and b) Implementation

Another simple technique for the generating a temperature-independent current is to force a temperature-independent voltage across a resistor with a very small temperature coefficient. This technique requires a temperature-independent voltage reference, hence is restricted to certain applications.

1.2.4 PTAT^2 Current References

A PTAT^2 current is a current which is proportional to the square of temperature. PTAT^2 current references are commonly used in voltage reference for curvature compensation. Most V_{GS} –based references use some kind of PTAT^2 current for temperature compensation as is shown in section 3.2.1.

A simple method of implementing a PTAT^2 current reference is to force a PTAT voltage through a resistor which shows a PTAT dependence. This method however depends on the technology. Similarly, the Gilbert Multiplier with a positive temperature coefficient resistor can be used in CMOS technologies to generate a PTAT^2 current [6].

Figure 1.7 illustrates a CMOS implementation for a PTAT2 current generator [7]. In this circuit, transistors N_1 and N_2 operate in sub-threshold region, transistors N_0 in the saturation region and N_R operates in the linear region [8]. The transistors P_0 –P_3 forms a four-transistor current mirror with a unity mirroring ratio. Using KVL for the voltage loop composed of transistors N_1, N_2 and N_R, the output current can be expressed as

$$I_1 = \frac{V_{GSN_1} - V_{GSN_2}}{R_{DSN_R}} = \frac{mV_T}{R_{DSN_R}} \ln\left(\frac{(W/L)_1}{(W/L)_2}\right) \tag{1.23}$$

The R_{DSN_R} is the output resistance of transistor N_R, and is given by

$$R_{DSN_R} = \frac{1}{K_{N_R}\left(V_{GSN_R} - V_{TH}\right)} \tag{1.24}$$

also,

$$V_{GSN_0} = V_{GSN_R} = V_{TH} + \sqrt{\frac{2I_0}{K_{N_0}}} \tag{1.25}$$

where $K_i = \mu C_{ox}\left(\frac{W}{L}\right)_i$ and m is gate-to-surface coupling coefficient (sub-threshold slope factor).

Since the current mirror has unity mirroring factor, $I_0 = I_1 = I_2 = I_{OUT}$, hence using the equations (1.23), (1.24), and (1.25) the output current can written as

$$I_{OUT} = \frac{2m^2 K_{N_R}^2}{K_{N_0}} V_T^2 \ln^2\left(\frac{(W/L)_1}{(W/L)_2}\right) \tag{1.26}$$

Note K_i depends on mobility. If in a technology the α_μ (the mobility temperature exponent) small and the mobility could be considered constant over the desired temperature range, the current I_{OUT} would be proportional to the square of the temperature.

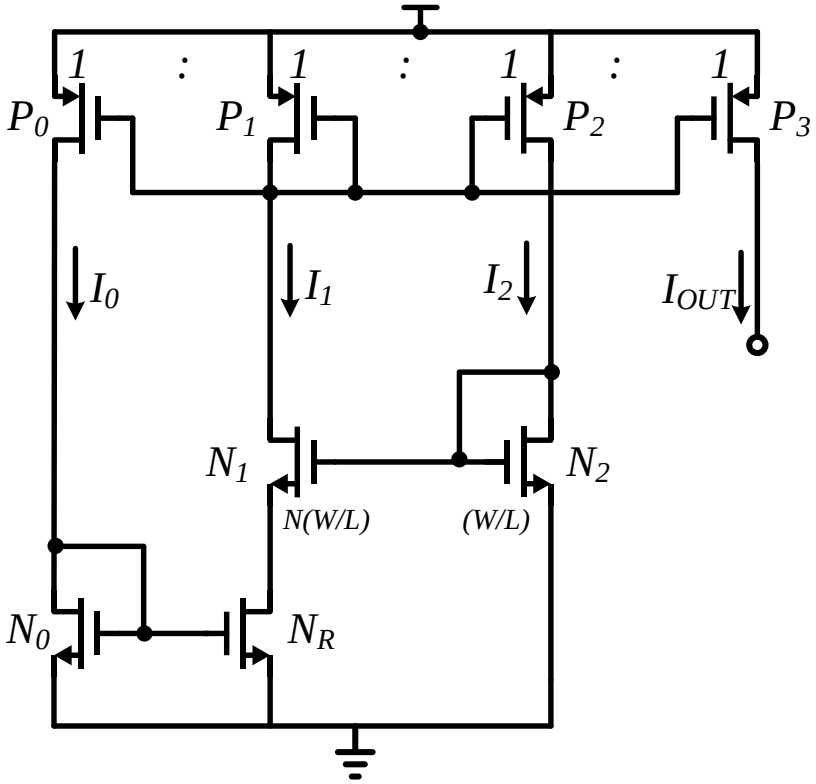


Figure 1.7: CMOS PTAT^2 Current Reference

Precise, integrated current references are usually difficult circuits to design [6]. This inaccuracies are due to the low tolerance (on the order of 10 -20% [6]) of the sheet resistance in digital CMOS processes. As seen from the various current references discussed above, most current references are derived from a voltage across a resistor, hence the tolerance of the resistor translates directly to the overall intolerance of the current reference.

1.3 Voltage References

Voltage references (VRs) are essential components in modern SOC applications. In order to ensure compatibility with the rest of the system, VRs are preferentially implemented with a standard digital CMOS process. Due to their higher accuracy and predictability, voltage references are more popular than current references in circuit design [6]. Since current references are usually derived by forcing a voltage across a resistor, the accuracy of the resistor (which is about 10% to 20% for integrated resistors [6]) directly translate into the accuracy of the reference current. Reference voltages on the other hand are usually based on resistor ratio making voltage references more accurate than the current references.

1.3.1 Types of Voltage References

There are various ways of realizing a voltage reference. Current mirrors, diodes and current references are usually the building blocks for voltage references. By the basis of technology in which the reference is constructed or the method of deriving the constant output voltage, voltage references can be grouped into four main categories as shown in Figure 1.8. Threshold voltage is the most obvious way of deriving a reference voltage in a strictly MOS technology. In bipolar processes, the emitter base junction of a BJT can be used to derive the band-gap voltage of silicon for use as a reference voltage. It is also possible to create a BJT, which is adequate to extract the band-gap voltage of silicon in a MOS process.

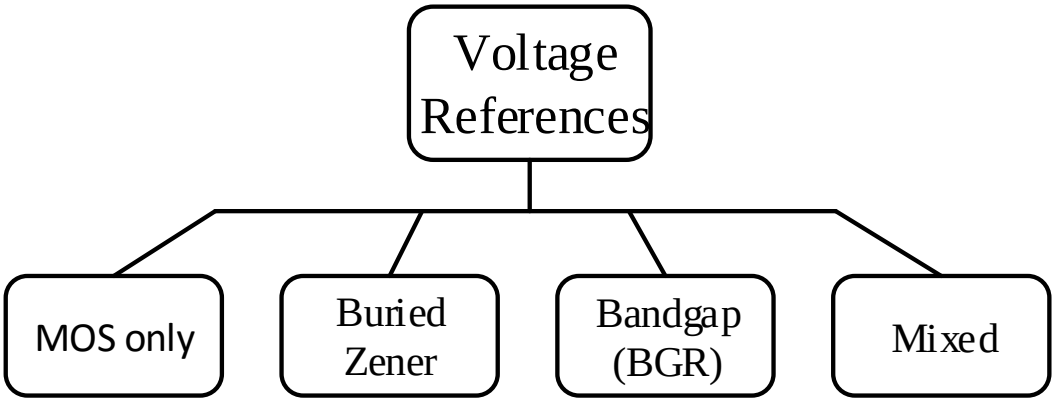


Figure 1.8: Categories of Voltage References

MOS Only Reference

With the drive for the integration of various mixed signal functional modules into one System on Chip (SOC), there have been numerous attempts to design a good voltage reference using only MOS components.

The most obvious method of producing a MOS Only reference uses the difference between two different threshold voltages to extract the constant reference voltage as implemented in [9]. This design of course is based on the availability of a process in which there are two different threshold voltages for the same type of device (either NMOS or PMOS). Such feature can be obtained by using a selective channel implant, by using different materials for the gate stack, or by doping differently the poly-silicon gates. This cannot be done in the standard CMOS process because of the additional fabrication steps required.

Another type of MOS only voltage references, implemented with a standard CMOS technology, are based on a weighted difference between the gate-source voltages of two

MOS transistors [10]. Other methods take advantage of characteristics of a MOS devices operating in sub-threshold to achieve stable references [11], [12], and [13].

Buried Zener References

The most basic type of reference that can be constructed uses the reverse breakdown voltage of a zener diode. This is usually implemented as shunt regulator by using a resistor and a Zener diode [14] as shown in figure 1.8a. This reference has very little dependence on the supply but it does have a fairly strong temperature dependence.

A much temperature stable reference can be achieved by thermally compensating the Zener diode as shown in Figure 1.8b. The thermal compensation of the Zener diode is done by connecting in series with the Zener diode a forward-biased diode having an equal but opposite temperature coefficient (TC). Thermal stability can further be enhanced by substrate thermo-stating [14]. This can achieve a reference with a typical TC of 0.3 ppm/°C.

A common problem with references based on breakdown Zener diodes is noise, especially avalanche noise, which affects devices with breakdown above 5V, where avalanche breakdown predominates [14]. Some of this noise can be eliminated if the zener diode is buried in the substrate away from the surface giving rise to buried Zener references.

A Zener reference is typically used in applications where extremely high precision is necessary. The tailor made processes that are required are generally significantly more expensive than a standard digitaI CMOS process which makes a buried zener reference a poor choice for inexpensive mixed signal ICs. Additionally the best breakdown voltages

range from 6 V to 7 V, hence usually require supply voltages on the order of 10 V to operate [14].

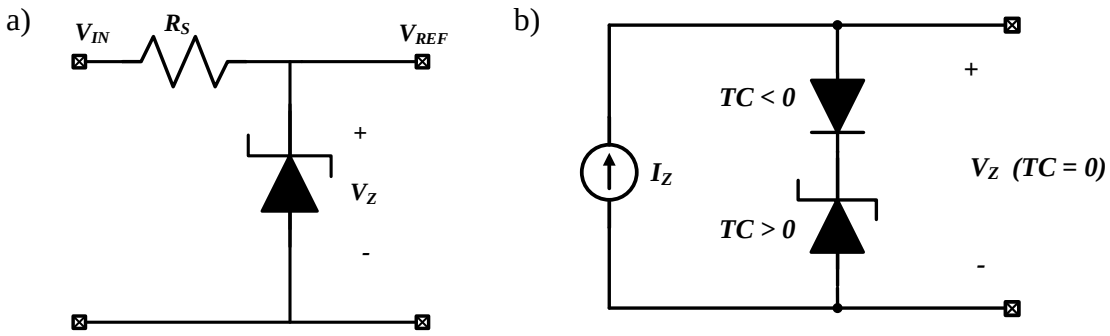


Figure 1.9: Zener Diode References a) Zener Diode as Shunt Regulator b) Thermally Compensated Breakdown Zener Diode

Bandgap References (BGR)

Due to the limitation of the Zener diodes discussed above, for applications with supply voltages below 10 V, bandgap voltage references are used since the output is primarily determined by the bandgap voltage ($V_{G0} = \frac{E_{G0}}{q} \approx 1.205V$). This type of reference uses the base emitter junction of two or more bipolar transistors to extract the 0K bandgap voltage (V_{G0}) of silicon.

BGRs relies on the temperature dependence of the base-emitter voltage (V_{BE}) BJTs or an equivalent forward-biased diode.

Mixed References

A BiCMOS processes can integrate both BJT and MOS devices on a single chip. Unfortunately, these processes are much more expensive than a standard digital CMOS process and are therefore not a valid for SOC applications. However, it is possible to create two types of bipolar transistors in a digital CMOS process without adding any process steps. These transistors may not be high gain or high speed devices but they function consistently from chip to chip, and therefore, can be used to extract the bandgap voltage for a reference. In modern literature, any reference that is dependent on the bandgap voltage of Si is considered a bandgap reference. Such references are discussed in the next section 2.

1.3.2 Curvature-Correction Techniques

A reference voltage temperature dependence can be represented as a polynomial shown below

$$V_{REF}(T) = V_{REF}|_{T_0}\left(1 + TC_1\left(\frac{T}{T_0}\right) + TC_2\left(\frac{T}{T_0}\right)^2 + TC_3\left(\frac{T}{T_0}\right)^3 + \cdots\right) \qquad (1.27)$$

T_0 is the reference temperature, TC_1 represents the first-order (linear) temperature dependence, TC_2 the second-order, and so on. Higher than first-order terms are usually lumped together and described as the "curvature" of the drift.

VRs can be categorized into different performance levels (i.e. zero-order, first-order, or second-order). Zero-order references are the most rudimentary since they are typically not temperature compensated. The first-order references are references in which the

dependence of the polynomial's first-order term on temperature is effectively cancelled. These references typically exhibit TCs ranging from 50 to 100 ppm/°C [6]. Second-order as well as high-order voltages references, compensate for one or more higher-order temperature dependent terms.

Zero-Order Compensation

This is the simplest and most rudimentary way generate a reference voltage. The zero-order is usually achieved by forcing current to flow through a pn junction diode. The circuit shown in Figure 1.8a is one of the most popular zero-order references. The other implementation uses a forward biased diode; this reference typically has a TC of -2.2 mV/°C [6].

First-Order Compensation

The BGRs discussed in section 1.3.1 is the most popular first-order reference. First-order compensation usually successfully compensates for the linear temperature term of BJT base-emitter voltage, V_{BE}, but usually does not compensate for the nonlinear term [6].

A PTAT term based on thermal voltage (V_T) is amplified by a factor and counter-balanced by the linear temperature term of BJT base-emitter voltage, which is a CTAT. The basic concept is clearly illustrated in the classical bandgap reference by WIDLAR (1971).

$V_T = \frac{kT}{q}$ has a positive TC equal to 0.086 mV/°C whilst V_{BE} has a temperature coefficient of 2.2 mV/°C. Hence, a first-order temperature compensation is obtained by properly combining V_{BE} and V_T given by

$$V_{REF} = V_{BE} + KV_T \tag{1.28}$$

where $K = -\frac{TC(V_{BE})}{TC(V_T)} = 25.6$ [15].

There two main ways of implementing a first-order reference. The first method is by properly adding two voltages proportional to V_{BE} and V_T to obtain a temperature-independent reference. This configuration known as the voltage-mode requires a minimum supply above 1.2 V and output is usually approximately $V_{G0} = 1.2\,V$.

To generate a reference sub- 1 V first-order BGR, a current-mode bandgap is used. In this implementation two currents, one proportional to V_{BE} and the other proportional to V_T , are properly scaled and summed up. The summed current, which is temperature-independent, goes through a resistor, generating a temperature-independent voltage. This method allows BGR to be implemented with sub-1 V supplies [7]. Figure 1.9 shows the implementation of first-order BGRs using the two techniques.

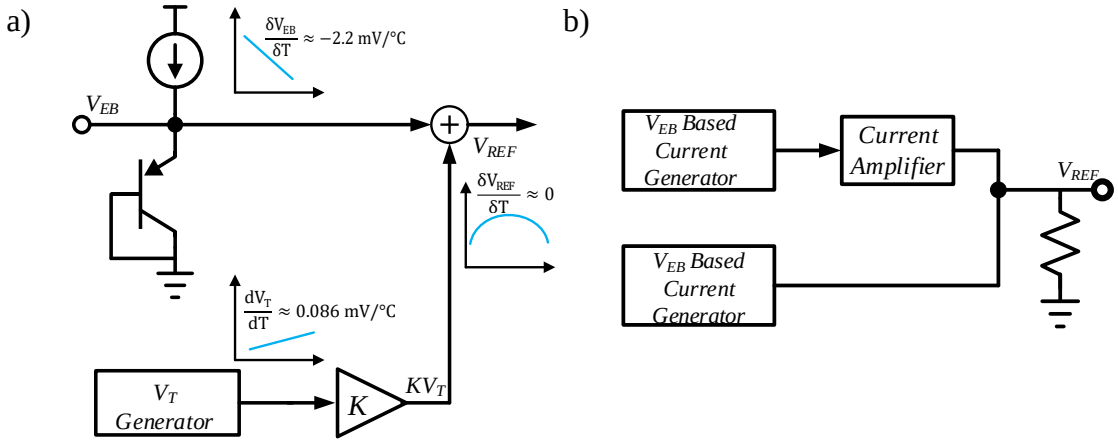


Figure 1.10: Conceptual Implementation of a First-Order Reference a) Voltage-Mode b) Current-Mode

Second-Order Compensation

The first-order references discussed above are not adequate for high precision and high performance systems such as data converters and power converters in battery powered ICs. This has resulted in the development of higher-order, curvature compensation techniques as in [12], [14], [16], and [17].

The second-order references do not just cancel the linear temperature term of V_{BE}. They also attempt to approximately cancel the nonlinear component of equation (2.3). This process can be accomplished by one of two separate techniques (or a combination of the two).

The first method is to make the value of $(\eta - \theta)$ in equation (2.3) zero. When this is done successfully, there would be no nonlinear temperature-dependent term in (2.3). Typically $\eta \approx 4$ for most processes, henceforth a perfect cancelation of the nonlinear term could be achieved by using a very strongly temperature-dependent bias current. Unfortunately, building a fourth-order temperature-dependent current is complicated, in fact many design use only $PTAT^2$ sources. The other technique, used by many of curvature- compensated references, is to simply add a curvature-correcting component which increases with temperature in a nonlinear fashion.

Second-order compensation, essentially tries to cancel the second-order term in the Taylor-series (equation (2.4)) of the diode relationship in equation (2.3). The traditional method of doing such compensation is through the addition of a $PTAT^2$ term to the output voltage relation of a first-order bandgap reference [6]. In this, the negative temperature dependence of the logarithmic term of V_{BE} is canceled with a positive quadratic term [6].

Figure 1.10a shows the temperature characteristics achieved by a typical PTAT^2 curvature-compensated reference.

One implementation of this technique is illustrated in Figure 1.10b [15]. A PTAT correction voltage KV_T is added to V_{EB} to cancel out the linear temperature variation of V_{EB}. After the PTAT correction voltage is added, the reference output V_{REF} will exhibit mostly the quadratic temperature variation as shown in the Figure 1.10b. Using a PTAT^2 correction voltage FV_T^2, the quadratic temperature variation of the V_{EB} is cancelled at the final reference output.

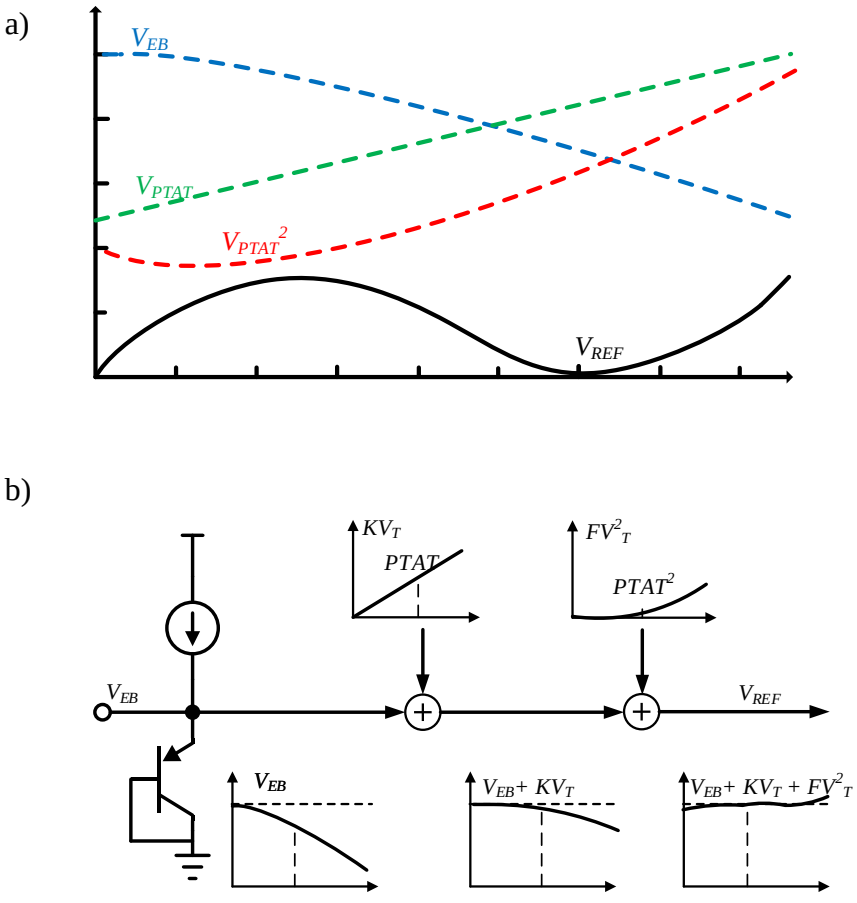


Figure 1.11: Squared PTAT Curvature-Correction a) Typical Temperature Dependence b) Implementation Concept

State-of-the-Art Curvature Correction Techniques

Various design approaches can be adopted to perform curvature correction to yield both the second-order compensation discussed above and higher compensation. One method is piecewise-linear compensation [19], [20]. Other techniques uses temperature-dependent resistor ratios. This method usually involves using resistors of different TCs to achieve a nonlinear or piecewise curvature correction [16] and [18].

The other is to cancel the nonlinearity using an exponential temperature compensation [21]. Figure 1.11 shows the temperature of a piecewise linear curvature-corrected bandgap reference [6].

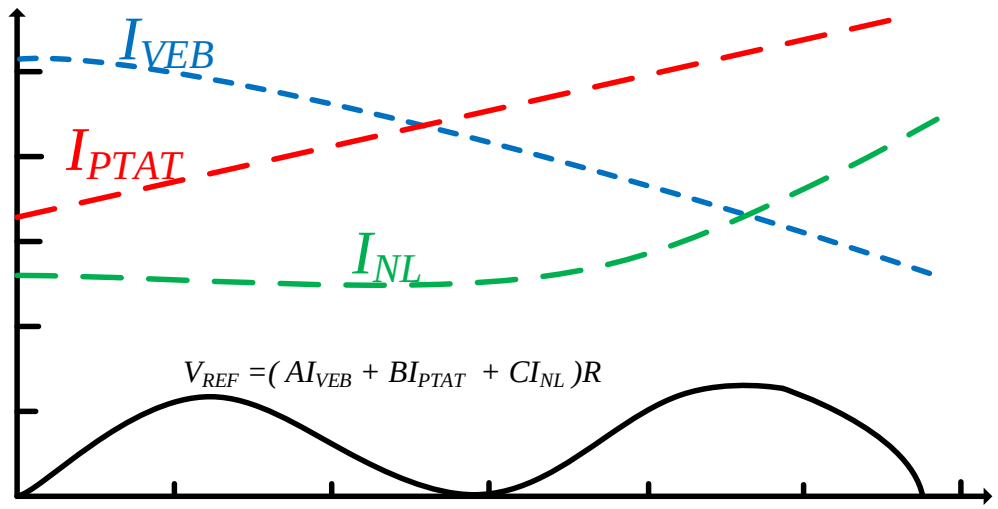


Figure 1.12: Temperature Dependence of Piecewise-Linear Curvature Corrected Bandgap

1.4 Definitions and Metrics

Power management circuits, data converters, oscillators and a variety of other circuits require some kind of reference standard to function at the desired degree of accuracy. Hence the primary requirements of voltage references (VRs) are accuracy and stability [14], [22].

VRs come in many forms and offer different features, but in the end, accuracy and stability, are a voltage reference's most important features [22], [14], as the main purpose of the reference is to provide a known output voltage. Variation from this known value is an error. Voltage reference specifications usually predict the uncertainty of the reference under certain conditions.

The ability of a voltage reference (VR) to maintain a constant output under varying external conditions is characterized in terms of performance parameters such as line sensitivity, and temperature coefficient. The long-term stability is also important metric for voltage references. These performance metrics for voltage reference applications are discussed in the next few sections.

1.4.1 Initial Accuracy

The initial accuracy of a VR indicates how close to the stated nominal voltage the reference voltage is guaranteed to be at room temperature under stated bias conditions [23].While the initial output voltage may vary from unit to unit, if it is constant for a given unit, then it can be easily calibrated [22]. This specification is usually for room temperature only, with a defined input voltage and load current. It provides a starting point

for most of the other specifications. In many applications, initial accuracy is the most important specification. Initial accuracy tolerance can be affected by package stress, so proper control of the solder temperature profile is essential and twisting of the PCB must be kept to a minimum. Typical initial accuracies are in the range of 1% to 0.01%, which translates into 1 LSB (least significant bit) error in 6 to 12 bit converters [24].

1.4.2 Temperature Coefficient (TC)

The temperature coefficient is a measure of a VR's ability to maintain the prescribed output voltage under varying temperature. The TC or "drift", has unit of parts-per-million per degree Celsius (ppm/°C). The temperature coefficient can be specified over several different temperature ranges, including the commercial temperature range (0 to 70°C), the industrial temperature range (-40 to 85°C), and the extended temperature range (-40 to 125°C) [23].

There are several methods of defining TC, with the "box" method being used most often [23]. This method to calculates maximum total error over the specified temperature range, whereas other methods use the values of the V_{REF} at the endpoints of the temperature range (T_{MIN}, T_{MAX}). The endpoints method fails to account for curvature (higher-order) in the temperature change, hence are usually not ideal. It should however be noted that the box method may under-estimate the TC if the temperature of the application is smaller than the range over which the TC is specified [23].

Equation (1.29) and (1.30) shows the formula for the box and endpoint measurement respectively.

$$TC_{BOX} = 10^6 \left(\frac{V_{REF\ MAX}|_T - V_{REF\ MIN}|_T}{V_{REF}|_{T_0}} \right) \left(\frac{1}{T_{MAX} - T_{MIN}} \right) \quad (1.29)$$

$$TC_{ENDPOINTS} = 10^6 \left(\frac{V_{REF}|_{T_{MAX}} - V_{REF}|_{T_{MIN}}}{V_{REF}|_{T_0}} \right) \left(\frac{1}{T_{MAX} - T_{MIN}} \right) \quad (1.30)$$

The Figure 1.12 shows the different methods for TC calculation [23].

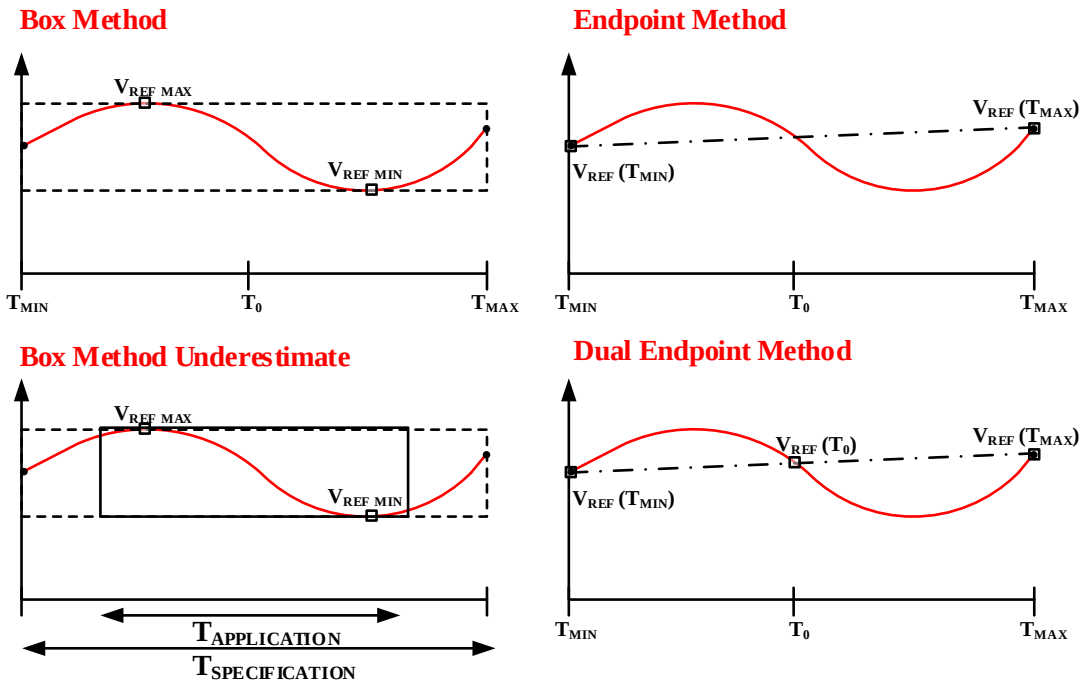


Figure 1.13: Different Methods for TC Calculation

1.4.3 Thermal Hysteresis

A change in output voltage as a result of a temperature change. When voltage references experience a temperature change and return to the initial temperature, they do not always have the same initial output voltage. Thermal hysteresis is challenging to correct and is a major source of error in systems that experience temperature changes of

25°C and above [25], [24]. Thermal hysteresis is not tested in production and datasheets only provide a typical shift [23], which is usually about 25 ppm.

1.4.4 Long-Term Stability

Long-term stability describes the typical shift in the reference voltage (V_{REF}) after 1000 hours (6 weeks) of continuous operation under nominal operating conditions and is it also an important performance metric for VRs, particularly for repeatability within a system. The long-term stability in a voltage reference increases with the square root of the elapsed time, usually expressed in ppm/1000 hours [23]. Longer-term shifts are caused by the aging of the circuit. The buried Zener references typically have a long-term stability of 5-20 ppm/1000 hours which is the best for monolithic references [24] whereas bandgap references generally have a long-term stability of 20-120 ppm/1000 hours.

1.4.5 Power Supply Rejection (PSR)

To ensure system robustness, an "ideal" voltage reference circuit must reject fluctuations in supply voltage and generate a clean reference voltage. PSR is often used to evaluate how well a voltage reference circuit rejects supply noise or spurious signals at a given frequency coupled on the supply rails, which can be expressed in dB as

$$PSR = 20\log\left(\frac{V_{REF}}{V_{DD}}\right) \tag{1.31}$$

The PSR over a wide frequency range describes the susceptibility of the voltage reference circuit to power supply noise.

1.4.6 Line regulation

An error produced by a change in the input voltage, $\frac{\Delta V_{REF}}{\Delta V_{DD}}$. This is a dc specification and does not include the effects of ripple voltage or line transients. The importance of line regulation depends on the tolerance of the input supply. The line regulation (LR) of a VR expressed in ppm [23] is given by

$$LR = 10^6 \left(\frac{V_{REF}|_{V_{DD_{MAX}}} - V_{REF}|_{V_{DD_{MIN}}}}{V_{REF}|_{V_{DD_{MIN}}}} \right) \left(\frac{1}{V_{DD_{MAX}} - V_{DD_{MIN}}} \right) \tag{1.32}$$

Due the recent drive for low power mixed-mode SOC applications, power consumption, noise, area and power supply rejection (PSR) has become very important design criteria for voltage references (VR).

2. CMOS BANDGAP VOLTAGE REFERENCES

Since the mid 1970's, bandgap references (BGR) circuits have been widely used in analog IC. Most BGR circuit require some kind of diode but unfortunately, a good diode is usually not available in most standard digital CMOS processes. It is usually possible to create two types of bipolar junction transistor (BJT) devices from the standard structures in a digital CMOS process. One of these structures is similar to a lateral BJT device in a typical bipolar process and other is similar to that of a standard vertical device that can be found in several bipolar processes.

In this section, we briefly describe pn diodes temperature characteristics and the implementation of BJTs in CMOS processes. We will also discuss an implementation of low power bandgap voltage reference in CMOS technology.

2.1 Bipolar Transistors (BJT) in CMOS

A realistic BJT has certain design and specified characteristics. The device doping has to follow a specific pattern; emitter needs to have the highest doping, followed by the base, with the collector having the lowest doping. The base of ideal BJT is usually very narrow to increase the speed of the device. A narrow base helps reduce the amount of charge that can be stored on the base and hence improves the device's switching speed [1]. The collector must have a much larger area than the emitter to allow as many charge carriers as possible to be collected. This design pattern improves the current gain of the device.

In a standard digital CMOS process it is not possible to control these parameters since only the standard CMOS structures can be used. It is not possible for a designer to change

any of these process parameters. In typical single well CMOS processes, either NPN devices (p-well process) or PNP (n-well process) devices are available.

The first transistor type is a lateral transistor that has a cross-section similar to that in Figure 2.1a. These lateral transistors is an arrangement of the standard MOSFET structure into a topology that will function as a bipolar transistor and is usually available twin-well process like the $IBM180\ CMOS7RF$ process. It is modeled as an npn, with the n+ cathode as the emitter, the p-well base, and deep n-well as the collector. Unfortunately they do not have ideal BJT characteristics.

The other structure is a vertical pnp transistor as shown Figure 2.1b, with the p+ junction, n-well, and substrate forming the emitter, base, and collector respectively. The vertical device is much simpler than the lateral device but has one significant drawback. To create the collector it is necessary to use the substrate as an active terminal in the transistor; meaning the collector voltage of all vertical devices on a single chip must be connected to the same potential. Hence, it is usually used as simple two terminal device (diode) in which the N-well and the substrate ring surrounding the device are shorted together.

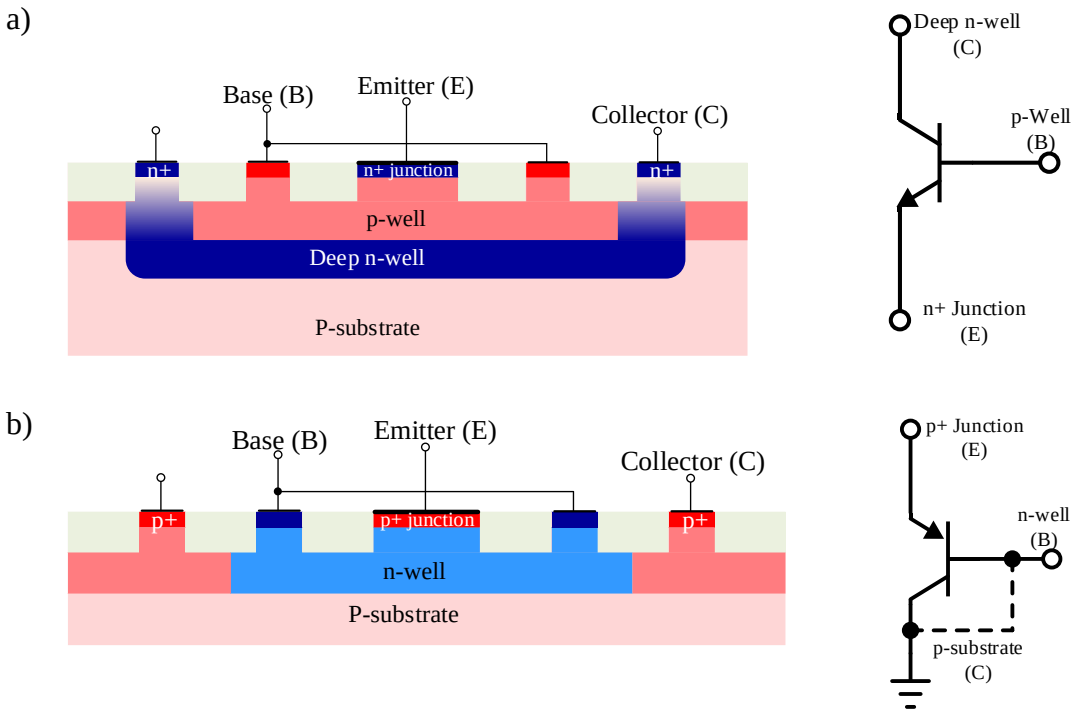


Figure 2.1: CMOS BJTs a) Lateral NPN b) Vertical PNP

2.2 V_{EB} Temperature Characteristics

The collector current, I_c, and forward voltage of the emitter-base diode of a *pnp* BJT can be express as [14]

$$V_{EB} = V_T \ln\left(\frac{I_c}{I_s}\right) \tag{2.1}$$

The saturation current, I_s, is given by [6]

$$I_s = CT^{\eta} e^{-\frac{V_{G0}}{V_T}} \tag{2.2}$$

where C is a temperature-independent constant and η is a process dependent constant ranging from 3.6 to 4. The I_c can be expressed a temperature dependent current given by:

$$I_c = DT^{\theta} \tag{2.3}$$

D is a constant and θ is a number defining the temperature dependence of the current forced through the collector.

Using (2.1)-(2.3) and solving for the constants at reference temperature, T_0, the temperature dependence of V_{EB} can be expressed as

$$V_{EB} = V_{G0} - \frac{T}{T_0}[V_{G0} - V_{BE}(T_0)] - [\eta - \theta]V_T \ln\left(\frac{T}{T_0}\right) \tag{2.4}$$

Obtaining the Taylor-series expansion of the logarithmic components of equation (2.4), the temperature dependence, V_{EB}, can be expressed as [6]

$$\begin{aligned} V_{EB} = V_{G0} + (\eta - \theta)V_T|_{T_0} - \left[\frac{V_{G0} - V_{EB}(T_0) + (\eta - \theta)V_T|_{T_0}}{T_0}\right]T \\ - \left\{\frac{(\eta - \theta)V_T|_{T_0}}{T_0}\left[T \ln\left(\frac{T}{T_0}\right) - T + T_0\right]\right\} \end{aligned} \tag{2.5}$$

where $V_{EB}(T_0)$ is the base-emitter voltage at T_0 and $V_T|_{T_0}$ is the thermal evaluated at T_0.

An understanding of the V_{EB} relation above is central for the designing of accurate bandgap references.

Based on (2.1) and (2.2), the TC of the V_{EB} is usually approximated as:

$$TC(V_{EB}) = \frac{\partial V_{EB}}{\partial T} = -\left(\frac{V_{G0} - V_{EB}}{T} + \frac{3k}{q}\right) \tag{2.6}$$

assuming $V_{EB} = 650\ mV$ at room temperature, we get $TC(V_{EB}) = -2.2\ mV/°C$

2.3 Commercial Voltage Reference ICs

Since the 1960s when the discrete Zener diode was introduce, monolithic voltage references have evolved over many generations [24], so that today they are available in various distinct categories. These include the Zener, MOS only, bandgap, the buried-zener, the XFET® from Analog Devices, along with the FGA™ from Xicor/Intersil and mixed references. Integrated voltage references are now manufactured using various processes [24] (e.g. Bipolar, JFET, complementary-bipolar, Bi-CMOS, CMOS).

The new design processes has led to high thermal stabilities, improved initial accuracies, lower-power, lower noise, smaller chips and packages. Voltage references today are subdivided into different types which includes micro-power, ultra-high precision, low dropout, low noise, shunt and general purpose references [24]. A lot of these references have added features for high performance applications such as automotive, space, defense, and avionics. Some references even allow for user trimming, filtering and adjustment of the reference voltage.

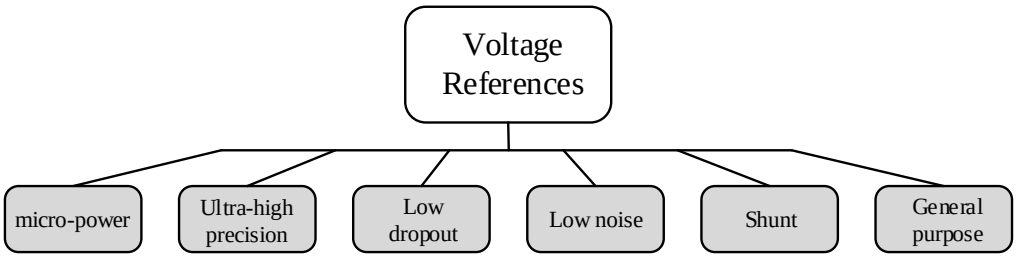


Figure 2.2: Types of Commercial Monolithic Voltage References

The invention of the bandgap references by Bob Widlar in the late 1960's [24] was probably due the fact that the references that was created by Zener diodes were sensitive to temperature drift, noisy and required more than 5 V to function [24]. Even though Zener references today are much less noisy and offers better temperature stability, they still require high voltages to function, hence are not ideal for low voltage applications. Hence the bandgap reference is the most popular for low voltage designs.

The LM10 of National Semiconductor's (now part of Texas Instruments Inc.) was the earliest device to use the first generation bandgap references. During the inventions of the BGR by Bob Widlar, Analog Devices Inc. also introduced its legendary AD580. The AD580 was the first precision BGR [24] and based on what is referred to today as the *Brokaw cell* (we will discuss the CMOS implementation of it in the next section).

Since its invention, BGRs have been refined and manufactured by various analog product makers [24]. Although the two-terminal (shunt) bandgaps are most common, there are more sophisticated series types. Table 2.1 provides a summary of some of the popular proprietary bandgap based voltage reference products. Table 2.2 performance comparison of selected bandgap references in today's market.

Table 2.1: Popular Proprietary Bandgap Based Voltage Reference Products

Manufacturers	**Products**
Analog Devices	ADR34xx, ADR280, REF19x
Intersil	ISL21010-xx, ISL21080-xx, ISL21060-xx
Linear Technology	LTC6655, LT1004, LM185, LT1034, LT1634
Maxim	MAX6072, MAX6071, MAX6070, MAX6010, MAX8069
Microchip	MCP1525/41
Texas Instruments	LM412x, LM4132, LM4140, REF29xx, REF3012

Table 2.2: Performance Comparison of Selected Bandgap References in Today's Market

Specification	**REF3012**	**MAX6070**	**REF191**	**ISL21080-09**	**MCP1525/41**
Technology	CMOS	N/A	CMOS	N/A	CMOS
Temperature Range (℃)	-40 – 125	-40 – 125	-40 – 85	-40 – 85	-40 – 85
Supply Voltage (V)	1.8 – 5.5	2.7 – 5.5	3– 15	2 – 5.5	2.7 – 5.5
Supply Current (µA)	42	130	45	0.35	95
Vref (V)	1.250	1.250	2.048	0.9	2.5
Initial Accuracy (± %)	0.2	0.08	0.1	0.7	1
TC (ppm/℃)	35	8	10	50	50
LR (µV/V)	60	100	16	30	107
PSR (dB) @120Hz	-62	-100	-82	-40	-75
Output Voltage Noise (0.1 to 10Hz, µVp-p)	14	3.6	20	40	145

2.4 The Classical CMOS Bandgap Reference

The most common bandgap reference (BGR) is a first order voltage reference. These reference is based on summing the voltage of a forward-biased diode (or base-emitter junction) and a PTAT voltage obtained from the ΔV_{EB}. These can either be implemented as a current or voltage mode as shown in Figure 1.10 or a voltage mode whose CMOS implementation is shown in Figure 2.2

From the Figure 2.2 the, we have

$$V_{REF} = V_{EB2} + V_{R_1} \tag{2.7}$$

Also, assuming the op-amp has large gain and that its input terminals (V_A and V_B) are at the same voltage, then

$$V_{R_{PTAT}} = V_{EB2} - V_{EB1} = \Delta V_{EB} \tag{2.8}$$

Considering (1.15),

$$I = \frac{V_{R_{PTAT}}}{R_{PTAT}} = \frac{\Delta V_{EB}}{R_{PTAT}} = \frac{V_T \ln(n)}{R_{PTAT}} \tag{2.9}$$

This makes,

$$V_{R_1} = IR_1 = \frac{R_1}{R_{PTAT}} V_T \ln(n) \tag{2.10}$$

Clearly, V_{R_1} is PTAT voltage and when added the V_{EB2}, as in (2.7) we will obtain a first order temperature reference given by:

$$V_{REF} = V_{EB2} + \frac{R_1}{R_{PTAT}} V_T \ln(n) \tag{2.11}$$

A zero TC (ZTC) can be obtained at a particular temperature by differentiating (2.11) and equating to zero.

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{EB2}}{\partial T} + \frac{R_1}{R_{PTAT}} \left(\frac{k}{T}\right) \ln(n) \tag{2.12}$$

Note that a room temperature $\frac{k}{T} \approx 0.086\, mV/°C$ and $\frac{\partial V_{EB2}}{\partial T} \approx -2.2 mV/°C$. Hence for ZTC at room temperature

$$\frac{R_1}{R_{PTAT}} \ln(n) = 25.58 \tag{2.13}$$

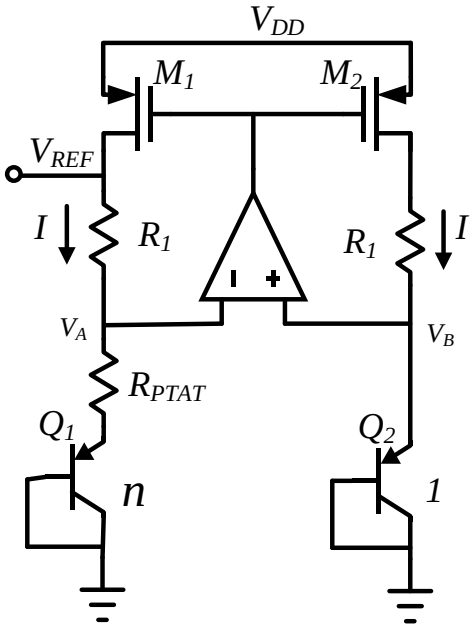


Figure 2.3: A CMOS Bandgap Reference (*The Brokaw Cell*)

Using the (1.15) and (2.4) it can be shown that for ZTC at $T = T_0$, the output V_{REF} is:

$$V_{REF}|_{T_0} = V_{G0} + [\eta - 1]V_T|_{T_0} \quad (2.14)$$

For the case of $T_0 = 300\ K$ and $\eta = 2.3$ implies,

$$V_{REF}|_{T_0} = 1.24\ V \quad (2.15)$$

The name bandgap originates from the fact that output is dependent of the bandgap voltage (V_{G0}) of silicon as seen in (2.14). The voltage reference circuit in Figure 2.3 is a CMOS implementation of the voltage reference originally proposed by Brokaw, A.P. in 1974. Due to the 1.24 V voltage output for ZTC this reference requires a supply above 1 V to function, hence other techniques have been proposed over the years for sub-1 V designs. An example of such circuits is described in the next section.

2.5 Design of Sub-1 V CMOS Bandgap Reference

This section presents a bandgap reference that is implemented in the *IBM180 CMOS7RF* process. The circuit is a current-mode BGR which uses a non-linear curvature compensation to achieve a 9 ppm TC at a supply of 1.1 V. For modern SOC application, it is necessary for embedded VRs to have high power -supply rejection (PSR) over wide frequency bandwidth in order to reject noise from the high speed on-chip digital circuits [26]. Hence, PSR enhancement techniques are used to achieve a PSR of -67dB at 100Hz and -42.7dB at 10MHz. The bandgap dissipates 14µA current at room temperature.

2.5.1 Circuit Overview

The bandgap Reference (BGR) is shown in Figure 2.3. The bandgap is composed of three main blocks: the op-amp, bandgap core and PSR enhancement circuit. The Self

Cascode (SC) current mirror is used to ensure high output impedance and also allow for low voltage operation.

2.5.2 Curvature Compensation

The overall concept of the BGR temperature compensation is illustrated in Figure 2.2a. The curvature compensation is based on a non-linear temperature discussed in section 1.3.2. The first step is to generate a PTAT current KV_T and use it to compensate the linear term of a V_{EB}-based current, I_{EB}. After the first-order correction, a non-linear current is added to $FV_T \ln\left(\frac{T}{T_0}\right)$ to compensate for the logarithm temperature terms of the V_{EB}-based current.

The circuit implementation of the non-linear compensation is shown in Figure 2.2b. Assuming the voltages at node A and B are equal, and using equation (1.14) - (1.16),

$$I_{PTAT} = \frac{V_{EB2} - V_{EB1}}{R_{PTAT}} = \frac{V_T}{R_{PTAT}} \ln(n) \tag{2.16}$$

and current I_{CTAT} is given by:

$$I_{CTAT} = \frac{V_{EB2}}{R_{CTAT}} \tag{2.17}$$

Since the currents through Q_1 and Q_2 is PTAT, applying (2.4),

$$V_{EB2} = V_{G0} - \frac{T}{T_0}[V_{G0} - V_{BE2}(T_0)] - [\eta - 1]V_T \ln\left(\frac{T}{T_0}\right) \tag{2.18}$$

Also the current through Q_3 is constant making:

$$V_{EB3} = V_{G0} - \frac{T}{T_0}[V_{G0} - V_{BE3}(T_0)] - [\eta]V_T \ln\left(\frac{T}{T_0}\right) \tag{2.19}$$

Hence,

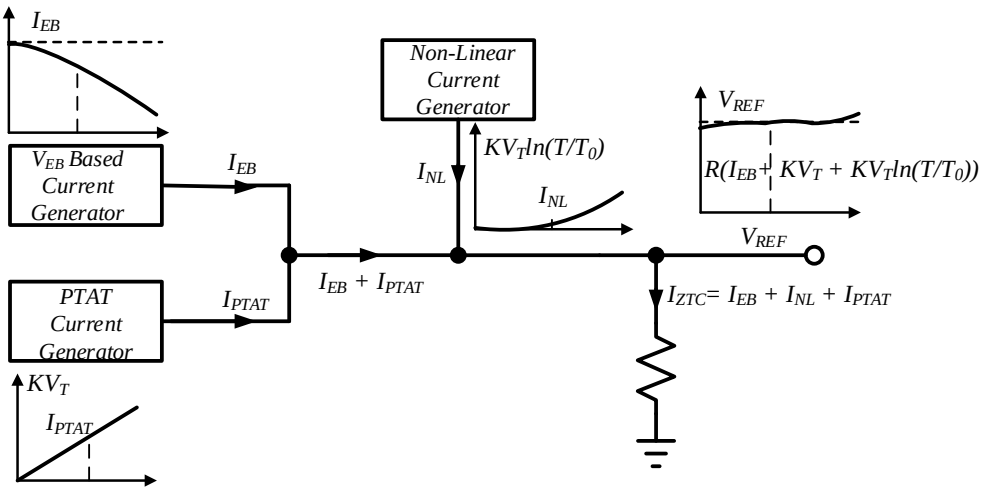
$$I_{NL} = \frac{V_{EB2} - V_{EB3}}{R_{NL}} = \frac{V_T}{R_{NL}} \ln\left(\frac{T}{T_0}\right) \tag{2.20}$$

This gives an output voltage:

$$V_{REF} = R_0[\frac{V_{EB2}}{R_{CTAT}} + \frac{V_T}{R_{PTAT}} \ln(n) + \frac{V_T}{R_{NL}} \ln\left(\frac{T}{T_0}\right)] \tag{2.21}$$

This allows for a compensated reference voltage other than 1.2V to be achieved.

a)



b)

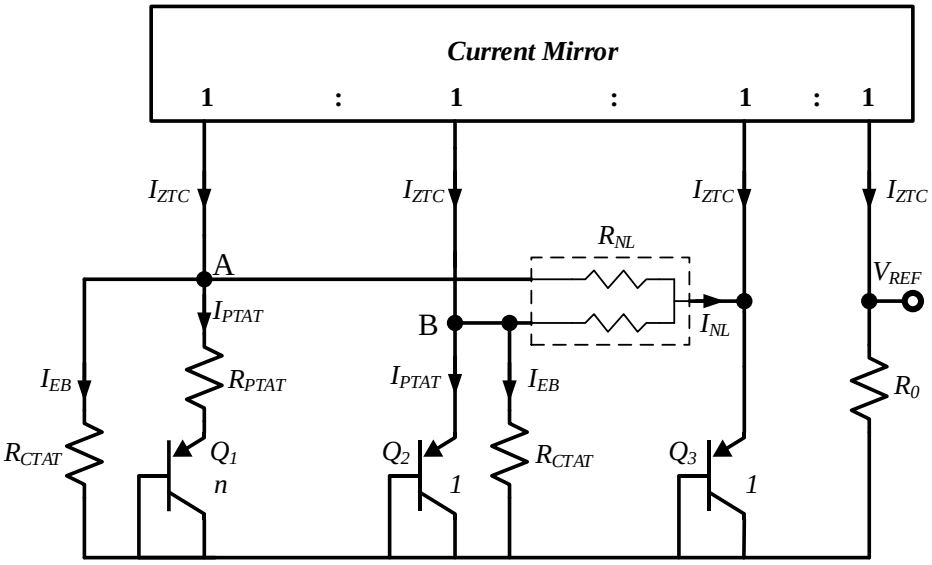


Figure 2.4 BGR Curvature Compensation a) Concept b) Implementation

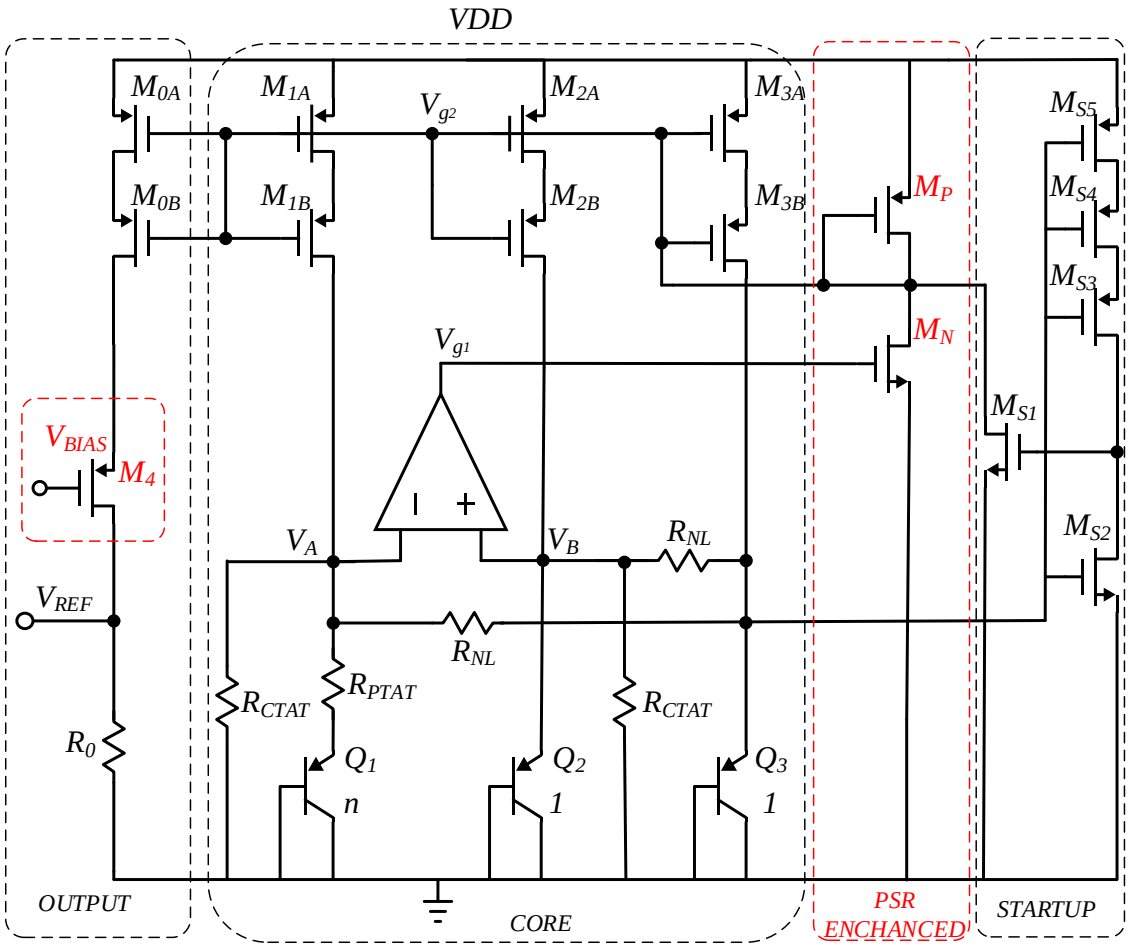


Figure 2.5: The Proposed Bandgap Reference (BGR)

2.5.3 PSR Improvement

The method used here is to add a voltage-adder (implemented with M_P and M_N) as shown in the Figure 2.4. This circuit feeds the supply noise directly into the feedback loop, hence modulating the V_{g2} of M_1, M_2 and M_0 current mirror with respect to their source terminal voltages. Since the drain current, I_D, varies with V_{GS}, the current becomes less sensitive to the supply noise.

The supply rejection of the circuit (with the adder) can be shown to be:

$$\frac{v_{REF}}{v_{dd}} = g_{o_0}R_0 + \frac{R_0}{1+g_{m_0}R_0}\frac{1}{R_{eq}}\left[\frac{g_{mN}-g_{mP}}{g_{mN}}\frac{1}{A}+\frac{1}{A_{dd}} + \frac{g_{oN}-g_{oP}}{g_{mN}}\frac{1}{A}\frac{g_{o1,2}}{g_{m1,2}}\right] \tag{2.22}$$

since $g_{o0} \ll \frac{1}{R_0}$, and $g_{m0}R_0 \gg 1$

$$PSR = \frac{v_{REF}}{V_{dd}} \approx \frac{1}{g_{m0}R_{eq}A_{dd}} \tag{2.23}$$

where $R_{eq} = R_{CTAT}//(\frac{1}{gmQ_1} + R_{PTAT}) - R_{CTAT}//(\frac{1}{g_{mQ_2}})$, where A and A_{dd} are the op-amp differential gain and PSR respectively.

To improve the supply rejection, self cascode devices are used to achieve low go_0 (high intrinsic output impedance).From (2.23) a high PSR can be achieved by using an op-amp with high PSR.

The adder circuit is implemented by using an NMOS (MN) and PMOS (M_P) [27]. Neglecting the ripple at the output of the op-amp (since PMOS input stage op-amp is used to achieve a high PSR), the PSR at node V_{g2} mainly depends on the PSR enhancement stage. The PMOS input stage op-amp uses a PMOS tail current mirror, resulting in a large impedance from VDD to the output and hence a large PSR Op-amp.

The diode-connected MP has a low impedance of $\frac{1}{g_{mP}}$, where g_{mP} is the trans-conductance of M_P. The PSR at node V_{g2} is given by

$$v_{g1} = \frac{r_{dsN}}{\frac{1}{g_{mP}} + r_{dsN}} v_{dd} \approx v_{dd} \tag{2.24}$$

From (15), the ripple from the supply is injected at node V_{g2}, so V_{g2} follows the supply ripple, maintaining the V_{GS} of M_0, M_1, M_2 and M_3 constant.

Though the PSR is increased by the above method, the bandwidth is limited. The transistor M_4, which operates in the linear region is used to extend the bandwidth. The C_{gs} of M_4 combined with its impedance allows for the creation of a pole close to the op-amp PSR zero, hence extending the PSR bandwidth of the whole circuit. Optimal result is obtained if M_4 is biased to operate in saturation but due headroom constraints it is made to operate in triode.

This allows for high PSR at high frequencies. The self cascode structure offers high output impedance similar to a regular cascode structure whilst output voltage requirements are similar to that of a single transistor [28].

2.5.4 Op-Amp

The op-amp is the two stage OTA shown in the Figure 2.5. The PMOS input of the op-amp allows for high PSR (A_{dd}), this helps improve the overall PSR of the bandgap as evident from (2.23). Since the input of the op-amp is biased by V_{EB}, the expected input-common mode range (ICR) voltage would be approximately from 400 mV to 800 mV.

Also with a PMOS input, the minimum supply would be determined by the upper limit of the ICR (ICR^+), i.e.

$$ICR^{+} = V_{DD(min)} - V_{dsat7} - V_{GS1,2} \approx 0.8\,V \tag{2.25}$$

From (2.25), with the transistors M_1 and M_2 operating in weak inversion with $V_{GS1,2} = 200\,mV$, and $V_{dsat7} = 100\,mV$, the minimum supply, $V_{DD(min)}$, would be $1.1\,V$.

The op-amp was designed to meet the following specifications: DC Gain of 75dB, 1.6MHz GBW with phase margin of 65°, PSR of -50dB and 3µA from 1.1 V.

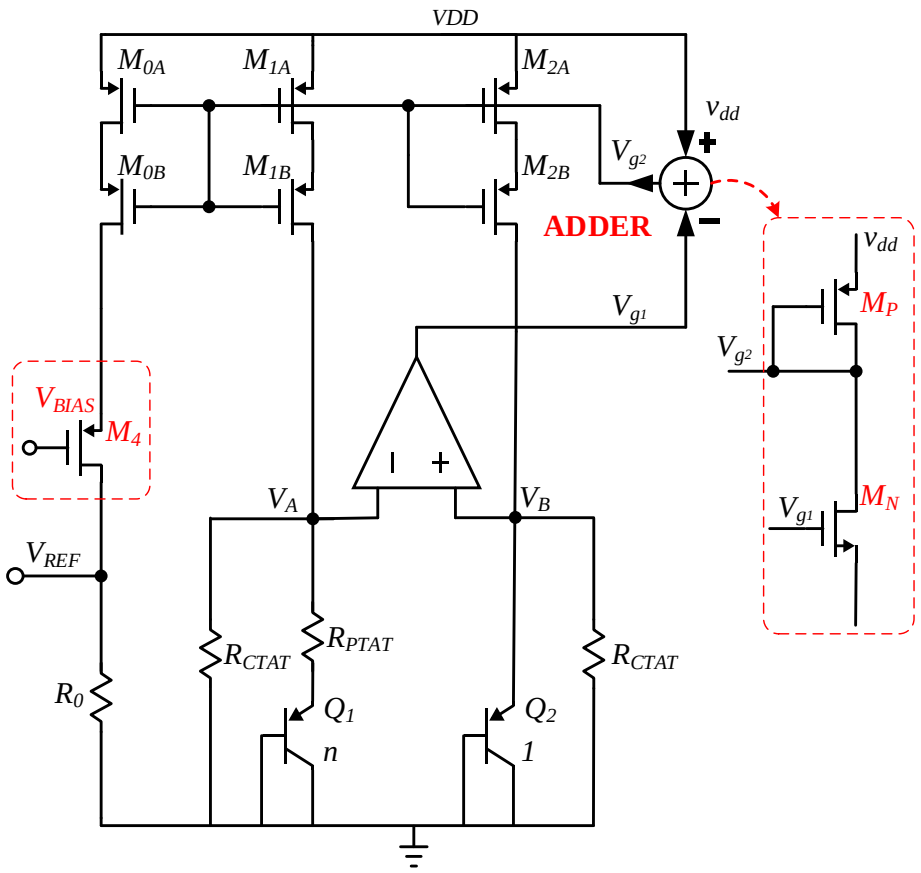


Figure 2.6: PSR Improvement Concept

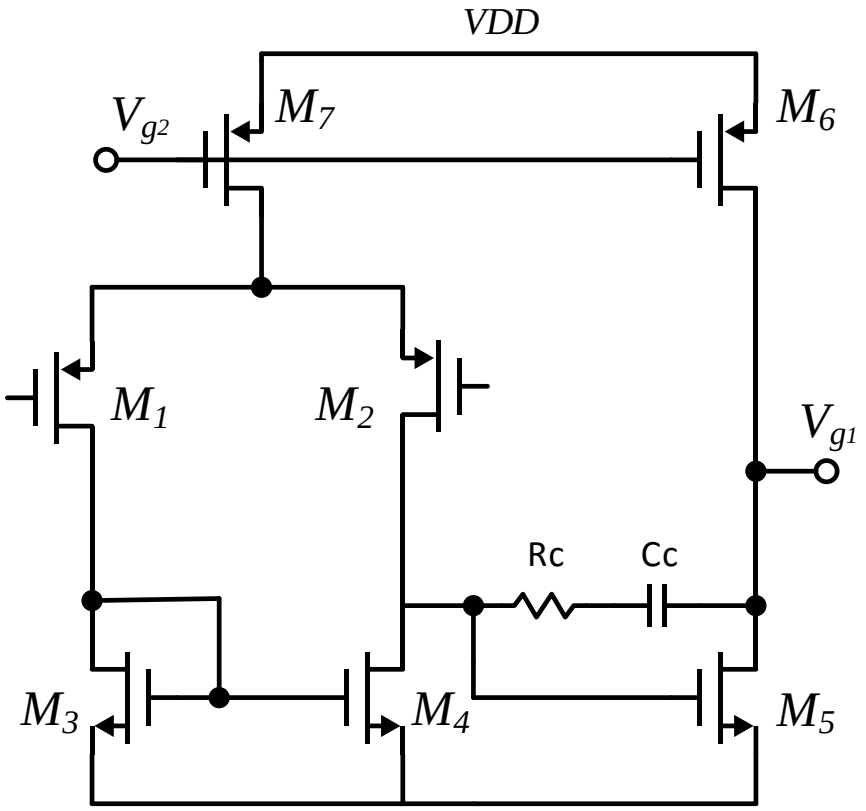


Figure 2.7: Op-Amp for BGR

2.5.5 Startup

The transistors $M_{S1} - M_{S5}$ form the startup for the circuit in Figure 2.5. There is no current drawn by the startup circuit once the BGR is on. At startup, there is no current through Q_1 , Q_2 and Q_3 making their V_{EB} zero. Hence the output of the inverter in the startup (consisting of $M_{S2} - M_{S5}$) is high, turning transistor M_{S1} on. As M_{S1} is turned on, the gate of the PMOS current mirrors in the core is lowered, hence the transistors $M_0 - M_3$ are turned on. When the desired current flows through Q_1 , Q_2 and Q_3 their V_{EB}

becomes close to 650 mV at room temperature, therefore the output of the inverter becomes low. This switches the transistor M_{S1} off.

2.5.6 Experimental Results

The proposed VR has been fully implemented in 0.18-μm CMOS technology. The measured temperature coefficient (TC) performance for temperatures ranging from -20℃ to 80℃ is shown in Figure 2.6. The TCs of the untrimmed voltage references range from 11-13 ppm for supply from 1.1 V to 2.2 V.

To measure the PSR of BGR a supply ripple of 200 mV peak is injected across the entire frequency range. An external high bandwidth amplifier is connected at the output of the BGR for the PSR measurement. The amplifier is constructed to have a gain of around 40 dB over the measured frequency to avoid hitting measurement equipment sensitivity floor. The PSR performance between 10Hz and 80MHz shown in Figure 2.9.

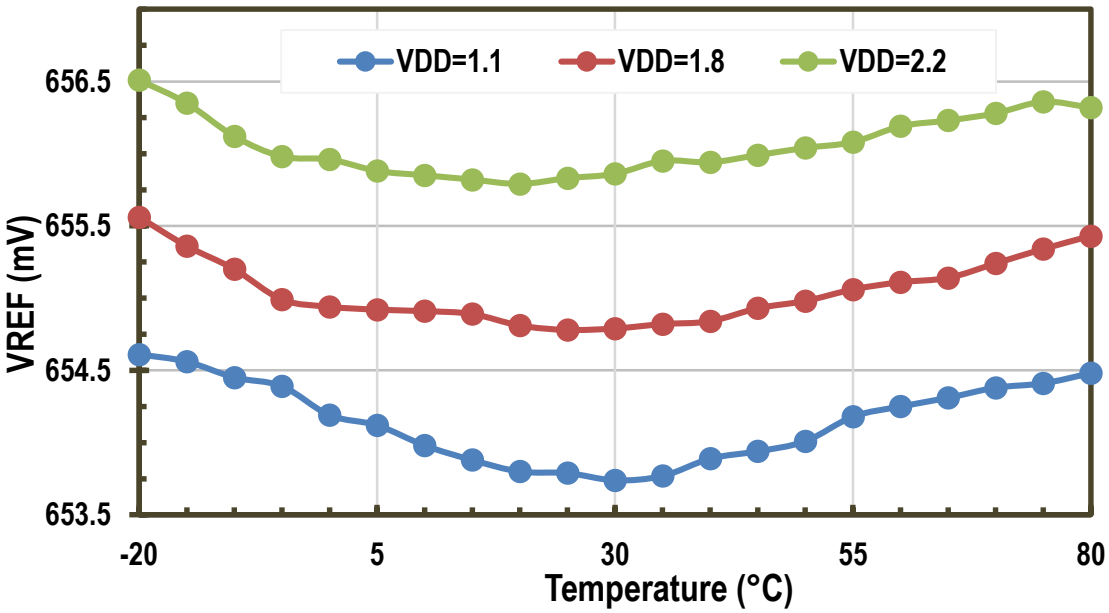


Figure 2.8: Measured Temperature Dependence of the Proposed BGR

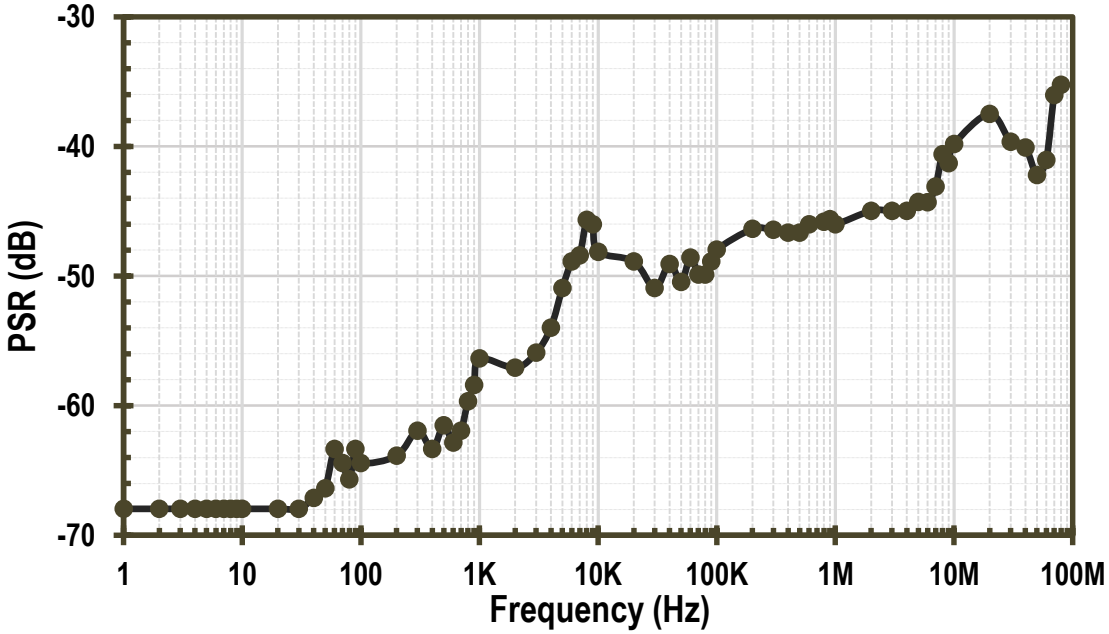


Figure 2.9: Measured PSR of Output BGR

Table 2.3: Performance Comparison of Sub-1 V BGR with Previous Works

Parameter	**This Work**	**[29]**	**[16]**	**[30]**	**[31]**	**[32]**
Technology	0.18µm	0.18µm	0.6µm	0.6µm	0.5µm	0.5µm BiCMOS
Supply Voltage (V)	1.1 to 2.2	1.1 – 1.8	2 –5	0.98 – 1.5	3.7	1 – 5
Supply Current (µA)	12	14	23	18	378	20
Vref (V)	0.655	1.012	1.142	0.603	1.121	0.190
TC(ppm/℃)	10	4	5.3	15	120	11
LR (%/V)	0.0497	N/A	0.125	0.73	N/A	0.025
PSR(dB) **@100Hz** **@10MHz**	 -67 -40	 -75 -23	 -40 -10	 -44 -17	 -43 -10	 N/A N/A
Die Area(mm^2)	0.32	N/A	0.057	0.24	0.4000	0.4000

3. AN ALL-MOSFET VOLTAGE REFERENCE WITH -50 dB PSR @ 80 MHz FOR LOW POWER SOC DESIGN

This section presents a voltage reference (VR) with PSR better than 50 dB for frequencies up to 80 MHz, which uses MOSFETs only. In addition to a compact MOSFET low-pass filter, a combination of feedback and feed-forward techniques is proposed for wide bandwidth PSR. The VR is fabricated in a standard 0.18µm CMOS process. It achieves a temperature coefficient of 19 ppm/°C from -35 °C to 80 °C. The line regulation is 0.098 %/V for a step from 1.1 V to 2.2 V supply voltage with 550 nW at room temperature and 0.0180 mm^2.

3.1 Motivation and Overview

Due to the nonlinear temperature behavior and voltage limitation of base-emitter voltages, bandgap BGRs, discussed in the previous section 2, are not suitable for high-precision applications with low power consumption [33], [34]. Furthermore, the use of resistors in BGRs makes it difficult to reduce the power consumption without a substantial increase in area [34]. The methods proposed in [34], [35] avoid the use of resistors, hence, achieve compact ultra-low power BGRs but with poor temperature stability (Temperature Coefficients (TCs) > 100ppm).

The noise injected to the output of VR circuit through the supply is the most significant noise, in comparison to other sources. Hence high PSR VR is desired to achieve better performances in both analog and digital systems, especially in radio frequency (RF) system. To meet the goals of low voltage supply and low power dissipation, it is necessary

to avoid using complex architecture and circuits. On the other hand, it is necessary to choose a structure to achieve high PSR, over a wide frequency range to reject noise coupled from high-speed digital circuit on the chip [26].

A resistor-less low-power non-bandgap voltage reference is presented in this section. In the proposed VR, a proportional to absolute temperature (PTAT) voltage is converted to a current proportional to μT^2. This current is used to extract a temperature-stable reference voltage from the V_{GS} of a diode-connected NMOS. In addition to a compact MOSFET low-pass filter (LPF), a combination of feedback and feed-forward techniques is also proposed for wide bandwidth PSR enhancement.

3.2 Architecture and Design

The basic topology of proposed VR circuit is shown in Figure 3.1. A PTAT voltage is generated using a PTAT voltage generator and converted to a current proportional to μT^2, which serves as bias current for the whole VR. Finally, a diode-connected pMOS transistor (active load) is used to generate a temperature-stable reference voltage:

$$V_{REF} = V_{TH} + \alpha V_T \tag{3.1}$$

α is determined by transistor ratios, V_{TH} (threshold voltage) serves as a complementary to absolute temperature (CTAT) voltage and αV_T is a PTAT voltage.

A 5 bit trimming is applied to the output current to cancel the effects of process variation. The PTAT voltage generator, the V-to-I converter and the feedback form a self-biased current source. The feedback in self-biased current source is used to provide feed-forward and feedback paths for power supply noise.

The feedforward and feedback paths enhance the PSR performance of the VR up to medium range frequency. The LPF is a compact MOSFET low-pass filter used to filter the supply noise at high frequencies.

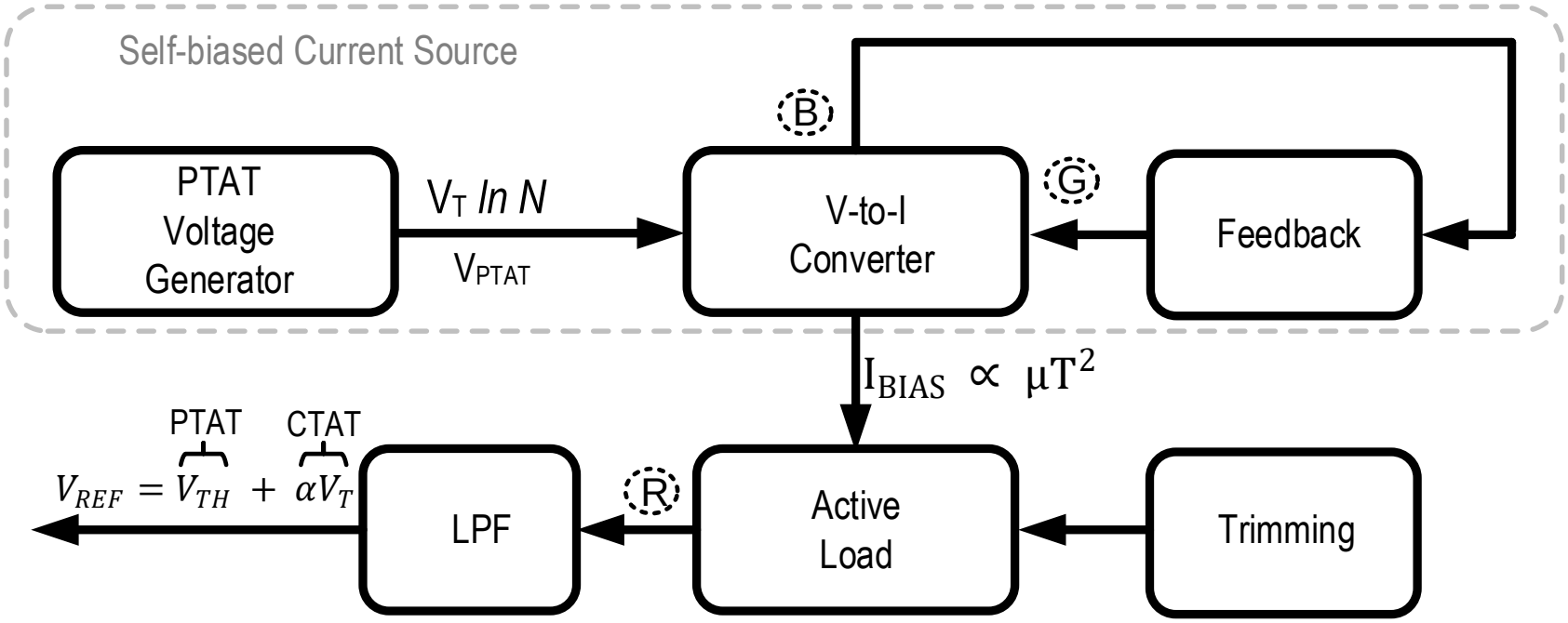


Figure 3.1: The Conceptual Bock Diagram of the Proposed VR Circuit

3.2.1 PTAT Voltage Generator

The difference between V_{GS} values of two PMOS transistors biased in sub-threshold region gives a PTAT voltage. The composite transistor, shown in Figure 3.2, is used to provide the desired PTAT voltage for the biasing of the VR. To eliminate the body effect through the source to body of each transistor, the transistors are implemented in their own wells.

The I_D of a MOSFET in weak inversion is based on the channel diffusion current and is given by the following expression

$$I_D = I_s\left(\frac{W}{L}\right)\left(1 - e^{-\frac{V_{DS}}{V_T}}\right)e^{\frac{V_{GS}-V_{TH}}{mV_T}} \tag{3.2}$$

$I_s = (m-1)\mu C_{ox}V_T^2$ is the characteristic current, m is gate-to-surface coupling coefficient (sub-threshold slope factor).

For $V_{DS} \geq 4V_T$, the effect of the V_{DS} on the current can be neglected [36]. From the Figure 3.2, using the equation (3.2), V_{PTAT} can be expressed by

$$V_{PTAT} = V_{GS1} - V_{GS2} = mV_T\ln(NK) \tag{3.3}$$

where $N = \frac{S_{MQ_2}}{S_{MQ_1}}$ and K is the ratio of the current through MQ_1 and MQ_2. Figure 3.3 shows the simulation results for the PTAT voltage of Figure 3.2 across process corners.

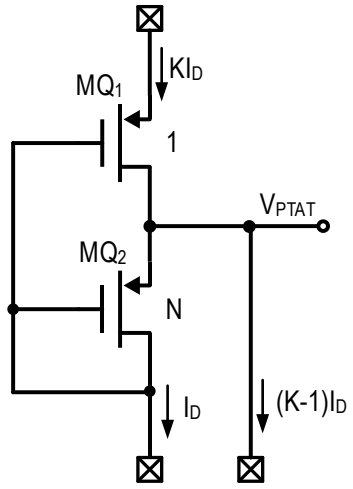


Figure 3.2: Composite Transistor PTAT Voltage Generator

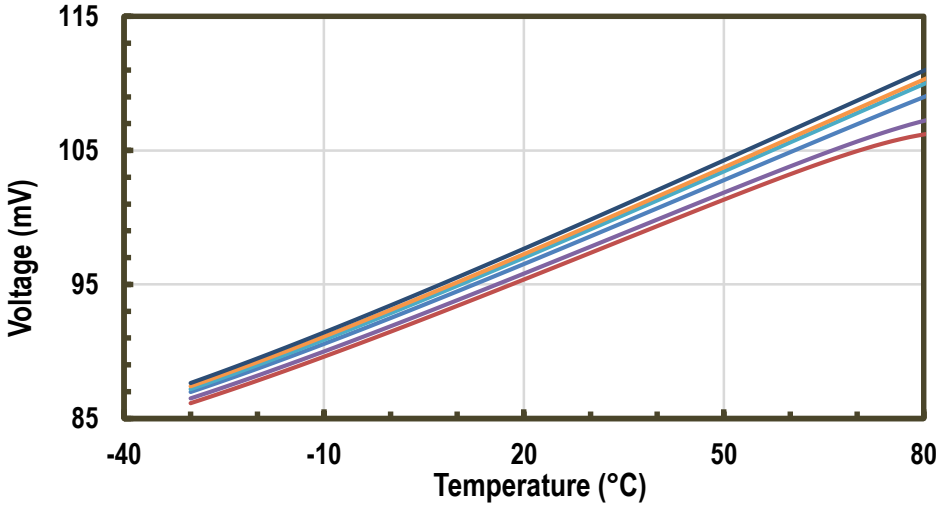


Figure 3.3: V_{PTAT} across Process Corners

3.2.2 Self-Biased Current Source

The Self-Biased Current Source serves as the core of the proposed VR and consists of an asymmetric source-input voltage–to-current converter, the PTAT voltage generator and a feedback branch. In Figure 3.4, an asymmetric source-input voltage-to-current converter is used to convert the PTAT voltage from the composite transistor into a bias current for

the VR. As discussed in the section 4.2.2, in addition to minimizing the voltage difference between A and B, the feedback is also used to realize a feedforward transfer function for power supply noise.

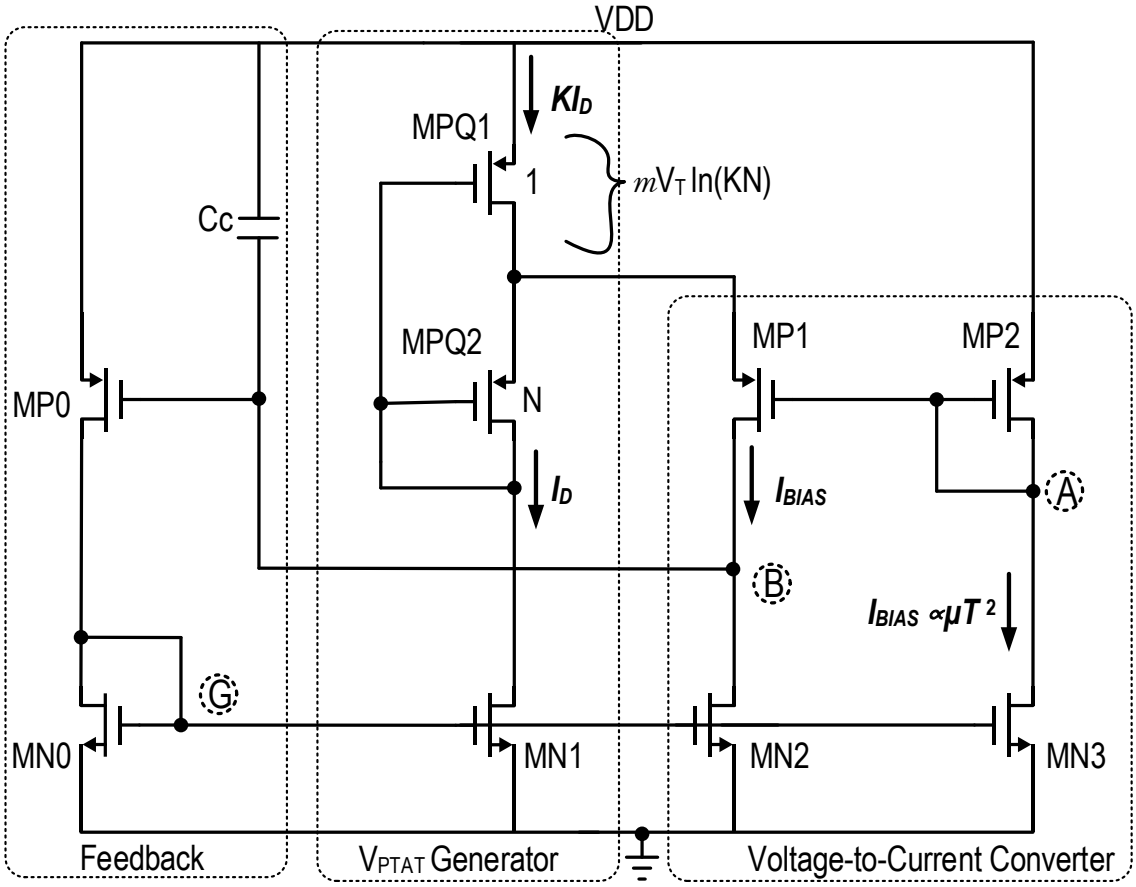


Figure 3.4: Self-Biased Current Source

From equation (3.6) and (3.7) for MP_1 and MP_2 in strong inversion;

$$V_{GS1} - V_{GS2} = V_{PTAT} = mV_T \ln KN \tag{3.4}$$

$$\sqrt{\frac{2I_{BIAS}}{k_P}}\left[\frac{1}{\sqrt{S_{MP2}}}-\frac{1}{\sqrt{S_{MP1}}}\right]=mV_T\,ln\,KN \tag{3.5}$$

$$I_{BIAS}=\frac{k_p}{2}(mV_T\,ln\,KN)^2S_{MP1}\left[\sqrt{\frac{S_{MP1}}{S_{MP2}}}-1\right]^2 \tag{3.6}$$

Where $k_p=\mu_pC_{ox}$ and μ_p is mobility of holes. The current is determined only by the aspect ratios ($S_{M_1}, S_{M_2}, S_{MP1}\ and\ S_{MP2}$) and the current ratio K.

Given equation (1.33), the TC of I_{BIAS} is given by:

$$TC_{I_{BIAS}}=\frac{1}{I_{BIAS}}\frac{\partial I_{BIAS}}{\partial T}=\frac{2+\alpha_\mu}{T} \tag{3.7}$$

The α_μ above in standard $0.18\mu m$ this makes I_{BIAS} negative TC. The simulation of the temperature dependence of I_{BIAS} is shown in Figure 3.5.

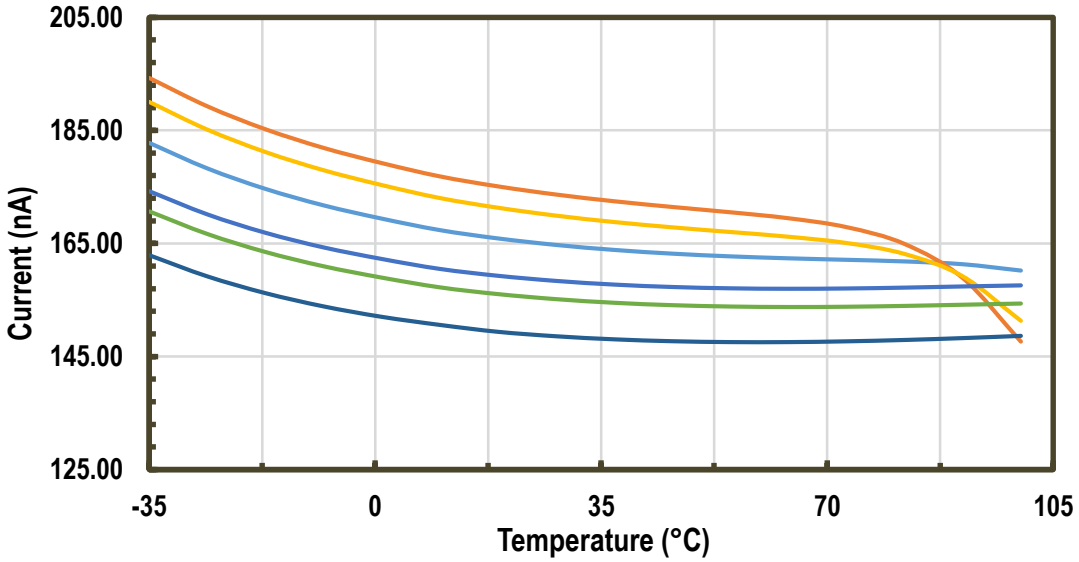


Figure 3.5: Temperature Dependence of I_{BIAS} across Process Corners

The use of the composite transistor allows for the minimum voltage requirement of the self-biased current source to scale with technology, unlike the solutions in [2, 3, and 5] which use BJTs.

Since the self-biased current source has two stable states corresponding to the current given by (3.6), and zero, a startup circuit (formed by M_{S1}-M_{S3} as shown in Figure 3.6) is used to ensure that the former state is achieved. A detail explanation of this startup circuit is done in section 4.2.4.

3.2.3 Loop Compensation

The usual constant-gm bias circuit has only one feedback loop, but the addition of $MN0$ and $MP0$ adds a feedback path (in Figure 3.6) that controls the gate voltage of $MN2$ without requiring the diode connection of $MN2$. A compensation capacitor (C_C) is placed at the high impedance node. This creates a dominant pole formed by C_C and $r_{dsMP1}//r_{dsMN2}$. The C_C can be connected between node B and node G instead of between B and VDD (or GND); this connection would benefit from the advantage of the Miller effect introduced by the voltage gain from node B to node G.

3.2.4 Reference Generator

Consider the active load of the proposed VR, shown in Figure 3.6. Assuming that all transistors of the active load ($MP5$ and $MP6$) work in the strong inversion, the output reference voltage is given by:

$$V_{REF} = V_{GSMP6} = V_{THMP6} + \sqrt{\frac{2MI_{BIAS}}{k_p S_{MP6}}} \tag{3.8}$$

From (3.8), it is apparent that the temperature dependence of the V_{REF} consists of two terms. One of the terms is due to the temperature dependence of V_{TH} and the other is due the temperature dependence of the I_{BIAS} and of mobility (μ_p).

As is seen from (3.6), I_{BIAS}, which is proportional to K_p ($\mu_p C_{ox}$), would completely suppresses the effect of the temperature dependence of mobility (μ_p) on V_{REF}. Using (3.6) and (3.8), we can write the expression for the output voltage V_{REF} as:

$$V_{REF} = V_{THMP6} + \alpha V_T \tag{3.9}$$

$$\alpha = mln\,KN \sqrt{M \frac{S_{MP1}}{S_{MP6}}} \left[\sqrt{\frac{S_{MP1}}{S_{MP2}}} - 1 \right]^{-1} \tag{3.10}$$

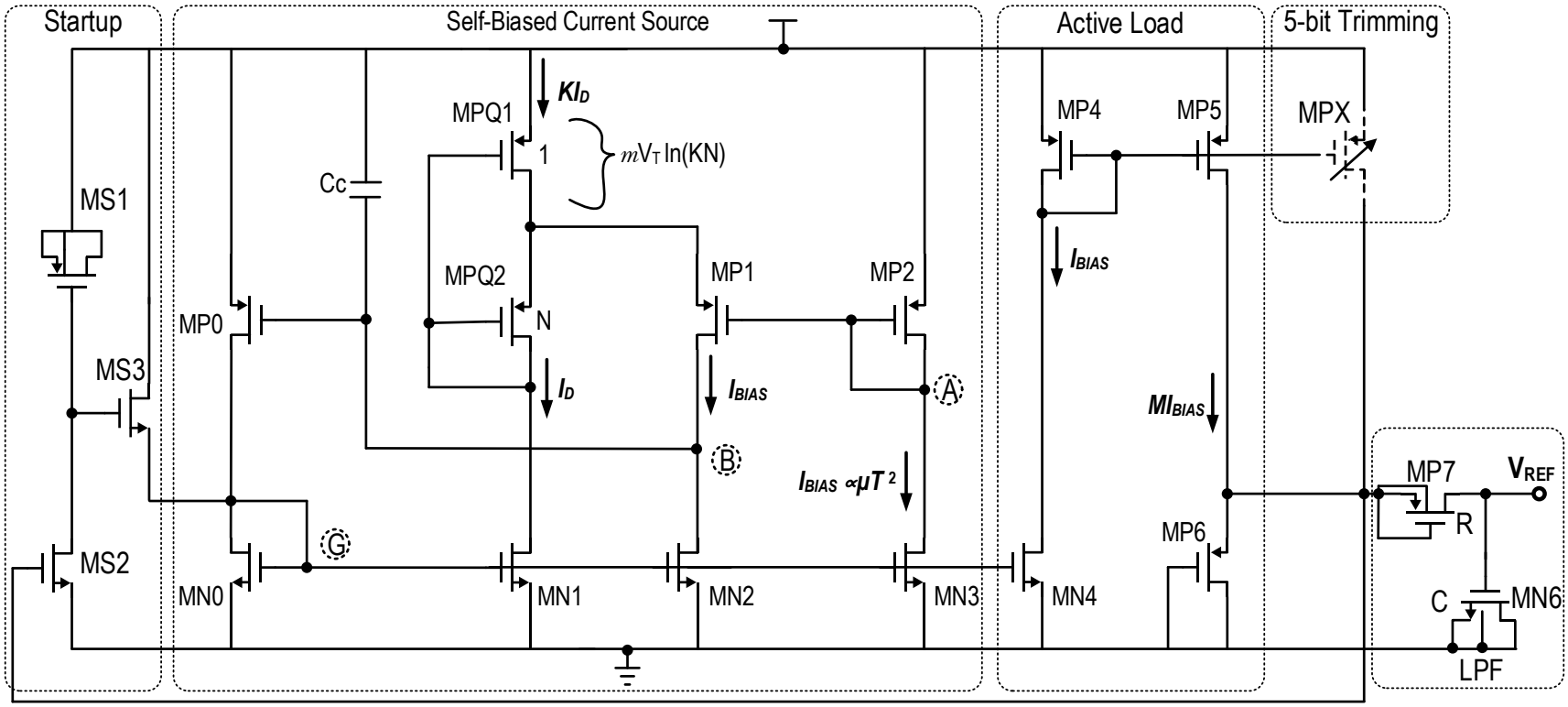


Figure 3.6: Proposed VR Circuit

3.2.5 PSR Improvement

The PSR of the VR can obtained by using similar analysis in section 4.2.4 and noting that the gain from node G to gate of $MP5$ is given by:

$$\frac{g_{mMN4}}{g_{mMP4}} \approx 1 \tag{3.11}$$

This gives PSR performance similar the expressions obtained in section 4.2.4. Here also, a compact MOSFET LPF with an equivalent 3dB bandwidth of 200Hz is used in the output to filter the noise without any extra power consumption.

3.2.6 Trimming Circuit

Since V_{TH} varies with process corners, output voltage (V_{REF}), which depends on V_{TH} as seen in (3.10), will also change from one process corner to the other even if accurate matching of the transistor ratios is attained. To compensate for these changes, the bias current of the active load MP3 is changed accordingly. To implement these variations the 5-bit current mirror shown Figure 3.7 is used. These allows for the bias current to be changed in binary multiples. Note the I_X is a mirror copy of I_{BIAS}.

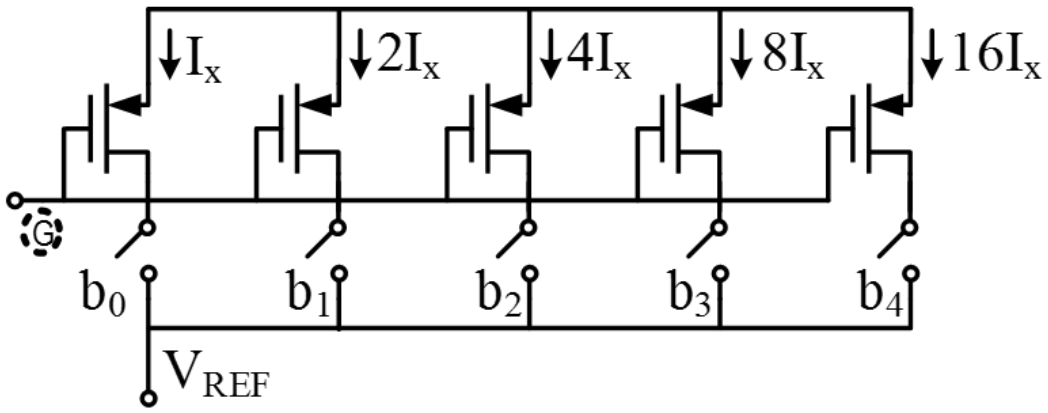


Figure 3.7: Trimming Circuit

3.3 Design Considerations

The main design considerations for the proposed VR are channel length modulation, process variation and the dynamic range. These consideration would be discussed in detailed in this section.

3.3.1 Channel Length Modulation

For proper device matching, minimum width and length should not be chosen for the devices used to define gains. Moreover, in order to substantially reduce the channel length modulation, long channel lengths are used for all transistors in the current mirrors, the feedback transistor MN0 and the active load pMOS MP6. Noise through the supply feeds through to the various nodes of the sub-circuits including the output node via the parasitic capacitances of the transistors. Hence, there is a need to keep the transistors small to minimize these parasitics at critical nodes.

The drain-source voltage of $MPQ1\ and\ MPQ2$, which operates in the subthreshold region, must be larger than $4V_T$ so that the V_{DS} dependence of the current in (3.2) becomes negligible. To achieve this at all temperatures $KN \geq 22$. In this design I used $K = 4$ and $N = 8$.

3.3.2 Process Variation

Neglecting the mismatch of the W/L ratios in (3.9), the sensitivity of the reference voltage is mainly due to the accuracy of threshold voltage of the diode-connected pMOS transistor MP6. To achieve a low sensitivity to process, the variation of the threshold voltage of the MP6 has to be minimized.

The Gaussian distribution of threshold depends on process variation and mismatch. The mismatch variation magnitude, dominated by random dopant fluctuations, is generally observed to be inversely proportional to$\sqrt{WL}$ [37]. Hence, such variations can be reduced by setting the channel length and width of MP6 large enough, until mismatch is negligible compared to the effect of process variations.

Process variations affect adjacent transistors similarly, and are due to intra-wafer, inter-wafer, or inter-batch non-uniformity of the process [11]. From simulations (shown in Figure 3.10), I observed that the variation of the reference voltage due process variations and mismatches is above 3% across temperature. I used the 5-bit trimming circuit to reduce this variation to less than 1%. The trimming process involves a single step trimming. I adjusted the output bias current to achieve designate reference value while also minimizing the temperature dependence.

3.3.3 Dynamic Range

The active load dictates the minimum supply voltage for the VR. We have to ensure that transistors MP6 and MP5 operate in strong inversion. Hence, the condition below has to be satisfied:

$$V_{DD} > V_{REF} + V_{dsatMP5} \tag{3.12}$$

To ensure that the all the transistors of pMOS current mirrors (MP0-MP3) are in strong inversion, a minimum supply 1.2 V is therefore required in the *IBM 0.18µm* CMOS process. The maximum supply is imposed by the maximum drain-source Voltage (V_{DSmax}) allowed for MOS transistors, as expressed below:

$$V_{DD} < V_{GS} + V_{DS}(max) \tag{3.13}$$

In *IBM 0.18µm* CMOS process, V_{DSmax} is 1.8 V, hence the maximum supply 2.2 V.

3.4 Temperature Compensation

By differentiating (3.9) with respect to temperature and taking into account equation (4.16) and (1.8) we obtain

$$\frac{\partial V_{REF}}{\partial T} = -\alpha_{V_{TH}} + m\frac{k}{q} ln\, KN \sqrt{M\frac{S_{MP1}}{S_{MP6}}}\left[\sqrt{\frac{S_{MP1}}{S_{MP2}}} - 1\right]^{-1} \tag{3.14}$$

The first-order temperature coefficient of the threshold voltage ($\alpha_{V_{TH}}$) of a large pMOS transistors in the *IBM 0.18µm* CMOS process is 0.990 mV/℃. It is evident from (3.15),

the temperature coefficient is independent of the temperature dependence of the carrier mobility. The perfect suppression of the temperature dependence of the mobility is achieved; this leads to a smaller temperature coefficient over a wide temperature range (-30 ℃ to 110℃) compared to [5].

The zero temperature coefficient (ZTC) is achieved by setting the equation (3.15) to zero:

$$\sqrt{M\frac{S_{MP1}}{S_{MP6}}} = \frac{\alpha_{V_{TH}}\left[\sqrt{\frac{S_{MP1}}{S_{MP2}}} - 1\right]}{m\frac{k}{q}\ln KN} \tag{3.15}$$

It is clear that (3.16) is true within some approximations and the simplified transistor characteristics. This first-order condition for a ZTC has been calculated by neglecting any non-ideal effect. Henceforth, if (3.16) is satisfied, (3.9) can be written as

$$V_{REF} = V_{TH0} + \alpha_{V_{TH}} T_0 \tag{3.16}$$

3.5 Design of the Proposed Voltage Reference

As way of designing the proposed reference in Figure 3.6, the following steps can be useful.

i. Start by stetting the PTAT voltage (V_{DS} of $MPQ1$) at 100 mV room temperature. This ensures that V_{DSMPQ1} is above $4V_T$ over whole temperature range.

ii. Pick an I_{BIAS} at room temperature, $\frac{S_{MP1}}{S_{MP2}}$, and use (3.6) to calculate S_{MP1} and S_{MP2}. For example, I used $I_{BIAS} = 100\text{nA}$ and $\frac{S_{MP1}}{S_{MP2}} = 4$. Note relatively large channel lengths should be use (at least above 3µm for 0.18µm process).

iii. Use (3.3) to determine the ratio of N and K. Note m can be extracted for a particular temperature. In my design the m at room temperature is 1.3.

iv. Using the bias current and (3.2), the S_{MPQ1} and S_{MPQ2} is determined. Since these transistors operates in subthreshold use lengths above 4µm to ensure proper ratio matching.

v. To minimize the consumption, the current through $MP0$ is half of I_{BIAS}. These current should not be reduce below a quarter of I_{BIAS}, doing that will create stability problems.

vi. Since the currents through the current mirror transistors $MN0 - MN4$ are known their sizes can be determined.

vii. A simulation should be performed to determine $\alpha_{V_{TH}}$. As shown Figure 1.3b the $\alpha_{V_{TH}}$ varies with length for short channel devices and fixed for long channel devices.

viii. Using the value of $\alpha_{V_{TH}}$ determined above and (3.16) the size of the output transistor ($MP6$) is calculated. The length of $MP6$ should be large enough to ensure that $\alpha_{V_{TH}}$ is constant with changes in length. From Figure 1.3b the channel length should be at least above 2µm for the process I used.

Note: the procedure describe above is not a straight forward process, simulation should carried out to determine the best sizes that allows for optimal temperature performance.

3.6 Simulation Results

The proposed VR circuit was simulated over the temperature range -20 °C to 100 °C using a power supply voltage from 1.1 V-2.2 V. Figure 3.8 shows the simulation results for the V_{REF} across the temperature range. The change in the output voltage, obtained in simulation, 3.1 mV for the supply voltages from 1.1 V to 2.2 V over the temperature range. This corresponds to TC of 29 ppm. The results of simulation verify that the circuit operates according to the analysis given above and a temperature-stable voltage can be obtained.

Figure 3.9 shows the 1000 Monte-Carlo runs for mismatches and process variation of the untrimmed reference for temperature range of -20 °C to 100 °C. Figure 3.10 shows the variation of the trimmed and untrimmed reference voltage at room temperature for 1000 Monte- Carlo samples.

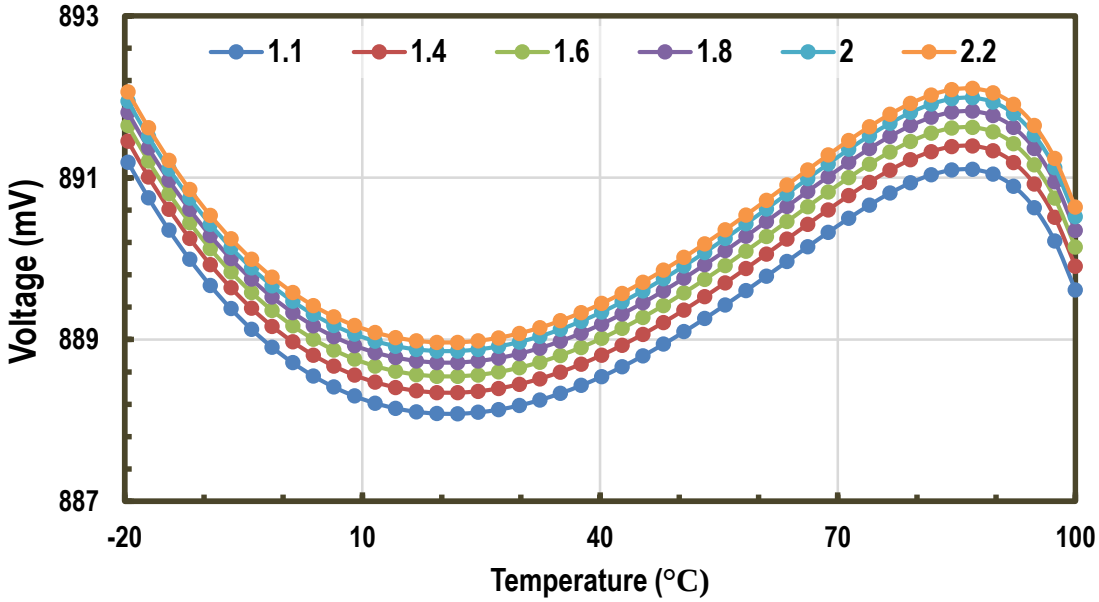


Figure 3.8: Simulation of V_{REF} for Various Supply Voltages

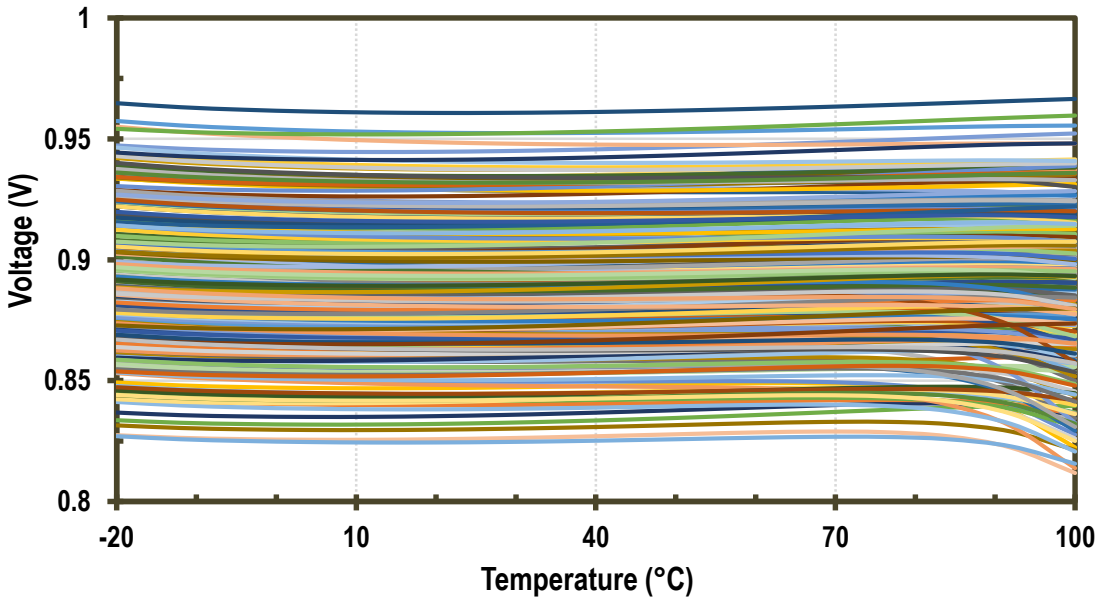
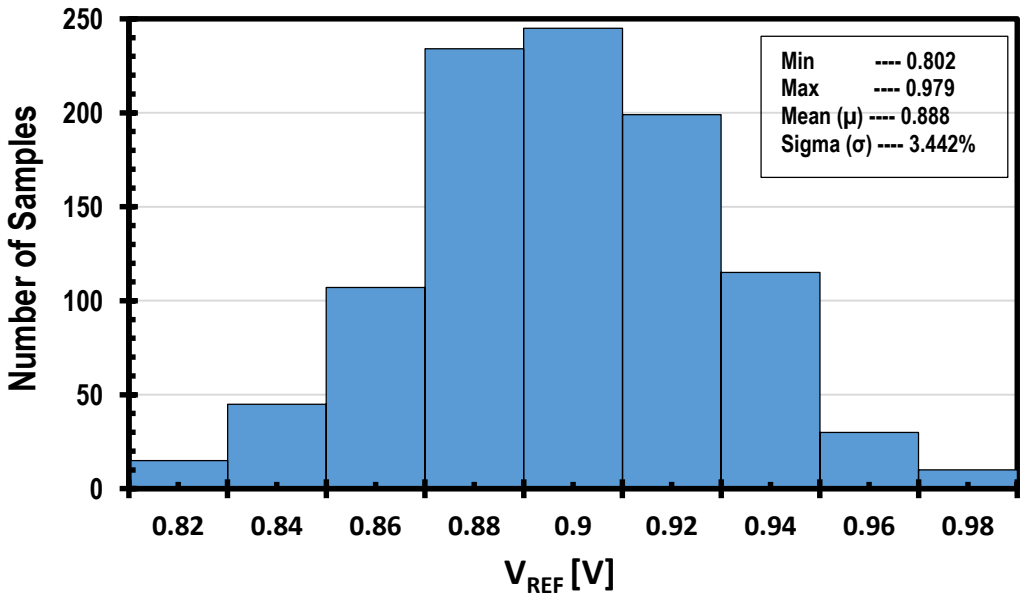


Figure 3.9: Monte Carlo Simulation for Untrimmed Reference for -20 °C to 100 °C

a)



b)

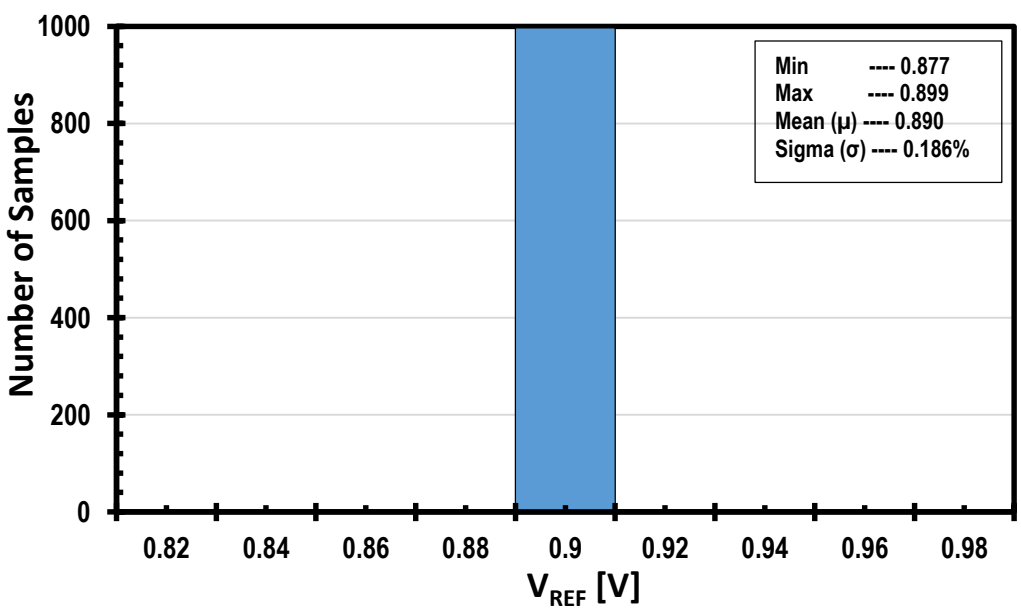


Figure 3.10: Monte Carlo Simulation @27 °C a) Untrimmed b) Trimmed

To verify the performance of the start-up circuit, I replaced the power supply by a step voltage and performed a transient simulation. The waveforms are shown in Figure 3.11. Figure 3.12a shows the variation of the accuracy of the reference with changing size of the PMOS diode MP6 for various power levels. There is a minimal change in the accuracy with changing size of the MP6. The power levels and the corresponding area of the MP6 to achieved an accuracy of 3.15% and a TC of 19 ppm is shown in Figure 3.12b.

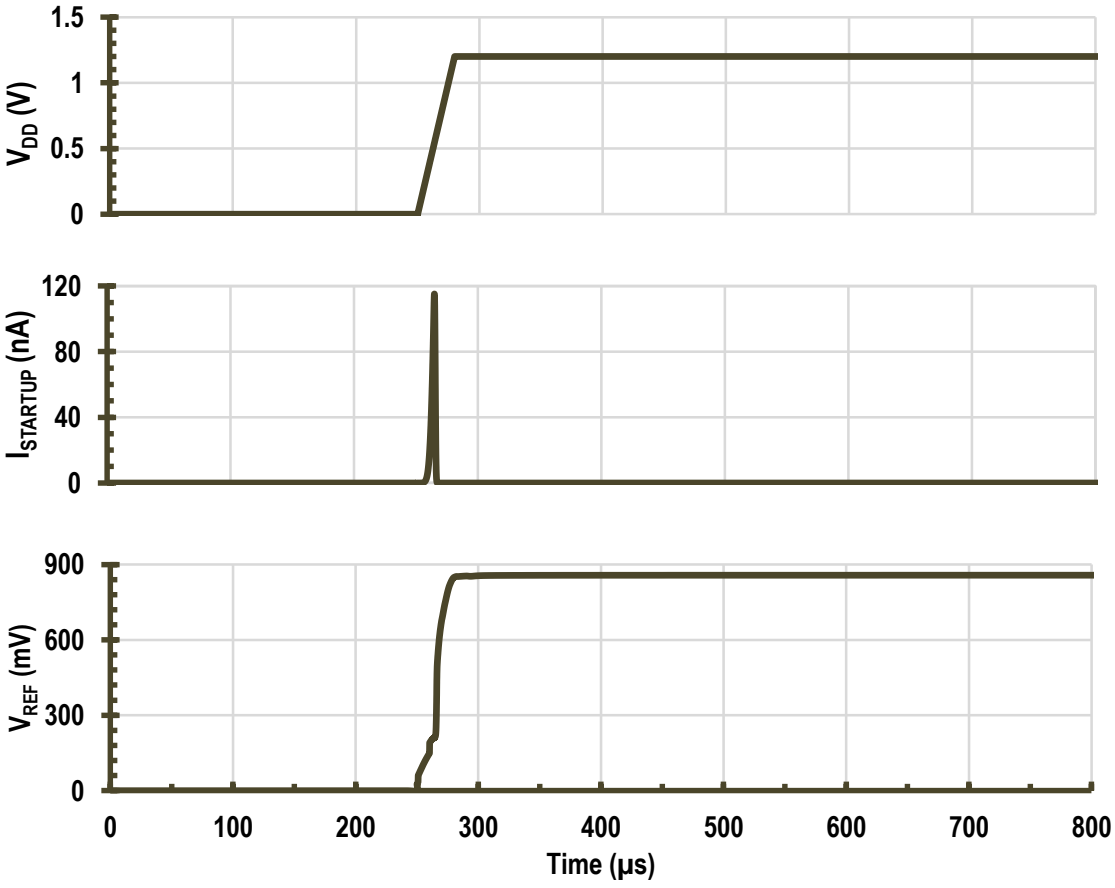
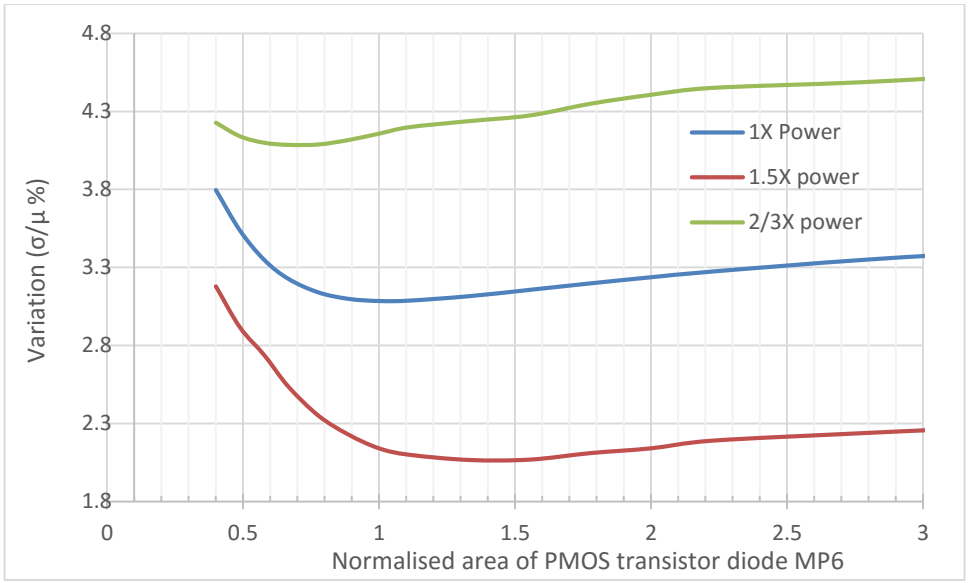


Figure 3.11: Startup Simulation

a)



b)

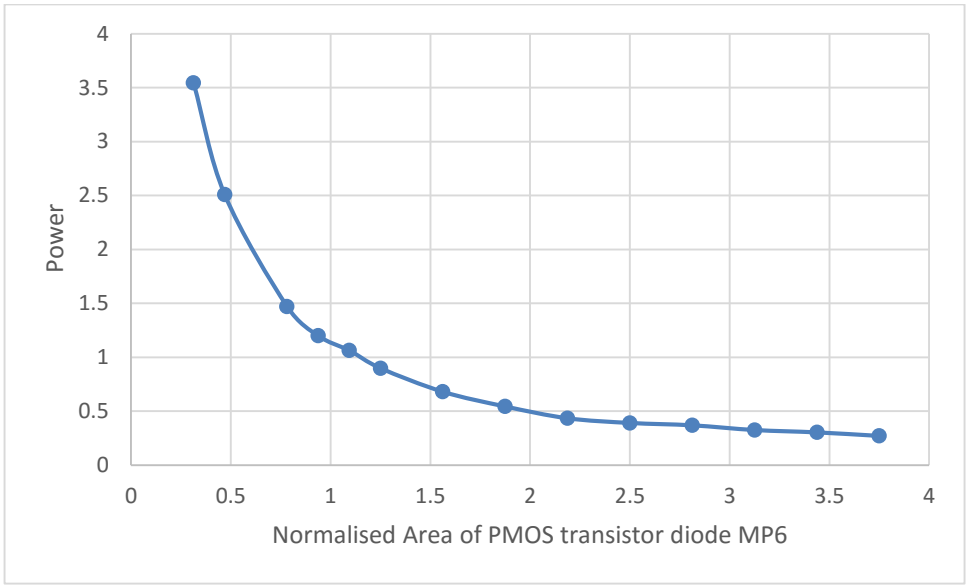


Figure 3.12: a) Accuracy of Reference Voltage vs. Area at Different Power Levels and b) the area of MP6 and Corresponding Power for 3.15% Accuracy and 19 ppm.

The PSR performance between 1Hz and 800MHz is shown in Figure 3.12, where the PSR with and without the compact MOSFET LPF are compared. The PSR without compact MOSFET LPF is more than 15dB at 10MHz due to the feedback and feedforward paths, while the PSR with compact MOSFET LPF is more than 50dB for frequencies up to 60MHz. This shows that the techniques used in the proposed VR can immensely improve PSR over a very wide bandwidth with minimum area overhead.

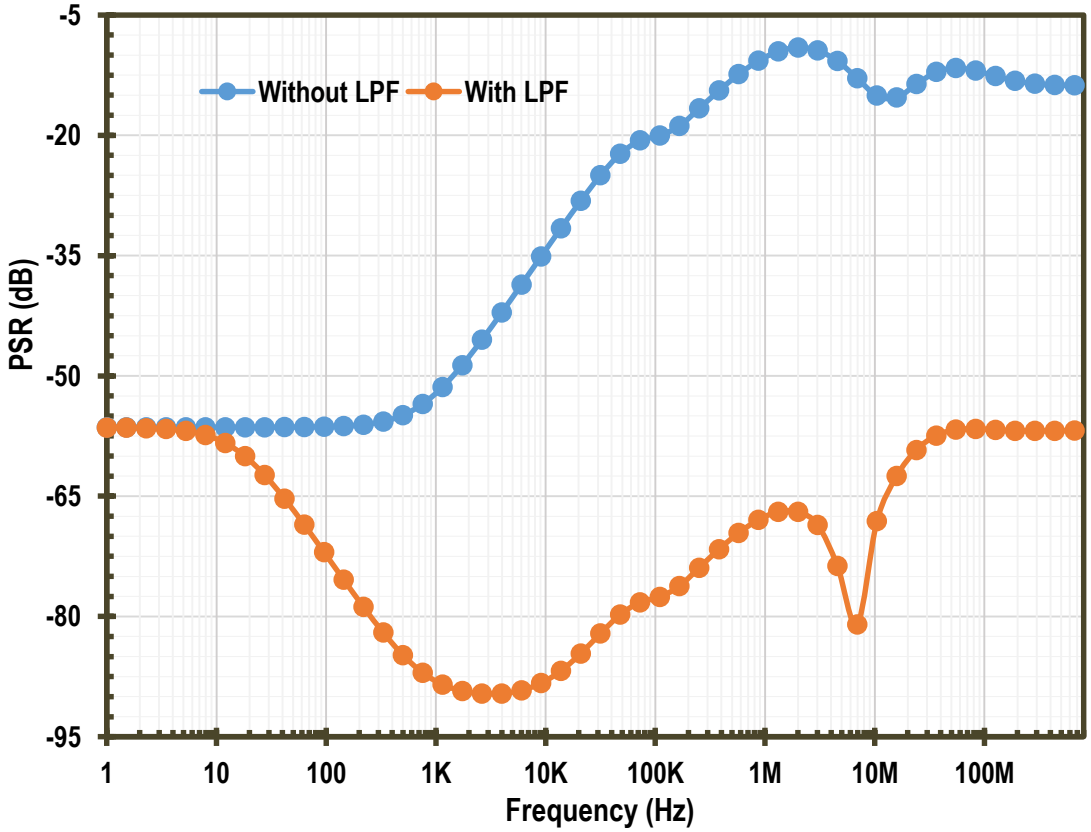


Figure 3.13: Simulated PSR of Output VR

4. AN ALL-MOSFET SUB-1 V VOLTAGE REFERENCE WITH A -51 dB PSR UP TO 60 MHz DESIGN

Though the circuit in section 3 achieves a high PSR over wide bandwidth, it has high current consumption and requires a supply voltage of 1.2 V to operate which makes it less ideal for low power, low voltage applications. The output is also depend on m leading to low thermal stability. This section introduces a reference which independent of m.

This section presents a voltage reference (VR) with PSR better than 50 dB for frequencies up to 60 MHz, which uses MOSFETs in strong inversion. In addition to a compact MOSFET low-pass filter, a combination of feedback and feed-forward techniques is proposed for wide bandwidth PSR. The VR is fabricated in a standard 0.18µm CMOS process. It achieves a temperature coefficient of 9.33 ppm/°C from -30 °C to 110 °C. The line regulation is 0.076 %/V for a step from 0.8 V to 2 V supply voltage with 360 nW at room temperature and 0.0143 mm^2.

4.1 Motivation and Overview

Voltage references (VRs), especially those with low temperature and power supply sensitivity, are essential components of many electronic systems. Due to the development of power-aware applications, low power consumption has been a design criterion of paramount importance for VR applications. With the integration of various functional modules such as radio frequency (RF) circuits, power management, and high frequency digital and analog circuits into one system on chip (SoC) in recent applications, power supply noise can cause significant system performance deterioration. This makes supply

noise rejection of the embedded VR crucial in modern SoC applications.

Due to the nonlinear temperature behavior and voltage limitation of base-emitter voltages, bandgap references (BGRs), which are among the most widely used VRs, are not suitable for high-precision applications with low power consumption [33], [34]. Furthermore, the use of resistors in BGRs make it difficult to reduce power consumption without a substantial increase in area [34]. The methods proposed in [34], [35] avoid the use of resistors, hence, achieve compact ultra-low power BGRs but with poor temperature stability (temperature coefficients (TCs) > 100ppm). Switched-mode BGRs such as in [33], [38] have lower power consumption in comparison with conventional BGRs, but are not as compact and have inferior TCs.

Sub-threshold-based MOSFET VRs, compared to BGRs, have an inherent advantage in power consumption. However, due to the effects of the temperature dependent gate-to-surface coupling coefficient, m, poor transistor ratio matching and the inaccuracies of models, designing sub-threshold-based MOSFET VRs is usually an inexact process [39], [40], resulting in inferior performance [42], [41]. Furthermore, it is difficult to achieve compact and low noise VRs due to either lack of accurate models or low sheet resistance in digital CMOS processes.

For modern SoC applications, it is necessary for embedded VRs to have high power supply rejection (PSR) over wide frequency bandwidth in order to reject noise from the high speed on-chip digital circuits [26]. Conventional techniques, such as using long channel lengths, cascode structures and pre-regulations, are usually adopted in VRs to improve (PSR). However, such techniques can only improve the low frequency

performance at the expense of headroom, area, and power dissipation.

A resistorless low-power non-bandgap voltage reference is presented in this section. All the MOSFETs in the core are standard CMOS transistors biased in strong inversion. By using strong inversion, we used some extra power compared with the weak inversion designs in [26, 27, and 28]. But, we achieved a more accurate reference since using strong inversion leads to better transistor ratio matching compared to using weak inversion [40], [43].

In the proposed VR, a proportional-to-absolute-temperature (PTAT) voltage is converted to a current proportional to μT^2. This current is used to extract a temperature-stable reference voltage from the V_{GS} of a diode-connected NMOS. In addition to a compact all-MOSFET passive low-pass filter (LPF), a feedback technique is also proposed for wide bandwidth PSR enhancement. The VR is fabricated in a standard 0.18 µm CMOS process.

4.2 Proposed Reference Voltage Architecture

This section explains the blocks proposed voltage reference. In this section each of the schematic of each of the blocks is explained.

4.2.1 Conceptual Block Diagram

The conceptual block diagram of the proposed VR circuit is shown in Figure 4.1. A PTAT voltage is generated using a PTAT voltage generator and converted to a current proportional to μT^2, which serves as a bias current for the whole VR. Finally, a diode-connected nMOS transistor (active load) is used to generate a temperature-stable reference

voltage:

$$V_{REF} = V_{TH} + \alpha V_T \tag{4.1}$$

where α is determined by transistor ratios, V_{TH} (threshold voltage) serves as a complementary to absolute temperature (CTAT) voltage, and αV_T is a PTAT voltage.

A 5-bit trimming is applied to the output current to cancel the effects of process variation. Also, in order to compensate for the unwanted parasitic diode leakage current at high temperatures, a temperature compensation branch is introduced to increase the output bias current at high temperatures. The PTAT voltage generator, the V-to-I converter, and the feedback form a self-biased current source. The feedback in a self-biased current source is used to provide feedforward and feedback paths for power supply noise. The feedback and feedforward paths enhances the PSR performance of the VR up to medium range frequency. The passive LPF is a compact all-MOSFET low-pass filter used to attenuate the supply noise at high frequencies.

4.2.2 PTAT Voltage Generator

The minimum supply voltage in most voltage references is dependent on the reference output voltage. Hence a simple way to decrease the minimum supply voltage of a voltage reference circuit is to reduce the reference's output voltage. In bandgap references, this can be done by either making sure that only part of the material bandgap affects the circuit or lowering the material bandgap. The latter is not feasible in standard CMOS technologies but the former solution is feasible and can be implemented in several ways.

The most power efficient and compact technique for low-power, low-voltage bandgap reference design is to virtually lower the material bandgap using an electrostatic field. By this, the circuit 'senses' a bandgap which is the material bandgap lowered by the electrostatic field. To implement this method one has to replace the conventional BJT with a dynamic threshold MOS transistor (DTMOS).

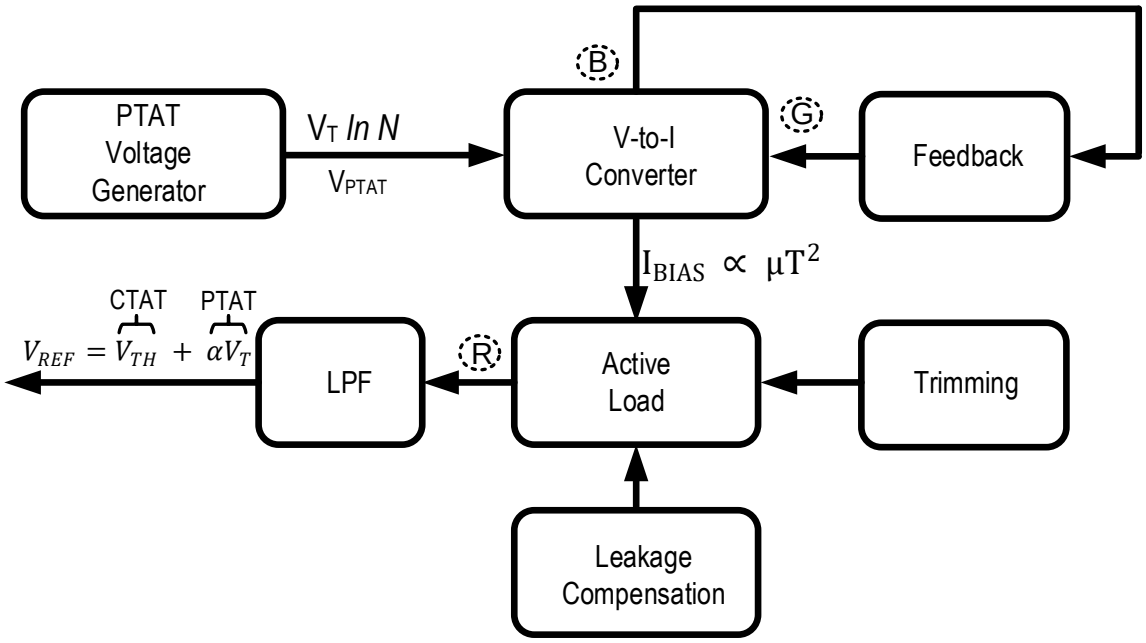


Figure 4.1: The Basic Concept of the Proposed VR

A cross-section of DTMOS is shown in Figure 4.2a. As can be seen, this device is a standard pMOS transistor with an interconnected body and gate [43], and its operation is similar to a BJT or a weak-inversion MOS operation; hence, it can be viewed as a lateral BJT with an extra gate over the base or as a MOS whose threshold voltage is dynamically controlled by the V_{GS} voltage.

Unlike diodes, which require at least 0.7 V turn-on voltage, DTMOS requires voltage even lower than the typical MOSFET threshold voltage. MOSFET threshold voltage scales with the process; however, the turn-on voltage of diodes is almost always fixed. This makes the DTMOS ideal for low-voltage applications. The DTMOS is compatible with digital CMOS technologies and can replace diodes or sub-threshold-based MOSFETs in conventional VRs.

As shown in Figure 4.2b, the difference between source-to-body voltages of two DTMOS with different aspect ratios is adopted to realize a PTAT voltage. The PTAT voltage, as seen in (4.4.4) is independent of high-order nonlinear temperature parameter, *m*, unlike in conventional sub-threshold-based MOSFET VRs. The temperature characteristics of two DTMOS transistors' source-to-body or source-to-gate voltages [44] with different aspect ratios and the resultant PTAT voltage (V_{PTAT}) are shown in Figure 4.2c.

$$V_{DTMOSi} = \frac{|V_{TH}|}{m} + V_T \, ln\left(\frac{I_{BIAS}}{I_{D0}} . \frac{1}{S_{DTMOSi}}\right); \quad i = 1, 2 \tag{4.2}$$

$$V_{PTAT} = V_{DTMOS1} - V_{DTMOS2} = V_T \, ln\left(\frac{S_{DTMOS2}}{S_{DTMOS1}}\right) \tag{4.3}$$

$$V_{PTAT} = V_T \, ln \, N \tag{4.4}$$

where $S_i = \left(\frac{W}{L}\right)_i$, $N = \frac{S_{DTMOS2}}{S_{DTMOS1}}$, $V_T = \frac{kT}{q}$ is the thermal voltage, I_{D0} is process dependent characteristic current and V_{DTMOSi} is the source- to- gate voltage of transistor $DTMOSi$.

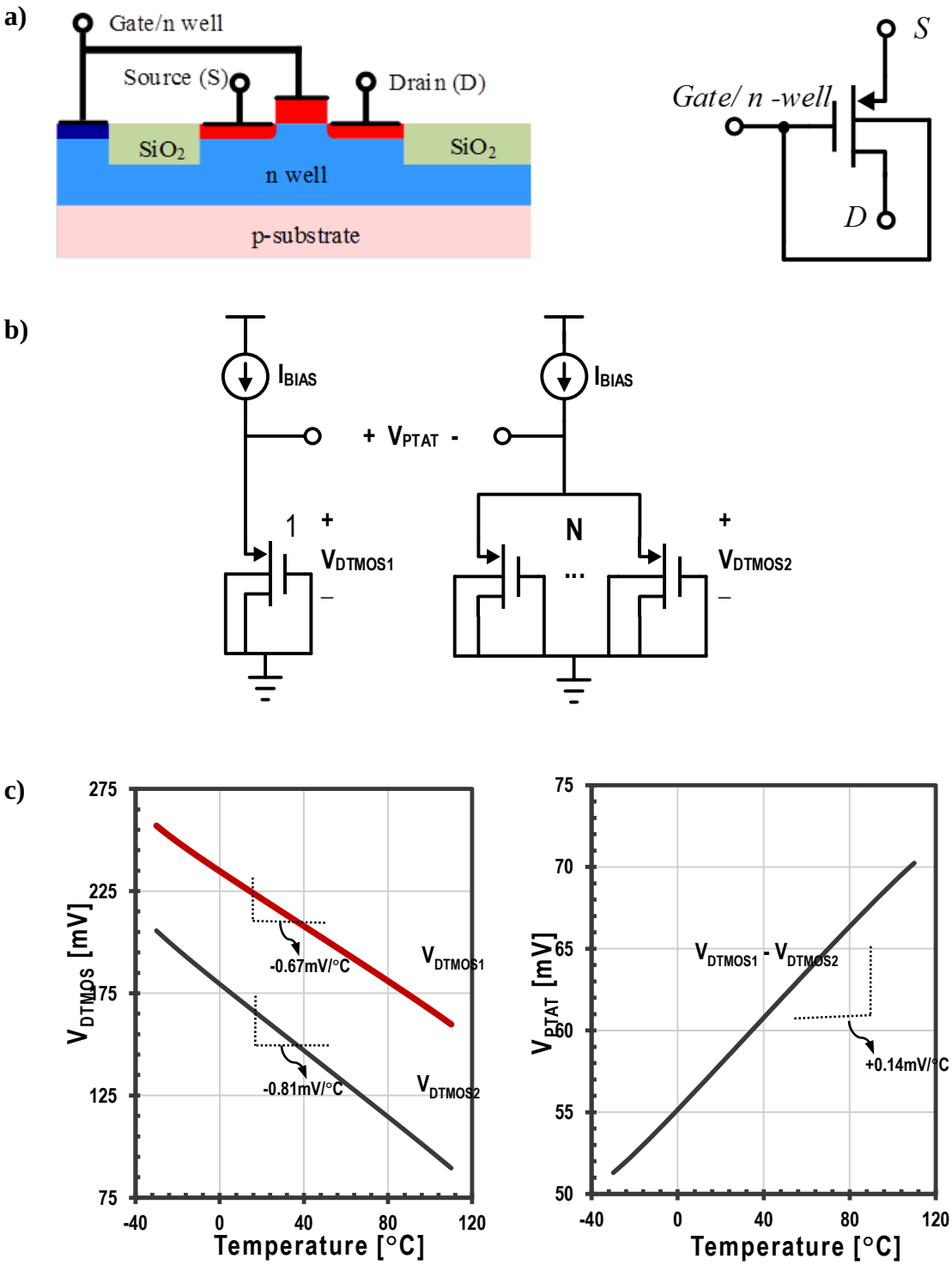


Figure 4.2: Cross Section of a DTMOS Transistor and Schematic Connection b) PTAT Generation from DTMOS c) Simulated Temperature Characteristics of DTMOS and Corresponding PTAT Voltage

4.2.3 Self-Biased Current Source

The self-biased current source serves as the core of the proposed VR and consists of an asymmetric source-input voltage–to-current converter (formed by transistors $MN1, MN2, MP1$ and $MP2$), the PTAT voltage generator from the $DTMOS1$ and $DTMOS2$, and a feedback branch (consisting of $DTMOS0$, $MN0$ and $MP0$). In Figure 4.3, the asymmetric source-input voltage-to-current converter (transconductance) is used to convert the PTAT voltage from the DTMOS into a bias current for the VR. In addition to minimizing the voltage difference between nodes A and B, the feedback is also used to realize a partial feedforward transfer function for power supply noise.

Assuming the channel length is sufficiently long, the representation for the drain, I_D, for a MOSFET in strong inversion [45] is given by

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\,[V_{GS} - V_{TH}]^2 \tag{4.5}$$

From (3.2) and for MN1 and MN2 in strong inversion; we can derive I_{BIAS}

$$V_{GSi} = V_{THi} + \sqrt{\frac{2I_{BIAS}}{k_n S_i}}, where\ k_n = \mu C_{OX}, i = MN1, MN2 \tag{4.6}$$

$$V_{GSMN1} - V_{GSMN2} = \sqrt{\frac{2I_{BIAS}}{k_n}}\left[\frac{1}{\sqrt{S_{MN2}}} - \frac{1}{\sqrt{S_{MN1}}}\right] \tag{4.7}$$

Equating (4.4) and (4.7) yields,

$$\sqrt{\frac{2I_{BIAS}}{k_n}}\left[\frac{1}{\sqrt{S_{MN2}}}-\frac{1}{\sqrt{S_{MN1}}}\right]=V_T\,ln\,N \tag{4.8}$$

$$I_{BIAS}=\frac{k_n}{2}(V_T\,ln\,N)^2 S_{MN1}\left[\sqrt{\frac{S_{MN1}}{S_{MN2}}}-1\right]^2 \tag{4.9}$$

The current is determined only by the aspect ratios (S_{DTVM1}, S_{DTVM2}, S_{MN1} and S_{MN2}). Unlike the current in [41], the current here is not dependent on the temperature dependent gate-to-surface coupling coefficient, m. This makes the current significantly less dependent on process variations.

The mobility depends on temperature [10] as:

$$\mu(T)=\mu_0\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{4.10}$$

Where μ_0 is the mobility at temperature T_0, and α_μ is the mobility temperature exponent.

Given (4.10), the I_{BIAS} in (4.9) can be becomes:

$$I_{BIAS}=\frac{C_{ox}\mu_0}{2}\left(\frac{1}{T_0}\right)^{\alpha_\mu}\left(\frac{k}{q}ln(N)\right)^2 S_{MN1}\left[\sqrt{\frac{S_{MN1}}{S_{MN2}}}-1\right]^2 T^{2+\alpha_\mu} \tag{4.11}$$

Differentiating (4.11), the temperature coefficient (TC) of I_{BIAS} is given by:

$$TC_{I_{BIAS}}=\frac{\left(\frac{\partial I_{BIAS}}{\partial T}\right)}{I_{BIAS}}=\frac{2+\alpha_\mu}{T} \tag{4.12}$$

Note that the α_μ is above -2 in standard $0.18\mu m$ which makes I_{BIAS} decrease with temperature. This unique property is due to process used for the design of the proposed VR.

The proposed self-biased current source allows us to generate a current that is independent of *m* without using transistors in weak inversion, resistors, or bipolar junction transistors (BJTs). The DTMOS technique allows for the minimum voltage requirement of the self-biased current source to scale with technology, unlike the solutions in [31], [34], [42] which use BJTs. Also, since the I_{BIAS} is independent of m and does not depend on devices in weak inversion, as opposed to [41], it is easier to design the circuit in standard CMOS process and still achieve a high precision VR.

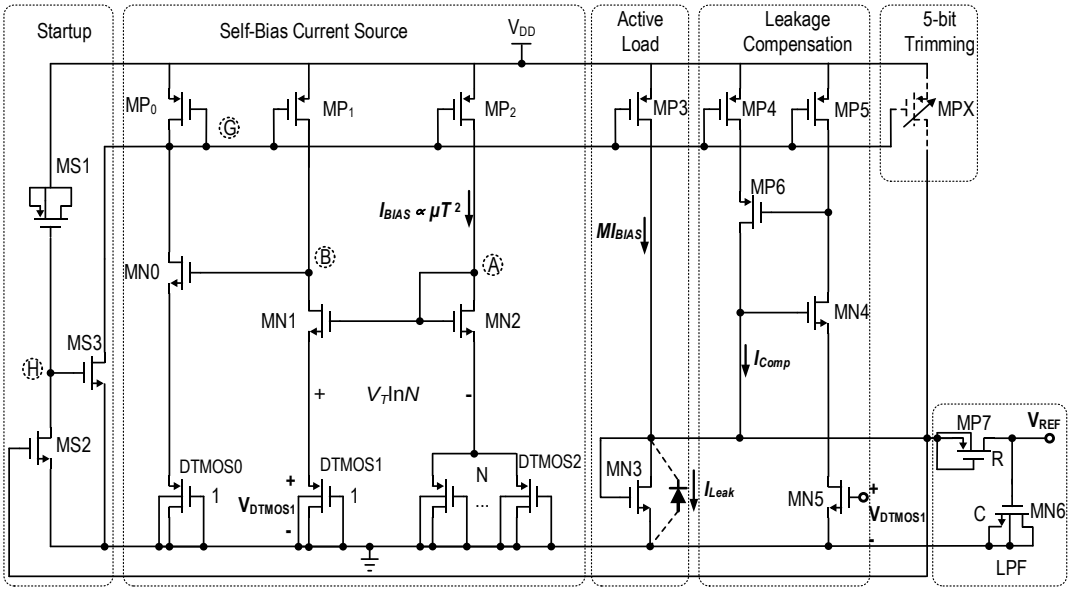


Figure 4.3: Proposed VR circuit

4.2.4 Startup Circuit

The self-biased current source is stable for currents corresponding to the current given by (4.9), and zero, a startup circuit (formed by $MS1 - \mathrm{MS3}$ as shown in Figure 4.3) is used to ensure that the former state is achieved. At startup, the transistor $MS1$ is off since V_{REF} is zero. This makes the voltage across MOSFET capacitor, $MS1$, zero; hence, the node H is pulled up to V_{DD}. As a result $MS3$ is turned on, pulling down node G and thereby allowing I_{BIAS} to flow. When I_{BIAS} reaches the value given by (4.9), V_{REF} becomes the desired value and $MS2$ is turned on. This pulls the node H to ground as the voltage across MOSFET capacitor, $MS1$ is charged to V_{DD} ; MS3 is turned off, which allows the VR to function as desired. The MOSFET capacitor, $MS1$, gets discharged when the circuit is powered down.

4.2.5 Reference Generator and Leakage Compensation

Consider the active load of the proposed VR, shown in Figure 4.3. Assuming that all transistors of the active load (MN_3 and MP_3) work in the strong inversion, the output reference voltage will be given by:

$$V_{REF} = V_{GSMN3} = V_{THMN3} + \sqrt{\frac{2MI_{BIAS}}{k_n S_{MN3}}} \tag{4.13}$$

From (4.13), it is apparent that the temperature dependence of the V_{REF} consist of two components. The first component is due to the temperature dependence of V_{TH}, and the

second is due the temperature dependence of I_{BIAS} as well as the mobility (μ). As is evident from (4.13), I_{BIAS}, which is proportional to K_n (μC_{ox}), completely suppresses the effect of the temperature dependence of mobility (μ) on V_{REF}.

As a first order approximation, the V_{TH} decreases linearly with temperature [5] as given by:

$$V_{TH}(T) = V_{TH0} - \alpha_{V_{TH}}(T - T_0) \tag{4.14}$$

where V_{TH0} is the threshold voltage at temperature T_0, and $\alpha_{V_{TH}} = \frac{\partial V_{TH}}{\partial T}\Big|_{T=T_0}$. Using (4.9) and (4.13), we can write the expression for the output voltage V_{REF} as:

$$V_{REF} = V_{THMN3} + \alpha V_T \tag{4.15}$$

$$\alpha = ln\, N \sqrt{M \frac{S_{MN1}}{S_{MN3}}} \left[\sqrt{\frac{S_{MN1}}{S_{MN2}}} - 1\right]^{-1} \tag{4.16}$$

Leakage current effects at room temperature is insignificant. Nevertheless, intrinsic carrier concentration (ni) is exponentially dependent on temperature, and thus, leads to increase in leakage current at high temperature [12]. The leakage current is essentially the reverse saturation current of a diode, which gives it an exponential temperature dependency. A diode placed between the drain and body terminals of a MOSFET is used to model the existence of the leakage current for large signals as shown Figure 4.3. This is similar to a temperature dependent current source between the drain and the source terminals of the MOSFET.

The substrate diode leakage current of the diode-connected nMOS transistor, $MN3$,

becomes substantial at high temperatures (above 80 °C). This leads to a sharp decrease in the V_{REF}. The leakage compensation circuit, formed by $MN4 - MN5$ and $MP4 - MP6$, is used to compensate for the effect of the leakage on the output current. A thermal switch, formed by transistors $MN4, MN5\ and\ MP6$ is used allow I_{COMP} (copied multiple of I_{BIAS}) to flow into the drain $MN3$ to compensate the leakage current. The $MN5$, with its gate connected across $V_{DTMOS1,}$ is off at low temperatures (below 50 °C) since its threshold voltage at these temperatures is higher than V_{DTMOS1}. As a result, $MP6$ is also off, hence, cutting off I_{COMP}. $MN5$ gradually begins to turn on as temperature increases because V_{TH} decreases faster with a temperature rise compared to the V_{DTMOS1}. $MP6$ is progressively turned on as the temperature increases since its gate voltage is slowly lowered. This allows I_{COMP} to steadily increase to compensate for the leakage current as temperature increases. Figure 4.4a and Figure 4.4b illustrate the active load and leakage compensation circuit configuration for low and high temperature operations, respectively.

4.2.6 PSR Improvement

The self-biased current source is designed to ensure high PSR performance from low to medium frequencies. The feedback, which used to minimize the voltage difference between node A and B in the self-biased current source, creates a feed-forward transfer function (Path0 in Figure 4.5a) for power supply noise (PSN). Power supply noise can be distributed to the output through four (4) main paths as shown in Figure 4.5a:

i) Path0, $v_{dd,noise}$ from the source of MP_0 to node G; ii) Path1, $v_{dd,noise}$ from the source of MP_1 through node B to node G; iii) Path2, $v_{dd,noise}$ from the

source of MP_2 through node A and B to node G; iv) The direct path, $v_{dd,noise}$ from the source of MP_3 to node R

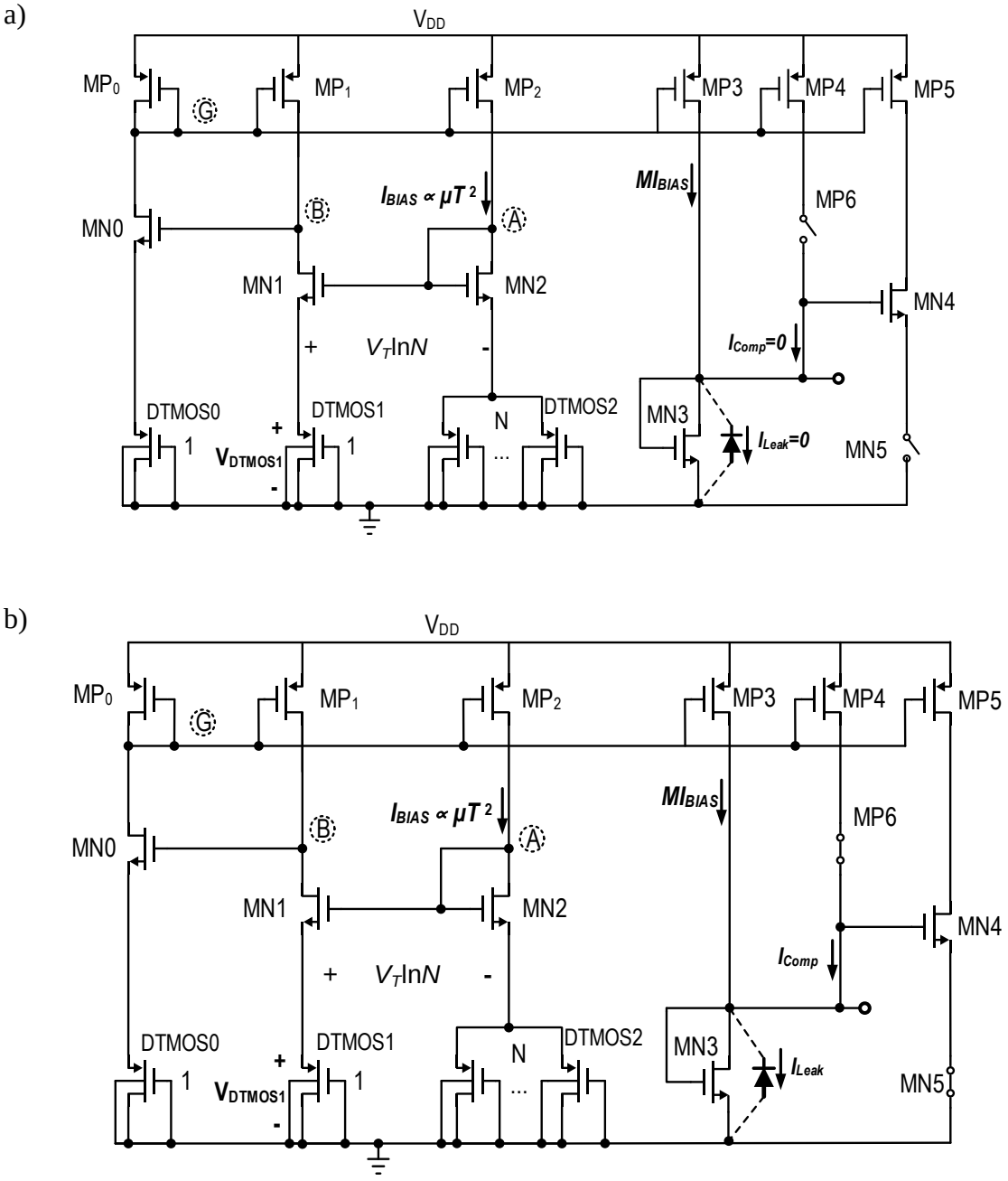


Figure 4.4: Leakage Compensation Configuration a) Low Temperature and b) High Temperature

Paths 0, 1, and 2 are the main paths for $v_{dd,noise}$ to be distributed to node G (gate of MP_3) and forms a cancellation path. The supply noise through the path0 forms the feed-forward path.

The main idea behind the PSR improvement is to use the cancellation path to replicate the supply noise through the direct path and hence cancel the supply noise at the output.

The supply noise at the node R (v_R) is given by:

$$v_R = (PSR_{Direct} - PSR_{Can})v_{dd,noise} \tag{4.17}$$

where $PSR_{Direct}$and PSR_{Can} is the PSR through the direct path and cancellation path to node R, respectively.

From Figure 4.5,

$$PSR_{Direct} = \left(\frac{g_{mMP3}}{g_{mMN3}} + \frac{1}{g_{mMN3}r_{dsMP3}}\right) \approx \left(1 + \frac{1}{g_{mMN3}r_{dsMP3}}\right) \tag{4.18}$$

$$PSR_{Can} = path0 + (path1 + path2)A_{feedback} \tag{4.19}$$

where $path0 = \frac{g_{mMP0}r_{dsMN0}}{1+g_{mMP0}r_{dsMN0}} \approx 1$, $path1 \approx -r_{dsMN1}g_{mMP1}$ and $path2 = \frac{r_{dsMN1}}{r_{dsMP2}}(r_{dsMP2}g_{mMP2} + 1) \approx r_{dsMP2}g_{mMP2} + 1$

From Figure 4.5, for low to medium frequencies, the closed gain of the feedback loop ($A_{feedback}$), would be,

$$A_{feedback} = \begin{cases} \left(\frac{1}{g_{mP0}r_{dsP1}}\right) & f < f_{GBW(feedback)} \\ 0 & f_{GBW(feedback)} \leq f < f_{medium} \end{cases} \tag{4.20}$$

Hence,

$$PSR_{Can} = \begin{cases} \left(1 + \dfrac{1}{g_{mPMOS} r_{dsPMOS}}\right) & f < f_{GBW(feedback)} \\ 1 & f_{GBW(feedback)} \leq f < f_{medium} \end{cases} \tag{4.21}$$

where we assume $g_{mPMOS} r_{dsMPOS} = g_{mMPi} r_{dsMPi}$ since all the PMOS transistors form a current mirror.

Using (4.17), (4.18) and (4.21), the PSR at node R becomes,

$$PSR_R = \frac{v_R}{v_{dd}} \approx \begin{cases} 0 & f < f_{GBW(feedback)} \\ \dfrac{1}{g_{mPMOS} r_{dsPMOS}} & f_{GBW(feedback)} \leq f < f_{medium} \end{cases} \tag{4.22}$$

Note the PSR_R includes both the supply noise from the gate and source of $MP3$.

As apparent from (4.22), for frequencies within the feedback loop bandwidth, the noise at node G (v_G) is $\left[1 + \frac{1}{gmr_{ds}}\right] v_{dd,noise}$. This is because of the feedback and feedforward effects. Consequently, the power supply noise at the gate (node G) and at the source of $MP3$ cancel out at the output of the VR for frequencies within the loop bandwidth, as evident from (4.22). Beyond the loop bandwidth frequency, noise at node G becomes $v_{dd,noise}$; hence, the noise through the output resistor of $MP3$ remains at the output as shown in (4.22). The feedback helps maintain a high PSR at the output up to a medium frequency range. Thus we need an improvement of the PSR at higher frequencies, which is achieved by using the compact MOSFET passive LPF discussed next.

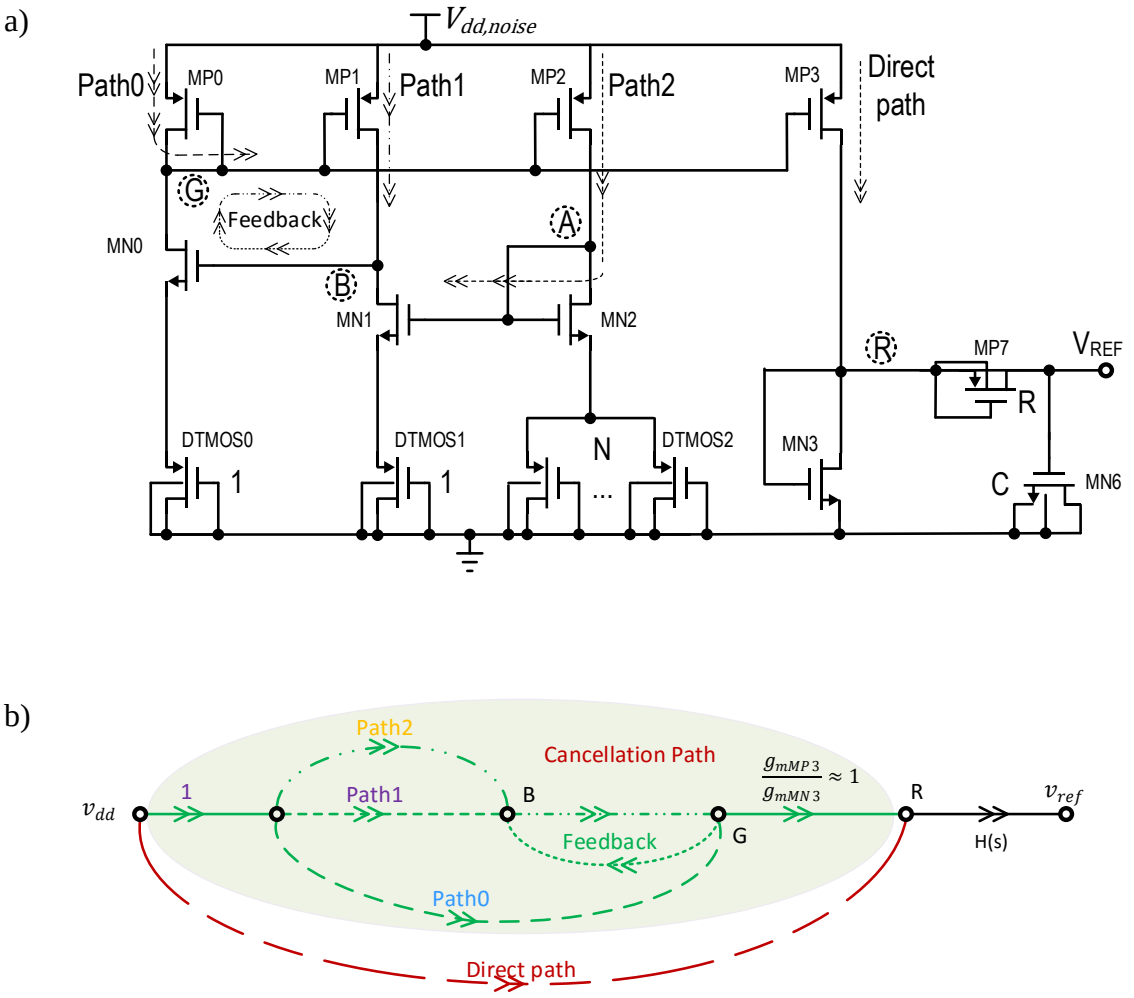


Figure 4.5: Power Supply noise Paths at (a) and Small Signal Diagram for PSR at (b)

4.2.7 Compact MOSFET Low Pass Filter (LPF)

At high frequency domain, parasitic capacitors play an increasingly important role in PSR performance. A compact MOSFET LPF with an equivalent 3 dB bandwidth of 200 Hz is used in the output to attenuate the noise without any extra power consumption. The LPF, formed by transistors MN6 (in strong inversion) and MP7 (in cut-off), can be

modeled as an RC filter shown in Figure 4.6a. From the model, the transfer function of the filter is given by:

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1}{1 + \frac{sC_2R}{1 + sC_1R}} \tag{4.23}$$

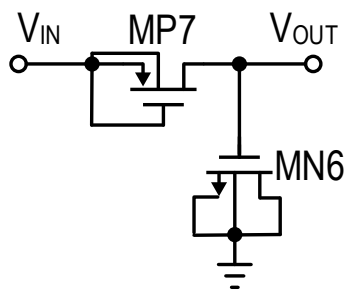
where $R \approx R_{dsMP7}, C_1 \approx C_{gdMP7} + C_{bdMP7}\ and\ C_2 \approx C_{gsMN6} + C_{gdMN6}$.

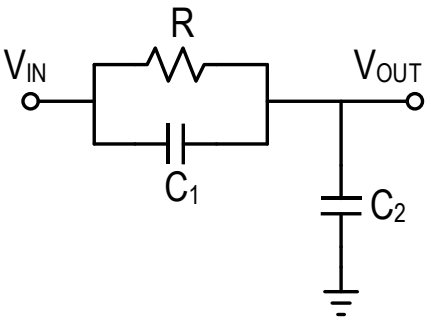
Note $C_{gsMN6} = \frac{2}{3}C_{ox}(WL)_{MN6} + C_{ox}(WL_D)_{MN6}$, $C_{gdMN6} = C_{ox}(WL_D)_{MN6}$, $C_{gdMP7} = C_{ox}(WL_D)_{MP7}$, and $C_{bdMP7} = C_{ox}(WL)_{MP7}$. The L_D is the process dependent lateral diffusion of junction under gate and C_{ox} is the gate capacitance per unit area. The resistance, R $(1/g_{dsMP7})$, can be estimated by differentiating (3.2) while noting that $V_{SGMP7} = 0$;

$$g_{dsMP7} = \partial I_D/\partial V_{DS} == (m-1)\mu C_{ox}V_T S_{MP7}\left(e^{-\frac{V_{DS}}{V_T}}\right)e^{-\frac{|V_{TH0},p|}{mV_T}} \tag{4.24}$$

The simulated frequency characteristics of the compact MOSFET LPF and its equivalent RC model are shown in Figure 4.6b. Unlike a conventional RC filter of same 3 dB bandwidth, the compact MOSFET LPF occupies a small chip area (9 μm × 20 μm).

a)





MOSFET LPF

Equivalent RC Model

b)

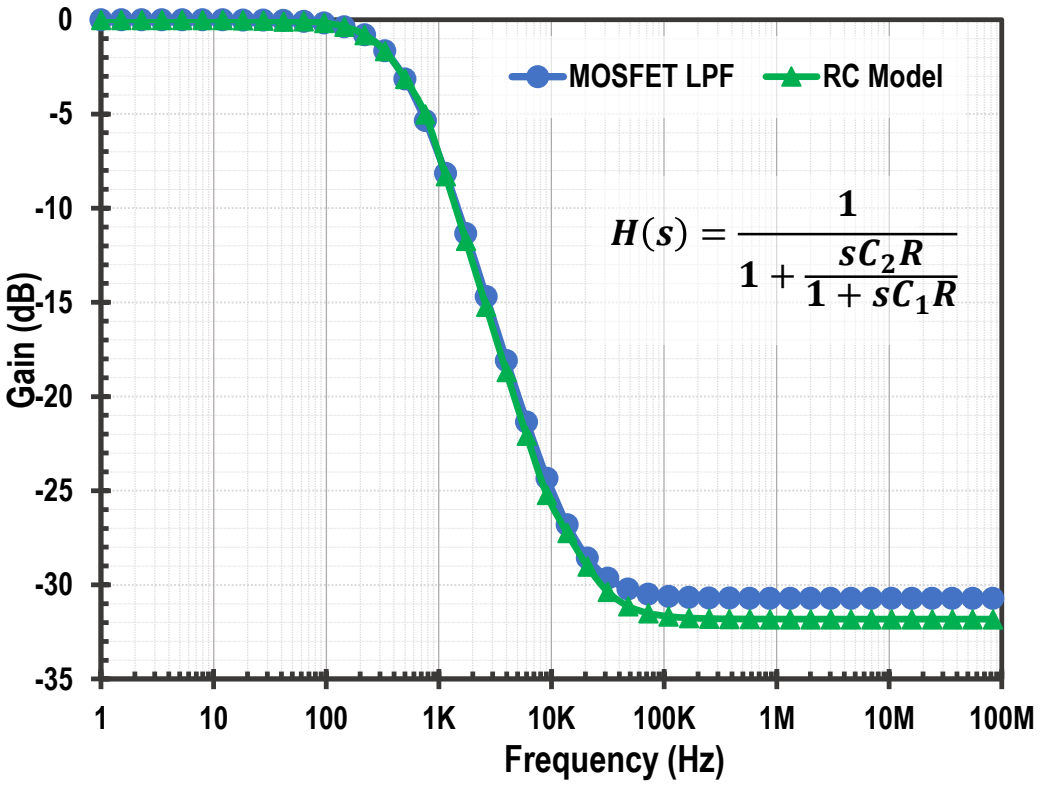


Figure 4.6: The compact MOSFET LPF and Equivalent RC Model along with b) the MOSFET LPF and Equivalent RC Model Response

4.3 Design Considerations

The main design consideration for the proposed VR are channel length modulation, process variation and the dynamic range. These considerations are discussed in detail in this section.

4.3.1 Channel Length Modulation

For proper device-matching minimum width and lengths should be not selected for the devices sizes determining gains. Moreover, in order to substantially minimized the channel length modulation, long channel lengths are used for all transistors in the current mirrors, the feedback transistor $MN0$ and the active load nMOS $MN3$. The supply noise feeds through to the various nodes of the sub-circuits including the output node via the parasitic capacitances of the transistors. Thus, there is a need to keep the transistors small to minimize these parasitics at critical nodes.

The supply voltage of DTMOS transistors is limited by the diode turn-on voltage in conventional bulk silicon technology [37]. The p-n diode between the body and source should be reverse biased; hence, the V_{DTMOS} must not exceed 0.6 V. This is not a concern in our design since the current converter and feedback ensure that V_{DTMOS} never exceeds threshold voltage.

4.3.2 Process Variation

Neglecting the mismatch of the W/L ratios in (4.15), the sensitivity of the reference voltage is mainly due to the accuracy of the threshold voltage of the diode-connected

nMOS transistor $MN3$. To achieve a low sensitivity to the process, we have to minimize the variation of the threshold voltage of the $MN3$.

Essentially, the Gaussian distribution of threshold depends on process variation and mismatch. The mismatch variation magnitude, dominated by random dopant fluctuations, is generally observed to be inversely proportional to √WL [34]. Consequently, such variations can be reduced by setting the channel length and width of $MN3$ large, such that the mismatch is negligible compared to the effect of process variations.

The process variations correspondingly affect adjacent transistors [11], and are due to intra-wafer, inter-wafer, or inter-batch non-uniformity of the process [11]. From simulations, we observed that the variation of the reference voltage due to process variations is above 7% across temperatures. I used a 5-bit trimming circuit to reduce this variation to less than 1% as shown in Figure 10. The trimming process involves a single-step trim. I adjusted the output bias current to achieve the designated reference value while also minimizing the temperature dependence. From the experimental results, I measured a variation of 0.9% and 0.357% for the untrimmed references and trimmed references, respectively.

4.3.3 Dynamic Range

The self-bias current source dictates the minimum supply voltage for the VR. For better transistor ratio results, we had to ensure that transistors $MN1$ and $MN2$ could operate in strong inversion. Hence, the condition below had to be satisfied:

$$V_{DD} > V_{DTMOS2} + V_{GSMN_2} + V_{dsatMP_2} \tag{4.25}$$

To ensure that all the transistors of pMOS current mirrors (MP_0-MP_3) were in strong inversion, a minimum supply of 0.8 V was required in the *IBM 0.18 µm* CMOS process. The maximum supply imposed by the maximum drain-source Voltage (V_{DSmax}) allowed for MOS transistors, as expressed below:

$$V_{DD} < V_{REF} + V_{DSMP3}(max) \tag{4.26}$$

In *IBM 0.18 µm* CMOS process, V_{DSmax} is 1.8 V; hence, the maximum supply is 2.2 V.

4.4 Temperature Compensation

By differentiating (4.15) with respect to temperature yields:

$$\frac{\partial V_{REF}}{\partial T} = -\alpha_{V_{TH}} + \frac{k}{q} ln\, N \sqrt{M \frac{S_{MN1}}{S_{MN3}}} \left[\sqrt{\frac{S_{MN1}}{S_{MN2}}} - 1 \right]^{-1} \tag{4.27}$$

where k is the Boltzmann constant and q is the electron charge. The first-order temperature coefficient of the threshold voltage ($\alpha_{V_{TH}}$) of a long channel nMOS transistor in the *IBM 0.18 µm* CMOS process is approximately 0.940 mV/℃. From (4.20), the temperature coefficient is independent of the carrier mobility and of the gate-to-surface coupling coefficient, *m*. The perfect suppression of the temperature dependence of the mobility and of the gate-to-surface coupling coefficient, *m*, was achieved, which led to a smaller temperature coefficient over a wide temperature range (−30 ℃ to 110℃) compared to

other VRs [33], [34], [42], [28– 29].

The zero temperature coefficient (ZTC) is achieved by setting (4.27) to zero:

$$\sqrt{M\frac{S_{MN1}}{S_{MN3}}} = \frac{\alpha_{V_{TH}}\left[\sqrt{\frac{S_{MN1}}{S_{MN2}}} - 1\right]}{\frac{k}{q} ln\, N} \tag{4.28}$$

It is clear that this is true within some approximations and the simplified transistor characteristics. This first-order condition for a ZTC has been calculated by neglecting non-ideal effects. Henceforth, if (4.28) is satisfied, (4.15) can be written as $V_{REF} = V_{TH0} + \alpha_{V_{TH}} T_0$.

4.5 Simulation Results

The proposed VR circuit was simulated over the temperature range -10 °C to 110 °C using a power supply voltages from 0.8 V-2.2 V. Figure 4.7 shows the simulation results for the V_{REF} across the temperature range. The change in the output voltage, obtained in simulation, is 0.6 mV to 1.3 mV for the supply voltages from 0.8 V-2.2 V over the temperature range. This corresponds to TC from 12 ppm to 23 ppm. The results of the simulation verify that the circuit operates according to the analysis given above and a temperature-stable voltage can be obtained. Figure 4.8 shows the 140 Monte-Carlo runs for mismatches and process variation. The results shows a δ of 7.617% and 0.539% for the untrimmed and trimmed reference respectively.

To verify the performance of the start-up circuit, I replaced the power supply by a step voltage and performed a transient simulation. The waveforms are shown in Figure 4.9.

Figure 4.10 illustrates how measured reference voltage varies with supply voltage. The line regulation (LR) is about 0.087%/V for voltages above 0.8 V at room temperature.

The PSR performance between 1Hz and 800MHz shown in Figure 4.11, where the PSR with and without the compact MOSFET LPF are compared. The PSR without compact MOSFET LPF is more than 40dB at 10MHz due to the feedback and feed-forward paths, while the PSR with compact MOSFET LPF is more than 50dB for frequencies up to 60MHz. This shows that the techniques used in the proposed VR can immensely improve PSR over a very wide bandwidth with minimum area overhead.

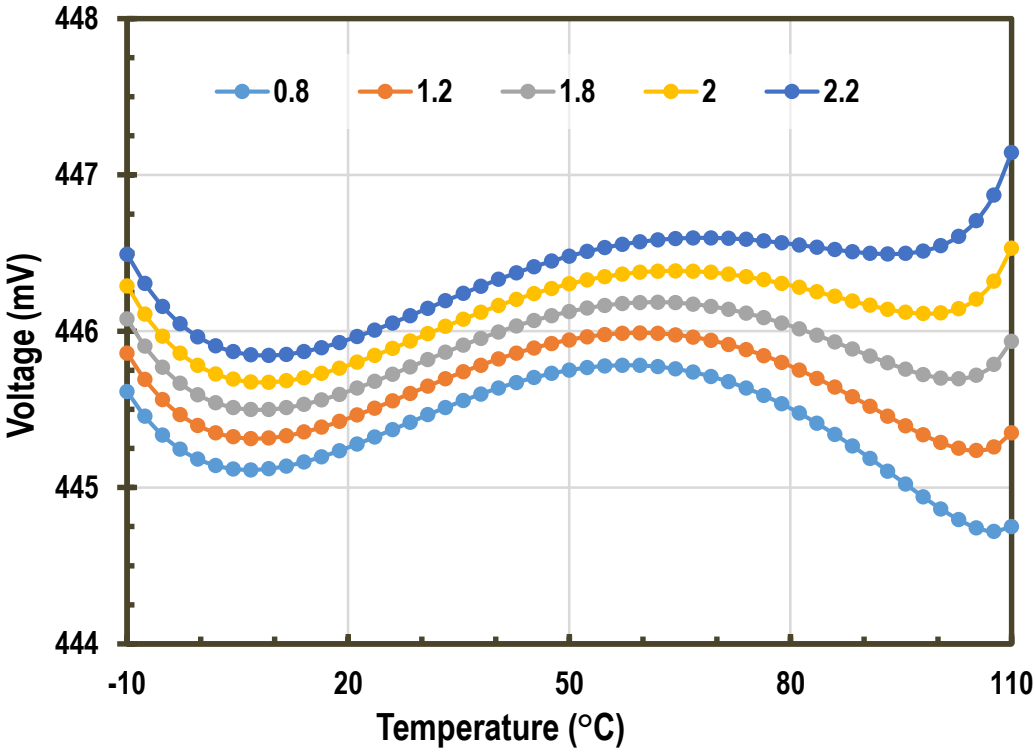


Figure 4.7: Simulation of V_{REF} for Various Supply Voltages

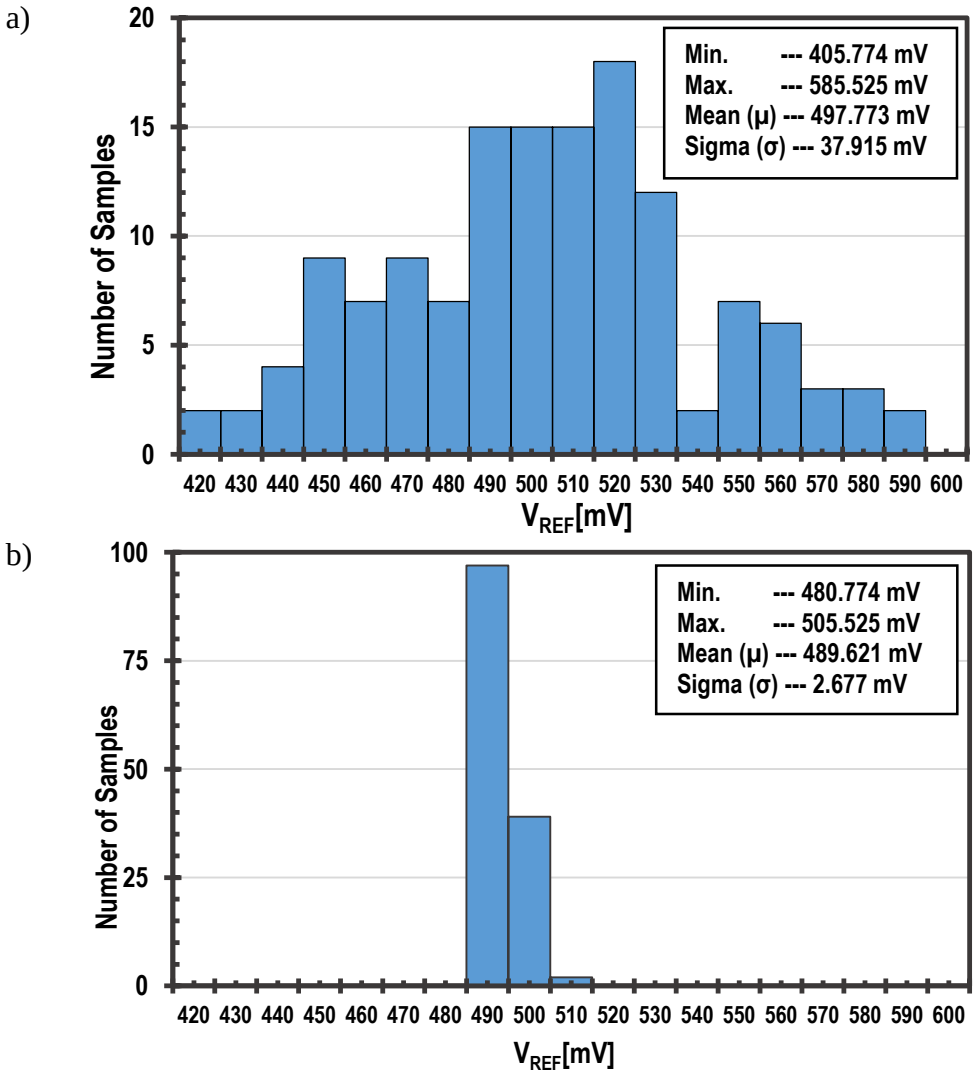


Figure 4.8: Monte Carlo Simulation for V_{REF} a) Untrimmed VREF @ 27 °C and b) Trimmed VREF @ 27 °C

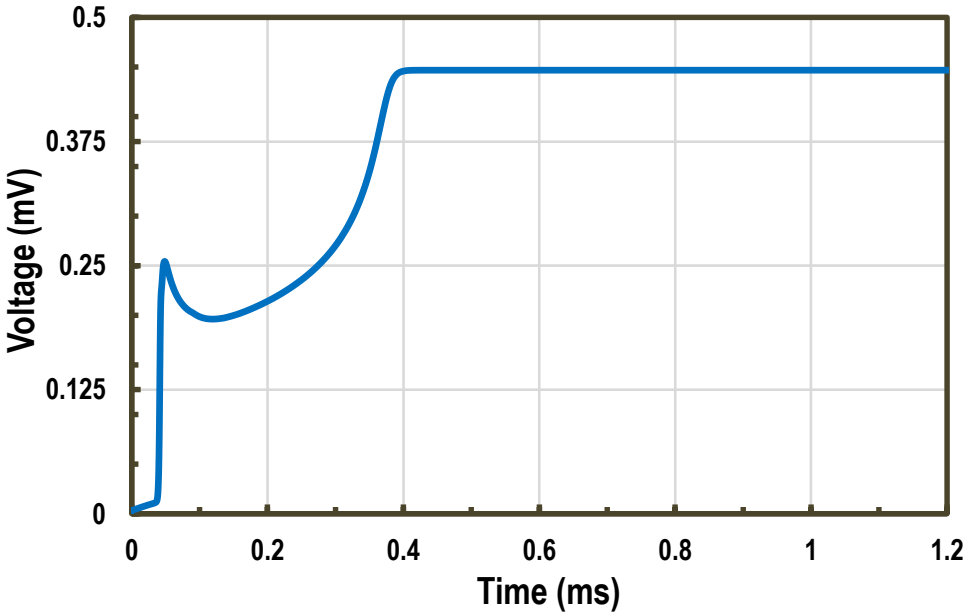


Figure 4.9: Simulation Results for Start-Up of the VR

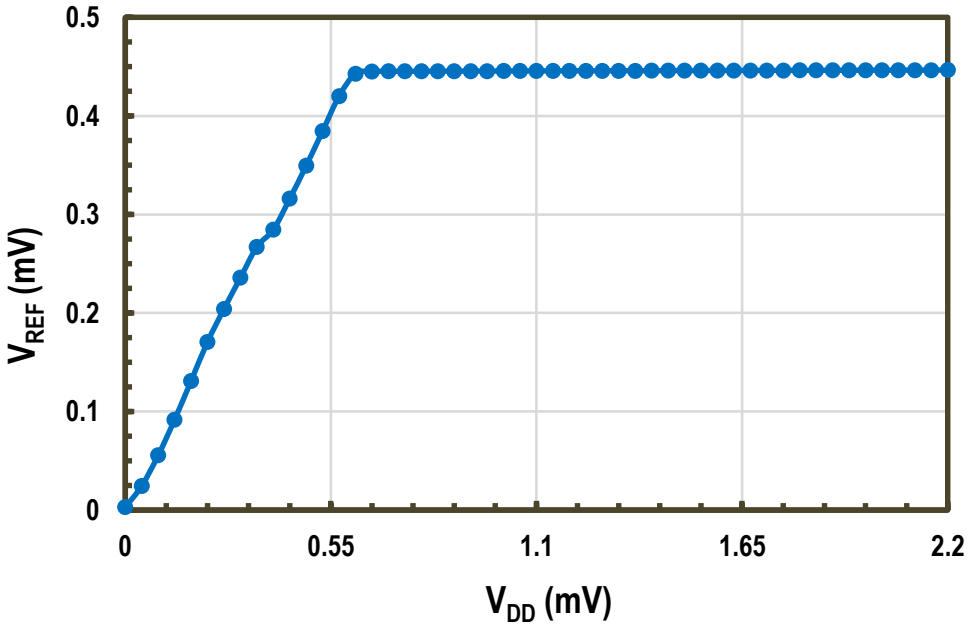


Figure 4.10: Reference Voltage v.s. Power Supply Voltage

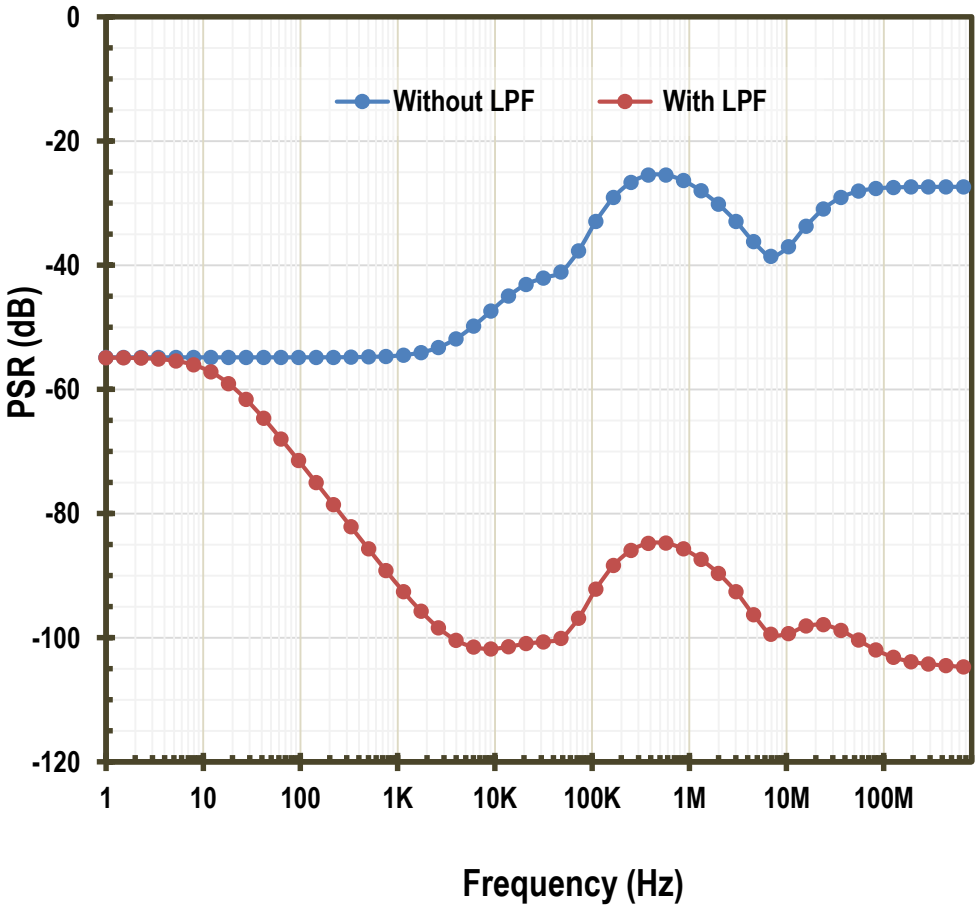


Figure 4.11: Simulated PSR of Output VR

5. EXPERIMENTAL RESULTS

This section presents the experimental results for the voltage references discussed in sections 3 and 4. We will discuss the laboratory setup for the testing. The test results for the two circuit is also presented in this section.

5.1 Setup for Testing the VRs

The proposed VRs have been fabricated with IBM 0.18-µm CMOS technology. The DC supply voltage for the VRs is provided from programmable output LDO (TPS7A8300RGWR). The schematic of the of the power supply for the VR testing is shown in the Figure 5.1. The LDO output can be varied from 0.8 V to 3.95 V in steps of 50 mV. The 6-pole DIP switch is used to vary the output of the LDO depending on the switch position.

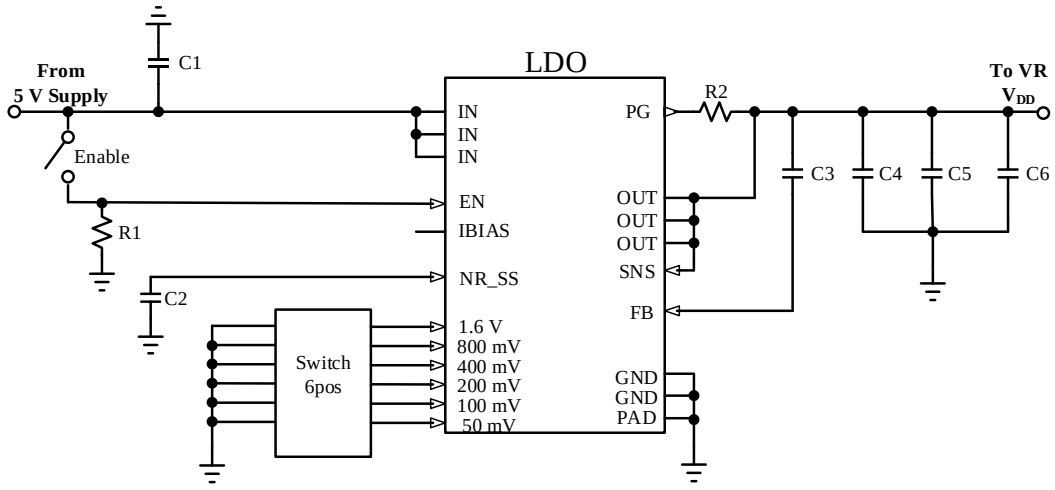


Figure 5.1: DC Power Supply for VR

The setup for temperature performance measurement is shown in Figure 5.2b. An ultra-low input bias current (TI-OPA 129) amplifier is used as an external buffer to isolate loading of the DC multi-meter from the voltage reference. The power-supply rejection measurement setup is shown in Figure 5.2a. The supply ripple injected is around 200 mV peak across the entire frequency range.

An external high bandwidth (TI-OPA 354) amplifier is connected at the output of the VR for the PSR measurement. The amplifier is constructed to have a gain of around 40 dB over the measured frequency to avoid hitting the measurement equipment sensitivity floor. As in the Figure 5.3, to avoid the temperature performance of TI-OPA 129 and the TPS7A8300RGWR from affecting the DC test results, the VR chip is mounted on separate PCB and placed in the temperature chamber alone. A picture of the laboratory setup for testing is shown in Figure 5.2.

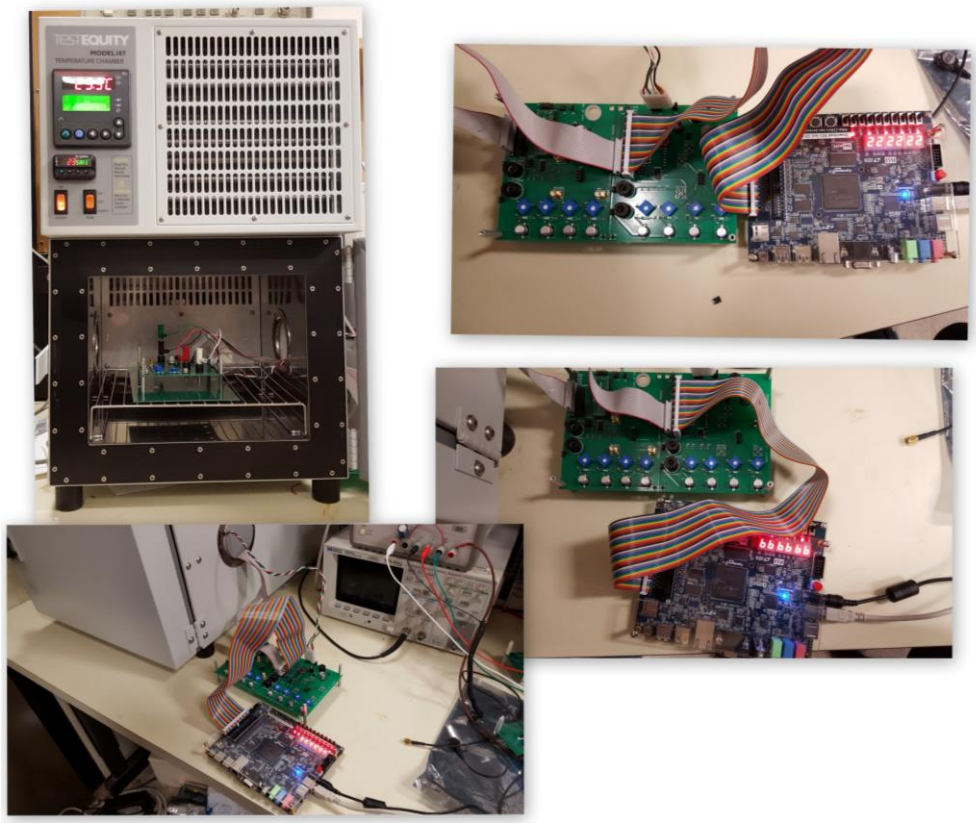


Figure 5.2: The Laboratory Setup for Testing

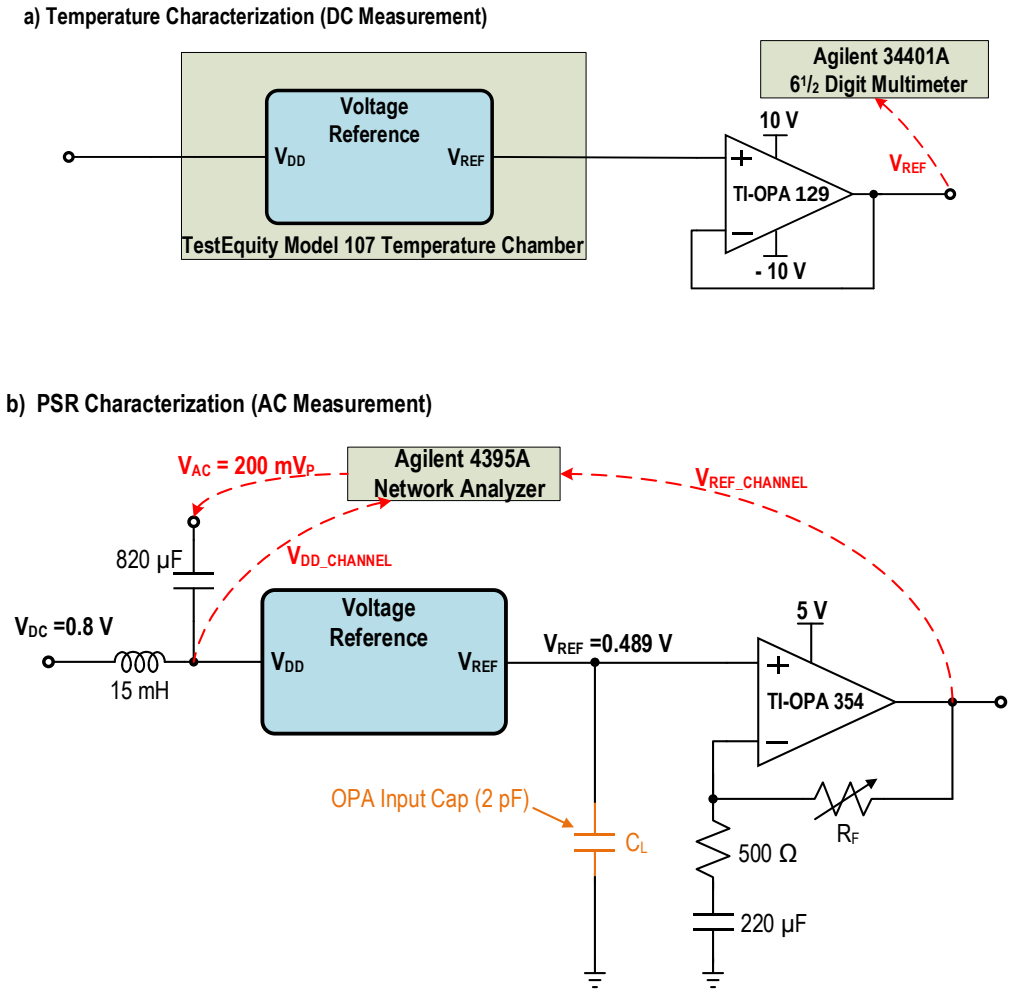


Figure 5.3: PSR and Temperature Stability Measurement Setup

5.2 Experimental Results An All-Mosfet Voltage Reference With -50 dB PSR @ 80 Mhz For Low Power Soc Design

The chip micrograph is shown in Figure 5.4, and the active area is 0.018 mm^2. This compact area is achieved because I did not use any resistors, or BJTs.

The TCs the trimmed reference is 19ppm to 29 ppm for supply from 1.1 V to 2.2 V shown in Figure 5.5. Figure 5.6 shows a similar plot in which the performance of five trimmed samples for temperatures ranging from -35℃ to 80℃ is shown. The 3 sigma variation of the trimmed reference is 1.0462%

Figure 5.7 illustrates how measured reference voltage varies with supply voltage. The line regulation (LR) is about 0.093%/V for voltages above 1.2 V at room temperature.

The PSR performance between 10Hz and 80MHz is shown in Figure 5.8, where the PSR with and without the compact MOSFET LPF are compared. The PSR without compact MOSFET LPF is more than 28dB for frequencies up to 30MHz due to the feedback and feed-forward paths, while the PSR with compact MOSFET LPF is more than 50dB up to 70MHz. This shows that the techniques used in the proposed VR can immensely improve PSR over a very wide bandwidth with minimum area overhead.

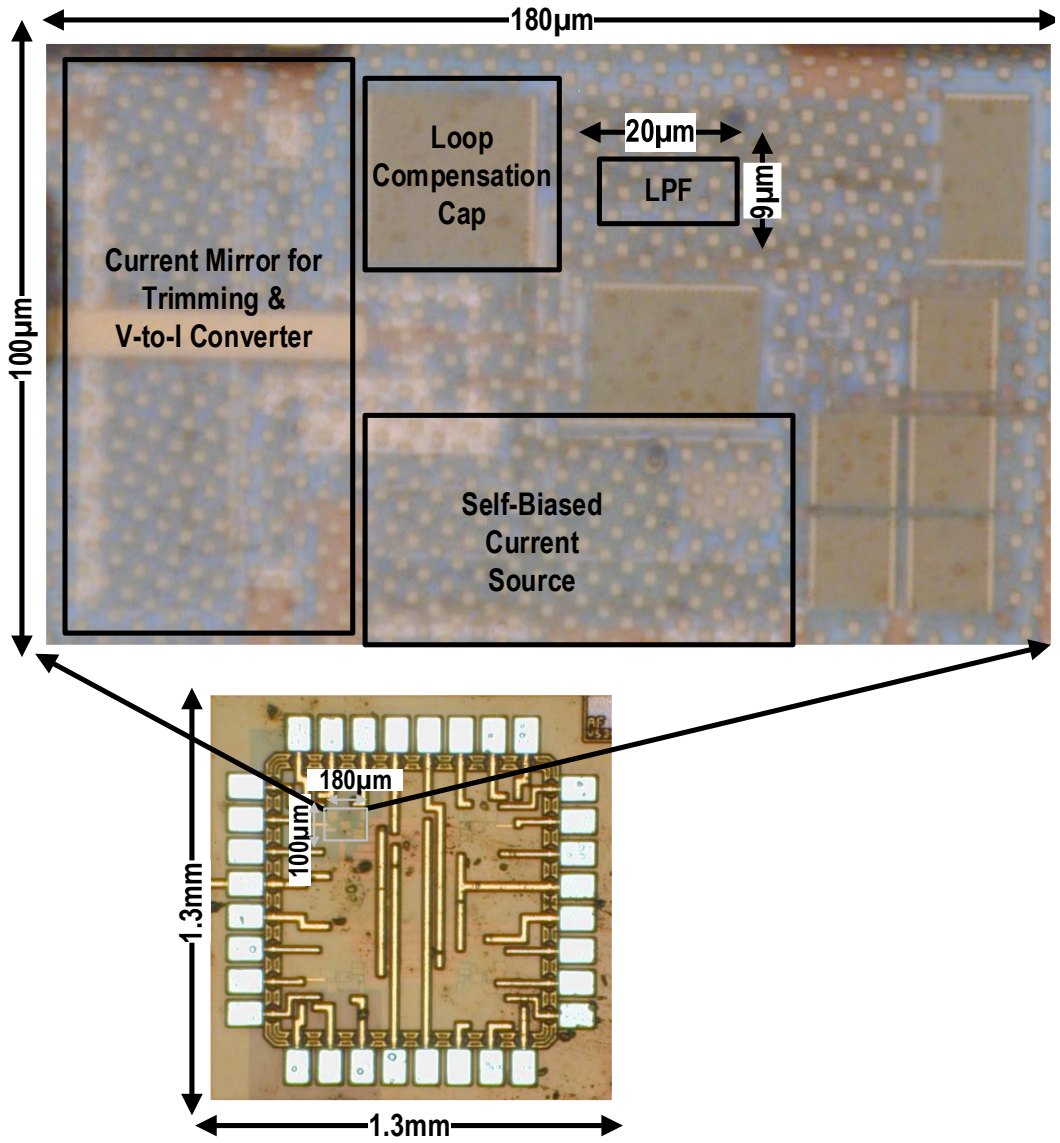


Figure 5.4: Chip Micrograph of the Proposed VR1

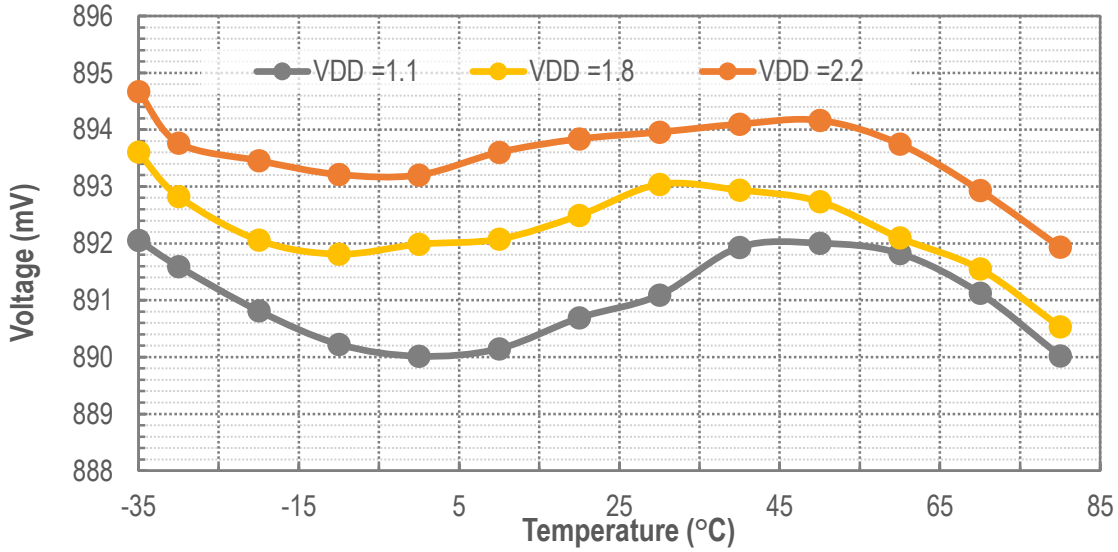


Figure 5.5: Measured Temperature Dependence of the Proposed VR1

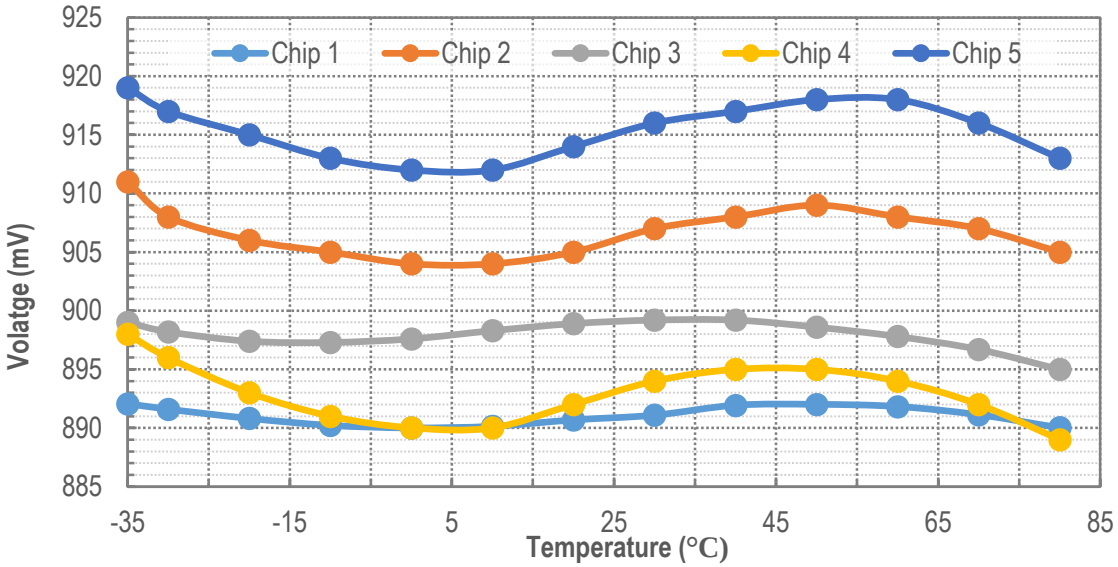


Figure 5.6: Measured Temperature Dependence of Five Trimmed Samples

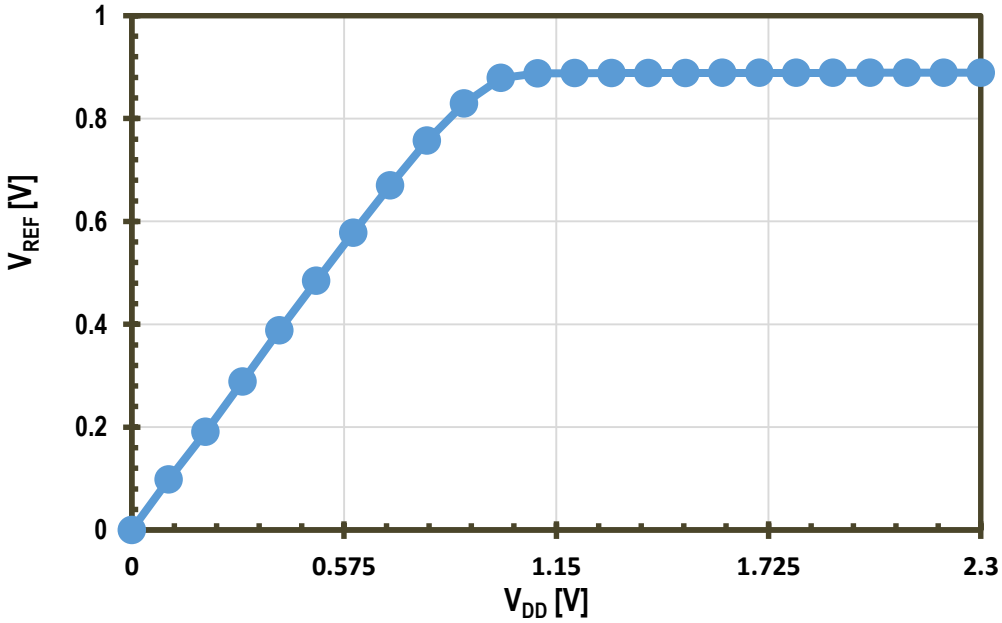


Figure 5.7: Supply dependence of V_{REF}

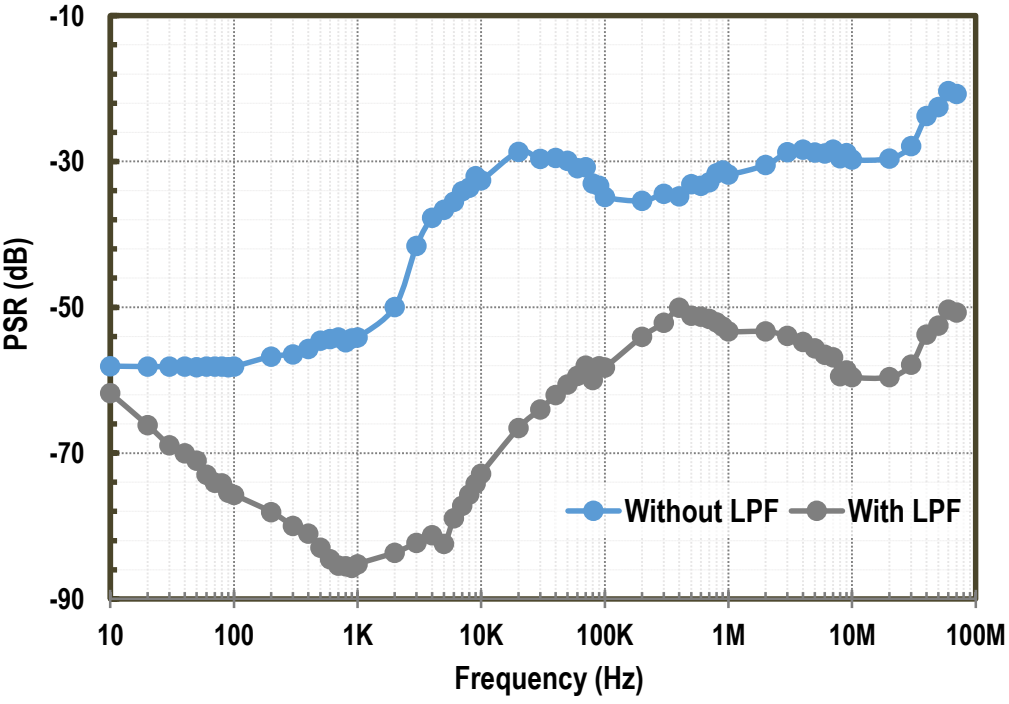


Figure 5.8: Measured PSR of VR1

5.3 Experimental for the All-MOSFET Sub-1 V Voltage Reference with a -51 dB PSR up to 60 MHz

The proposed VR has been fabricated with IBM 0.18-μm CMOS technology. The chip micrograph is shown in Figure 5.8, and the active area is 0.0143 mm^2. This compact area is achieved because I did not use any resistors, BJTs, or devices in the subthreshold. The compactness gained was at the expense of a relative higher quiescent power dissipation.

The TCs of the untrimmed voltage references ranged from 16-113 ppm with an average of 48.8 ppm, while those of the trimmed ones ranged from 9-29 ppm with an average of 18.3 ppm for supply from 0.8 V to 2. The temperature performance of a single untrimmed and trimmed sample for 0.8 V, 1.5 V and 2 V is shown in Figure 5.9a and Figure 5.9b, respectively. Figure 5.9c and Figure 5.9c shows plots in which the performance of six untrimmed and trimmed samples measured at 0.8 V for temperatures ranging from −30 ℃ to 110 ℃ is shown. The variation of untrimmed references and that of trimmed references was 0.9% and 0.357%, respectively.

Figure 5.10a illustrates how measured reference voltage varies with supply voltage. The line regulation (LR) is about 0.076%/V for voltages above 0.8 V at room temperature. Figure 5.10b shows the measured current consumption of the proposed VR, which decreases with rising temperature, with 450nA at room temperature.

The PSR performance between 10Hz and 70MHz is shown in Figure 5.11, where the PSR with and without the compact MOSFET LPF are compared. The PSR without compact MOSFET LPF is more than 40dB for frequencies up to 30MHz due to the feedback and feed-forward paths, while the PSR with compact MOSFET LPF is more than

50dB up to 60MHz. This shows that the techniques used in the proposed VR can immensely improve PSR over a very wide bandwidth with minimum area overhead.

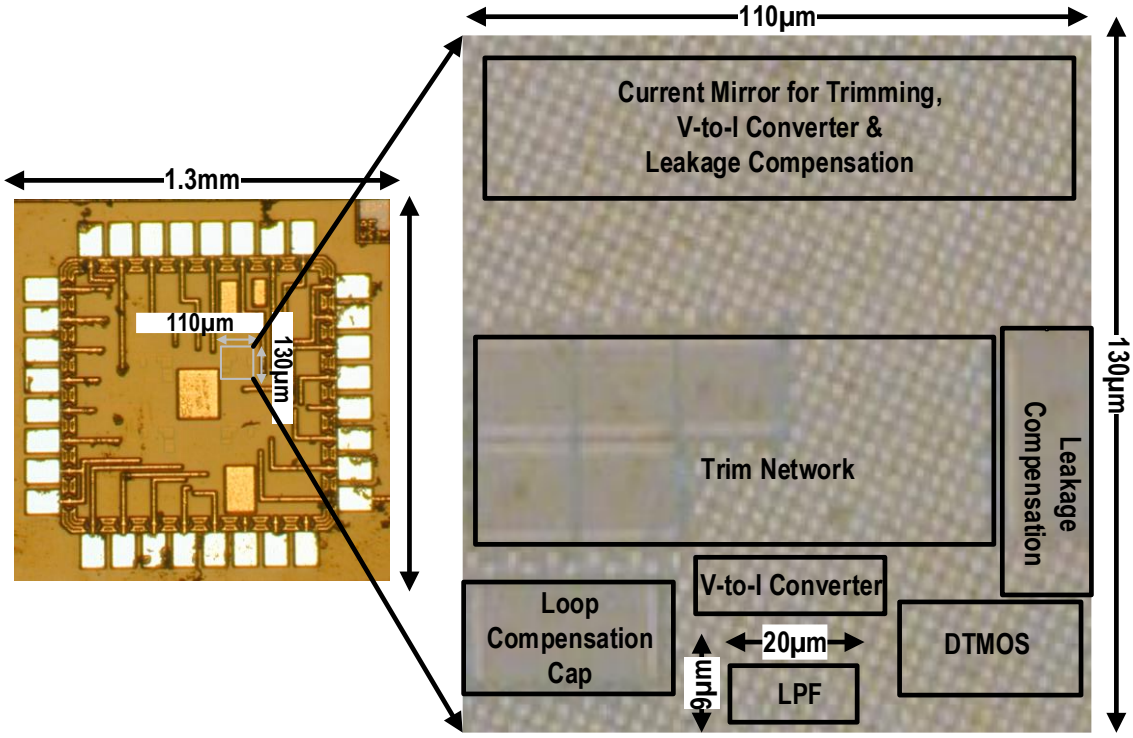
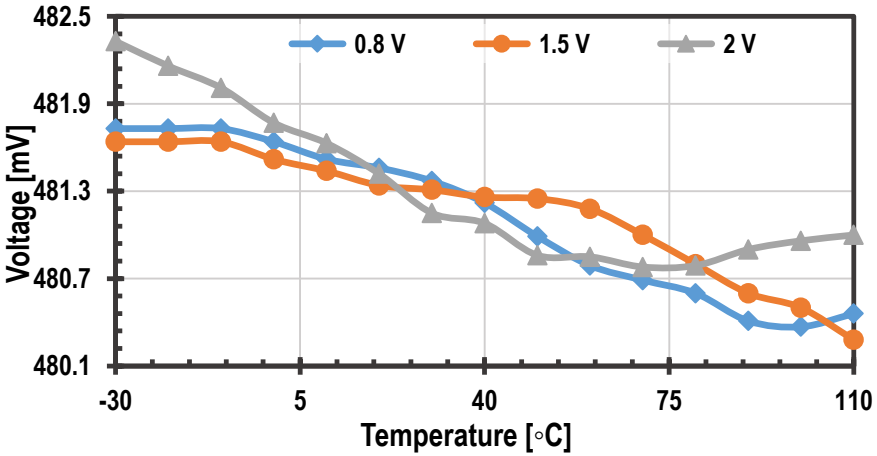
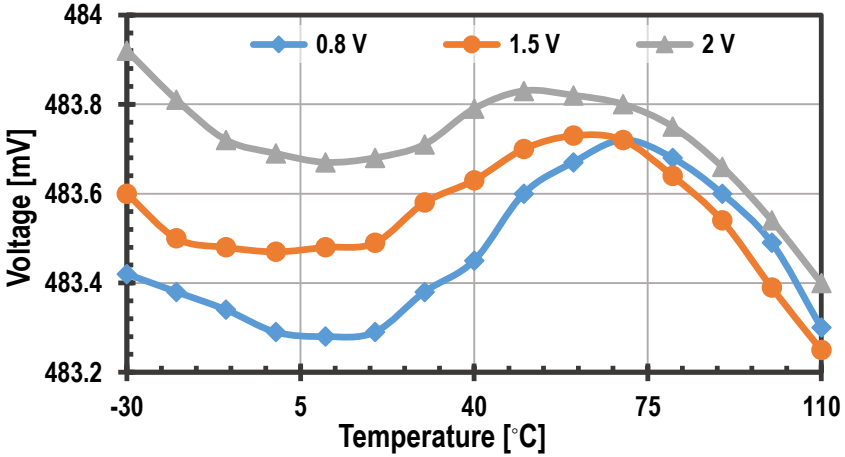


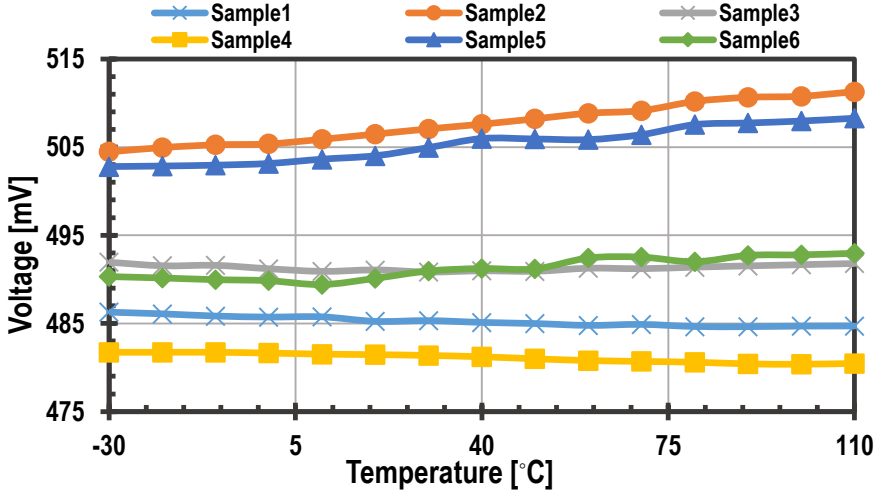
Figure 5.9: Chip Micrograph of the Proposed VR2



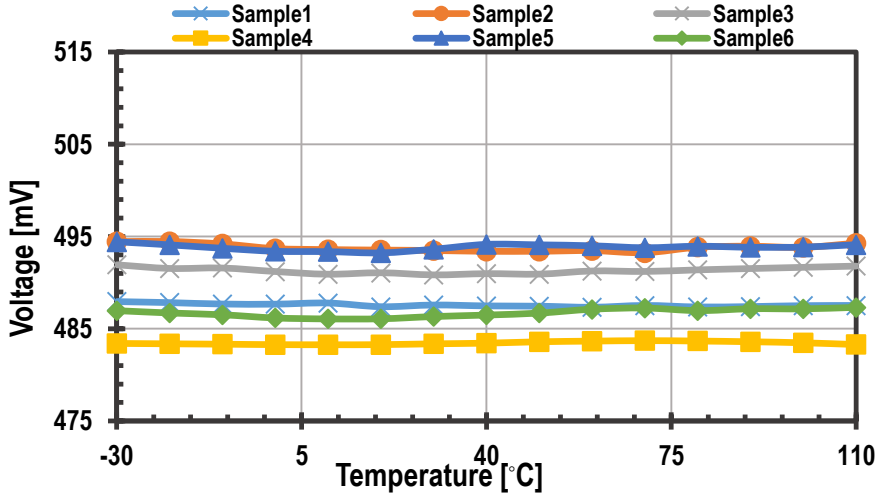
a) **Untrimmed reference for different supply voltages**



b) **Trimmed reference for different supply voltages**



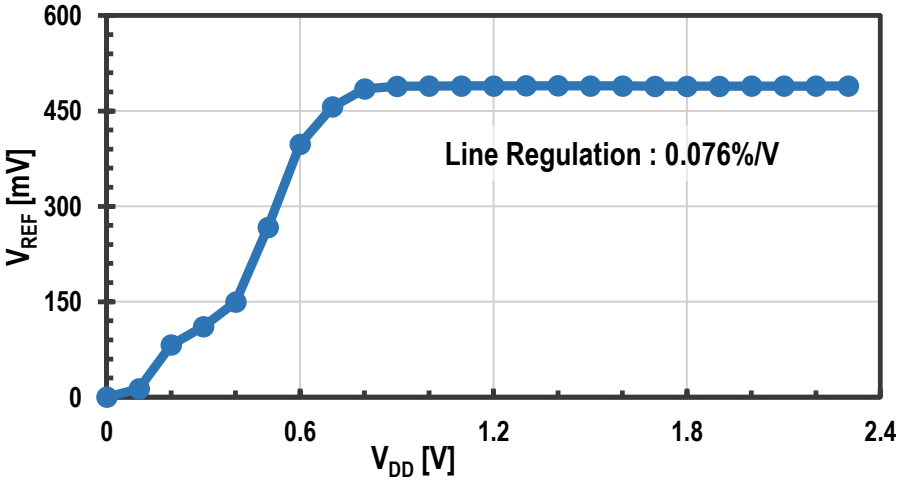
c) **Untrimmed reference for six samples**



d) **Trimmed reference for six samples**

Figure 5.10: Measured Temperature Dependence of the Output Voltage (V_{REF}) of the Proposed VR

a)



b)

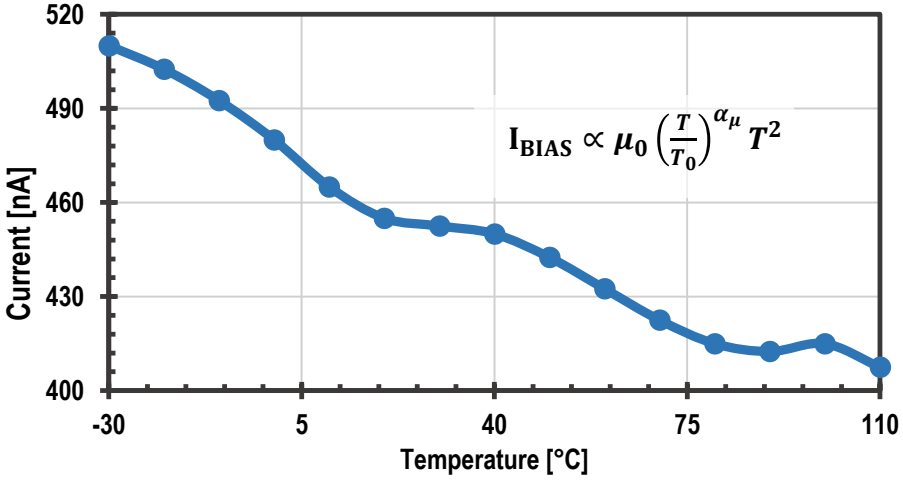


Figure 5.11: a) Supply Dependence of V_{REF} b) Quiescent Current of the VR2

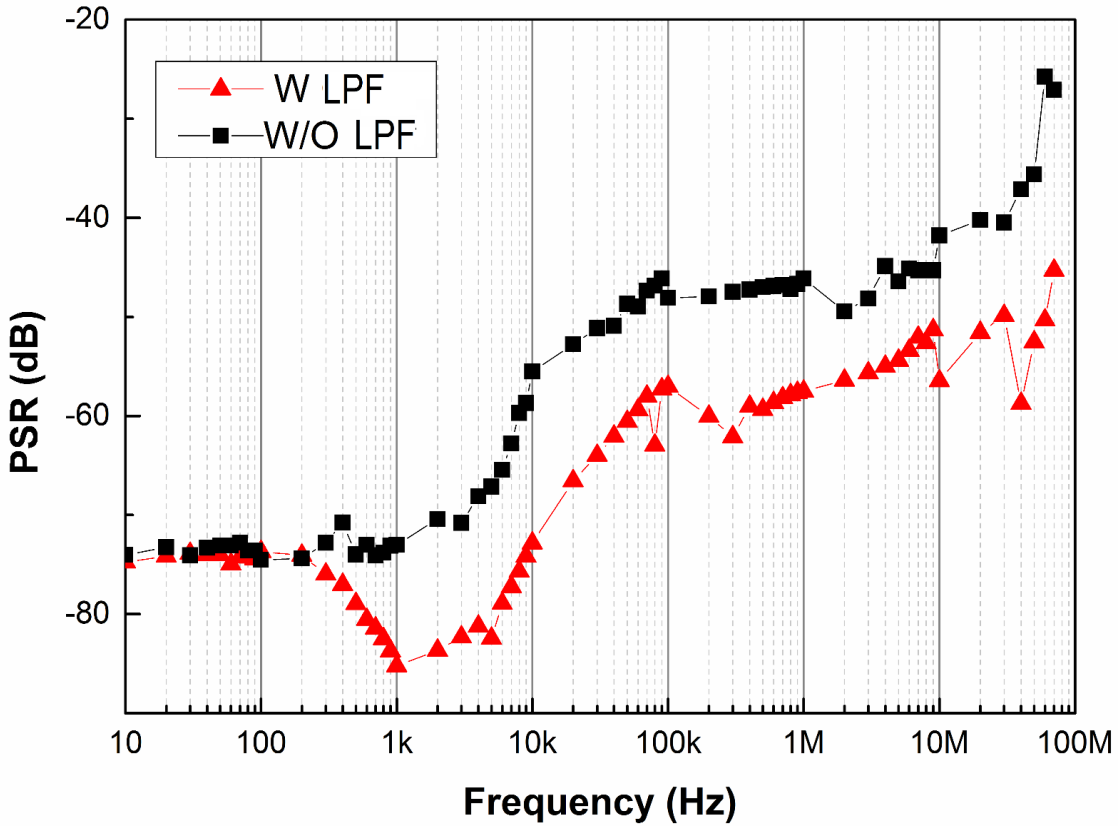


Figure 5.12: Measured PSR of Output Reference Voltage

Table 5.1 summarizes the performances of the two references proposed in this work and compares it with previously reported state-of-the-art voltage references. Although STBM VRs and switched mode VRs have advantages in power consumption, they usually occupy larger area due to the large transistor sizes and capacitances used. Furthermore, the proposed VRs compared with other VRs is more stable in terms of TC, LR, and PSR.

Table 5.1: Performance Summary and Comparison with Previous Works

Parameter	**This Work1**	**This Work2**	**[1] ISSCC 15**	**[3] JSSC 13**	**[4] ISSCC 15**	**[4] JSSC 09**	**[2] JSSC 02**	**[6] JSSC 2012**
Technology (CMOS)	0.18µm	0.18µm	0.13µm	0.18µm Twin-Well	0.35µm Twin-Well	0.35µm	0.5µm	0.13µm
Temperature Range (℃)	-35 - 80	-30 - 110	0 - 80	-40 - 120	-10 - 110	0 - 70	0 – 70	-20 - 85
Type	All MOSFET	All MOSFET	Switched Mode BGR with charge pump and resistors	BGR with STBM	BGR with resistors and STBM	STBM without resistors	BGR without resistors	Switched Mode BGR with resistors
Supply Voltage (V)	1.1 – 2	0.8 – 2	0.5 – 1.5	1.2 – 1.8	1.4 – 3	1.4 - 3	3.7	0.75 – 1.6
Supply Current (µA)	0.500	0.450	0.064	0.083	0.0205	0.214	378	0.230
Vref (V)	0.889	0.489	1.176	1.090	1.176	0.745	1.121	0.256
Ripple in Output Voltage	None	None	50µV	None	None	None	None	20mV
TC (ppm/℃)	19	9.33	75	147	12.75	15	120	40
LR (%/V)	0.098	0.076	0.198	N/A	0.198	N/A	N/A	N/A
PSR (dB)								
@100Hz	-75	-75	-40.0	-59	N/A	-45	-43	-70
@100kHz	-58	-57	N/A	-10.0	N/A	-22	-10	N/A
@10MHz	-60	-57	N/A	N/A	N/A	N/A	N/A	N/A
@60MHz	-50	-51	N/A	N/A	N/A	N/A	N/A	N/A
Die Area (mm^2)	0.0180	0.0143	0.0264	0.0294	0.4800	0.0550	0.4000	0.0700

6. CONCLUSIONS

Voltage and current references find applications in a variety of electronic circuits. These reference are usually required to produce same output or predictable outputs under varying circuit and environmental conditions. Temperature-drift is one of the most important condition to contend when designing a voltage reference.

In this thesis, three new voltage reference circuits were proposed, designed and fabricated in 0.18-µm CMOS technology. First, a BJT sub -1 V bandgap reference based on non-linear temperature compensation was presented. This reference achieved a temperature coefficient of 11ppm without any form of trimming. It was shown how the PSR of the bandgap can be enhance by using a feedforward technique.

A novel MOSFET-Based Voltage Reference with high PSR up to 60MHz implemented in IBM 0.18-µm CMOS technology was presented next. PSR improvement with feedback and feed-forward techniques have been described in detail. Also a LPF filter designed with MOSFET only was introduced. These allowed us to achieve a PSR better than 50 dB for frequencies up to 60 MHz. The concept of a DTMOS for low voltage application was described in detail. The VR which does not use any resistor, BJTs or subthreshold devices achieved a small temperature coefficient of 9.33ppm and consumes nanowatts of power at room temperature. The high performance and design flexibility with compact area makes this VR more suitable than other VRs for multifunctional SOC applications without any additional process requirement.

Another MOSFET-Based Voltage Reference with high PSR up to 60MHz implemented in IBM 0.18-µm CMOS technology was presented. The generation of PTAT

voltage from a composite transistor was introduce and used to design the voltage reference. The reference achieved 20ppm while consuming 720nW at room temperature. This reference also used the feedforward and feedback in addition to the compact MOSFET LPF to achieve high PSR from DC up to 60MHz.

Finally, the performances of the references are compared with the state-of-art-references in literature and it was concluded that the proposed voltage references have comparable performance with the bandgap references and better performance than the non-bandgap ones. Table 6.1 below shows the main difference between the two all MOSFET references proposed in this work.

Table 6.1: Main Difference Between the two Proposed VRs

	Proposed VR1	Proposed VR2	BGR in section 2.5
Type	All MOSFET	All MOSFET	BGR
PTAT Voltage source	Composite transistors in subthreshold	DTMOS	ΔV_{EB}
Output depends on m	Yes	No	No
Compensation	No	Leakage current	Piecewise nonlinear
Normalized Area	1.25	1	22.4
Normalized Power	2	1	25
Supply (V)	1.2 – 2	0.8 – 2	1.1 – 2.2
PSR @ 10MHz	-60	-57	-40

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APPENDIX

AN AUTO-CALIBRATED, TEMPERATURE COMPENSATED BANDGAP REFERENCE WITH ON CHIP HEATING

Due to the high precision requirement of integrated circuits used in applications such as automobile, avionics, and space, the embedded voltage references are expected to maintain a relatively fixed output voltage over a wide temperature range. For these applications it's also essential for the reference to have very high initial accuracies.

Most voltage references usually require one-time calibration (trimming) to achieve the high precision requirements. The single time calibration leads to the deviation of the reference voltage from the specified value after a period of operation, hence resulting in reduced system performance over time. This trimming is usually a single temperature point trimming (usually performed at room temperature) since more than one temperature point trimming requires heating the chip which is expensive.

To mitigate this problem, a scheme for voltage reference calibration on chip without requiring any external heating is introduce in this section. This allows for the reference voltage to be calibrate while in use. Based on the requirement of the application, the proposed scheme can optimize the reference voltage for best performance.

A.1 Calibration of a 2nd Order Bandgap Reference

Consider the Figure A.1, a 2nd order compensated bandgap reference voltage. To properly calibrate and optimized this reference voltage for minimum temperature coefficient, the voltage for three separate temperature points are used. For an ideal

reference, the volatges $V[T_1]$, $V[T_2]$ and $V[T_3]$ are equal. In a practical reference, best thermal stability is achieved by minimizing the difference between the voltages at these three temperatures. Equations (A.1) and (A.2) shows the expressions for optimizing the temperature performance. An optimized temperature performance is achieved if the value of $F(V)$ is minimized.

$$F(V)_{mn}|_{(x,y,z)} = \left|V[T_m]_{(x,y,z)} - V[T_n]_{(x,y,z)}\right| \tag{A.1}$$

$$F(V) = \sum \alpha F(V)_{mn} \tag{A.2}$$

where $V[T_n]_{(x,y,z)}$ is the reference voltage at temperature T_n for design vector (x, y, z).

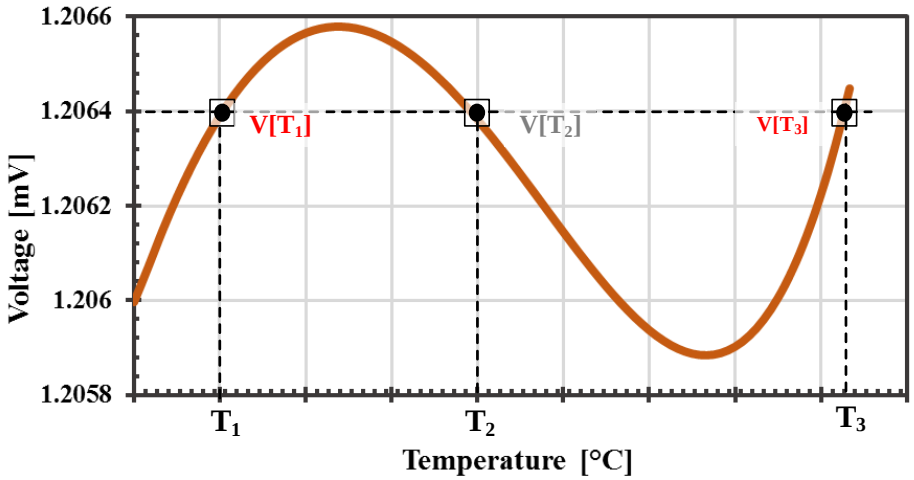


Figure 0.1: Calibration Concept

A.2 System Architecture

The system for the on chip calibration consist of analog blocks (temperature sensor, heater, performance metrics quantization and the bandgap reference) and digital blocks (finite state machine (FSM), and cost function). The temperature sensors are used to

measure the on chip temperature, heater is used for heating the chip and the digital circuit is used for the optimization base on the cost function and for changing the design variables of the bandgap reference. The block diagram of the proposed auto-calibration system is shown Figure A.2.

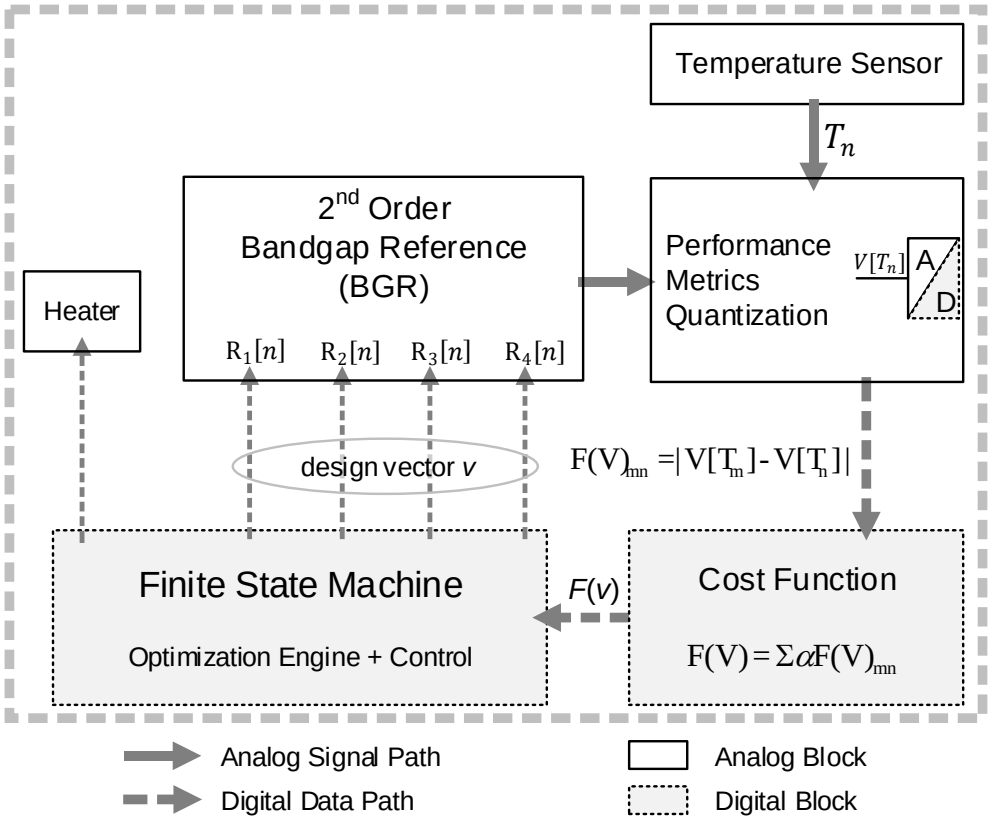


Figure 0.2: Block Diagram of the Proposed Auto-calibration Bandgap Reference System

A.2.1 Temperature sensor

The PTAT voltage source for the temperature sensor is based on reverse and forward MOS diode. This circuit has been used in the temperature sensor [46] and the bandgap voltage reference [42]. The PTAT voltage, from [46] is given by:

$$V_{PTAT} = mV_T \ln(N) \tag{A.3}$$

where $N = \frac{S_{MN1}}{S_{MN2}}$.

The op-amp is chopper stabilized to reduce the offset errors and minimized non-PTAT variations of PTAT voltage. A detail discussion of how the op-amp offset is eliminated is given in the next section. An averaging notch filter is used to remove the chopping ripple from the modulator of the chopped op-amp. Figure A.3 shows the temperature sensor schematic. The code output from the ADC is shown Figure A.4 and Figure A.5 shows the monte-carlo simulation for both VPTAT and it's slope.

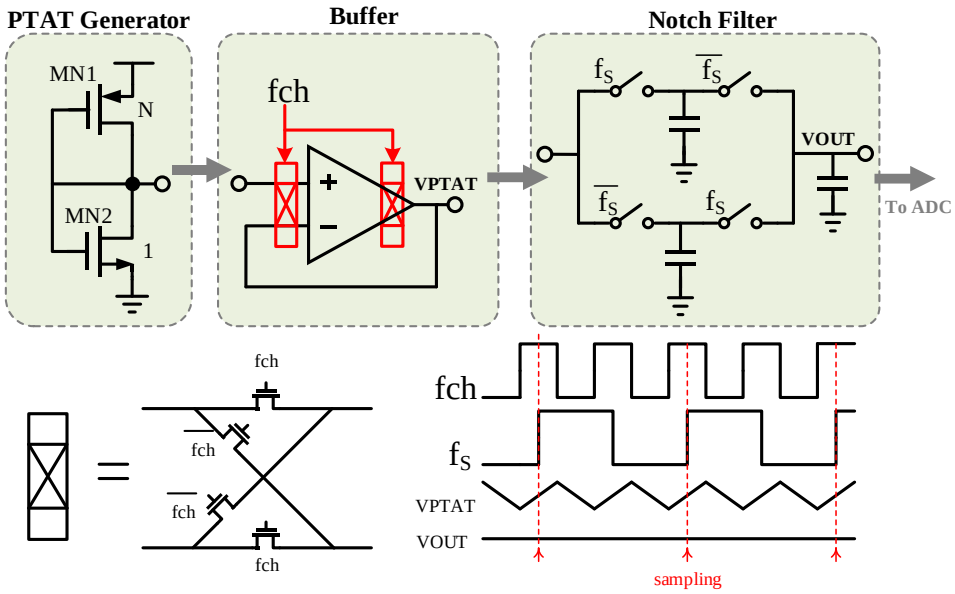


Figure 0.3: Temperature Sensor

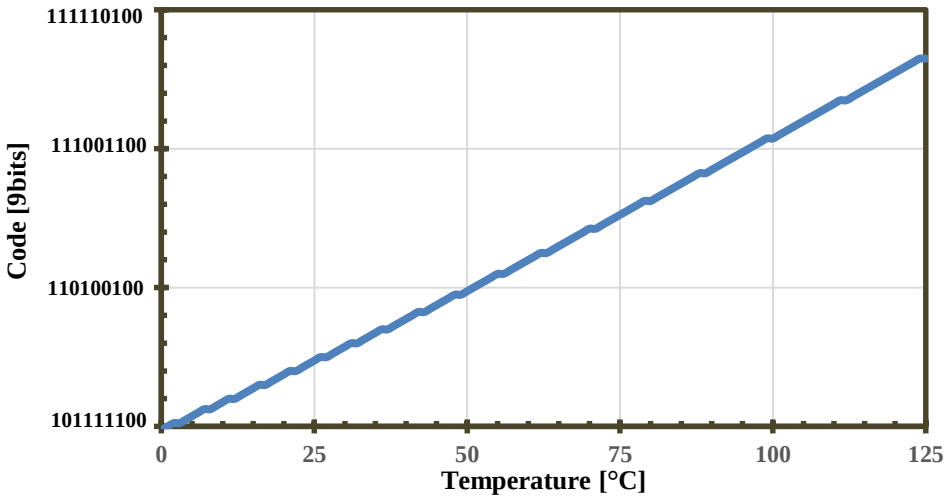
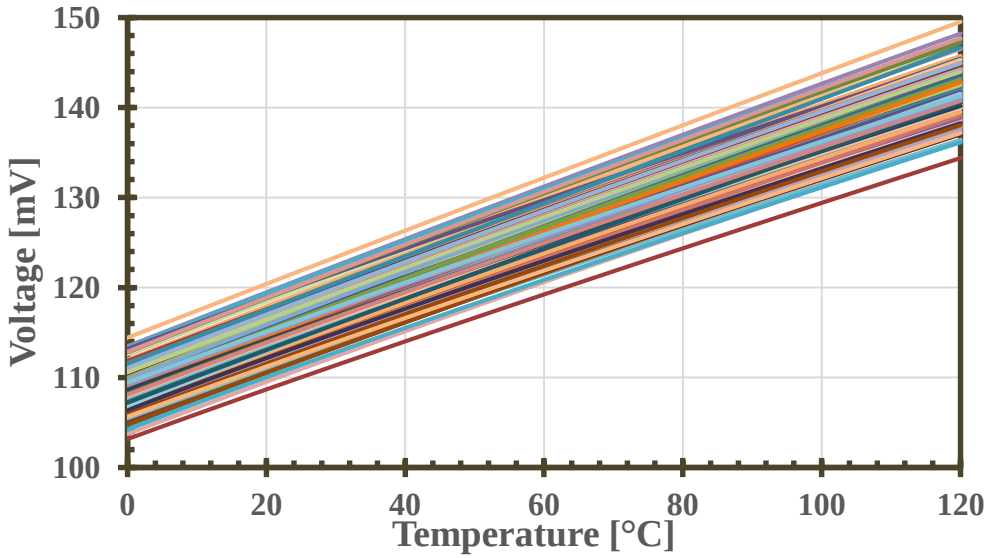


Figure 0.4: ADC Output Code vs. Temperature

a)



b)

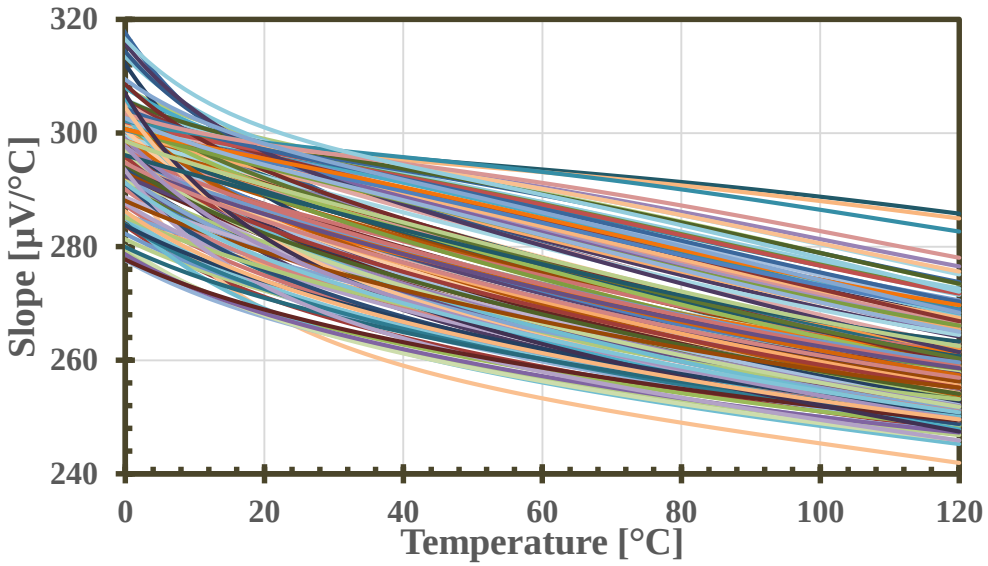


Figure 0.5: Monte-Carlo Simulation a) VPTAT and b) Slope of VPTAT

A.2.2 2nd Order Bandgap Voltage Reference

The reference used in circuit is a piece-wise 2nd order bandgap voltage reference circuit. The circuit uses chopper stabilization to cancel the opamp offset voltage. The chopping technique has better noise performance in comparison with auto-zeroing.

Curvature of Bandgap

The second order bandgap is shown in Figure A.6. The circuit is a first order voltage mode bandgap with added piece-wise nonlinear compensation. From Figure A.6,

$$I_0 = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{V_T}{R_1}\ln(n) \tag{A.4}$$

The output voltage V_{REF} is given by;

$$V_{REF} = V_{BE1} + I_0(2R_0 + R_3 + R_2) + I_{NL}(2R_0 + R_3) \tag{A.5}$$

$$V_{REF} = V_{BE1} + \alpha V_T + I_{NL}(2R_0 + R_3) \tag{A.6}$$

where $\alpha = \frac{1}{R_1}(2R_0 + R_3 + R_2)\ln(n)$ and I_{NL} is a nonlinear piece-wise current which is controlled by the PTAT voltage, I_4R_4.

The reference voltage, V_{REF}, is a first order bandgap reference for low temperature; the PTAT voltage αV_T is used to compensate the first order temperature dependence of V_{BE1} and the nonlinear temperature dependence term of V_{BE1} (see (2.4) in section 2.2) is compensated using the nonlinear voltage, $I_{NL}(2R_0 + R_3)$.

The PTAT voltage, I_4R_4, is used to control the turning on the transistor switches $MN3$ and $MN4$. The two switches are turned at high temperature to allow the current I_{NL} to flow. Depending on the value of R_4, the temperature at which the switches $MN3$ and $MN4$ are turned on can be varied; this results in the control of the 2nd order part of the bandgap output.

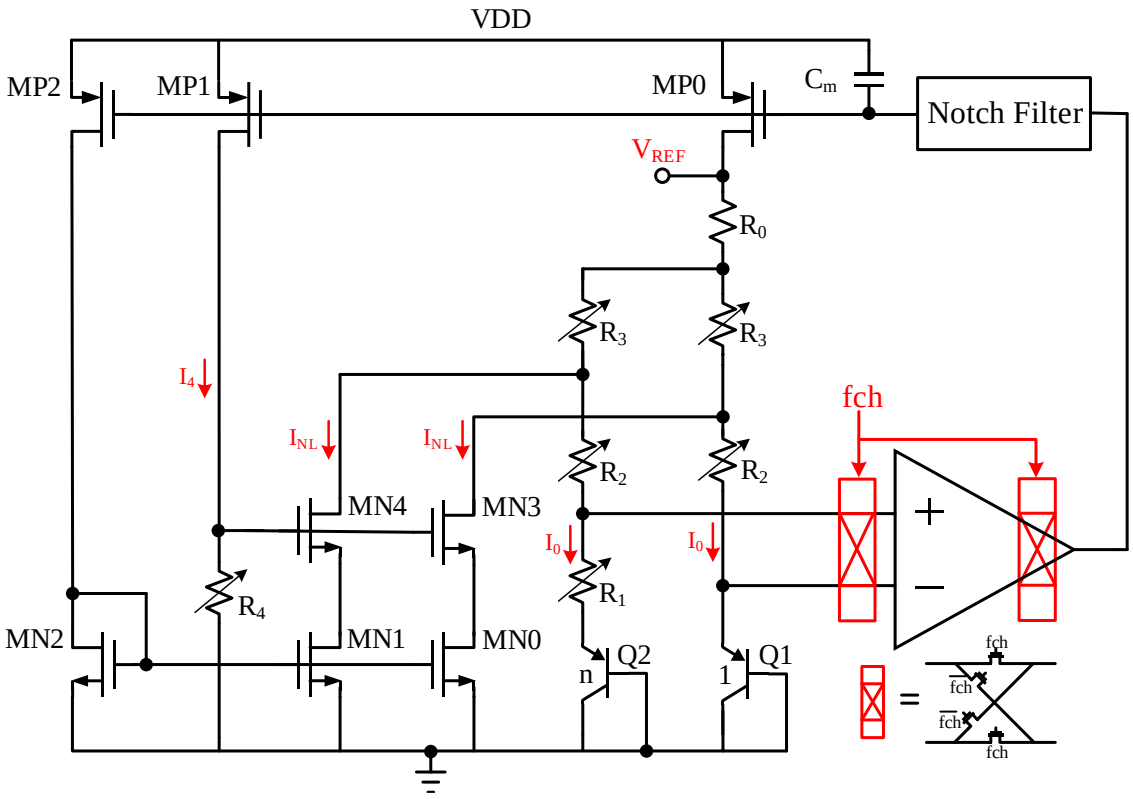


Figure 0.6: Piecewise Nonlinear 2nd Order Bandgap Reference

Figure A.7 shows how output, V_{REF}, is generated by combining the PTAT voltage (αV_T), $V_{BE1}$and the nonlinear voltage ($I_{NL}(2R_0 + R_3)$). The Figure A.7 also shows the resultant 2nd order V_{REF} curvature. From (A.6), the PTAT voltage is determined by the α

and hence can be change by varying the values of R_3 and R_2. This makes it possible to vary the low temperature curvature of V_{REF}. Also the non-linear voltage is determined by the value of I_{NL}, making it possible to change the high temperature curvature by varying the value of R_4 since I_{NL} is determined by the value of R_4. Hence, in the calibration process, the resistors R_4, R_3 and R_2 are used to optimize the bandgap curvature for given power level.

From (A.4) the current of the bandgap is determined by the value of resistor R_1 and hence the resistor R_1 is used set the current or power level. A copy of the current, I_0, is used to bias the op-amp.

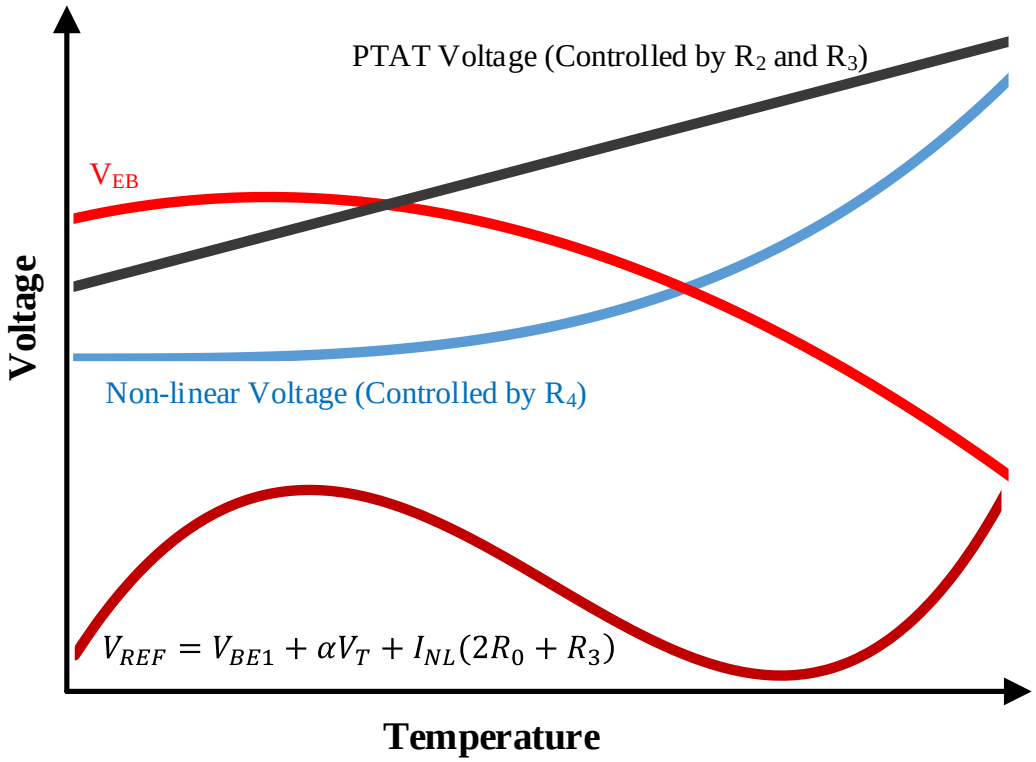


Figure 0.7: Curvature of Proposed 2nd Order Bandgap

Op-amp and offset Cancellation

From the Figure A.6, if the offset of the op-amp (V_{os}) is included the output of the reference would be;

$$V_{REF} = V_{BE1} + \alpha V_T + I_{NL}(2R_0 + R_3) + \left(1 + \frac{R_0 + R_3 + R_2}{R_1}\right) V_{os} \qquad \text{(A.7)}$$

The V_{os} has a nonlinear temperature dependence (Non-PTAT) and hence cannot be trimmed with the normal PTAT trimming. Typically, the error in the output of the bandgap associated with the op-amp offset can be several tens of mV since the offset of CMOS op-amps are usually in several mV and it's amplified by the closed loop gain, $1 + \frac{R_0+R_3+R_2}{R_1}$, as shown in (A.7).

A chopping scheme is used to minimize the offset of the op-amp and hence it's associated error on the bandgap output. A 75dB folded cascode op-amp, shown in Figure A.8, is used in the design of the bandgap. Since modulator $MD0$ and $MD1$ has a fully differential signal paths between them, the offset associated with the mismatch between $MP1 - MP2$ and $MN0 - MN1$ is completely eliminated. However, the inherent asymmetry of the low voltage cascode current mirror makes it difficult to completely remove the errors associated with $MP4 - MP5$ mismatch.

Considering the first phase (ϕ_1) of the chopping scheme, when $MP4$ and $MP5$ are connected to $MP6$ and $MP7$ respectively, the drain currents of $MP6$ and $MP7$ is;

$$I_{DMP6} = I_{DMP4} = \beta[V_{GSMP4} - V_{THMP4}]^2 \qquad \text{(A.8)}$$

$$I_{DMP7} = I_{DMP5} = \beta[V_{GSMP5} - V_{THMP5}]^2 \tag{A.9}$$

where $\beta = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{MP4,5}$

Taking note that $V_{GSMP4} = V_{GSMP5}$,

$$I_{DMP7}|_{\phi_1} = I_{DMP6} + \beta[V_{THMP4} - V_{THMP5}]^2 + 2\sqrt{\beta I_{DMP6}}[V_{THMP4} - V_{THMP5}] \tag{A.10}$$

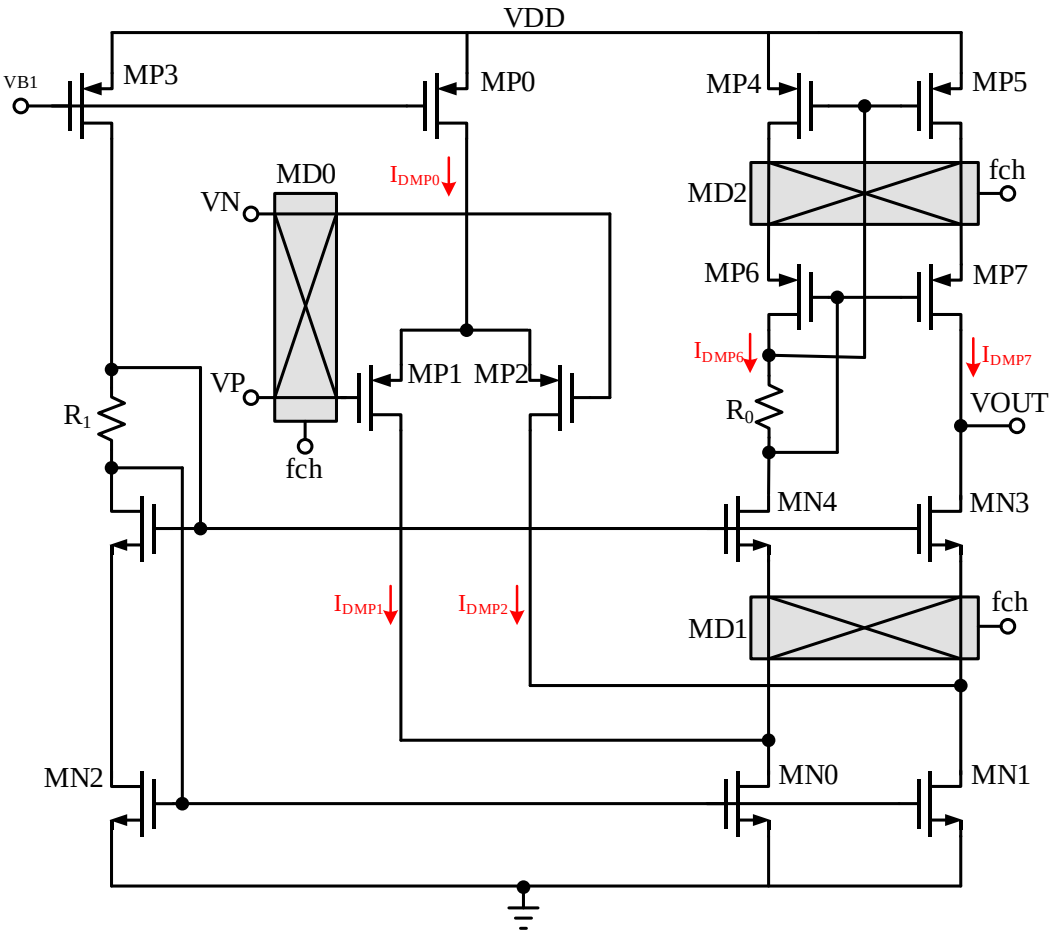


Figure 0.8: Folded Cascode Op-amp with Chopping Scheme

In the second phase (ϕ_2) since $MP4$ and $MP5$ are swapped;

$$I_{DMP7}|_{\phi_2} = I_{DMP6} + \beta[V_{THMP5} - V_{THMP4}]^2 + 2\sqrt{\beta I_{DMP6}}[V_{THMP5} - V_{THMP4}] \tag{A.11}$$

The remaining current mismatch is calculated as;

$$\Delta I_{DMP4,5} = \frac{I_{DMP7}|_{\phi_1} + I_{DMP7}|_{\phi_2}}{2} - I_{DMP6} = \beta \Delta V_{THMP4,5}^2 \tag{A.12}$$

The remaining offset is therefore given by;

$$V_{os} = \frac{\Delta I_{DMP4,5}}{g_{mMP1,2}} = \frac{\beta \Delta V_{THMP4,5}^2}{g_{mMP1,2}} = \frac{g_{mMP4,5}^2 \Delta V_{THMP4,5}^2}{4 g_{mMP1,2} I_{DMP4,5}} \tag{A.13}$$

where $\Delta V_{THMP4,5} = V_{THMP4} - V_{THMP5}$ and g_{mMx} is the transconductance of Mx.

The op-amp offset needs to be less than 50 µV in order to achieved high precision reference (less than 1% variation). This can be done by making sure that $\Delta V_{THMP4,5}$ is less than 5 mV.

The modulator switching signal is a non-overlapping clock phase 1 (ϕ_1) and phase 2 (ϕ_2) shown in Figure A.9. An averaging notch filter is used filter the chopping ripple. The continuous time sample and hold operation allows for the notch filter to behave like band stop filter at the chopping frequency.

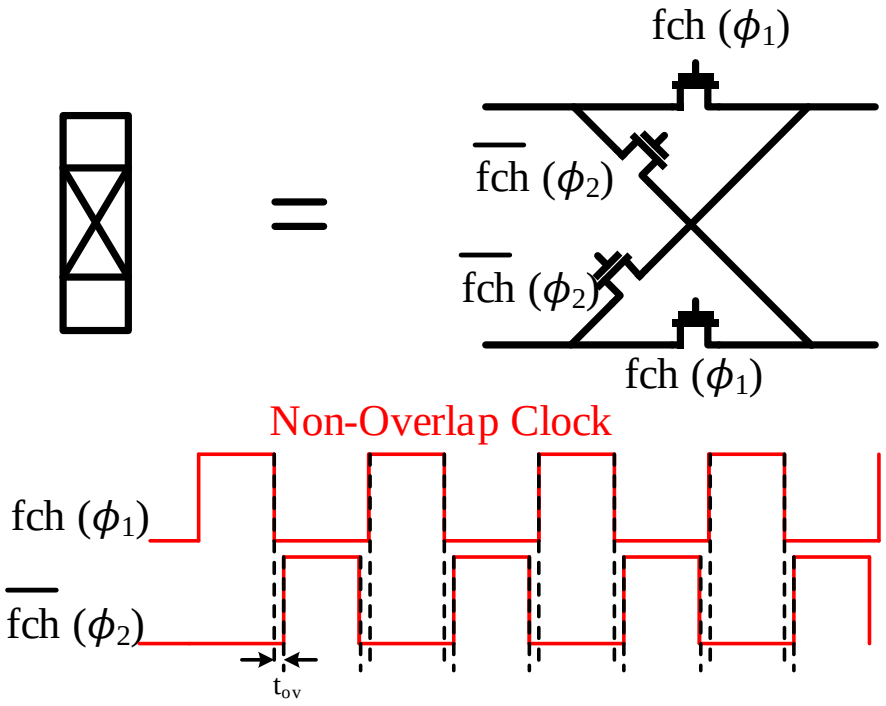


Figure 0.9: Modular and Non-overlap Clock

Bandgap Simulation Results

The simulated bandgap output voltage for both when the chopper is active and when the chopper is off for a 0 °C – 125 °C temperature range is shown in Figure A.10. The temperature coefficient is 4.3 ppm and 4.6 ppm for the chopper being on and off respectively. The low frequency noise is reduce by about 20 times with the chopper active as shown in the Figure A.11.

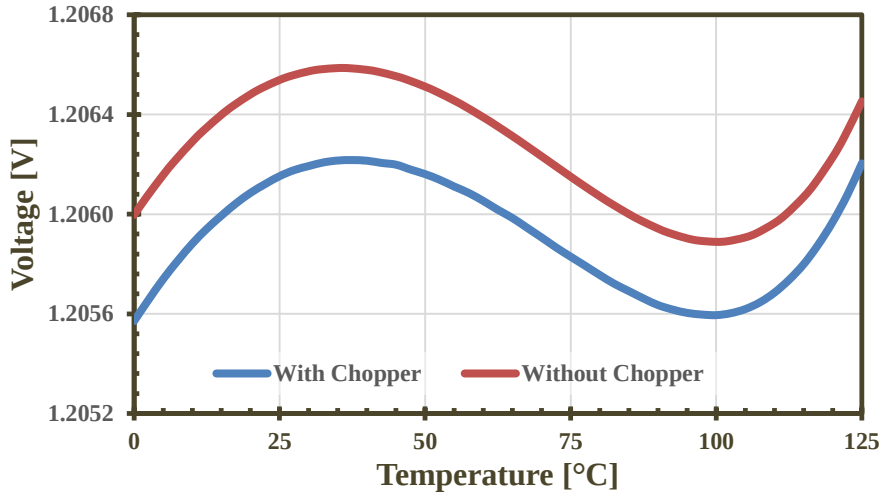


Figure 0.10: Temperature Dependence of 2nd Order BGR Output Voltage

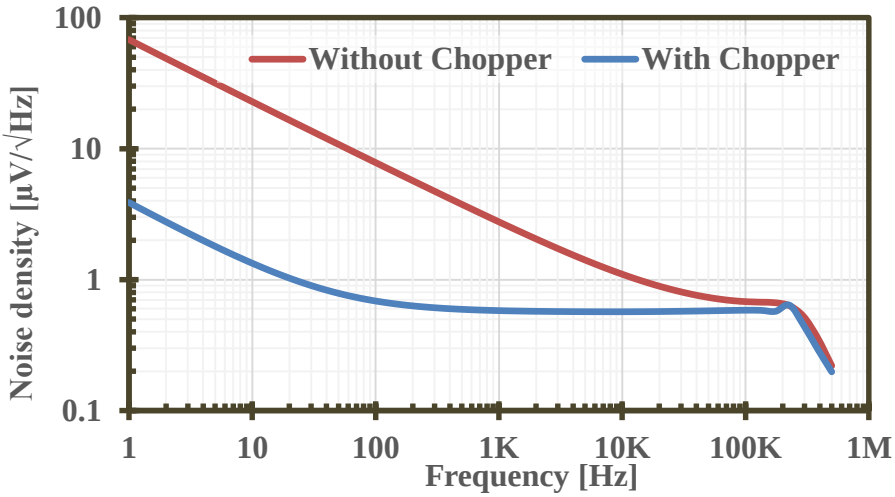


Figure 0.11: Noise Spectrum of V_{REF} from 1 Hz to 500 kHz

Since the non PTAT offset voltage of the Op-amp is substantially reduce by the chopping, the variation of the output reference voltage due to mismatches is drastically reduce as shown by the Monte Carlo simulation results in Figure A.12. The 3σ variation

of the reference voltage at room temperature is 4.4 % and 0.33% for without and with the chopper active.

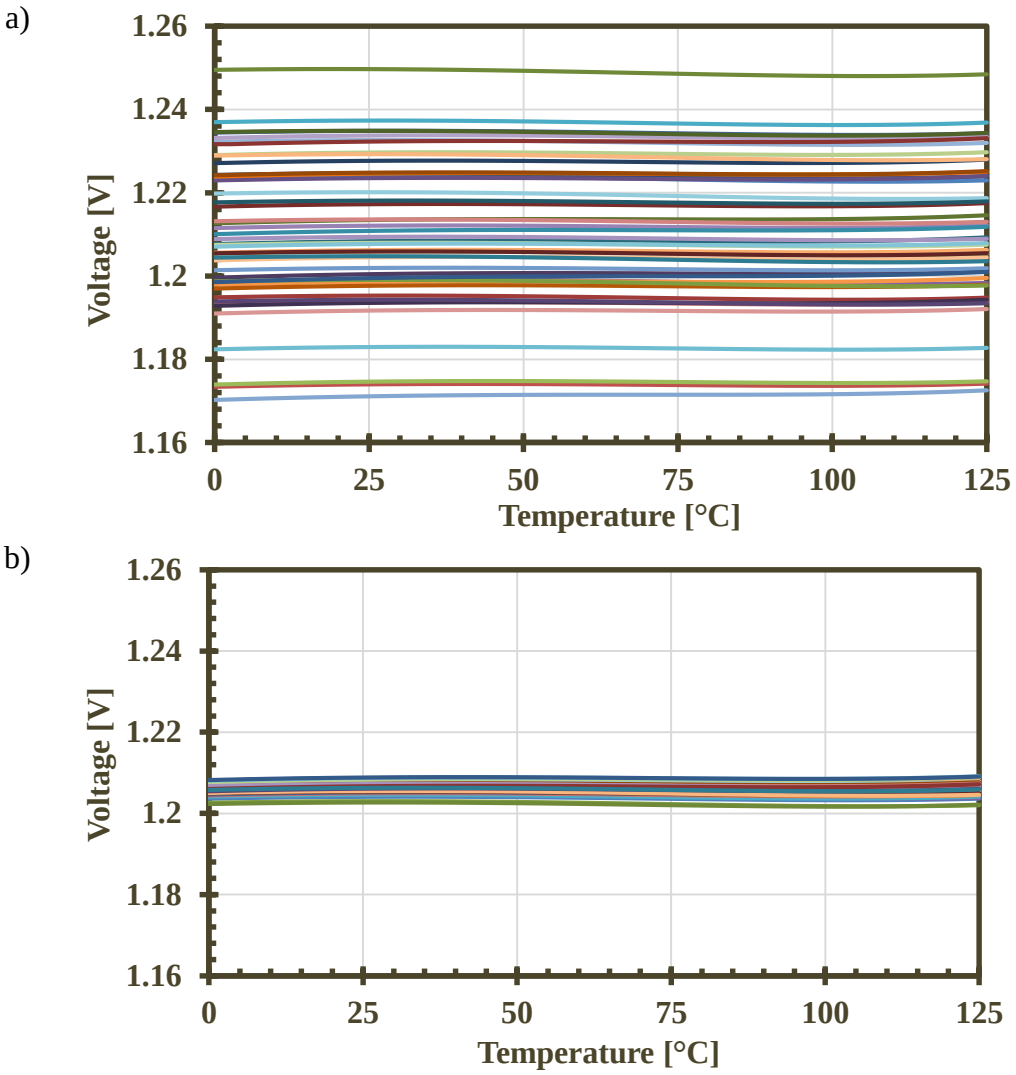


Figure 0.12: Monte Carlo Simulation a) Without Chopper and b) With Chopper

A.2.3 Heater

The heater is a P+ polysilicon resistor based heating element. The heater is design for a power 150mW, at a 3 V supply. The supply for the heater is separated from the main chip supply. From [47], [48], the temperature (T) decreases with distance, L, from the heater as function given below:

$$T = T_0 + \beta P_R \left(\frac{1}{L}\right) \tag{A.14}$$

where β is a constant of 1.26 with unit Kμm/mW, T_0 is the temperature in kelvin (K) at $L = \infty$ and P_R is the power dissipation by the heater.

From the experimental data of [47], [48], the temperature decreases swiftly with distance, L, and saturates at 100μm independent of the power of the heater. Hence, three (3) temperature sensors are place at a distance of 100μm, 125μm, and 150μm and the actual bandgap reference is place at 175μm from the each of the four (4) heaters to avoid a temperature gradient on the bandgap as shown in Figure A.13.

A.2.4 Calibration and Optimization Scheme

The calibration of the bandgap reference is achieved by sampling the reference voltage at three (3) different temperatures and calibrating the reference voltage curvature in two main steps: by first optimizing the low temperature first order curvature and then adjusting the second order high temperature curvature to achieve the best temperature drift performance.

The reference voltage is sampled at T_1, T_2, and T_3 which is 20 °C, 60 °C and 120 °C in this design. Since the first order curvature is affected only by R_3 and R_2, the sampling at temperature T_1, and T_2 is done by varying R_3 and R_2 with all other resistors fixed.

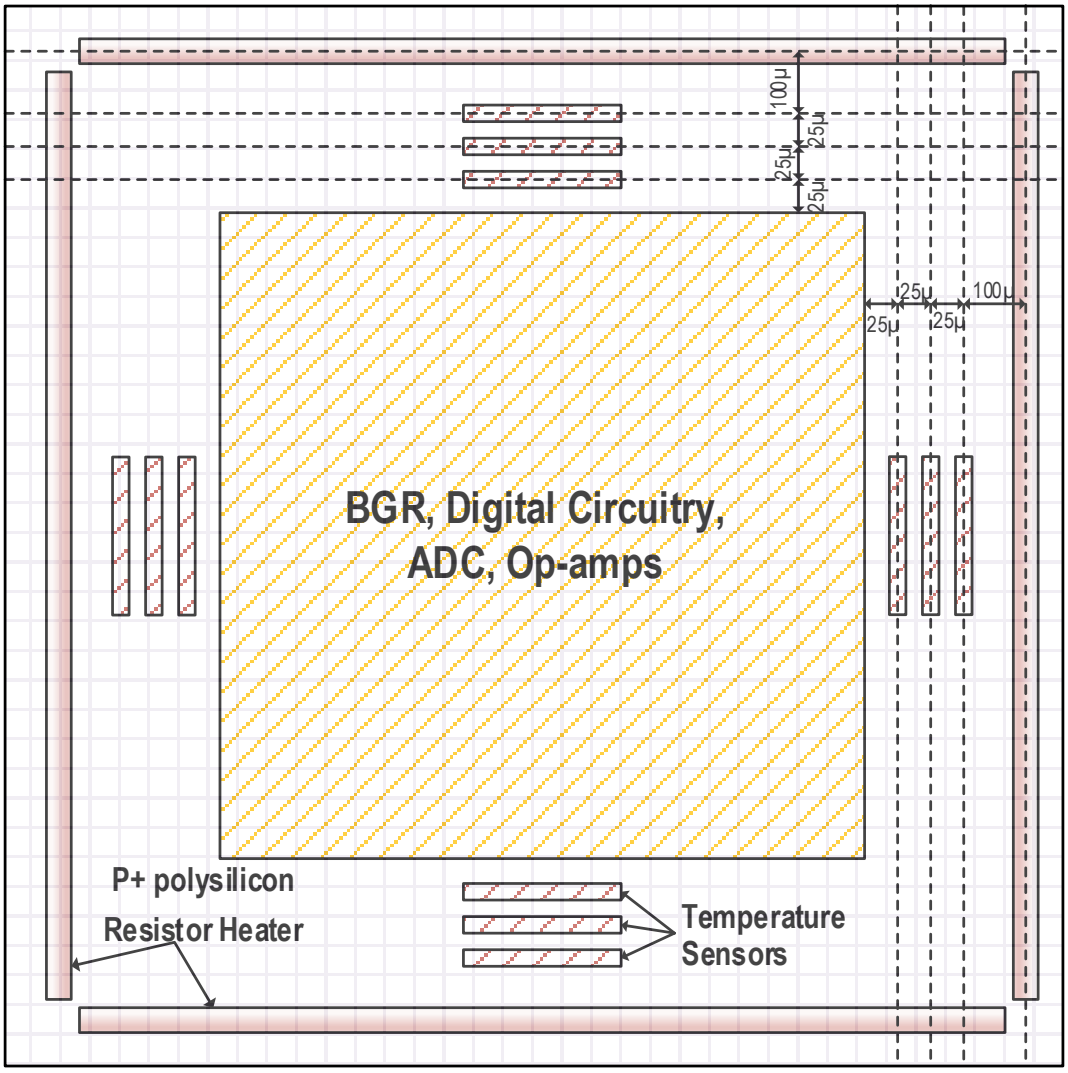


Figure 0.13: Chip Floor Plan which has 12 Sensors and 4 Heaters

This results in 1024 samples since R_3 and R_2 are both 5 bit each. Figure A.14 shows a flowchart for the sampling of the reference voltage at T_1, and T_2. An optimized first order curvature is achieved by searching for the R_3 and R_2 values that gives the minimum value of $F(V)_{12}|_{(x,y,z)}$ in the expression below:

$$F(V)_{12}|_{(x,y)} = \left|V[T_1]_{(x,y)} - V[T_2]_{(x,y)}\right| \tag{A.15}$$

where x, and y represents the design vectors for R_2, and R_3 respectively and $V[T_1]_{(x,y)}$ is the reference voltage at temperature T_1 for design variable vector (x, y).

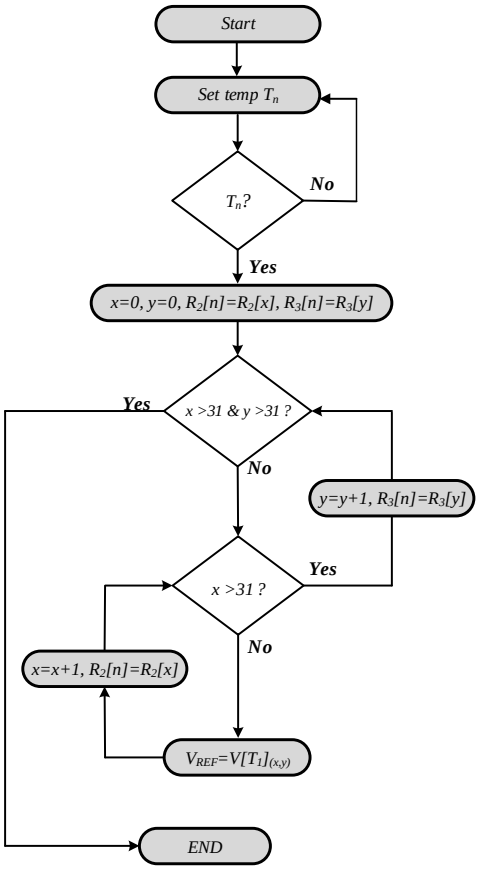


Figure 0.14: Flowchart for Reference Voltage Sampling

$F(V)_{12}$ Contour as well as the optimal solution (x, y) of the calibration engine is shown in Figure A.15. The R_2, and R_3 are set using the optimal design vector solution, (x, y).

The next is to optimize the higher temperature curvature. This is achieved by sampling the reference voltage at T_2, and T_3, while varying the R_4 and keeping the R_2, and R_3 set at their optimal solution. The best 2nd order curvature is obtained by finding the value of R_4 that results in a smallest value of $F(V)_{23}|_{(x,y,z)}$ in the equation below:

$$F(V)_{23}|_{(x,y,z)} = \left|V[T_1]_{(x,y,z)} - V[T_2]_{(x,y,z)}\right| \quad \text{(A.16)}$$

where x, y and z represents the design vectors for R_2, R_3 and R_4 respectively and $V[T_1]_{(x,y,z)}$ is the reference voltage at temperature T_1 for design variable vector (x, y, z). $F(V)_{23}$ Contour as well as the optimal solution (x, y, z) of the calibration engine is shown in Figure A.16. The R_2, R_3 and R_4 are set using the optimal design vector solution, (x, y, z).

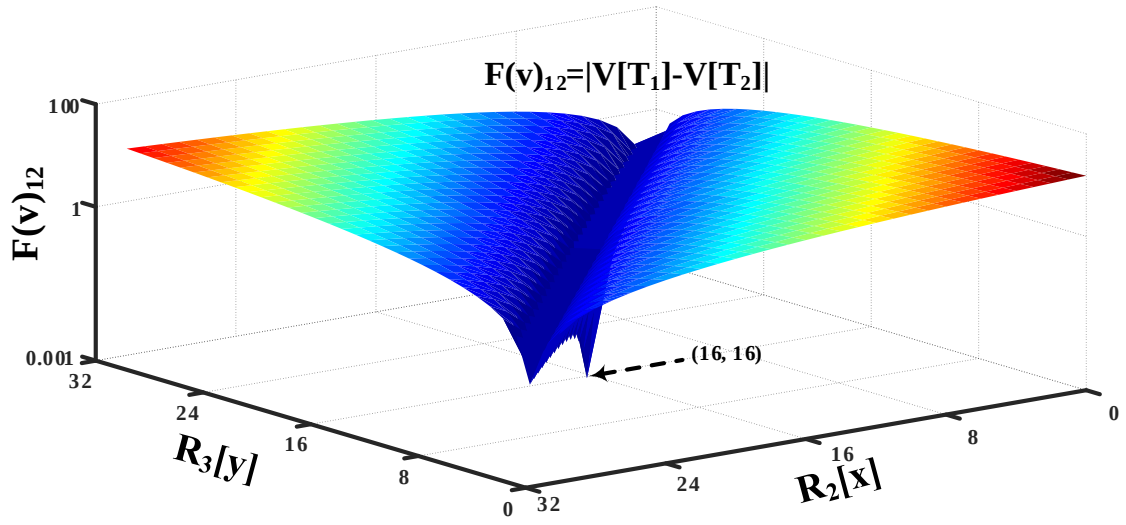


Figure 0.15: $F(V)_{12}$ Contour as well as the Optimal Solution (x,y) of the Calibration Engine

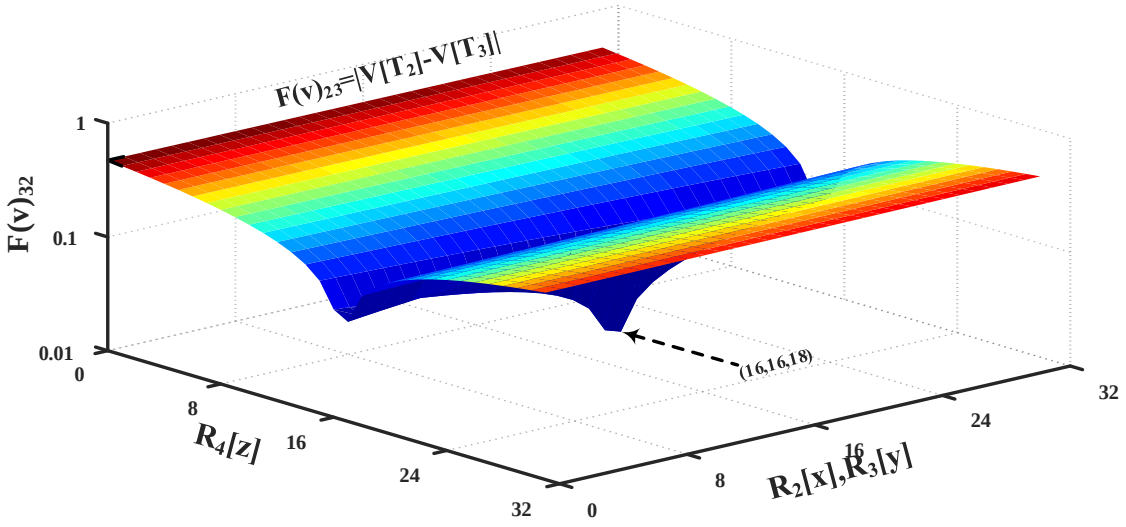


Figure 0.16: $F(V)_{23}$ Contour as well as the Optimal Solution (x,y,z) of the Calibration Engine