ULTRA-LOW POWER TRANSMITTER AND POWER MANAGEMENT FOR

INTERNET-OF-THINGS DEVICES

A Dissertation

by

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ABSTRACT

Two of the most critical components in an Internet-of-Things (IoT) sensing and transmitting node are the power management unit (PMU) and the wireless transmitter (Tx). The desire for longer intervals between battery replacements or a completely self-contained, battery-less operation via energy harvesting transducers and circuits in IoT nodes demands highly efficient integrated circuits. This dissertation addresses the challenge of designing and implementing power management and Tx circuits with ultra-low power consumption to enable such efficient operation.

The first part of the dissertation focuses on the study and design of power management circuits for IoT nodes. This opening portion elaborates on two different areas of the power management field: Firstly, a low-complexity, SPICE-based model for general low dropout (LDO) regulators is demonstrated. The model aims to reduce the stress and computation times in the final stages of simulation and verification of Systems-on-Chip (SoC), including IoT nodes, that employ large numbers of LDOs. Secondly, the implementation of an efficient PMU for an energy harvesting system based on a thermoelectric generator transducer is discussed. The PMU includes a first-in-its-class LDO with programmable supply noise rejection for localized improvement in the suppression.

The second part of the dissertation addresses the challenge of designing an ultra-low power wireless FSK Tx in the 900 MHz ISM band. To reduce the power consumption

and boost the Tx energy efficiency, a novel delay cell exploiting current reuse is used in a ring-oscillator employed as the local oscillator generator scheme. In combination with an edge-combiner PA, the Tx showed a measured energy efficiency of 0.2 nJ/bit and a normalized energy efficiency of 3.1 nJ/(bit·mW) when operating at output power levels up to -10 dBm and data rates of 3 Mbps. To close this dissertation, the implementation of a supply-noise tolerant BiCMOS ring-oscillator is discussed. The combination of a passive, high-pass feedforward path from the supply to critical nodes in the selected delay cell and a low cost LDO allow the oscillator to exhibit power supply noise rejection levels better than −33 dB in experimental results.

DEDICATION

Para Mariana, que creyó en mi, caminó a mi lado y me levantó en cada caída durante esta aventura sin pedirme nada a cambio.

Para Jacobo, que me quitó todos mis miedos cuando me sonrió.

Para mis padres, Jorge y Silvia, quiénes me enseñaron con su ejemplo que nada es inalcanzable.

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CHAPTER I

INTRODUCTION

1.1   The Internet-of-Things (IoT)

The origins of the Internet-of-Things (IoT) can be traced back to 1999 when the Auto-ID research group in the Massachusetts Institute of Technology (MIT) was exploring the application of networked radio identification (RFID) systems to the then emerging sensing technologies [1, 2]. However, accepting the definition of the IoT conception as *"the point in time when more things or objects were connected to the Internet than people"* [1], the Cisco Internet Business Solutions Group (IBSG) concluded that the IoT emerged between 2008 and 2009. A massive IoT network, expected to accommodate more than 50 billion devices by 2020 [1], will (and to some extent, already is) enable the exchange of information and communication of all the things and individuals connected [3], which when coupled with efficient sensing technologies, offers an endless pool of possibilities. As such, the IoT platform has already triggered the development of multiple and diverse applications in a variety of fields such as: healthcare, wearable technology, logistics, smart homes and buildings, and smart infrastructure for smart cities, to mention a few. Illustrated in Fig. 1 is an example of the potential communications links established by all the "things" part of the IoT. Multiple wireline and wireless network standards such as Bluetooth, ZigBee, Ethernet, and of course cellular technology (4G/5G), can be used to ultimately reach the Internet cloud where the bulk of the data storage is done.

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Because of the variety of technologies converging into the IoT, the characteristics and requirements of every node and gateway are vastly different. However, there are similarities in the sense that most of the nodes require some sort of sensing but particular levels of processing power; also, every node needs to be able to transmit information but an embedded receiver might be optional in some cases. Furthermore, every node and gateway share the fundamental requirement of a local power supply, which might be in the form of an AC power outlet, a battery, or an energy harvesting system. A collection of such nodes forms what is known as wireless sensor networks (WSN). A WSN might expand over different spaces, at the personal or body-area levels. Fig. 1 also shows small examples of the so-called PAN (personal area network) and BAN (body area network) within the IoT network context.
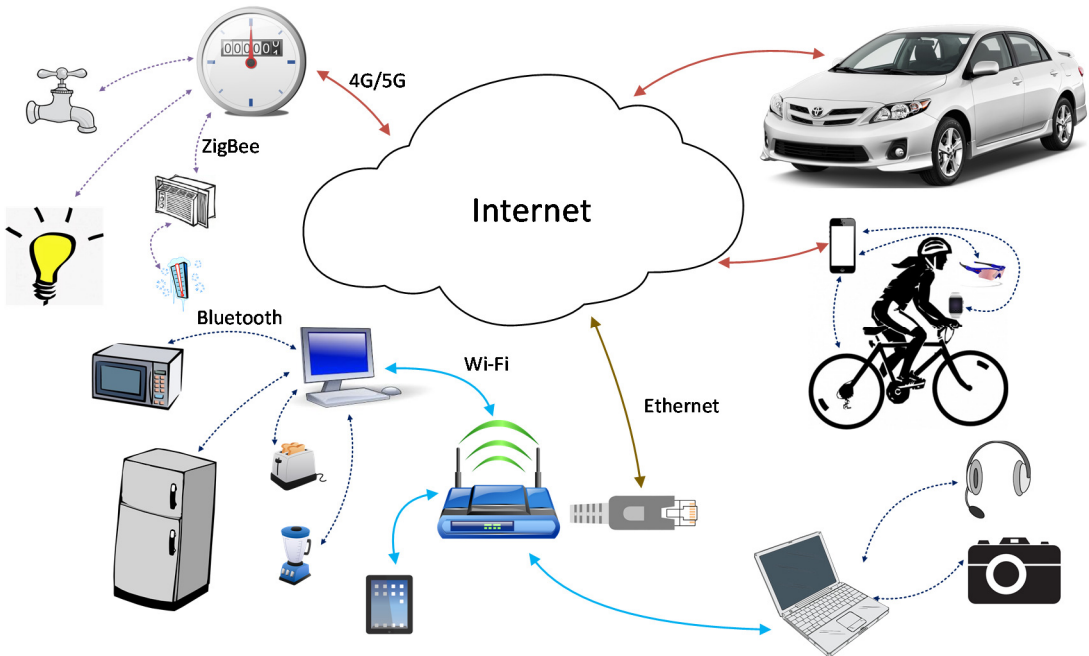
Fig. 1. Internet-of-Things network diagram example.

1.2 Inside an IoT node

A general, conceptual description of the blocks typically incorporated in a WSN/IoT node is shown in Fig. 2. The node can have a single or multiple energy sources, which might include: an AC outlet for stationary nodes located in areas with utility services; a rechargeable or disposable battery; a naturally available resource in the environment such as sun light, temperature gradients, and electromagnetic waves; an induced source such as vibrational energy; or alternative energy sources such as methanol.
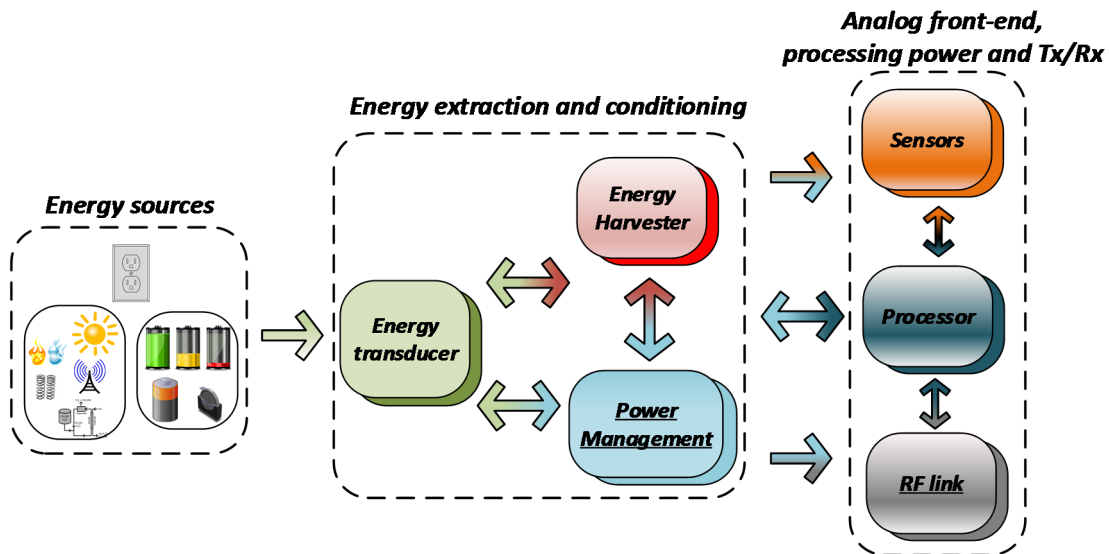
Fig. 2. Wireless sensor network/IoT node description.

For the electronic circuits in the node to operate using energy from whatever source is available, this energy must be in the form of an electric potential (voltage). An energy transducer is used to transform from one type of energy to another. Some examples

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of commonly used transducers are shown in Fig. 3, and include: a solar cell that converts incident sun light into a voltage; a thermoelectric generator that uses a temperature gradient between its plates to produce electrical energy; a piezoelectric device that generates a voltage when deformed (stressed) by external forces; a resistively-terminated antenna that converts electromagnetic waves at radio frequencies (RF) into an AC voltage; and a methanol fuel cell, where a chemical reaction generates a voltage between anode and cathode of the fuel cell. Although strictly speaking transformer-rectifier pair is not an energy transducer, these elements are required for AC-to-DC conversion when power is directly obtained from the power mains. On the other hand, while a battery is a transducer in itself (stacked electrochemical cells transforming chemical into electrical energy), when batteries are the primary energy source, some power conditioning is still required before the battery voltage reaches the circuits that perform the actual sensing, processing and transmitting/receiving tasks.
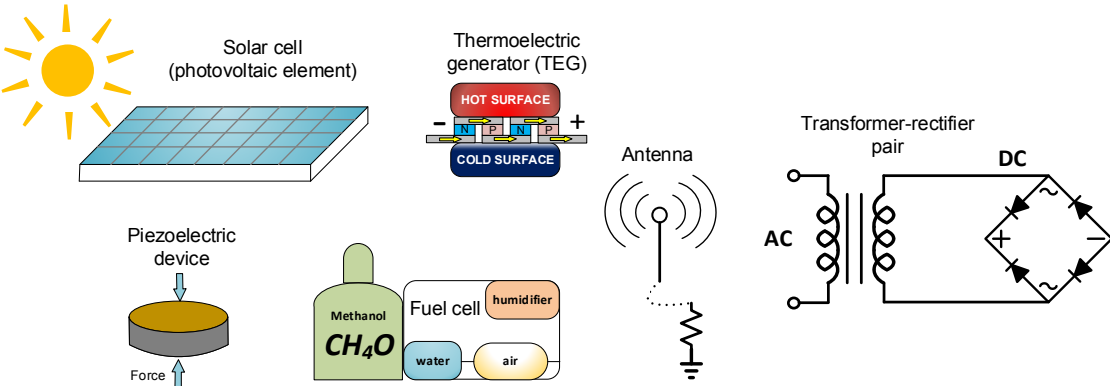
Fig. 3. Examples of energy transducer and a transformer-rectifier for AC-DC voltage conversion.

After the energy has been converter to the required –voltage– form, an energy harvester circuit is employed to extract the maximum amount of power (energy per unit time) from the energy transducer in the most efficient way. Simple circuits such as inductor-based DC-DC converters, RF rectifiers, and charge pumps are commonly used for this purpose [4-6]. Some examples of these type of circuits are shown in Fig. 4. After maximum energy extraction is guaranteed, additional power management and conditioning is required to properly scale the voltage levels, minimize supply noise, and regulate the provided output voltage. Additional switching converters or linear regulators are employed for this last step before delivering a clean supply for the sensitive circuits that form the IoT node. A conceptual block diagram of the energy extraction and conditioning chain is shown in Fig. 5.
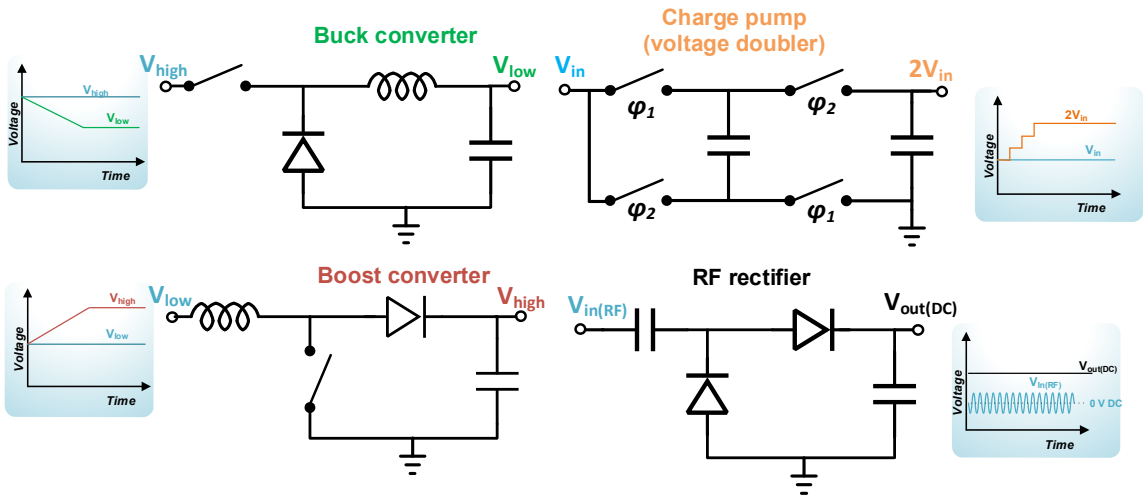
Fig. 4. Examples of circuits for efficient energy extraction from the transducer.

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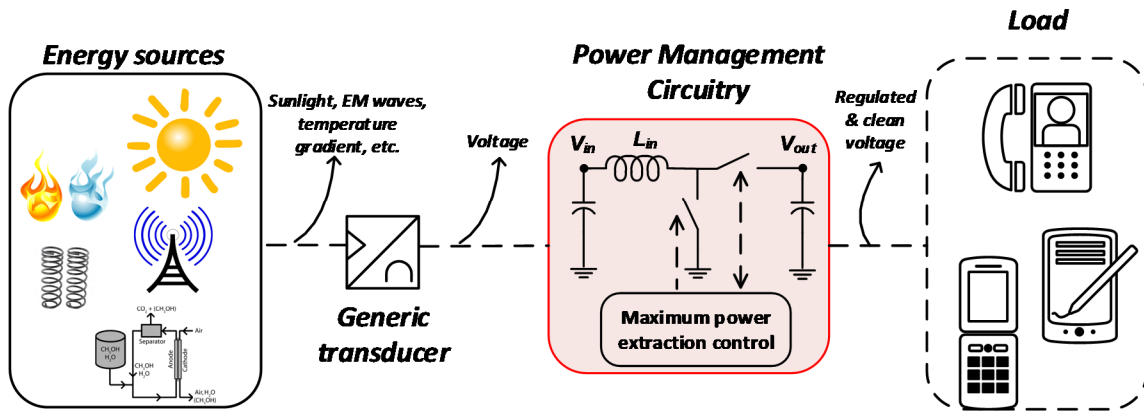
Fig. 5. Conceptual diagram of the energy extraction and conditioning chain.

The bulk of the work performed in an IoT node, as perceived by the end-user, is carried in the section that implements the sensing activities, provides the processing power and enables the communication link with the network gateway or with peer nodes. The sensors block primarily determines the application in which the node will be used. Temperature and humidity sensors embedded in the node enable climate monitoring and control; similarly, heart rate and bioimpedance sensors combined with accelerometers are the foundation of fitness monitors. The plethora of available sensors with different accuracies and sensitivities is part of the reason for the limitless potential of WSN.

An analog readout front-end used to acquire sensor's signals is shown in Fig. 6 [7]. It consists of a low noise, low power amplifier with variable gain (A); a low speed, low noise, and high resolution analog-to-digital converter (ADC) frequently based on the successive approximation architecture (SAR); bias and clock generators; a digital logic block; and a serializer output block.

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Analog front-end readout circuit
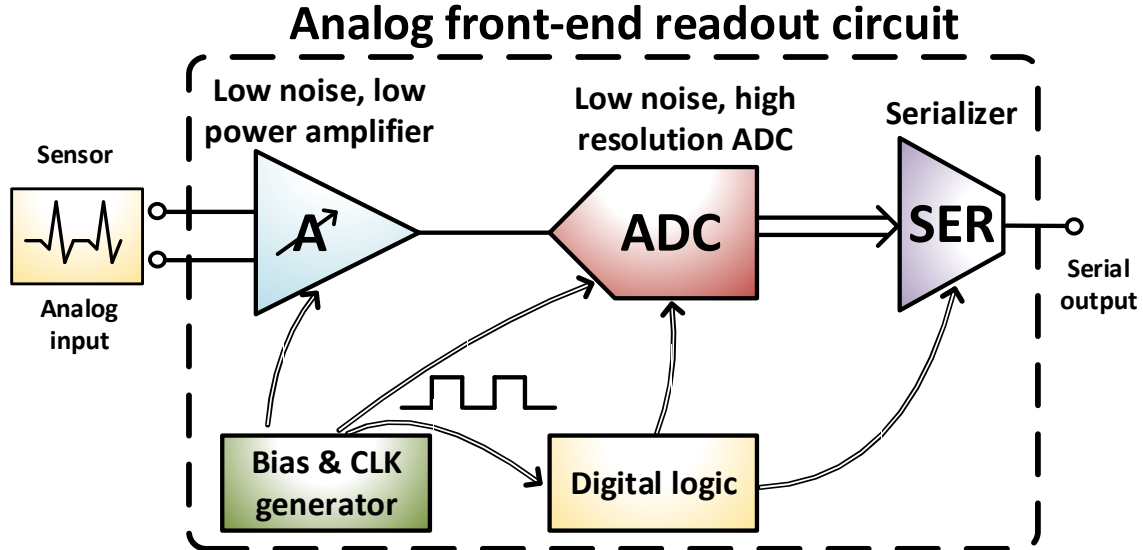
Fig. 6. Typical circuit blocks used in the analog front-end for sensor signal readout and acquisition.

Equally important for a pleasant user experience is the processor that executes, oversees, and coordinates the operation of the IoT node. The amount of processing power required per node greatly varies according to the application. For instance, nodes exclusively dedicated to monitor certain variable (water flow, energy consumption, etc.) and transmit its value at regular time intervals require a minimum of processing power which might be addressed with a simple finite state machine (FSM). Conversely, nodes that *i)* handle larger volumes of information, *ii)* perform complex operations on the acquired measurement before transmitting it, or *iii)* need to display it on a screen in a user-friendly mode, rely heavier on fast and powerful integrated processor. An easily identifiable node falling in the latter category is a smartphone. Furthermore, processors for mobile applications not only strive for high performance but also compete to achieve the lowest power consumption for long battery life. Examples include families of multi-

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core processors such as Samsung's Exynos, Qualcomm's Snapdragon, Apple's A4-9, some of which (Samsung & Qualcomm) already integrate the wireless radios. Based on the manufacturer's features description of the Snapdragon processor [8], a top level block diagram is depicted in Fig. 7.

4G LTE & Wi-Fi wireless radios	Graphics processor
Camera control	Multimedia/graphics accelerator
Display/LCD control	
GPS-Location unit	Sensors engine
Central processing unit	Multimedia processor
	Security/authentication circuits
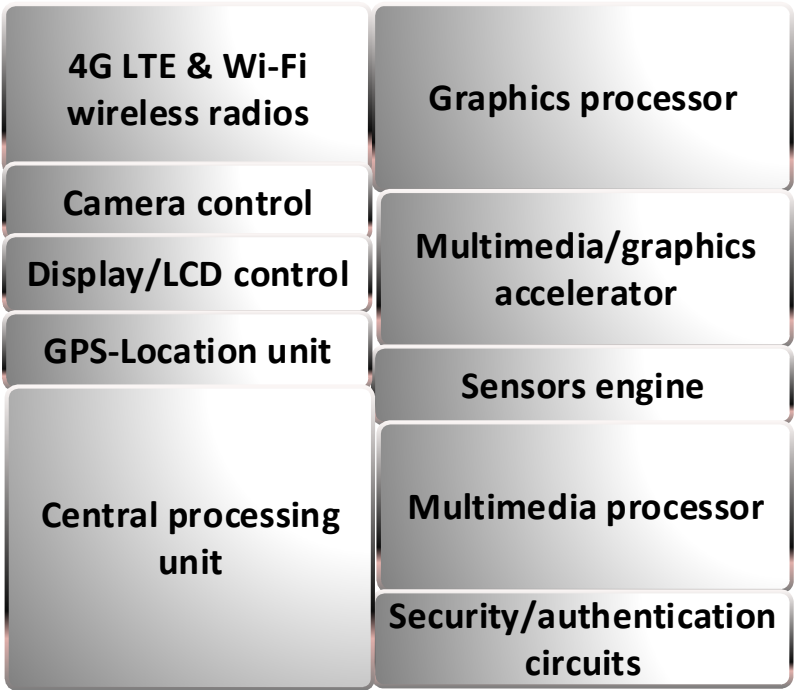
Fig. 7. Snapdragon's conceptual block diagram [8].

The last block element illustrated in Fig. 2 is the one in charge of the RF communication link. As illustrated in Fig. 1, there are several standards which can be used to establish a wireless channel. While LTE (cellular), Wi-Fi (IEEE 802.11b/g/n), Bluetooth (and its Low-Energy version –BLE–), ZigBee (IEEE 802.15.4) are amongst the most used standards, some other recently released standards focused on power

optimization like IEEE 802.15.6 for wireless body area networks (WBAN), 6LoWPAN (IPv6 over low power personal area networks), and proprietary protocols in the sub-1 GHz ISM (industrial, scientific, and medical) frequency bands are gaining important traction to achieve the lowest possible power consumption on the IoT node during data transmission and reception.

1.3   Research scope and motivation

This dissertation focuses on low and ultra-low power integrated circuits for IoT nodes targeting sensing and monitoring tasks for immediate transmission of raw (unprocessed) data results. In particular, the design and implementation of models and integrated circuits for the two underlined blocks in Fig. 2 are addressed. The next few chapters present and discuss in detail novel models, circuits and techniques for the power management and the RF (up)-link sections in IoT nodes. In order to provide context and understand the importance, motivation, and driving factors of this research, the rest of this chapter briefly touches on the problems that the integrated circuits here proposed aim to solve. The different building blocks that will be discussed throughout the dissertation are highlighted in Fig. 8 as key elements in the performance of an IoT node. The design and implementation of critical circuits such as switching and linear voltage regulators for power management (chapter 3), and its modeling (chapter 2); as well as local oscillators (LO) and power amplifiers for the wireless gateway part (chapter 4 and 5) are thoroughly discussed.

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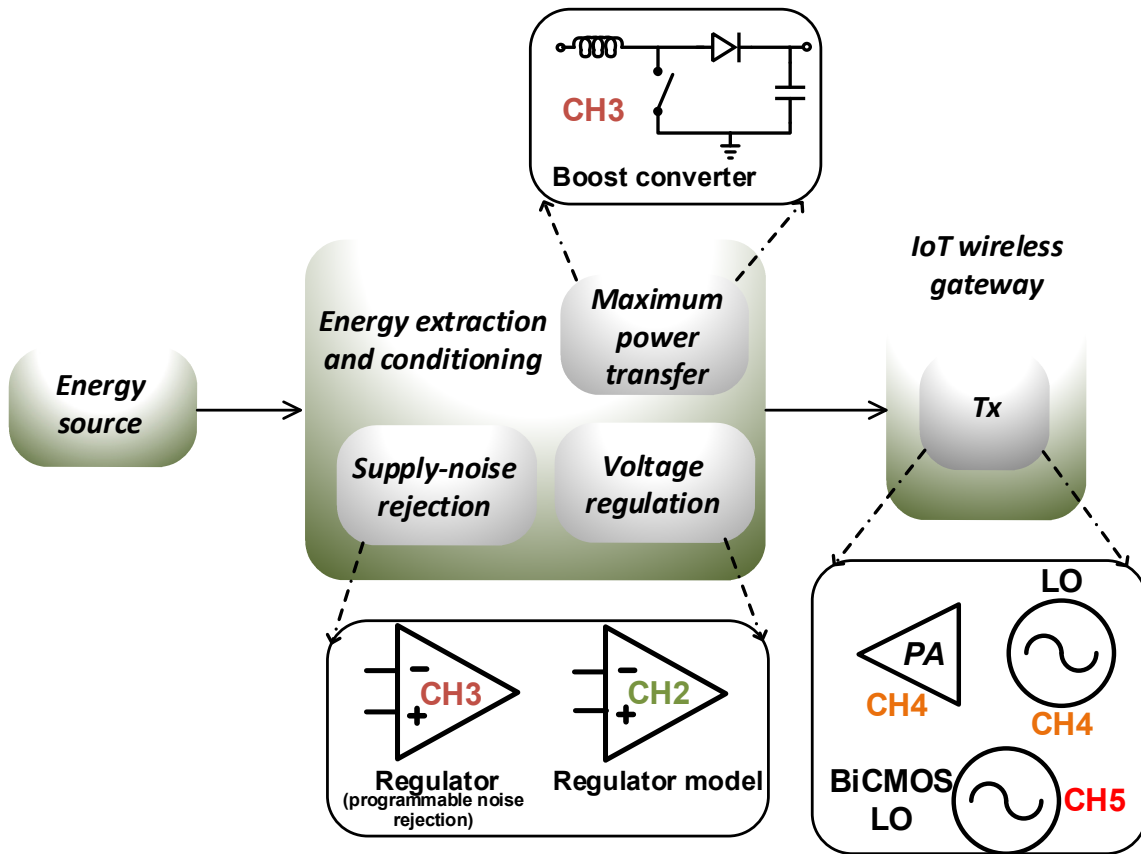
Fig. 8. Building blocks of an IoT node addressed in the dissertation.

An important part of every power management unit (PMU) used to provide supply voltage(s) for the operation of the brain (processor) of every System-on-Chip (SoC) like an IoT node, are the low dropout (LDO) regulators used to develop and deliver clean and regulated output voltages for the rest of the circuitry. However, as the number of LDOs per SoC increases, so does the complexity and time required to perform a reliable verification for the complete SoC at the transistor-level. To reduce the burden imposed on the simulators, chapter II describes a methodology to generate an LDO model that can be used to replace its transistor-level counterpart in top level SoC final simulations and verification. The proposed model is exclusively based on SPICE primitive components

which provides the required flexibility when dealing with excessively long top level netlists. Using the LDO model, it is demonstrated via simulation that important time reductions are achieved without significant loss in accuracy.

Chapter III digs further into the complete PMU circuitry. In this case, an integrated circuit is designed, fabricated and tested to demonstrate an end-to-end energy harvesting concept using a thermoelectric generator array as energy transducer. The proposed solution tackles several important problems in PMU: *a)* achieve high efficiency and continuous maximum power extraction, *b)* adapt to diverse conditions presented at the transducer output such as array reconfigurations triggered by different needs of the load circuit or by a varying temperature gradient within the target range, *c)* provide a well-regulated output voltage, and *d)* maintain *a), b)* and *c)* while providing high supply noise rejection, particularly at the PMU switching frequency. Although it might be argued that conditions *a)-d)* are typically expected from a high performance PMU, building a PMU targeted for an energy-harvest-powered IoT node poses tough challenges both at the architectural and circuit-levels to accomplish the PMU specifications under severe power consumption restrictions. In the presented scenario, the PMU must operate with extremely low power levels to avoid an important efficiency degradation. The proposed PMU was fabricated in 0.5 μm CMOS, experimental results showed overall system efficiency better than 57% @ 1.6 V output voltage, and a switching noise suppression in the supply of 40dB at the switching frequency. Furthermore, the PMU includes a first-of-its-kind, capacitor-less LDO with adaptive power supply transfer function that places a notch at the average switching frequency, allowing for the PMU to operate within a wide range of switching

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frequencies in response to the varying conditions of the thermoelectric transducer while providing high supply noise rejection.

Chapter IV takes on a different challenge than previous chapters, this chapter discusses the details of an integrated circuit design implementing an ultra-low power transmitter (Tx) for IoT nodes. The fundamental goal of the proposed Tx is to reduce its power consumption and maximize its energy efficiency per transmitted bit. It follows that reducing the power required in the communication link section of the IoT node can significantly decrease the total node consumption. Between the analog front-end, the processor, and the wireless radio, it is the power consumption of the latter which dominates over that of the rest of the node components.

Reaching ultra-low power consumption levels in a wireless Tx requires a comprehensive approach that includes a system-level Tx design that anticipates and considers potential (new) circuit architectures that are of low power nature by themselves. Following this convention, chapter IV discusses the design strategy that lead to the proposed Tx, which operates in the 900 MHz ISM band using a wideband frequency-shift keying modulation. Taking advantage of these system level considerations, it is possible to use an open-loop, free-running ring-oscillator as the local oscillator (LO) generator in the proposed Tx. Moreover, a novel type of ultra-low power delay cell termed as vertical delay cell is introduced and employed to build the ring-oscillator. This oscillator architecture and the synthesizer-less approach further reduce the Tx power consumption. However, proposing a new, low power LO stage is only half of the way toward the ultimate goal of high energy efficiency in the Tx. An edge-combiner power amplifier (PA) stage is

used for implicit frequency multiplication of the LO at the PA output port. This PA structure allows the oscillator to operate at only ⅓ of the RF frequency. The Tx was fabricated in 0.18 μm CMOS technology and experimental results showed an oscillator tuning range large enough to provide an RF carrier tunability of 0.15 GHz–1.05 GHz. The maximum output power is −10 dBm, and the normalized energy efficiency is 3.1 nJ/(bit-mW) while transmitting with a 3 Mbps data rate.

Continuing the research in ring-oscillators, chapter V presents a BiCMOS ring-oscillator with high tolerance to supply-noise. To grant the ring-oscillator with this feature, a feedforward path from the supply to strategic nodes in the delay cells forming the oscillator is used in combination with a low-cost LDO. From a black-box point of view, the proposed solution reduces the supply sensitivity of the oscillator, which in turn relaxes the specifications of a global LDO in the PMU driving the oscillator in an IoT node. To avoid a simple transference of the requirements and power consumption from the global to the local LDO and feedforward path, the approach described in chapter V uses only passive components to build a high-frequency feedforward path with cut-off frequency as low as allowed by the allocated area. Due to its implementation and connection points, this feedforward filter essentially shields the delay cell against supply noise with frequencies higher than its cut-off frequency. To complement the solution, a low-cost LDO with bandwidth equal or larger than the cut-off frequency of the feedforward filter is used. In this way, the supply rejection provided by the LDO protects the oscillator against supply noise with frequencies below the cut-off of the feedforward filter. The

composite solution provides superior supply noise tolerance without strongly increasing the overall power consumption.

Finally, chapter VI presents this dissertation's conclusions, summarizes its contributions and sheds light into related opportunities for future work.

CHAPTER II

A COMPREHENSIVE MODEL FOR CMOS LOW DROPOUT VOLTAGE

REGULATORS

A comprehensive, yet simple and of fast simulation time SPICE-oriented model for CMOS Low-Dropout (LDO) voltage regulators is presented in dissertation. The self-contained model tracks the instantaneous LDO output current to continuously describe the LDO operation. A set of nonlinear polynomials obtained from simulation data describes the pass transistor in the LDO loop context and constitutes the cornerstone of the model. Additional but key to the accurate modelling of the small and large signal LDO characteristics is the inclusion of individual models for the error amplification path, feedback stage and frequency compensation. The topology-independent LDO model is portable and useful in the design, analysis and verification of integrated systems that use LDOs. Altogether, the computational and assembling efforts are minimized by using only SPICE elements in the model. To fully verify the model validity, three modelling case studies for different LDO structures are presented, one of which includes comparison versus experimental results. The generated models demonstrate the versatility of the approach and expose the model as an agile tool to examine the LDO effects at the system level. The models exhibit analysis-dependent simulation time reduction factors up to 10x and 110x when compared with circuit schematic-level and extracted-level simulations, respectively.

2.1   Introduction

It is the coexistence and interaction of analogue and digital circuits that enable the high performance of the state-of-the art integrated circuits. The high level of integration displayed in such systems is part of the reason for the widespread use of the low-dropout voltage regulator (LDO) [9-12]. Whether the LDO is used to increase the isolation between analog and digital circuits (Fig. 9a), generate multiple on-chip supply domains (Fig. 9b), or improve the point-of-load regulation in power delivery networks (Fig. 9c), high performance LDOs seem to be present in almost every integrated circuit. While in some applications the LDO is still considered an ancillary circuit able to provide clean supply voltages to noise-sensitive circuits, the LDO has turned into a central piece in certain systems due to its extensive use [11, 13, 14]. Due to the recurrent use of LDOs, there is a pressing need for an LDO model able to provide fast evaluation of LDO structures within the main system's context. Furthermore, an accurate LDO model is key to reduce computing and simulation time of integrated systems using multiple LDOs. Replacing the LDO with its model counterpart allows to focus the design and debugging efforts on the main system.
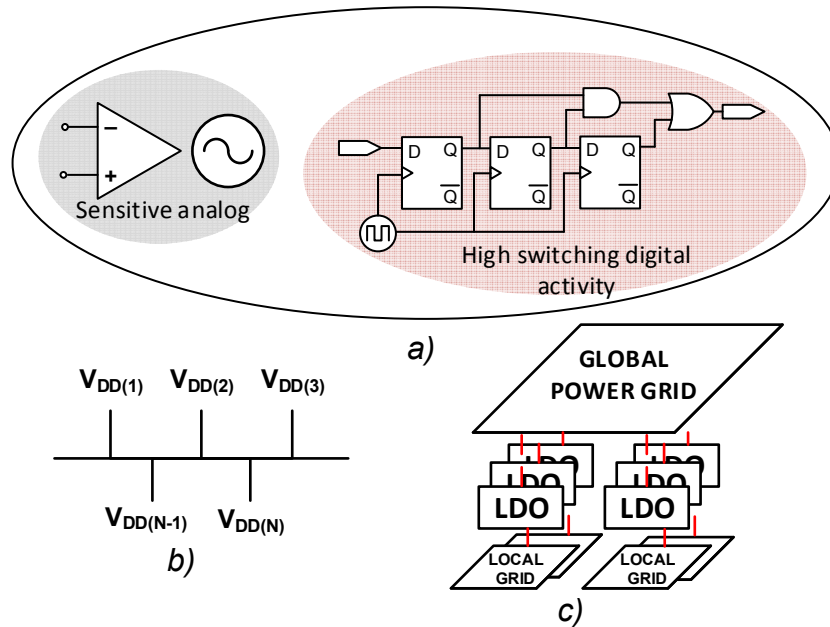
Fig. 9. Examples of LDOs use in Systems-on-Chip: a) Increase isolation between analog and digital circuitry, b) Generate multiple power domains, and c) Improve point-of-load regulation.

Contrary to the case of switched-mode power supplies where different models have been developed in the last 30 years [15-17], the available options for LDO models are limited and far from a self-contained solution. The models in [18-20] use an actual transistor to model the pass device, with [18] providing a full characterization for only one regulator topology; [19] and [21] limited to small-signal AC analyses; and [20] using Verilog-A to complement the model. The model in [22] elegantly describes the LDO for electromagnetic compatibility purposes but does not evaluate other fundamental LDO specifications of interest for integrated circuit design. While the LDO synthesis framework in [23] demonstrated an efficient specification-to-silicon design flow, this methodology is complex and only applicable to LDOs using particular types of error amplifiers and compensation methods.

This chapter presents a comprehensive, SPICE-compatible LDO model that captures the frequency and time-domain LDO characteristics. The model is able to describe different LDO structures for all the load current values of interest. By exclusively employing SPICE elements, the model can be used in the multiple circuit simulation tools based on a SPICE engine, facilitating the model's adoption during the design stage by providing a readily available and low complexity model for integrated LDOs with suitable accuracy.

2.1.1 Low dropout regulators: Basics

In the general LDO (Fig. 10), the output voltage (V_{OUT}) is ideally a clean, scaled and regulated version of a noisy, unregulated input voltage (V_{IN}). Four major sub-blocks constitute the LDO in Fig. 10:

- **Pass transistor (M_P).** This device provides the current (I_L) demanded by the load (R_L). While an NMOS transistor can be used, a PMOS reduces the V_{IN} to V_{OUT} voltage drop. In Fig. 10, g_{ds}, C_{gd}, C_{gs}, C_{gb} and C_{ds} are M_P's drain-to-source conductance, gate-to-drain, gate-to-source, gate-to-bulk and drain-to-source capacitances, respectively. Since the performance of the LDO is tightly related to the I_L, M_P should be carefully sized accordingly to the I_L and dropout voltage ($V_{DO} = V_{IN} - V_{OUT}$) requirements. For a first order approximation, (1) can be used to determine the required width (W) of M_P (the length L is typically chosen based on the minimum

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allowable per the process technology L_{min}). In (1) μ_p is the hole mobility and C_{ox} is the oxide capacitance.

$$W = \frac{2I_L}{\mu_p C_{ox} V_{DO}^2} L_{min} \tag{1}$$

- **Feedback stage (β).** β feeds a scaled version of V_{OUT} (βV_{OUT}) to the error amplifier. It is typically implemented with a resistor divider. In Fig. 10, $\beta = R_2/(R_1+R_2)$.

- **Error amplifier (EA).** This amplifier compares a voltage reference, V_{ref}, with βV_{OUT} and modifies the M_P error control signal (V_{EA}) until the loop reaches the $\beta V_{OUT} \approx V_{ref}$ condition. The frequency response of the EA largely influences the overall LDO performance. While a wide bandwidth EA improves the linear part of the transient response and increases the supply-noise rejection, it generally entails high power consumption from the EA. particularly when M_P has been sized to provide I_L levels in the tens of mA-range. In the same way, a large EA slew rate improves the non-linear part of the LDO transient response at expense of reduced current efficiency.

- **Frequency compensation scheme (FCS).** The FCS secures the loop stability; it can be passive or active and implemented off-chip or on-chip in an active or mixed (active + passive) fashion. In Fig. 10, an off-chip capacitor C_L with series resistance R_{ESR} act as FCS. In the case of internally-compensated LDO structures (on-chip FCS), the dominant pole

of the LDO regulation loop is typically located at the intersection of the EA

and M_P gate. Conversely, in an externally-compensated LDO (off-chip

FCS), the dominant pole is defined by the external C_L (as in Fig. 10) at the

output node.

- The EA and FCS sub-blocks are sometimes merged when an on-chip FCS

  is used.

Multiple variations of the LDO in Fig. 10 have been proposed in the literature [24-

29]. Though the details differ from LDO to LDO [24], the structure in Fig. 10 forms the

backbone of many LDOs with different characteristics [25-29]. Consequently, the

proposed model is derived from the Fig. 10 structure. Yet, the modelling approach can be

applied to most internally or externally-compensated LDOs where the four mentioned sub-

blocks can be identified.
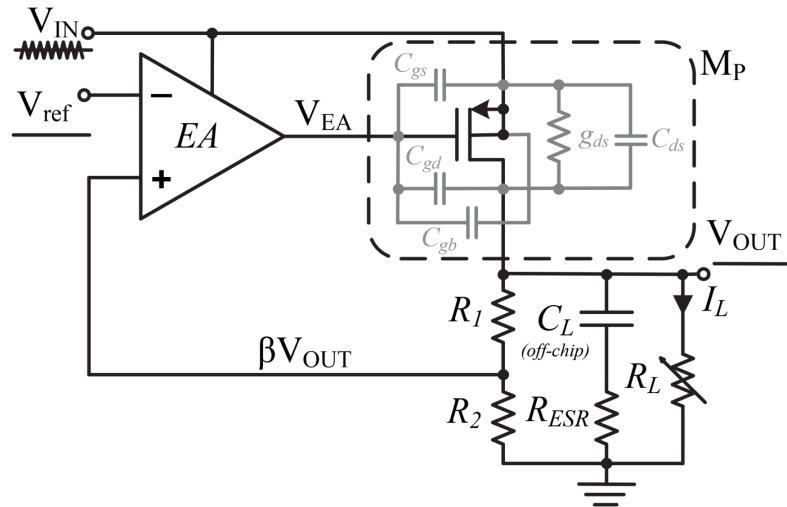
Fig. 10. General CMOS LDO structure.

2.1.2 Transfer-function-based LDO model

Every LDO sub-block has an associated frequency-dependent, small signal transfer function (TF). Thus, a TF-based approach is often used to model LDOs. The sub-blocks of the Fig. 10 LDO are mapped to their equivalent TFs in Fig. 11. In this model A_{MP} and A_{EA} represent the M_P and EA voltage gain at DC, respectively; ω_{PD} is the loop dominant pole due to C_L and the LDO output resistance; ω_z is a zero due to C_L and R_{ESR}; and $\omega_{PND1,\,2}$ are non-dominant poles at the output and internal nodes of EA, respectively. The Fig. 11 model describes the LDO AC characteristics accurately *only* for a small set of I_L values in the proximity of the bias point at which the TF coefficients were obtained. The limited I_L-range and its inadequacy to characterize the large signal LDO behavior are the two main drawbacks of this modeling approach.

For a comprehensive description of LDOs, a model supporting the following analyses is proposed in this dissertation:

- **Transient.** Time-domain analysis used to evaluate load and line regulation as the LDO response (ΔV_{OUT}) to ΔI_L and ΔV_{IN} steps, respectively.

- **DC**. Bias point analysis used to evaluate V_{OUT} for static I_L values.

- **AC**. Frequency-domain analysis used to evaluate the LDO response to V_{IN} perturbations with frequency f_n, for all f_n of interest.

- **Stability (STB)**. Frequency-domain analysis used to evaluate loop stability in terms of the magnitude and phase of the open loop gain response.

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$$\frac{s/\omega_z + 1}{s/\omega_{PD} + 1}$$

A_{MP}

M_P voltage gain

FCS dominant pole & zero

V_{IN} +

Σ

V_{OUT}

β Feedback Factor

$$\frac{A_{EA}}{(s/\omega_{PND1} + 1)(s/\omega_{PND2} + 1)}$$

EA gain and poles

Σ

V_{ref}
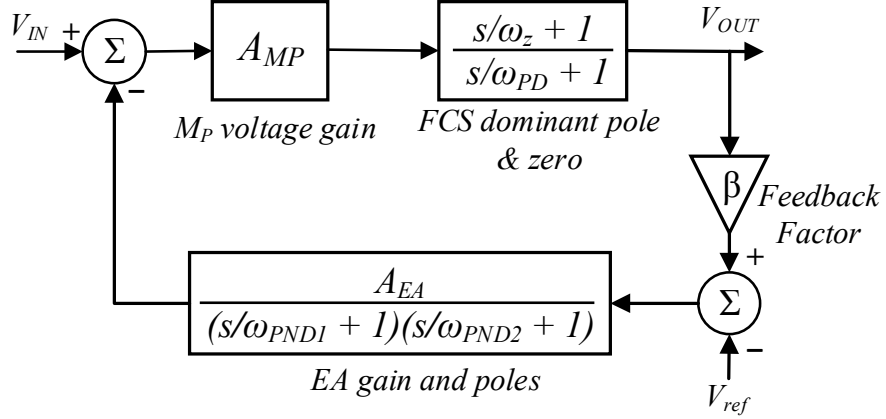
Fig. 11. TF-based model of an LDO using a two-stage EA.

2.2 Proposed LDO model

An LDO regulator should be able to supply a range of I_L values while maintaining a constant V_{OUT}. This is done by modulating the M_P's parameters (e.g. transconductance g_m) via a change in its source-gate voltage (V_{sg}) commanded by the EA. During this processing, M_P closely interacts with critical voltage signals (V_{EA}, V_{IN} and V_{OUT}) and with the load resistance R_L. For the above reasons, in a robust and self-contained LDO model, I_L should be constantly monitored and the M_P model's parameters modified accordingly to dynamically reflect the behavior of a real, transistor-level (TL) LDO.

The proposed model reproduces the operation of a TL-LDO using a two-step approach. Firstly, the values of relevant M_P parameters (g_m, g_{ds}, C_{gs}, C_{gd}, C_{gb} and C_{ds}) are generated via a set of polynomials in terms of the instantaneous I_L, as shown in Fig. 12 for the polynomial describing g_m, $g_m(I_L)$. The $g_m(I_L)$ coefficients are used in a polynomial current-controlled current source (PCCCS). This PCCCS steers current into a 1 Ω resistor

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(R_T) and generates a voltage signal denominated $g_m{}^v$, which carries the nonlinear information about g_m. While the units of $g_m(I_L)$ are S or A/V, the signal at the PCCCS output is current. Thus, the action of the PCCCS is similar to artificially multiplying $g_m(I_L)$ by a 1 V scaling factor which gives dimensional congruence to the operation. Secondly, $g_m{}^v$ is weighted by its instantaneous controlling voltage (V_{sg} or V_{IN}-V_{EA}, in this case) using a two-port, polynomial voltage-controlled current source (PVCCS) to generate I_{gm} (Fig. 12). I_{gm} represents the g_m-contribution to I_L. In step two, the PVCCS de-embeds the g_m information from the voltage signal $g_m{}^v$. For dimensional correctness, $g_m{}^v$ is artificially multiplied by a 1 Ω^{-1}/V scaling factor, removing the effect of R_T and 1 V scaling factor from step one. As will be detailed later in this chapter, the process of Fig. 12 is repeated for all the relevant parameters of M_P to generate the LDO response at V_{OUT} and I_L.

$$I_x = g_m(I_L)\cdot 1V$$
$$g_m{}^v = I_xR_T = g_m(I_L)\cdot 1V \cdot 1\Omega$$

$$(V_{IN} - V_{EA}) = V_{sg}$$
$$I_{gm} = g_m{}^vV_{sg}\cdot 1\Omega^{-1}/V$$
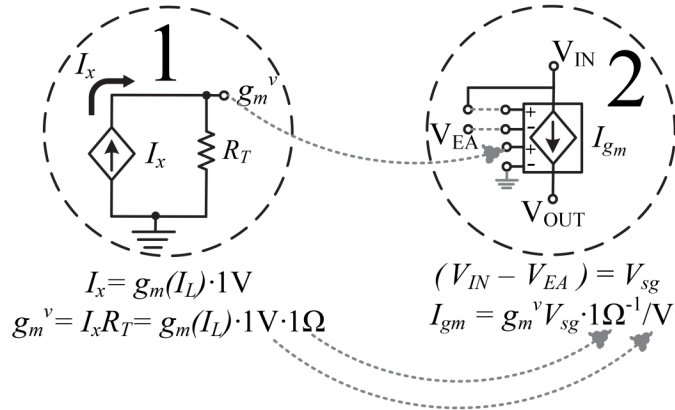
Fig. 12. Implementation of the g_m-parameter to model M_P.

To understand the rationale behind the modelling approach, consider M_P as part of a weakly nonlinear circuit, where the M_P drain current (I_D) is approximated by (16) and $a_{1, 2, 3}$ are the linear gain and second/third-order nonlinearity coefficients [30].

$$I_D = a_1 V_{sg} + a_2 V_{sg}^2 + a_3 V_{sg}^3 \tag{2}$$

The nonlinear large signal transconductance G_M [31] (parameter that quantifies the transistor's property to convert input voltage into an output current) can be obtained from the M_P V-I transfer characteristics, or dividing (16) by the input voltage of M_P (V_{sg}) to get:

$$G_M = a_1 + a_2 V_{sg} + a_3 V_{sg}^2 \tag{3}$$

Following (3), the large signal equations relating I_D ($I_D \approx I_L$) with V_{sg} could be invoked to reflect the G_M dependency on I_L. For the case when the transistor operates in saturation region, (3) can be re-written (4) as to show the G_M dependency on I_L.

$$G_M = a_1 + a_2 \left(\sqrt{\frac{I_L}{K'}} + V_T \right) + a_3 \left(\sqrt{\frac{I_L}{K'}} + V_T \right)^2 \tag{4}$$

In (4), K' encompasses the physical characteristics of M_P ($K' = \mu_p C_{ox} W/2L$) and V_T is the threshold voltage. Further expanding (4), an expression directly showing I_L as independent variable in can be obtained (5).

$$G_M = \underbrace{a_1 + a_2 V_T + a_3 V_T^2}_{b_1} + \sqrt{I_L} \underbrace{\left(\frac{a_2}{\sqrt{K'}} + \frac{2 a_3 V_T}{\sqrt{K'}} \right)}_{b_2} + I_L \underbrace{\left(\frac{a_3}{K'} \right)}_{b_3} \tag{5}$$

Using the first four terms of a Taylor series to approximate the $\sqrt{I_L}$ term and grouping the b-terms, the expression in (5) becomes (6). Collecting this time the c-terms in (6), finally the raw dependence of G_M on I_L is clear in (7).

$$G_M = \underbrace{b_1 + \frac{5}{16}b_2}_{c_1} + I_L \underbrace{\left(\frac{15}{16}b_2 + b_3\right)}_{c_2} - I_L^2 \underbrace{\left(\frac{5}{16}b_2\right)}_{c_3} + I_L^3 \underbrace{\left(\frac{1}{16}b_2\right)}_{c_4} \tag{6}$$

$$G_M = c_1 + c_2 I_L + c_3 I_L^2 + c_4 I_L^3 \tag{7}$$

However, this approach would leads to three G_M polynomials of I_L powers, one per M_P operation region (subthreshold, triode and saturation). This piecewise modelling of M_P requires a dynamic assessment of the operating region, which increases the complexity [32].

The proposed LDO model reduces this complexity by describing every M_P parameter with a single polynomial of the form (8) or (9). However, to guarantee that the polynomials' evaluations are valid for all operating regions, the g_i and g_i^* coefficients are obtained via a polynomial fitting designed to mimic the M_P data extracted from the TL LDO across the entire I_L range.

$$G_M(I_L) = g_o + g_1 I_L + g_2 I_L^2 + g_3 I_L^3 + \cdots + g_n I_L^n \tag{8}$$

$$G_M(I_L, V_{sg}) = g_0^* + g_1^* I_L + g_2^* V_{sg} + g_3^* I_L^2 + g_4^* I_L V_{sg} + g_5^* V_{sg}^2 + \ldots \tag{9}$$

Describing M_P in the model through polynomials fitted from simulation data breaks any dependency on the transistor model, increasing the portability and simulation speed of the proposed LDO model. Furthermore, the g_o coefficient in (8) and (9) reflects a boundary value of the parameter. Thus, the model provides a convenient way to explore the effects of individual M_P parameters in the LDO performance. More importantly, the description of the M_P parameters with (8) and (9) enables the modelling concept of Fig. 12. For instance, if the g_i coefficients are used in a PCCCS, its output current can be mapped to the instantaneous values of the M_P parameters. Each parameter's contribution

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towards the LDO response is obtained by weighting it with its controlling voltage. The linear combination of the individual contributions fully characterizes the M_P influence on the LDO response for all I_L of interest. In order to determine which M_P parameters require individual polynomial modelling, the LDO in Fig. 10 was subjected to an I_{Lmin} to I_{Lmax} (1-50 mA) DC sweep[1]. The results of the characterization are shown in Fig. 13.
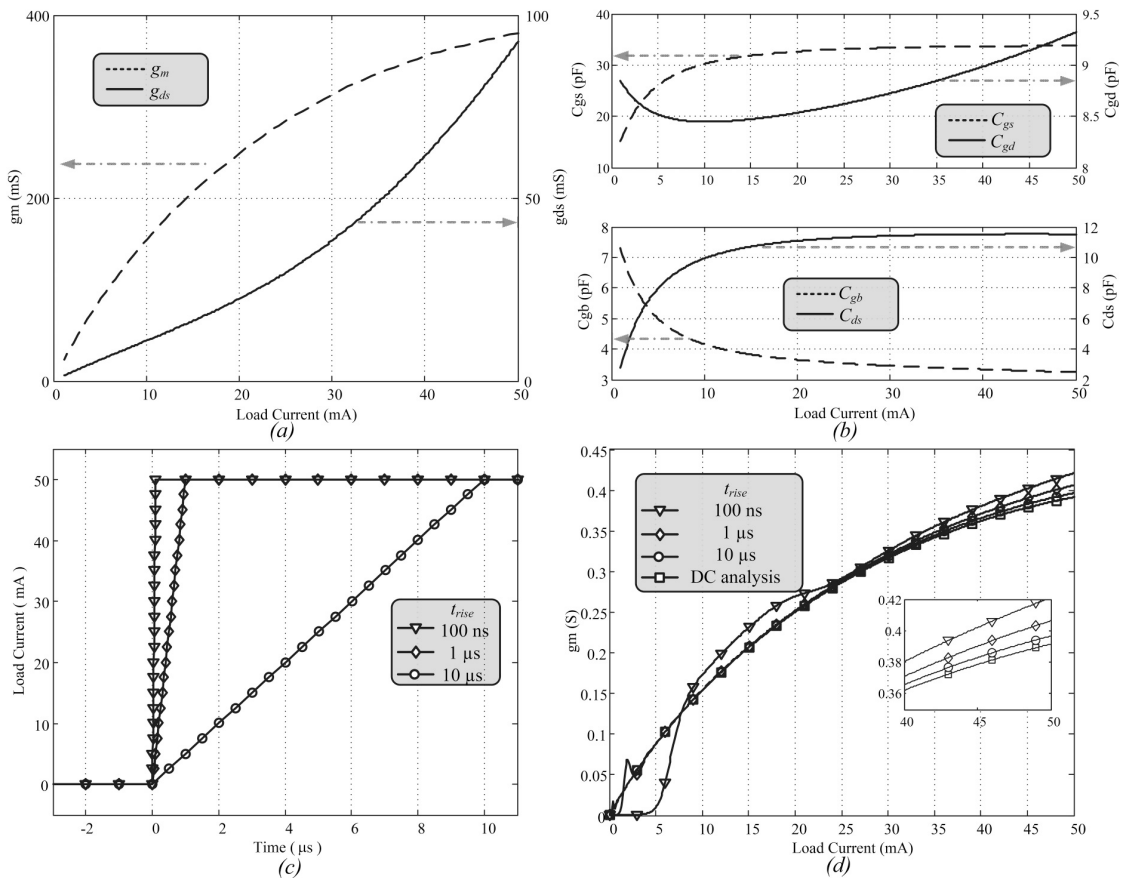
Fig. 13. M_P characterization results: (a) M_P's g_m and g_{ds} in function of I_L during a I_{Lmin} to I_{Lmax} DC sweep; (b) M_P's C_{gs}, C_{gd}, C_{gb} and C_{ds} in function of I_L during a I_{Lmin} to I_{Lmax} DC sweep; (c) I_L transient event (step) with different t_{rise} for M_P transient characterization, and (d) M_P static and dynamic g_m comparison.

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[1] In this analysis, the bulk transconductance, g_{mb}, has been neglected since in most cases the M_P source and bulk terminals are tied together.

From Fig. 13a and Fig. 13b it is concluded that independent polynomials are required for g_m, g_{ds} and C_{ds}. However, C_{gd} remains fairly constant with I_L ($\Delta C_{gd} < 10\%$) and can be modelled using a fixed capacitor with the average C_{gd_av} value. Also, due to zero source-bulk potential, C_{gs} and C_{gb} are clustered in one polynomial (denoted as C_{gs} from now on). Note that the mostly monotonic nature of the results in Fig. 13 makes them candidates for polynomial fitting. These polynomials will indeed describe M_P within the $I_{Lmin-max}$ limits.

The solution of the DC characterization sweep captures the nonlinear M_P I-V relations, which are represented by fitted polynomials of sufficiently high order that enable an accurate-by-construction LDO model in the targeted I_L range. Nevertheless, the DC analysis is static and memory-less [33]. To test the approach in transient simulations, the LDO in Fig. 10 is subjected to a transient event (I_L step) of duration t_{rise} (Fig. 13c). The variations of the M_P g_m during the transient event (dynamic g_m) are compared with those observed during the DC sweep (static g_m) in Fig. 13d. As shown in Fig. 13d, dynamic and static g_m diverge for fast transitions (small t_{rise}); whereas as t_{rise} increases, both g_m closely follow each other. This trend is consequence of the characterization setup (LDO loop limiting the M_P bias point's update rate in response to a transient stimulus) and is consistent in the rest of the M_P parameters. Therefore, to approximate the dynamic LDO characteristics using fitted polynomials, t_{rise} should observe a minimum value, t_{min}. To find t_{min}, the following assumptions are made:

- The LDO observes a first order low-pass Butterworth frequency response up to its unity-gain frequency, ω_u, and

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- The EA slew-rate (SR_{EA}) and the voltage swing at the gate of M_P required to take I_L from I_{Lmin} to I_{Lmax} (ΔV_{sg_max}) satisfy (10); i.e. there is no SR distortion [34].

$$\Delta V_{sg\_max} < \frac{SR_{EA}}{\omega_u} \tag{10}$$

During an I_L transient event, both stimulus (ΔI_L) and response (ΔV_{OUT}) occur at the V_{OUT} node. Therefore, under the above assumptions, V_{OUT} exhibits a rising time obeying (11) [34] in response to ΔI_L. Similarly, (11) provides the t_{min} value that an I_L transient event can take for the LDO loop and the proposed model to track it.

$$t_{rise} > \frac{2.2}{\omega_u} = t_{min} \tag{11}$$

Although the conditions introduced to arrive at (11) might appear to preclude some LDO designs from using the model, (10) and (11) only define a limit for increased accuracy and the model can still be used during transient events with $t_{rise} < t_{min}$, at expense of reduced accuracy.

Even though more rigorous approaches to model the nonlinear circuit dynamics are available such as: symbolic modeling applied to weakly nonlinear analog circuits for system-level design exploration [35]; neural network and time series-based models for nonlinear behavioral modeling [36]; and nonlinear model order reduction in weakly time-invariant and time-varying nonlinear circuits [37, 38]. These techniques, [35-38], tend to produce complicated models and its implementation at the SPICE level is cumbersome at best. Furthermore, sometimes such complex models require access to additional programming environments or simulation engines.

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In the proposed model, the static and dynamic circuit nonlinearities are described using a set of continuously evaluated polynomials whose response is dictated by the loop dynamics. This approach produces a straightforward, SPICE-compatible model accurate within the bandwidth of the target LDO. Furthermore, gearing the multiple parameters of the PCCCS, it is possible to extend the model functionality and include the temperature dependency via the built-in first and second order temperature coefficients, which can be extrapolated from simulation results across the temperature gradient of interest.

The incorporation of the EA, β and FCS sub-blocks to the model via suitable amplifier models [39-42] and passive components is key for a self-contained LDO model, and is addressed in Chapter 2.3. While in some cases, β and FCS are comprised of purely passive components (which can be directly incorporated in the model), some LDO structures might implement either β or FCS (or both) using active elements. In the latter case, these sub-blocks can be treated and modeled similarly to the EA, as will be shown. For identification purposes, Fig. 6a shows conceptual representations of the LDO sub-blocks and their potential interconnections. Examples of typical circuits used to build each sub-block are shown in Fig. 6b. For LDOs using a feed-forward stage (FFS), $K(f)$ represents its gain (Fig. 6b).
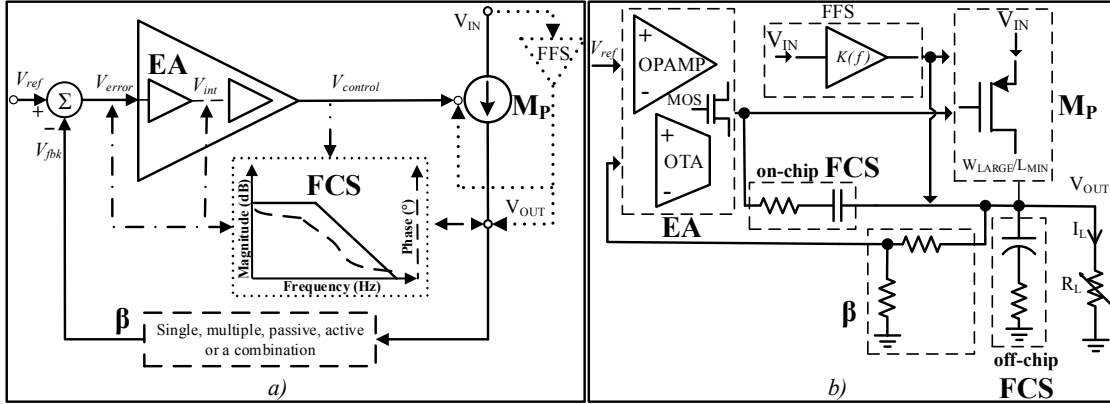
Fig. 14. a) LDO conceptual sub-block identification for modeling; b) Typical devices and circuits implementing the sub-blocks.

2.3 LDO model implementation

A model for the LDO in Fig. 10 is built in this section to illustrate the modelling approach. The TL LDO was designed in 0.5 μm CMOS for a 1-50 mA I_L and a 3.2/3 V_{IN}/V_{OUT} ratio. An external 10 μF C_L implements the FCS for a maximum f_u ($\omega_u/2\pi$) of 2.5 MHz and 77° phase margin (PM), and a min f_u of 600 kHz (88° PM).

2.3.1 M_P polynomial representation

Using the data acquired with the DC characterization discussed in chapter 2.2, any suitable curve fitting technique [43] can be used to obtain the M_P-describing polynomials: $g_m(I_L)$, $g_{ds}(I_L)$, $C_{gs}(I_L)$, and $C_{ds}(I_L)$. Table 1 shows the coefficients of 5th order (8)-type fitted polynomials corresponding to the Fig. 10 LDO model. These coefficients are obtained applying the *polyfit* function (least squares method) in Matlab® [43] to the Fig.

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13 data. The average error between the obtained polynomials and the characterization data is < 2%.

Table 1. Polynomial coefficients for a 5th order fitting.

Parameter	p_0	p_1	p_2	p_3	p_4	p_5
g_m	2.1×10^{-3}	19.6	-0.5×10^3	1.3×10^4	-1.9×10^5	1.2×10^6
g_{ds}	7.8×10^{-5}	1.2	-18.4	0.7×10^3	2.8×10^3	-7.8×10^4
C_{gs}	-2.1×10^{-11}	-2.8×10^{-9}	2.1×10^{-7}	-7.5×10^{-6}	1.3×10^{-4}	-8.8×10^{-4}
C_{ds}	2×10^{-12}	1.7×10^{-9}	-1.2×10^{-7}	-4.5×10^{-6}	-7.9×10^{-5}	5.3×10^{-4}

In Fig. 15a, the Table 1 coefficients are used in four PCCCS to implement the $g_m(I_L)$, $g_{ds}(I_L)$, $C_{gs}(I_L)$ and $C_{ds}(I_L)$ polynomials. The PCCCS measure I_L via 0 V source (V_{sense}) and ultimately generate signals $g_m{}^v$, $g_{ds}{}^v$, $C_{gs}{}^v$ and $C_{ds}{}^v$ representing the updated parameters values (as in Fig. 12).
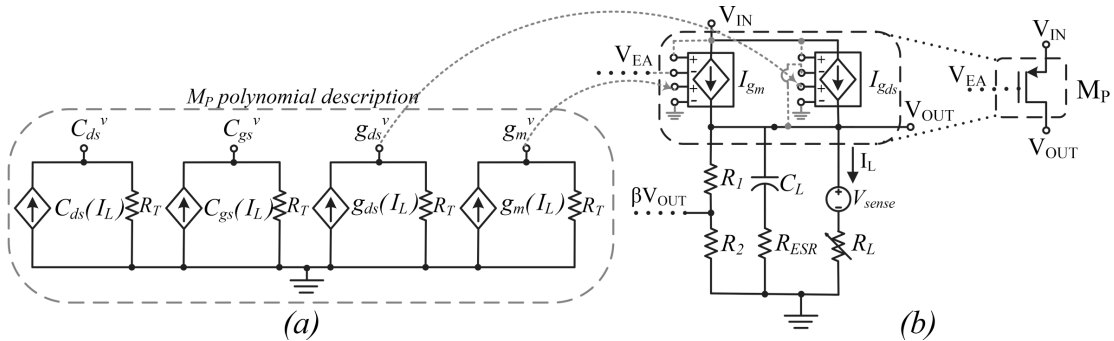
Fig. 15. M_P model and partial (g_m and g_{ds}) implementation: a) M_P polynomial description using PCCS (Step 1 in Fig. 12); b) $g_m{}^v$ and $g_{ds}{}^v$ weighting and contributions towards I_L (I_{gm} and I_{gds}) using two 2-port PVCCS (Step 2 in Fig. 12).

To generate the g_m and g_{ds} contributions to I_L (I_{gm} and I_{gds}), the $g_m{}^v$ and $g_{ds}{}^v$ signals are weighted using two 2-port PVCCS realizing (12) and (16) (Fig. 15b). The PVCCS implement (9)-type polynomials (with [0, 0, 0, 0, 1] as the $g_0{}^*$-$g_4{}^*$ coefficients) to multiply the signals at its two ports.

$$I_{g_m}=g_m{}^v(V_{IN}-V_{EA})=g_m{}^v V_{sg} \tag{12}$$

$$I_{g_{ds}}=g_{ds}{}^v(V_{IN}-V_{OUT})=g_{ds}{}^v V_{sd} \tag{13}$$

The weighting of the $C_{gs}{}^v$ and $C_{ds}{}^v$ signals is done using the circuit in Fig. 16, where the C_{xy} capacitance is tuned using a CCCS with variable gain K_{xy} and capacitor C_{Mxy}. To obtain K_{xy}, $C_{gs}(I_L)$ and $C_{ds}(I_L)$ are mapped to auxiliary polynomials $K_{gs}(I_L)$ and $K_{ds}(I_L)$ using (16). The $K_{gs}(I_L)$ and $K_{ds}(I_L)$ coefficients are used in two PCCCS to generate voltage signals $k_{gs}{}^v$ and $k_{ds}{}^v$, which represent the variable gains required to emulate $C_{gs}(I_L)$ and $C_{ds}(I_L)$, respectively. A two-port PVCCS implements I_{Cxy} in Fig. 16. The corresponding PVCCS multiply the C_{Mxy} current (I_{Mxy}) with $k_{xy}{}^v$ as in (15) and (16) to model a $C_{xy}(I_L)$ capacitance between x and y, this is: gate-source for $C_{gs}(I_L)$ or drain-source for $C_{ds}(I_L)$. The complete M_P model is shown in Fig. 17, where the ports of the PVCCS implementing I_{gm}, I_{gds}, I_{Cgs}, and I_{Cds} are omitted.
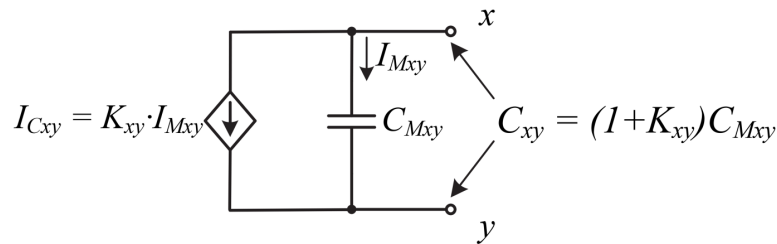
Fig. 16. Model for the variable C_{xy} of M_P.

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$$K_{xy}(I_L) = \frac{C_{xy}(I_L)}{C_{Mxy}} - 1, \quad C_{Mxy} = \min\left|C_{xy}(I_L)\right| \tag{14}$$

$$I_{C_{gs}} = k_{gs}{}^v I_{Mgs} \tag{15}$$

$$I_{C_{ds}} = k_{ds}{}^v I_{Mds} \tag{16}$$
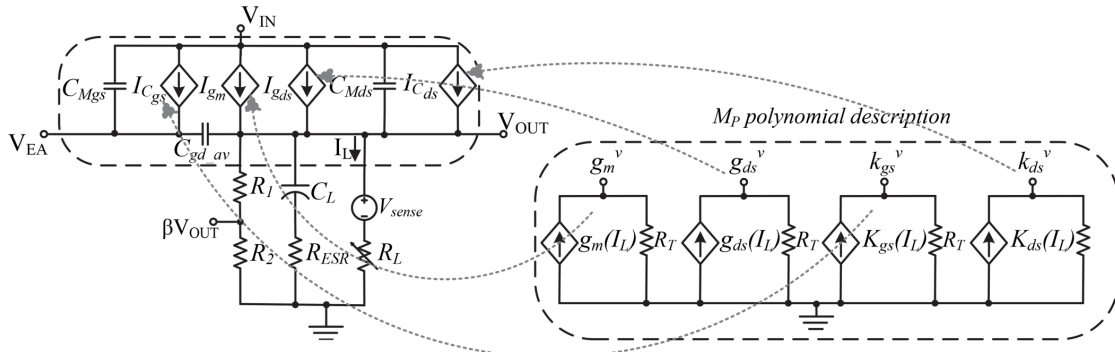
Fig. 17. Complete M$_P$ model. C$_L$ and β included to show the connections.

2.3.2   EA model

A modified, SPICE-amiable version of [42] is adopted in the proposed LDO model to describe the EA (Fig. 19). Yet, other models can also be used [39-41]. In Fig. 19, the so-called threshold element TE1 (TE2) provides a logic '1' ('0') when its input exceeds its threshold and a logic '0' ('1') otherwise [42]. In our EA model, each TE is replaced by two switches with complementary open-close voltages. The threshold values are obtained from the EA I/O transfer characteristics, similar to the one shown in Fig. 18.
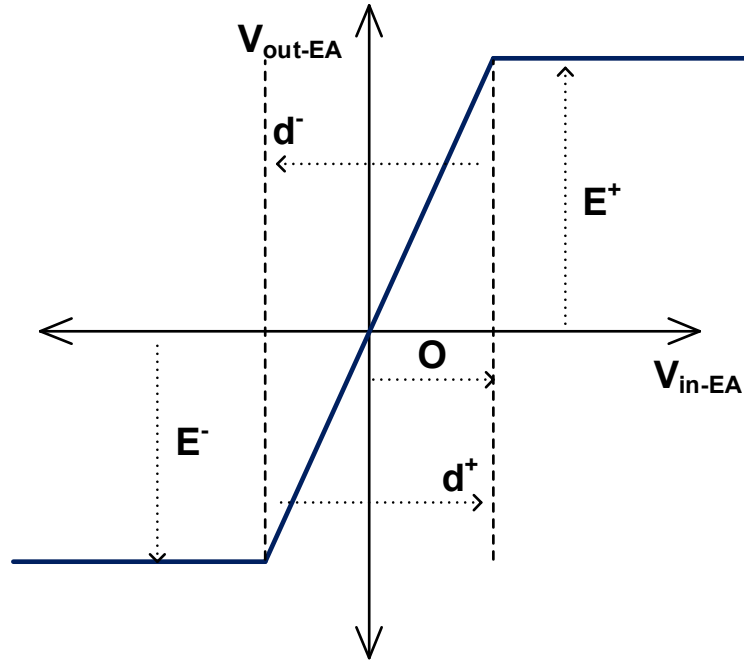
Fig. 18. Threshold values for the EA model obtained from the EA I/O transfer characteristics.

The thresholds can be approximated as follows: d^+ and d^- are the positive and negative limits in the I/O curve; E^+ and E^- are the maximum and minimum EA output voltages; and O is the input voltage which causes the EA output to saturate [42]. The TEs and resistor-switch logic gates generate the enable signals (Z_{1-4}) for switches S_{1-4}. The output of the EA model (V_{EA}) is determined as follows: through S_2 with a current proportional to the input differential voltage (V_D) and the EA transconductance (G_a); through S_3 and S_4 with a fixed current to emulate the positive (I_r) and negative (I_f) SR conditions; or with no current when saturated (S_1 open). The $R_a C_a$ product models the pole at M_P's gate. However, since the capacitance at this node is embedded in the M_P model, it is enough to assign the value of the EA output resistance to R_a. Additional EA poles and zeros can be added to the model using unity gain stages and RC products [42].

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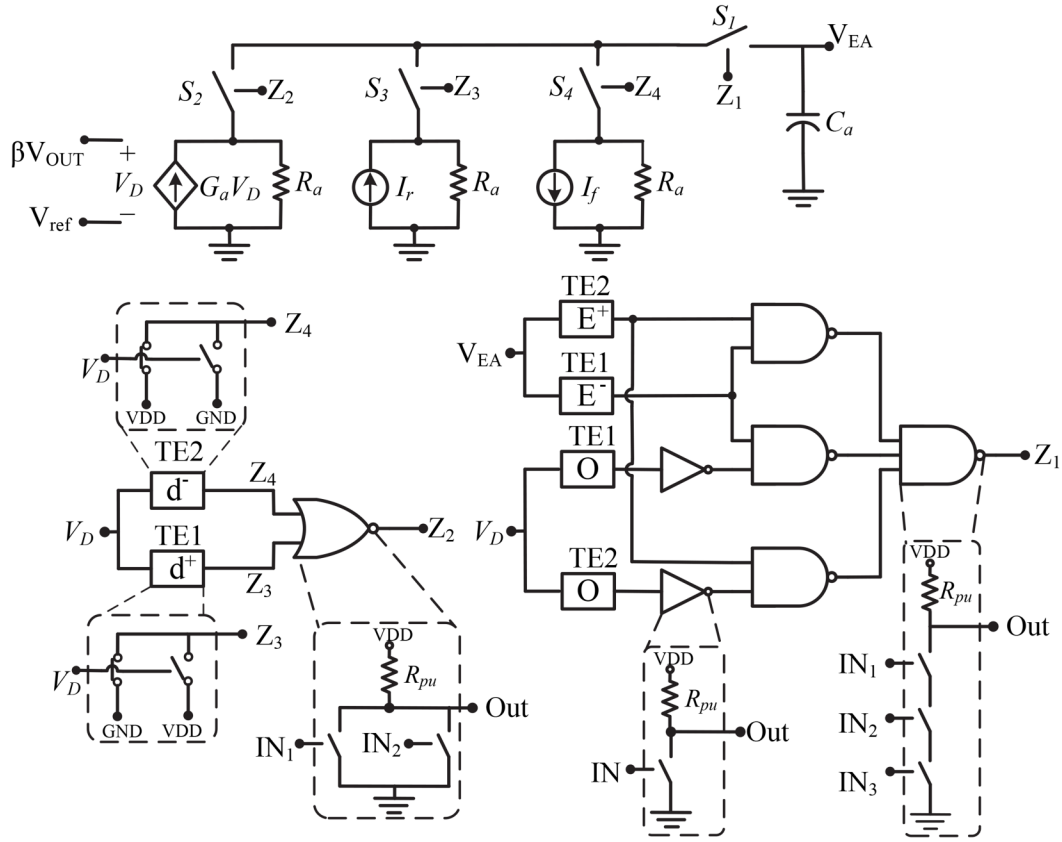
Fig. 19. EA model. Modified and adapted from [42].

In the modeling case study for the LDO in Fig. 10, the gain of the EA (A_{EA}) is 51 dB (i.e. $G_a R_a$ ~355) and the pole at the gate of M_P is located in average at 13 kHz. A second pole is included (~$10 f_u$) in the EA model to mimic the EA frequency response with 1% accuracy up to 10 MHz. Note that this information could also be used to model the EA using a VCCS-based model [39] and provide a simpler solution for an LDO model suitable for AC analyses. Nevertheless, the model in Fig. 19 can be constructed following the flow diagram in Fig. 20 and allows for a complete, transient-compatible LDO model without significantly increasing the complexity.
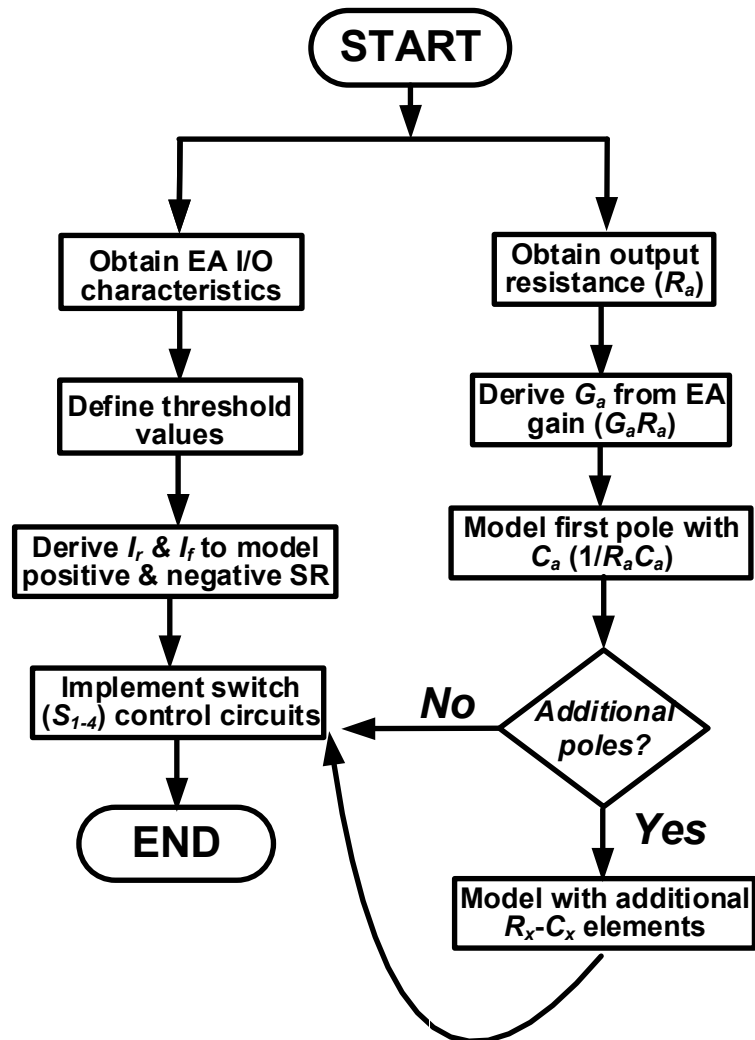
Fig. 20. Flow diagram to implement EA model.

2.3.3   *Frequency compensation scheme (FCS) and β*

In the case of the Fig. 10 LDO, the FCS (C_L and R_{ESR}) and β ($R_{1,\,2}$) are included in the model using passive components (Fig. 17). Although FCS and β in passive form are the norm in most LDOs, the modelling of LDOs with active FCS is also supported by this model and is illustrated with a case study in Chapter 2.4. In short, the modeling of active

FCS and β stages can be carried similarly to the EA stage by characterizing their frequency and nonlinear transient responses using the approach of Fig. 19.

2.3.4 Special considerations for PSR modeling

If the TL LDO to be modeled uses an EA defined as Type-B amplifier [44], the Fig. 19 EA model is suitable to characterize the PSR of the LDO in question. However, if the TL LDO contains any Type-A amplifier [44], a direct V_{IN}-M_P's gate AC path should be included. As shown in Fig. 21, a VCVS with attenuation A_{AT} can be used to reflect the EA PSR in the model. Notice that this direct path is only present for AC signals and does not disturb the M_P bias point. To determine A_{AT}, the TL EA V_{IN}-to-V_{EA} noise path should be evaluated (i.e. obtain V_{EA}/V_{IN}) and the result subtracted from A_{EA}; this residue normalized by A_{EA} amounts to A_{AT}. This modification does not result in any loss of generality since for Type-B EA, A_{AT} equals zero.
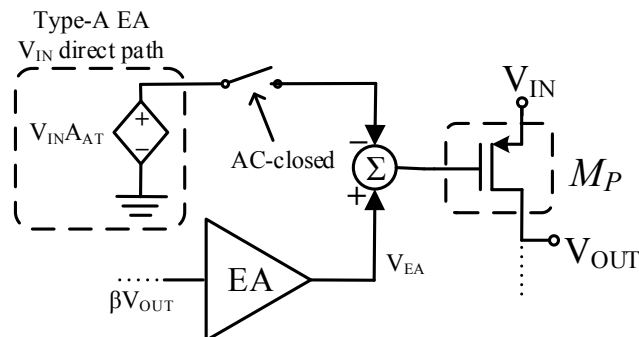
Fig. 21. Modification to model's PSR path when a Type-A EA is present.

While the main purpose of the model is to provide a low complexity yet accurate representation for a large collection of LDO structures, the model can also be used to study the LDO influence on the load circuit performance. For example, the pole/zero location and/or voltage gain of the EA and/or FCS can be conveniently modified in the LDO model for a rapid examination of such parameter's influence on certain LDO specifications, extending the model's application from the verification to the design stage.

2.4   Model simulation results for different LDO structures

This section shows the LDO model generality by evaluating its performance for three LDO structures: *i)* The general LDO (Fig. 10); *ii)* A high power-supply rejection (PSR) LDO [25] (Fig. 22a); and *iii)* A fast transient LDO with on-chip FCS [27] (Fig. 22b). The performance of the model for the LDO in [27] was compared against a) simulation results at the TL, and b) actual experimental results from a fabricated LDO. The simulation time and error per analysis are quantified using Cadence Virtuoso ADE XL–IC6.1.5.
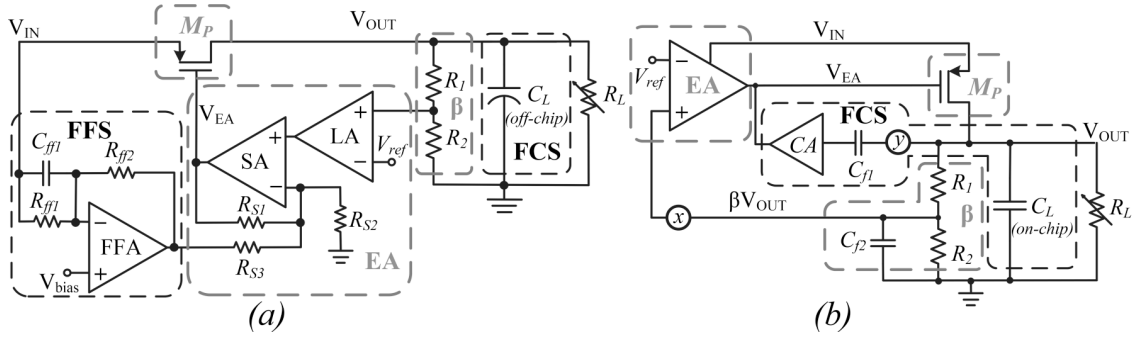
Fig. 22. LDOs modeled as case studies: a) High PSR LDO [25]; b) Fast transient LDO with on-chip, active FCS [27].

2.4.1 Model for the general LDO structure

The development of the proposed model for the Fig. 10 LDO was used to illustrate the model creation flow in Chapter 2.3. The simulation results for both, the resulting model and the actual TL LDO are presented and contrasted in Fig. 24 and Fig. 24. The model's error at V_{OUT} during a DC analysis (with respect to the TL LDO) is 0.08% (<2.5 mV) for all its I_L range, as shown in Fig. 23. The results of the loop stability analysis (STB), shown in Fig. 24a, exhibit small phase and magnitude errors, noticeable only above 10 kHz. As shown in Fig. 24b, the model reproduces the TL LDO PSR with an error <1 dB up to 30 kHz. To evaluate load regulation, a 200-ns t_{min} is calculated using (11) (considering a 1.1 MHz average f_u). Thus, a t_{rise} of 1-µs ($t_{rise} \gg t_{min}$) is used in an I_L step. The results (Fig. 24c) show that the model's V_{OUT} variations follow those of the TL LDO with an error of few mV. For the line regulation test, a 3.2-3.8 V V_{IN} step was used and the results (Fig. 24d) also show errors of few mV.

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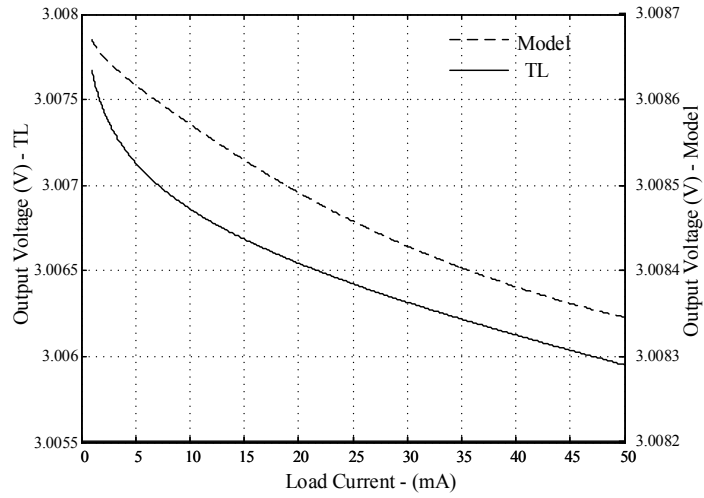
Fig. 23. DC analysis simulation results for the TL LDO of Fig. 10 and its generated model.
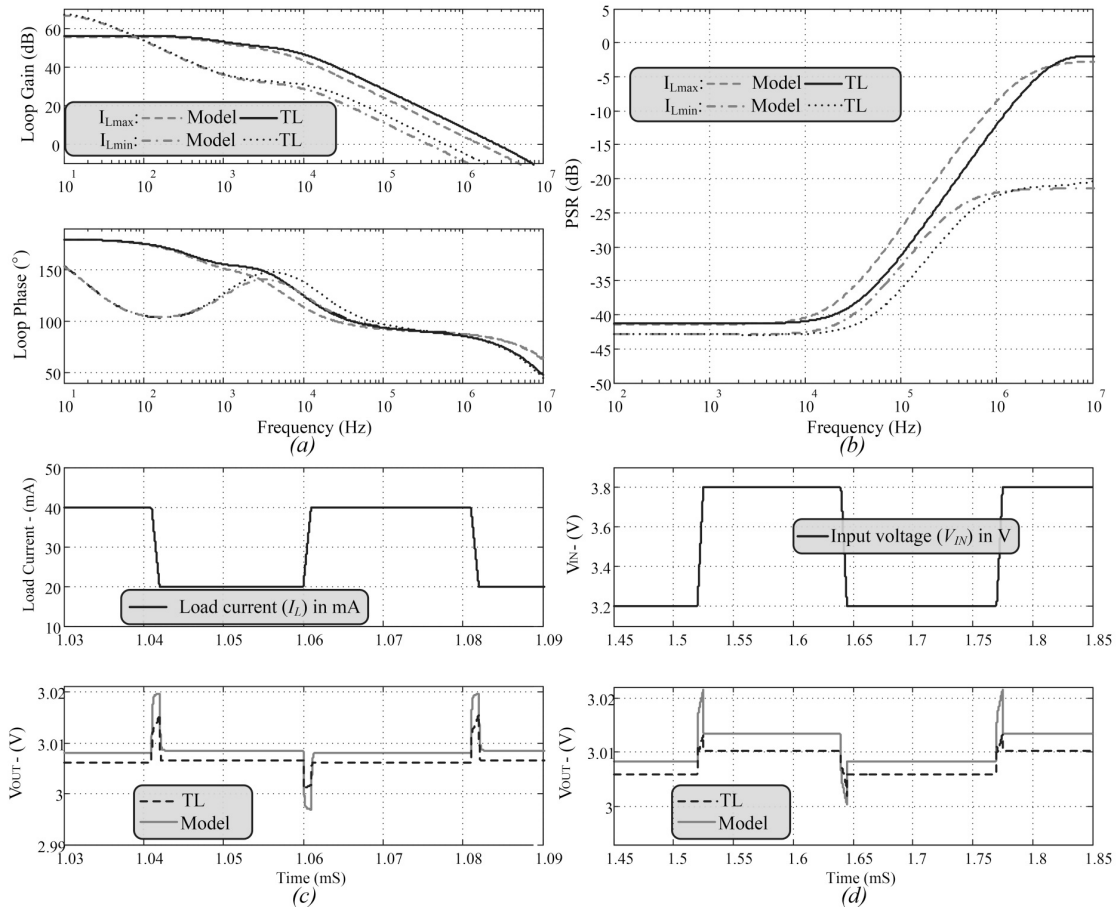
Fig. 24. Responses of the Fig. 10 TL LDO and model during: a) STB analysis; b) PSR analysis; c) Load transient analysis: 20-40 mA I_L step: and d) Line transient analysis: 3.2-3.8 V V_IN step.

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Table 2 summarizes the results including the positive ($+\Delta V_{OUT,max}$) and negative ($-\Delta V_{OUT,min}$) spikes during I_L-transient events. Higher order effects due to small parasitic elements, not included in the model, raise small discrepancies mostly at high frequencies. However, there is still a reliable agreement between the model and TL results.

Table 2. Comparison between TL and LDO model for the general LDO structure (Fig. 10).

Analysis	TL-I_{Lmin}/I_{Lmax}	Model-I_{Lmin}/I_{Lmax}	Error-I_{Lmin}/I_{Lmax}
DC-V_{OUT} (V)	3.008/3.006	3.009/3.008	0.001/0.002
STB (Mag-Phase)			
@ DC	(67dB-153°) / (56dB-179.5°)	(66.7dB-153.6°) / (55.4dB-179.5°)	(0.3dB-0.6°) / (0.6dB-0°)
@ HF[a]	(8.4dB-85.6°) / (5.9dB-91°)	(4.2dB-87.5°) / (1.8dB-90.7°)	(4.2dB-1.9°) / (4.1dB-0.3°)
PSR (dB)			
@10 KHz	-42.8 / -40.9	-42.6 / -40.4	0.2 / 0.5
@100 KHz	-36.2 / -31.3	-32.8 / -27.3	3.4 / 4
Load reg. (mV/A)	20.6	24.9	4.3
$+\Delta V_{OUT,max}$ (mV)	9.3	11.7	2.4
$-\Delta V_{OUT,max}$ (mV)	5.6	11.9	6.3
Line reg. (mV/V)	7.34	8.53	1.19
$+\Delta V_{OUT,max}$ (mV)	2.9	8.1	5.2
$-\Delta V_{OUT,max}$ (mV)	4	8	4

[a] Measured at 0.3 MHz and 1 MHz for I_{Lmin} and I_{Lmax}, respectively

2.4.2 Model for a high PSR LDO

The LDO in Fig. 22a [25] includes a feedforward stage (FFS) to improve PSR. Its EA path consists of amplifiers LA, SA and resistors $R_{S1\text{-}3}$. The FFS is formed by amplifier FFA and $R_{ff1,2}$-C_{ff1}. The TL LDO in Fig. 22a is designed in 0.6 μm CMOS for 1-50 mA I_L, 3.0/2.8 V_{IN}/V_{OUT} ratio and 2.5 MHz maximum f_u. In the model, M_P is polynomially represented as in Fig. 17 and passive elements model β and FCS. The EA and FFS are

independently AC-characterized and described using the Fig. 19 model. Table 3 summarizes the results of the analyses performed on the Fig. 22a LDO model. The differences between TL LDO and model responses are negligible at low frequency and slightly increase at higher frequencies. The number of time constants in the EA/FCS models can be increased to further reduce the high frequency errors if required.

Table 3. Comparison between TL and model for an LDO with FF-stage [25].

Analysis	TL-I_{Lmin}/I_{Lmax}	Model-I_{Lmin}/I_{Lmax}	Error-I_{Lmin}/I_{Lmax}
DC-V_{OUT} (V)	2.806/2.806	2.806/2.806	< 0.001/ <0.001
STB (Mag-Phase)			
@ DC	(76.4dB-153°) / (62.4dB-180°)	(74.5dB-153.5°) / (62.3dB-180°)	(1.9dB-0.5°) / (0.1dB-0°)
@ HF[a]	(1.1dB-88.4°) / (4.3dB-70.3°)	(1.3dB-88.1°) / (2dB-75.2°)	(0.2dB-0.3°) / (2.3dB-4.9°)
PSR (dB)			
@100 KHz	-43.2 / -64.6	-44.3 / -65.5	1.1 / 0.9
@1 MHz	-37 / -26.5	-35.1 / -29.6	1.9 / 3.1
Load reg. (mV/A)	8.7	4.5	4.2
+Δ$V_{OUT,max}$ (mV)	5.8	7.5	1.7
-Δ$V_{OUT,max}$ (mV)	5.2	6.7	1.5
Line reg. (mV/V)	1.25	1.73	0.48
+Δ$V_{OUT,max}$ (mV)	5.2	4.8	0.4
-Δ$V_{OUT,max}$ (mV)	2.8	4.9	2.1

[a] Measured at 80 KHz and 1 MHz for I_{Lmin} and I_{Lmax}, respectively

2.4.3   Model for a fast transient LDO

In the LDO in Fig. 22b [27], C_{f1} and current amplifier (CA) act as active, on-chip FCS and V_{OUT} transient detector. The LDO in Fig. 22b was designed and fabricated in 0.6 μm CMOS for a 0.1-50 mA I_L, 3.0/2.8 V_{IN}/ V_{OUT} ratio and ~500 kHz f_u.

To approximate the experimental results of the fabricated LDO, the effects of additional parasitic elements (metal routing and chip finishing) must be included in the model. Thus, the characterization data was extracted from the post-layout LDO view. This can be done segmenting the LDO layout such that inner nodes can be probed (e.g. V_{EA}). Using these data, M_P is polynomially described as in Fig. 17 and β is modelled with $R_{1,2}$ and C_{f2}. To model the FCS and EA, two AC analyses are required for independent characterization. The loops are opened (one at a time) and an AC test signal is injected at the near end (x for EA and y for FCS in Fig. 22b). Using the collected frequency responses, both EA and FCS can be modelled with the selected amplifier model.

Table 4 summarizes the performances of the post-layout version of the Fig. 22b LDO, its model and experimental results. The model shows errors below 2 dB and 1° in the PSR and STB analyses when compared against both post-layout and experimental results (PSR) up to 500 kHz (STB). Due to independent EA and FCS modelling, the model's responses to load and line regulation tests show good correlation with post-layout results (mV-range errors). Also against post-layout results, the errors in the V_{OUT} spikes after a load transient round the 10%, providing a good estimate of the LDO performance. Conversely, due to un-modelled parasitic elements of the test board, chip package and measurement equipment connectors, the model's load regulation error against experimental results is of one order of magnitude. This performance is expected since the data used to generate the model was obtained from a post-layout level characterization, against which the model observes remarkable resemblance.

Table 4. Comparison between post-layout, model and measurements for an LDO with active FCS [27].

Analysis	PostLayout-I_{Lmin}/I_{Lmax}	Model-I_{Lmin}/I_{Lmax}	Error-I_{Lmin}/I_{Lmax}	Measurement-I_{Lmin}/I_{Lmax}
DC-V_{OUT} (V)	2.806/2.803	2.807/2.806	0.001/ 0.003	2.819 / 2.775
STB (Mag-Phase)				
@ DC	(65.9dB-178.1°) / (50.1dB-179.5°)	(65.1dB-178.5°) / (51dB-179.3°)	(0.8dB-0.4°) / (0.9dB-0.2°)	n/a
@ HF[a]	(1.8dB-78.8°) / (3.2dB-86.6°)	(3dB-77.3°) / (1.1dB-86.7°)	(1.2dB-0.5°) / (2.1dB-0.1°)	n/a
PSR (dB)				
@10 KHz	-43.6 / -35	-42.5 / -34.5	1.1 / 0.5	-42 / -36
@100 KHz	-24 / -15.3	-22.9 / -14.8	1.1 / 0.5	-22 / -16
Load reg. (mV/mA)	0.08	0.06	0.02	0.902
+$\Delta V_{OUT,max}$ (mV)	197	208	11	281
-$\Delta V_{OUT,max}$ (V)	0.512	0.487	0.025	1.207
Line reg. (V/V)	0.002	0.004	0.002	0.003
+$\Delta V_{OUT,max}$ (mV)	97	103	6	209
-$\Delta V_{OUT,max}$ (mV)	96	107	11	428

[a] Measured at 0.5 MHz and 0.35 MHz for I_{Lmin} and I_{Lmax}, respectively

The feasibility of applying the proposed model to LDO structures with off-chip or on-chip FCS and with enhanced features [25, 27], showcases the generality of our approach. Moreover, while the case studies are designed in 0.6 μm, the core principles of the simulation-based model enable its use in nanometric technologies. Admittedly, the model's complexity in terms of the number of time constants to be included in the EA and FCS models correspondingly increases to reflect the high frequency characteristics of an LDO in advanced processes. Thus, the additional complexity during circuit modelling is unavoidable if the high performance (i.e. wide bandwidth) of a nanometric LDO is to be reflected in the model.

Furthermore, considerations such as flicker noise or loop gain might steer designers away from using minimum length transistors in the EA and FCS [24, 45]. Thus, an LDO in advanced processes does not necessary use the minimum available length

(except for M_P), which partially dampens the technology-dependent modelling complications.

2.5 Simulation time comparison

A testbench with multiple LDOs is used to compare the simulation times of the Fig. 10 TL LDO and its 5th order model. A transient analysis is used to replicate the scenario where the load repeatedly demands current from LDOs of the general structure. Each LDO is subjected to 100 I_{Lmax}-I_{Lmin}-I_{Lmax} steps with a 10-μs period. Depending on the number of LDOs in the testbench, the model reduces the simulation time by 2 to 4 times (Fig. 25a). Moreover, in the case of a DC bias point analysis (Fig. 25b) the model reduces simulation time by nearly 10 times. Fig. 25c shows the simulation time reduction factor per analysis when the Fig. 25b LDO 5th order model is compared with its TL (schematic) and post-layout counterparts. The testbench applied simultaneous stimulus to 100 LDOs. The time reduction ranges from 1 to ~9 times versus the schematic case; and between 10 to 110 times versus the post-layout case. The simulation time reduction provided by the model increases with the complexity of the TL LDO and the benefits are greater when the model replaces the extracted version of an LDO in a larger testbench.
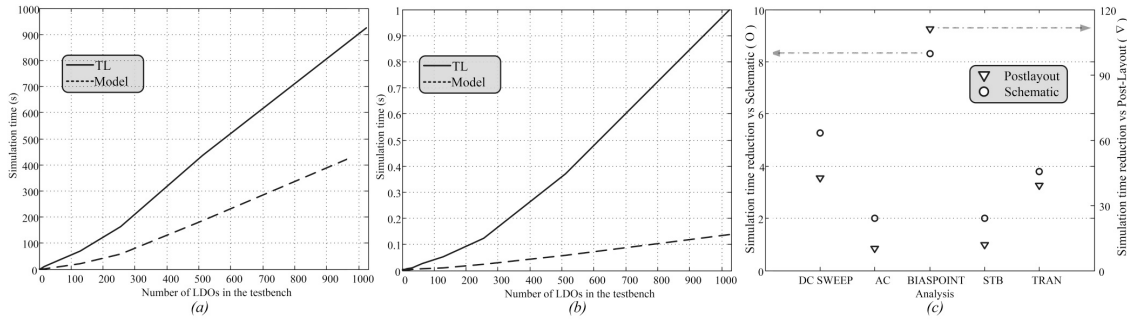
Fig. 25. Simulation time comparison for: a) TL and model for the Fig. 10 LDO during a transient analysis; b) TL and model for the Fig. 10 LDO during a bias point analysis; c) Simulation time reduction factor per analysis for the Fig. 22a LDO model versus its schematic and postlayout counterparts.

While comparing the simulation time reduction factors of different LDO models is complex due to the different testbenches in which they are simulated, Table 5 qualitatively compares the proposed model against other previously reported models for linear regulators. From this comparison table, it is possible to conclude that the proposed model is among the most complete in terms of applicability to multiple LDO structures, acting as a self-contained model, and reproducing time-domain analysis; all of this while avoiding the use of additional hardware description languages.

Table 5. Qualitative comparison for the features of several LDO models.

Reference	[18]	[19]	[20]	[21]	Generic	This work
Approach	VCVS+ transistor	VCVS+ transistor	Verilog-A	TF+QZ algorithm	TF-based	Polynomial
Multiple LDO structures	No	No	Yes	Yes	Yes	Yes
Time-domain analysis	Yes	No	Yes	No	No	Yes
Self-contained	No	No	Yes	Yes	Yes	Yes

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2.6   Conclusion

This chapter discussed a comprehensive LDO model capable of approximating the small and large signal LDO behaviors. The model describes in detail the LDO using a combination of nonlinear polynomials, voltage and current controlled-sources and passive elements. Due to its SPICE-oriented nature, the model exclusively uses SPICE elements, which makes it portable, flexible and easy to construct. A wide range of externally and internally compensated LDO structures can be accurately represented using the model. The model construction was detailed for three LDO structures with contrasting characteristics: a basic, fast transient and high PSR topologies. The performance of the models shows good agreement with that of the transistor level LDOs. Furthermore, a comparison of the model versus experimental results is also included for the fast transient structure. The model provides LDO-structure and analysis-dependent simulation time reduction factors from 2x to 10x with respect to schematic-level and from 10x to 110x with respect to post-layout SPICE simulation. The model also provides design insights that are generally hard to acquire directly from the transistor level circuit and offers an accurate alternative for verification of systems with extensive use of LDOs.

CHAPTER III

A POWER MANAGEMENT UNIT WITH 40 dB SWITCHING-NOISE-SUPPRESSION FOR A THERMAL HARVESTING ARRAY[*]

A high efficiency, maximum power point tracking (MPPT) Power Management Unit (PMU), with 3.6 µW quiescent power, aimed at a thermoelectric generator (TEG) array is presented. The proposed energy harvesting PMU is made up of a boost converter with a cascaded capacitor-less low drop-out (CL-LDO) voltage regulator. The segmented approach allows the PMU to match the TEG array's changing dynamic series resistance via the boost converter and simultaneously provide voltage regulation with adaptive, high switching noise rejection via the CL-LDO. The boost converter's switching frequency (f_{sw}) is tracked via a sense-and-control loop which modifies the CL-LDO's power supply rejection (PSR) characteristics to place a notch in the PSR transfer function around the average f_{sw}. Experimental results show an overall system efficiency better than 57% @ 1.6 V output voltage, PSR of 40dB at f_{sw}, and a notch-tuning range of 15-65 kHz. The total active area is 0.93 mm^2 in 0.5 µm CMOS.

3.1   Introduction

Integrated systems designed to fulfill the sensing and communications needs of medical implantable systems and wireless sensor networks or Internet of Things (IoT) applications have experienced a rapid evolution in recent years [46-50]. To keep up with the progress made in such advanced systems, similar development and improvement in compact energy sources and power management units (PMU) capable of meeting the power needs of such devices is required. Energy harvesting (EH) units have emerged as a valuable alternative to either replace or complement the battery-operation of wireless transmitters [51, 52]. In such systems, whether energy is harvested from human [51], RF [52], solar [53], vibrational [54], thermal [4], or multiple sources [55-57], reducing the intrinsic power consumption of the EH-PMU is critical for an efficient solution.

In addition to transferring most of the harvested energy to the load while consuming minimum power, there are other challenges the EH-PMU has to simultaneously meet. Such challenges include: maintaining a constant output voltage despite variations on the source conditions (adaptive input-to-output voltage gain); and ideally, providing a clean and regulated output voltage under different load conditions. Due to their high efficiency and intrinsic use of energy storage passive elements, most EH-PMUs use either inductor-based switching regulators [58] or switch-capacitor converters [59] to interface the EH transducer with the output load. However, due to the constant switching involved, these solutions tend to introduce large voltage ripple at the

output. Although using super/ultra-capacitors alleviates the ripple problem, such devices largely impact the bill-of-materials (BOM) cost and board area.

This dissertation introduces an EH-PMU capable of extracting maximum power from a 3x3 thermoelectric generator (TEG) array via a boost converter with input resistance tracking capability. Furthermore, a low power, capacitor-less low-dropout voltage regulator (CL-LDO) cascaded with the boost converter acts as a ripple-reduction mechanism, providing high switching-noise-suppression to the output regulated voltage.
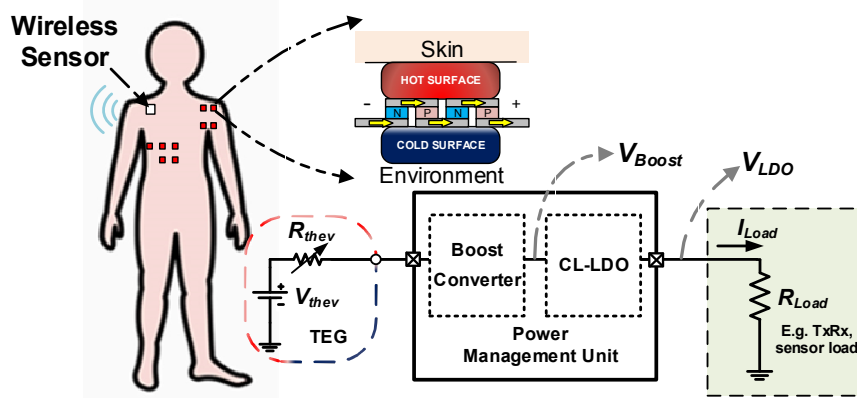
Fig. 26. Proposed EH-PMU implementation in a medical application setting.

The proposed EH-PMU is suitable for operation in a medical application setting as the one illustrated in Fig. 26. Micropelt's MPG-DG655 TEG unit modules [60] are used to build a 3x3 array (electrically modeled with the R_{thev}, V_{thev} Thevenin equivalent). Taking advantage of a skin-environment temperature gradient ranging between 0.23-2.1°C, the array is able to produce a V_{thev} of ~200 mV while adopting configurations from all-parallel to all-series unit elements. Whilst V_{thev} can be maintained almost constant via array

reconfiguration, the values for R_{thev} range between 19 Ω to 1.53 kΩ (due to unit TEG module resistance of 170 Ω). The boost converter uses V_{thev} as its input voltage and produces a higher voltage, V_{Boost}, which is adequate to power CMOS circuitry. A CL-LDO cascaded with the boost converter uses V_{Boost} as input to generate its regulated, cleaner version (V_{LDO}). Though the better quality V_{LDO} is the EH-PMU primary output, V_{Boost} is also available as a secondary output voltage.

3.2   Energy harvesting power management unit

In addition to low intrinsic power consumption, for an EH-PMU to be truly viable as a standalone or complementary energy source for noise sensitive blocks, it should: *a)* Extract maximum power from the EH source; and *b)* Deliver a CMOS compatible, clean, regulated output voltage. To meet these requirements, the proposed low-power EH-PMU (Fig. 27) uses a boost DC-DC switching converter as front-end and a CL-LDO as back-end. The boost converter applies a maximum power point tracking (MPPT) technique at the interface with the TEG array, achieving optimum energy extraction while conditioning the EH-PMU internal voltage levels.
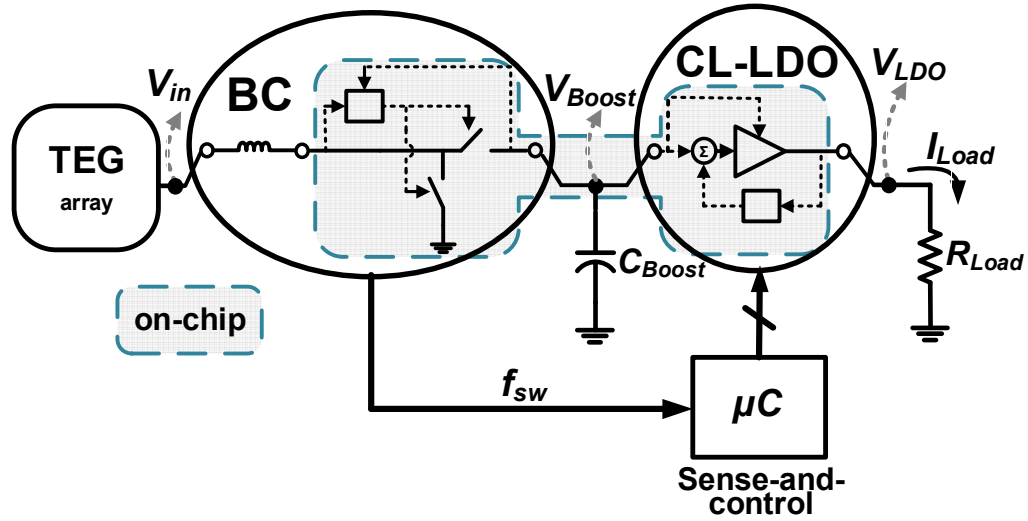
Fig. 27. EH-PMU for a TEG array using a boost converter and a CL-LDO.

The front-end boost converter brings V_{thev} to usable –higher– CMOS levels at its output V_{Boost} (1.8 V). However, demanding voltage regulation and reduced voltage ripple from the front-end, increases the burden and complexity on the boost converter, which translates in a power hungry boost converter controller and a low system efficiency. Conversely, using a cascaded CL-LDO provides superior ripple rejection and a steady and regulated output voltage (V_{LDO}, 1.6 V) to the EH-PMU load. The supply-noise-rejecting capabilities of the proposed CL-LDO come from programmable notch-like characteristics in its supply-to-output path. Furthermore, the ultra-low power consumption of the CL-LDO yields high efficiency. Leveraging the superior switching-noise suppression of the CL-LDO, it is possible for our EH-PMU to use an off-chip capacitor C_{Boost} in the order of nF. While replacing the supercapacitor [54] with a nF-C_{Boost} reduces the long-term energy storage capabilities, it also considerably reduces the board area and bill-of-materials

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expenses. In turn, the regulated output voltage at V_{LDO} is an inexpensive solution, suitable for loads with low supply-ripple and low current requirements [49, 50].

To complement the EH-PMU, a Sense-and-Control (SaC) loop is implemented using an external microcontroller. The SaC determines the boost converter average switching frequency ($\overline{f_{sw}}$) and generates tuning signals for the CL-LDO to place a notch around $\overline{f_{sw}}$. As a result, significant ripple reduction at the EH-PMU output is obtained and experimentally demonstrated.

3.3   Energy harvesting power management unit front-end

The EH-PMU front-end uses the boost converter shown in Fig. 28, which employs zero current switching (ZCS) and MPPT techniques to improve its efficiency. As suggested in [4, 61], MPPT is achieved by matching the resistance of the source (TEG array, R_{thev}) to the input resistance of the harvester (R_{in}). In Fig. 28, the MPPT loop modulates the switching frequency (f_{sw}) of the boost converter until the $R_{in} \approx R_{thev}$ condition is reached.
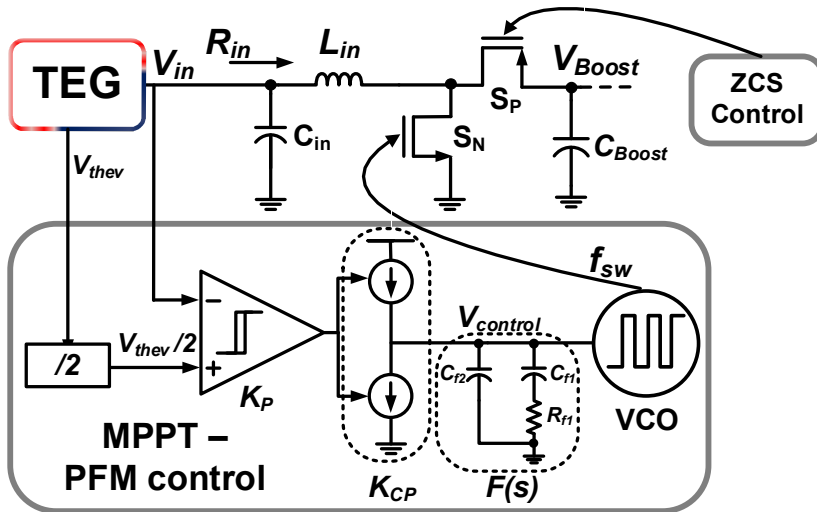
Fig. 28. Implemented Boost Converter with MPPT and ZCS schemes.

It is during each reconfiguration event within the TEG array that the boost converter must quickly and accurately track and match the new R_{thev} value to ensure continuous maximum power transfer from the array. Once R_{in} has been matched to R_{thev}, the input voltage for the boost converter settles at half the TEG array open circuit voltage $V_{thev}/2$, indicating that the maximum point for power (MPP) transfer has been reached. Thus, following the MPP under R_{thev} changes due to TEG array reconfiguration requires a dynamic MPPT scheme.

For comparison purposes, the $V_{thev}/2$ threshold is obtained through a capacitive divider [4] (Fig. 29). During phase φ_1 the TEG-boost converter connection is opened and V_{thev} is sampled into capacitor C_{s1}. Later, during φ_2, the TEG-boost converter connection is restored and C_{s1} is connected in parallel with C_{s2}. Through charge redistribution, the voltage developed in both C_{s1} and C_{s2} is now equal to $V_{thev}/2$ (provided $C_{s1} = C_{s2}$).

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3.3.1   Input resistance matching

As mentioned in chapter 3.1, the TEG array modules can reconfigure their interconnections to take advantage of different temperature gradients naturally available throughout the human body to increase overall system power extraction. For the proposed 3x3 array, the two major scenarios that take into consideration the best/worst case power conditions are the fully parallel and fully series connections of the array, respectively. The design of the EH-PMU was aimed at voltages ranging from 50 mV to 200 mV, which are voltages delivered by a single TEG module under a temperature gradient of approximately 0.23°C to 2.1°C.

The series-parallel connection of the TEG array leads to an R_{thev} ranging from 1.53 kΩ to 19 Ω for the series and parallel configurations, respectively. For the design of the boost converter, Discontinuous Conduction Mode (DCM) was selected due to the low power nature of the application and in order to maintain power consumption to a minimum. For DCM operation, [62] shows that R_{in} can be approximated to:

$$R_{in} \approx \frac{2L_{in}f_{sw}}{D_{NMOS}^2} \tag{17}$$

In (17), L_{in}, f_{sw}, and D_{NMOS} are the input inductor value, switching frequency of the boost converter, and duty cycle of the control signal of NMOS switch S_N; all in reference to Fig. 28. This prompts the use of a Pulse Frequency Modulation (PFM) scheme to control R_{in}. Although both D_{NMOS} and f_{sw} are capable of modulating R_{in}, the R_{in}-quadratic dependency on D_{NMOS} requires a highly precise and power hungry control scheme. Hence,

f_{sw} is selected as the control variable to maintain a linear control of R_{in} by setting the value of D_{NMOS} at 50% of the switching period.
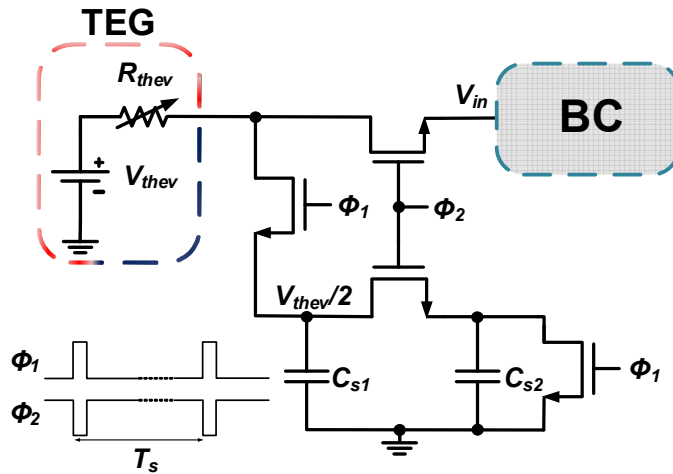
Fig. 29. Capacitive divider for $V_{thev}/2$ extraction [4].

A second approach to minimize power consumption by the boost converter was to restrict the f_{sw} range over which the converter will operate to low values. This reduces the total dynamic power consumption for the system. Choosing a 5 mH inductor as L_{in} sets the value of f_{sw} to vary from ~38 kHz to ~500 Hz for the required R_{thev} values to match. While this L_{in} value might seem high, it is not uncommon for integrated energy harvesting systems to use off-chip inductors with similar or higher values [63]. In our case, the selected L_{in} value allows successful operation using low switching frequencies, which in turn reduces the overall power consumption and maximizes the global efficiency.

3.3.2 Maximum power point tracking loop

As described in [4], the MPPT scheme possesses a matching range over which the system can assure maximum power extraction. The MPPT scheme allows for rapid maximum power extraction when changes occur on the equivalent R_{thev}. Similar to a Phase Locked Loop (PLL), loop stability is a primary concern in order to avoid unstable responses from the system when an R_{thev} change occurs.

The block diagram in Fig. 30 presents the small-signal model that makes up the MPPT system of Fig. 28, where $V_{thev}/2$ and V_{in} are the halved open circuit voltage of the TEG array and the input voltage of the boost converter, correspondingly. The variables K_P, K_{CP}, $F(s)$, and $H_{c\text{-}in}(s)$ are the linear gain of the comparator, charge pump bias current, filter transfer function, and control-to-input transfer function for the boost converter, respectively. Hence, the open loop transfer function of the complete MPPT loop is given by:

$$TF_{OL}(s) = K_P K_{CP} F(s) H_{c-in}(s) \tag{18}$$

The control-to-input transfer function, $H_{c\text{-}in}(s)$, is obtained following [62]. Assuming steady-state operation, both the input source (V_{thev}) and the boost converter output voltage (V_{Boost}) can be presumed to be AC ground during the small-signal analysis due to the 10 nF C_{Boost}. Under these assumptions, the small-signal model shown in Fig. 30 is used to analyze the MPPT loop stability. The parameters j_1 and r_1, (Fig. 30) are obtained via three dimensional Taylor series expansions of the average input and output voltages

and duty cycle [64] at steady-state operation. The variable $V_{control}$, seen in both Fig. 28 and Fig. 30, is the VCO control voltage coming from the filter block, $F(s)$.
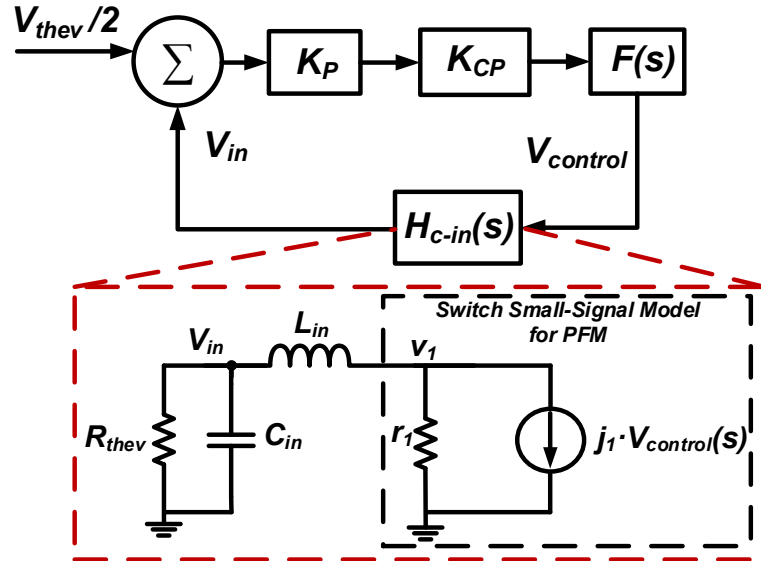
Fig. 30. Control loop and equivalent small-signal model for PFM boost converter.

Using the simplified model of Fig. 30, the $H_{c-in}(s)$ transfer function includes the effect of the VCO linear gain and yields (19), where the natural frequency and damping are given by (20) and (21), respectively.

$$H_{c-in}(s) = \frac{V_{in}(s)}{V_{control}(s)} = \frac{\frac{j_1 r_1}{L_{in}C_{in}}}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{19}$$

$$\omega_o = \sqrt{\frac{R_{thev} + r_1}{L_{in}C_{in}R_{thev}}} \tag{20}$$

$$\xi = \frac{(L_{in} + C_{in}R_{thev}r_1)}{2\sqrt{(C_{in}L_{in}R_{thev})(R_{thev} + r_1)}} \tag{21}$$

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Extending the charge-pump-based PLL analogy, an external, second order passive loop filter $F(s)$ formed by capacitors $C_{f1,2}$ and resistor R_{f1} (Fig. 28) is used to enhance the MPPT loop response. In this case, (18) becomes:

$$TF_{OL}(s) = \frac{K_p K_{CP}(sC_{f1}R_{f1} + 1)H_{c-in}(s)}{(C_{f1} + C_{f2})s(s(C_{f1}||C_{f2})R_{f1} + 1)} \tag{22}$$

Assuming a V_{in} of 100 mV, with C_{f1} of 100 nF, C_{f2} of 10 nF, and R_{f1} of 500 Ω, for a $K_P \approx 80$ dB, and K_{CP} of 100 nA (charge pump current [65]); in the mid-value of R_{thev} (775 Ω), the MPPT loop has unity gain frequency (UGF) of 2 kHz, and phase margin (PM) of 88°. Thus, a second order $F(s)$ allows for a stable system response over a wide range of equivalent resistance values (R_{thev}) and a rapid response after a TEG array reconfiguration.

3.3.3   Zero current switching scheme

Reducing stress on monolithic components and improving efficiency are important goals for any switching converter to reach. In order to address both these issues, a zero current switching (ZCS) technique is employed. The ZCS scheme shown in Fig. 31 minimizes the inductor current losses through the PMOS switch, S_P, and is implemented following [66]. The ZCS is performed via a skewed voltage peak detector in the V_{sw} node. This voltage is next compared to a fixed reference, V_{zref}. The comparison result is used to generate voltage V_{c2}, which eventually regulates the on/off time of S_P (Fig. 31), reducing the inductor current losses.
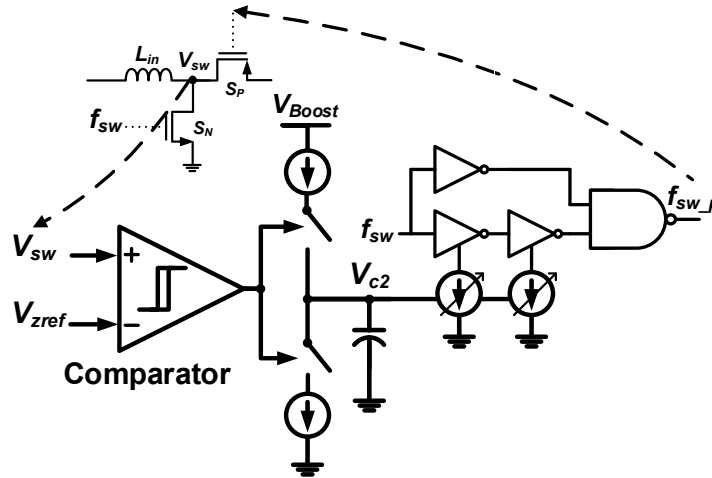
Fig. 31. Zero Current Switching Tracking loop implementation [66].

As discussed in [58], when S_P is turned off and L_{in}'s current has not been fully delivered, an associated voltage surge is perceived at V_{sw}. This voltage surge is proportional to the rate of change of the remaining current in L_{in} when S_P is off. Ideally the inductor current would fall to zero before the PMOS is switched off, thus, reducing any losses associated with this switch. A dynamic Zero Current Switching Tracking (ZCST) loop [66] is implemented to minimize the potential losses associated with negative inductor current.

3.4 Energy harvesting power management unit back-end

Even though the EH-PMU front-end successfully performs MPPT from the TEG harvester and develops an output voltage V_{Boost} sufficiently high to drive low power circuits, V_{Boost} exhibits a large voltage ripple. Thus, directly using V_{Boost} to power electronic circuits might lead to unacceptable performance or failure of the energy-

recipient circuits, particularly in the case of circuits with high supply-noise sensitivity. The proposed EH-PMU incorporates an LDO as its back-end to solve this problem. Although using an LDO to reduce the ripple in V_{Boost} and produce a quiet voltage, V_{LDO}, might seem as a straightforward solution; the high end-to-end efficiency expected from the EH-PMU limits the power that can be used to design a high performance LDO. Furthermore, to reduce the cost of the required external components of the solution, a capacitor-less LDO (CL-LDO) is used.

For the CL-LDO in the EH-PMU back-end to successfully attenuate the magnitude of the ripple in V_{Boost}, the CL-LDO should possess high power supply rejection (PSR) at and around the ripple frequency (f_{sw}). Multiple CL-LDO advanced structures with notorious PSR improvements have been recently proposed [67-71]. However, most of these works report current consumptions from several to a few hundreds of μA and are designed to deliver load currents between 20 to 100 mA. Nonetheless, in the case of a CL-LDO targeted for EH applications, the available current to deliver to the load might be scarce and dependent on the conditions surrounding the EH transducer (thermal gradient between the TEG plates). Thus, investing even ten μA to get a well-regulated and ripple-reduced output voltage represents a major cut to the available current to be delivered to the load, and can seriously harm the end-to-end system's efficiency. Thus, to reduce the CL-LDO complexity and quiescent current, it is convenient to analyze the basic CL-LDO structure of Fig. 32 to determine its fundamental PSR limits.

3.4.1 Basic CL-LDO

In the CL-LDO of Fig. 32, the error amplifier (EA) is assumed to be a single stage differential pair amplifier; the pass transistor (M_P) is a PMOS device with parasitic gate-to-source, gate-to-drain, and gate-to-bulk capacitances, C_{gs}, C_{gd}, and C_{gb}, respectively; resistors R_{1-2} form a feedback voltage divider, $\beta = R_2/(R_2+R_1)$; and V_{ref} is selected such that $V_{out} \approx \beta V_{ref}$ (assuming large loop gain). The load is modeled by resistor R_L and capacitor C_L (to account for the load *parasitic* capacitance and/or a small on-chip capacitance).
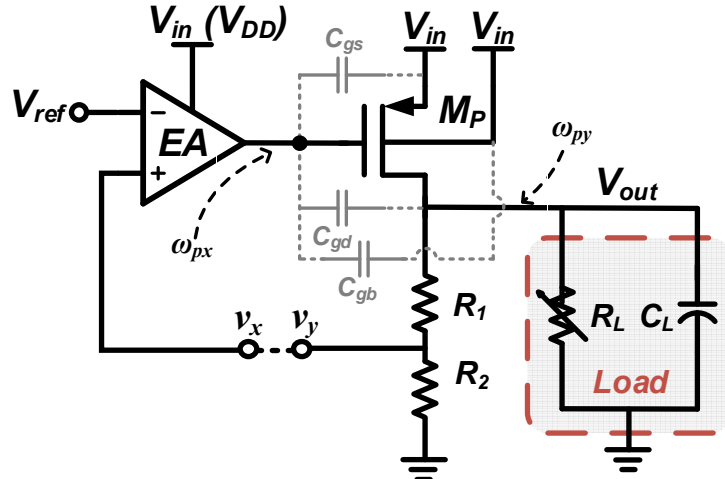
Fig. 32. Simple CL-LDO structure.

The open loop gain of the CL-LDO in Fig. 32 –$LG(s)$, evaluated from v_x to v_y– is given by (23). $LG(s)$ contains two poles (ω_{px} and ω_{py}) and one zero (ω_z). A_{EA} and A_{MP} represent the DC voltage gain of the EA and M_P, respectively. To approximate the locations of the poles (24) and zero (25), it is assumed that *a)* C_L is due to the supply-line

capacitance of the load circuit and/or explicit on-chip decoupling capacitance, thus, C_L amounts to only a few pF (e.g. $C_L \leq 10$ pF); and *b)* The EA output conductance, g_{oE}, is smaller than the total output conductance, g_{OUT}, formed by g_L ($1/R_L$) and the M_P conductance, g_{oMP} (i.e. $g_{oE} < g_{OUT}$, with $g_{OUT} = g_L + g_{oMP}$). In (24)-(25), C_p stands for the total equivalent M_P's gate parasitic capacitance (i.e. From Fig. 32, $C_p \approx C_{gs} + C_{gb}$), and gm_{MP} denotes the M_P transconductance.

$$LG(s) = A_{EA}(s)A_{MP}(s)\beta = \frac{A_{EA}A_{MP}\beta(s/\omega_z - 1)}{(s/\omega_{px} + 1)(s/\omega_{py} + 1)} \tag{23}$$

$$\omega_{px} \approx \frac{g_{oEA}}{A_{MP}C_{gd}}, \quad \omega_{py} \approx \frac{g_{OUT}(C_p/C_{gd} + 1) + gm_{MP}}{(C_p/C_{gd} + 1)C_L + C_p} \tag{24}$$

$$\omega_z \approx \frac{gm_{MP}}{C_{gd}} \tag{25}$$

The approximations for ω_{px} (typically the dominant pole) and ω_z are consistent with the expressions found in previous works [27]. However, due to the low I_L in our application, the gm_{MP} and g_{oMP} values might have similar magnitudes. Thus, a detailed expression for ω_{py} is provided in (24). As expected, satisfactory phase margin and loop stability can only be achieved if enough separation exists between ω_{px} and ω_{py} for all I_L of interest. Assuming a C_p/C_{gd} ratio > 4 for the process used (0.5 µm) [72], a maximum C_L of 10 pF, a C_{gd} in the order of 2 pF (M_P is small due to the low I_L), A_{MP} of ~30 dB, the denominator of ω_{px} is only slightly larger than the denominator of ω_{py}. Similarly, the numerator of ω_{px} is at least 2 to 3 times smaller than the numerator of ω_{py} (again, due to low I_L). According to our assumptions, ω_{px} is indeed at lower frequency than ω_{py}, however, the two poles might not be adequately spaced to guarantee loop stability (depending on

the total loop gain). In this case, loop stability can be achieved using Miller compensation at expense of reduced gain-bandwidth product (GBW) and increased power consumption.

Similarly, the PSR of the CL-LDO in Fig. 32 is given in (26), with its DC value determined by the loop gain ($A_{EA}A_{MP}\beta$). *PSR(s)* has two zeros ($\omega_{zPSR1} < \omega_{zPSR2}$) and two poles ($\omega_{pPSR1} < \omega_{pPSR2}$) which are approximated in (27) and (28), respectively. Analyzing (26), it can be concluded that the DC PSR of the CL-LDO starts to degrade at ω_{zPSR1} (lowest frequency zero in (26)) and that in order to improve the PSR performance, ω_{zPSR1} should be pushed to higher frequencies. Unfortunately this solution generally entails increased power consumption, which cannot be tolerated in a CL-LDO for low power EH applications.

$$PSR(s) = \frac{1}{A_{EA}A_{MP}\beta} \frac{(s/\omega_{zPSR1} + 1)(s/\omega_{zPSR2} + 1)}{(s/\omega_{pPSR1} + 1)(s/\omega_{pPSR2} + 1)} \tag{26}$$

$$\omega_{zPSR1} \approx \frac{g_{oEA}}{A_{MP}C_{gd}}, \qquad \omega_{zPSR2} \approx \frac{gm_{MP}}{C_p} \tag{27}$$

$$\omega_{pPSR1} \approx \frac{gm_{EA}}{C_{gd}}, \qquad \omega_{pPSR2} \approx \frac{gm_{MP}}{C_L\left(1+\frac{C_p}{C_{gd}}\right)+C_p} \tag{28}$$

Nonetheless, it is interesting to note that ω_{zPSR1} in *PSR(s)* and ω_{px} in *LG(s)* share the same expression. This means that the pole at the gate of M_P in *LG(s)* is reflected as a zero in *PSR(s)* (due to the closed loop shaping action). This fact will be later recalled as the basis of the proposed PSR enhancement technique.

3.4.2   Proposed CL-LDO

In the two-stage EH-PMU, the ripple noise present at V_{Boost} (front-end-output/back-end-input) exhibits the strongest components at and around the switching frequency (f_{sw}). This localized noise nature suggests that it is not strictly necessary for the CL-LDO to exhibit uniformly high PSR across the frequency spectrum (from DC through f_{sw}), and as long as the PSR at f_{sw} is adequate, most of the switching noise at V_{Boost} will not be present at the PMU output voltage (V_{LDO}). Thus, a low power CL-LDO capable to emphasize its PSR at particular frequencies is implemented as the EH-PMU back-end. For higher flexibility, the CL-LDO PSR characteristics can be modified via a programmable bank of capacitors to reject particular frequencies (f_{sw}) within the range of interest.

One way for the CL-LDO to selectively reject a given f_{sw}, is to make its PSR transfer function to partially resemble a notch filter. If said notch is centered at f_{sw}, the main CL-LDO ripple noise components can be significantly attenuated at the PMU output. This approach is conceptually shown in Fig. 33, by getting rid of the strongest supply-noise component at f_{sw} via the notch in the PSR transfer function, this structure allows to improve the PSR performance of the PMU without using an LDO with high PSR for all frequencies (which in general results in large power consumption).
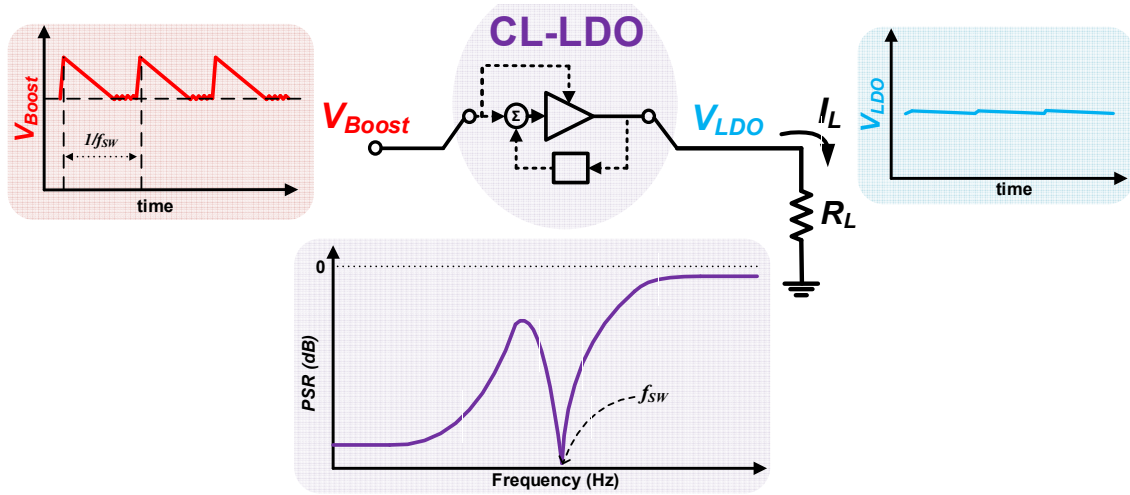
Fig. 33. Conceptual CL-LDO operation.

The concept of using a tunable, continuous time notch/band-reject filter to remove noise at specific, well-identified frequencies has been widely exploited in wireless receivers [73-75]. In such applications, the notch filter can be merged with the low-noise amplifier (LNA) [73] at the receiver front-end to implement either an image rejection filter or to get rid of strong blockers [74]. Notch filtering has also been demonstrated using a broadband resistive feedback LNA with embedded feedforward to improve blocker rejection at third and higher oscillator harmonics [75].

The transfer function $H_{NOTCH}(s)$ of a *generic* second order symmetrical notch filter with input V_{genIN} and output V_{genOUT} is shown in (29) [76].

$$H_{NOTCH}(s) = \frac{V_{genOUT}}{V_{genIN}} = \frac{K(s^2 + \omega_{zN}^2)}{s^2 + (\omega_{oN}/Q_p)s + \omega_{oN}^2} \tag{29}$$

Note that whereas the poles of (29) can be real or complex, the zero-pair ($\pm\omega_{zN}$) is complex. The natural frequency is represented by ω_{oN}, K is the gain in the passband, and Q_p is the quality factor. Thus, to grant notch filter characteristics to the PSR of the CL-

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LDO in Fig. 32, a pair of complex *poles* should be placed at the gate of M_P, such that, due to the loop action, are reflected as complex *zeros* in the PSR transfer function.

Including a notch in the CL-LDO PSR transfer function using techniques similar to the presented in [73-75] is neither straightforward nor convenient. In the case of an LNA with notch filtering, the notch is generally placed at frequencies out of the band of interest (to reject interferers and out-of-band blockers) and the additional phase shift at the notch frequency, $|\omega_{zN}|$, does not affect the correct reception of the transmitted signals within the system bandwidth. However, in the case of the LDO, the loop GBW is maximized (within power budget) to have fast transient response and extended noise suppression. Thus, when the f_{sw} is lower than the LDO GBW, the phase shift due to the required complex poles at the gate of M_P (responsible for generating the notch in the PSR transfer function) might jeopardize the loop stability and render the LDO unstable. For this reason, any modification made to include complex poles at the gate of M_P in the circuit of Fig. 32 should not affect the loop stability.

Consider the circuit of Fig. 34 where the EA of the CL-LDO in Fig. 32 is implemented at the transistor level using an NMOS-input differential pair (M_1-M_2). Shown in a dashed line box in Fig. 34 is an auxiliary circuit used to modify the PSR characteristics of the CL-LDO and simultaneously stabilize the regulator. The auxiliary circuit is composed of transistor M_{CG} (biased via V_{CG} and I_{CG}), a coupling capacitor C_C and a series $R_Z C_Z$ load. Note that the coupling action of C_C enables the interaction of the auxiliary circuit with the v_x-v_y regulation loop, allowing for the M_P bias point to be determined by the regulation loop. To further understand the function of the auxiliary

circuit, the operation of the CL-LDO in Fig. 34 should be analyzed from two different perspectives: circuit stability and PSR.
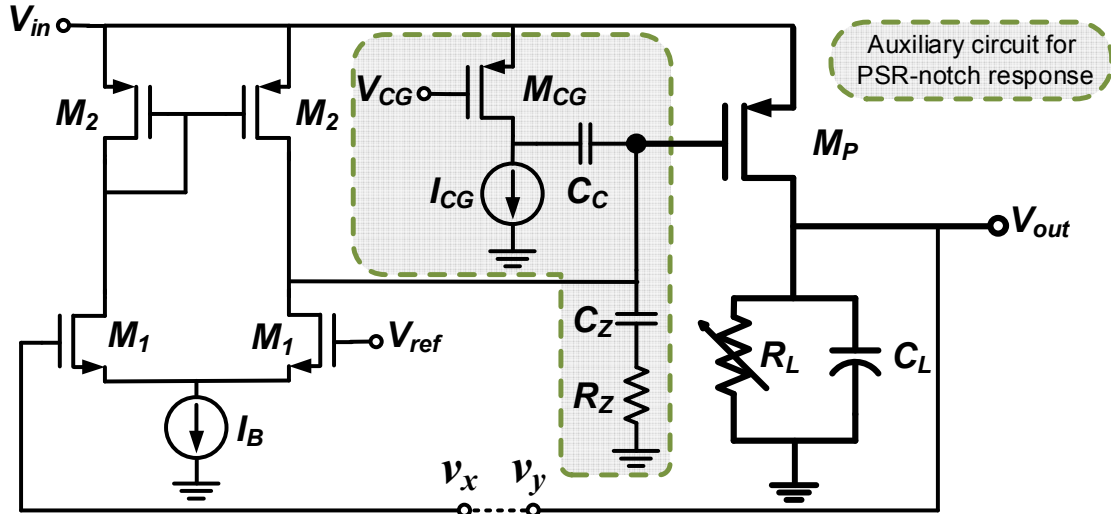
Fig. 34. Transistor-level implementation of the proposed CL-LDO.

3.4.3   CL-LDO stability

If V_{CG} in Fig. 34 is a clean bias voltage, for the v_x-v_y loop-stability purposes the auxiliary circuit appears only as an equivalent passive load. This load is formed by the parallel of the series $R_Z C_Z$ branch and the series $R_{CGEQ} C_C$. While C_C, C_Z and R_Z are passive elements, R_{CGEQ} is the parallel of the M_{CG} output resistance and the output resistance of the current source I_{CG}. This is further illustrated in Fig. 35, where the small signal model of the v_x-v_y loop is shown (note that for this analysis V_{ref} and V_{in} in Fig. 34 are assumed clean voltages -analog ground-). In Fig. 35, g_{mEA} and g_{mMP} represent the transconductances

of the EA and M_P, respectively, g_{oEA} is the EA output conductance, C_{gd} is the gate-to-drain parasitic capacitance of M_P and C_1 is the total parasitic capacitance at the gate of M_P (gate-to-source plus gate-to-bulk parasitic capacitances mainly). The expression for the equivalent admittance of the auxiliary circuit seen in the v_x-v_y loop $-Y_{EQ}-$ is given in (30), where g_z and g_{CGEQ} denote the conductances of R_Z and R_{CGEQ}. The expressions for the zeros ($\omega_{zEQ1,2}$) and pole (ω_{pEQ}) of (30) are given in (31) and (32), respectively.
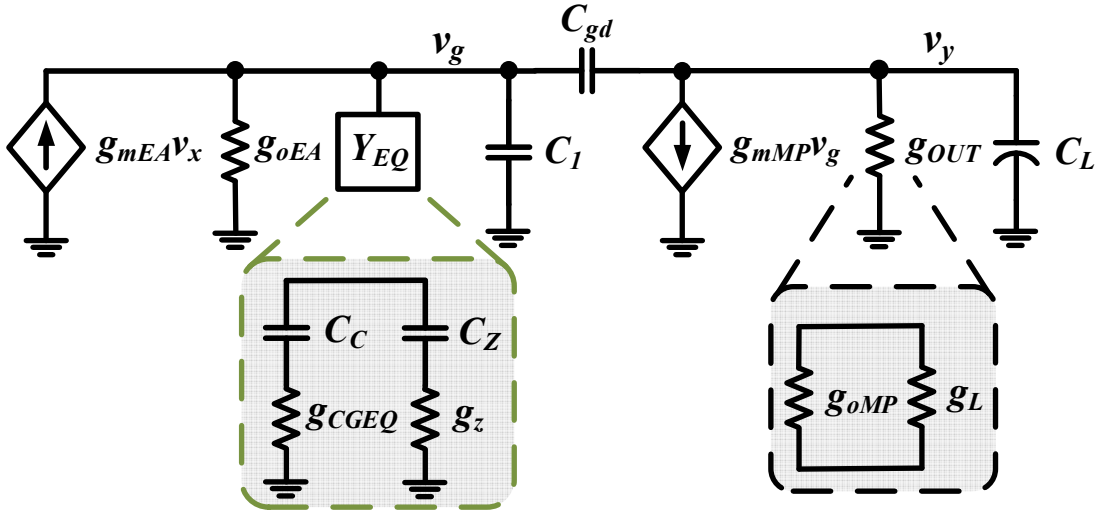
Fig. 35. Small signal open loop model to analyze stability in the proposed CL-LDO.

$$Y_{EQ}^{-1} = Z_{EQ} = \frac{1}{g_z + g_{CGEQ}} \frac{(s + \omega_{zEQ1})(s + \omega_{zEQ2})}{s(s + \omega_{pEQ})} \tag{30}$$

$$\omega_{zEQ1} = \frac{g_{CGEQ}}{C_C} \qquad \omega_{zEQ2} = \frac{g_z}{C_z} \tag{31}$$

$$\omega_{pEQ} = \frac{g_z g_{CGEQ}}{g_z + g_{CGEQ}} \left[\frac{C_z + C_C}{C_z C_C} \right] \tag{32}$$

Using (30), it can be shown that the open loop gain (from v_x to v_y) of the circuit in Fig. 34 can be simplified to (33).

$$\frac{v_y}{v_x} = \frac{-A_{EA}A_{MP}(s + \omega_{zEQ1})(s + \omega_{zEQ2})(s - \omega_{z3})}{(s + \omega_{pST1})(s + \omega_{pST2})(s + \omega_{pST3})(s + \omega_{pST4})} \qquad (33)$$

The loop gain of the proposed CL-LDO (33) has three zeros and four poles. Two of the zeros arise directly from the auxiliary circuit ($\omega_{zEQ1,2}$) and the third zero (ω_{z3}) is the same as the zero in the basic CL-LDO *LG(s)* in (23) (i.e. $\omega_{z3} = \omega_z$ in (25)). Conversely, it is hard to determine useful, closed-form expressions for the poles of (33) unless the following application-specific (low power EH system) assumptions are made: *a)* $C_C > C_Z > C_L$; *b)* M_P provides only low I_L levels, thus C_{gd} and C_1 are both $<< C_Z$; *c)* A_{MP} is low; and *d)* Both EA and M_{CG} operate at low inversion levels, however $g_{CGEQ} < g_{oEA}$ (e.g. $I_{CG} < I_B$ in Fig. 34).

The approximated, design-friendly expressions of the zeros ($\omega_{zEQ1} < \omega_{zEQ2} < \omega_{z3}$) and poles ($\omega_{pST1} < \omega_{pST2} < \omega_{pST3} < \omega_{pST4}$) of (33) are summarized in Table 6. Interestingly, ω_{zEQ1} and ω_{pST1} virtually cancel each other, which reduces (33) to a two-zero, three-pole system. Moreover, ω_{pST4} and ω_{z3} can be regarded as high frequency time constants, further simplifying the CL-LDO stability analysis to a two-pole ($\omega_{pST2,3}$) one-zero (ω_{zEQ2}) system where the GBW can be approximated as $A_{EA}A_{MP}\omega_{pST2}$. Feedback resistors R_1 and R_2 (Fig. 32) have been removed in the proposed CL-LDO (Fig. 34). While the decision to obviate the feedback resistors leads to $\beta = 1$ and represents the worst-case for stability in any feedback system (maximum GBW), this configuration reduces the CL-LDO quiescent current consumption which is of paramount importance in the target application.

Nonetheless, the partial tracking of ω_{zEQ2} and ω_{pST2} eases this stability concern due to the mitigation of the loop phase deterioration.

Table 6. Proposed CL-LDO loop poles and zeros.

ZEROS	POLES
$\omega_{zEQ1} \approx \dfrac{g_{CGEQ}}{C_C}$	$\omega_{pST1} \approx \omega_{zEQ1} \dfrac{g_{oEA}}{g_{oEA}+g_{CGEQ}}$
$\omega_{zEQ2} \approx \dfrac{g_Z}{C_Z}$	$\omega_{pST2} \approx \omega_{zEQ2} \dfrac{g_{oEA}+g_{CGEA}}{g_Z+g_{CGEA}}$
$\omega_{z3} \approx \dfrac{g_{mMP}}{C_{gd}}$	$\omega_{pST3} \approx \dfrac{g_{OUT}(g_Z+g_{CGEQ})}{g_{mMP}C_{gd}+(g_Z+g_{CGEQ})C_L}$
--	$\omega_{pST4} \approx \dfrac{g_{mMP}C_{gd}+(g_Z+g_{CGEQ})C_L}{C_L(C_I+C_{gd})+C_IC_{gd}}$

The required CL-LDO I_L range is determined based on the min and max theoretical power (P_{in}) that can be extracted from the TEG array; this is given by V_{thev}^2/R_{thev}. For the mid-range temperature gradient (100 mV V_{thev}), the min-max P_{in} range is ~6-500 µW. In the ideal 100% EH-PMU efficiency scenario, these P_{in} values translate to a CL-LDO I_L range of about 4-300 µA @ 1.6 V V_{LDO}. The Bode plot of the loop gain is shown in Fig. 36 for a C_L of 10 pF and I_L of 4 µA, 300 µA and 1 mA. For the target I_L values, the UGF varies from 480-870 kHz and the PM is better than 48° in the worst stability case, proving that the adopted frequency compensation resulting from the auxiliary circuit is suitable for this application. In the out-of-range I_L case of 1 mA, the UGF is reduced due to the action of ω_{pST3}, but the PM is 99° and the loop is still stable.
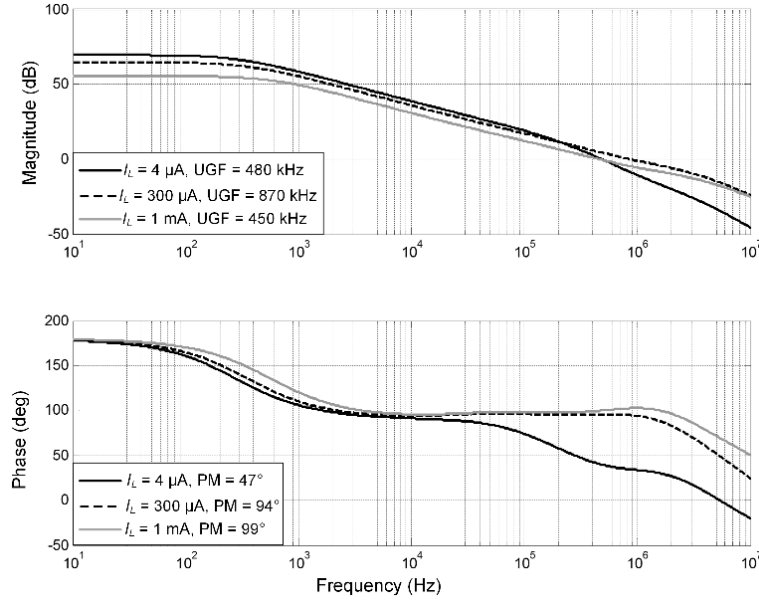
Fig. 36. CL-LDO loop gain for different I$_L$ values (postlayout simulation).

3.4.4 CL-LDO PSR

The PSR small signal model of the proposed CL-LDO is shown in Fig. 37. Unlike the small signal representation for the loop gain in Fig. 35, for PSR-purposes transistor M$_{CG}$ is directly on the input signal path to the output (V_{LDO}). As a result, M$_{CG}$ implements a common-gate stage whose output is AC-coupled (via C_C) to a load formed by the series $R_Z C_Z$ circuit and the gate of M$_P$. In the model of Fig. 37, the EA is represented as in [44, 77]. Conductances g_1, g_2 and g_{m1}, and current source I model the used Type-A EA [44] (M$_1$-M$_2$ in Fig. 34). Except for g_{mCG} (M$_{CG}$ transconductance) and g_{oCG} and g_{ocm} (output conductances of M$_{CG}$ and current mirror I$_{CG}$ in Fig. 34, respectively) all the variables are as previously defined. It can be shown that the PSR of the Fig. 37 model contains a total

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of four zeros and four poles, but more importantly, the PSR expression can be arranged as (34).
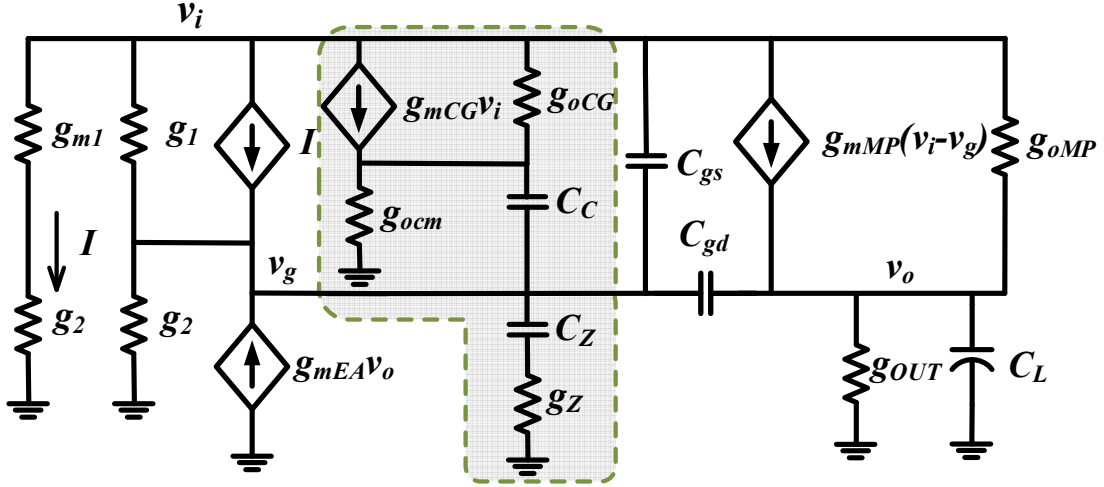
Fig. 37. Small signal model to analyze PSR in the proposed CL-LDO.

$$PSR_{NOTCH}(s) = \frac{v_o}{v_i} \approx \frac{1}{A_{EA}A_{MP}} \frac{\left(\frac{s}{\omega_{zN1}}+1\right)\left(s^2+2\zeta\omega_{No}s+\omega_{No}^2\right)\left(\frac{s}{\omega_{zN4}}+1\right)}{\left(\frac{s}{\omega_{pN1}}+1\right)\left(\frac{s}{\omega_{pN2}}+1\right)\left(\frac{s}{\omega_{pN3}}+1\right)\left(\frac{s}{\omega_{pN4}}+1\right)} \tag{34}$$

Under the same *a)-d)* assumptions of chapter 3.4.3: *a)* $C_C > C_Z > C_L$; *b)* M_P provides only low I_L levels, thus C_{gd} and C_l are both $<< C_Z$; *c)* A_{MP} is low; and *d)* Both EA and M_{CG} operate at low inversion levels, however $g_{CGEQ} < g_{oEA}$ (e.g. $I_{CG} < I_B$ in Fig. 34), the location of the poles of (34) can be approximated as shown in Table 7. Note that the four poles ω_{pN1-4} are real and exist in the LHP. However, of particular interest is the location of the zeros since, as previously discussed, the PSR degradation onset occurs at the location of the most dominant zero in the PSR (ω_{zN1}), but also any notch-filter-like behavior will stem from the characteristics of the zeros. While the location of ω_{zN1} can be

controlled with C_C, it is fair to assume this is the dominant zero due to the presence of A_{MP} and A_{CG} (M$_{CG}$ gain) in the ω_{zN1} expression. Also in Table 7, ω_{zN4} can be safely regarded as a high-frequency zero since it is dependent on small parasitic capacitance C_{gs} (due to small M$_P$). More relevant for the operation of the overall EH-PMU is the interaction of $\omega_{zN2\text{-}3}$. Although these two zeros do not directly appear in (34), their effect is captured in the form of a second order equation in the numerator of (34). It can be shown that if the damping factor of the second order equation (ζ, in Table 7) is smaller than 1, ω_{zN2} and ω_{zN3} generate a complex pair with non-zero real component, producing a notch at the frequency ω_{No}.

Table 7. Proposed CL-LDO PSR poles and zeros.

ZEROS/NOTCH/ζ	POLES
$\omega_{zN1} \approx \dfrac{g_{oEA}}{A_{MP}A_{CG}C_C}$	$\omega_{pN1} \approx \dfrac{g_{oCG}}{C_C}$
$\omega_{No}^{2} \approx \dfrac{g_z g_{mcg}}{2C_Z C_{gd}}$	$\omega_{pN2} \approx \dfrac{g_z}{C_Z}$
$\zeta \approx \dfrac{C_z g_{mcg}}{8g_z C_{gs}}$	$\omega_{pN3} \approx \dfrac{g_{mEA}}{C_{gd}}$
$\omega_{zN4} \approx \dfrac{g_{mMP}}{C_{gs}}$	$\omega_{pN4} \approx \dfrac{g_{mMP}C_{gd}}{(C_L + C_{gd})(C_{gs} + C_{gd})}$

Assuming a fixed, small C_{gd} (a few pF due to small M$_P$), the notch can be tuned via g_z, g_{mcg} and C_z. Furthermore, R_z ($1/g_z$) is implemented using a high-R resistor with a

total value of ~300 kΩ, leaving g_{mcg} and C_z as the notch-tuning elements. To account for potential parameter variations, a programmable capacitor bank is used to realize C_z. A 4-bit external control signal is used to choose between 16 different C_z values (for a maximum of ~40 pF). A second degree of programmability is added by externally setting V_{CG} to vary g_{mcg} as needed. For assumption *a)* in chapter 3.4.3 to remain valid, a second 4-bit capacitor bank for C_C is also implemented and set accordingly (for a maximum of ~80 pF). The need for the C_C bank was first highlighted in [78], where a more complex expression for ω_{No} is presented since assumption *a)* is not made. According to the ω_{No} expression, a combination of the aforementioned values requires a g_{mcg} in the order of 1 μS to produce a notch within the target f_{sw} range. Such g_{mcg} values can be obtained with less than 1 μA I_{CG} (Fig. 34), which complies with the low power requirement of the CL-LDO. For illustration, Table 8 shows the values of the time constants of Table 7. The combination of the parameters leads to a suitable ζ of 0.825 and provides the conditions for a notch at ~65 kHz. For the case of Table 8, the poles and zeros are obtained at I_L of 100 μA, calibration capacitors C_C and C_Z of 60 pF and 29 pF, respectively, and a calibrated g_{mCG} of about 1 μS.

Table 8. Proposed CL-LDO PSR poles and zeros numerical value for a notch @ 65 kHz.

ZEROS/NOTCH/ζ	POLES
$f_{zN1} \approx 390\ Hz$	$f_{pN1} \approx 10\ kHz$
$f_{No} \approx 65\ kHz$	$f_{pN2} \approx 18.2\ kHz$
$\zeta \approx 0.825$	$f_{pN3} \approx 4.2\ MHz$
$f_{zN4} \approx 30.5\ MHz$	$f_{pN4} \approx 7.1\ MHz$

Although the PSR is inversely proportional to the loop gain [44] (as such, it degrades at low frequencies with the square root of I_L), notice that the zeros in Table 7 (PSR) do not directly correspond to the poles in Table 6 (loop gain) and vice versa. This property of the proposed CL-LDO allows to have a set of complex zeros in the PSR transfer function without complex poles in the loop gain. To understand the beneficial pole-zero disparity between (33) and (34), consider Fig. 38 where a simplified PSR block diagram of the CL-LDO is shown. $A_{EA}(s)$, $A_{MP}(s)$ and $A_{CG}(s)$ represent the frequency-dependent gain of the EA, M_P and auxiliary circuit (dashed line box in Fig. 37), respectively. Paths 1, 2 and 3 represent the v_i-to-v_o noise paths affecting the PSR. Assuming large loop gain, path 1 suffers large attenuation at v_o, thus only paths 2 and 3 are considered in this conceptual analysis.

Solving for v_o/v_i in Fig. 38 yields (57), where $A_{MPDP}(s)$ is the direct path from v_i-to-v_o due to g_{mMP} and g_{oMP}. Condensing the effects of the auxiliary circuit in $A_{CG}(s)$, it can be shown that (57) has four poles and four zeros if the individual $A_{EA}(s)$, $A_{MP}(s)$, $A_{CG}(s)$

and $A_{MPDP}(s)$ have: one-pole (at v_g); one-pole (at v_o) and one-zero (due to C_{gs} and C_{gd}); two poles and two zeros; and one pole (at v_o), respectively. Furthermore, (57) approximates (34) under the assumptions made and introduces a notch in the PSR without compromising the loop stability. This is due to $A_{CG}(s)$ being purely passive for stability purposes (Fig. 35) but active for PSR purposes (Fig. 37), thus (33) and (34) experience different effects from $A_{CG}(s)$.
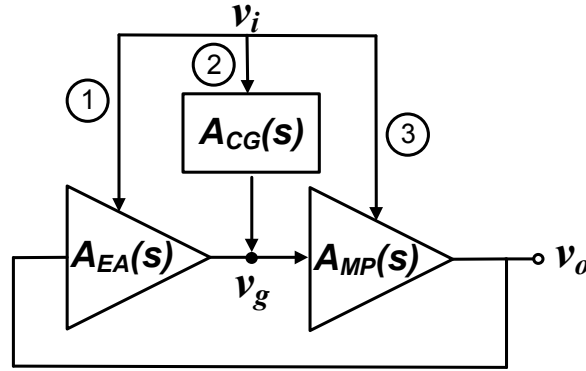
Fig. 38. Simplified PSR block diagram for the proposed CL-LDO.

$$\frac{v_o}{v_i} = PSR_{NOTCH} = \frac{A_{CG}(s)A_{MP}(s) + A_{MPDP}(s)}{1 + A_{EA}(s)A_{MP}(s)} \tag{35}$$

Table 9 summarizes the CL-LDO design parameters. While the rated I_L range is from 4 to 300 μA, as shown in Fig. 36, it is possible to supply an absolute maximum I_L of 1 mA. The V_{in}/V_{out} dropout voltage complies with the typical 200 mV limit for PMOS pass devices and the quiescent current (I_Q) is within acceptable range for low power operation due to the EA and auxiliary circuit working at low inversion levels.

Table 9. Proposed CL-LDO design parameters summary.

PARAMETER	VALUE
I_L range (µA)	4 – 300 (1000)
V_{in}/V_{out} (V/V)	1.8/1.6
I_Q (µA)	1.4
$C_{L\text{-}max}$ (pF)	10
$C_C/C_{Z\text{-}max}$ (pF)	80/40
R_Z (kΩ)	~300

3.5   Sense-and-control loop

An off-chip sense-and-control (SaC) loop was implemented using the low power, 8-bit Microchip's microcontroller PIC16F1783. After the boost converter has reached MPP and locked into a nearly constant f_{sw} (for a given load current), the PIC determines the average f_{sw} ($\overline{f_{sw}}$) and uses this value to map it on a look-up table (LUT). The LUT contains the appropriate control signals for the CL-LDO such that the notch is placed at f_{sw} for maximum voltage ripple suppression. For every $\overline{f_{sw}}$ of interest, the LUT contains two calibration entries, one for the analog V_{CG} value (generated through the PIC's 8-bit digital-to-analog converter with a resolution better than 4 mV in a 0-1 V range), and a second entry with the proper 8-bit digital word to tune the C_C and C_Z capacitor banks (4 bits per bank).

Once the tuning is completed, the CL-LDO notch is placed in the vicinity of $\overline{f_{sw}}$,

effectively rejecting the undesired boost converter switching noise. The CL-LDO notch

can be tuned as often as N_P/min(f_{sw}) seconds (N_P is the number of f_{sw}-periods used to

estimate $\overline{f_{sw}}$). In our prototype, a high PSR is obtained by accurately measuring $\overline{f_{sw}}$ (N_P

of 100), which allows for optimum notch placement. Since slow load changing conditions

are assumed, the notch tuning is performed with a 1-second interval. Note that a slow

update rate avoids unnecessary power consumption on the external PIC (70µA in this

case). While our proof-of-concept uses an off-chip SaC loop, notice that an on-chip finite-

state-machine (FSM) could implement the SaC loop. Within the FSM, a synchronous

counter could be used to measure f_{sw} and directly tune the banks of capacitors with its final

count. Similarly, this count (binary word) could be used in a basic digital-to-analog

converter to generate the analog V_{CG} value for notch calibration purposes.

3.5.1   Look-up table contents optimization

While the LUT can be filled using data obtained at the design and simulation stage,

such calibration entries might require small adjustments to compensate for potential

process variations. A straightforward way to verify the adequacy of the initial calibration

estimates to tune a notch at frequencies $f_{sw}(0)...f_{sw}(n)$ is with a one-time CL-LDO PSR

characterization using said estimates and updating the LUT as necessary. Alternatively, it

is possible to perform a foreground, automatic PSR estimation to determine if the initial

calibration estimates provide suitable notch control and noise rejection. If the PSR is not

satisfactory for a particular $f_{sw}(k)$, the calibration entry for $f_{sw}(k)$ is then adjusted accordingly and updated in the LUT.

The circuit in Fig. 39 can be used for PSR estimation. In this approach, a peak detector based on signal amplification (R_F/R_I) and partial rectification [79] is employed to estimate the supply noise at the CL-LDO input and output. Before the measurement, the initial calibration estimates for a notch at $f_{sw}(k)$ are used. After the measurement is completed, the PIC used for the SaC loop can sample the results at $V_{n\_in,\ \_out}$ and process them to obtain a PSR indicator. If the PSR indicator is satisfactory, the calibration entries for $f_{sw}(k)$ are confirmed and marked as reliable in the LUT. Otherwise, if the initial calibration estimates are off after fabrication (resulting in insufficient PSR due to imperfect notch tuning), the PIC runs a search algorithm (Fig. 40) to find a new calibration estimate that provides a notch (and higher PSR) at $f_{sw}(k)$. Once the new calibration entries are determined, the LUT is updated. This process is repeated for every f_{sw} of interest.
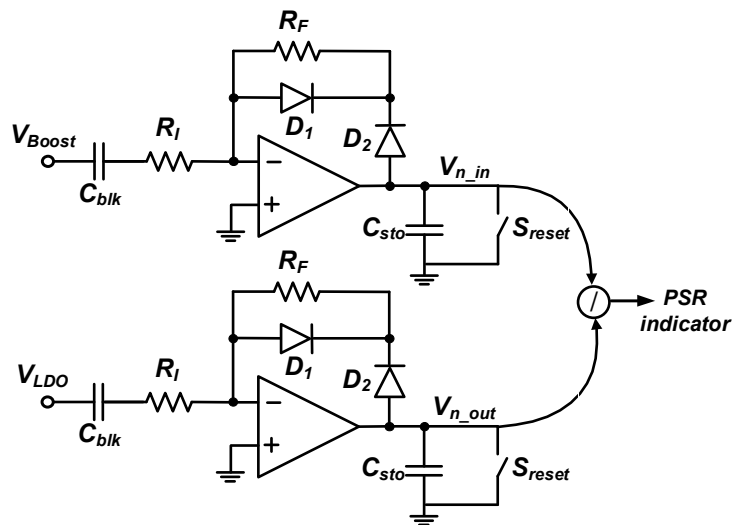
Fig. 39. PSR measurement circuit.

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Note that the suggested, on-board PSR measurement method can be seamlessly integrated, and while the amplifiers required might consume additional power, the power overhead is experienced only during a short period of time required for the LUT optimization, after which both amplifiers can be shut-down. Furthermore, additional, more complex techniques to measure PSR on-chip can be used [80].
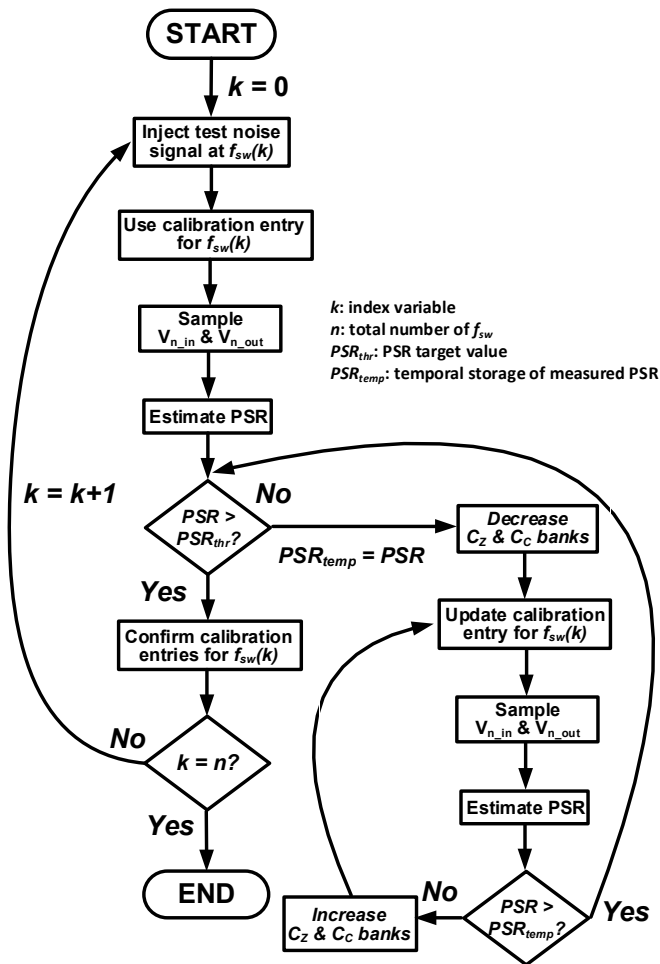
Fig. 40. LUT optimization algorithm.

3.6   Measurements

The EH-PMU was designed and fabricated in 0.5 μm CMOS process. Fig. 41 presents the testbench setup and die microphotograph, with an active area of 0.93 mm^2. Resistance matching between the EH-PMU front-end (boost converter) was performed by varying the series impedance of a 3x3 TEG array composed of MPG-DG655 modules. While the details of the array reconfiguration are out of the scope of this work, a total of 42 switches [4] enable any possible parallel/series combination of the units in the array. These interconnecting switches can be controlled by the same PIC implementing the SaC loop. By monitoring the output of an off-the-shelf temperature sensor, the PIC can decide the state of the interconnecting switches and reconfigure the array.
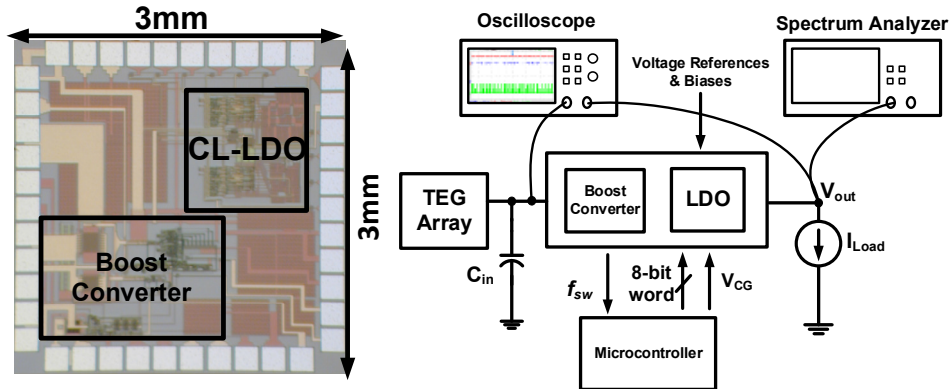
Fig. 41. Die microphotograph and testbench setup.

Resistance variation step was performed from 19 Ω to 1.53 kΩ in order to make sure stability is correctly achieved under drastic loop parameter variations. Fig. 42 shows

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that the correct MPP is achieved of 100 mV for both TEG resistance equivalencies. Broader ranges of matching can be accomplished via a tradeoff between f_{sw} and L_{in} value.
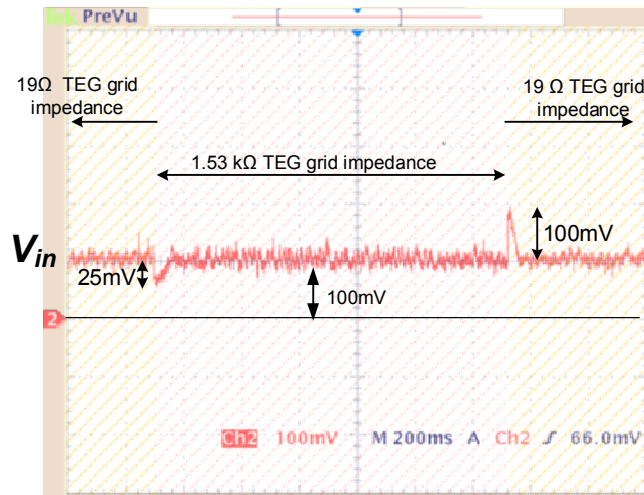
Fig. 42. Correct MPPT is achieved through PFM control loop.

The boost converter and CL-LDO outputs are shown in Fig. 43 (upper and lower signals, respectively) for a load current of 10 µA. Before the notch is introduced (Fig. 43A) the CL-LDO output shows an attenuation of the switching noise of ~6 dB. However, when the CL-LDO tuning is completed and the notch in the PSR has been properly placed (Fig. 43B), the attenuation reaches 40 dB.
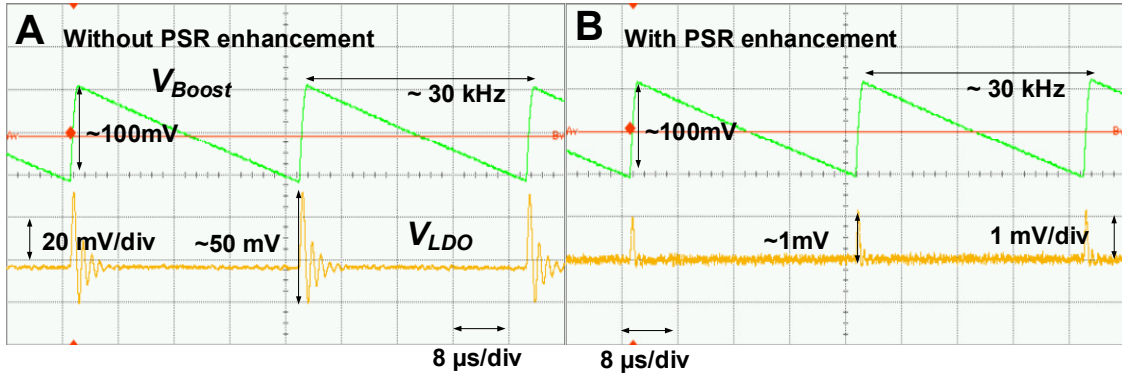
Fig. 43. Switching noise suppression from CL-LDO.

The measured CL-LDO PSR is shown in Fig. 44 for three combinations of C_C bank, C_Z bank and g_{mcg}. The total range over which the notch can be programmed is roughly between 15 kHz to 65 kHz. While the boost converter might switch at $f_{sw} < 15$ kHz, the intrinsic, low-frequency PSR of the CL-LDO can successfully attenuate the ripple at these f_{sw} values. Although the optimum ripple rejection is achieved when the notch is centered at f_{sw}, in the event of slight f_{sw} variations ($f_{sw}^* = f_{sw} + \Delta f_{sw}$) after the notch has been tuned, the switching noise at f_{sw}^* will still experience attenuation due to the steep skirt around the center notch frequency (e.g. a notch centered at 27 kHz has 36 dB suppression at 32 kHz, this is Δf_{sw} of 18.5%).
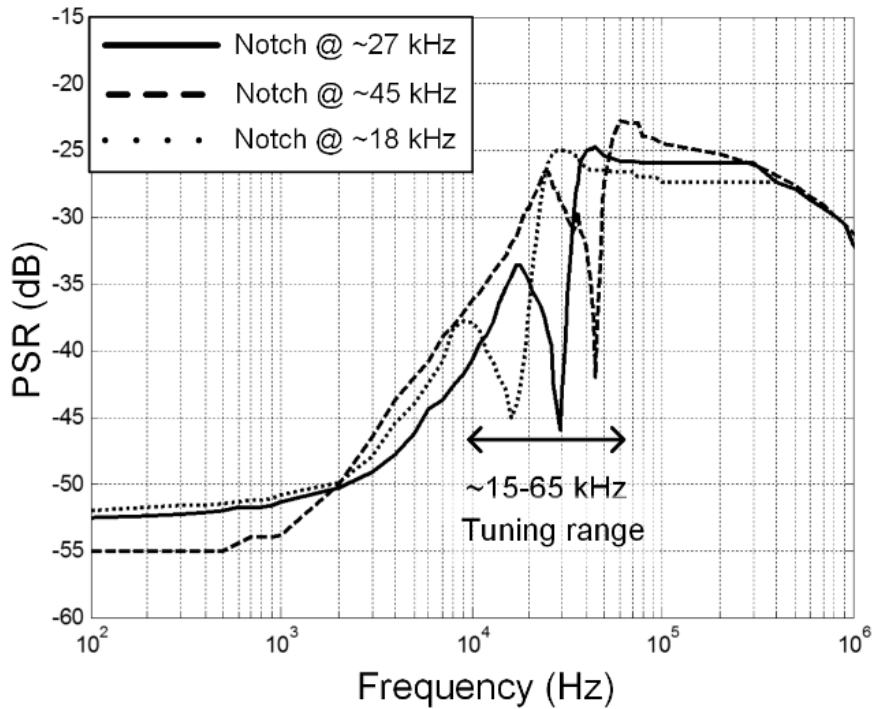
Fig. 44. CL-LDO measured PSR with notch tuning range of 15-65 kHz.

From the CL-LDO load transient response to a 4-300 μA I_L step (Fig. 45), the measured load regulation is 17 mV/mA. Interestingly, even though the modest bandwidth of the CL-LDO results in a settling time of 5 μs, this recovery interval represents less than 3% of the total Rx-to-Tx or Tx-to-Rx turnaround time in IEEE 802.15.4 standard-compliant devices [81]. Thus, an ultra-low power radio powered by the proposed EH-PMU could afford a frequency synthesizer with a settling time of nearly 187 μs and still meet the IEEE 802.15.4 standard (which specifies a turnaround time of 12 symbol periods or 192 μs @ 62.5 ksymbol/s).
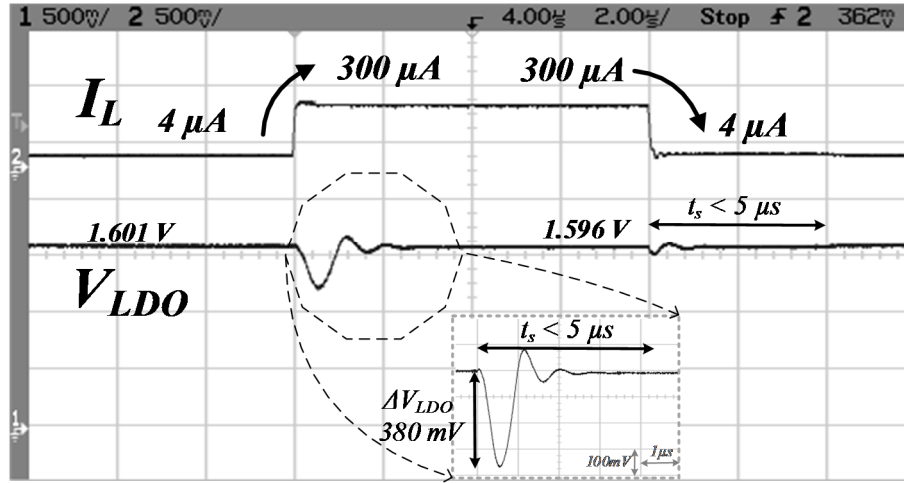
Fig. 45. CL-LDO load transient response to a 4 µA to 300 µA I_L step.

Influenced by the small on-chip C_L and low bias current available to drive the gate capacitance of M_P, the Fig. 45 measurement also shows that the voltage undershoot (ΔV_{LDO}) departs up to 380 mV from the nominal V_{LDO}. Despite its short duration, there might be load circuitry for which this V_{LDO} undershoot could cause undesired operation. When necessary, it is possible to combine the proposed CL-LDO with voltage spike-triggered dynamic biasing techniques [82] to reduce the magnitude of the voltage dip, at the expense of increased current consumption.

As shown in Fig. 46, the overall maximum system end-to-end efficiency was measured at 57.57% (V_{Boost} of 1.8 V and V_{LDO} of 1.6 V) for input (V_{thev}) voltages of 140 and 190 mV. The total EH-PMU power consumption is 3.6 µW (1 µW in the boost converter and 2.6 µW in the CL-LDO). Table 10 presents the overall system performance for the proposed EH-PMU compared to state-of-the-art systems. The total power consumption does not take into account the power consumed by the microcontroller SaC implementation.
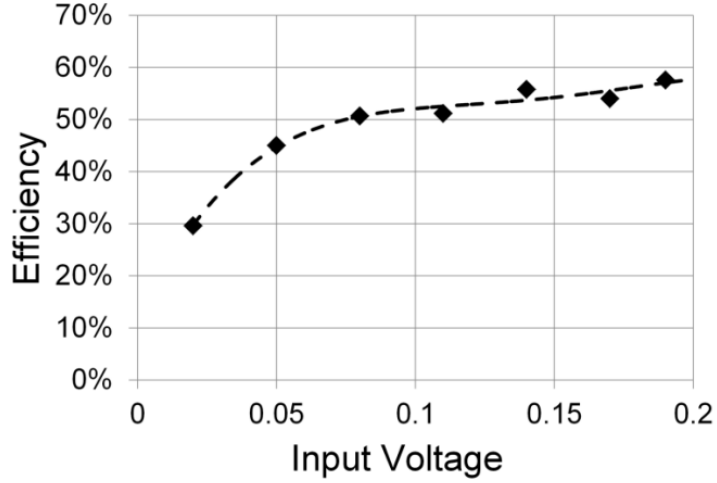
Fig. 46. End-to-end system efficiency.

Table 10. Performance summary and comparison for the proposed PMU.

	[53]	[55]	[56]	[57]	This work
Input voltage	0.38-3.3 V	20-160 mV	30 mV	1 V	50-250 mV
Output voltage	Multiple	1.88 V	Multiple	1.8 V	1.6 V
Quiescent	1.2 μW	-	-	-	3.6 μW
MPPT	✓	✓	✗	✗	✓
Max. Efficiency	92%	58%	38%	88%	57.57%
PSR	-	-	-	-	**-40 dB @f_{sw}**
Topology	Buck +Boost	Buck +Boost	Rectifier +Boost+LDO	Buck +Boost	Boost +LDO
Process	0.13 μm	0.35 μm	0.13 μm	0.35 μm	0.5 μm

3.7   Conclusion

An energy harvesting power management unit (EH-PMU) based on a combination of a boost converter and a capacitor-less LDO (CL-LDO) with high efficiency and enhanced noise suppression has been presented. The boost converter delivers MPPT from

an array of TEG devices through a frequency modulation scheme. The matching scheme is capable of correctly match from 19 Ω to 1.53 kΩs. The CL-LDO includes an auxiliary circuit for enhanced PSR. A notch at the switching frequency of the boost converter is added in the CL-LDO PSR transfer function. The EH-PMU employs a Sense-and-Control loop to send the switching frequency information from the boost converter to the CL-LDO to correctly shift the notch to the switching frequency. End-to-end system efficiency of 57.57% is achieved by the EH-PMU, and 40 dB noise suppression at the switching frequency is measured. The proposed power consumption/power delivering capabilities of the EH-PMU are suitable for energy harvesting assisted devices in the 100s of μW range.

CHAPTER IV

AN ULTRA-LOW POWER PLL-LESS WIRELESS TRANSMITTER FOR IOT

APPLICATIONS

This chapter presents an ultra-low power, PLL-less, energy efficient transmitter for Internet-of-Things (IoT) applications. To reduce the typical bottlenecks in low power transmitter (Tx) architectures, this work introduces an ultra-low power cell referred to as vertical delay cell. A ring-oscillator based on this delay cell is used together with an edge-combiner-type power amplifier, which acts as a frequency multiplier and allows the oscillator to operate at only ⅓ of the RF frequency. A digital calibration scheme is used for frequency correction. Due to the wideband binary frequency shift keying (BFSK) modulation used in the Tx, the close-in phase noise requirements of the local oscillator can be relaxed and the interest is centered in its far-out phase noise. Thus, it is possible for the ring oscillator to operate in an open loop fashion, avoiding the continuous operation of costly frequency dividers. The Tx was fabricated in 0.18 μm CMOS technology and occupies an active area of 0.112 mm^2. Due to the wide tuning range of the oscillator, the RF carrier tunability is 0.15 GHz–1.05 GHz. The maximum output power is −10 dBm, and the normalized energy efficiency is 3.1 nJ/(bit-mW) while transmitting with a 3 Mbps data rate. Under these conditions, the total measured power consumption from a 1.65 V (oscillator), and 1.8 V (power amplifier and digital circuitry) voltage sources is 935 μW and 620 μW for output powers of −10 dBm and −15 dBm, respectively.

4.1   Introduction

A fully deployed Internet-of-Things (IoT) platform envisions a ubiquitous global network where not only inanimate objects but also people and animals are able to establish on-demand, robust communications links between each other. The perpetual connectivity state maintained by every IoT node opens up limitless possibilities and applications in multiple consumer segments as diverse as: health care, structural health monitoring, home appliances, home and industrial automation, and traffic management to mention a few [83]. Ultra-low power operation sits on the top of the list of the technical challenges that an IoT-competent device must overcome [84]. Minimum power consumption in active mode is critical to enable long time intervals between replacements of the local energy reservoir in an IoT, particularly in those nodes located in isolated or with limited access spaces (e.g., implantable devices). Furthermore, since the typical energy source of an IoT node is either a small form factor battery or an energy harvesting unit [85] with limited resources, it becomes imperative for the IoT to operate with extremely low power levels and in an energy-efficient fashion. While an IoT node is a complex device that might include a power management unit, memory, microcontroller, different sensors and their corresponding analog front-end, and a wireless radio, it is typically the latter element which consumes the highest power [85, 86]. The need to reduce the power consumption of the wireless gateway in the IoT nodes has motivated the recent development of highly efficient radio transmitters [50, 87-94].

Some of the clever approaches undertaken to reduce the Tx power consumption are illustrated in Fig. 47 and include: the use of subharmonic injection-locked (IL) oscillators to apply phase multiplexing techniques at a fraction of the RF signal [87] (Fig. 47a), the implementation of an edge-combiner power amplifier (PA) that allows direct modulation and operation based on cascaded IL ring oscillators directly locked to an off-chip crystal oscillator [50] (Fig. 47b), the use of an intermediate frequency (IF) quadrature backscatter technique which avoids the use of RF active circuitry in the Tx while supporting spectrally efficient modulation schemes while operating at low power consumption levels due to its simple architecture and low operating frequency [88] (Fig. 47c), the co-design and optimization of the voltage-controlled oscillator (VCO) and its corresponding frequency divider that yields a low power frequency synthesizer and enables an efficient polar Tx architecture [89] (Fig. 47d), the use of a 2-tone RF signal as a transmission vehicle for information embedded in the spacing between these tones (Δf) by means of a digitally-assisted Tx based on a digitally-controlled oscillator (DCO) and a Gilbert-cell-like PA [90] (Fig. 47e), the use of a power-VCO in a heavily duty-cycled direct-RF Tx architecture ($\mu\%$ duty cycle) [91] (Fig. 47f), the use of a delta-sigma digitally-controlled polar PA in a direct digital-to-RF-envelope Tx [92] (similar to Fig. 47d), sophisticated three-point modulation loops in polar PA-based Tx [93] (one extra modulation point than Fig. 47d), and a subharmonic ILRO with a digital PA supporting high modulation rates [94] (similar to Fig. 47a).
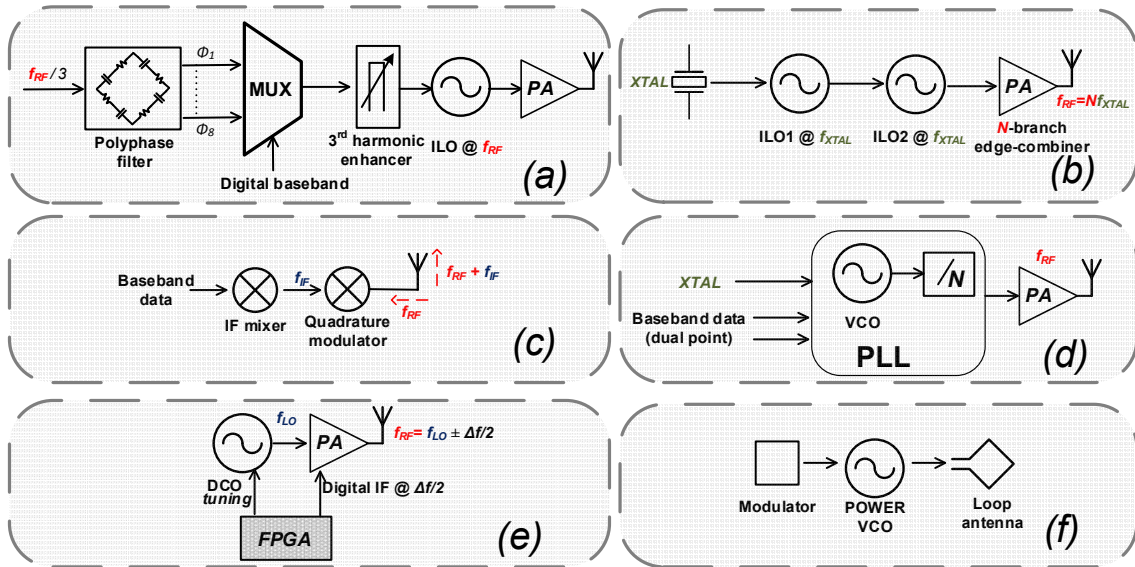
Fig. 47. Some state-of-the-art approaches for low power Tx, a) Subharmonic IL oscillator, b) Edge-combiner PA, c) IF backscattering technique, d) Multi-point modulation in a polar Tx, e) Two-tone RF signal transmission, f) Power VCO.

From the previous state-of-the-art review, it is possible to identify two clear trends in the energy efficient wireless Tx design, *i)* architectures that strive to reduce the absolute power consumption and deliberately use modulation schemes with low spectral efficiency low like on-off keying (OOK) or (frequency-shift keying) FSK to reduce complexity (and ultimately power) [50, 90, 91], and *ii)* Tx chains sporting more complex modulations that maximize spectral efficiency and allow higher data rates while consuming power levels well above 1 mW or radiating low output powers (P_{out}) [87-89, 92-94]. Both approaches have their pros and cons: *i)* is useful in applications that require the sporadic transmission of small data packets and suit themselves for energy harvesting-powered systems. Conversely, the Txs in the category *ii)* can be used to transmit a higher volume of information while making efficient use of the available power in the attached energy reservoir but pose tougher requirements on their power management units. This chapter

discusses the implementation of a Tx architecture for operation in the 902-928 MHz Industrial, Scientific, and Medical (ISM) frequency band that sits somewhere in-between categories *i)* and *ii)*. A conceptual diagram of the proposed Tx is shown in Fig. 48. The Tx architecture uses both system–level and circuit–level techniques to reduce the power consumption; yet, it is also capable of operating up to a data rate of 3 Mbps. Thus, this work achieves an energy efficiency better or comparable to other Tx implementations operating at sub-200 kbps data rates [50, 90, 91] while transmitting a maximum P_{out} of -10 dBm for a 15 times faster throughput.
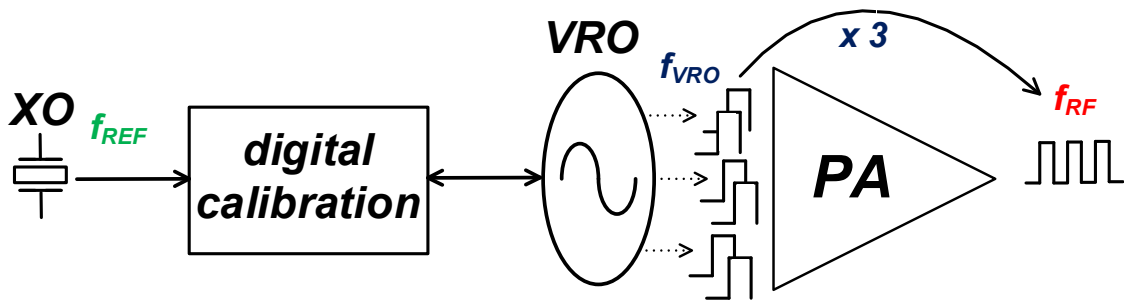
Fig. 48. Conceptual diagram of the proposed Tx.

The Tx presented in this work introduces an unbalanced —yet differential— ultra-low power delay cell coined as vertical delay cell. A vertical three-stage ring-oscillator (denoted as *VRO* from now on) based on vertical delay cells with a digital RC delay tuning scheme form the core of the Tx. An edge-combiner switching PA takes advantage of the multiple phases available at the *VRO* output and enables a 3x frequency multiplication of the *VRO* frequency (f_{VRO}), allowing the oscillator to nominally operate at ⅓ of the RF frequency (f_{RF}), which further reduces the overall power consumption. An on-chip Pierce

stabilization circuit for a 32.768 kHz crystal oscillator is used as the reference signal (f_{REF}) in the digital calibration algorithm employed for f_{VRO} correction. The open-loop, digitally-assisted architecture employed for the local oscillator (LO) generation interfaces with an external field programmable gate array (FPGA), which calculates the required coarse and fine digital words for the RC-delay tuning. Three 7-bit resistive-string-based digital-to-analog converters (DAC) generate the actual control voltages for the RC tuning based on the calibration words generated by the FGPA.

The rest of the chapter is organized as follows: Section 4.2 describes the Tx architecture at the conceptual level and presents the system-level considerations. Section 4.3 introduces the vertical delay cell and illustrates its use in a vertical ring oscillator (VRO). Section 4.4 discusses the edge-combiner power amplifier, and elaborates on the implemented digitally-assisted frequency correction scheme. Section 4.5 discusses the experimental results and finally, Section 4.6 provides this work's conclusions.

4.2   Proposed Tx architecture

The proposed Tx architecture is shown in Fig. 49. The Tx is optimized for operation in the 902-928 MHz band. The joint design and optimization of the VRO employed as LO generation stage and the edge-combiner PA greatly reduces the power

dissipation of what typically are the two most power-hungry blocks in the Tx chain[2]. The delay cell used in the *VRO* is labeled "vertical" due to its stacked arrangement. By construction, the structure of the vertical delay cells enforce the reuse of current (charge) drawn from the supply during its operation, leading to an intrinsically lower power consumption than other horizontal delay cells. Furthermore, by using a three-stage *VRO* in combination with a three-leg switching edge-combiner PA similar to [50], the *VRO* needs to run at only $\frac{1}{3}f_{RF}$. The implications of this approach along with the system-level choices supporting it, and key building blocks are discussed below.
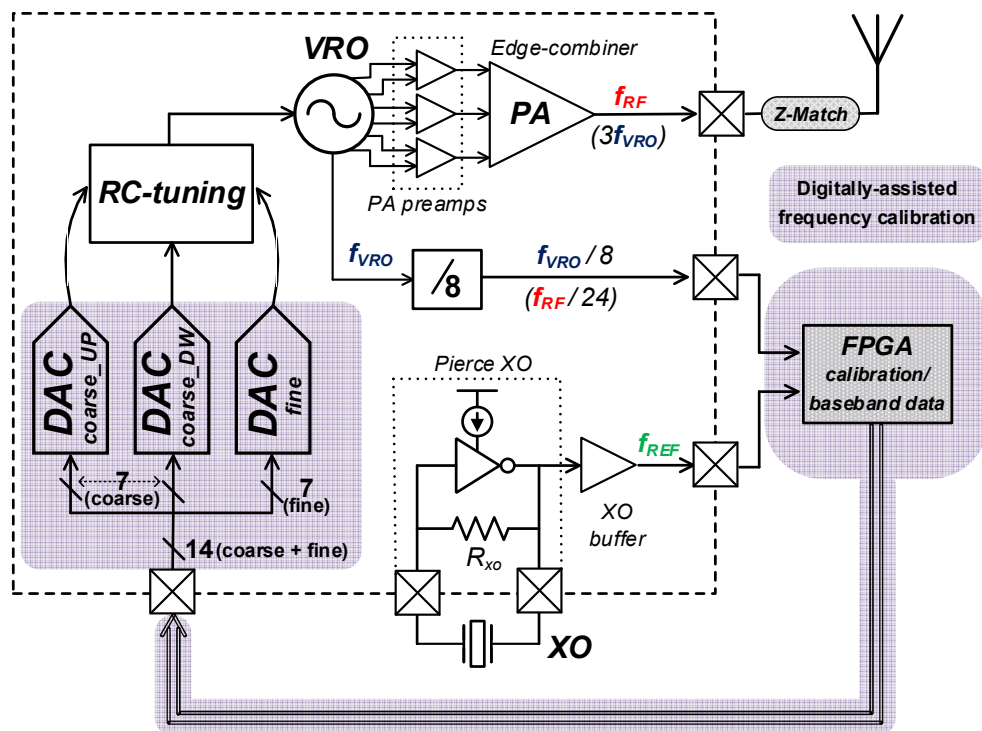
Fig. 49. Top-level Tx block diagram.

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[2] Using an edge-combiner PA reduces the oscillator power consumption (P_{cons}) and required oscillation frequency (*f*) by N, where N is the number of branches in the edge-combiner PA. This holds under the assumption of a proportional relation between P_{cons} and *f* (for the same supply voltage).

4.2.1   A PLL-less local oscillator (LO) generation stage

Replacing the typical phase-locked-loop-based frequency synthesizer (PLL-FS) with an open-loop LO is a challenging task but is crucial to enabling the Tx low-power operation. Furthermore, PLL-FSs are not only power-hungry, but they require large area to implement an adequate loop filter, and also exhibit long settling times which might hamper the performance in heavily duty-cycled applications [50]. Conversely, the open-loop LO proposed in this work exhibits short wake-up and turn-around times, allowing for fast modulation rates if directly applied at the *VRO*. On the other hand, using an open-loop, free-running LO instead of a PLL-FS LO also implies higher close-in phase noise levels (due to the lack of noise-suppressing loop gain [95]). Furthermore, the LO phase noise directly appears as noise in the transmitted signal [96]. Thus, high LO phase noise levels in the Tx could lead to spectral corruption between the two tones (f_1 and f_2) used to represent the mark and space states in the binary version of FSK used in the proposed Tx architecture. In the worst case scenario, f_1 and f_2 might be undistinguishable on the receiver side. To alleviate this concern, we have used a wideband FSK modulation. In this scheme, the frequency deviation (Δf) between f_1 and f_2 and the center frequency (f_c) is increased. Since the modulation index (h) is proportional to Δf ($h = \Delta f/DR$, where DR is the data rate), h also increases, which concentrates the transmitted signal power around $f_c \pm \Delta f$ instead of around f_c [97]. If Δf is equal to the frequency offset from f_{VRO} for which the phase noise of the *VRO* has already rolled-off (e.g., a few MHz), it is the far-out phase noise of the *VRO* that becomes important for the adequate transmission and reception of

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f_1 and f_2. Unlike the close-in phase noise, the far-out phase noise of a well-designed free-running LO is not so different from that of a narrow bandwidth PLL-FS LO (since it is typically dominated by the oscillator [98]). Using a sufficiently large Δf allows us to use a digitally-calibrated free-running LO in our ultra-low power, energy efficient Tx. The modulated signals under two different Δfs are illustrated in Fig. 50.
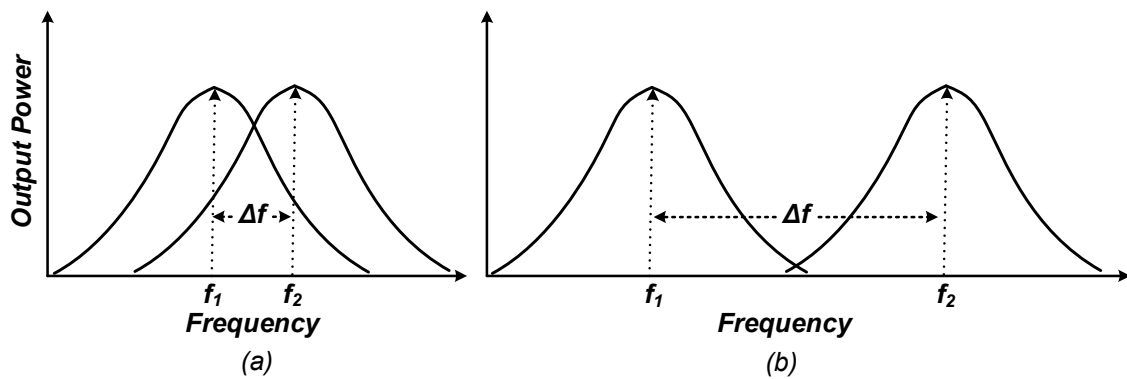
Fig. 50. BFSK modulation with a) small Δf (LO phase noise buries f_1 and f_2); b) large Δf (negligible LO phase noise effect).

Equally important in the Tx architecture is the digitally-assisted frequency correction scheme, which guarantees that the *VRO* oscillates with the required frequency after the calibration is completed. Shown in Fig. 51 is an example of the *VRO* output signal before and after calibration. Previous to calibration, the frequency is slightly off-target (by an error δ) due to process and/or temperature variations. Conversely, after the frequency correction scheme is applied, the *VRO* frequency is on-point for the transmission of a mark state (f_1).

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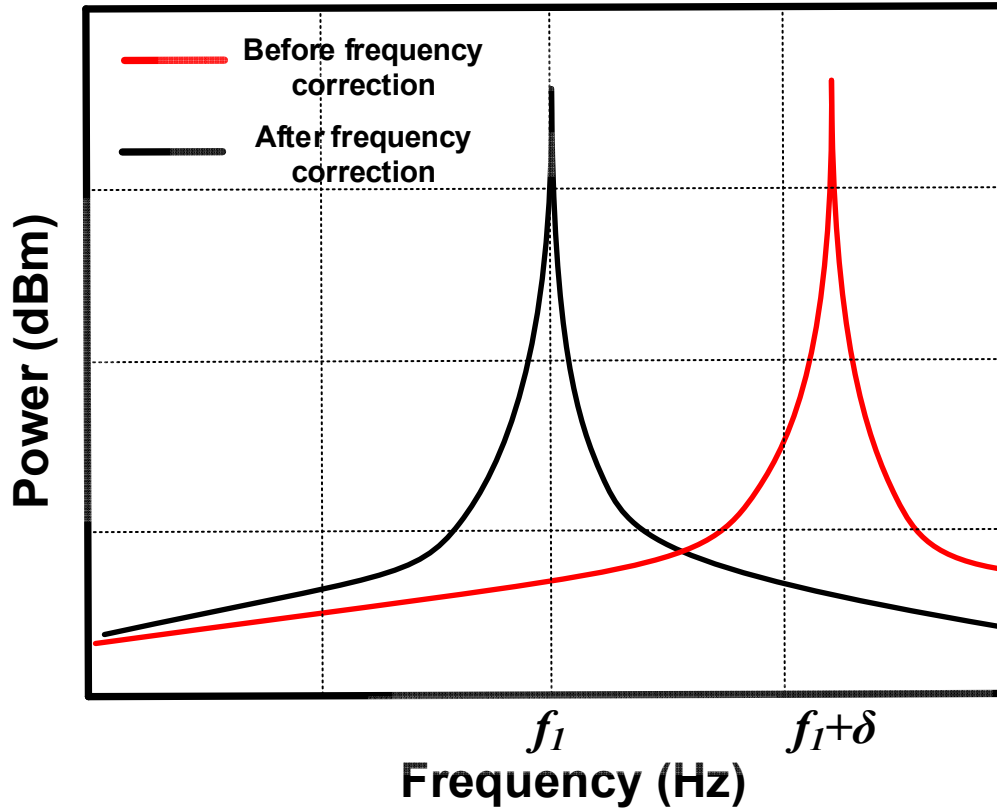
Fig. 51. Conceptual description of the frequency correction scheme effect in the *VRO* output frequency for the correct transmission of a mark state (f_1).

4.3   VRO analysis and design

The proposed *VRO* is based on vertical delay cells. As shown in Fig. 52, the vertical delay cell can be thought of as an unwrapped version of the differential cascode voltage-switch-logic (DCVSL) delay cell. Previous works have used some form of the DCVSL delay cell to implement ring-oscillators [99-101] and frequency dividers [101]. Due to its small input capacitance, reduced switching noise, low power, and speed, the DCVSL style is a natural candidate for high frequency operation circuits. However, the DCVSL cell, like most implementations of differential structures, has two mirrored paths

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that process the positive and negative inputs and generate the differential output (V_{diff}). Thus, for an output voltage swing of $\frac{1}{2}V_{diff}$, a single path implementation consumes roughly half the power of that used by its differential counterpart. Nonetheless, as enticing as halving the power is, the multiple benefits of differential signaling generally overcome this power trade-off. To provide an alternative to this conundrum, we propose a delay cell based on the DCVSL structure that uses a single path to ground but is also able to generate differential output signals. As a result, power consumption is decreased while the characteristics of differential signaling are preserved.
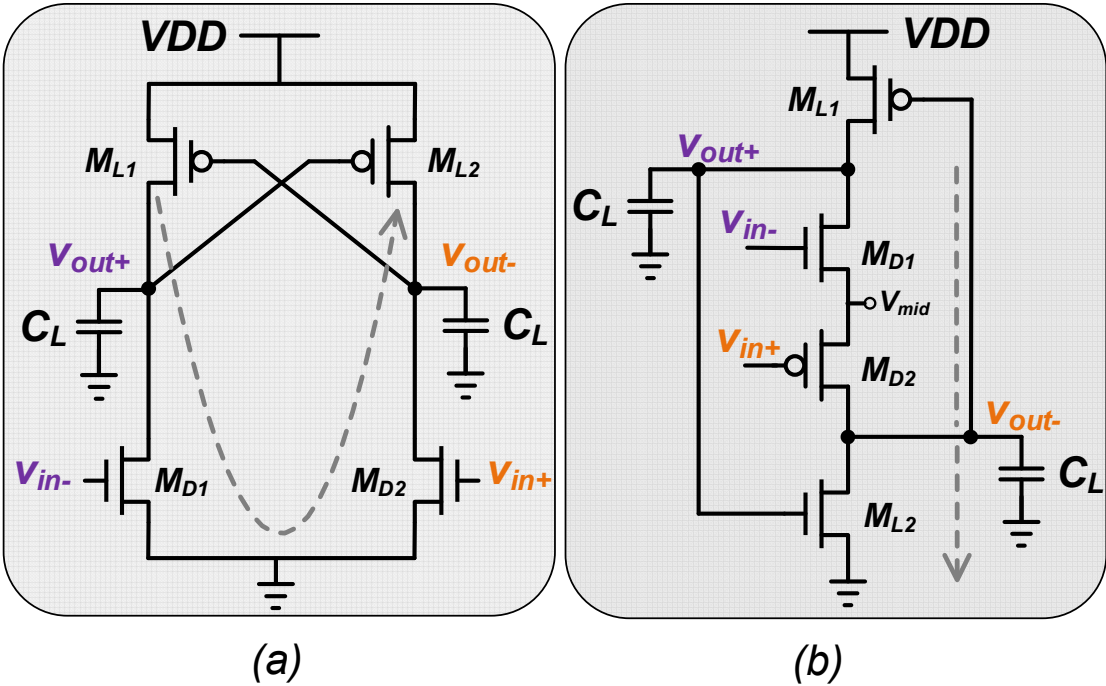
Fig. 52. a) Typical DCVSL delay cell, and b) Proposed vertical delay cell.

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Intuitively, in the DCVSL cell of Fig. 52, a packet of charge $Q_1 = C_L V_{DD}$ Coulombs is drawn from VDD every time either driver transistor (M_{D1} and M_{D2}) is turned off to represent a logic high state at the corresponding output. Later on, when the input switches and the driver transistor is turned on, Q_1 is simply discarded to ground to represent a logic low state at the output. This mechanism is continuously executed in the two branches forming the DCVSL cell. However, in the presence of differential inputs, only one of the two outputs is a logic high at a given instant (while the other is a logic low). Thus, it is conceptually possible to reuse Q_1 (instead of discarding it), to represent the logic high state of the complementary output when the branch that initially drew it needs to switch to a logic low state. Also shown in Fig. 52 is the proposed vertical cell, which can actually operate in such fashion. By fully unwrapping the DCVSL cell, and making the necessary changes to the structure, the same packet of charge Q_1 can be used to represent two consecutive high states (one at each output). In the vertical delay cell, transistors M_{D2} and M_{L2} are of the complementary type with respect to the DCVSL cell (Fig. 52). Under the assumption of differential input signals v_{in-} and v_{in+}, the lower part of the vertical delay cell (M_{D2} and M_{L2} in Fig. 52b) is able to accept Q_1 at the precise instant that the upper part (M_{D1} and M_{L1} in Fig. 52b) needs to discard it to switch states. Since there is only one charge packet circulating at a time, the vertical delay cell enforces differential operation while exploiting verticality and reducing the power consumption.

To further understand the operation of the vertical delay cell, Fig. 53 illustrates the two possible states that the cell can temporarily settle into. While both outputs experience a similar voltage swing, due to the vertical nature of the structure, signals v_{out+} and v_{out-}

operate at different common-mode voltage levels. The middle point of the vertical cell, V_{mid}, is set at ½V_{DD}. As a result, v_{out+} (upper output) can reach voltages between ½V_{DD} and V_{DD}, whereas v_{out-} (lower output) might sway between GND and ½V_{DD}, yielding common-mode levels (trip points) of ¾V_{DD} and ¼V_{DD} for v_{out+} and v_{out-}, respectively. For low power operation, ¼V_{DD} is typically below the transistor threshold voltage (V_{TH}), and the vertical delay cell preserves the zero-quiescent current feature (disregarding leakage) of its DCVSL predecessor.
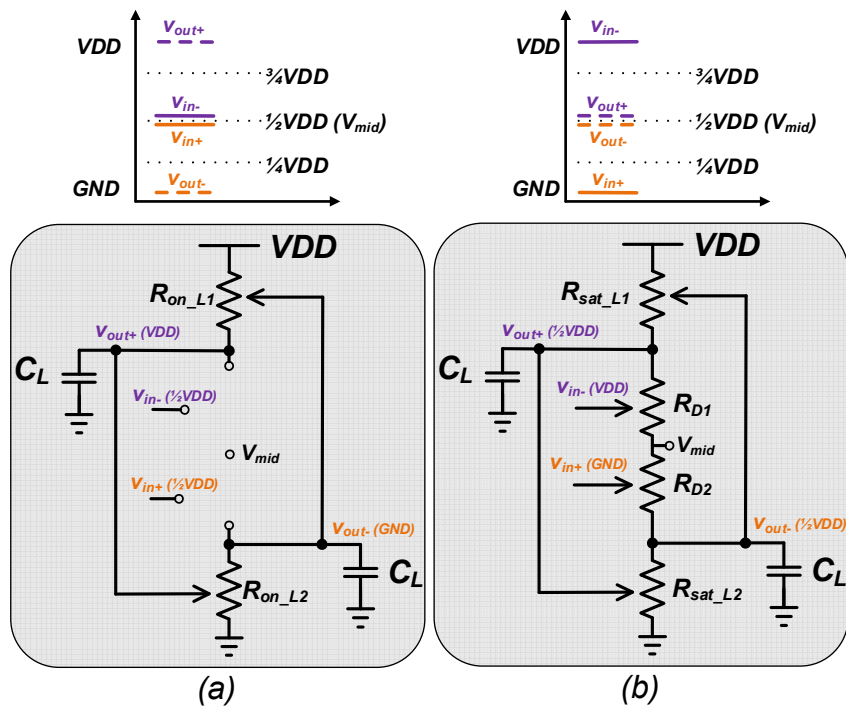
Fig. 53. Equivalent models for the vertical delay cell during its two possible states showing the corresponding common-mode levels: a) Logic high (low) at v_{out+} (v_{out-}), and b) Its complementary logic high (low) state at v_{out-} (v_{out+}).

For a graphical comparison of the output levels, Fig. 54 shows a sketch of the input and output signal waveforms of both DCVSL (Fig. 54a) and the proposed vertical delay cell (Fig. 54b) under the assumption of input signals with linear ramps during the transitions. As anticipated, the vertical delay cell waveforms experience half the voltage excursion (swing) than that of the DCVSL. However, the characteristic delay asymmetry (different low-to-high and high-to-low transition times) of the DCVSL logic style [101] is present in both delay cell and is further discusses later in this chapter.
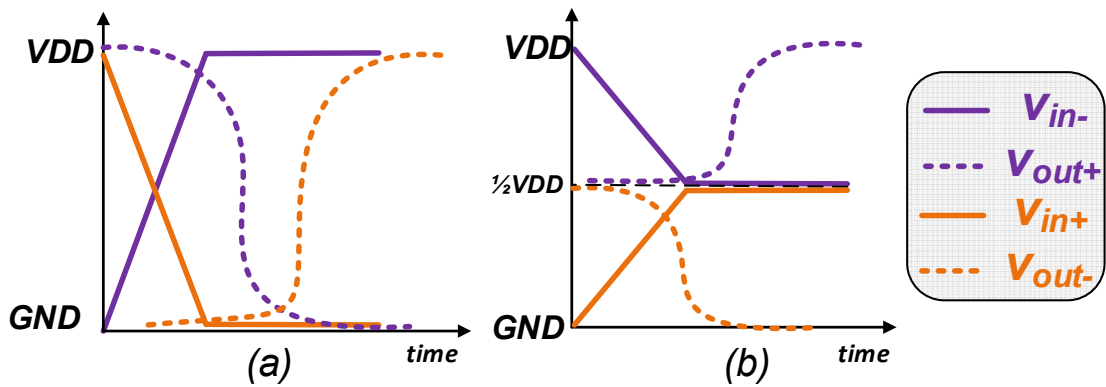
Fig. 54. Output levels comparison of a) DCVSL cell, and b) Proposed vertical delay cell.

Shown in Fig. 53a is the first state of the delay cell, where both inputs, v_{in-} and v_{in+}, are at a $\frac{1}{2}V_{DD}$ level, which corresponds to a logic low for the upper section and a logic high for the lower section. Under these conditions, the driver devices M_{D1-2} experience a close-to-zero voltage between their gate and source terminals. This is represented by open paths between V_{mid} and v_{out+} and v_{out-} in Fig. 53a. Due to the lack of a ground path, the C_L capacitors are charged to V_{DD} and GND (v_{out+} and v_{out-}, respectively) through the on-resistance of the latch devices M_{L1-2}, which operate in the triode region during this state.

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The second state in which the vertical delay cell might operate is shown in Fig. 53b. In this case, inputs v_{in-} and v_{in+} are at the opposite voltage rails, V_{DD} and GND, respectively. Depending on the V_{DD} level and the threshold voltage of M_{D1-2}, these driver devices may operate in either triode or subthreshold region; thus, for fast switching, it is important to guarantee a V_{DD} voltage high enough to put transistors M_{D1-2} in triode region ($\frac{1}{2}V_{DD} >$ max(V_{TH})) while operating on the second state. Conversely, transistors M_{L1-2} operate in saturation during this state to allow both output signals to reach $\frac{1}{2}V_{DD}$. While in this state there is a path to ground, the total resistance is large (due to the saturated latch devices), allowing for low power consumption.

The delay of the cell in Fig. 53b can be estimated using the alpha-power (α-power) MOSFET model originally proposed in [102] and further expanded in [101] for application in DCVSL cells. Despite its vertical nature, the proposed cell inherits the well-known delay asymmetry from its DCVSL counterpart [101], as will be shown. To obtain the expressions for the high-to-low and low-to-high propagation delays (τ_{PHL} and τ_{PLH}, respectively) we follow the steps in [101, 102].

The current-voltage equations of the α-power model [102] are given by (36), (37), and (38).

$$I_D = \begin{cases} 0 & V_{GS} \leq V_{TH} \\ \dfrac{I'_{DO}}{V'_{DO}} V_{DS} & V_{DS} < V'_{DO} \\ I'_{DO} & V_{DS} \geq V'_{DO} \end{cases} \tag{36}$$

$$I'_{DO} = I_{DO} \left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}} \right)^{\propto} \tag{37}$$

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$$V'_{DO} = V_{DO} \left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}} \right)^{\alpha/2} \tag{38}$$

In the α-power model the transistor drain current (I_D) is specified for three operation regions (cutoff, triode, and saturation, from top to bottom in (36)), V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, V_{TH} is the transistor's threshold voltage, V_{DD} is the supply voltage, V_{DO} is the drain saturation voltage at the $V_{GS} = V_{DD}$ condition, I_{DO} is the drain current at the $V_{GS} = V_{DS} = V_{DD}$ condition, and α is the velocity saturation index, which is a unitless parameter for a transistor with a given length determined from simulations [102].

In the case of the *VRO*, each vertical delay cell drives and is driven by identical vertical delay cells. Thus, the input and output slew rates are assumed to be similar as was done in [102]. However, to simplify the delay analysis, a linear ramp with rising (falling) input transition time T_{tn} (T_{tp}) is used [101]. To obtain an expression for T_{tn}, the time it takes for the input ramp to charge the load capacitance C_L from $0.1V_{DD}$ to $0.9V_{DD}$ is calculated and expressions similar to [102] are obtained in (39) and (40). Note that due to the half-V_{DD} swing of the vertical delay cell outputs, when numerically evaluating (39) and (40), the variable V_{DD} in should be properly adjusted to ½V_{DD}. Similarly, the variables with added subindex P or N denote a voltage (V_{DO}) or current (I_{DO}) corresponding to the PMOS or NMOS transistors of the stage driving the cell under analysis, correspondingly.

$$T_{tn} = \frac{C_L V_{DD}}{I_{DOP}} \left(\frac{0.9}{0.8} + \frac{V_{DOP}}{0.8 V_{DD}} \ln \left(\frac{10 V_{DOP}}{e V_{DD}} \right) \right) \tag{39}$$

$$T_{tp} = \frac{C_L V_{DD}}{I_{DON}} \left(\frac{0.9}{0.8} + \frac{V_{DON}}{0.8 V_{DD}} \ln \left(\frac{10 V_{DON}}{e V_{DD}} \right) \right) \tag{40}$$

Assuming also that the input signal triggering a transition at the output reaches its final value before said output reaches the point of delay measurement ($\frac{1}{2}V_{DD}$ in the general case and $\frac{1}{4}V_{DD}$ in the vertical delay cell case), τ_{PHL} and τ_{PLH} corresponding to the upper output of the vertical delay cell v_{out+} are given by (41) and (42).

$$\tau_{PHL} = K_{HL}T_{tn}\left[\left(\frac{v_{TN} + \alpha_N}{1 + \alpha_N} + C_L\frac{V_{DD}}{2I_{DON}}\right) - \frac{1}{2}\right] \tag{41}$$

$$\tau_{PLH} = 2K_{LH}T_{tp}\left[\left(\frac{v_{TP} + \alpha_P}{1 + \alpha_P} + C_L\frac{V_{DD}}{2I_{DOP}}\right) - \frac{1}{2}\right] \tag{42}$$

From (41) and (42), α_N and α_P are technology dependent parameters for N and P-type devices, respectively [102]; v_{TN} and v_{TP} are the ratios of the transistor's threshold voltage to V_{DD} (V_{THN}/V_{DD} and V_{THP}/V_{DD}, respectively); K_{HL} and K_{LH} are correction factors given by (43) and (44), respectively, and calculated using empirical parameters ($\gamma_{N,P}$ and $\zeta_{N,P}$) obtained from simulations [101]; and finally, W_N/W_P denotes the N to P width ratio of the delay cell (for the same length). Table 11 contains the values of the design and empirical parameters used in a 0.18 μm CMOS process. In Table 11, C_L represents the input capacitance of the vertical delay cell, and the channel widths ratio (W_P/W_N) corresponds to a PMOS latch device and to an NMOS driver in Fig. 52b (M_{L1} and M_{D1}, respectively).

$$1/K_{HL} = \gamma_N + \zeta_N\frac{W_N}{W_P} \tag{43}$$

$$1/K_{LH} = \gamma_P + \zeta_P\frac{W_N}{W_P} \tag{44}$$

Table 11. Design and empirical parameters values for delay calculation in 0.18 μm CMOS process.

Parameter	Value
C_L	200 fF
V_{DD}	1.35 – 1.65 V
V_{THN}/V_{THP}	0.5/0.6 V
α_N/α_P	1.1/1.4
γ_N/γ_P	0.26/0.36
ζ_N/ζ_P	0.403/0.245
W_P/W_N	0.5/21.6 μm

From the delay expressions for the upper output at v_{out+} in Fig. 52b, τ_{PHL} includes only the time it takes a rising-input (T_{tn}) at v_{in-} to turn M_{D1} on enough such that V_{mid} is propagated to v_{out+} (which represents a logic-low level). Conversely, τ_{PLH} at v_{out+} has two components [101]: t_1, which is the time it takes for a rising-input at $\boldsymbol{v_{in+}}$ to increase the resistance of M_{D2} such that $\boldsymbol{v_{out-}}$ toggles; and t_2, which is the time it takes a falling edge in $\boldsymbol{v_{out-}}$ to reduce the M_{L1} resistance such that V_{DD} propagates to v_{out+} (representing a logic-high level). Unlike the DCVLS cell case, where t_1 is due to an NMOS, and t_2 is due to a PMOS, both τ_{PLH} components (at v_{out+}) in the vertical cell are due to P-type devices. Hence, the expression for τ_{PLH} (42) in the vertical delay cell is different from its DCVSL counterpart [101]. Fig. 55 shows the waveforms and details the signal transitions for the delays quantification at the v_{out+} output of the cell in Fig. 52b. Due to the duality of the upper and lower part of the delay cell, the delays (τ_{PHL} and τ_{PLH}) for the lower output (v_{out-}) exhibit an opposite behavior than that of the ones in the upper section of the cell, meaning

that for v_{out-}, τ_{PHL} is longer than τ_{PLH} (contrary to the upper output v_{out-}). The delays for v_{out-} are approximated by (45) and (46).
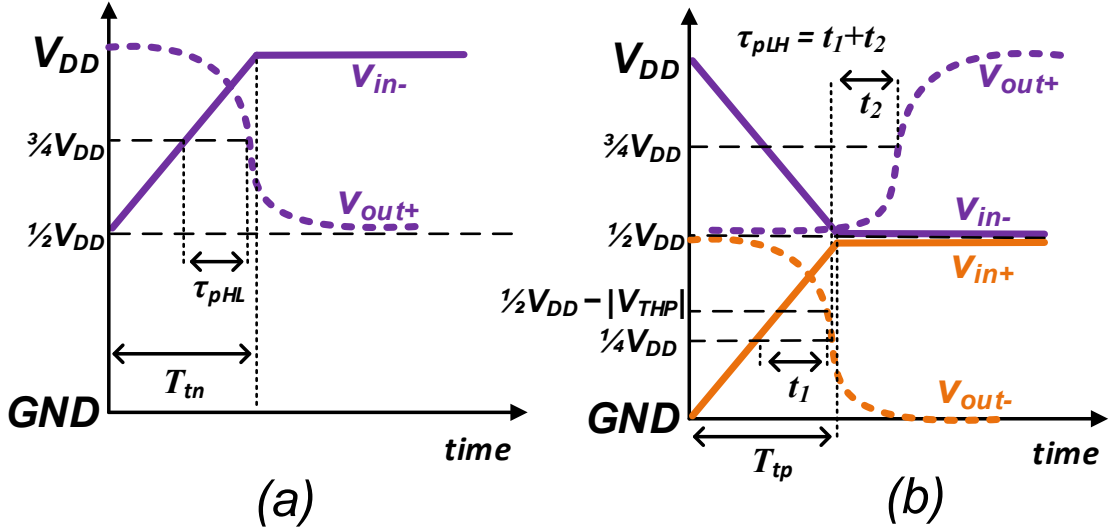
Fig. 55. Vertical delay cell waveforms and signal transitions details for a) τ_{pHL}, and b) τ_{pLH} in the v_{out+} (upper) output.

$$\tau_{PHL} = 2K_{HL}T_{tn}\left[\left(\frac{v_{TN} + \alpha_N}{1 + \alpha_N} + C_L\frac{V_{DD}}{2I_{DON}}\right) - \frac{1}{2}\right] \tag{45}$$

$$\tau_{PLH} = K_{LH}T_{tp}\left[\left(\frac{v_{TP} + \alpha_P}{1 + \alpha_P} + C_L\frac{V_{DD}}{2I_{DOP}}\right) - \frac{1}{2}\right] \tag{46}$$

To mitigate the delay asymmetry which reduces the maximum achievable speed of the cell, two tiny helper transistors were added to accelerate the transition of the lagging delay path (τ_{PHL} for v_{out-}, and τ_{PLH} for v_{out+}). The final form of the vertical delay cell is shown in Fig. 56a, where the core of the delay cell corresponding to Fig. 52b is drawn in bold style and the added helper transistors (M_{B1} and M_{B2}) are shown in lighter color. For a low-to-high transition at v_{out+} to occur (going from the second to the first state, as show

in Fig. 53b→a), M_{L2} needs to first switch to triode region in order to eventually fully turn on M_{L1}. To quickly push M_{L2} to triode region without increasing the size of M_{D1} (which increases the input capacitance), transistor M_{B1} in Fig. 56a, takes advantage of the falling input at v_{in-}, which originally triggered the low-to-high transition, to help raise the M_{L2} gate voltage. Similarly, for a high-to-low transition at v_{out-}, M_{L1} needs to switch to triode region for M_{L2} to fully turn on and propagate GND to v_{out-}. In this case, transistor M_{B2} uses the rising-input at v_{in+} to contribute to the discharge of the M_{L1} gate.
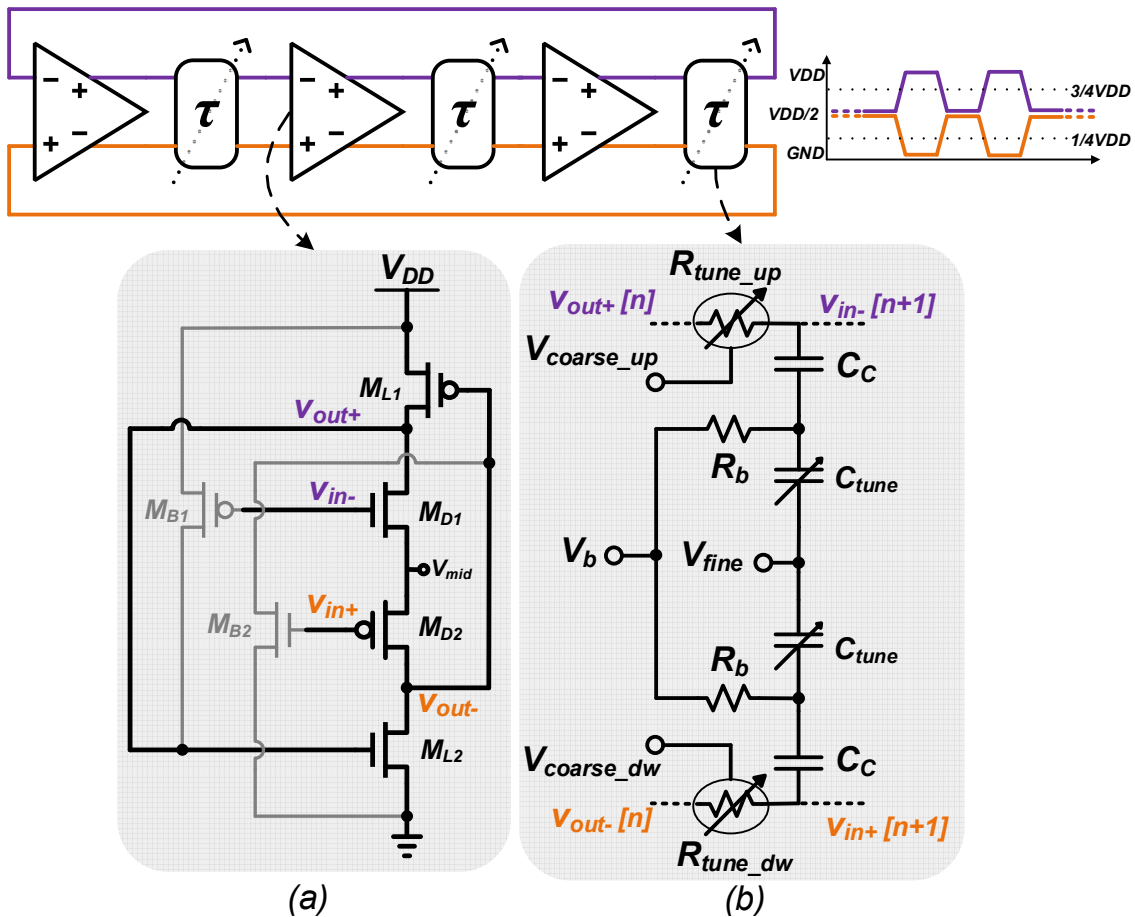
Fig. 56. *VRO* and its building blocks: a) vertical delay cell, and b) RC delay tuning cell.

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Three vertical delay cells are used to form the *VRO*. While the delay cell is differential, and it is possible to use an even number of stages to build a ring oscillator, due to the different common-mode levels of the differential outputs, an odd number should be used to avoid the use of an inter-stage level shifter. Fig. 56b shows the tuning circuit used to achieve a wide delay (and frequency) range of operation. A resistor-capacitor array is used to modulate the total delay. The coarse control is obtained via a voltage-controlled resistor implemented with a PMOS (R_{tune_up}) and an NMOS (R_{tune_dw}). Using different type of transistors for coarse control helps to compensate for the different common-mode levels of v_{out+} and v_{out-}. The fine control is provided by a voltage-controlled varactor (C_{tune}) in series with a fixed capacitor C_C. The series array decreases the overall capacitance added by the tuning circuit and allows for a fine frequency control. Resistor R_b is used to independently set the bias point for the varactor to further control its region of operation.

4.4   Power amplifier and frequency correction scheme

4.4.1 Pre-amplifiers and edge-combiner power amplifier

While it can be intuitively concluded that the use of a current recycling *VRO* reduces the overall power consumption of the Tx, a careful interfacing between the *VRO* and the PA is still required to maximize the ultra-low power characteristic of the *VRO*. The selected PA architecture was previously exploited in [50] to ensemble a low power Tx. Due to its (AND-OR) logic gate-like structure, the so-called edge-combiner PA

performs an implicit frequency multiplication at its output port when its input signals are properly routed. The operation of the edge-combiner is analogous to that of the combinational circuit in Fig. 57, where three equally spaced clock signals Φ_1, Φ_2, and Φ_3 with period T (frequency $F = T^{-1}$) act as inputs of the AND-OR combinational circuit. Due to the precise delay among the input signals, the output of the OR gate is a signal with a period of $\frac{1}{3}T$ (or a frequency $3F$).
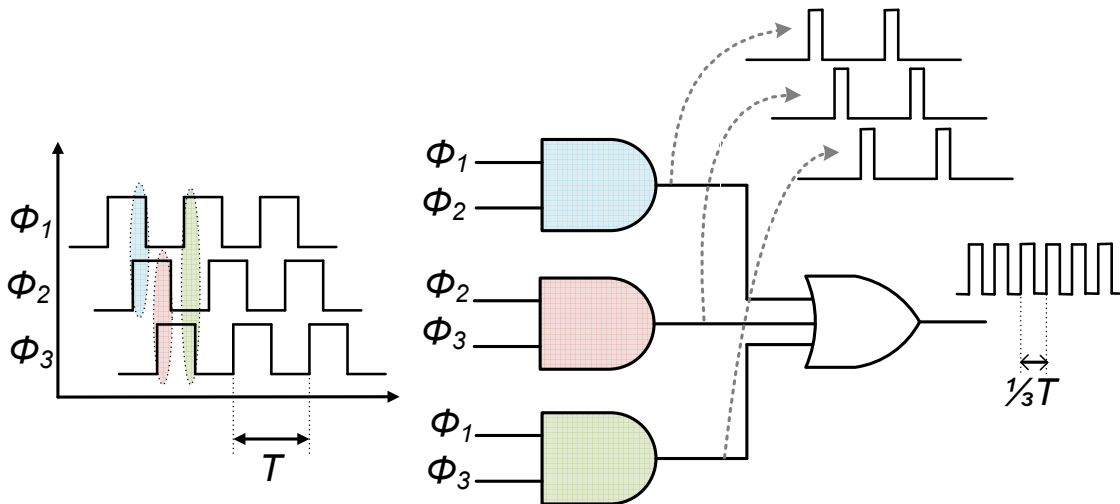
Fig. 57. Conceptual description of the operation of the edge-combiner as a logic gate array.

As illustrated in Fig. 56, the vertical nature of the delay cells used in the *VRO* result in differential output signals with similar voltage swings but centered on different common-mode voltages (V_{CM}). The circuit schematics of the *VRO* buffer acting as swing restoring stage and the edge-combiner PA is shown in Fig. 58. Out of the six 60°-spaced phases available from the *VRO*, three have a $\frac{1}{2}V_{DD}$ to V_{DD} swing, and the other three sway between 0 (ground) and $\frac{1}{2}V_{DD}$. To simplify the design of the edge combiner and increase

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the isolation between the *VRO* and the PA, the capacitively coupled, single-ended pseudo-differential buffer illustrated in Fig. 58 is used.
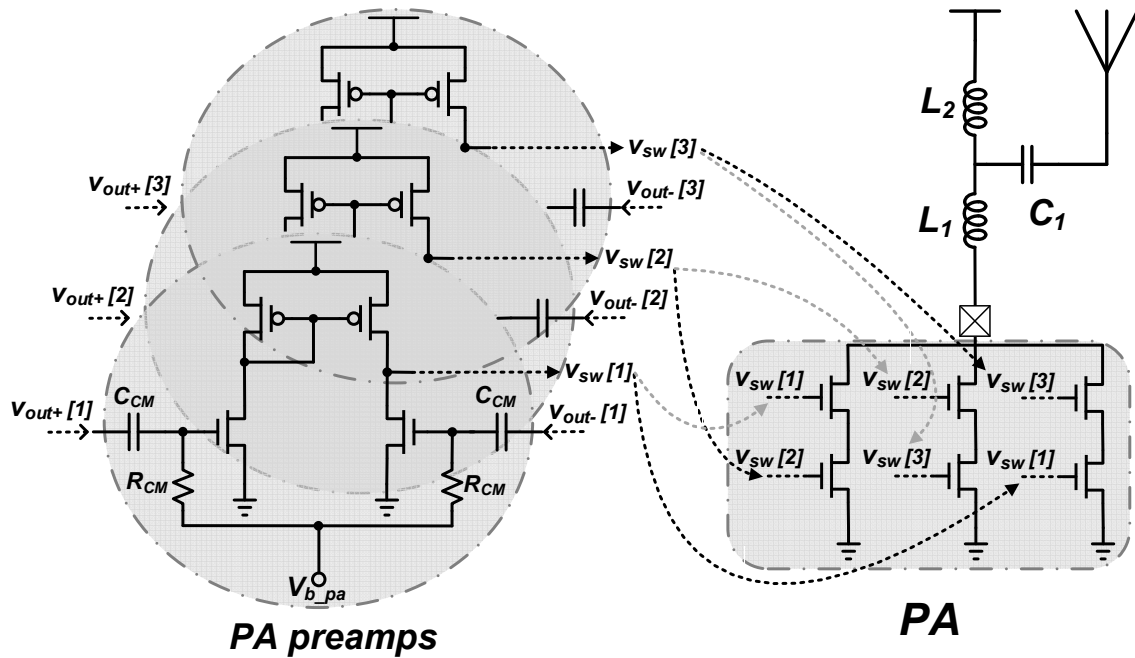
Fig. 58. Edge-combiner PA and the pre-amplifiers used to interface with the *VRO*.

AC-coupling (via capacitor C_{CM} in Fig. 58) removes the different V_{CM} of the *VRO* outputs and enables an independent definition of the pre-amplifiers (preamps) bias point (via R_{CM}) for optimum power performance. Using the complementary phases of the *VRO* at every pre-amplifier doubles the absolute signal swing available at the input of the edge-combiner PA which minimizes the on-resistance of the PA switch transistors.

Unlike [50], which uses a 9x frequency multiplication factor, we have used a 3x factor in the edge-combiner. While to reduce the effect of delay mismatches in the *VRO* at the PA output. Mismatches between the individual vertical delay-cells introduce

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spurious tones at the PA output with an offset f_{VRO} with respect to f_{RF}. In our implementation, due to the 3x multiplication factor, the potential added spur would appear ±300 MHz away from f_{RF}. While it might be argued that the low reference frequency required in edge-combiners using larger multiplication factors [50, 103] enables further reduction in the LO power consumption, this does not necessarily hold when an ultra-low power delay cell is used to generate a higher frequency reference. Furthermore, our approach eliminates the need for an external crystal oscillator in the MHz range and allows for a potential mismatch-induced spur to be heavily attenuated at the PA output bandpass filter (matching network). For the PA termination, an inductor-tapped matching network is used to transform the impedance looking into the drain of the switches in the PA to a suitable low impedance (50 Ω).

4.4.2 Digital calibration scheme for LO frequency correction

As previously discussed, the characteristics of the wideband BFSK modulation employed allow for an LO generation based on an open-loop *VRO*. While this approach reduces power consumption of the LO, ring-oscillators tend to suffer large frequency drifts due to temperature and process variations [104]. Thus, some form of frequency correction is necessary before initiating a transmission.

The digitally-assisted frequency calibration scheme implemented for this purpose is shown in Fig. 49. The adopted frequency correction concept relies on the availability of an on-chip highly accurate reference frequency with period T_{REF} ($1/f_{REF}$). An external

Altera Cyclone-V FPGA determines how many f_{VRO} periods fit into one T_{REF} period to determine if f_{VRO} is above or below target. After resolving for the sign of the error, a binary search algorithm is employed to speed-up or slow-down the *VRO*. During every iteration of the algorithm, two 7-bit words carrying the updated fine (FINE[6:0]) and coarse (COAR[6:0]) tuning information are generated and routed to the parallel calibration port in the Tx chip. Three 7-bit resistive string based digital-to-analog converters (DAC) are used to translate FINE[6:0] and COAR[6:0] into analog voltages that can be applied to the RC-delay tuning circuit of Fig. 56b. When the algorithm has converged within its minimum detectable error, the final values of FINE[6:0] and COAR[6:0] can be stored in ROM space, avoiding the need to rerun the search algorithm unless a calibration request is prompted. A flow diagram of the binary search algorithm implemented in the FPGA is shown in Fig. 59 . While we have used an external FPGA for the digitally-assisted calibration approach to demonstrate our ultra-low power Tx concept, the synthesis and integration of binary search algorithms and its variants in the form of state machines [105] have been previously demonstrated and can be seamlessly integrated for a fully monolithic solution.
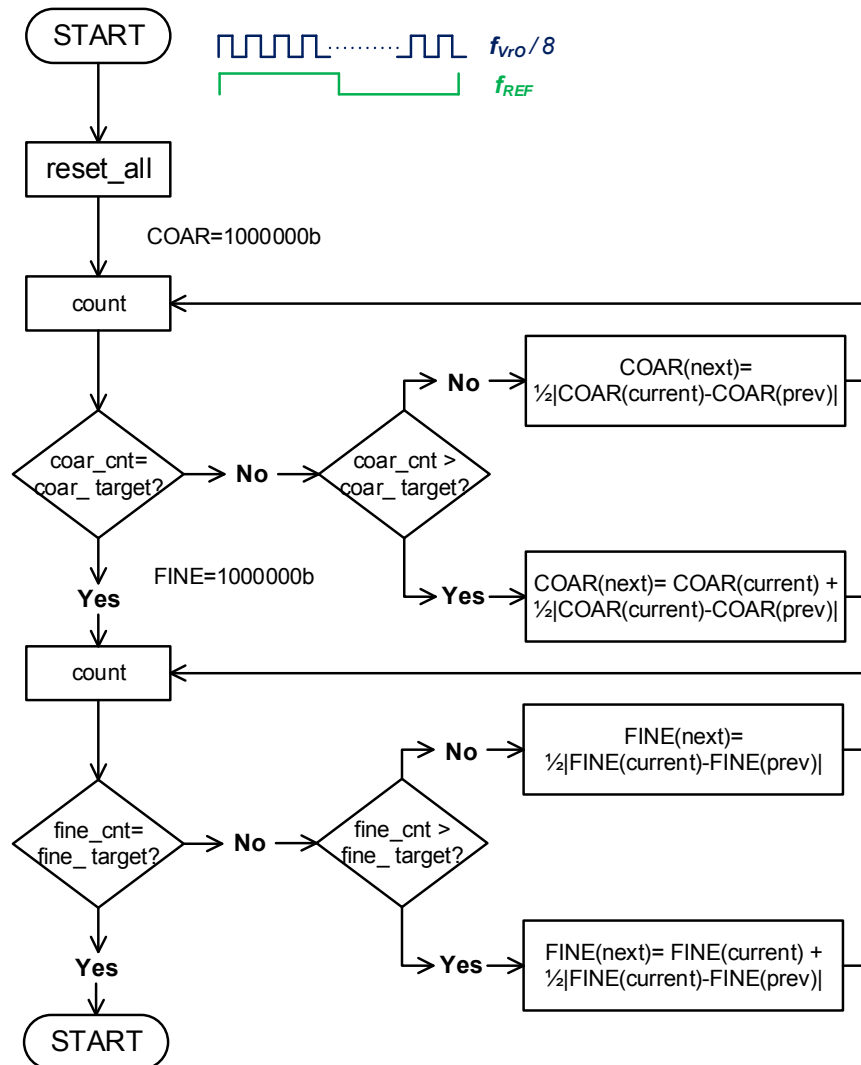
Fig. 59. Binary search algorithm used to calibrate the *VRO* frequency.

The resistive-string-based DAC is shown in Fig. 60. Three such DACs are used to generate the V_{fine}, V_{coarse_up} and V_{coarse_dw} input signals for the *VRO* tuning circuit. While the V_{fine} DAC operates in a standalone fashion, the V_{coarse_up} and V_{coarse_dw} DACs share a ½VDD voltage reference to define the maximum and minimum levels of the full-scale voltage, respectively. The different full-scale ranges for the up and down coarse controls

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compensate for the different V_{CM} in the upper and lower loops in the *VRO*, keeping symmetry on the delay added by the tuning stage on both upper and lower loops.
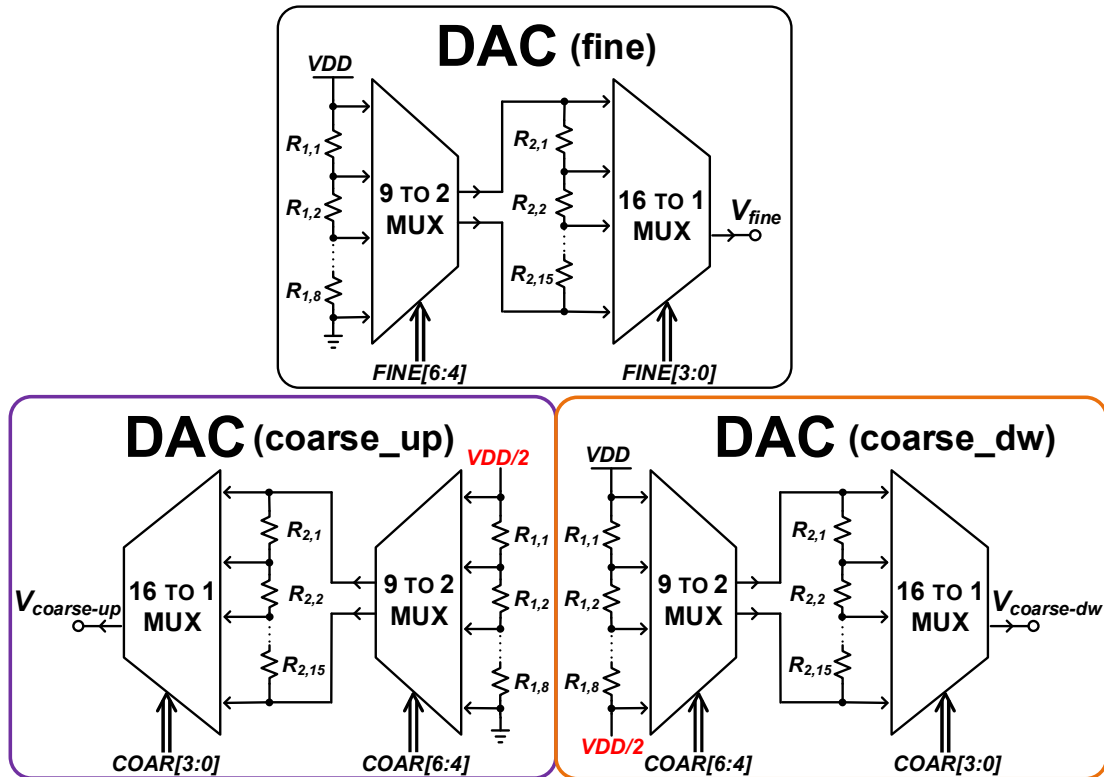
Fig. 60. Resistive-string-based DACs used to generate the tuning voltages for the RC delay tuning cell.

The intrinsic monotonicity of this DAC structure makes it an ideal candidate for our application. Furthermore a segmented, two-stage resistor string [106] decreases the number of resistors required to implement every 7-bit DAC from 128 to only 24. In this case, the first DAC stage resolves the 3 MSBs (N=3) and the second stage resolves the 4 LSBs (M=4). Due to the direct, unbuffered connection between the two resistor segments [107], the complete resistor string corresponding to the LSBs appears in parallel with the

selected resistor from the MSBs string. For $R = R_{1,1\text{-}N} = R_{2, 1\text{-}M}$, the effective selected resistor in the MSB string becomes $^{15}/_{16}R$ which represents an induced error of 1 LSB (of the second DAC segment). Most importantly, this slight deviation from the ideal R and its equivalent voltage drop does not impact the monotonicity of the DAC, nor does it jeopardize the convergence of the search algorithm. Note that while the DAC output impedance changes for every code, this is not a concern since the DACs drive purely capacitive loads in the tuning circuit (Fig. 56b).

By guaranteeing monotonicity, the selected DAC structure meets the first of the two most important characteristics for our application, with the second being low power consumption. To achieve the latter, R is selected to be ~30 kΩ. The required 9 to 2 MUX and 16 to 1 MUX are based on a transmission-gate implementation, and the digital logic to decode both MUX inputs only needs to operate at low frequencies (proportional to the data rate).

A Pierce oscillator circuit, shown in Fig. 61, is implemented using an external 32.768 kHz crystal oscillator (XO). The XO output signal f_{REF} is used by the FPGA to calculate the frequency error in the $f_{VRO}/8$ signal. In Fig. 61, transistors M_1 through M_5 operate in the subthreshold region, and together with R_1 form a bias current (i_{bias}) generator based on the mutual mobility and threshold voltage temperature compensation principle [108]. In this approach, it is possible to carefully size M_5 (240 nm/40 μm) to push it into deep sub-threshold, such that it operates around its zero-temperature-coefficient region when biased with a constant voltage (via M_1-M_4 subthreshold divider). This circuit yields a (quasi)-temperature-stable current i_{bias} that is mirrored to the core of the crystal oscillator

(XO core). The 50 nA current i_{bias} is designed to be 5 times larger than the minimum required to compensate the crystal losses, this guarantees the XO start-up and a consistent oscillation frequency across temperature variations. The stabilized XO signal is further amplified and buffered via the structure formed by transistors M_9-M_{15} and the two buffers in the XO amplification and buffer stage in Fig. 61. A 12:1 scaled replica of the XO core is used for the generation of a reference voltage (X_{ref}) used in the XO amplification stage. X_{ref} tracks across PVT variations in the operating point of the XO-stabilization inverter, and guarantees the proper operation of the XO amplification stage.
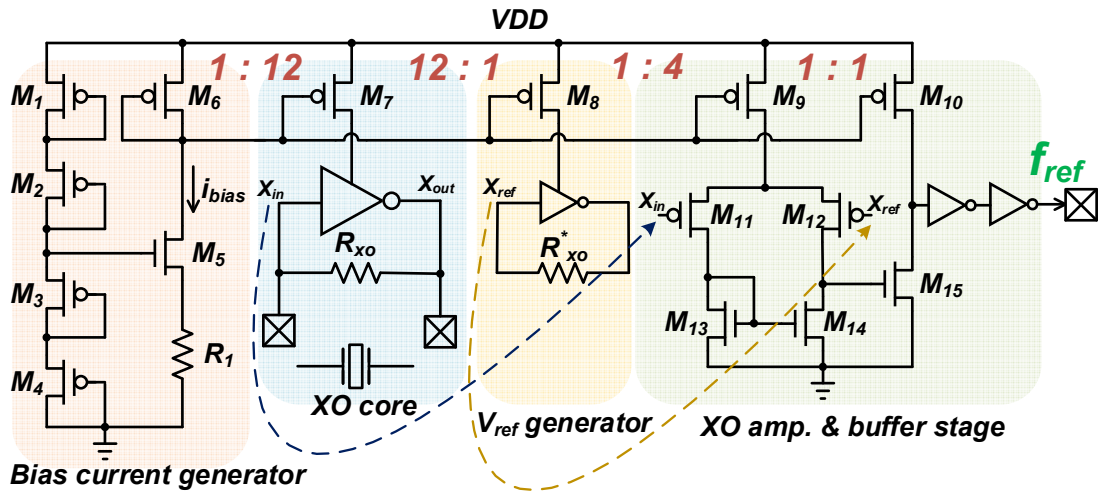
Fig. 61. Crystal oscillator schematic including bias current generation and buffering stage.

4.5   Experimental results

The Tx was implemented and fabricated in 0.18 μm CMOS technology and encapsulated in a QFN56 package. The die microphotograph is shown in Fig. 62. . While

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the die area is 2 x 2 mm, the design is clearly pad-limited. The active area occupied by the

Tx is only 0.112 mm^2, including the required buffers for testing purposes.
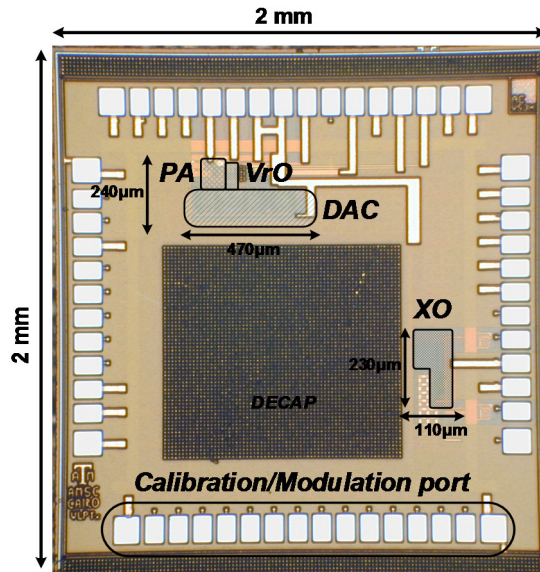
Fig. 62. Die microphotograph of the Tx.

The measurement results for the achievable tuning range of the *VRO* are shown in

Fig. 63. Taking advantage of the digital nature of the vertical delay cell, by means of

which, the propagation delay is proportional to the net supply voltage (highlighted by the

V_{DD} presence in (41), (42), (45) and (46)), a third degree of frequency controllability was

added by varying the *VRO* supply. As a result, the total observed range is between 50 MHz

and 350 MHz with a maximum supply of 1.75 V. Furthermore, since f_{VRO} is effectively

multiplied by 3 at the PA output, the *VRO* opens the possibility for a self-contained Tx

operating from 150 MHz to 1.05 GHz. Using the COARSE control word, it is possible to

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discretely tune the frequency in 600 KHz steps (COARSE LSB). Conversely, the FINE control word allows a programmability in 60 KHz steps.
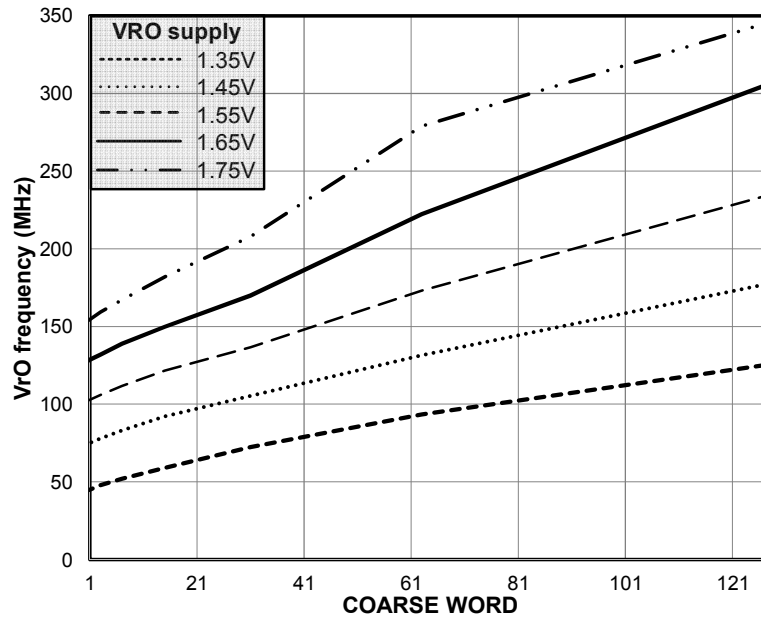
Fig. 63. *VRO* **measured tuning range 50–350 MHz translates into a PA RF range of 0.15–1.05 GHz.**

A capacitor-less low dropout voltage regulator (CL-LDO) can be used to provide the variable *VRO* supply level required to maximize the oscillator tuning range. Shown in Fig. 64 are two possible implementations of an LDO with variable output voltage (V_{OUT}). Since V_{OUT} is approximated by (47), when using an error amplifier (EA) with large DC gain (A_{EA}) V_{OUT} is mainly related to the reference voltage (V_{ref}) by the resistive feedback factor (β). Thus, in Fig. 64a, β can be modified through a MUX for a variable V_{OUT} in discrete steps. Conversely, in the approach of Fig. 64b β is kept constant while V_{ref} is assumed to be variable. Both approaches achieve the same goal of a variable V_{OUT}.

However, the former approach alters the loop stability every time a different β is selected, and the latter transfers the problem to designing an accurate, variable voltage reference. If such a reference is available on-chip, the latter approach is preferred. On the contrary, a careful design of the frequency compensation scheme is required to use the alternative in Fig. 64a.

$$V_{OUT} \cong \frac{V_{IN}}{A_{EA}\beta} + \frac{V_{ref}}{\beta} \tag{47}$$

(a)   (b)
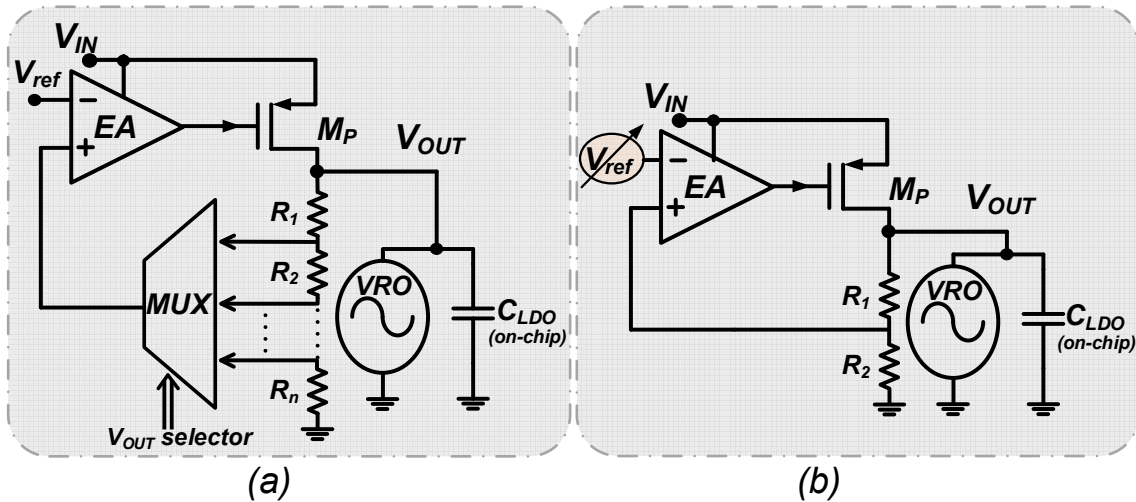
Fig. 64. Potential implementations of an LDO with variable V_{OUT}: a) Modified feedback factor, and b) Variable reference voltage.

The measured frequency stability against temperature of the XO is shown in Fig. 65. Due to the i_{bias} characteristics, there is only a total variation of 7 Hz from -10 °C to 100 °C, which accounts for a total accuracy of 213 ppm.
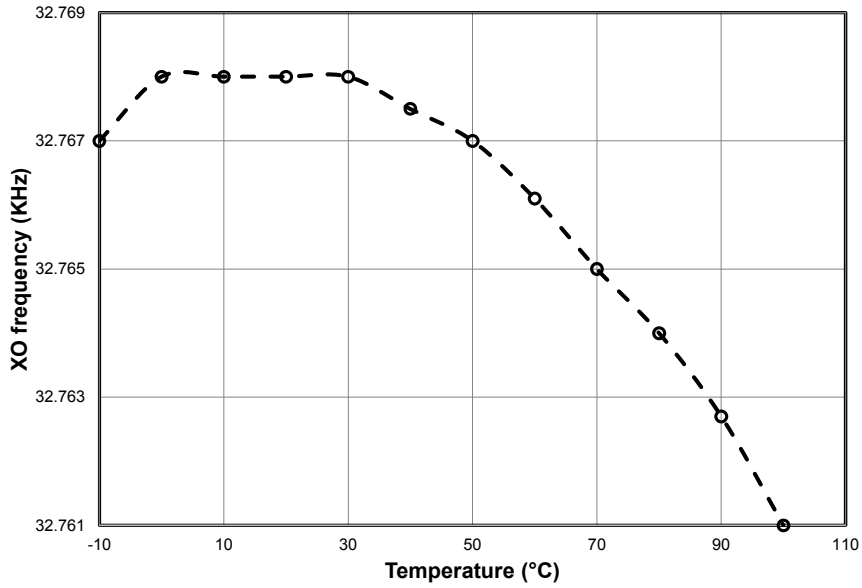
Fig. 65. XO frequency stability against temperature.

The maximum P_{out} available at the antenna was measured to be −10 dBm as shown in Fig. 66. In this case, the carrier-to-spur ratio is better than 43 dB. More importantly, the spurs observed in Fig. 66 with an offset of $f_{RF}/24$ (±38.125 MHz) are due to the auxiliary *VRO* frequency divider used for calibration purposes and are only present during the calibration stage. Fig. 67 shows the BFSK modulated signal using f_1 and f_2 tones with a *Δf* of 2 MHz. As a result, the inter-tone interference is 42 dB below f_1 and f_2.

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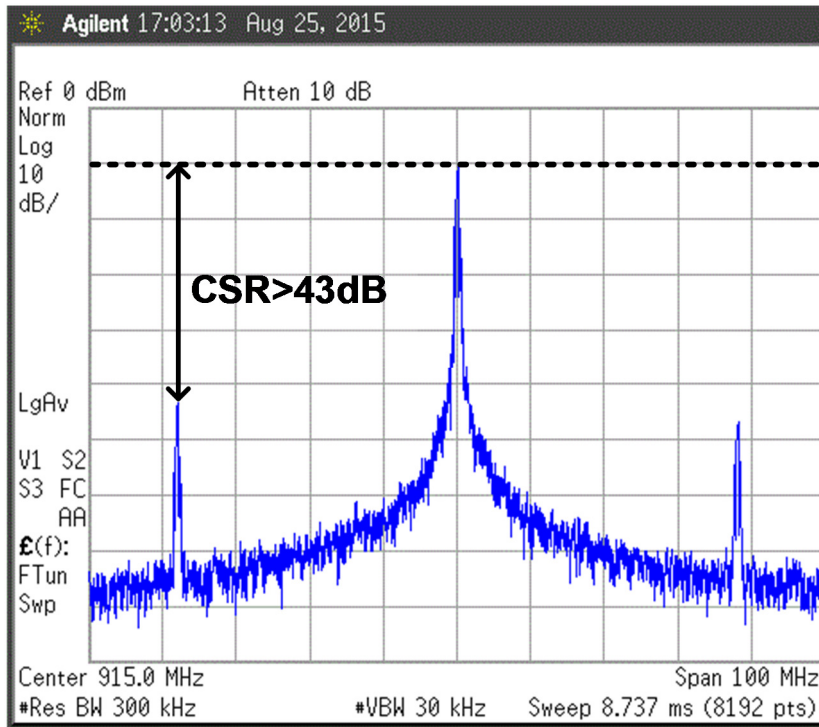
Fig. 66. PA maximum output power showing a 43 dB carrier-to-spur ratio (CSR).
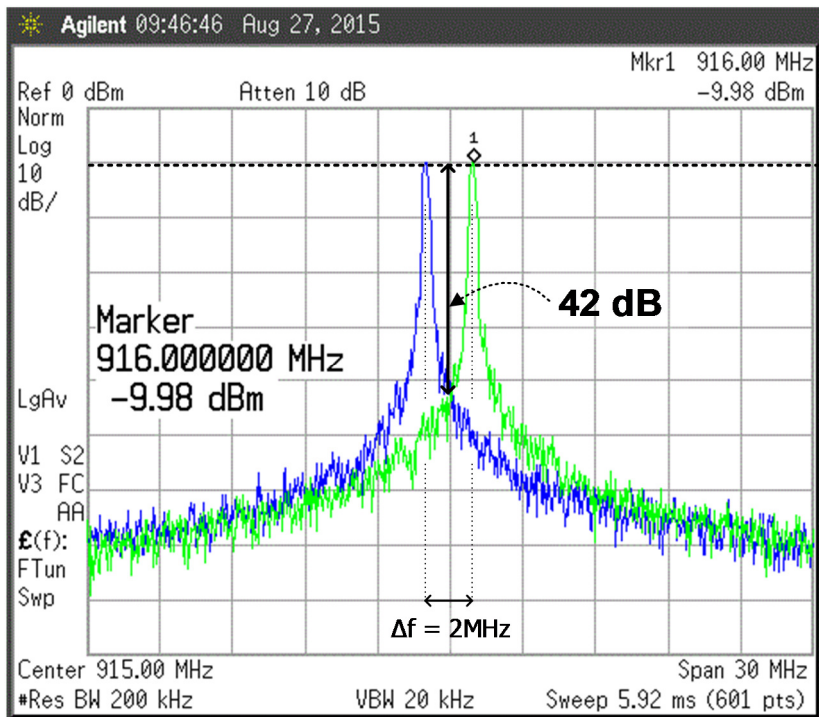
Fig. 67. BFSK modulated signal at the PA output for the 2 MHz frequency deviation case.

The phase noise of the *VRO* and the Tx carrier is shown in Fig. 68. While the close-in phase noise (10–80 KHz offsets) has the typical flat-looking shape of free-running oscillators, the measured phase noise at 1 MHz offset is –106 dBc/Hz in the case of the *VRO* running at 300 MHz, and –94 dBc/Hz in the case of the PA carrier output at $3f_{VRO}$ (~900MHz). Having established that our application centers its interest in the far-out phase noise of the LO, the obtained results enable the successful transmission. To further illustrate this point, a bit pattern was transmitted using the proposed Tx at 1 and 3 Mbps data rates. Fig. 69 shows the time representation of such bit patterns received using a signal analyzer. The correct reception of the bit patterns shows that the use of our *VRO* for LO purposes does not introduce significant interference between f_1 and f_2 due to the large frequency deviation employed.

(a)   (b)
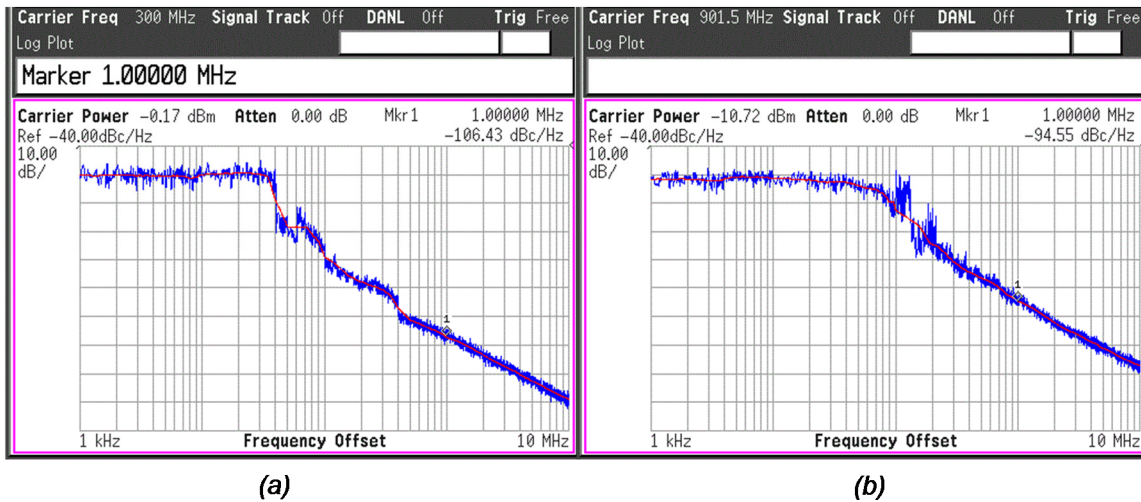
Fig. 68. Phase noise of a) *VRO* with f_{VRO} of 300 MHz for -106 dBc/Hz @ 1 MHz, and b) Tx carrier at 900 MHz with -94 dBc/Hz @ 1 MHz.
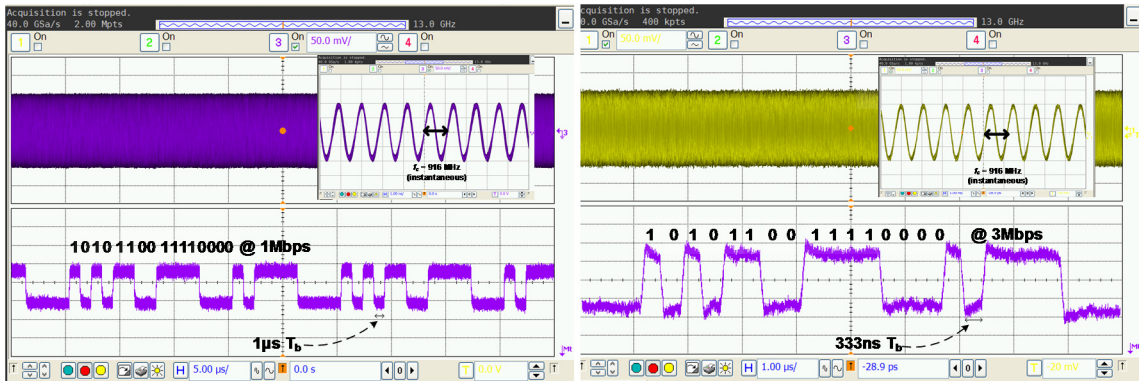
Fig. 69. Transmitted bit pattern (1010110011110000) at 1 and 3 Mbps received in a signal analyzer.

The current consumption of the Tx for a −15 dBm P_{out} is 363 µA from 1.65 V (*VRO*), and 1.8 V (PA and digital circuitry). The by-block power consumption breakdown is shown in Fig. 70. Under these conditions the Tx energy efficiency is 0.2 nJ/bit. Furthermore, the normalized Tx efficiency at the maximum P_{out} is 3.1 nJ/bit·mW.
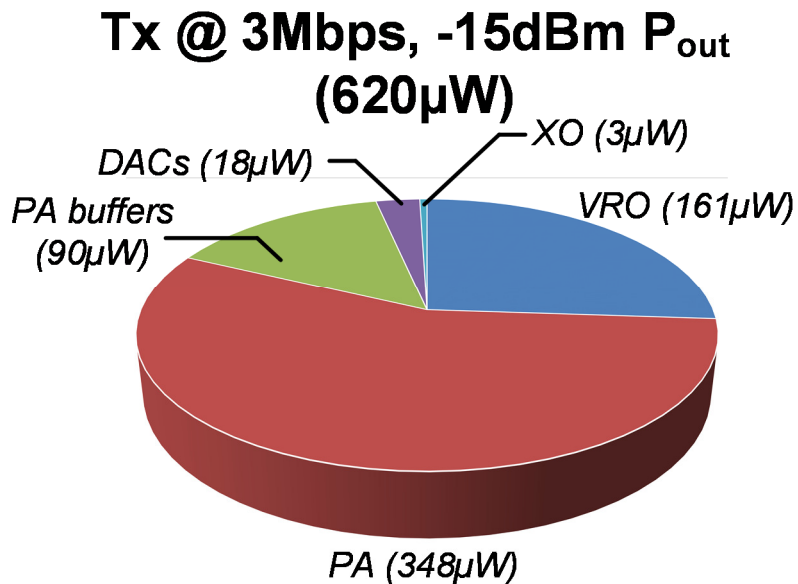
Fig. 70. Tx power consumption per circuit block.

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To put the obtained experimental results in context, Table 12 shows the measurement results summary and the performance comparison with other state-of-the-art low power Tx. Note that [50] and [88] have absolute power consumptions considerably lower than our work. However, [50] operates in the 400 MHz band with a 200 kbps data rate, requires a high frequency external crystal (48 MHz) and reports the power consumption at −17 dBm P_{out}. Similarly, [88] operates at only −28.6 dBm P_{out}. Conversely, we have measured the energy efficiency at 3 Mbps data rate and −10 dBm and −15 dBm P_{out}. The 0.2 nJ/bit energy efficiency is superior to most compared works in Table 12. Furthermore, the 3.1 nJ/bit·mW normalized energy efficiency at −10 dBm P_{out} is the best amongst the compared works. Moreover, the proposed Tx has the largest available tuning range, which potentially enables a wide operating range while maintaining its low power consumption characteristics.

Table 12. Performance summary and comparison for the proposed Tx.

	[50]	[93]	[90]	[92]	[89]	[88]	This work
Frequency (MHz)	400	900	915	2400	400	5800	915
f_{RF} tuning range (MHz)	288-468	780-950	780-1000	1700-2500	402-450	N/A	**150-1050**
f_{RF} tuning range (%)	45	52	24	33	12	N/A	**98**
Data rate (kbps)	200	200	10	2000	4500	2500	**3000**
P_{out} max. (dBm)	-11	-3	-3	0	-5	N/A	-10
Technology (nm)	130	130	90	90	40	65	180
Power cons. (µW)	90	1700	900	4600	1770	113	935/620
@ P_{out} (dBm)	-17	-10	-6	-10	-10	-28.6	-10/-15
FOM$_1$*(nJ/bit)	0.450	8.50	90	2.70	0.390	0.045	0.311/**0.200**
FOM$_2$** (nJ/(bit·mW))	22.55	85	358.3	27	3.9	32.6	**3.1**/6.3
Modulation	BFSK	FSK/MSK	OOK/ASK/ 2-tone/BPSK	HS-OQPSK/ π/4-DQPSK/ GFSK	GMSK/ π/4-D8PSK/ π/8-D8PSK	32-QAM	BFSK

*FOM$_1$ = Power consumption/Data rate. ** FOM$_2$=FOM$_1$/P_{out}. Tuning range (%) = (tuning range in MHz)/f_{RF} x 100.

4.6   Conclusions

This work presented an ultra-low power, PLL-less, energy efficient transmitter for Internet-of-Thing applications. A current reusing, vertical delay cell is introduced and used to build a vertical ring-oscillator with ultra-low power consumption. Due to the use of wideband BFSK modulation, it is possible to use the vertical ring oscillator as the Tx local oscillator generator. A digitally-assisted frequency correction and calibration algorithm is implemented to compensate the possible frequency variations that the oscillator might experience. The power amplifier is based on an edge-combiner, which effectively multiplies the frequency at the oscillator output by a factor of 3. The Tx was fabricated in 0.18 μm CMOS technology and occupies an active area of 0.112 mm^2. Due to the wide tuning range of the oscillator, the total RF carrier tunability is 0.15 GHz−1.05 GHz. The maximum output power is −10 dBm, and the normalized energy efficiency at this power is 3.1 nJ/bit·mW while transmitting with a 3 Mbps data rate.

CHAPTER V

A BICMOS RING OSCILLATOR WITH FEEDFORWARD PATH FOR IMPROVED

POWER SUPPLY REJECTION

The voltage-controlled oscillator (VCO) is often regarded as the core circuit block on clock generation schemes employed in most of modern electronic systems. The selection and design of the VCO ultimately defines the performance of entire systems. Typically the selection of the VCO is reduced to two choices: inductor-capacitor-based (LC) or ring oscillator (RO). Table 13 presents a brief comparison of the two approaches. Whereas LC oscillators exhibit better noise performance and lower supply sensitivity; ROs are more compact and have a larger tuning range than LC structures. Furthermore, RO can be directly integrated in standard CMOS processes.

Table 13. Comparison between LC-based and ring oscillator (RO).

	LC	RO
Area	Expensive	Cheap
Tuning range	Narrow	Wide
Phase noise	Good	Not the best
# phases	2 (differential)	Multiple
Supply sens.	Low	High

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Available RO structures with improved noise performance lean heavily on power hungry voltage regulators [109] or complex calibration and compensation circuits [110] to reduce the supply sensitivity of the delay cells in the RO. While these approaches reduce the RO frequency variation and improve the jitter performance under supply noise, they are expensive and do not solve the supply noise problem by construction. This chapter discusses the implementation of a supply noise tolerant RO based on BiCMOS delay cells. To improve the RO supply noise immunity, a low-cost voltage regulator is used in combination with a high frequency feedforward path from the supply rail to inner nodes within the delay cell. The composite solution provides superior supply noise tolerance without strongly increasing the overall power consumption.

5.1 The problem of supply noise in ring oscillators

The most important sources of timing uncertainty or jitter in the output signal of a RO-based VCO are *i)* the intrinsic noise of the transistors and devices forming the RO, and *ii)* noise in the supply rail of the RO [111]. While it is possible to reduce the intrinsic noise at expense of larger devices in the RO and higher current consumption [112], the noise in the supply of the RO is typically dependent on the switching activity of neighbor circuits and the quality of the regulator that generates the supply (when existing). Thus, it is not uncommon for the supply noise to dominate the RO intrinsic noise [113].

In light of the situation, multiple solutions have been proposed to mitigate the impact of supply noise in ROs, some targeting delay cells with reduced supply sensitivity

and some others using sophisticated voltage regulators, complex biasing techniques and meticulous calibration of the positive and negative supply-sensitivity components of particular delay cells. In [114], Maneatis proposed a differential delay-cell using symmetric loads and self-biasing. In the Maneatis delay cell, the differential mode resistance of the delay cell is independent of the common-mode voltage thanks to the linear I-V characteristics of the symmetric load used. As a result, the delay of the cell is kept constant under supply variations (in the absence of mismatch). More recently, Pankratz [113] proposed a source-follower-based delay cell in a multiloop RO structure. The intrinsic saturation resistance of the source-follower improves the supply noise isolation in the RO at expense of a complex multiloop structure to guarantee sufficient delay-cell gain for sustained oscillations. The supply-regulated approach to reduce supply-noise-induced jitter in RO-based PLLs typically requires a voltage regulator with high power consumption to avoid disturbing the PLL dynamics [115] or convoluted split-tuned architectures with coarse and fine tuning loops for the RO [116]. The last type of approach for supply-noise influence reduction in RO calls for intensive calibration of the positive and negative supply-sensitivity components for the delay cell in question. Amongst the works exploiting this technique are [117], which uses a modified Lee-Kim delay cell [99]. In [117], an auxiliary transistor is trimmed to exhibit a supply sensitivity opposite to that of the delay cell. Using a successive approximation algorithm, the transistor with counter-sensitivity is digitally calibrated to suppress the supply sensitivity of the delay cell. Similarly, in [111] the supply sensitivity of the delay cell is reduced by means of dynamic and joint biasing of the pull-up and pull-down components of the delay cell used.

As can be concluded from the previous discussion, the approaches undertaken to address the supply-noise problem in delay-cell-based RO are delay-cell dependent and some degree of optimization and/or calibration is sometimes required. The remaining of this chapter discusses the implementation of a bipolar-MOS (BiCMOS) differential delay cell that uses a dual approach to reduce the supply-noise influence on the oscillation frequency of an RO built using such BiCMOS delay cells.

5.2   A BiCMOS delay cell for ring oscillators

A current-mode logic (CML) differential delay cell is shown in Fig. 71a. Due to its partial output voltage swing (compared to the typical CMOS inverter which operates with full swing) and the fact that the bias current (I_b) can be quickly steered from one branch to the other (e.g. from v_{on} to v_{op}), the CML cell is widely accepted as one of the faster commutating delay cells [118]. As such, it has long been used to implement high speed frequency dividers [119] and ring oscillators [120]. However, previous works have demonstrated that its supply-noise sensitivity is linked to the characteristics and noise processing of the cell's load [118, 121] (R_L in Fig. 71a). These works have proposed sensitivity-compensation techniques based on careful tuning of the admittance of additional circuits with the proper supply sensitivity [121]; and similarly meticulous calibration of load varactors at the CML delay cell output [118]. While both techniques significantly reduce the supply sensitivity, the former approach increases the number of transistors per delay cell, the complexity and power consumption; and the latter technique

links the supply-sensitivity to the oscillation frequency which is certainly undesirable. Furthermore, both [118, 121] techniques rely on finding the tiny sweet spot at which the supply sensitivity is cancelled.
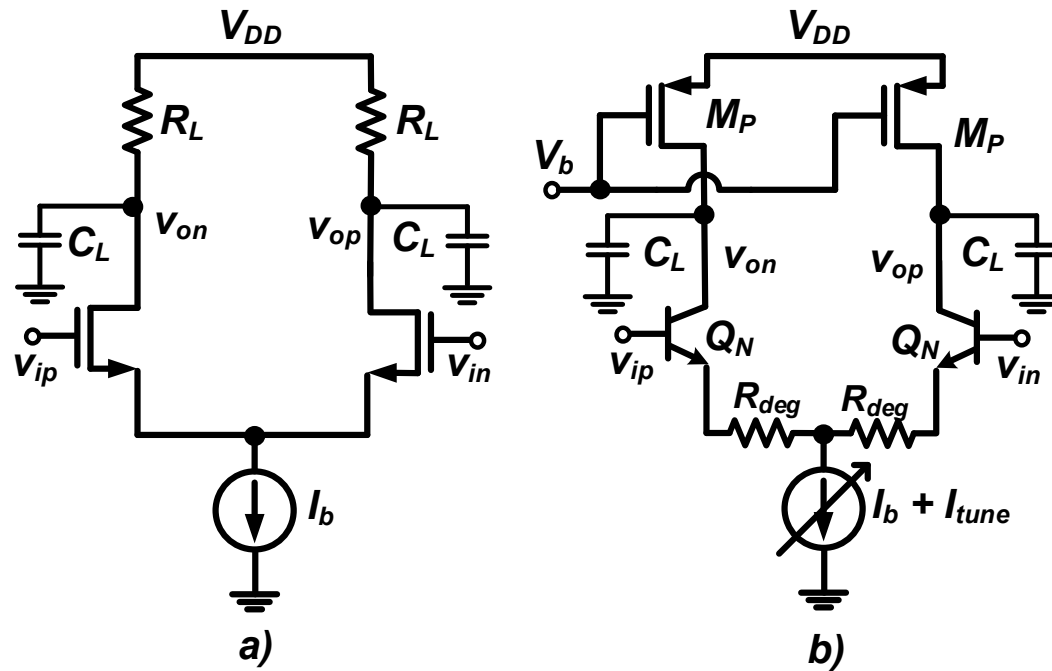
Fig. 71. a) Typical CML delay cell, and b) BiCMOS CML-like delay cell used in this work.

Shown Fig. 71b is the BiCMOS version of the current-mode logic (CML) cell used as test vehicle for the proposed supply-noise cancellation technique in this work. The NPN transistors Q_N act as the input drivers while PMOS devices M_P are permanently biased in the triode region such that they act as voltage-controlled active loads to emulate a load resistance (R_L). Resistors R_{deg} are used to improve the linear range of the RO. An NMOS cascode current mirror implements the tail current source which contains acts as bias (I_b) and frequency tuning (I_{tune}) port.

To identify the components affecting the propagation delay (τ) of the Fig. 71b delay cell, it is possible to use the linear model shown in Fig. 72, which is a modified version of the one used in [122]. The model in Fig. 72 assumes that transistors Q_N work in linear region for a partial-swing operation of the differential delay cell, and that the M_P devices are biased in triode region and show an equivalent resistance equal to R_L. Under the assumption of differential operation, the Fig. 72 model represents only half-circuit of the BiCMOS delay cell and defines (all in reference to Q_N): g_m as the transconductance, r_π as the input (base-emitter) resistance, and r_b, r_e, and r_c, as parasitic resistances at the base, emitter and collector, respectively. Similarly, Q_N parasitic capacitances at the base-emitter, base-collector, and collector-substrate (C_{be}, C_{bc}, C_{cs}, respectively) terminals are included in the model. Following [122], C_{bc} is split into intrinsic (C_{bci}) and extrinsic (C_{bcx}) components. This separation allows the model to consider the distributed nature of C_{bc} by using the technological parameter X_{cjc}, as shown in (48) and (49), where X_{cjc} ranges between 0 and 1. Note that the small signal model disregards the output resistance (r_o) of Q_N since it is assumed that the equivalent triode resistance displayed by M_P is smaller than r_o ($R_L \ll r_o$). Likewise, the gate-to-drain and drain-to-source parasitic capacitances associated with M_P are embedded in the load capacitor C_L. Subject to these conditions, it is safe to approximate the BiCMOS delay cell as a single pole system. In this case, the delay can be estimated using (50).
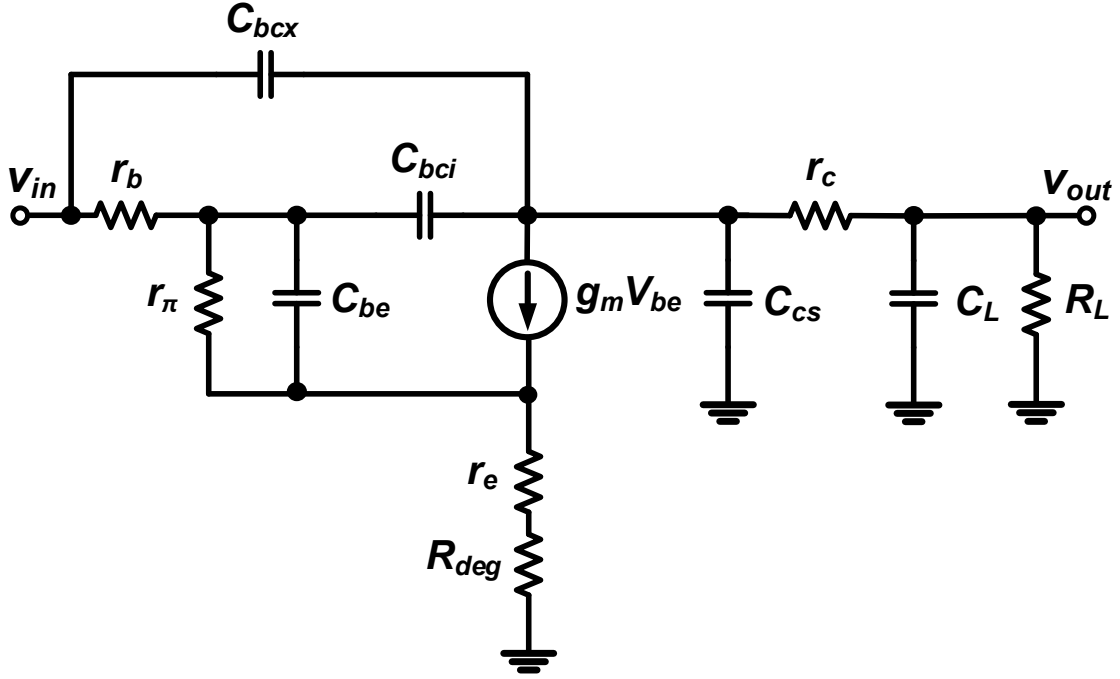
Fig. 72. Small signal model to analyze the BiCMOS CML-like delay cell [122].

$$C_{bci} = X_{cjc}C_{bc} \tag{48}$$

$$C_{bcx} = (1 - X_{cjc})C_{bc} \tag{49}$$

$$\tau = \ln 2 \left(\frac{(r_e + R_{deg} + r_b)C_{be}}{1 + g_m(r_e + R_{deg})} + r_b C_{bci}\left(1 + \frac{g_m(r_c + R_L)}{1 + g_m(r_e + R_{deg})}\right) \right. $$

$$\left. + (r_c + R_L)(C_{bci} + C_{bcx} + C_{cs}) + R_L C_L \right) \tag{50}$$

Inspecting (50) in search of the dominant source of delay variation under supply variations, it is clear that the first three components mostly depend on small parasitic capacitances of Q_N which are isolated (to some degree) from the supply rail via M_P. On the other hand, the $R_L C_L$ term in (50) involves the largest capacitor in the cell (considering inter-stage routing parasitics in a ring oscillator) and R_L which is directly modulated by

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changes in the supply (51). Thus, under constant bias current (I_b), the major threat for delay variability during supply variations (noise) comes from the voltage-supply-dependent (V_{DD}) behavior of R_L. Examining the R_L expression in (51), it is clear that variations in V_{DD} directly modify the R_L value (particularly for small output swing, $V_{sw} = V_{ds}$), and as a consequence modulate both, the delay τ and the RO oscillation frequency f_{RO}, as shown in (52) (where N is the number of delay cells composing the RO).

$$R_L = \frac{1}{\mu_p C_{ox} W_p/L_p \left(V_{DD} - V_b - |V_{THp}| - |V_{ds}|/2\right)} \quad (51)$$

$$f_{RO} = \frac{1}{2N\tau} \quad (52)$$

From the previous analysis, it can be concluded that to reduce the delay fluctuation of the BiCMOS cell and the frequency variation it entails, the equivalent R_L must be kept constant under supply (V_{DD}) variations. Note that while an implementing R_L with passive resistors keeps R_L (mostly) constant under supply variations, it directly translates such variations to the output node, which actually worsens the problem.

Embracing the fact that in the absence of a high quality LDO, some amount of supply noise will be present, solving the constant-R_L problem calls for a solution that instead of wasting valuable resources (power) in shielding the delay cell from the supply noise, sets the conditions for a by-construction noise-cancellation. A technique with these characteristics is discussed in chapter 5.3.

5.3   Low cost feedforward path

As conceptually shown in the 3-stage free-running RO of Fig. 73, low frequency supply noise can distort the shape of the RO output frequency spectrum. On the other hand, high-frequency supply noise is typically up-converted and appears as a spurious tone at an offset from f_{RO}. The impact that supply-noise has at the φ_x outputs in Fig. 73 greatly depends on the characteristics of the delay cells and the manner that each cell process the supply noise. As shown in the bottom part of Fig. 73, if an LDO is used to suppress the amount of supply noise reaching the RO at $V_{DD}*$, the distortion or deviation from the ideal f_{RO} is significantly minimized. Unfortunately, if the RO supply node is used as the RO frequency tuning port within a phase-locked-loop-based (PLL) frequency synthesizer, the intrinsic dropout voltage of the LDO reduces the available voltage headroom to tune the RO. Furthermore, to avoid disrupting the PLL stability and dynamic response, the LDO bandwidth must be much larger than that of the frequency synthesizer loop, which typically implies high power consumption in the LDO and reduces the appeal of this particular approach.

Considering the BiCMOS delay cell in Fig. 71b and having identified that the main component of the delay variability in the presence of supply noise is the V_{DD}-dependent value of R_L, it is possible to extrapolate the concept used in [25] and implement a feed-forward path from the supply to an inner node of the delay cell and theoretically prevent the processing of supply-noise in the delay cell for a supply ripple-independent operation. While the feed-forward approach was originally proposed to improve the power-supply

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rejection of an LDO [25], the goal is the same as in our application: maintain a constant source-to-gate voltage (V_{sg}) in key transistors, such that even though the source of M_P (connected to the supply in Fig. 71b) might vary due to supply ripple, the gate will vary in the same amount keeping a constant V_{sg} even in the presence of supply noise. As a consequence, R_L is also constant and both the delay τ and f_{RO} are stabilized and (ideally) supply-noise-immune.
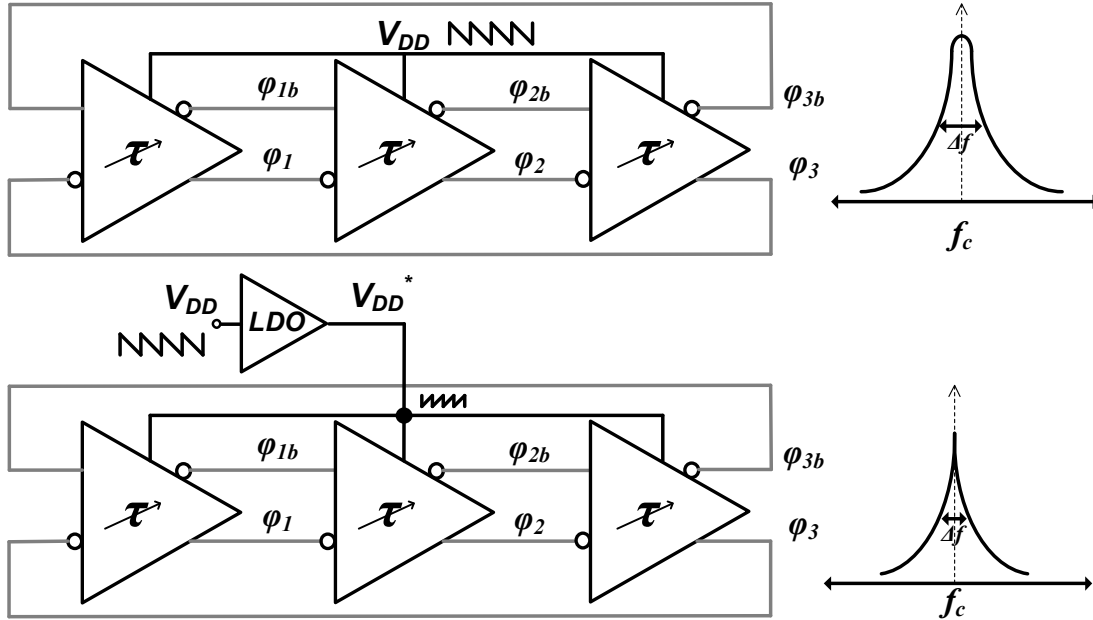
Fig. 73. Effect of supply noise in the RO frequency spectrum.

Intuitively, a high-pass filter (HPF) with slightly higher-than-DC cutoff frequency (f_{3dB}) and unity gain over a broadband range would be the best fit to ensure that the noise in the supply (source of M_P) is perfectly coupled to the gate of M_P for optimum source-gate voltage variations tracking. However, an active implementation of such filter would

demand high supply rejection and low-noise from the noise-coupling filter to avoid injecting additional noise at the gate of M_P. Unlike [25] where the LDO loop gain suppresses the intrinsic and supply noise of the feed-forward filter, in our case these two requirements demand high power consumption in the feed-forward implementation and would turn this into an expensive solution. Conversely, a passive HPF is a better candidate since it is not affected by supply noise (it does not require a supply voltage to operate). However, the passive capacitor-resistor (C-R) implementation of the HPF might incur in serious area penalties if f_{3dB} (53) is to be reduced to close to DC.

$$f_{3dB} = \frac{1}{2\pi RC} \tag{53}$$

In light of the shortcoming of both approaches, high power for high LDO bandwidth and large area for low f_{3dB} in C-R HPF, a composite solution leveraging the best characteristics of each approach is implemented, as shown in Fig. 74. A C-R HPF implements the feed-forward path $A_{FF}(s)$ in Fig. 74. The additional capacitor C_C in $A_{FF}(s)$ provides bias point isolation and avoids current leakage to ground through resistor R. Assuming a purely capacitive load at V_b due to the gate of the six M_P devices (two per delay cell in a 3-stage RO) denoted as C_g, $A_{FF}(s)$ is given by (54). Note in (54) that f_{3dB} is lower than in the simple C-R filter (53) which actually improves the noise-coupling action of the HPF at lower frequencies. Similarly, the voltage divider between C_C and C_g introduces an error in the magnitude of the supply noise couple to the gate of M_P. However, this error can be significantly reduced by choosing $C_C \gg C_g$. This capacitive relation can be achieved without important area expenditure if the M_P devices are properly sized (small L and efficient routing). For example, in this case C_C has a value of 10 pF, which is +33

times larger than the parasitic C_g, reducing the difference between the source and gate

voltages to below 3%.
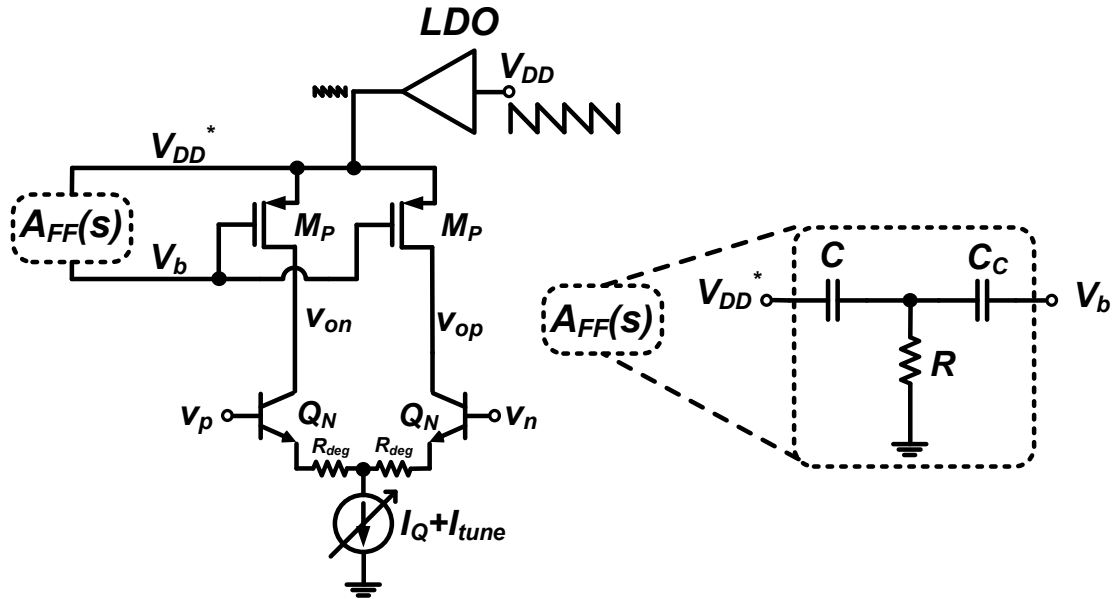
Fig. 74. Composite solution to the power supply-noise problem in a BiCMOS delay cell.

$$A_{FF}(s) = \frac{C_C}{C_g + C_C} \frac{sRC}{sR(C + C_C||C_g) + 1} \tag{54}$$

For an f_{3dB} around 4 kHz, the nominal values of R and C in the HPF are 60 pF and

640 kΩ, respectively. While theoretically this setup reject supply noise above 4 kHz, the

HPF approach does not provide any protection against low frequency supply noise. To

tackle supply noise below 4 kHz, it is possible to use a simple LDO with a bandwidth

slightly larger than f_{3dB}. In this way, low frequency noise is attenuated by the power supply

rejection (PSR) of the LDO, whereas the high frequency noise is rejected via the $A_{FF}(s)$

approach. Using an LDO with narrow bandwidth to regulate the supply of an RO within a

PLL context is only possible if the LDO is out of the synthesis loop, which implies that the RO is *not* tuned via its supply voltage. Thus, the LDO can be designed to provide strong supply rejection up to a low frequency dominant pole while operating with low power consumption. In this case, the LDO shown in Fig. 75 featuring a two-stage, Miller compensated error amplifier followed by a P-type pass transistor (M_{PASS}) is designed to provide low frequency supply noise rejection.
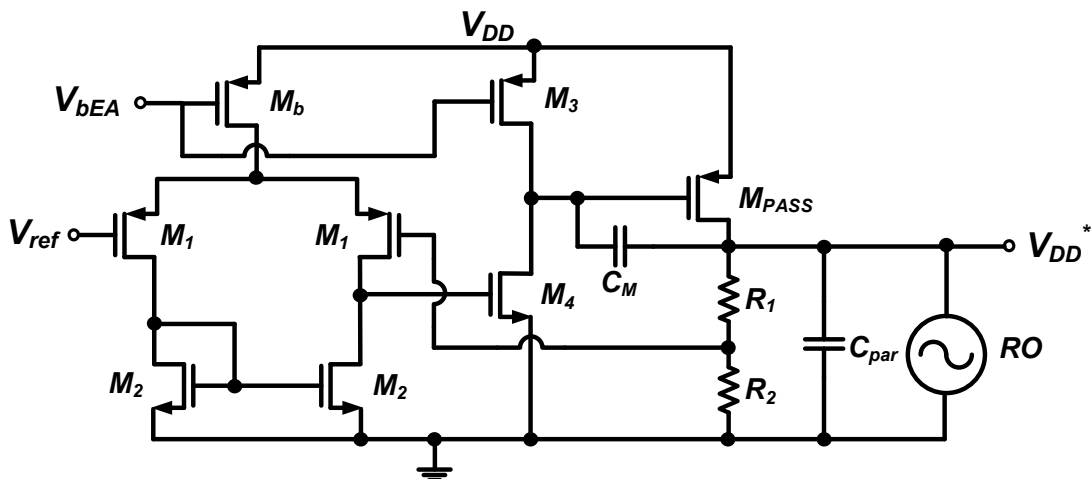
Fig. 75. Simple LDO for low frequency supply noise rejection.

In the LDO of Fig. 75, C_{par} represents the supply-line parasitic capacitance of the RO, C_M is a 5 pF miller compensation capacitor, and V_{ref} is a 1 V reference voltage that in conjunction with the R_1-R_2 voltage divider (150 kΩ R_1, and 100 kΩ R_2) sets V_{DD}* to 2.5 V from a 2.7 V V_{DD}. The LDO current consumption is only18 µA and is designed to sustain a C_{par} up to 5 pF and a maximum load current of 5 mA. The simulated LDO stability (loop magnitude and phase) and PSR curves are shown in Fig. 76 and Fig. 77, respectively. The

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LDO loop exhibits a unity-gain frequency (UGF) of 3.85 MHz and a phase margin (PM) of 53°. As shown in Fig. 77, the PSR is better than 53 dB at frequencies below 4 kHz (f_{3dB} of HPF), these PSR characteristics allow for significant attenuation of the low frequency supply noise and a seamless hand-off between the LDO to the HPF-noise rejection methods.
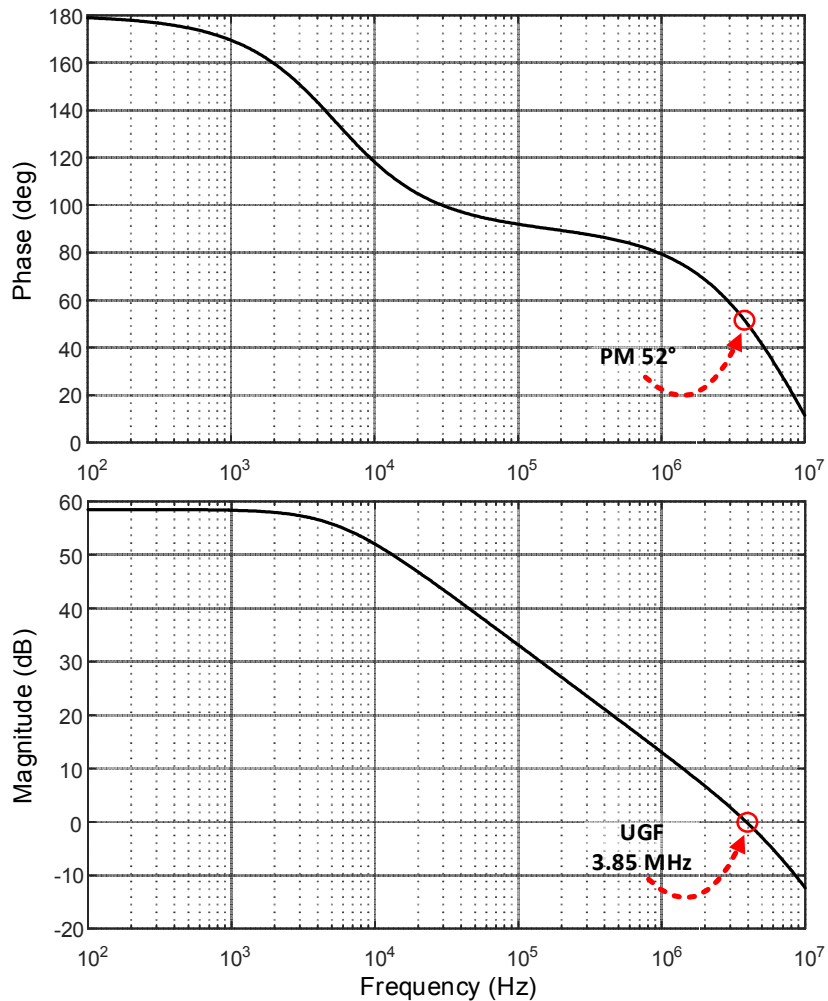
Fig. 76. Simulated LDO loop magnitude and phase.

It is important to note that the LDO PSR is better than 50 dB up to 10 kHz, this allows some room for variations in the HPF f_{3dB} and guarantees that the two noise-rejection techniques have some overlap in the frequencies at which they operate. As a result, the RO will exhibit high tolerance to supply noise against both low and high frequency aggressors.
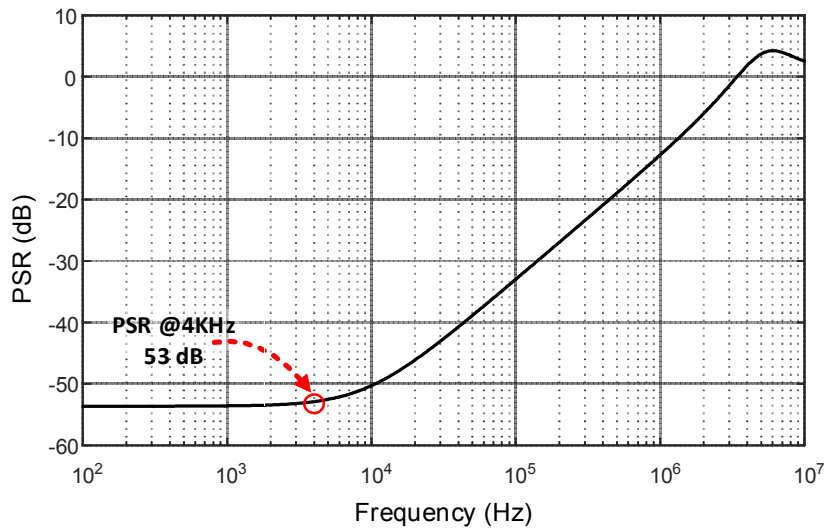
Fig. 77. LDO PSR for 5 pF C_L and 5 mA I_L.

Having avoided tuning the RO from the supply enables the use of the dual LDO+HPF supply noise rejection approach in RO-based PLLs. However, it demands the use of a secondary tuning port, which in this case is at the tail of the differential pair. The interconnections of the delay cells forming the 3-stage RO and the tuning scheme via an extended swing cascode current mirror are shown in Fig. 78. A replica bias circuit [123] is used to maintain constant output swing (V_{sw}) in the RO during the required tail current

variations to adjust the output frequency. The replica bias circuit of Fig. 79 modifies the bias voltage V_b as the tail current ($I_b + I_{tune}$ in Fig. 78) is varied to achieve the target oscillation frequency. By changing V_b, it is possible to adjust the equivalent triode resistance R_L of M_P and keep V_{sw} constant for different tail currents ($V_{sw} = (I_b + I_{tune})R_L$). If the reference voltage V_{ref_sw} in Fig. 79 is defined as (55), where V_{sw} is the target output swing, the replica bias loop forces the voltage drop across M_P to be equal to V_{sw} disregarding of the value of the tail current. As expected, M_P and R_{deg} in the replica branch are identical to their counterpart components in the delay cell. However, the current mirror is reduced to half the value of the delay cell and a buffer device (M_{buf}) is included between the OPAMP that amplifies the voltage error and the actual output V_b. This configuration avoids loading the OPAMP output and prevents an unexpected increase of the replica loop gain during transient (due to M_P going briefly into saturation), thus guaranteeing loop stability [123].
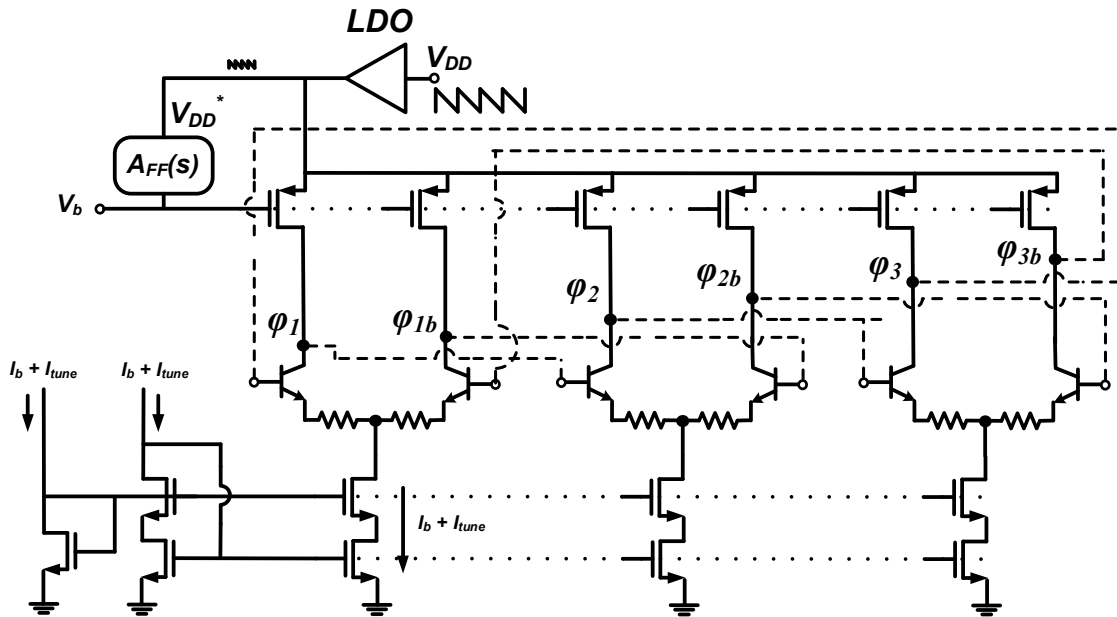
Fig. 78. Detailed schematic of the RO including the frequency tuning scheme via the tail current.
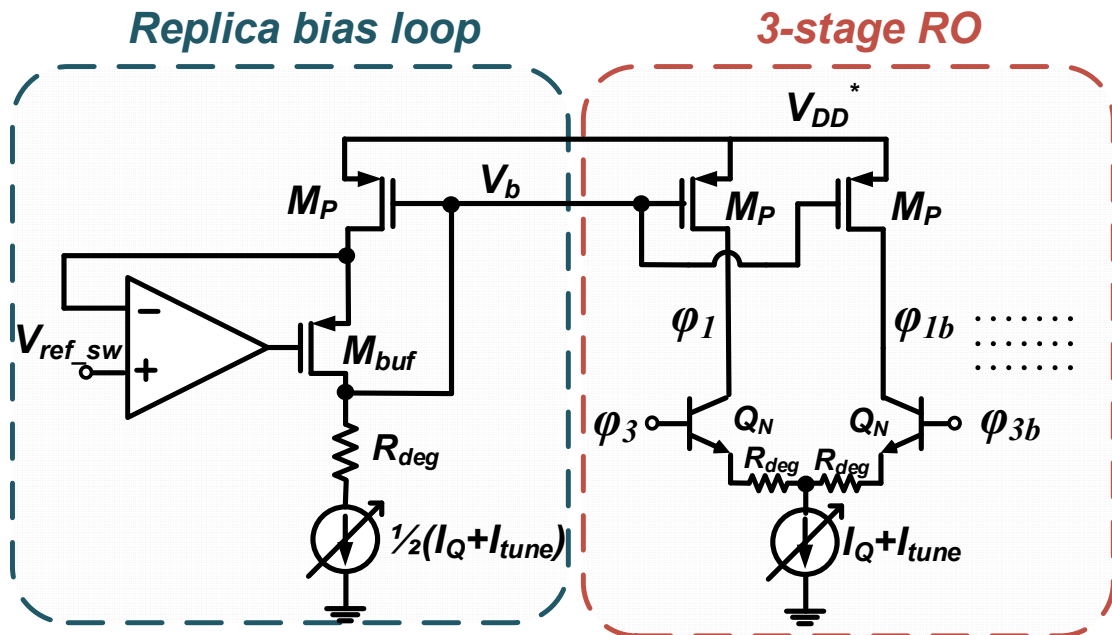
Fig. 79. Replica bias loop for constant output swing.

$$V_{ref\_sw} = V_{DD}{}^* - V_{sw}/2 \tag{55}$$

The RO output frequency stability with and without the proposed power supply noise rejection (PSNR) composite technique is shown in Fig. 80. In this test, the RO was tuned to oscillate at 2.1 GHz assuming a noise-less supply. After tuning, a 1 MHz, 200 mV$_{PP}$ sinusoidal signal was superimposed in the main supply voltage (V_{DD} node in Fig. 78). As evidenced in Fig. 80, without any control over the supply noise in the RO, its frequency largely deviates from the original target, reaching a high 2.35 GHz, and a low of 1.55 GHz, for a total deviation of 0.8 GHz. Conversely, when the HPF and LDO are enabled, the frequency deviation reduces to less than 50 MHz, or 16 times less than in the case where no PSNR technique is applied.
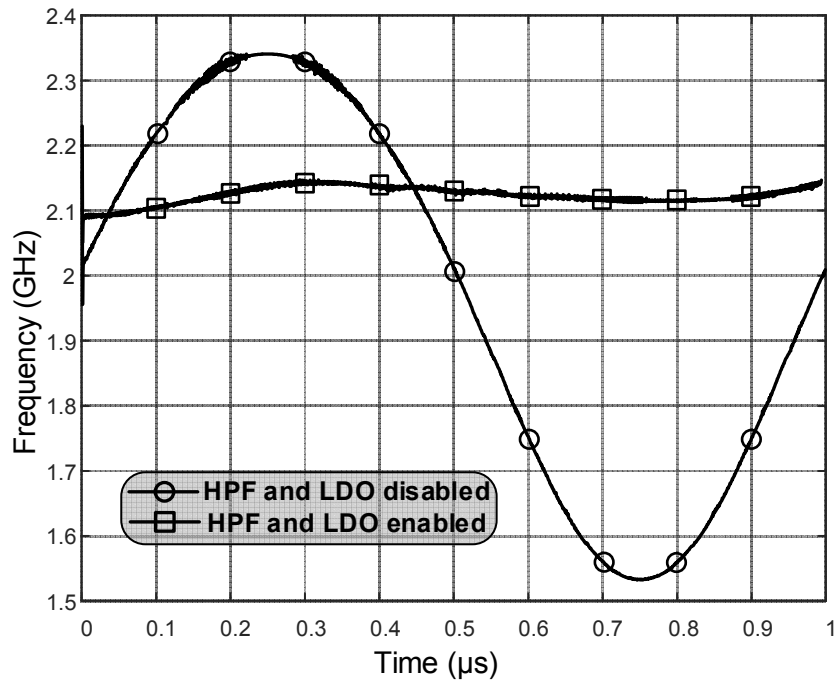
Fig. 80. RO frequency stability in the presence of a 200 mV$_{PP}$, 1 MHz aggressor in the supply.

5.4   Measurement results

The BiCMOS RO, including the PSNR composite technique, was fabricated using 0.25 μm SiGe:C (Silicon-Germanium-Carbon blend) BiCMOS technology from NXP semiconductors, and encapsulated in a QFN28 package. The die microphotograph is shown in Fig. 81, and while the total chip area is 1 mm^2, the design area is pad-limited and the actual active area is only 0.16 mm^2. The on-chip LDO uses a 2.7 V external input voltage (V_{DD}) to generate the required 2.5 V at the V_{DD}^* internal node. The setup shown in Fig. 82 is used to simulate the injection of supply noise to the LDO input through a sinusoidal signal with variable amplitude and frequency superimposed on V_{DD}.
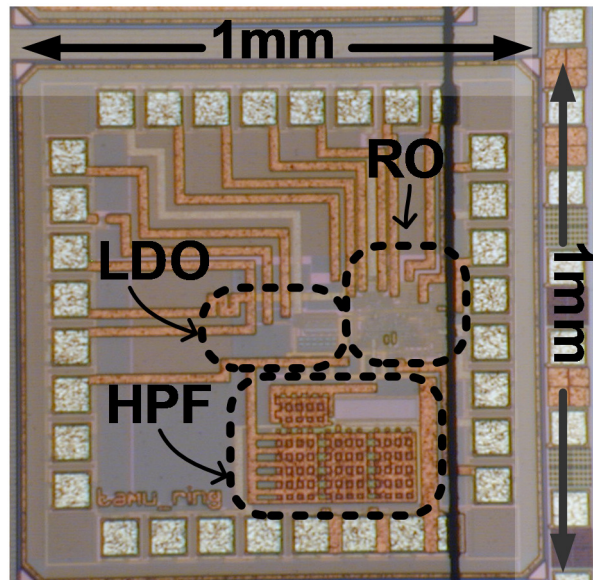
Fig. 81. Die microphotograph of the RO + PSNR solution.
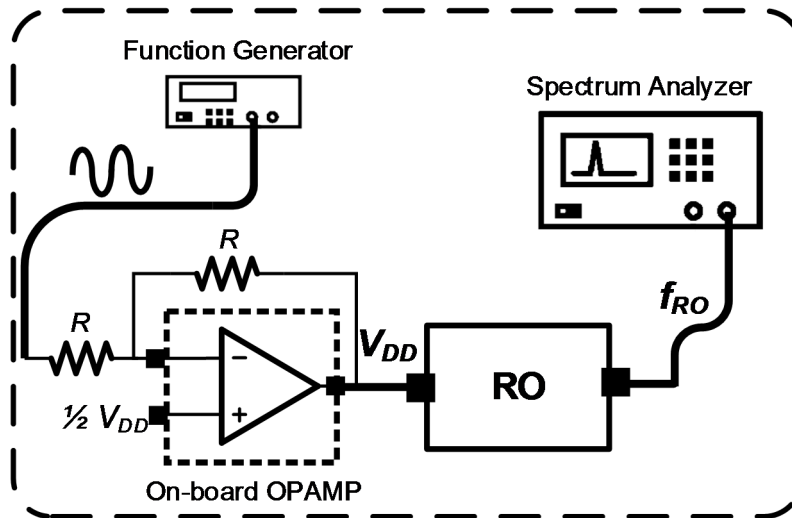
Fig. 82. Setup for RO frequency stability measurement under supply noise aggressors.

The spectrum of the RO output for f_{RO} of 317 MHz is shown in Fig. 83, in this case a 0.2 V_{PP} sinusoidal signal with 80 MHz frequency (f_{noise}) is superimposed in the supply as a noisy aggressor. The up-converted supply-noise is found to be attenuated more than 43 dB. For the same tuning current (and f_{RO}), the RO spectrum in Fig. 84 shows the noise rejection for a supply aggressor with 10 MHz f_{noise} and 0.2 V_{PP} amplitude; in this case, the up-converted noisy tone is attenuated by more than 32 dB. For a f_{RO} of 947 MHz, measurement results show (Fig. 85) that a supply aggressor with f_{noise} of 80 MHz (0.2 V_{PP}) is attenuated more than 36 dB.
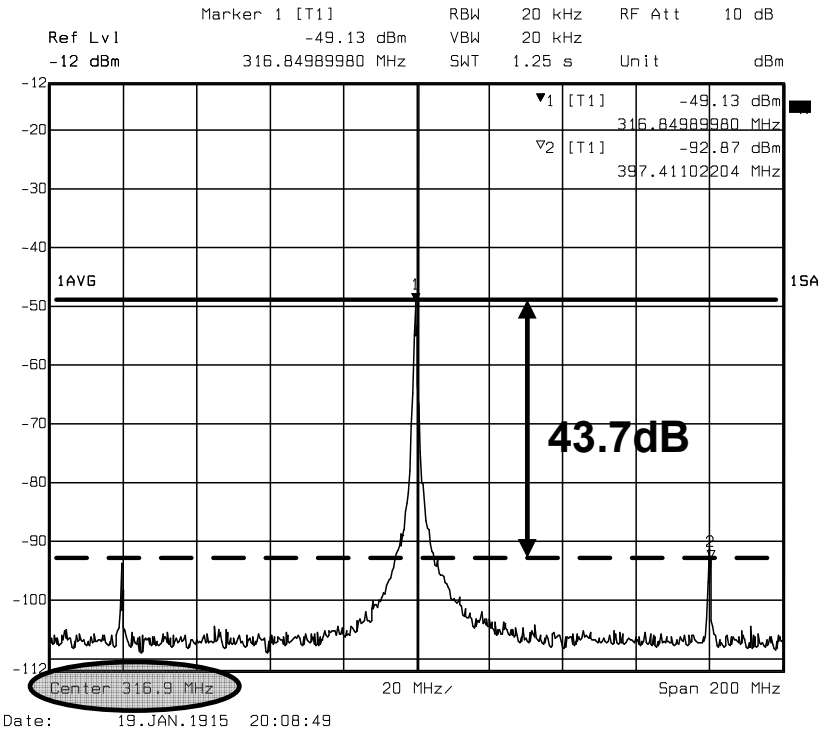
Fig. 83. RO spectrum for 317 MHz *f_RO* **under the presence of a 0.2 V_PP, 80 MHz supply aggressor.**
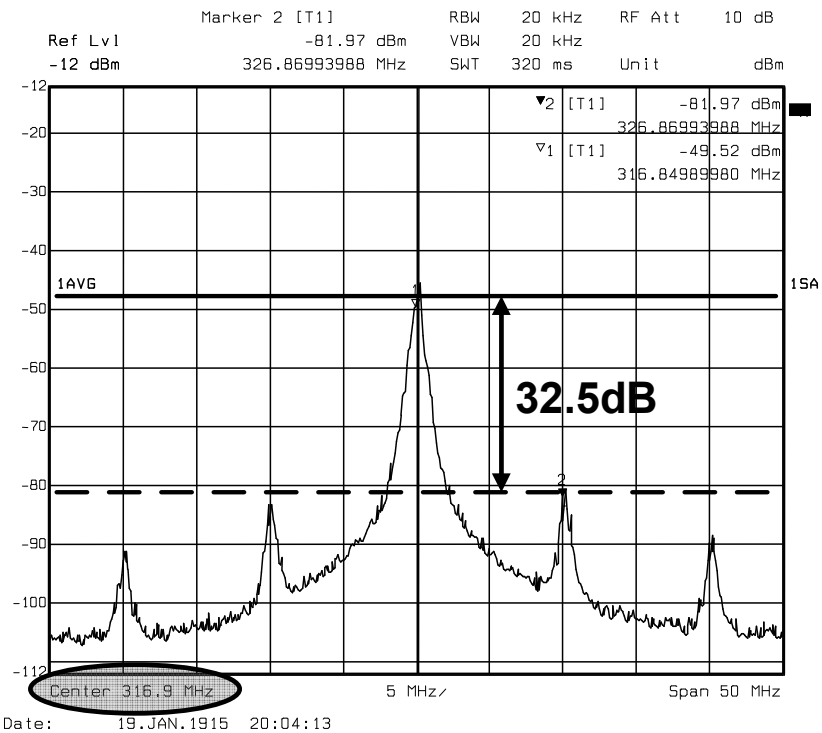
Fig. 84. RO spectrum for 317 MHz *f_RO* **under the presence of a 0.2 V_PP, 10 MHz supply aggressor.**

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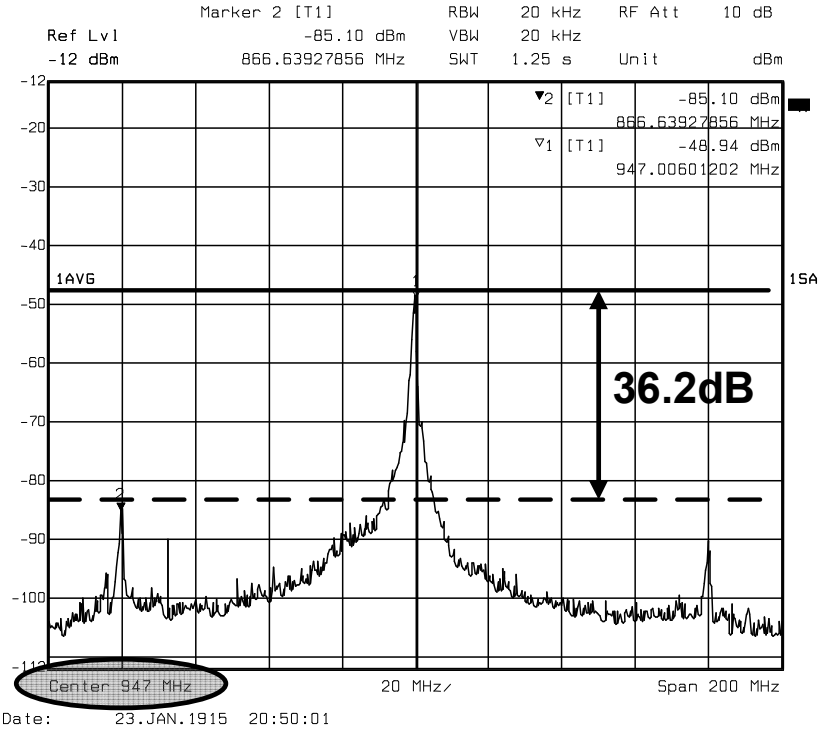
Fig. 85. RO spectrum for 947 MHz f_{RO} under the presence of a 0.2 V$_{PP}$, 80 MHz supply aggressor.

Using the PSNR metric (57) defined in [116], it is possible to quantify the output phase noise due to supply noise. In (57), T is the oscillation period (assuming a clean supply), T_j is the peak-to-peak deterministic jitter amplitude resulting from a supply noise with total amplitude equal to ΔV_{DD}. Assuming a sinusoidal signal is used to represent the supply noise, the value of Tj can be calculated using (57) [116], where M is the attenuation of the up-converted tone in dB, with respect to f_{RO}, due to f_{noise} measured at $f_{RO} \pm f_{noise}$.

$$PSNR = 20\log\frac{T_j/T}{\Delta V_{DD}} \tag{56}$$

$$T_j = \frac{2T}{\pi}10^{(M/20)} \tag{57}$$

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The calculated PSNR of the proposed RO and supply-noise rejection composite technique is -33.7 dB at 317 MHz f_{RO} and 80 MHz f_{noise}, -22.5 dB at 317 MHz f_{RO} and 10 MHz f_{noise}, and -28.2 dB at 947 MHz f_{RO} and 80 MHz f_{noise}. These results demonstrate that superior tolerance to aggressors in the RO supply can be achieved using the proposed RO structure and supply noise rejection schemes. Table 14 summarizes the performance of the RO and compares its performance against other RO with supply noise rejection schemes. While the proposed RO oscillates with a f_{RO} roughly 2/3 of that of the compared works in Table 14, the PSNR is the best despite having the RO in an open-loop, free-running fashion.

Table 14. Measurement results summary and performance comparison.

	[109]	[110]	[116]	This Work
Technology	65 nm (CMOS)	0.18 μm (CMOS)	0.18 μm (CMOS)	0.25 μm (BiCMOS)
Year	2013	2015	2009	2016
Supply (V)	1	1.8	1.8	2.5
Area (mm^2)	0.24	0.24	0.093	0.16
Structure	PLL	PLL	PLL	free-running RO
Freq. rang (GHz)	N/A – 1.6	1.4 – 2.5	0.5 – 2.5	0.3 – 0.95
PSNR (dB) @ f_o (Noise amp.–f_{noise})	+9.62 @ 1.6 GHz (47.6 mV$_{PP}$ – 10 MHz)	–0.94 @ 2.08 GHz (20 mV$_{PP}$ – 1 MHz)	–28 @ 1.5 GHz (200 mV$_{PP}$ – 8.85 MHz)	–33.7 @ 0.32 GHz (200 mV$_{PP}$ – 80 MHz) –28.2 @ 0.95 GHz (200 mV$_{PP}$ – 80 MHz)
Power (mW)	0.99 @ 1.6 GHz	59.8 @ 2 GHz	3.9 @ 1.5 GHz	< 1 @ 0.3 GHz 3 @ 0.95 GHz

5.5   Conclusions

A BiCMOS RO with a PSNR technique consisting of a simple and low-cost LDO and a supply-noise coupling HPF was presented in this chapter. The dual technique deals separately with low and high frequency noise components, the reduced LDO bandwidth (for low power consumption) attenuates noise components below 4 kHz by more than 53 dB and the HPF couples the high frequency noise components (> 4 kHz) to the gate of key transistors in the delay cell composing the RO. As a results, the net gate-to-source voltage remains constant even in the presence of supply noise and the effective propagation delay of the cell remains unchanged, allowing for a stable RO oscillation frequency, low up-converted noise tones and high PSNR figures. The fabricated prototype in SiGe:C 0.25 μm technology demonstrated a PSNR better than -28.2 dB for sinusoidal supply noise components of 0.2 V_{PP} and 80 MHz. While an underestimation of routing parasitics degraded the expected frequency that the RO could reach in experimental results, the obtained PSNR is still comparable to state-of-the art solutions and provides and alternative for frequency synthesizers that intend to use ring-oscillators at their core to increase tuning range and integrability. Similarly, although this worked presented the composite PSNR technique for a BiCMOS delay cell, it is certainly possible to use the proposed technique in purely CMOS oscillators.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1   Summary of research

This dissertation discussed and presented the design and implementation of two key building blocks for IoT nodes: power management unit and wireless transmitter. The solutions proposed to the current needs for low power and high noise suppression in power management units and for ultra-low power transmitter architectures represent one more step toward the optimum IoT node where efficient PMU circuits enable an energy-harvested-power SoC to operate in a self-contained and battery-less fashion, and where new transmitter architectures exploit current reuse concepts that enable an increase in its energy efficiency and net power consumption, which in turn, opens the door to an IoT completely power by harvested energy from one or multiple sources.

The following list summarizes the contributions of this dissertation:

- A compact and flexible model for general LDO structures exclusively based on SPICE primitives for easy integration and simulation speed-up in top-level testbenches for large SoC including multiple LDOs. The model uses real data obtained from schematic or post-layout instances of the LDO to map the characteristics of the pass transistors into fitted polynomials that describe the LDO across the entire load current range.

- A high-efficiency PMU for energy-harvesters based on thermoelectric generators including a boost converter with maximum power point tracking and improved stability, and a first-in-its-class capacitor-less LDO with programmable supply rejection for localized improvement.

- A high efficiency 900 MHz ISM transmitter for IoT nodes with data rate requirements of up to 3 Mbps. The joint design and optimization of an ultra-low power oscillator with an edge-combiner power amplifier in a transmitter using a wideband frequency-shift keying modulation enabled an overall reduction in the transmitter power consumption.

- A novel, ultra-low power delay-cell that exploits current reuse termed as "vertical delay cell" was introduced and was applied for the implementation of an ultra-low power ring-oscillator.

- A BiCMOS ring-oscillator with a novel technique for increased supply noise tolerance based on passive high-pass filters and low-cost voltage regulators.

6.2   Areas for future work

It is possible to identify several lines of work worth to explore that can build on top of the important steps taken in the research presented in this dissertation. These areas include, but are not limited to:

- Automation of the LDO model generation approach suggested in chapter II via an independent SPICE netlist creator and reader.

- Integration of the Sense-and-Control loop in the proposed PMU of chapter III via a finite state machine.

- Design and system integration of a built-in, spectrally-based supply rejection measurement system for fine tuning of the look-up-table required in the Sense-and-Control algorithm of the PMU.

- Migration of the proposed PMU to a smaller technology to explore the use of higher switching frequencies in the PMU front-end and the potential removal of the capacitor at the output of the boost converter.

- Integration of the digitally-assisted frequency correction loop in the ultra-low power Tx proposed in chapter IV.

- Exploration of on-chip transformer-based output matching network for the edge-combining power amplifier in the Tx.

- Explore the use of the BiCMOS oscillator proposed in chapter V in the context of a closed-loop, frequency-synthesizer for improved supply noise filtering and potential removal of local LDO via a small trade-off with the synthesizer loop bandwidth.

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