BLOCKER TOLERANT RADIO ARCHITECTURES

A Dissertation

by

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ABSTRACT

Future radio platforms have to be inexpensive and deal with a variety of co-existence issues. The technology trend during the last few years is towards system-on-chip (SoC) that is able to process multiple standards re-using most of the digital resources. A major bottle-neck to this approach is the co-existence of these standards operating at different frequency bands that are hitting the receiver front-end. So the current research is focused on the power, area and performance optimization of various circuit building blocks of a radio for current and incoming standards.

Firstly, a linearization technique for low noise amplifiers (LNAs) called, Robust Derivative Superposition (RDS) method is proposed. RDS technique is insensitive to Process Voltage and Temperature (P.V.T.) variations and is validated with two low noise transconductance amplifier (LNTA) designs in 0.18μm CMOS technology. Measurement results from 5 dies of a resistive terminated LNTA shows that the proposed method improves IM3 over 20dB for input power up to -18dBm, and improves IIP_3 by 10dB. A 2V inductor-less broadband 0.3 to 2.8GHz balun-LNTA employing the proposed RDS linearization technique was designed and measured. It achieves noise figure of 6.5dB, IIP_3 of 16.8dBm, and P_{1dB} of 0.5dBm having a power consumption of 14.2mW. The balun LNTA occupies an active area of 0.06mm^2.

Secondly, the design of two high linearity, inductor-less, broadband LNTAs employing noise and distortion cancellation techniques is presented. Main design issues and the performance trade-offs of the circuits are discussed. In the fully differential architecture, the first LNTA covers 0.1-2GHz bandwidth and achieves a minimum noise figure (NFmin) of 3dB, IIP_3 of 10dBm and a P_{1dB} of 0dBm while dissipating 30.2mW. The 2nd low power bulk driven LNTA with 16mW power consumption

achieves NFmin of 3.4dB, IIP_3 of 11dBm and 0.1-3GHz bandwidth. Each LNTA occupy an active area of $0.06mm^2$ in 45nm CMOS.

Thirdly, a continuous-time low-pass $\Delta\Sigma$ADC equipped with design techniques to provide robustness against loop saturation due to blockers is presented. Loop overload detection and correction is employed to improve the ADC's tolerance to blockers; a fast overload detector activates the input attenuator, maintaining the ADC in linear operation. To further improve ADC's blocker tolerance, a minimally-invasive integrated low-pass filter that reduces the most critical adjacent/alternate channel blockers is implemented. An ADC prototype is implemented in a 90nm CMOS technology and experimentally it achieves 69dB dynamic range over a 20MHz bandwidth with a sampling frequency of 500MHz and 17.1mW of power consumption. The alternate channel blocker tolerance at the most critical frequency is as high as -5.5dBFS while the conventional feed-forward modulator becomes unstable at -23.5dBFS of blocker power. The proposed blocker rejection techniques are minimally-invasive and take less than 0.3μsec to settle after a strong agile blocker appears.

Finally, a new radio partitioning methodology that gives robust analog and mixed signal radio development in scaled technology for SoC integration, and the co-design of RF FEM-antenna system is presented. Based on the proposed methodology, a CMOS RF front-end module (FEM) with power amplifier (PA), LNA and transmit/receive switch, co-designed with antenna is implemented. The RF FEM circuit is implemented in a 32nm CMOS technology. Post extracted simulations show a noise figure $<$ 2.5dB, S_{21} of 14dB, IIP_3 of 7dBm and P_{1dB} of -8dBm for the receiver. Total power consumption of the receiver is 11.8mW from a 1V supply. On the transmitter side, PA achieves peak RF output power of 22.34dBm with peak power added efficiency (PAE) of 65% and PAE of 33% with linearization at -6dB power back off. Simulations show an efficiency of 80% for the miniaturized dipole antenna.

DEDICATION

To my parents and family

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NOMENCLATURE

P_{1dB}	1dB compression point
IIP_3	Input referred 3^{rd}-order Inter-modulated distortion
C.T. $\Delta\Sigma$ Modulator	Continuous Time Delta Sigma Modulator

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1. INTRODUCTION

1.1. Motivation

Future radio platforms should support multiple-input-multiple-output (MIMO) operation. These radios have to be inexpensive and deal with a variety of co-existence issues as shown in the Fig. 1.1. The figure shows the crowded spectrum of todays wireless communication. The technology trend during the last few years is towards system on chip that is able to process multiple standards re-using most of the digital and digitization resources. A major bottle-neck to this approach is the co-existence of this standards operating at different frequency bands that are hitting the antenna and receiver front-end. So the current research is focused on the optimization of various building blocks of the wireless transceivers for current and incoming standards.

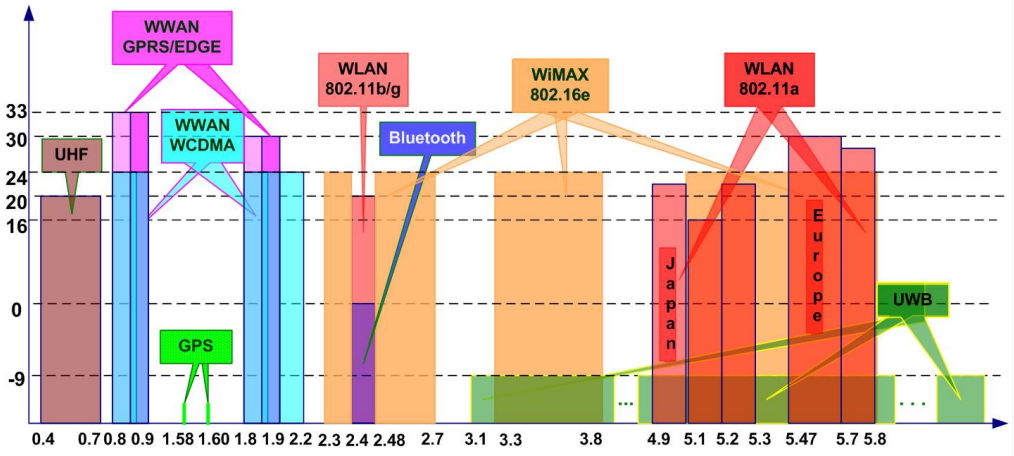


Figure 1.1: Crowded radio spectrum showing co-existence with multiple standards

Fig. 1.2 is the SAW-less DC conversion receivers. It can be noticed that the

dedicated expensive, off chip SAW (surface acoustic wave) filter is removed. The co-existence issue becomes more severe in broadband multi-standard receivers and is a bottle neck. Since the amount of out-of-band (OOB) power is excessive compared with the desired channel as can be seen in Fig. 1.1, the linearity of both front-end and digitizer becomes the main limitation for achieving the required performance. This issue is even more relevant for cost effective SAW-less architectures, where no or very weak RF filtering is present at the low noise amplifier (LNA) input. Non-linearities generate cross products and some of them are folded-back into the main channel increasing dramatically the in-band noise level.

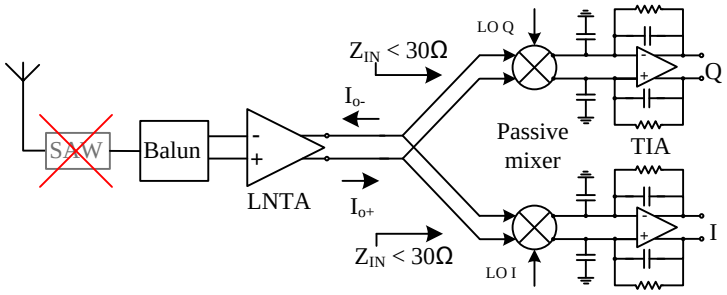


Figure 1.2: SAW less direct conversion receiver

Software defined radios (SDRs) achieve the required performance to replace the dedicated radios but also reconfigure to other standards and hence pose a benefit. Fixed, high-Q SAW filters are usually employed before the dedicated radio front ends to remove the large out of band interference. These SAW filters are expensive, not on CMOS process and not suited for reconfigurable radio concept. Removing this dedicated filter decreases the cost of the radio and makes the SDR possible but requires the radio receiver to accommodate much higher linearity than a standard

dedicated radio. So this research focuses on the advancement of SDRs and implementing the radios on the inexpensive CMOS process by developing high linearity radio front ends. However, the RF front-end must co-exist with high power blockers due to the lack of RF filtering, hence demanding more linear LNAs and Mixers. In this way, this research advances the science and/or technology.

CMOS technology and the receiver architectures will enable the cost-effective implementation of the systems. SAW-less receiver architectures are cost-effective but demands highly linear radio front ends due to the broadband nature of the entire communication system. The purpose of part of this research is to develop Inductor-less highly linear Low noise amplifiers for radio front-ends. This goal is achieved with minimum impact in both noise and power consumption. The proposed solutions from the research are also robust to the process voltage and temperature (P.V.T.) variations.

1.2. Goals and Achievements of the Research

Some part of the research work is devoted to the development of low cost, highly linear, inductor-less RF front-ends and ADCs. The research work on RF front-ends resulted in the development of multiple linearization techniques for low noise amplifiers. One proposed linearization technique is based on derivative superposition called robust derivative superposition (RDS) method is insensitive to P.V.T variations. The technique enhanced the linearity (IIP_3) of resistive terminated low noise transconductance amplifier (LNTA) by 10dB. Highly linear LNTAs are very critical for receivers especially for SAW less radio front ends. SAW less radio front end is a cost effective and a possible solution for software defined radio (SDR). SDRs replace the multiple dedicated radios in a receiver with a single programmable radio, reducing, area, cost and power consumption.

The RDS linearization technique is composed of 2 transistors operating in triode and sub-threshold region improving the linearity of the main transistor operating in strong inversion. The power penalty of this technique is less than 8%. These research findings are reported in [1, 2]. With this experience two more linearized low noise transconductance amplifiers (LNTAs) architectures focusing on large signal linearity are developed and implemented on TSMC 45nm. Large signal linearity is usually characterized by 1dB compression point (P_{1dB}). Measurement results from Low noise transconductance amplifiers shows large signal linearity, $P_{1dB} >$ 0dBm and small signal linearity $IIP_3 >$ 10dBm. The inter-modulation distortion components are under -70dB for input power as large as -15dBm, which outperform the linearity of the conventional LNTA by more than 10dB. The findings from this work are reported in [3]. Experimental results from these different architectures verified the theory; outperforming the linearity of the existing architectures. Large signal linearity is very critical for the cost effective SDRs with minimum or no RF filtering. The significance of these high linearity numbers is that the LNTAs can accommodate high out of band interferences without being desensitized or blocked. Minimum Noise figure measured is 3dB. Less Noise figure is required for good sensitivity in the receiver. The research on high linearity radio front ends is quite relevant to the current technology trend and strongly contributes to the state of the art.

As part of developing blocker tolerant radio architectures, part of this research work is focused on developing blocker tolerant ADC architectures for wireless applications. A thorough research is done on the sensitivity of CT$\Delta\Sigma$ ADC to blockers. Strong OOB blockers degrade the DR of the ADC and can potentially destabilize the system. The effect of blocker and jitter interaction on the in-band noise is also studied. A blocker tolerant CT$\Delta\Sigma$ ADC for broadband receivers is proposed. With the integrated blocker detector/attenuator, the input signal is reduced to prevent

the system from getting saturated in presence of blockers.

The proposed solution is effective for rapidly varying blockers that may saturate the loop when operating with its full dynamic range. Although the input signal is attenuated in the proposed blocker detection scheme, the system is less prone to saturation with only a moderate SNR degradation in the presence of blockers. The proposed system with the blocker detector settles in less than 0.3μs. This fast detection and self-correction is highly important in radio applications to maintain the communication active. To further attenuate the blockers, an active minimally-invasive integrated LPF filter that attenuates the most critical adjacent/alternate blockers is employed. Power overhead due to the proposed blocker tolerant techniques is only 6% of the total power budget. The design of building blocks and/or the entire system could be easily adopted to new applications and/or different semiconductor technologies. With the proposed solutions/ideas a blocker tolerant radio for wireless applications can be realized.

The last part of the research is focused on developing CMOS front-end-module (FEM). CMOS FEM is based on a new radio partitioning methodology. RF circuitry with inductors consumes a large die area making a complete radio in scaled technology more expensive than in older technology. RF circuitry is usually lower performing in SoC technology because of breakdown voltage and sub-optimal metal layers chosen for digital density. By properly partitioning the radio and developing a design methodology for the SoC analog/mixed-signal radio, the die size/cost is greatly reduced and this function can be developed concurrently with digital collateral at the beginning of a technology development cycle. This chapter presents a novel CMOS RF front end module (FEM) with Power amplifier (PA), Low noise amplifier (LNA) and Transmit/Receive (T/R) switch co-designed with Antenna. The co-design gives the advantage and improves the overall performance. This CMOS FEM is separated

from the system on chip (SoC) transceiver. This separated FEM design methodology gives robust analog and mixed signal radio development in scaled technology for SoC integration, and the co-design of the RF FEM-antenna system.

1.3. Organization

The design and implementation of the novel circuit blocks mentioned in 1.2 are explained in a detailed manner in the following chapters. A highly robust linearization technique for broadband LNTAs is presented in Chapter 2. The proposed Robust Derivative Superposition (RDS) method for linearizing LNTAs is employed on a conventional resistive terminated LNTA and a noise/distortion canceling balun LNTA. Noise, linearity and power trade-offs are drawn are analyzed in detail. Transistor level implementation of the LNTAs based on the proposed linearization techniques is described in detail. Experimental results from the prototype built in 0.18μm CMOS technology are discussed and comparison with state of the LNTAs is presented.

Chapter 3 describes a high linearity low noise amplifiers with noise and distortion cancellation. Blocker tolerant radio receivers are discussed and the proposed highly linear LNTA complements those receivers. Performance and power trade-offs are discussed with detailed analysis. Large signal linearity is identified to be crucial linearity parameter for the wide-band receivers. Experimental results from the prototype fabricated in 45nm technology are discussed. The chapter concludes with a performance comparison with state-of-the-art LNTAs.

A blocker tolerant continuous time delta-sigma analog to digital converter (ADC) is described in Chapter 4. The sensitivity of CT$\Delta\Sigma$ ADC to blockers is briefly discussed. A blocker tolerant ADC architecture with two solutions is presented. The realization of the proposed ADC architecture using various circuit techniques is described in detail. A minimally invasive integrated blocker filter is proposed to

improve the blocker immunity. The noise, power and area trade-offs of this block are briefly discussed. Design of a 20MHz signal bandwidth 12-bit ADC based on the proposed architecture is presented. The simulation and experimental results from the prototype built using a 90nm digital CMOS technology are also discussed.

Chapter 5 discusses the design highlights and novel ideas of the CMOS FEM. The integrated circuit of this FEM is fabricated on a 32nm technology. The new radio partition methodology and the resulting benefits are briefly discussed. Spectral power combination through dipole antenna for a class-D PA is discussed. A new highly efficient passive T/R switch is proposed in this chapter. Conclusions are drawn in chapter 6 and a possible area for future work related to the presented architectures are identified.

2. LINEARIZING LOW NOISE AMPLIFIERS BY ROBUST DERIVATIVE SUPERPOSITION*

2.1. Introduction

Wide-band multi-standard front-end is attractive for its re-usability and low cost. The design of multi-standard front-end requires low noise and high linearity for wide frequency range. Parallel front-end structure with a number of conventional narrow-band front-ends has disadvantage of huge die area and lack of reconfigurability. Recently, wide-band multi-standard low noise amplifier (LNA) has been implemented using deep sub-micron CMOS technology [4]. High f_t transistor enables it possible to build such a wide-band front-end without an inductor. Although the noise and bandwidth of deep sub-micron CMOS improves as the minimum channel length decreases, linearity has been gradually degraded with short-channel effect and low power supply.

2.2. Broadband LNAs

Wide-band multi-standard LNA can be implemented using deep sub-micron CMOS technologies; the most popular topologies are based on common-source [5], common-gate [6] and resistive shunt and series feedback [4] configurations as shown in Fig. 2.1. The primary concern of wide-band multi-standard front-end is having high linearity to relax the performance requirement for following building block. Since it is not allowed to use filters in front of LNA and there might exist huge blockers which can create inter-modulation products in the frequency region of desired signal band, LNA needs to be highly linear to minimize inter-modulation distortion. If LNA were

*Part of this chapter is reprinted with permission from "Inductorless wideband CMOS LNAs with nonlinearity cancellation," by H. M. Geddada *et al.*, *IEEE Midwest Symposium on circuits and systems*, pp. 1-4, Copyright 2011 by IEEE.

not linear enough in the environment that huge blockers exist, SNDR (signal to noise and distortion) at the output of LNA is dominated by distortions than noise. In this circumstance, lowering noise figure does not help to improve SNDR. Although it is generally told that linearity of last stage of RF front-end is the most dominant for linearity performance of the system, the linearity of LNA in the wide-band multi-standard system is extremely important because of its wide-band characteristic.

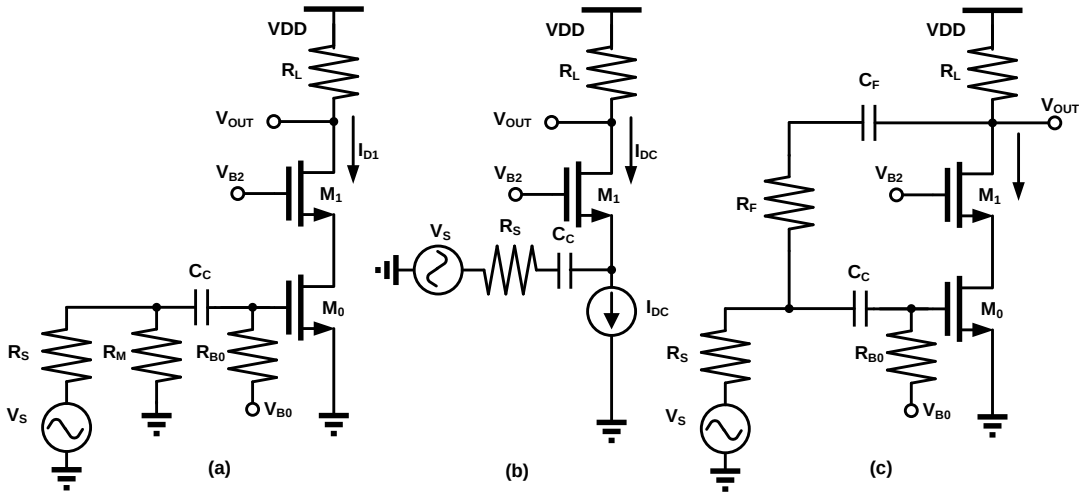


Figure 2.1: Broadband LNAs (a)resistive termination LNA, (b)common gate LNA, (c)resistive shunt-feedback LNA

Using inductors in wide-band application is general for better frequency response. Unfortunately, however, inductors might potentially cause a few problems in practice. Not only it requires a huge area but also it may cause coupling problem. Therefore, reducing the number of inductors in the system is required. Exploiting high f_T transistors in deep sub-micron CMOS technology, RF front-end could be implemented

with a small number of inductors or even without inductors. The theory and design methodology of the mentioned broadband LNAs can be found in [7] and/or in its references. In the next few sections most popular broadband LNAs like Resistive feedback LNA and balun LNA will discussed briefly.

2.2.1. Resistive feedback LNA

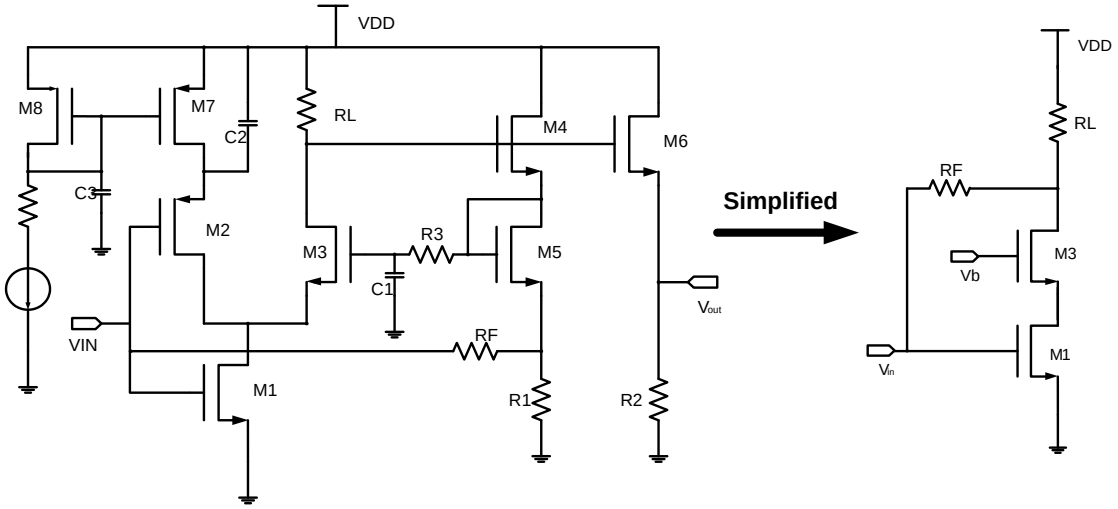


Figure 2.2: Resistive shunt-feedback LNA [8]

One very popular wide-band inductor-less CMOS LNA is resistive feedback LNA. Authors in [8] reported the resistive feedback LNA and can be seen in the Fig. 2.2. The fundamental concept of the LNA is resistive feedback for input impedance matching over wide frequency range. In fact, this structure is another version of simple cascode resistive feedback structure consisting of M_1, M_3, R_L and R_F. M_1 generates signal current if V_{in} is applied at the gate. M_3 acts as cascode transistor.

The input impedance of this structure is simply determined as

$$R_{in} = \frac{R_F}{1 + g_{m1}R_L(\frac{R_F}{R_F + R_L})} \tag{2.1}$$

while noise figure is determined as

$$F \approx 1 + \frac{R_S}{R_F} + \gamma\frac{1}{g_{m1}R_S} \tag{2.2}$$

To meet the input impedance matching and to have low noise characteristic, the transconductance of M_1, g_{m1}, should be maximized. Sticking with simple cascode structure is not proper for increasing g_{m1} because of voltage headroom problem. DC current injection using PMOS devices, M_2 and M_7 is required to increase the current of M_1 and transconductance g_{m1} without voltage headroom restriction. Furthermore, current reusing by using transconductance of M_2 helps to boost the overall transconductance. Therefore, both low noise below 3dB and wide-band input impedance matching could be obtained.

Enhancing the transconductance G_{meff} enabled it possible to have low noise and input impedance matching over wide frequency range. With the help of enhanced transconductance, higher gain could be also obtained without degrading noise and input impedance matching performance. Moreover, implementing resistive feedback for input matching led not to use inductors at the input stage. Exploiting high f_T transistors in deep sub-micron CMOS technology helped to avoid using inductors for frequency peaking bandwidth extension. Resistive feedback also helps the linearity of the LNA better. DC feedback scheme automatically set the DC bias voltage for M_1, M_2 , and M_3 which are critical transistors for the LNA. DC feedback stabilizes the bias condition against process and temperature variation. The only external

bias is the constant current biasing created by M_8 in the Fig. 2.2. It means that all transistors bias voltage will be properly adjusted for M_8 to flow the fixed current.

Linearity seems not critically considered in this design. Considering 2^{nd} order derivative of g_m, bias conditions for M_1 and M_2 need to be properly set for high linearity. Using M_1 and M_2 as complementary input stage could accumulate 2^{nd} order derivative of g_m to make the situation even worse. Although resistive feedback alleviates the non-linearity of the LNA, this effect is minor as far as R_F of the LNA is kept large enough for low noise performance. Other techniques have also been reported [9–11]. Most of the linearization schemes reported are very sensitive to P.V.T variations.

2.2.2. Noise and distortion canceling LNA

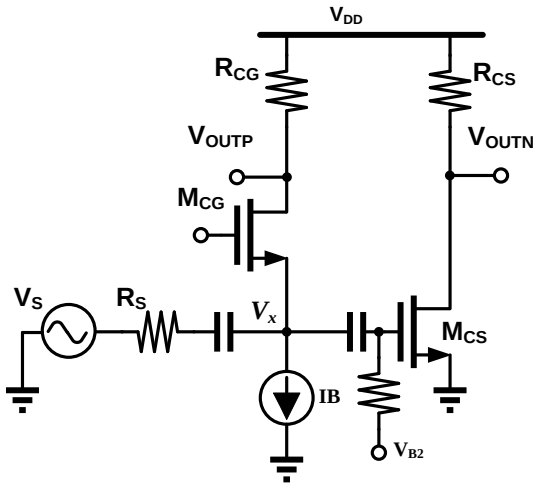


Figure 2.3: Typical broadband balun-LNA [12]

Another popular wide-band inductor-less CMOS LNA is presented in the works [12, 13] with single-ended inputs are primarily used in RF applications because the signals produced by antennas are single-ended in nature. However, differential operation has significant advantages like immunity from common-mode noise and elimination of second order distortion. Hence, baluns are needed to perform this conversion at some point in the signal chain. Active baluns are usually narrow-band in nature and we would have to use many of them in parallel to realize a wide-band LNA. On the other have, passive baluns have high loss and hence degrade NF significantly. Hence, a wide-band LNA that performs the operation of a balun as well is a useful component. The topology used to realize the wide-band balun-LNA is shown in Fig. 2.3 [13]. For maximum power transfer, the power match is realized by the implementing the g_m of the of the CG transistor to be 20mS. This ensures perfect impedance matching for $R_S = 50\Omega$. Some other important properties of the balun-LNA are described below.

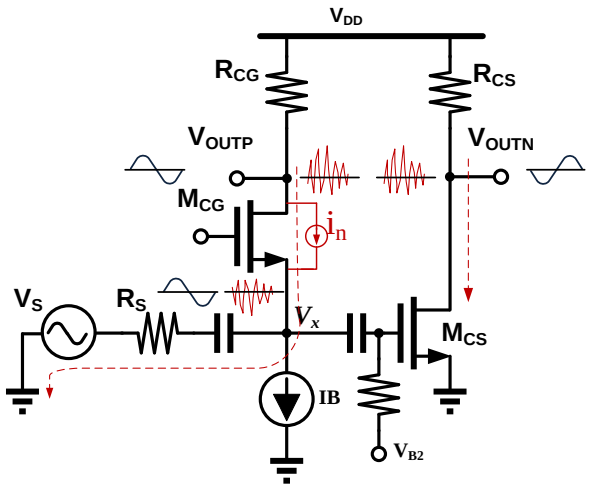


Figure 2.4: Noise/distortion cancellation in CG and CS configuration balun-LNA [12]

In the illustration shown in Fig. 2.4, i_n represents the thermal noise due to the channel of the CG-stage. As seen in the figure, this noise current flows through the source resistance and generates a noise voltage that is out of phase with the noise voltage at the CG-output. This noise voltage now acts as an input to the CS stage. Hence, while the signal components arrive out of phase at the output, the thermal noise of the CG stage appears as a common-mode component and is hence canceled. Thus the noise of the CG stage is canceled and the balun-LNA is limited by the noise contribution due to the CS stage. Also, if we consider any distortion components introduced by the CG stage as an additional current source between the source and the drain, by the same mechanism described for noise, the distortion of the CG-stage too is canceled at the output. Hence, this LNA topology while providing balun functionality conveniently provides noise and distortion cancellation too. From the discussion above, we note that the noise and distortion of the above mentioned LNA topology is limited by the CS stage.

2.3. Distortion in LNAs

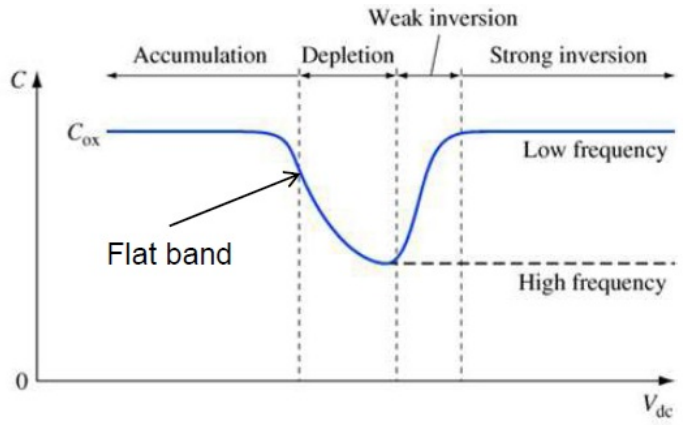


Figure 2.5: DC characteristics of the input parasitic capacitor C_{gs} in a transistor

The distortion in a transistor can arise from (1) the nonlinear parasitic capacitors (gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, the drain-bulk capacitance C_{db}), (2) nonlinear transconductance (g_m) and nonlinear output conductance (g_{ds}). The MOSFET capacitances are less nonlinear than g_m/g_{ds} for frequencies less than $f_T/10$ [14] and signal swings are relatively small.

C_{gs} is the parasitic capacitor between gate and source terminals of a transistor. Depending on the input signal swing, the value of C_{gs} changes. DC characteristics of the C_{gs} is shown in Fig. 2.5 .It can be noticed from the figure that C_{gs} is very non-linear in the transition from weak inversion to strong inversion. When large signals are given as input to the transistor, this transition can potentially happen. C_{gd} influences the linearity indirectly through feedback [15]. Due to this nonlinearity, distortion components appear at the output along with the fundamental.

Main source of distortion comes from the non-linear transconductance (g_m). Assuming soft nonlinearity (signal is moderately small) and neglecting nonlinearities from parasitic capacitors and g_{ds}, the drain current of a MOS transistor can be expressed as

$$i_{ds} = g_1 V_{gs} + g_2 V_{gs}^2 + g_3 V_{gs}^3 + \dots \tag{2.3}$$

where g_i is th t^{th} -order distortion coefficient of a transistor obtained by taking derivative of the drain-source DC current $\mathrm{I_{DS}}$ with respect to the gate-to-source voltage $\mathrm{V_{GS}}$ at the DC bias point

$$g_1 = \left.\frac{\partial \mathrm{I_{DS}}}{\partial \mathrm{V_{GS}}}\right|_Q, \qquad g_2 = \left.\frac{\partial^2 \mathrm{I_{DS}}}{2!\partial \mathrm{V^2_{GS}}}\right|_Q, \qquad g_3 = \left.\frac{\partial^3 \mathrm{I_{DS}}}{3!\partial \mathrm{V^3_{GS}}}\right|_Q \tag{2.4}$$

To characterize the g_m nonlinearity for a single transistor, we fix its $\mathrm{V_{DS}}$ and sweep

the V_{GS}, by taking the first three derivatives of the drain-source DC current I_{DS} with respect to the V_{GS} at every DC bias point, we can obtain Fig. 2.6. Simulation setup is also given in the same figure.

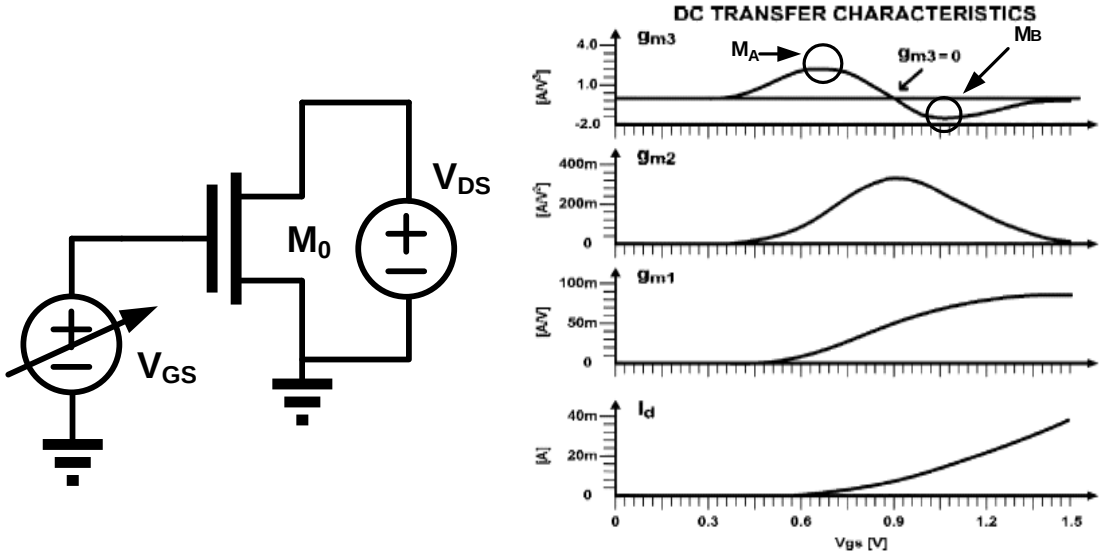


Figure 2.6: DC transfer characteristics (drain current and its derivatives with respect to the gate voltage) of a transistor at fixed V_{DS}

Distortion of MOS transistors is mainly caused by the non-linear transconductance (g_m) and output conductance (g_{ds}). In the literature many linearization techniques mainly focus on linearizing g_m, assuming (1) drain current (i_{ds}) is controlled only by the gate-source voltage (V_{gs}), and (2) (g_{ds}) nonlinearity is negligible. These assumptions are valid for small load resistance, small voltage gain, small input signal, and a drain-source voltage (V_{DS}) sufficiently large that a small-signal variation of V_{DS} does not appreciably perturb the bias point. However as the technology scales down, the g_{ds} nonlinearity becomes more prominent. Current i_{ds} is controlled not

only by V_{gs} but also the V_{ds}, which can be approximated by the two dimensional Taylor series [12, 14]

$$\begin{aligned} i_{ds} = {} & g_1 V_{gs} + g_2 V_{gs}^2 + g_3 V_{gs}^3 + g_{ds1} V_{ds} + g_{ds2} V_{ds}^2 + g_{ds3} V_{ds}^3 \\ & + C(1,1) V_{gs} V_{ds} + C(2,1) V_{gs}^2 V_{ds} + C(1,2) V_{gs} V_{ds}^2 \end{aligned} \tag{2.5}$$

where g_i is the i$^{\text{th}}$ order transconductance as defined in Eq. 2.4; g_{dsi} represents the nonlinear output conductance effect which is proportional to the $\mathrm{I_{DS}}$ derivatives with respect to $\mathrm{V_{DS}}$; $C(m,n)$ is the cross modulation term describing the dependence of g_i on $\mathrm{V_{DS}}$ or g_{dsi} on $\mathrm{V_{GS}}$ as given in Eq. 2.8

$$g_{dsi} = \left. \frac{1}{i!} \frac{\partial^i \mathrm{I_{DS}}}{\partial \mathrm{V^i_{DS}}} \right|_Q \tag{2.6}$$

$$C(m.n) = \left. \frac{1}{m!n!} \frac{\partial^{(m+n)} \mathrm{I_{DS}}}{\partial \mathrm{V^m_{GS}} \partial^m \mathrm{V^n_{DS}}} \right|_Q \tag{2.7}$$

2.4. Existing Solutions

Many Linearization techniques for broadband amplifiers have been proposed over the last few years. Few of them are discussed in this section.

2.4.1. Optimum gate biasing

A FET can be linearized by biasing at a gate-source voltage ($\mathrm{V_{GS}}$) at which the 3$^{\text{rd}}$ order derivative of its DC transfer characteristic is zero [11]. High 3$^{\text{rd}}$ order input inter-modulation distortion products ($\mathrm{IIP_3}$) can be achieved only in the neighborhood of the bias point usually called 'soft spot'; e.g. linearity improves for signal power under -25dBm. In addition, this linearization method is very sensitive to process, voltage and temperature (P.V.T.) variations. The sweet spot of $g_3 = 0$ can be seen in the Fig. 2.7 [11] at $V_{GS} \approx 0.66$V.

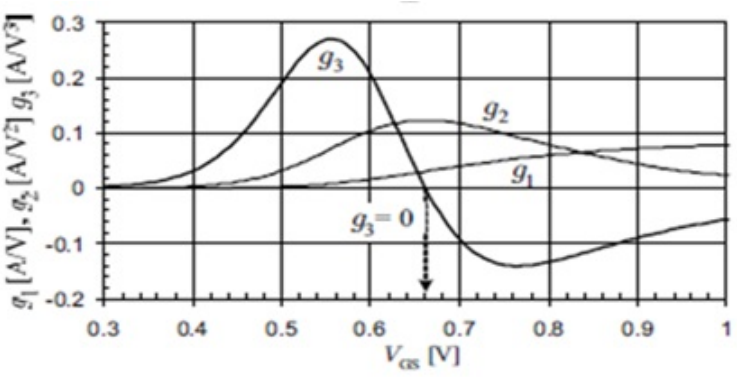


Figure 2.7: Optimum gate biasing sensitive to P.V.T. variations [11]

2.4.2. Derivative superposition method

Research has been done to cancel 2nd order derivative of gm for high linearity. One way of canceling is by using two transistors working different region. Fig. 2.9 shows DC current, transconductance and its 1st order and 2nd order derivative of single transistor over V_{GS} with V_{DS} fixed.

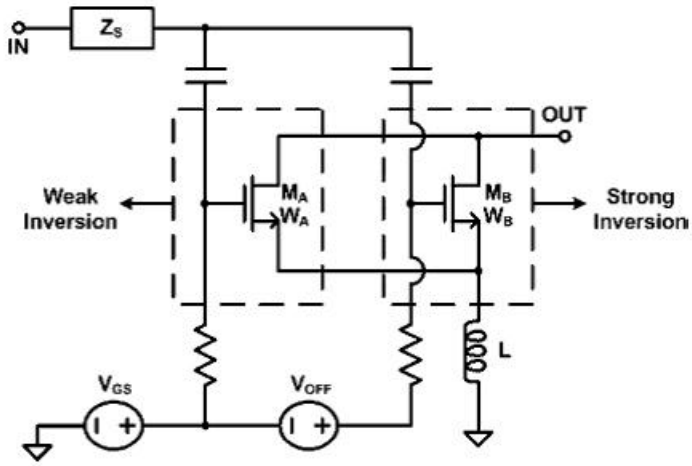


Figure 2.8: DS method implementation [16]

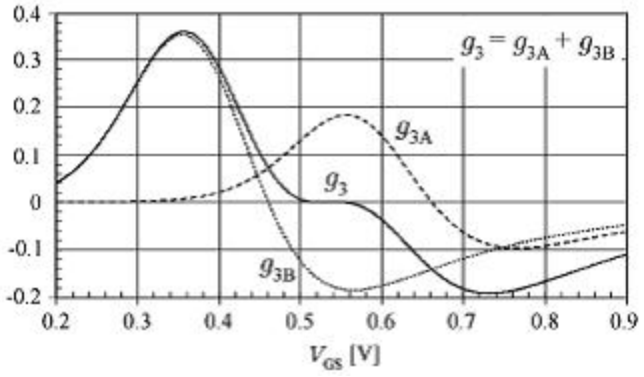


Figure 2.9: DS method of overlapping the 2nd order derivatives of g_m in strong and weak inversion transistors [16]

The transistor level implementation of the Derivative superposition method to cancel the 3rd order distortion is shown in Fig. 2.8. As we can see from the Fig. 2.9, 2nd order derivative of g_m in weak inversion region and that in strong inversion region have different polarity. Exploiting this characteristic, low distortion region could be achieved. Suppose that main transistor, M_B, is working in the strong inversion. Its 2nd order derivative of g_m is negative. The additional transistor, M_A, working in the weak inversion could minimize the 2nd order derivative of g_m. Since usually the positive peak magnitude of 2nd order derivative of g_m is larger than the negative peak magnitude, the size of the additional transistor is smaller than that of the main transistor. Thus by combining g_3 of strong inversion and weak inversion transistors with opposite polarities, the effective $g_3 = g_{3A} + g_{3B}$ can be made zero, as shown in Fig. 2.9. As the additional transistor is working in weak inversion region, only little amount of additional current is required.

This conventional DS method has some drawbacks along with the benefits. If the transistor working region is not properly set, 1st order derivative of g_m i.e, g'_m could

be accumulated which consequently could increase the 2nd order distortion and affect the SNDR at the LNA output. As we can see in the Fig. 2.6, if we assume that M_A and M_B are working at the marked regions, we could cancel 2nd order derivative of g_m. Unfortunately, however, 1st order derivative of g_m plot in Fig. 2.6 shows that this method will add 1st order derivative of g_m of M_A and that of M_B. Furthermore, each transistor's 1st order derivative of g_m is fairly large at the marked regions. Biasing could also be a potential problem. Constant voltage biasing for transistors is sensitive to process and temperature variation while constant current biasing is proved to be stronger against process and temperature variation. However, the decision scheme of current value which helps DS method to be reliable against variation is questionable.

2.4.3. Linearization by multi-gated transistors (MGTR)

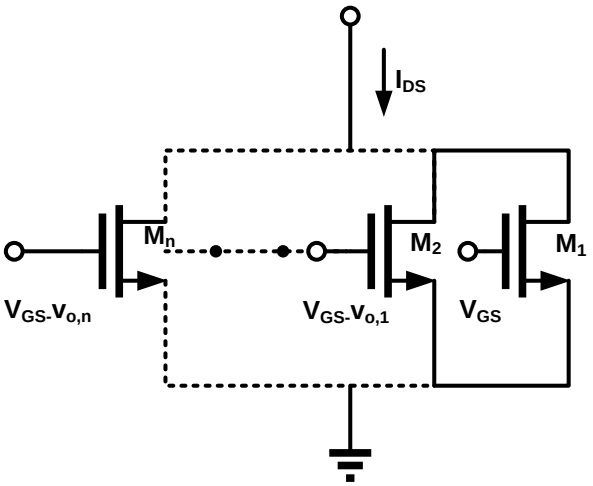


Figure 2.10: Schematic of MGTR with n transistors in parallel [9]

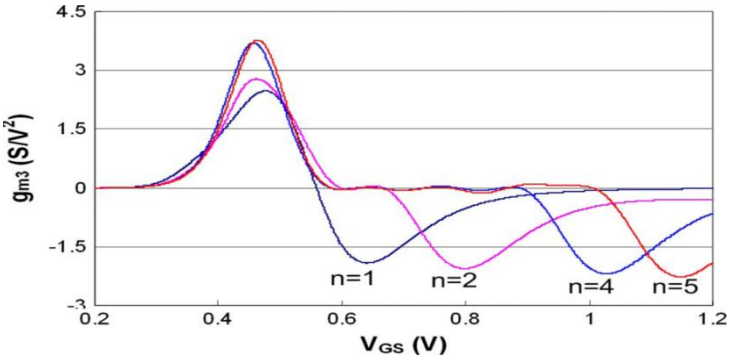


Figure 2.11: Simulated g_3 of MGTR with different number of transistors [9]

To reduce the 3rd order Input referred Inter-modulation product (IIP_3) sensitivity to the bias, an improved derivative superposition (DS) method was proposed in [17]. It employs multiple gated parallel (auxiliary) FETs of different widths and gate biases to achieve a composite DC transfer characteristic with an extended range in which the third-order derivative is close to zero. Schematic implementation of the MGTR is shown in Fig. 2.10. Simulated 3rd order distortion coefficient, g_3 of the MGTR transistor is shown in Fig. 2.11. The effective g_3 is zero for wide range of input signal, making it robust to P.V.T. variations.

These auxiliary transistors biased in sub-threshold region add higher order harmonic components because they turn on and off for large voltage swings. It is, however, difficult to achieve high linearity figures for all technology corners and temperature variations. With the increase in number of transistors the input range increases at the expensive of higher input capacitor. It should be remember that this parasitic capacitor C_{gs} is nonlinear too. Beyond certain number of auxiliary transistors, the nonlinearity of C_{gs} can dominate the nonlinearity of g_m.

2.5. Proposed Linearization Technique: Robust Derivative Superposition

Research has been done for canceling 2^{nd} order derivative of g_m using derivative superposition technique to improve IIP_3 in narrow-band application [16]. Unfortunately, derivative superposition normally accumulate 1^{st} order derivative of g_m, if working regions for transistors are not carefully chosen. Furthermore, voltage biasing of derivative superposition makes this method sensitive to process and temperature variation. In this work, it is shown that exploiting the inherent high f_T of deep sub-micron transistors and the proposed techniques based on the derivative superposition method, highly linear figures can be achieved for broadband LNAs. Design procedure, selection of transistors working region and biasing scheme are also presented.

In the previous sections the importance of RF front-end linearity to broadband receivers was discussed. Any proposed linearization technique should effectively work for broadband frequencies. In order to characterize and confirm that the proposed linearization scheme works for broad band frequencies, two simple and popular topologies are chosen in the current research. To make the linearity characterization more efficient and to simply the input matching network, a resistive terminated LNA with an input matching resistance of 50Ω is used as a first test bench. A noise canceling balun-LNA discussed in section 2.2.2 is chosen as a second test bench to evaluate the proposed linearization technique.

2.5.1. *Resistive terminated LNA*

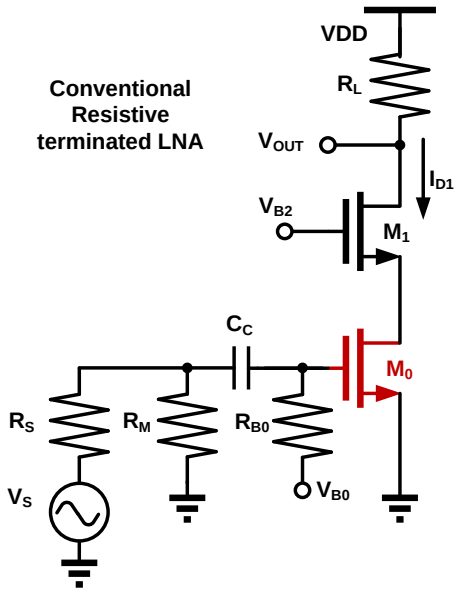


Figure 2.12: Conventional resistive terminated broadband LNA

Fig. 2.12 shows a conventional resistively terminated LNA. R_M is the input resistance of 50Ω for broad-band power matching. The proposed linearization technique assumes the nonlinearity is dominated by the g_m and neglects the non-linearities from the other sources like parasitic capacitors and output conductance. This assumption is fair if the operating frequencies are less than $f_T/10$ [14] and the output signal swings are small, as in a current mode receiver [18].

Fig. 1.2 shows an example of current mode receiver in which the the low noise transconductance amplifier (LNTA) drives a passive mixer and trans-impedance amplifier (TIA) combination. The input impedance of the LNTA load (passive mixer + TIA) can be as small as 5Ω and can have a peak value of less than 30Ω for inband

frequencies (discussed in chapter 3). As the load impedance is small and the output voltage signals at the LNTA output are small. Thus the nonlinearities from the g_{ds} are negligible and distortion is mainly limited by the g_m.

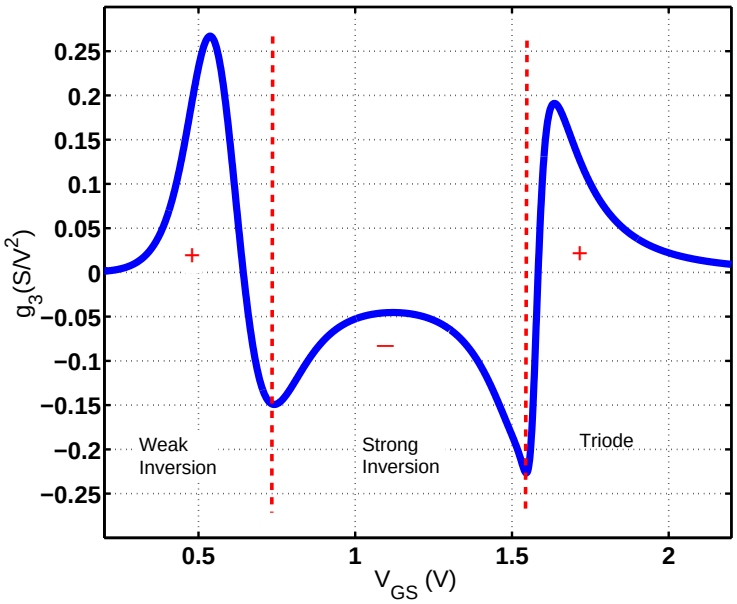


Figure 2.13: g_3 of a transistor in different operating regions

First we characterize a transistor to find its 3$^{\text{rd}}$ order distortion component (g_3). Fig: 2.13 shows the 3$^{\text{rd}}$ order nonlinearity characteristics of the resistive terminated LNA shown in Fig. 2.12. It can be noticed that g_3 crosses through zero and has different polarity in different regions of operation. It can be noticed from the figure and has been reported in previous publications [16] that the third-order variation of the current, $(d^3I_D)/(dV_{GS}^3) = g_m'' = 3!g_3$ in a saturated transistor M_0 is negative. On the other hand, g_3 for a weak inversion region biased transistor, M_S and triode region biased transistor, M_T are positive [16, 19].

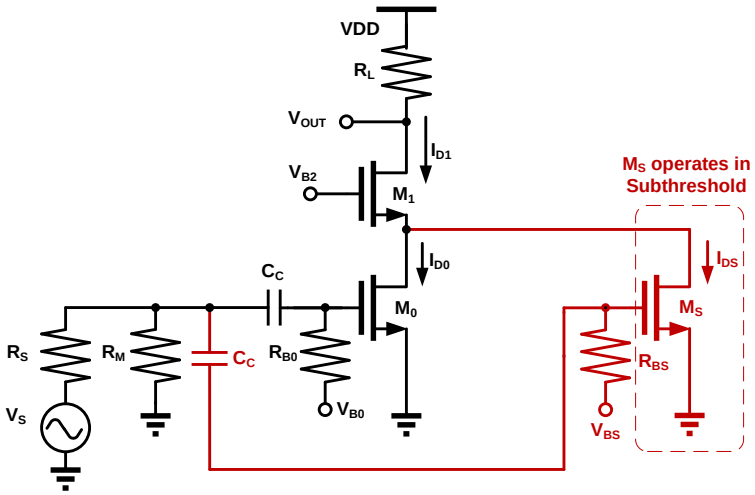


Figure 2.14: Conventional derivative superposition (DS) method to improve IIP_3

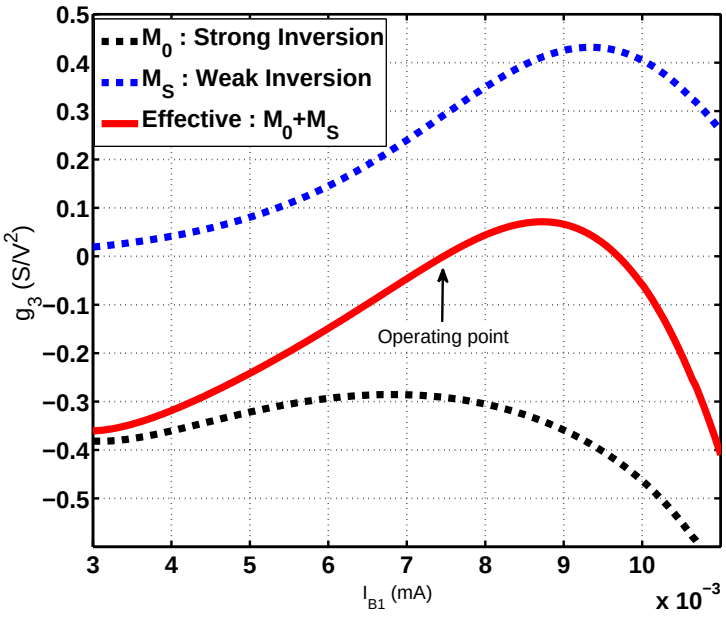


Figure 2.15: g_3 cancellation at single operating point in conventional DS method

The conventional derivative superposition linearization technique is briefly discussed in section 2.4 and also shown in Fig. 2.14. The positive polarity of the g_3 in a weak inversion transistor M_S is used to cancel the negative g_3 of a strong inversion transistor M_0. The cancellation is shown in Fig. 2.15. From the figure it can be noticed that the effective g_3 is canceled at a single bias point, usually called "soft spot".

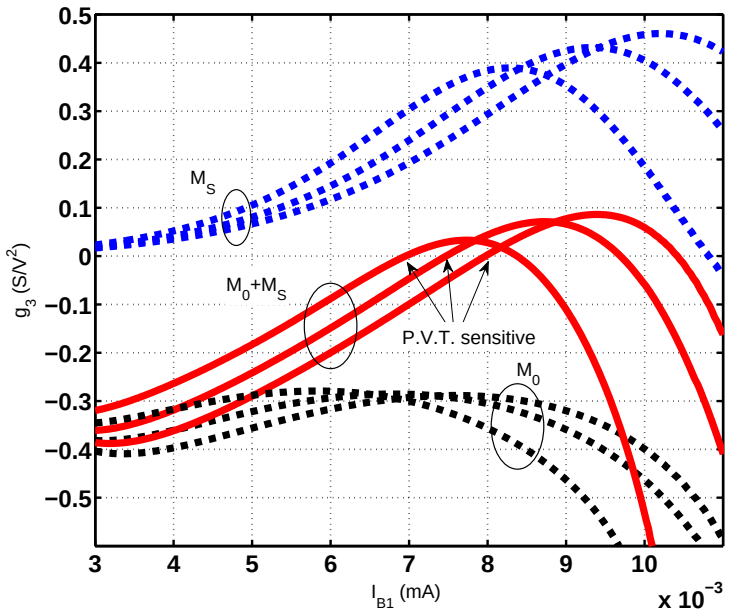


Figure 2.16: Simulated waveforms showing the sensitivity of 3$^{\text{rd}}$-order harmonic cancellation at various technology corners in conventional DS method

If the circuit can be accurately biased at this "soft spot", large IIP_3 can be achieved. But P.V.T. variations usually change the bias point as shown in Fig. 2.16 and the cancellation may not be accurate. Besides, the cancellation is only for very short input range. This limits the large signal linearity (P_{1dB}). Thus the conventional

derivative super position method is sensitive to P.V.T. variations and not effective for large signal linearity.

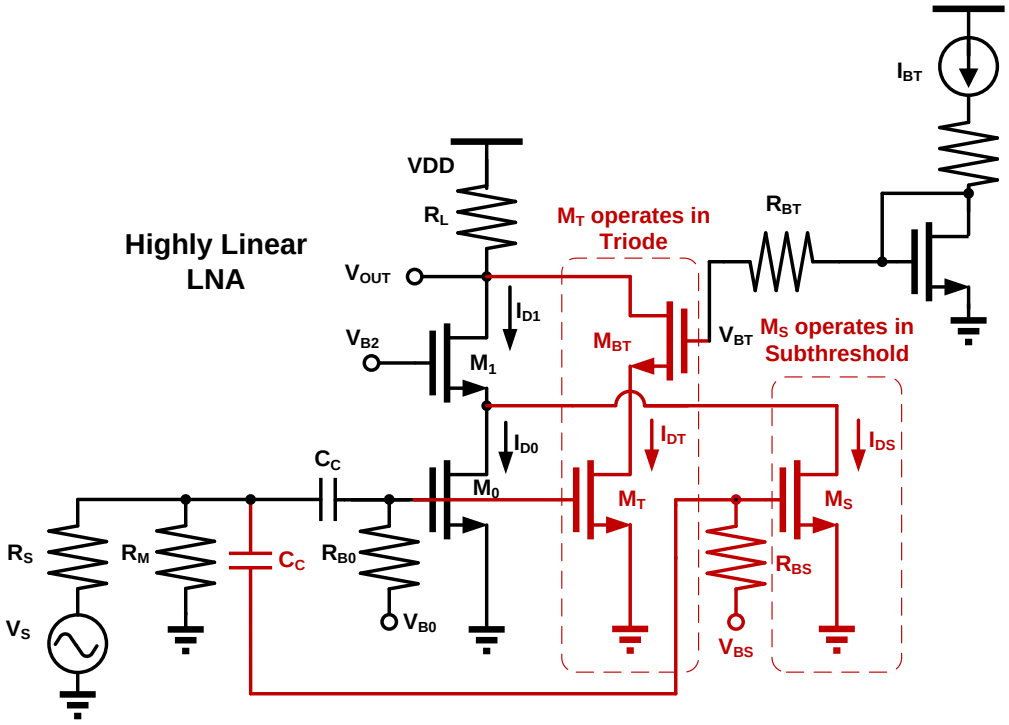


Figure 2.17: Highly linear LNA employing proposed robust derivative superposition (RDS) method

Based on the observations in Fig: 2.13, the linearized architecture is constructed with the main transistor M_0 operating in strong inversion and compensated by a two auxiliary transistors operating in triode (M_T) and sub-threshold (M_S) regions, respectively, as shown in Fig. 2.17. The negative 3rd-order nonlinearity of the main transistor M_0 is efficiently compensated by the positive 3rd-order non-linearities of M_T and M_S, improving the IIP_3 by 11dB. Contrary to other linearization techniques,

the combination of transistors operating in triode and sub-threshold regions show smooth positive third-order nonlinearities that can be easily adjusted to cancel the negative 3rd harmonic distortion component of the main transistor. A remarkable property is that the curvatures of g_m'' for the three transistors M_0, M_S and M_T oppose and compensate each other, allowing nonlinearity cancellation for large signals when the currents of these transistors are combined as depicted in the Fig. 2.18. For a fair comparison, the conventional and the linearized LNAs are fabricated separately on the same die.

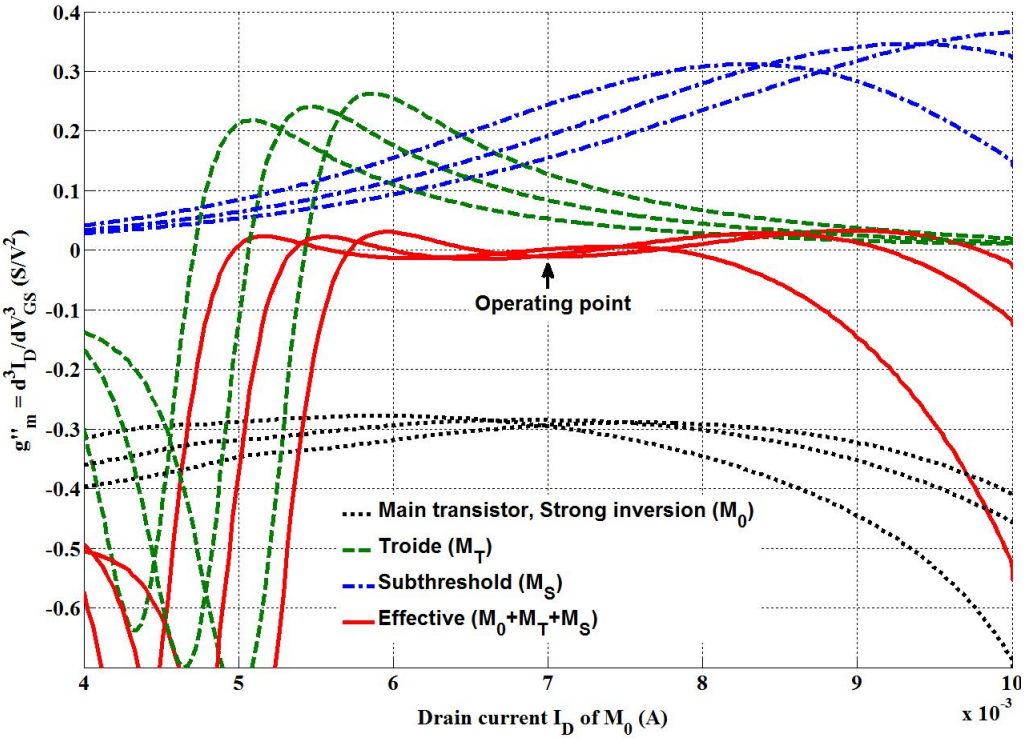


Figure 2.18: Simulated waveforms showing the cancellation of 3rd-order harmonic at various technology corners in a RDS linearization technique

Fig. 2.18 shows the simulated waveforms of the third-order nonlinearity coefficient from all the three M_0, M_T and M_S transistor as well as the composed topology at typical-typical, slow-slow and fast-fast corners. Notice that the cancellation is insensitive to P.V.T variations. The proposed architecture achieves high linearity over a large input range. Outstanding linearity is achieved even if 7mA bias current of M_0 changes by 1 mA around the operating point. An important design aspect in this scheme is that the channel delays from the main circuit path and the auxiliary paths are similar at RF frequencies such that the nonlinearity cancellation is carried out with enough accuracy over the desired frequency range. In practice, RDS is affected by the drain-source voltage of the triode transistor M_T. The V_{DS} of M_T is fixed through M_2 and its bias network. M_2 also avoids LNA gain degradation due to the finite output resistance of M_T.

Table 2.1: Dimensions and parasitic capacitors of transistors in RDS schematic in Fig. 2.17

	M_0	M_T	M_S
Width(μm)	94	9	56
Length (μm)	0.18	0.18	0.18
C_{gs} (fF)	150	15	70
Current (mA)	6.96	0.35	0.065

Table 2.1 shows the sizes, parasitic capacitance and currents in each branch of the RDS linearization technique. Although M_S is a medium size transistor, the input gate capacitance is less because it is operating in weak inversion region. Thus, the bandwidth is not affected significantly. Another advantage of the triode transistor

is that M_T can share the same gate bias as that of M_0 which avoids an additional AC coupling capacitor. Because the compensating transistors are small, their bias currents I_{DT} and I_{DS} are less than 5% of the bias current, I_{D0} used for M_0. As the compensation is a feed-forward scheme, the stability of the LNA is unaffected.

2.5.2. Wide-band balun LNA

The proposed linearization technique can also be employed in broadband inductorless balun-LNA architectures [12, 13] as depicted in Fig. 2.19. This common-gate common-source topology presents significant benefits such as balanced outputs as well as noise and distortion cancellation in the CG stage [12]. However, the noise and distortion performance of this LNA is limited by the CS amplifier (M_{N1} in Fig. 2.19). Equal transconductances and load resistors (R_L=100Ω) are employed in both CG and CS stages to maintain the circuit balanced.

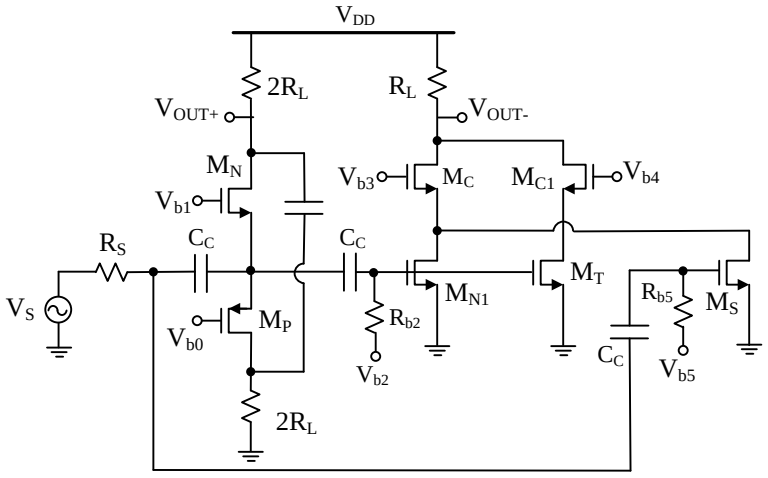


Figure 2.19: Noise and distortion canceling balun-LNA employing RDS linearization technique

Assuming perfect noise cancellation in the CG stage, the simplified noise factor (F) for the balun-LNA is given by

$$F = 1 + \frac{\gamma g_{mCS} R_L^2 (1 + g_{mCG} R_s)^2}{R_s A_V^2} \tag{2.8}$$

$$A_V = (g_{mCG} + g_{mCS}) R_L \tag{2.9}$$

$$g_{mCG} = g_{mN} + g_{mP}, \quad g_{mCS} = g_{mN1} \tag{2.10}$$

where γ is the fitting parameter of the noise model. Its value is around $2/3 \sim 2$ for short channel devices. Noise contributions from the auxiliary transistors, M_S and M_T are negligible as their transconductances are significantly smaller than the main transistor. By applying the proposed linearization technique, IIP_3 and P_{1dB} compression point of 16.8dBm and 0.5dBm respectively, are achieved. Noise/distortion cancellation of the balun-LNA and the advantages of using the PMOS-NMOS for the input CG stage will be explained in chapter 3.

2.6. Test Chips and Measurement Results

Fig. 2.20 shows the chip photo-micrograph of the test chips. Due to the intrinsic high linearity of the LNAs, adding an on-chip output buffer for measurement would degrade the linearity performance to be observed. Hence the three LNAs were implemented as standalone blocks without any buffer on Jazz Semiconductor 0.18μm CMOS technology. The main goal was to test and compare the linearity performance. In the three LNAs, resistor $R_L$was chosen to be 100Ω as a compromise to achieve good internal gain and output matching. The total load resistance seen by the LNA without a buffer is $R_L||R_{PORT} = 33.3\Omega$, which is in the range of the impedance presented by a passive mixer and TIA combination [20]. The chip was wafer probed using RF probes at the input/output pads and DC probes at the bias

pads. Area of each test chip is 0.06mm^2

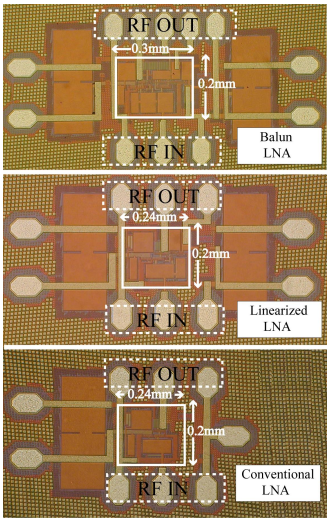


Figure 2.20: Chip micrographs of LNA prototypes on 0.18μm CMOS technology

2.6.1. S_{11} and voltage gain

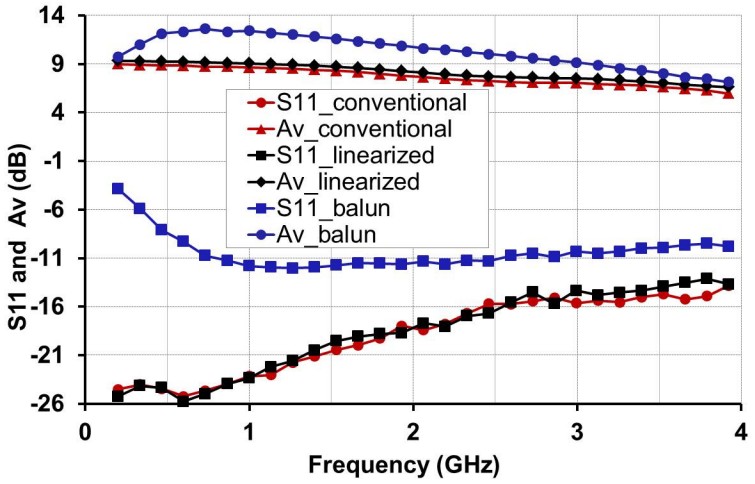


Figure 2.21: Input matching and gain performance of the three LNAs

Fig. 2.21 displays S_{11} and unloaded voltage gain A_V (internal gain by de-embedding the 50Ω load impedance of the test equipment) of the LNAs. As the resistively terminated LNAs have 50 Ω input matching resistors (R_M), the results show broadband input matching. As in [10], gains A_V of the LNAs were de-embedded from the measured S-parameters using the port impedance (Z_{PORT}) of the output port (50Ω for a single-end port, 100Ω for a differential port), where the characteristic impedance Z_0 is 50Ω:

$$A_V = S_{21}\frac{Z_{22} + Z_{PORT}}{Z_{PORT}} + 3dB(balun) \tag{2.11}$$

$$Z_{22} = \left\{\frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right\} \tag{2.12}$$

In the case of the balun lna, S_{21} is the single-ended input to differential output S-parameter gain. So 3dB is added to A_V to take the 50Ω-to-100Ω impedance conversion into account

2.6.2. Linearity

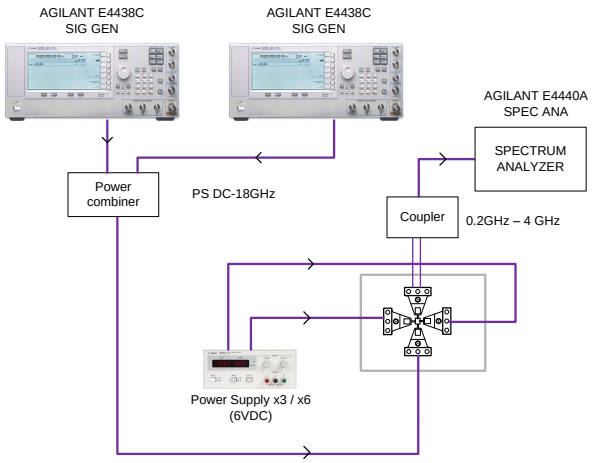


Figure 2.22: Two tone measurement setup to characterize the linearity of LNA

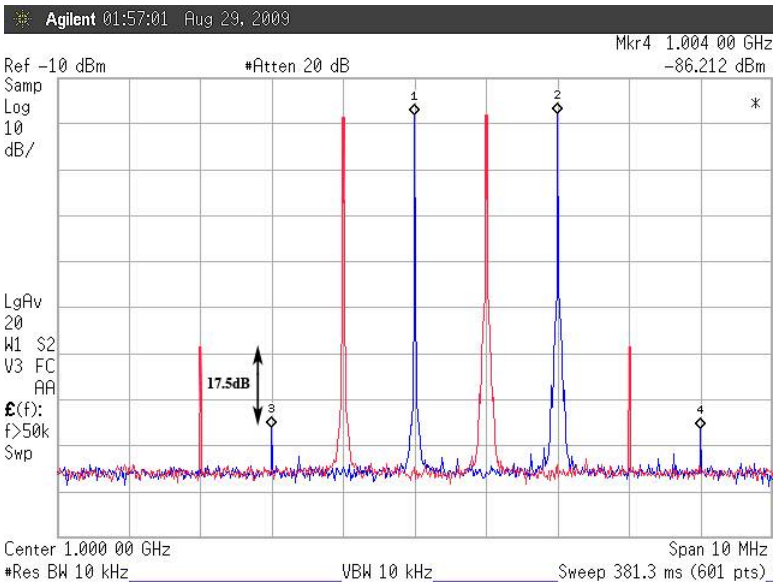


Figure 2.23: Measured two tone test results for the resistive terminated LNA

Fig. 2.22 shows the measurement setup for characterizing the linearity of the LNA. Two signal generators are used to generate the two tones and are combined to through a power combiner before giving it the the device-under-test (DUT) (LNA). Extensive characterization is done by changing the frequency spacing of the two tones, varying the power of the tones, characterizing multiple chips for mismatch. In case of balun LNA, as the output is differential, a coupler is used to convert the differential signal into single ended before giving it to the spectrum analyzer.

Two-tone test results are shown in Fig. 2.23. The results are for the frequency spacing of (Δf) = 2MHz at -16.5dBm input power per tone. The input tones are 999MHz and 1001MHz for the conventional resistive terminated LNA (no markers) and 1000MHz and 1002MHz for the linear LNA (markers). The linearized LNA outperforms the conventional LNA by 17.5dB of IM3 improvement for the case of -16.5dBm input power per tone.

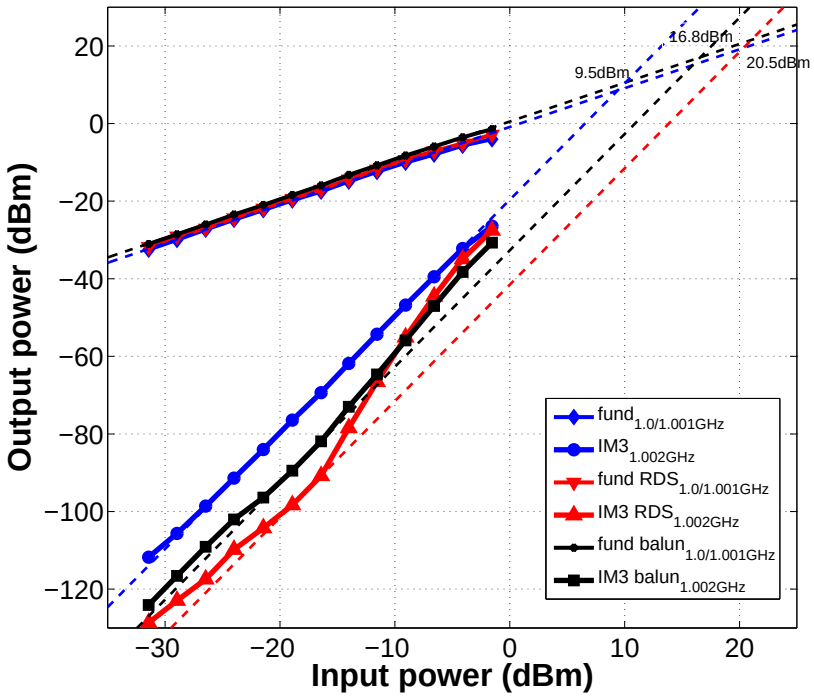


Figure 2.24: Meausred IIP_3 of the three LNAs

Fig. 2.24 shows the measured IIP_3 characterization of three LNAs. RDS technique in resistive terminated LNA improves IIP_3 by 11dB from 9.5dBm to 20.5dBm. Fig. 2.24 also shows the measured IIP_3 of 16.8dBm for balun-LNA. For very large signals, the compensation circuits enter into highly nonlinear regimes, resulting in limited linearity improvement mainly due to the transistor operating in the sub-threshold region. If large input power is expected, the operating points of both M_T and M_S have to be judiciously selected.

Fig. 2.25 shows the frequency dependancy of IIP_3. It can be noticed that IIP_3 is constant over the frequency with very small variations. This shows that the proposed linearization technique is very effective over wide frequency range.

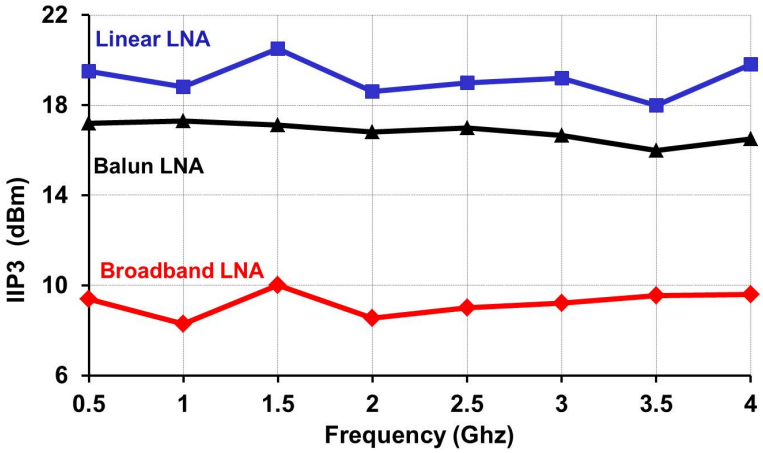


Figure 2.25: IIP_3 vs average frequency of the tones in a two tone test

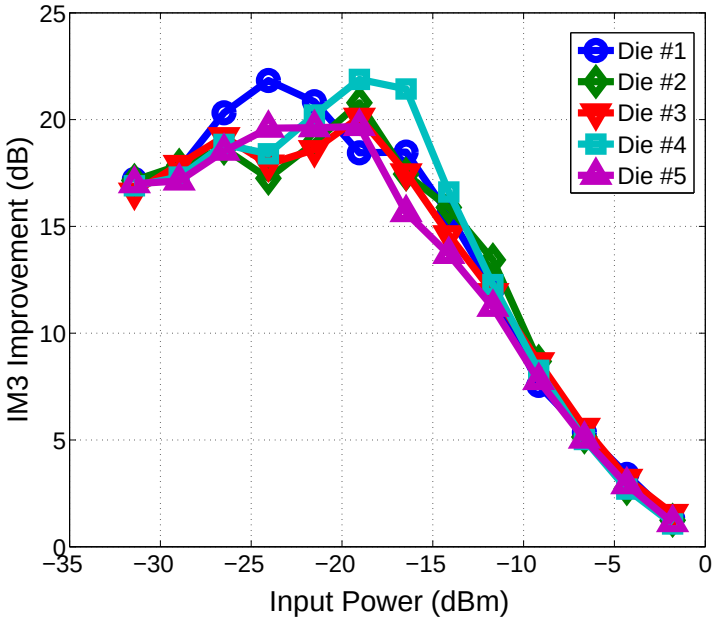


Figure 2.26: Measured linearity improvement performance of five chips

The linearity improvement as a function of input power is shown in Fig. 2.26, where the non-monotonic variations of IM3 at the lower input power are due to the measurement inaccuracy at low power levels (no on-chip output buffer). The figure reveals that the linearity of the linearized LNA outperforms the conventional LNA by 10dB with input signal power as high as -10dBm showing good large signal linearity. It also demonstrates the robustness of the linearization scheme to mismatches, since IM3 is improved by more than 10dB up to -10dBm input power for five dies at the same bias condition.

2.6.3. Noise figure

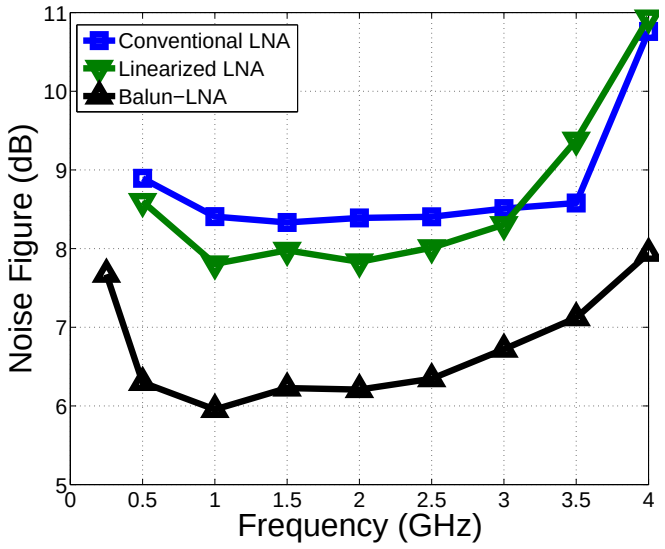


Figure 2.27: Measured NF of the conventional, linearized and balun-LNAs

Fig. 2.27 shows the measured NF of the three LNAs. The main reasons for relatively high noise figures are the resistive termination at the input of the conventional

and linearized LNAs, non-optimized layout with respect to minimization of the noise contribution due to gate resistance (noise contribution from the gate resistance can be reduced by increasing the number of fingers in the transistors), and the inaccuracy associated with the noise measurements without an output buffer. Without the output buffer, the LNA is loaded with a noisy 50Ω of the output port. The loading decreases the gain and the noise contribution of the output port is significant.

The chip photomicrograph is shown in Fig. 2.20. The conventional and linearized single-ended resistive terminated LNAs occupy 0.24 $0.2mm^2$ each while consuming 6.96mA and 7.5mA from 2.4V supply, respectively. The balun-LNA occupies 0.3 $0.2mm^2$ while consuming 7.1mA from a 2V supply. As evident from Table 2.2, the balun-LNA achieves similar or better performance compared to recent broadband CMOS LNAs.

2.6.4. Performance summary

Table 2.2: Performance comparison with recently published works

	[12]	[21]	[22]	[23]	This work
Tech..[nm]	65	130	8130	45	180
BW [GHz]	0.2-5.2	1-7	0.8-2.1	0.6-10	0.3-2.8
A_V[dB]	13-15.6	17	14.5	10	9.6-12.5
NF [dB]	2.9-3.5	2.4	2.6	3	5.95-6.5
IIP_3 [dBm]	0-4	-4.1	16	6	16.8
Power[mW]	14	25	17.4	30	14.2
Vdd[V]	1.2	1.4	1.5	-	2
No. of Coils	0	0	0	2	0
Area(mm^2)	0.009	0.019	0.0992	-	0.06
FOM	16.22	6.343	102.3	-	34.3

$$FOM = \frac{IIP3_{AVG}[mW].PowerGain_{AVG}[abs].BW[GHz]}{Pdc[mW](F_{AVG}-1)} \tag{2.13}$$

2.7. Summary

A highly linear LNA for SAW-less radios is proposed. A robust derivative superposition technique insensitive to process variations with little penalty in power consumption ($< 6\%$) and wide-band frequency effectiveness was proposed. The technique was employed and validated in the designs of a resistively terminated LNA and a balun-LNA. The balun-LNA presented in this work simultaneously achieves impedance matching, noise and distortion canceling, and a well-balanced output. The proposed linearization approach can be extended to most of the existing topologies.

3. WIDE-BAND, INDUCTOR-LESS, LOW NOISE TRANSCONDUCTANCE AMPLIFIERS WITH HIGH LARGE-SIGNAL LINEARITY*

3.1. Introduction

Future communication devices are expected to support multiple standards and features on a single chip. Therefore, significant research efforts have been dedicated to develop wide-band receivers that can replace the multiple narrow-band front-ends [18, 20, 24, 25]. Since wide-band receivers have much less frequency selectivity comparing to narrow-band receivers, the front-end circuit amplifies not only the in-band signal but also the out-of-band (OOB) signals. Strong OOB signals can potentially clip or saturate the front-end Low Noise Amplifier (LNA) resulting in gain compression and inter-modulation, hence reduce the signal-to-noise ratio (SNR) in the receiver. OOB blockers or jammers may also degrade the SNR by reciprocal mixing with the LO phase noise [20]. Therefore, linearity in the front-end LNA is very critical to avoid distortion and signal compression especially in presence of strong OOB blockers.

Inductor-less wide-band LNAs are becoming popular due to the reduction in the real estate of the silicon [3, 12, 26]. These LNAs significantly reduce cost, area, and power, while enabling simultaneous processing of several channels. But absence of inductors removes the inherent on-chip filtering provided by the passive inductors in the RF front-end and thus demands high linearity in the LNA over wide frequency range to accommodate the different standards. Linearity requirement in wide-band systems due to concurrent reception of multiple channels without filtering becomes

*Part of this chapter is reprinted with permission from "Fully balanced low-noise transconductance amplifiers with P1dB > 0dBm in 45nm CMOS,", by H. M. Geddada *et al.*, *IEEE Proc. ESSCIRC*, pp. 231−234, Copyright 2011 by IEEE

more challenging especially with SAW-less receivers [18, 20, 24, 25]. Another major challenge in the LNA design is achieving a low noise figure (NF) while satisfying impedance matching requirements over several GHz of bandwidth [3, 12, 26].

This chapter deals with the design of two broadband inductor-less fully balanced LNTAs outperforming the large signal linearity of existing solutions. A remarkable in-band 1-dB compression point (P_{1dB}) of approximately 0dBm for broadband operation in an environment of coexisting radios operating simultaneously in close proximity is the key achievement. The proposed architectures employ noise and distortion cancellation techniques which make them suitable for broadband applications. Complementary RF characteristics of NMOS and PMOS transistors are utilized to improve IIP_2 and IIP_3.

The chapter is organized as follows. Section 4.2 introduces some of the recent and most promising blocker tolerant receiver architectures; it is also shown how the proposed LNTA can be employed in those architectures. Section 4.3 discusses the LNTA architecture. Power, noise, linearity trade-offs and the circuit implementation are discussed in section 4.4. Section 4.5 discusses the measurement results and conclusions are drawn in section 4.6.

3.2. Receiver Architecture

Many architectural innovations have been reported to develop wide-band blocker resilient receivers. Mixer first architectures with good linearity have been reported in [27–29]. As front end LNA is missing, these architectures suffer from noise and LO feed through to antenna. Authors in [18, 25] propose a blocker-tolerant receiver by employing the LNA and voltage sampling mixer as shown in Fig. 3.1. Impedance looking into the down conversion mixers has a bandpass characteristic that tracks the LO frequency. The resultant high-Q filter loads the wide-band LNA. LNA sees

high impedance for in-band signals and thus amplifies them. For OOB frequencies, LNA sees low impedance and are then attenuated resulting in blocker filtering and good OOB linearity.

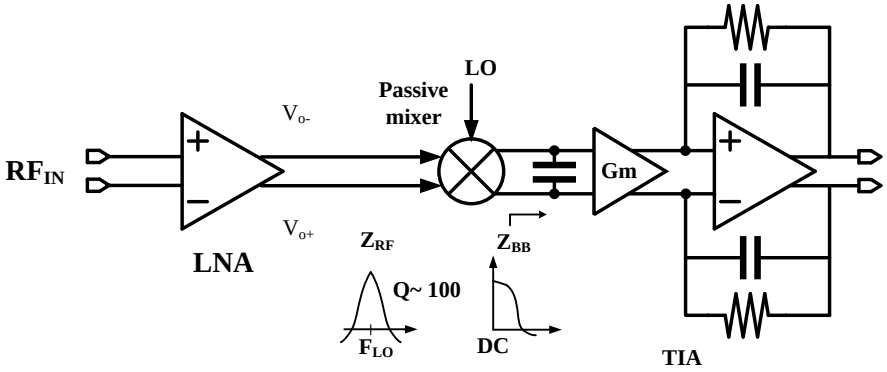


Figure 3.1: Blocker tolerant radio architectures: voltage-mode receiver [25]

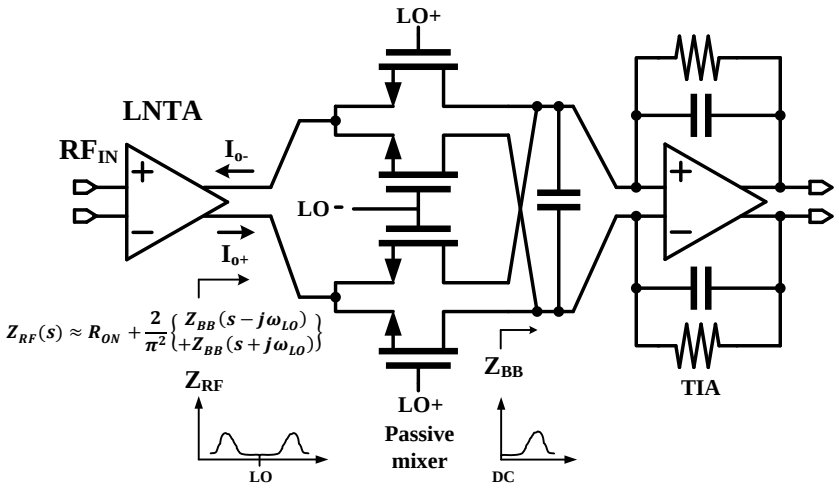


Figure 3.2: Blocker tolerant radio architectures: current-mode receiver [20]

Another relevant work on blocker resilient receivers is shown in Fig. 3.2 [20, 24]. This architecture replaces the front end LNA by a RF transconductance (LNTA). The LNTA is followed by a current-mode passive mixer and a TIA combination. In such an approach, the impedance seen by the LNTA is the series combination of mixer switch resistance and the up converted input impedance of the TIA. Thus low load impedances (Z_{RF}) for LNTA can be ensured. Z_{RF}, a function of frequency, can be as small as 5 Ω and can have a peak value of less than 30 Ω, depending on R_{ON} and Z_{BB} as given by Eq. 3.1. This architecture offers better performance than both active mixer and voltage-mode mixer implementations in terms of noise, linearity and power consumption [18].

$$Z_{RF}(s) = R_{ON} + \frac{2}{\pi^2}\{Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO})\} \tag{3.1}$$

In Eq. 3.1, R_{ON} is the 'ON' resistance of the passive mixer switch and Z_{BB} is the input impedance of the baseband filter, TIA. ω_{LO} is the local oscillator frequency in direct conversion receiver. At low frequencies, $Z_{BB} \approx \frac{1}{G_{m,TIA}}$.

In this work, the proposed inductor-less, wide-signal wide-band LNTAs are targeted for the receiver architecture in Fig. 3.2. Power consumption in this architecture scales down with technology [30]. It also has the potential to handle large signal with less distortion as the information is carried in current [20, 30].This architecture also have the advantage of low output impedance for the LNTA and thus reduced output nonlinearity with less output signal swings. Wide-signal operation and distortion of the LNTA is mostly determined by the MOSFET transconductance in the LNTA. By these architectural improvements, the LNTA sees low load impedance at the output. By having low voltage signal swings at the output node, the targeted LNTA avoids output nonlinearities and achieves large linearity figures.

This chapter deals with the design of two broadband, inductor-less, fully balanced LNTAs with high large signal linearity. A worst case 1-dB compression point (P_{1dB}) of approximately 0dBm for broadband operation in an environment of coexisting radios operating simultaneously in close proximity is the key achievement. The proposed architectures employ noise and distortion cancellation techniques which make them suitable for broadband applications. Complementary RF characteristics of NMOS and PMOS transistors are utilized to improve IIP_2 and IIP_3.

3.3. LNTA Architecture

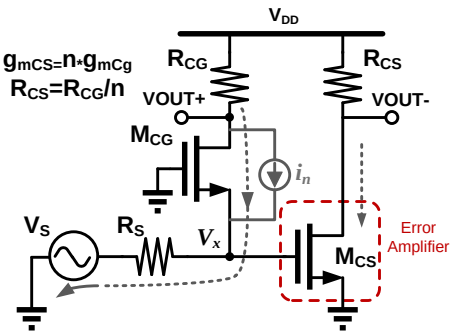


Figure 3.3: Noise and distortion canceling LNA

Blaakmeer et al. proposed noise canceling common gate (CG) common source (CS) balun-LNA in [12] as shown in Fig. 3.3. Common-source (CS) stage acts as an error amplifier (EA) stage to cancel the noise/distortion (errors) of the input common-gate (CG) stage. This topology employed unequal transconductance gains (g_m) in the CG and CS branches as well as unequal output impedances to minimize the noise contribution of the CS stage. The unbalanced devices are sensitive to process variations and therefore degrade the differential operation of the entire

receiver. Also, the NF degrades if equal g_m's are employed in both the branches of this topology under the same input matching constraints. Noise and distortion performance of this LNA is limited by the CS stage. Work reported in [3] improved the linearity of this amplifier topology by linearizing the CS stage with a linearization scheme proposed in [2]. It achieves good linearity but still suffers from high NF due to the use of equal load impedances for CG and CS stages. To improve the large signal handling, [30] proposes a wide-swing LNTA but has lower g_m demanding better noise performance from the following stages in a radio receiver.

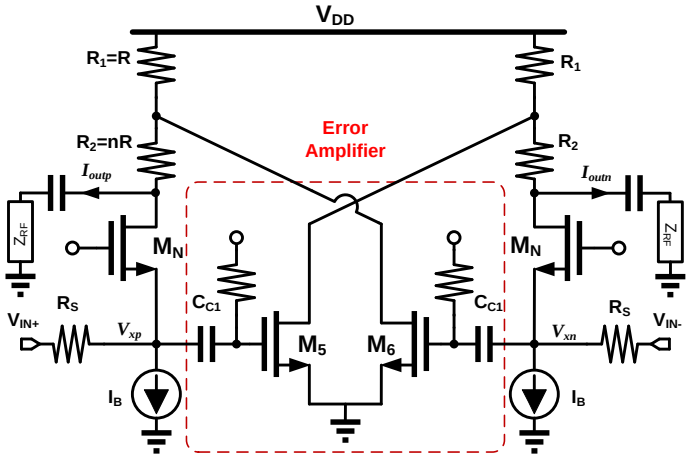


Figure 3.4: Fully balanced differential LNTA employing noise and distortion cancellation

In this work a fully balanced differential architecture with low NF and high linearity with large signal operation is proposed. Fig. 3.4. shows the simplified schematic of the proposed LNTA. The CG transistors M_N realize the input stage, whereas the CS transistors M_5 and M_6 realize the error amplifier (EA) stage of the LNTA. A remarkable property of this configuration is that noise and distortion of

the CG transistors appear as common mode signals at the output and are canceled in the differential output [12]. The input common gate stage is employed to obtain wide-band input matching and high linearity. The output signals of the CG stage are added with the error amplifier signal through resistive dividers composed by R_1-R_2. Authors in [31] used inductors to combine the signals.

3.4. Circuit Design

3.4.1. Impedance matching and gain

For the LNTA in Fig. 3.4, the input impedance is given as

$$Z_{in} = \frac{R_{in}}{1 + sR_{in}C_p} \tag{3.2}$$

$$R_{in} = \frac{Z_L + r_{0N}}{1 + g_{mN}r_{0N}} \tag{3.3}$$

$$C_P \approx C_{gs,N} + Cgs, 5 + C_{P,c1} \tag{3.4}$$

$$Z_L = (R_1 + R_2)||Z_{RF} \tag{3.5}$$

where Z_{RF} is the input impedance of the next stage as shown in Fig. 3.4 and r_{0N} is the intrinsic output impedance of the transistor. For the targeted architecture in Fig. 3.2, $Z_{RF} < 30\Omega$. Thus $Z_{RF} << (R_1 + R_2) = (n+1)R \approx 300\Omega$, hence $Z_L < 30\Omega$ in Eq. 3.5. As $Z_L << r_{0N}$ in Eq. 3.3, $R_{in} \approx \frac{1}{g_{mN}}$. Parasitic capacitor C_p at the source node of M_N (M_P) node is moderately large and makes the pole $1/(R_{in}C_p)$ as the dominant pole in the system and limits the bandwidth of the LNTA.

Major contributors of C_p are given in Eq. 3.4. $C_{gs,N}$ and $C_{gs,5}$ are the gate-source parasitic capacitors of M_N and M_5 respectively. $C_{p,c1}$ is the parasitic shunt capacitance of AC coupling capacitor C_{C1} which could be large (15% to 20% of C_{C1}) depending on the lower cut-off frequency of the target band-width and the kind of capacitors available in the technology. In practice, a series bond wire inductance

from the package can be used to resonate out this input parasitic capacitance, C_p and improve the bandwidth and S_{11}. Simulations results of this effect are shown in section 4.5. Thus, wide-band input impedance matching can be guaranteed until the effects of the parasitic capacitors limit the frequency response of the input stage. The architecture can operate up to several GHz if deep sub-micron technologies with high f_t are employed.

3.4.2. Noise

In order to calculate the noise factor, some simplifications are made to get some insightful results. The transistors are assumed to have infinite output impedance and the bias current source (I_B) for the CG transistor is assumed to be ideal (Final LNTA implementation does not include the bias current source). Only thermal noise from transistors ($(\bar{i_n^2}/\Delta f) = 4KT\gamma g_m$) and resistors ($(\bar{i_n^2}/\Delta f) = 4KT/R$) are accounted. Noise from the gate resistance (R_g) is ignored. γ is the noise parameter in MOS transistors and is in the range of $2/3 \sim 2$ for short channel devices. The relative noise factor of each noise generating element is obtained by dividing the individual output noise by that of the source impedance $Rs = 50\Omega$. The noise factor, F due to the thermal noise of the CG transistors, CS transistors and resistors, R_1 and R_2 is derived as

$$F_{CG} = \frac{\gamma g_{mCG}(1 - \frac{g_{mCS}R_s}{n+1})^2}{R_s G_m^2} \tag{3.6}$$

$$F_{CS} = \frac{\gamma g_{mCS}(1 + g_{mCG}R_s)^2}{(n+1)^2 R_s G_m^2} \tag{3.7}$$

$$F_{(n+1)R} = \frac{(1 + g_{mCG}R_s)^2}{(n+1)RR_s G_m^2} \tag{3.8}$$

Where F_{CG}, F_{CS} and $F_{(n+1)R}$ are the noise contributions from CG stage, CS stage and resistors (R_1,R_2) respectively. G_m is the effective transconductance from input

(V_{xp}) to output (I_{outp}) and is given by

$$G_m = g_{mCG} + \frac{g_{mCS}}{n+1} \tag{3.9}$$

The topology's noise factor is then obtained as

$$F = 1 + F_{CG} + F_{CS} + F_{(n+1)R} \tag{3.10}$$

According to Eq. 3.6, the condition for noise cancellation of FCG stage is

$$\begin{aligned} g_{mCS} &= \frac{n+1}{R_s} \\ &= (n+1)g_{mCG} \end{aligned} \tag{3.11}$$

Under this condition, Eq. 3.9 reduces to $G_m = 2g_{mCG}$. In the targeted receiver architecture, the impedance seen looking into the passive mixer (Z_{RF}) is small compared to R_1+R_2. So the output current of the error amplifier is divided by the resistors R_1 and R_2 before reaching the output. The effective transconductance of the LNTA is computed as $G_m = 2g_{mCG} = 40mS$. Therefore, the error amplifier allows noise optimization and also boosts the architecture's gain from 20mS to 40mS.

As shown in Fig. Fig. 3.3 and Fig. 3.4, the noise contribution of the CG transistors results in a common-mode noise. The remaining noise present in the LNTA is due to the error amplifier and the resistive dividers. Using Eq. 3.7 and Eq. 3.8, and assuming that Eq. 3.11 holds it can be shown that

$$F_{CS} = \frac{\gamma}{n+1} \tag{3.12}$$

$$F_{(n+1)R} = \frac{R_s}{(n+1)R} \tag{3.13}$$

From Eq. 3.12 and Eq. 3.13 while F_{CS} is independent of R, $F_{(n+1)R}$ decreases with increase in R resulting in less overall NF. But larger R increases the voltage drop on the load resistors (n+1)R decreasing the linearity. For a $g_{mCG} = 20ms = (1/Rs)$, I_{CG} is around 1.4mA for (V_{DSAT} = 140mV) in this technology. Using Eq. 3.12 and for the equal V_{DSAT} in CG and CS transistors, $I_{CS} = (n+1)I_{CG}$. Total current consumption $I_{DC} = (I_{CG}+I_{CS}) = (n+2)I_{CG}$ increases with increase in n. Therefore, increasing g_{mCS} provides better noise performance at the cost of an increased power. So an optimum n and R can be obtained for satisfying NF, voltage headroom and the power. $n = 4$ and $R = 45\Omega$ are chosen in this design.

3.4.3. Power efficient design

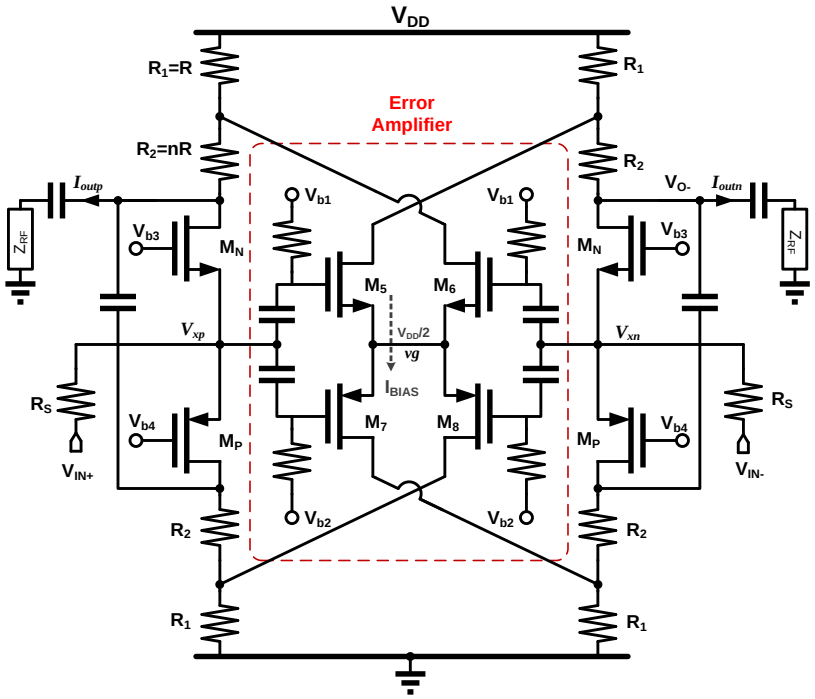


Figure 3.5: Complete schematic of the fully differential LNTA

The schematic shown in Fig. 3.4 is transformed to power efficient and high linearity architecture keeping the noise and input matching properties unaltered. Fig. 3.5 shows the final transformed schematic of the LNTA. The core of this LNTA architecture consists of complimentary PMOS-NMOS CG and CS stages. The input stage is implemented by a current reuse M_N and M_P combination to reduce the power consumption, to improve the circuit linearity, and to avoid the biasing inductors or any noise contribution from additional bias circuitry. PMOS-NMOS pair also removes the even order distortion components and 3^{rd} order distortion due to 2^{nd} order interaction [22] which is discussed in the following section.

The error amplifier stage is also transformed to current reuse PMOS-NMOS pair. First, separately, source terminals of M_5 and M_8 (M_6 and M_7) are connected. Each of these connected nodes acts as a virtual ground independently. But due to the differences in the strength of PMOS and NMOS, the node could deviate from being a virtual ground. In the next transformation, these two independent virtual ground nodes are connected together to make a single strong virtual ground as node v_g in Fig. 3.5. The DC voltage values for the nodes x and v_g can be designed to have $V_{DD}/2$. By stacking the PMOS-NMOS pair, higher supply voltage can be employed without any reliability issue [32]. Thus this transformation to PMOS-NMOS combination improves the architecture's power and linearity performance. The details are briefly explained in the next few sections.

3.4.4. Linearity

Since the LNTA is driving a low impedance, the output voltage swing is assumed to be small and hence nonlinear effects of the transistor output conductance (g_{ds}) are negligible. This implies that the major source of nonlinearity stems from the transconductance of the LNTA. Using a power series expansion for the transistor's

soft non-linear model, the drain current of the NMOS transistor (M_N) is given by

$$i_{ds} = g_1 V_{gs} + g_2 V_{gs}^2 + g_3 V_{gs}^3 + \dots \tag{3.14}$$

where g_i is th ith -order distortion coefficient of a transistor obtained by taking derivative of the drain-source DC current I_{DS} with respect to the gate-to-source voltage V_{GS} at the DC bias point

$$g_1 = \frac{\partial \mathrm{I_{DS}}}{\partial \mathrm{V_{GS}}}, \qquad g_2 = \frac{\partial^2 \mathrm{I_{DS}}}{2! \partial \mathrm{V^2_{GS}}}, \qquad g_3 = \frac{\partial^3 \mathrm{I_{DS}}}{3! \partial \mathrm{V^3_{GS}}} \tag{3.15}$$

From Fig. 3.5, in the present implementation of stacked PMOS-NMOS stages, the nonlinear current in the PMOS (M_P) has the same expression but with opposite polarity for v_{gs}. So, $v_{gs} = v_{gs,n} = -v_{gs,p}$. The total drain current from the single ended input CG stage is given by

$$\begin{aligned} i_{CG} &= i_{ds,N} - i_{sd,P} \\ &= i_{1,CG} + i_{2,CG} + i_{3,CG} + \dots \\ &= g_{1,CG} V_{gs} + g_{2,CG} V_{gs}^2 + g_{3,CG} V_{gs}^3 + \dots \\ &= (g_{1N} + g_{1P}) V_{gs} + (g_{2N} - g_{2P}) V_{gs}^2 + (g_{3N} + g_{3P}) V_{gs}^3 + \dots \end{aligned} \tag{3.16}$$

where $g_{1,CG} = g_{1,N} + g_{1,P}$, $g_{2,CG} = g_{2,CG} - g_{2,P}$, $g_{3,CG} = g_{3,N} + g_{3,P}$ and $i_{j,CG}$ is the jth harmonic current in CG stage and the subscripts N and P corresponds to NMOS and PMOS respectively. From Eq. 3.16, it can be inferred that a PMOS-NMOS combination reduces the even order distortion coefficients. This can be seen from the PMOS-NMOS characterization as shown in Fig. 3.6, Fig. 3.7 and Fig. 3.8.

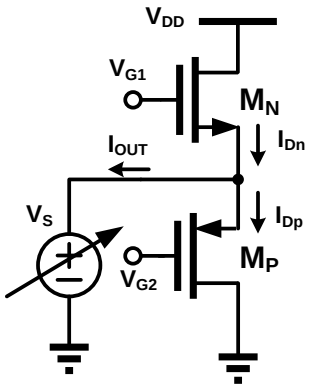


Figure 3.6: Characterization setup for stacked PMOS-NMOS pair

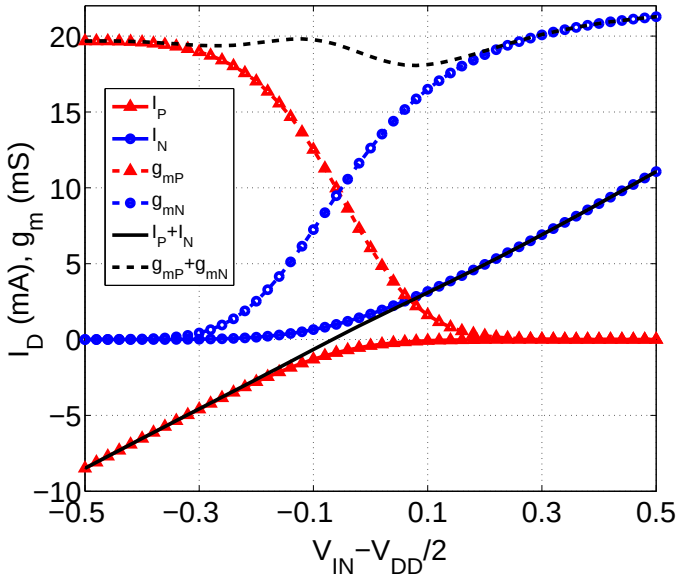


Figure 3.7: Current and transconductance of class AB push-pull input stage

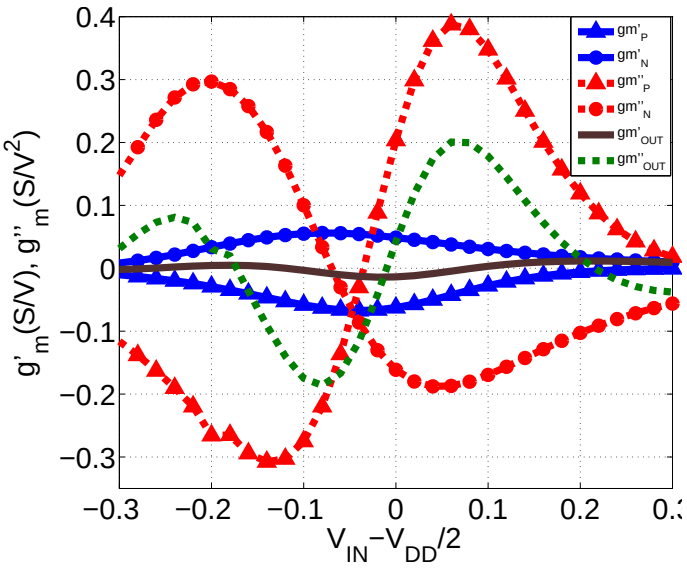


Figure 3.8: Derivatives of g_m in PMOS-NMOS input pair

Fig. 3.6 shows the characterization setup for the input CG stage. The current and g_m of the individual transistors and their combination is shown in Fig. 3.7. It can be seen that the combined $g_{m,OUT}$=$g_{m,N}$+$g_{m,P}$ is more linear than the individual g_m's. Fig. 3.8 shows the derivative curves and 2nd order distortion reduction.

LNTA output current will have 3rd order nonlinearity due to the 3rd order distortion in CG stage, CS stage and 2nd order interaction between these two stages. Total differential 3rd order nonlinear current ($i_{3,LNTA}$) in the LNTA output current $I_{out} = (I_{outp} - I_{outn})$ is given by

$$i_{3,LNTA} = 2[(-\frac{i_{3,CG}}{2} + \frac{i_{3,CG}R_s}{2}\frac{g_{1,CS}}{n+1}) \tag{3.17}$$

$$+ \frac{g_{3,CS}v_{gs}^3(3\omega)n}{n+1} + g_{2,CS}V_{x,CG}(2\omega)\frac{V_{gs}(\omega)n}{n+1}] \tag{3.18}$$

$$V_{x,CG}(2\omega) = \frac{i_{2,CG}R_s}{2} = \frac{g_{2,CG}}{2}V_{gs}^2(2\omega) \tag{3.19}$$

$v_{x,CG}(2\omega)$ is the 2nd order distortion due to $g_{2,CG}$ at node v_x. From Eq. 3.18 three major sources of 3rd order nonlinearity in the LNTA are (a) 3rd order distortion in input CG stage, ($g_{3,CG}$) given by the first term, (b) 3rd order distortion in the CS stage, ($g_{3,CS}$) given by the 2nd term and (c) 2nd order interaction of CG and CS stages ($g_{2,CG}$,$g_{2,CS}$) given by the last term. IM3 due to 3rd order nonlinearity in the CG stage $g_{3,CG}$ gets canceled in a similar way as the noise (treating i_n as nonlinear current in Fig. 3.3) and becomes negligible in Eq. 3.18. 3rd order distortion of the CS stage limits the performance of the LNTA. Due to the horizontal and vertical electric fields, the mobility of carriers in a MOSFET degrades resulting in nonlinear current [33]. From the Taylor series expansion of g_m, the low frequency expression for third-order distortion coefficient of a single transistor is given by

$$g_3 = \frac{g_m''}{3!} = -\frac{\theta}{(1+\theta V_{DSAT})^4} \tag{3.20}$$

where, $V_{dsat} = V_{gs} - V_{th}$ and θ is the channel mobility degradation factor. Eq. 3.20 assumes mobility degradation is dominated by vertical electric field. Higher V_{DSAT}s with maximum voltage head room are employed in the CS transistors of the EA. 85% of the total power is consumed in the EA to decrease its noise and improve its linearity. V_{DS} for the CS transistors is also high ensuring the nonlinearity from the output conductance (g_{ds}) negligible.

2nd order interaction of the CG and CS stages also results in IM3. Fundamental and the IM2 (due to $g_{2,CG}$)produced by the input CG stage experience 2nd order distortion of the CS stage $g_{2,CS}$ and results in IM3 products [22]. This is alleviated by reducing the g_2 of both CG stage. As mentioned in [22,34] and also observed from Eq. 3.16, a PMOS-NMOS pair in inverter configuration has inherent g_2 cancellation, that reduces the 2nd order distortion. In fact this pair reduces all the even order

distortion coefficients.

3.4.4.1. Large signal linearity

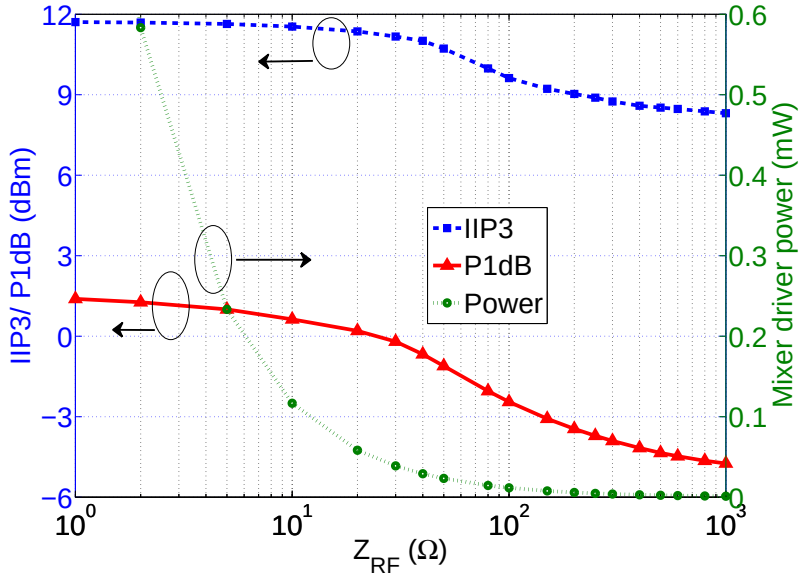


Figure 3.9: IIP_3, P_{1dB} and power consumption in switch drivers versus the load impedance

Stacked PMOS/NMOS input CG stage has wide signal operation capability [30]. Performance of this stage is boosted by employing the noise/distortion cancellation technique [12] by an error amplifier. The employed error amplifier also utilizes the stacked PMOS/NMOS. Thus voltage headroom limit on the P_{1dB} is relaxed by maximizing the supply voltage on the stacked PMOS-NMOS while meeting the reliability standards [15]. Thus, the proposed architecture inherently achieves high large signal linearity. Current re-use in this stacked PMOS-NMOS stages also reduces power consumption. Higher supply voltage is unavoidable for large signal operation.

A simulation showing the dependency of P_{1dB}, IIP_3 and power consumption on the load impedance (Z_{RF}) of the LNTA is shown in Fig. 3.9. As the output impedance (Z_{RF}) increases, output voltage signal swing increases, increasing the output nonlinearities. It can be seen from the figure that the IIP_3 and P_{1dB} decrease with the increase in Z_{RF}. Beyond 30Ω, the output nonlinearities dominate the distortion products and thus degrade the LNTA linearity. For the current mode architectures, the load impedance (Z_{RF}) can be as small as 5Ω, achieving large IIP_3 and P_{1dB}. Even with Z_{RF} as high as 30Ω, the proposed architecture can easily achieve more than 0dBm of P_{1dB} and 18dBm of IIP_3.

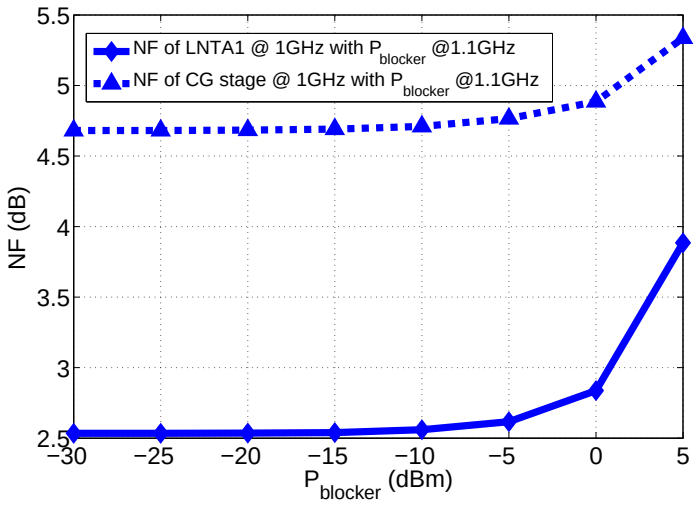


Figure 3.10: Simulation result showing the effect of nonlinearities on the noise floor in presence of a large blocker

Z_{RF} for the targeted receiver architecture comprises of the ON resistance of the passive mixer switch (R_{ON}) in series with the up-converted TIA input impedance. Assuming the major contributor for Z_{RF} is the R_{ON}, the amount of power consumed

by the driver (P_{dr}) driving the passive mixer with ON resistance R_{ON} is given by

$$R_{ON} = \frac{2L}{\mu C_{ox} W (V_{DD} - V_{th})} \tag{3.21}$$

$$P_{dr} = 4WLC_{ox}V_{DD}^2 f \tag{3.22}$$

Switch size increases to decrease R_{ON}. Thus P_{dr} increases to drive larger switch with lower R_{ON} [10] which can be seen in Fig. 8. Besides, to have low base-band impedance ($Z_{BB}(s) \approx \frac{1}{G_{m,TIA}}$, see Fig. 1), more power is needed to have high G_m in the TIA.

Fig. 3.10 displays the effect of nonlinearities on the noise floor in presence of a large blocker for the proposed LNTA. Using a PSS simulation, the noise is measured at 1 GHz in presence of a large blocker at 1.1GHz. The load impedance, Z_{RF} of 30Ω is used in this simulation. The reduced output impedance of the PMOS/NMOS transistors when forced into triode region also increases the noise contribution of the resistors (R_1, R_2). Due to the nonlinearity in the system, the large blocker up-converts some of the low frequency noise to the signal band [30]. The system gets more nonlinear with large signal swings and thus the NF increases with blocker power. This dynamic simulation also confirms the large signal capability of the LNTA with NF<3dB with blocker power of 0dBm. Beyond 0dBm, the NF increases rapidly as can be seen from the figure. The difference in the NF of the input CG stage without the CS stage and the LNTA is due to the noise canceling.

3.4.5. Stability and high supply voltage reliability

Given the multiple cross-connections in the circuit, the LNTA stability is investigated by means of stability factor (K) and Δ, which indicates unconditional stability

if $|\Delta| < 1$and $K > 1$ for all frequencies [35].

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.23}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.24}$$

Fig. 3.11. Show the values of K and Δ of the LNTA. Minimum value of $k = 2.86$ is found at low frequencies but increases with frequency, while the peak value of Δ is less than 0.3.

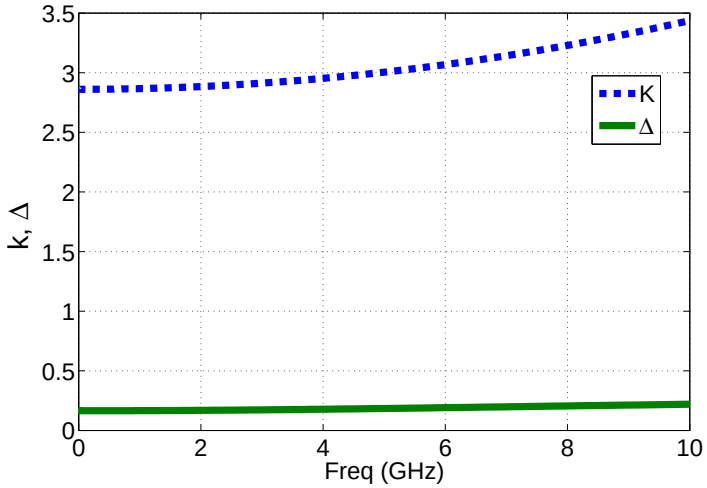


Figure 3.11: Stability factors (K, Δ) versus the frequency

Targeting large linearity figures makes the use of higher supply voltages unavoidable [25]. Standard supply voltage for the employed 45nm technology is 1.1V. But in this design in-order to have sufficient headroom, supply voltage of 2.2V was used. This would make sure that the voltage compression happens after the current (g_m) compression. But proper precautions have to be taken to ensure reliability and life

time. Terminal to terminal voltages should not exceed the reliability limits either during start-up or normal operation. In Fig. 3.5, the common source node of the CS transistors is a near virtual AC ground with DC voltage of $V_{DD}/2(=1.1V)$. Thus each CS transistors works under a DC supply voltage of $V_{DD}/2$. For the CG transistors, the signal swing (polarity) at the drain follows that of the source terminal. So the V_{DS} do not go beyond the rated voltage. The signal swings are within the breakdown voltages of the active junctions of the transistors during the normal operation. So every transistor is oblivious to the increase in the supply voltage. Although a startup circuit is not explicitly implemented in the current design, a start-up circuit similar to the one proposed in [25] can be used to give more reliability during the startup.

3.4.6. Circuit implementation and statistical behavior

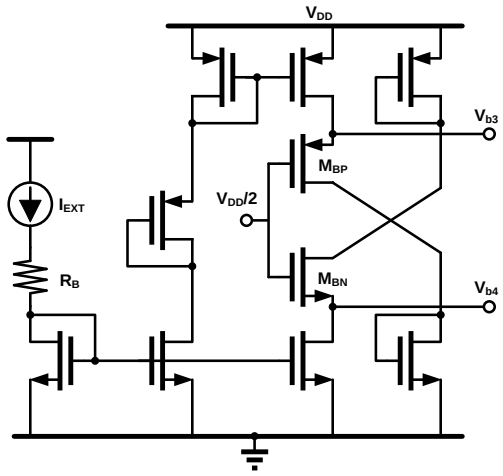


Figure 3.12: Bias circuit for CG and CS transistors

To have a better NF at a moderate power consumption according to the section refsec:IInoise, n=5 was chosen in this design. CG transistors consume 1.0 mA

and sets the $g_{mCG} = 20mS$ for input matching. CS transistors consume 5.71mA to achieve a NF of 2.5dB. V_{DSAT} of CS transistors is 145 mV to have less 3^{rd} order distortion according to Eq. 3.20 Proper ratio-metric design and symmetric layout procedure was followed to get the proper noise/distortion cancellation. Replica biasing is also used to bias the CG and CS transistors to give robustness to cancellation over P.V.T. variations. Bias circuit as shown in Fig. 3.12 is employed to bias the stacked PMOS-NMOS in input CG stage. Voltage $V_{DD}/2$, obtained through a resistive divider is applied to the gates of M_{BP} and M_{BN} sets the voltage at V_x in Fig. 3.5 to be around $V_{DD}/2$. Scaled version of the similar bias circuit is employed to bias the CS transistors.

Table 3.1: 400 Runs monte-carlo statistical distributions

	I_{DC}(A)	G_m(dB)	NF_{min}(dB)	S_{11}(dB)	IIP_3(dBm)	P_{1dB}(dBm)
μ	13.78m	38.42	2.56	-17.91	19.05	-0.31
σ	105.1u	0.37	14.53m	93.53m	0.1	0.124

The robustness of the design to the PVT variations is investigated through Monte Carlo analysis. Over 400 runs, both process variations and in-wafer device mismatches were considered. PVT variations are simulated on all LNTA components. Mean (μ) and standard deviation (σ) of the LNTA metrics are given in Table 3.1. Data in this table is taken at 1 GHz frequency for the LNTA1. It can be noticed that is small for most of the parameters owing to the ratio metric design, replica biasing and symmetric layout. Correlation factor of 0.9 is used for the resistors (R_1 and R_2) in the Monte-Carlo simulation pertaining to the symmetric layout.

3.4.7. Bulk driven LNTA

Due to the use of higher supply voltage, the associated power consumption in the LNTA is moderately high even though P_{1dB} of 0dBm is achieved. To this end, a low power technique using bulk driven circuits [36] is used. As the employed technology is a triple well process, a low power bulk driven LNTA as shown in Fig. 3.13 is also designed that gives comparable performance at lower power. For this circuit, EA transistor sizes and currents are scaled down to maintain the value of the original g_{mCS}. The bulk driven g_m boosting technique improves the power savings by 47% compared with the previous design. Although g_{mb} is small in scaled technology, (only 10% of main g_m in 45nm), effective G_{mb} is twice the actual g_{mb} as the signal driving the bulk is amplified (x2) by g_{mCS} and R_1.

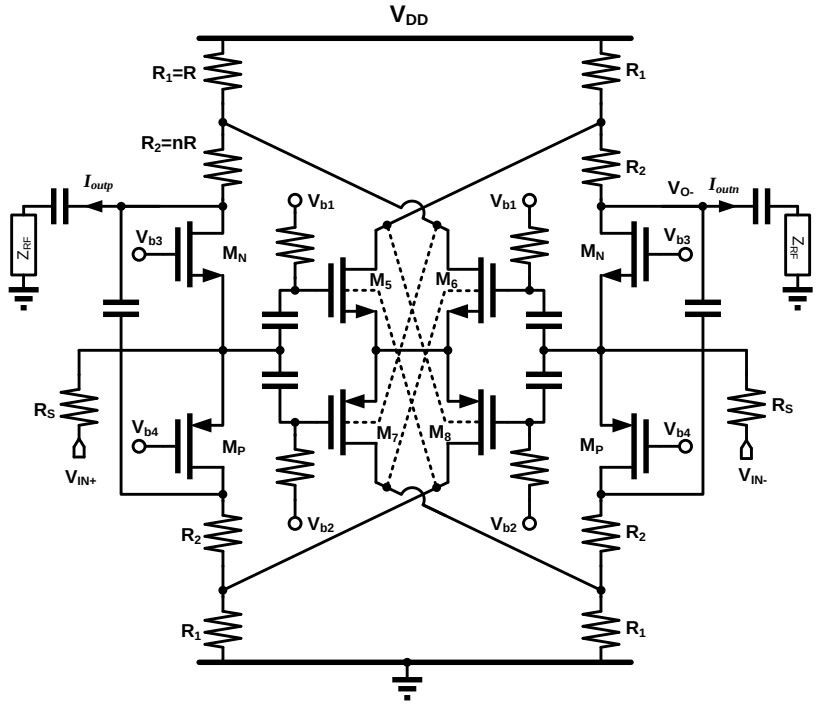


Figure 3.13: Low power buk driven LNTA

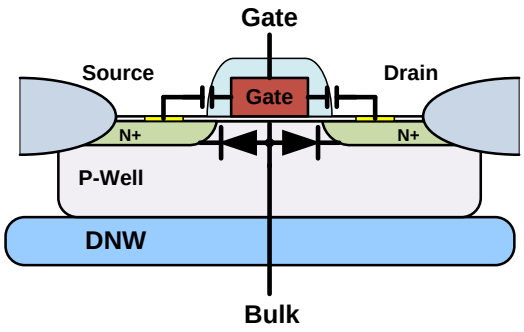


Figure 3.14: Reliability of junctions in bulk driven LNTA, bulk-source & bulk-drain diodes

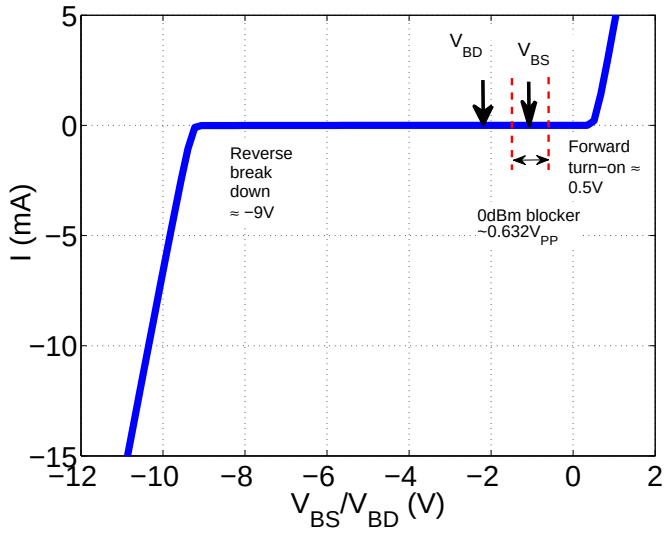


Figure 3.15: Reliability of bulk driven LNTA at 0dBm blocker, bias point of the diodes and voltages across the diodes for 0dBm input blocker

Reliability has to be ensured as signal is injected into the bulk. For NMOS transistors as shown in Fig. 3.14, the bulk (P-well) is more negatively biased than

its source and drain. From Fig. 3.13, it can be noticed that for transistor M_5 and M_6 the voltage difference between the source and bulk terminals is less than zero. So the diodes never turn on even for 0dBm signal as the V_{BS} is negative and large. The drain terminal is more positively biased than the source terminal. Bulk-drain diode is more negatively biased than the bulk-source diode, so this diode also does not turn on. Fig. 3.15 shows the operating regions of the diodes (bulk-drain, bulk-source) of a NMOS transistor (M_5 or M_6). As the bulk is more negative biased than the source and drain, the diodes never turn on even with moderately large signal. On the other side, the diodes the break down voltage is around -9V which is very high compared to the voltage signals associated with a 0dBm signal. Similarly PMOS bulks are connected to achieve high reliability.

3.5. Test Chip and Measurement Results

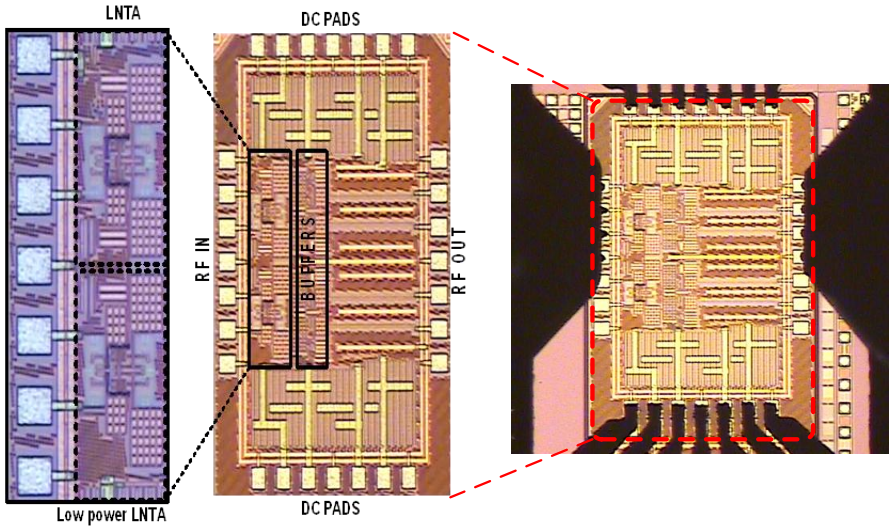


Figure 3.16: Micro-photographs of the proposed LNTA prototypes on 45nm CMOS occupying 0.06mm^2 each

The wideband LNTAs were fabricated in a 45nm technology and occupy an active area of 0.06mm^2 each. The chips were measured by on-wafer probing. Fig. 3.16 shows the chip micro photograph of both LNTAs. No RF specific process options like MIM capacitor or thick metals were used. For test purposes, the LNTA is loaded with an on-chip output buffer which uses a dedicated power supply. It isolates the LNTA output from the testing equipment.

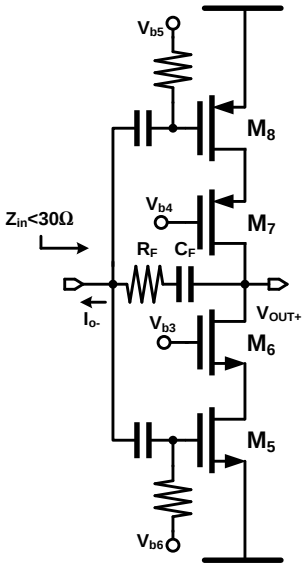


Figure 3.17: Programmable output buffer for measurements

Fig. 3.17 shows the output buffer employed in both LNTAs. The output buffer is a resistive feedback amplifier with programmable gain. The simulated buffer bandwidth is greater than 8 GHz; S_{21} is programmable in the 6-14dB range, and S_{22} < -10dB. The buffer operates in two gain modes to facilitate the measurement of NF and linearity more accurately. The high gain mode is used to measure NF while the low gain mode is used to measure linearity. $Z_{IN} \approx 30\Omega$ and S_{22} <-10dB are main-

tained in the buffer for both modes. The buffer was added for testing purposes only and its performance was de-embedded for reporting the final measurements. 4-port VNA was employed to measure the input matching and gain of the differential circuits providing true differential-mode S-parameters.

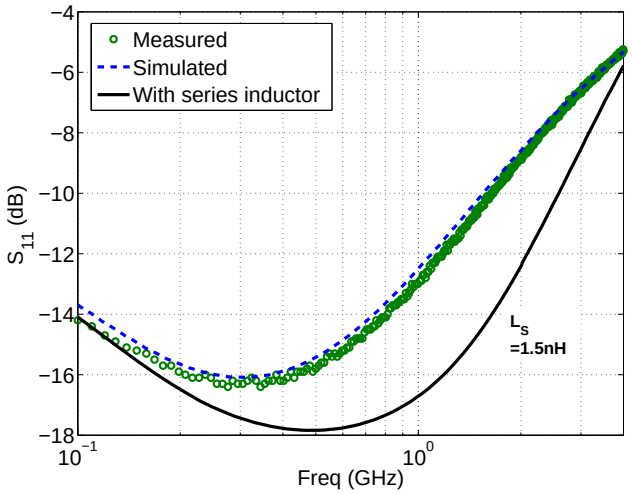


Figure 3.18: Simulated and measured input impedance matching (S_{11}) of LNTA1

Fig. 3.18 shows the input matching (S_{11}) of LNTA1. The impedance matching is better than -10dB up to 1.5GHz. It can be noticed that the measurement result is very close to the post layout simulations result with layout parasitics. An input bond wire inductance would improve the matching by resonating out the input parasitic capacitance. A simulation showing this improvement in matching and bandwidth extension with a series inductance of $L_S = 1.5$nH is also shown in the figure.

Transconductance gain (g_m) is measured from the Y parameters as given by Eq.

3.25

$$g_m = Real\{Y_{21}\}$$
$$g_m = Real\{\frac{-2S_{21}/Z_0}{(1+S_{11})(1+S_{22}) - S_{21}S_{12}}\} \tag{3.25}$$

where Z_0 is the characteristic impedance (= 100Ω differential) and S_{XY} are the measured differential S-parameters. Measured g_m is shown in Fig. 3.19. The small signal g_m variation is within 10% in the entire 0.2-2GHz bandwidth. Measured result is slightly less than the post layout simulation due to the increase in parasitics at the output.

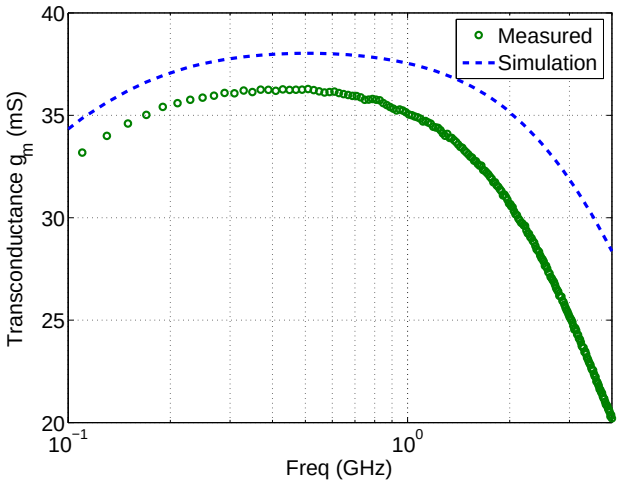


Figure 3.19: Simulated and measured transconductance gain (G_m) of LNTA1

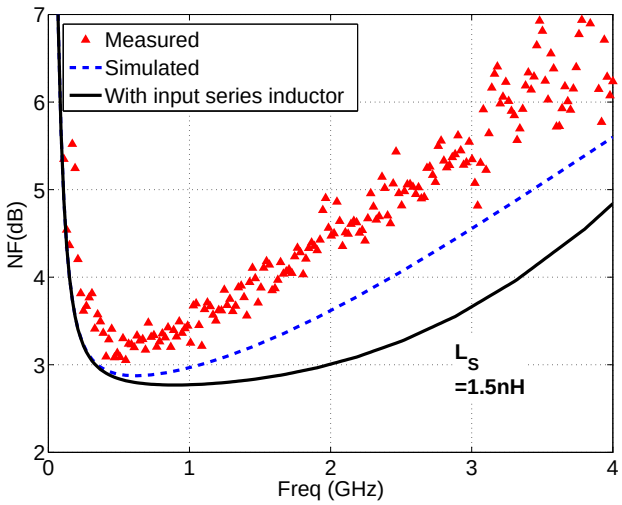


Figure 3.20: Simulated and measured noise figure for LNTA1.

Noise and linearity measurements require an extra off-chip passive baluns for single-to-differential conversions. NF was measured with the buffer in high gain mode. Two external baluns at the input and output were employed and NF was measured using a noise meter. High gain is required for good accuracy of the NF measurement. High gain in the DUT will reduce the influence of any external noise sources at the output. The measured noise figure is less than 4.6dB in the 0.2-2GHz range and is shown in Fig. 3.20. Simulations showed that a series inductance (bond wire inductance) of 1.5nH (Q≈15) would further extend the bandwidth and improve the NF by 0.6dB at 2GHz. Low frequency NF degradation is attributed to the off-chip baluns with lower cut-off frequency of around 500MHz. The increase in the measured NF from the simulated is due to the decrease in the measured gain (g_m).

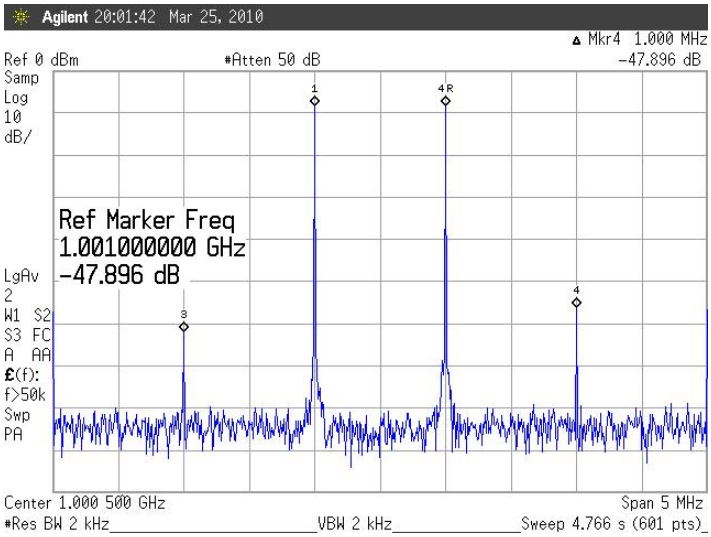


Figure 3.21: Measured IM3 of 47.9dB from a two tone test of LNTA1 with input power of -15dBm each at 1GHz and 1MHz spacing

Linearity is characterized by two tone test. To characterize the worst case non-linearity, OOB load impedance of $Z_{RF} = 30\Omega$ is used at the output for the linearity measurements. The result of a two tone test is shown in Fig. 3.21. For the two test tones at 1 GHz with 1 MHz spacing and a total -12dBm input power (-15dBm each), the IM3 is found to be under 47dBm. A complete IIP_3 characterization curve for the LNTA1 is depicted in Fig. 3.22. For most of the existing linearized LNTAs in the literature [22], the 3^{rd} -order distortion quickly increases at moderately high power. But in this implementation, this effect is not seen (see Fig. 3.22). This is due to the targeted receiver architecture (less output nonlinearities) and inherent large signal capability of the LNTA.

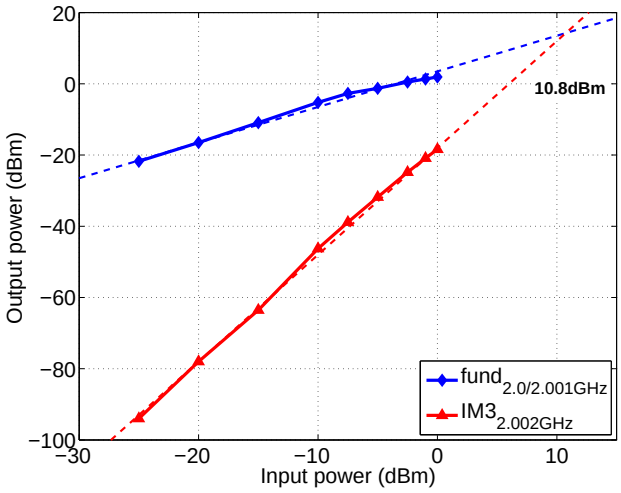


Figure 3.22: IIP_3 characterization for LNTA1 showing IIP_3 of 10.8dBm

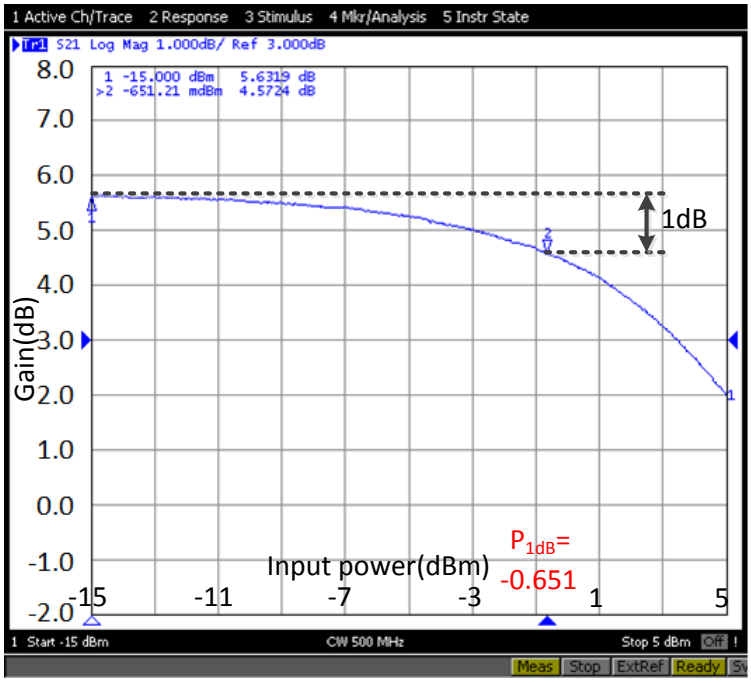


Figure 3.23: 1dB compression point of LNTA1 with output buffer in low gain mode

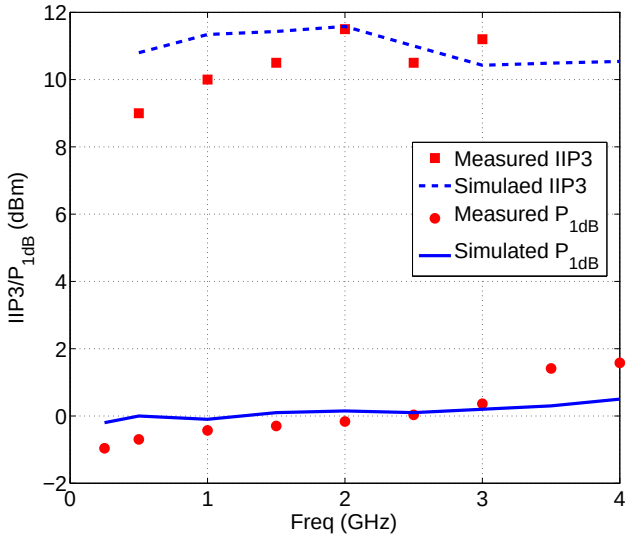


Figure 3.24: Measured IIP_3 and P_{1dB} at different frequency inputs

Large signal linearity characterization is done both by employing VNA and a power meter. For this measurement the output buffer is put in low gain mode with input impedance 30Ω. Fig. 3.23 shows the P_{1dB} measurement of the LNTA1 from VNA. The input power at 1.5GHz is swept on the X-axis and the power gain drops by 1dB when Pin ≈ -0.6dBm. For accurate measurements, another set of P_{1dB} measurements using power meter were also recorded giving P_{1dB} of 0dBm. Remarkable large signal linearity is demonstrated by the P_{1dB} measurement over 0dBm. The linearity measurements are taken at various frequency points and the high linearity is consistently achieved at all the in-band frequencies as shown in Fig. 3.24. Higher linearity figures can be achieved for $Z_{RF} < 30\Omega$ at the load as shown by the simulation in Fig. 3.9.

The experimental results for the g_m-boosted LNTA are depicted in Fig. 3.25 and Fig. 3.26. Similar performances were obtained: S_{11} less than -10dB up to 2.4GHz,

overall g_m is approximately 33mS. NF is under 5dB up to 3GHz, while the $P_{1dB}$is 0dBm. Table 3.2 summarizes the most relevant Inductor-less Wide-band LNAs targeting high linearity. Dominant pole is located at the input. That is why even when the bulk with large parasitic capacitor is connected at the output, the bandwidth did not decrease. Besides in low power bulk driven prototype, the CS transistors are scaled down to have the same G_m at reduced power consumption. This scaling also reduced the parasitic capacitance from the transistors.

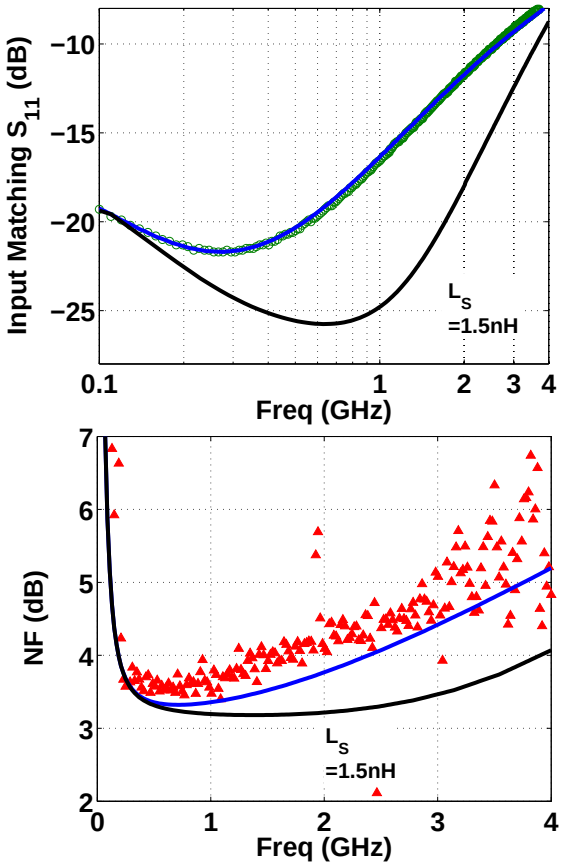


Figure 3.25: Measured S_{11} and NF of low power bulk driven LNTA (lines: simulations; markers: measurements; L_s=series inductance of 1.5nH at the input)

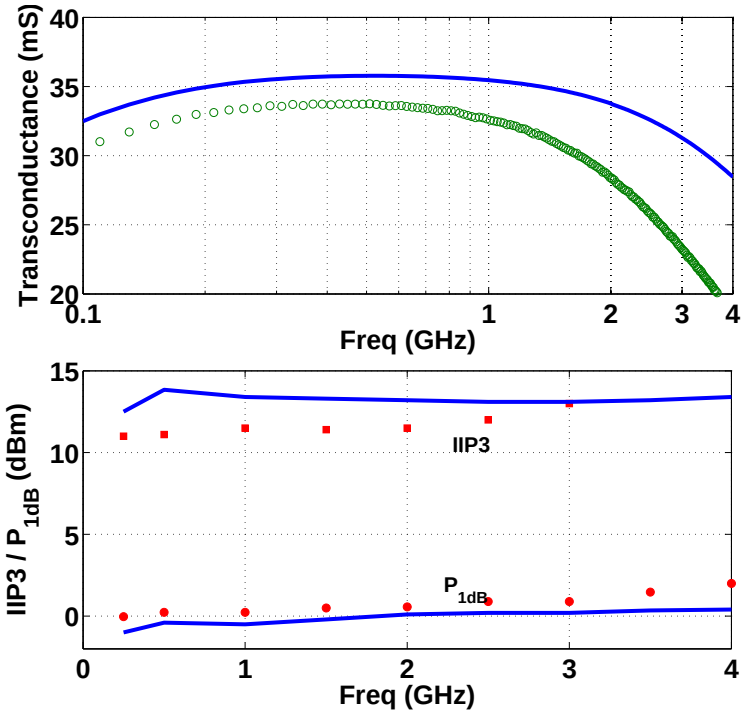


Figure 3.26: Measured g_m and linearity of low power bulk driven LNTA (lines: simulations; markers: measurements; L_s=series inductance of 1.5nH at the input)

Table 3.2 shows the performance comparison of the LNTAs with the latest state of the art. It can be noticed that the linearity of the proposed LNTA and low power bulk-driven LNTAs (LP LNTA) are very good.

Table 3.2: Performance comparison of the proposed LNAs with the recently published linear LNAs

parameter	[22]	[37]	[23]	[38]	[39]	[40]	[41]	LNTA	LP LNTA
Tech..(nm)	130	180	45	130	90	90	130	45	45
Freq(GHz)	0.8-2.1	1-3	0.6-10	0.1-2.7	6	0.4-3	0.1-0.93	0.1-2	0.1-3
S_{11}(dB)	<-8.5	<-9	-	<-10	-	<-10	<-10	<-9	<-9
Gain(dB)	14.5^{ϕ}	16.9	10	20	16.5	15	13	-1.7^{ψ}	-1.65^{ψ}
g_m(mS)	NA	NA	NA	NA	NA	NA	NA	36.5	34.5
NF_{min}(dB)	2.6	2.6	3	4.0^{η}	2.5	2.3	4	3	3.4
IIP_3(dBm)	16	-0.7	6	-12	-10	5	-10.2	10.8^{ψ}	12^{ψ}
P_{1dB}(dBm)	-11^{θ}	-11^{θ}	-	-21	-	-10	-18	0^{ψ}	0.4^{ψ}
Supply(V)	1.5	1.8	-	1.2	-	2	1.2	2.2	2.2
Power(mW)	17.4	12.6	30^{φ}	1.32	9.2	0.72	-	30.2^{δ}	16^{δ}
Active Area(mm^2)	0.099	$0.073^{\star}$	-	0.007	0.0017	-	0.27	0.06	0.06

$^{\phi}$ Internal gain

$^{\psi}$ With $R_L = 30\Omega$

$^{\eta}$ NF is shown in the 1.6GHz to 2.6GHz frequency band

$^{\theta}$ graphically estimated

$^{\varphi}$ includes the power of the V-to-I converter

* active area

$^{\delta}$ LNTA Core power

3.6. Summary

The proposed LNTA architectures drastically reduce the noise/distortion contribution of the amplifier input stage to achieve remarkable linearity with low power consumption by employing current-reuse and push-pull class AB The proposed LNTA

architectures drastically reduce the noise/distortion contribution of the amplifier input stage to achieve remarkable linearity by employing current-reuse and push-pull class AB biasing while maintaining equal output impedances for the next stage in the receiver chain. The proposed architectures achieve P_{1dB} over 0dBm within the entire 0.2-2GHz frequency band. Since the LNTA output is current, these architectures can be easily coupled to both passive mixers and Gilbert cells.

4. DESIGN TECHNIQUES TO IMPROVE BLOCKER TOLERANCE OF CONTINUOUS-TIME ΔΣ ADCs*

4.1. Introduction

Recent developments in mobile computing and wireless INTERNET have led to exponential growth in demand for efficient portable computers and smart phones. The low-cost, low-power digital computing required by these gadgets is facilitated by process scaling and is expected to continue to 10.8 nm physical gate length by 2020 [42]. Broadband systems require high-resolution analog-to-digital conversion solutions, especially when weak target signals are hidden within a background of strong blockers/jammers. The very soft filtering (one-pole or two-pole roll-off) in front of the ADC and the huge out-of-band (OOB) power of high frequency blockers demand a highly linear RF front-end circuitry [3, 43] and a very high resolution ADC [44, 45]. This fact by itself requires increasing the ADC resolution over the required in-band signal dynamic range.

The most popular approach in radio receiver design is to remove the expensive baseband filter before the ADC and perform most of the signal processing in the digital domain [46–48]. This approach becomes ever more effective as process technologies scale but at the same time places ever higher dynamic range demands on the ADC. However, strong OOB blockers may occupy most of the ADC dynamic range if pre-filtering is removed. The blockers degrade the in-band signal-to-noise ratio (SNR) and may destabilize the ΔΣ loop by overloading it with an additional penalty of long recovery time [49].

*Part of this chapter is reprinted with permission from "A Wideband low-power continuous-time ΔΣ modulator for next generation wireless applications," by X. Chen, Ph.D. dissertation, Oregon State Univ., Corvallis, Oregon, Copyright 2007 by Xuefeng Chen.

To improve the immunity to blockers, a CT $\Delta\Sigma$ with a high-pass filter (HPF) in the feedback and a counter low-pass filter (LPF) in the feed-forward path is suggested in [50]. LPF helps to filter out the input blockers and these additional filters barely increase the total power consumption. However, this architecture demands stringent matching requirements on the two filters for stability when designed for high frequency operation; noise and linearity issues arise since these additional blocks are placed at the input of the modulator. In [51] a low-pass signal transfer function (STF) is achieved by employing dual feed-back. However, the complexity and the mismatch variation in the coefficient cancellation increase with the order of the system; higher bandwidths are required for the amplifiers in the loop filter.

Solutions reported in [44, 48] and [49] propose reconfigurable $\Delta\Sigma$ architectures which dynamically change the STF roll-off for power savings depending on the blockers at the input. In [48] blocker power is estimated by a 5-bit flash ADC at the modulator input and digital signal processing (DSP). Latency in DSP processing could result in system instability when strong blockers are present at the ADC input. In [44], [49] overload is detected by monitoring an internal node of the ADC, however the loop order change is done by modifying the loop parameters, whose time constants are large, making this approach not very practical for wireless applications.

In this work, a 5^{th} order CT $\Delta\Sigma$-Modulator with a feed-forward loop architecture is employed as a test bed to demonstrate the effectiveness of the proposed blocker sensitivity reduction techniques. This architecture is low power and area efficient but inherently has signal transfer function (STF) peaking at various nodes and only 1st order STF roll-off outside the signal band. Through the use of an integrated, minimally-invasive LPF in conjunction with a blocker detection/attenuation technique, robustness against loop saturation due to blockers is achieved. The power and noise overhead of these techniques are within 6% and 17% of the total ADC

budget, respectively. This chapter is organized as follows. Section 4.2 discusses the sensitivity of CT-ΔΣ ADCs to blockers, jitter as well as their effects on system performance. Section 4.3 introduces the proposed blocker tolerant architecture, while section 4.4 discusses the circuit implementation of relevant ADC sub-blocks. Experimental details are discussed in section 4.5 and conclusions are drawn in section 4.6.

4.2. Sensitivity of ΔΣ ADC to Blockers and Jitter

4.2.1. System architecture

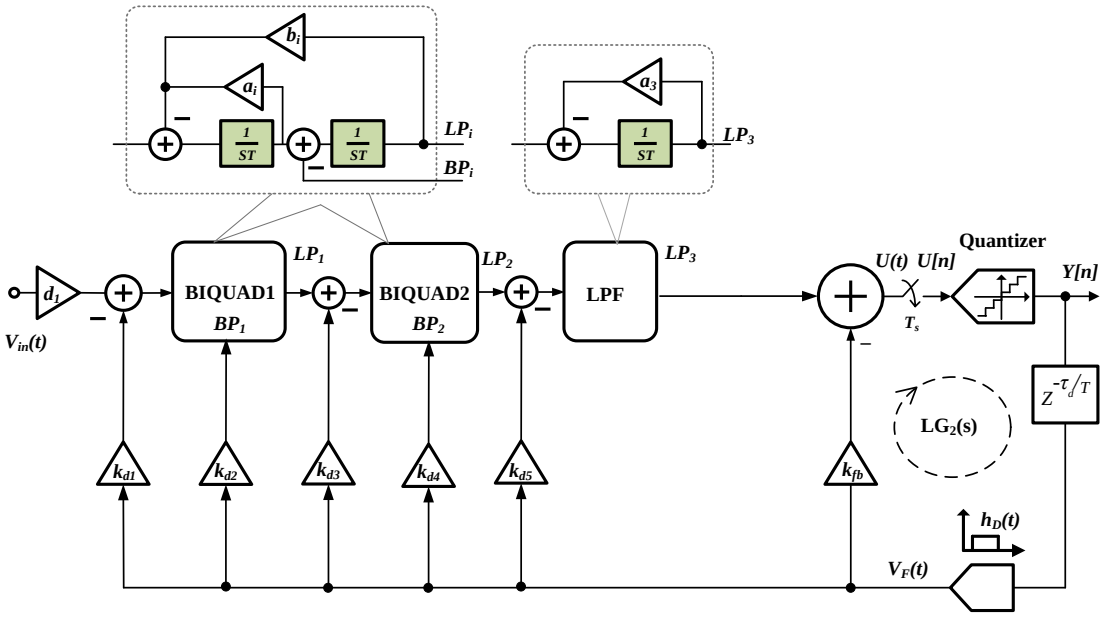


Figure 4.1: 5^{th}-order CTΔΣ ADC with feed-back architecture

The target CT-ΔΣ modulator can be realized by using either feedback (CIFB) [52] or feed-forward (CIFF) [53] topologies. Fig. 4.1 shows the ADC in CIFB architecture. In a CIFB topology, each integrator output has a significant amount of input

signal. To avoid voltage clipping, lower integrator coefficients have to be used, which translates to larger capacitors. Hence, the first stage can have only a moderate gain which requires higher bias currents in the later stages so as to reduce their input-referred noise. A major advantage of CIFB architecture is that the N^{th} order feedback compensated loop filter provides N^{th} order attenuation to high frequency blockers [54].

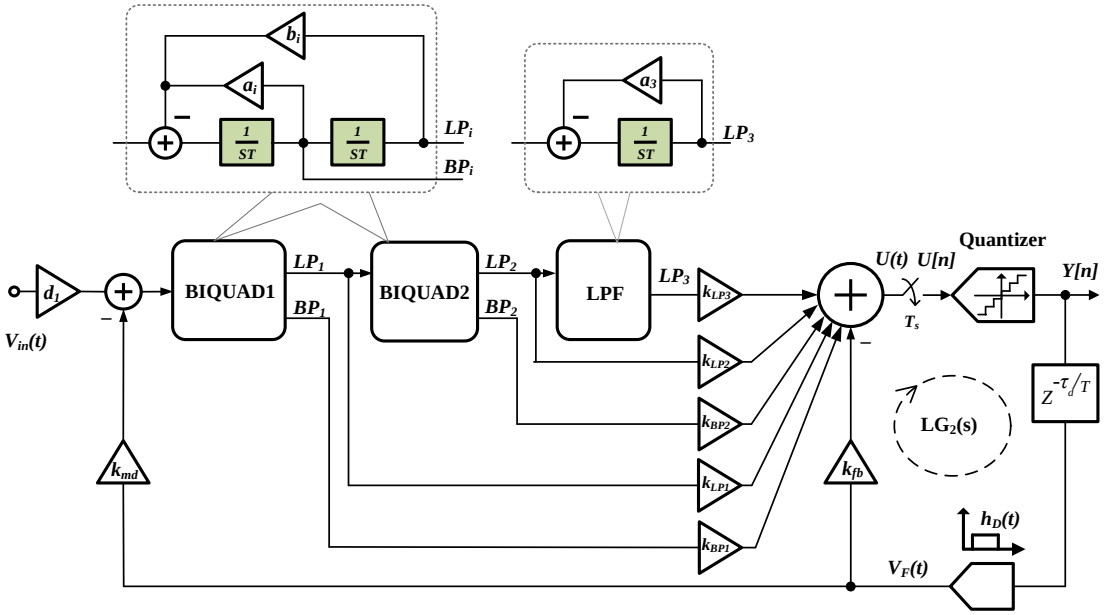


Figure 4.2: 5^{th}-order CT$\Delta\Sigma$ ADC with feed-forward architecture

CIFF has the advantages of being low power, less complex and dynamically more stable than CIFB architecture [51,55,56]. We choose CIFF architecture as a test bed to evaluate the proposed blocker reduction techniques due to its highest sensitivity to peaking effects due to blockers. However, the proposed blocker reduction techniques

can also be extended to CIFB architecture to further improve its blocker tolerance. The CIFF architecture employed in this design is shown in Fig. 4.2. A zero order loop (LG_2) around the quantizer is realized using another feed-back DAC (K_{fb}) to make the architecture less sensitive to filter's excess loop delay (ELD) [52].

4.2.2. Signal transfer function and loop filter

For this system, $LF(s)$ is defined as the open loop transfer function from DAC output, $V_F(t)$ to the sampler input, $U(t)$. Similarly, $FF(s)$ is the open loop transfer function from modulator input, $V_{in}(t)$ to $U(t)$. Then the loop gain (LG) for the system is given by

$$LG(s) = LF(s)H_D(s)sinc(\frac{\omega T_s}{2})e^{-j\omega T_s} \tag{4.1}$$

where H_D(s) denotes the Laplace transform of the DAC output waveform and T_s is the loop delay which is set to one clock period in this design. The sinc(x) function is a result of the first order sample and hold inherently present at the quantizer input. The Noise transfer function (NTF) and STF are given by

$$NTF(s) = \frac{1}{1 - LG(j\omega)} \tag{4.2}$$

$$STF(s) = \frac{FF(j\omega)}{1 - LG(j\omega)} = FF(j\omega)NTF(j\omega) \tag{4.3}$$

The design issues arise when considering the peaking effects at various filter nodes. Let us consider the case of a 5^{th} order $\Delta\Sigma$ modulator targeting SNDR of 74dB in a bandwidth of 20MHz, with an oversampling ratio is 12.5. Fig. 4.3 shows the relevant open and closed loop signal transfer functions in CIFF as well as the NTF. 5^{th} order NTF in Eq. 4.2 has 5 in-band zeros, 5 OOB poles with 10 dB OOB gain. The STF shows amplification for most of the OOB channels, suggesting that quantizer

saturation may happen in presence of strong blockers. Besides, having OOB peaking and 1st order OOB roll-off in the STF, CIFF architectures are susceptible to internal filter gain peaking, which may saturate the system in presence of blockers.

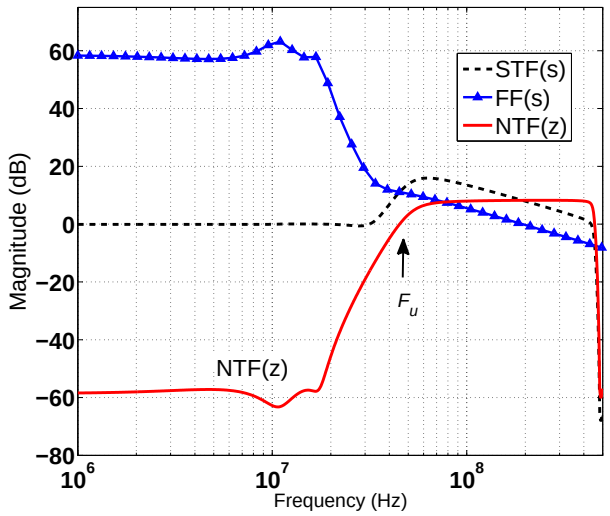


Figure 4.3: Transfer functions in feed-forward architecture

The direct trajectories from modulator input (V_{in}) to the integrator output nodes (V_{XPi}; e.g., BP1, LP1, BP2, LP2 or LP3 in Fig. 4.2) of the loop filter do not touch the loop,LG_2, hence the closed loop gain from V_{in} to V_{XPi} increase accordingly. The loop gain (LG_2) formed by fast DAC (K_{fb}) is given as

$$LG_2(s) = -K_{fb}H_D(s)e^{-j\omega T_s} \tag{4.4}$$

Closed-loop gain from V_{in} to V_{XPi} is then computed as

$$\begin{aligned} G_{XPi}(j\omega) &= FF_{XPi}(j\omega)(1 - LG_2(j\omega))NTF(j\omega) \\ &= FF_{XPi}(j\omega)(1 + KfbH_D(j\omega)e^{-j\omega T_s})NTF(j\omega) \end{aligned} \tag{4.5}$$

where $FF_{XPi}(j\omega)$ is the open-loop gain $V_{XPi}/V_{in}(j\omega)$. Low-frequency gain of the first bi-quad stage (FF_{BP1}) is 20 dB to minimize the noise contribution of subsequent stages. Since NTF positive roll-off can be as high as 30 dB/octave in a 5$^{\text{th}}$ order system and due to the high gain of the first bi-quad, the closed-loop voltage gain at the first bi-quad output (G_{BP1}) could be over 20 dB at intermediate frequencies.

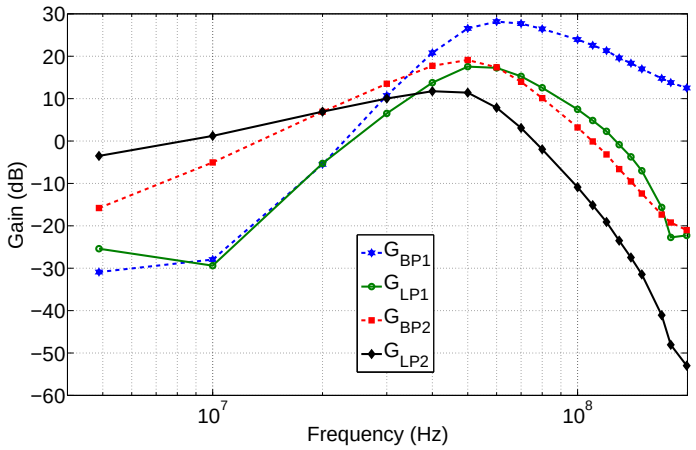


Figure 4.4: Simulation showing the closed loop AC gain from input to the internal nodes of feed-forward 5$^{\text{th}}$-order CT$\Delta\Sigma$ ADC architecture

The voltage gain, G_{XPi} at various filter nodes is plotted in Fig. 4.4. In this case,

the band-pass output of the first bi-quad (BP1) is the most critical node, but gain at most of the filter output nodes is over 10 dB for the frequency range around F_u (30 MHz to 90 MHz, see Fig. 4.3 and Fig. 4.4). Even at the corner of the system passband some nodes present gain over 6 dB. The saturation in these nodes when significant power is present in this frequency band overloads both the filter and quantizer and thus destabilizes the loop.

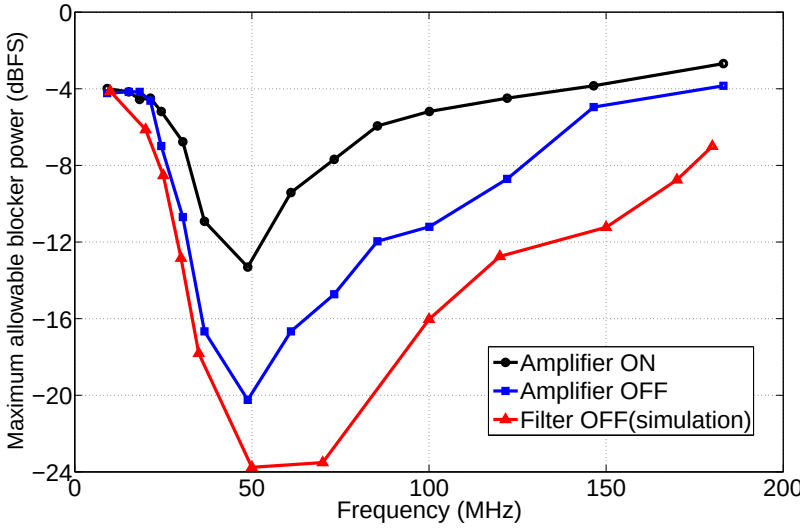


Figure 4.5: Simulation showing maximum OOB blocker tolerance with -12dBFS in-band signal at 6MHz

Fig. 4.5 displays the profile of the maximum tolerable blocker power by the ADC before being saturated in presence of -12 dBFS in-band signal. Blocker power of -23 dBFS in the range of 50-70 MHz saturates the loop and makes it unstable. We also tested the case of large blockers and small in-band signal, achieving similar results. Blockers at very high frequency are usually not a major issue due to the 1st order

filtering usually implemented in the trans-impedance amplifier. The 1st order filtering provided by the feed-forward architecture also kicks in at high frequencies. However, adjacent and alternate channel blocker requirements are usually very stringent in standards like [57].

4.2.3. Loop sensitivity to blockers

Presence of the strong blockers at the ADC input increase the signal swings in the loop overloading the filter and the quantizer resulting in an eventual unstable loop. DSP after the ADC usually detect the presence of blockers and controls the gain of the Programmable Gain Amplifier (PGA), adjusting the input signal power to fit into the ADC linear range. This correction is usually a slow process because of DFT calculations. Rapidly varying input signals can drive a modulator loop into instability even if their amplitudes are relatively small [58]. It gets worse if the analog pre-filtering is removed to filter out those OOB signals.

Fig. 4.6 shows the effect of a blocker on the loop performance. Notice that the blocker power is well below signal power but it is placed on the critical blocker frequency range, leading to loop saturation after few clock cycles. Prior to the blocker arrival, the system was operating with a -6 dBFS in-band signal then a blocker at 50 MHz frequency with -22 dBFS power appears for 100 clock periods (200 nsec) and then disappears. Though it is only present for this short period, the blocker de-stabilizes the system for more than 360 clock cycles (720 ns) which can be seen from Fig. 4.6. In this case the loop takes time to come back to linear operation after the blocker disappears. Once some of the internal nodes are saturated, the loop becomes hardly non-linear and return to steady state cannot be guaranteed. The conventional technique used to study the analysis of non-linear systems is phase portraits, where a number of simulations are run for different error and error velocity

cases. These simulations can be emulated in our case analyzing the pulse response of the modulator employing fast blockers.

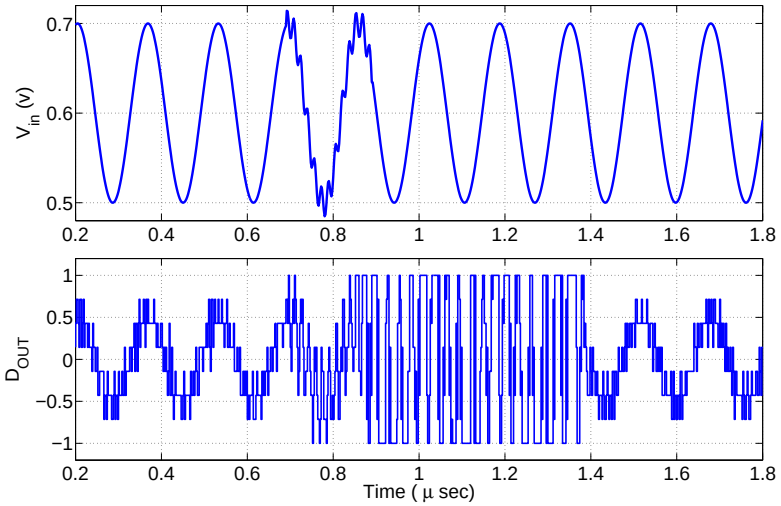


Figure 4.6: Simulation showing the presence of an agile blocker with -23dBFS at 50MHz frequency for 100 clock periods destabilizes the ADC operating with -6dBFS input signal

The amount of time the system takes to get back to linear operation depends on several factors such as order and bandwidth of the loop, initial conditions of the system, blocker power and the duration of the blocker signal. With some internal nodes being saturated, the loop becomes hardly non-linear and there is no guarantee it will be stable if the input signal is attenuated after adjusting PGA gain through the DSP. Even if the loop stability is recovered, this longer time correction through the DSP can not be tolerated in most wireless applications.

4.2.4. Sensitivity of ADC to jitter

Effect of jitter on the performance of the CT $\Delta\Sigma$ ADC is very well documented in literature [54, 59]. But in most parts of the literature discussing jitter effects on CT $\Delta\Sigma$ ADC, phase noise was conveniently considered as equally distributed over frequency. But in reality phase noise has spectral profile and increases with a slope of 3 when frequency gets closer to clock frequency (f_s) [60]. Phase noise is constant (white) only beyond a certain offset frequency. Phase noise and clock jitter are related as below [61].

$$\sigma_j^2 = \int_0^\infty S_\phi(f) \frac{sin^2(\frac{\pi f}{f_0})}{(\pi f_0)^2} \, \mathrm{d}f \tag{4.6}$$

where $S_\phi(f)$ is the power spectral density of the phase noise σ_j^2 is the RMS period jitter. Clock jitter causes random phase modulation to the output bit stream causing the OOB quantization noise to fold into the signal band raising the noise floor.

To ease the analysis of the effect of the DAC clock jitter on the CT modulator, the timing error of the DAC output signal transition edges is modeled as an equivalent error in the signal magnitude. Fig. 4.7 shows this equivalence for the NRZ DAC pulse. If the timing error of the signal transition edge between the (n-1)$^{\text{th}}$ and the n$^{\text{th}}$ clock period is Δt(n), then the equivalent magnitude error $\epsilon_j(n)$ for the n$^{\text{th}}$ DAC pulse induced by clock-jitter in a (non-return to zero) NRZ waveform is given by

$$\epsilon_j(n) = \frac{(y(n) - y(n-1))\Delta t(n)}{T_s} = \frac{dy(n)\Delta t(n)}{T_s} \tag{4.7}$$

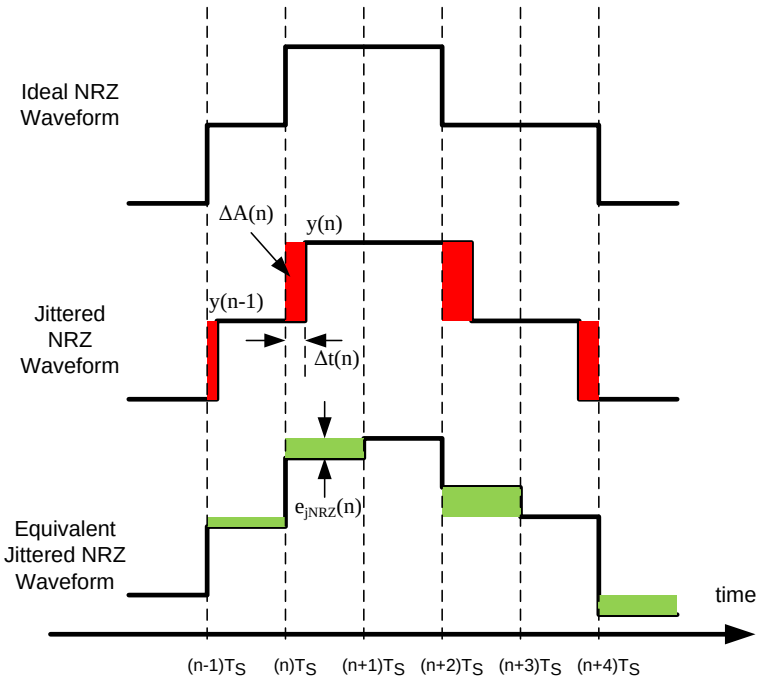


Figure 4.7: Effect of clock jitter in CT$\Delta\Sigma$ ADC with NRZ DAC in the feed-back

Modulator output $y(n)$ consists of input signals (in-band signal and OOB blockers) and quantization noise($e_q(n)$). $\Delta t(n)$ is the period jitter at sampling instant nT_s. T_s is the sampling period. The modulators output can be expressed in the time domain as

$$y(n) = v_{in}(t) * STF(t)|_{t=nT_s} + e_q(n) * NTF(n) \tag{4.8}$$

where STF and NTF stand for the signal transfer function and noise transfer function respectively. e_q stands for quantization noise. It is assumed that the modulator output y(n) and the clock jitter Δt(n) are statistically independent of each other and the clock jitter is a white noise process. The symbol '$*$' denotes convolution

operation. The differential variation of the modulator's output can be written as

$$dy(n) = du(n) + de_q(n) * ntf(n) \tag{4.9}$$

where $u(n) = v_{in}(t) * STF(t)|_{t=nT_s}$. Assuming that in-band $STF(s) = f[stf(t)]$, where f is the Fourier transform operator, is time invariant and with unity gain, for in-band signals, then

$$\sigma_{dy}^2 = \sigma_{dy}^2|_{du(n)} + \sigma_{dy}^2|_{deq(n)*ntf(n)} \tag{4.10}$$

For a sinusoidal input signal, $v_{in}(t) = Asin(\omega_{sig}t)$, it can be shown that [62]

$$du(n) = u(n) - u(n-1) = 2Asin(\frac{\pi}{2OSR_{sig}})cos(\frac{\omega_{sig}(2n-1)T_s}{2} + \phi_{sig}) \tag{4.11}$$

where $OSR_{sig} = f_s/2f_{sig}$ and ϕ_{sig} is the excess phase of the STF. If the term, $\pi/(2OSR_{sig})$ is much less than 1, then the approximation of sin(x) $\approx$ x can be applied to the sinusoidal item in the above equation.Therefore power of the signal related component in $dy(n)$ is given by

$$\sigma_{dy}^2|_{du(n)} \approx \frac{\pi^2}{2}(\frac{A^2}{OSR_{sig}^2}), \text{if } OSR_{sig} >> 1 \tag{4.12}$$

Therefore, signal to jitter noise, $SJNR_{sig}$ due to the power of signal related component in $dy(n)$ is given by

$$SJNR_{sig} = \frac{OSR}{4\pi^2 BW^2 \sigma_j^2} \tag{4.13}$$

From the above expression, $SJNR_{sig}$ increases with OSR . This is because with

the increase in OSR, signal related transitions decrease at the output. Eq. 4.13 does not include the jitter induced noise power from the shaped quantization noise $de_q(n) * NTF(n)$ as given in Eq. 4.10. Power of the quantization noise in $dy(n)$ is given by

$$\sigma^2_{dy}|_{de_q(n)*NTF(n)} = \frac{\Delta^2}{12}\sigma^2_{NTF} \tag{4.14}$$

where Δ is the LSB of the quantizer and σ^2_{NTF} is given as [54]

$$\sigma^2_{NTF} = \frac{1}{\pi}\int_{-\pi}^{\pi} |NTF(e^{j\omega})|^2(1 - cos(\omega))d\omega \tag{4.15}$$

SJNR due to shaped noise $(de_q(n) * NTF(n))$ is given by [54]

$$SJNR_{noise} = \frac{3A^2}{OSR.BW^2.\Delta^2.\sigma_j^2.\sigma^2_{NTF}} \tag{4.16}$$

From the above expression, $SJNR_{noise}$ decreases with aggressiveness of the noise shaping, σ^2_{NTF} (see Eq. 4.16). $SJNR_{noise}$ can be reduced by employing more quantizer levels and thus smaller quantization step, Δ. $SJNR_{noise}$ improves with the input signal amplitude unlike $SJNR_{sig}$ (see Eq. 4.13) Strong out of band quantization noise convolves with the broadband noise of the clock and down converts as in-band noise. This convolution process is shown in Fig. 4.8. Fig. 4.9 shows the increase in the noise floor when the jitter tone convolves with the OOB quantization noise.

4.2.5. Sensitivity of ADC to blockers and clock jitter

In the previous sections, the sensitivity of the CT $\Delta\Sigma$ ADC to blockers and jitter separately were discussed. In this section, their effect together on the ADCs

is presented. Clock jitter causes random phase modulation to the output bit stream causing the OOB quantization noise to fold into the signal band raising the noise floor. The problem aggravates in presence of OOB blockers. Blockers convolve with the clock jitter and appear as in-band noise. Fig. 4.8 shows this effect in which a sinusoidal jitter tone is assumed in the clock to show the convolution effectively.

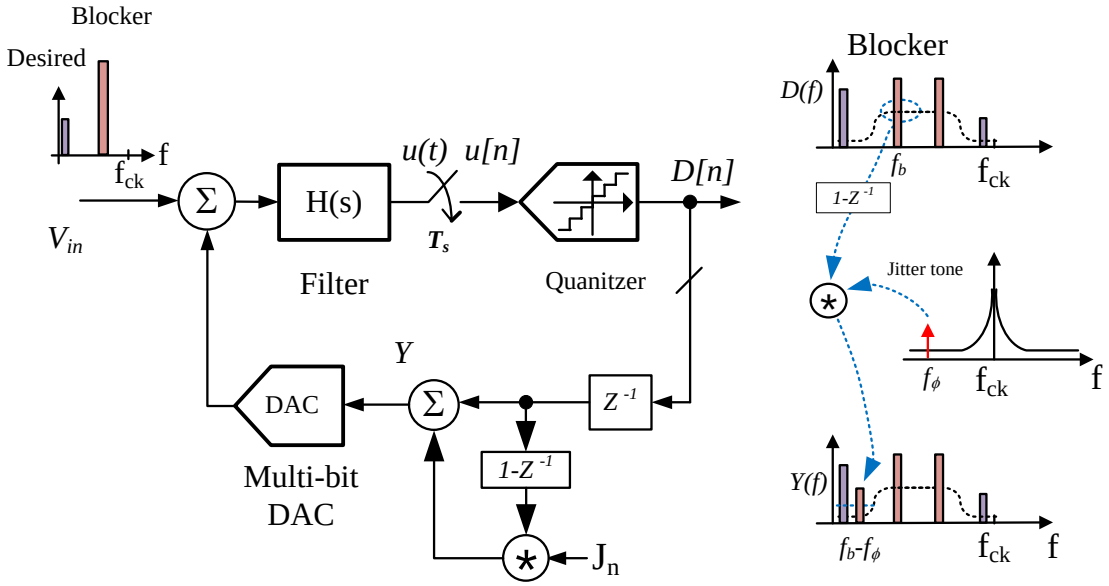


Figure 4.8: Effect of clock jitter and blockers together on CTΔΣ ADC. Blockers convolve with phase noise (e.g. jitter tone) and then fold back into baseband

The down converted jitter-induced blocker in-band noise degrades the modulator dynamic range. Following the analysis given in [54, 62] with OOB blocker as input signal, it has been shown that jitter noise due to clock jitter and blocker is given

by [62]

$$\sigma_{ej}^2|_{blocker} = 2(\sigma_{j,rms}/T_s)^2 A_{BLK}^2 G_{\omega BLK}^2 sin((\omega_{BLK}T_s)/2) \tag{4.17}$$

where A_{BLK} and ω_{BLK} are the amplitude and frequency of the blocker, respectively. $G_{\omega BLK}$ is the gain of the STF at frequency ω_{BLK} and $\sigma_{j,rms}$ is the rms-jitter in the clock. The jitter-induced blocker noise is a function of clock jitter, blocker power and the gain $G_{\omega BLK}$ at blocker frequency which could be larger than unity for a wide frequency range; see STF in Fig. 4.3.

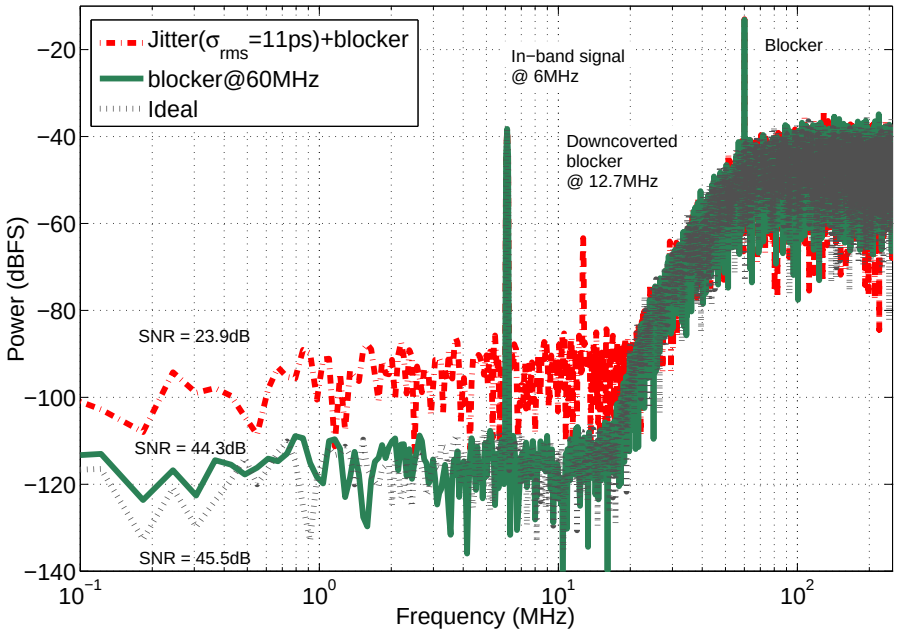


Figure 4.9: Sinusoidal jitter tone at 72.7MHz convolve with the blocker signal at 60MHz and generates in-band noise tones at 12MHz. Jitter tone also convolve with the strong OOB quantization noise and down converts it to baseband noise

A simulation showing the aforementioned convolution is displayed in Fig. 4.9. A blocker at 60 MHz and a sinusoidal jitter tone at 72.7 MHz with an equivalent $\sigma_{j,rms}$ of 11 ps convolute at the DAC input and generates an in-band tone at 12.7 MHz. It has $\sigma_{ej}^2|_{blocker}$ of -62.87 dBFS which is in good agreement with the simulation result. Noise level increases over 10 dB due to the convolution of jitter and OOB quantization noise. The proposed techniques reduce $G_{\omega BLK}$ at the critical frequencies thus reducing the in-band jitter-blocker induced noise. Existence of multiple blockers degrade the in-band performance as shown in Fig. 4.10

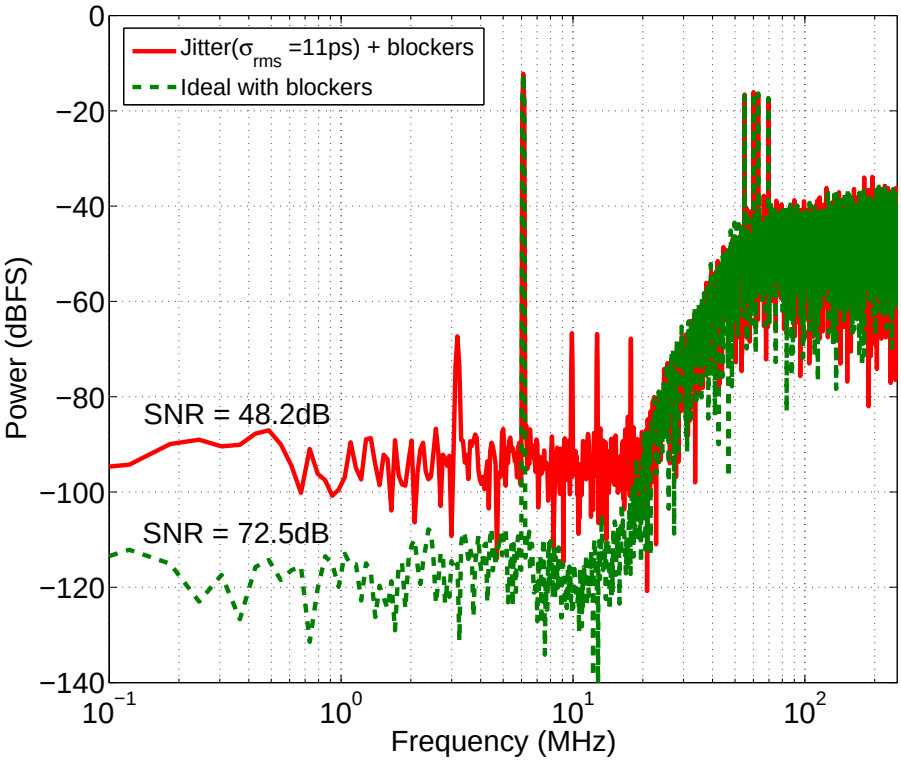


Figure 4.10: Blocker filter improves the SNR by 6.7dB for 4 blockers

4.3. Design Techniques for Blocker Tolerant CT ΔΣ ADC Architectures

As shown in Fig. 4.2, the loop filter of the ΔΣ modulator is implemented through two bi-quads and a first order LPF. The resonant frequencies in the bi-quads are used to optimally place the complex zeros in the NTF so as to achieve a uniform suppression of the quantization noise over the entire signal band. The quality factor (Q) of the bi-quads are optimally chosen to be finite to make the system less sensitive to the blockers and peaking at the cost of finite zeros in the NTF. The feed-forward currents and I_{DAC2} are summed in current-mode before sampling. Two techniques, as discussed below, are proposed in this work to deal with the blockers which potentially degrade the dynamic range and cause system instability.

4.3.1. Non-invasive integrated filter to increase blocker tolerance

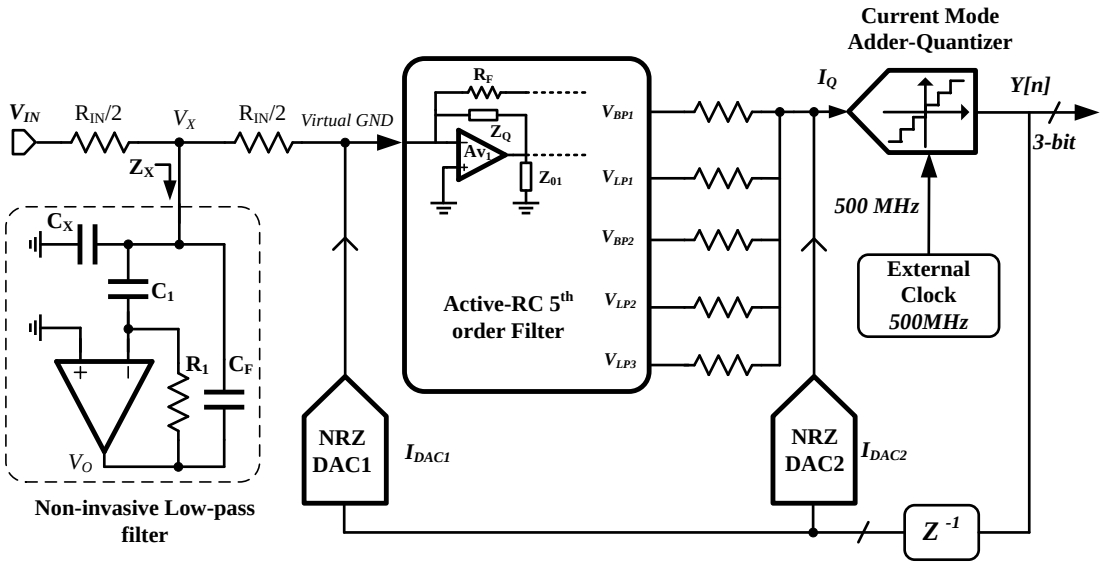


Figure 4.11: 5^{th}-order continuous-time feed-forward ΔΣ ADC with a non-invasive low-pass filter

A front-end filter improves the blocker tolerance since the ADC input power is reduced due to the attenuation of OOB blockers. The conventional filtering techniques process both the in-band signals and the blockers by the same circuitry. In-band components also travel through the filter components, whose quality is affected by the non-linearities and noise of the passive and active devices. The result is that the SNDR of the signal at the output of the filter degrades as follows:

$$SNDR|_{out} = SNDR|_{in} - 10log_{10}(1 + \frac{N_{filter}^2 + \sum_{i=2}^{N} H_i^2}{N_{in}^2}) \tag{4.18}$$

where H_i^2 is the power of the i^{th}-harmonic distortion components generated by the filter, usually measured when the signal and harmonics are in-band; more accurate computations should also include the in-band noise generated by filters non-linearities and OOB blockers. N_{in} and N_{filter} are the input and filters input-referred noise, respectively. The SNDR at the filters output is further reduced when the in- band folding of blocker signals due to OOB filters non-linearity is accounted. Therefore, the benefits of the regular filtering techniques are partially offset by these effects. Conventional low-noise linear filters are usually power and area hungry.

An ideal filter should not degrade the in-band performance but would be able to filter of the OOB signals. Authors in [63] employ a frequency dependent negative resistor (FDNR) based filter topology that provides shaping to the noise of the active and passive elements used. The fully-differential FDNR based filters are still power hungry since it requires employing 4 op-amps per bi-quadratic section in their implementation. Similar noise-shaping filter is achieved in the architecture proposed in this work but with minimum in-band noise and distortion. The proposed implementation uses only one op-amp to realize 2^{nd}-order filtering and does not suffer from common mode issues.

Minimally invasive integrated low pass butter worth filter is employed at the input of the ADC as shown in Fig. 4.11. This realization takes advantage of the existing input resistance R_{IN} of the ADC input stage, which is split into two sections to accommodate the frequency dependent impedance Z_x. This impedance creates a grounding path for the high-frequency signals; Z_x is very large for in-band signals and thus its noise and distortion contribution for in-band signals is negligible. The expression for the Z_x can be found employing conventional circuit analysis techniques; assuming an ideal amplifier, it can be found that

$$Z_x = \frac{1}{R_1 C_1 C_f} \frac{1}{(s + \frac{C_1 + C_x + C_f}{R_1 C_1 C_f})} \tag{4.19}$$

This driving impedance element shows a -20dB/decade roll-off at low frequencies, while it reduces at a rate of -40dB/decade at medium and high-frequencies. Notice that Z_x is capacitive at low frequencies which suggest that this network does not have significant effect on the node V_x; neither noise nor distortion due to this block are critical for baseband operation. However, at medium and high frequencies, all capacitors help in decreasing the impedance of Z_x thus absorbing the high frequencies. Assuming a virtual ground at the modulators input, the transfer function at V_x is then given by

$$\frac{V_x}{V_{in}} = \frac{Z_x}{\frac{R_{IN}}{2} + 2Z_x} = \frac{0.5\omega_{0f}^2}{s^2 + \frac{\omega_{0f}}{Q} + \omega_{0f}^2} \tag{4.20}$$

where $\omega_{of}^2 = 4/(R_{IN} R_1 C_1 C_f)$ and $\omega_{0f}/Q = (C_1 + C_x + C_f)/(R_1 C_1 C_f)$. Selecting the components, the filter shape can be easily synthesized. This filter absorbs the OOB blocker power at the most critical frequencies. The amplifier is built using a low-gain (around 20 dB) high-bandwidth, class-AB amplifier which meets large

signal performance requirements with good linearity and low power consumption (1.4 mW).

The noise generating elements of this filter are R_{IN}, R_1 and the op-amp. R_{IN} is part of the ADCs loop filter and its noise contribution is accounted for in the ADC noise budget. Following are the expressions for the noise transfer function referred to V_X for both R_1 and op-amp

$$\frac{V_x}{V_{n,r1}} = \frac{1}{R_1 C_1} \frac{s}{(s^2 + \frac{\omega_{0f}}{Q} + \omega_{0f}^2)} \tag{4.21}$$

$$\frac{V_x}{V_{n,op}} = \frac{s(s + \frac{C_1 + C_f}{R_1 C_1 C_f})}{s^2 + \frac{\omega_{0f}}{Q} + \omega_{0f}^2} \tag{4.22}$$

where $V_{n,r1} = \sqrt{(4KTR_1)}$ is the noise of resistor, R_1 and $V_{n,op}$ is the input referred noise of the op-amp. From Eq. 4.21 and Eq. 4.22 $V_{n,r1}$ and $V_{n,op}$ are shaped by band pass and high pass like transfer functions, respectively.

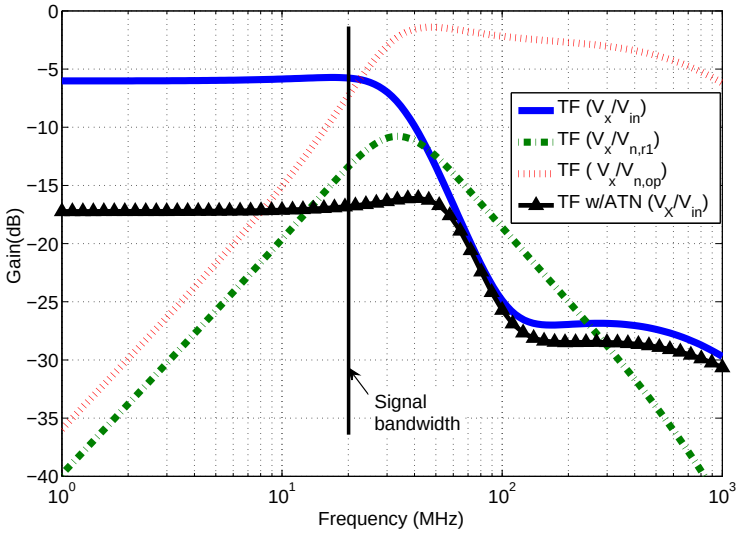


Figure 4.12: Signal and noise magnitude response of a minimally-invasive low-pass filter

The filters signal and noise transfer functions are depicted in Fig. 4.12. Note that the in-band gain of -6dB is not due to the added impedance Z_x but by resistance division, $R_{IN}/2$. Noise shaping of $V_{n,r1}$ and $V_{n,op}$ results in reduced integrated in-band noise. The plots slightly deviate from equations 4.20- 4.22 due to the finite gain of op-amp and high frequency parasitic poles. According to Fig. 4.12, $V_x/V_{n,op}$ becomes close to unity only for frequencies outside the signal band hence does not degrade the in-band performance. Within the signal band of the ADC, the integrated noise power from R_1 and Op-Amp can be approximated as (for $C_1 < C_F$)

$$V_{x,n} = \frac{1}{\sqrt{3}R_1C_1\omega_{0f}}\sqrt{(V_{n,r1}^2 + V_{n,op}^2)f_{of}} = \alpha V_{n,TOT} \tag{4.23}$$

where $\alpha = 1/(\sqrt{3}R_1C_1\omega_{of})$ is the factor by which the integrated noise is reduced by the noise shaping. For butter-worth realization, $\alpha = 0.2$. As a result the total integrated in-band noise voltage contribution at V_x is less than 15 μV rms which is well below the ADC thermal and quantization noise levels.

To avoid significant roll off at the signal band corner due to the added LPF, the cut-off frequency of the filter is chosen to be 32MHz. R_{IN}= 1.6KΩ,R_1 = 4.14KΩ,C_1= 3.3pF,C_F=4.51pF,C_x=4pF are the values of the components used to realize the minimally invasive filter. Input referred thermal noise of the ADC excluding the minimally invasive LPF is 42.13μV. Input referred noise of the added LPF, $V_{x,n} < 15\mu$V increases the ADC noise by 6.8% to 45μV keeping the thermal noise to be at -80dBFS. Overall ENOB is expected to be 12 bits.

Inband linearity is very good for this filter as Z_x is purely capacitive for low frequencies. OOB linearity of this filter is characterized by two-tone test (-6 dBFS blockers each at $f_{b1} = 60MHz$ and $f_{b2} = 111.5MHz$) where it is verified that in-band inter-modulation products is -87dBFS (over 14-bit linearity) as shown in Fig. 4.13.

The blocking signals f_{b1} and f_{b2} are attenuated by 16dB and 25dB, respectively, by the filter.

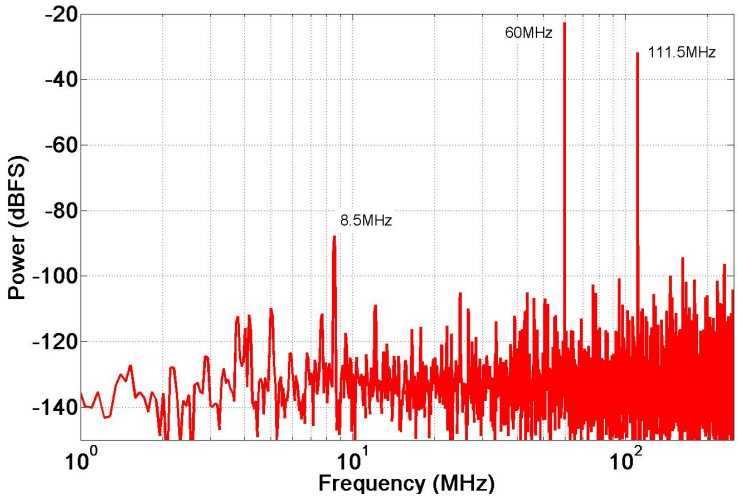


Figure 4.13: Simulations showing OOB linearity with two -6dBFS blockers at 60MHz and 111.5MHz

If a regular 1-pole filter were added before the ADC, most of the specifications must be better or at least equal to the ones required by the first OPAMP in the ADC loop filter. Filter linearity should be similar or better than ADC linearity. Non-invasive filters linearity is clearly superior, see Fig. 4.13. Power could be similar to OPAMP 1 in loop filter; e.g. 3mW. Non-invasive filter requires only 1.4mW. Noise for a regular filter is similar to the one of the loop filters first stage and it is most likely system thermal noise will increase by 3dB. Non-invasive solution increases in-band noise by 6.5% only. Besides the proposed filter gives 2^{nd} order filtering.

Existence of multiple blockers degrade the in-band performance as shown in Fig. 4.14. From the figure it can be noticed that the employed blocker filter improves

the SNR by 6.7 dB for 4 blockers. In reality for wide-band radios with limited pre-filtering the OOB power is huge. In such cases the improvement would be high. We can also notice that the in-band jitter induced blocker tones are attenuated as the blocker power is suppressed by the blocker filter.

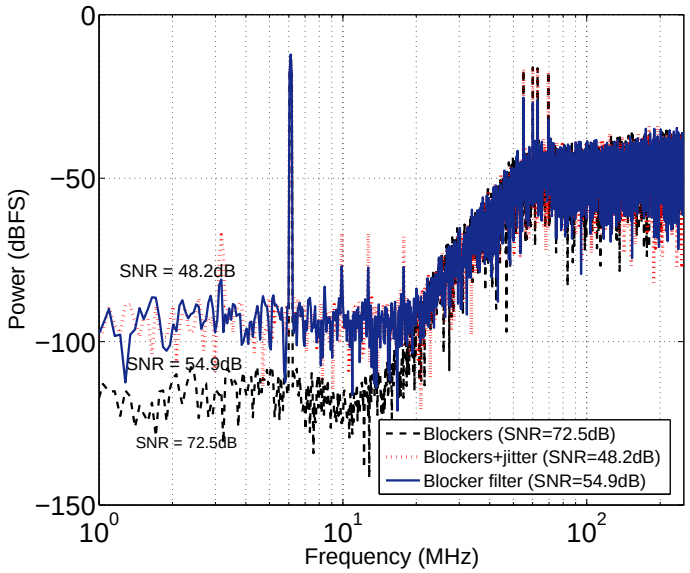


Figure 4.14: Blocker filter improves the SNR by 6.7dB for 4 blockers

Adding Z_x does not degrade the stability of the loop significantly. A simulation showing the gain and phase response of LF(s) (see Eq. 4.1) with and without the blocker filter is shown in Fig. 4.15. It can be seen that the response is same in both the cases. This is expected as the active RC integrators provide virtual ground nodes that can properly sink the output signals of the current mode DAC. Thus the integrated minimally invasive filter does not pose any stability issues. The stability is also confirmed by a step response as shown in Fig. 4.16. It can be seen that the response is same in both the cases.

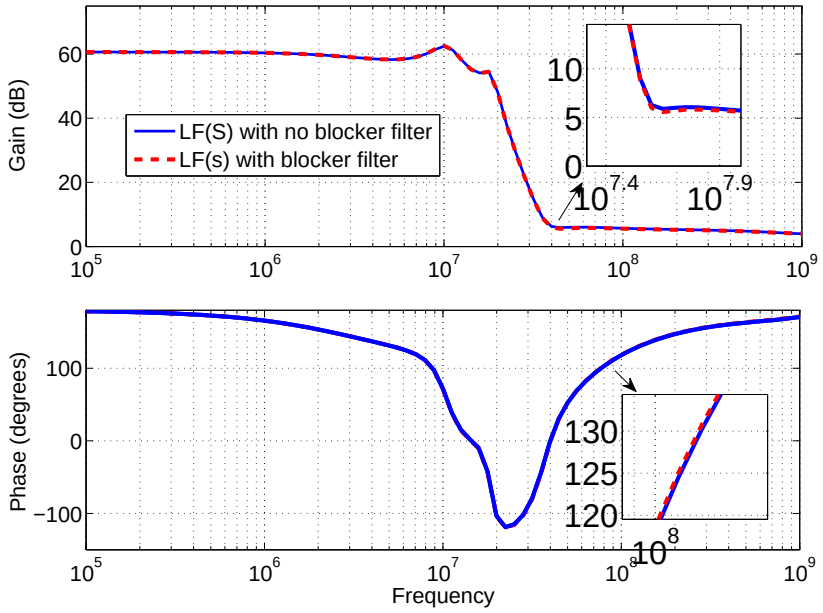


Figure 4.15: Bode response of LF(s) defined in Eq. 4.1 with and without the blocker filter

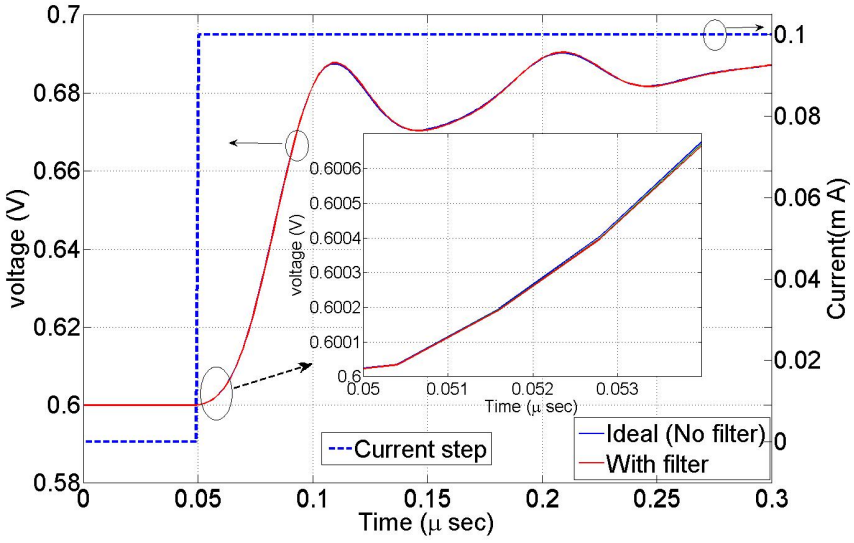


Figure 4.16: Step response of the loop filter and the summer

4.3.2. Overload detector and variable gain attenuator

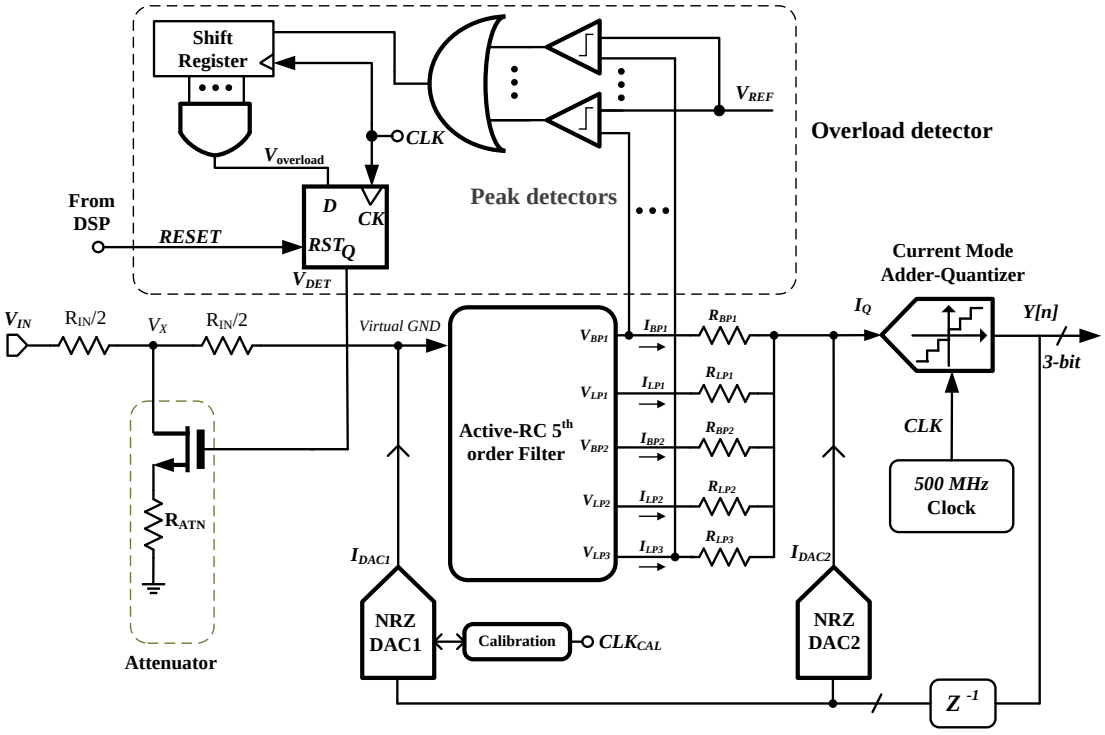


Figure 4.17: 5^{th}-order continuous-time feed-forward $\Delta\Sigma$ ADC with overload detector monitoring the critical filter nodes and controlling the attenuator

OOB blockers may cause peaking in internal nodes and overload the CT-$\Delta\Sigma$ ADC loop. A loop overload detection block is designed to detect the peaking and thus the corresponding blockers. The employed wide bandwidth overload detector and attenuator are very effective to detect and attenuate the blockers. The overload detection system is realized by using a set of simple voltage level comparators, digital logic and a voltage attenuator implemented with a T-network at the ADC input, as shown Fig. 4.17 for the case of a single attenuation factor. The overload detectors

monitor the critical integrator output nodes (BP1, LP1, LP2, BP2, LP3) of the loop filter to detect overloading conditions. More than one node is being monitored as the node peaking is a function of its initial conditions and the closed loop gain from input to the node. When overload occurs (internal signal swings exceed their linear range defined by $V_{threshold}$), the detector output raises a flag ($V_{OVERLOAD} = 1$).

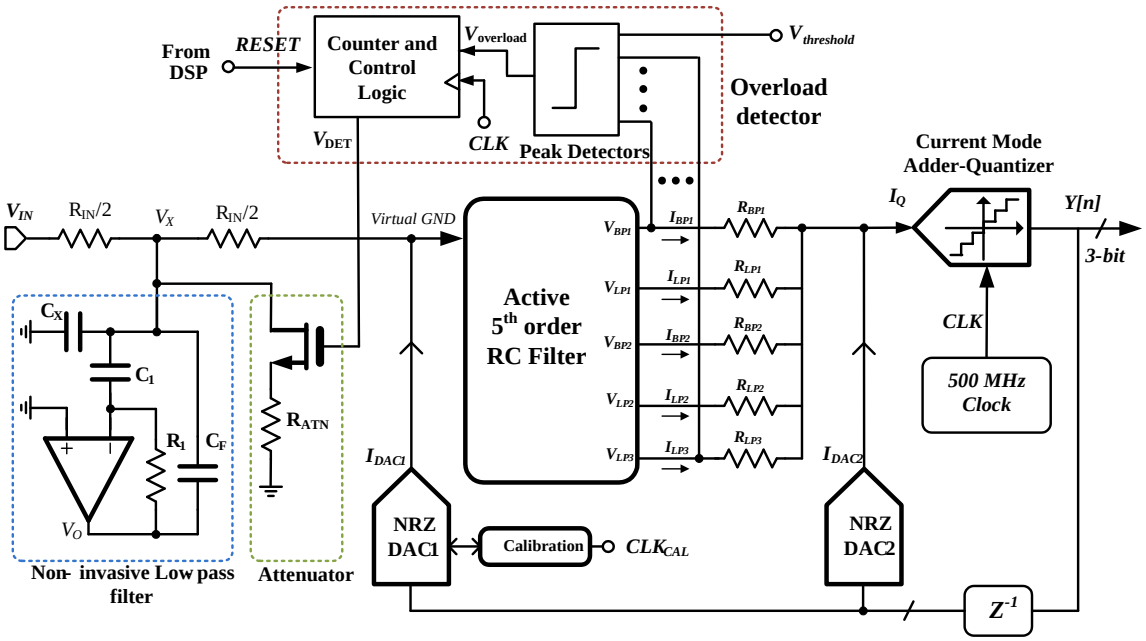


Figure 4.18: 5^{th}-order continuous-time feed-forward $\Delta\Sigma$ ADC with overload detector monitoring the critical filter nodes and controlling the attenuator. Low-pass filter at the input attenuates the OOB blockers at the critical frequencies (40MHz-80MHz) and beyond

To avoid false alarms due to glitches in the system, a minimum number of consecutive overloading detections are required before the attenuator is activated; five clock cycles in this prototype, but more conservative schemes can be used. This

scheme is implemented by logic functions. Fig. 4.18 shows the block diagram of the complete 5^{th}-order $\Delta\Sigma$ ADC. Critical output nodes of the loop filter are monitored by the peak detectors whose output is processed by the logic circuits to generate a control signal,V_{DET}. This signal controls the attenuation factor to reduce the ADC input power maintaining the internal signals within the ADCs linear range. The PGA available in most of the receivers can be used for this purpose, however, in this prototype the technique is realized by a single attenuator of 9.4 dB.

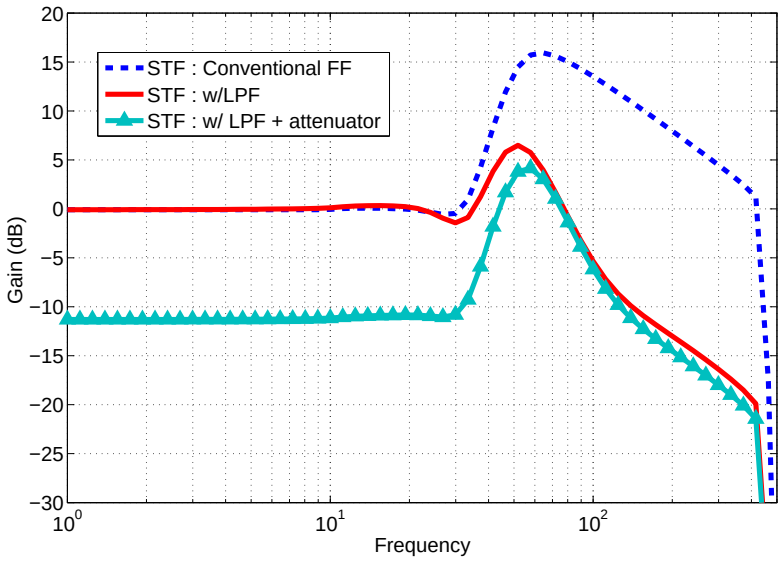


Figure 4.19: Simulation showing the STF of the ADC with the proposed blocker tolerant techniques

The attenuation factor can be made programmable for different blocker powers by making R_{ATN} adjustable. Notice that both the in-band and OOB signals are attenuated, by the attenuator. Although attenuation decreases the SNR by the attenuation factor, it improves the blocker tolerance. Actually SNDR degradation is less than

attenuation factor as the distortion decreases with the decrease in the overall input power. When the DSP at the output bit stream determines that there is no blocker, it restores the input signal level by resetting the overloading protection system. This overload detection-attenuation achieves fast settling time (blocker adaptation time) because attenuation is done outside the $\Delta\Sigma$ loop, keeping the loop transfer function invariant.

Fig. 4.19 shows the reduction in OOB peaking and the increase in OOB attenuation in the STF with the proposed blocker reduction techniquesThe proposed blocker reduction techniques also reduce the input referred blocker noise which is a consequence of the non-linearity in the loop filter and DAC and jitter in the DAC clock. Loop filter non linearity down converts the inter-modulation products of the OOB blockers raising the in-band noise. As discussed in section 4.2, jitter convolves with OOB blockers and down converts as in-band noise. Thus by attenuating the blocker power before entering the ADC the proposed blocker reduction techniques improve its stability and performance. The schematic of the modulator with the proposed blocker reduction techniques is shown in Fig. 4.18.

4.4. Circuit Implementation

4.4.1. Loop filter

Individual sections of the 5^{th}-order loop filter are realized using active-RC integrators as shown in Fig. 4.20. $\pm 30\%$ capacitive tuning is employed in the integrator time constants to counter the P.V.T. variations of the time constants. The schematic of the OTA employed in the filter is shown in Fig. 4.21. To achieve both high gain and high bandwidth, the OTA is implemented using a 2-stage amplifier stabilized through a feed-forward path (g_{mff}) [64].

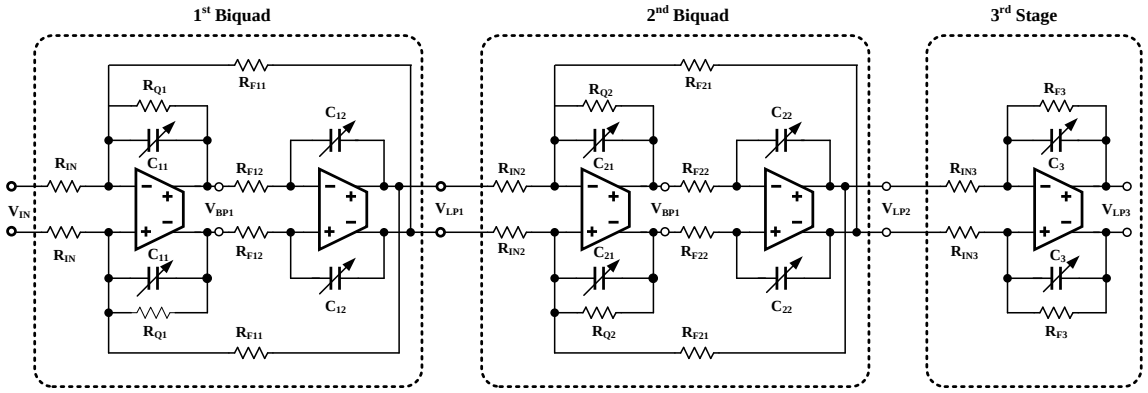


Figure 4.20: Block diagram of the complete 5$^{\text{th}}$-order loop filter employing active-RC integrators

The 1$^{\text{st}}$ stage (g_{m1}) is realized by a current re-use complementary input stage to increase its transconductance and to minimize the input referred noise; this stage provides over 26-30dB DC gain. The 2$^{\text{nd}}$ and feed-forward stages are optimized for high bandwidth and medium gain performance. For better linearity, the 2$^{\text{nd}}$ stage requires enough voltage gain which is achieved through complementary stages for high gm. This stage provides 10-15 dB gain when loaded by the filter passives, thus stage input signal could be as large as 50-100 mVpk. To further improve the linearity performance, an additional differential pair connected in cross coupled to the 2$^{\text{nd}}$ stage with source degeneration technique is employed [65]. Simulation results for this linearization technique along with source degeneration factor of 0.5 shows an improvement of more than 10 dB in HD3 while noise, area and power consumption do not increase by more than 10%.

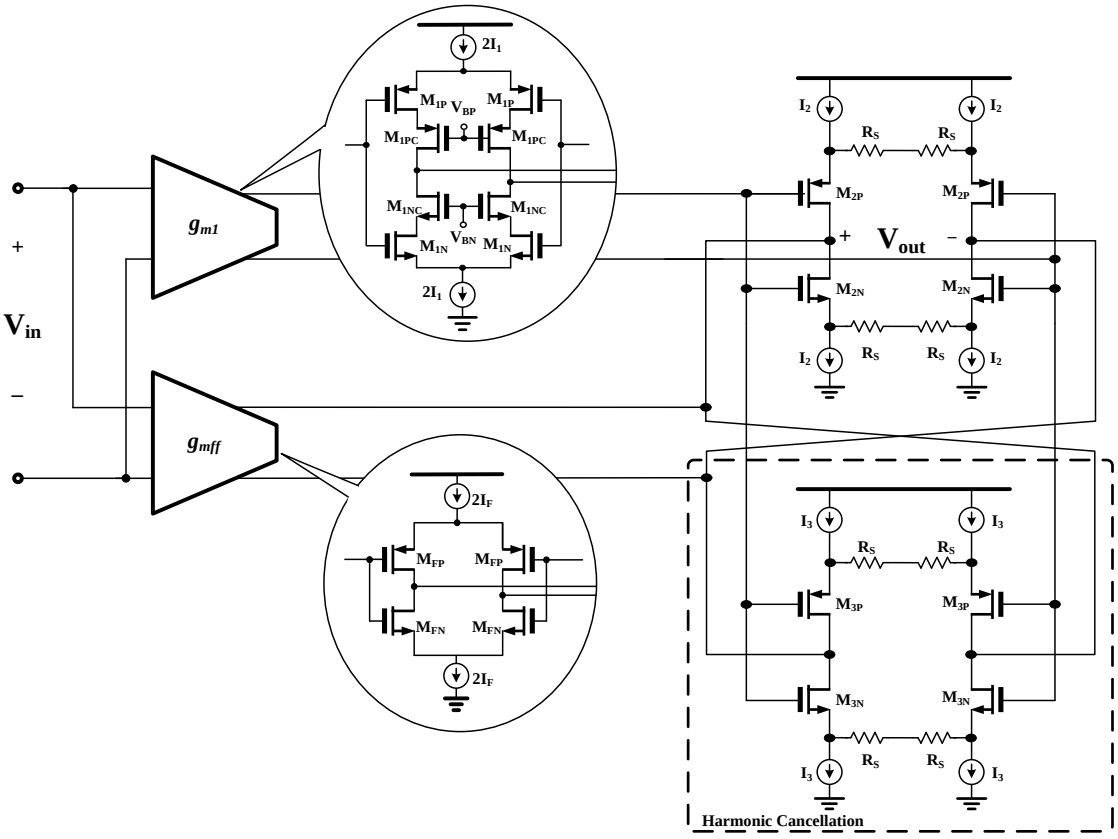


Figure 4.21: Simplified schematic of the two stage feed-forward g_m compensated OTA employed in the active-RC integrator

4.4.2. Current-mode adder-quantizer

For robust loop stability and performance, the summing amplifier in feed-forward architectures usually needs high GBW and is very power demanding. In the proposed modulator, summing of the feed-forward and DAC_2 current signals is done in current mode by using the low input impedance of a common gate transistor which greatly reduces the power consumption. The proposed current-mode adder-quantizer block consists of a current summing stage, current comparison stage and a latch stage. Fig. 4.22 depicts how the current input signals are summed at the source node of a

common-gate stage. A g_m-boosting technique was implemented in order to increase the in-band transconductance of the common-gate stage which lowers the effective input impedance (Z_{ins}) at the summing node. A_V is the voltage gain of the amplifier employed in gm-boosting. The same amplifier is used to set the common mode DC voltage (V_{REF}) at the summing node. The DC bias is designed such that only the summed AC input signal (I_Q) is delivered to the current comparison stage.

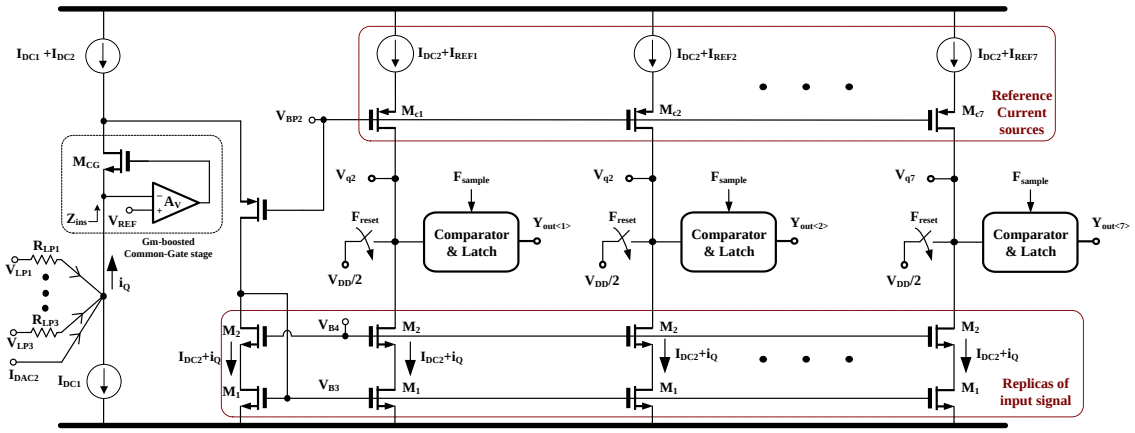


Figure 4.22: Schematic of a single ended current-mode adder-quantizer circuit with low power dissipation and reduced complexity

The 3-bit quantization is done in current mode by using simple current mirrors. I_Q is replicated through a set of current mirrors (1:1) and each branch current (I_Q) is compared with a quantized reference current level (I_{REFi}). The difference current ($I_Q - I_{REFi}$) flows through the high impedance cascode node, amplifying the difference value in voltage. In order to reduce the time required to resolve the signal at high impedance node, a reset step is performed after each current comparison. The outputs of the current-mode comparison are given to the next stage comprised

of a Strong-Arm comparator [66, 67] followed by an S-R latch. The outputs of the current-mode comparison are given to the next stage comprised of a Strong-ARM comparator [25], [26] followed by an NAND based S-R latch. The schematics of the implemented comparator and latch circuits are shown in Fig. 4.23. More details of the adder-quantizer stage can be found in [68]. More examples on power efficient current mode quantizers and other sub-blocks for $\Delta\Sigma$ ADC can be found in [69–71].

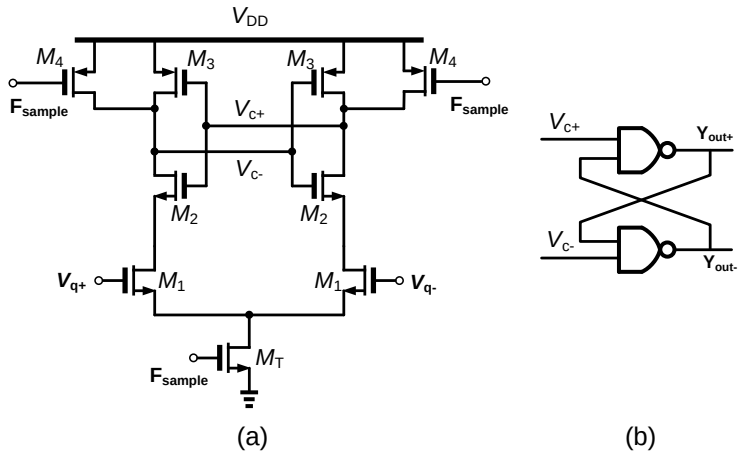


Figure 4.23: Schematics of (a) Strong-ARM comparator (b) S-R latch

4.4.3. Digital to analog converter

Both DAC_1 and DAC_2 in Fig. 4.18 are current steering 3-bit unary weighted DACs. Due to unavoidable mismatches, parasitic capacitors and other non-idealities, these DACs have static and dynamic errors. Static current cell mismatches and transistor nonlinear output impedance generate harmonic distortion components. Dynamic errors include errors due to glitch energy, which is caused by clock feed through due to C_{gd} (M_1,M_2) and voltage fluctuations at the source node of switch transistors

M_1,M_2 resulting from charging and discharging the parasitic capacitor C_P as shown in Fig. 4.24. The non-idealities of $\mathrm{DAC_1}$ appear at the modulators output without the any noise shaping, so it has the most stringent requirements in terms of linearity and noise. In presence of blockers due to large signal swings in the loop the in-band distortion gets worse.

In this work, reduced swing and high cross-over DAC drivers are used to reduce the glitch energy by guaranteeing either one of the DAC switches are always closed, minimizing clock feed through effects [72]. To further reduce the clock feed-through due to C_{gd}, two cross coupled dummy transistors (M_3, M_4) are used [49]. M_3 and M_4 have the same size of M_1 and M_2 and thus cancel the current injection of the main transistor pair.

Current source calibration at the start up [73] or Data Weighted Averaging (DWA) [74] are commonly used techniques to improve the DAC linearity. In this work, a calibration technique similar to [49] is employed at start up but with digitally assisted current sources to improve the linearity of the DAC_1. Fig. 4.24 shows a unit cell of $\mathrm{DAC_1}$ and the calibration circuit shared by all the 7 unit cells. $\mathrm{M_S}$ is the main current source in each unit cell of DAC. In calibration mode, $\mathrm{M_S}$ is disconnected from the DAC by turning off switch ($\overline{\mathrm{cal_i}}$) and connected to the calibration loop through $\mathrm{cal_i}$. I_{REF} is the external reference current to which each unit cell of DAC is calibrated. Current source, $\mathrm{M_S}$ is designed to carry a nominal current of $I_{COARSE} = (I_{REF} - 3\sigma_C)$, where σ_C is the standard deviation of I_{COARSE}. $N_C = 32$ sub-current cells are used to provide the mismatch current in $\mathrm{M_S}$ of each unit DAC cell. The feedback loop formed by $\mathrm{M_S}$, comparator, and the sub-current cells force the current in $\mathrm{M_S}$ and the sub current cells to be close to I_{REF}. Voltage reference (V_{REF}) for the comparator is generated by the replica bias as show in Fig. 4.24 which is essentially the $\mathrm{V_{DS}}$ of the current source $\mathrm{M_S}$ in normal operation. $\mathrm{M_C}$ is a cas-

code transistor to bias the V_{DS} of M_S for proper current mirroring. The calibration loop converges and stops when $V_{cali} < V_{REF}$. This happens when the difference in current $I_{REF} - I_{COARSE}$ is provided by auxiliary quantized sub-cells (I_s) with some quantization error (I_{qn}) as follows.

$$I_{REF} - I_{COARSE} = \sum_{i=1}^{j} I_s + (I_{qn}), j \in [1, N_c] \tag{4.24}$$

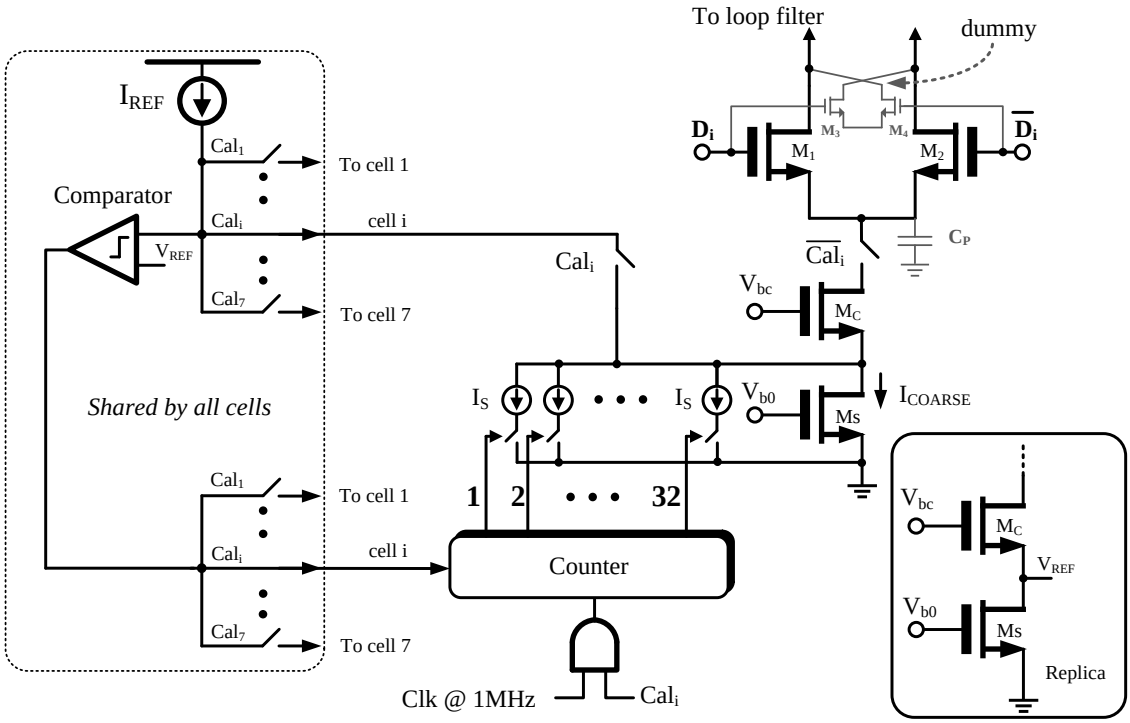


Figure 4.24: Schematic of a unit DAC cell including the digital calibration circuit, 32 sub-current sources controlled by a counter to calibrate the mismatches

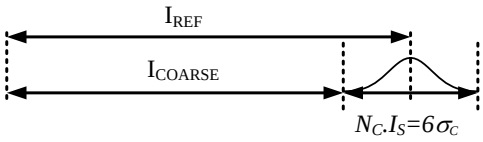


Figure 4.25: Current distribution for DAC calibration with 6-σ_C yield

As shown in Fig. 4.25, the design is centered for $j = N_c/2$ and $I_{qn} = 0$ in Eq. 4.24 After calibration, to have a minimum of 12 bit linearity in the DAC, $I_s = max(I_{qn})$ is chosen as follows.

$$I_s = 6\sigma_c/N_c \tag{4.25}$$

$$\sigma_c^2 = \sigma_{(\frac{\Delta I_{COARSE}}{I_{COARSE}})} = (\frac{g_m}{I_{COARSE}})^2 \frac{A_{vt}^2}{WL} + \frac{A_\beta^2}{WL} \tag{4.26}$$

where σ_C^2 is the variance of the error current in I_{COARSE}. A_{vt} and A_β are the variability parameters for threshold and mobility of the technology, respectively [75]. σ_C^2 decides the W/L and g_m of the current cell M_S in Fig. 4.24. The employed digital calibration technique is robust to noise and glitches in the circuit unlike [49] where the calibrated voltage is stored on the C_{gs} of the transistor and is sensitive to noise, glitches and charge leakage.

4.5. Experimental Results

The proposed techniques are tested in a 5^{th} order CT $\Delta\Sigma$ ADC fabricated in a 90nm CMOS technology which features 8 metal levels and MOM capacitors. The active area of the IC occupies 0.43 mm^2 silicon area as shown in Fig. 4.26. Single-ended open drain NMOS buffers are employed on chip for measurement purposes. The overall power consumption of the ADC (excluding the output buffers) is 17.1 mW with an additional 0.4 mW for DAC calibration. The off-chip clock from a signal

generator has rms jitter of 0.2%.

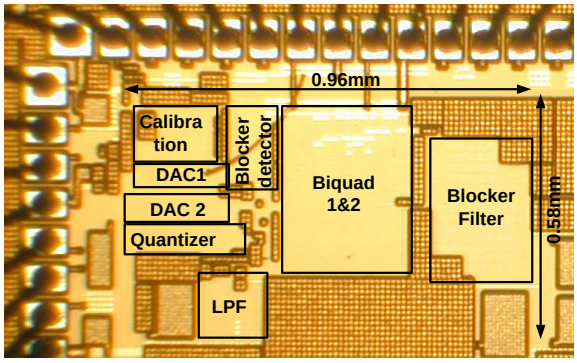


Figure 4.26: Chip micrograph; active area is 0.43mm^2

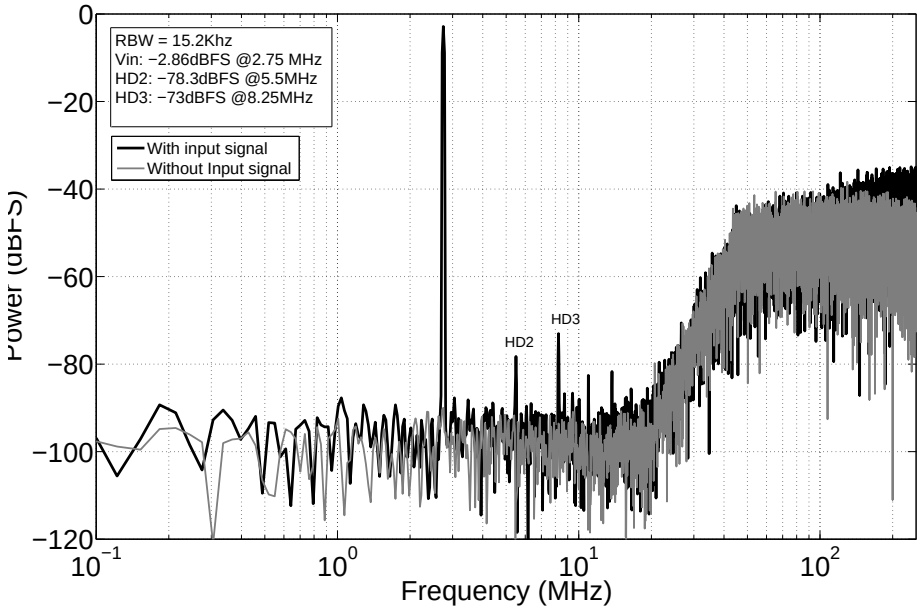


Figure 4.27: Measured output spectrum of the modulator with -2.86dBFS input signal at 2.75MHz

Fig. 4.27 shows the output spectrum of the modulator with an input of -2.86 dBFS at 2.75 MHz The measured peak SNR and SNDR, in 20 MHz bandwidth, is 66 dB and 64 dB, respectively. The 3rd harmonic distortion (HD3) and 2nd harmonic distortion (HD2) in this case are -73 dBFS and -78.3 dBFS, respectively. The measured SNR and SNDR for different input signal powers is shown in Fig. 4.28 in which 69 dB dynamic range (DR) is annotated. It was noticed in the laboratory that clock jitter, power supply noise and noise from on-chip single ended output buffers coupled to the ADC and degraded the expected dynamic range.

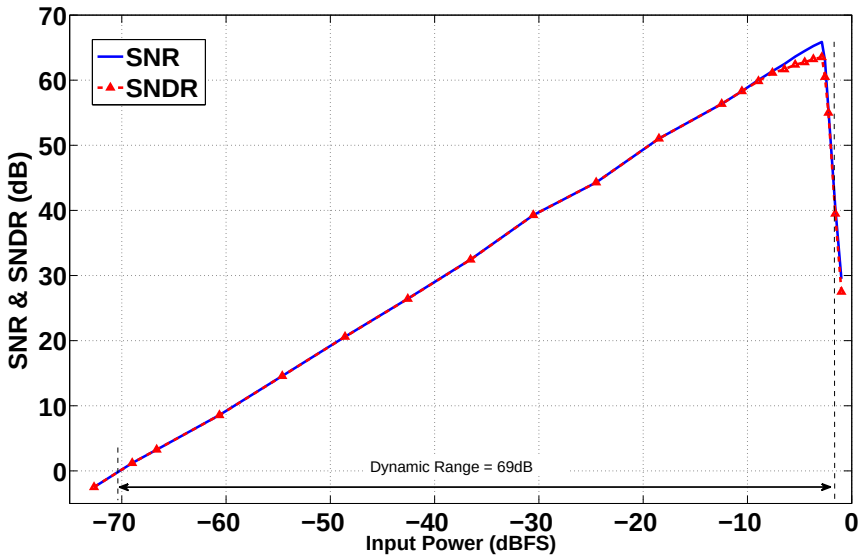


Figure 4.28: Measured SNR and SNDR versus input signal power

Third order inter-modulation distortion (IM3) performance is characterized by injecting two tones around 19.5 MHz with 0.61 MHz separation, each having a power of -9.8 dBFS. Notice in Fig. 4.3 that internal filter peaking of around 7 dB occurs under this measurement and then limiting loop linearity; larger input signals can not

be used in this case.

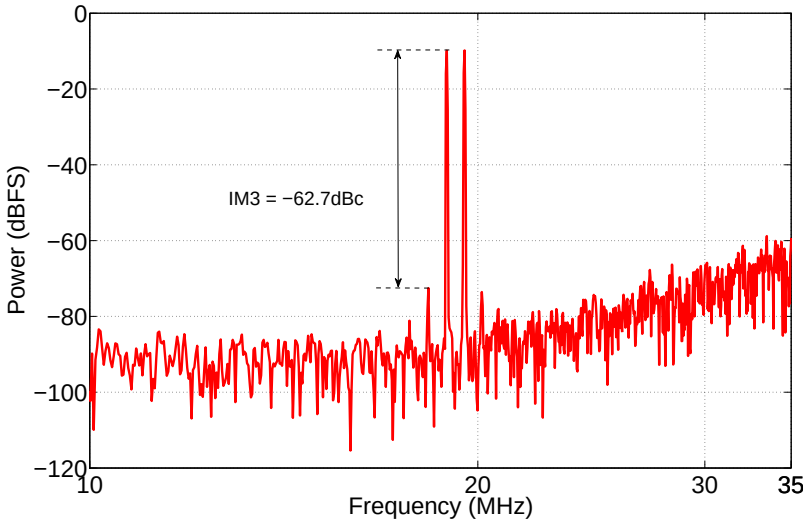


Figure 4.29: Two tone test for IM3 measurement

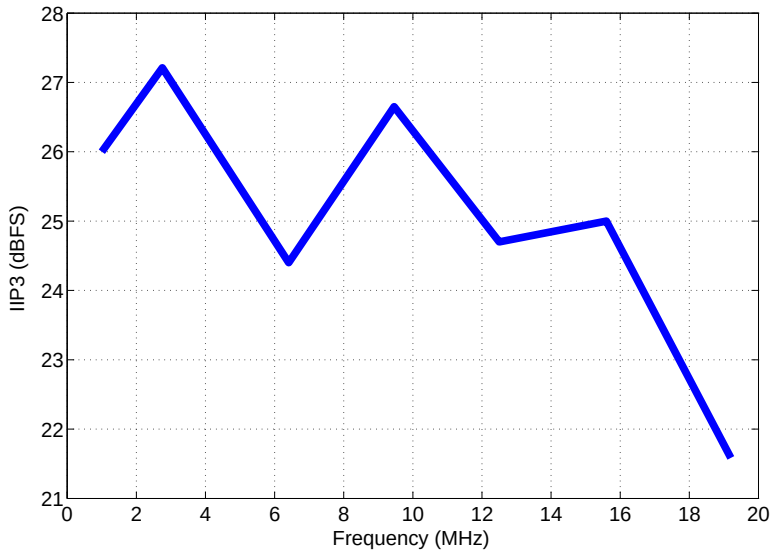


Figure 4.30: Measured in-band IIP3 as a function of frequency

As shown in Fig. 4.29, IM3 of -62.7 dBc at the band edge of the ADC is the worst case for the whole band as the loop gain reduces at the band edge. The noise level increases in this plot mainly due to the out-of band folding as well as due to the noise contribution of the signal generators. Fig. 4.30 shows the measured linearity of the system as a function of the frequency. It can be seen that IIP3 decreased by 4dB at the band edge compared to the low frequency IIP3.

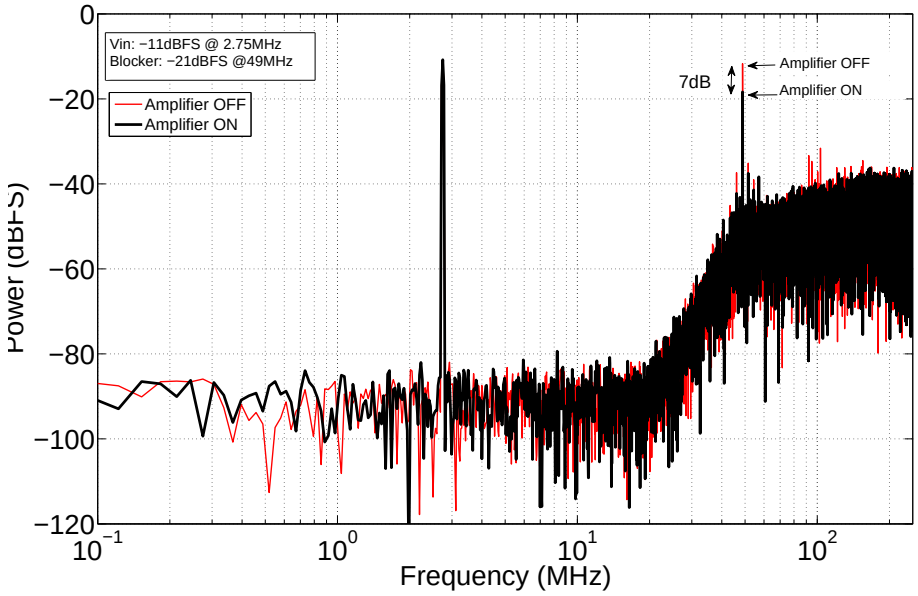


Figure 4.31: Modulators spectrum for 49MHz blocker in presence of -11.5dBFS input signal at 2.75MHz; this result shows a blocker attenuation of 7dB when the input low pass filter is activated.

Blocker rejection by the minimally-invasive LPF is characterized by sweeping the blocker frequency in presence of a -11.5 dBFS in-band signal at 2.75 MHz The modulators spectrum for the case of a -25 dBFS blocker tone at 49 MHz is shown in

Fig. 4.31. The LPF reduces the blocker power by 7 dB while SNR is improved by 3.6dB. This improvement in SNR is due to reduction in system nonlinearities when the blocker is attenuated. Usually strong blocker powers compress the gain of the system for in-band signal degrading modulators SNR.

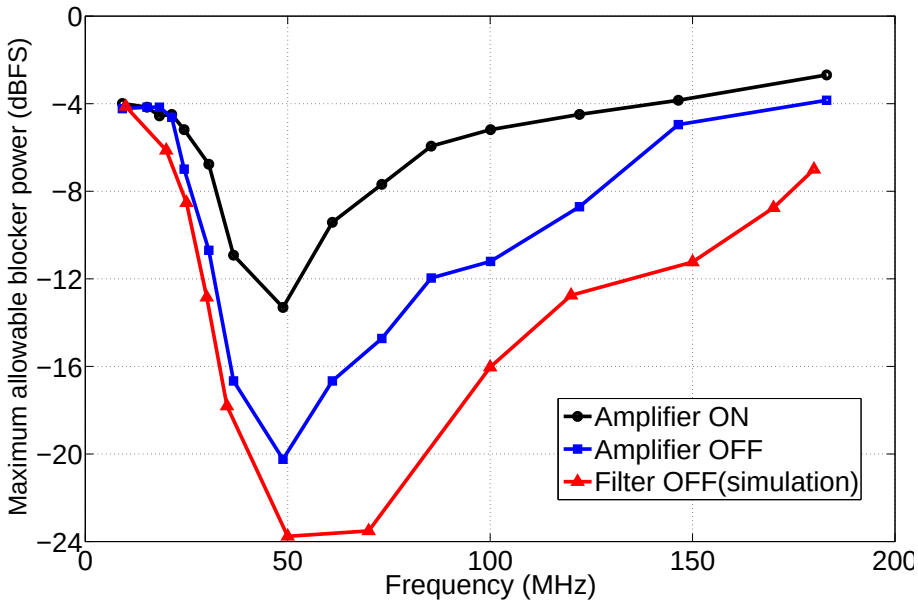


Figure 4.32: Blocker tolerance with the amplifier ON and OFF in presence of an in-band -11.5dBFS signal at 2.75MHz

Fig. 4.32 shows the maximum allowable blocker power to the modulator beyond which the SNDR decreases by 3 dB and eventually saturates the system. Amplifier ON is the case where OTA (used in the non-invasive filter) is activated for the measurement. The Amplifier OFF case has first order filtering pole approximately at $4/(R_{IN}C_X)$; see Fig. 4.11. Filter OFF is the case in which the input low pass filter is completely removed. This case is different from Amplifier OFF case as the

input shunt impedance Z_X cannot be excluded for measurement and can only be done through simulations. Fig. 4.31 is a particular frequency point of Fig. 4.32 for cases Amplifier ON and Amplifier OFF at 49 MHz. First order filtering (Amplifier OFF trace) improves blocker tolerance by 4dB or more beyond 49MHz, while the 2^{nd} order non-invasive filter increases blocker tolerance by 11 dB for the same frequency range.

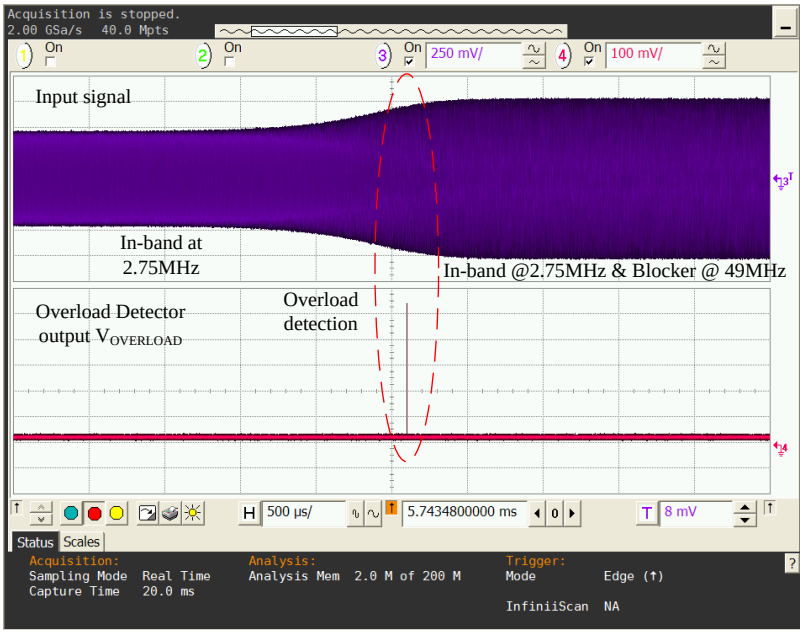


Figure 4.33: Blocker arrival and the detection

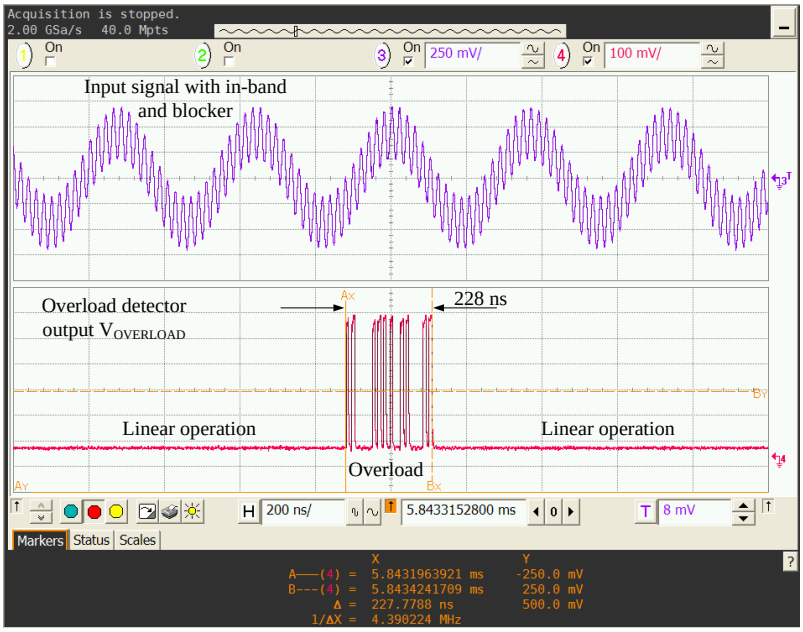


Figure 4.34: Zoomed view of Fig. 4.33. The system stays saturated for 228ns (transient period) before coming back to linear operation

The feasibility of the saturation detection system was tested employing an ON-OFF modulated sinusoidal blocker signal as depicted in the Fig. 4.33. An OOB blocker was added to the in-band signal as a step but the finite bandwidth ADC driver limits the speed of the input transitions. Top trace in Fig. 4.33 shows -11.75 dBFS in-band signal at 2.75 MHz and an added blocker at 49 MHz with -12 dBFS input power. The modulator (Amplifier OFF in Fig. 4.32) can tolerate only -20 dBFS power at this critical blocker frequency. The overload detector monitoring the critical nodes provides a flag signal ($V_{OVERLOAD}$) when the signal swings in one or more nodes consistently exceeds the amplifiers linear range. The bottom trace in Fig. 4.33 shows the $V_{OVERLOAD}$ signal; see Fig. 4.16. When overload is detected, the PGA is then activated reducing the modulators signal power to maintain the linear

operation of the loop. Fig. 4.34 is a zoomed view of the waveforms. The system takes 228ns of blocker adaptation time to return back to linear operation after being overloaded by a strong blocker. when the overload detector turns-on the input attenuator the input signal gets attenuated by 9.4dB to which brings the system from overload state to linear operation.

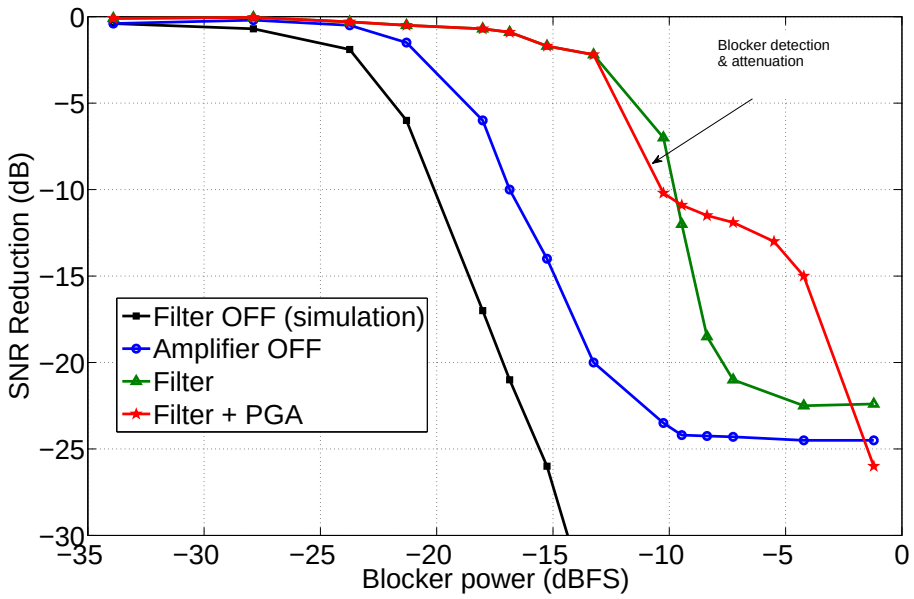


Figure 4.35: SNR reduction with the blocker power

Fig. 4.35 shows the reduction in SNR for a -12 dBFS in-band signal at 2.75 MHz with the blocker power at the critical frequency of 49 MHz. SNR decreases with the increase of the blocker power due to increase in system non-linearities, gain compression and eventual quantizer overload. At the medium blocker power levels, both OOB quantization noise and blocker power increases the in-band noise due to the non-linearity in both DAC and loop filter. Stronger blockers saturate the loop

filter and quantizer resulting in the steep fall in the SNR. By employing the input low pass filter, the OOB blockers are attenuated at critical frequencies and beyond; this increases systems robustness to blockers by maintaining the system performance which is shown by the Filter curve. The PGA kicks in when large signals are observed in the system. When the PGA is activated it reduces the input signal by 9.4 dB in this prototype. Although SNR is reduced, blocker tolerance of the system is improved.

Table 4.1: Performance comparison of blocker tolerant ADCs

	[49]	[50]	[51]	This work
Fs[MHz]	250	64	160	500
BW [MHz]	10	1	5	20
Dynamic Range[dB]	71	65^{ϕ}	76	69
Blocker reduction [dB] adjacent/alternate channels	8/15	$9.5/20^{\eta}$	10	$15/18^{\theta}$
Settling time (μ sec)$^{\psi}$	51	0	0	<0.3
Power consumption [mW]	18	4.1	6	17.1
Area[mm^2]	1.35	0.14	0.56	0.43
Technology [nm]	130	180	130	90

$^{\phi}$ fixed input resistance

$^{\eta}$ Extracted from a plot comparing measured and simulated performance, no in-band signal

$^{\psi}$ blocker adaptation time

$^{\theta}$ With -11.5dBFS in-band signal at 2.75MHz and blockers at adjacent / alternate channels for a 20MHz BW ADC

Table. 4.1 compares the performance of the proposed solution with the latest ADCs intended for high blocker tolerance. The proposed blocker reduction tech-

niques provide a total of 18 dB blocker attenuation at the most critical frequency range in presence of a -12 dBFS in-band signal. The blocker tolerance of the proposed architecture outperforms previously reported topologies in speed (settling time) and blocker robustness

4.6. Summary

A thorough discussion on the sensitivity of CT $\Delta\Sigma$ ADC to blockers is presented. Strong OOB blockers degrade the DR of the ADC and can potentially destabilize the system. The effect of blocker and jitter interaction on the in-band noise is also explained. A blocker tolerant CT $\Delta\Sigma$ ADC for broadband receivers is proposed. With the integrated blocker detector/attenuator, the input signal is reduced to prevent the system from getting saturated in presence of blockers. The proposed solution is effective for rapidly varying blockers that may saturate the loop when operating with its full dynamic range. Although the input signal is attenuated in the proposed blocker detection scheme, the system is less prone to saturation with only a moderate SNR degradation in the presence of blockers. The proposed system with the blocker detector settles in less than 0.3μs. This fast detection and self-correction is highly important in radio applications to maintain the communication active. To further attenuate the blockers, an active minimally-invasive integrated LPF filter that attenuates the most critical adjacent/alternate blockers is employed. Power overhead due to the proposed blocker tolerant techniques is only 6% of the total power budget.

5. ACTIVE ANTENNA: A CMOS FRONT END MODULE (FEM)*

5.1. Introduction

System on a Chip (SoC) demands high levels of integration and rapid product development. Digital products can be co-developed with new technology for rapid deployment while RF products lag behind, requiring a stable process with accurate models, special CAD tool support, hand-crafted layouts and multiple design iterations. With fast-track design methodologies required for short product life cycles, we cannot allow RF design to hold SoC product development hostage in today's competitive marketplace. RF circuitry with inductors consumes a large die area making a complete radio in scaled technology more expensive than in older technology. RF circuitry is usually lower performing in SoC technology because of breakdown voltage and sub-optimal metal layers chosen for digital density. By properly partitioning the radio and developing a design methodology for the SoC analog/mixed-signal radio, the die size/cost is greatly reduced and this function can be developed concurrently with digital collateral at the beginning of a technology development cycle. This will lower risk and reduce the time-to-market (TTM).

This chapter presents a novel CMOS RF front end module (RF-FEM) with Power amplifier (PA), Low noise amplifier (LNA) and Transmit/Receive (T/R) switch co-designed with Antenna. The co-design gives the advantage of reducing/removing the losses in the matching circuits, which are typically employed in the conventional radios and improves the overall performance. From the proposed radio partitioning methodology, the CMOS RF-FEM is separated from the system on chip (SoC)

*Part of this chapter is reprinted with permission from "A flip-chip-packaged 25.3dBm class-D outphasing power amplifier in 32nm CMOS for WLAN application," by H. Xu *et al.*, *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1596-1605, Copyright 2011 by IEEE

transceiver. This separated RF-FEM design methodology gives robust analog and mixed signal radio development in scaled technology for SoC integration, and the co-design of the RF FEM-antenna system.

This chapter presents the design highlights and novel ideas of a radio transceiver (active antenna) operating at 2.5GHz, based on a novel radio partitioning methodology. Conventional system level radio design with the matching circuits is discussed in section 5.2. Concept of co-design, the new radio partition methodology and the resulting benefits are briefly discussed in section 5.3. Section 5.4 introduces the class D power amplifiers and the conventional power combiners employed in them. Proposed Spectral power combination through dipole antenna for a class D PA is also discussed in this section. Section 5.5 introduces a non-invasive, less lossy passive T/R switch. Section 5.6 discusses the receiver architecture and the design of the front end LNTA. Antenna design and related issues are discussed in section 5.7. Simulated and measurement results are shown in section 5.8. Conclusions are drawn in section 5.9.

5.2. Radio Design

5.2.1. Radio partition methodology

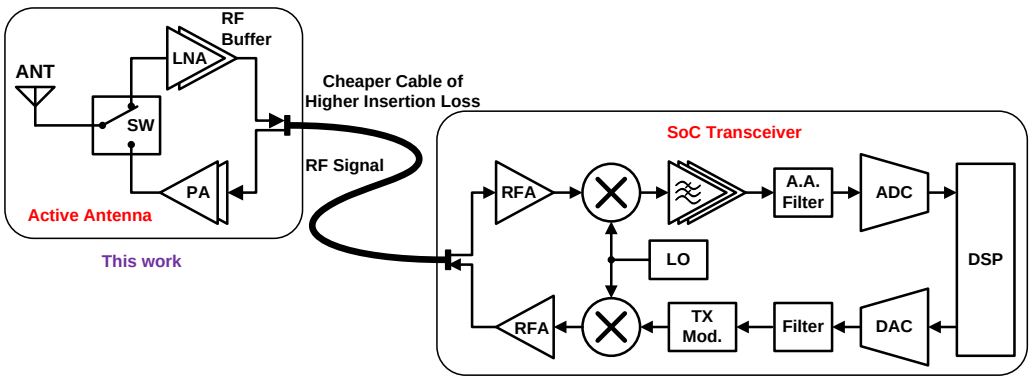


Figure 5.1: Radio partition methodology: Features of a separated CMOS-FEM

This work proposes a novel methodology for partitioning and developing RF/analog radio transceivers for rapid time to market with low manufacturing cost for SoC integration. It places the RF front end module (RF-FEM) external to the remaining analog/mixed signal radio transceiver in an SoC. The RF-FEM can be implemented in technology most suitable for the application and can be co-designed with an antenna for the best performance and lowest cost as shown in Fig. 5.1. The RF-FEM IP can be reused for many SoC technology nodes. The analog/mixed signal transceiver for SoCs can be designed to be reconfigurable for different standards and usage models.

Fig. 5.1 shows the key ideas of the separated CMOS RF-FEM. Expensive RF cables from the antenna to the RF front end can be replaced by cheaper RF cables with higher insertion loss. This is acceptable as the active antenna provides gain to the signal in Rx (Tx) before (after) it passes through the lossy cable. This RF partition also ensures that different RFFEMs placed separately on different dies suffer from less spatial interference among them. One possible top level implementation of the antenna integrated RF-FEM is shown in Fig. 5.2. FEM, co-designed with antenna feeds the antenna directly without using any expensive RF cables.

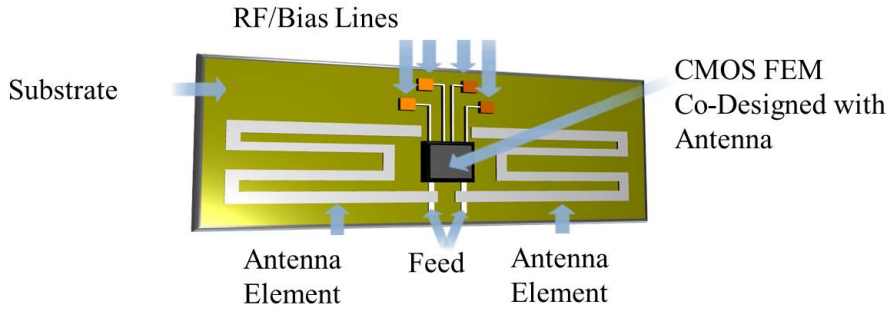


Figure 5.2: Antenna integrated FEM

Fig. 5.3 shows the top level schematic of a wireless system with the new radio partition methodology. The digitally dominated SoC transceiver can leverage the advantages of the technology scaling without waiting for the RF models during the technology development. The CMOS FEM can be on relatively older technology node with well-developed RF models. For millimeter wave applications, the antenna can be on silicon making the CMOS FEM completely on a single die. Interference between the digital engines (clock) and the RF can also be reduced spatially. One reconfigurable TRx in the SoC can be reused for different standards with different RE-FEMs. Thus this solution results in less active area.

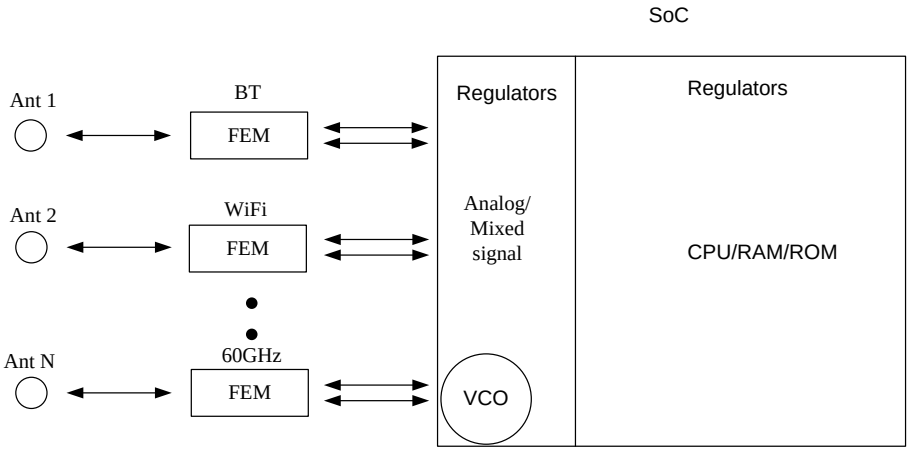


Figure 5.3: Antenna and FEM co-designed, FEM can be on an older technology node while SoC can scale down aggressively with new technology nodes using speculative models for analog/mixed-signal/digital designs

5.2.2. Matching circuits in a radio transceiver

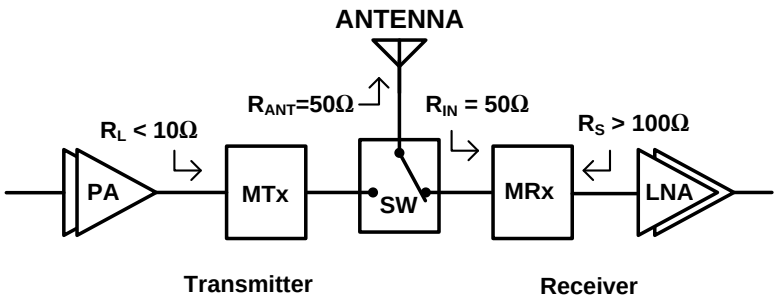


Figure 5.4: Conventional radio front-end

Fig. 5.4 shows a conventional radio-front end with Power amplifier (PA) and its matching network (MTx), low noise amplifier and its matching networks (MRx). Without the matching network (MTx) between PA and the antenna (50Ω load), the PA needs to have a 20V peak to peak swing across its load to deliver 1W of power to RANT. It is not practical and the sub-micron CMOS cannot support such a large swing due to break down issues. Thanks to the matching networks, high power can be delivered to the antenna by impedance transformation through a matching network. Typical matching networks are transformers, low-pass LL Low-Hi matched network (Fig. 5.5), High-pass LL Low-Hi matched network (with interchanged capacitors and inductor locations in Fig. 5.5) etc. These matching networks transform the 50Ω antenna impedance to less than 10Ω (low-pass LL Low-Hi) and greater than 10Ω (High-pass LL Low-Hi). With effective load $R_L < 10\Omega$, PA needs less than 5-V p-p to deliver 1W of power to the antenna (assuming lossless matching networks). In case of transformers, the turn ratio between the primary and secondary coil decide

the impedance transformation.

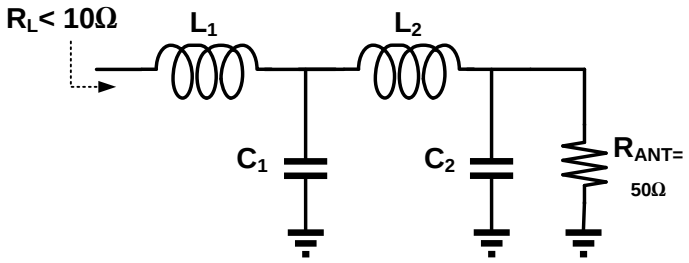


Figure 5.5: Low-pass LL Low-Hi matched network for PA antenna interface

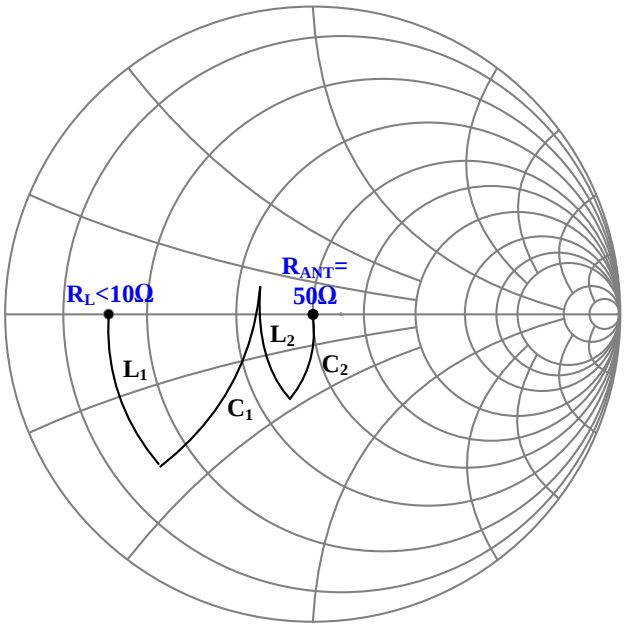


Figure 5.6: Impedance transformation by the matching network in Fig. 5.5. $R_L < 10\Omega$ is the effective load seen by the power amplifier in Fig. 5.4 after interposing a matched network between PA and R_{ANT}

Fig. 5.5 and Fig. 5.6 show the matching network and the corresponding impedance transformation for the PA antenna interface. On the smith chart it can be noticed that the 50Ω antenna impedance is transformed to 10Ω by the matching network in Fig. 5.5. Most of these matching networks are passive and employ inductors. Inductors do not scale down with technology and their quality factor is getting worse with the sub-micron technologies due to the process optimized for digital devices and substrate conductivity. Depending on the frequency of operation these inductors can also be bulky (for low frequency transceivers). Thus these matching networks are bulky and lossy. The loss in the matching network for PA-Antenna interface could be between 0.5 to 1.5dB. This loss degrades the power added efficiency (PAE) of the PA and the peak RF power transmitted by a lot. For example a loss of 3dB in the matching network mean half of the RF power transmitted is dissipated in the matching network.

Thanks to the radio partitioning, the separated CMOS FEM can be on an older and matured CMOS process with developed RF models. This matured process can support better inductors. Nevertheless the problem should be solved through design innovation rather than purely depending on the process. So in this work we propose a CMOS FEM with no MTx (see Fig. 5.11, will be discussed in the section 5.3). By removing the MTx, the loss associated in the MTx is also avoided. Thus high PAE numbers on a small form factor for PA can be achieved.

On the Rx side, the function of the matching network, MRx is to transform the impedance in such a way that the impedance seen by the antenna looking into the MRx should be 50Ω for maximum power transfer and best sensitivity. Another way of interpreting the function of MRx is, looking at the antenna through MRx from LNA transforms the R_{ANT} to conjugate match the input impedance of the LNA. If LNA were common source, its input impedance would be high for CMOS gates. So

MRx transforms the R_{ANT} to high impedance. This transformation is shown in Fig. 5.7 and Fig. 5.8. R_{ANT} transforming to high impedance also benefits the NF which can be seen from Fig. 5.9 and Eq. 5.1.

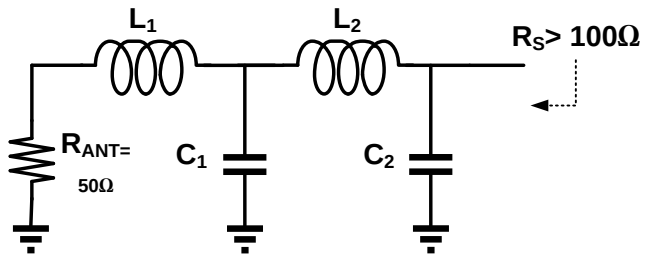


Figure 5.7: High-pass LL Low-Hi matched network for LNA antenna interface

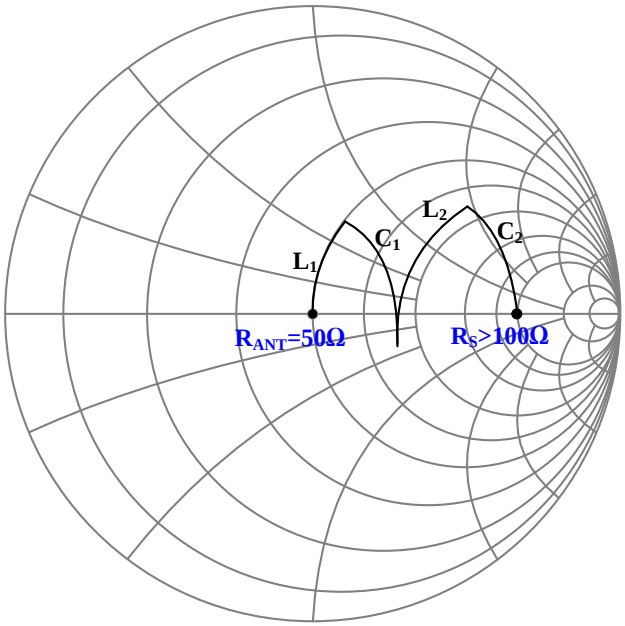


Figure 5.8: Impedance transformation by the matching network MRx shown in Fig. 5.7

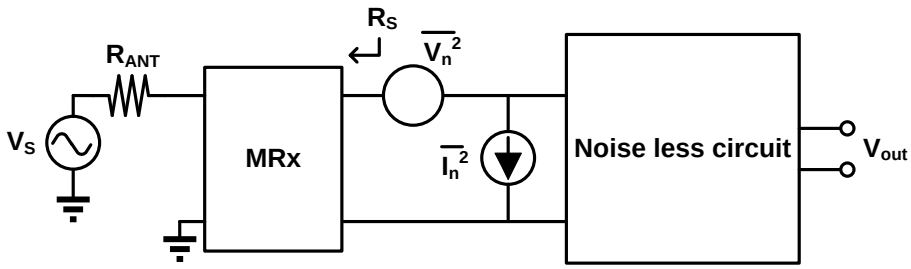


Figure 5.9: Rx front-end with matching network MRx

Noise Factor for the circuit in Fig. 5.9 is given by (assuming V_n and I_n are not correlated)

$$\begin{aligned} F &= \frac{4KTR_S + \overline{(V_n + I_n R_s)^2}}{4KTR_S} \\ &= 1 + \frac{\overline{(V_n + I_n R_s)^2}}{4KTR_S} \end{aligned} \tag{5.1}$$

Now if R_S is high then the noise factor is less and that transformation is done by the matching circuit MRx. It is quite relevant to mention that most of the matching networks for MRx employ transformers and/or inductors. The quality factors associated with these inductors are less and thus there is a limit on the impedance transformation ratio beyond which the loss in MRx offsets the advantages of impedance transformation by adding more signal loss.

So from the above discussion it can be concluded that the PA needs low load impedance for effective power transfer to load with low voltage swings and the LNA prefers to have high source impedance to have better NF and sensitivity.

5.3. Radio Co-design

5.3.1. Breaking 50Ω barrier

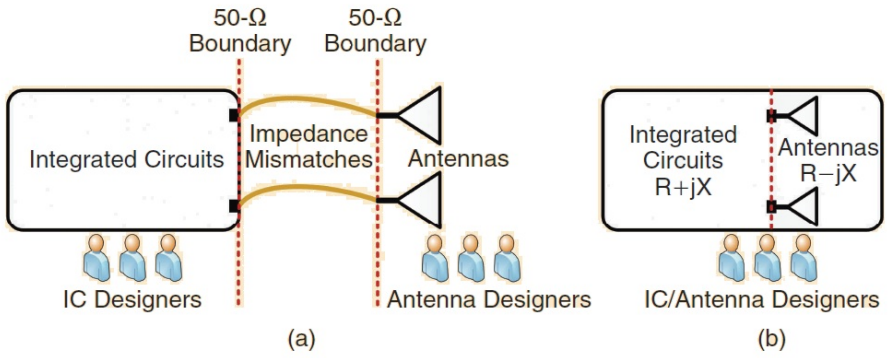


Figure 5.10: Co-design: (a)traditional 50Ω boundary between IC designers and antenna designers (b)conjugate matching between IC and onchip/onboard antennas [76]

Matching is a standard RF design procedure considering phase delay. RF designers match the input and output to known impedance (mostly 50Ω) so they can design blocks independently, knowing that they will work correctly when hooked up with each other. A matched transmission line can be inserted in between RF blocks without the standing wave issue. Theoretically, radio performance could be improved by utilizing mismatch into design. But there will be some difficulty in block-level testing (e.g. noise figure, matching) as most of the standard measurement instruments are 50Ω matched. In co-design, optimization usually involves the interaction of stages and requires more knowledge, and may take longer to design. When RF blocks are physically close ($< \lambda/20$) to each other (e.g. LNA and Mixer), design with lump-circuit model is more practical. Impedance matching is redundant at this

point. Deliberate and full-customized design is necessary. New design guidelines need to be developed in this direction to get the best performance from the radio through co-design methodology.

Co-design of RF front-end along with the antenna gives many benefits without the constraint of 50Ω boundary condition. By removing this constraint, new antenna with better efficiency can be implemented. This gives scope to choosing the proper impedance for Rx/Tx efficiency. Fig. 5.10 [76] shows the traditional 50Ω boundary condition between IC designers and antenna designers. It can also be seen that the co-design can remove this boundary and choose the impedance for antenna desired by Tx/Rx for better efficiency.

Another great advantage of antenna and FEM co-design is the elimination of the matching networks. For example Antenna can be designed to have 10Ω impedance and remove the MTx matching network between PA and the antenna. Thus the entire loss associates with the matching network, MTx can be avoided and the PA can deliver to the 10Ω load more efficiently. This improves the PAE and the peak RF output power. This saves the valuable silicon area by avoiding the bulky inductors in the matching networks.

From the discussion in the section 5.3 it can be concluded that PA desires to see low impedance for antenna for the Tx efficiency whereas the LNA desires to high input impedance for antenna. Unless two separate antennas are employed for Tx and Rx it is impossible to achieve two different input impedance for antenna at the same frequency. As PA is the most power consuming block in the entire transceiver, in the proposed implementation, the input impedance of the antenna (Z_{ANT}) is chosen to be less ($\approx 10\Omega$) so as to improve the PA efficiency. This would impact the NF of the LNA but a matching network and proper design in the LNA made its NF to be less than 3dB.

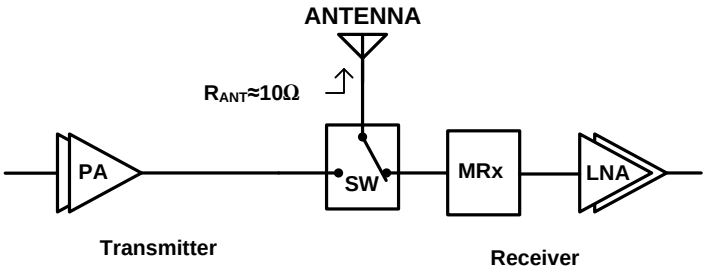


Figure 5.11: Co-designed antenna CMOS-FEM with no matching network(MTx) between PA and antenna

Fig. 5.11 shows the co-designed Antenna-FEM block with no matching network between PA and the antenna. 50Ω boundary is removed between the RF IC and the antenna.

5.3.2. Advantages of RF-FEM-antenna co-design

The cost of RF cables, baluns, filters and front end modules can be >\$5 in notebook MIMO radios, and are simplified or eliminated at a much lower cost with an external RF-FEM co-designed with the antenna. Today, cables, baluns and switches attenuate radio signals by 3-5dB, degrading sensitivity, increasing power consumption and creating additional heat from power amplifiers that must deliver additional power to overcome these losses. Because the RF-FEM is external to the SoC, a lower cost, more suitable technology can be used, such as 90nm CMOS, which is much less expensive\mm^2 than highly-scaled technology.

Furthermore, existing RF-FEM components and layouts that have been characterized can be re-used for shorter development time and lower development cost. Process enhancements, such as thick metal to improve power amplifier efficiency, can be employed in a cost-effective way if needed. RF-FEM-antenna co-design results in

lower cost and better RF performance. Co-design of the RF-FEM with balanced antennas reduces power dissipation and platform noise. Antennas can be designed with complex impedances as part of the PA and LNA matching networks, and with filtering characteristics to improve performance while lowering cost. RF-FEM-antenna co-design capitalizes on and extends recent radio and antenna research, and accelerates flexible multi-com architecture implementation in notebook, MID and smart phone platforms.

5.4. Transmitter: Power Amplifier

5.4.1. Class D PA

Radio frequency power amplifiers require matching networks to efficiently transfer RF power at transistor output to antenna port. This process is an impedance transformation in RF domain, which converts standard load impedance (50Ω in most of applications) to a low impedance at transistor output for generating high RF output power. However, this output matching network is lossy and bulky, especially when it is integrated on wafer. Usually the higher impedance transformation ratio leads bigger loss of the matching network. However, higher impedance transformation is required for high output power or low power supply voltage. This exhibits challenges to design highly efficient integrated high power PA. It is especially true for CMOS due to low breakdown voltage and mediocre quality passive components. As a result, mobile platform manufactures have to use high cost external PA module for high power application (eg. LTE/WiMax) and suffer efficiency (battery life) trade-off using integrated PAs for some low RF power wireless application (eg. WiFi, Bluetooth). The standards with high peak to average ratio like WiFi, Wimax and LTE requires high output power while maintaining high efficiency at power back-off.

Several techniques have been proposed in the literature to address the needs for

efficiency and SoC integration. Digital pre-distortion [77] improves the efficiency of the PA by allowing operation at a smaller back-off and linearizes the mildly non-linear power amplifier through DSP. To maintain optimum efficiency in the PA, Envelope tracking (ET) techniques can be used to adjust the power supply of a linear PA [78]. In an Envelope Elimination and Restoration (EER) transmitter [79], an efficient switching PA is used to process the phase information, while the amplitude is introduced via supply modulation. In out-phasing architectures [80–88], the PA input signal decomposes into two constant amplitude components that are efficiently processed through switching power amplifiers whose outputs are then combined together.

Out-phasing PA technique is promoted as one of advanced techniques to enhance power efficiency at back-off [86] and lower cost (no input/interstage matching networks required). Outphasing transmitters [80, 81] decompose the desired RF signal signal ($x(t) = a(t)cos[\omega t + \varphi]$) with amplitude $a(t)$ and phase information (φ) into two constant-amplitude (digital) signals S_1 and S_2 with only phase modulation.

$$S_{1,2} = Acos[\omega t \pm \theta(t) + \varphi] \tag{5.2}$$

where $\theta(t)$, the out-phasing angle, is obtained as

$$\theta(t) = cos^{-1}[\frac{a(t)}{2A}], \text{where} A = max[\frac{a(t)}{2}] \tag{5.3}$$

Since the amplitude information of the original signal is transformed into the phase domain, the resulted out-phasing signals can be processed or amplified with high-efficiency nonlinear switching power amplifiers. A class-D PA is a switched mode PA which is typically configured as an inverter. The overlap of the voltage and current

waveforms of each transistor in a class D is minimum resulting in a high efficiency. The vector sum of the two PA outputs will follow the desired signal amplitude. However, the power combiner required in the out-phasing system still takes significant area in the design. Reducing loss in power combiner is also highly desired for wireless mobile platform.

5.4.2. Power combiner

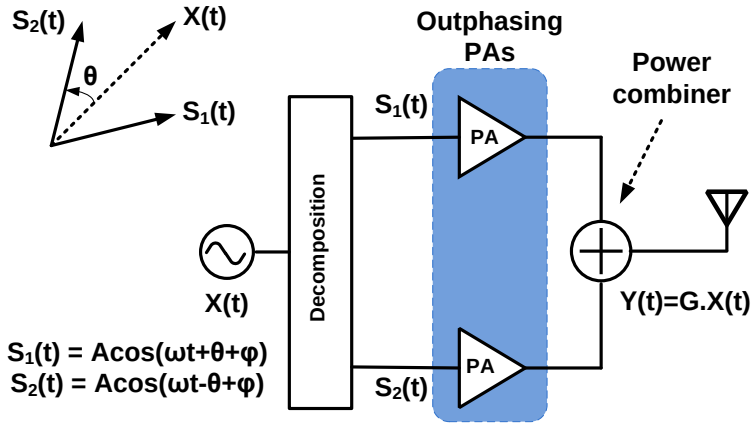


Figure 5.12: Traditional outphasing system

Fig. 5.12 describes a typical out-phasing system. It usually requires two switched-mode power amplifiers and a power combiner. This power combiner can be either isolating (e.g., Wilkinson) or non-isolating combiner [80] that combines the two constant amplitude signals. An isolating combiner [85, 87, 88] achieves good linearity due to the lack of interaction between the two PAs, but has poor average efficiency, since it draws constant supply current regardless of the amplitude of the output RF signal. A non-isolating combiner, on the other hand, introduces interaction between the two PAs and the currents flowing are a function of the output RF signal. Thus it

results in reduced power dissipation for small output amplitudes, improving back-off efficiency. This PA interaction, however, can degrade linearity [89].

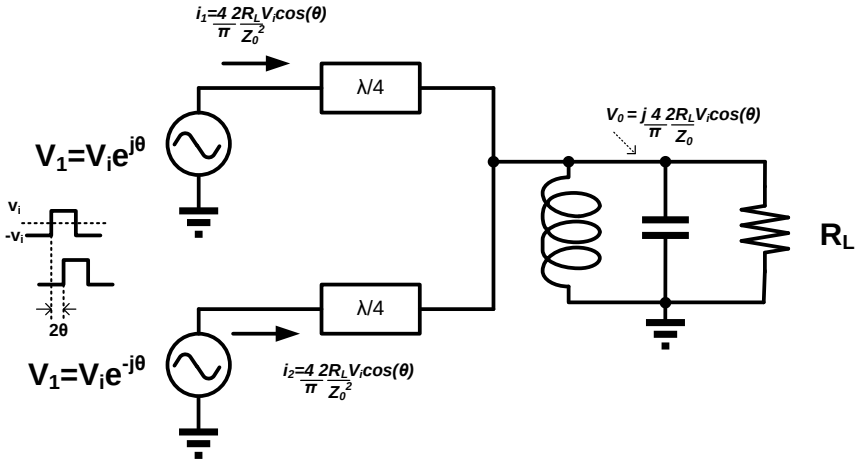


Figure 5.13: Traditional outphasing PA with $\lambda/4$ combiner

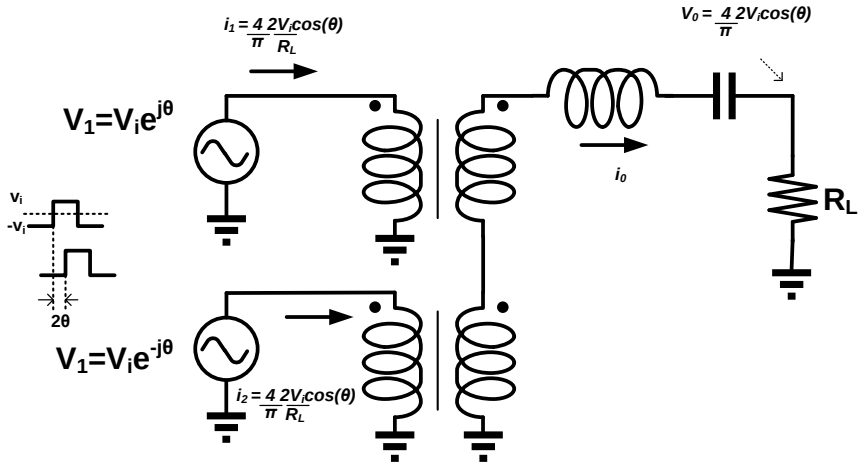


Figure 5.14: Traditional outphasing PA with transformer combiner

Fig. 5.13 and Fig. 5.14 shows two ways of non-isolating power combining to improve the back-off efficiency. In Fig. 5.13, the out-phasing signals are combined by $\lambda/4$ combiner. In Fig. 5.14, a transformer is employed to combine the amplified out-phased signals. The $\lambda/4$ transmission lines convert out-phasing voltage signals $V_i e^{\pm j\theta}$ to current signals $-jV_i e^{\pm j\theta}/Z_o$. These currents flow to a common load $\mathrm{R_L}$ and generate output voltage V_o

$$V_o = -j\frac{4}{\pi}\frac{2R_L V_i cos(\theta)}{Z_o} = -j|V_o(\theta)| \tag{5.4}$$

where $\frac{4}{\pi}$ is the coefficient of the fundamental component of a square-wave, and Z_o is the characteristic impedance of the $\lambda/4$ transmission line. Phasor representation of the output voltage at fundamental frequency is shown in the above equation. As shown in Fig. 5.13, the current signals are proportional to $cos(\theta)$, and therefore the instantaneous output voltage($i_1(\theta) = i_2(\theta) = (jV_o(\theta))/Z_o = |V_o(\theta)|/Z_o$). This results in reduce power dissipation when delivering small output amplitude, and therefore improved back-off efficiency compared with the isolating combiner case.

Similar analysis on the transformer combining in Fig. 5.14 show that the output voltage is

$$V_o = \frac{4}{\pi}2V_i cos(\theta) \tag{5.5}$$

Output voltage and the currents in the transformer are proportional to $cos(\theta)$ which validates the out-phasing summation property and non-isolating power combining property of the transformer combiner.

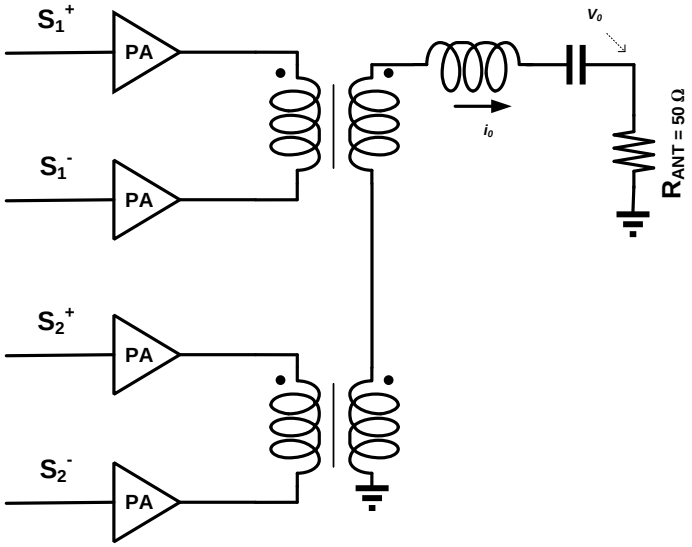


Figure 5.15: Outphasing class-D CMOS PA (fully differential) with transformer combiner

Fig. 5.15 is differential implementation of out-phasing system which has many advantages [35, 87]. On-die transformer combiner is usually used in integrated outphasing power amplifier for this purpose. However, it takes significant die area. Using off-chip power combiner will also introduce additional BOM cost.

5.4.3. Spectral power combination

In this section, a technique to implement out-phasing power combining through dipole antenna is proposed. This technique can also remove on die inductors/transformers. This kind of power combination through the dipole antenna is a non-isolating type as there is an interaction between the two PAs (through the antenna) and the power flowed (radiated) through the combiner (here, antenna) is a proportional to the output RF power. This technique can significantly reduce die area (by as much as 90%) and generate high efficiency.

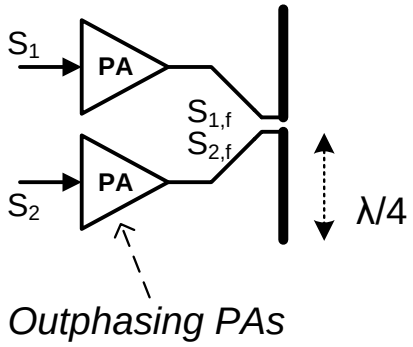


Figure 5.16: Proposed outphasing system combining through half-wave dipole antenna

The proposed approach is to eliminate on-chip or off-chip power combiner components, and merge the functions of out-phasing combiner and antenna together. This solution is shown on Fig. 5.16. A dipole antenna is used to be connected directly to two out-phasing PA branches, working as an out-phasing combiner. This can significantly reduce the die area. In addition to the cost saving, the insertion loss of on-die/off-die combiner is also reduced from the out-phasing system. Antenna input settings for peak and min powers for the half wave dipole antenna are shown on Fig. 5.17 and Fig. 5.18.

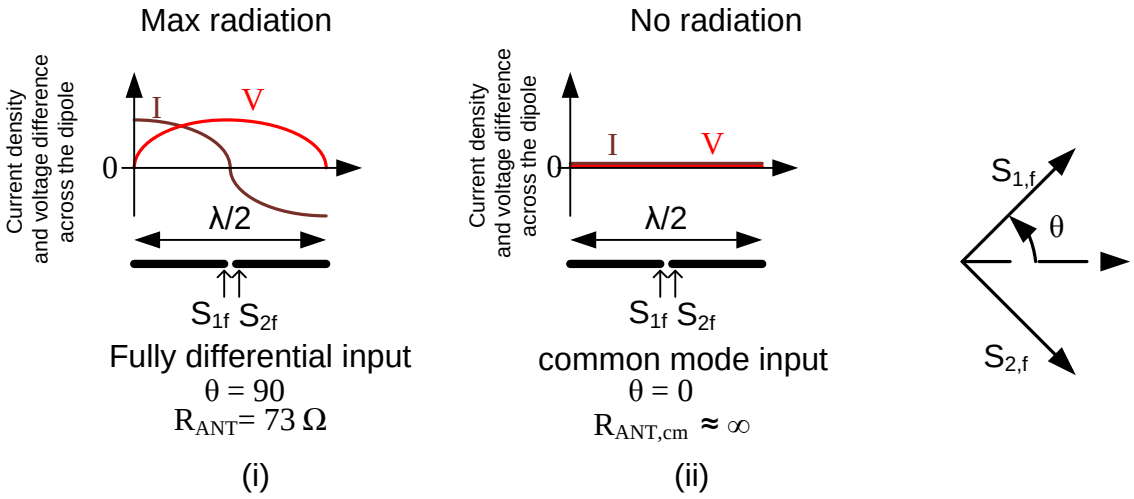


Figure 5.17: Current density and voltage difference across the half wave ($\lambda/2$) dipole antenna in (i)differential and (ii)common-mode operation

$S_{1,f}$ and $S_{2,f}$ are the fundamental components of the amplified out-phasing signals (S_1, S_2). Let

$$S_{1,f} = Acos(\omega t + \theta)$$
$$S_{2,f} = Acos(\omega t - \theta) \tag{5.6}$$

Where θ is the out-phasing angle as defined. Both the out-phasing signals can be decomposed into differential and common mode signals as below

$$S_{1,f} = \frac{S_{1,f} - S_{2,f}}{2} + \frac{S_{1,f} + S_{2,f}}{2}$$
$$S_{2,f} = \frac{S_{2,f} - S_{1,f}}{2} + \frac{S_{1,f} + S_{2,f}}{2} \tag{5.7}$$

Now the fundamental component of the differential ($S_{d,f}$) and common-mode

($S_{cm,f}$) input signal to the antenna is

$$S_{d,f} = S_{1,f} - S_{2,f} = -2Asin(\omega t)sin(\theta)$$
$$S_{cm,f} = S_{1,f} + S_{2,f} = 2Acos(\omega t)cos(\theta) \tag{5.8}$$

Half wave ($\lambda/2$) dipole antenna is an example of resonance antennas. Typically it achieves a differential impedance of zero reactance and 73Ω resistance at resonance for simple structures like the one shown in Fig. 5.16 [90, 91]. The input resistance is also called as radiation resistance. In ideal conditions common mode signal sees infinite impedance with zero current density and zero radiation. Voltage and current density distribution in a dipole antenna is shown in Fig. 5.18. Now the power radiated by the antenna in differential $P_{d,f}$ and common mode $P_{cm,f}$ is given by

$$P_{d,f} = \frac{S_{d,f,rms}^2}{R_{ANT}} = \frac{2A^2sin^2(\theta)}{R_{ANT}}$$
$$P_{cm,f} = \frac{S_{cm,f,rms}^2}{R_{ANT}} = \frac{2A^2cos^2(\theta)}{R_{ANT,cm}} \approx 0 \tag{5.9}$$

Thus the power is scaled as a function of $sin^2(\theta)$ which is in agreement with Fig. 5.19 and Fig. 5.20. (In transformer and transmission line combiners it is a function of $cos^2(\theta)$ as shown previously see Fig. 5.13 and Fig. 5.13). Thus the dipole antenna can be used as a power combiner in class D PAs.

Fig. 5.18 explains the mechanism of out-phasing combining through a half wave dipole antenna (see, Fig. 5.12). For this dipole antenna, when the two driving signals S_1 and S_2 are anti-phase (180 degree), the antenna provides the desired impedance to PAs for peak power radiation. When signals S_1 and S_2 are in-phase (0 degree), the antenna shows an open circuit (very high impedance) at PA output for minimum radiation. In anti-phase, the input impedance of the antenna is the radiation resistance

of the half wave dipole which is close to 73Ω [90, 91]. But a load resistance of 73Ω is too high for an efficient power transmission for the PA. So through miniaturization in the antenna (discussed later in the section 5.7 on antenna design), the radiation resistance of the half wave dipole is decreased close to 10Ω which is the desirable load for the PA (through load pull simulations) for its maximum efficiency and peak RF output power.

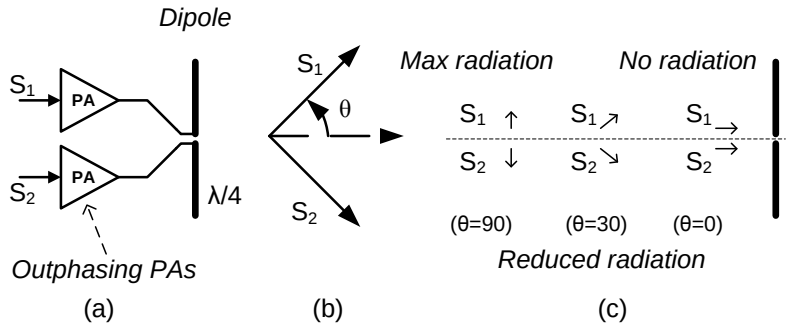


Figure 5.18: Mechanism of outphasing combining through half wave dipole antenna: (a)proposed power combination through dipole antenna (b)outphasing angle(θ) (c)radiation vs. θ

To prove the concept of out-phasing and spectral combination through a dipole antenna some EM/circuit simulations are performed. Fig. 5.19 shows simulated normalized radiated power as a function of out-phasing angle on a dipole antenna design. It matches perfectly with the out-phasing theory. An out-phasing PA system (with realistic RF switch model having ON resistance of $R_{on} = 25 \approx 30\%$ of R_L (load resistance) is also modeled together with a dipole antenna. Fig. 5.20 and Fig. 5.21 presents the linearity and efficiency of the proposed spectral combination system. The whole system presents good linearity and promising PA efficiency.

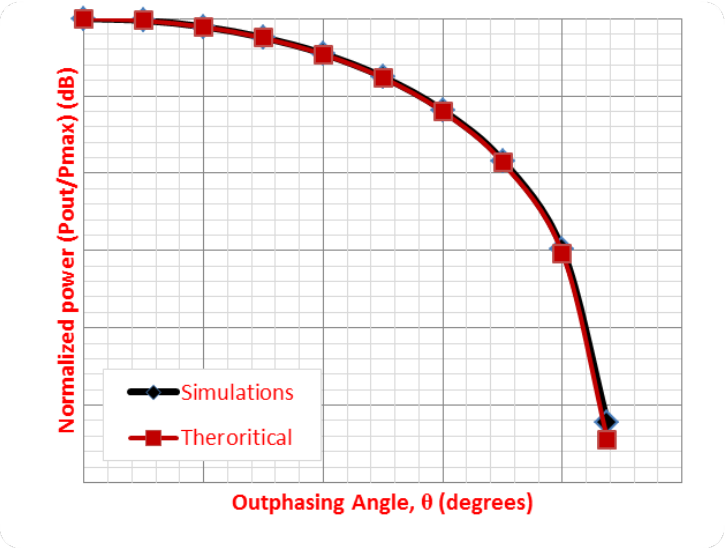


Figure 5.19: Normalized radiated power vs. outphasing angle

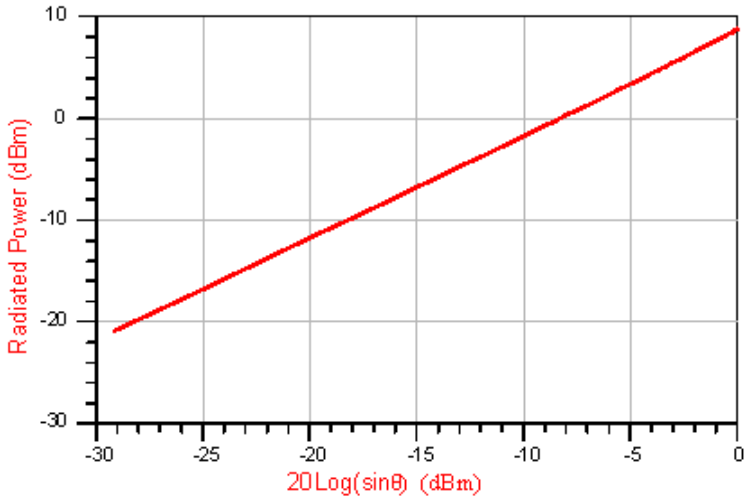


Figure 5.20: Normalized radiated power vs. outphasing angle in log-scale showing good linearity

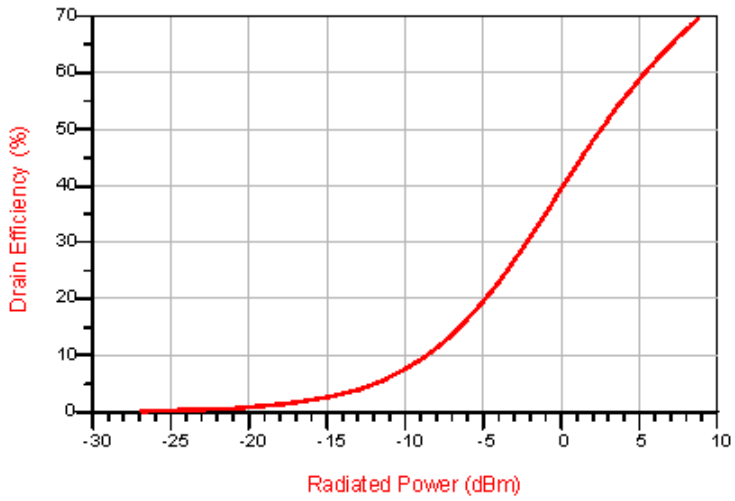


Figure 5.21: Drain efficiency vs. radiated power

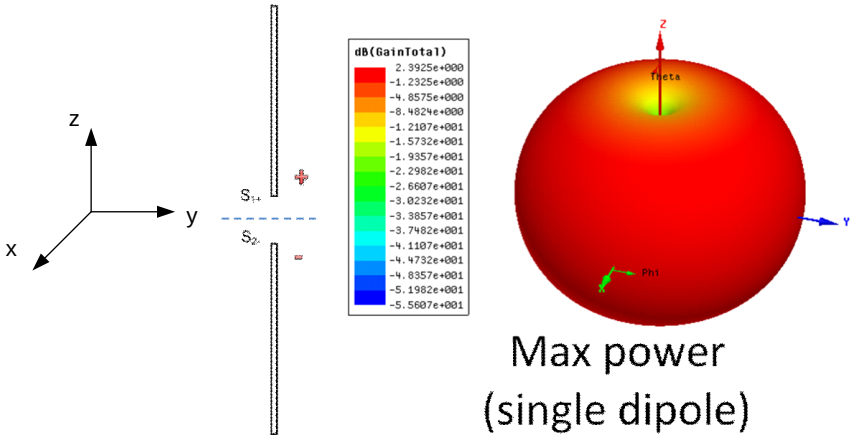


Figure 5.22: Radiation pattern at maximum output power, $\theta = 90°$

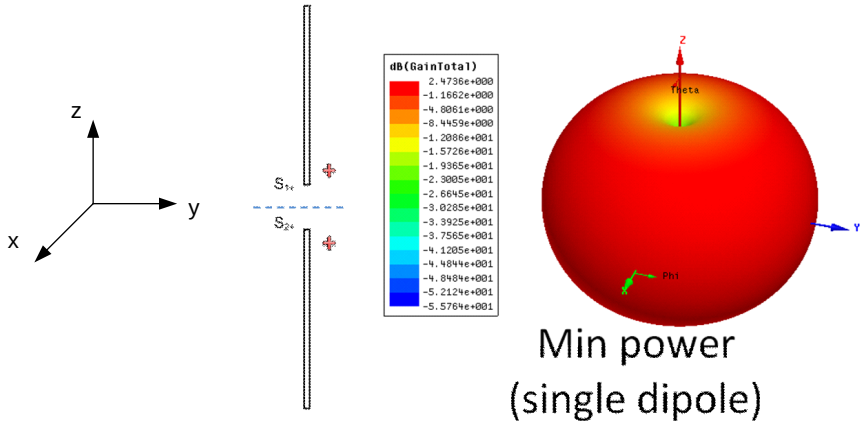


Figure 5.23: Radiation pattern at minimum output power, $\theta = 0°$

In order to guarantee modulated signals can be received in all directions, antenna has to have a good out-phasing linearity in all radiating directions. For this case, radiation pattern has to be maintained with all out-phasing angles. Fig. 5.22 and Fig. 5.23 shows the radiation patterns of peak and minimum power cases. Antenna actually shows identical patterns regardless of out-phasing angles which is desirable. Fig. 5.24 shows the schematic the class D PA cell. The supply voltage is doubled by employing cascode transistors so as to increase the peak RF power of the PA.

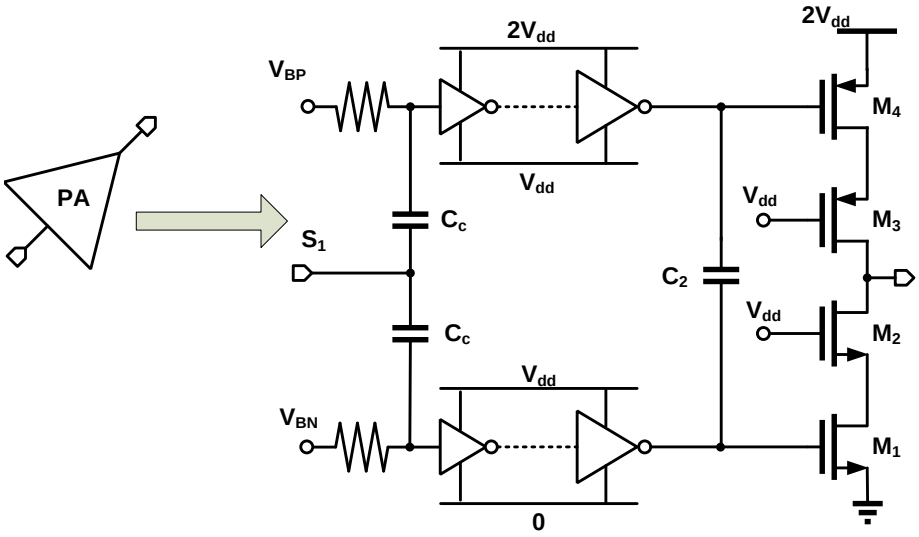


Figure 5.24: Simplified schematic of the class-D PA

5.5. Transmit/Receive (T/R) Switch

5.5.1. Introduction & existing solutions

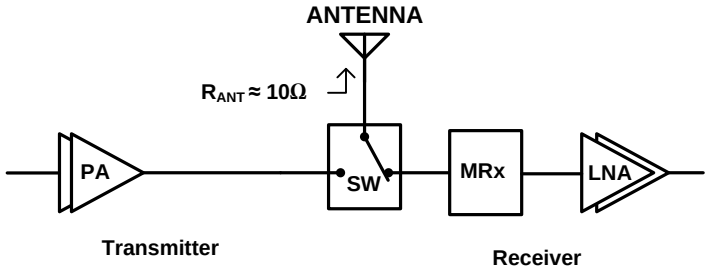


Figure 5.25: Co-designed antenna CMOS-FEM with integrated T/R switch

In the previous section, the matching network between the PA and the antenna and thus its associated losses are removed by taking advantage of the co-design as shown in Fig. 5.25. Optimum antenna impedance was chosen to get the best PAE. The other lossy block between PA and antenna is the Transmit/Receive (T/R) switch. T/R switch is very important circuit block as its efficiency directly affects the performance of the Tx and Rx.

A high quality Transmit/receive (T/R) switch is a key building block for a radio frequency front end. An Ideal (T/R) switch should have low insertion loss, high linearity, wide bandwidth, high power handling capability and high isolation. CMOS has become very promising with its ever shrinking process and scaling friendly for RF, IF and baseband blocks on the same die. Designing a highly linear, efficient T/R switch on an advanced CMOS is challenging due to low device breakdown, low mobility, high substrate conductivity and various parasitics of CMOS process. A typical lossy T/R switch introduces loss on both receiver (Rx) and transmitter (Tx) chain as turning on one or the other. These losses degrade overall power efficiency and noise figure. Usually large devices with low on resistance (RON) are used. It sometimes requires thick gate or cascode devices to have better isolation and good power handling capability [92]. Fig. 5.25 shows the function of the T/R switch in a CMOS-FEM. In Rx mode, the T/R switch connects the receiver to the antenna while showing high impedance to the Tx path. In Tx mode, it connects the transmitter to the antenna while disconnecting the receiver.

The authors in [93] demonstrated a floating body technique but the reported P1dB is only 20dBm, which is not sufficient to meet many standards like WiFi etc. Besides the insertion loss is more than 1dB and switch is not an integrated solution. Another standalone solution from the authors in [94] showed the need for a high impedance substrate achieving an insertion loss of more than 1.5dB in Rx and Tx

modes. Authors in [95] demonstrated an integrated solution but the insertion loss of the T/R switch in Tx mode is 1.8dB which is very undesirable and significantly degrades the efficiency of the PA. Besides the solution also showed only 15dB isolation to the Rx in transmit mode which significantly compromises the reliability of the devises in the LNA. LNA typically employs thin gate devices for better performance.

The current solution in industry is using T/R switch off-chip with different technology like Gallium Arsenide (GaAs) Metal-Semiconductor Field Effect Transistors (MESFETs) or High-Electron-Mobility-Transistors (PHEMTs). This makes the solution very expensive. There are some on chip CMOS solutions most of which employs thick gate transistor switches with remote body contacts, as in Fig. 5.26. Thick gate transistors are lossy and the performance of these solutions is very mediocre and is not good for many standards.

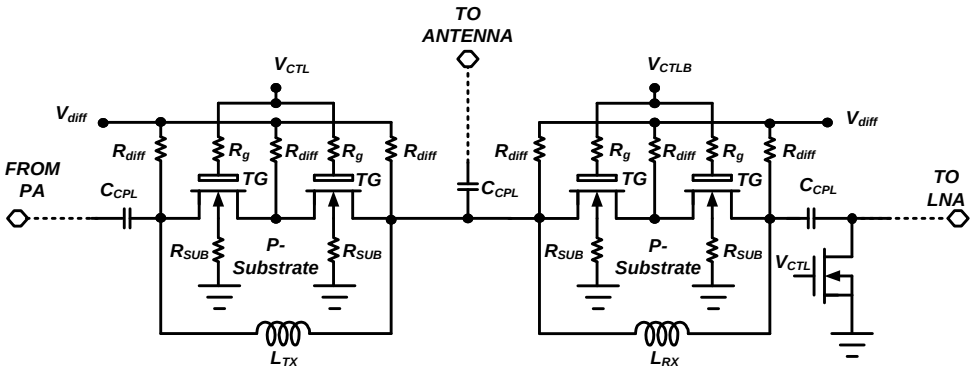


Figure 5.26: CMOS T/R switch with remote body resistance [92]

Fig. 5.26 shows the schematic of an integrated Single Pole, Double Throw (SPDT) CMOS T/R switch which consists of two switch units. The two switch units include an Rx switch and a Tx switch. V_{CTL} controls the mode of operation. It employs

thick gate (TG) transistors as switches to achieve high breakdown voltages. On the LNA side it has a shunt transistor to improve the isolation (attenuation) from PA to LNA. Inductance of the Inductors L_{TX} and L_{RX} are used to resonate out the parasitic capacitance of the switches. The use of remote body contacts for the TG transistors may allow the body to be bootstrapped to improve the power handling capabilities of RF switch. Although TG transistors can handle moderately large powers they are lossy devices which decrease the performance of the transceiver. Linearity is also a big concern in these types of T/R switches as it is limited by the nonlinear transistors. Large parasitic capacitors associated with these bulky TG transistors degrade the Noise, linearity and Isolation performance of the switches. This directly degrades the performance of the transceiver. So the authors in [92, 96] proposed a substrate isolation technique through layout (Remote body resistance) which enhances the power handling capability of the transmit side switch and also reduces the insertion loss. The measured insertion loss is approximately 0.1dB in the Rx mode and approximately 0.4dB in the Tx mode.

Another contribution of this research is a new circuit topology for a Radio Frequency (RF) Transmit/Receive (T/R) switch which multiplexes the antenna to a Low Noise Amplifier (LNA) or multiplexes the antenna to a Power Amplifier (PA) in an antenna, PA, LNA and T/R switch co-design system. The proposed RF switch is fabricated in CMOS technology with the transmitter and receiver to provide a completely integrated radio. The two novel ideas in the proposed T/R switch can be described as follows. 1) The proposed solution uses only one transistor switch in a non-invasive style and re-uses some of the components of transceiver circuit to toggle between PA and LNA. 2) Co-design of LNA, PA T/R switch and antenna benefits the proposed idea to be more effective.

5.5.2. Proposed solution: Passive T/R switch

Fig. 5.27 shows the co-designed antenna and radio transceiver with power amplifier (PA) on the transmitter and LNA on the receiver. A CMOS RF switch multiplexes the antenna to LNA or to PA. The shown T/R switch could be a dedicated discrete off chip block or could be on chip.

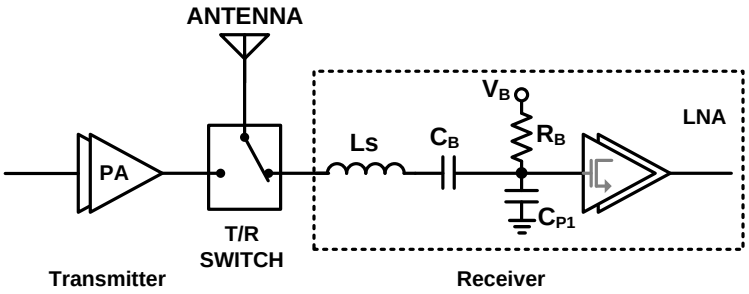


Figure 5.27: Generic RF front-end with T/R switch (matching network, MRx embedded with the LNA)

Typically LNAs use series inductors Ls at the input for input matching, bandwidth extension or to resonate out the input parasitic capacitance C_{P1} as shown in Fig. 5.27. C_B is a DC blocking capacitor and RB is employed to set the DC biasing point of the input transistors in the LNA. CB and RB are usually of big value that set the lower cut off frequency ($1/R_BC_B$) of operation in the in the LNA. At the frequency of transceiver operation CB is typically a short circuit and RB is open. Fig. 5.28 shows the implementation of the RF switch by reusing the inductor L_S and DC coupling cap (C_B) of the LNA circuit. In the proposed solution, the dedicated T/R switch is removed as shown in the figure. A shunt switch (RxSW) at the input of LNA is added which controls the mode of operation of the transceiver.

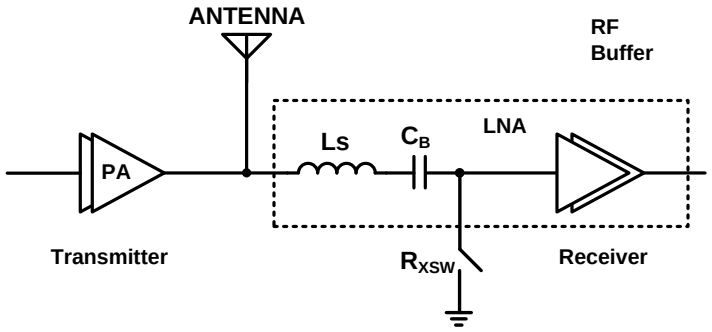


Figure 5.28: Proposed efficient and non-invasive T/R switch reusing the components of matching network, MRx and bias network of LNA

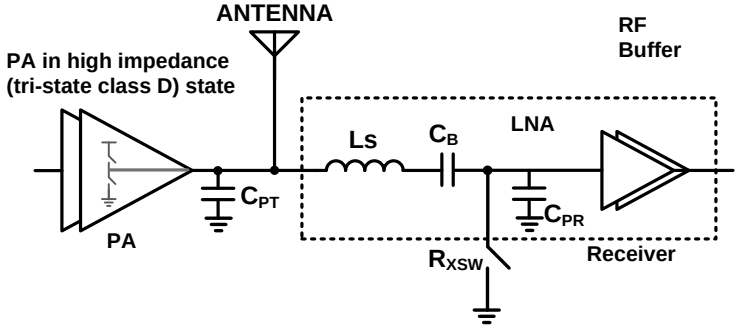


Figure 5.29: Operation of T/R switch in Rx mode

Rx mode: In receiver mode, RxSW is OPEN and PA is in high impedance (tri-state) state as shown in Fig. 5.29. In this mode L_S resonate out the parasitic capacitance C_{P1} (see Fig. 5.30) through series resonance and improves the gain and noise figure of the LNA. Removing the dedicated T/R switch block after the antenna avoids the loss in the T/R switch block and improves the system performance. Since there are no series switches, performance of the LNA improves in sensitivity, noise

figure, linearity and gain. Kick back from the mixer LO can desensitize the receiver. But Isolation is not critical in this implementation as the front end G_m (LNTA) cell is driving a Rx buffer and not a mixer (discussed in the section 5.6 on receiver).

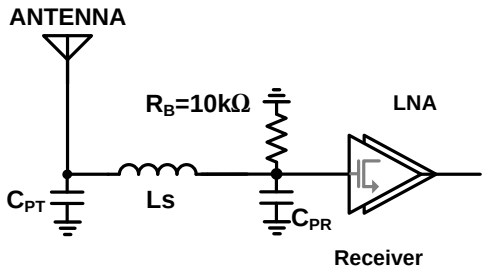


Figure 5.30: Equivalent small signal model in Rx mode

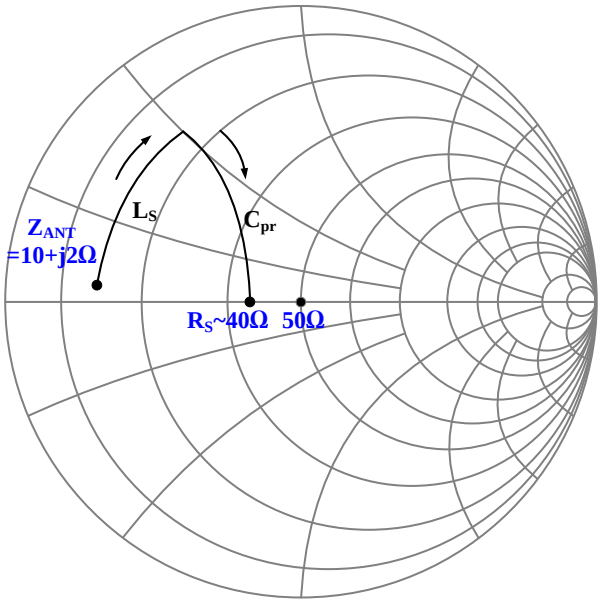


Figure 5.31: Impedance matching for the LNA input

In section 5.2 it is discussed on how matching network at the Rx input improves the NF by transforming the source impedance to high value (see Fig. 5.8), Eq. 5.1). From Fig. 5.30 and smith chart in Fig. 5.31, it can be seen that the inductor, L_S and the parasitic capacitor C_{PR} transforms the low antenna impedance to a relatively higher value improving the effective NF as per Eq. 5.1. The choice of low impedance ($Z_{ANT} \approx 10\Omega$) comes from optimum peak RF power and PAE. The reason for choosing $Z_{ANT} = 10 + j2\Omega$ is discussed in the next section.

Tx mode: Fig. 5.32 shows the transceiver in transmit mode. In this mode of operation, switch RxSW is closed. This makes the inductor Ls in parallel with parasitic capacitor C_{P2}. (C_B is short in the frequency of operation). The parallel Ls resonate out the parasitic capacitor C_{PT} (shunt resonance) and improve the output matching of the PA. Ls also act as high impedance to the LNA. This high impedance ($Z_{rx} = \omega_{RF} L_s$) isolates the LNA from the PA. Inductor being a passive element can with stand high power levels of PA without any break down issues unlike devices used as switches [92]. The shunt switch RxSW also ensures that the signal at the input of LNA is small and protects the LNA without any transistor break downs due to high signal swings that may leak from PA.

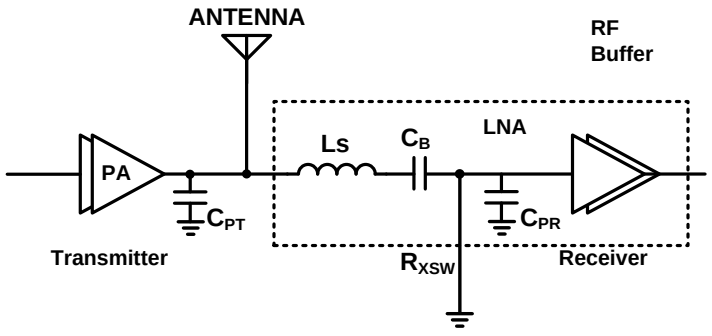


Figure 5.32: Operation of T/R switch in Tx mode

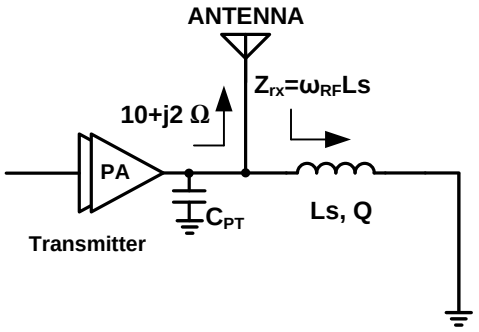


Figure 5.33: Equivalent small signal model in Tx mode, parallel resonance

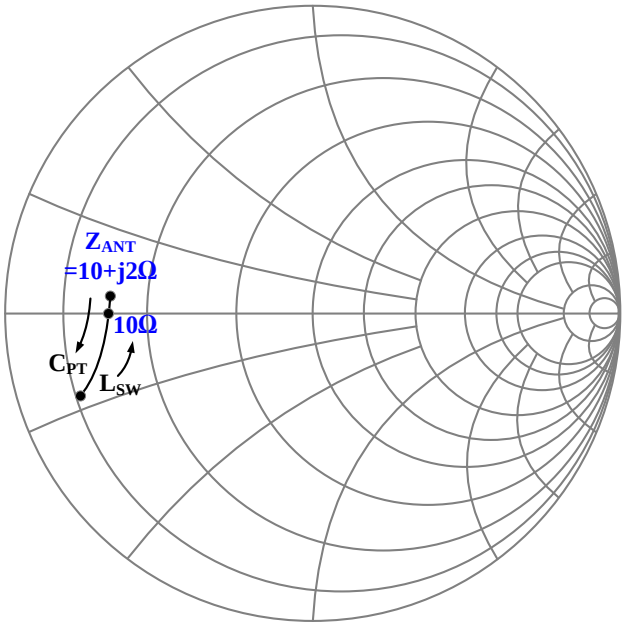


Figure 5.34: Impedance matching for the PA output

From the Rx and Tx modes of operation, it should be observed that a single inductor L_S is not sufficient to resonate out two different parasitic capacitors (C_{PR}

and C_{PT}) at the same frequency. So another parameter is exploited from the antenna design. The antenna is designed to have a $Z_{ANT} = 10 + j2\Omega$. Im(Z_{ANT}) and Ls are two design choices to resonate out the two parasitic capacitors as shown in Fig. 5.31 and Fig. 5.35. From Fig. 5.33 and Fig. 5.31, it can be seen how the shunt capacitor C_{PT} and the shunt inductor (L_S) transform the $Z_{ANT} = 10 + j2\Omega$ to a real 10Ω.

Power loss in the passive T/R switch in Tx mode: Fig. 5.33 is very ideal small signal model. Fig. 5.35 shows a realistic small signal model to find the power loss in the proposed T/R switch.

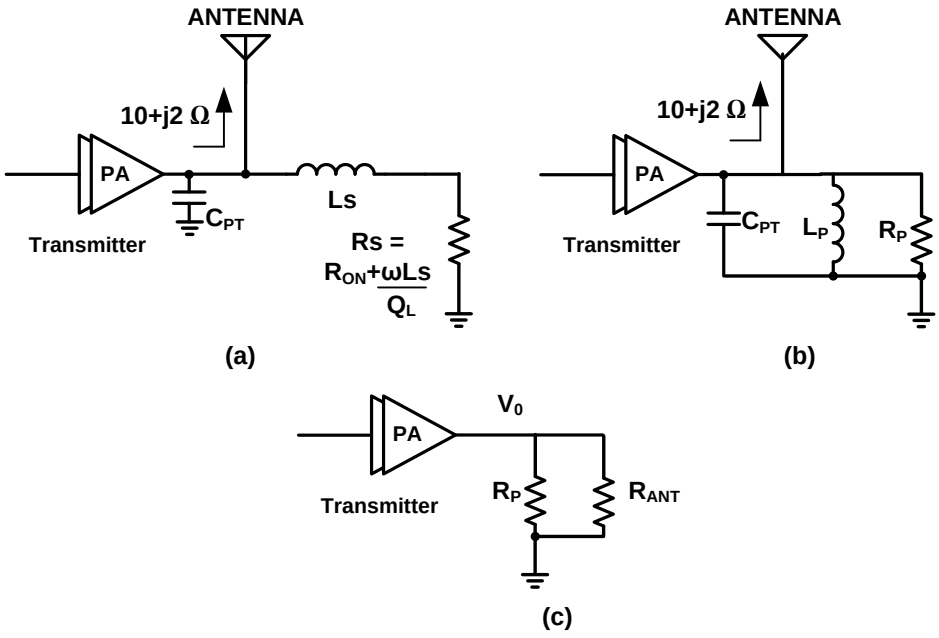


Figure 5.35: Circuit transformation to find the loss in the proposed T/R switch in Tx mode

Resistor R_s is a combination of the ON resistance of the switch and the series resistance of the inductor with a qualitfy factor Q_L.

$$R_S = R_{ON} + \frac{\omega_{RF} L_S}{Q_L} \tag{5.10}$$

Defining new quality factor for the RLC circuit in Fig. 30(a)

$$Q_S = \frac{\omega_{RF} L_S}{R_S} \tag{5.11}$$

Using series to parallel transformation, for frequencies around $f_{RF} = 2.5GHz$with a quality factor Q_S results in a transformation as shown in Fig. 30(b) with

$$L_P \approx L_S \tag{5.12}$$

$$R_P = R_S(1 + Q_S^2) \tag{5.13}$$

RF output power is given by

$$P_{RF} = \frac{V_o^2}{R_{ANT}} \tag{5.14}$$

and power loss in passive switch is given by

$$P_{sw}(\%) = \frac{V_o^2}{R_P} \tag{5.15}$$

Percentage of the RF power lost in the proposed switch is given by

$$\begin{aligned} P_{sw} &= \frac{P_{sw}}{P_{RF}} \times 100 \\ &= \frac{R_{ANT}}{R_P} \times 100 \end{aligned} \tag{5.16}$$

So for a circuit with $Q_s = 6$ and $R_s = 5$ results in $R_P = 185$ then power loss in dB is $10log(\frac{P_{sw}}{P_{RF}}) = 10log(\frac{R_{ANT}}{R_P}) = -12dB$

5.5.3. Conclusions

By now it is apparent that the proposed passive T/R switch describes high-performance CMOS RF switches having lower insertion loss, greater isolation and greater power handling capability. The embodiment includes a RF Front end co-design, inductor re-use, and non-invasive single switch control. The proposed work can be fabricated in a complementary Metal-Oxide Semiconductor (CMOS) technology with the transmitter and receiver to provide a completely integrated radio. Therefore, in contrast to some of the prior art discrete switches processed with a technology that is different from the transceiver, the present invention uses a common processing technology that provides a lower cost solution. By applying the new circuit topology, lossy switch transistors can be removed partially. In Receiver (Rx) mode, LNA sees only the inductor. This inductor has 2 benefits. Firstly it is not as lossy as the transistor. Secondly it helps to resonate out the input parasitic cap (C_{P1}) of the LNA and thus improving the matching, bandwidth, gain and noise figure. It being a passive element does not have any linearity limitation and can achieve high linearity figures.

In transmit mode (Tx) mode, Inductor can withstand high voltages without any break down issues unlike conventional transistor switches. Inductor resonates out the parasitic capacitance at the Power amplifier (PA) and thus helps to improve the output matching of the power amplifier. Comparing to traditional solution, there is also no lossy serial switch associated with Tx mode. The loss reduced between PA and antenna can significantly improve overall Tx efficiency. Isolation is also improved without any leakages due to parasitic in transistor switches. The proposed

work employs only one thin gate non-invasive shunt transistor, RxSW in (see Fig. 5.28) and avoids all the lossy thick gate (TG) series transistors. Non-invasive switch in receive mode and no switch in series for PA avoids the loss due to the switch. No switch in series for receiver avoids loss due to the switch. Inductor reuse in receive and transmit modes saves the silicon area.

5.6. Receiver

5.6.1. Receiver architecture

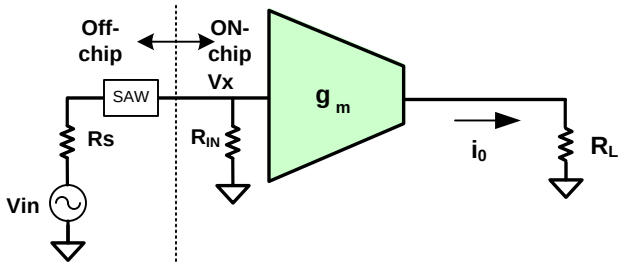


Figure 5.36: Impedance matching at the receiver input in presence of a SAW filter

Conventionally antenna, SAW filter and IC are designed separately and put together. For proper operation and better power matching and noise performance, 50Ω is traditionally taken as reference impedance so that every block function properly when put together as shown in Fig. 5.36. Assuming a 0dB loss for in-band signals in the SAW filter, the voltage V_x and V_{in} are related as below for perfect impedance matching

$$V_x = \frac{V_{in}}{2}, \text{ when } R_{IN} = R_S/2 \tag{5.17}$$

For SAW-less radios, we can remove the 50Ω constraint provided that the trace connecting the antenna and the RFIC is not very long and it is not attenuating the RF signal.

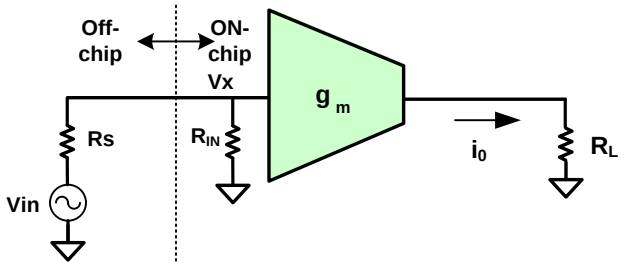


Figure 5.37: SAW-less receiver showing the antenna and the RFIC interface

$$V_x = \frac{V_{in}}{2}, \text{ when } R_{IN} = R_S/2 \tag{5.18}$$

$$V_x = V_{in}, \text{ when } R_{IN} = \infty \tag{5.19}$$

So from Fig. 5.37 and Eq. 5.19 there is an improvement of 6dB in signal power (and in SNR if noise remains the same) when the traditional 50Ω constraint is removed. Inductor peaking at the input further improves the g_m of the LNTA.

Fig. 5.38 shows the receiver chain in the proposed CMOS FEM. The front end LNTA (g_m) drives a buffer immediately entering the SoC which in turn drives the mixer. Thus there is strong isolation between the antenna and the LO. The buffer may need to have 50Ω input impedance to power match the 50Ω cables/traces and to avoid any reflections

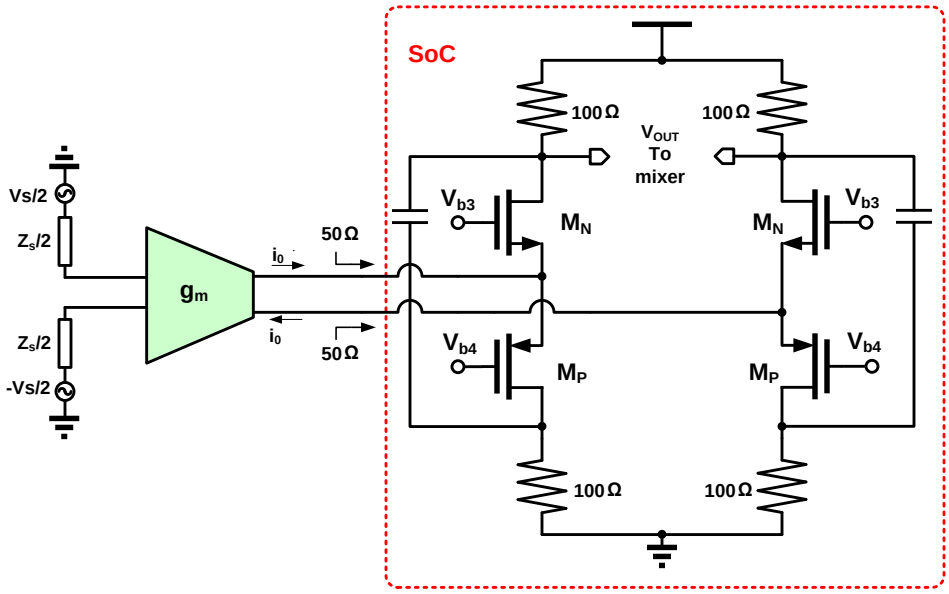


Figure 5.38: Receiver chain in the proposed CMOS-FEM

5.6.2. Low noise transconductance amplifier

Front end LNTA (g_m) cell is implemented by employing complementary PMOS-NMOS transistors in common source operation as shown in Fig. 5.39. Effective transconductance of the cell is given by $G_M = g_{MP} + g_{MN}$. 2^{nd} order distortion is inherently canceled in this topology by the virtue of the complementary nature of the PMOS and NMOS transistors [3]. Besides low distortion, the circuit is also low power as M_P and M_N reuse the current. Voltage headroom is not a concern as the output is a current signal feeding a 50Ω load and the voltage swing is small. V_{DD} of 1V and thin gate transistors are employed.

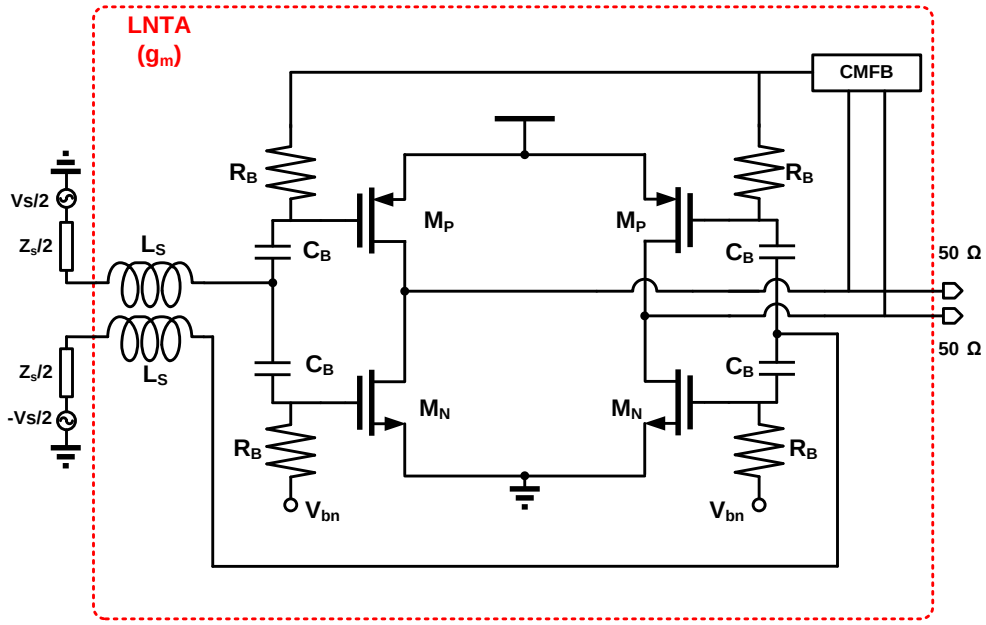


Figure 5.39: Front-end G_m cell in the CMOS-FEM

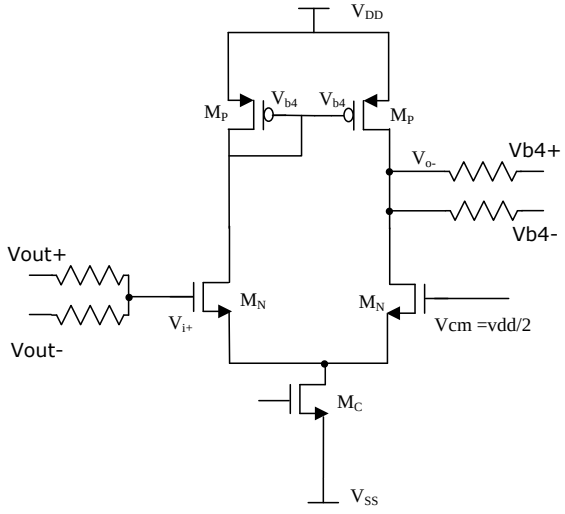


Figure 5.40: CMFB circuit in LNTA

A common mode feedback circuit is employed to bias the gates of the PMOS transistors. A simple one stage amplifier is used in the CMFB circuit. The employed common mode feedback (CMFB) circuit is shown in Fig. 5.40. The stability of the CMFB loop is verified by a step response on the supply as can be seen from Fig. 5.41.

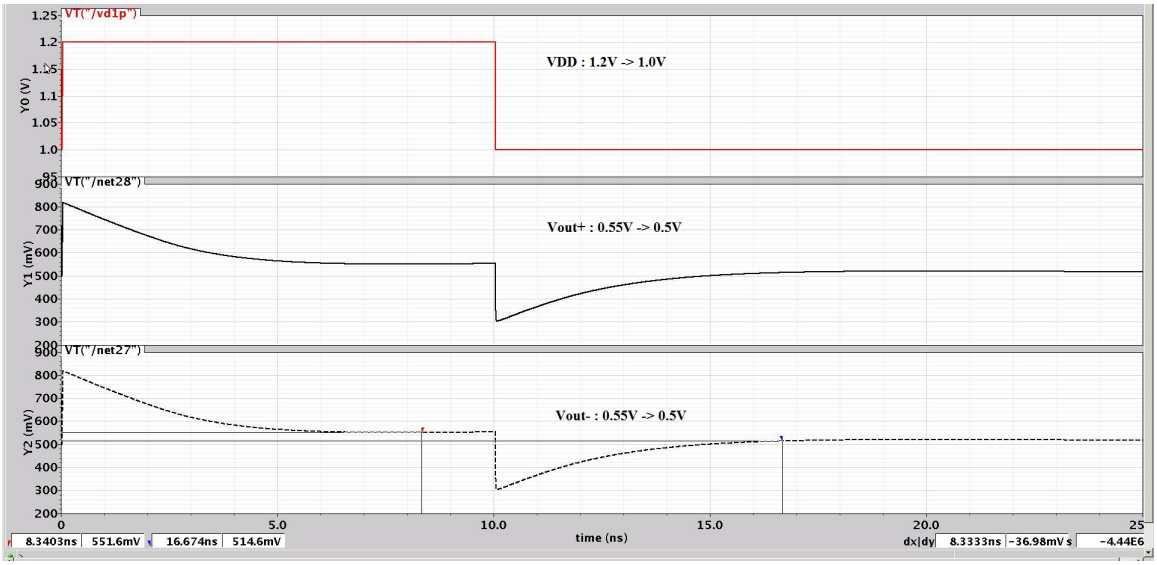


Figure 5.41: Step response to check the stability of CMFB loop in LNTA

5.7. Antenna

5.7.1. Design of a dipole antenna

A dipole antenna is designed on the board. The IC and the board are flip chip assembled which reduces the parasitic of the connecting routing from the IC to the antenna. The antenna is designed to have an input impedance of $Z_{ANT} = 10 + j2\Omega$. The radiation resistance (series resistance of input impedance) of a short dipole with

length L is given by [90, 91].

$$R_{series} = \frac{\pi}{6} Z_o (\frac{L}{\lambda})^2 \text{ for } L << \lambda \tag{5.20}$$

where $\lambda = \frac{c}{f}; c$ =speed of light, and f =frequency of operation.

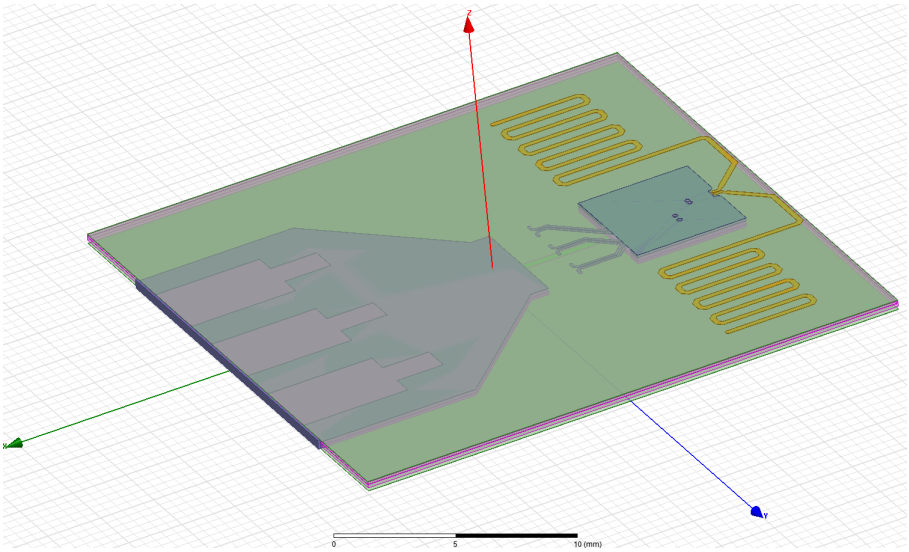


Figure 5.42: Miniaturized dipole antenna with meandered arms modeled in a EM simulator (HFSS)

Short dipoles have low radiation resistance as desired but have a high capacitive reactance. So they are inefficient antenna; but can be used in low frequency applications. For the proposed architecture, the target antenna should have low series resistance and low reactance. Meander dipole antenna has low resistance as well as low reactance in the Z_{ANT}. This is observed and confirmed through EM simulations in HFSS as shown in Fig. 5.42. Obtaining an expression for the exact Z_{ANT} for a

complex antenna structure like shown in Fig. 5.42 is not straight forward. For a half wave dipole antenna with simple structure at resonance frequency, the input impedance is standard and is equal to 73Ω which is higher than the specification. This is the reason for not choosing a simple half wave dipole although the spectral combination is proven effective (see section 5.4). The spectral combination is also verified in the implemented meander dipole antenna as shown in Fig. 5.42. The cross section of the board on which the dipole antenna is implemented is shown in Table 5.1. Same material is used for pre-preg and the core and the dielectric constant is 4.4.

Table 5.1: Cross section of the 4 layer board with thickness in mm

layer name	material	Thickness (μm)
solder mask		20
ENIG		5
Metal layer 1	Copper	18
Pre - preg	Dielectric	100
Metal layer 2	Copper	18
Core	Dielectric	150
Metal layer 3	Copper	18
Pre - preg	Dielectric	100
Metal layer 4	Copper	18
ENIG		5
solder mask		20

The simulation result showing the input impedance of the antenna is shown in Fig. 5.43. The obtained Z_{ANT} (differential) through EM simulations is $15 + j2\Omega$.

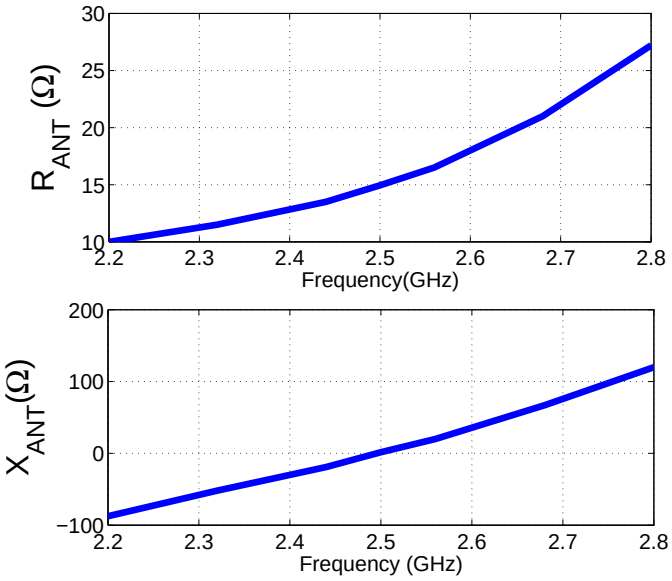


Figure 5.43: Input impedance simulation result for dipole antenna from EM simulator (HFSS)

5.7.2. Common mode coupling

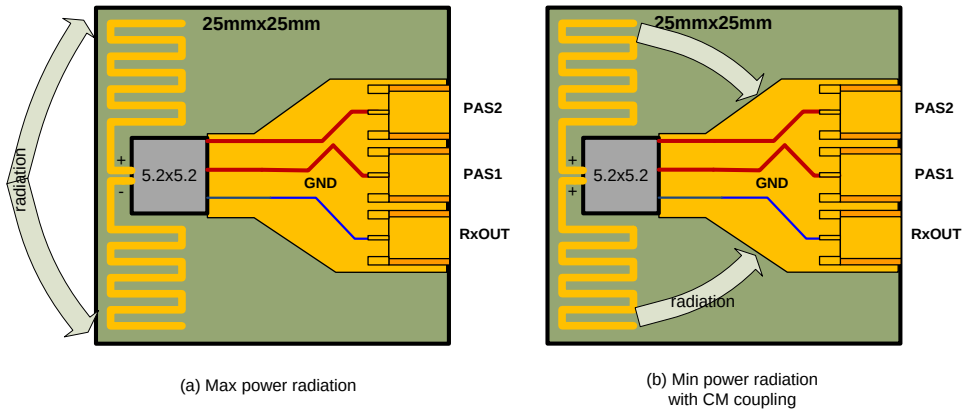


Figure 5.44: Common mode coupling on the board in the minimum radiation case

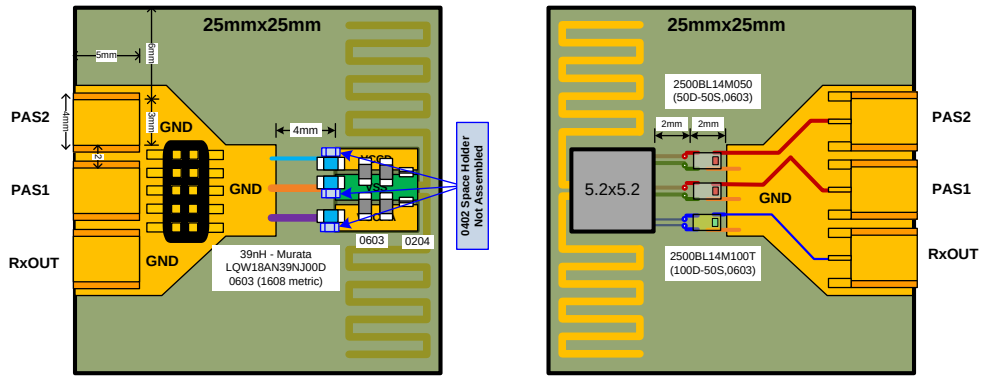


Figure 5.45: Ground Isolation by using (a)inductors for power supply and (b)baluns for RF signals

The radiation patterns are theoretically supposed to be as shown in Fig. 5.22 (peak radiation) and Fig. 5.23 (minimum radiation). But due to common mode coupling (in minimum radiation case) there is a finite radiation from the dipole to the nearest ground plane in the board.

Ideally antenna should not radiate in the minimum radiation case but due to the common mode coupling there is a radiation leakage. This radiation leakage is from the antenna to the ground plane as shown in Fig. 5.44(b), when the antenna is excited by common mode signals. The ground plane could be power supply planes to the IC. This common mode radiaion degrades the linearity and thus the dynamic range of output power as shown in Fig. 5.46. The figure also shows the radiated power after the ground isolation fix (see Fig. 5.45). An ideal linear curve is added to the figure with a slope of one for comparison.

To reduce the common mode radition to the ground plane, the ground plane is spatially kept at a distance. The power signals are feed to the IC through inductors. The inductor offers zero impedance to the DC supply but offers high impedance to

the common mode high frequency signals. Similarly baluns are employed for the RF signals from the IC to isolate the ground of the IC at the centre (5.2 x 5.2 mm^2) and the board's ground plane. These inductors and baluns can be seen in Fig. 5.45. Even after the ground isolation, when the out-phasing angle gets closer to zero ($10logsin^2\theta \longrightarrow -35$), the power radiated to the ground plane is considerable. This small power leakage is due to the finite impedance offered by the inductors and baluns at ω_{RF}. These inductors (39nH) for power signals and baluns for RF signals are employed to isolate the AC ground of the IC and the board.

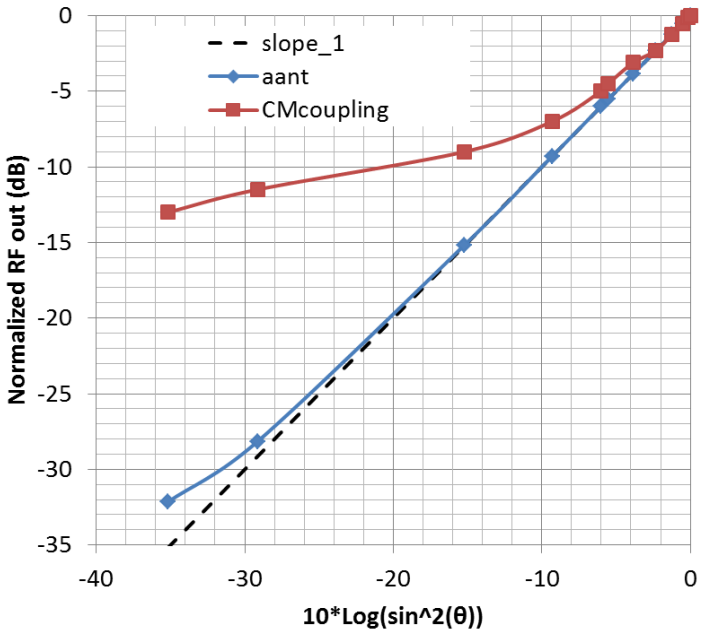
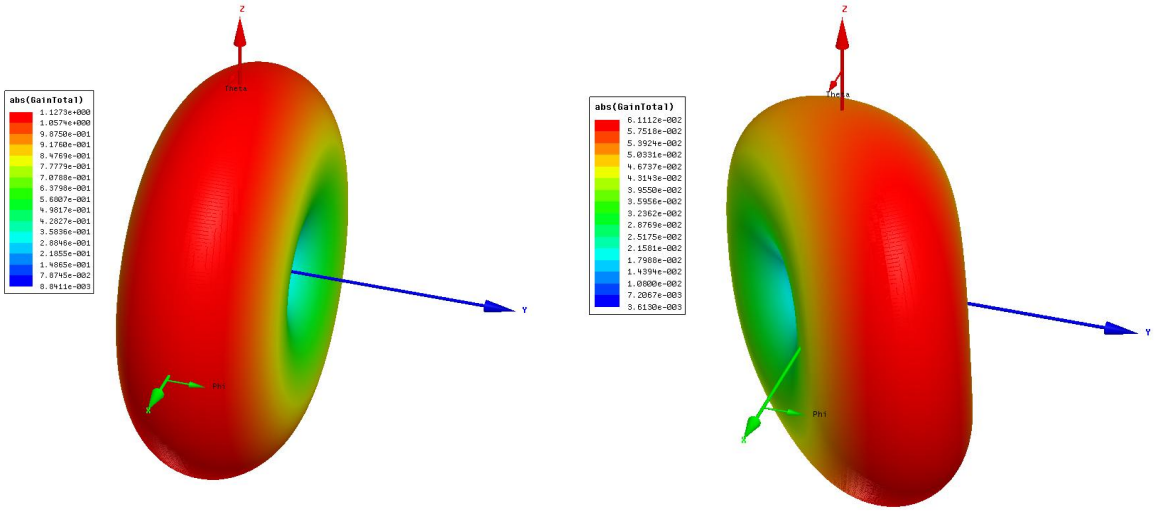


Figure 5.46: Normalized radiated output power of the dipole antenna before and after ground isolation



(a) Max radiation (b) Min radiation

Figure 5.47: Radiation of the dipole antenna after ground isolation for the dipole antenna in Fig. 5.42

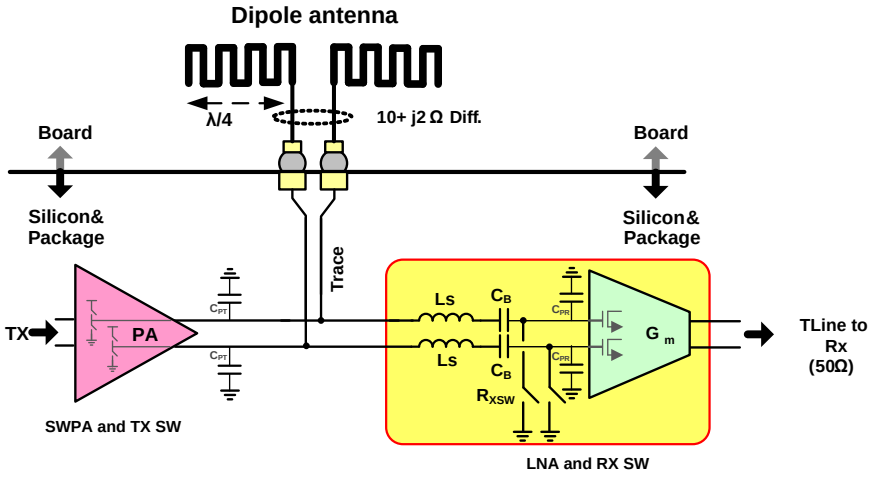


Figure 5.48: Complete system of CMOS front-end module (active antenna)

Fig. 5.47 shows the slight change in the radiation pattern as the out-phasing angle gets closer to the minimum radiation case. This is due to the common mode leakage. Fig. 5.48 shows the complete system schematic of the CMOS Front-end-module implemented on a 32nm silicon technology.

5.8. Results

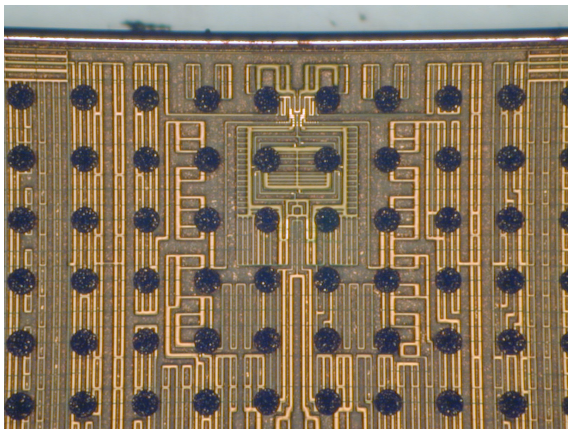


Figure 5.49: Chip micrograph of active antenna in 32nm technology with an active area of 0.15mm^2

Fig. 5.49 shows the chip micro graph of the active part of FEM on 32nm CMOS. Black dots in the picture are the bumps that go for the flip-chip assembly. The spiral ring at the middle is the inductor that realizes the T/R switch. The PA is located very close to top to reduce any mismatches/parasitics between the PA and the antenna. The active area of the IC occupies 0.15mm^2. The fabricated board with 4 metal layers and printed antenna is shown in Fig. 5.50. It is the test board for characterizing the active antenna. left picture is the bottom side and right picture is top side.

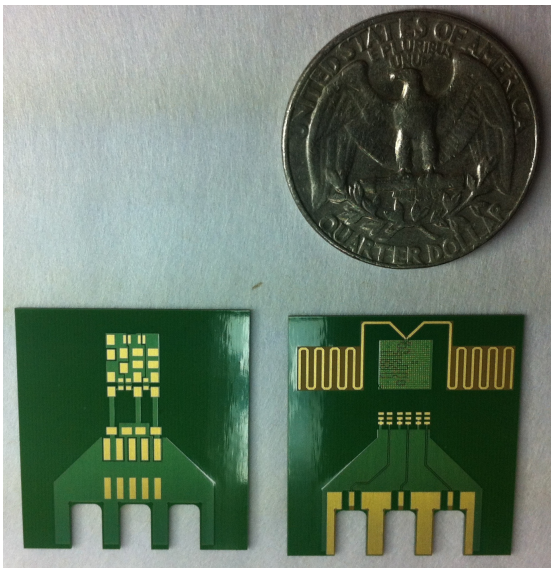


Figure 5.50: Fabricated board for the CMOS-FEM IC assembly

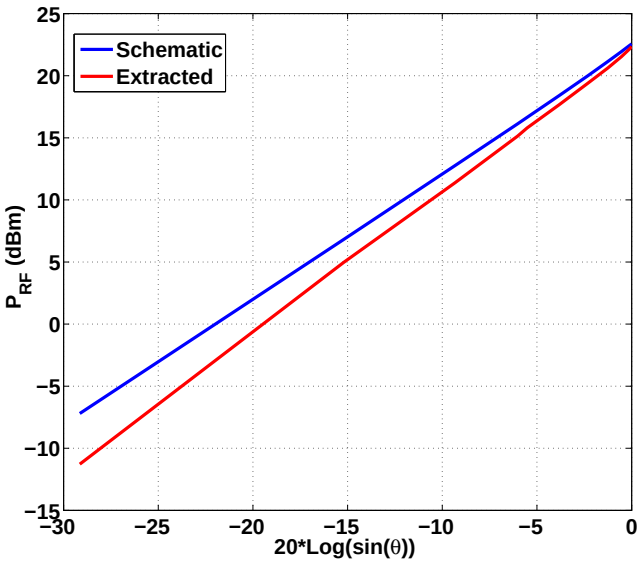


Figure 5.51: Simulations showing the output RF power Vs outphasing angle (θ) in the transmitter with S-parameters of the antenna as load to the transceiver

Fig. 5.51 shows the extracted simulations of the RF output power of the PA with respect to the out-phasing angle. The simulations are done by driving the PA with out-phasing signals (S_1 and S_2). For this data, the whole transceiver as shown in Fig. 5.48 is simulated with the S-parameters of the antenna as a load in Tx mode. The simulation results matches perfectly with the out-phasing theory. The power radiated from the antenna is a function of input out-phasing angle as expected. The radiated power P_{RF} in dBm scales linearly with 20log(sin(θ)) as can be seen from Fig. 5.51. The linearity of the extracted PA-antenna block decreases (slope less than 1) due to the increase in parasitic capacitors that leaks power which is dominating when antenna radiates minimum power (when θ is small).

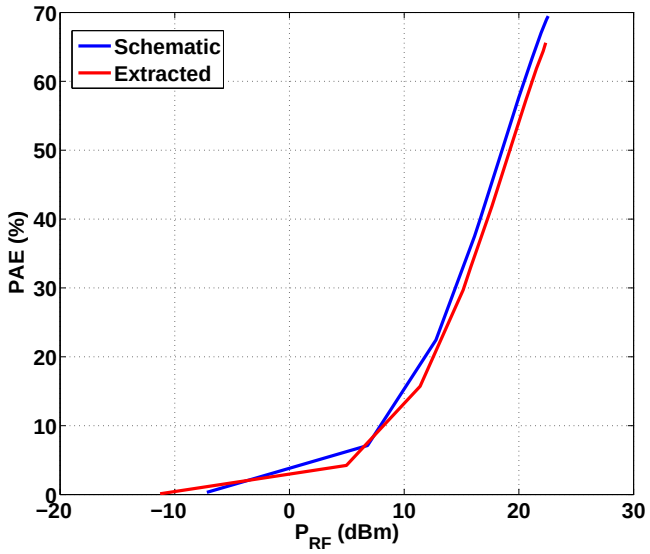


Figure 5.52: PAE vs. PA output power (P_{RF})

Fig. 5.52 shows the power added efficiency of the PA (PAE) with respect to the RF output power. Peak efficiency of more than 65% is obtained form both schematic and

post-layout simulations. PA can transmit a peak RF power of 22.34dBm (extracted). The whole system presents good linearity and promising PA efficiency. At 6dB back off, the PA can achieve 33% PAE. Some of the results of this plot are summarized in the Table. 5.2.

Table 5.2: Post extracted simulation results of the PA in active antenna system

	PA
Peak RF [dBm]	22.34
Peak PAE [%]	65
PAE at -6dB back-off [%]	30
PAE at -6dB back-off [%] with linearization	33
Area[mm^2]	0.03
Technology [nm]	32

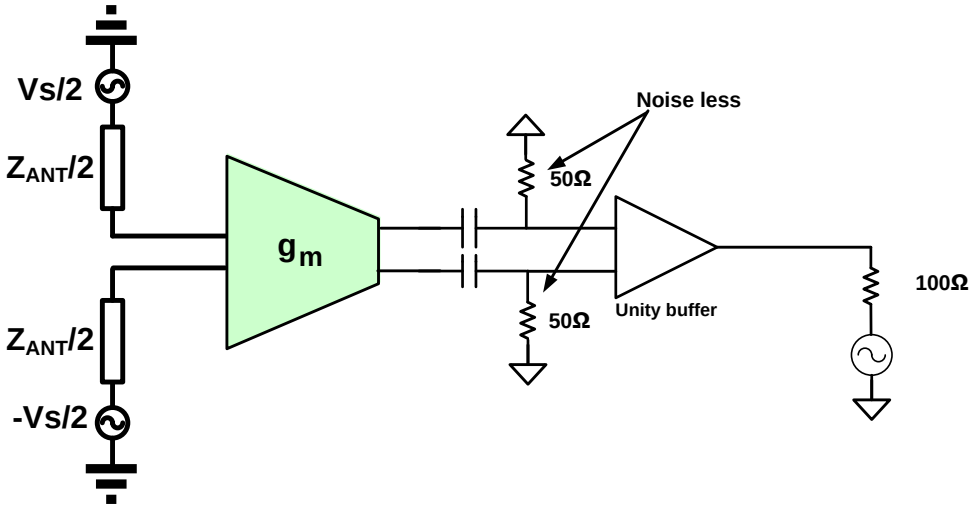


Figure 5.53: Test bench to characterize LNTA in the Rx

For Rx simulations, again the whole system in Fig. 5.48 is simulated with T/R switch in Rx mode. The antenna is emulated as a port for simulation (needs excitation for noise, and s-parameter simulations) with port impedance equal to Z_{ANT} at 2.5GHz. The load impedance for the LNTA is assumed to be a noise less (just for simulations) 100Ω differential (emulating the input impedance of the buffer on the SoC, see Fig. 5.38). The simplified simulation setup can be seen in Fig. 5.53

Gain S_{21} and noise figure obtained from the above test bench are shown in Fig. 5.54 and Fig. 5.55 respectively. From simulations, S_{21} is obtained to be 14dB and the NF is found to be less than 2.5dB. Simulation results for linearity show an IIP_3 of 7dBm, and P_{1dB} of -8dBm with a total power consumption of 11.8mW in the LNTA cell. Performance summary for the LNTA is summarized in Table. 5.3.

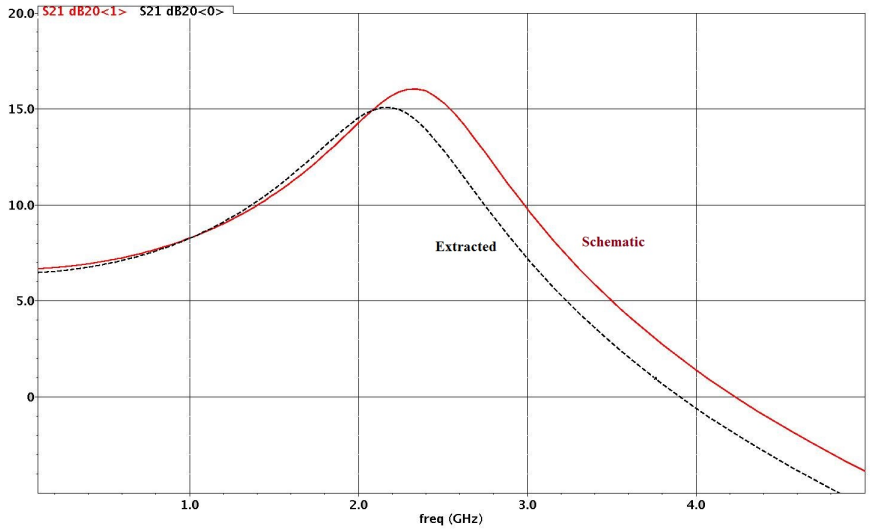


Figure 5.54: Simulated S_{21} of LNTA in the Rx

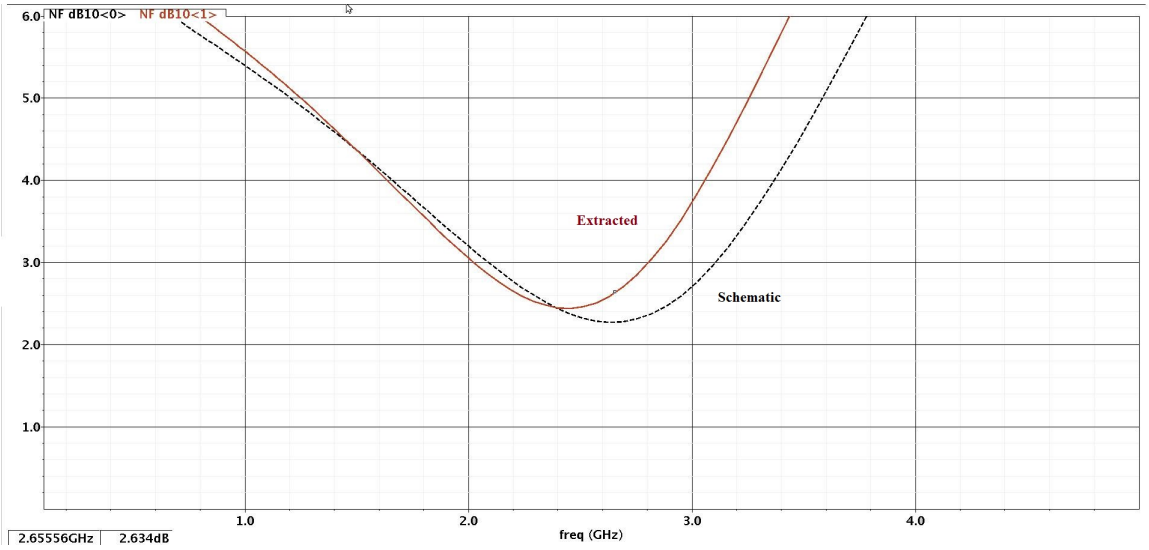


Figure 5.55: Simulated NF of LNTA in the Rx

Table 5.3: Performance summary of LNTA

	LNTA at 2.5 GHz
NF [dB]	< 2.5
S_{21} [dB]	14
IIP_3 [dBm]	7
P_{1dB} [dBm]	-8
Diff G_m [mS]	180
Power consumption [mW]	11.8
Area[mm^2] including L_S	0.12
Technology [nm]	32

Fig. 5.56 shows the efficiency of the dipole antenna with the out-phasing angle.

EM Simulations show an efficiency of 80% in the antenna. At lower out-phasing angle, the data is not so accurate due to the power leakage is comparable to the minimum power radiation.

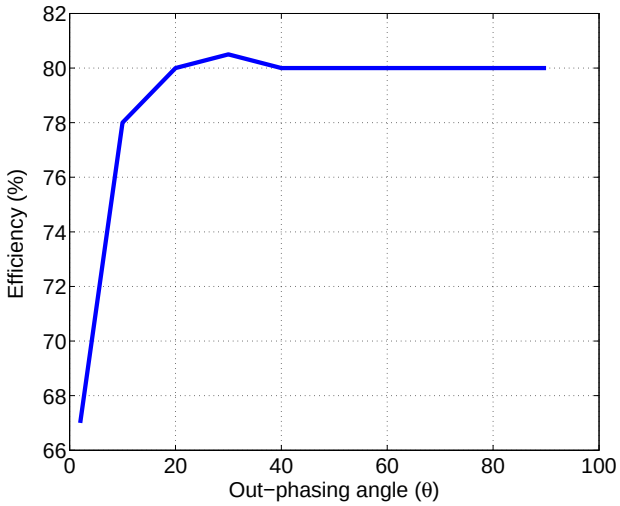


Figure 5.56: Efficiency of the dipole antenna from EM simulations

5.9. Summary

This proposal is a methodology for partitioning and developing RF/analog radio transceivers for rapid time to market with low manufacturing cost for SoC integration. It places the RF front end module (RF-FEM) external to the remaining analog/mixed signal radio transceiver in a SoC. The RF-FEM can be implemented in technology most suitable for the application and can be co-designed with an antenna for the best performance and lowest cost. The RF-FEM IP can be reused for many SoC technology nodes. The analog/mixed signal transceiver for SoCs can be designed to be reconfigurable for different standards and usage models.

This research is focused on developing a separate CMOS RF-FEM for radios.

This RF-FEM is co-designed with the antenna. The present work describe the high performance CMOS RF T/R switch having lower insertion loss (<1dB), greater isolation, high linearity and greater power handling capability. The results also includes a RF front end co-design with integrated T/R switch, inductor re-use, inductor tuning of the input and output parasitic capacitor of the Rx and Tx respectively. The proposed T/R switch does not employ any remote body contacts or series switches. This research work also proposes class-D power amplifier with innovative power combination through dipole antenna. This power combination scheme avoids any passive transformers or inductors thus saving large silicon area. Avoiding the lossy and bulky transformers also improve the peak RF power and power efficiency of the power amplifiers.

6. CONCLUSIONS

6.1. Summary

Circuit and system level innovations for next generation wide-band radio architectures were proposed in this research work. Wide-band radio receivers are essential for the software defined radio realization. Wide-band receivers have the potential to replace the multiple narrow-band receivers. The problems of blockers to wide-band receivers is quite relevant and is properly explained in the previous chapters.

Two highly linear wide-band LNAs are proposed in chapters 2 and 3. Main contribution of these LNA prototypes to the state of the art is the linearity. The linearity is studied carefully and new linearization schemes were proposed in this dissertation. Novel linearization techniques are developed to enhance the linearity especially large signal linearity (P_{1dB}). These LNA architectures are compatible and complement the blocker tolerant radio architectures [18, 20, 24, 25].

The ADC prototype based on the proposed architecture achieves blocker tolerance and fast blocker transient times that are orders of magnitude better than the existing blocker tolerant ADCs. New digitally assisted DAC calibration scheme was also proposed that is robust to P.V.T. variations.

In chapter 5, a novel radio partitioning was proposed that can save power and money. Radio development including Collateral (developing models, tools, etc..) is inconsistent with SoC Product development. SoCs are about integration and time to market (TTM). The proposed radio partitioning methodology is to move the tuned RF circuitry off-chip to FEM. The CMOS FEM, usually RF blocks can remain on the old technology node while the digitally dominated SoC can scale down the technology node much faster and meet the market soon. This lowers development and

manufacturing cost, time to market and risk. Analog/Mixed-Signal circuits on the SoC have no inductors and thus are low cost/size. Speculative models from unmatured technology are good enough for digital, analog and mixed signal circuits. By leveraging the advantages of the new radio partition methodology and co-design, the implemented prototype on 32nm has removed traditional lossy/bulky matching circuits. A novel class D power amplifier with spatial power combination through a dipole antenna was proposed which reduces the area and increases the efficiency of the PA. An inductor based T/R switch was proposed that provides good isolation and less insertion less.

The proposed architectures are compatible with the deep sub-micron CMOS technologies and are easily scalable.

6.2. Possible Area for Future Work

Proposed LNA/LNTA architectures performance can be further improved by proper layout. These highly linear LNA architectures can be used to realize a blocker resilient radio receivers. The proposed linearization techniques can be employed in other parts of the radio chain to build a highly linear radio receiver.

Combined effect of Jitter blockers is properly explained in the chapter on the ADC's. Blocker tolerant techniques are proposed in this work. There is still a scope to work on the jitter tolerant ADC's

An efficient CMOS front end is proposed in the chapter on active antenna. A class D witching power amplifier is employed in the CMOS FEM prototype. Other class of power amplifiers can be explored by the keeping the same kind of proposed radio partitioning. A dipole antenna was used as a power combiner for the class D power amplifier out-phasing signals. This dipole antenna needs to have a ground plane far from the dipole arms to avoid any radiation in minimum radiation mode.

Some new antenna architectures can be explored to avoid the ground plane problem.

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