DESIGN OF INTEGRATED MICROWAVE FREQUENCY SYNTHESIZER-BASED DIELECTRIC SENSOR SYSTEMS

A Dissertation

by

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ABSTRACT

Dielectric sensors have several biomedical and industrial applications where they are used to characterize the permittivity of materials versus frequency. Characterization at RF/microwave frequencies is particularly useful since many chemicals/biomaterials show significant changes in this band. The potential system cost and size reduction possible motivates the development of fully integrated dielectric sensor systems on CMOS with high sensitivity for point-of-care medical diagnosis platforms and for lab-on-chip industrial sensors.

Voltage-controlled oscillator (VCO)-based dielectric sensors embed the sensing capacitor within the excitation VCO to allow for self-sustained measurement of the material under test (MUT)-induced frequency shift with simple and precise readout circuits. Despite their advantages, VCO-based sensors have several design challenges. First, low frequency noise and environmental variations limit their sensitivity. Also, these systems usually place the VCO in a frequency synthesizer to control the sample excitation frequency which reduces the resolution of the read-out circuitry. Finally, conventional VCO-based systems utilizing LC oscillators have limited tuning range, and can only characterize the real part of the permittivity of the MUT. This dissertation proposes several ideas to: 1) improve the sensitivity of the system by filtering the low frequency noise and enhance the resolution of the read-out circuitry, 2) improve the tuning range, and 3) enable complex dielectric characterization in VCO/synthesizer-based dielectric spectroscopy systems.

The first prototype proposes a highly-sensitive CMOS-based sensing system for permittivity detection and mixture characterization of organic chemicals at microwave frequencies. The system determines permittivity by measuring the frequency

difference between two VCOs; a sensor oscillator with an operating frequency that shifts with the change in tank capacitance due to exposure to the MUT and a reference oscillator insensitive to the MUT. This relative measurement approach improves sensor accuracy by tracking frequency drifts due to environmental variations. Embedding the sensor and reference VCOs in a fractional-N phase-locked loop (PLL) frequency synthesizer enables material characterization at a precise frequency and provides an efficient material-induced frequency shift read-out mechanism with a low-complexity bang-bang control loop that adjusts a fractional frequency divider. The majority of the PLL-based sensor system, except for an external fractional frequency divider, is implemented with a 90 nm CMOS prototype that consumes 22 mW when characterizing material near 10 GHz. Material-induced frequency shifts are detected at an accuracy level of 15 ppm_{rms} and binary mixture characterization of organic chemicals yield maximum errors in permittivity of <1.5%.

The second prototype proposes a fully-integrated sensing system for wideband complex dielectric detection of MUT. The system utilizes a ring oscillator-based PLL for wide tuning range and precise control of the sensor's excitation frequency. Characterization of both real and imaginary MUT permittivity is achieved by measuring the frequency difference between two VCOs: a sensing oscillator, with a frequency that varies with MUT-induced changes in capacitance and conductance of a delay-cells' sensing capacitor loads, and a MUT-insensitive reference oscillator that is controlled by an amplitude-locked loop (ALL). The fully integrated system is fabricated in 0.18 μm CMOS, and occupies 6.25 mm^2 area. When tested with common organic chemicals ($\epsilon'_r < 30$), the system operates between 0.7-6 GHz and achieves 3.7% maximum permittivity error. Characterization is also performed with higher ϵ'_r water-methanol mixtures and phosphate buffered saline (PBS) solutions, with 5.4% maximum permittivity error achieved over a 0.7-4.77 GHz range.

DEDICATION

To my dear parents,

lovely wife Enas,

daughter Maryam,

sisters Rania and Lama,

and to all my family

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First and foremost, I would like to thank Allah for guiding me and giving me the patience and the strength to complete this work.

﴿وَكَانَ فَضْلُ اللَّهِ عَلَيْكَ عَظِيمًا﴾ [سورة النساء: ١١٣]

"And ever has the favor of Allah upon you been great." [An-Nisa' : 113]

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1. INTRODUCTION*

1.1 Motivation

Detection of chemicals and biological materials is vital in an enormous number of applications, including pharmaceutical, medical, oil, gas and food/drug safety fields. An effective material detection approach involves characterizing physical and electrical properties of materials under test (MUT), such as electrical permittivity [1]. This motivates the development of efficient permittivity detection techniques such as dielectric spectroscopy (DS) systems which are used to characterize the permittivity of MUT versus frequency.

DS systems are used in numerous applications such as medical and pharmaceutical applications, DNA sensing, forensics, and bio-threat detection [2–10]. The use of DS in the radio and microwave frequency range as a label-free technique for biological sample characterization has been demonstrated for length scales from tissues down to molecules. For example, normal versus cancerous breast tissue discrimination is shown in [11], while on the cellular level DS as a technique for cell counting is reviewed in [12] and cancer investigations are discussed in [13]. On the molecular level, concentration, pH dependence of binding/dimerization, and thermal denaturation of proteins in aqueous solution was studied using BDS [14], [15]. DS is also a valuable technique for industrial applications in material characterization at radio and microwave frequencies, e.g. detection of concentration, bulk density, structure,

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moisture content, etc. [16].

Since many chemicals/bio-materials show significant changes at RF/microwave frequencies [15], permittivity detection in this band is particularly useful for chemical detection [17–19] and for medical applications, such as cell detection [8], [9] and blood sugar monitoring [10]. Hybrid laboratory setups are often used for broadband MUT characterization, with separate instruments individually covering sub-regions of the sensing frequency range [1]. These instruments are often bulky and expensive, while also requiring large sample sizes. This motivates the development of CMOS BDS biosensor systems that offer the integration levels necessary to enable low-cost, point-of-care diagnostic platforms that can operate on aqueous biological samples in the microliter range [2].

1.2 Overview

Capacitance-based sensing, where a capacitor exposed to a MUT exhibits changes in electrical properties, is a common technique reported in the literature for permittivity detection. Different techniques have been employed to detect the changes in the sensor and characterize the MUT. Following this is an overview of these techniques.

First approach is to detect the sensor's reflection and or transmission properties to characterize the MUT [10], [20], [21]. A drawback of these approaches is that they require somewhat large transducer structures which limits them to microwave permittivity sensing applications. However, recent dielectric spectroscopy systems have enabled complex permittivity detection over extended frequency ranges. The work of [17] measures MUT-induced changes in insertion loss of off-chip coupled transmission lines using parallel low- and high-bandwidth RF modules to extend ϵ'_r detection over a MHz to GHz range. In [18], [19] integration of on-chip sensors and RF receiver front-ends is achieved to enable both real and imaginary (ϵ'_r, ϵ''_r)

permittivity detection over wide bands. However, these CMOS implementations lack the integration of critical components, such as the sensor [17], frequency synthesizer (excitation source) and read-out ADC [17–19], necessitating the use of expensive, bulky equipment (e.g. RF signal generator) for system operation.

Another microwave-based technique is to deposit the MUT on top of a microwave resonator and observe the permittivity change as a shift in the resonance frequency. On-board sensors have been implemented using this resonant-based technique in [22, 23]. And a CMOS integrated microwave chemical sensor based on capacitive sensing is proposed in [2] with an LC voltage-controlled oscillator (VCO) that utilizes a sensing capacitor as a part of its tank. The real part of the permittivity of the MUT applied on the sensing capacitor changes the tank resonance frequency, and hence the VCO free-running frequency. Embedding the material sensitive VCO in a phase-locked loop (PLL) allows the oscillator free-running frequency shift to be translated into a change in the control voltage, which is read by an analog to-digital converter (ADC). A multi-step detection procedure, with the ADC output bits controlling an external tunable reference oscillator to equalize the control voltage in both the presence and absence of the material, is then used to read-out the sensor oscillator frequency shift. While this system was able to measure the real part of the permittivity of organic chemicals and binary organic mixtures in the range of 7 to 9 GHz with a 3.5% error, defined as the absolute difference between the room temperature (20°C) measured and theoretical values [24]- [25], it suffers from several drawbacks: 1) An expensive tunable reference frequency source is required. 2) The ADC resolution limits the accuracy of the frequency shift detection. 3) Utilizing a single VCO sensor necessitates a complicated multi-step measurement procedure and makes the system performance susceptible to low-frequency environmental variations. 4) The system can not characterize the loss of the MUT ($\epsilon_r''(\omega)$)

using frequency shift measurements due to the oscillation frequency being relatively insensitive to changes in resistive loading. 5) The tunning range is limited.

1.3 Organization

The remainder of the dissertation discusses the proposed architectures to enhance VCO-based dielectric spectroscopy systems. The implementation of these architectures and the experimental results are presented. This dissertation is organized as follows. Section 2 discusses VCO-based systems, and describes the different parts of the system (the read-out circuitry and the VCO), and the system noise.

Section 3 discusses a highly-sensitive CMOS-based sensing system for permittivity detection and mixture characterization of organic chemicals at microwave frequencies. The proposed system along with the bang-bang control loop that is utilized for frequency shift measurement is explained. System and circuit implementations are discussed. Finally, electrical and chemical experimental measurements are presented.

Section 4 discusses a fully-integrated sensing system is proposed for wideband complex dielectric detection of materials under test (MUT). The system utilizes a ring oscillator-based phase-locked loop (PLL) for wide tuning range and precise control of the sensor's excitation frequency. Ring oscillator-based sensing system that can detect complex permittivity using frequency shift measurement is explained. System and circuit implementations are discussed. Finally, electrical and chemical experimental measurements are presented. Finally, Section 5 concludes the thesis.

2. BACKGROUND*

2.1 VCO-Based Sensing System

Fig. 2.1 shows a self-sustained oscillator-based sensing system consisting of an oscillator loaded with a sensing capacitor and a read-out block. Exposing the sensing capacitor to a MUT changes its capacitance by $\Delta C(\omega)$ and conductance by $\Delta G(\omega)$ proportional to ϵ_r' and ϵ_r'' of the MUT, respectively. Depending on the oscillator type, characterization of $\Delta C(\omega)$ and $\Delta G(\omega)$ is possible with measurement of the oscillator's free running frequency and/or amplitude.

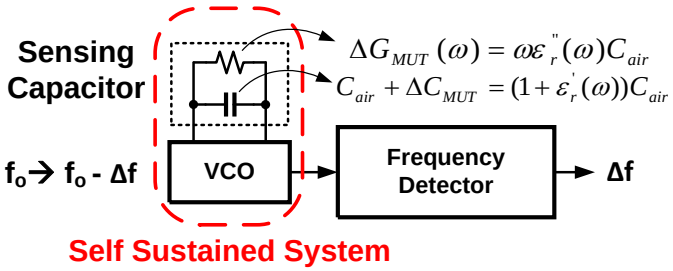

Figure 2.1: VCO-based sensing system.

The frequency resolution, defined as the minimum frequency shift that can be detected by the system, is primarily a function of the system's input referred noise

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and frequency detector quantization noise. Note that both the VCO phase noise and the frequency detector circuitry can contribute to the system's input-referred noise. The performance of the sensing system in Fig. 2.2(a) is limited by VCO temperature sensitivity and low frequency noise. This motivates the use of a reference oscillator [26], as shown in Fig. 2.2(b), and measuring the desired frequency shift as the difference between the sensing and the reference VCOs. One practical issue with this approach is that the two VCOs should be in close proximity to maximize noise correlation. However, this causes VCO frequency pulling when the VCOs are simultaneously operating. In order to avoid this, the two VCOs can be periodically activated such that only one operates at a time [26]. This results in a beneficial high-pass filtering of the correlated low-frequency noise between the sensor and reference VCO.

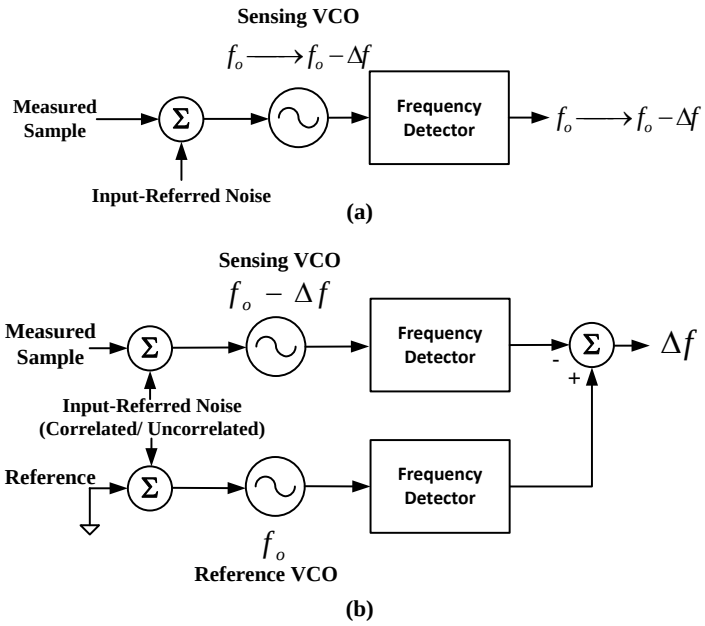

Figure 2.2: VCO-based sensors incorporating: (a) a single VCO, (b) reference and sensing VCOs.

2.2 Frequency Detector

One common frequency detector implementation is a frequency counter [26]. While this method can achieve high resolution, it requires long measurement times, on the order of milliseconds. Also, since the VCOs are embedded in an open loop system, the absolute oscillator frequency drift makes it difficult to characterize the MUT properties at a precise frequency.

A PLL can serve as a closed-loop frequency detector circuit, as shown in Fig. 2.3 [2], to enable MUT characterization at a precise frequency. For a fixed division ratio, N, and reference frequency, f_{ref} , the change in the VCO free-running frequency is translated into a change in the control voltage, V_c, and read out using an ADC. This method also offers a significantly faster measurement time set by PLL settling, typically on the order of microseconds, which is useful for high-throughput chemical characterization systems and emerging biosensor platforms for real-time monitoring of fast biological processes, such as protein-drug binding kinetics [27].

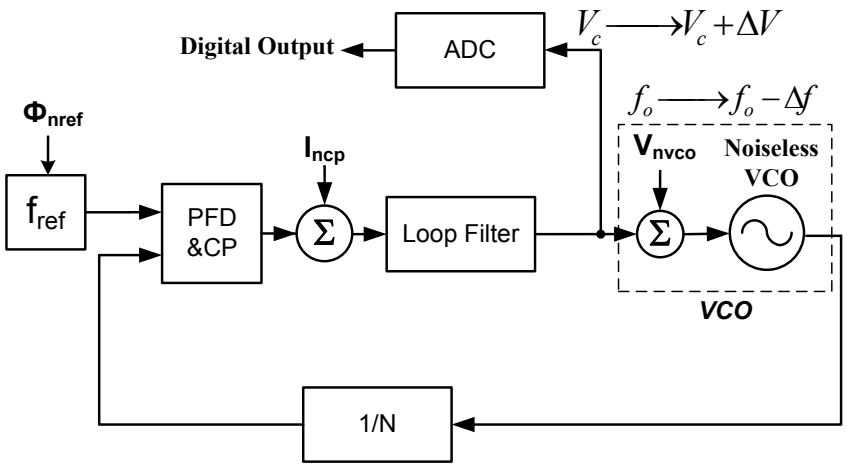

Figure 2.3: A VCO-based sensor using a PLL and an ADC as a frequency detector.

2.3 VCO

This subsection compares LC and ring oscillator-based sensors in terms of: i) the effect of the sensor's capacitance and conductance variations on their oscillating frequency and amplitude, ii) system tuning range and sensitivity versus frequency, and iii) system noise.

2.3.1 LC Oscillator-Based Sensor

An LC oscillator's frequency is a function of the total tank capacitance C_t, consisting of the sensing capacitor, varactors, and the parasitic capacitors from the transistors and inductors, and the tank inductance L_p (Fig. 2.4).

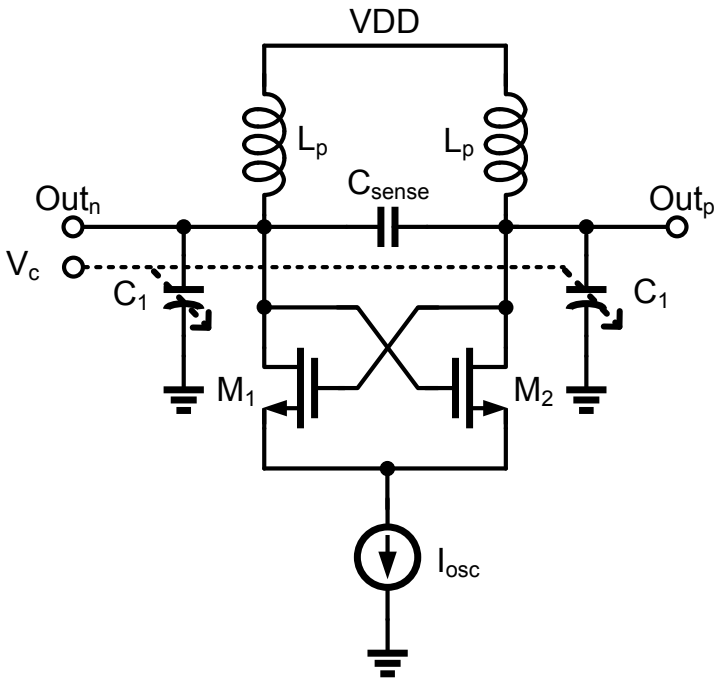

Figure 2.4: Schematic of a typical LC sensing VCO.

$$f_o = \frac{1}{2\pi\sqrt{L_p C_t}} \tag{2.1}$$

As the effect of the sensor conductance on the oscillating frequency is very small, simple frequency shift measurements can be used to characterize variations in the sensor's capacitance [2], [28]. The relative frequency shift $\Delta f_o/f_o$ can be expressed in terms of the relative shift in the total load capacitance by

$$1 + \frac{\Delta f_o}{f_o} = \frac{1}{\sqrt{1 + \Delta C_t(f_o)/C_t}}, \tag{2.2}$$

which for small $\Delta C_t(f_o)/C_t$ can be approximated as

$$\frac{\Delta f_o}{f_o} \approx -\frac{1}{2}\frac{\Delta C_t(f_o)}{C_t}. \tag{2.3}$$

While measurements of a current-limited oscillator's output amplitude is a potential technique to characterize variations in the sensor's conductance, as the amplitude is function of the bias current I_{osc} and the total tank conductance G_t,

$$A = \frac{4}{\pi}\frac{I_{osc}}{G_t}, \tag{2.4}$$

a drawback of this approach is that precise amplitude measurement necessitates high resolution voltage-mode ADCs.

LC oscillator-based sensing systems also typically display limited operating frequency ranges due to several factors: i) the tank quality factor, ii) large bulky inductors for low frequency operation, and iii) decreased frequency shift sensitivity to variations in the sensor's capacitance due to increased total tank capacitance C_t at the low frequency ranges. On the other hand, their excellent phase noise allows for low noise frequency shift measurements. Because of these factors, LC oscillator-based sensing systems have been used in low-noise narrow-band capacitive sensing

applications at high frequencies [2], [28].

2.3.2 Ring Oscillator-Based Sensor

As discussed in Subsection 4.2 [29], the fundamental frequency and amplitude of an N-stage ring oscillator as a function of the total delay cell output capacitance C_t and conductance Gt (Fig. 2.5) can be approximated by

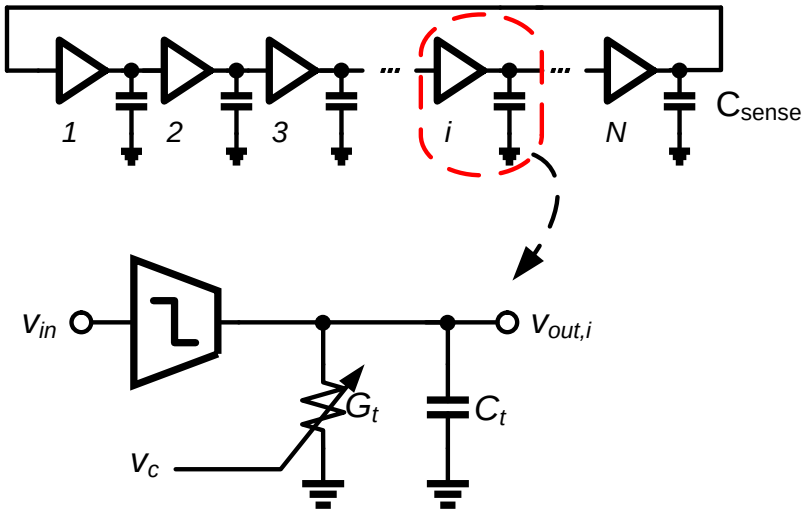

Figure 2.5: Schematic of an N−stage ring VCO and delay stage model.

$$f_o = \frac{1}{2\pi}\frac{G_t}{C_t}\tan\frac{\pi}{N}, \tag{2.5}$$

and

$$A = \frac{4}{\pi}\frac{I_{osc}}{G_t}\cos\frac{\pi}{N}. \tag{2.6}$$

Unlike LC oscillators, ring oscillators' frequency is a function of both the delay cell

G_t and C_t. The relative frequency shift $\Delta f_o/f_o$ can be expressed in terms of the relative shift in the delay cell output capacitance and conductance by

$$1 + \frac{\Delta f_o}{f_o} = \frac{1 + \Delta G_t(f_o)/G_t}{1 + \Delta C_t(f_o)/C_t}, \tag{2.7}$$

which for small $\Delta C_t(f_o)/C_t$ and $\Delta G_t(f_o)/G_t$ can be approximated as

$$\frac{\Delta f_o}{f_o} \approx \frac{\Delta G_t(f_o)}{G_t} - \frac{\Delta C_t(f_o)}{C_t}. \tag{2.8}$$

Thus, there is the potential to extract both conductance and capacitance variations based on simple frequency shift measurements, provided that these terms can be separated.

Relative to LC oscillators, ring oscillators offer advantages of wide tuning range and reduced area consumption. In addition, the frequency of a ring oscillator is more sensitive to capacitance variations due to the following: i) it is directly proportional to $1/C_t$, allowing 2X improvement in frequency shift, ii) frequency tuning can be achieved by changing the load conductance, which obviates additional varactors and minimizes C_t to the sensor and parasitic transistor/resistor capacitances. While employing conductance tuning decreases the ring oscillator's frequency shift with conductance variations at high frequencies ($G_t \propto f$), as shown in (2.8), fortunately, the ϵ_r'' MUT-induced frequency shift remains constant due to the conductance being directly proportional to frequency and ϵ_r'' (Fig. 2.1).

Overall, with simple frequency shift measurements ring oscillator-based systems provide the potential to characterize both the sensor capacitance and conductance, while LC oscillator-based systems can only characterize sensor capacitance. Utilizing only frequency-shift measurements is a major advantage for ring oscillator-based systems due to the ability to achieve high resolution and noise filtering with sufficient

measurement time, which minimizes the impact of increased ring oscillator phase noise.

2.4 System Noise

This subsection discusses the noise of VCO-based system which is function of the phase noise of the VCO and the added noise due to the read-out circuit. In counter-based method, the counter quantization noise contribute to the system noise. In PLL-based method, all the blocks in the PLL other than the VCO contribute to system noise and should be analyzed by considering the transfer function from that particular block to the control voltage node. The PLL filters high-frequency content of the VCO input-referred noise, $V_{n,vco}$, as the transfer function, $V_c/V_{n,vco}$, is a low-pass response with a cut-off frequency equal to the loop bandwidth [2], while noises from the charge pump, $I_{n,cp}$, and input reference clock, $\phi_{n,ref}$, are band-pass filtered by the loop. Also, in the locked condition the charge pump noise is scaled due to it only appearing on the control voltage for a time equal to the reset path delay of the phase-frequency detector (PFD) [30], which is a fraction of a reference clock cycle. Assuming a low-noise input reference clock, the VCO noise and charge pump noise are generally dominant. However, care should also be used in choosing the loop filter resistor, as its noise on the control voltage is high-pass filtered by the loop. Note, an important tradeoff exists between the control voltage noise level and the PLL settling time, as reducing the PLL bandwidth filters more VCO input-referred noise and charge pump noise at the cost of increased the system measurement time. Another important noise source, the system quantization noise is set by the ADC resolution [2]. This implies a significant increase in ADC resolution requirements and overall complexity for improved frequency shift measurement capabilities.

3. A HIGHLY-SENSITIVE CMOS FRACTIONAL-N PLL-BASED MICROWAVE CHEMICAL SENSOR *

3.1 Introduction

This section presents a CMOS fractional-N PLL-based chemical sensor based on detecting the real part of a MUT's permittivity. Detection of this real part of the permittivity is suitable for the characterization of mixing ratios in mixtures which is beneficial in many applications, including: (1) medical applications such as the estimation of the glucose concentration in blood [10], and (2) the estimation of moisture content in grains [31]. The system utilizes both a sensor and reference VCO which enables improved performance and lower complexity relative to the system in [2]. For the frequency-shift read-out, instead of controlling an expensive externally tunable reference oscillator, a low-complexity bang-bang control loop periodically compares the control voltage when the sensor and the reference oscillator are placed in the PLL loop and adjusts a fractional-N loop divider. Since the system determines permittivity by measuring the frequency difference between the sensor and reference VCO, common environmental variations are cancelled out and the measurement procedure is dramatically simplified to a single-step material application. Also, utilizing a high-resolution fractional divider allows the frequency shift resolution measurement to be limited by system noise, rather than the ADC quantization noise [2].

This section is organized as follows. Subsection 3.2 provides an overview of the proposed fractional-N PLL-based chemical sensor system. Key design techniques for the capacitive sensor and the VCO, which is optimized to minimize the effect of the

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imaginary part of the permittivity on the oscillation frequency to ensure the real part is accurately detected, are discussed in Subsection 3.3. Subsection 3.4 provides more circuit implementation details of the shared-bias sensor and reference VCO, other PLL blocks, and the bang-bang comparator which senses the VCO control voltage. The 90 nm CMOS prototype and the chemical sensing test setup are detailed in Subsection 3.5. Subsection 3.6 shows the experimental results, including characterization of key circuit blocks and organic chemical mixture detection measurements. Finally, Subsection 3.7 concludes the section.

3.2 Proposed Fractional-N PLL-Based System

As discussed in Section 2, the use of a reference VCO enables filtering of correlated low frequency noise between the sensor and reference VCO. This is achieved in a PLL-based system with the proposed sensor architecture shown in Fig. 3.1. Here, the PLL utilizes a single fixed reference clock and is controlled by the f_s clock, which alternates between having the sensor oscillator and fixed integer divider, N_S, in the loop and having the reference oscillator and adjustable fractional divider, N_R, present.

When f_s is in the low-state, the reference VCO frequency, $f_{vco,R}$, is set to $8N_R f_{ref}$ and the control voltage settles to $V_{c,R}$, while when f_s is in the high-state the sensor VCO frequency, $f_{vco,S}$, is set to $8N_S f_{ref}$ and the control voltage settles to $V_{c,S}$. Assuming that the two division values are equal, $N_R = N_S$, the difference between $V_{c,R}$ and $V_{c,S}$ is a function of the MUT-induced frequency shift between the two VCOs and

$$f_{vco,R} = f_o + K_{vco} V_{c,R} \tag{3.1}$$

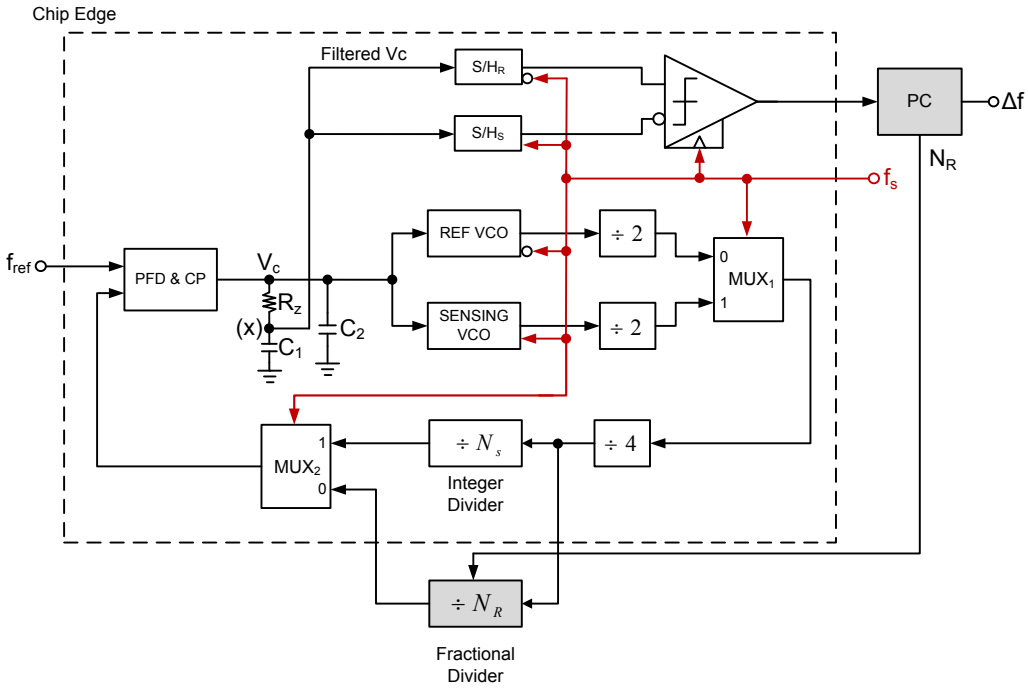


Figure 3.1: Block diagram of the dielectric sensor based on a fractional-N frequency synthesizer with sensor and reference VCOs and dual-path loop dividers. A bang-bang control loop adjusts the fractional divider value to determine the frequency shift between the sensor and the reference VCO.

$$f_{vco,S} = (f_o - \Delta f) + K_{vco} V_{c,S}, \tag{3.2}$$

where K_{vco} is the VCO gain in Hz/V, f_o is the free running frequency of the reference VCO, and Δf is the difference between the free running frequencies of the reference and sensing VCOs, which is the subject of detection. Substituting $f_{vco,R} = 8N_R f_{ref}$ and $f_{vco,S} = 8N_S f_{ref}$ results in

$$8N_R f_{ref} = f_o + K_{vco} V_{c,R} \tag{3.3}$$

$$8N_S f_{ref} = (f_o - \Delta f) + K_{vco} V_{c,S}. \tag{3.4}$$

Thus, as shown in Fig. 3.2(a), the frequency shift can be approximated as

$$\Delta f = K_{vco}(V_{c,S} - V_{c,R}). \tag{3.5}$$

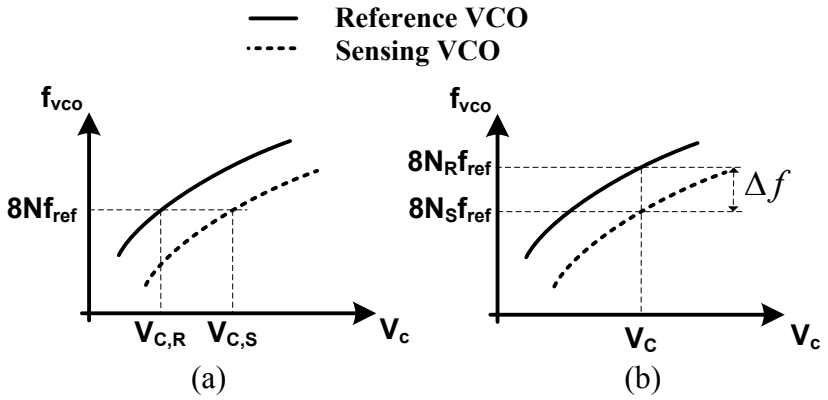


Figure 3.2: VCO frequency versus control voltage: (a) $N_R = N_S = N$, and (b) $V_{c,R} = V_{c,S} = V_c$.

However, measuring the frequency shift based on the difference between $V_{c,R}$ and $V_{c,S}$ suffers from two drawbacks: 1) The accuracy is degraded due to the VCO gain nonlinearity. 2) A high resolution ADC is required. Using (5), the relationship between the VCO frequency, frequency shift in ppm, the average VCO gain, supply voltage, V_{DD}, and the number of ADC bits, N_{ADC}, is

$$\Delta f(ppm) = \frac{V_{DD}K_{VCO}}{2^{N_{ADC}}} \times \frac{10^6}{f_{vco}}. \tag{3.6}$$

For example, if V_{DD} = 1.2 V, K_{vco} =500 MHz/V, and $f_{vco,S}$ = 10 GHz, an ADC with a minimum 10-bit resolution is required to detect frequency shifts in the order of $\sim$ 60 ppm. The following describes how these two drawbacks are mitigated by a

different detection algorithm and a bang-bang control loop.

In order to eliminate the effect of VCO gain nonlinearity, a different detection algorithm is used that is based on changing the division value, N_R, until the control voltage $V_{c,R}$ becomes equal to the control voltage $V_{c,S}$, as shown in Fig. 3.2(b). Here the difference between N_R and N_S represents the frequency shift between the two VCOs.

$$\Delta f = 8 f_{ref}(N_R - N_S) \tag{3.7}$$

Here the frequency shift measurement is independent of the VCO gain nonlinearity. However, the measurement accuracy is still limited by the reference frequency value and the resolution of the adjustable frequency fractional divider. As reducing the reference frequency mandates reducing the PLL bandwidth, which increases the PLL settling time, this system employs an off-chip fractional divider, N_R. While this fractional divider could easily be implemented in the CMOS chip, since designing high-resolution dividers is much easier than high-resolution ADCs, due to tape-out time constraints an external divider was used in this prototype, as shown in Fig. 3.1. A fractional divider with M-bit fractional resolution provides a minimum frequency shift of $\Delta f(min, ppm) = f_{ref}(1/2^M)(10^6/f_{vco})$. For example, utilizing a 25 MHz reference frequency, 10 GHz VCO frequency, and a 25-bit fractional divider results in a resolution of 7.7×10^{-5} ppm.

In order to alleviate the need for a high resolution ADC, a bang-bang control loop is used to adjust the divider value. Here the term "bang-bang" indicates that the control loop's error detector, which is a comparator, generates only a quantized logical "-1" or "+1" depending only on the error sign, similar to the operation of a bang-bang phase detector used in clock-and-data recovery systems [32]. As illus-

trated in Fig. 3.3, the control voltage is sampled during each phase of the switching clock, f_s, using sample and hold circuits $(S/H)_R$ and $(S/H)_S$ and applied to a comparator. The comparator output is used to adjust the fractional divider value and determine the frequency shift. A cumulative density function (CDF) of the average comparator output, V_{comp}, versus the difference between $V_{c,R}$ and $V_{c,S}$ is shown in Fig. 3.4, assuming Gaussian system noise. If the average comparator output is near a logical "-1" or "+1", the difference between $V_{c,R}$ and $V_{c,S}$ is significantly larger than the total system noise and the system uses the averaged comparator output to adjust the reference divider. As the difference between $V_{c,R}$ and $V_{c,S}$ moves toward zero, the system noise causes the comparator to output a similar number of "-1" and "+1" outputs, and the averaged output approaches zero. Once the averaged comparator output is near zero to within a certain tolerance, the frequency shift is then calculated. As the sensor divider remains fixed, this approach ensures that the frequency shift is measured at a fixed frequency, regardless of the frequency shift.

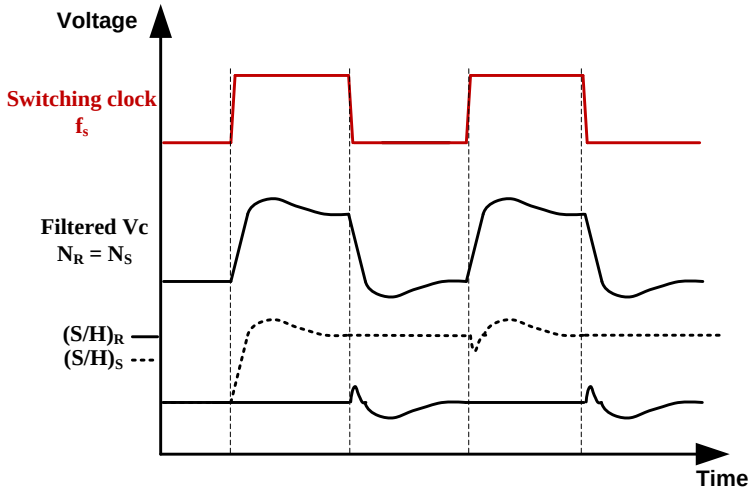


Figure 3.3: System signals: Sensor/Reference control f_s, filtered control voltage V_c, and output of sample and hold circuits.

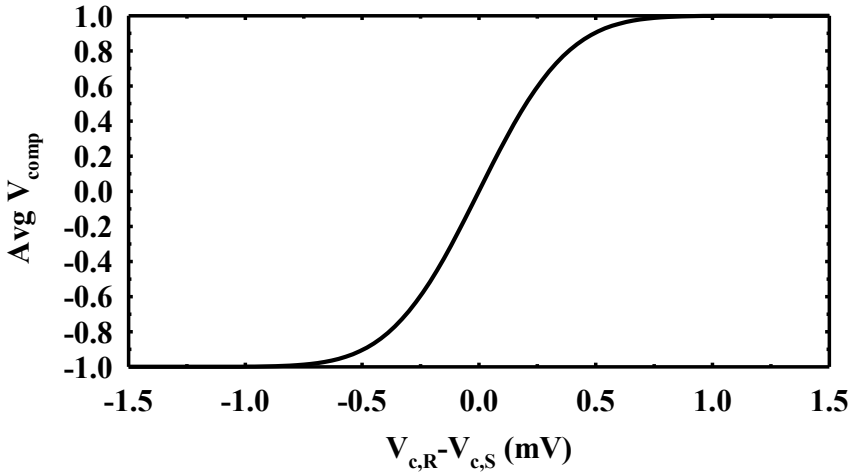


Figure 3.4: CDF function that represents the averaged comparator output versus the difference between $V_{c,R}$ and $V_{c,S}$ with sigma = 0.25 mV, which corresponds to 15 ppm at k_{vco} = 500 MHz/v.

The flowchart of Fig. 3.5 summarizes the system operation as follows: (1) The MUT is deposited on top of the sensing VCO, (2) the comparator output bits are readout to a PC and digitally filtered, (3) the division ratio, N_R, is tuned until the average comparator output approaches zero at which (4) the frequency shift is measured as $f_{ref}(N_R - N_S)$. Note that this measurement procedure requires only a single MUT application, and is dramatically simpler than the multi-step MUT application and de-application procedure of [2]. Several techniques are utilized in order to improve the system noise performance and account for mismatches between the sensor and reference VCO. A filtered version of the PLL control voltage at node X (Fig. 3.1) is sampled in order to filter high frequency noise. Additional low-frequency noise filtering is also possible by increasing the averaging time of the comparator outputs. As the mismatches between the two VCOs and the comparator input-referred offset introduces a systematic system offset, this is accounted for during sensor calibration

by characterizing the system with the sensing VCO not loaded with any MUT. For this calibration case with the sensor only exposed to air, the difference between N_R and N_S, is read out, recorded, and serves as the overall system offset. Note that this offset calibration should be performed at each material characterization frequency in order to account for the VCOs' Kvco variation with frequency. In addition, any Kvco mismatch between the VCOs can be calibrated by performing measurements with control materials of known permittivity; with system accuracy improving with the number of calibration materials employed. Additional sensor calibration details are provided in the experimental results of Subsection 3.6.2.

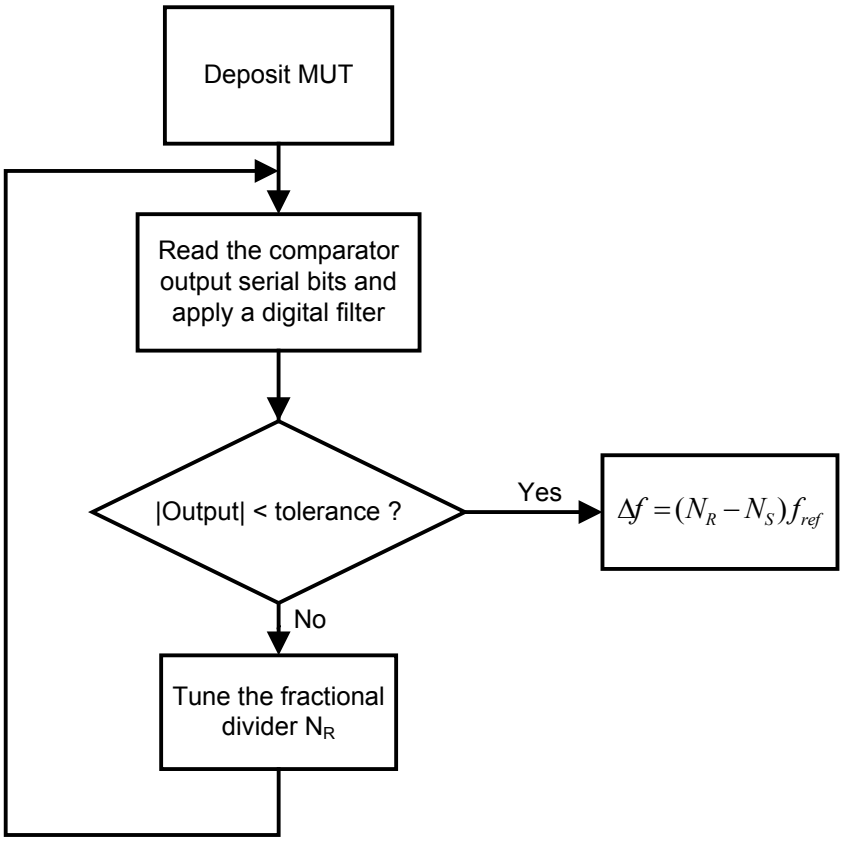


Figure 3.5: Flowchart of the frequency shift measurement algorithm.

Table 3.1 summarizes the 10 GHz PLL system-level specification. The PLL utilizes a 25 MHz reference clock and is designed with a damping factor of 1 for robust operation and a 1 MHz bandwidth to enable fast switching between the sensor and reference VCOs. Tradeoffs between system noise and loop filter area are considered in selecting the charge pump current and loop filter parameters. While increasing the charge pump current decreases the contributed noise on the control voltage [30], for a given bandwidth and damping factor it increases the required loop filter capacitor which increases the area. Thus, a 100 μA charge pump current is selected to enable reasonable loop filter values. Also, as the control voltage is observed at the loop filter internal node X, the values of R_z and C_1 are selected to enable a fast switching frequency between the two VCOs, f_s.

Table 3.1: 10 GHz PLL parameters

f_{ref}	25 MHz
Damping Factor, ζ	1
Bandwidth	1 MHz
k_{vco}	600 MHz/V
Charge Pump Current, I_{cp}	100 μA
R_z	49 kΩ
C_1	13 pF
C_2	800 fF

3.3 Sensor Design

3.3.1 Sensing Element

Each MUT has a frequency-dependent complex relative permittivity $\varepsilon_r(\omega) = \varepsilon'_r(\omega) - j\varepsilon''_r(\omega)$, with both real and imaginary components. The real part represents the stored energy within the material and the imaginary part represents the material's loss, with the loss tangent quantifying the ratio between $\varepsilon''_r(\omega)$ and $\varepsilon'_r(\omega)$ (tan δ $= \varepsilon''_r(\omega)/\varepsilon'_r(\omega)$). As the objective of the implemented sensor is to detect the real part of the MUT's complex permittivity, the MUT is placed on top of a capacitor-based sensor and the permittivity is measured with the change in the sensor's capacitance. This subsection explains the sensor's design and key characteristics. It also discusses the effect of the material's loss on the capacitance measurements and permittivity detection.

A capacitor implemented on the top metal layer of a CMOS process with area of 0.0461 mm^2, shown in Fig. 3.6(a) and (b), forms the sensing element. The 325 $\mu m \times 142$ μm capacitor has the equivalent circuit model shown in Fig. 3.6(c). The MUT affects the electromagnetic (EM) fields between t1 and t2, with the admittance $Y_{12}(\omega)$ between t1 and t2 having a fixed capacitive component due to direct parallel-plate capacitance between the capacitor's metal, C_{fixed}, a parallel plate capacitance to substrate, C_{10}, C_{20}, and a fringing capacitance that changes according to the permittivity of the MUT, $C_{12,MUT}$. Loss components are present due to the substrate loss and MUT loss, which are modeled by R_{sub} and $G_{12,MUT}$, respectively. EM simulations show that the capacitor qualify factor in air is approximately 4.7 at 10 GHz and degrades to 1.7 when loaded with a MUT with permittivity of 10 and tan $\delta = 1$. While this sensor capacitor Q is lower than anticipated due to an error in the substrate loss estimation in the initial design phase, it is only a minor

contributor to the total oscillator tank Q and it does not have a major impact on the overall system performance.

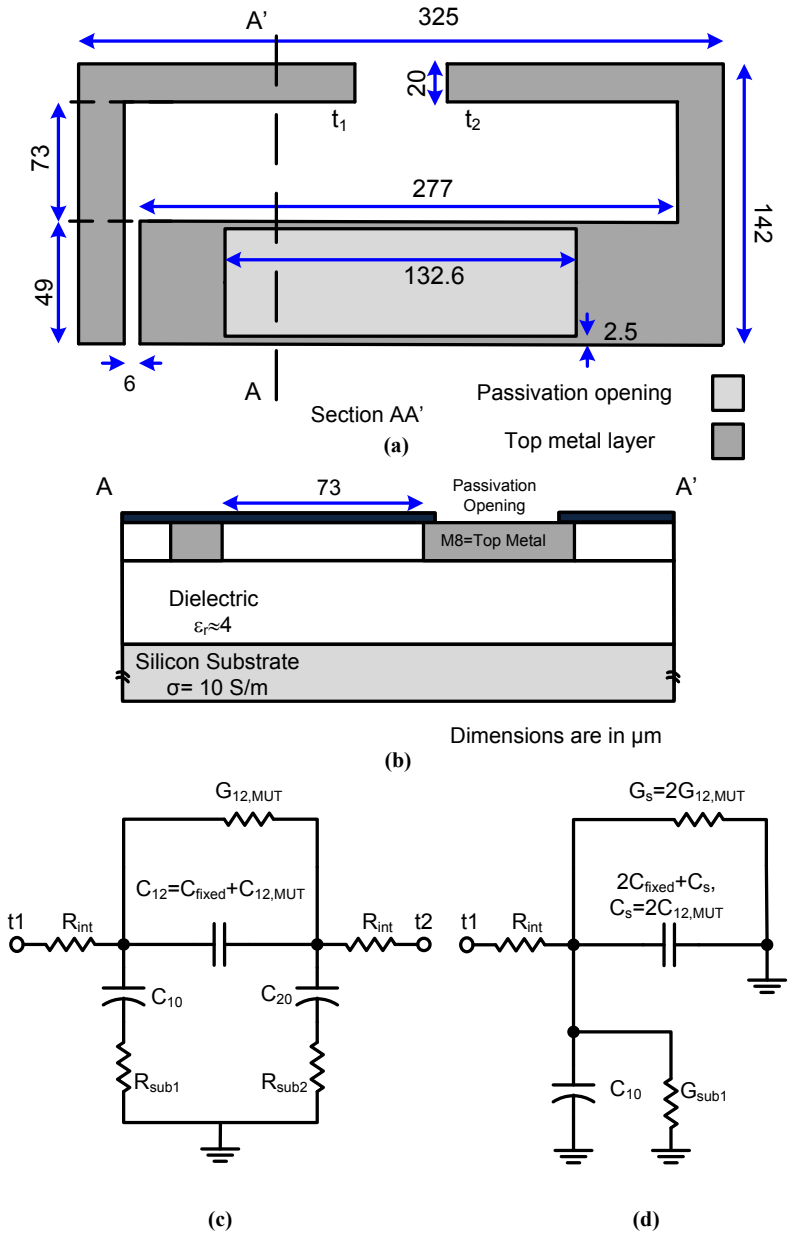


Figure 3.6: The sensor capacitor. (a) Top view of the sensor, (b) cross section (AA') view of the sensor, (c) differential electrical model seen between t1 and t2, and (d) single-ended version of the capacitor model. All dimensions are in microns.

Table 3.2: Sensor capacitor model parameters in AIR

C_{12}	7 fF
C_{10}	18 fF
C_{20}	55 fF
G_{sub1}	0.32 mS
G_{sub2}	1.15 mS
R_{int}	0.55 Ω

When the sensor is exposed to air, the fringing component consists only of $C_{12,air}$ due to air being lossless. After depositing a MUT with permittivity of $\varepsilon_r(\omega) = \varepsilon'_r(\omega) - j\varepsilon''(\omega)$ the fringing component changes to the parallel combination of $C_{12,MUT}$, and a conductive part, $G_{12,MUT}$. Neglecting the sensor interconnect resistance, R_{int}, the equivalent parallel-plate capacitance and conductance of the sensing element are approximately given by

$$\begin{aligned} C_{12,MUT} &= \varepsilon'_r(\omega) C_{12,air} \\ G_{12,MUT} &= \omega \varepsilon''_r(\omega) C_{12,air}. \end{aligned} \tag{3.8}$$

Fig. 3.6 (d) shows the equivalent half circuit model, where C_s is the effective capacitance proportional to the real part of the material's dielectric constant, $C_s = 2\varepsilon'_r(\omega) C_{12,air}$, and G_s is the effective parallel conductance modeling the effect of the material loss, $G_s = 2\omega\varepsilon''_r(\omega) C_{12,air}$.

The capacitance C_s changes with ε'_r and with the height of the MUT deposited on top of the sensing capacitor [2]. EM simulations for the sensing capacitor were

performed using Sonnet†, with Fig. 3.7 showing the value of the sensing capacitance versus the MUT height for different values of ε'_r up to 30. The capacitance increases with MUT height until saturating for heights larger than 50 μm, which is considered to be the sensor EM field saturation height.

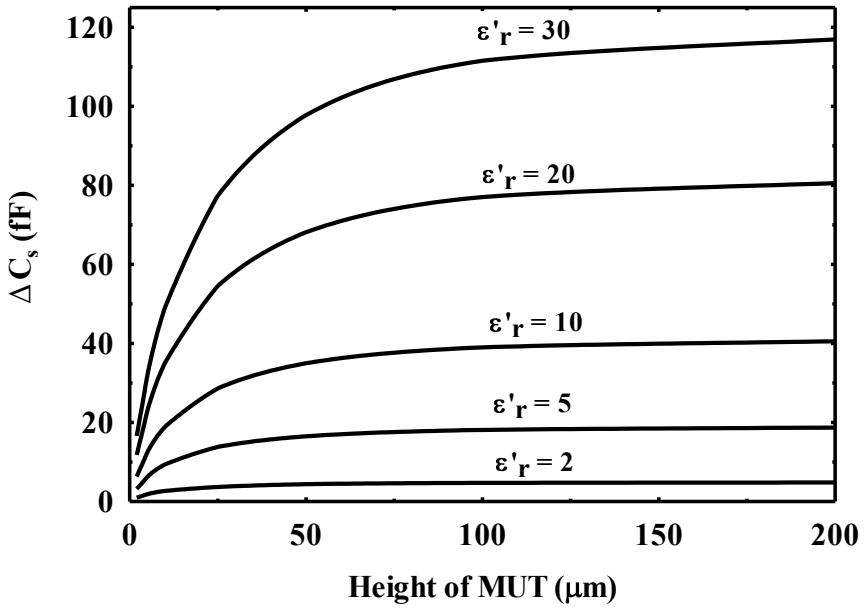


Figure 3.7: Sensing capacitance variations versus the deposited height of the MUT for five ε'_r values.

A more detailed expression for the sensor input capacitance is obtained from the total admittance at terminal t1, including the sensor interconnect resistance.

$$Y_{t1} \cong j\omega C_o \frac{1 - R_{int}G_o}{1 + \omega^2 R_{int}^2 C_o^2} + G_o \frac{1 + \omega^2 C_o^2 R_{int}/G_o}{1 + \omega^2 R_{int}^2 C_o^2}, \tag{3.9}$$

where $G_o = G_{sub} + G_s$, and $C_o = 2C_{fixed} + C_s + C_{10}$.

†Sonnet Software Inc.: www.sonnetsoftware.com

Equation (3.9) shows that in addition to the sensor capacitance terms, the sensor conductance can impact the total equivalent capacitance at t1 due to the interconnect resistance term. R_{int} should be minimized in order to minimize the effect of the sensor conductance on its capacitance. As shown in Table 3.2, R_{int} value of 0.55 Ω is achieved by using wide top-level metal connections. Fig. 3.8 shows that this allows for a nearly linear relationship between Cs and ε'_r, with the loss tangent (tan δ) having only a small effect on the value of C_s for ε'_r less than 10.

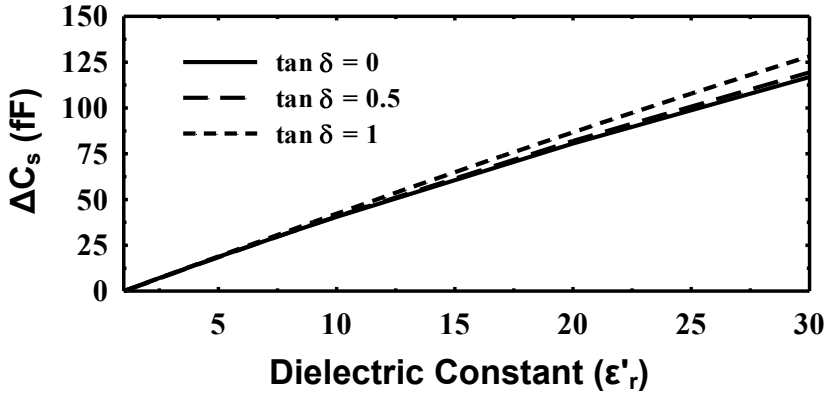


Figure 3.8: Sensing capacitance variations versus ε'_r of MUT for height 200 μm (above saturation height) at 10 GHz.

3.3.2 Sensing VCO

Fig. 3.9 shows a simplified schematic of the sensing VCO used to measure the $C_s(\omega)$ capacitance change due to the MUT deposition. The large intrinsic transconductance, with relatively small parasitic capacitance, of the NMOS cross-coupled transistors allows for high-frequency operation at the nominal 1.2 V supply voltage. In addition to the sensing capacitor, inductor L_1 and capacitor C_1 make up the os-

cillator's resonance tank. By applying the MUT, $C_s(\omega)$ changes and the frequency of oscillation shifts by a value of Δf. Assuming C_1 is much larger than $C_s(\omega)$, there is a linear relationship between $\Delta f/f_o$ and the relative C_s capacitance change for small frequency shifts.

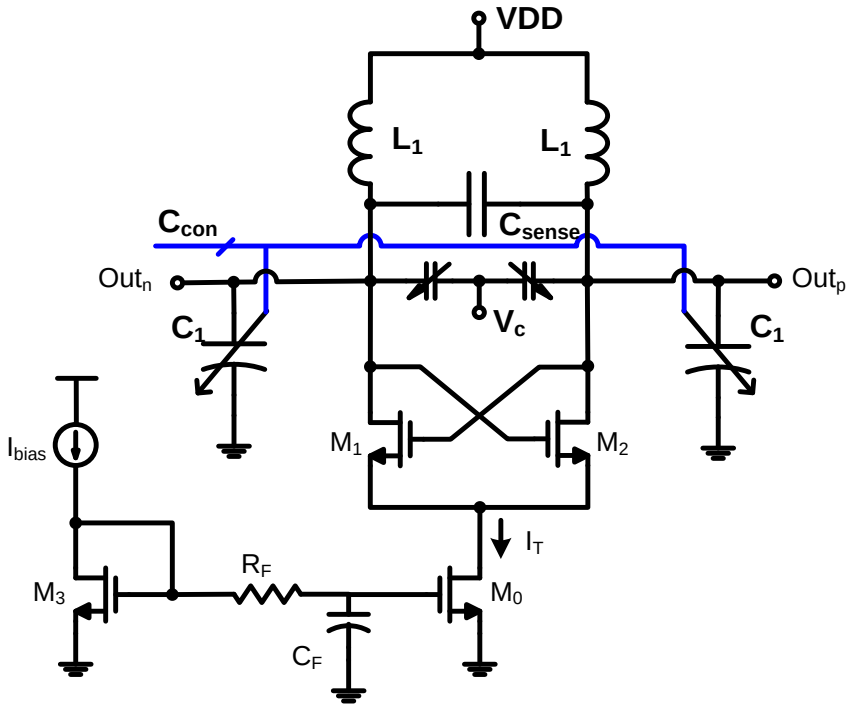


Figure 3.9: Simplified schematic of the NMOS cross-coupled sensing VCO.

$$\Delta f/f_o \approx -\frac{1}{2}\frac{\Delta C_s}{(C_1+C_s)} \approx -\frac{(\varepsilon_r'(\omega)-1)C_{12,air}}{(C_1+C_s)}$$

where f_o is the resonance frequency in air.

The simulation results of Fig. 3.10, which show the percentage variation of the VCO resonance frequency with ε_r' for different values of tan δ, verify this linear relationship and show only a small impact due to tan δ. Note that the material loss, or

ε_r'', can affect the frequency shift due to two reasons: (1) It can potentially change C_s. However, as shown in the previous subsection, ε_r'' has a small effect on C_s. (2) Loss variations result in amplitude variations, which translate into frequency variations due to amplitude modulation to frequency modulation (AM-FM) conversion [33]. This is a non-linear process, as shown in the VCO simulation results of Fig. 3.11. For small amplitudes up to around 0.45 V, the frequency is nearly constant versus the amplitude. However, as the amplitude further increases, the frequency decreases dramatically. Thus, to minimize the AM-FM conversion the selected range for the VCO single-ended amplitude is designed below 0.45 V.

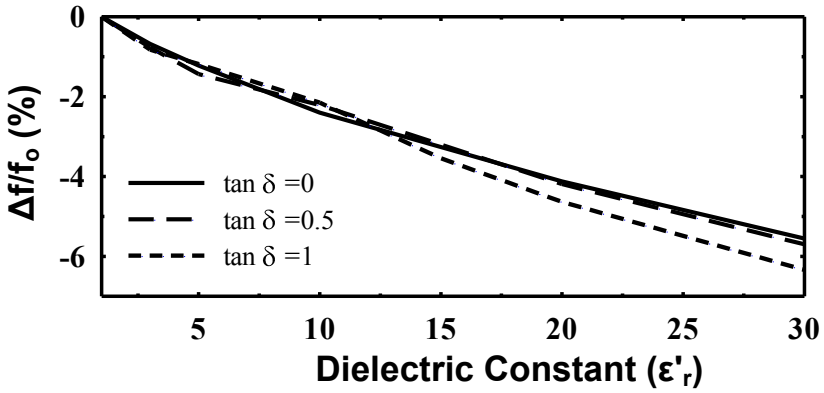


Figure 3.10: Percentage variation of the resonance frequency versus ε_r' for different values of tan δ at a MUT height of 200 μm.

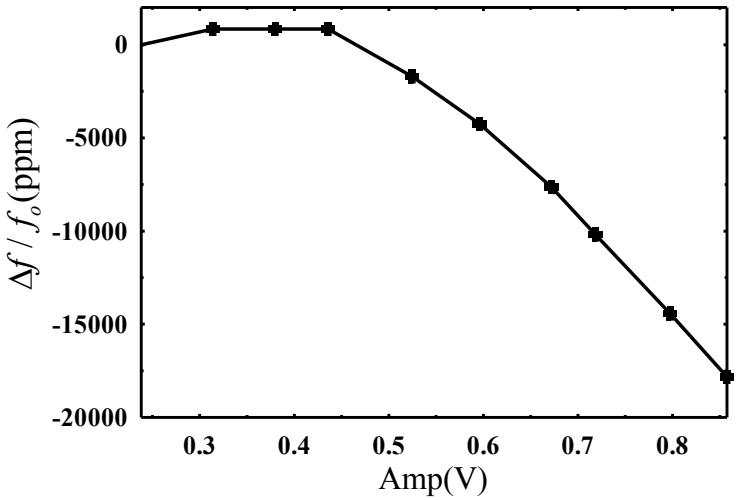


Figure 3.11: Percentage variation of the VCO output frequency versus the single-ended amplitude level.

3.4 Circuit Implementation

3.4.1 Sensor and Reference VCOs

In order to track the frequency drift of the sensing VCO due to environmental conditions and low frequency noise, a reference VCO is also employed as shown in Fig. 3.12(a). Since the frequency shift is measured as the difference in the oscillating frequency of both the sensing and reference VCOs, any correlated noise is filtered [26]. While noise correlation is maximized with the sharing of as much elements as possible, with the best scenario involving the sharing of all VCO components except the sensing and reference capacitors, the periodic enabling of the VCOs in this case necessitates a high-frequency switch, which degrades the tank quality factor considerably at 10 GHz. However, it is still possible to share the tail current source, which represents a main source of flicker noise, between the two VCOs with a low-frequency switch. Thus, the VCO noise contribution in the system frequency

shift measurements is affected only by the non-common elements, which include the cross coupled pair and the LC tank. It is worth mentioning that the applied MUT has negligible impact on both the sensor and reference VCO tank inductance due to the virtually unity relative permeability of the materials under study. Moreover, any changes in the inductor's parasitic capacitance due to MUT application is minimized due to the 1 μm passivation layer between the MUT and the inductors.

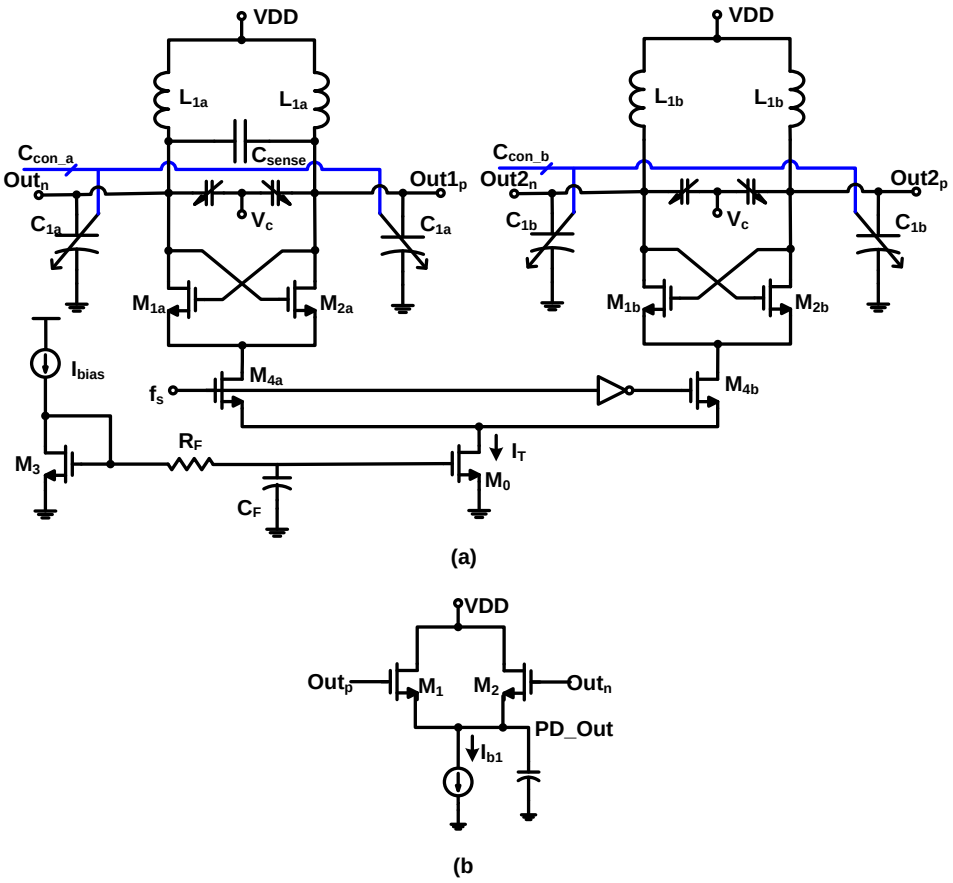


Figure 3.12: (a) Schematic of the shared-bias VCO circuits (the sensing VCO and the reference VCO) with a common tail current source to increase correlated noise. (b) Peak detector schematic.

The VCO phase noise should be minimized to enhance the sensor sensitivity, particularly at low frequency offsets where flicker noise dominates. In order to achieve this, the following design techniques are implemented: (1) The inductor quality factor is maximized at the operating frequency by employing a single-turn inductor using wide, 4 μm thick, top metal (Al) tracks that are 5.75 μm from the substrate, resulting in an inductor factor (Q_{L1}) of around 18. When varactor and sensor capacitor losses are included, the total tank Q degrades to 10 in air and around 7 when loaded with a MUT with permittivity of 10 and tan $\delta = 1$. (2) A low pass filter formed with R_F and C_F reduces the noise contribution of the bias transistor M_3.

In order to minimize the phase noise due to AM-FM conversion, the oscillator's bias current is adjusted to keep the single-ended oscillation amplitude around 0.45 V (Fig. 3.11). A peak detector, shown in Fig. 3.12(b), is connected to the VCO output to sense the amplitude level which is used to control the amplitude.

Table 3.3 summarizes the VCO transistor sizes and tank component values. Post-layout simulations show that the VCO operating near 10 GHz has a 7% tuning range, phase noise of -107 dBc/Hz at a 1 MHz offset, and 9 mA current consumption.

Table 3.3: Sizes of transistors in VCO

Transistor	$W(\mu)/L(\mu)$
M_0	480/0.8
M_1, M_2	22/0.1
M_3	80/0.8
M_4	768/0.1
L_1	220 pH
C_1	$\approx$ 1 pF

3.4.2 Frequency Divider

Fig. 3.13 shows a detailed block diagram of the on-chip integer divider. In order to provide flexibility in reference clock selection, the integer divider has a programmable ratio from 256 to 504 with a step of 8. The divider is partitioned into current-mode logic (CML) stages, which offer high frequency operation and superior supply noise rejection, for the initial divide-by-8, followed by CML-to-CMOS conversion and the use of static CMOS circuitry to implement the remaining division in a robust and low-power manner.

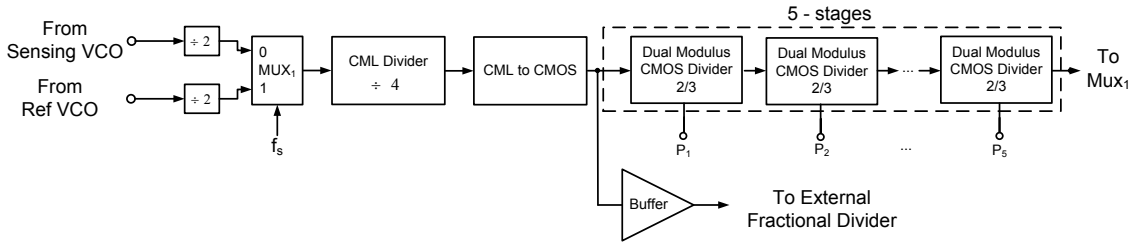


Figure 3.13: Integer frequency divider block diagram.

Two independent CML divide-by-2 blocks are utilized for the initial 10 GHz frequency division in order to provide sufficient isolation between the sensor and reference VCOs and also reduce oscillator loading (Fig. 3.14(a), (b)). These initial dividers are AC coupled to the VCO for proper biasing and consume 2 mA each with an effective 12 GHz bandwidth. A MUX unit then selects which divided clock is placed in the loop and also serves as a buffer to drive a second CML divide by 4 stage. As this second divider stage works near 1.25 GHz, it only consumes 0.3 mA. The CML-to-CMOS converter stage shown in Fig. 3.14(c) [34] drives both a buffer to the external fractional divider and the on-chip 5-stage dual-modulus 2/3 divider

shown in Fig. 3.14(d) [35] that provides a programmable division ratio from 32 to 63 with a step of 1.

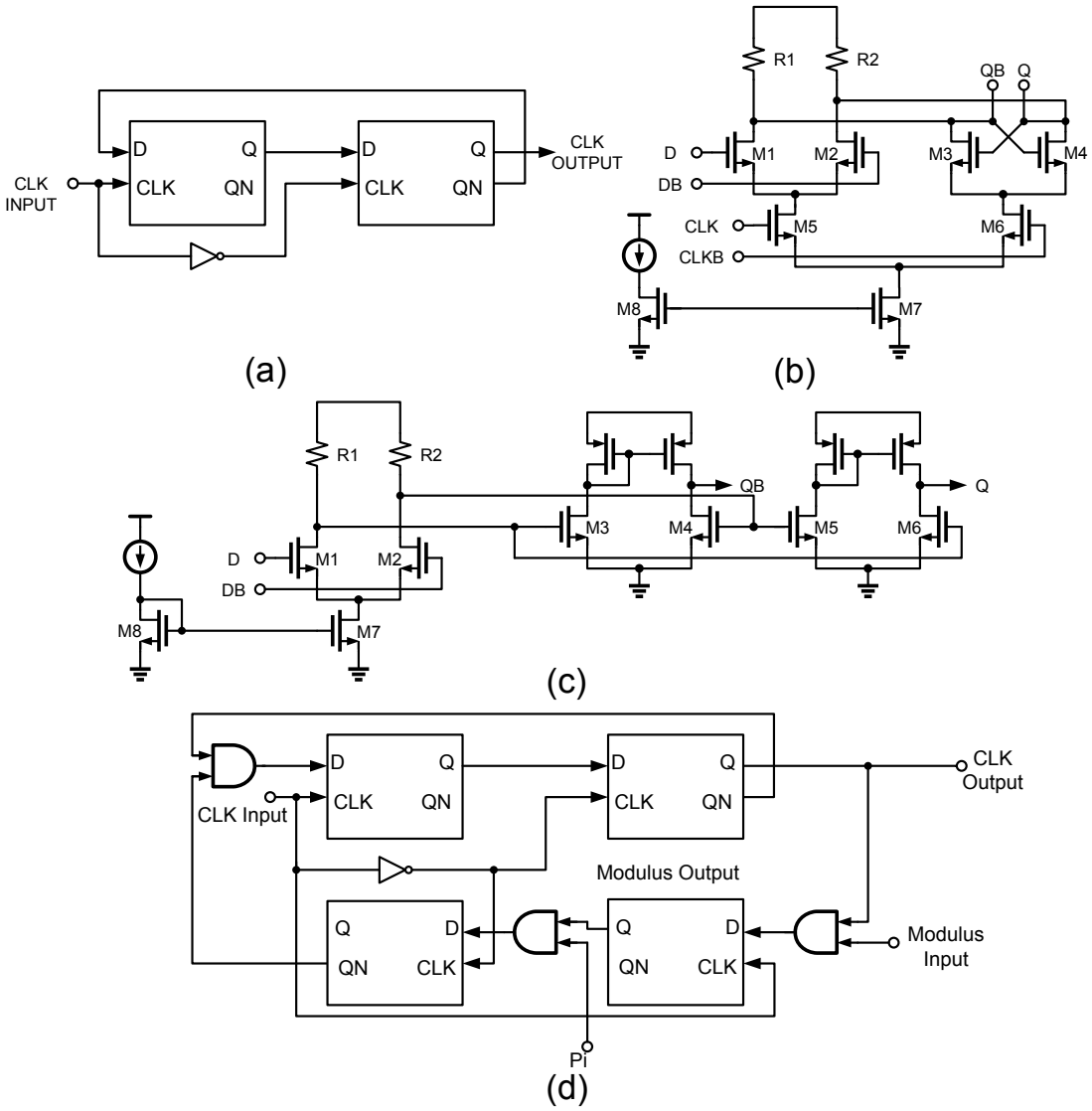


Figure 3.14: Schematics of (a) the CML-based divide-by-2, (b) the CML latch, (c) the CML-to-CMOS converter, and (d) the dual-modulus 2/3 divider.

3.4.3 PFD and Charge Pump

The phase-frequency detector (PFD) is implemented using the common topology shown in Fig. 3.16 [36]. A relatively low 25 MHz reference frequency for the 90 nm CMOS technology allows for a static CMOS design for robustness and low power consumption.

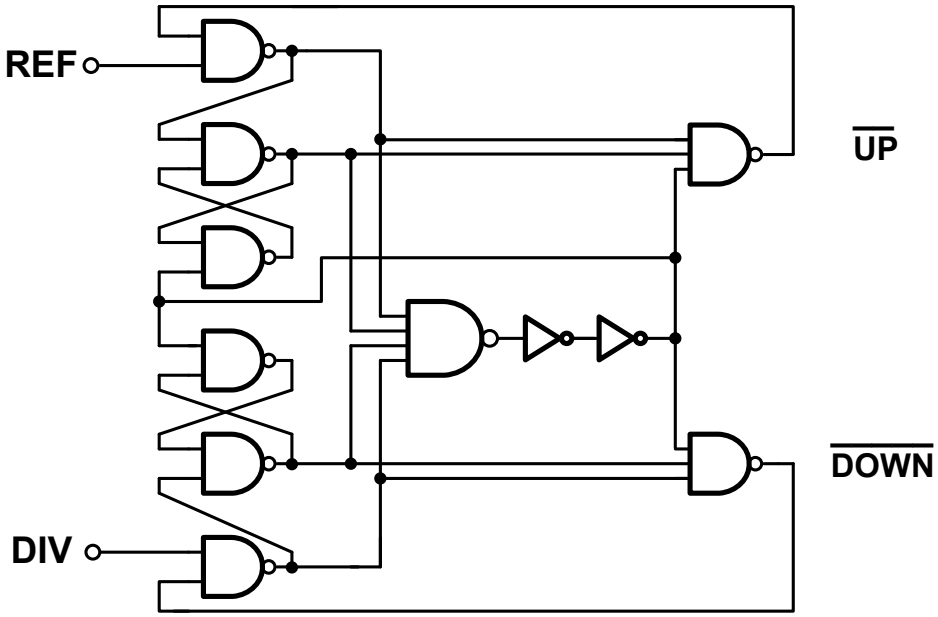


Figure 3.15: PFD schematic.

Fig. 3.16 shows the charge pump (CP) schematic [36], [37]. Here current from the M5/M6 down/up current sources is steered between a path attached to the loop filter and an auxiliary path connected to a V_{ref} voltage. This approach allows the current sources to conduct current at all times, which reduces the charge sharing that can occur if the current source drain voltages completely discharge to the sup-

ply voltages and results in lower deterministic disturbances on the control voltage. Improved matching between the charge pump up/down currents is also achieved by using dummy switch transistors M8 and M9 in the bias current mirror path.

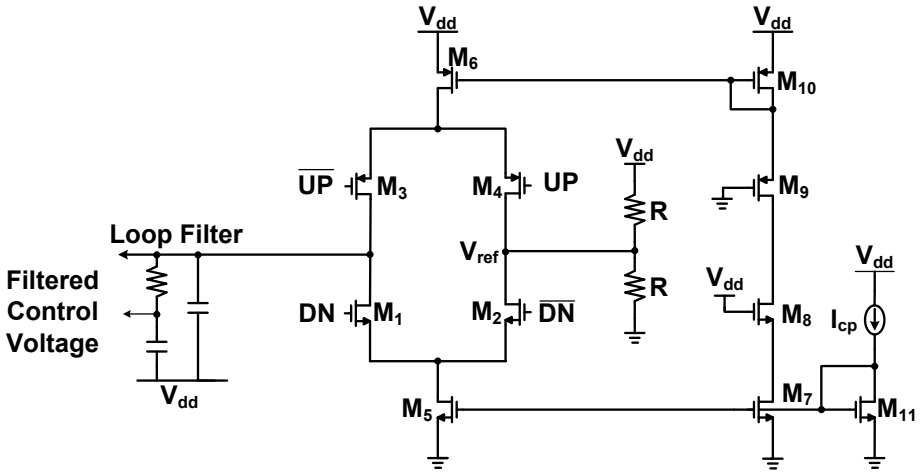


Figure 3.16: Charge pump schematic.

3.4.4 S/H and Comparator

The S/H and comparator circuits are shown in Fig. 3.17. As mentioned in Subsection 3.2, the filtered VCO control voltage is sampled when both the sensor and reference oscillator are in the PLL loop. The f_s clock signal controls the transmission-gate switches to hold the control voltage on a 1pF capacitor, C. These sampled control voltage signals are applied to a dynamic voltage-mode sense-amplifier comparator. This comparator's output is buffered through a series of inverters, stored with an SR latch, and driven off-chip for digital filtering to control the adjustable divider. While the kHz-range sample clock frequency relaxes the comparator design, it is important to reduce the comparator input-referred noise, as it appears directly on the critical VCO control voltage. Note that while the comparator offset also directly

contributes to the system offset, this is less critical because it can be measured and canceled through the sensor calibration procedure described in Subsection 3.6.2.

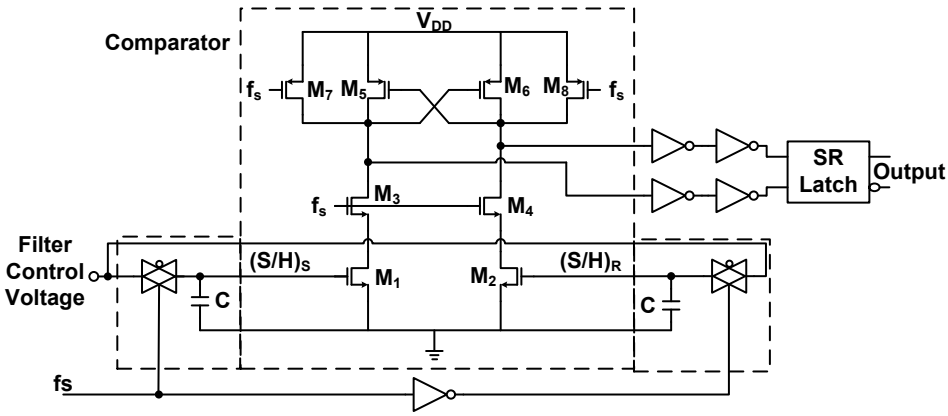


Figure 3.17: Comparator and sample and hold circuits.

3.4.5 System Sensitivity

As mentioned in Subsection 2.3, amongst the core PLL circuits, the VCO, charge pump, and loop filter resistor contribute to the simulated closed-loop PLL output phase noise of Fig. 3.18. Here a phase noise of -88 dBc /Hz is achieved at a 1MHz offset. Using the simulated noise from each block and the transfer function from that block to the control voltage, an overall integrated noise is calculated and converted to a frequency noise using a K_{vco} of 600 MHz/V, resulting in a 2 ppm_{rms} frequency noise. However, as the comparator for the bang-bang control loop is directly attached to the control voltage, its noise must also be carefully considered. Utilizing the dynamic comparator noise simulation procedure described in [38] results in a comparator input-referred noise of 0.2 mV_{rms} which, using (5), is equivalent to 12 ppm_{rms} with a K_{vco} of 600 MHz/V. Combining the noise contributions statistically yields an overall system noise estimate of 12.2 ppm_{rms}, indicating that the overall system noise is

actually dominated by the comparator of the bang-bang control loop. This insight allows for further performance improvements in future implementations by locating the comparator after a low-noise pre-amplifier stage designed for reduced input-referred noise [39]. Note that the above analysis is for air loading, and the VCO performance will degrade when loaded with a lossy MUT. Simulations indicate that when loaded with a MUT of ε_r' of 10 and tan δ of 1, the phase noise degrades by 5 dB. However, due to the noise of the comparator used in the current design, this MUT-loading noise degradation has minimal impact on overall system sensitivity.

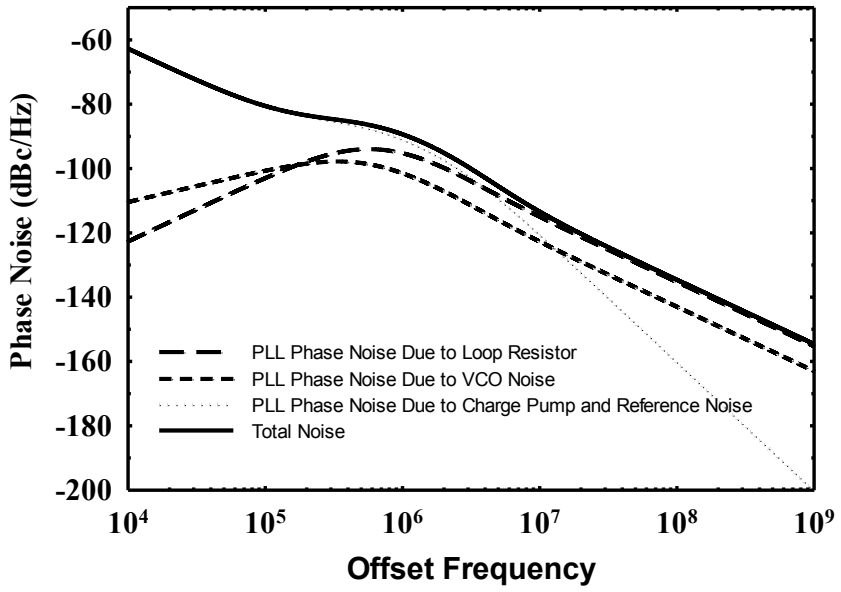


Figure 3.18: Simulated closed-loop PLL 10 GHz output phase noise.

3.5 System Integration and Test Setup

3.5.1 System On-Board Integration

Fig. 3.19 shows the chip microphotograph of the PLL-based dielectric sensor, which was fabricated in a 90 nm CMOS process and occupies a total chip area of 2.15mm^2. As detailed in Table 3.4, the overall chip power consumption is 22 mW, with the VCO and high-frequency dividers consuming the most power. An open-cavity micro lead frame (MLP) 7×7 mm^2 QFN 48 package is used for chip assembly[‡] to allow for MUT deposition on top of the sensing capacitor. All electrical connections between the chip and the package lead frame are made via wirebonding.

Table 3.4: Sensor chip power consumption

Block	Power Consumption (mW)
VCO	10.8
High Frequency Dividers	7.2
PFD + CP	0.4
Output Buffer	3.6
Total	22

An off-chip commercial discrete fractional frequency divider (ADF4157) from Analog Devices[§] is utilized in order to achieve high resolution in the frequency shift measurements. The external divider has 25-bit resolution, which allows for potential frequency shift measurements down to 6×10^{-4} ppm, considering the divide-by-8 on-chip CML divider. This implies that the system is not limited by the divider

[‡]Majelac: www.majelac.com
[§]Analog Devices: www.analog.com

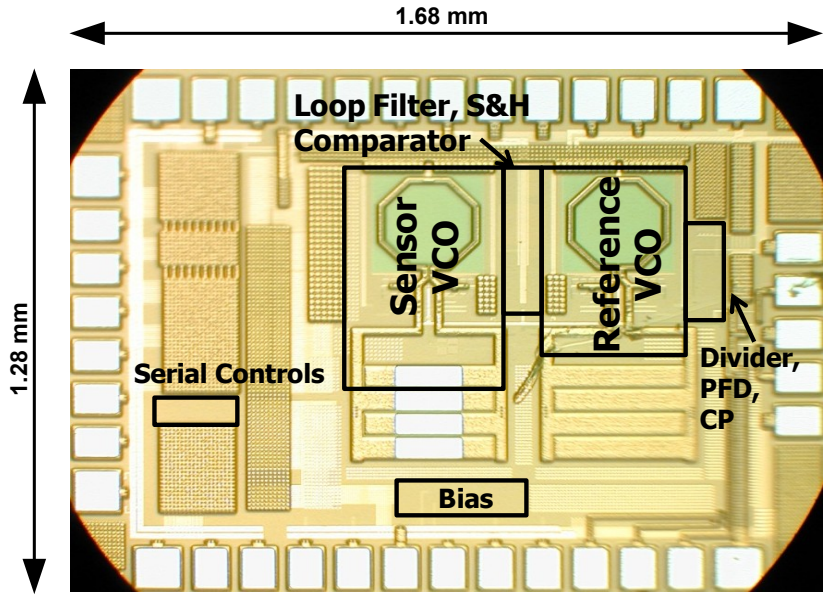


Figure 3.19: Micrograph of the PLL-based dielectric sensor chip.

quantization noise, but rather the system random noise discussed earlier.

Fig. 3.20 shows the photograph of the PCB with the mounted sensor chip and the external divider. The sensor chip interfaces with the external divider with a buffered version of the on-chip CML divide-by-8 output at 1.25 GHz (Fig. 15) driven to the external divider, and the divided output signal at 25 MHz fed back to the CMOS chip to MUX_2 (Fig. 3.1) that selects the PFD input based on the switching clock phase. Simple level-shifting interface ICs are used to condition the comparator's serial output bits to levels sufficient for the PC, which performs the digital filtering. The frequency shift measurement algorithm of Fig. 3.5 is performed automatically via a Labview[¶] program, such that the MUT is deposited on top of the sensor, the external reference divider is adjusted with a successive-approximation procedure, and the corresponding frequency shift is measured directly.

[¶]www.ni.com/labview

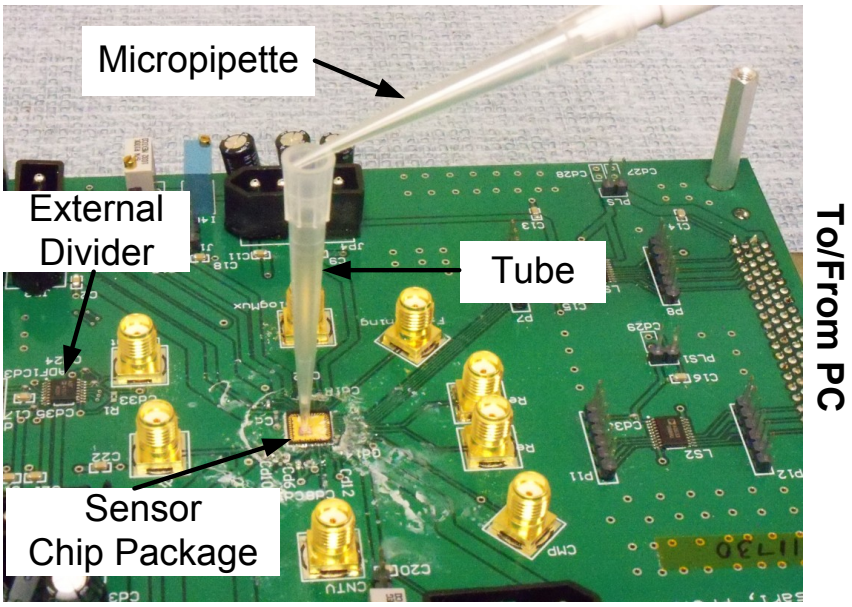


Figure 3.20: Photograph of the PCB with the chip, external divider, micropipette, and the MUT application tube indicated.

3.5.2 Chemical Sensing Test Setup

Organic chemical liquids, including Methanol and Ethanol and their mixtures, are applied to the sensor chip via a plastic tube fixed on top of the chip [2]. Due to the 1.2mm tube diameter being comparable to the chip area and tube mechanical handling limitations, both the reference and sensing VCOs are covered by the MUT during testing. In order to avoid the effect of the MUT on the reference VCO, the metal capacitor in Fig. 3.19 is not attached to the reference oscillator. While this does result in a systematic offset between the VCOs, this is easily measured with the sensing capacitor exposed to air and later calibrated out.

In order to control the volume of the material applied on the sensor chip, a Finnpipette[‖] single-channel micropipette is utilized to apply the liquid via the tube.

[‖][Online]. Available: http://www.thermoscientific.com

After material application the tube is capped to avoid evaporation. All measurements were performed with volumes less than 20 μL, which is sufficient to cover the sensor in excess of the saturation height due to the small sensor size.

3.6 Experimental Results

This subsection discusses the fractional-N PLL-based chemical sensor experimental results. First, key measurements of the PLL and system sensitivity are presented. Next, data is shown with the system characterizing organic chemical mixtures.

3.6.1 PLL and Sensitivity Characterization

The output spectrum and phase noise of the closed-loop PLL with the sensor VCO in the loop is measured at the output of the divide-by-8 CML block, as shown in Fig. 3.21 and Fig. 3.22, respectively. For the 1.3 GHz signal, reference spurs less than -60 dBc and a phase noise of -97 dBc/Hz at a 1 MHz offset are achieved. This phase noise converts to -79 dBc/Hz at a 1 MHz offset for the on-chip 10.4 GHz signal. As shown in Fig. 3.23, the PLL achieves a 640 MHz locking range between 10.04 to 10.68 GHz and a 885 MHz/V K_{vco}, at control voltage of 0.85 V, with the sensing VCO in the loop. Due to the absence of the sensor capacitor, the PLL achieves a 650 MHz locking range between 10.49 to 11.14 GHz and a 925 MHz/V K_{vco}, at control voltage of 0.85 V, with the reference VCO in the loop. Similar phase noise is achieved for both VCOs operating inside the PLL versus the control voltage.

In order to characterize the system noise level, the bang-bang divider control is set in open-loop and a CDF of the average comparator output is produced by varying the external divider value, N_R. A switching frequency of $f_s = 1$ kHz is employed in order to allow enough time for the PLL to settle with high accuracy. The results in Fig. 3.24 are fitted to a Gaussian distribution and a system noise sigma of 15 ppm is extracted. This noise value is very close to the 13 ppm predicted by previously

discussed system simulations, indicating that the comparator noise is most likely currently limiting the system performance.

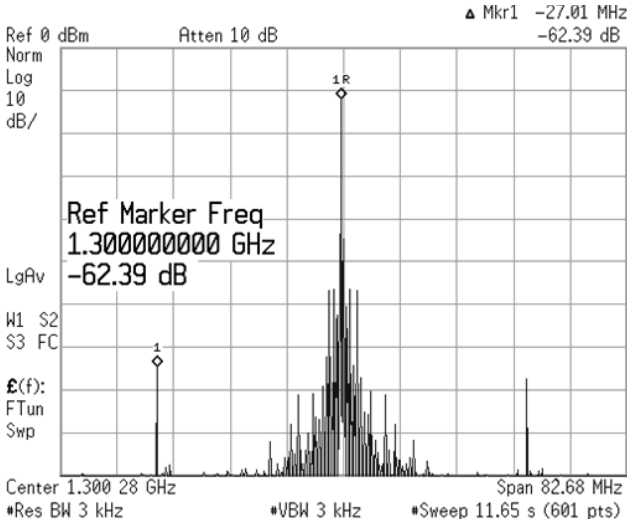


Figure 3.21: PLL output spectrum after CML divide-by-8 divider.

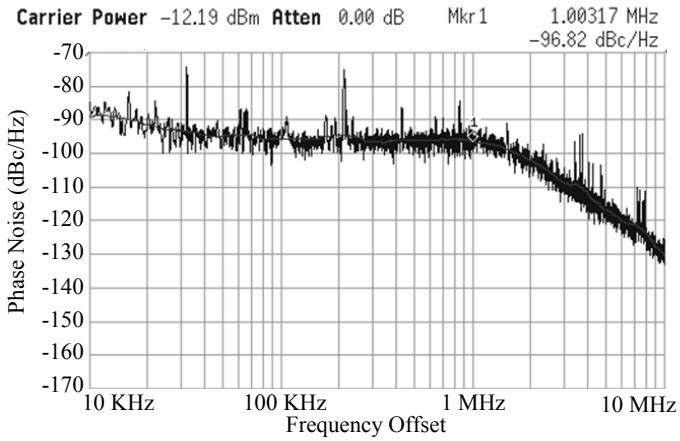


Figure 3.22: Reference VCO phase noise measurements after CML divide-by-8 divider.

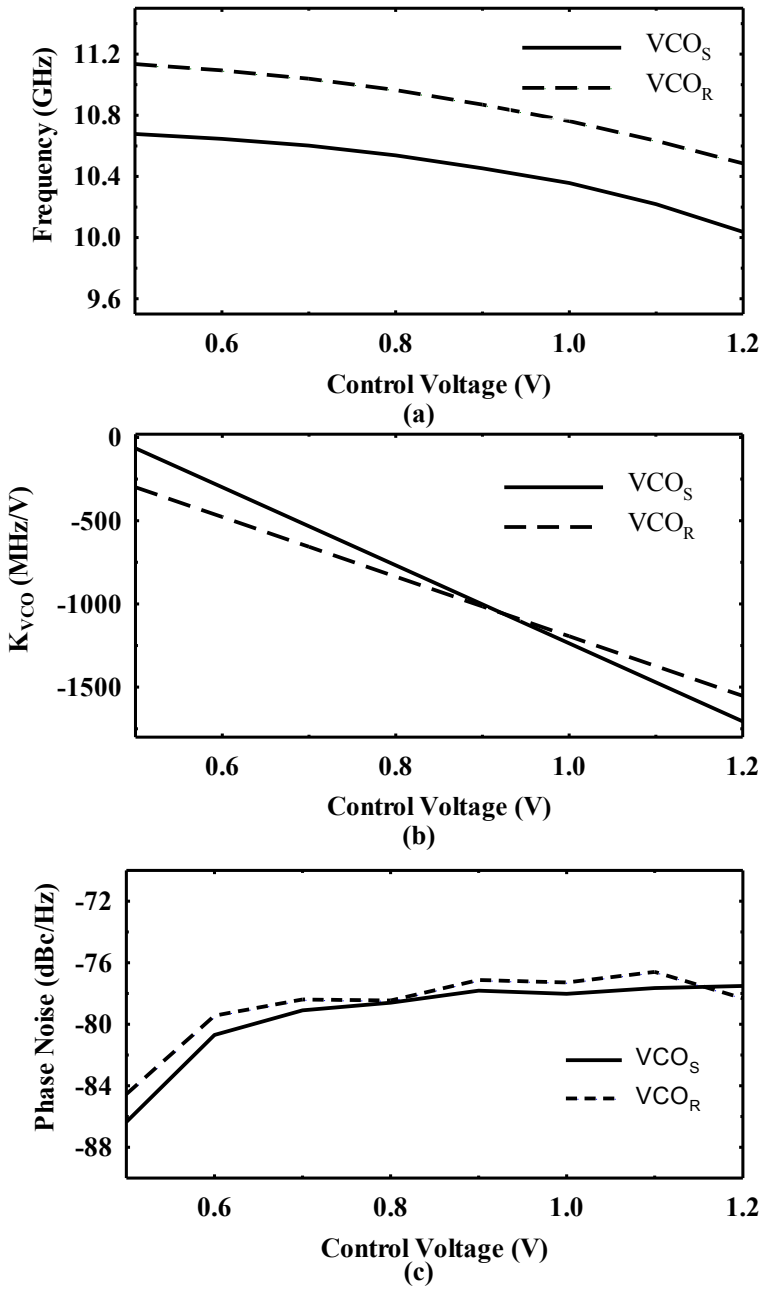


Figure 3.23: PLL measurements versus the control voltage with both reference VCO and sensor VCO: (a) VCO frequency, (b) K_{VCO}, (c) phase noise at a 1MHz offset.

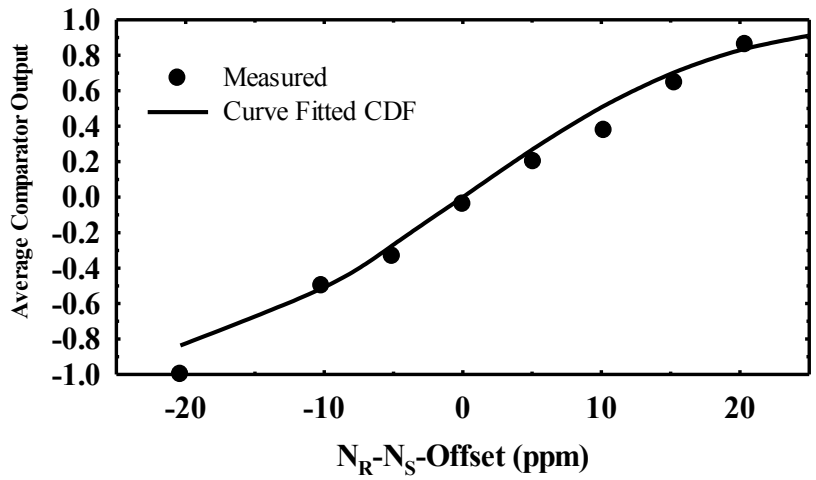


Figure 3.24: Measured average comparator output versus the difference in the divider values.

3.6.2 Chemical Measurements

Dielectric Frequency Dispersion and Mixture Theories

For pure MUTs, the complex permittivity frequency dependency follows the Cole-Cole model [24] and the complex permittivity numbers in [25]. The model is as follows

$$\varepsilon(\omega) = \varepsilon'(\omega) - j\varepsilon''(\omega) = \varepsilon_{r,\infty} + \frac{\varepsilon_{r,0} - \varepsilon_{r,\infty}}{1 + (j\omega\tau)^{1-\alpha}} \tag{3.10}$$

where $\varepsilon_{r,0}$ is the static permittivity at zero frequency, $\varepsilon_{r,\infty}$ is the permittivity at ∞, τ is the characteristic relaxation time and α is the relaxation time distribution parameter.

Binary mixtures are composed of two materials: (1) the environment (host), and (2) the inclusion (guest), with ratios of $(1 - q)$ and q, respectively. The complex permittivity of a binary mixture is a function of the complex permittivities of the

two constituting materials and the fractional volume ratio, q. This relationship is mathematically defined as follows [40]- [41]:

$$\frac{\varepsilon_{eff} - \varepsilon_e}{\varepsilon_{eff} + 2\varepsilon_e + \nu(\varepsilon_{eff} - \varepsilon_e)} = q\frac{\varepsilon_i - \varepsilon_e}{\varepsilon_i + 2\varepsilon_e + \nu(\varepsilon_{eff} - \varepsilon_e)} \tag{3.11}$$

where ε_{eff} is the effective mixture permittivity, ε_e is the permittivity of the environment, ε_i is the inclusion permittivity, and ν is a parameter to define the employed model. ν has values of 0, 2, and 3 corresponding to Maxwell-Garnett, Polder-van Santen, and quasi-crystalline approximation rules, respectively.

Sensor Calibration

As previously described in the Fig. 3.5 flowchart, the MUT is deposited on the sensor and the corresponding frequency shift is measured to determine the permittivity. Due to process variations, system offset, and K_{vco} mismatches, the relationship between frequency shift and permittivity has to be calibrated for stable and accurate measurements. While (10) predicts an ideally linear shift in frequency with MUT ε_r', the use of a higher-order polynomial function allows additional degrees of freedom to calibrate for items such as K_{vco} mismatches. A quadratic equation is used to describe the frequency shift in MHz as a function of the permittivity [2]

$$\Delta f = a(\varepsilon_r' - 1)^2 + b(\varepsilon_r' - 1) + c \tag{3.12}$$

where a, b and c are the calibration constants. Note that the constant c represents the system offset mentioned in Subection 3.2. Three calibration materials are required to determine these constants. In this work air, pure ethanol, and pure methanol are used as calibration materials whose ε_r' at the testing frequency (10.4 GHz) are 1, 4.44-j2.12 ($\tan\delta = 0.48$) and 7.93-j7.54 ($\tan\delta = 0.95$), respectively [25]. Deposit-

ing each of these calibration materials on the sensor independently and measuring the induced frequency shifts allows extraction of a, b, and c, which are found to be -0.0162, 19.9046 and 360.0808, respectively. During this calibration process the comparator output is digitally filtered by averaging for 100-200 bits in order to ensure stable measurements. Fig. 3.25 shows how the measured frequency shift Δf versus permittivity ε_r' matches with the calibration curve.

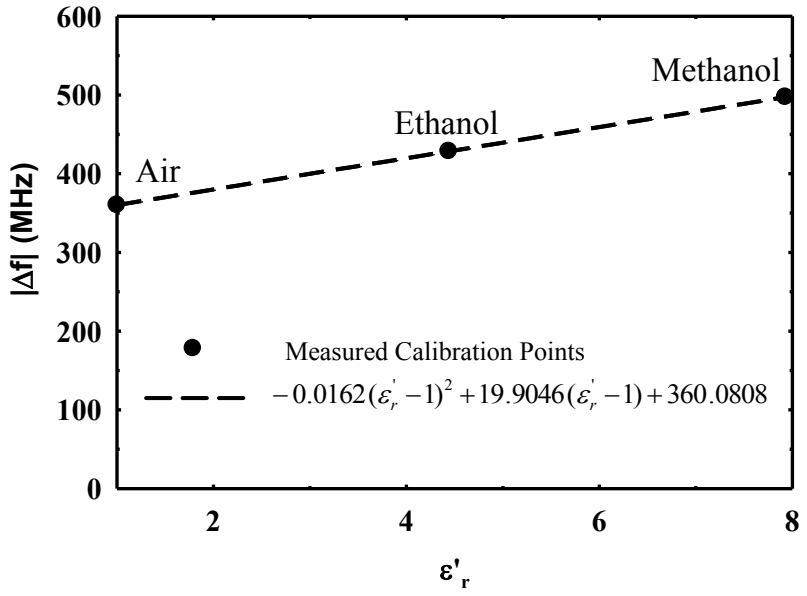


Figure 3.25: Fitted absolute frequency shift $|\Delta f|$ versus ε_r' at the sensing frequency of 10.4 GHz with the calibration points indicated.

Mixture Characterization and Permittivity Detection

As a proof of concept, the system is used to detect the permittivity of a mixture of Ethanol and Methanol with several ratios of q and $(1-q)$ respectively, $0 \leq q \leq 1$. Mixture accuracy is ensured by preparation with high volumes using a micropipette

with 1 μL accuracy. For example, with a q of 0.4 and a total volume of 500 μL, 200 μL of pure Ethanol is mixed with 300 μL of pure Methanol using the micropipette. Then 20 μL is taken from the mixture and deposited on top of the sensor for detection. For this case, the absolute value of the frequency shift is then measured and found to be 454.45 MHz ($|\Delta f - c| = 94.37$ MHz). Using (3.12) and the values of a, b and c, the permittivity is then estimated to be 5.76. Repeating this procedure for other q values, Fig. 3.26(a) shows the frequency shift values versus q, and Fig. 3.26(b) compares the measured ε' versus q with the theoretical Polder-van Santen mixture model ($\nu = 2$) (3.11). The maximum difference between the measured and theoretical permittivity is less than 1.5%, as shown in Fig. 3.26(b). Note that the maximum error values are achieved for mixtures with comparable host and guest levels. Higher accuracy levels are achieved for more extreme ratios, with the sensor able to differentiate mixture permittivities with fractional volume down to 1%. These measurements show that the detected permittivities fit quite well to the theoretical values and that the system can characterize mixtures at a high accuracy level.

Table 3.5 summarizes the performance and compares the results with prior work. This work achieves a higher level of integration and higher frequency measurement capabilities relative to the work of [23], [42] - [43]. Compared to the system in [2], the presented fractional-N PLL-based sensor achieves a more than 2X improvement in permittivity error at comparable power consumption and CMOS IC area.

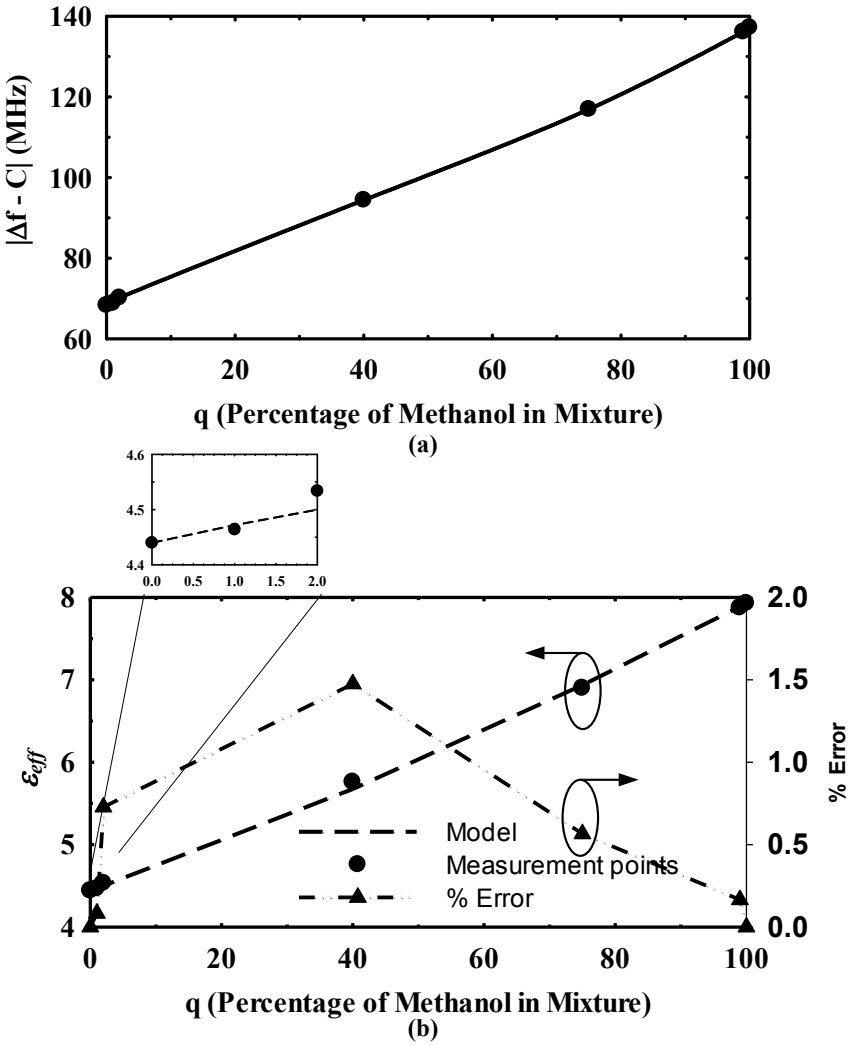


Figure 3.26: Measurement results of an ethanol-methanol mixture, (a) frequency shift versus the concentration of methanol in the mixture, and (b) effective dielectric constant derived from the measured frequency shifts and compared to the model with ν =2 and permittivity percentage error.

Table 3.5: Performance summary and comparison to previous work

	Operating Frequency	Sensor Read-Out Approach	Area	Power Consumption	Permittivity Error
[8]	0.4-35 GHz	S-parameter lab measurements	NA	NA	3%[a]
[23]	4.5 GHz	Discrete components [b]	NA	NA	2 %
[42]	500 - 800 MHz	Discrete components [c]	NA	NA	3 %
[44]	1, 2 and 3 GHz	Network Analyzer	112 × 2.4 mm^2 [d]	NA	0.7 % - 12 %
[43]	8 GHz	Network Analyzer	40 × 15 mm^2 [d]	NA	0.5%
[20]	120-130 GHz	Integrated reflectometer PLL in 250 nm SiGe BiCMOS	1.4 mm^2	247.5 mW	NA
[2]	7 - 9 GHz	Integrated PLL in 90 nm CMOS [e]	2.5 × 2.5 mm^2	16.5 mW	3.5%
This Work	10.4 GHz	Integrated PLL in 90 nm CMOS [f]	1.68 × 1.28 mm^2	22 mW	1.5%

[a] Error is reported at 25 GHz.
[b] The system uses fractional-N PLL, micro-controller and ADC.
[c] The system uses PLL, peak detector and micro-controller.
[d] Sensor area only.
[e] Tunable reference oscillator is required.
[f] Off-chip fractional divider is used.

System Accuracy Limitations

Although the measured 15 ppm_{rms} system noise without material application (Fig. 3.24) converts to a $0.1\%_{rms}$ permittivity value from (3.12), several error sources contribute to the 1.5% maximum error observed between the measured and theoretical permittivity values. A discussion of these error sources follows, along with proposed solutions.

- **Kvco mismatch:** While system performance is insensitive to K_{vco} nonlinearity, K_{vco} mismatch does impact the system error. The use of a higher-order polynomial curve and additional calibration materials can reduce this error term.

- **Temperature dependency:** Since permittivity measurements are performed at room temperature without precise temperature control, while 20°C permittivity values are used in the calibration procedure, any temperature variation will degrade sensor accuracy. A potential solution for future systems is to employ an accurate temperature sensor and integrated heater beside the sensing capacitor for temperature stabilization.

- **Mixing accuracy:** It is important to follow standard mixing procedures to ensure high measurement accuracy levels. Increasing the volumes mixed to obtain a given ratio can improve this.

- **Air/gas bubbles:** Any air or gas bubbles present in the material on top of the sensing capacitor will impact the measured permittivity. A more advance microfluidics structure for material dispensing is a potential solution to this issue.

3.7 Conclusion

This work presented a self-sustained fractional-N PLL-based CMOS sensing system for dielectric constant detection of organic chemicals and their mixtures at precise microwave frequencies. System sensitivity is improved by employing a reference VCO, in addition to the sensing VCO, that tracks correlated low-frequency drifts. A simple single-step material application measurement procedure is enabled with a low-complexity bang-bang control loop that samples the difference between the control voltage with the sensor and reference oscillator in the PLL loop and then adjusts a fractional frequency divider. Binary mixture characterization of organic chemicals show that the system was able to detect mixture permittivities with fractional volume down to 1%. Overall, the high-level of integration and compact size achieved in this work makes it suitable for lab-on-chip and point-of-care applications.

4. A WIDE-BAND FULLY-INTEGRATED CMOS RING-OSCILLATOR PLL-BASED COMPLEX DIELECTRIC SPECTROSCOPY SYSTEM*

4.1 Introduction

This section presents a fully-integrated CMOS PLL-based dielectric spectroscopy system that addresses the operating bandwidth and complex permittivity detection limitations of previous VCO-based BDS biosensing systems, while maintaining their advantages of efficiency and accuracy [45]. The proposed system employs a differential sensing architecture that has the advantages of both [28] and [26], but replaces the LC sensing and reference VCOs with wide tuning range ring VCOs. As the ring VCOs' oscillation frequency is a function of the delay cells' RC time constant, it is possible to detect both $\epsilon'_r(\omega)$ and $\epsilon''_r(\omega)$ by employing delay cells with sensor element loads whose capacitance and conductance (loss) changes with MUT application. A novel detection procedure is proposed which employs an amplitude-locked loop (ALL) to efficiently detect both $\epsilon'_r(\omega)$ and $\epsilon''_r(\omega)$ independently through only two frequency shift measurements. As a simple digital counter can be employed to perform these frequency shift measurements, this dramatically simplifies the read-out circuitry relative to coherent detection systems [17]− [19] that require high-resolution ADCs.

The section is organized as follows. Subsection 4.2 provides detailed derivation of the oscillating frequency of ring oscillators as function of the delay cells load capacitance and conductance at the fundamental frequency and its harmonics. The ALL-based detection procedure that de-couples the impact of MUT-induced changes

*Reprinted with permission from "A 0.18-μm CMOS Fully Integrated 0.7-6 GHz PLL-Based Complex Dielectric Spectroscopy System," IEEE Custom Integrated Circuits Conference, Sept. 2014.©2014 IEEE, and "A Wide-Band Fully-Integrated CMOS Ring-Oscillator PLL-Based Complex Dielectric Spectroscopy System," by O. Elhadidy, S. Shakib, K. Krenek, S. Palermo, K. Entesari, accepted in IEEE Transactions on Circuits and Systems I: Regular Papers, 2015. ©2015 IEEE.

in $\epsilon'_r(\omega)$ and $\epsilon''_r(\omega)$ with two frequency shift measurements along with the proposed system are explained in Subsection 4.3. Subsections 4.4, 4.5 provide the details of the circuit implementation and the complex permittivity detection measurement setup, respectively. Experimental results of the BDS prototype, fabricated in a 0.18-μm CMOS technology, are presented in Subsection 4.6. Finally, Subsection 4.7 concludes the section.

4.2 Ring-Oscillator Analysis

The oscillating frequency of N-stage ring oscillator shown in Fig. 4.1 is given by

$$f_o = \frac{1}{2Nt_d}, \tag{4.1}$$

where t_d is the delay of each stage. In case the oscillating signal is a square wave the delay can be calculated by

$$t_d = 0.7C_t/G_t, \tag{4.2}$$

where C_t and G_t are the total load capacitance and conductance of the delay stages. Substituting (4.2) in (4.1) the oscillating frequency can be calculated by

$$f_o = \frac{0.7}{N}\frac{G_t}{C_t}. \tag{4.3}$$

Equation(4.3) is not accurate for ring oscillator with small number of stages as will be shown later in this subsection. Also (4.3) assumes that the delay stages load capacitance and conductance are fixed versus frequency. This subsection provides detailed derivation of the oscillating frequency and amplitude of N-stage ring oscillator as function of the load capacitance and conductance at the fundamental frequency and its harmonics. First, the derivation is preformed considering the fundamental compo-

nent of the oscillating frequency only, then the effect of the harmonics is considered.

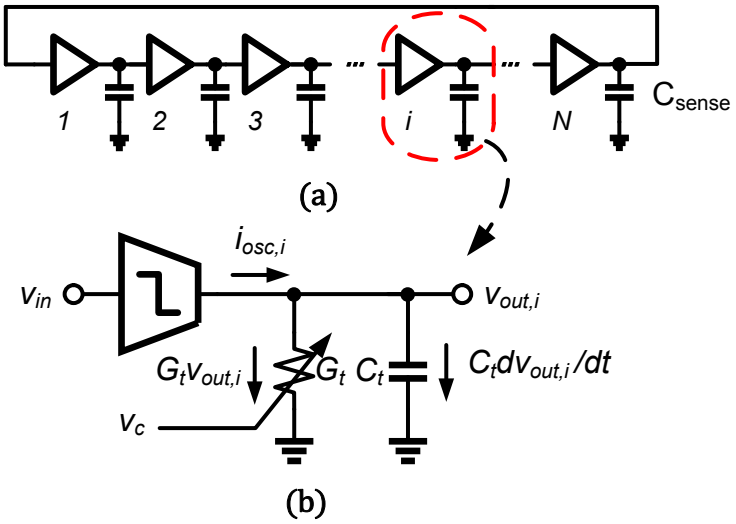


Figure 4.1: Schematic of an N−stage ring VCO and delay stage model.

The delay stages are modeled as an ideal transcoductor loaded with capacitance C_t, which includes the delay cells' loading and parasitic capacitance and the sensor capacitance, C_{sense}, and conductance G_t. At the output of stage i, the current $i_{osc,i}$ as function of the voltage $v_{out,i}$ is given by

$$i_{osc,i} = G_t v_{out,i} + C_t \frac{dv_{out,i}}{dt} \tag{4.4}$$

For oscillator with a symmetric delay stages, with bias current I_{osc}, oscillating at frequency of f_o with amplitude of A, the fundamental components of the current and the voltage at the output of each stage (assuming full current switching) are

$$i_{osc,i} = \frac{4}{\pi} I_{osc} \sin(\omega_o t), \tag{4.5}$$

$$v_{out,i} = A\sin(\omega_o t - \Delta\phi), \tag{4.6}$$

where $\Delta\phi$ is the phase shift of the delay stages. $\Delta\phi$ equals to π/N so that the total phase shift around the loop equals to 2π. Substituting (4.5) and (4.6) in (4.4)

$$\frac{4}{\pi}I_{osc}\sin(\omega_o t) = AG_t(\omega_o)\sin(\omega_o t - \Delta\phi) + A\omega_o C_t(\omega_o)\cos(\omega_o t - \Delta\phi). \tag{4.7}$$

Expanding the $\sin(\omega_o t - \Delta\phi)$ and $\cos(\omega_o t - \Delta\phi)$ terms

$$\begin{aligned}\frac{4}{\pi}I_{osc}\sin(\omega_o t) =& AG_t(\omega_o)\Big(\sin(\omega_o t)\cos(\Delta\phi) - \cos(\omega_o t)\sin(\Delta\phi)\Big) \\ &+ A\omega_o C_t(\omega_o)\Big(\cos(\omega_o t)\cos(\Delta\phi) + \sin(\omega_o t)\sin(\Delta\phi)\Big).\end{aligned} \tag{4.8}$$

Combining the coefficients of the $\sin(\omega_o t)$ and $\cos(\omega_o t)$ terms

$$\begin{aligned}\frac{4}{\pi}I_{osc}\sin(\omega_o t) =& A\Big(G_t(\omega_o)\cos(\Delta\phi) + \omega_o C_t(\omega_o) sin(\Delta\phi)\Big)\sin(\omega_o t) \\ &+ A\Big(\omega_o C_t(\omega_o)\cos(\Delta\phi) - G_t(\omega_o)\sin(\Delta\phi)\Big)\cos(\omega_o t).\end{aligned} \tag{4.9}$$

By equating the coefficients of the $\sin(\omega_o t)$ and $\cos(\omega_o t)$ terms of (4.9), the oscillating frequency and amplitude can be determined by

$$f_o = \frac{1}{2\pi}\frac{G_t(f_o)}{C_t(f_o)}\tan(\frac{\pi}{N}), \tag{4.10}$$

$$A = \frac{I_{osc}}{G_t(f_o)}\cos(\frac{\pi}{N}). \tag{4.11}$$

Next, The effect of the harmonics is considered. In this case the current and the voltage are given by

$$i_{osc,i} = \sum\nolimits_{k=1,3,5,\ldots} \frac{4}{\pi}\frac{1}{k} I_{osc}\sin(k\omega_o t), \tag{4.12}$$

$$v_{out,i} = \sum\nolimits_{k=1,3,5,\ldots} A_k \sin(k\omega_o t - \Delta\phi_k), \tag{4.13}$$

where A_k is the amplitude of the k^{th} harmonic. Similar to the first case (which consider the fundamental component only), substituting (4.12) and (4.13) in (4.4) and by equating the coefficients of the $\sin(k\omega_o t)$ and $\cos(k\omega_o t)$ terms of the result, the phase and the amplitude of the k^{th} harmonic can be determined by

$$\tan\Delta\phi_k = k\omega_o\frac{C_t(f_o)}{G_t(f_o)}, \tag{4.14}$$

$$A_k = \frac{4}{\pi}\frac{1}{k}\frac{I_{osc}}{\sqrt{(k\omega_o C_t(f_o))^2 + (G_t(f_o))^2}}. \tag{4.15}$$

Substituting (4.14) and (4.15) in (4.13), the voltage can be expressed as

$$v_{out,i} = \sum\nolimits_k \frac{1}{k}\frac{4}{\pi}\frac{I_{osc}}{G_t(kf_o)}\frac{1}{\sqrt{1+(k\omega_o\frac{C_t(kf_o)}{G_t(kf_o)})^2}}\sin\left(k\omega_o t - \tan^{-1}(k\omega_o\frac{C_t(kf_o)}{G_t(kf_o)})\right). \tag{4.16}$$

In order to calculate the oscillating frequency f_o, first the delay of the oscillator stages

t_d is calculated by determining the time at which $v_{out,i}$ equals zero. To simplify the analysis, only the first and the third harmonics are considered. Thus the voltage $v_{out,i}$ can be expressed as

$$v_{out,i} = \frac{I_{osc}}{G_t(f_o)} \frac{1}{\sqrt{1+(\omega_o \frac{C_t(f_o)}{G_t(f_o)})^2}} \sin(\omega_o t - \tan^{-1}(\omega_o \frac{C_t(f_o)}{G_t(f_o)})) + \frac{1}{3} \frac{I_{osc}}{G_t(3f_o)} \frac{1}{\sqrt{1+(3\omega_o \frac{C_t(3f_o)}{G_t(3f_o)})^2}} \sin(3\omega_o t - \tan^{-1}(3\omega_o \frac{C_t(3f_o)}{G_t(3f_o)})). \quad (4.17)$$

As $v_{out,i}$ approaches zero, the term $\sin(\omega_o t - \tan^{-1}(\omega_o \frac{C_t(f_o)}{G_t(f_o)}))$ tends to zero and the term $\sin(3\omega_o t - \tan^{-1}(3\omega_o \frac{C_t(3f_o)}{G_t(3f_o)}))$ approaches 1. Using this approximation, $v_{out,i}$ can be expressed as

$$v_{out,i} \approx \frac{I_{osc}}{G_t(f_o)} \frac{1}{\sqrt{1+(\omega_o \frac{C_t(f_o)}{G_t(f_o)})^2}} (\omega_o t - \tan^{-1}(\omega_o \frac{C_t(f_o)}{G_t(f_o)})) \quad (4.18)$$

$$+ \frac{1}{3} \frac{I_{osc}}{G_t(3f_o)} \frac{1}{\sqrt{1+(3\omega_o \frac{C_t(3f_o)}{G_t(3f_o)})^2}}. \quad (4.19)$$

As $v_{out,i}(t = t_d) = 0$ then

$$\omega_o t_d - \tan^{-1}(\omega_o \frac{C_t(f_o)}{G_t(f_o)}) = \frac{1}{3} \sqrt{\frac{(G_t(f_o))^2 + (\omega_o C_t(f_o))^2}{(G_t(3f_o))^2 + (3\omega_o C_t(3f_o))^2}}. \quad (4.20)$$

Substituting (4.1) in (4.20), and considering that $\omega_o C_t(f_o)/G_t(f_o)$ and $\omega_o C_t(3f_o)/G_t(3f_o)$ are $\gg 1$, then

$$\tan^{-1}\omega_o \frac{C_t(f_o)}{G_t(f_o)}) \approx \frac{\pi}{N} - \frac{C_t(f_o)}{9C_t(3f_o)} \tag{4.21}$$

Thus the frequency can be calculated by

$$f_o = \frac{1}{2\pi}\frac{C_t(f_o)}{G_t(f_o)} tan(\frac{\pi}{N} + \frac{1}{9}\frac{C_t(f_o)}{C_t(3f_o)}) \tag{4.22}$$

It is important to note that (4.22) tends to (4.11) as $C_t(3f_o) \to \infty$ (which means the third harmonic is completely filtered). Equation (4.22) shows that the oscillating frequency is function of $C_t(3f_o)$ and it is not function of $G_t(3f_o)$. The reason is that the impedance at the third harmonic is dominated by the capacitive component of the load.

Fig. 4.2 shows the normalized oscillating frequency of N stage ring oscillator versus the number of stages N obtained by (4.3), (4.11), (4.22), and simulations. Simulations shows that the proposed model in (4.22) predicts the oscillating frequency accurately regardless of the number of stages. However, (4.3) predicts the oscillating frequency accurately for high number of stages only (because the signal becomes closer to a square wave). Equation (4.11) fails to predict the oscillating frequency accurately, although it achieves more accurate and comparable estimation versus (4.3) for ring oscillator with 3 and 4 stages respectively.

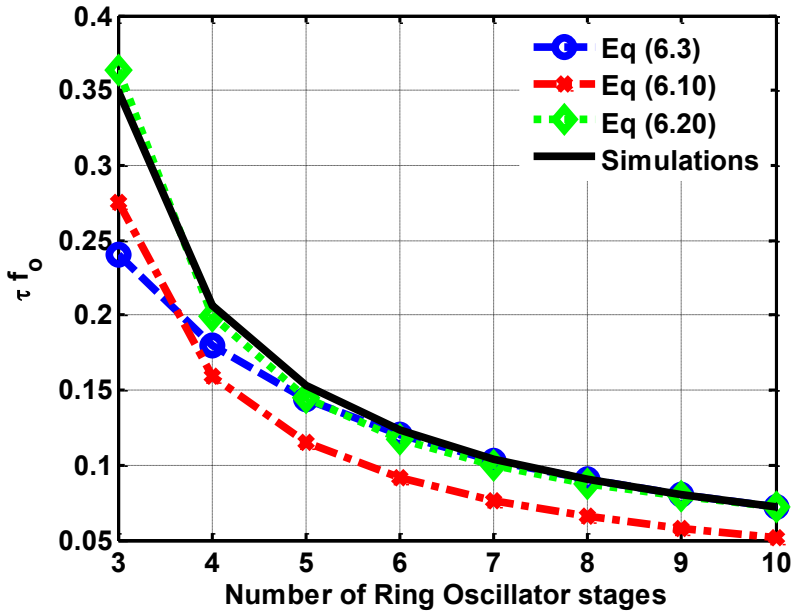


Figure 4.2: Normalized frequency of an N−stage ring oscillator versus the number of stages calculated using Delay, Sine and proposed models and the simulations.

4.3 Proposed Ring-Oscillator PLL-Based System

As discussed in Subsection 2.2, unlike LC oscillators, ring oscillators' frequency is a function of both the delay cell G_t and C_t. Thus, there is the potential to extract both conductance and capacitance variations based on simple frequency shift measurements, provided that these terms can be separated. This subsection first details key characteristics of ring oscillator-based sensors for complex permittivity detection. The proposed PLL-based sensor system is then described.

4.3.1 Complex Permittivity Detection

A novel two-step procedure is proposed to characterize variations in a ring oscillator's sensor capacitance and conductance based on only two frequency shift measurements. In addition to the sensing oscillator (SVCO), the proposed system utilizes

an unexposed, MUT-insensitive reference oscillator and an ALL. Consider first the open-loop case shown in Fig. 4.3, with the sensor load substituted with a dummy capacitor and a PMOS resistor M_p in the reference oscillator (RVCO) delay cell. After MUT application, the first step is ϵ_r' measurement mode, where the ALL is activated to set the reference oscillator amplitude equal to that of the sensor oscillator by adjusting the M_p gate voltage to match the two delay cells' conductance. Using Table 4.1, the frequency shift between the reference and the sensing oscillators with the ALL ON ($\Delta f_{ALL,ON}$) can be calculated by

$$\begin{aligned}\Delta f_{ALL,ON} &= f_{RVCO,ALL,ON} - f_{SVCO} \\ &= \frac{G_t + \Delta G_{MUT}(f_{SVCO})}{C_t} - \frac{G_t + \Delta G_{MUT}(f_{SVCO})}{C_t + \Delta C_{MUT}(f_{SVCO})}.\end{aligned} \tag{4.23}$$

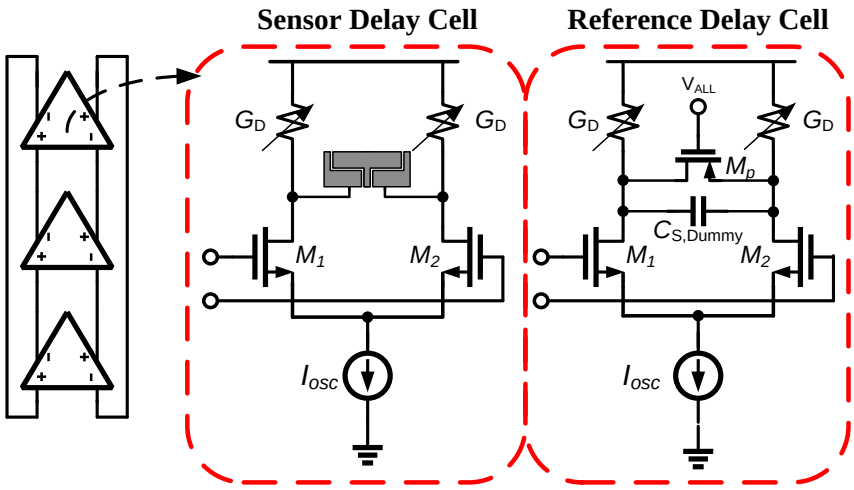


Figure 4.3: 3−stage sensing and reference ring oscillators' delay cells.

Then the normalized $\Delta f_{ALL,ON}/f_{SVCO}$ is calculated by

Table 4.1: Open-loop reference and sensing VCOs oscillation frequency

	Reference VCO Frequency f_{RVCO}	Sensing VCO Frequency f_{SVCO}
Air	$\propto \frac{G}{C}$	$\propto \frac{G}{C}$
MUT-ALL ON	$\propto \frac{G+\Delta G_{MUT}}{C}$	$\propto \frac{G+\Delta G_{MUT}}{C+\Delta C_{MUT}}$
MUT-ALL OFF	$\propto \frac{G}{C}$	

$$\frac{\Delta f_{ALL,ON}}{f_{SVCO}} = \frac{\Delta C_{MUT}(f_{SVCO})}{C_t}, \tag{4.24}$$

which shows that $(\Delta f_{ALL,ON})$ is a function of only $\Delta C_{MUT}(f_{SVCO})$, regardless of MUT loss, and can be used to determine ϵ'_r. In the second step, ϵ''_r measurement mode, while the MUT is still on top of the sensor the ALL is deactivated and the frequency shift $\Delta f_{ALL,OFF}$ can be calculated by

$$\begin{aligned}\Delta f_{ALL,OFF} &= f_{RVCO,ALL,OFF} - f_{SVCO} \\ &= \frac{G_t}{C_t} - \frac{G_t + \Delta G_{MUT}(f_{SVCO})}{C_t + \Delta C_{MUT}(f_{SVCO})}.\end{aligned} \tag{4.25}$$

Then the normalized $\Delta f_{ALL,OFF}/f_{SVCO}$ is calculated by

$$\frac{\Delta f_{ALL,OFF}}{f_{SVCO}} = \frac{\Delta C_{MUT}(f_{SVCO})/C_t - \Delta G_{MUT}(f_{SVCO})/G_t}{1 + \Delta G_{MUT}(f_{SVCO})/G_t}, \tag{4.26}$$

which shows that $\Delta f_{ALL,OFF}$ is a function of both the sensor capacitance $\Delta C_{MUT}(f_{SVCO})$ and conductance $\Delta G_{MUT}(f_{SVCO})$. As $\Delta C_{MUT}(f_{SVCO})$ has been previously determined in ϵ'_r mode, it is possible to isolate $\Delta G_{MUT}(f_{SVCO})$ and de-

termine ϵ_r'' using (9) and (10). In summary, the proposed system only requires two straightforward frequency shift measurements to completely and precisely characterize the MUT complex permittivity.

4.3.2 System Architecture

Placing the sensing VCO inside an integer-N PLL allows precise control of the sensing frequency [28], as shown in the proposed BDS system block diagram (Fig. 4.4). In parallel, the open-loop reference VCO is controlled by an RC-filtered version of the PLL control voltage, $V_{c,filtered}$, to enable cancellation of frequency drift due to temperature variations and correlated low frequency noise [46]. The ALL is realized as two peak detectors connected to the reference and sensing VCOs that feed a high gain opamp controling M_p in the reference VCO. Disabling the ALL is achieved by connecting the gate of M_p to VDD to maximize its resistance.

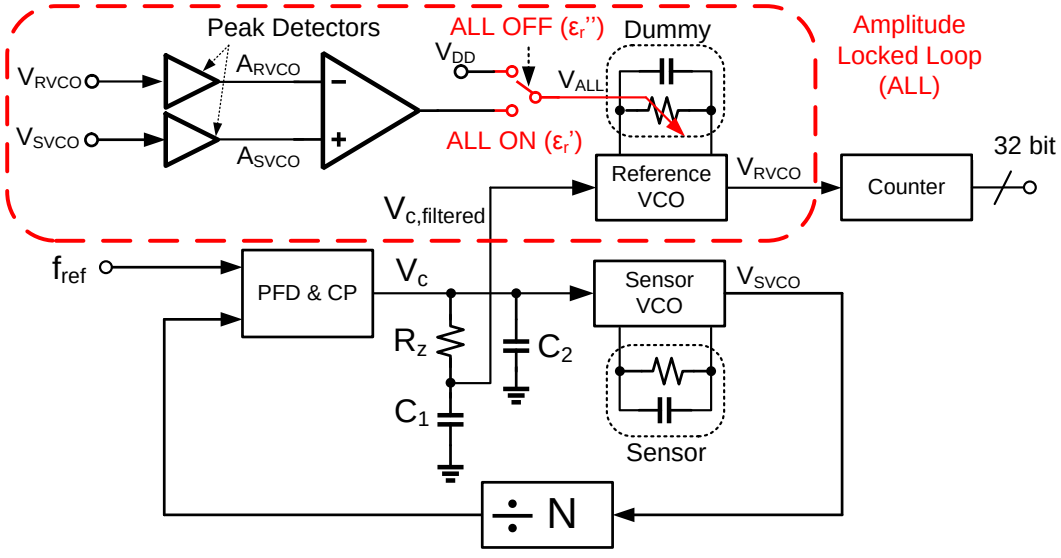


Figure 4.4: Broadband PLL−based complex dielectric spectroscopy system.

The SVCO and RVCO frequency-vs-voltage curves of Fig. 4.5 illustrate the closed-loop system operation. Placing the MUT on top of SVCO shifts its free running frequency down from point i by a value that varies with both MUT ϵ_r' and ϵ_r''. The PLL then maintains an SVCO frequency equal to Nf_{ref} by adjusting the control voltage from $V_{c,Air}$ to $V_{c,MUT}$ (point ii), which adjusts G_D by ΔG_{PLL} to compensate for $\Delta C_{MUT}(f_{SVCO})$ and $\Delta G_{MUT}(f_{SVCO})$. ΔG_{PLL} can be calculated by equating i and ii from table 4.2

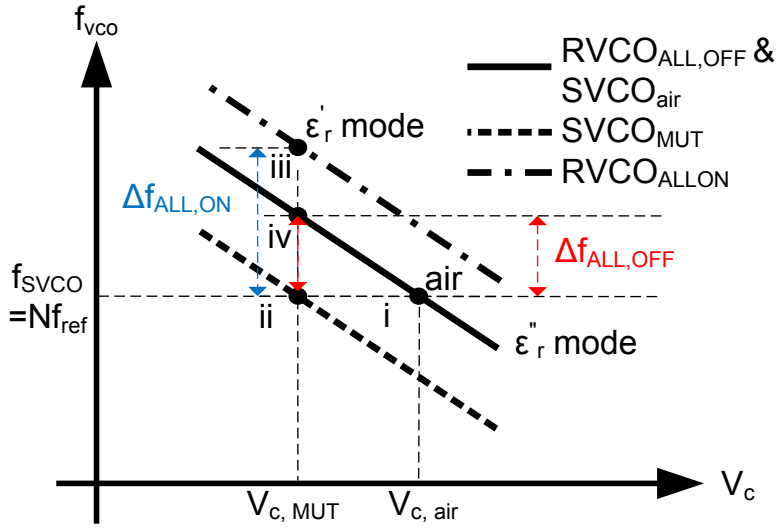


Figure 4.5: Sensor and reference VCO frequency versus control voltage during the MUT characterization procedure.

$$\frac{G_t + \Delta G_{PLL} + \Delta G_{MUT}}{C_t + \Delta C_{MUT}} = \frac{G_t}{C_t}. \tag{4.27}$$

Then G_{PLL}/G_t can be calculated by

Table 4.2: Reference and sensing VCOs oscillation frequency in the closed-loop PLL system

	Reference VCO Frequency f_{RVCO}	Sensing VCO Frequency f_{SVCO}
Air	$\propto \frac{G}{C}$ (i)	$\propto \frac{G}{C} = Nf_{ref}$ (i)
MUT ALL ON ϵ_r' mode	$\propto \frac{G+\Delta G_{PLL}+\Delta G_{MUT}}{C}$ (iii)	$\propto \frac{G+\Delta G_{PLL}+\Delta G_{MUT}}{C+\Delta C_{MUT}} = Nf_{ref}$ (ii)
MUT ALL OFF ϵ_r'' mode	$\propto \frac{G+\Delta G_{PLL}}{C}$ (iv)	

$$\frac{\Delta G_{PLL}}{G_t} = \frac{\Delta C_{MUT}}{C_t} - \frac{\Delta G_{MUT}}{G_t}. \tag{4.28}$$

In ϵ_r' mode, the ALL is enabled to match the RVCO delay cell conductance to that of the SVCO (point iii). $f_{SVCO,ALL,ON}$ can be calculated by substituting i and 4.28 in iii from table 4.2

$$f_{SVCO,ALL,ON} = Nf_{ref} \times (1 + \frac{\Delta C_{MUT}(f_{SVCO})}{C_t}). \tag{4.29}$$

Thus

$$\begin{aligned} \frac{\Delta f_{ALL,ON}}{f_{SVCO}} &= \frac{f_{RVCO,ALL,ON} - Nf_{ref}}{f_{SVCO} = Nf_{ref}} \\ &= \frac{\Delta C_{MUT}(f_{SVCO})}{C_t}. \end{aligned} \tag{4.30}$$

In ϵ_r'' mode, the ALL is disabled and the RVCO frequency returns to its original $V_{c,MUT}$ value (point iv). The normalized frequency shift between the oscillators can be calculated by substituting i and v in iv

$$\frac{\Delta f_{ALL,OFF}}{f_{SVCO}} = \frac{f_{RVCO} - N f_{fref}}{N f_{fref}} = \frac{\Delta C_{MUT}(f_{SVCO})}{C_t} - \frac{\Delta G_{MUT}(f_{SVCO})}{G_t}. \quad (4.31)$$

Note that in comparing the open-loop and closed-loop systems, equations (4.24) and (4.30) remain the same while equations (4.26) and (4.31) are different because the PLL controls the frequency by modifying the delay cells' load conductance. Thus, precise frequency shift measurements allow for computation of $\Delta C_{MUT}(f_{SVCO})$ and $\Delta G_{MUT}(f_{SVCO})$ with (4.30) and (4.31). Given that the sensing oscillator frequency is always $N f_{ref}$, the frequency shifts $\Delta f_{ALL,ON}$ and $\Delta f_{ALL,OFF}$ can be determined by simply measuring the oscillating frequency of the reference VCO. This is achieved using an on-chip 32-bit counter to allow for noise filtering by averaging over a long time interval. This method enables the same frequency detection precision as in [26], while also accurately controlling the sample excitation frequency as in [2], [28].

The PLL uses a 28.5 MHz reference clock and is designed for a damping factor of around 1 and a 0.5 MHz bandwidth. For wide tuning range, 0.5-6 GHz, the integer divider, N, can be varied from 16-248 with a step of 8. This allows for a frequency resolution of 228 MHz. In order to have a fixed PLL bandwidth independent of the divider setting, the charge pump current is varied between 10-160 μA such that the ratio of the charge pump current to the division ratio is constant. This allows for stable system operation and noise performance over the wide tuning range.

4.4 Circuit Implementation

4.4.1 Sensing Element

Fig. 4.6 (a) shows the capacitor sensing element which was built on the 4 μm thick top Aluminum metal layer of the 0.18 μm CMOS process stack. A 9 μm vertical separation is present from the silicon substrate with relative permittivity ϵ'_{si}= 11.9 and DC conductivity $\sigma_{DC,si}$ = 7.4 S/m (Fig. 4.6 (b)). The differential voltage at the ring VCO delay cell output creates a fringing electric field between the capacitor's fingers, which penetrates the liquid sample above to act as the dielectric probe. As the passivation layer would introduce a small equivalent series capacitance between the sensor surface and the liquid sample, a standard passivation cut is made above the sensor to avoid this desensitizing effect.

Controlling sensor parasitic loading is important for robustness of VCO start-up against substrate loss, good sensitivity, and high frequency operation. A commercial electromagnetic (EM) field solver Sonnet[†] is used to carefully select the sensor's finger spacing, width, and length to reduce parasitic series resistance, capacitive loading, and substrate loss. While finger spacing should be chosen small to maximize sensitivity, the metal thickness sets the lower limit on the spacing to avoid the overall sensor capacitance being dominated by the MUT-insensitive sidewall contribution. Thus, the finger spacing was chosen equal to the metal thickness at 4 μm, which is close to the optimum value that maximizes the sensitivity. Setting the trace width involves a compromise with the series metal resistance, which is reduced with wide fingers, and substrate capacitive/loss loading, which is reduced with narrow fingers. The narrowest trace in the sensor layout is chosen to be 30 μm long and 10 μm wide, while the longest trace is 50 μm long and 26 μm wide. Also, the sensor leads are 2

[†]Sonnet Software Inc.: www.sonnetsoftware.com

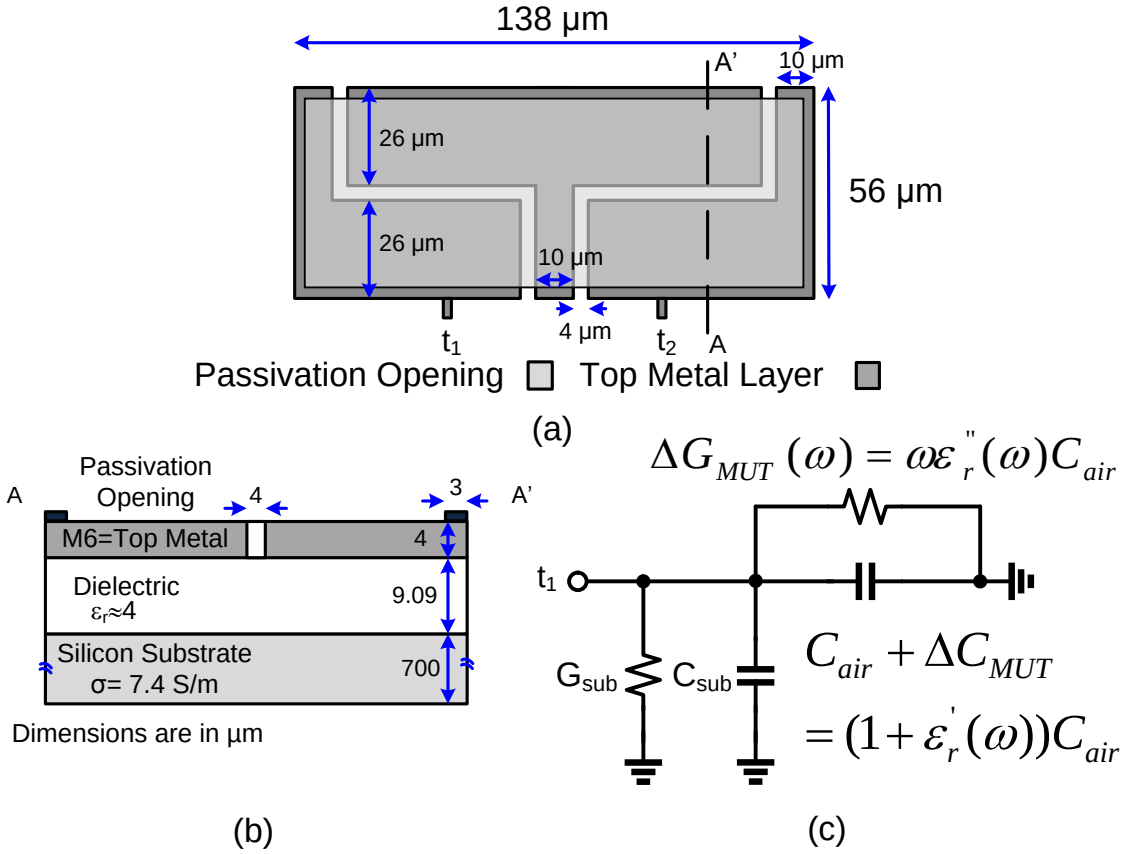


Figure 4.6: Sensing Capacitor: (a) top view, (b) cross section (AA') view of the sensor, and (c) single−ended model.

μm wide to limit their additional shunt capacitance.

EM simulations indicate that the MUT-exposed sensor is very well approximated by the lumped π-model in Fig. 4.6 (c), [2], [28]. Fig. 4.7 (a) shows that the equivalent capacitive admittance is a linear function of ϵ_r' and insensitive to ϵ_r'', with a fixed (air-loaded) capacitance of 15.6 fF and a slope of 1.69 fF/ϵ_r'. Similarly, Fig. 4.7 (b) shows that the equivalent conductance is a linear function of ϵ_r'' and insensitive to ϵ_r', with a fixed (air-loaded) equivalent shunt resistance of 180 kΩ at 1 GHz and 10 kΩ at 6 GHz.

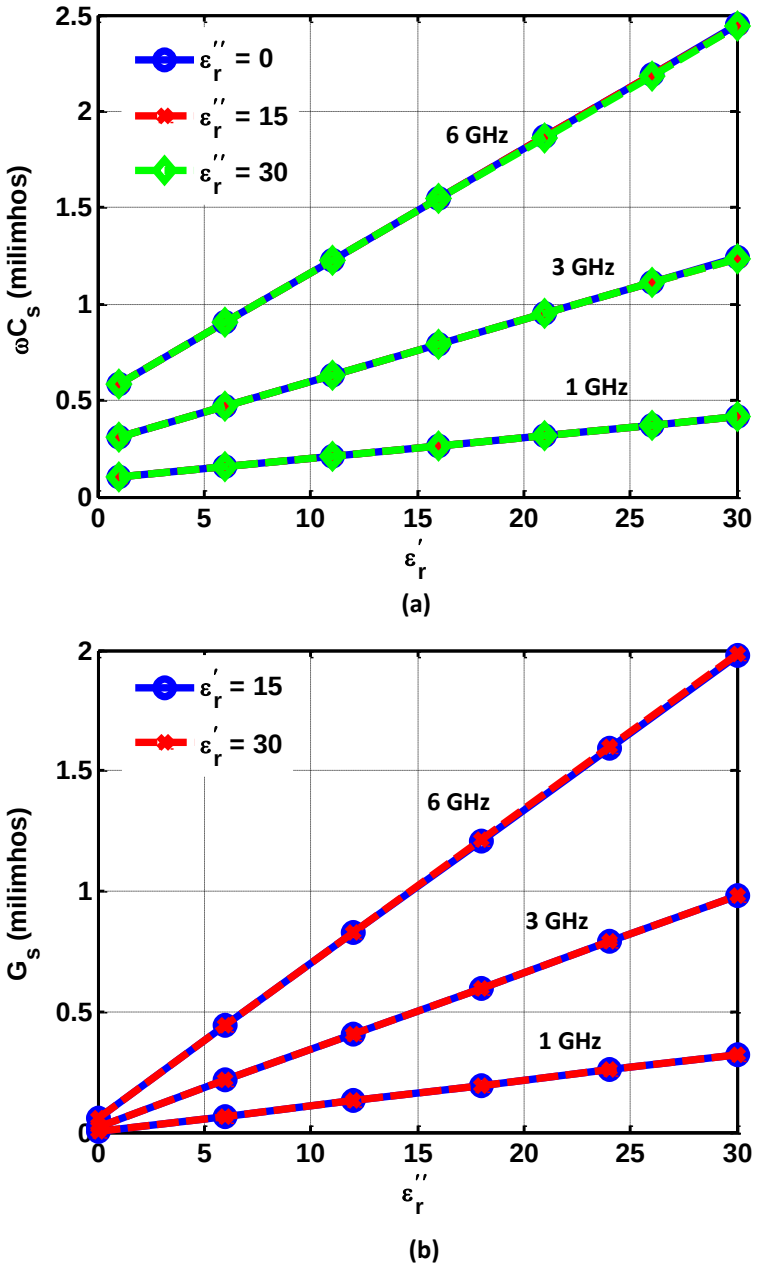


Figure 4.7: Sensing capacitor EM simulations at 1, 3 and 6 GHz: (a) single−ended $\omega\times$capacitance (ωC_s) versus ϵ_r' for different ϵ_r'', and (b) single−ended conductance (G_s) versus ϵ_r'' for different ϵ_r'.

4.4.2 VCO

The sensing and reference oscillators are implemented using a three-stage ring VCO topology with CML delay stages, as shown in Fig. 4.8. Aside from the sensor and the dummy capacitor/M_p load, the two ring oscillators are identical. The three-stage CML topology allows for wide-band operation and low harmonic distortion, with the CML delay cell gain designed higher than 2 to guarantee oscillation for worst-case MUT loss. Frequency tuning is performed by varying G_D, which consists of a 2-bit discrete resistor bank and a PMOS transistor in triode for continuous tuning. Compared to varactor tuning, this method has less parasitic capacitance, wider tuning range, and better K_{vco} linearity. In order to make the oscillation amplitude independent of G_D and the frequency setting, the VCO bias current is set via a common mode feedback circuit which utilizes a replica delay cell and an external reference voltage V_{ref} to force $I_{osc}/(2G_D) = V_{DD} - V_{ref}$ [36]. It is important to note that while the amplitudes of the sensing and the reference oscillators are independent of G_D, they are still functions of the sensor loss and the M_p resistance respectively, as the replica delay cell is MUT-insensitive and also doesn't contain M_p.

Post-layout simulations show that the oscillator tuning range is 0.5−6.3 GHz and the gain (K_{VCO}) varies between $\sim$ 2.8−3.2 GHz/V as a function of the resistor bank setting. Wider tuning range and lower frequencies can be achieved by adding larger resistors to the resistor bank and optimizing the biasing circuitry. At 6 GHz oscillation, the phase noise is -79 dBc/Hz at 1MHz and -101 dBc/Hz at 10 MHz. Including biasing, the two oscillators consume 6.2−77.4 mW from the 1.8 V supply while operating between 0.5−6.3 GHz.

As discussed in Subection 4.1, the oscillating frequency of ring oscillators is function of the load capacitance and conductance of the delay cells at the oscillating

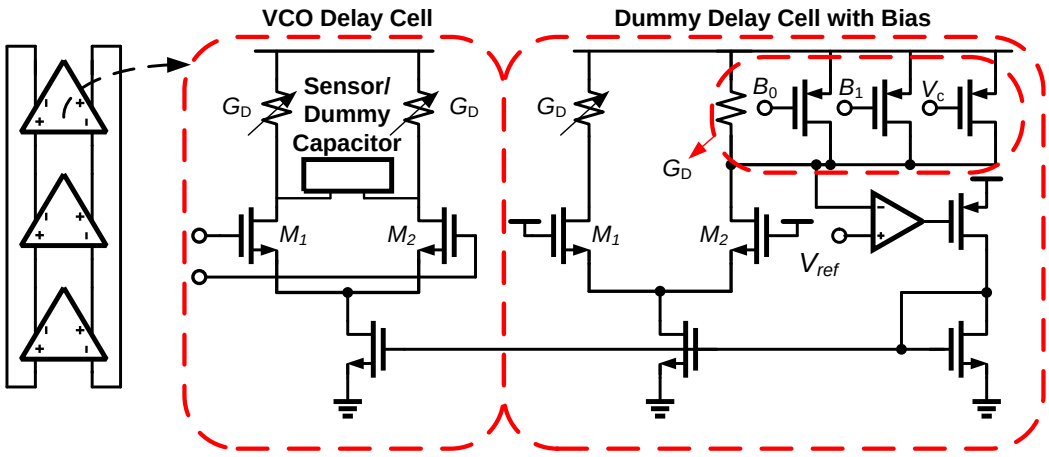


Figure 4.8: VCO replica biasing scheme.

frequency and its harmonics. This may cause an error in the permittivity characterization versus frequency which is function of the ratio between the total capacitance of the delay cell at the fundamental frequency to the total capacitance at the third harmonic $(C_t(f_o)/C_t(3f_o))$ which can be expressed as

$$\begin{aligned}\frac{C_t(f_o)}{C_t(3f_o)} &= \frac{1+\Delta C(f_o)/C_t}{1+\Delta C(3f_o)/C_t} \\ &\approx 1+\frac{\Delta C(f_o)}{C_t}-\frac{\Delta C(3f_o)}{C_t} \\ &= 1+\frac{\Delta C(f_o)-\Delta C(3f_o)}{C_t} \\ &= 1+\frac{(\epsilon_r'(f_o)-\epsilon_r'(3f_o))\epsilon_o C_{air}}{C_t}. \end{aligned} \tag{4.32}$$

In this design the sensor capacitance is less than 5% of the total load capacitance of the delay cells which result in less than 1.5 % error in the frequency shift due to the third harmonic component of the sensor capacitance for difference between the MUT permittivity at the fundamental frequency and at the third harmonic component

$(\epsilon'_r(f_o) - \epsilon'_r(3f_o))$ of around 10.

4.4.3 Amplitude Locked Loop

A block diagram of the ALL, where the amplitude difference between the reference and sensing VCOs is monitored by two peak detectors and amplified by a two stage opamp to control M_p in the reference VCO, is shown in Fig. 4.9. Here the peak detector is modeled by a gain K_{PD}, representing the variation of the PD output voltage versus the amplitude of the input signal, and the reference VCO is modeled by a gain $K_{VCO,ALL,A}$, representing the reference oscillator output amplitude versus the M_p gate voltage. Using Fig. 4.9 and assuming that the opamp has a gain of A_{opamp} and an offset of $V_{All,offset}$, the amplitude of the reference oscillator can be calculated by

$$\begin{aligned} A_{VCO,ref} &= \frac{A_{ALL}}{A_{ALL}+1}(A_{VCO,sens} + V_{ALL,offset}), \\ &= A_{VCO,sens}\frac{A_{ALL}}{A_{ALL}+1}(1 + \frac{V_{ALL,offset}}{A_{VCO,sens}}), \end{aligned} \tag{4.33}$$

where $A_{ALL} = A_{opamp}K_{VCO,ALL,A}K_{PD}$. Substituting (2.6) in (4.33)

$$K_{PD}\frac{I_{osc}}{G_{VCO,ref}} = K_{PD}\frac{I_{osc}}{G_{VCO,ref}}\frac{A_{ALL}}{A_{ALL}+1}(1 + \frac{V_{ALL,offset}}{A_{VCO,sens}}). \tag{4.34}$$

Thus $G_{VCO,ref}$ can be calculated by

$$G_{VCO,ref} = G_{VCO,sens}\frac{\frac{1+A_{ALL}}{A_{ALL}}}{1 + \frac{V_{ALL,offset}}{A_{VCO,sens}}}. \tag{4.35}$$

Equation (4.35) shows that the ALL offset and open loop gain can cause mismatch

between the load conductances of the sensing and the reference oscillators which will result in an error in the permittivity detection. In order to minimize this error, the opamp gain should be maximized and its offset relative to the oscillator amplitude should be minimized. So, a two-stage opamp is utilized that have 63 dB DC gain and 9.5 kH 3dB bandwidth, which yields an ALL open loop gain (A_{ALL}) of 38 dB, and less than 10 mV offset $V_{ALL,offset}$. The closed loop bandwidth of the ALL is ∼700 kHz. System stability over PVT variations is ensured by designing the loop to have ∼90° phase margin.

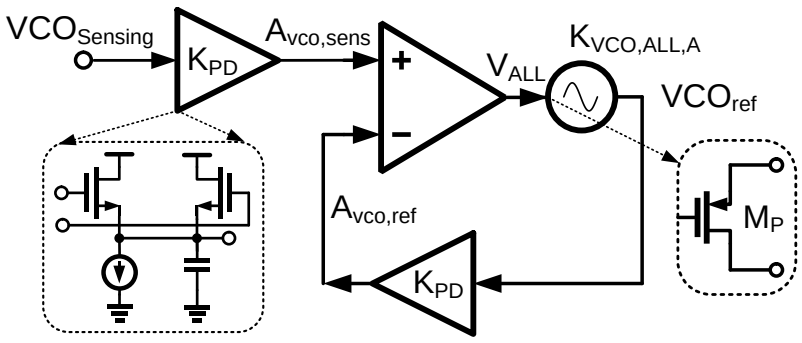


Figure 4.9: ALL block diagram.

4.4.4 Frequency Divider

Fig. 4.10 shows the programmable frequency divider block diagram. In order to robustly divide the high-speed VCO output, a CML topology is used in an initial divide-by-8 block. The subsequent divider stages are implemented in static CMOS to save power, with a differential CML-to-CMOS converter [34] following to convert the divide-by-8 CML logic levels to the rail-to-rail swing needed to drive CMOS dual modulus 2/3 dividers [35]. Five dual modulus divider cells are fed to a 5:1 multiplexer

to allow a division ratio ranging from 2 to 31 in steps of unity, resulting in an overall divider ratio N ranging from 16 to 248 in steps of 8.

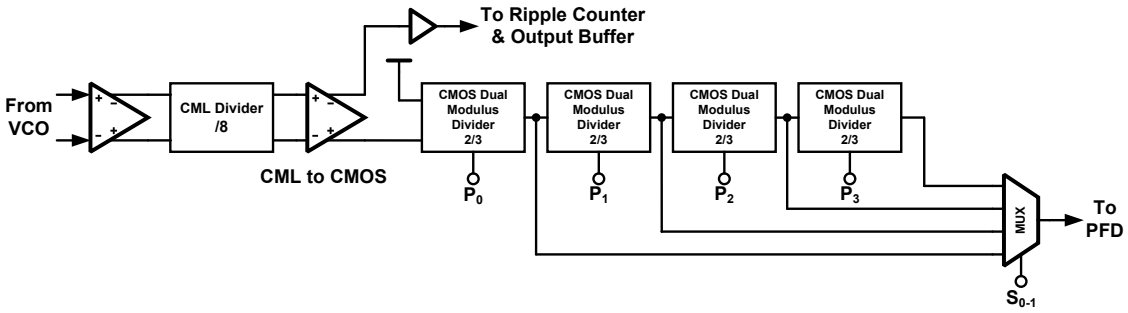


Figure 4.10: Frequency divider block diagram.

4.4.5 Phase Frequency Detector and Charge Pump

The phase-frequency detector (PFD) compares the divider output with the 28.5 MHz reference frequency to generate the charge pump control signals. A classic tri-state PFD topology, described in Section 3.4.3 [36], is implemented because of the relatively low 28.5 MHz reference frequency for the 180 nm CMOS technology. This allows a robust operation and low power consumption. Dummy pass-gates are utilized to match the delay of the up and down signals and their complementaries. Four inverters are employed in the feedback reset path to eliminate the PFD dead-zone.

As a fixed reference frequency is used to synthesize a wide frequency range, programmability is implemented in the charge pump to ensure a constant charge pump current to division ratio and keep the bandwidth and damping factor stable over wideband operation. Shown in Fig. 4.11, the charge pump utilizes 4-b DACs for the up and down current sources to allow for a programmable output between 10-

160μA. Emphasis is placed on reducing disturbances on the VCO control voltage due to charge sharing and mismatches between the up and down currents. In order to reduce charge sharing, a differential topology is implemented which steers current onto a dummy path regulated by Opamp1 to keep the current sources' drain nodes relatively constant over operating frequency [36]. The up and down currents of the charge pump are matched by regulating the down current to match the up transistor current using Opamp2 and the replica bias path consisting of M_{p2}, M_{p3}, M_{n3} and M_{n2}. Controlling the down current, rather than the up current, is chosen due to the higher PMOS output resistance in the 0.18 μm CMOS technology. This minimizes the variation of the charge pump current versus the control voltage, allowing for reduced fluctuations in the PLL bandwidth and damping factor.

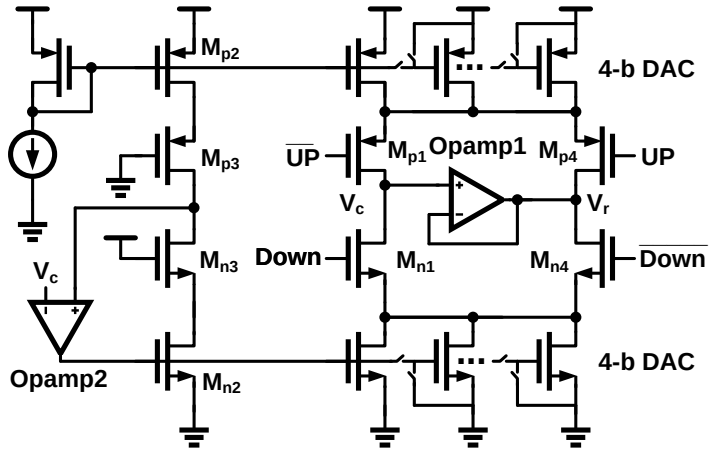


Figure 4.11: Charge pump.

4.4.6 Counter

The counter (which is used to measure the oscillating frequency of the reference VCO) is implemented as a CML divide-by-8 stage followed by a CML-to-CMOS block and a 32-bit asynchronous ripple counter as shown in Fig. 4.12. The maximum frequency after the divide-by-8 stage is less than 1 GHz which enables implementing the asynchronous counter using static CMOS gates to achieve low power and robust operation. The ripple counter accumulates the edges of the reference VCO over a relatively long time interval, that can be adjusted externally by controlling the counter enable input pulse width. The reference VCO frequency is estimated as the ratio of the accumulated digital counter word N_{count} to the enable pulse width

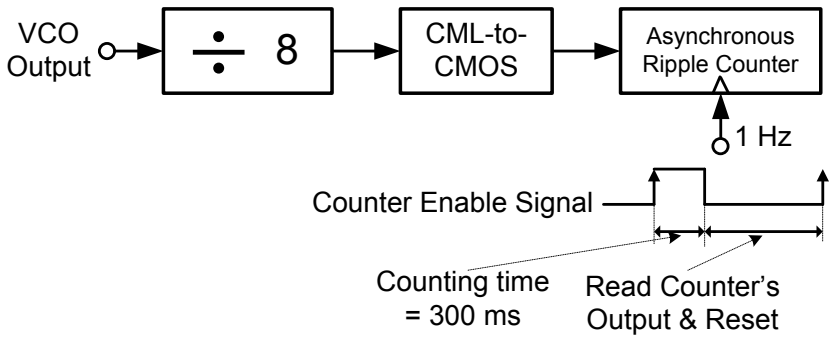


Figure 4.12: Counter block diagram.

$$f_{ref} = 8\frac{N_{count}}{\Delta T_{en}}. \tag{4.36}$$

Assuming the counter does not saturate, the quantization noise of the counter is bounded by $\pm 1/\Delta T_{en}$, where ΔT_{en} is the counting time. Thus, a 32-b counter is utilized for a very long counting interval (>5 s at the maximum frequency) before

potential saturation. This results in a small quantization error (<0.1 ppm for ΔT_{en} > 0.1 s). The large ΔT_{en} enabled by the 32-b counter also offers improved jitter rejection, as it results in a lower corner frequency for the effective lowpass filtering of high-frequency reference VCO jitter [26].

Using an asynchronous ripple counter requires its ripple delay to be accommodated between successive counting intervals, i.e. a sufficiently long dead time is introduced before each counter word is read. Thus, in this work the counter enable is clocked by a 1 Hz clock with 30% duty cycle to achieve 300 ms counting time, and allows for 700 ms to read the counter's output Fig. 4.12.

4.4.7 System Sensitivity

Total system noise is set by: i) the counter quantization noise, and ii) the noise of the reference VCO and the PLL and ALL circuitry. In this subsection, each of these sources are discussed and their effect on the overall noise of the counter's output, $\sigma_{\Delta f/f_o}$, is estimated.

As discussed before, the quantization noise of the counter is bounded by $\pm 1/\Delta T_{en}$, where ΔT_{en} is the counting time (assuming the counter does not saturate). A 32-b counter enables a very long counting interval and negligible quantization noise. Now the noise due to the rest of the system blocks is examined. As discussed in [26], [47] the standard deviation in the oscillator frequency at the counter's output $\sigma_{\Delta f/f_o}$ can be determined using the oscillator phase noise S_ϕ by

$$\sigma_{\Delta f/f_o} = \frac{8}{(2\pi f_o \Delta T_{en})^2} \int_0^\infty S_\phi \sin^2(\pi \Delta T_{en}) df. \tag{4.37}$$

Given that the oscillator phase noise is $S_\phi = (N_1 f_c)/f^3 + N_1/f^2$, where N_1 is frequency domain white noise figure of merit and f_c is the corner frequency, then (13) can be calculated (as discussed in [47]) by

$$\sigma_{\Delta f/f_o} = \frac{5\sqrt{N_1 f_c}}{f_o}. \tag{4.38}$$

Thus, the reference oscillator phase noise should be determined, and then $\sigma_{\Delta f/f_o}$ can be calculated using (14).

This RVCO phase noise is a function of i) the reference VCO open-loop phase noise, ii) the PLL noise, and iii) the ALL noise when ON. In analyzing the PLL contribution, the noise sources' closed-loop transfer function to the VCO control voltage are determined and then integrated by the RVCO (K_{RVCO}/s) to determine the phase noise impact. As noise from the input reference clock, charge pump, and output-referred SVCO phase noise are all bandpass filtered by the loop at the control voltage, the net result is that the system low-pass filters all these components at the RVCO output. Although, in order to not over-estimate the two VCOs' noise contribution, correlated noise sources (temperature, common bias circuitry, and supply) should be also considered, as the PLL will cancel correlated low-frequency noise. When the ALL is OFF, simulations show that the uncorrelated VCO noise dominates the output phase noise response and the estimated $\sigma_{\Delta f/f_o}$ is $\sim$ 83ppm ($\sim$ 0.008%). However, the ALL also impacts system noise through the Mp control in the RVCO load, which affects both the oscillator amplitude and frequency. This is mapped to the RVCO phase noise by multiplying the ALL voltage noise at the VCO input, $V_{ALL,rms}$, by the M_p gate voltage to phase noise transfer function, which is equal to $K_{VCO,ALL,f}/s$, where $K_{VCO,ALL,f}$ is the VCO gain seen at the gate of M_p. In the current system the ALL is the dominant noise contributor when activated, with the estimated $\sigma_{\Delta f/f_o}$ increasing to $\sim$ 965ppm ($\sim$ 0.1%).

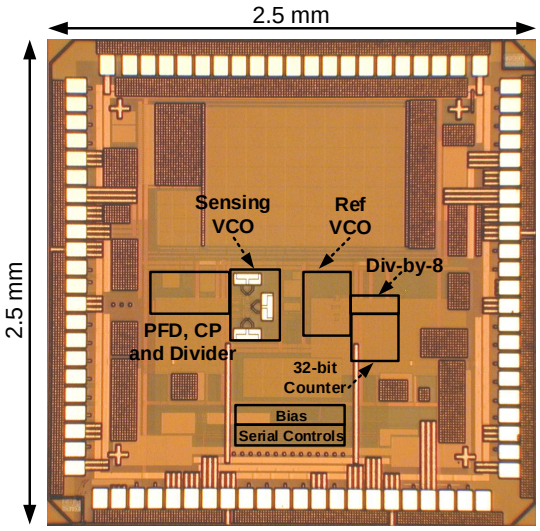
It is important to highlight that the system noise increase with the ALL ON is due to the opamp noise and the large $K_{VCO,ALL,f}$. One potential technique to reduce this ALL noise is to use a low noise opamp with chopping to reduce the

flicker noise. Another possibility is to reduce $K_{VCO,ALL,f}$, which is a function of the M_p size necessary to match the maximum MUT loss. This can be achieved with a dual loop ALL consisting of a digital loop that coarsely controls a parallel resistor bank and an analog loop that finely sets M_p conductance with low effective $K_{VCO,ALL,f}$.

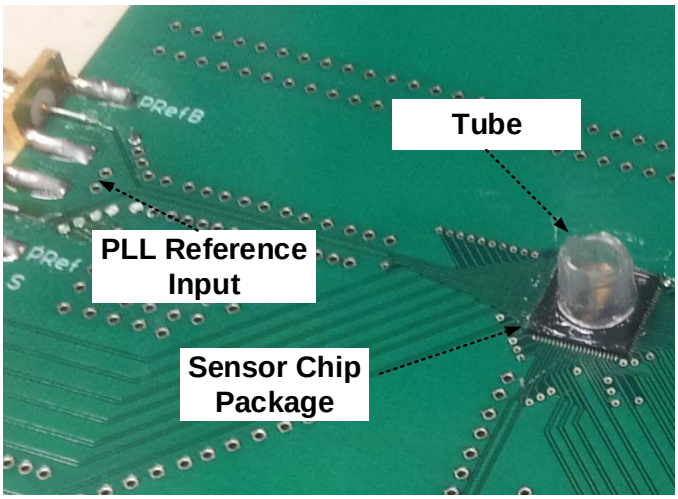
4.5 System Integration and Test Setup

Fig. 4.13 shows the BDS system chip micrograph, which is fabricated in a 0.18 μm CMOS process. The three sensing capacitors were laid out such that the fringing electric field components of each two adjacent sensors are perpendicular, which minimizes parasitic coupling between the adjacent stage outputs of the ring VCO through the potentially high-permittivity liquid sample region above. The oscillator area is 0.0035 mm^2 and 0.069 mm^2 without and with the sensing capacitors, respectively. Total chip area is 6.25 mm^2 and total system power consumption is 69-140 mW from a 1.8V supply. Utilizing a 28.5 MHz reference frequency, the PLL operates between 0.7-6 GHz for MUTs with ϵ_r' in the range between 1 and 30 and ϵ_r'' in the range between 0 and 30, corresponding to organic chemical values. Operation up to 4.788 GHz for pure water-based measurements and up to 5.016 GHz for phosphate buffered saline (PBS)-based measurements is achieved.

An open-cavity micro lead frame (MLP) 10×10 mm QFN 88 package is used for chip assembly to allow for MUT deposition on top of the sensing capacitors (Fig. 4.13 (b)). All electrical connections between the chip and the package lead frame are made via wire-bonds which are covered by epoxy to protect them from the MUT. The MUTs, including methanol, ethanol, pure water, and PBS are applied via a Finnpipette single-channel micropipette into a plastic tube fixed on top of the chip. Exceeding the sensor saturation height for reliable measurements only requires



(a)



(b)

Figure 4.13: (a) Micrograph of the PLL−based complex dielectric spectroscopy chip. (b) PCB with the packaged chip and MUT-application tube.

MUT volumes less than 20 μL [2], [23]. The tube is capped to avoid evaporation [28], which is particularly important in the characterization of mixtures with different evaporation rates.

4.6 Experimental Results

4.6.1 PLL and Sensitivity Characterization

As shown in Fig. 4.14, the 2-b VCO load resistor control allows PLL operation between 0.68−6.15 GHz with the VCO gain varying between 2.9−3.3 GHz/V and the phase noise maintained below -75 dBc/Hz at a 1 MHz offset. For these fixed 1 MHz and 10 MHz measurements beyond the PLL loop bandwidth, the open-loop VCO phase noise dominates and is higher at the maximum frequency setting. The PLL output spectrum, measured at the divide-by-8 output, is shown in Fig. 4.15 for the maximum 6.15 GHz operation. Utilizing the aforementioned charge pump design techniques allows suppression of the 28.5 MHz spurs to below -52 dBc.

In order to characterize system sensitivity, the VCO open loop phase noise is estimated by measuring the phase noise at the divide-by-8 output with the maximum 6.15 GHz operation and the minimum PLL bandwidth setting, as shown in Fig. 4.16. The estimated VCO flicker noise corner frequency is 2.5 MHz. System noise is characterized by the standard deviation of the counter-measured reference oscillator's without any MUT applied. Fig. 4.17(a) shows the $\sigma_{\Delta f/f_o}$ versus counting time with the ALL OFF and ON, along with the estimated quantization noise, for the PLL operating at 6.15 GHz. As the quantization noise is small, the measured noise is relatively constant for counter times greater than 100 ms and dominated by the VCO and ALL noise with the ALL OFF and ON, respectively. Fig. 4.17(b) shows the $\sigma_{\Delta f/f_o}$ is also relatively constant over the PLL operating frequency at $< 0.02\%$ and $< 0.12\%$ with the ALL OFF and ON, respectively, which is similar to the simulated values mentioned in Subsection 4.4.7. A similar maximum system noise of $< 0.12\%$ is measured with MUT applied. This frequency noise can be converted to permittivity noise using calibrated system equations discussed in Subsection 4.6.2, which results

in a 0.2-3.5% change in permittivity.

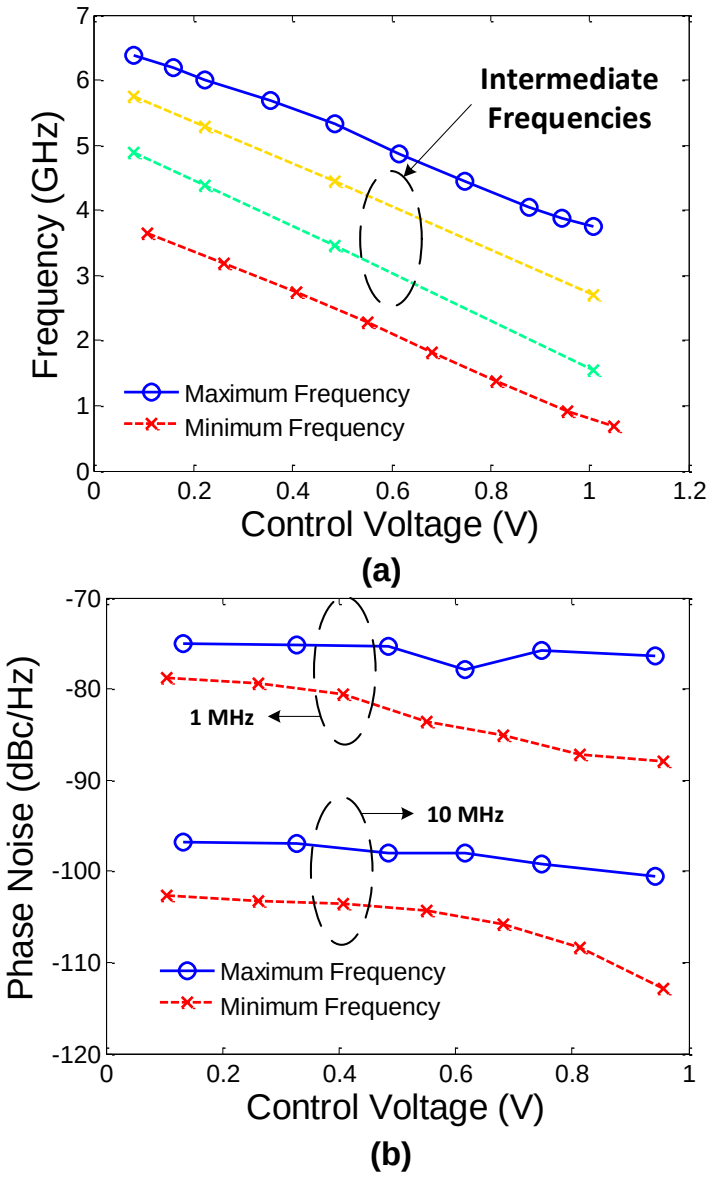


Figure 4.14: PLL measurements versus the control voltage at the maximum and the minimum frequency setting. (a) VCO frequency. (b) Phase noise at 1 MHz and 10 MHz offsets.

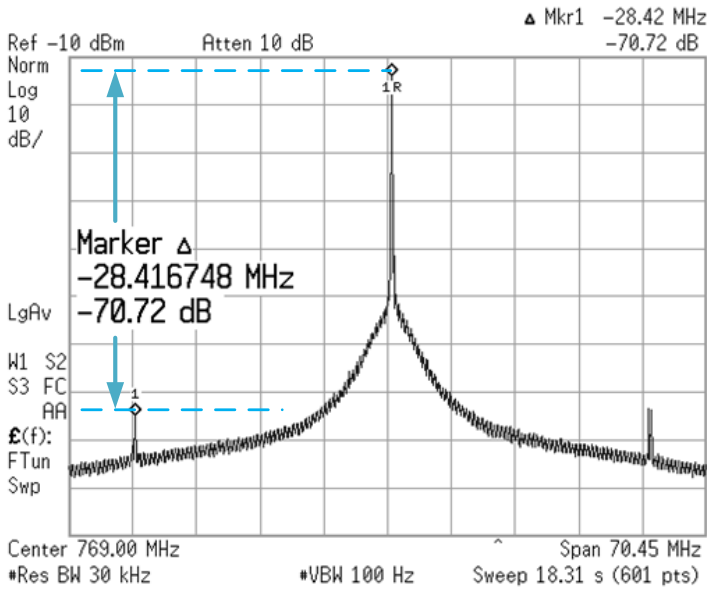


Figure 4.15: PLL output spectrum after CML divide−by−8 divider.

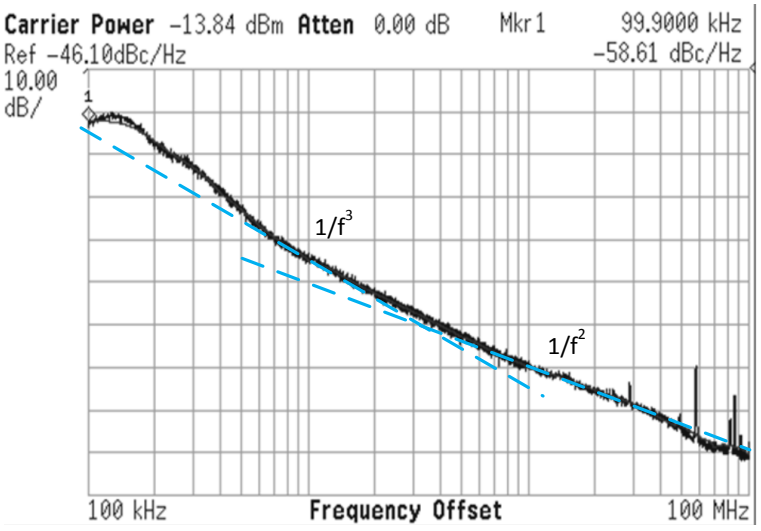


Figure 4.16: VCO output phase noise after CML divide−by−8 divider.

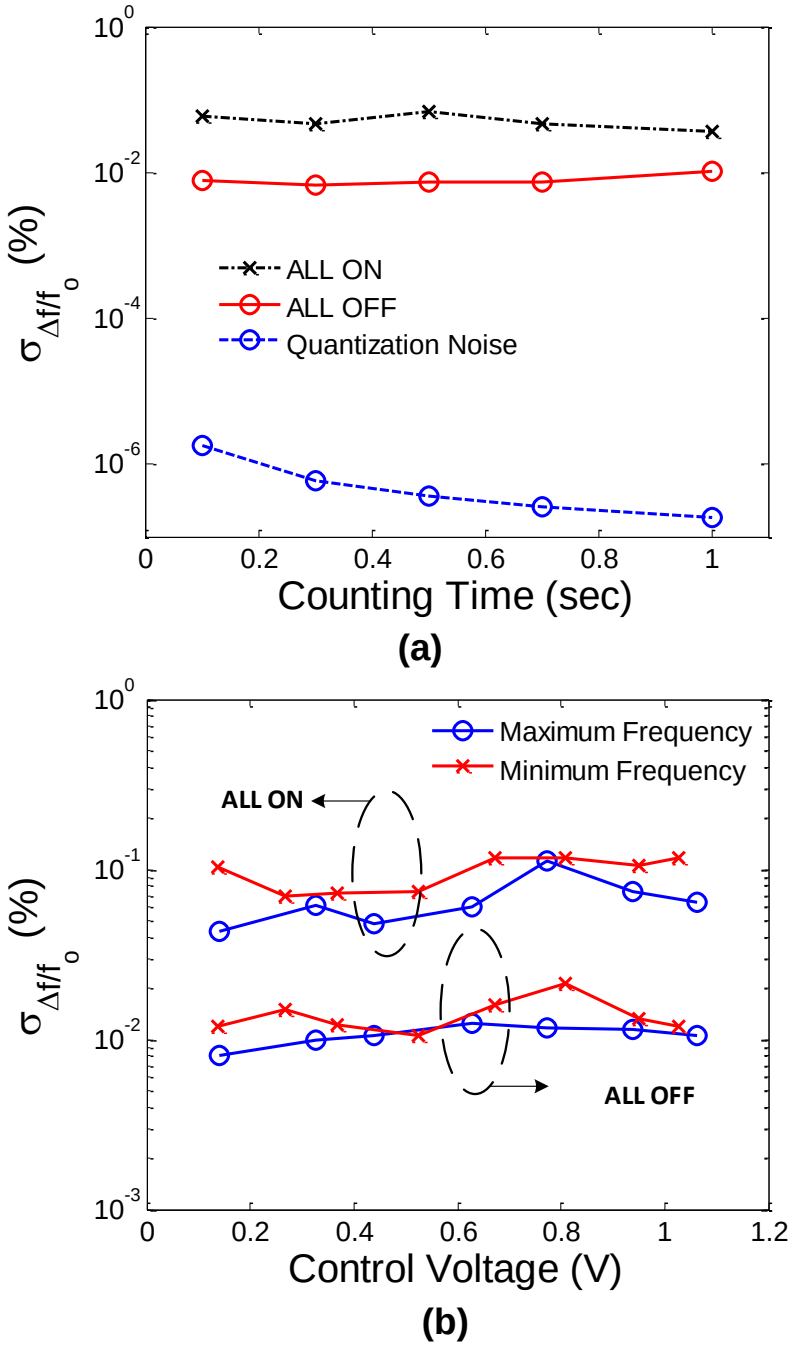


Figure 4.17: System noise measurements at 6.15 GHz versus (a) counting time and (b) control voltage with 300 ms counting time.

4.6.2 Chemical Measurements

Dielectric Frequency Dispersion and Mixture Theories

The theoretical value of the frequency dependent complex permittivity of pure MUTs is defined by the Cole-Cole model [24].

$$\varepsilon(\omega) = \varepsilon'(\omega) - j\varepsilon''(\omega) = \varepsilon_{r,\infty} + \frac{\varepsilon_{r,0} - \varepsilon_{r,\infty}}{1 + (j\omega\tau)^{1-\alpha}}, \tag{4.39}$$

where $\varepsilon_{r,0}$ is the static permittivity at DC, $\varepsilon_{r,\infty}$ is the permittivity at ∞, τ is the characteristic relaxation time, and α is the relaxation time distribution parameter. In this work, theoretical values at a temperature of 27° are considered [25]. Note that in the reported results, as there is no dedicated temperature control over the sample, temperature variation is one of the measurement error sources.

For Binary mixtures, the complex permittivity is defined by [40]- [41]

$$\frac{\varepsilon_{eff} - \varepsilon_e}{\varepsilon_{eff} + 2\varepsilon_e + \nu(\varepsilon_{eff} - \varepsilon_e)} = q\frac{\varepsilon_i - \varepsilon_e}{\varepsilon_i + 2\varepsilon_e + \nu(\varepsilon_{eff} - \varepsilon_e)}, \tag{4.40}$$

where ε_{eff} is the effective mixture permittivity, ε_e is the permittivity of the environment, ε_i is the inclusion permittivity, q is the fractional volume ratio, and ν is a parameter to define the employed model. ν has values of 0, 2, and 3 corresponding to Maxwell-Garnett, Polder-van Santen, and quasi-crystalline approximation rules, respectively. The Polder-van Santen model is used to determine the complex permittivity of ethanol and methanol [2], [28]. While for water-based mixtures, the Polder-van Santen model is used to determine the DC permittivity of the mixture $\varepsilon_{r,eff,0}$ and the high frequency permittivity $\varepsilon_{r,eff,\infty}$ is calculated by [48]

$$\Delta\varepsilon_{eff} = q\Delta\varepsilon_i + (1-q)\Delta\varepsilon_e, \tag{4.41}$$

where $\Delta\varepsilon_{eff} = \varepsilon_{eff,0} - \varepsilon_{eff,\infty}$, $\Delta\varepsilon_i = \varepsilon_{i,0} - \varepsilon_{i,\infty}$, and $\Delta\varepsilon_e = \varepsilon_{e,0} - \varepsilon_{e,\infty}$. The characteristic relaxation time of the mixture τ_{eff} is calculated by [48]

$$log(\tau_{eff}) = qlog(\tau_i) + (1-q)log(\tau_e), \tag{4.42}$$

where τ_e and τ_i are the characteristic relaxation time of the environment and the inclusion MUTs, respectively. The Cole-Cole model (4.39) is then used to calculate the frequency dependent permittivity of the mixture based on the calculated values of $\varepsilon_{eff,0}$, $\varepsilon_{eff,\infty}$, and τ_{eff}.

For PBS, the real part of the permittivity is the same as that of the DI-water. However, the imaginary part is determined by $\varepsilon''_{r,PBS} = \varepsilon''_{r,water} + \sigma_{PBS}/(\omega\varepsilon_o)$, where σ_{PBS} is the conductivity of the medium [49]. In this work σ_{PBS} of 1.4 S/m is used for a 1X PBS solution [50].

Mixture Characterization and Permittivity Detection

System performance over a 0.7−6 range is first evaluated by exposing the sensor to several binary mixtures of ethanol and methanol with mixing ratios of methanol q = {0, 20, 50, 80, 100}%. After MUT deposition, two frequency shift measurements are obtained: first with the ALL ON, and then with the ALL OFF. For all the reported results a 300 ms counting time is used with the counter clocked as shown in Fig. 4.4. With the same MUT in place, each measurement is repeated 10 times and averaged. From (11) and (12), the relative frequency shifts $\Delta f_{ALL,ON}/Nf_{ref}$ and $(\Delta f_{ALL,ON} - \Delta f_{ALL,OFF})/Nf_{ref}$ are functions of $\Delta C_{MUT}(\omega)/C$ and $\Delta G_{MUT}(\omega)/G$ respectively, and can be used to extract ϵ'_r and ϵ''_r. As described in [2], [28], system calibration is performed with a quadratic equation to fit $\Delta f_{ALL,ON}/Nf_{ref}$ and $(\Delta f_{ALL,ON} - \Delta f_{ALL,OFF})/Nf_{ref}$ as a function of reported ϵ'_r and ϵ''_r of three reference mixtures (q = {0, 50, 100}%) [25]- [41]. For mixtures with q = {20, 80}, ϵ'_r and ϵ''_r are determined

by substituting frequency shift measurements in the calibrated equations, with the measured and reported values of ϵ_r' and ϵ_r'' shown in Fig. 4.18. The resulting maximum error between the measured and theoretical values over the entire frequency range is less than 3.7% for both ϵ_r' and ϵ_r''.

System performance over mixing ratio is verified using more binary mixtures of ethanol and methanol with mixing ratios of methanol (q) between 0 and 100% for several frequencies. Fig. 4.19 shows measured and theoretical ϵ_r' and ϵ_r'' versus mixing ratio, q, with the measurements following the theoretical values with a maximum error of 3.5%.

In order to demonstrate the system potential for biomedical applications, where biosamples are usually contained within water or PBS solutions, two experiments are conducted. The first experiment utilizes several binary mixtures of de-ionized (DI) water and methanol with mixing ratios of methanol (q) between 0 and 100%. Theoretical permittivity of water-methanol mixture is calculated as described in [48]. Due to the non-monotonic behavior of ϵ_r'' versus q, four materials are utilized for calibration: $q = \{0, 20, 80, 100\}$% at low frequencies and $q = \{0, 20, 60, 100\}$% at high frequencies. Fig. 4.20 shows for mixtures with $q = 50$, measured and theoretical ϵ_r' and ϵ_r'' versus frequency, with a maximum 3% error. Here the frequency range of 0.7-4.77 GHz is lower than the previous ethanol−methanol mixtures due to the higher DI water ϵ_r'. Note that in order to calibrate the frequency shift measurements over the entire frequency range, the maximum frequency is limited by the maximum VCO/PLL operating frequency with water (highest permittivity) and the minimum frequency is limited by the minimum VCO/PLL operating frequency with Air (lowest permittivity). Fig. 4.21 shows measured and theoretical ϵ_r' and ϵ_r'' versus mixing ratio, q, with the measurements following the theoretical values with a maximum 5.4% error.

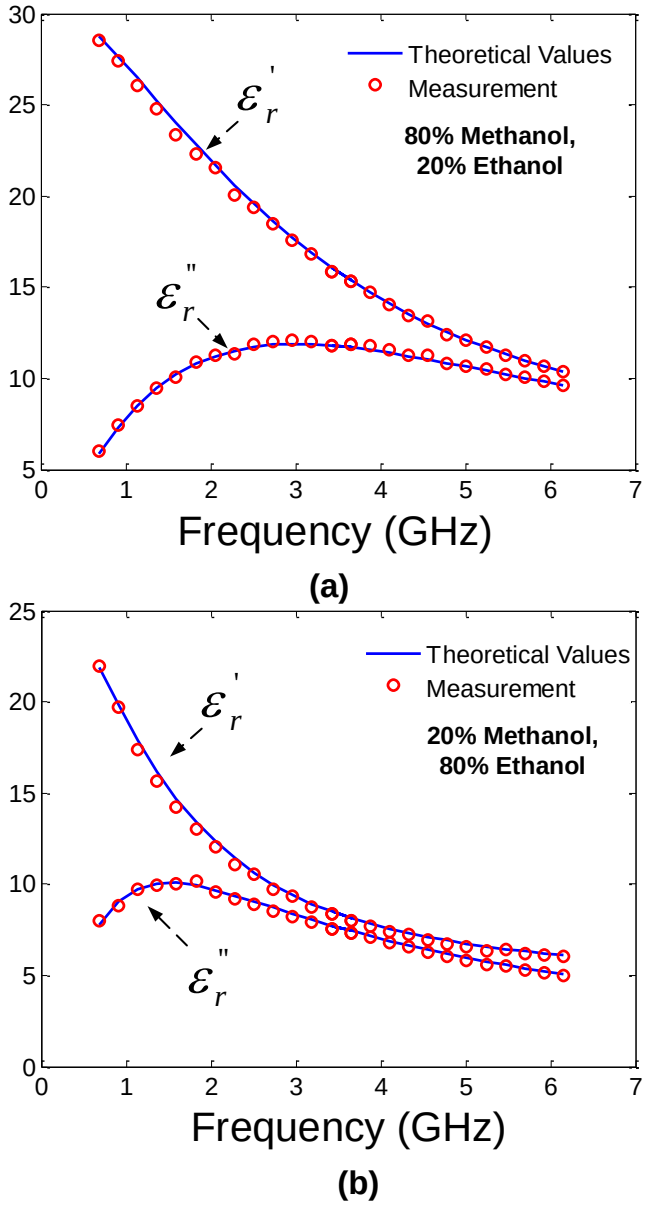


Figure 4.18: Measured and theoretical ϵ_r' and ϵ_r'' of ethanol-methanol mixtures versus frequency for: (a) 80% methanol and 20% ethanol, and (b) 20% methanol and 80% ethanol mixtures.

In the second experiment, the effect of varying the sample DC conductivity on its ϵ_r'' was investigated by adding 1X PBS (Gibco 10010) to DI water to vary the

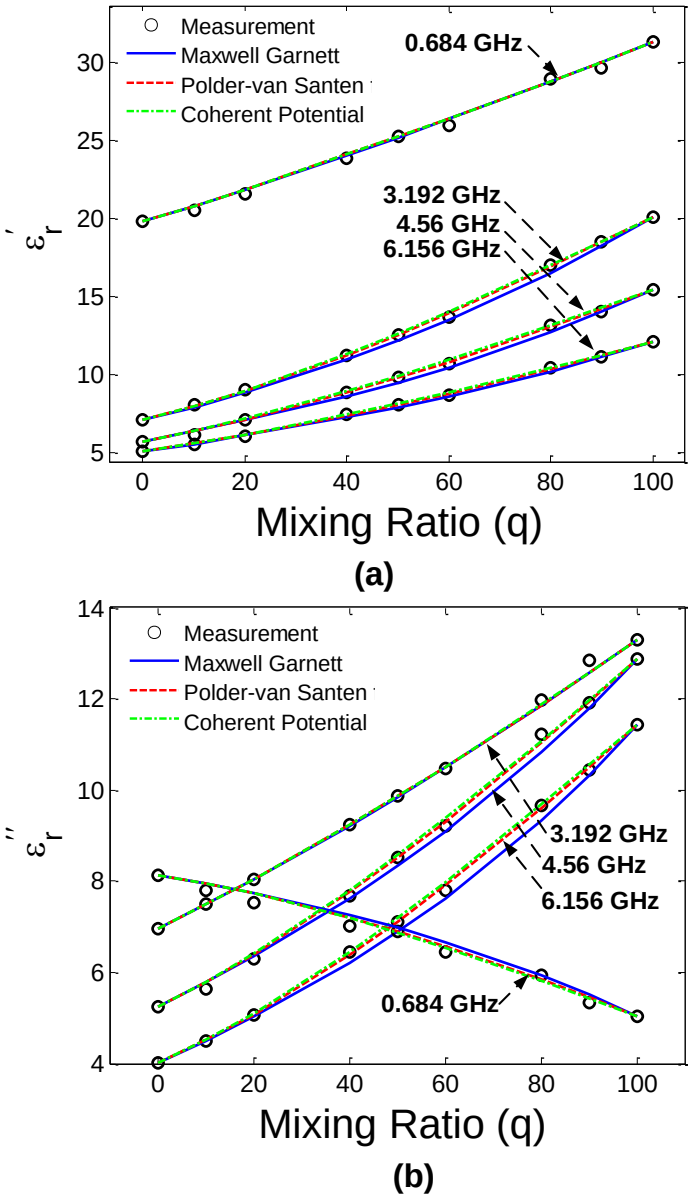


Figure 4.19: Measured and theoretical (a) ϵ_r' and (b) ϵ_r'' of ethanol-methanol mixtures versus mixing ratio, q, at different frequencies.

overall mixture's salt concentration. Fig. 4.22 shows excellent agreement between measured and theoretical values of ϵ_r'' versus frequency, where q=0% corresponds to DI water with no PBS added, and q=100% corresponds to 1X PBS solution. The

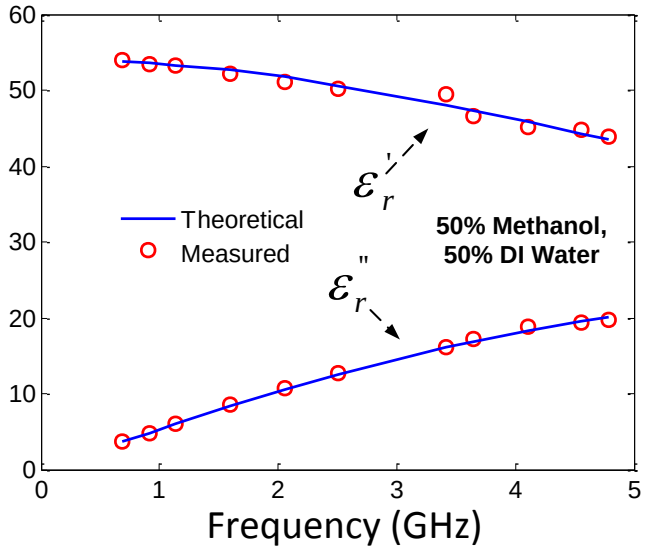


Figure 4.20: Measured and theoretical ϵ_r' and ϵ_r'' of 50% water-methanol mixture versus frequency.

points q={0, 50, 100}% were used for calibration, and the maximum error in ϵ_r'' is 4.5% over the entire band 0.7 GHz-4.77 GHz. These results verify the potential for this system to be used for biomedical applications. For example, the system could be extended to characterize particle suspensions by employing a microfluidic system to confine the sample/particles on top of the sensing area.

Table 4.3 summarizes the system performance and compares this work against other reported CMOS dielectric spectroscopy systems. To the best of our knowledge, this work presents the first fully integrated system that could characterize both MUT ϵ_r' and ϵ_r''. Compared to [17], [18], and [19], which require external frequency synthesizers and voltage-mode ADCs, the proposed system integrates the sensor inside the on-chip VCO/PLL and uses a simple counter for frequency shift measurements that yield comparable accuracy. Note that the power consumption of the proposed ring oscillator based system should scale with technology. Relative to the LC-VCO

systems of [2], [28], and [51], this work achieves a much wider continuous 0.7-6 GHz range, while also characterizing both ϵ_r' and ϵ_r''.

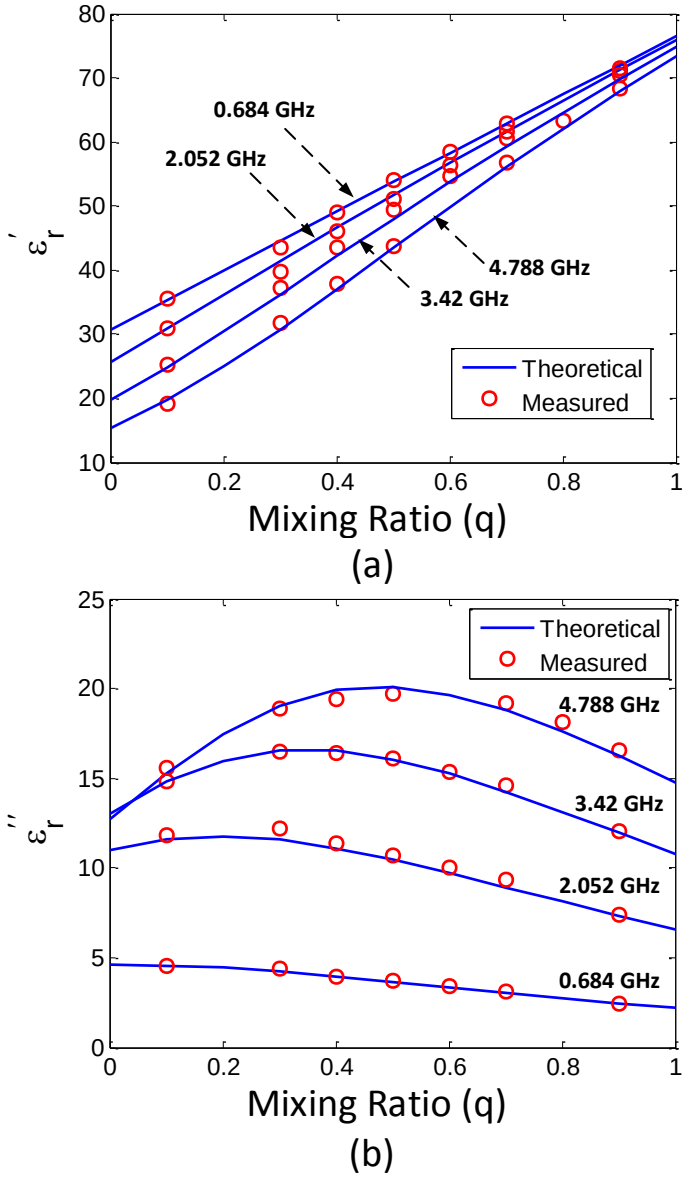


Figure 4.21: Measured and theoretical (a) ϵ_r' and (b) ϵ_r'' of water-methanol mixtures versus mixing ratio, q, at different frequencies.

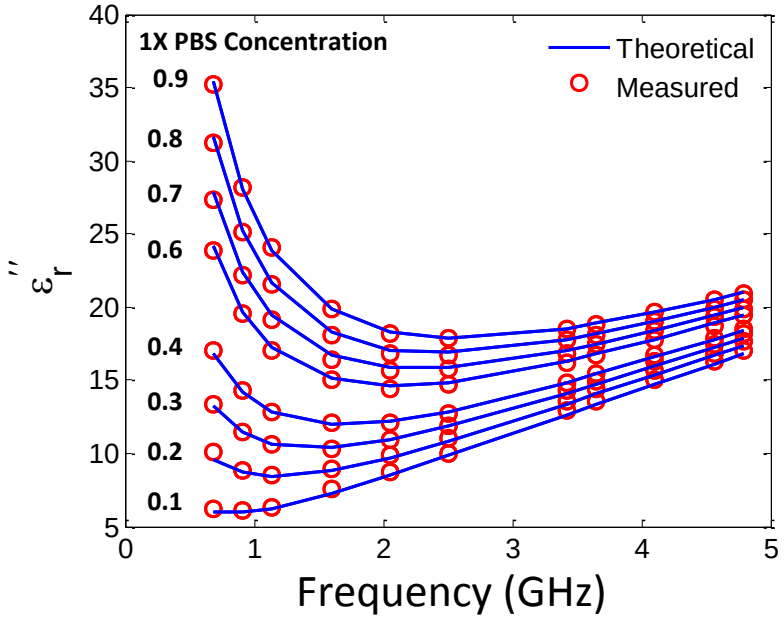


Figure 4.22: Measured and theoretical ϵ_r'' of PBS with different salt concentration versus frequency.

Table 4.3: Performance summary and comparison to previous work

Specification	This Work	[18]	[19]	[17]	[2]	[28]	[51]
Technology	180 nm	65 nm	180 nm	350 nm	90 nm	90 nm	65 nm
Functionality	$\epsilon_r', \epsilon_r''$	$\epsilon_r', \epsilon_r''$	$\epsilon_r', \epsilon_r''$	ϵ_r'	ϵ_r'	ϵ_r'	ϵ_r'
Fully Integrated	Yes	No	No	No	Yes	Yes	Yes
Sensing Frequency (GHz)	0.7-6	1-50	1-10	0.05-2.5	7-9	10.4	6.5/11 17.5/30
Max Error	3.7 %	NA	rms error 1%	1% (2GHz) 8.7%(2.5GHz)	3.7 %	1.5 %	NA
Noise	0.12 % frequency shift 0.2-3.5 % permittivity change	1%[a] permittivity change	NA	NA	3.5% permittivity change	1.5×10^{-3}% frequency shift 0.1 % permittivity change	5×10^{-4}% frequency shift
Power (mW)	69-140	114	65-72	4-9	16.5	22	65
Area (mm^2)	6.25	1.2	9	1.44	6.25	2.15	1.6[b]

[a] Calculated for $|\epsilon| = 4.45$ at 20 GHz.
[b] Estimated based on the area of one channel.

4.7 Conclusion

This work presented a fully integrated BDS system utilizing a ring oscillator-based PLL for wide band operation. A novel procedure is proposed for extracting MUT ϵ_r' and ϵ_r'' using two frequency shift measurements, which is considerably simpler than voltage measurement approaches. The proposed system achieves the highest CMOS integration level and could accurately characterize ϵ_r' and ϵ_r'' of methanol-ethanol mixtures, water-methanol mixtures, and PBS solutions over a wide frequency range.

5. CONCLUSION

Dielectric spectroscopy systems that study the permittivity of MUT versus frequency have several biomedical and industrial applications. High sensitivity, low power and fully integrated systems are required for Lab-on-chip and point-of-care applications. This thesis presented several techniques to enhance self-sustained CMOS dielectric spectroscopy systems.

First a self-sustained fractional-N PLL-based CMOS sensing system is presented. A reference VCO is employed, in addition to the sensing VCO, to track correlated low-frequency drifts. A simple single-step material application measurement procedure is enabled with a low-complexity bang-bang control loop that samples the difference between the control voltage with the sensor and reference oscillator in the PLL loop and then adjusts a fractional frequency divider. The system employs a 25-bit fractional-N which enables down to 6×10^{-4} ppm quantization noise. The system achieves 15 ppm noise limited by the noise of the comparator which maps to a $0.1\%_{rms}$ permittivity error. Binary mixture characterization of organic chemicals yield maximum errors in permittivity of $<1.5\%$.

Another frequency measurement technique is proposed that employs a sensing VCO that is placed inside an integer-N PLL, to allow precise control of the sensing frequency. In parallel, a reference VCO is placed in an open-loop configuration and is controlled by an RC-filtered version of the PLL control voltage, to enable cancellation of frequency drift due to temperature variations and correlated low frequency noise [46]. A simple digital counter is employed to perform the frequency shift measurements by measuring the oscillating frequency of the reference VCO (while the oscillating frequency of the sensor is set by the PLL). A 32-bit counter is em-

ployed that yields a quantization noise less than 0.01 ppm. Table 5.1, compares the bang-bang fractional-N based frequency measurement technique with the counter-based technique. The bang-bang fractional-N based frequency technique achieves faster measurement time. On the other hand, the counter-based method has lower bandwidth which enables better noise filtering.

Table 5.1: Bang-bang fractional-N based versus counter-based frequency measurement techniques

Technique	Bang-bang fractional-N based	Counter-based
PLL Divider	Fractional-N	Integer-N
Speed	Fast (μsec)	Slow ($m$sec)
Bandwidth	Low (Hz)	High (KHz- MHz)

A wide tuning range ring VCO based complex dielectric spectroscopy system is proposed. As the ring VCOs' oscillation frequency is a function of the delay cells' RC time constant, it is possible to detect both $\epsilon'_r(\omega)$ and $\epsilon''_r(\omega)$ by employing delay cells with sensor element loads whose capacitance and conductance (loss) changes with MUT application. A novel two-step detection procedure is proposed which employs an amplitude-locked loop (ALL) to efficiently detect both $\epsilon'_r(\omega)$ and $\epsilon''_r(\omega)$ independently through only two frequency shift measurements. When tested with common organic chemicals ($\epsilon'_r < 30$), the system operates between 0.7-6 GHz and achieves 3.7% maximum permittivity error. Characterization is also performed with higher ϵ'_r water-methanol mixtures and phosphate buffered saline (PBS) solutions, with 5.4% maximum permittivity error achieved over a 0.7-4.77 GHz range.

Overall, the high-level of integration and compact size achieved in these proposed systems makes them suitable for lab-on-chip and point-of-care applications. However, there are several requirements to enable biomedical applications, lower noise and lower power consumptions. In order to extend the proposed systems to biomedical applications such as characterizing particle suspensions, a microfluidic system is required to confine the sample/particles on top of the sensing area. And, the appropriate frequency range should be chosen based on the application. Regarding the system noise, it is one of the most important parameter of the system. The low frequency variations and flicker noise usually dominates the noise performance of sensors. Introducing a reference oscillator in addition to the sensing oscillator allows canceling the low frequency correlated noise. In order to increase the correlated noise between the two oscillators, more elements should be shared between the oscillators. Ideally only one oscillator is employed (all elements are shared) with switches to choose between the sensor and a dummy capacitor. While this maximizes the correlation the switches limits the maximum frequency. Note that to enable this in ring-oscillator based system with the ALL, a sample and hold circuit is required to track the peak detector output with the sensing oscillator enabled and hold it while the reference oscillator enabled. Finally, power consumption is an important system parameter because low power consumption enables portable applications. Technology and maximum operating frequency of the system are the most important factors that determine the power.

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