A FAULT TOLERANT 3-PHASE ADJUSTABLE SPEED DRIVE TOPOLOGY WITH COMMON MODE VOLTAGE SUPPRESSION

A Thesis

by

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ABSTRACT

A fault tolerant adjustable speed drive (ASD) topology is introduced in this work. A conventional ASD topology is modified to address: a) drive vulnerability to semiconductor device faults b) input voltage sags c) motor vulnerability to effects of long leads and d) achieve active minimization of common mode (CM) voltage applied to the motor terminals. These objectives are attained by inclusion of an auxiliary IGBT inverter leg, three auxiliary diodes, and isolation - reconfiguration circuit. The design and operation of the proposed topology modifications are described for different modes; (A) Fault mode, (B) Auxiliary Sag Compensation (ASC) mode and (C) Active Common Mode Suppression mode. In case of fault and sag, the isolation and hardware reconfiguration are performed in a controlled manner using triacs/anti-parallel thyristors/solid state relays. In normal operation, the auxiliary leg is controlled to actively suppress common mode voltage. For inverter IGBT failures (short circuit and open circuit), the auxiliary leg is used as a redundant leg. During voltage sags, the auxiliary leg along with auxiliary diodes is operated as a boost converter. A current shaping control strategy is proposed for the ASC mode. A detailed analysis of common mode performance of the proposed topology is provided and a new figure of merit, Common Mode Distortion Ratio (CMDR) is introduced to compare the attenuation of common mode voltage with that of a conventional ASD topology for three different modulation strategies. The output filter design procedure is outlined. A design example is presented for an 80 kW ASD system and simulation results validate the proposed

auxiliary leg based fault tolerant scheme. Experimental results from a scaled prototype rated at 1 hp prototype also confirm the operation. The common mode analysis is also validated with the experimental results.

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NOMENCLATURE

PWM	Pulse Width Modulation
AC	Alternating Current
DC	Direct Current
CM	Common Mode
RC	Resistor Capacitor
LC	Inductor Capacitor
RLC	Resistor Inductor Capacitor
LCR	Inductor Capacitor Resistor
RMS	Root of Mean of Squares
THD	Total Harmonic Distortion
IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
TkW-hr	Trillion Kilo Watt Hour
V	Volts
A	Amperes
IEC	International Electrotechnical Commission
SEMI	Semiconductor Equipment and Materials International
IEEE	Institute of Electrical and Electronics Engineers
NEMA	National Electrical Manufacturers Association
MDS	Motor Drive System
ASD	Adjustable Speed Drive

hp	Horse Power
U.S.	United States
p.u.	per unit
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
AZSPWM	Active Zero State Pulse Width Modulation
CM	Common mode
R-L	Resistor Inductor
PSIM®	Simulation package by Powersim Inc.
MATLAB®	Software by Mathworks Inc.
APT	Anti-parallel thyristors
FFT	Fast Fourier Transform

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I INTRODUCTION

I.1. Introduction

Electric energy is a major source of energy all over the world. The estimated cumulative annual electric energy production of the world in 2011 was 22.126 TkW-hr [1]. This generation is projected to increase up to 39 TkW-hr by 2040 [2]. According to International Energy Statistics, in 2011 United States domestic electricity consumption was 4.12 TkW-hr [1]. Out of this, in United States, about 38% of all electric energy is consumed by motor driven equipment like pumps, compressors and fans [3].

The increase in average retail price for electricity (in cents/kW-hr) for different sectors is illustrated in Figure 1. Figure 1 is plotted by taking annual average of the data obtained from Energy Information Administration [4]. It is evident from Figure 1 that the price of electricity has been steadily increasing. Motor drives consume up to half of the electricity used by manufacturing sector. Increasing prices of electricity and large electric energy consumption has motivated the industry to increase efficiency of motor-driven systems. The extensive use of motor drives implies that incremental improvement in efficiency has a significant financial impact. One of the most effective ways to boost motor actuated system efficiency is use of adjustable speed drive (ASD).

In pump or fan applications, a small reduction in speed can significantly reduce energy consumption. This is due to the facts that load torque, and hence power, profile is non-linearly dependent on speed. For example, a pump or fan running at 50% speed may consume only 12.5% ($1/8^{th}$) of the rated power at 100% speed. Traditionally, the motor is operated at constant speed using direct drives. Mechanical control valves are used to

regulate flow or mechanical gears are used to change speed of the pump which in turn changes flow speed. Regular maintenance is essential when mechanical elements like control valve or gears are used. Also, these mechanical speed control methods are lossy. Modern motor drive systems use ASDs for conditioning input power to the motor. The input power is controlled using ASD to achieve variable speed operation more efficiently.

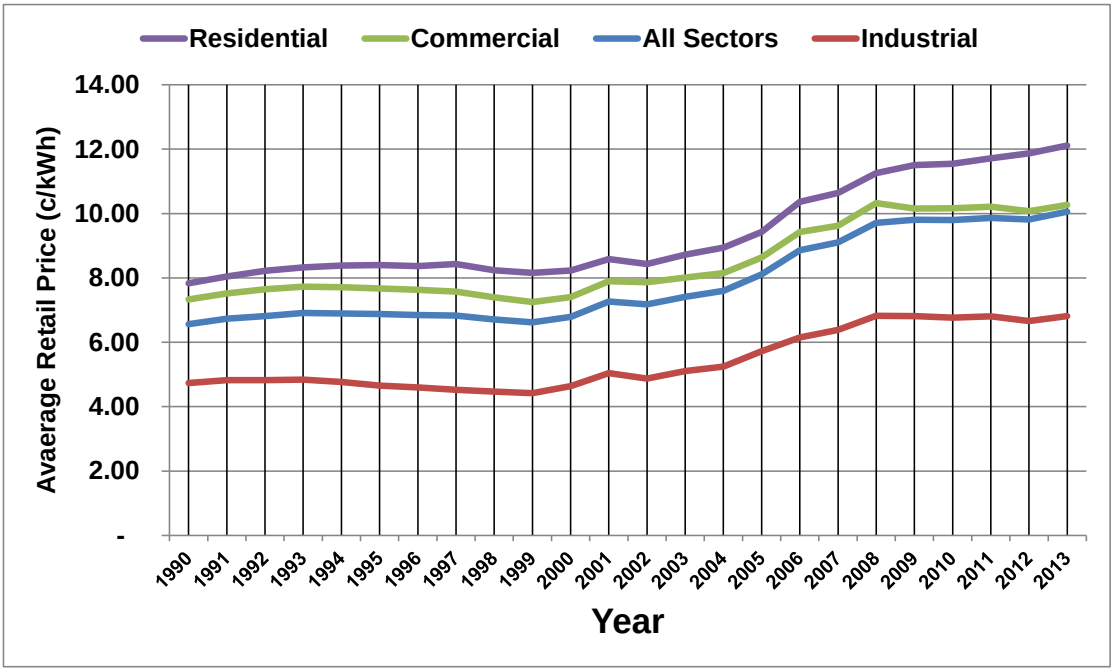

Figure 1. Average retail price of electricity in United States from 1990 to 2013

The input power to the electric motor is conditioned using Power Electronic blocks. These power electronic blocks offer benefits of precise control and enhanced

efficiency. A typical motor drive system (MDS) with ASD is shown in Figure 2. The measurement and control unit changes the operating point based on the load.

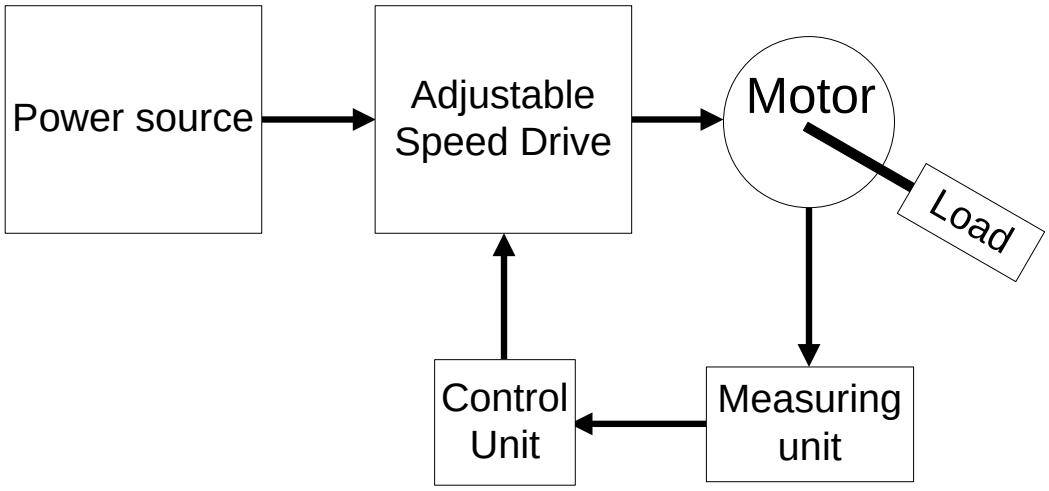

Figure 2 Typical motor drive system with ASD, motor and control

A more detailed schematic of a conventional MDS is shown in Figure 3. The major power electronics blocks in ASD are as follows:

a. Front end: 3-phase diode rectifier or 6-pulse rectifier

b. DC link

c. Back end: 3-phase PWM inverter

The front end consists of a 3 phase diode rectifier (*D1-D6*) which converts 3 phase AC voltage to DC voltage. An L-C filter is formed using L_{rec} and C_{dc} to achieve a stiff DC bus voltage. Large input line inductors also improve the input current harmonics. The 3-phase PWM inverter converts this DC voltage into a 3 phase output to

control the machine. Output filters are employed when long motor leads are used. The other components of MDS include the motor and utility supply.

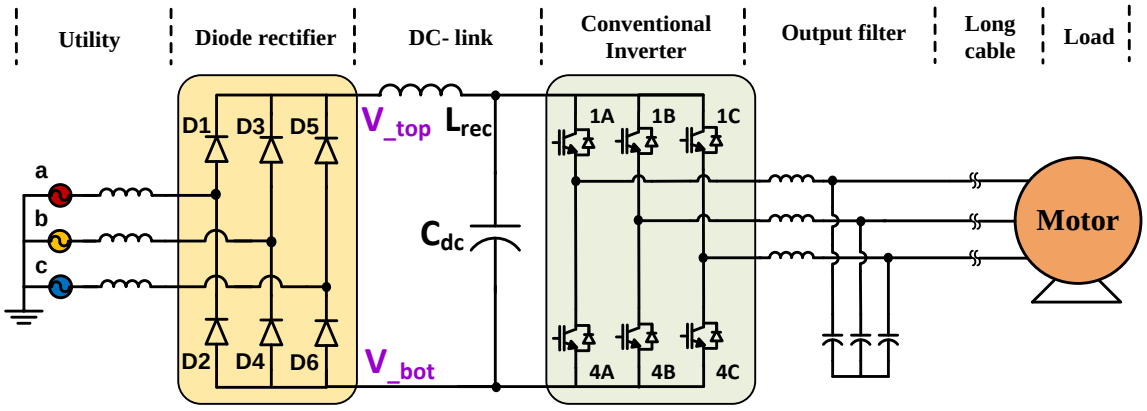

Figure 3. Conventional ASD topology with three phase diode rectifier, DC link, PWM inverter and output filter

I.2. Issue Affecting Motor Drive System Availability

The use of MDS is widespread in applications like wastewater treatment, petrochemical industry, cement industry, compressor, crusher and steel rolling mills [5]. In a number of these applications, MDS is integral part of a continuous process [6]. Any interruption of the manufacturing process is expensive because of production loss and follow-up costs [7, 8]. Therefore the availability of MDS in such applications has an immense financial impact. This has triggered interest in failure modes of both ASDs and motors [5, 9-12]. Other power interruption phenomena like voltage sag/ swells which affect MDS availability have also been studied extensively [13-15]. These and other

factors which affect the availability of MDS are summarized in Figure 1. The following sections provide descriptions on the nature and effect of these factors.

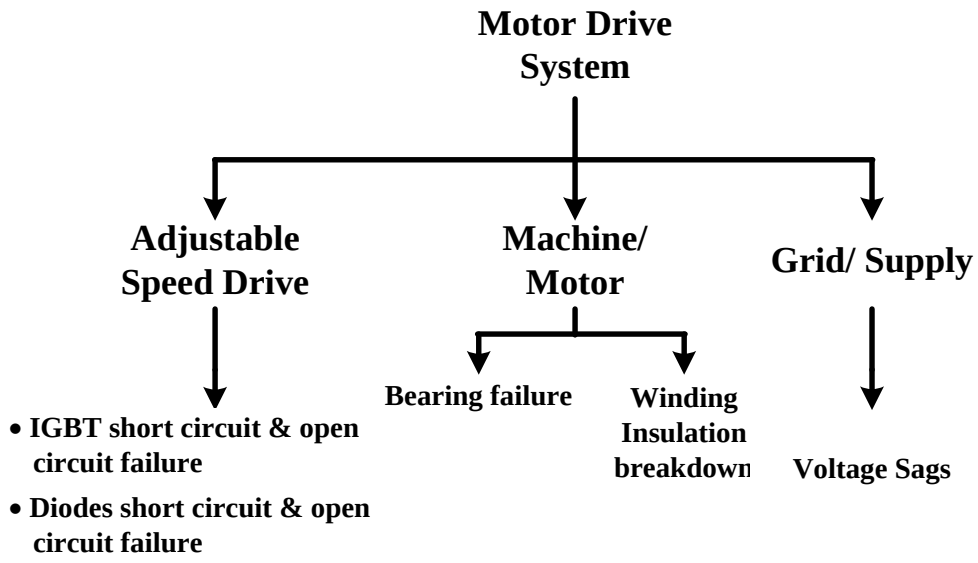

Figure 4. Issues affecting motor drive system availability

I.3. Adjustable Speed Drive

The failure of ASD is closely related to failure of semiconductor devices. Failures in power electronic circuits result in up to 37% of ASD failures and power switching components have been identified to have greater failure rates than other components in the drive system [16]. Up to 40% of the 3-phase inverter failures in the field can be attributed to power transistor failures [17].

I.3.1. Semiconductor device failure

The conventional ASD topology shown in Figure 3 uses diodes and Insulated Gate Bipolar Transistors (IGBTs) as power semiconductor devices. Modern drives use

highly integrated power modules which utilize different materials in their construction. This leads to non-uniform thermo-mechanical stresses and consequently fatigue induced failures [18]. Another mode of failure for high power IGBT modules is insulation failure [19]. Other failure mechanisms for IGBT due to parasitic bipolar junction transistor (BJT) latch up, V_{CE} overvoltage breakdown due to high $\frac{dV_{CE}}{dt}$ spikes during turn off, and thermal breakdown are discussed in [20]. A summary of failure mechanisms for power semiconductors is provided in Table 1.

Table 1. Failure mechanisms in power semiconductor devices

Device	Failure state	Failure mechanisms (add more info)
IGBT, MOSFET, Diode	Open	• Bond wire fatigue; lift-off and wire heel cracking • Aluminum reconstruction • Brittle cracking and fatigue crack propagation • Corrosion of interconnections • Solder fatigue and solder voids • Gate drive failure (IGBT & MOSFET) • Insufficient device derating
	Short	• Burnout failures • Latch up • Energy shocks • Second breakdown • Insufficient device derating • Body diode reverse recovery (MOSFET) • Gate drive failure (IGBT & MOSFET) • High voltage breakdown

I.4. Motor

I.4.1. High frequency common mode voltage

In depth analysis of motor failure data obtained from a survey of industrial and commercial installations is provided in [12]. This data on electric machine failures provides significant insight. Bearing and winding failures together account for almost 70% of total electric machine failures in this survey. The data also reveals that mechanical breakage and insulation breakdown are the dominant cause for bearing and winding failures respectively. Besides mechanical and thermal failure mechanisms, bearing currents leads to bearing failure. According to [21], up to 9% of bearing failures are caused by bearing currents. Apart from mechanical breakage and overheating, large voltage overshoots lead to insulation breakdown failures.

A modern high frequency PWM motor drive results in a high frequency common mode voltage at the motor terminals. This high frequency voltage leads to a high frequency current which flows to the ground through stray coupling capacitors. There are multiple paths available to this current, and its relative magnitude in each path depends on the respective impedance values and adopted grounding scheme. This high frequency current partly flows through the motor bearings. The bearing currents can be the result of capacitive coupling through one or more of the following – capacitive discharge current, circulating current and shaft grounding current [22, 23].

If the motor frame is earthed and shaft is not (Figure 5), a portion of common mode voltage on the stator is induced on the shaft through internal parasitic coupling capacitors. Typically C_{sr} is smaller relative to C_{rf}. So the shaft voltage is usually

insufficient to cause a lubrication film breakdown. However, if this induced voltage is high enough it can cause capacitor discharge current.

The high frequency circulating currents exist due to the high frequency common mode current which leaks in to the stator frame which in turn leads to a high frequency flux. This asymmetric flux induces a voltage between the shaft ends. This voltage can induce a circulating current through the bearings which tries to cancel the asymmetric flux. The path of this circulating current is rotor/shaft to bearing to frame to bearing.

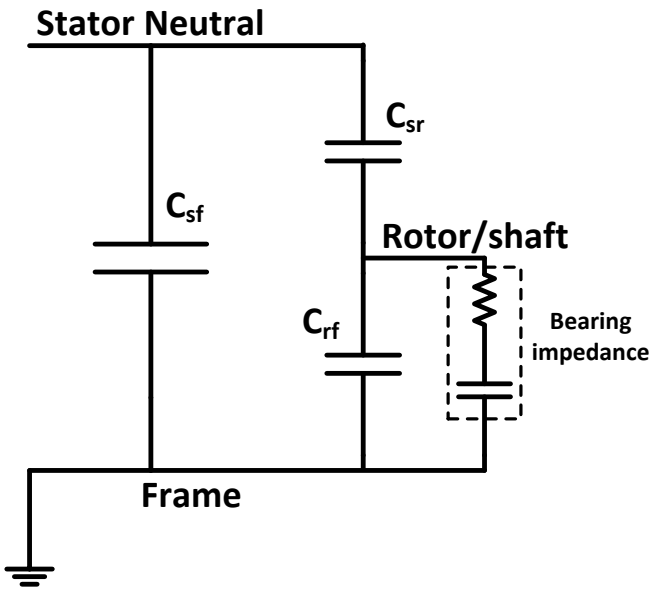

Figure 5. Parasitic capacitive coupling between stator, frame and rotor

The shaft grounding current occurs when the motor shaft is earthed through gearbox and inverter. Any increase in motor frame voltage above ground causes a

current to flow through motor frame, the drive-end bearing to the shaft which returns back to the inverter.

In all three mechanisms if energy of the high frequency current pulses is higher that a threshold value, it leads to the erosion of the bearing and races through a phenomenon known as Electrical Discharge Machining (EDM). These repeated discharging events gradually erode the bearing races [12, 24]. This leads to early mechanical failure of the machine. It is important to note that electrical grounding plays a vital role in determining the magnitude and generation mechanism of bearing currents [22, 23].

I.4.2. Effect of long leads

As mentioned before, high dv/dt overshoots damage motor winding insulation. With the introduction of fast power semiconductor devices like IGBTs, designers have pushed for higher inverter switching frequencies to improve output current quality, reduce audible noise and filter size. As the inverter switching frequency increases, the voltage transients become faster, i.e. rise/fall time reduce, and dv/dt overshoots become larger. Prolonged dielectric or voltage stresses lead to gradual deterioration of the dielectric strength of insulation material and ultimately result in catastrophic failure. Along with carrier frequency, motor cable length plays a critical role in determining the voltage overshoot stress on the motor terminals. Significant research has been conducted to examine the effect of carrier frequency and motor cable length on motor terminal overshoot. NEMA standard MG1 and technical guides from different manufacturers provide guidelines on stator winding insulation strength for different applications.

Magnetic wire insulation life curves shown in Figure 6 illustrate the effect of increasing cable length and carrier or switching frequency.

The voltage overshoots due to reflected voltage pulses and ringing with cable parasitic elements lead to escalated voltage stress on the motor winding insulation. A detailed reflection analysis is presented in [25] which relates motor terminal overshoots with motor cable length and PWM voltage rise time. A parameter called critical rise time, (1), is computed to determine the rise time to obtain a desired voltage overshoot (≈20%) [25].

$$t_r = \frac{3 \cdot l_c \cdot \Gamma_L}{v \cdot 0.2} \tag{1}$$

where

l_c is cable length;

Γ_L is reflection coefficient at the load (typical value is 0.9);

v is pulse velocity given by $\frac{1}{\sqrt{L_c \cdot C_c}}$;

L_c is cable inductance per unit length;

C_c is cable capacitance per unit length;

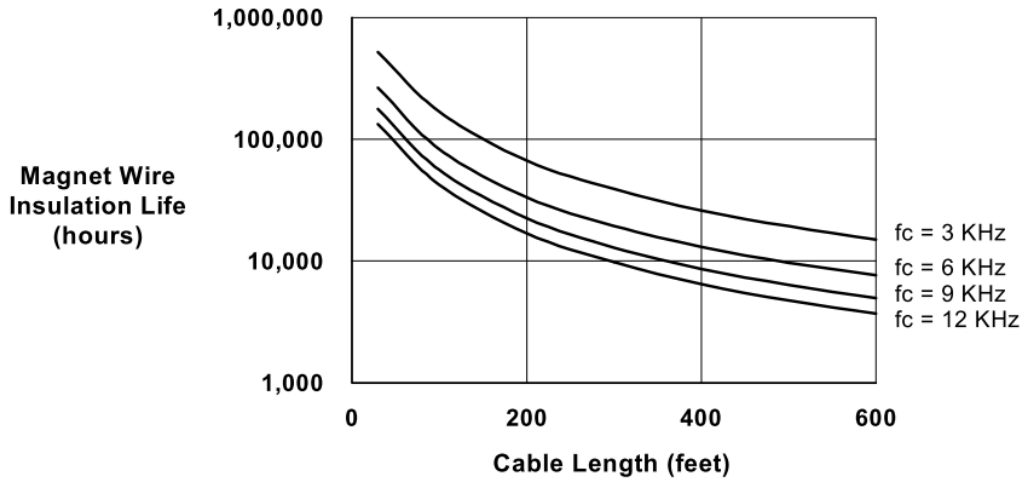

Figure 6. Insulation life of magnetic wire versus cable length for various inverter carrier frequency (f_c) (Source: [26] copyright ABB, 2014, all rights reserved.)

It is observed for a lower overshoot, the rise time should be limited to a larger value.

I.5. Grid/Supply

I.5.1. Voltage sags

Like any other industrial equipment, voltage sags in the supply can also lead to MDS trips and unwanted shutdowns. IEEE 1547.2 standard defines voltage sag as "a decrease to between 0.1 to 0.9 p.u. in rms voltage or current at the power frequency for duration of 0.5 cycle to 1 min" [27]. Voltage sag is different from complete loss of voltage or interruption. Interruptions are result of faults in the immediate power circuit. On the other hand, voltage sags occur due to faults on a wider power network. Voltage sags typically cause disruption of operation of sensitive electronic loads like ASDs.

According to various power quality surveys, voltage sags are the main cause of disturbances which lead to production loss. This loss is caused by voltage drops of more than 13% of rated voltage and a duration longer than one half cycle [15].

Standards like SEMI F47 and IEC standards 61000-4-11 (less than 16 Amperes) and 61000-4-34 (greater than 16 Amperes) define equipment immunity requirements with respect to voltage sags. Based on these standards, typical under-voltage protection level for DC bus voltage is set at 87% to 70% of the nominal value in commercial drives [28, 29]. This lock out protects the power electronic components during under voltage condition. Although under-voltage trip is an important protection feature, according to [28] a tripped could take up to 8 hours before returning to full production capacity in an oil and gas application. Similarly in a gas plant, the estimated cost of an outage less than 0.1 s (5 cycles) is about $200,000 [7]. For an automobile manufacturing plant, momentary outage cost was reported to be over $300,000 [30]. The cost of a single sag event for another industrial customer is estimated to be €1200 [31, 32].

I.6. Prior Work

In this section, existing solutions are presented which mitigate the effect of the above discussed factors influencing MDS availability. First, existing fault tolerant topologies are explored. Second, the existing common mode voltage minimization techniques are discussed. Third, remedies available for reducing dv/dt at motor terminals are presented. Next, the previously published voltage sag compensation techniques are described.

I.6.1. ASD failures

A number of fault tolerant ASD topologies have been proposed to mitigate effects of semiconductor device failures. A detailed review of published fault detection techniques is provided in [33] and fault tolerant inverter topologies have been presented in [10] and [34]. Since fault detection is not the focus of this work, it is not discussed here in detail. Fault tolerance is typically achieved by introducing redundancy or added complexity. Three techniques are popular in literature.

First approach (Figure 7) is to connect the faulty phase to DC link mid-point using anti-parallel thyristors (APTs) [35]. Second approach (Figure 8) is to isolate the faulty phase and connect the motor neutral to the DC link mid-point [36]. A third approach (Figure 9) is to introduce an additional leg which is connected to the motor neutral [37].

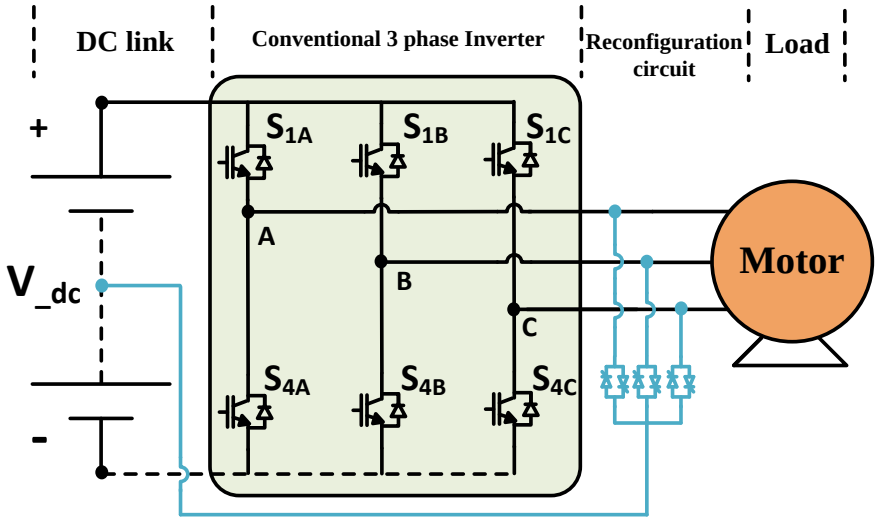

Figure 7. Fault tolerant approach with faulted phase connected to DC link mid-point

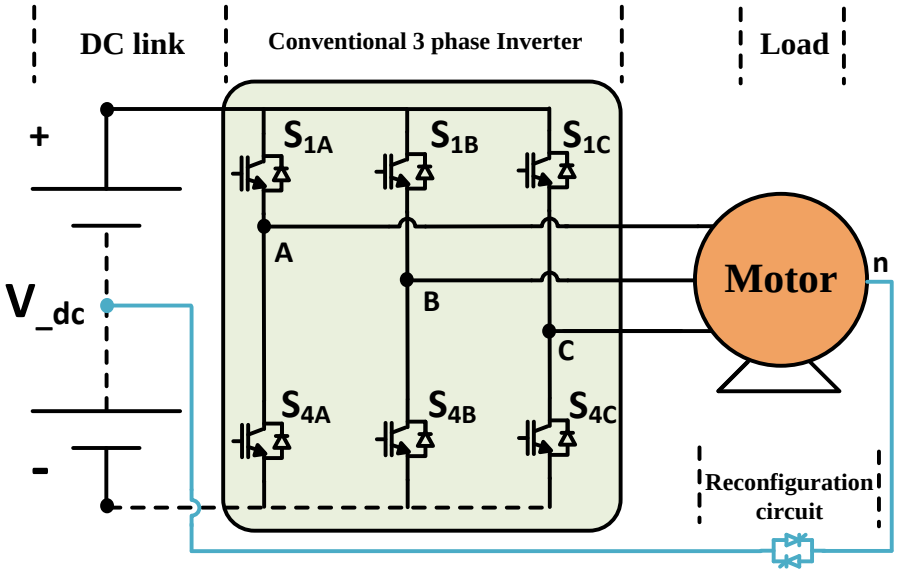

Figure 8. Fault tolerant approach with motor neutral connected to DC bus mid-point

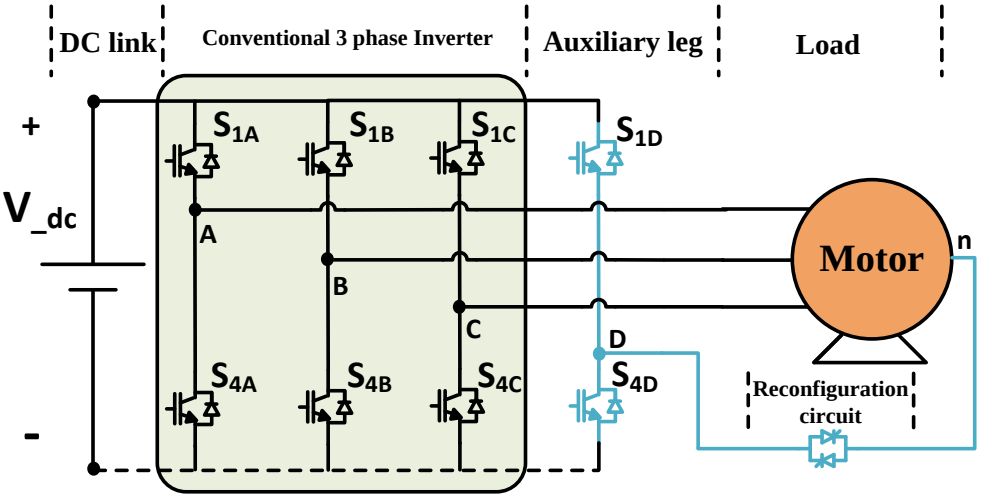

Figure 9. Fault tolerant approach with motor neutral connected to auxiliary leg

The disadvantages of these three approaches have been summarized [10] in Table 2. Other techniques involve inclusion of parallel inverters [10], redundant modules [10] and redundant series leg [10]. More recently, phase redundant approach [17, 38-40] has gained popularity due to 100% post fault output capabilities without drive overrating at a lower cost. A detailed cost and feature comparison of different fault tolerant topologies is presented in [9].

Table 2. Disadvantages of existing fault tolerant approaches

Approach	Disadvantage
Faulted leg to DC-link mid-point	• Line to line output voltage is reduced to half of the nominal value • Lower inverter output power • Access to DC-bus mid-point is required • 60 Hz current flows through the mid-point which requires oversizing of DC capacitors
Motor neutral to DC-link mid-point	• Higher current in post fault operation requires device oversizing • Line to line voltage is reduced to half of the nominal value • Access to both DC bus mid-point and motor neutral is required. • Oversizing of DC bus capacitor due to 60 Hz current • Extra cost due to the long fourth wire
Motor neutral to auxiliary leg	• Extra cost due to the additional auxiliary leg • Operation only possible for a short period of time due to losses and magnetization [41] • Complex control strategy required • Access to motor neutral point is required • Extra cost due to the long fourth wire

I.6.2. High frequency common mode voltage

High frequency common mode voltages induce high frequency bearing currents which cause erosion of bearing and race. A lot previous work has been done on the detection of bearing faults. Since the focus of this work is not bearing fault detection, these detection techniques are not described here.

The existing solutions to the problems of bearing currents and common mode voltage fall under one of the following two categories. Firstly, the motor installation could feature: insulated or ceramic bearings, grounding brush contact, conductive grease and insulated coupling methods [23]. Additional filter components ($\frac{dv}{dt}$ filter or sinusoidal output filters) can also be installed to modify the shape of inverter output. Common mode filters are also installed to attenuate the common mode current. Secondly, modification to the inverter could be made to eliminated common mode voltage, such as: a dual inverter bridge approach open winding [42] and double winding machines [43]. Alternative approaches involving auxiliary inverter have been illustrated in [44, 45]. Another method proposed in [46] involves the use of an additional half bridge to actively cancel common mode voltage. A summary of existing solutions [23] is provided in Table 3.

Table 3. Existing solutions for attenuation of common mode voltage and bearing current

Solution	Effect	Disadvantage
Correct electrical installation	Limits the problem	Techniques like shaft grounding brushes are prone to wear and tear
Insulated bearing and other insulated coupling methods	Effectiveness needs to evaluated on case to case basis	Effect depends on the motor frame size and needs to be decided on case to case basis. Expensive.
Install Faraday shields in motor	Reduces parasitic coupling between stator and rotor	Expensive and difficult to manufacture
Conducting grease	Provides low impedance path to avoid partial insulating effect	Particulates added to make the grease conductive can erode bearing
Modify Switching frequency	Reduces the high frequency harmonics in common mode voltage	Can lead to audible noise, heating and performance issues
Output filter	Effective in reducing high frequency common mode voltage	Expensive and bulky
Modify inverter topology	Reduces common mode voltage at the source	Expensive and complex

I.6.3. Effect of long leads

Three methods have been published to mitigate the effect of high voltage stress; inverter output reactors, inverter output $\frac{dv}{dt}$ filters and cable termination filters (Figure 10).

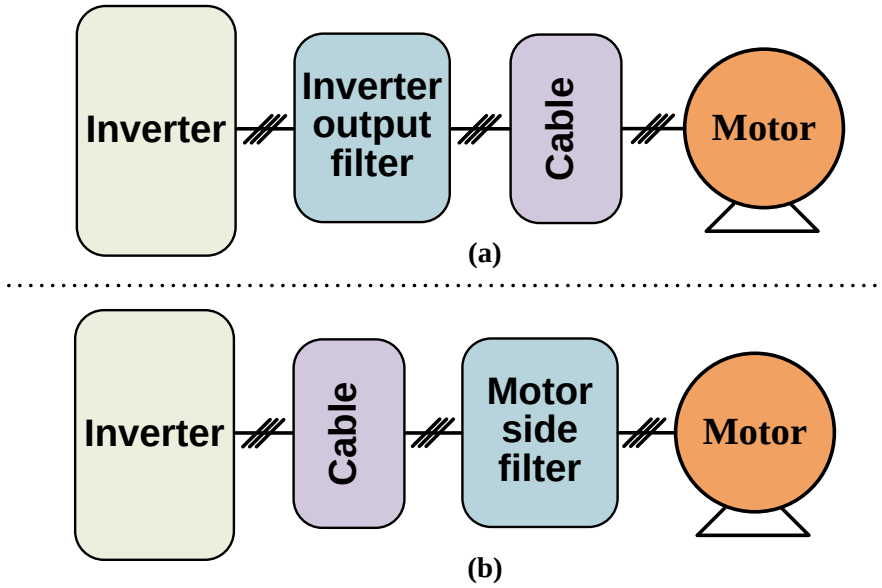

Figure 10. Different passive filter types used to mitigate effect of dv/dt. (a) output reactors and dv/dt filters, and (b) cable termination or motor side filter

A review of different mitigation techniques has been presented in [47]. A design method for inverter output filter has been proposed in [25]. This method utilizes reflected wave analysis for filter design. A comparison of the design with cable termination filter/ motor terminal filter is also presented. Design of motor side passive resistive, first order and second order termination filter has been proposed in [48]. The effectiveness of these filters and power loss comparison is also discussed. Another LC clamp filter has been proposed in [49]. The size and power loss of the proposed filter topology is relative smaller than conventional filters.

I.6.4. Voltage sags

To improve the ride through performance of ASDs, several approaches can be found in the literature. One approach is to modify existing drive topologies to add ride through capability. A number of such techniques have been discussed in [30]. These techniques have been summarized in Table 4.

Table 4. ASD ride through by modification of existing drive

Sl. No.	Technique	Advantages	Disadvantages
1	Additional DC bus capacitors	Simple and rugged	• Relatively higher cost • Large volume requirement • Additional pre-charge and voltage balancing concerns
2	Load Inertia	• No additional hardware requirement • Commercially available • 2 sec of ride through for sags up to 80% nominal voltage • No delays in acceleration of motor at the end of sag event	• Motor speed reduced • Torque is reversed • Dependent on load inertia
3	Operation at reduced speed/load	• No additional hardware requirement • As speed and load decrease, ride through ability increases	• Only useful for variable torque load • Application may not tolerate reduced speed/torque operation
4	Low voltage motor	• No additional hardware required • Higher ride through time can be realized	• Lower voltage motor with same power rating requires higher current rating • Motor insulation capability should handle drive output rating • Sub-optimal use of drive

It is observed that all the four techniques discussed in Table 4 utilize modification of existing design, without increasing complexity. More intensive techniques involve use of additional hardware. These techniques employ complex control methods and are more expensive.

An auxiliary boost converter can be added in parallel with the existing DC bus to provide immunity to voltage sags. The topology has been shown in the Figure 11. The dc bus voltage is monitored and in case of voltage sag, boost converter can regulate the DC bus voltage to the reference value. Due to the additional hardware and control requirement, this solution tends to be more expensive. Also, the boost converter is to be rated for higher currents (> 1 p.u.) [8, 30].

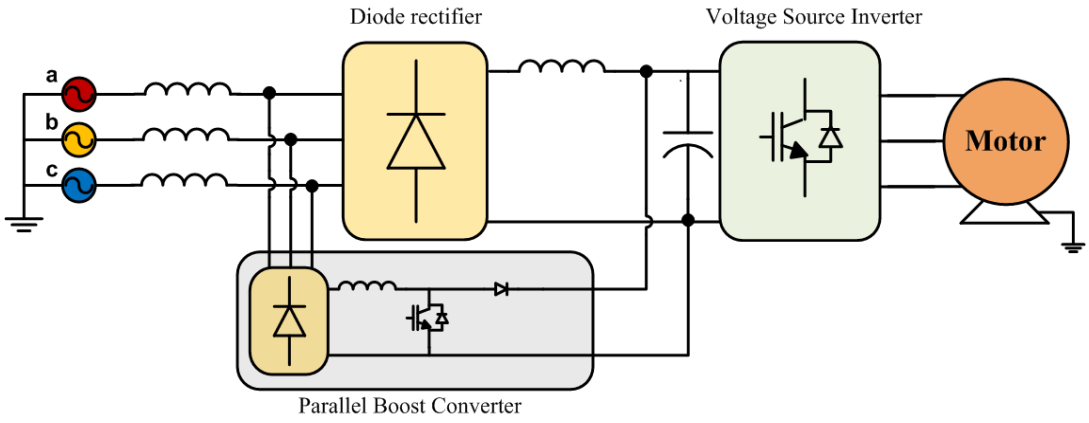

Figure 11. ASD with parallel boost converter for sag ride through

Another solution is to have a diode rectifier followed by boost converter in the regular operating condition. In this case, additional DC link choke and diode are in the path of power flow and hence affect efficiency. In both these solutions, the boost

converter will not be able to provide any ride through during outage [8, 30]. A similar approach is proposed in [13], where auxiliary diodes and additional IGBT leg are added to form a boost converter. In this approach, the DC link choke and diode are only added when the voltage sag occurs. The integrated boost converter regulates DC bus voltage during sag events. A more complex solution is to have a PWM rectifier at the front end. This topology is shown in Figure 12. Active front end offers several advantages such as regulated DC bus with immunity to voltage sags and transients, lower input current THD and regenerative braking capability. The sag ride-through capability is only limited by the current rating of the rectifier. This topology however is more complex and expensive (almost twice). The line reactors at the input are essential.

Other topologies with energy storage have also been explored in the literature. A concise comparison of topologies based on different energy storage elements have been presented in [8]. Unlike previous topologies, presence of an energy storage element in the system allows for full power ASD ride-through in case of power outage.

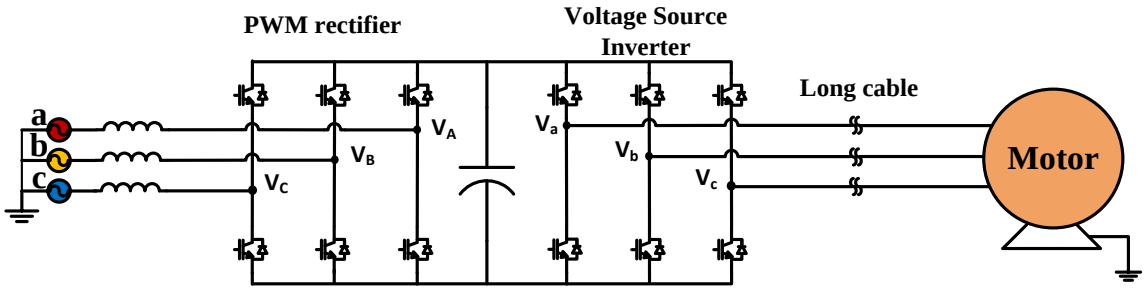

Figure 12. ASD topology with active front end

Energy storage can be used as a stand-by power source. There are two ways to interface it to the MDS. One method is to interface the energy storage system to the DC bus using a power converter. The other method is to set-up a re-charging path through the AC input and the discharging of the energy storage occurs through unidirectional connection made to the DC bus. A general topology has been show in Figure 13.

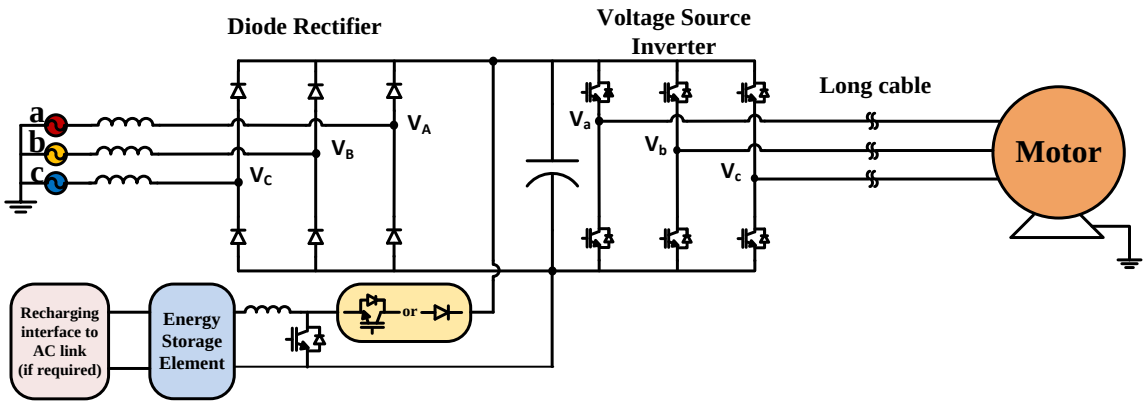

Figure 13. Energy storage interfaced to the DC link with recharging through DC bus or AC line

In this configuration, different energy storage elements like batteries, super-capacitors, flywheels, fuel cells and super conducting magnetic storage (SMES) can be used. The choice of storage element depends on the requirements like dynamic performance, energy range, power range, cost, lifetime, weight and volume constraints, and complexity of implementation. Another energy storage interface technique is to use this energy storage as a stand-by for ac line power. This topology is illustrated in Figure 14.

At the distribution level, shunt connected power electronics device like Dynamic Voltage Restorer (DVR) has been developed to compensate for sags and swell [50]. DVR makes the loads immune to power disturbances by compensating for upstream disturbances using energy storage. The load is supplied the compensated voltage.

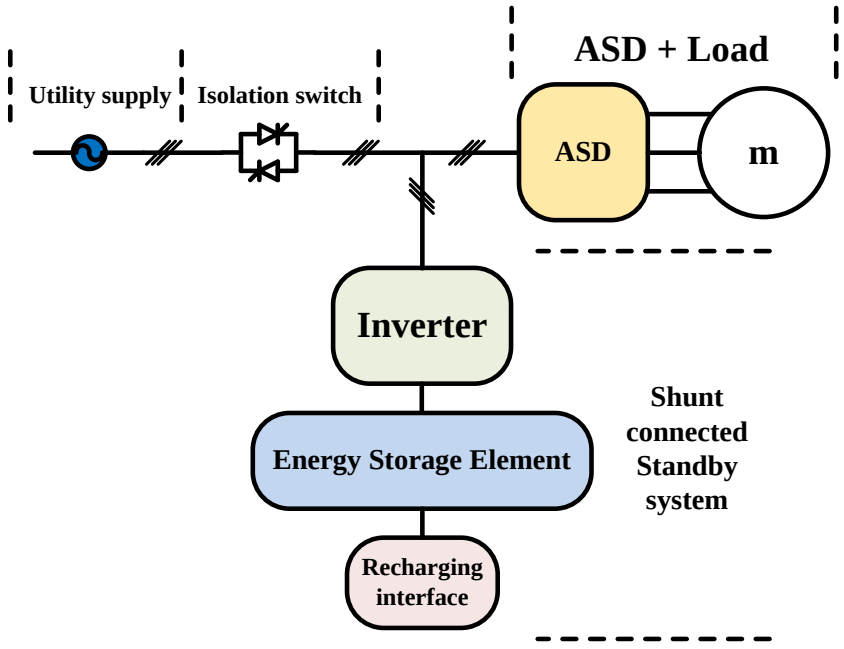

Figure 14. Shunt connected energy storage as standby AC power

I.7. Research Objective

As discussed in the previous section, the factors affecting failure of MDS have been studied rigorously in the literature. Though a number of different solutions exist which address these problems separately, none of the discussed approaches tackle all these issues with a single solution. The objective of this research is to develop a single motor drive system solution to mitigate the vulnerability of the adjustable speed drive to

semiconductor device failures, motor to bearing failure and winding insulation breakdown and system to input voltage sags. A fault tolerant 3-phase adjustable speed drive topology with active common mode suppression is explored. In addition to fault tolerance and common mode suppression, voltage sag compensation is also investigated. The topology operation is explored for three different mode of operation (a) Failure mode, (b) Voltage Sag Compensation mode and (c) Active Common Mode Voltage Suppression mode.

In the failure mode operation, short and open circuit device faults are considered. An isolation and reconfiguration strategy is discussed for the topology. The voltage and current transients are also investigated for input and output. The voltage sag compensation technique is described for the proposed topology. The sag isolation and reconfiguration strategy is illustrated. A new current shaping based control strategy is developed. Active common mode suppression technique is discussed and filter design procedure is described. Analysis of common mode voltage in different modulation strategies is investigated for the developed topology and the conventional drive topology. A new figure of merit is also developed to compare common mode performance in different cases.

A design example is provided for an 80 kW motor drive system with a 100 hp machine. The component sizing information is also presented. The simulation results are presented for different modes of operation. The experimental results obtained on laboratory prototype rated at 1 hp are discussed.

I.8. Thesis Outline

The thesis is organized in the following manner. In section I, a brief introduction about MDS is provided. The different factors which effect availability of a MDS such as ASD device failures, motor bearing and winding failure and voltage sags are reviewed along with existing solutions. The disadvantages of the existing solutions are discussed and a research objective is presented.

In section II, the proposed topology and its advantages are presented. The operation of the proposed topology is detailed for different operating modes. Section III presents an in-depth simulation based comparison of the common mode and differential mode performance of different modulation strategies. In section IV, the design of an 80 kW ASD is covered along with device ratings. The simulation and experimental results are presented to validate operation. In section V, conclusion and future work are discussed.

I.9. Conclusion

Motor drive systems are widely used in continuous process industry. Any interruption of manufacturing process, i.e. failure of motor drive system, has significant financial impact. Four different factors affecting availability of motor drive system: a) semiconductor failure, b) motor bearing failure, c) motor winding breakdown and d) voltage sags were reviewed and summarized. A detailed discussion on the existing solutions and their disadvantages was presented. The research objective and thesis organization were presented in the end.

II PROPOSED ADJUSTABLE SPEED DRIVE TOPOLOGY

The fault tolerant non-regenerative AC motor drive system proposed in this work is shown in Figure 15. The proposed topology is obtained after modifications to the conventional ASD topology. The topology consists of a three phase diode rectifier (*D1-D6*) and auxiliary diodes (*D7-D9*) followed by a 4-leg inverter ($S_{1A\text{-}D}$ and $S_{4A\text{-}D}$) along with isolation (T_{si} and $T_{fia\text{-}d}$) and reconfiguration (T_{sr} and $T_{fra\text{-}d}$) circuits for sag and fault mode operations. A current limiting resistor R_{fr} and a parallel relay S_{fr} are included as part of the fault reconfiguration circuit. An alternate topology is shown in Figure 16. In Figure 16, this current limiting function is performed by inductors ($L_{2a\text{-}d}$). In the following discussion, only topology shown in Figure 15 is described.

During normal operation the 4th leg, hereby know as auxiliary leg (S_{1D} and S_{4D}), is coupled to the conventional 3 phase inverter topology using the output filter. This auxiliary leg enables active common mode suppression by imposing a voltage at the inverter output which is equal but opposite to the common mode voltage magnitude. In case of grid phase voltage sag, this auxiliary leg (S_{1D} and S_{4D}) and diodes (*D7-D9*) form a boost converter to achieve sag compensation. For fault mode operation, this auxiliary leg replaces the faulty leg after hardware reconfiguration. The output filter on the inverter side smoothens out $\frac{dV}{dt}$ transitions which reduces voltage overshoots at motor terminals. Thus, the proposed system reduces vulnerability to device faults, bearing currents, winding breakdown and voltage sag.

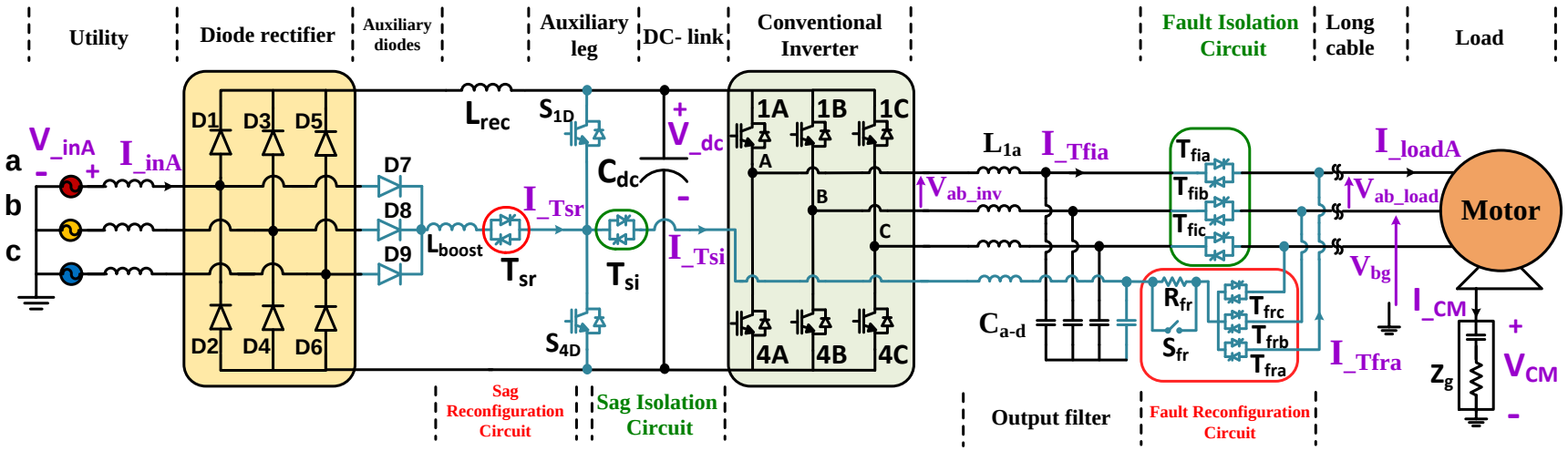

Figure 15.Proposed fault tolerant ASD topology with auxiliary leg (S_{1D},S_{4D}) and diodes (*D7, D8, D9*), isolation (T_{si}, T_{fia}, T_{fib}, T_{fic}) and reconfiguration (T_{sr}, T_{fra}, T_{frb}, T_{frc}, S_{fr}, R_{fr}) circuit

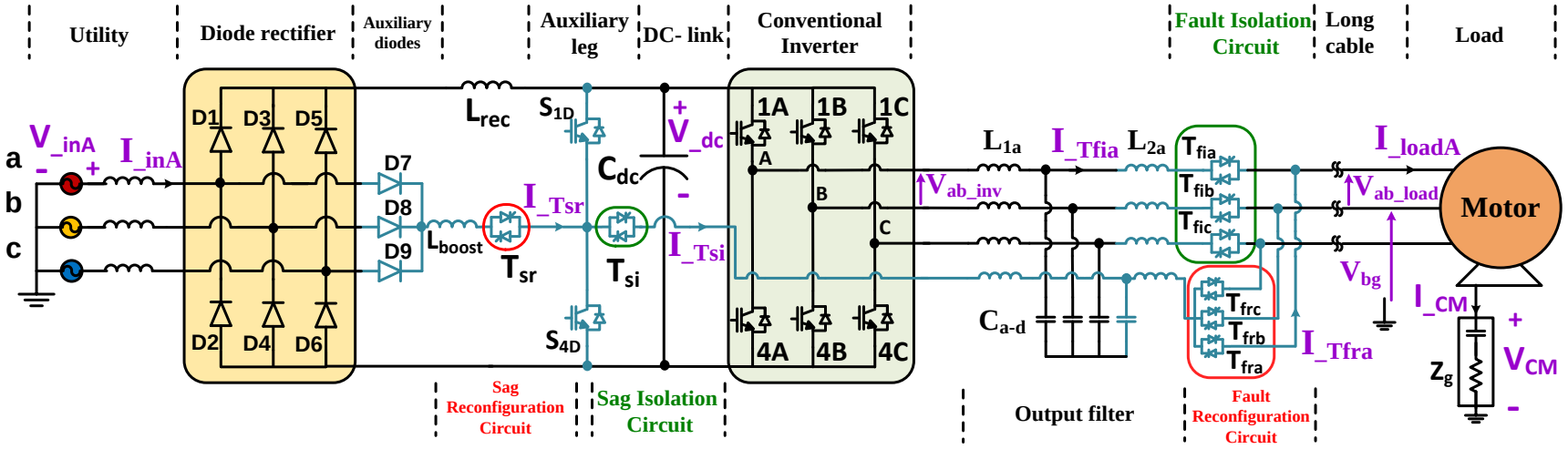

Figure 16. Alternate fault tolerant ASD topology with auxiliary leg (S_{1D},S_{4D}) and diodes (*D7*, *D8*, *D9*), isolation (T_{si}, T_{fia}, T_{fib}, T_{fic}) and reconfiguration (T_{sr}, T_{fra}, T_{frb}, T_{frc}) circuit

The system proposed in Figure 15 has various advantages:

- A single auxiliary half bridge (S_{1D} and S_{4D}) performs multiple tasks: (a) fault tolerance capability during open and short circuit device faults, i.e. S_{1D} and S_{4D} along with T_{si}, T_{fib}, T_{fic}, T_{fra}, S_{fr} (all ON assuming inverter phase A is faulty); (b) active common mode suppression during normal operation: i.e. with S_{1D} and S_{4D} along with T_{fia}, T_{fib}, T_{fic} and T_{si} (all ON) and (c) sag compensation during voltage sags: i.e. with S_{1D} and S_{4D} along with T_{sr}, T_{fia}, T_{fib}, T_{fic} (all ON).
- Modular design of proposed fault tolerant modifications and simple control strategy enables retro-fit capability.
- Use of anti-parallel thyristors/ triacs/ solid state relays allow fast and controlled system reconfiguration in case of faults and minimize conduction losses [51].
- Active common mode suppression reduces the size of the common mode filters.
- Operation at full load even under fault conditions.
- The inverter output filter reduces $\frac{dV}{dt}$ at motor terminals for long motor leads.

The design and operation of the proposed fault tolerant ASD topology is covered in this section, and may be best understood by studying it in three detailed sub-sections: (A) Fault mode operation, (B) Active Common Mode Suppression (ACMS) operation with modulation strategy and filter design, (C) Auxiliary Sag Compensation (ASC) operation with current shaping control strategy.

The state transition diagram for handover between different operating modes is shown in Figure 17. It is noted that in post fault or ASC operation, ACMS is unavailable. However, the fault tolerant ability helps in avoiding unplanned shutdowns.

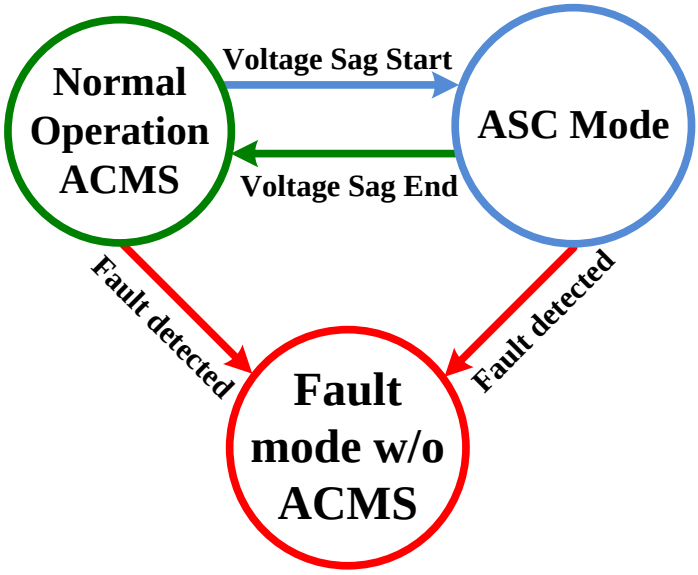

Figure 17. State transition diagram for different operating modes

It is noted that the isolation and reconfiguration circuit can consist of triacs/ anti-parallel thyristors/ solid state relays. The choice between these options is dependent on the power rating specifications. Triacs and solid state relays are typically available for lower power ratings than thyristors. For the following discussion, term "triac" is used exclusively instead of "triac/anti-parallel thyristors/ solid state relay". However, the discussion remains unchanged when anti-parallel thyristors or solid state relays are used in place of triacs.

II.1. Fault Mode Operation

As discussed before, different fault tolerant approaches are available in the literature. Each approach has its advantages and limitations. In this work, a phase redundant approach is adopted to achieve fault tolerant design. Although additional

switches add to the cost, phase redundant approach is superior to other approaches because of its full output voltage and current range. This means that the system can operate at full load even under fault condition. This is a valuable feature in critical applications for continuous process industry.

Fault tolerant capability is added to a conventional ASD topology by introducing a redundant auxiliary leg (S_{1A} and S_{1D}). This provides fault tolerance in case of open and short circuit failures of inverter IGBT and anti-parallel diode. However, failures in the inverter IGBTs and anti-parallel diodes - hereby called devices - are treated as the same in this discussion as they have similar effects on the inverter operation. A typical fault tolerant topology operates according to the flow chart Figure 18. Fault tolerant operation includes three distinct steps: (i) Fault isolation, (ii) Hardware reconfiguration, and (iii) Post fault control. As discussed later in this section, appropriate delays are inserted between these steps to avoid large overshoots in transients. The proposed topology implements these steps for both open and short circuit device failures.

Typical device open circuit fault detection time for a 3 phase inverter is in the order of milliseconds [33]. Most of the published methods rely on sensing inverter phase currents and their deviation from normal operation to detect open circuit faults. Recently, faster methods have been published which use V_{CE} voltage of the low side device to detect open circuit fault [52]. Other methods have also been published which utilize adaptive techniques to diagnose and identify faults [53]. Since the focus of this work is not fault diagnosis, the detection time for open circuit fault is taken to be 2 ms. For short circuit failure a detection time of 4 μs is used, as modern gate drives employ

schemes such as de-saturation protection which can complete fault detection in less than 5 μs [54]. Also the open circuit and short circuit faults are discussed for IGBT S_{1A} only, however the same discussion is applicable in case of other device failures.

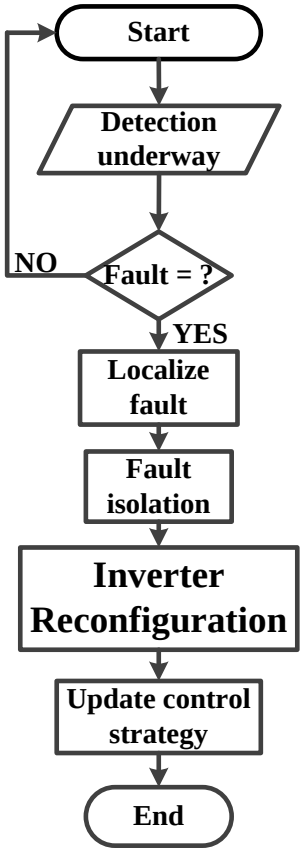

Figure 18. Inverter operation under fault condition

The topology schematic in Figure 15 has been simplified (Figure 19) for better understanding of failure mode operation of IGBT S_{1A}. The components added to a conventional topology are in blue color. First the open circuit device failure is discussed.

During normal operation triac T_{fia} (fault isolation for phase A) is normally turned on while T_{fra} (fault reconfiguration for phase A) and S_{fr} (reconfiguration relay) are normally OFF. When a fault is detected, T_{fia}, T_{fra}, S_{fr} and all the inverter switches are turned OFF. This is done to avoid any catastrophic transients. After a preset wait time of a few microseconds T_{fra} is turned ON, and the gating signals of S_{1A} and S_{4A} are applied to S_{1D} and S_{4D} respectively. The reconfiguration relay S_{fr} is turned ON after a short delay (40 µs) following turn ON of T_{fra}. This completes reconfiguration and update of control strategy. The control of healthy legs (B and C) in post fault operation is unaltered.

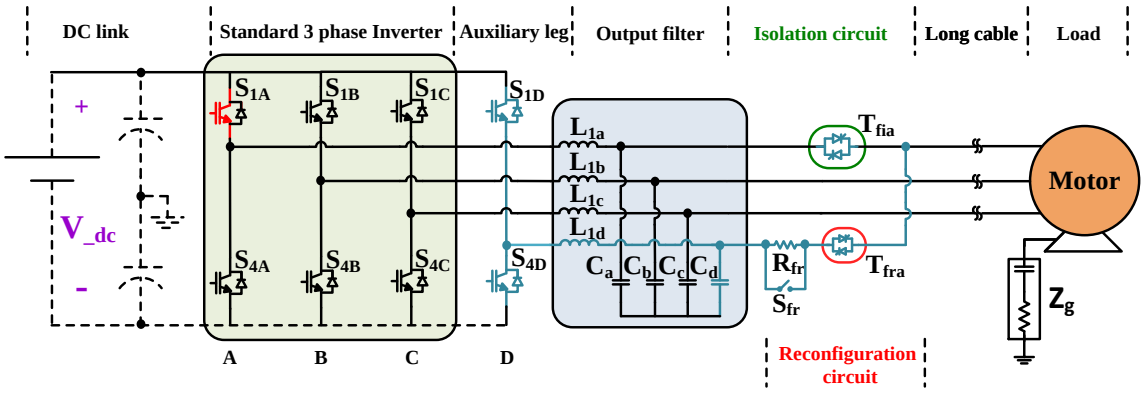

Figure 19. Simplified schematic of the proposed topology to illustrate inverter switch S_{1A} failure ride-through

The operation under short circuit failure is similar to the above discussion, except for the fault detection time. As discussed before, the detection time for short circuit faults is 4 µs. Once short circuit failure is detected, the de-saturation protection turns off the S_{4A} immediately, and controller temporarily turns off all other switches. The

reconfiguration and post fault control strategy is same as the open circuit failure case. The operation in fault mode is summarized in the form of a flow chart in Figure 20.

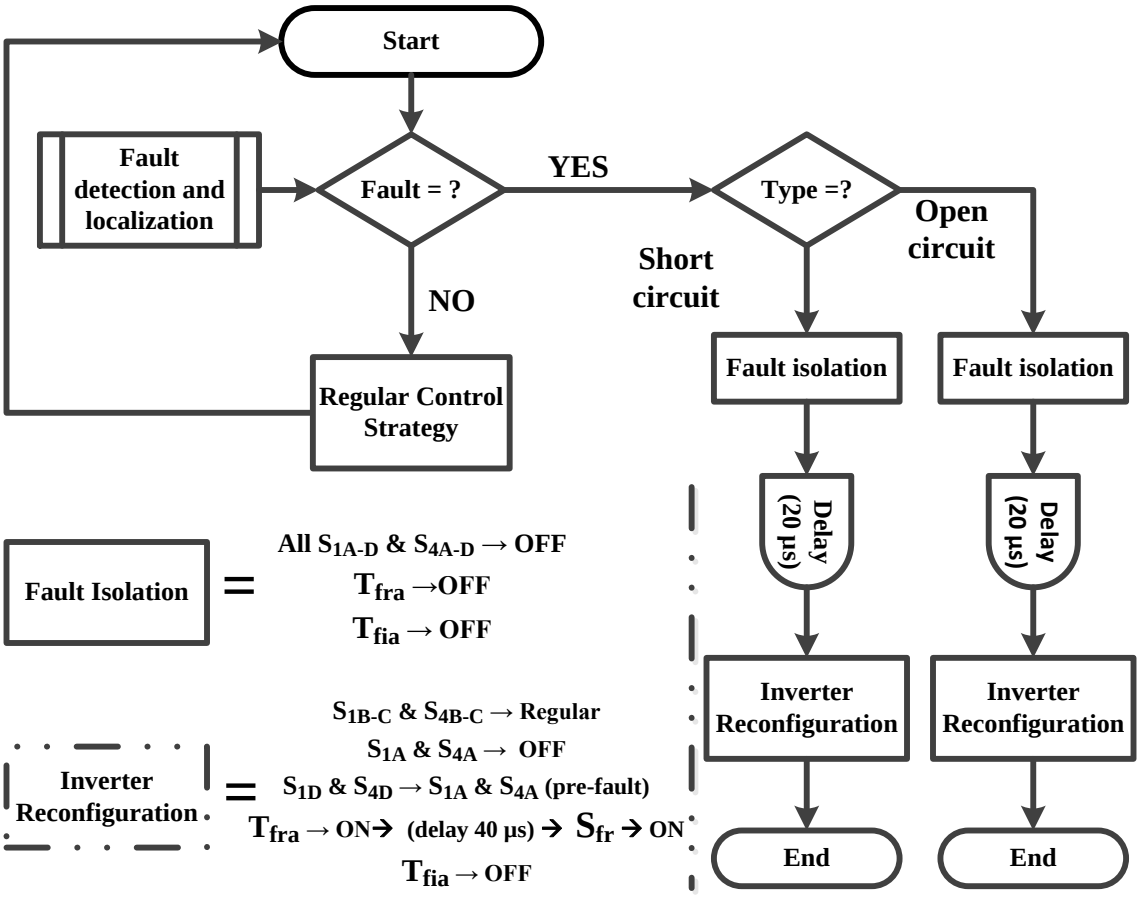

Figure 20. Control flow chart for isolation and reconfiguration strategy in open and short circuit fault condition

The other semiconductor devices present in the drive are front-end rectifier diodes. The proposed topology can handle both short circuit and open circuit rectifier diode failures after employing appropriate derating and fault isolation scheme. The

principle of fault isolation, hardware reconfiguration and control update discussed for the inverter can be utilized.

Rectifier diode open and short circuit faults also require intelligent fault isolation schemes. In open circuit failure, a dc current is drawn by the faulted rectifier phase. This is usually undesirable. So a dc current triggered relay can be used to isolate the faulted phase.

In case of a short circuit failure, a more complex fault isolation scheme is required to successfully detect and isolate a fault. The two isolation schemes are shown in Figure 21. In Figure 21 (a)-(c), fuses are proposed to be used to isolate fault. As shown in [11], using fuses to isolate diode short circuit failure is not a reliable isolation strategy. In case of a fault, more than one fuse can blow and will result in drive trip. Another isolation strategy proposed in Figure 21 (d)-(f) uses circuit breaker/ relays to isolate the faulted phase intelligently. This strategy assumes successful detection and localization of short circuit fault using techniques like reverse current detection [55]. When the fault is detected, the faulted phase is disconnected.

As it is evident from the proposed topology (Figure 15), there is an asymmetry between top and bottom diode of a phase in terms of open circuit fault tolerance. A failure in one of the top diodes (*D1, D3, D5*), can be replaced respectively by (*D7, D8, D9*). This is done by turning ON T_{sr} and auxiliary leg and T_{si} being turned off, i.e. only body diodes are used. When an open circuit failure occurs in one of the bottom diodes (*D2, D4, D6*), such a replacement is not possible. After isolation of diode failure, the front end is reduced to a single phase diode rectifier. In this case as well as in case of

short circuit fault in any one of the diodes (*D1 – D6)*, the topology can be operated in auxiliary sag compensation (ASC) mode. This operation is discussed in section II.3. It is noted that appropriate device de-rating is required for operation of front end in single phase.

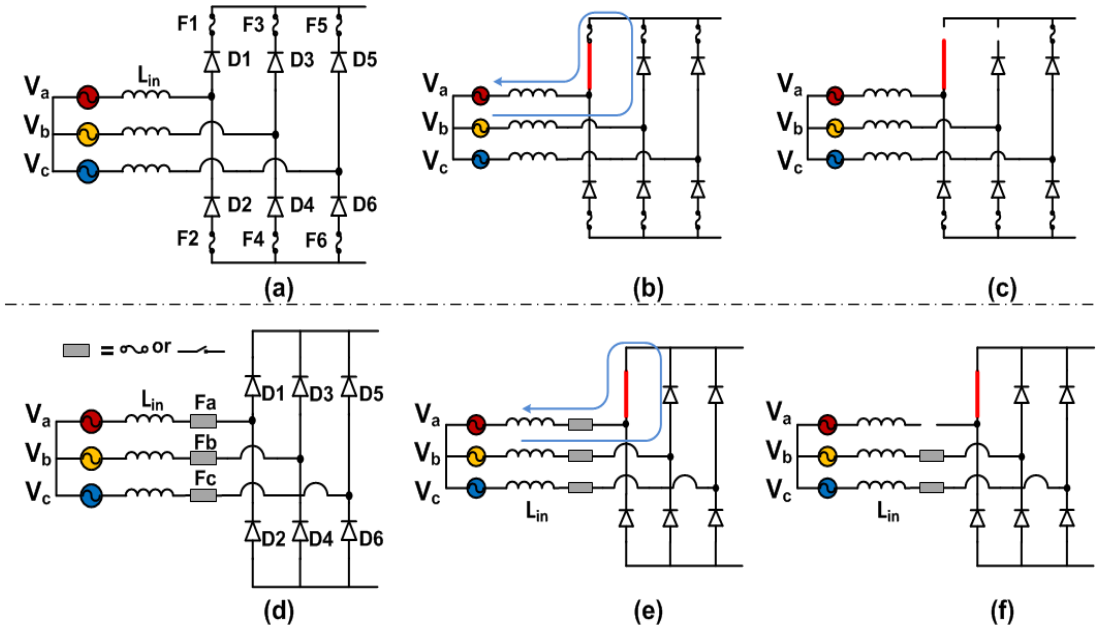

Figure 21. Operation of short circuit fault isolation schemes for rectifier diode,(a) – (c) uses fuses & (d) – (f) uses circuit breakers/relays

II.2. Active Common Mode Suppression Mode

In a conventional 3 phase sinusoidal PWM inverter (Figure 3), common mode voltages at the inverter output terminals exists due to two reasons. One source of common mode is the diode rectifier. The common mode voltage in the rectified voltage

shown in Figure 3 can be given by (2). The simulation waveforms confirming this are shown in Figure 22.

$$V_{\_cm,rec} = \frac{V_{\_top} + V_{\_bot}}{2} \tag{2}$$

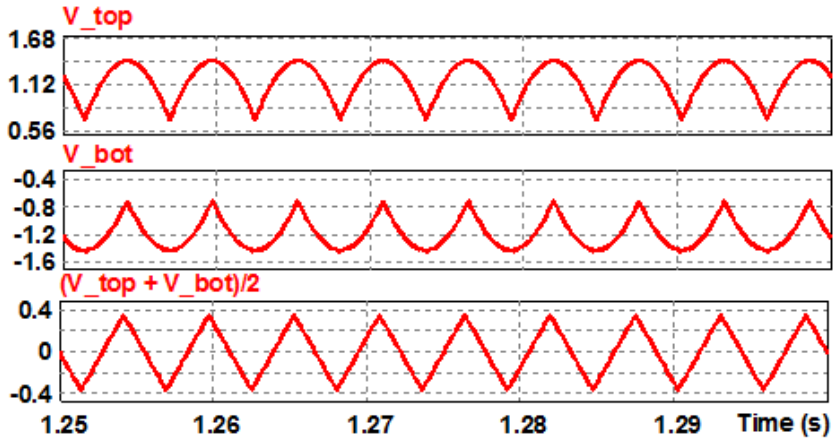

Figure 22. Common mode voltage at the diode rectifier output

The analytical expression [56] of this common mode voltage can be written as (3).

$$V_{\_cm} = \frac{3\sqrt{2}}{8\pi} V_{l-l,rms} \cdot \sin(3\omega t) + \frac{3\sqrt{2}}{80\pi} V_{l-l,rms} \cdot \sin(9\omega t) + \ldots \tag{3}$$

The second source of common mode is the switching pattern of the inverter. In a conventional 3 phase sinusoidal PWM inverter, three switches are ON at any time. This

leads to a common mode voltage on the output terminals at each time instant. With an even number of legs and with an appropriate switching strategy, it is possible to ensure that an equal number of output terminals are connected to positive and negative of the DC bus. So if higher order effects like dead-time and DC ripple are neglected, the common mode voltage on the output terminals is zero at each instant. The common mode suppression scheme proposed in [46] is based on this principle. This technique is utilized in the proposed topology. It is noted that the output CM voltage will have a beat frequency because of the difference in the triplen frequency harmonics of input supply and inverter output (if inverter modulation scheme introduces 3rd harmonic).

II.2.1. Modulation strategy

Different modulation schemes have been proposed to improve the common mode performance of 3 phase voltage source inverters [57-60]. The modulation strategy used in this paper is referred to as Active Zero State PWM (AZSPWM). In AZSPWM strategy (Figure 23) zero states of a conventional space vector PWM are replaced with the next nearest vectors [61, 62]. AZSPWM contains third harmonic component of the output fundamental frequency which introduces common mode voltage on the output terminals, however this low frequency component has minimal effect on common mode current. This generates the gating signals for three inverter legs. In order to cancel out the common mode voltage generated by AZPWM [46], the gating signals for S_{1D} and S_{4D} are generated using logic equation given in (4). This ensures that equal numbers of inverter output terminals are connected to positive and negative DC rails.

$$S_{1D} = S_{1A} \oplus S_{1B} \oplus S_{1C} \tag{4}$$

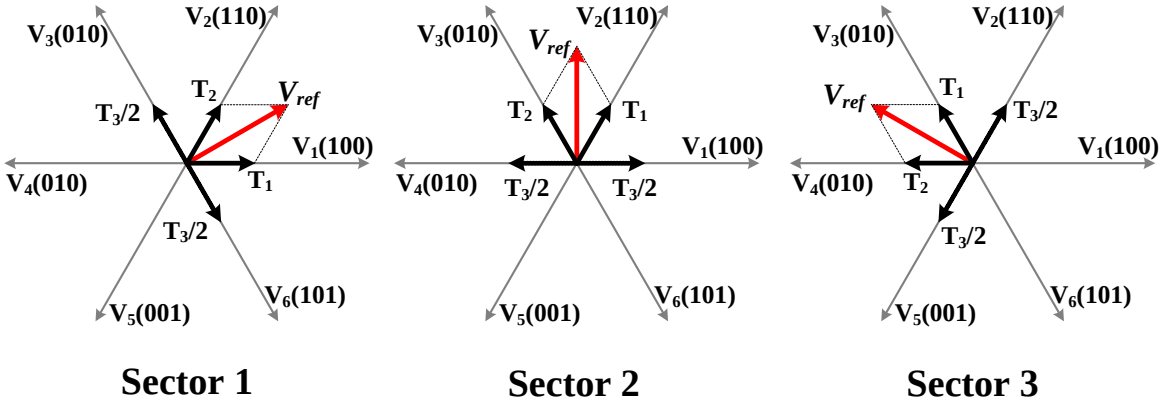

Figure 23. Modulation strategy (AZSPWM) in sector 1-3 (Sectors 4,5 and 6 are not shown).

II.2.2. Inverter output filter

The auxiliary leg is coupled to the 3 phase inverter by using an output filter shown in Figure 24. The output filter has two functions. Primary function of $L_{1a\text{-}d}$ and $C_{a\text{-}d}$ is to attenuate the switching frequency (f_{sw}) harmonics and suppress common mode voltage. As the higher frequency components are significantly attenuated, the effect of $\frac{dV}{dt}$ on motor terminals is minimized [25]. If all the inductors $L_{1a\text{-}d}$ (=L_f) and capacitors $C_{a\text{-}d}$ (=C_f) are identical, it can be shown by mathematical analysis that common mode voltages at the load neutral (V_{cm}) and is related to the filtered phase voltages [63]. The relationship is given in (5).

$$V_{cm} = \frac{4 \cdot (V_{an} + V_{bn} + V_{cn})}{3s^2 L_f C_g + 4(s^2 L_o C_g + s R_o C_g + 3)} \tag{5}$$

From (5), V_{cm} is dependent on the filtered phase voltages which are controlled. If the filtered voltages are balanced then $V_{cm} \rightarrow 0$. In order to achieve this, the switching frequency harmonics are filtered.

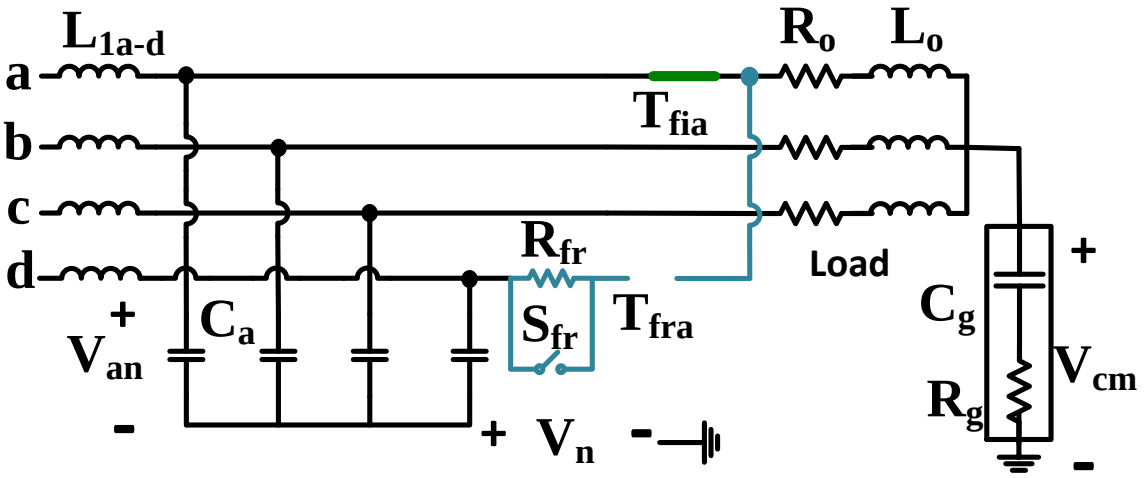

Figure 24. Inverter output filter structure

The modulation scheme has been analyzed for calculating ripple current (Figure 25). The I_{pk-pk} is maximum ripple when the volt-sec applied across the inductor L_f is maximum [64]. This occurs when reference vector (V_{ref}) is aligned with V_1, i.e. $T_2 = 0$.

Using the volt-sec balance principle, the peak to peak ripple current at switching frequency is given by (6).

$$I_{pk-pk} = \frac{d_0\, d_1\, V_{dc}}{2\, L_f\ f_{sw}} \tag{6}$$

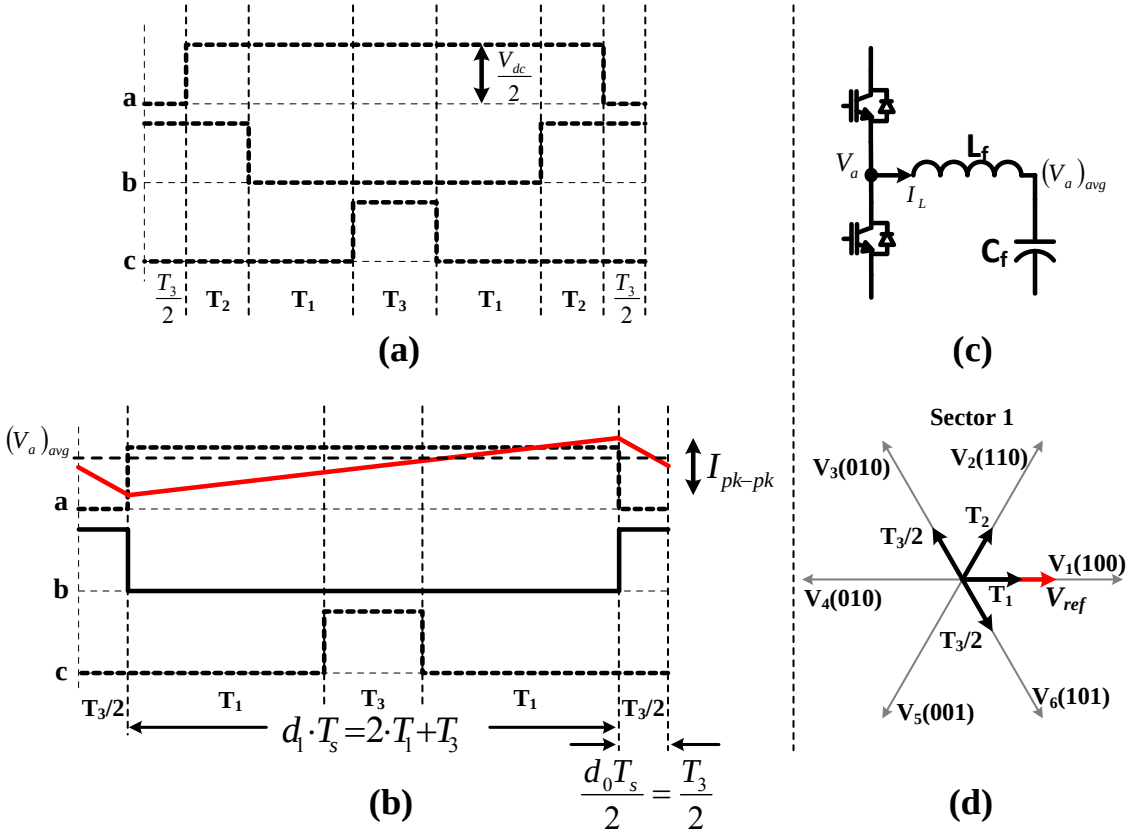

Figure 25. Ripple current analysis for AZSPWM modulation scheme (a) switching in sector 1, (b) switching sequence when reference vector is aligned to V_1, (c) half-bridge representation with filter components (d) reference vector (V_{ref}) aligned to V_1

When the reference vector is aligned with V_1 and modulation index is maximum i.e. 1.15, then d_0 and d_1 are given by (7) and (8).

$$d_1 = 2 * \left(\frac{0.866}{2} * \frac{sin(60° - 0°)}{sin\ 60°} \right) + \left(\frac{1}{2} - \frac{0.866}{2} * \frac{sin(60° - 0°)}{sin\ 60°} \right) \tag{7}$$

$$d_0 = \left(\frac{1}{2} - \frac{0.866}{2} * \frac{sin(60° - 0°)}{sin\ 60°} \right) \tag{8}$$

In order to attenuate switching frequency (f_{sw}) harmonics, the value of filter components are chosen using (9).

$$\frac{1}{2\pi\sqrt{L_f\ C_f}} \leq \frac{2 \cdot f_{sw}}{3} \tag{9}$$

A larger value of filter elements (lower value of cut-off frequency) can be chosen. Another factor to consider while designing the filter is the damping coefficient. The damping coefficient for series RLC circuit is given by (10). The value of R_{damp} (series damping resistor for C_f) is chosen to minimize overshoot and power loss.

$$\zeta = \frac{R_{damp}}{2}\sqrt{\frac{C_f}{L_f}} \tag{10}$$

The second function of the filter is to limit the current flow between two filter capacitors during transients. In case of a fault in S_{1A}, during reconfiguration T_{fia} and T_{fra} are both ON for a brief period. Charge exchange between the faulty phase capacitor (C_a) and healthy auxiliary phase capacitor (C_d) takes place and resistor R_{fr} limits this current transient. The worst case voltage difference between the two filter capacitors (V_{dc}) is used to choose the resistor value (R_{fr}) for limiting this current transient (11).

$$R_{fr} \cdot I = V_{dc} \tag{11}$$

The power loss in resistor R_{fr} is not significant as it only conducts for a very short time, effectively the time taken by the relay to turn ON. In order to dampen out resonances in the filter, additional RC damping elements can be added in parallel with the filter inductors ($L_{1a\text{-}d}$). The resistance and capacitor values are determined to minimize power loss and maximize damping near resonant frequencies.

II.3. Auxiliary Sag Compensation

In the proposed topology, sag ride through is achieved by integrating a boost converter in a conventional ASD topology [13]. For better understanding of ASC

operation, the proposed topology is simplified (Figure 26) to illustrate sag compensation. The components (in blue) added to implement ride through are 3 auxiliary diodes (*D7*, *D8*, *D9*), 2 triacs (T_{si} and T_{sr}) and boost inductor. The sag isolation triac (T_{si}) disconnects the auxiliary leg from output filter. Sag reconfiguration triac (T_{sr}) enables boost converter operation by connecting the auxiliary diodes to the mid-point of the auxiliary leg.

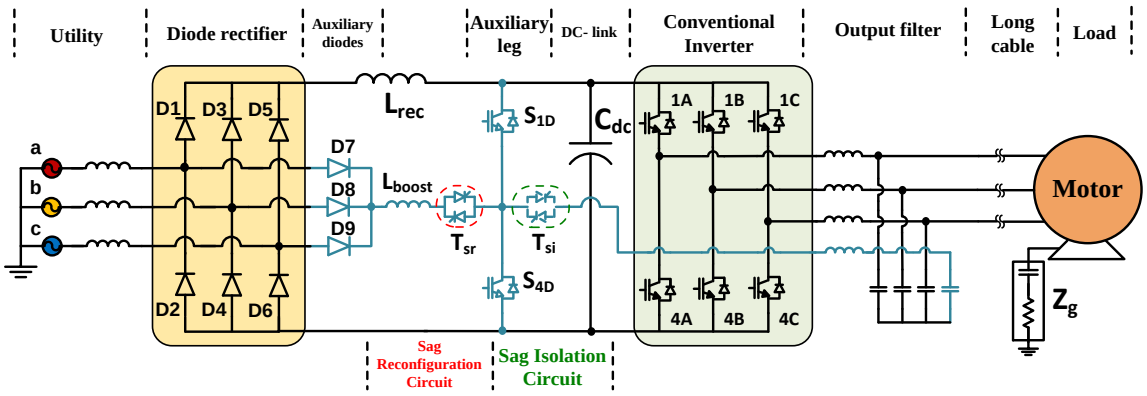

Figure 26. Proposed topology simplified to emphasize sag compensation mode of operation. Components added for sag mode operation are highlighted in blue.

Input line voltages are continuously monitored for detecting voltage sag. When voltage sag is detected, T_{si} is turned OFF and T_{sr} is turned ON. The front end circuit is now reconfigured with two possible paths. In addition to the regular path through *D1*, *D3* and *D5*, a secondary path is established through the integrated boost converter consisting of *D7*, *D8*, *D9*, boost inductor (L_{boost}), T_{sr}, S_{1D} and S_{4D}. This second path is operated as a boost converter in continuous conduction mode to draw current during the voltage sag. When the input voltage returns to nominal level, the isolation triac (T_{si}) and

reconfiguration triac (T_{sr}) are turned OFF along with the auxiliary leg (S_{1D} and S_{4D}) for few hundreds of milliseconds (0.1-0.2 s). This is done to let the current in the boost inductor to decay down to zero before the auxiliary leg returns to ACMS mode of operation.

The boost inductor is designed using (12) to limit the inrush current. V_{sag} is the input voltage when sag occurs, D is the duty cycle and T_S is the switching time period.

$$V_{sag} = L_{boost} \cdot \frac{\Delta I}{D \cdot T_S} \tag{12}$$

The final inductor value (L_{boost}) is adjusted to limit the current ripple to limit the input current during sag mode operation.

A current shaping control strategy (Figure 27) is proposed for the ASC mode operation. This current shaping is similar to the conventional power factor correction technique where boost inductor current is shaped. The conventional voltage and current control loops with PI controller are used. The reference dc bus voltage ($V_{\_dcref}$) is compared with the sensed dc bus voltage ($V_{\_dc}$). This error is the input to a PI controller which generates a scaling factor. The reference current shape $\overline{V_{rect}}$ is obtained from the ASC rectified voltage (V_{rect}) as shown in Figure 27. $\overline{V_{rect}}$ represents the required boost inductor current shape behavior, i.e. when the voltage is low the boost current should be higher and vice-versa. The boost inductor operates in continuous conduction mode. This

shape is scaled to obtain the reference current. This reference is compared with I_{boost} to generate error signal which is the input to a PI controller. The output of the PI controller is the duty cycle of S_{4D}. The voltage $V_{\_dcref}$ is chosen to be higher than dc bus voltage under normal operation. This helps to reduce the input currents during transients as well as during ASC mode operation and enables lower device ratings.

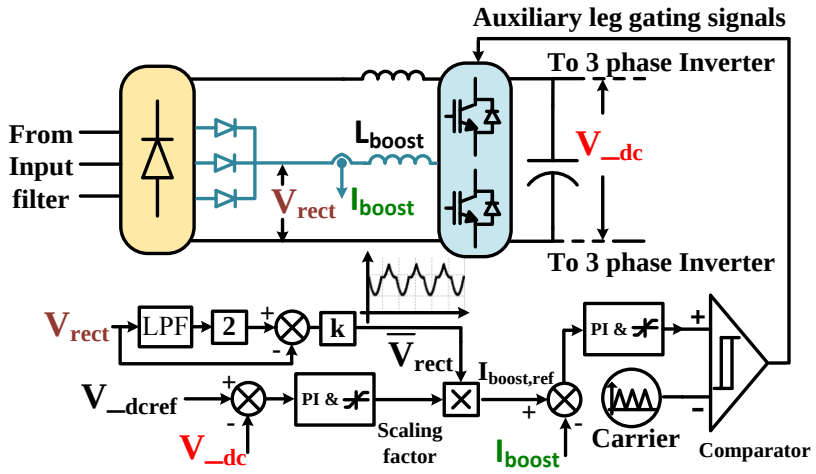

Figure 27. Current shaping based control strategy for auxiliary sag compensation mode operation

II.4. Conclusion

A fault tolerant adjustable speed drive topology was described in this section. The operation of the proposed topology was discussed for different modes a) Fault mode, b) Active Common Mode Suppression, and c) Auxiliary Sag Compensation mode. During fault mode operation, auxiliary leg replaced the faulted leg. In normal operation, auxiliary leg was operated to suppress common mode voltage at the inverter

output. The output filter design was detailed. When voltage sag was detected, the auxiliary leg is reconfigured to form a boost converter to regulate the dc bus voltage. The current shaping control strategy was also discussed to control the boost inductor current to regulate the DC bus voltage at a reference value. A higher than nominal reference value was chosen for DC bus voltage to limit the input current transients.

III COMMON MODE AND DIFFERENTIAL MODE ANALYSIS

III.1. Introduction

A PWM based modulation strategies are widely used in modern adjustable speed drive inverters. Using a PWM scheme allows generation of variable output voltage and frequency. However, PWM techniques also introduce unwanted low and high frequency harmonics, and could result in higher stress on the switching devices. Various modulation schemes have been proposed for AC motor drive applications to optimize and shape the inverter output spectra. The differential and common mode performances of some of these modulation schemes have been studied in [57, 60-62, 65].

In this section, the differential and common mode performance of Active Zero State PWM strategy is compared with conventional Sine PWM (SPWM) and Space Vector Modulation (SVM) strategies for the proposed and conventional topology. The comparison is done based on the data obtained from simulations. A new figure of merit, Common Mode Distortion Ratio (CMDR), is introduced for comparing common mode performance of different modulation strategy in motor drive applications.

III.2. Differential Mode Analysis

The comparison of PWM techniques is presented in [66]. The first order distortion factor (DF_2) defined in (13), is used as a quality index to compare performance of different modulation strategies for ac motor drive application.

$$DF_2 = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2} \tag{13}$$

where V_1 is the fundamental voltage component of the line to line voltage, h is the harmonic order (fundamental = 60 Hz) and V_h is the line to line voltage harmonics. DF_2 is a representation of harmonic current in an AC motor drive application. The differential mode line to line voltage harmonic distortions cause harmonic currents. The index DF_2 is defined to give a higher weightage to lower order harmonics, as lower order harmonics determine the torque ripple and cause motor heating. The higher order harmonic currents are attenuated because of the inductive nature of the load (by the leakage inductance of the motor). So to minimize the torque ripple and motor heating, a PWM strategy with lower DF_2 is chosen.

A simulation based comparison is carried out for differential mode harmonic quality of output line to line voltage of AZSPWM, SPWM and SVM strategies with varying modulation index (m). DF_2 is used as the quality index. As the differential mode performance remains unchanged between proposed 4-leg and conventional topology, a conventional 3-leg inverter topology (Figure 28) is used for this analysis. In all the simulations, the DC bus voltage is taken to be 2 p.u. and load is 1 Ω.

It is noted that the analysis done for a purely resistive load holds true for a load with power factor other than unity. This is the case for all three modulation schemes discussed. In all three modulation schemes, three switches are ON at any instant. As three switches are ON at all times, it provides a stiff inverter output voltage. This makes the

line to line output voltage harmonics independent of load power factor. Therefore, DF_2 variation is only studied with changing modulation index.

The modulation index parametric sweep is performed in PSIM® simulation software. The frequency domain data is exported to MATLAB® and DF_2 values are calculated for different modulation indices. The DF_2 values are calculated for SPWM, AZSPWM and SVM modulation strategies using the line to line voltages ($V_{\_ab}$).

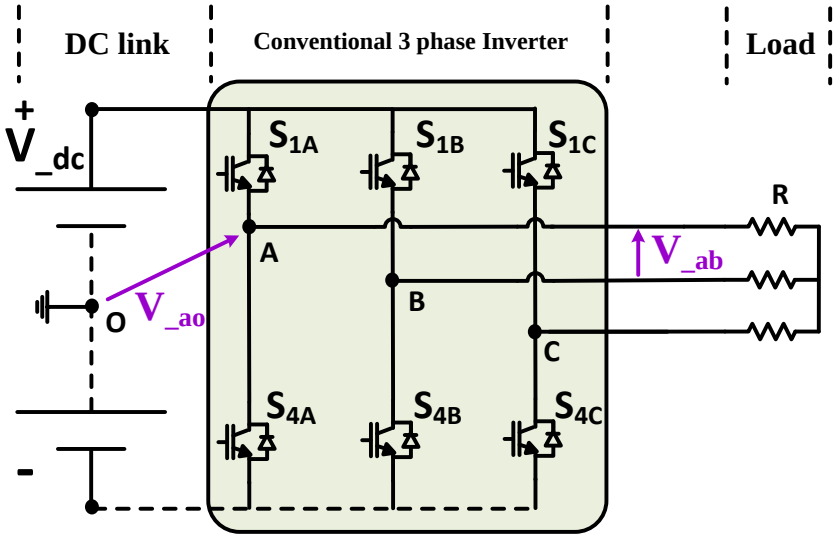

Figure 28. Schematic for simulation of differential mode analysis

The values of DF_2 are plotted against modulation index as shown in Figure 29. It is evident that the differential mode performance of the AZSPWM strategy degrades at lower modulation indices. This is expected because at low modulation index values the zero states are imposed for greater period of time. In SPWM and SVM, when zero state is applied to the inverter it imposes a line to line voltage of zero. However, when these

zero states are replaced with active zero states the line to line voltage is non-zero. So as the modulation index decreases, the switching frequency harmonics increase rapidly in AZSPWM strategy. It is noted that the proposed topology includes an output filter which will reduce the impact of this increased harmonic distortion. It is also observed that the distortion factor goes up in SPWM at modulation indices greater than unity. This is due to the fact that in over-modulation region, line to line voltage in SPWM strategy contains lower order harmonics (square wave harmonics:5^{th}, 7^{th}, 11^{th}, etc.) due to non-linearity. As the figure of merit, DF_2, gives higher weightage to lower order harmonics, the performance of SPWM degrades due to the introduction of lower order harmonics.

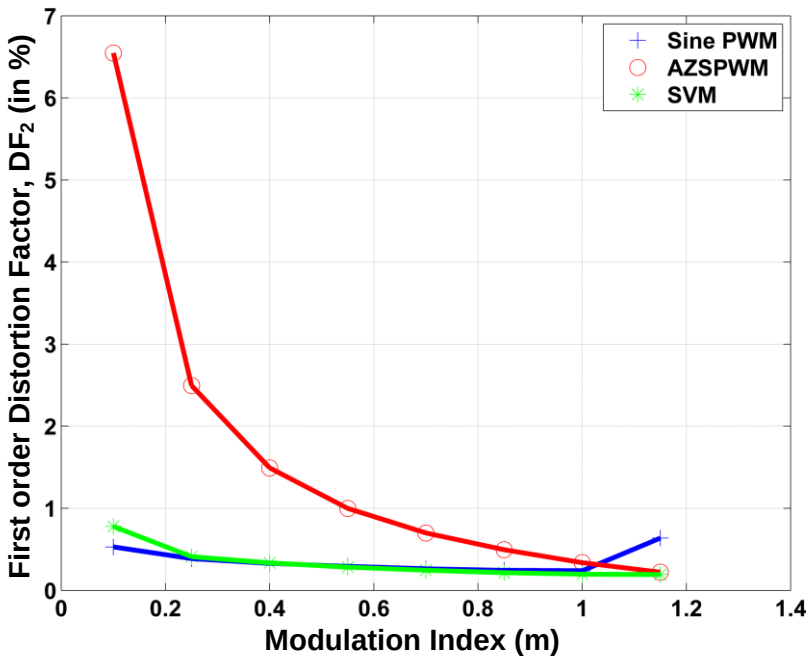

Figure 29. First order distortion factor (DF_2) plotted for variation in modulation index

III.3. Common Mode Analysis for 3-Leg and 4-Leg Topologies

AZSPWM strategy used in the proposed topology reduces common mode voltage significantly. In order to highlight this improvement, simulation based common mode analysis is done for sinusoidal PWM, AZSPWM & SVM with conventional 3-leg and proposed 4-leg inverter. The schematic used for simulation of 3 leg (components in black) and 4-leg (components in black and blue) inverter topology is shown in Figure 30.

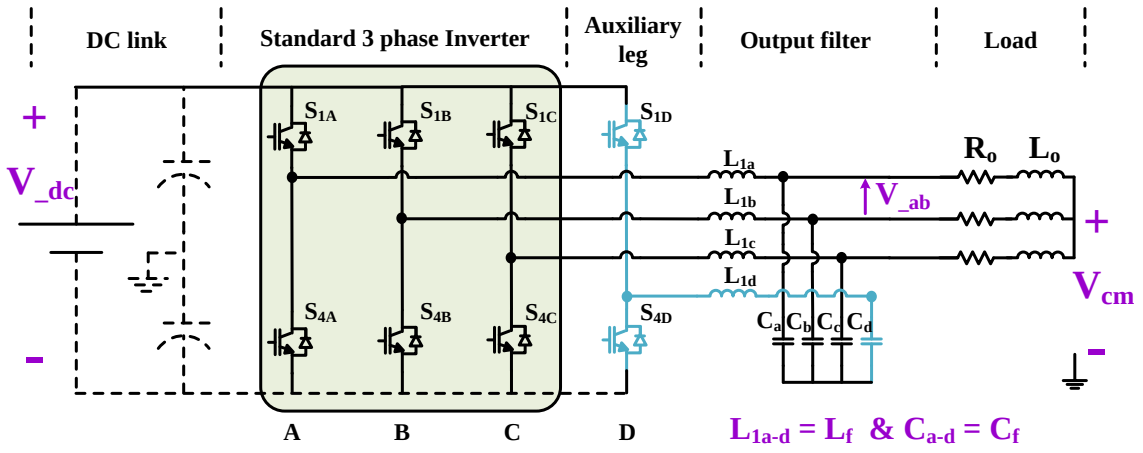

Figure 30. Schematic used for common mode analysis of 3 leg (components in black) and 4-leg (components in black and blue)

The system parameters are summarized in Table 5. The filter parameters are chosen to achieve output power and line to line voltage of 1.p.u.

Table 5. Simulation parameters for comparison between SPWM and AZSPWM

Simulation Parameter	Value	Simulation Parameter	Value
Output Power	1 p.u.	Load (R_o, L_o)	(0.81Ω, 1.04mH)
Load line to line voltage ($V_{\_ab}$)	1 p.u.	L_f, C_f	7uH,580uF
Load power factor	0.9	$V_{\_dc}$	1.633 (p.u.)

For modulation index=1, the common mode voltages of the studied 3-leg and 4-leg topologies are shown in Figure 31 to Figure 34. It is evident that common mode voltage is significantly reduced in both 3-leg and 4-leg topology for AZSPWM modulation. It is also observed that the higher order frequency content of the common mode voltage is reduced for AZSPWM. The frequency spectra for both topologies shown in Figure 32 and Figure 34 clearly illustrate this.

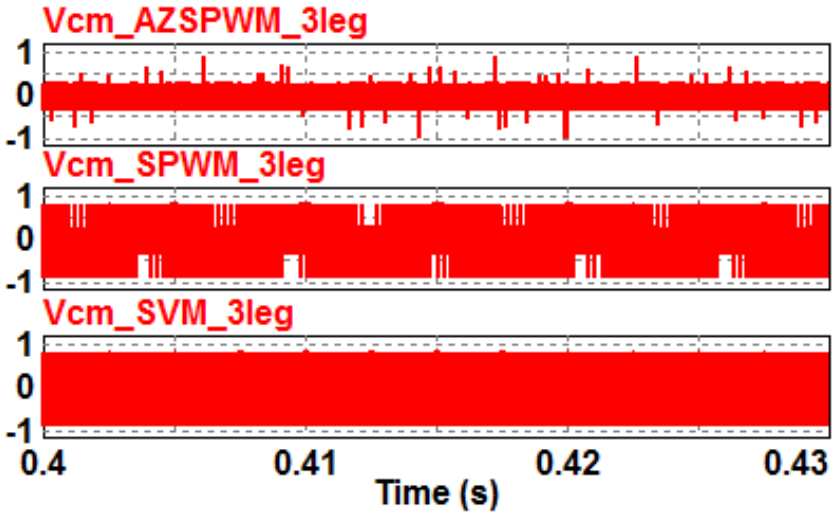

Figure 31. Comparison of common mode voltage for different modulation strategies (AZSPWM, SPWM, SVM) in 3-phase inverter topology

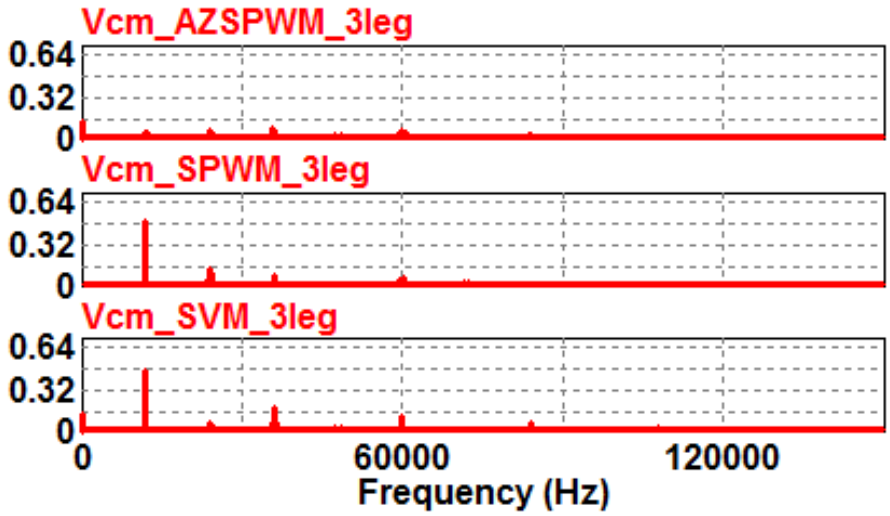

Figure 32. Comparison of common mode voltage FFT for different modulation strategies (AZPWM, SPWM, SVM) in 3 phase inverter topology

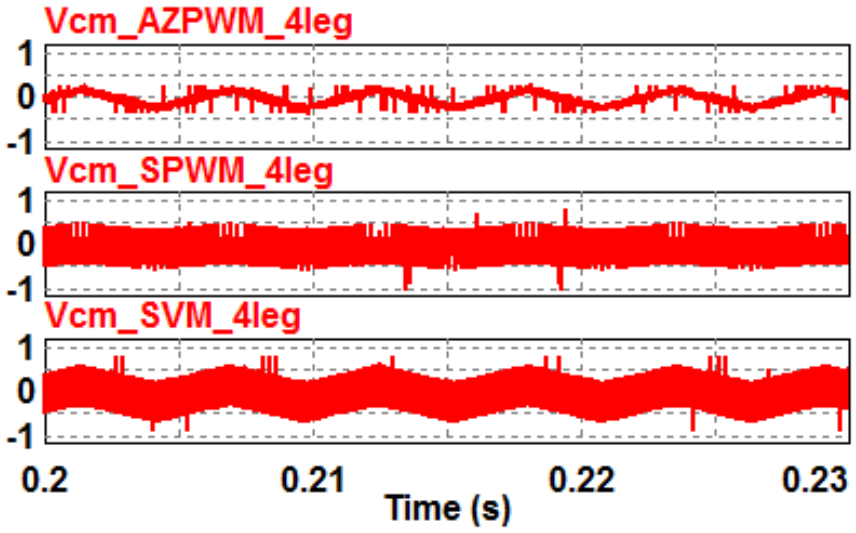

Figure 33. Comparison of common mode voltage for different modulation strategies (AZSPWM, SPWM, SVM) in 4-leg inverter topology

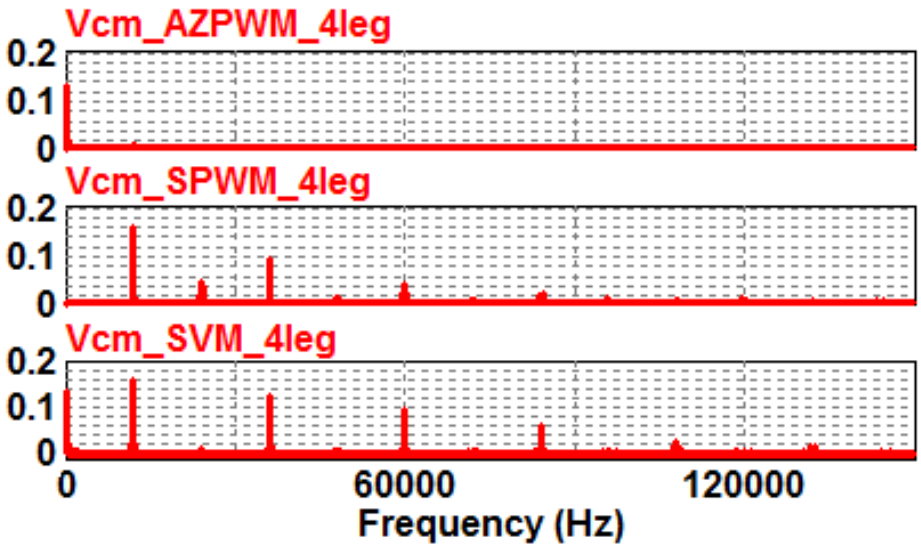

Figure 34. Comparison of common mode voltage FFT for different modulation strategies (AZPWM, SPWM, SVM) in 4-leg inverter topology

A new figure of merit called Common Mode Distortion Ratio (*CMDR*) is introduced to compare the common mode performance of these three modulation strategies. The *CMDR* (defined in (14)) is the square root of weighted sum of square of common mode voltage ($V_{cm,h}$) (including fundamental component ($h=1$), if present), normalized to fundamental component of differential mode line to line voltage ($V_{dm,1}$).

$$CMDR = \frac{1}{V_{dm,1}} \sqrt{\sum_{h=1}^{\infty} (h \cdot V_{cm,h})^2} \tag{14}$$

In motor drive applications, common mode voltage induces a common mode current through the ground coupling capacitor. In light of this fact, the proposed

definition is a measure of common mode current that will flow through a ground coupling capacitor when the common mode voltage is applied across the ground coupling capacitor. This definition is dual of the definition for first order distortion factor (DF_2) given in (13). As discussed earlier, DF_2 is used in evaluation of PWM strategies in ac motor drive applications (inductive load).

While DF_2 is the measure of harmonic phase current in the motor (similar to $\frac{V}{X_L}$), *CMDR* is the measure of common mode current (similar to $V \cdot X_C$) when a PWM strategy is applied to the inverter. The obtained quantity is normalized with respect to the fundamental component of differential mode line to line voltage (desired component of voltage).

For the same parameters given in Table 5, the variation of *CMDR* is plotted (Figure 35) with varying modulation index for sinusoidal PWM strategy in 3-leg and 4-leg inverter, SVM in 3-leg and 4-leg, and AZSPWM strategy in 3-leg and 4-leg inverter.

It is observed that the figure of merit *CMDR* is helpful to compare the performances of different modulation strategies and their effects on common mode currents. For better common mode current performance, a lower *CMDR* value is desirable. From Figure 35, it is also observed that 4-leg topologies are superior to 3-leg topologies for any modulation strategy for most of the modulation index range (>0.3). AZSPWM strategy when applied to 4-leg inverter topology yields the best performance. Another observation is that although from Figure 32 it can be concluded that the AZSPWM strategy is significantly better than SPWM and SVM for 3-leg topology, a

comparison of *CMDR* shows that the common mode current resulting from all the 3-leg modulation strategies are only marginally different. Also, it is observed that there is trade-off between the common mode and differential mode performance of different modulation schemes.

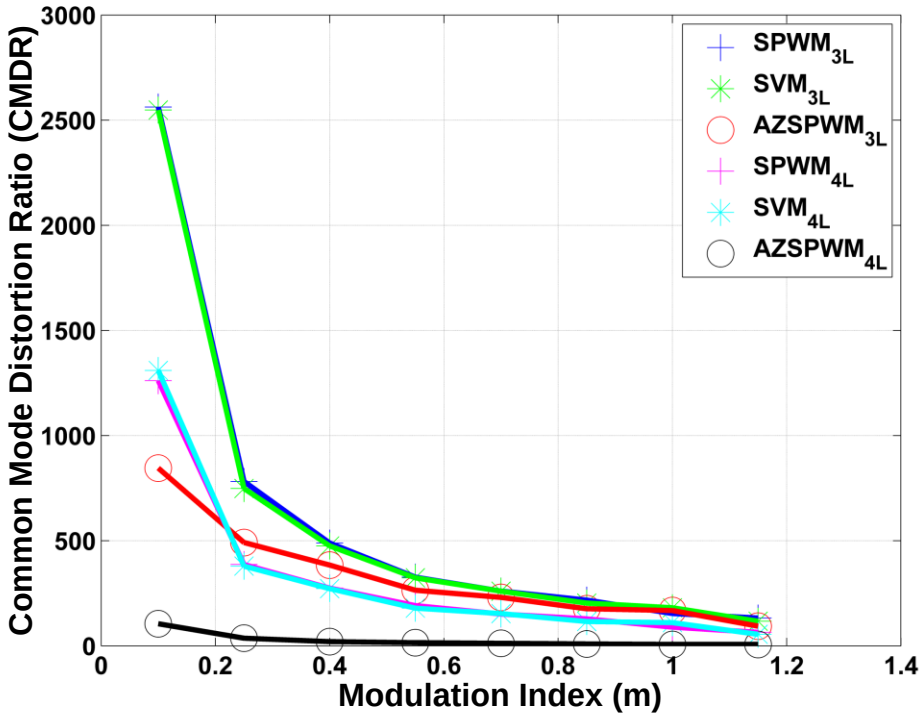

Figure 35. Common mode distortion ratio (*CMDR*) comparison for different modulation and topology combinations

III.4. Conclusion

A simulation based differential and common mode analysis was presented for three modulation schemes – Sinusoidal PWM (SPWM), Space Vector Modulation (SVM) and Active Zero State PWM (AZSPWM). The differential mode harmonic

quality index, first order distortion factor (DF_2) was used to compare differential mode performance of these modulation schemes. The variation of DF_2 was studied with changing modulation index and it was shown that for AZSPWM differential output line-line voltage harmonic distortion increases when modulation index decreases. However, the presence of output filter will mitigate the increase in harmonics. The common mode analysis was presented for the above three modulation schemes for both conventional 3-leg and proposed 4-leg inverter topology. A new figure of merit, Common Mode Distortion Ratio (*CMDR*), is introduced to compare the performance in different cases. The variation of *CMDR* is studied for changing modulation index. The obtained *CMDR* plots show that AZSPWM has superior performance when compared to SPWM and SVM over the entire modulation range.

The analysis in this section was used to understand the trade-off of differential and common mode performance for different modulation schemes. It was observed that none of the discussed modulation schemes preserved both differential and common mode performance throughout the modulation range. A trade-off between differential and common mode performance was observed.

IV DESIGN OF MOTOR DRIVE SYSTEM

IV.1. Design Example and Component Sizing

An 80 kW ASD system is designed for a 100 hp 3-phase induction machine. The motor parameters are summarized in Table 6.

Table 6. A 100 hp 3-phase induction machine parameters

Motor Parameter	Value	Motor Parameter	Value
Power (in hp)	100	r_r	0.015 (p.u.)
Stator line-line voltage	460 Vrms	X_{ls}	0.10 (p.u.)
Poles	4	X_{lr}	0.10 (p.u.)
Rated slip	0.0175	X_m	3.0 (p.u.)
r_s	0.010 (p.u.)		

The under-voltage lock out condition for the drive has been assumed to be 87% of the nominal dc bus voltage. The drive input overcurrent limit has been taken to be 2 times the peak unfiltered input current ($I_{\_inA}$) under regular operation. For the output current ($I_{\_loadA}$), an over current limit of 2 times the peak load current is set to avoid nuisance tripping during fault transients. The input voltage to the drive is 480 V (line-line rms) and dc link voltage ($V_{\_dc}$) is 650V. The values of different passive components are tabulated in Table 7. The DC bus capacitor (C_{dc}) has been overrated (50 μF/kW) to limit the input and output currents during faults. For Z_g, more details are provided in the section providing simulation results for common mode suppression (section IV.2.3).

Table 7. Passive component values selected for system simulation

Line side	Value	DC bus	Value	Motor side	Value
Z_{base}	3.1 Ω	Z_{base}	5.6 Ω	Z_{base}	2.8 Ω
L_{in}(60Hz)	0.2mH (2.5%)	L_{rec}	250 μH	$L_{1a\text{-}d}$ (60Hz)	160 μH (2%)
		C_{dc}	3.75mF	$C_{f\,a\text{-}d}$(60Hz)	2.5 μF
		L_{boost}	250 μH	R_{fr}	70 Ω

The ratings for various devices are summarized in Table 4. All the ratings are based on $I_{base,\,rms}$ = 90 A and V_{base} = 480 V. All devices have been de-rated accounting for increased current during full load operation under sag condition. The current rating for the boost inductor is not required to be 180 Arms because it only operates for a short time duration. However, it should be designed to avoid saturation.

Table 8. Summary of component voltage and current ratings

Device	Rating	Device	Rating	Device	Rating
Rectifier diode (*D1-D6*)	180 A_{rms} (2 p.u.) 1200 V(4.33 p.u.)	C_{dc}	1200 V (4.33 p.u.)	IGBT ($S_{1A\text{-}D}$ *to* $S_{4A\text{-}D}$)	1200 V (4.33 p.u.) 200 A_{rms} (2.22 p.u.)
Auxiliary diodes (*D7-D9*)	180 A_{rms} (2p.u.), 1200 V (4.33 p.u.)	T_{si}	200 A_{rms} (2.22 p.u.) 600V (2.22 p.u.)	L_{1a} *to* L_{1d}	200 A_{rms} (2.22 p.u.)
L_{boost}, L_{rec}	180 A_{rms} (2 p.u.)	T_{sr}	180 A_{rms} (2 p.u.) 600 V (2.16 p.u.)	C_{fa} *to* C_{fd}	≥600 V (2.16 p.u.) 40 A_{rms} (0.44 p.u.)
T_{fia} *to* T_{fid}	1200 V (4.33 p.u.) 200 A_{rms} (2.22 p.u.)	T_{fra} *to* T_{frd}	1200 V (4.33 p.u.) 200 A_{rms} (2.22 p.u.)	S_{fr}	1200 V (4.33 p.u.) 200 A_{rms} (2.22 p.u.)

The inverter switching frequency is 13 kHz and boost converter switching frequency is 10 kHz.

IV.2. Simulation Results

The proposed topology is simulated using PSIM® for 80 kW ASD system with the parameters in Table 6 and Table 7. This discussion is divided in four parts – (1) Fault mode operation, (2) Sag mode operation, (3) Common Mode Suppression (4) Long cable simulation. A description of current and voltage parameters, and device labels can be found in Figure 15.

IV.2.1. Fault mode operation

In open circuit fault, the time of occurrence of fault is important. Assume the load current (I) and load voltage (V) as in Figure 36. The load power factor is less than unity. This results in the following four distinct intervals:

1. t_1 → V is positive and I is negative
2. t_2 → V is positive and I is positive
3. t_3 → V is negative and I is positive
4. t_4 → V is negative and I is positive

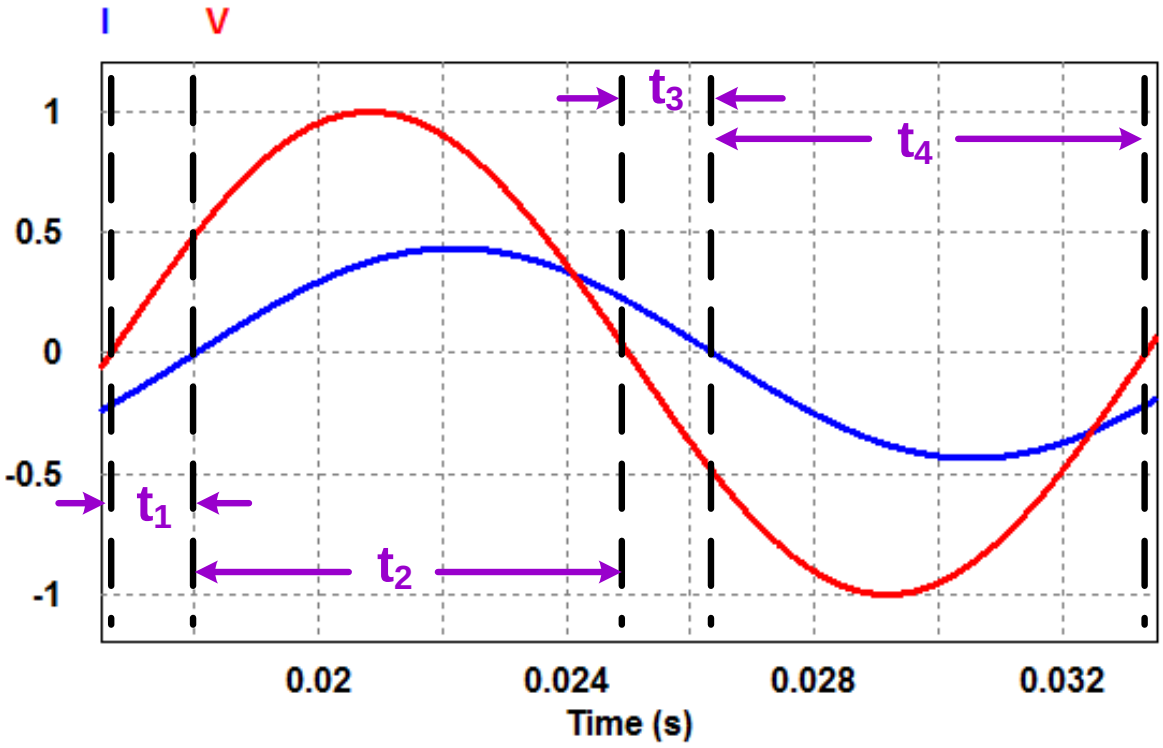

Figure 36. Load current (I) and load voltage (V) to highlight the importance of time of occurrence of fault

The current commutation in "just after" or $t = 0^+$ condition are shown in Figure 37. It is observed that path of the current is not affected if an open circuit S_{1A} fault occurs in intervals t_1, t_3 & t_4. For a fault in interval t_2, an immediate change is observed in the inverter output voltage, i.e. inverter output voltage goes to $V = -Vdc/2$ instead of $V = +Vdc/2$. This leads to rapid change in the load current. Hence for transients, this is the worst case scenario in case of an open circuit fault. In case of short circuit fault, the detection is fast so the transients are limited.

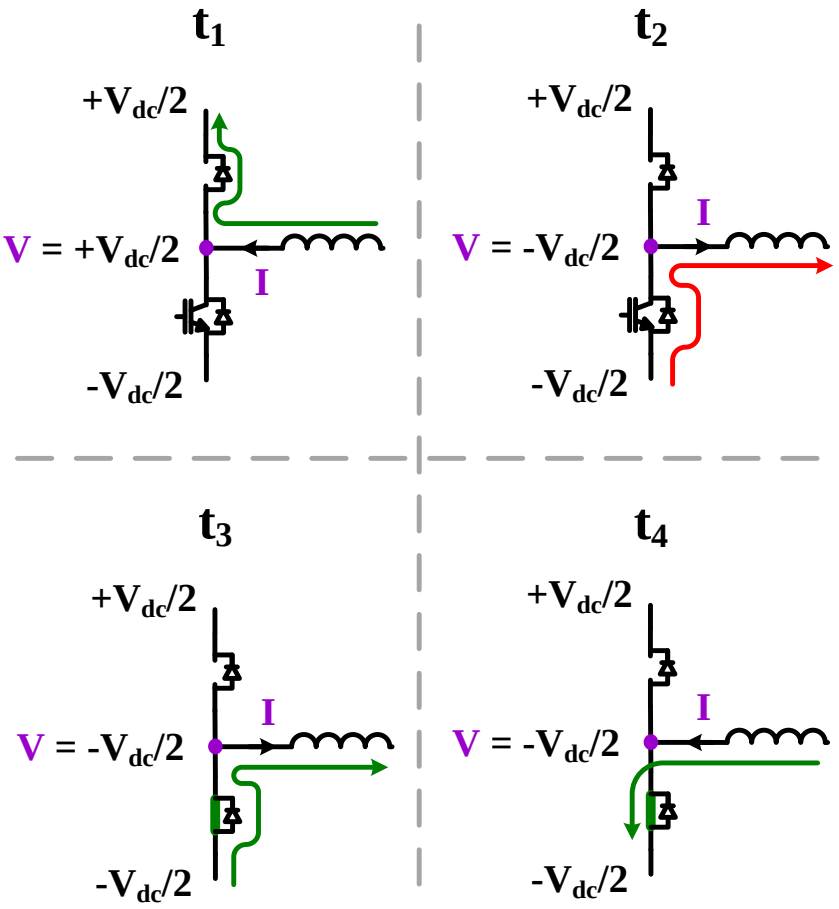

Figure 37. Post S_{1A} open circuit fault current commutation in different time of fault regions

The operation of the topology in fault mode is verified for the cases of open circuit fault in S_{1A} (Figure 38 and Figure 39) and short circuit fault in S_{1A} (Figure 40 and Figure 41). The rising edge of the "Fault" pulse in Figure 38 to Figure 41 indicates the start of fault. The falling edge shows the completion of detection. The transient waveforms illustrate that the overcurrent and under-voltage performance of the topology are within the defined specifications.

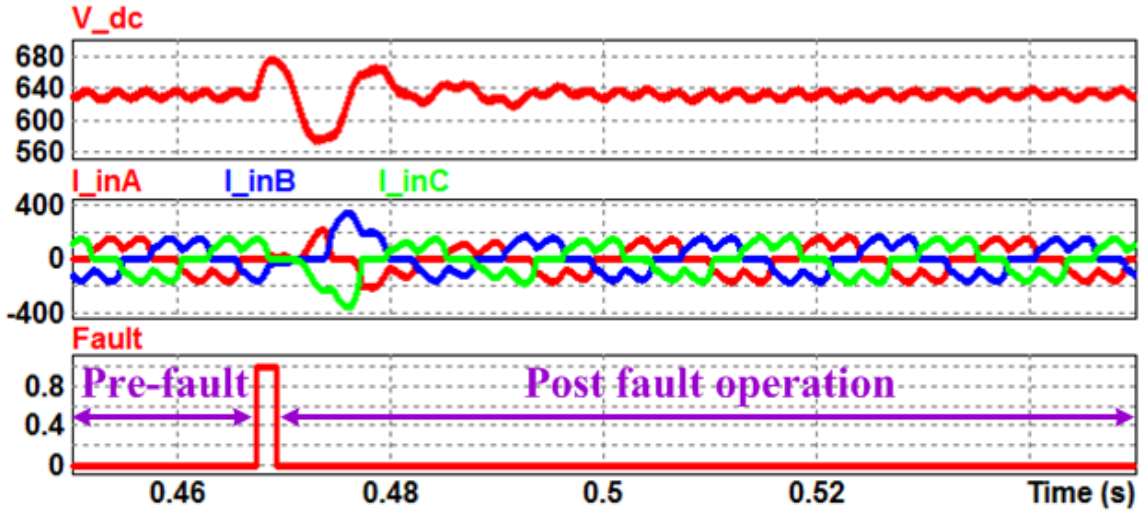

Figure 38. Operation under open circuit fault: DC bus voltage (volts), unfiltered input currents (amperes) and fault signal are shown

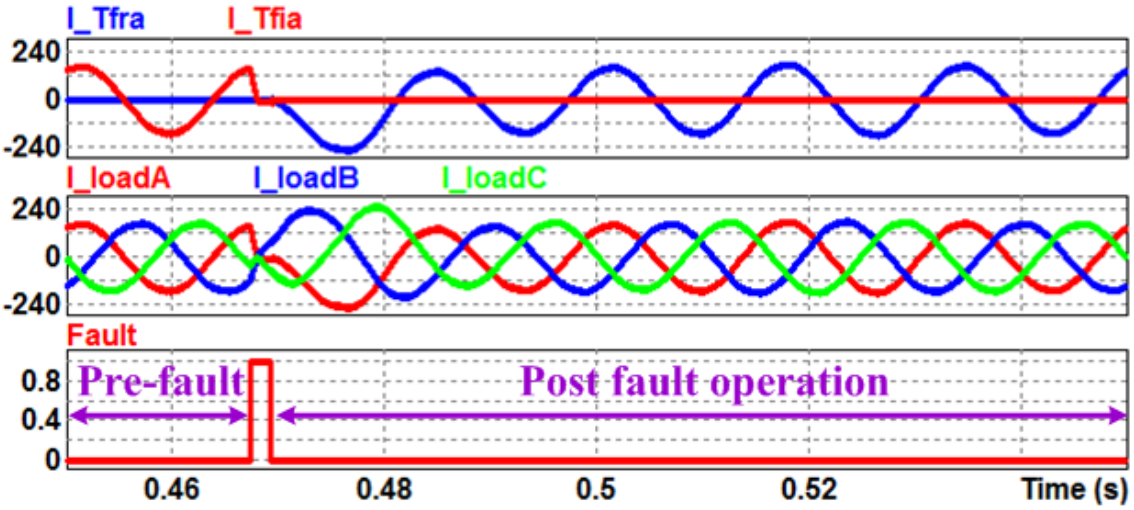

Figure 39. Operation under open circuit fault: isolation (T_{fia}) and reconfiguration (T_{fra}) triac currents (amperes), load currents (amperes) and fault signal are shown

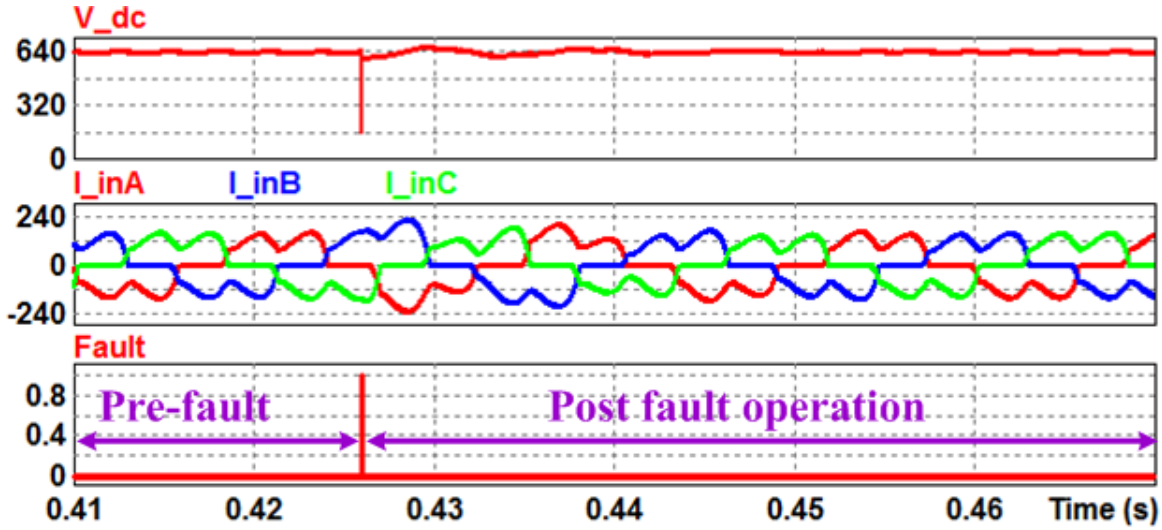

Figure 40. Operation under short circuit fault at t=0.4 s: DC bus voltage (volts), unfiltered line currents (amperes) and fault signals are shown

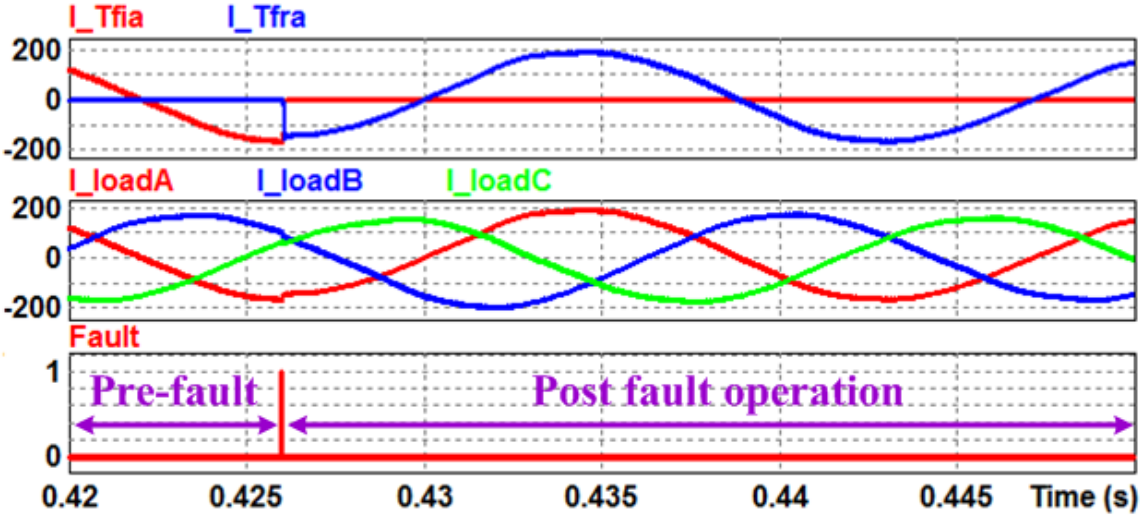

Figure 41. Operation under short circuit fault at t=0.4 s: isolation (T_{fia}) and reconfiguration (T_{fra}) triac current (amperes), load currents (amperes) and fault signal are shown

The detection times used for open circuit and short circuit fault simulations are 2 ms and 4 μs respectively. It is observed in Figure 40 that the DC bus voltage ($V_{\_dc}$) falls below the under-voltage limit during a short circuit fault transient. When the fault is detected, the gating signals to all the devices are turned off for a period of 20 μs. This period ensures that the controller can complete all diagnostic checks before returning to normal operation. It may be seen from Figure 40 and Figure 41 that following a fault, the ASD supplies nominal load current within two cycles (60Hz).

IV.2.2. ASC operation

The auxiliary sag compensation operation is studied for a phase to neutral sag to 50% and 500 ms long. When voltage sag is detected, the auxiliary leg and auxiliary diodes are reconfigured to form a boost converter which supplies the DC link capacitor. The boost converter operates at a switching frequency of 10 kHz. The transient performance in ASC operation is shown in Figure 42 to Figure 45.

At t= 0.25 s, input phase C-to-neutral voltage sags to 50% of nominal value and at t=0.75 s returns to nominal value. In sag compensation operation, the DC bus is regulated at 690V, i.e. approximately 9% higher than regular operation (635V). The DC voltage transients are limited within ±13% of the nominal value. A higher DC bus reference voltage is selected during sag to restrict the input and output current transients to within the overcurrent limit specified. It can be observed that the input current quality degrades during sag operation, but returns to normal under regular operation. It is to be noted that these currents discussed are un-filtered input currents and the grid-side filtered currents are expected to be of much better quality.

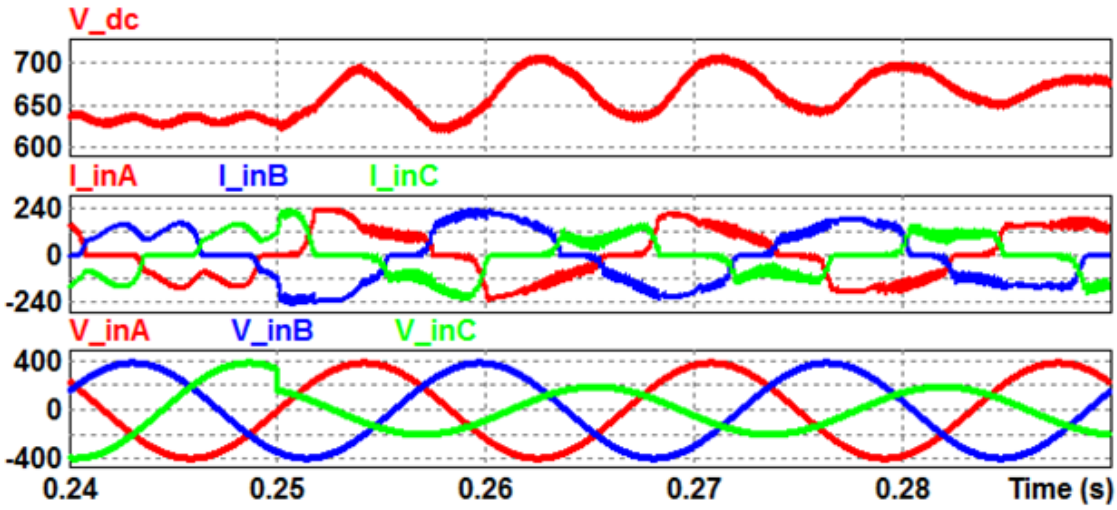

Figure 42. ASC operation with phase to neutral sag of phase C to 50% introduced at t= 0.25 s: DC bus voltage (volts), un-filtered drive input currents (amperes), line voltages (volts).

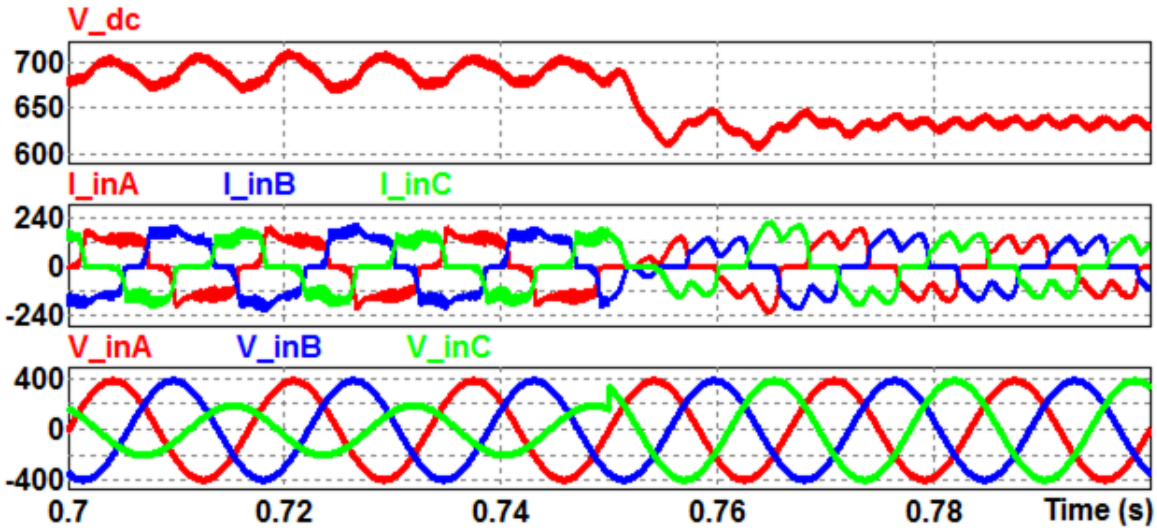

Figure 43. ASC operation with phase to neutral sag of phase C to 50% returning to normal operation at t=0.75 s: DC bus voltage (volts), un-filtered drive input currents (amperes) and line voltages (volts).

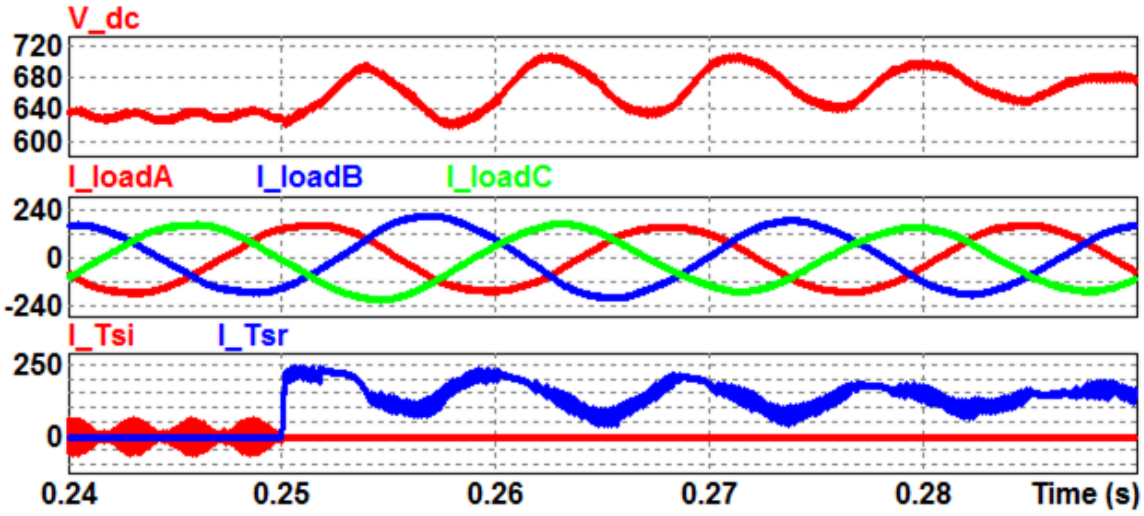

Figure 44. ASC operation with phase to neutral sag of phase C to 50% introduced at t = 0.25 s: DC bus voltage (volts), load currents (amperes), sag isolation (T_{si}) and reconfiguration (T_{sr}) triac currents (amperes).

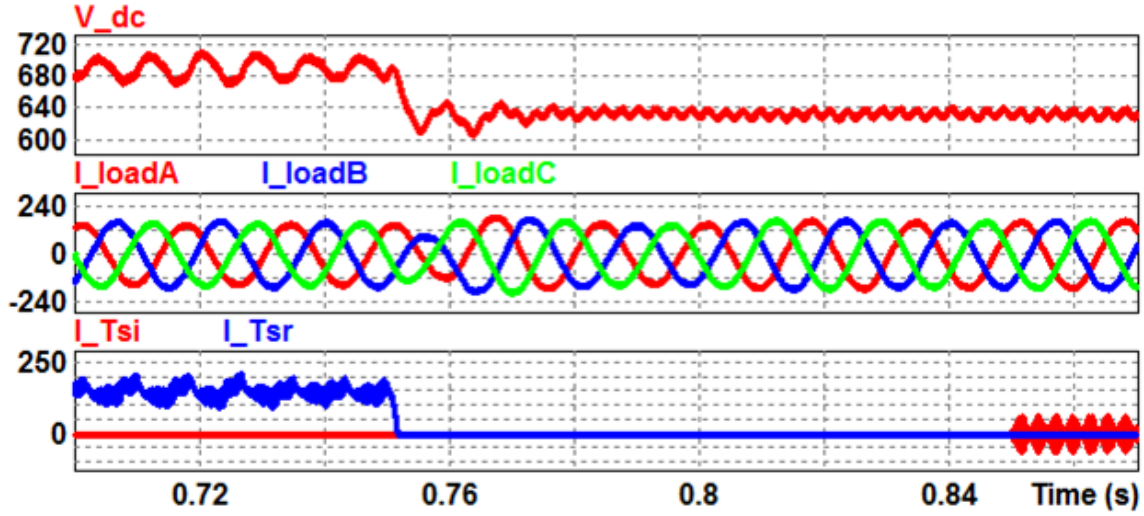

Figure 45. ASC operation with phase to neutral sag of phase C to 50% returning to normal operation at t=0.75 s: DC bus voltage (volts), load currents (amperes), sag isolation (T_{si}) and reconfiguration (T_{sr}) triac currents (amperes).

The current through the sag isolation triac T_{si} (Figure 45) shows a blanking period before returning to normal operation. This blanking time ensures that the boost inductor current decays to zero before returning to normal operation.

IV.2.3. ACMS mode operation

The different parasitic coupling capacitors in the motor were discussed earlier in section I.4. In this work, the bearing current is modeled using a model discussed in [67]. The discharge events are modeled by using a DIAC with breakdown voltage of 30 V. The model used for simulation is shown in Figure 46. The values of parasitic coupling capacitors are obtained for a 100 hp machine from the graph given in [68]. The values are summarized in Table 9. A small series resistance (≈ 10Ω) is added to each parasitic capacitor.

Table 9. Parasitic coupling capacitors for 100 hp motor

Parasitic Capacitor	**Value (in pF)**
C_{sf}	11000
C_{sr}	110
C_{rf}	1100
C_b	110

The state transition diagram discussed in Figure 17 illustrated that the ACMS mode is the normal mode of operation in the absence of sags and faults. Figure 47 shows the common mode current and voltage in normal and fault mode operations. It may be seen

from the voltage waveform that ACMS system, under normal operation, attenuates switching frequency harmonics in the common mode voltage.

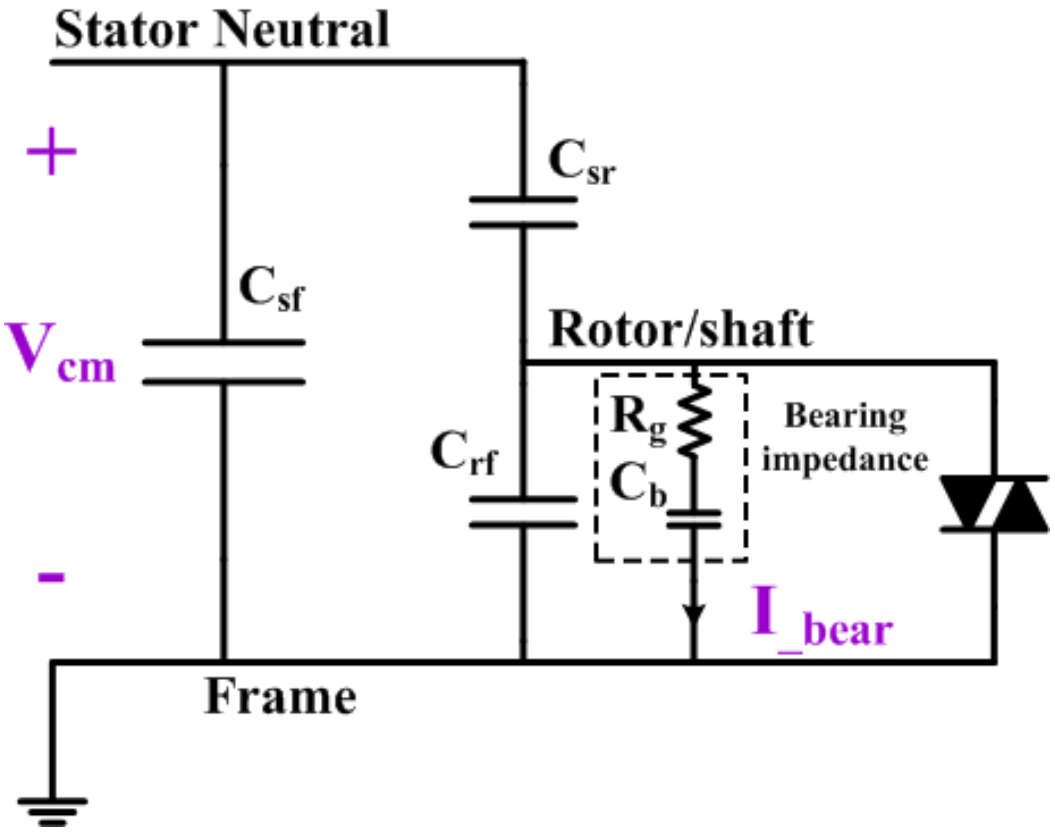

Figure 46. Modeling bearing discharge currents

The normal and post fault common mode current and voltage performances may be compared in Figure 48 and Figure 49. The common mode performance degrades in post fault operation, i.e. a number of discharge events are observed. It is observed that high frequency switching harmonics play a great role in determining the common mode current magnitude.

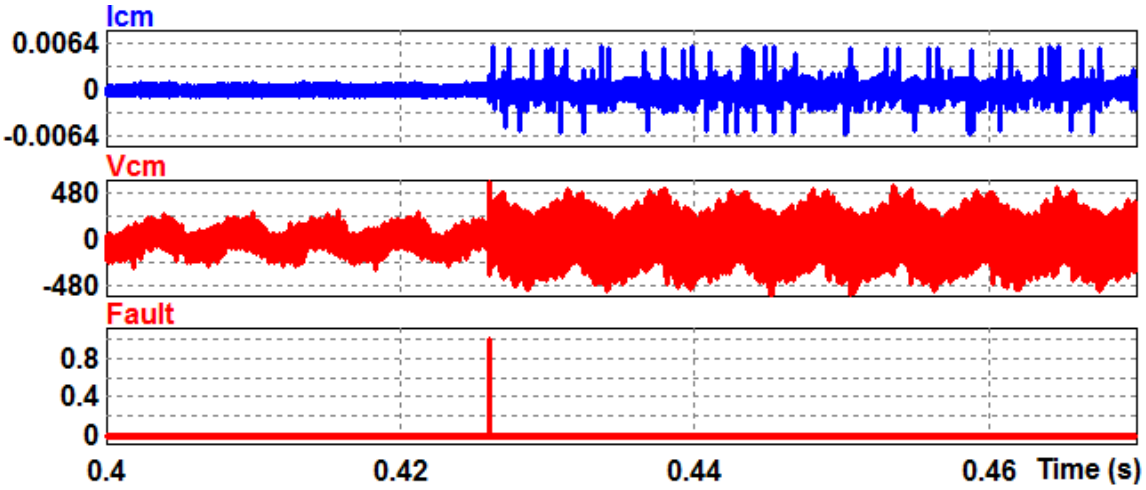

Figure 47. Common mode current (amperes) and voltage (volts) pre and post fault operation

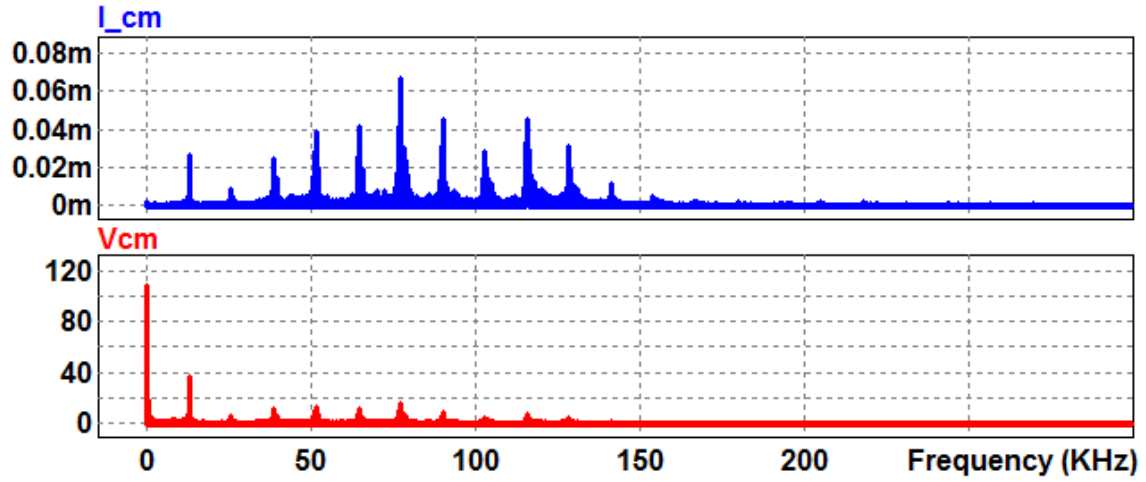

Figure 48. Common mode current (amperes) and voltage (volts) frequency spectrum for normal operation

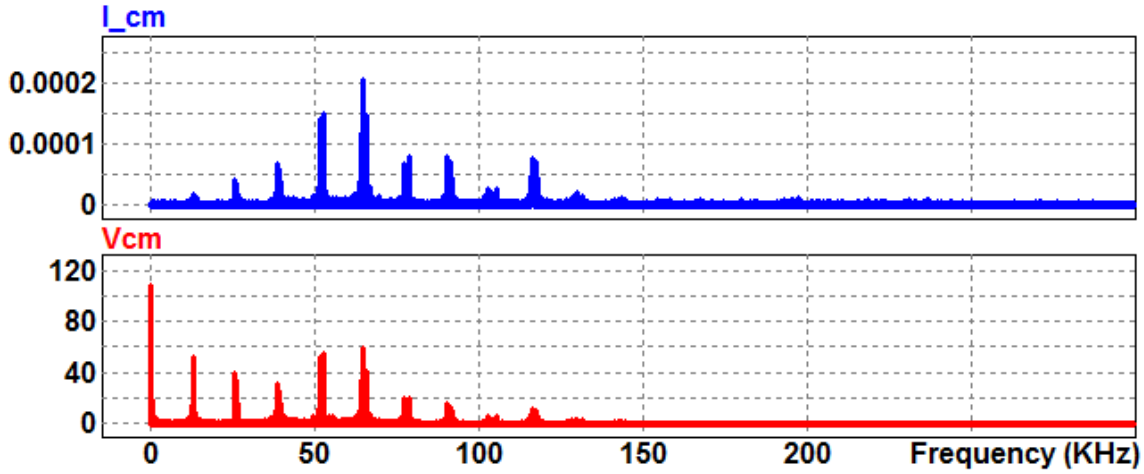

Figure 49. Common mode current (amperes) and voltage (volts) frequency spectrum for post fault operation

IV.2.4. Long cable simulation

The effect of long cable is discussed in section I.4.2. For all simulations, the proposed ASD topology is simulated with a long cable (~100 ft) model and without the auxiliary leg and the output filter. The output of the inverter is directly connected to the motor through a long cable. The long cable is modeled in five sections, each 20 ft. long. The distributed parameter model of the cable is shown in Figure 50.

For simulation, the time step is chosen as 0.1 µs to emulate a rise time of 0.1 µs. The cable parameters for each 20 ft. section are taken for BELDEN 29528 motor supply cable [69]. The simulation results are shown in Figure 51 and Figure 52. Large voltage overshoots are observed (Figure 52) when long lead is included between the inverter output and motor terminals. These large overshoots result from cable parasitics.

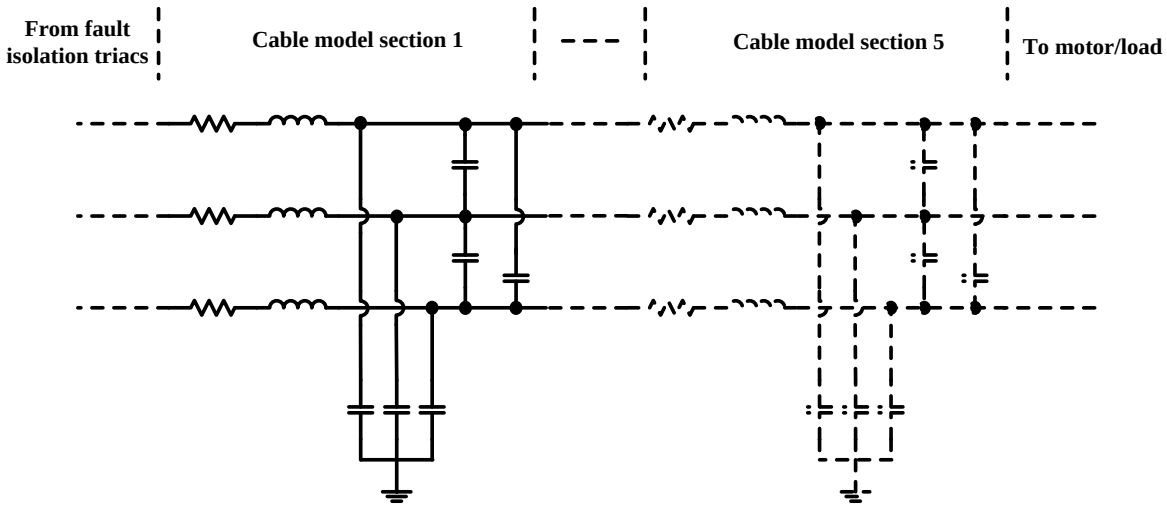

Figure 50. Distributed parameter modeling of cable for simulations

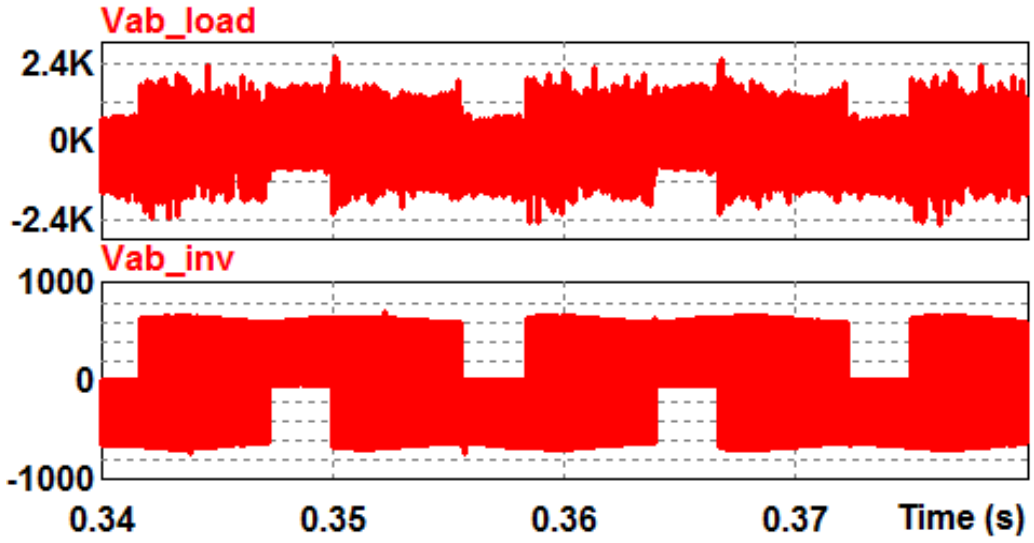

Figure 51. Effect of long cable on 3-leg inverter without output filter

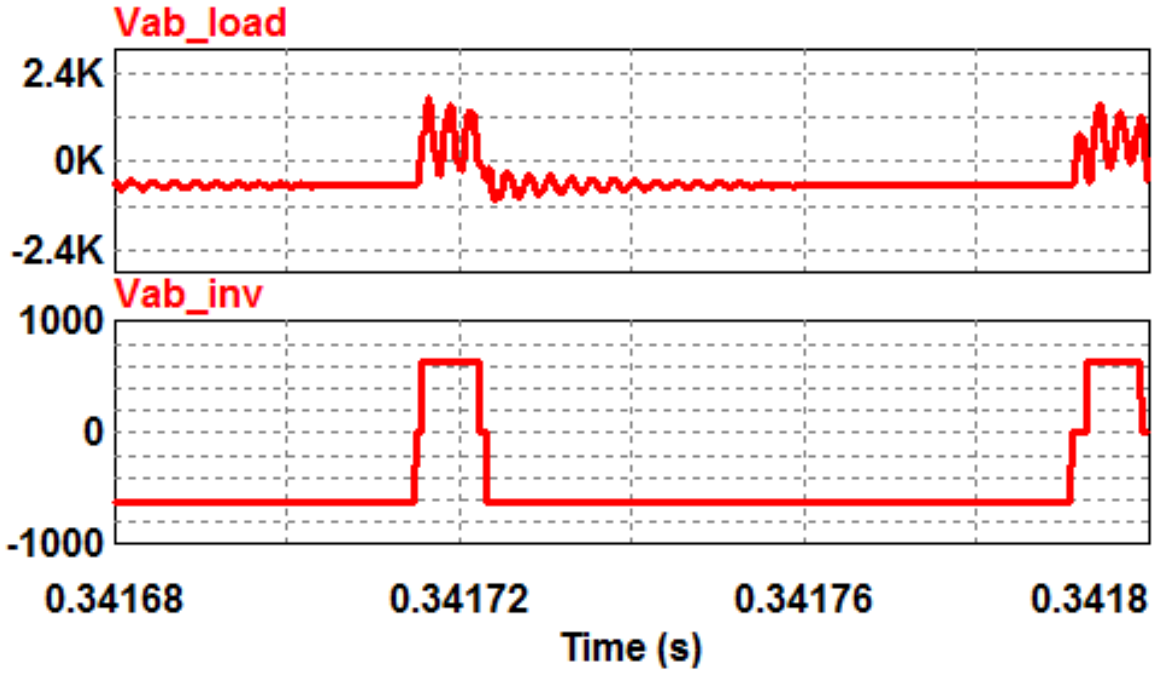

Figure 52. Zoomed in waveforms for effect of long motor leads on 3-leg inverter without output filter

The proposed topology is simulated with the same long cable model. The rise time is again chosen to be 0.1 µs. The simulation results are presented in Figure 53 and Figure 54. It is observed that the line to line voltage at the load/motor terminal is the filtered form of line to line inverter output voltage. As the high frequency voltage components are filtered from the inverter output, the voltage overshoots are not observed at the motor terminal in case of the proposed topology with the output filter. This demonstrates the efficacy of the proposed output filter in reducing the motor winding vulnerability to voltage overshoot.

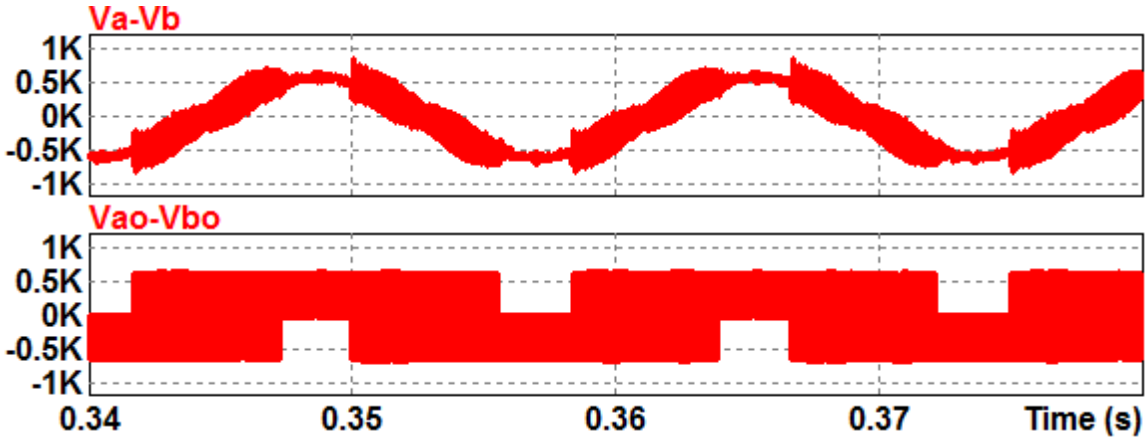

Figure 53. Effect of long cable on proposed 4-leg inverter with output filter

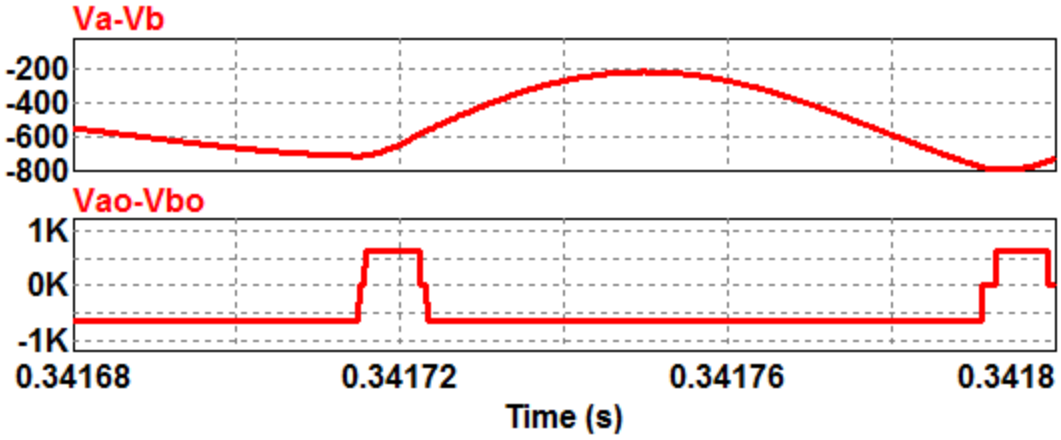

Figure 54. Zoomed in waveform to highlight the effect of long cable on proposed 4-leg inverter with output filter

IV.3. Experimental Results

The experimental results obtained for common mode performance and fault mode operation are discussed in this section. The effect of long cable is also validated in this section. A volt/hertz control comparison is presented for conventional drive topology with SPWM and proposed topology with AZSPWM. The open circuit fault operation of the proposed topology is verified on a 1 hp rated experimental prototype with an R-L load standing in for the electric machine (power factor=0.9). The control is implemented using TI TMS320F28335 microcontroller and ALTERA Cyclone II FPGA. For the implementation, random turn-on solid state relays are used in place of triacs. For the sake of clarity, the isolation and reconfiguration triacs are still referred to as triacs. The resistor R_{fr} and parallel relay S_{fr} are replaced with small inductors. A description of current and voltage parameters, and device labels can be found in Figure 16.

The open circuit fault is emulated by turning off the gating signal to S_{1A} at an arbitrary moment using an SPST switch on the FPGA board. After detection time of 2 ms, all the switches of the inverter and triac T_{fia} are turned OFF. After a predefined wait period (100 μs), the hardware reconfiguration is activated by the controller to replace the faulty leg with the healthy auxiliary leg. The reconfiguration triac T_{fra} is turned ON. The gating signals for the two un-faulted legs remain unchanged and that of the auxiliary leg are updated. The inverter enters fault mode operation. The operation of the system in open circuit fault mode is shown in Figure 55 and Figure 56. The waveform for DC bus voltage ($V_{\_DC}$), common mode voltage (V_{CM}), triac T_{fra} current ($I_{\_Tfra}$) and triac T_{fia} current ($I_{\_Tfia}$) are shown.

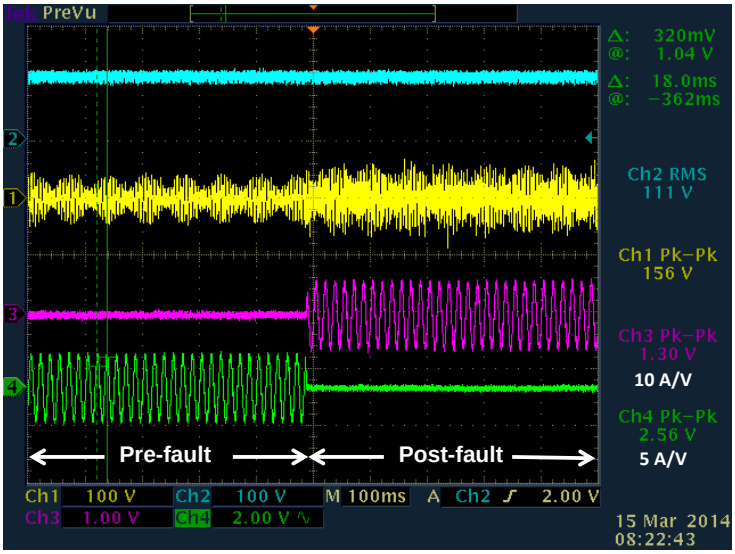

Figure 55. Experimental result for open circuit fault. Ch1: Common mode voltage at load neutral (V_{CM}), Ch2: DC bus voltage ($V_{\_DC}$), Ch3: T_{fra} current ($I_{\_Tfra}$) and Ch4: T_{fia} current ($I_{\_Tfia}$)

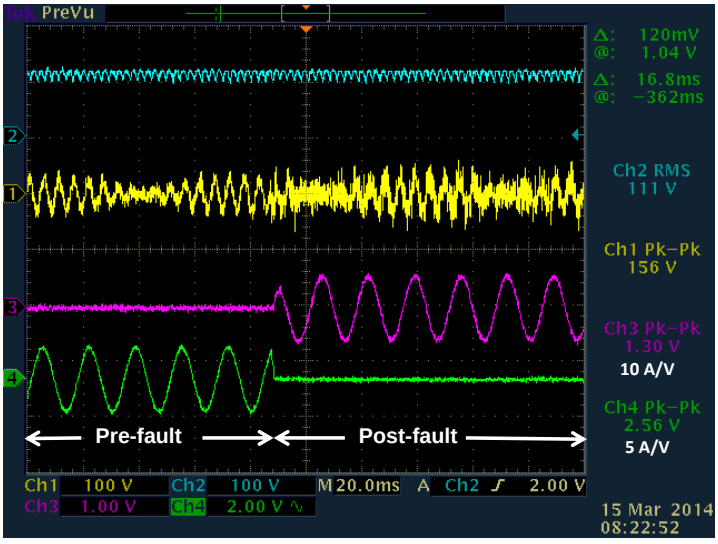

Figure 56. Zoomed waveforms for open circuit fault, Ch1: Common mode voltage at load neutral (V_{CM}), CH2: DC bus voltage ($V_{\_DC}$), Ch3: T_{fra} current ($I_{\_Tfra}$) and Ch4: T_{fia} current ($I_{\_Tfia}$)

It can be seen that the load current is transferred from triac T_{fia} (conducting pre-fault) to triac T_{fra} (conducting post fault), which demonstrates completion of the reconfiguration process. The beat frequency observed in the common mode voltage is due to the difference (≈ 5 Hz) in inverter output fundamental frequency and utility supply input frequency. It can also be observed that common mode performance degrades in post fault condition, since 3-leg operation increases switching frequency harmonic components in the common mode voltage. Another set of experimental results are presented in Figure 57 and Figure 58. The load current is shown in Figure 57 and the load line to line and line voltages are shown in Figure 58. The wait time in these set of experiments is reduced from 100 µs to 20µs.

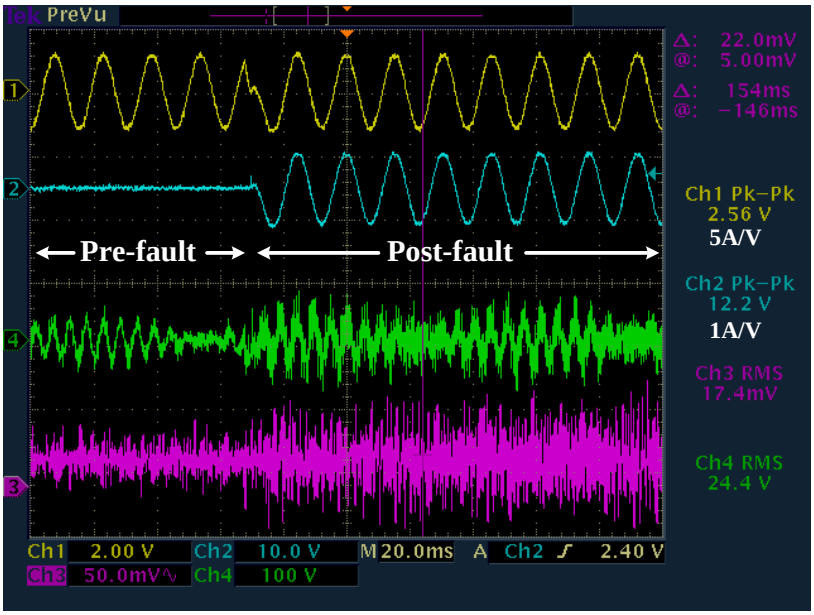

Figure 57. Waveforms for open circuit fault, Ch1: load current ($I_{\_loadA}$), CH2: T_{fra} current ($I_{\_Tfra}$), Ch3: common mode voltage (V_{cm}) and Ch4: common mode current ($I_{\_cm}$)

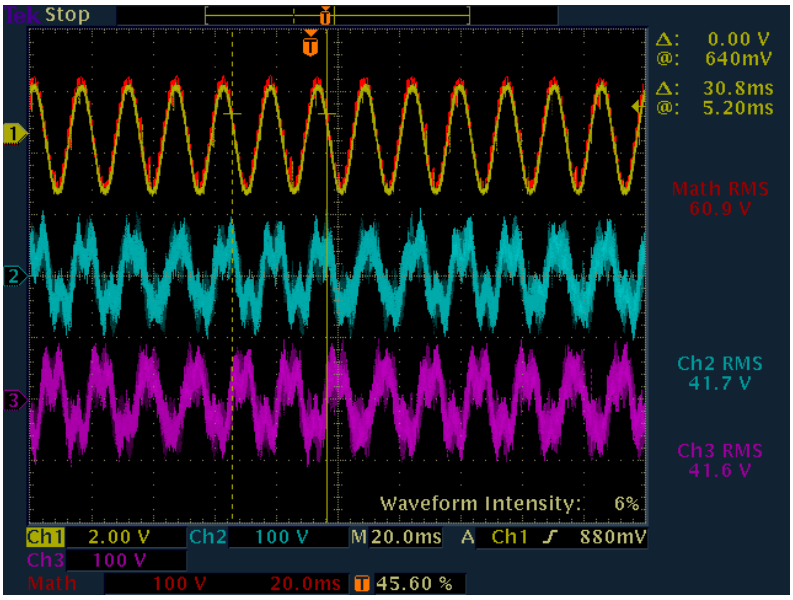

Figure 58. Ch1: Line to line voltage at motor (V_{ab_load}) and Ch2 & Ch3: line to ground load voltages (V_{bg} and V_{cg})

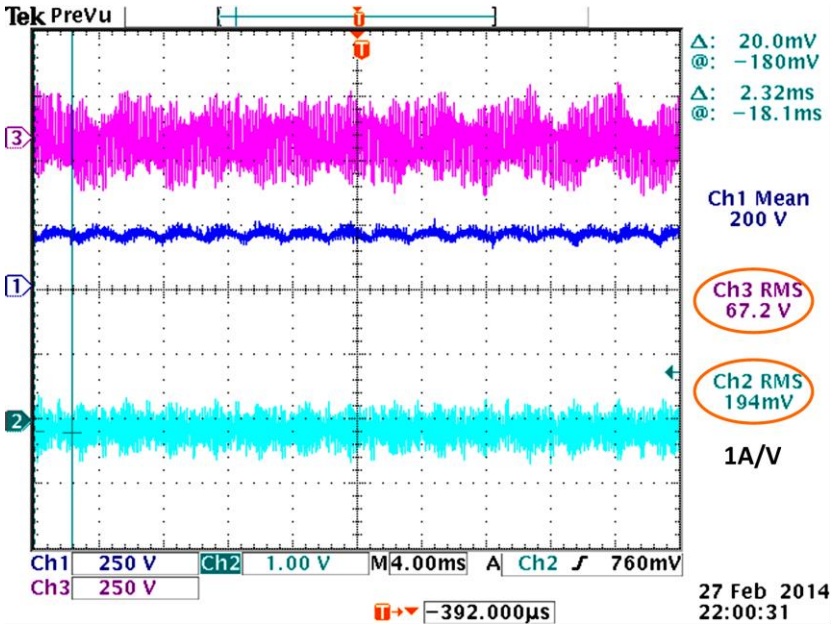

Figure 59. Common mode performance in sine PWM (3-leg). Ch1: DC bus voltage ($V_{\_DC}$), Ch2: common mode current ($I_{\_CM}$), Ch3: common mode voltage (V_{CM})

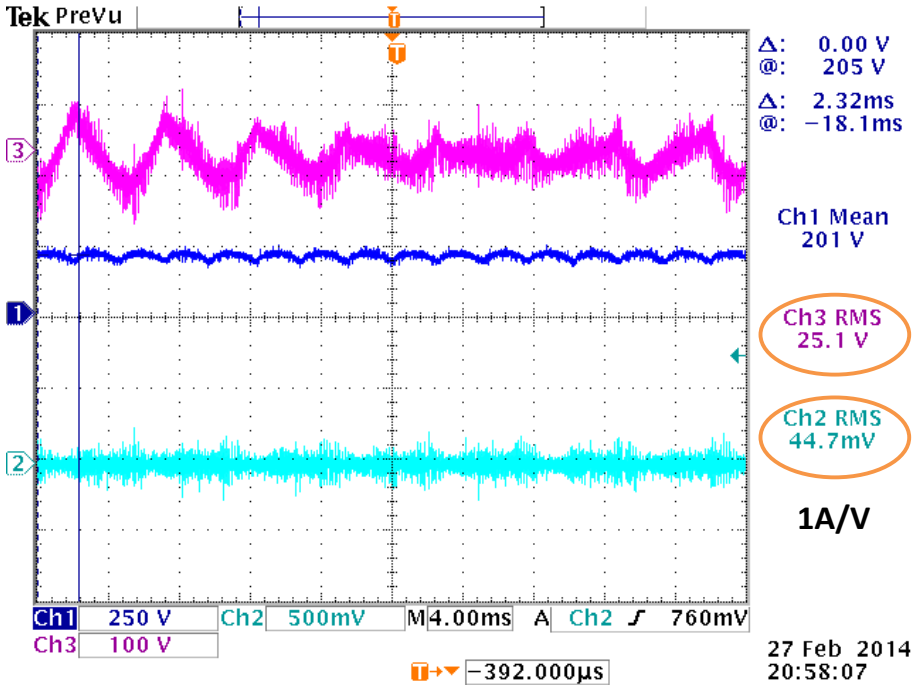

Figure 60. Common mode performance in AZSPWM (4-leg) (scales different from Figure 59). Ch1: DC bus voltage ($V_{\_DC}$), Ch2: common mode ground current ($I_{\_CM}$), Ch3: common mode voltage at load neutral (V_{CM})

The common mode performances of the AZSPWM modulation strategy (4-leg) and sinusoidal PWM (3-leg) have been verified on the 1 hp rated experimental prototype. A DC bus voltage of 200V is used with a resistive load. A ground coupling capacitor (C_g) of 10 nF is used between load neutral and ground. The load neutral voltage and the ground current through coupling capacitor are shown in Figure 59 and Figure 60 for 3-leg Sine PWM and 4-leg AZPWM operation respectively. As in previous results, the beat frequency observed in the common mode voltage is due to the difference (≈ 5Hz) in inverter fundamental frequency and supply frequency. It can be seen that there is a significant reduction in rms value common mode voltage (~60%) and ground

current (~80%) in the AZPWM case. As shown in the analysis section II.D, there is a third harmonic component in common mode voltage and high frequency components have been significantly attenuated.

The inverter output frequency for the hardware is varied to emulated open loop V/Hz control. The CMDR is calculated for 3 leg SPWM and 4 leg AZSPWM cases for different frequencies. The modulation indices at different frequencies are summarized in Table 10.

Table 10. Volt/hertz control emulation: variation of modulation indices with inverter output frequency

Inverter output frequency (in Hz)	Modulation index (SPWM)	Modulation index (AZSPWM)
65	1	0.753
45	0.692	0.521
30	0.462	0.348

The common mode voltage data obtained in these three cases is exported to MATLAB® and processed to obtain CMDR. The CMDR variation with frequency is plotted in Figure 61. It is evident that as analyzed in section III, the common mode performance in a conventional SPWM strategy degrades as the modulation index decreases (frequency decreases). The variation in CMDR is significantly lower for AZSPWM strategy in the entire modulation index range. This result is in close agreement with the analysis presented in section III.3.

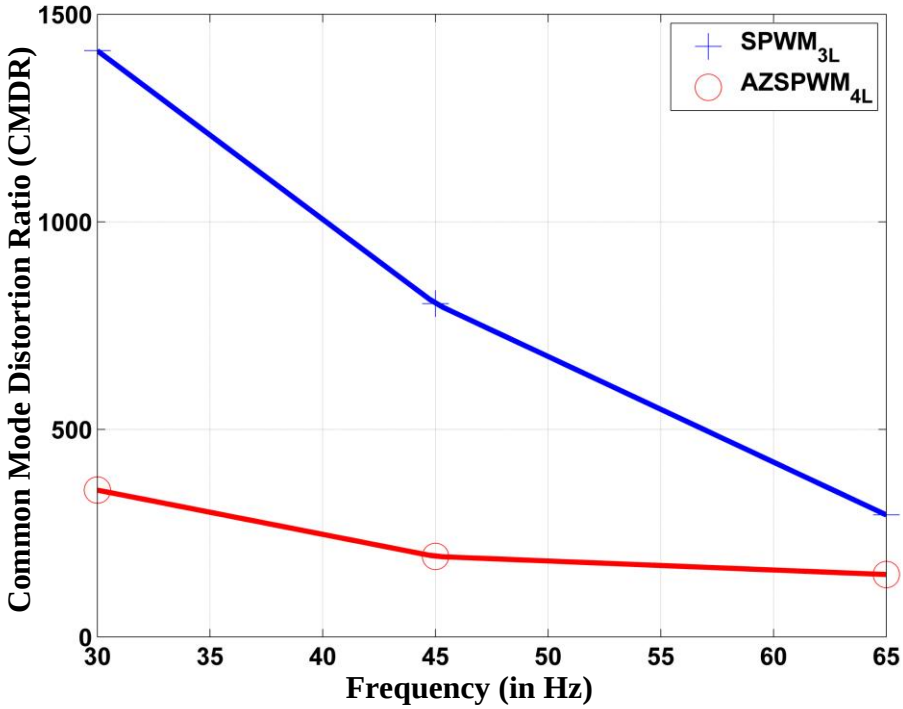

Figure 61. Variation of CMDR with frequency in volt/hertz control for 3-leg SPWM and 4-leg AZPWM strategies

The effect of long cable (~90 ft.) is also verified on the prototype for 3-leg (conventional) and 4-leg (proposed) inverter. The cable consists of three 12 AWG wires twisted together. The cable parameters are tabulated in Table 11.

Table 11. Cable parameters

Cable parameter	Value per feet
Inductance	0.28 µH
Conductor to conductor Capacitance	6 pF

The long cable (~90 ft.) is directly connected between the 3-leg inverter and R-L load. The inverter is modulated with AZSPWM modulation and modulation index = 1. The effect of long lead wire parasitics can be observed in Figure 62 and Figure 63. The pulse width modulated line to line voltage is measured at inverter output and load terminals. The measurements in Figure 63 show line to line voltage overshoot of 75% of the nominal value. It is observed that the largest overshoot occurs when the step change in voltage is maximum (negative to positive DC bus).

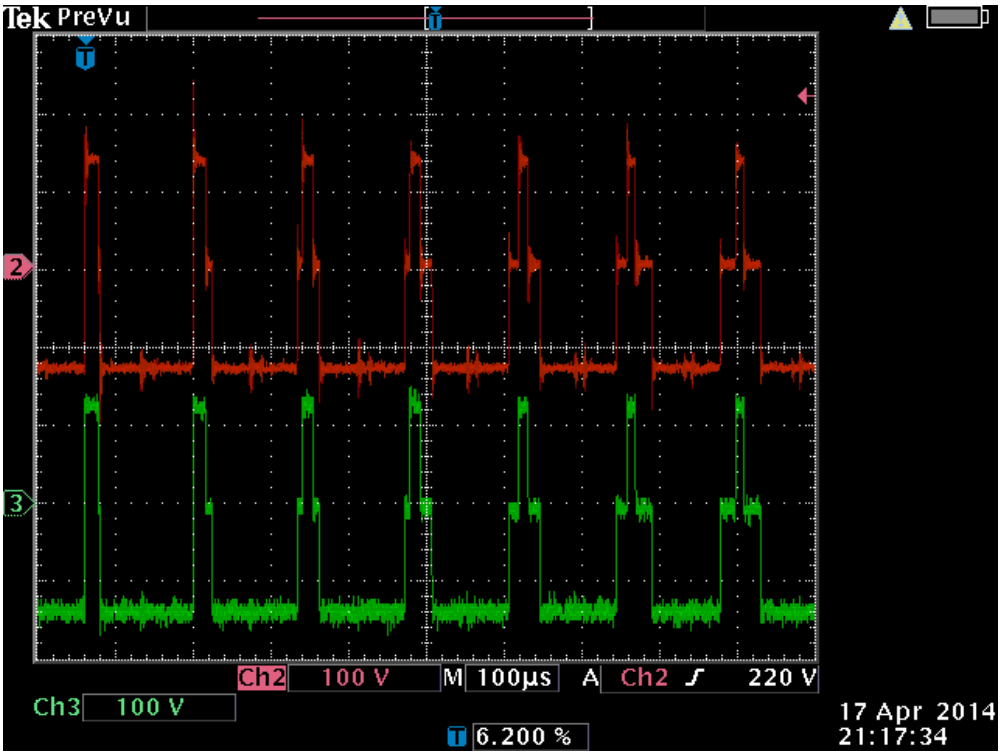

Figure 62. Effect of long cable on 3 phase inverter without output filter. Ch2: line to line voltage at load and Ch3: line to line voltage at inverter

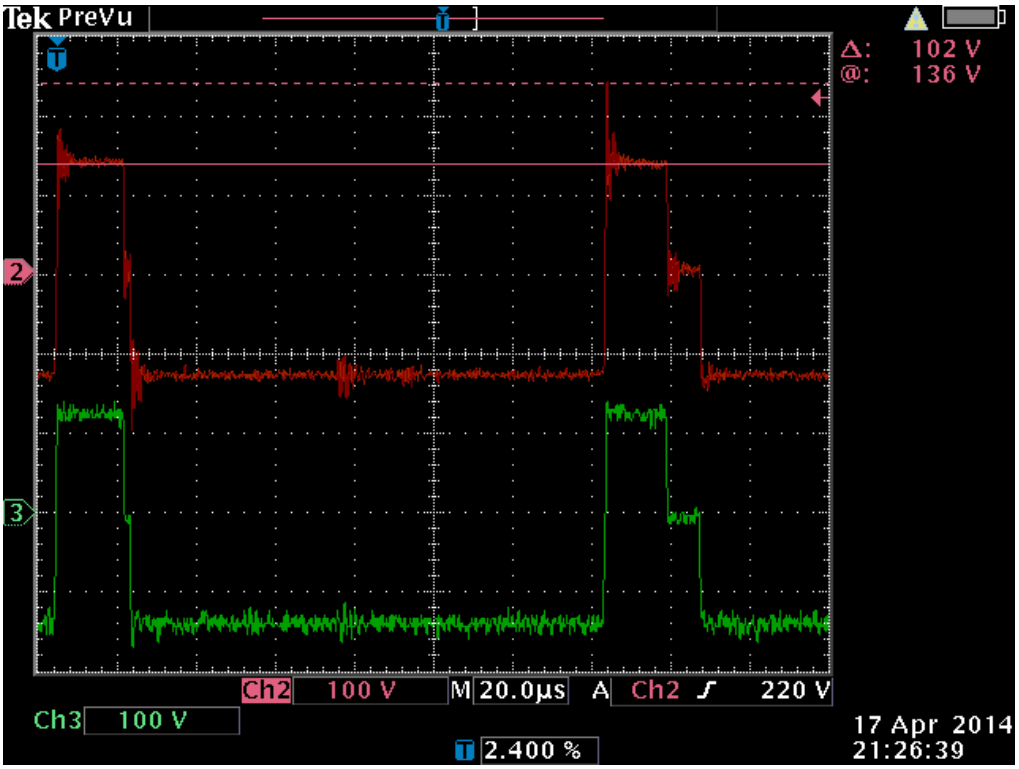

Figure 63. Zoomed in waveforms. Ch2: line to line voltage at load and Ch3: line to line voltage at inverter

The measurements are repeated with the long cable for the proposed topology shown in Figure 16. The current limiting resistor R_{fr} and parallel relay S_{fr} is replace with small inductors. The results are seen Figure 57 and Figure 58. It is observed that large voltage overshoots are absent from the line to line voltage at the load. The output filter in the proposed topology filters out high frequency components from the line to line inverter output voltage (Figure 64). The zoomed in waveforms in Figure 65 confirm the absence of large voltage overshoots at the load terminals.

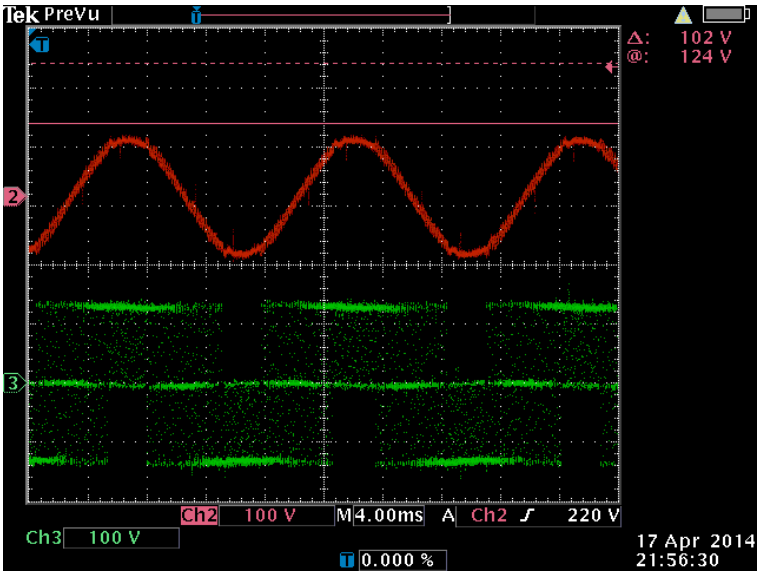

Figure 64. Long motor leads with the proposed topology (4-leg). Ch2: line to line voltage at load and Ch3: line to line voltage at inverter

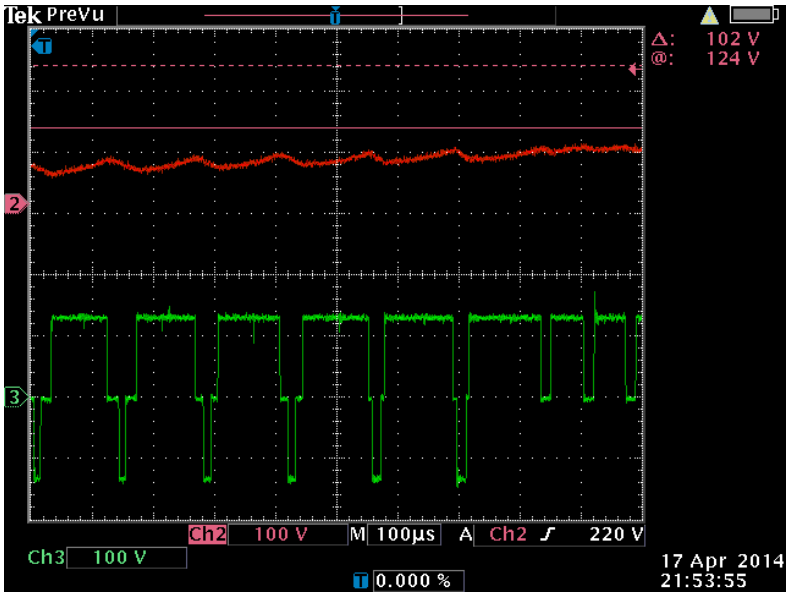

Figure 65. Zoomed in waveform for long lead with proposed topology (4-leg). Ch2: line to line voltage at load and Ch3: line to line voltage at inverter

IV.4. Conclusion

A design example was presented for an 80 kW system. The simulation results were discussed for operation in different modes. The results obtained from simulation were shown to meet the design specification. The transient performance of the topology in case of transition from one operation mode to another was discussed. The experimental results obtained from laboratory prototype rated at 1 hp were presented. The transient voltage and currents were shown for open circuit fault in switch S_{1A}. The fault isolation and reconfiguration process was validated. The common mode performances of 3-leg SPWM and 4-leg AZSPWM based ASD topologies were compared. The open loop volt/hertz control scheme was emulated by changing inverter output frequency and modulation index. The results were compared for 3-leg SPWM and 4-leg AZSPWM strategies using the proposed figure of merit, CMDR. The common mode analysis in Section III is also validated with experimental results. Finally, long cable effect was illustrated. In the proposed topology, line to line voltages at the load terminals are free from large voltage overshoots.

V CONCLUSION AND FUTURE WORK

V.1. Summary

Motor drive systems (MDSs) use a significant portion of the electric energy used in the industry. The increase in electricity prices and demand for efficiency has led to the introduction of adjustable speed drives (ASDs) to replace mechanical gears and valve controlled systems. Adjustable speed drives enable variable speed operation by controlling input power to the motor which results in higher efficiency and greater energy savings.

In a number of applications, MDS are integrated in continuous process industry. Any interruption of production leads to significant financial impact due to production loss and other follow-up costs. Further, the introduction of ASDs has led to a lot of interest in the study of failure modes of the MDS with the intent to maximize availability. The different issues concerning availability of MDS: a) semiconductor failures, b) motor bearing failure, c) motor winding breakdown and d) grid voltage sags, have been extensively studied. A number of solutions have been proposed which address these concerns independently. In this thesis, a single solution is proposed to reduce vulnerability of motor drive system to semiconductor faults in ASD, bearing failure and winding breakdown in motors and sags in the utility supply voltage. This is achieved by the inclusion of an auxiliary inverter leg, 3 diodes, isolation and reconfiguration circuits to a conventional ASD topology. The proposed topology operates in three different modes.

The operation of the proposed topology is discussed in detail for different modes of operation, a) Fault mode, b) Active Common Mode Suppression mode, and c) Auxiliary Sag Compensation mode. The Active Zero State PWM strategy (AZSPWM) is used to achieve common mode suppression. The isolation, reconfiguration and control strategy is discussed for different modes of operation. The common mode and differential mode performance of AZSPWM strategy is compared with conventional Sinusoidal PWM (SPWM) and Space Vector Modulation (SVM) strategies. A new of merit, Common Mode Distortion Ratio (*CMDR*), is proposed to compare the common mode performances. The first order distortion factor, DF_2, is used to evaluate differential mode performance of different modulation schemes.

The operation of the proposed topology is validated by design and simulation of an 80 kW motor drive system with a 100 hp induction motor load. The voltage and current ratings for different passive and semiconductor components is presented. The simulation results are presented for different modes of operation and transients are studied in detail. The simulation results are experimentally verified on a laboratory prototype rated at 1 hp. The experimental results for open circuit faults are discussed. The common mode performance of the proposed topology is compared with a conventional 3-leg inverter topology. An open loop volt/hertz operation is emulated by varying the inverter output frequency and modulation index. From experimental data, a comparison based on *CMDR* is presented for SPWM and AZSPWM schemes with varying frequency. The effects of long cable are also illustrated on the laboratory prototype.

V.2. Future Work

The following areas could be explored for future work:

- Evaluation of reliability of the proposed topology
- Exploring optimized modulation strategy (common mode and differential mode performance) for operation in a wide modulation and power factor range
- Testing the proposed topology with a motor load
- Comparison of the size of common mode filter in conventional and proposed system
- Validate auxiliary sag compensation performance
- Quantify cost increase and availability improvements
- Explore similar approach for other adjustable speed drive topologies

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