# A CMOS FRACTIONAL FREQUENCY SYNTHESIZER FOR A FULLY INTEGRATED S-BAND EXTRAVEHICULAR ACTIVITY (EVA) RADIO TRANSCEIVER

A Thesis

by

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# ABSTRACT

Extravehicular activity (EVA) is an important aspect of space explorations. It enables astronauts carry out tasks outside the protective environment of the spacecraft cabin. The crew requires EVA radio transceivers to transmit and receive information among themselves and with equipment in space. Communication is done through the S frequency band (2GHz to 4GHz). Since the EVA radio transceiver is part of the space suits the astronauts wear for EVA, it is important that lightweight, low power consumption and miniaturized systems are utilized in their design and implementation. This thesis presents the design and implementation of a fully integrated frequency synthesizer for carrier signal generation in the EVA radio transceiver.

The transceiver consists of a dual up-conversion transmitter (TX) and a direct conversion receiver (RX) at 2.4GHz. It supports 10 channels spaced at 6MHz for both video and voice communications, covering the frequency band from 2.4GHz to 2.454GHz. Therefore in the TX mode, the frequencies required are 0.8GHz to 0.818GHz (quadrature) and 1.6GHz to 1.636GHz (differential) for dual up-conversion to prevent the pulling problem between the power amplifier (PA) and voltage controlled oscillator (VCO) of the synthesizer. In RX mode, the frequencies from 4.8GHz to 4.908GHz are synthesized with a divide-by-two circuit to generate quadrature signals of 2.4GHz to 2.454GHz.

In order to cover the frequency ranges in both TX and RX modes with a small area and low power consumption, a dual-band VCO fractional-N PLL is implemented. The dual-path loop filter topology is utilized to further reduce chip area.

The fractional synthesizer is fabricated in 0.18µm CMOS technology and has a loop bandwidth of around 40kHz. It occupies a relatively small area of 1.54mm$^2$ and consumes a low power of 22.68mW with a 1 V supply for the VCO and 1.8V supply for the rest of the blocks. The synthesizer achieves a reference spur performance of less than –62.34dBc for the lower band (LB) and less than –68.36dBc for the higher band (HB). The phase noise at 1MHz for the LB ranges from -125.38 to -130.39 dBc/Hz and for the HB -113.12 to -120.16 dBc/Hz. Thus the synthesizer achieves low power consumption with good spectral purity while occupying a small chip area making it suitable for EVA radio applications.

# DEDICATION

To my Lord and Savior Jesus Christ, whose I am and whom I serve… (Acts 27:13)

# ACKNOWLEDGEMENTS

I would like to express my profound gratitude to Dr Kamran Entesari for his direction, help and guidance during my Masters program. Thank you for believing in me and demanding nothing but excellence. I've grown as a better engineer under your tutelage. My sincere appreciation goes to Dr. Edgar Sanchez-Sinencio, Dr. Sunil Khatri and Dr. Ben Zoghi, for serving on my thesis committee and for your invaluable contributions and insights.

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# 1. INTRODUCTION

The future of manned space exploration demands the development and use of low-power, lightweight and miniaturized communication systems. A very important aspect of manned space exploration is extravehicular activity (EVA) which enables astronauts carry out experiments, repairs and space structure construction outside the protective environment of the spacecraft cabin [1]. The astronauts carry out EVA wearing special apparel known as the EVA mobility unit (EMU). The EMU which is a pressurized and oxygen enriched space suit, houses essentials like water and food, medical monitoring systems, body waste management systems for the entire duration of EVA, and communication systems. The communication systems include the EVA radio which enables the crew to transmit and receive information among themselves and with equipment in space [2]. Information is transmitted through the S-Band, the frequency band of 2GHz to 4GHz, which is typically used by weather radars, for satellite communications and some wireless communication standards.

High performance wireless transceiver systems have been implemented in CMOS technologies for a host of wireless communications applications [3-6]. A key building block in the transceiver is the frequency synthesizer whose purpose is to generate the local oscillator (LO) signals for the transmitter (TX) and receiver (RX). This work presents a fully integrated CMOS frequency synthesizer for an S-Band transceiver at 2.4GHz for EVA radio applications.

## 1.1 EVA Transceiver Architecture

The EVA transceiver makes use of the direct conversion RX (DCR) and a dual up-conversion TX (Fig. 1-1). The DCR consists of a band select filter (BPF) which selects the desired RX band and rejects out-of-band signals, a low noise amplifier (LNA) which amplifies the desired signal with minimal noise contribution, passive current-mode mixers for down-conversion of the RF signal to baseband, transimpedance amplifiers (TIA) to convert the output of the mixer from current to voltage and provide some amplification, low pass channel select filters (LPF) and variable gain amplifiers (VGA) [7]. The DCR is used because its design process is simpler than heterodyne receivers. In the DCR there is no image problem, hence an image reject filter is not needed, the channel selection is carried out by low pass filters which are easily integrated on-chip, the VGAs operate at baseband and the number of mixing spurs are greatly reduced and are easier to deal with [7].

The DCR however suffers from LO emissions and DC offsets produced by LO leakage to the antenna. The LO emissions may negatively impact other receivers working in the same band by desensitizing them [7]. The DC offset on the other hand is amplified with the desired signal in the LNA/Mixer cascade and can saturate the baseband circuits making signal detection impossible [7]. Another problem with the DCR is that, the desired signal, when down-converted to baseband (around zero frequency) is relatively small and is susceptible to flicker noise. Flicker noise which is essentially low frequency noise can easily corrupt the received signal especially for short-channel CMOS technologies [7].

One way to minimize the problem of LO leakage is to layout the RF signal path and LO symmetrically [7].

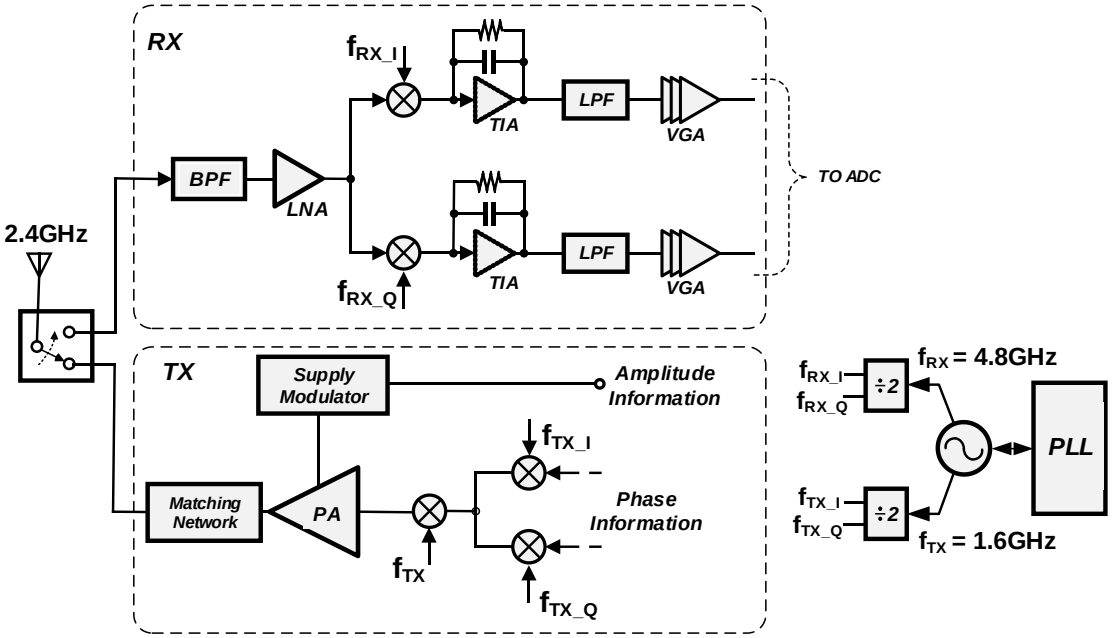



Figure 1- 1 EVA Transceiver Architecture

A DC-free coding approach [8] is also implemented where the bandwidth from DC to a determined offset ($f_1$) does not carry any information. The actual information stored in $f_2 - f_1$ is therefore not affected in any way by DC offsets and is not significantly affected by flicker noise as shown in Fig. 1-2.

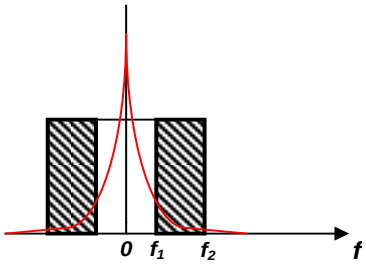


Figure 1- 2 DC-free Coding

The TX consists of a supply modulator whose input is the amplitude information of the signal to be transmitted. This block together with the PA forms a class H amplifier which tracks the input signal amplitude and uses that to modulate the voltage on the supply rails of the PA [9]. The role of the matching network after the PA is to deliver maximum signal power to the antenna and filter out-of-band components that result from PA nonlinearity [7].

In the TX of fully integrated transceiver systems, the problem of oscillator pulling between the outputs of the power amplifier (PA) and voltage controlled oscillator (VCO) of the synthesizer is a serious issue if both frequencies are the same or harmonics of each other. This problem is addressed by making the VCO and PA operate at different frequencies sufficiently wide apart [7] and which are not integer multiples of each other [3]. As shown in Fig. 1-1, the TX performs a phase shift at $f_{TX\_I}/f_{TX\_Q}$ (0.8GHz) after which the output is translated by $f_{TX}$ (1.6GHz) to the RF frequency (2.4GHz). Thus the problem of VCO pulling is prevented in the TX.

**1.2 Frequency Planning and Proposed Architecture for PLL**

The required LO signals for this transceiver are 0.8GHz quadrature and 1.6GHz for the dual up-conversion TX and 2.4GHz quadrature for the DCR as mentioned earlier.

As a result, assuming a divide-by-2 circuit is used to generate the quadrature signals, the VCO has to operate at 1.6GHz in TX mode and 4.8GHz in RX mode. In order to implement the frequency planning shown in Fig. 1-1, two synthesizers or a synthesizer with two VCOs operating at the two desired frequencies can be used. However, these two approaches are inefficient in terms of area and power consumption.

To overcome these inefficiencies, a single synthesizer with a dual-band VCO, originally used in [10] as a wideband VCO, is proposed to generate the frequencies at 1.6GHz and 4.8GHz for the TX and RX, respectively. The required quadrature signals are then generated by a divide-by-2 circuit implemented as part of the synthesizer.

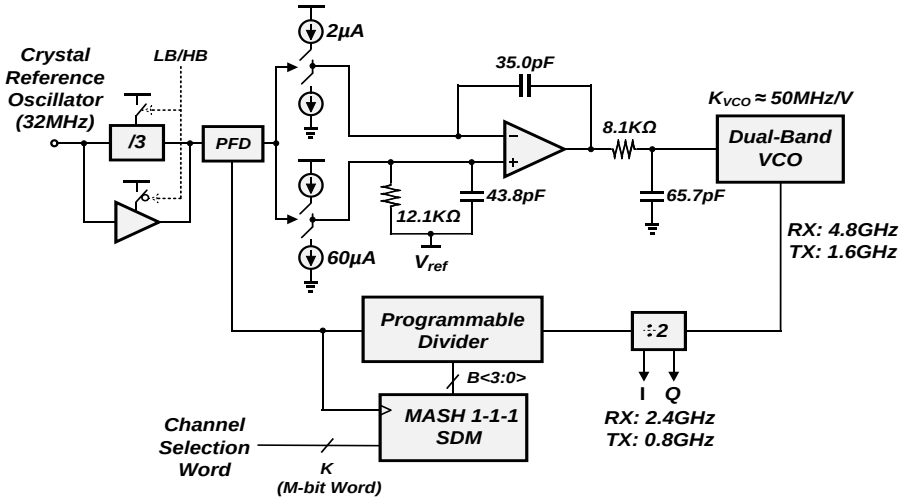



Figure 1- 3 Phase Locked Loop Architecture

The PLL Architecture chosen for the transceiver is shown in Fig. 1-3. This fourth order type-II PLL consists of a dual-band VCO[1] to cover the desired frequency bands, a divide-by-2 unit to generate the required I/Q signals, a pulse-swallow programmable loop divider and a 3rd-order MASH 1-1-1 sigma delta modulator (SDM) to provide the fractional divide ratios with a resolution of approximately 2Hz, a divide by three (/3) reference frequency divider to simplify the design of the loop divider, a phase/frequency detector (PFD), two charge pumps and a dual-path active loop filter to realize small capacitors which can be easily integrated on-chip.

### 1.3 Thesis Organization

This thesis document is organized as follows. Section 2 highlights some fundamentals of PLLs. The linear model is introduced and transfer functions for the individual blocks of the PLL are derived for initial design and noise analysis. The dual-path loop filter is analyzed in this section and its advantages of providing small loop capacitors for narrow bandwidths is established. Section 3 contains the circuit design and implementation of the PFD, charge pumps, loop filter and dividers. The VCO design is explained briefly in this section. A test chip without the SDM is fabricated in 0.18μm CMOS and fabrication measurement results are included in this section. In section 4, the analysis, modeling and design of the MASH 1-1-1 SDM and concepts of fractional division are discussed. A second test chip with the SDM included is fabricated in

[1] The dual-band VCO as described in Section 3-5 is the work of Mr Masoud Moslehi Bajestan (Analog & Mixed Signal Center, Texas A&M University, CS, TX, 77843), a collaborator in this research.

0.18μm CMOS with the measurement results reported. The conclusions are discussed in Section 5 and the list of references used is outlined in Section 6.

# 2. FUNDAMENTALS OF PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

In this section, some fundamentals of charge pump PLLs (CP-PLL) and the basic operation of each of the blocks are described. After the general considerations of the basic charge pump PLL are presented, the linear model is introduced and utilized in an initial design for the PLL architecture described in Section 1. Equations are derived for the analysis of the loop and for the calculation of loop parameters. The noise transfer functions are derived from the linear model and the phase noise contributions of the blocks of the PLL are obtained.

## 2.1 PLL Basics

A PLL is a non-linear feedback system which compares the phase of the feedback signal usually from a voltage controlled oscillator (VCO) to the phase of a reference clock signal using a phase detector (PD). A low pass loop filter (LF) is inserted to remove unwanted high frequency components of the phase error (the phase difference between the reference and the VCO) and provide the control voltage for the VCO, Fig 2-1.

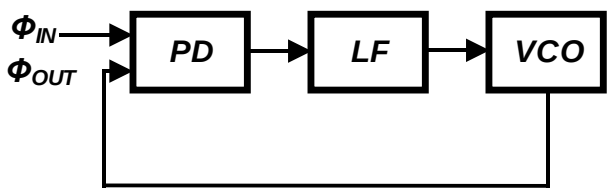



Figure 2- 1 Basic PLL Block Diagram

The blocks are connected to form a negative feedback loop, hence, the control voltage changes the VCO frequency in a direction that reduces the phase difference [11].When the phase difference does not change with time, the PLL is said to be locked. Though the PLL is essentially a non-linear system, under locked conditions, with small phase error; it can be modeled as a linear system. Therefore, powerful tools of linear analysis like Laplace and Fourier transforms can be used to analyze the behavior of the loop.

The basic CP-PLL is made up of a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a frequency divider (FD) and a voltage controlled oscillator (VCO), Fig. 2-2.

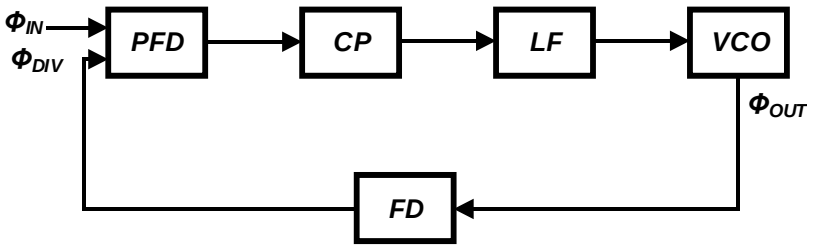



Figure 2- 2 Charge Pump PLL

### 2.1.1 Reference Signal

The accuracy and stability of the PLL's output frequency depends heavily on the purity of the reference signal [12]. In order to generate reference signals of very precise and stable frequencies, crystals (commonly quartz crystals) are used.

### 2.1.2 Phase Frequency Detector (PFD)

The PFD senses the phase difference between the reference signal and the feedback signal from the frequency divider and generates signals (UP and DN) that are used to control the charge pump switches. The net duty cycle of the UP and DN signals is the phase error between the inputs to the PFD. The PFD is made up of two resettable D-Flip-Flops with an AND gate and some delay in the reset path to ensure minimum width on the output pulses to prevent the dead-zone. Dead-zone is caused when the output pulse widths are not wide enough to properly reset the DFFs and fully turn on the charge pump switches during each cycle. The schematic of the PFD is shown in Fig. 2-3. The data terminals are held permanently at HIGH ('1'). The reference ($f_{REF}$) and feedback ($f_{DIV}$) signals are applied to the clock terminals of the flip-flops [11].

An active UP signal tells that the $f_{REF}$ is leading $f_{DIV}$ and an active DN signal tells that $f_{REF}$ is lagging behind the $f_{DIV}$. These conditions tell the PLL to either raise or lower VCO frequency respectively. Fig. 2-4 shows the ideal waveforms of the PFD. As mentioned earlier the difference between the UP and DN signals constitutes the phase error.

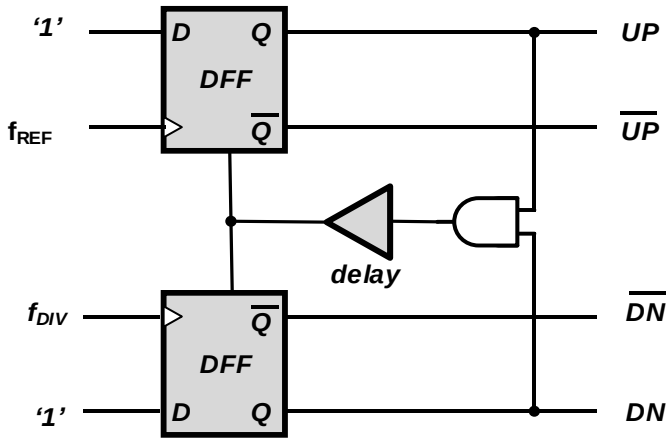



Figure 2- 3 Phase Frequency Detector Schematic

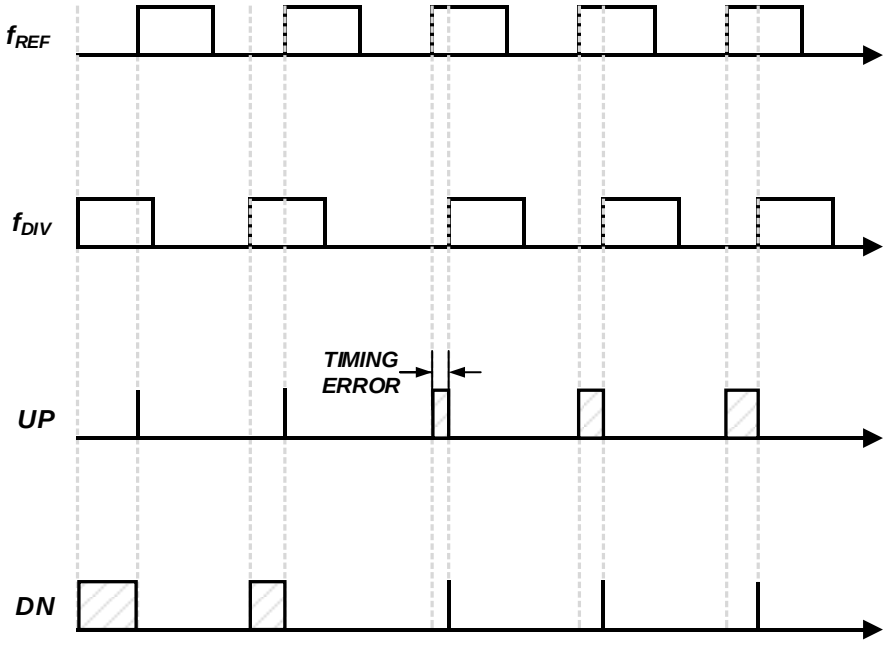



Figure 2- 4 Ideal PFD Waveforms

### 2.1.3 Charge Pump

The charge pump (Fig. 2-5) is a pair of electronic switches that are controlled by the UP and DN outputs of the PFD. When the reference signal leads the feedback signal, the UP switch is turned on. The charge pump sources current from the $I_{UP}$ current source and delivers charge onto the loop filter which increases the control voltage and as a result increases the VCO frequency. When the reference signal lags the feedback signal, the DN switch is turned on and this extracts the $I_{DN}$ current from the loop filter. This action discharges the loop filter and lowers the control voltage. The VCO frequency is decreased as a result.

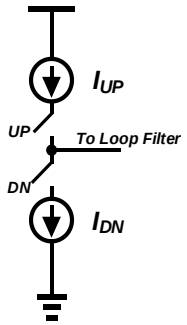



Figure 2- 5 Charge Pump Model

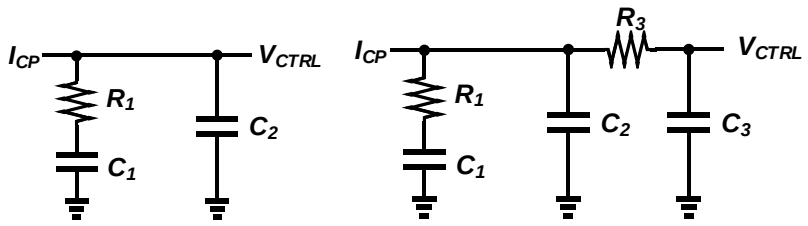
### 2.1.4 Loop Filter

The purpose of the loop filter in a PLL is to establish the loop dynamics and to deliver a control voltage for the VCO [11]. It is also used in filtering out the noise from

the reference signal and the charge pump switching activity. Two broad classes of loop filters exist: passive and active loop filters.

*2.1.4.1 Passive Loop Filter*

A typical passive loop filter used in CP-PLLs is shown in Fig. 2-6 (a). In order to provide higher suppression, an additional low pass filter stage can be added to it as shown in Fig. 2-6 (b). In spite of its simplicity, a major drawback of passive loop filters is that for narrow bandwidths, very large capacitors are required which occupy a large area and thus make full integration difficult.




a) b)

Figure 2- 6 a) Second Order and b) Third Order Passive Loop Filters

*2.1.4.2 Active Loop Filter*

As mentioned earlier, the capacitor sizes for the passive loop filters become prohibitively large for narrow bandwidth PLLs when better noise and spur rejection is required. The capacitor sizes are sometimes in the nano-farad range and these either occupy a larger chip area or have to be implemented off chip. Some active loop filter

topologies reduce the loop filter capacitance by using capacitive multiplication to increase the effective capacitance and reduce chip area [12].

### 2.1.5 Frequency Dividers

Frequency dividers are used in the PLL loop to divide the VCO frequency and the reference frequency to comparable frequencies that can be processed by the PFD. The reference frequency divider is usually fixed while the loop divider can be programmable. The frequency divider allows for high frequency signals to be synthesized by the PLL with a low frequency reference signal. For example, frequencies in the gigahertz range can be synthesized from a reference frequency in the tens of megahertz. The most popular frequency dividers are digital counters. They can be easily implemented and programmed and therefore can allow the synthesizer to output many different frequencies.

### 2.1.6 Voltage Controlled Oscillator

The VCO is one of the most critical blocks in the frequency synthesizer. There are two popular types of VCOs used in CMOS technology: the ring oscillator and the LC-tank oscillator. While the ring oscillator has the advantages of wide tuning range, small chip area, easier implementation, and not necessarily requiring passive components like inductors and varactors, its poor phase noise performance and high power consumption makes it undesirable for synthesizers with stringent phase noise performance and power consumption specifications. The LC-tank oscillator on the other hand, has the advantages of achieving higher oscillation frequencies, with lower phase

noise and lower power consumption. However, these come at a cost of increased chip area for on-chip inductors and smaller tuning range.

## 2.2 Linear Model and Analysis of the PLL

As mentioned earlier, when the PLL is locked, the non-linear loop can be represented by a linear model. The linear model of the PLL is shown in Fig. 2-7. The linear model is useful as an initial design approximation for the bandwidth and stability of the PLL and also for determining the noise contributions of the various blocks in the PLL as shown in Fig. 2-8.

Transfer functions describe in mathematical form the relationship between the inputs and outputs of blocks in a linear system. In the case of the PLL, the inputs and outputs of the transfer functions are phase quantities. These important transfer functions that are derived from the linear model aid with the initial design of the PLL.

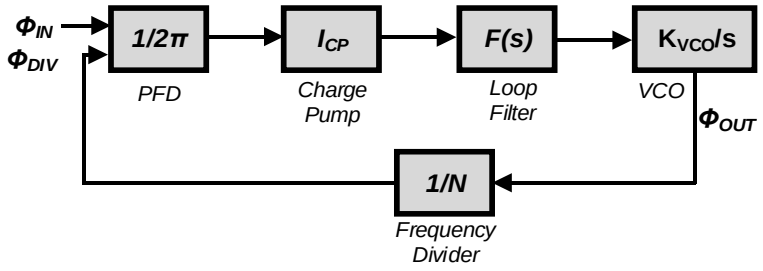



Figure 2- 7 Linear Model of PLL

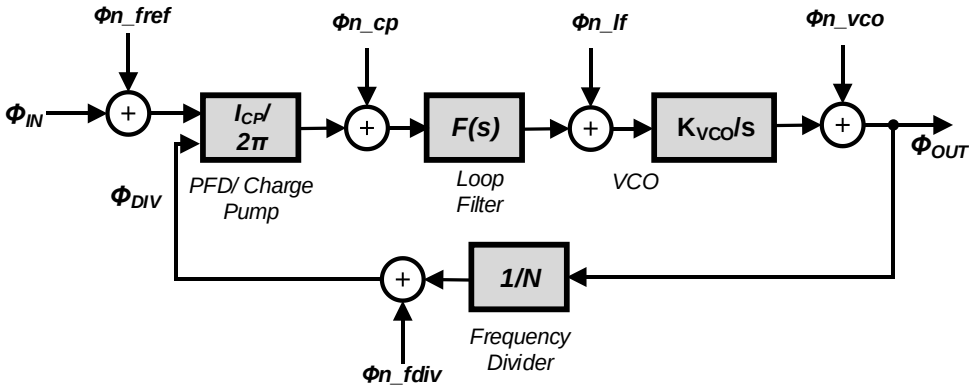



Figure 2- 8 Linear Model of PLL showing Noise Contributions of the PLL BLocks

### 2.2.1 Phase Frequency Detector and Charge Pump

The transfer function of the PFD is a gain term that is derived from slope of its transfer characteristic between -2π to 2π in Fig 2-9. The charge pump is modeled by the magnitude of the current that is delivered or extracted from the loop filter.

The transfer function of the PFD and CP together is given by:

$$\frac{I_{CPout}}{\theta_{PD}} = \frac{I_{CP}}{2\pi} \qquad 2-1$$

Where $I_{CPout}$ is the current delivered or extracted from the loop filter, $\theta_{PD} = \theta_{IN} - \theta_{DIV}$ i.e. the phase difference between input phase and feedback phase.

The PFD state diagram can be used to describe the operation of the PFD. The PFD has three states for the output UP and DN signals which depend on which signals, $f_{REF}$ or $f_{DIV}$, rise first. Assuming the PFD starts in the UP=0, DN=0 state, when $f_{REF}$ 'leads' (rises before) $f_{DIV}$, the UP signal is active and the PFD transitions into state UP=1, DN=0 and continues that way until $f_{DIV}$ leads $f_{REF}$. This takes the PFD back into

its initial or null state, and if $f_{REF}$ continues to 'lag' $f_{DIV}$ would transition to the state UP=0, DN=1.

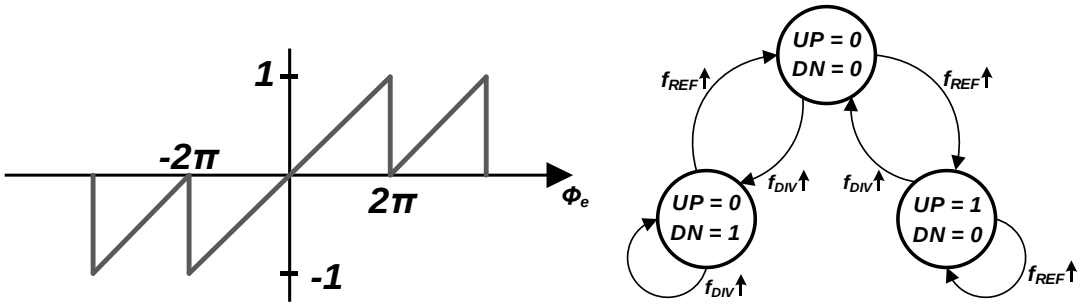



Figure 2- 9 Ideal PFD Transfer Characteristic and PFD State Diagram

### 2.2.2 Dual Path Loop Filter (DPLF)

In the DPLF,two signal paths $V_Z$ and $V_P$ are added as shown in Fig. 2-10 to create a low frequency virtual zero which provides stability for the PLL loop without the need for a large loop filter capacitor [11-13]. The filter makes use of two charge pumps with current scaling factor B.

The transfer function for the third order DPLF is given by:

$$F(s) = \frac{V_{CTRL}(s)}{I_{CP}(s)} = \frac{1 + s(C_P + B \cdot C_Z) \cdot R_P}{sC_Z \cdot (1 + sC_P R_P)} \cdot \frac{1}{1 + sC_3 R_3} \qquad 2-2$$

From the transfer function, it can be seen that there is a zero, $\omega_z = 1/\boldsymbol{\tau_Z}$, which is dependent on the current scaling factor B. Therefore, the location of zero can be controlled by changing the current ratio B. Moreover, increasing B minimizes the total

required capacitance. $\omega_p = 1/\boldsymbol{\tau_P}$ and $\omega_3 = 1/\boldsymbol{\tau}_3$ are the high frequency poles of the filter.

$$\tau_Z = (C_P + B \cdot C_Z) \cdot R_P \qquad 2-3$$

$$\tau_P = C_P R_P \qquad 2-4$$

$$\tau_3 = R_3 C_3 \qquad 2-5$$

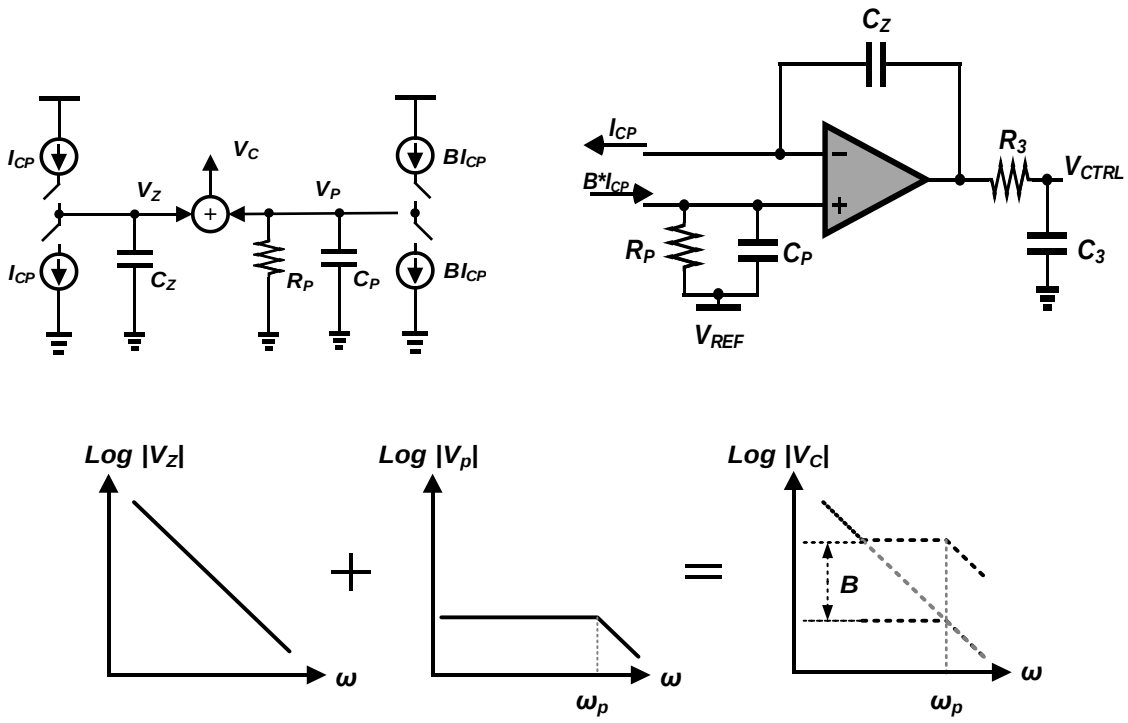



Figure 2- 10 Dual Pass Loop Filter Theory and Implemetation

### 2.2.3 Frequency Divider

The frequency divider divides the VCO output frequency by N to make it comparable to the reference frequency [12]. The expression in (2-6) shows the relationship between the VCO frequency ($f_{VCO}$) and the divider output frequency ($f_{DIV}$).

$$f_{VCO} = N \times f_{DIV} \qquad 2-6$$

Integrating both sides gives the phase representation (2-7)

$$\theta_{VCO} = N \times \theta_{DIV} \qquad 2-7$$

Phase transfer function of loop divider therefore is

$$\frac{\theta_{DIV}(s)}{\theta_{VCO}(s)} = \frac{1}{N} \qquad 2-8$$

### 2.2.4 Voltage Controlled Oscillator

The VCO output frequency in radians per second is given by

$$\omega_{VCO} = \omega_0 + K_{VCO} \cdot V_{CTRL} \qquad 2-9$$

Where $\omega_0$ is the free running frequency of the VCO, $K_{VCO}$ is the VCO gain and $V_{CTRL}$ is the loop filter control voltage. The phase deviation of the VCO output frequency from the free running frequency is given by the control voltage multiplied by the VCO gain (2-10)

$$\theta_{VCO} = \int_{-\infty}^{t} (\omega_{VCO} - \omega_0)dt = \int_{-\infty}^{t} K_{VCO} V_{CTRL}(t)dt \qquad 2-10$$

In the S-domain equation (2-10) above becomes

$$\theta_{VCO}(s) = \frac{K_{VCO}(s)V_{CTRL}(s)}{s} \qquad 2-11$$

$$\frac{\theta_{VCO}(s)}{V_{CTRL(s)}} = \frac{K_{VCO}(s)}{s} \qquad 2-12$$

**2.3 System Transfer Functions**

The open loop transfer function, GH(s), with the dual path loop filter transfer function is shown in (2-13). From this transfer function, we can find the loop bandwidth and phase margin which gives an idea of the stability of the system.

$$GH(s) = \frac{K_{PD}K_{VCO}}{s^2} \cdot \frac{1 + s(C_P + B \cdot C_Z) \cdot R_P}{sC_Z \cdot (1 + sC_PR_P)} \cdot \frac{1}{1 + sC_3R_3} \cdot \frac{1}{N} \qquad 2-13$$

The loop bandwidth or cross-over frequency, $\omega_c$, is given in (2-14) assuming $BC_z >> C_p$

$$\omega_c \approx \frac{K_{PD}K_{VCO}}{N} \cdot \frac{C_p + BC_z}{C_z} \cdot R_p \approx \frac{K_{PD}K_{VCO}}{N} \cdot B \cdot R_p \qquad 2-14$$

The zero frequency is placed at a factor α below $\omega_c$ and the high frequency poles are placed a factor β above $\omega_c$ to ensure stability. The two high frequency poles $\omega_p = 1/\tau_p$ and $\omega_3 = 1/\tau_3$ are made to coincide with each other for better out-of-band noise rejection while maintaining good phase margin. To further optimize for better phase noise performance, $R_3$ is made a factor of γ smaller than $R_p$ while $C_3$ is made a factor of γ larger than $C_p$. The equations calculating $R_p$, $C_p$, $R_z$, $C_z$, $R_3$ and $C_3$ are given by (2-15) to (2-19) where α = 6 and β = 4 for good phase margin > $60^0$ [14].

$$R_P = \frac{2\pi N}{BI_{cp}K_{VCO}} \cdot \omega_c \qquad 2-15$$

$$C_p = \frac{1}{6R_p\omega_c} = \frac{BI_{cp}K_{VCO}}{12\pi N\omega_c^2} \qquad 2-16$$

$$C_z = \frac{4}{BR_p\omega_c} = \frac{2BI_{cp}K_{VCO}}{\pi N\omega_c^2} \qquad 2-17$$

$$R_3 = \frac{R_p}{\gamma} = \frac{2\pi N}{BI_{cp}K_{VCO}} \cdot \left(\frac{\omega_c}{\gamma}\right) \qquad 2-18$$

$$C_3 = \gamma C_p = \gamma \frac{BI_{cp}K_{VCO}}{12\pi N\omega_c^2} \qquad 2-19$$

## 2.4 PLL Phase Noise and Loop Filter Optimization

As mentioned earlier, the noise transfer functions for the different blocks of the PLL can be derived from the linear model. This is important because it gives an idea of how the noise from each block of the PLL is affected or "shaped" by the loop and also aids in finding the phase noise contributions of the individual blocks. This information is useful in the optimization of the filter parameters to meet the area, phase error and phase noise requirements of the PLL. For the fourth order type II PLL with the DPLF implemented as the loop filter, the noise transfer functions for the reference, the two charge pumps, $R_3$ and $R_p$ in the loop filter, the loop filter opamp and the VCO are considered.

### 2.4.1 Noise Transfer Functions

Using Mason's rule, the transfer functions are as follow:

Noise at the reference:

$$NTF_{fref} = \frac{\emptyset_{OUT}}{\emptyset_{n_{fref}}} = \frac{NK_{PD}K_{VCO}(1+s\tau_z)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \quad 2-20$$

Noise at the VCO:

$$NTF_{VCO} = \frac{\emptyset_{OUT}}{\emptyset_{n_{VCO}}} = \frac{s^2C_zN(1+s\tau_P)(1+s\tau_z)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \quad 2-21$$

Charge pump 1 noise:

$$NTF_{CP1} = \frac{\emptyset_{OUT}}{i_{n_{CP1}}} = \frac{s^2C_zN(1+s\tau_P)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \cdot \frac{1}{sC_z} \quad 2-22$$

Charge pump 2 noise:

$$NTF_{CP1} = \frac{\emptyset_{OUT}}{i_{n_{CP2}}} = \frac{s^2C_zN(1+s\tau_P)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \cdot \frac{R_P}{1+s\tau_P} \quad 2-23$$

Noise at opamp (referred to the input of the opamp):

$$NTF_{OPAMP} = \frac{\emptyset_{OUT}}{v_{n_{OPAMP}}} = \frac{s^2C_zN(1+s\tau_P)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \quad 2-24$$

Noise from $R_3$:

$$NTF_{R3} \cong \frac{\emptyset_{OUT}}{i_{n_{R3}}} = \frac{s^2C_zN(1+s\tau_P)(1+s\tau_3)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \cdot \frac{R_3}{1+sC_4R_4} \quad 2-25$$

Noise from $R_P$:

$$NTF_{RP} = \frac{\emptyset_{OUT}}{i_{n_{RP}}} = \frac{s^2C_zN(1+s\tau_P)}{K_{PD}K_{VCO}(1+s\tau_z)+s^2C_zN(1+s\tau_P)(1+s\tau_3)} \cdot \frac{R_P}{1+s\tau_P} \quad 2-26$$

The transfer functions are plotted in MATLAB and the results are shown in Fig. 2-11 below.

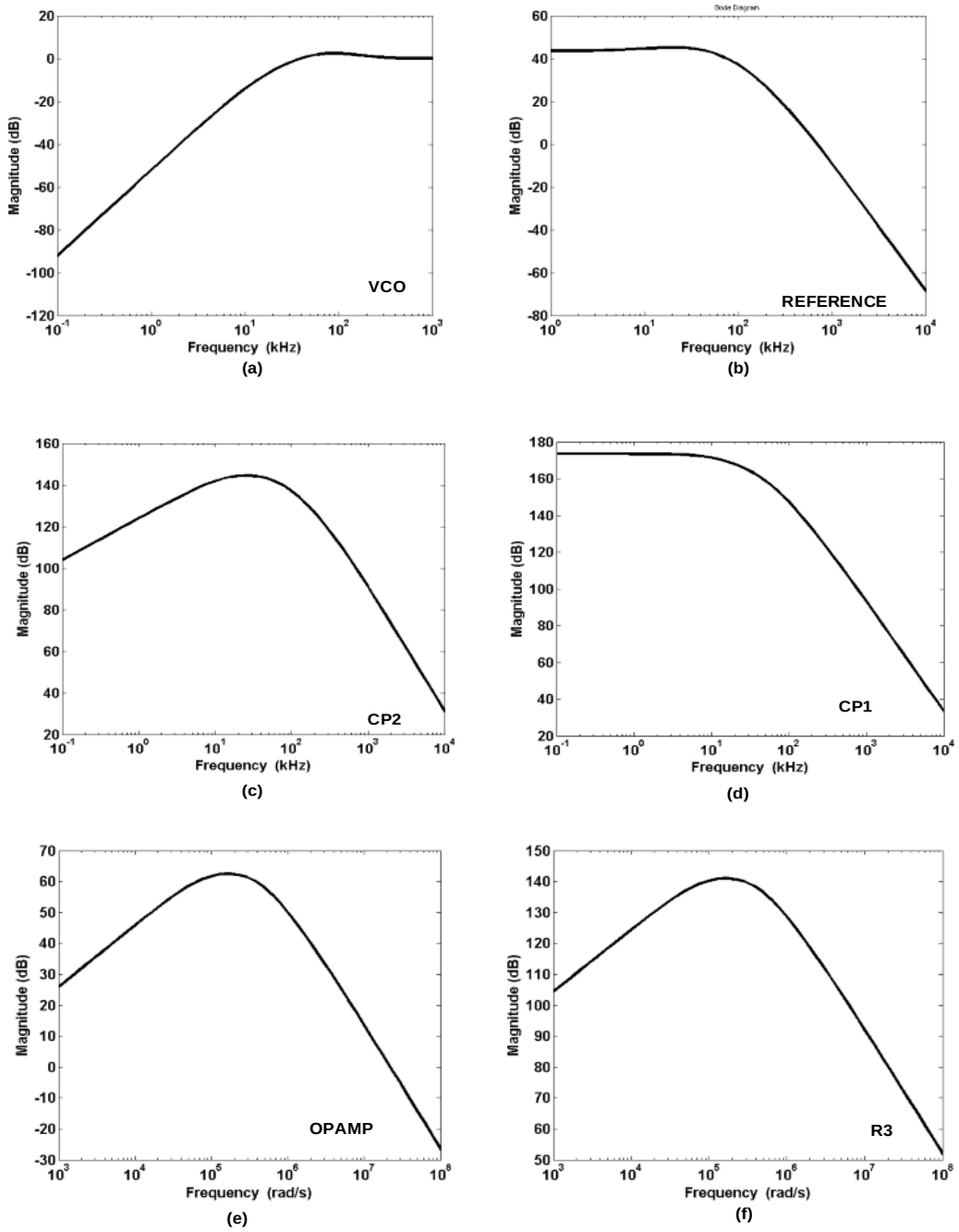
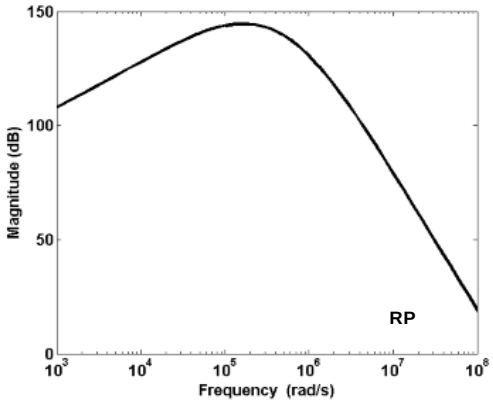



Figure 2- 11 MATLAB Simulation of the Noise Transfer Function for (a) VCO (b) Reference (c) Charge Pump 2 (d) Charge Pump 1 (e) Opamp (f) R3 and (g) RP




(g)

Figure 2-11 Continued

### 2.4.2 Loop Filter Optimization

A model of the PLL is built and simulated in the Advanced Design Systems (ADS)[2] simulator for the phase noise contributions of the different blocks of the PLL. The loop filter parameters are optimized to achieve the phase noise specification of the receiver of -120dBc/Hz at 1MHz offset and -130dBc at 3MHz for a 2.4GHz carrier while keeping the area occupied by the capacitances and phase error to a minimum. Some parameters of the PLL are fixed while others are used as variables in the optimization process. The fixed parameters are the reference frequency which is set at 32MHz and the VCO gain ($K_{VCO}$) set at $2\pi\times50$MHz for N = 150. The critical parameters which set the required phase noise, phase error and capacitance are the charge pump current, $I_{CP}$, and the loop bandwidth, $\omega_c$. The charge pump current multiplication factor

[2] www.home.agilent.com

B and $\gamma$ are additional optimization parameters. It is observed that increasing B and $\gamma$ improves the phase noise but at the expense of increased capacitance of the loop filter [15]. In this application therefore, $I_{CP}$ = 2µA, $\omega_c$ = 40kHz, B = 30 and $\gamma$ = 1.5. Table 2-1 outlines the optimized loop filter parameters and the phase noise @ 1MHz for the various blocks of the PLL. The plots for the phase noise contributions of the PLL blocks are shown in Fig. 2-12.

Table 2- 1 OPTIMIZED LOOP PARAMETERS AND PASSIVE ELEMENTS

| **Loop Parameters** | | **Passive Elements** | | **Phase Noise @ 1MHz (dBc/Hz)** | |
|---|---|---|---|---|---|
| Reference frequency | 32MHz | $R_P$ | 12.117kΩ | $L_{CP1}$ | -149.97 |
| Loop Bandwidth ($\omega_c$) | 40.76 KHz | $C_P$ | 43.78pF | $L_{CP2}$ | -177.27 |
| $K_{VCO}$ | 50MHz/V | $C_Z$ | 35.026pF | $L_{OPAMP}$ | -153.85 |
| $I_{CP}$ | 2µA | $R_3$ | 8.078kΩ | $L_{R3}$ | -148.63 |
| B | 30 | $C_3$ | 65.67pF | $L_{RP}$ | -171.99 |
| N | 2*(72—81) | $C_{TOTAL}$ | 144.476pF | $L_{FREF}$ | -139.54 |
| $\gamma$ | 1.5 | | | $L_{DIV}$ | -176.96 |
| Phase Margin | $61.5^0$ | | | $L_{VCO}$ | -126.93 |

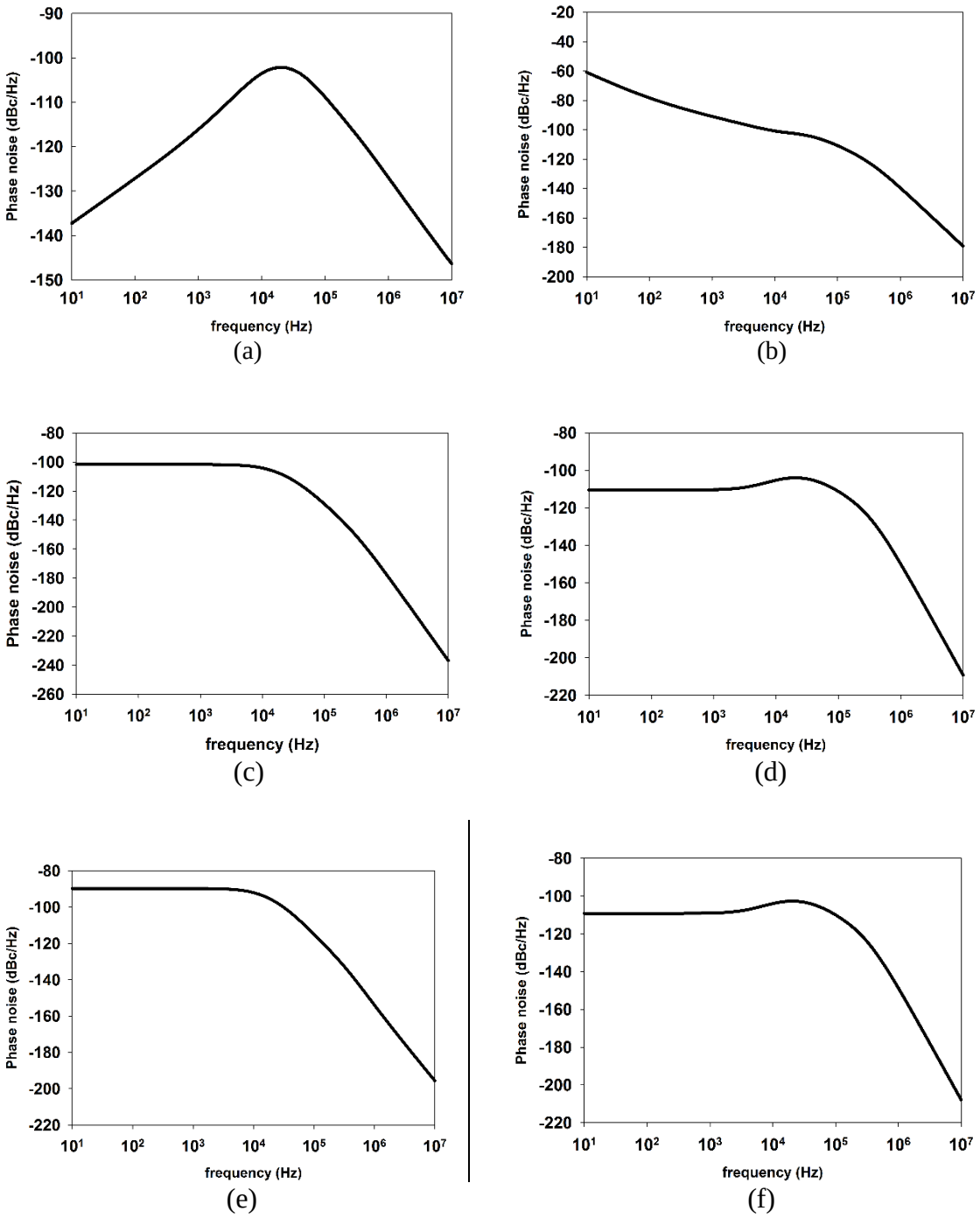
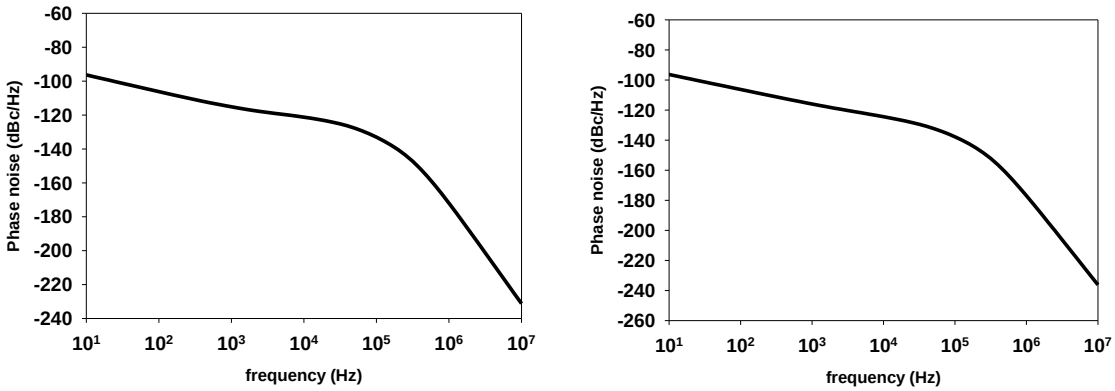



Figure 2- 12 Phase Noise Contributions for (a) VCO (b) Reference (c) Charge Pump 2 (d) Charge Pump 1 (e) Opamp (f) $R_3$ (g) $R_P$ (h) Loop Divider




(g) (h)

Figure 2-12 Continued

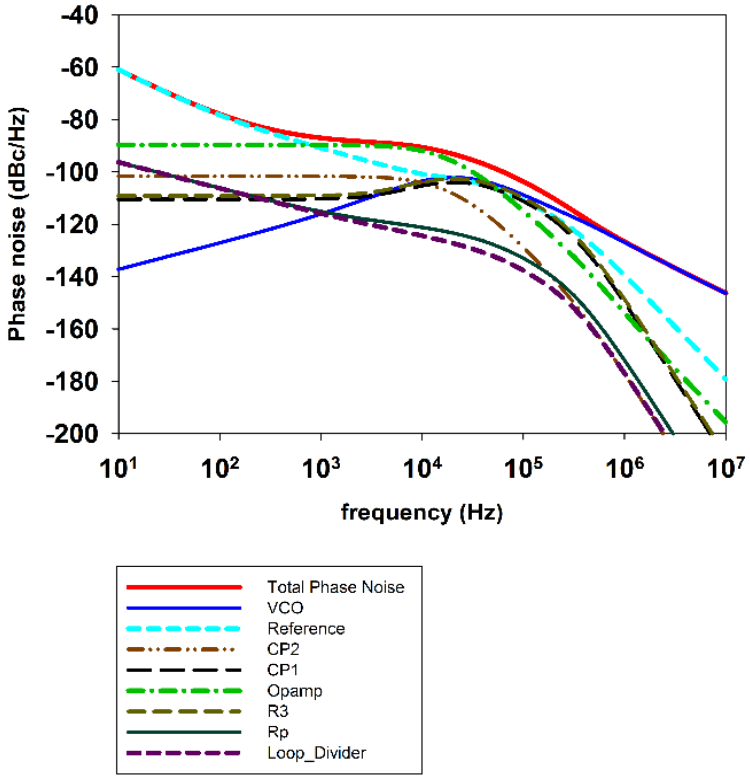



Figure 2- 13 Overall Phase Noise Contributions

Fig. 2-13 is a plot of the overall phase noise along with the contricutions from the individual blocks. The overall PLL phase noise at 1MHz is -126.64dBc/Hz and at 3MHz is around -134dBc/Hz for a 2.4GHz carrier. The loop filter is simulated and the AC response is shown in Fig 2-14. The unity gain bandwidth is 40.8kHz and the phase margin of around 61° is achieved.

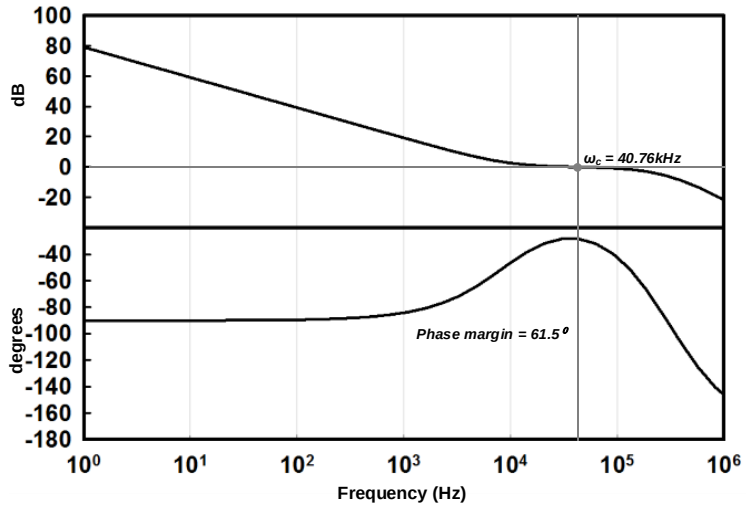



Figure 2- 14 AC Response of Loop Filter

# 3. PLL IMPLEMENTATION – PHASE I

In this section, the first phase of the implementation of the frequency synthesizer is presented. The synthesizer is implemented without the sigma-delta modulator (SDM) block, as shown in Fig 3-1. The implementation details of the VCO, frequency dividers, PFD, charge pumps, and loop filter are discussed. The synthesizer is fabricated in 0.18µm CMOS technology and measurement results are included at the end of the section.

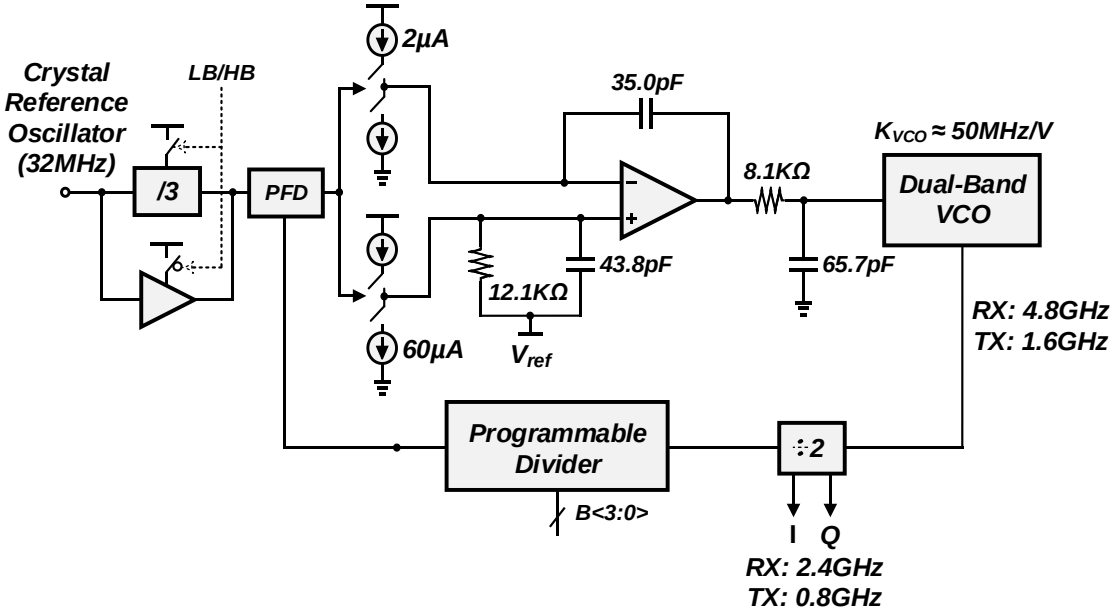



Figure 3- 1 PLL without SDM block

### 3.1 Phase Frequency Detector (PFD)

The PFD is implemented with two D-Flip Flops, a NAND gate and some delay in the reset path. The delay is made up of two inverters with load capacitors to give a total delay of approximately 2ns. The schematic of the PFD is shown in Fig. 3-2

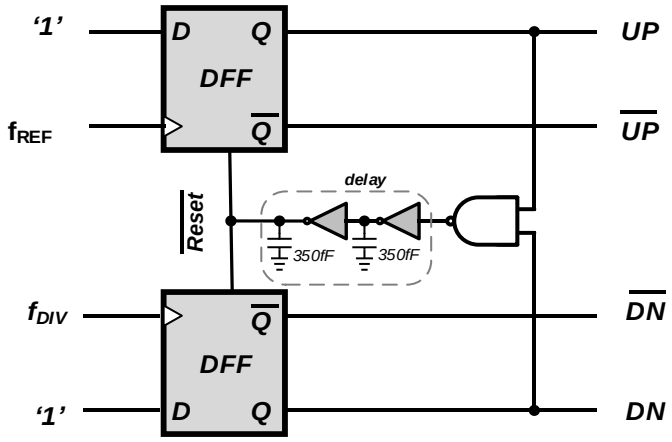



Figure 3- 2 Phase Frequency Detector Schematic

The transfer characteristic of the PFD, which is the plot of the difference between the average voltage value of the UP and DN signals versus the phase difference between them, is simulated and there is no dead-zone present because of the delay in the reset path as shown in Fig 3-3. Fig 3-4 shows the PFD waveforms when the reference signal "leads" and "lags" the signal from the frequency divider.

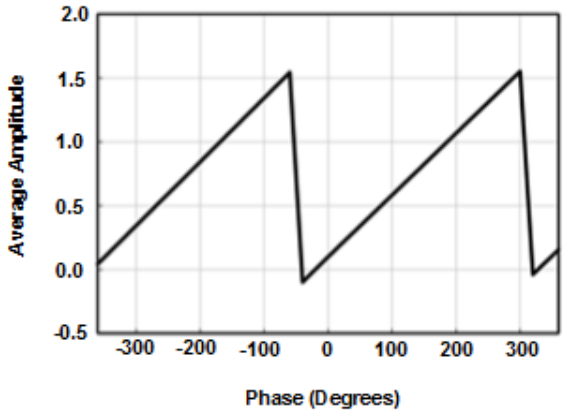



Figure 3- 3 PFD Transfer Characteristic

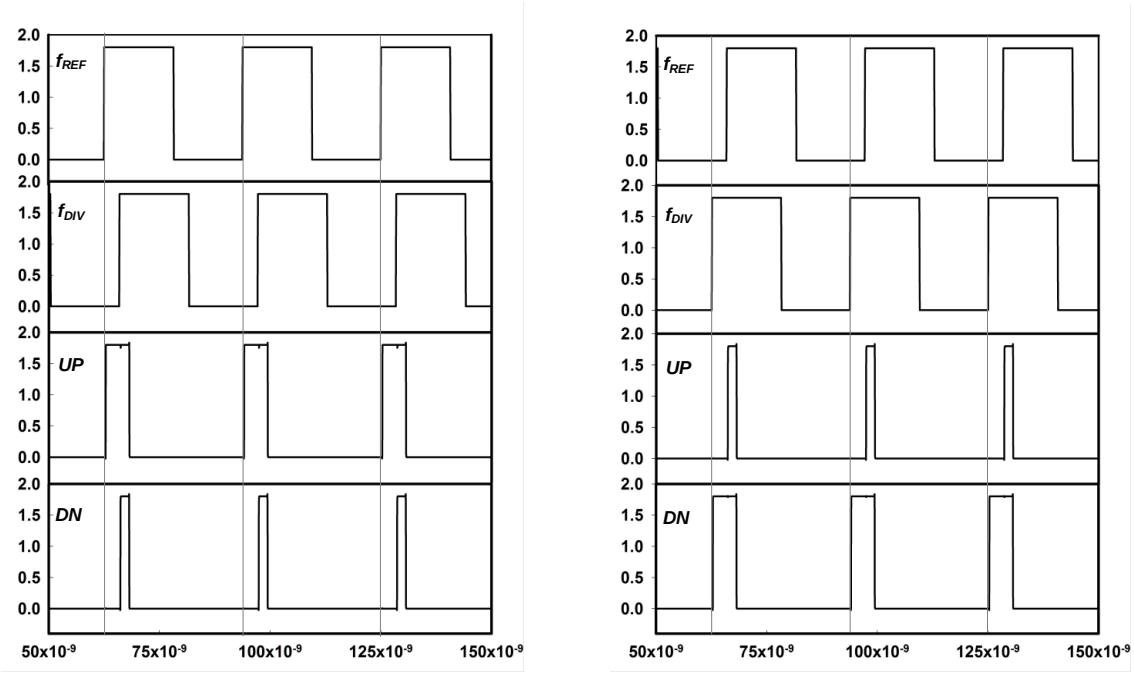



Figure 3- 4 PFD Waveforms (a) $f_{REF}$ leads $f_{DIV}$ (b) $f_{REF}$ lags $f_{DIV}$

### 3.2 Charge Pump

The charge pump is required to sink and source current into the loop filter based on the PFD outputs [7]. For the implementation of the virtual zero in the dual path loop filter two charge pumps are required with one charge pump delivering current B times the other. The same architecture is used for both charge pumps and is shown in Fig 3-5. The charge pumps only differ in their connections to the PFD $UP, \overline{UP}, DN$ and $\overline{DN}$ signals[12] and the currents they deliver.

The transistors *Mn1a* and *Mp1a* form the main switches for the charge pump and are controlled by the PFD $UP$ and $\overline{DN}$ signals, respectively. A dummy branch consisting of *Mn1b* and *Mp1b* is included to prevent glitches which result in ripples on the control voltage. The dummy switches are controlled by the complements of the signals controlling the main switches. The glitches are caused by the voltage difference between the $V_{OUT}$ node and the nodes $m_1$ and $m_2$ when *Mn1a* and *Mp1a* are switched on and off. The dummy branch ensures that nodes $m_1$ and $m_2$ are kept relatively stable when the main switches are turned on and off by providing a path for the current to flow even when the main charge pump switches are off. The nodes at $V_{REF}$ and $V_{OUT}$ are kept equal with the action of the opamp in the active loop filter configuration when the loop is locked [12].This helps to limit the output swing of the charge pumps and hence reduces the mismatch between $I_{UP}$ and $I_{DN}$.

Switches *Mn2a, Mn2b, Mp2a* and *Mn2b* are complementary switches which are used to generate complementary charge to cancel out glitches due to charge injection and clock feed through from the charge pump and dummy switches.

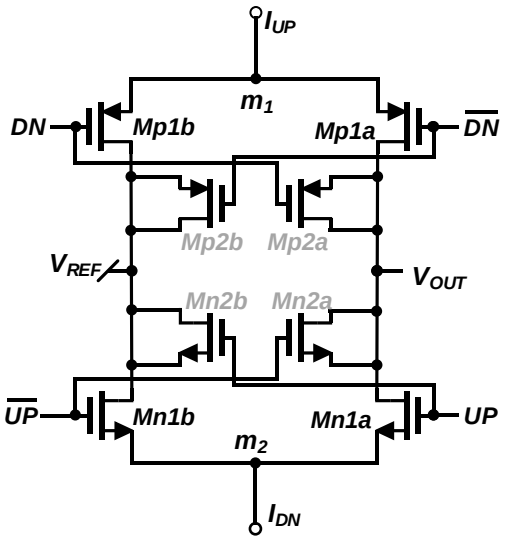



Figure 3- 5 Charge Pump Schematic

### 3.2.1 Programmable Charge Pump Bias

The $I_{UP}$ and $I_{DN}$ currents for the two charge pumps are provided by a programmable current source (Fig. 3-6) and a fixed current source (Fig. 3-7) to be able to adjust the current ratio B. The programmable source is controlled by the control bits cp<3:0> and it changes in steps of 10 µA. The programmability of the charge pump current makes it easier to control the loop parameters and compensate for PVT variations in the PLL.

The programmable charge pump is simulated for all values of the bias control, cp<3:0> and the simulation result shown in Fig. 3-8. From the plot the bias current varies linearly with the programmable control between setting $0101_2$ and $1111_2$.

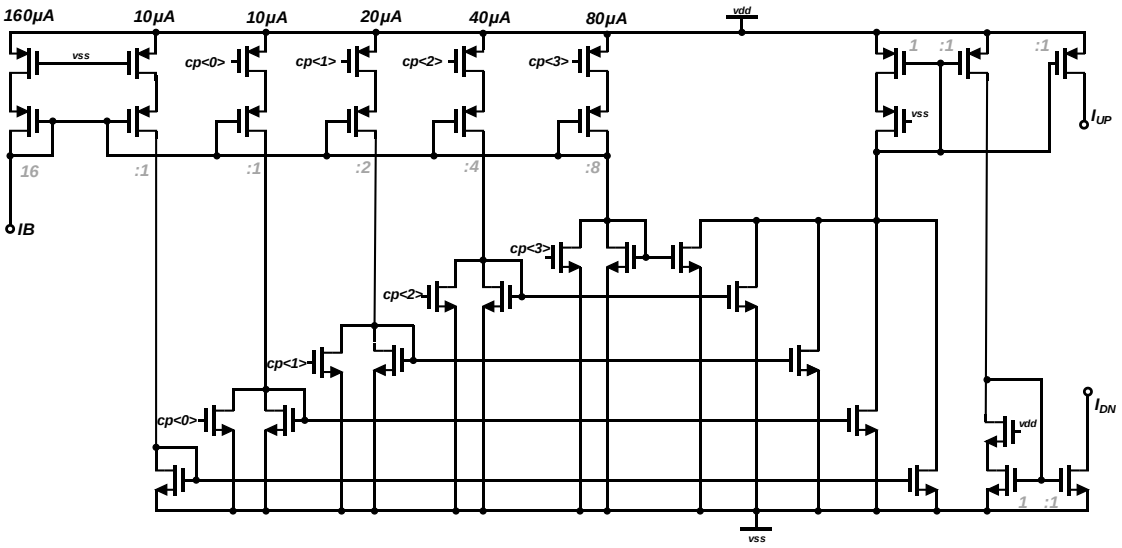



Figure 3- 6 Programmable Charge Pump Bias

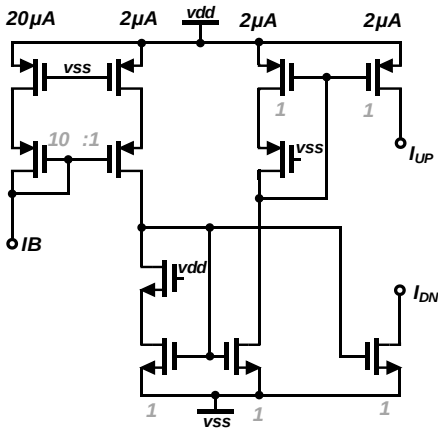



Figure 3- 7 Fixed Charge Pump Bias

The value of current for the charge pump, $I_{cp}$, is chosen to be 2µA and the scaling factor B chosen to be 30. Therefore, the programmable charge pump current for the loop parameters is set to be 60µA as shown in Fig. 3-8.

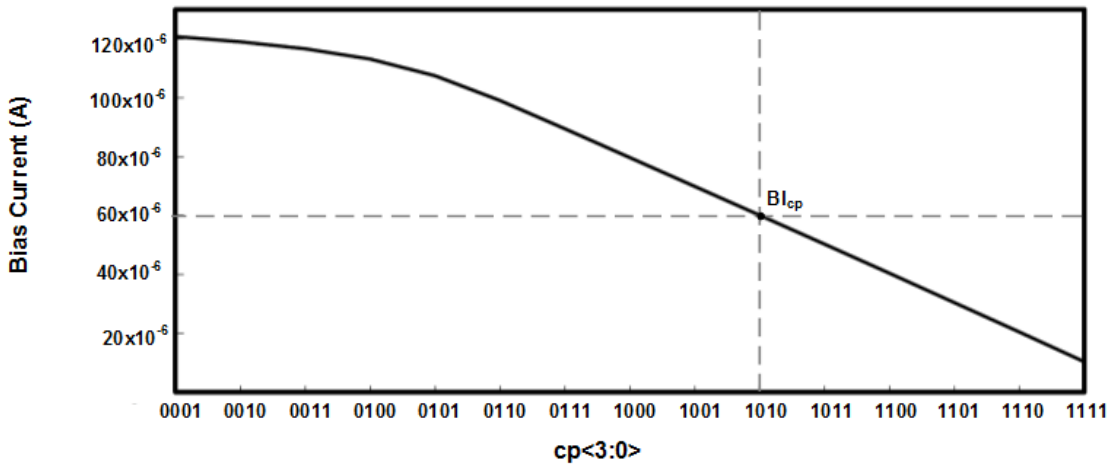



Figure 3- 8 Programmable Charge Pump Bias Currents

### 3.3 Dual Path Loop Filter

The architecture for the loop filter showing the connections to the charge pumps is shown in Fig 3-9. The first charge pump receives its bias current through $I_{UP1}$ and $I_{DN1}$ from the fixed bias current source and delivers a current ($I_{CP}$) of 2µA to the loop filter. The second charge pump delivers a current ($B*I_{CP}$) of 60µA and it receives its bias current from the programmable charge pump bias through $I_{UP2}$ and $I_{DN2}$.

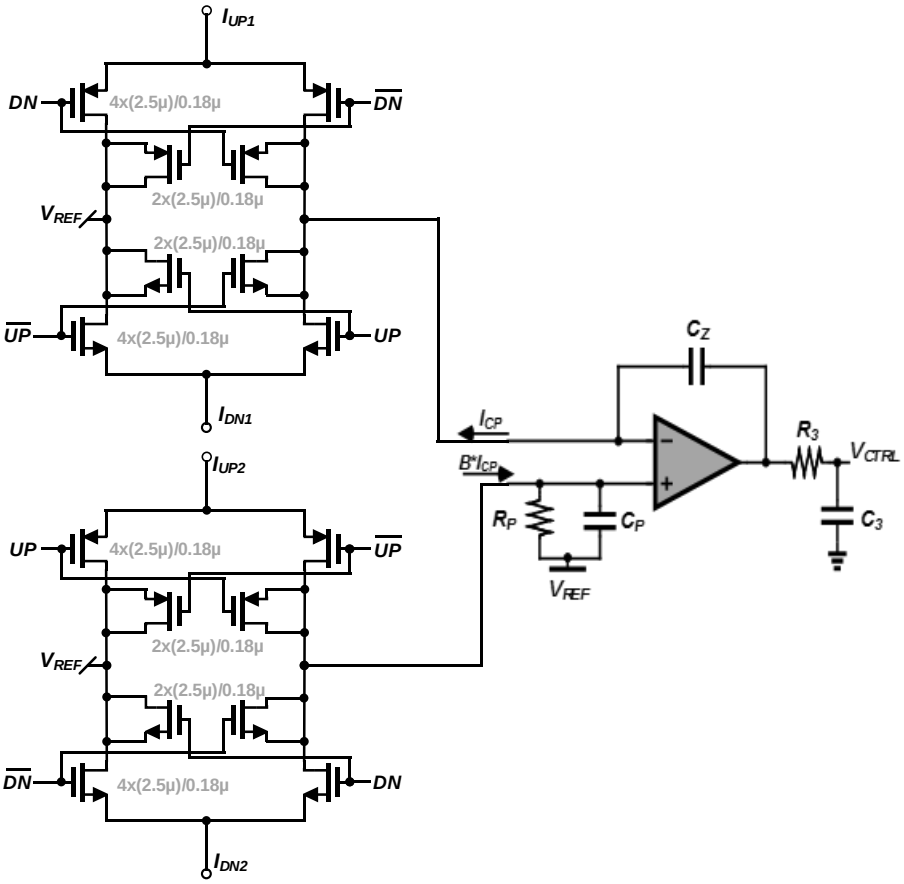



Figure 3- 9 Dual Path Loop Filter with Charge Pumps

In the analysis of the dual-path loop filter in section II, the opamp is assumed to be ideal with infinite gain and bandwidth. However in the actual implementation, the effect of finite gain and bandwidth of the opamp is considered. In the following analysis, the opamp is modeled first with finite gain as $A(s) = A(0)$, where A(0) is the DC gain of the amplifier. The output voltage of the opamp is given by

$$V_0 = A(s)[V_p - V_z] \qquad 3-1$$

This yields an overall transfer function for the DPLF of

$$\frac{V_0}{I_{CP}} = \frac{1 + s(BC_z + C_p) \cdot R_p}{sC_z(1 + sC_pR_p)\left(1 + \frac{1}{A(0)}\right)} \cong \left(\frac{1 + s(BC_z + C_p) \cdot R_p}{sC_z(1 + sC_pR_p)}\right)\left(1 - \frac{1}{A(0)}\right) \qquad 3-2$$

Thus to design for an output error ($\varepsilon < 1\%$), the gain required is calculated as follows:

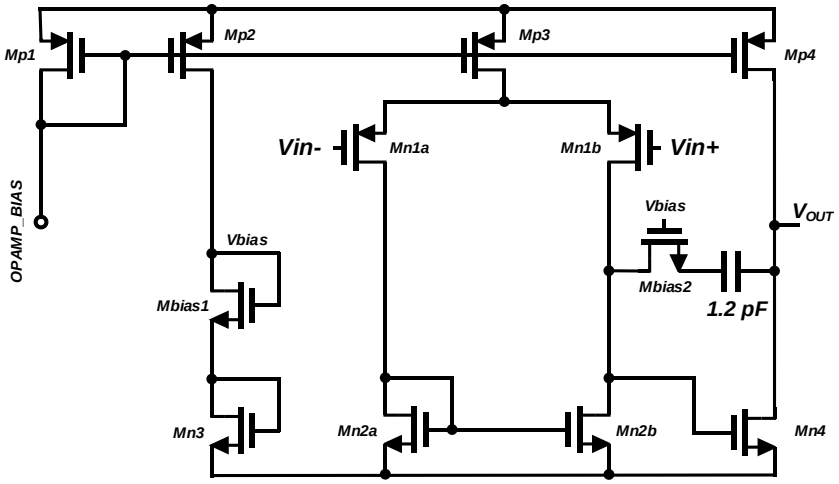
$$\varepsilon = \frac{1}{A(0)} < 0.01 \qquad 3-3$$

$$A(0) > 100V/V \; or \; 40dB \qquad 3-4$$

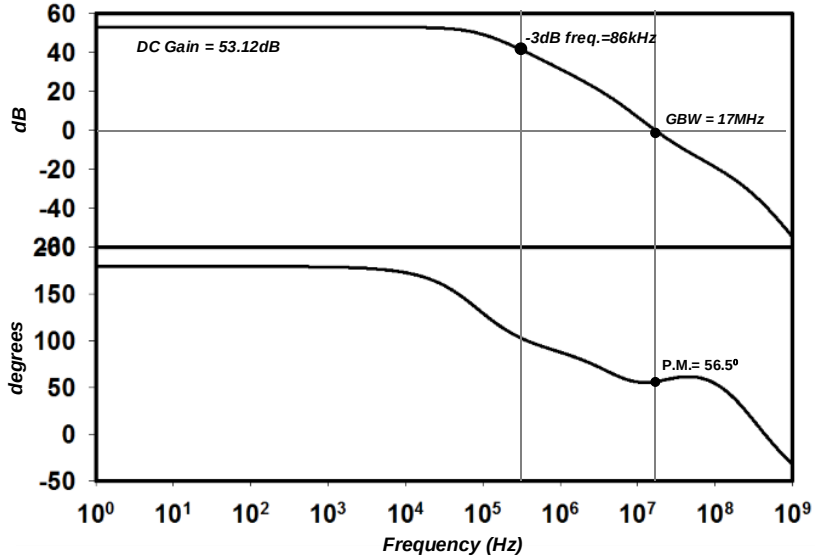
The DC gain required for the opamp is at least 40dB, and the 3-dB bandwidth is designed such that it is greater than the PLL loop bandwidth. The schematic of the opamp and its frequency response are shown in Fig. 3-10 (a) and (b). A two stage opamp is used in order to maximize the output swing and provide a wide range for the VCO control voltage. Another key issue with the active implementation of the filter is the noise produced by the transistors. To minimize the noise contribution of the opamp, relatively large sized PMOS input devices are used. It is known that PMOS devices have a lower flicker noise coefficient for a particular technology, and that large gate area minimizes the flicker noise effect. The flicker noise of a MOSFET transistor is given as:

$$\overline{i_n^2} = \frac{K_f}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \Delta f \qquad 3-5$$

Where $K_f$ is the flicker coefficient, f is the frequency, $g_m$, W, L and $C_{ox}$ are the transconductance, width, length and gate oxide capacitance per unit area.




(a)




(b)

Figure 3- 10(a) OPAMP Schematic (b) AC Response

Table 3-1 summarizes the performance of the opamp

Table 3- 1 OPAMP PERFORMANCE SUMMARY

| **Parameter** | **Cload = 35pF** |
|---|---|
| Gain (dB) | 53.12 |
| BW (MHz) | 17.08 |
| Phase margin ($^{o}$) | 56.52 |
| Slew Rate +/-(V/μs) | 1.42/-57.03 |
| ICMR (V) | 1.73 |
| Output Swing ($V_{pp}$)* | 1.788 |
| Power Consumption (μW) | 258.7 |

### 3.4 Frequency Dividers

#### 3.4.1 Divide – By – Three Reference Frequency Divider

In order to simplify the design of the programmable divider considering the dual band VCO design, two different reference frequencies (32MHz and 32/3 MHz) are chosen for the two modes (4.8GHz and 1.6GHz, respectively). A divide-by-three circuit[7], Fig. 3-11,is used to maintain the divide ratio of the programmable divider when the VCO frequency is switched from RX mode to TX mode. The circuit is made up of two D-flip flops, a NAND gate and an INVERTER. The circuit operates as follows: assuming an initial condition of LOW or '0' at the input of the AND gate G, during the first clock cycle, $f_{OUT}$= '0'. One of the inputs of G is HIGH or '1' and the input of $DFF_A$ is also '1'. In the second clock cycle, the output of G (which is '0') is passed to $f_{OUT}$. The HIGH input of $DFF_A$ is passed to its output and both inputs of G are HIGH. In the third clock cycle, the HIGH output of G is passed to $f_{OUT.}$ Thus, for every

three clock cycles, there is one pulse for the output, implementing the divide by 3 operation.

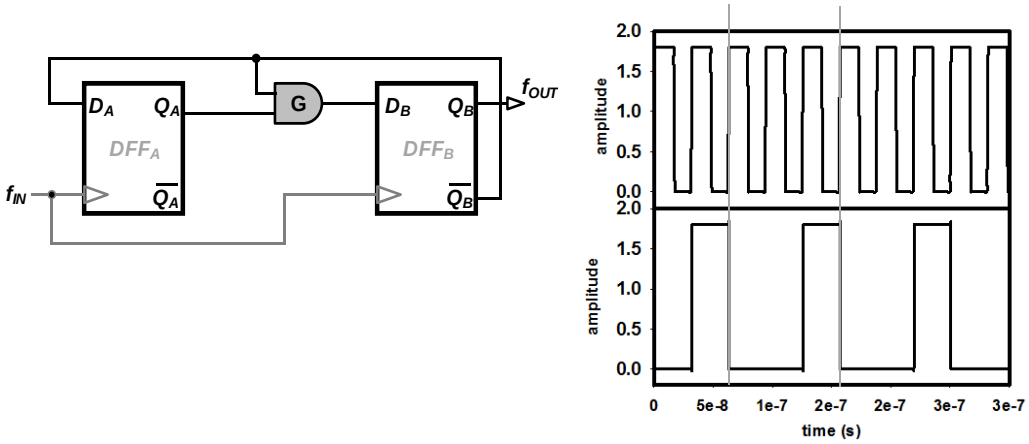
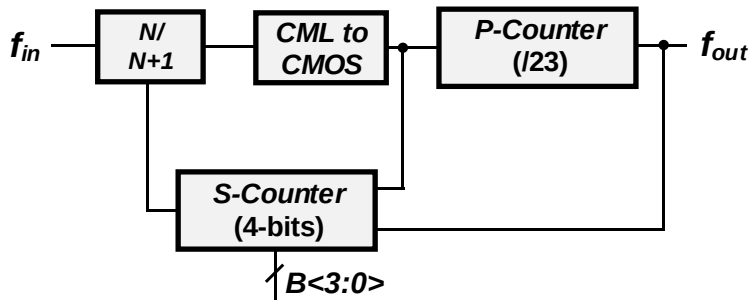



Figure 3- 11 Schematic of Divide-by-Three Circuit and Waveforms

Hence, for the input signal running at 32MHz and the output signal is divided by 3 to give 10.667MHz as shown in Fig. 3-11.

### 3.4.2 Programmable Divider

The pulse-swallow architecture is used for the frequency divider, Fig 3-12. It is made up of a divide by N/N+1 dual-modulus prescaler, a fixed divide-by-p (program) counter and a programmable swallow (s-) counter. As a result of the high speed input to the prescaler, current mode logic (CML) blocks are used to implement the prescaler. The output swings of these blocks are not large enough to drive the p- and s- counters which require CMOS levels. A CML-to-CMOS block is used to convert the output swing of the prescaler to CMOS logic levels for the p- and s- counters.




$N_{int} = NP + S = 3x23+\{0,1,\ldots,15\} = \{69,70,\ldots,84\}$

Figure 3- 12 Pulse Swallow Divider Architecture

In general, the divider operates as follows: the s-counter is loaded with S =(0 to 15) represented by 4 bits (B<3:0>) and sets the prescaler to divide by (N+1), S times.

With P > S, the prescaler divides by N, the remaining P – S times. Thus the overall divide ratio, $N_{int} = (N + 1)S + (P - S)N = NP + S$.

*3.4.2.1 Dual Modulus Prescaler Design*

The schematic of the dual modulus (N/N+1) prescaler is shown in Fig. 3-13. The value of N = 3. The prescaler divides by 3 or 4 depending on the input to the modulus control (MC) port. When MC is logic level HIGH or "1", the OR gate always outputs a '1'. As a result, the output of the AND gate passes the output of $DFF_A$to the input of $DFF_B$. Each DFF is made up of two latches. With MC HIGH,the prescaler has the four latches in a loop and this achieves the divide-by-4 operation. When MC is LOW, the circuit implements the divides-by-3 operation [7].

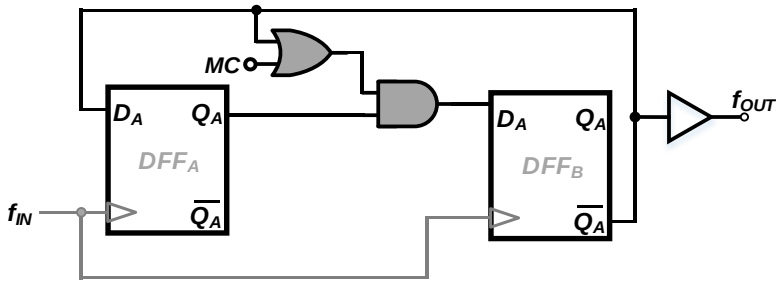



Figure 3- 13 Prescaler Schematic

Since the maximum input frequency to the prescaler is in the 2.4GHz range, CML flip-flops and logic gates are used in the design because they can operate at high speeds [16,17]. The first DFF is made of two cascaded CML latches, Fig 3-14. The AND operation is embedded into the second DFF by using the CML-Latch (AND) block, Fig. 3-15, as the first latch in the cascade. This is done to save the area and static power a separate CML-AND gate would have contributed. The circuits in Fig 3-14 and 3-15 omit the tail current source to make it possible to use low supply voltages. However, to define accurate bias currents, the clock pair is biased with a current mirror and the CLOCK signal is capacitively coupled. The bias circuit is shown in Fig. 3-16. The value of the coupling capacitors is 5 to 10 times the clocked pair's input gate capacitance to prevent attenuation of the clock signal amplitude [7]. The CML-(N)OR gate is implemented with the circuit in Fig. 3-17.

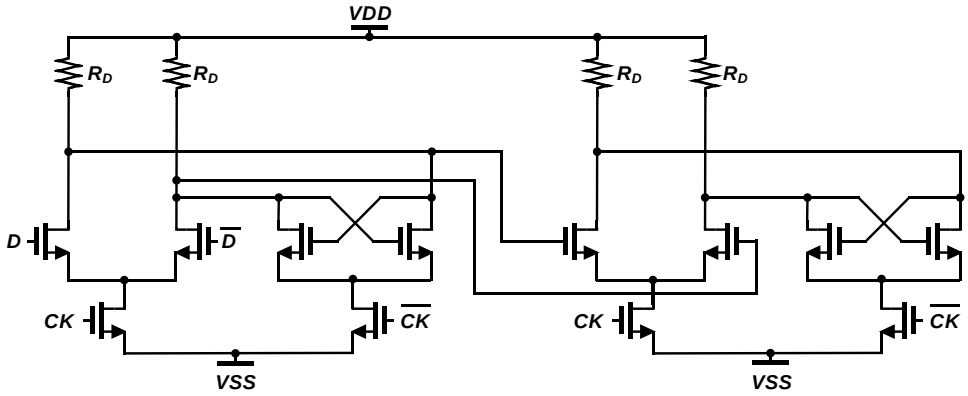



Figure 3- 14 CML-DFF

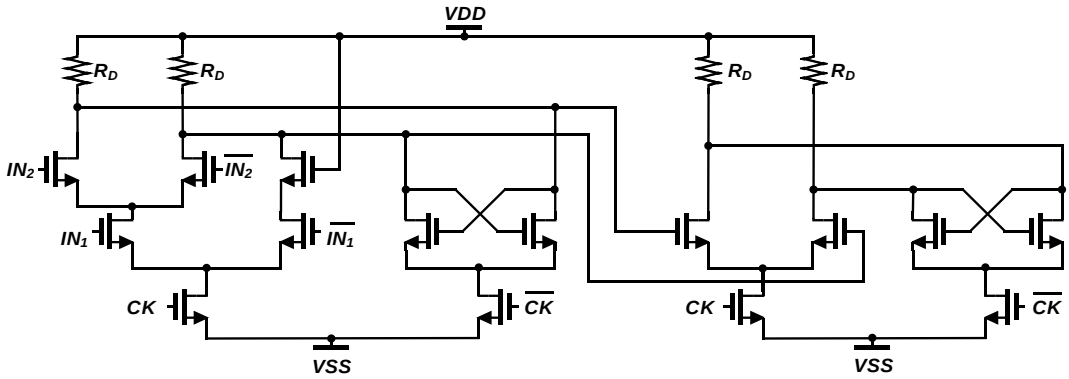



Figure 3- 15 CML – DFF with embedded AND gate

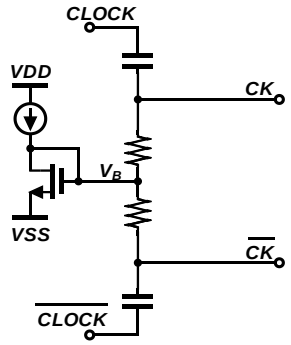



Figure 3- 16 Bias Circuitry for CML Latches

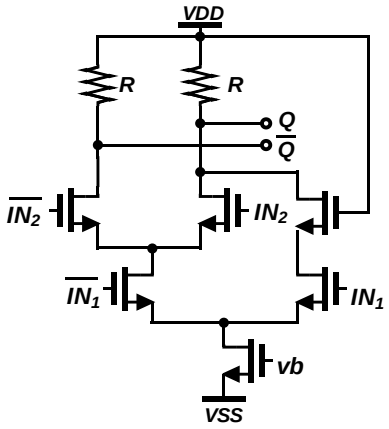



Figure 3- 17 CML (N)OR GATE

Fig. 3-18 shows how MC sets the prescaler to divide by four when MC is HIGH and to divide by three when MC is LOW.

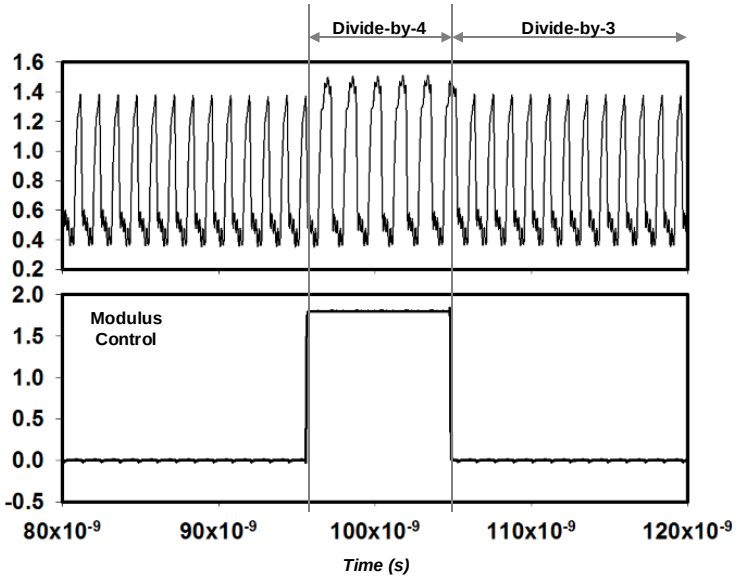



Figure 3- 18 Prescaler Output: Divide-by-4 Operation when MC = 1 and Divide-by-3 Operation when MC = 0

*3.4.2.2 CML-to-CMOS Design*

The output swings of the CML blocks are not large enough to drive the p- and s-counters which require CMOS levels. The CML to CMOS circuitis used totransform the output swing levels of the prescaler to CMOS levels for the p- and s counters to operate properly[16]. The CML to CMOS schematic is shown in Fig 3-19(a). The capacitors at the input of the converter serve as coupling capacitors to block the DC level from the prescaler output.After the coupling capacitors is the pair of self-biased inverters. The digital CMOS inverter is made to operate as an analog amplifier by connecting a resistor in negative feedback between the input and output. This causes the inverter to be biased at its trip point (point A in Fig. 3-20) where it has the highest gain. [17]

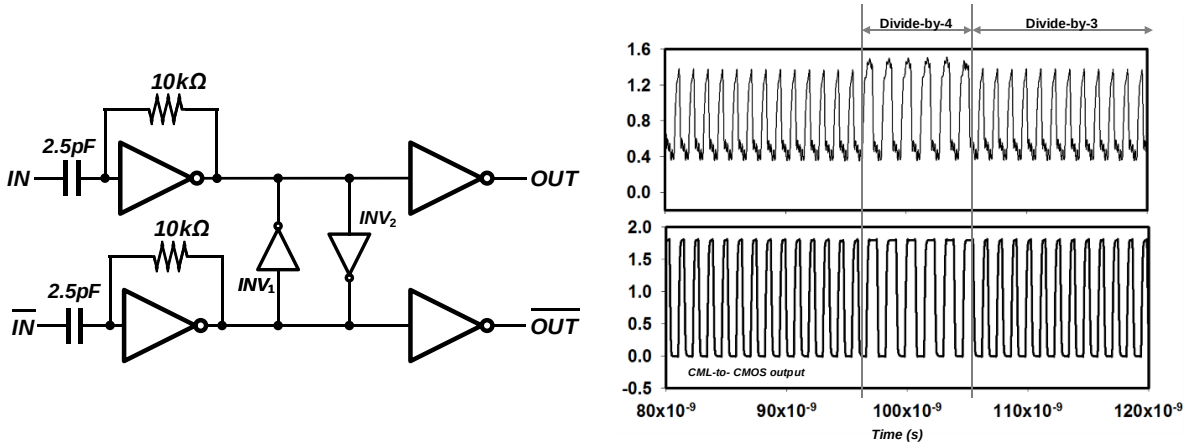



Figure 3- 19 (a) CML to CMOS Converter (b) CML Level Input and CMOS Level Output

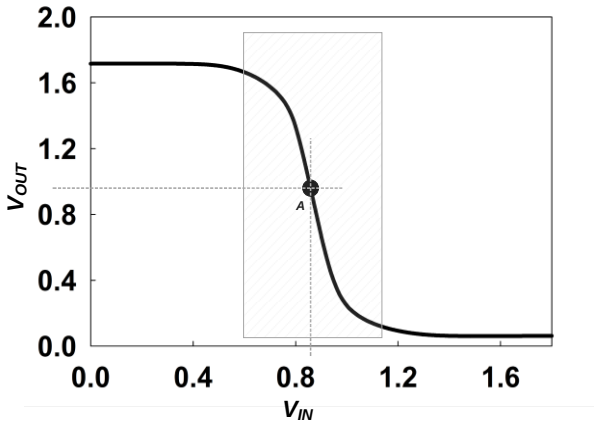



Figure 3- 20 Simulated Transfer Characteristic of Self-Biased Inverter

The simulation results in Fig. 3-19(b) show the input to the CML to CMOS circuit which is the output of the prescaler and the CMOS level waveform after the conversion. The swing for the CML circuit is about 1V and the single ended output of the CML to CMOS is from 0V to 1.8V.

*3.4.2.3 Program Counter Design*

The P-Counter in this case is a 5-bit asynchronous counter shown in Fig 3-21. This architecture is used because of its simplicity and low power consumption[12, 18]. The D-Flip Flops (DFFs) used in the counter are Loadable TSPC Flip-Flops [18], as shown in Fig 3-22. The counter inputs P<4:0> are set to binary $10110_2$ for the counter to count from 22→0 to realize the divide-by-23 operation. The combinational circuitry (consisting of NOR, NAND and INVERTERS) with the NOR-embedded D Flip-Flop (NORDFF), Fig. 3-23(b), are used to reset the counter after the final state [18].

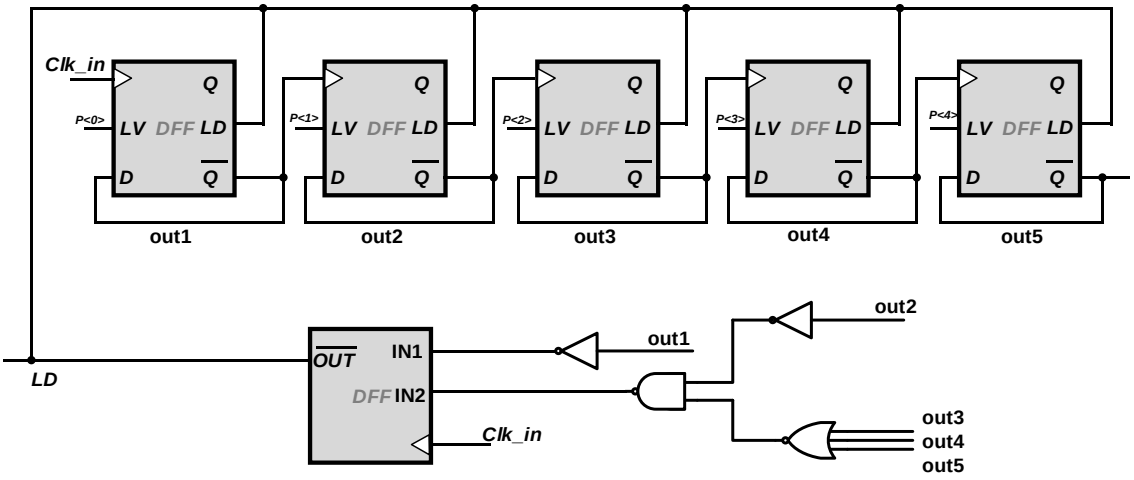



Figure 3- 21 Program Counter

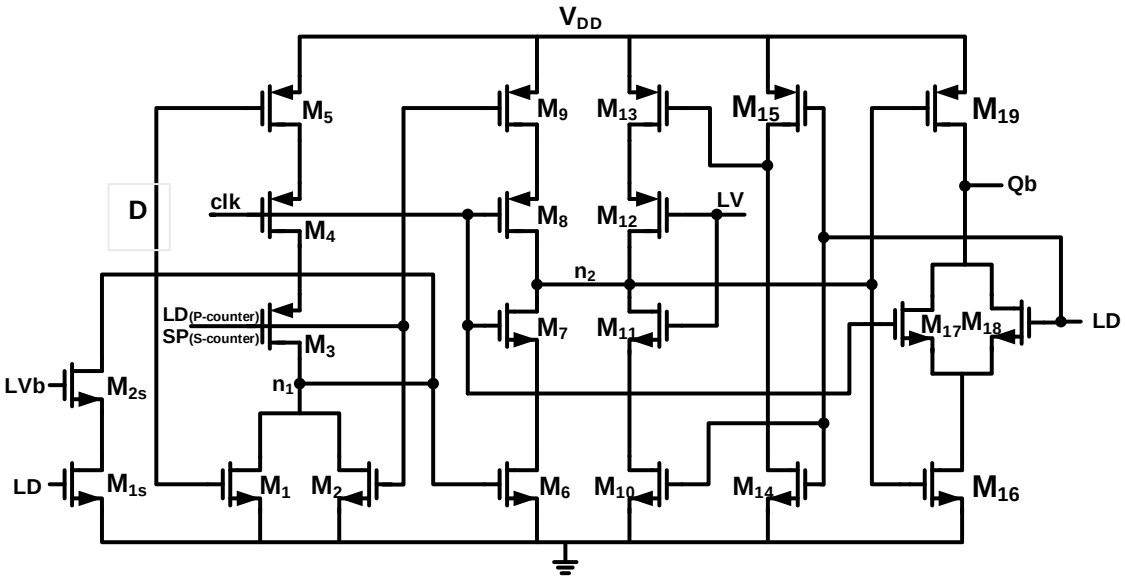



Figure 3- 22 Loadable TSPC D Flip-Flop

In Fig. 3-22, when LD is “0”, nodes n1 and n2 are precharged to $V_{DD.}$ At the rising edge of the clock, M7 and M17 are turned on. M6 is already turned on by the voltage at node n1 and this provides a path to ground for node n2. The output Qb is “1” after the rising clock edge regardless of the state of LV.

When LD goes to “1”, the node n1 is pulled to ground by $M_2$, turning off $M_6$. $M_{10}$, $M_{13}$ and $M_{18}$ are turned on as a result. When LV is “0”, node n2 is charged to $V_{DD}$ hence the output at $Q_b$ is “0”. On the other hand, when LV is “1”, node n2 is pulled to ground, hence $Q_b$ is “1”.

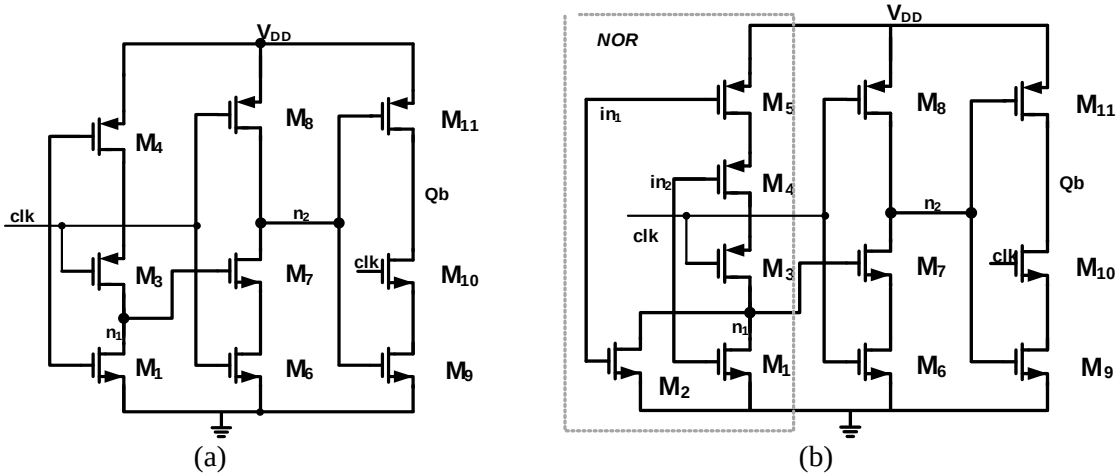



Figure 3- 23 (a) TSPC Flip-Flop (b) TSPC NOR Embedded DFF

In order to implement the NOR embedded DFF, transistors $M_2$ and $M_5$ are added to the TSPC flip-flop shown in Fig. 3-23(a)

*3.4.2.4 Swallow Counter Design*

The swallow counter is a 4 bit programmable counter which makes use of the Loadable TSPC Flip-flops and the NOR-DFF in Figs 3-22 and 3-23, respectively. The schematic is shown Fig. 3-24. The s-counter counts down from its initial value (determined by the inputs to B<3:0>) to zero and resets when the p-counter finishes its count cycle and asserts the LD signal. The s-counter provides the modulus control (MC) for the prescaler.

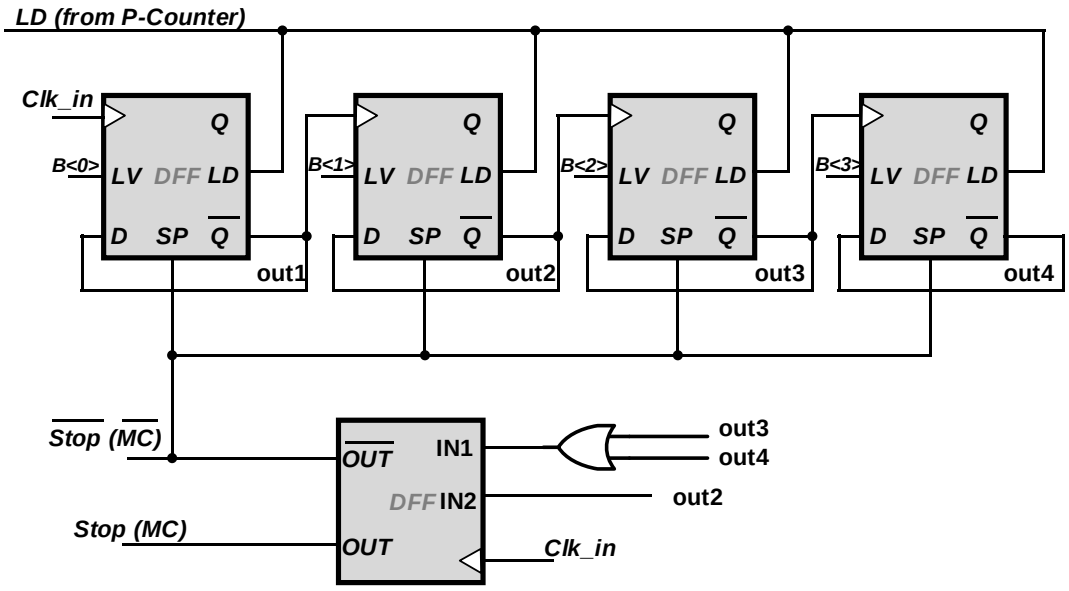



Figure 3- 24 Swallow Counter Schematic

Fig. 3-25 is the simulation result for a divide-by-75 operation. From the figure the prescaler divides by 4 for six times and then divides by 3 for the rest of the 17 times to

give $N_{int} = 4 \times 6 + 3 \times 17 = 75$. The LD signal from the p-counter is shown which resets the divider after every count cycle.

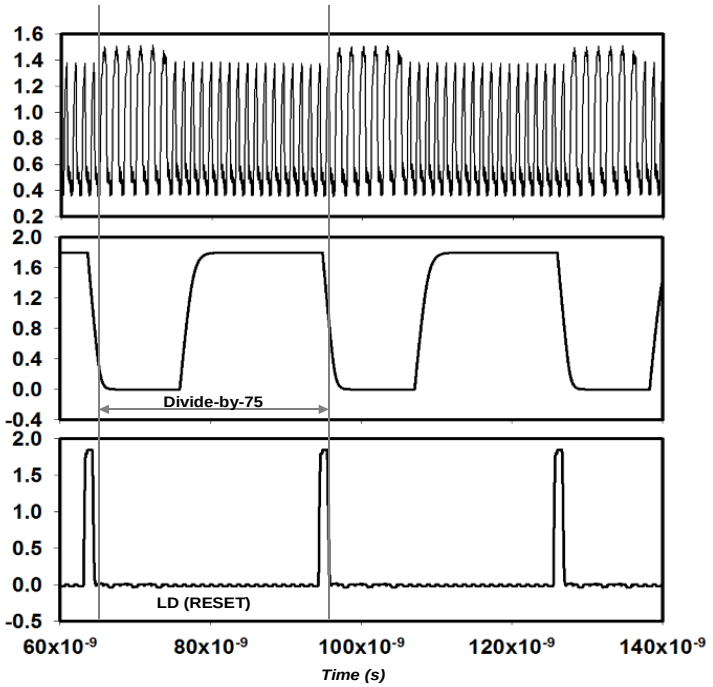



Figure 3- 25 Divide-by-75 Operation of the Frequency Divider

### 3.5 Voltage Controlled Oscillator

The VCO in this synthesizer is required to provide LO signals at two frequency bands at 1.6GHz and 4.8GHz for the TX and RX sides, respectively. A conventional LC tank oscillator would not suffice in covering this wide tuning range. One solution could be to use two VCOs optimized to operate at the two frequency bands. However, this solution is inefficient in terms of area and power consumption.

The inductance of an LC tank can be switched to generate multiple frequency bands. In this implementation, the switch resistance degrades the quality factor (Q) of the resonator and hence the phase noise of the oscillator.

Multiple frequency peaks of higher order LC tanks based on coupled inductors have been used to realize multiband or wideband VCOs [10, 19-22]. In [10], it has been shown that by taking advantage of both inductive and capacitive coupling in a $4^{th}$ order resonator, it is possible to achieve balanced operation and the same figure of merit (FoM) in the two bands. This method is used in the implementation of the dual-band VCO. Since this technique does not require any switches connected to the LC tank, it achieves a better phase noise performance. The layout is more compact because of the nesting of the inductors. The schematic of the VCO is shown in Fig. 3-26. It consists of two coupled LC tanks forming a resonator and an active switching network for selecting the desired oscillation mode.

The resonator, as mentioned earlier, makes use of both inductive and capacitive coupling to achieve a balanced operation in the two modes of oscillation. In one mode of oscillation, when there is positive coupling between the two inductors, the voltages across the LC tanks (V1 and V2) are in phase and have the same amplitude. Therefore there is no currentthrough the coupling capacitor (Cc). Thus the oscillation frequency in that mode is:

$$\omega_H = \frac{1}{\sqrt{(L+M)C_P}} \qquad 3-6$$

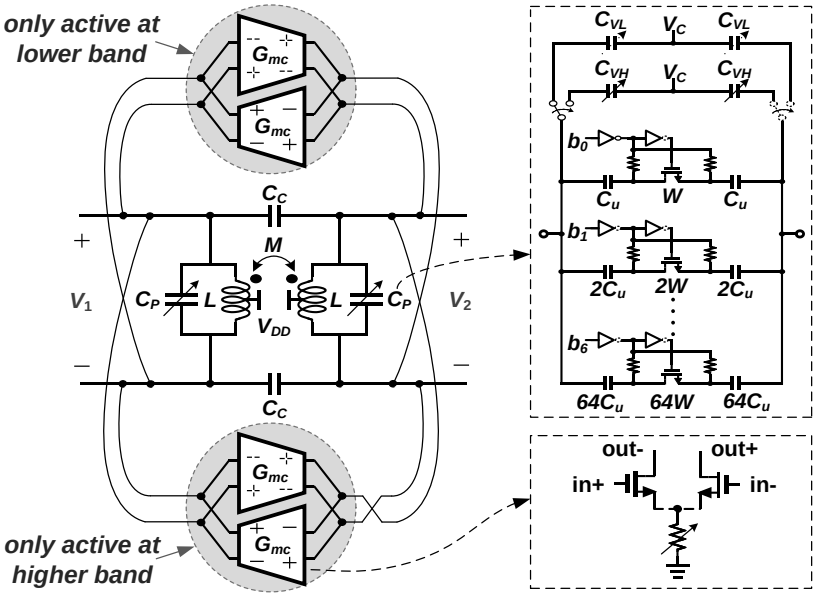



Figure 3- 26 VCO Schematic

On the other hand, when there is negative coupling between the two inductors of the resonator, the two voltages ($V_1$ and $V_2$) still have the same amplitude but are $180^0$ out of phase. Thus the effective capacitance seen in each tank is Cp + Cc and the effective inductance is L-M. The oscillation frequency therefore is

$$\omega_L = \frac{1}{\sqrt{(L-M)(C_P+C_C)}} \qquad 3-7$$

From (3-6) and (3-7) it can be seen that when M<0, both M and $C_c$ increase the separation between the two resonance frequencies. The selection of the desired oscillation mode is achieved by changing the polarity of the $G_m$ cells ($G_{mc}$) between the two ports. The $G_m$ cells are realized using NMOS differential pairs and are biased with

digitally controlled variable resistors to minimize the flicker noise contribution in the VCO.

There is a trade off between the power consumption and the phase noise performance in an LC oscillator. By choosing a small value of inductance and consuming more current, the phase noise performance can be improved. Considering a maximum power consumption of 10mW for the VCO, an inductance value of 2.3nH (4.6nH differential) was chosen. Fig 3-27 (a) shows the layout of the coupled inductors. The inner coil has 4 turns with metal width of 12μm. The outer coil has 3 turns with metal width of 15.5μm. Both are implemented in 0.18μm CMOS technology using the top metal layer (2μm thick)

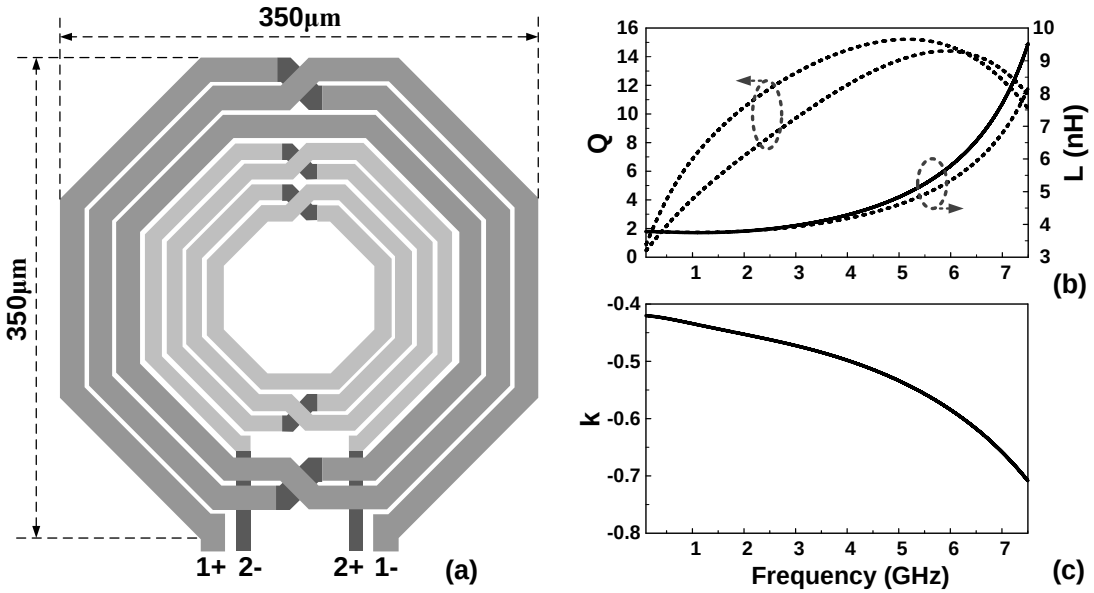



Figure 3- 27 (a) Layout of Two Coupled Inductors (b) Simulated Inductance Quality Factor Values vs. Frequency for the Internal (dashed lines) and External (solid lines) Coils (c) Simulated Coupling Factor (k) for the Coupled Inductors

In Fig. 3-27(b) and (c), the quality factor, inductance and coupling factor (k = M/L) for the two inductors are simulated using the EM simulator Sonnet[3].

In order to completely separate the two oscillation modes ($\omega_L$ and $\omega_H$), values of $k \approx -0.53$ and $C_c \approx 1.8C_{pmin}$ are chosen, where $C_{pmin}$ is the minimum value of the parallel capacitor, $C_p$.

Coarse tuning and fine tuning are used together to cover the entire tuning ranges for both modes of the synthesizer. With a 7-bit binary weighted switched capacitor bank, the coarse frequency tuning is achieved while the fine tuning is achieved by a pair of NMOS varactors. In order to preserve the overall synthesizer loop parameters, $K_{VCO}$ must be kept constant in both TX and RX modes. To this end, different varactors are used in each mode of operation. $C_{VL}$ is used in the TX mode and $C_{VH}$ in the RX mode, as shown in Fig. 3-27. The simulated VCO frequency tuning curves are shown for the RX mode and TX mode in Fig. 3-28 and 3-29, respectively.

[3] www.sonnetsoftware.com

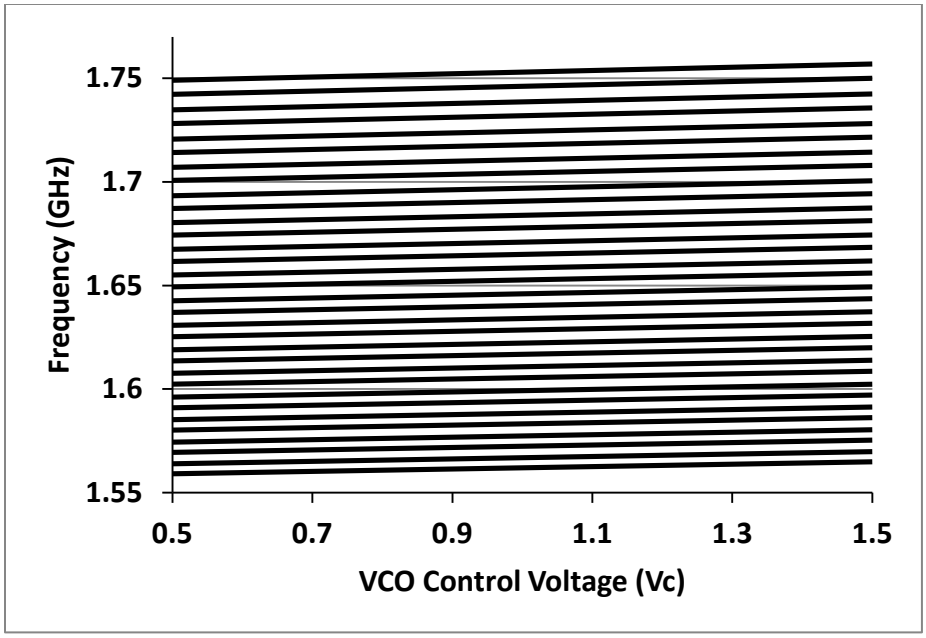



Figure 3- 28 Simulated VCO Frequency Tuning Characteristic in Lower Frequency Band

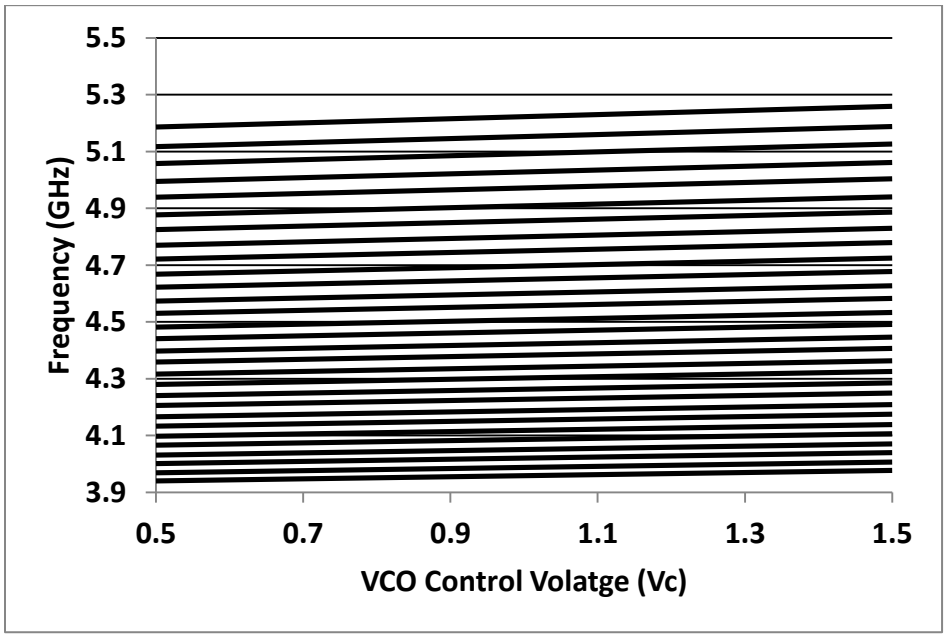



Figure 3- 29 Simulated VCO Frequency Tuning Characteristic in Higher Frequency Band

### 3.6 Measurement Results

The frequency synthesizer was fabricated in 0.18μm CMOS technologywith 6 metal layers and packaged in a 48-pin quad-flat no-leads (QFN) package. A die photo of the chip is shown in Figure 3-32. The chip active core area is 0.95mm×1.4mm.

A low phase noise signal generator (Agilent 33250A 80MHz function/arbitrary waveform generator) was used to produce the reference clock. Characterization was performed in the frequency domain with an Agilent E4446a spectrum analyzer. Figure 3-33 shows the fabricated PCBs for measuring the synthesizer performance.

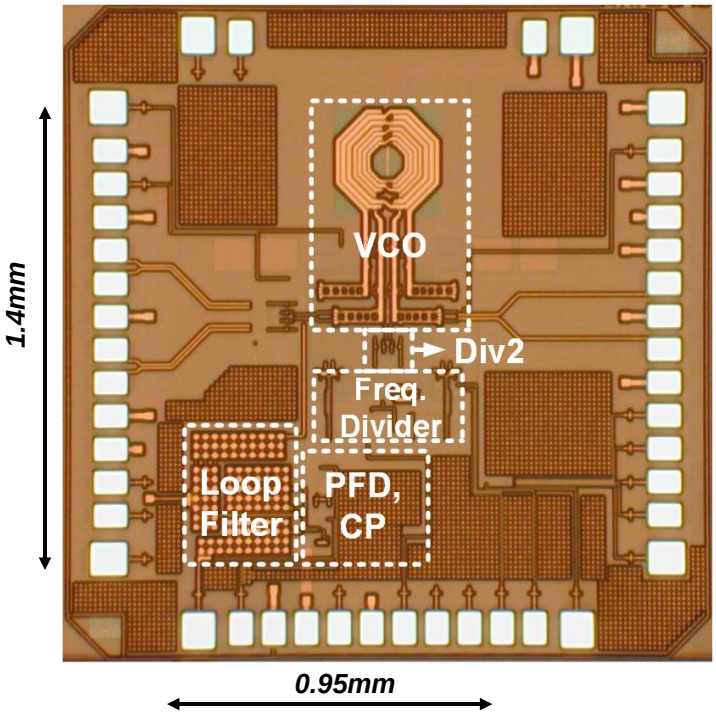



Figure 3- 30 Die Photo of the Frequency Synthesizer.

The dual-band VCO draws a current of 10 mA from a 1 V voltage supply in both modes. The measured tuning range is from 1.477 to 1.92 GHz for the lower resonant mode (LRM) mode and from 2.94 to 4.98 GHz for the high resonant mode (HRM) of the VCO and it successfully meets the required frequency tuning range for both the TX and the RX modes.

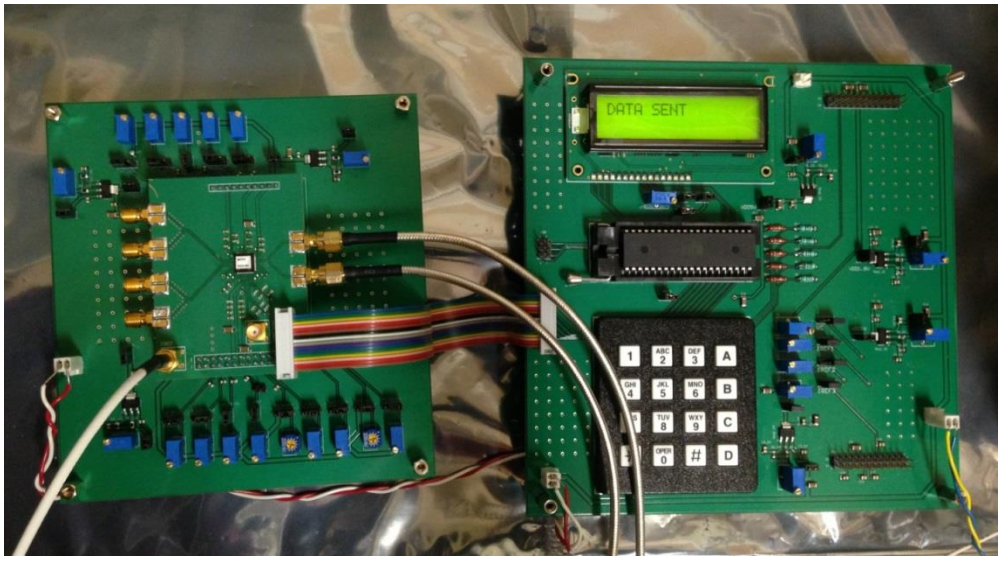



Figure 3- 31 PCBs of the Synthesizer under Test

Fig. 3-34 shows the output spectrum of the frequency synthesizer in locked condition at 1.6GHz and 4.8GHz. As can be seen, spurious levels are -72.04 dBc@10.67MHz and -75.77 dBc@32.3MHz.

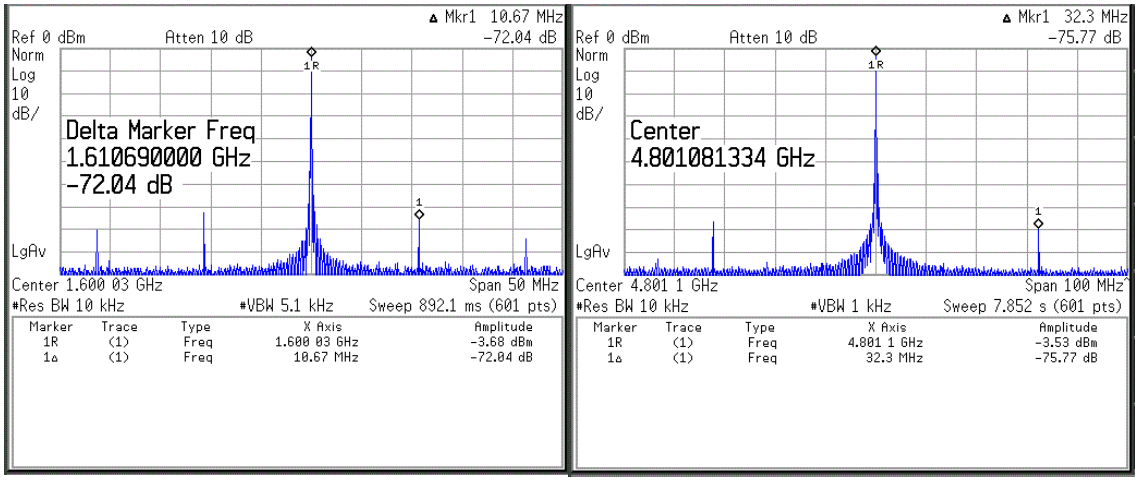



Figure 3- 32 Output Spectrum of the Frequency Synthesizer at 1.6GHz and 4.8GHz

Figs. 3-35 and 3-36 show the measured phase noise of the synthesizer at frequencies of 1.6GHz and 4.8GHz. The synthesizer achieves excellent phase noise performance of -130.83dBc/Hz and -120.16dBc/Hz at 1MHz offset from carrier frequencies of 1.6 and 4.8GHz, respectively. The close-in phase noise is measured to be about -70dBc/Hz. At very low offset frequencies, the rise in phase noise is due to the phase noise of the signal generator which is multiplied by $N^2$ (N=division factor) inside the loop bandwidth. The PLL bandwidth is around 40kHz and the worst case settling time to a 10ppm accuracy is estimated to be less than 180μs.

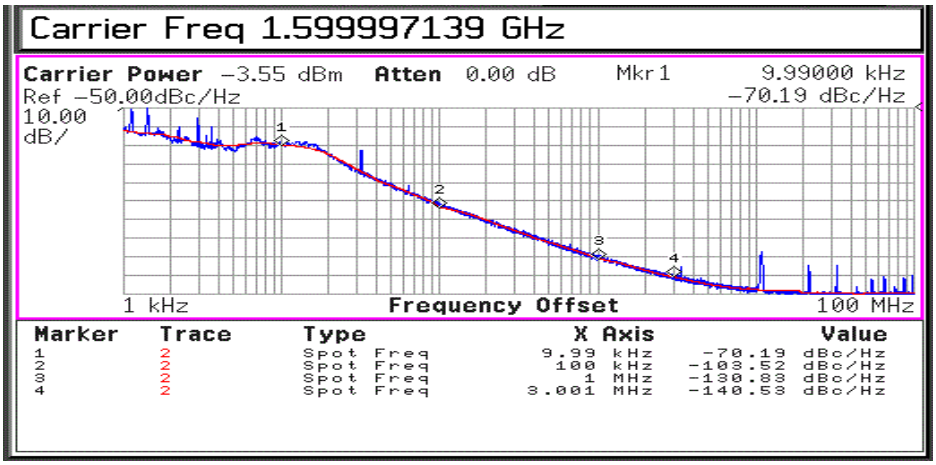



Figure 3- 33 Measured Phase Noise of the Synthesizer at 1.6 GHz

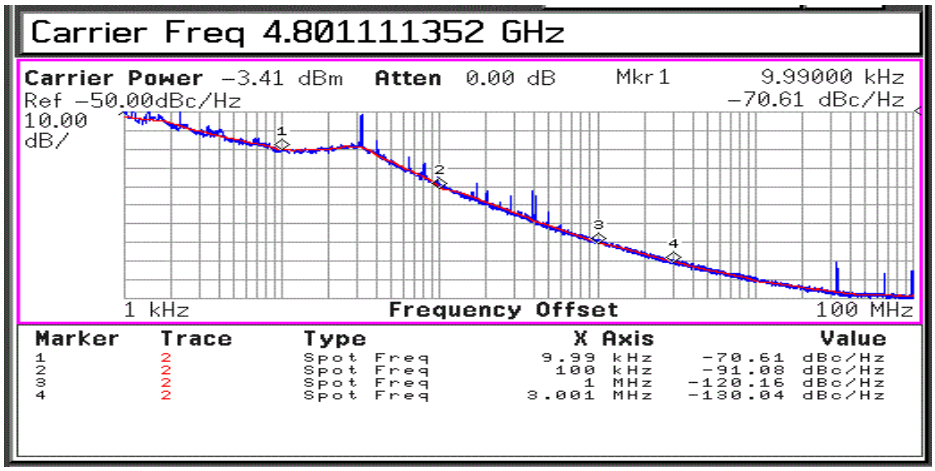



Figure 3- 34 Measured Phase Noise of the Synthesizer at 4.8 GHz

Table 3-3 shows the power consumption of each building block of the synthesizer. Of the 22mW total power consumption, around 10mW is consumed by the VCO.

Table 3- 2 BREAKDOWN OF THE SYNTHESIZER POWER CONSUMPTION

| **Building Block** | **Current (mA)** | **Supply Voltage (V)** | **Power Consumption (mW)** |
|---|---|---|---|
| VCO | 10 | 1 | 10 |
| Divide-by-2 | 2.6 | 1.8 | 4.68 |
| Loop freq. Divider | 3.2 | 1.8 | 5.76 |
| PFD and CP | 0.8 | 1.8 | 1.44 |
| Total | | | 21.88 |

Table 3-4 summarizes the performance of the fabricated synthesizer. The synthesizer achieves the required dual-band operation and with high spectrum purity.

Table 3- 3 PERFORMANCE SUMMARY OF THE SYNTHESIZER

| | |
|---|---|
| Synthesized Frequencies | 1.477-1.92GHz, 2.94-4.98GHz |
| Reference frequency | LB: 32/3 MHz<br>HB: 32 MHz |
| Spur @ $f_{ref}$ | < -72 dBc |
| Phase noise @ 1MHz offset | 1.6GHz: -130.83 dBc/Hz<br>4.8GHz: -120.16 dBc/Hz |
| Power | 21.88 mW |
| Supply Voltage | VCO: 1V<br>The rest of PLL: 1.8V |
| Die Area | 1.33 $mm^2$ |
| Technology | 0.18µm CMOS |

# 4. PLL IMPLEMENTATION – PHASE II

In this section the system analysis and design procedure of a 3rd Order MASH 1-1-1 SDM based on [23] for fractional PLL applications is discussed. The SDM block is implemented and added to the synthesizer from section 3. The concept and motivation for fractional divide ratios, the fundamentals of sigma delta modulation and the properties of oversampling and noise shaping that make it attractive for this application are briefly discussed. Some simulation results for the noise shaping of the SDM and of the PLL with the SDM selecting the channel frequencies are presented. The fractional PLL is implemented in 0.18μm CMOS technology. The measurement results and some conclusions are presented.

## 4.1 Introduction

In the integer PLL, the output frequency step size (channel spacing) is constrained the reference frequency (4-1).

$$f_{out} = N * f_{ref} \qquad (4-1)$$

For finer resolutions for the frequency synthesizer, a smaller reference frequency has to be used with larger divide ratios. Using a smaller reference frequency limits the loop bandwidth and hence would increase the settling time of the PLL. In a typical PLL, the PFD/CP noise is increased by 20log(N) when transferred to the PLL output. Therefore, large divide ratios corrupt the close-in phase noise performance of the PLL.

The fractional-N concept is used to produce frequency resolutions finer than the reference frequency. This removes the dependency of the output frequency steps on the reference frequency. The advantage is that for a given frequency resolution, larger reference frequencies and hence smaller divider ranges can be used. This would improve upon the overall phase noise performance of the PLL. Higher reference frequencies mean larger loop bandwidths can be selected and this reduces the settling time of the PLL. The fractional modulus is given by the average from switching repetitively between predetermined integer values. The use of SDM in generating the fractional divide modulus in PLLs is attractive because of the oversampling and noise shaping properties offered by this circuit.

**4.2 Oversampling and Noise Shaping Concepts of SDM**

When input signals are sampled at a rate higher than the Nyquist rate they are said to be oversampled. Oversampling reduces the in-band quantization noise by redistributing a fixed amount of noise power over a much larger bandwidth. Noise shaping on the other hand is a process whereby the in-band quantization noise of an SDM is pushed to higher frequencies by the action of the negative feedback loop [24].

The basic first order sigma delta modulator is a negative feedback loop with a loop filter, H(z), and a quantizer in the forward path, as shown in Fig. 4-1. In order to measure quantization noise and the effect of quantization on the input signal, a linearized model is required [25]. In the linear model, the quantizer is modeled as an additive noise source, E(z), (see Fig 4-2).

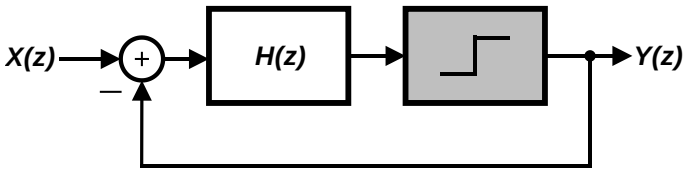



Figure 4- 1 First Order Sigma Delta Modulator

The transfer function for the linear model can be found as

$$Y(z) = \frac{H(z)}{1 + H(z)} \cdot X(z) + \frac{1}{1 + H(z)} \cdot E(z) \qquad 4 - 2$$

Where $\frac{\mathrm{H(z)}}{1+\mathrm{H(z)}}$ is known as the signal transfer function (STF) and $\frac{1}{1+\mathrm{H(z)}}$ is the noise transfer function (NTF).

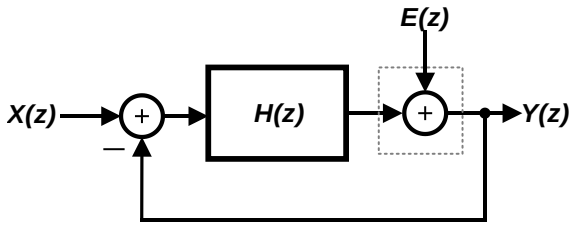



Figure 4- 2 Linear Model of First Order SDM

The loop filter H(z) is an integrator and has the transfer function expressed in (4-3) as

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \qquad 4 - 3$$

Inserting 4-3 into 4-2 results in 4-4. The signal, X(z), is delayed by one sample period ($z^{-1}$) and remains unchanged while the in-band quantization noise spectrum, E(z), is attenuated or "shaped" by the high-pass function ($1-z^{-1}$),[11, 23].

$$Y(z) = (z^{-1}) \cdot X(z) + (1 - z^{-1}) \cdot E(z) \qquad 4-4$$

### 4.3 System Analysis of MASH 1-1-1 SDM

The MASH 1-1-1 architecture consists of a cascade of first order SDMs whose outputs are processed by an error cancelation network (ECN). As shown in Fig. 4-3, the negative of the quantization error of the first stage, $E_1(z)$, and second stage, $E_2(z)$ are the inputs to the second and third stages respectively. The transfer functions for the three stages are given as follows:

$$Y_1(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E_1(z) \qquad 4-5$$

$$Y_2(z) = -z^{-1} \cdot E_1(z) + (1 - z^{-1}) \cdot E_2(z) \qquad 4-6$$

$$Y_3(z) = -z^{-1} \cdot E_2(z) + (1 - z^{-1}) \cdot E_3(z) \qquad 4-7$$

The output of the SDM, Y(z), is given in the expression below as

$$Y(z) = z^{-2} \cdot Y_1(z) + z^{-1}(1 - z^{-1}) \cdot Y_2(z) + (1 - z^{-1})^2 \cdot Y_3(z) \qquad 4-8$$

Inserting 4-5, 4-6, and 4-7 into 4-8 gives the overall transfer function of the SDM

$$Y(z) = z^{-3} \cdot X(z) + \cancel{z^{-2}(1 - z^{-1}) \cdot E_1(z)} - \cancel{z^{-2}(1 - z^{-1}) \cdot E_1(z)} + \cancel{z^{-1}(1 - z^{-1})^2 \cdot E_2(z)} - \cancel{z^{-1}(1 - z^{-1})^2 \cdot E_2(z)} + (1 - z^{-1})^3 \cdot E_3(z)$$

$$Y(z) = z^{-3} \cdot X(z) + (1 - z^{-1})^3 \cdot E_3(z) \qquad 4-9$$

Therefore the input signal is delayed by 3 sample periods and the noise of the third stage is shaped by the third order high pass function $(1 - z^{-1})^3$. It can be seen from the analysis that ideally the quantization noise from the first and second stages are totally cancelled out by the ECN.

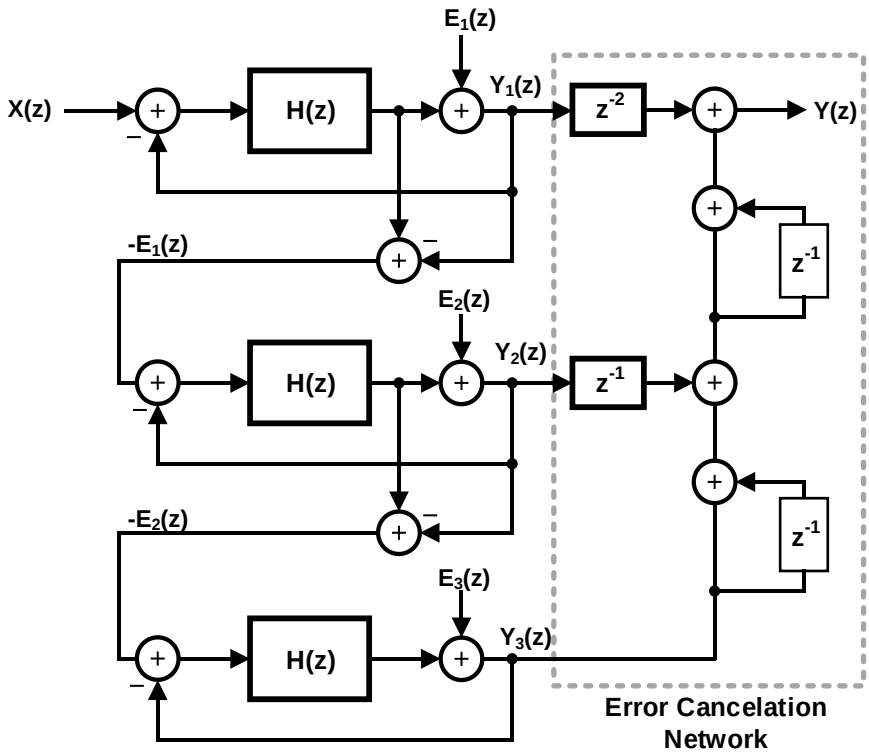



Figure 4- 3 Linear Model of MASH 1-1-1

For the EVA transceiver, there are 10 channels each spaced 6MHz from each other. The bandwidth that the synthesizer must scan is 54 MHz from 2.4GHz to 2.454GHz as shown in Fig 4-4. To cover the entire bandwidth of 54MHz, with a

reference frequency of 32MHz, the division ratios from 75 to 76.6875 in fractional steps of 0.1875 are required. Therefore, $N_{int} = 75\ or\ 76$.

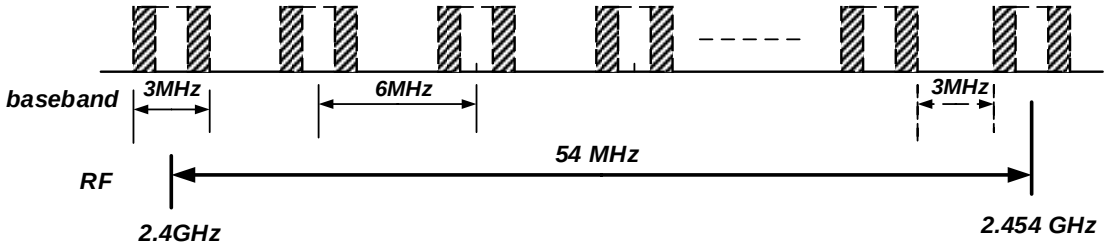



Figure 4- 4 Frequency Planning

In Table 4-1, the channel numbers (n) from 0 – 9 with their respective integer and fractionality factor are presented for the entire range

Table 4- 1: CHANNEL NUMBERING

| Output Frequency | Channel Number (n) | $N_{int}$ (Integer Division Ratio) | Fractionality Factor (X) |
|---|---|---|---|
| 2400+6n | 0 – 5 | 75 | 0.1875n |
| | 6 – 9 | 76 | 0.1875*(n-6) + 0.125 |

The overall divide ratio (ODR) is given by

$$ODR = N_{int} + X \qquad 4-10$$

$$where\ X = \left(\frac{K}{F}\right) \qquad 4-11$$

K is the M-bit input word to the SDM and $F = 2^M$. A 24 bit input word, K, is chosen for the SDM. The frequency resolution is given by $f_{REF}/2^M$. The resolution for the 24 bit input is approximately 2Hz. Since the input to the SDM is a DC value, the output of the SDM would be a periodic bitstream whose average is equal to the input DC value. The periodic sequence in the output is known as limit cycles [25]. In order to prevent limit cycles, the LSB of the input bitstream is preset to "1" to set an irrational number condition as analysed in [23]. The importance of choosing a high resolution for the input bitstream is so that when the LSB is preset to "1" to prevent limit cycles, the error introduced in the output frequency is minimal [23, 26]. Table 4-2 details the DC Inputs which are used in the selection of the various channels, their binary representation, the channel number (n), the ODR and the frequency expected at the output.

The output of the SDM is a signed 3-bit number. Two's complement binary number representation is used due to the ease of addition and subtraction [23]. The 3-bit number has 8 levels at the output from -3 to +4. Thus to realize the overall divide ratio of $N_{int} + X$, the divider's integer range should have the following moduli: $N_{int}$-3, $N_{int}$-2, $N_{int}$-1, $N_{int}$, $N_{int}$+1, $N_{int}$+2, $N_{int}$+3, $N_{int}$+4.

Table 4- 2 DC INPUTS FOR CHANNEL SELECTION

| **K (DC Input Word)** | **Binary Representation** | **n** | **$N_{int}$ + X** | **Channel Frequency (GHz)** |
|---|---|---|---|---|
| 1 | 0000 0000 0000 0000 0000 0001 | 0 | 75 | 2.400 |
| 3145729 | 0011 0000 0000 0000 0000 0001 | 1 | 75 + 0.1875 | 2.406 |
| 6291457 | 0110 0000 0000 0000 0000 0001 | 2 | 75 + 0.3750 | 2.412 |
| 9437185 | 1001 0000 0000 0000 0000 0001 | 3 | 75 + 0.5625 | 2.418 |
| 12582913 | 1100 0000 0000 0000 0000 0001 | 4 | 75 + 0.7500 | 2.424 |
| 15728641 | 1111 0000 0000 0000 0000 0001 | 5 | 75 + 0.9375 | 2.430 |
| 2097153 | 0010 0000 0000 0000 0000 0001 | 6 | 76 + 0.1250 | 2.436 |
| 5242881 | 0101 0000 0000 0000 0000 0001 | 7 | 76 + 0.3125 | 2.442 |
| 8388609 | 1000 0000 0000 0000 0000 0001 | 8 | 76 + 0.5000 | 2.448 |
| 11534337 | 1011 0000 0000 0000 0000 0001 | 9 | 76 + 0.6875 | 2.454 |

The pulse swallow divider designed has a complete range from 69 to 85. The range required for this application is from 72 to 80. In order to output the correct divide ratio, a 4-bit word, $N_{offset}$ is added to provide the correct control signals for the frequency divider. $N_{offset}$ is 3 for $N_{int} = 75$ and 4 for $N_{int} = 76$.

Table 4- 3 OUTPUT CODING TABLE FOR MASH 1-1-1

| Output Level | $b_3$ | $b_2$ | $b_1$ |
|---|---|---|---|
| -3 | 1 | 0 | 1 |
| -2 | 1 | 1 | 0 |
| -1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |

### 4.4 System Architecture and Circuit Implementation

The system architecture of the MASH 1-1-1 SDM is shown in Fig. 4-5. The system consists of a cascade of three first order digital accumulators. The implementation of the SDM is broken into two major sections: the design of the first order digital accumulator and the design of the error cancelation network.

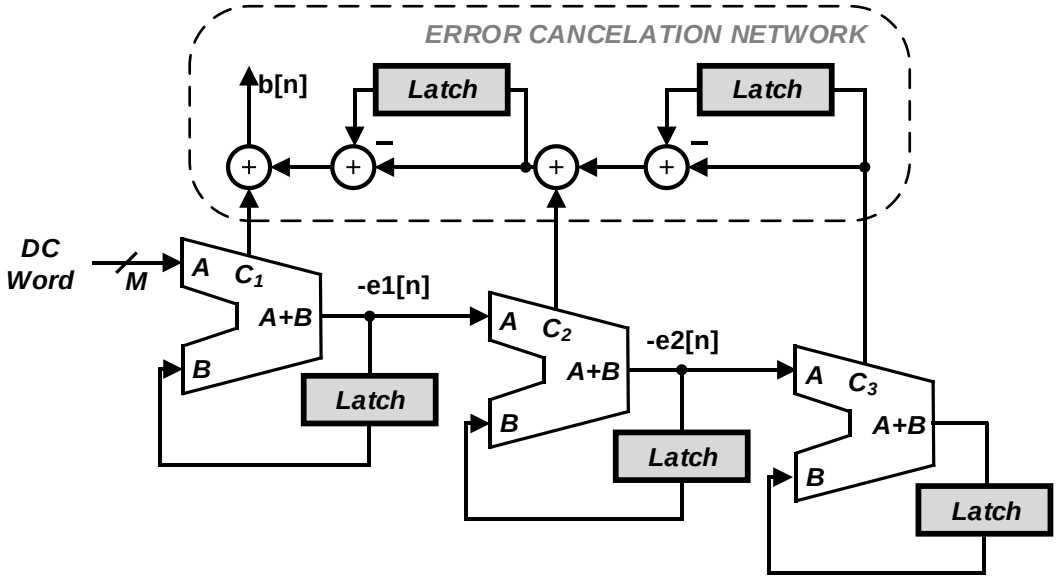



Figure 4- 5 MASH 1-1-1 Architecture for SDM

### 4.4.1 First Order Digital Accumulator Design

The first order accumulator is made up of a 24-bit Adder and a 24-bit Latch as shown in Fig. 4-6. In [24], it is proved that the accumulator is equivalent to a first order sigma delta modulator and hence has similar noise shaping properties.

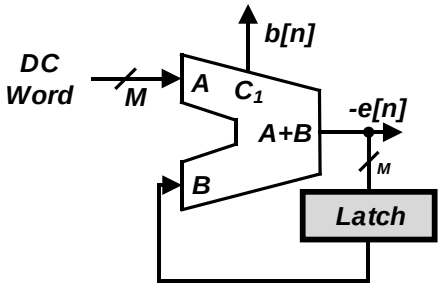



Figure 4- 6 Digital Accumulator

*4.4.1.1 24-bit Adder Design*

The 24 bit adder, Fig. 4-7(a), is composed of six 4-bit Carry Look Ahead (CLA) adders. The Carry Look Ahead architecture is faster than the conventional ripple adder. This is because the carry bit is not propagated through every single bit of the adder. The CLA makes use of propagate and generate signals to determine the carry out signal of each block [27]. In order to further speed up the adder, pipelining techniques are used where a single bit register is connected in the carry chain of the six 4-bit CLA stages[28]. The CLA adder consists of three subsystems:

- The Sum Generator
- The Carry Generator
- The Generate and Propagate Signal Generator

The sum generator block (Fig. 4-7(b)) is made up of a 4 bit ripple carry adder. The inverting mirror single bit adder [29] is used as a building block to eliminate the inverters from the critical delay path. As a result, there is minimum delay along the carry chain. The inverting mirror adder schematic is shown in Fig. 4-8

The generate (G) and propagate (P) signals are used to compute the carry-out signal independent of the ripple adder therefore making it independent of the delay of the ripple adder. The circuit consists of AND and XOR Gates (Fig. 4-7(b))

$$P = A \oplus B \qquad 4-12$$

$$G = A \cdot B \qquad 4-13$$

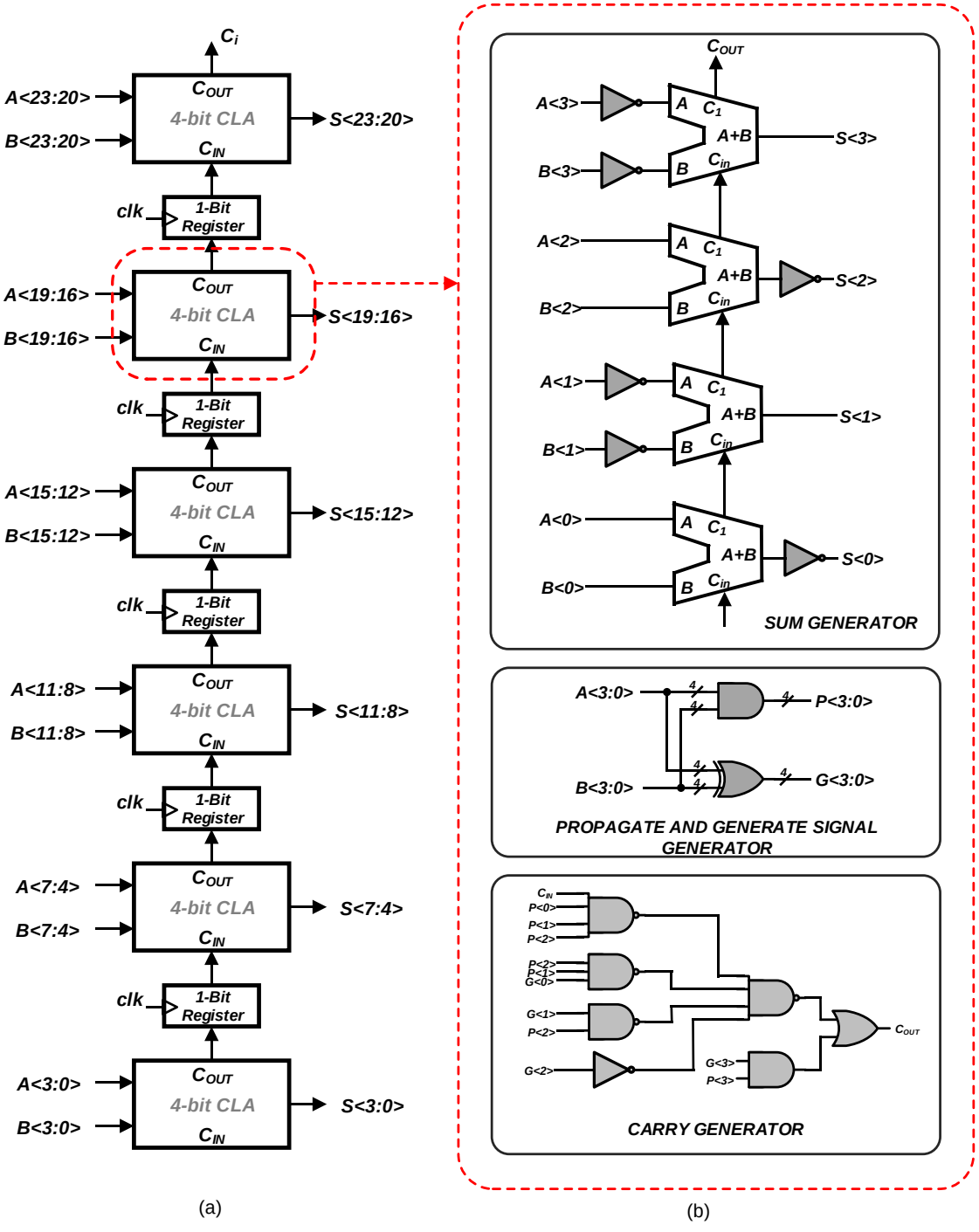



Figure 4- 7 (a) 24-bit Pipelined Adder (b) 4-bit CLA Adder Blocks: Sum Generator; Propagate and Generate Signal Generator and Carry Generator

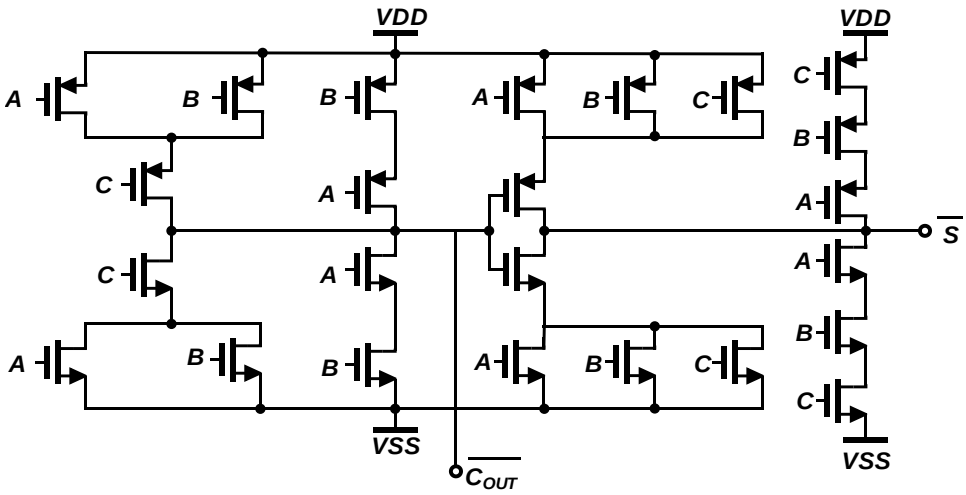



Figure 4- 8 Inverting Single Bit Mirror Adder

The Carry Generator block generates the carry signal from the P and G signals with the carry-in according to the following expression:

$$C_{OUT} = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_{IN} \qquad 4-14$$

*4.4.1.2 Single Bit Register Design*

A True Single Phase Clock (TSPC) D Flip Flop (see Fig. 4-9) is used for the single bit register because of the advantage of having a single clock phase, the power and area savings.

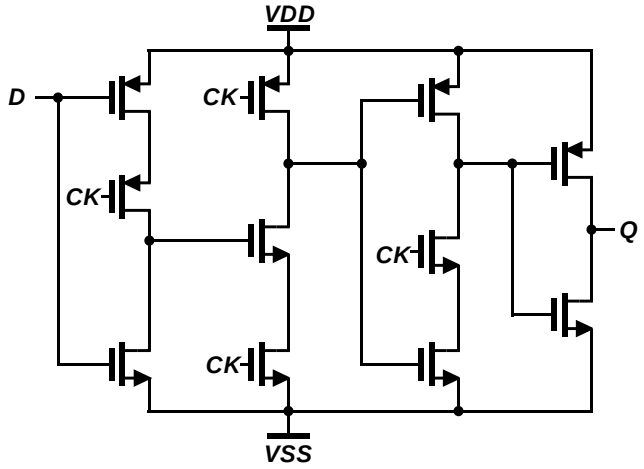



Figure 4- 9 TSPC D-FF Schematic

To verify the correct operation of the first order accumulator, a sinusoidal input of 54.6785 KHz was applied to the first order SDM. The results in Fig. 4-10 show a first order noise shaping.

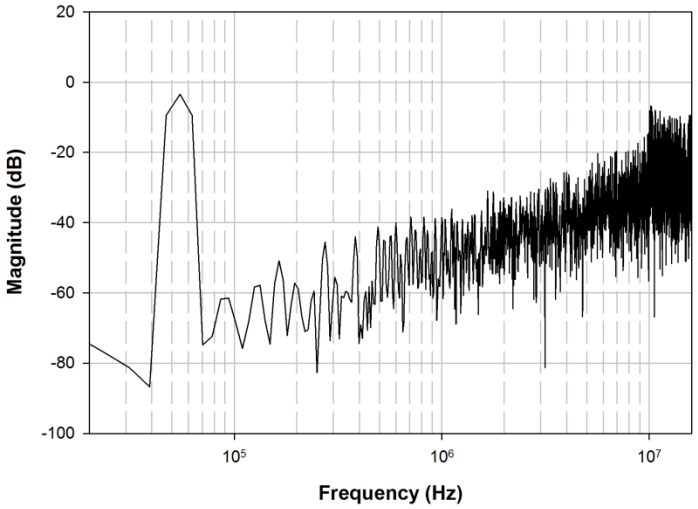



Figure 4- 10 First Order Noise Shaping

### 4.4.2 Error Cancelation Network Design

The carry outputs of the First Order Digital Accumulators are processed by the error cancelation network which implements the difference equation shown in 4-12:

$$b[n] = C_3[n] - 2C_3[n-1] + C_3[n-2] + C_2[n] - C_2[n-1] + C_1[n] \qquad 4-15$$

The Error Cancelation Network [30] is shown in Fig. 4-11

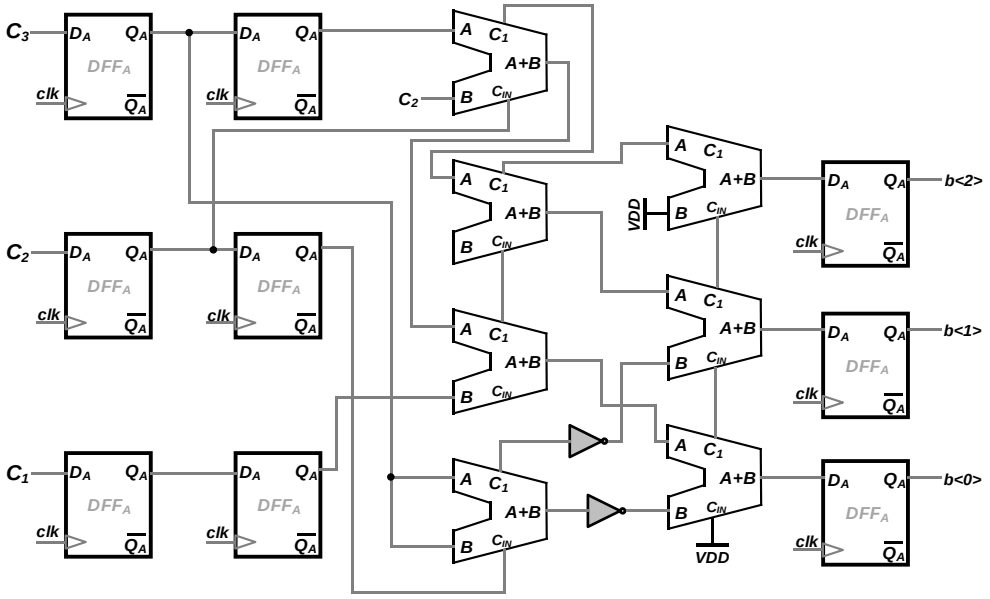



Figure 4- 11 Error Cancelation Network

Two tests are undertaken on the MASH 1-1-1 SDM. The first one verified the noise shaping properties of the SDM and the second one verified that the correct output frequency was chosen for a particular DC input word to the SDM.

In Fig. 4-12, the output of the SDM is plotted. It has eight output levels as expected for a MASH 1-1-1 topology. This waveform is generated for all the channels and is sampled. Fig. 4-13 shows the noise shaping plots for two of the channels. Most of the noise is concentrated at higher frequencies. Since the PLL bandwidth is 40.3 kHz, the high frequency noise is supressed by the PLL Loop Filter.

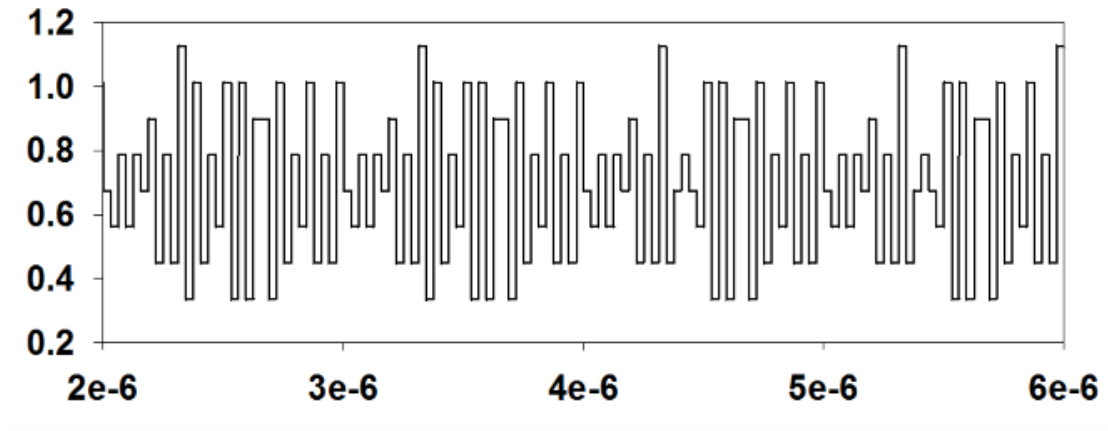



Figure 4- 12 SDM Output

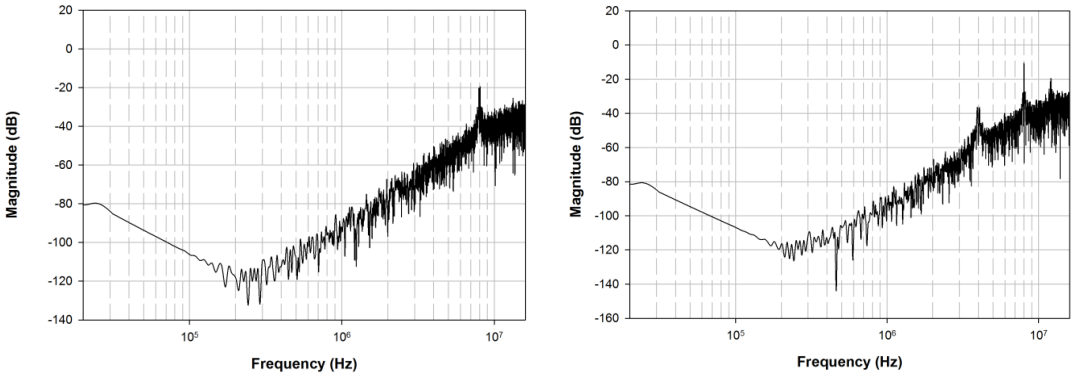



Figure 4- 13 Third Order Noise Shaping Plots for two channels

In order to speed up simulations, the PLL was modeled with verilogA blocks and the SDM left at the transistor level for the second set of simulations

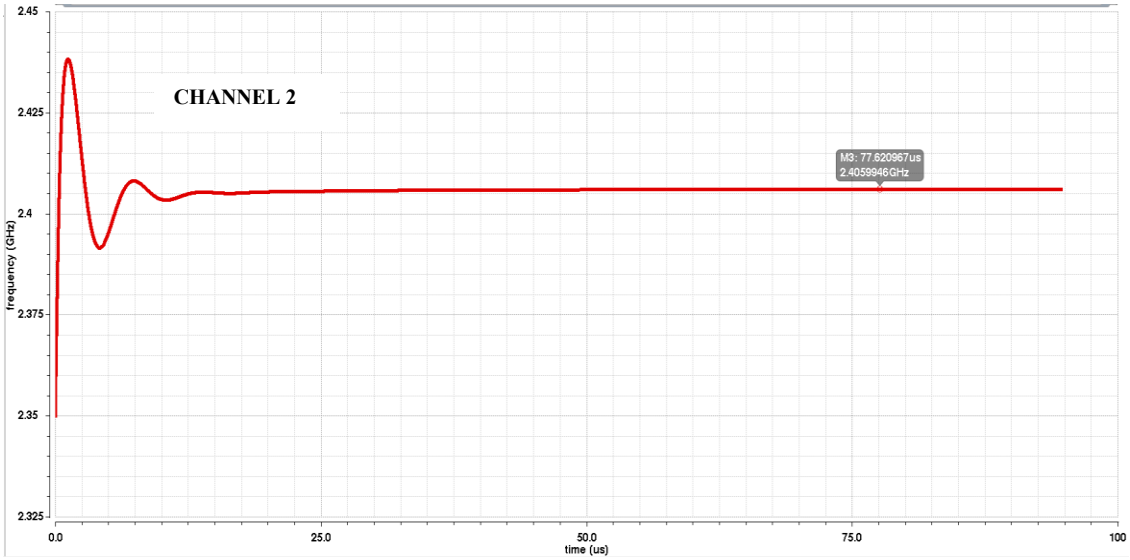



Figure 4- 14 VCO Output Frequency for PLL with Channel 2 Selected

Fig. 4-14 shows the result from the PLL when channel 2 is selected. The ideal value that the frequency is supposed to settle to is 2.406GHz. The PLL settles to approximately 2.406GHz for a settling time less than 50us. Fig. 4-15 shows that the PLL settles correctly to approximately 2.436GHz for settling time less than 50us.

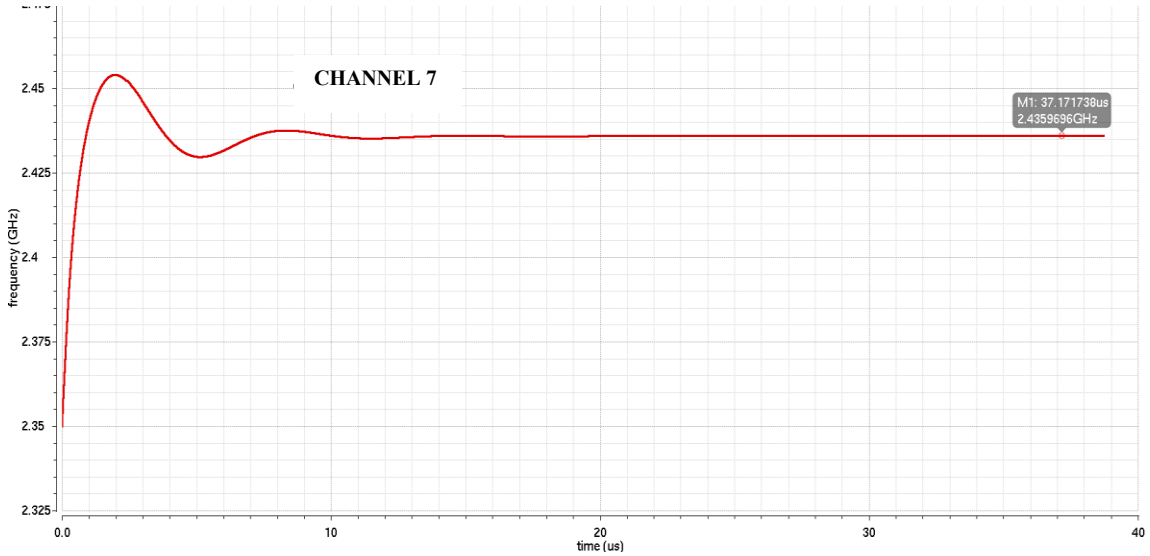



Figure 4- 15 VCO Output Frequency (~2.436GHz) for PLL with Channel 7 Selected

## 4.5 Fractional-N Synthesizer Measurement Results

The fractional synthesizer was fabricated in 0.18µm CMOS technology. The packaging used was a 48-pin QFN package. The chip active core area is 1.1mm x 1.4mm. The output spectrum and phase noise are measured for each of the 10 channels for the higher band (4.8 GHz) and the lower band (1.6 GHz).

### 4.5.1 Test Setup

For the frequency spectrum and phase noise measurements, an Agilent E4446a spectrum analyzer was used. A low phase noise signal generator was used to generate the 32 MHz reference clock. The die photo for the fractional synthesizer is shown in Fig 4-16. Fig. 4-17 shows the fabricated PCBs and the test setup for the chip measurements.

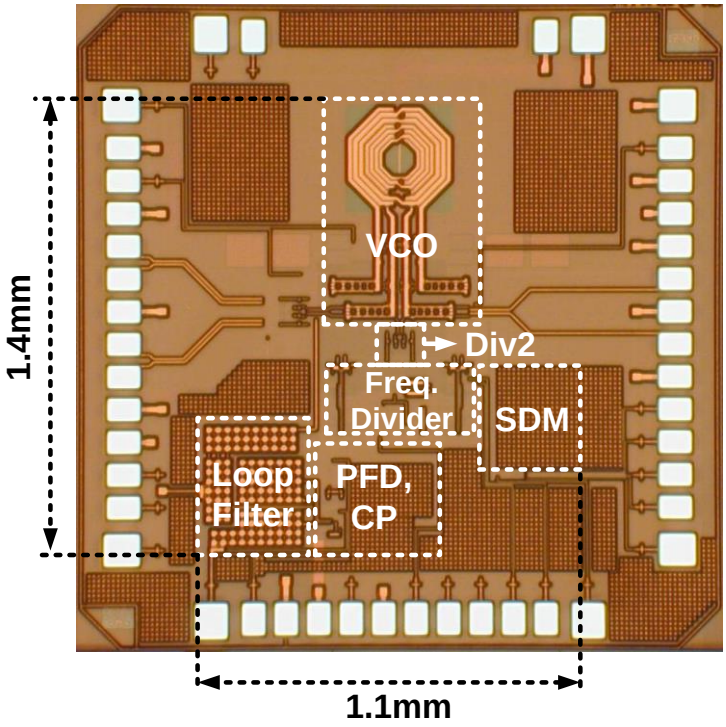


Figure 4- 16 Die Photo of Frequency Synthesizer

Figure 4- 17 Fabricated PCBs and Measurement Setup

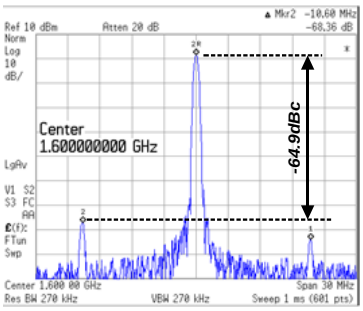
The DC input words for the sigma delta modulator, the divide ratios they implement and the expected synthesized frequencies for lower and higher bands are outlined in table 1. The measurements are performed for each of the DC inputs to verify the correct operation of the SDM in providing the fractional divide ratios.

### 4.5.2 Measurement Results

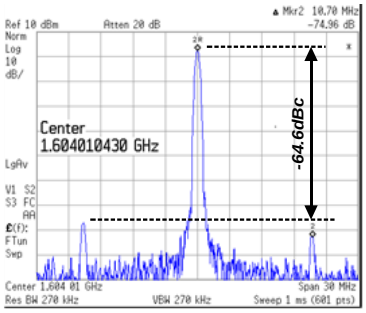
The measurement results for the synthesizer are shown in Fig. 4-18 for the lower band and Fig. 4.19 for the higher band. The synthesized frequency and phase noise results are summarized in Tables 2 and 3.

Table 4- 4 DC INPUTS FOR CHANNEL SELECTION

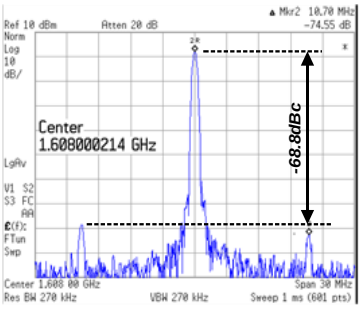
| **Channel** | **Binary Input to SDM** | **$N_{int}$ + X** | **LB (GHz)** | **HB (GHz)** |
|---|---|---|---|---|
| 1 | 0000 0000 0000 0000 0000 0001 | 75 | 1.600 | 4.800 |
| 2 | 0011 0000 0000 0000 0000 0001 | 75 + 0.1875 | 1.604 | 4.812 |
| 3 | 0110 0000 0000 0000 0000 0001 | 75 + 0.3750 | 1.608 | 4.824 |
| 4 | 1001 0000 0000 0000 0000 0001 | 75 + 0.5625 | 1.612 | 4.836 |
| 5 | 1100 0000 0000 0000 0000 0001 | 75 + 0.7500 | 1.616 | 4.848 |
| 6 | 1111 0000 0000 0000 0000 0001 | 75 + 0.9375 | 1.620 | 4.860 |
| 7 | 0010 0000 0000 0000 0000 0001 | 76 + 0.1250 | 1.624 | 4.872 |
| 8 | 0101 0000 0000 0000 0000 0001 | 76 + 0.3125 | 1.628 | 4.884 |
| 9 | 1000 0000 0000 0000 0000 0001 | 76 + 0.5000 | 1.632 | 4.896 |
| 10 | 1011 0000 0000 0000 0000 0001 | 76 + 0.6875 | 1.636 | 4.908 |



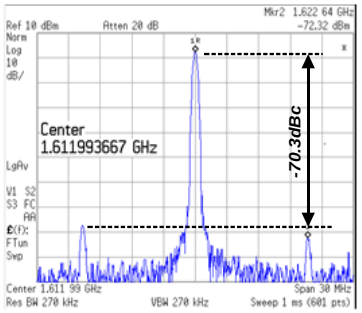

(a) Ch1 ~ 1.600GHz



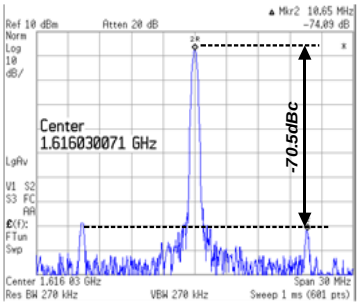

(b) Ch2 ~1.604GHz



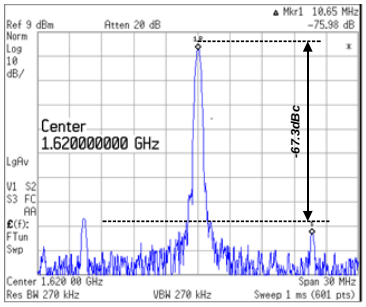

(c) Ch3 ~ 1.608GHz



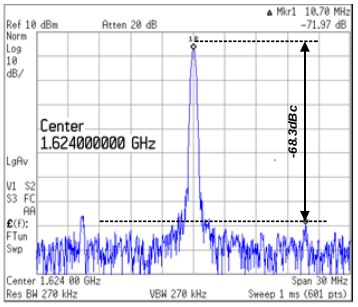

(d) Ch4 ~ 1.612GHz



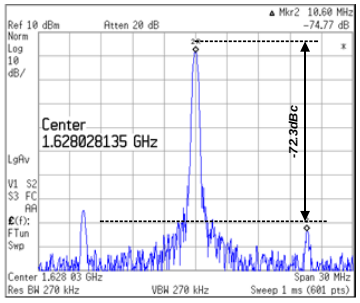

(e) Ch5 ~ 1.616GHz



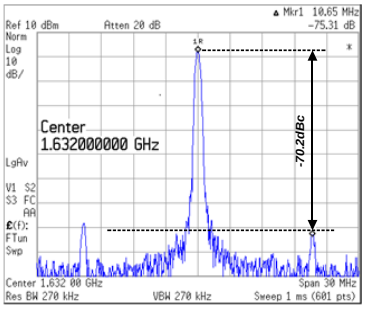

(f) Ch6 ~ 1.640GHz



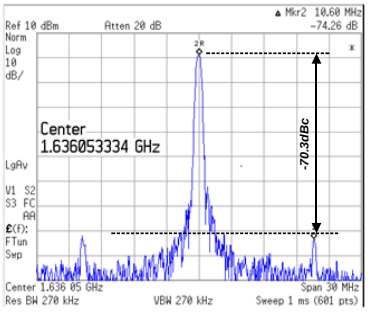

(g) Ch7 ~1.624GHz




(h) Ch8 ~ 1.628GHz

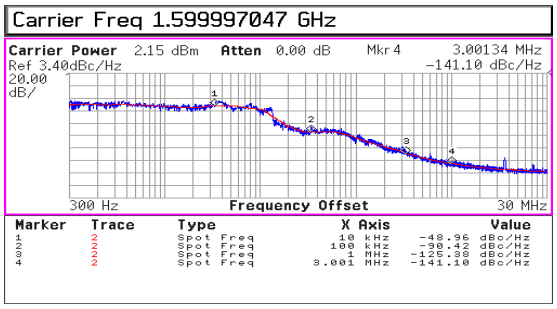



(i) Ch9 ~ 1.632GHz

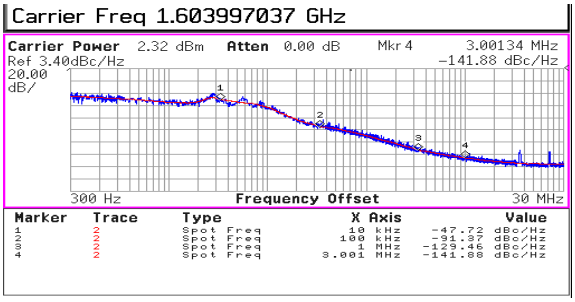



(j) Ch10 ~ 1.636GHz

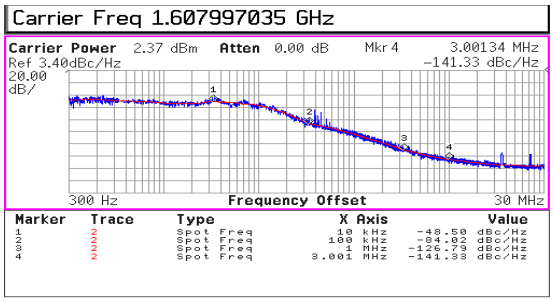
Figure 4- 18 Output Spectrum for Lower Band (a) Channel 1 (b) Channel 2 (c) Channel 3 (d) Channel 4 (e) Channel 5 (f) Channel 6 (g) Channel 7 (h) Channel 8 (i) Channel 9 (j) Channel 10



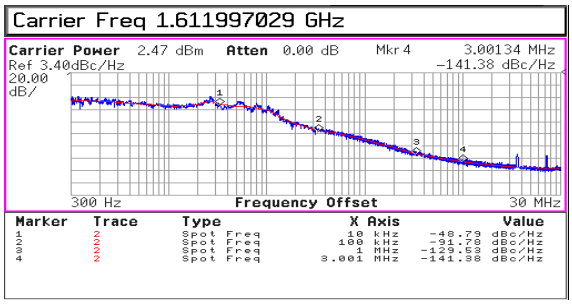

(b)



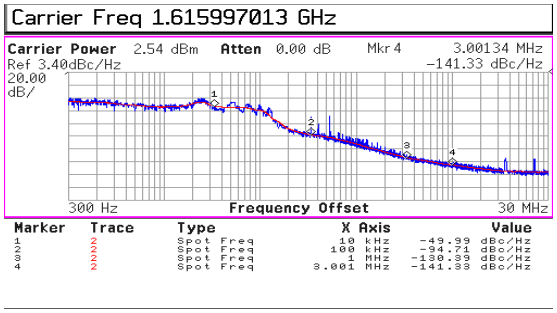

(a)



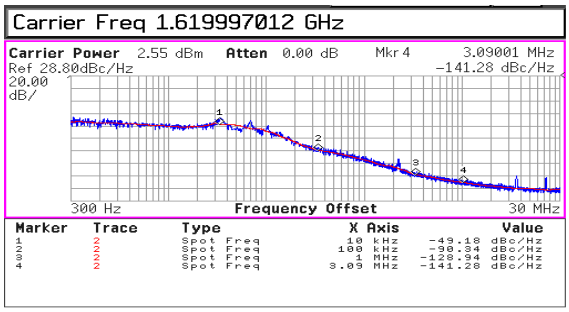

(d)



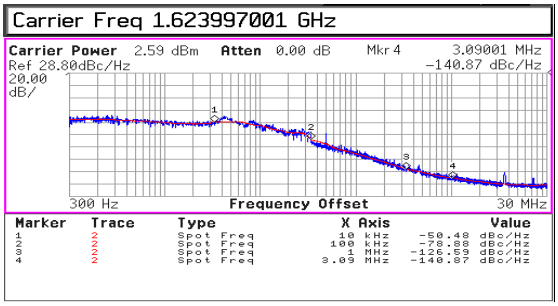

(c)



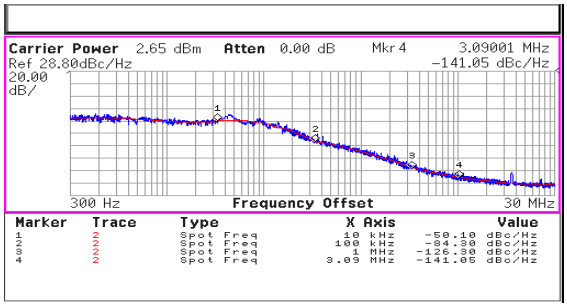

(f)




(e)

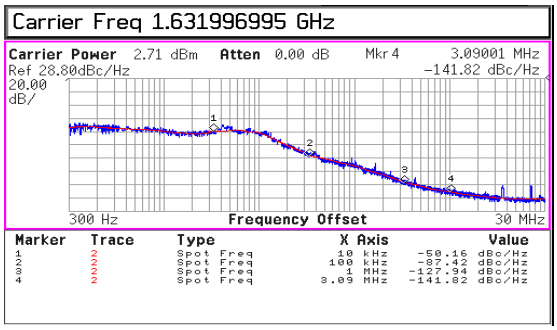



(h)

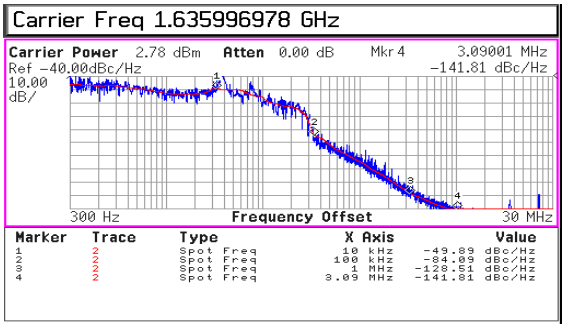



(g)

Figure 4- 19 Phase Noise for Lower Band (a) Channel 1 (b) Channel 2 (c) Channel 3 (d) Channel 4 (e) Channel 5 (f) Channel 6 (g) Channel 7 (h) Channel 8 (i) Channel 9 (j) Channel 10




(i)

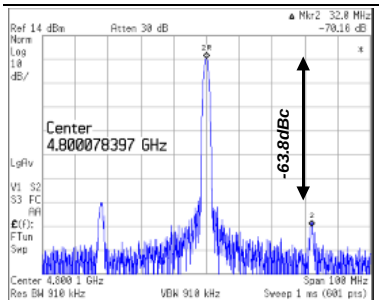



(j)

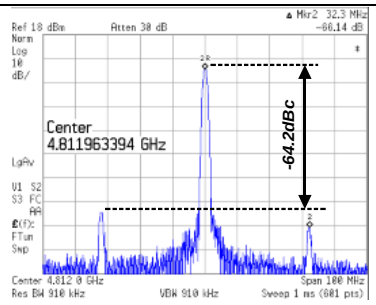
Figure 4-19 Continued

Table 4- 5 SUMMARY OF RESULTS FOR LOWER BAND

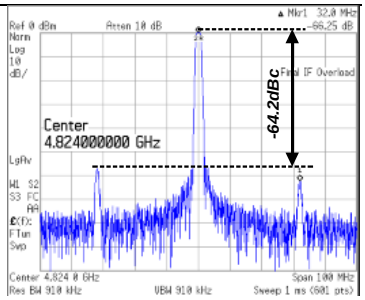
| **Channel** | **Center Frequency(GHz)** | **Phase Noise @ 1MHz (dBc/Hz)** |
|---|---|---|
| 1 | 1.600 | -125.38 |
| 2 | 1.604 | -129.46 |
| 3 | 1.608 | -126.79 |
| 4 | 1.612 | -129.53 |
| 5 | 1.616 | -130.39 |
| 6 | 1.620 | -128.94 |
| 7 | 1.624 | -126.59 |
| 8 | 1.628 | -126.30 |
| 9 | 1.632 | -127.94 |
| 10 | 1.636 | -128.51 |



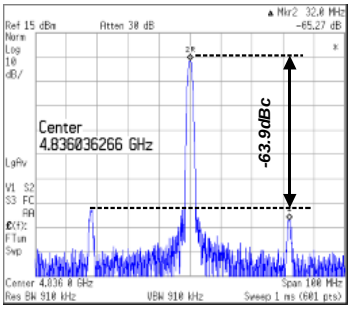

(a) Ch1 ~ 4.800GHz



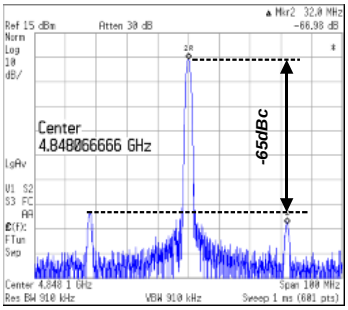

(c) Ch2 ~ 4.812GHz



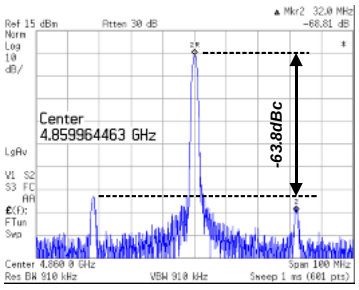

(b) Ch3 ~ 4.824GHz



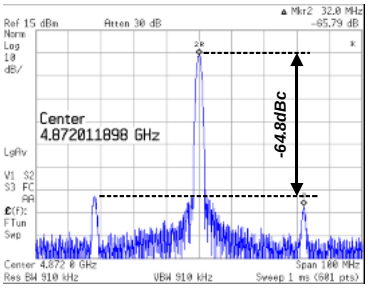

(e) Ch4 ~ 4.836GHz



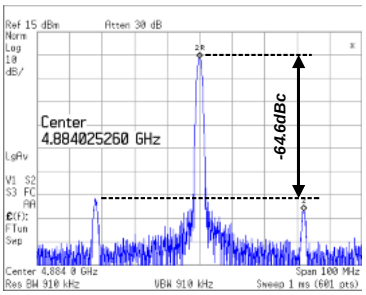

(d) Ch5 ~ 4.848GHz



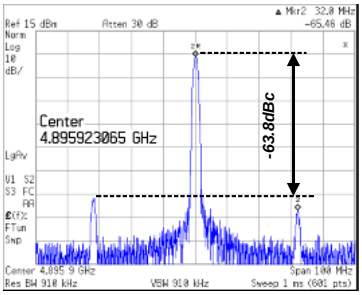

(j) Ch6 ~ 4.860GHz



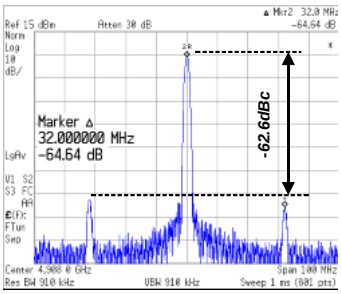

(i) Ch7 ~ 4.872GHz




(h) Ch8 ~ 4.884GHz




(g) Ch9 ~ 4.896GHz




(f) Ch10 ~ 4.908GHz

Figure 4- 20 Output Spectrum for Higher Band (a) Channel 1 (b) Channel 2 (c) Channel 3 (d) Channel 4 (e) Channel 5 (f) Channel 6 (g) Channel 7 (h) Channel 8 (i) Channel 9 (j) Channel 10

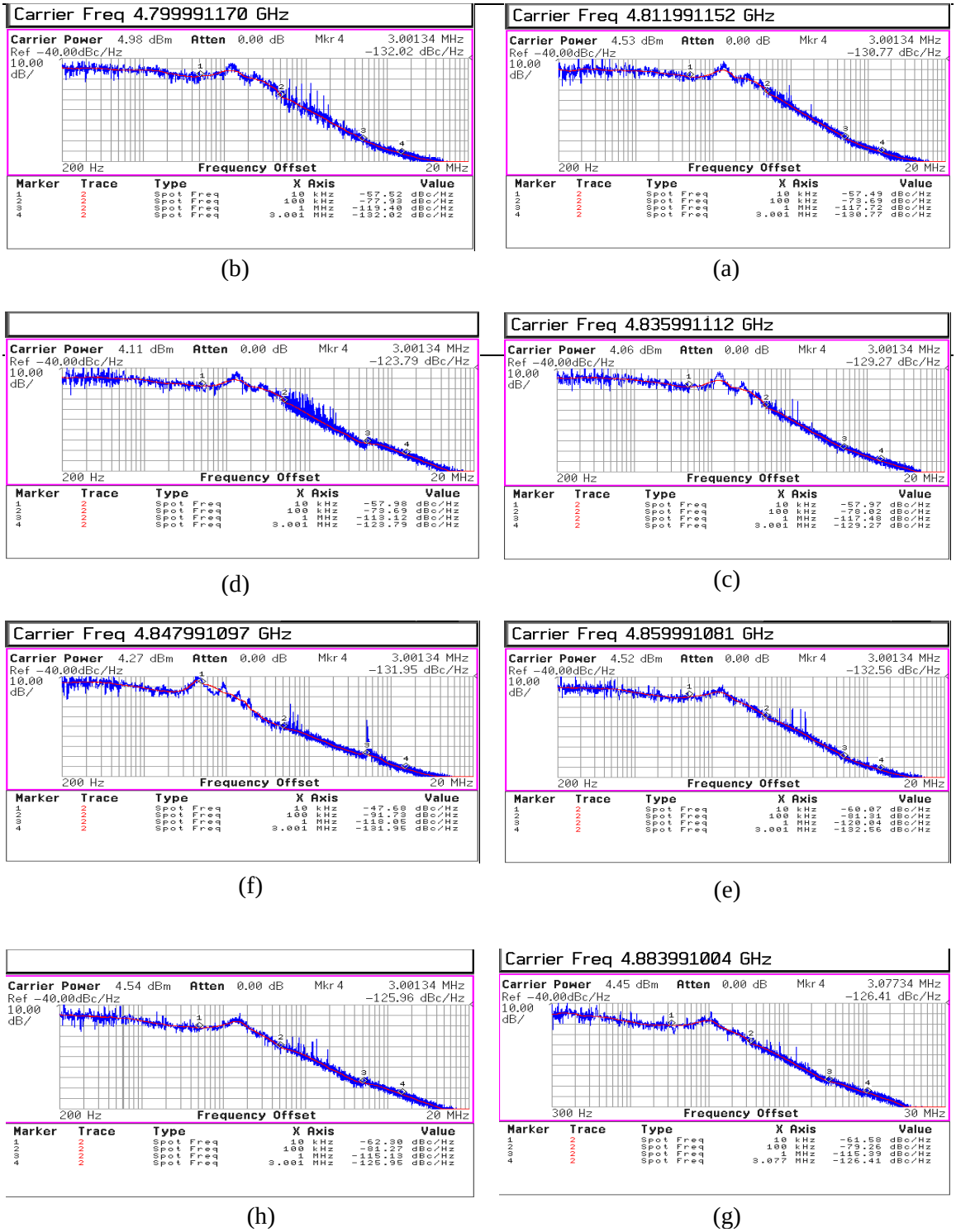
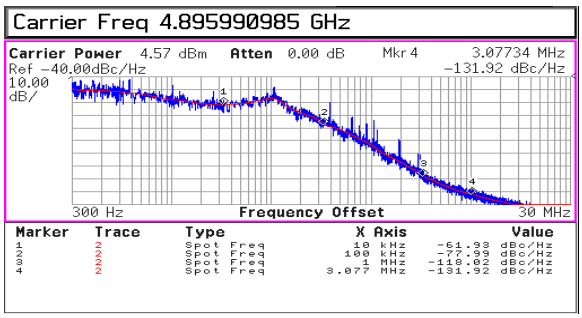
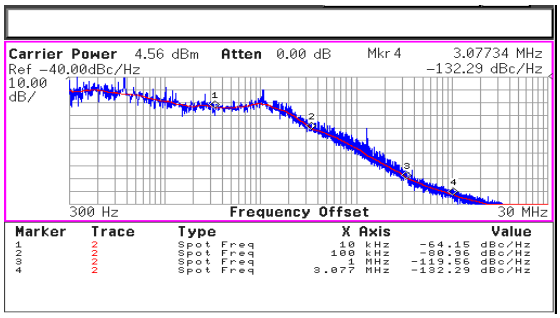



Figure 4- 21 Phase Noise for Higher Band (a) Channel 1 (b) Channel 2 (c) Channel 3 (d) Channel 4 (e) Channel 5 (f) Channel 6 (g) Channel 7 (h) Channel 8 (i) Channel 9 (j) Channel 10




(j)




(i)

Figure 4-21 Continued

Table 4- 6 SUMMARY OF RESULTS FOR HIGHER BAND

| **Channel** | **Center Frequency (GHz)** | **Phase Noise @ 1MHz (dBc/Hz)** |
|---|---|---|
| 1 | 4.800 | -119.40 |
| 2 | 4.812 | -117.72 |
| 3 | 4.824 | -113.12 |
| 4 | 4.836 | -117.48 |
| 5 | 4.848 | -118.05 |
| 6 | 4.860 | -120.04 |
| 7 | 4.872 | -115.13 |
| 8 | 4.884 | -115.39 |
| 9 | 4.896 | -118.02 |
| 10 | 4.908 | -119.56 |

From the results above, the synthesizer achieves phase noise performance of between -125.38dBc/Hz and -130.39dBc/Hz at 1MHz for the first and fifth channels respectively in the lower band. For the higher band, phase noise performance ranges

from -113.12 dBc/Hz for channel 3 to -120 dBc/Hz at 1 MHz for channel 6. The synthesizer achieves the spur performance at 10.6 MHz of less than -68.36 dBc for the lower band and -64.64 dBc for the higher band at 32 MHz.

Table 4-7 summarizes the performance of the fabricated synthesizer. The synthesizer achieves the required dual-band operation and with high spectrum purity.

Table 4- 7 PERFORMANCE SUMMARY OF THE SYNTHESIZER

| | |
|---|---|
| VCO Synthesized Frequencies | LB: 1.48-1.92GHz,<br>HB: 2.94-4.92GHz |
| Reference frequency ($f_{ref}$) | LB: 32/3 MHz<br>HB: 32 MHz |
| Spur @ $f_{ref}$ | LB: < -64.64 dBc<br>HB: < -68.36 dBc |
| Phase noise @ 1MHz offset | LB: -125.38 to -130.39 dBc/Hz<br>HB: -113.12 to -120.16 dBc/Hz |
| Power | 22.68mW |
| Supply Voltage | VCO: 1V<br>The rest of PLL: 1.8V |
| Die Area | 1.33 $mm^2$ |
| Technology | 0.18µm CMOS |

# 5. CONCLUSIONS AND FUTURE WORK

The focus of this research was a fully integrated dual band VCO PLL for EVA radios. The PLL was required to generate the LO signals for the EVA radio in both the transmit (1.6 GHz) and receive (4.8 GHz) modes of operation. The PLL chip was designed in two phases and both chips (the integer and fractional PLLs) are fabricated in 0.18µm CMOS technology.

Some basics of charge pump PLLs were discussed in section 2 and the dual path loop filter theory was introduced. This method made it possible for implementing narrow bandwidth PLLs with on-chip loop filter capacitors. The implementation details of the blocks of the integer PLL were discussed in section 3. The section concluded with measurement results from the fabricated chip. The integer PLL consumes a total of 21.88mW of power at a supply voltage of 1 V for the VCO and 1.8 V for the rest of the PLL blocks. At the lower band of 1.6 GHz, a phase noise of -130.83dBc/Hz at 1MHz offset from the carrier while -120.16dBc/Hz is the phase noise achieved at 1MHz offset for the 4.8 GHz band.

In section 4, the design and implementation of a MASH 1-1-1 sigma-delta modulator was considered. This block was added to the integer PLL of section 3 to generate the fractional divide ratios required. The fractional PLL was tested for all 10 channels for the RX and TX modes. The phase noise ranges from -125.38dBc/Hz and -130.39dBc/Hz at 1MHz offset and from -113.12 dBc/Hz for channel 3 to -120 dBc/Hz at

1 MHz for the 1.6GHz and 4.8GHz bands respectively. The total power consumption for the PLL with the SDM is 22.68mW.

The synthesizer is compared with some previous works in table 5-1

Table 5- 1 COMPARISON TABLE

| | [31] | [32] | This Work | |
|---|---|---|---|---|
| Type | Two VCOs | Two VCOs | Dual-Band VCO | |
| Technology | 45nm CMOS | 0.13μm CMOS | 0.18μm CMOS | |
| Supply Voltage (V) | 1.1 | 1.2 | 1.8<br>1 for VCO | |
| Power (mW) | 22-31.9 | 34-77 | 18.2-22.7 | |
| VCO Freq. (GHz) | 4.3-7.2/<br>7-10 | 3-4.8/<br>4-6 | 1.48-1.92/<br>2.94-4.98 | |
| Output Range (GHz) | 0.1-5 | 0.4-6 | 1.53-1.67/<br>4.6-5 | |
| Ref. Spur Level (dBc) | N/A | -66 | LB: < -70.2<br>HB:< -63.8 | |
| PN (dBc/Hz)<br>Offset freq.(MHz)<br>LO freq. (GHz) | -122<br>2<br>7.2 | -134.7<br>3<br>1.8 | -141.3<br>3<br>1.62 | -132.6<br>3<br>4.86 |
| Active Area ($mm^2$) | 0.41 | 2.3 | 1.54 | |

In the measurement of the PLL chip, the VCO tuning curve had to be manually selected. For future work, an automatic frequency calibration (AFC) circuit would be

designed to automatically select the VCO tuning curves (coarse tuning) while the PLL loop does the fine tuning.

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