NOVEL RF/MICROWAVE CIRCUITS AND SYSTEMS FOR LAB ON-CHIP/ON-BOARD CHEMICAL SENSORS

A Dissertation

by

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ABSTRACT

Recent research focuses on expanding the use of RF/Microwave circuits and systems to include multi-disciplinary applications. One example is the detection of the dielectric properties of chemicals and bio-chemicals at microwave frequencies, which is useful for pharmaceutical applications, food and drug safety, medical diagnosis and material characterization. Dielectric spectroscopy is also quite relevant to detect the frequency dispersive characteristics of materials over a wide frequency range for more accurate detection. In this dissertation, on-chip and on-board solutions for microwave chemical sensing are proposed.

An example of an on-chip dielectric detection technique for chemical sensing is presented. An on-chip sensing capacitor, whose capacitance changes when exposed to material under test (MUT), is a part of an LC voltage-controlled oscillator (VCO). The VCO is embedded inside a frequency synthesizer to convert the change in the free runing frequency frequency of the VCO into a change of its input voltage. The system is implemented using 90 nm CMOS technology and the permittivities of MUTs are evaluated using a unique detection procedure in the 7-9 GHz frequency range with an accuracy of 3.7% in an area of 2.5 × 2.5 mm^2 with a power consumption of 16.5 mW. The system is also used for binary mixture detection with a fractional volume accuracy of 1-2%.

An on-board miniaturized dielectric spectroscopy system for permittivity detection is also presented. The sensor is based on the detection of the phase difference between the input and output signals of cascaded broadband True-Time-Delay (TTD) cells. The sensing capacitor exposed to MUTs is a part of the TTD cell. The change of the permittivity results in a change of the phase of the microwave signal passing through the TTD cell. The system is fabricated on Rogers Duroid substrates with a total area of 8 × 7.2 cm^2. The permittivities of MUTs are detected in the 1-8 GHz frequency range with a detection accuracy of 2%. Also, the sensor is used to extract the fractional volumes of mixtures with accuracy down to 1%.

Additionally, multi-band and multi-standard communication systems motivate the trend to develop broadband front-ends covering all the standards for low cost and reduced chip area. Broadband amplifiers are key building blocks in wideband front-ends. A broadband resistive feedback low-noise amplifier (LNA) is presented using a composite cross-coupled CMOS pair for a higher gain and reduced noise figure. The LNA is implemented using 90 nm CMOS technology consuming 18 mW in an area of 0.06 mm^2. The LNA shows a gain of 21 dB in the 2-2300 MHz frequency range, a minimum noise figure of 1.4 dB with an IIP3 of -1.5 dBm. Also, a four-stage distributed amplifier is presented providing bandwidth extension with 1-dB flat gain response up to 16 GHz. The flat extended bandwidth is provided using coupled inductors in the gate line with series peaking inductors in the cascode gain stages. The amplifier is fabricated using 180 nm CMOS technology in an area of 1.19 mm^2 achieving a power gain of 10 dB, return losses better than 16 dB, noise figure of 3.6-4.9 dB and IIP3 of 0 dBm with 21 mW power consumption.

All the implemented circuits and systems in this dissertation are validated, demonstrated and published in several IEEE Journals and Conferences.

To My Father, Mother, Brother and Sister

ACKNOWLEDGEMENTS

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1. INTRODUCTION

Recent multi-disciplinary research focuses on expanding the use of electronic circuits and systems to include applications that employ electrical circuits in non-electrical applications. These applications include chemical/biochemical sensors, biomedical devices and microelectromechanical systems (MEMS). The global trend in this research area is moving towards portable, implantable and lab-on-chip systems that require: (1) complete integration of the system on silicon platforms, such as CMOS and SiGe processes, (2) miniaturization of on-baord implementations, and (3) self-sustained implementation to achieve a stand-alone operation without the need of any external equipment. In other words, self-sustained miniaturized/integrated systems are necessary for portable and implantable sensors.

Nowadays, chemical/biochemical sensing is one of the attractive multi-disciplinary applications in the academic and industrial fields. Chemical sensing and characterization can be performed using electrical, physical and mechanical properties of materials under characterization, such as the dielectric constant (permittivity) [1], the thermal conductivity [2, 3], the mass density and viscosity [4, 5]. The reported chemical sensors based on the detection of thermal conductivity, mass density and viscosity as material's properties are using micromachined structures, such as bridges, cantilevers, clamped beams and suspended MEMS resonators [2, 3, 4, 5]. These structures impose difficulties and challenges in fabrication, specially for on-chip integration and on-board miniaturization. Accordingly, the permittivity is one material's

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property that is promising for simpler implementation of the sensing unit compared to other properties and is the focus of this dissertation.

1.1 Definition of the Permittivity

The relative permittivity of a material, ϵ_r, is a dimensionless complex number, or $\epsilon_r = \epsilon_r' - j\epsilon_r''$, where ϵ_r' is the real part of the permittivity and reflects the extent to which the material concentrates electrostatic lines of flux. The imaginary part of the permittivity, ϵ_r'', represents the attenuation of electromagnetic (EM) waves passing through the material.

Moreover, the permittivity is a frequency dependent quantity. The dependency of the complex permittivity, $\epsilon_r(\omega)$, on frequency, for a large class of compounds, is represented by frequency dispersive equations. Many representations exist for frequency dispersive complex permittivities, and one of the most common equations is the *Cole-Cole* representation [6, 7, 8] and is given by

$$\epsilon_r(\omega) = \epsilon_r'(\omega) - j\epsilon_r''(\omega) = \epsilon_{r,\infty} + \frac{\epsilon_{r,0} - \epsilon_{r,\infty}}{1 + (j\omega\tau)^{1-\alpha}} \tag{1.1}$$

where $\epsilon_{r,0}$ is the static permittivity at zero frequency, $\epsilon_{r,\infty}$ is the permittivity at $\omega = \infty$, τ is the characteristic relaxation time and α is the distribution (relaxation time) parameter. All of these constants are fixed for a particular material and vary from one material to another. As an example, Fig. 1.1 shows the frequency dependency of the complex permittivity of Ethanol using its reported Cole-Cole parameters: $\epsilon_{r,0} = 4.5$, $\epsilon_{r,\infty} = 25.07$, $\tau = 143$ ps and $\alpha = 1$.

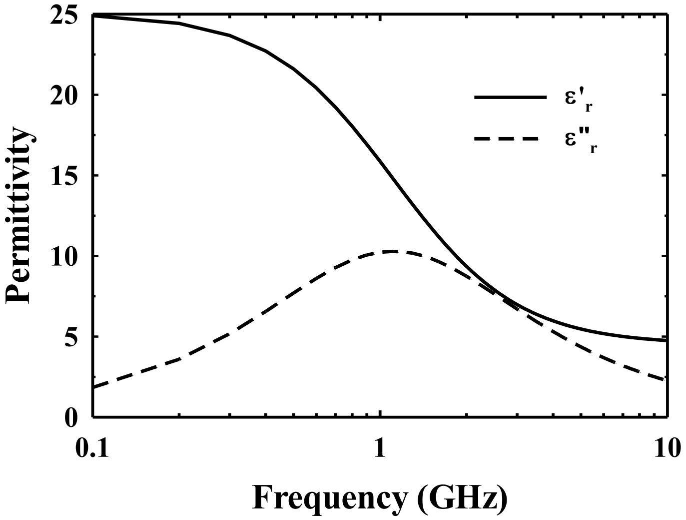

Figure 1.1: Complex permittivty of ethanol versus frequency following the Cole-Cole model.

1.2 Importance of Dielectric Sensing

In general, sensing the dielectric properties of chemicals and biochemicals is quite relevant to a variety of applications. Soil characterization and leaf sensing are examples of dielectric characterization used to improve the quality of agricultural crops [9, 10]. Also, dielectric characterization is employed in gas and smoke detection, alarm sensing and oil exploration and processing. In health care fields, dielectric characterization can be used in drug and food safety, medical diagnosis and instrumentation [11, 12, 13, 14, 15].

1.2.1 Dielectric Sensing at Microwave Frequencies

The ability to sense dielectric properties of chemicals/biochemicals at RF and microwave frequencies is also useful because of the following;

- The use of microwave signals is increasing in wireless communications. Therefore, it is necessary to study the interaction between microwave signals and chemicals/biochemicals used in medical and pharmaceutical applications [11]. This interaction can be found by calculating the amount of energy absorbed by these materials, which is a function of their permittivities at microwave frequencies. An example of these interactions is the study of possible health hazards and non-thermal effects caused by microwave signals on biochemicals inside living organisms, such as the human blood [12]. Another example is studying the effect of microwave radiation on food and drug safety,

- Microwave dielectric detection for chemicals/biochemicals is also useful for medical diagnosis. Some studies have shown that the dielectric properties of biological samples such as blood [12, 13], semen [14], and cerebra spinal fluid [15] show appreciable change in patients with specific diseases compared to healthy people at microwave frequencies. One example is the detection of glucose concentration in blood by means of dielectric measurements, which has potential application in blood sugar control for diabetics [16, 17],

- Knowledge of the dielectric properties of chemicals/biochemicals at microwave frequencies helps in the development of microwave medical techniques that depend on the high frequency electromagnetic properties of these chemicals and biochemicals. Examples of these medical microwave techniques are the microwave thermography and tomography [18],

- Characterization of chemicals and mixtures is useful for measurement of dielectric properties of chemicals, polymers and gels at microwave frequencies to provide important information regarding their chemical composition and structure [11].

1.2.2 Microwave Dielectric Spectroscopy

Dielectric spectroscopy means the detection of the dielectric constant of the material under test (MUT) at a wider frequency range. The need for broadband microwave dielectric spectroscopy is quite relevant because;

- The above mentioned applications for microwave dielectric measurement can be applied for a wider range of frequencies. This can help in studying interactions of materials with signals in a wider frequency range for more accurate characterization,

- Many materials may share the same value of the permittivity at a single frequency. Therefore, detecting the unique frequency dispersive characteristics [6] of the material under test over a wide frequency range is useful for more accurate material detection,

- Low-frequency techniques for zero-frequency permittivity detection of ionic liquids fail due to high electrical conductance of these liquids at low frequencies [19]. However, the dielectric properties of these liquids can be easily extracted at microwave frequencies, and then they can be extrapolated to obtain the static dielectric constant [19].

1.3 Existing Dielectric Sensing Architectures

In this subsection, several reported architectures for dielectric sensors, either implemented on-board or integrated on silicon, are discussed.

1.3.1 On-Board Dielectric Sensors

On-board sensor implementations are promising for self-sustained miniaturized implementations with dielectric spectroscopy capability, specially at microwave frequencies. Generally, dielectric detection techniques are classified as frequency domain and time domain techniques. Many frequency domain techniques for dielectric detection are based on microwave resonators [16, 20], where the permittivity detection is due to the change of the resonance frequency and the quality factor of the resonator when the MUT is applied. This technique is narrowband and cannot be applied for broadband microwave dielectric spectroscopy. Reported broadband spectroscopy sensors are based on measuring the magnitude and phase of the scattering matrix parameters of a transmission line or a coaxial probe exposed to the MUT [21, 22, 23] which are then used to estimate the permittivity of the MUT over a wide frequency range. Planar miniaturized techniques based on substrate integrated waveguide resonators and planar microstrip resonators are also employed for low-cost, wideband miniaturized permittivity detection with moderate accuracy compared to resonator-based sensors [1, 24, 25]. Reported frequency domain techniques [21, 22, 23, 1, 24, 25] employ vector network analyzers (VNA) to measure the scattering parameters of the sensor for permittivity detection. This technique enables high detection accuracy by taking advantage of highly precise commercial and bulky VNAs.

Time domain dielectric spectroscopy (TDDS) technique is based on measuring the reflection of a fast rising step voltage applied to a transmission line terminated by the sample subject to characterization [26, 27, 28]. Compared to frequency domain spectroscopy techniques, time domain spectroscopy has the advantage of capturing the frequency domain characteristics of sample under test at once using a single step voltage generator followed by applying mathematical time to frequency signal conversion, such as Fourier transform, thus eliminating the need of a wideband frequency synthesizer. However, reported time domain spectroscopy techniques are associated with bulky step voltage generators and digital oscilloscopes [27] or bulky Time-Domain Reflectometers (TDR) [28].

To the best of author's knowledge, all reported on-board frequency and time domain spectroscopy techniques are not suitable for self-sustained operation due to the need for bulky and expensive measurement equipment, such as VNAs, scopes and TDRs. Accordingly, reported techniques are not suitable for portable and implantable sensors.

1.3.2 Integrated Dielectric Sensors

Integrated sensors on Silicon are promising and challenging to achieve size and cost reduction, lower power consumption, enormous signal processing capabilities and high throughput for lab-on-chip applications. The reported dielectric sensors on silicon are based on direct measurement of the complex impedance of the sample. Generally, the capacitance measurement is the basic technique in many sensing and detection applications, such as: chemical/biochemical sensing [29, 30, 31, 32, 33, 34, 35, 36, 37], contact impedance sensing [38], and finger-print detection [39]. In case of chemical/biochemical sensing, the complex impedance changes due to molecular interaction with bio-materials and/or electromagnetic interaction with chemicals. In [29], a fully electronic CMOS DNA detection based on capacitance measurement is presented. An interdigitated capacitor is implemented on CMOS process and the change of the sensing impedance is translated into change in the frequency of the waveform generated by means of alternatively charging and discharging the sensing capacitor with reference currents. In [30], a CMOS capacitance sensor for humidity detection is presented. The change of the impedance is translated into a corresponding change of frequency within the range of 135-160 KHz, using a charging circuit acting as a capacitance-to-frequency converter. In [31, 32], CMOS capacitance sensing for permittivity detection of chemicals, such as acetone and methanol, is incorporated with microfluidic structures to expose the sensor to liquids under test. The capacitance change is translated into a voltage using the charge-based capacitance measurement (CBCM) technique. In [38], another technique based on capacitance sensing is proposed for contact impedance sensors by embedding the sensing capacitor as a part of an off-chip LC tank whose resonance frequency is changed within the range of 40-120 MHz upon the change of the sensing capacitance. In [33, 34], a fully integrated CMOS electrochemical impedance spectroscopy within the range of 10 Hz-50 MHz is presented to characterize biomaterials such as DNAs and proteins. In this technique, an on-chip electrode along with an external reference electrode are used to sense the impedance variation of a mixture including the electrolyte with biomaterial under test. I-Q mixers are used to detect the real and imaginary parts of the electrochemical impedance. In [35], a broadband capacitive spectroscopy is proposed and simulated for detection in the frequency range of 1 MHz-1 GHz using a down-conversion mixing architecture proving a capacitance sensitivity of 0.7 fF without fabrication and experimental validation. In [36, 37], a broadband capacitance to current converter is proposed and fabricated without material characterization. The sensor shows a conversion ratio of 164 pA/aF in the frequency range of 1 Hz-1 GHz. Other than capacitance sensing techniques, inductance sensing technique is employed for DNA detection in [40]. The sensing inductor with magnetic beads is embedded in the LC tank of a 1 GHz VCO and the frequency shift upon exposure to DNA is detected.

CMOS capacitance sensing techniques that require DC reference currents [29, 30, 31, 32] can not be used for non-static dielectric characterization, especially at microwave frequencies. Also, sensing techniques employing external sources [33, 34, 35, 36, 37] in the frequency range of 1 Hz-1 GHz are not suitable for self-sustained operation. Therefore, the capacitance sensing techniques pose immediate challenges on extending the sensing frequency to the microwave range with a self-sustained operation.

1.4 Summary of Challenges for Microwave Dielectric Sensor Implementation

The main objective in dielectric sensors is to integrate a sensing element with on-chip/on-board RF circuits and systems. The sensing element exhibits changes when exposed to MUTs and the interface circuitry converts the change of the sensing element into a baseband signal that can be easily extracted and read-out. The challenges of on-chip/on-board microwave dielectric sensing implementation is summarized as follows

1. Implementation of an on-chip dielectric sensor at frequencies above 1 GHz. To the best of author's knowledge, there is no work reported in the literature for such frequencies.
2. Implementation of wideband dielectric spectroscopy systems.
3. Self-sustained operation of the dielectric sensors suitable for portable and implantable systems.
4. Miniaturization of on-board self-sustained dielectric sensors at microwave frequencies.
5. Exposure of the on-chip/on-board sensing elements to MUTs for permittivity detection and characterization.
6. Developing sensing algorithms including sensor calibration for accurate permittivity detection and match the measured values to reported theoretical permittivities [6].

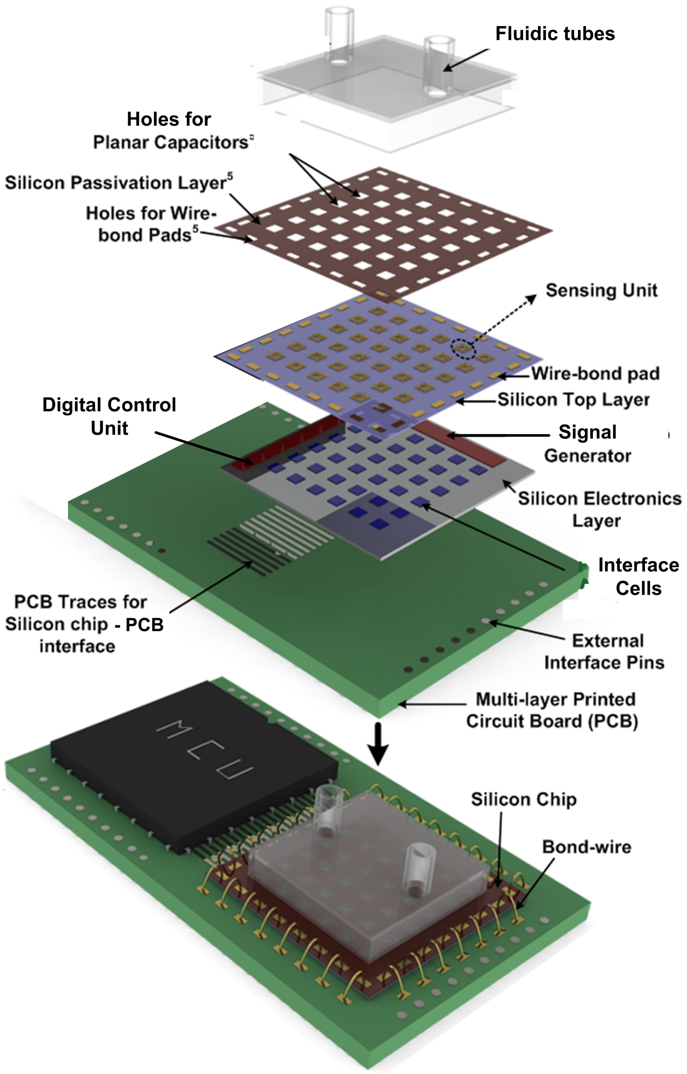

Figure 1.2: Illustrative example of a fully integrated platform for dielectric sensing.

Fig. 1.2 shows an illustrative example of a self-sustained fully integrated sensing platform addressing most of the above mentioned challenges. This platform contains: (1) A Printed Circuit Board (PCB) for hybrid integration of the sensor chip, (2) a CMOS layer including the signal generator and the interface and read-out circuits for control and detection, (3) sensing elements on top of the CMOS process, (4) holes on top of the sensing elements to make it exposable to MUT, and (5) fluidic tubes acting as a container for the liquids under characterization.

1.5 Goals and Objectives of the Dissertation

The primary objective of this dissertation is to propose, implement and validate on-chip/on-board prototypes for chemical sensing at microwave frequencies. This objective is summarized as follows:

- Implementing a prototype for an on-chip self-sustained chemical sensing at microwave frequencies: An on-chip capacitor working as a sensing element is to be integrated with an LC voltage controlled oscillator (VCO) inside a frequency synthesizer to convert the real part of the permittivity into a change in the control voltage suitable for detection [41].
- Developing a prototype for an on-board self-sustained dielectric spectroscopy system for 1-8 GHz frequency range: An on-board sensing capacitor is embedded inside a phase shifter. Commercial correlators are used to translate the capacitance change into a voltage that can be measured [42, 43].

The advances in wireless communications motivate the trend of developing multi-band/multi-standard terminals for low-cost and compact-size transceivers. The design trend is now focused on using a single broadband front-end to accommodate all the standards as well as to reduce the chip area. Accordingly, the secondary objective in the earlier years of the PhD program was towards the implementation of wideband RF amplifiers for multi-band/multi-standard receiver's front end. This objective is summarized as follows:

- Implementation of a wideband Low-noise Amplifier (LNA) with noise cancellation: A broadband CMOS resistive feedback LNA with composite cross-coupled input CMOS pair is to be implemented and validated with noise figure reduction [44, 45].

- Implementation of a CMOS Distributed Amplifier (DA) with flat Bandwidth extension: A four stage distributed amplifier is to be implemented on CMOS using cross-coupled artificial transmission lines for uniform input impedance matching up to 16 GHz [46].

1.6 Organization of the Dissertation

The dissertation contains five sections, besides the introduction section, organized as follows;

- Section 2 presents a novel self-sustained CMOS microwave chemical sensor using a frequency synthesizer. The sensor targets the detection of the real part of the permittivity of organic chemicals in the frequency range of 7-9 GHz. The detailed analysis of the sensor and the frequency synthesizer, including electromagnetic simulation of the sensing element, is also presented. The system, including the sensing element and the frequency synthesizer, are implemented using 90 nm CMOS technology. A unique detection algorithm for sensing purpose is proposed including sensor calibration. The sensor is proved to detect the permittivity of organic liquids in the targeted frequency range with an error of 3.5% and to characterize binary mixtures with an error less than 2%.

- In Section 3, an on-board dielectric spectroscopy system in the 1-8 GHz frequency range is presented. A sensing capacitor exposed to the MUT is part of a true-time-delay (TTD) cell excited by a microwave signal at the sensing frequency of interest. The phase shift of the microwave signal at the output of the TTD cell compared to its input is a measure of the permittivity of MUTs.

TTD cells are designed to detect permittivities within the range of 1-30 considering non-ideal effects, such as electromagnetic coupling between adjacent TTD cells. Sensor calibration and detection algorithms are also applied. The permittivity of organic chemicals and fractional volumes of binary mixtures are detected with an error less than 2%.

- Section 4 explains a new broadband low noise amplifier (LNA) utilizing a composite NMOS/PMOS cross-coupled transistor pair to increase the amplification while reducing the noise figure. The implemented prototype using 90 nm CMOS technology is evaluated showing a conversion gain of 21 dB across 2-2300 MHz frequency range, an IIP3 of -1.5 dBm at 100 MHz, and minimum and maximum noise figure of 1.4 dB and 1.7 dB with a power consumption of 18 mW.

- In Section 5, a state-of-the-art four-stage distributed amplifier with coupled inductors in the gate-line is presented. The proposed coupled inductors in conjunction with series-peaking inductors in the cascode gain stages provide bandwidth extension with flat gain response without any additional power consumption. The new four-stage distributed amplifier, fabricated using 0.18 μm CMOS process, achieves a power gain of around 10 dB, return loss better than 16 dB, noise figure of 3.6-4.9 dB and a power consumption of 21 mW over 16 GHz 1-dB flat bandwidth.

- Finally, Section 6 concludes the discussion about novel microwave chemical sensors and broadband amplifiers with a proposed plan for future work.

2. A SELF-SUSTAINED CMOS MICROWAVE CHEMICAL SENSOR USING A FREQUENCY SYNTHESIZER

2.1 Introduction

As discussed in Section 1, integrated sensors on silicon,specially CMOS-based sensors, capable of direct detection of dielectric properties of chemicals/biochemicals are promising to achieve size and cost reduction, lower power consumption, enormous signal processing capabilities and high throughput for lab-on-chip applications. One challenge in the implementation of integrated sensors is the self sustainability for portable and implantable sensors. To the best of our knowledge, most reported microwave CMOS-based sensors require external signal generators, which is not suitable for self-sustained operation. Self-sustained sensors reported at microwave frequencies are normally based on discrete microwave resonators [47, 48]. In [47], frequency sweep generators and power detectors are used to find the shift in the magnitude response of a 70 mm long planar resonator when exposed to MUT. In [48], a dielectric sensor is reported based on detecting the variation of the reflected and transmitted signals through a microwave cavity resonator exposed to MUT. In this system, a PLL is employed to adjust the frequency of a VCO to match the resonant frequency of the resonator till no energy is reflected from the resonator. Planar and cavity resonators are bulky in size at microwave frequencies (1-10 GHz range). Therefore, self-sustained techniques in [47, 48] are all constrained by high cost and large size of measurement set-up and are not suitable for CMOS on-chip integration. Consequently, the implementation of a self-sustained on-chip dielectric sensor at microwave

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frequencies is of great importance for lab-on-chip applications.

In this section, a self-sustained integrated microwave dielectric sensing scheme is presented [41]. The sensor is based on using a sensing element (capacitor) which is part of a tank circuit of an LC VCO to detect the real part of the permittivity (ϵ_r') independent of the imaginary part (ϵ_r''). The sensing capacitor is located on the top metal layer of a CMOS process and is exposed to MUT. Thus, the capacitance value and the VCO output frequency are changed accordingly. Embedding the VCO inside a frequency synthesizer loop converts the variation of the capacitance into a change in the control voltage of the VCO. Accordingly, the proposed sensor makes use of the on-chip synthesizer for both microwave signal generation and capacitance to voltage conversion for a self-sustained operation. The output frequency of the VCO is chosen arbitrarily between 7 and 9 GHz, or the center frequency is chosen to be at 8 GHz, for proof of concept. The system can be synthesized for other center frequencies and wider frequency range by employing different designs for the synthesizer. A low-power Analog-to-Digital-Converter (ADC) is used to read the control voltage and perform further processing in the digital domain.

To our knowledge, this is the first work presented for integrated self-sustained permittivity sensors at such frequencies (7-9 GHz) and even at any frequencies above 1 GHz. This work targets the detection of the frequency dependent ϵ_r' of MUTs in the frequency locking range of the synthesizer (7-9 GHz). The detection of real part of the permittivity is enough to characterize the mixing ratios in mixtures which can be helpful in many applications, including: (1) the estimation of moisture content in grains, which are important in industry and agriculture [9]; and (2) medical applications such as the estimation of the glucose concentration in blood for blood sugar control [16, 17].

In this section, Subsection 2.2 presents the basic concepts and system operation of the sensor. Subsection 2.3 describes the circuit-level design and implementation of the sensing elements, PLL circuits and ADC. System integration and test setup are presented in Subsection 2.4. Subsection 2.5 discusses the electrical test results of the PLL and the ADC. Also, it presents the dielectric characterization of organic chemicals and the sensitivity characterization of the sensor. In Subsection 2.6, mixtures are characterized as an application for dielectric sensing and Subsection 2.7 concludes and summarized the work proposed in this section.

2.2 Basic Concept and System Functionality

2.2.1 Basic Concept

The effect of the frequency-dependent complex permittivity [6] of the MUT applied to a sensing capacitor appears as a parallel combination of a capacitance, C_s, and a frequency dependent resistance, $R(\omega)$. The value of the sensing capacitor, C_s, changes proportional to real part of the material's permittivity ($C_{s,mat} \approx \epsilon_r' C_{s,air}$, where $C_{s,air}$ and $C_{s,mat}$ are the capacitance values when exposed to air and MUT, respectively). However, the material's loss (ϵ_r''), affects the value of the parallel resistance, $R(\omega) = \frac{Q_c}{\omega C_s}$, where Q_c is the quality factor of the capacitor and is inversely proportional to the loss tangent of the material ($\tan\delta = \frac{\epsilon_r''}{\epsilon_r'}$). Therefore, the value of the resistance can be approximated as $R(\omega) \approx \frac{\epsilon_r'}{\omega \epsilon_r'' C_s} \approx \frac{1}{\omega \epsilon_r'' C_{s,air}}$. The sensing capacitor is a part of an LC tank circuit of a VCO. The presence of the MUT changes the capacitance C_s and changes the free-running oscillation frequency of the VCO. However, the change of the quality factor, Q_c, due to ϵ_r'' affects the amplitude of oscillation and the phase noise without affecting the oscillation frequency. Therefore, the change of the capacitance upon ϵ_r' variation can be detected independent of ϵ_r''. This work targets the detection of the real part of the permittivity, ϵ_r' which is useful for mixture characterization.

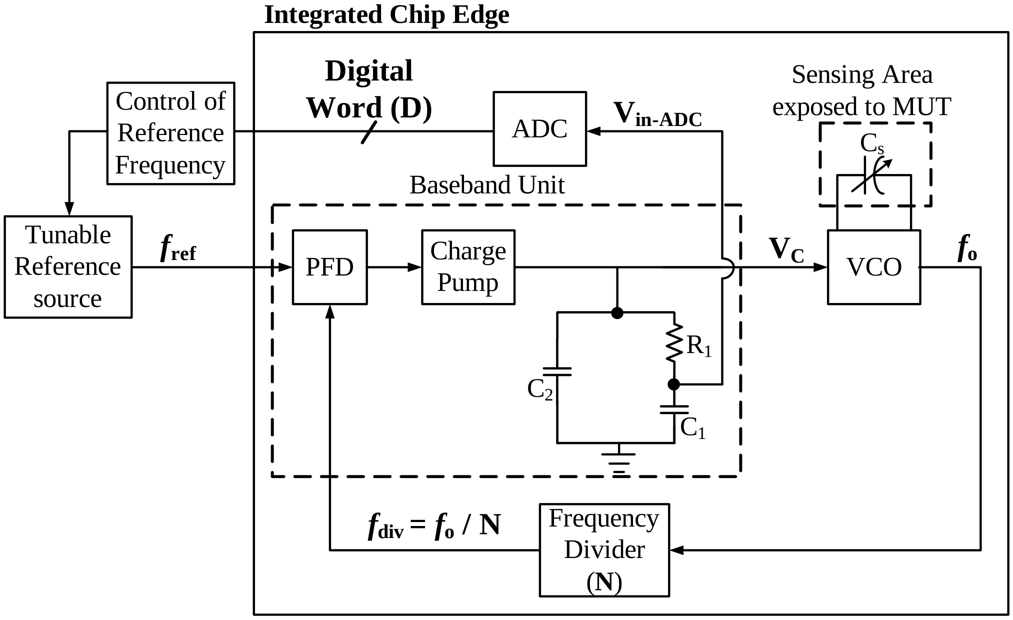

Figure 2.1: Block diagram of the dielectric sensor basic read-out circuitry based on a frequency synthesizer loop and an analog-to-digital converter

Fig. 2.1 shows the block diagram of the basic sensor and read-out circuitry based on a frequency synthesizer loop and an ADC for permittivity detection of MUTs. The VCO is located inside a type II frequency synthesizer loop [49, 51, 50] including a divide by N integer frequency divider, a phase and frequency detector (PFD), a charge pump and a loop filter. The synthesizer loop adjusts the VCO control voltage in a way that $f_o = N \cdot f_{ref}$, where f_o is the frequency at the output of the VCO and f_{ref} is the reference frequency. The sensing capacitance value (C_s) changes according to the permittivity of the MUT (ϵ_r') after exposure. However, for fixed values of N and reference frequency, f_{ref}, the frequency at the output of the VCO ($f_o = N \cdot f_{ref}$) remains constant and independent of ϵ_r'. Therefore, to maintain the same value of f_o, the change of the C_s is converted to a change in the control voltage, V_C, at the VCO input to compensate the variation of C_s. From Fig. 2.1, the voltage drop across C_1 is related to V_C through a low-pass response given by

$\frac{1}{1+j\omega C_1 R_1}$. Therefore, the voltage across C_1 changes according to V_C. This voltage is used as an input to the ADC ($V_{in,ADC}$) for further processing and computation. Spurs and high frequency noise at $V_{in,ADC}$ are suppressed or reduced compared to the control voltage (V_C) as will be explained later in Subsection 2.3.2. This voltage is digitized through the ADC and is used to control f_o through either a variable f_{ref} or a variable N as will be discussed later. The frequency synthesizer, the sensing element and the ADC are fully integrated on silicon. However, for simplicity and proof of concept, the frequency divider is fixed and the output of the ADC is used to tune an external source manually as a variable reference frequency (f_{ref}) to control the output frequency (f_o).

Table 2.1: Parameters for each block and loop filter components of the frequency synthesizer.

Center output frequency (f_o)	$\approx$ 8 GHz
Reference frequency (f_{ref})	$\approx$ 31.25 MHz
Frequency division ratio (N)	256
Loop bandwidth (f_c)	$\approx$ 0.5 MHz
Charge pump current (I)	25 μA
Loop filter elements	$C_1 =$ 35 pF, $C_2 =$ 0.57 pF, $R =$ 35 KΩ
Zero frequency (ω_z)	130 KHz
Pole frequency (ω_p)	7.7 MHz
VCO gain (K_v)	850 MHz/V

The parameters for each block of the synthesizer and the loop filter components are calculated based on Gardner's stability condition (Loop bandwidth $< f_{ref}/10$) [51, 50, 49] and a loop damping ratio (ζ) close to 1 (the loop phase margin $> 60°$)

and acceptable settling time less than 80 μs. The main design parameters of the frequency synthesizer are given in Table 2.1.

The system is simulated using Simulink to ensure the phase locking and stability of the loop. It is noticed from Table 2.1 that the value of C_1 is much larger than C_2. Accordingly, the capacitive loading effect of the ADC on the frequency synthesizer is minimal at $V_{in,ADC}$ compared to V_C.

2.2.2 System Functionality

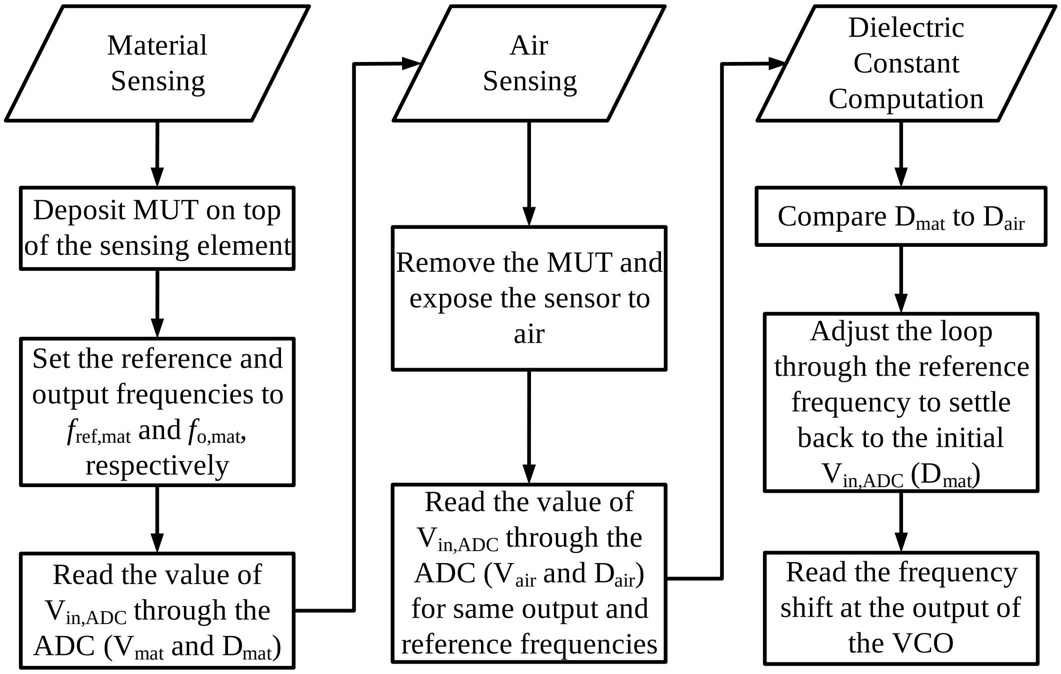

Figure 2.2: Flow-chart of ϵ_r' detection procedure through basic read-out circuitry.

Fig. 2.2 shows the flow-chart describing the procedure of the MUT ϵ_r' detection using the basic read-out circuitry in Fig. 2.1. The division ratio, N, is fixed and the reference frequency, f_{ref}, is tunable and controlled using the voltage ($V_{in,ADC}$)

MATLAB R2010a, MathWorks, Inc.

read out through the ADC. The target is sensing the dielectric constant of the MUT at a given sensing frequency (f_s). As the dielectric constant of air is equal to 1 for all frequencies and the dielectric constant of MUTs (such as organic chemicals) is varying with frequency [6], the material sensing should be performed first at the sensing frequency ($f_s = f_{mat}$) and then, the air sensing takes place and the output frequency shifts to f_{air}. Accordingly, the detected frequency shift ($\Delta f = f_{air} - f_{mat}$) is a measure of the permittivity of the MUT at $f_s = f_{mat}$. The detection procedure can be summarized in three steps

1) Material Sensing: The MUT is deposited on top of the sensing element and the sensing capacitor value changes to $C_{s,mat}$. The reference frequency is set to a value of $f_{ref,mat}$ and the output frequency is $f_{o,mat} = N.f_{ref,mat}$. The ADC input voltage ($V_{in,ADC} = V_{mat}$) is digitized and stored as a digital codeword (D_{mat}) for further processing.

2) Air sensing: The MUT is removed and the sensing elements are then exposed to air and the value of C_s changes to $C_{s,air}$. Since the dividing factor (N) and the reference frequency remain unchanged, the synthesizer loop keeps the PLL output frequency unchanged ($f_{o,mat}$) but the ADC input voltage changes from V_{mat} to V_{air} and the digital codeword at the ADC output changes from D_{mat} to D_{air} to compensate the variations of the sensing capacitor, C_s.

3) Dielectric Constant Computation: The sensing element is still exposed to air. The values of D_{air} and D_{mat} are compared to each other and then the reference frequency is changed to $f_{ref,air}$ so that the new ADC input voltage and digital codeword change back to the initial value, V_{mat} and D_{mat}, respectively. Also, the VCO output frequency moves to $f_{o,air}$ ($f_{o,air} = N.f_{ref,air}$). The frequency shift, $\Delta f = f_{o,air} - f_{o,mat} = N \cdot (f_{ref,air} - f_{ref,mat})$, is a representation of the sensing capacitor (C_s) variation, and is used to detect the relative permittivity of the MUT.

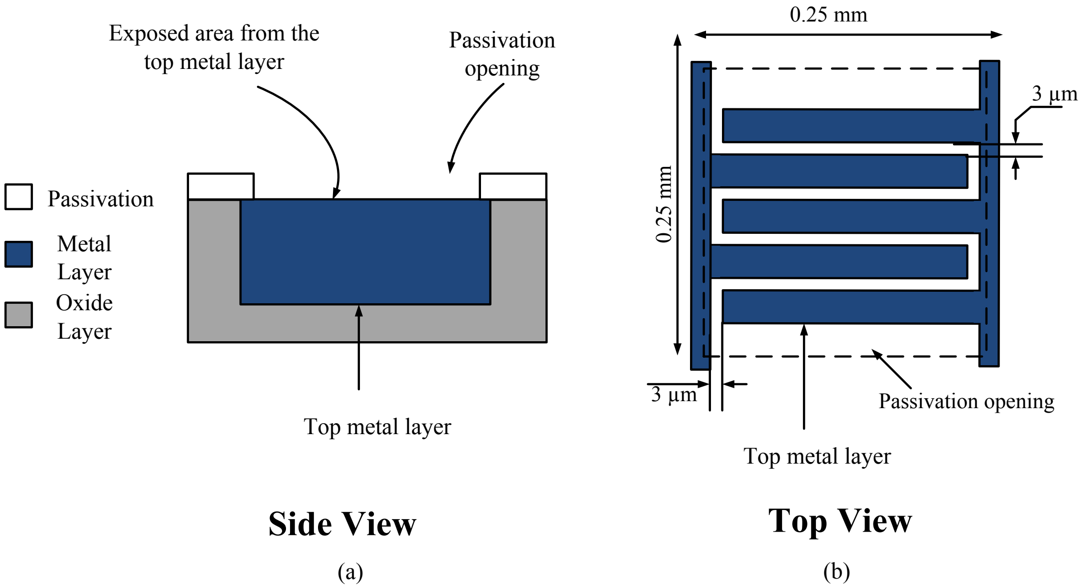

Figure 2.3: (a) Side view of the interdigitated capacitor with a passivation opening on the top, and (b) Top view of the interdigitated sensing capacitor implemented on top of the CMOS process with an opening in the passivation layer.

2.3 Circuit Implementation

2.3.1 Sensing Element

The sensing element is a capacitor whose capacitance changes upon exposure to MUT due to the change of the EM field distribution around it as a result of the permittivity variation. The sensing capacitor is implemented using the top metal layer (M8) in a 90 nm CMOS process and an opening in the passivation layer is provided to expose the capacitor directly to MUTs as shown in Fig. 2.3(a). The sensing capacitor has an interdigitated structure as shown in Fig. 2.3(b). The interdigitated capacitor is designed and simulated using the EM simulator Sonnet for different MUTs with ϵ_r' range of 1-30. The capacitor is a 5-finger structure with 3 μm finger separation and a total area of 0.25 × 0.25 mm^2. The capacitance value, C_s, versus ϵ_r' is shown

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Sonnet Inc. www.sonnet.com

in Fig. 2.4 for frequencies of 7, 8 and 9 GHz. Simulation results show a capacitance in air ($\epsilon_r' = 1$) of 100 fF which increases proportionally with the permittivity of the MUT up to 1.2 pF at $\epsilon_r' = 30$ for all three frequencies.

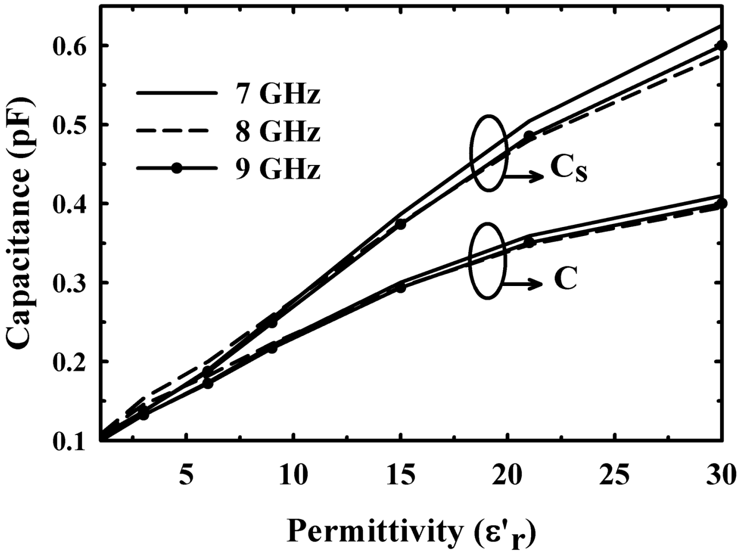


Figure 2.4: Simulated values of the sensing capacitance (C_s) and the equivalent series capacitance of C_s and C_f (C) versus the permittivity (ϵ_r') for frequencies of 7, 8 and 9 GHz.

As shown in Fig. 2.4, detecting materials with broad range of ϵ_r' imposes wide variations in the value of C_s leading to a wide change in the free running oscillation frequency of the VCO. Accordingly, to compensate the wide variations in C_s, the varactor in the VCO should have a wide tuning range equal to the tuning range of C_s, or the VCO should have a large gain (K_v) that might be infeasible or could destabilize the synthesizer loop. Therefore, a fixed parallel-plate capacitor, C_f, implemented between the metal layers M6 and M7 of the CMOS process, is used in series with

C_s to lower the effect of variations of C_s. For a fixed capacitor $C_f = 1.2$ pF, the equivalent series combinations of C_s and C_f, C, versus ϵ'_r of the MUT is shown in Fig. 2.4 at frequencies of 7, 8 and 9 GHz. From Fig. 2.4, C_s variation in the range of 0.1-1.2 pF is limited to 0.1-0.4 pF using the C_f for permittivity range of 1-30. Fig. 2.4 shows that employing C_f in series with C_s decreases the rate of variation of C with ϵ'_r ($\frac{\partial C}{\partial \epsilon'_r}$). Same EM simulations are performed for different values of ϵ''_r in the range of 1 to 30. Simulations show that values of C_s and C vary with ϵ'_r independent of ϵ''_r.

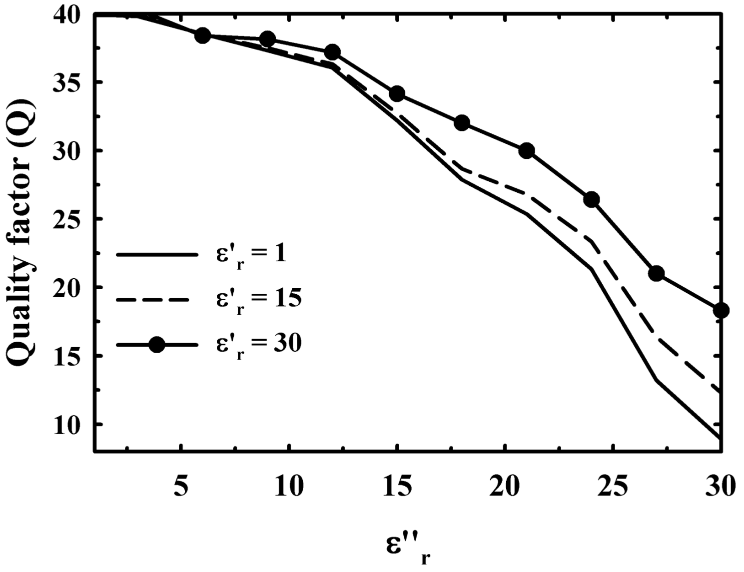


Figure 2.5: Simulated quality factor of the sensing capacitor versus the ϵ''_r of the MUT at a frequency of 8 GHz for different values of ϵ'_r.

The effect of the imaginary part of the permittivity of the MUT (ϵ''_r) appears as a degradation in the quality factor of the sensing capacitor (C_s) as shown in Fig. 2.5. This figure shows the values of the quality factor (Q) of the sensing element versus

ϵ_r'' for $\epsilon_r' = 1$, 15 and 30. As shown in Fig. 2.5, the quality factor of the capacitor is much larger than 1 ($Q^2 >> 1$). Accordingly, the change in the capacitance C_s due to the resistive part of C_s (by a factor of $\frac{1}{1+\frac{1}{Q^2}}$), can be ignored. In conclusion, ϵ_r'' affects the quality factor of the tank and the oscillation amplitude without affecting the sensing capacitance and the oscillation frequency. Accordingly, the detection of ϵ_r' is independent of ϵ_r''

2.3.2 VCO

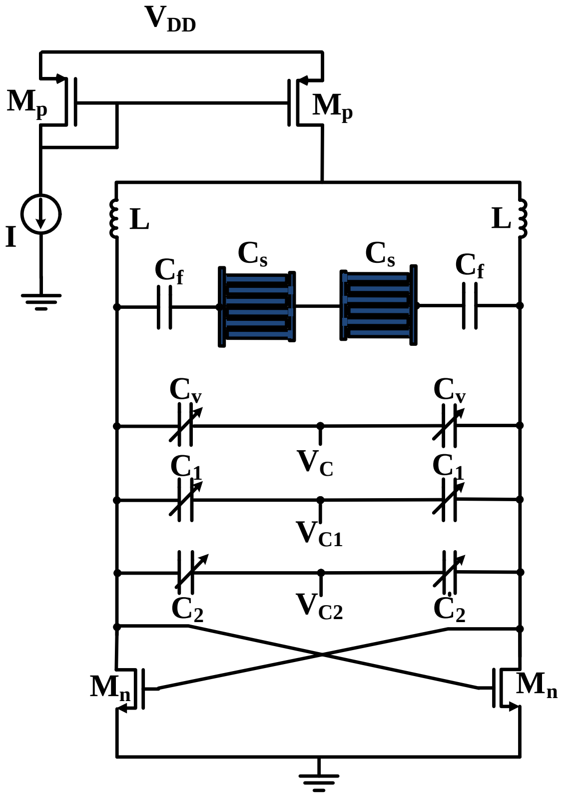


Figure 2.6: Circuit schematic of the VCO with sensing capacitors as part of the LC tank.

In order to detect the change in the capacitance C_s (or C) caused by the deposition of the MUT on top of the sensing element, a VCO is employed to implement a self-sustained mechanism for chemical detection. Fig. 2.6 shows the schematic of a differential cross-coupled VCO employing a sensing capacitor pair in addition to the conventional tank including lumped inductors and varactors. Capacitance variation caused by MUT deposition results in a shift in the oscillation frequency of the VCO. The control voltage at the output of the loop filter in the synthesizer loop (Fig. 2.1), V_C, is used to control the varactor C_v. However, the extra varactors, C_1 and C_2, are also parts of the tank circuit to provide additional degree of freedom in controlling the VCO gain and compensate for PVT variations. Both C_1 and C_2 can be manually tuned using external control voltages, V_{C1} and V_{C2}, respectively. Also, they can adjust the VCO output frequency to sense the values of ϵ_r' at a wider frequency range as will be discussed in Subsection 2.5.

VCO phase noise is chosen such that the overall variance of the noise voltage at $V_{in,ADC}$ (Fig. 2.1) is much less than half of the ADC resolution to make the sensor resolution limited by the ADC performance. The ADC performance is presented later in Subsection 2.5.2 with an ADC resolution of 2.2 mV. Assuming that the phase noise of the VCO is injected as a noise source at the output of the synthesizer, the VCO phase noise is mapped into voltage noise at the control voltage (V_C) through a bandpass response centered around the closed loop bandwidth of the synthesizer (f_c). This response is approximately given by $A_{BP}(j\omega) = A_{CL}(j\omega) \cdot \frac{1}{N} \cdot \frac{j\omega}{K_{VCO}}$; where $A_{CL}(j\omega)$ is the closed loop gain of the frequency synthesizer, N is the frequency division ratio and K_{VCO} is the VCO gain. The first order low-pass filtering through R_1 and C_1, with corner frequency of $\omega_z = 2\pi \cdot 130$ Krad/s, suppresses the high frequency noise at $V_{in,ADC}$. Also, this filtering helps in reducing the reference spurs, at around 30 MHz offset (more than two decades away from the corner frequency), by more than 40 dB. Therefore, we can assume that the reference spurs do not affect the detection accuracy. Accordingly, the overall noise variance ($\overline{V^2_{n,in,ADC}}$) at $V_{in,ADC}$ due to the VCO phase noise ($PN(j\omega)$) is approximately given by:

$$\overline{V^2_{n,in,ADC}} = 2 \cdot \int_{f_1}^{f_2} |PN(j\omega)| \cdot |A_{CL}(j\omega) \cdot \frac{1}{N} \cdot \frac{j\omega}{K_{VCO}} \cdot \frac{1}{1+\frac{j\omega}{\omega_z}}|^2 \, df \tag{2.1}$$

Due to the bandpass response around the closed loop bandwidth (f_c), the value of VCO phase noise at the closed loop bandwidth (f_c) offset is critical in the design. Also, the integration limits, f_1 and f_2, can be set to $f_c/10$ and $10 \cdot f_c$; respectively. Accordingly, the phase noise of the VCO should be chosen such that $\overline{V^2_{n,in,ADC}} < \eta \cdot \frac{\text{ADC resolution}}{2}$, where η is a margin factor ($\eta < 1$) to take into account other noise sources inside the loop and also the ADC noise. According to this analysis, a VCO phase noise at 500 kHz offset of -90 dBc/Hz results in noise standard deviation of 64 μV which is 30 times less than the ADC resolution (2.2 mV) ($\eta = 0.07$). Accordingly, the sensor resolution is limited by the ADC resolution and -100 dBc/Hz of phase noise at 500 kHz offset provides acceptable performance. Table 2.2 shows the VCO circuit parameters for a center frequency of 8 GHz and an average VCO gain of 850 MHz/V.

Table 2.2: VCO circuit parameters and elements values.

$(\frac{W}{L})_n$	$(\frac{W}{L})_p$	V_{DD} (V)	I (mA)	L (nH)
$\frac{72\mu m}{0.1\mu m}$	$\frac{90\mu m}{0.1\mu m}$	1.3	11	0.2

C_s (pF)	C_f (pF)	C_v (pF)	C_1 (pF)	C_2 (pF)
0.1-0.6	1.2	0.6-0.9	0.25-0.7	0.25-0.7

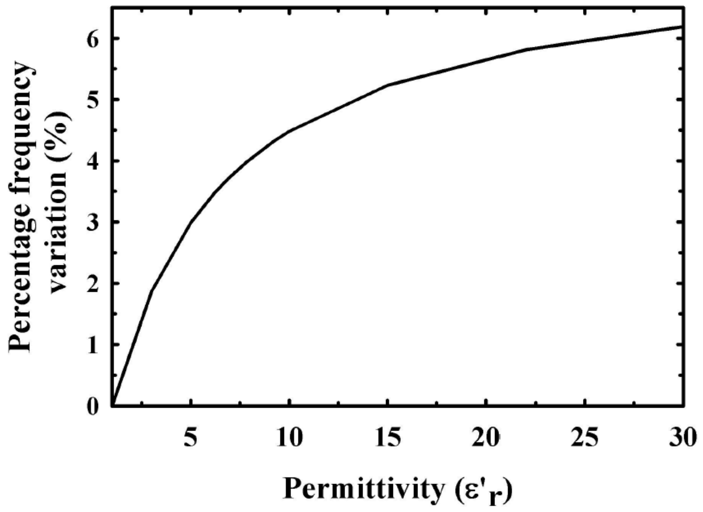
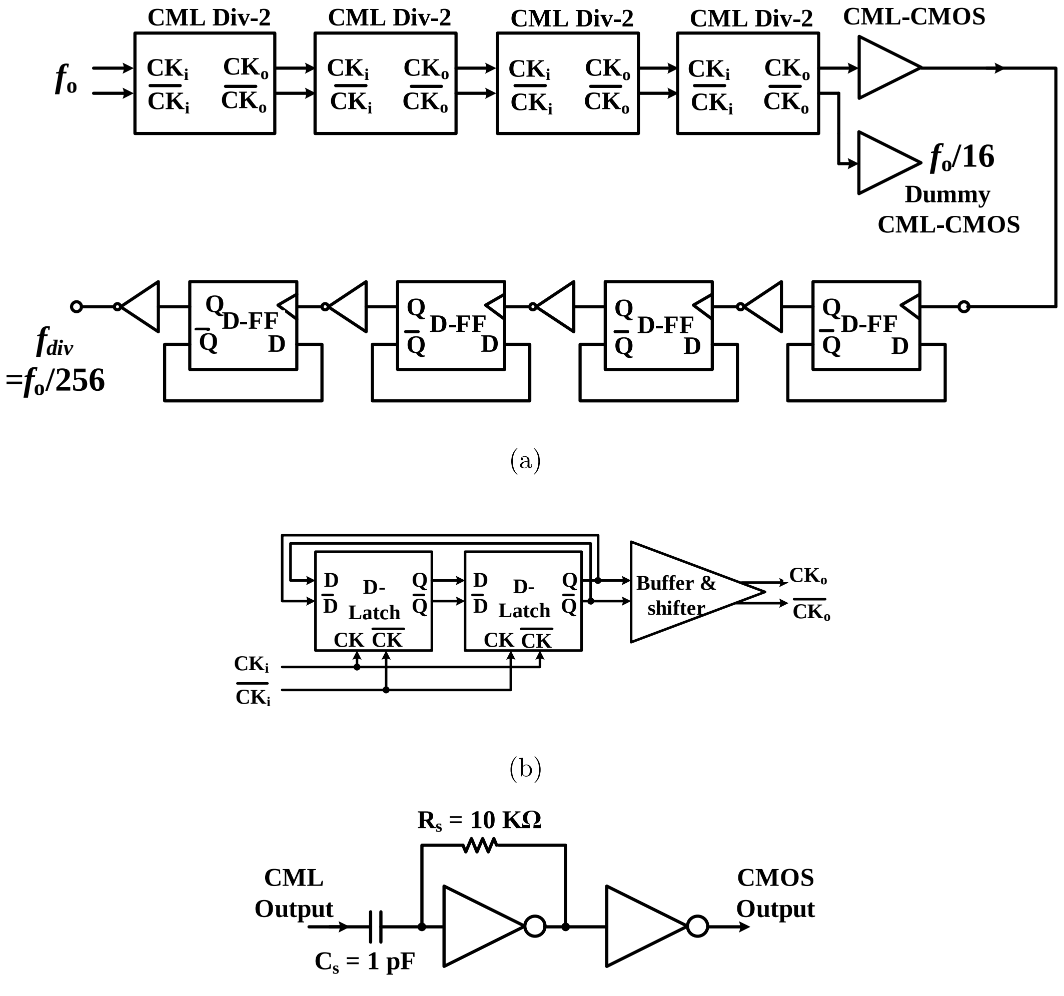


Figure 2.7: Simulated percentage variation in the VCO output frequency for MUTs with $1 < \epsilon_r' < 30$ compared to the case of $\epsilon_r' = 1$.

The sensing capacitors are simulated using Sonnet and their two-port models are extracted and embedded into Cadence to simulate the VCO. Fig. 2.7 shows the simulated percentage variation in the free running frequency of the VCO when exposed to MUT with a permittivity range of 1-30 compared to the case when exposed to air ($\epsilon_r' = 1$) at $f_0 = 8$ GHz. A percentage variation up to 6.2 % is observed for permittivities up to 30. Similar to Fig. 2.4, the rate of frequency change decreases for large values of permittivity. The post-layout simulations of the VCO show that the maximum and minimum values of C_s, C_v, C_1 and C_2 correspond to oscillation frequencies of 7 and 9.5 GHz respectively. Also, the VCO achieves a minimum output peak voltage of 200 mV and a phase noise of -105 and -111 dBc/Hz at 0.5 and 1 MHz offsets; respectively.

Spectre 6.2, Cadence 2008.



(a)

(b)

(c)

Figure 2.8: (a) Schematic of the frequency divide-by-256 circuit, (b) Schematic of the CML based divide-by-2 circuit and (c) schematic of CML to CMOS converter.

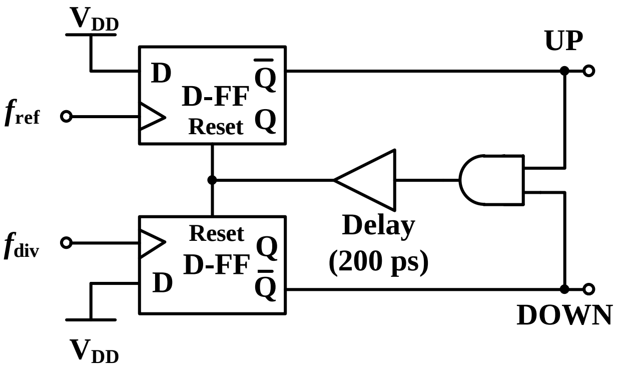
Frequency dividers are categorized by operating frequency into: (i) Current-Mode Logic (CML) dividers adopted for high frequency operation and (ii) Static CMOS

D-FF dividers adopted for low frequencies [52, 53].

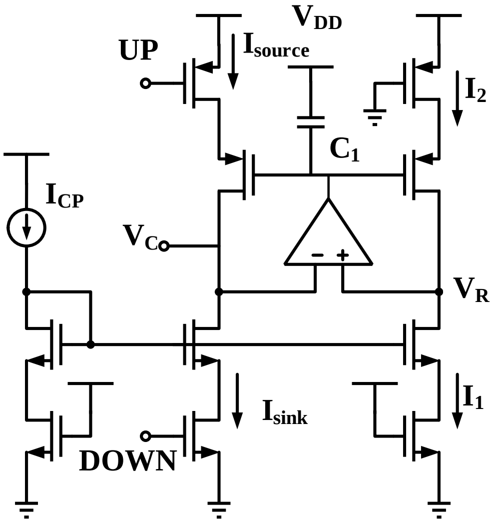
Fig. 2.8(a) shows the frequency divide-by-256 circuit consisting of: (1) Asynchronous divide-by-16 using four cascaded divide-by-2 circuits, each employs a cross-coupled CML D-latch and a buffer and level shifter (Fig. 2.8(b)); (2) CML-to-CMOS converters (Fig. 2.8(c)) used to change the signaling from CML to CMOS level. It is composed of a series capacitor for DC block followed by a self-biased inverter with shunt resistor followed by another inverter for amplification. A dummy converter is connected to unused output node to balance loading effect, and (3) CMOS-logic divide-by-16 using four cascaded D-FFs, each triggered by the input clock. The total power consumption of the divider is 0.5 mW.

2.3.4 PFD and Charge Pump

A tri-state PFD [54] is utilized in the PLL as shown in the Fig. 2.9(a). A 200 ps delay is implemented by inverter chains before the reset of the D flip-flop to mitigate the PFD dead zone issue. The timing mismatch of the PFD output signals (UP and DOWN signals) is minimized by proper design and layout. Fig. 2.9(b) shows the simplified schematic of the charge pump [55]. A rail-to-rail operational amplifier is used to decrease the mismatch between the sink and source currents to decrease the variation in the charge pump current and the control voltage (V_C). The op-amp virtually shorts V_C and V_R to reduce the current mismatch between I_{Sink} and I_1 and between I_{Source} and I_2. Since I_1 and I_2 are matched, I_{Sink} and I_{Source} are ideally matched too. A capacitor C_1 is needed to compensate the phase margin of the op-amp over the required range of V_C. With the op-amp, the mismatch of the charge pump current is improved to less than 3% over a control voltage range of 80% the power supply voltage. The power consumption of PFD and charge pump is 0.1 mW.



(a)



(b)

Figure 2.9: Schematics of (a) PFD and (b) Charge pump.

2.3.5 ADC

When the PLL is locked, noise and spurs of the control voltage would limit the sensor resolution. While the ADC samples $V_{ADC,in}$, the disturbance (including noise, glitches and ripples) at the control voltage has to be smaller than half the ADC quantization error in order to validate the accuracy of the ADC output. The disturbance at $V_{ADC,in}$ results from the mismatch of sink and source charge pump currents, leakage current, charge injection, and reference clock feed-through.

Many ADC architectures, such a Sigma-Delta, dual slope and algorithmic architectures, can be used for this sensing purpose. Sigma-Delta ADCs are suitable for a very high resolution at the cost of area, power consumption and complexity. Dual slope architectures have the draw-back of more introduced noise and non-linearities. Algorithmic ADCs have small area and low-power consumption with enough resolution for our sensing purpose. That is why algorithmic ADC is selected over other ADC architectures in this application, especially with the low-speed requirements for sensing purpose. The circuit of the algorithmic ADC is shown in Fig. 2.10. It operates with two non-overlapping clocks, ϕ_1 and ϕ_2. The architecture employs 10 clock cycles to obtain a 9-bit digital output. During the clock phase ϕ_s, the input is sampled onto C_1, while the amplifier is reset. The operational amplifier (OPAMP) output offset is sampled and stored onto C_3. Although C_3 is not necessary for the ADC operation, it improves its resolution under large mismatch conditions by cancelling the amplifier's offset.

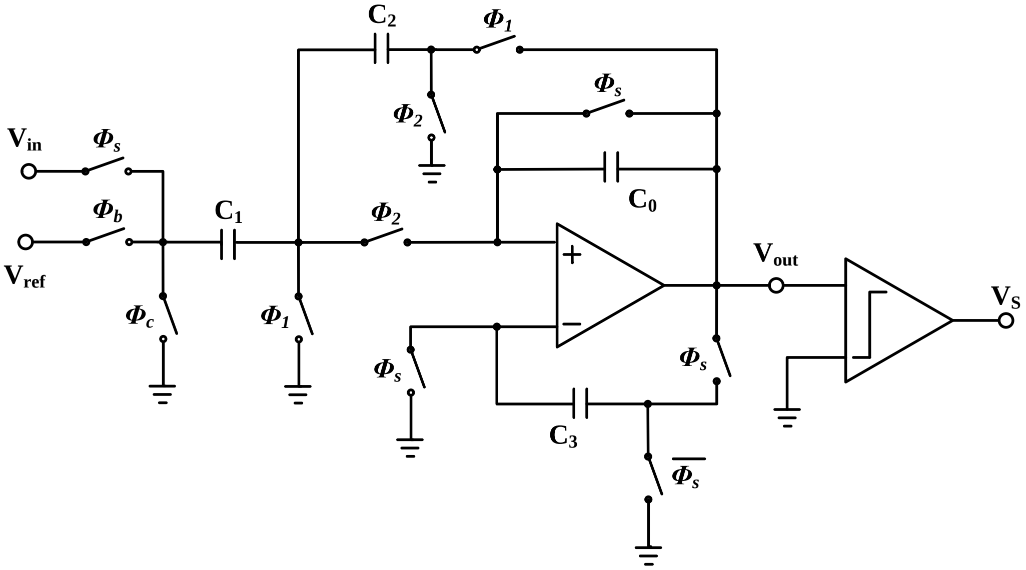


Figure 2.10: Schematic of the algorithmic Analog to Digital Converter. The control clock phases are implemented using logic operations as $\phi_b = \phi_1 V_s + \phi_2 \bar{V_s}$ and $\phi_c = \phi_2 V_s + \phi_1 \bar{V_s}$.

The clocks ϕ_b and ϕ_c are defined in the caption of Fig. 2.10. They should be non-overlapping and be made logic low during the ϕ_s phase. The conversion is carried out during the clock cycles after the sampling phase ϕ_s. During the clock phase ϕ_1, the output voltage V_{out} is sampled onto C_2. The purpose of this phase is to multiply the output by a factor of two during ϕ_2. If the output bit during the previous conversion cycle was determined to be logic high, then C_1 is connected to ground during this clock phase; otherwise, V_{ref} is connected to C_1. The process of multiplying the input by two and subtracting or adding V_{ref} can be performed by using only two capacitors, however, using three capacitors allows us to increase its resolution through the alternating switching technique. Charge injection from the switches is minimized by turning off the switches in a proper sequence. For instance, during the sampling phase, the ϕ_s switch used to sample the offset should turn off after the ground switch is opened. Furthermore, the ϕ_1 switch should act as an early switch preventing charge injection from the input switch onto C_1. The comparator detects the sign of the output of the operational amplifier, V_s, to update the ϕ_b and ϕ_c clock phases. This process continues until 9 bits have been determined.

2.4 System Integration and Test Setup

The chemical sensor is implemented using a 90 nm CMOS process. Spiral inductors are used in the VCO and are implemented using the top metal layer (M8), which is the thickest and farthest metal layer from the substrate improve its quality factor (around 12 at 8 GHz). The sensing interdigitated capacitor (C_s) is implemented using the M8 layer with passivation opening for material exposure. The Metal-Insulator-Metal capacitors of the CMOS process are used for all other capacitors including the fixed capacitor (C_f) and the loop filter capacitors. The varactors used in the VCO (C_v, C_1 and C_2) are implemented using PMOS varactors of the CMOS process for wider tuning range ($\approx 50\%$) and higher quality factor (≈ 35). Transistors and varactors are laid out with maximum number of fingers and close to minimum width to minimize the series gate resistance. Tapering is used to connect inductors to transistors and varactors to minimize the parasitic capacitance due to discontinuities. Several independent ground signals are used for each block. The critical blocks are isolated using diffusion regions to prevent leakage between ground signals to avoid glitches and spikes that can affect the operation of different blocks.

Fig. 2.11 shows a microphotograph of the fabricated chemical sensor. The whole system occupies an area of $2.5 \times 2.5\ \text{mm}^2$ (including the testing pads). The fabricated chip is encapsulated inside an open cavity micro lead frame package (MLP) to ensure that the sensing elements are exposed to air and MUTs. Input and output AC/DC signals are applied and monitored using an FR-4 printed circuit board (PCB).

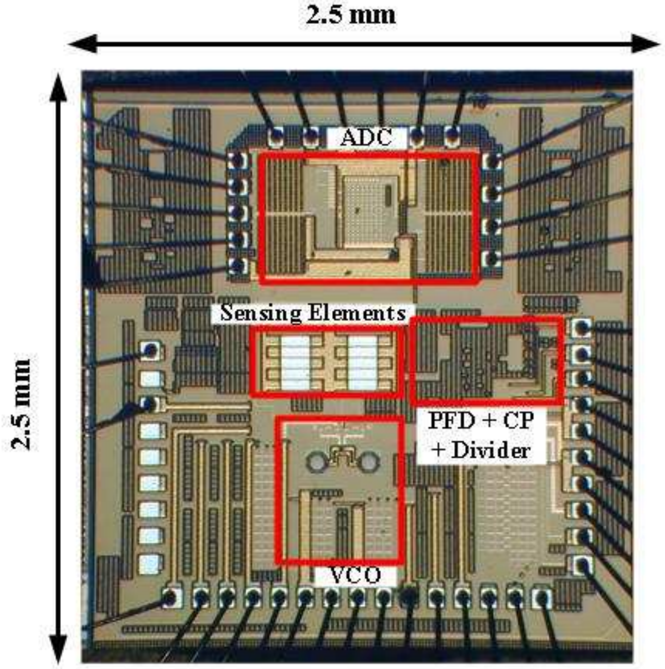
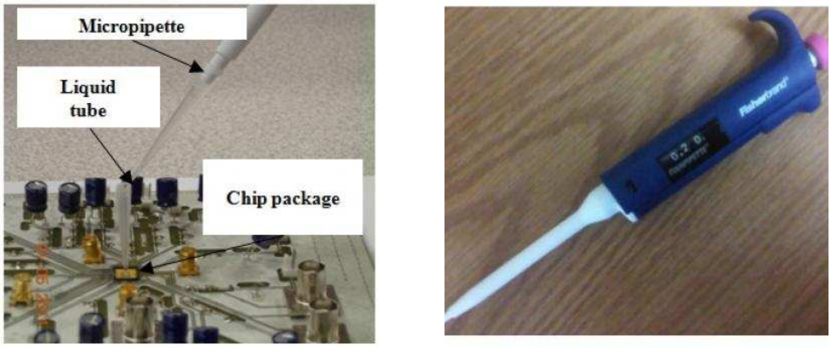


Figure 2.11: Microphotograph of the fabricated CMOS chemical sensor with a chip size of 2.5 × 2.5 mm^2 (including the testing pads).

A cylindrical tube is fixed and glued on top of the sensing elements and the passivation opening as shown in Fig. 2.12(a). The tube contains the liquid subject to characterization. A FinnpipetteII single-channel micropipetter shown in Fig. 2.12(b) is employed to insert liquids inside the tube with a volume range of 0.2-20 μL. The pipette is also used to remove the chemical after the material sensing step and commercial compressed gas dusters are then used to clean the sensor from the chemical to be used in the next detection steps.

Available [online]: http://www.thermoscientific.com
www.dust-off.com



(a) (b)

Figure 2.12: (a) Photograph of the open cavity MLP with a tube on top and (b) Photograph of the micropipette used to insert defined volumes of liquids inside the tube.

2.5 Experimental Procedures and Results

In this subsection, the circuits, including the frequency synthesizer and the ADC, are electrically characterized. Then, the experimental chemical detection and sensor characterization are presented.

2.5.1 Characterization of the Frequency Synthesizer

The bandwidth of the PLL is around 500 kHz. The reference frequency is ranging from 27.34-37.11 MHz. All circuit blocks are powered by a 1.3 V supply. The measured power consumptions are 14.3, 0.5 and 0.1 mW for the VCO, frequency dividers and charge pump; respectively. The spectrum and phase noise measurements of the frequency synthesizer are carried out by an Agilent E4446A spectrum analyzer. When exposed to air, the frequency synthesizer measurements showed a locking range of 7-9.5 GHz corresponding to a reference frequency range of 27.34-37.11 MHz. Fig. 2.13 shows the variation of the output frequency with the steady state value of $V_{in,ADC}$, which is the same as V_C. The voltages V_{C1} and V_{C2} of the varactors are tuned manually to cover the locking range of 7-9.5 GHz. Accordingly, frequency scanning can be performed to detect the frequency dependent permittivity. However, when MUT is deposited on top of the sensor, the locking range suitable for permittivity scanning will be limited only from 7 to 9 GHz due to increase of C_s.

The output spectrum of the frequency synthesizer when operating at a reference frequency of 31.57 MHz, or an output frequency of 8.082 GHz, is shown in Fig. 2.14. This measurement is performed when the ADC is turned ON at an ADC sampling rate of 1.1 kHz. The spectrum shows a 57.5 dBc reference spur rejection at a frequency offset of 31.57 MHz. Based on Fig. 2.14, no spurious effect at the sampling frequency of the ADC (at 1.1 kHz) is remarked. Fig. 2.15 shows the dependence of the measured reference spur rejection on the output frequency in the range of 7-9.5 GHz. The plot shows that the spur rejection is better than 55 dBc for the whole frequency range.

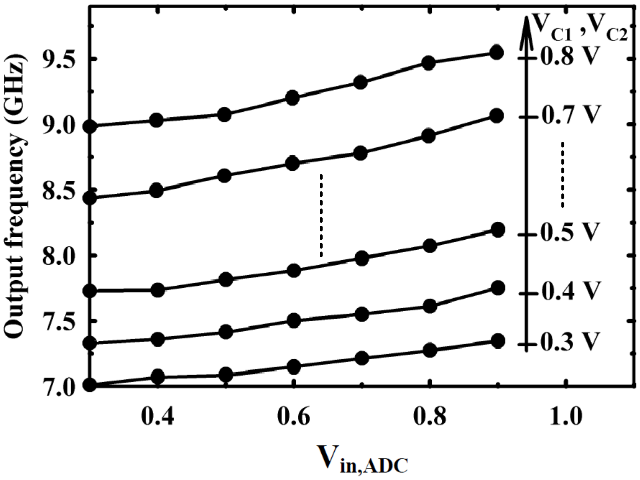


Figure 2.13: Measured output frequency of the frequency synthesizer versus $V_{in,ADC}$ while varying the voltages V_{C1} and V_{C2} manually when the sensor is exposed to air.

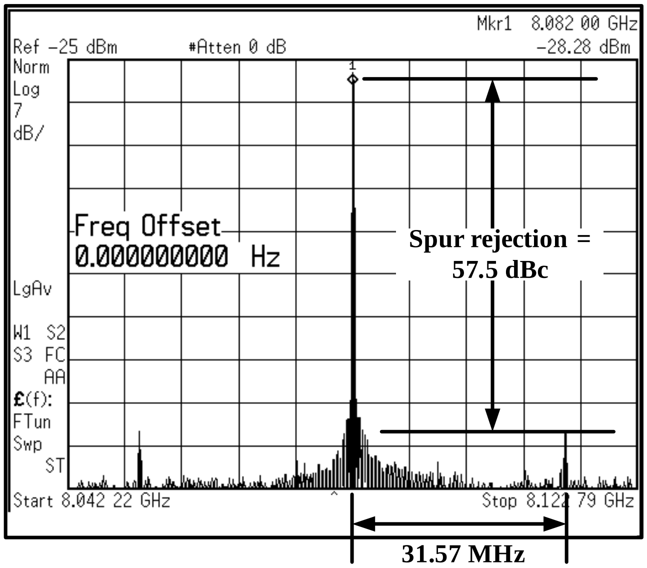


Figure 2.14: Measured output frequency spectrum at 8.082 GHz output frequency and measured reference spur rejection at 31.57 MHz offset.

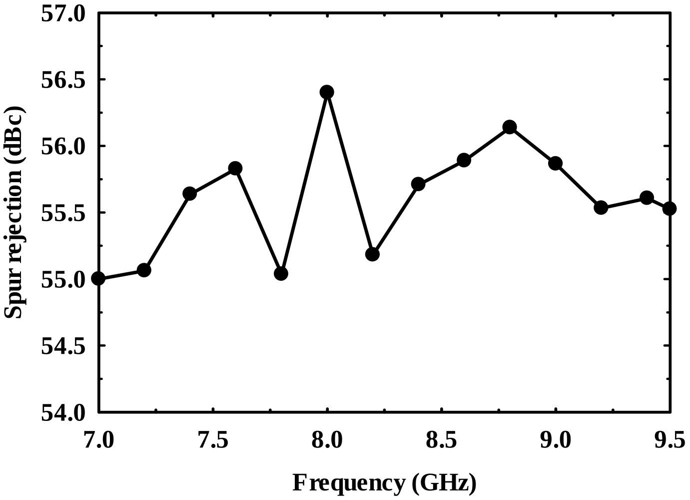
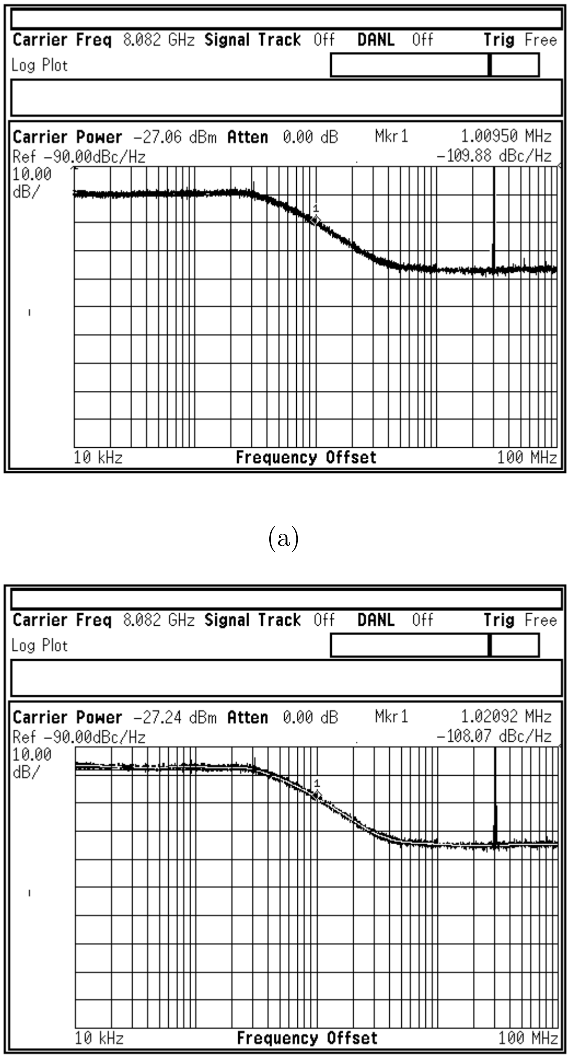


Figure 2.15: Measured reference spur rejection vs. the output frequency.



(b)

Figure 2.16: Measured output phase noise spectrum at 8.082 GHz carrier frequency: (a) the ADC is OFF; and (b) the ADC is ON.

Fig. 2.16(a) and (b) show the phase noise measurements of the frequency synthesizer when the ADC is turned OFF and ON; respectively. These measurements show that the ADC noise degrades the phase noise at the output of the synthesizer by less than 2 dB. In Fig. 2.16(b), the phase noise at the closed loop bandwidth (≈500 kHz) and 1 MHz offsets are -102 and -108 dBc/Hz; respectively. These values of phase noise are enough to ensure that the noise variations on the input voltage of the ADC are less than half the ADC resolution as proved in Subsection 2.3.2.

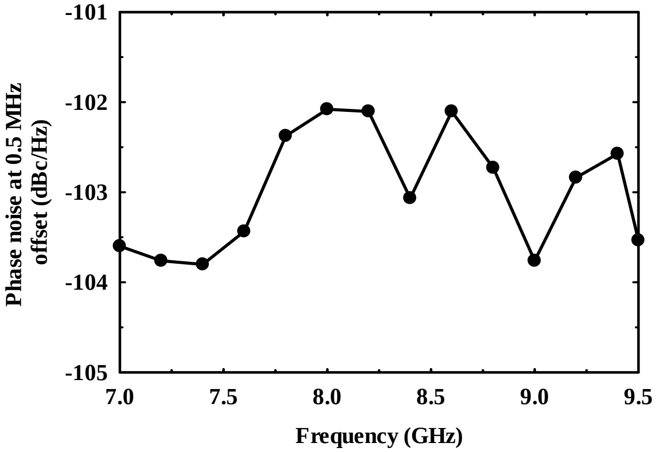


Figure 2.17: Measured phase noise at 0.5 MHz offset vs. the output frequency, when the ADC is ON.

Fig.2.17 shows the dependency of the measured phase noise at 0.5 MHz offset on the output frequency. This plot proves phase noise below -102 dBc/Hz at 0.5 MHz offset for the whole frequency range. The PLL has a settling time of around 70 μs. Table 2.3 shows the summary of the performance of the frequency synthesizer.

Table 2.3: Summary of the performance of the frequency synthesizer.

Frequency range	Phase noise at 0.5 MHz offset	Reference spur rejection	Settling time	Supply Voltage	Power consumption
7-9.5 GHz	<-102 dBc/Hz	>55 dBc	70 μs	1.3 V	15 mW

2.5.2 ADC Characterization

The algorithmic ADC consumes 1.5 mW in an area of 1.1 × 0.6 mm^2. The input dynamic range of the ADC ranges from 0.25 to 0.95 V. The measured FFT plot with sampling rate of $f_{sampling} = 1.1$ kHz is shown in Fig. 2.18. The values of SNR are 61 and 52 dB with noise integration in 100 Hz and 550 Hz ($f_{sampling}/2$) bandwidth, respectively. The sensor measurements are performed with an ADC sampling rate of 1.1 kHz without any digital filtering, which is equivalent to noise integration in a band of 550 Hz ($f_{sampling}/2$), or an SNR of 52 dB. This is approximately equivalent to a mean effective number of bits (ENOB) of 8.3 bits, or an ADC resolution of around 2.2 mV.

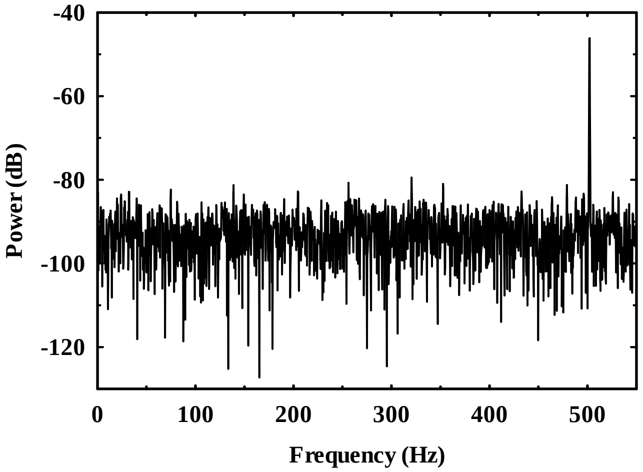
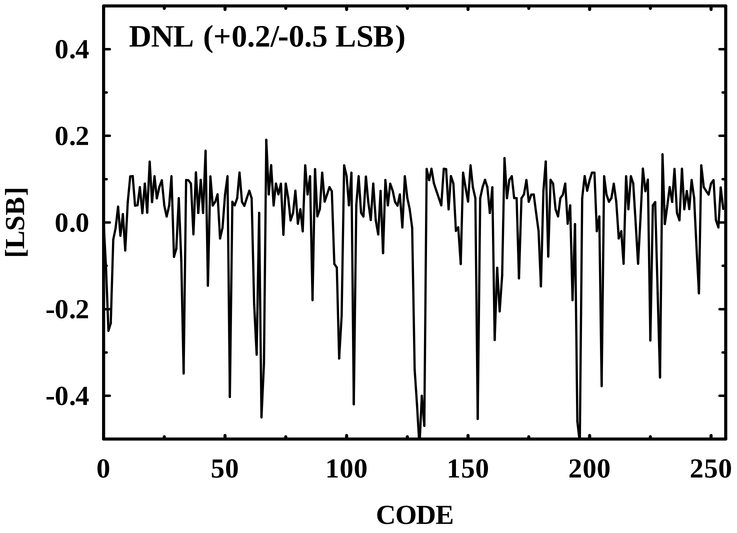
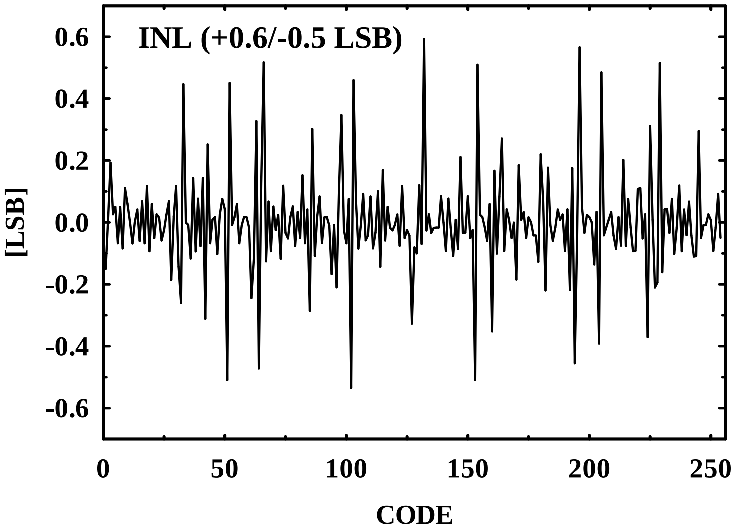


Figure 2.18: FFT plot of the ADC with sampling rates of 1.1 kHz with 10 mV_{pp} input signal.

Applying a slow ramp with a frequency of 2 Hz, the measured DNL and INL are within +0.2/-0.5 LSB and +0.6/-0.5 LSB, as shown in Fig. 2.19(a) and (b), respectively. Table 2.4 summarizes the performance of the ADC.



(a)



(b)

Figure 2.19: Measured (a) DNL and (b) INL of the ADC by applying a 2 Hz ramp signal.

Table 2.4: Summary of the performance of the ADC.

Sampling Rate	SNR/ENOB SNR/ENOB	SNR/ENOB SNR/ENOB	DNL DNL	INL INL	Power consumption
1.1 kHz	52 dB / 8.3 bits at BW = 550 Hz	61 dB / 9.8 bits at BW = 100 Hz	+0.2/-0.5 LSB	+0.6/-0.5 LSB	1.5 mW

2.5.3 Permittivity Dependence on Frequency and Liquid Volume

As discussed in Section 1, the permittivity changes with frequency according to the cole-cole model represented by [6]

$$\epsilon_r(\omega) = \epsilon_r'(\omega) - j\epsilon_r''(\omega) = \epsilon_{r,\infty} + \frac{\epsilon_{r,0} - \epsilon_{r,\infty}}{1 + (j\omega\tau)^{1-\alpha}} \tag{2.2}$$

The Cole-Cole equation gives the values of the complex permittivity as a function of the frequency and will be used to verify the measurements. Also, the change of EM field around the sensing capacitor depends on the volume of the liquid under test. Accordingly, the sensing is performed for each MUT for volume range of 0.2-20 μL by inserting different volumes of MUTs inside the tube on top of the sensing element using the micropipette. During dielectric characterization, two parameters are tuned: (1) liquid's volume (S_v) in the range of 0.2-20 μL, and (2) sensing frequency (f_s) in the range of 7-9 GHz. Then, the permittivity of the MUT is estimated for each combination of (f_s,S_v) and is denoted by $\epsilon_r'(f_s, S_v)$. To detect $\epsilon_r'(f_s, S_v)$ for a particular MUT, the procedure in Fig. 2.2 is applied to get the frequency shift for each volume and sensing frequency, $\Delta f(f_s, S_v)$.

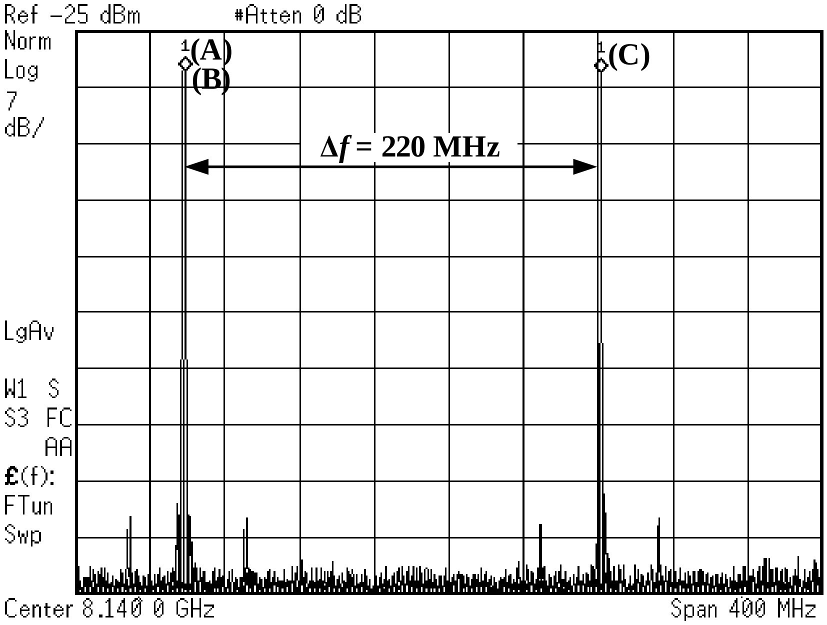


Figure 2.20: Output frequency spectrum at different steps of detecting the permittivity of Ethyl acetate at $f_s = 8$ GHz and $S_v = 20\ \mu$L.

As an example, Ethyl Acetate as a MUT is characterized at $f_s = 8$ GHz and $S_v = 20\ \mu$L. The detection procedure in Fig. 2.2 is applied as follows: (1) Material sensing: the reference frequency is set to $f_{ref,mat} = f_s/N = 31.25$ MHz, the varactors C_1 and C_2 are tuned to lock the synthesizer at $f_s = 8$ GHz as shown in Fig. 2.20 (point A). The ADC output (D_{mat}) is read out with time as shown in Fig. 2.21 (plot A). The average value of the ADC output is $D_{mat} = 1DE$ in the hexadecimal basis, (2) Air sensing: Ethyl acetate is removed, the output frequency (point B in Fig. 2.20) is the same and the ADC reading changes to $D_{air} = 0E1$ (plot B in Fig. 2.21); and (3) the reference frequency is tuned till the average of the ADC output settles back to D_{mat}

(plot C in Fig. 2.21) with $f_{ref,air} = 32.11$ MHz, or an output frequency of 8.221 GHz (point C in Fig. 2.20). In each step, multiple ADC readings are taken out and averaged for better detection accuracy. The measured frequency shift $|\Delta f(8\text{ GHz}, 20\ \mu\text{L})| = N \cdot (f_{ref,air} - f_{ref,mat})$, is around 220 MHz.

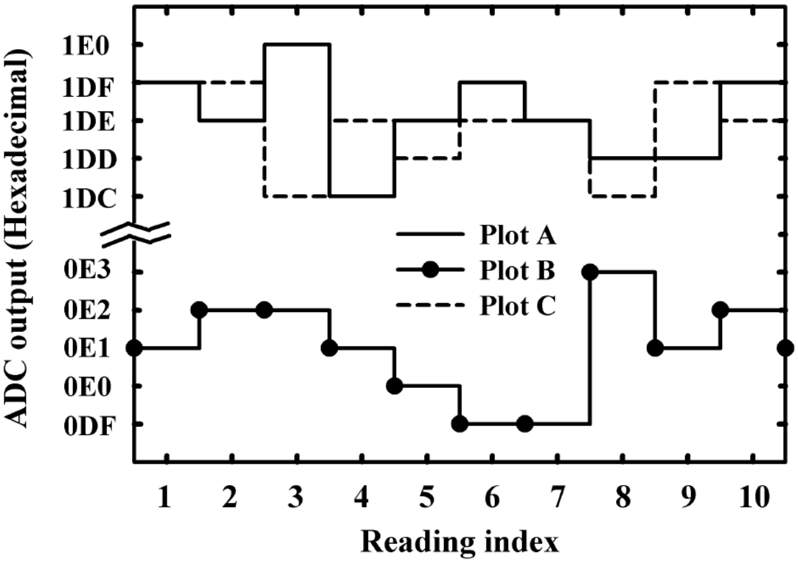


Figure 2.21: ADC digital output at different steps of detecting the permittivity of Ethyl acetate at $f_s = 8$ GHz and $S_v = 20\ \mu$L.

2.5.5 Dielectric Characterization of Organic Chemicals

A variety of organic chemicals are used for characterization, including: (1) Alcohols: Ethanol ($CH_3 - CH_2 - OH$), Methanol ($CH_3 - OH$), Isopropanol ($CH_3 - CH_3 - CH - OH$) and 2-butyl-alcohol ($CH_3 - CH - OH - CH_2 - CH_3$); (2) Organosulfur compounds: Di-methyl-sulphoxide, or DMSO ($CH_3 - CH_3 - SO$); (3) Glycols: Ethylene glycol ($C_2H_6O_2$); (4) Ketones: Acetone ($CH_3 - CH_3 - CO$); (5) Esters: Ethyl-acetate ($CH_3 - COO - CH_2 - CH_3$); and (6) Alkyl benzenes: Xylene

($C_6H_4 - CH_3 - CH_3$). Air, Ethanol, Methanol and DMSO are used as calibration materials because they have average permittivities of 1, 5, 10 and 30 in the frequency range of 7-9 GHz to be able to characterize unknown organic chemicals with ϵ_r' range of 1-30. Permittivities of these calibration materials are assumed to be known using reported dispersive equations and parameters (2.2) [6, 7, 8]. The frequency shifts achieved due to deposition of calibration materials are measured and detected ($\Delta f = f_{o,air} - f_{o,mat} = N \cdot (f_{ref,air} - f_{ref,mat})$). The theoretical reported permittivities of calibration materials along with frequency shifts detected upon their deposition are used to find the absolute value of the frequency shift versus permittivity ($|\Delta f|$ vs ϵ_r') characteristic curves. Then, other unknown organic chemicals are deposited. Frequency shifts achieved for these chemicals are mapped into ϵ_r' values using the $|\Delta f|$ vs ϵ_r' characteristics. This procedure is explained in detail as follows:

1) Sensor Characterization: $|\Delta f|$ vs ϵ_r' characteristics using calibration materials:

The detection procedure shown in Fig. 2.2 is first performed for calibration materials and the frequency shifts are found for the volume range of 0.2-20 μL in the frequency range of 7-9 GHz with a frequency step of 0.1 GHz. The measured absolute frequency shifts, $|\Delta f(f_s, S_v)|$, with respect to reported permittivities for calibration materials are used to have a full $|\Delta f|$ vs ϵ_r' characteristics for each volume and sensing frequency using curve fitting. Parabolic functions, or second order polynomials, are suitable curves for this purpose because the variations in $|\Delta f|$ decreases for larger amount of permittivities (Fig. 2.7). Therefore, $|\Delta f|$ vs ϵ_r' curve is represented as

$$|\Delta f(f_s, S_v)| = a(f_s, S_v) \cdot \epsilon_r'^2(f_s, S_v) + b(f_s, S_v) \cdot \epsilon_r'(f_s, S_v) + c(f_s, S_v) \quad (2.3)$$

where a, b and c are the polynomial fitting parameters and are functions of sensing frequency (f_s) and liquid volume (S_v). Fig. 2.22 shows the fitted $|\Delta f|$ vs ϵ_r' characteristics at volumes ranging from 0.2 μL to 20 μL at the sensing frequency of 8 GHz as an example. Similar graphs are generated for frequencies between 7 and 9 GHz with a frequency step of 0.1 GHz. Fig. 2.23 shows the standard deviation of the frequency shift ($|\Delta f|$) over six different trials at 8 GHz. For small volumes ($S_v <$ 5 μL), the standard deviation is high due to non-sufficient field confinement around the sensor. For larger volumes ($S_v <$ 15 μL), the standard deviation is smaller ($\approx$ 2.2 MHz). Similar plots are generated for frequencies of 7-9 GHz and show similar values of standard deviation. The contour plots in Fig. 2.24(a), (b) and (c) show the dependence of the mean values of the fitting parameters, $a(f_s, S_v)$, $b(f_s, S_v)$ and $c(f_s, S_v)$ on the sensing frequency (f_s) and the volume (S_v), respectively. Fig. 2.25 shows the uncertainty values representing the maximum deviation of a, b and c from their mean values over six trials at 8 GHz. This maximum deviation is high ($> 5\%$) at smaller volumes and are around 2% at higher volumes. Similar plots are generated for frequencies of 7-9 GHz and show that this deviation is nearly independent of frequency.

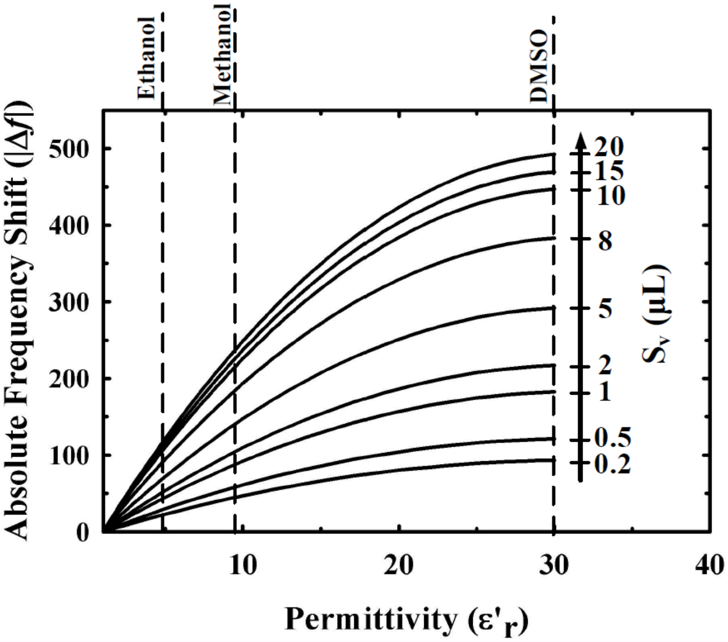


Figure 2.22: Fitted $|\Delta f|$ vs ϵ_r' characteristics at volumes ranging from 0.2 μL to 20 μL at the sensing frequency of 8 GHz.

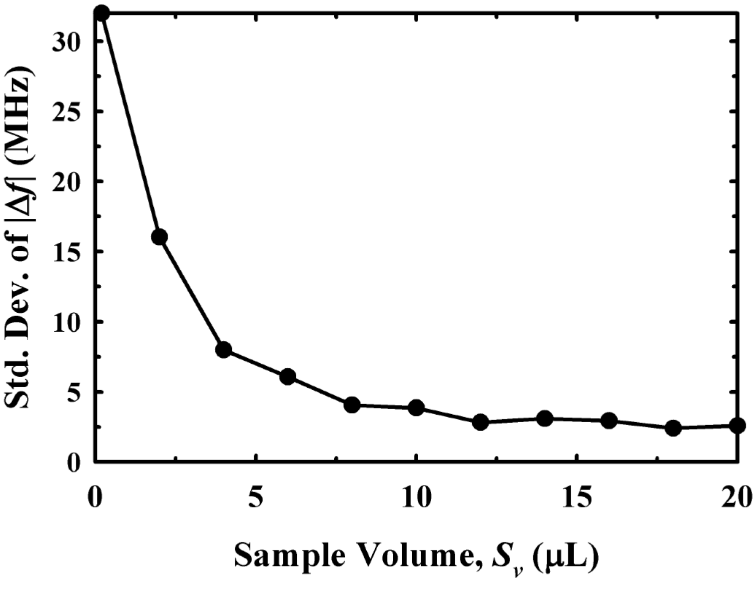
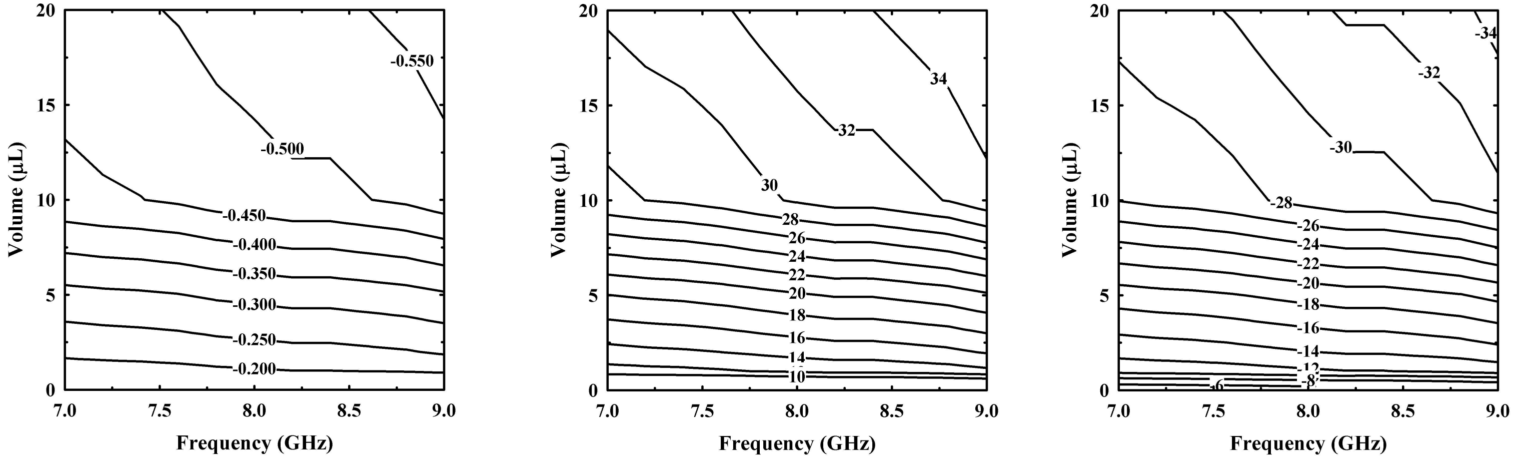


Figure 2.23: Standard deviation of the frequency shift as a function of the sample volume at the sensing frequency of 8 GHz.



(a)

(b)

(c)

Figure 2.24: Contour plots showing the variations of the fitting parameters with sensing frequency (f_s) and the liquid's volume (S_v): (a) $a(f_s, S_v)$, (b) $b(f_s, S_v)$, and (c) $c(f_s, S_v)$.

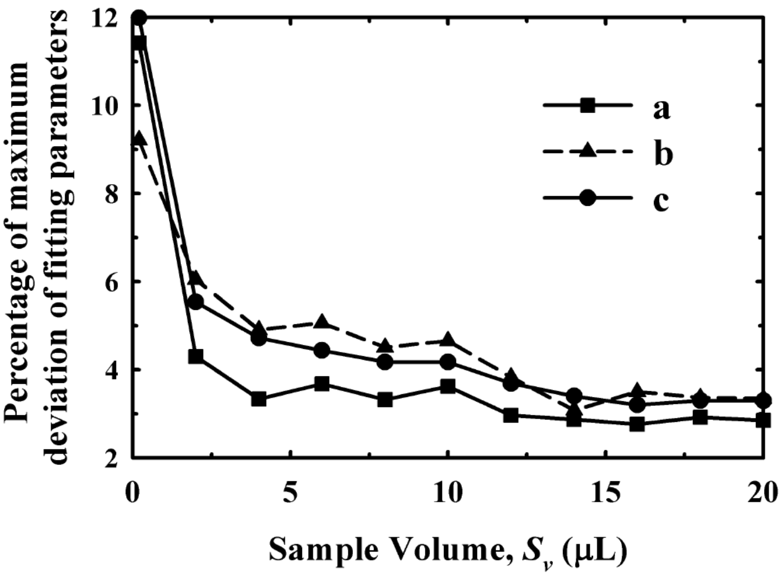


Figure 2.25: Maximum deviation of the fitting parameters (a, b and c) as a function of the sample volume at the sensing frequency of 8 GHz.

2) Dielectric characterization of organic materials under test:

The detection procedure in Fig. 2.2 is then performed for organic chemicals under test including acetone, ethylene glycol, ethyl acetate, isopropanol, 2-butyl alcohol and xylene, whose permittivities are assumed to be unknown. The frequency shifts achieved upon deposition of these chemicals are measured for different volumes (S_v) and frequencies (f_s). Using the calibration curves (Fig. 2.24) and fitting parameters (2.3), the measured frequency shifts for each chemical are mapped into frequency and volume dependent permittivities, $\epsilon_r'(f_s, S_v)$, that are given by

$$\epsilon_r'(f_s, S_v) = \frac{-b(f_s, S_v) + \sqrt{b^2(f_s, S_v) - 4 \cdot a(f_s, S_v) \cdot [c(f_s, S_v) - |\Delta f(f_s, S_v)|]}}{2 \cdot a(f_s, S_v)} \tag{2.4}$$

As an example, ethyl acetate is characterized at $f_s = 8$ GHz and $S_v = 20$ μL. The measured frequency shift $|\Delta f(8 \text{ GHz}, 20\ \mu\text{L})| = N \cdot (f_{ref,air} - f_{ref,mat})$, is found to be 220 MHz as shown before in Subsection 2.5.4. From the contour plots in Fig. 2.24, the values of a, b and c at $f_s = 8$ GHz and $S_v = 20$ μL as 0.53, -33.2 and 30, respectively. Substituting the values of $|\Delta(f)|$, a, b and c in (2.4) results in a permittivity ϵ_r'(8 GHz, 20 μL) of 5.9. Similar procedure is applied for other frequencies, volumes and chemicals and repeated six times for each case. Fig. 2.26(a), (b) and (c) show the average extracted values of ϵ_r' as a function of f_s for different values of S_v and different materials. Fig. 2.26 shows that the $\epsilon_r'(f_s, S_v)$ detection accuracy increases with increasing the volume of liquid deposited. The value of $\epsilon_r'(f_s, S_v)$ does not change for volumes larger than 10 μL at which the measurement results for the organic chemicals are very close to the theoretical values based on Cole-Cole equation [6]. This is because EM fields are well confined for these volumes and the field intensity becomes independent of S_v leading to a fixed sensing capacitance (C_s). The relative error between the detected permittivities and the theoretical models is around ±3.7%. Error bars showing the variance of the six permittivity measurements around the mean values for $S_v = 20$ μL are shown in Fig. 2.26.

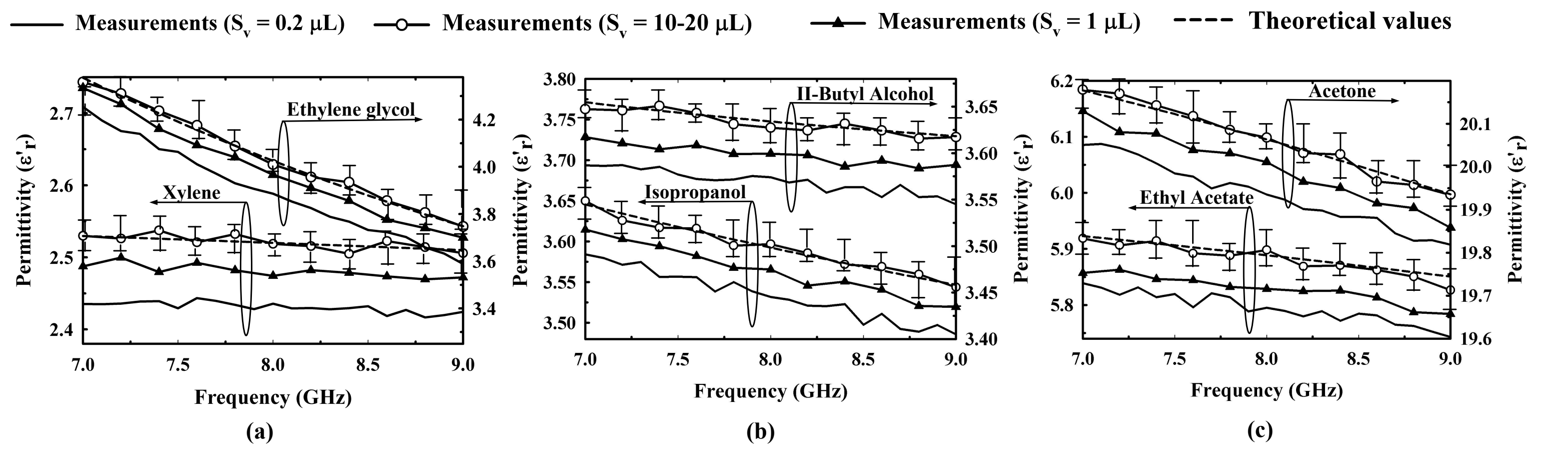


Figure 2.26: Measured permittivities versus frequency for different volumes for (a) Xylene and acetic acid, (b) Isopropanol and II-Butyl Alcohol and (c) Ethyl acetate and Acetone. The measured ϵ'_r is compared with theoretical values from (2.2).

2.5.6 Sensitivity Characterization

1) Minimum and maximum detectable frequency shifts (Δf_{min} and Δf_{max}): The voltages V_{C1} and V_{C2} on the varactors (C_1 and C_2) are tuned manually to cover the locking range (Fig. 2.13). For each value of V_{C1} and V_{C2}, the reference frequency is tuned to sweep the output frequency versus $V_{ADC,in}$. The value of $V_{ADC,in}$ corresponds to a digital code at the output of the ADC. The minimum detectable frequency shift (Δf_{min}) is the shift in the output frequency corresponding to the change of the Least Significant Bit (LSB) at the ADC output. The maximum detectable frequency shift (Δf_{max}) is the difference between the minimum and maximum output frequencies for each value of V_{C1} and V_{C2} (Fig. 2.13). Δf_{min} and Δf_{max} are shown in Fig. 2.27 versus the values of V_{C1} and V_{C2}.

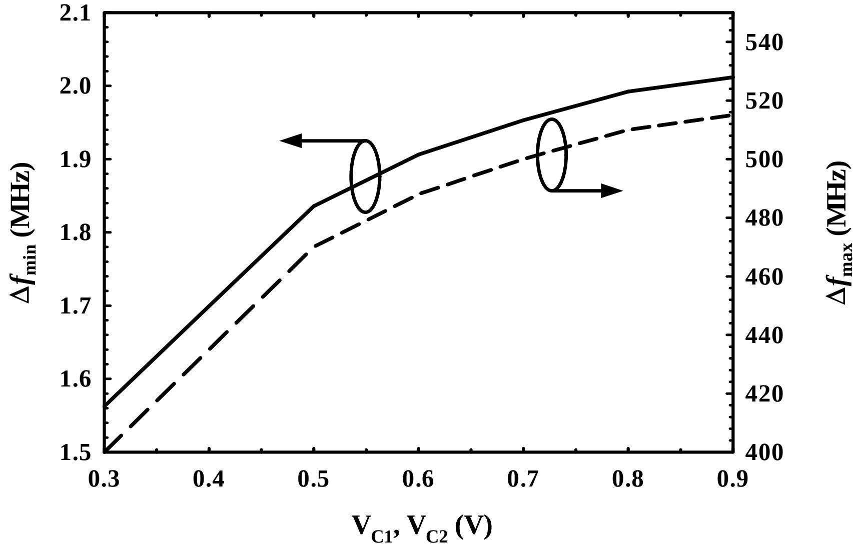


Figure 2.27: Minimum and maximum detectable frequency shifts versus V_{C1} and V_{C2}.

From Fig. 2.27, Δf_{min} is below 2 MHz for all values of V_{C1} and V_{C2}. Also, the ratio of Δf_{min} to Δf_{max} is about 0.0035 which is approximately $\frac{1}{2^{\mathrm{ENOB}}}$, where ENOB is the effective number of bits at the ADC output (ENOB = 8.3). This conclusion is consistent with the fact that the sensor resolution is limited by the ADC performance. Accordingly, higher resolution ADCs, using digital filter at the ADC output or using higher resolution architectures such as Sigma-Delta ADCs, are promising for better chemical sensing resolution.

2) Resolution of the permittivity ($\Delta\epsilon_r'$): The minimum detectable frequency shift Δf_{min} (Fig. 2.27) can be mapped into a value of permittivity resolution ($\Delta\epsilon_r'$). This can be estimated from the $|\Delta f|$ vs ϵ_r' characteristic curves, such as the characteristic curves shown in Fig. 2.22 for a sensing frequency of 8 GHz. However, the dependence of Δf on the permittivity is not linear (Fig. 2.22). Therefore, the permittivity resolution is also a non-linear function of the permittivity. Due to the parabolic dependence of $|\Delta f|$ on ϵ_r' (2.3), the worst case permittivity resolution occurs at large values of permittivities (around 30). This worst case resolution can be found by estimating the change in permittivity corresponding to change of frequency shift between Δf_{max} and $\Delta f_{max} - \Delta f_{min}$, as shown in Fig. 2.28 ($f_s = 8$ GHz). From Fig. 2.28, the worst case resolution of permittivity at $f_s = 8$ GHz is about 1 at ϵ_r' close to 30. This corresponds to a relative error of 3.3 %. Similarly, the best case resolution at permittivities close to 1 is found to be 0.035 corresponding to a relative error of 3.5 %. Accordingly, the permittivity resolution is ranging from 0.035 to 1 with a detection error around 3.5 %.

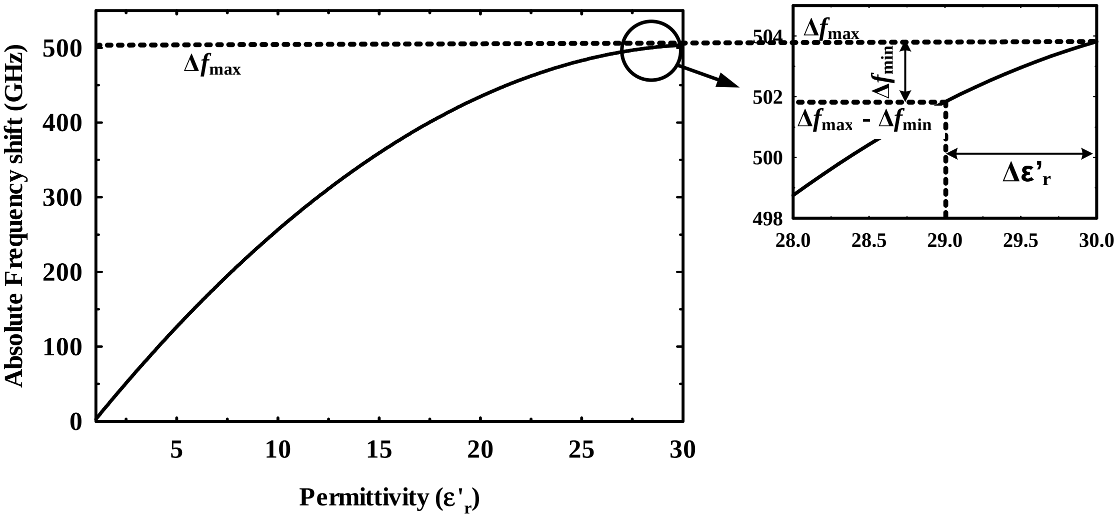


Figure 2.28: Estimation of the worst case permittivity resolution from $|\Delta f|$ vs ϵ_r' characteristic curves at a sensing frequency of 8 GHz.

Finally, Table 2.5 summarized the specifications of this sensor and compares it to reported discrete and integrated capacitive chemical/biochemical sensors. This comparison shows that this is the first work done as a microwave self-sustained CMOS chemical sensor in the range of 7-9 GHz with reasonable detection accuracy.

Table 2.5: Comparison of the proposed CMOS sensor with reported integrated and discrete sensors.

	Target	Sensing Frequency	Integration /Technology	Area	Power Consumption	Sensitivity/Accuracy
[47]	Chemicals Permittivity detection	500 - 800 MHz	NO	NA	NA	Permittivity Error $\approx$ 3 % [a]
[1]	Chemicals Permittivity detection	1, 2 and 3 GHz	NO	$>$ 112 $\times$ 2.4 mm^2	0 [b]	0.7 % $<$ Permittivity Error $<$ 12 % [a]
[24]	Chemicals Permittivity detection	8 GHz	NO	4000 $\times$ 1500 cm^2	0 [b]	Permittivity Error $\approx$ 0.3 %
[37] [c]	Capacitive sensing	1 Hz - 1 GHz	0.18 μm CMOS	3.9 $\times$ 3.83 mm^2	NA	Capacitance resolution $\approx$ 13 aF in 64 steps
[29]	Capacitance measurements for DNA detection	DC	0.5 μm CMOS	6.4 $\times$ 4.5 mm^2	NA	NA
[31]	Chemicals Permittivity detection	DC	0.18 μm CMOS	NA	NA	Permittivity Error $<$ 6 % [a]
[33]	Impedance Spectroscopy and DNA detection	10 Hz - 50 MHz	0.35 μm CMOS	2 $\times$ 2 mm^2	84.8 mW	Admittance resolution $\approx 10^{-8}$ S
[57]	Bioparticles localization	DC	0.35 μm CMOS	6.4 $\times$ 6.4 mm^2	NA	Capacitance resolution $\approx$ 0.42 fF
[30]	Humidity detection	DC	0.6 μm CMOS	4.8 mm^2	1.19 mW	Relative humidity $\approx$ 0.073 %
This work	Chemicals Permittivity detection	7 - 9 GHz	90 nm CMOS	2.5 $\times$ 2.5 mm^2	16.5 mW	Permittivity Error $<$ 3.5 %

[a] Errors are estimated and extracted from reported measurements.

[b] Only passive circuits are fabricated. The shift in S-parameters for permittivity detection is measured using network analyzers. accordingly, these sensor are not self-sustained.

[c] No material characterization is performed. Sensing elements require CMOS post-processing.

2.6 Application to Permittivity Detection: Mixture Characterization

As mentioned before, sensing dielectric properties of chemicals is used to measure the permittivity of materials subject to characterization. However, it can also be used to detect the mixing ratios in a certain mixture or composite. Dielectric mixing rules are formulas to compute the effective permittivity of a mixture as a function of permittivities of the mixing elements, the fractional volumes and parameters characterizing the microstructure of the mixture [56]. For binary mixtures, two components are composing the mixture: (i) the environment (host) and (ii) the inclusion (guest), with mixing ratios of (1-q) and q, respectively ($0 \leq q \leq 1$). Assuming isotropic mixtures and spherical inclusions of the guest inside the host, many formulas exist for mixture theory [56]: (i) *Maxwell Garnett* formula, (ii) *Polder-van Santen* formula, and (iii) *Coherent Potential* formula. These mixing formulas are collected in one *Unified Mixing Approach* [58] with a dimensionless parameter υ as follow

$$\frac{\epsilon_{eff} - \epsilon_e}{\epsilon_{eff} + 2\epsilon_e + \upsilon(\epsilon_{eff} - \epsilon_e)} = q \cdot \frac{\epsilon_i - \epsilon_e}{\epsilon_i + 2\epsilon_e + \upsilon(\epsilon_{eff} - \epsilon_e)} \tag{2.5}$$

where ϵ_e and ϵ_i are the complex permittivities of the environment and inclusions, respectively, q is the volume fraction of the inclusions in the mixtures, ϵ_{eff} is the effective complex permittivity of the mixture and υ = 0, 2 and 3 corresponding to Maxwell Garnett, Polder-van Santen and Coherent Potential rules, respectively.

The fabricated frequency synthesizer-based chemical sensor is used for mixture characterization. Two organic chemicals are mixed together with different volume fractions (q and $(1 - q)$) and the same permittivity detection procedure discussed in Sec. V is applied to extract the permittivity of mixtures with different mixing ratios using same calibration materials and $|\Delta f|$ vs ϵ'_r characteristics. Mixture characterization is performed for two binary mixtures: (i) Ethanol-Methanol mixtures and (ii) Xylene-Ethanol mixture. As an example, Ethanol-Methanol binary mixture is subject to characterization with fractional volumes of $q = 0.4$ and $(1 - q) = 0.6$ for ethanol (inclusion) and methanol (environment), respectively, with a total volume of 20 μL and a sensing frequency of 8 GHz ($a = 0.53$, $b =$ -33.2 and $c = 30$). Using the micropipette, 8 μL of ethanol and 12 μL of methanol are mixed together and inserted inside the tube on top of the sensor. The detection procedure in Fig. 2.2 is applied and the frequency shift is detected to find the permittivity using (2.4). Similar procedure can be repeated for all values of q between 0 and 1 with a step of 0.01. Fig. 2.29 shows the detected ϵ'_r values versus q for the Ethanol-Methanol mixture at $S_v = 20$ μL and $f_s = 8$ GHz along with the the theoretical values (2.5: $\upsilon = 0$, 2 and 3). Zoomed pictures of the measured and theoretical permittivities in the ranges of $0 \leq q \leq 0.05$, $0.3 \leq q \leq 0.7$ and $0.95 \leq q \leq 1$ are also provided. Fig. 2.29 shows detected permittivities very close to theoretical values proving the ability of the sensor to characterize mixtures with 1-2 % accuracy in the fractional volume (q). Also, mixture characterization is performed for Xylene (inclusion) and Ethanol (environment) mixture and measured and theoretical values are provided in Fig. 2.30.

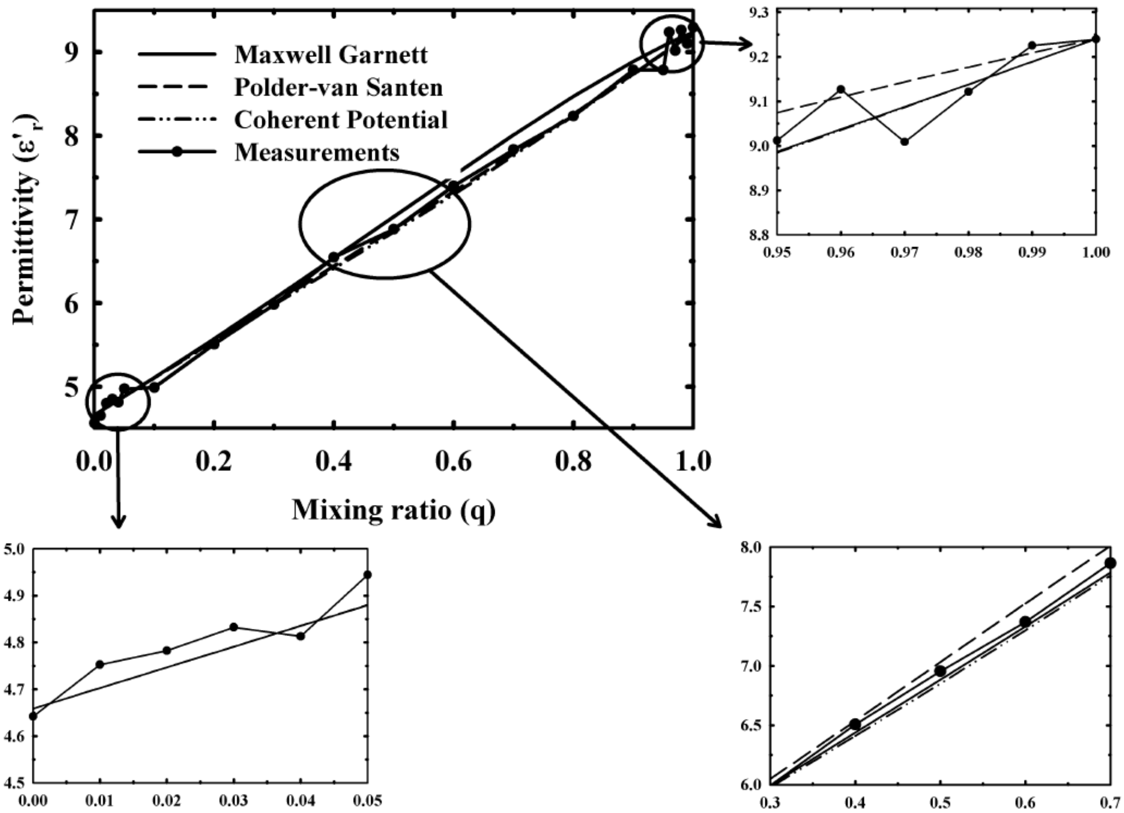


Figure 2.29: The measured and theoretical permittivities versus the mixing ratio, q, for the Ethanol-Methanol binary mixture at $S_v = 20$ μL and $f_s = 8$ GHz with zoomed views at $0 \leq q \leq 0.05$, $0.3 \leq q \leq 0.7$ and $0.95 \leq q \leq 1$.

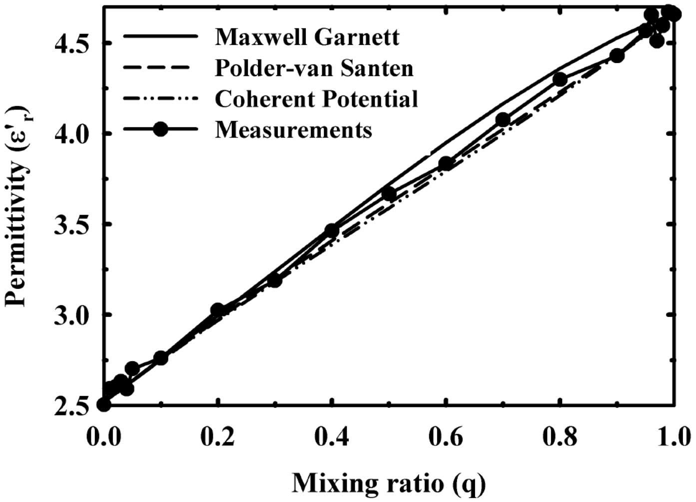


Figure 2.30: The measured and theoretical permittivities versus the mixing ratio, q, for the xylene-ethanol binary mixture at $S_v = 20\ \mu\text{L}$ and $f_s = 8$ GHz.

2.7 Summary

A self-sustained on-chip chemical sensor for permittivity detection of organic chemical liquids on 90 nm CMOS technology is developed. The design of the integrated sensing element, VCO and self-sustained frequency synthesizer system has been presented in detail. The proposed system is able to measure the permittivity of organic chemicals under test in the frequency range of 7-9 GHz. Sensitivity characterization is performed proving a detection error less than 3.7 % and limited by the ADC resolution. The system is also used to detect the permittivities of binary mixtures with fractional volume accuracy of 1-2%.

3. A 1-8 GHZ MINIATURIZED ON-BOARD DIELECTRC SPECTROSCOPY SYSTEM FOR PERMITTIVITY DETECTION OF ORGANIC CHEMICALS

3.1 Introduction

Broadband microwave dielectric spectroscopy is necessary for accurate detection and characterization of chemicals and biochemicals at the sensing frequencies. It also helps in characterization at low-frequencies by means of data extrapolation of the detected microwave permittivities. One main challenge in dielectric spectroscopy system is the self-sustainability which aims to perform the complete sensing operation in a stand-alone fashion using elements integrated on-board without the need of any external equipment. Self-sustained systems are necessary for portable sensors targeting many applications, including biological and medical sensors, such as portable and body implanted blood sugar control devices. As mentioned in Section 1, reported time domain [26, 27, 28] and frequency domain [21, 22, 23, 1, 24, 25] spectroscopy systems are not self-sustained because they need external equipments for signal generation and measurement, such as VNAs, TDRs and scopes.

In this section, a novel low-cost, compact size, broadband dielectric spectroscopy system for the frequency range of 1-8 GHz is presented [42, 43]. The sensor employs a sensing capacitor as a part of a broadband true-time-delay (TTD) cell. The sensing capacitor is exposed to the MUT, and as a result the capacitance and the phase of the signal passing through the TTD cell change as a function of the permittivity of the MUT. This phase shift is measured using on-board phase detectors working based on the principle of correlation. Compared to reported broadband frequency

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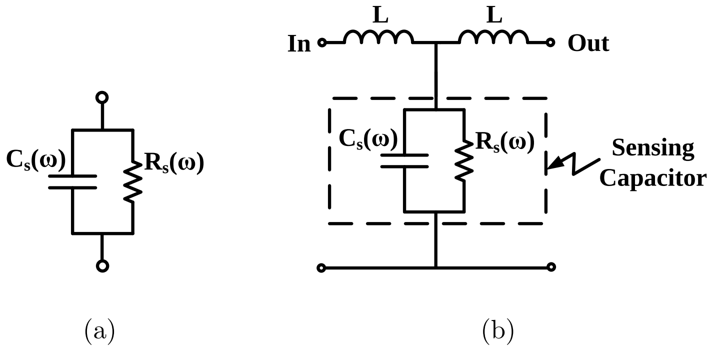
domain dielectric spectroscopy techniques [21, 22, 23, 1, 24, 25], the proposed technique employs simple lumped passive elements operating as TTD elements that can be easily miniaturized and reconfigured for a wide frequency range operation with high accuracy. The implementation of the proposed sensor is considered as the first step toward a self-sustained miniaturized dielectric spectroscopy system since no external VNA, TDR or scope are used for detection purpose. However, as a proof of concept, the microwave signal applied to the TTD cells is generated using an external microwave signal generator, which can be replaced by on-board miniaturized discrete frequency synthesizers for a fully self-sustained system. In this work, the real part of the permittivity (ϵ_r') of the MUT is detected. Since materials have different frequency dispersion characteristics over a broad frequency range [6], the detection of ϵ_r' over wide range of frequencies (1-8 GHz) is enough to distinguish among MUTs without extraction of their loss properties.

In this section, Subsection 3.2 discusses the sensing cell analysis, design and simulations. It also discusses design considerations of cascaded sensing units including electromagnetic coupling between adjacent TTD cells, design methodology of cascaded cells and fabricated prototype characterization. The system implementation is presented in Subsection 3.3. Circuit implementation and test setup for chemicals are described in Subsection 3.4. Subsection 3.5 shows the detailed experimental procedures and results for sensor calibration and dielectric spectroscopy of organic chemicals in the frequency range of 1-8 GHz for different sample volumes. Subsection 3.6 presents applications to dielectric characterization and spectroscopy including the estimation of the static permittivity using extrapolation and the mixture characterization. Finally, Subsection 3.7 summarizes and concludes the proposed work.

3.2 Basic Idea and Sensing Cell Design

3.2.1 Sensing Cell Design

The relative permittivity of any material is a frequency dependent complex quantity given by $\epsilon_r(\omega) = \epsilon_r'(\omega) - j\epsilon_r''(\omega)$ [6]. Accordingly, a capacitor exposed to a material under test and excited by a signal at a certain frequency can be used to detect the complex permittivity of this material at the excitation frequency. A sensing capacitor can be modeled as a capacitance in parallel with a resistor. When exposed to air ($\epsilon_r' = 1$ and $\epsilon_r'' = 0$), the sensing element is ideally modeled as a capacitance of C_{s0} with an infinite parallel resistance. When exposed to material under test ($\epsilon_r(\omega) = \epsilon_r'(\omega) - j\epsilon_r''(\omega)$), the capacitor's model changes to a capacitance of $C_s(\omega)$ in parallel with a resistance of $R_s(\omega)$ as shown in Fig. 3.1(a). The value of the capacitance changes proportional to the real part of the permittivity independent of the material's loss. The increase of material's loss, or the imaginary part of the permittivity, results in lower resistance in parallel, thus degrading the quality factor of the sensing capacitor.



(a) (b)

Figure 3.1: (a) Electrical model of the sensing capacitor when exposed to MUT, and (b) sensing capacitor embedded inside the TTD cell.

In order to detect the change in the sensing capacitance ($C_s(\omega)$) for a wide frequency range, the capacitor is embedded inside a TTD cell as shown in Fig. 3.1(b). The TTD cell is a low-pass LC T-network that can provide a phase shift up to 90° [59]. The change of the capacitance (C_s) is translated into a change in the phase shift of the microwave signal passing through the TTD cell which is used to estimate ϵ_r' of the MUT as will be explained later. The TTD cell elements should be designed for broadband input/output matching for wideband spectroscopy purpose. The TTD cell is firstly assumed to be a T-network composed of two inductors (L) and a high quality factor sensing capacitance (C_s) with an infinite sensing resistance ($R_s(\omega) = \infty$). The two-port S-parameters of this network with respect to a characteristic impedance of Z_0 are proved to be given by [59]

$$S_{11} = \frac{j\frac{\omega}{Z_0}(2L - C_s Z_0^2 - \omega^2 L^2 C_s)}{D(j\omega)} \tag{3.1}$$

$$S_{12} = \frac{2}{D(j\omega)} \tag{3.2}$$

$$S_{21} = \frac{2}{D(j\omega)} \tag{3.3}$$

$$S_{22} = \frac{-j\frac{\omega}{Z_0}(2L - C_s Z_0^2 - \omega^2 L^2 C_s)}{D(j\omega)} \tag{3.4}$$

where

$$D(j\omega) = (2 - \omega^2 L C_s) + j\frac{\omega}{Z_0}(2L + C_s Z_0^2 + \omega^2 L^2 C_s) \tag{3.5}$$

Using (3.1) and (3.4), the condition for perfect input/output matching ($|S_{11}| = |S_{22}| = 0$) is given by;

$$Z_0^2 = \frac{2L}{C_s} \cdot (1 - \frac{\omega^2 L C_s}{2}) \tag{3.6}$$

Accordingly, for perfect broadband matching condition in (3.6) is frequency independent for

$$\omega^2 L C_s << 2 \tag{3.7}$$

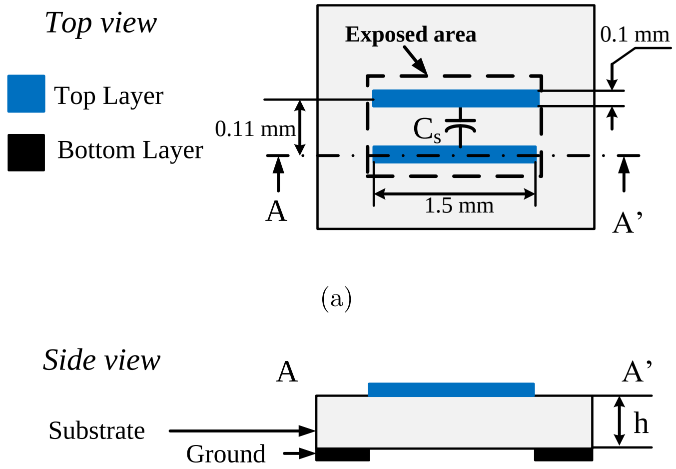
where $Z_0 = \sqrt{\frac{2L}{C_s}}$. However, for broadband matching better than 10 dB, and using (3.1), (3.4) and (3.7), the matching condition is given by;

$$|\frac{\omega}{Z_0} \cdot (2L - C_s Z_0^2)| < \frac{2}{3} \tag{3.8}$$

The frequency dependent phase shift of the signal passing through the TTD cell is the phase of S_{21} ($\phi(\omega)$). Using (3.3) and considering the broadband matching condition in (3.7), the phase shift of the TTD cell is given by

$$\phi(\omega) \approx \sin^{-1}(\omega C_s Z_0) \approx \sin^{-1}(\omega \sqrt{2LC_s}) \tag{3.9}$$

Accordingly, the change of the capacitance (C_s) upon exposure to the MUT is translated into a change of the phase shift of the microwave signal passing through the TTD cell if the matching condition is satisfied.



(a)

(b)

Figure 3.2: Layout of the sensing capacitor on Rogers Duroid 5880: (a) Top view, and (b) cross-sectional view.

Fig. 3.2 shows the implementation of the sensing capacitor on Rogers Duroid 5880 substrate ($\epsilon_r' = 2.2$, $\tan\delta = \frac{\epsilon_r''}{\epsilon_r'} = 0.001$ and $h = 0.787$ mm). The sensing capacitor is implemented using a pair of metal lines on the top metal layer with the ground plane removed under the sensing capacitor to reduce the parasitic capacitance as shown in Fig. 3.2. The sensing capacitor is simulated using Sonnet. The values of the capacitance (C_s) and quality factor ($Q_s = \omega C_s R_s$) of the sensing capacitor versus ϵ_r' and $\tan\delta$ are shown in Fig. 3.3(a) and (b), respectively, for different frequencies. In this simulation, the permittivities are assumed frequency independent for simplicity. Fig. 3.3(a) shows that the capacitance increases with ϵ_r' from 40 fF to around 300 fF for permittivities ranging from 1 to 30 at different frequencies (1, 4 and 8 GHz). The simulation was performed for different values of $\tan\delta$ and the value of the sensing capacitance was proved to be independent of material's loss at all frequencies.

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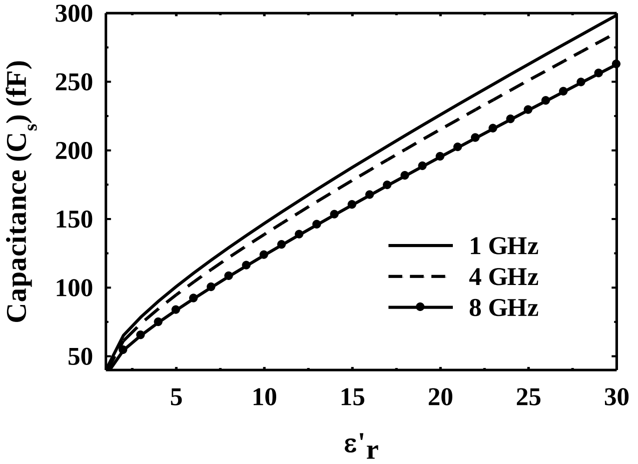
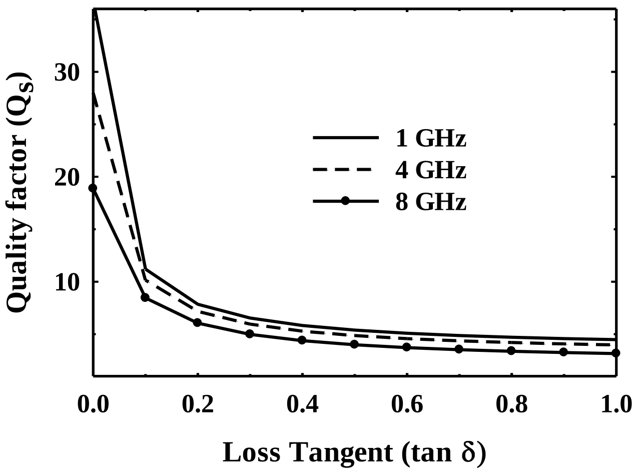
Fig. 3.3(b) shows that the quality factor of the sensing capacitor decreases with the increase of the material's loss.



(a)



(b)

Figure 3.3: Electromagnetic simulations of the sensing capacitor at 1, 4 and 8 GHz: (a) Sensing capacitance (C_s) versus ϵ_r', and (b) quality factor (Q_s) of the sensing capacitor versus $\tan\delta$.

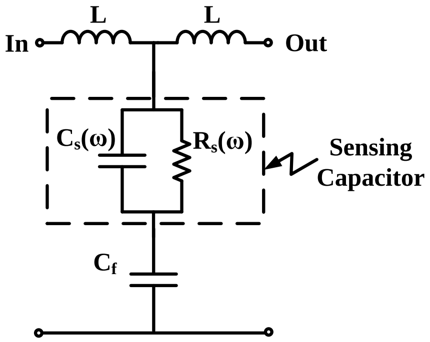
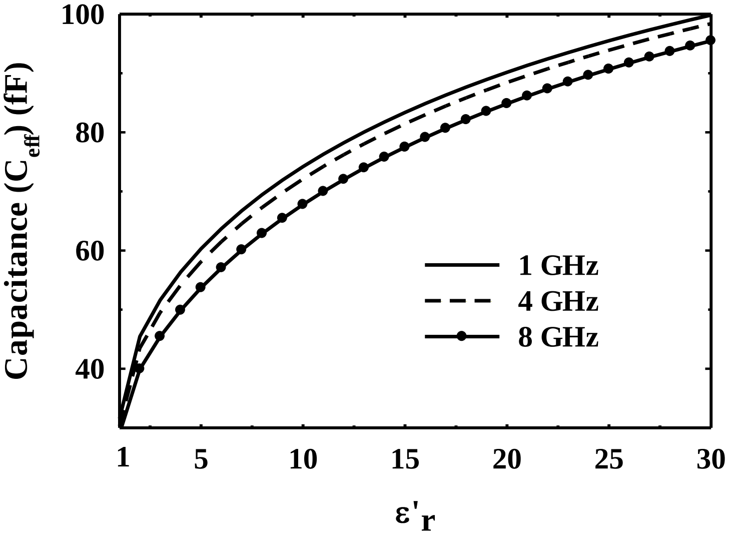
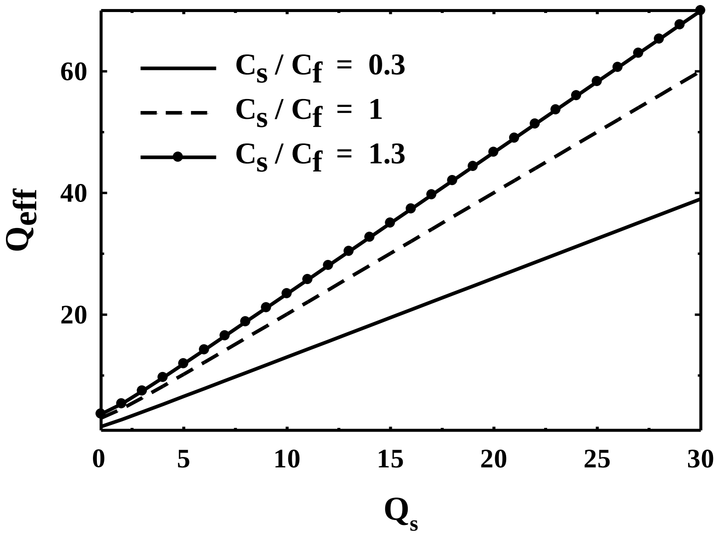


Figure 3.4: Schematic of the TTD cell with fixed capacitor (C_f) in series with the sensing capacitor.

From Fig. 3.3(a), the wide variation of the sensing capacitance (C_s) can be noticed. This is to cover a wide range of ϵ_r'. Based on (3.1), large values of C_s, corresponding to larger values of $|S_{11}|$, may affect the input/output impedance matching. This results in reflections in the TTD cell leading to phase shift errors and then degrading the detection accuracy. One way to compensate for the effect of increasing C_s on the value of $|S_{11}|$ is to increase the value of L without compromising the sensitivity of the sensing capacitor to MUTs. However, based on (3.1) and (3.7), increasing both L and C_s decreases the upper limit of frequency at which matching condition is satisfied. One other way is to use a smaller sensing capacitor to limit the variations of the capacitance and prevent mismatch. However, smaller sensing capacitors results in harder manipulation of the tubes containing the liquids under characterization on top of the sensing for elements, as will be shown later. Accordingly, to prevent mismatches, a fixed capacitor (C_f) is added in series with C_s, as shown in Fig. 3.4, to suppress the wide variations of C_s at the cost of the sensitivity reduction without decreasing the sensing capacitor. For a fixed capacitance of $C_f =$ 150 fF, the values of combined series capacitance of C_s and C_f (C_{eff}) versus ϵ_r' are shown in Fig. 3.5(a) and are limited to values between 30 fF and 100 fF.



(a)



(b)

Figure 3.5: Effect of adding a fixed capacitor in series with the sensing capacitor: (a) The effective capacitance versus ϵ_r' at 1,4 and 8 GHz, and (b) the effective quality factor (Q_{eff}) versus Q_s for values of $\frac{C_s}{C_f} = 0.3$, 1 and 1.3.

The sensitivity of the capacitance to the permittivity of MUTs is defined as the ratio between the change of capacitance and the change of the permittivity $(C_{\max} - C_{\min})/(\epsilon'_{r,\max} - \epsilon'_{r,\min})$. The addition of the series fixed capacitor C_f degrades the sensitivity from 8.6 fF to 2.4 fF, but with the advantage of keeping broadband input matching. The degradation of the sensitivity is compensated by cascading multiple TTD cells as will be shown later.

Assuming that the fixed capacitor (C_f) has a very high quality factor ($Q_f >> Q_s$), then the overall quality factor (Q_{eff}) of the series combination of the sensing and fixed capacitors is proved to be given by

$$Q_{\text{eff}} = Q_s + \frac{1 + Q_s^2}{Q_s} \cdot \frac{C_s}{C_f} \tag{3.10}$$

Fig. 3.5(b) shows the values of Q_{eff} versus Q_s for different values of $\frac{C_s}{C_f}$. The effective quality factor (Q_{eff}) of the series combination of C_s and C_f is always higher than Q_s. Therefore, the addition of a series fixed capacitor reduces the wide variations of the sensing capacitance for broadband matching (Fig. 3.5(a)), but desensitize the loss effect of the sensing capacitor. Accordingly, the performance of the TTD cell is expected to be independent of ϵ''_r as will be shown later.

For wideband impedance matching better than 10 dB up to 8 GHz frequency range, conditions in (3.7) and (3.8) should be satisfied. Accordingly, the values of TTD cell elements are chosen to be: $L = 0.09$ nH, 40 fF $< C_s <$ 300 fF and $C_f =$ 150 fF satisfying the condition for input matching better than 10 dB in (3.8) and the wideband input matching condition in (3.7).

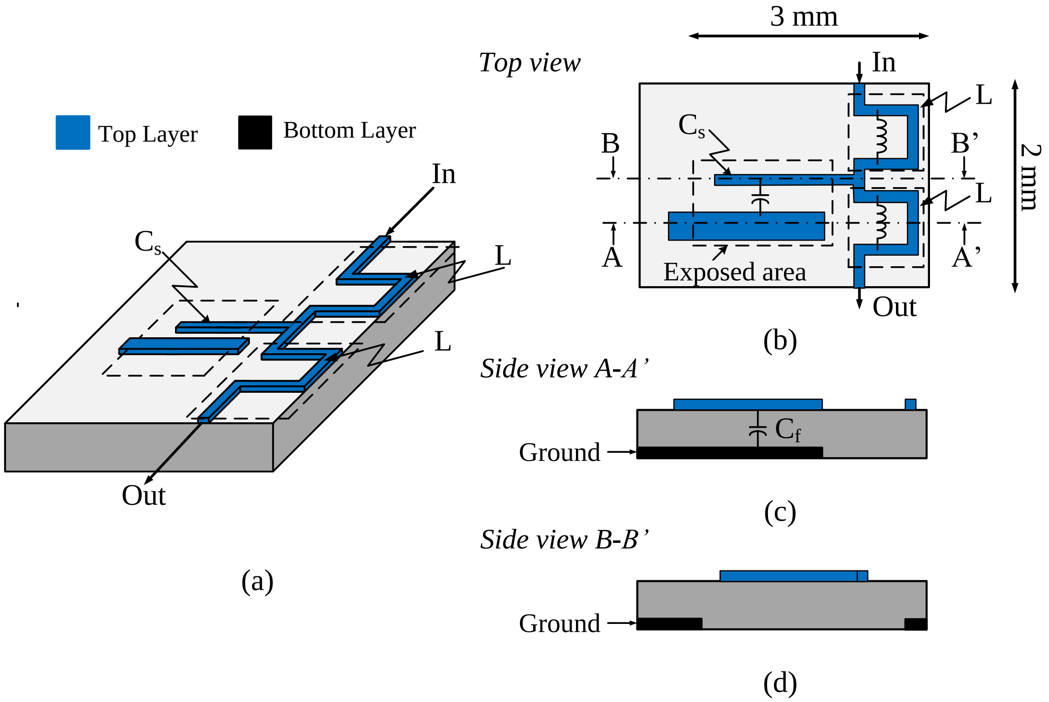
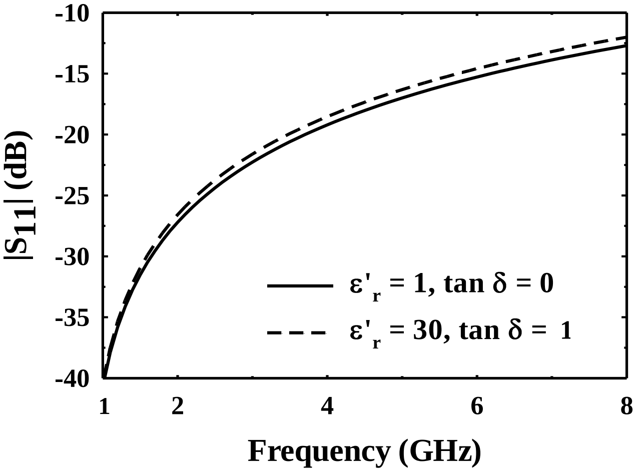
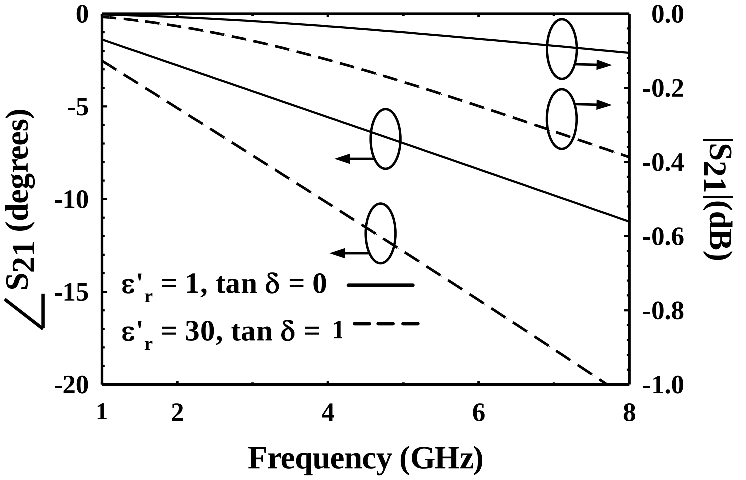


Figure 3.6: Layout of the basic TTD cell on Rogers Duroid 5880 substrate with a total area of 2×3 mm^2: (a) 3-D view, (b) top view, (c) A-A' cross-sectional side view, and (d) B-B' cross-sectional side view. Drawing is not to scale.

The TTD cell is implemented on Rogers substrate as shown in Fig. 3.6, with a total area of 2×3 mm^2. The planar inductor (L) is implemented using a meander line and the fixed capacitor (C_f) is implemented as a vertical parallel-plate capacitor between the top and bottom layers of the substrate. The capacitance of the sensing capacitor can be evaluated using the partial capacitance technique along with conformal mapping techniques evaluating the total capacitance between two sets of fingers in multi-layered structures [60, 61]. The inductance of meander line inductors (L) is based on the segmentation of the meander line into several straight lines. The overall inductance of the meander line is the resultant of the self-inductance effects of each straight line along with the mutual inductance effect between lines as reported in [62]. The TTD cell is simulated using Sonnet with materials having permittivities within the range of 1-30 and loss tangents within the range of 0-1.



(a)



(b)

Figure 3.7: Simulations of the TTD cell when exposed to materials with permittivity range of 1-30 and loss tangent range of 0-1: (a) $|S_{11}|$ in dB, and (b) $\angle S_{21}$ and $|S_{21}|$ in dB.

Fig. 3.7(a) shows that the return loss is better than 12 dB over the 1-8 GHz frequency range for two different materials ($\epsilon_r' = 1$, $\tan\delta = 0$; and $\epsilon_r' = 30$, $\tan\delta = 1$). Fig. 3.7(b) shows the magnitude and phase of S_{21} of the TTD cell. The phase of S_{21} reflects the amount of phase shift generated by the TTD cell. The phase shift increases with both frequency and ϵ_r'. For the same value of ϵ_r', the simulation is performed for different values of $\tan\delta$ ($0 < \tan\delta < 1$) and proved no phase shift dependency on the material's loss. Fig. 3.7(b) on the right axis shows the insertion loss is less than 0.07 and 0.4 dB for materials with $\epsilon_r' = 1$, $\tan\delta = 0$; and $\epsilon_r' = 30$, $\tan\delta = 1$; respectively, for the 1-8 GHz frequency range. Accordingly, the TTD cell can detect ϵ_r' independent of material's loss.

3.2.2 Cascaded TTD Cells

As shown in Fig. 3.7, the phase shift of the microwave signal passing through the TTD cell increases with the sensing frequency and permittivity (ϵ_r'). For example, at 1 GHz, the phase shift changes from 1.5° to 3.3°, whereas, at 8 GHz, the phase shift changes from 11° to 22° when ϵ_r' changes from 1 to 30. The change of phase shift will be detected using a correlator whose output is the cosine of the phase shift as will be explained later. Accordingly, the low values of phase shift, especially at lower frequencies, results in poor detection accuracy. Therefore, the phase shift generated by a single broadband TTD cell is not enough for accurate detection for a wide frequency range. To improve the detection accuracy, the overall phase shift may be increased by cascading multiple TTD cells. Assuming broadband input/output impedance matching for each TTD cell, the phase shift resulting from cascading N-TTD cells ($\phi_N(\omega)$) is approximately given by the phase shift of one cell $\phi(\omega)$

multiplied by N.

$$\phi_N(\omega) = N \cdot \phi(\omega) = N \cdot \sin^{-1}(\omega\sqrt{2LC_s}) \tag{3.11}$$

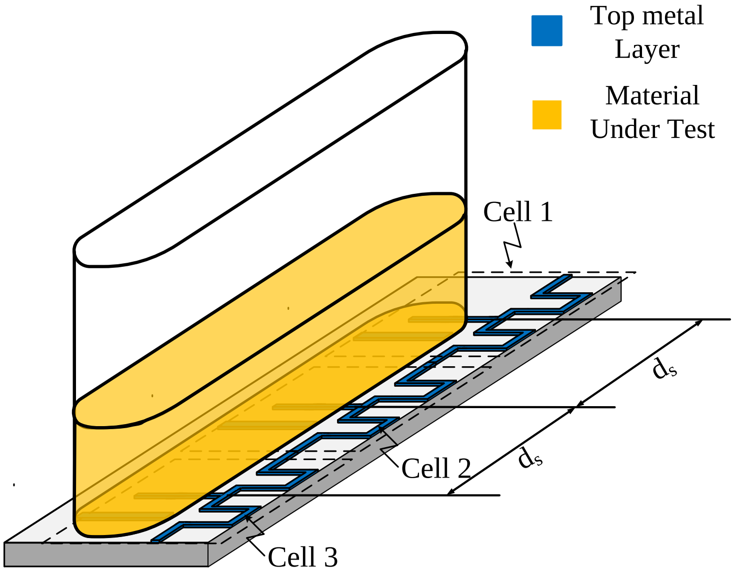
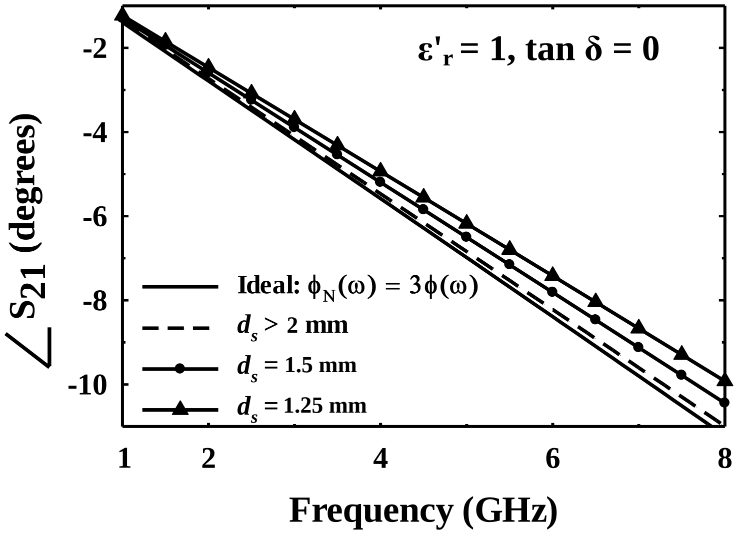


Figure 3.8: Layout of three TTD cells with a center-to-center distance of d_s and material under test on top of the sensing capacitor

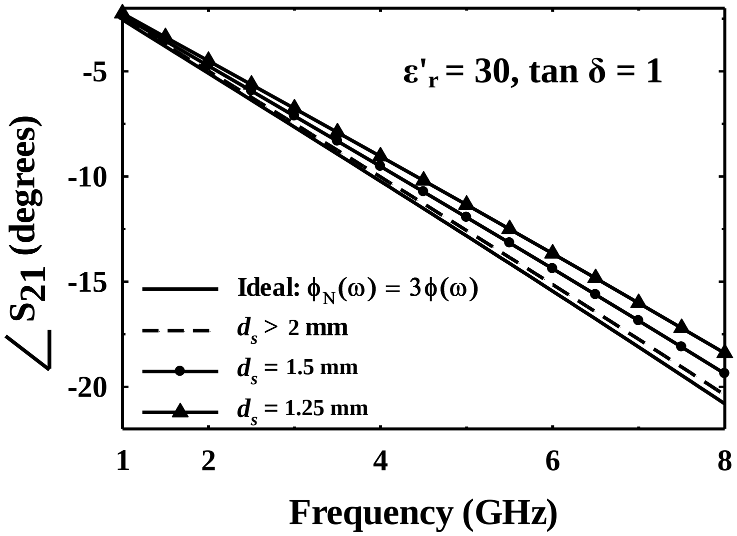
The phase shift in (3.11) is valid assuming no electromagnetic (EM) coupling between different TTD cells. However, placing the TTD cells next to each other for miniaturization and exposing them to MUTs provides EM coupling among different TTD cells through the deposited material. As a result, the phase shift in (3.11) is not an accurate measure of the real phase shift. For simplicity, the EM coupling effect on one arbitrary cell is assumed to be only from the closest preceding and following stages and the effect of far-away cells is ignored. Fig. 3.8 shows the layout of three adjacent cascaded TTD cells with the liquid deposited on top of the sensing capacitors to study the coupling effect of cells 1 and 3 on cell 2. The length of the TTD cell, or the center-to-center distance between TTD cells, is given by d_s. Using EM simulation, the phase shift of a microwave signal passing through three TTD cells in Fig. 3.8 is simulated and swept versus frequency for different values of d_s and different materials as shown in Fig. 3.9(a) and (b).

The simulated phase shifts for different values of d_s are compared to the ideal phase shift $\phi_N(\omega) = N \cdot \phi(\omega)$, where $N = 3$. Increasing the separation between the TTD cells (d_s) is expected to decrease the electromagnetic coupling effect and therefore the simulated phase shift approaches the ideal response. Increasing d_s above 2 mm results in minor change in the phase response of the three TTD cells compared to the ideal response at the cost of an increase of the sensor's area. Therefore, a value of $d_s = 2$ mm is chosen as the center-to-center distance between TTD cells.

As mentioned before, the output of the correlator used for detection is the cosine of the phase shift of the microwave signal passing through N-TTD cascaded cells. The phase shift should be limited to values between 0 and 90° to prevent any phase ambiguity due to the cosine function. As the phase shift across one TTD cell varies with frequency (Fig. 3.7(b)), the assigned number of cascaded TTD cells should also vary with the sensing frequency to avoid ambiguity. In other words, the phase shift is measured across a larger number of TTD cells for lower frequencies.



(a)



(b)

Figure 3.9: Simulated phase response of three cascaded TTD cells for different values of d_s with the ideal response defined as $\phi_N(\omega) = N \cdot \phi(\omega)$, where $N = 3$, for two values of permittivity: (a) $\epsilon_r' = 1$, $\tan\delta = 0$; and (b) $\epsilon_r' = 30$, $\tan\delta = 1$.

Based on the phase shift values in Fig. 3.7(b), the sensing frequency range of 1-8 GHz is divided into m sub-frequency ranges and the number of cascaded TTD cells varies according to each range. The i^{th} frequency range ($1 \leq i \leq m$) covers the range between $f_{L,i}$ and $f_{H,i}$ with N_i cascaded TTD cells. In this range, the minimum phase shift is $N_i \cdot |\phi(f = f_{L,i}, \epsilon_r' = \epsilon_{r,\min}')|$ and the maximum phase shift is $N_i \cdot |\phi(f = f_{H,i}, \epsilon_r' = \epsilon_{r,\max}')|$. For a given N_i, the value of $f_{H,i}$ is selected such that $N_i \cdot |\phi(f = f_{H,i}, \epsilon_r' = \epsilon_{r,\max}')| \approx 90°$ to achieve the best accuracy without phase ambiguity. For example, for 1-8 GHz frequency range, if the maximum value of N is arbitrarily selected to be 14 ($1 \leq \epsilon_r' \leq 30$), then the first subfrequency range (i =1) is chosen such that $f_{L,1} = 1$ GHz (minimum frequency) and $|\phi(f = f_{H,1}, \epsilon_r' = 30)| = \frac{90}{N_i}$ which occurs at $f_{H,1} = 2.4$ GHz as shown in Fig. 3.7(b). Higher subfrequency ranges (i >1) are chosen such that $f_{L,i} = f_{H,\text{i-1}}$ and $|\phi(f = f_{H,i}, \epsilon_r' = 30)| = \frac{90}{N_i}$. Similar procedure is repeated to cover the entire range from 1 to 8 GHz.

Assuming that N_i arbitrarily drops by 2 from one subfrequency to another for $N_{\max} = 14$ and 1 GHz $\leq f \leq$ 8 GHz, the frequency range is divided into 6 bands as shown in Fig. 3.10. For proof of concept, simple prototypes are fabricated using Rogers Duroid 5880 substrate with the TTD cell described above. Each prototype is composed of N-TTD cells in cascade with N = 4, 6, 8, 10, 12 and 14, and center-to-center separation of 2 mm. Fig. 3.11 shows the photograph of one of the prototypes with N = 14. Fig. 3.12(a) shows an input matching better than 10 dB for the 14 TTD cells in cascade when exposed to air ($\epsilon_r' = 1$ and $\tan\delta = 0$ for all frequencies) and methanol whose permittivity is frequency dependent and follows the cole-cole model given in [6].

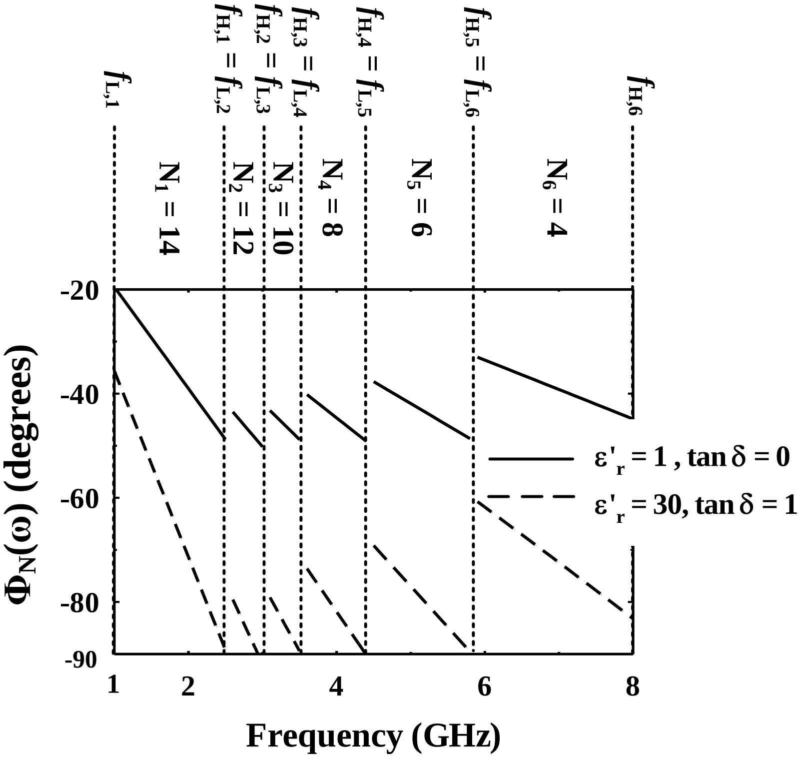


Figure 3.10: Simulated phase response versus frequency for different subfrequency ranges ($4 \le N \le 14$).

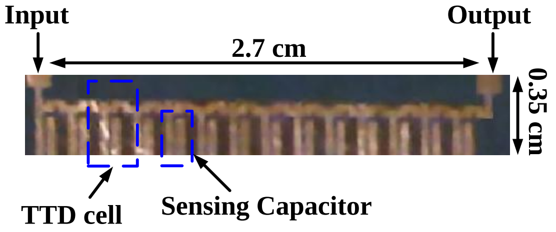
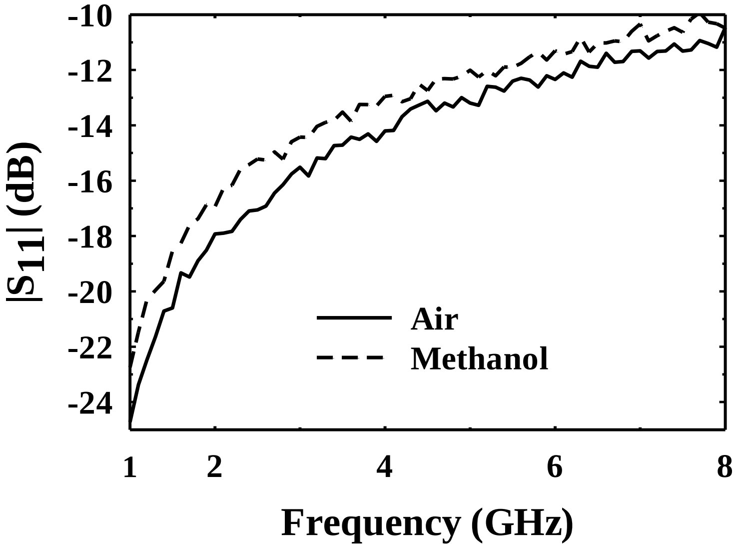
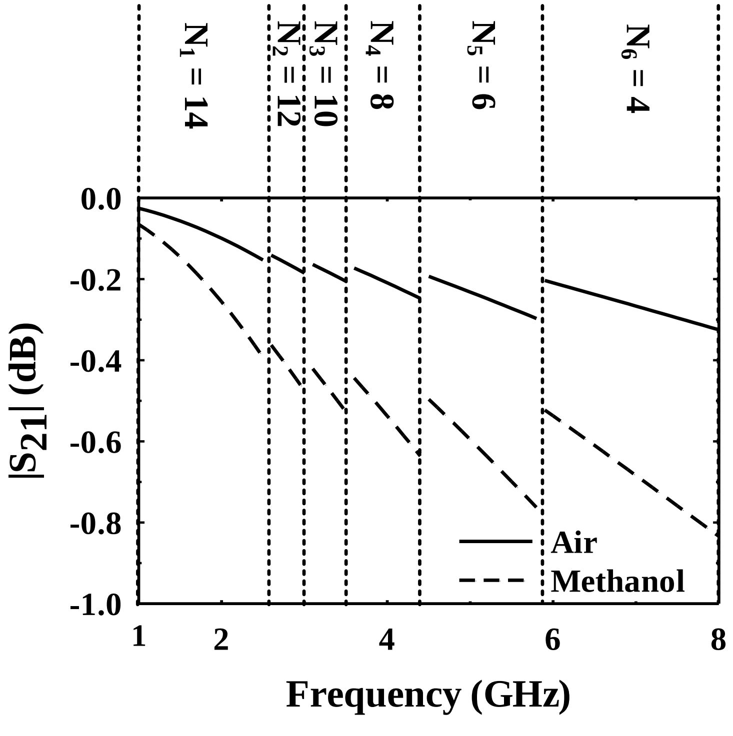


Figure 3.11: Prototype of 14 TTD cells in cascade fabricated using Rogers Duroid 5880 substrates ($\epsilon_r' = 2.2$, $\tan\delta = \frac{\epsilon_r''}{\epsilon_r'} = 0.001$ and $h = 0.787$ mm).

The insertion loss and phase shift are measured across each prototype in the corresponding subfrequency range specified in Fig. 3.10. For example, the detection in 4.3-5.9 GHz frequency range is performed using the prototype composed of 6 cascaded TTD cells. Fig. 3.12(b) shows the insertion loss for air and methanol for different values of N corresponding to different subfrequency ranges. This measurement proves insertion loss less than 0.3 and 0.8 dB, for air and methanol; respectively, for the entire frequency range which corresponds to values of loss less than 0.07 and 0.2 dB for a single TTD cell. These results mean that the effect of lossy materials, such as methanol [6], on the insertion loss of the TTD cell is minimal. Accordingly, the output of the correlator is less sensitive to loss properties and the real part of the permittivity can be detected with enough accuracy. Moreover, one way to minimize the effect of the amplitude variation due to material's loss on the output of the correlator is proposed in [63]. This circuit can be added to the system by applying the output of the TTD cell to a voltage limiter, or to a high gain amplifier to saturate the amplitude level of the signal at the input of the correlator. Accordingly, the output of the correlator is less dependent on the amplitude variation due to material's loss in case a higher detection accuracy of ϵ_r' is needed with highly loss materials.



(a)

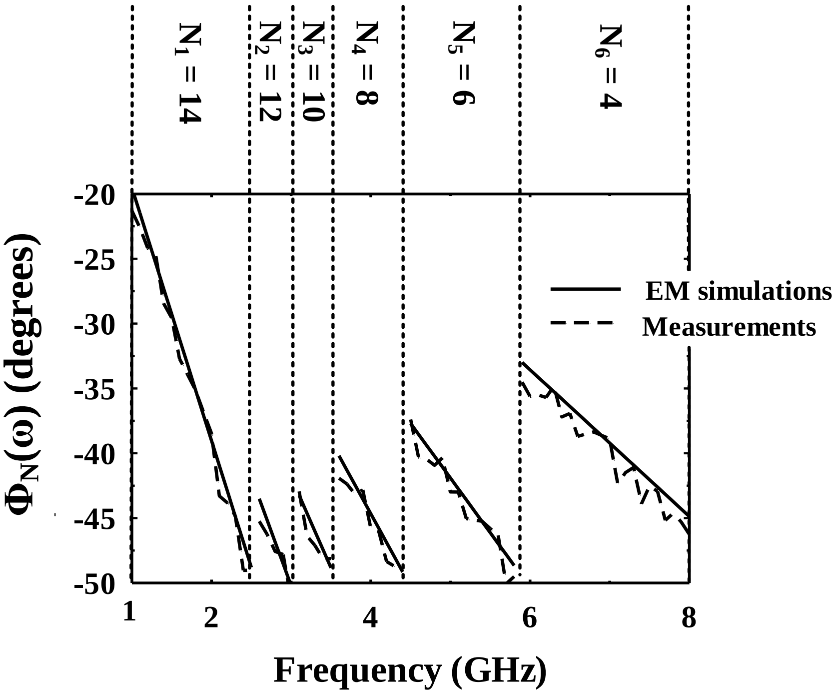


(b)

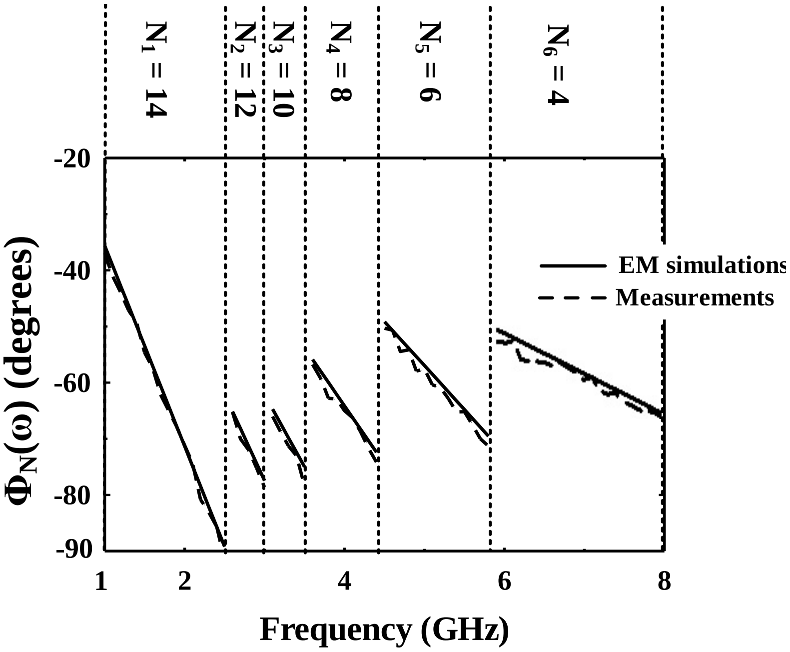
Figure 3.12: (a) Measured return loss and (b) measured insertion loss of the prototypes when air and methanol are deposited.

Fig. 3.13 shows the measurements of the phase shift compared to EM simulations considering the frequency dependency of ϵ_r' of deposited materials. The EM simulation is performed separately for each frequency considering the corresponding value of ϵ_r' of air and methanol from the cole-cole model in the simulation. Fig. 3.13(a) and (b) show the simulated and measured phase response of different prototypes when exposed to air and methanol, respectively, proving the proper operation of cascaded TTD cells.

In this system, the frequency range is limited to 1-8 GHz. However, the proposed system and techniques are still valid for chemical detection at frequencies higher than 8 GHz. This requires extending the frequency range at which acceptable input matching is still achieved as given in (3.7) and (3.8). The upper frequency limit can be increased above 8 GHz by decreasing the value of the TTD cell elements in Fig. 3.4, including the sensing capacitor, to make the input matching condition less sensitive to any capacitance variation due to permittivity of MUTs. However, this comes at the cost of lower phase shift and sensitivity, especially at lower frequencies. Moreover, the lower frequency limit can be decreased by employing more number of TTD cells in cascade for higher detection accuracy at low frequencies at the cost of larger sensor area.



(a)



(b)

Figure 3.13: Simulated and measured phase shift of the prototypes when (a) air and (b) methanol are deposited.

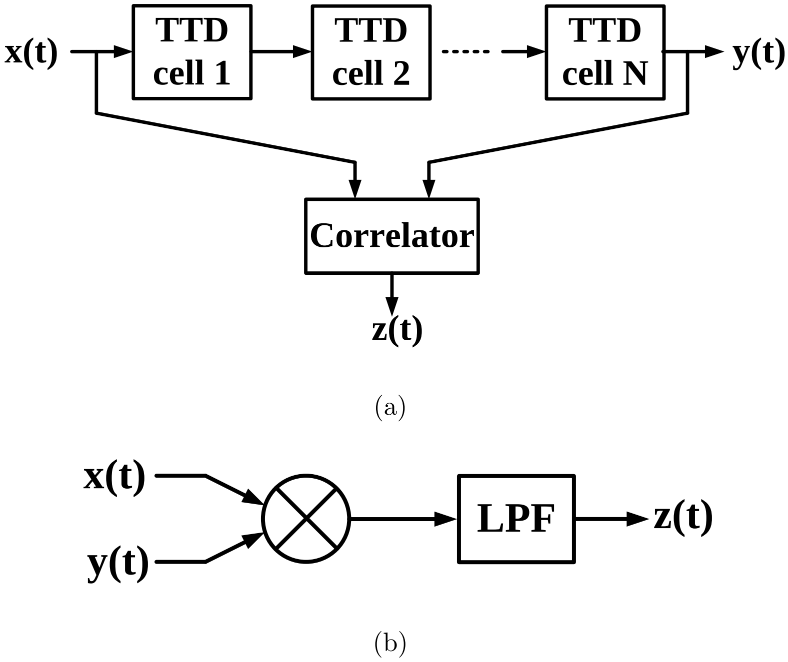


Figure 3.14: (a) N-cascaded TTD cells with the input and output signals applied to a correlator, and (b) functional block diagram of the correlator.

In order to detect the phase shift of a microwave signal passing through the chain of N cascaded TTD cells, the input and output signals are applied to a correlator as shown in Fig. 3.14(a). The correlator consists of a down-conversion mixer followed by a low-pass filter (LPF) as shown in Fig. 3.14(b). In Fig. 3.14, $x(t)$ is a single-tone signal at the sensing frequency ($\omega_s = 2\pi f_s$) with an amplitude of A_1, or $x(t) = A_1 \cdot \cos(\omega_s t)$. $y(t)$ is a phase-shifted version of $x(t)$ with an amplitude of A_2, or $y(t) = A_2 \cdot \cos(\omega_s t - \phi_N(\omega_s))$, where $\phi_N(\omega_s)$ is the phase shift achieved by N- cascaded TTD cells and is approximately equal to N times the phase shift achieved by one TTD cell ($\phi_N(\omega_s) \approx N \cdot \phi(\omega_s)$). According to the EM simulations shown in Fig. 3.7(b), the TTD cell exhibits very low loss over the entire frequency range. Therefore, as a first order approximation, the amplitudes of $x(t)$ and $y(t)$ are assumed to be equal ($A_1 = A_2 = A$). Accordingly, the output of the down-conversion mixer in Fig. 3.14(b) is the product of $x(t)$ and $y(t)$ and is given by

$$x(t) \cdot y(t) = \frac{A^2}{2}\cos(\phi_N(\omega_s)) + \frac{A^2}{2}\cos(2\omega_s t - \phi_N(\omega_s)) \tag{3.12}$$

If the cut-off frequency of the low-pass filter following the mixer is much lower than $2\omega_s$, then the output of the correlator $z(t)$ is a DC signal given by

$$z(t) = \frac{A^2}{2} \cdot \cos(N \cdot \phi(\omega_s)) \tag{3.13}$$

Therefore, the DC output of the correlator $z(t)$ is proportional to the cosine of the phase shift through N- cascaded TTD cells and can be used to detect the permittivity in the corresponding frequency range. However, based on the analysis performed in subection 2.2, the number of TTD cells assigned for permittivity detection is made frequency dependent for good detection accuracy (Fig. 3.10). Therefore, the signals at the input of the correlator ($x(t)$ and $y(t)$) should be reconfigured such that the number of TTD cells allocated between the input signals (N_i) varies according to the the subfrequency range (Fig. 3.10).

This can be simply performed by switching the location of the second input of the correlator ($y(t)$) in a chain of cascaded TTD cells as shown in Fig. 3.15. The system shown in Fig. 3.15 has two major practical issues: (1) the correlator should be wideband covering the frequency range of 1-8 GHz. This can be alleviated by employing two or more correlators, each covering a portion of the 1-8 GHz frequency range; and (2) commercial microwave mixers have both inputs matched to low input impedance (around 50 Ω). Therefore, using a correlator to detect the phase shift between two points ($x(t)$ and $y(t)$) on a single chain of N-cascaded TTD cells (Fig. 3.15) loads the chain with more than one low impedance loads at the same time, thus affecting the overall input matching and the proper operation of the TTD cells. To alleviate this problem, two separate chains of TTD cells are employed. The two chains are excited using the same signal generator ($p(t) = A\cos(\omega_s t)$). The first and second chains are responsible for generating the inputs of the correlator $x(t)$ and $y(t)$, respectively, as shown in Fig. 3.16. For example, to detect the permittivity in the first subfrequency range ($i = 1$ and $N_i = 14$), $x_1(t) = A\cos(\omega_s t)$ and $y_4(t) = A\cos(\omega_s t - 14 \cdot \phi(\omega_s))$, are selected from chains 1 and 2, respectively, and applied to the correlator to have an output voltage proportional to $\cos(14 \cdot \phi(\omega))$. For the second subfrequency range ($i = 2$ and $N_i = 12$), $x_1(t) = A\cos(\omega_s t)$ and $y_3(t) = A\cos(\omega_s t - 12 \cdot \phi(\omega_s))$ are selected from chains 1 and 2, respectively, for a correlator output proportional to $\cos(12 \cdot \phi(\omega))$. Further signal switching is then performed to cover the entire 1-8 GHz frequency range.

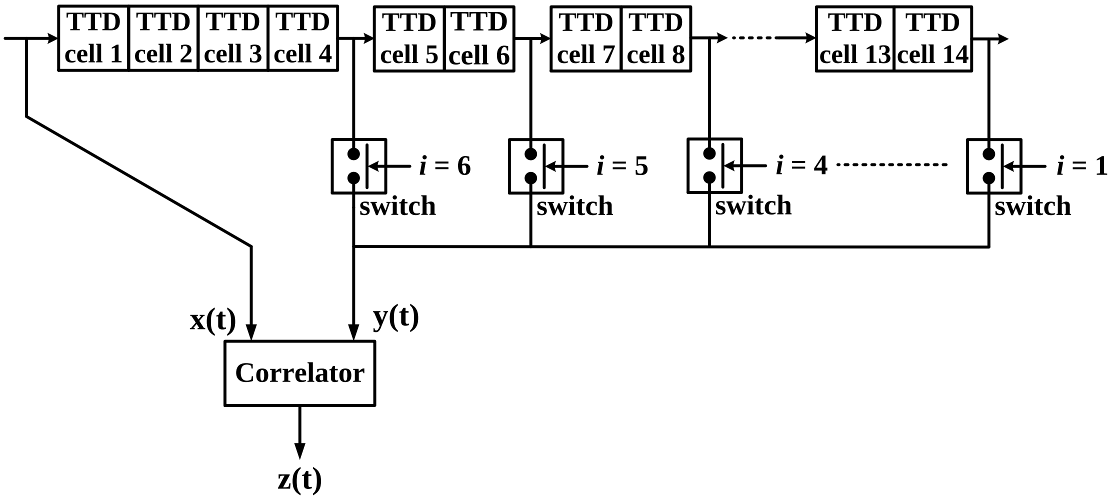


Figure 3.15: Reconfigurable sensing system by switching the input ($y(t)$) applied to the correlator.

Single-pole dual-throw (SPDT) RF switches are used to select the signals $x(t)$ and $y(t)$ from chains 1 and 2 according to the subfrequency range using the control signals (C_k: $1 \leq k \leq 8$). The signals selected from chains 1 and 2 are then applied to correlators. In this design, two correlators are used. Correlator 1 covers the frequency range up to 3.5 GHz ($i = 1$, 2 and 3) and correlator 2 covers the frequency range up to 8 GHz ($i = 4$, 5 and 6) as will be shown in the next subsection. Fig. 3.16 shows an example of the switching setup used to detect the permittivity in the first subfrequency range where the switches C_4 and C_8 are activated to connect $x_1(t)$ and $y_4(t)$ to correlator 1. The output of correlator 1 ($z_1(t)$) is then proportional to $\cos(14 \cdot \phi(\omega))$.

Two 50 Ω resistors (R_1 and R_2) are inserted in series with each chain to make the overall impedance seen by the signal generator $p(t)$ to be 50 Ω for proper input matching. The use of these resistors helps in input matching at the cost of power loss for each chain of TTD cells.

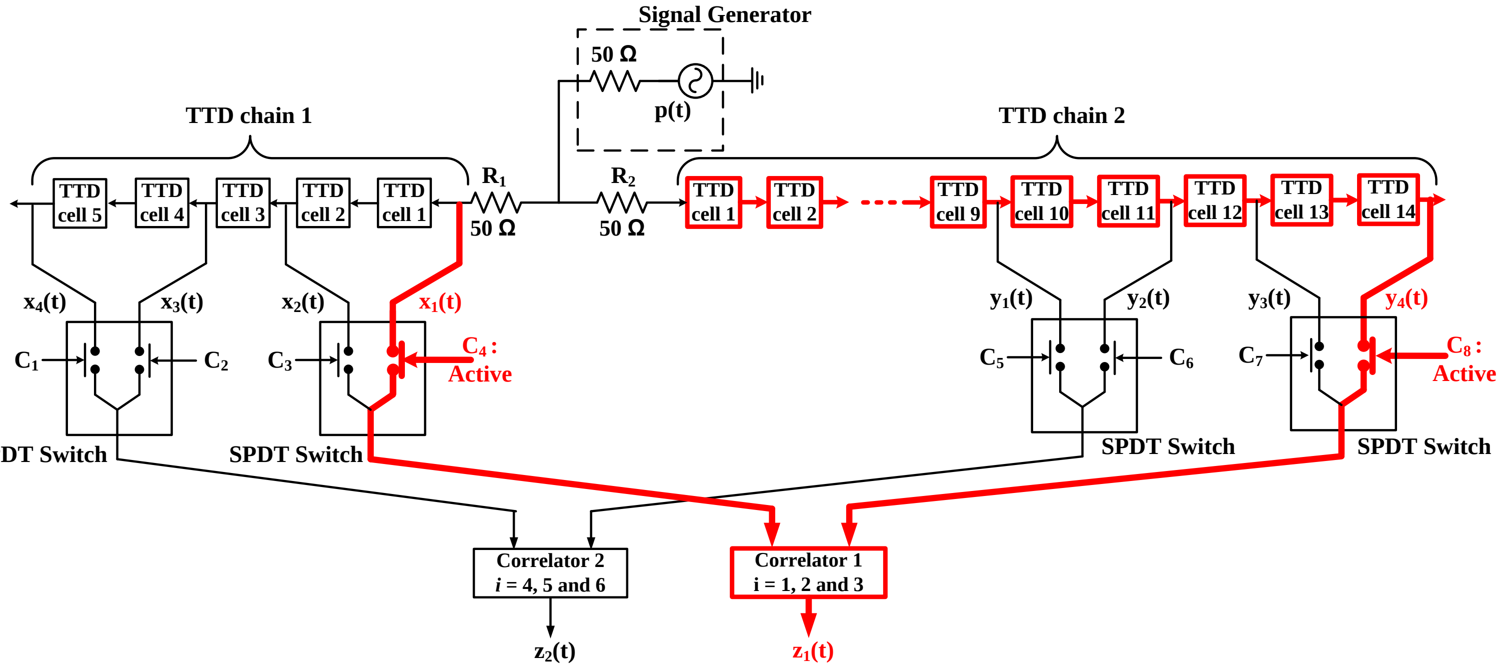


Figure 3.16: Block diagram of the dielectric spectroscopy system. The bold lines in red represent the switching setup for permittivity detection in the first subfrequency range ($i = 1$ and $N_i = 14$).

Table 3.1 shows different switching configurations for different subfrequency ranges, the corresponding selected signals and the corresponding values of N_i and detected phase shifts. The subfrequency ranges are overlapping to ensure full coverage of the sensing frequencies in the 1-8 GHz range. For example, in subfrequency range 3, switches C_3 and C_7 in TTD chains 1 and 2 are activated to enable correlation between $x_2(t) = p(\omega_s t - 2\phi(\omega_s))$ and $y_3(t) = p(\omega_s t - 12\phi(\omega_s))$. The phase shift between $x_2(t)$ and $y_3(t)$ is equal to $10 \cdot \phi(\omega_s)$, which is the phase shift corresponding to 10 cascaded TTD cells.

Table 3.1: Different switching combinations for the system in Fig. 15 along with the corresponding signals, frequency range and detected phase shift.

i	Subfrequency range	Active Switches	$x(t)$	$y(t)$	$z(t)$	N_i	Phase shift
1	1-2.5 GHz	C_4 and C_8	$x_1(t)$	$y_4(t)$	$z_1(t)$	14	$14 \cdot \phi(\omega)$
2	2.2-3 GHz	C_4 and C_7	$x_1(t)$	$y_3(t)$	$z_1(t)$	12	$12 \cdot \phi(\omega)$
3	2.8-3.5 GHz	C_3 and C_7	$x_2(t)$	$y_3(t)$	$z_1(t)$	10	$10 \cdot \phi(\omega)$
4	3.3-4.5 GHz	C_2 and C_6	$x_3(t)$	$y_2(t)$	$z_2(t)$	8	$8 \cdot \phi(\omega)$
5	4.3-5.9 GHz	C_2 and C_5	$x_3(t)$	$y_1(t)$	$z_2(t)$	6	$6 \cdot \phi(\omega)$
6	5.7-8 GHz	C_1 and C_5	$x_4(t)$	$y_1(t)$	$z_2(t)$	4	$4 \cdot \phi(\omega)$

3.4 Circuit Implementation and Test Setup

The dielectric spectroscopy system is fabricated on Rogers Duroid substrates with a total area of 8×7.2 cm^2. The passive TTD cell is similar to the one shown in Fig. 3.6 and multiple TTD cells are arranged in cascade as shown in Fig. 3.8. Correlation and switching in Fig. 3.16 are performed using commercial discrete components. SPDT switches are packaged RF MEMS switches (2SMES-01) from Omron Inc. operating up to 10 GHz. A DC voltage of 34 V is used for actuation achieving a high isolation when open (> 30 dB) and a low insertion loss when closed (< 1 dB) up to 8 GHz.

Correlators are implemented using discrete surface mount double balanced passive mixers from Mini-Circuits. Two mixers are used to cover the entire frequency range from 1-8 GHz with a conversion loss < 7 dB: (1) MCA1-42+ used for detection in subfrequency ranges 1, 2 and 3 covering the 1-3.5 GHz frequency range, and (2) MCA1-80LH+ used for detection in subfrequency ranges 4, 5 and 6 covering the 3.5-8 GHz frequency range. Fig. 3.17 shows the photograph of the fabricated sensor using two chains of TTD cells, four SPDT switches, two passive mixers with necessary components for biasing and RF/DC input/output connections.

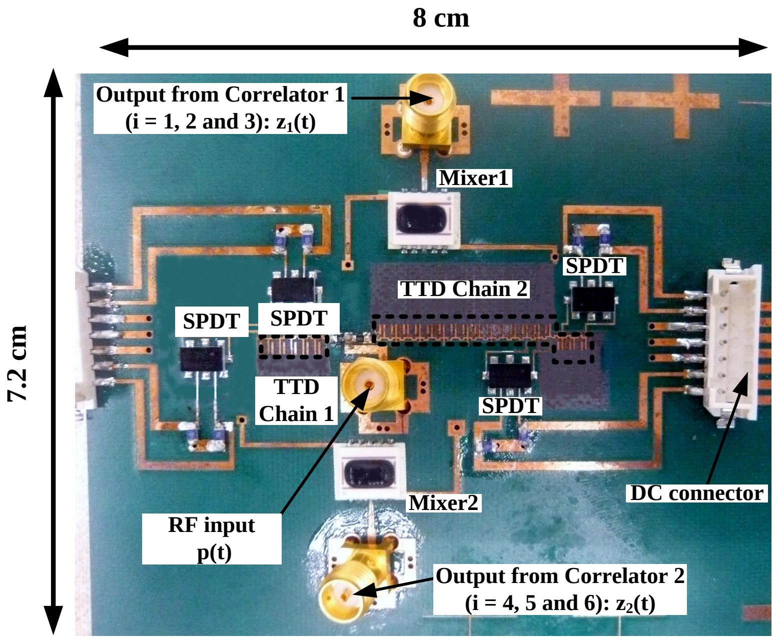


Figure 3.17: Photograph of the fabricated sensor.

Omron Inc. www.omron.com

Mini-Circuits Inc. www.minicircuits.com

The effect of capacitive and resistive loading of the switches in the OFF and ON states and the mixers should be considered regarding (1) the input impedance matching, and (2) the detection accuracy. For impedance matching, EM simulation of TTD cells is performed along with the reported S-parameters of the switches in both ON and OFF states and the mixers. This simulation adds fine tuning to the dimensions of the TTD cell to achieve proper input/output return loss and a phase-frequency response for the sensor similar to the one shown in Fig. 3.10. For example, the capacitive loading of the switch mandates slight decrease in the sensing and fixed capacitors to compensate for this extra added capacitance. Moreover, for more accurate detection and measurements, sensor calibration needs to be performed as an initial step before permittivity detection to de-embed the effect of any non-idealities, loading and mismatches as shown in Subsection 3.5.1.

For chemical sensing, the liquids under test are contained in plastic cylindrical tubes fixed and glued on top of the sensing elements in both TTD chains in a way similar to the one reported in [64]. The effect of the plastic tubes ($\epsilon_r \approx 2.2$) was not considered in the EM simulations using Sonnet in Fig. 3.13. However, the similarity between the simulations and prototype measurements employing the plastic tubes in Fig. 3.13 proves minimal effect of these tubes on the permittivity detection. Moreover, the effect of the plastic tube on the capacitance of the sensing elements is constant regardless of the permittivity of material deposited on top of the sensor. Accordingly, sensor calibration procedure discussed in subection 5.A can remove any effect from the plastic tube on the detected permittivity. Fig. 3.18(a) shows the photograph of a tube glued on top of TTD cells in one of the TTD chains. A Finnpipette single-channel micropipetter shown in Fig. 3.18(b) is used to insert liquids under test inside the tubes with 0.2 μL resolution and to remove the liquids from the tubes after

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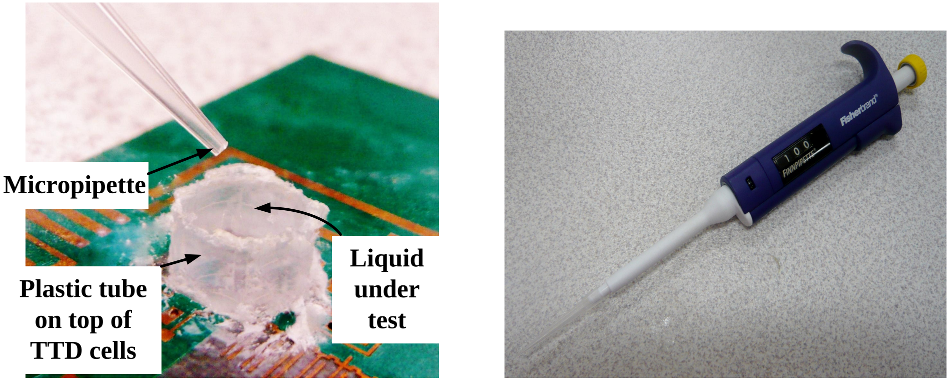
Available [online]: http://www.thermoscientific.com sensing. Commercial gas dusters are used to clean the TTD cells from any residues of deposited liquids.



(a) (b)

Figure 3.18: (a) Photograph of the tube on top of the sensing elements, and (b) Photograph of the micropipette used to insert liquids under test inside the tube.

3.5 Experimental Procedures and Results

As mentioned earlier, the detected permittivity depends on the sensing frequency and the volume of liquid deposited on top of the sensing elements. Therefore, the sensing process is performed for organic chemicals while sweeping two independent parameters: (1) The sensing frequency (f_s), which is tuned by changing the frequency of the input microwave signal, $p(t)$, in the range of 1-8 GHz; and (2) The sample volume (S_v), which is tuned by inserting different volumes of liquids inside the tubes on top of the sensing elements using the micropipette. Sample volumes are tuned within the range of 50-250 μL.

Organic chemicals are subject to permittivity detection, including: (1) Alcohols: Ethanol ($CH_3 - CH_2 - OH$), Methanol ($CH_3 - OH$), Isopropanol ($CH_3 - CH_3 -$

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$CH - OH$) and II-butyl-alcohol ($CH_3 - CH - OH - CH_2 - CH_3$); (2) Ketones: Acetone ($CH_3 - CH_3 - CO$); (3) Esters: Ethyl-acetate ($CH_3 - COO - CH_2 - CH_3$); and (4) Alkyl benzenes: Xylene ($C_6H_4 - CH_3 - CH_3$). The objective is to detect the permittivity of each material at a given sensing frequency and sample volume ($\epsilon'_r(f_s, S_v)$). The sensing system is measured by applying a sinusoidal signal using Agilent E8267D microwave signal generator for 1-8 GHz frequency range with a frequency step of 0.4 GHz.

First, the sensor is characterized using calibration materials to find the sensor's characteristic curves relating the output voltage from the correlator (V_c) and the permittivity of the MUT at each sensing frequency and sample volume. Second, unknown organic chemicals under characterization are deposited and the measured output voltage from the correlator is used along with the sensor's characteristic curves to find the permittivity of MUT ($\epsilon'_r(f_s, S_v)$). This procedure is explained in more detail as follows:

3.5.1 Sensor Characterization: V_c vs ϵ'_r Characteristic Curves Using Calibration Materials

Air, Ethanol and Methanol are used as calibration materials. Permittivities of the calibration (reference) materials are assumed to be known from the *Cole-Cole* models [6]. Each calibration material is deposited on top of the sensing elements and the output voltage of the correlator is read out at each sensing frequency and sample volume ($V_c(f_s, S_v)$). The measured values of $V_c(f_s, S_v)$ with respect to reported permittivities for the calibration materials are used to have a full V_c vs ϵ'_r characteristics for each value of sample volume and sensing frequency using curve fitting.

Since three calibration materials are used, curve fitting is limited to second order (quadratic) polynomials. Increasing the number of materials used for calibration increases the order of polynomial fitting function and improves the detection accuracy. Employing three calibration materials is proved to be enough for a good accuracy of permittivity detection as will be shown later. The V_c vs ϵ'_r characteristic equation is represented as

$$|V_c(f_s, S_v)| = a(f_s, S_v) \cdot \epsilon'^2_r(f_s, S_v) \tag{3.14}$$

$$+ \; b(f_s, S_v) \cdot \epsilon'_r(f_s, S_v) + c(f_s, S_v) \tag{3.15}$$

where a, b and c are the polynomial fitting parameters and are functions of sensing frequency (f_s) and the sample volume (S_v). Fig. 3.19 shows the fitted V_c vs ϵ'_r characteristics at volumes ranging from 50 μL to 250 μL at the sensing frequency of 1 GHz as an example. These plots can be used to extract the values of a, b and c at 1 GHz for different values of S_v using curve fitting.

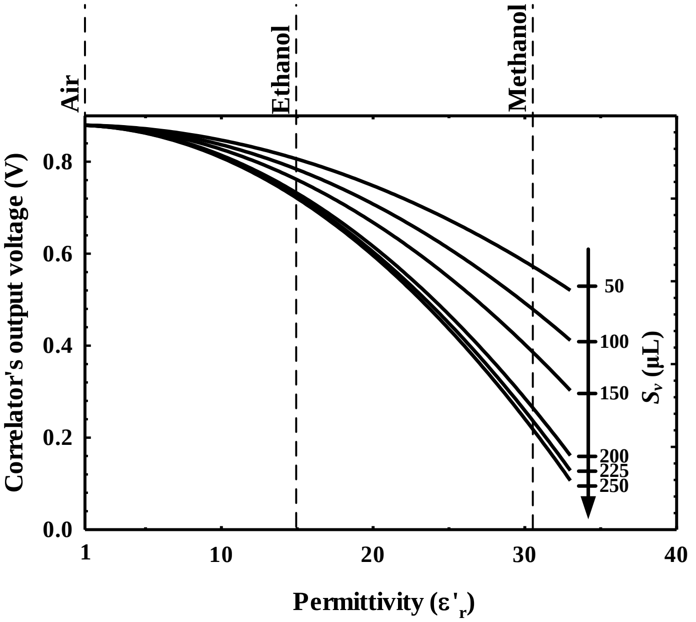


Figure 3.19: Fitted V_c vs ϵ'_r characteristics at volumes ranging from 50 to 250 μL at the sensing frequency of 1 GHz.

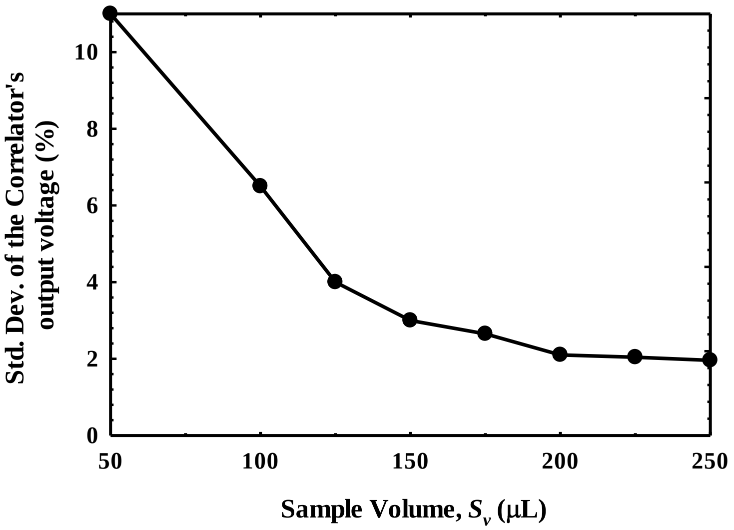
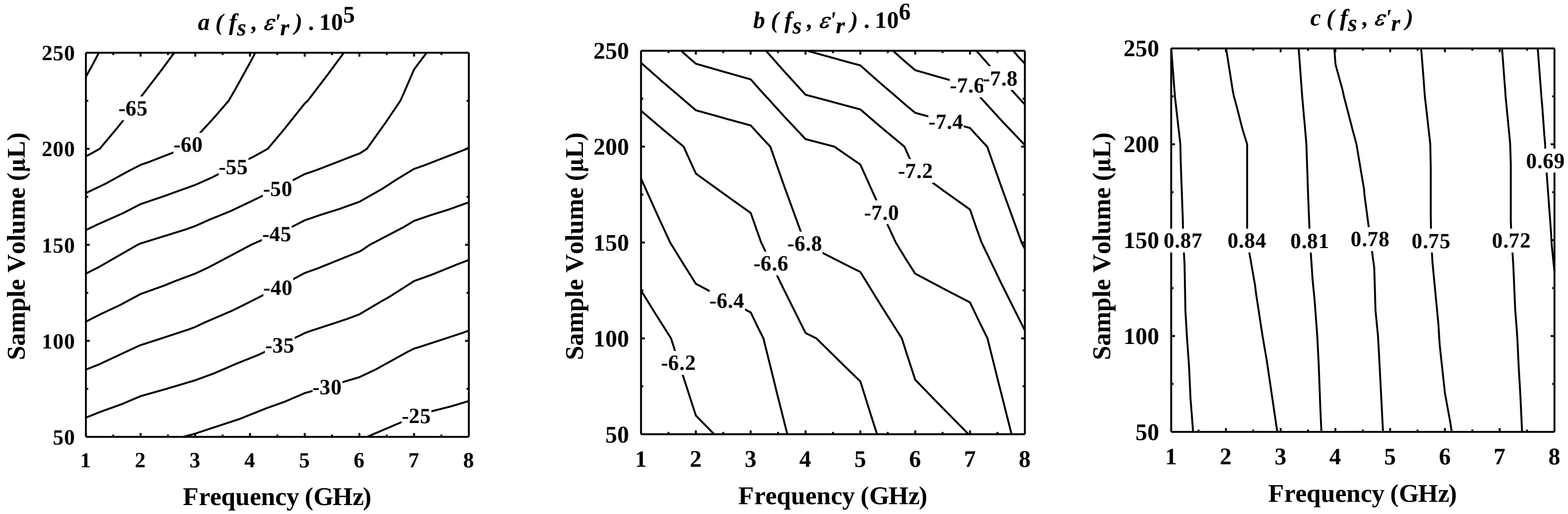


Figure 3.20: Standard deviation of the correlator's output voltage as a function of the sample volume (S_v) at a frequency of 1 GHz.

Fig. 3.20 shows the standard deviation of the correlator output voltage (V_c) over 20 different trials at 1 GHz. The standard deviation decreases with increasing the sample volume and reaches a value of 2% for $S_v > 200\mu$L at which the EM fields are well confined around the sensing elements. Plots similar to Fig. 3.19 and 3.20 are generated for frequencies in the range of 1 to 8 GHz with a frequency step of 0.4 GHz. The dependency of the standard deviation on the sample volume (S_v) at all frequencies is similar the one at 1 GHz (Fig. 3.20).

As the mean values of the fitting parameters (a, b and c) over the 20 different trials are dependent on both the sensing frequency and sample volume, contour plots are used to illustrate this dependency as shown in Fig. 3.21(a), (b) and (c). The values of $a(f_s, S_v)$, $b(f_s, S_v)$ and $c(f_s, S_v)$ in Fig. 3.21 are used for characterization of unknown organic chemicals in the next step of the sensing procedure.



(a) (b) (c)

Figure 3.21: Contour plots showing the variations of the fitting parameters with sensing frequency (f_s) and the sample volume (S_v): (a) $a(f_s, S_v) \cdot 10^5$, (b) $b(f_s, S_v) \cdot 10^6$, and (c) $c(f_s, S_v)$.

3.5.2 Dielectric Spectroscopy of Organic Chemicals

Organic chemicals are subject to permittivity detection in the frequency range of 1-8 GHz, including acetone, ethyl acetate, isopropanol, II-butyl alcohol and xylene. In order to detect the permittivity of an organic chemical at a given sensing frequency (f_s) and sample volume (S_v), the sensing process is performed in three steps:

(1) Characteristic Equation: Extract the values of the fitting parameters (a, b and c) corresponding to the sensing frequency (f_s) and sample volume (S_v) from the contour plots in Fig. 3.21.

(2) Material Sensing: The frequency of the microwave signal generator is set to f_s and a volume of S_v of the MUT is deposited on top of the sensing elements. The voltage at the output of the correlator ($V_c(f_s, S_v)$) is then detected.

(3) Permittivity Computation: Using the extracted values of $a(f_s, S_v)$, $b(f_s, S_v)$ and $c(f_s, S_v)$; and the detected voltage at the output of the correlator ($V_c(f_s, S_v)$), the value of permittivity, $\epsilon_r'(f_s, S_v)$, is found as follows

$$\epsilon_r'(f_s, S_v) \quad = \quad \frac{-b(f_s, S_v) + \sqrt{\gamma}}{2 \cdot a(f_s, S_v)} \tag{3.16}$$

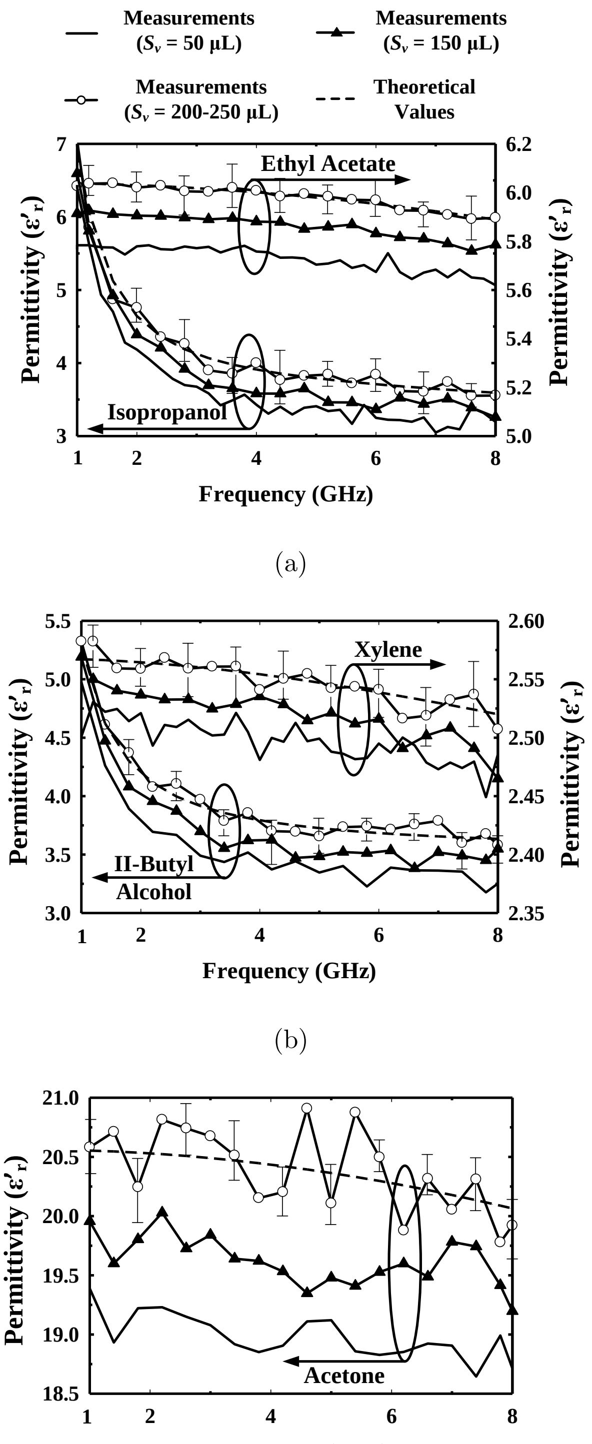
where

$$\gamma = b^2(f_s, S_v) - 4 \cdot a(f_s, S_v) \cdot [c(f_s, S_v) - V_c(f_s, S_v)] \tag{3.17}$$

Similar procedure is repeated for other chemicals at all values of f_s and S_v to perform full dielectric spectroscopy of MUT for 1-8 GHz frequency range.

As an example, Ethyl Acetate is characterized at $f_s = 1$ GHz and $S_v = 250$ μL. The above sensing procedure is applied as follows: (1) the extracted values of a, b and c are -70 $\cdot 10^{-5}$,-6.8 $\cdot 10^{-6}$ and 0.87; respectively. Accordingly, the characteristic equation is given by V_c(1 GHz, 250 μL) = -70 $\cdot 10^{-5} \epsilon_r'^2$-6.8 $\cdot 10^{-6} \epsilon_r'$ + 0.87, (2) 250 μL of Ethyl Acetate is deposited and the frequency of the signal generator is set to 1 GHz. The measured correlator's output voltage V_c(1 GHz, 250 μL) is found to be 0.848 V; and (3) Substituting the values of V_c(1 GHz, 250 μL), a, b and c in (3.16) and (3.17) results in a permittivity ϵ_r'(1 GHz, 250 μL) of 6.7.

Fig. 3.22(a), (b) and (c) show the average measured values of ϵ_r' of different organic chemicals versus the sensing frequency (f_s) for different values of S_v over 20 different trials. Fig. 3.22 shows that the accuracy of detection of $\epsilon_r'(f_s, S_v)$ increases with increasing the volume of liquid deposited on top of the sensing elements. The value of $\epsilon_r'(f_s, S_v)$ does not change for volumes larger than 200 μL at which the measurement results for the organic chemicals are very close to the theoretical values based on *Cole-Cole* models [6]. This is because EM fields are well confined around the sensing capacitors for these volumes and the electromagnetic field intensity becomes independent of S_v. The absolute value of the relative error between the measured permittivities at $S_v > 200\mu$L and the theoretical values is less than 2%. Error bars in Fig. 3.22 show the variance of measured points (20 different trials) around the mean values for S_v = 250 μL.



(a)

(b)

(c)

Figure 3.22: Measured permittivities versus frequency for different volumes for (a) Isopropanol and Ethyl Acetate, (b) Xylene and II-Butyl Alcohol and (c) Acetone. The measured permittivity is compared with values from the cole-cole model.

3.6 Applications to Dielectric Characterization and Spectroscopy

3.6.1 Estimation of Permittivities at Low Frequencies

As mentioned before, one of the advantages of broadband dielectric spectroscopy is the possibility to detect the low-frequency permittivity of samples using extrapolation. The detected permittivities of MUTs in Fig. 3.22 in the frequency range of 1-8 GHz are used to estimate the values of ϵ_r' of these materials at frequencies below 1 GHz, specially at zero-frequency. This can be done by fitting the measured points in Fig. 3.22 to a polynomial function given by

$$\epsilon_r' = \sum_{i=0}^{n} x_i \cdot f^i \tag{3.18}$$

where x_i are the coefficients of the polynomial function, n is the polynomial order and f is the frequency in GHz. The higher the order of the polynomial (n) is, the higher the fitting accuracy is. Then, the values of ϵ_r' at frequencies below 1 GHz can be found by substituting $f < 1$ in (3.18). As an example, the measured points of Isopropanol for $S_v = 250\ \mu L$ are fitted to a fifth order polynomial function: $\epsilon_r' = -0.0106f^5 + 0.248f^4 - 2.3f^3 + 10.06f^2 - 20.7f + 20.1$. This polynomial function is plotted for all frequencies between 0 and 8 GHz along with the measured points in the 1-8 GHz range as shown in Fig. 3.23. The permittivity of Isopropanol at zero-frequency is estimated to be 20.1 compared to a theoretical value of 20.24 [6]. Similar procedure with fifth order polynomial fitting is repeated for other MUTs and the zero-frequency permittivity is estimated and compared to the theoretical value as shown in Table 3.2 with an error less than 2%.

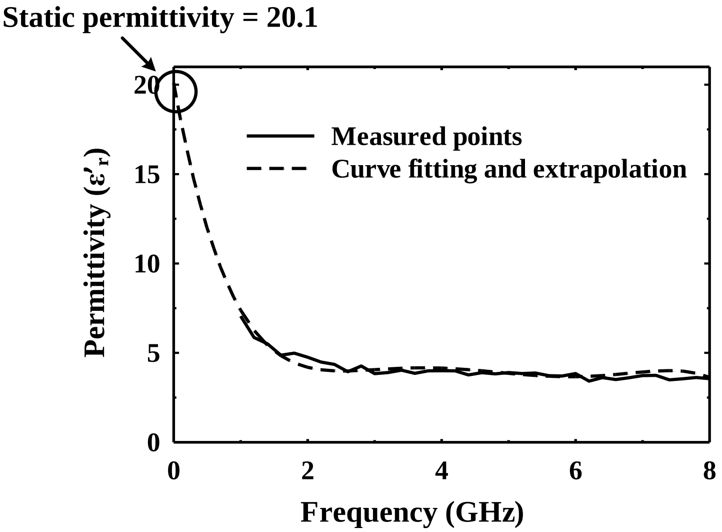


Figure 3.23: Measured points for Isopropanol ($S_v = 20\mu$L) with the extrapolated curve to estimate the permittivity of isopropanol at frequencies below 1 GHz.

Table 3.2: Estimated and Theoretical Static Permittivities of MUTs.

MUT	Estimated value	Theoretical value [6]
Isopropanol	20.1	20.24
Ethyl Acetate	6.12	6.04
II-Butyl Alcohol	15.66	15.8
Xylene	2.56	2.568
Acetone	20.5	20.55

3.6.2 Mixture Dielectric Characterization

In this subsection, the dielectric spectroscopy system is employed to characterize binary mixtures similar to the way described in Section 2. The unified mixing approach in (2.5) is used to estimate the complex permittivities of binary mixtures.

The sensing procedure in Subsection 3.5 is employed to characterize ethanol (host) - methanol (guest) mixtures. Characteristic equations developed in Subsection 3.5 for different sensing frequencies and sample volumes are employed in mixture characterization. For example, ethanol-methanol binary mixture is characterized at $f_s = 4.5$ GHz and $S_v = 250$ μL with fractional volumes of $(1 - q) = 0.2$ and $q = 0.8$; respectively. The sensing process described in Subsection 3.5 is performed as follows: (1) at $f_s = 4.5$ GHz and $S_v = 250$ μL, the values of a, b and c are $-58 \cdot 10^{-5}$, $-7.43 \cdot 10^{-6}$ and 0.773; respectively. (2) Using the micropipette, 50 μL of Ethanol and 200 μL of methanol are mixed together ($q = 0.8$) and deposited on top of the sensing cells. The frequency of the signal generator is set to 4.5 GHz and the output voltage of the correlator is found to be 0.77 V; and (3) Using the values of a, b, c and V_c and (3.16) and (3.17), the value of the permittivity is found to be 6.26. Similar procedure is applied for all values of q between 0 and 1. Fig. 3.24 shows the average values of the detected dielectric constant of the ethanol-methanol mixture ($\epsilon_r'(f_s = 4.5$ GHz, $S_v = 250$ μL)) versus q over ten different trails compared with one of the theoretical mixture models ($\upsilon = 0$ in (2.5)). Zoomed portion of ϵ_r' vs q within the ranges of $0 \leq q \leq 0.05$ and $0.95 \leq q \leq 1$ are also shown. Fig. 3.24 shows detected permittivities are very close to theoretical values with a relative error less than 2% with a fractional volume (q) accuracy of 1%. Error bars in Fig. 3.24 show the variance of the ten measured points around the mean values for $0 \leq q \leq 0.05$ and $0.95 \leq q \leq 1$.

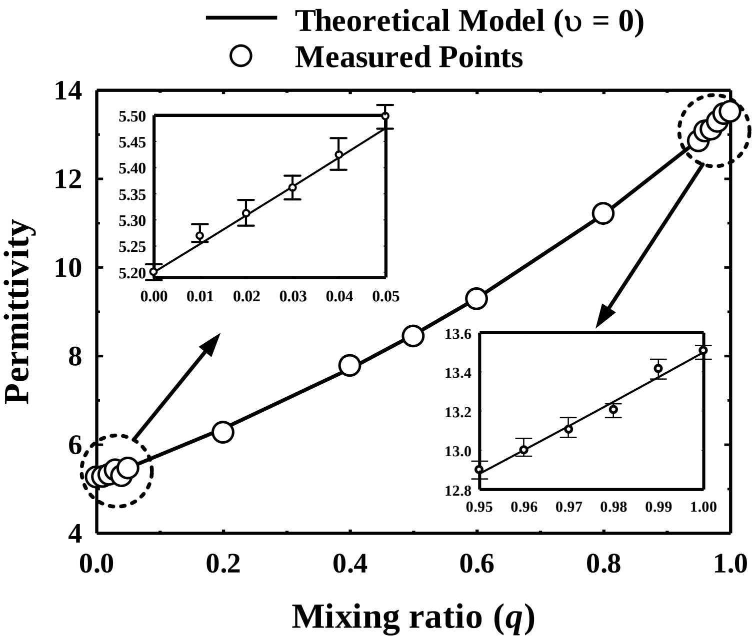


Figure 3.24: The measured and theoretical permittivities versus the mixing ratio, q, for the Ethanol-Methanol binary mixture at $S_v = 250\ \mu$L and $f_s = 4.5$ GHz with zoomed views at $0 \leq q \leq 0.05$ and $0.95 \leq q \leq 1$.

3.7 Summary

A miniaturized platform for broadband dielectric spectroscopy system has been developed for permittivity detection of organic chemicals for the frequency range of 1-8 GHz. The design of cascaded TTD cells to detect the frequency dependent permittivity has been presented in detail considering non-ideal effects such as the electromagnetic coupling between adjacent cells. The spectroscopy system, including TTD cells, correlators and SPDT switches, has been calibrated using reference materials. Using a unique detection procedure, the system is demonstrated to detect the permittivity of organic chemicals in the 1-8 GHz frequency range, and estimate the static permittivity using extrapolation with an accuracy of 2%. Also, the system is used to characterize the binary mixtures to around 1% fractional volume acuracy.

4. A CMOS INDUCTOR-LESS NOISE-CANCELLING BROADBAND LOW NOISE AMPLIFIER WITH COMPOSITE TRANSISTOR PAIR

4.1 Introduction

Today, the advances in semiconductor technology guide the progress in the wireless communications circuits and systems area. Various new communication standards have been developed to accommodate a variety of applications at different frequency bands, such as digital video broadcasting at 450-850 MHz, FM transceivers at 87-108 MHz, satellite communications at 950-2150 MHz, global positioning system (GPS) at 1.2 GHz, and cellular radios at 850-1900 MHz. The modern wireless industry is now motivated by the global trend of developing multi-band/multi-standard terminals for low-cost and multifunction transceivers [65, 66, 67]. Stacking several front-ends for the reception of various standards was one of the design trends to realize these wideband receivers [65, 66, 67]. Today, the design trend is now focused on using single wideband front-ends in order to accommodate all the standards using a single front-end as well as reduce the chip area. Single wideband front-ends face many challenging problems including very low noise figure, high linearity requirements, and low area consumption.

Wideband low noise amplifiers are key building blocks in wideband front-ends. Inductor-less topologies have been proposed to reduce the area consumption [68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78]. These LNAs usually rely on resistive feedback techniques for wideband input matching, which leads to poor noise figure, and hence, poor sensitivity. In addition, due to the flicker noise, they are not suitable for

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sub-100 MHz communications. Therefore, noise cancellation techniques have been proposed in the literature to overcome the poor noise figure of these inductor-less wideband LNAs [68, 71]. These techniques depend on the matching between the devices to be able to achieve the required noise figure reduction. The best reported noise figure using this approach is 1.9 dB [68]. Reducing the noise figure below 1.9 dB is still challenging and a solution is provided in this section.

The proposed broadband LNA in this section achieves a low noise figure by utilizing a composite NMOS/PMOS transistor pair connected in a cross-coupled configuration to provide partial noise cancellation of the main transistors [44]. The proposed solution does not rely on the matching between the devices making the new architecture more tolerant to process variation.

The section is organized as follows: In subsection 4.2, the conventional wideband LNA with resistive matching is discussed. Subsection 4.3 presents the basic idea of the proposed wideband LNA. Also, analytical expressions for the performance parameters are derived. Subsection 4.4 discusses the actual circuit implementation, the optimum sizing of the proposed LNA, and comparison to the conventional LNAs. Subsection 4.5 demonstrates the measured and simulated results for on-wafer and packaged prototypes. Finally, Subsection 4.6 concludes and summarizes the proposed work.

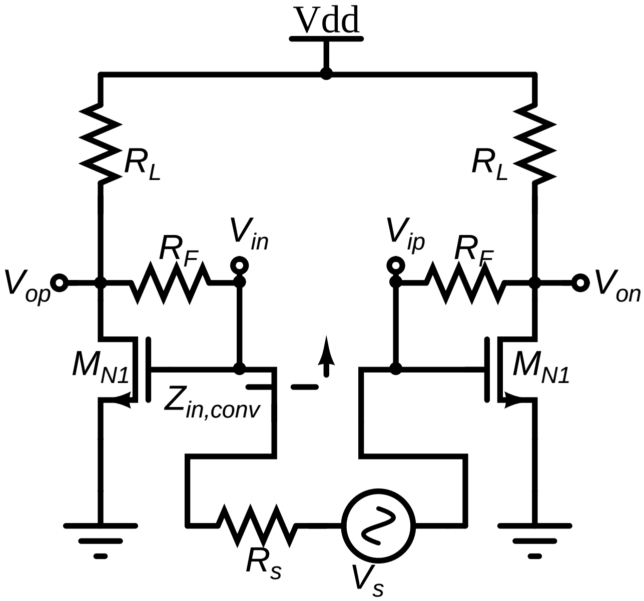


Figure 4.1: Conventional broadband LNA with resistive matching

4.2 Background

Fig. 4.1 presents the conventional broadband LNA with resistive shunt feedback matching. For this architecture, the differential input resistance, $R_{in,conv}$, and differential voltage gain, $A_{v,conv}$, are given as follows

$$\begin{aligned} R_{in,conv} &= \frac{2}{g_{m,n}} \cdot \left(1 + \frac{R_F}{R_L}\right) = R_s, \qquad (4.1) \\ A_{v,conv} &= \frac{V_{op} - V_{on}}{V_{in} - V_{ip}} = -g_{m,n} \cdot R_F // R_L, \qquad (4.2) \end{aligned}$$

where $g_{m,n}$ is the transconductance of the transistor M_N, $g_{m,n}R_F >> 1$. R_L consists of the load resistance and the output resistance of the transistor M_N. Considering the thermal noise of the input transistor, R_F and R_L, and assuming the LNA is designed with perfect matching ($R_{in,conv} = R_s$), the noise figure, NF_{conv} is calculated from [78]

$$NF_{conv} = 1 + \frac{2\gamma_n}{g_{m,n}R_s} + \frac{1}{2}\left(1 + \frac{2}{g_{m,n}R_s}\right)^2 \frac{R_s}{R_F} + \frac{2}{g_{m,n}^2 R_L R_s}. \tag{4.3}$$

The parameter, γ_n, is the transistor thermal noise factor. The first term in (4.3) is due to the thermal noise of the transistor, while the second and third ones are due to R_F and R_L, respectively. For this LNA, the noise figure is mainly determined by the noise contribution of the MOS transistor. To design for a lower NF_{conv}, the value of $g_{m,n}$ has to increase through either increasing the transistor aspect ratio or current consumption. Increasing the aspect ratio increases the input/output capacitance and therefore limits the wideband operation. This limitation is shown later in this section through schematic-level simulations. On the other hand, increasing the current increases the power consumption of the LNA. Typically, the minimum NF_{conv} is around 1.8 dB.

The main reason for the high noise figure can be explained qualitatively using Fig. 4.2. In this figure, the noise due to the NMOS transistor at the right section of the circuit is considered. The left section is replaced with its equivalent input resistance, $R_s/2$. As shown the noise current generates an output voltage, V_{on}. Then, V_{on} produces a voltage at node V_x, which is then amplified by the left section with an opposite polarity. The exact analysis shows that $V_{on} = -V_{op}$, and therefore the total output noise doubles leading to a higher noise figure. To overcome this problem, a new architecture is proposed to avoid doubling the output noise voltage and as a result reduces the lower limit than the one defined by (4.3).

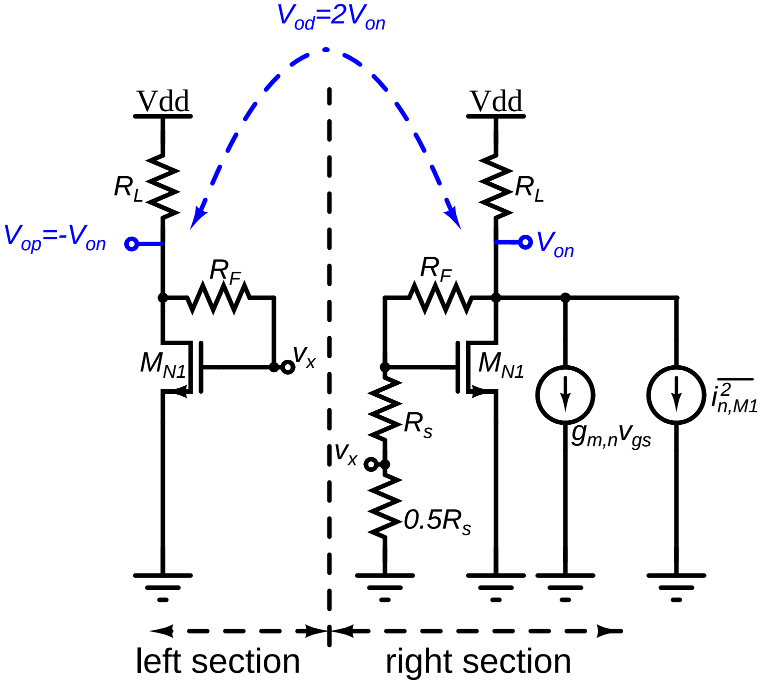
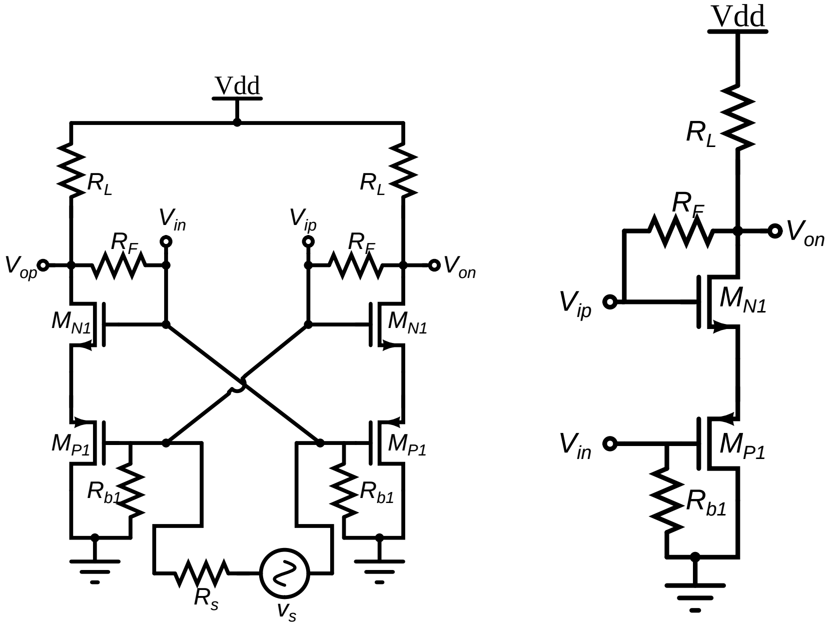


Figure 4.2: Equivalent circuit model showing the effect of noise current of M_N for the conventional LNA.

4.3 Proposed Wideband LNA

Fig. 4.3 shows the simplified schematic of the proposed broadband LNA architecture. This architecture is similar to the conventional broadband LNA with resistive matching, however, the overall noise figure is reduced by incorporating the transistor M_P and connecting the gate of M_P to the gate of M_N in a cross-coupled fashion. As shown below, this composite configuration of the NMOS and PMOS transistors reduces the output noise of the two transistors and results in a lower output noise. The input matching is adjusted through the resistive feedback resistance R_F and the effective transconductance of the overall LNA.



(a) (b)

Figure 4.3: (a) Simplified schematic of the proposed LNA architecture, and (b) half-circuit model.

4.3.1 Basic Idea: Qualitative Analysis

The basic cell of the proposed LNA is the composite NMOS/PMOS transistors configuration shown in Fig. 4.4. In this configuration, the NMOS and PMOS transistors appear in series, and the inputs are assumed to be V_1 and V_2. Ideally, if the two inputs have the same amplitude and phase, then the source voltage of the two transistors, V_s, is the same as the input leading to a zero output current. On the other hand, if the two inputs have the same amplitude but differ in phase, then V_s is an AC ground resulting in a finite output current. Hence, this configuration amplifies the differential voltage and rejects the common-mode one. Due to series configuration of the two transistors, shown in Fig. 4.4, the effective transconductance, $g_{m,eff}$, is given by the series combination of the NMOS and PMOS transistors.

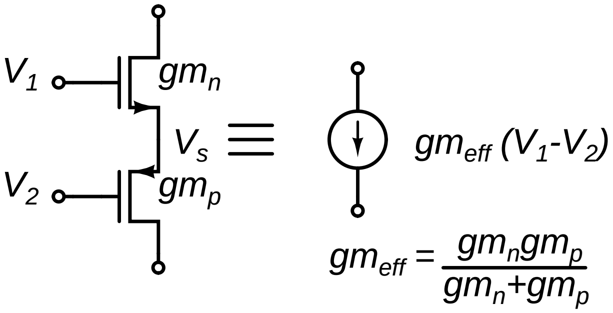


Figure 4.4: Composite NMOS/PMOS transistor architecture.

As a result, the output current is given by

$$i_o = g_{m,eff} \cdot (V_1 - V_2), \tag{4.4}$$

$$g_{m,eff} = \frac{g_{m,n} \cdot g_{m,p}}{g_{m,n} + g_{m,p}}, \tag{4.5}$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductance of the NMOS and PMOS transistors, respectively. The composite NMOS/PMOS transistor is used as the basic cell to reduce the overall noise figure of the LNA shown in Fig. 4.3(a). The amplification of the input signal is demonstrated by considering the half-circuit model shown in Fig. 4.3(b). In this model, input signals to gates of M_N and M_P carry different polarity ($V_{in} = -V_{ip}$) leading to an amplification of the input signal. In case both inputs have the same polarity ($V_{in} = V_{ip}$), the output AC current is zero, leading to common-mode noise rejection.

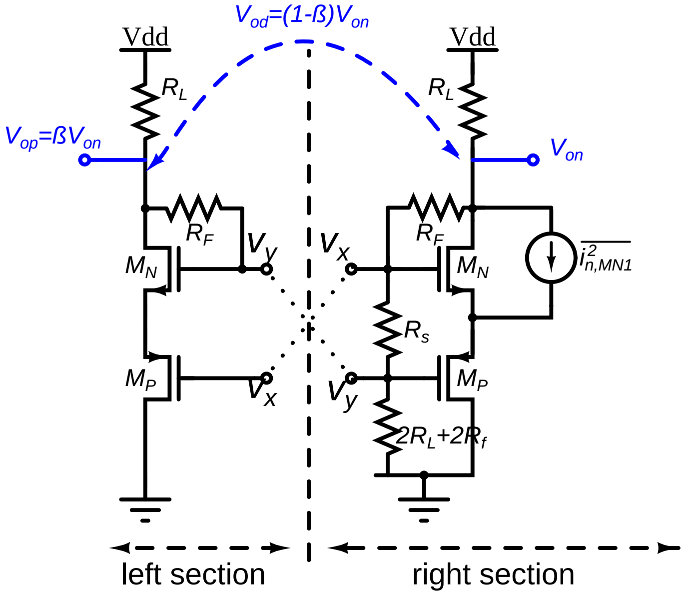
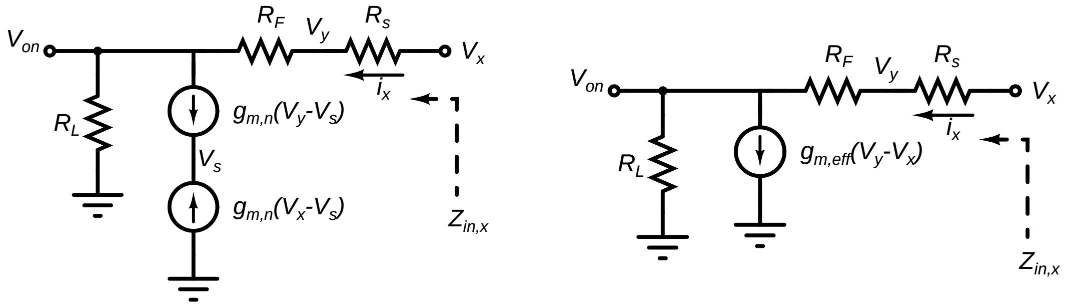


Figure 4.5: Equivalent circuit model showing the effect of noise current of M_N for the proposed LNA.

Considering the noise generated by the NMOS and PMOS transistors, the cross connection leads to partial noise cancellation of the generated noise. The partial noise cancellation is clarified qualitatively for the proposed architectures, as shown in Fig. 4.5. In this figure, the noise current due to the right NMOS transistor, i_{n,M_N}, is considered. The left section is replaced by its input impedance, which is analytically derived using the small signal model in Fig. 4.6.



(a) (b)

Figure 4.6: Equivalent small-signal model to find the input impedance of the left section for noise analysis. (a) actual model (b) reduced mode using $g_{m,eff}$

This input impedance, $Z_{in,x}$, in Fig. 4.6(b), is derived using KVL as follows

$$\begin{aligned} V_x &= i_x\left(R_F+R_s\right)+V_{on} \\ &= i_x\left(R_F+R_s\right)+\left(i_x-g_{m,eff}\left(V_y-V_x\right)\right)R_L \\ &= i_x\left(R_F+R_s\right)+\left(i_x+g_{m,eff}R_s\right)R_L \\ &= i_x\left(R_F+R_s+R_L+g_{m,eff}R_sR_L\right). \qquad (4.6) \end{aligned}$$

Assuming perfect matching and using (4.12), (4.6) is simplified to

$$V_x=i_x2\left(R_F+R_L\right)+i_xR_s. \qquad (4.7)$$

Hence, the input impedance for the noise analysis is given by

$$Z_{in,x}=\frac{V_x}{i_x}=2\left(R_F+R_L\right)+R_s. \qquad (4.8)$$

The above expression points out that the equivalent input impedance is the source impedance R_s between nodes V_x and V_y, and a series resistance of $2\left(R_F + R_L\right)$ to ground.

R_s represents the source impedance, which appears in series with $2\left(R_F + R_L\right)$. The noise current $i_{n,MN}$ produces an output noise voltage, V_{on}. Then, V_{on} generates a noise voltage at nodes V_x and V_y. These two voltages drive the left section and produce an output noise voltage, V_{op}, which is a fraction of V_{on} ($V_{op} = \beta V_{on},\ \beta < 1$). Due to the cross connection, V_{op} carries the same polarity as V_{on}, and thereby the differential output noise voltage and noise figure are reduced. Similarly the noise generated by M_P is partially canceled. In the conventional case, V_{on} and V_{op} carry different polarities, and therefore the conventional LNA with resistive feedback has higher noise figure.

4.3.2 Performance Parameters

In this subsection, analytical expressions for the input impedance, voltage gain, and noise figure of the proposed LNA are demonstrated.

4.3.2.1 Input/Output Transfer Function

The transfer function of the proposed LNA in Fig 4.3(a), is calculated using the half-circuit small-signal model shown in Fig 4.7. In this model, $C_{gs,n}$ and $C_{gs,p}$ are the gate-source capacitance of the NMOS/PMOS transistors, while C_o and C_s are the output and source parasitic capacitances, respectively. Also, the effect of output conductance of transistors M_N and M_P is neglected for simplicity.

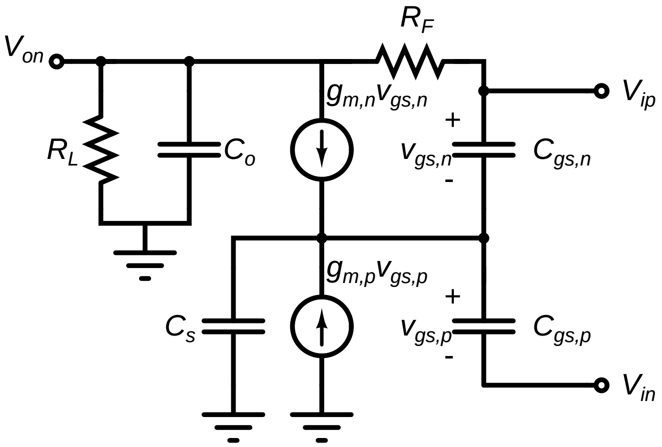


Figure 4.7: Half-circuit small-signal model of the proposed LNA.

Small-signal analysis results in a differential transfer function as follows

$$\begin{aligned} A_v(s) &= \frac{V_{op}-V_{on}}{V_{in}-V_{ip}} = -\frac{A_{v,mid}\cdot(1+s/\omega_z)}{(1+s/\omega_{po})\cdot(1+s/\omega_{ps})} \approx \frac{A_{v,mid}}{1+s/\omega_{po}}, \\ A_{v,mid} &= 2g_{m,eff}\left(R_F//R_L\right), \\ \omega_z &= \frac{2g_{m,p}}{2C_{gs,p}+C_s}, \\ \omega_{po} &= \frac{1}{C_o\cdot(R_F//R_L)}, \\ \omega_{ps} &= \frac{g_{m,n}+g_{m,p}}{C_{gs,p}+C_{gs,n}+C_s}, \end{aligned} \tag{4.9}$$

where $A_{v,mid}$ is the mid-band gain, ω_{po} is the pole at the output, and ω_{ps} and ω_z are due to the parasitic capacitances $C_{gs,n}$, $C_{gs,p}$, and C_s. In case $g_{m,n} = g_{m,p}$ and $C_{gs,p} = C_{gs,n}$, the source voltage of M_N and M_P is AC ground, and hence ω_{ps} and ω_z cancel out each other and are not effective. This is also concluded from (4.9), when $\omega_{ps} = \omega_z$. However in case $g_{m,n} \neq g_{m,p}$, the zero location appears at the lower frequency compared to the non-dominate pole location. Because ω_{ps} and ω_z

appear after the dominate pole, the gain expression effectively has a single pole as demonstrated in (4.9). The above analysis is verified using circuit-level simulation. The results for both the simulation and the analytically evaluated expression in (4.9) are shown in Fig. 4.8. In this simulation, the current through R_L is steered to avoid increasing the supply voltage. In the actual implementation, the load resistance is replaced with a PMOS transistor in a push-pull architecture to provide higher gain. Fig. 4.8 shows that the output pole determines the 3-dB upper cut-off frequency ($A_{v,mid} = 18.4$ dB, $\omega_{po} = 2\pi 3$ G rad/s). In addition, the effect of ω_z and ω_{ps} does not appear up-to 5 GHz. Simulations show their effect starts to appear after 20 GHz in this example.

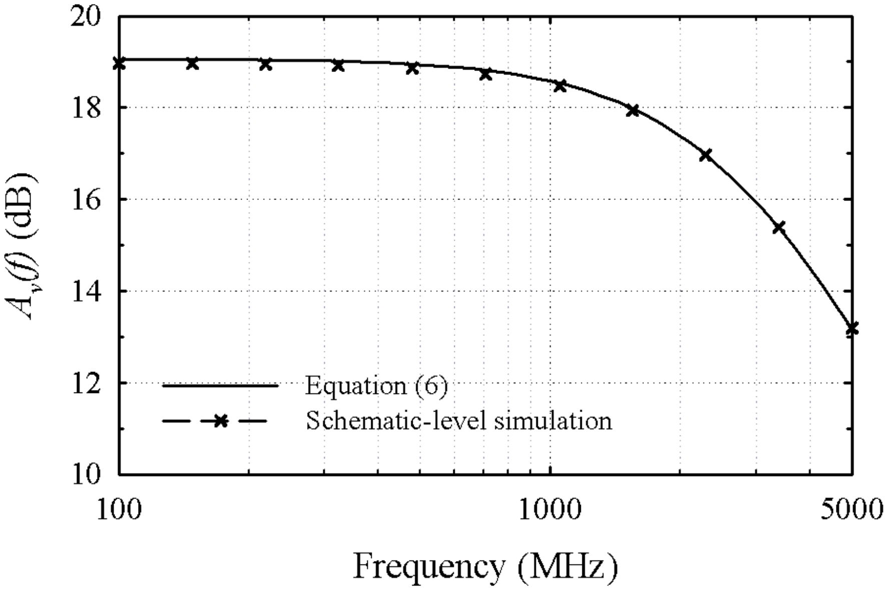


Figure 4.8: Schematic-level simulated frequency response of the proposed LNA versus the analytical expression in (4.9) ($g_{m,n} = 60$ mS, $g_{m,p} = 60$ mS, $R_F = 500\ \Omega$, $R_L = 230\ \Omega$, $C_o = 350$ fF, $C_{gs,n} = 160$ fF, $C_{gs,p} = 380$ fF, $C_s = 150$ fF).

The approximated gain expression in (4.9) is similar to the gain expression of the conventional LNA with resistive feedback given by (4.2), and therefore it has the same gain properties. In addition, the output pole for both the proposed and the conventional LNA is similar with the assumption of having the same C_o. Increasing the gain requires a higher value of $R_F//R_L$, which reduces the upper cut-off frequency of the LNA. This is an indicative of the design trade offs between gain and bandwidth that is also seen in conventional amplifier.

4.3.2.2 Input Impedance

Using the small-signal model in Fig 4.7, the half-circuit input impedance of the proposed LNA is analytically given by

$$\begin{aligned} Z_{in,half}(s) &= \frac{R_F//\frac{1}{sC_{gd,n}}}{1+A_v(s)}//\frac{1}{s\left(C_{gs,n}+C_{gs,p}\right)} \\ &// \frac{g_{m,n}+g_{m,p}+sC_s}{s\left(g_{m,n}-g_{m,p}\right)\left(C_{gs,n}+C_{gs,p}\right)}, \end{aligned} \tag{4.10}$$

where $A_v(s)$ is the gain of the LNA defined in (4.9) considering the dominant pole ω_{po}, and $C_{gd,n}$ is the gate-drain capacitance of NMOS transistor. The input impedance is composed of three parallel impedance as follows: 1) $\frac{R_F//sC_{gd,n}}{1+A_v}$ which is responsible for the input matching, 2) $\frac{1}{s(C_{gs,n}+C_{gs,p})}$ which is due to the finite input capacitance, and 3)$\frac{g_{m,n}+g_{m,p}+sC_s}{s(g_{m,n}-g_{m,p})(C_{gs,n}+C_{gs,p})}$ which appears due to non-equal values of $g_{m,n}$ and $g_{m,p}$. For $g_{m,n}=g_{m,p}$, the source voltage of NMOS/PMOS transistors is a virtual AC-ground, and the input impedance is clearly the parallel combination of the first two terms in (4.10). However in the actual design, it is hard to guarantee similar $g_{m,n}$ and $g_{m,p}$ because of the design or process mismatches, and therefore the third term in (4.10) is effective. In this design, $g_{m,n}$ and $g_{m,p}$ are assumed to be equal, and therefore the third term can be removed as an approximation.

The above analysis is verified using circuit-level simulations and the results are shown in Fig. 4.9. In this plot, the half-circuit input impedance is normalized to $R_s/2$ for both the schematic-level simulated and analytically-evaluated results. The results indicate that initially the input impedance is matched to the source resistance $R_s/2$. Then around 1 GHz the input impedance starts to increase because of the gain reduction. At 3 GHz, $C_{gs,n}$, $C_{gs,p}$ and $C_{gd,n}$ start to be effective and thus the input impedance is reduced.

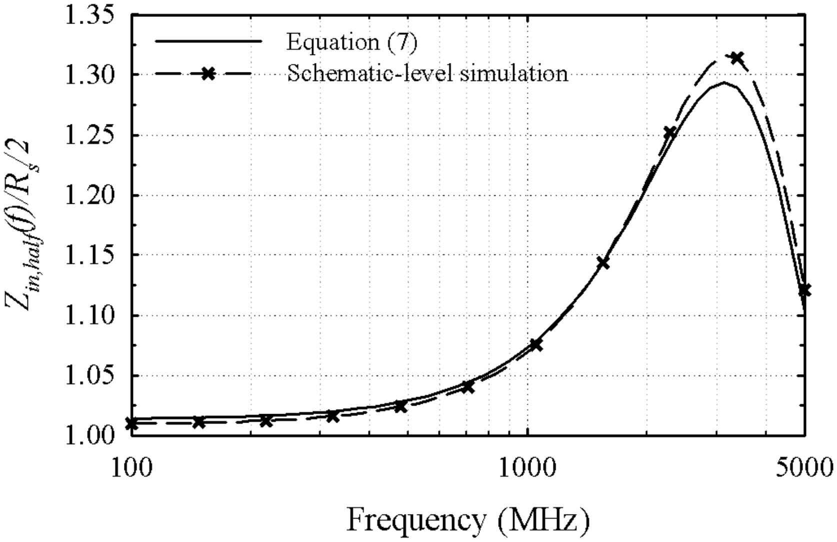


Figure 4.9: Schematic-level simulation of the half-circuit input impedance normalized to $R_s/2$ of the proposed LNA versus the analytical expression in (4.10) ($g_{m,n} = 60$ mS, $g_{m,p} = 60$ mS, $R_F = 500\ \Omega$, $R_L = 230\ \Omega$, $C_o = 350$ fF, $C_{gs,n} = 160$ fF, $C_{gs,p} = 380$ fF, $C_s = 150$ fF, $C_{gd,n} = 50$ fF).

The differential input impedance, $Z_{in}(s) = 2Z_{in,half}(s)$, could be further simplified in terms of poles and zeros using (4.10) as follows

$$Z_{in} = \frac{R_{in,mid} \cdot (1 + s/\omega_{po})}{1 + sR_F\left(C_{gd,n} + \frac{C_{gs,n}+C_{gs,p}}{A_{v,mid}}\right) + s^2\frac{R_F(C_{gs,n}+C_{gs,p})}{A_{v,mid}\omega_{po}}}, \tag{4.11}$$

where

$$R_{in,mid} \quad = \quad 2 \cdot \frac{R_F}{1 + A_{v,mid}} = \frac{1}{g_{m,eff}}\left(1 + \frac{R_F}{R_L}\right) = R_s. \tag{4.12}$$

Eq. (4.12) demonstrates that the mid-band value of the input impedance, $R_{in,mid}$ depends on the value of $g_{m,eff}$ and the ratio of $\frac{R_F}{R_L}$ similar to the conventional LNA defined in (4.1). Changing either of these quantities helps to improve the matching, i.e. $R_{in,mid} = R_s$. As an example, to reduce the value of $R_{in,mid}$ either the value of $g_{m,eff}$ has to increase or the value $\frac{R_F}{R_L}$ has to decrease. Increasing $g_{m,eff}$ leads to a lower noise figure, however, the input capacitance increases leading to a poor matching at higher frequencies, i.e. lower bandwidth. On the other hand, reducing the value of $\frac{R_F}{R_L}$ lowers the gain and hence increases the noise figure. This is the tradeoff between increasing the bandwidth of the input impedance versus having a lower noise figure at higher frequencies.

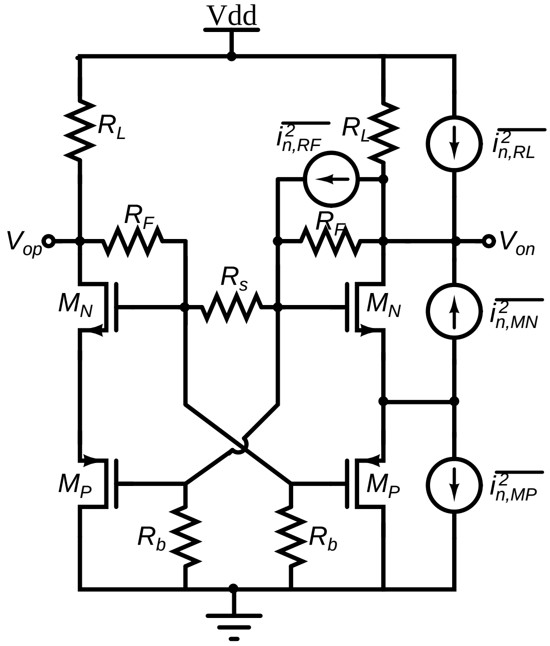


Figure 4.10: Noise sources in the proposed LNA.

4.3.2.3 Noise Figure

The different noise sources affecting the overall noise figure of the LNA are shown in Fig. 4.10, where only the noise contributors of half of the circuit is shown. The effect of the parasitic capacitances will be ignored to simplify the analysis and because noise figure is important in the mid-band of operation. Assuming $R_s << R_F$ and $R_s << R_L$, the resultant output differential noise voltage due to M_N, $\overline{v^2_{ond,M_N}}$, is given by

$$\overline{v^2_{ond,M_N}} = 2. \left(\frac{g_{m,eff}}{g_{m,n}} R_L // R_F \cdot \frac{1}{1 + g_{m,eff} \frac{R_L R_s}{R_L + R_F}} \right)^2 \cdot \overline{i^2_{n,M_N}}, \qquad (4.13)$$

where $\overline{i^2_{n,M_N}}$ is the noise current due to both thermal and flicker noise. The first term is the transimpedance gain for the noise current generated by M_N. The doubling is due to the fact that there are two of each device one on each half circuit. Assuming perfect matching, (4.13) reduces to

$$\overline{v^2_{ond,M_N}} = \frac{1}{2}\cdot\left(\frac{g_{m,eff}}{g_{m,n}}R_L//R_F\right)^2 \cdot \overline{i^2_{n,M_N}}. \tag{4.14}$$

The input-referred voltage noise due to M_N is obtained by dividing (4.14) by $A_{v,mid}$ defined in (4.9)

$$\overline{v^2_{in,M_N}} = \frac{1}{8}\cdot\left(\frac{1}{g_{m,n}}\right)^2 \cdot \overline{i^2_{n,M_N}}. \tag{4.15}$$

The noise current of M_N is due to its thermal and flicker noise voltage. This current is given by

$$\overline{i^2_{n,M_N}} = 4kT\gamma_n g_{m,n}\Delta f + \frac{K_{F,n}I_{DC}}{fC_{ox}L_n^2}\Delta f, \tag{4.16}$$

where k is Boltzmann constant, γ_n and $K_{F,n}$ are the thermal and flicker noise factors, respectively, I_{DC} is the DC current, C_{ox} is the oxide capacitance per unit area, and L_n is the channel length of M_N. Substituting (4.16) in (4.15), the input-referred noise voltage is as follows

$$\overline{v^2_{in,M_N}} = \frac{1}{2}\frac{kT\gamma_n}{g_{m,n}}\Delta f + \frac{K_{F,n}I_{DC}}{8fC_{ox}L_n^2 g_{m,n}^2}\Delta f. \tag{4.17}$$

Similar analysis is applied to the remaining noise contributors of the circuit. The input-referred voltage noise due to M_P is hence given by

$$\overline{v^2_{in,M_P}} = \frac{1}{2}\frac{kT\gamma_p}{g_{m,p}}\Delta f + \frac{K_{F,p}I_{DC}}{8fC_{ox}L_p^2 g_{m,p}^2}\Delta f. \tag{4.18}$$

The input-referred voltages noise due to the thermal noise of R_F and R_L, $\overline{i^2_{n,R_F}} = (4kT/R_F)\Delta f$ and $\overline{i^2_{n,R_L}} = (4kT/R_L)\Delta f$ are as follows

$$\begin{aligned} \overline{v^2_{in,R_F}} &= \frac{1}{2}\left(1+\frac{1}{g_{m,eff}R_s}\right)^2 \frac{R_s^2}{R_F}kT\Delta f, \qquad (4.19) \\ \overline{v^2_{in,R_L}} &= \frac{kT}{2g^2_{m,eff}R_L}\Delta f. \qquad (4.20) \end{aligned}$$

Finally, the total noise figure is obtained by summing the quantities of (4.17), (4.18), (4.19) and (4.20) and then dividing by $kTR_s\Delta f$. $kTR_s\Delta f$ is the noise generated by the source resistance at the input of the LNA. Hence, the total noise figure, NF_{tot} is as follows

$$\begin{aligned} NF_{tot} &= 1 + \frac{\gamma_n/g_{m,n} + \gamma_p/g_{m,p}}{2R_s} + \frac{\left(\frac{K_{F,n}}{g^2_{m,n}L^2_n} + \frac{K_{F,p}}{g^2_{m,p}L^2_p}\right) I_{DC}}{8kTfC_{ox}R_s} \\ &+ \frac{1}{2}\left(1+\frac{1}{g_{m,eff}R_s}\right)^2 \frac{R_s}{R_F} + \frac{1}{2g^2_{m,eff}R_LR_s}. \qquad (4.21) \end{aligned}$$

The above analysis shows that the noise contribution of the NMOS/PMOS transistor is reduced compared to the conventional LNA in (4.3), while the noise contribution of the feedback and load resistances remains the same. Assuming $g_{m,n} = g_{m,p}$ and $\gamma_n = \gamma_p$ for simplicity, the noise contribution (thermal and flicker) of the NMOS/PMOS transistors is reduced by one-half compared to the conventional architecture. A similar conclusion is also reached for the flicker noise. As a result, the lower limit of the noise figure of the low noise amplifier with resistive feedback is reduced using the proposed approach. It is important to mention that this architecture requires higher supply voltage.

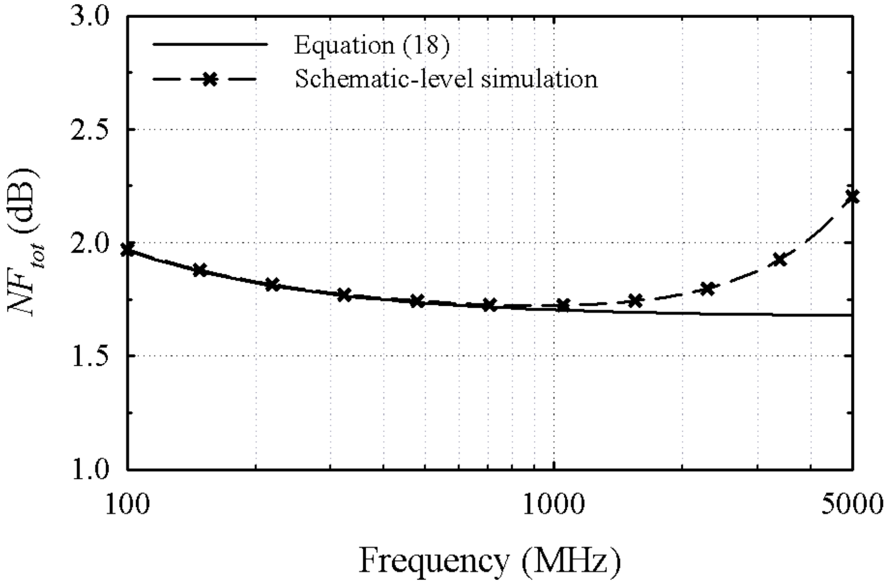


Figure 4.11: Schematic-level simulation of the noise figure of the proposed LNA versus the analytical expression in (4.10) ($g_{m,n} = 60$ mS, $g_{m,p} = 60$ mS, $R_F = 500\ \Omega$, $R_L = 230\ \Omega$, $C_o = 350$ fF, $C_{gs,n} = 160$ fF, $C_{gs,p} = 380$ fF, $C_s = 150$ fF, $C_{gd,n} = 50$ fF, $\gamma_n = 1.6$, $\gamma_p = 1.3$, $K_{F,n} = 4.5 \cdot 10^{-28}$, $K_{F,p} = 1.8 \cdot 10^{-28}$).

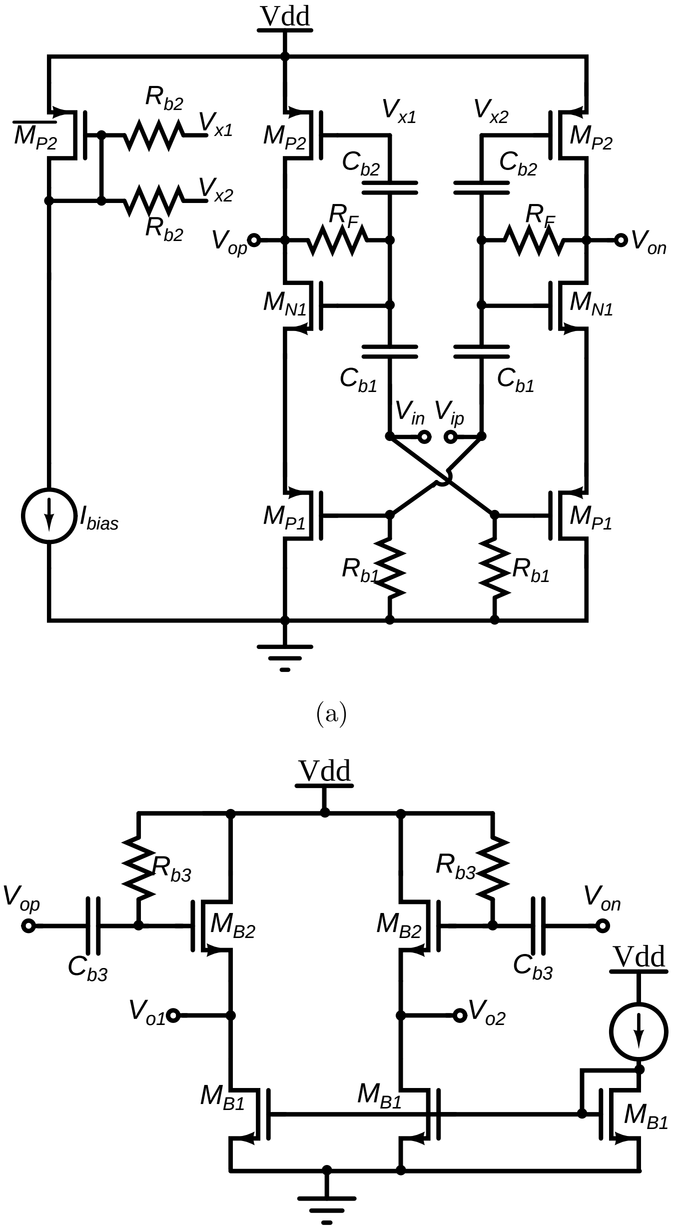
Fig. 4.11 shows the simulated and the analytically-evaluated noise figure of the proposed LNA. At low frequencies, the noise figure increases because of the flicker noise. At higher frequencies, the noise figure starts to increase again because of the finite bandwidth of the LNA, which increases the noise contribution of the feedback resistance. The effect of parasitics was not included in deriving (4.21), and therefore, the analytical expression does not follow the simulated schematic-level results around and above the cut-off frequency. Simulations also show that the noise contribution at higher frequencies (around 1 GHz) is mainly thermal noise due to the NMOS/PMOS transistors and resistances. Schematic-level noise analysis indicates that the noise contribution of the NMOS/PMOS transistors is almost the same as the feedback and load resistances. This result points out that the noise contribution of the transistors is reduced such that they are not the main noise contributors. In this example, the minimum value of NF_{tot} is 1.7 dB. However, in the actual circuit implementation, the noise figure is further reduced by using a push-pull architecture.

4.4 Circuit Implementation

4.4.1 Circuit Description

Fig. 4.12(a) shows the actual implementation of the proposed LNA. In this implementation, the load, R_L, is replaced by a PMOS transistor, M_{P2} forming a push-pull architecture. This transistor serves for two main purposes: (1) to provide the DC current biasing, and (2) to provide an additional gain to increase the overall gain and reduce the noise figure of the LNA. The DC biasing is adjusted with the current source I_{bias}, which is mirrored through the current mirror M_{P2}. This current also determines the gate-source voltages of M_{N1} and M_{P1}, and therefore no additional DC biasing circuit is required. The DC voltage of the output node is determined from the gate-source voltages of M_{P1} and M_{N1}, i.e. $V_{on,DC} = V_{op,DC} = V_{SG,M_{P1}} + V_{GS,M_{N1}}$. The gate of M_{P1} is biased to ground through the resistance R_{b1}, which is much higher than the value of the source resistance, R_s.

Transistor M_{P2} also provides an additional transconductance to increase the overall gain of the LNA. Increasing the overall gain helps to reduce the noise contribution of the load and feedback resistances, and therefore lowering the overall noise figure. With the additional M_{P2} transistor, the voltage gain, input impedance, and noise



(a)

(b)

Figure 4.12: Complete schematic of (a) the proposed broadband LNA demonstrating the biasing circuit, and (b) the buffer ($V_{DD} = 1.8$ V).

figure are modified as follows

$$\begin{aligned}
A_{v,mid} &= \left(2g_{m,eff} + g_{m,M_{P2}}\right)\left(R_F//R_L\right), && (4.22)\\
Z_{in,mid} &= \frac{2R_F}{1+A_{v,mid}} \simeq \frac{2}{2g_{m,eff}+g_{m,M_{P2}}}\left(1+\frac{R_F}{R_L}\right), && (4.23)\\
NF_{mid} &= 1+\frac{2\gamma_n g_{m,eff}^2}{g_{m,n}R_s\left(2g_{m,eff}+g_{m,Mp2}\right)^2}+\frac{2\gamma_p g_{m,eff}^2}{g_{m,p}R_s\left(2g_{m,eff}+g_{m,Mp2}\right)^2}\\
&+ \frac{\gamma_p g_{m,Mp2}}{R_s\left(2g_{m,eff}+g_{m,Mp2}\right)^2}+\frac{R_s^2}{2R_F}\left(1+\frac{2}{\left(2g_{m,eff}+g_{m,Mp2}\right)R_s}\right)^2 && (4.24)
\end{aligned}$$

where $g_{m,M_{P2}}$ is the transconductance of M_{P2}. It is important to mention that adding another composite transistor as the load helps in reducing the NF more, however it requires a higher supply voltage.

The capacitors C_{b1} and C_{b2} are added to isolate the DC biasing of each gate of the transistors. These capacitors and the resistors R_{b1} and R_{b2} limit the lower cut-off frequency of the amplifier. The lower cut-off frequency can be estimated by expressing the output current at the lower frequencies as follows ($C_{b1} = C_{b2} = C_b$ and $R_{b1} = R_{b2} = R_b$)

$$i_{o,ac} = \left(2g_{m,eff} + g_{m,M_{P2}}\right)\cdot V_{in}\cdot\frac{\frac{g_{m,eff}}{2g_{m,eff}+g_{m,M_{P2}}}+sR_bC_b}{1+sR_bC_b}. \tag{4.25}$$

Finally, the lower cut-off frequency can be analytically calculated using (4.25) to find the 3-dB cut-off frequency. The resultant 3-dB lower cut-off frequency is

$$\omega_L = \frac{1}{R_bC_b}\cdot\sqrt{1-2\left(\frac{g_{m,eff}}{2g_{m,eff}+g_{m,Mp2}}\right)^2}. \tag{4.26}$$

In this implementation, the lower cut-off frequency is adjusted around 2 MHz. Widths of the transistors are increased by using maximum number of fingers to reduce the required current to achieve a specific $g_{m,eff}$. The upper value for widths of the transistors is limited by the required upper cut-off frequency around 2.4 GHz. In addition, increasing the transistor width helps to reduce the flicker noise and required headroom. On the other hand, width per finger is minimized to reduce the effective series gate resistance resulting in higher gain and lower noise figure. A buffer is designed to drive the 50 Ω load impedance. Fig. 4.12(b) shows the schematic of the buffer. Table 4.1 shows the circuit element values and transistor aspect ratios for the proposed LNA and buffer.

Table 4.1: Circuit element values and transistor aspect ratios for the implemented LNA and buffer

$(\frac{W}{L})_{M_{N1}}$	$(\frac{W}{L})_{M_{P1}}$	$(\frac{W}{L})_{M_{P2}}$	R_F	C_c	R_b
$\frac{170\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{465\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{152\ \mu\text{m}}{0.1\ \mu\text{m}}$	780 Ω	7.8 pF	100 kΩ
$(\frac{W}{L})_{M_{B1}}$	$(\frac{W}{L})_{M_{B2}}$	C_{b3}	R_{b3}	$I_{bias,B}$	I_{bias}
$\frac{330\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{80\ \mu\text{m}}{0.1\ \mu\text{m}}$	7.8 pF	13.9 kΩ	9.5 mA	5 mA

4.4.2 Sizing the Composite Transistor

The composite NMOS/PMOS transistors are sized in a way to maximize the bandwidth. In this subsection, a design methodology is presented to find the optimum width of the NMOS and PMOS transistor. The input capacitance of the LNA is proportional to the gate-source capacitance and hence the width and length of the input devices. The input capacitance, C_{in}, is written as

$$C_{in} = W_n L_n C_{ox} + W_p L_p C_{ox} = (W_n + W_p)\, L C_{ox}, \tag{4.27}$$

where W_n, W_p and $L_n = L_p = L$ are the channel width and length of the NMOS and PMOS transistors, respectively. C_{ox} is the oxide capacitance per unit area. Eq. (4.27) indicated that the input capacitance depends on $W_n + W_p$. Reducing this quantity maximizes the bandwidth of the amplifier. The value of the required effective transconductance determines both values. The inverse of the transconductance for long and short channel device approximation is given by

$$\frac{1}{g_{m,eff}} = \frac{1}{g_{m,n}} + \frac{1}{g_{m,p}} = \begin{cases} \sqrt{\frac{L}{2W_n C_{ox}\mu_n I_{DC}}} + \sqrt{\frac{L}{2W_p C_{ox}\mu_p I_{DC}}}, & \text{long channel} \\ W_n v_{sat,n} C_{ox} + W_p v_{sat,p} C_{ox}, & \text{short channel} \end{cases} \tag{4.28}$$

where v_{sat} is the velocity saturation constant. Eqs. (4.27) and (4.28) are used along with a constrained optimization algorithm to find the optimum value of W_n and W_p. This optimization problem is defined as following

$$\begin{aligned} \text{minimize:} \quad & C_{in}(W_n, W_p) \propto W_n + W_p \\ \text{given:} \quad & \frac{1}{g_{m,eff}(W_n, W_p)} = \text{constant.} \end{aligned} \tag{4.29}$$

The constrained optimization in (4.29) is solved analytically using Lagrange Multipliers resulting in the following design requirement for the ratio W_n/W_p

$$\frac{W_n}{W_p} = \begin{cases} \left(\frac{\mu_p}{\mu_n}\right)^{1/3}, & \text{long channel} \\ \left(\frac{v_{sat,p}}{v_{sat,n}}\right)^{1/2}, & \text{short channel} \end{cases} \tag{4.30}$$

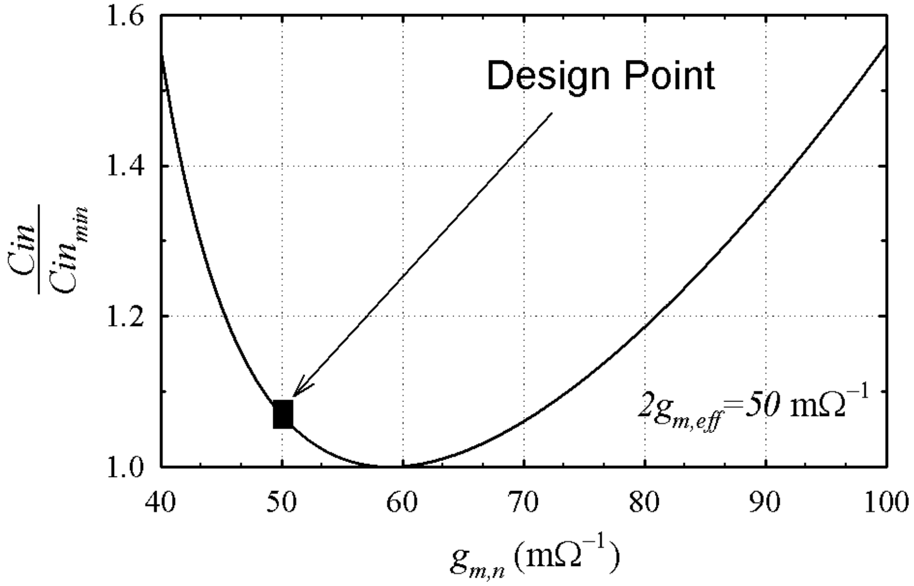


Figure 4.13: Input capacitance normalized to its minimum value versus $g_{m,n}$ for $2g_{m,eff} = 50\ mS$.

Fig. 4.13 shows the input capacitance normalized to its minimum value versus a sweep of $g_{m,n}$ for a constant $g_{m,eff} = 25\ mS$ using (4.27). As depicted, there is an optimum value for both $g_{m,n}$ and $g_{m,p}$ to minimize the input capacitance. In this design, the optimum value of $g_{m,n}$ is around 59 mS. In the actual implementation, $g_{m,n}$ and $g_{m,p}$ are designed for 50 mS each, which reduces the input bandwidth by 4%.

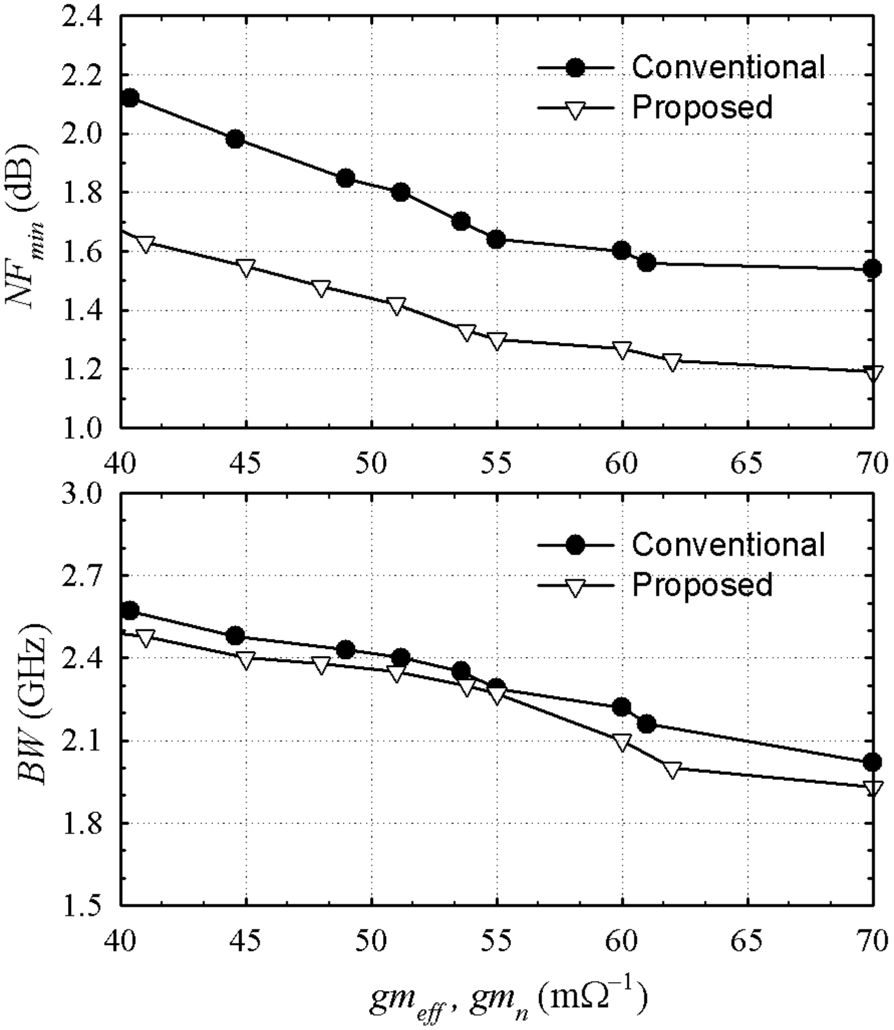


Figure 4.14: Minimum NF (top) and bandwidth (bottom) versus the transconductance value of proposed and conventional LNAs ($I_{bias} = 5\ mA$/half circuit).

4.4.3 Comparison with Conventional LNA

In this subsection, a comparison of the proposed LNA with the conventional one is demonstrated through schematic-level simulations. In both topologies, the push-pull architecture is employed. In addition, the biasing current is fixed to 10 mA (5 mA in each half circuit). Fig. 4.14 shows the simulated minimum noise figure versus the value of $g_{m,eff}$ and $g_{m,n}$ for the proposed and conventional LNA, respectively. As depicted, for the same transconductance the proposed LNA achieves a lower noise figure compared to the conventional one. There is a difference of 0.3 to 0.5 dB in the noise figure. For example, with a transconductance of 55 mS the proposed LNA achieves a minimum noise figure of 1.3 dB versus 1.65 dB for the conventional case.

Increasing the transconductance of the conventional LNA helps to reduce its minimum noise figure. However, the minimum is limited to 1.52 dB for the same current consumption of 10 mA. This is because increasing the transconductance requires the increase of the width of the input device, which increases the input capacitance, and hence reduces the bandwidth. This is clarified through schematic-level simulation of the bandwidth versus the transconductance value in Fig 4.14. For the same transconductance, both amplifier have the same bandwidth because the bandwidth is limited by the output pole in this example. However to design for the same noise figure and current consumption, the transconductance of the conventional architecture has to be higher than the proposed one, leading to a lower bandwidth. As a result, the proposed LNA provides the minimum noise figure for the same bandwidth. In addition, its lower limit for the noise figure is lower than the conventional one making it suitable for designing a broadband LNA with sub 1.5 dB of minimum noise figure.

The linearity of the proposed LNA is slightly lower than the conventional one. This is due to the higher supply voltage requirement. Also, the proposed LNA does not have an inherent non-linearity cancellation similar to the noise. Schematic-level simulations show that for a gain of 20 dB the conventional architecture achieves an IIP3 of 0.5 dBm, while the proposed one achieves an IIP3 of -1 dBm. Increasing the linearity requires increasing the supply voltage, which results in higher power consumption.

4.5 Simulation and Experimental Results

The broadband LNA is fabricated using 90 nm CMOS technology provided by IBM. The die microphotograph is shown in Fig. 4.15, where the area of the LNA core is 0.2×0.3 mm^2. Two measurement setups are used for estimating the performance of the LNA. The first setup uses on-wafer probing. In this setup, the input and output signals are applied using a G-S-G-S-G differential probe, and the DC signals are applied using an 8-pin DC-probe. This measurement setup is used to extract the performance of the LNA without the effect of external components. It provides a comparison with the existing reported broadband LNAs that use on-wafer probing in their measurements. In the second measurement setup, the LNA is encapsulated in a micro leadframe (MLP) package, where the input/output signals are applied/monitored using an FR-4 printed circuit board (PCB). In the case of MLP package, the RF and DC signals are applied from a PCB-board. This measurement setup is used to evaluate the performance of the LNA including the PCB traces and packaging effect.

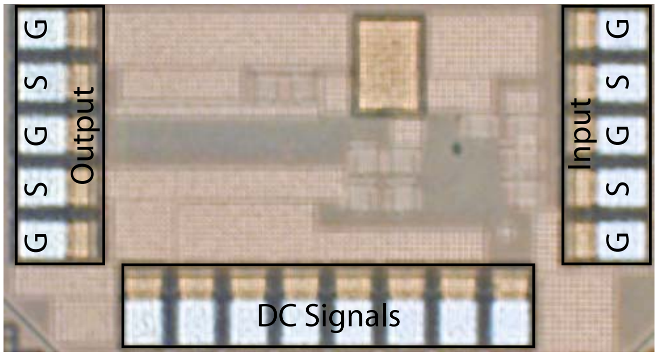


Figure 4.15: Die-photo of the proposed LNA.

Figs. 4.16 and 4.17 show the measured and simulated S_{11} for both measurement setups. In case of the on-wafer measurement, S_{11} is lower than -10 dB up to 1.6 GHz, while it reduces to 1.1 GHz in the case of packaged model. The reducing in the bandwidth in the packaged model is due to the increase of input capacitance because of the PCB traces. Better design of the PCB could lead to a better performance.

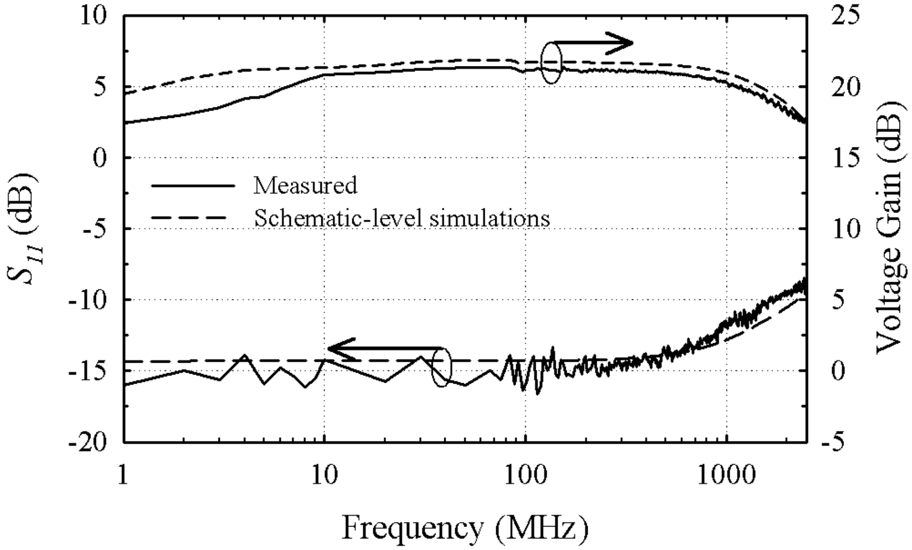


Figure 4.16: Measured and simulated S_{11} and voltage gains for the on-wafer prototype.

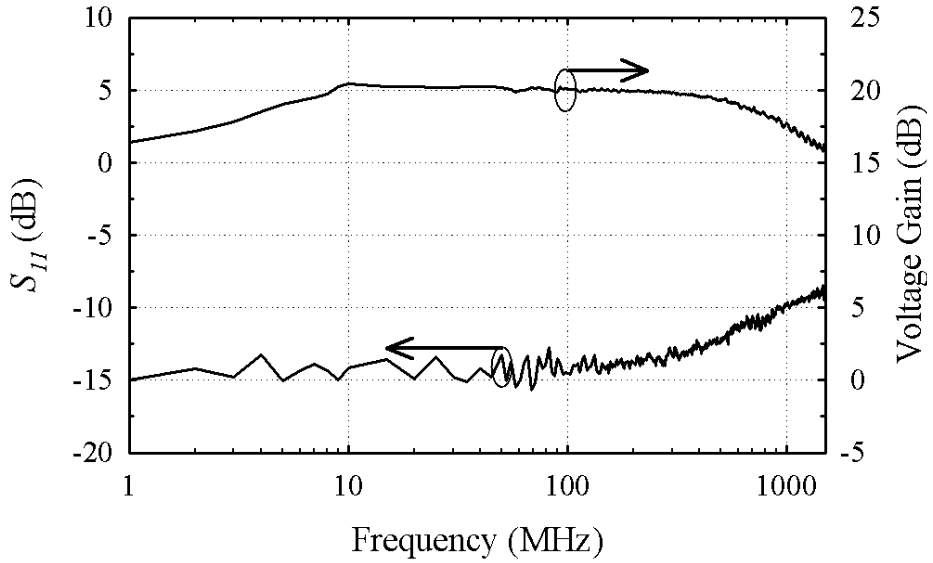


Figure 4.17: Measured S_{11} and voltage gain for the packaged prototype.

The measured and simulated voltage gains after de-embedding the buffer effect are also shown in Figs. 4.16 and 4.17. A mid-band gain of 21 and 20 dB is measured for the on-wafer and packaged LNAs, respectively. The 1 dB difference in the mid-band gain is due to the extra losses introduced by the traces at the output of LNA. The lower cut-off frequency is 2 MHz, while the upper cut-off frequency is 2.3 GHz and 1.1 GHz for the on-wafer and packaged LNAs, respectively. The difference in the upper cut-off frequency is due to the extra capacitance at the input and output of the packaged prototype. The difference in the lower cut-off frequency could be due to the lower cut-off frequency of the balun used in the measurement. The buffer drives the 50 Ω impedance of network analyzer. A measured S_{22} better than -13 dB across the band of interest is obtained as shown in Figs. 4.18 and 4.19. The measured reverse isolation, S_{12}, is lower than -30 dB for both cases.

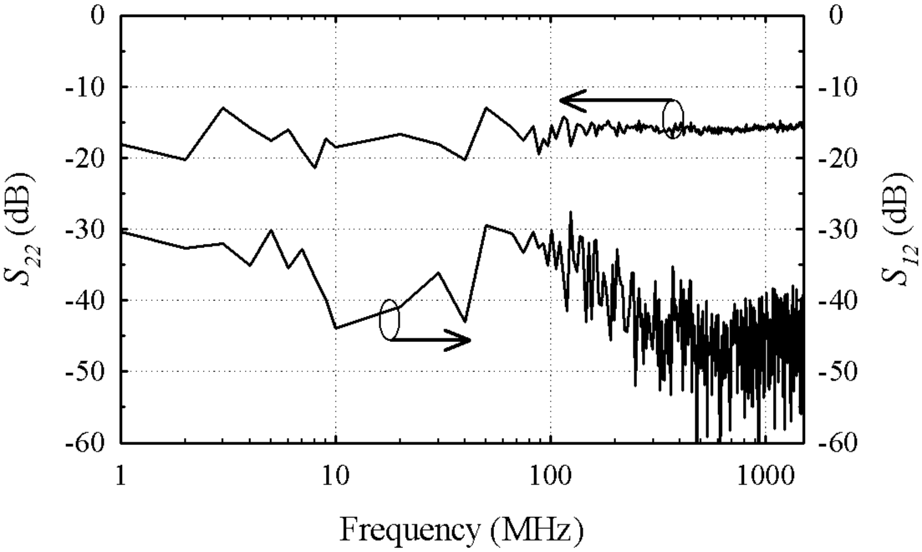


Figure 4.18: Measured S_{22} and reverse isolation (S_{12}) for the on-wafer prototype.

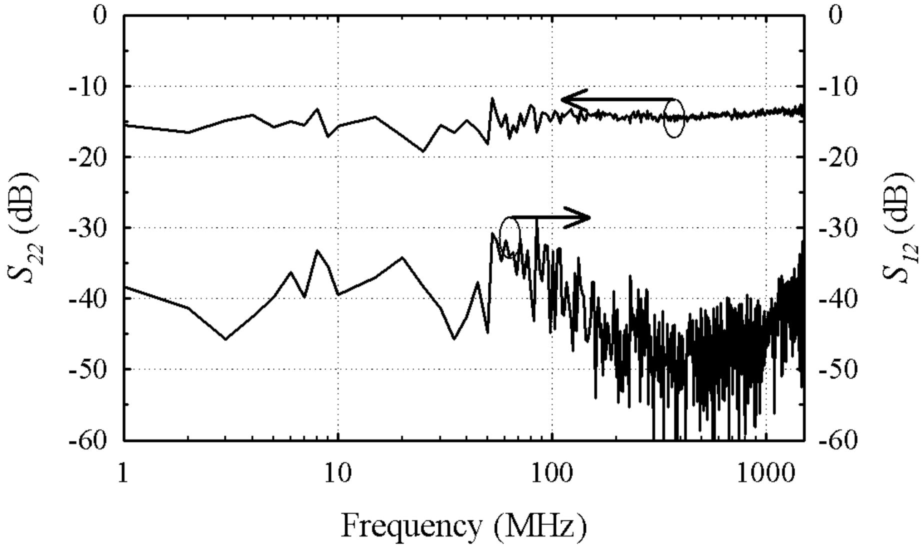


Figure 4.19: Measured S_{22} and reverse isolation (S_{12}) for the packaged prototype.

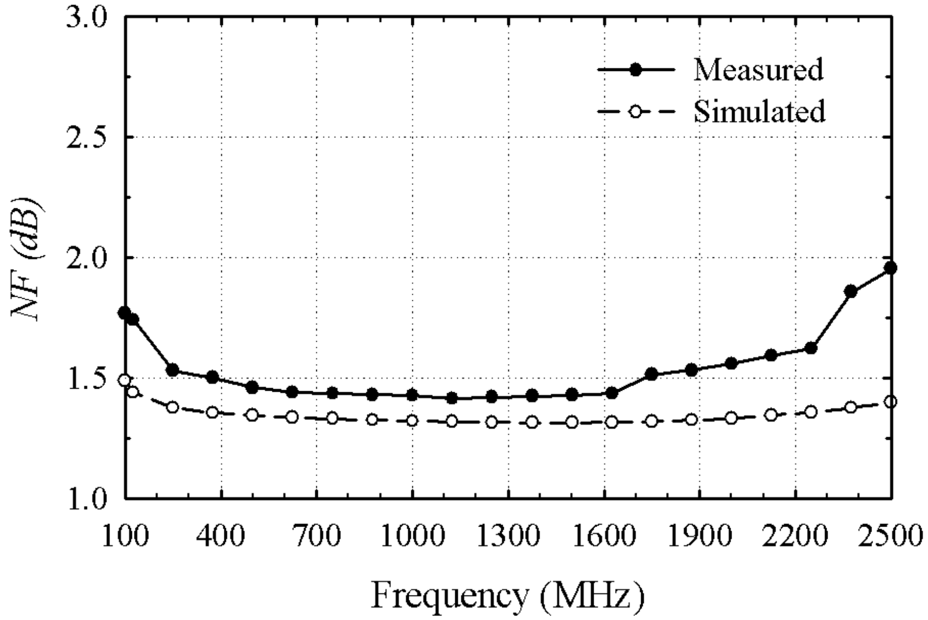


Figure 4.20: Measured and simulated noise figures versus the operating frequency for the on-wafer prototype.

The measured and simulated noise figures versus the operating frequency for the on-wafer prototype are shown in Fig. 4.20. The excess noise due to the buffer is de-embedded from measurements by measuring its output noise when the LNA is switched off. This excess noise is then subtracted from the total output noise of LNA+Buffer. The noise figure of the LNA reaches a minimum value of 1.4 dB. Around 1.6 GHz the noise figure starts to increase reaching a maximum value of 1.7 dB at 2.3 GHz, which is the upper cut-off frequency of the proposed LNA. At 100 MHz, the noise figure is 1.75 dB. For the packaged prototype, the noise figure also reaches a minimum value at 900 MHz. Below this frequency, the noise figure increases because of the flicker noise reaching 1.9 dB at 100 MHz as shown in Fig. 4.21. Above 900 MHz the noise increases because of the bandwidth of the LNA that is limited by the package parasitics. These measurements show that the proposed LNA achieves an almost constant noise figure from 100 MHz up to its upper cut-off frequency. This property does not exist in many existing broadband LNAs, which achieve a minimum noise figure at a specific frequency and have a much higher noise figure across the entire frequency range.

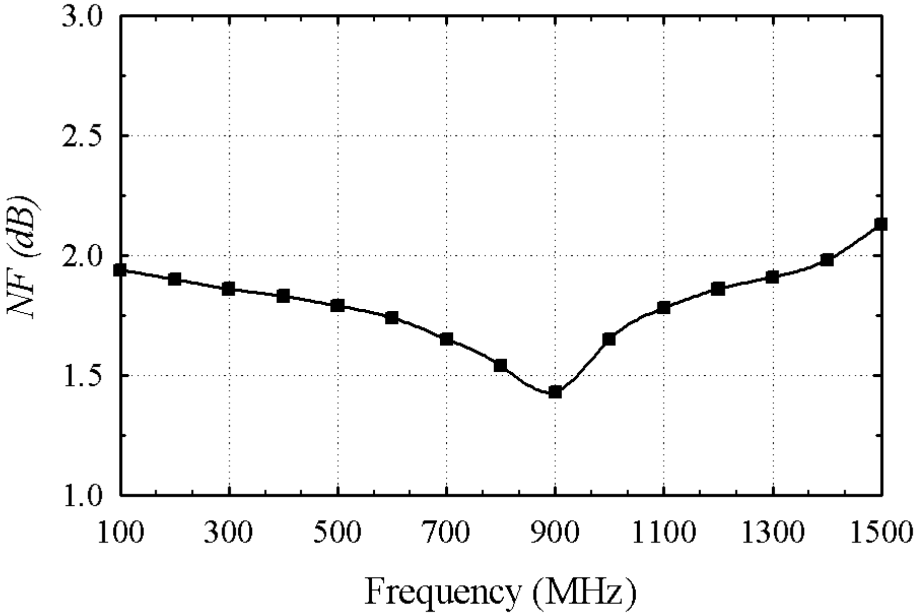


Figure 4.21: Measured noise figure versus the operating frequency for the packaged prototype.

A two-tone IIP3 measurement is performed for the LNA and the result is shown in Fig. 4.22 and Fig. 4.23 for the on-wafer and packaged prototypes, respectively. The two tones are applied with the same amplitude and a frequency offset of 1 MHz. A measured IIP3 higher than -1.5 dBm is obtained for both the prototypes.

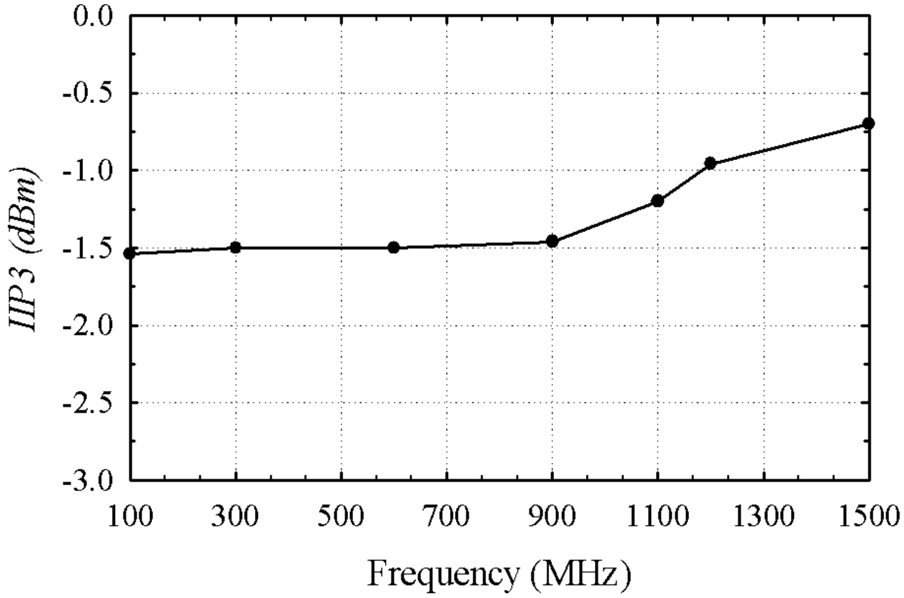


Figure 4.22: Measured $IIP3$ versus the frequency for the on-wafer prototype.

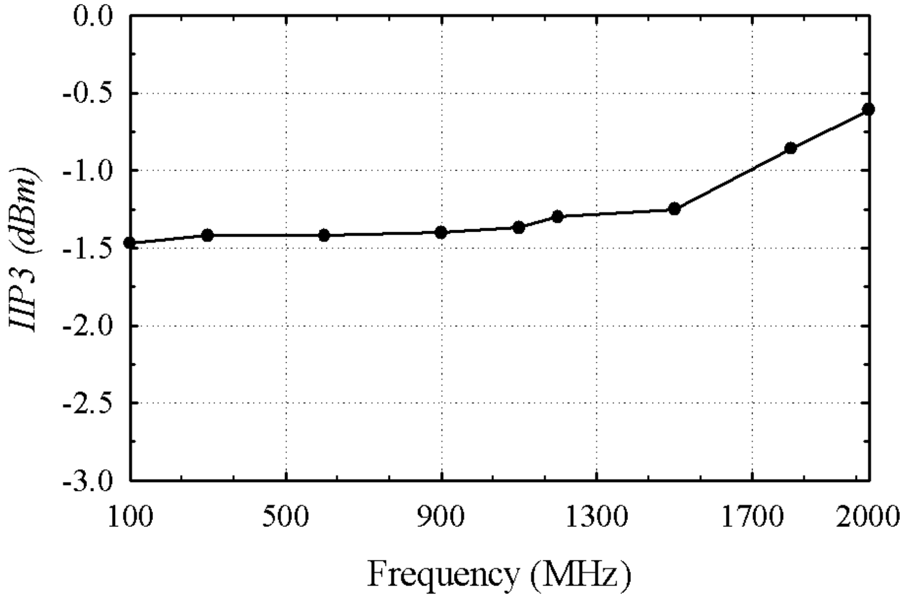


Figure 4.23: Measured $IIP3$ versus the frequency for the packaged prototype.

Table 4.2: Performance summary of the proposed broadband LNA and comparison with the existing work

Ref.	Gain (dB)	Freq. Range (GHz)	NF_{min} (dB)	NF@100 MHz (dB)	IIP3 (dBm)	P_{DC} (mW)	A.Area (mm^2)	Tech CMOS	Package	Topology
[68]	13.7	0.002-1.6	1.9	2.4(a)	0	35	0.075	0.25 μm	On-Wafer	Single-Ended
[69]	25	up to 5.5 GHz	2	>4.5	<-6	38	0.03	90 nm	On-Wafer	Single-Ended
[70]	24	0.5-7	2	N.A.	-6.7	42	0.013	90 nm	On-Wafer	Single-Ended
[71]	12.5(b)	0.1-1.6(a)	2.5	>4.5	16	11.6	0.1	0.13 μm	On-Wafer	Single-Ended
[72]	17.4	0-6	2.5	>2.6(a)	-8	9.8	0.002	90 nm	On-Wafer	Single-Ended
[73]	16	0.4-1	3.5	N.A.	-8	9.8	0.002	90 nm	N.A.	Single-Ended
[74]	17	1-7	2.4	N.A.	-17	16.8	0.07	90 nm	Chip-on-Board	Differential
[75]	15.6	0.2-5.2	3	N.A.	0	14	0.01	65 nm	Chip-on-Board	Differential
[76]	16	0.1-8	3.4	>6	-9	16	0.034	90 nm	Chip-on-Board	Differential
[77]	21	0.3-0.92	2	N.A.	-3.2	3.6	0.33	0.18 μm	N.A.	Differential
[78]	16.5	1-10	3.9	N.A.	-5	36	0.021	65 m	Chip-on-Board	Differential
This work	20	0.002-1.1	1.43	1.9	-1.5	18	0.06	90 nm	MLP	Differential
This work	21	0.002-2.3	1.4	1.7	-1.5	18	0.06	90 nm	On-Wafer	Differential

[a] Estimated from data provided in the corresponding papers.

[b] Power Gain.

The LNA, excluding the output buffer, consumes 10 mA from 1.8V supply. The performance of the proposed LNA and comparison with existing state-of-the-art inductor-less broadband LNAs around the same frequency range are summarized in Table 4.2. As depicted in the table, the proposed broadband LNA with composite NMOS/PMOS transistors provides the minimum noise figure, and has less variations across 100 MHz to the upper cut-off frequency when compared to the state-of-the-art architectures.

4.6 Summary

A broadband LNA employing a new noise-cancelling technique is proposed in this section. The LNA relies on a composite NMOS/PMOS transistor pair for implementing the noise cancellation. The theory shows that the proposed approach reduces the lower limit of the conventional LNA with resistive feedback, allowing for a noise figure below 1.5 dB. Also, optimum sizing of the composite transistors was demonstrated. On-wafer measurements of a fabricated prototype using 90 nm CMOS technology show a voltage gain of 21 dB with a 3-dB bandwidth of 2.3 GHz. A minimum noise figure of 1.4 dB and an IIP3 of -1.5 dBm are also measured. The measured noise figure is lower than the best reported noise figure by 0.5 dB. In addition, measurements of a packaged prototype was also presented. The LNA consumes 18 mW from a 1.8 V supply.

5. A CMOS DISTRIBUTED AMPLIFIER WITH EXTENDED FLAT BANDWIDTH AND IMPROVED INPUT MATCHING USING GATE-LINE WITH COUPLED INDUCTORS

5.1 Introduction

With increasing interest on commercial wideband integrated systems such as radars, wireless ultra-wideband (UWB) and optical receivers, there is a demand for wideband CMOS amplifiers in the front-end section of such systems. Distributed amplification is one of the well-known methods to provide such performance by absorbing the parasitic capacitances of parallel gain stages into an artificial transmission line which in return guarantees the gain uniformity and input/output matching within the bandwidth of operation[79].

Various distributed amplifiers have been reported in 0.18 μm CMOS process recently. Liu et al. [80], [81] presented distributed amplifiers with 1-dB bandwidth of 14 and 22 GHz, respectively. The reported amplifiers with cascode gain stages suffer from high power consumption and considerable input mismatch. Shigematsu et al. [82], employed resistive source degeneration technique for common source gain stages to achieve a 1-dB bandwidth of 39 GHz. Although this technique improves the bandwidth enormously, it results in low gain, high power consumption and high input mismatch. Tsai et al. [83] implemented distributed amplifiers with cascaded gain stages to achieve high gain-bandwidth product, but the amplifier consumes a huge amount of power and the input matching is poor. High power consumption and poor input matching have been the important drawbacks of the reported amplifiers,

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because bandwidth extension has been traditionally achieved by reducing the loading capacitance of the gate-line provided by the single-stage amplifier. Therefore, to achieve similar gain performance, the power consumption of the amplifier has been increased. Also, due to non-uniform loading of the gate-line, the input matching has been degraded, especially at higher frequencies. The non-uniform loading appears because of frequency dependency of the gate-line capacitance which comes from the Miller effect of the gain stage.

The proposed 3-stage distributed low noise amplifier (DLNA) in [84] used standard cascode gain stages, and the power consumption and noise figure are considerably reduced by optimizing the bias point of the amplifiers ($P_{DC} \sim 9$ mW), but the achieved 1-dB bandwidth is only around 6.2 GHz. To increase the gain-bandwidth product while keeping the power consumption low, the distributed amplifiers in [85] employed a three-stage amplifier with cascode gain cells with series-peaking inductor and achieved a 1-dB bandwidth of 11 GHz with a power consumption of 21.6 mW. The advantage of peaking inductor is to increase the gain-bandwidth product of the gain stage without increasing the power consumption. On the other hand, the gain peaking does not allow maximum flat bandwidth extension. It also changes the input Miller capacitance of the gain-stage at higher frequencies which degrades the uniformity of the gate-line and limits the input matching of the amplifier. The proposed amplifier in [86] employs inductive peaking with the stagger-tuning technique to achieve bandwidth enhancement with gain flatness. Since the gain cells are replaced by cascaded stages to boost the gain, the total power consumption of the amplifier is considerably high ($P_{DC} \sim 260$ mW). Also, the input matching of the amplifier is degraded at high frequencies close to cut-off due to non-uniform loading of the gate-line caused by the Miller capacitance. The proposed weighted amplifier in [87] employs coupled inductors in both gate- and drain-lines to minimize the size of the amplifier and also allows the transconductance of different stages to be different to optimize the noise figure of the amplifier with an added degree of freedom.

This section presents a CMOS distributed amplifier which takes advantage of gate-line with coupled inductors in conjunction with cascode gain stages with series-peaking inductors employed in [85]. This approach provides bandwidth extension with flat gain response and improves the input matching of the amplifier simultaneously without any additional power consumption. The section is organized as follows: In Subsection 5.2, the proposed amplifier architecture is demonstrated and a design methodology for flat bandwidth extension and input matching improvement is proposed. Circuit design and implementation are discussed in Subsection 5.3, and the simulation and measurement results are presented in Subsection 5.4. Finally, Subsection 5.5 summarized and concludes the presented work.

5.2 Distributed Amplifier Architecture

5.2.1 Background

Fig. 5.1(a) shows a conventional distributed amplifier with artificial transmission lines and g_m-cells where L_g, C_g and L_d, C_d are gate-line and drain-line inductors and capacitors, respectively. In order to guarantee a constructive addition of forward path currents at the bandwidth of operation, the signals should be in phase at the output of each g_m-cell ($\Delta\theta_g = \Delta\theta_d$ or $\sqrt{L_g C_g} = \sqrt{L_d C_d}$). For proper input/output matching, the characteristic impedance of gate/drain lines and the termination impedance, Z_0, should be the same ($\sqrt{L_g/C_g} = \sqrt{L_d/C_d} = Z_0$).

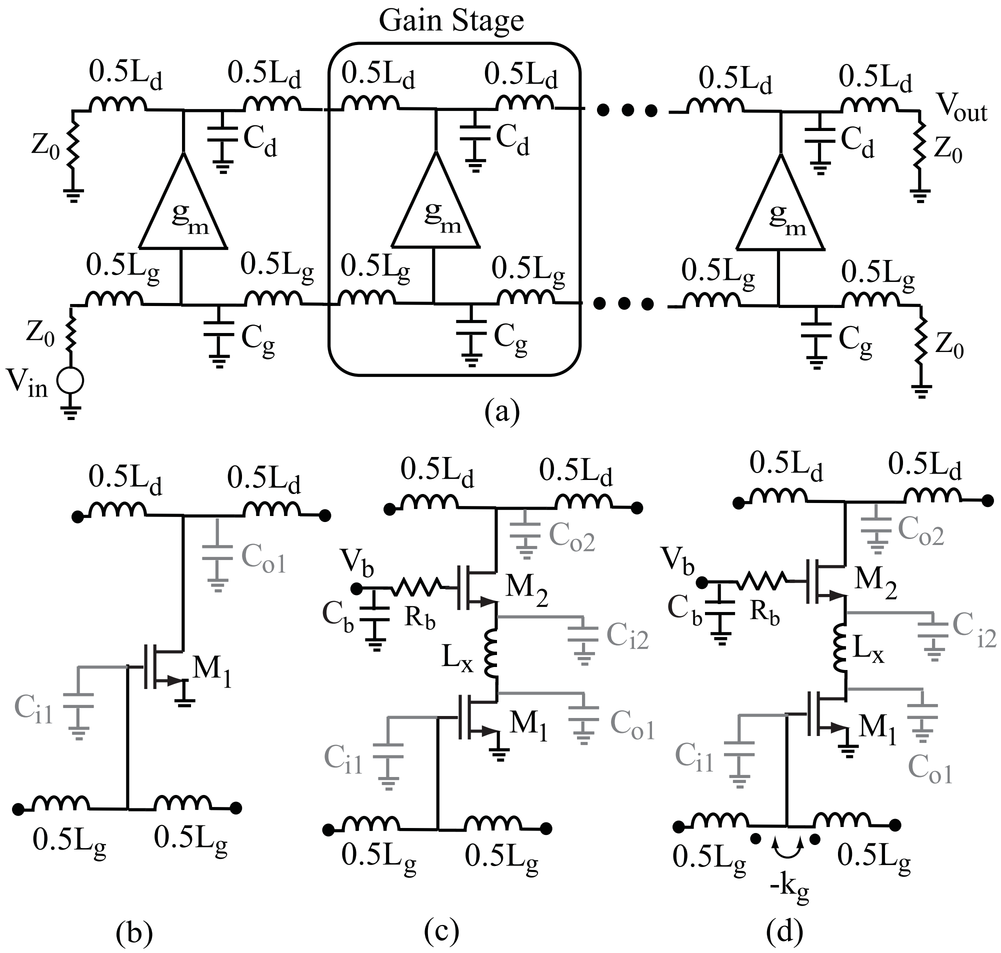

Figure 5.1: (a) A conventional distributed amplifier with artificial transmission lines and g_m-cells, (b) common-source gain stage, (c) cascode gain stage with series-peaking inductor, L_x, and, (d) the proposed gain stage with coupled inductors in gate-line.

As a result, $L_g = L_d$ and $C_g = C_d$ in an ideal amplifier. The cut-off frequencies of the emulated transmission lines are given by [79]

$$f_g = \frac{1}{\pi\sqrt{L_g C_g}} \equiv f_d = \frac{1}{\pi\sqrt{L_d C_d}} \tag{5.1}$$

Usually C_g is limited by the input capacitance of the g_m-cell which means the bandwidth of the distributed amplifier can be optimized by optimizing C_g while keeping g_m large enough to provide the required gain. Therefore, $C_g > C_d$ in practice and an additional output parallel capacitance is needed to increase C_d to be the same as C_g. Fig. 5.1(b) shows a common-source gain stage. The main drawback of this structure is the Miller capacitance at the gate of each gain stage which results in bandwidth reduction. To avoid this issue, a cascode stage can be used (Fig. 5.1(c) where $L_x = 0$). The cascode bandwidth is primarily limited by the pole associated to the internal node of the cascode cells whose value is $P_{cascode} = g_{m2}/(C_{o1}+C_{i2})$, where C_{o1} is the output capacitance of M_1, C_{i2} is the input capacitance of M_2, and g_{m2} is the transconductance of M_2. To suppress the cascode stage dominant pole at higher frequencies, a bandwidth-enhancing inductor (L_x in Fig. 5.1(c)) is added to the amplifier [85]. This compensation method results in high frequency gain peaking at the drain of M_1 if bandwidth extension without power consumption penalty is desired [86]. To see how much power consumption improvement is achieved by employing L_x in the cascode topology, the cascode stage in Fig. 5.1(c) is simulated with and without L_x. The simulation is performed for a gain of 4 dB ($g_{m1} = g_{m2} = 31$ mS) and the same 3-dB bandwidths using 0.18 μm CMOS process design kit using Cadence. The value of L_x is adjusted for a gain peaking of 1.24 dB for maximum bandwidth extension. Fig. 5.2 shows the simulated power consumption vs. bandwidth for a cascode stage with and without L_x. For a bandwidth of 16 GHz, a power consumption improvement factor of 1.8 is achieved. Employing L_x allows increasing the transistor size to achieve the same transconductance with lower power consumption for the same bandwidth.

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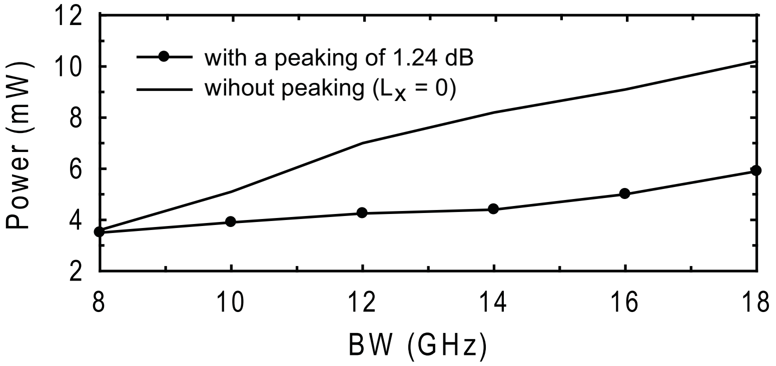

Figure 5.2: The simulated power consumption vs. 3-dB bandwidth for a cascode gain stage with and without L_x for a gain of 4 dB. The value of L_x is adjusted for a gain peaking of 1.24 dB.

This gain peaking does not allow flat bandwidth extension. It also changes the input Miller capacitance of M_1 at higher frequencies which degrades the uniformity of the gate-line and hence the input matching of the amplifier. The proposed gain stage in Fig. 5.1(d) extends the maximum flat bandwidth and improves the input matching simultaneously by introducing mutual coupling with a coefficient of k_g between two adjacent gate inductors as discussed later in this subsection.

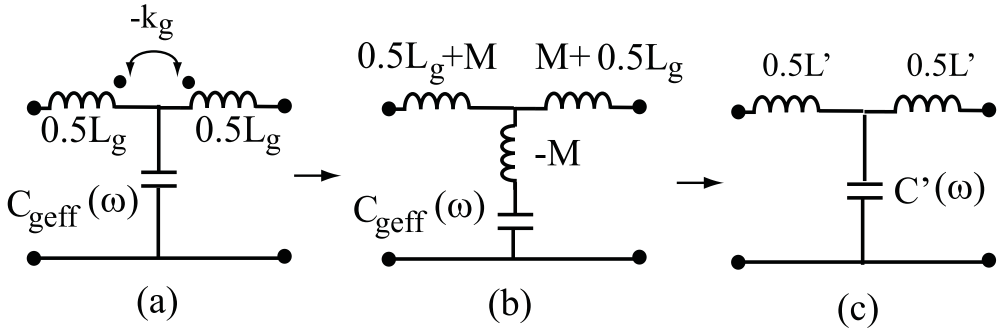

Figure 5.3: The equivalent circuit of the gate-line with (a) coupled inductors, (b) T-model for the coupled inductors, and (c) effective L' and $C'(\omega)$.

5.2.2 Gate-Line with Coupled Inductors

Fig. 5.3(a) shows the equivalent circuit of the gate-line with coupled inductors where $C_{geff}(\omega)$ is the effective loading capacitance at the input of g_m-cell and has strong frequency dependency especially for cascode cells with series peaking inductor. The coupled inductor is substituted by a T-model in Fig. 5.3(b) where $M = k_g L_g/2$ is the mutual inductance between two adjacent $L_g/2$ inductors. The negative inductance $-M$ is in series with $C_{geff}(\omega)$. Fig. 5.3(c) shows the equivalent gate-line circuit with effective inductance, L', and capacitance, $C'(\omega)$, given by

$$
\begin{aligned}
L' &= L_g(1+k_g) \\
C'(\omega) &= \frac{C_{geff}(\omega)}{1+\omega^2 k_g(\frac{L_g}{2})C_{geff}(\omega)}
\end{aligned}
\tag{5.2}
$$

Since $0 \leq k_g < 1$, L' is always larger than the physical inductance, L_g. As a result, a gate-line with lower physical inductance (ohmic loss) can be used. Also, $C'(\omega)$ is less sensitive to the variation of $C_{geff}(\omega)$ with frequency because of the coupling coefficient, k_g, which also allows the input matching improvement as discussed later. The cut-off frequency, f'_g, of the new gate-line is found by evaluating $C'(f)$ at f'_g as follows

$$
f'_g = \frac{1}{\pi\sqrt{L'C'(f'_g)}} = \frac{1}{\pi}.\sqrt{\frac{1+2\pi^2 f'^2_g L_g C_{geff}(f'_g)k_g}{L_g C_{geff}(f'_g)(1+k_g)}}
\tag{5.3}
$$

Hence

$$
f'_g = \frac{1}{\pi\sqrt{L_g C_{geff}(f'_g)(1-k_g)}}
\tag{5.4}
$$

The dependency of $C_{geff}(\omega)$ to frequency is known for a specific g_m-cell topology as discussed in Subsection 5.3. Since $0 \leq k_g < 1$, increasing k_g improves the bandwidth of the gate-line compared to the case where $k_g = 0$ with similar physical L_g. Also, the characteristic impedance of the new line is defined as

$$\begin{aligned} Z'_g(\omega) &= \sqrt{\frac{L'}{C'(\omega)}.(1-(\frac{\omega}{\omega'_g})^2)} \\ &= \sqrt{L_g(1+k_g).\frac{1+\omega^2 k_g(\frac{L_g}{2})C_{geff}(\omega)}{C_{geff}(\omega)}.(1-(\frac{\omega}{\omega'_g})^2)} \end{aligned} \tag{5.5}$$

Similar to $C'(\omega)$, $Z'_c(\omega)$ has also less dependency to $C_{geff}(\omega)$ which means the gate-line characteristic impedance is less degraded by the g_m-cell frequency variation. Also, by adjusting the value of $Z'_c(\omega)$ using k_g and L_g, an input matching close to the source impedance, Z_0, within the band of interest is achievable as will be seen in the design methodology subsection.

5.2.3 Gain Stage

Fig. 5.4(a) shows the AC equivalent circuit of the cascode gain stage with series-peaking and gate-line with coupled inductors. Fig. 5.4(b) represents the high-frequency small-signal model suitable for calculating the total transconductance $G_{m,T} = I_o/V_i$ as follows

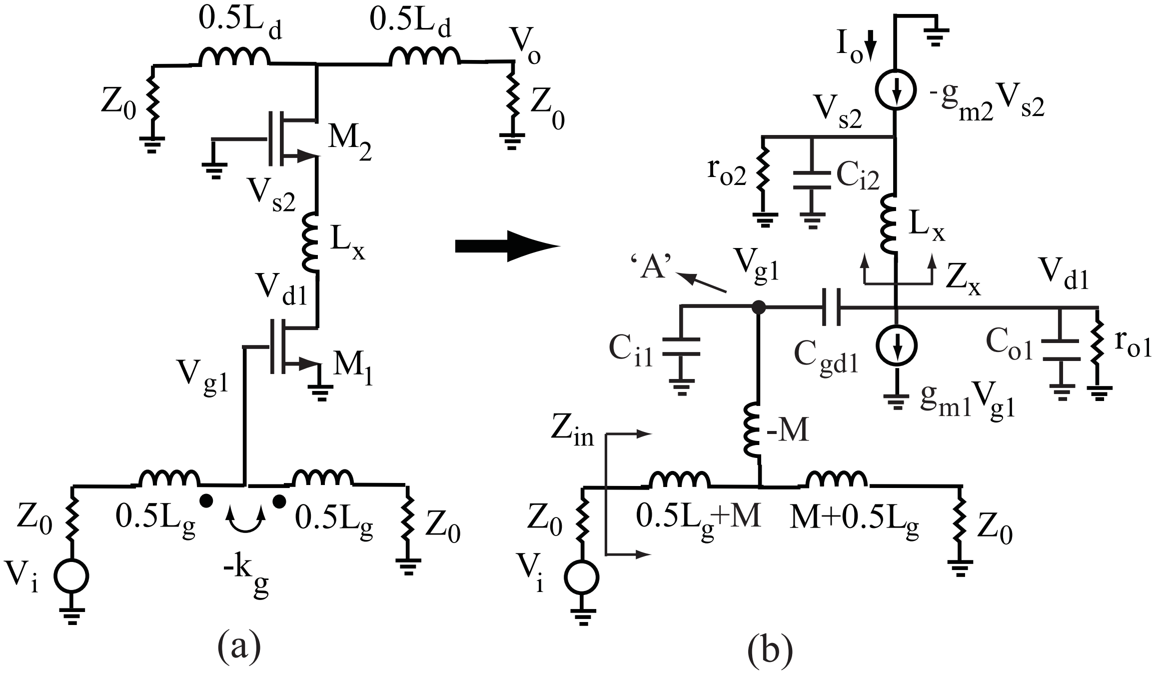

Figure 5.4: (a) The schematic of a cascode gain stage with peaking and gate-line with coupled inductors and (b) small-signal model, for $G_{m,T}$ calculation.

$$\begin{aligned} G_{m,T}(s) = \frac{I_o}{V_i}(s) = -g_{m2}.\frac{V_{s2}}{V_i}(s) &= -g_{m2}.\frac{V_{s2}}{V_{g1}}(s).\frac{V_{g1}}{V_i}(s) \\ G_{m,T}(s) &= G_{m,C}(s).\frac{V_{g1}}{V_i}(s) \end{aligned} \tag{5.6}$$

where $G_{m,C} = -g_{m2}.V_{s2}/V_{g1}$ is the transconductance of the cascode stage. Assuming $C_{gd1} \ll C_{i2}, C_{o1}$ and neglecting the effect of r_{o1} and r_{o2}, the voltage gain, V_{s2}/V_{g1}, is calculated by multiplying V_{s2}/V_{d1} and V_{d1}/V_{g1} transfer functions given by

$$\frac{V_{s2}}{V_{d1}}(s) = \frac{1}{s^2 L_x C_{i2} + s L_x g_{m2} + 1} \tag{5.7}$$

$$\frac{V_{d1}}{V_{g1}}(s) = -g_{m1}.(Z_x || \frac{1}{sC_{o1}}) \tag{5.8}$$

where g_{m1} is the transconductance of M_1 and

$$Z_x(s) = sL_x + \frac{\frac{1}{g_{m2}}}{1 + s(\frac{C_{i2}}{g_{m2}})} \tag{5.9}$$

As a result

$$G_{m,C}(s) = -g_{m1}.\frac{1}{1 + sZ_xC_{o1}}.\frac{1}{1 + s\frac{C_{i2}}{g_{m2}}} \tag{5.10}$$

$G_{m,C}$ has a pole at $f_0 = g_{m2}/(2\pi C_{i2})$. The inductive behavior of Z_x due to L_x resonates with C_{o1} at higher frequencies, resulting in a gain peaking at f_p in the frequency response [86]. Fig. 5.5 shows the normalized transconductance of the cascode stage, $|G_{m,CN}(jf)|_{dB} = |G_{m,C}(jf)/g_{m1}|_{dB}$, vs. frequency for different values of L_x. For a small value of L_x, $G_{m,C}$ has a low-frequency pole ($f_0 < f_p$) showing a gain roll-off at mid-band. By increasing L_x, f_p decreases, the gain roll-off in the mid-band disappears and gain-peaking increases. Therefore, the value of L_x is selected to achieve the maximum bandwidth with minimum roll-off in the mid-band.

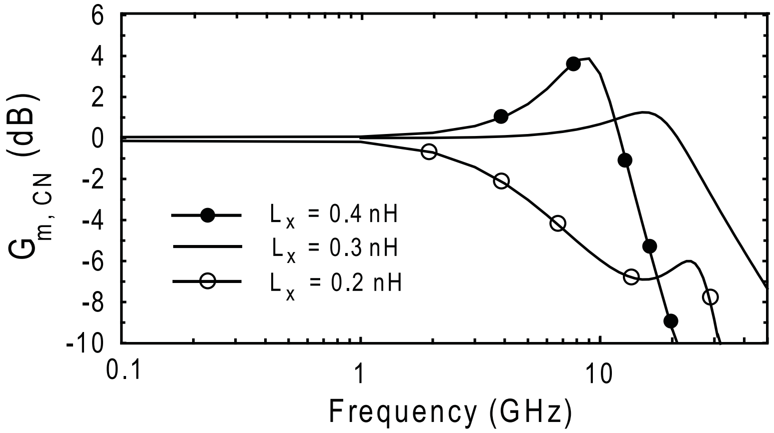

Figure 5.5: $|G_{m,CN}(jf)|_{dB}$ vs. frequency for different values of L_x.

The effective loading capacitance of the cascode stage at node $'A'$ in Fig. 5.4(b) is calculated using Miller effect

$$C_{geff}(s) = C_{i1} + C_{gd1}(1 - \frac{V_{d1}}{V_{g1}}(s)) \tag{5.11}$$

Finally, the transfer function of the gate-line is given by

$$\frac{V_{g1}}{V_i}(s) = \frac{1}{s^2(\frac{L_g}{2})(1-k_g)C_{geff}(s) + sZ_0C_{geff}(s) + 2} \tag{5.12}$$

Since $C_{geff}(s)$ is a function of frequency itself as described in (5.8) and (5.11), the transfer function of the gate-line is not simply a second order low-pass response. The input return loss of the gain stage is found by calculating the input impedance Z_{in} in Fig. 5.4(b) and using the equation $S_{11}(s) = \frac{Z_{in}(s)-Z_0}{Z_{in}(s)+Z_0}$ and is given by

$$\begin{aligned} S_{11}(s) \;\; = \;\; & \frac{s^3\frac{L_g^2}{4}(1-k_g^2)C_{geff}(s) + \cdots}{s^3\frac{L_g^2}{4}(1-k_g^2)C_{geff}(s) + 2s^2C_{geff}(s)\frac{L_g}{2} + \cdots} \\ & \frac{\cdots + s[L_g(1+k_g) - C_{geff}(s)Z_0^2]}{\cdots + s[L_g(1+k_g) + C_{geff}(s)Z_0^2] + 2Z_0} \end{aligned} \tag{5.13}$$

The term $\frac{L_g^2}{4}(1-k_g^2)C_{geff}(s)$ is the coefficient of the highest order term in both numerator and denominator polynomials. Increasing k_g reduces the value of this coefficient for a certain value of L_g at a certain frequency . This means that the poles and zeros of $S_{11}(s)$ will shift to higher frequencies and in case $S_{11}(s)$ has a small value at low frequencies, increasing k_g increases the frequency at which S_{11} starts to degrade.

5.2.4 Drain-Line

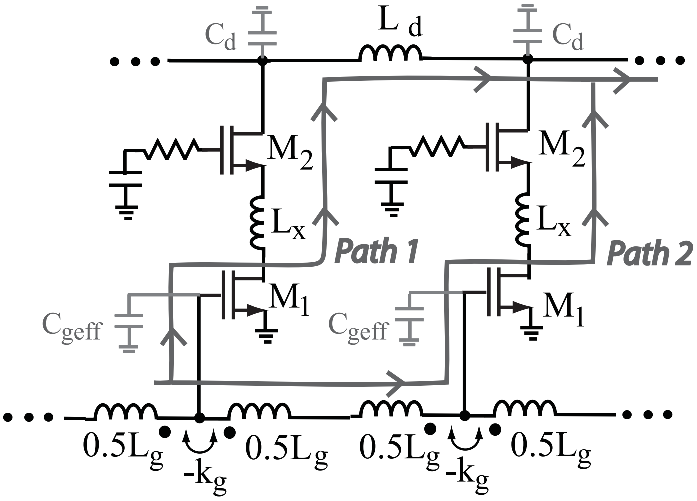

Figure 5.6: Two different signals passing through gate and drain lines between two arbitrary gain stages.

With the coupled inductor in the gate line, the phase delays of the gate and drain lines between each gain stage are different. Fig. 5.6 shows two different signals passing through gate and drain lines between two arbitrary gain stages and adding up at the output of the second stage. Both signals are passing through equal series peaking inductors. Therefore, L_x does not generate any phase difference between the two signals. To provide in-phase signals at the output of each g_m-cell, the equivalent circuit of the coupled gate-line with effective values of L' and $C'(\omega)$ derived in (5.2) is used as follows

$$\begin{gathered}\sqrt{L'C'(\omega)} = \sqrt{L_d C_d} \\ \sqrt{\frac{L_g(1+k_g)C_{geff}(\omega)}{1+\omega^2 k_g(\frac{L_g}{2})C_{geff}(\omega)}} = \sqrt{L_d C_d} \end{gathered} \tag{5.14}$$

Also, to provide matching at the drain-line

$$Z_d = \sqrt{L_d/C_d} = Z_0 \tag{5.15}$$

Equations (5.14) and (5.15) provide the required values of L_d and C_d for a given $C_{geff}(\omega)$, k_g and L_g to provide phase matching as will be seen in the design methodology subsection.

Drain-line inductors can also be coupled similar to the gate-line ones with a coupling factor of k_d. Since there is no Miller effect and non-uniform loading at the drain of M_2 in Fig. 5.1(d), reasonable output matching is achievable without coupling the drain-line inductors. The advantage of coupling the drain-line inductors is to reduce their effective value by a factor of $(1+k_d)$ to achieve smaller inductors with lower loss. Since reducing the size of the amplifier has not been the major purpose of this work, drain-line inductors are not coupled to each other to simplify the layout implementation.

5.2.5 Number of Stages

There is no limit on the number of the stages in a distributed amplifier with lossless artificial lines. However, both gate and drain artificial lines are lossy in practice (L_g and L_d have limited quality factors). Therefore, there is an optimum value for number of stages of an amplifier with artificial lines (Fig. 5.1(a)) which is given by [79]

$$N_{opt} = \frac{\ln(\frac{\theta_{rd}}{\theta_{rg}})}{\theta_{rd} - \theta_{rg}} \tag{5.16}$$

where θ_{rg} and θ_{rd} are real part of the gate- and drain-line propagation constants, respectively. Assuming the loss of C_g and C_d is negligible, θ_{rg} and θ_{rd} are approximated by [79]

$$\begin{gathered} \theta_{rg} = \frac{R_g}{2L_g} \cdot \frac{d\theta_{ig}}{d\omega}, \theta_{rd} = \frac{R_d}{2L_d} \cdot \frac{d\theta_{id}}{d\omega} \\ \cos(\theta_{ig}) = 1 - 2 \cdot (\frac{\omega}{\omega_g})^2, \cos(\theta_{id}) = 1 - 2 \cdot (\frac{\omega}{\omega_d})^2 \end{gathered} \tag{5.17}$$

where R_g and R_d are the loss of inductors L_g and L_d, and θ_{ig} and θ_{id} are the imaginary part of the gate- and drain-line propagation constants, respectively. To find out the optimum number of stages, N'_{opt}, for the gain stage with coupled inductors in the gate-line (Fig. 5.1(d)), the effective inductance, L', presented in (5.2) is employed. By combing equations (5.2), (5.16), and (5.17), N'_{opt} is given by

$$N'_{opt} = \frac{Q_d Q'_g \sqrt{(1 - (\frac{f}{f_d})^2)(1 - (\frac{f}{f'_g})^2)} \cdot \ln(\frac{Q'_g}{Q_d} \cdot \sqrt{\frac{1-(\frac{f}{f'_g})^2}{1-(\frac{f}{f_d})^2}})}{Q'_g \sqrt{(1 - (\frac{f}{f'_g})^2)} - Q_d \sqrt{(1 - (\frac{f}{f_d})^2}} \tag{5.18}$$

where $Q_d = L_d \omega_d / R_d$ and $Q'_g = (L_g(1 + k_g)\omega'_g)/R_g$. The optimum number of stages for the amplifiers with cascode g_m-cells (Fig. 5.1(c)) in CMOS technology is calculated to be 3 in [80], [81], [84], and [85], considering the loss of reported inductors on silicon,. For the proposed distributed amplifier, The optimum number of gain stages can be set higher (four in this design) due to lower loss inductors in the artificial gate-lines as a result of mutual coupling. The design procedure presented in the design methodology subsection, shows how N'_{opt} is found using (5.18) assuming the loss of inductors are known.

5.2.6 Design Methodology

To achieve an overall flat response for $G_{m,T}$, the gate-line cut-off frequency needs to be selected in a way that the transfer function of the line compensates the gain peaking of $G_{m,C}$ at f_p meaning

$$|\frac{V_{g1}}{V_i}(jf_p)| = \frac{|g_{m1}|}{|G_{m,C}(jf_p)|} = \frac{1}{|G_{m,CN}(jf_p)|} \tag{5.19}$$

By substituting $s = j(2\pi f)|_{f_p}$ in (5.12), equation (5.19) is modified to

$$\sqrt{(1-(\frac{f_p}{f'_g}.\frac{C_{geff}(f_p)}{C_{geff}(f'_g)})^2)^2 + (\pi f_p C_{geff}(f_p) Z_0)^2} = \frac{|G_{m,CN}(jf_p)|}{2} \tag{5.20}$$

Solving the above equation for given f_p, $C_{geff}(f_p)$ and Z_0 results in the required gate-line cut-off frequency, f'_g, and the value of $C_{geff}(f'_g)$ through (5.12).

To have a matched gain-stage at the input, equation (5.5) is evaluated at $f = f_p$ to satisfy $Z'_g(f_p) = Z_0$ or

$$\sqrt{L_g(1+k_g).\frac{1+2(\pi f_p)^2 k_g L_g C_{geff}(f_p)}{C_{geff}(f_p)}.(1-(\frac{f_p}{f'_g})^2)} = Z_0 \tag{5.21}$$

By knowing the values of f'_g, and $C_{geff}(f'_g)$ and solving two nonlinear equations (5.4) and (5.21) together, the required values of k_g and L_g found to achieve a flat response and acceptable input matching. Also, by solving (5.14) and (5.15) at f_p, using the values of k_g, L_g and $C_{geff}(f_p)$, the values of L_d and C_d will be found.

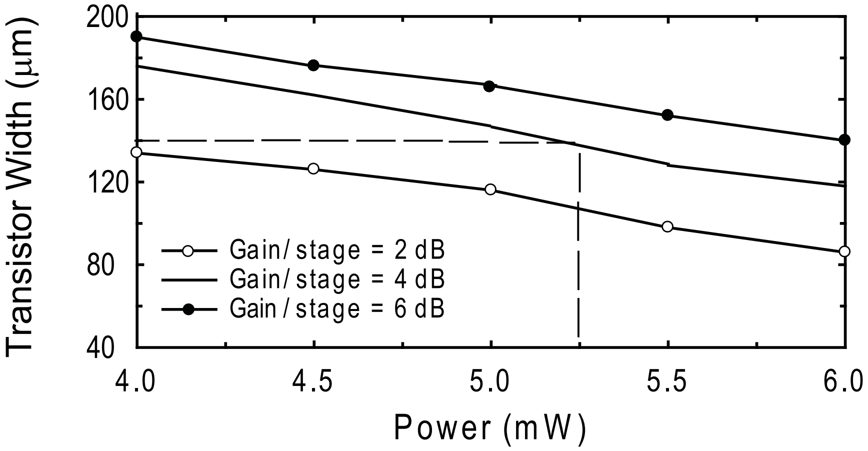

Figure 5.7: The simulated aspect ratio of transistors M_1 and M_2 in Fig. 5.1(d) vs. power consumption of each gain stage for different values of gain per stage.

In conclusion, a design methodology is proposed based on the derived equations. The purpose of this methodology is to design a distributed amplifier with cascode gain stages and coupled gate inductors to achieve maximum flat bandwidth and acceptable input matching for a given total gain and power consumption. A summary of systematic design steps is explained first and then, these steps are applied to design the desired distributed amplifier in 0.18 μm process.

Step 1: Assume the optimum number of stages, N'_{opt}, to be a number between 3-5. Therefore, is within the range of optimum number of stages reported for various distributed amplifiers [79]. The total gain and power consumption of the amplifier and thus for each stage are given.

Step 2: Find the transistors biasing current and aspect ratios for a certain gain and power consumption per stage using Fig. 5.7. It shows the simulated aspect ratio of transistors M_1 and M_2 in Fig. 5.1(d) vs. power consumption of each gain stage for different values of gain per stage using Cadence assuming $(\frac{W}{L})_1 = (\frac{W}{L})_2$.

Step 3: Extract the values of C_{i1}, C_{i2}, C_{o1}, and C_{gd1} using Cadence and knowing the calculated aspect ratios, .

Step 4: Calculate the value of cascode stage transconductance, $G_{m,C}$, using (5.9) and (5.10) and maximize the bandwidth of the cascode amplifier (f_p) by adjusting L_x to cancel the gain roll-off effect due to the pole, $f_0 = g_{m2}/(2\pi C_{i2})$ as shown in Fig. 5.5.

Step 5: Find The effective loading capacitance of the cascode stage, C_{geff}, at f_p using (5.11).

Step 6: Calculate the gate-line cut-off frequency, f_g', using (5.20) to achieve a flat response for $G_{m,T}$,.

Step 7: Find the values of k_g and L_g by solving (5.4) and (5.21) assuming the matching condition at the vicinity of f_p.

Step 8: Knowing the values of k_g and L_g, and evaluating (5.14) and (5.15) at $f = f_p$, calculate L_d and C_d and $f_d = 1/\pi\sqrt{L_d C_d}$ to provide the required phase matching between the gate- and drain-lines.

Step 9: By finding the practical values of loss for the calculated L_g and L_d using the available design kit, calculate the values of R_g, R_d, Q_g' and Q_d and the optimum number of stages using (5.18). If this number is the same as what is assumed in Step 1, then the design is finalized. If not, change the value of N_{opt}' and repeat all the following steps until similar value of N_{opt}' is achieved from Steps 1 and 9.

This design methodology is applied to design a distributed amplifier in 0.18 μm process as follows,

Step1: A four-stage amplifier with an overall power gain of 10 dB and a power budget of around 21 mW is considered (power gain per stage $\sim$ 4 dB and power consumption per stage $\sim$ 5.25 mW).

Steps 2,3: The appropriate device aspect ratio are then selected for a given gain and power consumption per stage using Fig. 5.7 ($(\frac{W}{L})_1 = (\frac{W}{L})_2 = \frac{140\ \mu m}{0.18\ \mu m}$). The values of parasitic capacitances are then calculated using Cadence ($C_{i1} = C_{i2}$ =0.94 pF, $C_{o1} = 0.47$ pF and $C_{gd1} = 0.26$ pF).

Steps 4,5: For the selected transistor aspect ratio, the series peaking inductor, L_x, is adjusted to be around 0.3 nH to maximize the flat bandwidth of the cascode gain stage ($f_p = 16$ GHz) as shown in Fig. 5.5. In this case, $|G_{m,CN}(jf_p)|_{dB} = 1.24$ dB. Also, $C_{geff}(f_p)$ is calculated from (5.11).

Step 6: To achieve the flat response within the bandwidth, the cut-off frequency, f'_g, is calculated to be around 21.7 GHz using (5.20).

Step 7: By solving (5.4) and (5.21) together, the values of k_g and L_g are found to be 0.21 and 0.45 nH, respectively.

Step 8: The value of L_d is calculated to be 0.5 nH through (5.14) assuming $k_g = 0.2$, $L_g = 0.4$ and $f_p = 16$ GHz to equalize gate- and drain-line phase shifts.

Step 9: The loss of inductor $L_g = 0.4$ nH and $L_d = 0.5$ nH are found to be 3.4 and 4.2 Ω using the 0.18 μm CMOS process design kit, and the value of N'_{opt} is found to be close to four using (5.18).

To verify the proposed design methodology, the effect of various combinations of (L_g, k_g) is investigated on the gate-line insertion loss, $|(V_{g1}/V_i)(jf)|_{dB}$, the total normalized transconductance, $|G_{m,TN}(jf)|_{dB} = |G_{m,T}(jf)/g_{m2}|_{dB}$, and the input return loss ,$|S_{11}(jf)|_{dB}$, of a single gain-stage using equations (5.6)-(5.13) and MATLAB. Fig. 5.8 shows the simulated $|(V_{g1}/V_i)(jf)|_{dB}$, $|G_{m,TN}(jf)|_{dB}$, and $|S_{11}(jf)|_{dB}$ of the gain-stage for different values of k_g and L_g where $L_x = 0.3$ nH, $f_p = 16$ GHz, and $|G_{m,CN}(jf_p)|_{dB} = 1.24$ dB.

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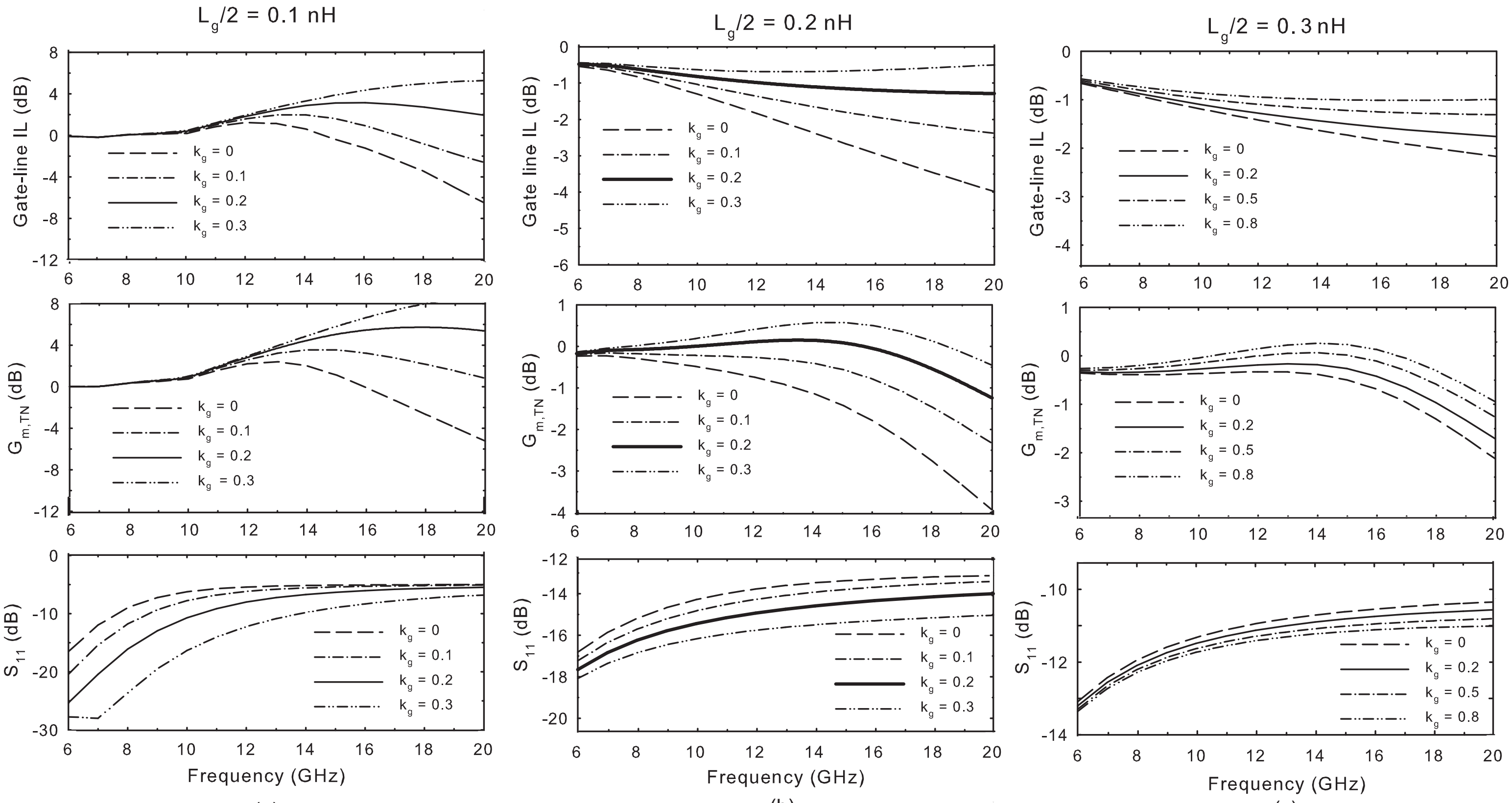


(a) (b) (c)

Figure 5.8: Simulated $|(V_{g1}/V_i)(jf)|_{dB}$, $|G_{m,TN}(jf)|_{dB}$, and $|S_{11}(jf)|_{dB}$ of a single gain-stage for $L_g/2$ of (a) 0.1 nH, (b) 0.2 nH and (c) 0.3 nH and different values of k_g ($L_x = 0.3$ nH, $f_p = 16$ GHz and $|G_{m,CN}(jf_p)|_{dB} = 1.24$ dB)

In case of $L_g/2 = 0.1$ nH (Fig. 5.8(a)), a peaking in the gate-line response is observed due to the effect of C_{geff} on the line which adds up to the peaking introduced by the cascode stage. As a result, the overall peaking of the total transconductance is increased. For $k_g = 0$, this peaking is minimum, but the input return loss is worse than 10 dB for 8-16 GHz frequency range. Increasing k_g improves the input matching, but the peaking level in the total response becomes unacceptable.

In case of $L_g/2 = 0.2$ nH (Fig. 5.8(b)), the effect of gate-line insertion loss peaking due to C_{geff} is eliminated by increasing the value of L_g compared to the previous case. The gate-line insertion loss cancels out the peaking of $|G_{m,CN}(jf)|$ at f_p for $k_g = 0.2$ and a flat transconductance response is achieved with S_{11} <-15 dB over the band of interest. Increasing k_g to 0.3 improves the gate-line cut-off frequency and input matching, but the total transconductance shows peaking at f_p because f'_g increases and $|(V_{g1}/V_i)(jf_p)| < 1/|G_{m,CN}(jf_p)|$. Therefore, flat bandwidth extension is not achieved although input matching shows more improvement. For $k_g = 0$, the gate-line cut-off frequency drops below f_p. As a result, $|G_{m,TN}(jf)|$ does not achieve maximum flat bandwidth extension.

In case of $L_g/2 = 0.3$ nH (Fig. 5.8(c)), the cut-off frequency of the line drops below f_p for lower value of k_g which limits the bandwidth extension ($k_g = 0$ provides lowest bandwidth extension). To increase the cut-off frequency of the line, k_g needs to increase considerably ($\sim$ 0.5-0.8) which results in total or partial peaking cancellation of $|G_{m,CN}(jf)|$ at f_p for $k_g = 0.5$ or 0.8, respectively. On the other hand, increasing k_g does not improve the gate-line response at lower frequencies as much as frequencies close to cut-off (an insertion loss of 0.8-1 dB is observed for the gate-line around 6-8 GHz frequency range for 0< k_g <0.8). Therefore, the overall transconductance response is not completely uniform within the band of interest which results in larger input mismatch compared to the previous case where $L_g/2 = 0.2$ nH. The results of the above simulation show a gain stage with $L_g/2 = 0.2$ nH and $k_g = 0.2$ provides the widest flat response with best input matching for $f_p = 16$ GHz. As shown earlier, similar values are obtained for L_g and k_g using the proposed design methodology.

5.3 Circuit Design and Implementation

The four-stage amplifier with f_p of 16 GHz, a power gain of 10 dB and an overall power budget of 21 mW is implemented using the procedure explained in the previous subsection. Fig. 5.9 illustrates the schematic of the entire four-stage amplifier including two bias-Ts were used at the input and output RF terminals to bias different gain stages during the measurement.

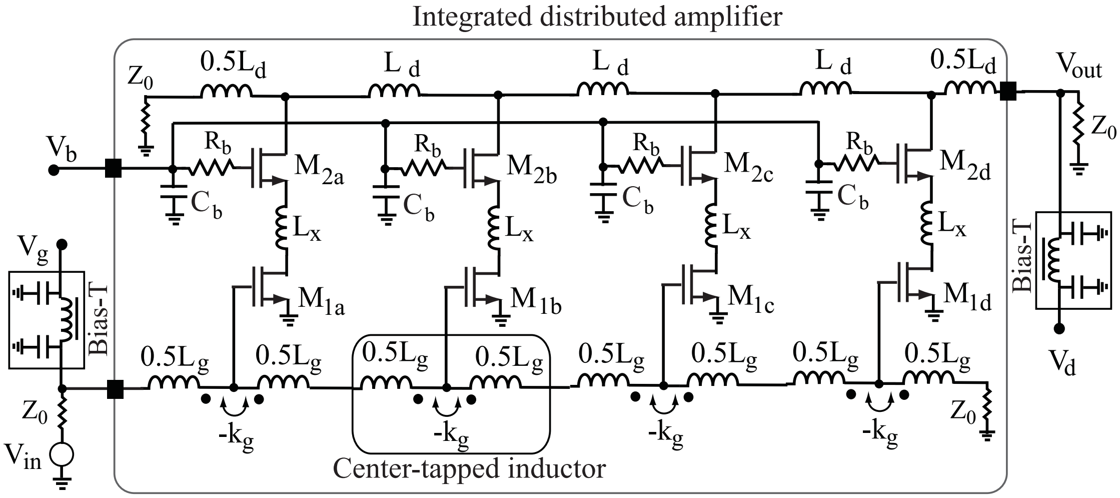


Figure 5.9: The schematic of the entire four-stage amplifier including bias-Ts.

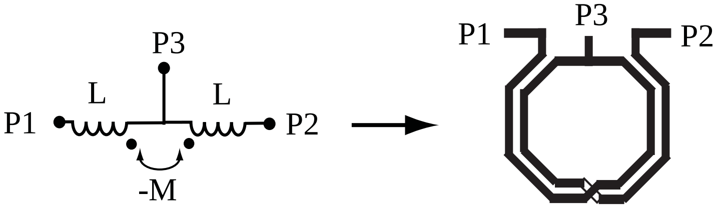
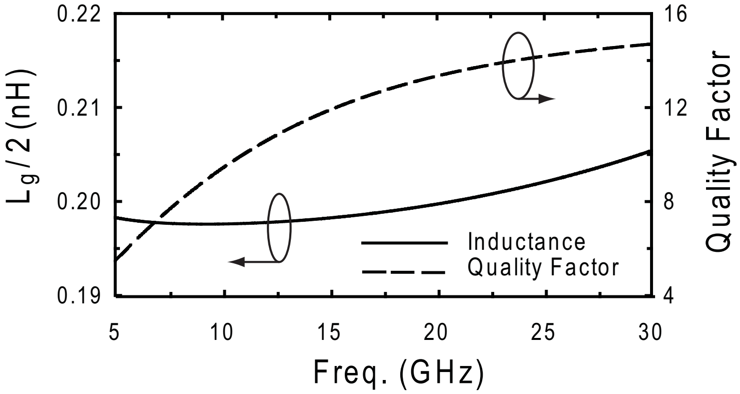
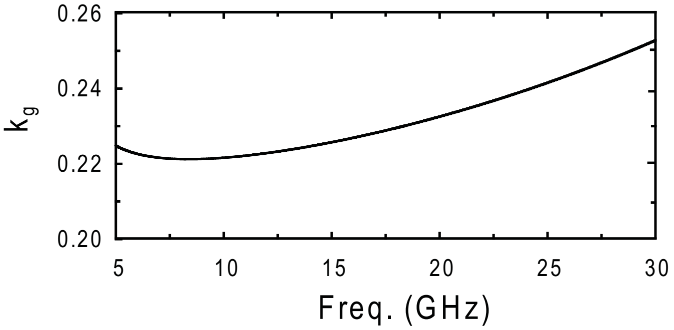


Figure 5.10: Layout of a center-tapped differential inductor.



(a)



(b)

Figure 5.11: (a) Simulated inductance and quality factor, and (b) simulated coupling coefficient of the gate-line coupled inductor vs. frequency using Sonnet.

The coupled inductor is implemented differentially as shown in Fig. 5.10 [88]. When the windings of the inductor are designed properly, the magnetic fields add constructively due to strong mutual coupling between the two inductors resulting in an increase in inductance without a corresponding increase in series resistance and a higher inductor Q (Q ~12 at 16 GHz). In order to consider high frequency effects in inductor/mutual coupling realization, EM simulation is used. The metal/dielectric profile of the process is employed in Sonnet.to optimize the layout of each inductor. The simulated inductance, quality factor and coupling coefficient of the implemented gate-line coupled inductor versus frequency are shown in Fig. 5.11.

In layout implementation, ground plane is used to shield the inductors from each other. The distance between ground plane and inductors is optimized using full-wave simulation to reduce the unwanted coupling to < -40 dB while minimizing the extra parasitic capacitance. All the inductors are realized with top metal layer which is the thickest and farthest layer from the substrate to reduce the substrate loss. The parasitic capacitance of the wide drain line inductors is considered at the output of each gain stage to avoid additional drain capacitances for phase velocity balance between gate and drain lines. Both inductors L_d and L_x are implemented using standard spiral structures and optimized using full-wave simulation.

The transistors are laid out with maximum number of fingers and close to minimum width to minimize the effective series gate resistance [89]. Tapering is used to connect inductors to transistors and pads to minimize the parasitic due to discontinuities. Capacitance degeneration at the source of M_2 in Fig. 5.1(d) results in negative input resistance at the gate of M_2 at very low frequencies. To avoid this problem, series resistance, R_b, and shunt capacitance, C_b, are added to the gate of M_2. C_b compensates the gain reduction at higher frequencies because of R_b. Table 5.1 shows the circuit element values and transistor aspect ratios for the implemented distributed amplifier. Fig. 5.12 shows a microphotograph of the fabricated distributed amplifier with a chip size of 1.4 mm × 0.85 mm (including testing pads) using 0.18 μm CMOS process.

Table 5.1: Circuit element values and transistor aspect ratios for the implemented distributed amplifier.

L_g (nH)	L_d (nH)	L_x (nH)	k_g	$(\frac{W}{L})_{1,2}$
0.4	0.5	0.3	0.22	$\frac{140\mu\text{m}}{0.18\mu\text{m}}$

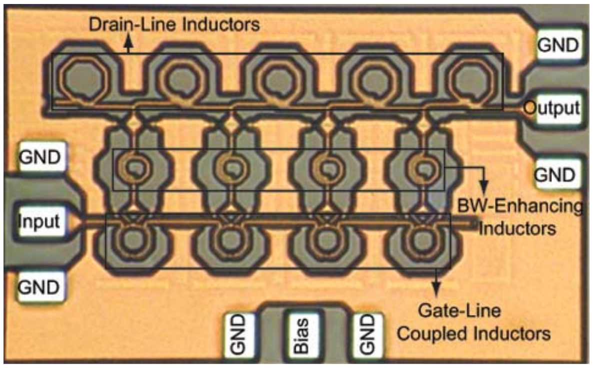


Figure 5.12: Microphotograph of the proposed CMOS distributed amplifier with a chip size of 1.4 × 0.85 mm^2 (including testing pads).

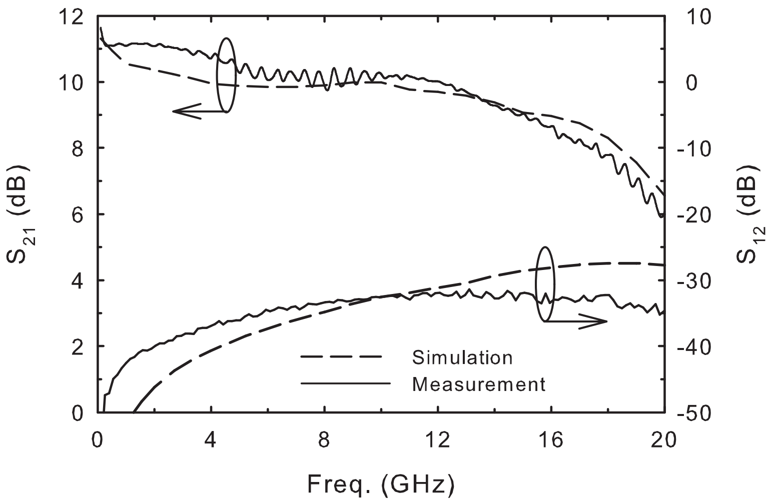
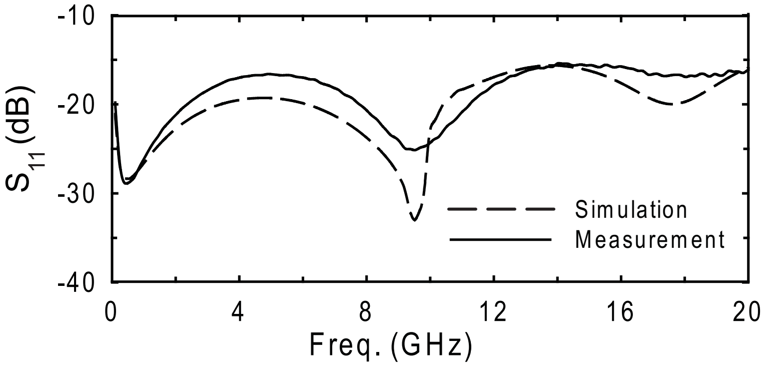


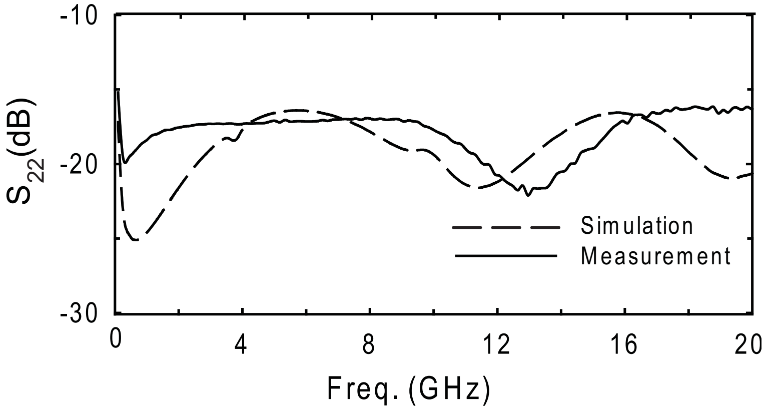
Figure 5.13: Simulated and measured gain (S_{21}) and reverse isolation (S_{12}).

5.4 Simulation and Measurement Results

The CMOS distributed amplifier chip was tested via on wafer probing using Ground-Signal-Ground (GSG) coplanar air probes. S-parameter measurements of the circuit were carried out using the Agilent N5230C vector network analyzer. The measurements are performed under operating conditions of V_{DD} = 1.3 V and the overall current consumption of 16 mA. Fig. 5.13 demonstrates the simulated and measured forward gain (S_{21}) and reverse isolation (S_{12}) verifying the accuracy of post-layout simulations. The power gain is around 10 dB with 1 dB frequency band around 16 GHz, and the in-band isolation is less than -30 dB. No gain peaking is observed in the gain response due to employing coupled-gate inductors. The superior input-output isolation is partly due to the utilization of cascode cells in the proposed amplifier. Fig. 5.14 depicts the simulated and measured input and output return loss (S_{11} and S_{22}). S_{11} and S_{22} remain below 16 and 18 dB in the operating band, respectively. The improved input return loss is also due to employing coupled gate-line inductors which result in more uniform transmission line as discussed earlier.



(a)



(b)

Figure 5.14: Simulated and measured (a) input return loss (S_{11}) and, (b) output return loss (S_{22}).

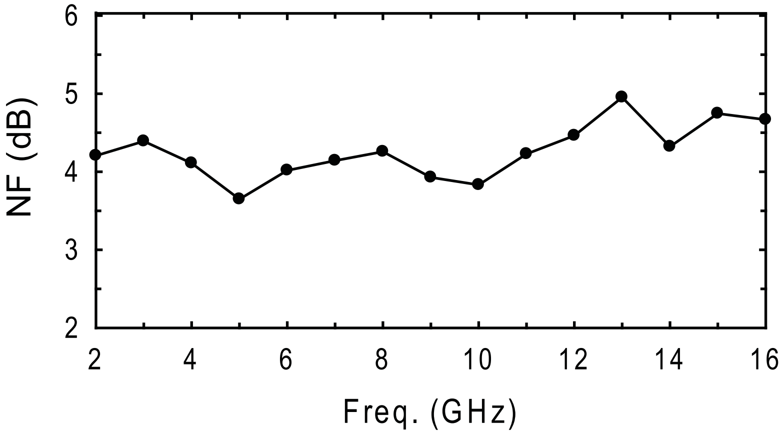


Figure 5.15: Measured noise figure (NF) of the distributed amplifier.

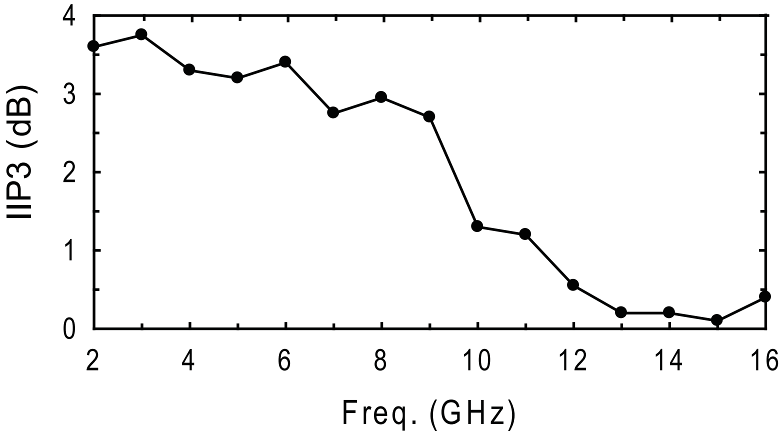


Figure 5.16: Measured third order intercept point (IIP3) of the distributed amplifier.

The measured noise figure of the distributed amplifier is reported in Fig. 5.15. The noise figure is around 3.6-4.9 dB within the band of interest. The linearity measurement was performed using the Agilent E4446A spectrum analyzer. The measured IIP_3 vs. frequency is shown in Fig. 5.16 and varies between 0.1-3.75 dBm within the band of interest. Table 5.2 shows a comparison among different performance parameters for recent distributed amplifiers fabricated using 0.18 μm CMOS process and this work. All the amplifiers listed in Table 5.2 were measured using bias-Ts.

5.5 Summary

A distributed amplifier with coupled inductors in gate artificial transmission line is proposed to extend the flat bandwidth and improve the input matching of the amplifier without any power consumption penalty. The detailed analysis of the distributed amplifier, including the gate-line with coupled inductors and the gain stage was presented. In addition, a design methodology for extending the flat bandwidth and improving the input matching of the amplifier was proposed. The fabricated circuit in a standard 0.18 μm CMOS process, exhibits a pass-band gain of 10 dB and a flat 1-dB bandwidth of 16 GHz. Because of the coupled gate inductors input matching better that 16 dB is achieved. Also, the circuit consumes a DC power of 21 mW.

Table 5.2: Performance Comparison of Recent Distributed Amplifiers in 0.18 μm CMOS process.

Ref.	Gain (dB)	BW (GHz)	P_{DC} (mW)	IIP_3 (dBm)	NF (dB)	S_{11}, S_{22} (dB)	Area (mm^2)	No. of stages
[80]	10.6	14^*	54	$9.4^‡$	$3.4 - 5.4$	$< -11, < -12$	1.35	3
[81]	7.3	22^*	54	$9.6^‡$	$4.3 - 6.1$	$< -8, < -9$	1.6	3
[82]	4	39^*	140	N/A	N/A	$< -10, < -10$	3.3	8
[83]	9	$25^†$	60	N/A	4.7	$< -10, < -12$	0.36	2
[84]	8.6	6.2^*	9	3	$4.2 - 6.2$	$< -16, < -10$	1.16	3
[85]	8	11^*	21.6	$(-4.1) - (-3.0)$	2.9	$< -12, < -10$	0.76	3
[86]	20	$39.4^†$	250	$-4.5^‡$	$8.0 - 9.4$	$< -10, < -20$	2.24	2×4
This Work	10	16^*	21	$0.1 - 3.75$	$3.6 - 4.9$	$< -16, < -18$	1.19	4

^{a} 1-dB bandwidth, †3-dB bandwidth, ‡$IIP_3 = OIP_3 - Gain|_{dB}$.

6. CONCLUSIONS

In this dissertation, novel on-chip and on-board RF/Microwave systems for chemical sensing and permittivity detection have been presented. A prototype for an on-chip self-sustained chemical senor is proposed, implemented using 90 nm CMOS technology and validated for permittivity detection. The entire system, including the sensing element, the VCO, the frequency synthesizer and the ADC are fully analyzed and experimentally characterized for a given sensing resolution. Sensor calibration is performed using reference materials, including air, Ethanol, Methanol and DMSO. Organic chemicals under test, including Isopropanol, II-Butyl Alcohol, Ethyl Acetate, Ethylene Glycol and Acetone, are characterized and their permittivities are detected in the 7-9 GHz frequency range with an error less than 3.7% . The sensor is used for mixture characterization with mixing ratio accuracy better than 2%. The sensing system consumes 16.5 mW with a total area of 2.5×2.5 mm^2.

A miniaturized on-board platform for microwave dielectric spectroscopy has been proposed. The sensing system is based on the detection of the phase difference between the input and output signals of an on-board broadband True-Time-Delay (TTD) cell. The design of TTD cells for permittivity detection has been presented considering: (1) broadband input matching in the 1 - 8 GHz frequency range, (2) cascading multiple TTD cells to achieve larger phase shifts suitable for accurate detection, especially at low frequencies, and (3) minimum distance between adjacent TTD cells to minimize electromagnetic coupling between different cells. The entire spectroscopy system, including sensing elements, TTD cells, SPDT switches and correlators for phase detection, has been fabricated on top of Rogers Duroid 5880 substrates. Sensor calibration and detection algorithms have been performed to detect the permittivties of organic chemicals in the 1-8 GHz frequency range with an accuracy of 2%. Also, the system is able to characterize binary mixtures with a fractional volume accuracy of 1%.

As a future work, two other prototypes for microwave dielectric spectroscopy are under development: (1) a fully integrated CMOS chemical sensor for ***complex*** permittivity detection in the frequency range of 1 - 12 GHz: Similar to the technique proposed in section 2, the sensing capacitor is implemented on the top metal layer of a CMOS process. The effect of the real and imaginary parts of the complex permittivity is translated into a change in the capacitance and resistance, respectively, of the sensing capacitor exposed to MUTs. The sensing capacitor is embedded inside a capacitive divider structure with a fixed capacitor. This structure is excited by a microwave signal at the sensing frequency. IQ mixers are used to detect the real and imaginary parts of the voltages at the two terminals of the capacitive divider. The magnitude and phase of the ratio between the two voltages represent the values of the capacitance and the resistance of the sensing capacitor. Accordingly, the values of the real and imaginary parts of the permittivity of MUTs can be estimated for a wide range of frequencies, and (2) a miniaturized on-board sensor using the same technique to detect the complex permittivity in the frequency range of 0.7 - 2.5 GHz: A planar sensing capacitor, similar to the one described in section 3, is used with commercial IQ mixers for signal detection.

In the field of CMOS broadband amplifiers, an inductor-less resistive feedback LNA is presented for a higher gain and lower noise figure by using a composite cross-coupled CMOS pair. The inductor-less LNA is implemented using 90 nm CMOS technology in an area of 0.06 mm^2. The LNA is evaluated using two measurement setups: (1) on-wafer probing, and (2) packaged setup. The experimental results using the on-wafer probing show a gain of 21 dB across the 2-2300 MHz frequency range, noise figure ranging between 1.4 and 1.7 dB with an IIP3 of -1.5 dBm. The packaged setup shows a gain of 20 dB across the 2-1100 MHz frequency range, noise figure ranging between 1.43 and 1.9 dB with an IIP3 of -1.5 dBm. The LNA consumes 18 mW from a 1.8 V supply.

Also, a four-stage distributed amplifier is implemented using 180 nm CMOS technology for flat bandwidth extension response up to 16 GHz without any additional power consumption compared to other distributed amplifiers. The flat extended bandwidth is provided using coupled inductors in the artificial transmission line connected to the gates of the transistors, along with series peaking inductors embedded in cascode gain stages. The amplifier is fabricated using 180 nm CMOS technology in an area of 1.19 mm^2 achieving a power gain of 10 dB, input/output return losses better than 16 dB, noise figure of 3.6-4.9 dB, and IIP3 higher than 0 dBm with 21 mW power consumption.

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