LOW-POWER LOW-NOISE CMOS ANALOG AND MIXED-SIGNAL DESIGN TOWARDS EPILEPTIC SEIZURE DETECTION

A Dissertation

by

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Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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April 2013

Major Subject: Electrical Engineering

ABSTRACT

About 50 million people worldwide suffer from epilepsy and one third of them have seizures that are refractory to medication. In the past few decades, deep brain stimulation (DBS) has been explored by researchers and physicians as a promising way to control and treat epileptic seizures. To make the DBS therapy more efficient and effective, the feedback loop for titrating therapy is required. It means the implantable DBS devices should be smart enough to sense the brain signals and then adjust the stimulation parameters adaptively.

This research proposes a signal-sensing channel configurable to various neural applications, which is a vital part for a future closed-loop epileptic seizure stimulation system. This doctoral study has two main contributions, 1) a micropower low-noise neural front-end circuit, and 2) a low-power configurable neural recording system for both neural action-potential (AP) and fast-ripple (FR) signals.

The neural front end consists of a preamplifier followed by a bandpass filter (BPF). This design focuses on improving the noise-power efficiency of the preamplifier and the power/pole merit of the BPF at ultra-low power consumption. In measurement, the preamplifier exhibits 39.6-dB DC gain, 0.8 Hz to 5.2 kHz of bandwidth (BW), 5.86-μV_{rms} input-referred noise in AP mode, while showing 39.4-dB DC gain, 0.36 Hz to 1.3 kHz of BW, 3.07-μV_{rms} noise in FR mode. The preamplifier achieves noise efficiency factor (NEF) of 2.93 and 3.09 for AP and FR modes, respectively. The preamplifier power consumption is 2.4 μW from 2.8 V for both modes. The 6^{th}-order follow-the-

leader feedback elliptic BPF passes FR signals and provides -110 dB/decade attenuation to out-of-band interferers. It consumes 2.1 μW from 2.8 V (or 0.35 μW/pole) and is one of the most power-efficient high-order active filters reported to date. The complete front-end circuit achieves a mid-band gain of 38.5 dB, a BW from 250 to 486 Hz, and a total input-referred noise of 2.48 μV_{rms} while consuming 4.5 μW from the 2.8 V power supply. The front-end NEF achieved is 7.6. The power efficiency of the complete front-end is 0.75 μW/pole. The chip is implemented in a standard 0.6-μm CMOS process with a die area of 0.45 mm^2.

The neural recording system incorporates the front-end circuit and a sigma-delta analog-to-digital converter (ADC). The ADC has scalable BW and power consumption for digitizing both AP and FR signals captured by the front end. Various design techniques are applied to the improvement of power and area efficiency for the ADC. At 77-dB dynamic range (DR), the ADC has a peak SNR and SNDR of 75.9 dB and 67 dB, respectively, while consuming 2.75-mW power in AP mode. It achieves 78-dB DR, 76.2-dB peak SNR, 73.2-dB peak SNDR, and 588-μW power consumption in FR mode. Both analog and digital power supply voltages are 2.8 V. The chip is fabricated in a standard 0.6-μm CMOS process. The die size is 11.25 mm^2.

The proposed circuits can be extended to a multi-channel system, with the ADC shared by all channels, as the sensing part of a future closed-loop DBS system for the treatment of intractable epilepsy.

DEDICATION

To Lili

ACKNOWLEDGEMENTS

First of all, my appreciation goes to my advisor, Dr. Edgar Sánchez-Sinencio, for his long-time support and encouragement throughout my graduate study. In the past six years under his guidance, I always regard him as a role model of being a brilliant scientist with serious scientific attitude and a great teacher with wisdom to inspire and encourage his students. He not only has taught me technical knowledge for my research work but also the vision to explore new areas for my future professional development. I am truly grateful to him for letting me involve in this interesting project. The work presented in this dissertation would not have been done without his advice.

I am greatly indebted to Dr. Jordi Parramon for being my mentor and manager during my intern work at Boston Scientific. He is the one who guided me to the wonderland of implantable electronic design for neural applications. His support and guidance are vital to my PhD research. I also want to extend my gratitude to Tim White at Boston Scientific for his help on the layout of my circuits.

I would like to thank Dr. José Silva-Martínez, Dr. Arum Han and Dr. Samba Reddy for serving on my committee. I am heartily thankful to them for reviewing my work, sharing their thoughts and giving me helpful suggestions.

Thanks also go to Lei Chen, Weigi Ho, Shan Huang, Xi Chen, Heng Zhang and Erik Pankratz for fruitful discussions on both course and research works. Their friendship makes my time at Texas A&M University a joyful experience.

Finally, I am deeply thankful to my wife, Lili Liu, and my parents for their kindness, enduring support and continuous encouragement to my work and life.

TABLE OF CONTENTS

CHAPTER Page

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Motivation

Epileptic seizures are sudden recurrent convulsions due to synchronized neuro-firings that interrupt normal brain functions. As a result, patients may experience loss of cognition, loss of motor control, and possibly even death. About 50 million people worldwide (including around 3 million in the US) suffer from epilepsy [1]. Medication is the mainstay of epilepsy treatment today. However, one third of patients with epilepsy have seizures that are refractory to any medical therapy. Surgical treatment can be effective in patients with partial or focal seizures. However, patients with generalized seizures, or those who have more than one epileptogenic zone, usually do not show complete seizure control with existing surgical therapies [1], [2]. Besides, surgery may cause irreversible effect to patient's brain function.

Recently, increasing evidence shows deep brain stimulation (DBS) as an effective and safe way of controlling intractable epileptic seizures [3], [4]. The emerging DBS technology enables the treatment of many medicine/surgery intractable neural disorders, such as Parkinson's disease, essential tremor, depression and epilepsy, *etc.* As shown in Fig. 1.1, a modern DBS system usually includes an implanted pulse generator (IPG) in patient's body and multiple leads routing through the neck to the patient's brain with electrodes targeted into the specific brain area. The IPG delivers the electrical pulse stimulations through the electrodes for the inhibition of over-excitable brain tissues [5].

Among all the indications, epileptic stimulation has been fast emerging with increasing research efforts dedicated to it.

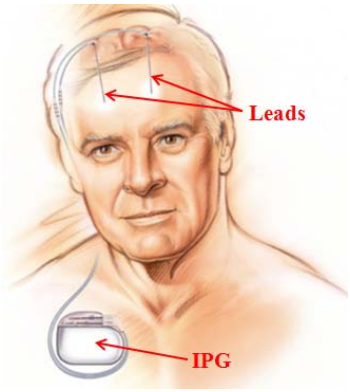

Fig. 1.1. Implantable DBS system (Plot courtesy of Medtronic, Inc.).

Currently, few DBS systems work with the benefit of neural sensing. The titration of therapy requires visual inspection of clinical symptoms by a physician, who then manually adjusts the stimulation therapy through a clinician programmer communicating wirelessly to the IPG. This is eventually a "one-way" system. Taking the advantage of continuous and automatic delivery of stimulation therapy requires a closed-loop brain-machine interfacing (BMI) system, which should have the capability of monitoring brain activities chronically and identifying the oncoming seizure onset correctly. There have been numerous seizure detection algorithms, including feature extraction and classification, developed over years for the closed-loop control of neuro-stimulation for epileptic patients [2]. The implementation of the algorithms requires a low-noise front-end circuit and a high-resolution analog-to-digital converter (ADC) for

preconditioning of the signal before it gets to the digital signal processing (DSP) or field-programmable gate array (FPGA) module.

1.2 Literature Review

For the past few decades, many research efforts have been devoted to the epileptic seizure detection algorithms. This review focuses on hardware-efficient algorithms which can fit into battery-powered implantable devices with small area and low-power consumption requirements. Reliable seizure detection requires accurate neural signal feature extraction and classification. Most research groups concentrate on the intracranial electroencephalography (IEEG) as the signal for seizure detection. Compared to scalp EEG, IEEG has three main advantages including 1) a higher signal-to-noise ratio (SNR); 2) a better spatial resolution; 3) allowing direct recording from seizure generating regions [2]. Thus, IEEG signals greatly improve the sensitivity of seizure detection. Efficient seizure detection algorithms will enable closed-loop epilepsy prostheses by stimulating the epileptogenic focus within an early onset stage.

Feature extraction is the signal recording and processing through mathematical computation to form characterizing measures, i.e. feature vectors or variances, which can be classified [2], [6]. Feature classification is a computational process to sort characterizing measures by optimal decision boundary between seizure and non-seizure cases [6]. Over years, a growing number of sensitive and specific seizure detection algorithms have been seen in literature [7]-[11]. Tzallas *et al.* used the time-frequency analysis for the determination of EEG segments containing epileptic seizures and

artificial neural networks (ANN) for the classification [7]. Liang *et al.* combined approximate entropy and spectrum analysis to reduce the detection false rate and applied linear least squares (LLS) to classifying windowed EEGs [8]. Lyapunov exponent for complex analysis has been long developed for effective seizure classification [9], [10]. Recently, wavelet transform and wavelet artificial neural networks (WANN) also emerge for non-stationary feature extraction and classification [11]. Among them, [11] reported the Complementary metal–oxide–semiconductor (CMOS) integrated circuit (IC) implementation of the neural interface and wavelet transforms processor. However, all the above-mentioned works need extensive computational power consumption, and thus are not suitable for battery-powered IPGs.

In past few years, low-power implantable seizure-onset detectors have been proposed to reduce the computational power burden [12], [13]. In [12], the algorithm is based on multi-voltage-window feature extraction and counter-based classification, while [13] has single-voltage window and event-based classification. The total power dissipation is 51 μW for [12] and 350 nW for [13], both of which achieved at least 100 times improvement in power consumption compared with previous reported works. However, [12] suffers from high detection delay due to slow comparators and [13] is limited by sensitivity degradation due to baseline variations. Safi-Harb *et al.* later proposed an improved seizure-onset detector based on single-window dual-path algorithm [14]. Single voltage window has less complexity and allows more immunity to variations in baseline and threshold voltage due to noise and offsets. Dual overlapped time windows effectively reduce detection latency as well. However, offline training is

required for all algorithms proposed in [12]-[14], which exposes them to limited patient selection. Raghunathan *et al.* combined multistage time and frequency analyses optimized for feature extraction that relies on seizure-onset-distinct patterns in lieu of pre-training [15].

However, those aforementioned hardware systems usually suffer from limited seizure detection accuracy due to simple pre-determined thresholds of specific signal parameters resulted from low-order modeling of complex manifestation of physiological processes[12]-[15]. Therefore, data-driven computation which aims to modeling pathological signals based on observing and analyzing data in lieu of modeling the underlying processes has been recently developed for classification by optimized feature boundaries trained by machine-learning on a patient-to-patient basis to simultaneously improve both sensitivity and specificity of detection [16]. Data-driven computation thus leads to a more sophisticated trend for seizure detection implemented on system-on-chip (SOC) by integrating spectrum energy based feature extractor [6]. Yoo *et al.* reported the recent state-of-the-art SOC which achieves the full integration of both seizure extractor and classifier based on support vector machine (SVM) learning to simultaneously minimize off-chip components, reduce system power consumption to microwatt level, and maximize correct detection rate [17].

In recent years, many implantable CMOS closed-loop DBS systems have been reported. Lee *et al.* [18] discussed a closed-loop DBS stimulator for Parkinson's diseases (PD). It consists of 8 neural-amplifier channels and 64 stimulation channels. The chip consumes 271 μW at 1.8 V power supply in 0.18-μm CMOS process. However, it still

needs the off-the-shelf microprocessor (μP) to close the loop. This system is good for PD application, but its 8-bit logarithmic ADC cannot meet the high-resolution (> 12 bits) requirement for seizure applications (Note: the resolution specification for the epileptic DBS system will be discussed in Section 2.2.1). Avestruz *et al.* [19] described a spectral analysis IC for local filed potential (LFP) applications. It has 4 sensing channels with each channel consuming 5 μW at 1.8 V power supply in 0.8 μm CMOS process. But it relies on the off-the-shelf ADC and micro-processor (μP) for closed-loop stimulation. For the purpose of low cost and low power, an on-chip ADC is always desired for the efficient use of integrated DSP power. Medtronic in 2012 reported an implantable closed-loop DBS device for seizure control [20]. It achieves integrations of sensing and classification blocks, but the stimulator is still off-the-shelf. In ISSCC 2012, Chen *et. al.* reported the latest state-of-the-art closed-loop seizure SOC, which achieved fully integration of all building blocks including stimulator, with a total power consumption of 2.8 mW in 0.18-um CMOS process [21].

The seizure detection systems for closed-loop application reported to date mainly concentrate on IEEG signals at low frequency (< 100 Hz) [8], [14], [20], [21]. It is also worth noting that [8] and [14] are only PCB implementations yet. The correlation of low-frequency EEG signals with seizure onsets is complicated by flicker-noise filtering and patient-specified feature extraction [6]. Researches also show that low-frequency IEEG detection does not give clear enough information about seizure onset locations [22]. Recently reported clinical trials [23]-[27] show that a certain type of brain wave termed fast ripple (FR) could provide a simplified alternative way to reliable seizure

detection, since it resides in higher signal band (> 250 Hz), *i.e.*, less prone to flicker noise, and may provide more universal seizure-onset indications than the EEG does by possibly avoiding patient-specific training. Increasing evidence shows that the rate of FR is much higher within seizure onset zone than lower-frequency ripples [23], [25]. FR has also been visually identified near the time of seizure onset from implanted electrodes in epileptogenic zones [27]. Past researches [23]-[27] prove FR as a good indicator to seizure onset zone and a promising precursor to seizure onset time as well. Thus, this research focuses on the FR detection.

In this dissertation, a closed-loop seizure stimulator is discussed to provide a top-level system overview where the proposed FR-detection channel can play a critical role. The scope of this PhD work is on the development of a FR-based seizure detection technique. The future goal of this work could involve the development of an implanted system that can catch FR seizure precursors, send warnings and then tranquilize through stimulations the real seizure before it spreads. To the best of author's knowledge, as of today, there is no seizure closed-loop DBS system commercially available yet.

1.3 System Overview

There are many challenges associated with the design of a power-efficient closed-loop seizure stimulator. 1) To extend the recharge interval of battery and allocate enough power to the stimulation circuitry, a good power scheme needs to be developed to save power from other main building blocks, such as the front end, ADC and DSP. 2) For the reliable recording of bio-signals, the total input-referred noise of the front-end

circuit should be lower than the typical extracellular neural background noise of 5-10 μV_{rms} [28]. 3) The front end should be able to reject any electrode-tissue interface induced DC offsets. 4) Reliable DSP algorithm should be developed for the detection of FR patterns and the controlling of stimulation parameters. 5) The system is required to reject the stimulation artifacts that may saturate the neural amplifiers.

To address the aforementioned challenges, a closed-loop DBS system is proposed. Fig. 1.2 shows the system block diagram. The system consists of 16 sensing and stimulation channels, which share the same electrodes. The number of 16 is chosen to accommodate the existing 16-channel simulator in the Boston Scientific Precision SCS® platform. The front end is composed of sixteen low-noise preamplifiers multiplexed to a single bandpass filter (BPF). The preamplifier is designed to provide a 40-dB DC gain, upto 5-kHz bandwidth (BW), and 6-μV_{rms} input referred noise. The BPF is a 6^{th}-order follow-the-leader feedback (FLF) elliptic filter with designed passband from 250 Hz-500 Hz, out-of-band rolloff of -110 dB/decade, and in-band ripple of 0.5 dB. The occurrence of seizure is random. It may start developing minutes, hours, or even days before the seizure onset [29]. Therefore, the front end (preamplifier + BPF) needs to monitor the brain activity continuously. Besides, multiple channels are usually desired for multiple electrodes. Therefore, micro-watt power is often required for each front-end channel.

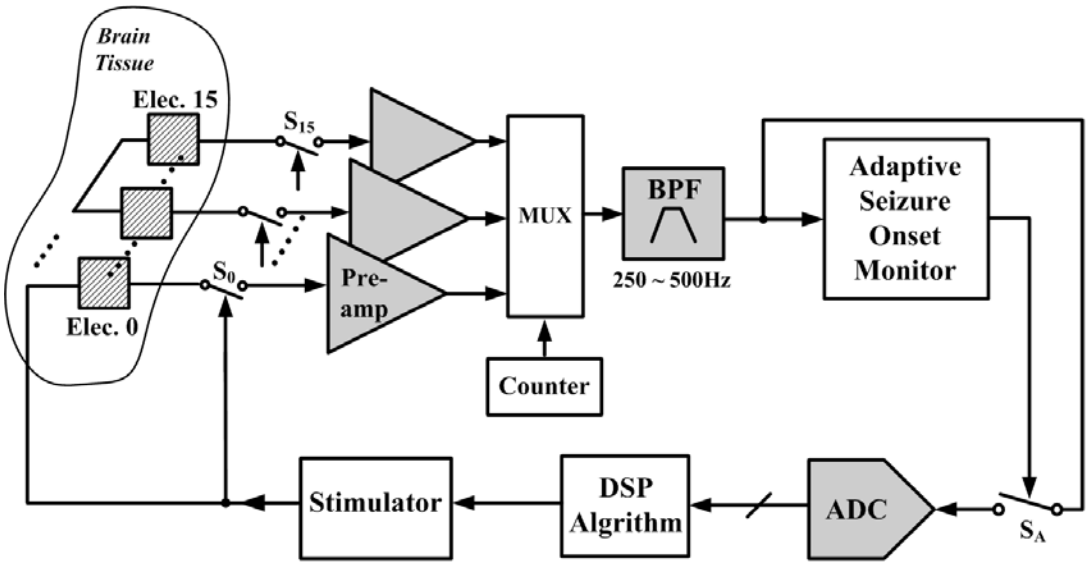

Fig. 1.2. Block diagram of the proposed closed-loop system.

The ADC and DSP can be time-multiplexed to reduce power consumption, which indicates that they are turned on only when the front end sees an FR energy burst, and for the rest of the time, they are in sleep mode. Thanks to the time multiplexing, milli-watt power consumption is reasonable for the ADC and DSP blocks. The ADC resolution is required to be 14 bits (as discussed in Section 2.2.1). An analog low-power seizure-onset monitor can be incorporated for the loop control. The monitor extracts the energy of incoming FR signals. The energy extraction can be done by a Gilbert multiplier which consumes only sub-micro power for this application. If the energy exceeds a certain threshold, switch S_A closes and meanwhile both ADC and DSP are turned on. To avoid false decision, the threshold should be adaptive to the background-noise fluctuation [30]. For human temporal-lobe seizures, the focal time is about 20 seconds before the seizure spreads to other brain areas [26]. Therefore, the ADC will

have enough time to digitize the incoming signal burst and DSP to figure out the optimal stimulation parameters for the patient. A scheme of "non-overlap sensing and stimulation" is used. When the stimulator delivers stimulation pulses, the sensing channels are isolated from the electrodes ($S_0 - S_{15}$ off). Sensing is active ($S_0 - S_{15}$ on) only when stimulation is off. The stimulation artifact issue is therefore alleviated by using this scheme. The specifications for building blocks are summarized in Table 1.1.

Table 1.1. Specifications of building blocks

Preamplifier		BPF		ADC	
Gain	40 dB	Passband	250 - 500 Hz	Resolution	14 bits
Noise	< 10 uV	In-band Ripple	< 0.5 dB	Max Bandwidth	5 kHz
Max Bandwidth	5 kHz	Rolloff	-33 dB /octave	Reconfigur-able	Yes
Power	< 5 uW	Power	< 5uW	Power	< 3 mW

1.4 Research Contribution

This research investigates a new seizure detection scheme based on FR-signal detection, which can be an essential part of a proposed closed-loop seizure-control DBS system. The main contributions of this work include two challenging building blocks in the seizure detection circuit. They are the front-end circuit (preamp + BPF) and the ADC, both gray colored in Fig. 1.2, with focuses on low-power low-noise neural amplifier design, power-efficient high-order filtering methods, configurable analog

modulation techniques, and area-power-saving decimation methodologies. The main contributions of this work are summarized as following:

1) Proposed a micropower low-noise neural recording front-end circuit for epileptic seizure detection. To the authors' knowledge, the proposed epileptic seizure-detection front end is the first to achieve the FR-recording functionality. The circuit achieves one of the best power-noise efficiencies among the literature.
2) Proposed a low-power configurable neural-signal recording system for seizure detection. The system consists of the aforementioned front-end circuit and a sigma-delta ADC with scalable bandwidth and power consumption. The proposed ADC features a fully integrated decimation filter with improved power and area efficiency compared to state-of-the-arts.

1.5 Dissertation Organization

Chapter I gives a research background overview, provides a literature review of epileptic seizure detection, and discusses the top-level system view of this application. Chapter II presents the design methodology for a low-power configurable neural recording system suitable for epileptic seizure detection. Chapter III describes the proposed micropower low-noise neural recording front-end circuit, with experimental verification through a test chip fabricated in XFab 0.6-μm CMOS process. Chapter IV describes the proposed low-power high-resolution neural ADC, with experimental results from the prototype chip implemented in XFab 0.6-μm CMOS process. Chapter V

discusses both bench-top measurement and saline-solution test results for the complete neural recording channel. Chapter VI summarizes this research and discusses the future work.

CHAPTER II

PROPOSED LOW-POWER CONFIGURABLE NEURAL RECORDING SYSTEM FOR EPILEPTIC SEIZURE DETECTION *

2.1 Introduction

Recently, deep brain stimulation (DBS) has been emerging as a promising way of treating patients with neurological conditions ranging from Parkinson's disease [31], [32], depression [33], [34], and epilepsy [3], [4]. The detection of brain activities is required for the reliable delivery of stimulation therapy. Smart and miniaturized implantable devices with capability of capturing neural information from the brain are becoming important aids to neurosurgeons. Successes in acquiring of neural action potential (AP) signals and various electroencephalography (EEG) signals have been achieved by integrated sensor interface systems [35], [36]. Among the new indications, epileptic seizure detection poses stringent challenges for the low-power low-noise integrated neural recording of brain potentials due to the unpredictable sudden occurrence of seizures. Recently, micropower EEG CMOS acquisition systems for chronic seizure detection have been developed [6], [37], [38]. Although EEG has the advantage that it is noninvasive, its correlation with seizure onsets is complicated by flicker-noise filtering and patient-specified feature extraction [6].

Intracranial Electroencephalography (IEEG) or Electrocorticography (ECoG) could provide a simplified alternative way to reliable seizure detection, since it resides in higher signal band (*i.e.*, less prone to flicker noise), and may provide more universal seizure-onset indications than the EEG does. Recent evidence shows that a certain type of high-frequency oscillation termed fast ripple (FR) recorded in hippocampus area of epileptic patients is strongly associated with epileptic seizure onset [23]-[25]. It is widely recognized that FR is an indication to localize the epileptogenic focus (i.e., seizure onset zone) in mesial temporal lobe and neocortical seizures [23]-[25]. Further clinical evidence shows that FR can also be a precursor to the electrographic seizure onset time. FR has been visually identified near the time of seizure onset from implanted electrodes in epileptogenic zones [27]. FR can be recorded by IEEG and may provide valuable information for seizure onset detection. The energy of FR lies mainly within the 250 - 500 Hz frequency range. The amplitude varies from 30 μV to 1.5 mV depending on the electrode size used in IEEG recording [24], [25], [27], [39].

Besides, it is desirable for this system to have the capability of processing neural action potentials as well. We do not intend to have action potential as a seizure precursor. The AP signal is recorded because 1) the analysis of AP signals provides useful information for the positioning of DBS electrodes to the right target inside patient's brain; 2) it could also give neurophysicians a unique opportunity to learn directly the pathological properties of targeted neurons [40], [41]; and 3) it is for the demonstration of the system's capability of sensing higher frequency neural signals.

Typical extracellular neural action potentials have amplitudes in the range of 50 μV–1 mV, with frequency band ranging 100 Hz to > 1 kHz [42], [43].

In this work, we discuss a fully integrated low-power configurable neural recording system designed to demonstrate the functionality of a complete channel for epileptic seizure detection. This prototype chip is capable of sensing both FR and AP signal with 13-bit resolution to fulfill the clinical requirements as discussed in Section 2.2.1. The ADC power consumption is scalable with the signal bandwidth (BW) to make the system more energy efficient. Our goal for this prototype system is to capture FR signal at the seizure onset time through *in-vitro* test. The integration of a wireless communication block is essential for *in-vivo* testing for an implantable device, but it is out of the scope of this chapter. This chapter is organized as follows. Section 2.2 describes the system-level design and considerations of this neural interface circuit. Section 2.3 concludes the chapter. We have previously reported the neural front-end circuit design in [44], its discussion will be presented in Chapter III.

2.2 System-Level Design

Over the past few years, there have been intensive research efforts on developing neural acquisition ICs for neural spikes and/or local field potentials (LFP). Avestruz *et al.* [19] described a spectral analysis IC for LFP applications, but it relies on the off-the-shelf ADC for the signal recording. For the purposes of low cost and low power, an on-chip ADC is always desired for the efficient use of integrated DSP power. Muller *et al.* [45] presented a DC-coupled neural recording system for spike detection. It is composed

of the ADC, digital lowpass filter and DAC in a servo-loop to suppress the DC offset and LFP. It achieves small area for each channel. However, the power hungry digital filter for offset and LFP attenuation is implemented off-chip on an FPGA. Lee *et al.* [18] proposed an 8-channel neural signal chain for both AP and LFP recording, but the logarithmic ADC only has 8-bit resolution, which is not enough for the epileptic seizure detection. Verma *et al*. [6] presented a micro-power CMOS bio-potential acquisition system for chronic seizure detection, but it is susceptible to noise folding due to non-idealities in anti-aliasing filters. In this research, we propose a neural recording system with full integration and high resolution suitable for implantable seizure detection. The required system specifications for the proposed system, in terms of resolution and power, are discussed in the following section.

2.2.1 System Specifications

For both AP and LFP applications, the desired dynamic range can be higher than 60 dB, corresponding to μV level of input-referred noise for the front-end circuit and high resolution for the ADC [35]. For the seizure detection, particularly, the resolution requirement is derived from two aspects: 1) For the localization of DBS electrodes, AP signals captured by one guiding microwire may come from different neurons, high ADC resolution (> 10 bits) is needed to distinguish various signal sources, as well as the movement-related signal changes [46]. 2) For seizure onset detection, at least 12-bit resolution is required to extract correct FR signal patterns [23], [24]. In addition, the feature extraction accuracy in the digital domain improves as the resolution of ADC

increases to at least 10 bits [6]. This greater than 10 bits resolution is the minimum requirement to achieve acceptable false positive rate, even though the SNR of original IEEG signal is usually less than 15 dB [47]. Considering resolution loss due to various static or dynamic errors, the ADC design target is set to be higher than 14 bits.

The power specifications for such a system are discussed below. Since seizures may start developing minutes, hours, or even days before their occurrences [24], [25], the integrated front-end circuit must monitor for prolonged periods. Besides, a multi-channel system is usually desired for multiple electrodes. Therefore, micro-watt power is often required for each front-end channel. On the back end, an ADC can be shared by multiple channels on an interrupt-based manner to minimize the power and area overhead. The ADC wakes up briefly and digitizes the signal, only when the front end senses a seizure burst. An analog low-power seizure-onset monitor can be developed to control the ADC. The monitor extracts the energy of incoming FR signals. The energy extraction can be done by a Gilbert multiplier which consumes only sub-micro power for this application. If the energy exceeds a certain threshold, the ADC will be turned on. To avoid false decision, the threshold should be adaptive to the background-noise fluctuation [30]. For human temporal-lobe seizures, the focal time is about 20 seconds before the seizure spreads to other brain areas [26]. Therefore, the ADC will have enough time to response. For the seizure-quiet time, the ADC can be put in sleep mode. Thus, milli-watt power consumption is reasonable for the ADC.

2.2.2 System Architecture

The proposed epileptic seizure recording system consists of a front-end circuit including preamplifier and bandpass filter (BPF), a single-to-differential converter circuit and a sigma-delta ADC (including analog modulator and decimation filter). We have discussed the front end in a previous paper [44]. We briefly discuss it here for completeness. We focus in this chapter on the design considerations and details of a low-power neural ADC, especially on the decimation filter as a part of the ADC. Fig. 2.1 shows the system block diagram.

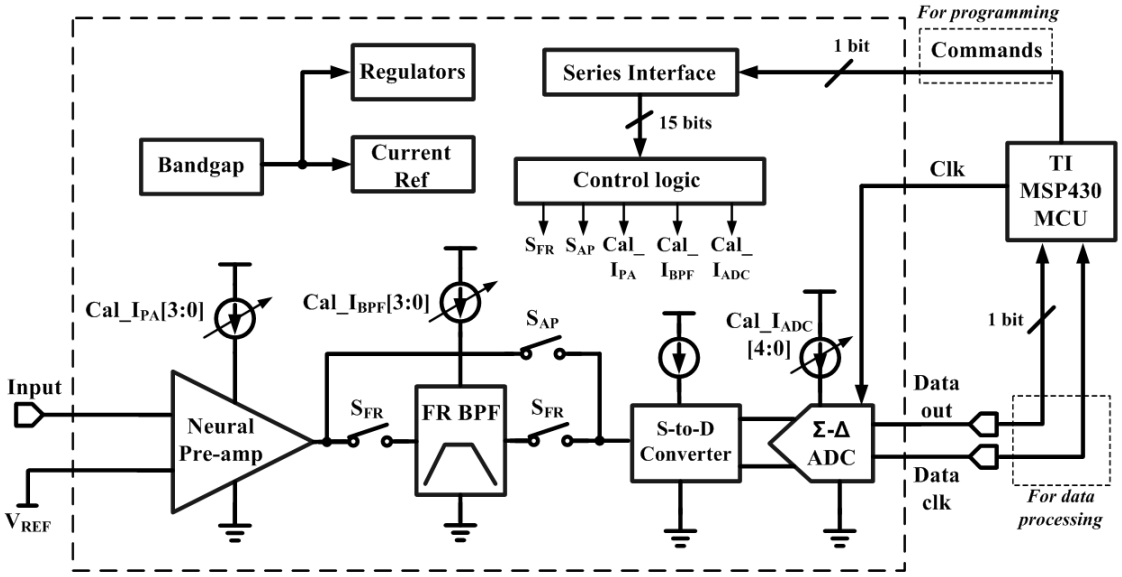

Fig. 2.1. System block diagram of the proposed neural recording system.

The integrated peripheral circuits include a bandgap circuit, two linear voltage regulators for separate analog and digital power supplies, and a current reference circuit to provide bias currents throughout the entire chip. Additionally, a series interface

accepts the 15-bit commands from an external microprocessor unit (MCU) and generates the control bits through the control logic for the chip configuration. The communication with the MCU is based on the standard series peripheral interface (SPI) protocol. The series interface is only activated for a brief period of time (~ 20 μs) based on the chip-select (CS) signal from the MCU, when the system initially turns on. It gets deactivated right after the chip configuration, therefore consumes little power. The MCU provides the clock to drive the ADC, thus it can easily program the ADC's sampling frequency (f_s). The MCU also fetches the ADC data at the speed defined by the data clock. The data is then stored in the MCU memory for post data processing.

The binary-weighted PMOS current DACs are designed to adjust the bias current of analog blocks. For example, $Cal\_I_{PA}[3:0]$, $Cal\_I_{BPF}[3:0]$ and $Cal\_I_{ADC}[4:0]$ are the control bits for the tuning of the preamplifier, BPF and ADC, respectively. The unit current branch is 2 nA for both Cal_I_{PA} and Cal_I_{BPF} DACs and 80 nA for the Cal_I_{ADC} DAC. The switches S_{AP} and S_{FR} select the signal paths for action-potential (AP) and fast-ripple (FR) applications, respectively. The preamplifier provides a DC gain of ~40 dB. The BPF (250 – 500 Hz) is dedicated to the extraction of FR signals. In FR mode, the signal goes through both the preamplifier and BPF. In AP mode, the signal bypasses the BPF, which is shut off by setting $Cal\_I_{BPF}[3:0]$ all high. In both modes, the ADC finally digitizes the signal. Since the AP signal is recorded for guiding the placement of DBS electrodes in this application, it can be digitally bandpass filtered during the on-line data processing by the dedicated physiology system that monitors the electrode position, if necessary [48].

For different neural applications, the BW requirements are different. With the ADC's oversampling ratio (OSR) fixed, the BW and power consumption of the decimation filter can scale with the sampling frequency. The bias current for each OTA in the sigma-delta modulator can also scale accordingly through the settings of $Cal\_I_{ADC}[4:0]$, since OTAs are the only blocks consuming static power in the ADC. For the OTA power configuration, $Cal\_I_{ADC}[4:0]$ is set as [11110] for FR mode (I_{bias} = 2.5 μA) and [11011] for AP mode (I_{bias} = 10 μA). Note the PMOS DAC is low-bit active.

A single-to-differential (S-to-D) converter converts the single-ended signal from the front-end circuit to differential signals, since the ADC processes signal differentially and is robust to any common-mode errors. Differential ADC also achieves superior linearity and better matching against process variations than the single-ended version. The S-to-D converter also drives the capacitive sample-and-hold in the ADC. Fig. 2.2 shows the schematic of the circuit.

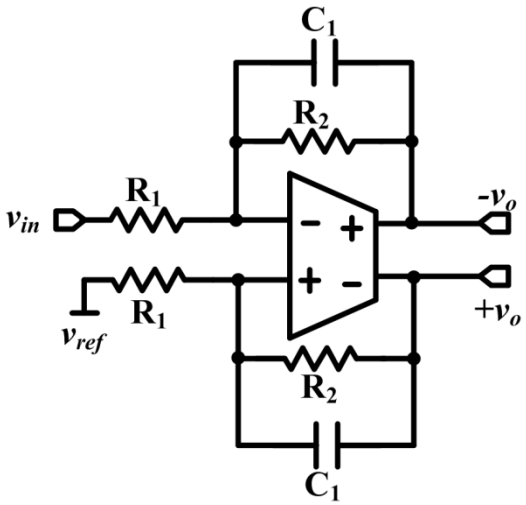

Fig. 2.2. Schematic of the single-to-differential converter.

Since it has a much smaller impact on noise than the front-end circuit, its power consumption is negligible. The transfer function can be computed as $v_o/v_{in} = R_2/[2R_1(1+sR_2C_1)]$. By choosing $R_2 = 2R_1$, the input v_{in} is converted into the differential signals with the same amplitude as $|v_{in}|$ in signal band. Concurrently, the pole at $(R_2C_1)^{-1}$ provides the first-order low-pass anti-aliasing filtering. The front-end circuit consists of two building blocks, the preamplifier and the bandpass filter, and achieves good power-noise efficiency. Design considerations and analysis of the front end are given in Chapter III.

2.3 Conclusions

This chapter has demonstrated a configurable neural recording system capable of the acquisition and digitization of both neural-spike and fast-ripple signals. Specifications of the building blocks are determined through system-level analysis. Front-end circuit and ADC designs will be discussed in Chapter III and IV, respectively. The integrated SPI interface allows for the possibility of integrating the system with any future digital control or DSP blocks through standard buses. This prototype circuit can be extended to a multi-channel system, with the ADC shared by all channels, as the sensing part of a future closed-loop DBS system for the treatment of intractable epilepsy.

CHAPTER III

PROPOSED MICROPOWER LOW-NOISE NEURAL RECORDING FRONT-END CIRCUIT FOR EPILEPTIC SEIZURE DETECTION *

3.1 Introduction

Roughly 50 million people suffer from epilepsy worldwide. Among them about one third have seizures that are not controlled by medication [1]. Brain stimulation may provide an effective way of controlling intractable epileptic seizures [3], [4]. One difficulty of realizing such stimulation therapy lies in reliable seizure onset detection. In current state of the art, clinical determination of seizure onset time still relies on an epileptologist's visual inspection of patients' electroencephalogram (EEG) recordings [22], [49]. Recently, researchers have attempted to design implantable deep-brain-stimulation (DBS) devices with automated brain activity detection capabilities [19], [50].

Evidence increasingly shows that a certain type of high-frequency oscillation termed fast ripple (FR) recorded in hippocampus area of epileptic patients is strongly associated with epileptic seizure onset [23]–[25]. FR can be recorded by intracranial electroencephalography (IEEG) and may provide valuable information for seizure detection. The energy of FR lies mainly within the 250 - 500 Hz range.

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The FR amplitude varies from 30 μV to 1.5 mV depending on electrode size used in IEEG recording [24]–[27], [39]. Since seizures may start developing minutes, hours, or even days before their occurrences [29], the integrated front-end circuit must monitor for prolonged periods, requiring ultra-low power. The neural front end must boost these weak neural signals before any further signal processing can be performed. Meanwhile the total input-referred noise of the amplifier should be lower than the typical extracellular neural background noise of 5-10 μV_{rms} [28]. Since the amplifier power is inversely proportional to $\overline{v_{ni}^2}$, where $\overline{v_{ni}^2}$ is the input-referred noise power spectral density (PSD), the noise-power tradeoff must be well balanced throughout the design.

In this chapter, we present a fully integrated low-power low-noise CMOS front-end circuit designed for recording epileptic fast ripples. The functionality of recording action potentials is added in the system chip and the measurement results are discussed in Section 5.3.1. Section 3.2 describes system-level design and considerations for the front-end circuit. Section 3.3 discusses the operational transconductance amplifier (OTA) design to achieve a good noise-power tradeoff. Section 3.4 describes the design of a 6th order elliptic bandpass filter (BPF) with passband specified as 250 – 500 Hz. Section 3.5 presents experimental results and saline-solution test results of the front-end circuit, and Section 3.6 concludes this chapter.

3.2 Overall System Architecture

The whole neural front-end circuit consists of two stages, the preamplifier stage and the bandpass filter stage, as shown in Fig. 3.1. The preamplifier has a capacitive

feedback configuration similar to the topology in [51], [42]. Two identical MOS-bipolar pseudoresistors [52] consisting of transistors M_{b1}–M_{b2} and M_{b3}–M_{b4} provide extremely high on-chip incremental resistance R_H (>10^{12} Ω). The design procedure is shown below.

1) From the desired gain of 40 dB, we choose feedback capacitor C_f value of 0.2 pF, thus input capacitance C_s is calculated as 20 pF.

2) R_H combined with C_f creates a low-frequency highpass pole f_h ($= (2\pi R_H C_f)^{-1} = 0.36$ Hz) that blocks the DC offset induced by the electrode-tissue interface while passing the neural signals of interest. A low f_h is designed to prevent the pseudoresistor noise from coupling to the front-end output (as explained later in this section).

3) The OTA noise ($v_{n,OTA}$) gets coupled to the preamplifier output by a gain of $A_n = 1+sC_s/(sC_f+R_H^{-1})$ and corrupts signals, thus the OTA noise needs to be minimized as discussed in Section 3.3.

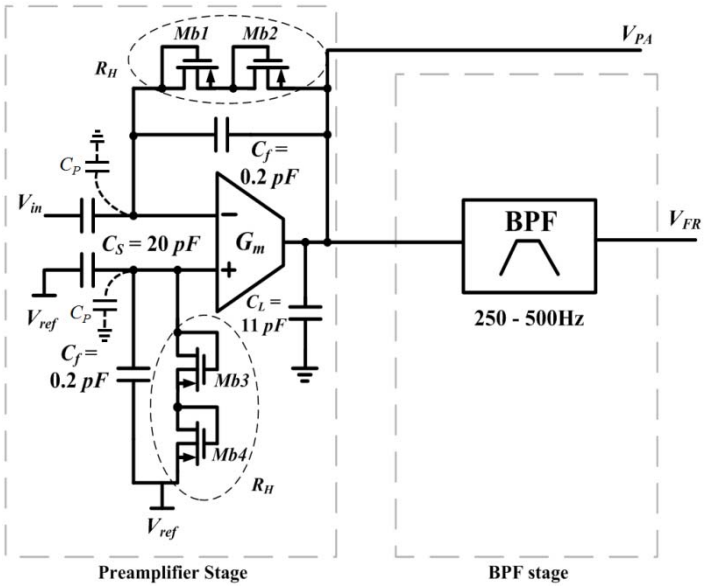

Fig. 3.1. System block diagram of the proposed neural front-end circuit.

As shown later in this section, the front-end gain is C_s/C_f, where C_s is the preamplifier input capacitor. The noise transfer function (NTF) of the pseudoresistor [53] within the signal band is approximately

$$NTF = \frac{\overline{v_{no,R_H}}}{\overline{i_{n,R_H}}} = \frac{1}{sC_s} \cdot \frac{C_s}{C_f} = \left. \frac{1}{j2\pi f C_f} \right|_{s=j2\pi f}, \tag{3.1}$$

where $\overline{v_{no,R_H}}$ is the voltage noise density of R_H at the front-end output and $\overline{i_{n,R_H}}$ is the current noise density of R_H, with $\overline{i_{n,R_H}^2} = 4kT/R_H$, where k is Boltzmann's constant (= 1.38 E-23 $J \cdot K^{-1}$) and T is the absolute temperature. Our preamplifier drives a bandpass filter, which limits the noise bandwidth (see Section 3.4 for more discussion of filter operation). Since the BPF is designed with a narrow bandwidth B (250 – 500 Hz), the integrated voltage noise of R_H at the front-end output is approximated as

$$V_{no,rms,R_H} = \sqrt{\int_B \overline{i_{n,R_H}^2} \cdot |NTF|^2} \cong \sqrt{\frac{kTB}{R_H}} \cdot \frac{1}{\pi \, f_{o,BPF} C_f}, \tag{3.2}$$

where $f_{o,BPF}$ is the center frequency of the BPF. Equation (3.2) shows that a high R_H (i.e., f_h is low) reduces the pseudoresistor noise. A high R_H also reduces the loading to the OTA. It is worth mentioning that for many other neural applications such as electrocardiography (ECG), local field potential (LFP) and surface EEG, there is useful information lying between 0.1 Hz and 1 kHz [35]. Though this front-end circuit is dedicated to the FR recording, a low f_h makes the preamplifier itself also useful in other applications. The final device will be a battery-driven implant encapsulated in a well-shielded metal case, so it will not pick up any low-frequency power-line interferers. The symmetrical loading on the positive input of the OTA makes the circuit symmetrical and

robust to common-mode input. Additionally, the pseudoresistors provide the necessary DC resistive feedback to bias the OTA. One drawback of the pseudoresistor is that its resistance (R_H) varies with large voltage swing across it. The R_H variation is about 10 times with ±200 mV voltage difference across it [51]. This may create signal distortion. Fortunately, with small input amplitude (< 1.5 mV), the distortion is tolerable for this application. In other words, since f_h is extremely lower than FR frequency (0.36 Hz *v.s.* 500 Hz), a 10-time variation on f_h will not affect FR signal much.

Since the preamplifier stage is in closed loop with capacitive feedback, we can open the loop as shown in Fig. 3.2 to analyze the loop gain, where v_t is the applied test signal and v_r is the return signal. By solving the KCL nodal equation and neglecting R_H, since $R_H C_f >> R_o C_L$, the loop gain $T(s)$ can be approximated as

$$T(s) = -\frac{v_r}{v_t} \cong \frac{G_m \beta R_o}{1 + sR_o C_{Ltot}}, \tag{3.3}$$

where G_m and R_o are the OTA transconductance and output resistance, respectively; $\beta = C_f/(C_f + C_s + C_p)$ is the capacitive divider feedback factor and C_p is the OTA input parasitic capacitance; $C_{Ltot} = C_L + (1-\beta)C_f$ is the effective total load capacitance and C_L is the load capacitor.

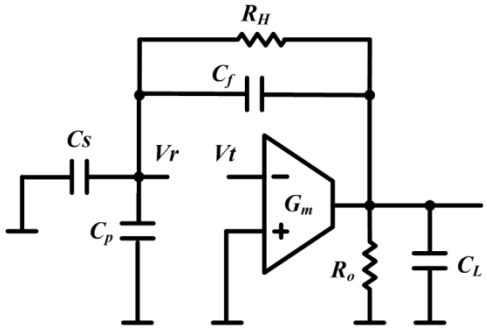

Fig. 3.2. Open-loop configuration of the gain stage.

The simplified amplifier model in Fig. 3.2 assumes that the source impedance is low. Seizure-detecting macroelectrodes usually render a finite electrode/tissue impedance ~ 200 – 500 Ω in this application [39]. It can be modeled as a resistor R_s in series with C_s at the amplifier input. With the impact of this source impedance, (3.3) can be modified as

$$T(s) = \frac{G_m \beta R_o (1 + sR_s C_s)}{1 + sR_o \left[C_{Ltot} + \frac{R_s}{R_o} \frac{C_s (C_p + C_f)}{(C_p + C_f + C_s)} \right]} \quad . \tag{3.4}$$

With the value of R_s < 500 Ω, the added zero f_z (= $(2\pi R_s Cs)^{-1}$ = *16 MHz*) is far beyond the signal band. Since $R_s << R_o$ (~ GΩs), the additional term in the denominator is much less than C_{Ltot}. Therefore, this source impedance has negligible impact on the amplifier transfer function.

When closing the loop, considering the highpass pole introduced by R_H and C_f and assuming the DC loop gain $G_m \beta R_o >> 1$, the preamplifier's transfer function yields

$$H(s) = \frac{V_{PA}(s)}{V_{in}(s)} = -\frac{C_s}{C_f + (sR_H)^{-1}} \frac{T(s)}{1 + T(s)} = -\frac{C_s}{C_f} \frac{1}{1 + s(C_{Ltot} / \beta G_m)} \frac{sR_H C_f}{1 + sR_H C_f} . \tag{3.5}$$

The ratio C_s/C_f determines the midband gain. The highpass cutoff frequency is at $1/(R_H C_f)$ and lowpass cutoff frequency is at $\beta G_m / C_{Ltot}$. The dominant noise source ($\overline{v_{ni,OTA}^2}$) in this design is the OTA, and the input-referred noise of the preamplifier is

$$\overline{v_{ni,amp}^2} = \overline{v_{ni,OTA}^2} \cdot \frac{(C_s + C_f + C_p)^2}{C_s^2} . \tag{3.6}$$

Increasing the input transistor size reduces flicker noise but also increases C_p, which in turn compromises the input-referred noise of the overall system. Besides, an increased

C_p decreases β, and thus reduces the loop gain. An optimized input gate size should be found to obtain a good compromise between these mentioned tradeoffs.

A bandpass filter follows the gain stage to process FR signals. To the best of our knowledge, most biopotential amplifiers published to date [42], [35] and [54] rely only on 1st-order RC filters that provide at most 6 dB/octave attenuation, which is insufficient for FR signal processing [23]. Epileptic patients' brain waves usually contain oscillations ranging 80 – 500 Hz. Oscillations between 80 – 200 Hz, termed ripples, have the same order of amplitude as FRs, but are not related to epileptic focus [25]. This ripple power must be sufficiently attenuated (at least 10 – 30 dB attenuation in 80 – 200 Hz) by a filter to render a good signal-to-noise ratio (SNR) for FRs [23], [25]. Therefore, modern clinical intracranial EEG recording for epileptic applications requires -33 dB/octave (-110 dB/decade) filter rolloff [23], [25]. This specifies that, in this application, the filter should be at least 6th order [55]. The filter's upper rolloff is required to attenuate interferers above 500 Hz, such as epileptiform interictal spikes (~ 5 kHz) [23]. Since this high-frequency power is far away from the signal band, the rolloff requirement is not as stringent as that for the ripple power. Thus, the 6th order specification is mainly determined by the lower rolloff. This filter along with the preamplifier will be a part of a future integrated micropower analog seizure-warning system.

3.3 Low-Power Low-Noise OTA Design

In this section, we discuss the design strategies to achieve the low-power and low-noise OTA for neural recording.

3.3.1 Noise Limit of a Differential Pair in Subthreshold Region

As mentioned in Section 3.1, this neural front end must continuously monitor epileptic brain activities. The front end must consume minimal power to budget for subsequent blocks in the DBS system. Besides, the multi-channel applications also require low power consumption for each channel. As mentioned before, the typical extracellular neural background noise is on the order of 5–10 μV_{rms}. To achieve a good noise-power tradeoff, we first investigate the theoretical noise limit of a differential-input amplifier at a certain bias-current level. Using the EKV model [56], the MOS transconductance g_m in saturation is

$$g_m = \frac{\kappa\, I_D}{U_T} \frac{2}{1+\sqrt{1+4\cdot IC}}. \tag{3.7}$$

A similar expression exists using the "one equation all region" or ACM model [57], [58]. In (3.7), κ is the subthreshold slope factor of approximately 0.7 [59], U_T is the thermal voltage of 26 mV at room temperature of 300 K, and I_D is the drain current. IC is the inversion coefficient and is defined as the ratio of drain current I_D to the moderate inversion characteristic current I_S of a MOS transistor, given by $IC=I_D /I_S = I_D /(2\mu C_{ox}U_T^2 W/ \kappa L)$ [57], [60] where μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W is the transistor width, and L denotes the effective channel length. $IC <$

0.1 indicates roughly weak inversion, *0.1 < IC < 10* moderate inversion, and *IC > 10* strong inversion. Low noise design is basically targeted to maximize the input transconductance and minimize the input-referred noise due to all other noise sources, such as load transistors and resistors, at a given power. We bias our input transistors in deep subthreshold region with an *IC* value of about 0.02, so

$$g_m \approx \frac{\kappa\, I_D}{U_T}. \tag{3.8}$$

Note that subthreshold operation trades speed and linearity for power efficiency. It is well suited for this application with low signal frequency and amplitude, but high demand for noise. The subthreshold MOSFET's current-noise PSD can be modeled [51], [60] as

$$\overline{i_n^2} = 4kT\frac{1}{2\kappa}g_m = 2kT\frac{I_D}{U_T}. \tag{3.9}$$

Based on (3.8) and (3.9), we can derive the input-referred noise PSD of an ideal subthreshold differential pair as

$$\overline{v_{ni}^2} = 2\frac{\overline{i_n^2}}{g_m^2} = 4kT\cdot\frac{U_T}{\kappa^2\, I_B}, \tag{3.10}$$

where I_B is the bias current for each transistor in the differential pair. This neural preamplifier is designed to consume less than 1 μA total current. The partitioned bias current to the differential input pair is $2I_B$ (= 800 nA). Equation (3.10) indicates that an input-referred voltage noise of 48 nV/√Hz at 300 K is the theoretical noise limit of a differential-input amplifier biased in subthreshold region with the target current level of 800 nA.

3.3.2 OTA Topology for Low-noise Low-power Design

Recently, various OTA topologies have been explored to get a low noise and high power efficiency. The one-stage OTA with three current mirrors is among the popular OTA topologies for low-noise neural amplifier design [51], [54] and [61]. This OTA topology can achieve a wide output swing but relatively low gain. Cascode transistors are added to the output branch to enhance gain at the cost of reduced output swing [51], [54]. Nevertheless, this OTA topology itself is not very power efficient, since the current mirrors both contribute noise and consume power. The reported NEF (see Section 3.3.5 for definition) is limited to 4 – 5 for this OTA topology. The 2-stage OTA can achieve both large gain and wide output swing, but the 2^{nd} stage consumes considerable current to ensure stability, thus limiting the OTA power efficiency. An NEF of 19.4 is reported for a 2-stage OTA-based neural amplifier [62]. Push-pull operation has recently been added to a 2-stage OTA to reduce the output quiescent current and improve the NEF to 3.26 [35]. In contrast, the folded cascode (FC) OTA can reach the theoretical NEF limit (~ 2) of any differential-pair based OTA [42]. The FC OTA can also achieve a good input common-mode range and a reasonably high open-loop gain within one stage. Thus, we choose an FC topology in this design.

The low-noise strategy is to minimize the quiescent currents that do not contribute to the overall transconductance of the OTA, such as the output-branch bias current. Fortunately, the resulting side effect of reduced slew rate is not a main concern here since there is no rapid change of large signals involved in this neural recording application. Wattanapanitch *et al.* in 2007 [42] proposed a large current scaling of 16:1

(input bias current : output-branch current) to a conventional FC structure and achieved a NEF of 2.67 with a bandwidth (BW) of 5.32 kHz and a total current consumption of 2.7 μA. However, such severe current scaling increases the impedance looking into the source of the transistors in the output branch such that it even becomes comparable to the drain resistances of the input transistors and the bottom current-sinking transistors. Thus, the resulting current divider greatly lowers the effective transconductance $G_{m,eff}$ of a conventional FC OTA. To achieve low input-referred noise, it is crucial to maximize the $G_{m,eff}$ of the OTA at a given bias current. To alleviate the problem of $G_{m,eff}$ attenuation, the design in [42] adds cascode transistors to the input transistors, increasing their output impedance but sacrificing headroom.

In this chapter, we adopt a current splitting technique [63], [64] to increase the drain resistances of both input transistors and current-sinking transistors. The current-splitting technique was originally proposed by Bahmani *et al.* [63] in a pseudo-differential OTA, and later adapted by Assaad *et al.* [64] into a fully-differential folded-cascode topology by adding a tail current source and two folded output branches. Both reports' proposed techniques increase the OTA's effective G_m at certain power consumption. In our OTA topology, we combine this current splitting technique with the output-current scaling [42] technique to lower the OTA noise.

Fig. 3.3 shows the proposed OTA schematic, and Fig. 3.4 includes the schematic of a conventional FC OTA without current splitting [42] for comparison. The bias current in each branch is marked on the schematics. In this design, we scale the output-branch bias current to *1/N* of the input bias current. We choose scaling factor $N = 16$ to

achieve a good tradeoff between the reduced output-branch noise and the aforementioned $G_{m,eff}$ attenuation issue. To apply the current-splitting technique, we divide each input transistor M_{P1}-M_{P2} (see Fig. 3.4) of the conventional FC OTA into segments *A/N* and *B/N*, where *A* and *B* are the splitting factors such that $A + B = N$. Thus the currents in M_1, M_4 and in M_9, M_{10} (see Fig. 3.3) are reduced by the ratios of *A/N* and *(A+1)/(N+1)*, respectively, relative to the conventional FC. Note that before current splitting the current in M_{N3}, M_{N4} (see Fig. 3.4) is $(N+1)I_B/N$, while after current splitting the current in M_9, M_{10} (see Fig. 3.3) becomes $(A+1)I_B/N$. Thus, the current is reduced by *(A+1)/(N+1)*. As will be shown later in this section, we choose $A = 8$, so that the currents of M_1, M_4, M_9 and M_{10} (see Fig. 3.3) are halved, and their effective drain resistance is doubled.

Compared to the state-of-art design in [42], the current splitting technique used in our OTA presents two advantages: first, current splitting enhances the drain resistance of both input and bottom transistors without any additional cascoding; second, since M_9–M_{12} are internally biased as shown in Fig. 3.3, current splitting obviates the additional biasing branch M_b along with the source degeneration resistor R_b in Fig. 3.4. Note that R_b is usually much higher than other degeneration resistances, because the current is commonly minimized in biasing branch to save power.

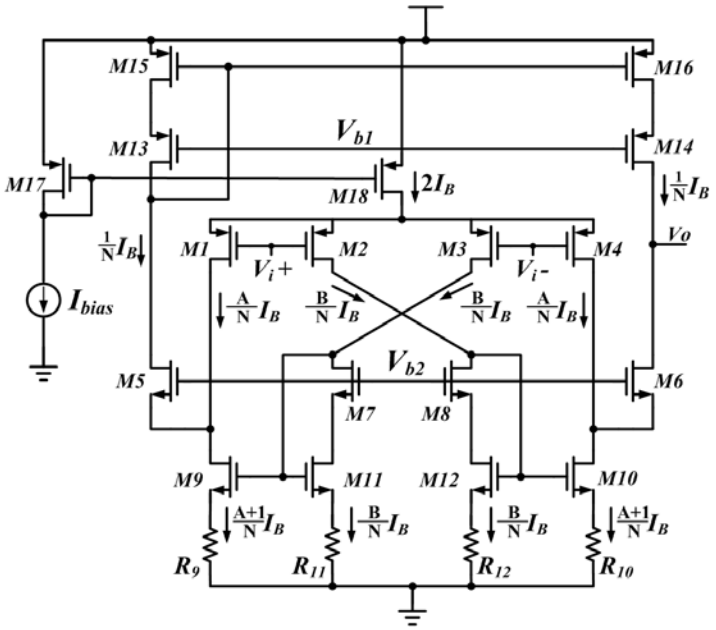

Fig. 3.3. Schematic of the low-noise OTA with both current scaling and current splitting techniques.

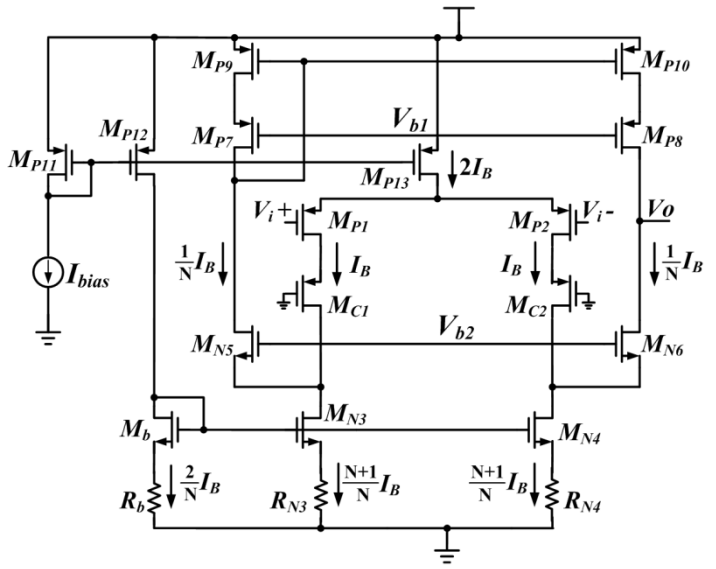

Fig. 3.4. Schematic of a conventional FC OTA without current splitting [42].

In Fig. 3.3, by cross coupling M_2 and M_3, the small-signal current of M_2 adds in phase with the small-signal current of M_4 through the current mirror formed by M_{12} and M_{10}. The same small-signal addition happens in the other half circuit. To compute the total G_m of the OTA, use (3.8) for each input transistor and its corresponding bias current indicated in Fig. 3.3. Assuming all the small-signal currents caused by the differential input go completely through the sources of M_5 and M_6, the ideal transconductance of the current-splitting FC OTA is

$$G_m = \frac{\kappa I_B}{U_T} \cdot \frac{(2A+1)}{N}. \tag{3.11}$$

Equation (3.11) implies that for the same bias current level, we can increase the ideal G_m by merely selecting a larger A value. However, the current noise from M_2 and M_3 scales by $((A+1)/B)^2$ to the output by the current mirroring. Therefore, we need a detailed analysis on the splitting factor and noise tradeoffs to reach an optimal noise-performance point. The input-referred noise PSD of a differential pair with current splitting is

$$\overline{v_{ni,cs}^2} = 2 \cdot \left(\overline{i_{n,M1,4}^2} + \left(\frac{A+1}{B}\right)^2 \overline{i_{n,M2,3}^2} \right) \cdot \frac{1}{G_m^2} = \frac{4kT}{U_T} \left(A + B\left(\frac{A+1}{B}\right)^2 \right) \frac{I_B}{N} \cdot \frac{1}{G_m^2}, \tag{3.12}$$

where $\overline{i_{n,M1,4}^2}$ and $\overline{i_{n,M2,3}^2}$ are the current noise from $M_{1,4}$ and $M_{2,3}$, respectively. Substituting (3.11) into (3.12) and then normalizing by (3.10), the normalized input-referred noise PSD of a current-splitting differential pair yields

$$\overline{v_{ni,normalized}^2} = \frac{\overline{v_{ni,cs}^2}}{\overline{v_{ni}^2}} = N \cdot \frac{A + B\left(\frac{A+1}{B}\right)^2}{(2A+1)^2} = \frac{\frac{A}{N} + \frac{[(1+A)/N]^2}{[1-(A/N)]}}{\left(\frac{1+2A}{N}\right)^2}. \tag{3.13}$$

We plot (3.13) in Fig. 3.5 and find that when $A = 8$, the noise is almost equal to that of a simple differential pair. The ideal G_m is also enhanced by (17/16) times that of a simple differential pair. Therefore, we choose $A = B = 8$. It is seen that the proposed OTA avoids G_m and noise degradation while providing high output resistance of both input and bottom transistors.

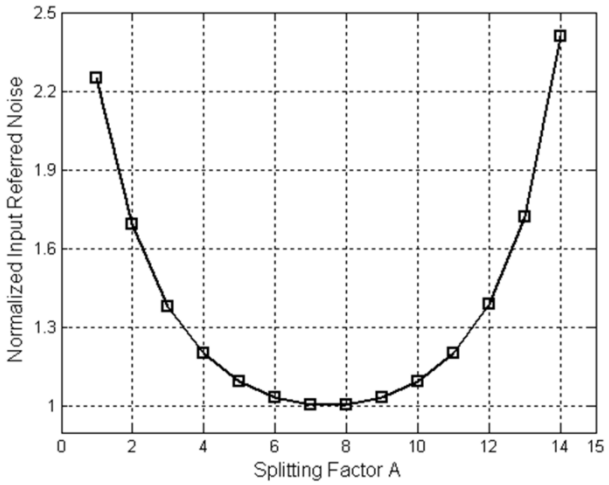

Fig. 3.5. Effect of current splitting technique on the noise of a differential pair.

Equation (3.11) is only valid for ideal components, thus we need to derive the actual non-ideal transconductance. Fig. 3.6 displays the OTA half circuit for the $G_{m,eff}$ calculation. A current divider is formed due to the output-current scaling as mentioned before. It consists of G_{s6}, g_{d4} and G_{d10}, where G_{s6} is the conductance looking into the source of M_6, g_{d4} is the drain conductance of M_4, and G_{d10} is the output conductance of the source-degeneration structure of M_{10}. Since $g_{d10}^{-1} >> R_{10}$, we can derive $G_{d10} = (g_{d10}^{-1} + R_{10} + g_{m10} R_{10} g_{d10}^{-1})^{-1} \approx g_{d10} (1 + g_{m10} R_{10})^{-1}$, where g_{m10} and g_{d10} are the transconductance

and drain conductance of M_{10}, respectively. We choose degeneration factor $g_{m10}R_{10} = 12$ as shown later. The drain of M_6 is at the AC ground, thus $G_{s6} = g_{m6}$, where g_{m6} is the transconductance of M_6. With the effect of this current divider, the effective transconductance transfer functions from M_4 and M_2 to the output are

$$G_{m4} = g_{m4} \cdot \frac{g_{m6}}{g_{m6} + G_{d10} + g_{d4}}, \tag{3.14}$$

$$G_{m2} = g_{m2} \cdot \left(\frac{A+1}{B}\right)\left(\frac{g_{m6}}{g_{m6} + G_{d10} + g_{d4}}\right), \tag{3.15}$$

where g_{m2} and g_{m4} are the transconductance of M_2 and M_4, respectively. By substituting $g_{m4} = \kappa A I_B /(NU_T)$ into (3.14) and $g_{m2} = \kappa B I_B /(NU_T)$ into (3.15) and then adding up (3.14) and (3.15), the effective transconductance of the proposed OTA yields

$$G_{m,eff} = \frac{g_{m6}}{g_{m6} + G_{d10} + g_{d4}} \cdot \frac{\kappa I_B}{U_T}\frac{(2A+1)}{N} = \left(1 - \frac{G_{d10} + g_{d4}}{g_{m6} + G_{d10} + g_{d4}}\right) \cdot G_m . \tag{3.16}$$

Table 3.1 shows the simulated operating points of all main transistors. We compute

$$G_{m,eff} \approx 98\%\ G_m = 1.04\ \frac{\kappa I_B}{U_T}. \tag{3.17}$$

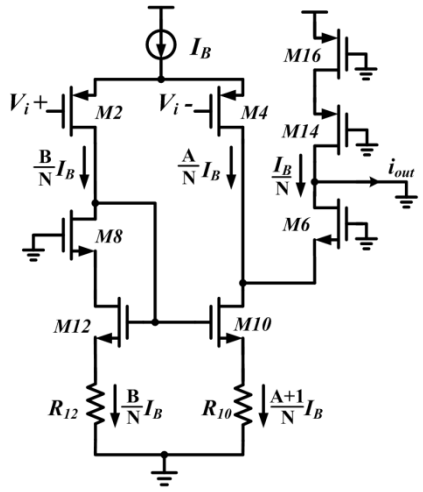

Fig. 3.6. Half circuit of Fig. 3.3 for the effective G_m analysis.

Table 3.1. Operating points for transistors in the OTA with I_{tot} = 872 nA

Devices	***W/L (um)***	g_m ***(μS)***	I_D ***(nA)***	g_m/I_D	g_{out}^* ***(nS)***	***Inversion Coefficient***
M1, M2, M3, M4	240/3	5.36	201.6	26.6	4.7	0.02
M9, M10	45/8	4.35	220.8	19.7	1.9**	0.44
M5, M6	8.0/6.0	0.42	19.2	21.7	0.5	0.25
M15, M16	2.0/2.0	0.29	19.2	15.3	14.7	1.22
M13, M14	2.0/1.0	0.42	19.2	22.1	0.5**	0.22

*Output conductance of transistors

**Effective conductance looking into the cascade structure

Evaluating (3.11) and (3.17) yields G_m = 11 μS and $G_{m,eff}$ = 10.8 μS. For comparison, the performance degradation of a conventional FC OTA without current splitting will be discussed in Section 3.3.7.

3.3.3 Source Degeneration for Low-Noise Design

Furthermore, we apply source degeneration to reduce the noise of transistors M_9–M_{12}, for the local feedback from the degeneration resistor forces some of the noise current to circulate inside the MOS transistor without coupling to the output. We define $\gamma = g_m/I_D$ and degeneration factor $\alpha = g_mR$, where R, I_D, and g_m are the degeneration resistance, transistor drain current, and transconductance, respectively. Hence, the current noise PSD is attenuated by $1/(1+g_mR)^2 = 1/(1+\alpha)^2$, but the resistor consumes headroom $V_{headroom} = I_DR = \alpha / \gamma$. We can thus derive $R = \alpha / (\gamma I_D)$. Note that α should only be maximized with affordable R and $V_{headroom}$ values. In this design, we choose γ and α as 20 and 12, respectively. So, a reasonable $V_{headroom} = 600\ mV$ is achieved. The

drain currents $I_{D9,10}$ and $I_{D11,12}$ are 225 nA and 200 nA, respectively. So, the values of $R_{9,10}$ and $R_{11,12}$ are calculated as 2.67 MΩ and 3 MΩ, respectively. We inter-digitize unit resistors in series in the layout to achieve good matching.

We show that this selection of R value gives an optimal design tradeoff between noise and voltage headroom. The maximum output swing that can be achieved with this FC structure is $V_{o,\ swing} = VDD - (V_{headroom}+4|V_{DSAT}|)$, where $|V_{DSAT}|$ is the minimum drain-source voltage to keep each output transistor in saturation region, which is typically 100 mV for subthreshold transistors. Thus the $V_{o,swing}$ is around 1.8 V in this design with a VDD of 2.8 V. For this neural application, the output swing requirement is only within 400 mV_{pp}. Thus, this 600 mV headroom will not affect the amplifier linearity. Fig. 3.7 shows the normalized (to $\overline{v_{ni}^2}$) OTA noise is minimized with the 600 mV headroom. At low $V_{headroom} = I_D R$ (i.e., R is low), M_9–M_{12} contribute significant noise, and the higher $G_{d9,10}$ reduces $G_{m,eff}$, so the input referred OTA noise is high. Increasing R reduces the OTA noise. But when $V_{headroom} > 600\ mV$, it starts driving M_9 and M_{10} slightly less saturated, reducing their output resistances and thus $G_{m,eff}$. This effect counteracts any further noise deduction from increased R.

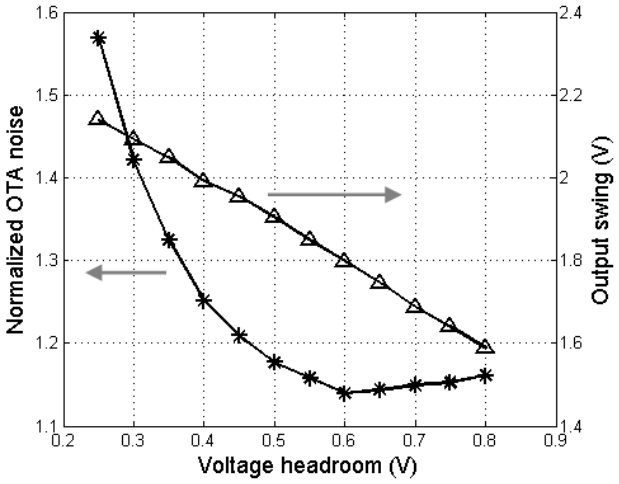

Fig. 3.7. Simulated OTA noise and output swing with respect to voltage headroom.

Examining Fig. 3.3, the supply-voltage requirement to keep the OTA active is

$$VDD > |V_{DSAT,M18}| + |V_{DSAT,M2}| + V_{GS,M10,\min} + V_{headroom} = 2|V_{DSAT}| + V_{TH} + V_{headroom}, \qquad (3.18)$$

where $V_{GS,M10,min}$ is the minimum gate-source voltage for $M_{9,10}$ and V_{TH} is the threshold voltage of $M_{9,10}$. Hence, with a typical NMOS V_{TH} value of 1 V for this 0.6 μm CMOS process, we calculate $VDD_{min} \approx 1.8\ V$. In Fig. 3.8, we sweep the supply voltage and measure the AC transconductance G_{meff}, indicating a VDD_{min} of roughly 2.0 V, as the curve has a sharp knee at 1.9 V. The effective G_m drops drastically below this voltage. We choose 2.8 V mainly because it is convenient to use a universal 1.28 V (~ *VDD/2*) reference voltage generated by the integrated bandgap circuit.

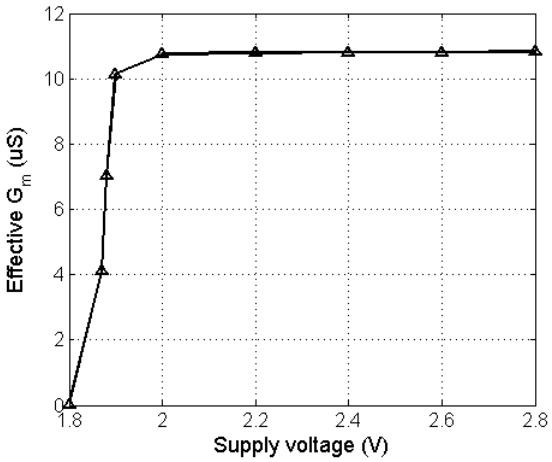

Fig. 3.8. Simulated effective G_m with respect to supply voltage.

3.3.4 OTA Noise Analysis

After applying all the noise-reduction techniques including current scaling, current splitting and bottom-transistor source degeneration, the remaining main noise contributors are M_1–M_4, R_9–R_{12} and M_{15}–M_{16}. We bias M_{15} and M_{16} in above-threshold region to minimize their noise. As shown in Section 3.3.2, the noise contribution of M_1–M_4 is the same as a simple differential pair in subthreshold region. The input-referred noise PSD of the entire OTA is

$$\overline{v_{ni,OTA}^2} = 4kT\frac{U_T}{\kappa^2 I_B} + \frac{1}{G_{m,eff}^2}\cdot 8kT\cdot\left(\frac{1}{R_9}+\frac{1}{R_{11}}+\frac{1}{2\kappa}\frac{\kappa I_B}{N U_T}\frac{2}{1+\sqrt{1+4\cdot IC_{15}}}\right). \quad (3.19)$$

Substituting $G_{m,\,eff} = 98\%\, G_m$ into (3.19) yields

$$\overline{v_{ni,OTA}^2} = 4kT\frac{U_T}{\kappa^2 I_B}\left(1+\frac{2 U_T N^2}{(0.98)^2\cdot I_B(2A+1)^2}\cdot\left(\frac{1}{R_9}+\frac{1}{R_{11}}+\frac{I_B}{N U_T}\frac{1}{1+\sqrt{1+4\cdot IC_{15}}}\right)\right). \quad (3.20)$$

Given the known constants and design parameters, we compute

$$\overline{v_{ni,OTA}^2} = 1.14 \times 4kT \frac{U_T}{\kappa^2 I_B} = 1.14 \ \overline{v_{ni}^2} \cdot \tag{3.21}$$

Equation (3.21) indicates that the noise of our OTA is only 1.14 times that of an ideal differential pair biased in subthreshold region. Our design has minimized all noise sources except for those of the input transistors. Evaluating (3.21), we calculate $\overline{v_{ni,OTA}} = 51 \ nV/\sqrt{Hz}$ as the input-referred noise voltage density of our OTA at 300 K, which is close to the theoretical noise limit of 48 $nV/\sqrt{Hz}$ from Section 3.3.1.

3.3.5 Noise Efficiency Factor

For a fair comparison of the noise-power tradeoff among neural amplifiers, the noise efficiency factor (NEF) proposed in [65] is adopted

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}}, \tag{3.22}$$

where $V_{ni,rms}$ is the amplifier total input-referred noise voltage, I_{tot} is the amplifier total supply current, and BW is the amplifier -3 dB bandwidth. NEF normalizes the total input-referred noise of an OTA to that of a single-BJT amplifier with the same bandwidth and supply current. It provides a good figure of merit (FOM) for comparison of various low-noise OTA designs. Assuming a first-order roll-off for noise [66], $V_{ni,rms}$ can be derived as

$$V_{ni,rms} = \sqrt{\overline{v_{ni,OTA}^2} \cdot \frac{\pi}{2} \cdot BW} \ . \tag{3.23}$$

Substituting (3.21) and (3.23) into (3.22), and noting that $I_{tot} = 2I_B$, we find

$$NEF = \sqrt{\frac{2.28}{\kappa^2}} = 2.16 \cdot \tag{3.24}$$

Equation (3.24) gives the theoretical NEF of the proposed OTA. In real practice, taking into account the flicker noise and the additional power consumption in the biasing circuit, the NEF will be a little larger than the theoretical value.

3.3.6 OTA Design Procedures

This section summarizes the design procedure for the low-noise low-power OTA.

1) From the power consumption specification, the total bias current partitioned to the input differential pair of the OTA is 800 nA. By operating in deep subthreshold region, the noise limit of a differential pair at room temperature calculates 48 $nV/\sqrt{Hz}$.

2) The preamplifier input referred noise spec is < 5 μV_{rms}. We design $V_{ni,rms}$ = 3 μV_{rms} to give enough margin. Based on (3.23), the opamp cutoff frequency f_c is calculated as 1.5 kHz, which is enough to cover the fast-ripple range.

3) As shown in Fig. 3.1, C_f is chosen as 0.2 pF and C_p is estimated to be 0.5 pF. *Cs* is computed as 20 pF to give a 40 dB closed-loop gain. The resulted feedback factor β is 0.01. With a load capacitance C_L = 11 pF, *Gm* calculates as 10.7 μS form the f_c requirement.

4) As discussed before, equal splitting is chosen in compliance with the noise and splitting factor tradeoff. Thus the g_m for each split input device ($M_{1\text{-}4}$) is 5.35 μS. The resulting g_m / I_D value of 26.5 ensures deep subthreshold operation for these devices. Consequently, the $(W/L)_{1\text{-}4}$ value is designed at 240μm/3μm to achieve good tradeoff

between flicker noise, gate capacitance and loop gain.

5) We chose L = 8 μm for bottom transistors $M_{9\text{-}12}$ for two main design considerations, minimizing noise contribution and increasing output impedance.

6) The bias current of $M_{15\text{-}16}$ was scaled down by 16 times to minimize their noise contributions. The aspect ratio is chosen to be 2μm/2μm to have it biased in moderate inversion for both minimized noise and good matching for the current mirror.

7) Finally, source-degeneration resistances are designed to achieve good tradeoff of noise suppression and voltage headroom, as discussed in Section 3.3.3.

3.3.7 Remarks

Compared to a conventional FC OTA, current-splitting OTAs have higher $G_{m,eff}$, lower degeneration-resistor area, and reduced noise. Current-splittnig OTAs provide an extra degree of freedom that can either provide higher g_m for a given current, less power for a fixed g_m, or a compromise in between. Because we also degenerate the NMOS transistors to reduce output noise (see Section 3.3.3), the current-splitting topology provides the additional advantage of reduced current in each branch, consuming less headroom. The current in M_{N3} and M_{N4} of conventional FC OTAs (see Fig. 3.4) is twice that of current splitting. Based on the discussion in Section 3.3.3, to achieve the same factor of noise reduction on these transistors at the same power, α should be $\sqrt{2}$ times the one with current splitting, thus $\sqrt{2}$ times the voltage headroom because $V_{headroom} = \alpha / \gamma$ as shown before. This headroom increase consumes output swing and raises the output conductance of M_{N3} and M_{N4}. From simulations, the effective output conductance $G_{d,N4}$

$\approx g_{m,N6}$, where $g_{m,N6}$ is the transconductance of M_{N6}. While increasing the transistor aspect ratio *W/L* may slightly improve this headroom problem, simulations indicate that headroom improvements are minute, essentially requiring less degeneration and in turn more noise. Re-computing (3.16) and noting that $G_m = \kappa I_B / U_T$ for the conventional FC OTA, the effective transconductance yields

$$G_{m,eff,con} = \frac{g_{m,N6}}{g_{m,N6} + G_{d,N4} + g_{d,P2}} \cdot \frac{\kappa I_B}{U_T} \approx 0.5 \frac{\kappa I_B}{U_T}. \tag{3.25}$$

Defining $R_{N3,4} = R$, we calculate $R = R_{9,10}/\sqrt{2} = 1.88\ M\Omega$. Substituting $G_{m,eff,con}$ and $R_{N3,4}$ values into (3.19), the input-referred noise PSD of the conventional FC OTA yields

$$\overline{v_{ni,OTA,con}^2} = 1.77 \times 4kT \frac{U_T}{\kappa^2 I_B} = 1.77 \overline{v_{ni}^2}. \tag{3.26}$$

Comparing (3.17) and (3.25), the current splitting technique prevents the 50% $G_{m,eff}$ loss from the severe output current scaling. Comparing (3.21) and (3.26), the OTA with current splitting reduces noise by 36%. Table 3.2 summarizes the OTA performance improvements by using current splitting.

Table 3.2. Performance comparison of OTAs

	Current Splitting FC	**Conventional FC**
$R_{degeneration}$	$2\sqrt{2}\,(1+9/8)\,R = 6R$	$(1+1+17/2)\,R = 10.5R$
Current	$2.215\ I_B$	$2.25\ I_B$
$G_{m,eff}$	$1.04\ g_m$*	$0.5\ g_m$*
Noise	$1.14\ \overline{v_{ni}^2}$	$1.77\ \overline{v_{ni}^2}$
Gain	$1.04 g_m \beta \left[R_{d6}(1 + g_{m6}(g_{d4} + G_{d10})^{-1}) \;//\; R_{d14}(1 + g_{m14} R_{d16}) \right]$	$0.5 g_m \beta \left[R_{d,N6}(1 + g_{m,N6}(g_{d,P2} + G_{d,N4})^{-1}) \;//\; R_{d,P8}(1 + g_{m,P8} R_{d,P10}) \right]$
NEF	2.16	2.68

* $g_m = \kappa I_B / U_T$

Setting the preamplifier's load capacitance C_L = 11 pF, we obtain the preamplifier BW as 1.3 kHz through simulation. We explore the potential of extending the proposed preamplifier topology towards higher-frequency (~ 10 kHz) neural applications, such as neural action-potential recording. Keeping the value of C_L fixed through simulations, we increase the bias current of the preamplifier to extend BW and lower input-referred voltage noise.

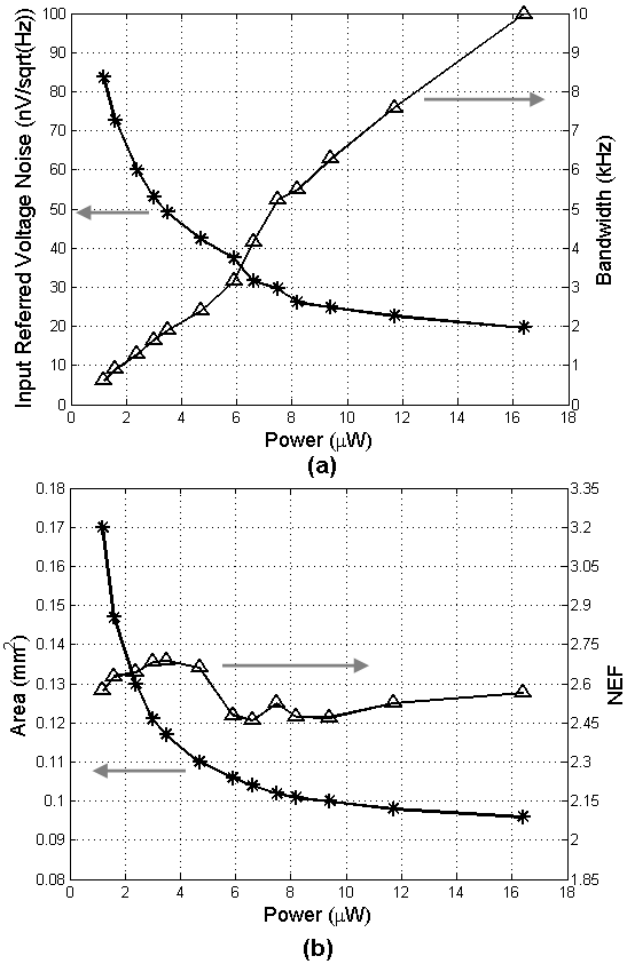

Fig. 3.9. Simulated power tradeoffs for (a) input-referred voltage noise and bandwidth and (b) area and NEF.

When changing the bias current, we scale the source-degeneration resistors by the same ratio to keep the source degeneration factor unchanged. The resistor value and thus the amplifier area are inversely proportional to the bias current. Fig. 3.9 (a) shows the simulation results. Compared to the preamplifier in [51], with the same input-referred voltage noise (20 nV/√Hz) and comparable BW, our preamplifier consumes 16.4 μW (versus 80 μW). Compared to [42], with the same input-referred voltage noise (30 nV/√Hz) and comparable BW, our preamplifier consumes 7.5 μW (versus 7.6 μW). The area and NEF dependence on power is shown in Fig. 3.9 (b). The plots in Fig. 3.9 clearly illustrate the noise, BW, power and amplifier area tradeoffs in a neural amplifier design. The general guide for neural amplifier design is to carefully evaluate these tradeoffs and achieve a good design balance for certain applications.

3.4 Bandpass Filter Design

From the discussion of BPF specifications in Section 3.2, Table 3.3 summarizes the BPF requirements for FR signal sensing. We choose the follow-the-leader feedback (FLF) architecture [67] for the BPF design because of its good tradeoff between sensitivity and tuning ability compared to both simple cascading and more complex leap-frog architectures. We choose an elliptic approximation to achieve a fast filter rolloff. Fig. 3.10 shows the filter block diagram.

Table 3.3. Specifications of the FR bandpass filter

Order	6
Passband	250 Hz - 500 Hz
Passband ripple	≤ 0.5 dB
Rolloff	-33 dB/octave
Attenuation	≥ 30 dB at 125 Hz and below

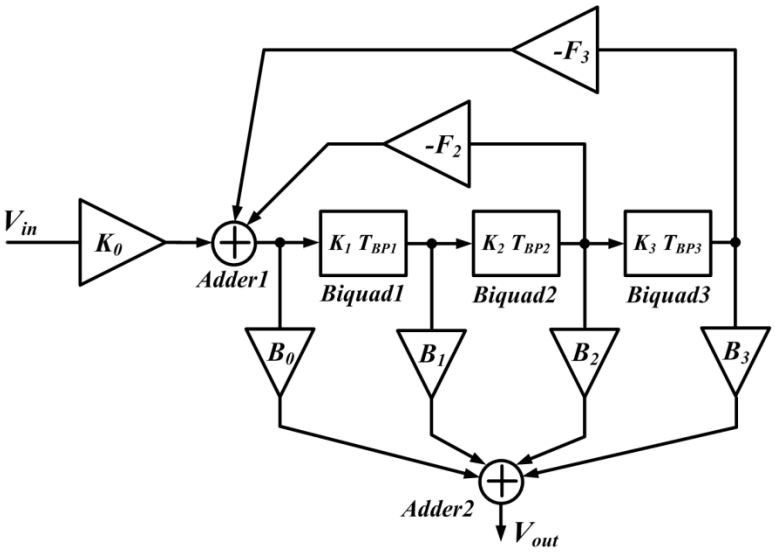

Fig. 3.10. Block diagram of the 6th-order FLF elliptic bandpass filter.

The feedback is based on a primary resonator structure with identical biquadratic sections (biquads) T_{BP1} -T_{BP3}, except biquad gains. F_2 and F_3 are the feedback coefficients. Four feed-forward coefficients B_0 -B_3 are added to realize the elliptic filter's finite zeros. K_0 is the filter gain coefficient; K_1, K_2 and K_3 are the gain coefficients of each biquad. We synthesize a 3rd-order lowpass (LP) filter prototype and then perform a LP-to-BP transformation to obtain the desired 6th-order BPF. The results are shown in Table 3.4, where Q and f_o are the quality factor and center frequency of biquads, respectively.

Fig. 3.11 shows the biquad block diagram. The design procedure for biquads is discussed as follows. Neglecting excess-phase-compensation resistors $R_{1,2}$ (since $R_i << |1/sC_i|$ within the passband 250 – 500 Hz), the transfer function of biquad1 – biquad3 becomes

$$H_i(s) = \frac{v_{bp,i}}{v_{in,i}} = \frac{K_i \frac{\omega_{o,i}}{Q_i} s}{s^2 + \frac{\omega_{o,i}}{Q_i} s + \omega_{o,i}^2} = \frac{\frac{g_{m1,i}}{C_{1,i}} s}{s^2 + \frac{g_{mr,i}}{C_{1,i}} s + \frac{g_{m1,i} g_{m2,i}}{C_{1,i} C_{2,i}}} (i = 1, 2, 3). \quad (3.27)$$

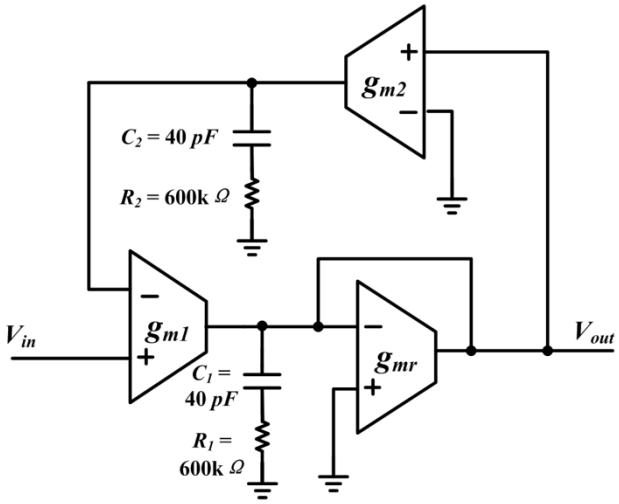

Fig. 3.11. Biquad block diagram. The series resistance for the excess phase compensation is 600k Ω.

The design procedure of the BPF is discussed below.

1) As discussed above, through filter approximation and synthesizing by using MATLAB®, the filter coefficients and biquad parameters are computed in Table 3.4.

2) From the biquad transfer function (3.27), the parameters can be mapped to the expressions of g_m and C as shown below.

Center frequency: $\omega_{o,i}^2 = g_{m1,i}\, g_{m2,i}/(C_{1,i}C_{2,i})$. (3.28)

Bandwidth: $BW_i = \omega_{o,I}/Q_i = g_{mr,I}/C_{1,i}$. (3.29)

Quality factor: $Q_i = (g_{m1,I}\, g_{m2,i}C_{1,I}/g_{mr,i}^2/C_{2,i})^{0.5}$. (3.30)

Gains: $H_i(j\omega_o) = K_i = g_{m1,I}/g_{mr,i}$. (3.31)

In this design, $\omega_{o,i}$, BW_i and Q_i are equal for all the three biquads. But K_i vary with $g_{m1,i}$.

3) For design simplicity, we choose equal value for C_1 and C_2 as 40 pF. Substituting the Q, f_o, and K_i values from Table 3.4 into equations (3.28) – (3.31), we can compute all the g_m values as shown in Table 3.5. Note that the product $g_{m1,i} \cdot g_{m2,i}$ is nominally the same for all the biquads.

4) Two adders (adder1 and adder2 in Fig. 3.10) are realized by differential pairs to achieve signal addition in current mode. Since $B_0 = 0$, we can use the same topology as shown in Fig. 3.12 for both adders. B_1 -B_3 are implemented as $B_i = g_{mA,i}/g_{md}$, where $g_{mA,1}$, $g_{mA,2}$ and $g_{mA,3}$ are the transconductances of $M_{A1,2}$, $M_{A3,4}$ and $M_{A5,6}$, respectively. The same implementation is applied to K_0, F_2 and F_3 as well. Similar to the biquad G_m cells, the adders are also source degenerated to improve linearity.

Table 3.4. Parameters of the 6th order FLF elliptic filter

K0	0.6596	***B0***	0	***F2***	0.6517
K1	2.3573	***B1***	0.1939	***F3***	0.238
K2	2.186	***B2***	-0.3878	***Q***	2.2318
K3	2.0064	***B3***	1.1939	***fo***	353.55 Hz

Table 3.5. Parameters of Biquads

	Biquad1	***Biquad2***	***Biquad3***
g_{m1} ***(nS)***	93.8	87.0	80.0
g_{m2} ***(nS)***	84.1	90.7	98.8
g_{mr} ***(nS)***	39.8	39.8	39.8
C_1 ***(pF)***	40	40	40
C_2 ***(pF)***	40	40	40

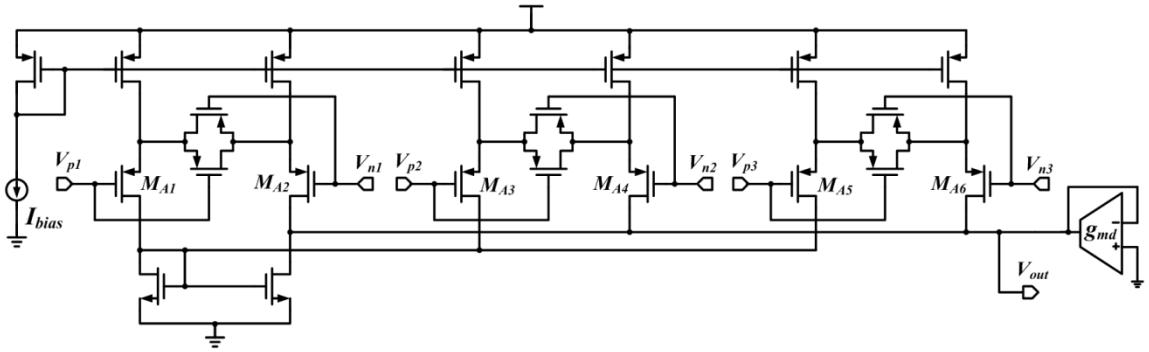

Fig. 3.12. Schematic of the adders.

This paragraph discusses the 6th-order BPF's sensitivity to parameter variation. Q and ω_o errors are the principal cause of high-order filters' frequency-response degradation [68]. Applying Mason's rule to the filter block diagram (see Fig. 3.10) and inserting (3.27), the filter transfer function yields

$$T(s) = K_0 \frac{B_1 K_1 \frac{x_1}{Q_1} \cdot \prod_{i=2}^{3}\left(x_i^2 + \frac{x_i}{Q_i} + 1\right) + B_2 K_1 K_2 \left(x_3^2 + \frac{x_3}{Q_3} + 1\right) \cdot \prod_{i=1}^{2}\left(\frac{x_i}{Q_i}\right) + B_3 K_1 K_2 K_3 \cdot \prod_{i=1}^{3}\left(\frac{x_i}{Q_i}\right)}{\prod_{i=1}^{3}\left(x_i^2 + \frac{x_i}{Q_i} + 1\right) + F_2 K_1 K_2 \left(x_3^2 + \frac{x_3}{Q_3} + 1\right) \cdot \prod_{i=1}^{2}\left(\frac{x_i}{Q_i}\right) + F_3 K_1 K_2 K_3 \cdot \prod_{i=1}^{3}\left(\frac{x_i}{Q_i}\right)}, \quad (3.32)$$

where $x_i = s/\omega_{o,i}$. Fig. 3.13 shows the system-level simulation results.

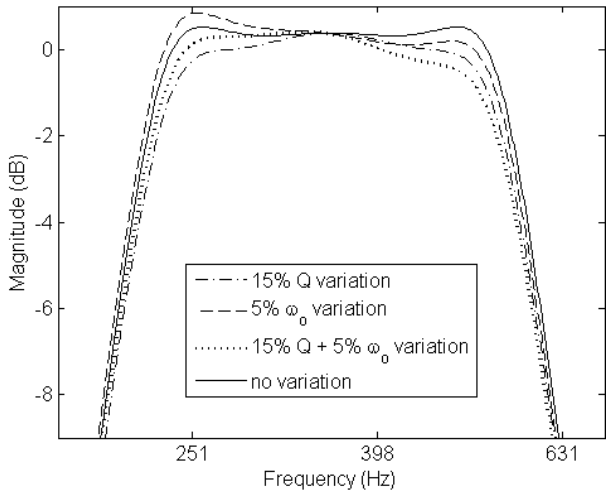

Fig. 3.13. Filter sensitivity to the Q and ω_o of the biquads.

The tolerable variation limits of the biquad's Q and ω_o are 15% and 5%, respectively to restrict passband ripple variation < 0.5 dB and filter bandwidth and center frequency variations < 5% and 2%, respectively. The biquad Q variation mainly changes the filter bandwidth, while the biquad ω_o variation alters the filter center frequency. The rolloff is less sensitive to parameter variations. We lay out the G_m cells, resistor arrays, and capacitor arrays in common-centroid patterns. A filter tuning scheme is discussed later in this section.

Fig. 3.14 shows the schematic of the G_m cells used in the biquads. These G_m cells have the same I_{bias}, except for g_{m2}, which has tunable I_{bias}. The bias current is 16 nA in each input transistor. To achieve small g_m values (tens of nS) for this low-frequency filter design, we source degenerate the input transistors $M_{1,2}$ with triode PMOS transistors $M_{3,4}$ [69]. The source degeneration also improves the G_m cells' linearity. The degeneration factor a is

$$a = 1 + \frac{\beta_1}{4\beta_2},\ \ where\ \beta = \mu C_{ox}\frac{W}{L}. \tag{3.33}$$

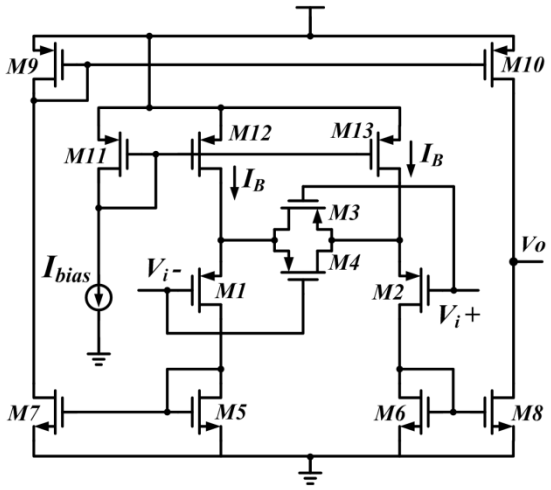

Fig. 3.14. Schematic of the Gm cells in the biquads.

Increasing *a* yields better linearity, but compromises the input range and tuning ability of the G_m cells. Adopting the analysis in [69], the input range before $M_{3,4}$ enters saturation region is

$$|v_{in}| \le \sqrt{\frac{a^2 + a + 0.5}{a^4 + 0.25}}. \tag{3.34}$$

We choose a value of *a* as 2.5 to get a good design tradeoff. The input range with this *a* value is ± 485mV and is enough for this application. All the load transistors M_5 – M_{13} are designed with longer length than input transistors to minimize their noise.

To tune the filter, we only tune $g_{m2,i}$ (thus Q_i and $\omega_{o,i}$), leaving BW_i and K_i unchanged. A 5-bit binary-weighted current DAC adjusts the bias currents of $g_{m2,i}$ through a bank of current sources controlled by the input digital code. An on-chip bandgap circuit generates the reference current for the current-source bank. The BPF

consumes 800 nA total. Each biquad dissipates 200 nA, and there are three biquads. Adder1 dissipates 111 nA, and adder2 dissipates 89 nA.

3.5 Experimental Results

This neural front-end recording circuit was fabricated in XFab 0.6 μm CMOS process with two-poly-three-metal (2P3M) layers. All the capacitors were built as poly-poly capacitors for maximum linearity. All resistors were implemented with high-resistance polysilicon, except R_H, which is implemented by MOS-bipolar pseudoresistors [52]. An on-chip bandgap circuit generates all the reference currents and voltages for the entire chip to minimize the use of off-chip components in the neural detection implant. Fig. 3.15 displays the die photo. The total area of the front-end is 0.45 mm^2, of which the preamplifier occupies 0.13 mm^2.

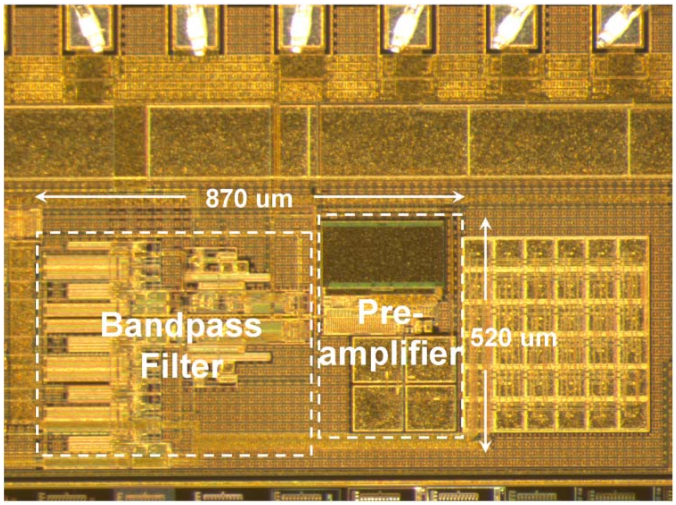

Fig. 3.15. Die microphotograph of the neural front-end circuit.

The chip is sealed in the standard ceramic DIP 28-pin package. We use a HP 89441A vector signal analyzer (VSA) for a series of bench-top tests to verify the functionality of the front-end circuit. These tests include AC response, noise, THD, CMRR and PSRR measurements. Fig. 3.16 shows the experimental setup.

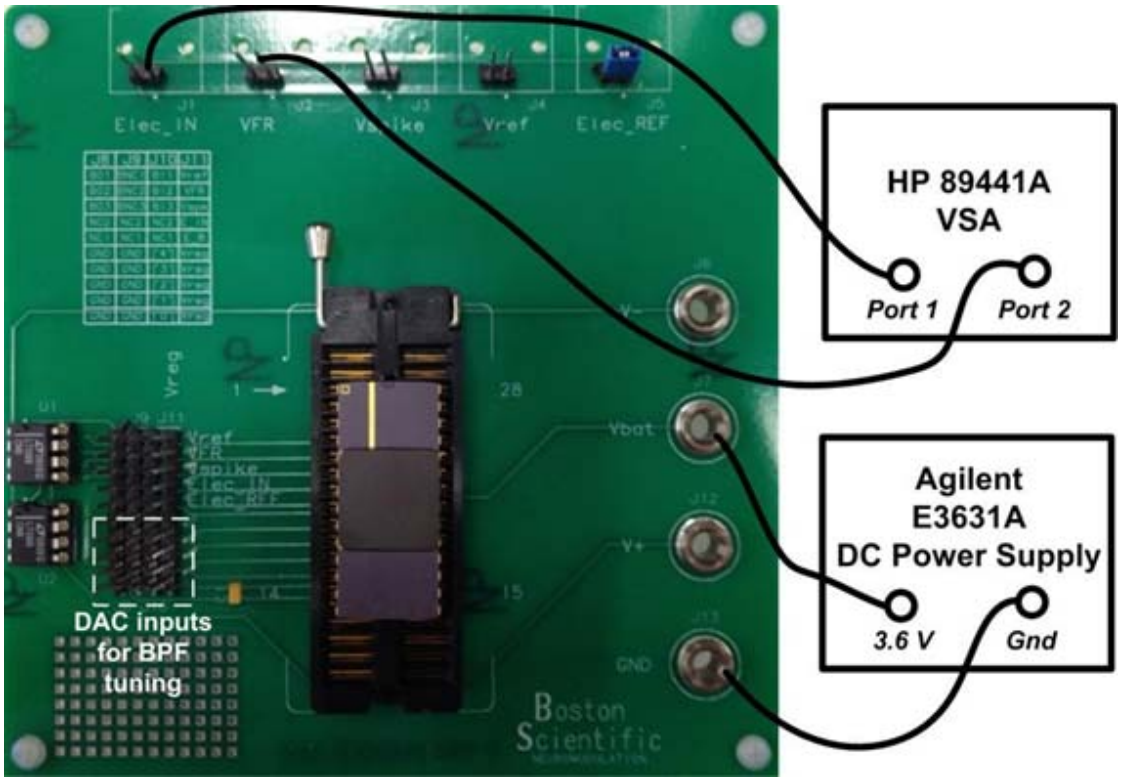

Fig. 3.16. Bench-top test setup for the neural front-end circuit.

3.5.1 Preamplifier Test Results

The preamplifier mid-band gain is designed to be 40 dB by setting C_s to 20 pF and C_f to 0.2 pF. Fig. 3.17 shows the measured AC response of the preamplifier. The measured preamplifier mid-band gain is 39.4 dB, slightly lower than the designed value of 40 dB. This discrepancy is likely due to capacitor mismatches or the additional

fringing capacitance on the small C_f capacitors [51] or the finite OTA gain (Simulations show that a finite OTA gain of 1500 V/V can cause this 0.6 dB discrepancy). The highpass and lowpass cutoff frequencies are measured at 0.36 Hz and 1.3 kHz, respectively. The load capacitance of the preamplifier is 11 pF.

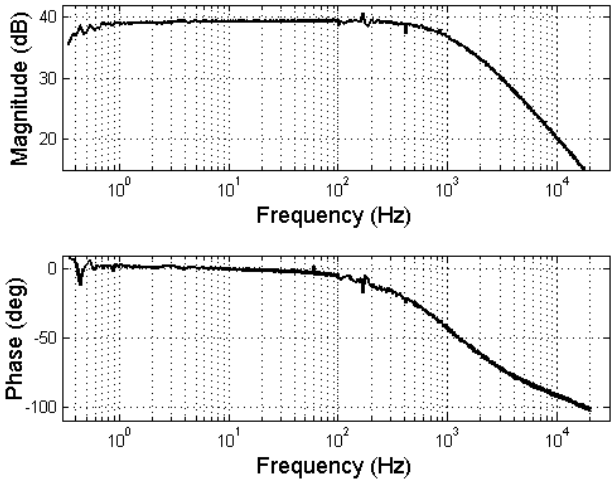

Fig. 3.17. Measured AC response of the preamplifier.

Total input-referred noise was measured as the total output noise divided by the mid-band gain. Fig. 3.18 plots the measured input-referred noise spectral density together with the simulated curve. We observe that the measured spot noise at 1 kHz for the preamplifier is 60 nV/√Hz, which is close to the calculated value of 51 nV/√Hz by using (3.21). The slight difference is mainly due to the degraded gain mentioned above. It could also be caused by the simplified subthreshold models shown in (3.8) – (3.10). The $1/f$ noise corner occurs near 50 Hz. The total input-referred noise of 3.07 μV_{rms} was obtained by integrating the area under the measured curve from 0.5 Hz–30 kHz. The resulting NEF is 3.09. The preamplifier consumes a total power of 2.4 μW from a 2.8 V

power supply. The total current consumption of the preamplifier is 872 nA. The input transistors consume most of the current (800 nA).

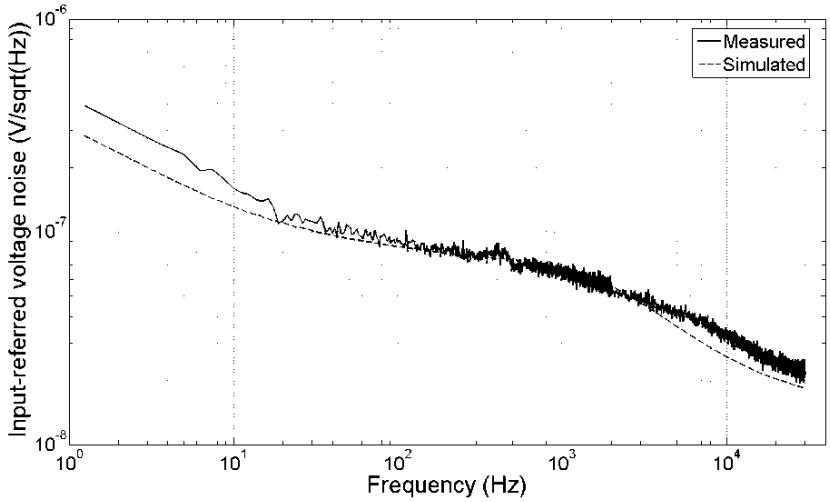

Fig. 3.18. Measured and simulated (dashed line) input-referred voltage noise spectra of the preamplifier.

Our amplifier achieves one of the best NEFs at the lowest power consumption within kilo-hertz bandwidth in the literature. The total harmonic distortion (THD) is 1% with a maximum 10 mV_{pp} input signal. The measured CMRR and PSRR exceed 66 dB and 80 dB across the bandwidth from 0.36 Hz to 1.3 kHz, respectively. While there are few papers in the literature to which we can compare addressing the on-silicon epileptic fast ripple detection, there are several reported neural action potential amplifiers [42], [51], [54], [61], [62], [70], [71]. Table 3.6 lists a comparison of the proposed preamplifier with these works.

Table 3.6. Neural preamplifier performance comparison

	Mohseni 2004 [62]	Gosselin 2007 [61]	Yin 2007 [54]	Harrison 2003 [51]	Wattana-panitch 2007 [42]	Shahrokhi 2010 [70]	Rodriguez-Perez 2012 [71]	This Work 2011
Current /Power	38.3 μA /115 μW	4.67 μA /8.4 μW	8 μA /27.2 μW	16 μA /80 μW	2.7 μA /7.6 μW	4.25 μA /12.75 μW	1.6 μA /1.92 μW	0.872 μA /2.4 μW
Gain	39.3 dB	49.52 dB	39.3 dB	39.5 dB	40.85 dB	73 dB	47.5 dB	39.4 dB
Bandwidth	0.1 Hz - 9.1 kHz	98.4 Hz – 9.1 kHz	0.015 Hz - 4 k Hz	0.025 Hz - 7.2 kHz	45 Hz - 5.32 kHz	10 Hz - 5 kHz	167 Hz - 6.9 kHz	0.36 Hz – 1.3 kHz
Load capacitor	N/A	0.4 pF	3 pF	17 pF	9 pF	N/A	N/A	11 pF
Total input referred noise	7.8 μV_{rms} 0.1 Hz - 10 kHz	5.6 μV_{rms} 1 Hz - 50 kHz	3.6 μV_{rms} 20 - 10 kHz	2.2 μV_{rms} 0.5 Hz - 50 kHz	3.06 μV_{rms} 10 Hz - 98 kHz	6.08 μV_{rms} 10 Hz - 5 kHz	3.8 μV_{rms} 1 Hz - 100 kHz	3.07 μV_{rms} 0.5 Hz - 30 kHz
NEF	19.4	4.9	4.9	4	2.67	5.55	2.16	3.09
Max. signal	5 mV_{p-p} (THD 1.1%)	2.4 mV_{p-p} (THD 1%)	17.4 mV_{p-p} (THD 1%)	16.7 mV_{p-p} (THD 1%)	7.3 mV_{p-p} (THD 1%)	N/A	3.1 mV_{p-p} (THD 1%)	10 mV_{p-p} (THD 1%)
CMRR	N/A	> 50 dB	N/A	> 83 dB	> 66 dB	N/A	83 dB	> 66 dB
PSRR	N/A	> 50 dB	N/A	> 85 dB	> 75 dB	N/A	N/A	> 80 dB
Die area	0.107 mm^2	0.050 mm^2	0.201 mm^2	0.160 mm^2	0.160 mm^2	0.02 mm^2	0.08 mm^2	0.130 mm^2
Process	1.5 μm CMOS	0.18 μm CMOS	1.5 μm CMOS	1.5 μm CMOS	0.5 μm CMOS	0.35 μm CMOS	0.13 μm CMOS	0.6 μm CMOS

3.5.2 Front End Test Results

Fig. 3.19 shows the measured AC response of the entire front-end circuit for FR recording. The passband is 250 – 486 Hz. The passband gain is 38.5 dB, and the in-band ripple is less than 0.5 dB. The filter rolloff is measured as -110 dB/decade. The achieved attenuation is around 30 dB for $f < 200$ Hz and ≥ 30 dB for $f > 5$ kHz. Simulations show that the high-frequency level-off is mainly caused by the finite feed-forward coefficient B_0 (see Fig. 3.10). By design, $B_0 = 0$. However, in the layout, the parasitic (trace or

junction) capacitances could provide a finite feed-forward path (i.e., finite B_0) between the output of adder1 and one of the inputs of adder2. Setting $B_0 = 0.1$ for simulations, the result reproduces the measured high-frequency level-off. Fig. 3.20 shows the front-end simulation results with $B_0 = 0$ and $B_0 = 0.1$. The effect of finite B_0 can be clearly observed.

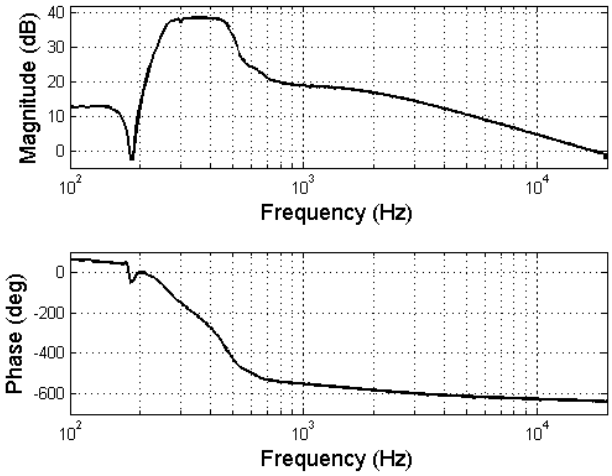

Fig. 3.19. Measured AC response of the neural front-end circuit.

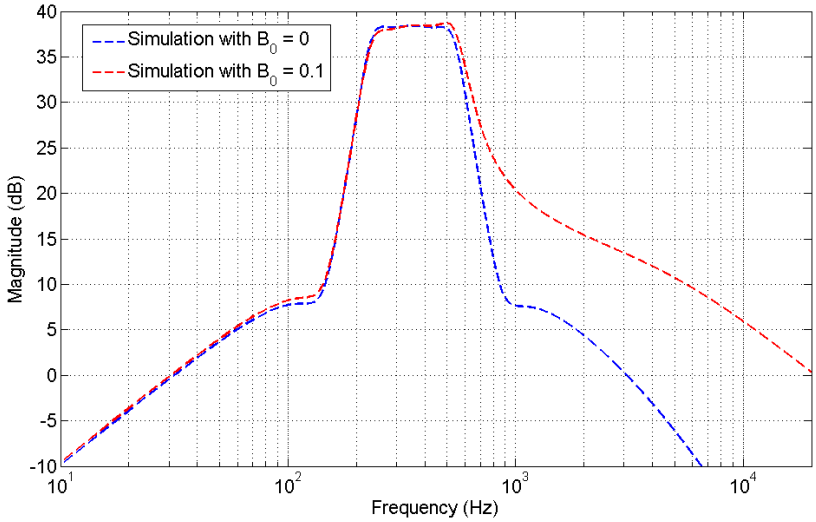

Fig. 3.20. Comparison of front-end simulation results for $B_0 = 0$ and $B_0 = 0.1$.

Fig. 3.21 plots the front-end measured and simulated input noise spectral densities. A good agreement in between measurement and simulation is achieved. The total input-referred noise of the front end is 2.48 μV_{rms} obtained by integrating through the passband. The corresponding NEF is 7.6 while consuming a total power (preamplifier + filter) of 4.5 μW from the 2.8-V power supply. The maximum input amplitude for the entire front end is 3.4 mV_{pp} (1% THD). This input range can well cover the epileptic FR signals. The dynamic range of the front end is achieved as 54 dB. The measured CMRR and PSRR exceed 79 dB and 68 dB across the passband, respectively.

Table 3.7 compares the performance of our front-end circuit with the state-of-the-art for EEG acquisition. Our proposed front end provides one of the highest-order on-chip filtering for EEG preconditioning applications reported so far in the literature [6], [35], [42], [51], [54], [72]. This front end consumes 0.75 μW/pole and is the most power-efficient reported to date. We use a power/pole metrics to be able to compare, in a fair way, with similar filters of different orders.

Table 3.7. Neural front-end circuit performance comparison

	Harrison 2003 [51]*	**Wattanapanitch 2007 [42]***	**Shojaei-Baghini 2005 [72]**	**Verma 2010 [6]**	**This work**
Current/ Power	180 nA/ 0.9 μW	743 nA/ 2.1 μW	22 μA/ 73 μW	3.5 μA/ 3.5 μW	1.6 μA/ 4.5 μW
Filter Topology	OTA dominant pole	1st-order BPF	1st-order LPF	2nd-order LPF	6th-order FLF Elliptic BPF
Power/ pole	0.9 μW/ pole	2.1 μW/ pole	73 μW/ pole	1.75 μW/ pole	0.75 μW/ pole
Roll off	-20 dB/decade	-20 dB/decade	-20 dB/decade	-40 dB/decade	-110 dB/decade
In-band ripple	N/A	N/A	N/A	N/A	0.5 dB
Bandwidth	0.014 - 30 Hz	0.39 - 295 Hz	0.05 - 170 Hz	0.5 - 100 Hz	250 - 486 Hz
Total input-referred noise	1.6 μV_{rms}	1.66 μV_{rms}	6 μV_{rms}	1.3 μVrms	2.48 μV_{rms}
NEF	4.8	3.2	80	N/A	7.6
Gain	39.8 dB	40.9 dB	55 dB	60 dB	38.5 dB
Max. input (THD 1%)	12.4 mV_{p-p}	7.2 mV_{p-p}	N/A	N/A	3.4 mV_{p-p}
Dynamic Range	69 dB (THD 1%)	63.7 dB (THD 1%)	N/A	N/A	54 dB (THD 1%)
CMRR	> 86 dB	66 dB	100 dB (60 Hz)	> 60 dB	> 79 dB
PSRR	> 80 dB	75 dB	N/A	N/A	> 68 dB
Applications	Surface EEG	Parkinson's Disease	ECG Recording	Seizure Detection	Epileptic FR Detection
Process	1.5 μm CMOS	0.5 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.6 μm CMOS

* The authors also reported the measurement results for their front end configured for lower frequency neural recording

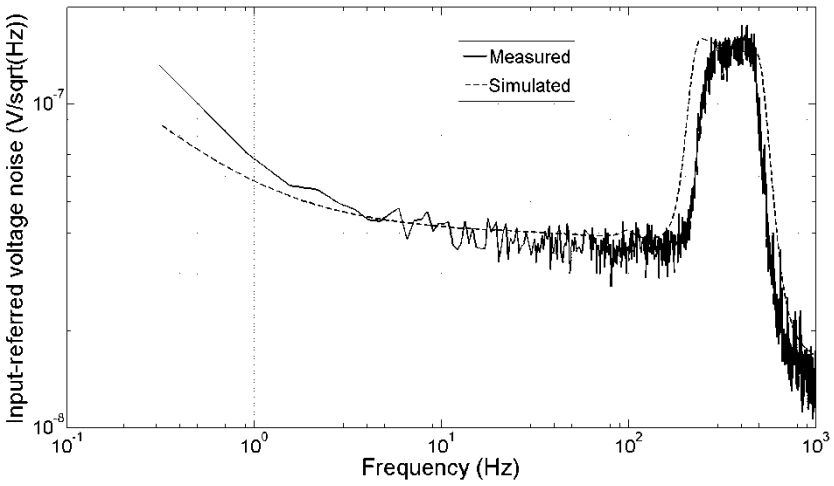

Fig. 3.21. Measured and simulated (dashed line) input-referred voltage noise spectra of the neural front-end circuit.

3.5.3 Saline-Solution Test Results

The front-end circuit was also tested in a sterilized saline solution with an 8-contact lead (Boston Scientific Neuromodulation, Model SC2108 Linear). Saline solution is used to emulate patient's brain tissue. An artificial 2 mV_{pp} IEEG signal was generated using an Agilent 33250A arbitrary waveform generator. This signal was fed into the saline solution through contact 1 of the lead. Contact 3 collected the signal, and the neural front-end circuit amplified and filtered the input signal.

Fig. 3.22 shows the experimental setup for the saline-solution test. The front-end gain and bandwidth were set at 38.5 dB and 250 - 486 Hz, respectively. The upper and lower traces in Fig. 3.23 show the input and output signals, respectively. A 320-Hz signal tone was embedded in some segments of the input signal to emulate the fast ripple signal, and this tone was correctly extracted and amplified by the front-end circuit.

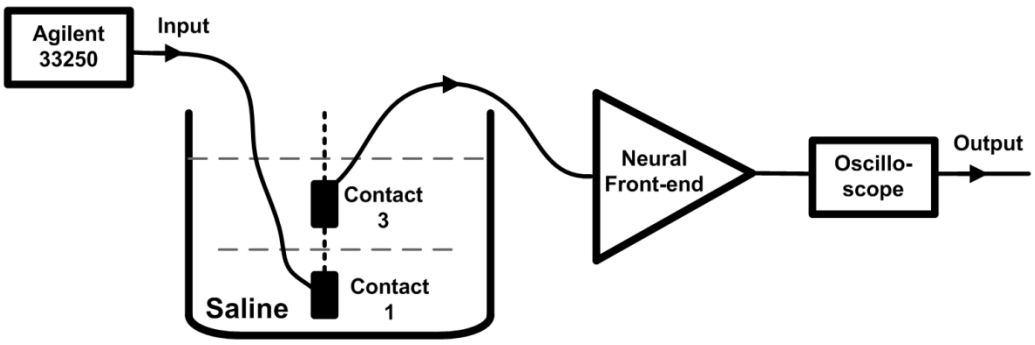

Fig. 3.22. Saline-solution test setup for the neural front-end circuit.

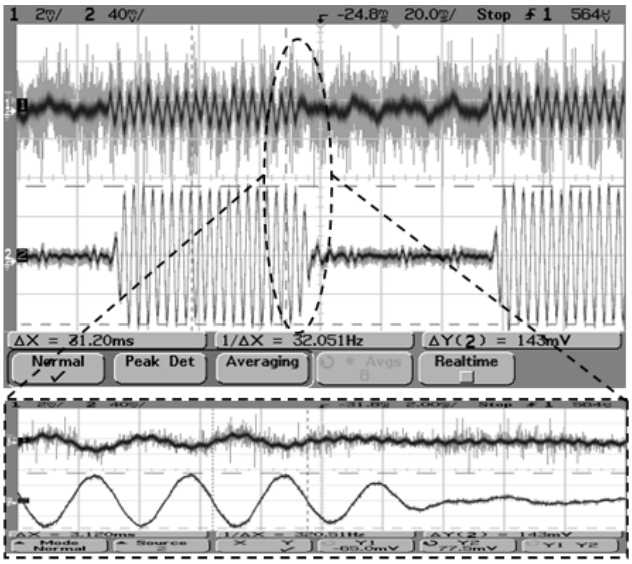

Fig. 3.23. Measured input (upper trace) and output (lower trace) of the front-end testing in a saline solution (input is a 2 mV_{pp} artificial IEEG signal). The output fast ripple signal is 320 Hz and 143 mV_{pp}. Inset: a close-up view of one segment of the input and output traces.

3.6 Conclusions

This chapter has presented a micropower low-noise front-end circuit for epileptic fast ripple recording. The presented system is the first to achieve the epileptic fast-ripple-recording functionality. We combined several low-noise design techniques to make the preamplifier achieve one of the best noise-power tradeoffs among neural amplifiers reported to date. The on-chip bandpass filter used in the system provides a sharp out-of-band rolloff that meets the clinical need for seizure detection and achieves one of the best power efficiencies in literature. Thus, our front-end circuit design can be embedded in an integrated-circuit solution to seizure detection for future deep-brain-stimulation therapy for intractable epilepsy.

CHAPTER IV

PROPOSED LOW-POWER CONFIGURABLE NEURAL ANALOG-TO-DIGITAL CONVERTER (ADC)*

4.1 Introduction

A sigma-delta (ΣΔ) ADC is designed to digitize the signal from the neural front-end circuit. In recent years, successive approximation (SAR) ADC has been explored and become popular for the neural sensing applications, mainly due to its low power consumption in the kHz sampling frequency range [6], [35]. However, SAR ADCs are usually limited at the medium resolution with $n \leq 10$ bits [73], [74]. It is mainly due to the fact that the number of unit capacitors grows exponentially with the ADC bits [75]. The minimum unit-capacitor size is usually constrained by the layout rules, *kT/C* noise and the capacitive-array distortion due to small unit size [73], [74]. The SAR resolution is also limited by capacitor mismatches and comparator offsets. On the other hand, a ΣΔ ADC does not have the minimum-unit-capacitor constraint and is less sensitive to component mismatch and offsets because of the noise shaping [76]. Thanks to the oversampling technique, a ΣΔ ADC does not need a dedicated anti-aliasing filter, which SAR ADC often requires. Therefore, ΣΔ ADCs are usually working with high resolutions ($n \geq 12$).

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*©[2012] IEEE. Reprinted, with permission, from "A low-power configurable neural recording system for epileptic seizure detection," by C. Qian, J. Shi, J. Parramon, and E. Sánchez-Sinencio, *IEEE Trans. Biomed. Circuits Syst.*, accepted on Nov. 12, 2012.

Moreover, ΣΔ ADC shows better power scaling ability, since both analog and digital power can scale down proportionally as the sampling frequency scales. But, for SAR ADCs, the two dominant power sources, namely the comparator and the DAC capacitor array, do not scale accordingly [77]. Due to the reasons stated above, as resolution increases beyond 8 bits, ΣΔ ADCs have shown to be more power efficient [77] than SAR ADCs. As mentioned in Section 2.2.1, for FR seizure detection, the resolution requirement is higher than 10 bits. Thus, we choose sigma-delta modulation as our ADC architecture.

4.2 ADC Architecture

The proposed ADC consists of a sigma-delta modulator (SDM) followed by a digital decimation filter. We choose a 2^{nd}-order single loop with single-bit quantizer and DAC as our SDM architecture. Single-loop structure achieves good tradeoff of stability and mismatching, compared with multi-loop or cascading structures. A single-bit DAC avoids the linearity problem and is more suitable for medium-high-resolution applications than multi-bit DACs. With the 2^{nd}-order noise shaping and an oversampling ratio of 200, the dynamic range of the SDM can achieve 14 bits with the single-bit DAC. This design meets the resolution specification for neural applications as discussed in Section 2.2.1. The decimation filter achieves improved power and area efficiency, thanks to the simple implementation of a sinc filter and the 8-cycle data pipelining in the succeeding IIR filter. We carefully design the decimation filter to avoid in-band noise

increase due to aliasing, thus retain the dynamic range of the whole ADC. We discuss the SDM design first. The decimation filter design follows in Section 4.4.

4.3 Sigma-Delta Modulator (SDM) Design

Fig. 4.1 shows the topology of the SDM. The loop coefficients are determined from behavioral simulations and are set to [0.5, 2]. The selection of these coefficients ensures a unit signal transfer function (STF) with 2 clock delays, but the noise transfer function (NTF) is 2nd-order high-pass filtered. Fig. 4.2 shows the switch-level schematic of the SDM and the interconnection to the decimation filter.

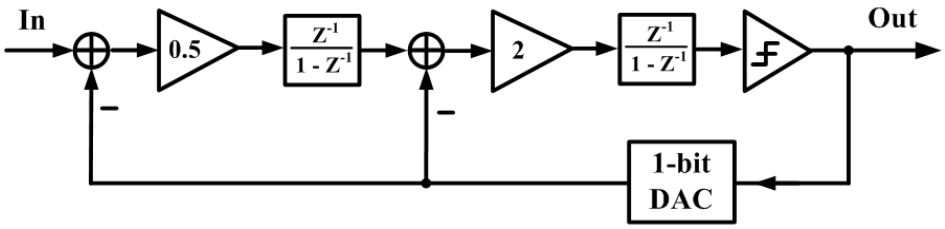

Fig. 4.1. Single-loop 2nd-order SDM topology.

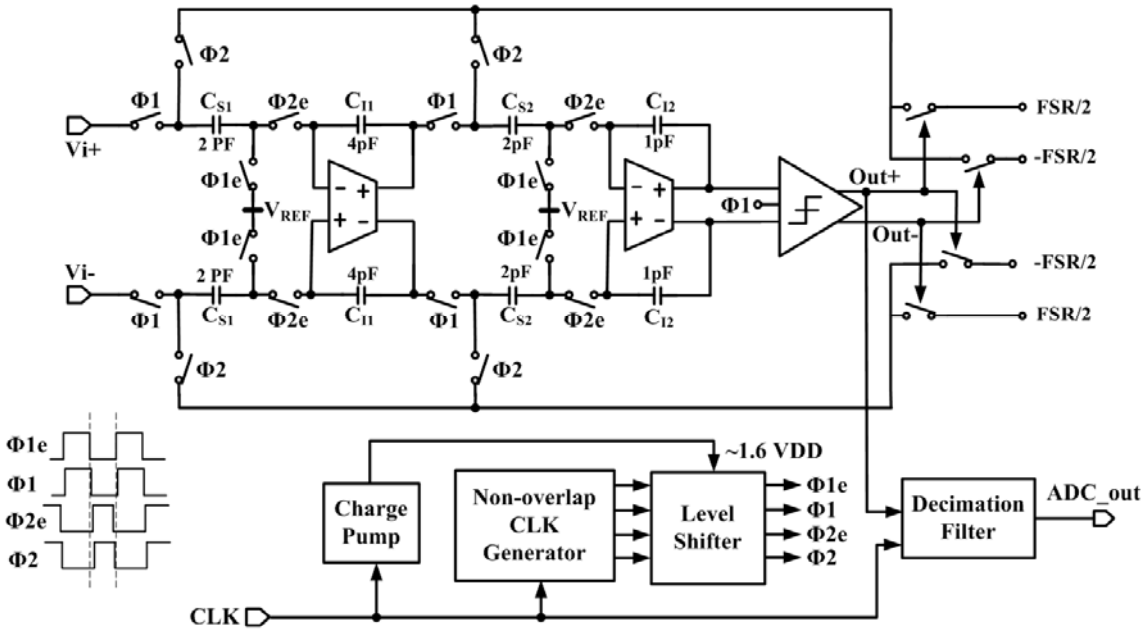

Fig. 4.2. Schematic of the sigma-delta ADC.

The SDM design is similar to what is reported in [76]. The improvements are 1) the current-splitting technique [63], [64] adopted to boost the OTA's speed and slew rate (SR); 2) the voltage doubler [78] used to enhance the linearity of switches.

As shown in Fig. 4.2, Φ_1 and Φ_2 are the non-overlap clocks. C_S and C_I are the sampling and integrating capacitors, respectively. A comparator implements the 1-bit quantizer. The quantization noise power (P_Q) after the noise shaping [79] is known as

$$P_Q = FSR^2 \pi^{2L} / [12 \cdot (2^B - 1)^2 (2L+1) OSR^{2L+1}], \tag{4.1}$$

where FSR is the SDM full scale range, B is the bit resolution of the quantizer, OSR is the oversampling ratio, and L is the modulator order. In practice, the SDM performance is also limited by other major noise sources, such as the switch kT/C noise and the OTA noise. The kT/C noise power [80] is given by

$$P_{kT/C} = \frac{kT/C_S}{f_S/2} \cdot f_B = \frac{kT}{OSR \cdot C_S}, \tag{4.2}$$

where f_B is the signal bandwidth and $OSR = f_s /(2f_B)$. In this design, we choose B = 1, L = 2, and OSR = 200 as discussed earlier. The FSR is set as 0.8 V, which can cover the signal range for all neural applications, without imposing much SR constraint to the OTAs. Thus, this FSR choice avoids the performance overdesign for the seizure detection. By choosing C_S = 2 pF, we compute P_Q = -114 dB and $P_{kT/C}$ = -110 dB.

The OTA noise is carefully reduced by increasing the input transistor geometry size and reducing the g_m of the load transistors. The simulated noise of the first OTA within 5 kHz BW is -125 dB and is negligible compared to the other two noise sources. The peak signal power is $P_{sig,\,peak} = FSR^2/8$, thus the SDM's dynamic range (DR) can be computed as

$$DR = \frac{P_{sig,peak}}{P_Q + P_{kT/C}} = \frac{FSR^2/8}{FSR^2\pi^{2L}/[12\cdot(2^B-1)^2(2L+1)OSR^{2L+1}] + kT/(OSR\cdot C_S)}. \tag{4.3}$$

Fig. 4.3 plots the SDM's DR along with the P_Q-noise-limited DR ($DR_Q = P_{sig,\,peak}/P_Q$) and the kT/C-noise-limited DR ($DR_{kT/C} = P_{sig,\,peak}/P_{kT/C}$). It shows that an OSR of 200 is at the border of kT/C-noise-limited region and gives an efficient SDM design. The calculated DR at this point is 97.7 dB (= 16 ENOBs). ENOB is the effective number of bits and $ENOB = (DR - 1.76)/6.02$.

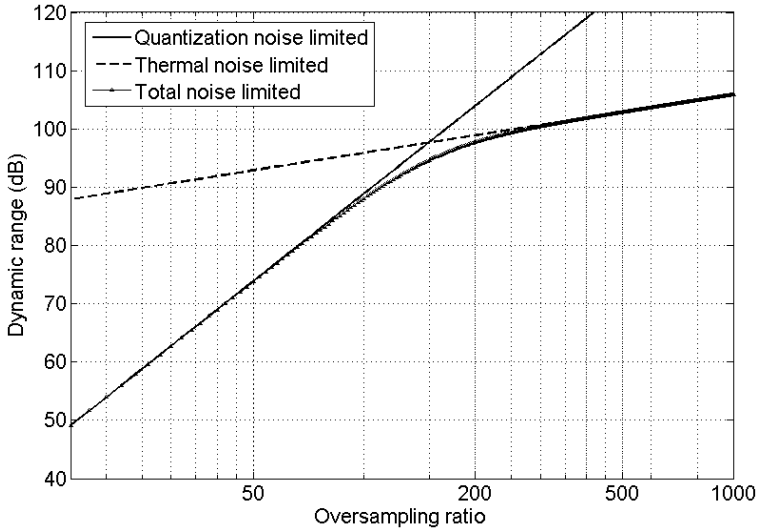

Fig. 4.3. Calculated SDM *DR* with respect to *OSR*.

4.3.1 Low-Power High-Performance Integrator Design

The first OTA has dominant impact on the modulator performance. The design procedures based on the specifications are discussed below.

1) In this application, the maximum ADC speed $f_{s,max} = 2\ MHz$. To reach a good settling accuracy (< 0.5 LSB) within the half clock cycle for a 16-bit resolution, the first OTA's gain-bandwidth product (GBW) should be at least 20 times $f_{s,max}$, *i.e.*, allowing for 10 time constants [81].

2) Thus, in the Φ_2 phase, $GBW = \beta G_m/C_{Ltot} = 2\pi \cdot 40\ MHz$, where G_m is the OTA transconductance; $\beta = C_{I1}/(C_{I1} + C_{S1} + C_p)$ is the feedback factor and C_p (~ 0.5 pF) is the first OTA's input parasitic capacitance; $C_{Ltot} = C_L+(1-\beta)C_{I1}$ is the total load capacitance and C_L (~ 0.3 pF) is the OTA's load capacitor.

3) From the ADC kT/C noise requirement and the loop coefficient calculated in Section 4.3, the first integrator capacitance values are designed as $C_{S1} = 2\ pF$ and $C_{I1} = 4pF$. Therefore, we calculate $\beta = 0.62$, $C_{Ltot} = 1.8$ pF and thus $G_m = 730\ \mu$S.

4) We adopt the current-recycling folded cascode (CRFC) as our OTA topology. As discussed in Section 3.3.1, this technique was originally proposed by Bahmani *et al.* [63] in a pseudo-differential OTA, and later adapted by Assaad *et al.* [64] into a fully-differential folded-cascode topology. Fig. 4.4 shows the schematic of the OTA.

5) In comparison to a conventional FC, by equally splitting the input transistors and making a current ratio of 1:4 ($M_{11,12}$: $M_{9,10}$), the CRFC can boost the g_m and SR by 2.5 and 4 times, respectively [64]. Thus, $g_{m1\text{-}4} = G_m/5 = 146\ \mu S$. With a designed $g_m/I_D = 16$, we calculate $I_D = 9.2\ \mu A$, where I_D is the drain current of M_1 - M_4.

6) The dc gain achieved is 60 dB, with a GBW of 42 MHz and phase margin of 55°.

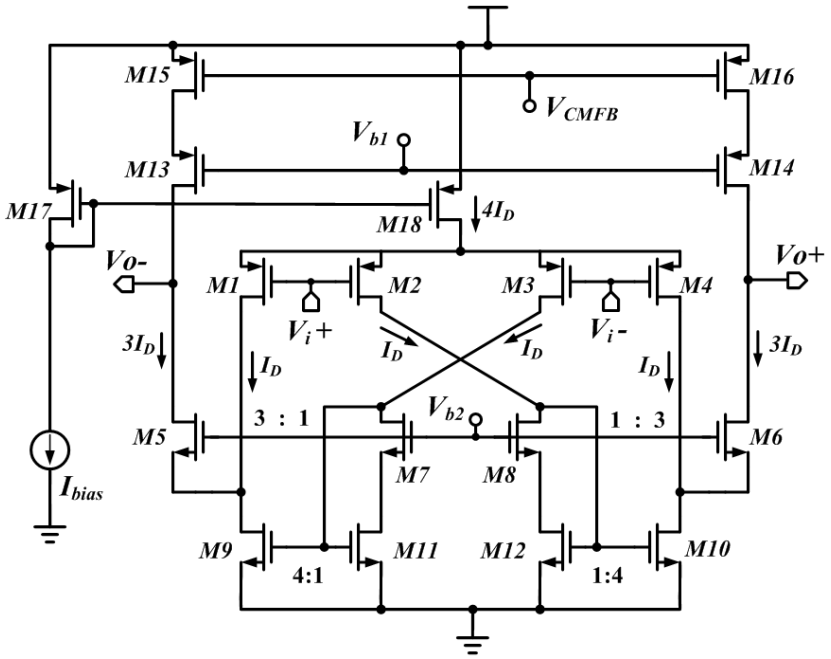

Fig. 4.4. Schematic of the first OTA in the SDM.

The first integrator accounts for 50% of the modulator power dissipation. Since the noise and non-idealities of the second integrator are attenuated by the 1st-order noise shaping, its current and capacitance are scaled by half to reduce the power consumption. For the FR recording, after the f_s and power scaling, the integrators consume about 17% power of that for AP recording.

4.3.2 Clocker Booster Design

Since the switch conductance and charge injection are signal-dependent, they may cause distortion when operating at the low clock voltage. Fig. 4.5 shows the charge pump [78] used to boost the clock signals driving the NMOS switches in the modulator.

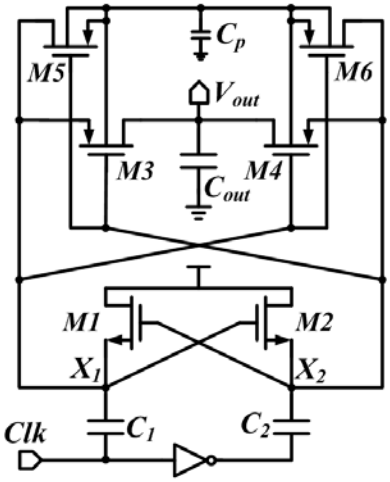

Fig. 4.5. Schematic of the charge pump.

The design procedures of this clock voltage booster are discussed here.

1) C_1 and C_2 act like two batteries storing a charge of $C_{1,2} \cdot V_{DD}$ each. $C_{1,2}$ is chosen as 50 pF to minimize the output loading effect as discussed below.

2) Driving by the clock, nodes X_1 and X_2 toggle alternatively between V_{DD} and $2V_{DD}$.

3) Two PMOS series switches M_3 and M_4 are needed to connect $2V_{DD}$ to the output alternatively. C_{out} is chosen as 100 pF.

4) To ensure the reverse bias of the vertical PN junctions, the bulk voltage of $M_{3,4}$ is always required at $2V_{DD}$. This is done by M_5 and M_6, since they always switch to the highest voltage.

5) The parasitic capacitor C_p (= *1 pF*) preserves the bulk voltage during switching.

6) All switch sizes $(W/L)_{M1\text{-}6}$ are chosen as 160μm/0.6μm. Large width and minimum length are designed to reduce R_{ON}.

The output voltage is a little lower than $2V_{DD}$ due to the loading from the stage it drives. For a V_{DD} = 2.8 V, the simulated V_{out} value is 4.5 V. For the CMOS process used in this design, a maximum gate-source voltage of 6 V can be tolerated without causing voltage stress on the transistors.

4.3.3 Comparator Design

The design of comparator can be relaxed in sigma-delta modulators, because the nonidealities of the comparator undergo the same noise shaping as the P_Q noise. Fig. 4.6 shows the comparator [82] consisting of a dynamic latch and a SR latch. It is worth mentioning that the pseudo-differential topology used here saves the comparator from

any static power consumption and is suitable for this moderate-speed (up to 2 MHz) application.

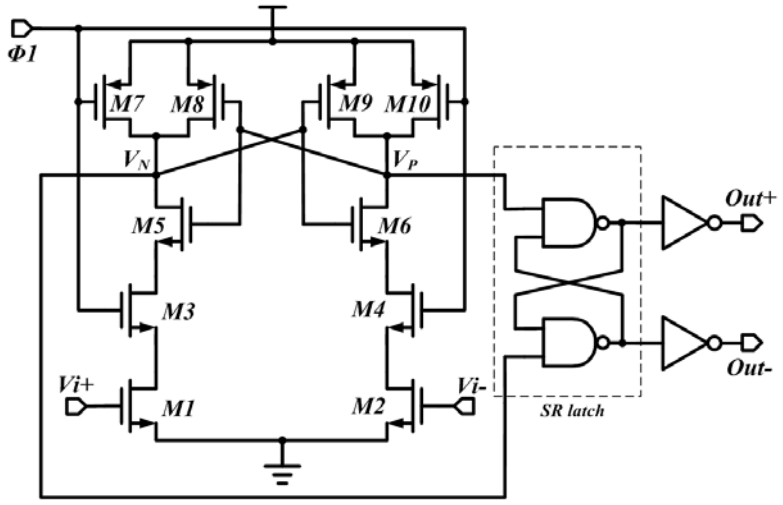

Fig. 4.6. Schematic of the comparator.

When Φ_1 is low, M_7 and M_{10} pull both nodes V_N and V_P high while M_3 and M_4 are turned off. This operation resets the dynamic latch when the SR latch locks the previous comparator decision. The comparator output controls the timing of the feedback DAC. When Φ_1 goes high, the dynamic latch regenerates the input difference into rails. The design procedures of the comparator are shown below.

1) Minimum lengths of 0.6μm are chosen for all devices $M_{1\text{-}10}$ to improve circuit speed.

2) Large width $W_{1\text{-}2} = 16\ \mu m$ is chosen for the input devices $M_{1\text{-}2}$. It improves comparator gain and matching.

3) The PMOS width $W_{8\text{-}9} = 8\ \mu m$ and NMOS width $W_{5\text{-}6} = 4.4\ \mu m$ are chosen in the dynamic latch to achieve a good balance between transconductance and parasitic capacitance, and thus improve the latch time constant, which is $\tau \approx (C_{gs}+C_{gd})/(g_{mN}+g_{mP})$.

4.4 Decimation Filter Design

A sigma-delta ADC usually consists of a sigma-delta analog modulator followed by a digital decimation filter. A decimation filter is useful to 1) lower the word rate of the oversampled signals from the modulator, 2) remove the out-of-band quantization noise, and 3) avoid the aliasing of high frequency components down to the signal band. When the power efficiency of the analog modulator keeps improving, the decimation filter becomes the bottle neck of power efficiency for the whole ADC. In the audio frequency range, the state-of-art decimation filter usually consumes tens of milliwatts [83], [84], while the modulator can consume only hundreds or even tens of μW's [80], [82]. The decimation filter also occupies larger area than the modulator. There are many research efforts through years to improve both the power and area efficiency of decimation filters. One of the popular architectures for decimation filters is the cascaded integrator-comb (CIC) filter [85]. Though the CIC structure has very simple hardware implementations, its wordlength is large in order to avoid register overflow in the integrator stages running at full sampling frequency. A polyphase decomposition technique has been developed to reduce the wordlength of comb filters, but it requires large adder trees that consume significant power [86]. A modified filter structure was

reported in [87] to improve the distribution of zeros of the CIC filter to reduce both the P_Q noise and the bit rate, but it still uses two multipliers and is not power efficient.

In this chapter, we propose a direct implementation of the impulse response (IR) of a sinc filter in the 1st stage. This simple implementation requires only one shift register and one adder as the main components. A one-multiplier structure is proposed through data pipelining for the IIR filter used in the 2nd stage. Therefore, the proposed decimation filter is area and power efficient and obviates the aforementioned problems in literature. Fig. 4.7 shows the schematic of our proposed decimation filter.

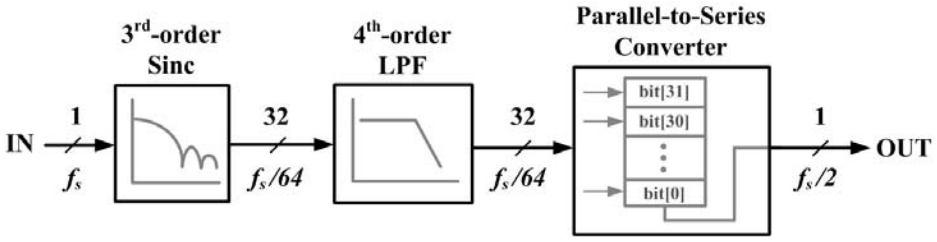

Fig. 4.7. Block diagram of the decimation filter.

The first stage is a 3rd-order sinc filter with a decimation factor of 64. A 4th-order IIR lowpass filter (LPF) follows the sinc filter to attenuate the high frequency quantization noise. The 32-bit wordlength is employed to accommodate the standard 32-bit DSP architecture in medical applications. The last stage is a parallel-to-series converter which is simply a 32-bit shift register and converts the output samples into a series bit stream. It makes the chip compatible to any module that communicates with standard SPI protocol. The specifications of each block are discussed in the following Section 4.4.1 and 4.4.2.

4.4.1 Sinc^3 Filter Design

The order of the sinc filter is chosen to be 3, because it should be at least one order higher than the modulator to ensure the filter cuts off at a faster rate than the NTF rises at high frequencies [88]. We choose the decimation factor $M = 64$, since it results in a residual *OSR* of 3.125 that can prevent passband droop, limit the increase of baseband noise to less than 0.25 dB [89] and allow enough transition band ($= f_s/M - 2f_B$) to attenuate the aliasing components. We put all the decimation factors on the 1st stage to lower the operation frequency of the succeeding stages as much as possible. It is part of the strategy to save power. The transfer function of the sinc filter is

$$H(z) = \frac{1}{M^N}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^N = M^{-N}\left(\sum_{k=0}^{M-1} z^{-k}\right)^N = M^{-N} \cdot \sum_{n=0}^{N(M-1)} a_n \cdot z^{-n}, \tag{4.4}$$

where M (= *64*) is the decimation factor, N (= *3*) is the filter order, and a_n are the filter coefficients. Fig. 4.8 shows the block diagram of the sinc^3 filter. A design procedure is provided below.

1) A shift register constantly receives the incoming bits from the SDM at the speed of f_s. The sinc filter samples *[N(M-1)+1]* (= *190*) input bits in every *64* clock cycles. This is the decimation by *64*.

2) In time domain, the output samples are

$$y_m = M^{-N} \cdot \sum_{n=0}^{N(M-1)} a_n \cdot x_{-(n+Mm)}, \; with\ m = 0, 1, 2 \ldots, \tag{4.5}$$

where $x_{-(n+Mm)}$ are the delayed input samples. The coefficients a_n can be calculated [90] as

$$a_n = \begin{cases} 0.5(n+1)(n+2), & for \quad 0 \le n < (M-1), \\ 0.5M(M+1) + (n+1-M)(2M-2-n), & for \quad (M-1) \le n < (2M-1), \\ 0.5(3M-n-2)(3M-n-1), & for \quad (2M-1) \le n \le 3(M-1), \end{cases} \tag{4.6}$$

where a_n are 12 bits long.

3) Since the input bits are either 1 or 0, 190 multiplexers can be employed to pass either a_n or 0 to a 190-input adder for implementing the summation in (4.5). No multiplier is thus needed in the first stage.

4) Finally, the decimal point of summation results is shifted left by 18 bits to realize the division by M^N.

Thanks to the decimation by 64, the combinational logic (the multiplexers and adders) has equivalently 64 clock cycles to process the data. Thus the adder is effectively running at $f_{clk}/64$, saving power and avoiding any setup time violations.

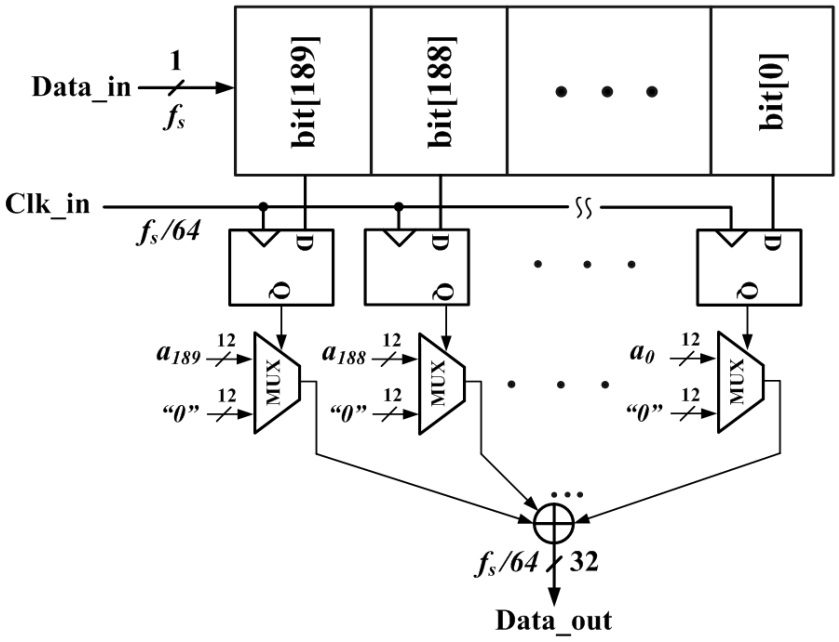

Fig. 4.8. Block diagram of the sinc^3 filter.

4.4.2 Digital IIR Filter Design

The order of the IIR filter is designed to be 4, achieving a good tradeoff between fast rolloff and small in-band ripples. The $f_{s,\,max}$ (= 2MHz) sets the maximum value of 5 kHz for the cut-off frequency (f_B). At least 90-dB stopband rejection is required to have enough attenuation of the out-of-band noise [91]. The specifications of the IIR filter are summarized in Table 4.1. In order to save both power and area, we minimize the number of multipliers to be 1 in the filter by using a novel 8-cycle data pipelining, as discussed in details later. The filter consists of two 2nd-order IIR LPF sections in cascading. The transfer function of the overall 4th order IIR LPF is

$$H(Z) = \left(\frac{A_{11} + A_{12}Z^{-1} + A_{13}Z^{-2}}{1 + A_{14}Z^{-1} + A_{15}Z^{-2}} \right) \cdot \left(\frac{A_{21} + A_{22}Z^{-1} + A_{23}Z^{-2}}{1 + A_{24}Z^{-1} + A_{25}Z^{-2}} \right). \tag{4.7}$$

Table 4.2 summarizes the filter coefficients obtained from the elliptic filter approximation by using Matlab®. Fig. 4.9 shows the block diagram of the IIR filter.

Table 4.1. Specifications of the digital IIR filter

Order	4
Max. cut-off frequency	5 kHz
Stopband attenuation	100 dB
Passband ripple	≤ 0.5 dB

Table 4.2. Coefficients of the IIR filter

A11	***A12***	***A13***	***A14***	***A15***
0.02459	0.04871	0.02459	-0.85695	0.25735
A21	***A22***	***A23***	***A24***	***A25***
1	1.892	1	-0.70812	0.65859

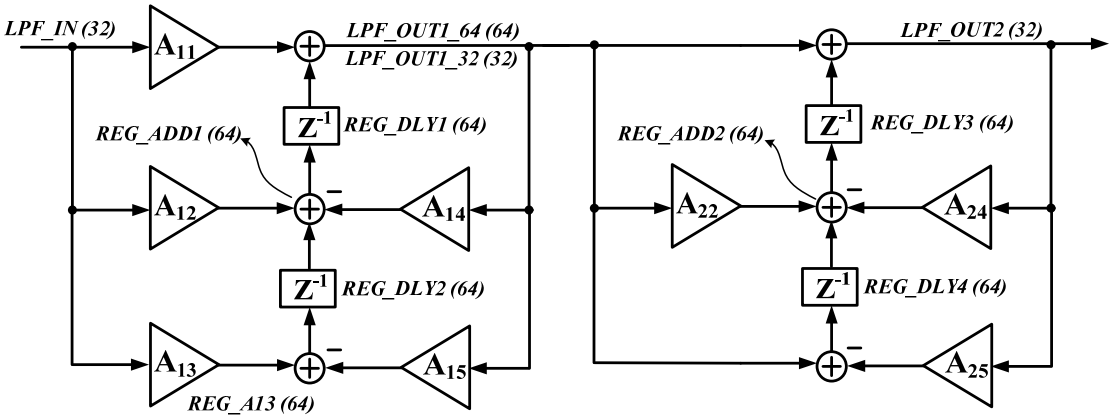

Fig. 4.9. Block diagram of the 4th-order IIR LPF.

The design procedure for the IIR filter is discussed below.

1) All the register names are shown in the figure. For example, "*LPF_OUT1_32 (32)*" denotes a register named as "*LPF_OUT1_32*" with a register length of 32 bits.

2) The filter processes data with the fixed-point arithmetic. For a 32 bit data, the first 4 bits are integer bits and the rest 28 bits are fraction bits. MSB is the sign bit. Each filter coefficient is 32 bits.

3) A 3-bit counter running at $f_{CLK}/8$ controls the operation of the filter. Table 4.3 summarizes the steps of the data pipelining based on the counter cycles. For example, during counter cycle (000), the input *LPF_IN* multiplies *A11* and then adds to the data in *REG_DLY1*. The result is 65 bits, but it gets truncated to both 64 bits and 32 bits. The registers *LPF_OUT1_64* and *LPF_OUT1_32* get updated with the 64-bit and 32-bit results, respectively.

4) The unit-delay elements (z^{-1}) are implemented by registers $REG\_DLY_{1\text{-}4}$. The unit delay is realized by the fact that these registers always participate in the computations before they get updated.

Note from Table 4.3 that every register is updated every 8 counter cycles, thus the IIR filter is effectively running at $f_{CLK}/64$.

Fig. 4.10 shows the simulated magnitude responses of the individual stages and the overall decimation filter with the sampling frequency of 2 MHz. The passband droop is less than 0.5 dB, thanks to the residual OSR of 3.125. If the signal is decimated to Nyquist rate, the droop will increase significantly and then a droop correction filter will be needed at the final stage [89].

Table 4.3. The 8-cycle data pipelining of the IIR filter

Counter cycle	***Operation***	***Register updated***
000	(LPF_IN * A11) + REG_DLY1	LPF_OUT1_32 LPF_OUT1_64
001	(LPF_IN * A12) + REG_DLY2	REG_ADD1
010	(LPF_OUT1_32 * A14) + REG_ADD1	REG_DLY1
011	LPF_IN * A13	REG_A13
100	(LPF_OUT1_32 * A15) + REG_A13	REG_DLY2
101	LPF_OUT1_64 + REG_DLY3 (LPF_OUT1_32 * A22) + REG_DLY4	LPF_OUT2 REG_ADD2
110	(LPF_OUT2 * A24) + REG_ADD2	REG_DLY3
111	(LPF_OUT2 * A25) + LPF_OUT1_64	REG_DLY4

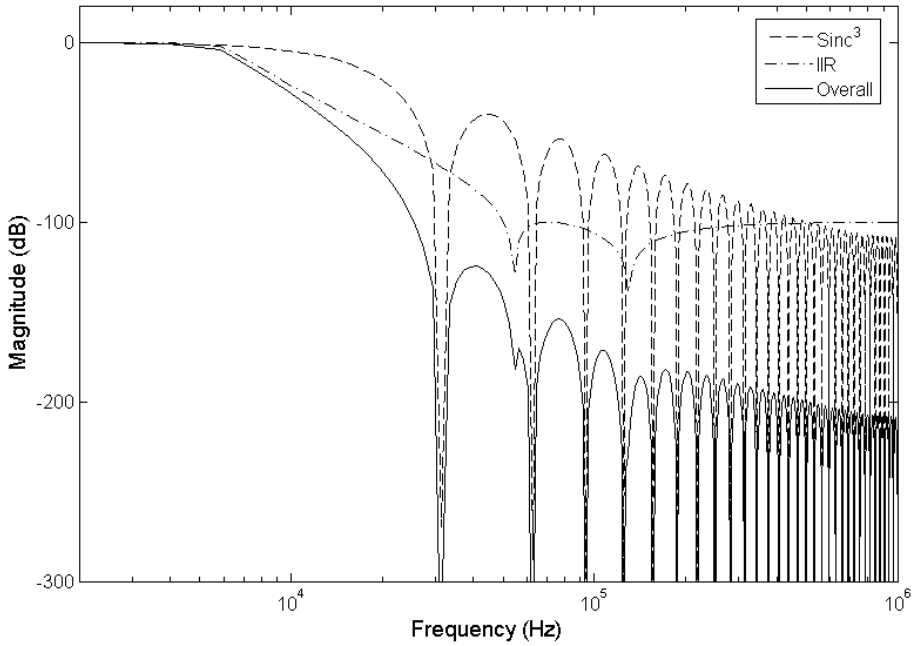

Fig. 4.10. Simulated magnitude responses of the first stage, second stage and the overall decimation filter (f_s = 2 MHz).

4.5 Experimental Results

This neural ADC was fabricated in XFab 0.6-μm CMOS process with two-poly–three-metal (2P3M) layers. An integrated I-V reference circuit is implemented to generate all the bias currents and voltages. Two regulators provide analog and digital power supplies separately. Fig. 4.11 displays the die microphotograph. The die area is 9.33 mm^2, of which the decimation filter occupies ~ 70% of area.

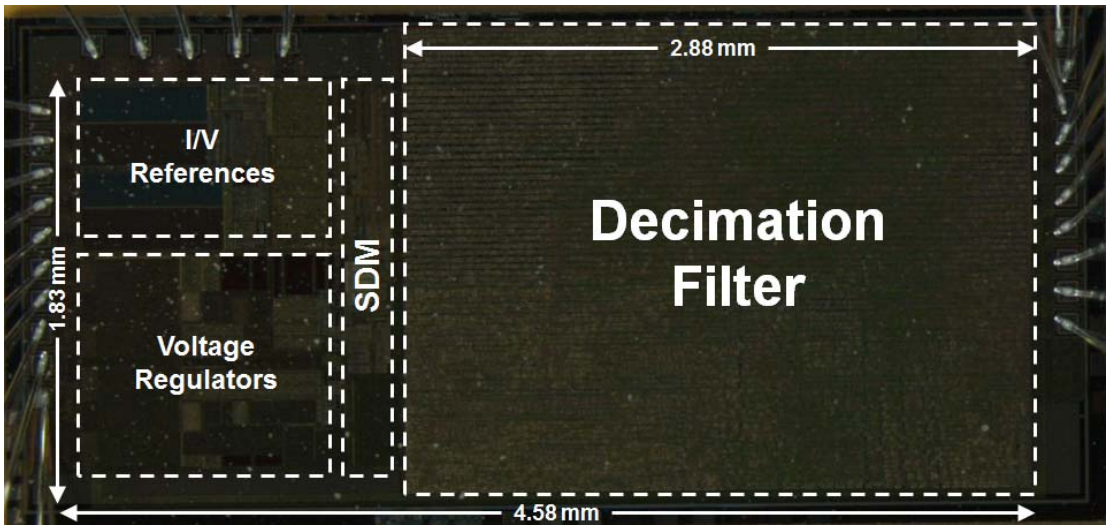

Fig. 4.11. Die microphotograph of the ADC.

The chip is sealed in the standard ceramic DIP 40-pin package and mounts to the PCB test board as shown in Fig. 4.12 for testing. Fig. 4.13 shows the test setup. A test sinusoidal signal (from an Agilent 33250 function generator) was fed into the on-board S-to-D converter, which generates the differential input signal to the ADC. A Texas Instrument (TI) MCU provides the reset and clock signals to drive the ADC. The digitized signal was fetched by the SPI interface of an oscilloscope (Agilent DSO7014A) for spectrum plotting.

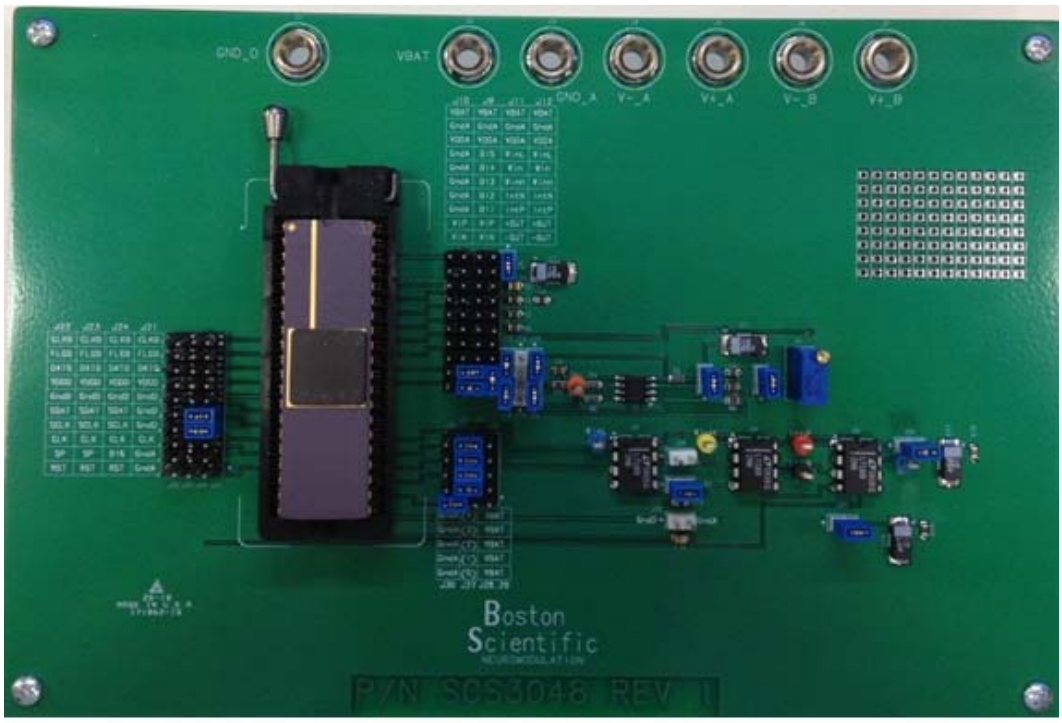

Fig. 4.12. The PCB board for ADC testing.

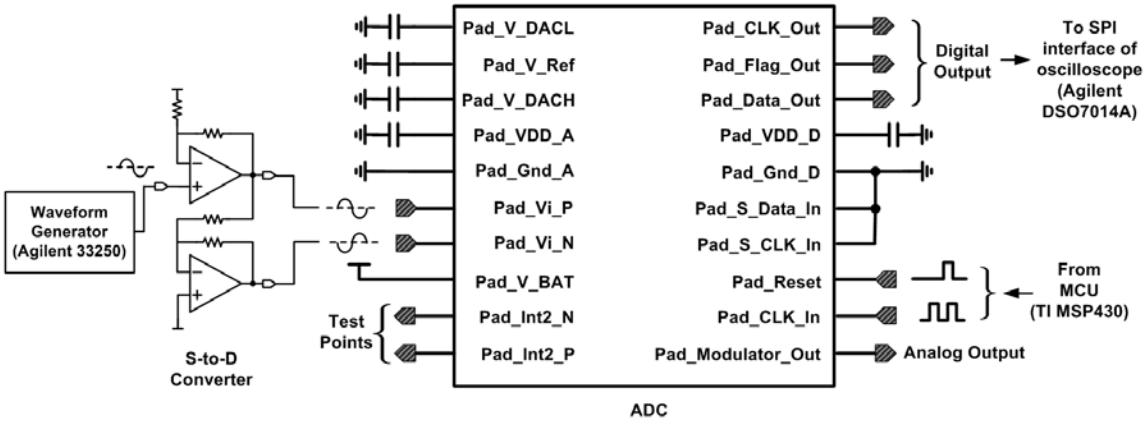

Fig. 4.13. The ADC test setup.

4.5.1 ADC Measurement Results

The ADC (modulator + decimation filter) is clocked at 2 MHz and 333 kHz for the AP and FR recordings, respectively. The series output data of the ADC is captured by the oscilloscope through the SPI interface and processed offline by software. Fig. 4.14 and Fig. 4.15 show the measured output spectra (2500-pt FFT up to $f_s/2$) of 2.3-kHz and 400-Hz inputs for the AP and FR modes, respectively.

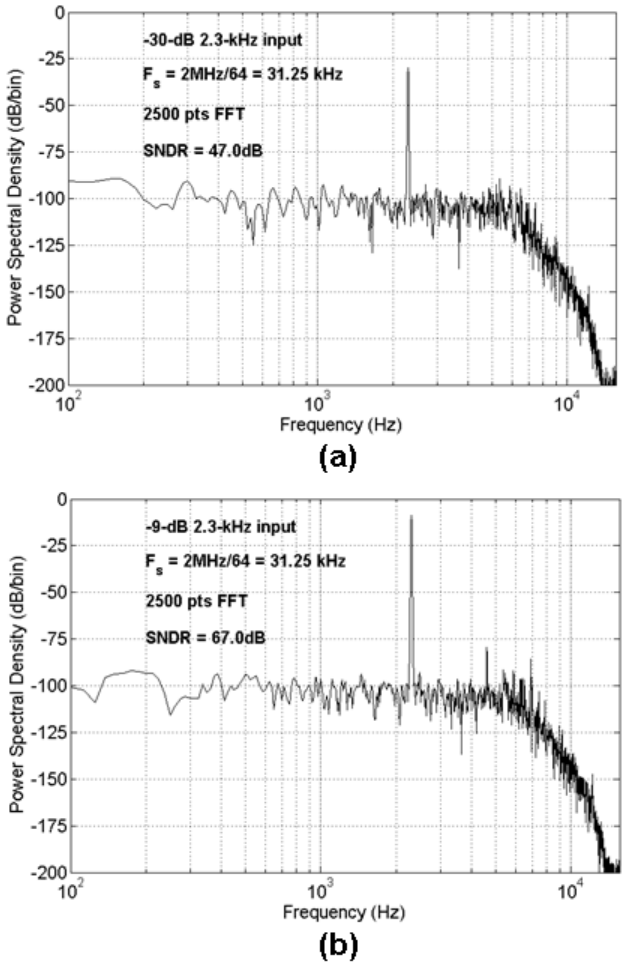

Fig. 4.14. Measured ADC output spectra of a 2.3-kHz signal tone with input level of (a) -30 dB and (b) -9 dB for AP mode.

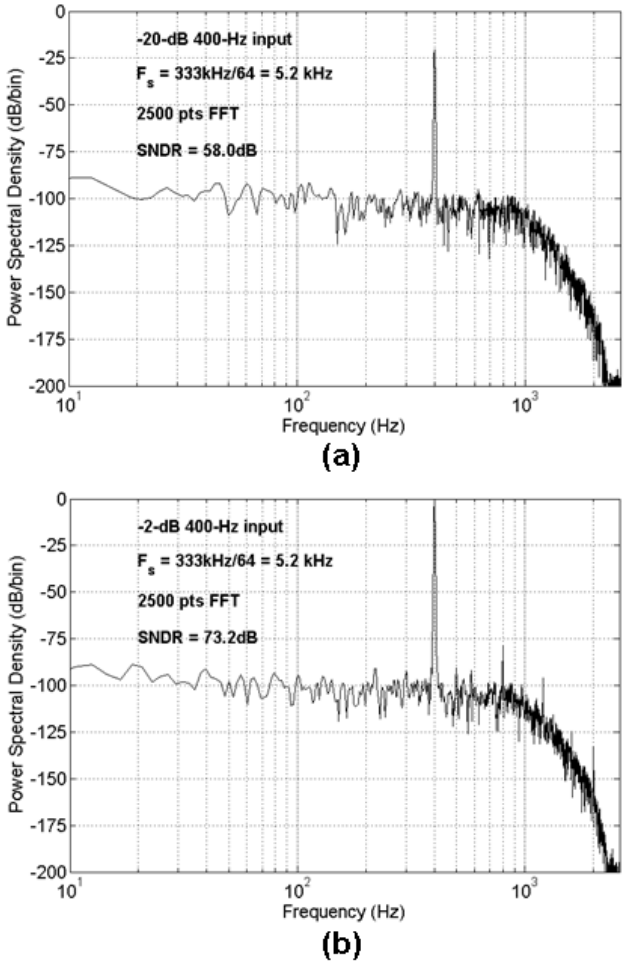

Fig. 4.15. Measured ADC output spectra of a 400-Hz signal tone with input level of (a) -20 dB and (b) -2 dB for FR mode.

They all show the out-of-band rolloff due to the digital filtering from the decimation filter and the 3.125 residual OSR. No harmonics are observed when signal is at the low levels (-30 dB for AP mode and – 20 dB for FR mode). Harmonic distortions appear in the spectra, as the input level becomes high. The peak SNDR is achieved at

input level -9 dB for AP mode and -2 dB for FR mode. Fig. 4.16 shows the measured SNR and SNDR versus the input amplitude normalized to the FSR.

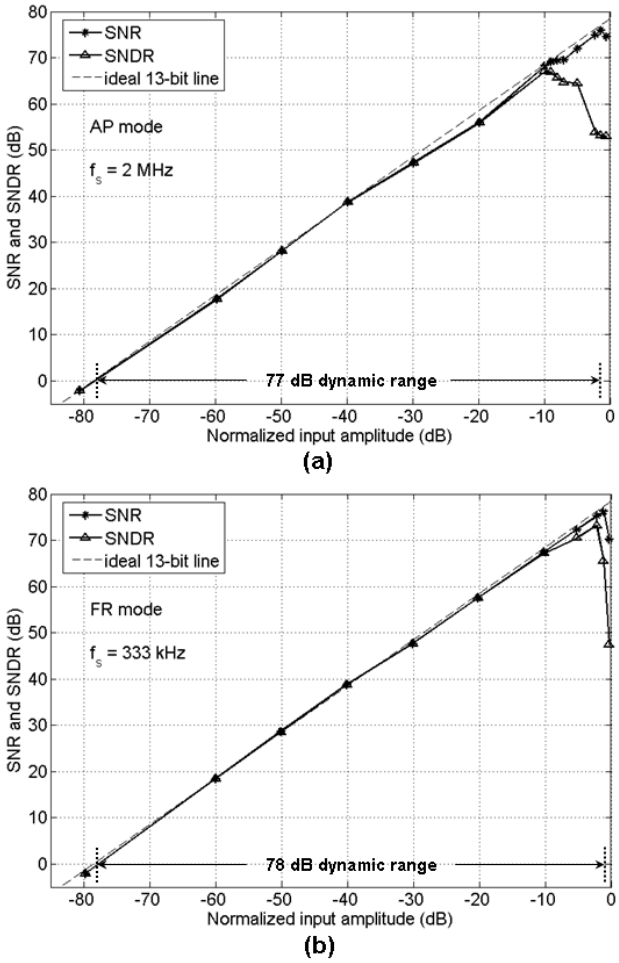

Fig. 4.16. Measured ADC SNR, SNDR and DR for (a) AP and (b) FR mode.

The peak SNR measures 75.9 dB and 76.2 dB while peak SNDR reaches 67 dB and 73.2 dB for the AP and FR modes, respectively. The dynamic range is 77 dB in 5-kHz BW for AP mode and 78 dB in 832-Hz BW for FR mode. The analog and digital

power consumption is 756 μW and 2 mW for the AP mode and 252 μW and 336 μW for the FR mode. The ADC performance is summarized in Table 4.4. The distribution of ADC power consumption is shown in Fig. 4.17. We can see the decimation filter consumes most of the power. Integrator 1 consumes the second most.

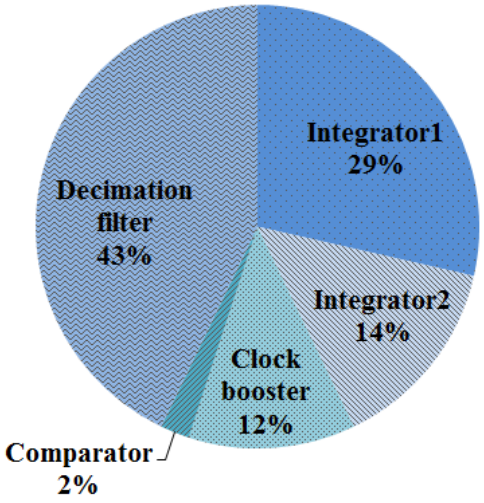

Fig. 4.17. Distribution of the ADC power consumption.

4.5.2 Comparison with State-of-the-Art Designs

For fair comparison of ADC performance, only sigma-delta ADCs with integrated decimation filter design using similar CMOS processes are selected. [36], [83], [84], [91]. Since there are not many sigma-delta ADCs reported for this neural application, the audio ADCs with similar bandwidth [83], [84], [91] are only included for reference. Table 4.4 summarizes the ADC performance from different works. The presented ADC shows comparable performance among the others and especially achieves superior power efficiency for the decimation filter design. It is worth

mentioning that our ADC performs better than [36] in terms of both speed and resolution, which is the closest system to ours for a wide range neural signal detection from spike to local field potential.

Table 4.4. Sigma-delta ADC (including decimation filter) performance references

	Mollazadeh 2009 [36]	**Nguyen 2005 [84]**	**Yang 2003 [83]**	**Maulik 2000 [91]**	**This Work**	
Applications	EEG	Audio	Audio	N/A	AP	FR
Analog Supply voltage (V)	3.3	3.3	5	5	2.8	
Digital Supply voltage (V)	3.3	3.3	1.8	3.3	2.8	
DR (dB)	55	106	114	94	77	78
Sampling frequency (MHz)	0.016	6.144	6.144	32	2	0.333
BW (kHz)	0.15	20	20	250	5	0.832
Analog power (mW)	N/A	18	55	210	0.756	0.252
Digital power (mW)	N/A	14	13	280	2	0.336
Total power (mW)	0.076	32	68	490	2.756	0.588
ADC area (mm^2)	9	1.82	5.62	21	9.23	
CMOS process	0.5 μm	0.35 μm	0.35 μm	0.6 μm	0.6 μm	

With the similar filter performance and the same-size CMOS process, we compare our decimation filter to the one reported in [91]. The digital power is proportional to CV^2f, where C is the total loading capacitance which is proportional to the total number (n) of transistors, V is the supply voltage and f is the operating frequency of the digital circuit. With the similar supply voltage, if f in [91] is scaled to the same frequency (2 MHz) as in this work, its digital power will scale down to 17.5

mW. But this scaled-down value is still much higher than its counterpart (2 mW) in this work. Two main reasons can explain the power saving of our digital filter. First, *n* is smaller than that of [91], 115 k versus 150 k. It is due to the direct IR implementation of the $sinc^3$ filter and the one-multiplier structure of the IIR filter. Second, the 8-cycle data pipelining makes the IIR filter run at effectively lower frequency than the CIC architecture does in [91].

4.6 Conclusions

A 2^{nd}-order sigma-delta ADC was proposed to digitize the neural signals for the closed-loop DBS system. The ADC is power and bandwidth configurable for recording both fast ripple and action potentials. The techniques of sinc-filter direct implementation and IIR-filter data pipelining make the decimation filter design competitive to the state-of-the-arts in terms of power efficiency.

CHAPTER V

MEASUREMENT OF THE LOW-POWER NEURAL RECORDING SYSTEM*

5.1 PCB Setup

This neural recording system was fabricated in XFab 0.6-μm CMOS process with two-poly–three-metal (2P3M) layers. All the capacitors were built as poly-poly capacitors for maximum linearity. All resistors were implemented with high-resistance polysilicon. An on-chip bandgap circuit and an I-V reference circuit generate all the reference currents and voltages for the entire chip to minimize the use of off-chip components in the neural-detection implant. Fig. 5.1 displays the die photo.

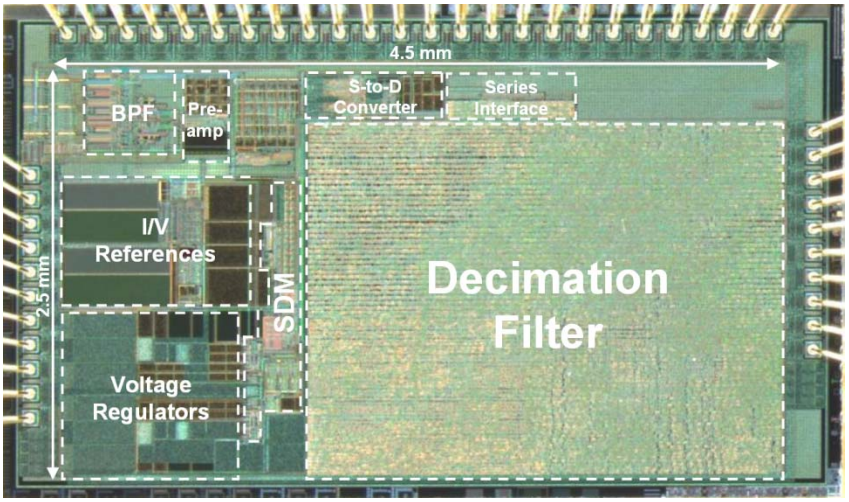

Fig. 5.1. Die microphotograph of the neural recording system.

*©[2012] IEEE. Reprinted, with permission, from "A low-power configurable neural recording system for epileptic seizure detection," by C. Qian, J. Shi, J. Parramon, and E. Sánchez-Sinencio, *IEEE Trans. Biomed. Circuits Syst.*, accepted on Nov. 12, 2012.

The total die area is 11.25 mm^2. The ADC area is 9.23 mm^2, of which the decimation filter occupies 6.43 mm^2 (70%). The die is assembled in 100-pin CERQUAD packages. The chip is soldered to a PCB for the prototype testing. The PCB setup is shown in Fig. 5.2.

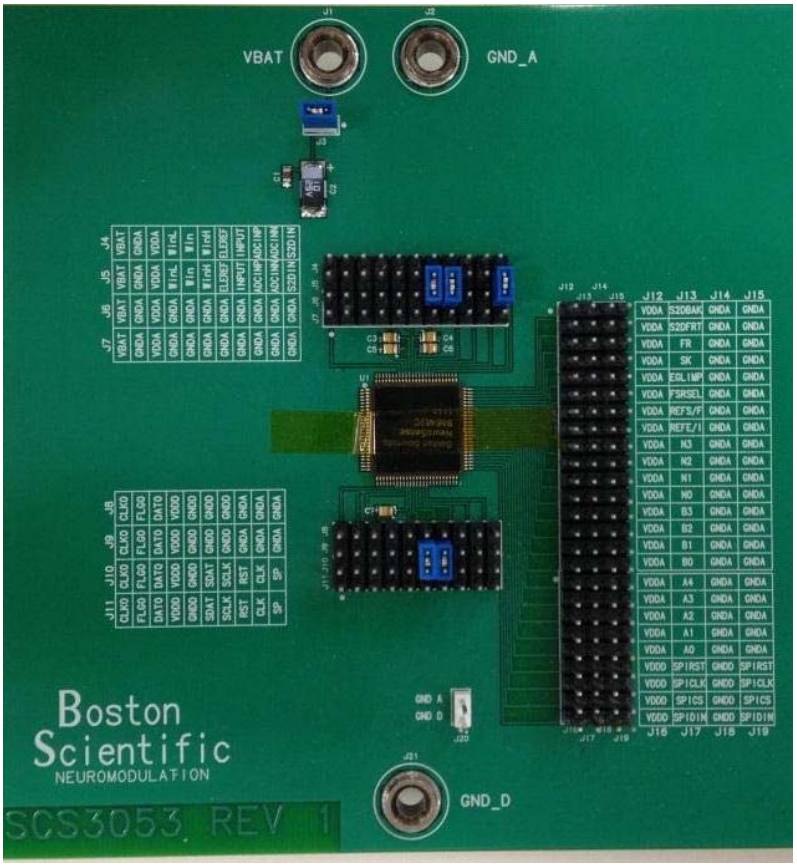

Fig. 5.2. PCB setup of the neural recording system.

5.2 Test Scheme

A TI MSP430 F2618 MCU is used for the experiment. The MCU performs two separate tasks for the measurement of the neural recording system. The 1st task is chip configuration based on the SPI transfer of the 15-bit command string to the device under

test (DUT) as discussed in Section 2.2. The 2nd task is the data fetch from DUT to the MCU memory for post data processing. The test setup is shown in Fig. 5.3. The test flow diagram for both Task 1 and 2 is shown in Fig. 5.4.

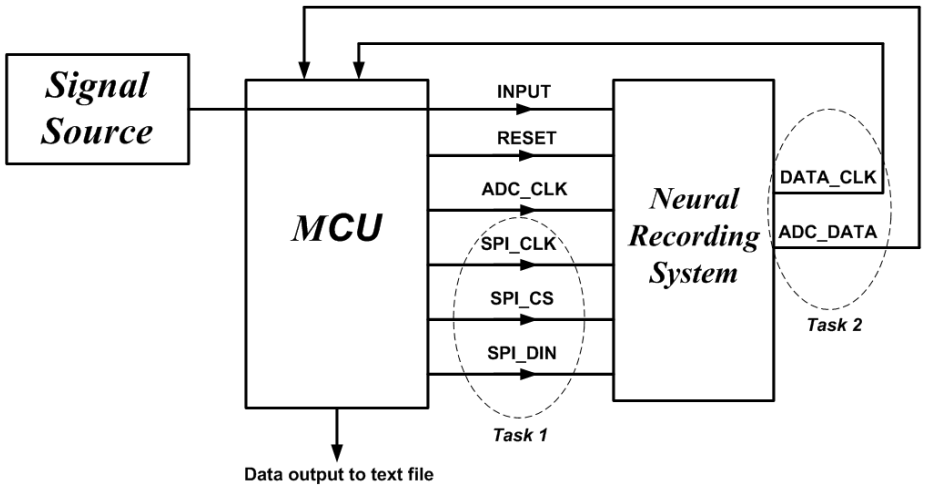

Fig. 5.3. Neural recording system test setup.

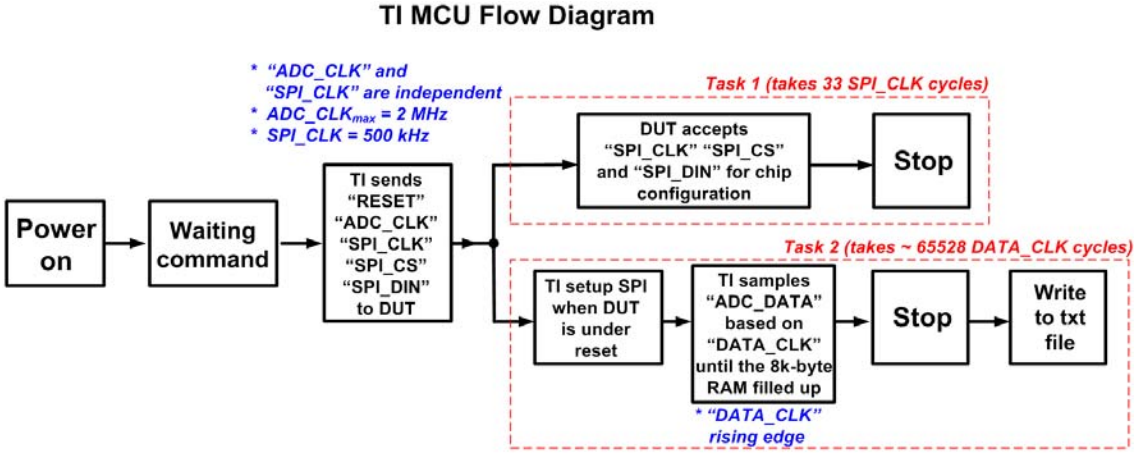

Fig. 5.4. Neural recording system test flow diagram.

Task 1 contains 3 SPI input signals to the DUT. They are *SPI_CLK*, *SPI_CS* and *SPI_DIN* as shown in Fig. 5.3. *SPI_CLK* is the divide-by-2 clock of a 1-MHz MCU system clock (*ACLK*). The clock diagram is shown in Fig. 5.5 for generating and transmitting these three SPI signals. The DUT configures itself based on the control bits contained in *SPI_DIN* signal. Note that the *SPI_DIN* is 32-bit long. It gives redundant bit space for any future commend expansion. As shown in Fig. 5.5, Task 1 takes 33 *SPI_CLK* cycles to finish. It takes the first 32 clock cycles for data stacking and the last clock cycle for transferring the 32-bit word from the shift register to chip configuration.

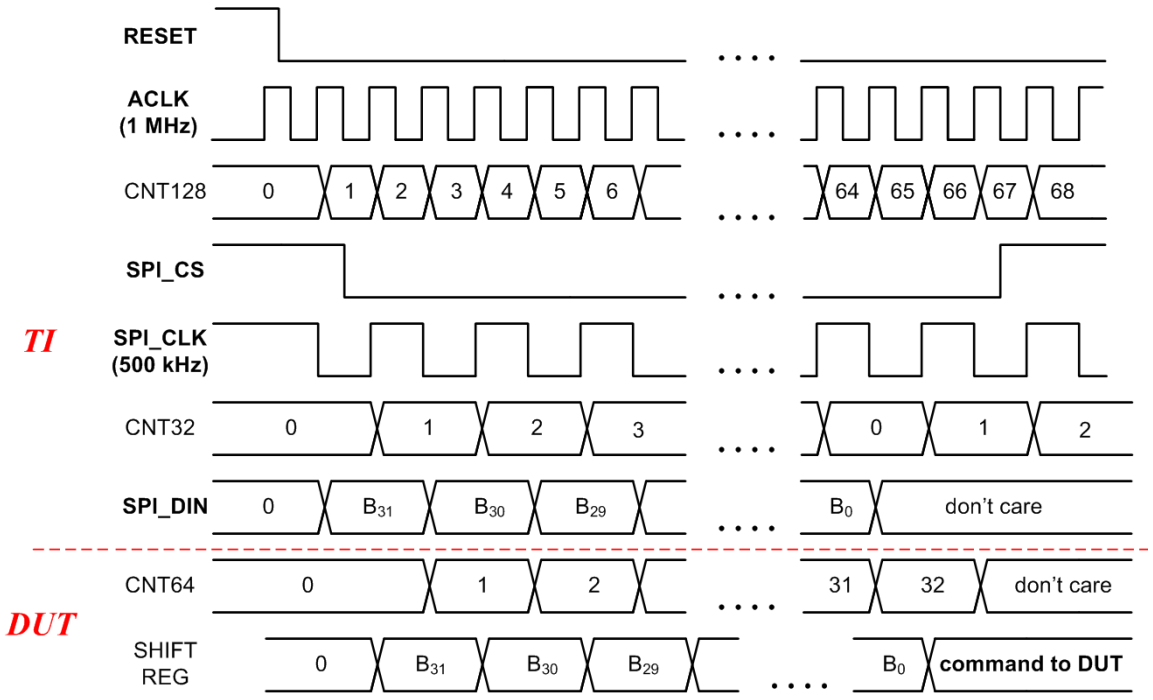

Fig. 5.5. Clock diagram for Task 1.

For Task 2, we treat the MCU as the SPI slave, with *DATA_CLK* as the master clock and *ADC_DATA* as the master-out-slave-in (MOSI) signal. The rising edge of

DATA_CLK samples *ADC_DATA* as soon as the clock starts. The clock diagram for Task 2 is shown in Fig. 5.6. The data is continuously written to the defined 8k-byte MCU memory space until it fills up. Then the fetching process stops and the MCU writes the last 8188 bytes (e.g. 2047 samples, since each sample is a 32-bit word) from the memory space to a text file. The 1st rising edge of *DATA_CLK* deterministically samples bit 23 (if LSB is bit 0). Fig. 5.7 shows the memory space after the data fill-up. Note that the nominal term "8k-byte" indicates (2^{13}-1 = 8191) bytes. The measured data is processed in MATLAB®, including FFT transformation, power spectrum plotting and SNDR calculations.

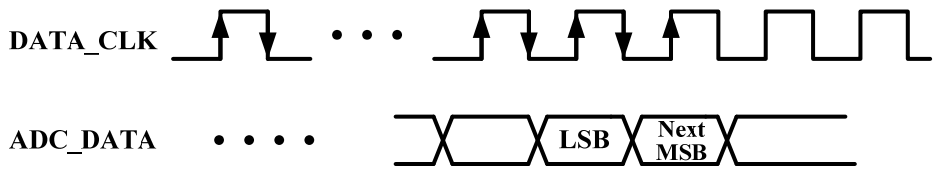

Fig. 5.6. Clock diagram for Task 2.

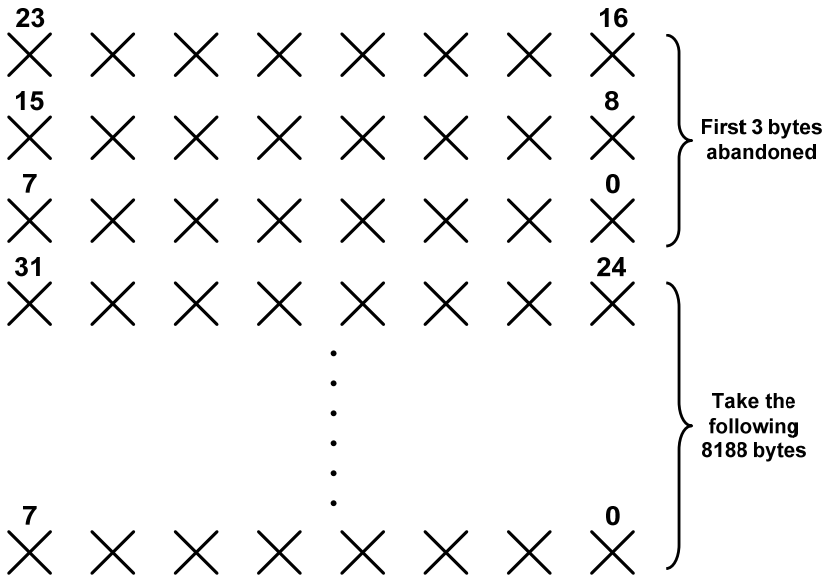

Fig. 5.7. Memory space with data filled up.

5.3 Measurement Results

We added the AP mode to the front-end circuit in this neural system chip. We briefly report here the front-end measurement results for this mode, which has not been covered in [44]. The front-end measurements in FR mode are reported in Section 3.5. For the system, both bench-top and saline-solution measurements are done to demonstrate the functionality of this neural recording prototype.

5.3.1 Additional Front-End Experimental Results for AP Mode

As a part of system measurement, Fig. 5.8 shows the measured AC response of the front-end circuit configured in AP mode. Since the signal bypasses the BPF in AP mode, the front end just consists of the preamplifier with load capacitance of 3 pF.

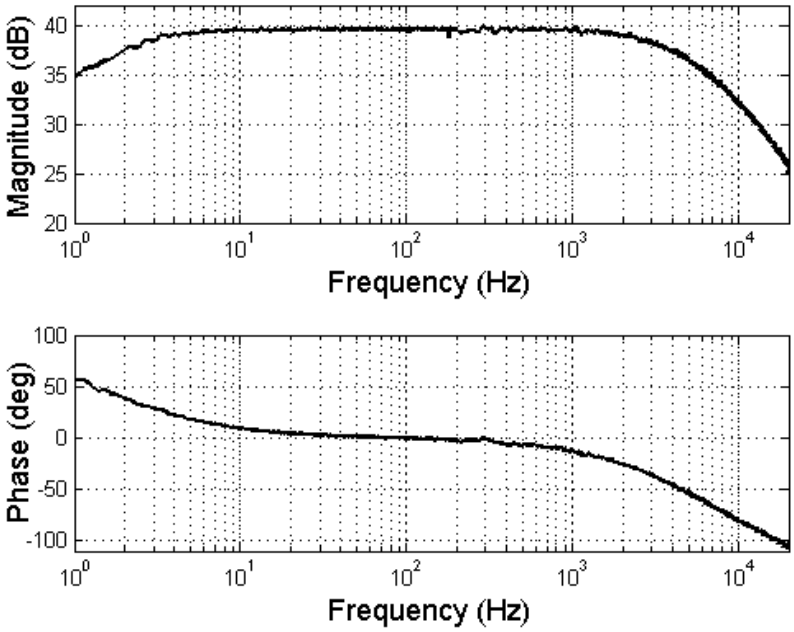

Fig. 5.8. Measured AC response of the front end in AP mode.

The measured front-end mid-band gain is 39.6 dB. The highpass and lowpass cutoff frequencies are measured at 0.8 Hz and 5.2 kHz, respectively. The input-referred noise was measured as the total output noise divided by the mid-band gain.

Fig. 5.9 plots the measured input-referred noise spectral density of the front end in AP mode. The measured spot noise at 1 kHz is 60 nV/√Hz. The 1/ f noise corner occurs near 100 Hz. The total input-referred noise of 5.86 μV_{rms} was obtained by integrating the area under the measured curve from 0.5 Hz – 30 kHz. The resulting noise efficiency factor (NEF) is 2.93. The NEF is defined as the normalization of the total input-referred noise of an OTA to that of a single-BJT amplifier with the same bandwidth and supply current [65]. The total harmonic distortion (THD) is 1% with a

maximum 10 mV_{pp} input signal. The front end consumes a total power of 2.4 μW in AP mode. The front-end performance in FR mode is presented in [44].

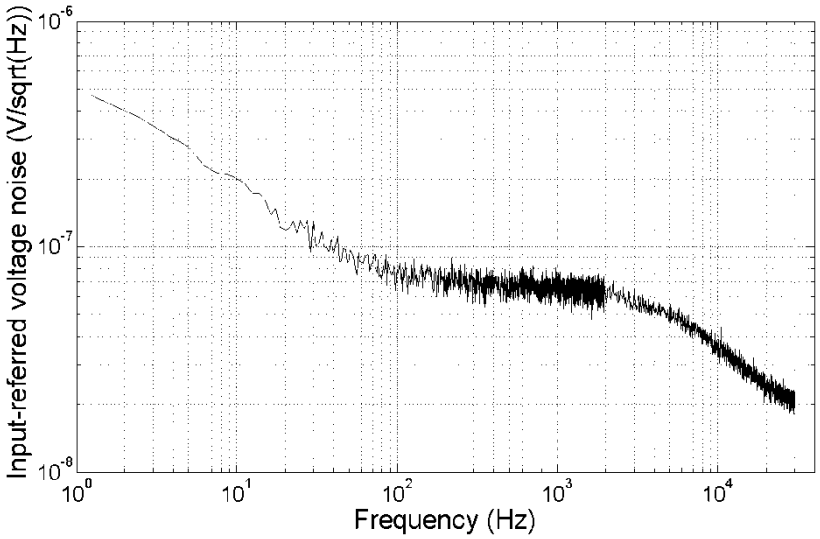

Fig. 5.9. Measured input-referred voltage noise spectrum of the front end in AP mode.

5.3.2 Neural Recording System Comparison with State-of-the-Art Designs

Table 5.1 summarizes the performance of system (front-end circuit and ADC) for both modes. It also compares this work to some reported neural recording systems [70], [71] in literature. The front-end performance is comparable to others. Our ADC design achieves superior resolution, but with larger area and higher power consumption due to different process nodes and ADC architectures from others. In comparison to [70] and [71], the uniqueness of this work is that it achieves much higher-order signal filtering and much higher-resolution of A-D conversion for FR epileptic seizure detection.

Table 5.1. Measured performance summary of the neural recording system and comparison with literature

	[70]	**[71]**	**This work [92]**	
Voltage supply	3 V	1.2 V	2.8 V	
Process	0.35 μm CMOS	0.13 μm CMOS	0.6 μm CMOS	
Applications	Epileptic Seizure	Neural Spike	Neural Spike	Epileptic Seizure
Front End				
Power consumption	4.25 μA /12.75 μW	1.6 μA /1.92 μW	0.85 μA /2.4 μW	1.6 μA /4.5 μW
Gain	73 dB	47.5 dB	39.6 dB	38.5 dB
Bandwidth	10 Hz - 5 kHz	167 Hz - 6.9 kHz	0.8 Hz - 5.2 kHz	250 - 486 Hz
Total input referred noise	6.08 μV_{rms}	3.8 μV_{rms}	5.86 μV_{rms}	2.48 μV_{rms}
NEF	5.55	2.16	2.93	7.6
Max. signal	N/A	3.1 mV_{pp} (THD 1%)	10 mV_{pp} (THD 1%)	3.4 mV_{pp} (THD 1%)
CMRR	N/A	83 dB	> 66 dB (below 5.2 kHz)	> 79 dB (250 - 500 Hz)
PSRR	N/A	N/A	> 80 dB (below 5.2 kHz)	> 68 dB (250 - 500 Hz)
Area/channel	0.02 mm^2	0.08 mm^2	0.13 mm^2	0.45 mm^2
ADC				
Architechture	SAR	SAR	Sigma-delta	Sigma-delta
Dynamic range	N/A	N/A	77 dB	78 dB
Peak SNR	N/A	N/A	75.9 dB	76.2 dB
Peak SNDR	N/A	N/A	67 dB	73.2 dB
ENOB	6.0 bits	7.62 bits	13 bits	13 bits
Sampling frequency	111 kHz	90 kHz	2 MHz	333 kHz
Bandwidth	55.5 kHz	45 kHz	5 kHz	832 Hz
Analog power	N/A	N/A	756 μW	252 μW
Digital power	N/A	N/A	2 mW	336 μW
Total power	2.77 μW	1.8 μW	2.75 mW	588 μW
Area	0.211 mm^2	0.08 mm^2	9.23 mm^2	

This design can greatly benefit from technology scaling. With advanced small-size and multi-metal-layer processes, both silicon and routing areas can be drastically reduced. For example, by switching from 0.6-μm to 0.18-μm CMOS process, the same decimation filter design can save a factor of 10 times in area, which is approximately the square of feature-size reduction. The power consumption of decimation filter can be reduced by around 100 times, since $P_{digi} \propto CV^2$, where C is the node capacitance scaled by 10 times and V is the supply voltage scaled by 3.3 times.

As mentioned in Chapter II, for the seizure detection, the ADC runs in a "one-shot" mode. It means, whenever the front end senses a pre-ictal seizure burst, the ADC is turned on briefly (up to about 20 seconds before the focal seizure spreads to other brain areas [26]). In future development, the control of "one-shot" mode can be realized by adding an analog FR-burst detector with adaptive threshold [30] in the front end. The micropower front-end circuit takes care of the long-term monitoring, thus the ADC can be deactivated during most of the time. This low-duty-cycled ADC power consumption is much lower than the stated value above. Besides, the digital power (a dominant power source in this design) can be significantly reduced by transitioning to smaller feature-size process in future implementation. This prototype IC in 0.6-μm CMOS is only a proof-of-concept.

5.3.3 System Bench-top Measurement Results

A 400-Hz sinusoidal signal with 400 μV amplitude was injected to test the system. After the 38.5-dB front-end gain (in FR mode), the output tone should be at

-21.5 dB with respect to FSR. Fig. 5.10 shows the output spectrum. The measured tone is -21.4 dB with SNDR of 55.2 dB. Compared to the ADC SNDR plot for FR mode (shown in Fig. 4.16), adding the front end only degrades the SNDR by less than 1 dB.

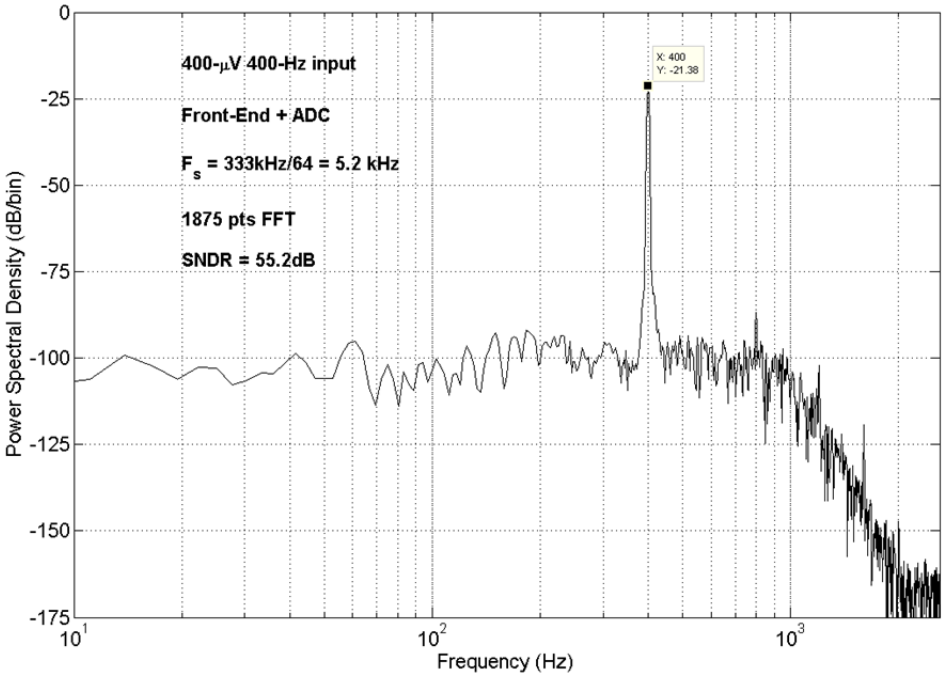

Fig. 5.10. Measured output spectrum of the system (with front end driving ADC).

5.3.4 Saline-Solution Experiments

To demonstrate the capability of seizure detection for this system, a piece of synthetic IEEG signal is generated based on the seizure data obtained from the public dataset by FHSLib [93]. The selected data was recorded differentially between left temporal lobe mesial depth (LTMD) electrode 1 and 2 from a patient. The signal shown in Fig. 5.11 demonstrates the IEEG signal that has undergone high-pass filtering and represents the FR oscillations for oncoming seizures. The electrographic seizure onset

time is also indicated in the figure. Fig. 5.11 shows the input signal to the neural system for testing purpose.

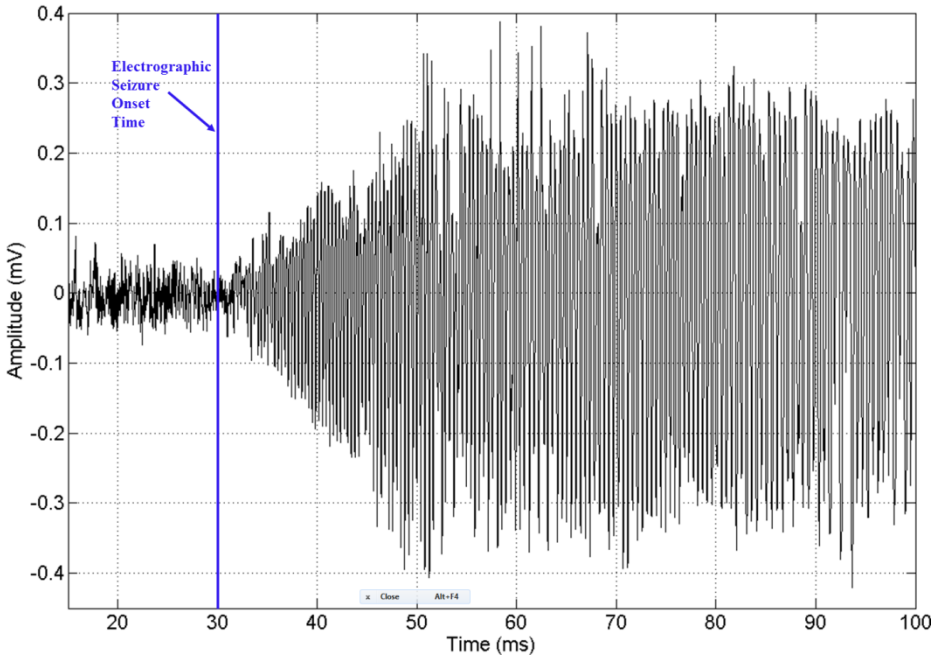

Fig. 5.11. Emulated human left temporal seizure signal.

Fig. 5.12 displays the saline-solution test setup. The artificial IEEG signal was fed into a sterilized saline solution with an 8-contact lead (Boston Scientific Neuromodulation, Model SC2108 Linear) through an Agilent 33250A arbitrary waveform generator. This ictal signal was injected into the saline solution through contact 1 of the lead. Contact 3 collected the signal. The neural front-end circuit suppressed interferers and amplified the emulated FR signal. The ADC digitized it. Fig. 5.13 shows the spectrum of the recorded electrographic seizure signal. The output signal SNDR is around 36.4 dB, which is mainly limited by the input SNDR (5.4 dB). The

SNDR improvement from input to output is due to the front-end bandpass filtering. The experimental result demonstrates the system's capability of recording FR signals at electrographic seizure onset time.

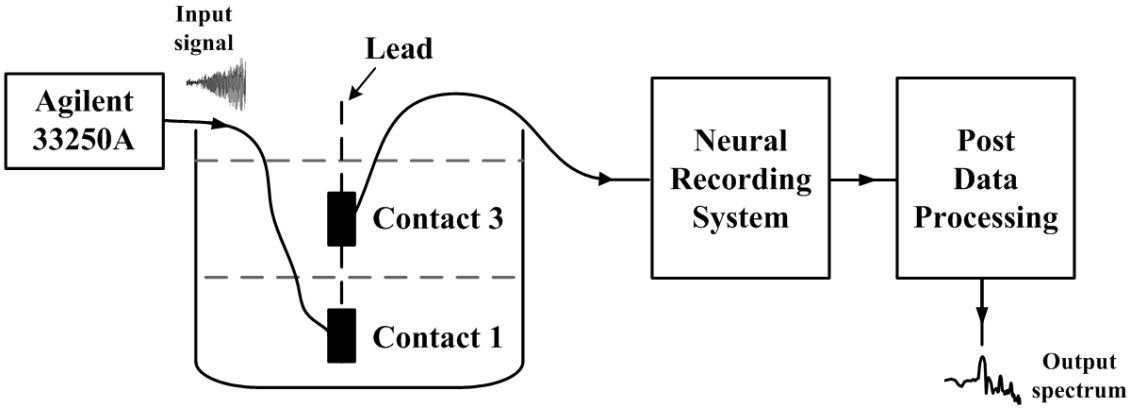

Fig. 5.12. Saline-solution test setup.

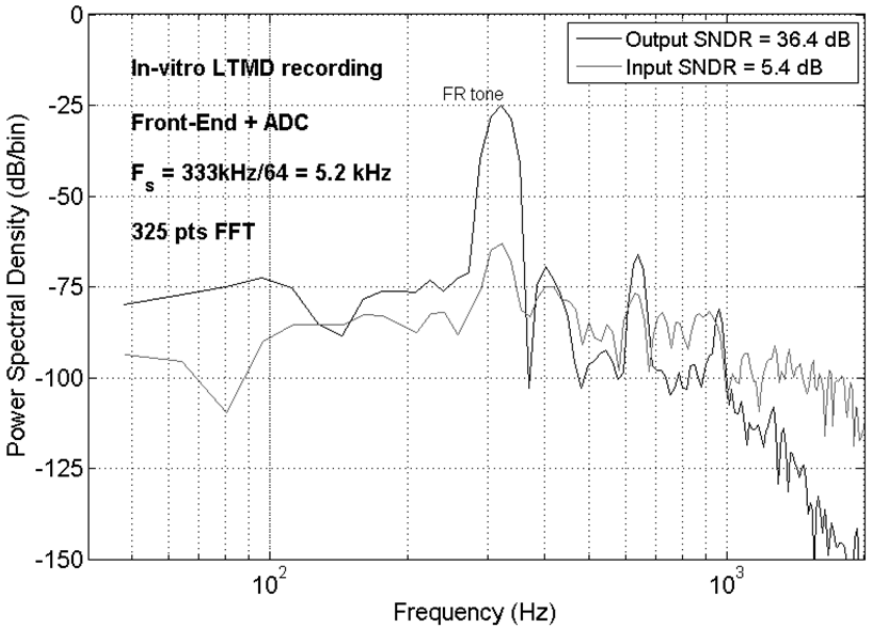

Fig. 5.13. In-vitro recording of emulated ictal seizure event.

5.3.5 Closed-Loop System Comparison

For the completeness of discussion, we have a comparison of the proposed system to state-of-the-art closed-loop seizure DBS systems. Up to date, the main stay is 8-channel sensing-stimulation channels [20], [21]. Simultaneous sensing and stimulation capabilities are already achieved in literature [20], [21], [70]. Medtronic Inc. [20] presented a closed-loop DBS device for seizure control. Multiple IC modules (*e.g.*, sensing circuitry, accelerometer and classifier) are integrated on PCB board with the existing stimulator. Several techniques are combined from front end to back end to mitigate the stimulation artifacts and realize the concurrent sensing while stimulating. Symmetrical electrode configuration is applied to minimize stimulation propagation into the signal chain. Passive common-mode filtering is used at the front-end input. Heterodyning-based BPF is embedded in the neural amplifier to attenuate stimulation interferences. On the back-end signal processor, algorithmic methods are used to further separate sensing signal from stimulation interference. A fully-integrated SOC solution would be more attractive and low cost for such a system.

Chen *et. al.* [21] recently reported the first complete silicon solution for closed-loop seizure-controlling DBS system. It achieves low-cost and low-power operation by integrating all recording, classification, and stimulation modules onto one single chip. However, it compromises the artifact-rejection performance. The sensing channels are completely saturated after stimulation and take ~1.5 seconds to recover back. This time delay may severely jeopardize the treatments in certain applications.

Shahrokhi *et. al.* [70] managed to extend the DBS system into 128 channels and

employed a reset phase to mitigate the stimulation interference issue. But the reset phase still causes delay in sensing channels. Our system proposes 16 sensing-stimulation channels with time-multiplexing operations to alleviate the artifact problem. It achieves a good balance between channel numbers, component integration and artifact immunity in comparison with other reports. Table 5.2 gives a detailed closed-loop system comparison.

5.4 Conclusions

Both bench-top and saline-solution test results are presented for the proposed neural recording system. The system demonstrated the functionality of recording electrographic seizure onset. The main contribution of this work lies in the low-power decimation filter design and the demonstration of entire system to the seizure detection based on FR sensing.

Table 5.2. Closed-loop DBS system comparison with literature

	[20]*, 2012	**[21], 2013**	**[70], 2010**	**This work [92]**
Voltage supply	1.8 V	2.0 V	3.0 V	2.8 V
Process	0.8 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.6 μm CMOS
Front End				
Power consumption/channel	2.5 μA /4.5 μW	3.3 μA /6.625 μW	4.25 μA /12.75 μW	1.6 μA /4.5 μW
Gain	46 - 64 dB	40.6 - 60.9 dB	73 dB	38.5 dB
Bandwidth	1 - 20 Hz	0.1 Hz - 7 kHz	10 Hz - 5 kHz	250 - 486 Hz
Input referred noise	1.5 μV_{rms}	5.23 μV_{rms}	6.08 μV_{rms}	2.48 μV_{rms}
NEF	29	1.77	5.55	7.6
Area/channel	5 mm^2	0.22 mm^2	0.02 mm^2	0.45 mm^2
ADC				
Architechture	N/A	DMSAR	SAR	Sigma-delta
Dynamic range	N/A	54 dB	N/A	78 dB
Peak SNR	N/A	N/A	N/A	76.2 dB
Peak SNDR	N/A	N/A	N/A	73.2 dB
ENOB	N/A	9 bits	6.0 bits	13 bits
Sampling frequency	N/A	62.5 kHz/channel	111 kHz	333 kHz
Bandwidth	N/A	7 kHz	55.5 kHz	832 Hz
Analog power	N/A	N/A	N/A	252 μW
Digital power	N/A	N/A	N/A	336 μW
Total power	N/A	5.8 μW	2.77 μW	588 μW
Area	N/A	0.495 mm^2	0.211 mm^2	9.23 mm^2
System				
# of channels	8	8	128	16
Artifact mitigation	Filtering+algorithm	None	Reset	Time multiplexing

* Front-end results for [20] are obtained from [19]; ADC is off-chip component in [19] and [20].

CHAPTER VI

CONCLUSIONS

6.1 Summary

This research discusses the architecture and challenges for epileptic seizure detection for closed-loop application. The work mainly involves two essential building blocks, the neural front-end circuit and the ADC. The methodological design and hardware implementation are presented. The saline-solution experiment is conducted to study the feasibility on biomedical applications for both building blocks.

The front end requires low-power (sub-microwatt) and low-noise (microvolt) operation for chronic monitoring of patient's brain wave signals. A combined technique of input-pair splitting and output-branch scaling is proposed to mitigate the noise-power tradeoff in preamplifier design. The designed folded-cascode amplifier achieves one of the best noise efficiency performances among reported neural amplifiers.

High-order filtering is required to fulfill modern clinical needs for automated epileptic seizure detection. It is highly desired to have analog high-order filter for neural signal pre-conditioning in low-power front-end design. A 6^{th}-order G_m-C bandpass filter with follow-the-leader feedback elliptic architecture is proposed to achieve a balance between filter sensitivity and tunability. The active source degeneration is added to the G_m cell to achieve good linearity and low-frequency operation for neural applications. The proposed filter achieves one of the best power/pole efficiencies reported to date.

A bandwidth and power scalable neural ADC is proposed. Second-order single-loop single-bit sigma-delta topology is chosen to achieve enough resolution for seizure recording with low power consumption and good stability for the analog modulator. The techniques of sinc-filter direct implementation and IIR-filter data pipelining are combined to make the decimation filter competitive to the state-of-the-arts in terms of power efficiency. The SPI interface allows for the possibility of integrating the system with any future microcontroller or DSP blocks through standard buses for implementing on-chip seizure-detection algorithms.

The performance of all proposed building blocks is verified through test chips fabricated in XFab 0.6-μm CMOS process. Besides, a complete signal-sensing channel is implemented and tested. Both bench-top and saline-solution test results demonstrate the system's capability of recording FR signals for seizure detection. The prototype circuit shows the feasibility of extending itself to a future closed-loop DBS system for the treatment of intractable epilepsy.

6.2 Future Work

For the extension of this PhD work, it would be interesting to complete the closed-loop seizure stimulation system. To accomplish this, there are more challenges besides the recording-channel development (see Section 1.3). The future work could include but not limit to 1) an ultra-low-power analog seizure warning circuit which can turn on/off power-hungry components based on the sensing of imminent FR energy bursts; 2) a DSP algorithm for reliable FR feature extraction and classification, which is

hardware and power efficient; 3) the immunity of front-end circuit to stimulation-induced artifacts.

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