LINEARITY AND NOISE IMPROVEMENT TECHNIQUES EMPLOYING LOW POWER IN ANALOG AND RF CIRCUITS AND SYSTEMS

A Dissertation

by

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Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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December 2012

Major Subject: Electrical Engineering

ABSTRACT

The implementation of highly integrated multi-bands and multi-standards reconfigurable radio transceivers is one of the great challenges in the area of integrated circuit technology today. In addition the rapid market growth and high quality demands that require cheaper and smaller solutions, the technical requirements for the transceiver function of a typical wireless device are considerably multi-dimensional. The major key performance metrics facing RFIC designers are power dissipation, speed, noise, linearity, gain, and efficiency. Beside the difficulty of the circuit design due to the trade-offs and correlations that exist between these parameters, the situation becomes more and more challenging when dealing with multi-standard radio systems on a single chip and applications with different requirements on the radio software and hardware aiming at highly flexible dynamic spectrum access. In this dissertation, different solutions are proposed to improve the linearity, reduce the noise and power consumption in analog and RF circuits and systems.

A system level design digital approach is proposed to compensate the harmonic distortion components produced by transmitter circuits' nonlinearities. The approach relies on polyphase multipath scheme uses digital baseband phase rotation pre-distortion aiming at increasing harmonic cancellation and power consumption reduction over other reported techniques.

New low power design techniques to enhance the noise and linearity of the receiver front-end LNA are also presented. The two proposed LNAs are fully differential and have a common-gate capacitive cross-coupled topology. The proposed LNAs avoids the use of bulky inductors that leads to area and cost saving. Prototypes are implemented in IBM 90 nm CMOS technology for the two LNAs. The first LNA

covers the frequency range of 100 MHz to 1.77 GHz consuming 2.8 mW from a 2 V supply. Measurements show a gain of 23 dB with a 3-dB bandwidth of 1.76 GHz. The minimum NF is 1.85 dB while the input return loss is greater than 10 dB across the entire band. The second LNA covers the frequency range of 100 MHz to 1.6 GHz. A 6 dBm third-order input intercept point, IIP3, is measured at the maximum gain frequency. The core consumes low power of 1.55 mW using a 1.8 V supply. The measured voltage gain is 15.5 dB with a 3-dB bandwidth of 1.6 GHz. The LNA has a minimum NF of 3 dB across the whole band while achieving an input return loss greater than 12 dB.

Finally, A CMOS single supply operational transconductance amplifier (OTA) is reported. It has high power supply rejection capabilities over the entire gain bandwidth (GBW). The OTA is fabricated on the AMI 0.5 um CMOS process. Measurements show power supply rejection ratio (PSRR) of 120 dB till 10 KHz. At 10 MHz, PSRR is 40 dB. The high performance PSRR is achieved using a high impedance current source and two noise reduction techniques. The OTA offers a very low current consumption of 25 uA from a 3.3 V supply.

DEDICATION

To my great parents, my beloved sister, Maha, and my lovely wife, Salma.

ACKNOWLEDGEMENTS

Before any one, I am thanking Allah the almighty for his blessing and mercy.

I am thankful to the members of my committee, Professor Sebastian Hoyos, the chair of the committee and my research advisor, Professor Edgar Sanchez-Sinencio, Professor Laszlo B. Kish, and Professor Mahmoud El-Halwagi, for their support, guidance, and helpful suggestions. Their guidance has served me well.

I wish to acknowledge all my colleagues, from the Analog Mixed Signal Center (AMSC) for their inspiring discussions and help. Special thanks to my friend and roommate, Ahmed Alaa Helmy. His friendship, assistance, and valuable discussions have meant more to me than I could ever express.

I would like to acknowledge my parents for their love that provided me with inspiration and support at each stage of my life. I owe them everything and wish I could show them just how much I love and appreciate them. I am also thankful to my sister, Maha, for her continuous support during this research work. I wish to thank my wife, Salma, for her encouragement during the last stage of my PhD. Her love and support allowed me to finish this journey. Finally, I would like to dedicate this work to all my family. I hope that this work makes you proud.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

Within the last two decades, Number of wireless standards for wireless communication has increased at a tremendous pace: Cellphones (GSM, EDGE, CDMA, W-CDMA,UMTS etc), communication networks (WIFI 802.11 a/b/g, bluetooth, WiMax, UWB etc), satellite services (GPS). The resulting crowded spectrum and the increase of users' demand for flexibility and mobility have pushed the evolution of transceivers compatible with as many different standards and frequency bands as possible. And since the sky has no limits, the progress in wireless communications never stops. A strong potential, in the last decade, has been directed to the idea on multi-bands, multi-standards on the same chip, which enables the user to access different communications wireless standards from single portable small device. Together these developments have imposed great challenges in the design of the wireless transceivers and puts tremendous efforts on RFIC designers to provide solutions and overcome problems especially with the rapid growth of CMOS technology into deep sub-micron.

The implementation of highly integrated multi-bands and multi-standards reconfigurable radio transceivers is one of the great challenges in the area of integrated circuit technology today. In addition the rapid market growth and high quality demands that require cheaper and smaller solutions, the technical requirements for the transceiver function of a typical wireless device are considerably multi-dimensional. The major key performance metrics facing RFIC designers are power dissipation, speed, noise, linearity, gain, and efficiency. Beside the difficulty of the circuit design due to the trade-offs and correlations that exist between these parameters, the situation becomes more and more challenging when dealing with multi-standard radio

systems on a single chip and applications with different requirements on the radio software and hardware aiming at highly flexible dynamic spectrum access.

From the RF transmitter point of view nonlinearity due to DACs, mixers, and power amplifiers (PA) creates spectral growth outside the signal band which interferes with adjacent channels. Also, the nonlinearity causes distortion within the signal band which increases the bit error rate after reception. Therefore, transmitter building blocks should be designed to meet both the linearity requirements and the desired transmit spectrum mask.

From the RF receiver point of view, the quality of a communication system is mainly influenced by the sensitivity of the receiver, which is defined as the minimum detectable signal the receiver can catch. A critical receiver stage is the first amplifier, low noise amplifier (LNA), that should have a low noise figure (NF) as well as sufficient gain to provide high sensitivity and also a high dynamic range. Dynamic range is set by the difference between linearity and sensitivity performance. Both metrics continue to become progressively challenging in many systems, for example, linearity requirements are becoming increasingly severe in many cases due to greater spectrum usage to avoid intermodulation products from strong signals. The third-order intermodulation products have substantial influence on the receiver performance. These undesired signals appear in a band close to the operating frequency and cause interference in the receiver system. In most cases intermodulation can be reduced by increasing the current through the active device however this will increase the power consumption which is an essential design factor to be reduced for of longer battery life and lower cost solutions.

Another important source of noise, beside the thermal and flicker noise coming from the circuit active and passive device, is the power supply noise which can significantly decrease the performance by reducing the dynamic range of the whole

system especially, in high precision systems or if the circuits that are sensitive to supply noise are at the very beginning of the power supply/reference chain. Reducing the supply noise and having higher rejection is very essential and challenging in System-on-Chip (SOC) design of modern integrated circuits that have employed analog building blocks to be placed on the same die together with noisy digital circuitry.

In this dissertation, four different projects are presented that have proposed solutions to improve the linearity, reduce the noise and power consumption in analog and RF circuits and systems. The dissertation is organized as follows: Chapter 2 provides a system level design digital approach to compensate the harmonic distortion components produced by transmitter circuits' nonlinearities. The approach relies on polyphase multipath scheme uses digital baseband phase rotation pre-distortion aiming at increasing harmonic cancellation and power consumption reduction over other reported techniques. Chapters 3 and 4 provides new low power design techniques to enhance the noise and linearity of the receiver front-end LNA. Both proposed LNAs are fully differential and have a common-gate capacitive cross-coupled topology. The proposed LNAs avoids the use of bulky inductors that leads to area and cost saving. Prototypes are implemented in IBM 90 nm CMOS technology for the two LNAs. Circuit implementations are presented for the LNAs along with simulation results and measurements. In Chapter 5, a CMOS single supply operational transconductance amplifier (OTA), with high power supply rejection ratio (PSRR), is presented. A high output impedance current source and noise reduction techniques are used to improve of PSRR both at DC and at higher frequency up to the gain bandwidth (GBW) of the OTA, respectively. The presented OTA has a simple structure and it offers a very low current consumption compared to other reported structures. Chapter 6 concludes.

2. A MULTI-PHASE MULTI-PATH TECHNIQUE FOR DISTORTION CANCELLATION*

Nonlinearities in transmitter circuits, such as power amplifiers (PAs), cause degradation in system performance and adjacent channel spectral growth interference. Poly-phase multi-path is considered among the techniques that can compensate the nonlinearities, creating a clean output spectrum. However, the poly-phase technique requires analog phase shifters which consume considerable power. Aiming at reducing the power consumption, this work presents a novel multi-phase multi-path technique with digital phase shifters. The technique is capable of canceling most of the harmonic and intermodulation products produced by a current-output nonlinear circuit to achieve the required linearity. The proposed system has advantages over existing poly-phase techniques in power consumption, accuracy, and flexibility. However, it lacks image rejection and local oscillator harmonic cancellation. Detailed analyses and simulations of the new technique are provided to show the effectiveness of the harmonic distortion cancellation.

2.1 Introduction

In RF transmitters, nonlinearity due to DACs, mixers, and power amplifiers (PAs) creates spectral growth outside the signal band, which interferes with adjacent channels. Also, the nonlinearity causes distortion within the signal band, which increases the bit error rate after reception. Therefore, transmitter building blocks should be designed to meet both the linearity requirements and the desired transmit spectrum mask.

*Part of this chapter is reprinted with permission from "A Multiphase Multipath Technique With Digital Phase Shifters for Harmonic Distortion Cancellation," by E. A. Sobhy and S. Hoyos, Dec. 2010. *IEEE Trans. Circuits Syst. II*, vol. 57, no. 12, pp. 921-925.

Cartesian feedback (CFB) [1, 2] is one of the methods to linearize an RF transmitter and enhance the spectral purity of nonlinear circuits. CFB is an analog solution that achieves high efficiency and shows robustness to process parameters, supply voltage, and junction temperature (PVT) variations, but has phase alignment limitations and stability issues [2]. Digital predistortion [3, 4, 5] is also a linearization solution. It is cost efficient but its accuracy is limited by the predistorter design and the degree it tracks the nonlinearity.

Another solution to cancel the distortion products is using the poly-phase multi-path technique [6, 7], in which the authors use several frequency-independent phase shifters in a multi-path topology. Two sets of phase shifters are used: one before and another after the nonlinear block to cancel the unwanted signal. The poly-phase multi-path technique significantly relaxes the requirements on the high quality band-pass LC filters used in conventional transmitters to remove the unwanted harmonics and sidebands. This makes the poly-phase circuits very attractive in multi-standards and cognitive radio transmitter architectures. In order not to increase the system complexity over a single path topology, the poly-phase technique is used with current-output nonlinear circuits [6], where the area and current are split into multi paths. In [6], a current-output power upconverter (PU) architecture is designed based on the poly-phase multi-path technique to produce a clean output spectrum. No RF filters are used at the output, aiming at software-defined radio applications. As reported in [6], the chip consumes 228 mW. A large portion of the consumed power, 156 mW, is used to realize the second set of phase shifters.

In this work, a novel multi-phase multi-path architecture is presented that no longer uses the analog phase shifters after the nonlinear block. Instead, these de-rotation phase shifters are moved to the digital front-end together with the original rotation phase shifters. This new digitally generated multi-phase topology has ad-

vantages over the architecture in [6] such as flexibility, power saving, and robustness to mismatches. These advantages come out at the cost of some signal loss, which can be minimized by proper choice of the digital phase shifts, double sideband transmission, and non-cancellation of the local oscillator (LO) harmonics that can be filtered out using a low quality bandpass filter. The Chapter is organized as follows. In Section 2, background on the poly-phase architecture in [6] is summarized. Section 3 covers the new proposed solution, showing the analyses and simulations for single and two-tone tests. In Section 4, mismatches between paths are considered. Applications are presented in Section 5.

2.2 Background

Fig. 2.1 shows the poly-phase multi-path technique presented in [6]. The input signal, at frequency ω, is injected into N paths with matched nonlinear circuits. In each path, the signal undergoes equal phase rotation and de-rotation before and after the nonlinear circuit, respectively. The output spectrum of the nonlinear block has frequency components at ω and also at multiples of ω due to harmonic distortion. The phase shift vector $\underline{\varphi} = [\varphi_1, \varphi_2, ..., \varphi_N]$ is chosen such that phases between paths are equidistant $[\varphi_j = 360(j-1)/N,\ j = 1, 2, 3..., N]$. Choosing such a phase shift vector results in equal phases for the desired fundamental signals at the end of each path. Therefore, they are aligned to add up coherently. On the other hand, the undesired distortion components tend to cancel out after addition, except for the harmonics at $(PN+1)\omega$, where $P = 0, 1, 2, ...$ In the case of two input tones at ω_1 and ω_2, the nonlinear block not only generates harmonics of the two tones but also intermodulation products at $m\omega_1 + n\omega_2$, where m and n are negative and positive integers. Cancellation of the intermodulation products follows the same principle as canceling the harmonics. Once again, the intermodulations at $m + n = PN + 1$,

where $P = 0, 1, 2, ..,$ are not canceled by this scheme. This means that whatever the values of N and $\underline{\varphi}$ are, some intermodulation components are never canceled.

One of the challenges of the architecture in Fig. 2.1 is the phase shifter design after the nonlinear circuit, which is implemented in the analog domain, contrary to the first set of phase shifters, which is implemented in the digital domain [8]. Harmonics at the output of the nonlinear circuit require de-rotation by a constant phase over a wide band. The architecture in [6] implements the second set of phase shifters using mixers of identical LO frequencies with different phases, as shown in Fig. 2.2. These phases are generated by digital circuits (dividers and buffers) that consume 69% of the total chip power [6]. Also, mismatches between these phases affect the magnitude of canceled harmonics and intermodulations. Another point is that the poly-phase circuit in Fig. 2.2 cannot be used if the PA is implemented after the mixer because the de-rotation cannot be done before the nonlinear circuit. Therefore, this topology is restricted to using the PU architecture that combines the functionality of the PA and the upconversion mixer.

2.3 Proposed system

The proposed multi-phase multi-path circuit is shown in Fig. 2.3. The main idea is to implement both phase shifts (rotation and de-rotation) in the digital domain before the nonlinear block. The digitally rotated data is driven to multiple DACs to generate the multi-phase baseband signals. Moving the de-rotation phases to the digital domain requires proper choice of $\underline{\varphi} = [\varphi_1, \varphi_2, ..., \varphi_N]$ to cancel the undesired distortion products. In such a way, the second set of analog phase shifters in [6] is avoided. As noted above, this would save 69% of the total power consumption in the implementation of [6]. Also, having full digital control on the shifters in the baseband leads to high accuracy in generating the phases. Hence, more immunity

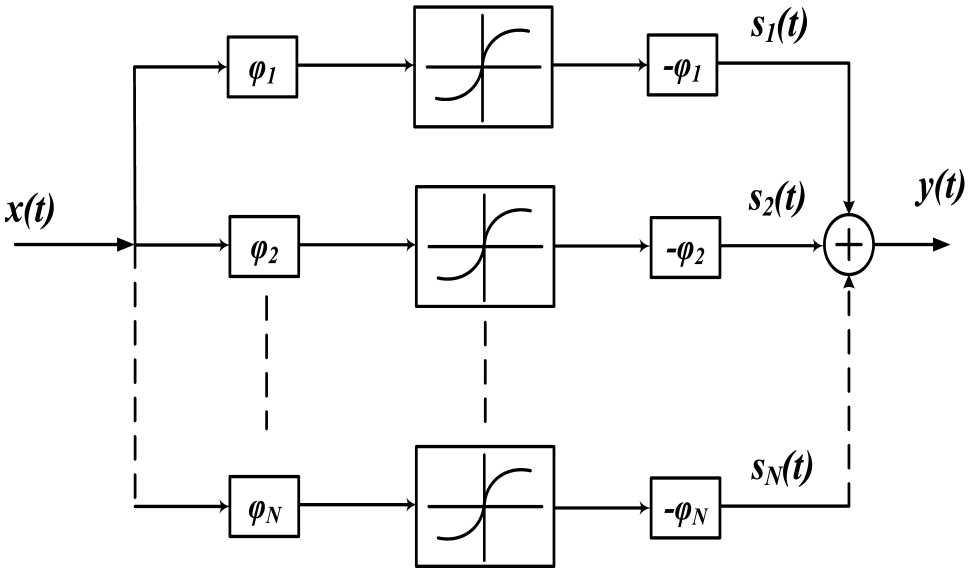

Figure 2.1: Poly-phase multi-path technique proposed in [6].

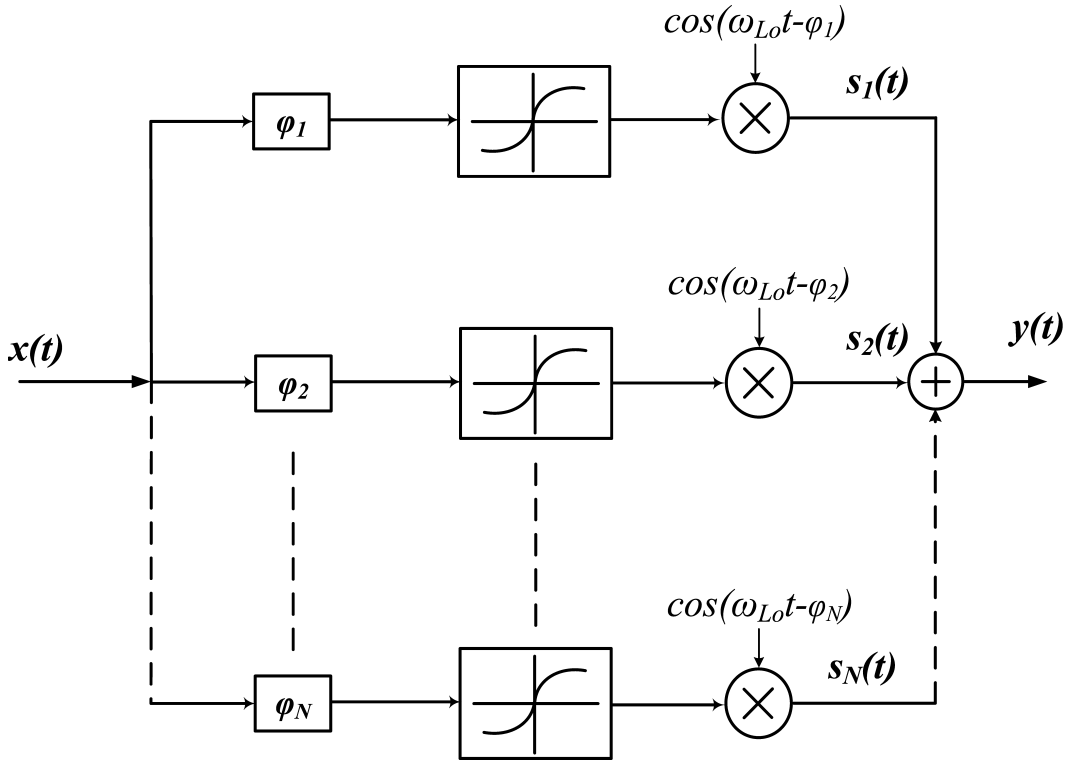

Figure 2.2: Poly multi-path technique implemented with mixers that operate as wide-band phase shifters.

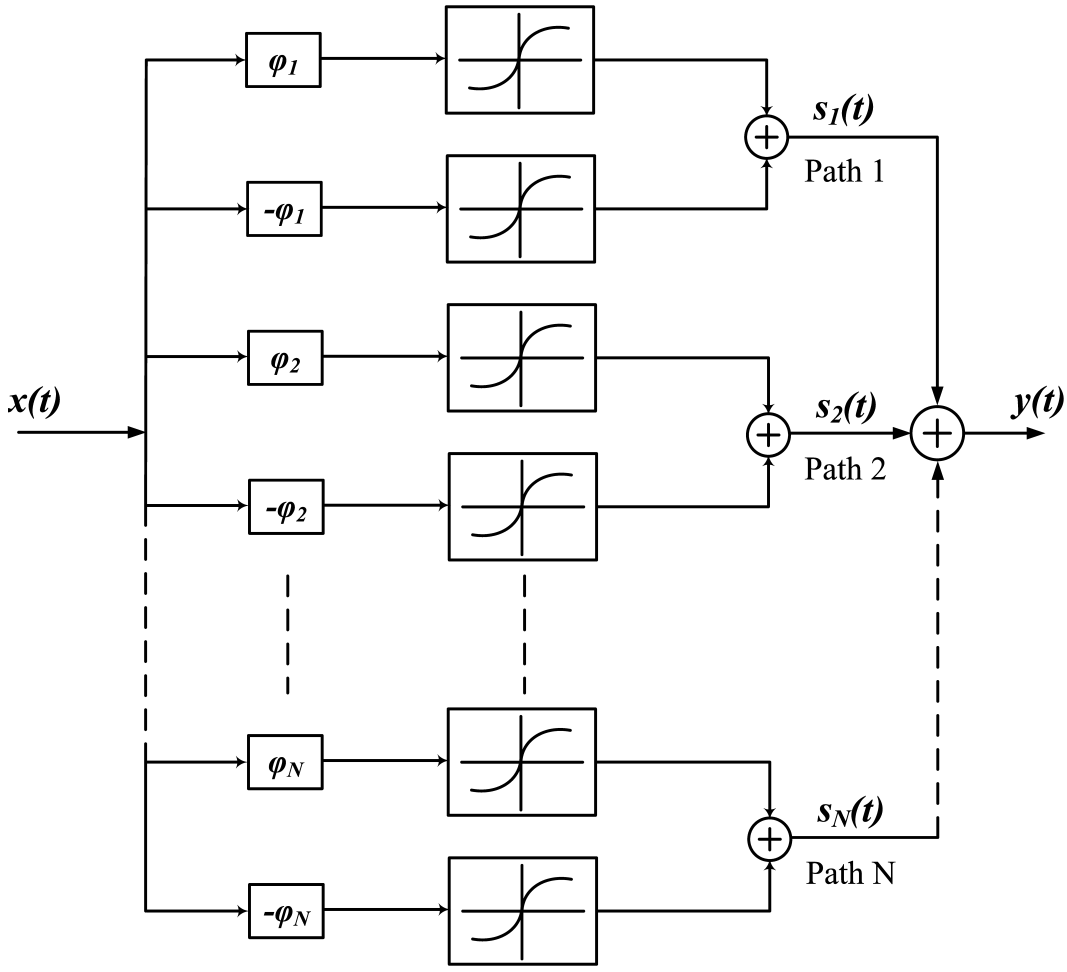

Figure 2.3: Proposed multi-phase multi-path technique.

to mismatches is achieved. Moreover, the proposed technique can be applied to conventional transmitter architectures, where the mixer is followed by a current-ouput PA that is split into multi-PAs in the RF section, as will be shown in Section V. It is worth mentioning that the proposed technique is more suitable to be used with communication systems that use complex-valued constellations, such as QPSK, that have a double sideband spectrum. In contrast, the reported technique in [6] can be used for single sideband transmission because it is capable of canceling one of the LO sidebands. The following subsections show how to choose N and $\underline{\varphi}$ in the proposed technique to cancel the harmonics and intermodulations.

2.3.1 Single-tone test

Consider a sinusoidal baseband signal, $x(t) = A\cos(\omega t)$, applied to the proposed system in Fig. 2.3. Assume the nonlinear block has a memoryless characteristic given by $w(t) = \sum_{k=0,1,2..} a_k u^k(t)$ where $u(t)$ and $w(t)$ are the input and output, respectively, and a_k is constant for all values of k. The signal, $s_j(t)$, at the end of path j, where $j = 1, 2, 3, ...N$, is given by

$$\begin{aligned} s_j(t) &= \sum_k a_k A^k[\cos^k(\omega t + \varphi_j) + \cos^k(\omega t - \varphi_j)] \\ &= \sum_k b_k[\cos(k\omega t + k\varphi_j) + \cos(k\omega t - k\varphi_j)] \\ &= \sum_k 2b_k \cos(k\omega t)\cos(k\varphi_j). \end{aligned} \tag{2.1}$$

where b_k depends on a_k and A for all values of k. After adding the signals at the end of each path, the output signal $y(t)$ will be given as

$$y(t) = \sum_k \left[2b_k \cos(k\omega t) \sum_j \cos(k\varphi_j) \right]. \tag{2.2}$$

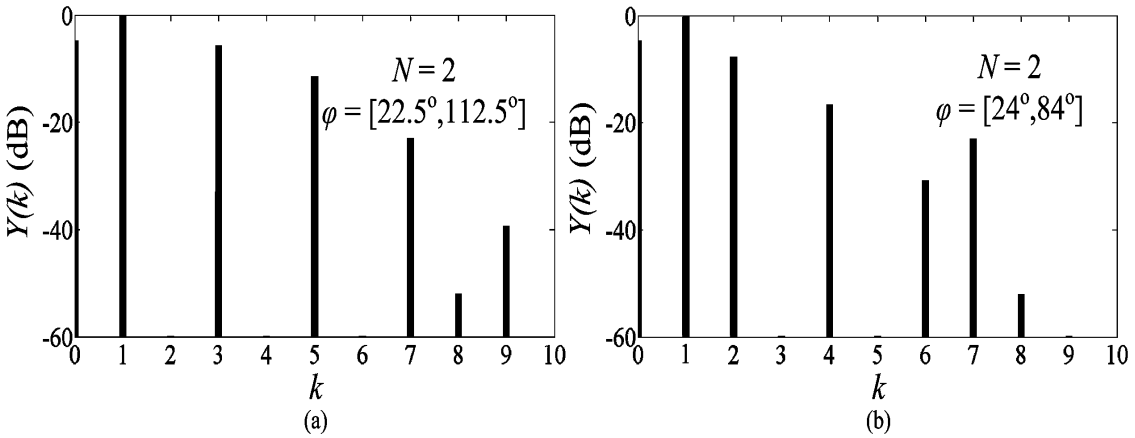

Figure 2.4: Output spectrum of the proposed multi-phase scheme for a single-tone input. (a) $N = 2$ and $\varphi = [22.5^o, 112.5^o]$. (b) $N = 2$ and $\varphi = [24^o, 84^o]$. $a_k = [0, 1, 0.2, -1.6242, 0.5, 2.638, 0.7, -4.284, 0.8, 6.954]$.

From the above equation, each harmonic is multiplied by a factor $\gamma_k = 2\sum_j \cos(k\varphi_j)$. Canceling the kth harmonic requires choosing $\underline{\varphi}$ such that γ_k is equal to zero except at $k = 1$, which corresponds to the desired signal component. For example, choosing $N = 2$ and $\underline{\varphi} = [22.5^o, 112.5^o]$ results in $\gamma_k = 0$ for $k = 2, 4, 6$. Thus, the 2nd, 4th, and 6th harmonics are canceled. Also, $N = 2$ and $\underline{\varphi} = [24^o, 84^o]$ cancel the 3rd, 5th, 9th harmonics, and any harmonic $k = 3^r 5^t$ for all non-negative r and t. To verify the previous analysis, simulations are done for the proposed system when a single-tone input is applied using ideal phase shifters and nonlinear circuits. The spectrum of the system output, $Y(k)$, is plotted in Fig. 2.4, which illustrates the harmonic cancellation.

2.3.2 Two-tone test

In order to test the proposed architecture performance on intermodulation products, a two-tone input signal, $x(t) = A_1 \cos(\omega_1 t) + A_1 \cos(\omega_2 t)$, is applied. The signal

at the end of path j is given by

$$\begin{aligned} s_j(t) &= \sum_k 2[b_k \cos(k\omega_1 t) + c_k \cos(k\omega_2 t)] \cos(k\varphi_j) \\ &+ \sum_{m,n} 2d_{m,n} \cos[(m\omega_1 + n\omega_2)t] \cos[(m+n)\varphi_j]. \end{aligned} \tag{2.3}$$

where b_k, c_k, and $d_{m,n}$ depend on a_k, A_1, and A_2 for all non-negative integers k and positive or negative integers values of m and n. From the above equation, the output of the nonlinear circuit not only includes the harmonics of the input tones, but also contains the intermodulation products at $\omega = m\omega_1 + n\omega_2$. The system output signal $y(t)$ is given by

$$\begin{aligned} y(t) = &\sum_k \left\{ 2[b_k \cos(k\omega_1 t) + c_k \cos(k\omega_2 t)] \sum_j \cos(k\varphi_j) \right\} \\ &+ \sum_{m,n} \left\{ 2d_{m,n} \cos[(m\omega_1 + n\omega_2)t] \sum_j \cos[(m+n)\varphi_j] \right\} \end{aligned}$$

$$\begin{aligned} &= \sum_k [b_k \cos(k\omega_1 t) + c_k \cos(k\omega_2 t)]\gamma_k \\ &+ \sum_{m,n} d_{m,n} \cos[(m\omega_1 + n\omega_2)t]\gamma_{m,n}. \end{aligned} \tag{2.4}$$

Eqn. (2.4) shows that the same factor γ_k is multiplied by the intermodulation terms by replacing k with $m+n$. Therefore, if N and $\underline{\varphi}$ are chosen to cancel the kth harmonic, the intermodulation products at $m\omega_1 + n\omega_2$ with $m+n=k$ are also canceled. Fig. 2.5 shows the simulation results of a two-tone test. Fully differential operation for the circuit model employed in the implementation is assumed to cancel the even nonlinearities. Fig. 2.5(a) shows the output spectrum without distortion cancella-

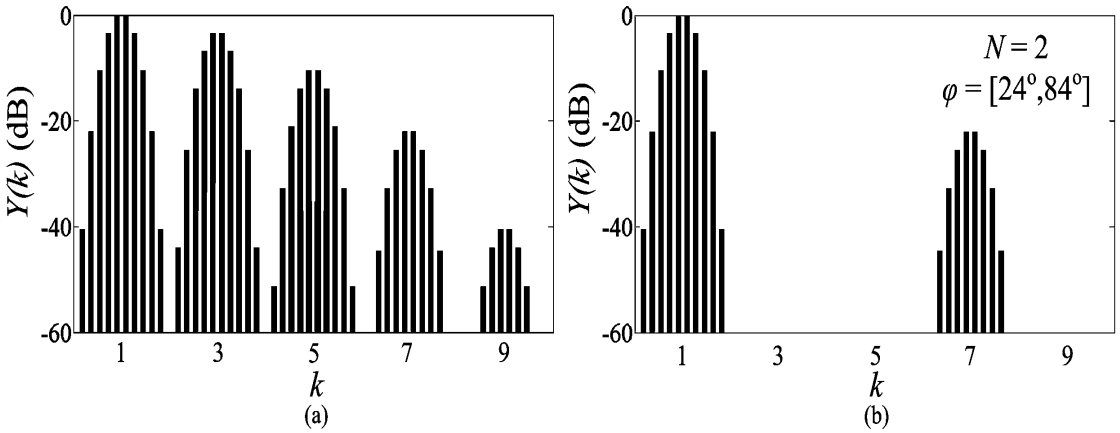

Figure 2.5: Output spectrum for a two-tone input. (a) Without distortion cancellation. (b) Proposed multi-phase with $N = 2$ and $\varphi = [24^o, 84^o]$. $a_k = [0, 1, 0, -1.6242, 0, 2.638, 0, -4.284, 0, 6.954]$.

tion. Choosing $N = 2$ and $\underline{\varphi} = [24^o, 84^o]$ cancels the harmonics and intermodulation products of $k = m + n = 3$, 5, and 9 as shown in Fig. 2.5(b). Unfortunately, the intermodulation products at $\omega = m\omega_1 + n\omega_2$ with $m + n = 1$ are not canceled. Specially important in RF applications, are the third-order intermodulation products $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$. Cancellation of this group would also cancel the fundamental desired signal at $k = 1$, as explained in [6].

Note that the fundamental components at the output of each path in the proposed system do not add up in phase, which is an advantage in [6]. This attenuates the fundamental signal, which is multiplied by a factor γ_1 according to (2.2) and (2.4), and degrades the amount of power that can be delivered to the output. To quantify this, in the above mentioned example where $N = 2$ and $\underline{\varphi} = [24^o, 84^o]$, the output fundamental signal is degraded by 5.8 dB. Fortunately, this degradation can be minimized by using another set of phase shifts, $\underline{\varphi} = [12^o, 48^o]$, achieving the same performance. A loss of only 1.68 dB results in this case, which is acceptable and can be compensated by spending some extra transmission power.

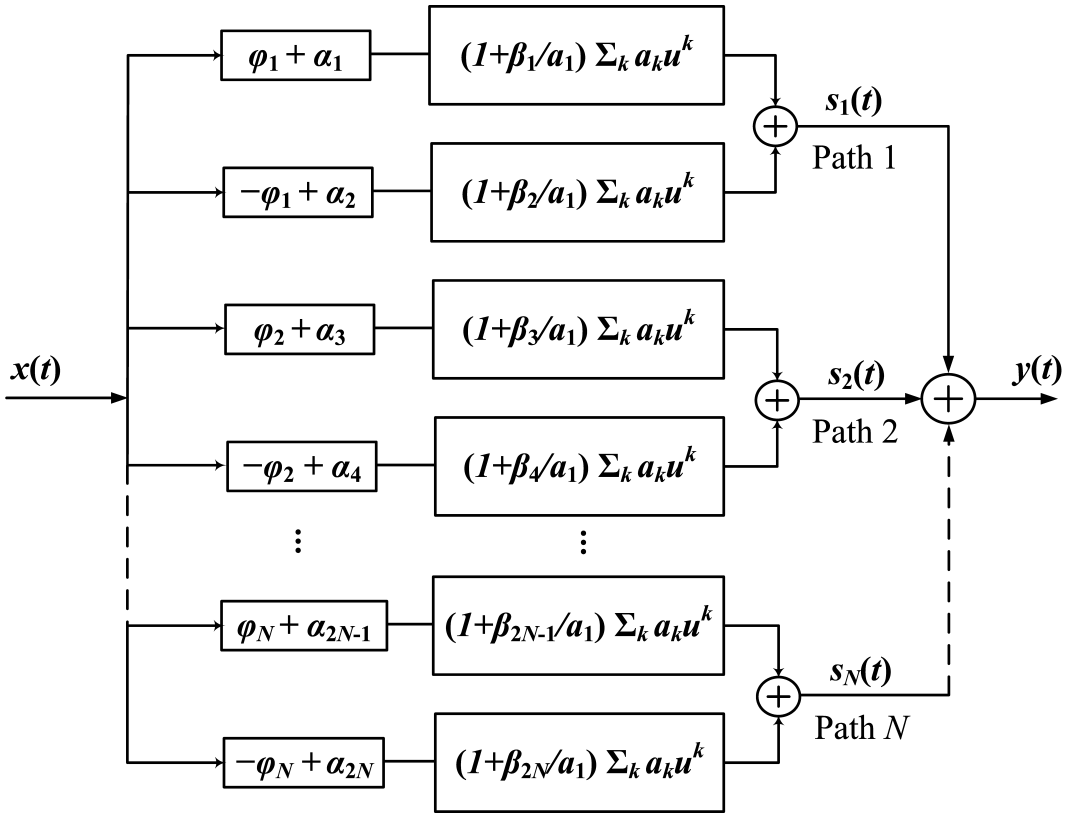

Figure 2.6: Proposed multi-phase multi-path system with gain and phase mismatches included.

2.4 Mismatches

In the previous section, the analysis was based on ideal phase shifters and identical nonlinear blocks. Gain and phase mismatches certainly affect the magnitude of the canceled harmonics and intermodulation. In order to quantify the impact of mismatches, a phase error vector $\underline{\alpha} = [\alpha_1, \alpha_2, \alpha_3, ..., \alpha_{2N}]$ and a gain error vector $\underline{\beta} = [\beta_1, \beta_2, \beta_3, ..., \beta_{2N}]$ are introduced, as depicted in Fig. 2.6. As an example, we study the effect of mismatches on the proposed system when configured to cancel the third harmonic for a single-tone input $x(t) = A\cos(\omega t)$. The system uses one path $(N = 1)^{\dagger}$ and $\underline{\varphi} = [30^o]$, which results in $\gamma_3 = 0$ in the matched case. Considering

$^{\dagger}N = 1$ means two subpaths with φ_1 and $-\varphi_1$ in the proposed technique, as indicated in Fig. 2.3

mismatches, $\underline{\alpha} = [\alpha_1, \alpha_2]$ and $\underline{\beta} = [\beta_1, \beta_2]$, the output of the proposed system $y(t)$ is given by

$$\begin{aligned} y(t) &= \sum_k b_k \Bigg[\left(1 + \frac{\beta_1}{a_1}\right) \cos(k\omega t + k\varphi + k\alpha_1) \\ &+ \left(1 + \frac{\beta_2}{a_1}\right) \cos(k\omega t - k\varphi + k\alpha_2) \Bigg] \\ &= \sum_k b_k \left[I_k \cos(k\omega t) - Q_k \sin(k\omega t) \right] \end{aligned} \tag{2.5}$$

where

$$\begin{aligned} I_k &= \left(1 + \frac{\beta_1}{a_1}\right) \cos(k\varphi + k\alpha_1) \\ &+ \left(1 + \frac{\beta_2}{a_1}\right) \cos(-k\varphi + k\alpha_2) \end{aligned} \tag{2.6}$$

$$\begin{aligned} Q_k &= \left(1 + \frac{\beta_1}{a_1}\right) \sin(k\varphi + k\alpha_1) \\ &+ \left(1 + \frac{\beta_2}{a_1}\right) \sin(-k\varphi + k\alpha_2). \end{aligned} \tag{2.7}$$

In this case, the kth harmonic distortion HD_k is given by

$$HD_k = \frac{b_k^2 (I_k^2 + Q_k^2)}{b_1^2 (I_1^2 + Q_1^2)}. \tag{2.8}$$

To quantify the effectiveness of the proposed multi-phase multi-path technique in the presence of mismatches, the improvement factor ζ_k is defined as the ratio between the kth harmonic distortion when no multi-phase multi-path scheme is applied (only one nonlinear block is used) to the kth order harmonic distortion of the proposed multi-phase system output with mismatches, i.e.,

$$\zeta_k = \frac{b_k^2 / b_1^2}{HD_k}. \tag{2.9}$$

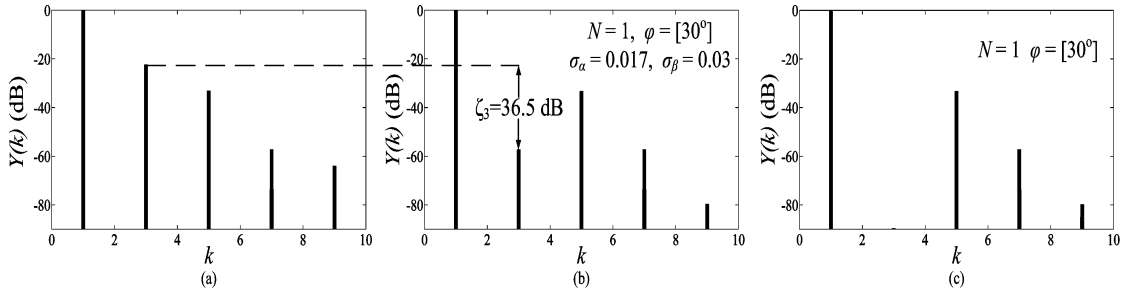

Figure 2.7: Output spectrum for a single-tone input. (a) Without distortion cancellation. (b) Proposed multi-phase scheme with gain and phase mismatches. (c) Proposed multi-phase scheme without mismatches

$$\begin{aligned}\zeta_3 &= \frac{b_3^2/b_1^2}{HD_3} = \frac{I_1^2+Q_1^2}{I_3^2+Q_3^2} \\ &= \frac{\left(1+\frac{\beta_1}{a_1}\right)^2+\left(1+\frac{\beta_2}{a_1}\right)^2+2\left(1+\frac{\beta_1}{a_1}\right)\left(1+\frac{\beta_2}{a_1}\right)\cos(2\varphi+\alpha_1-\alpha_2)}{\left(1+\frac{\beta_1}{a_1}\right)^2+\left(1+\frac{\beta_2}{a_1}\right)^2+2\left(1+\frac{\beta_1}{a_1}\right)\left(1+\frac{\beta_2}{a_1}\right)\cos[6\varphi+3(\alpha_1-\alpha_2)]} \quad (2.10)\end{aligned}$$

In our example ($N = 1$ and $\underline{\varphi} = [30^o]$), ζ_3 is given by (10) at the top of the next page. Simulations are done for the proposed system in Fig. 2.6. Fully differential operation is used to cancel the even harmonics. The standard deviation values of the phase and gain errors are chosen as in [9] ($\sigma_\alpha = 0.017$ and $\sigma_\beta = 0.03$). Fig. 2.7 shows the average system output spectrum over a thousand runs. Here, γ_3 is shown to be 36.5 dB, which matches well with the analytical value derived in (2.10). The improvement factor can be generalized for any N and $\underline{\varphi}$ chosen to cancel a group of harmonics as follows:

$$\zeta_k(N, \underline{\varphi}) = \frac{B}{C} \quad (2.11)$$

where B and C are given by (2.12) and (2.13) at the top of the next page, respectively.

All the previous analyses and results are valid for the intermodulation products

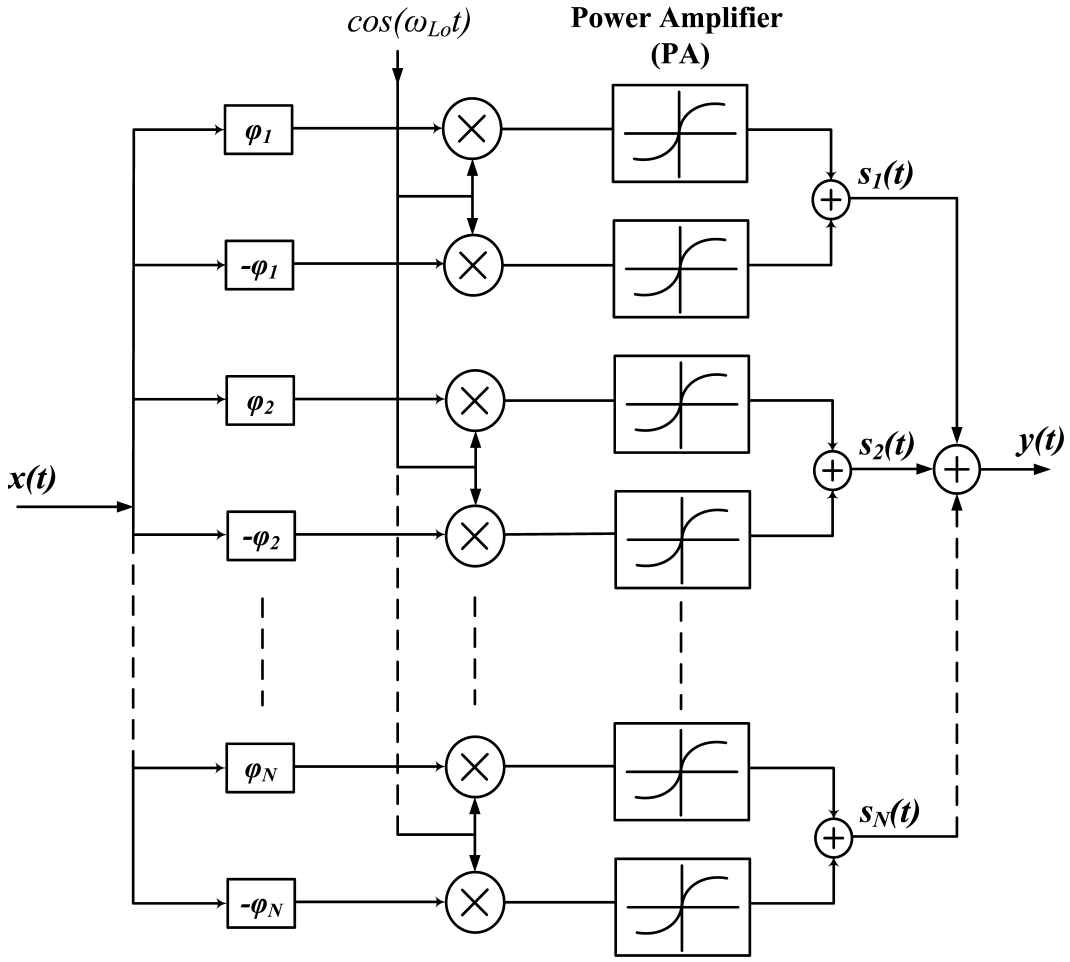

Figure 2.8: Conventional transmitter architecture using current-output multi-PAs with the proposed digitally generated multi-phase technique.

at $\omega = m\omega_1 + n\omega_2$ by replacing k with $m + n$.

2.5 Applications

One of the limitations of the poly-phase multi-path technique reported in [6] is that it can only be used with the current-output PU architecture. Applying the technique on conventional transmitter architectures where the mixer is followed by the PA will not cancel the nonlinearities. This is because the nonlinearity block (PA) needs to be inserted between the phase shifters and the mixers for the poly-phase technique to work, as in Fig. 2.2. On the other hand, the proposed multi-phase

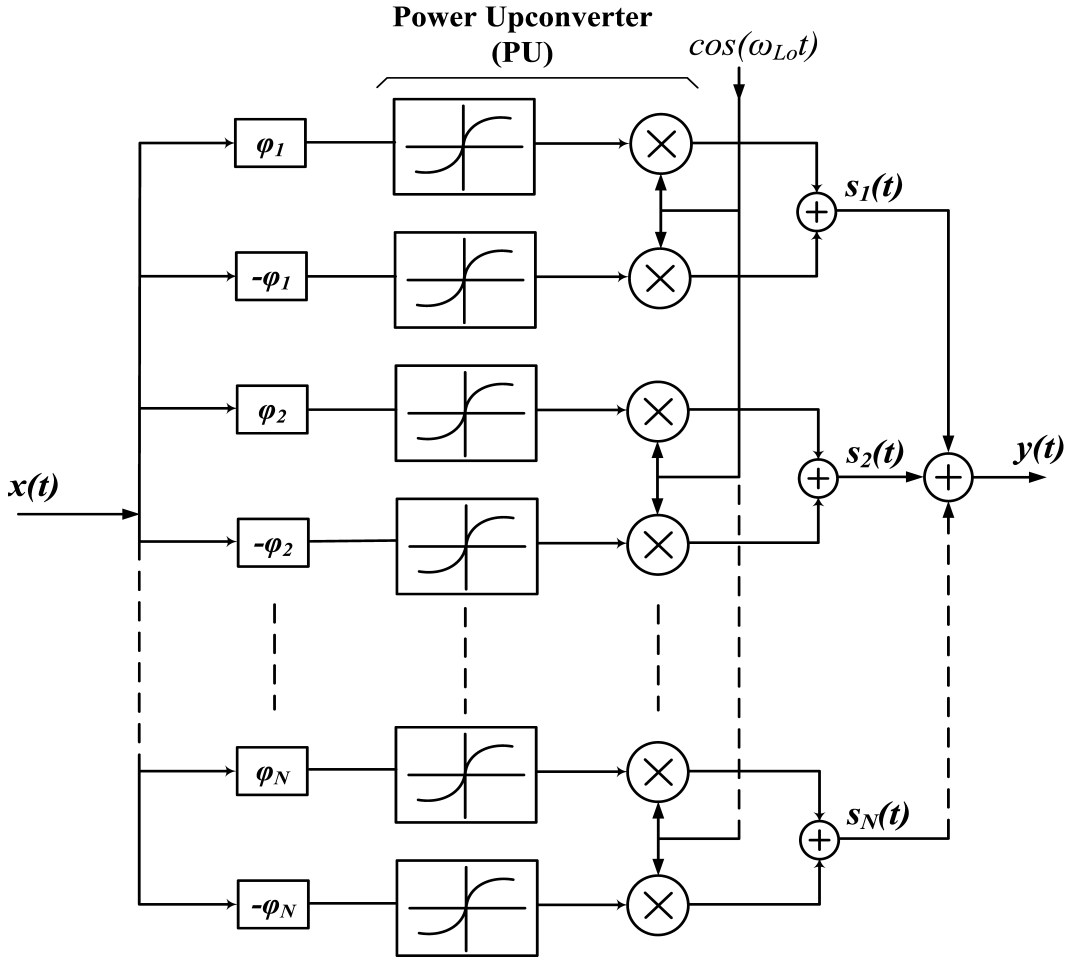

Figure 2.9: Current-output power upconverter model with the proposed digitally generated multi-phase multi-path technique.

technique can be applied to a current-output PA architecture that is split into multi-PAs, as shown in Figs. 2.8 and 2.9. However, it does not cancel the signal image and LO harmonics, which is an advantage in [6]. The proposed technique is capable of canceling the unwanted signals that fall in the LO sidebands, i.e., the signals at $\omega_{LO} + k\omega_B$, where ω_{LO} is the LO frequency and ω_B is the baseband signal frequency, are canceled for $k \neq 1$ depending on N and $\underline{\varphi}$. This is clear in the system shown in Fig. 2.10 that uses $\phi_1 = 30^o$ to cancel the 3rd order nonlinearity.

As an example, a multi-tone signal is applied to the systems shown in Fig. 2.8 and

$$
\begin{aligned}
B = \sum_{i=1}^{2N} \left(1+\frac{\beta_i}{a_1}\right)^2 + 2\sum_{i=1}^{N} \left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2i}}{a_1}\right)\cos(2\varphi_i + \alpha_{2i-1} - \alpha_{2i}) \\
+2\sum_{i=1}^{N-1}\sum_{j=i+1}^{N}\Bigg[\left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2j-1}}{a_1}\right)\cos(\varphi_i - \varphi_j + \alpha_{2i-1} - \alpha_{2j-1}) \\
+\left(1+\frac{\beta_{2i}}{a_1}\right)\left(1+\frac{\beta_{2j}}{a_1}\right)\cos(-\varphi_i + \varphi_j + \alpha_{2i} - \alpha_{2j}) \\
+\left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2j}}{a_1}\right)\cos(\varphi_i + \varphi_j + \alpha_{2i-1} - \alpha_{2j}) \\
+\left(1+\frac{\beta_{2i}}{a_1}\right)\left(1+\frac{\beta_{2j-1}}{a_1}\right)\cos(-\varphi_i - \varphi_j + \alpha_{2i} - \alpha_{2j-1})\Bigg]
\end{aligned}
\tag{2.12}
$$

$$
\begin{aligned}
C = \sum_{i=1}^{2N} \left(1+\frac{\beta_i}{a_1}\right)^2 + 2\sum_{i=1}^{N} \left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2i}}{a_1}\right)\cos[k(2\varphi_i + \alpha_{2i-1} - \alpha_{2i})] \\
+2\sum_{i=1}^{N-1}\sum_{j=i+1}^{N}\Bigg[\left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2j-1}}{a_1}\right)\cos[k(\varphi_i - \varphi_j + \alpha_{2i-1} - \alpha_{2j-1})] \\
+\left(1+\frac{\beta_{2i}}{a_1}\right)\left(1+\frac{\beta_{2j}}{a_1}\right)\cos[k(-\varphi_i + \varphi_j + \alpha_{2i} - \alpha_{2j})] \\
+\left(1+\frac{\beta_{2i-1}}{a_1}\right)\left(1+\frac{\beta_{2j}}{a_1}\right)\cos[k(\varphi_i + \varphi_j + \alpha_{2i-1} - \alpha_{2j})] \\
+\left(1+\frac{\beta_{2i}}{a_1}\right)\left(1+\frac{\beta_{2j-1}}{a_1}\right)\cos[k(-\varphi_i - \varphi_j + \alpha_{2i} - \alpha_{2j-1})]\Bigg]
\end{aligned}
\tag{2.13}
$$

Fig. 2.9. Saleh's nonlinear AM-AM conversion model [10], $w(t) = au(t)/[1 + bu^2(t)]$, is used, where $u(t)$ and $w(t)$ are the input and output of the nonlinear block, respectively ($a = 1.0536$ and $b = 0.0860$). The maximum input signal amplitude is adjusted to be at the 1-dB compression point of the model.

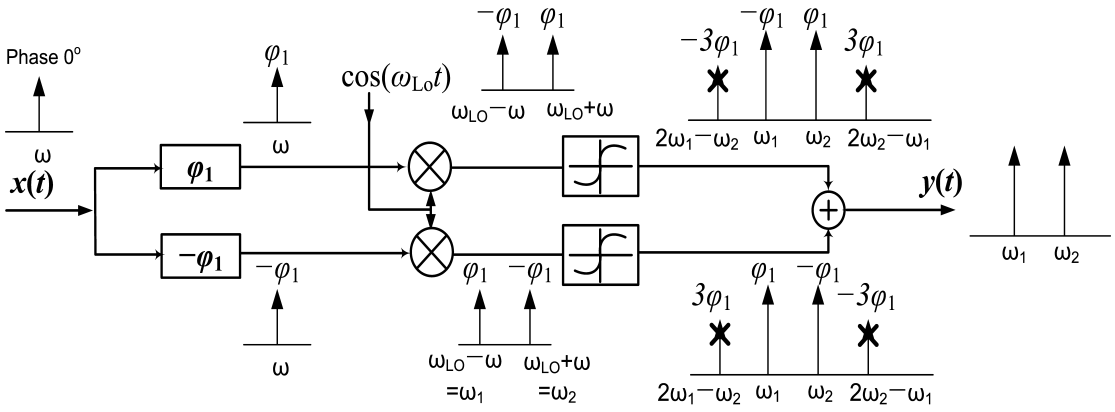

Figure 2.10: Cancellation of the 3rd order nonlinearity in the signal side bands

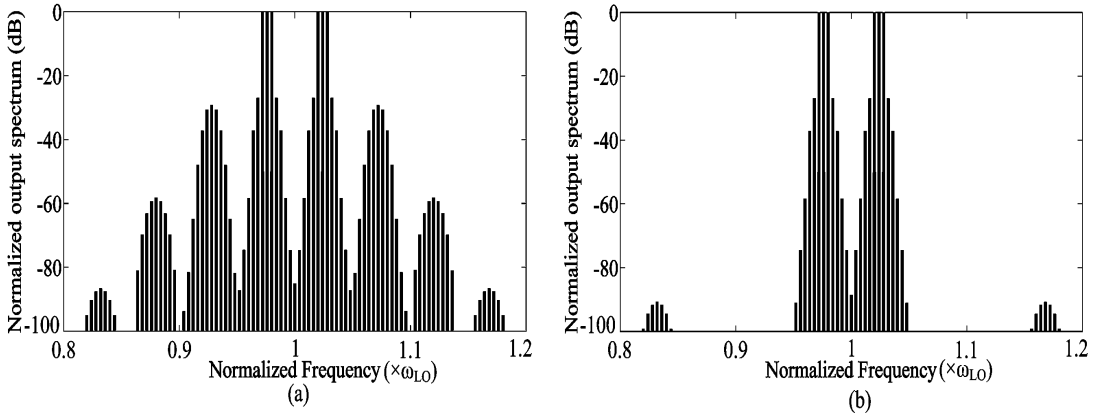

Figure 2.11: Comparison between the normalized output spectrum. (a) Without distortion cancellation. (b) With the proposed multi-phase technique.

Table 2.1: Comparison between the poly-phase technique in [6] and the proposed technique

Aspects of comparison	[6]	Proposed
Signal Harmonic Rejection	Yes	Yes
Need Analog Phase Shifters	Yes	No
Flexibility to different current-ouput PA Architecture	No	Yes
Fundamental Signal Alignmnet From Each Path	Yes	No
Third-Order Intermodulation Cancellation	No	No
LO Harmonic Cancellation	Yes	No
Signal Image Rejection	Yes	No

Fig. 2.11 shows a comparison between the output spectrum without distortion cancellation and when the proposed technique is applied for $N = 2$ and $\underline{\varphi} = [12^o, 48^o]$. It is clear that the proposed technique can reduce the distortion that appears on the signal sidebands. This reduction significantly relaxes the requirements on the high-quality band-pass filter used in the transmitter output to remove the far LO harmonics. Therefore, the tunability of such filters will be easier, making the proposed multi-phase technique attractive to multi-standard transmitter architectures. Table 2.1 summarizes the trade-offs between the poly-phase technique in [6] and the proposed multi-phase multi-path technique with digital phase shifters.

3. MULTIPLE FEEDBACK LOW POWER INDUCTORLESS WIDEBAND CMOS LNA*

A wideband low noise amplifier (LNA), which is a key block in the design of broadband receivers for multi-band wireless communication standards, is presented in this work. The LNA is a fully differential common-gate (CG) structure. It uses multiple feedback paths which add degrees of freedom in the choice of the LNA transconductance to reduce the noise figure (NF) and increase the amplification. The proposed LNA avoids the use of bulky inductors that leads to area and cost saving. A prototype is implemented in IBM 90 nm CMOS technology. It covers the frequency range of 100 MHz to 1.77 GHz. The core consumes 2.8 mW from a 2 V supply occupying an area of 0.03 mm^2. Measurements show a gain of 23 dB with a 3-dB bandwidth of 1.76 GHz. The minimum NF is 1.85 dB while the average NF is 2 dB across the whole band. The LNA achieves a return loss greater than 10 dB across the entire band and a third-order input intercept point IIP_3 of -2.85 dBm at the maximum gain frequency.

3.1 Introduction

Multi-band multi-standard concepts have gained considerable interest in modern wireless communications systems [11, 12, 13, 14]. To support a wide set of communication standards and to accommodate different applications in a single device, broadband transceivers are essential and inevitably in demand. A wideband RF receiver front-end architecture constructed by one single path [15] provides lower cost, area,

*Part of this chapter is reprinted with permission from "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback," by E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, and E. Sanchez-Sinencio , Dec. 2011. *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3154-3161.

and power consumption compared to the parallel-path architectures [16, 17]. Single path wideband concept can also accommodate emerging standards for cognitive radio applications, resulting in efficiency improvement in utilizing scarce spectrum resources.

One of the major challenges in wideband receivers is the design of a wide-band low-noise amplifier (LNA) that is shared among different standards. As the first block in the receiver chain, such an LNA should achieve good impedance matching, high and flat gain, and low noise figure (NF) across a wide frequency band. In addition, good linearity and low area and power consumption LNAs are required for high performance and low cost radios.

Recently, many wideband LNAs in CMOS technology have been reported, including distributed amplifiers [18] and resistive shunt feedback amplifiers [19, 20]. The former offers superior bandwidth in terms of high power consumption, large area, and deterioration of noise performance, which limits its widespread applications. The latter provides good broadband matching, noise, and gain, but it is hampered by greater power consumption, which makes them unattractive for low-power applications. Other implementations are inductor-based, such as L-degenerated broadband LNAs [21]. They have good performance in terms of NF and power consumption. However, the use of area consuming on-chip bulky inductors makes them unattractive for use in upcoming wireless low cost transceivers.

One of the wideband LNA topologies that has been widely investigated is the common-gate (CG) LNA. CG LNA is attractive compared to other topologies as it features wideband input impedance matching. Also, it offers good linearity, stability, and low power consumption. However, its main drawback is the relatively high NF [22]. This is due to the input matching condition, which restricts a certain value of transconductance to be used that leads to low gain and hence, high NF. Noise reduc-

tion techniques are used to overcome the disadvantage of the CG LNA configuration [22, 23, 24, 25, 26, 27]. Gain boosting scheme using negative feedback employing capacitive cross-coupling [22, 23], dual negative feedback [26], and positive-negative feedback [27] are applied to break the tradeoff between the input matching condition and the NF, which lead to simultaneous reduction in noise and power dissipation. However, reducing the noise figure below 2 dB is still challenging in CG LNAs.

In this work, a wideband differential CG LNA employing multiple feedback is proposed. It uses three feedbacks to add more flexibility in determining the g_m of the impedance matching device. This breaks the lower bound of the noise performance and leads to reduction in the noise figure and increase in the gain. To the best of the authors' knowledge, the proposed LNA achieves the lowest NF and highest gain among CG LNAs reported in the literature while consuming low power. It also avoids the use of bulky inductors resulting in considerable area and cost savings. The presented LNA covers frequency bands for Digital Video Broadcasting (DVB) at 450-850 MHz, Global System for Mobile communications (GSM) at 900 MHz, and Global Positioning System (GPS) at 1.2 and 1.5 GHz, providing a practical solution for multi-standard applications. The Chapter is organized as follows. In Section 2, existing noise reduction techniques for CG LNA using negative and positive feedbacks are discussed. Section 3 covers the proposed CG LNA, showing detailed analysis for the major LNA parameters. Finally, in Section 4, circuit implementation is presented along with simulation results and measurements.

3.2 Background

Fig. 3.1 (a) shows the differential configuration of the conventional CGLNA. In this circuit, the differential voltage gain, $A_v = \frac{Vop-Von}{Vip-Vin}$, and the differential input

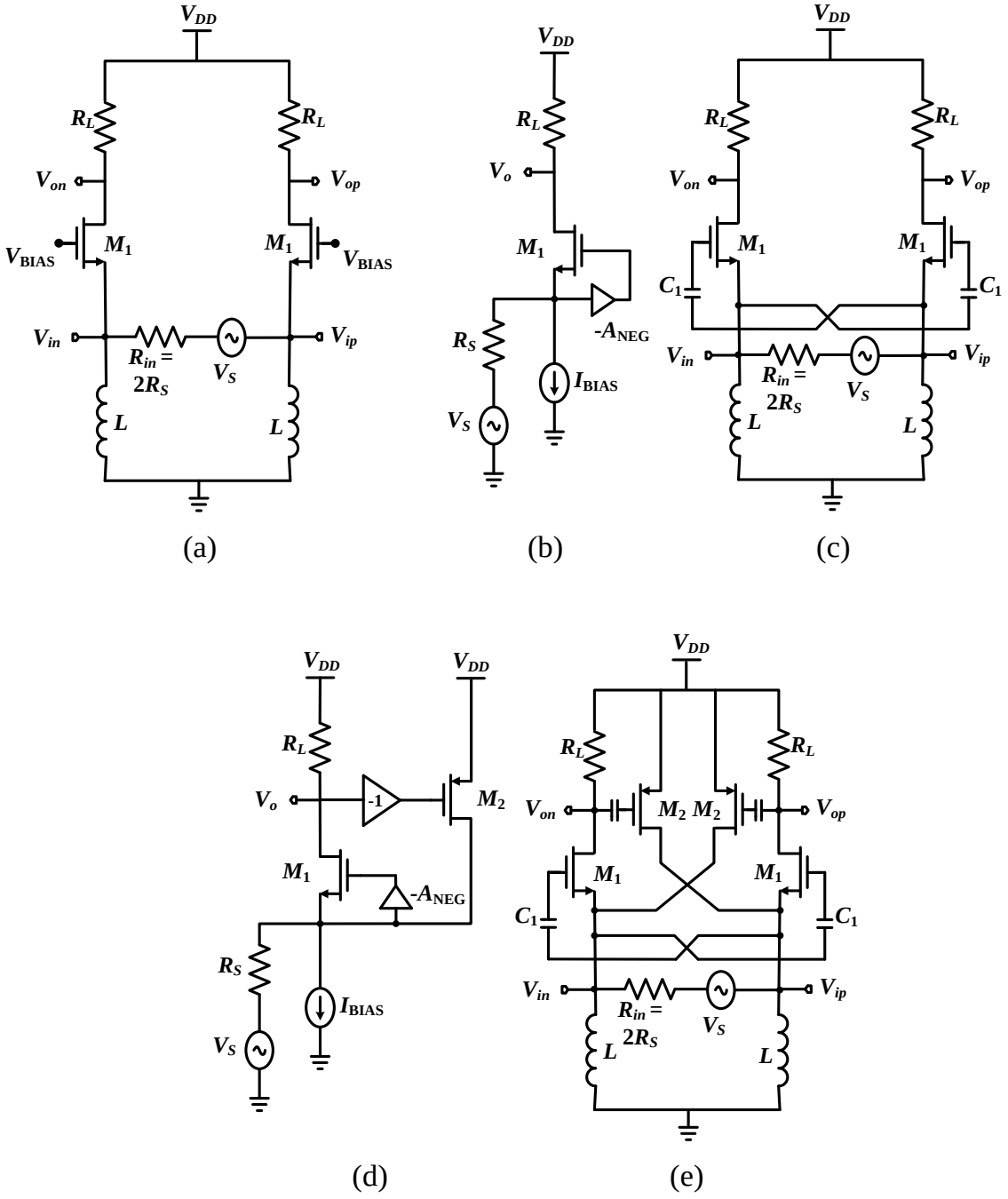

Figure 3.1: Conventional differential CGLNA and low noise feedback techniques

impedance, R_{in}, are given by

$$A_v = g_{m1}R_L. \tag{3.1}$$

$$R_{in} = 2/g_{m1}. \tag{3.2}$$

where g_{m1} is the transconductance of transistor M_1. Assuming perfect matching condition ($R_{in} = 2R_S = 100\Omega$), the noise factor, F, is given by

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}. \tag{3.3}$$

where γ is the excess channel thermal noise coefficient, and α is the ratio between g_{m1} and the zero-bias drain conductance, g_{do1}. The last term in (3.3) represents the noise contribution due to the load, R_L. Due to the power matching constraint, the CGLNA suffers a relatively high noise figure, NF. Noise reduction techniques are used to improve the NF of the CGLNA. In the following subsections, these techniques are briefly presented.

3.2.1 Negative feedback CGLNA employing capacitive cross-coupling

The idea to improve the noise performance of the CGLNA is based on introducing a decoupling mechanism between the input power matching condition and the NF. This is achieved by improving the effective transconductance and enhancing the gain. The single-ended model of the transconductance boosting structure is shown in Fig. 3.1 (b). The structure uses an inverting gain A_{NEG} that is inserted in the feedback between the gate and source terminals of M_1. The effective g_{m1} is boosted to $g_{m1}(1 + A_{NEG})$ with input impedance matching of $1/\left[g_{m1}(1 + A_{NEG})\right] = R_S =$

50Ω. This means smaller bias current, less channel noise from M_1, and consequently smaller noise contribution and power consumption. The noise factor, F, is then given by

$$F = 1 + \frac{\gamma}{(1 + A_{NEG})\alpha} + \frac{4R_S}{R_L}. \tag{3.4}$$

One possible way to implement the inverting gain, A_{NEG}, is to use cross-coupling capacitors, C_1 as shown in the differential CGLNA topology in Fig. 3.1 (c) [22]. A_{NEG} is approximately given by the capacitors ratio, $(C_1 - C_{gs1})/(C_1 + C_{gs1})$, where C_{gs1} is the gate-source capacitance of M_1. For $C_1 >> C_{gs1}$, A_{NEG} is almost unity, which reduces A_v, R_{in}, and F to the following

$$A_v = 2g_{m1}R_L. \tag{3.5}$$

$$R_{in} = 2R_S = 1/g_{m1}. \tag{3.6}$$

$$F = 1 + \frac{\gamma}{2\alpha} + \frac{4R_S}{R_L}. \tag{3.7}$$

Comparing to the conventional CGLNA, F is reduced and the effective transconductance is increased with reduction in power consumption.

3.2.2 Positive-negative feedback CGLNA

The negative feedback CGLNA reduces the noise figure by the use of capacitive divider. Meanwhile, its transconductance, g_{m1} is restricted to 10 mS to satisfy the input power matching condition. Thus, this solution suffers from low gain. To alleviate the restriction of low g_{m1}, a positive feedback along with the nega-

tive feedback is used in [27]. To increase the gain, the idea is to create a positive current feedback path through M_2 as shown in the single-ended model in Fig. 3.1 (d). This feedback path increases the input impedance of the LNA to be equal to $1/\left[g_{m1}(1+A_{NEG})(1-A_{POS})\right]$, where $A_{POS} = g_{m2}R_L$ is the positive feedback gain which varies from 0 to 1 for stability. In this way, g_{m1} can be chosen arbitrarily to values higher than 10 mS without restricting the input matching condition. For example, if A_{POS} is designed to be 0.5 and $A_{NEG} = 1$, then $g_{m1} = 20$ mS for the 50Ω input matching to be satisfied. Thus, the gain increases.

The fully differential positive-negative CGLNA in [27] is shown in Fig. 3.1 (e). Since the positive feedback loop provides degree of freedom in a way that the impedance matching does not fix the bias current, the current will be a design variable to improve the noise performance. Considering the thermal channel noise, under input matching condition, the noise factor is given by:

$$F = 1 + \frac{(1-A_{POS})\gamma}{(1+A_{NEG})\alpha} + g_{m2}R_S\frac{\gamma}{\alpha} + \frac{R_S}{R_L}\left(2-A_{POS}\right)^2. \tag{3.8}$$

For $A_{NEG} = 1$ and $A_{POS} = 0.5$, A_v, R_{in}, and F are reduced to the following:

$$A_v = 2g_{m1}R_L. \tag{3.9}$$

$$R_{in} = 2R_S = 2/g_{m1}. \tag{3.10}$$

$$F = 1 + \frac{\gamma}{4\alpha} + g_{m2}R_S\frac{\gamma}{\alpha} + \frac{9R_S}{4R_L}. \tag{3.11}$$

The third term in (3.11) represents the noise due to M_2. The value of g_{m2} is chosen

to be small which translates to small noise contribution. Therefore, the positive-negative feedback CGLNA can achieve a lower NF than the negative feedback and conventional CGLNAs with higher gain. However, power consumption increases compared to negative feedback CGLNA.

3.3 Proposed CGLNA

The idea of the proposed CGLNA is based on adding more degree of freedom on the impedance matching condition of the positive-negative feedback CGLNA in Fig. 3.1 (e). In this way, there will be more flexibility in choosing the optimum value of the LNA transconductance that achieves minimum noise figure. Fig. 3.2 shows the proposed CGLNA. The biasing inductors are replaced by current sources (M_3s), that are capacitively cross-coupled using C_2 ($C_2 >> C_{gs3}$) [23]. As shown in the single-ended model in Fig. 3.3, the capacitively coupled transistor, M_3, creates another positive current feedback path beside the one created by M_2. Therefore, the output current of the LNA becomes the sum of the current provided by the source and those injected through M_2 and M_3, making the current gain larger than unity.

3.3.1 Input impedance

The two current (shunt) positive feedback paths have the effect of increasing the CGLNA input impedance. Referring to Fig. 3.2, the input impedance is given by:

$$\begin{aligned} R_{in} &= \frac{2}{g_{m1}\left(1+A_{NEG}\right)\left(1-A_{POS}-B_{POS}\right)} \\ &= \frac{2}{2g_{m1}\left(1-A_{POS}-B_{POS}\right)} \end{aligned} \tag{3.12}$$

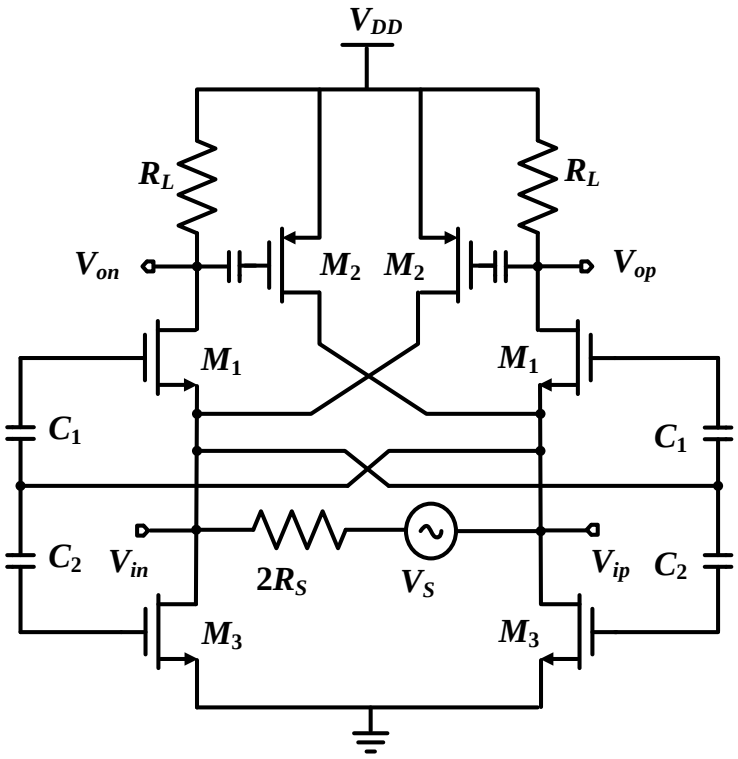

Figure 3.2: Schematic of the proposed CGLNA (biasing circuit not shown).

where $A_{POS} = g_{m2}R_L$, $B_{POS} = g_{m3}/2g_{m1}$, and $A_{Neg} = 1$. Thus, the input matching condition is given by

$$2g_{m1}R_S\,(1 - A_{POS} - B_{POS}) = 1. \tag{3.13}$$

From (3.13), two degrees of freedom, A_{POS} and B_{POS}, exist that allow arbitrary choice of g_{m1} achieving high gain and optimum minimum noise figure, as will be seen in the noise analysis.

3.3.2 Stability

The condition of stability is based on the approach of the return ratio, RR [25]. This approach is used to study the amplifier stability in the presence of multiple feedback loops and to model bidirectional paths between input and output. For the

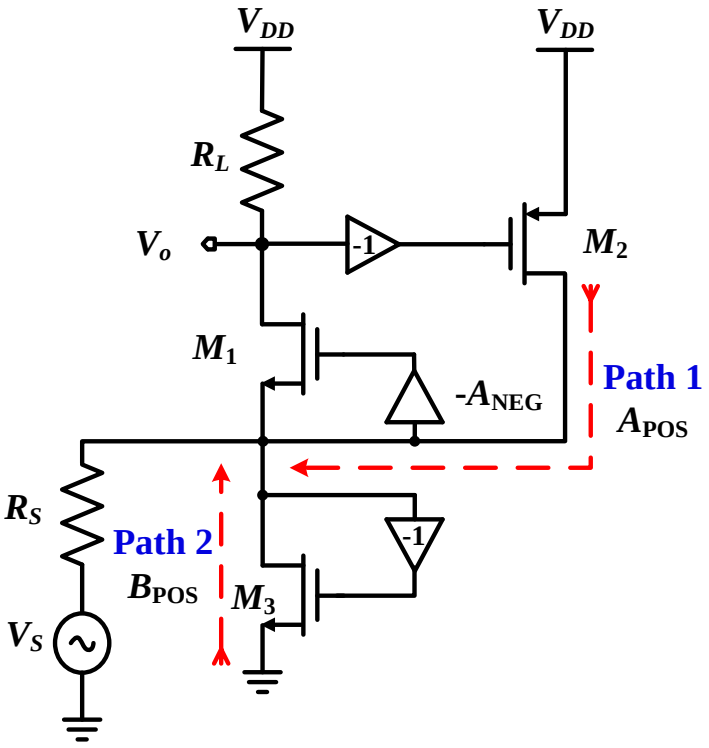

Figure 3.3: Simplified single-ended CGLNA model.

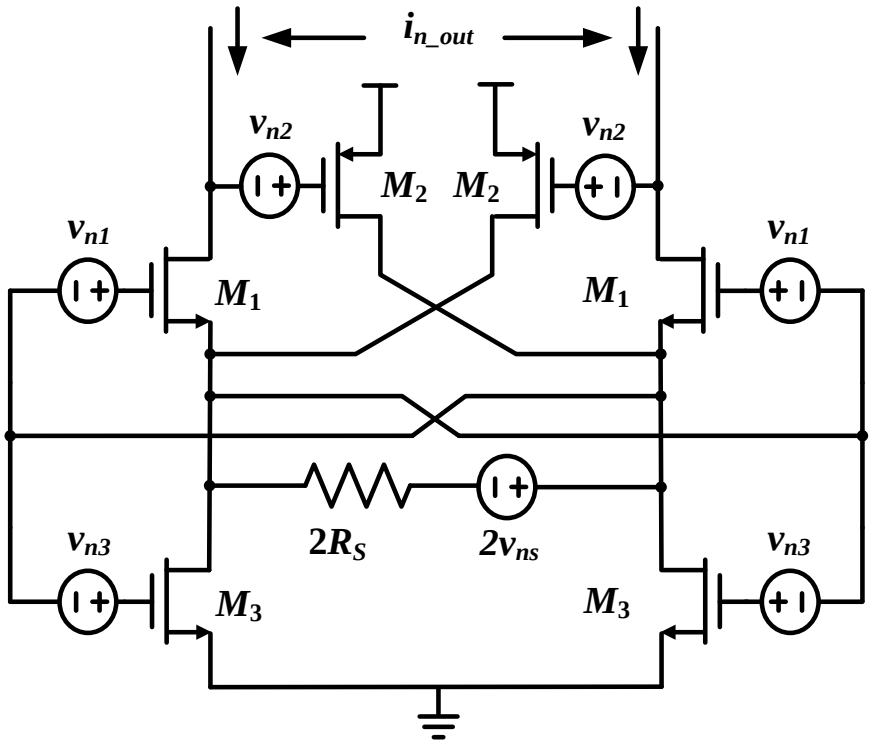

Figure 3.4: Schematic of the proposed CGLNA showing noise sources.

proposed CGLNA, the RR has the following expression:

$$RR = \frac{-2g_{m1}R_S}{1+2g_{m1}R_S}(A_{POS} + B_{POS}). \tag{3.14}$$

The proposed CGLNA is stable if $-1 < RR < 0$ and this can be guaranteed by setting $(A_{POS} + B_{POS}) < 1$ with a safe margin to take into account any process variation.

3.3.3 Noise analysis

Fig. 3.4 shows a simplified model for the noise sources of the proposed CGLNA. The circuit noise performance is analyzed and its NF is computed assuming that the dominant noise sources are due to the thermal noise of the transistors and the load. The coupling capacitors, C_1 and C_2, in Fig. 3.2 are replaced with short circuits

since they are much larger than the gate capacitance of the input transistors, M_1, and M_3, respectively. In this case, the noise due to the source resistance, v_{ns}, the thermal noise due to M_2, v_{n2}, and that due to M_3, v_{n3}, as shown in Fig. 3.2, create two equal and opposite noise currents in the output branches with magnitudes of $g_{m1}v_{ns}/2$, $g_{m1}g_{m2}R_sv_{n2}/2$, and $g_{m1}g_{m3}R_sv_{n3}/2$, respectively. While the thermal noise due to M_1, v_{n1}, creates two unequal output noise currents with differential value of $g_{m1}\left(g_{m1}R_s-1\right)v_{n1}$. The output differential current due to each noise source is given by:

$$\begin{aligned}
\overline{i_{ns-out}^2} &= 4kTR_sg_{m1}^2\Delta f. \\
\overline{i_{n1-out}^2} &= 4kT\frac{\gamma_1}{\alpha}g_{m1}\left(g_{m1}R_s-1\right)^2\Delta f. \\
\overline{i_{n2-out}^2} &= 4kT\frac{\gamma_2}{\alpha}g_{m2}\left(g_{m1}R_s\right)^2\Delta f. \\
\overline{i_{n3-out}^2} &= 4kT\frac{\gamma_3}{\alpha}g_{m3}\left(g_{m1}R_s\right)^2\Delta f. \qquad (3.15)
\end{aligned}$$

Assuming $\gamma_1=\gamma_2=\gamma_3=\gamma$, the noise factor, F, is given by:

$$\begin{aligned}
F=\frac{\overline{i_{ntotal-out}^2}}{\overline{i_{ns-out}^2}} &= 1+\frac{\gamma}{\alpha}\frac{\left(g_{m1}R_s-1\right)^2}{g_{m1}R_s}+\frac{\gamma}{\alpha}g_{m2}R_s \\
&\quad +\frac{\gamma}{\alpha}g_{m3}R_s+\frac{R_s}{R_L}\left(1+\frac{1}{2g_{m1}R_s}\right)^2. \qquad (3.16)
\end{aligned}$$

Note that the last term accounts for the noise contribution due to the load, R_L. Increasing the value of R_L relative to R_s reduces the load noise contribution to the overall noise figure. Under the input power matching condition, F reduces to

$$\begin{aligned}
F &= 1+\frac{\gamma}{\alpha}\frac{\left(\eta-1\right)^2}{\eta}+2\frac{\gamma}{\alpha}\left(1-A_{POS}\right)\eta \\
&\quad -\frac{\gamma}{\alpha}\left(1-\frac{R_s}{R_L}A_{POS}\right)+\frac{R_s}{R_L}\left(1+\frac{1}{2\eta}\right)^2. \qquad (3.17)
\end{aligned}$$

Table 3.1: Comparison between different CGLNA configurations together with the proposed one

	Convent. CGLNA	Negative feedback CGLNA	Positive-Negative feedback CGLNA	This work
Differential input impedance, R_{in}	$\frac{2}{g_{m1}}$	$\frac{1}{g_{m1}}$	$\frac{1}{g_{m1}(1-A_{POS})}$	$\frac{1}{g_{m1}(1-A_{POS})-g_{m3}/2}$
g_{m1} for the input matching	$\frac{1}{R_S}$	$\frac{1}{2R_S}$	$\frac{1}{2R_S(1-A_{POS})}$	$\frac{1+g_{m3}R_S}{2R_S(1-A_{POS})}$
A_v at the input matching	$\frac{R_L}{R_S}$	$\frac{R_L}{R_S}$	$\frac{R_L}{R_S(1-A_{POS})}$	$\frac{R_L(1+g_{m3}R_S)}{R_S(1-A_{POS})}$
NF at the input matching	$1+\frac{\gamma}{\alpha}+\frac{4R_S}{R_L}$	$1+\frac{\gamma}{2\alpha}+\frac{4R_S}{R_L}$	$1+\left(0.25+\frac{0.5R_s}{R_L}\right)\frac{\gamma}{\alpha}+\frac{9R_S}{4R_L}$	$1+\left(0.06+\frac{0.35R_s}{R_L}\right)\frac{\gamma}{\alpha}+\frac{3.11R_s}{R_L}$
Percentage of NF reduction relative to the conventional CGLNA	–	28%	44.4%	53.4%

where $\eta = g_{m1}R_s$ and A_{POS} are the optimization parameters used to determine the minimum noise factor for the proposed CGLNA. To find the optimum value of η, $\frac{dF}{d\eta} = 0$. As a result, for large R_L,

$$\eta_{opt} = \frac{1}{\sqrt{3-2A_{POS}}}. \tag{3.18}$$

For small values of A_{POS}, (3.18) becomes:

$$\eta_{opt} = \frac{1}{\sqrt{3}}\left(1+\frac{A_{POS}}{3}\right). \tag{3.19}$$

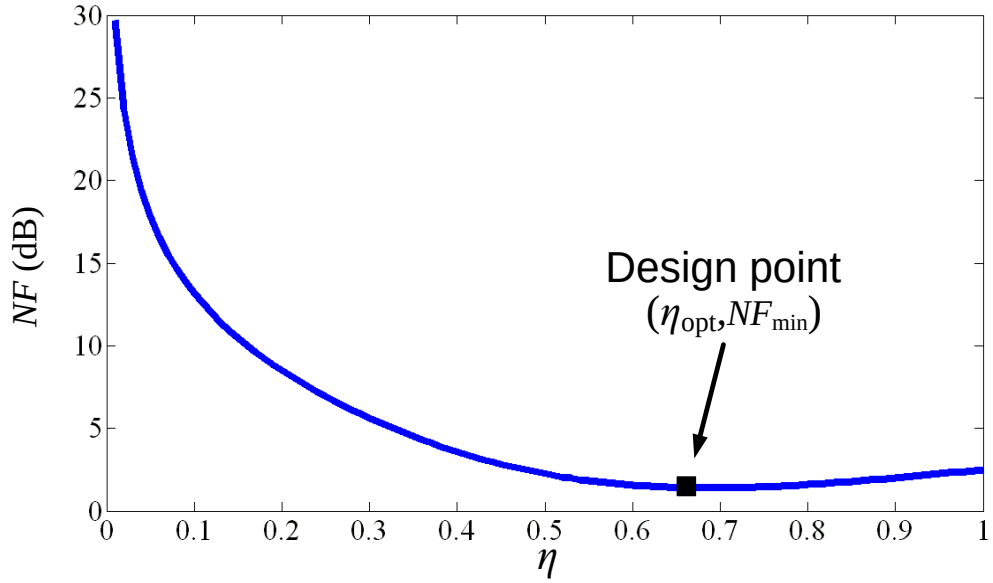

Figure 3.5: Calculated noise figure versus the optimization parameter η for the proposed CGLNA at $A_{POS} = 0.35$, $R_L = 650\Omega$, $\gamma = (4/3)$, and $\alpha = 0.8$

Accordingly, the minimum noise factor, F_{min}, is given by:

$$F_{min} = 1 + 0.464\frac{\gamma}{\alpha} - \frac{\gamma}{\alpha}\left(1.155 - \frac{R_s}{R_L}\right)A_{POS} + \frac{R_s}{R_L}\left(1.866 - 0.2886A_{POS}\right)^2. \tag{3.20}$$

The negative sign for the third term in (3.20) plays an important role in reducing the proposed CGLNA noise factor. We can say that the combination of multiple feedbacks contributes to noise cancellation. As an example, for $A_{POS} = 0.35$ to ensure stability, F_{min} is given by:

$$F_{min} = 1 + \left(0.06 + \frac{0.35R_s}{R_L}\right)\frac{\gamma}{\alpha} + \frac{3.11R_s}{R_L}. \tag{3.21}$$

Graphically, Fig. 3.5 shows the noise figure versus sweep of the optimization parameter η. As depicted, there is an optimum value η_{opt} to minimize the NF

which is confirmed by with the above analysis. In this design example, a minimum noise figure, NF_{min}, of 1.4 dB can be achieved for typical values of short-channel devices. Compared to the conventional CGLNA and other reported feedback based CGLNA topologies, the proposed CGLNA achieves the lowest NF with advantages of removing the bulky inductors and arbitrary choice of g_{m1} without restricting the input matching condition. Table 3.1 summarizes the main properties of the different CGLNA configurations together with the proposed one. The last line is showing the percentage of reduction in NF for each feedback method relative to the conventional CGLNA at at $R_L = 650\Omega$, $\gamma = (4/3)$, and $\alpha = 0.8$. It can be shown that the proposed CGLNA can achieve the highest reduction among other toplogies.

3.4 Circuit design and measurement results

The proposed LNA with a voltage gain of 23 dB, 3-dB bandwidth of 1.76 GHz and a minimum noise figure of 1.85 dB over the band is implemented. A highly linear voltage buffer is used at the LNA output to drive the 50Ω load of the measuring equipment. Coupling capacitors are used between the LNA and the buffer to provide the buffer with separate DC bias. The gain and noise figure of the buffer are predetermined to de-embed their effect from the overall response to get the LNA response. The total schematic of the LNA with the buffer is shown in Fig. 3.6. Table 3.2 shows the transistor aspect ratios for the proposed LNA and buffer. In the layout implementation, the transistors are laid out with maximum number of fingers and close to minimum width per finger to minimize the effective series gate resistance, to reduce the signal loss and improve the noise figure specially for the input transistor, M_1. To reduce the effect of the flicker noise, the lengths of the transistors are increased. The coupling capacitors, employed in the design, are implemented using MIMCAP device supported by the IBM 90nm CMOS process which has a density

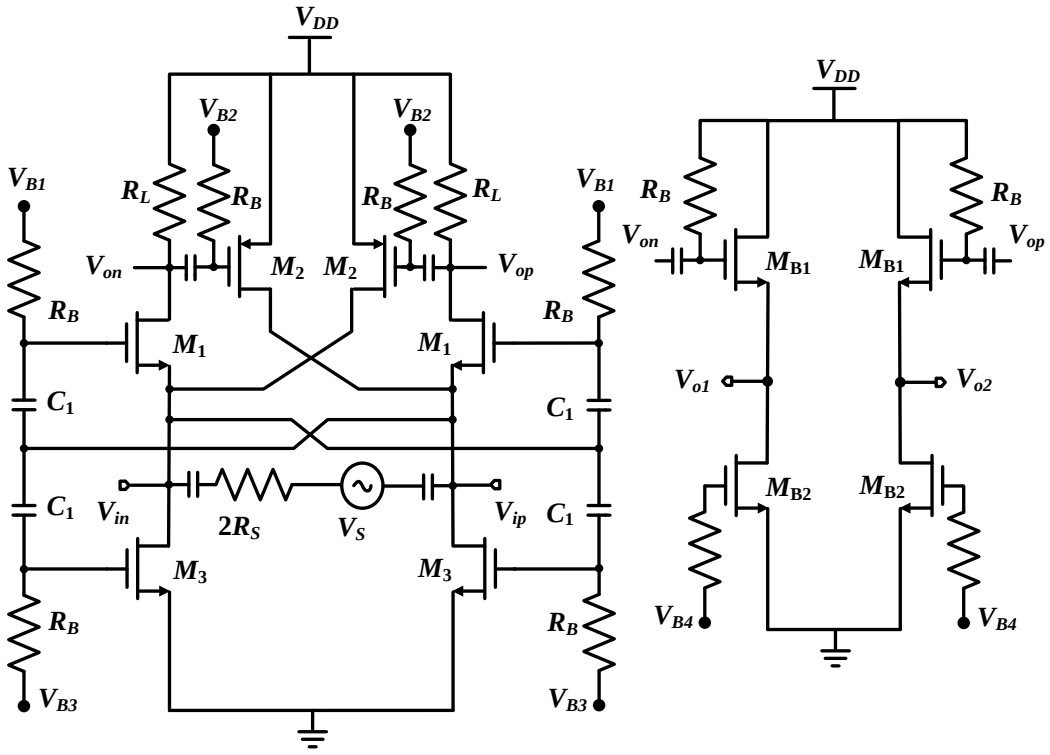

Figure 3.6: Schematic of the entire LNA with the output buffer

Table 3.2: Transistor aspect ratios for the LNA and buffer

$(\frac{W}{L})_{M_1}$	$(\frac{W}{L})_{M_2}$	$(\frac{W}{L})_{M_3}$	$(\frac{W}{L})_{M_{B1}}$	$(\frac{W}{L})_{M_{B2}}$
$\frac{75\ \mu\text{m}}{0.175\ \mu\text{m}}$	$\frac{1.2\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{6\ \mu\text{m}}{0.3\ \mu\text{m}}$	$\frac{35\ \mu\text{m}}{0.175\ \mu\text{m}}$	$\frac{50\ \mu\text{m}}{0.175\ \mu\text{m}}$

of 5.8 fF/μm^2 . The biasing resistors are implemented using poly resistors. Fig. 3.7 shows a micrograph of the fabricated CGLNA/buffer with a chip size of 1mm×1mm (including the pads). The core LNA area is 0.03 mm^2

The core LNA consumes 1.4 mA from a 2 V supply while the buffer consumes 10 mA. The LNA is encapsulated in a micro leadframe (QFN) open package, where the DC biases and input RF signal are applied/monitored using an FR-4 printed circuit board (PCB). The output signal is monitored using a G-S-G-S-G differential probe. This measurement setup is used to evaluate the performance of the LNA

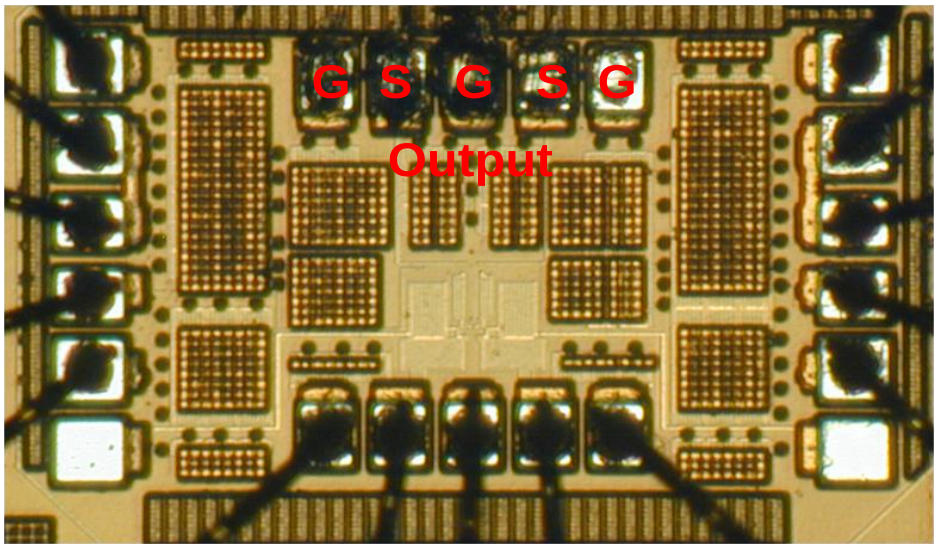

Figure 3.7: Die photo of the proposed LNA.

including the PCB traces and packaging effect. Baluns are used at input and the output for single-ended to differential signal conversion. Figs. 3.8, 3.9, and 3.10 show the post layout simulated and the measured input reflection coefficient, S_{11}, voltage gain, and noise figure, NF, respectively. They are plotted versus RF input frequency up to 2 GHz after de-embedding the effect of the output buffer. The measured S_{11} is lower than -10 dB from 100 MHz up to 1.8 GHz (Fig. 3.8). The voltage gain is measured to be 23 dB in the passband with an upper 3-dB frequency of 1.77 GHz (Fig. 3.9). The measured minimum NF is 1.85 dB at 0.7 GHz with degraded performance at the lower and higher frequencies because of the flicker noise and LNA bandwidth limitation respectively (Fig. 3.10). Across the entire 3-dB bandwidth, the average measured NF is 2 dB. These measurements show that the proposed LNA achieves an almost constant noise figure from 100 MHz up to its upper cut-off frequency. This property does not exist in many reported broadband LNAs, which achieve a minimum noise figure at a specific frequency and have a much higher noise

figure across the entire frequency range. The input-referred intercept point, IIP_3, for the proposed wideband CGLNA is measured using a two-tone test for a 300 MHz operating frequency. The two tones are applied with the same amplitude and a frequency offset of 10 MHz. An IIP_3 value of -2.85 dBm is obtained as shown in Fig. 3.11. As a measure of the stability of the proposed CGLNA, Fig. 3.12 shows a plot for the stability factor, K, that is calculated based on the S-parameters (LNA+buffer) through the following expression:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2\,|S_{12}|\,|S_{21}|} \tag{3.22}$$

Table 3.3 compares the performance of the proposed CGLNA with that of the state-of-the-art wideband LNAs around the same frequency range. The power consumption reported is of the core LNA only. As shown in the table, the proposed broadband LNA with multiple feedback provides the minimum noise figure among CG topologies. It also has low power consumption and high gain when compared to previously reported wideband LNAs.

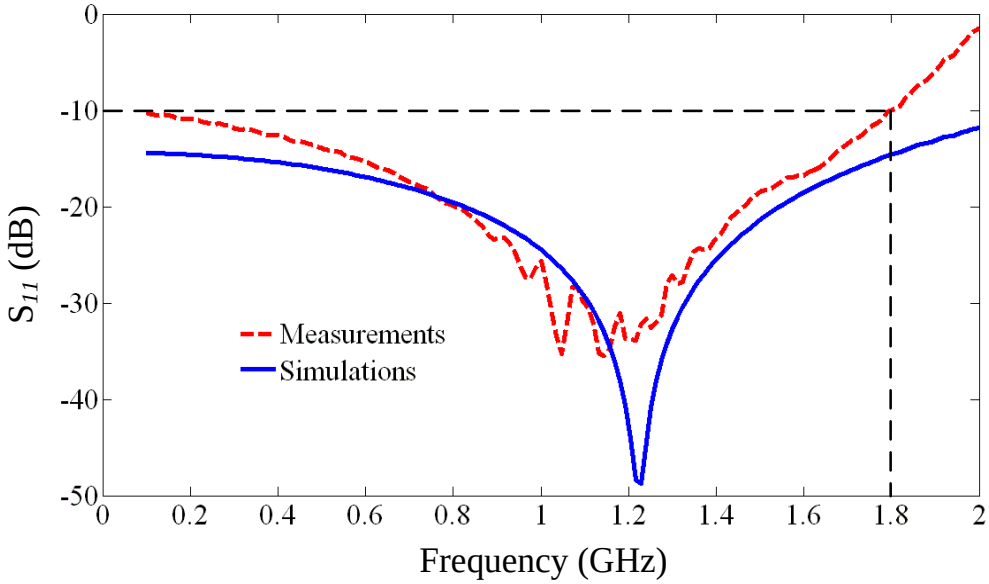

Figure 3.8: Measured and simulated input matching versus RF input signal frequency

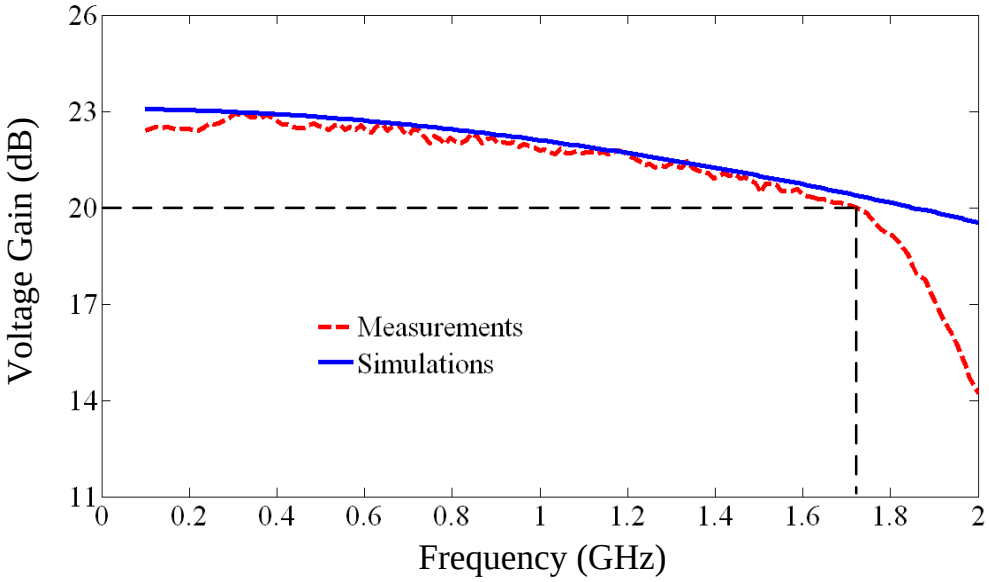

Figure 3.9: Measured and simulated voltage gain versus RF input signal frequency

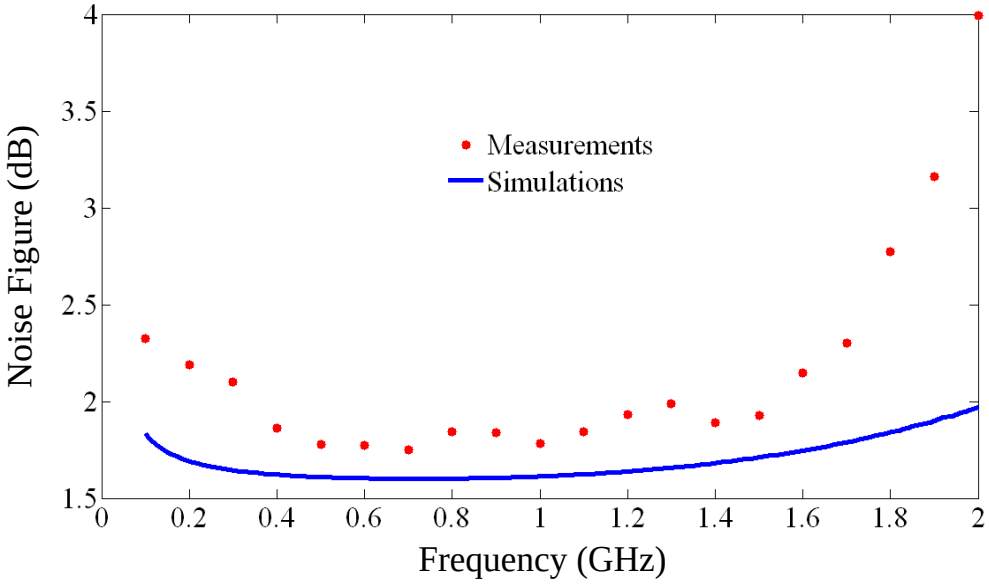

Figure 3.10: Measured and simulated noise figure versus RF input signal frequency

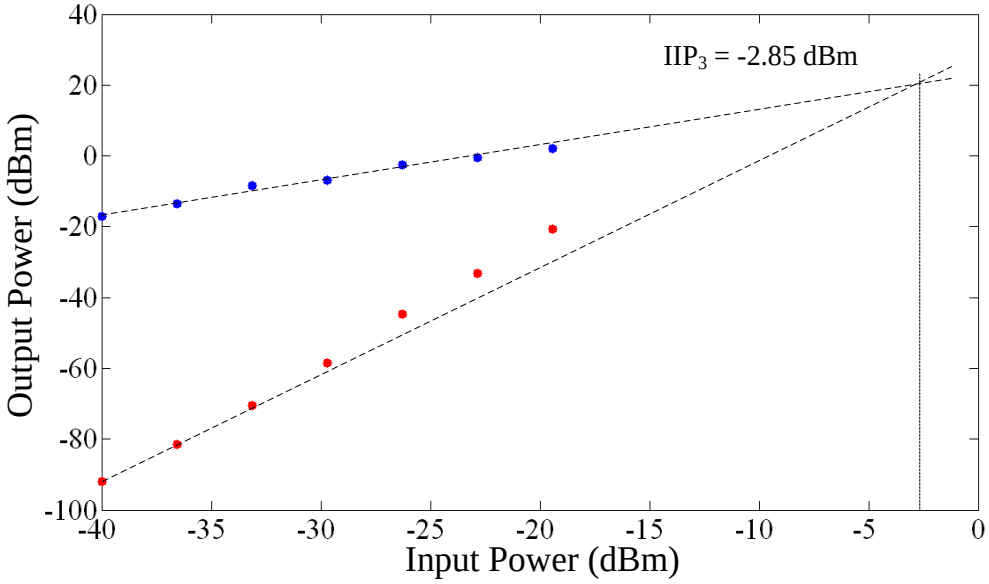

Figure 3.11: Measured IIP_3 for the proposed CGLNA

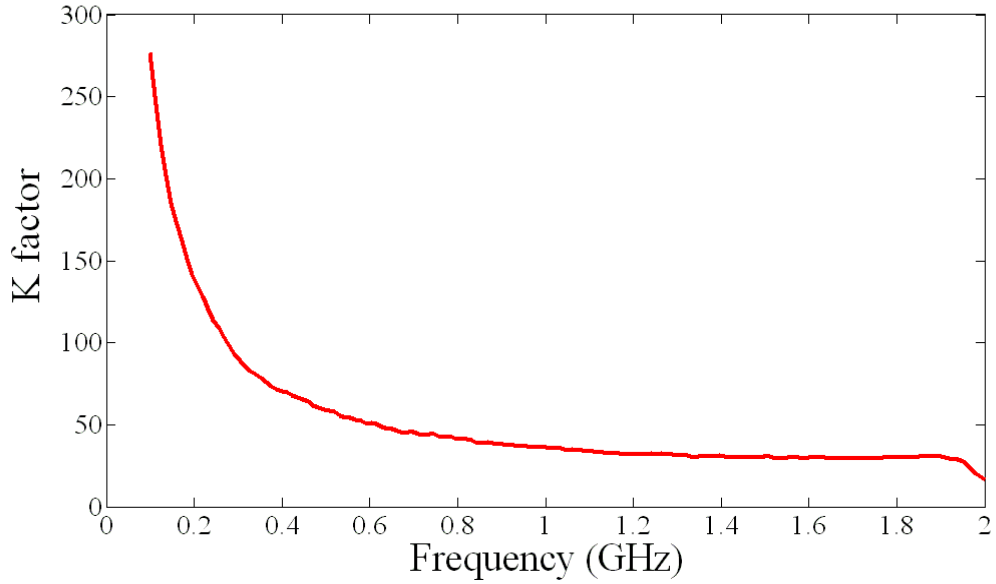

Figure 3.12: Stability factor for the proposed CGLNA

Table 3.3: Performance summary of the proposed broadband LNA and comparison with the existing work

Ref.	Gain (dB)	Freq. Range (GHz)	NF_{min} (dB)	NF_{max} (dB)	IIP_3 (dBm)	P_{DC} (mW)	Area (mm^2)	Tech CMOS
[26]	16.9	1.05-3.05	2.57	3.2 [a]	-0.7	12.6	0.073 [c]	0.18 μm
[27]	21	0.3-0.92	2	3.5 [a]	-3.2	3.6	0.33	0.18 μm
[28]	20.5 [b]	0.02-1.18	3 [a]	3.5 [a]	2.7	32.4	0.12 [c]	0.18 μm
[29]	13.7	0.002-1.6	1.9 [a]	2.4	0	35	0.075 [c]	0.25 μm
[30]	16	0.4-1	3.5	5.3	-17	16.8	0.07 [c]	90 nm
[31]	21	0.002-2.3	1.4	1.7	-1.5	18	0.06 [c]	90 nm
[32]	12.5 [b]	0.8-2.1	2.5 [a]	2.7 [a]	16	17.4	0.1	0.13 μm
[33]	18	0.1-5	2.5 [a]	4	-8	20	N.A.	0.13 μm
[34]	19	0.2-3.8	2.8	3.4	-4.2	5.7	0.025 [c]	0.13 μm
This work	23	0.1-1.77	1.85	2.35	-2.85	2.8	0.03 [c]	90 nm

[a] Estimated from data provided in the corresponding papers.
[b] Power Gain.
[c] Active area size.

4. LOW POWER INDUCTORLESS WIDEBAND COMMON GATE LNA WITH ENHANCED LINEARITY

A low power linear wideband low noise amplifier (LNA) is presented in this work. The LNA is a fully differential common-gate (CG) structure. It uses cross-coupling capacitors to reduce the noise figure compared to the conventional CG LNA. Complementary Derivative Superposition (DS) method is used employing an NMOS/PMOS pair to improve the linearity. The proposed LNA avoids the use of bulky inductors that leads to area and cost saving. A prototype is implemented in IBM 90 nm CMOS technology. It covers the frequency range of 100 MHz to 1.6 GHz. A 6 dBm third-order input intercept point IIP_3 is measured at the maximum gain frequency. The core consumes low power of 1.55 mW using a 1.8 V supply occupying an area of 0.03 mm^2. Measurements show a voltage gain of 15.5 dB with a 3-dB bandwidth of 1.6 GHz. The LNA has a minimum NF of 3 dB across the whole band while achieving an input return loss greater than 12 dB.

4.1 Introduction

Wireless broadband radios supporting multi standards have gained considerable interest in modern wireless communications systems [11, 12, 13, 14]. One key challenge to support a wide set of communication standards and to accommodate different applications in a single device is to design a low power, highly linear, and low noise broadband transceivers. Furthermore, highly linear receiver is inevitably demanding to simplify the expensive front-end module (FEM) and achieve reconfigurability utilizing the scarce spectrum.

As the first block in the receiver chain, the design of a wide-band low-noise amplifier (LNA) that is shared among different standards is a major challenge compared

to the use of multiple narrow bands LNAs supporting parallel-path receiver architectures [16, 17]. Such an LNA should be sufficiently linear to suppress interference and maintain high sensitivity. In addition, it should achieve good impedance matching, high and flat gain, and low noise figure (NF) across a wide frequency band. Also, low area and power consumption design is required for high performance and low cost radios.

Recently, many wideband LNAs in CMOS technology have been reported, including distributed amplifiers [18] and resistive shunt feedback amplifiers [19, 20]. The former offers superior bandwidth in terms of high power consumption, large area, and deterioration of noise performance, which limits its widespread applications. The latter provides good broadband matching, noise, and gain, but it is hampered by greater power consumption, which makes them unattractive for low-power applications. One of the wideband LNA topologies that has been widely investigated is the common-gate (CG) LNA. CG LNA is attractive compared to other topologies as it features wideband input impedance matching and low power consumption. However, it has relatively high NF [22]. This is due to the input matching condition, which restricts a certain value of transconductance to be used that leads to low gain and hence, high NF. Noise reduction techniques are used to overcome the disadvantage of the CG LNA configuration [22, 23, 35]. These techniques are based on gain boosting scheme that uses capacitive cross-coupling and multiple feedbacks to break the trade off between the input matching condition and the NF, which lead to simultaneous reduction in noise and power dissipation.

While the noise and bandwidth of nanoscale CMOS improve with scaling, unfortunately the linearity deteriorates with supply voltage, high-field mobility, velocity saturation, and poly-gate depletion effects [36, 37]. Contrary to the diminishing device linearity, the multimode front-ends require high linearity since radios in the same

platform interfere with each other and multiple channels applied simultaneously to an LNA without filtering act as in-band interferences. Consequently, broadband LNAs must maintain sufficient linearity over a wide frequency range. LNA linearization methods should be simple, should consume minimum power, and should preserve noise figure (NF), gain, and input matching. Many traditional linearization techniques are not feasible for LNAs. For example, resistive source degeneration and floating-gate input attenuation reduce the gain and worsen NF or input matching. Hence, LNA linearization proves significantly more challenging than that of baseband circuits, often requiring innovative techniques.

A Derivative Superposition (DS) method [38, 39] is a linearization scheme that manipulates the different polarity of the third-order derivative (g_3) of a drain current from weak to strong inversion region and has achieved extraordinary linearity in narrowband applications. Since the transconductance of the multi-gate transistor (MGTR) is inherently broadband, the DS method is used also with wideband LNAs achieving high linearity [40, 41].

In this work, a linear wideband differential CG LNA employing capacitor cross-coupling is presented. Complementary DS is used employing an NMOS/PMOS pair to improve the linearity. The presented LNA also avoids the use of bulky inductors resulting in considerable area and cost savings. The presented LNA covers frequency bands for Digital Video Broadcasting (DVB) at 450-850 MHz, Global System for Mobile communications (GSM) at 900 MHz, and Global Positioning System (GPS) at 1.2 and 1.5 GHz, providing a practical solution for multi-standard applications. The Chapter is organized as follows. In Section 2, the capacitor cross-coupled CG LNA is discussed in brief. In Section 3, previously reported CMOS LNA linearization techniques are presented . Section 4 covers the proposed CG LNA, showing detailed analysis for the major LNA parameters. In Section 5, circuit implementation is

presented along with simulation results and measurements.

4.2 Background

Fig. 4.1 (a) shows the differential configuration of the conventional CGLNA. In this circuit, the differential voltage gain, $A_v = \frac{Vop-Von}{Vip-Vin}$, and the differential input impedance, R_{in}, are given by

$$A_v = g_{m1}R_L. \tag{4.1}$$

$$R_{in} = 2/g_{m1}. \tag{4.2}$$

where g_{m1} is the transconductance of transistor M_1. Assuming perfect matching condition ($R_{in} = 2R_S = 100\Omega$), the noise factor, F, is given by

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}. \tag{4.3}$$

where γ is the excess channel thermal noise coefficient, and α is the ratio between g_{m1} and the zero-bias drain conductance, g_{do1}. The last term in (4.3) represents the noise contribution due to the load, R_L. Due to the power matching constraint, the CGLNA suffers a relatively high noise figure, NF.

Noise reduction techniques are used to improve the NF of the CGLNA. The idea to improve the noise performance of the CGLNA is based on introducing a decoupling mechanism between the input power matching condition and the NF. This is achieved by improving the effective transconductance and enhancing the gain. The single-ended model of the transconductance boosting structure is shown in Fig. 4.1 (b). The structure uses an inverting gain A_{NEG} that is inserted in the

feedback between the gate and source terminals of M_1. The effective g_{m1} is boosted to $g_{m1}(1 + A_{NEG})$ with input impedance matching of $1/\left[g_{m1}(1 + A_{NEG})\right] = R_S = 50\Omega$. This means smaller bias current, less channel noise from M_1, and consequently smaller noise contribution and power consumption. The noise factor, F, is then given by

$$F = 1 + \frac{\gamma}{(1 + A_{NEG})\alpha} + \frac{4R_S}{R_L}. \tag{4.4}$$

One possible way to implement the inverting gain, A_{NEG}, is to use cross-coupling capacitors, C_1 as shown in the differential CGLNA topology in Fig. 4.1 (c) [22]. A_{NEG} is approximately given by the capacitors ratio, $(C_1 - C_{gs1})/(C_1 + C_{gs1})$, where C_{gs1} is the gate-source capacitance of M_1. For $C_1 >> C_{gs1}$, A_{NEG} is almost unity, which reduces A_v, R_{in}, and F to the following

$$A_v = 2g_{m1}R_L. \tag{4.5}$$

$$R_{in} = 2R_S = 1/g_{m1}. \tag{4.6}$$

$$F = 1 + \frac{\gamma}{2\alpha} + \frac{4R_S}{R_L}. \tag{4.7}$$

Comparing to the conventional CGLNA, F is reduced and the effective transconductance is increased with reduction in power consumption.

4.3 Linearization techniques

LNA nonlinearity is generally originated from two main sources. First, is the transistor transconductance nonlineaity and this due to the nonlinear raltion between

the drain current and the gate-to-source volatge. For small signal operation, the nonlinear transconductance of NMOS is represented by a power series

$$i_{ds} = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3. \tag{4.8}$$

where g_1,g_2, and g_3 are the linear transconductance and the second and third order nonlinearity coefficients, rescpectively. These coefficients are obtained by taking the derivative of the drain dc current, I_{DS}, with respect to the gate-to-source voltage, V_{GS} at DC operating point

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad g_2 = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}, \quad g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3}. \tag{4.9}$$

Higher order nonlinear terms, beyond g_3, have less weight and can be neglected. Second source of LNA nonlineariy is the transistor nonlinear output conductance,g_{ds}, which becomes apparent under large output voltage swing and when the device operates near the linear region (i.e, small drain-to-soucre voltage). In general, most of the reported linearization techniques are concerned about cancelling the second and third order distortion due to g_2 and g_3. The distortion nonlinearity due to g_{ds} is less noticable and can be neglected to simplify the LNA design. In the following subsections, some of these techniques are presented.

4.3.1 Feedback

For the weakly nonlineary amplifier, G, the input-output characteristics can be a given by a power series

$$y = g_1 z + g_2 z^2 + g_3 z^3. \tag{4.10}$$

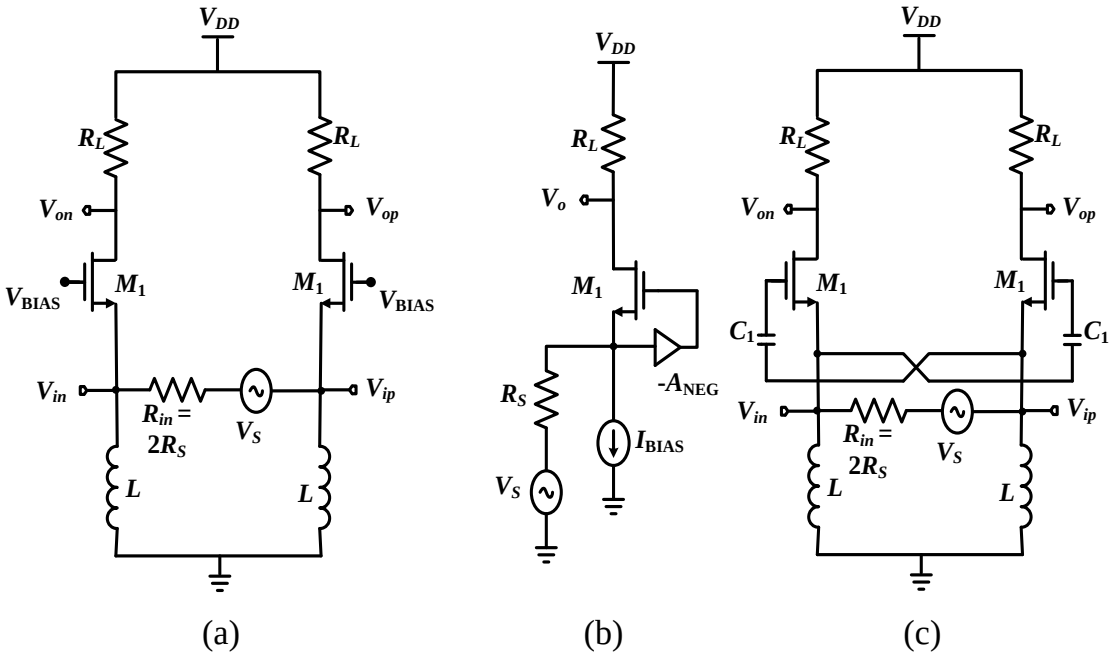

Figure 4.1: Conventional and capacitor cross-coupled differential CGLNA

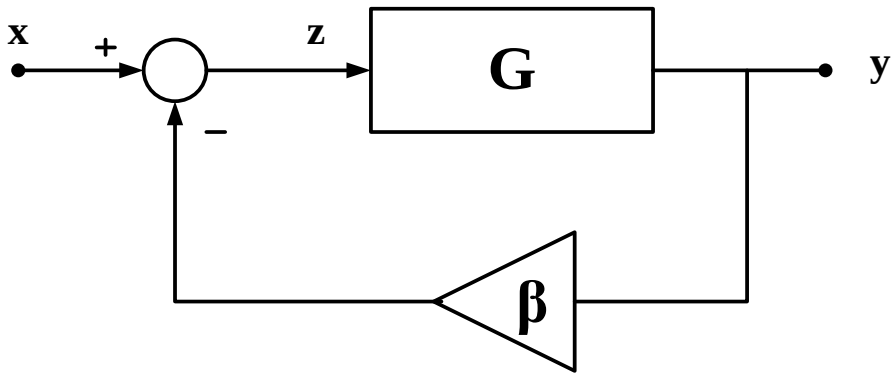

Figure 4.2: Nonlinear amplifier is a negative feedback.

where g_1,g_2, and g_3 are the linear gain and second and third order nonlinear coefficients of the amplifier, respectively. The goal of linearization techniques is to reduce/cancel g_2 and g_3 keeping only the linear term, g_1. The second and third order input intercept points, IIP_2 and IIP_3 of the amplifier, G, are given by:

$$\begin{aligned} A_{IIP_2,G} &= \sqrt{\frac{g_1}{g_2}} \\ A_{IIP_3,G} &= \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \end{aligned} \tag{4.11}$$

When the amplifier, G, is placed in a negative feedback, as shown in Fig. 4.2, the closed-power series

$$y = b_1 x + b_2 x^2 + b_3 x^3. \tag{4.12}$$

$$\begin{aligned} b_1 &= \frac{g_1}{1+g_1\beta} \\ b_2 &= \frac{g_2}{(1+g_1\beta)^3} \\ b_3 &= \frac{1}{(1+g_1\beta)^4}\left(g_3 - \frac{2g_2^2\beta}{1+g_1\beta}\right). \end{aligned} \tag{4.13}$$

where b_1, b_2, and b_3 are the closed-loop linear gain and second and third order nonlinearity coefficients, respectively, and $g_1\beta$ is the open-loop gain. IIP_2 and IIP_3 of the closed-loop system are given by:

$$\begin{aligned} A_{IIP_2,CL} &= \sqrt{\frac{b_1}{b_2}} = \sqrt{\left|\frac{g_1}{g_2}\right|(1+g_1\beta)^2} \\ A_{IIP_3,CL} &= \sqrt{\frac{4}{3}\left|\frac{b_1}{b_3}\right|} = \sqrt{\frac{4}{3}\left|\frac{g_1(1+g_1\beta)^3}{g_3 - \frac{2g_2^2\beta}{1+g_1\beta}}\right|} \end{aligned} \tag{4.14}$$

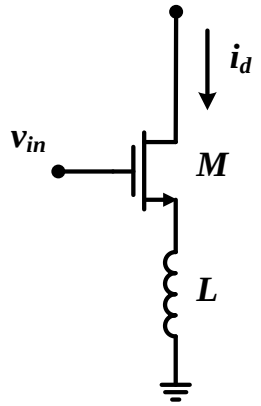

Figure 4.3: Inductively source-degenerated LNA.

Comparing (4.11) with (4.14), it is shown that the negative feedback improves the second order nonlinear distortion by a factor of $(1 + g_1\beta)$. It also improves the third order nonlinear distortion by $(1+g_1\beta)^{3/2}$ when $g_2 = 0$. When $g_2 \neq 0$, the improvment is less. This phenomenon is called second-order interaction, in which the third order nonlinear distortion does not only originate from the amplifier intrinsic third-order nonlinearity, but also from the second-order nonlinearity when a feedback exists.

As an example for the a feedback concept applied to LNAs is the famous inductive source degenerated LNA [42], shown in Fig. 4.3. The inductor, L, creats a feedback path between the output current, i_d, and the input voltage, v_{in}. It acts as frequency-dependent feedback element with $\beta = \omega L$. This feedback method is limited in enhancing the linearity of the LNA because of the insufficient open-loop gain which cannot be large due to the stringent LNA gain, noise, and matching requirements. Also, the effect of the second-order interaction opposes the improvement of the linearity due to feedback. The inductive degenrated LNA is also a not suitable with broadband applications. Using resistive source degeneration will worsen the gain, matching, and, noise figure. In general feedack linearity improvement is not as effective for LNAs as for the baseband circuits.

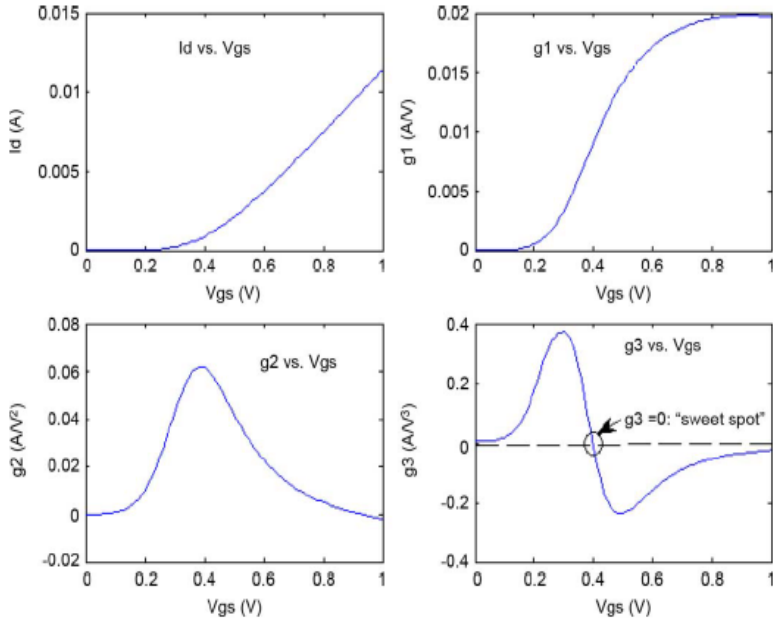

Figure 4.4: NMOS transconductance characteristics [43].

4.3.2 Optimal biasing at sweet spot

The third-order nonlinear coefficient, g_3, features a well-known linearity sweet spot [44]. At the sweet spot, the g_3 value crosses zero as the transistor changes bias from weak to moderate inversion. Fig. 4.4 shows plots for an NMOS drain current, g_1, g_2, and g_3. g_2 is always positive while g_3 has a sign inversion. Although the optimal biasing technique is simple, it has some limitations. The technique is sensitive to process variation which needs automatic biasing that can detect the sweetspot [44]. In this technique, the linearity is improved at certain operating point, which results in a limitation in the input signal range for effective distortion cancellation. Additionally, biasing the transistor at $g_3 = 0$ while require a vertain value of g_1 which leads to low gain and high noise figure.

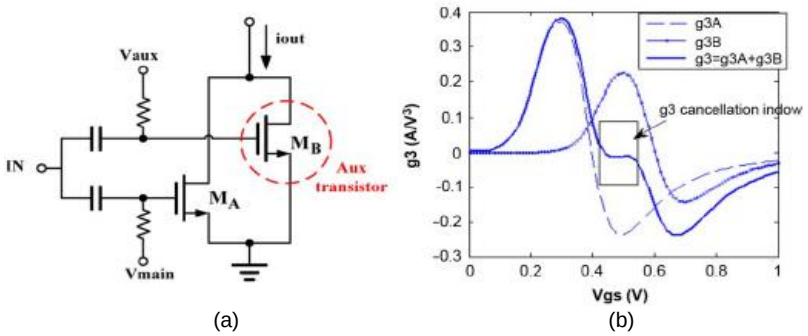

Figure 4.5: (a) DS method (b) Third-order nonlinear coeffiecients [43].

4.3.3 Derivative superposition (DS)

The derivative superposition method [38, 39, 40, 41] is a feedforward linearization technique when the main amplifier is combined together with an auxiliary one working in different region, as shown in Fig. 4.5(a). Exploiting g_3 sign inversion around the sweet spot, zero g_3 can be realized by biasing the main transistor at moderate inversion with negative g_3 and biasing the auxiliary transistor at weak inversion with positive g_3, Fig. 4.5(b). On contrary to the optimal biasing method, DS improves the linearity withing a bias-voltage range instead of just a point. Hence, DS is less sensitive to process variation and can accomodate higher input signal amplitudes. Moreover, the power consumption overhead is small since the auxiliary transistor is working in weak inversion. Since the positive and negative characteristic of g_3 are not symmetric, the cancellation window is fairly narrow with only one auxiliary transistor, but the window widens with more auxiliary transistors at the cost of degraded input matching, NF, and gain [45].

Conventional DS technique have some limitations. First, Although it improves third-order nonlinear distortion, but it ususally worsens the second-order distortion since the sign of g_2 is always positive in both weak and moderate inversion, as shown in Fig. 4.4. The weak inversion transistor used for the auxiliary path may not

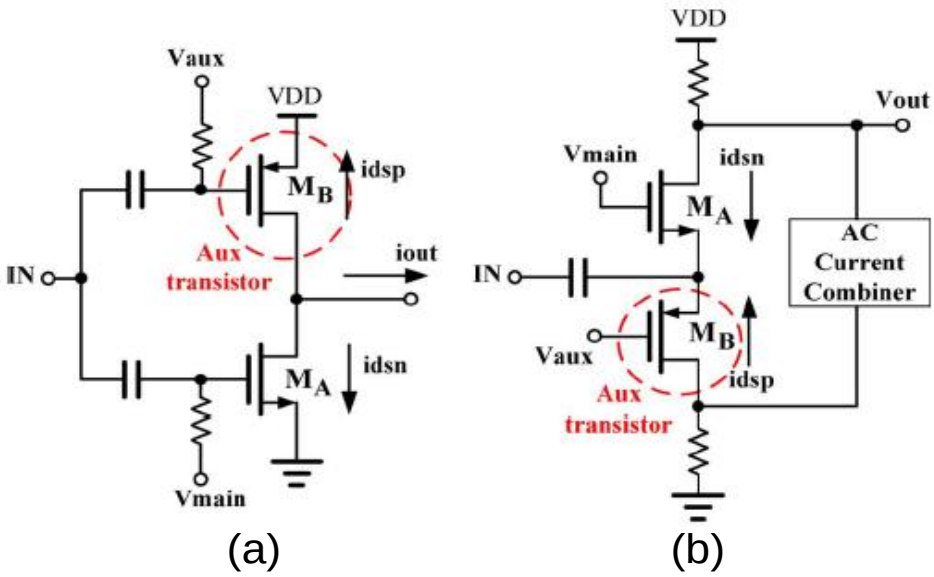

Figure 4.6: Complementary DS (a) Common-source NMOS/PMOS [40] (b) Common-gate NMOS/PMOS [41].

operate at high frequency. Additionally, weak inversion transistor models are generally not accurate resulting in a discrepancy between simulations and measurements. Moreover, matching between transistors working in different regions is difficult and subjected to sensitivity to PVT variations. Complementary DS can be used to improve the IIP_3 without hurting IIP_2 [40, 41]. The complementary DS method uses an NMOS/PMOS pair instead of using a dual weak/moderate inversion NMOS. Fig. 4.6 shows two different circuit realizations for the complementary DS, one using a common-source NMOS/PMOS and the other using a common-gate NMOS/PMOS. More details and analysis for the complementary DS are given in the following section.

4.4 Proposed linear CGLNA

The idea of the proposed LNA is based on enhancing the linearity of the cross-coupled CGLNA in [22] without hurting the gain, noise figure, and matching using the complementary DS linearization technique. As shown in Fig. 4.7, a common-

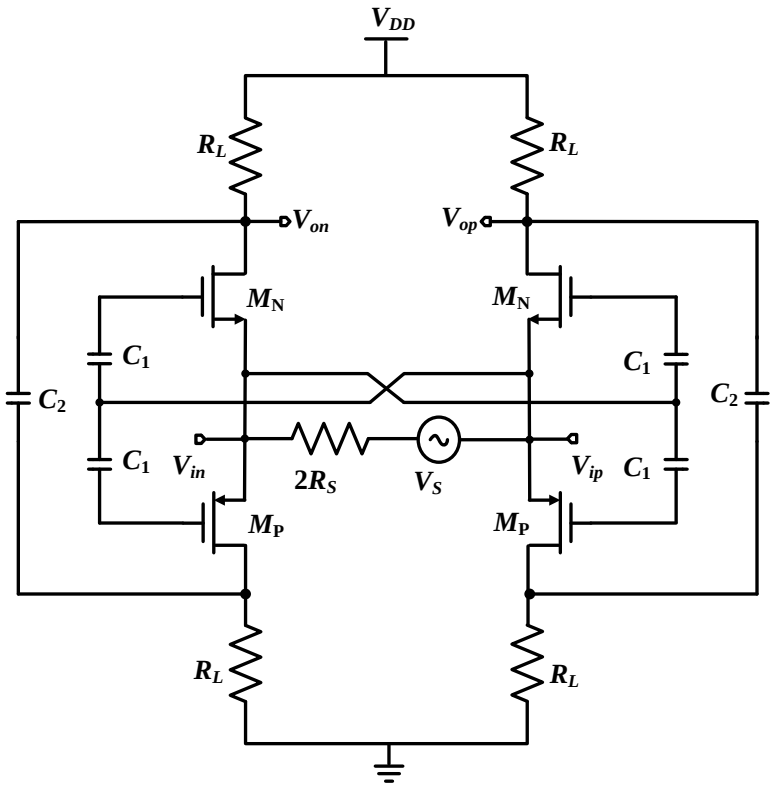

Figure 4.7: Schematic of the proposed CGLNA (biasing circuit not shown).

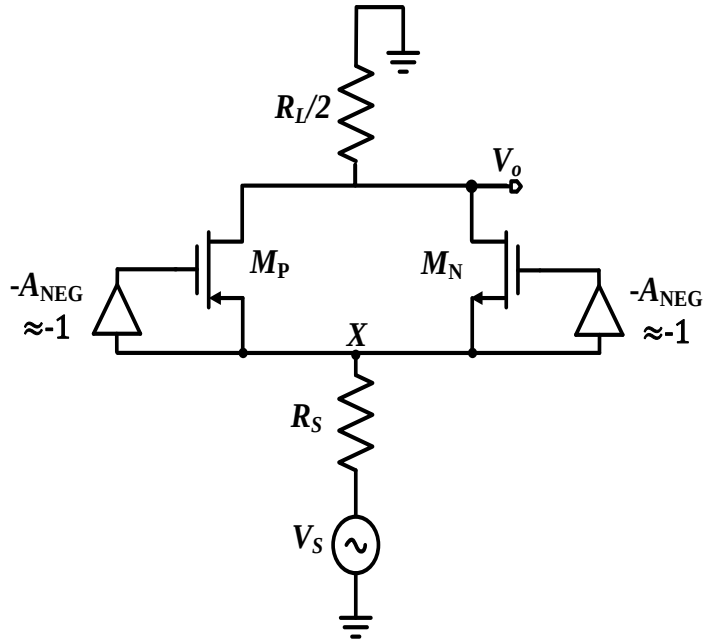

Figure 4.8: Simplified single-ended CGLNA model.

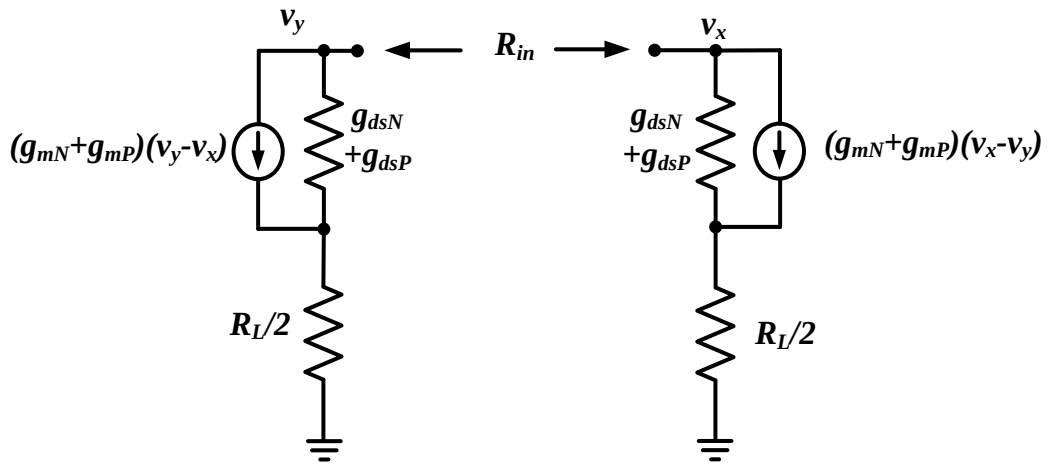

Figure 4.9: Small signal model of the proposed CGLNA.

gate pair NMOS/PMOS, M_N and M_P, that are capacitively cross-coupled using C_1. Another large coupling capacitor, C_2, with negligible impedance within signal bandwidth, is used to combine the ac current of M_N and M_P. The single-ended model is shown in Fig. 4.8. C_1 is replaced by short circuit boosting the effecive transconductance which leads to lower noise figure and lower power compared to conventional CGLNA. Also C_2 is replaced by short circuit combining M_N and M_P to cancel/reduce the third-order nonlinear distortion, g_3, to improve IIP_3 without hurting the IIP_2, as will seen in th following subsections.

4.4.1 Input impedance and gain

While calculating the input impedance of the proposed CGLNA, the coupling capacitors, C_1 and C_2, in Fig. 4.7 are replaced with short circuits since they are much larger than the gate and drain capacitances of the input transistors, M_N, and M_P. Referring to the small signal model of the proposed CGLNA, shown in Fig. 4.9, the differential input impedance, R_{in} is given by:

$$R_{in} = \frac{1 + g_{dsN}R_L/2 + g_{dsP}R_L/2}{g_{mN} + g_{mP} + g_{dsN}/2 + g_{dsP}/2}. \tag{4.15}$$

where g_{mN}, g_{mP}, and g_{dsN}, g_{dsP} are the transconductances and the output conductances of the transistors M_N and M_P, respectively. Thus, the input matching condition is given by

$$(2g_m + g_{ds})R_s = 1 + g_{ds}R_L/2. \tag{4.16}$$

where $g_m = g_{mN} + g_{mP}$, $g_{ds} = g_{dsN} + g_{dsP}$, and $R_s = 50\Omega$. Neglecting the transistors output conductances ($g_{ds} = 0$), the input matching condition reduces to

$$2g_m R_s = 1. \tag{4.17}$$

which is the same result for the cross-coupled CGLNA reported in [22]. Boosting the effective transconductance, $(2g_m)$, compared to the conventional CGLNA enables the use of lower g_{mN} and g_{mN} values to achieve the same resistive input matching. This means less bias current and hence, lower power consumption. Lower noise figure is also achieved as will be seen later.

The differential voltage gain, $A_v = \frac{Vop-Von}{Vip-Vin}$ of the proposed CGLNA, shown in Fig. 4.7, is given by:

$$A_v = \frac{2g_m + g_{ds}}{1 + g_{ds}R_L/2}R_L/2. \tag{4.18}$$

4.4.2 Stability

The condition of stability is based on the approach of the return ratio, RR [25]. This approach is used to study the amplifier stability in the presence of feedback loops and to model bidirectional paths between input and output. For the proposed

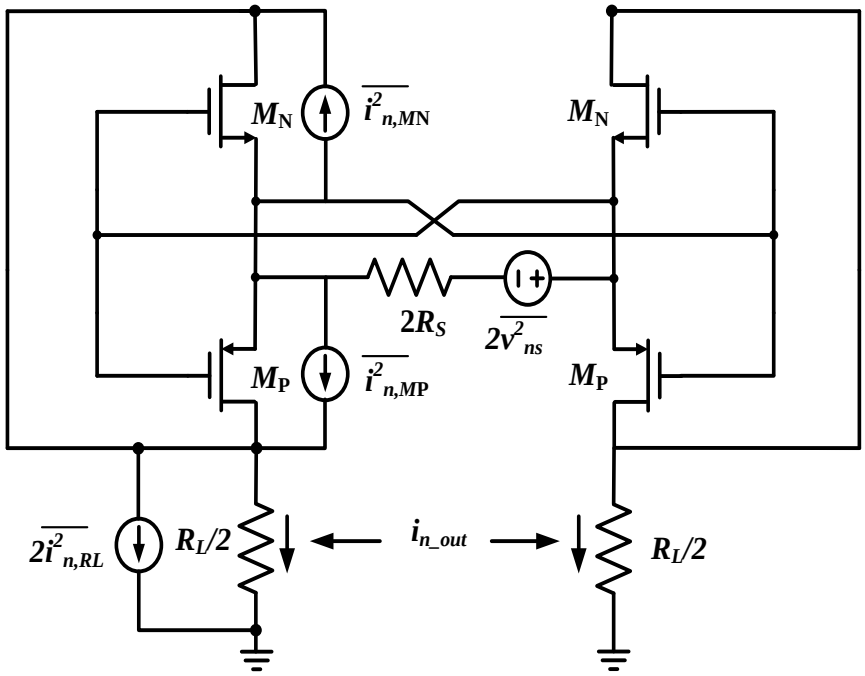

Figure 4.10: Schematic of the proposed CGLNA showing noise sources.

CGLNA, the RR has the following expression:

$$RR = \frac{-2g_m R_s}{1 + 2g_m R_s}. \tag{4.19}$$

The proposed CGLNA is stable if $-1 < RR < 0$ and this is always guaranteed.

4.4.3 Noise analysis

Fig. 4.10 shows a simplified model for the noise sources of the proposed CGLNA. The circuit noise performance is analyzed and its NF is computed assuming that the dominant noise sources are due to the thermal noise of the transistors and the load. The coupling capacitors, C_1 and C_2, in Fig. 4.7 are replaced with short circuits. Each half circuit contributes four sources of noise: The source resistance, v_{ns}, the thermal noise due to M_N, i_{n,M_N}, the thermal noise due to M_P, i_{n,M_P}, and that due to the load, i_{n,R_L}, as shown in Fig. 4.7. Constructing the small signal model of the

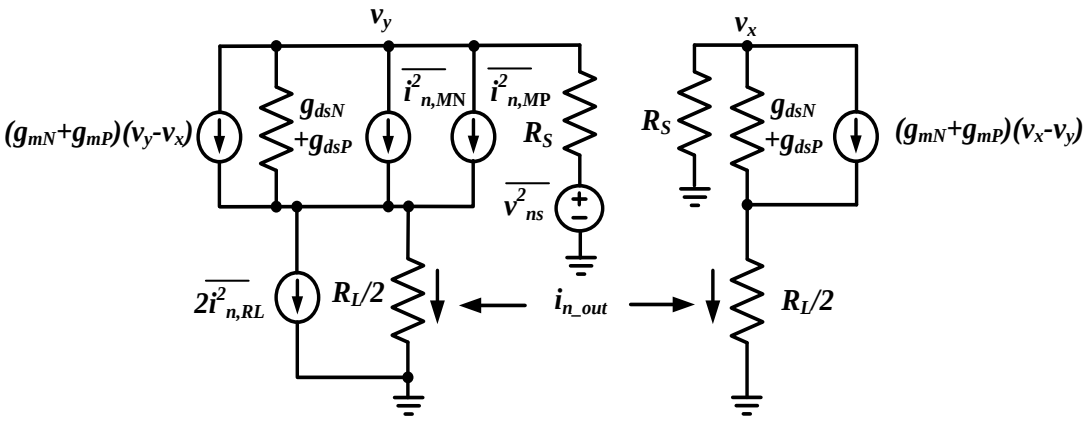

Figure 4.11: Small signal model of the proposed CGLNA showing noise sources.

transistors M_N and M_P and considering the effect of their output conductances, g_{dsN} and g_{dsP}, respectively, as shown in Fig. 4.11, the induced differential output noise currents due to each noise source is given by:

$$\overline{i^2_{ns-out}} = \frac{(2g_m + g_{ds})^2\overline{v^2_{ns}}}{(1 + 2g_mR_s + g_{gds}R_s + g_{gds}R_L/2)^2} \tag{4.20}$$

$$\overline{i^2_{n,M_N-out}} = \frac{\overline{i^2_{n,M_N}}}{(1 + 2g_mR_s + g_{gds}R_s + g_{gds}R_L/2)^2} \tag{4.21}$$

$$\overline{i^2_{n,M_P-out}} = \frac{\overline{i^2_{n,M_P}}}{(1 + 2g_mR_s + g_{gds}R_s + g_{gds}R_L/2)^2} \tag{4.22}$$

$$\overline{i^2_{n,R_L-out}} = \frac{2(2g_mR_s + g_{ds}R_s + 1)^2\overline{i^2_{n,R_L}}}{(1 + 2g_mR_s + g_{gds}R_s + g_{gds}R_L/2)^2}. \tag{4.23}$$

where $g_m = g_{mN} + g_{mP}$ and $g_{ds} = g_{dsN} + g_{dsP}$. Substituting with $\overline{v^2_{ns}} = 4kTR_s\Delta f$, $\overline{i^2_{n,M_N}} = 4kT\frac{\gamma_N}{\alpha_N}g_{mN}\Delta f$, $\overline{i^2_{n,M_P}} = 4kT\frac{\gamma_P}{\alpha_P}g_{mP}\Delta f$, and $\overline{i^2_{n,R_L-out}} = 4kT/R_L\Delta f$, the

noise factor, F, is given by:

$$F = \frac{\overline{i^2_{ntotal-out}}}{\overline{i^2_{ns-out}}} = 1 + \frac{\overline{i^2_{n,M_N-out}} + \overline{i^2_{n,M_P-out}} + \overline{i^2_{n,R_L-out}}}{\overline{i^2_{ns-out}}}$$

$$= 1 + \frac{\gamma_N}{\alpha_N}\frac{g_{mN}}{(2g_m + g_{ds})^2 R_s} + \frac{\gamma_P}{\alpha_P}\frac{g_{mP}}{(2g_m + g_{ds})^2 R_s} + \frac{2(2g_m R_s + g_{ds} R_s + 1)^2}{(2g_m + g_{ds})^2 R_s R_L}. \quad (4.24)$$

Note that the last term accounts for the noise contribution due to the load, R_L. Increasing the value of R_L relative to R_s reduces the load noise contribution to the overall noise figure. Neglecting the transistors output impedance and the load thermal noise and under the input power matching condition, $2(g_{mN} + g_{mP})R_s = 1$, F reduces to

$$F = 1 + \frac{\gamma_N}{\alpha_N}\frac{g_{mN}}{2g_m} + \frac{\gamma_P}{\alpha_P}\frac{g_{mP}}{2g_m}. \quad (4.25)$$

For $g_{mN} = g_{mP}$ and $\frac{\gamma_N}{\alpha_N} = \frac{\gamma_P}{\alpha_P} = \frac{\gamma}{\alpha}$, F is given by:

$$F = 1 + \frac{\gamma}{2\alpha}. \quad (4.26)$$

which is the same results for the cross-coupled CGLNA reported by Zhuo in [22]. Compared to the conventional CGLNA, the proposed CGLNA can achieve less noise figure using the same concept of transconductance boosting in [22]. intuitively, $g_m boosting$ allows the use of lower g_{mN} and g_{mP} values which is translated to smaller bias current that results in less channel noise from the input transistor and correspondingly leads to smaller noise contribution.

4.4.4 Linearity

As shown in the previous subsections, tha using the capacitively cross-coupled complementary NMOS/PMOS doesn't hurt the matching and noise figure compared

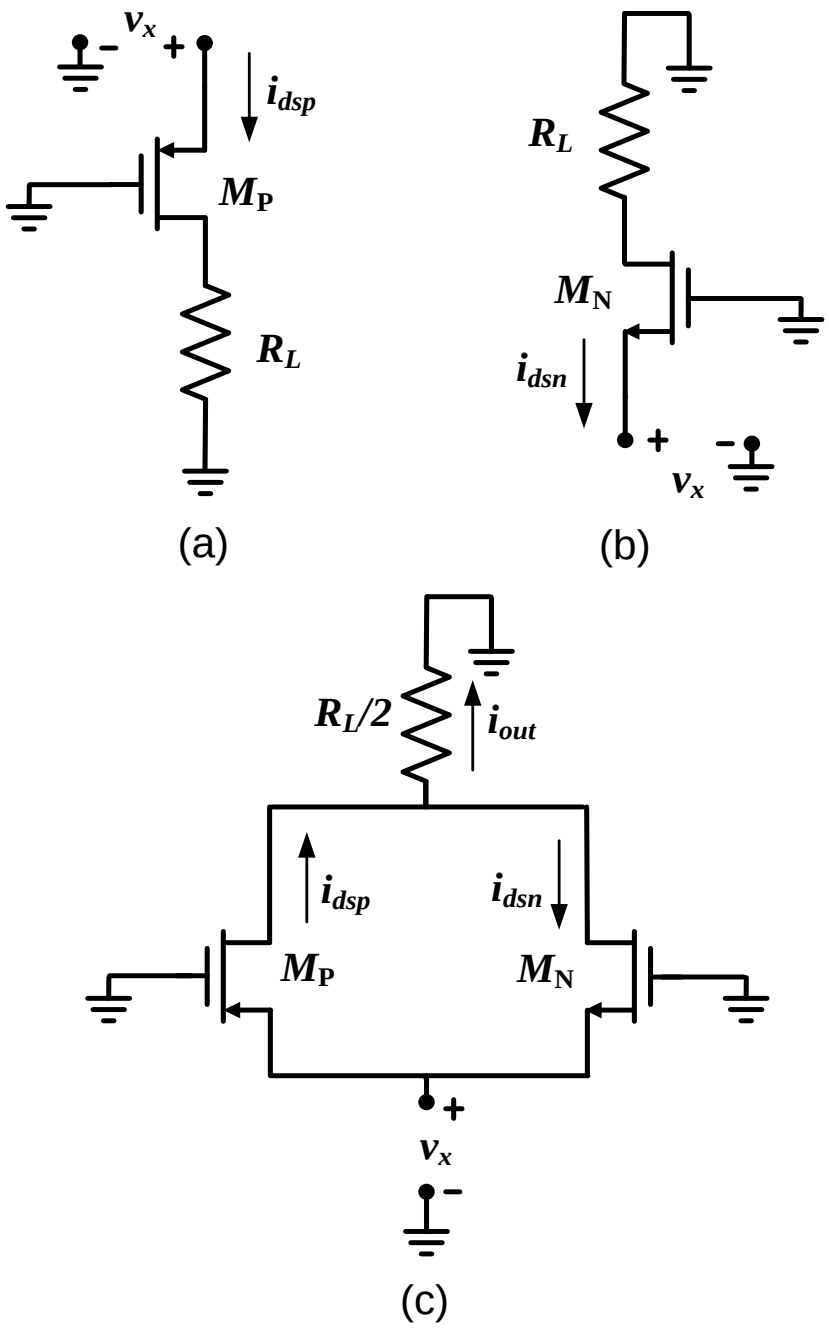

Figure 4.12: Common-gate schematic for distortion analysis (a) PMOS (b) NMOS (c) Complementary NMOS/PMOS DS.

to the capacitively cross-coupled NMOS. However, it has the advantage of enhancing the gain by combining the ac current using the large coupling capacitor, C_2, as shown in Fig. 4.7. The schematic of the common-gate amplifier for distortion analysis for NMOS, PMOS, and complementary NMOS/PMOS is shown in Fig. 4.12. The ac NMOS and PMOS currents, i_{dsn} and i_{dsp}, respectively and the ac complementary NMOS/PMOS output current, i_{out} are expressed by the following power series:

$$\begin{aligned} i_{dsn} &= g_{1N}v_{gs} + g_{2N}v_{gs}^2 + g_{3N}v_{gs}^3 \\ &= -g_{1N}v_x + g_{2N}v_x^2 - g_{3N}v_x^3. \end{aligned} \tag{4.27}$$

$$\begin{aligned} i_{dsp} &= g_{1P}v_{sg} + g_{2P}v_{sg}^2 + g_{3P}v_{sg}^3 \\ &= g_{1P}v_x + g_{2P}v_x^2 + g_{3P}v_x^3. \end{aligned} \tag{4.28}$$

$$\begin{aligned} i_{out} &= i_{dsp} - i_{dsn} \\ &= (g_{1P} + g_{1N})\, v_x + (g_{2P} - g_{2N})\, v_x^2 + (g_{3P} + g_{3N})\, v_x^3. \end{aligned} \tag{4.29}$$

It can be seen from (4.29) that the amplifier linear transconductance increases, the nonlinear second-order distortion decreases because g_{2P} and g_{2N} have the same sign, and the nonlinear third-order distortion decreases because g_{3P} and g_{3N} have different signs. As shown in Fig. 4.13, a cancellation window for g_3 exists for a finite input range compared to just a point in the optimal biasing linearization technique. Moreover, $g_2 = 0$ happens at the same region where the improvement of g_3 exists, which means that the optimum IIP_2 and IIP_3 can share the same optimum bias. Improvement in IIP_2 happens at a single point though. In our case, IIP_2 is not a

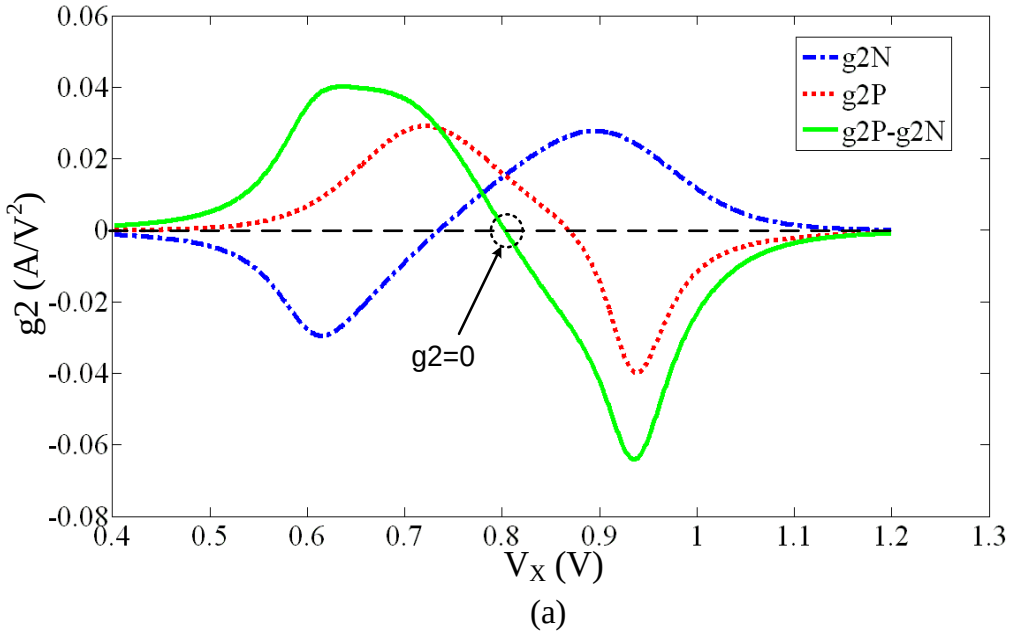

Figure 4.13: Second/third-order nonlinear distortion coefficients of NMOS, PMOS, and total for complementary NMOS/PMOS as a function of the bias (IBM 90 nm CMOS process, $(\frac{W}{L})_{M_N} = \frac{44\ \mu\text{m}}{0.1\ \mu\text{m}}$ and $(\frac{W}{L})_{M_P} = \frac{100\ \mu\text{m}}{0.1\ \mu\text{m}}$).

concern because we are dealing with differential signals.

4.5 Circuit design and measurement results

The proposed linear LNA with an IIP_3 of 6 dBm, voltage gain of 15.5 dB, 3-dB bandwidth of 1.6 GHz and a minimum noise figure of 3 dB over the band is implemented by the IBM 90nm CMOS process. A highly linear voltage buffer is used at the LNA output to drive the 50Ω load of the measuring equipment. Coupling capacitors are used between the LNA and the buffer to provide the buffer with separate DC bias. The gain and noise figure of the buffer are predetermined to de-embed their effect from the overall response to get the LNA response. The total schematic of the LNA with the buffer is shown in Fig. 4.14. Table 4.1 shows the transistor aspect ratios for the proposed LNA and buffer. In the layout implementation, the transistors are laid out with maximum number of fingers and close to minimum width per finger to minimize the effective series gate resistance, to reduce the signal loss and improve the noise figure specially for the input transistors, M_N and M_P. The coupling capacitors, employed in the design, are implemented using MIMCAP device supported by the IBM 90nm CMOS process which has a density of 5.8 fF/μm^2 . The biasing resistors are implemented using poly resistors. Fig. 4.15 shows a micrograph of the fabricated CGLNA/buffer with a chip size of 1mm×1mm (including the pads). The core LNA area is 0.03 mm^2

The core LNA consumes 0.86 mA from a 1.8 V supply while the buffer consumes 10 mA from a 2 V supply. The LNA is encapsulated in a micro leadframe (QFN) open package, where the DC biases and input RF signal are applied/monitored using an FR-4 printed circuit board (PCB). The output signal is monitored using a G-S-G-S-G differential probe. This measurement setup is used to evaluate the performance of the LNA including the PCB traces and packaging effect. Baluns are used at

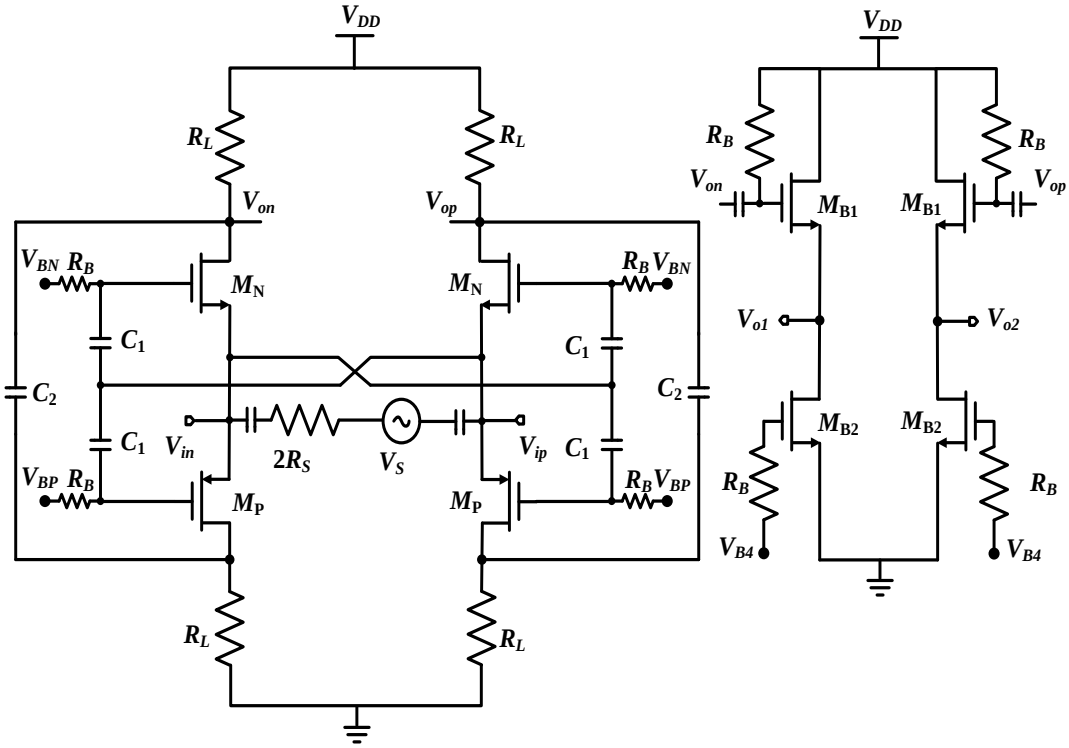

Figure 4.14: Schematic of the entire LNA with the output buffer

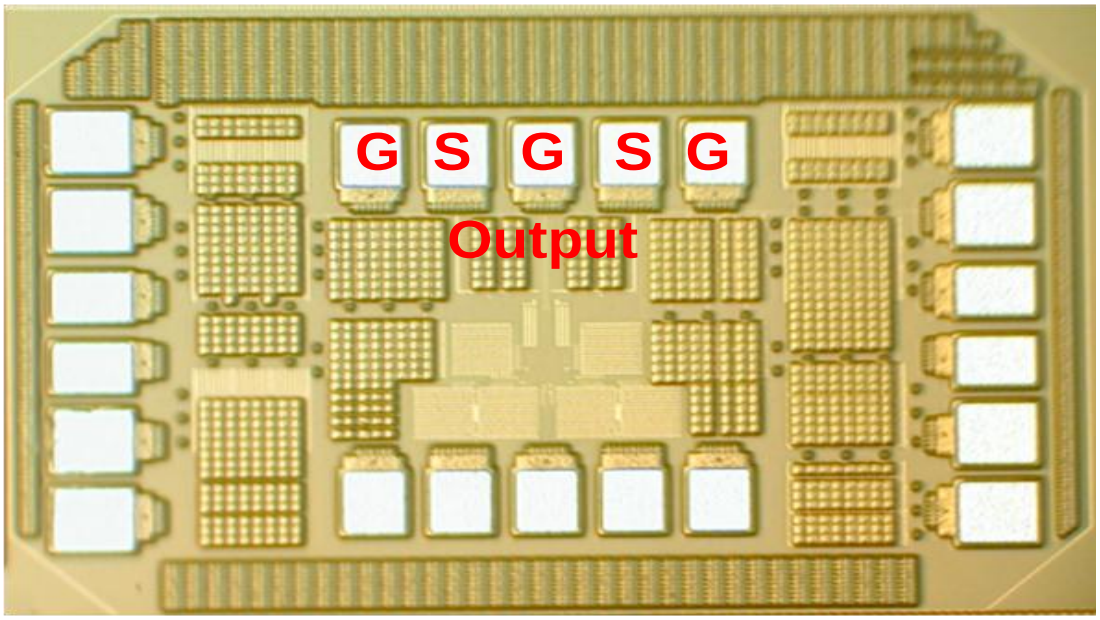

Figure 4.15: Die photo of the proposed LNA.

input and the output for single-ended to differential signal conversion. Figs. 4.16, 4.17, and 4.18 show the post layout simulated and the measured input reflection coefficient, S_{11}, voltage gain, and noise figure, NF, respectively. They are plotted versus RF input frequency up to 2 GHz after de-embedding the effect of the output buffer. The measured S_{11} is lower than -12 dB from 100 MHz up to 2 GHz (Fig. 4.16). The voltage gain is measured to be 15.5 dB in the passband with an upper 3-dB frequency of 1.6 GHz (Fig. 4.17). The measured minimum NF is 3 dB with degraded performance at the lower and higher frequencies because of the flicker noise and LNA bandwidth limitation respectively (Fig. 4.18). The input-referred intercept point, IIP_3, for the proposed wideband CGLNA is measured using a two-tone test for a 150 MHz operating frequency. The two tones are applied with the same amplitude and a frequency offset of 30 MHz. An IIP_3 value of 6 dBm is obtained as shown in Fig. 4.19.

Table 4.2 compares the performance of the proposed CGLNA with that of the state-of-the-art wideband LNAs around the same frequency range. The power consumption reported is of the core LNA only. As shown in the table, the proposed broadband LNA can achieve good NF and linearity with low power consupmtion when compared to previously reported wideband LNAs.

Table 4.1: Transistor aspect ratios for the LNA and buffer

$(\frac{W}{L})_{M_N}$	$(\frac{W}{L})_{M_P}$	$(\frac{W}{L})_{M_{B1}}$	$(\frac{W}{L})_{M_{B2}}$
$\frac{44\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{100\ \mu\text{m}}{0.1\ \mu\text{m}}$	$\frac{35\ \mu\text{m}}{0.175\ \mu\text{m}}$	$\frac{50\ \mu\text{m}}{0.175\ \mu\text{m}}$

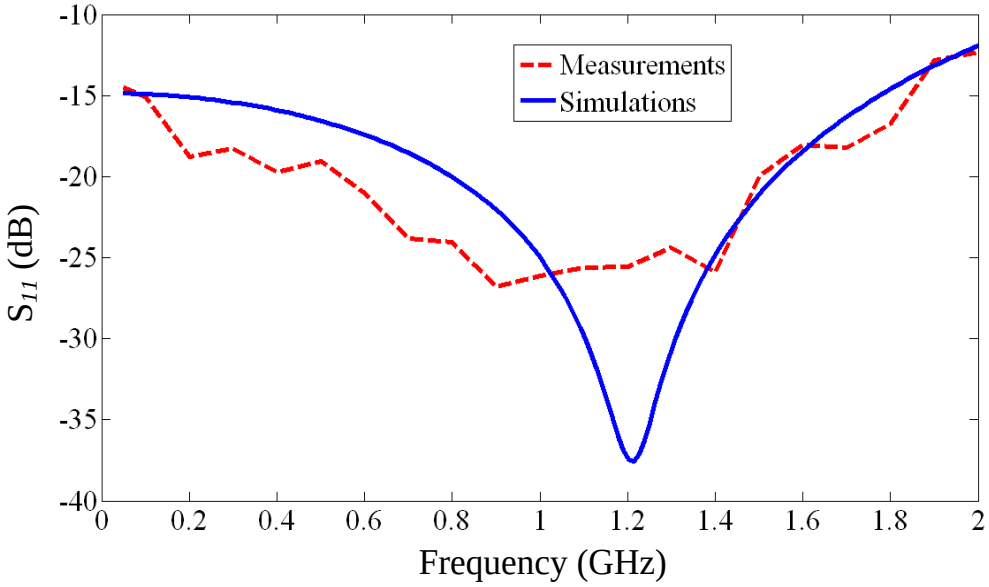

Figure 4.16: Measured and simulated input matching versus RF input signal frequency

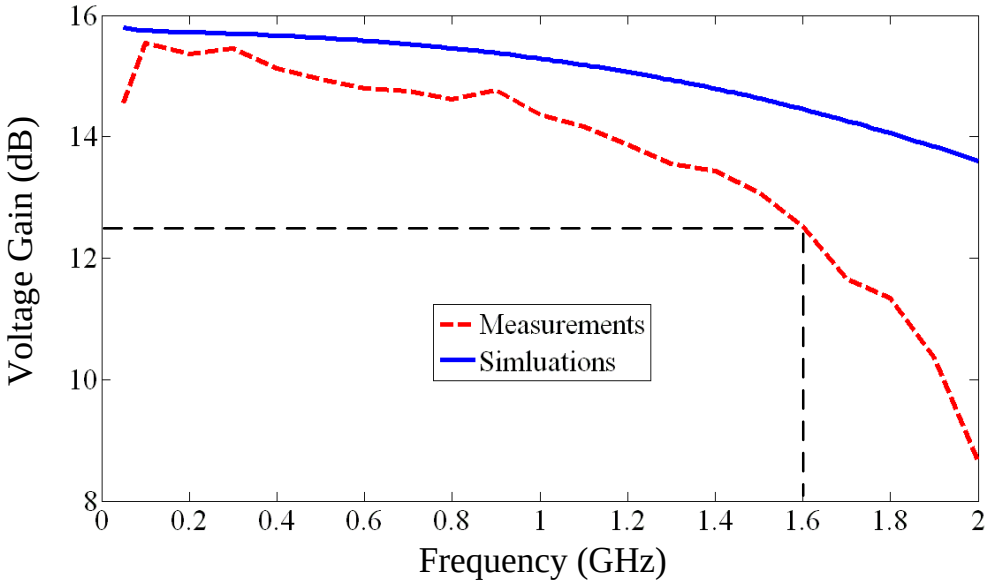

Figure 4.17: Measured and simulated voltage gain versus RF input signal frequency

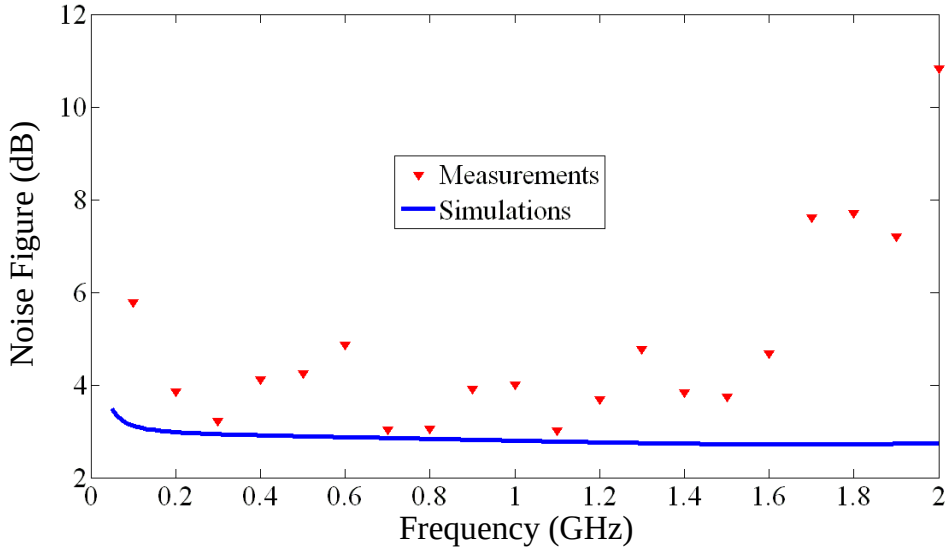

Figure 4.18: Measured and simulated noise figure versus RF input signal frequency

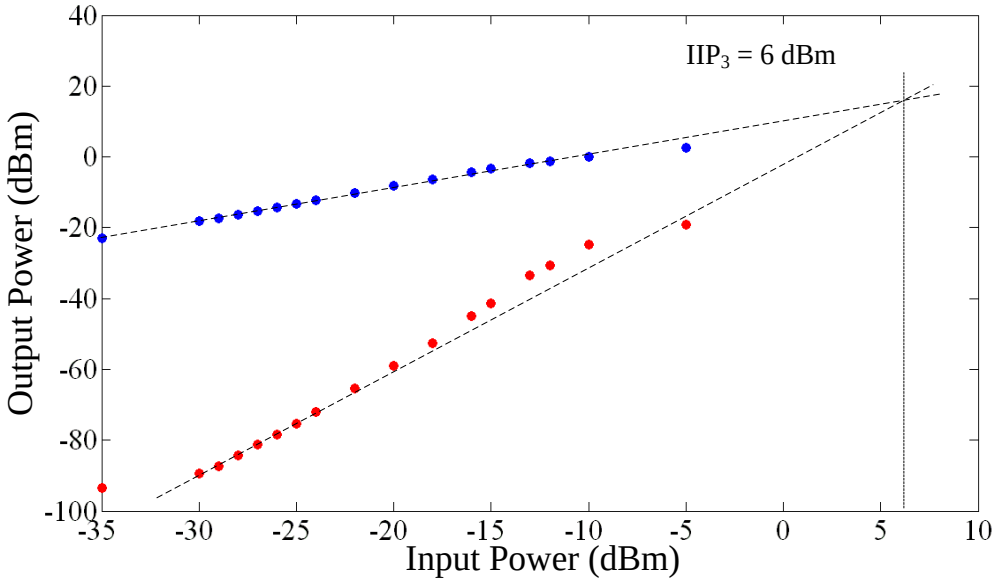

Figure 4.19: Measured IIP_3 for the proposed CGLNA

Table 4.2: Performance summary of the proposed broadband LNA and comparison with the existing work

Ref.	Gain (dB)	Freq. Range (GHz)	NF_{min} (dB)	S_{11} (dB)	IIP_3 (dBm)	P_{DC} (mW)	Active Area (mm^2)	Tech CMOS
[40]	14 [b]	0.048-1.2	3	<-8	3	34.8	0.16	0.18 μm
[41]	14.5 [b]	0.8-2.1	2.6	-8.5	16	17.4	0.1	0.13 μm
[28]	20.5 [b]	0.02-1.175	3 [a]	<-10	2.7	32.4	0.12	0.18 μm
[29]	13.7	0.002-1.6	1.9 [a]	<-8	0	35	0.075	0.25 μm
[46]	14 [b]	0.04-1.2	2.1	<-10	0	14.4	0.036	0.18 μm
[47]	11.4	0.054-0.88	4.2	<-16.7	5	41.4	0.71 [c]	0.18 μm
[48]	14.5[b]	0.072-0.85	3.6	<-9	2.5	9.6	0.08	0.13 μm
[49]	14.5[b]	0.15-1	2.5	<-8	1	3	0.06	0.13 μm
This work	15.5	0.1-1.6	3	-12	6	1.55	0.03	90 nm

[a] Estimated from data provided in the corresponding papers.
[b] Power Gain.
[c] Total area

5. HIGH-PSRR LOW-POWER SINGLE SUPPLY OTA*

A CMOS single supply operational transconductance amplifier (OTA) is reported in this work. It has high power supply rejection capabilities over the entire gain bandwidth (GBW). The OTA is fabricated on the AMI 0.5 μm CMOS process. Measurements show power supply rejection ratio (PSRR) of 120 dB till 10 KHz. At 10 MHz, PSRR is 40 dB. The high performance PSRR is achieved using a high impedance current source and two noise reduction techniques. The OTA offers a very low current consumption of 25 μA from a 3.3 V supply. It is suitable for applications such as Low Drop Out voltage regulators (LDOs).

5.1 Introduction

TThe recent trend of System-on-Chip (SOC) implementation of modern integrated circuits (IC) processes, have employed analog circuits to be placed in the same environment with noisy digital, switched capacitors, and DC-DC converter circuitry, thus experience a high noise coming in from the supply lines. This noise can significantly decrease the performance by reducing in the dynamic range of the whole system, especially in high precision systems or if the circuits that are sensitive to supply noise are at the very beginning of the power supply/reference chain. It is therefore essential that the circuits in these applications, e.g. operational amplifiers (OAs) that are used as voltage reference buffers or as on chip low dropout regulators, have good power supply regulation both at DC and at high frequency.

The performance of a system influenced by power supply variation is described as Power Supply Rejection Ratio (PSRR) [50]. If the transfer function from input

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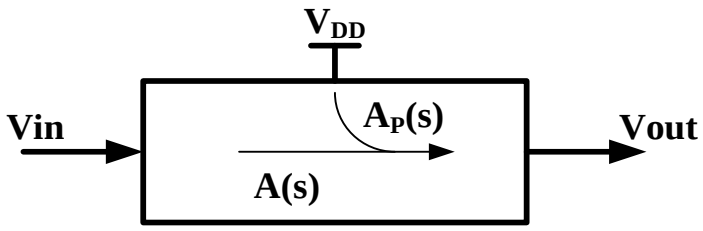

Figure 5.1: Block Diagram of general electric circuit.

to output is $A(s)$ and the transfer function from power node to output is $Ap(s)$, $PSRR(s)$, as shown in Fig. 5.1, is defined as:

$$PSRR(s)(dB) = 10log(\frac{Ap(s)}{Ap(s)}). \tag{5.1}$$

A number of different techniques have been developed to overcome the problem of power supply rejection [50, 51, 52, 53]. The main focus of most of the solution is directed towards the improvement of the supply line rejection for mid frequency range where the compensation capacitor of the two stage miller amplifier, in Fig.5.2, becomes short, thus making the second stage acts like a unity gain buffer and reflects the variation at the supply lines to the output without any attenuation. One of the techniques is the insertion of a cascode transistor [51] between the compensation capacitor and gate of output transistor to prevent it from getting diode connected at high frequency. This technique offers a much improved high frequency power supply rejection ratio (PSRR) but complicates the compensation of the amplifier. Another method involves using a parallel path [52] from the supply lines to the output to cancel out the noise coming from the supply at the frequency of interest. This method provides a high PSRR without disturbing the signal path and has no effect on the stability, but need a separate branch which increases the power requirement.

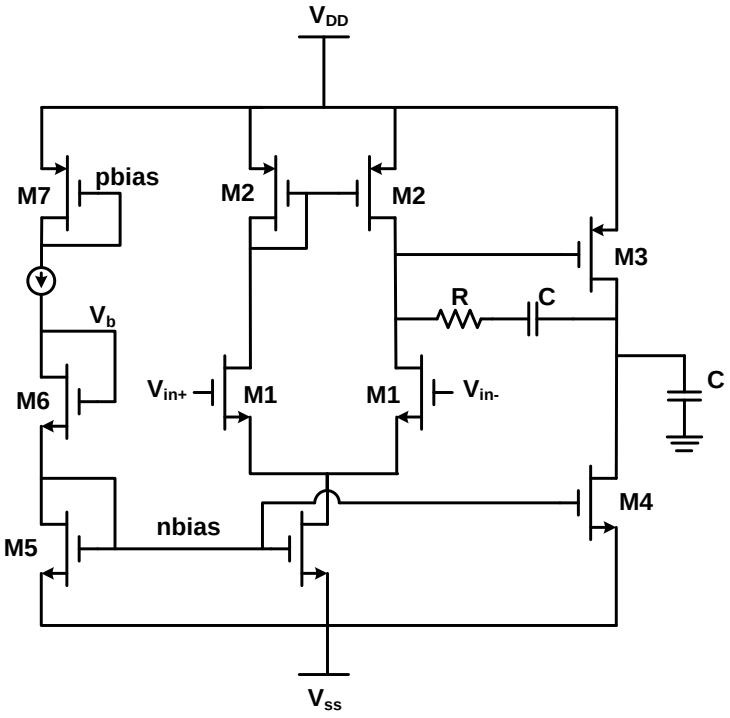

Figure 5.2: Two Stage Miller Amplifier.

A high PSRR class AB topology [53] is also a solution. It uses a completely separated NMOS and PMOS signal path and a thick gate oxide transistor which shields the NMOS cascode transistors from impact ionization at high supply voltages. This technique requires extra fabrication process for the thick gate oxide.

In this work, a CMOS single supply operational transconductance amplifier (OTA) with high PSRR is presented. A high output impedance current source [54, 55] and noise reduction techniques are used to improve of PSRR both at DC and at higher frequency up to the gain bandwidth (GBW) of the OTA, respectively. The presented OTA has a simple structure and it offers a very low quiescent current (25 μA) compared to other reported structures. The Chapter is organized as follows. In Section 2, background on the PSRR rejection techniques is summarized. Section 3 covers the new proposed solution. Finally, measurement result is shown in section 4.

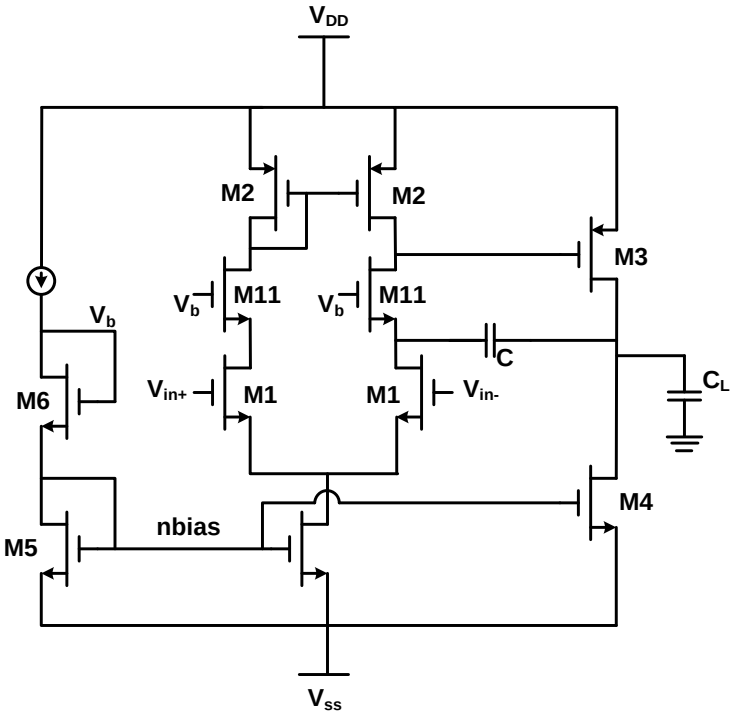

Figure 5.3: Cascode Compensation PSRR technique.

5.2 Background

5.2.1 Use of cascode transistor [51]

The circuit for realizing high PSRR using a cascode compensation technique is shown in Fig. 5.3. The addition of the cascode transistors in the input stage permits the connection of the compensating capacitor to the source of a common-gate device (cascode transistor), which decouples the gate of the driver transistor from the compensation capacitor. This technique offers a much improved high-frequency power-supply rejection ratio (PSRR), but complicates the compensation of the amplifier. One disadvantage of this circuit, however, is a reduction in common-mode input range due to the voltage drop across the cascodes which limits the use of such circuits in applications that uses a virtual ground such as the switched capacitor integrators. Unity gain buffers which required wide common-mode input range can't

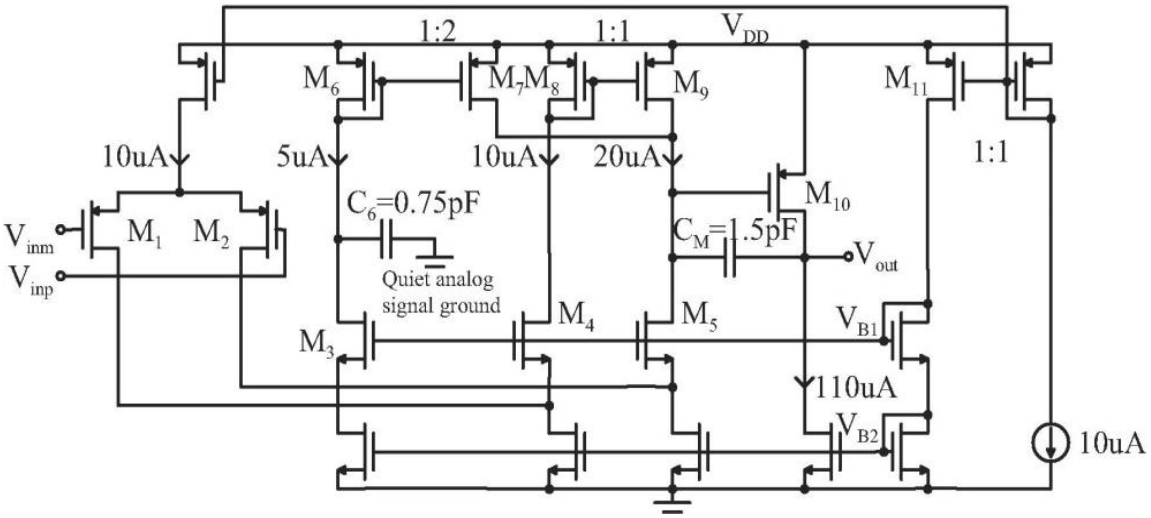

Figure 5.4: Parallel path using current mirror PSRR technique.

use this scheme.

5.2.2 Use of Parallel path [52]

A simple circuit technique is presented for improving poor midband power supply rejection ratio (PSRR) of single ended amplifiers that use Miller capacitance to set location of the dominant pole. The principle of the technique is to create an additional parallel signal path from the power supply to the output, which cancels the dominating unity gain signal path through the output stage and Miller capacitor above the dominant pole frequency. The technique is able to have improvement of more than 20 dB over the two stage Miller capacitance amplifier. As shown in Fig. 5.4, a current amplifier is created from the supply to the output using current mirror, thus controlling the size of the capacitor needed in the branch by the current ratio. The parallel path for the PSRR circuitry means that the third pole is not visible to the differential signal path, and therefore it does not degrade the stability margins. In other words, high frequency pole considered, which allows the presented technique to be used equally well in heavy resistive load applications, where the absolute sec-

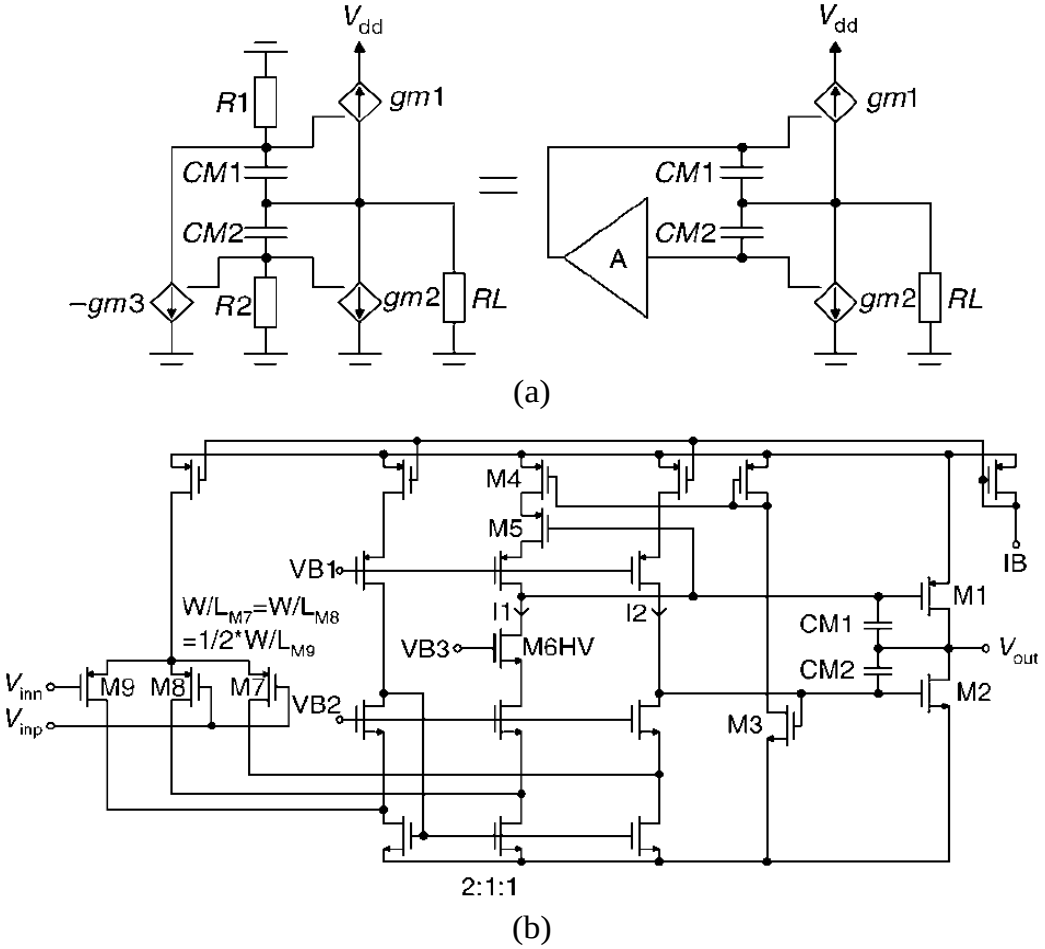

Figure 5.5: (a) Small signal model of the output stage (b) Implementation of Class AB compensation for high PSRR.

ond pole location varies considerably with the load current. Also, this technique is robust to mismatches since it relies on current mirror and capacitor ratios which are well controlled in practice. However, the introduction of the parallel path leads to a reduction in the DC gain by 6 dB, and an increase in noise and offset of the amplifier.

5.2.3 Use of ground referenced negative feedback [53]

The main idea behind the PSRR improvement technique discussed here is to use ground referenced negative feedback, provided by the class AB control loop, to lower the positive power supply gain above the dominant pole frequency. The negative

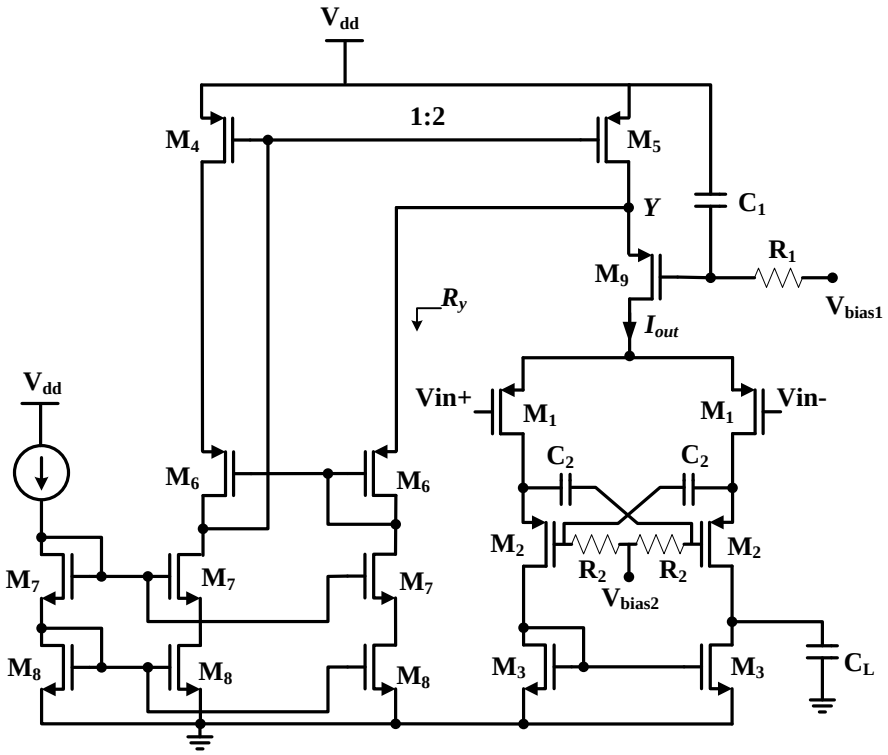

Figure 5.6: Proposed High PSRR single supply OTA.

feedback path that is responsible for boosting PSRR can be most easily seen by looking at the small signal model of the output stage as shown in Fig. 5.5(a). If gm2 is neglected by assuming that the disturbance at the Vout is small, the gm1 along with gm3 forms a ground referenced miller compensated amplifier which has a feedback network formed by CM2 and R2 around it. It is this feedback that attenuates any disturbance injected from the power supply through gm1 by the frequency dependent loop gain. The complete amplifier is shown in Fig. 5.5(b)

5.3 Proposed system

The target is to build an low power OTA with high PSRR not only at DC, to reduce the influences of 50/60 Hz clock-frequencies, but also at higher frequency which is important especially in aliasing (sampled data) contexts where high frequency

power supply noise can be folded back into the signal band [50]. As shown in Fig. 5.6, a single stage differential pair OTA is used, (M1-M3), in order to minimize the power consumption and to avoide the GBW limitation of the two stage configuration. The cascode transistor M2 is used to achieve higher open loop voltage gain. To obtain a high PSRR at DC, an improved tail current source (CS) with high output impedance is used [54, 55]. The CS consists of transistors (M4-M8) and achieves a low compliance voltage VDSAT which is suitable for the OTA cascode configuration employed. For proper operation, transistors M4 and M5 need to satisfy the following aspect ratios:

$$\frac{W}{L}_{M_5} = 2\frac{W}{L}_{M_4} \tag{5.2}$$

For higher frequency PSRR improvement, two noise reduction solutions are utilized. The first solution, as shown in Fig. 5.6, uses a capacitor, C_1, and a resistor, R_1, to form a high pass filter. This filter injects the noise coming from the supply through M6. The supply noise has an opposite polarity and tends to reduce the noise coming from the direct pass through M5. Applying the small signal and calculating $\frac{i_{out}}{vdd}$ that is approximately given by:

$$\frac{i_{out}}{vdd} = \frac{-sC_1R_1}{(1+sC_1R_1)\,(R_y + 1/g_{m9})}. \tag{5.3}$$

Given that $g_{m6}r_{o6}$ and $g_{m9}r_{o9} >> 1$, where g_{mk} and r_{ok} are the transconductance and output resistance of transistors M6 and M9, respectively. R_y is the resistance seen from node Y as shown in Fig. 5.6. Eq. (5.3) represents the high pass filter response of the of the supply rejection with cut off frequency, $\omega = 1/(C_1R_1)$, that is adjusted at the frequency of interest.

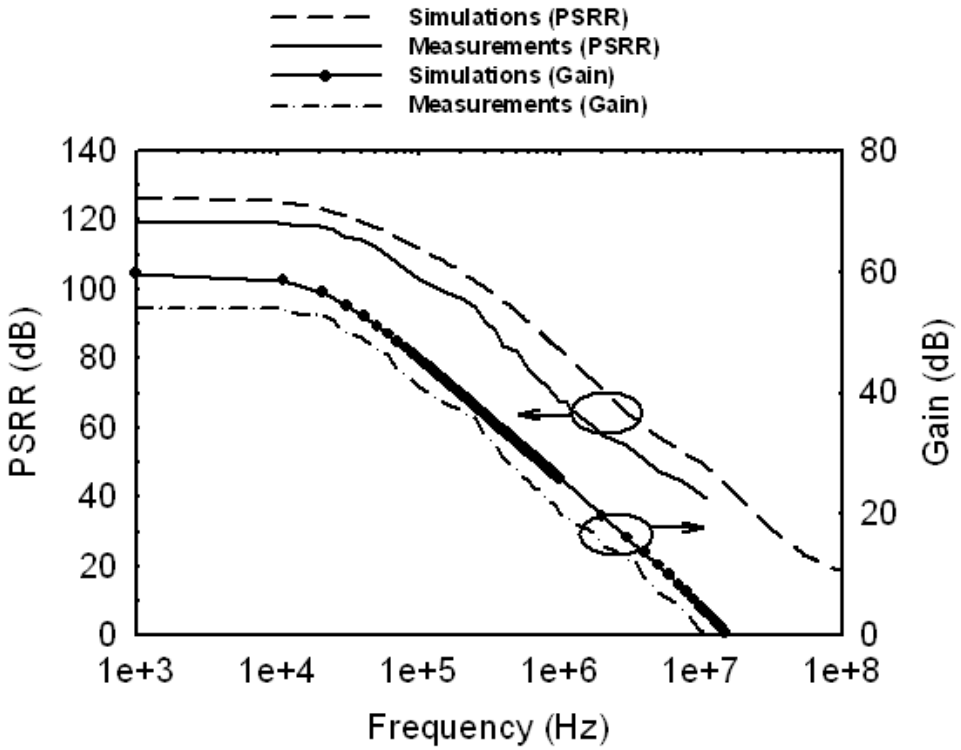

Figure 5.7: Measured and simulated Gain and PSRR.

The second solution to improve the PSRR is based on the cross coupled structure consisting of a pair of matched capacitors and resistors (C_2 and R_2), as shown in Fig. 5.6. The idea is based on trying to minimize the gate-to-source voltage of transistors M2 due to the noise coming from the supply at the frequency of interest and hence minimizing the noise current to the output. The drawback of this solution is the increase of the capacitance at the drains of M1 and hence the values of the nondominant poles at these nodes are reduced which in turns degrade the OTA GBW. Therefore, C_2 value should be carefully chosen.

5.4 Measurement result

The OTA is fabricated on the AMI 0.5 μm CMOS process. The OTA consumes 25 μA from a single supply of 3.3 V. Fig. 5.7 is showing the Gain and PSRR curves.

At 10 KHz, the PSRR is typically 120 dB and it starts to drop till it reaches 40 dB at 10 MHz. Other performance parameters are summarized in Table 5.1 and compared with other reported high PSRR amplifiers [53, 56, 57].

Table 5.1: The proposed high PSRR OTA performance and comparison

Parameters	This work	This work*	[56]	[57]	[53]
Technology	0.5μm	0.5μm	0.35μm	0.8μm	0.35μm
Power Suppy	3.3V	3.3V	2.7-5V	$\pm 1V$	2.7-5V
Load	1.2 pF	20 pF//2 MΩ	20 pF//10 KΩ	100 pF//25 KΩ	20 pF//1 MΩ
Voltage Gain (dB)	52	40	>106	>100	>90
GBW (MHz)	10	1.28	10.6	1.8	5.4
Phase Margin	42^o	83^o	51^o	51^o	61^o
PSRR (dB)	120 @1KHz 67.5 @1MHz 40 @10MHz	100 @1KHz 85 @1MHz	63 @100KHz 40 @1MHz	VDD 98.06 @1KHz 80.75 @10KHz VSS 107.46 @1KHz 91.94 @10KHz	64 @100KHz 30 @1MHz
SR+/SR- (V/μs)	3.62/4.56	0.22/0.3	5.8 min	0.82/0.75	-
Current consumption (μA)	25	25	298	203	165

$*$ Simulated.

6. CONCLUSION

In Chapter 2, a new multi-phase multi-path technique has been presented for harmonic distortion cancellation. It has full digital control in generating the phases at the digital front-end, aiming at increasing the accuracy and reducing the power consumption over other reported techniques. Moreover, flexibility in applying the proposed multi-phase scheme to different current-output PA architectures is achieved. Mathematical analyses along with simulations were done to verify the proposed idea. Trade-offs in signal loss, LO harmonics, and image rejection between the poly-phase multi-path technique in [6] and the proposed technique were also presented.

In Chapter 3, An inductorless broadband CGLNA employing noise reduction is proposed. The LNA relies on multiple feedbacks to fully decouple the tradeoff between noise and input power matching. The theory shows that the proposed approach reduces the lower limit of the noise performance of the previously reported CGLNAs, allowing for a noise figure around 1.4 dB. Measurements of a fabricated prototype in 90 nm CMOS technology show a voltage gain of 23 dB with a 3-dB bandwidth of 1.77 GHz. A minimum noise figure of 1.85 dB and an IIP_3 of -2.85 dBm are also measured. The measured noise figure is lower than the best reported noise figure of CGLNAs. The LNA consumes 2.8 mW from a 2 V supply.

In Chapter 4, An inductorless capcitive cross-coupled broadband CGLNA employing linearity distortion reduction is proposed. The LNA relies on complemantery NMOS/PMOS DS with capacitive coupling for linearity and noise improvement. The theory shows that the proposed approach can enhance the lineaity without hurting the noise and gain of the capacitive cross-coupled LNA. Measurements of a fabricated prototype in 90 nm CMOS technology show an IIP_3 of 6 dBm at voltage gain

of 15.5 dB with a 3-dB bandwidth of 1.6 GHz. A minimum noise figure of 3 dB and are also measured. The LNA consumes 1.55 mW from a 1.8 V supply.

In Chapter 5, A high PSRR OTA is proposed suitable for LDOs. The OTA is fabricated and measured. It has rejection capabilities over a wide band up to the GBW of the OTA. A 52 dB of gain is obtained through single stage differential amplifier with cascode transistors. High PSRR is achieved at DC till 10 KHz, 120 dB, using a high output impedance current source. PSRR improvement is achieved at higher frequencies using two noise reduction techniques, a high pass filter and cross coupled capacitors, which show a PSRR of 40 dB at 10 MHz.

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