ADVANCED HIGH-SPEED FLYWHEEL ENERGY STORAGE SYSTEMS FOR PULSED POWER APPLICATION

A Dissertation

by

SALMAN TALEBI RAFSANJAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2008

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Hamid A. Toliyat
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ABSTRACT

Advanced High-Speed Flywheel Energy Storage Systems

for Pulsed Power Applications. (December 2008)

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Power systems on modern commercial transportation systems are moving to more electric based equipment, thus improving the reliability of the overall system. Electrical equipment on such systems will include some loads that require very high power for short periods of time, on the order of a few seconds, especially during acceleration and deceleration. The current approach to solving this problem is sizing the electrical grid for peak power, rather than the average. A method to efficiently store and discharge the pulsed power is necessary to eliminate the cost and weight of oversized generation equipment to support the pulsed power needs of these applications. High-speed Flywheel Energy Storage Systems (FESS) are effectively capable of filling the niche of short duration, high cycle life applications where batteries and ultra capacitors are not usable. In order to have an efficient high-speed FESS, performing three important steps towards the design of the overall system are extremely vital. These steps are modeling, analysis and control of the FESS that are thoroughly investigated in this dissertation.

This dissertation establishes a comprehensive analysis of a high-speed FESS in steady state and transient operations. To do so, an accurate model for the complete FESS is derived. State space averaging approach is used to develop DC and small-signal AC models of the system. These models effectively simplify analysis of the FESS and give a strong physical intuition to the complete system. In addition, they result in saving time and money by avoiding time consuming simulations performed by expensive packages, such as Simulink, PSIM, etc.

In the next step, two important factors affecting operation of the Permanent Magnet Synchronous Machine (PMSM) implemented in the high-speed FESS are investigated in detail and outline a proper control strategy to achieve the required performance by the system. Next, a novel design algorithm developed by S.P. Bhattacharyya is used to design the control system. The algorithm has been implemented to a motor drive system, for the first time, in this work. Development of the complete set of the current- and speed-loop proportional-integral controller gains stabilizing the system is the result of this implementation.

In the last part of the dissertation, based on the information and data achieved from the analysis and simulations, two parts of the FESS, inverter/rectifier and external inductor, are designed and the former one is manufactured. To verify the validity and feasibility of the proposed controller, several simulations and experimental results on a laboratory prototype are presented.

To Maryam for her priceless love.

To my dear dad and mom for their continuous support and devotion.

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1. INTRODUCTION

1.1. Overview

Power systems on modern commercial transportation systems, such as spacecraft, ship, train, bus, and vehicle [1-3] are moving to more electric based equipment which has improved the reliability of the overall system through a more electric configuration. There are, however, several complications that must be taken into account when developing on-board electrical power supply networks.

First of all, electrical equipment on such systems will feed some loads that require very high powers for short periods of time in the order of a few seconds. An example can be that of accelerating an electrical train in railroad applications [4]. Similar to aircrafts at take-off, electrical trains consume very high power only for short periods of time during the acceleration, dissipating this power in the form of heat later when the train brakes. The current approach to this problem is sizing the electrical grid for the peak power, rather than the average.

Another consideration is that there will be a wide variety of electrical loads ranging from propulsion engines to very sensitive computer equipment. The uninterruptible power supply for the latter is of a special concern by itself, since computers control all vital functions of an airplane or a modern ship. Above all, the equipment needs to be as compact and lightweight as possible.

This dissertation follows the style and format of *IEEE Transactions on Industry Applications.*

The types of power required by these applications are different than conventional power generation equipment which is typically designed for constant load power. While generation equipment can be designed to provide high power levels on a continuous basis, a method to efficiently store and discharge the high pulsed power is necessary to eliminate the cost and weight of oversized generation equipment to support the pulsed power needs of these applications [5-7].

Traditionally, these are based around electrochemical batteries, however, they are not capable of high charge/discharge rates, have limited cycle life, unobservable state of charge, require continuous maintenance and impose disposal problems [8]. Existing battery based energy storage systems are well suited to provide power for durations of 5 minutes to 2 hours. These systems are of limited use in short duration, high cycle life, deep discharge, and small sized applications. Ultra Capacitors and Super Capacitors are newer technologies targeted to fill the energy storage requirements in the lower power ranges, and while offering high discharge powers for short durations they are limited by some of the same issues as batteries', i.e. cycle life limitations, disposal, and a much higher cost [9].

Driven by the growing demand for energy storage and power conditioning in commercial applications, Flywheel Energy Storage System (FESS) provides an alternative to electrochemical batteries and is free of the above mentioned disadvantages have been outlined successfully [7,9,10]. While being a very old technology, flywheels have gained a new life empowered by latest developments in rotating electrical machinery including non-contact magnetic bearings and permanent magnet motors/generators utilizing new powerful magnet materials (NdFeB and SmCo) [11-18].

Flywheel systems are best suited for peak output powers of 100 kW to 2 MW and for durations of 12 seconds to 60 seconds [7] and [9]. These systems may produce a lower power output for longer durations as the function between power output and time is a linear function. Similarly, while the energy is present in the flywheel to provide higher power for a shorter duration, the peak output power is limited by the generator design and the power electronics configuration. For instance, a flywheel designed for 125 kw for 16 seconds stores enough energy to provide 2 MW for 1 second. The energy level required for a 1 second discharge of 2 MW is less than 0.6 kW-hr, the same usable energy in a 16 second, 125 kW discharge flywheel. With a generator and power electronics designed for the 125 kW peak at its minimum output speed, the additional power is not realizable. To provide high discharge for very short durations, the generator and power electronics must be configured such that the power from the stored energy can be realized.

Low speed flywheels are a standard design in the market but are not able to offer advantages in size or cost [9, 19]. Higher speed systems allow the generator to be much smaller, minimizing the overall system size and cost [7, 9]. In a flywheel energy storage system, energy is stored in the form of kinetic energy by rotating a mass at a determined speed. High speed flywheel systems are designed to minimize losses in the system so that power is able to be pulled from the system for the longest possible time [20]. Technologies such as magnetic bearings [15-18], high speed generators [14, 21, 22], vacuum pumps, composite materials [23] and power electronics can increase the efficiency of flywheel systems but can also add cost to the system. A typical high-speed FESS consists of the main components, flywheel, motor/generator, vacuum-sealed housing, power electronics, and some times an external inductor as shown in Figure 1-1.

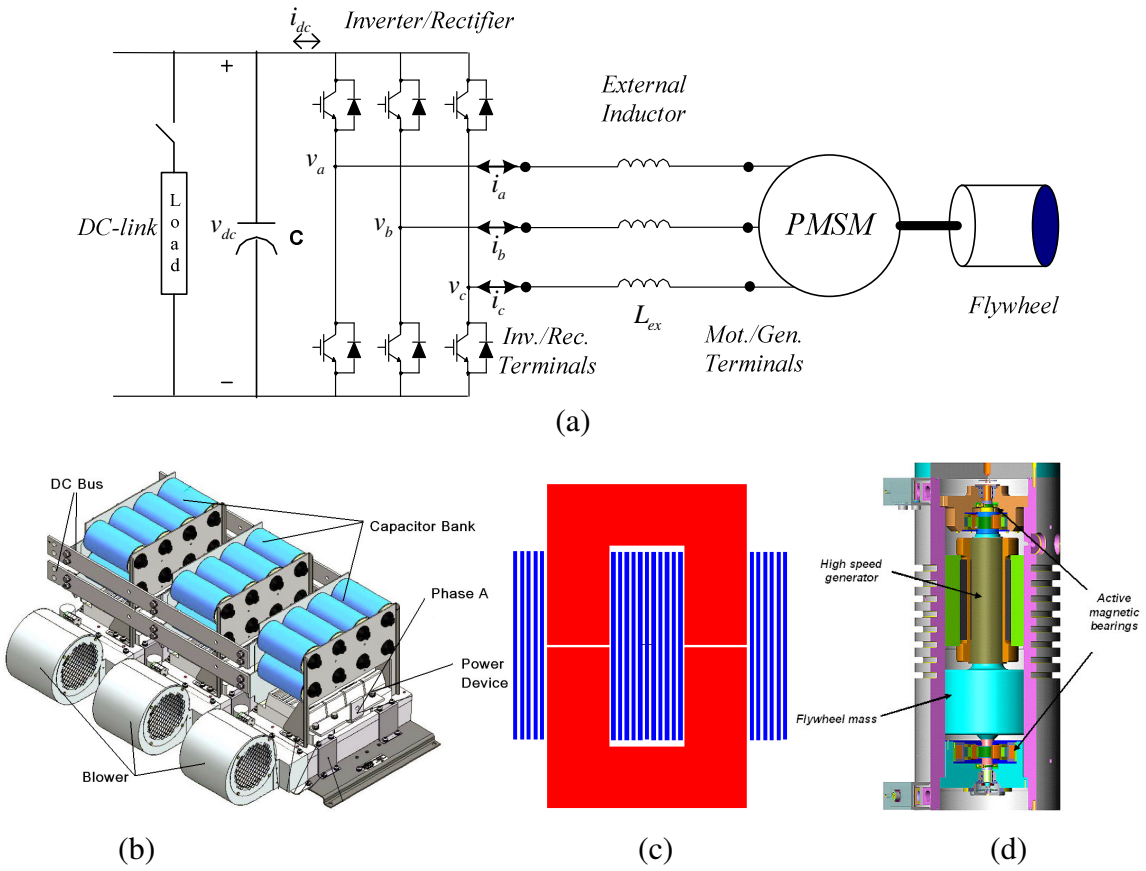


Figure 1-1 (a) Flywheel energy storage system with external inductor, (b) Three-phase IGBT-based inverter/rectifier, (c) External inductor, (d) PMSM/Flywheel [24].

If the flywheel operates at high speeds, the system requires the use of specialized bearings such as magnetic bearings for non-contact support of the flywheel. The functions of each component and how it affects the overall performance of the system are briefly described in the following sections.

1.2. Flywheel

The flywheel is the system component responsible for storing energy in kinetic form when spinning at high speed. When selecting the appropriate design configuration

for the flywheel, hub performance metrics such as stored energy vs. flywheel weight, stored energy vs. volume, or weight vs. cost can influence the overall performance of the system. For each application a different set of performance criteria are critical. For example in space applications, energy vs. weight ratio often has the highest importance [25-27], while for the earth-based applications energy vs. volume ratio tends to be more significant [28-34].

Flywheel performance metrics in a large degree depend on the materials used for the flywheel manufacturing. Presently, the most promising flywheel materials in terms of energy density are conventional high-strength steels and more modern composite materials. One of the advantages of the conventional high-strength steels is that they are mechanically well-known and predictable, as are their methods of manufacturing. The high-strength steels offer relatively high tensile strength in order of 330 ksi, but also high density (0.29 lb/in^3). As an example, a flywheel energy storage system developed and manufactured by Calnetix Inc. [24] for power conditioning applications employs a rotor made of hardened 4340 steel. The rotor assembly has a weight of 207 lbs and stores 1.25 kWh of energy when spinning at 36,000 rpm (weight of the motor/generator is not included). The ratios of the stored energy vs. rotor weight and volume are 13.3 Wh/kg and 105 kWh/m^3 respectively.

Modern composite materials feature much higher tensile strength up to 920 ksi combined with much lower density (typically 0.065 lb/in^3) [31]. The use of composite materials may increase both ratios of the energy vs. rotor weight and volume; however, practical data has only demonstrated an increase of the energy vs. weight ratio. One example of composite flywheel rotors is the transit bus flywheel system developed at the

Center for Electro Mechanics at the University of Texas in collaboration with Calnetix Inc. The stored energy vs. weight and energy vs. volume ratios in this example are 37 Wh/kg and 73 kWh/m^3 respectively (motor/generator is not included into consideration). Based on these and other examples, it appears that composites do not bring enough advantages to most applications (with the exception of space-based applications) to offset the inherent risks related to creep, temperature sensitivity, and integration.

The flywheel itself is not expected to be the most crucial component in development of flywheel systems for pulsed power applications since existing steel flywheels store enough energy for most scenarios. For example, the Vycon flywheel developed as a generator backup in UPS applications stores enough energy to deliver 125 kW for 16 seconds [35]. The same amount of energy could be used to deliver 2 MW for 1 second, but, as previously mentioned, this output requirement would require the redesign of the motor/generator and resizing of the power electronics.

1.3. Motor/Generator

Successful application of flywheel energy storage technology requires compact, reliable and highly efficient motors/generators to transfer energy into and out of flywheels. High-speed operation and high reliability requirements limit selection of motors/generators to brushless and windingless-rotor types [11-14, 21-22]. Among these, Permanent Magnet (PM) machines have the most advantages, including higher efficiency and smaller size when compared with other types of motors/generators of the same power rating, such as induction or variable reluctance machines. They also exhibit lower rotor losses and lower winding inductances, which make it more suitable for a vacuum

operating environment and the rapid energy transfer of flywheel applications [20]. Very low cogging torque and robust rotor construction with very low parts count are additional arguments for using PM motor/generators in flywheel applications.

In order to minimize system size, the motor/generator is designed to be operated at high speed. To illustrate this point, Figure 1-2 shows a 2 MW PM generator developed at Calnetix Inc. [24] side by side with a conventional low speed machine of the same rating. For a pulsed power output, this machine would be capable of a short output pulse of 10 MW, 5 times its continuous rating. Typical for PM machines, the pulsed output rating is 2 to 5 times the continuous machine power rating. For this output to be useful, the machine impedance must be very low to allow for the power to be removed very quickly. High-speed PM machines offer this low impendence with low number of stator turns and large operating magnetic air gaps.

Minimization of the machine size may cause a thermal issue specific for this application which will have to be addressed [20]. While most machines are designed to operate at a continuous output power, a pulsed output application will require short duration, high power output, combined with relatively long duration, low power input. This implies periodic existence of very high current and power densities within the machine, which will require an effective method to transfer heat within the design.

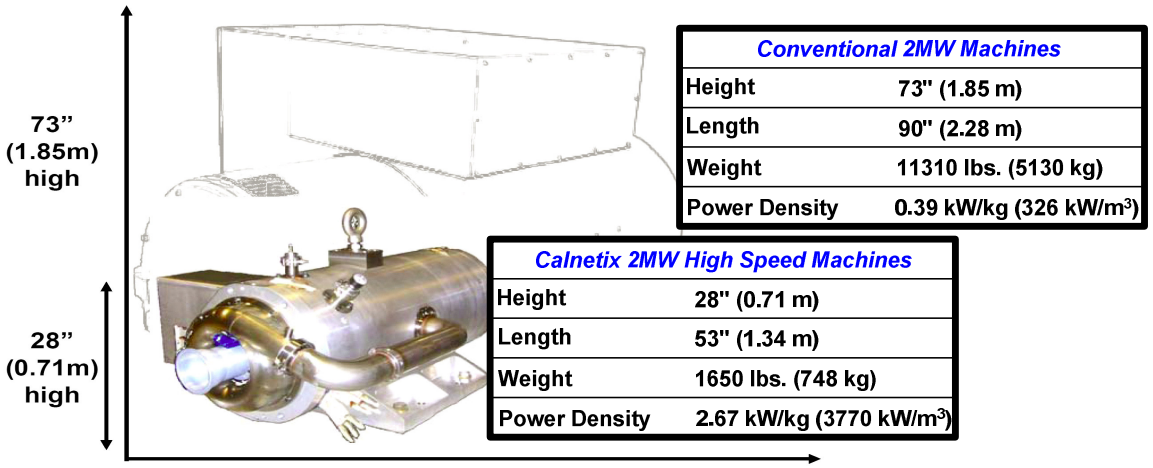


Figure 1-2 Comparison of high speed and low speed 2 MW machines [24].

1.4. Power Electronics

A high power output of the FESS depends not only on the generator, but also on its power electronics. Among other requirements, the latter must advance the power factor angle [36] and be capable of delivering the required power over a wide range of the rotor speeds. Depending on the system input and output types (DC or AC), as well as other factors, different types of power electronics can be used.

A topology that can be used with the proposed flywheel energy storage system is the three-phase IGBT-based PWM inverter/rectifier shown in Figure 1-1(a). In this topology, during the motoring operation when the flywheel is charged, the converter operates as an inverter. During the fast discharge of the flywheel the converter works as a controlled rectifier. It is crucial to maintain maximum efficiency during discharge of the flywheel by controlling the angle between the q-axis current component, torque component current, and the back-EMF at 0^{o}. Applying vector control results in maximum efficiency operation of the motor drive during charging and discharging operation [36].

At low speeds during discharge where the output voltage of the PM generator is low, a boost in voltage is needed. In this study, we propose to use a combination of the PM machine inductance and the converter and the DC link capacitor as a boost converter. In essence the machine windings are shorted out momentarily and therefore the magnetic energy is stored in the PM machine winding inductances. Later, this energy is released through the machine-side converter and is boosted by the DC bus capacitor.

1.5. External Inductor

As previously mentioned, the high-speed PM machines offer low inductances with low number of stator turns and large operating magnetic air gaps which is highly desired for withdrawal of a large amount of power from the machine. On the other hand, the low inductances result in high total harmonic distortion (THD) which increases the machine power losses and temperature. Therefore, using an external inductor in series with the machine in charging mode is necessary to reduce the THD and bring it within an accepted range. In the discharging mode, it is bypassed to take advantage of low inductances and allow the withdrawal of a large amount of current from the machine.

Sizing the external inductor is a critical task because several issues, price, size, weight, volume, ratings, losses, and control, are involved in the design procedure at the same time. It has been tried to design an external inductor such that it reduces the THD to an acceptable range as well as offers an acceptable weight, volume, price, loss, etc. In other words, a compromise between technical issues and price, as well as physical geometry is required.

1.6. Research Objectives

The main objective of this research is to identify an approach to the power electronics design and control such that it allows increasing power output of the permanent magnet generators at a rating of four times of the nominal power.

In this work, analysis, design, fabrication and control strategies of the power electronic activity point to one target which is withdrawal of kinetic energy stored in a high-speed flywheel through a permanent magnet synchronous machine (PMSM) at a rating of four times that of the PMSM nominal power. This goal is not achievable unless the power electronic and its control system establishes leading power factor at the PMSM terminals. Field Oriented Control (FOC) along with zeroing the d-axis current leads to this goal by achieving the maximum torque per amps control strategy.

Employing rather thick permanent magnets (PMs) in the fabrication of the PMSM results in small inductances of the machine that presents merits and demerits. It is desirable because it allows flows of a large current during discharge mode which leads to withdrawal of a huge power. On the other hand, small inductances cause high THD which results in torque pulsation, increased losses and etc. To overcome this problem, three single phase external inductors are designed. They are employed such that during charging mode it interfaces between the inverter and motor so that it reduces the THD and during the discharging mode where a small inductance is desired, it is bypassed.

Moreover, the inverter/rectifier is designed and fabricated such that it provides a high level of reliability, safety, and intelligent performance. Embedded sensors of the power electronic switches provide required signals for control as well as for protection

purposes. These protection features of the devices protect the inverter/rectifier under variety of faults.

These features facilitate a unique performance for the FESS which establishes the approach toward the main goal i.e. achieving four times the PMSM nominal power over a short discharge time.

1.7. Dissertation Outline

In order to conduct the stated research objectives, this dissertation is outlined as follows:

Section 1 covers state-of-the-art on high-speed FESS', applications, components, and their issues. In this section the advantages of high-speed FESS' is discussed and the main goals of this research are introduced.

In Section 2, the high-speed FESS shown in Figure 1-1(a) including a DC bus, a pulse width modulation (PWM) inverter/rectifier, an external inductor, a PMSM, and a high-speed flywheel is modeled in synchronous d-q reference frame (SDQRF).

In Section 3, according to the model developed in Section 2, direct current (DC) and small-signal alternative current (AC) analysis of the FESS is presented to obtain a great deal of information required for PWM inverter/rectifier design and development of the control strategies of the FESS.

Section 4 introduces two important factors affecting operation of the PMSM, namely power factor and armature reaction, in regenerative mode. The control strategy of the FESS is next outlined such that the FESS performance meets the main objectives of

this research. Finally, the FESS along with its control system is simulated to verify the desired performance.

In Section 5, according to the desired power rating, performance, and the simulation results, the inverter/rectifier power devices and the DC bus capacitor bank are selected and the inverter is designed and fabricated. This section covers all the features of the inverter/rectifier.

Section 6 covers the design of the external inductor. This inductor is considered to be a saturable inductor to perform as a linear inductor during the charging mode with a low current. In the discharging mode, it is saturated to allow the withdrawal of a large amount of current from the machine.

In Section 7, on the software side, the control algorithms are developed in "C" framework and run on TMS320F2812 DSP based controller on Code Composer Studio (CCS) V3.1. On the hardware side, an experimental test-bed is built to verify the control algorithms feasibility and performance.

Section 8 is a summary of the relevant conclusions and possible extensions that can be drawn from the work presented in this dissertation.

2. MODELING THE FESS IN SDQRF

To design the parts and outline the control strategy of a high-speed FESS, a comprehensive analysis of the FESS either in steady state or transient operation is considered necessary. As a result, establishing a comprehensive analytical model is needed for analysis purposes in an effort to avoid time consuming simulations managed by expensive packages, such as Simulink, PSIM, etc. So far, all the research works performed in this regard are focused on software applications [37-45] for analysis purposes and no analytical model has been presented. In this section, a comprehensive analytical model of the high-speed FESS in a synchronous d-q reference frame (SDQRF) is presented which results in a strong physical intuition of the complete system with good accuracy [46].

The FESS shown in Figure 2-1 including a DC bus, a three-phase PWM inverter/rectifier, an external inductor, a PMSM, and a high-speed flywheel is modeled in this section. As a result, the non-linear time varying differential equations of the FESS are transformed to a SDQRF attached to the PMSM rotor.

To develop the model, the original system is partitioned to several basic sub-circuits, the DC bus, the PWM inverter/rectifier, the external inductor, the PMSM, and the flywheel. Then, after modeling each part individually in SDQRF, they are all integrated to achieve the equivalent model of the whole system in SDQRF.

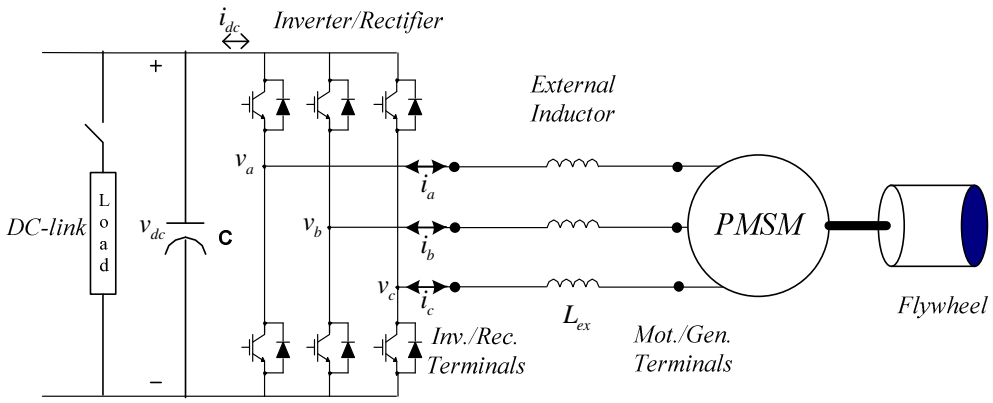


Figure 2-1 Flywheel energy storage system.

2.1. DC Bus

In motoring operation, the DC bus is modeled by a DC power supply in parallel with a capacitor and in generating mode, the DC power supply is replaced by a load such as a resistor and the DC bus current direction, as shown in Figure 2-2, is reversed. Notice that in the generating mode the DC bus voltage should be controlled. This is because it may experience some variations, and therefore different notations are used for the DC bus voltages, while the bus current may vary with time in both modes.

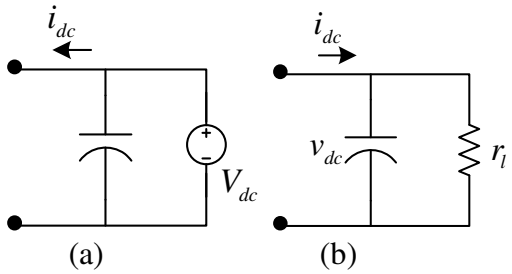


Figure 2-2 DC-bus model, (a) Charging mode, (b) Discharging mode.

2.2. PMSM

The PMSM is a PM machine with a sinusoidal back electro motive force (back-EMF). Figure 2-3 depicts a cross-section of the simplified three-phase surface mounted

PMSM [47]. The stator windings, as-as', bs-bs', and cs-cs' are shown as lumped windings for simplicity, but are actually distributed about the stator. Electrical rotor speed and position, ω_r and θ_r, are defined as P/2 times the corresponding mechanical quantities, where P is the number of poles. Based on the above motor definition, the voltage equation in the abc stationary reference frame is given by

$$v_{abcs} = R_s i_{abcs} + p\lambda_{abcs} \tag{2-1}$$

where

$$f_{abcs} = [f_{as}\ f_{bs}\ f_{cs}]^T, \quad f : v, i, \lambda \tag{2-2}$$

and $v, i,$ and λ stand for voltage, current, and flux-turn and the stator resistance matrix is given by

$$R_s = diag\left[r_s\ r_s\ r_s\right] \tag{2-3}$$

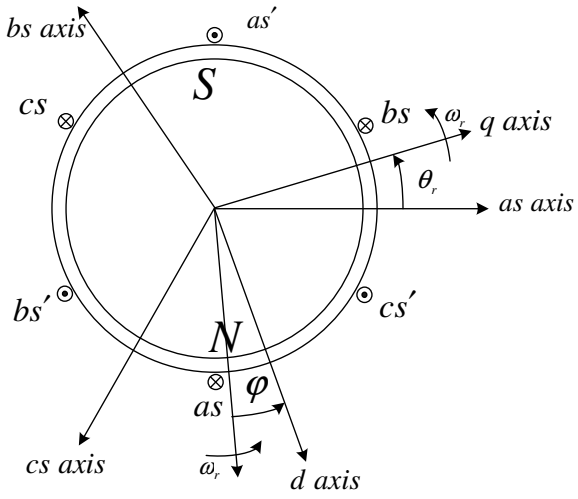


Figure 2-3 Cross-section of the PMSM.

The flux linkages equation can be expressed by

$$\lambda_{abcs} = L_s i_{abcs} + \Lambda_m \tag{2-4}$$

where

$$L_s = \begin{bmatrix} L_{ls}+L_A & -\frac{1}{2}L_A & -\frac{1}{2}L_A \\ -\frac{1}{2}L_A & L_{ls}+L_A & -\frac{1}{2}L_A \\ -\frac{1}{2}L_A & -\frac{1}{2}L_A & L_{ls}+L_A \end{bmatrix}, \quad \Lambda_m = \sqrt{2/3}\lambda_m \begin{bmatrix} \sin(\theta_r+\varphi_1) \\ \sin(\theta_r+\varphi_1-\frac{2\pi}{3}) \\ \sin(\theta_r+\varphi_1+\frac{2\pi}{3}) \end{bmatrix} \tag{2-5}$$

where L_s is the stator self inductance matrix, L_{ls} and L_A are the stator phase leakage and magnetizing inductances, respectively. Λ_m is PM flux linkages vector in which, $\sqrt{2/3}\lambda_m$ denotes the amplitude of the flux linkages established by the PM as viewed from the stator phase windings. In other words, the magnitude of $p(\Lambda_m)$ would be the magnitude of the open-circuit voltage induced in each stator phase winding (back-EMF). The constant phases of the flux linkages are arbitrary, as denoted by φ_1.

The electromagnetic torque may be written as

$$T_e = (\frac{P}{2})\left\{\sqrt{\frac{2}{3}}\lambda_m[(i_{as}-\frac{1}{2}i_{bs}-\frac{1}{2}i_{cs})\cos(\theta_r)-\frac{\sqrt{3}}{2}(i_{bs}-i_{cs})\sin(\theta_r)]\right\} \tag{2-6}$$

The above expression for torque is positive for motoring operation. The torque and speed are related by the electromechanical motion equation given by (2-7).

$$T_e = Jp\omega_m - f_m\omega_m \tag{2-7}$$

where J in kg.m^2 is the inertia of the rotor and the coupled flywheel. p is the derivative operator and the constant f_m is a damping coefficient associated with the rotational system of the machine and the coupled flywheel. It has the units N.m.s per radian of mechanical rotation. In the high-speed flywheel applications, the flywheel shaft is

suspended on magnetic bearings and operated in a vacuum. Thus the typical machine losses, friction and windage amount to almost zero, in other words, f_m effect can be ignored in this application.

The voltage and torque equations can be expressed in the rotor reference frame (synchronous reference frame) in order to transform the time-varying variables into steady state constants. The transformation of the three-phase variables in the stationary reference frame to the rotor reference frame is defined as

$$f_{qdos} = K_s f_{abcs} \tag{2-8}$$

where

$$K_s = \sqrt{2/3}\begin{bmatrix} \cos(\theta_r + \varphi) & \cos(\theta_r + \varphi - 2\pi/3) & \cos(\theta_r + \varphi + 2\pi/3) \\ \sin(\theta_r + \varphi) & \sin(\theta_r + \varphi - 2\pi/3) & \sin(\theta_r + \varphi + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{2-9}$$

$$f_{qdos} = [f_{qs}\ f_{ds}\ f_{os}]^T, \quad f : v, i, \lambda \tag{2-10}$$

The constant phases of the d-q axes are arbitrary, as denoted by φ. Multiplying (2.1) by K_s and carrying out the differentiation of the last term results in

$$v_{qdos} = r_s i_{qdos} + p\lambda_{qdos} - [pK_s]K_s^{-1}\lambda_{qdos} \tag{2-11}$$

where

$$[pK_s]K_s^{-1} = \begin{bmatrix} 0 & -\omega_r & 0 \\ \omega_r & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} = -\omega_r X,\ X = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2-12}$$

Then (2-11) reduces to

$$v_{qdos} = r_s i_{qdos} + p\lambda_{qdos} + \omega_r X \lambda_{qdos} \tag{2-13}$$

Similarly, if the flux linkages equation (2-4) is multiplied by K_s, it results in

$$\lambda_{qdos} = K_s L_s K_s^{-1} i_{qdos} + K_s \Lambda_m = L_{qdos} i_{qdos} + \Lambda_{qdos} \tag{2-14}$$

where

$$L_{qdos} = \begin{bmatrix} L_{ls} + \frac{3}{2} L_A & 0 & 0 \\ 0 & L_{ls} + \frac{3}{2} L_A & 0 \\ 0 & 0 & L_{ls} \end{bmatrix}, \quad \Lambda_{qdos} = \lambda_m \begin{bmatrix} -\sin(\varphi - \varphi_1) \\ \cos(\varphi - \varphi_1) \\ 0 \end{bmatrix} \tag{2-15}$$

The d- and q-axes magnetizing inductances are defined by

$$L_{md} = L_{mq} = \frac{3}{2} L_A \tag{2-16}$$

where the q- and d-axes self inductances are given by $L_{qs} = L_{ls} + L_{mq}$ and $L_{ds} = L_{ls} + L_{md}$, respectively. In a surface mount PM machine, these inductances are equal to L, then L_{qdos} is denoted as

$$L_{qdos} = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L_{ls} \end{bmatrix} \tag{2-17}$$

So the qdo transformed equations are defined as

$$v_{qdos} = R_s i_{qdos} + L_{qdos} p(i_{qdos}) + \omega_r X L_{qdos} i_{qdos} + \omega_r X \Lambda_{qdos} \tag{2-18}$$

These equations are derived for the three wire stator windings, so

$$i_a + i_b + i_c = 0 \Rightarrow i_{os} = 0 \Rightarrow v_{os} = 0 \tag{2-19}$$

and we will have

$$\begin{cases} v_{qs} = r_s i_{qs} + L p i_{qs} + \omega_r L i_{ds} + e_{qs} \\ v_{ds} = r_s i_{ds} + L p i_{ds} - \omega_r L i_{qs} + e_{ds} \\ v_{os} = 0 \end{cases} \tag{2-20}$$

where e_{qs} and e_{ds} are the back-EMF of the q- and d- axes respectively given by

$$\begin{aligned} e_{qs} &= \omega_r \lambda_m \cos(\varphi - \varphi_1) \\ e_{ds} &= \omega_r \lambda_m \sin(\varphi - \varphi_1) \end{aligned} \tag{2-21}$$

The electromagnetic torque can be written as

$$T_e = (\frac{P}{2})(\lambda_{ds} i_{qs} - \lambda_{qs} i_{ds}) \tag{2-22}$$

From (2-22), it can be seen that torque is related only to the d- and q-axes currents. Substituting λ_{ds} and λ_{qs} from (2-15) into (2-22), results in

$$T_e = T_{qs} + T_{ds} \tag{2-23}$$

where

$$\begin{aligned} T_{qs} &= \frac{P}{2} \lambda_m \cos(\varphi - \varphi_1) i_{qs} \\ T_{ds} &= \frac{P}{2} \lambda_m \sin(\varphi - \varphi_1) i_{ds} \end{aligned} \tag{2-24}$$

The equivalent circuit for the PMSM is illustrated in Figure 2-4. Notice that gyrator theory is employed to model the interaction between *qs* and *ds* circuitries. The gyrator shown in Figure 2-5 is a converter, unlike the transformer, characterized by a fundamental linking equation that links variables of different dimensions by the means of a gyration coefficient noted g [48]. The following equations are often given to describe a gyrator:

$$\begin{aligned} effort_2 &= g.flow_1 \\ effort_1 &= g.flow_2 \end{aligned} \tag{2-25}$$

In generating mode, the current directions are alone reversed. As a result in a similar manner the equivalent model can be achieved for the generating mode where the equations are summarized as follows:

$$\begin{cases} e_{qs} = r_s i_{qs} + Lpi_{qs} + \omega_r L i_{ds} + v_{qs} \\ e_{ds} = r_s i_{ds} + Lpi_{ds} - \omega_r L i_{qs} + v_{ds} \end{cases} \tag{2-26}$$

$$T_e = -(\frac{P}{2})\lambda_m(\cos(\varphi - \varphi_1))i_{qs} + \sin(\varphi - \varphi_1))i_{ds}) \tag{2-27}$$

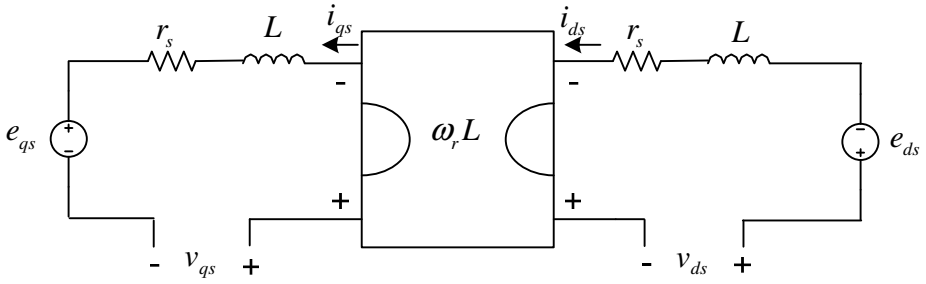


Figure 2-4 d-q model of PMSM in rotor reference frame.

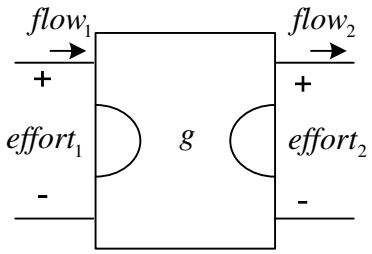


Figure 2-5 Gyrator model.

2.3. PWM Inverter/Rectifier

In this section, the three-phase controlled current PWM inverter shown in Figure 2-1 is to be transformed to an equivalent stationary circuit using d-q transformation. The switches operate in continuous conduction mode (CCM) and the switch pattern may be any PWM control, as long as its switching harmonics are not dominant.

The switching function denoted by S given by (2-28) is continuous sinusoidal in nature, assuming that the high-order switching harmonics do not contribute much to

distort the fundamental components. The constant phase of the switching function is arbitrary, as denoted by φ_2. The modulation index *m* is controlled externally.

By this transformation, the switch set becomes time-invariant transformers shown in Figure 2-6 [49]. The result of the transformation is given by (2-29)

$$v_{abcs} = SV_{dc}, \quad S = \sqrt{2/3}m \begin{bmatrix} \sin(\theta_r + \varphi_2) \\ \sin(\theta_r + \varphi_2 - \frac{2\pi}{3}) \\ \sin(\theta_r + \varphi_2 + \frac{2\pi}{3}) \end{bmatrix} \tag{2-28}$$

$$v_{qdos} = K_s V_{abcs} = K_s S V_{dc} = m V_{dc} \begin{bmatrix} -\sin(\varphi - \varphi_2) \\ \cos(\varphi - \varphi_2) \\ 0 \end{bmatrix} \tag{2-29}$$

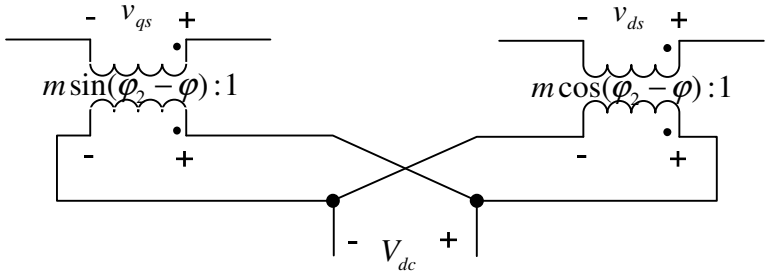


Figure 2-6 d-q model of the PWM inverter.

The difference between the inverter and rectifier models appears at the DC bus voltage. Since in the inverting operation, the DC bus is connected to a DC power supply, the DC bus voltage is constant while in the rectifying mode this voltage is controlled externally and can vary. As a result, the equivalent model for the rectifier is summarized by expressions (2-30) and (2-31), respectively.

$$v_{abcs} = Sv_{dc} \tag{2-30}$$

$$v_{qdos} = K_s v_{abcs} = K_s S v_{dc} = m v_{dc} \begin{bmatrix} -\sin(\varphi - \varphi_2) \\ \cos(\varphi - \varphi_2) \\ 0 \end{bmatrix} \tag{2-31}$$

Notice that from modeling point of view, the two equivalent models given by (2-29) and (2-31) don't appear very different, while in practice the external control and their behavior are completely different.

2.4. Flywheel

It is time to derive the equivalent circuit for the flywheel. To do so, one can use the differential equation describing the behavior of the flywheel system given by (2-32) to understand how to arrange the elements.

$$T_e = Jp\omega_m + f_m \omega_m \tag{2-32}$$

One can see that the motor torque tends to accelerate the flywheel and the frictions tend to slow it down. The equation is analogous to (2-33) which corresponds to the electrical representation of a torque (voltage) source moving the series combination of an inertia (inductor), and a friction (resistor) [48]. Therefore, according to the electrical analogy theory the mechanical side can be represented by an equivalent electric circuit as shown in Figure 2-7.

$$v = Lpi + ri \tag{2-33}$$

The voltage across the terminals of each element represents the torque actually applied to it and the current through each element represents the speed of the shaft. This circuit clearly illustrates the power dissipated due to the frictional losses and the energy

stored in the inertia and the mechanical power delivered by the motor. The voltage across the inertia represents J times the acceleration of the motor shaft.

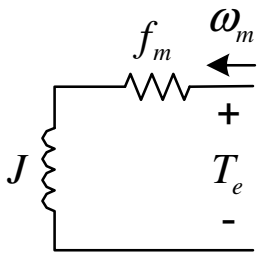


Figure 2-7 Electrical analogy representation of the flywheel.

2.5. External Inductor

The external inductor is assumed to be a three phase inductor in order to cover a general case study. Then in the case of using three single phase inductors, the model is easily modified by making zero the mutual inductances between the phases. Consider the coupled magnetic circuit shown in Figure 2-8. Although the permeance of the magnetic path of the center leg is higher than that of the outer two legs, it can be solely assumed making a first approximation that they are equal.

Based on the above explanation, the voltage equation in the abc stationary reference frame is given by

$$v_{abcs} = L_{ex} p i_{abcs} \tag{2-34}$$

where L_{ex} is an inductance matrix as

$$L_{ex} = \begin{bmatrix} L_s^{ex} & -L_m & -L_m \\ -L_m & L_s^{ex} & -L_m \\ -L_m & -L_m & L_s^{ex} \end{bmatrix} \tag{2-35}$$

where L_s^{ex} and $-L_m$ stand for phase self and mutual inductances, respectively.

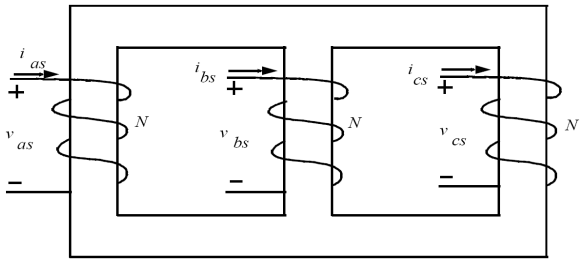


Figure 2-8 Three phase external inductor.

Multiplying (2-34) by K_s given by (2-9) and manipulating the equation in a similar manner as was done for the PMSM, yields [50]

$$v_{qdoex} = L_{qdoex}\, p(i_{qdoex}) + \omega_r X L_{qdoex} i_{qdoex} \tag{2-36}$$

where

$$L_{qdoex} = K_s L_{ex} K_s^{-1} = \begin{bmatrix} L_s^{ex} + L_m & 0 & 0 \\ 0 & L_s^{ex} + L_m & 0 \\ 0 & 0 & L_s^{ex} - 2L_m \end{bmatrix} \tag{2-37}$$

The d- and q- axes inductances are equal and denoted by L^{ex}

$$L^{ex} = L_s^{ex} + L_m \tag{2-38}$$

In the case of using three single phase inductors, L_m will be zero. The d-q model of the external inductor is expressed by (2-39) and is shown in Figure 2-9.

$$\begin{cases} v_{qex} = L^{ex} p i_{qex} + \omega_r L^{ex} i_{dex} \\ v_{dex} = L^{ex} p i_{dex} - \omega_r L^{ex} i_{qex} \\ v_{oex} = 0 \end{cases} \tag{2-39}$$

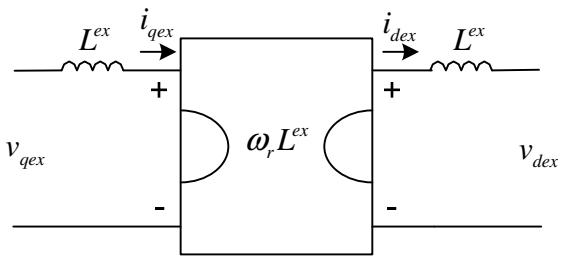


Figure 2-9 d-q model of the three phase external inductor.

2.6. d-q Model Reconstruction

To integrate the flywheel and the PMSM equivalent circuits, gyration theory is involved. The electro-mechanical conversion in the PMSM involves a gyration since it links a flow variable on one side to an effort variable on the other side. The electro-mechanical conversion in the PMSM is described by the following equations:

$$\begin{cases} T_{qs} = \dfrac{P}{2}\lambda_m \cos(\varphi - \varphi_1) i_{qs} \\ e_{qs} = \dfrac{P}{2}\lambda_m \cos(\varphi - \varphi_1) \end{cases} \tag{2-40}$$

$$\begin{cases} T_{ds} = \dfrac{P}{2}\lambda_m \sin(\varphi - \varphi_1) i_{ds} \\ e_{ds} = \dfrac{P}{2}\lambda_m s\,\mathrm{in}(\varphi - \varphi_1) \end{cases} \tag{2-41}$$

The gyration description is completed by the following mechanical equation:

$$T_e = T_{qs} + T_{ds} = Jp\omega_m + f_m\omega_m \tag{2-42}$$

In order to comply with the standard definition of a gyrator, that's sufficient to define the gyration coefficient for the q- and d- axes as follows:

$$\begin{aligned} g_{qs} &= \frac{P}{2}\lambda_m \cos(\varphi - \varphi_1) \\ g_{ds} &= \frac{P}{2}\lambda_m \sin(\varphi - \varphi_1) \end{aligned} \tag{2-43}$$

Figure 2-10 models the interaction between the PMSM and the flywheel.

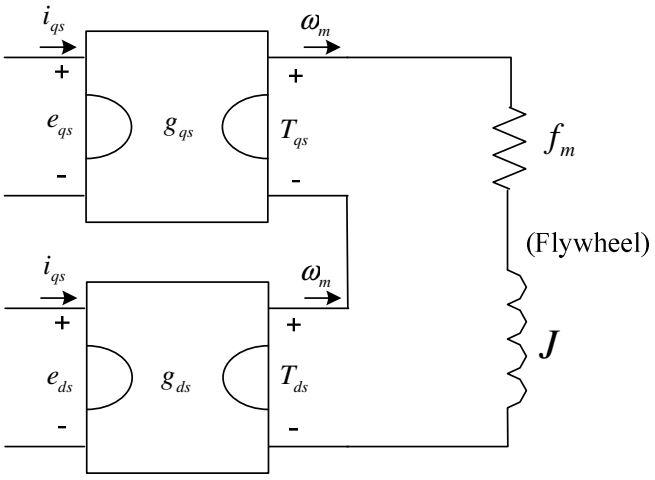


Figure 2-10 Integration of the PMSM with the flywheel.

As mentioned before, the gyration also happens inside the PMSM and the external inductor, denoted by a general term, $\omega_r XL_{qdo} i_{qdo}$, given by (2-18) and (2-36). In this case the gyration coefficients are given by (2-44) for the PMSM, and the external inductor, respectively. Since the external inductor is in series with the PMSM phase windings, obviously, these two sub-circuits can be integrated as shown in Figure 2-11, by defining a combined gyration factor as given by (2-44).

$$g = \omega_r L$$
$$g_{ex} = \omega_r L^{ex} \tag{2-44}$$

$$g_{tot} = \omega_r L_{tot} = \omega_r (L + L^{ex}) \tag{2-45}$$

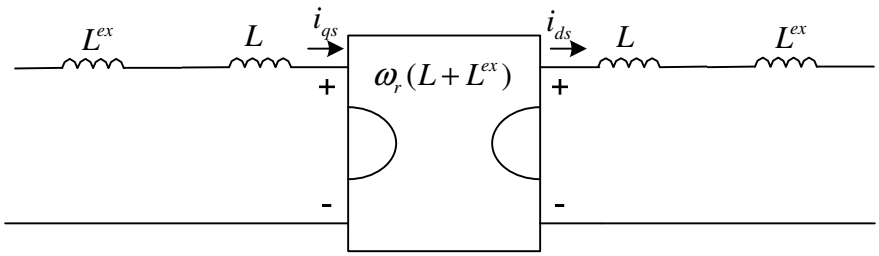


Figure 2-11 Integrating the external inductor with the PMSM.

The only thing is remaining is connection of the inverter/rectifier output terminals with the PMSM/external inductor terminals which can be easily obtained by substituting v_{qdos} given by (2-20) by similar term from (2-29).

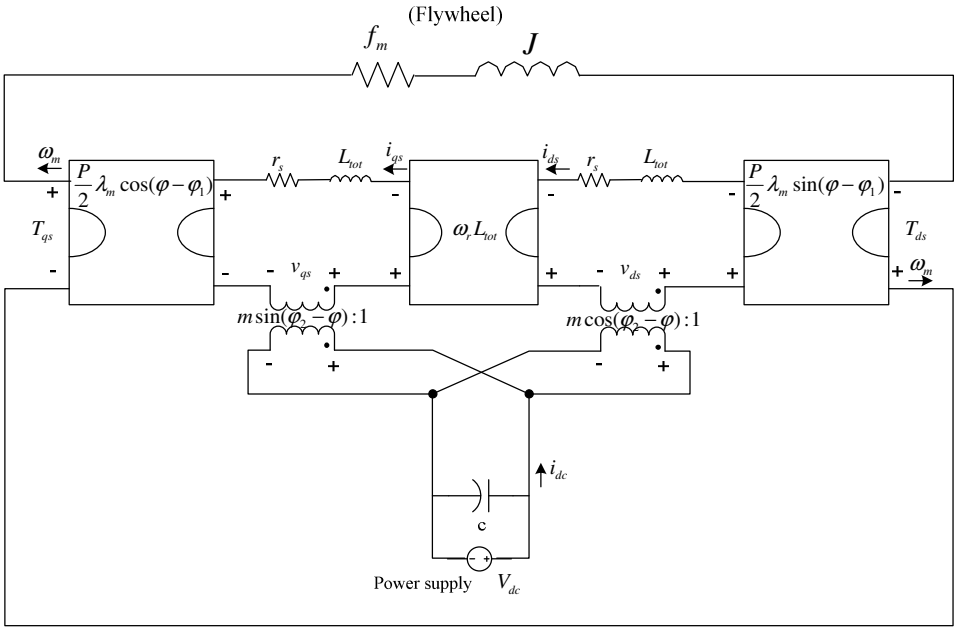
Integrating the d-q models of the DC bus, the PWM inverter/rectifier, the PMSM, and the flywheel, results in the equivalent circuits illustrated in Figure 2-12. Since the FESS status changes between the motoring (charging) and the generating (discharging) modes, the equivalent circuits are illustrated for both modes of operations.

2.7. Circuit Reduction

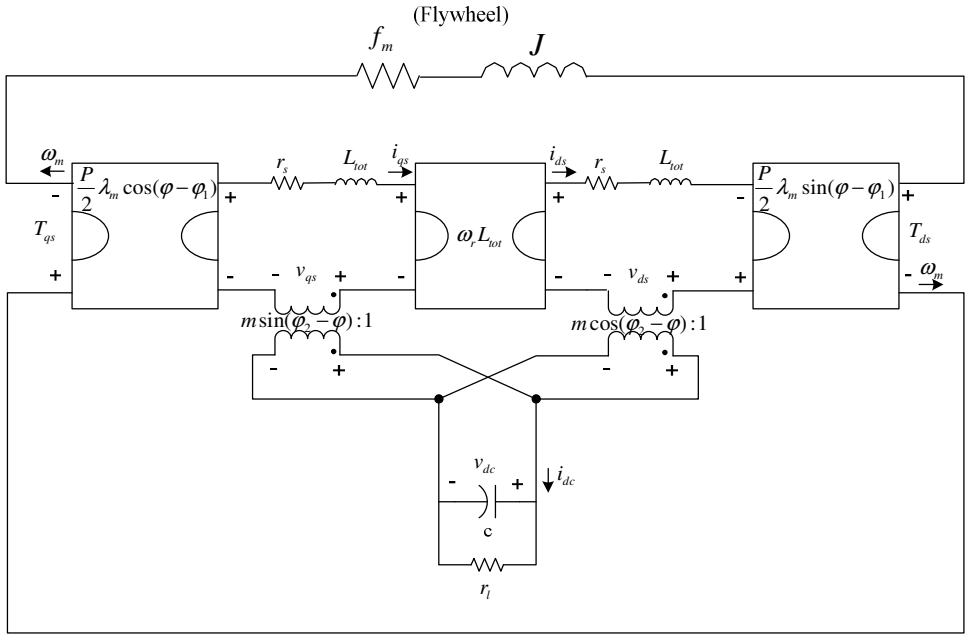
The stationary circuits shown in Figure 2-12 can be simplified noticing the fact that the phase of the d-q transform can be set to an arbitrary value. One possible selection is $\varphi = \varphi_1$ then the model reduces as shown in Figure 2-13. Another choice is $\varphi = \varphi_2$. Then one of the transformers vanishes, as shown in Figure 2-14.

It is evident that the first selection simplifies the original system much more than the previous one does. Moreover, the first selection coincides with the standard d-q reference frame definition in literature where the d-axis is aligned with the PM magnetic field axis. It is duly noted that there is no loss of generality throughout these procedures.

In the next section, a complete DC and small signal AC analysis of the FESS for both charging (motoring) and discharging (generating) modes of operations using the developed d-q model is presented. The analysis gives a good intuition of the FESS operation under any condition.

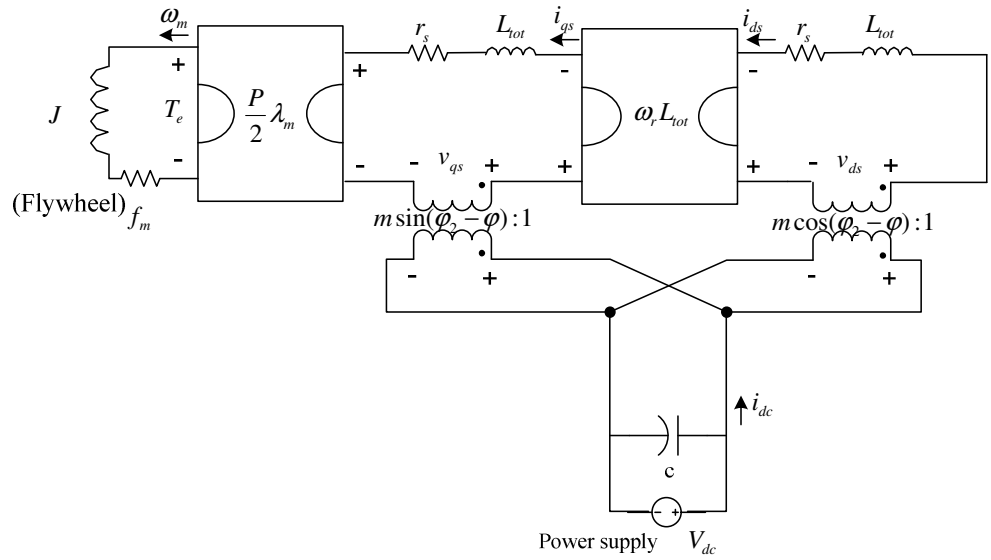


(a)

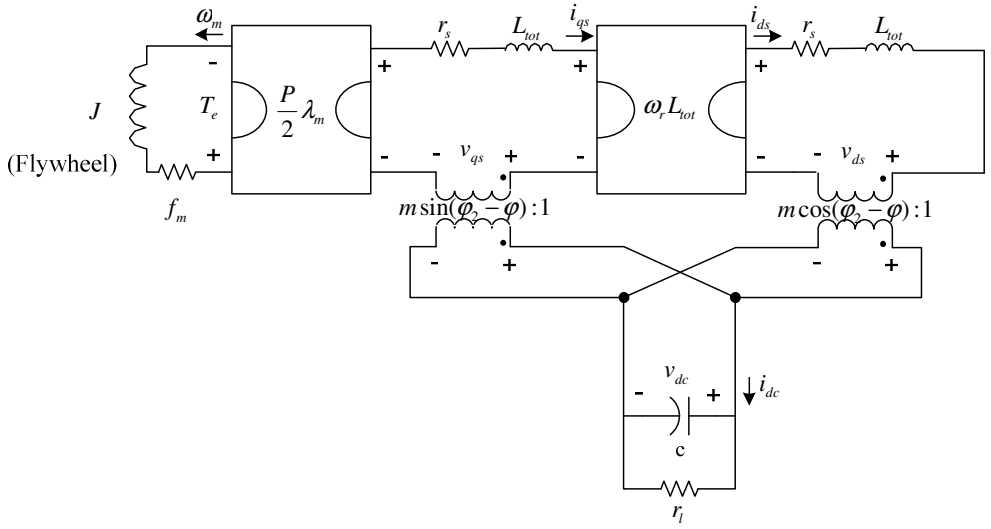


(b)

Figure 2-12 FESS model in d-q reference frame, a) Charging mode b) Discharging mode.

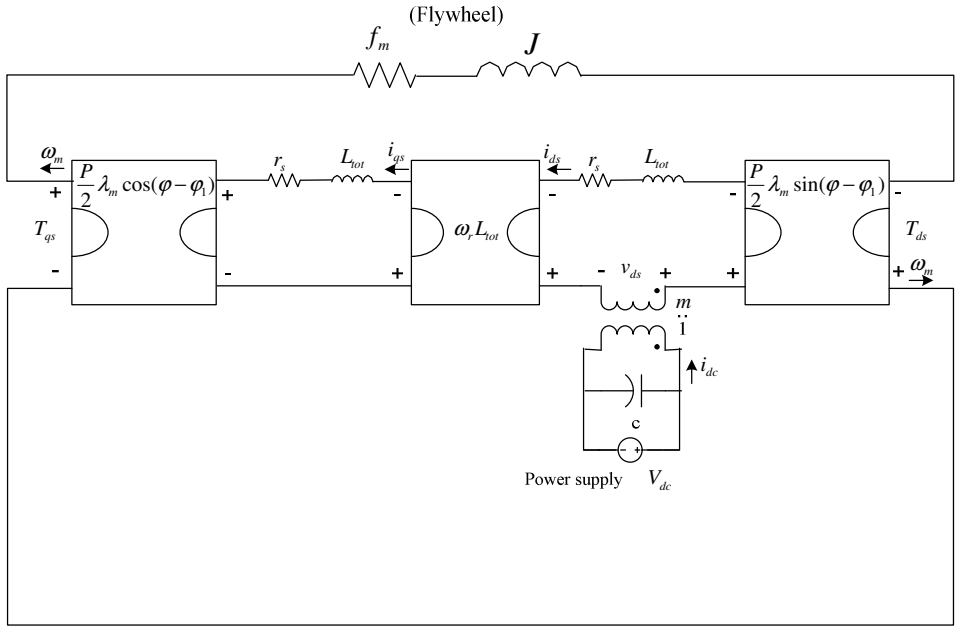


(a)

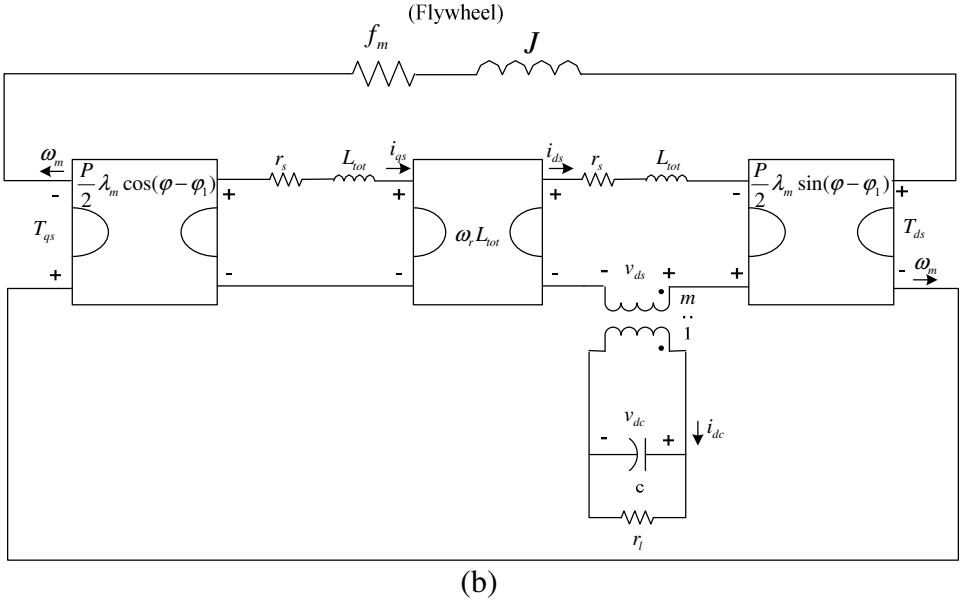


(b)

Figure 2-13 FESS reduced d-q model ($\varphi = \varphi_1$), a) Charging mode b) Discharging mode.



(a)



(b)

Figure 2-14 FESS reduced d-q model ($\varphi = \varphi_2$), a) Charging mode b) Discharging mode.

3. DC AND SMALL-SIGNAL AC ANALYSIS OF THE FESS

In this section the DC and small-signal AC analysis of the FESS is presented to achieve a great deal of information required for PWM inverter/rectifier design and development of the control strategies of the FESS under all conditions. Note that in the high-speed FESS application, the flywheel shaft is suspended on magnetic bearings and operated in a vacuum. Thus the typical machine losses, friction and windage, are almost zero, in other words, f_m influence can be ignored in this application. So in the DC and small-signal AC analysis performed henceforth , it is assumed that f_m is zero.

3.1. Charging Mode

The FESS d-q model was derived in the previous section, for convenience the d-q model for the charging mode is illustrated again in Figure 3-1. Writing KVL equations for the loops I, II, and III, the nonlinear state space equations representing the behavior of the FESS are achieved.

$$\begin{cases} pi_{qs} = -\dfrac{r_s}{L_{tot}} i_{qs} - \omega_r i_{ds} - \dfrac{\lambda_m}{L_{tot}} \omega_r + \dfrac{m}{L_{tot}} \sin(\varphi_0) V_{dc} \\ pi_{ds} = \omega_r i_{qs} - \dfrac{r_s}{L_{tot}} i_{ds} + \dfrac{m}{L_{tot}} \cos(\varphi_0) V_{dc} \\ p\omega_r = (\dfrac{P}{2})^2 \dfrac{\lambda_m}{J} i_{qs} \end{cases} \tag{3-1}$$

where $[i_{qs}, i_{ds}, \omega_r]^T$ and $[m, \varphi_0]^T$ denote the states and control input vectors of the system. Note that in Figure 3-1, the transformers turn ratios are denoted as a function of m and $\varphi_0 = \varphi_2 - \varphi$ for simplicity.

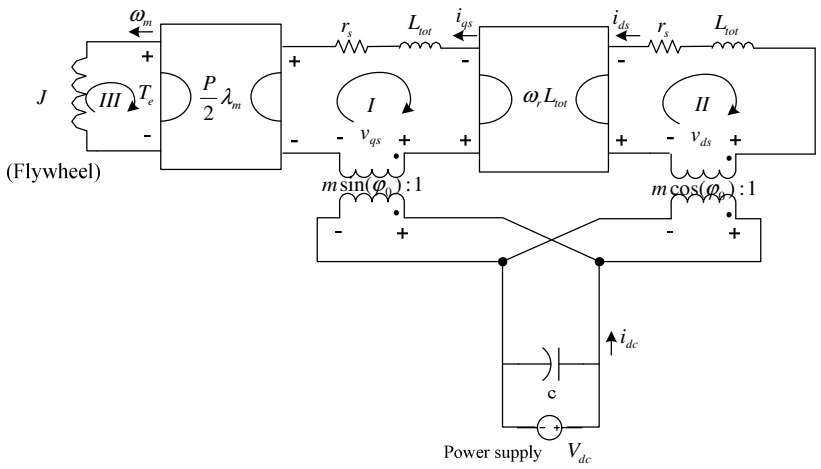


Figure 3-1 FESS d-q model during the charging mode ($\varphi_0 = \varphi_2 - \varphi$).

This is a nonlinear set of differential equations, and hence the next step is to perturb and linearize them to construct DC and small-signal AC equations. In the perturbation and linearization steps, it is assumed that an averaged voltage, current, or speed consists of a constant (DC) component and a small ac variation around the DC component. Similarly, we assume that the inverter input control signals, m and φ_0 can be expressed as DC values plus small AC variations given by (3-2).

$$\begin{cases} i_{qs} = I_{qs} + \hat{i}_{qs} \\ i_{ds} = I_{ds} + \hat{i}_{ds} \\ \omega_r = \omega_r + \hat{\omega}_r \end{cases}, and \begin{cases} m = M + \hat{m} \\ \varphi_0 = \phi_0 + \hat{\varphi}_0 \end{cases} \tag{3-2}$$

where it is assumed that

$$\begin{cases} I_{qs} \gg \hat{i}_{qs} \\ I_{ds} \gg \hat{i}_{ds} \\ \omega_r \gg \hat{\omega}_r \end{cases}, and \begin{cases} M \gg \hat{m} \\ \phi_0 \gg \hat{\varphi}_0 \end{cases} \tag{3-3}$$

Ignoring the power loss, the power consumption by the FESS during the charging mode is due to the acceleration of the flywheel, $p\omega_r$. In other words, if the rotational

speed of the flywheel is constant the FESS doesn't draw any power from the DC power supply. Because of this, in the next analysis it is assumed that the acceleration is constant while the rotational speed of the flywheel is not.

Substituting (3-2) into (3-1) results in the large-signal averaged set of equations given by (3-4).

$$\begin{cases} p(I_{qs}+\hat{i}_{qs}) = -\dfrac{r_s}{L_{tot}}(I_{qs}+\hat{i}_{qs}) - (\omega_r+\hat{\omega}_r)(I_{ds}+\hat{i}_{ds}) - \dfrac{\lambda_m}{L_{tot}}(\omega_r+\hat{\omega}_r) + V_{dc}\dfrac{(M+\hat{m})}{L_{tot}}\sin(\phi_0+\hat{\varphi}_0) \\ p(I_{ds}+\hat{i}_{ds}) = (\omega_r+\hat{\omega}_r)(I_{qs}+\hat{i}_{qs}) - \dfrac{r_s}{L_{tot}}(I_{ds}+\hat{i}_{ds}) + V_{dc}\dfrac{(M+\hat{m})}{L_{tot}}\cos(\phi_0+\hat{\varphi}_0) \\ p(\omega_r+\hat{\omega}_r) = (\dfrac{P}{2})^2\dfrac{\lambda_m}{J}(I_{qs}+\hat{i}_{qs}) \end{cases} \tag{3-4}$$

Upon multiplying this expression out and collecting terms, we obtain the complete set of differential equations given by (3-5) which is exactly equal to (3-4). These equations contain three types of terms [51]. The DC terms do not contain any time-varying quantities. The first-order AC terms are linear functions of the AC variations in the circuit, while the second-order AC terms are functions of the respective of the AC variations. If the small-signal assumptions of (3-3) are satisfied, the second-order terms are much smaller in magnitude than the first-order terms, and hence can be neglected.

$$
\begin{cases}
L_{tot}\,p(I_{qs}+\hat{i}_{qs}) = \left\{ \begin{array}{l} \underbrace{-r_s I_{qs} - \omega_r L_{tot} I_{ds} - \lambda_m \omega_r + V_{dc} M \sin(\phi_0)}_{DC\ terms} \\ \underbrace{-r_s \hat{i}_{qs} - \omega_r L_{tot} \hat{i}_{ds} - I_{ds} L_{tot} \hat{\omega}_r - \lambda_m \hat{\omega}_r + V_{dc} M \cos(\phi_0)\hat{\varphi}_0 + V_{dc} \sin(\phi_0)\hat{m}}_{small-signal\ AC\ terms} \\ \underbrace{-\hat{\omega}_r L_{tot} \hat{i}_{ds} + V_{dc} \cos(\phi_0)\hat{m}\hat{\varphi}_0}_{2-order\ nonlinear\ terms} \end{array} \right\} \\
L_{tot}\,p(I_{ds}+\hat{i}_{ds}) = \left\{ \begin{array}{l} \underbrace{\omega_r L_{tot} I_{qs} - r_s I_{ds} + V_{dc} M \cos(\phi_0)}_{DC\ terms} \\ \underbrace{+\omega_r L_{tot} \hat{i}_{qs} - r_s \hat{i}_{ds} + I_{qs} L_{tot} \hat{\omega}_r - V_{dc} M \sin(\phi_0)\hat{\varphi}_0 + V_{dc} \cos(\phi_0)\hat{m}}_{small-signal\ AC\ terms} \\ \underbrace{+\hat{\omega}_r L_{tot} \hat{i}_{qs} - V_{dc} \sin(\phi_0)\hat{m}\hat{\varphi}_0}_{2-order\ nonlinear\ terms} \end{array} \right\} \\
Jp(\omega_r + \hat{\omega}_r) = \left\{ \underbrace{(\frac{P}{2})^2 \lambda_m I_{qs}}_{DC\ terms} \quad \underbrace{+(\frac{P}{2})^2 \lambda_m \hat{i}_{qs}}_{small-signal\ AC\ terms} \right\}
\end{cases}
\tag{3-5}
$$

The equations of the DC values, are collected below:

$$
\begin{cases}
L_{tot}\,pI_{qs} = 0 = -r_s I_{qs} - \omega_r L_{tot} I_{ds} - \lambda_m \omega_r + V_{dc} M \sin(\phi_0) \\
L_{tot}\,pI_{ds} = 0 = \omega_r L_{tot} I_{qs} - r_s I_{ds} + V_{dc} M \cos(\phi_0) \\
Jp\omega_r = (P/2)^2 \lambda_m I_{qs}
\end{cases}
\tag{3-6}
$$

The DC equivalent circuit corresponding to the set of equations given by (3-6) is shown in Figure 3-2.

The small-signal AC equations are summarized below.

$$
\begin{cases}
L_{tot}\,p\hat{i}_{qs} = -r_s \hat{i}_{qs} - \omega_r L_{tot} \hat{i}_{ds} - I_{ds} L_{tot} \hat{\omega}_r - \lambda_m \hat{\omega}_r + V_{dc} M \cos(\phi_0)\hat{\varphi}_0 + V_{dc} \sin(\phi_0)\hat{m} \\
L_{tot}\,p\hat{i}_{ds} = \omega_r L_{tot} \hat{i}_{qs} - r_s \hat{i}_{ds} + I_{qs} L_{tot} \hat{\omega}_r - V_{dc} M \sin(\phi_0)\hat{\varphi}_0 + V_{dc} \cos(\phi_0)\hat{m} \\
Jp\hat{\omega}_r = (P/2)^2 \lambda_m \hat{i}_{qs}
\end{cases}
\tag{3-7}
$$

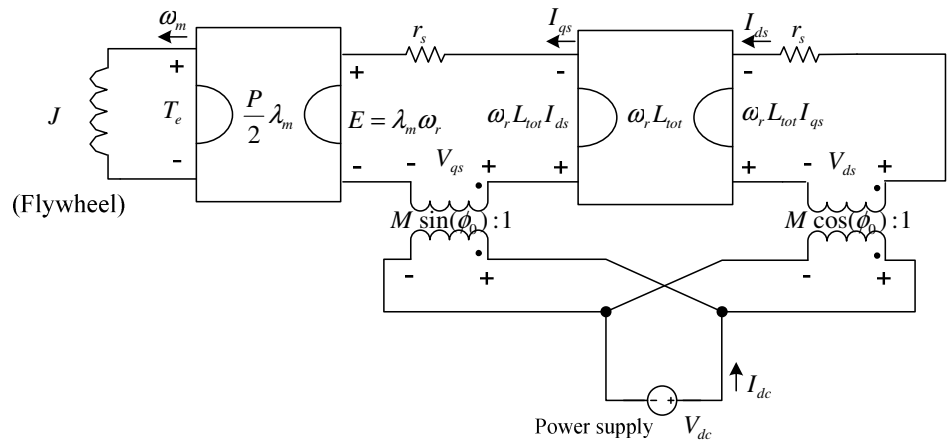


Figure 3-2 FESS DC model during the charging mode.

The final step is to construct an equivalent circuit that corresponds to these equations. The small-signal AC circuit is drawn as shown in Figure 3-3(a). It is necessary to obtain a simplified circuit. Figure 3-3(b) shows this circuit where the sources are integrated. The voltage sources are:

$$\begin{aligned} v_1 &= -V_{dc} \sin(\phi_0)\hat{m} - V_{dc} M \cos(\phi_0)\hat{\varphi}_0 \\ v_2 &= -V_{dc} \cos(\phi_0)\hat{m} + V_{dc} M \sin(\phi_0)\hat{\varphi}_0 \end{aligned} \tag{3-8}$$

3.1.1. DC Analysis

The DC equivalent circuit of the FESS during the charging mode was shown in Figure 3-2. Comparing with the discharging mode, the charging mode is run in a longer period of time and with a lower phase current. So, the drop voltage across the PMSM winding resistor r_s, is very small as compared with the DC bus voltage. So in the DC analysis r_s can be ignored as shown in Figure 3-4. Writing KVL equations for the loops I, II, and III, the DC equations representing the behavior of the FESS is achieved.

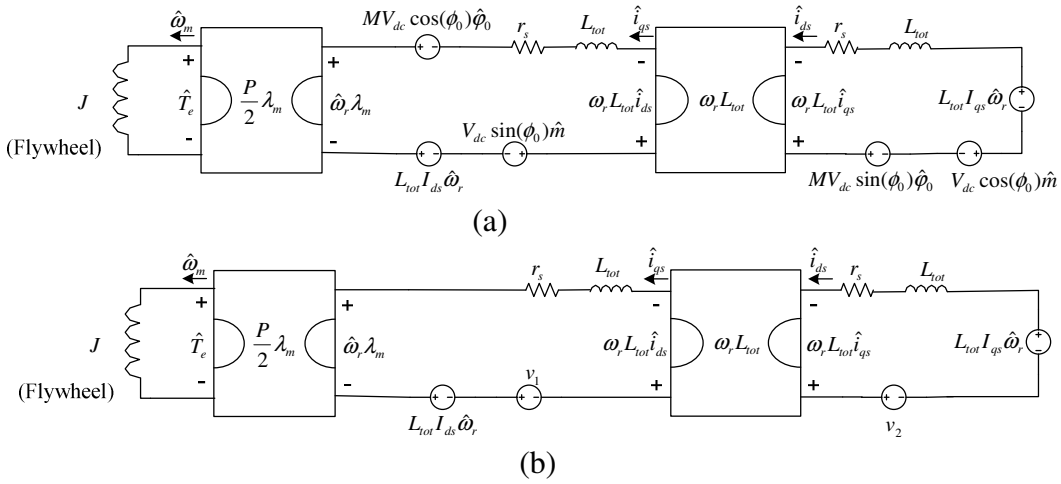


Figure 3-3 FESS small-signal AC mode during the charging mode,
a) Complete model, b) Simplified model.

$$\begin{cases} -\omega_r L_{tot} I_{ds} - \lambda_m \omega_r = -V_{dc} M \sin(\phi_0) \\ \omega_r L_{tot} I_{qs} = -V_{dc} M \cos(\phi_0) \\ (P/2)^2 \lambda_m I_{qs} - Jp\omega_r = 0 \end{cases} \tag{3-9}$$

It is found from (3-9) that

$$I_{qs} = (\frac{2}{P})^2 \frac{J}{\lambda_m} p\omega_r \tag{3-10}$$

$$I_{ds} = -(\frac{2}{P})^2 \frac{J}{\lambda_m} p\omega_r \tan(\phi_0) - \frac{\lambda_m}{L_{tot}} \tag{3-11}$$

$$\omega_r = -(\frac{P}{2})^2 \frac{\lambda_m V_{dc} M \cos(\phi_0)}{L_{tot} Jp\omega_r} \tag{3-12}$$

The PWM inverter output real power P_{inv}^{out} and reactive power Q_{inv}^{out} are found to be [52]

$$P_{inv}^{out} = V_{qs} I_{qs} + V_{ds} I_{ds} \tag{3-13}$$

$$Q_{inv}^{out} = V_{qs} I_{ds} - V_{ds} I_{qs} \tag{3-14}$$

where

$$V_{qs} = \lambda_m \omega_r + \omega_r L_{tot} I_{ds}$$
$$V_{ds} = -\omega_r L_{tot} I_{qs} \tag{3-15}$$

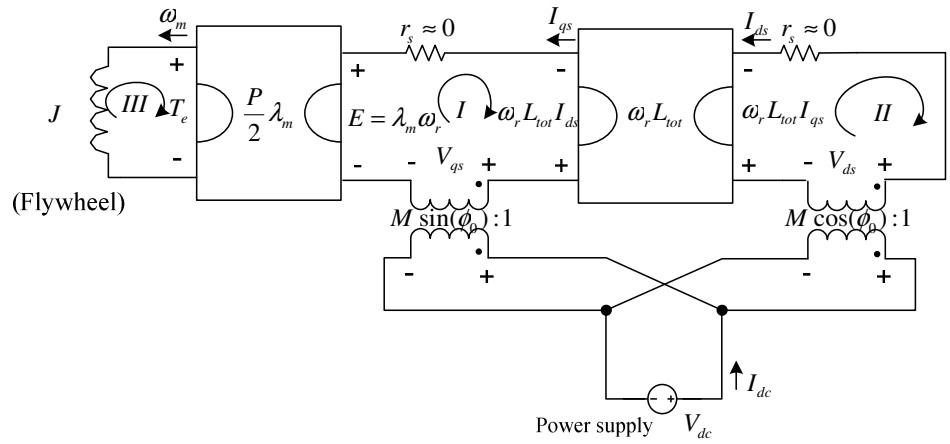


Figure 3-4 FESS DC model during the charging mode.

Substituting (3-15) into (3-13) and (3-14) results in

$$P_{inv}^{out} = \lambda_m \omega_r I_{qs} \tag{3-16}$$

$$Q_{inv}^{out} = \lambda_m \omega_r I_{ds} + \omega_r L_{tot} I_{ds}^2 + \omega_r L_{tot} I_{qs}^2 \tag{3-17}$$

where $I_{qs}, I_{ds}, and\ \omega_r$ are given by (3-10) to (3-12). Then the power factor PF is expressed as

$$PF = \frac{P_{inv}^{out}}{(P_{inv}^{out\,2} + Q_{inv}^{out\,2})^{1/2}} \tag{3-18}$$

In the case that the PMSM is not run in a field weakening mode, i.e. I_{ds} is controlled to remain zero, the DC analysis of the FESS is simplified very significantly. To keep $I_{ds} = 0$, ϕ_0 should be controlled such that (3-19) holds. The DC variables of the FESS for zero and non-zero I_{ds} are summarized in Table 3-1.

$$I_{ds} = 0 \Rightarrow \tan(\phi_0) = -(\frac{P}{2})^2 \frac{\lambda_m^2}{L_{tot} Jp\omega_r} \tag{3-19}$$

Table 3-1 Analytical model of the FESS for charging mode.

Var.	$I_{ds} \neq 0$	$I_{ds} = 0$
I_{qs}	$(2/P)^2 Jp\omega_r / \lambda_m$	
I_{ds}	$-(2/P)^2 Jp(\omega_r)\tan(\phi_0)/\lambda_m - \lambda_m / L_{tot}$	0
ω_r	$-(P/2)^2 \lambda_m V_{dc} M \cos(\phi_0) / L_{tot} Jp(\omega_r)$	
V_{qs}	$\lambda_m \omega_r + \omega_r L_{tot} I_{ds}$	$\lambda_m \omega_r$
V_{ds}	$-\omega_r L_{tot} I_{qs}$	
P_{inv}^{out}	$\lambda_m \omega_r I_{qs}$	
Q_{inv}^{out}	$\lambda_m \omega_r I_{ds} + \omega_r L_{tot} I_{ds}^2 + \omega_r L_{tot} I_{qs}^2$	$\omega_r L_{tot} I_{qs}^2$
PF	$P_{inv}^{out} / (P_{inv}^{out2} + Q_{inv}^{out2})^{1/2}$	
ϕ_0	N/A	$\tan^{-1}(-(P/2)^2 \lambda_m^2 / L_{tot} Jp\omega_r) + \pi$
M	N/A	$\lambda_m \omega_r / \sin(\phi_0) V_{dc}$

3.1.2. Small-Signal AC Analysis

Based on (3-7), the small signal model of the FESS in charging mode can be presented as state space differential equations given by (3-20).

$$\begin{bmatrix} \dot{\hat{i}}_{qs} \\ \dot{\hat{i}}_{ds} \\ \dot{\hat{\omega}}_r \end{bmatrix} = \begin{bmatrix} \frac{-r_s}{L_{tot}} & -\omega_r & -I_{ds}\frac{-\lambda_m}{L_{tot}} \\ \omega_r & \frac{-r_s}{L_{tot}} & I_{qs} \\ \frac{(P/2)^2 \lambda_m}{J} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{qs} \\ \hat{i}_{ds} \\ \hat{\omega}_r \end{bmatrix} + \begin{bmatrix} \frac{V_{dc} M \cos(\phi_0)}{L_{tot}} & \frac{V_{dc}\sin(\phi_0)}{L_{tot}} \\ \frac{-V_{dc} M \sin(\phi_0)}{L_{tot}} & \frac{V_{dc}\cos(\phi_0)}{L_{tot}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{\varphi}_0 \\ \hat{m} \end{bmatrix} \tag{3-20}$$

Now we can analyze the small-signal AC model of the system at any operating point. It is possible to derive the small-signal AC model at any speed. Since the starting

and ending speeds are the most critical operating points in which the mode of operation is changed, these points are of higher interest, however, there is no loss of generality throughout the speed range.

3.2. Discharging Mode

The FESS d-q model was derived in the previous section, for convenience the d-q model for the discharging mode is illustrated here again in Figure 3-5.Writing KVL equations for the loops I, II, and III and KCL equation for the node I, the nonlinear state space equations representing the behavior of the FESS are obtained.

$$\begin{cases} pi_{qs} = -\dfrac{r_s}{L_{tot}} i_{qs} - \omega_r i_{ds} + \dfrac{\lambda_m}{L_{tot}} \omega_r - \dfrac{m}{L_{tot}} \sin(\varphi_0) v_{dc} \\ pi_{ds} = \omega_r i_{qs} - \dfrac{r_s}{L_{tot}} i_{ds} - \dfrac{m}{L_{tot}} \cos(\varphi_0) v_{dc} \\ pv_{dc} = \dfrac{m \sin(\varphi_0)}{c} i_{qs} + \dfrac{m \cos(\varphi_0)}{c} i_{ds} - \dfrac{1}{r_l c} v_{dc} \\ p\omega_r = -(\dfrac{P}{2})^2 \dfrac{\lambda_m}{J} i_{qs} \end{cases} \tag{3-21}$$

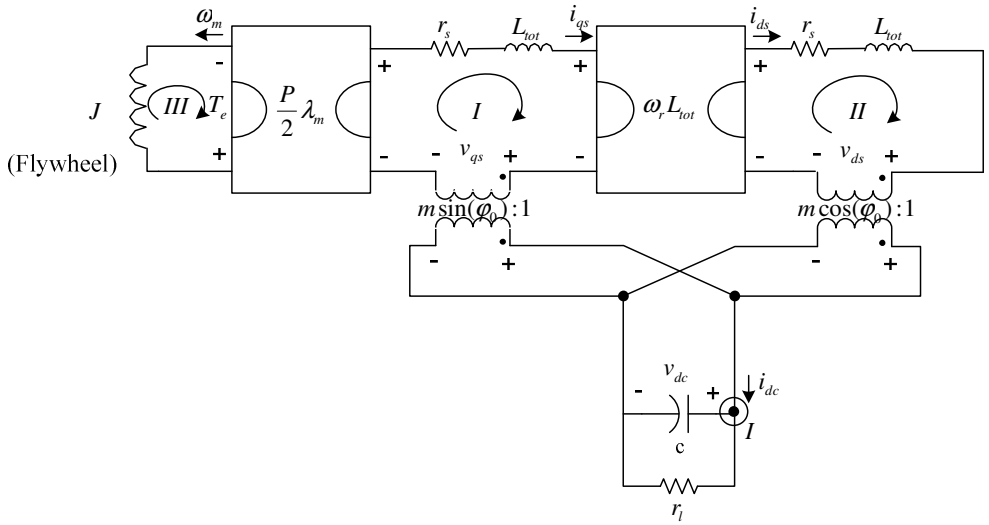


Figure 3-5 FESS d-q mode during the discharging mode, $(\varphi_0 = \varphi_2 - \varphi)$.

where $[i_{qs}, i_{ds}, v_{dc}, \omega_r]^T$ and $[m, \varphi_0]^T$ denote the states and control inputs vectors of the system. Note that in Figure 3-5, the transformers turn ratios are denoted as a function of $m, and\ \varphi_0 = \varphi_2 - \varphi$ for simplicity.

This is a nonlinear set of differential equations, and hence the next step is to perturb and linearize it, to construct DC and small-signal AC equations. In the perturbation and linearization step, it is assumed that an averaged voltage, current, or speed consists of a constant (DC) component and a small AC variation around the DC component. Similarly, we assume that the rectifier input control signals, m and φ_0 can be expressed as DC values plus small AC variations given by (3-22).

$$\begin{cases} i_{qs} = I_{qs} + \hat{i}_{qs} \\ i_{ds} = I_{ds} + \hat{i}_{ds} \\ v_{dc} = V_{dc} + \hat{v}_{dc} \\ \omega_r = \omega_r + \hat{\omega}_r \end{cases}, and \begin{cases} m = M + \hat{m} \\ \varphi_0 = \phi_0 + \hat{\varphi}_0 \end{cases} \tag{3-22}$$

where it is assumed that

$$\begin{cases} I_{qs} \gg \hat{i}_{qs} \\ I_{ds} \gg \hat{i}_{ds} \\ V_{dc} \gg \hat{v}_{dc} \\ \omega_r \gg \hat{\omega}_r \end{cases}, and \begin{cases} M \gg \hat{m} \\ \phi_0 \gg \hat{\varphi}_0 \end{cases} \tag{3-23}$$

Note that, during the discharging mode the real source power of the FESS is the deceleration of the flywheel $p\omega_r$. In other words, if the rotational speed of the flywheel is constant the FESS doesn't experience any regenerative mode. Because of that, in the up coming analysis it is assumed that the deceleration is constant but not the rotational speed of the flywheel. Substituting (3-22) into (3-21) results in large-signal averaged set of equations given by (3-24).

$$\begin{cases} p(I_{qs}+\hat{i}_{qs}) = -\dfrac{r_s}{L_{tot}}(I_{qs}+\hat{i}_{qs}) - (\omega_r+\hat{\omega}_r)(I_{ds}+\hat{i}_{ds}) + \dfrac{\lambda_m}{L_{tot}}(\omega_r+\hat{\omega}_r) - \dfrac{(M+\hat{m})}{L_{tot}}\sin(\phi_0+\hat{\varphi}_0)(V_{dc}+\hat{v}_{dc}) \\ p(I_{ds}+\hat{i}_{ds}) = (\omega_r+\hat{\omega}_r)(I_{qs}+\hat{i}_{qs}) - \dfrac{r_s}{L_{tot}}(I_{ds}+\hat{i}_{ds}) - \dfrac{(M+\hat{m})}{L_{tot}}\cos(\phi_0+\hat{\varphi}_0)(V_{dc}+\hat{v}_{dc}) \\ p(V_{dc}+\hat{v}_{dc}) = \dfrac{(M+\hat{m})\sin(\phi_0+\hat{\varphi}_0)}{c}(I_{qs}+\hat{i}_{qs}) + \dfrac{(M+\hat{m})\cos(\phi_0+\hat{\varphi}_0)}{c}(I_{ds}+\hat{i}_{ds}) - \dfrac{1}{r_l c}(V_{dc}+\hat{v}_{dc}) \\ p(\omega_r+\hat{\omega}_r) = -(\dfrac{P}{2})^2\dfrac{\lambda_m}{J}(I_{qs}+\hat{i}_{qs}) \end{cases} \tag{3-24}$$

Upon multiplying this expression and collecting terms, we obtain the complete set of differential equations given by (3-25) which is exactly equal to (3-24). These equations contain three types of terms [51]. The DC terms contain no time-varying quantities. The first-order AC terms are linear functions of the AC variations in the circuit, while the second- and third-order AC terms are functions of the products of the AC variations. If the small-signal assumptions of (3-23) are satisfied, the second- and third-order terms are much smaller in magnitude than the first-order terms, and hence can be neglected.

$$
\begin{cases}
L_{tot}\,p(I_{qs}+\hat{i}_{qs}) = \left\{ \begin{array}{l}
\underbrace{-r_s I_{qs} - \omega_r L_{tot} I_{ds} + \lambda_m \omega_r - V_{dc} M \sin(\phi_0)}_{DC\ terms} \\
\underbrace{-r_s \hat{i}_{qs} - \omega_r L_{tot} \hat{i}_{ds} - I_{ds} L_{tot} \hat{\omega}_r + \lambda_m \hat{\omega}_r - V_{dc} M \cos(\phi_0)\hat{\varphi}_0 - M \sin(\phi_0)\hat{v}_{ds} - V_{dc} \sin(\phi_0)\hat{m}}_{small-signal\ AC\ terms} \\
\underbrace{-\hat{\omega}_r L_{tot} \hat{i}_{ds} - M \cos(\phi_0)\hat{v}_{ds}\hat{\varphi}_0 - V_{dc} \cos(\phi_0)\hat{m}\hat{\varphi}_0 - \sin(\phi_0)\hat{v}_{ds}\hat{m} - \cos(\phi_0)\hat{v}_{ds}\hat{m}\hat{\varphi}_0}_{2-\ and\ 3-order\ nonlinear\ terms}
\end{array} \right\} \\
L_{tot}\,p(I_{ds}+\hat{i}_{ds}) = \left\{ \begin{array}{l}
\underbrace{\omega_r L_{tot} I_{qs} - r_s I_{ds} - V_{dc} M \cos(\phi_0)}_{DC\ terms} \\
\underbrace{+\omega_r L_{tot} \hat{i}_{qs} - r_s \hat{i}_{ds} + I_{qs} L_{tot} \hat{\omega}_r + V_{dc} M \sin(\phi_0)\hat{\varphi}_0 - M \cos(\phi_0)\hat{v}_{dc} - V_{dc} \cos(\phi_0)\hat{m}}_{small-signal\ AC\ terms} \\
\underbrace{+\hat{\omega}_r L_{tot} \hat{i}_{qs} + M \sin(\phi_0)\hat{v}_{dc}\hat{\varphi}_0 + V_{dc} \sin(\phi_0)\hat{m}\hat{\varphi}_0 + \sin(\phi_0)\hat{v}_{dc}\hat{m}\hat{\varphi}_0 - \cos(\phi_0)\hat{v}_{dc}\hat{m}}_{2-\ and\ 3-order\ nonlinear\ terms}
\end{array} \right\} \\
cp(V_{dc}+\hat{v}_{dc}) = \left\{ \begin{array}{l}
\underbrace{I_{qs} M \sin(\phi_0) + I_{ds} M \cos(\phi_0) - (1/r_l) V_{dc}}_{DC\ terms} \\
\underbrace{+I_{qs} M \cos(\phi_0)\hat{\varphi}_0 + M \sin(\phi_0)\hat{i}_{qs} + I_{qs} \sin(\phi_0)\hat{m} - I_{ds} M \sin(\phi_0)\hat{\varphi}_0 + M \cos(\phi_0)\hat{i}_{ds} + I_{ds} \cos(\phi_0)\hat{m} - (1/r_l)\hat{v}_{dc}}_{small-signal\ AC\ terms} \\
\underbrace{M \cos(\phi_0)\hat{i}_{qs}\hat{\varphi}_0 + I_{qs} \cos(\phi_0)\hat{m}\hat{\varphi}_0 + \sin(\phi_0)\hat{i}_{qs}\hat{m} + \cos(\phi_0)\hat{i}_{qs}\hat{m}\hat{\varphi}_0 - M \sin(\phi_0)\hat{i}_{ds}\hat{\varphi}_0 - I_{ds} \sin(\phi_0)\hat{m}\hat{\varphi}_0 + \cos(\phi_0)\hat{i}_{ds}\hat{m} - \sin(\phi_0)\hat{i}_{ds}\hat{m}\hat{\varphi}_0}_{2-\ and\ 3-order\ nonlinear\ terms}
\end{array} \right\} \\
Jp(\omega_r+\hat{\omega}_r) = \left\{ \underbrace{-(\frac{P}{2})^2 \lambda_m I_{qs}}_{DC\ terms} \quad \underbrace{-(\frac{P}{2})^2 \lambda_m \hat{i}_{qs}}_{small-signal\ AC\ terms} \right\}
\end{cases}
\tag{3-25}
$$

The equations of the DC values, are consolidated and expressed below:

$$
\begin{cases}
pI_{qs} = 0 = -\dfrac{r_s I_{qs}}{L_{tot}} - \omega_r I_{ds} + \dfrac{\lambda_m}{L_{tot}}\omega_r - \dfrac{1}{L_{tot}} V_{dc} M \sin(\phi_0) \\
pI_{ds} = 0 = \omega_r I_{qs} - \dfrac{r_s I_{ds}}{L_{tot}} - \dfrac{1}{L_{tot}} V_{dc} M \cos(\phi_0) \\
pV_{dc} = 0 = \dfrac{1}{c} I_{qs} M \sin(\phi_0) + \dfrac{1}{c} I_{ds} M \cos(\phi_0) - \dfrac{1}{r_l c} V_{dc} \\
p\omega_r = -(\dfrac{P}{2})^2 \dfrac{\lambda_m}{J} I_{qs}
\end{cases}
\tag{3-26}
$$

The DC equivalent circuit corresponding to the set of equations given by (3-26) is shown in Figure 3-6.

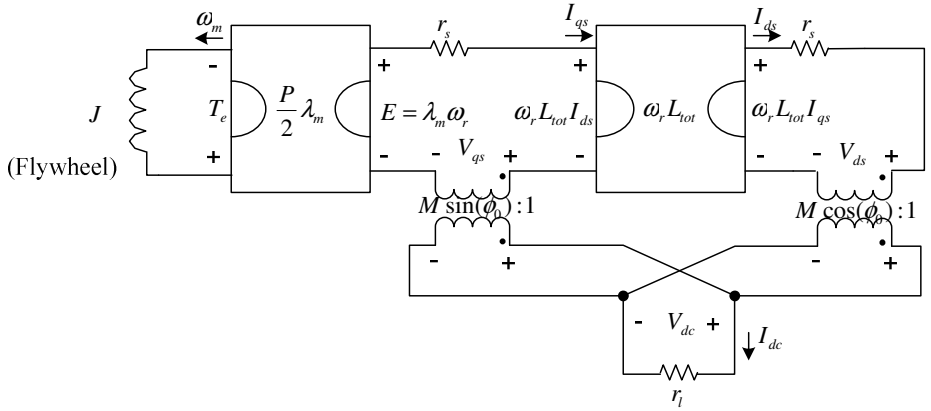


Figure 3-6 FESS DC mode during the discharging mode.

The small-signal AC equations are summarized below.

$$\begin{cases} p(\hat{i}_{qs}) = -\dfrac{r_s\hat{i}_{qs}}{L_{tot}} - \omega_r\hat{i}_{ds} - \dfrac{M\sin(\phi_0)}{L_{tot}}\hat{v}_{ds} + (\dfrac{\lambda_m}{L_{tot}} - I_{ds})\hat{\omega}_r - \dfrac{V_{dc}\sin(\phi_0)}{L_{tot}}\hat{m} - \dfrac{V_{dc}M\cos(\phi_0)}{L_{tot}}\hat{\varphi}_0 \\ p(\hat{i}_{ds}) = \omega_r\hat{i}_{qs} - \dfrac{r_s\hat{i}_{ds}}{L_{tot}} - \dfrac{M\cos(\phi_0)}{L_{tot}}\hat{v}_{dc} + I_{qs}\hat{\omega}_r - \dfrac{V_{dc}\cos(\phi_0)}{L_{tot}}\hat{m} + \dfrac{V_{dc}M\sin(\phi_0)}{L_{tot}}\hat{\varphi}_0 \\ p(\hat{v}_{dc}) = \dfrac{M\sin(\phi_0)}{c}\hat{i}_{qs} + \dfrac{M\cos(\phi_0)}{c}\hat{i}_{ds} - \dfrac{1}{r_l c}\hat{v}_{dc} + \dfrac{I_{qs}\sin(\phi_0)+I_{ds}\cos(\phi_0)}{c}\hat{m} + \dfrac{I_{qs}M\cos(\phi_0)-I_{ds}M\sin(\phi_0)}{c}\hat{\varphi}_0 \\ p(\hat{\omega}_r) = -(\dfrac{P}{2})^2\dfrac{\lambda_m}{J}\hat{i}_{qs} \end{cases} \tag{3-27}$$

The final step is to construct an equivalent circuit that corresponds to these equations. The small-signal AC circuit is drawn as shown in Figure 3-7(a). It is necessary to find a more simplified circuit. Figure 3-7(b) shows this circuit where sources are integrated. The voltage and current sources are:

$$\begin{aligned} v_1 &= -V_{dc}\sin(\phi_0)\hat{m} - V_{dc}M\cos(\phi_0)\hat{\varphi}_0 \\ v_2 &= -V_{dc}\cos(\phi_0)\hat{m} + V_{dc}M\sin(\phi_0)\hat{\varphi}_0 \\ i_1 &= [I_{qs}\sin(\phi_0) + I_{ds}\cos(\phi_0)]\hat{m} + [I_{qs}\cos(\phi_0) - I_{ds}\sin(\phi_0)]M\hat{\varphi}_0 \end{aligned} \tag{3-28}$$

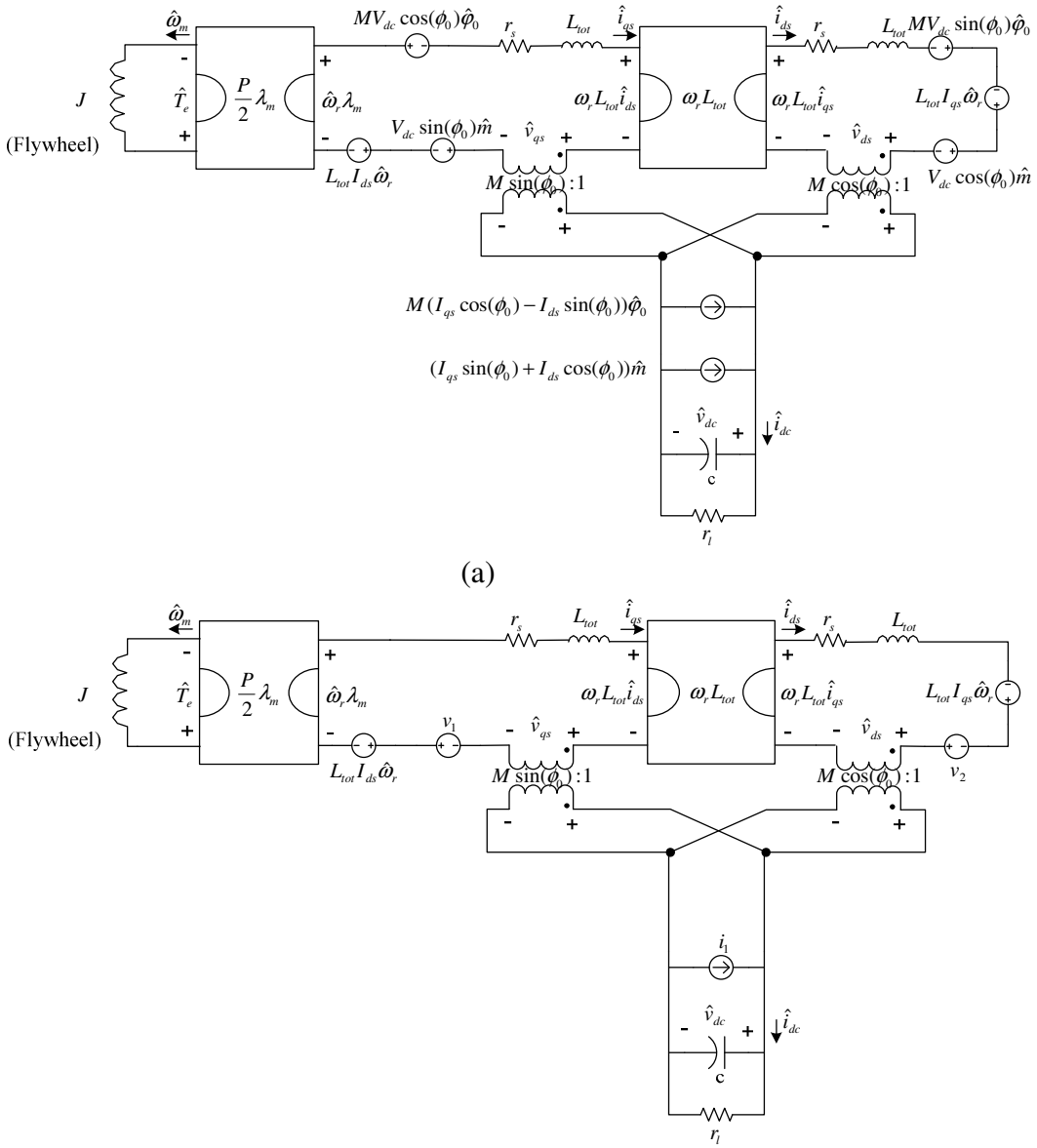


Figure 3-7 FESS small-signal AC mode during the discharging mode,
a) Complete model b) Simplified model.

3.2.1. DC Analysis

The DC analysis can be performed by the steady-state circuit, as shown in Figure 3-6. It is found from Figure 3-6 that

$$I_{qs} = -(\frac{2}{P})^2 \frac{J}{\lambda_m} p\omega_r \tag{3-29}$$

and ignoring the voltage drop across r_s of the d-axis equivalent circuit results in

$$\omega_r L_{tot} I_{qs} = V_{dc} M \cos(\varphi_0) \tag{3-30}$$

Then the DC transfer function is found to be

$$G_V = \frac{V_{dc}}{E} = -(\frac{2}{P})^2 \frac{L_{tot} Jp(\omega_r)}{\lambda_m^2 M \cos(\phi_0)} \tag{3-31}$$

where

$$E = \lambda_m \omega_r \tag{3-32}$$

Note that ignoring the voltage drop across r_s of the d-axis equivalent circuit is considered as a reasonable, but a simplifying approximation. Because the value of r_s is very small, and more significantly, the PMSM is not run in field weakening mode, so I_{ds} is set to zero, however, to preserve the generality of the analysis, I_{ds} is assumed to non-zero.

Obviously, (3-31) represents the boost action of the PWM rectifier operation. G_V ranges from zero to infinity by controlling M and ϕ_0. However, this is impeded in practice by current or voltage ratings.

The PWM rectifier input real power P_{rec}^{in} and reactive power Q_{rec}^{in} are found from [52]

$$P_{rec}^{in} = V_{qs} I_{qs} + V_{ds} I_{ds} \tag{3-33}$$

$$Q_{rec}^{in} = V_{qs} I_{ds} - V_{ds} I_{qs} \tag{3-34}$$

where

$$V_{qs} = \lambda_m \omega_r - r_s I_{qs} - \omega_r L_{tot} I_{ds}$$
$$V_{ds} = -r_s I_{ds} + \omega_r L_{tot} I_{qs} \tag{3-35}$$

Substituting (3-35) into (3-33) and (3-34) results in

$$P_{rec}^{in} = \lambda_m \omega_r I_{qs} - r_s I_{qs}^2 - r_s I_{ds}^2 \tag{3-36}$$

$$Q_{rec}^{in} = \lambda_m \omega_r I_{ds} - \omega_r L_{tot} I_{ds}^2 - \omega_r L_{tot} I_{qs}^2 \tag{3-37}$$

I_{ds} should be found in order to obtain the amount of reactive power. Writing a KCL equation at DC bus results in

$$I_{ds} = \frac{\frac{1}{r_l} V_{dc} - I_{qs} M \sin(\phi_0)}{M \cos(\phi_0)} \tag{3-38}$$

and substituting (3-29) and (3-31) into (3-38) results in

$$I_{ds} = (\frac{2}{P})^2 \frac{Jp(\omega_r)}{2\lambda_m r_l M^2 \cos(\phi_0)^2} (r_l M^2 \sin(2\phi_0) - 2\omega_r L_{tot}) \tag{3-39}$$

now Q_{rec}^{in} can be evaluated as given by (3-37) using (3-29) and (3-39). Then the power factor PF becomes

$$PF = \frac{P_{rec}^{in}}{(P_{rec}^{in\,2} + Q_{rec}^{in\,2})^{1/2}} \tag{3-40}$$

In the event that the PMSM is not run in field weakening mode, i.e. I_{ds} is controlled to be zero, the DC analysis of the FESS is simplified significantly. To keep $I_{ds} = 0$, M *and* ϕ_0 should be controlled such that (3-41) holds. The DC variables of the FESS at zero and non-zero I_{ds} are summarized in Table 3-2.

$$I_{ds} = 0 \Rightarrow M^2 \sin(2\phi_0) = \frac{2\omega_r L_{tot}}{r_l} \tag{3-41}$$

Table 3-2 Analytical model of the FESS for discharging mode.

Var.	$I_{ds} \neq 0$		$I_{ds} = 0$	
I_{qs}	$-(2/P)^2 Jp(\omega_r)/\lambda_m$			
I_{ds}	$I_{ds} = (2/P)^2 Jp(\omega_r)(r_l M^2 \sin(2\phi_0) - 2\omega_r L_{tot})/2\lambda_m r_l M^2 \cos(\phi_0)^2$			0
V_{dc}/E	$-(2/P)^2 L_{tot} Jp(\omega_r)/\lambda_m^2 M \cos(\phi_0)$		$L_{tot} I_{qs}/\lambda_m M \cos(\phi_0)$	
V_{qs}	$\lambda_m \omega_r - r_s I_{qs} - \omega_r L_{tot} I_{ds}$		$\lambda_m \omega_r - r_s I_{qs}$	
V_{ds}	$-r_s I_{ds} + \omega_r L_{tot} I_{qs}$		$\omega_r L_{tot} I_{qs}$	
P_{rec}^{in}	$\lambda_m \omega_r I_{qs} - r_s I_{qs}^2 - r_s I_{ds}^2$		$\lambda_m \omega_r I_{qs} - r_s I_{qs}^2$	
Q_{rec}^{in}	$\lambda_m \omega_r I_{ds} - \omega_r L_{tot} I_{ds}^2 - \omega_r L_{tot} I_{qs}^2$		$-\omega_r L_{tot} I_{qs}^2$	
PF	$P_{rec}^{in}/(P_{rec}^{in\,2} + Q_{rec}^{in\,2})^{1/2}$		$(1+(L_{tot} I_{qs}/\lambda_m)^2)^{-1/2}$	
ϕ_0	NA	$1/2\sin^{-1}(2\omega_r L_{tot}/r_l M^2)$		
M	NA	$(V_{qs}^2 + V_{ds}^2)^{1/2}/V_{dc}$		

3.2.2. Small-Signal AC Analysis

Based on (3-27), the small signal model of the FESS in discharging mode can be expressed as the state space differential equations given by (3-42).

$$\begin{bmatrix} \dot{\hat{i}}_{qs} \\ \dot{\hat{i}}_{ds} \\ \dot{\hat{v}}_{dc} \\ \dot{\hat{\omega}}_r \end{bmatrix} = \begin{bmatrix} -\frac{r_s}{L_{tot}} & -\omega_r & -\frac{M\sin(\phi_0)}{L_{tot}} & \frac{\lambda_m}{L_{tot}} - I_{ds} \\ \omega_r & -\frac{r_s}{L_{tot}} & -\frac{M\cos(\phi_0)}{L_{tot}} & I_{qs} \\ \frac{M\sin(\phi_0)}{c} & \frac{M\cos(\phi_0)}{c} & -\frac{1}{r_l c} & 0 \\ -(\frac{P}{2})^2 \frac{\lambda_m}{J} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{qs} \\ \hat{i}_{ds} \\ \hat{v}_{dc} \\ \hat{\omega}_r \end{bmatrix} + \begin{bmatrix} -\frac{V_{dc} M\cos(\phi_0)}{L_{tot}} & -\frac{V_{dc}\sin(\phi_0)}{L_{tot}} \\ \frac{V_{dc} M\sin(\phi_0)}{L_{tot}} & -\frac{V_{dc}\cos(\phi_0)}{L_{tot}} \\ \frac{I_{qs} M\cos(\phi_0) - I_{ds} M\sin(\phi_0)}{c} & \frac{I_{qs}\sin(\phi_0) + I_{ds}\cos(\phi_0)}{c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{\varphi}_0 \\ \hat{m} \end{bmatrix}$$

(3-42)

Now we can analyze the small-signal AC model of the system at any operating point. It is possible to derive the small-signal AC model at any speed. Since the starting and ending speeds are the most critical operating points in which the mode of operation is changed, these points are of higher interest, however, there is no loss of generality throughout the speed range.

3.3. Simulation Results

The parameters of a 240 kW, 19 to 23 krpm FESS and its desired operation are presented in Table 3-3. The analytical model is used to simulate the DC operating points, illustrated in Table 3-4 to Table 3-6. In the next section, the FESS and its control system are simulated by PSIM package to verify the accuracy of the developed analytical model.

The simulations results for DC operating points based on Table 3-1 and Table 3-2 are illustrated in Table 3-4 and Table 3-5. Note that $\phi_0 = \varphi_2 - \varphi_1$ where φ_1 is the arbitrary angle of the linkages flux and not the back-EMF. For example, in Table 3-4, the angle between the inverter phase voltage and the phase back-EMF is 96.5^o - 90^o=6.5^o.

Table 3-3 FESS parameters and desired operation.

PMSM/Flywheel	
Rated Power	60 kW
Number of Poles	2
Operating Speed Range	19 – 23 krpm
L-N back-EMF constant	5.95 V_{rms} / krpm
Winding Resistance (Per Phase)	8.17 mΩ
$L=L_{qs}=L_{ds}$	91.3 μH
Moment of Inertia (PMSM/Flywheel)	0.63 kgm2
Fractional Coefficient (B)	0 Nm.sec/rad
DC Bus	
DC Bus Voltage	500 V
Capacitor Bank	23.4 mF
Resistive Load (Regenerative Mode)	1.04 Ω
External Inductor	
Charging Mode	150 uH
Discharging Mode	0 uH
FESS Desired Operation	
Rated Output Power in Speed Range	240 kW
Rated Speed Range	23 – 19 krpm
Duration of Discharge	2 sec
Duration of Charge	58 sec
Total Delta Energy	0.58 MJ
System Efficiency	80 %

Table 3-4 240 kW FESS charging in 58 sec with constant I_{qs} (Inverter output).

Speed (rpm)	L_{ext} (uH)	I_{qs} (A)	I_{ds} (A)	I_{as} (Arms)	V_{qs} (V)	V_{ds} (V)	P_{inv}^{out} (kW)	Q_{inv}^{out} (kVar)	PF	M	ϕ_0 (deg)
23000	150	46.2	0	26.7	237.0	-26.9	10.959	1.242	0.99	0.48	96.5
21500	150	46.2	0	26.7	221.6	-25.1	10.244	1.161	0.99	0.44	96.5
19000	150	46.2	0	26.7	195.8	-22.2	9.053	1.026	0.99	0.39	96.5

Table 3-5 240 kW FESS discharging in 2 sec with constant I_{qs} (Rectifier input).

Speed (krpm)	L_{ext} (uH)	I_{qs} (A)	I_{ds} (A)	I_{as} (Arms)	V_{qs} (V)	V_{ds} (V)	P_{rec}^{in} (kW)	Q_{rec}^{in} (kVar)	PF	M	ϕ_0 (deg)
23	0	1340.8	0	774.0	226.0	294.8	303.11	-395.31	-0.63	0.74	37.2
21.5	0	1340.8	0	774.0	210.6	275.6	282.39	-369.53	-0.63	0.69	37.2
19	0	1340.8	0	774.0	184.8	243.6	247.8	-326.6	-0.63	0.61	37.2

Table 3-6 240 kW discharging in 2 sec with constant power (Rectifier input).

Speed (krpm)	L_{ext} (uH)	I_{qs} (A)	I_{ds} (A)	I_{as} (Arms)	V_{qs} (V)	V_{ds} (V)	P_{rec}^{in} (kW)	Q_{rec}^{in} (kVar)	PF	M	ϕ_0 (deg)
23	0	1051.0	0	606.8	228.4	231.1	240.0	-242.9	-0.72	0.65	44.7
21.5	0	1130.0	0	652.4	212.3	232.3	240.0	-262.5	-0.69	0.63	42.4
19	0	1296.0	0	748.2	185.2	235.4	240.0	-305.11	-0.64	0.6	38.2

It should be noted that according to (3-31) and for the given FESS parameters, the maximum amount of G_V to maintain the DC bus voltage equal to 500 V is $G_{V,\max} = 500/195|_{\omega_r=19000rpm} = 2.56$.

4. CONTROL DESIGN OF THE FESS

The development of robust controllers for high-speed flywheel rotors supported on magnetic bearings has been extensively studied over the past decade [53-61]. Different types of controllers have been proposed for this challenging control problem. For instance [53-55], [56], [57], and [58-61] propose use of H_∞ control, fuzzy logic controllers, nonlinear controllers, and PI-based vector control systems as their solutions. As is obvious, each of these controllers have their inherent advantages and disadvantages.

In this section a novel PI-based vector controller is implemented with the FESS to meet the desired performance either in steady state or in transient conditions. PID controllers and more specifically PI controllers are widely used in motion control such as in high speed FESS. The main characteristics of these controllers can be summarized as (i) set point regulation (error zeroing) against arbitrary disturbances, (ii) robustness against modeling errors, and (iii) three terms controllers that are easier to adjust during the design stage as well as in real time in the case of adaptive control implementation.

A control algorithm which acts to regulate the operation of the FESS in both charge (motoring) and discharge (generating) modes is developed [62]. The algorithm regulates the operation of the FESS by charging the flywheel with constant current during charge mode and regulating the DC bus voltage during discharge mode under constant power.

4.1. PMSM Control Concept

Similar to a DC machine, the q-axis current of the PMSM is distinctly equivalent to the armature current; while the d-axis current constitutes a part of the field current equivalent and the other part is contributed by the permanent magnet field. In [36] two important factors affecting operation of the machine: power factor and armature reaction were investigated in detail. When the PMSM is operating as a generator its output power is absolutely dependent on leading, unity or lagging power factor at the terminal of the PMSM as well as its torque angle, the angle between the rotor field and stator current phasor. In other words, these items affect the terminal voltage of the machine and the output power.

Reference [36] verifies that by using a leading power factor one can achieve a higher output power from the machine than with unity or lagging power factors. Moreover, when the phase current increases the terminal voltage drops significantly under all leading, unity and lagging power factors. The reason for this is that the armature reaction is caused by high phase current, similar to that in the operation of DC machines. Therefore, with a proper control strategy that makes the torque angle equal to 90^{o}, the armature reaction is completely eliminated.

4.1.1. Power Factor (Lead, Unity or Lag)

Let's consider Figure 4-1, which depicts the terminal voltage and output power of a 125 kW PMSM tested under three different load power factors such as 0.95 leading, 1.0 and 0.95 lagging. The parameters of the PMSM are given in Table 4-1. However, the control strategy is kept the same for the three tests, the torque angle, $\gamma \neq 90^{o}$ is selected

for control strategy to point out the effect of the armature reaction. As the figure shows, by leading power factor, the output power drawn from the machine is higher than for the other cases for similar phase currents. Figure 4-2 depicts the phasor diagrams confirming the above claim. In this figure, it is assumed that the back-EMF is constant, i.e. the armature reaction is not taken into account.

It is interesting to note that the vector control with 90 degrees torque angle control strategy achieves the goal explained in this section [63]. In other words, as shown in Figure 4-2, this control strategy, naturally, provides the PMSM with leading power factor. In this method, the value of leading power factor is solely dependent on the phase current of the PMSM. It means that higher phase current causes smaller leading power factor and consequentially higher terminal voltage and higher output power.

Table 4-1 PM synchronous machine parameters.

Rated Power	125 kW
Number of Phases	3
Number of Poles	2
Operating Speed Range	20 – 36 krpm
Winding Connection	Star
Nominal No-load Voltage	279.5 V L-N rms at 36 krpm
Winding Resistance (Per Phase)	0.02 Ohm
Winding Inductance (Per Phase)	70 – 120 μH
Moment of Inertia (PMSM+Flywheel)	0.633 kgm^2
Fractional Coefficient (B) (Flywheel)	4.2 e-5 Nm.sec/rad

4.1.2. Armature Reaction

Figure 4-1 shows that when the phase current increases, the terminal voltage drops deeply in all the three cases. The reason is related to armature reaction caused by

high phase current, exactly the same as what happens in DC machines. By analogy with a DC machine, the q-axis current of the PMSM is distinctly equivalent to the armature current; while the d-axis current constitutes a part of the field current equivalent and the other part is contributed by the permanent magnet field.

Therefore, if we can apply a good control strategy that make the torque angle, γ, equal to 90^o then the armature reaction is completely eliminated. Table 4-2 shows the effect of eliminating armature reaction on the terminal voltage and output power. It is noticeable that in a $\gamma \neq 90^o$ control strategy (Id $\neq$ 0); however, when the value of leading power factor is bigger (0.95), the output power is lower. The reason is that the terminal voltage increment in $\gamma = 90^o$ control strategy (Id = 0) overcomes the power factor increment in the other control strategies. It is interesting to observe again that this goal is obtained by vector control with $\gamma = 90^o$.

To summarize it, it is verified that vector control with 90^0 torque angle achieves both goals: leading power factor and no armature reaction resulting in a higher output power. The investigation results are depicted in Figure 4-2. The phasor diagram shows the control strategy results in the maximum output power from the FESS under constant phase current.

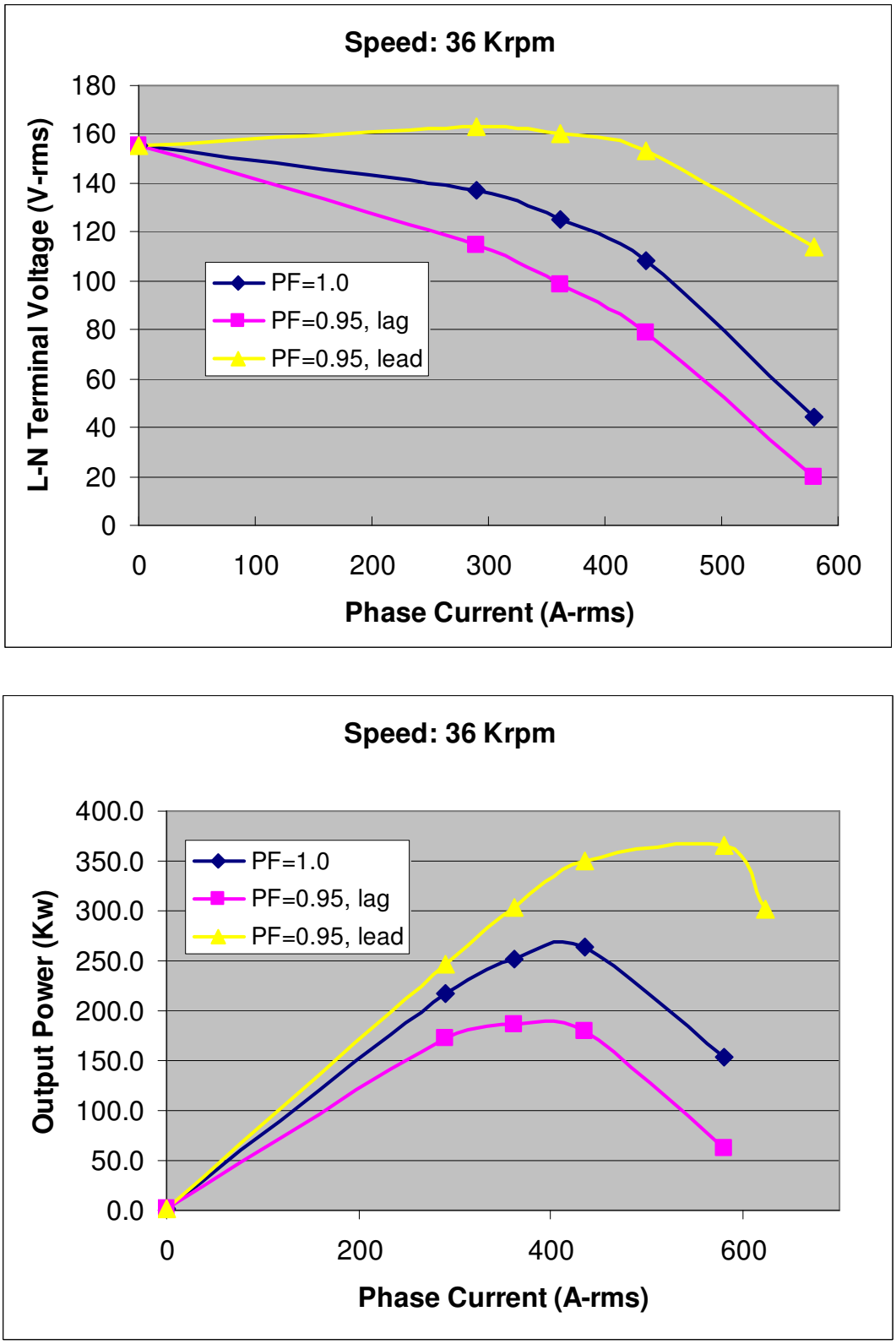


Figure 4-1 Terminal voltage and output power of the PMSM ($\gamma \neq 90^{o}$) [24].

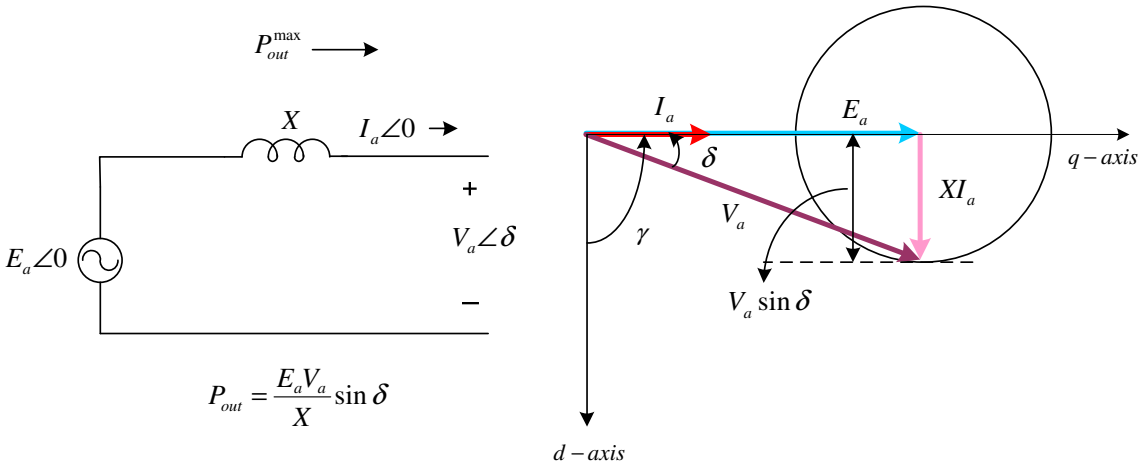


Figure 4-2 Phasor diagram of the PMSM in regenerating mode with leading power factor and no armature reaction.

Table 4-2 Armature reaction effect on the terminal voltage and output power of the PMSM.

$\gamma = 90^o$ Control Strategy (Id = 0)				$\gamma \neq 90^o$ Control Strategy (Id ≠ 0)			
Terminal Voltage (V-rms)	Phase Current (A-rms)	Leading P.F.	Output Power (KW)	Terminal Voltage (V-rms)	Phase Current (A-rms)	Leading P.F.	Output Power (KW)
279.5	0	-	0.0	279.5	0	-	0.0
292.9	289.8	0.961	244.7	298.8	289.8	0.95	246.8
305.6	434.6	0.921	367.0	282.7	434.6	0.95	350.2
318.4	579.5	0.871	482.1	221.8	579.5	0.95	366.3
321.3	623	0.854	512.8	169.6	623	0.95	301.1

4.2. FESS Control System

Figure 4-3 shows a high level picture of the FESS and its controllers. In the charge as well as discharge modes, field orientation control is employed to control the system. Regardless of the inner current loop controllers which are common in both modes of operations, two outer loops, speed loop and voltage loop controllers are implemented in the charge and the discharge modes, respectively.

During charging, the inner current loop controllers and the outer speed loop controller regulate the whole system performance and during discharging mode the outer speed loop controller is inactive and instead a DC bus voltage regulator controls the DC bus voltage shown in Figure 4-3. Obviously, the current, speed, and DC bus voltage regulations are realized by PI controllers.

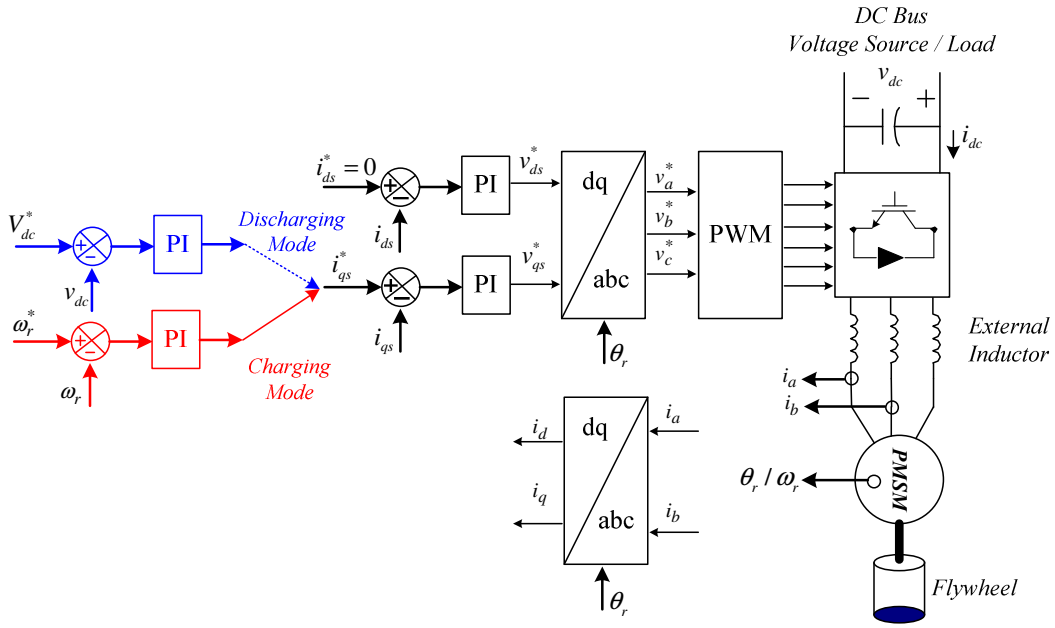


Figure 4-3 Flywheel energy storage system along with the controllers.

Before the control algorithm is described, the motor variables in the rotor reference frame and the relationships between the powers at different points of the FESS are presented as they are used in the consequentially developed control algorithms.

4.2.1. d-q Model of the FESS

To outline the control system, the d-q model of the FESS derived in Section 2 is used. For convenience the large-signal models are depicted in Figure 4-4. According to the d-q model, (4-1)-(4-3) represent the voltage, electromagnetic torque, and electromechanical equations of the FESS in the rotor reference frame.

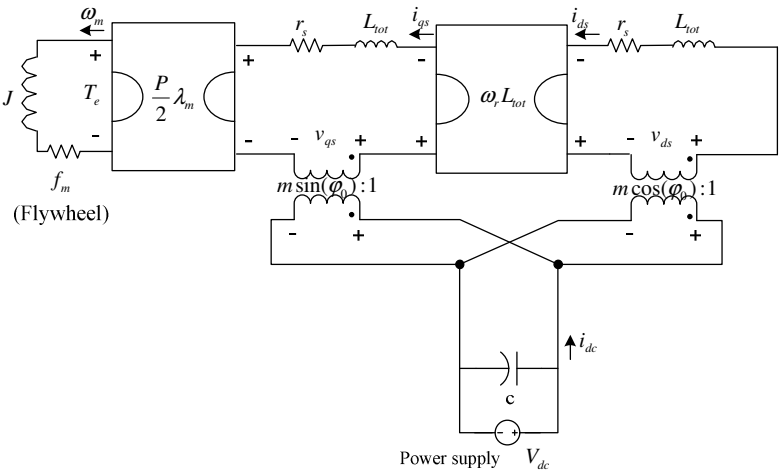
$$\begin{aligned} Ch: &\begin{cases} v_{qs} = r_s i_{qs} + L_{tot} p i_{qs} + \omega_r L_{tot} i_{ds} + \omega_r \lambda_m \\ v_{ds} = r_s i_{ds} + L_{tot} p i_{ds} - \omega_r L_{tot} i_{qs} \end{cases} \\ Disch: &\begin{cases} \omega_r \lambda_m = r_s i_{qs} + L_{tot} p i_{qs} + \omega_r L_{tot} i_{ds} + v_{qs} \\ 0 = r_s i_{ds} + L_{tot} p i_{ds} - \omega_r L_{tot} i_{qs} + v_{ds} \end{cases} \end{aligned} \tag{4-1}$$

$$T_e = \pm \frac{P}{2} \lambda_m i_{qs} \tag{4-2}$$

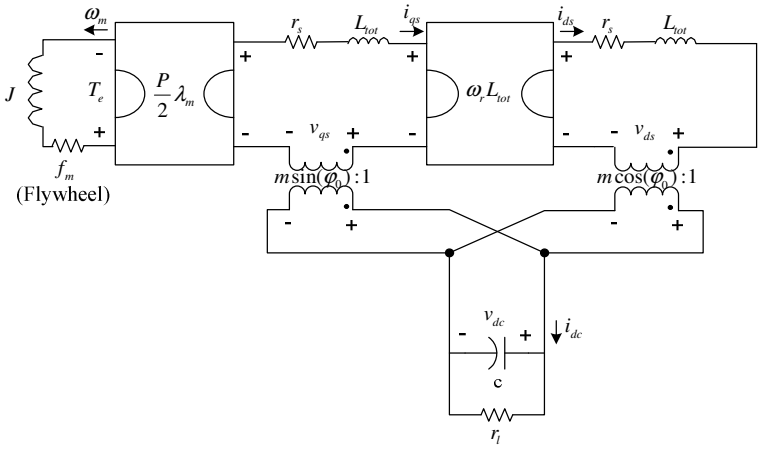
$$T_e = J \frac{d}{dt} \omega_m + f_m \omega_m \tag{4-3}$$

where v_{qs}, v_{ds}, i_{qs}, and i_{ds} denote the q- and d-axes components of the inverter/rectifier terminal voltages and currents, r_s denotes the PMSM phase winding resistance. $L_{tot} = L + L^{ex}$ where $L = L_{qs} = L_{ds}$, d- and q-axes inductances of the PMSM, and $L^{ex} = L_s^{ex} + L_m$, where L_s^{ex} and L_m are self and mutual inductances of the external inductance respectively. ω_m and ω_r are the mechanical and electrical rotational speeds of the machine, $\sqrt{2/3}\lambda_m$ denotes the amplitude of the flux linkages established by the permanent magnets as viewed from the stator phase windings, T_e is the electromagnetic torque developed by the PMSM, J is moment of inertia of the PMSM rotor plus the flywheel, and f_m is friction coefficient. Note that in the developed model, the modified park transformation matrix

given by (4-4) is used. Then according to (4-4) and λ_m definition, the coefficient 3/2 is removed from the torque equation (4-2).



(a)



(b)

Figure 4-4 FESS d-q model, a) Charging mode b) Discharging mode.

$$K_s = \sqrt{2/3}\begin{bmatrix} \cos(\theta_r) & \cos(\theta_r - 2\pi/3) & \cos(\theta_r + 2\pi/3) \\ \sin(\theta_r) & \sin(\theta_r - 2\pi/3) & \sin(\theta_r + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{4-4}$$

As mentioned before, vector control with 90^o torque angle achieves leading power factor and no armature reaction thus resulting in a higher output power. In other words, it leads to the maximum torque/ampere ratio which is the most desired characteristic during acceleration and deceleration in the FESS application. In this control, the torque angle is maintained at 90^o degrees; hence, the field or direct axis current is made to be zero, leaving only the torque or the quadrate axis current in place. This is the mode of operation for speeds lower than the base speed.

In regenerative mode, the direction of the power flow is from the PMSM toward the DC bus. The machine's output electrical power is equal to the mechanical power minus any losses. In the FESS, the flywheel shaft is suspended vertically using magnetic bearings and is operated in vacuum. Thus the typical machine losses, friction and windages, are essentially eliminated so that the electrical power is approximately equal to the mechanical shaft power as shown by (4-5). Additionally, the eddy current and hysteresis losses are minimal in the PMSM used for this application.

$$P_{PMSG}^{out} = T_e \omega_m \tag{4-5}$$

Also, the speed of the machine is related to the developed electromagnetic torque and the inertia by (4-3), however, f_m can be eliminated from the equation.

Therefore the power into the rectifier is the electrical power from the generator, P_{PMSG}^{out}. If the rectifier losses are neglected, the power into the rectifier is equal to the output power of the rectifier. Output power of the rectifier is given by the product of the rectifier current, i_{dc}, and the DC bus voltage as given in (4-6).

$$P_{rec}^{in} = v_{dc} i_{dc} = P_{PMSG}^{out} \tag{4-6}$$

The rectifier current can be then expressed as a function of the motor torque, the shaft speed and the DC bus voltage as given by (4-7).

$$i_{dc} = \frac{T_e \omega_m}{v_{dc}} \tag{4-7}$$

4.2.2. FESS Control During Charging Mode

From (4-3) the motor speed can be regulated if the motor torque is controlled. In the field orientation technique, the torque control is achieved by properly controlling the current components, i_{qs} and i_{ds}. The d-axis current, i_{ds}, is commanded to zero which results in a linear relationship between the machine torque and current as shown in (4-2). Then the FESS control algorithm shown in Figure 4-5 can be described as following.

1. Determine the motor speed set point, ω_m^*, to achieve the desired ω_m during the charging mode.

2. Convert the commanded motor speed value, ω_m^*, to a commanded motor torque, T_e^*, using (4-3).

3. Convert the commanded motor torque, T_e^*, to a commanded motor current, i_{qs}^*, using (4-2).

4. Regulate the motor current, i_{qs}, to the commanded value, i_q^*, through a high bandwidth current regulator and the field orientation motor control algorithm.

The available feedback variables are the motor speed, ω_m, the rotor position, θ_r, and the motor phase currents, i_a and i_b.

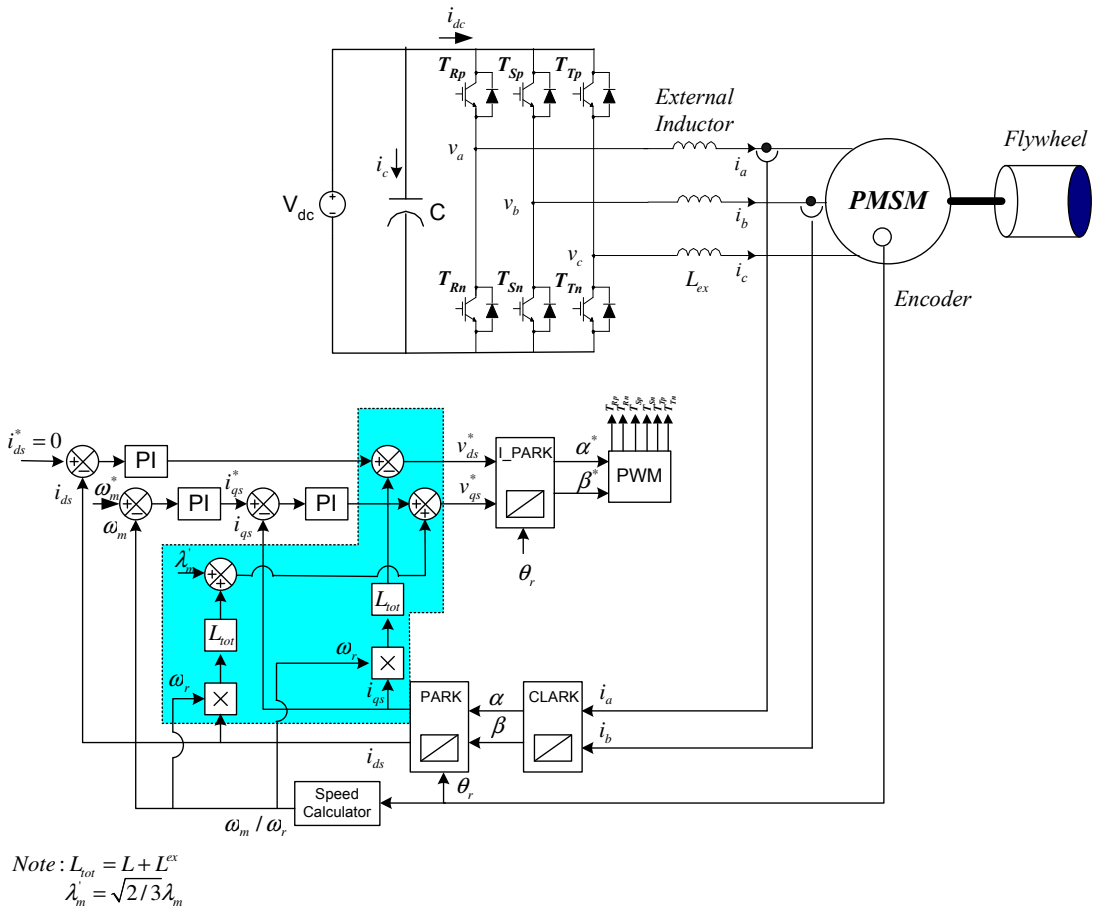


Figure 4-5 Charging mode control block diagram.

The block diagram representation of the charge control algorithm is shown in Figure 4-5. There are two components to the controller: the proportional integral (PI) and the feed-forward (FF) block, highlighted area. The respective outputs are summed together to form v_{qs}^* and v_{ds}^* commands.

One drawback to PI control acting alone is that the system must wait for an error signal before a control adjustment is made. One technique that can be used to minimize the dependence on the PI controller is the feed-forward control which is implemented in the controller. To derive the feed-forward block diagram, setting i_{ds} to zero in (4-1) results in (4-8) which determines the configuration of the feed-forward block diagram.

$$Ch: \quad \begin{cases} v_{qs} = r_s i_{qs} + L_{tot} p i_{qs} + \omega_r \lambda_m \\ v_{ds} = -\omega_r L_{tot} i_{qs} \end{cases} \tag{4-8}$$

4.2.3. FESS Control During Discharging Mode

From the previous discussion it can be seen that the DC bus voltage can be controlled if the rectifier current and as a result the motor torque are controlled as given by (4-7). The relationship between the motor current and the inverter current can be derived by substituting (4-2) into (4-7) where ω_r, the electrical speed, equals the product of the number of pole pairs, P/2, and ω_m, the mechanical speed. The result is given by (4-9). This equation is used in the control algorithm for discharging mode.

$$i_{qs} = \frac{v_{dc} i_{dc}}{\lambda_m \omega_r} \tag{4-9}$$

Therefore the FESS control algorithm during the discharge shown in Figure 4-6 mode can be described as follows:

1. Calculate the commanded inverter current value, i_{dc}^*, to achieve the desired v_{dc}^* during discharge mode.

2. Convert the commanded inverter current, i_{dc}^*, to a commanded motor current, i_{qs}^*, using (4-9).

3. Regulate the motor current, i_{qs}, to the commanded value, i_{qs}^*, through a high bandwidth current regulator and the field orientation motor control algorithm.

The available feedback variables are the DC bus voltage, v_{dc}, the rectifier output current, i_{dc}, and the motor speed, ω_m, the rotor position, θ_r, and the motor currents i_a and

i_b. A discussion similar to the one before can be held for the feed-forward controls function in this block diagram.

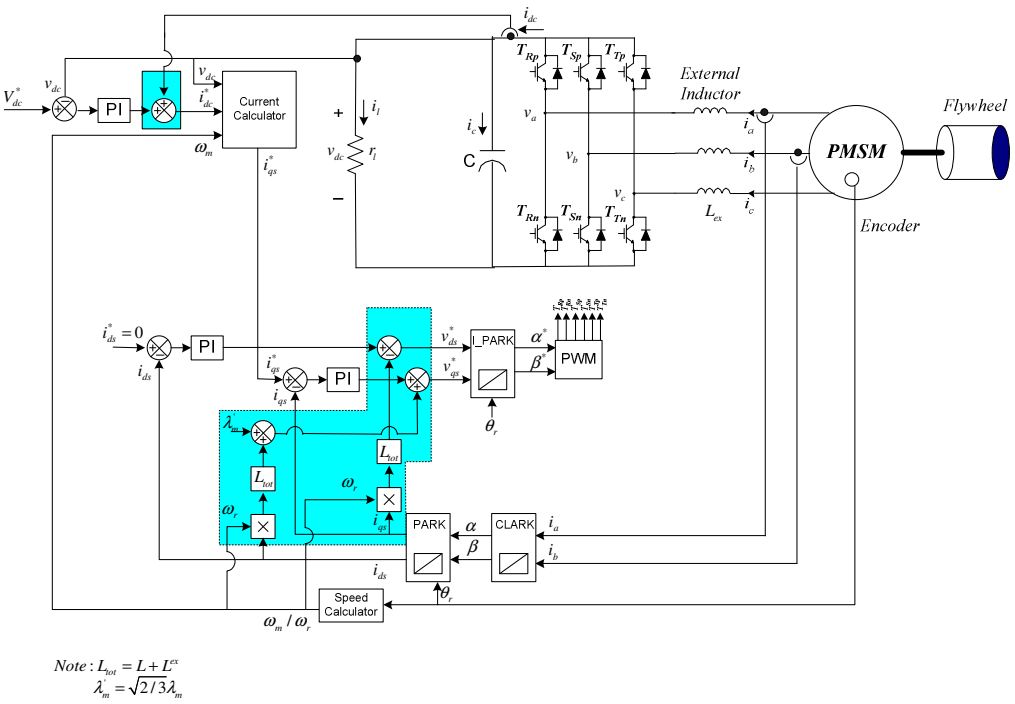


Figure 4-6 Discharging mode control block diagram.

The FESS whole control algorithm is depicted in Figure 4-7 which combines both the charging and discharging mode controls. Obviously, in the charging mode, the speed-loop controller determines the i_{qs}^{*} and in the discharging mode, the DC bus voltage-loop controller does the job.

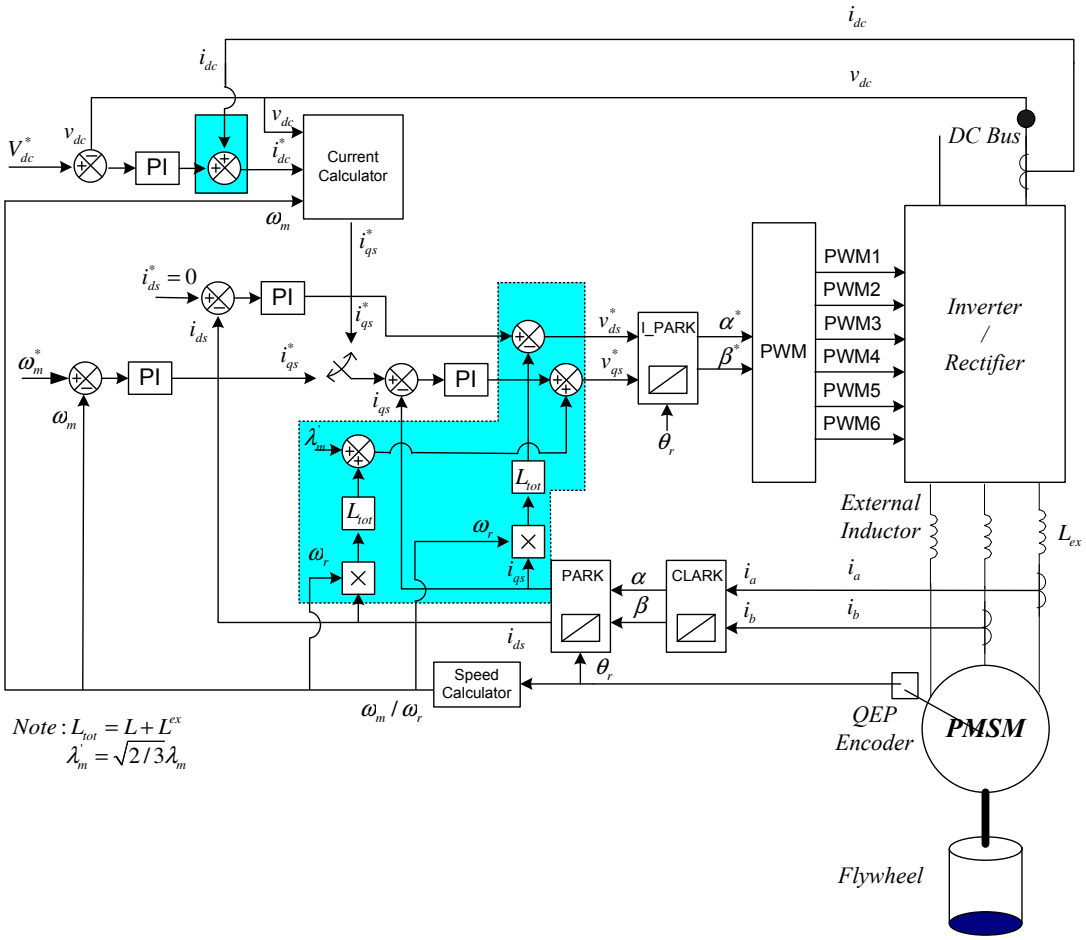


Figure 4-7 Block diagram of the FESS control system.

4.3. Block Diagram Derivations

In this section, the current-, speed-, and voltage-loop block diagrams are derived and then the PI controllers are designed. Combining (4-3) and (4-8) results in:

$$\frac{P}{2}\lambda_m i_{qs} = J\frac{d}{dt}\omega_m + f_m\omega_m \tag{4-10}$$

Combining (4-8) and (4-10), the correspondent block diagram with the current and speed loop controllers is derived as shown in Figure 4-8. The inverter is modeled as

a gain with a time lag by $k_{in}(1+sT_{in})^{-1}$. The current sensor is modeled as a gain, H_c, and the speed sensor is modeled by $H_\omega(1+sT_\omega)^{-1}$ [64].

According to Figure 4-8, the back-EMF crosses the q-axis current loop, and it could be simplified by moving the pick-off point for the back-EMF loop from speed to current output point as shown in Figure 4-9(a) [64]. Figures 4-9(b) and (c) show the equivalent block diagrams where the latter depicts the closed-loop current controller with unity feedback. The open-loop transfer function of the current-loop and the PI controller are given by (4-11).

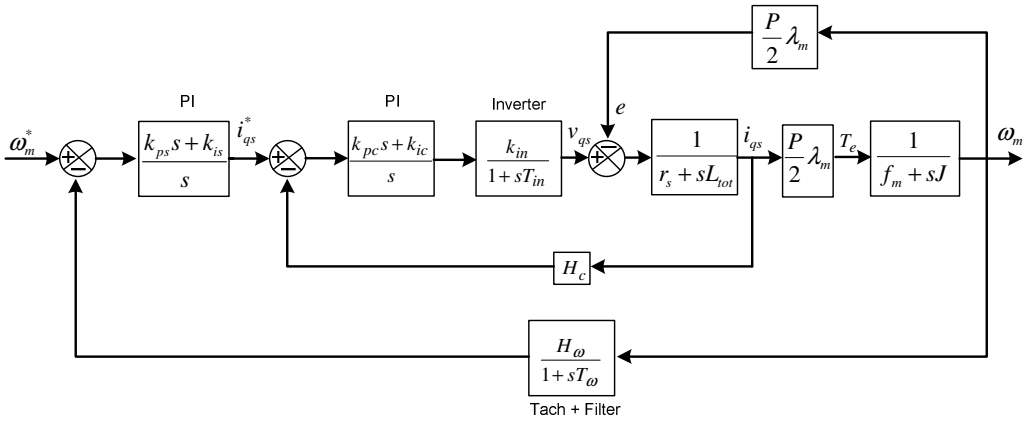
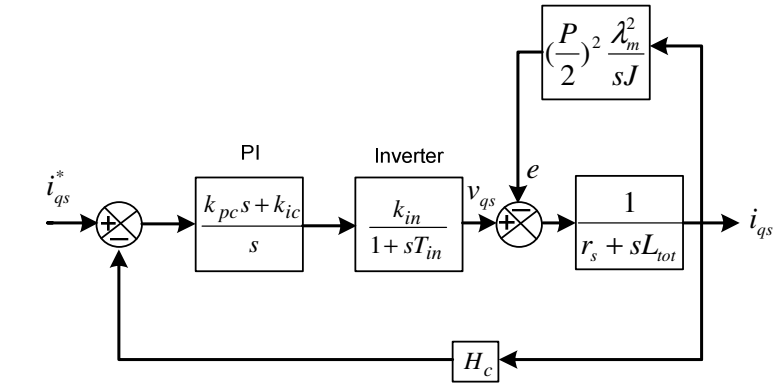


Figure 4-8 Block diagram of the speed-controlled FESS.

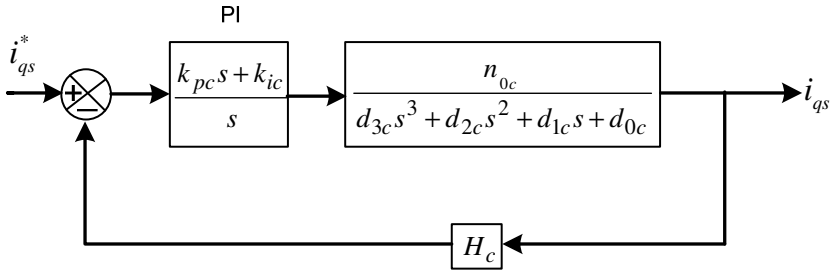
$$P_c(s)=\frac{N_{pc}(s)}{D_{pc}(s)}=\frac{n_{1c}s+n_{0c}}{d_{3c}s^3+d_{2c}s^2+d_{1c}s+d_{0c}}$$
$$C_c(s)=\frac{N_{cc}(s)}{D_{cc}(s)}=\frac{k_{pc}s+k_{ic}}{s} \qquad (4\text{-}11)$$

where

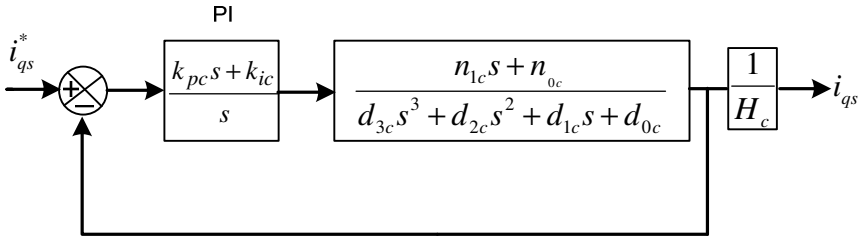
$$
\begin{aligned}
n_{1c} &= k_{in} J H_c \\
n_{0s} &= k_{in} f_m H_c \\
d_{3c} &= T_{in} L_{tot} J \\
d_{2c} &= L_{tot} J + T_{in} L_{tot} f_m + T_{in} r_s J \\
d_{1c} &= L_{tot} f_m + r_s J + T_{in} r_s f_m + T_{in} (\frac{P}{2} \lambda_m)^2 \\
d_{0c} &= r_s f_m + (\frac{P}{2} \lambda_m)^2
\end{aligned}
\tag{4-12}
$$



(a)



(b)



(c)

Figure 4-9 (a) Block diagram of the current-loop controller, (b) Simplified block diagram, (c) Block diagram of the current-loop controller with unity feedback.

Considering the PI controller and the feedback gain, H_c, the closed-loop transfer function of the current-loop can be presented by (4-13).

$$\frac{I_{qs}(s)}{I_{qs}^{*}(s)} = \frac{n_{2cl}s^2 + n_{1cl}s + n_{0cl}}{d_{4cl}s^4 + d_{3cl}s^3 + d_{2cl}s^2 + d_{1cl}s + d_{0cl}} \tag{4-13}$$

where

$$\begin{aligned}
n_{2cl} &= \frac{1}{H_c}k_{pc}n_{1c} \\
n_{1cl} &= \frac{1}{H_c}(k_{pc}n_{0c} + k_{ic}n_{1c}) \\
n_{0cl} &= \frac{1}{H_c}k_{ic}n_{0c} \\
d_{4cl} &= d_{3c} \\
d_{3cl} &= d_{2c} \\
d_{2cl} &= d_{1c} + k_{pc}n_{1c} \\
d_{1cl} &= d_{0c} + k_{pc}n_{0c} + k_{ic}n_{1c} \\
d_{0cl} &= k_{ic}n_{0c}
\end{aligned} \tag{4-14}$$

Considering the internal current-loop controller, the block diagram of the speed-loop controller is shown in Figure 4-10. For control purpose, a PI controller is sufficient, however, since the measured speed signal is smooth, a PID controller can be also implemented. Transfer function of the open-loop speed controller and the PI controller are given by (4-15).

$$\begin{aligned}
P_s(s) &= \frac{N_{ps}(s)}{D_{ps}(s)} = \frac{n_{2s}s^2 + n_{1s}s + n_{0s}}{d_{6s}s^6 + d_{5s}s^5 + d_{4s}s^4 + d_{3s}s^3 + d_{2s}s^2 + d_{1s}s + d_{0s}} \\
C_s(s) &= \frac{N_{cs}(s)}{D_{cs}(s)} = \frac{k_{ps}s + k_{is}}{s}
\end{aligned} \tag{4-15}$$

where

$$
\begin{aligned}
n_{2s} &= n_{2cl}(\frac{P}{2})\lambda_m H_\omega \\
n_{1s} &= n_{1cl}(\frac{P}{2})\lambda_m H_\omega \\
n_{0s} &= n_{0cl}(\frac{P}{2})\lambda_m H_\omega \\
d_{6s} &= JT_\omega d_{4cl} \\
d_{5s} &= (f_m T_\omega + J)d_{4cl} + JT_\omega d_{3cl} \\
d_{4s} &= f_m d_{4cl} + (f_m T_\omega + J)d_{3cl} + JT_\omega d_{2cl} \\
d_{3s} &= f_m d_{3cl} + (f_m T_\omega + J)d_{2cl} + JT_\omega d_{1cl} \\
d_{2s} &= f_m d_{2cl} + (f_m T_\omega + J)d_{1cl} + JT_\omega d_{0cl} \\
d_{1s} &= f_m d_{1cl} + (f_m T_\omega + J)d_{0cl} \\
d_{0s} &= f_m d_{0cl}
\end{aligned}
\tag{4-16}
$$

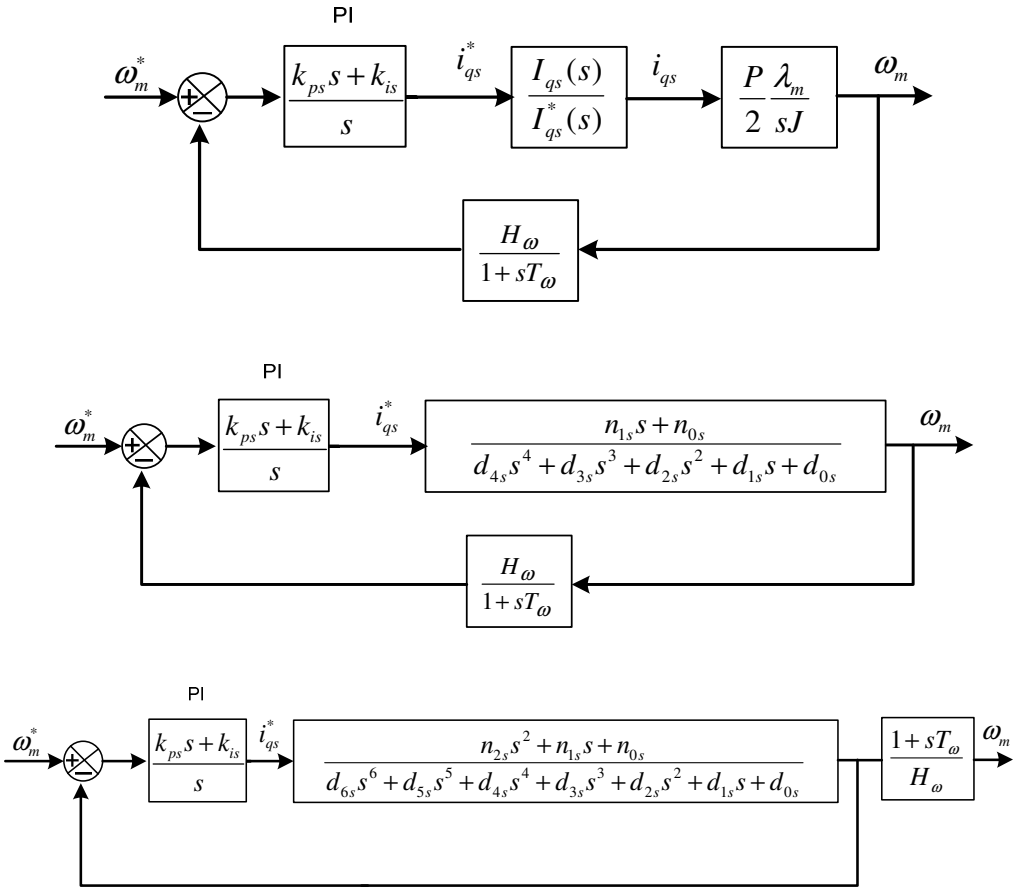


Figure 4-10 Block diagram of the speed-loop controller.

Combining (4-5), (4-6), (4-8), (4-9) and (4-10) and considering the parallel capacitor bank, c, and load resistance, r_l, at the DC bus, the block diagram representing the DC bus voltage control-loop is derived and depicted as in Figure 4-11.

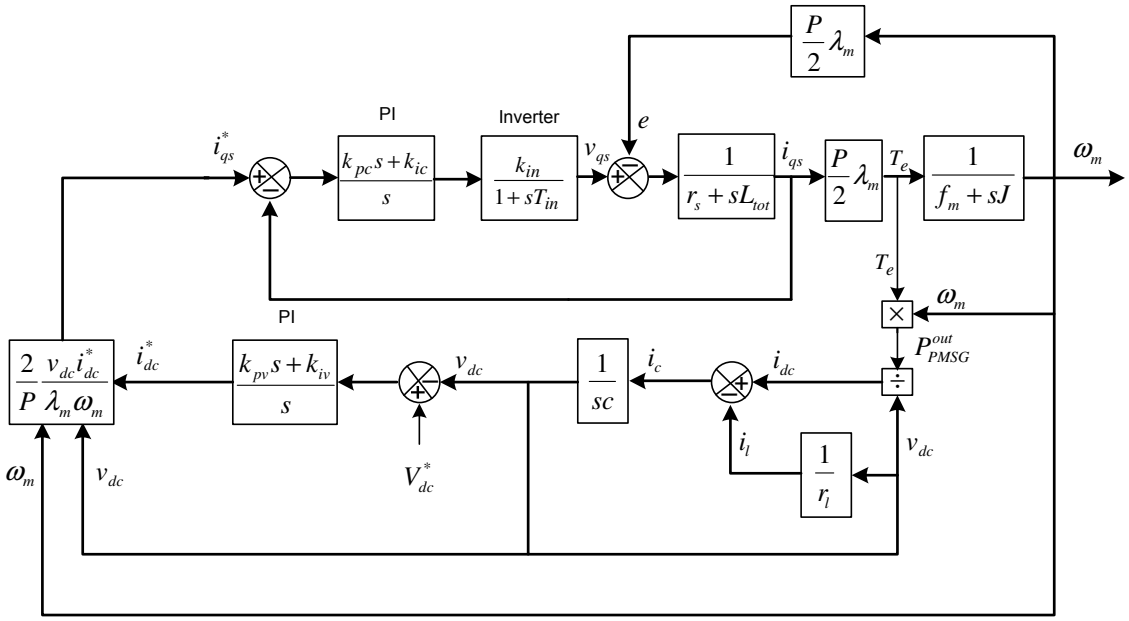


Figure 4-11 Block diagram of the DC bus voltage-controlled FESS.

4.4. Current-Loop Controller Design

The design of the current-controller is important for achieving the desired transient and steady-state characteristics for the FESS. Because of the high frequency harmonics of the phase current waves, a PI controller is sufficient. Selection of the values of gains of such a controller by using the new algorithm developed by Dr. S.P. Bhattacharyya [65-66] is performed as follows:

The closed loop characteristic polynomial is

$$\begin{aligned}\delta_c(s,k_{pc},k_{ic}) &= D_{pc}D_{cc}+N_{pc}N_{cc}\\ \delta_c(s,k_{pc},k_{ic}) &= d_{3c}s^4+d_{2c}s^3+(d_{1c}+k_{pc}n_{1c})s^2+(d_{0c}+n_{0c}k_{pc}+n_{1c}k_{ic})s+n_{0c}k_{ic}\end{aligned} \tag{4-17}$$

$\delta_c(s,k_{pc},k_{ic})$ can be divided into even and odd parts, however, in this case we will have the controller gains in both even and odd parts which complicates the problem. To simplify it, we form the new polynomial given by (4-18).

$$\begin{aligned}&\upsilon_c(s,k_{pc},k_{ic})=\delta_c(s,k_{pc},k_{ic})N_{pc}(-s)=\upsilon_{5c}s^5+\upsilon_{4c}s^4+\upsilon_{3c}s^3+\upsilon_{2c}s^2+\upsilon_{1c}s\\&+k_{pc}(-n_{1c}^2s^3+n_{0c}^2s)+k_{ic}(-n_{1c}^2s^2+n_{0c}^2)\end{aligned}\tag{4-18}$$

where

$$\begin{aligned}&\upsilon_{5c}=-d_{3c}n_{1c}\\&\upsilon_{4c}=d_{3c}n_{0c}-d_{2c}n_{1c}\\&\upsilon_{3c}=d_{2c}n_{0c}-d_{1c}n_{1c}\\&\upsilon_{2c}=d_{1c}n_{0c}-d_{0c}n_{1c}\\&\upsilon_{1c}=d_{0c}n_{0c}\end{aligned}\tag{4-19}$$

Note that the even-odd decomposition of $\upsilon_c(s,k_{pc},k_{ic})$ is:

$$\begin{aligned}&\upsilon_c(s,k_{pc},k_{ic})=\upsilon_c^{\,e}(s^2,k_{ic})+s\upsilon_c^{\,o}(s^2,k_{pc})\\&\upsilon_c^{\,e}(s^2,k_{ic})=\upsilon_{4c}s^4+\upsilon_{2c}s^2+k_{ic}(-n_{1c}^2s^2+n_{0c}^2)\\&\upsilon_c^{\,o}(s^2,k_{pc})=\upsilon_{5c}s^4+\upsilon_{3c}s^2+\upsilon_{1c}+k_{pc}(-n_{1c}^2s^2+n_{0c}^2)\end{aligned}\tag{4-20}$$

The polynomial $\upsilon_c(s,k_{pc},k_{ic})$ exhibits the parameters separation property. Namely, k_{pc} appears only in the odd part and k_{ic} only in the even part. Closed loop stability is achieved by fulfilling the requirement that the 4 zeros of $\delta_c(s,k_{pc},k_{ic})$ lie in the open LHP. This is equivalent to $\sigma_{\delta c}=4$ and $\sigma_{\upsilon c}=4+Z^+-Z^-=4+0-1=3$ where Z^+ (Z^-) denoted the number of RHP (LHP) zeros of the plant, that is, zeros of $N_{pc}(s)$. Obviously, there are no $j\omega$-axis zeros.

Based on this, we can develop the following procedure to calculate the set of PI controllers stabilizing the closed loop system [65-66]. First, fix $k_{pc}=k_{pc}^*$ and let

$0 < \omega_1 < \omega_2 < ... < \omega_{l-1}$ denote the real, positive, finite frequencies which are zeros of $\omega \upsilon_c^{\,o}(-\omega^2, k_{pc}^*) = 0$ of odd multiplicities. Let $\omega_0 = 0$, and determine strings of integers $i_0, i_1, ..., i_{l-1}$ such that

$$\sigma_{\upsilon_c} = 3 = sign[\upsilon_c^{\,o}(0, k_{pc}^*)]\{i_0 - 2i_1 + 2i_2 ....(-1)^{l-1} 2i_{l-1}\} \tag{4-21}$$

where υ_c is of odd degree and $i_o = \operatorname{sgn} \upsilon_{rc}(\omega_o), i_1 = \operatorname{sgn} \upsilon_{rc}(\omega_1), i_2 = \operatorname{sgn} \upsilon_{rc}(\omega_2) ..., i_{l-1} = \operatorname{sgn} \upsilon_{rc}(\omega_{l-1})$ and $\upsilon_{rc}(\omega)$ is the real part of the characteristic polynomial given by (4-22). Let $I_1, I_2, ...$ denote distinct strings $\{i_0, i_1, ...\}$ satisfying (4-21). The complete stabilizing set in (k_{pc}, k_{ic}) space can be found by sweeping k_{pc} over the real axis. From (4-21), we can see that the range of sweeping can be restricted to those values such that the number of roots, $l-1$ can satisfy (4-21). Therefore, $\omega \upsilon_c^{\,o}(-\omega^2, k_{pc}^*) = 0$ must have at least two real nonnegative roots including zero. It is obvious that $\omega \upsilon_c^{\,o}(-\omega^2, k_{pc}^*) = \upsilon_{ic}(\omega, k_{pc}^*)$ given by (4-22).

$$\begin{aligned}
&\upsilon_c(j\omega, k_{pc}, k_{ic}) = \upsilon_{rc}(\omega, k_{ic}) + j\upsilon_{ic}(\omega, k_{pc}) \\
&\upsilon_{rc}(\omega, k_{ic}) = \upsilon_c^{\,e}(-\omega^2, k_{ic}) = \upsilon_{4c}\omega^4 - \upsilon_{2c}\omega^2 + (n_{1c}^2\omega^2 + n_{0c}^2)k_{ic} \\
&\upsilon_{ic}(\omega, k_{pc}) = \omega \upsilon_c^{\,o}(-\omega^2, k_{pc}) = \omega[\upsilon_{5c}\omega^4 - \upsilon_{3c}\omega^2 + \upsilon_{1c} + (n_{1c}^2\omega^2 + n_{0c}^2)k_{pc}]
\end{aligned} \tag{4-22}$$

Solving (4-23) results in Figure 4-12 which demonstrates that for every positive k_{pc}, $\upsilon_{ic}(\omega, k_{pc}^*)$ has one real positive root and as a result it can satisfy (4-21).

$$\upsilon_{ic}(\omega, k_{pc}^*) = 0 \Rightarrow k_{pc}^* = -\frac{\upsilon_{5c}\omega^4 - \upsilon_{3c}\omega^2 + \upsilon_{1c}}{n_{1c}^2\omega^2 + n_{0c}^2} \tag{4-23}$$

Now we find the k_{ic} range for any fixed $0 \le k_{pc}^* < +\infty$ by solving the non-equalities given by (4-24).

$$
\begin{aligned}
&\text{if } sign[\upsilon_c{}^o(0,k_{pc}^*)]>0 \Rightarrow I_1=\{1,-1\} \Rightarrow \begin{cases}\upsilon_{rc}(\omega_0,k_{ic})>0\\ \upsilon_{rc}(\omega_1,k_{ic})<0\end{cases} \Rightarrow k_{ic}\\
&\text{if } sign[\upsilon_c{}^o(0,k_{pc}^*)]<0 \Rightarrow I_1=\{-1,1\} \Rightarrow \begin{cases}\upsilon_{rc}(\omega_0,k_{ic})>0\\ \upsilon_{rc}(\omega_1,k_{ic})<0\end{cases} \Rightarrow k_{ic}
\end{aligned}
\tag{4-24}
$$

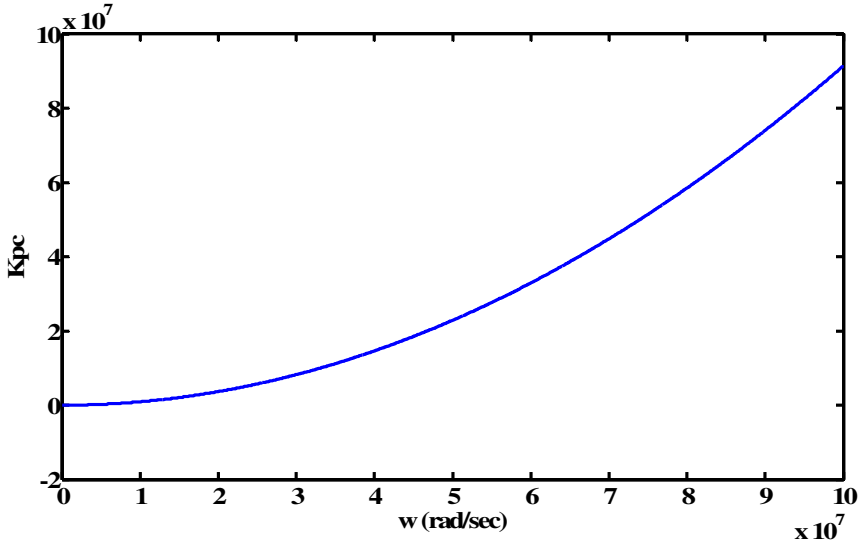


Figure 4-12 Range of k_{pc} which satisfies (4-23).

4.5. Speed-Loop Controller Design

The set of PI controllers which stabilizes the closed loop system are achieved in a similar manner to the current loop controller. Similarly, the closed loop characteristic polynomial is

$$
\begin{aligned}
&\delta_s(s,k_{ps},k_{is}) = D_{ps}D_{cs}+N_{ps}N_{cs}\\
&\delta_s(s,k_{ps},k_{is}) = d_{6s}s^7+d_{5s}s^6+d_{4s}s^5+d_{3s}s^4+(d_{2s}+n_{2s}k_{ps})s^3\\
&+(d_{1s}+n_{1s}k_{ps}+n_{2s}k_{is})s^2+(d_{0s}+n_{1s}k_{is}+n_{0s}k_{ps})s+n_{0s}k_{is}
\end{aligned}
\tag{4-25}
$$

To simplify the problem, we form the new polynomial

$$
\begin{aligned}
&\upsilon_s(s,k_{ps},k_{is}) = \delta_s(s,k_{ps},k_{is})N_{ps}(-s)\\
&\upsilon_s(s,k_{ps},k_{is}) = \upsilon_{9s}s^9+\upsilon_{8s}s^8+\upsilon_{7s}s^7+\upsilon_{6s}s^6+\upsilon_{5s}s^5+\upsilon_{4s}s^4+\upsilon_{3s}s^3+\upsilon_{2s}s^2+\upsilon_{1s}s\\
&+k_{ps}[n_{2s}^2s^5+(2n_{2s}n_{0s}-n_{1s}^2)s^3+n_{0s}^2s]\\
&+k_{is}[n_{2s}^2s^4+(2n_{2s}n_{0s}-n_{1s}^2)s^2+n_{0s}^2]
\end{aligned}
\tag{4-26}
$$

where

$$
\begin{aligned}
&\upsilon_{9s} = d_{6s}n_{2s}\\
&\upsilon_{8s} = d_{5s}n_{2s}-d_{6s}n_{1s}\\
&\upsilon_{7s} = d_{4s}n_{2s}-d_{5s}n_{1s}+d_{6s}n_{0s}\\
&\upsilon_{6s} = d_{3s}n_{2s}-d_{4s}n_{1s}+d_{5s}n_{0s}\\
&\upsilon_{5s} = d_{2s}n_{2s}-d_{3s}n_{1s}+d_{4s}n_{0s}\\
&\upsilon_{4s} = d_{1s}n_{2s}-d_{2s}n_{1s}+d_{3s}n_{0s}\\
&\upsilon_{3s} = d_{0s}n_{2s}-d_{1s}n_{1s}+d_{2s}n_{0s}\\
&\upsilon_{2s} = -d_{0s}n_{1s}+d_{1s}n_{0s}\\
&\upsilon_{1s} = d_{0s}n_{0s}
\end{aligned}
\tag{4-27}
$$

The even-odd decomposition of $\upsilon_s(s,k_{ps},k_{is})$ is:

$$
\begin{aligned}
&\upsilon_s(s,k_{ps},k_{is}) = \upsilon_s^{\,e}(s^2,k_{is})+s\upsilon_s^{\,o}(s^2,k_{ps})\\
&\upsilon_s^{\,e}(s^2,k_{is}) = \upsilon_{8s}s^8+\upsilon_{6s}s^6+\upsilon_{4s}s^4+\upsilon_{2s}s^2+k_{is}[n_{2s}{}^2s^4+(2n_{2s}n_{0s}-n_{1s}^2)s^2+n_{0s}{}^2]\\
&\upsilon_s^{\,o}(s^2,k_{ps}) = \upsilon_{9s}s^8+\upsilon_{7s}s^6+\upsilon_{5s}s^4+\upsilon_{3s}s^2+\upsilon_{1s}+k_{ps}[n_{2s}{}^2s^4+(2n_{2s}n_{0s}-n_{1s}^2)s^2+n_{0s}{}^2]
\end{aligned}
\tag{4-28}
$$

Closed loop stability is fulfilled by the requirement that the 7 zeros of $\delta_s(s,k_{ps},k_{is})$ lie in the open LHP. This is equivalent to $\sigma_{\delta s}=7$ and $\sigma_{\upsilon_s}=7+Z^+-Z^-=7+0-2=5$.Based on this, we can develop the following procedure to calculate the set of PIs stabilizing the closed loop system [65-66]. First, fix $k_{ps}=k_{ps}^*$ and let $0<\omega_1<\omega_2<...<\omega_{l-1}$ denote the real, positive, finite frequencies which are zeros of $\omega\upsilon_s^{\,o}(-\omega^2,k_{ps}^*)=0$ of odd multiplicities. Let $\omega_0=0$, and determine strings of integers $i_0,i_1,...,i_{l-1}$ such that

$$\sigma_{\upsilon_s} = 5 = sign[\upsilon_s{}^{o}(0, k_{ps}^{*})]\{i_0 - 2i_1 + 2i_2 ....(-1)^{l-1} 2i_{l-1}\} \tag{4-29}$$

Let $I_1, I_2, ...$ denote distinct strings $\{i_0, i_1, ...\}$ satisfying (4-29). The complete stabilizing set in (k_{ps}, k_{is}) space can be found by sweeping k_{ps} over the real axis. From (4-29), we can see that the range of sweeping can be restricted to those values such that the number of roots, $l-1$ can satisfy (4-29). Therefore, $\omega\upsilon_s{}^{o}(-\omega^2, k_{ps}^{*}) = 0$ must have at least 3 real nonnegative roots including zero in order to satisfy (4-29). Now we solve the $\omega\upsilon_s{}^{o}(-\omega^2, k_{ps}^{*}) = 0$ to construct $I_1, I_2, ...$ It is obvious that $\omega\upsilon_s{}^{o}(-\omega^2, k_{ps}^{*})$ is equal to $\upsilon_{is}(\omega, k_{ps}^{*})$ given by (4-30).

$$\begin{aligned}
&\upsilon_s(j\omega, k_{ps}, k_{is}) = \upsilon_{rs}(\omega, k_{is}) + j\upsilon_{is}(\omega, k_{ps}) \\
&\upsilon_{rs}(\omega, k_{is}) = \upsilon_s{}^{e}(-\omega^2, k_{is}) = \upsilon_{8s}\omega^8 - \upsilon_{6s}\omega^6 + \upsilon_{4s}\omega^4 - \upsilon_{2s}\omega^2 \\
&+k_{is}[n_{2s}{}^2\omega^4 - (2n_{2s}n_{0s} - n_{1s}^2)\omega^2 + n_{0s}{}^2] \\
&\upsilon_{is}(\omega, k_{ps}) = \omega\upsilon_s{}^{o}(-\omega^2, k_{ps}) = \omega[\upsilon_{9s}\omega^8 - \upsilon_{7s}\omega^6 + \upsilon_{5s}\omega^4 - \upsilon_{3s}\omega^2 + \upsilon_{1s} \\
&+k_{ps}[n_{2s}{}^2\omega^4 - (2n_{2s}n_{0s} - n_{1s}^2)\omega^2 + n_{0s}{}^2]
\end{aligned} \tag{4-30}$$

Solving (4-31) results in Figure 4-13 which demonstrates that for any k_{pc} in the range $0 \le k_{pc} \le 2.1\times10^6$, $\upsilon_{ic}(\omega, k_{pc}^{*})$ has two real positive roots and as a result it can satisfy (4-29).

$$\upsilon_{is}(\omega, k_{ps}^{*}) = 0 \Rightarrow k_{ps}^{*} = -\frac{\upsilon_{9s}\omega^8 - \upsilon_{7s}\omega^6 + \upsilon_{5s}\omega^4 - \upsilon_{3s}\omega^2 + \upsilon_{1s}}{n_{2s}{}^2\omega^4 - (2n_{2s}n_{0s} - n_{1s}^2)\omega^2 + n_{0s}{}^2} \tag{4-31}$$

Now we find the k_{ic} range for any fixed $0 \le k_{ps}^{*} < 2.1\times10^6$ by solving the non-equalities given by (4-32).

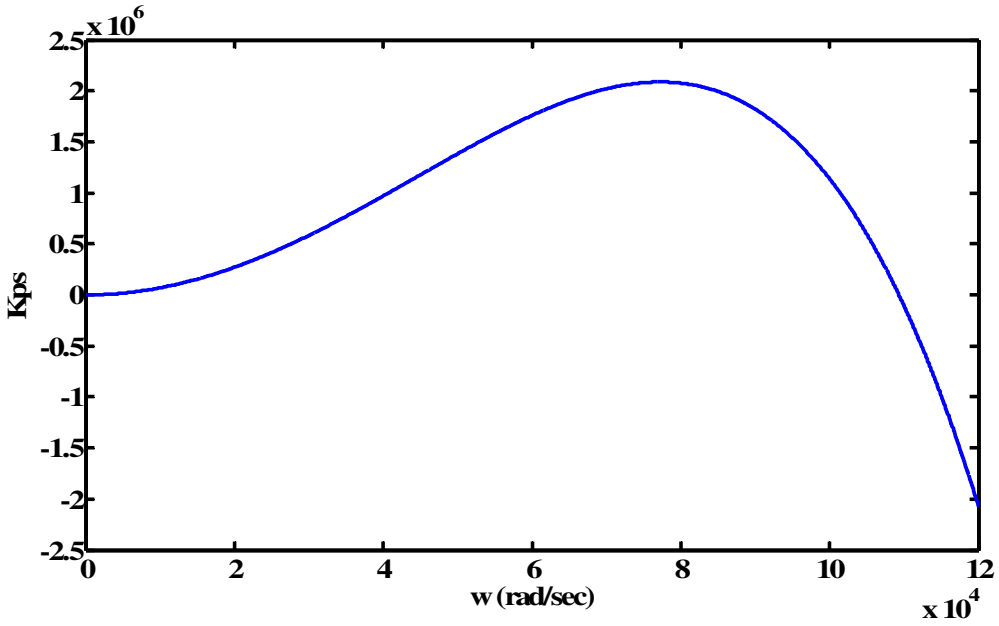


Figure 4-13 Range of k_{pc} which satisfies (4-29).

$$
\begin{aligned}
&\text{if } sign[\upsilon_s^{\,o}(0,k_{ps}^*)]>0 \Rightarrow I_1=\{1,-1,1\} \Rightarrow \begin{cases} \upsilon_{rs}(\omega_0,k_{is})>0 \\ \upsilon_{rs}(\omega_1,k_{is})<0 \\ \upsilon_{rs}(\omega_2,k_{is})>0 \end{cases} \Rightarrow k_{is} \\
&\text{if } sign[\upsilon_s^{\,o}(0,k_{ps}^*)]<0 \Rightarrow I_1=\{-1,1,-1\} \Rightarrow \begin{cases} \upsilon_{rs}(\omega_0,k_{is})<0 \\ \upsilon_{rs}(\omega_1,k_{is})>0 \\ \upsilon_{rs}(\omega_2,k_{is})<0 \end{cases} \Rightarrow k_{is}
\end{aligned}
\qquad (4\text{-}32)
$$

4.6. Voltage-Loop Controller Design

Figure 4-11 represents a non-linear behavior by the DC-bus voltage controller. As a result the method used for the design of PI controllers of the current-loop and speed-loop controllers can not be implemented here.

Essentially, in the voltage-loop, the PI controller is producing a current command which will force the voltage on the capacitor to the desired value. The first-guess gains of the PI controller can be set by using pole-zero cancellation where $k_{pv}/k_{iv}=1/r_l c$

and $k_{pv} = 2\pi r_l c f_{bw}$ [37]. A high bandwidth, f_{bw}, is not necessary because of the disturbance decoupling in the total controller.

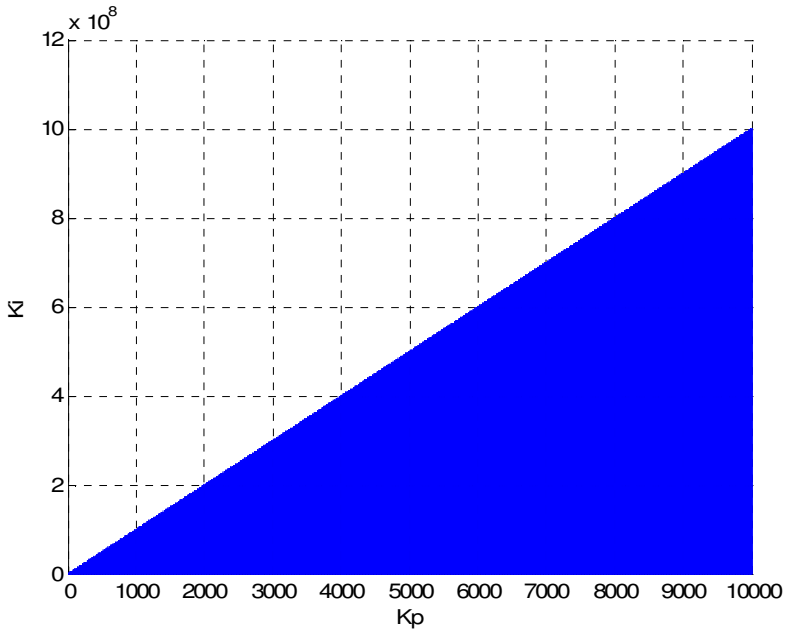
4.7. Set of PI Controllers

The parameters of the FESS shown in Figure 2-1 and the desired operation are presented in Table 3-3. The set of PI controllers for the current-loop controller is depicted in Figure 4-14(a). Selecting the gains $(k_{pc} = 10, k_{ic} = 1000)$ from the set, Figure 4-14(b) represents the set of PI controllers for the speed-loop controller. The gains of the voltage-loop PI controller can be set by using pole-zero cancellation as discussed before.

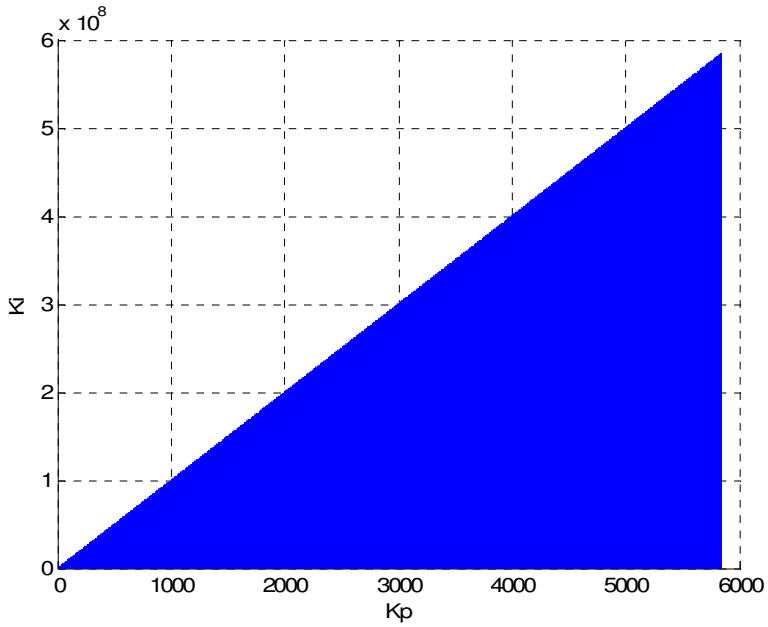
$$\begin{aligned} k_{pv} / k_{iv} &= 1 / r_l c = 1 / (.04 \times .024) = 40 \\ k_{pv} &= 2\pi r_l c f_{bw} = 2\pi \times 1.04 \times .024 \times 8000 = 1250 \end{aligned} \tag{4-33}$$

The 240 kW, 19 to 23 krpm FESS with its control system depicted in Figure 4-7 is modeled using PSIM package and both charging and discharging modes are simulated. Figure 4-15 shows transients of the q-axis current, speed, electromagnetic torque, output power, and the DC bus voltage at the beginning of the discharging mode at 240 kW load cycle which is the most critical moment of the operation. This operation is experienced just by two points out of the two sets of PI controllers, $(k_{pc} = 10, k_{ic} = 1000), (k_{ps} = 400, k_{is} = 4000)$ and $(k_{pv} = 1250, k_{iv} = 31)$. Obviously, the FESS represents a fast dynamic behavior and rapidly tracks the desired operation. As it is depicted in Figure 4-15, the q-axis current, speed, electromagnetic torque, and output power rapidly track the desired values in less than 0.5 msec without any overshoot or undershoot. The DC bus voltage response shown in Figure 4-15 (d) reaches the desired value, 500 V, in less than 20 msec and keeps the voltage in a narrow band, 0.2%, at the

discharging duration. At the beginning of the regenerative mode, the minimum DC bus voltage is 492 V, 98% of the rating value.

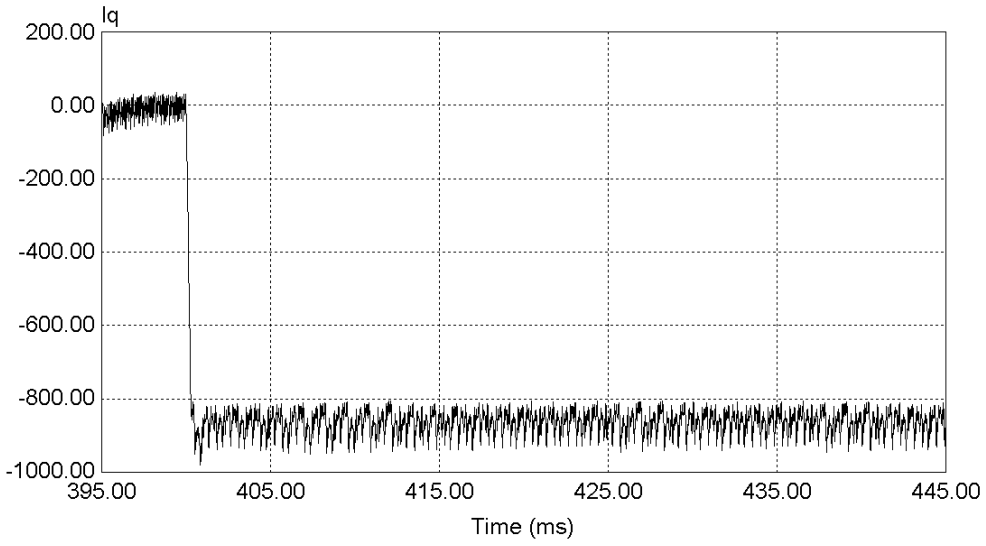


(a)

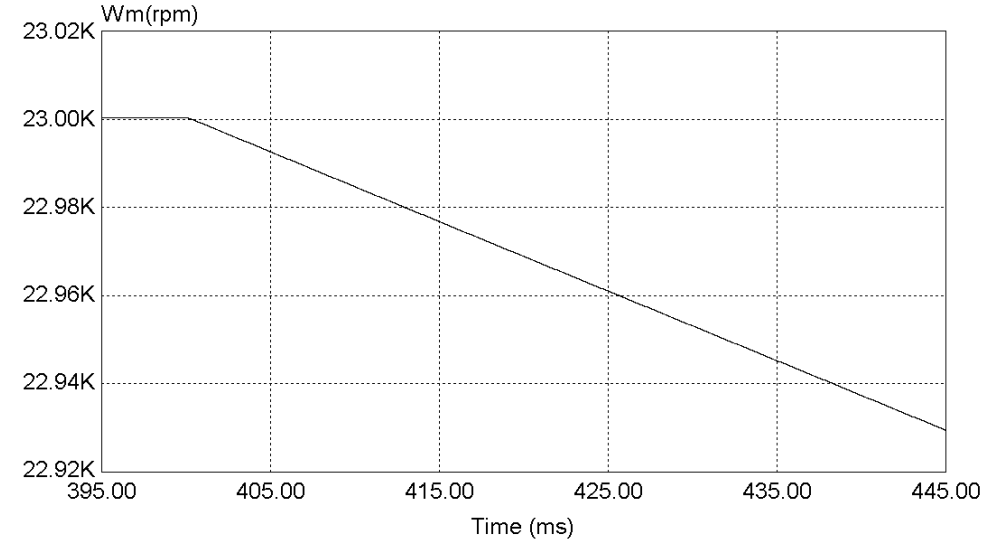


(b)

Figure 4-14 Set of PI controllers, (a) for the current loop, (b) for the speed loop.

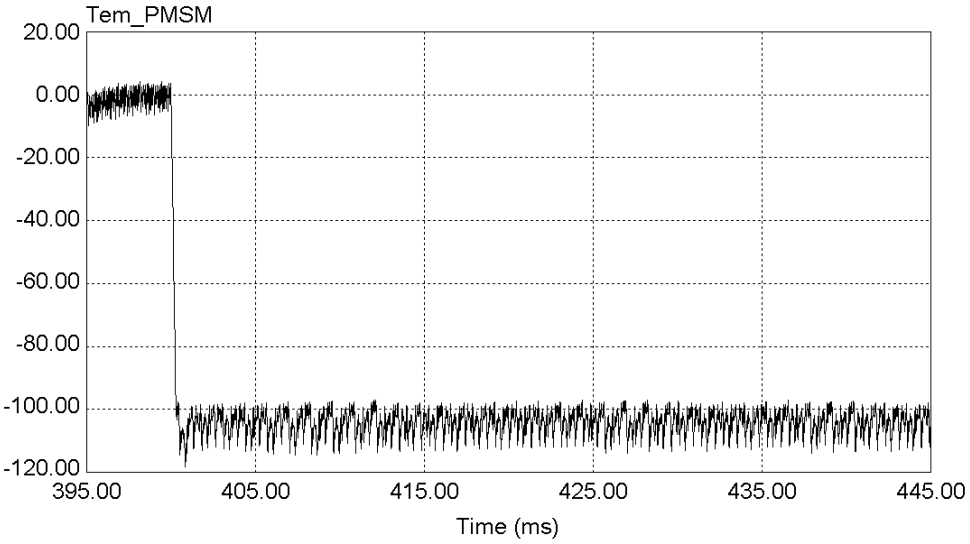


(a)

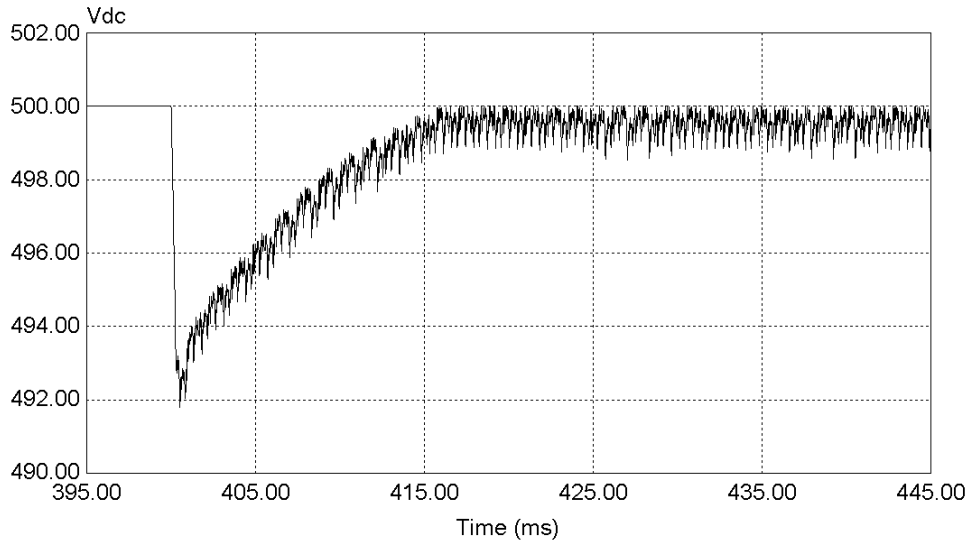


(b)

Figure 4-15 At the beginning of discharging mode,
(a) q-axis current (A), (b) Motor speed (krpm), (c) Electromagnetic torque (N.m),
(d) DC bus voltage (V), (e) Output power (MW), (f) Phase current (A).

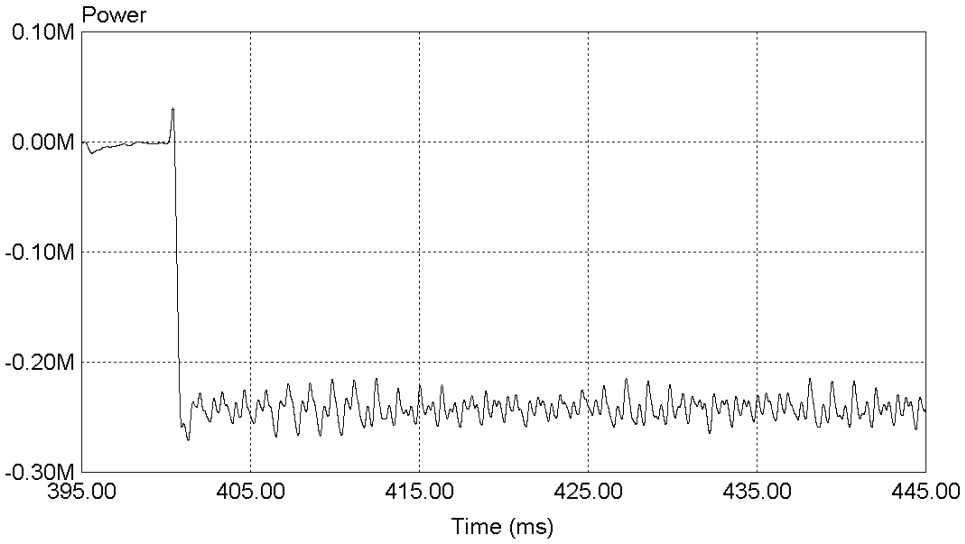


(c)

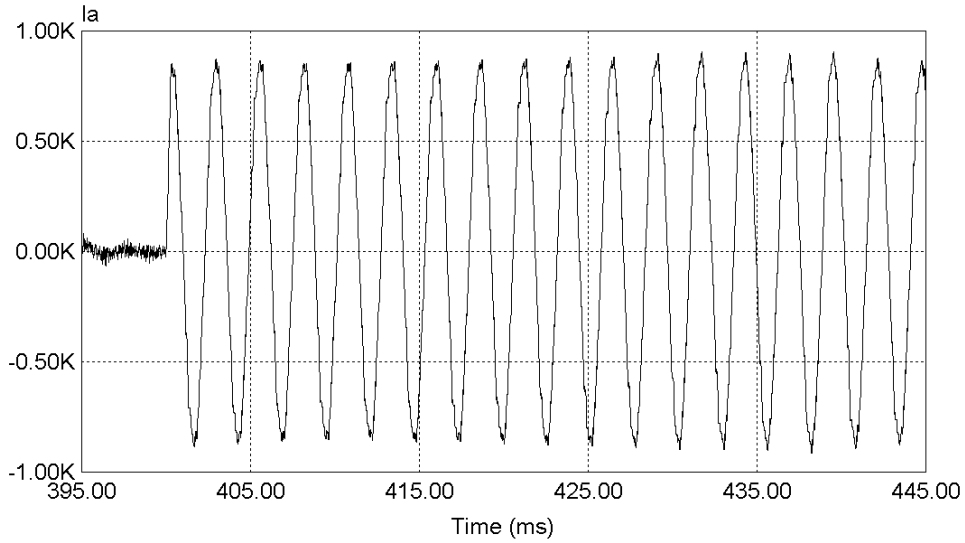


(d)

Figure 4-15 Continued.



(e)



(f)

Figure 4-15 Continued.

4.8. Simulation Results

The FESS along with its control system is simulated for both charging and discharging modes of operations. The block diagram of the controlled FESS is illustrated in Figure 4-7. The parameters of the PMSM and the FESS desired performance is

presented in Table 3-3. The simulation results are summarized in Table 4-3 and Table 4-4 at the PMSM and the rectifier terminals, respectively. Figures 4-16 to 4-19 illustrate the simulation results in time domain.

Table 4-3 240 kW FESS charging in 58 sec and discharging in 2 sec (PMSM output/input).

Mode	Sw. Freq. (kHz)	Ext. Ind. (uH)	Speed (rpm)	Line Voltage (Vrms)	Line Current (Arms)	DPF	PF	Output Power (kW)	THD (%)
Discharging	5	0	23000	315	616	-0.73	-0.62	240	5
	5	0	19000	305	750	-0.62	-0.5	240	8
Charging	8	150	23000	235	24	1	0.92	9.9	25
	8	150	19000	195	24	1	0.88	8.4	22

Table 4-4 240 kW FESS charging in 58 sec and discharging in 2 sec (Rectifier input/inverter output).

Mode	Sw. Freq. (kHz)	Ext. Ind. (uH)	Speed (rpm)	Line Voltage (Vrms)	Line Current (Arms)	DPF	PF	Cap. Ripple Current (Arms)
Discharging	5	0	23000	315	616	-0.73	-0.62	303
	5	0	19000	305	750	-0.62	-0.5	405
Charging	8	150	23000	240	24	1	0.7	2.5
	8	150	19000	193	24	1	0.62	2.5

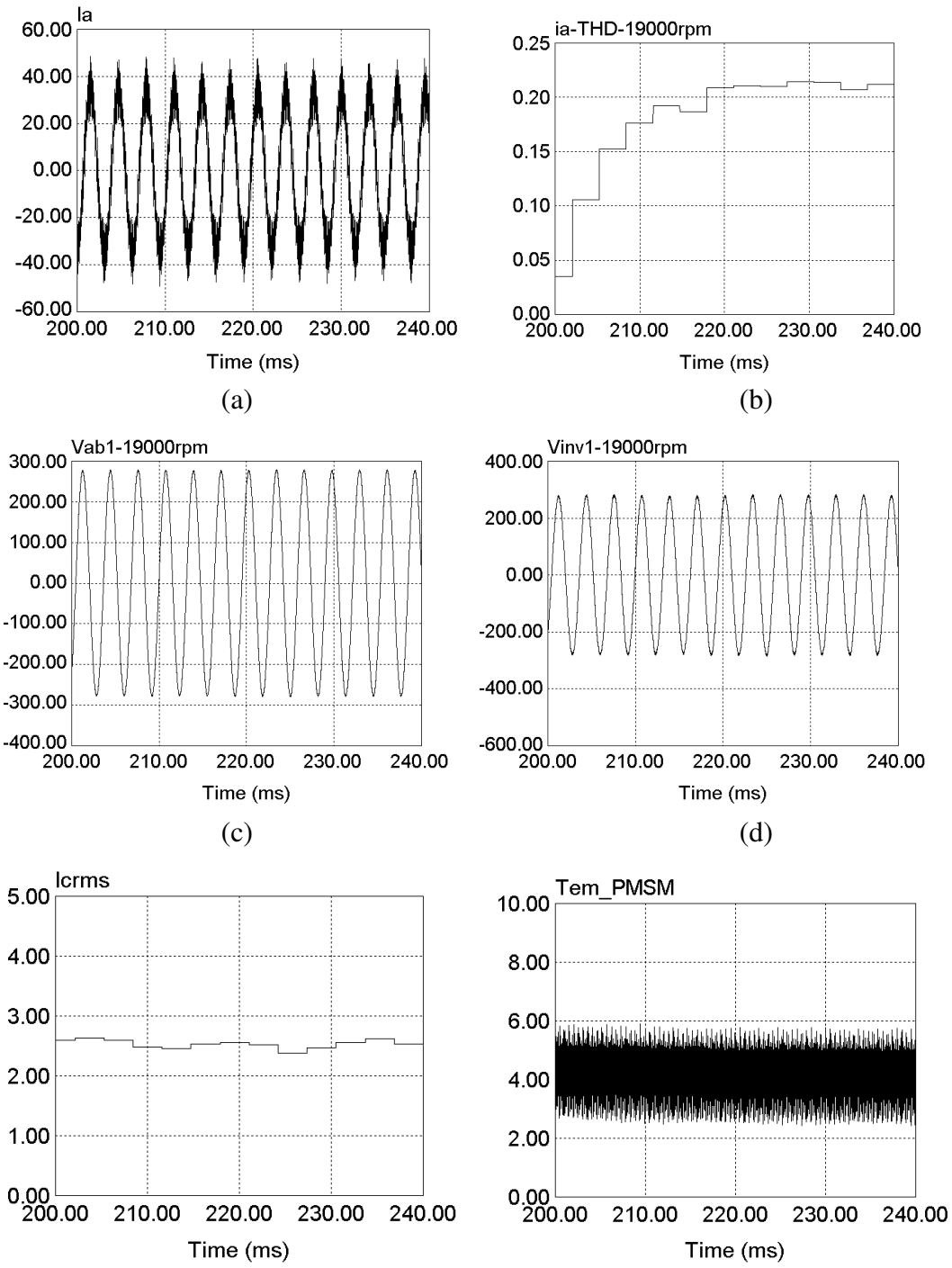


Figure 4-16 Charging of the FESS at 19 krpm,
a) Phase current b) Phase current THD c) Fundamental component of the PMSM line voltage d) Fundamental component of the inverter line voltage e) DC bus capacitor current (rms) f) Electromagnetic torque of the PMSM g) Absorbed power by the PMSM h) PMSM speed i) Power factor (PF) at the PMSM terminal j) Power factor (PF) at the inverter terminal.

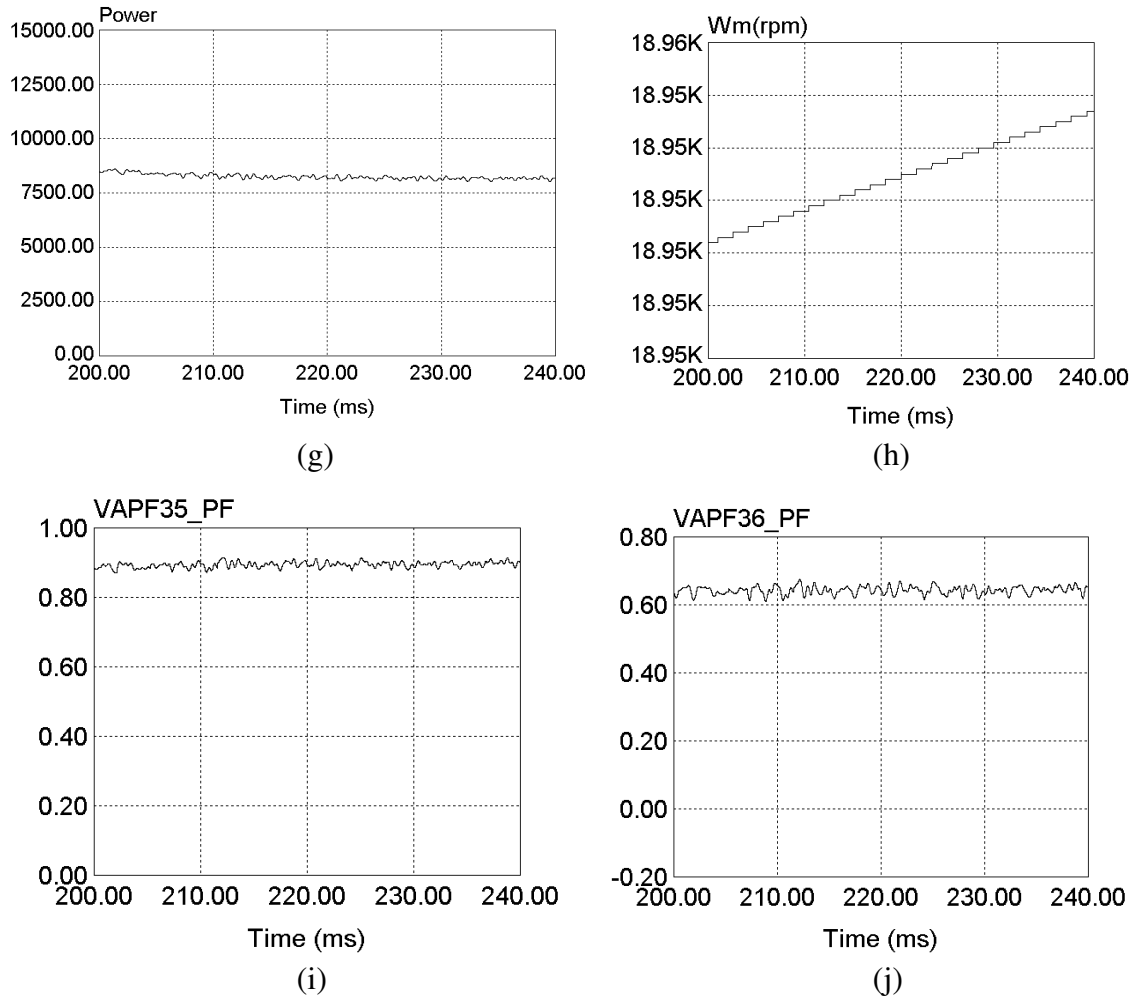


Figure 4-16 Continued.

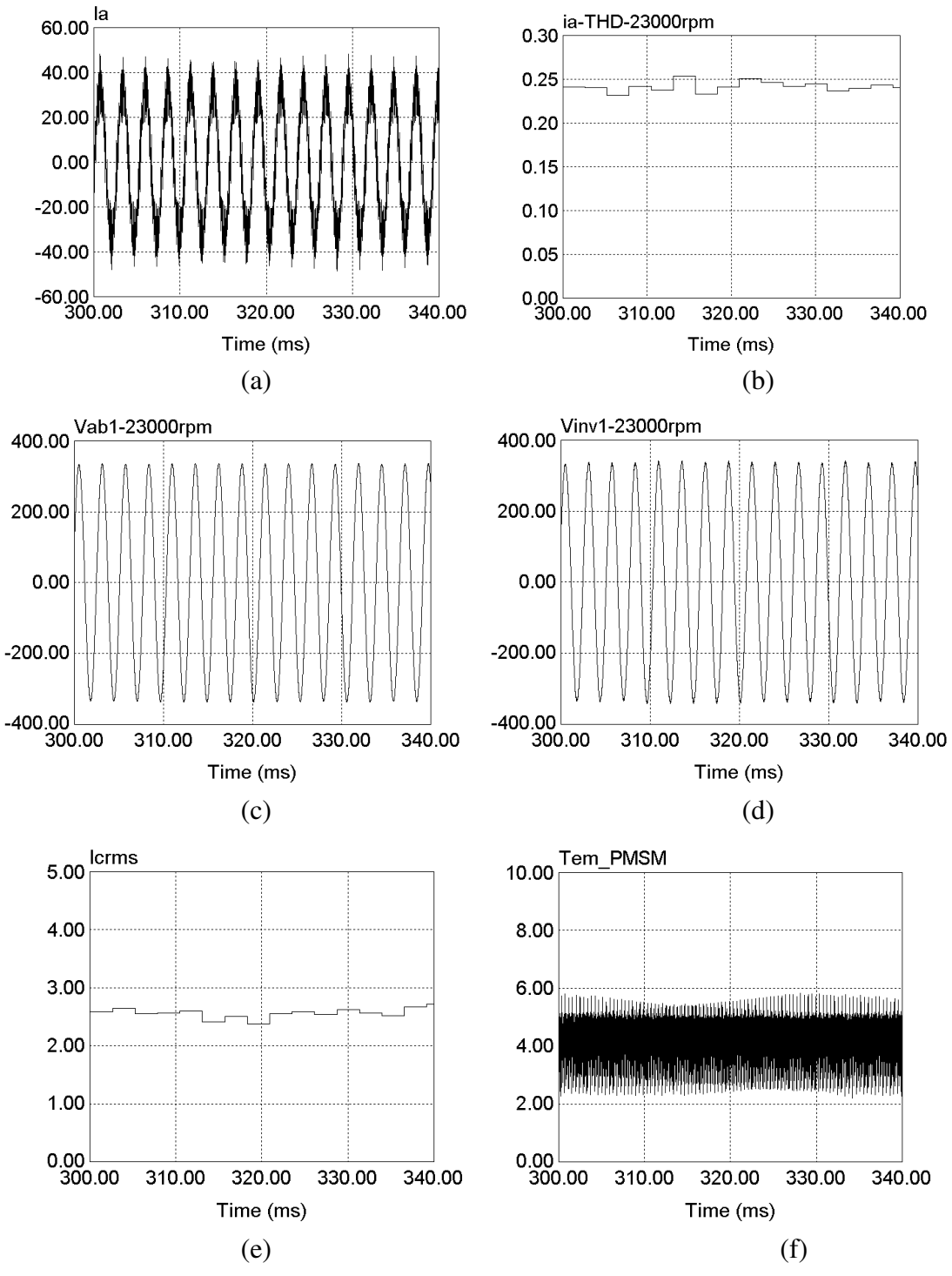
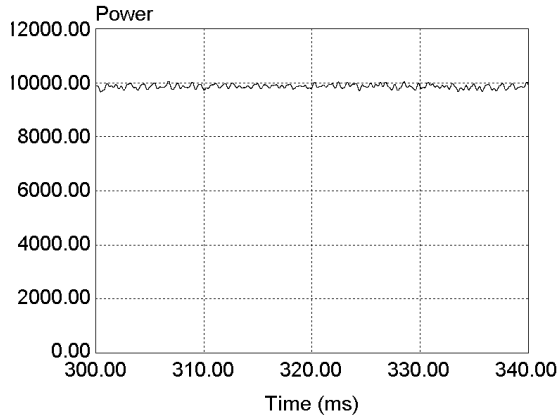


Figure 4-17 Charging of the FESS at 23 krpm,
a) Phase current b) Phase current THD c) Fundamental component of the PMSM line voltage d) Fundamental component of the inverter line voltage e) DC bus capacitor current (rms) f) Electromagnetic torque of the PMSM g) Absorbed power by the PMSM h) PMSM speed i) Power factor (PF) at the PMSM terminal j) Power factor (PF) at the inverter terminal.



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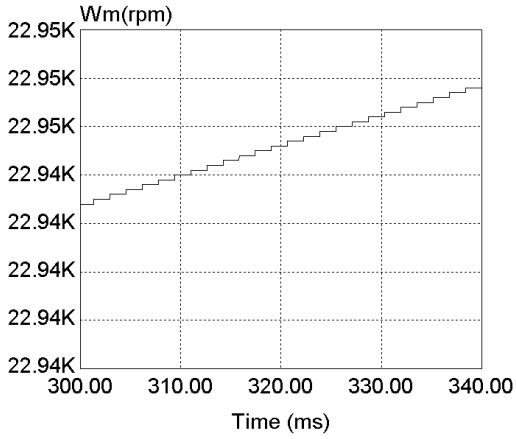

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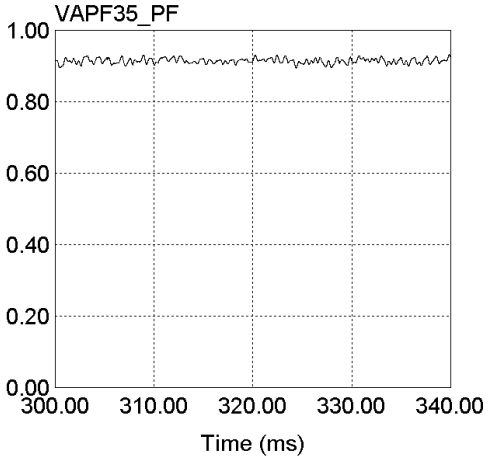
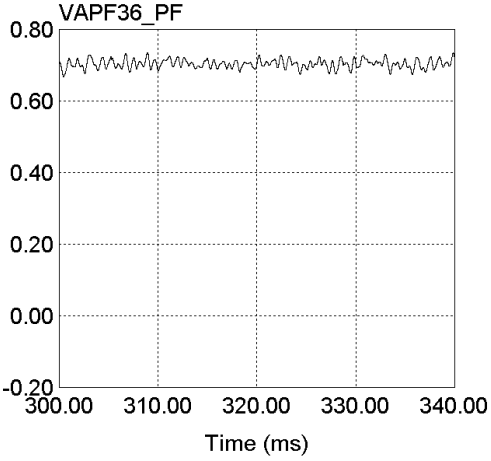


(i)



(j)

Figure 4-17 Continued.

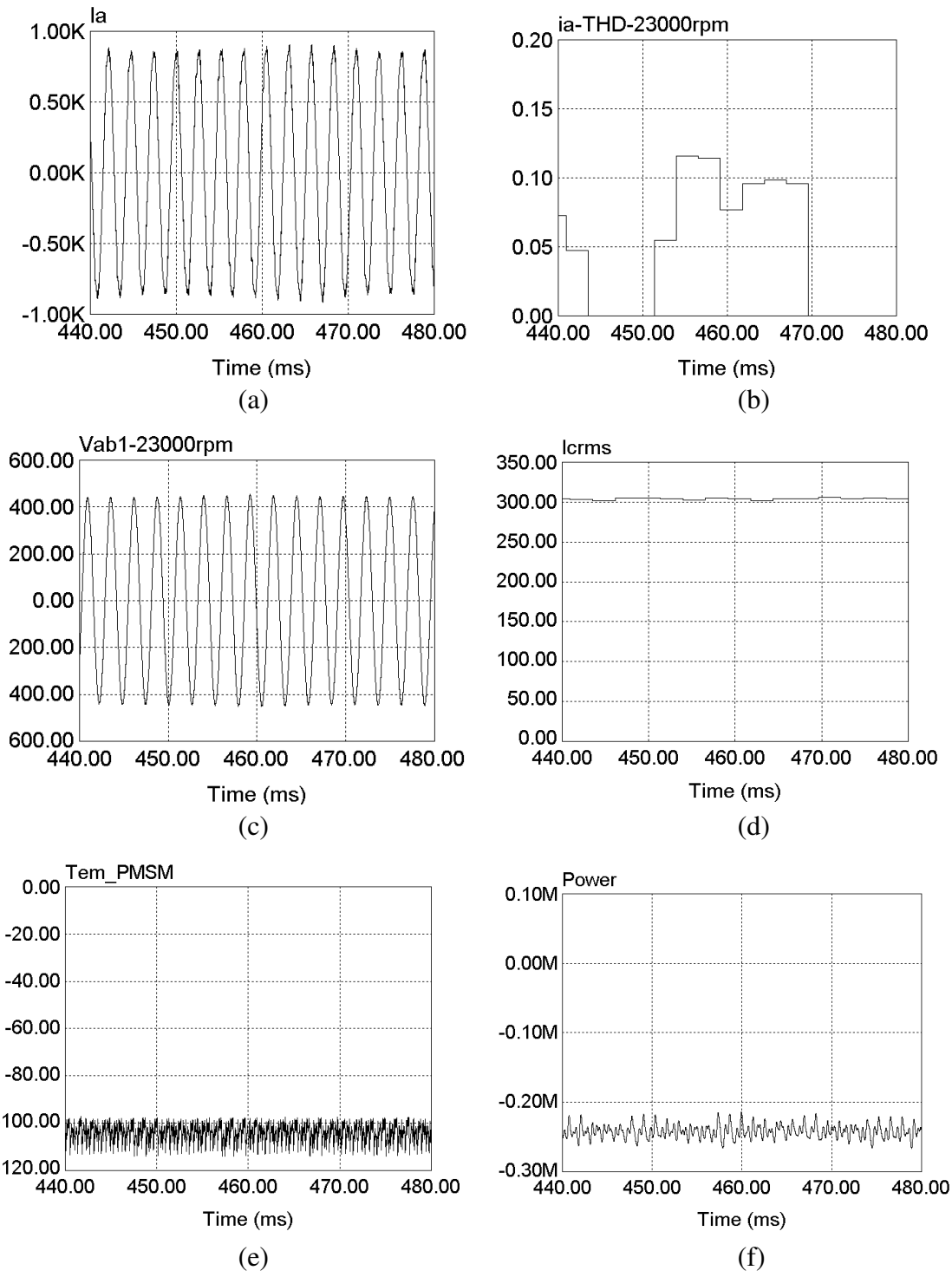
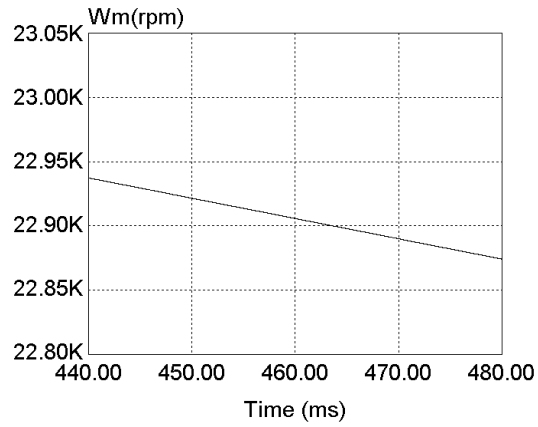


Figure 4-18 Discharging of the FESS at 23 krpm,
a) Phase current b) Phase current THD c) Fundamental component of the PMSM (rectifier) line voltage d) DC bus capacitor current (rms) e) Electromagnetic torque of the PMSM f) Output power of the PMSM g) PMSM speed h) Power factor (PF) at the PMSM (rectifier) terminal (i) DC bus voltage.



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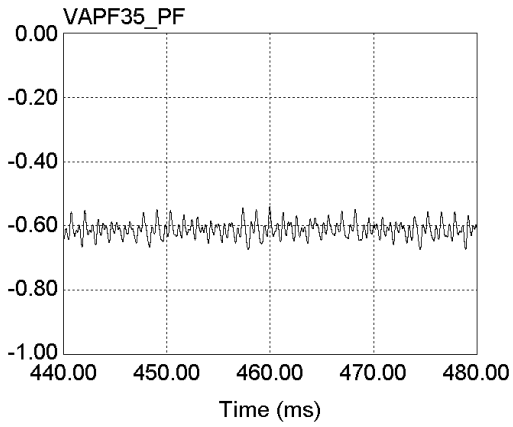

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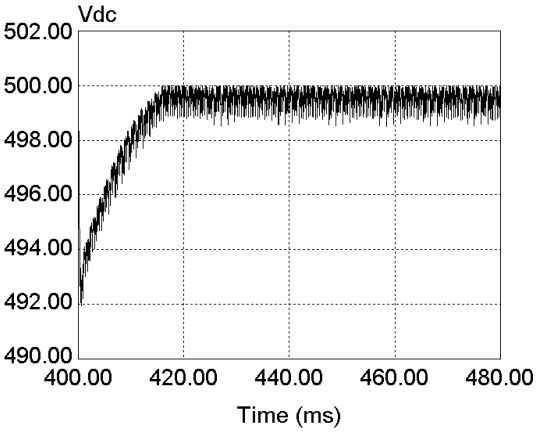
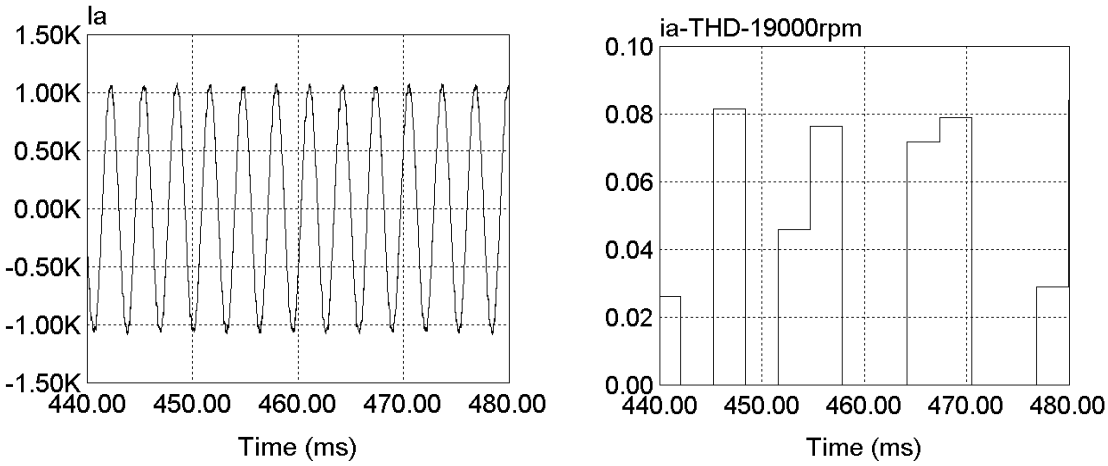


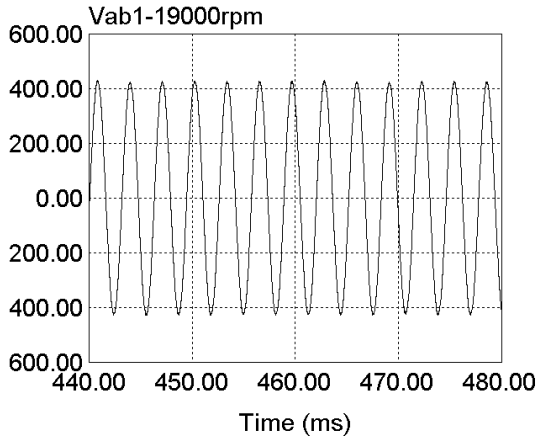
(i)

Figure 4-18 Continued.



(a)

(b)



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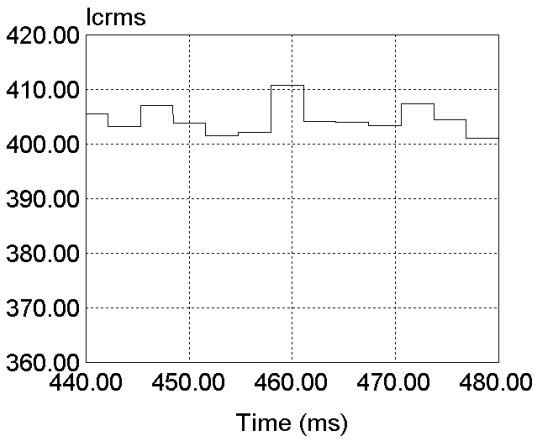
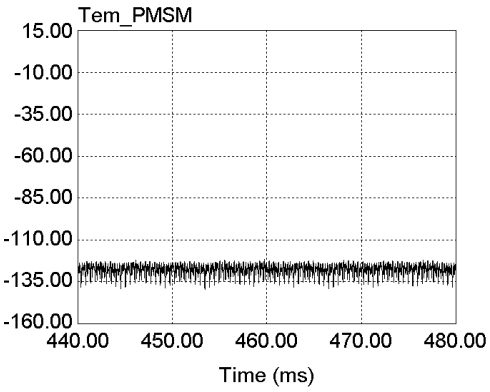
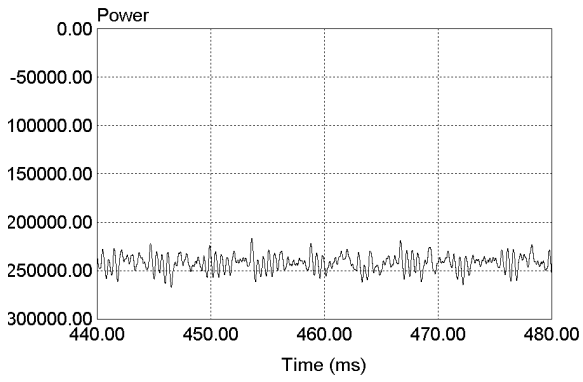


(d)

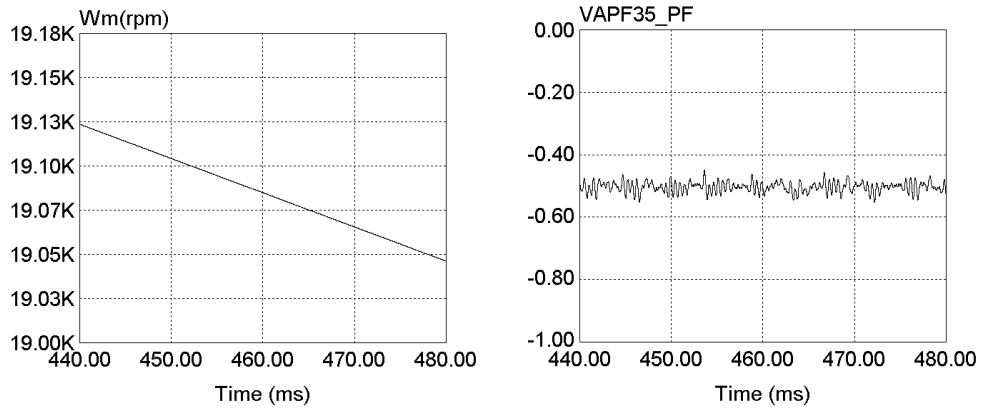


(e)



(f)

Figure 4-19 Discharging of the FESS at 19 krpm,
a) Phase current b) Phase current THD c) Fundamental component of the PMSM (rectifier) line voltage d) DC bus capacitor current (rms) e) Electromagnetic torque of the PMSM f) Output power of the PMSM g) PMSM speed h) Power factor (PF) at the PMSM (rectifier) terminal (i) DC bus voltage.



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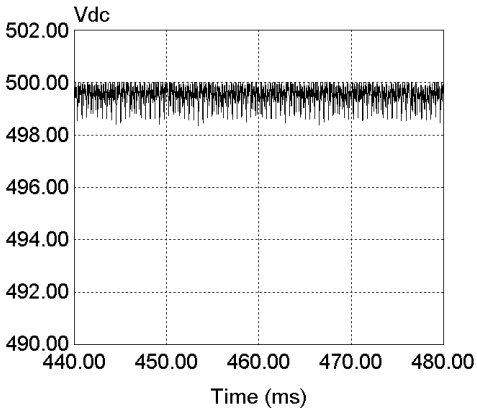


(i)

Figure 4-19 Continued.

4.9. Comparison Between PSIM Simulation and Analytical Results

To verify the precision of the analytical model derived in Sections 2 and 3, the FESS (The parameters of the FESS is given in Table 3-3) is simulated using PSIM package in previous section. In addition, the analytical model was used in Section 3 to simulate the DC operating points. Table 4-5 shows the results all together. The analytical results and the simulation results are in complete agreement, except for the reactive power and the PFs. The reason is due to ignoring harmonics in modeling the PWM inverter/rectifier. So if the external inductor or the PMSM inductors are larger, the analytical model results will be in a close agreement with the simulation results.

Table 4-5 PSIM and analytical model simulation results.

Tool	PSIM				Analytical Model			
Mode	Discharging		Charging		Discharging		Charging	
ω_r (krpm)	19	23	19	23	19	23	19	23
I_{qs} (A)	1298	1067	42	42	1296	1051	46	46
I_{ds} (A)	0	0	0	0	0	0	0	0
I_{as} (A)	750	616	24	24	748	607	27	27
V_s (V)	305	315	193	240	300	325	197	239
PF	-0.5	-0.62	0.88	0.92	-0.64	-0.72	0.99	0.99
DPF	-0.62	-0.73	1	1	-0.64	-0.72	0.99	0.99
P_{inv}^{out} (kW)	N/A	N/A	8.4	9.9	N/A	N/A	9.1	11
Q_{inv}^{out} (kVAR)	N/A	N/A	3.9	4.22	N/A	N/A	1.0	1.2
P_{rec}^{in} (kW)	240	240	N/A	N/A	240	240	N/A	N/A
Q_{rec}^{in} (kVAR)	-416	-304	N/A	N/A	-305.11	-243	N/A	N/A
M	0.61	0.63	0.39	0.48	0.6	0.65	0.39	0.48
THD (%)	8	5	22	25	0	0	0	0

5. INVERTER DESIGN, FABRICATION AND FEATURES

In this section, first, based on the nominal ratings of the FESS and the thermal analysis the appropriate device is selected. Then according to the DC bus nominal voltage, its acceptable ripple, and most significantly capacitor ripple current, the DC bus capacitor is selected. Finally, the features of the fabricated inverter are described.

5.1. Selection of the Device

The DC bus nominal voltage is 500 Vdc and the maximum over-voltage should not be more than +60 V. Based on the simulation results presented in Section 4, the maximum fundamental component of the PMSM phase current during the worst discharging mode of operation, at 240 kW and 19 krpm, is 1060 A-peak. Considering the relevant current ripple, the absolute maximum current will be even higher than 1060 A. Based on these data, SKiiP1242GB120-4DU(D)L was the primary choice of the device. The maximum ratings of the continuous current and break down voltage of the device are 1200 A and 900 V which meet the desired ratings of the FESS. The data sheet of the device is shown in Table 5-1 [67].

Note that the following advantages verify that why a SKiiP (Semikron integrated intelligent Power) type device, regardless of the device part number, could be a proper choice for the application [68]. Main characteristics of the SKiiP are:

- SKiiP integrates power semiconductor switches, heatsink and gate driver unit with protection and monitoring circuit.

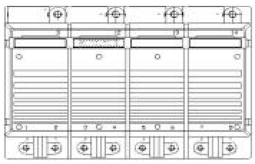
- Based on SKiiP pressure contact technology, a compact power module design with very low thermal resistances, high thermal cycling capability and low parasitic stray inductances are achievable.
- SkiiP is equipped with closed loop current sensors, used for short circuit and over-current protection.
- Normalized analog voltage signals of the actual AC current value, the actual ceramic substrate temperature value and the actual DC-link voltage value are available at the gate driver connector of the SKiiP for use in the control unit.
- Low switching over-voltages due to thorough low-inductive structure, i.e. high permissible DC link voltage and reduction of interference generation.
- Repairable and recyclable by excluding hard moulding and internal soldering optimal adjustment of internal intelligent driver.
- Load test of complete systems carried out at manufacturer, Semikron.

In the next step thermal analysis is done using SemiSel package to verify that the device meets the thermal limit. The thermal analysis illustrated in Figure 5-1 shows that the device junction temperature doesn't go above 80 ^{o}C under 240 kW load cycle. Note that the maximum limit for the junction temperature is 115~120 ^{o}C which is far above the thermal analysis results.

Some devices with lower ratings such as SKiiP942GB120 also meet the thermal limits as well, but as they are not much different from price point of view, SKiiP1242GB120-4DU(D)L has been chosen finally. As a result, higher reliability and safety margins are obtainable.

Table 5-1 Datasheet of device SKiiP1242GB120-4DU(D)L [67].

SKiiP 1242GB120-4D



SKiiP® 2

2-pack - integrated intelligent Power System

Power section

SKiiP 1242GB120-4D

Power section features

- SKiiP technology inside
- CAL diode technology
- Integrated current sensor
- Integrated temperature sensor
- Integrated heat sink
- IEC 60721-3-3 (humidity) class 3K3/IE32 (SKiiP® 2 System)
- IEC 60068-1 (climate) 40/125/56
- UL recognized file no. E63532

1) with assembly of suitable MKP capacitor per terminal

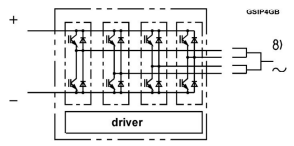
8) AC connection busbars must be connected by the user; copper busbars available on request

Absolute Maximum Ratings		T_s = 25 °C unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
IGBT			
V_{CES}		1200	V
V_{CC} 1)	Operating DC link voltage	900	V
V_{GES}		± 20	V
I_C	T_s = 25 (70) °C	1200 (900)	A
Inverse diode			
I_F = - I_C	T_s = 25 (70) °C	1200 (900)	A
I_{FSM}	T_j = 150 °C, t_p = 10 ms; sin.	8640	A
I²t (Diode)	Diode, T_j = 150 °C, 10 ms	373	kA²s
T_j, (T_{stg})		- 40 (- 25) ... + 150 (125)	°C
V_{isol}	AC, 1 min. (mainterminals to heat sink)	3000	V

Characteristics		T_s = 25 °C unless otherwise specified			
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
IGBT					
V_{CEsat}	I_C = 1000 A, T_j = 25 (125) °C		2,6 (3,1)	3,1	V
V_{CEO}	T_j = 25 (125) °C		1,2 (1,3)	1,5 (1,6)	V
r_{CE}	T_j = 25 (125) °C		1,3 (1,8)	1,6 (2)	mΩ
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}, T_j = 25 (125) °C		(60)	1,6	mA
E_{on} + E_{off}	I_C = 1000 A, V_{CC} = 600 V			300	mJ
	T_j = 125 °C, V_{CC} = 900 V			529	mJ
$R_{CC'+EE'}$	terminal chip, T_j = 125 °C		0,13		mΩ
L_{CE}	top, bottom		3,8		nH
C_{CHC}	per phase, AC-side		5,6		nF
Inverse diode					
V_F = V_{EC}	I_F = 1000 A, T_j = 25 (125) °C		2,1 (2)	2,6	V
V_{TO}	T_j = 25 (125) °C		1,3 (1)	1,4 (1,1)	V
r_T	T_j = 25 (125) °C		0,8 (1)	1,1 (1,3)	mΩ
E_{rr}	I_C = 1000 A, V_{CC} = 600 V			39	mJ
	T_j = 125 °C, V_{CC} = 900 V			49	mJ
Mechanical data					
M_{dc}	DC terminals, SI Units	6		8	Nm
M_{ac}	AC terminals, SI Units	13		15	Nm
w	SKiiP® 2 System w/o heat sink		3,5		kg
w	heat sink		8,5		kg

Thermal characteristics (P16 heat sink; 275m³/h); "$_r$ " reference to temperature sensor

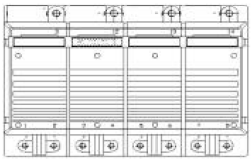
$R_{th(j-s)I}$	per IGBT						0,023	K/W
$R_{th(j-s)D}$	per diode						0,063	K/W
$R_{th(s-a)}$	per module						0,033	K/W
Z_{th}	R_i (mK/W) (max. values)				tau$_i$(s)			
	1	2	3	4	1	2	3	4
$Z_{th(j-r)I}$	2	18	3	0	1	0,13	0,001	1
$Z_{th(j-r)D}$	7	48	8	0	1	0,13	0,001	1
$Z_{th(r-a)}$	1,6	22	7	2,4	494	165	20	0,03



Case S 4

Table 5-1 Continued.

SKiiP 1242GB120-4D



SKiiP® 2

Absolute Maximum Ratings		T_a = 25 °C unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
V_{S1}	stabilized 15 V power supply	18	V
V_{S2}	unstabilized 24 V power supply	30	V
V_{iH}	input signal voltage (high)	15 + 0,3	V
dv/dt	secondary to primary side	75	kV/µs
V_{isolIO}	input / output (AC, r.m.s., 2s)	3000	Vac
V_{isol12}	output 1 / output 2 (AC, r.m.s., 2s)	1500	Vac
f_{sw}	switching frequency	14	kHz
f_{out}	output frequency for I=I_C ;sin.	1	kHz
T_{op} (T_{stg})	operating / storage temperature	- 40 ... + 85	°C

2-pack - integrated intelligent Power System

2-pack
integrated gate driver

SKiiP 1242GB120-4D

Gate driver features

- CMOS compatible inputs
- Wide range power supply
- Integrated circuitry to sense phase current, heat sink temperature and DC-bus voltage (option)
- Short circuit protection
- Over current protection
- Over voltage protection (option)
- Power supply protected against under voltage
- Interlock of top/bottom switch
- Isolation by transformers
- Fibre optic interface (option for GB-types only)
- IEC 60068-1 (climate) 25/85/56

Characteristics					(T_a = 25 °C)
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
V_{S1}	supply voltage stabilized	14,4	15	15,6	V
V_{S2}	supply voltage non stabilized	20	24	30	V
I_{S1}	V_{S1} = 15 V		290+580*f/f_{max}+1,2*(I_{AC}/A)		mA
I_{S2}	V_{S2} = 24 V		220+420*f/f_{max}+0,85*(I_{AC}/A)		mA
V_{iT+}	input threshold voltage (High)			12,3	V
V_{iT-}	input threshold voltage (Low)	4,6			V
R_{IN}	input resistance		10		kΩ
$t_{d(on)IO}$	input-output turn-on propagation time			1,5	µs
$t_{d(off)IO}$	input-output turn-off propagation time			1,4	µs
$t_{pERRRESET}$	error memory reset time	9			µs
t_{TD}	top / bottom switch : interlock time		3,3		µs
$I_{analogOUT}$	8 V corresponds to max. current of 15 V supply voltage		1200		A
$I_{Vs1outmax}$	(available when supplied with 24 V)			50	mA
I_{A0max}	output current at pin 12/14			5	mA
V_{0l}	logic low output voltage			0,6	V
V_{0H}	logic high output voltage			30	V
I_{TRIPSC}	over current trip level ($I_{analog\ OUT}$ = 10 V)		1500		A
I_{TRIPLG}	ground fault protection				A
T_{tp}	over temperature protection	110		120	°C
U_{DCTRIP}	trip level of U_{DC}-protection ($U_{analog\ OUT}$ = 9 V); (option)	900			V

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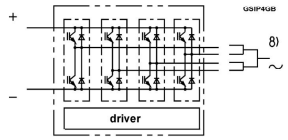
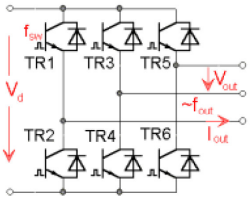


Case S 4

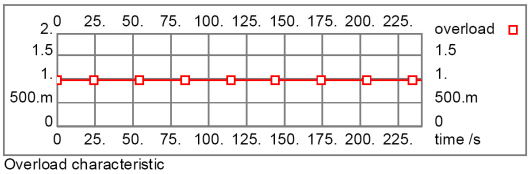
Project :

Topology :	DC/AC
Circuit :	B6I
Application	Scaled 240kW Flywheel
User	Salman Talebi
Description	PF is considerd in the defined load cycle



Circuit :

V_d	500 V		
V_{out}	1 V	f_{out}	316 Hz
I_{out}	1 A	Cos_{phi}	0.70
P_{out}	0.00 kW	f_{sw}	8.0 kHz
Overload Factor	1.00	Overload Duration	120 s
$f_{min\ out}$	316.00 Hz	$V_{min\ out}$	1 V



Overload characteristic

Device :

Product Line	SKiiP
Name	SKiiP1242GB120
Max. Junction Temperature	150 °C
Use Maximum Values	No

Transistor		Diode	
E_{tr}	300.00 mJ (@600V)	E_d	39.00 mJ
$V_{CE0.125}$	1.30 V	$V_{T0.125}$	1.00 V
$r_{C.125}$	1.80 mOhm	$r_{T.125}$	1.00 mOhm
$V_{ce.sat}$	3.10 V	V_f	2.00 V
I_c	1000.00 A	I_f	1000.00 A
$R_{th(j-c)}$	0.023 K/W	$R_{th(j-c)}$	0.063 K/W
$R_{th(c-s)}$	0.000 K/W		

Data set from 2/19/2002

Cooling :

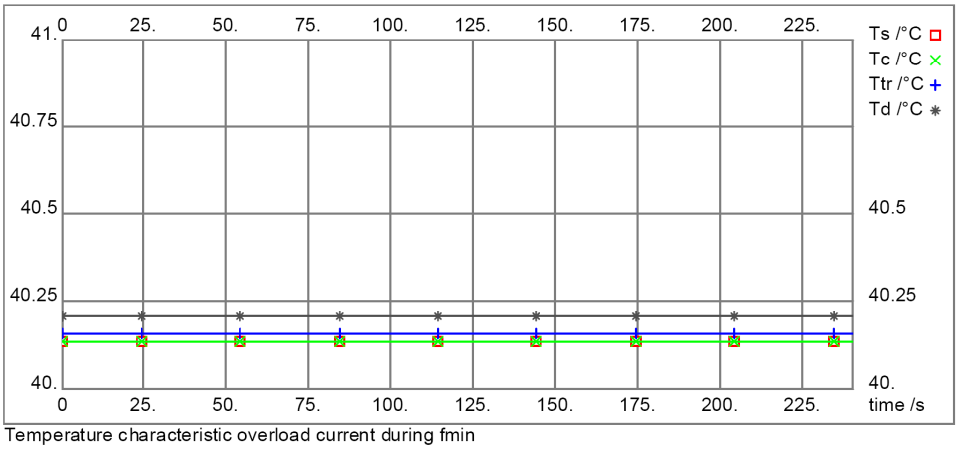
Ambient Temperature	40 °C
Number of switches per heat sink	2
Number of parallel devices on the same heat sink	1
Additional power source at this heat sink	0 W
Semikron - Heat sink	P16_360
Correction Factor	1.00
Cooling Method	Forced Air Cooling
Flow rate	275 m^3/h
$R_{th\ (s-a)}$	0.033 K/W

Losses and Temperatures:

	Rated Current	Overload	Min. Frequency and Overload
$P_{cond\ tr}$	0 W	0 W	0 W
$P_{sw\ tr}$	1 W	1 W	1 W
P_{tr}	1 W	1 W	1 W
$P_{cond\ d}$	0 W	0 W	0 W
$P_{sw\ d}$	1 W	1 W	1 W
P_d	1 W	1 W	1 W
P_{tot}	4 W	6 W	4 W

Figure 5-1 Thermal analysis of the device SKiiP1242GB120-4DU(D)L.

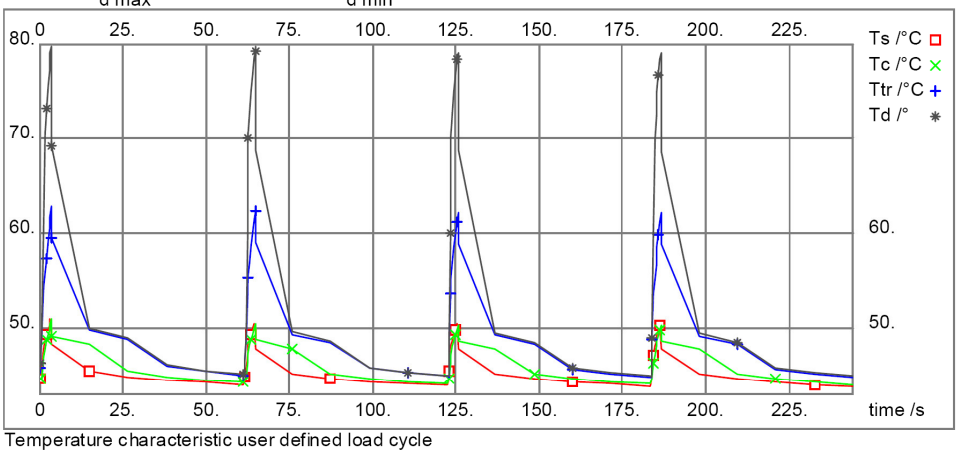
T_s	40 °C	40 °C	40 °C
T_c	40 °C	40 °C	40 °C
T_{tr}	40 °C	40 °C	40 °C
T_d	40 °C	40 °C	40 °C



Temperature characteristic overload current during fmin

User Defined Load Cycle:

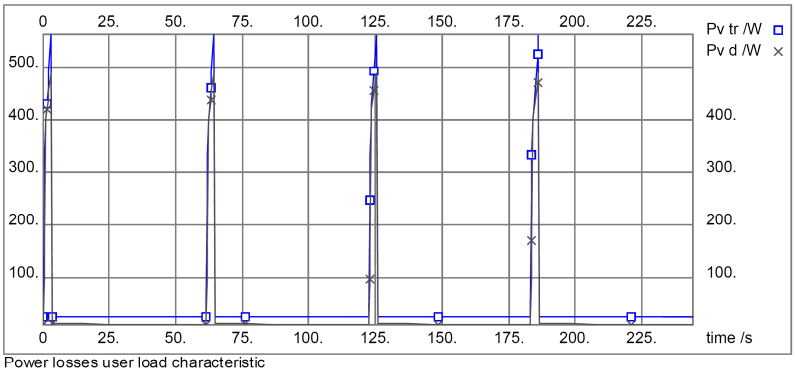
$T_{s\,max}$	51 °C	$T_{s\,min}$	44 °C
$T_{c\,max}$	51 °C	$T_{c\,min}$	44 °C
$T_{tr\,max}$	63 °C	$T_{tr\,min}$	45 °C
$T_{d\,max}$	80 °C	$T_{d\,min}$	45 °C



Temperature characteristic user defined load cycle

$P_{tr\,av}$	276 W	$P_{d\,av}$	201 W
$Pv_{tr\,max}$	564 W	$Pv_{tr\,min}$	24 W
$Pv_{d\,max}$	489 W	$Pv_{d\,min}$	10 W

Figure 5-1 Continued.



Power losses user load characteristic

Number	Time /s	I_{out} *	V_{out} *	Power Factor	f_{out} /Hz	f.sw /kHz
1	0	24.00	240.00	0.70	383.30	8.00
2	1	616.00	315.00	-0.62	383.30	5.00
3	3	750.00	305.00	-0.50	316.70	5.00
4	3.1	24.00	193.00	0.62	316.70	8.00
5	61	24.00	240.00	0.70	383.30	8.00

* This values are rated to the given base value.

Evaluation:

This configuration seems to be too powerful.

Figure 5-1 Continued.

5.2. DC-Bus Capacitor Selection

The objective of this section is to select the appropriate DC bus capacitor bank to meet the requirement of the inverter/rectifier employed in the 240 kW FESS. The DC bus capacitor is a load-balancing energy storage element between the DC and AC sides of a voltage source inverter (VSI) and PWM rectifier. Therefore, the selection of a proper DC bus capacitor bank is necessary for desired electrical, thermal, and mechanical performance of the inverter/rectifier-drive system.

In high-power applications, the capacitor is usually aluminum electrolytic. This type of capacitor provides a unique value in high energy storage and low device impedance. Selecting the right capacitor for the application requires good knowledge of all aspects of the application environment, from mechanical to thermal to electrical [69].

The size of this capacitor depends on the amount of AC energy it must absorb to maintain a required amount of current ripple at the DC bus and the level of rms current it can tolerate because of equivalent series resistor (ESR) heating [70-71]. The wave shape of the inverter DC bus current i_{dc} as well as the capacitor rms current i_{crms} depends on the PWM modulation index and the amplitude and power factor of the inverter/rectifier output current.

5.2.1. Load Power Factor

The fact is that, load power factor determines the amount of current flows through the freewheeling diode (FWD) is compare to the IGBT [69]. At zero power factor, the inverter/rectifier generates only reactive power where FWD and IGBT shares the rms current equally. And no power is supplied from the DC bus (harmonic power components are neglected). On the other hand, at unity power factor purely active power is generated by the inverter/rectifier where IGBT carries the total rms current. And maximum current is supplied by the DC bus. A general relationship between power factor and relative conductivity, in other words, current sharing of IGBT and FWD is depicted in Figure 5-2 for a sine-PWM VSI. It is shown that during the motoring mode of operation (invering operation), the conductivity of IGBT increases from 0.5 as the PF reaches unity. The conductivity of FWD decreases in this mode. The relative conductivity of the IGBT and the FWD does just the opposite during the generating mode of operation (rectifying operation).

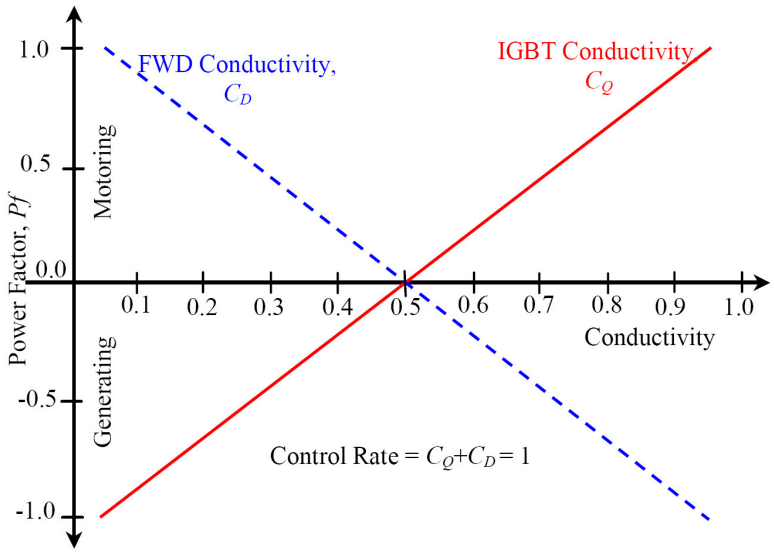


Figure 5-2 Relationship between load power factor and average conductivity of IGBT and FWD for a sine-PWM voltage source inverter.

5.2.2. Capacitor Ripple Current Waveform Considerations

There is a maximum rms current capability (I_{cmax}) of the capacitor, provided by the manufacturer, which is a constraint in determining its thermal stability and demanded working life. The second objective in selecting the DC bus capacitor is to make sure that the rms current is less than the I_{cmax} [70-71]. This is required not to exceed the maximum allowable hot spot temperature of the electrolytic capacitor beyond which the electric strength of the dielectric material is lowered due to additional chemical reactions between the electrolytic material and the aluminum oxide of the anode foil.

Depending on the shape of the capacitor ESR vs. frequency curve, changes in the current duty cycle may lead to capacitor power dissipation that is proportional to the rms ripple current, proportional to the square of the rms ripple current, or somewhere between these two extremes.

5.2.3. Power Range

Three main aluminum electrolytic capacitor types used in higher-power inverter applications are: snap-mount, plug-in, and screw-terminal capacitors shown in Figure 5-3 and Table 5-2 [69]. Larger snap-in capacitors are used in the 1-20 kW range. Screw-terminal and plug-in capacitors also begin seeing use in the 500 W and higher power ranges.

Figure 5-3 Snap-in, plug-in, and screw-terminal, respectively from left to right.

5.2.4. Mechanical and Assembly Issues

Screw-terminal and plug-in capacitors offer a more rugged package for higher vibration and shock performance for very little additional cost compared to snap-mount capacitors [69]. A little additional assembly effort is required in using plug-in or screw-terminal capacitors. For screw-terminal capacitors, proper thread torque needs to be monitored. A large bank of snap-mount plug-in capacitors might make sense when a large circuit board topology is desired and can be afforded, or if extremely low inductance is desired. However, should there be a capacitor problem, capacitor location

and replacement might be difficult, and an expensive circuit board and bank might be difficult or impossible to rework. Screw-terminal capacitors can be circuit-board mounted, or alternatively, a laminated or discrete bus structure may be employed. Screw-terminal capacitors generally use a heavier-duty paper-electrolyte pad compared to the snap-mount capacitors. This often allows them to operate at lower failure rates in banks for the same stored energy.

Table 5-2 Comparison of three main capacitor types used in power inverters.

Category	**Snap-in Capacitor**	**Plug-in Capacitor**	**Screw-terminal Capacitor**
Application power range	0.1 - 30 kW	0.5 - 50 kW	0.5 kW - 10 MW
Mechancal Integrity	Moderate	Excellent	Excellent
Mounting scheme	Circuit board	Circuit board	Circuit board or bus assembly
Cost of Assembly	Low	Moderate	High
Ability to re-work	Poor	Moderate	Superior
Ability to heatsink	Poor	Poor	Superior
Ripple current per cap	< 50 A	< 50 A	< 100 A
Max Temperature	105 ºC	105 ºC	105 ºC
Voltage Range	6.3 - 500	6.3 - 500	6.3 - 550
Size Range	22x25 to 50x105	35x40 to 50x143	35x40 to 90x220
Best Typical Life at 85 ºC	90k hours	> 100k	> 100k
Overvoltage withstand	Moderate	Moderate	Superior
Series Inductance	Low (10-40 nH)	Moderate (20-40 nH)	Moderate (25-80 nH)

5.2.5. 85 ºC Versus 105 ºC Ratings

The can-temperature together with the operating voltage inserts significant influence on the working life of the electrolytic capacitors [69]. From the rule of thumb, for each 10 ^{o}C working temperature decrease from the rated value, the typical working life is doubled. This is due to the fact that at lower temperature, the diffusion of the gaseous parts of the electrolyte through the end seal is reduced and thus the drying out of the capacitor is delayed.

As far as the thermal environment is concerned, all three of these capacitor types have ratings availabilities from 85 ºC to 105 ºC with ripple. In general, 105 ºC-rated capacitors give longer life and/or higher ripple current capability. The main difference in construction between the 85 ºC and the 105 ºC capacitors is in the anode foil. The anodization voltage (formation voltage) is higher for the 105 ºC capacitors. Since the anode capacitance per foil area is lower at higher anodization voltages, this usually means that there is a little less capacitance available in the same case size in a 105 ºC rated capacitor compared to its 85 ºC counterpart.

5.2.6. ESR and Ripple Current Versus Voltage Rating

The current flowing through the capacitor causes Ic^2.Rc loss (converts to heat) on its ESR, which imposes the maximum limit on the rms ripple current capability of the capacitor itself. Now even though the highest capacitance density for a given bus voltage is realized with the highest capacitor voltage ratings, you might wonder about the ripple current rating. High-voltage capacitors must offer some advantages to stringing lower-voltage capacitors in series. In general, higher-voltage capacitors use higher resistive electrolyte and denser papers, so their ESR is much higher [69]. On the other hand, ripple rating varies only weakly with the ESR, inversely as the square root of the ESR. It turns out that two 550V caps of a given size in parallel will handle about the same or a little more ripple than two 300V or even two 250V caps of the same size in series. And two 400V caps in parallel handily beat two 200V caps in series. One thing to keep in mind is that the high-voltage caps are a little more expensive, but save on component count and complexity, and one needn't worry about voltage division between series legs. Also, when caps are used in series, additional voltage derating is recommended.

5.2.7. ESR for Non-Sinusoidal Ripple Current

Ripple current in inverter applications is almost never sinusoidal. Generally there are two strong frequency components of the ripple current, a rectified mains component and an inverter switching component, plus many harmonics of these two components. The fundamental frequency of the rectified mains ripple current, $f_{RM,}$ is given by (5-1) [69].

$$f_{RM} = f_L \times N_\phi \times N_B \tag{5-1}$$

where f_L is the line frequency, N_ϕ is the number of phases, and N_B is 1 for half-wave bridge rectification and 2 for full-wave bridge rectification. In our application the fundamental frequency of i_{dc} as well as i_c is six times the frequency of the fundamental component of the PMSM phase current. The fundamental frequency of the inverter/rectifier ripple current is equal to the switching frequency, f_{sw}. Since the ESR varies with frequency, the precise power loss would be calculated as the sum of the power losses at each frequency. But since this is cumbersome, a shortcut approximation is often used. Generally it is considered acceptable to lump the total rms current into two components, one at f_{RM} and the other at the switching frequency, f_{sw}.

5.2.8. Specification of the Selected Capacitor

All factors influencing the DC bus capacitor were mentioned in the previous section. One thing that should be pointed out here is that in most applications as well as FESS, DC bus voltage ripple is not as effective as DC bus capacitor ripple current. According to the PSIM simulations results, a bank of 5~8 mF is enough to meet the DC bus voltage requirements for the 240 kW inverter/rectifier but as it will be shown, the rms

current of the capacitor would be more effective. In other words, the number and the capacitance of the bank will be determined by the DC bus current not by the voltage ripple.

Based on the dimensions and types of the selected devices (SKiiP1242GB120-4DU(D)L), cooling system (forced air), DC bus structure (vertical configuration), ambient temperature (40 ^{o}C), and the DC bus current extracted from PSIM simulations, the specifications of the selected DC bus capacitor is shown in Table 5-3 [72].

Table 5-3 Specifications of the selected DC bus capacitor.

Type	DCMC 85 ^{o}C
Rated voltage	500 Vdc (550 Vdc Surge)
Capacitance	3900 uF
ESR Max. @ 25 ^{o}C and 120 Hz	37.5 mΩ
Ripple Max. @ 85 ^{o}C and 120 Hz	11.6 A
Nominal size D x L	3 x 5 5/8 inches

The DC-link capacitor bank includes 24 caps such that any device, 1242GB120, consists of eight 3900 uF 500 V (7800 uF @ 1000 V). According to the datasheet of the capacitor, maximum ripple current of the bank will be:

Ripple Max. @ 45 ^{o}C and 1 kHz: 12 x 11.6 x 2.24 x 1.2 = 374.2 A

Ripple Max. @ 45 ^{o}C and 5 kHz: 12 x 11.6 x 2.24 x 1.24 = 386.6 A

Ripple Max. @ 45 ^{o}C and 10 kHz and up: 12 x 11.6 x 2.24 x 1.27 = 396 A

As it was mentioned in the previous section, the DC-link capacitor current mainly includes two frequencies, 6 times of the fundamental frequency (changing between 6 x 316.7 ~ 6 x 383.3 Hz) and switching frequency, 5 or 8 kHz. Also the ambient temperature considered for thermal analysis is 40 ^{o}C while the minimum temperature given in the datasheet for ripple current multiplier is 45 ^{o}C. As a result it can be said that at 40 ^{o}C and 2~8 kHz the maximum ripple current is almost 400 A which meets the requirement of the worst operating point of the FESS given in Table 4-4 (worst case from DC bus current point of view, Figure 5-4). In other words, at 240 kW discharging mode and 19 krpm in which the rms current of the capacitor is 405 Arms.

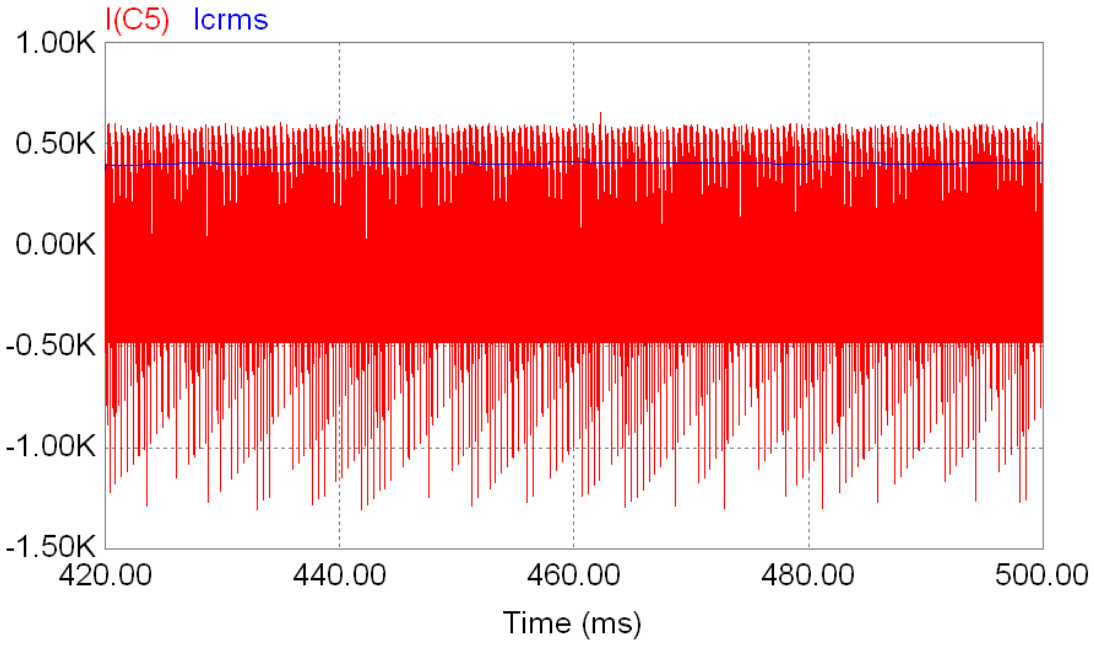
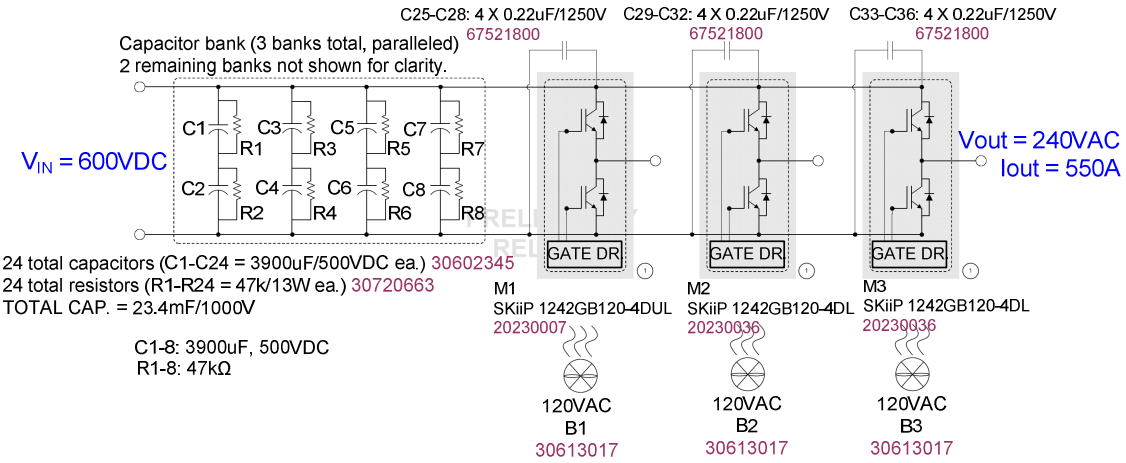


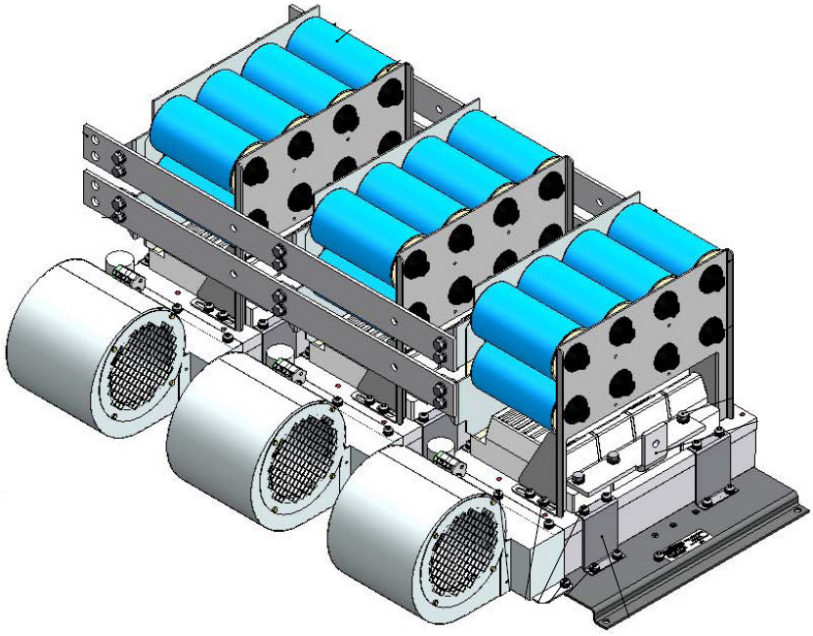
Figure 5-4 DC-link capacitor ripple current.

5.3. Inverter/Rectifier Specification

The schematic of the designed and fabricated inverter is depicted in Figure 5-5.



(a)



(b)

Figure 5-5 240 kW inverter/rectifier schematic,
a) Equivalent circuit b) Physical structure.

The SKiiP1242GB120-4DUL(DL) unit is capable of driving at 14 kHz maximum. The 240 kW system is rated per work scope with a 5 kHz switching frequency. This is limited by the thermal requirements of the system. Each SKiiP unit will be equipped with a blower that will move 275 cubic meters per hour of air flow. These fans operated at 115Vac and consume a maximum of 300 watts each.

The SKiiPPACK has a unique, integrated low inductance bus structure. This bus structure is not only low inductance; it is very user friendly for final assembly into the cabinet. This system will have a single Positive DC connection and a single Negative DC connection.

The gate driver, integrated sensors, protection capability, and control port connection of the SKiiPPACK assembly are described later. The specification of the fabricated inverter/rectifier shown in Figure 5-6 is given by Table 5-4.

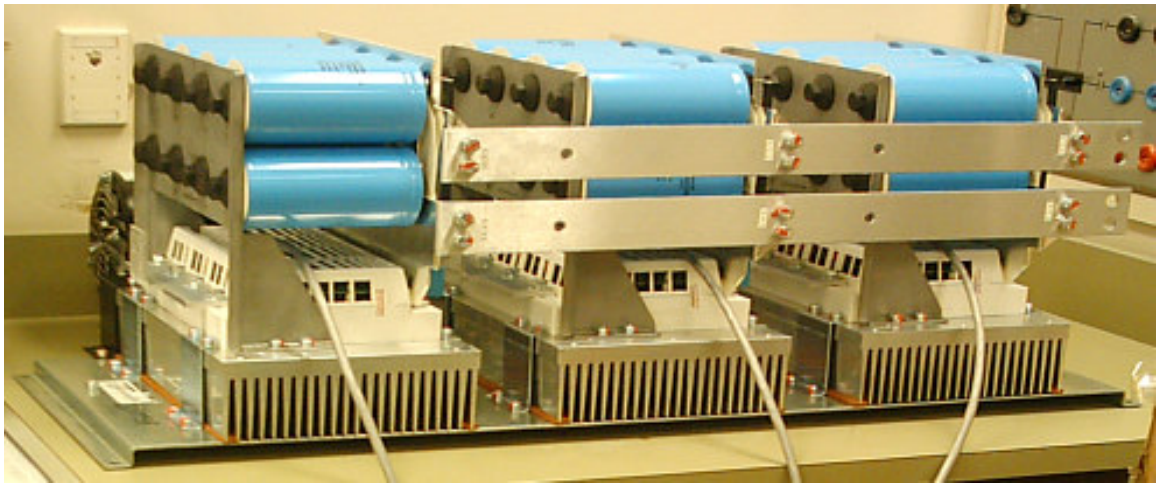


Figure 5-6 240 kW fabricated inverter/rectifier.

Table 5-4 Specification of the fabricated inverter/rectifier.

Input voltage	500 Vdc
Output voltage	190 ~ 315 Vrms
Output current	750 Arms
Ambient temperature	40°C
Protection	Standard SKiip protection
Cooling	Forced air
Device	SKiip 1242GB120-4DUL assemblies Each device consists of: One +/- vertical DC bus structure Eight 3900 uF 500 V electrolytic capacitors (7800 uF @ 1000 V total) Eight 47 kohm voltage sharing resistors Four 0.47 uF 1250 V snubber capacitor One 120 Vac blower One AC connection

5.4. Inverter/Rectifier Features

5.4.1. Device

As discussed earlier, SKiiP1242GB120-4DUL(DL) was chosen as the inverter/rectifier device. Type designation of the device is given in Table 5-5 [73].

5.4.2. SKiiP System Power Section Assembly

Figure 5-7 shows the scheme of a SKiiP [68]. In contrast to conventional transistor modules, the direct copper bonding (DCB) substrates carrying the IGBT and diode chips are not soldered on to a copper base plate, but are pressed almost with the

complete surface directly to the heatsink by means of a plastic pressure spread. The electrical connection of the DCB to the SKiiP terminals, designed for connection of laminated and low-inductance bus bars is made by pressure contacts and low-inductive track layout. A metal plate serves as pressure element and as thermal and EMI-shield for the driver circuit, which is also integrated into the SKiiP case.

By paralleling many, relatively small IGBT-chips and with their optimal contact to the heatsink, the thermal resistance may be reduced considerably compared to standard modules, since the heat is spread evenly over the heatsink.

Table 5-5 Type designation of the device.

Designator	SKiiP 12 4 2 G B 12 0 - 4 DU(D) L
12	Nominal current IC (@ Theatsink = 25 °C) divided by 100
4	Chip specification
2	SKiiP generation
G	Chip type, IGBT
B	2 pack (half bridge, dual)
12	Voltage class, VCES = 1200 V
0	Chip generation
4	Number of used modular half bridges
DU(D)	Gate driver designator D: gate driver DU: gate driver with DC-link voltage measurement and over voltage protection
L	Heatsink designator, standard profile for forced air cooling

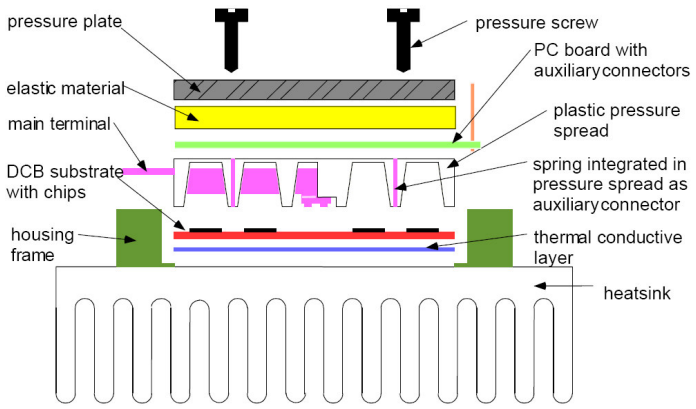


Figure 5-7 The scheme of a SKiiP.

5.4.3. SKiiP 1242GB120-4DUL (4DL)

SKiiP1242GB120-4DUL(DL) system contains 4 single ceramic substrates as shown in Figure 5-8. Each ceramic substrate contains a full phase leg with upper (TOP) and lower (BOTTOM) IGBT as well as the corresponding freewheeling diodes. Paralleling of four ceramic substrates achieves high output current capability. To parallel 4 power sections of the SKiiP System the DC and AC terminals are paralleled to each other.

This feature of the SKiiP technology provides low stray inductance values in the commutation circuit and therefore allows high utilization of the IGBT blocking voltage Vces.

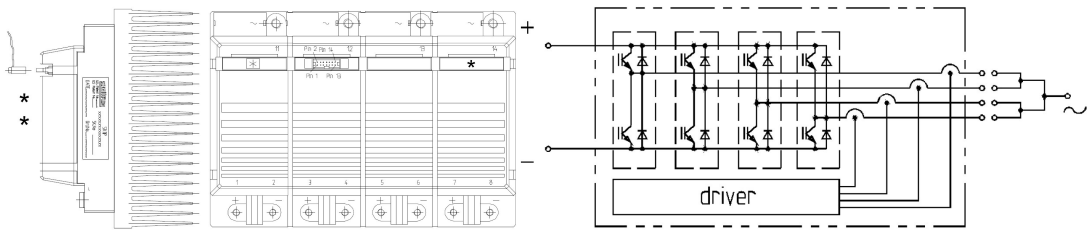


Figure 5-8 4-fold SKiiP system (SKiiP1242GB120-4DU(D)L).

5.4.4. Features of Heatsink

SKiiP1242GB120-4DU(D)L is equipped with a high performance heatsink , P16/360 shown in Figure 5-9.

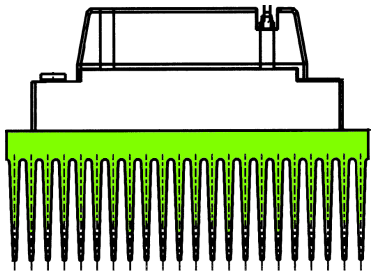


Figure 5-9 Case S4, weight without heatsink: 3.54 kg, P16: 8.46 kg.

Table 5-6 contains transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature if the generated losses are known. The given thermal resistances represent worst case values. Evaluation of thermal impedance is given by (5-2) and (5-3).

Junction-sensor (r: subscript for sensor):

$$Z_{th(j-r)} = \sum R_{th(j-r)n} * [(1 - e^{t/taun})], n = 1,2,3,4 \quad (5\text{-}2)$$

Sensor-ambient:

$$Z_{th(r-a)} = \sum R_{th(r-a)n} * [(1 - e^{t/taun})], n = 1,2,3,4 \quad (5\text{-}3)$$

Table 5-6 Thermal characteristics (P16 heat sink; 275m3/h), "r " reference to temperature sensor.

Z_{th}	R_i(mK/W)(max. values)				tau_i(s)			
N	1	2	3	4	1	2	3	4
$Z_{th(j-r)I}$	2	18	3	0	1	0.13	.001	1
$Z_{th(j-r)D}$	7	48	8	0	1	0.13	.001	1
$Z_{th(r-a)}$	1.6	22	7	2.4	494	165	20	0.03

5.4.5. Forced Air Cooling

In contrast to natural air cooling, forced air cooling can reduce the thermal heatsink resistance to 1/5...1/15. The rated surface temperature of forced air-cooled heatsink should not exceed 80...90 °C at a supply air temperature of 35 °C (condition for datasheet ratings).

The heat conductivity of the heatsink has tremendous influence on the cooling effect, which requires a thick root and a maximum number of fins. R_{thha} is mainly determined by the rate of air flow per time $V_{air/t}$, depending on the average cooling air velocity v_{air} and the transfer cross section A.

$$V_{air/t} = v_{air} \times A \tag{5-4}$$

Instead of the assumed laminar air flow, air whirlings on the fin surfaces will affect turbulent flow conditions between the fins, which will improve heat dissipation to the atmosphere, provided the fin surfaces are set out accordingly.

The transfer cross section of the heatsink will be reduced by increased number of fins and fin width as well as by increased heatsink length (fin length L) and the cooling air-pressure drop Δp will rise. Consequently, heat dissipation is dependent on the characteristics of the fan, which are described in the fan characteristic $\Delta p = f(V_{air/t})$ (Figure 5-10).

The thermal transient resistance of the heatsink assembly R_{tha} depends on the rate of air flow which may be determined by combining fan and pressure drop characteristics $\Delta p = f(V_{air/t}, L)$ or $\Delta p = f(v_{air}, L)$ of the heatsink.

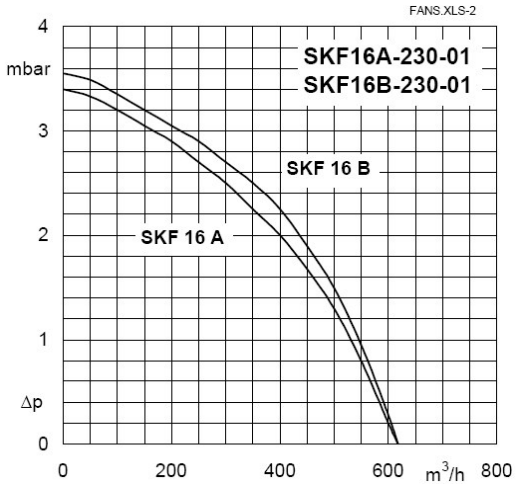


Figure 5-10 Fan characteristic $\Delta p = f(V_{air/t})$ for SEMIKRON P16 fans.

Figure 5-11 shows the assembly of the 4-fold SKiiP1242GB120-4DU(D)L on the air-cooled heatsink P16.

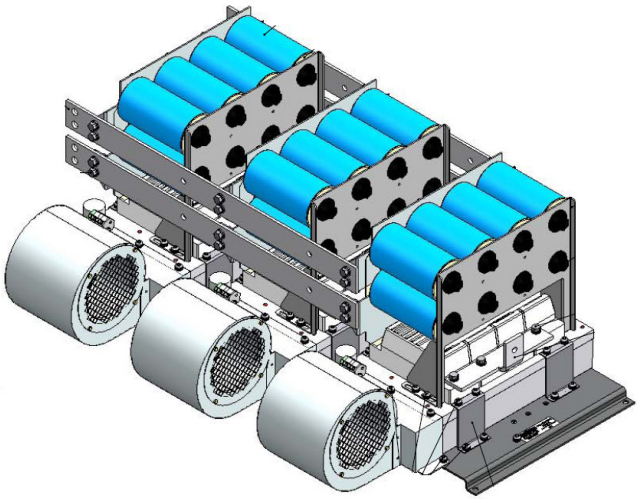


Figure 5-11 Assembly of the 4-fold SKiiP1242GB1204DU(D)L on the air-cooled heatsink P16.

5.4.6. Snubber Capacitors

The 220 nF / 1250 V film capacitors are adapted onto the DC-terminals of the SKiiP1242GB120-4DU(D)L system. These capacitors reduce the over voltage peak during commutation.

5.4.7. DC-Link Capacitors and Bus Bars

The capacitor banks with low stray inductance for direct mounting onto the SKiiP1242GB120-4DU(D)L are shown in Figure 5-11. The capacitor bank comes along with a reinforced support plate, the snubber capacitors and 47 kohm voltage sharing resistors. The specification of the DC-link capacitor bank are shown in Table 5-3.

The DC-link capacitor bank includes 24 caps such that any device, consists of eight 3900 uF 500V (7800 uF @ 1000V).

5.4.8. Connections to Power Terminals

A low-inductive “sandwich” bus bar structure is used to connect the DC-link to the DC terminals of the SKiiP System. The DC-link bank is designed such that each DCB faces the same impedance to the voltage source. This way the current distribution is as even distributed.

The AC outputs of the SkiiP1242GB120-4DU(D)L circuit are paralleled externally. They are connected as symmetric as possible to ensure the even current distribution.

5.5. The Integrated Gate Driver

The SKiiPs contain a driver unit shown in Figure 5-12, laid out as an SMDPCB, which integrates all the necessary protective and monitoring functions and which is positioned over the pressure plate [68]. SKiiPs may be driven and supplied on potential of the super ordinate control system (CMOS or TTL level). The SKiiP driver integrates all necessary potential separation, a switch-mode power supply (SMPS) and the power drivers.

SKiiPs are equipped with current sensors in the AC-outputs and temperature sensors as well as a DC-link voltage sensor. The driver valuates the signals transmitted by the sensors in order to care for over current/ short-circuit, over temperature and over voltage protection as well as supply-under voltage protection. An error signal and standardized analogous voltage signals of the actual AC-output current value, the actual heatsink temperature and, the DC-link voltage are available on separate potentials at the driver connector for evaluation in the super ordinate control circuit.

The maximum switching frequency of the SKiiP1242GB120-4DU(D)L is limited by the average current of the driver power supply and the power dissipation of driver components. The given value for $f_{sw(\max)}$ (14 kHz) in the data sheet is valid for an ambient temperature of 25 °C, for higher temperatures a reduction of f_{sw} might be necessary.

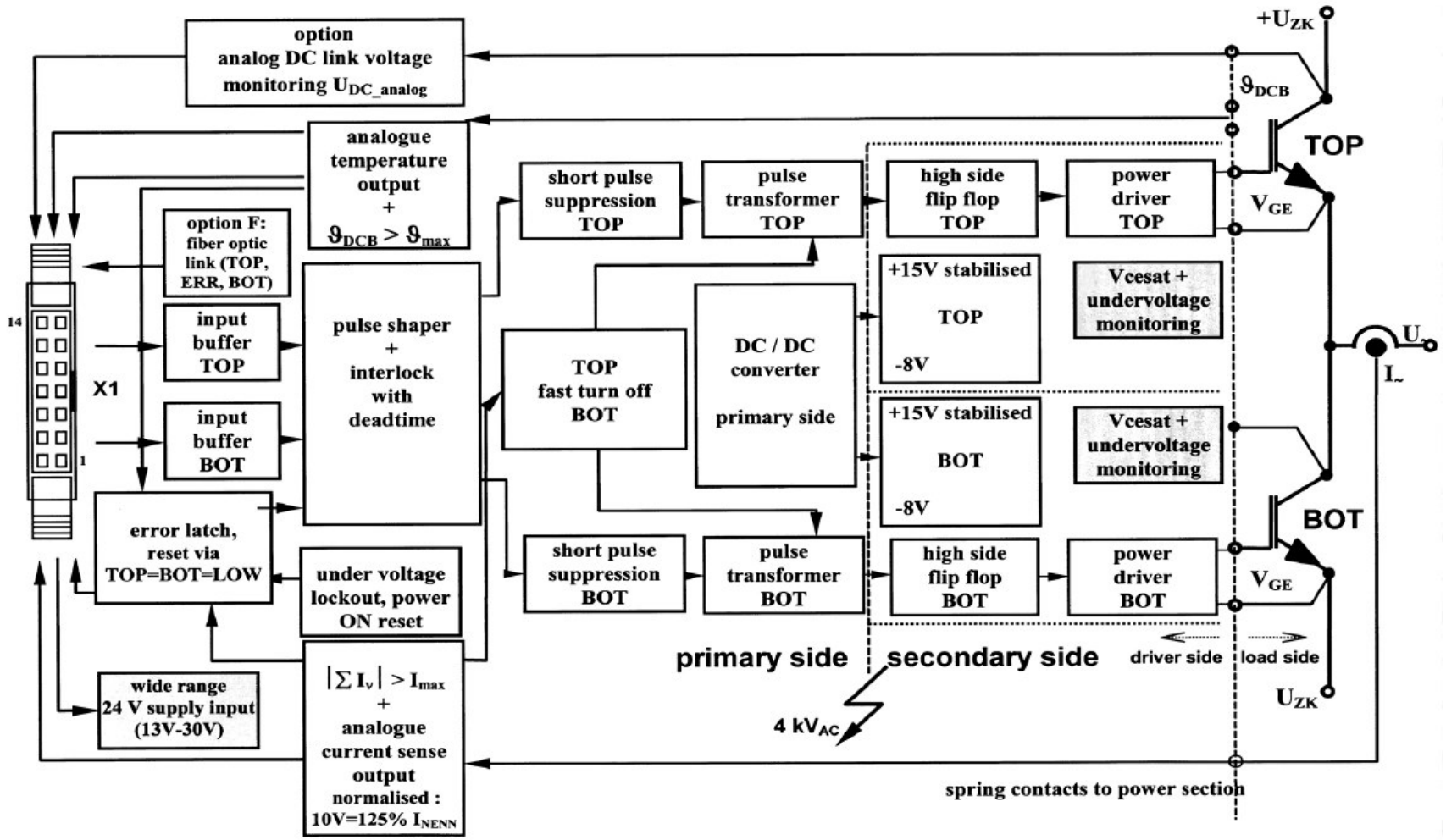


Figure 5-12 Gate driver block diagram.

5.5.1. Integrated Sensor Functions

The SKiiP features several integrated sensors, compensated current sensor per phase leg, temperature sensor on ceramic substrate, and sensing of DC link voltage.

5.5.1.1. Integrated Current Sensor

Current sensors integrated close to the AC-terminals in the SKiiP1242GB120-4DUL(DL) case frame. The sensor is characterized by a small measuring fault (< 0.25 %), a low degree of non-linearity (< 0.1 %) and short response times (< 1 µs). Direct and alternating current may be measured, respectively. The output currents of the SKiip driver sensors have been summarized and normalized in such a way that the type current , IC @ 25 °C, indicated in the datasheet, 1200 A, will generate a voltage of 8V at the actual current output of the SKiiP. The direction of voltage corresponds to the direction of AC-current flow, > 0 V: current flow out of the SKiiP, < 0 V: current flow into the SKiiP,. As soon as 125 % of IC @ 25 °C has been reached, this voltage will increase to its limit value of 10 V, and the over current protection (OCP) inside the SKiiP will be triggered off. The IGBTs will be turned off within 1 µs and the error memory will be set.

With the OCP-principle over-currents will be detected and turned off earlier than with VCE monitoring, since no gating time comparable to VCE-monitoring will be required. Moreover, the turn-off threshold level is not dependent on the temperature as with VCE protection.

The accuracy of the current sensor depends on several points as there are:

• Tolerance of current sensor electronic

• Tolerance of burden resistor of current sensor

• Tolerance of SKiiP internal amplification circuitry (e.g. by offset of operational amplifiers, tolerances of external passive components etc.)

• Tolerance due to temperature drift

The maximum tolerance values can be calculated by the values given in the following equation (Table 5-7):

$$\Delta I = IC * K_{IO} + I_{actual}(K_{Ierror} - K_{IO} + |\Delta T| * TC_{Error}) \quad (5\text{-}5)$$

Where IC is the nominal current per DCB, and ΔI is the absolute deviation per DCB.

Table 5-7 Tolerance evaluation parameters.

Parameter	Value
Offset K_{IO}	0.35 %
Gain Error K_{Ierror}	1.50 %
Temperature Coefficient TC_{Error}	0.001 %/K

As an example, for SKiiP1242GB120-4DU(D)L with IC = 1200 A, the deviation at the current level of $I_{actual} = 1000A$ and $T = 40^{o}C$:

Deviation = 1200 A * 0.35 % + 1000 A * (1.5 % - 0.35 % + |40 °C - 25 °C | * 0.001 % / K) = 15.8 A

5.5.1.2. Integrated Temperature Sensor

The integrated temperature sensor is a semiconductor resistor with a linear proportional characteristic to the temperature. The sensor is soldered onto the ceramic substrate close to the IGBT and freewheeling diodes and indicates the actual substrate temperature. The sensor is insulated. An evaluation circuit realized on the integrated

driver provides a normalized, analog voltage signal of the actual ceramic substrate temperature value shown in Figure 5-13. The ceramic substrate temperature is very close to the heatsink temperature.

The accuracy of the temperature sensor is approximately ± 3 °C. Please note that the temperature sensor is designed for $T_r > 30^o C$. The tolerance band is very wide temperatures below 30 °C.

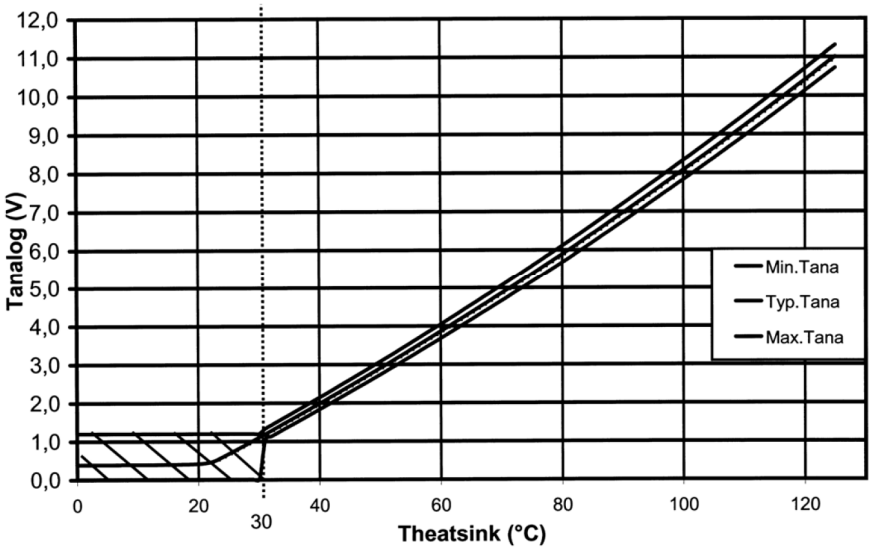


Figure 5-13 Analog temperature signal Uanalog OUT vs. T_{sensor}:
(at pin "Temp. analog OUT").

5.5.1.3. Integrated DC Link Voltage Monitoring

With the option U "analog DC-link voltage-sense", a normalized, analog voltage signal of the actual DC-link voltage level is available at pin 12 of the gate driver control cable. The measurement is realized by a high impedance differential amplifier. Normalization of the actual DC-link-voltage signal is shown in Table 5-8.

Table 5-8 DC-link voltage monitoring range.

V_{CES}	$V_{DC} \leftrightarrow V_{DCanalog}$	$V_{CCmax} \leftrightarrow V_{DCTripmin}$
1200 V	900 V ↔ 9	900 V

The failure of the measured signal is ± 2 % @ Ta = 25 °C. The over voltage trip level is Vccmax. The analog output signal VDCanalogOUT is filtered with a time constant of t = 500 µs.

5.5.2. Protection and Supervisory Functions

The SKiiP gate driver features the following protection and supervisory functions

• Interlock and dead time generation for TOP and BOTTOM IGBTs

• Short pulse suppression

• Input pulse shaping

• Input signal clamping

• Under voltage monitoring of the (internal) supply voltage on primary side

• Transient over voltage and inverted polarity protection by suppressor diode

• Over temperature protection

• Short circuit and over current protection by current sensor and Vcesat monitoring

• Over voltage protection of the DC link voltage

The following section gives a description of the SKiiP System protection and supervisory functions as illustrated in the block diagram. The datasheets include timing and trip level data.

5.5.2.1. Over Current and Short Circuit Protection

As shown in the block diagram depicted in Figure 5-12 the SKiiP System features integrated current sensors per AC terminal. These current sensors are also used for AC current control. In addition they are used to protect the SKiiP System against over currents. The over current protection reacts independently of the temperature level and provides a reliable protection of the SKiiP System. If the AC output current is higher than the maximum permissible level of 125 % IC, the IGBTs are immediately switched off and switching pulses from the controller are ignored and the error latch is set. The output "ERROR OUT" is in HIGH state. In addition a VCEsat monitoring circuit is implemented to protect the phase leg against internal short circuit (shoot through protection).

5.5.2.2. Over Temperature Protection

The temperature of the ceramic substrate is monitored by an integrated temperature sensor. The over temperature trip threshold has been chosen at T = 115 ± 5 °C. At that temperature the IGBTs are switched off and switching pulses from the controller are ignored and the error latch is set. The outputs "Overtemp. OUT" and "ERROR OUT" are in HIGH state. The over temperature trip threshold has been chosen at 115 °C. For most air cooled applications this is sufficient to protect the system.

5.5.2.3. Under Voltage Protection of the Supply

The under voltage protection of the primary side monitors the internal 15 V DC which is provided by the internal DC/DC converter converting the unregulated input voltage to 15 V DC or by controlled + 15 V DC input.

If the under voltage trip level is reached, the IGBTs are switched off and switching pulses from the controller are ignored and the error latch is set. The output "ERROR OUT" is in HIGH state. Table 5-9 below gives an overview of the trip levels.

Table 5-9 Under voltage trip levels under different conditions.

Condition	Under voltage trip level
primary side, supply via 24 V pins	18.5 V
primary side, supply via 15 V pins	13.5 V
Internal regulated + 15 V	13.5 V
internal regulated - 15 V	- 13.5 V

5.5.2.4. DC Link Over Voltage Protection

If the operating DC link voltage is higher than VCCmax, 900 V, the IGBTs are turned off and switching pulses from the controller are ignored and the error latch is set. The output "ERROR OUT" is in HIGH state.

5.5.2.5. Short Pulse Suppression

The circuit suppresses short turn-on and off-pulses shown in Figure 5-14. This way the IGBTs are protected against spurious noise as they can occur due to bursts on the signal lines. Pulses shorter than 625 ns are for 100 % probability suppressed and all pulses longer than 750 ns get through for 100 % probability. Pulses with a length in-between 625 ns and 750 ns can be either suppressed or get through.

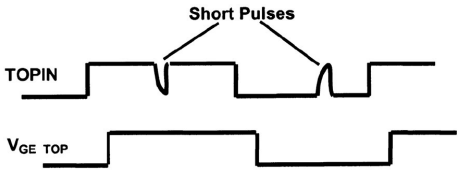


Figure 5-14 Pulse pattern - short pulse suppression.

5.5.2.6. Dead Time Generation, Top/Bottom Interlock

The interlock circuit prevents that the TOP and the BOT IGBT of one half bridge are switched on at the same time, internal short circuit. The internal interlock time is adapted to the power semiconductors, i.e. it is chosen as small as possible to allow high duty cycle but guarantees a safety margin against shoot through losses due to tail currents. The dead time does not add to a dead time given by the controller. Thus the total dead time is the maximum from either “built in dead time” “or “controller dead time”.

The propagation delay of the driver is the sum of interlock dead time, tTD, and driver input output signal propagation delay of the driver, td(on/off)IO, as shown in Figure 5-15. The I/O-delay, td(on/off)IO, includes the time for short circuit suppression. The interlock time is only active in case that the opposite device is switching with an inverted pulse pattern. Moreover the switching time of the IGBT chip has to be taken into account, not shown in Figure 5-15.

In general, it can be said, that in case both channel inputs, TOPIN and BOTIN, are at high level shown in Figure 5-16, the driver outputs, VGETOP and VGEBOT, will be turned off, but no error signal will be generated. Short pulses on the complementary

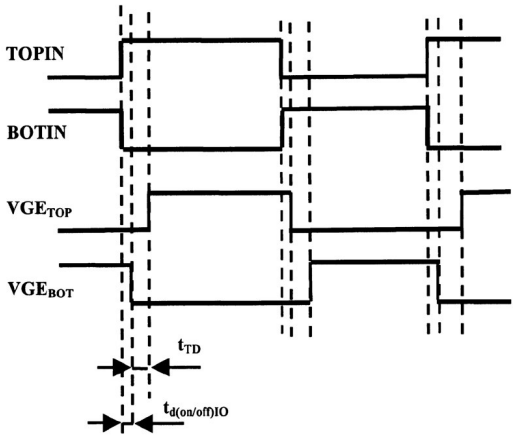


Figure 5-15 Pulse pattern - dead time generation.

input will be also ignored in the case for any pulses shorter than the short pulse suppression, 650 ns.

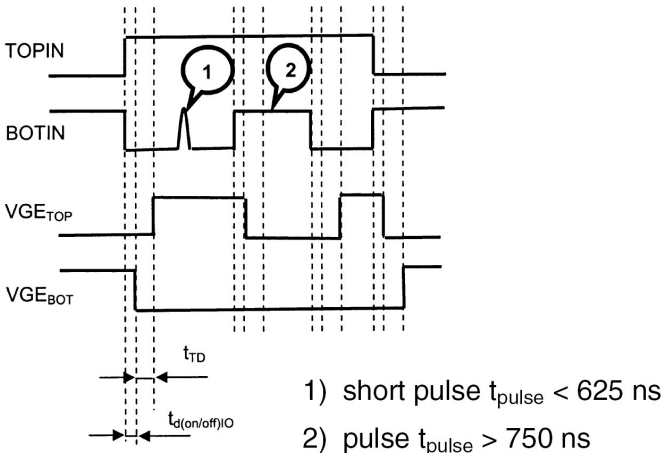


Figure 5-16 Signal logic behavior for both input pulses in ON state.

5.5.3. Device Control Port

As illustrated in Figure 5-17, the inverter/rectifier includes two '+', and '-' DC busses and three AC terminals connected to the external inductor or the PMSM terminals. Any device, in other words, any leg of the inverter has a 12-pin control port shown in

Figure 5-12, which is used for communication with the DSP Board through the control cable and interface boards. Note that 4 pins out of 14 are allocated to the external 15 V DC power supply required by the gate driver circuitries. Table 5-10 determines the function of each pin [74].

According to Figure 5-17 and Table 5-10 [74], each device imports two PWM signals for driving the top and bottom IGBTs and exports two analogue signals, phase current and DC bus voltage or temperature. Also it exports two logic signals determining the occurrence of any faults such as, over current, over temperature or under-voltage of the power supply. One pin is used to connect the cable shield to the ground of the gate driver circuitry, and the remained two pins are used when a 24 V DC power supply is supplying the gate driver circuits which is not the case in this project.

5.5.3.1. Connection to the Control Port

Because of voltage drop and for immunity against electromagnetic interference the maximum length of the control cable shouldn't exceed 3 meters. Also to avoid interferences, the control cable is placed as far as possible away from the power terminals, the power cables, the DC-link capacitors and all other noise sources. The ribbon cables is kept as close to GND as possible (heatsink).

5.5.3.2. Acquisition and Evaluation of Analogous Signals

To guarantee faultless processing of the analogous SKiiP signals, it is important to avoid ground loops and voltage drops in measuring wires which are not caused by measuring signals. Therefore, measuring signals have to be conducted on the ground side via the AUXGND-connections and not via power supply ground lines shown in Figure 5-

18. Because of the likely interferences in the environment, the evaluation of any analogous signal is done via a differential amplifier with reference to auxiliary ground, AUX-GND.

Table 5-10 PIN-array of half-bridge driver SKiiP 2 GB 2-fold.

Pin	Signal	Remark
1	Shield	
2	BOT IN[2)]	Positive 15V CMOS logic; 10 kΩ impedance
3	ERROR OUT[1)]	LOW = NO ERROR; open Collector Output; max. 30 V / 15 mA propagation delay 1 µs, min. pulse-width error-memory-reset 9 µs
4	TOP IN[2)]	Positive 15V CMOS logic; 10 kΩ impedance
5	Overtemp. OUT[1)]	LOW = NO ERROR = T_{DCB} < 115 + 5°C open collector Output; max. 30 V / 15 mA "low" output voltage < 0.6 V "high" output voltage max. 30 V
6	+ 24 VDC IN	24 V_{DC} (20 - 30 V) don't supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 19.5 V
7	+ 24 VDC IN	
8	+ 15 VDC IN	15 VDC + 4 % power supply don't supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
9	+ 15 VDC IN	
8	+ 15 VDC OUT	max. 50 mA auxiliary power supply when SKiiP system is supplied via pin 6/7
9	+ 15 VDC OUT	
10	GND	GND for power supply and GND for digital signals
11	GND	
12	Temp. analog OUT or V_{DC} analog OUT[3)]	V_{DC} when using option "U" actual DC-link voltage, 9 V refer to V_{DCmax} max. output current 5 mA; over voltage trip level 9 V
13	GND aux	reference for analogue output signals
14	I analog OUT	current actual value 8.0 V ⇔100 % I_C @ 25 °C over-current trip level 10 V ⇔125 % I_C @ 25 °C current value > 0 ⇔ SKiiP system is source current value < 0 ⇔ SKiiP system is sink

[1)] Open collector output, external pull up resistor necessary
[2)] "high" (max) 12.3 V, "low" (min) 4.6 V
[3)] When using option "U" the analog temperature signal is not available

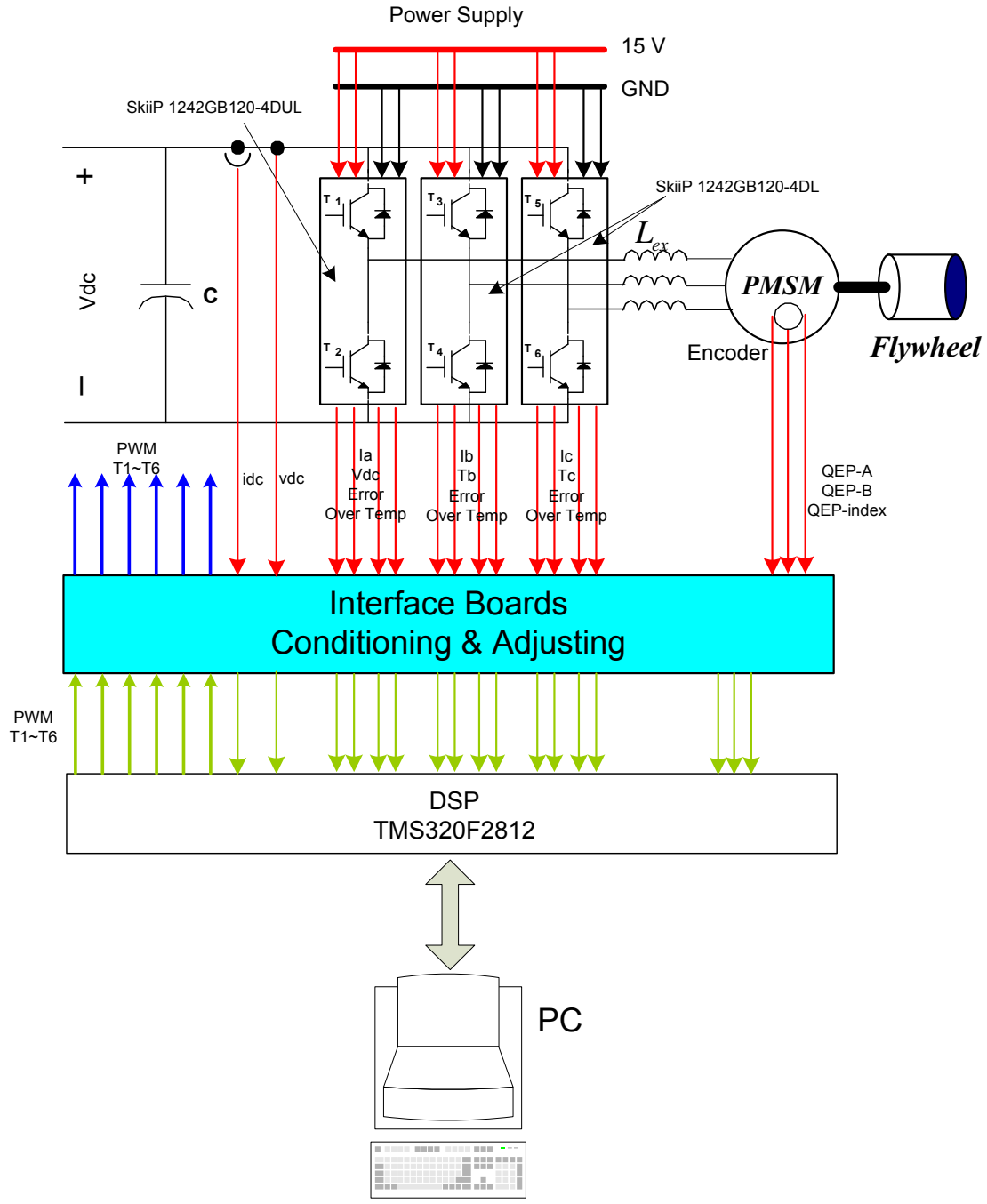


Figure 5-17 Integration of the inverter with the interface boards and the DSP board block diagram.

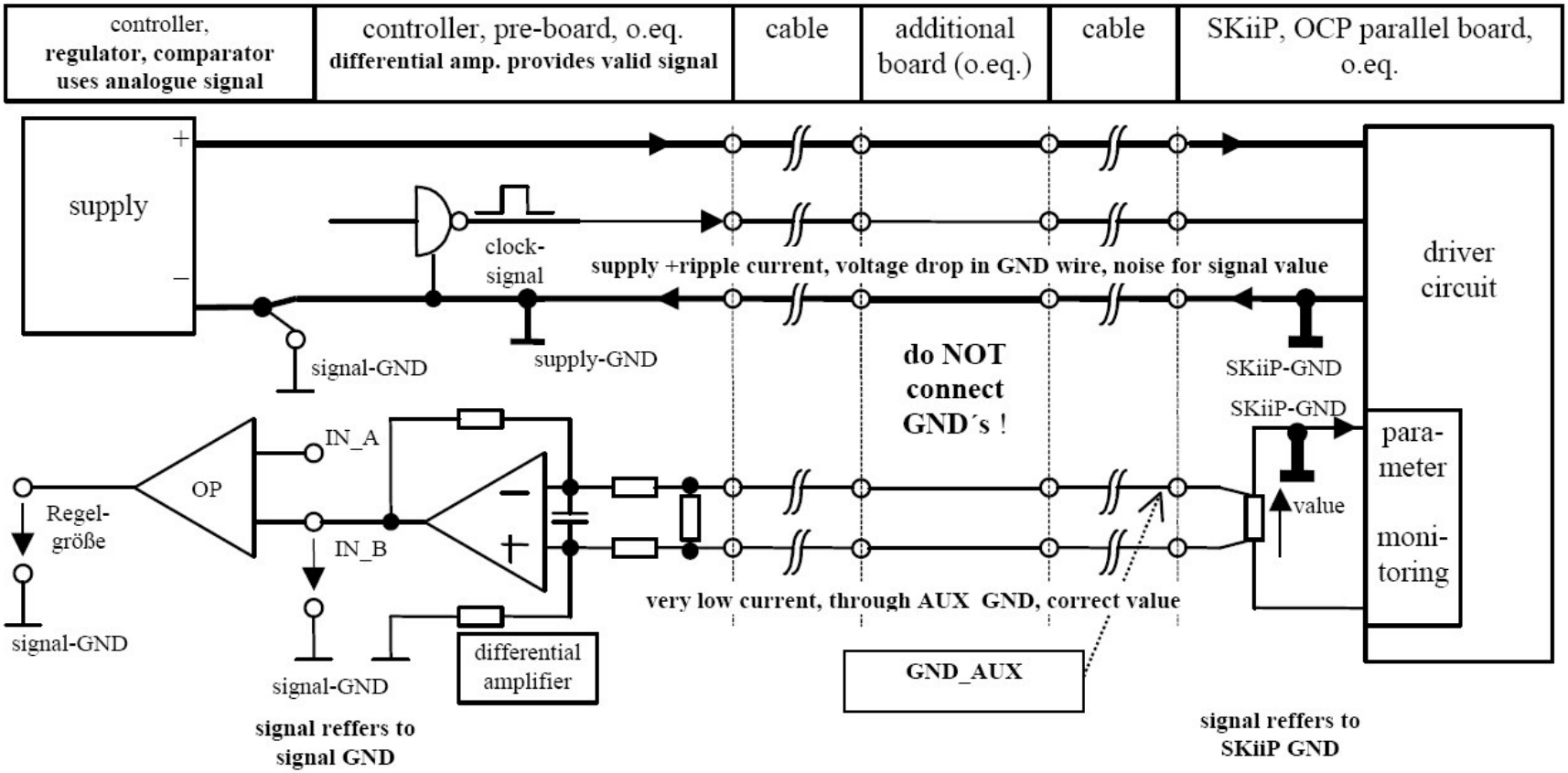


Figure 5-18 Processing of analogous SKiiP output signals.

5.5.3.3. Digital Input

Figure 5-19 shows the schematic of the SKiiP digital input lines. A 1 nF capacitor is connected to the input to obtain high noise immunity. This capacitor can cause for current limited line drivers a little delay of few ns, which can be neglected. It is compulsory to use circuits which switch active to +15 V and 0 V. Pull up and open collector output stages must not be used for TOP/BOT control signals.

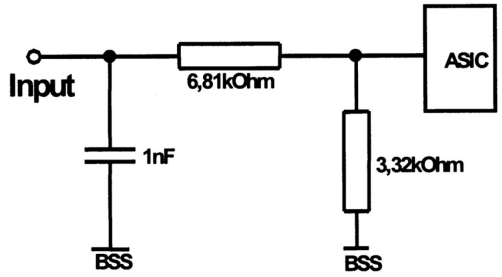


Figure 5-19 User interface - TOP/BOT input.

5.5.3.4. Analog Outputs

Figure 5-20 shows the schematic of the SKiiP analog output lines. The 475 Ω resistor in series with the voltage follower does avoid short circuit damages.

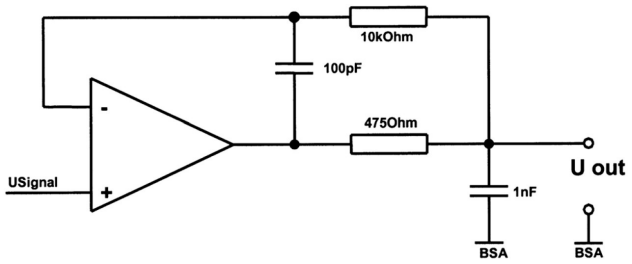


Figure 5-20 User interface- analog signal output.

For a trouble-free interaction of SKiiP and user side control, it is necessary to adapt the user input to the SKiiP outputs. For that reason the auxiliary analog signal ground BSA is used when analog signals are measured. The ground BSA is on the SKiiP driver board on the same potential as BSS, which is the ground of the power supply. The difference is that the BSA line is not used for supply currents and for that reason no voltage drop due to supply current will be caused.

In the following section, a schematic shown in Figure 5-21 and a description is given for an analog input circuit on the controller board of the user.

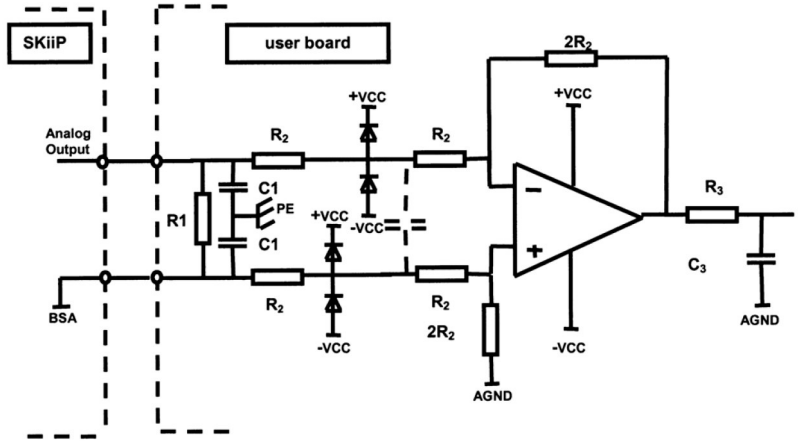


Figure 5-21 Symmetric wired differential amplifier.

The circuit in Figure 5-21 is a symmetrical wired differential amplifier.

• At the input there is a 10 kΩ resistor (R1). The interference sensitivity of the over all circuit (user control, driver) is reduced by a continuous current flow through this resistor.

• Capacitor C1 leaks differential and common mode high-frequency interference currents. This capacitor should not be larger than 100 pF to ensure that there is no additional time delay in the system. On the interface board it is chosen as 68 pF.

• The symmetrical wiring of the amplifier is as shown in Figure 5-21. Note that no capacitor is in parallel to the feedback resistor or to the resistor of the non-inverting input to ground (2R2 = 20 kΩ). These capacitors have often higher tolerances, so the common-mode rejection of the circuitry is reduced by this effect.

• The input resistor should be split up and installed between the clamping-diodes. The current in the diodes is limited by this resistor. A diode with a low reverse current, 1N4148, is selected.

• If a low pass filtering shall be implemented in the input circuit, this should be done with a capacitor between the input resistors (see dotted lines). In most cases this capacitor is not necessary and the smoothing can be realized by a simple R-C network ,R3 and C3, at the end of the operational amplifier.

5.5.3.5. Error Latch and Error Feedback

Any error detected will set the error latch and force the output "ERROR OUT" into HIGH state. Switching pulses from the controller will be ignored. Reset of the error latch is only possible with no error present and all input signals in LOW state for the time TpRESET = 9 µs. All logical error outputs are open collector transistors with Vexternal = 3.3 - 30 V / Imax = 15 mA (Low signal = "no error" - wire break monitoring). The external pull-up voltage is set to 15 V. An external pull-up resistor Rpull-up to the controller logic high level is required. The resistor has to be in the range: Vexternal/Imax < Rpull-up <10 kΩ, which is selected to be 4.7 kΩ.

The external filter capacitor Cext is not compulsory but for noise immunity it is used. It is advised to choose a value of something in the range of a few nF, because the RC time constant must not exceed the minimum error duration time of 9 µs.

Figure 5-22 illuminates the principle of the Error output for the SKiiP. The error transistor is an ordinary open collector transistor. The resistor Rsens acts as sensor for the short circuit protection. In case that the current exceeds the specified Imax = 15 mA the transistor will be turned off and the error signal can be detected by the customer. This way the error transistor is short circuit proof.

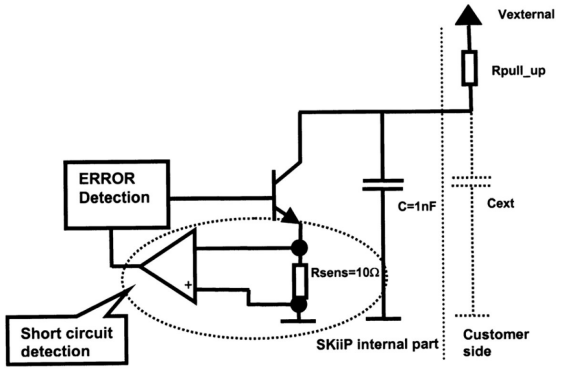


Figure 5-22 SKiiP - open collector error transistor.

5.5.3.6. Requirements of the Auxiliary Power Supply

Table 5-11 shows the required features of an appropriate power supply for the SKiiP System. All values are related to one SKiiP. In case that the gate driver is supplied with 24 V it is possible to use 15 V provided at the pins 8 and 9 of the gate driver connector as an auxiliary power supply, e.g. for a level-shifter at the controller's output signals.

The current consumption of the SKiiP System depends on the level of supply voltage used, the standby current of the gate driver, the switching frequency, the capacitance of the IGBT gates in use and on the actual main AC-current.

In the data sheets for each gate driver an equation is given which describes the current consumption depending on standby current, switching frequency and AC output current. The power supply is rated such that the continuous current is at least 20 % higher than that of the calculated consumption current from the SKiiP. The rated peak current of the supply must fulfill the specification in the table.

In the datasheet the equations for the evaluation of the current consumption shown in Table 5-12 is given for both supplying with 24 V and 15 V. Note that in our setup, regulated 15 V is chosen as the power supply.

5.5.3.7. Error Management

The error management of SKiiP can be described by Table 5-13. Any error condition will cause the error signals on the corresponding pins to go high on the open collector output, indicated by "X".

Table 5-11 The required features of an appropriate power supply for the SKiiP system.

Unregulated 24 V power supply	20 – 30 V
Regulated power supply 15 V ± 4 %	15 V
I_{out} 15 V (can be used if 24 V supply is active)	<50 mA
Minimum peak current of auxiliary 15 V supply	1.5 A
Minimum peak current of auxiliary 24 V supply	1.5 A
Max. rise time of auxiliary 15 V supply (the voltage slope has to be continuous – no plateau in voltage slope)	50 ms
Max. rise time of auxiliary 24 V supply (the voltage slope has to be continuous – no plateau in voltage slope)	50 ms
Power on reset completed after	130 ms

Table 5-12 The equations for the evaluation of the current consumption.

I_{s1}	V_{s1} = 15 V	$290+580*f/f_{max}+1.2*(I_{AC}/A)$	mA
I_{s2}	V_{s2} = 24 V	$220+420*f/f_{max}+0.85*(I_{AC}/A)$	mA

Table 5-13 Error management.

	Pin 3 ERROR HB1 OUT	Pin 5 Overtemp. OUT
VCE-protection HB1	X	
OCP* HB1	X	
Temperature protection	X	X
DC-link over voltage protection	X	
Internal supply voltages error	X	

* OPC = Over Current Protection

5.6. Interface Boards

In the previous sections, it was explained how to read the analog signals, phase currents, DC bus voltage, and temperature, and pass the PWM pulses to the control port of the inverter/rectifier devices. Actually, six of the differential amplifiers shown in Figure 5-21, are interfacing between the devices control port and the DSP Board ADC channels through an adjusting and conditioning board (ACB). Also, the PWM pulses generated by the DSP Board are transferred to the devices control port through this ACB. Moreover, the pulse signal from the optical encoder coupled to the PMSM shaft is filtered and is scaled down from 5.0 V to 3.3 V on the ACB and applied to IO port of the DSP Board.

The reason for using the ACB is that the ADC channels of the DSP TMS3202812 are able to read the analog signals in the range 0-3 V. Therefore, the analog signals from the devices control port should be filtered and scaled down in this range and then transferred to the ADC channels. Similarly, the PWM signals generated by the DSP are in the range of 0-3.3 V and they should be converted to the range 0-15 V and then apply to the gate driver of the devices. So PWM gate pulse isolation & magnitude conversion are

handled by the inverters on the ACB. Also the Encoder signal is filtered and rescaled through a filter on the ACB.

The ACB has been designed such that to be capable of reading 10 analog signals and generating 12 PWM pulses. Depending on the analogues signal, it might be bidirectional, such as phase currents, DC bus current, and temperature or unidirectional as DC bus voltage.

5.6.1. ADC Input Signal Conditioning

The ACB contains 10 amplifiers capable of gain and DC offset adjustment such that all analogue signals, the output signals from the differential amplifiers, can be tuned between 0 and 3 V. Please note that only 6 of the 10 filters are used for this work. Figure 5-23 depicts the schematic of one of the amplifiers on the ACB.

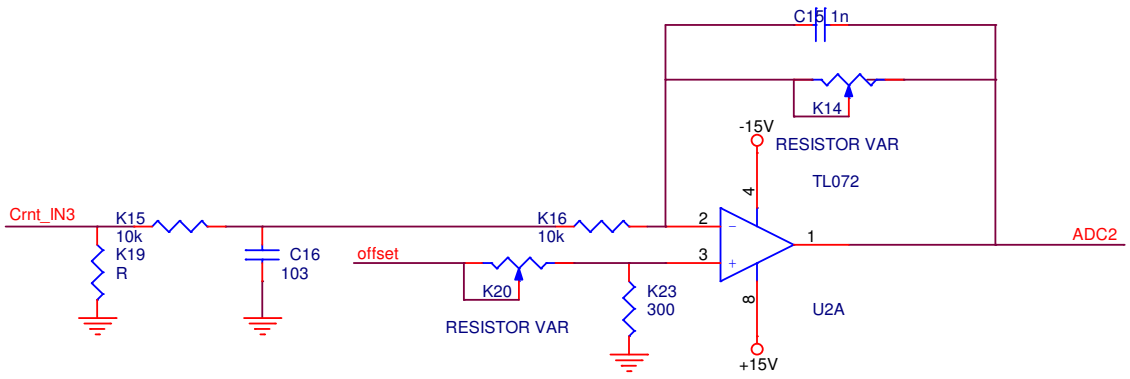


Figure 5-23 ADC input signal conditioning circuit.

5.6.2. PWM Gate Driver Signal Conditioning

The output PWM signal of the DSP board can be set either to 3.3V or 5.0V via a jumper (might change according to the custom design and third party boards). On the

other hand, the IGBT gate drivers need 0-15V pulses. The converter shown in Figure 5-24 is used to isolate, amplify and invert the PWM signals.

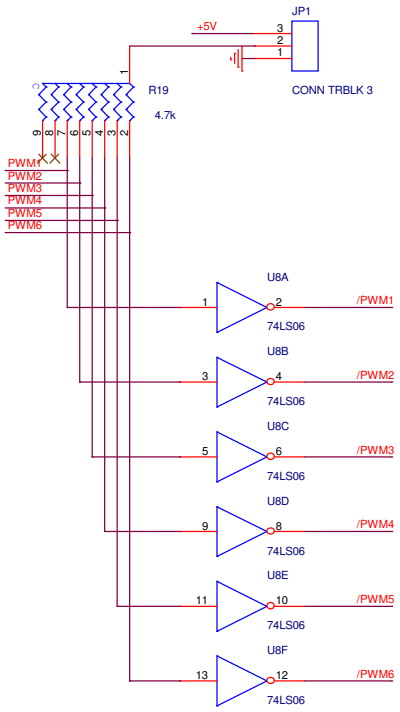


Figure 5-24 PWM gate signal conditioning circuit.

5.6.3. Encoder Pulse Conditioning

Ph_A, Ph_B and Ph_Z (index) pulses are converted from 5V to ~3.3V and filtered by the below circuit.

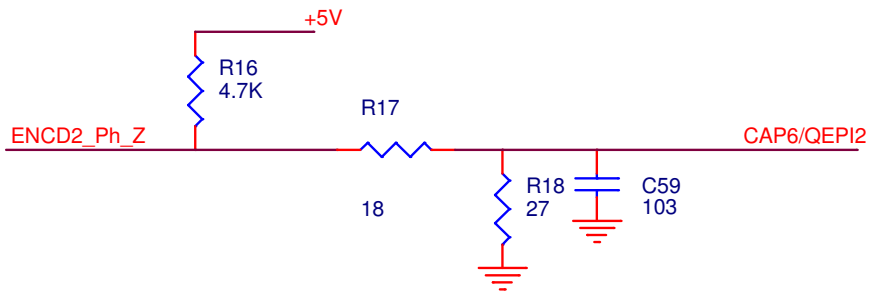


Figure 5-25 Encoder output signal conditioning.

Figure 5-26 depicts the interface board (ACB), the DSP board, the differential amplifiers, the control cables and their connections.

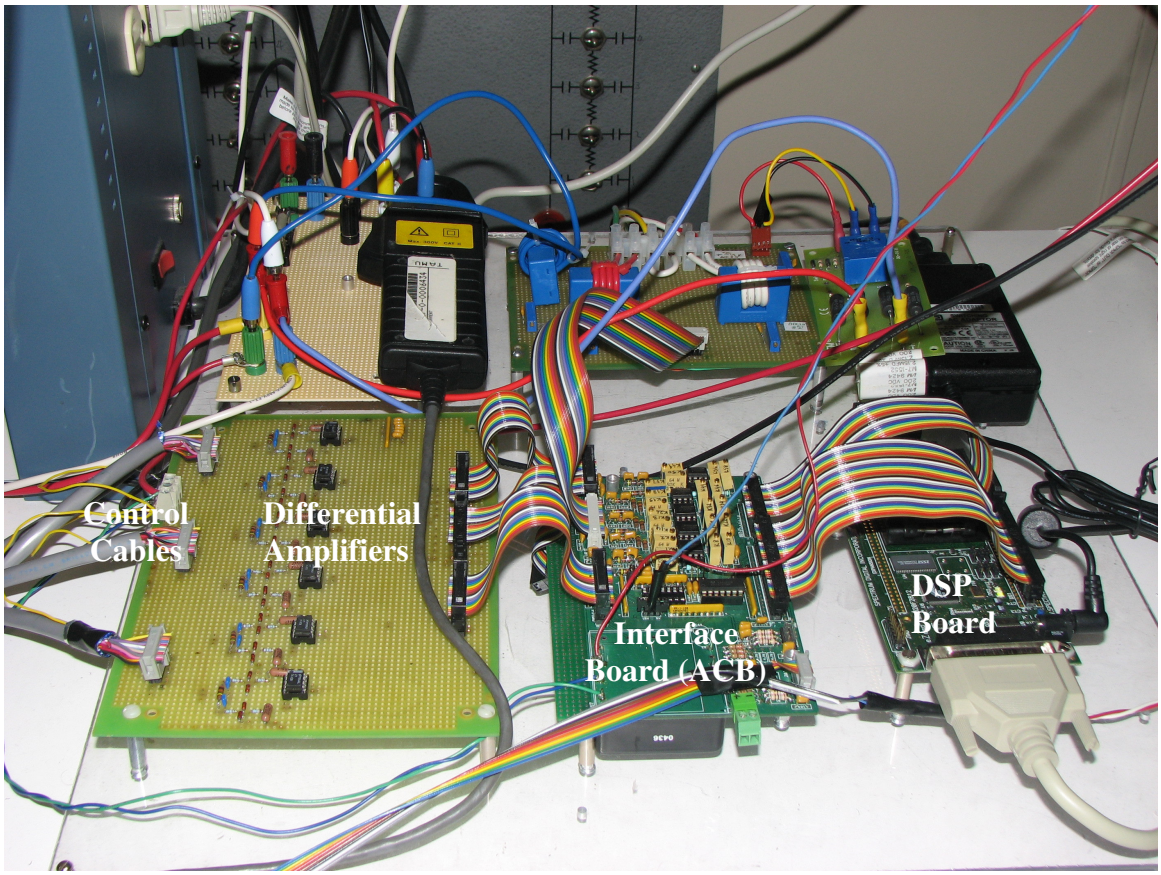


Figure 5-26 Integration of the interface boards and the DSP board.

6. EXTERNAL INDUCTOR DESIGN

Typical for PM machines, the pulsed output rating is 2 to 5 times the continuous machine power rating. For this output to be useful, the machine impedance must be very low to allow for the power to be removed very quickly. High-speed PM machines offer this low impendence with low number of stator turns and large operating magnetic air gaps which is highly desired for withdrawal of a large amount of power from the machine. On the other hand, the low inductances result in high THD which increases the machine power losses and temperature. Therefore, the external inductor is needed for the flywheel energy storage system in order to reduce the harmonics and PMSM rotor losses to manageable levels. However, for the discharging mode, due to desired fast response time, no external inductor is applicable.

The required switching frequencies and external line inductance values have been determined after iterations between power electronics simulations and machine loss and thermal analyses. The THDs analyses of the PMSM were performed and corresponding rotor losses were calculated using Ansoft 2-D finite element analysis (FEA) transient solver with motion. Table 6-1 summarize the switching frequency and external inductance value requirements and calculated losses.

6.1. Thermal Analysis of the FESS

Thermal analysis is used to predict the temperature rises of the components in order to provide enough margins for safety operation. The heat in the rotor can only be

removed through radiation to the stationary parts. In the thermal analysis, the housing is assumed to be maintained at 125 °F.

Table 6-1 Losses for the 240 kW pulse power [24].

Mod.	Sw. Freq. (kHz)	Ext. Ind. (uH)	Speed (krpm)	Cur. (A)	Pow. (kW)	THD (%)	Core loss (W)	Teeth loss (W)	Cu loss (W)	PM loss (W)	Sleeve loss (W)	Total loss (W)	Eff. (%)
Dis. Ch.	5	0	19	771	260	8.4	637	158	16338	85	1220	18438	93.4
Dis. Ch.	5	0	23	652	267	8.6	791	197	11760	70	1225	14043	95
Ch.	8	150	19	27	9	21.2	637	158	22	0.2	12.5	829	91.6
Ch.	8	150	23	26	10	25	791	197	23	0.23	15	1026	90.7

The transient thermal analyses based on lumped parameter thermal model were performed [20]. Figure 6-1 shows the simulated temperature distributions when the temperature becomes stabilized. It is found that the rotor temperature is higher at the top due to smaller radiation surface area and winding temperature is higher at the end-turn winding.

The thermal analysis results are listed in Table 6-2. We can see that with the chosen switching frequency and the external inductor there are adequate thermal margins to ensure safety operation of the FESS.

Table 6-2 Simulated maximum temperatures for 240 kW pulse power [75].

Component	Design Limit	Predicted	Safety Margin
Winding	392 °F/ 200 °C	255 °F/ 124 °C	137 °F/ 76 °C
Permanent Magnet	446 °F/230 °C	262 °F/ 128 °C	184 °F/ 102 °C

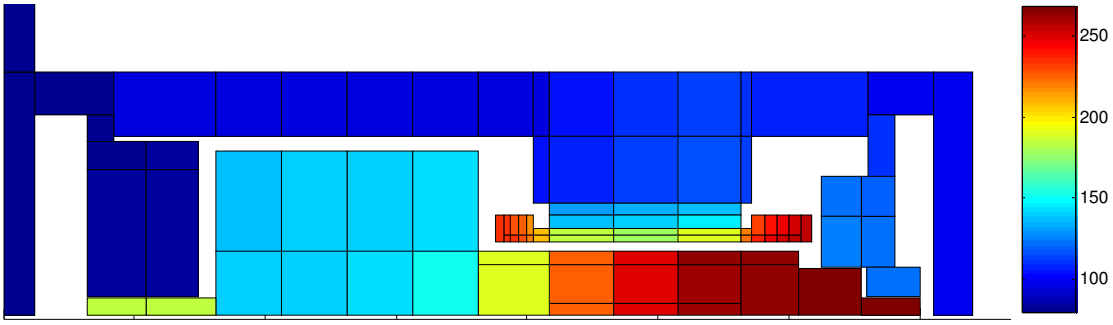


Figure 6-1 Simulated temperature distribution at steady state for 240 kW pulse power [75].

6.2. External Inductor Design

The required external line inductance value, 150 μH, was determined after iterations between power electronics simulations and machine loss and thermal analyses. As mentioned before, the 150 μH inductor should be bypassed in the discharging mode. The bypass of the inductor can be managed in two ways, by a circuit breaker/power device or through a saturable inductor. The former method is so expensive since the circuit breaker/power device should be rated at 240 kW power level, however, it breakes the circuit at low current level. So it is more reasonable to design a 150 μH saturable inductor such that in the charging mode it operates in linear operating area and in discharging mode it is saturated by high current and becomes ineffective.

6.3. 150 μH Saturable Inductor

The design of the inductor depends upon five related factors, desired inductance, applied voltage (across inductor), frequency, operating flux density, and temperature rise. With these requirements established, the designer must determine the maximum values

for, B_{ac}, which will not produce magnetic saturation in linear operating mode, and make trade-offs that will yield the highest inductance for a given volume.

The core material selected determines the maximum flux density that can be tolerated for a given design, a temperature rise and efficiency. Amorphous materials exhibit linear hysteresis loops with low coercivity, a high saturation induction of 0.7–1.8 T, high permeability and low core loss. Their unique combination of low loss and high saturation flux density provide for weight and volume reductions of up to 50% and improvements in energy efficiency. The amorphous materials have relatively low losses with small temperature dependence or even a negative temperature coefficient. They have lower losses than the best grain-oriented steel grades, about 0.25 W/kg at 1.4 T.

According to the benefits mentioned above, POWERLITE C-Cores manufactured with iron based Metglas Amorphous Alloy 2605SA1 are selected as the core material for the design of the saturable inductor [76]. A typical DC hysteresis loop of Metglas Alloy 2605SA1 is shown in Figure 6-2.

Obviously, the inductor winding should be rated for 750~800 A(rms), the maximum rating current in the discharging mode. So in the selection of the core size, the ratings at discharging mode have been considered rather than charging mode.

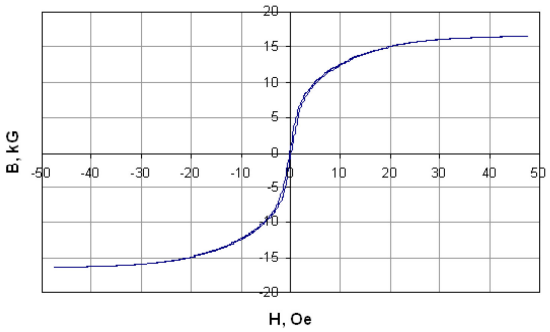


Figure 6-2 Typical DC hysteresis loop, Metglas Alloy 2605SA1.

6.4. Primary Design Procedure

In this section the design is explained step by step as following [77]:

Step No. 1: Design a saturable AC inductor with the specifications shown in Table 6-3.

Table 6-3 The specifications of the desired saturable inductor.

Line current	Charge: I_L = 25 ~ 30 Arms Discharge: I_L = 750~800 Arms
Line fundamental frequency	310 ~ 400 Hz
Current density	J = 300 A/cm^2
Efficiency goal	90% ~ 100%
Magnetic material	Amorphous Alloy 2605SA1
Magnetic material permeability	μm = 1500
Flux density	Linear: Bac = 1 T
Window utilization	Round wire: Ku = 0.4, Foil: Ku = 0.6
Waveform factor	Sine: Kf = 4.44
Temperature rise goal	Tr = 50°C

Step No. 2: Calculate the apparent power, Pt or VA of the inductor, L.

As mentioned above, the inductor should be sized for the discharging mode ratings. It should be designed such that it presents a 150 μH inductor at charging mode, 25 ~ 30 Arms, and a 5 ~ 15 μH inductor at discharging mode, 750 ~ 800 Arms.

$$V_L I_L = 2\pi f L I_L^2 = 2 \cdot \pi \cdot 400 \cdot 0.000010 \cdot 800^2 = 16085[W] \quad (6\text{-}1)$$

Step No. 3: Calculate the area product, Ap, and select a core.

$$A_p = \frac{VA(10^4)}{K_f K_u f B_{ac} J}[cm^4]$$
$$A_p = \frac{16085(10^4)}{4.44 \cdot 0.4(0.6) \cdot 400 \cdot 1 \cdot 300} = 754.7(503.1)[cm^4] \quad (6\text{-}2)$$

As a sample, Figure 6-3 shows the magnetization curve of AMCC-1000 vs. magnetizing force [78]. According to this figure, for a core with 0.5 mm air gap length, when the ampere-turns change from 400 to 3000 A, the A_L-value changes from 3 μH/N^2 to 0.1 μH/N^2. For instance, if this core is selected for the inductor design and the air-gap is set to 0.5 mm, then the winding should have 7 turns to result in 150 μH or 3 μH/N^2. In this case, under 45 A, 300 A-turns, the inductor will operate in its linear operating area and as soon as the current increases the inductance value reduces such that at 750~800 A, 5250~5600 A-turns, it presents an inductance value around 5 μH or 0.1 μH/N^2. Assuming a 300 A/cm^2 current density (it is explained shortly) for the wire or foil, the cross section area of the winding should be around 2.75 cm^2, which means 19.25 cm^2 total cupper area. According to Table 6-4 window area of the core is 42 cm^2 which results in 0.46 fill factor. Typical values for fill factor are 0.4 and 0.6 for round and foil wires, respectively. So this simple example verifies that the core size should be close to this core.

So based on the calculated Ap and the explanation above, the closest laminations to the calculated area product, Ap, are AMCC 630, AMCC 800A, AMCC 800B, AMCC 1000, AMCC 1725, and AMCC 1843 presented in Table 6-4 [76]. The cores dimensions and performance parameters are presented in Table 6- 4.

The current density, J, can be related to the area product, Ap, of the inductor for a given temperature rise. The relationship is derived in [77]. The relationship between current density, J, and area product, Ap, for temperature increases of 25°C and 50°C is

graphed in Figure 6-4. So for the inductor design a temperature rise of 50°C and a current density of 300 A/cm^2 are considered according to short discharging time, 2 sec.

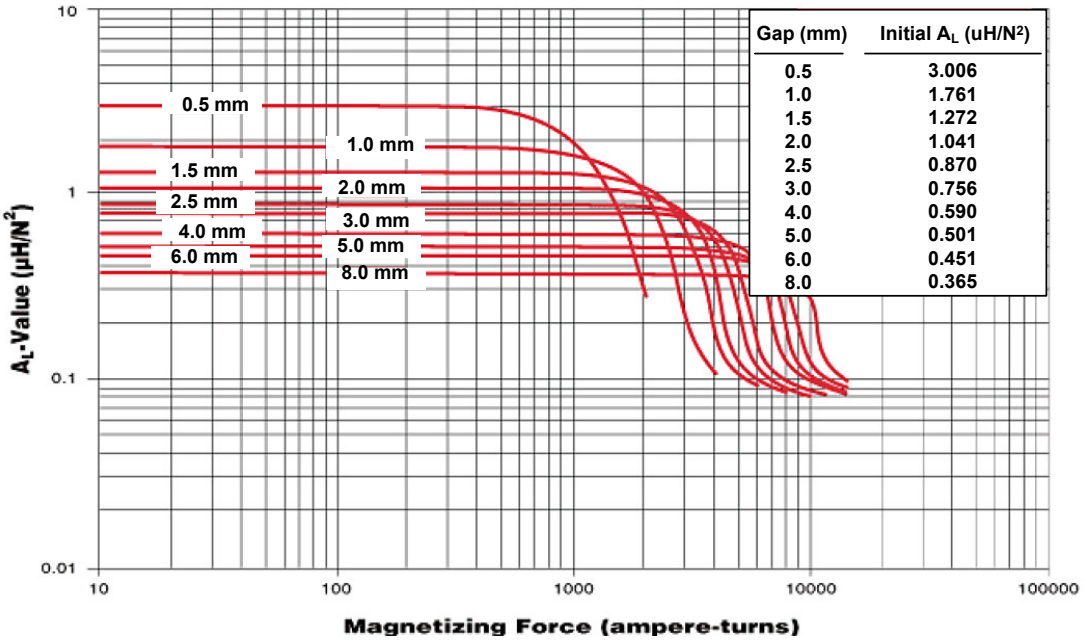


Figure 6-3 AMCC-1000 magnetization curves.

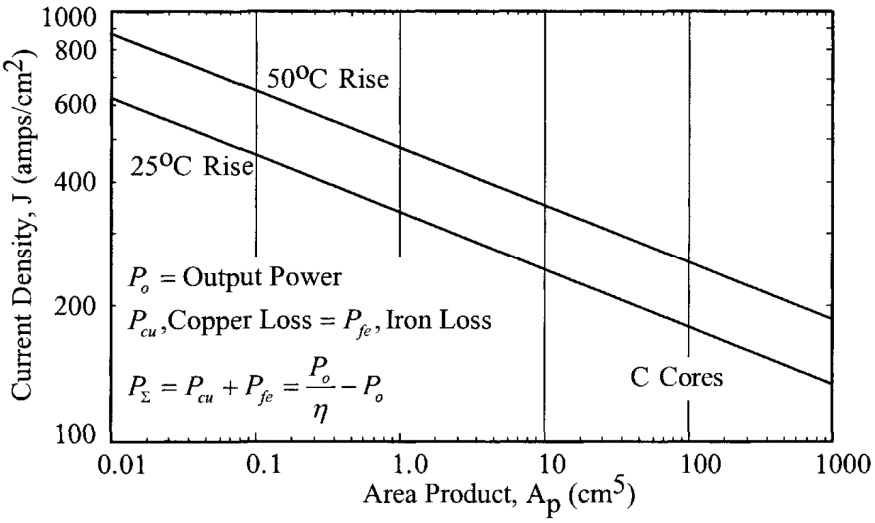
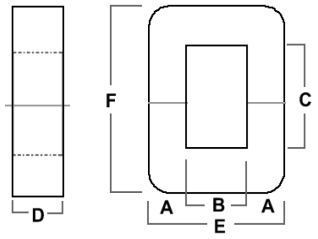


Figure 6-4 Current density, J, versus area product, Ap, for C cores.

Table 6-4 AMCC cores dimension and performance parameters.

Core Type AMCC1000 Amorphous Metal C-Core Part Designation	Core Dimension 						Performance Parameters				
	a mm	b mm	c mm	d mm	e mm	f mm	MPL cm	ac cm^2	Wa cm^2	Ap cm^4	W kg
AMCC630	25.0	40.0	85.0	70.0	90.0	135.0	35.6	14.3	34.0	486.2	3.67
AMCC800A	25.0	40.0	85.0	85.0	90.0	135.0	35.6	17.4	34.0	591.6	4.45
AMCC800B	30.0	40.0	95.0	85.0	100.0	155.0	39.3	21.0	38.0	798.0	5.93
AMCC1000	33.0	40.0	105.0	85.0	106.0	171.0	42.7	23.0	42.0	966.0	7.06
AMC1725	63.5	38.1	97.8	88.9	165.1	224.8	53.63	46.3	37.3	1725.0	17.82
AMCC1843	63.5	38.1	121.9	76.2	165.1	248.9	58.45	39.7	46.4	1843.0	16.65

Step No. 4: Calculate the number of inductor turns, N_L.

$$N_L = \frac{V_L \cdot 10^4}{K_f B_{ac} f A_c}, [turns] \tag{6-3}$$

From now on, I consider the required performance for charging mode, 150 μH inductance value at 25~30 Arms. According to the loss analysis results shown in Table 6-1, with this value of the inductor, the THD is around 20% ~ 25%. So in calculation of V_L, current harmonics should be considered in the rms value of the inductor voltage. To do so, FFT analysis of the line current wave has been performed using PSIM package to evaluate the current harmonics at different harmonic frequencies (up to 49^{th} harmonic).

The line current wave and the corresponding FFT results are presented in Figure 6-5. The numbers of turns for different designs are shown in Table 6-5.

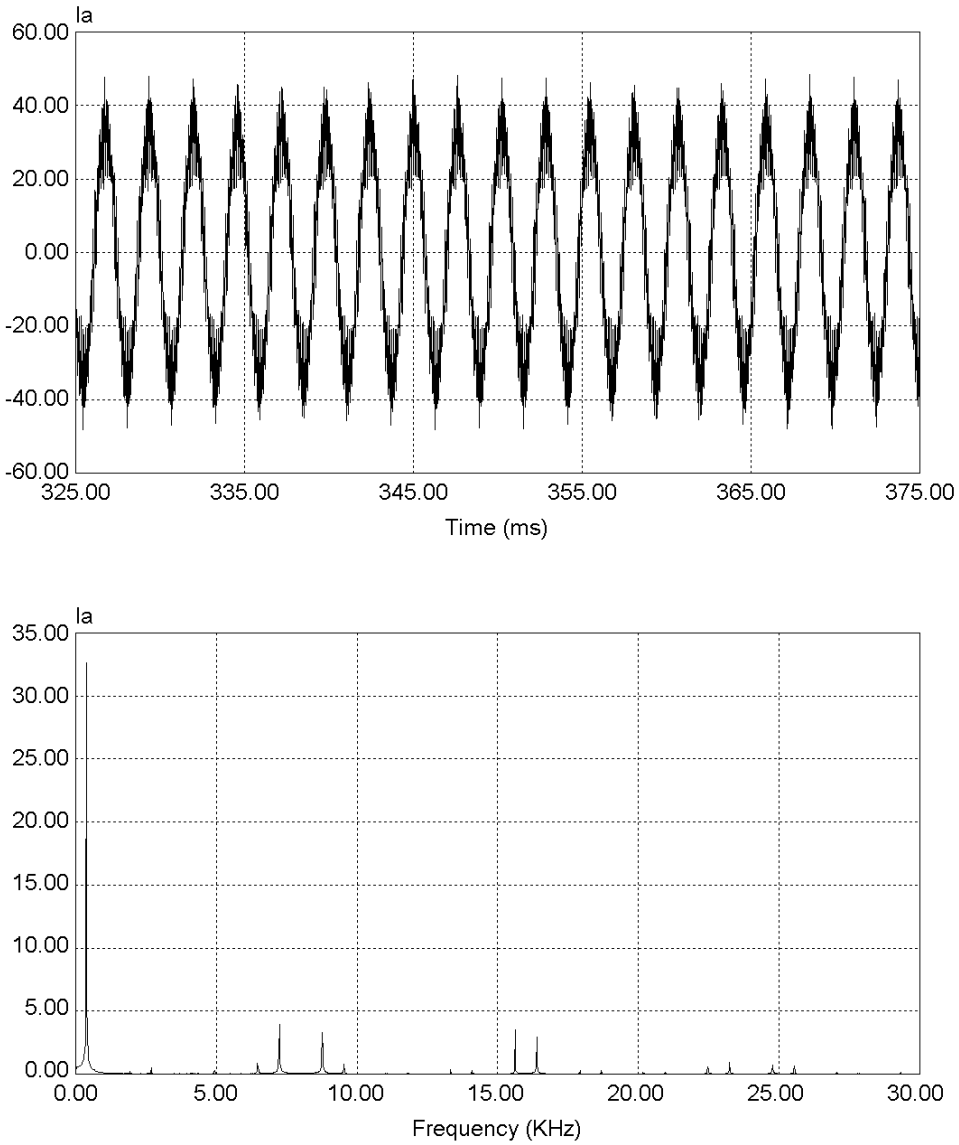


Figure 6-5 Line current wave and its FFT analysis results at 23 krpm and charging mode.

Step No. 5: Calculate the required gap, l_g.

$$l_g = \frac{0.4\pi N_L^2 A_c (10^{-8})}{L} - \frac{MPL}{\mu_m}, [cm] \tag{6-4}$$

where MPL is Magnetic Path Length of the core. The required gaps for different designs are shown in Table 6-5.

Step No.6: Calculate the fringing flux , F.

$$F = 1 + \frac{l_g}{\sqrt{A_c}} \ln \frac{2G}{l_g} \tag{6-5}$$

where G is the winding length and it is assumed equal to dimension c presented in Table 6-4. The fringing fluxes for different cores are shown in Table 6-5.

Step No. 7: Using the fringing flux, recalculate the series inductor turns, N_{Lnew}.

$$N_{Lnew} = \sqrt{\frac{l_g L}{0.4\pi A_c F (10^{-8})}}, [turns] \tag{6-6}$$

The recalculated inductor turns for different designs are shown in Table 6-5.

Step No. 8: Using the new turns, recalculate the flux density, B_{ac}.

$$B_{ac} = \frac{V_L (10^4)}{K_f N_{Lnew} A_c f}, [T] \tag{6-7}$$

The recalculated flux densities for different designs are shown in Table 6-5.

Step No. 9: Calculate the inductor bare wire area, Awb.

$$A_{wb} = \frac{I_L}{J}, [cm^2]$$
$$A_{wb} = \frac{825}{300} = 2.75 cm^2 \quad (6\text{-}8)$$

Step No. 10: Select a wire or foil.

Before the wire or foil is selected, it should be pointed out that the maximum fundamental frequency of the inductor current will be almost 400 Hz. To reduce the copper losses, the skin effect should be taken into account. Skin effect accounts for the fact that the ratio of effective alternating current resistance to direct current is greater than unity. The magnitude of this effect, at high frequency on conductivity, magnetic permeability, and inductance, is sufficient to require further evaluation of conductor size, during design. The skin depth is defined as the distance below the surface, where the current density has fallen to 37 percent of its value at the surface.

$$\varepsilon = \frac{6.62}{\sqrt{f}} k, [cm] \quad (6\text{-}9)$$

where ε is the skin depth, f is the frequency in Hz, and k is equal to 1 for copper. When selecting the wire for high frequency, it is recommended to select a wire where the relationship between the AC resistance and the DC resistance is 1. In other words, the diameter/tickness of the wire/foil should be two times the skin depth.

Using this approach, the wire/foil diameter/tickness should be two times $\varepsilon = 0.331$cm. The wire/foil size closest to this size is AWG #2 or a foil with 0.662 cm tickness. So in the case of round wire, AWG #2, 9 (n_p) parallel wires is needed to meet the inductor bare wire area, 2.75 cm^2. The resistivity of this wire is 0.52 μohm/cm. Note

that in the case of foil selection, the height of the foil should be less but close to the height of the core window, c/2. So in the design, different foils should be considered for different types of the cores.

Step No. 11: Calculate the inductor winding resistance, R_L.

At this point we can calculate the resistance per unit length of the wire/foil. For copper at a given temperature T, the resistivity is given by:

$$\rho = 1.724(1 + 0.0042(T - 20)(10^{-6}), [\Omega - cm] \quad (6\text{-}10)$$

If we assume that the maximum ambient temperature is 40 ^{o}C, and the losses in the component give rise to an additional temperature rise of 50 ^{o}C, then we should use a value of 90 ^{o}C, when calculating the resistivity of copper. This responds to 2.23 μΩ-cm. The resistance per unit length of conductor, say for AWG #2, is given by:

$$R_{unit} = \frac{\rho}{n_p A_{wb}} = \frac{2.23}{9 \times 0.3363} = 0.736 \mu\Omega - cm \quad (6\text{-}11)$$

For Metglas POWERLITTE C-Cores, the mean turn length is approximated by [79]:

$$MLT = 2(a + 2b + d), [cm] \quad (6\text{-}12)$$

The total resistance for the winding is given by:

$$R_L = R_{unit} MLT \; N_{Lnew}, [\Omega] \quad (6\text{-}13)$$

The calculated resistances for different designs are shown in Table 6-5.

Step No. 12: Calculate the inductor winding copper loss, Pcu.

$$P_{cu} = R_L I_L^2 \quad (6\text{-}14)$$

The calculated copper losses for different designs are shown in Table 6-5.

Step No. 13: Calculate the core losses, P_{fe}.

For Metglas POWERLITE C-Cores, the core losses are given by the expression [79]:

$$P_{fe} = 6.5 f^{1.51} B_{ac}^{1.74}, [W/kg] \quad (6\text{-}15)$$

where f is in kHz. The core losses are proportional to frequency to the power of 1.51. As a result, it is necessary to take the losses of the harmonics (up to 49^{th} harmonic) into account, since in the charging mode the inductor current is rich of harmonics. To consider the harmonics losses, the FFT analysis results of the line current shown in Figure 6-5 are used. The total core losses for different designs are presented in Table 6-5.

Step No. 14: Calculate the gap loss, Pg.

The gap loss does not occur in the air gap, itself, but is caused by magnetic flux, fringing around the gap, and reentering the core in a direction of high loss. As the air gap increases, the flux across the gap fringes more and more, and some of the fringing flux strikes the core, perpendicular to the laminations, and sets up eddy currents which cause additional losses called gap loss, Pg. Also distribution of the fringing flux is affected by other aspects of the core geometry, the proximity of the coils turns to the core, and whether there are turns on both legs. Accurate prediction of the gap loss depends on the amount of fringing flux.

$$P_g = K_i E l_g f B_{ac}^2, [W] \quad (6\text{-}16)$$

Where, E is the strip or tongue width in cm and Ki is the gap loss coefficient which is 0.0388, 0.0775, and 0.1550 for two-coil C core, single-coil C core, and lamination, respectively. The gap losses for different designs are presented in Table 6-5.

Step No. 15: Calculate the total inductor losses, Ploss.

$$P_{loss} = p_{cu} + P_{fe} + P_g \tag{6-17}$$

The total losses for different designs are presented in Table 6-5.

Step No. 16: Calculate the inductor surface area, SA and the temperature rise, Tr.

Painstaking accuracy can be employed to calculate the actual surface are of the wound component. However the boundry layer associated with the natural convection in the air tends to round off the surface contours and so the effective convective surface is approximated by the surface area of a box barely enclosing the wound component. For Metglas POWERLITE C-Cores, this area is calculated as follows [79]:

$$SA = 2f(b+d) + 2(b+d)(b+e0+2f(b+e), [cm^2] \tag{6-18}$$

Then the temperature rise of the wound component can be approximated by using the formula below.

$$\Delta T = 315.5(\frac{P_{loss}}{SA})^{0.833}, [^oC] \tag{6-19}$$

The temperature rise for different designes are presented in Table 6-5.

Step No. 17: Calculate the window utilization, Ku.

$$k_u = \frac{n_p N_{Lnew} A_{wb\#2}}{W_a} \tag{6-20}$$

The window utilization factors for different designs are presented in Table 6-5. Steps 1 to 17 were performed in MATLAB and the analysis results are collected in Table 6-5.

Table 6-5 Primary design results of the saturated 150 uH inductor.

Step#	Description	AMCC 630	AMCC 800A	AMCC 800B	AMCC 1000	AMCC 1725	AMCC 1843
Step 1	Desired performance						
Step 2	$V_L I_L$ (W)	16085	16085	16085	16085	16085	16085
Step 3	Ap (Cm^2)	486.2	591.6	798.0	966.0	1725.0	1843.0
Step 4	NL	21.51	17.68	14.65	13.37	6.64	7.75
Step 5	Lg(mm)	5.31	4.32	3.51	3.16	1.35	1.69
Step 6	F	1.49	1.38	1.31	1.28	1.10	1.13
Step 7	NLnew	17.26	14.65	12.37	11.34	5.64	6.55
Step 8	Bac	1.25	1.21	1.18	1.18	1.18	1.18
Step 9	Awb	2.69	2.69	2.69	2.69	2.69	2.69
Step 10	ε (cm)	0.331	0.331	0.331	0.331	0.331	0.331
Step 11	RL	0.3873	0.3569	0.3092	0.2878	0.1653	0.1813
Step 12	Pcu	0.28	0.26	0.22	0.21	0.12	0.13
Step 13	Pfe	5.06	5.80	7.49	8.85	22.31	21.02
Step 14	Pg	9.10	6.94	6.53	6.41	5.28	6.32
Step 15	Ploss	14.44	13.00	14.28	15.48	27.71	27.47
Step 16	ΔT	9.8	8.4	8.0	7.9	8.9	8.7
Step 17	Ku	1.35	1.18	0.85	0.70	0.43	0.40

6.5. Inductor Design Using PExprt

Power Electronics Expert (PExprt) is an interactive, PC-based design tool that uses analytical expressions to design magnetic components, such as transformers and inductors [80]. Libraries of magnetic cores, bobbins, insulators, and conductors allow you to define the model to your exact specifications. Using PExprt, you can do the following:

• Design inductors, multi-winding transformers, coupled inductors.

• Introduce waveform or converter data.

• Optimize constructive parameters, such as core size, core material, number of turns, air gap length, wire gauge, and number of parallel turns.

• Calculate performance parameters, such as winding losses, core losses, flux density, DC and AC resistance, Irms currents, magnetizing inductance, leakage inductance, and temperature rise.

• Consider complex effects, such as skin and proximity effects, fringing flux near the air-gap for energy calculations, and incremental permeability as a function of field strength.

• Generate model netlists for Maxwell, SPICE, PSpice, SIMPLORER, and Saber electrical simulators.

•Use the models with an additional electrical simulator (PSpice, SIMPLORER, or Saber) to analyze the entire power electronics application.

•Calculate winding losses based on FEA field solution.

Rather than resulting a single design alternative, PExpert's output consists of a complete series of valid designs meeting specified design objectives. These results can then be evaluated in terms of several criteria, including power loss and temperature rise.

To design a magnetic component in PExprt, the below general procedure should be followed:

1. Select a design library from the list of stock libraries.

2. Optionally, select cores, wires, and core materials from the design library. Only the selected elements are considered in the design process.

3. Introduce the magnetic component specifications.

4. Optionally, specify design inputs, such as gap position, geometry, thermal constraints, wire spacing, maximum flux density, and maximum number of parallel turns.

5. Optionally, select modeling inputs, such as winding losses and optimization criteria.

6. Generate a list of possible designs that meet your specifications.

7. Select a design, and explore one or more performance results, such as core losses, winding losses, or temperature rise.

8. Select a design, and explore one or more constructive results, such as core size, core material, wire gauge, gap length, or number of turns.

6.6. PExprt Working Window

The main PExprt screen is called the working window [80]. This window contains the areas where you create and define the PExprt model. The working window is divided into four major areas:

- Input/Output Data area
- Elements Information area
- Libraries area
- Graphical Information area

6.6.1. Input/Output Data Area

The Input/Output Data area contains different tabs, depending on the design status. The following three tabs are the ones that initially appear:

• Waveforms tab. This tab is used to define the inductor specifications and waveform.

• Design Inputs tab. This tab is used to define the design inputs.

•Modeling Options tab. This tab is used to define the modeling options.

This area is used to define inputs and other specifications. When the parameters in the Input/Output Data area are changed, the values for related parameters in that window are automatically updated. The graph is also automatically updated in the Graphical Information area.

6.6.2. Elements Information Area

The Elements Information area contains information about each element included in the libraries. When an element in the library tree is selected, its information is displayed in this area.

6.6.3. Libraries Area

PExpert works with libraries in order to select elements (cores, wires, core materials) that you want to be considered during the design process. Two types of libraries are available in PExpert: stock libraries and design libraries. You can create your own stock libraries in order to introduce elements you commonly employ in your applications. These libraries can be composed of custom elements, as well as any of the elements contained in the stock libraries.

A project's design library is the only library that is considered during the design process. All or part of the elements in this library are included during the design process. The PExpert design engine calculates the power losses of all possible combinations of cores, wires, and cores materials that are selected using the specified design library. Using the design library, you can define design constraints by selecting part or only one of the cores, wires, and core materials contained in the design library. Also you can consider multiple combinations of the various cores, wires, and core materials contained in the design library

6.6.4. Graphical Information Area

The Graphical Information area displays different types of graphical information, depending on the design status and which tab is selected in the Input/Output Data area.

6.7. Design Inputs for the Saturable Inductor

To design the inductor, first of all, the design library is stablished based on the data used for the primary design. Then, the design input data should be specified. The parameters which can be entered on the Design Inputs tab of the Input/Output Data area vary depending on the type of magnetic component is specified for the PExprt project. Table 6-6 explains the design input parameters for the inductor and their impact on the total design.

Before explaining the design input parameters, it should be noted that PExpert is a tool for designing magnetic components used in DC/DC converters in which the inductor current includes a major DC component plus the high frequency ripples. In order to be

able to use this tool for designing the saturable inductor, it is assumed that the DC component of the inductor current is ignorable, but the sinusoidal current ripple is remarkable. Also note that PExpert receives the voltage of the inductor as an input and based on the inductance value, calculates its current. Keeping this in mind and considering the high frequency components of the inductor current, the rms value of the inductor voltage in charging mode will be around 50 Vrms. This is the reason why the sinusoidal voltage magnitude given as the input data is larger than the fundamental component of the inductor current multiplied by the inductor impedance.

Table 6-6 Design input data and their impacts.

Parameter	Available Options	Design Impact
Gap	Central Leg, Both Legs, None	Since the fringing energy of the gap can be considered during the design process, the position of the gap determines the value of the gap length.
Geometry	Concentric Component, Planar Component, Toroidal Component	
Permeability	Constant, Permeability as a function of H	When you select this option, PExprt considers the permeability constant or a function of the magnetic field strength.
Ventilation Type	Low, Normal, High	This value determines the film coefficient for the radiation of temperature. Low means close environment, while High means forced ventilation. When you select Low, you obtain a higher temperature rise than when you select High for the same specifications.
Radiation & Convection	Radiation and Convection effects	When you select this option, PExprt considers the Radiation & Convections effects in the thermal calculations.
Ambient Temprature	Ambient Temperature	PExprt calculates temperature values assuming this ambient temperature value.
Bobbin	Include	If this is not selected, PExprt presents designs with no bobbin.

Table 6-6 Continued.

Parameter	Available Options	Design Impact
Winding Setup	2D Winding Setup, 1D "Completely-Full", 1D "Partially-Full"	This parameter determines the most feasible winding strategy in order to create the setup you specify (i.e., to create a 1D analytical-based model or a 2D FEA-based model). The following types of models are available: •2D Winding Strategy: PExprt allows more than one winding in the same layer. For example, two parallel windings may be placed in the same layer. •1D "Completely-Full": PExprt fills the layers with turns, filling the entire window height. •1D "Partially-Full": PExprt allows layers partially filled with turns.
Winding Efficiency	Awire/Awinding (Wire area/Winding area), Spacing	The parameter determines how to modify the wire spacing. The worse the winding spacing, the lower the number of wires that fit in the window.
Fixed Gap	Considered	If this is selected, PExprt generates designs with the gap value defined here. Since the gap is fixed, you cannot optimize the number of turns
Margin Tapes	Window Height and Window Width percentages	PExprt presents solutions with the specified top and central margin tapes.
Limit Values	Maximum Temperature •Bsat/Bmax: This value is specified as a percentage of the saturation flux density. (PExprt is not designed to provide components working above saturation value of the flux density.) •Maximum Gap: This value is specified as a percentage of the window height. •Maximum Parallel Turns •Maximum Number of Layers: This value is particularly useful in the design of planar components, where the cost of the components depends strongly on the number of layers.	PExprt presents solutions with a temperature below the Maximum Temperature value. •Bsat/Bmax is the maximum value of flux density PExprt considers for the calculations. •PExprt presents solutions with a gap length below the Maximum Gap value. •PExprt uses the Maximum Parallel Turns value for the maximum number of parallel windings to be considered during the design process. •PExprt uses the Maximum Number of Layers value for the maximum number of layers to be considered during the design process.

In addition, several optional modeling options are introduced, in order to improve the accuracy of the results. Table 6-7 explains the modeling option input parameters and their impact on the total design.

Table 6-7 Modeling option input parameters and their impact on the total design.

Parameter	Available Options	Design Impact
Winding Losses Calculation	Irms and DC Resistance, Harmonics and AC Resistance (Skin), Harmonics and AC Resistance (Dowell). To account for the Harmonics in the losses calculation, specify how many harmonics to consider during the design process. You can introduce this information specifying the number of harmonics or by means of the relative influence of one harmonic with respect to the previous one.	During the design process, there are three possible ways to calculate the losses in the conductors: •Irms and DC Resistance: Winding losses are calculated as: $P = I_{rms}^2 * R_{DC}$ •Harmonics and AC Resistance (Skin): Winding losses are calculated as: $P = I_{DC}^2*R_{DC} + I_{rms\_1}^2*R_{AC\_1} + I_{rms\_2}^2*R_{AC\_2} + I_{rms\_3}^2*R_{AC\_3} + ...$ •Harmonics and AC Resistance (Dowell): Winding losses are calculated as: $P = I_{DC}^2*R_{DC} + I_{rms\_1}^2*R_{AC\_1} + I_{rms\_2}^2*R_{AC\_2} + I_{rms\_3}^2*R_{AC\_3} + ...$
Core Losses Calculation	Steinmetz, Jiles Atherton (hysteresis) and Jiles Atherton (hysteresis) + Eddy	During the design process, there are three possible ways to calculate the losses in the conductors: •Steinmetz: Core losses are calculated using Steinmetz equation •Jiles Atherton (hysteresis): Core Losses are calculated using Jiles Atherton model. Therefore, only hysteresis losses are considered. •Jiles Atherton (hysteresis) + Eddy: Hysteresis core Losses are calculated using Jiles Atherton model. Eddy core losses are considered using an additional analytical model.
Optimize number of turns for minimum losses	No Optimization, Apply Optimization (for Mode 1 or Mode 2)	If you select No Optimization, PExprt does not iterate to find the lower losses solution for each combination of core/wire/material. If you select Apply Optimization, PExprt optimizes using two possible approaches (Mode 1 or Mode 2).
List of Results	Show all solutions, Selection	PExprt calculates all solutions meeting initial specifications, but you can configure which ones to present. If you select Show all solutions, PExprt shows all meeting specifications. If you select Selection, only those that meet the selection criteria are included on the List of Results tab.
Selection of elements from the Design Library	Apply Restrictions, No Restriction (all possible configurations)	If you want to use all the elements you have selected in the design library for the design process, select No Restrictions. However, if you have selected many elements in the design library, and you do not know how many of them make sense to be considered in the design, select Apply Restrictions to allow PExprt to select the appropriate elements for your design.

The design input data considered for the design of the saturable inductor are depicted in Figure 6-6 to Figure 6-8 and their description and impacts on the design are already explained in Tables 6-6 and 6-7.

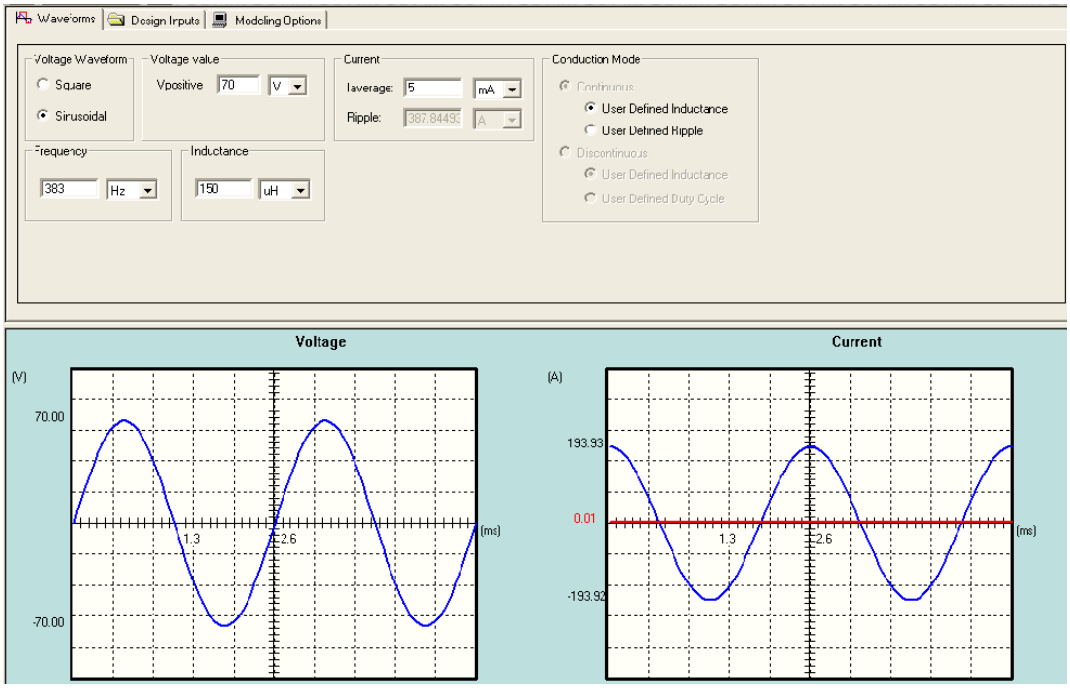


Figure 6-6 Waveforms tab in the input/output data area.

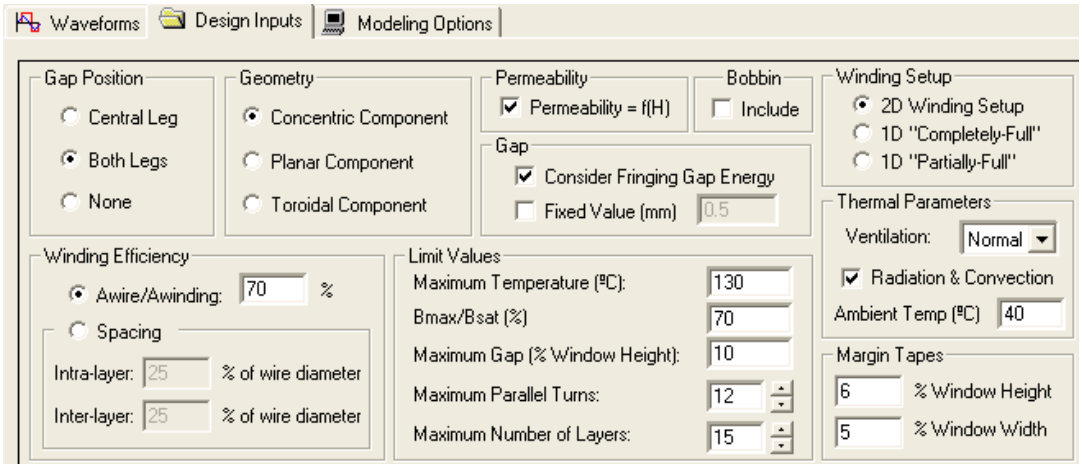


Figure 6-7 Design inputs tab in the input/output data area.

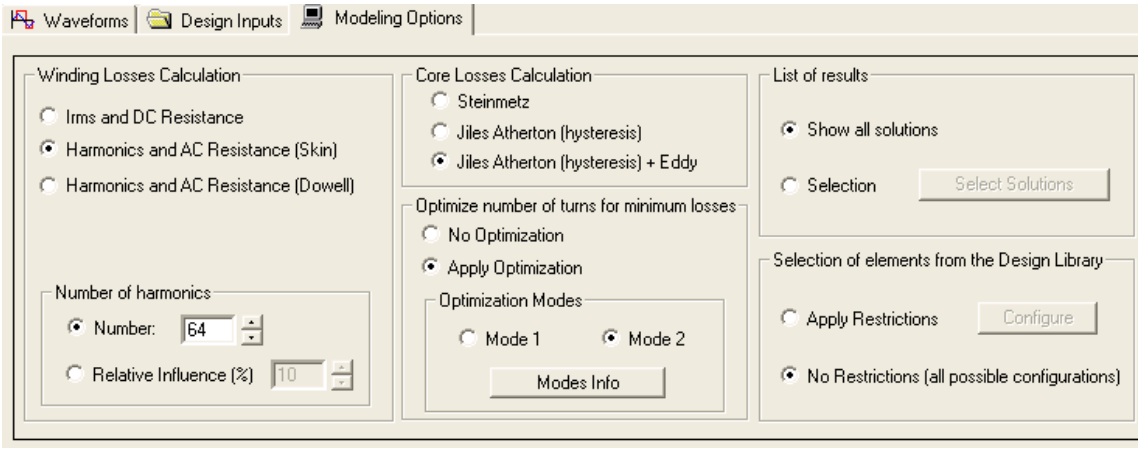


Figure 6-8 Modeling options tab in the input/output data area.

After the design library is selected and the design input data are defined, it is time to generate designs and explore the solution results. The list of results are appeared on the List of Results tab of the Input/Output data area shown in Figure 6-9.

After generating various designs for this particular inductor (Figure 6-9), the highlighted design with the detailed specifications shown in Figure 6-10 has been selected as the final design since it meets the desired performance and is more feasible to be fabricated. Now the performance results of the currently selected design can be explored in detail. Figure 6-10 presents the detailed results for this design.

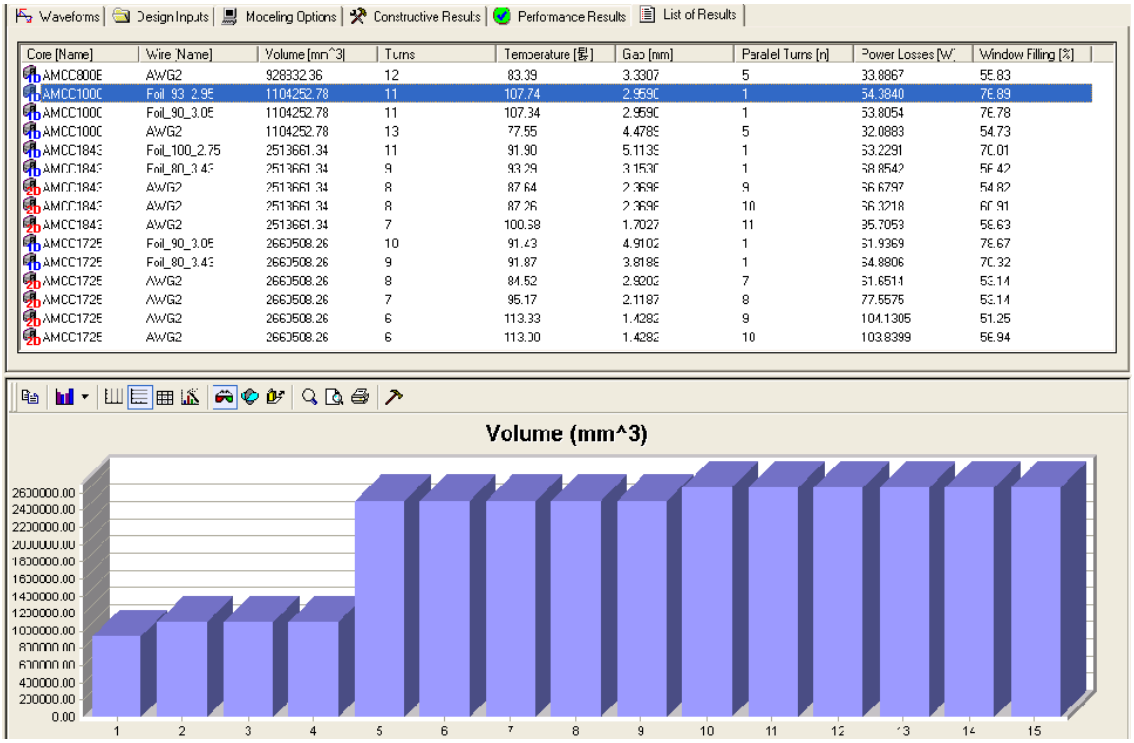


Figure 6-9 List of results tab of the input/output data area.

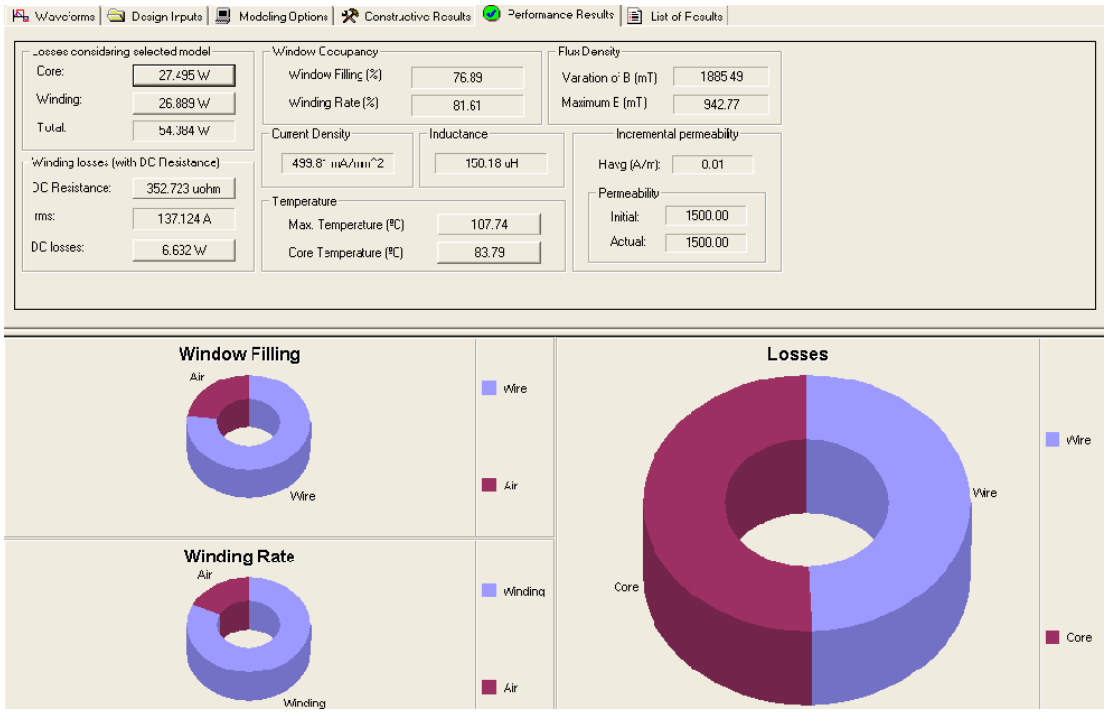


Figure 6-10 Performance results tab for the design in the input/output data area.

Figure 6-11 displays the Constructive results tab in the Input/Output Data area and the cross-section of the current design in the Graphical information area.

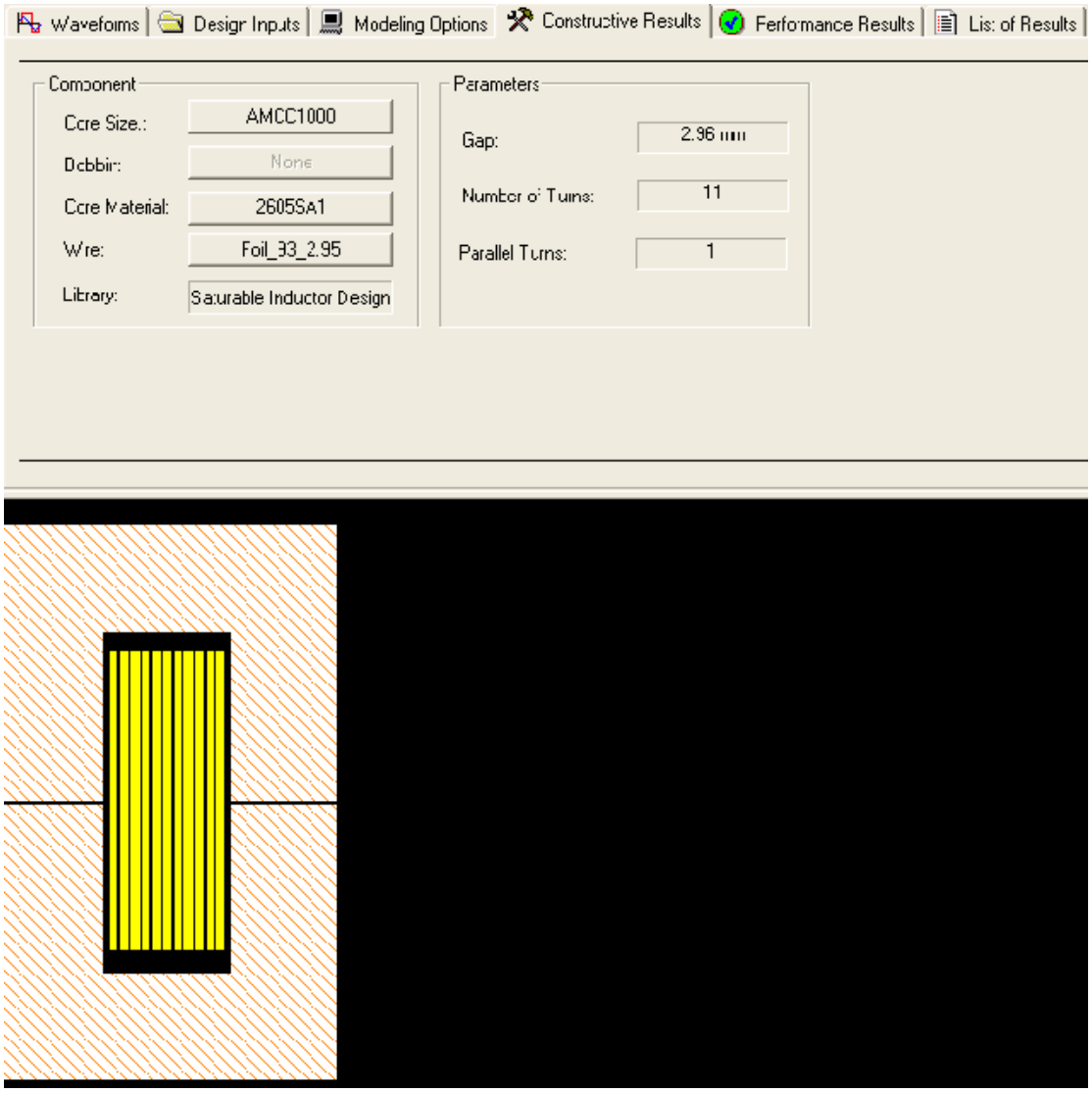


Figure 6-11 Constructive results tab in the input/output data area.

6.8. FEA of the Designed Inductor

As it was expected, the primary design and the PExprt design procedures almost resulted in similar results. Considering the required inductance, core size, volume, power

loss, temperature rise the design consists of the core AMCC1000, 11-turn foil winding , two air-gap with total length 2.96 mm. The size and wait of the core is shown in Table 6-5. In this section the inductor, shown in Figure 6-12 is modeled with Maxwell 2D in order to confirm its saturation performance under different loads.

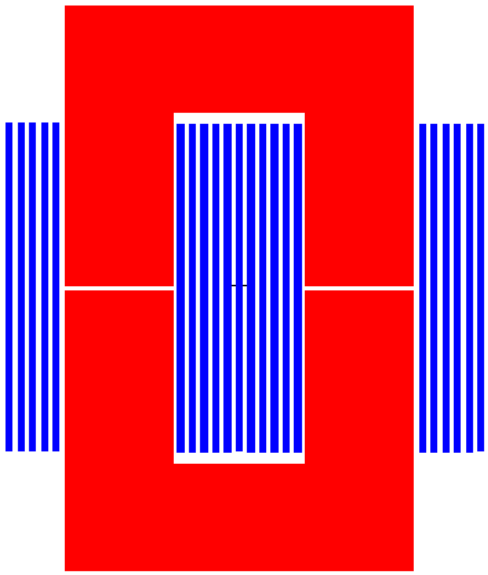


Figure 6-12 The schematic of the designed saturable inductor.

Figure 6-13 and Figure 6-14 show the flux lines and the flux densities for100 and 1200 Apeak inductor current, respectively. As it is desired, at 100 A inductor current which is considered as the charging mode maximum current, the core operates at linear operating area and at 1200 A which is considered as the discharging mode maximum current, the core is completely saturated and experiences a 1.5 T flux density which is the maximum flux density of the core material.

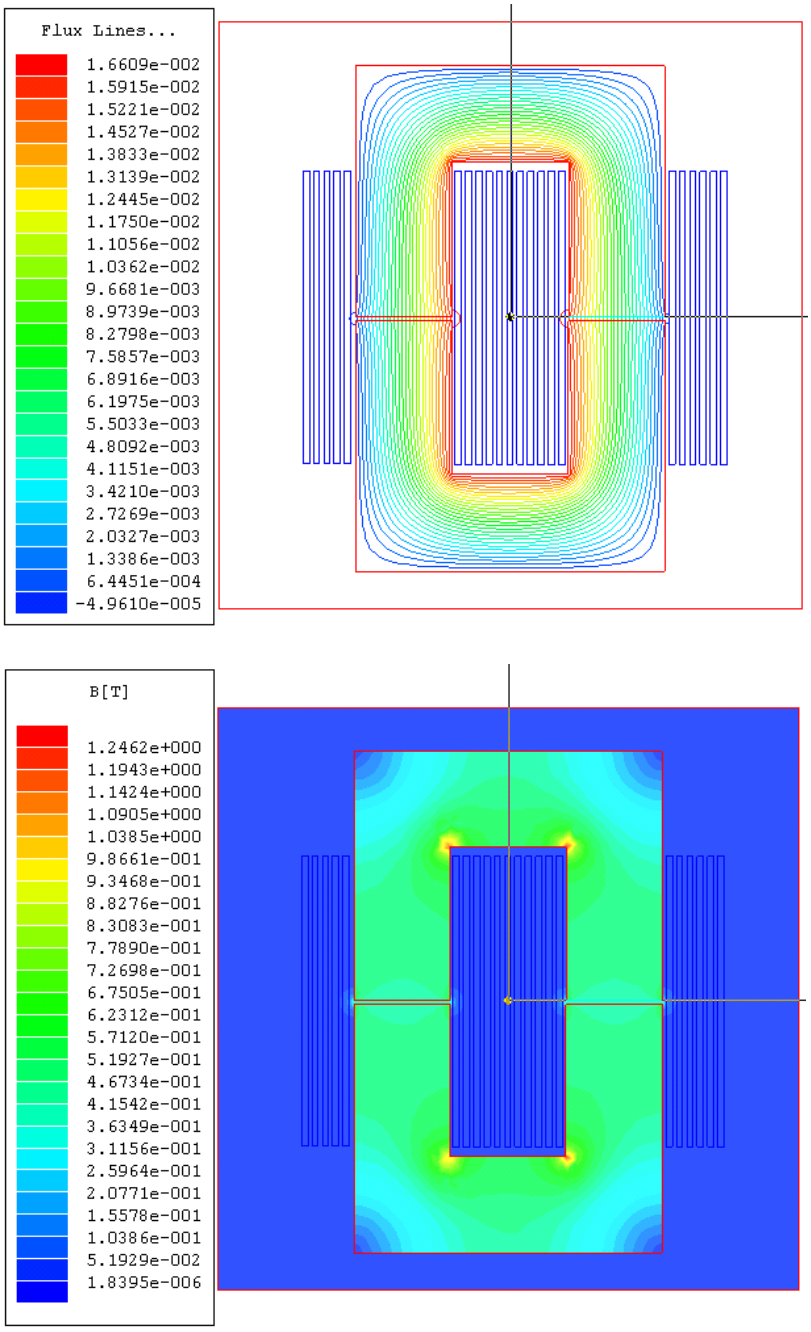


Figure 6-13 Flux lines and flux density of the inductor at I_L =100 A.

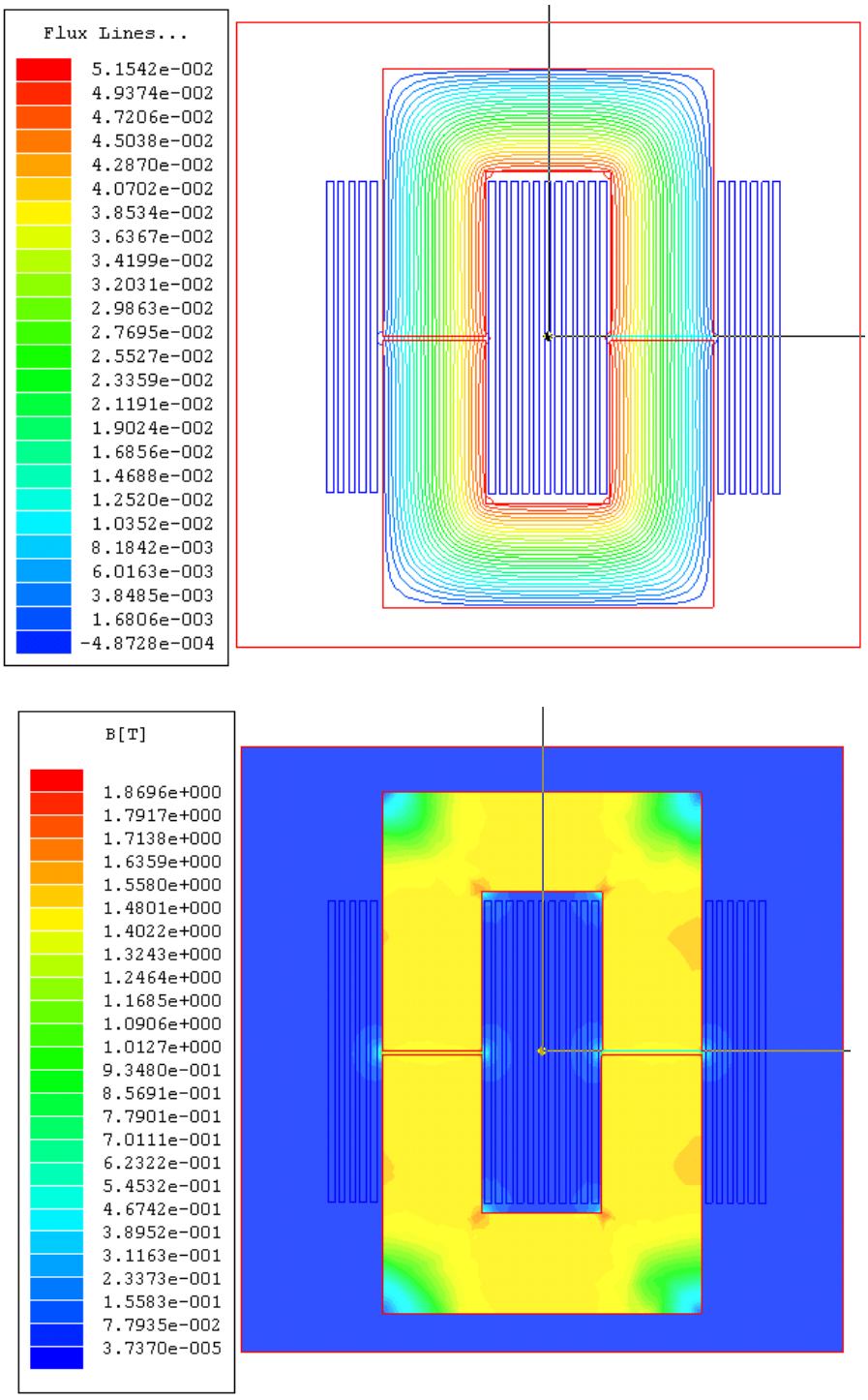


Figure 6-14 Flux lines and flux density of the inductor at I_L =1200 A.

Finally, the flux-turn and the inductance values against inductor current are depicted in Figure 6-15 and Figure 6-16, respectively. The figures are in strong agreement with the required performance of the designed inductor.

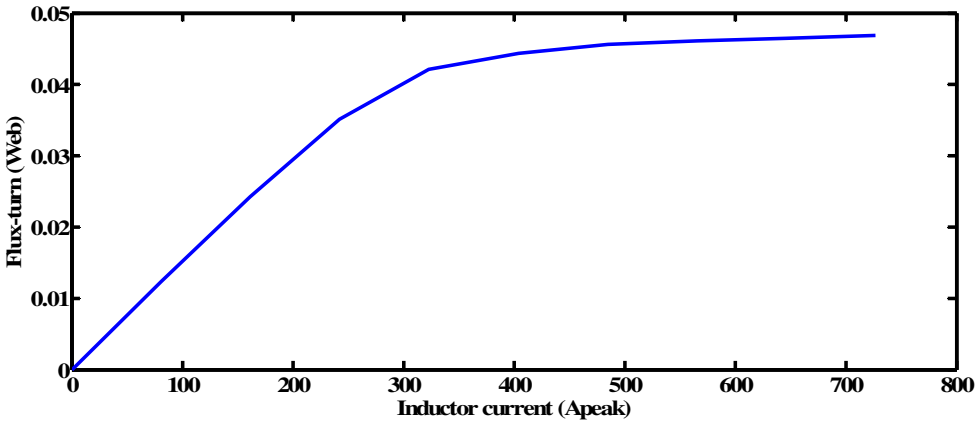


Figure 6-15 Flux-turn vs. inductor current.

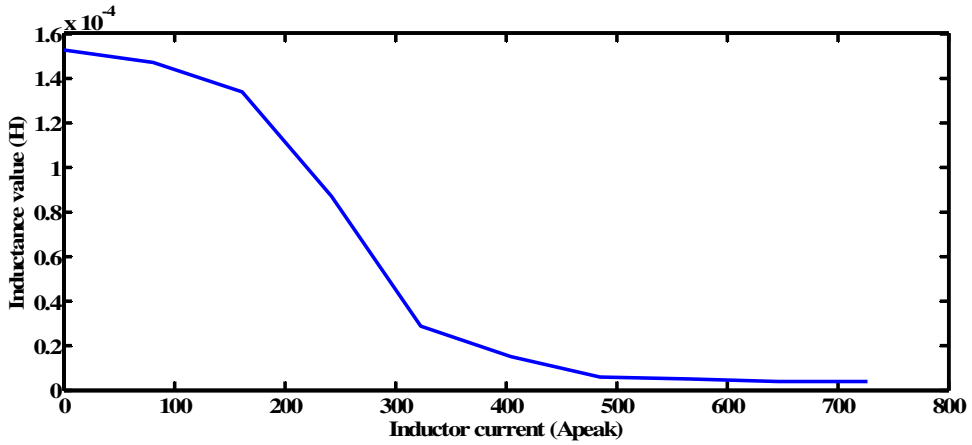


Figure 6-16 Inductance value vs. inductor current.

7. DSP CODE DEVELOPMENT AND EXPERIMENTAL RESULTS

7.1. Hardware Organization

The block diagram of the laboratory experimental setup is given in Figure 7-1. Experiments have been performed on an emulated FESS including a 2.5 kW 4-pole PMSM as a motor/generator, a 7.5 hp 4-pole induction machine (IM) as a load/motor, the 240 kW inverter/rectifier, a resistor panel as a DC bus load, a V/f control IM drive, an interface board, and eZdsp™ TMS320F2812 controller board. The control algorithms have been developed on the DSP TMS320F2812. Figure 7-2 shows the experimental setup used for the test.

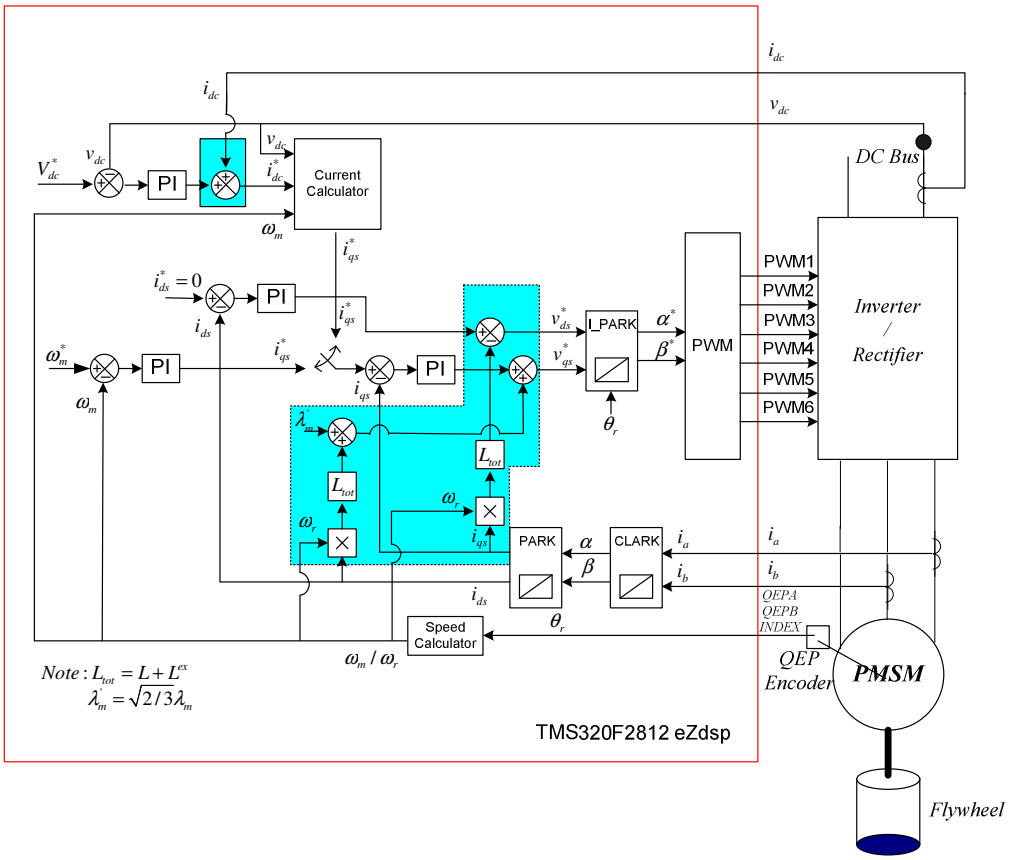


Figure 7-1 Overall block diagram of the experimental setup.

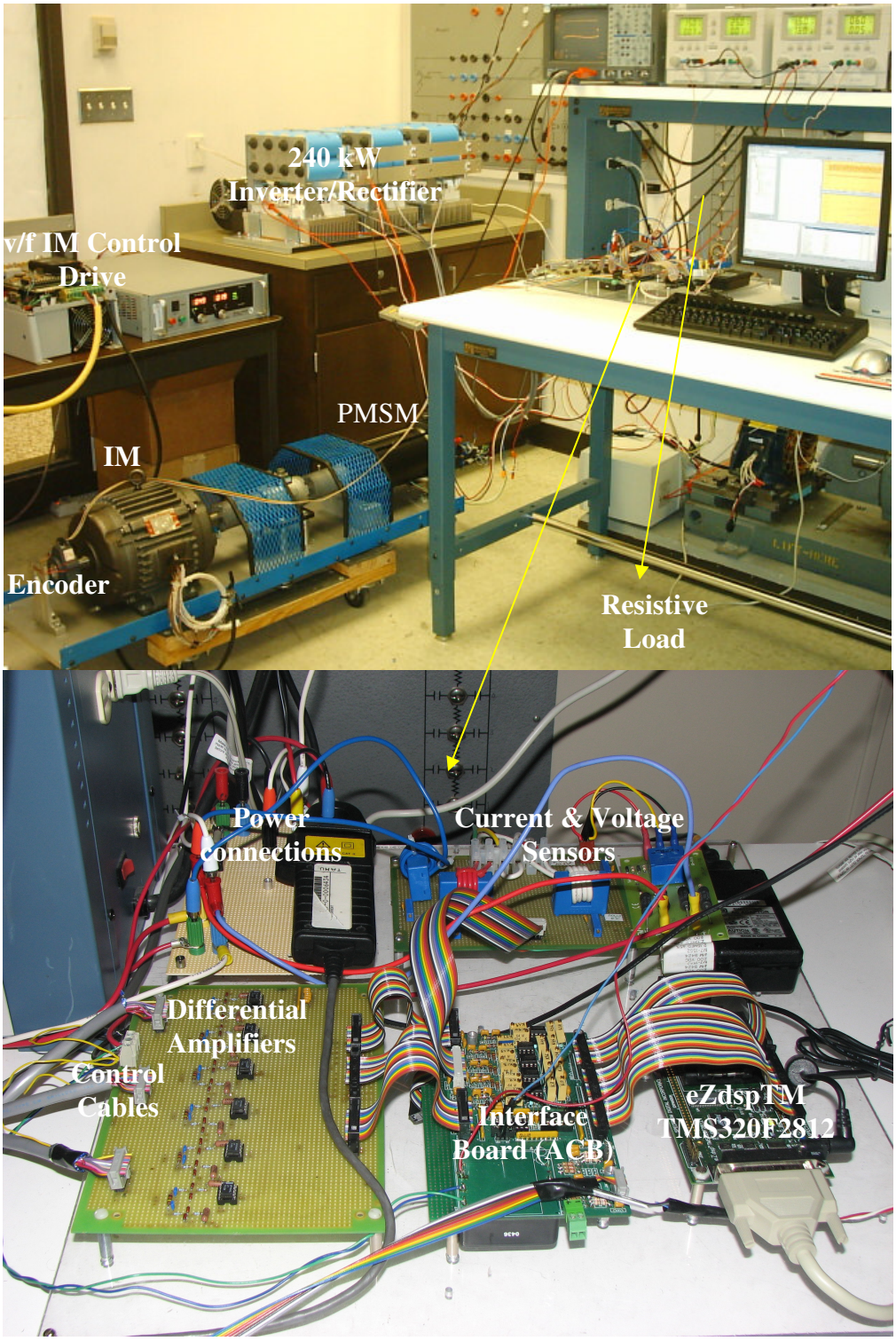


Figure 7-2 Experimental set-up.

The back-EMF of the PMSM at the shaft speed of 1000 rpm is shown in Figure 7-3. The peak-to-peak line voltage is 126 volts. To detect the rotor position an incremental shaft encoder with resolution of 1024 pulse per revolution is used.

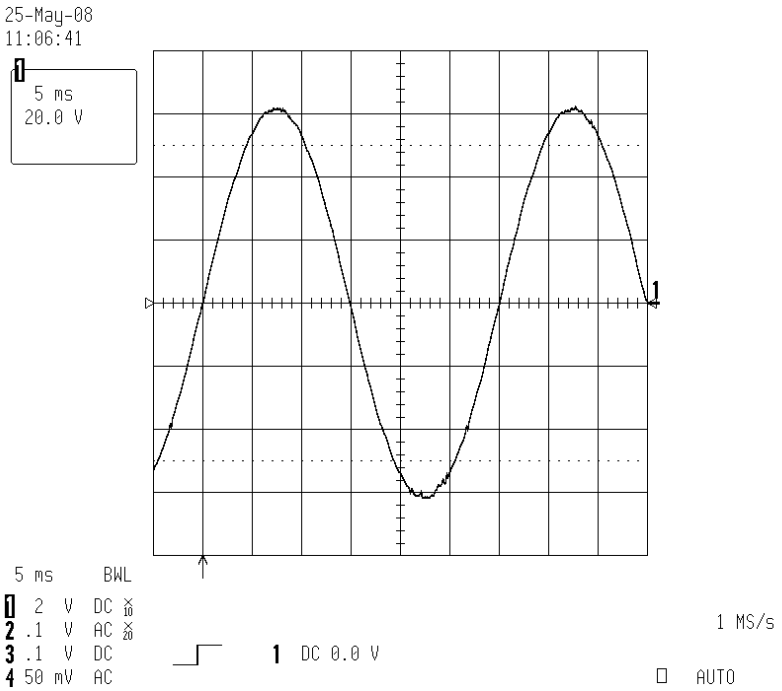


Figure 7-3 Line-to-line back-EMF of the PMSM at 1000 rpm.

In motoring mode, the IM plays the role of the load of the PMSM and in the regenerative mode it emulates the flywheel performance. Therefore, in the regenerative mode, the v/f control IM drive reduces the speed of the PMSM through controlling the IM speed and it provides the PMSM with the power demanded by the DC bus load. As illustrated in Figure 7-1 and Figure 7-2, the PMSM is driven by the voltage-source inverter during charging mode and supplies the PWM rectifier during discharging mode.

The controller of the emulated FESS is served to read the feedback signals, phase a and b currents, DC bus voltage and current and position signals, implement the speed or

torque, current and voltage control algorithms and finally generates the gate driver PWM signals by means of space vector PWM modulation technique. TMS320F2812 has been used as the controller. The schematic of the interface of TMS320F2812 is illustrated in Figure 7-4. Four input channels related to the 10-bit Analog-to-Digital Converter (ADC) are selected to read the two-phase currents, DC bus voltage and current and then transfer the 0-3.0 V analog signal desired values. PWM1-PWM6 channels are used as the output of the controller.

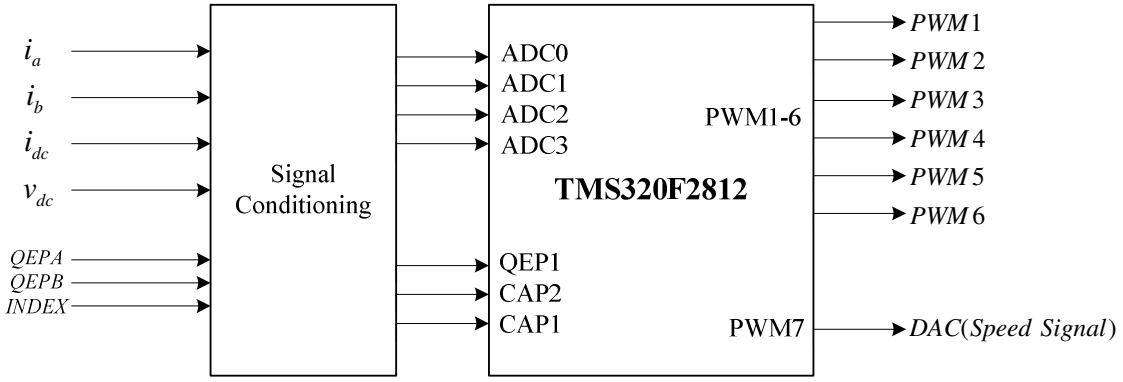


Figure 7-4 The interface of TMS320F2812.

Theoretically, the field oriented control for the PMSM drive allows the motor/generator torque be controlled independently with the flux like DC motor operation [63]. In other words, the torque and flux are decoupled from each other. The rotor position is required for variable transformation from stationary reference frame to synchronously rotating reference frame. As a result of this transformation called Park transformation, q-axis current will be controlling torque while d-axis current is forced to zero. Therefore, the key module of this system is the information of rotor position from the QEP encoder.

The encoder coupled to the IM shaft generates two quadrature pulses and one index pulse. These signals are shown in Figure 7-1 as QEP_A, QEP_B and QEP_index. These signals are applied to TMS320F2812 CAP/QEP interface circuit to determine the motor speed, position and direction of rotation.

7.2. Software Organization

The body of the software consists of two main modules, the initializing module and the PWM interrupt service routine (ISR) module. The first one is executed only onece at the startup. The second module interrupts waiting loop by the PWM underflow. When the interrupt flag is set, the corresponding ISR is served. Figure 7-5 shows the general structure of the software. The complete control algorithm is executed within the PWM ISR so that it runs at the same frequency of switching frequency or at a fraction of it. The waiting loop can be easily replaced by a user interface.

7.3. Experimental Results

The experimental setup is illustrated in Figure 7-2. This set-up is to verify the control algorithm performance, especially, in regenerative mode which is more challenging. During the motoring mode a DC power supply is exciting the DC bus and during the discharging mode this power supply is switched off, and the resistor panel is paralleled with the DC bus and plays the role of the load.

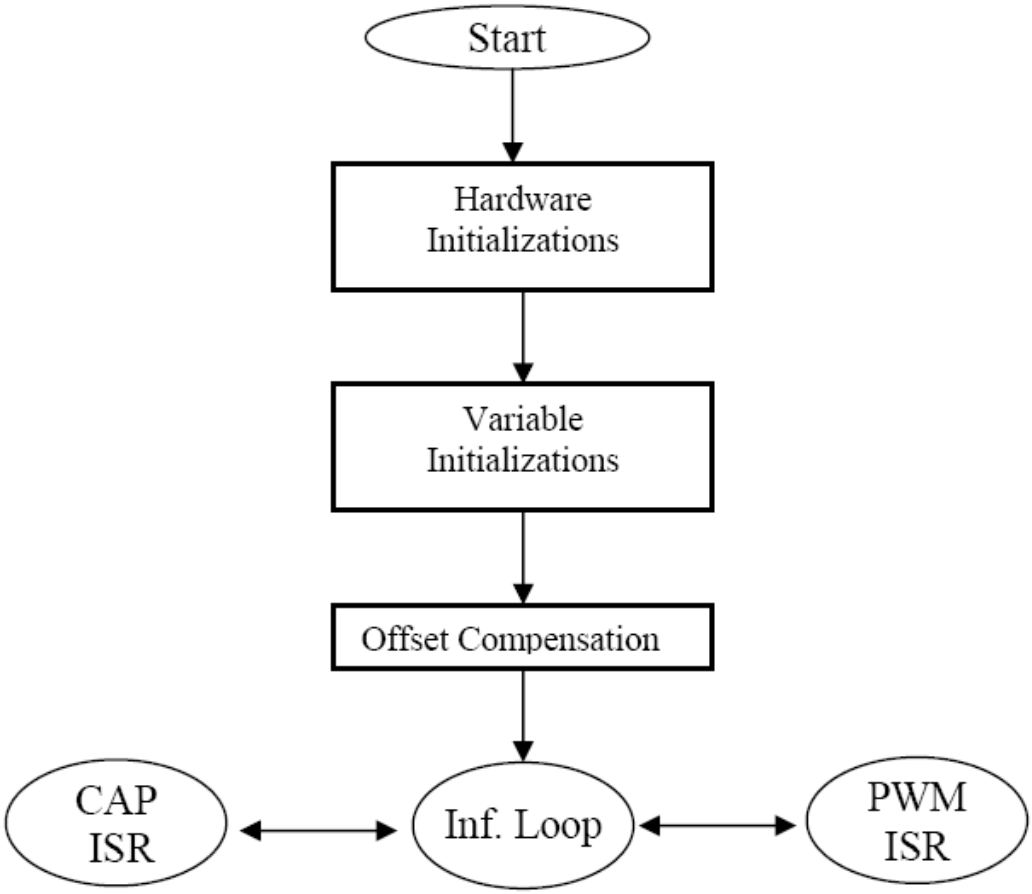


Figure 7-5 General structure of the software.

Since the internal current and voltage sensors of the inverter provide the normalized analog signals relative to the nominal rating of the devices (1200 A and 900 V), in the experiments, the output analog signals are very close to zero. Because of that, external voltage and current sensors shown in Figure 7-2 are used for measuring the signals.

In this section the most critical focus has been done on the regenerative mode and several tests have been performed to verify the consistency of the control algorithm in this mode. As mentioned before, a V/f control IM drive was used to emulate the flywheel performance. In other words, the V/f control IM drive reduces the speed as it is

commanded and provides the PMSM with the required power by the DC bus load and the entire losses. The only difference between a real FESS and the emulated system is that in a FESS, the DC bus load determines the deceleration of the flywheel and PMSM speed but in the emulated system, the deceleration is controlled by an input signal, speed set point. So basically there is no remarkable difference between the FESS and the emulated system and it can demonstrate the consistent performance of the control algorithm.

The experiments were managed step by step as following:

- The DC power supply is switched on to source the DC bus of the inverter.
- The PMSM is run as a motor in order to monitor the rotor position through the encoder attached to the IM shaft and have the right initial angle in the starting of the regenerative mode.
- The motor speed set point is set to zero and when it is stopped, the mode of operation is switched to regenerative mode.
- The IM speed is increased to a set point in which the pick value of the PMSM line voltage is almost equal to the DC power supply voltage.
- The DC power supply is switched off and the DC bus load is switched on, instantly.
- By means of the v/f control IM drive, the speed is reduced and the DC bus voltage, PMSM line-to-line voltage, phase current, and speed signals are monitored.

Before the experiment results are demonstrated, to have an idea about how the open loop system works, the following test has been performed and the results are depicted in Figure 7-6. The test is done such that the v/f control IM drive runs the PMSM at 830 rpm. The PMSM terminal voltage is rectified by the diode rectifier configured by the devices anti-parallel diodes when the inverter/rectifier IGBTs are off. The PMSM and

the diode rectifier source a 32 Ω resistive load, in parallel with the rectifier DC bus. As shown, the line voltage is clamped by the DC bus capacitors and the phase current looks rich in harmonics. Moreover, the voltage and current magnitudes are dependent on the speed of the drive and in case of change in speed, all other parameters vary.

The previous experiment emphasizes the importance of a closed loop controller in order to be able to maintain the DC bus voltage as well as optimizes the phase current when the PMSM speed varies in a wide range. The following experiments represent the performance of such a controller.

For all experiments, the DC bus voltage set point is 50 V. Figures 7-7 to 7-12 illustrate the emulated FESS performance at no load. Actually, it shows the performance of the system at different speeds. Obviously, the DC bus voltage doesn't change in a wide range of the speed, 830 rpm – 135 rpm. The line-line voltage shown in Figure 7-8 shows that the inverter performs in six-step mode, because the back-EMF and the DC bus voltage are equal at 830 rpm. At all speeds the phase current is low enough to compensate for the PMSM and the rectifier losses.

Note that the speed signal is read from DAC channel of the DSP. Since the DSP calculates the speed based on the QEP Encoder signals considering the rotational direction, the speed range, 0-3000 rpm, will be measurable by a 0-1.5 V signal at the DAC channel. Moreover, using x10 probe for more clarity, the speed range 0-3000 rpm is mapped to a 0-150 mV signal on the oscilloscope screen.

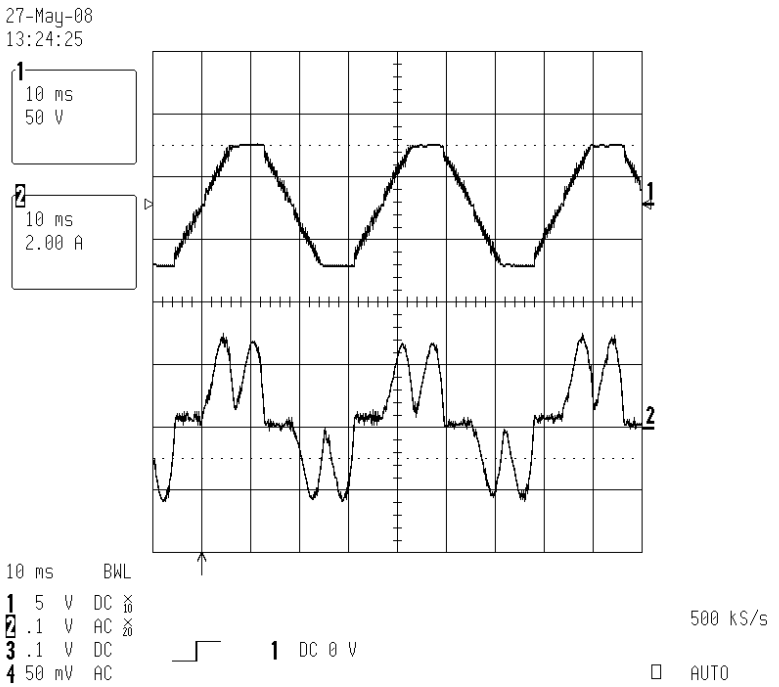


Figure 7-6 Line-to-line voltage and phase current of the PMSM at 830 rpm and under a 32 Ω resistive load.

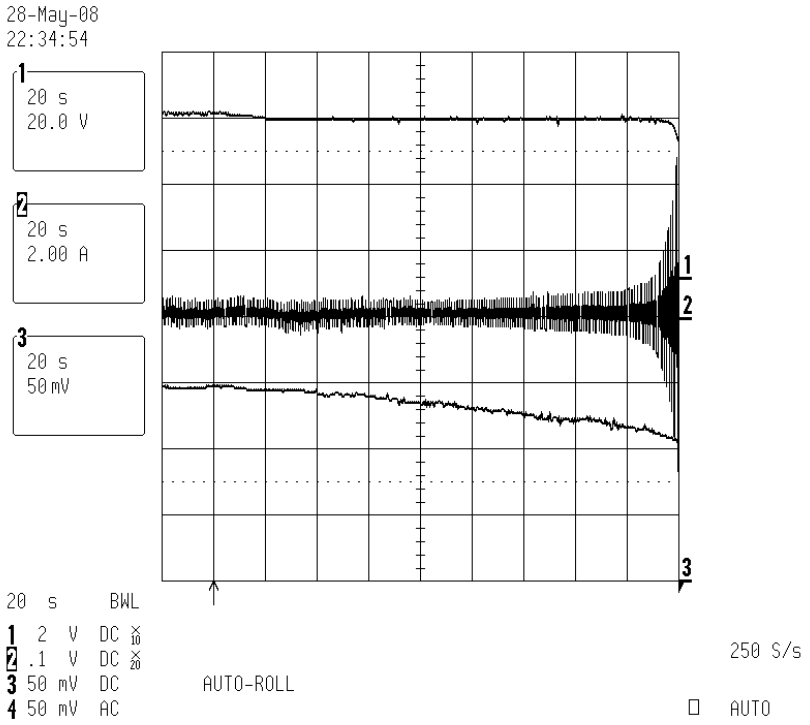


Figure 7-7 Regenerative mode at 830-100 rpm and at no load, Trace 1: DC bus voltage, Trace 2: Phase current, Trace 3: PMSM speed.

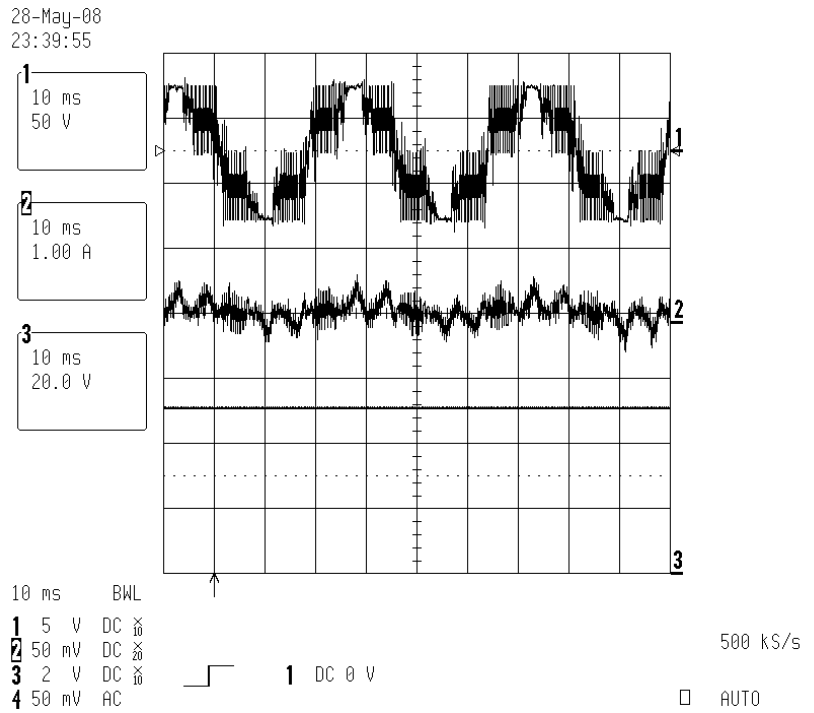


Figure 7-8 Regenerative mode at 850 rpm at no load, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

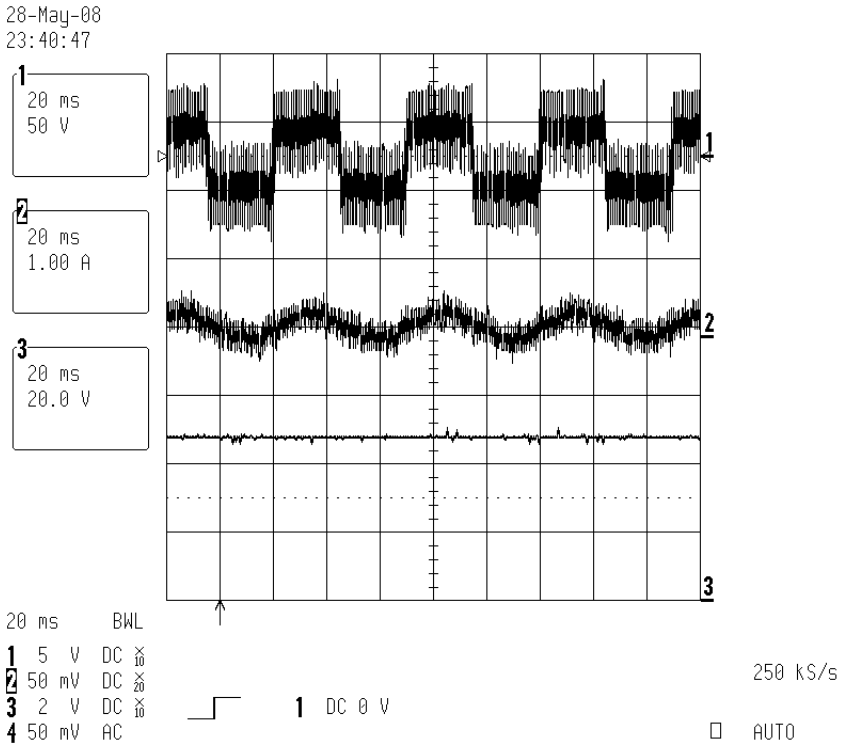


Figure 7-9 Regenerative mode at 600 rpm and at no load, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

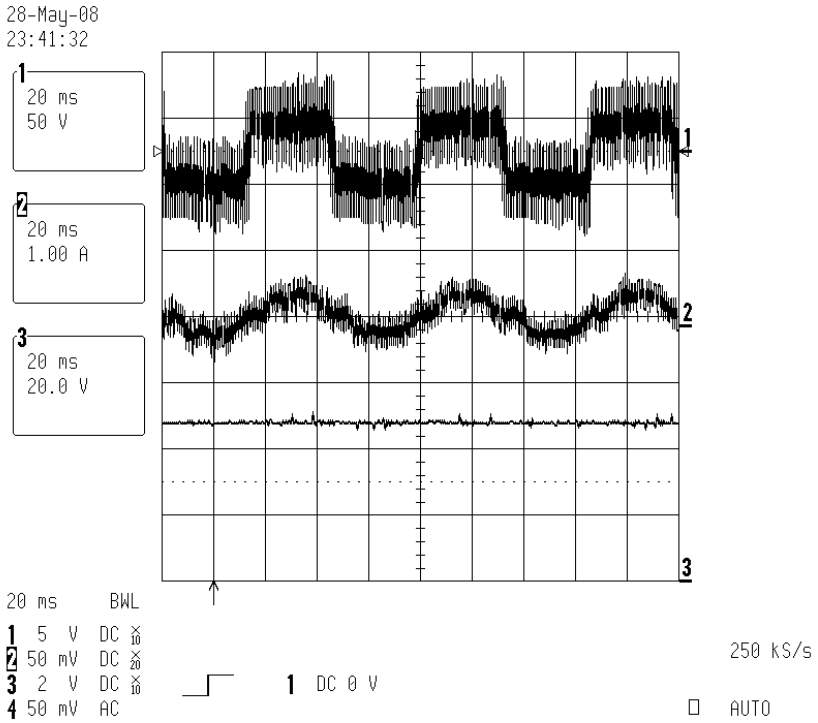


Figure 7-10 Regenerative mode at 450 rpm and at no load, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3:DC bus voltage.

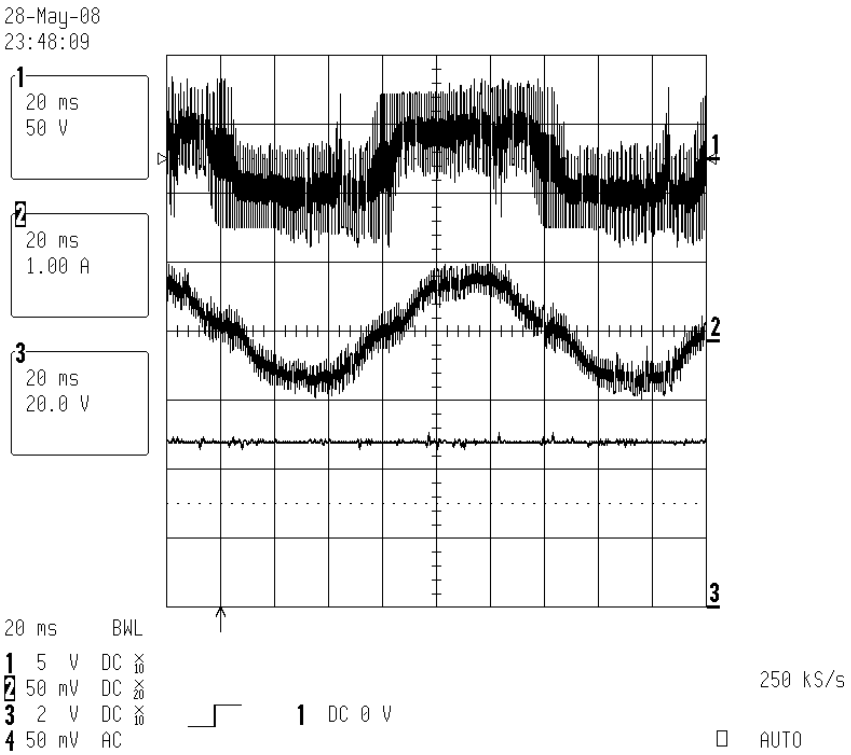


Figure 7-11 Regenerative mode at 250 rpm and at no load Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

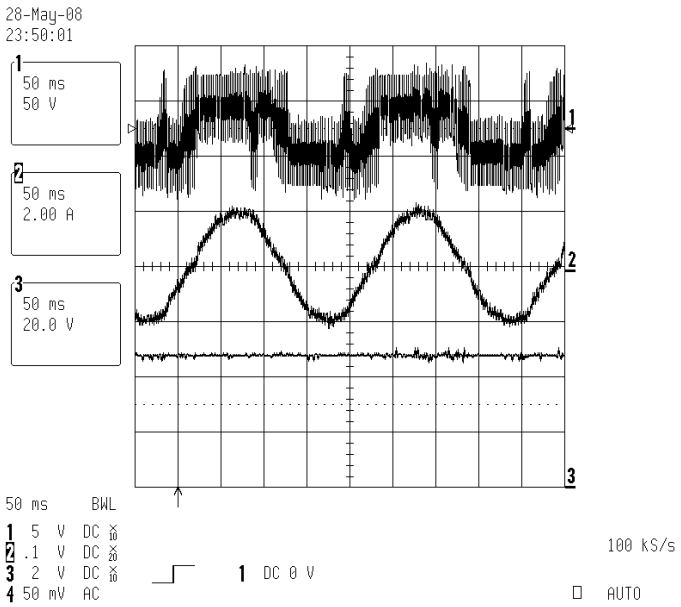


Figure 7-12 Regenerative mode at 140 rpm and at no load, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

Figures 7-13 to 7-22 illustrate the emulated FESS performance while sourcing a DC bus load, Rl = 32 Ω, Idc = 1.6 A. Figures 7-13 to Figure 7-14 illustrate the transients during the connecting and disconnecting the DC bus load when the PMSM is running at 750 and 600 rpm, respectively. Actually, this is the worst disturbance that might be considered for the system. As shown in Figure 7-14, the worst case scenario, the DC bus voltage drops 3 V and less than 2 seconds it builds up and settles at the set point. Also Figure 7-14 illustrates the over voltage of the DC bus when the load is disconnected from the DC bus. As it is shown, the DC bus over voltage will be around 3 V and then it reduces to zero in less than 2 seconds. Note that this high qualified performance is resulted by implementation of the feed forward (FF) block diagram shown in Figure 7-1 as part of the DC bus voltage-loop controller. Otherwise, the undershoot and overshoot of the DC bus voltage for the same load cycle will be almost four times larger as shown in Figure 7-15.

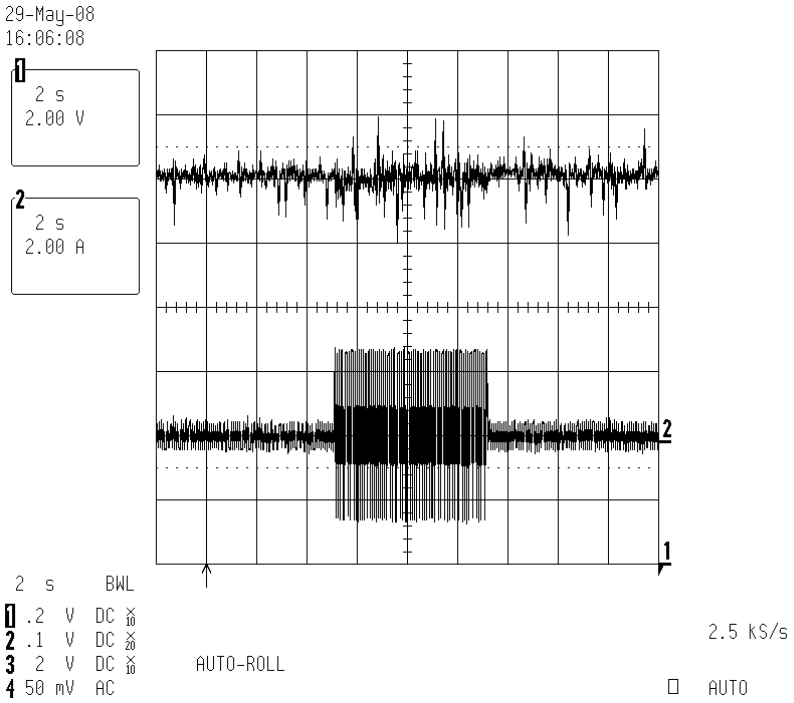


Figure 7-13 Connecting and disconnecting the DC bus load at 750 rpm, with the FF controller (Rl = 32 Ω, Idc = 1.6A), Trace 1: DC bus voltage, Trace 2: Phase current.

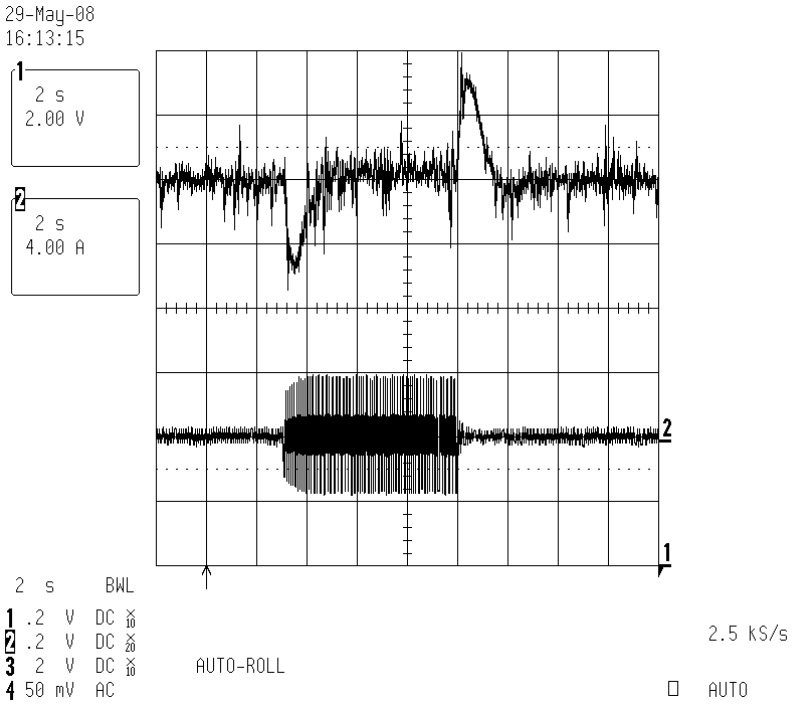


Figure 7-14 Connecting and disconnecting the DC bus load at 600 rpm, with the FF controller (Rl = 32 Ω, Idc = 1.6A), Trace 1: DC bus voltage, Trace 2: Phase current.

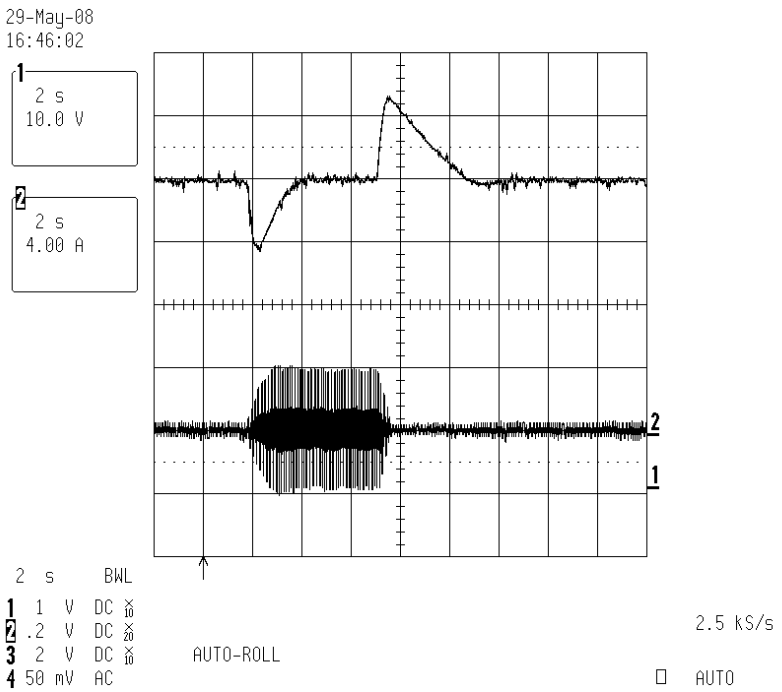


Figure 7-15 Connecting and disconnecting the DC bus load at 600 rpm, without the FF controller (Rl = 32 Ω, Idc = 1.6A), Trace 1: DC bus voltage, Trace 2: Phase current.

Regardless of the loading instance, as it is shown in Figure 7-16, the DC bus voltage stays at the set point, 50 V, for a wide range of speed, 850 rpm – 270 rpm.

As mentioned before, at 875 rpm (Figure 7-17), the peak of the line back-EMF of the PMSM is equal to the DC bus voltage, 50 V. As a result, there is not sufficient voltage difference between these two voltages such that it produces the phase current in a sinusoidal form, but as the speed reduces the current wave form becomes more sinusoidal. It is seen that at 280 rpm the current wave is purely sinusoidal. Moreover, in Figure 7-16 and Figure 7-22 at around 330 rpm a resonance occurs between the DC bus capacitor and the motor inductors.

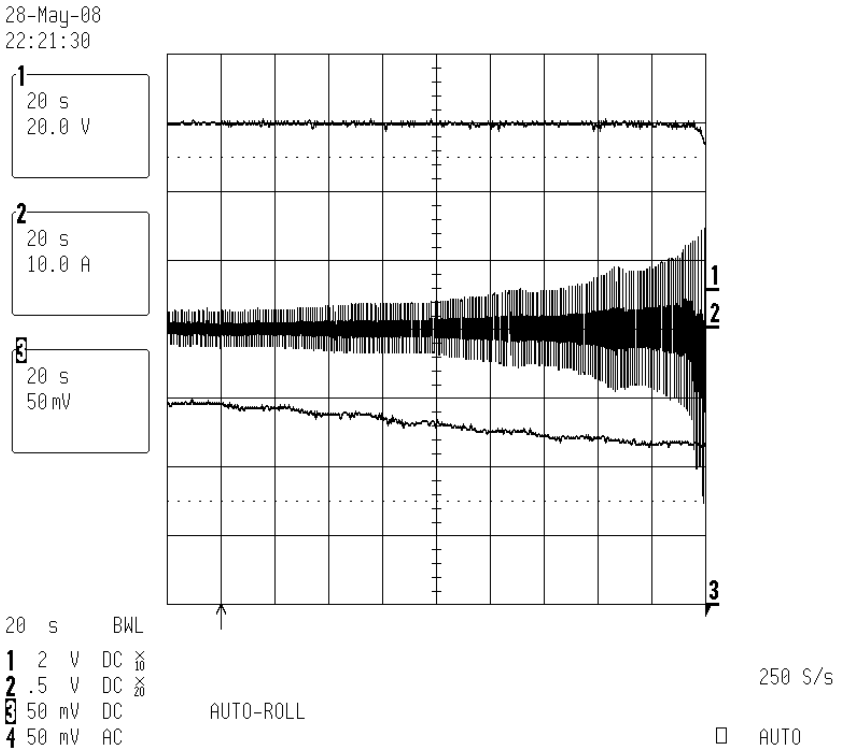


Figure 7-16 Regenerative mode at 850 - 275 rpm and Rl = 32 Ω, Idc = 1.6 A, Trace 1: DC bus voltage, Trace 2: Phase current Trace 3: PMSM speed.

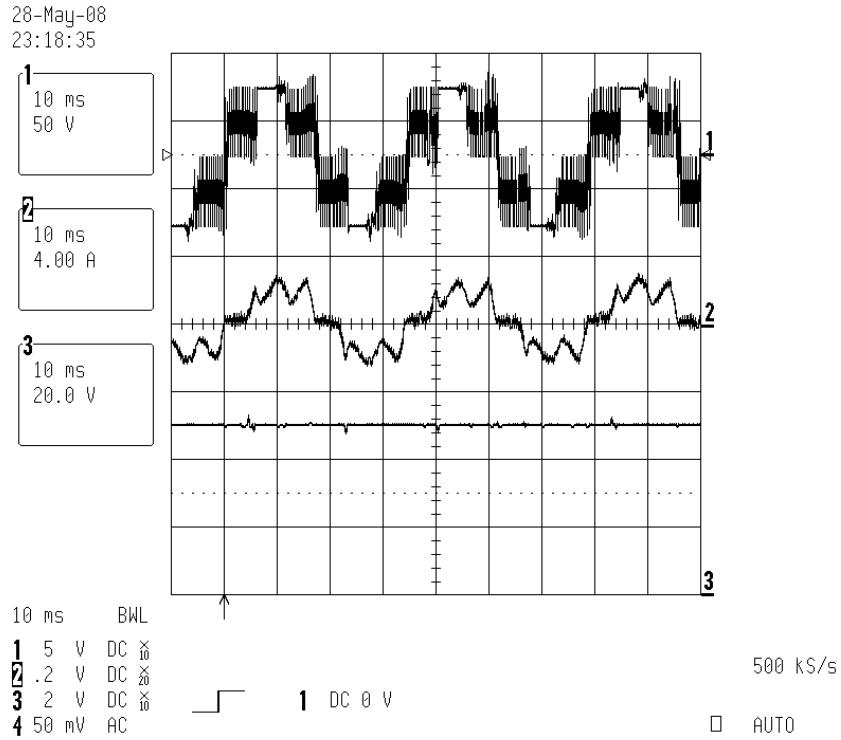


Figure 7-17 Regenerative mode at 875 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

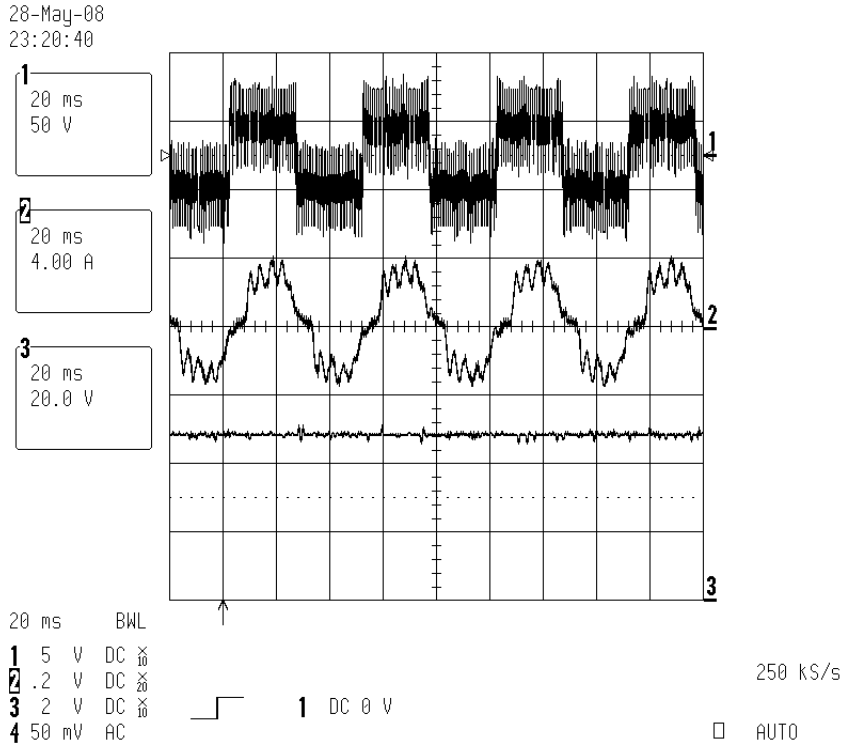


Figure 7-18 Regenerative mode at 600 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

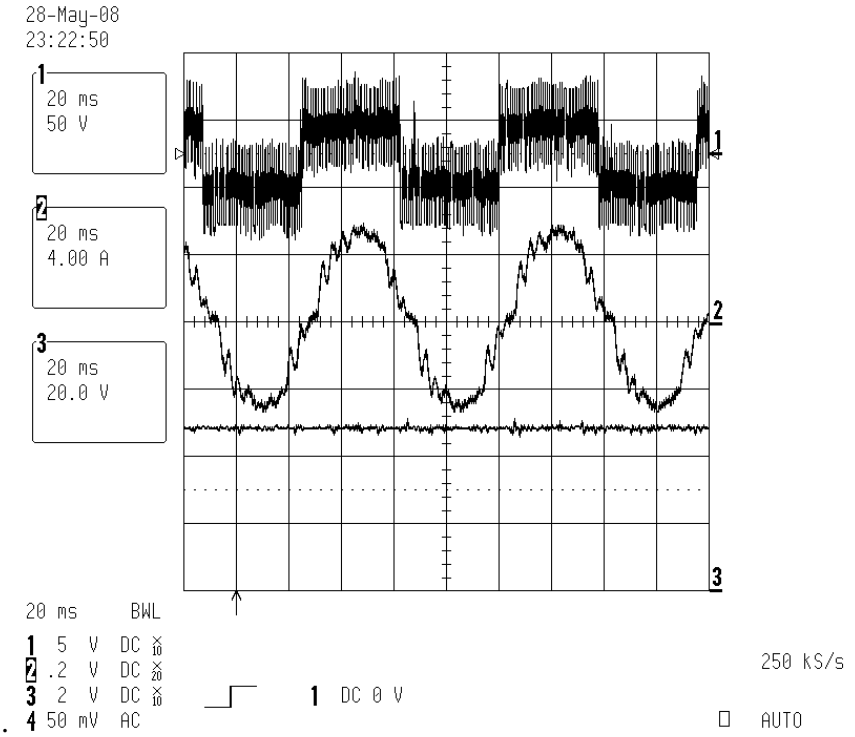


Figure 7-19 Regenerative mode at 400 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

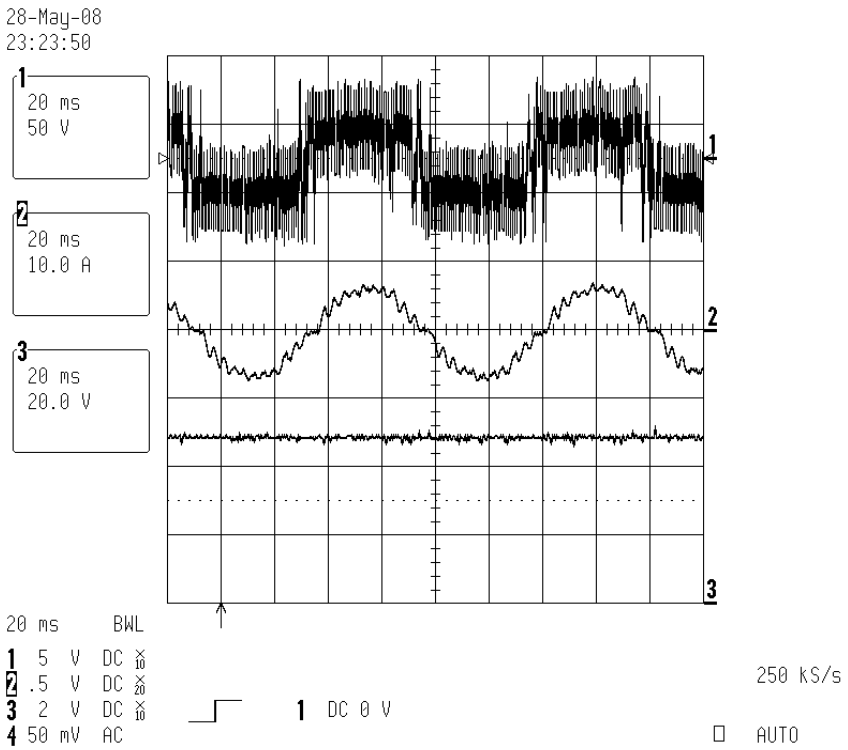


Figure 7-20 Regenerative mode at 350 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

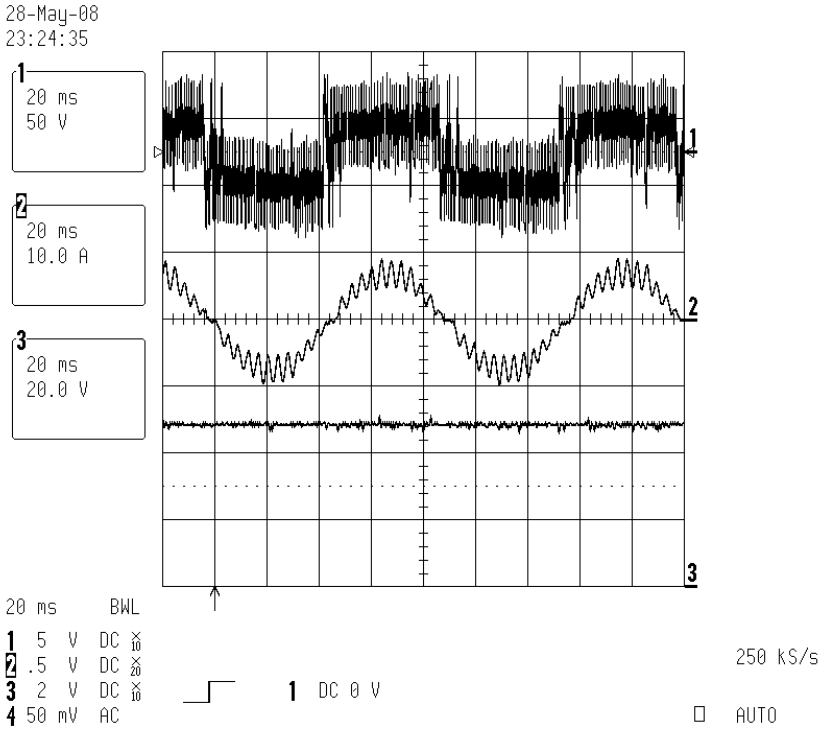


Figure 7-21 Regenerative mode at 330 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

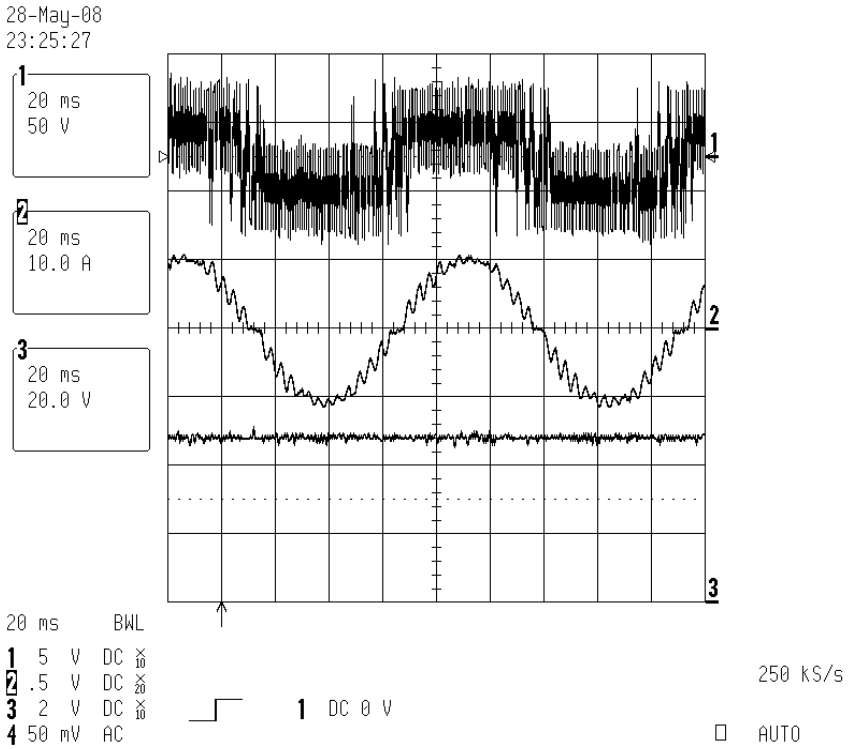


Figure 7-22 Regenerative mode at 280 rpm and under 32 Ω load, 1.6 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

Similarly, Figures 7-23 to 7-31 illustrate the emulated FESS performance while sourcing the DC bus load, Rl = 16 Ω, Idc = 3.2 A. Figures 7-23 and Figure 7-24 illustrate the transients during the connecting and disconnecting of the DC bus load when the PMSM is running at 750 and 600 rpm respectively. Actually, this is the worst disturbance that can be considered for the system. As it is shown in Figure 7-24, the worst case scenario, the DC bus voltage drops 7 V and in less than 2 seconds it builds up and settles at the set point. Also, Figure 7-24 illustrates the over voltage of the DC bus when the load is disconnected from the DC bus. As shown, the DC bus over voltage will be around 7 V and then it reduces to zero in around 3 seconds. Note that this high qualified performance is resulted by implementation of the feed forward (FF) block diagram (Figure 7-1) in the

DC bus voltage-loop controller. Otherwise, the undershoot and overshoot of the DC bus voltage for the same load cycle will be almost four times larger as shown in Figure 7-25.

Regardless of the loading instance, as shown in Figure 7-26, the DC bus voltage stays at the set point, 50 V, for a wide range of speed, 850 rpm – 350 rpm.

As mentioned before, at 850 rpm (Figure 7-27), the peak of the line back-EMF of the PMSM is equal to the DC bus voltage. As a result, there is not enough voltage difference between these two voltages such that it makes the phase current in a sine wave form but as the speed reduces the current wave form becomes more sinusoidal such that at 400 rpm the current wave is purely sinusoidal. Moreover, in Figure 7-26 and Figure 7-30 at around 450 rpm a resonance occurs between the DC bus capacitor and the motor inductors.

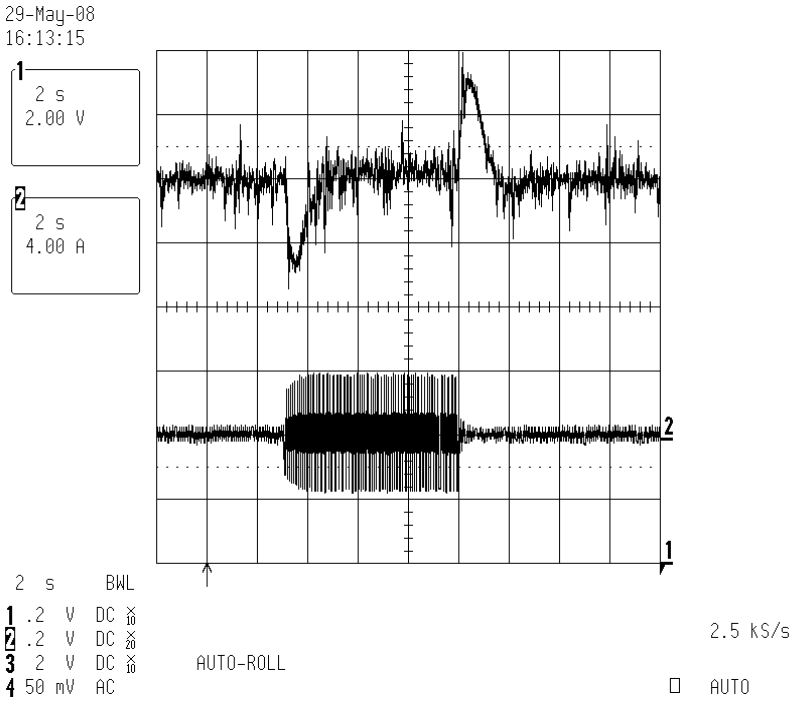


Figure 7-23 Connecting and disconnecting the DC bus load at 750 rpm with the FF controller (Rl = 16 Ω, Idc = 3.2A), Trace 1: DC bus voltage, Trace 2: Phase current.

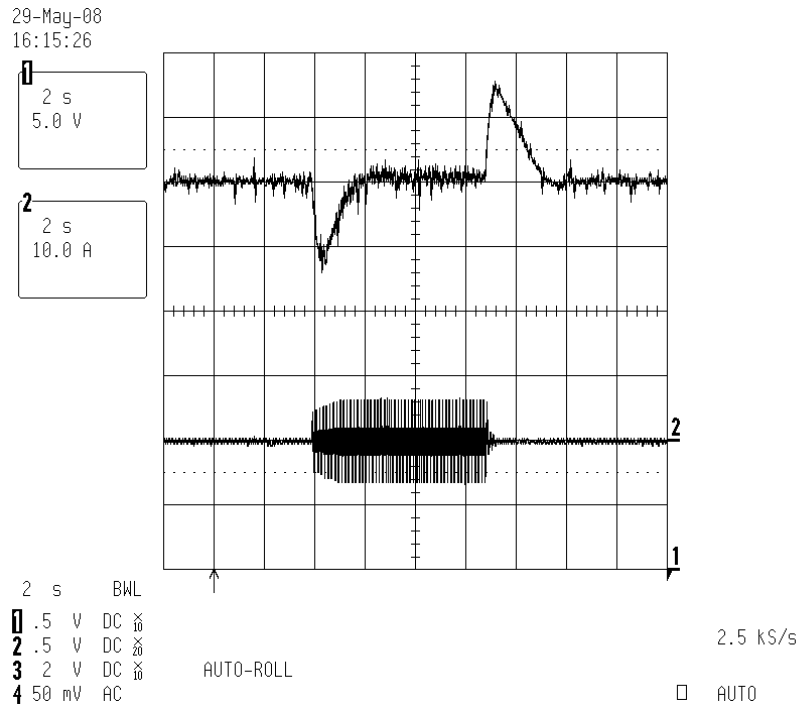


Figure 7-24 Connecting and disconnecting the DC bus load at 600 rpm with the FF controller (Rl = 16 Ω, Idc = 3.2A), Trace 1: DC bus voltage, Trace 2: Phase current.

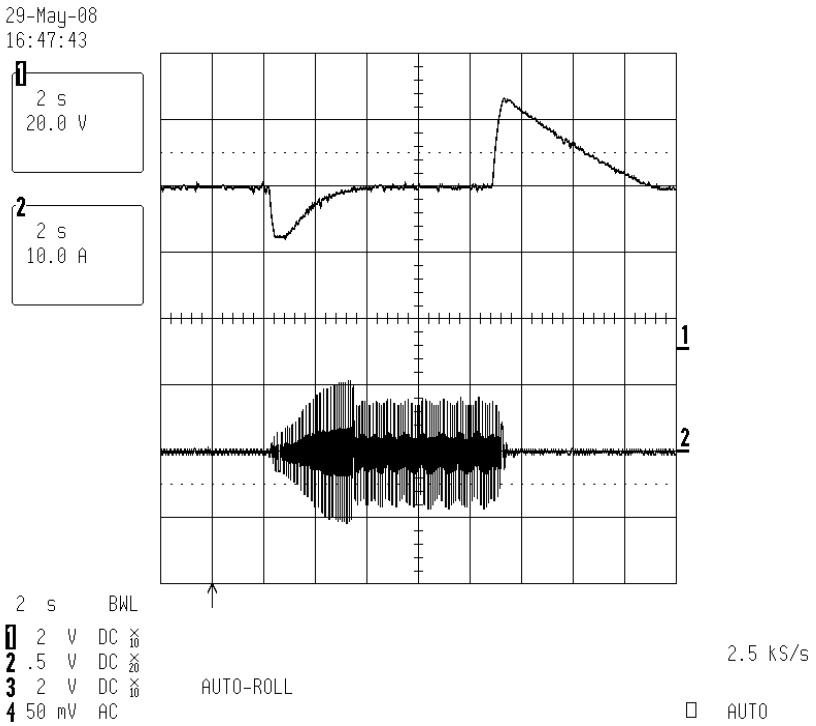


Figure 7-25 Connecting and disconnecting the DC bus load at 600 rpm without the FF controller (Rl = 16 Ω, Idc = 3.2A), Trace 1: DC bus voltage, Trace 2: Phase current.

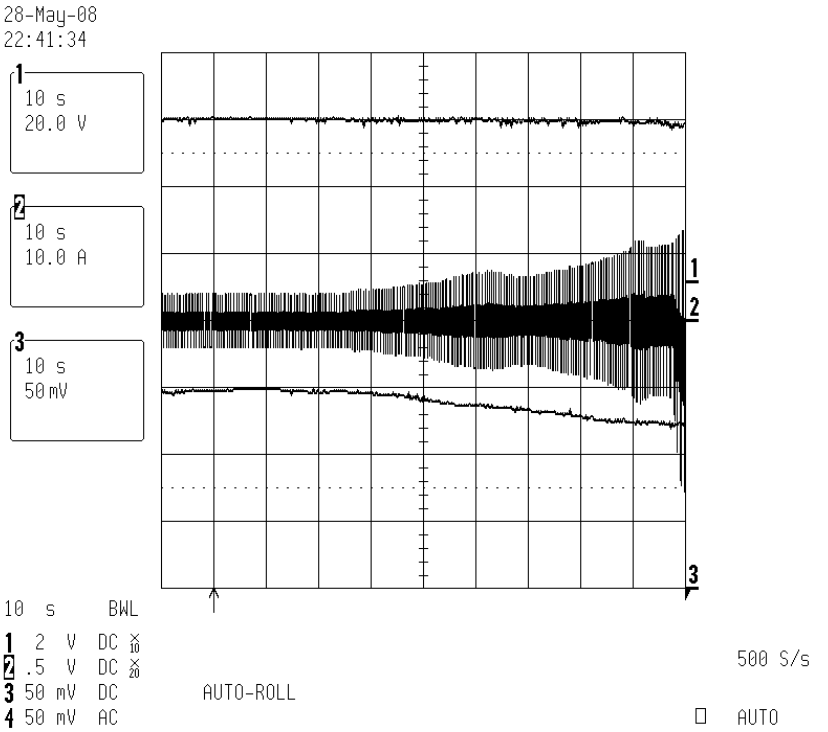


Figure 7-26 Regenerative mode at 830 - 390 rpm and under 16 Ω load, Idc = 3.2 A, Trace 1: DC bus voltage, Trace 2: Phase current, Trace 3: PMSM speed.

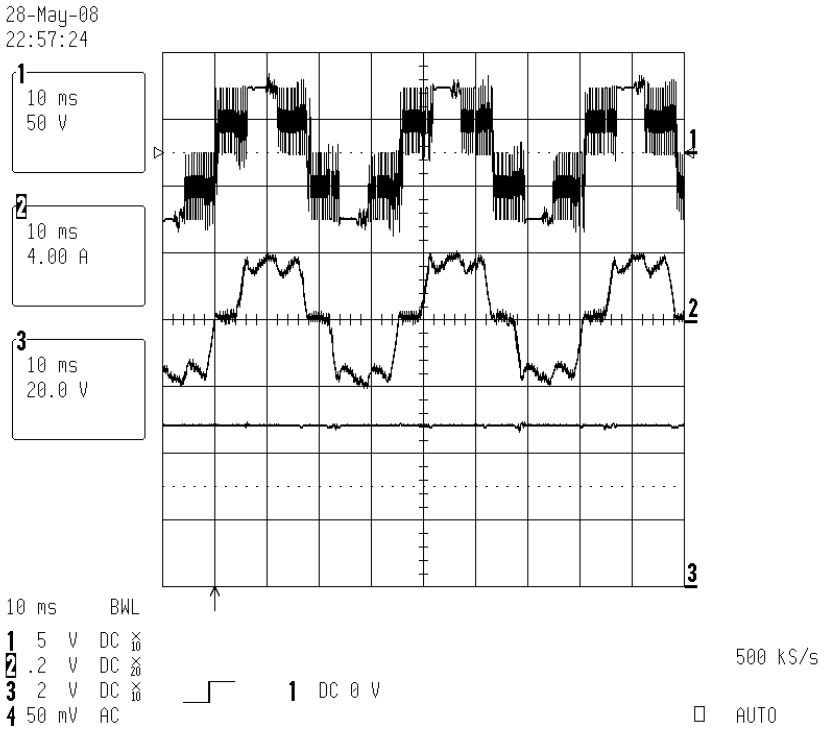


Figure 7-27 Regenerative mode at 850 rpm and under 16 Ω load, 3.2 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

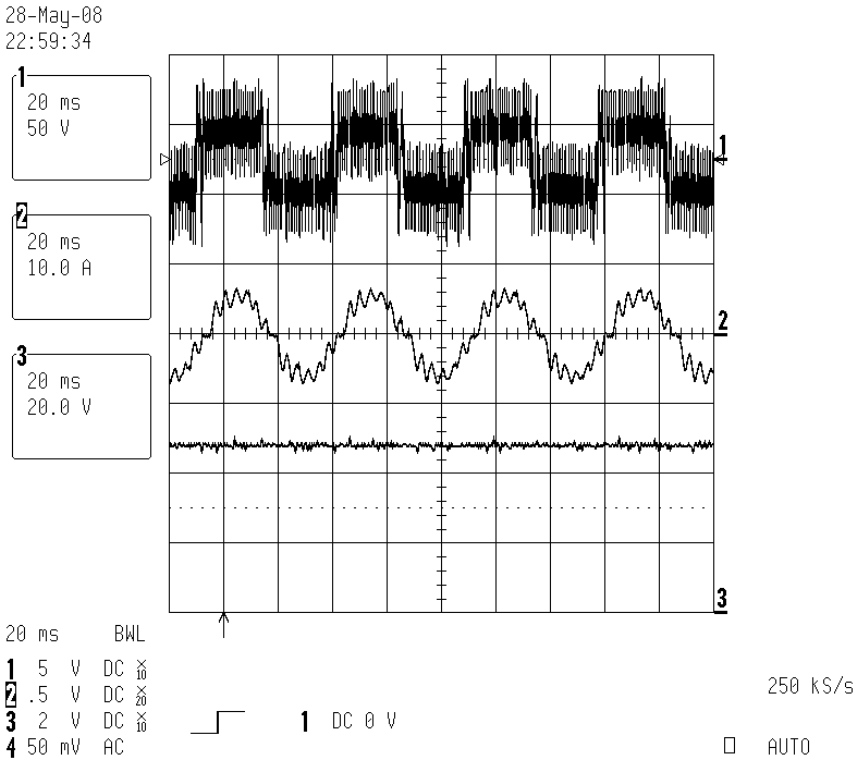


Figure 7-28 Regenerative mode at 600 rpm and under 16 Ω load, 3.2 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

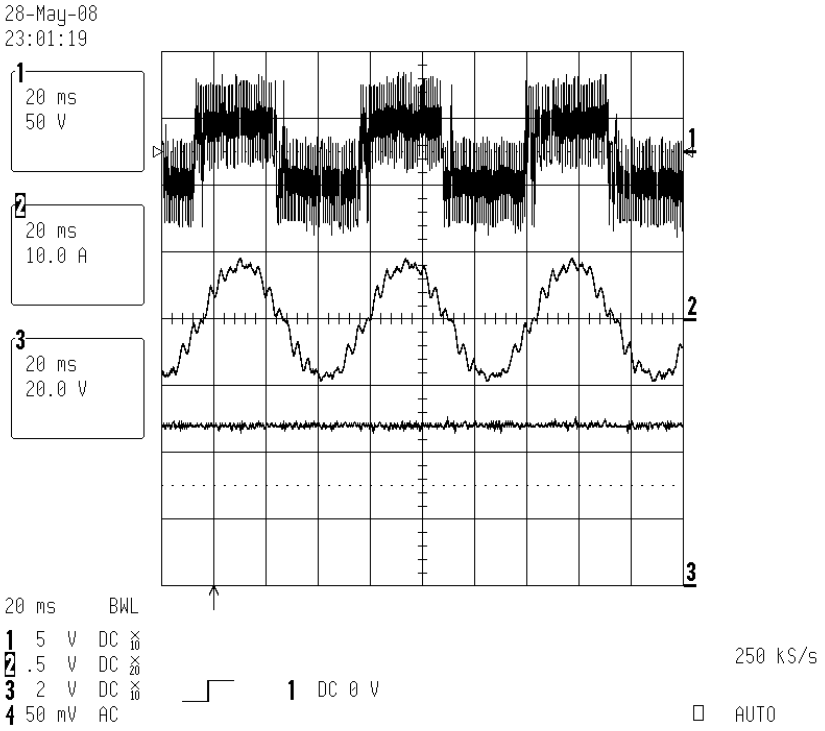


Figure 7-29 Regenerative mode at 470 rpm and under 16 Ω load, 3.2 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

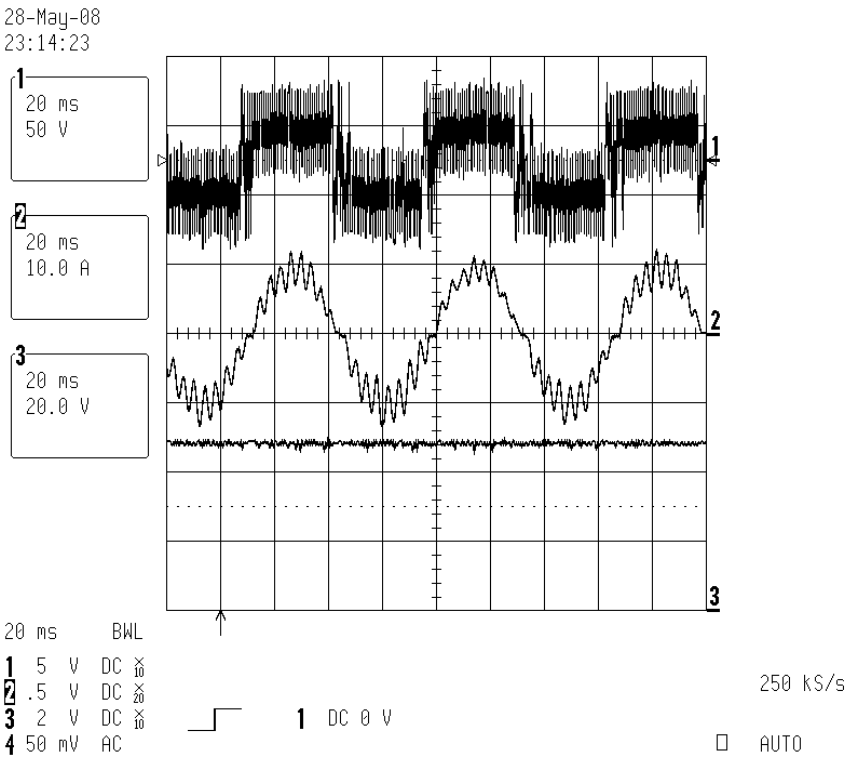


Figure 7-30 Regenerative mode at 450 rpm and under 16 Ω load, 3.2 A, Trace 1: Line-to-line voltage, Trace 2: Phase current, Trace 3: DC bus voltage.

8. CONCLUSIONS AND FUTURE WORK

8.1. Conclusions

Flywheels are now being designed with new advancements in rotating machinery including non-contact magnetic bearings and permanent magnet (PM) motors/generators. New powerful magnet materials and power electronics enable flywheels to effectively fill the niche of short duration, high cycle life applications where batteries and ultra capacitors are not usable.

PM machines offer the most advantages, including higher efficiency and smaller size when compared with other types of motors/generators for the same power rating. They also exhibit lower rotor losses and lower winding inductances, which make them more suitable for a vacuum operating environment and the rapid energy transfer in flywheel applications. In contrast, PM machines have small inductances because of the large air gap resulting in high THD, especially, at low phase currents. This makes an external inductor in series with the machine windings necessary for reducing the THD and reduced thermal losses.

To design the parts and outline the control strategy, a comprehensive analysis of the FESS either in steady state or transient operation is necessary. As a result, establishing a comprehensive analytical model is needed for analysis purposes to avoid time consuming simulations managed by expensive packages, Simulink, PSIM, etc. So far, all the research work performed in this area are focused on software applications [1-4] for analysis purposes and no specific analytical model has been presented.

In Section 2, a comprehensive analytical model of the high-speed FESS in SDQRF has been presented which results in a strong physical intuition to the complete system with good accuracy. The high-speed FESS is modeled such that the nonlinear time varying differential equations of the FESS are transformed to the SDQRF attached to the PMSM rotor. The original system is partitioned into basic sub-circuits modeling in SDQRF, and integrated to achieve the equivalent circuit model of the complete system. The derived model is nonlinear in nature.

In Section 3, the DC and small-signal AC models of the FESS are derived for the purpose of analysis. State space averaging approach is used to derive the DC and small-signal AC models. To develop the DC and small-signal AC equivalent circuits, first the nonlinear sets of differential equations of the nonlinear equivalent circuits of the FESS are developed. Then the set of equations are perturbed and linearized around specific operating points of the FESS operating range. It is shown possible to derive the small-signal AC model at any speed. Since the starting and ending speeds are the most critical operating point in which the mode of operation is changed, these points are of more interest, however, there is no loss of generality throughout the speed range.

The resulted equations contain three types of terms. The DC terms contain no time-varying quantities. The first-order AC terms are linear functions of the AC variations in the circuit, while the second-order and higher AC terms are functions of the products of the AC variations. If the small-signal assumptions are satisfied, the second-order terms and higher orders are much smaller in magnitude than the first-order terms, and hence can be neglected.

As a result, the DC terms configure the DC model and the first-order AC terms forms the small-signal AC equivalent circuits of the high-speed FESS. Then different DC and small-signal AC analysis can be performed on the FESS.

In Section 4, two important factors affecting operation of the machine: power factor and armature reaction i.e. non-zero i_{ds} were investigated in detail. When the PMSM is operating as a generator, its output power is absolutely dependent on leading, unity or lagging power factor at the terminal of the PMSM as well as its torque angle, the angle between the rotor field and stator current phasor. In other words, these items affect the terminal voltage of the machine and the output power.

It is verified that by using a leading power factor one can achieve a higher output power from the machine than with unity or lagging power factors. Moreover, when the phase current increases, the terminal voltage drops significantly under all leading, unity and lagging power factors. The reason for this is that the armature reaction caused by high phase current, similar to the operation of DC machines. Therefore, with a proper control strategy that makes the torque angle equal to 90^o, the armature reaction is completely eliminated. It is verified that vector control with 90^o torque angle achieves both goals resulting in a higher output power.

Then, with these results and the FESS model derived in Section 2, a control algorithm for the FESS has been outlined. The control system includes current, speed and voltage loops all of which use PI controllers. Setting $i_{ds} = 0$ results in linear operation of the q-axis current and speed loop controllers. As a result the linear system theory is applicable for the design of these PI controllers.

In the next step, a novel design algorithm was used to generate the entire set of stabilizing PI controllers for the current- and speed-loops of the FESS. The algorithm was presented step by step for both current and speed loop controllers for the 240 kW, 19-23 krpm FESS.

According to the nonlinearity of the DC bus voltage-loop controller, the algorithm is not applicable to this controller. Therefore, the PI gains were chosen based on pole-zero cancellation concept, however the results show a highly acceptable performance by the DC bus voltage controller.

Finally, the FESS and its control system were modeled in PSIM and were simulated. The simulation results represent a proper performance by the FESS. To verify the accuracy of the model derived in Section 2, a comparison is made between the simulation results achieved by PSIM model and the analytical model.

In Section 5, the simulation results in addition to thermal analysis are used for the selection of the inverter/rectifier devices and the DC bus capacitor bank. In other words, based on the nominal ratings of the FESS, the thermal analysis, the DC bus voltage ripple, and maximum DC bus current ripple the appropriate devices and DC bus capacitor bank are selected and have the inverter/rectifier fabricated by Semikron. The features of the inverter/rectifier is discussed in details in this section.

In Section 6, the design of the external inductor is outlined step by step. Primarily, based on the required ratings and performance of the inductor, core material is first selected then it is designed in a 17-step procedure. Then to model the core losses, fringing effect, saturation effects more accurately and optimize the primary design, the

inductor is redesigned by PExprt, a toolbox developed by Ansoft. Finally, the design is confirmed by FEA performed by Maxwell 2D.

In Section 7, experiments have been performed on an emulated FESS as a proof of the accuracy of the control algorithms and the system performance. The control algorithms are developed on the eZdsp TMS320F2812. The controller of the emulated FESS is served to read the feedback signals, phase a and b currents, DC bus voltage and current and position signals, implement the speed or torque, current and voltage control algorithms and finally generates the gate driver PWM signals by means of space vector PWM modulation technique.

8.2. Future Work

An analytical model for the high-speed FESS was introduced in Section 2. This model was developed based on some assumptions such as ignoring the harmonics of the phase current and ignoring inverter/rectifier losses. So an extension to the work, the inverter/rectifier d-q model can be updated to take the dominant harmonics into account. In addition, a more accurate power device model can be considered in modeling the inverter/rectifier to include the device losses.

In Section 3, the DC and small-signal AC models of the FESS were derived based on similar assumptions mentioned above. As an extension to the work, the small signal model of the devices can be considered in the small-signal AC model of the FESS, in order to predict the FESS performance more precisely in transients. Moreover, small-signal analysis can be implemented to the model and multivariable control algorithms can be evaluated in detail.

In Section 4, the FESS with its control system were modeled and simulated in PSIM. Another potential work for future is to model the PMSM and the PWM inverter/rectifier in addition to the external inductor and the DC link with SIMPLORER toolbox (Ansoft package) in which the machine and the converter can be modeled more accurately. Moreover, instead of using PI controllers, it is recommended to implement the well-known non-linear control strategies to the system and be compared with the implemented controllers.

In Section 5, the thermal analysis of the selected device was performed by Semisel, a toolbox developed by Semikron. This toolbox doesn't take the device current harmonics into account. Since in the charging mode, the phase current is rich in harmonics, it is an interesting extension to the work to do a comprehensive thermal analysis in Maxwell. In addition, a mechanical stress analysis on the DC bus will be another area to work on to make sure the mechanical feature of the inverter is strong enough to resist against the electromagnetic forces applied to the buses during the discharging mode.

In Section 6, the need for an external inductor is outlined and the design procedure has been explained step by step. However, using the external saturable inductor can be an effective way to reduce the THD, though it is an expensive method and also is bulky. So exploring another solution to the problem resulting in removing this part of the system is in demand. It might be possible to develop an optimal PWM modulation technique to improve the THD amount during the charging mode. So as another extension to the work, research on the PWM technique can be an interesting future work.

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