DESIGN OF MULTI-CHANNEL RADIO-FREQUENCY FRONT-END FOR 200MHZ PARALLEL MAGNETIC RESONANCE IMAGING

A Dissertation

by

XIAOQUN LIU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2008

Major Subject: Electrical Engineering

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Approved by:

Co-Chairs of Committee,	Takis Zourntos
	Steven M. Wright
Committee Members,	Jim Ji
	Mary P. McDougall
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ABSTRACT

Design of Multi-Channel Radio-Frequency Front-End for 200MHz Parallel Magnetic Resonance Imaging. (December 2008)

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Co-Chairs of Advisory Committee: Dr. Takis Zourntos
Dr. Steven M. Wright

The increasing demands for improving magnetic resonance imaging (MRI) quality, especially reducing the imaging time have been driving the channel number of parallel magnetic resonance imaging (Parallel MRI) to increase. When the channel number increases to 64 or even 128, the traditional method of stacking the same number of radio-frequency (RF) receivers with very low level of integration becomes expensive and cumbersome. However, the cost, size, power consumption of the Parallel MRI receivers can be dramatically reduced by designing a whole receiver front-end even multiple receiver front-ends on a single chip using CMOS technology, and multiplexing the output signal of each receiver front-end into one channel so that as much hardware resource can be shared by as many channels as possible, especially the digitizer.

The main object of this research is focused on the analysis and design of fully integrated multi-channel RF receiver and multiplexing technology. First, different architectures of RF receiver and different multiplexing method are analyzed. After comparing the advantages and the disadvantages of these architectures, an architecture of receiver front-end which is most suitable for fully on-chip multi-channel design is

proposed and a multiplexing method is selected. According to this proposed architecture, a four-channel receiver front-end was designed and fabricated using TSMC 0.18μm technology on a single chip and methods of testing in the MRI system using parallel planar coil array and phase coil array respectively as target coils were presented. Each channel of the receiver front-end includes an ultra low noise amplifier (LNA), a quadrature image rejection down-converter, a buffer, and a low-pass filter (LPF) which also acts as a variable gain amplifier (VGA). The quadrature image rejection down-converter consists of a quadrature generator, a passive mixer with a transimpedance amplifier which converts the output current signal of the passive mixer into voltage signal while acts as a LPF, and a polyphase filter after the TIA. The receiver has an over NF of 0.935dB, variable gain from about 80dB to 90dB, power consumption of 30.8mW, and chip area of $6mm^2$.

Next, a prototype of 4-channel RF receiver with Time Domain Multiplexing (TDM) on a single printed circuit board (PCB) was designed and bench-tested. Then Parallel MRI experiment was carried out and images were acquired using this prototype. The testing results verify the proposed concepts.

ACKNOWLEDGEMENTS

My journey of pursuing knowledge has been a long road filled with obstacles. These obstacles can not be conquered and my goal in each stage can not be turned into reality without the contributions of many people. Although it is so difficult, even impossible to reward them as much, I do acknowledge so many people who I learned from, who aided me in my work, and who I shared my happiness and sadness with from the beginning, especially during these years at Texas A&M University.

First, I would like to express my sincere gratitude to my advisor, Dr. Takis Zourntos, for his guidance, support and constant encouragement all these years. His open thought as a pioneering explorer led me omit from the research field of pure analog circuit design to MRI, seeking the applications of analog circuit design from communications to biomedical. His encouragement, support, trust, and his guidance gave me great confidence and inspiration in my research. His supervision and guidance all these years in my study in Texas A&M University has been invaluable.

I would like to express my special thanks to my co-advisor, Dr. Steven M. Wright for his invaluable help, instruction and guidance. His wealth of knowledge and insight in research have not only showed me the art of the wonderful NMR/MRI world, but also assisted and guided me effectively in exploring my research in this field. I am grateful to him and respect him not only for his pioneering expertise as an advisor, but also as a great human being. His great attitude toward research and his great personality have become the model of me and other students.

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NOMENCLATURE

ADC	Analog to Digital Converter
BPF	Band Pass Filter
CG LNA	Common Gate Low Noise Amplifier
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CS LNA	Common Source Low Noise Amplifier
DSP	Digital Signal Processing
FDM	Frequency Domain Multiplexing
FID	Free Induction Decay
FOV	Field of View
GBW	Gain-Bandwidth
GUI	Graph User Interface
IC	Integrated Circuit
IF	Intermediate Frequency
IM_3	Third Order Inter-Modulation
IRF	Image Rejection Filter
IRR	Image Rejection Ratio
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCD	Liquid Crystal Display

LHP	Left Hand Plane
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LO	Local Oscillator
MESFET	Metal Semiconductor FET
MRI	Magnetic Resonance Imaging
MSL	Micro Strip (Transmission) Line
Opamp	Operational Amplifier
P_{1dB}	1dB Compression Point
Parallel MRI	Parallel Magnetic Resonance Imaging
PCB	Printed Circuit Board
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Signal to Distortion Ratio
SEA	Single Echo Acquisition
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SMT	Surface Mount Technology
TDM	Time Domain Multiplexing
TIA	Transimpedance Amplifier
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company

TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier

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CHAPTER I

INTRODUCTION

After first proposed and developed during early 1970s, magnetic resonance imaging (MRI) technique was dramatically developed and MRI equipments were built in experiment labs as well as in hospitals as a non-invasive tomographic imaging technique while suffering the disadvantages as the most expensive and slowest imaging method [1]-[3]. In the past decade, there have been considerable interests in parallel magnetic resonance imaging (Parallel MRI) to allow for simultaneous analysis of multiple biological samples, to improve other valuable factors, such as enlarging the field-of-view (FOV), increasing signal-to-noise ratio (SNR), and especially to facilitate faster image acquisition [4]-[7]. For example, a 64-channel coil array on a printed circuit board (PCB) was designed, constructed and successfully used by McDougall and Wright to test the method of single echo acquisition (SEA) imaging in which an independent image was acquired with only one echo by entirely replacing the phase encoding steps with the spatial information obtained from the coil array [3], [8], [9]. As another example, in order to increase the image SNR, a 23-channel and a 90-channel receive only phase array of small surface coils, which were arranged over the dome of head in a continuous array, were built by Wiggins and Wald et al. [6]. These phase array coils allow for significant imaging time and SNR improvement over conventional coils [6].

This dissertation follows the style of *IEEE Journal of Solid State Circuits*.

Parallel MRI demands the signals from each coil be acquired, pre-processed and digitized simultaneously. The most cost-effective approach to satisfy this requirement for parallel MRI is updating the existing conventional single-channel MRI equipment to its multi-channel counterpart by designing a multi-channel receiver, instead of designing and building a totally new set of parallel MRI equipment because of the prohibitively high-cost a new one introduces.

The most direct multi-channel receiver design simply duplicates a single channel receiver chain as many times as needed for the parallel MRI experiment [10]. However, this approach of simple duplication is expensive and cumbersome [5] because conventionally each receiver chain is built from integrated circuits (ICs) with low level of integration and other necessary discrete components, and these ICs and components increase to a large number after duplication, especially for experiment up to 128 channels. Moreover, each channel needs a single cable connecting the coil in the main magnet and the receiver front-end out of the main magnet, and still another cable is needed to connect the output of the front-end and the digitizer. The large number of cables continues to make the receiver more bulky. This high-cost and cumbersomeness make the receiver to be bottle-neck of parallel MRI experiment and limit its application in research labs and hospitals. Therefore, much recent effort has been devoted to seeking an effective approach to reduce the complexity and cost of the receiver. In this work, the limitation of reducing the size and cost of the multi-channel receiver has been explored by on-chip CMOS circuit design and multiplexing technique.

1.1 On-Chip Circuit Design of MRI Receivers Using CMOS Technology

As mentioned above, most of the existing MRI receivers were designed and assembled with very low level of integration making the receivers of Parallel MRI system expensive and cumbersome. On-chip circuit design becomes a most effective solution with additional advantages [11]. T. L. Peck et al. designed an integrated gallium arsenide metal semiconductor FET (MESFET) on the same substrate with a micro coil [11]-[14]. Although this design is a successful try of on-chip circuit design of MRI receiver, it is still in low level of integration because there is only one channel on a single chip and only the preamplifier stage was designed on the chip. Advances in low-cost CMOS technology inspire a solution that dramatically reduces the cost and complexity while providing outstanding imaging quality by using CMOS IC design. The key points of this design are low noise and high integration. In order to acquire low noise, first, the topology of LNA is explored and designed with high gain and ultra low noise figure. Second, a filter has to be designed before the down-converter in order to attenuate to thermal noise at image frequency. Otherwise, a threshold of 3dB exists for the noise figure of the receiver because of the thermal noise folding from the image frequency at the down-converter. In order to acquire high integration, the out-of-chip components such as surface acoustic wave (SAW) filter or crystal filter before the down-converter is avoided by introducing an image reject quadrature down-converter satisfying not only image noise rejection but also fully on-chip circuit design.

For demonstration purposes, a four-channel front-end was on-chip designed by the author using TSMC CMOS 0.18μm technology. This CMOS IC design is a small

"chip" about the size of a finger nail after packaged and costs on the order of ten dollars with large volume production. The "chip" is even smaller about the size of a surface mounted technology (SMT) 0805-resistor if it is not packaged, and is small enough to be mounted on the same PCB of the coil array, and therefore the large bunch of cables originally connecting the coils and the receivers are avoided. This makes the multi-channel receiver more economic and compact, moreover, the signal power lose of the MR signal along each of these cables is reduced and therefore the SNR at the output of each channel of receiver is increased as much as the reduced signal power loss.

The signals at the output of the multi-channel front-end can be multiplexed using a RF switch controlled by a time clock signal to realize the solution of time domain multiplexing (TDM).

1.2 Time Domain Multiplexing

TDM technique for MRI application was first proposed and prototypes were designed and proved to be a cost-effective multi-channel solution by Wright et al. using a RF multiplexing switch [4], [5], [15], [16]. Using the RF switch, the MR signal from each signal source was sampled in respective time-slot, and sent to a single receiver of the existing conventional MRI system for amplification, down-conversion, filtering and digitization. In this approach, the bandwidth and components of a single receiver is effectively used by multiple channels, so that the number of the components and the cables between the front-ends and the digitizer are largely reduced, and therefore the receiver is more compact and cost-effective. The TDM method proposed has its

limitation. The bandwidth of the receiver is required to be *N* times that of the single channel. That is, at least *N* times Nyquist frequency of the down-converted MR signals, or in another word, the bandwidth of the MRI pulse sequence is required, where *N* is the number of the channels. Therefore, under the limitation of the bandwidth of the receiver of the existing conventional MRI system, the multiplexed channels are limited to a low number because of crosstalk. In the work of this dissertation, the TDM method is modified in order to eliminate the bandwidth limitation of the RF receiver by moving the RF switch to after the down-converter and the low-pass filter, right before the digitizer. Therefore the limitation of the bandwidth of the receiver is eliminated. After being multiplexed, the MR signals are sent to the digitizer for digitization. After the digitized MR signals are acquired, digital signal processing (DSP) technology is applied for separating the multiplexed signals and down-converting each channel of the MR signal to base-band. Finally, images are recovered from these base-band digitized MR signals.

1.3 Research Goals

This research addresses the issues regarding the multi-channel receiver front-end integrated in CMOS technology for parallel MRI. The CMOS circuit design of each block of the receiver front-end, including the LNA, mixer, low-pass filter (LPF), and variable gain amplifier (VGA), is also analyzed and illustrated. Moreover, the multiplexing approaches of TDM and FDM, as well as various trade-offs of them are investigated. For demonstration purposes, as mentioned above, an experimental prototype of four-channel RF front-end based on the proposed concept was designed

using TSMC CMOS 0.18μm technology to meet the 200MHz parallel MRI experiment. Moreover, also for demonstration purposes and verification, based on the analysis of this research, another experimental prototype of four-channel RF front-end together with a TDM circuit using commercial ICs and other necessary discrete components were designed in a single PCB and tested. Both prototype designs are frequency "universal", that is, suitable to a large range of MR signal frequency with only changing the local oscillator (LO) frequency provided.

The research goals and key contributions of this research are:

1. Analysis of CMOS RF front-end architectures for MRI: Superheterodyne, Direct Conversion, and Low-IF architectures. And finally, proposing an architecture that is suitable for fully integration for MRI applications.
2. Investigation of TDM and FDM.
3. The first CMOS multi-channel RF front-end design which dramatically decreases the cost and physical size of the multi-channel receiver.
4. The first house-made multi-channel RF front-end design with TDM technique.
5. Exploring the feasibility of the novel idea of "Digital Coil Array".
6. Low noise and high linearity circuit design of wide-band RF front-end which is also valuable for other wide-band application besides MRI.
7. Exploring the signal cross-talk and leakage among channels for multi-channel design on a single silicon substrate and on a single PCB.

8 Starting a new research field to explore the limitation of reducing the size, cost, and power consumption of receivers for parallel MRI.

1.4 Dissertation Organization

Chapter II reviews the existing RF receiver architectures and multiplexing methods. In order to achieve fully integrated design of multi-channel, a receiver front-end architecture is proposed in this chapter. Also a setup of multi-channel front-end with TDM is proposed.

Chapter III addresses the analysis and design of each building block of the fully integrated four-channel receiver front-end using CMOS TSMC 0.18μm. The front-end was designed to achieve ultra low noise figure, low power and high gain.

Chapter IV proposes architecture to setup 64-channel RF receiver front-end with TDM using parallel planar coil array in SEA as target coils, and analyzes the performance improvement of this architecture on MRI. Architecture using phase coil array as target coils is also proposed in order to prove the universality of the application of the multi-channel front-end with TDM on parallel MRI.

Chapter V addresses the design of a prototype of the first house-made multi-channel front-end with TDM on a single PCB in the MRI society. Bench-testing and MRI experiment results of this prototype are also addressed.

In Chapter VI, future work and conclusions are presented.

CHAPTER II

RECEIVER FRONT-END ARCHITECTURE AND MULTIPLEXING METHOD

2.1 Receiver Front-End Architecture

Although the MR signal from the output of the RF coil is theoretically possible to be digitized directly by analog to digital converter (ADC), due to the sampling frequency limitation and the trade-off between the sampling frequency and SNR of ADC, also due to the consideration of the data volume of the digitized MR signal and the computer resources to process this large volume of data if the MR signal is digitized at RF frequency, the MR signal has to be down-converted before digitization. When using down-conversion mixer, a LNA with enough gain is necessary to be placed before the mixer in order to overcome the noise of the mixer and the subsequent stages [17]. The LNA also has to be as low noise as possible in order to reduce the noise it introduces to the signal because no amplifier stage exists before the LNA and therefore the noise of the LNA is not suppressed. Moreover, filters are still needed before the mixer for thermal noise attenuation and signal selection if other signals exist at frequency nearby. After the mixer, low-pass filter is still necessary to attenuate the signal produced by the mixer at high frequency, and other gain stages are also needed to provide a proper signal power level for the input of the ADC. In conclusion, a RF/analog signal processing front-end is necessary before the ADC. Various RF front-end architectures exist [18]-[23]. The most common architecture is superheterodyne.

2.1.1 Superheterodyne

The superheterodyne architecture was first proposed by E. H. Armstrong in 1917 [17] as shown in Figure 2.1, and has been widely used in wireless communications, enjoying excellent sensitivity and selectivity [24]. In wireless communications applications, depending on different standard, the signal spectrum from the output of the antenna contains the signal band, which consists of a certain number of channels with certain bandwidth of each and certain channel spacing between the adjacent channels, and signals from other standards at frequencies out of the signal band (Out-of-band signals).

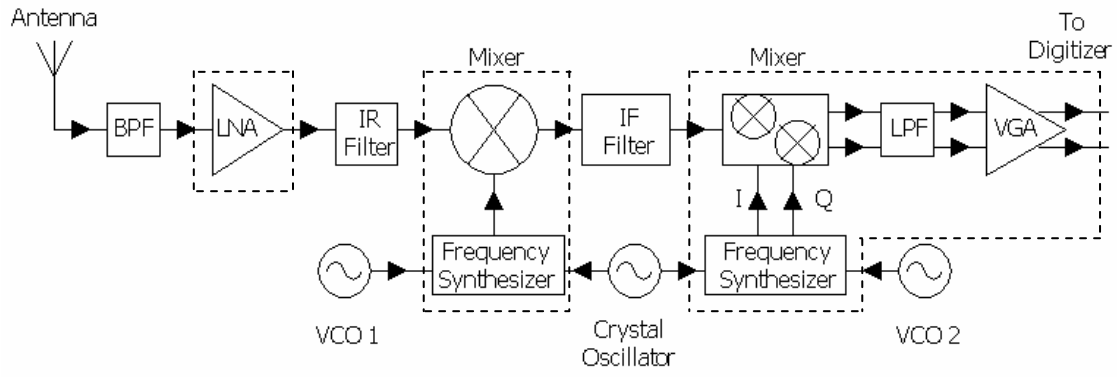


Figure 2.1 Superheterodyne Architecture
(The blocks within the dashed line area are on-chip)

In this architecture, the band-pass filter (BPF), also called the band-selection filter, attenuates the out-of-band signals, and then the selected signal band is amplified by a LNA, which introduces as little noise as possible and provides enough gain to suppress the noise of the subsequent stages. A band-pass image rejection filter (IRF)

after the LNA and before the mixer is used in order to attenuate the signal at the image frequency. The first mixer down-converts the RF signal to a certain intermediate frequency (IF), and the desired channel is selected by the band-pass IF filter, which is also called channel-selection filer. The IF is necessary to be high enough to relax the Q of the BPF and IRF. However, if the IF is too high, the Q of the IF filter has to be increased in order to effectively attenuate the out-of-channel signals. Therefore, a trade-off exists between the Q of IF filter and that of BPF and IRF. The selected desired channel, which is a complex signal in most cases, is then down-converted to base-band with real (Q) part and imaginary (I) part by a quadrature mixer. Next the base-band I, Q signals go through a LPF to further reject the out-of-channel signals. Now the signal is ready to be amplified by a VGA to proper value of amplitude for the input of the ADC.

Although the superheterodyne architecture enjoys excellent signal to noise and distortion ratio (SNDR), and acquires excellent SNR, this architecture suffers the following disadvantages:

1. The BPF, IRF and IF filter have to be out-of-chip because the Q of which is too high to be implemented in conventional CMOS technology [25].
2. The voltage controlled oscillator (VCO) has to be off-chip because of the low Q of the on-chip inductor [24].
3. This architecture is complicated and comprises many stages to be designed on-chip [25].
4. The BPF, IRF and IF filter are passive and therefore reduce the signal power, and in turn degrade the SNR, especially the BPF before the LNA [25].

In the application of MRI, the MR signal is a very clean signal containing only a single signal band at Larmor frequency, and only thermal noise exists out of the Larmor frequency. Therefore, the BPF and the IRF can be removed because no large out of band signal is needed to be attenuated. Since no Q of the BPF and IRF is needed to be relaxed by the IF, the first stage of the down-conversion together with the IF filter can also be removed if the thermal noise at the image frequency is not considered. After removing all these stages, we can find that this architecture turns in to a direct conversion receiver.

Note that the thermal noise at the image frequency has to be suppressed in order to reduce the noise figure of the receiver front-end to be smaller than 3dB. This issue is being discussed later in this chapter.

2.1.2 Direct Conversion

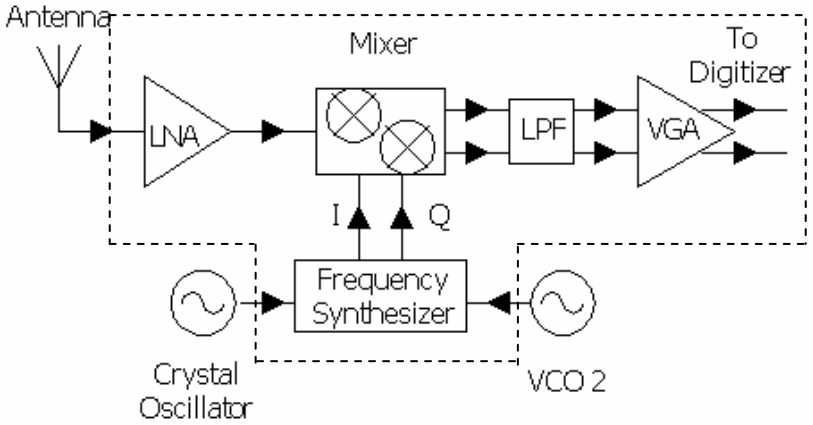


Figure 2.2 Direct Conversion Architecture
(The blocks within the dashed line area are on-chip)

Direct conversion architecture, as illustrated in Figure 2.2, has an advantage of simplicity and enjoys fully integration [25], however, this architecture also suffer the following disadvantages:

1. First and foremost, a small amount of energy at LO frequency radiates from the LO input port of the mixer and is received by the antenna, and/or leaks through the silicon substrate to the input of the LNA. These amount of energy at LO frequency are amplified by the LNA, and then "self-mixed" to the base-band in the mixer, causing a DC offset problem [17].
2. The leakage of the RF signal to the LO input port of the mixer is "self-mixed" with the RF signal, and also introduces DC offset problem [17].
3. Harmonics of RF and LO signals also have the same effect [25].
4. Flicker noise is large at low frequencies especially at base-band.

In order to overcome these problems, a low-IF architecture is used in this design.

2.1.3 Low-IF

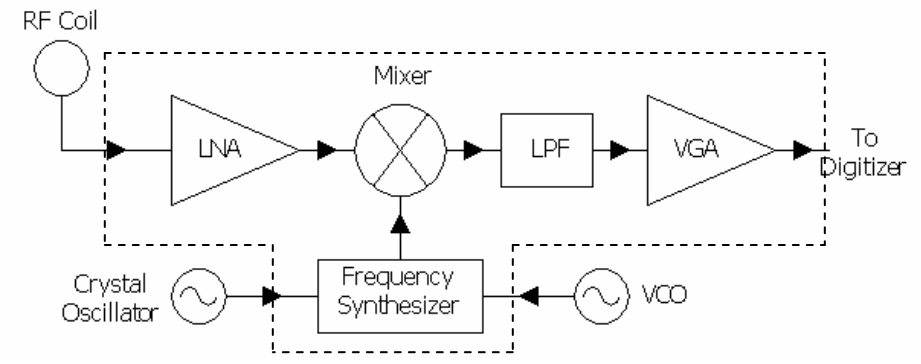


Figure 2.3 Low-IF Architecture
(The blocks within the dashed line area are on-chip)

As illustrated in Figure 2.3, the signal from the output of the RF coil is down-converted to a low IF frequency, which is chosen to be low enough to accommodate the sampling frequency limitation of the ADC. On the other hand, this IF has to be high enough to avoid the large flicker noise. Normally, the IF is chosen to be a little larger than the noise corner frequency which is about 500 kHz to 1 MHz in CMOS technology [25].

Since the RF signal is not down-converted to DC, this architecture is free from the DC offset problem, as well as flicker noise as mentioned above.

The Low-IF architecture increases the requirement of the ADC, however, with the advances of the CMOS and the effort of the talented CMOS analog designers, nowadays, a 16-bit ADC is not difficult to be designed with sampling frequency up to 20MHz.

However, although there is not large signal power at the image frequency, if the IRF is removed as shown in Figure 2.3, the thermal noise at the image frequency is folded to the down-converted signal at IF by the down-converter as illustrated in Figure 2.4. The noise folding decreases the SNR of the MR signal by 3dB, that is, increase the noise figure of the receiver front-end by 3dB [25]. Therefore, a threshold of 3dB is set for the noise figure of the receiver front-end. In order for reducing the noise figure of the front-end to lower than 3dB, it is necessary to place an IRF before the down-converter. Normally, a surface acoustic wave (SAW) filter or a crystal filter is used as the IRF to satisfy the requirement of high Q of the IRF. However, the SAW filter or crystal filter is passive and out-of-chip. In order for fully on-chip design, one solution is using CMOS

active filter to replace the SAW or crystal filter. However, in order to acquire the necessary high Q for the IRF, the CMOS active filter has to be very high order and be a very large circuit and therefore not only increases the complication of the receiver design but also introduces much thermal noise.

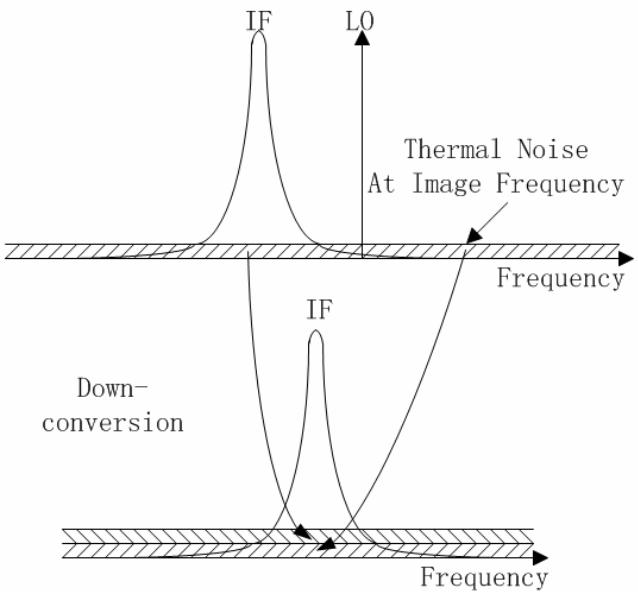


Figure 2.4 Thermal Noise Folding

A solution to this problem is using a quadrature generator for the LO signal and a polyphase filter after the down-converter [26]-[30].

2.1.4 Proposed Architecture of RF Receiver Front-End

As discussed above, the Low-IF architecture is updated by using a quadrature generator for the LO signal and a polyphase filter after the mixer [26]-[30] in order to avoid noise folding and satisfy fully on-chip design.

As shown in Figure 2.5, the MR signal from the MRI coil is amplified by the LNA and the pre-amp of the passive mixer in order to compensate the loss and suppress the noise of the passive mixer. Note that if the gain of the LNA is large enough, the pre-amp of the passive mixer can be ignored. After being amplified, the MR signal is sent to the mixer, which is a passive mixer in order for reducing the flicker noise, and mixed with the quadrature LO signals from the LO quadrature generator. After the down-converter, transimpedance amplifier (TIA) and the polyphase filter, the MR signal is down-converted to an intermediate frequency, and the thermal noise at the image frequency is attenuated. This down-converted MR signal still needs to be sent to a LPF in order to filter out the signal at the frequency of ω_{LO+RF} generated at the mixer. Finally, after amplified by the variable gain amplifier to a proper value of amplitude, the MR signal is sent to the RF switch for multiplexing.

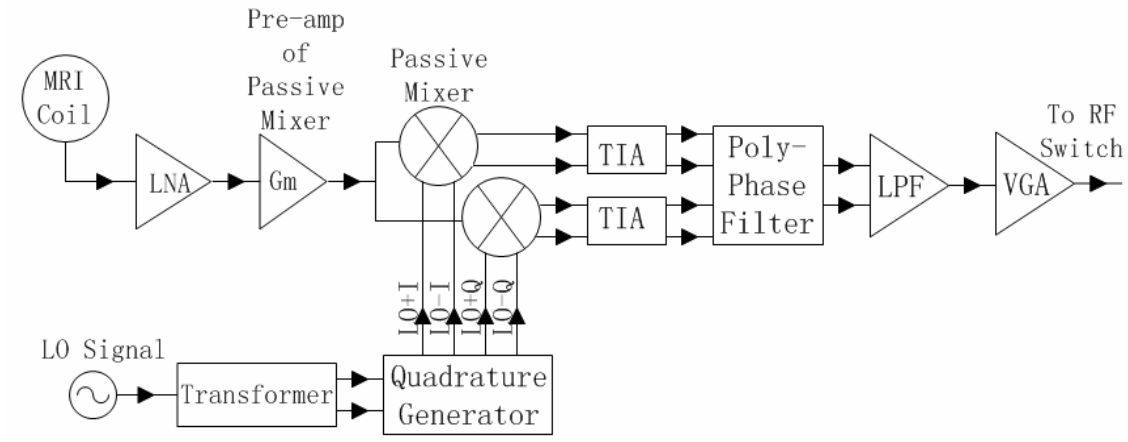


Figure 2.5 Proposed RF Receiver Front-End Architecture

The key points of image rejection in this architecture are the quadrature generator and the polyphase filter. First, the LO signal from the frequency synthesizer is transformed from single-ended to differential-ended by a transformer. Then the differential-ended LO signal is sent to the quadrature generator illustrated in Figure 2.6 [26] according to the Kirchhoff's Voltage Law (KVL) and Superposition Principle, where $R_Q = \frac{1}{\omega_{LO} C_Q}$. Then the quadrature LO signals are sent to the quadrature mixer shown as Figure 2.7.

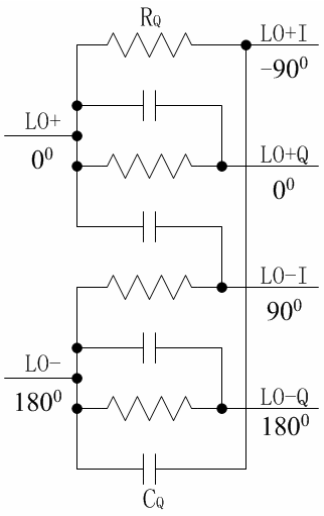


Figure 2.6 Quadrature Generator

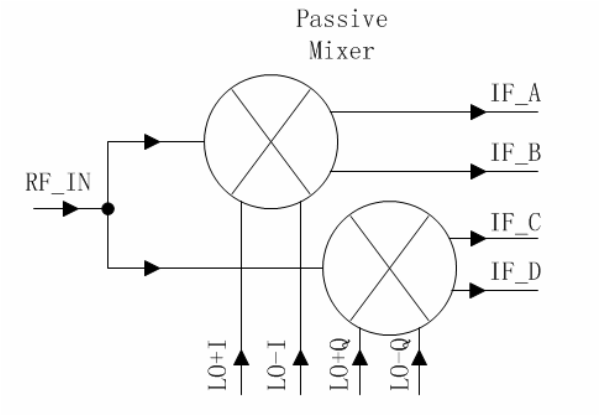


Figure 2.7 Quadrature Mixer

In order to analyze how the thermal noise at the image frequency is rejected, we can assume the input signal in Figure 2.7 is

$$S_{in}(t) = A_{RF}\cos\omega_{RF}t + A_{IM}\cos\omega_{IM}t \qquad 2.1$$

where $\omega_{RF} - \omega_{LO} = \omega_{LO} - \omega_{IM} > 0$

According to the relative phase shifts of the quadrature LO signals between each other, we can get

$$LO + I = \sin\omega_{LO}t \qquad 2.2$$

$$LO - I = \sin(\omega_{LO}t + 180^0) \qquad 2.3$$

$$LO + Q = \sin(\omega_{LO}t + 90^0) \qquad 2.4$$

$$LO - Q = \sin(\omega_{LO}t + 270^0) \qquad 2.5$$

Note that in order for simplicity, the amplitudes of the LO signals are neglecting. Then the RF input signal mixers with the LO signals respectively, and we can get the following results neglecting the high frequency components which are filtered by the LPF.

$$IF\_A = \frac{A_{RF}}{2}\cos(\omega_{IF}t + 90^0) + \frac{A_{IM}}{2}\cos(\omega_{IF}t) \quad 2.6$$

$$IF\_B = \frac{A_{RF}}{2}\cos(\omega_{IF}t - 90^0) + \frac{A_{IM}}{2}\cos(\omega_{IF}t + 180^0) \quad 2.7$$

$$IF\_C = \frac{A_{RF}}{2}\cos(\omega_{IF}t + 0^0) + \frac{A_{IM}}{2}\cos(\omega_{IF}t + 90^0) \quad 2.8$$

$$IF\_D = \frac{A_{RF}}{2}\cos(\omega_{IF}t + 180^0) + \frac{A_{IM}}{2}\cos(\omega_{IF}t + 270^0) \quad 2.9$$

In order for simplicity, equations (2.6)-(2.8) are rewritten as the following

$$IF\_A = \frac{A_{RF}}{2}\angle 90^0 + \frac{A_{IM}}{2}\angle 0^0 \quad 2.10$$

$$IF\_B = \frac{A_{RF}}{2}\angle -90^0 + \frac{A_{IM}}{2}\angle 180^0 \quad 2.11$$

$$IF\_C = \frac{A_{RF}}{2}\angle 0^0 + \frac{A_{IM}}{2}\cos\angle 90^0 \quad 2.12$$

$$IF\_D = \frac{A_{RF}}{2}\angle 180^0 + \frac{A_{IM}}{2}\angle 270^0 \quad 2.13$$

Next, the down-converted MR signals are sent to TIA, which is an opamp connected in negative feedback with a pair of shunt resistor and capacitor. The TIA transfers the IF signal from current to voltage, as shown in Figure 2.8.

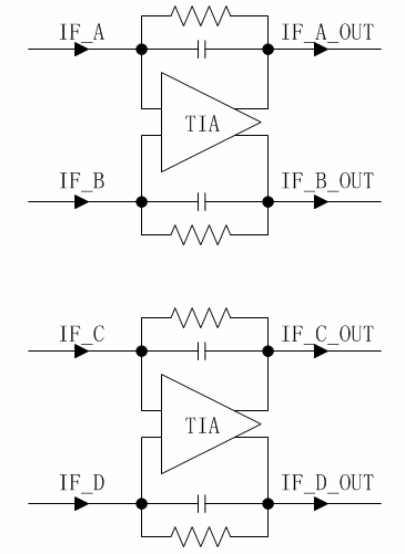


Figure 2.8 Transimpedance Amplifier

Since the TIAs are connected in negative feedback, each output IF signal of the TIA has a 180^0 phase shift, therefore, we can get the IF signals at the TIA outputs

$$IF\_A\_OUT = \frac{A_{RF}}{2}\angle 270^0 + \frac{A_{IM}}{2}\angle 180^0 \quad 2.14$$

$$IF\_B\_OUT = \frac{A_{RF}}{2}\angle 90^0 + \frac{A_{IM}}{2}\angle 0^0 \quad 2.15$$

$$IF\_C\_OUT = \frac{A_{RF}}{2}\angle 180^0 + \frac{A_{IM}}{2}\cos\angle 270^0 \quad 2.16$$

$$IF\_D\_OUT = \frac{A_{RF}}{2}\angle 0^0 + \frac{A_{IM}}{2}\angle 90^0 \quad 2.17$$

Then the IF signals at the TIA outputs are sent to the polyphase filter. As illustrated in Figure 2.9, according to the Kirchhoff's Voltage Law (KVL) and Superposition Principle, if the quadrature IF signals are connected in clockwise, we can get the output signals as shown in the left side of Figure 2.9. If the quadrature IF signals

are connected in counter clockwise, the signals are cancelled at the output as shown in the right side of Figure 2.9. Therefore with proper connection, we can get the IF signals while cancelling (rejecting) the thermal noise at the output of the polyphase filter as shown in Figure 2.10, where $R_P = \dfrac{1}{\omega_{IF} C_P}$

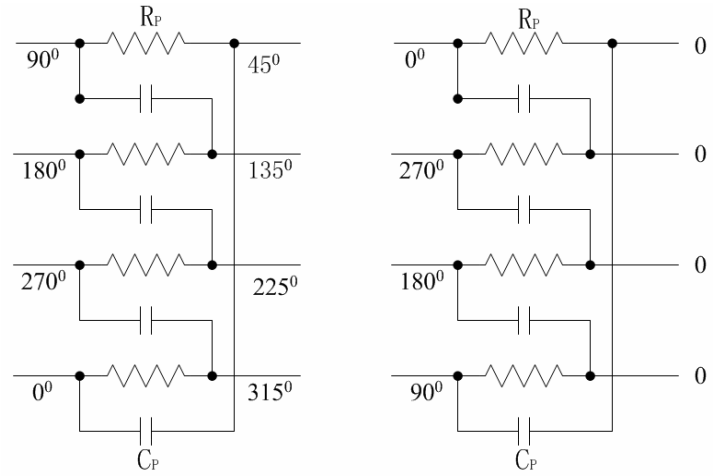


Figure 2.9 Polyphase Filter with Quadrature IF Input in Different Directions

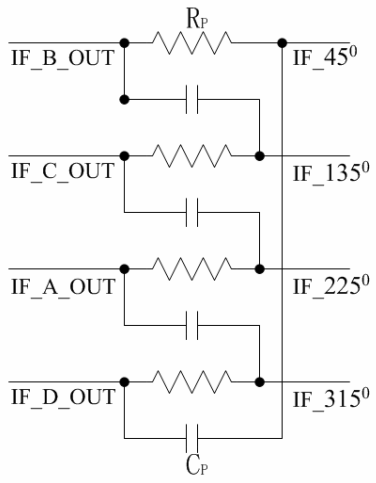


Figure 2.10 Image Rejection

As shown in Figure 2.10, if the quadrature MR signals from the output of the TIAs are connected to the polyphase filter at the sequence of IF_B_OUT, IF_C_OUT, IF_A_OUT, IF_D_OUT, according to equations (2.14) – (2.17), the quadrature MR signals are connected in clockwise and the quadrature thermal noises down-converted from the image frequency are connected in counter clockwise. Therefore, according to Figure 2.9, at the output of the polyphase filter, the thermal noise from the image frequency is rejected while the down-converted quadrature MR signals are reserved. From Figure 2.10, we can get two pair of differential MR signals, one is IF_45^0 and IF_225^0, the other is IF_135^0 and IF_315^0. Either one of these two pairs can be used as the differential input of the LPF and next to the VGA.

In the analysis about, all of the values of resistance, capacitance are assumed to be ideal, and the mixer gain, mixer phase mismatch are also assumed to be zero, however, in actually circuit design, the above values vary because of variation of process and temperature. Therefore, the image rejection ratio (IRR) becomes finite, and given in equation 2.18 [25], [31],

$$IRR \approx \frac{1}{4}\left(\left(\frac{\Delta A}{A}\right)^2 + (\tan(\theta))^2\right) \qquad 2.18$$

where ΔA and θ are the overall mismatches of gain and phase respectively between the quadrature signal paths because of the mismatches of the quadrature generator, mixer, and the polyphase filter. And A is the normalized overall gain of the signal path. For careful layout design of the capacitors, resistors and mixer, as well as good design skill of mixer, the IRR can be reduced to – 40 dB [25], [31], For the target of thermal noise rejection, this IRR value is small enough.

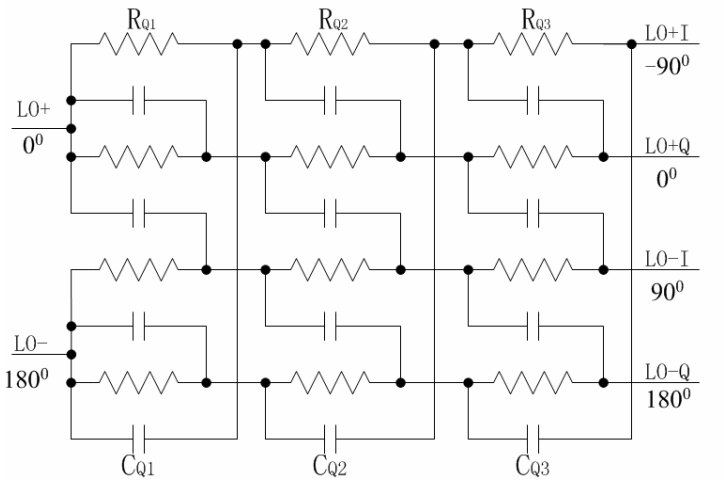


Figure 2.11 Wide-Band Quadrature Generator

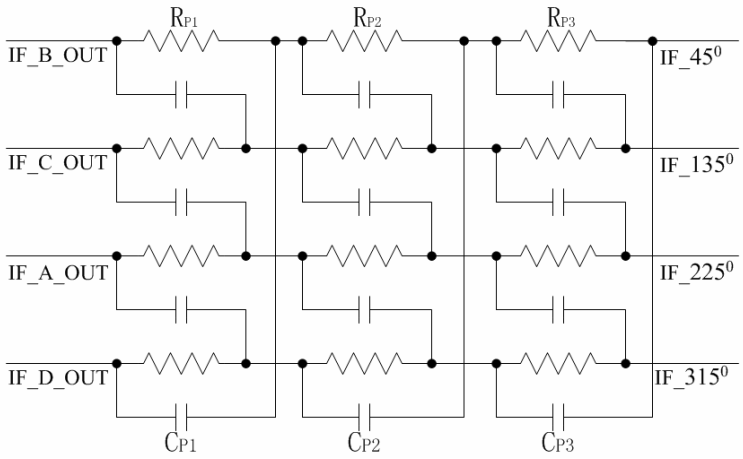


Figure 2.12 Wide-Band Polyphase Filter

Still one other problem exists. As shown in Figure 2.6 and Figure 2.10, the quadrature generator and the polyphase filter are both narrow-band. That is, the quadrature generator can only work at frequency of $\omega_{LO} = \frac{1}{R_Q C_Q}$, while the polyphase

filter can only work at frequency $\omega_{IF} = \frac{1}{R_P C_P}$. In order for wide-band application, multi-stage topology is used as shown in Figure 2.11 for the quadrature generator and Figure 2.12 for the polyphase filter, where $\frac{1}{R_{Q1}C_{Q1}} < \omega_{LO} = \frac{1}{R_{Q2}C_{Q2}} < \frac{1}{R_{Q3}C_{Q3}}$, and $\frac{1}{R_{P1}C_{P1}} < \omega_{IF} = \frac{1}{R_{P2}C_{P2}} < \frac{1}{R_{P3}C_{P3}}$. The values of $\frac{1}{R_{Q1}C_{Q1}}$, $\frac{1}{R_{Q3}C_{Q3}}$, $\frac{1}{R_{P1}C_{P1}}$ and $\frac{1}{R_{P3}C_{P3}}$ are selected in consideration of the 30% variation of the RC time constant as well as ensuring the IRR smaller than -40dB in the whole bandwidth. Specific values of the resistance and capacitance of the quadrature generator and polyphase filter are discussed and selected in circuits design Chapter III.

With the optimal architecture is determined, a four-channel RF front-end is to be designed on-chip or on a PCB. In order to reduce the amount of hardware resources, multiplexing technique is applied after the RF front-ends so that one digitizer and other signal processing blocks can be shared by multiple channels. There exist two types of multiplexing technique, one is frequency domain multiplexing (FDM), and the other is time domain multiplexing (TDM) [4], [5], [15], [16].

2.2 Multiplexing Techniques

2.2.1 Frequency Domain Multiplexing

As illustrated in Figure 2.13, an operational amplifier (opamp) adds up the output voltages of each channel and sends them to the digitizer for digitization. After

digitization, each channel is separated by software (using digital filter) from the four-channel digitized signals and is then ready for image reconstruction.

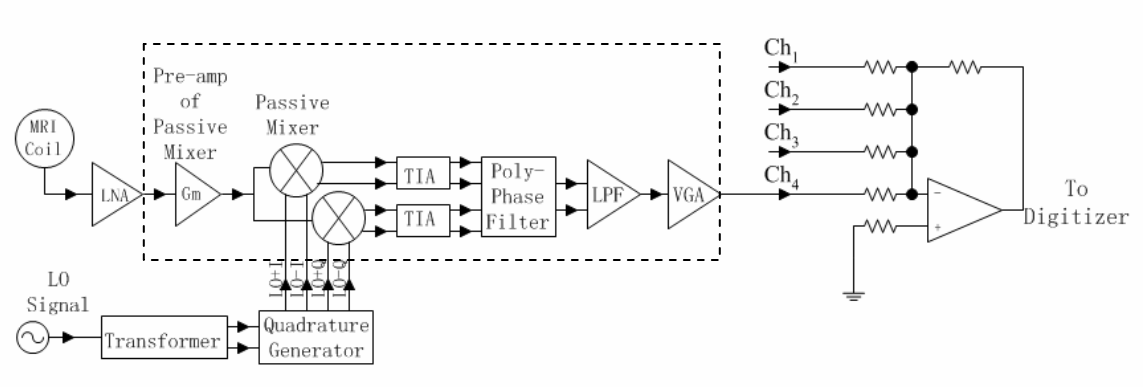


Figure 2.13 Frequency Domain Multiplexing
(The blocks within the dashed line area are on-chip)

Compared with the RF front-ends in wireless communications application, which select a single desired channel from other signal channels and signal bands with different frequencies, the FDM, on the other hand, combines a certain number of channels with different frequencies into a multi-channel signal. Therefore, the FDM technique introduces the following two problems, which reduce the SNR of the MR signal.

Problem 1: Signal to Distortion Ration (SDR) Reduced by Third Order Inter-Modulation (IM_3) Products:

As shown in Figure 2.14, due to the nonlinearity of active components, when two signals, at different frequencies f_1 and f_2, pass through the opamp, two IM_3 products are produced at the output of the opamp.

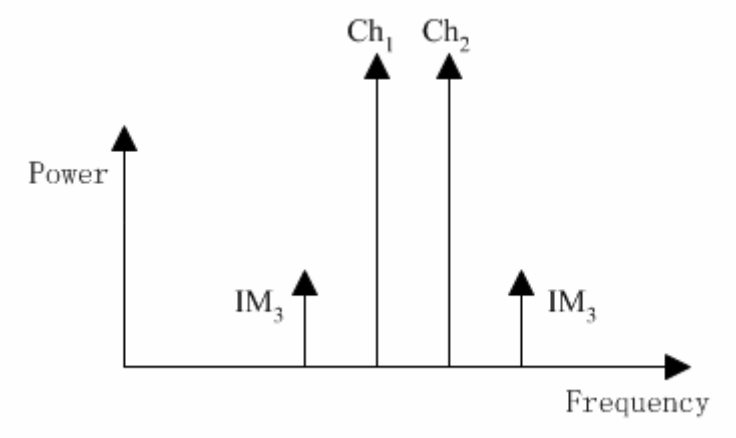


Figure 2.14 Third Order Inter-Modulation

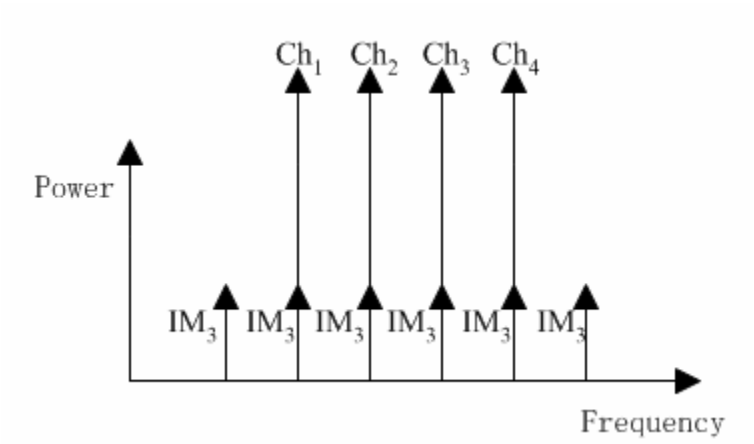


Figure 2.15 Dynamic Range Reduced by IM_3 Products

If four channels with the same channel spacing are added by the opamp, as illustrated in Figure 2.15, Ch_1 and Ch_2 produce IM_3 product on Ch_3, while Ch_2 and Ch_3 produce IM_3 product on Ch_1 and Ch_4, in addition, Ch_3 and Ch_4 produce IM_3 product on Ch_2. These IM_3 products can be treated as noise and decrease the SNR of each channel of signal.

Therefore the linearity of the opamp has to be improved in order to decrease the effects of IM_3 products on the SDR. A term of "IIP_3" is used in literature to denote the linearity according to the following equation

$$IIP_3 = \frac{(P_{out} - IM_3)}{2} + P_{in} \qquad 2.19$$

where P_{out} is the output signal power and P_{in} is the input signal power. We can assume that the SNR of a MR signal is 90dB for a 200MHz MRI experiment, and the gain of the opamp is 10dB, while the output signal power is 0dBm. We can easily compute that $IIP_3 = 35dBm$ in order to ensure that the IM_3 products are smaller than the thermal noise, which is too high for an opamp design.

Solution of Problem 1: Frequency Re-Arrangement

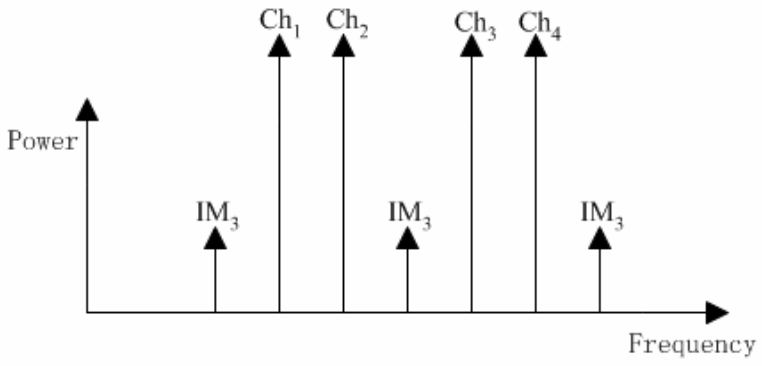


Figure 2.16 Frequency Re-Arrangement

If we re-arrange the frequency of each channel by increasing the channel spacing between Ch_2 and Ch_3, from Figure 2.16, we can find that none of the IM_3 products is at

the same frequency of any channel. However, the total bandwidth of the multiplied signals is therefore increased, and the requirement of the sampling frequency of the ADC is tightened. Moreover, the channel spacing turns into un-even.

Problem 2: Effect of LO Frequency Phase Noise on the Down-Converted Signals

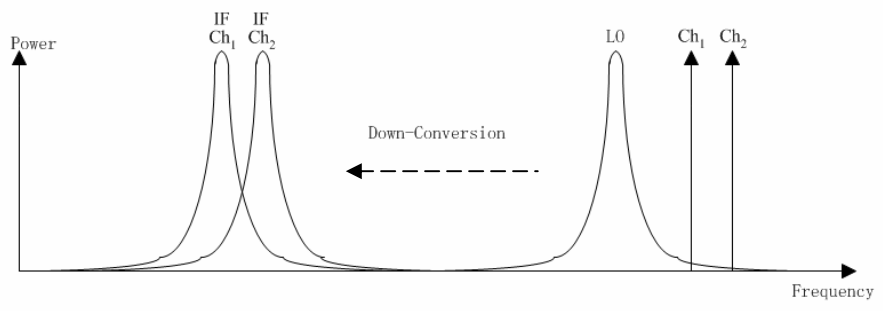


Figure 2.17 Effect of LO Frequency Phase Noise on the Down-Converted Signals

Because of the phase noise of the LO frequency, each down-converted IF signal contains the phase noise as illustrated in Figure 2.17. The phase noise of IF signal extends to adjacent channels, and therefore decreases the SNR of adjacent channels.

We can assume that the channel spacing (the frequency difference between the center frequencies of adjacent channels deducted by channel bandwidth a channel as illustrated in Figure 2.18.) is 100kHz, and the bandwidth of each channel is 20kHz. Normally, the LO frequency has a phase noise of $-144 dBc/\sqrt{Hz}$, at 100kHz offset for FLUKE 6080A [32] (The phase noise of another excellent frequency synthesizer HP

8656B is at the same level of FLUKE 6080A [33]), and therefore the phase noise energy of a certain channel on the adjacent channel is

$$-144+10\times\log_{10}(2\times10^{4})=-101dBc$$

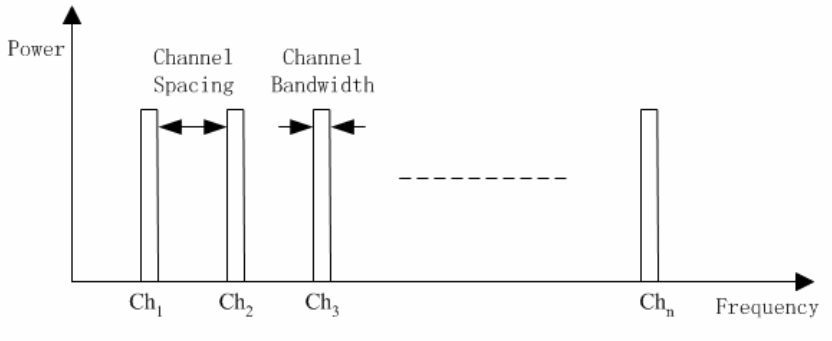


Figure 2.18 Illustration of Channel Spacing

If the channel spacing is smaller, for example, decreases to 20kHz, the phase noise of $-141dBc/\sqrt{Hz}$ at 20kHz offset for FLUKE 6080A, the phase noise energy of a certain channel on the adjacent channel is

$$-141+10\times\log_{10}(2\times10^{4})=-98dBc$$

If the channel spacing continues to decrease, for example, decreases to 1kHz, the phase noise is $-106dBc/\sqrt{Hz}$ at 1kHz offset for FLUKE 6080A, and the phase noise energy of a certain channel on the adjacent channel is

$$-106+10\times\log_{10}(2\times10^{4})=-63dBc$$

The following table is a summary of the calculated SNR of different offset frequency.

Table 2.1 SDR of Different Offset Frequency

Frequency Offset	1kHz	20kHz	100kHz
SNR	63dB	98dB	101dB

From the calculation results, we can evaluate that the channel spacing needs to be close to about 20kHz in order to maintain the SNR larger than 90dB. Considering the channel bandwidth, the frequency spacing between the center frequencies of the adjacent channels has to be larger than about 20kHz plus channel bandwidth. That is 40kHz in this case.

The previous calculation is based on the assumption of 20kHz channel bandwidth. In order to generalize the calculation, we can denote the bandwidth as B. Therefore the equation of the SNR is

$$SNR = -(Phase\_noise + 10 \times \log_{10}(B)) \tag{2.20}$$

That is, if the channel bandwidth is B, the SNR of a certain channel equals to the value in Table 2.1 deducted by $10 \times \log_{10}(\frac{B}{2 \times 10^4})$.

Based on the previous analysis, the application of the FDM approach on MRI is examined in the following. In parallel MRI experiments using phase array coils in [10], the spin echo signal is sensed and sampled by the RF front-end during the existence of the frequency encoding pulse, however, during this time interval, the phase encoding pulse does not exist as illustrated in Figure 2.19, therefore, the MR signal of each channel experiences the same frequency encoding and has the same carrier frequency.

Therefore, the FDM approach can not be applied in parallel MRI experiments using phase array coils before the experiment is modified.

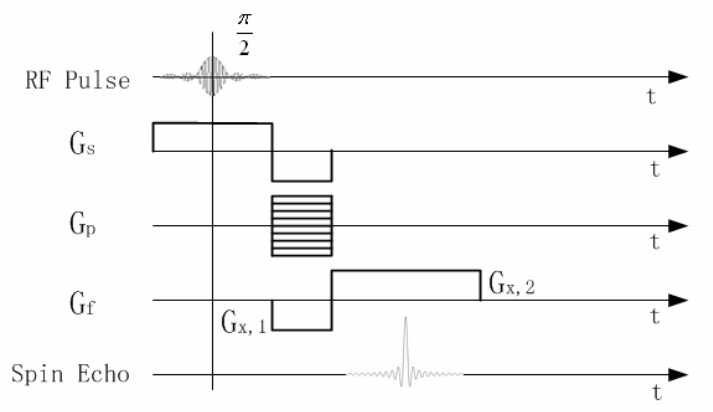


Figure 2.19 Gradient Echo Sequence for MRI

In another case, the SEA MRI experiment [3], [9], in which the coil array is placed parallel to the direction of main magnet field, and the slice selection gradient is orthogonal to the coil array plane, while the frequency encoding is along the direction of main magnet, the spatial localization provided by each phase encoding line is replaced by the spatial localization of each coil. In SEA, there is no phase encoding gradient and each coil experiences the same frequency encoding, and therefore, each MR signal from each coil has the same carrier frequency and FDM approach can not be applied in this case either before modification.

In order to explore the possibility of applying the FDM approach on parallel MRI experiments, an idea is proposed by applying a magnet gradient across the coil array, as

illustrated in Figure 2.20 and Figure 2.21 only to separate the carrier frequency of each coil.

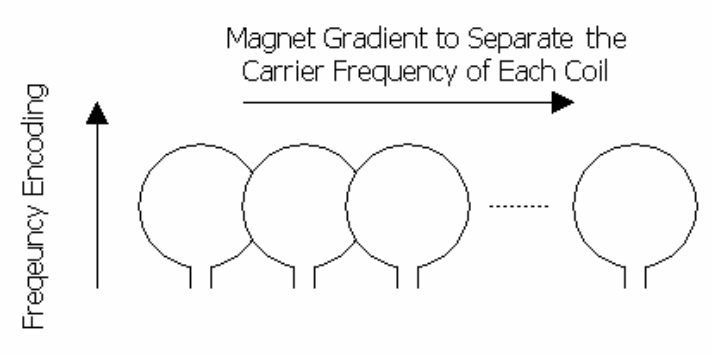


Figure 2.20 Simplified Illustration of
Applying a Magnet Gradient across the Phase Array

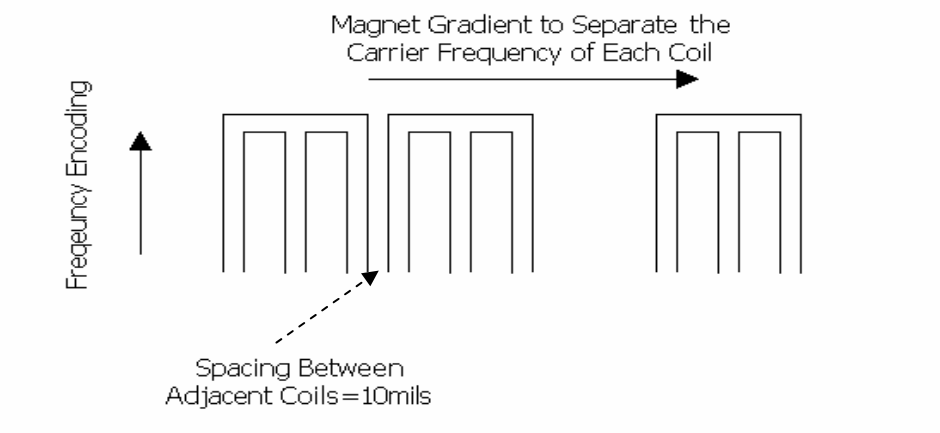


Figure 2.21 Simplified Illustration of
Applying a Magnet Gradient across the Planar Coil Array in SEA

As illustrated in Figure 2.20, each coil has a small part of its area overlapping its adjacent coils in order for decoupling, therefore, no matter how large the frequency separation magnet gradient is, frequency overlapping exists between adjacent channels

and therefore channel spacing is not larger than zero. Therefore the FDM approach can not be applied in this case although a magnet gradient is applied on the phase array to separate the center frequency of MR signal from each coil.

In the case of SEA, the spacing between the centers of the adjacent coils is 2mm, and the maximum frequency spacing between the center frequencies of the adjacent channels is 4kHz, therefore, using FDM, the SDR is limited. What is even worse, the channel bandwidth is mainly determined by the gradient of the frequency encoding because the length of each coil is much larger than the width of each coils. The bandwidth is possible to be much larger than the frequency spacing between the center frequencies of the adjacent channels. Therefore, frequency overlapping is possible to happen in this case.

Therefore, although the FDM approach provides a possible approach for parallel MRI experiment, based on the previous analysis, the approach is limited by bad SDR, and even can not be applied on parallel MRI experiments because of adjacent channel frequencies overlapping. As a possible method of overcoming these disadvantages, time domain multiplexing (TDM) technique is investigated.

2.2.2 Time Domain Multiplexing

The TDM receiver for MRI was first proposed and demonstrated as illustrated in Figure 2.12 by Wright et al. [4], [5], [15], [16]. (The down-conversion is dual-stage in [4], [5], [15], [16], and is simplified to single-stage in Figure 2.22 for the purpose of simplification.)

As illustrated in Figure 2.22, the RF switch is placed before the down-conversion mixer, and connects each signal source to the rest of the receiver chain in a sequence of time slots [16]. Each signal source is modulated by the switching waveform, and the resulting frequency spectrum of the modulated signal can be written as [16]

$$S_{mux}(f) = \sum_{n=-\infty}^{\infty} A_n S(f - nf_m) \tag{2.21}$$

where $S_{mux}(f)$ is the modulated MR signal, and f_m is the switching frequency. A_n is given by

$$A_n = \frac{\sin(\frac{n\pi}{N})}{n\pi} \tag{2.22}$$

where N is the duty ratio of the switching waveform.

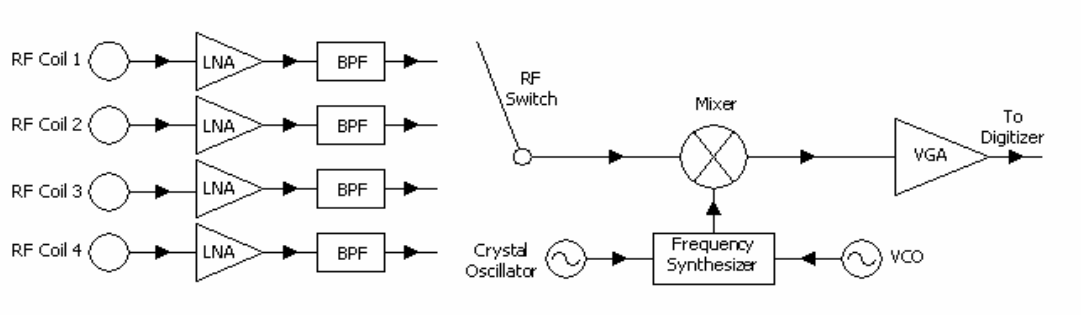


Figure 2.22 Multi-Channel RF Front-End with TDM

Investigating the frequency spectrum of the modulated signal, we can find that if a low-pass filter is placed anywhere after the RF switch, the high frequency part of the modulated signal is suppressed and crosstalk happens [16]. Therefore, the low-pass filter

originally succeeding the mixer is removed, and instead, a band-pass filter is placed before the RF switch in order to attenuate the thermal noise.

Compared with its FDM counterpart, the TDM architecture solves the two problems described previously because the signals are time-multiplexed in TDM instead of being frequency-multiplexed. In addition, TDM also enjoys fewer numbers of mixers and needs only one VGA.

However, TDM architecture also has the following disadvantages:

1. Insertion loss is possible to be introduced by the RF switch.
2. The channel number is limited by the ADC sampling frequency.
3. Crosstalk is introduced by the limited time-constant, $\tau = RC$, or in other word, bandwidth, of the stages succeeding the RF switch. That is, the channel number is limited by the receiver bandwidth [5].
4. The band-pass filter before the mixer needs to be high order and therefore is expensive and lossy.
5. The band-pass filter is out-of-chip.
6. Because of 1 and 4, additional gain stage is necessary.

Moreover, if CMOS circuits are designed, the CMOS analog circuit designer has the following difficulties:

1. The circuit of high order band-pass filter is much more complex than the low-pass filter, and if designed on chip, the high order band-pass filter consumes a large chip area and introduces much noise.
2. The RF switch can be designed using CMOS switch, however, the large charge-

injection by the CMOS switch introduces voltage spike at the input of the mixer because the input capacitance of the mixer is required to be as small as possible in order to reduce the time-constant $\tau = RC$. If charge injection cancellation circuit is used, the complexity of the circuit increases, and thermal noise is introduced.

3. The conversion gain of the mixer is limited in order to reduce the input capacitance.

Therefore the following modified TDM architecture is proposed by moving the RF switch backwards to after the receiver front-end, as illustrated by Figure 2.23.

2.3 Proposed Multi-Channel RF Front-End with TDM

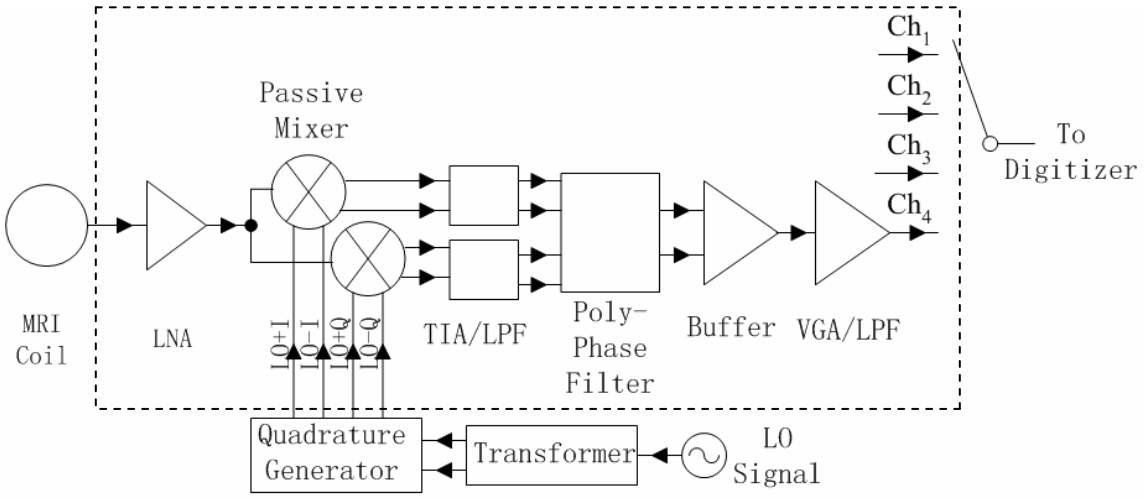


Figure 2.23 Proposed Architecture of the Four-Channel Front-End with TDM
(The blocks within the dashed line area are on-chip)

As illustrated in Figure 2.23, the proposed architecture solves the originally TDM technique. First, the energy at frequency of $f_{LO}+f_{RF}$ after the mixer is suppressed by the low-pass filter, and the bandwidth of this low-pass filter does not affect the crosstalk among the multiplexed channels because it is placed before the RF switch. Second, the band-pass filter in Figure 2.22 is removed. This makes it possible for fully on-chip design of the whole receiver because the high order band-pass filter is very difficult for on-chip design as discussed above. Third, the limited time constants of the mixer and the VGA do not cause crosstalk because the modulation of MR signal by the switching waveform happens after those stages.

CHAPTER III

CMOS CIRCUIT DESIGN OF THE RF FRONT-END

According to the discussion and the proposed architecture in Figure 2.23, a four-channel RF front-end was designed using TSMC 0.18μm technology on a single silicon substrate. Each channel of the RF front-end includes an ultra low noise amplifier, a passive mixer with a TIA which also acts as a low-pass filter, a quadrature generator and a polyphase filter, another low-pass filter which also acts as a variable gain amplifier (VGA). The receiver has an overall NF of 0.935dB, variable gain from about 80dB to 90dB, power consumption of 30.8mW, and chip area of 6mm^2.

3.1 Low Noise Amplifier Design

In MR experiment, the SNR of the MR signal from each planar coil is much smaller than the SNR of the MR signal from multi-turn solenoid coil because MR signal coupled by the planar coil is much smaller than that of multi-turn solenoid coil with the same size of its planar counterpart. Therefore, in order to maintain good image SNR, the NF of the RF front-end has to be as small as possible. In order to reduce the NF of the RF front-end, the NF of the LNA has to be as small as possible so that the noise introduced by the LNA is as low as possible, while the gain of the LNA has to be as large as possible in order to suppress the noise of the succeeding stages as much as possible.

In the society of analog circuit design, most of the research and designs of LNA are for the applications of wireless communications, which require the LNA to be preceded by a band-pass RF filter to attenuate the out of band signals. And this filter demands the input impedance of the LNA to be 50Ω, otherwise, poor and unpredictable performance of the filter will be resulted [25], [34]. Therefore, most of the CMOS LNAs using common source topology reported in literature were designed to have input impedances of 50Ω at the sacrifice of noise figure deviating from their minimum values. CMOS common gate LNAs with 50Ω input impedances using capacitive cross-coupling technique to reduce the noise figure were also reported in literature but the noise figure of which are still very difficult to be reduced to 2dB [35]-[45]. In the factor of power consumption, in wireless communications equipments, especially the portable terminals which are power supplied by battery, the LNA is required to be designed with power constrain. This also makes the NF of the LNA deviate from its minimum value. Therefore, LNAs with NF from 3dB to 5dB in digital TV, from 2dB to 3dB for Zigbee, Bluetooth equipment, 0.8dB to 2dB for GPS are mostly reported in literature.

However, in the applications of MRI, first, the MR signal from the output of the MR coil is “clean”, that is, no out of band signals exist, and the RF band-pass filter preceding the LNA is not necessary. Therefore the input impedance of the LNA is allowed to be other than 50Ω. Second, the output impedance of the coil can also be matched by passive components to an optimal value to acquire minimum NF for the LNA. Third, the MRI receiver is power supplied inside the lab instead of battery, therefore, the power constrain can be relaxed for acquiring optimal NF for the LNA.

Based on the above analysis, a common source LNA is analyzed and a topology for minimizing the NF is designed in the following.

3.1.1 CS LNA Noise Figure

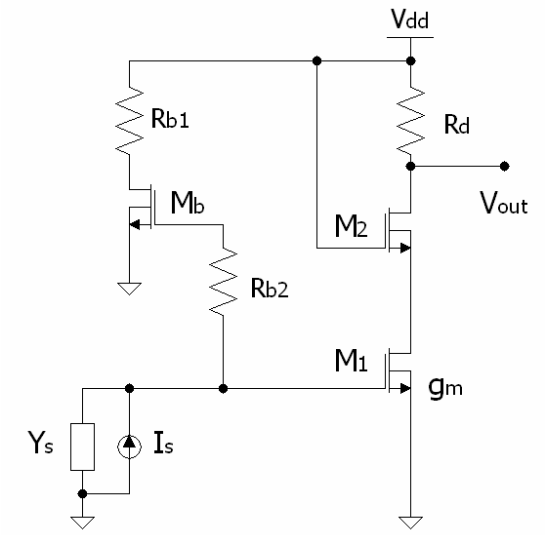


Figure 3.1 Common Source LNA

The common source LNA topology is shown in Figure 3.1. Y_s and I_s are the signal source inner admittance and signal source current respectively. R_{b1}, R_{b2} and M_b compose the DC bias circuit for the input transistor M_1. Normally there is a very large DC block capacitor between the signal source and the bias circuit. This DC block capacitor is not shown in Figure 3.1 in order for simplification. The DC bias circuit may contribute noise at the input of M_1, and therefore degrades the NF of the LNA. However, the noise of R_{b1} and M_b can be ignored because the noise current of R_{b1} and most of the noise current of M_b do not go through the input of the LNA. Moreover, the channel

width of M_b is designed to be very small, and the noise current of which is very small. The noise of R_{b2} can also be ignored if R_{b2} is much larger than $Z_s//R_{in}$ [17] for the reason that if R_{b2} is very large compared with $Z_s//R_{in}$, the noise current, $\frac{4kT\Delta f}{R_{b2}}$, will be very small, and when a portion of this noise current goes through $Z_s//R_{in}$, the noise voltage, $\frac{4kT\Delta f}{R_{b2}} \times (\frac{R_{b2} \times (Z_S // R_{in})}{Z_S // R_{in} + R_{b2}})^2 \approx \frac{4kT\Delta f \times (Z_S // R_{in})^2}{R_{b2}}$, at the output of the LNA will be very small and can be ignored. The cascode transistor M_2 reduces the miller effect of C_{gs} and isolates the output circuit and input circuit of the LNA in order to improve S_{12}, and therefore increase the stability of the LNA [17]. The noise contribution of M_2 at the output of the LNA, $4kT\gamma g_{d0\_1} \times (\frac{1/g_{m2}}{1/g_{m2} + r_{01}})^2$, can also be ignored because it is very small, where g_{m2} is the transconductance of M_2, and r_{01} is the transistor output resistance of M_1 deduced by Channel-Length-Modulation characteristic of transistor and is much larger than $1/g_{m2}$ with careful design. γ and g_{d0} are very important for thermal noise of transistor and will be defined and analyzed later.

According to the analysis above, with carefully design, the noise of the DC bias circuit and the cascode transistor M_2 can be ignore. The noise of LNA is mainly from the transducer transistor M_1. The noise performance of the LNA can be analyzed using the model illustrated in Figure 3.2 by ignoring the noise of the DC bias circuit and M_2.

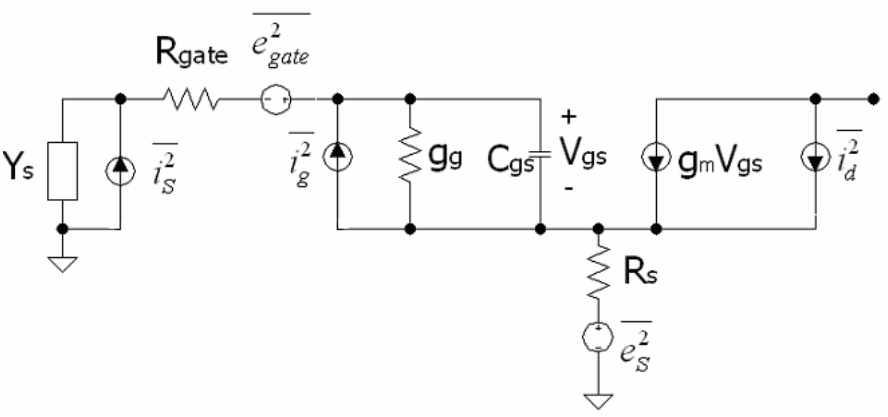


Figure 3.2 Small Signal Noise Performance Model of CS LNA

In order to analyze the noise performance model shown in Figure 3.2 [46]-[50], we need to give the definitions of the variables in the model and analyze them as the following.

Y_s: As shown in Figure 3.2, Y_s is the signal source admittance and equal to $G_s + jB_s$, where G_s is the signal source conductance and B_s is the signal source susceptance. $\overline{i_S^2}$ is the mean-square noise current of the signal source, and equal to $4kTG_S\Delta f$.

R_{gate}: R_{gate} is the polysilicon gate resistance given by [46] as

$$R_{gate} = R_{sh}\frac{W_{eff}}{12n^2 L_{eff}} + \frac{R_{con}}{W_{eff}L_{eff}} \qquad 3.1$$

where R_{sh} is the sheet resistance of the gate polysilicon reasonably given as 10Ω/sq [46], [51], and R_{con} is the contact resistance of silicon-to-poly and is about $25\,Ohms\cdot\mu m^2$ [46], [51]. n is the finger number of transistor M_1 in layout. With carefully layout design using multi-finger, it can be reduced at about 1Ω using TSMC 0.18μm

technology. W_{eff} and L_{eff} are the effective channel width and channel length of the transistor respectively. $\overline{e_{gate}^2}$ is the thermal noise of R_{gate}, and equals to $4kTR_{gate}\Delta f$.

C_{gs}: C_{gs} is the Gate-Source capacitance which dominates the imaginary part of the LNA input impedance, and is given by [46] as

$$C_{gs} = \frac{2}{3} W_{eff} L_{eff} C_{ox} + C_{gs,m} \tag{3.2}$$

where C_{ox} is gate-oxide capacitance per unit area, and is give by a unit of F/cm^2. $C_{gs,m}$ is the capacitance which is contributed by the metal connection around the transistor, and is around 1.8fF to 18.4fF for TSMC 0.18μm technology [46]. This capacitance is very small compared with $\frac{2}{3} W_{eff} L_{eff} C_{ox}$.

$\overline{i_d^2}$: $\overline{i_d^2}$ is the mean-square noise current of the transistor drain, and equal to $4kT\gamma g_{do}\Delta f$, where γ is a parameter depending on the bias and is used to account for the drain current noise[34]. g_{do} is defined as the drain conductance of the transistor at zero-bias [17]. γ and g_{do} are given respectively as the following equations [34].

$$\gamma = \frac{1}{[(V_{GS} - V_t) + LE_{sat}]^2} [\frac{2}{3}(LE_{sat})^2 + 2(V_{GS} - V_t)LE_{sat} + 2(V_{GS} - V_t)^2] \tag{3.3}$$

$$g_{do} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t) \tag{3.4}$$

where E_{sat} is given as

$$E_{sat} = \frac{2V_{sat}}{\mu_{eff}} \approx \frac{2V_{sat}}{\mu 0} \tag{3.5}$$

In the testing data of TSMC 0.18μm technology [52] provide by MOSIS as

$$V_{sat} = 8.821037 \times 10^4 \text{ m/s}$$

$$\mu 0 = 265.5797979 \text{ cm}^2/(V \cdot S)$$

$$L_{eff} = L_{drawn} - \text{L}_{\text{LINT}} = 0.14552 \mu\text{m}$$

therefore, $LE_{sat} \approx L\dfrac{2V_{sat}}{\mu 0} = \dfrac{0.14552\mu\text{m} \times 2 \times 8.821037 \times 10^4 \text{ m/s}}{265.5797979 \text{ cm}^2/(V \cdot s)} = 0.996V$

We can assume that $V_{GS} - V_t$ is around 0.1V to 0.2V. Then we can use MATLAB to evaluate the value of γ in TSMC 0.18μm technology as the following plot. From Figure 3.3, we can fine that γ is about 0.73 to 0.8, which is only a little larger than γ of the long channel transistor: 2/3. In the calculation of NF, we can use $\gamma = 0.8$ as worst case.

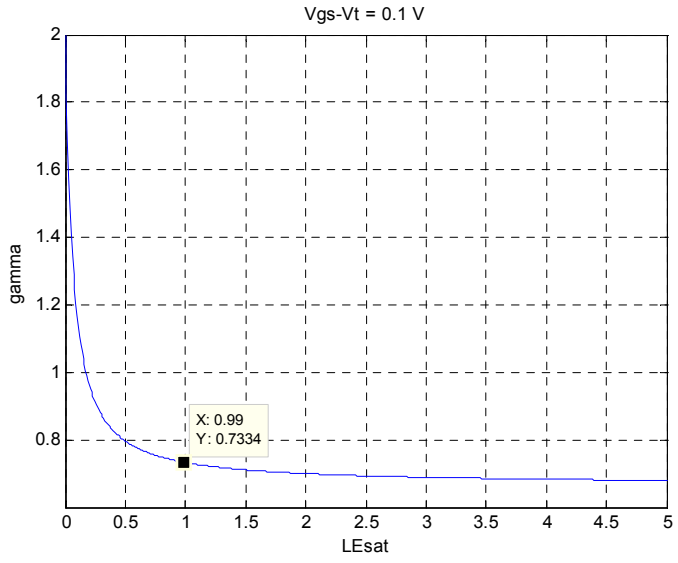


Figure 3.3 Plot of γ as a Function of LE_{sat}

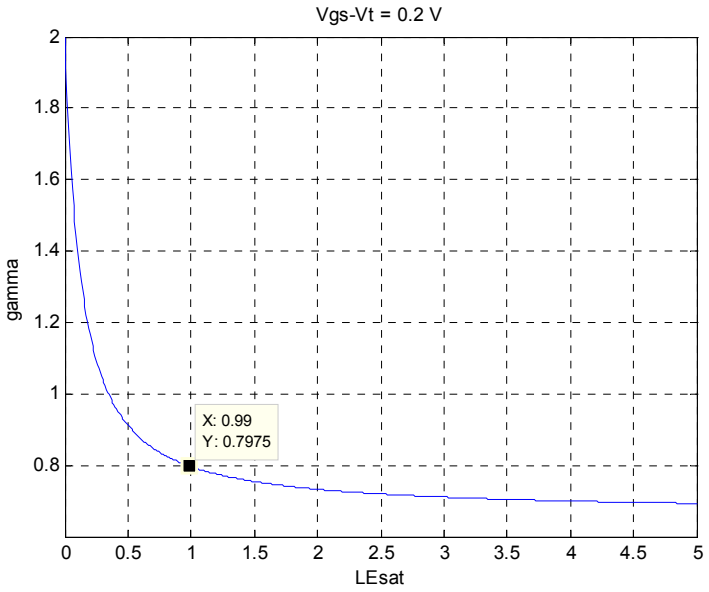


Figure 3.3 (Continued)

R_S**:** As shown in Figure 3.2, R_S is the transistor Source resistance which can be reduced to below 0.5Ω with careful design by increasing the number of the transistor fingers in layout. $\overline{e_S^2}$ is the thermal noise of R_S [46], and equals to $4kTR_S\Delta f$.

$\overline{i_g^2}$ and g_g: One other important noise source is the gate noise $\overline{i_g^2}$. The channel voltage fluctuation caused by the channel thermal noise is coupled by the gate-source capacitance C_{gs}, and therefore leading to a portion of the gate noise current $\overline{i_g^2}$ [17], [53], [54], which is given by [53]-[55] as

$$\overline{i_g^2} = 4kT\delta g_g \Delta f \qquad 3.6$$

where [34]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \qquad 3.7$$

$$\delta = \frac{1}{[(V_{GS} - V_t) + E_{sat}L]^4}[\frac{4}{3}(E_{sat}L)^4 + \frac{17}{2}(E_{sat}L)^3(V_{GS} - V_t) + 23(E_{sat}L)^2(V_{GS} - V_t)^2 + 45E_{sat}L(V_{GS} - V_t)^3 + \frac{15}{2}(V_{GS} - V_t)4] \quad 3.8$$

Then we can use equation to evaluate the value of δ using MATLAB as the following. And we can fine that δ is about 1.7 to 2, which is not much larger than δ of the long channel transistor: 4/3. And in the calculation of NF, we can use $\delta = 2$ as a worst case.

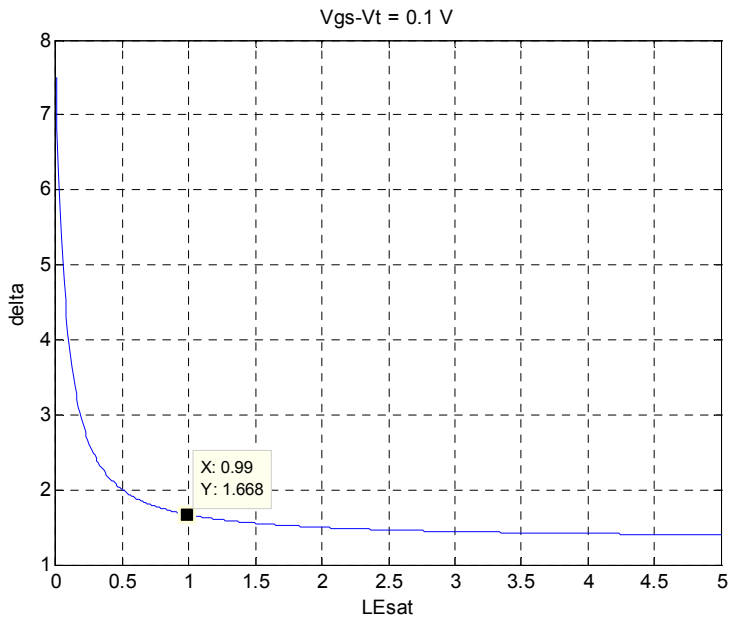


Figure 3.4 Plot of δ as a Function of LE_{sat}

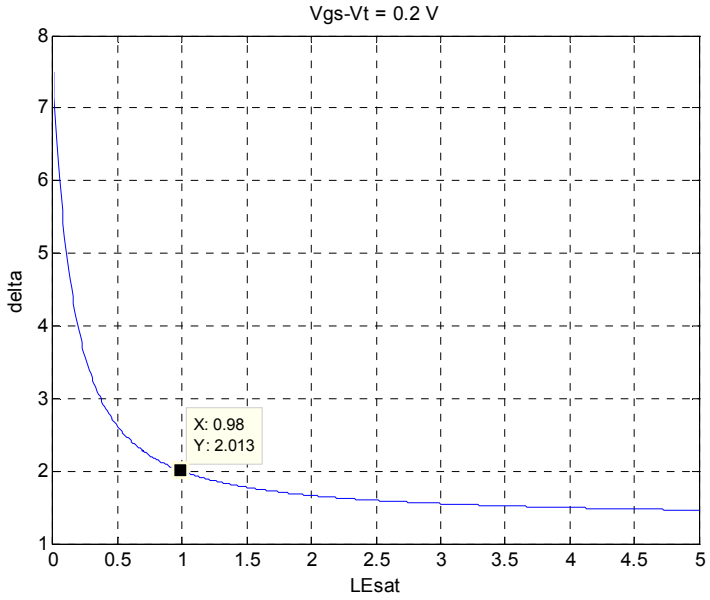


Figure 3.4 (Continued)

As analyzed previously, a portion of $\overline{i_g^2}$ is induced from the voltage fluctuation of the drain thermal noise, $\overline{i_g^2}$ is partly correlated with $\overline{i_s^2}$, therefore, we can divide $\overline{i_g^2}$ as two parts, $\overline{i_{gu}^2}$ and $\overline{i_{gc}^2}$, which are uncorrelated part and correlated with $\overline{i_s^2}$ respectively. That is

$$\overline{i_g^2} = \overline{i_{gu}^2} + \overline{i_{gc}^2} = 4kT\delta g_g(1-|c|)\Delta f + 4kT\delta g_g|c|\Delta f \qquad 3.9$$

where c is the correlation coefficient between the gate and drain noise current, and is given by[34], [53], [54] as

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} \times \overline{i_d i_d^*}}} \qquad 3.10$$

$$c = j\sqrt{\frac{5}{\gamma\delta}}\varepsilon \tag{3.11}$$

where $$\varepsilon = \frac{(E_{sat}L)^2}{[(V_{GS}-V_t)+E_{sat}L]^3}[\frac{1}{6}E_{sat}L+\frac{1}{2}(V_{GS}-V_t)] \tag{3.12}$$

Now, we can use MATLAB to evaluate the value of c, and get the following plot with different value of $V_{GS}-V_t$. We can find that c ranges from $j0.33$ to $j0.274$ for TSMC 0.18μm technology. This range value is close to that of the long channel technology.

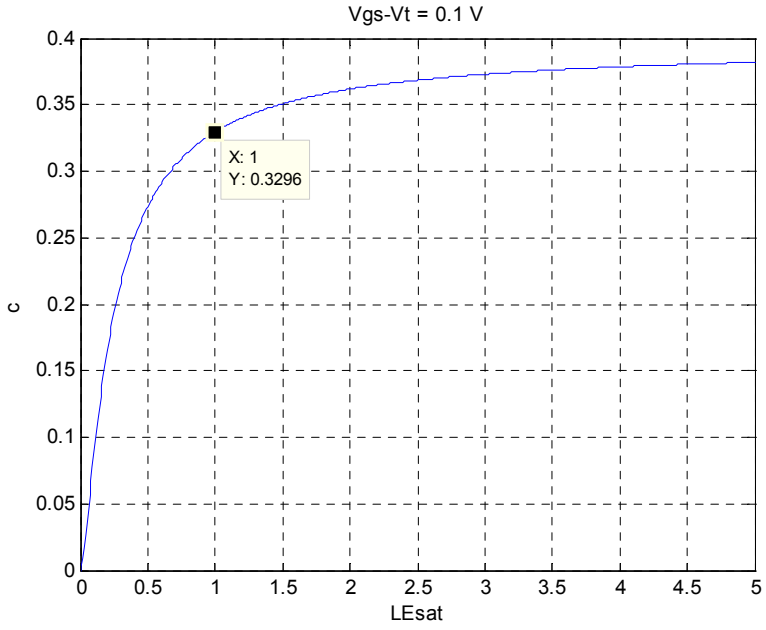


Figure 3.5 Plot of c as a Function of LE_{sat}

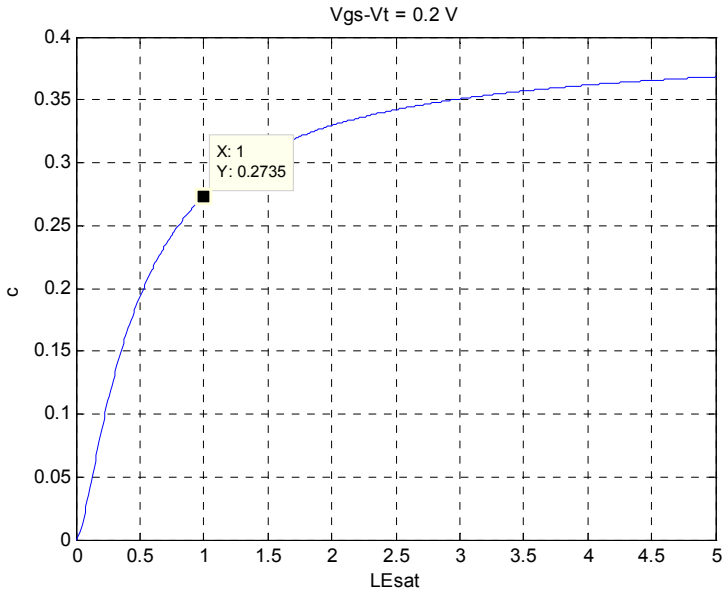


Figure 3.5 (Continued)

In order to simplify the calculation, we can convert the noise performance model shown in Figure 3.2 to Figure 3.6 as the following by converting R_{gate} to g_{gate} in shunt with C_{gs}, and $\overline{e_{gate}^2}$ to $\overline{i_{gate}^2}$ in shunt with C_{gs}. The conversion is illustrated in Figure 3.7.

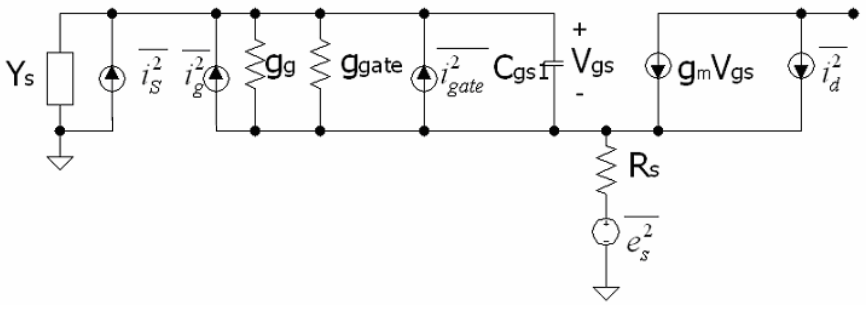


Figure 3.6 Equivalent Small Signal Noise Performance Model of CS LNA

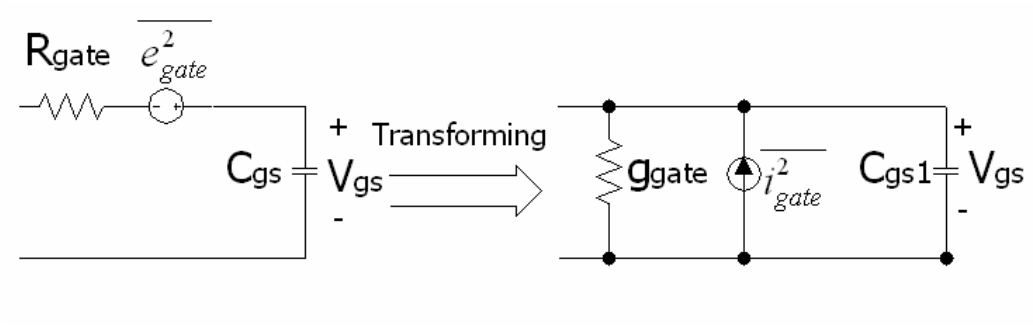


Figure 3.7 Conversion of Series R_{gate}, $\overline{e^2_{gate}}$ to Shunt g_{gate}, $\overline{i^2_{gate}}$

The calculation is as the following.

$$j\omega C_{gs1} + g_{gate} = \frac{1}{R_{gate} + \frac{1}{j\omega C_{gs}}} = \frac{j\omega C_{gs} + \omega^2 {C_{gs}}^2 R_{gate}}{1 + (R_{gate}\omega C_{gs})^2} \qquad 3.13$$

As, we know, R_{gate} can be reduced to smaller than 1Ω. And C_{gs} is smaller than 1pF even in worst case, therefore, at 200MHz, $(R_{gate}\omega C_{gs})^2$ is much smaller than 1. Then we can simplify equation (3.13) to equation (3.14)

$$j\omega C_{gs1} + g_{gate} = \frac{j\omega C_{gs} + \omega^2 {C_{gs}}^2 R_{gate}}{1 + (R_{gate}\omega C_{gs})^2} = j\omega C_{gs} + \omega^2 {C_{gs}}^2 R_{gate} \qquad 3.14$$

that is,
$$C_{gs1} = C_{gs} \qquad 3.15$$

and
$$g_{gate} = \omega^2 C_{gs}^2 R_{gate} \qquad 3.16$$

Comparing equation $g_{gate} = \omega^2 {C_{gs}}^2 R_{gate}$ with $g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$, and assuming that $g_{d0} = 10 \sim 40 m\frac{A}{V}$ and $R_{gate} = 1Ohm$ in worst case, if we ignore g_{gate}, there will be a

maximum error of 5~20% for the conductance between gate and source. After we got the value of g_{gate}, we can get $\overline{i_{gate}^2} = 4kTg_{gate}\Delta f$. And we can get the equivalent LNA noise model as Figure 3.8, where

$$g_g + g_{gate} = \omega^2 C_{gs}{}^2 (\frac{1}{5g_{d0}} + R_{gate}) \tag{3.17}$$

$$\overline{i_g^2} + \overline{i_{gate}^2} = \overline{i_{gu}^2} + \overline{i_{gc}^2} + \overline{i_{gate}^2} = 4kT[g_{gate} + \delta g_g(1-|c|)]\Delta f + 4kT\delta g_g|c|\Delta f \tag{3.18}$$

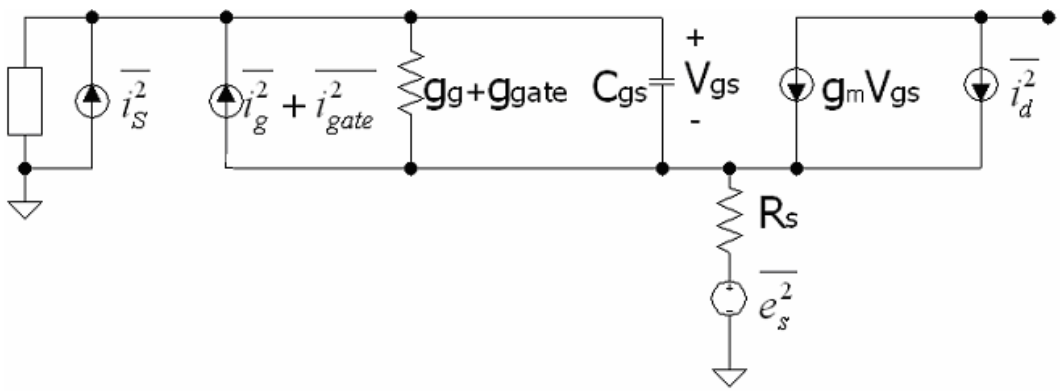


Figure 3.8 Rearranged Equivalent Small Signal Noise Performance Model of CS LNA

Next, we can calculate the noise figure of the LNA by calculating the noise current at the output of the LNA introduced by each noise source.

R_s: Using the equivalent circuit of Figure 3.9, we can get

$$i_{os} = \frac{i_s \times \frac{g_m R_s}{j\omega C_{gs}}}{Z_S + R_{gate} + R_g + \frac{1}{j\omega C_{gs}} + \frac{g_m R_s}{j\omega C_{gs}} + R_s} \tag{3.19}$$

$$\overline{i_{os}^2} = \frac{\overline{i_s^2} \times \frac{g_m^2 R_s^2}{\omega^2 C_{gs}^2}}{[\mathrm{Re}(Z_S) + R_{gate} + R_g + + R_s]^2 + [Lm(Z_S) + \frac{1}{\omega C_{gs}} + \frac{g_m R_s}{\omega C_{gs}}]^2} \tag{3.20}$$

$$\overline{i_s^2} = \frac{4kT\Delta f}{R_s} \tag{3.21}$$

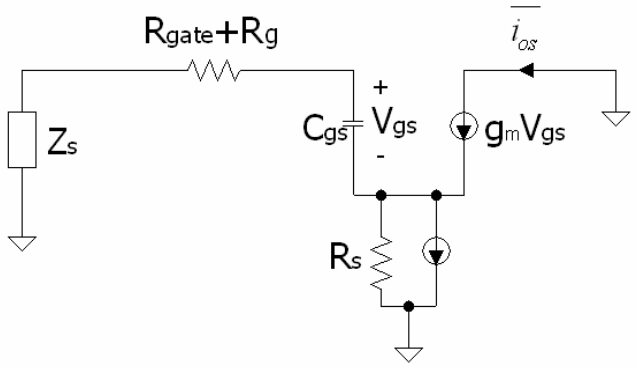


Figure 3.9 Equivalent Small Signal Model to Calculate $\overline{i_{os}^2}$

$\overline{i_d^2}$: Using the equivalent model shown in Figure 3.10, we can get

$$i_{od} = \frac{i_d \times (Z_S + R_{gate} + R_g + \frac{1}{j\omega C_{gs}})}{Z_S + R_{gate} + R_g + \frac{1}{j\omega C_{gs}} + \frac{g_m R_s}{j\omega C_{gs}} + R_s} \tag{3.22}$$

$$\overline{i_{os}^2} = \frac{\overline{i_s^2} \times \{[(\mathrm{Re}(Z_S) + R_{gate} + R_g]^2 + [Lm(Z_S) + \frac{1}{\omega C_{gs}}]^2\}}{[\mathrm{Re}(Z_S) + R_{gate} + R_g + + R_s]^2 + [Lm(Z_S) + \frac{1}{\omega C_{gs}} + \frac{g_m R_s}{\omega C_{gs}}]^2} \tag{3.23}$$

$$\overline{i_d^2} = 4kT\gamma g_{do}\Delta f \tag{3.24}$$

Comparing equations (3.19), (3.20), (3.21) and (3.22), (3.23), (3.24), we can find that the noise introduced by R_s at the output of LNA is much smaller than that of $\overline{i_d^2}$, therefore, in the following calculation, it is reasonable to ignore the noise from R_s.

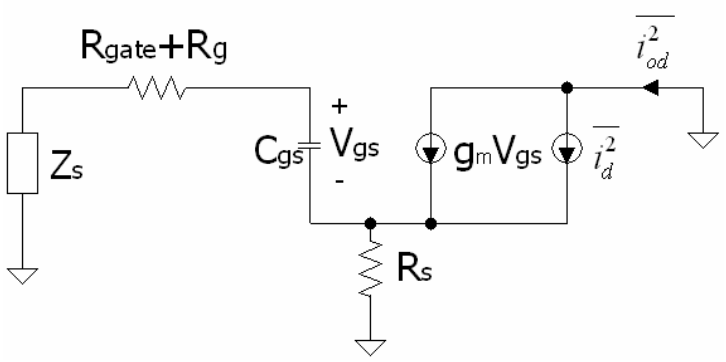


Figure 3.10 Equivalent Small Signal Model to Calculate $\overline{i_{od}^2}$

Moreover, with observation of the denominator of equation (3.22), we can find that $\frac{g_m R_s}{j\omega C_{gs}}$ is much smaller than $\frac{1}{j\omega C_{gs}}$, and R_s is much smaller than $R_{gate} + R_g$. Therefore in the following calculation, it is reasonable to assume that R_s is zero. Moreover, when calculating the noise contribution of signal source noise, $\overline{i_g^2}$, and $\overline{i_{gate}^2}$, in the denominator of the output noise current of each, we have similarly assumed that R_s is zero. Therefore, the small signal noise performance model of the LNA is simplified to Figure 3.11.

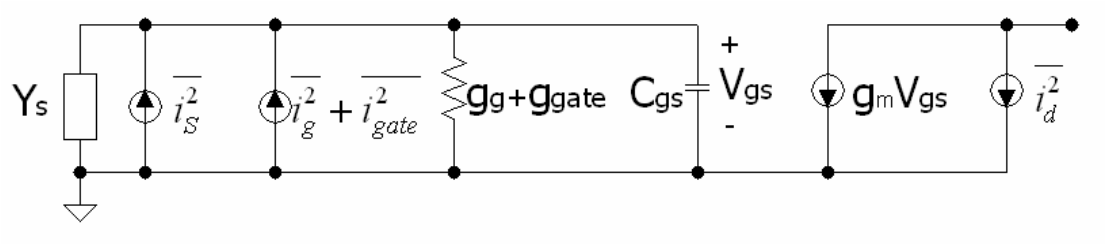


Figure 3.11 Equivalent Small Signal Model for Noise Factor Calculation

$$F = 1 + \frac{\overline{(i_{og} + i_{ogate} + i_{od})^2}}{\overline{i_{os}^2}} = 1 + \frac{\overline{i_{og}^2} + \overline{i_{ogate}^2} + \overline{i_{od}^2} + \overline{i_{og} i_{od}^*} + \overline{i_{og}^* i_{od}}}{\overline{i_{os}^2}} \quad 3.25$$

$$i_{os} = \frac{g_m i_s}{g_g + g_{gate} + G_S + j(\omega C_{gs} + B_S)} \quad 3.26$$

$$\overline{i_{os}^2} = \frac{g_m^2 \overline{i_s^2}}{(g_g + g_{gate} + G_S)^2 + (\omega C_{gs} + B_S)^2} \quad 3.27$$

$$i_{og} = \frac{g_m i_g}{g_g + g_{gate} + G_S + j(\omega C_{gs} + B_S)} \quad 3.28$$

$$\overline{i_{og}^2} = \frac{g_m^2 \overline{i_{og}^2}}{(g_g + g_{gate} + G_S)^2 + (\omega C_{gs} + B_S)^2} \quad 3.29$$

$$i_{ogate} = \frac{g_m i_{gate}}{g_g + g_{gate} + G_S + j(\omega C_{gs} + B_S)} \quad 3.30$$

$$\overline{i_{ogate}^2} = \frac{g_m^2 \overline{i_{ogate}^2}}{(g_g + g_{gate} + G_S)^2 + (\omega C_{gs} + B_S)^2} \quad 3.31$$

$$\overline{i_{og} i_{od}^*} = \frac{g_m \overline{i_g i_d^*}}{g_g + g_{gate} + G_S + j(\omega C_{gs} + B_S)} \quad 3.32$$

$$\overline{i_{og}^{*} i_{od}} = \frac{g_m \overline{i_g^{*} i_d}}{g_g + g_{gate} + G_S - j(\omega C_{gs} + B_S)} \tag{3.33}$$

And from (3.10), we know that [34]

$$\overline{i_{og} i_{od}^{*}} = (\overline{i_{og}^{*} i_{od}})^{*} = c\sqrt{\overline{i_g i_g^{*}} \times \overline{i_d i_d^{*}}} = j|c|\sqrt{\overline{i_g i_g^{*}} \times \overline{i_d i_d^{*}}} \tag{3.34}$$

Then we can get the noise factor

$$F = 1 + (\frac{\alpha\delta\omega^2 C_{gs}^2}{5 g_m G_S} + \frac{g_{gate}}{G_S}) + \frac{\gamma}{\alpha g_m G_S}[(g_g + g_{gate} + G_S)^2 + (\omega C_{gs} + B_S)^2] + 2|c|\sqrt{\frac{\delta\gamma}{5}} \frac{\omega C_{gs}}{g_m G_S}(\omega C_{gs} + B_S) \tag{3.35}$$

where G_S is real part of Y_S, and B_S is the imaginary part of Y_S.

And α is defined as

$$\alpha = \frac{1 + \rho/2}{(1+\rho)^2} \tag{3.36}$$

and

$$\rho = \frac{V_{GS} - V_t}{LE_{sat}} \tag{3.37}$$

therefore,

$$\alpha = \frac{1 + \frac{1}{2}(\frac{V_{GS} - V_t}{LE_{sat}})}{(1 + \frac{V_{GS} - V_t}{LE_{sat}})^2} = \frac{LE_{sat}[2LE_{sat} + LE_{sat}(V_{GS} - V)]}{2[LE_{sat} + (V_{GS} - V)]^2} \tag{3.38}$$

Now, we can use MATLAB to evaluate the values of α as shown in Figure 3.12, and we can find that α ranges from 0.76 to 0.87 in TSMC 0.18μm technology:

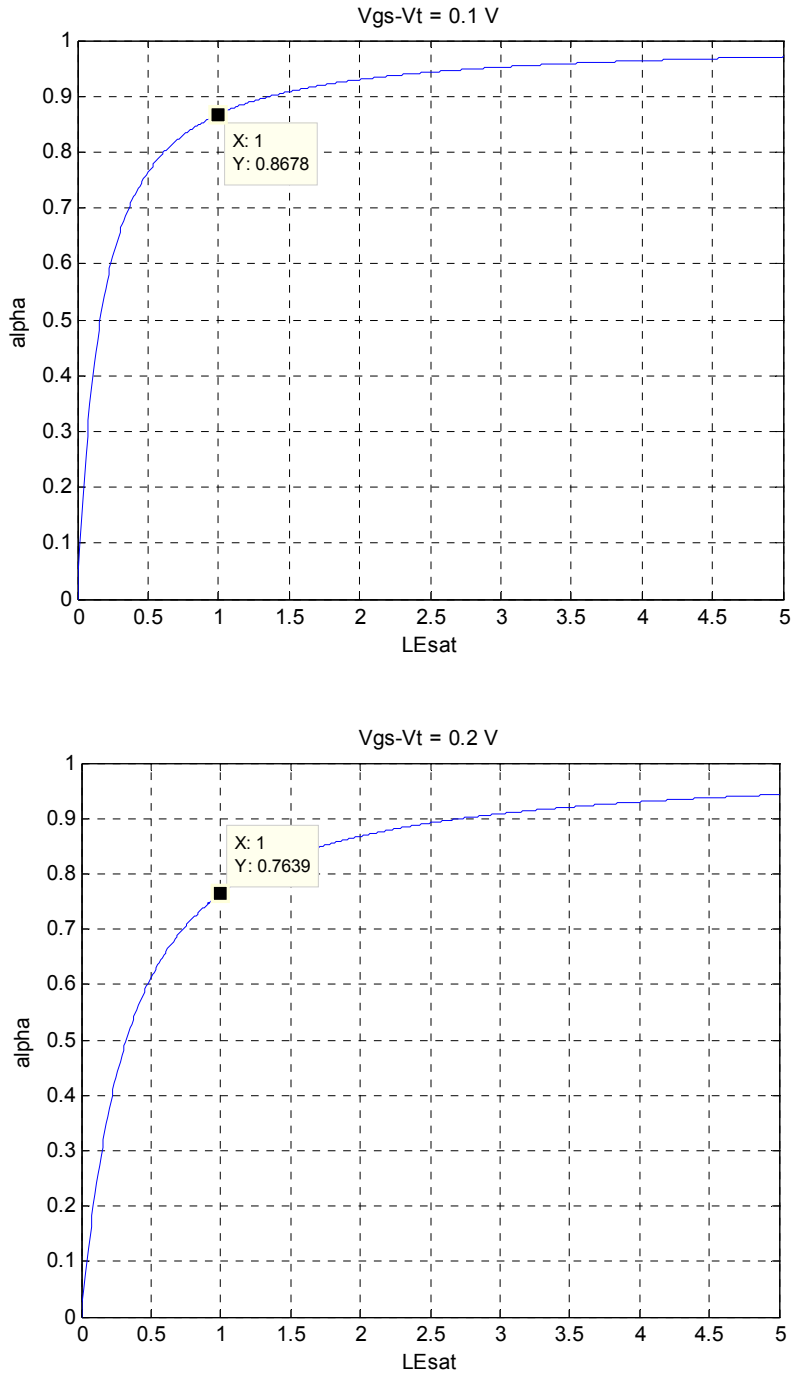


Figure 3.12 Plot of α as a Function of LE_{sat}

From equation (3.34), in order to determine the minimum noise factor, we can just take the first order derivation of the variables G_S and B_S, and set the derivation results to zero. Then we can get the optimal values for G_S and B_S to get minimum noise factor as

$$G_{Sopt} = \sqrt{(g_g + g_{gate})^2 + \frac{\alpha g_m g_{gate}}{\gamma} + \alpha^2 \omega^2 C_{gs}^2 \frac{\delta}{5\gamma}(1 - |c|^2)} \tag{3.39}$$

$$B_{Sopt} = -\omega C_{gs}(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}) \tag{3.40}$$

And we can get the equation of minimum noise factor by substituting G_{Sopt} and B_{Sopt} into equation and we can get

$$F_{\min} = 1 + \frac{(\frac{\alpha\delta\omega^2 C_{gs}^2}{5g_m} + g_{gate} + \frac{\gamma(g_g + g_{gate})^2}{\alpha g_m} - \frac{(\alpha\omega C_{gs}|c|\sqrt{\frac{\delta}{5}})^2}{\alpha g_m})}{\sqrt{(g_g + g_{gate})^2 + \frac{\alpha g_m g_{gate}}{\gamma} + \alpha^2\omega^2 C_{gs}^2 \frac{\delta}{5\gamma}(1 - |c|^2)}} + 2\frac{\gamma}{\alpha g_m}(g_g + g_{gate}) + \frac{\gamma}{\alpha g_m}\sqrt{(g_g + g_{gate})^2 + \frac{\alpha g_m g_{gate}}{\gamma} + \alpha^2\omega^2 C_{gs}^2 \frac{\delta}{5\gamma}(1 - |c|^2)} \tag{3.41}$$

For $\frac{\omega C_{gs}}{g_m} << 1$, the minimum noise factor becomes

$$F_{\min} = 1 + 2\sqrt{\frac{\delta\gamma}{5}(1 - |c|^2)}\frac{\omega}{\omega_T} \tag{3.42}$$

where

$$\omega_T = \frac{g_m}{C_{gs}} \tag{3.43}$$

ω_T is evaluated by the following equation.

$$\omega_T = \frac{3}{2}\mu_n \frac{1}{L^2}(V_{gs} - V_t)\frac{1+\rho/2}{(1+\rho)^2} \qquad 3.44$$

Using MATLAB we can get the value of $F_{\min}$ as a function of $V_{gs} - V_t$ using TSMC 0.18μm technology as shown in Figure 3.13, and we can find that $F_{\min}$ is very close to unity because $\frac{\omega}{\omega_T} << 1$ even at very small $V_{gs} - V_t$, which determine the power consumption of the LNA. Therefore, there exists the possibility to design LNA with very low noise figure and with very low power consumption because we have very small $\frac{\omega}{\omega_T}$.

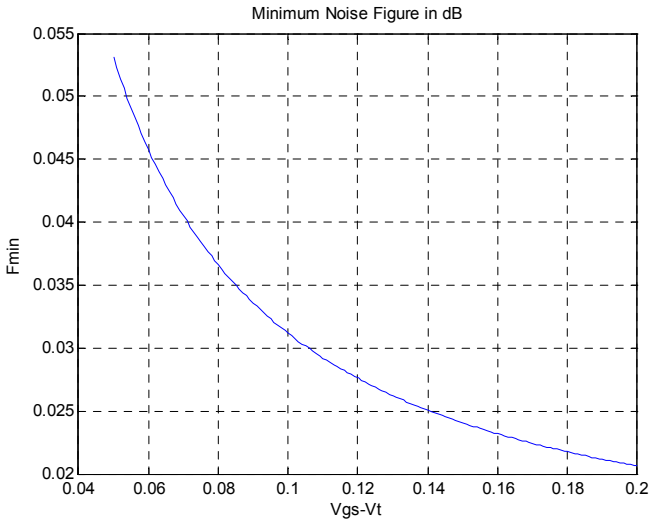


Figure 3.13 Plot of $F_{\min}$ as a Function of $V_{gs} - V_t$

However, from equation (3.39), for $\frac{\omega C_{gs}}{g_m} << 1$, G_{Sopt} becomes

$$G_{Sopt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{3.45}$$

And we rewrite the B_{Sopt} as

$$B_{Sopt} = -\omega C_{gs}(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{3.46}$$

where ωC_{gs} is $1.256mA/V$ if C_{gs} is 1pF at 200MHz, and therefore, both the real part and the imaginary part of the signal source impedance will be very large, that is, at the level of several hundred Ohms. This large requirement source impedance makes the matching very difficult because the capacitances of the matching network will be very small, and therefore, the output impedance of the matching circuit will be very sensitive to even a very small changes of the capacitance. In order to solve this problem, an "Extra Capacitor" is added in shunt with C_{gs}.

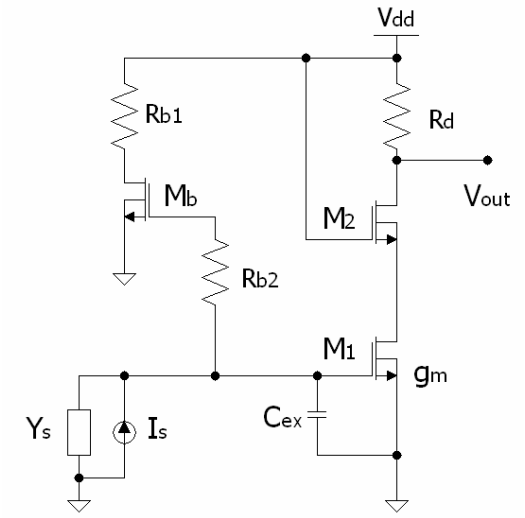


Figure 3.14 CS LNA with an "Extra Capacitor" in Shunt with C_{gs}

Nguyen et al. [56]-[58] firstly proposed a common source LNA topology with an "Extra Capacitor" to design an inductance source degeneration LNA with input impedance matched to 50Ω. Belostotski et al. [59] designed an inductance source degeneration LNA also with an "Extra Capacitor" connected in shunt with the gate and source of the transistor and acquired a noise figure as low as 0.25dB at 1.5GHz. Compared with the designs of Nguyen et al. [56]-[58] and Belostotski et al. [59], the LNA design of this work does not allow inductor because the receiver front-end is to be mounted on the same PCB with the MRI coil and placed in the magnet of the MRI system when imaging. Moreover, since the LNA is mounted close to the MRI coil, the LNA does not need to be matched to 50Ω. After carefully examining equations (3.35), (3.39), (3.40), (3.41), (3.45), (3.46), in this work, if an "Extra Capacitor" C_{ex} is connected in shunt with C_{gs} as shown in Figure 3.14, and if this C_{ex} is tuned to resonate the impedance of the MRI coil, G_S and B_S in equation (3.35) will be very small and very close to G_{Sopt} and B_{Sopt} as shown in equation (3.45), (3.46) respectively. And therefore, the noise figure of the LNA is very close to $F_{\min}$ as shown in equation (3.35).

The above discussion can also be analyzed in another way as the following.

The minimum noise factor and the optimal signal source impedance in Figure 3.14 are given in the following equations.

$$F_{\min} = 1 + 2\sqrt{\frac{\delta\gamma}{5}(1-|c|^2)}\,\frac{\omega}{\omega_T} \qquad 3.47$$

$$Z_{Sopt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}})}{\omega C_{gs}\{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + (\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}})^2\}} \quad 3.48$$

where $$C_t = C_{gs} + C_{ex} \quad 3.49$$

From equation (3.47), we can find that the minimum noise factor does not change by adding the "Extra Capacitor". And from equation (3.48), we can find that if C_{ex} is much larger than C_{gs}, the denominator of equation (3.48) will be largely increased and Z_{Sopt} is decreased with the same factor, and therefore, the circuit matching is relaxed.

3.1.2 CS LNA Gain and Power Consumption

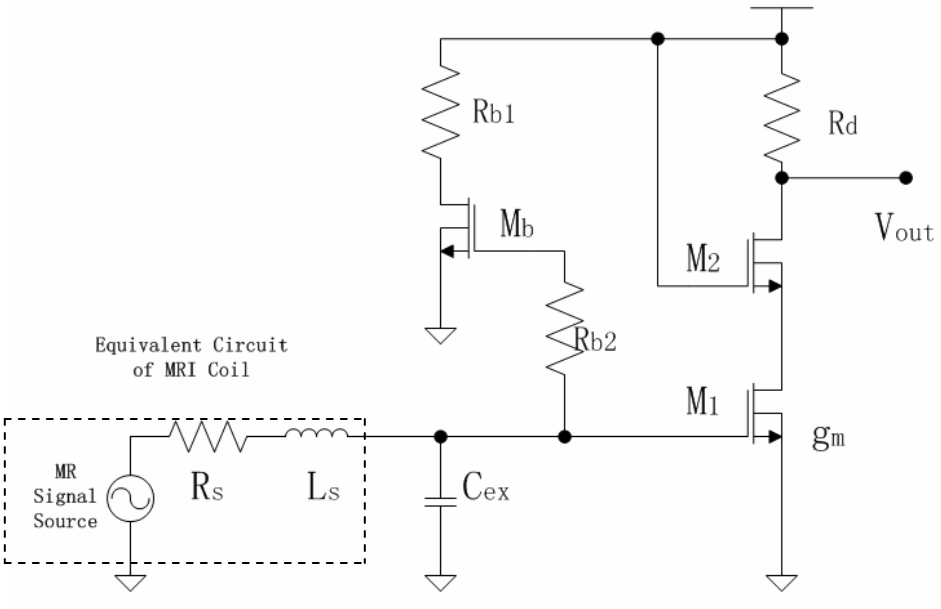


Figure 3.15 CS LNA Schematic with Equivalent circuit of MRI coil

In order to evaluate the gain of the LNA, we can analyze the LNA with the equivalent circuit of the MRI coil as shown in Figure 3.15. As an example but without loss of generality, equivalent circuit of the coil used in [3], [9] is analyzed here. Z_S is the signal source impedance and was given as the following.

$$Z_S = R_S + j\omega L_S \approx 1.78Ohms + j71Ohms \qquad 3.50$$

In order for analysis of the LNA conversion gain, Figure 3.15 is denoted as Figure 3.16.

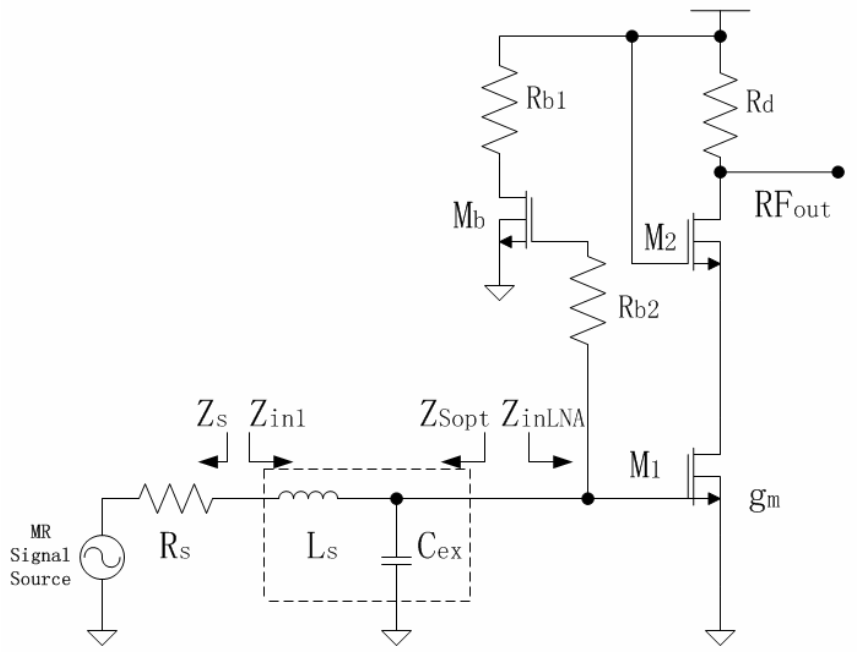


Figure 3.16 Schematic of CS LNA with Equivalent circuit of MRI coil

Z_{Sopt} is the optimal source impedance in order to acquire minimum LNA noise factor, and is given as equation (3.48). Z_{inLNA} is the input impedance of the LNA.

$$Z_{inLNA} \approx \frac{1}{R_g + \frac{1}{j\omega C_t}} = \frac{1}{\frac{1}{g_g} + \frac{1}{j\omega C_t}} \tag{3.51}$$

According to the power conservation theorem, we calculate the effective transconductance as the following [60]-[62].

$$g_{m,eff} = \frac{Z_{in1}}{Z_S + Z_{in1}} \times \sqrt{R_g \times real(\frac{1}{Z_{in1}})} \times g_m \tag{3.52}$$

where,

$$R_g = \frac{1}{g_g} \tag{3.53}$$

From equation (3.52), because R_g is very large, that is, the gain is very large although g_m is small in order to reduce the power consumption.

The power consumption can be evaluated by the supply voltage and the current of the transconductor. The supply voltage of TSMC 0.18μm technology is +/-0.9V, and the transconductor current is given as

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)^2 \frac{1+\rho/2}{(1+\rho)^2} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)^2 \alpha \tag{3.54}$$

As we know form equations (3.42), (3.43), (3.52), (3.53), we can get very low noise factor and very high gain although $(V_{gs} - V_t)$ is very small. In order to reduce the power consumption, we can choose $(V_{gs} - V_t)$ to be 0.1 V, and $\frac{W}{L} = 2000$, then we can get

$$I_D \approx 1.77mA$$

And we can find that the power consumption is very small.

3.1.3 CMOS Design and Simulation Result of LNA

According to the analysis above, a LNA was designed and simulated in TSMC CMOS 0.18μm technology. The simulation results are shown in Figure 3.17-3.22.

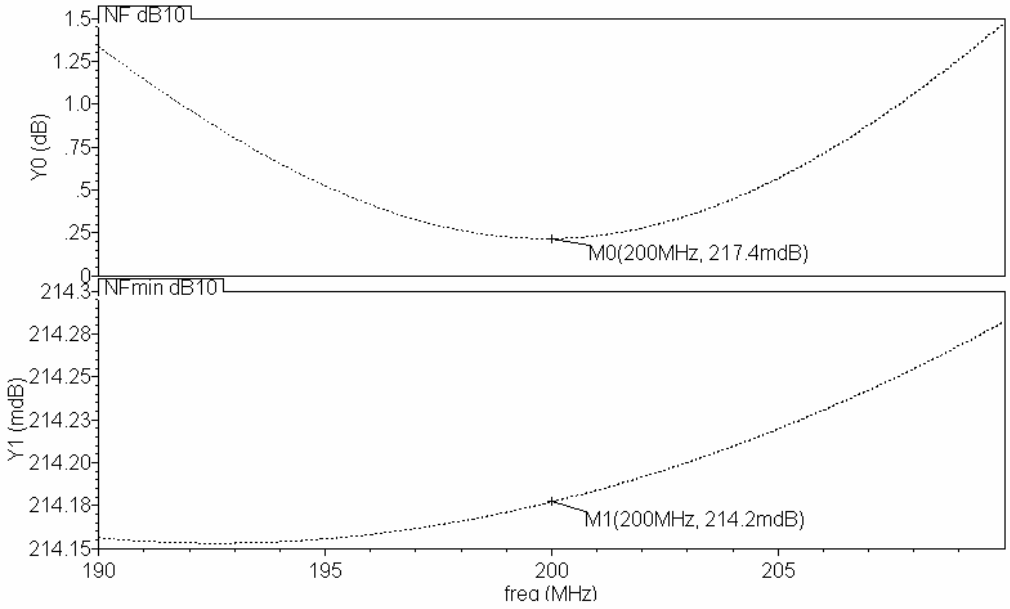


Figure 3.17 NF and NF_{min} of LNA

Device	Param	Noise Contribution	% Of Total
/PORT0	rn	1.02811e-15	95.02
M14.rb	rn	9.37108e-18	0.87
M14.m0	id	6.71315e-18	0.62
R15.Rpure	thermal_noise	3.49264e-18	0.32

Spot Noise Summary (in V^2/Hz) at 200M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.08198e-15
Total Input Referred Noise = 7.50018e-21
The above noise summary info is for noise data

Figure 3.18 Noise Summary of LNA

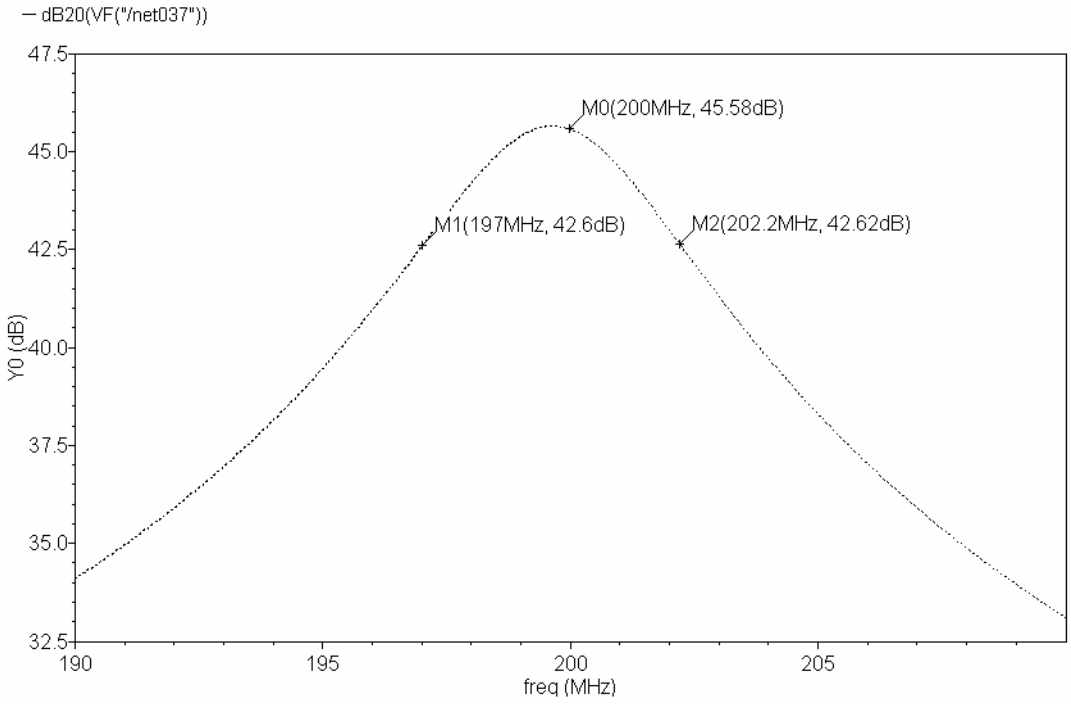


Figure 3.19 Conversion Gain of LNA

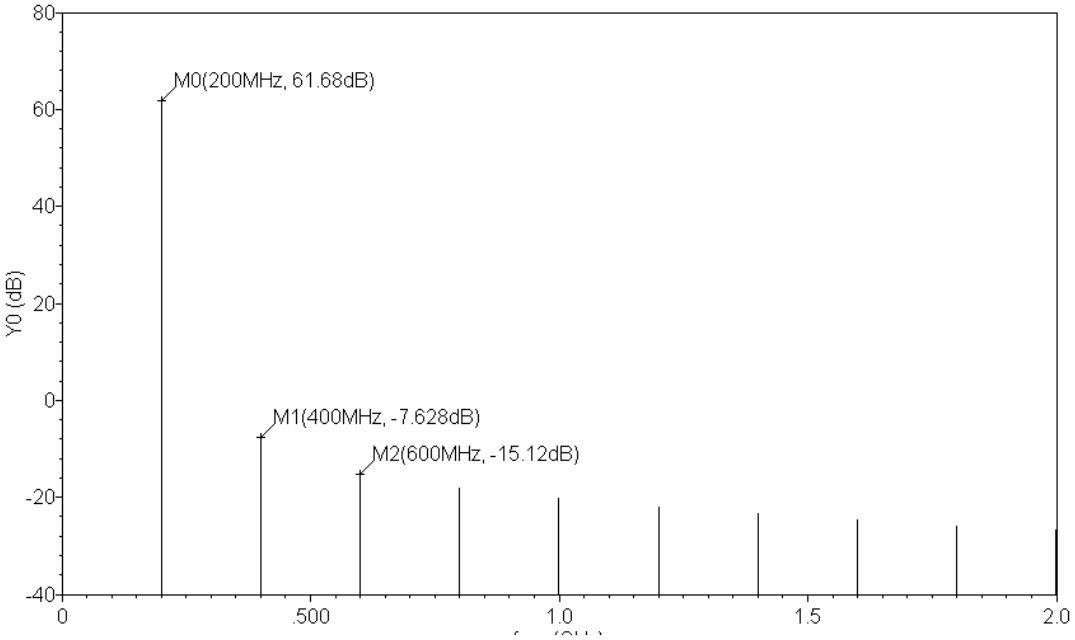


Figure 3.20 Harmonics of LNA

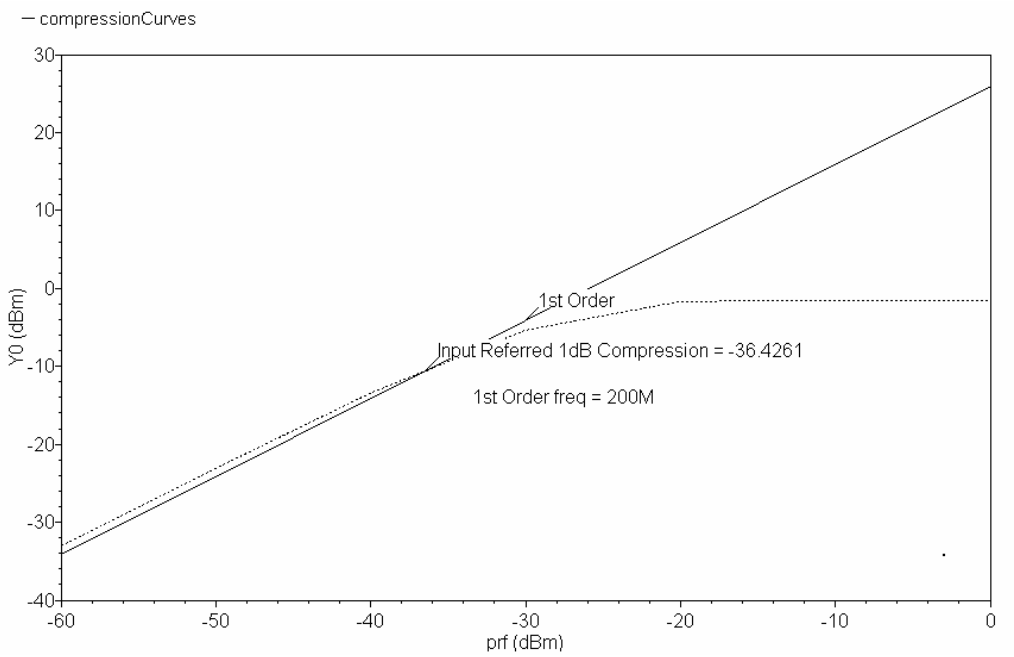


Figure 3.21 1dB Compression Point of LNA

i	-2.34045m	ibs	0
pwr	-2.10641m	ibulk	-2.84619n
v	900m	id	1.92635m
		ids	1.92634m
signal	OP("/V5" "??")	igb	0
i	-2.34045m	igcd	0
pwr	-2.10641m	igcs	0
v	900m	igd	0
		igs	0

Figure 3.22 Power Consumption of LNA

Figure 3.17 shows that the LNA noise figure is 0.217dB. This value is very close to the minimum noise figure which is 0.214dB as shown in Figure 3.17, and matches the calculation result very well. Figure 3.18 is the noise summary of each component, and shows that most of the noise is from the thermal noise of the parasitic resistance of the

MR coil, which introduces 95.02% of the total noise. The LNA introduced no more than 5% of the total noise.

Figure 3.19 shows that LNA conversion gain is 45.58dB. This value is much larger than a conversional LNA because is $g_{m,eff}$ much larger than g_m as being analyzed previously. This gain is large enough to suppress the noise figure of the succeeding stages. The -3dB bandwidth is 5.2MHz.

Figure 3.20 shows the harmonics of the LNA. The fundamental harmonic is at least 69.3dB larger than other higher order harmonics.

Figure 3.21 shows that the input referred 1dB compression point is -36.43dBm. This value seems small, however, note that the conversion gain is as large as 45.58dB, and the power supply voltage is +/-0.9V. This input referred 1dB compression point is large enough because the input signal from the MRI coil is much smaller than this value.

Figure 3.22 shows that the total current consumption of the LNA is 2.34mA and the current consumed by the LNA transconductor is 1.93mA. This value matches the analysis result above.

In order for summarization, the simulation results of the LNA specifications are listed in Table 3.1.

Table 3.1 Summary of LNA Simulation Results

Specification	Value
Noise Figure	0.217dB
Conversion Gain	45.58dB

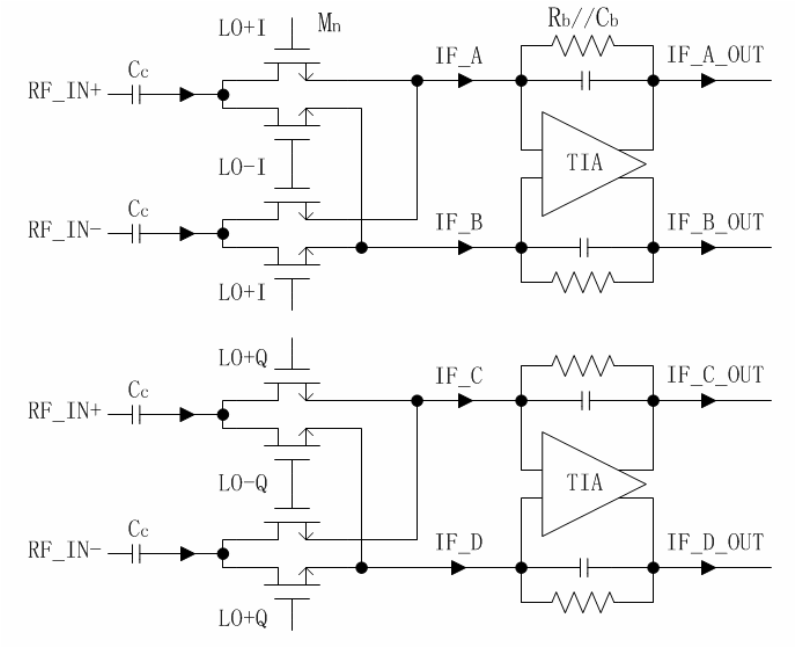
Table 3.1 (continued)

Specification	Value
-3dB Bandwidth	5.2MHz
Higher Order Harmonics	<-69.3dB (Compared with the Fundamental)
1dB Compression Points	-36.43dBm
IIP_3	-24.2dBm
Power consumption	4.2mW

In conclusion, the CMOS design of the LNA matches the analysis results in this chapter.

3.2 Mixer Design

The most commonly used topology of mixer is the Gilbert mixer, which effectively suppresses the LO frequency and RF feed-through to the IF. However, this topology suffers the trade-off among linearity, gain, thermal noise & headroom [17], [25], [63]. Moreover, this topology is vertically stacked by CMOS transistors, and therefore, for a voltage supply of +/-0.9V, the voltage headroom is limited for the trade-off. Finally, the flicker noise of this topology is high.



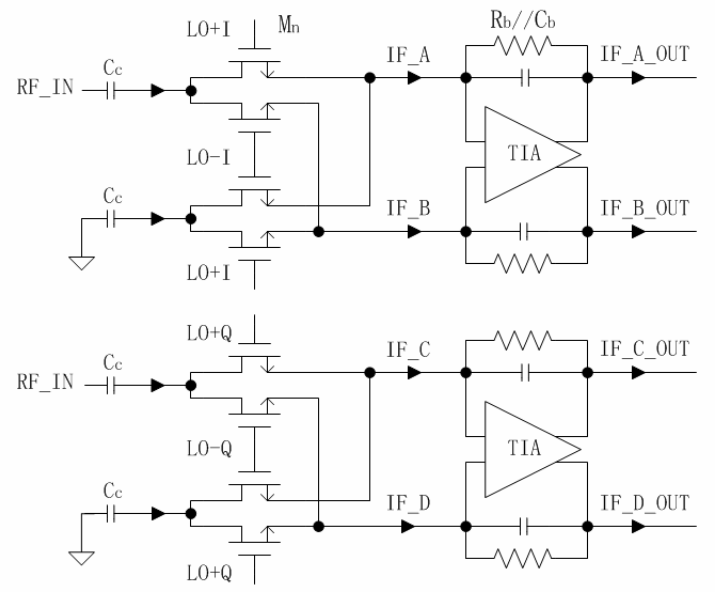
3.23 Double-Balanced Passive Mixer Design with Differential-Ended Input

In order to solve these problems, passive mixer [17], [25], [31], [64]-[69] topology as shown in Figure 3.23 is analyzed in the following. Compared with its Gilbert counterpart, this topology tips the CMOS transistors down instead of stacking them up vertically. Therefore, this topology enjoys more voltage headroom to relax the tradeoff among output voltage swing, linearity, and noise performance. Moreover and most importantly, since no DC current goes through the switching transistors, flicker noise is reduced.

As shown in Figure 3.16, note that RF signal at the output of the LNA is single-ended. In Figure 3.23, the RF signal at the input of the passive mixer is differential-ended for the double-balanced topology of the mixer in order to suppress the LO feed-

through to the output. Therefore an on-chip single-to-differential converter can be designed to convert the single-ended signal to differential-ended signal.

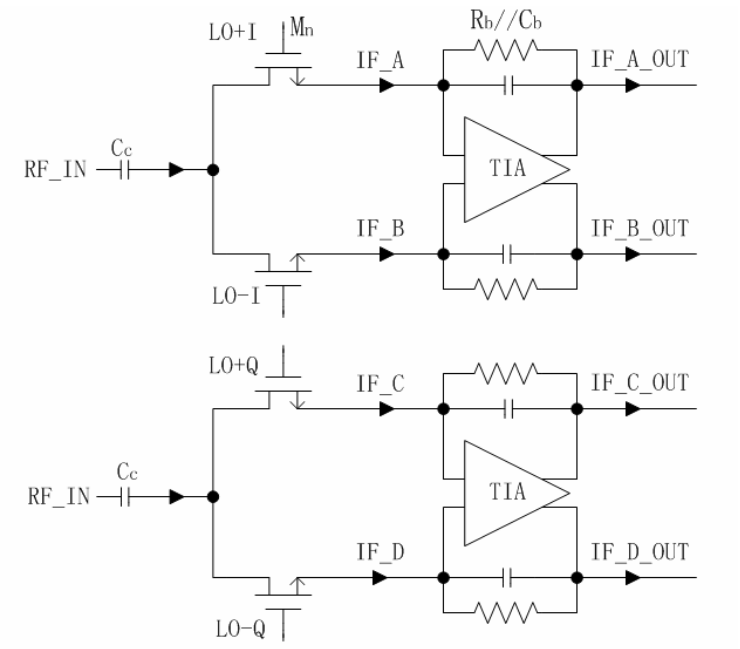
However, as shown in Figure 3.16, since there is no DC current in the switch transistors of the passive mixer because it was block by the AC coupling capacitor C_C, the LO feed-through to the output of the mixer is mainly from the leakage of the parasitic capacitance of the switching transistor and is much smaller than that of its Gilbert counterpart. In order for simplification, the single-to-differential converter is removed and single-ended RF signal is directly sent to the input of the passive mixer while the other end of the input is connected to ground through a AC coupling capacitor [64] as shown in Figure 3.24.



3.24 Double-Balanced Passive Mixer Design with Single-Ended Input

Still since there is no DC current through the switching transistor, the LO feed-through to output of each switch transistor is much smaller than it active counterpart, such as Gilbert mixer or active single-balanced mixer. And since the architecture of this receiver design is a low-IF topology, the IF frequency is 1MHz, which is much lower than the LO frequency, 199MHz, the small LO feed-through is very easy to be attenuated by a low-pass filter even if it is not cancelled by a double-balanced mixer topology. Therefore, still in order for simplification, single-ended topology of passive mixer as shown in Figure 3.25 is still suitable for this design.

However, comparing Figure 3.24 with Figure 3.25, we can find that there are only 4 more transistors in the double-balanced topology than in the single-balanced topology. Therefore, either one of these two topologies is suitable for this design.



3.25 Single-Balanced Passive Mixer Design with Single-Ended Input

The noise figure and conversion gain simulation results are shown in Figure 3.26 and Figure 3.27 respectively.

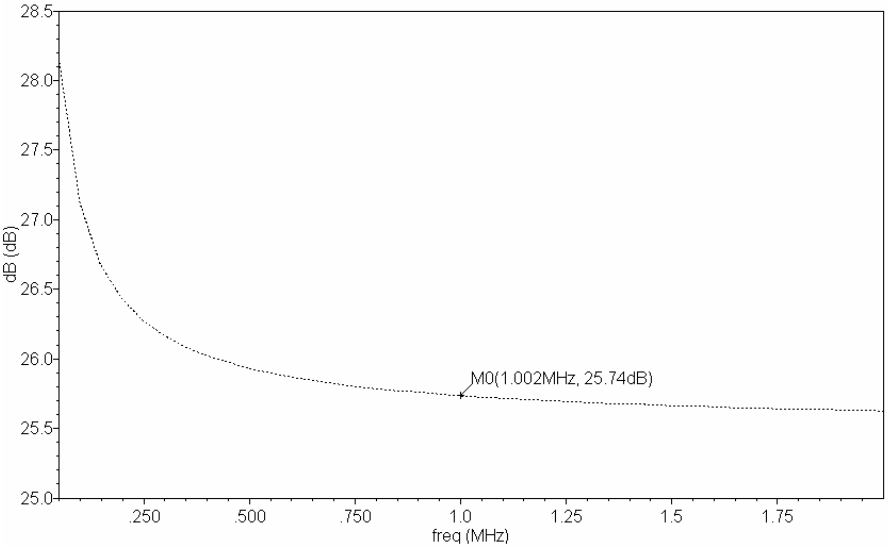


Figure 3.26 Noise Figure of Passive Mixer

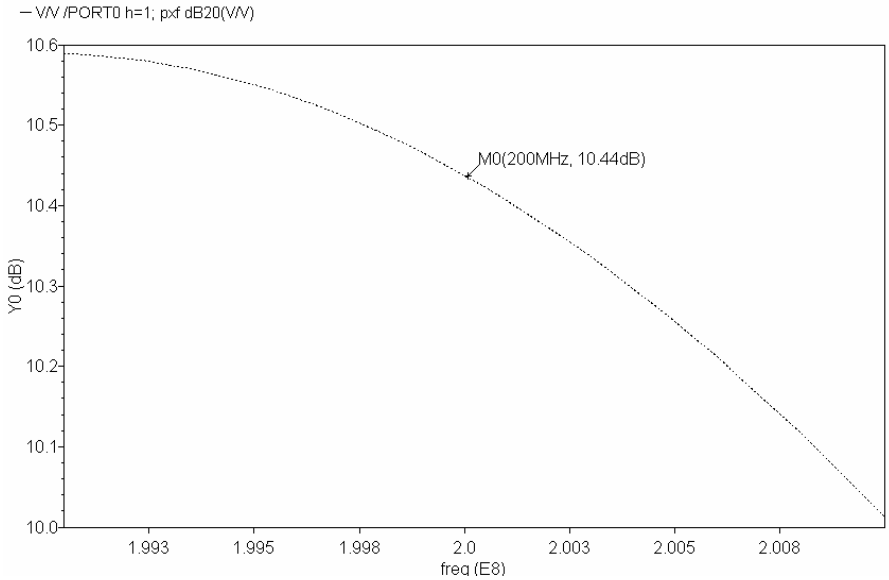


Figure 3.27 Conversion Gain of Passive Mixer

As shown in Figure 3.26, the noise figure is 25.74dB, and it can be effectively suppressed by the large gain of the LNA. As shown in Figure 3.27, the total conversion gain of the mixer (including the TIA) is 10.44dB. Since the output current signal of the switching transistors is converted by the TIA which is active, the conversion gain is positive in unit of dB.

At the output of the switching transistors, the mixed MR signal is a current signal and need to be converted into voltage signal. Therefore, trans-impedance amplifier (TIA) is designed. The TIA is an opamp which connected in negative feedback with a pair of shunt connected capacitor and resistor.

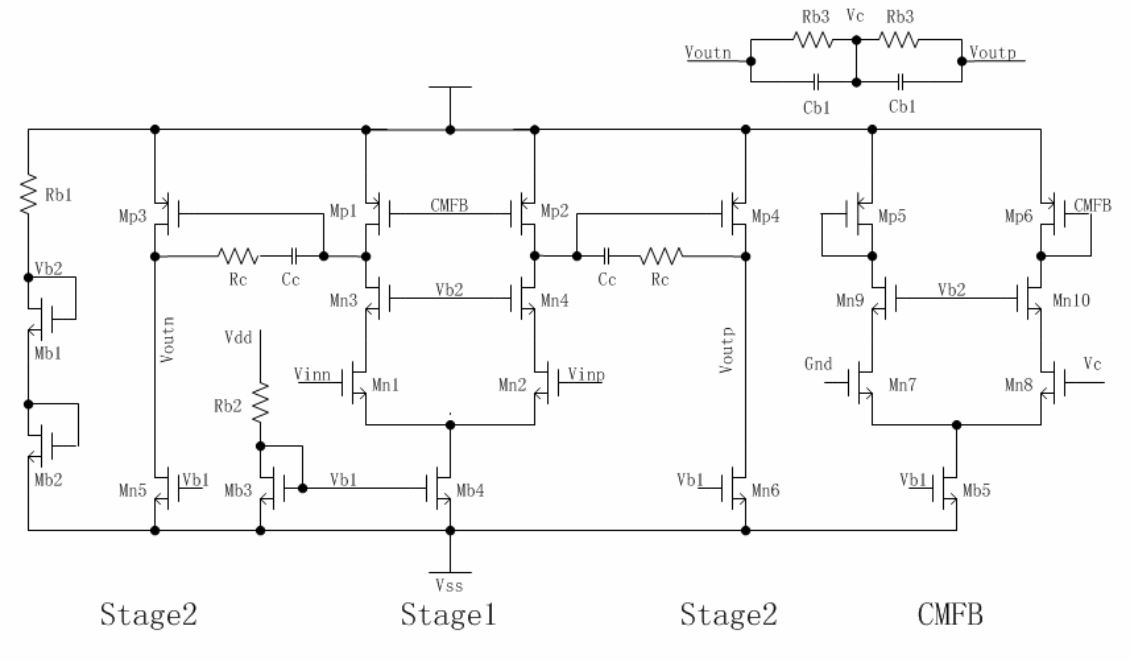


Figure 3.28 Schematic of Opamp

Figure 3.28 is the schematic of the opamp used in the TIA and the VGA/LPF. This is a two-stage differential opamp. This opamp has a gain-bandwidth (GBW) of 625MHz, and DC gain of 62dB with 73.6^0 of phase margin, while consuming 4mA current with +/-0.9V power supply.

The input stage consists of M_{n1}-M_{n4}, and M_{p1}-M_{p2}. And the NMOS transistors are connected in cascode in order to increase the output resistance of the first stage. This cascode topology increases about 6dB for the DC gain. However, it will introduce a high frequency pole and decrease the DC voltage headroom. If it is designed carefully, this high frequency pole will have very little effect on the GBW and phase margin. There is no cascode topology for the PMOS transistors because of the DC voltage headroom limitation of the TSMC 0.18μm technology with +/-0.9V power supply.

Between the first stage and the second stage, there is pole splitting compensation circuit consisting of R_C and C_C by moving the first pole to lower frequency and the second pole to higher frequency and therefore the phase margin is increased in order to improve the stability of the opamp. This will introduce a left hand plane (LHP) zero if R_C is large enough and we can cancel the second pole (the pole at the output of the first stage) by this LHP zero by adjusting the value of R_C, and therefore the GBW and phase margin are improved.

Since flicker noise is important in the design, and the flicker noise is decreased by increasing transistor size, therefore, the channel length is chosen to be 0.5μm instead of 0.18μm. However, the parasitic capacitance is increased by increasing the transistor size and the frequency of the high frequency pole is then decreased. Therefore trade-off

exists. The flicker noise is possible to be reduced by using PMOS as input transistors (transconductors), however, since PMOS transistor has lower mobility and the DC gain will therefore be decreased. In order for verifying this analysis, an opamp using PMOS transistors as input transistors was designed by the author, and after comparing with the opamp using NMOS transistors as input transistors, the author did not see obviously improvement of flicker noise while the DC gain decreased because of the smaller mobility of the PMOS transistors. Therefore, NMOS is selected by the author as the input transistors of the opamp. The DC working points (DC voltages of each net) are controlled the common mode feedback (CMFB) circuit consisting of M_{n7}-M_{n10}, M_{p5}-M_{p6}, and M_{b5}. In the CMFB circuit, the DC current of the "left arm" consisting of M_{n7}, M_{n9} and M_{p5} is a fixed value since V_{b2} is a fixed value because it is determined by R_{b1} and the diode connected transistors of M_{b1}, M_{b2}. The DC current of M_{b5} is also a fixed value because it is fixed by the current mirror consisting of M_{b4} and M_{b6}. Therefore the DC current of the "right arm" of the CMFB circuits consisting of M_{n8}, M_{n10} and M_{p6} is fixed. The Gate of M_{n8} senses the common mode voltage V_C of the output differential signals V_{outp} and V_{outn}, and compares it with the M_{n7} gate voltage which is 0V because the gate of M_{n7} is connected to ground. If V_C is higher than 0V, the drain voltage of M_{n8} decreases and then the voltage of CMFB decreases, that is, the gate voltage of M_{p1} and M_{p2} decreases, this causes the drain voltage of M_{p1} and M_{p2} increasing, that is, causes the gate voltage of M_{p3} and M_{p4} increasing, therefore the DC voltage of V_{outp} and V_{outn} decrease until it reaches 0V. Vise Versa. Therefore, the output common voltage is 0V.

In the layout of the opamp, M_{n1} and M_{n2}, M_{n3} and M_{n4}, M_{p1} and M_{p2} as well as the metal connections have to be very well matched and balanced because even a little unmatch and unbalance will cause both of the DC output voltages deviating from the common mode voltage. One goes to positive and the other goes to negative.

The simulation results are shown in Figure 3.29-Figure 3.31. In order for summarization, the values of the simulation results are listed in Table 3.2.

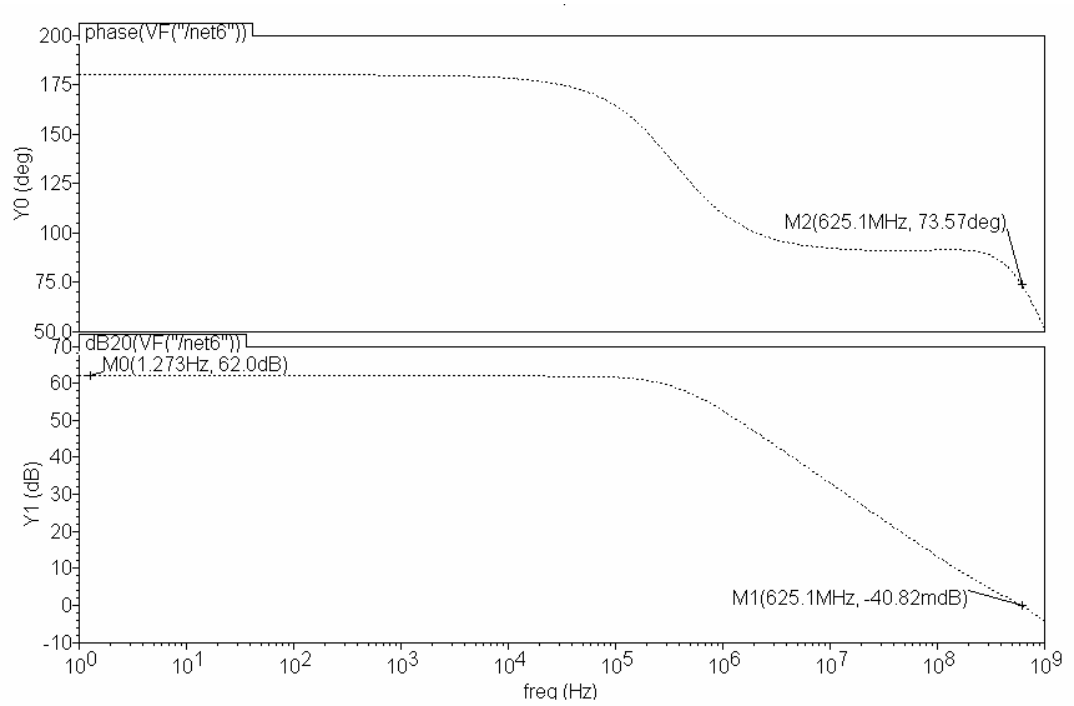


Figure 3.29 AC Simulation Results of Opamp

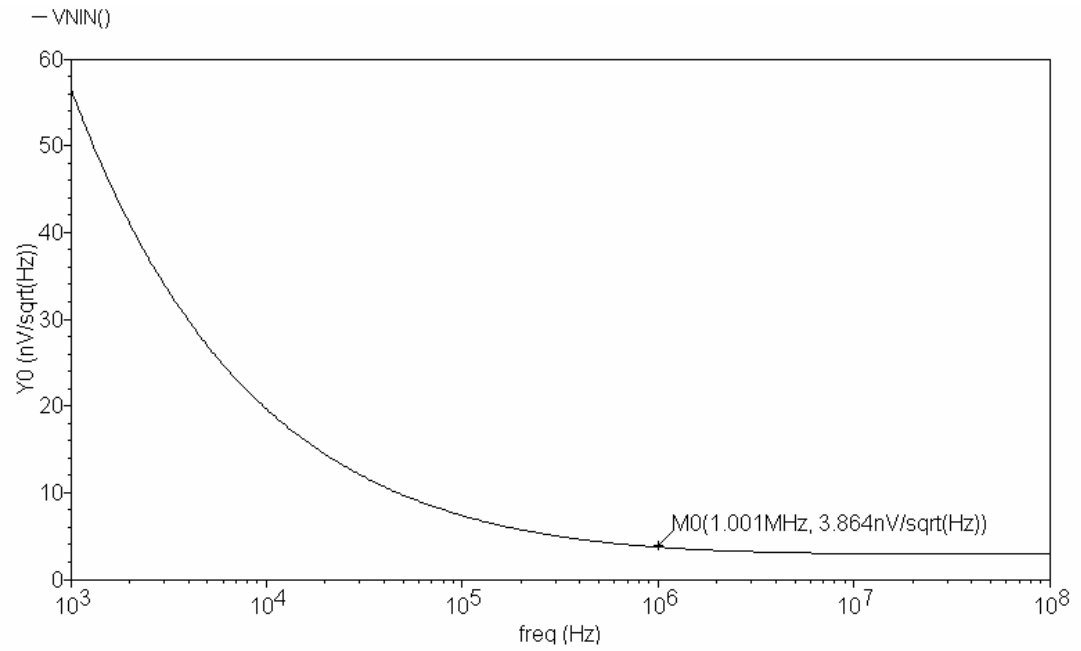


Figure 3.30 Input Referred Equivalent Noise of Opamp

signal	OP("/V0" "??")
i	-4.44281m
pwr	-3.99853m
v	900m
signal	OP("/V1" "??")
i	-4.44281m
pwr	-3.99853m
v	900m

Figure 3.31 Power Consumption of Opamp

Figure 3.29 is the AC simulation results. The AC simulation results show that the DC gain of the opamp is 62dB, and the Gain Bandwidth (GBW) is 625MHz while the Phase Margin is 73.6^0.

Figure 3.30 is the input referred equivalent noise simulation result. It shows that the input referred equivalent noise is 3.9nV/sqrt(Hz), and the noise corner is at about 47kHz.

Figure 3.31 shows that the opamp consumes 8mW of power under +/-0.9V supply.

Table 3.2 Summary of Opamp Simulation Results

Specification	Value
DC Gain	62dB
Gain Bandwidth	625MHz
Phase Margin	73.6^0
Positive Slew Rate	615V/μS
Negative Slew Rate	626V/μS
Input Referred Noise at 1MHz	3.9nV/sqrt(Hz)
Flicker Noise Corner	47kHz
Power Consumption	8mW

3.3 Quadrature Generator and Polyphase Filter Design

As shown in Figure 2.11 and Figure 2.12, the quadrature generator and the polyphase filter have the same topology. And for the reason of wide-band application, both use multi-stage. In the circuit design using TSMC 0.18μm technology, the quadrature generator uses the same schematic shown in Figure 2.11, and is redrawn in Figure 3.32 in the purpose of convenience. For the polyphase filter design, the IF

frequency is 1MHz, which is much lower than the RF frequency, therefore the sizes of the resisters and capacitors are much larger than those of the quadrature generator. In order to reduce the consumption of chip area, the polyphase filter uses the topology of two-stage instead of three-stage as shown in Figure 3.33.

The selection of the resistance and capacitance of values of both circuit are discussed in chapter II. The specific values of the resistance and capacitance are listed in Table 3.3 and Table 3.4.

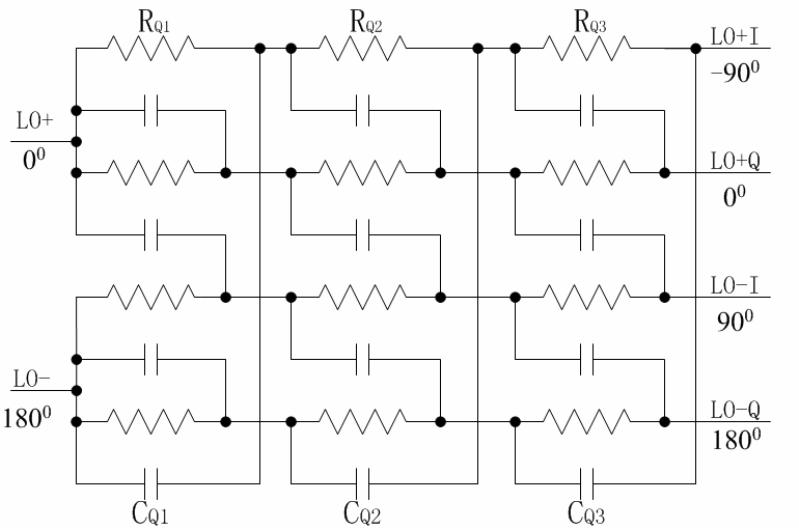


Figure 3.32 Schematic of Wide-Band Quadrature Generator

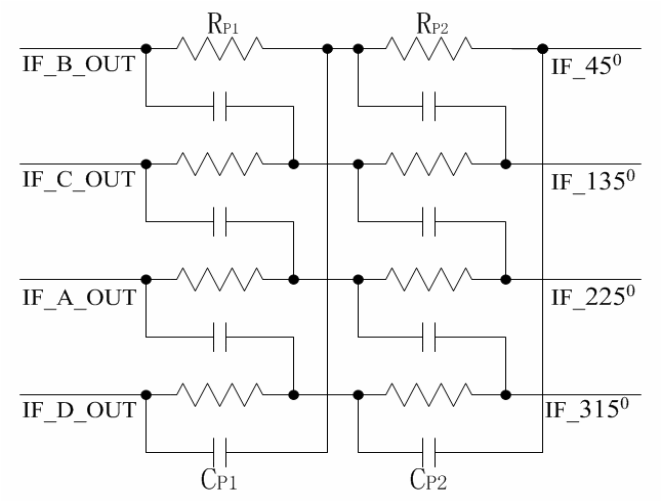


Figure 3.33 Schematic of Wide-Band Polyphase Filter

Table 3.3 Quadrature Generator Design Parameters

Parameter	Value
R_{Q1}	561.8Ω
R_{Q2}	835.4Ω
R_{Q3}	1309.8Ω
C_{Q1}, C_{Q2}, C_{Q3}	0.952pF

Table 3.4 Polyphase Filter Design Parameters

Parameter	Value
R_{P1}	56kΩ
R_{P2}	112kΩ
C_{P1}, C_{P2}	1.9pF

3.4 Buffer Design

As shown in Figure 2.23, after the MR signal is down-converted and goes pass the TIA/LPF and the polyphase filter, a buffer is placed between the polyphase filter and the VGA/LPF. The buffer is design as a simple differential amplifier shown as Figure 3.34.

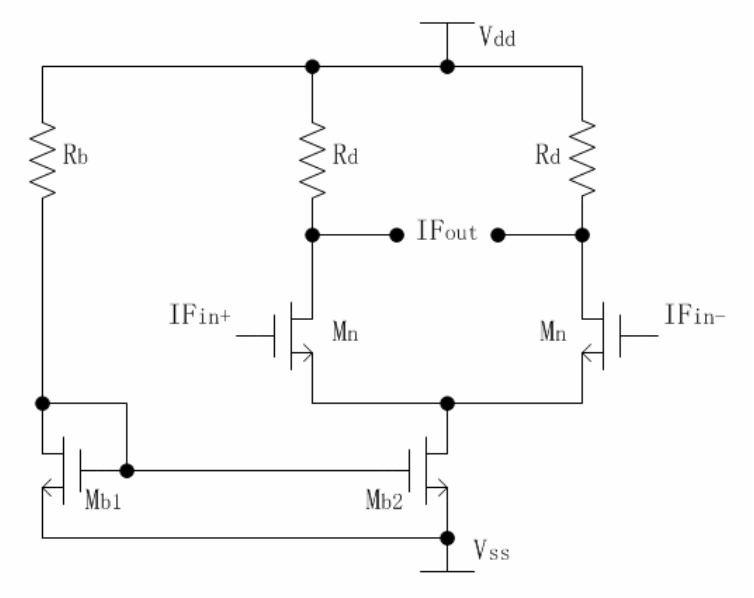


Figure 3.34 Schematic of Buffer

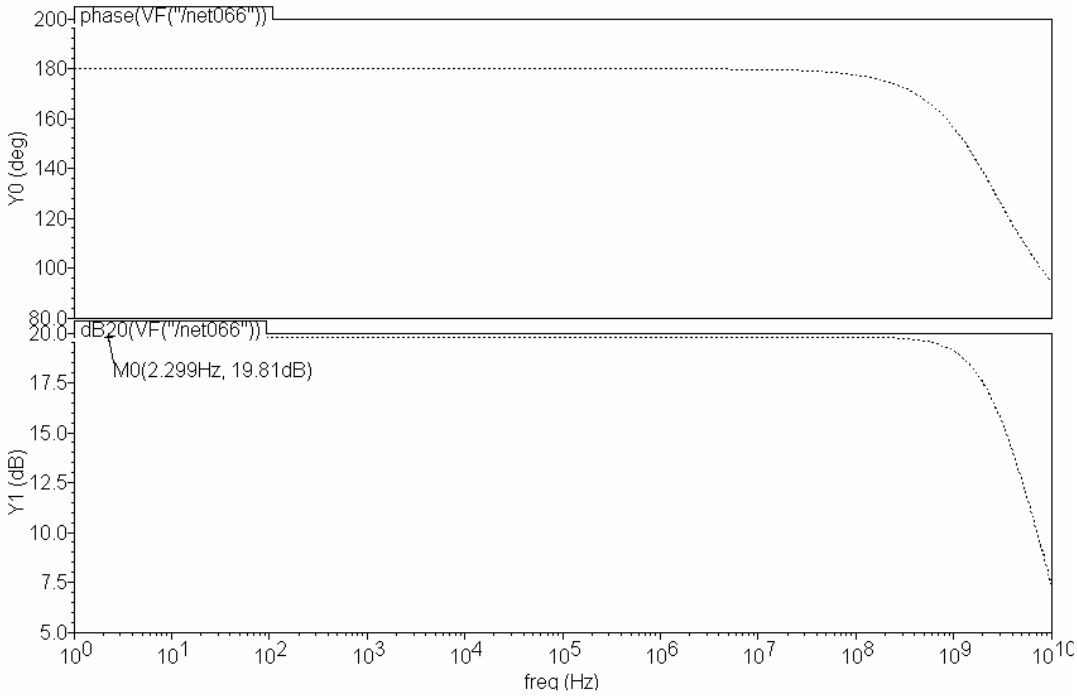


Figure 3.35 AC Simulation Results of Buffer

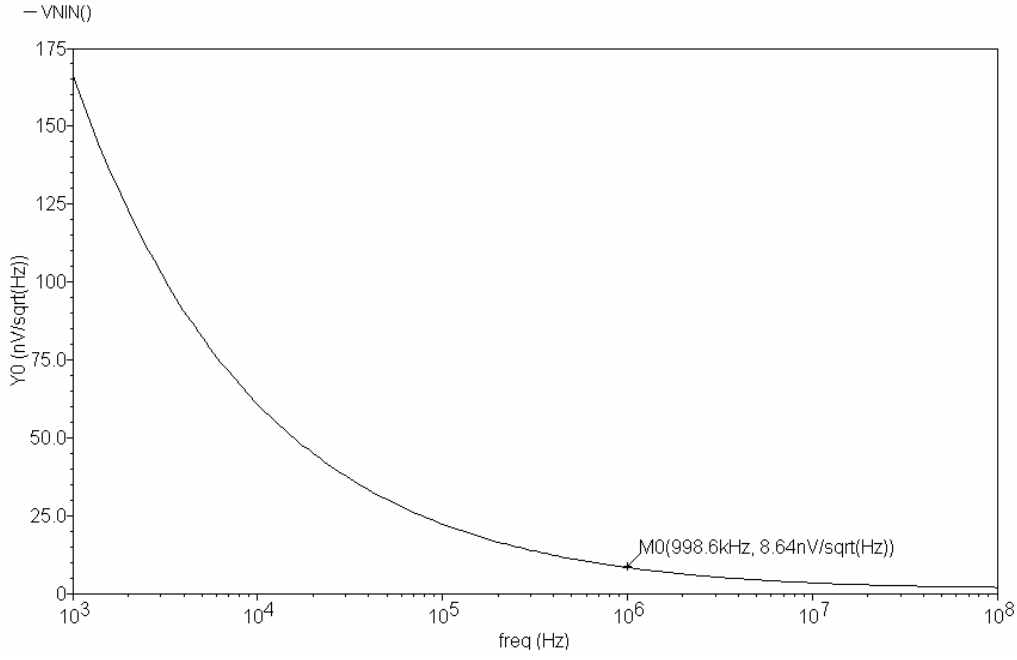


Figure 3.36 Input Referred Equivalent Noise of Buffer

As shown in Figure 3.35, the buffer has a voltage gain of 19.84dB. And since the buffer is a single stage amplifier, the bandwidth is very large and it is stable. As shown in Figure 3.36, the input referred equivalent noise is 8.64nV/sqrt(Hz), and its noise corner is about 50kHz. The simulation results are summarized in Table 3.5.

Table 3.5 Summary of Buffer Simulation Results

Specification	Value
DC Gain	19.8dB
Input Referred Noise at 1MHz	8.64nV/sqrt(Hz)
Flicker Noise Corner	50kHz
Power Consumption	2.5mW

3.5 VGA/LPF Design

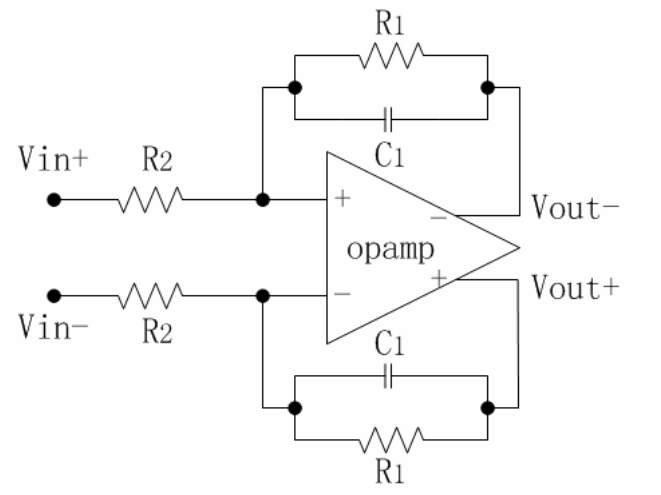


Figure 3.37 VGA/LPF

The VGA/LPF uses the same opamp as the TIA and connected in negative feed back as shown in Figure 3.37. R_2 is out-of-chip and the gain of the VGA varies according to the variation of the resistance of R_2. The feedback circuit consists of a shunt RC pair of R_1 and C_1. Therefore the VGA is also a first-order active filter which is analyzed in the following.

Since the second pole of the opamp is at much higher frequency than the first pole, the transfer function of the opamp is expressed as equation 3.55.

$$A(s) = \frac{G \cdot B}{s + B} \tag{3.55}$$

where G is DC gain of the opamp, and B is the first pole of the opamp. Then the transfer function of the VGA/LPF is acquired as equation 3.56.

$$\begin{aligned} H(s) &= -\frac{a}{s+p} \times \frac{1}{1 + (1 + \frac{a}{s+p}) \times (\frac{s+B}{G \cdot B})} \\ &= -\frac{a \cdot G \cdot B}{s^2 + (G \cdot B + p + a + B)s + (p \cdot G \cdot B + (p+a) \cdot B)} \\ &= -\frac{a \cdot G \cdot B}{s^2 + (p_1 + p_2)s + p_1 \cdot p_2} \end{aligned} \tag{3.56}$$

where $a = \frac{1}{R_2 C_1}$, $p = \frac{1}{R_1 C_1}$, p_1 and p_2 are the first pole and second pole of equation 3.56. Select $p = \frac{1}{R_1 C_1} \approx 30MHz$, and $30MHz < a = \frac{1}{R_2 C_1} < 180MHz$ so that the VGA DC gain range from 0dB to 15dB.

$$2\times\sqrt{p_1\cdot p_2}=2\times\sqrt{(p\cdot G\cdot B+(p+a)\cdot B)}<<G\cdot B<G\cdot B+p+a+B=p_1+p_2,$$

we can get $p_1<<p_2$. Then $p_2\approx G\cdot B+p+a+B$ and $p_1\approx\frac{(p\cdot G\cdot B+(p+a)\cdot B}{G\cdot B+p+a+B}\approx p$.

Then, we can choose $R_1=6k\Omega$, $C_1=4.75pF$, and R_2 ranges from $1k\Omega$ to $6k\Omega$, therefore, $p_1\approx p=\frac{1}{R_1C_1}\approx 35MHz$, and $p_2\approx G\cdot B+p+a+B>700MHz$ which can be ignored because it is at very high frequency.

The following is the simulation results of the VGA/LPF. As shown in Figure 3.38, when $R_2=1k\Omega$, the DC gain is 15.5dB, and the gain at 1MHz is 15.57dB. The attenuations at 200MHz and 400MHz are 14.43dB and 17.86dB respectively. As shown in Figure 3.39, when $R_2=1k\Omega$, the DC gain is 0dB, and the gain at 1MHz is 0dB. The attenuations at 200MHz and 400MHz are 29.29dB and 32.71dB respectively.

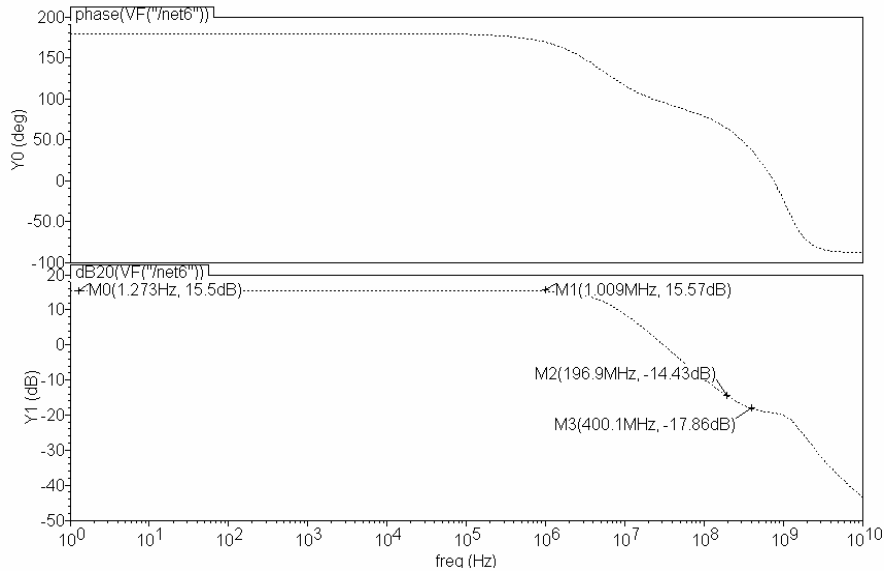


Figure 3.38 AC Simulation of VGA/LPF ($R_2=1k\Omega$)

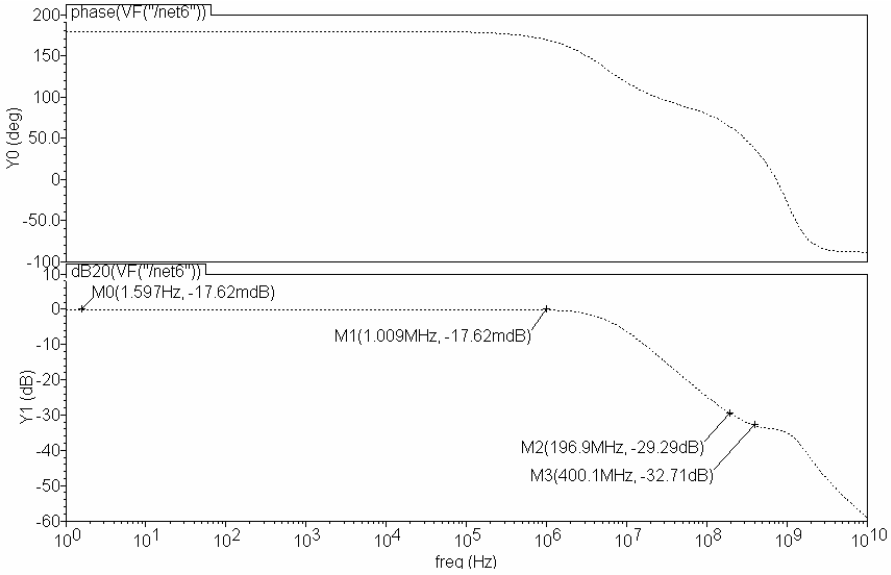


Figure 3.39 AC Simulation of VGA/LPF ($R_2 = 6k\Omega$)

3.6 Simulation and Layout of Front-End

After each block of the front-end architecture shown in Figure 2.23 was designed, the front-end was setup and simulation results were acquired.

As shown in Figure 3.40-Figure 3.43, the conversion gain varies from 81.62dB to 92.19dB. Comparing Figure 3.40 and Figure 3.41, Figure 3.42 and Figure 3.43, we can acquire that the suppression of the thermal noise at image frequency is about 31.6dB. The suppression is similar to the noise of a block with a 3dB noise figure being suppressed by a LNA with 31.6dB gain. And we can find that the suppression is efficient.

The total noise figure of the front-end is shown in Figure 3.44.

The simulation results are listed in Table 3.6. The layout of the four-channel front-end is shown in Figure 3.45. The pin definition and pin connection for testing are illustrated in Figure 3.46 and Table 3.7.

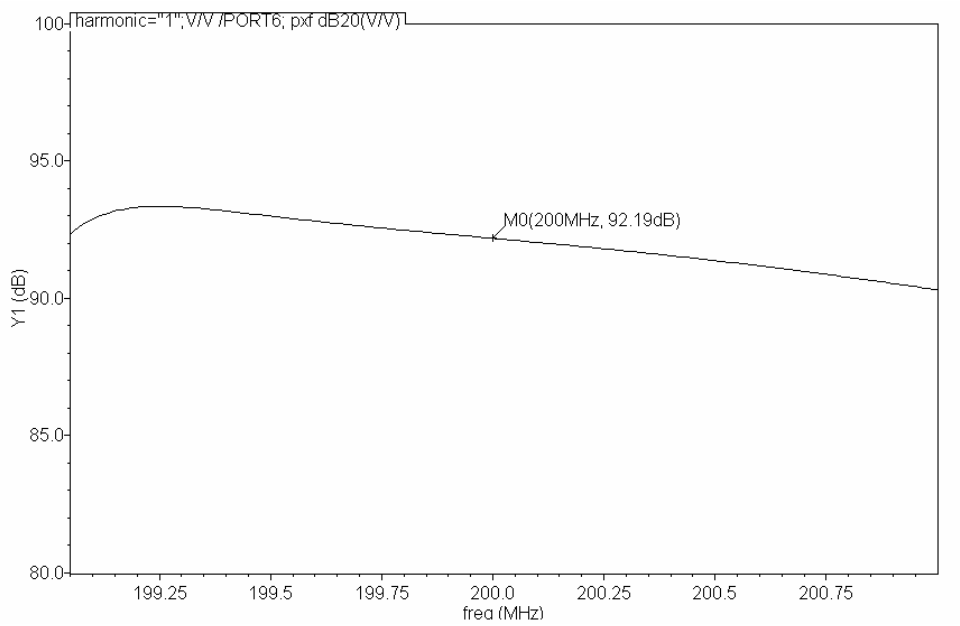


Figure 3.40 Conversion Gain of Receiver Front-End
(RF Frequency Higher than LO Frequency $R_2 = 6k\Omega$)

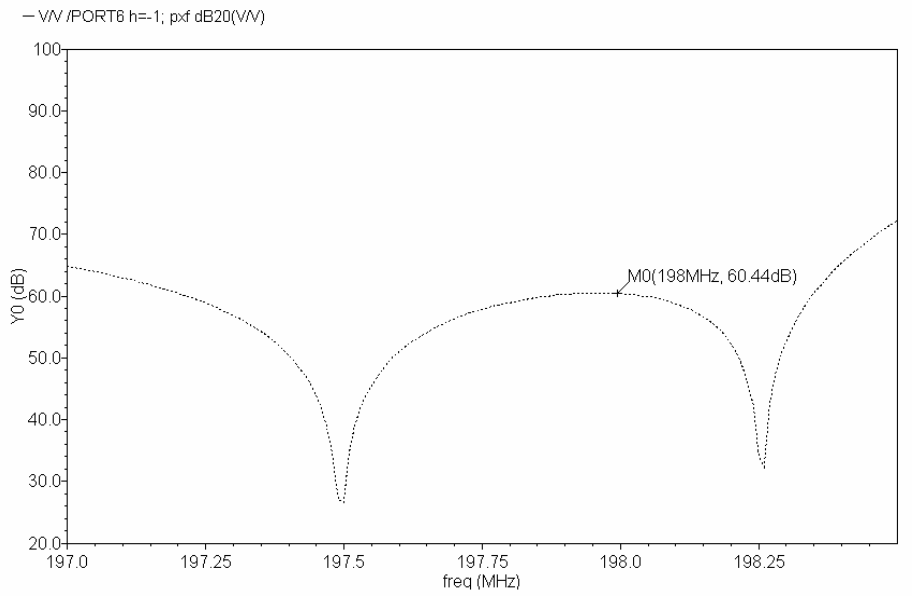


Figure 3.41 Conversion Gain of Receiver Front-End
(RF Frequency Lower than LO Frequency $R_2 = 6k\Omega$)

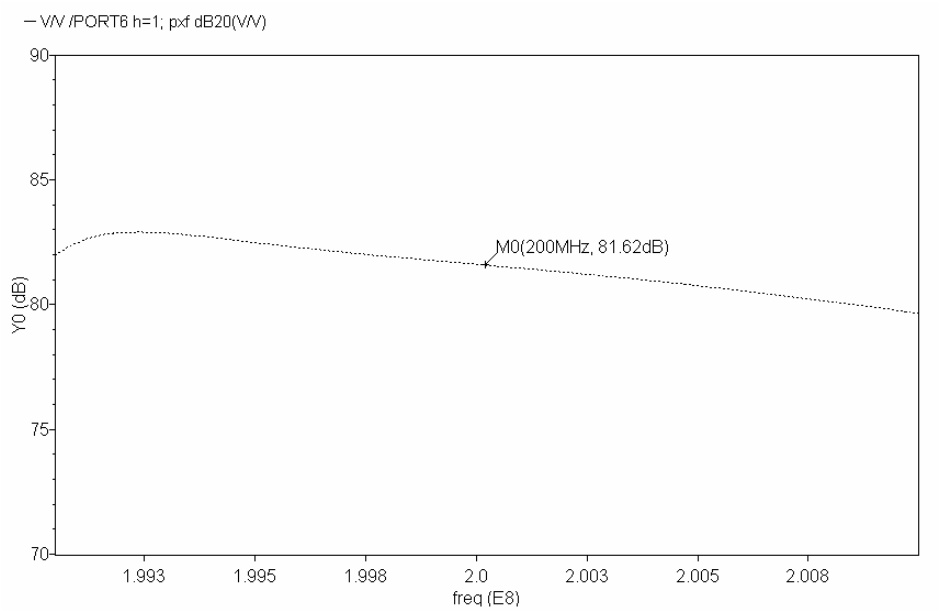


Figure 3.42 Conversion Gain of Receiver Front-End
(RF Frequency Higher than LO Frequency $R_2 = 1k\Omega$)

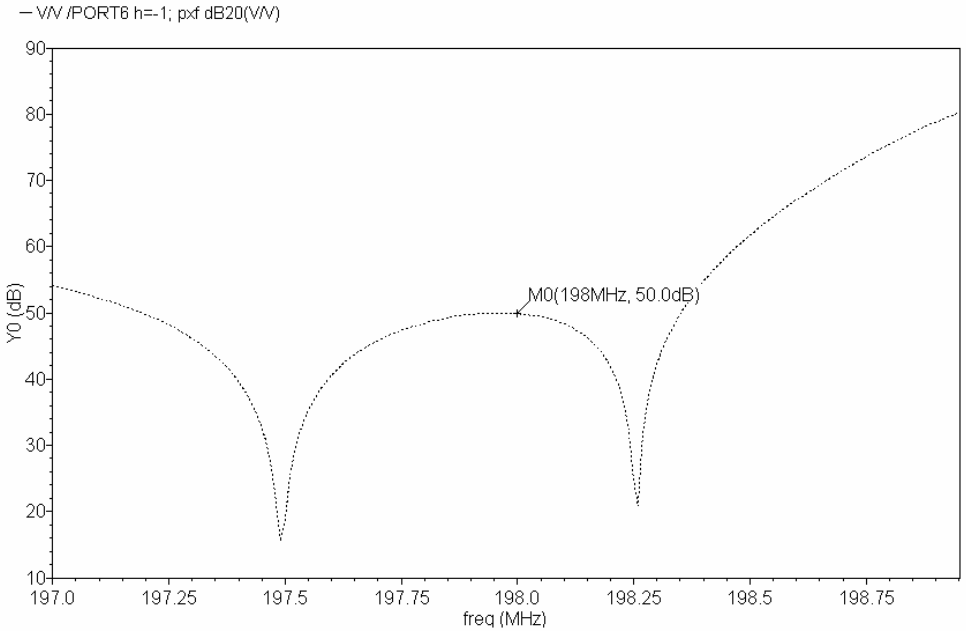


Figure 3.43 Conversion Gain of Receiver Front-End
(RF Frequency Lower than LO Frequency $R_2 = 1k\Omega$)

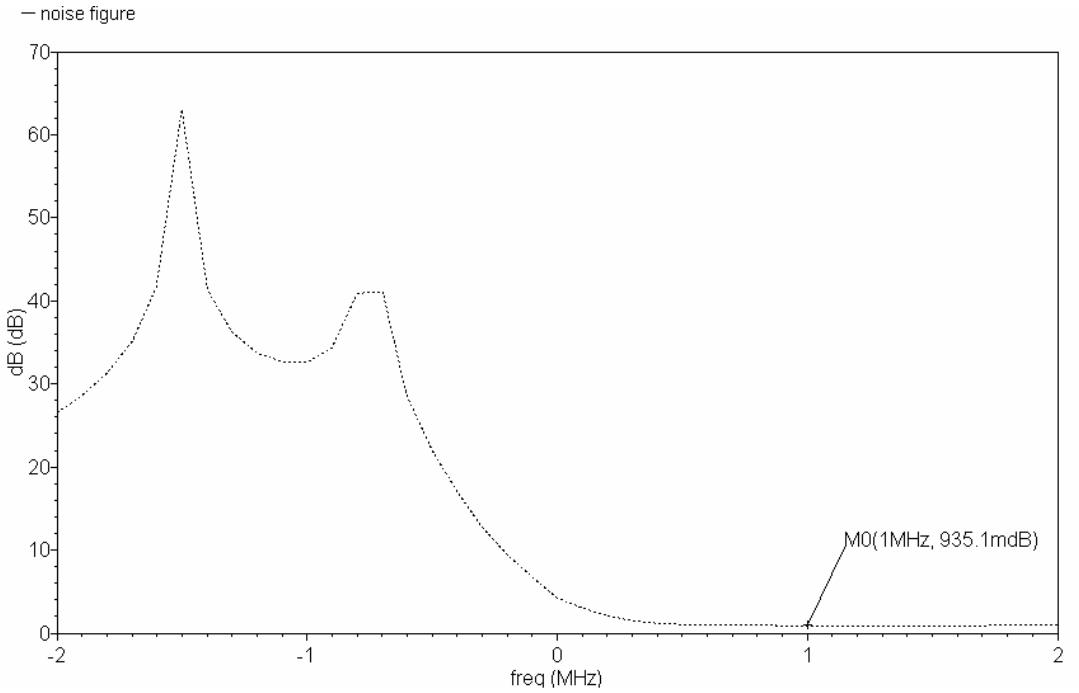


Figure 3.44 Noise Figure of Receiver Front-End

Table 3.6 Summary of Receiver Front-End Simulation Results

Specification	Value
Conversion Gain	80dB ~ 90dB
Noise Figure	0.935dB
Higher Order Harmonics	<-69.3dB (Compared with the Fundamental)
Power Consumption	30.8mW
Chip Area	6mm^2

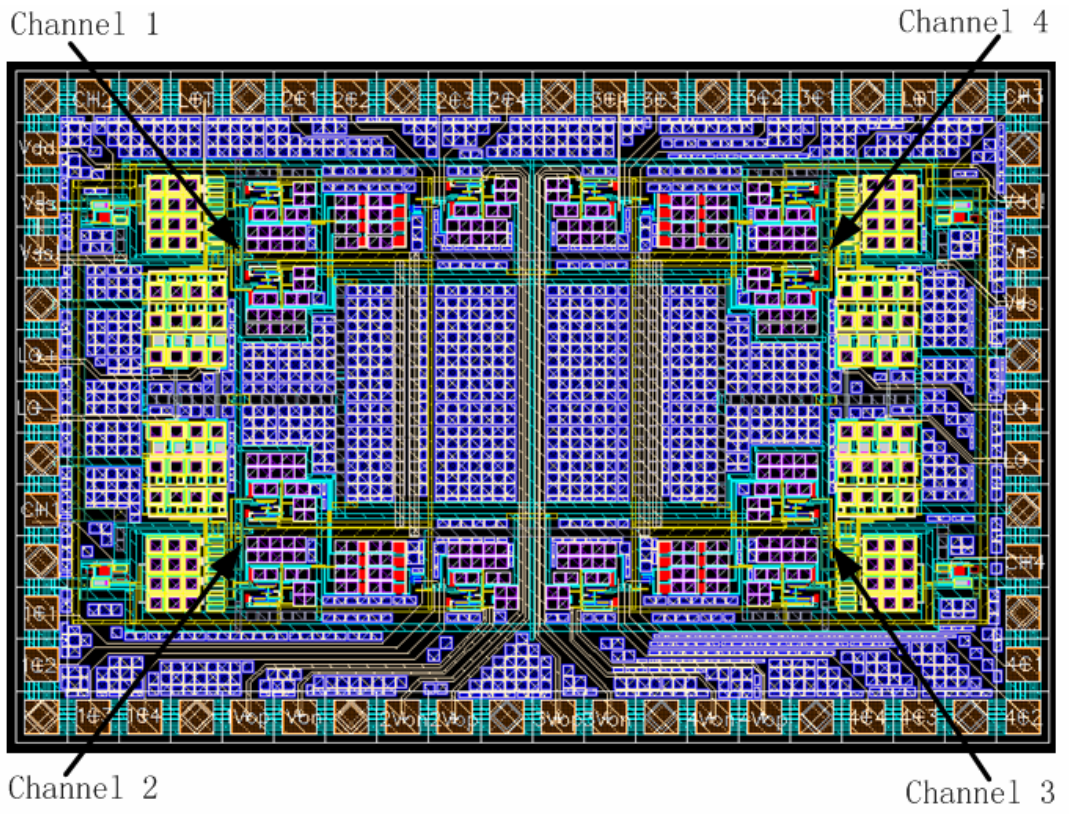


Figure 3.45 Layout of Four-Channel Receiver Front-End

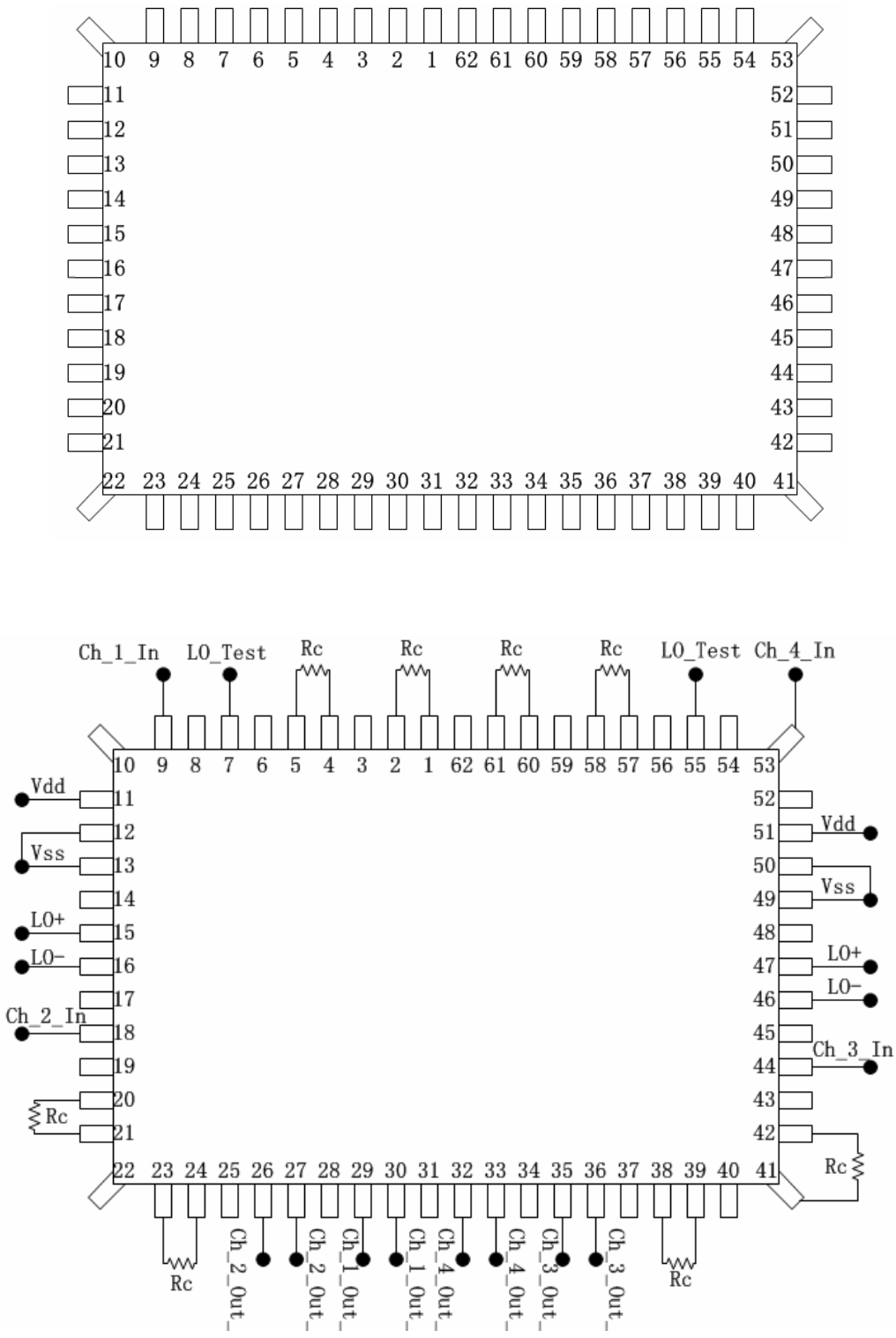


Figure 3.46 Pin Number (Upper) and Pin Connection (Lower)
of Four-Channel Receiver Front-End

As shown in Figure 3.46, R_C is the resistor controlling the gain of the receiver front-end. In the testing circuit, R_C is a fixed value resistor instead of a tunable resistor in order to reduce the board space. As the resistance of R_C ranges from 1kΩ to 6 kΩ, the gain of the receiver front-end ranges from 92.19dB to 81.64dB as illustrated in Figure 3.40 and Figure 3.42. LO_Test pin is the pin we can test the voltage of the LO signal inside the chip. All the other pins, whose connections are not shown in Figure 3.46, are ground pins. When doing testing, we can just use "via" to connect these ground pins to the ground plane on the bottom layer of the printed circuit board (PCB).

Table 3.7 Summary of Receiver Front-End Pin Definition

Pin Number	Pin Name	Description
1	1C4	Channel 1 Gain Control 4
2	1C3	Channel 1 Gain Control 3
3	GND	Ground
4	1C2	Channel 1 Gain Control 2
5	1C1	Channel 1 Gain Control 1
6	NC	No Connection
7	LOT	Testing Point of LO Signal
8	GND	Ground
9	CH1	Channel 1 Input
10	GND	Ground
11	Vdd	Positive Power Supply (+0.9V)
12	Vss	Negative Power Supply (-0.9V)
13	Vss	Negative Power Supply (-0.9V)
14	GND	Ground

Table 3.7 (Continued)

Pin Number	Pin Name	Description
15	LO+	Positive LO Input
16	LO-	Negative LO Input
17	GND	Ground
18	CH2	Channel 2 Input
19	GND	Ground
20	2C1	Channel 2 Gain Control 1
21	2C2	Channel 2 Gain Control 2
22	GND	Ground
23	2C3	Channel 2 Gain Control 3
24	2C4	Channel 2 Gain Control 4
25	GND	Ground
26	2Vop	Channel 2 Positive Output
27	2Von	Channel 2 Negative Output
28	GND	Ground
29	1Von	Channel 1 Negative Output
30	1Vop	Channel 1 Positive Output
31	GND	Ground
32	4Vop	Channel 4 Positive Output
33	4Von	Channel 2 Negative Output
34	GND	Ground
35	3Von	Channel 3 Negative Output
36	3Vop	Channel 3 Positive Output
37	GND	Ground
38	3C4	Channel 3 Gain Control 4
39	3C3	Channel 3 Gain Control 3

Table 3.7 (Continued)

Pin Number	Pin Name	Description
40	GND	Ground
41	3C2	Channel 3 Gain Control 2
42	3C1	Channel 3 Gain Control 1
43	GND	Ground
44	CH3	Channel 3 Input
45	GND	Ground
46	LO-	Negative LO Input
47	LO+	Positive LO Input
48	GND	Ground
49	Vss	Negative Power Supply (-0.9V)
50	Vss	Negative Power Supply (-0.9V)
51	Vdd	Positive Power Supply (+0.9V)
52	GND	Ground
53	CH4	Channel 4 Input
54	GND	Ground
55	LOT	Testing Point of LO Signal
56	GND	Ground
57	4C1	Channel 4 Gain Control 1
58	4C2	Channel 4 Gain Control 2
59	GND	Ground
60	4C3	Channel 4 Gain Control 3
61	4C4	Channel 4 Gain Control 4
62	GND	Ground

CHAPTER IV

TESTING ARCHITECTURES OF FOUR-CHANNEL FRONT-END IN MRI SYSTEM

As discussed in Chapter I, Parallel MRI experiment using phase coil array to increase SNR and FOV, and Parallel MRI experiment using SEA approach with narrow and long parallel planar coil array to reduce imaging time are two main research fields for Parallel MRI. Examples of the first approach reported in [6], [10], [70], [71] use phase array such as head, cardiac and spine coil array, while the SEA Parallel MRI experiment uses an array of very long and narrow parallel planar coils on a PCB [3], [8], [9]. Both types of coil arrays are explored as the target coils in the following.

4.1. Using Planar Coil Array in SEA as Target Coils

In order to explore the possibility of the idea of "digital coil array" integrating the coils, RF front-ends, and in future works, AD converters together with sample-and-hold circuit which also performs the function of multiplexing switches, on the same PCB and get digital MR signals from the output of the "digital coil array", the coil array used in [3], [8], [9] is first explored as target coil in this parallel RF front-end design.

4.1.1 Illustration of Planar Coil Array in SEA

As illustrated in Figure 4.1, 64 planar coils were etched on 10-mil thick RO3010 substrate with an overall array dimension of 13 × 8.1cm [3], [8], [9]. The individual coil footprint was 2mm (80mil) × 8.1cm with conductor tracks of 10mil in width, and a gap

of 20mil between them. The gap between adjacent coils was 10mil. Each coil was matched to 50Ω using a “Shunt C-Series C” matching circuit. A pair of single side varactors were used as the “Shunt C”, and the capacitances of the varactors were controlled by the 2 × 32 Channels DC Varactor Bias Board through the 4 × 20 Channels Ultrasonic Coaxial Cables. Between the varactors and the Ultrasonic Coaxial Cables, a tunable capacitor was used as the “Series C”, and a 10kΩ resistor was solder underneath the tunable capacitor in order to avoid the tunable capacitor acting as a DC blocker and therefore allow the DC controlling voltage going from the Ultrasonic Coaxial Cables, through the resistor, and then to the varactor. Between the center conductor track of the coil and the varactors, a 1000pF capacitor was used as DC blocker which blocked the varactor DC controlling voltage from going through the coil to the ground. At the far end, the 4 × 20 Channels Ultrasonic Coaxial Cables were connected to a Bias Insertion Board which connected the DC Varactor Bias Board for tuning the capacitance of the varactors as mentioned above through high resistance Carbon Wires. The Bias Insertion Board still contained DC block and sent the MR signal to the preamp.

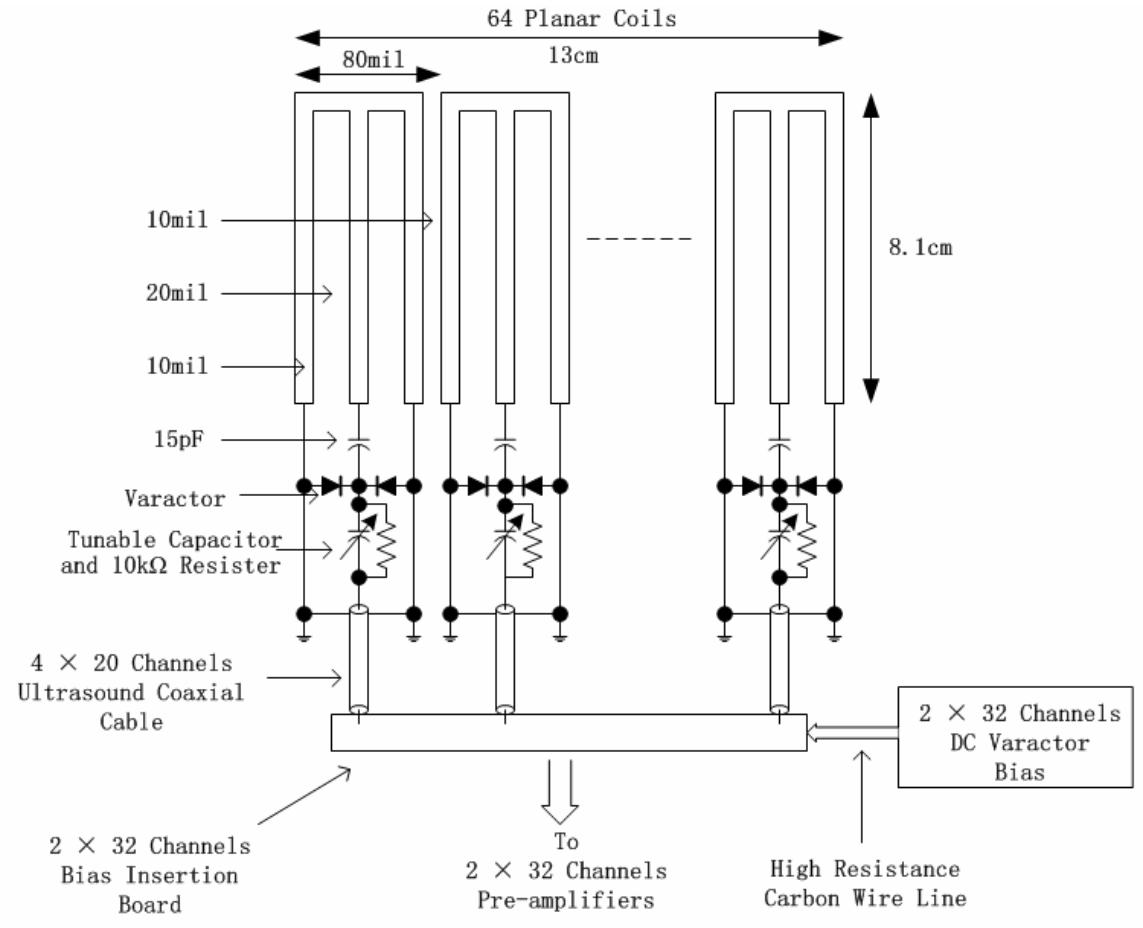


Figure 4.1 Planar Coil Array Proposed in SEA

4.1.2 Proposed Testing Architecture Using Planar Coil Array

In this work, a four-channel CMOS RF front-end was designed on a single silicon substrate, and will be mounted at the output of the coil array. No micro strip transmission line (MSL) is needed between the coil array and the RF front-end. Therefore, no power reflection problem exists and 50Ω matching circuit is not necessary.

However, a common source LNA was explored and designed in Chapter III as the preamplifier of the RF front-end. This LNA needs to have a certain value of signal

source impedance in order to acquire as small noise figure as possible. Although the output impedance of the coil does not need to be matched to 50Ω, it still needs to be matched to a certain value by shunt connected a C_{ex} about 11pF at the output of the coil as illustrated in Figure 3.16, and therefore the matching circuit of the coil is proposed and illustrated in Figure 4.2, Still another architecture is proposed and illustrated in Figure 4.3.

As illustrated in Figure 4.2, the 2 × 32 Channels DC Varactor Bais Board, High Resistance Carbon Wire Line, 2 × 32 Channels Bias Insertion Board, 4 × 20 Channels Ultrasonic Coaxial Cables are reserved only for tuning the varactors. Moreover, the 1000pF DC block capacitor is also reserved to block the varactor DC tuning voltage from leaking through the coil to the ground. In this proposed architecture, modifications are made as the following. At the output of coil, only a pair of varactors is used as C_{ex} to tune the output impedance of the coil in order to minimize the noise figure of the LNA. The Ultrasonic Coaxial Cables are no longer shared by the varactor DC control signals and the RF signals. They are only used to transmit the DC tuning voltage in order to tune the capacitance of the varactor. At the input of each Ultrasonic Coaxial Cable, a 100kΩ resistor is used as RF block to minimize the MR signal from leaking to the Ultrasonic Coaxial Cable. Since the capacitance of C_{ex} is around 11pF, if the capacitance range of the varactor is lower than this value, a fixed value non-magnetic capacitor can be mounted underneath the varactor, so that the value of 11pF is covered in the capacitance range of the varactor.

Another proposed architecture is shown in Figure 4.3. In this topology, the varactor is replaced by a fixed value nonmagnetic capacitance mounted in parallel with a tunable capacitor with tuning range of 1pF to 5pF. Since the varactor is no longer used in the architecture, the 2 × 32 Channels DC Varactor Bais Board, High Resistance Carbon Wire Line, 2 × 32 Channels Bias Insertion Board, 4 × 20 Channels Ultrasonic Coaxial Cables are discarded. Therefore, this architecture is simplified as shown in Figure 4.3.

In both proposed architectures, MR signal from the MR coil of each channel is sent to the front-end where the MR signal is amplified, down-converted to 1MHz, filtered, and amplified. Then the MR signals of each channel are sampled by the multiplexing switches in a sequence of time interleaves, and each signal is placed in a certain time slot among the sequence by means of time domain multiplexing. Finally, the multiplexed MR signals are sent by coaxial cable to the digitizer. Still five more cables are used for DC power supply (not shown in Figure 4.2 and Figure 4.3 in order for simplification), LO+, LO-, and IF Switch Control Clock respectively.

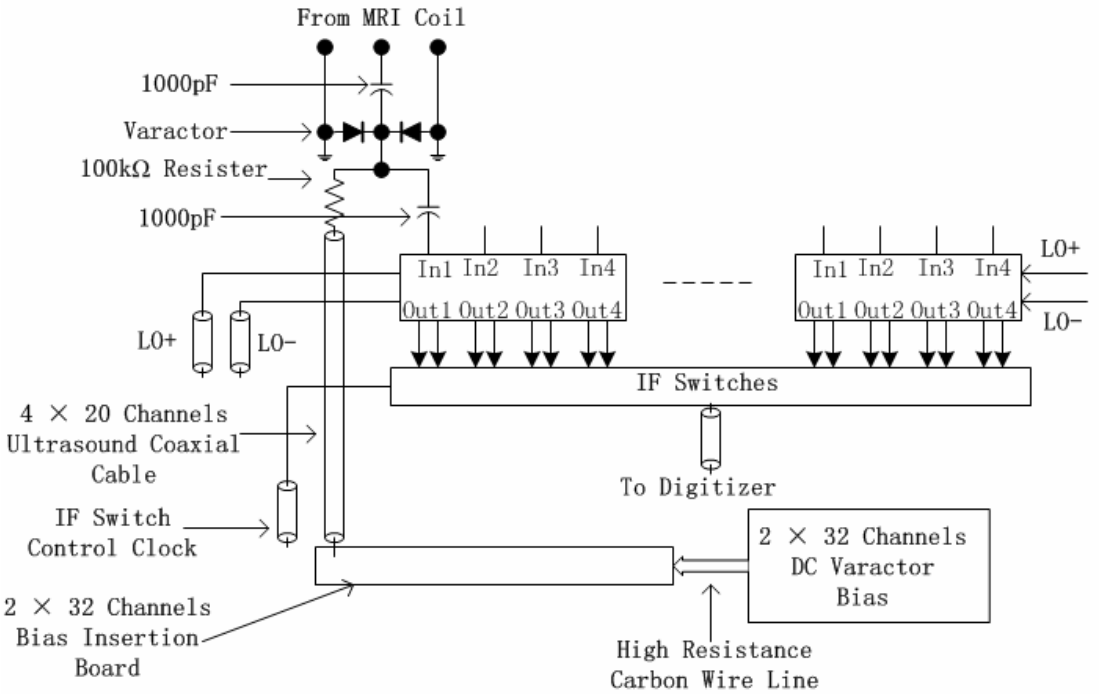


Figure 4.2 Proposed Architecture of Parallel RF Front-End Using Parallel Planar Coil Array (Using Varactor as C_{ex})

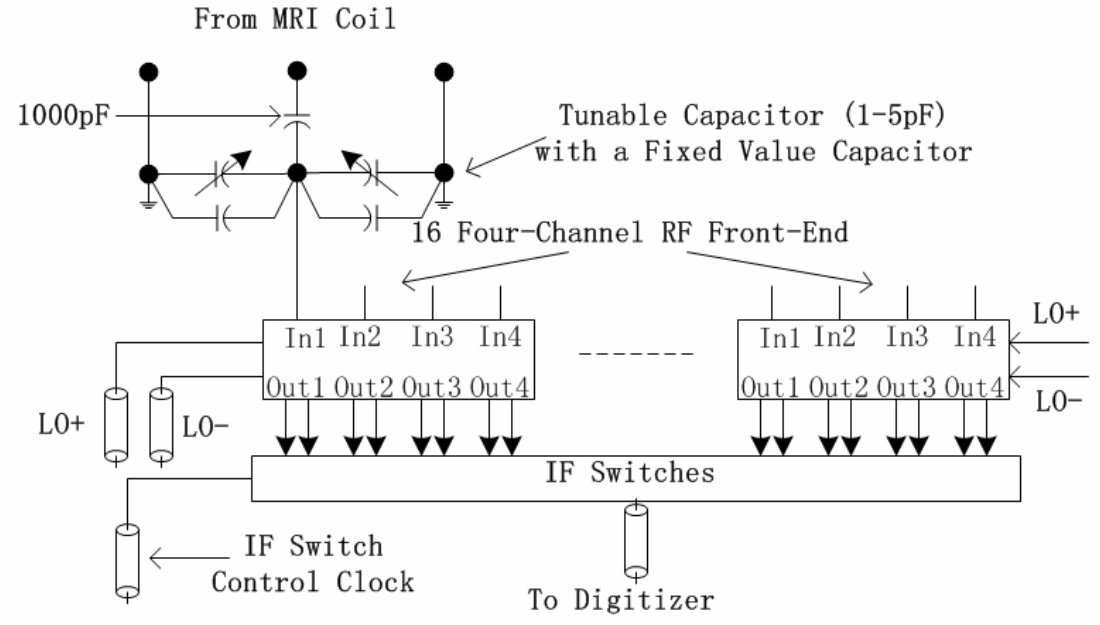


Figure 4.3 Proposed Architecture of Parallel RF Front-End Using Parallel Planar Coil Array (Using Tunable Capacitor as C_{ex})

4.1.3 Specifications of the Parallel MRI Receiver System Using the Proposed Architecture

The specifications of the parallel MRI receiver need to be specified in order to evaluate the image quality and to explore the limitation of channel number, so that we can multiplex as many channels as possible without degrading the image quality.

4.1.3.1 Carrier Frequency, Phantom, and Bandwidth

The carrier frequency of MR signal is the Larmor frequency, which is calculated by the following Larmor equation.

$$f = \frac{\gamma B_0}{2\pi} \tag{4.1}$$

Where γ is the gyromagnetic ratio, which is $2\pi \times 42.5759 rad/Tesla$ for ^{1}H, and B_0 is the static magnet field of the main magnet. The target MRI system is the 4.7T/33cm Bruker/GE Omega System in Magnetic Resonance Systems Lab (MRSL) in Texas A&M University, and therefore the Larmor frequency, that is, the carrier frequency is 200.228MHz.

In order for comparison, the same spin echo pulse sequence and the same phantom as proposed in [3], [9] are used in the analysis of the proposed receiver architectures. The spin echo pulse sequence is a standard one, with resolution 256 × 256, TR 250msec, TE 13msec, 1 average, FOV 14cm, spectral bandwidth 50kHz [3], [9]. The phantom is a 13-cm-diameter dish which contains spiraled compartments filled with distilled water, 1g/liter copper sulfate, and 0.5g/liter copper sulfate alternatively [3], [9].

And the phantom is placed on the coronal plane for imaging. The slice selection gradient is orthogonal to the coronal plane, and the slice thickness is 2mm, centered 4mm above the plane [3], [9]. The frequency encoding gradient is along the direction of the main magnet field.

4.1.3.2 Signal to Noise Ratio

In this part, the SNR of the MR signal at the output of the each coil is calculated by

$$SNR = 20 \times \log(\frac{Signal\_Voltage}{Noise\_Voltage}) \tag{4.2}$$

The signal voltage is the maximum value of the free-induction decay (FID) voltage and is calculated according to equation [3], [8], [9], [72].

$$V_{MAX} = \omega \times \Delta v \times M_{xy} \times \frac{B_1}{I} \tag{4.3}$$

where Δv is the volume of the phantom. Due to the characteristic of high localized field sensitivity, Δv is the phantom section which is exactly on top of a certain coil and exactly the same size of the coil as shown in Figure 4.4. M_{xy} is the net magnetization of this section of the phantom. B_1 is ratio of field of the coil which will be calculated in the following, while I is the current on the center trace of the coil. The noise voltage is acquired by calculating $\sqrt{4kTR\Delta f}$. The specific calculation steps are shown in the following.

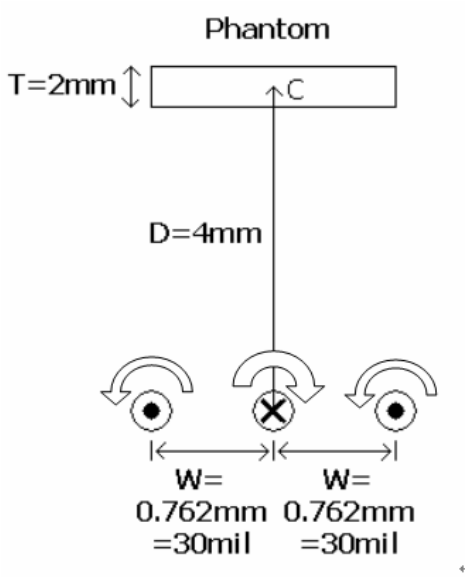


Figure 4.4 Cross Section View of a Coil; Field Produced by Each Wire;
And the Section of the Phantom on Its Top

(1). Calculate $\frac{B_1}{I}$ of the Coil

In this calculation, since the distance between the phantom and the coil is much larger than the width of the coil, the field in the phantom shown in Figure 4.4 is approximated to be uniform, and approximately equals to the field at the center of the phantom. According to the Biot-Savart expression, we can get $\frac{B_1}{I}$ in the center of the phantom as the following.

$$\frac{B_1}{I} = \frac{\mu_0}{2\pi}\left(\frac{\sin(\phi)}{D} - 2\times\frac{\frac{1}{2}\sin(\phi_1)}{\sqrt{D^2+W^2}}\right) \qquad 4.4$$

where ϕ and ϕ_1 are shown in Figure 4.5. And $\phi_1 = \tan^{-1}\left(\frac{D}{W}\right)$.

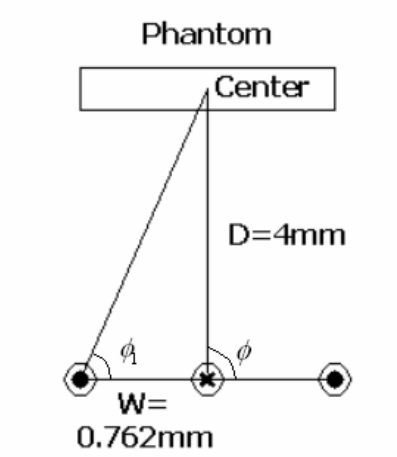


Figure 4.5 ϕ and ϕ_1 in $\frac{B_1}{I}$ Calculation

Therefore,
$$\frac{B_1}{I} = \frac{4\pi \times 10^{-7}(\frac{H}{m})}{2\pi}(\frac{\sin(90^0)}{4mm} - 2 \times \frac{\frac{1}{2}\sin(\phi_1)}{\sqrt{(4mm)^2 + (0.762mm)^2}}) \quad (4.5)$$
$$= \frac{4\pi \times 10^{-7}(\frac{H}{m})}{2\pi} \times \frac{8.75}{m} = 1.75\mu T / A$$

(2). Calculate the Maximum Signal Voltage

$$V_{MAX} = \omega \times \Delta v \times M_{xy} \times B_1$$

$$M_{xy} = \frac{N\gamma^2\hbar^2 B_0}{4kT} = 1.51 \times 10^{-11} \frac{J}{T \times mm^3}$$

$$\Delta v = 81mm \times 2mm \times 2mm = 324mm^3$$

$$\omega = 2\pi \times 4.7T \times 42.57 \times 10^6 (\frac{rad}{S \times T}) = 1258 \times 10^6 (\frac{rad}{S})$$

Then,

$$V_{MAX} = \omega \times \Delta v \times M_{xy} \times B_1$$
$$= 1258 \times 10^6 (\frac{rad}{S}) \times 324(mm^3) \times 1.51 \times 10^{-11} (\frac{J}{T \times mm^3}) \times 1.75(\frac{\mu T}{A}) = 10.8 \mu V$$

(3). Calculate the Thermal Noise Voltage

$$V_n = \sqrt{4kTR\Delta f} = \sqrt{4 \times 1.38 \times 10^{-23} (\frac{J}{K}) \times 300K \times 1.7(Ohms) \times 10^4 (Hz)} = 3.76 \times 10^{-2} \mu V$$

(4). SNR

$$SNR = \frac{10.8 \mu V}{3.76 \times 10^{-2} \mu V} = 287 \text{ or } SNR = 20 \times \log(\frac{1.84 \mu V}{3.76 \times 10^{-2} \mu V}) = 49 dB$$

Discussion: The SNR in MRI experiment using planar coil is smaller than that using multi-turn solenoid coil because the $\frac{B_1}{I}$ of planar coil is much smaller than that of multi-turn solenoid coil.

4.1.3.3 Bits of the Digitizer

The SNR of the digitizer MUST not be smaller than that of the signal

$$SNR_{ADC} = 6.02m + 1.76dB = 49dB$$

Then we can get $m = 7.9$, and we round it up to 8 bits. Therefore the resolution of the 16-bit digitizer of the 4.7 T/33cm Bruker/GE Omega System in Magnetic Resonance Systems Lab (MRSL) is high enough for the experiment of the proposed architectures.

4.1.3.4 Noise Figure of the Front-End

The calculation result of SNR shows that the SNR at the output of the planar coil is much smaller than that at the output of a multi-turn solenoid coil. This requires that the SNR degradation by the RF front-end has to be as low as possible, that is, the noise figure of the RF front-end has to be as low as possible.

The total noise figure of the RF front-end is calculated using the following equation.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \frac{F_5 - 1}{G_1 G_2 G_3 G_4} \qquad 4.6$$

where F_n is the noise figure (or in other context, noise factor) of the $n-th$ stage of the RF front-end, and G_n is the gain of the n-th stage. And we can find that the noise figure of a certain stage is suppressed by the total gain of the stages preceding this stage, therefore, the gain of the LNA is designed to be as large as possible in order to suppress the noise figure of the succeeding stages. Moreover, the LNA is the first stage of the RF front-end and the noise figure of which is not suppressed, therefore, the noise figure is required to be as low as possible.

Based on the previous discussion, a Common Source (CS) LNA was designed and discussed in Chapter III with a gain of 45.58dB and noise figure of 0.217dB. This gain high is enough in order to suppress to noise figure of the mixer, filter and amplifier. The noise figure of the whole receiver front-end designed in this work is 0.935dB and the gain ranges from about 80dB to 90dB.

4.1.3.5 Noise Performance Comparison between the Proposed Architectures and the Existing Architecture in SEA

As reported in [3], [9], Ultrasonic Cable is used in the receiver of [3], [8], [9], compared to the standard RG-174 cable, the Ultrasonic Cable is responsible for 26% of the decrease of SNR which is calculated as $\sqrt{Q}$, that is, 2.6 dB decrease of SNR. This is because, first, signal power lost in the cable including thermal lost and RF radiation, second, possible SNR degradation happens because of crosstalk among Ultrasonic Cables. And this 2.6 dB SNR degradation happens before the first gain stage, that is, the LNA. Therefore, it is not suppressed, and is treated as a noise figure of 2.6 dB added directly to the LNA. Then the total NF of the receiver is

$$F = F_{Ultrasound\_Cable} + \frac{F_{LNA} - 1}{F_{Ultrasound\_Cable}} + \frac{F_{Mixer} - 1}{F_{Ultrasound\_Cable} G_{LNA}}$$
$$+ \frac{F_{VGA} - 1}{F_{Ultrasound\_Cable} G_{LNA} G_{Mixer}} + \frac{F_{VGA} - 1}{F_{Ultrasound\_Cable} G_{LNA} G_{Mixer} G_{VGA}}$$
$$\approx F_{Ultrasound\_Cable} + \frac{F_{LNA} - 1}{F_{Ultrasound\_Cable}} = 4.3dB$$

where the noise figure of the LNA is 1.7 dB, and the gain is 32.5 dB in [3], [8], [9]. The noise figures of the succeeding stages are not important because of the high gain of the LNA as analyzed previously.

Analyzing the proposed architecture, we know that there is not cable between the MR coil and the front-end. Therefore, there is not SNR decrease before the receiver front-end. In conclusion, compared with architecture in [3], [8], [9], the proposed architecture acquires a NF drop from a value between 4.3dB to 0.935dB.

4.1.3.6 Linearity of the Front-End

The main magnet is shielded and therefore the MR signals at the output of each coil are “clean”, that is, no out of band signal exists, therefore, the requirement of linearity of the RF front-end is relaxed. One important limitation needs to be considered is the power supply of the receiver front-end is +/-0.9V. If the output voltage amplitude of the receiver front-end approaches this limitation, distortion happens and SDR decreases. Simulation result shows that when V_{pp} of the receiver front-end output voltage reaches 1.5V, the total harmonic distortion (THD) is 0.3%, that is, 50dB.

4.1.3.7 Limit of Maximum Channel Number

In the proposed TDM architecture, the switch for multiplexing was placed after the down-converters where MR signals are down-converted to IF, which is 1MHz. The speed of the switch is determined by the bandwidth of the MR pulse sequence.

The main limitations of the channel number are the bandwidth of the analog circuit after the switch [16], and the speed of the switch. In [4], [5], [15], [16], the switch was placed before the mixer and the succeeding stages, the limitation of the analog circuit bandwidth limited the channel number. On the other hand, in the proposed architectures, the switch is placed at the far-end of the receiver, and therefore the bandwidth of the analog circuit does not limit the channel number.

For example, we can select AD8184 (Analog Devices, Inc. Norwood, MA) [73] as the switch. The switching speed of AD8184 is as high as 10MHz. And if the channel width of the MR signal is 20kHz as discussed in Chapter II, the channel number is 500 if

the switching clock and the digitizer clock are phase locked. This number is large enough for a 256 channel coil array.

4.2 Using Phase Coil Array as Target Coils

In order for generalization, the phase coil array in [6], [10], [70], [71] is explored as target coils. As shown in Figure 2.20 and re-drawn in Figure 4.6, an simplified array of surface coils are placed with overlapping between adjacent coils in order for decoupling.

The same architectures as proposed in Figure 4.2 and Figure 4.3 were used and analyzed for this phase coil array. In these architectures, the capacitance range of the tunable capacitor or the varactor needs to be changed according to the impedance of the coil.

The specifications of this proposed topology are similar to those of the proposed architecture using planar coil array in SEA MRI.

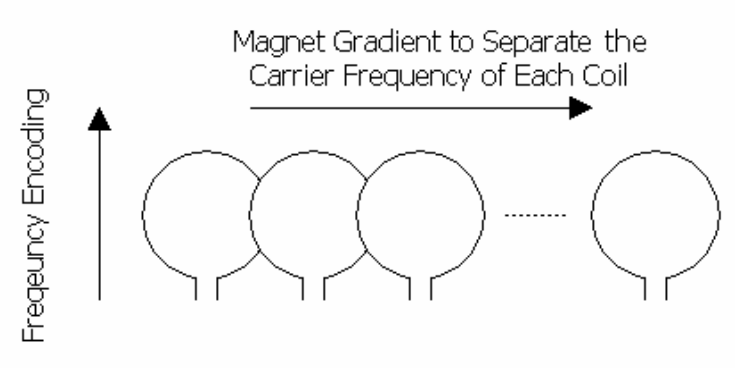


Figure 4.6 Simplified Illustration of the Phase Coil Array

CHAPTER V

DESIGN OF A FOUR-CHANNEL FRONT-END PROTOTYPE ON A PRINTED CIRCUIT BOARD

In order for verifying the proposed architecture of the receiver front-end and the TDM technique discussed in Chapter II, a prototype of four-channel front-end was designed and tested on a single PCB. As shown in Figure 5.1, in each channel, a differential MR signal at 200.228MHz was sent to two-stage dual matched LNAs for amplification. After amplified, the MR signal was sent to a pair of mixers for down-conversion to 0.5MHz. Then after the polyphase filter, LPF and VGA, the down-converted MR signals were sampled by a multiplexing switch and multiplexed to a single channel and were sent to the digitizer via the buffer. In this architecture, each MR coil was matched 50Ω. There were two stages of LNA as the preamplifiers, and therefore the total gain of the preamplifiers were increased to effectively suppress the noise of the succeeding stages. The quadrature generator, polyphase filter and the mixer worked together to attenuate the thermal noise at image frequency as discussed in Chapter II and Chapter III.

Figure 5.2 is the photograph of prototype of the four-channel front-end with TDM on a Single PCB. The dimension of the PCB is 20.5cm in length and 15cm in width. The dielectric of the PCB is FR4 with a thickness of 62mil, and the thickness of the copper layer is 1oz and it is silver plated.

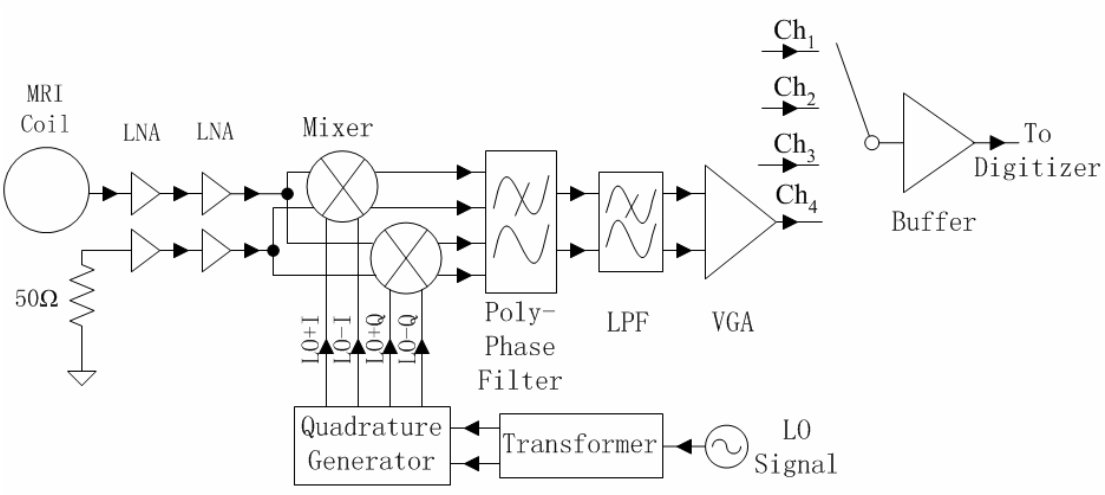


Figure 5.1 Architecture of the Four-Channel Front-End with TDM on a Single PCB

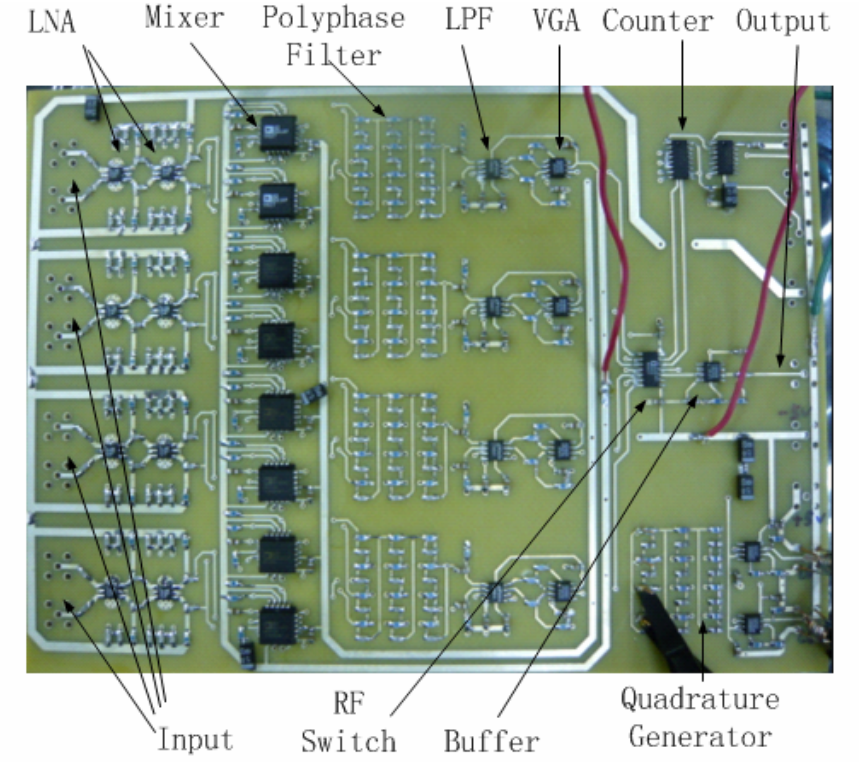


Figure 5.2 Photograph of the Four-Channel Front-End with TDM on a Single PCB

5.1 Main Targets of the Prototype

The main targets of the design of this prototype are

1. First house-made multiplexed multi-channel receiver.
2. Proposing an architecture which is suitable for on-chip design.

5.2 System Design

Before the selection of components for each stage of the receiver front-end, system level specifications and other considerations have to be determined in the following.

5.2.1 System Gain

The input signal of the prototype is from the MR coil and its peak voltage is at the level of several μV to about 100μV depending on different kinds of MR coil. The output signal of the prototype is sent to the 12-bit CompuScope 6012 digitizing card (Gage Applied Sciences, Montreal, Canada) and its maximum input voltage can be set from several hundred mV to several volts. Therefore, the voltage gain of the receiver front-end is determined to be about 70dB-90dB.

5.2.2 Noise Figure

As discussed in Chapter II, the noise figure is expected to be as small as possible, and it was mainly determined by the noise figure and the gain of the LNA. The author selected MERA-7433+ (Mini-Circuit, Brooklyn, New York) with noise figure of 2.7dB

and gain of 25dB at 200MHz [74] as the preamplifier for the consideration of cost and performance. Two stages of LNA were set up in the receiver front-end as the preamplifier, and the total gain adds up to 50dB so that it is high enough to suppress noise of the succeeding stages. Therefore, the specification of total noise figure of the receiver front-end is determined to be 3dB.

5.2.3 Input 1dB Compression Point

For a nonlinear memoryless, time-variant system, such as a receiver front-end, if the input signal level increases, the gain of the system decreases because of the nonlinear effect [25]. Therefore in RF circuits, the Input 1dB Compression Point (P_{1dB}) is defined as the input signal level increases to a certain value that causes the system gain to decrease by 1dB [25] as shown in Figure 5.3 where A_{in} is the input signal level and A_{out} is the output signal level. Here P_{1dB} is determined to be 20dB higher than the input MR signal level.

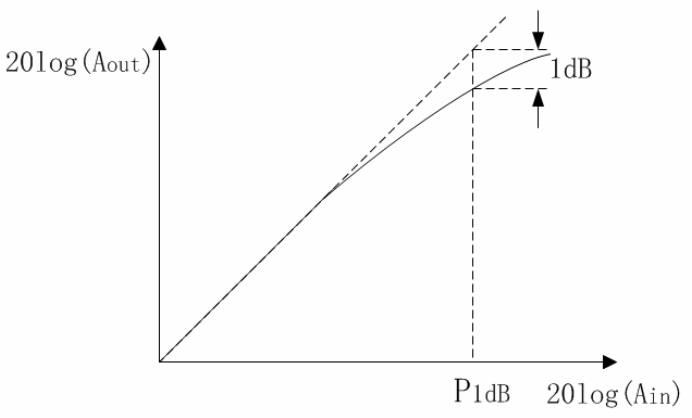


Figure 5.3 Definition of Input 1dB Compression Point

5.2.4 Input Third Intercept Point

For a nonlinear memoryless, time-variant system, such as a receiver front-end, if there is a two-tone signal at frequency of ω_1 and ω_2 sent to the input of the system, third order intermodulation (IM_3) products exhibits at frequency of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ at the output of the system besides the fundamental products at frequency of ω_1 and ω_2 because of nonlinearity effect [25]. As the input signal level increases, the IM_3 products increase faster than the fundamental products as shown in Figure 5.4, and the IIP_3 is defined to be the intersection point of the two lines [25].

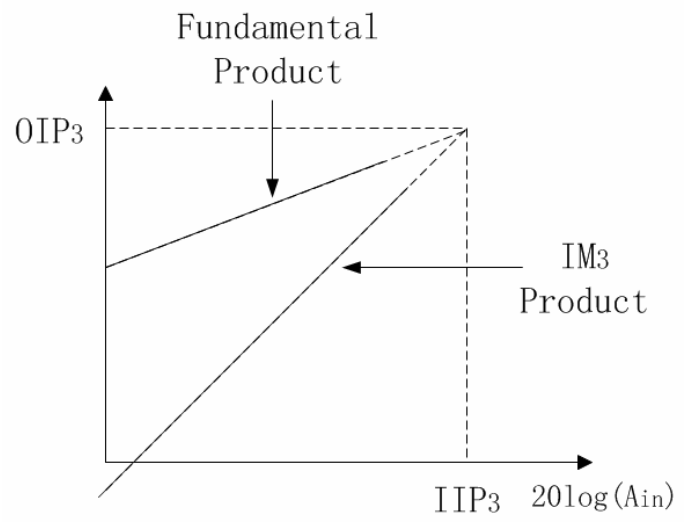


Figure 5.4 Definition of Input Third Intercept Point

Since the MR signal sent to the receiver front-end is clean, that is, containing only a single tone at the Larmor frequency and only thermal noise existing out of the Larmor frequency, the IIP_3 is relaxed.

5.2.5 Slew Rate

Slew rate is defined as the fastest changing rate of the output voltage of a circuit [75], such as VGA, opamp. At the intermediate frequency after the mixer, the MR signal is amplified to higher amplitude, and therefore the slew rate must be higher than the maximum changing rate of the signal voltage according to the following equation, where A is amplitude of the signal voltage.

$$SR > \max(\frac{d(A\cos\omega t)}{dt}) = A\omega \qquad 5.1$$

In worst case, if the power supply of the circuit is 5V, let $A = 5V$, and the intermediate frequency is 0.5MHz, therefore, after calculation, we can get the slew rate must be larger than 15.7V/μS.

5.2.6 Input Resistance and Capacitance of each Block

At RF, the input impedance of each block needs to be 50Ω as the load of the preceding stage. Otherwise, it has to be matched to 50Ω, and the simplest method is connecting 50Ω resistor at the input to the ground as shown in Figure 5.5. In this case, the input resistance of this block has to be high enough and the input capacitance has to be low enough so that the input impedance is close to 50Ω after being matched, and S_{22} of the previous stage is lower than -20dB.

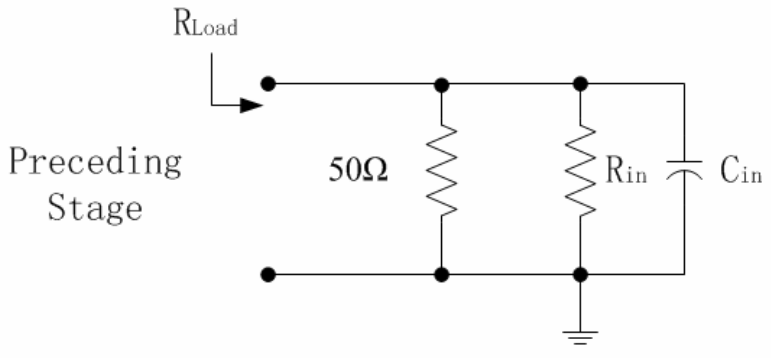


Figure 5.5 Input Matching Circuit of RF Block

The calculation of S_{22} is given as the following equation [76].

$$S_{22} = \frac{R_{Load} - 50}{R_{Load} + 50} \qquad 5.2$$

where R_{load} is load impedance of the preceding stage, that is, the matched input impedance as shown in Figure 5.5. And R_{load} is given as

$$R_{Load} = 50 // R_{in} // \frac{1}{j\omega C_{in}}$$

where ω is the Lamar Frequency of the MRI system and is 2π × 200MHz in this design.

Using MATLAB, we can evaluate the value R_{in} and C_{in} as shown in Figure 5.6. And we can find that if R_{in} is larger that 500Ω and C_{in} is smaller than 3pF, S_{22} is smaller than -19.9dB.

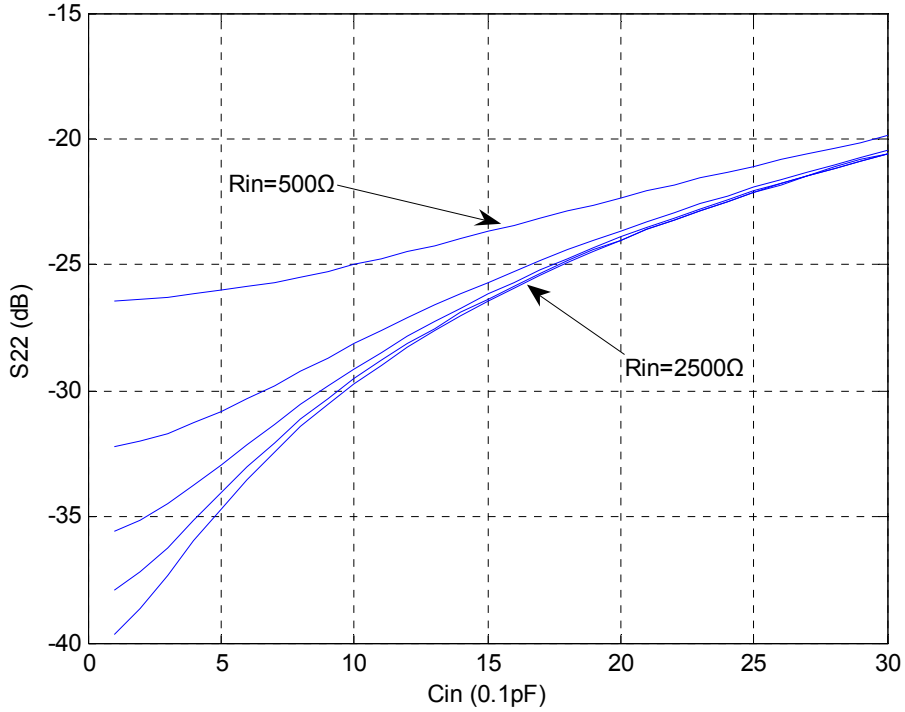


Figure 5.6 MATLAB Evaluation of Input Resistance and Capacitance

After down-conversion, the signal frequency is much lower than RF, and the connection line on the PCB between each block is much shorter than 1% of the signal wave length, therefore 50Ω matching is not necessary. However, the additional pole introduced by R_{in} and C_{in} of the succeeding stage still needs to be consider in order to ensure that the bandwidth is larger than IF. If R_{in} is larger that 500Ω and C_{in} is smaller than 3pF, the addition pole it introduces is much larger than IF. C_{in} still is not allowed to be too large to cause instability of the preceding block. Therefore the input resistance is determined to be larger than 500Ω and the input capacitance is determined to be smaller than 3pF.

5.2.7 Maximum Input Voltage

In order to avoid large distortion, normally each component has a specification of V_{inMax}. Therefore the maximum input voltage of each component has to be larger than the MR signal at the input.

5.2.8 Power Supply

The number of the power supply of the components has to be as small as possible in order to simplify the setup of the prototype. Therefore, the author selected +12V for the LNA, and +/-5V for the other components. There still exist digital components for processing the RF switch clock. The power supply of these digital components was selected to be +5V, but it was separated from the power supply of the analog components to avoid the digital signal leaking to the analog signal through the power supply.

5.2.9 Package

In order to minimize the size of the prototype, the packages of each component are selected to be surface mount (SMT) and as small as possible.

According to the discussion above, the components of the receiver front-end are selected and the specifications are listed in Table 5.1 [73], [74], [77], [78], in which the VGA and the buffer are setup using a high speed opamp of AD8009 (Analog Devices, Inc. Norwood, MA). And from Table 5.1, we can find that the specifications and the other requirements of the system design are satisfied. Note that the gain of the mixer

specified in [76] is 0dB. However, the author only used the mixer core of AD8009 to set up the mixer, and the gain of the mixer is about 3dB.

According to the specifications listed in Table 5.1, we can get the total gain of the receiver is 68dB to 91dB (including 3dB loss of the polyphase filter discussed in part 5.3.3.2). This satisfies the system design specification of total gain. Still the total noise figure can be calculated using equation (4.6) as the following equation.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \frac{F_5 - 1}{G_1 G_2 G_3 G_4} + \frac{F_6 - 1}{G_1 G_2 G_3 G_4 G_5} \approx 2.72dB$$

And we can find that the system design specification of total noise figure is also satisfied. From the specifications listed in Table 5.1 [73], [74], [77], [78], we can find that the system design specifications and other considerations are satisfied.

Table 5.1 List of the Selected Components and Specifications for each Stage

Stage	LNA	Mixer	LPF	VGA	Switch	Buffer
Model Number	MERA-7433+	AD831	LTC-1566-1	AD8009	AD8184	AD8009
Gain	25dB	3dB	12dB	0-22.5dB	0dN	0dB
NF	2.7dB	10.3 dB	34 dB	11 dB	14 dB	11 dB
IIP_3	10dBm	24dBm	N/A	N/A	N/A	N/A
P_{1dB}	18dBm	10dBm	N/A	N/A	N/A	N/A
V_{inMax}	10dBm	-10dBm	$1.5V_{pp}$	$3.7V_{pp}$	$3.15V_{pp}$	$3.7V_{pp}$
R_{in}	50Ω	RF:600kΩ LO: 500Ω	70MΩ	110kΩ	2.4MΩ	110kΩ
C_{in}	N/A	2pF	2pF	2.6pF	1.6pF	2.6pF
R_{out}	≈50Ω	<20Ω		<0.1Ω	28Ω	<0.1Ω

Table 5.1 (Continued)

Stage	LNA	Mixer	LPF	VGA	Switch	Buffer
Slew Rate	N/A	300V/μS	N/A	5500 V/μS	750 V/μS	5500 V/μS
Bandwidth	DC-1GHz	RF/LO: 500MHz IF: 250MHz	2.3MHz	700MHz	700MHz	700MHz
LO Input	N/A	0.1-1V	N/A	N/A	N/A	N/A
Power Supply	12V	+/-5V	+/-5V	+/-5V	+/-5V	+/-5V
Package	DL805	PLCC20	SO-8	SO-8	SO-14	SO-8

5.3 Circuit Design

5.3.1 MR Coil

In order for the testing of MR imaging using the prototype, a four SEA coil array as shown in Figure 5.7 was built with each coil matched to 50Ω. Each individual coil was designed to be 70mil in width and about 8cm in length. Each conductor track of the coil is 10mil in width and each gap between the adjacent tracks of a single coil is 20mil. The gap between the adjacent coils is about 1.6cm in order to minimize the coupling between coils. A phantom filled what $CuSO_4$ solution was place on top of the SEA coil. Axial imaging was done with the slice selection in perpendicular to the SEA coil.

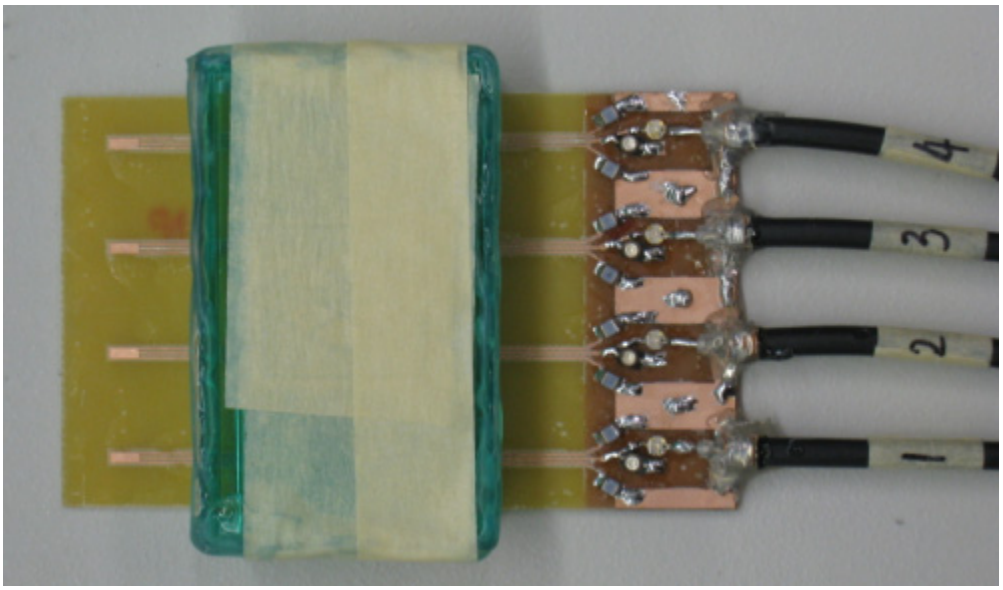


Figure 5.7 Four SEA Coil with Phantom on Top of It

5.3.2 Preamplifier

As shown in Figure 5.2, two stages of LNA are setup as the preamplifier to satisfy the requirement of the total gain of front-end, and to effectively suppress the noise figure of the succeeding stages, especially the LPF, which has a very high noise figure of 34dB.

Since the LNAs of each channel and each stage share the same power supply, MR signal leakage happens from the output of each LNA, especially the second stage which has larger MR signal at the output, to the other channel, and then crosstalk happens. In order to reduce signal leakage and crosstalk, the width of the power supply connection line is increased to 90mil to reduce parasitic resistance. And more importantly an array of decoupling 1000pF capacitors is connected from the power line to the ground plane at the bottom layer of the PCB through as many via holes as possible.

The capacitance of each capacitor is selected to be 1000pF basing on the consideration that for a capacitor package of SMT 0805, the parasitic inductance at its terminals is about 0.8nH [79], therefore at about 170MHz to 200MHz, the capacitance has lowest impedance. That is, an array of 1000pF capacitors doesn't not simply equal to a capacitor with larger capacitance for the application of decoupling. Figure 5.8 [74] shows the schematic of the array of decoupling capacitors connected between the power supply line and the ground. Note that the LNA is power supplied by the +12V power source via 90Ω resistor.

Still in order to reduce signal leakage and crosstalk, the array of capacitors has to be as close to the output of the LNA as possible. Moreover, the ground plane has to be in a plane as large as possible all in order to reduce the parasitic resistance and inductance.

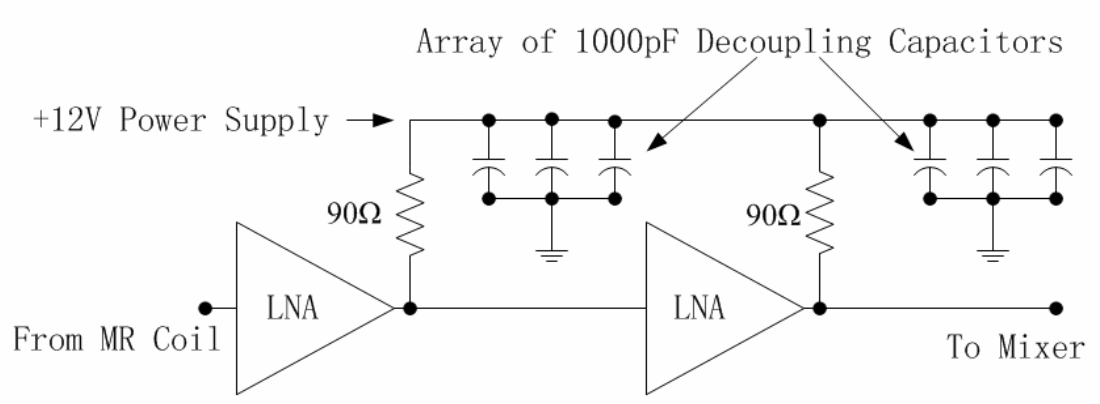


Figure 5.8 Power Supply and Decoupling of Preamplifiers

Another decoupling method is using RF choke connected in series with the 90Ω resistor. An RF choke is an inductor with impedance as high as 800Ω [79], and

effectively block the MR signal leaking from the output of the LNA through the power supply line to the output of other LNAs. However, the RF choke contains a ferrous core which is strongly magnetic and has to be out of the main magnet of the MRI system.

Each LNA consumes as much as 80mA DC current, therefore the dissipation of the heat generated by the preamplifiers has to be considered when designing the circuit on a PCB. If a fan mounted on the PCB, the prototype is bulky, and even worse, the fan also contain ferrous components and it will has to be out of the magnet. Moreover, the fan introduces noise to the LNAs and largely decreases the SNR of the MR signal. This problem is solved by using an area of metal layer on the PCB underneath the LNA and connecting this metal area to the ground plane on the bottom layer through as many via holes as possible, and therefore that heat is dissipated by large area of metal layer.

5.3.3 Down-Converter

As discussed in Chapter II and Chapter III, the mixer, the quadrature generator and the polyphase filter work together as an image rejection down-converter which attenuates the thermal noise at image frequency and down-convert the MR signal to IF. In this design, the architecture of the down-converter is the same as that of the chip design and modifications have been done in each of the three blocks.

5.3.3.1 Quadrature Generator and Polyphase Filter

Since this design is board level design, and there is enough board area for the layout of the polyphase filter, the polyphase filter was designed to be three stages instead

of two stages in the chip design discussed in Chapter III. Also since this work is a board level design, the parasitic capacitance of the connection line is at the level of 1pF, the capacitances of the capacitors in the quadrature generator and the polyphase filter are increased to 10pF and 270pF respectively while the resistances of the resistors in the quadrature generator and the polyphase filter are decreased according to $R_{Qn} = \frac{1}{\omega_{RFn} C_Q}$ and $R_{Pn} = \frac{1}{\omega_{IFn} C_P}$ respectively. The component values of the quadrature generator and the polyphase filter shown in Figure 2.11 and Figure 2.12 are listed in Table 5.2 and Table 5.3 respectively.

Table 5.2 Component Values of Quadrature Generator

Component	R_{Q1}	C_{Q1}	R_{Q2}	C_{Q2}	R_{Q3}	C_{Q3}
Value	66.5Ω	10pF	78.7Ω	10pF	95.3Ω	10pF

Table 5.3 Component Values Polyphase Filter

Component	R_{P1}	C_{P1}	R_{P2}	C_{P2}	R_{P3}	C_{P3}
Value	1kΩ	270pF	1.18kΩ	270pF	1.4kΩ	270pF

The LO signal was generated by a PTS 250 Frequency Synthesizer (Programmed Test Sources Inc. Littleton, MA), and was converted from single-ended to differential-

ended by a $1:\sqrt{2}$ transformer ADCH-80+ (Mini-Circuit, Brooklyn, New York) [80]. Next, the differential-ended LO signal was sent to the quadrature generator through a buffer whose input was matched to 50Ω using a 50Ω resistor at the input of the buffer. The buffer was a high speed opamp of AD8009 connected in negative non-inverting feedback with a gain of 2. Figure 5.9 shows the circuits processing the LO signal. Note that the impedance ratio of the transformer is $1:\sqrt{2}$ and each end of the transformer differential output is transmitted by a 50Ω coaxial cable to a 50Ω input of the buffer, therefore we can easily get the input impedance of the transformer is 50Ω.

After converted from single-ended to differential-ended, the LO signal was then sent to the quadrature generator as discussed in Chapter II and Chapter III.

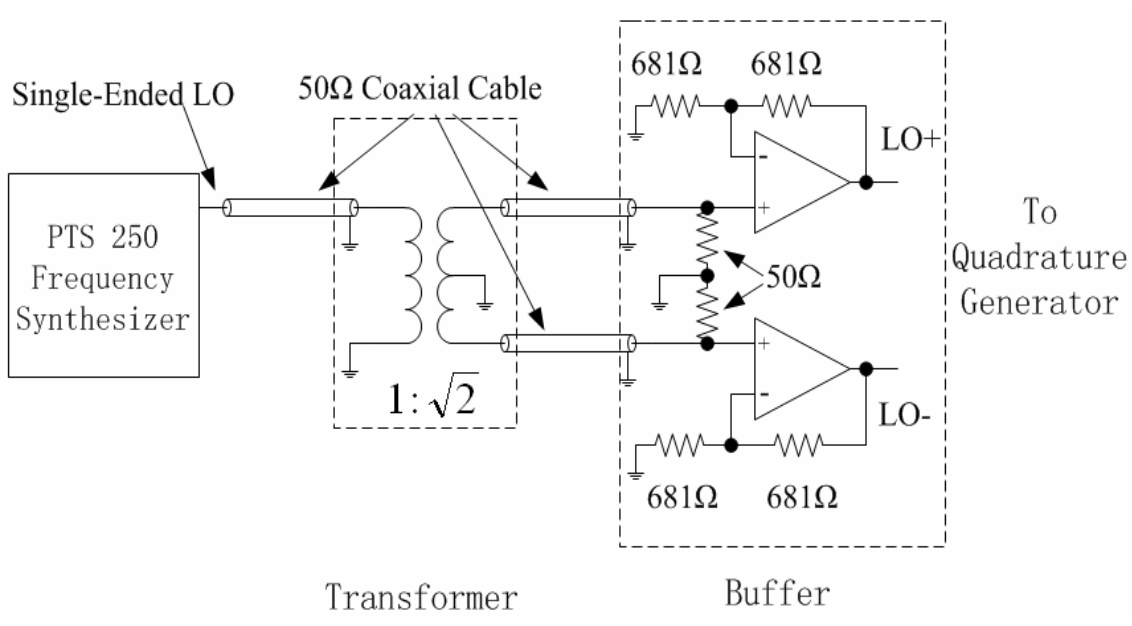


Figure 5.9 Single-Ended LO to Differential-Ended LO Conversion

5.3.3.2 Mixer Setup and Down-Converter Gain

The mixer was setup using the mixer core of AD831 (Analog Devices, Inc. Norwood, MA) [81] as shown in Figure 5.10. Note that according to the discussion in part 5.2.6, since the input capacitances of the mixer LO port and the RF port are small enough [81], and the input resistances are large enough, the inputs of the mixer LO port and RF port were matched to 50Ω by connecting a 50Ω resistor from each end of the inputs to the ground. In order from simplification, the input matching 50Ω resistors of both ports are not shown in Figure 5.10.

From Figure 5.10, we know that the DC current of the transconductors Q_1 and Q_2 are 18mA respectively, therefore we can calculate the tranconductance of Q_1 and Q_2 as equation 5.3 [82].

$$g_m = \frac{I_T}{2V_{th}} \tag{5.3}$$

where I_T is the DC current of each transconductor, and $V_{th}=kt/q\approx 26mV$ @ 300^0K. As shown in Figure 5.10, there is a 20Ω source degeneration resistor for each transconductor, therefore, the effective tranconductance of Q_1 and Q_2 is [82]

$$g_{m,eff} \approx \frac{g_m}{1+g_m\times 20\Omega} = \frac{\frac{I_T}{2V_{th}}}{1+\frac{I_T}{2V_{th}}\times 20\Omega} \approx \frac{\frac{18mA}{2\times 26mV}}{1+\frac{18mA}{2\times 26mV}\times 20\Omega} \approx 43.7mA/V$$

Then the conversion gain of the mixer is [17]

$$G_C = 20\times\log(\frac{2}{\pi} g_{m,eff}\times R_L) \approx 3dB$$

The down-converted signal at the output of the mixer was then sent to the polyphase filter as shown in Figure 2.12. As analyzed in [26] or using KVL, KCL and Superposition Principle, the three-stage polyphase filter has a lost of 3dB when the input capacitance of the LPF is much smaller than 270pF while the input resistance is much larger than 1kΩ [77]. Based on the above analysis, the total conversion gain of the down-converter is 0dB.

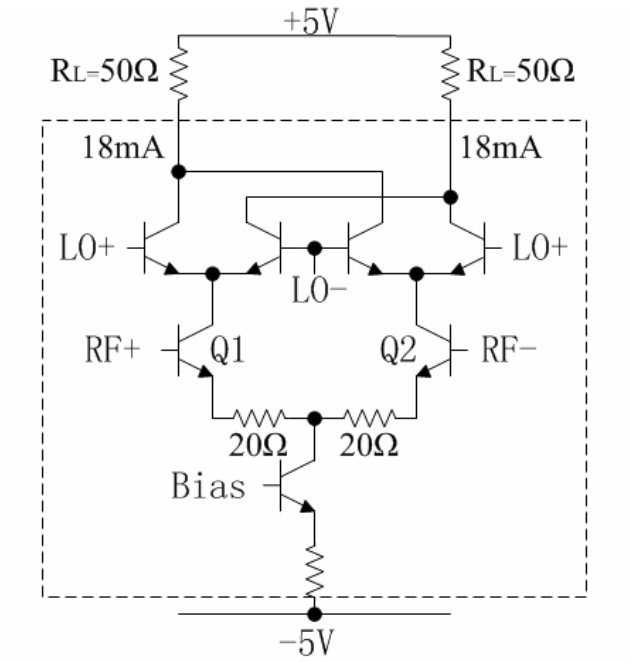


Figure 5.10 Setup of Mixer
(The Circuit inside the Dashed Line Is the Simplified Mixer Core of AD831)

5.3.4 LPF and VGA

After the signal was mixed and the noise at image frequency was rejected, the signal was sent to LPF to attenuate energy at high frequency generated by the mixer.

After being filtered, the MR signal was then sent to VGA for amplification. The LPF is LTC-1566-1 (Linear Technology Corporation, Milpitas, CA) with a gain of 12dB from DC to 2.3MHz and attenuation of more than 80dB for frequency higher than 100MHz [77]. The VGA is a high speed opamp of AD8009 set up in non-inversion feedback. The gain of the VGA is tuned by changing the value of the resistors, and therefore the gain of the VGA can be tuned. Figure 5.11 shows the setup of the LPF and VGA [77] [78]. After amplified to a proper value of voltage amplitude, the down-converted MR signal was sent to the switch for multiplexing.

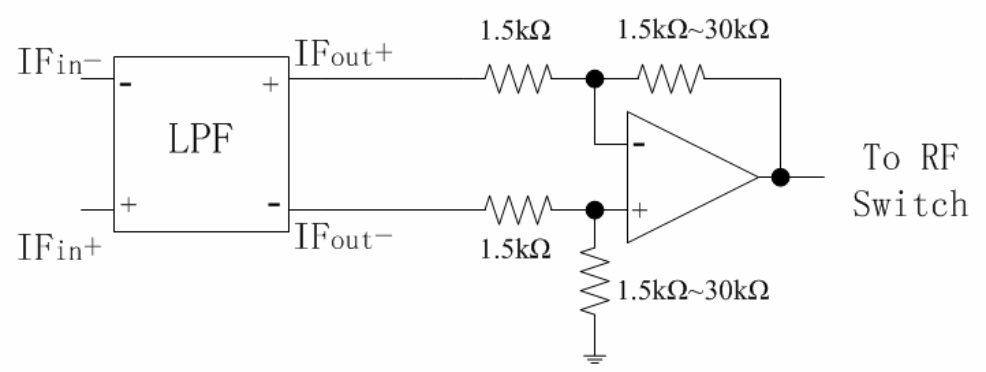


Figure 5.11 LPF and VGA

5.3.5 Multiplexing Switch and Switching Control

The RF switch AD8184 (Analog Devices, Inc. Norwood, MA) was selected as the multiplexing switch to multiplex the four channels of MR signals into one channel. Since 0.1% settling time of AD8184 is as small as 15nS [73], the switch frequency can be as high as 10MHz if the digitizer and the switch clock are phase locked. The switching control logic inputs for the switch were generated by 74ACT161 digital

counter (Fairchild Semiconductor Corporation, San Jose, California) with maximum counting frequency of 60MHz [83]. Note that all of the logic signals in this design are Transistor–Transistor Logic (TTL).

As shown in Figure 5.12, a 10MHz sinusoidal signal with DC offset of 0V from the MR system was sent to a coaxial Bias-Tee from Mini-Circuits (Mini-Circuit, Brooklyn, New York) which moved the DC offset of the sinusoidal single to equal to the amplitude of the sinusoidal. Then the sinusoidal signal was sent to an inverter which converted the sinusoidal to TTL. Next, the 10MHz TTL signal was sent to the counter and the frequency was converted down to 312.5MHz which was used as the switching frequency of the multiplexer. Moreover, a sampling trigger pulse generated from the MRI system was sent to the reset pin of the counter. Before the MRI system started to send out the MR signal (spin echo), the sampling trigger is at logic "0" so that the outputs of the counter Q_1 and Q_0 were reset to logic "0". Q_1 and Q_0 were connected to the switch control inputs A_1 and A_0, which worked together to determine which channel at the input of the switch was selected to the output according to Table 5.4 of true values. Therefore, at the beginning of the spin echo, channel 1 is selected to the output until the next conversion of the logic level of switching clock comes at which time channel 2 is selected to the output. Each conversion of the logic level of the switching clock causes the selected channel number increasing by 1. The timing diagram of the switching control is shown in Figure 5.13.

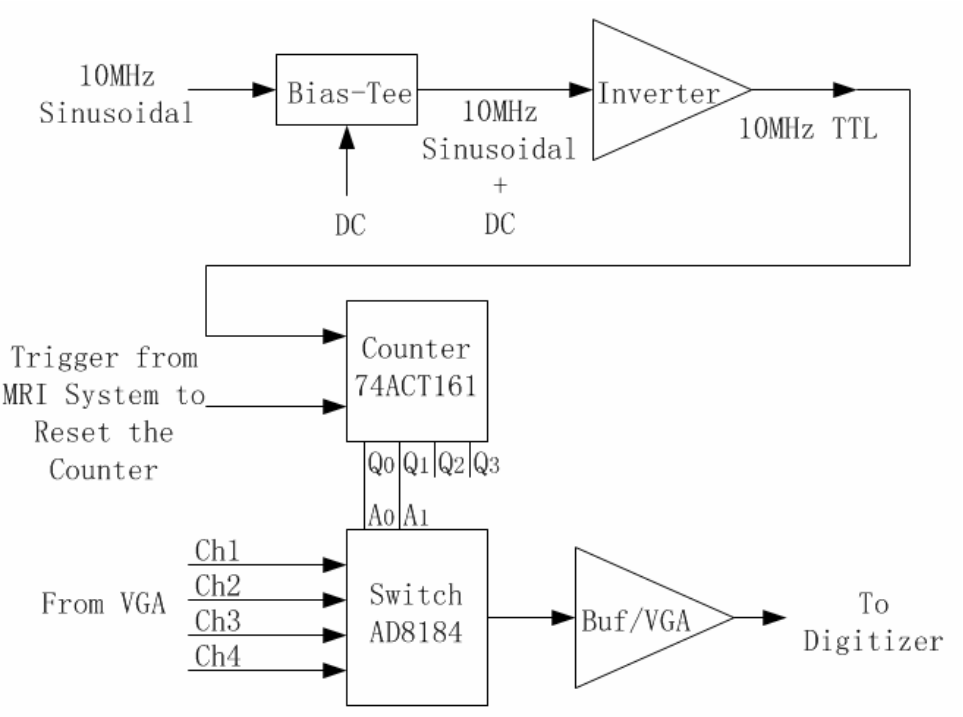


Figure 5.12 Multiplexing Switch and Switching Control

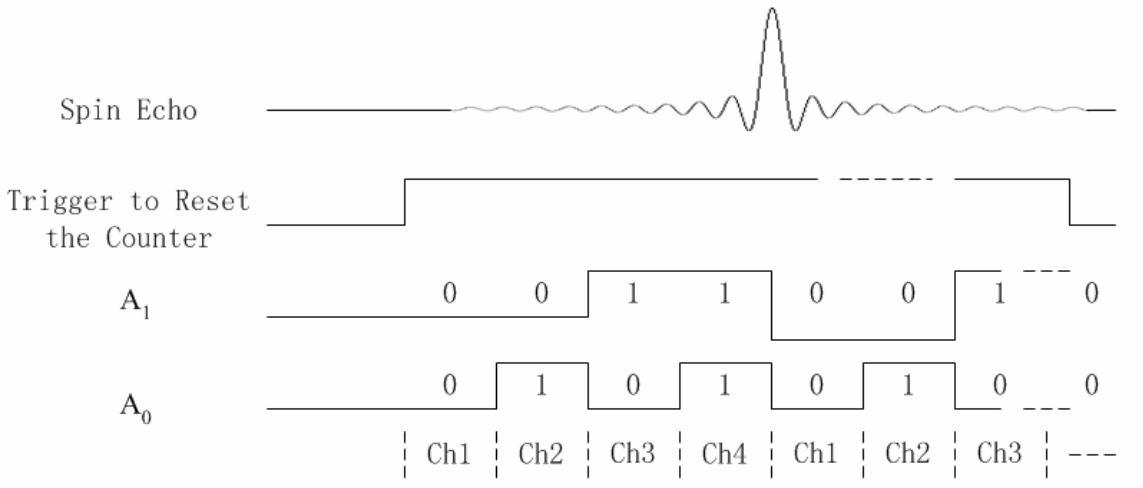


Figure 5.13 Timing of Switching Control

After multiplexed, The MR signal at the output of the switch was sent to a buffer which was set up as resistance negative feedback and also acts as a VGA using a high speed opamp of AD8009 for the following reasons. First, the opamp of AD8009 has higher capability of driving a capacitive load. Second, the voltage amplitude of the MR signal at the output of the buffer can be adjusted by adjusting the values of the resistance of the feedback resistor. Third, a 42Ω resistor was connected in series at the output of the buffer for the purpose of impedance matching.

The MR signal from output of the buffer was them sent to a CompuScope 6012 digitizer for digitization.

Table 5.4 True Values Table of the Switch

A_1	A_0	Output
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

In the following, two timing methods of the multiplexing and de-multiplexing are analyzed.

One is switching at the Nyquist sampling frequency of the sequence bandwidth, that is, the bandwidth of the MR signal which is at the level of tens kHz depending on the pulse sequence. And then the multiplexed signals are digitized at the Nyquist

sampling frequency of the MR signal. When digitizing the multiplexed signals, the switching clock from A_1 is also digitized by the additional channel of the digitizer. Since both the multiplexed signals and the switching clock are digitized by the digitizer using the same internal clock, they have the same time base. And therefore, the rising and falling edges of this switching clock are used to recognize at what time the channels to be separated. After being digitized, the multiplexed signals are separated into 4 set of raw data. Each set of raw data is then down-converted, filtered. Finally, the image of each channel is reconstructed.

The other method is switching at the Nyquist sampling frequency of the MR signal, and then digitizing the multiplexed signals. After digitization, the multiplexed signals are separated, and down-converted to baseband. And finally, the image of each channel is reconstructed. This method needs much higher switching frequency than the first method. Moreover, if the switching clock and the sampling clock of the digitizer are not phase locked, oversampling is still necessary. Because of the previous reasons, this method was not used in the testing of the prototype. However, the advantage of the method is that the clock sources do not need to be synchronized.

The first method assumes that the switching clock and the digitizer clock source are all phase locked. This requirement is very easy to be satisfied if the digitizer is equipped with the option of external clock source so that the digitizer and the switch use the same clock source. Unfortunately, the digitizer available for the testing of this prototype is not equipped with this option. Therefore, when the digitizer sample the multiplexed signals at the transient between adjacent channels, error may happens for

separating the multiplexed signals. However, this problem can be easily solved if the clock sources are synchronized by using a digitizer equipped with the option of external clock source.

5.3.6 Power Supply

In order to simplify the power supplies, in the prototype, the same type of the chips on different channel shared the same power supply, and some of the different type of the chips also shared the same power supply. Therefore, leakage may happen from one chip to other chips and from one channel to other channels. In order to solve this problem, the power supply of some types of the chips has to be separated from others. Firstly the power supply of the digital chips (counter and inverter) has to be separated from all other analog chips to avoid the TTL signals of the digital chips especially the rising and falling edges of the TTL signals leaking to the analog signals. Second, for the analog chips, since the signals at LNAs are much smaller than those at the other chips, a small portion of leakage to the LNAs will largely decrease the SNR of the signals at the LNAs, therefore, the power supply of the LNAs has to be separated from others analog chips.

In conclusion, there are three power supplies for the prototype. First, the LNAs uses +12V power supply. Second, the digital chips used +5V power supply. And finally, all the other chips used a +/-5V power supply. Each power supply used a 0.1μF ceramic capacitor and another 4.7μF Tantalum capacitor for a wide-band decoupling.

5.3.7 Ground Plane

The bottom layer of the PCB was used as the ground plane. In order to reduce the parasitic resistance on the ground, which causes leakage among chips, the ground plane has to be connected to a unique area instead of being separated into small patches by the connection lines on the bottom layer. Moreover, parasitic resistance still exists on the ground plane although it is small. In order to avoid leakage from digital chips to analog chips, the ground plane underneath the digital chips has to be separated from the ground plane underneath the analog chips. However, since the digital signal and the analog signals need to have the same reference voltage, both ground planes still need to tight up at the far-end.

5.4 Bench-Testing

5.4.1 Setup of the Bench Testing

First the prototype was set up on an antistatic poly sheet and powered by three sets of power source. A 199.728MHz signal-ended LO signal was generated PTS 250 Frequency Synthesizer, and converted to differential-ended by a transformer as discussed in part 5.3.3.1 and illustrated in Figure 5.9.

In this bench-testing, a 200.228MHz single-ended RF signal with voltage amplitude of $2V_{pp}$ was generated by PTS 250 Frequency Synthesizer and converted to differential-ended by a transformer. Before sent to the input of the pre-amplifier of the prototype, the RF signal was attenuated by 63dB.

The TTL switching clock was generated by a HP 33120A Function Generator and sent to the input of the counter. Not sampling trigger pulse was sent to the counter in this bench-testing, therefore, the reset pin of the counter was set to enable, that is, +5V for logic “1”.

The output of the prototype was sent to the CompuScope 6012 digitizer using a 50Ω cable. A Tektronix 2465A 350MHz Oscilloscope was also used to measure the signal on the prototype.

The setup up of the bench testing was shown in Figure 5.14.

Figure 5.14 Setup of Bench-Testing

5.4.2 Gain of the Receiver Front-End

In order to test the gain of each channel, modifications were done as the following. First, the RF signal was sent to one channel and the inputs of the other three channels were terminated using 50Ω resistors. Next, the two connection lines from the counter outputs Q_1 and Q_0 to the switch inputs A_1 and A_0 were cut to be broken, and A_1 and A_0 were connected to ground as logic "0" or +5V as logic "1" according to Table 5.4 for channel selection. In this measurement, the gain of the VGA was initially set to 11.2dB. Therefore the total gain of the receiver is calculated as the following according to the previous analysis.

$$Gain_{Total} = Gain_{\Pr eamp} + Gain_{Mixer+PolyPhaseFilter} + Gain_{LPF} + Gain_{VGA} + Gain_{Switch}$$
$$= 50dB + 0dB + 12dB + 11.2dB + 0dB = 73.2dB$$

A $2V_{pp}$ RF signal generated by the PTS 250 was attenuated by 63 dB and sent to on channel of the RF receiver. After amplifications and down-conversion, we can get the down-converted signal at the output of the receiver at $5.28V_{pp}$ at 0.5MHz as shown in Figure 5.15. So, we can get the receiver gain is 71dB. This measured gain of the prototype is 2.2dB smaller than the calculated value. The reasons of the missing of gain are analyzed as the following. First, the 90Ω resistor at the output of each LNA decreased the gain of the each LNA. Second, the gain of the chip of each stage has a range deviation from its standard value. However, the measured value is very close to the calculated value and satisfies the requirement of the system design.

The measured gain of each channel was listed in Table 5.5.

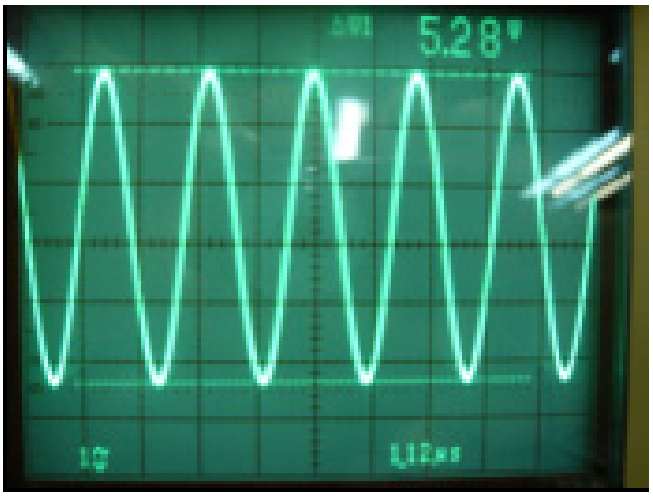


Figure 5.15 Measured Output Signal of Prototype

Table 5.5 Gain of each Channel

Channel Number	1	2	3	4
Gain	71.5dB	71dB	71dB	70.8dB

5.4.3 Suppression of Thermal Noise at Image Frequency.

It was tested by sending a RF signal at 200.228MHz, and sending another signal with the same power (voltage) at image frequency respectively. Then compare the output of each signal. As shown in Figure 5.16, we can find that when the signal was input to the receiver front-end at 200.228MHz while the LO frequency is 199.728MHz, the voltage amplitude of the output signal is $5.28V_{pp}$. When the signal was input to the receiver front-end at image frequency, the voltage amplitude of the output signal is

0.52V_{pp}. Therefore, we can get the suppression of the noise at the image frequency is 20dB. This value shows that the noise at image frequency was successfully suppressed.

The measured suppression of the noise at the image frequency of each channel was listed in Table 5.6.

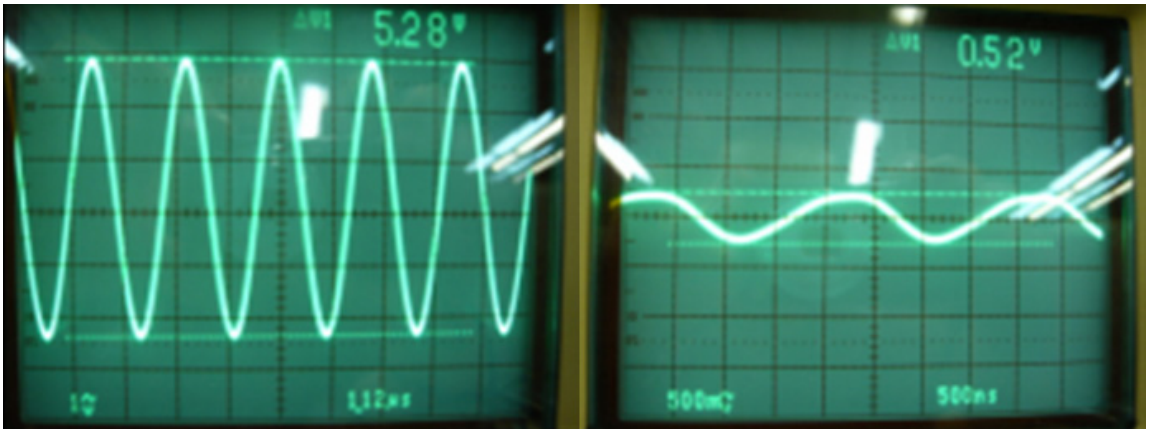


Figure 5.16 Suppression of the Noise at the Image Frequency. Left: Measured Output Signal with Input Signal at 200.228MHz; Right: Measured Output Signal with Input Signal at Image Frequency

Table 5.6 Suppression of Thermal Noise at the Image Frequency of each Channel

Channel Number	1	2	3	4
Suppression	18dB	20dB	20dB	22dB

5.4.4 Crosstalk among Channels

This was measured by sending a RF signal to only one channel and measuring signals at the output each channel. From Figure 5.17, we can get the crosstalk is 37 dB.

The measured crosstalk among the four channels was listed in Table 5.7.

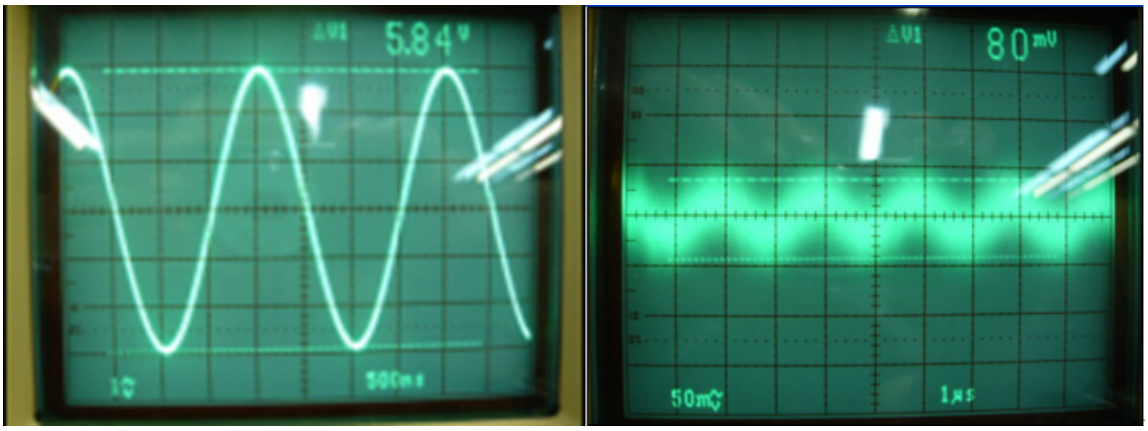


Figure 5.17 Crosstalk
Left: Measured Output Signal of the Channel with RF input
Right: Measured Output Signal of the Channel without RF Input

Table 5.7 Crosstalk among Channels

Channel Number	1	2	3	4
1	–	37dB	36dB	38dB
2	37dB	–	37dB	40dB
3	36dB	37dB	–	40dB
4	38dB	40dB	40dB	–

5.4.5 Other Measurements

5.4.5.1 Phase Shifts between each Quadrature LO Signal from the Output of the Quadranture Generator

Since the capacitors used in the quadradure generator are 10pF, and the parasitic capacitance on the connection lines of a PCB is at the level of 1pF, the phase shift between each LO signal at the output of the quadrature generator is possible to be affected by the parasitic capacitance. The degree of the suppression of the image frequency noise largely depends on how well the LO signals are shifted at the output of the quadrature generator. Therefore, the phase shifts between each LO signal at the output of the quadrature generator were measured as shown in Figure 5.18.

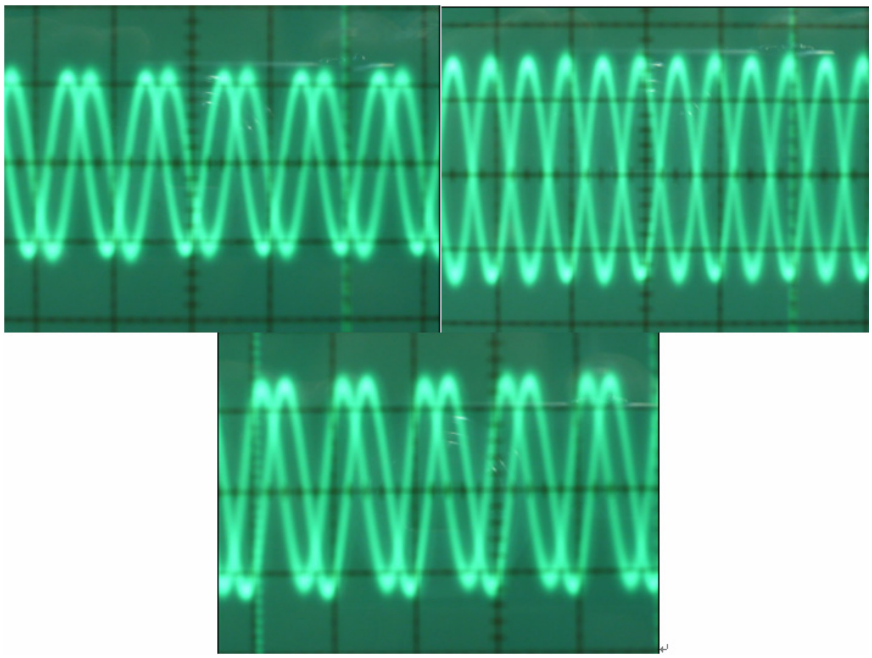


Figure 5.18 Phase Shifts between each Quadrature LO Signal from the Output of Quadranture Generator. Upper Left: LO_0^0 to LO_90^0; Upper Right: LO_0^0 to LO_180^0; Lower: LO_0^0 to LO_270^0

This measurement used a Tektronix 2465A 350MHz Oscilloscope and four identical probes in order to minimize phase mismatch among each probe.

The measured phase shifts between each channel at the output of the quadrature generator was listed in Table 5.8.

Table 5.8 Phase Shifts between Quadrature LO Signals

Channel Number	1	2	3	4
1	–	86^0	175^0	261^0
2	86^0	–	89^0	175^0
3	175^0	89^0	–	86^0
4	261^0	175^0	86^0	–

5.4.5.2 Multiplexed Signals Viewed at the Output of the Prototype

In order to view the output signal after the multiplexing of the switch, a RF signal was sent to the input of one of the four channels while the inputs of the other three channels were terminated by 50Ω resistors. The switch was controlled by the counter and the switch clock was generated by a HP 33120A Frequency Generator. The signal at the output of the prototype is shown as Figure 5.19.

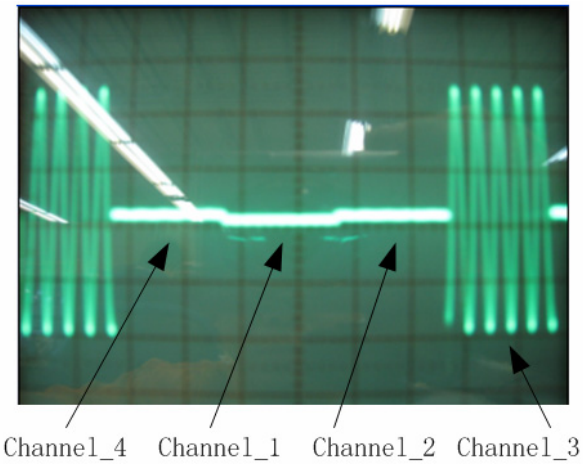


Figure 5.19 Multiplexed Signals Viewed at the Output of Prototype

5.5 MRI Testing

5.5.1 MR Image Acquired Using a Single Channel

Initially, a MR image was acquired using a single channel and using an orange as the phantom as shown in Figure 2.20. From Figure 2.20, we can find that phase jitter exists for the reason that the clock of the digitizer and the clock of the MRI system are not synchronized and therefore after the digitizer received the trigger from the MRI system, the digitizer waits until the succeeding rising or falling edge, depending the definition of the digitizer, before the digitizer starts to digitize the MR signal [84]. This time jitter is random and ranges from zero to on period of the digitizer clock because both clocks of the digitizer and the MRI system are free running from each other [84]. A Solution is illustrated in [84] by using over-sampling to decrease to time jitter and therefore decrease the phase jitter of the image.

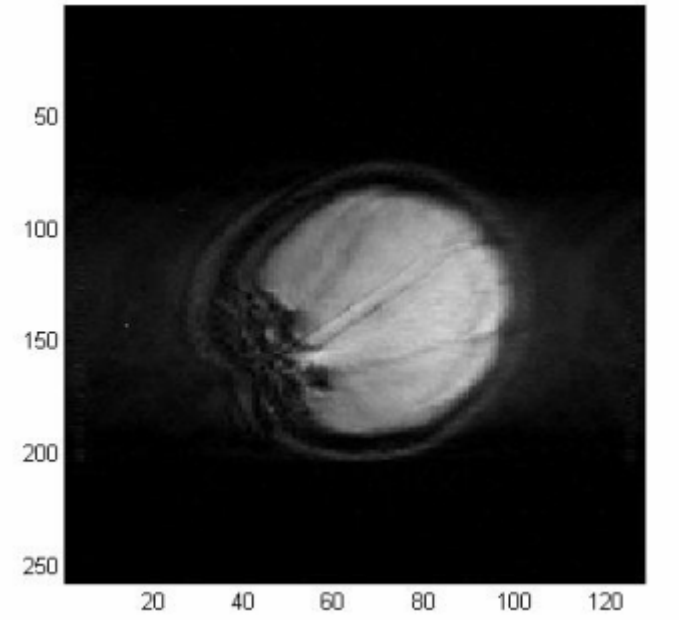


Figure 2.20 MR Image Acquired Using a Single Channel

5.5.2 Parallel MR Imaging with the Four-channel Receiver out of the Magnet

The bench testing and MR imaging using a single channel shows that single channel works as expect, then parallel images were acquired using the four-channel of the receiver prototype with the prototype was place out of the main magnet of the MR system. In this parallel imaging, a four SEA coil array as shown in Figure 5.7 was used as the receive coils. A phantom filled what $CuSO_4$ solution was place on top of the SEA coil array. Axial imaging was done with the slice selection of the in perpendicular with the SEA coil. The prototype was set about 10 meter away from the receive coil and each coil was connected to a receiver using a RG223 or RG58 cable with about 15 meter in length. The signal loss through these long cable decreases the SNR of the MR singles. In

order to solve this problem, a low noise preamplifier with a gain of 25dB was used between each receiver coil and the cable which connected the input of the receiver.

First, the signals from the receiver prototype before being multiplexed were digitized and saved. Images were acquired from these signals. In order for comparison, MR signal from each receive coil was also sent to a commercial MR system and image was acquired using the same pulse sequence. Figure 5.21 shows the images and SNR of the images acquired from the receiver prototype before being multiplexed. Figure 5.22 shows the images and SNR of the images acquired from commercial MR system. The average of SNR of the images in Figure 2.21 is 6dB higher than those of in Figure 2.22. However, the slice thickness of the images in Figure 2.21 is two times that of the images in Figure 2.22, therefore, the noise performance of the receiver prototype matches that of the commercial MR system.

In the next step, in order to verify the multiplexing of the prototype, the multiplexed MR signals and the switching clock from A_1 pin of the switch were digitized together using the dual channels of the digitizer. The multiplexing method in hardware and de-multiplexing method in software was talked in part 5.3.5. The images and the SNR of the images acquired from the de-multiplexed singles are shown in Figure 5.23. We can find that the SNR of the images acquired from the de-multiplexed signal still approximately match the SNR of the images acquired from the signal of the prototype before multiplexing and the SNR of the images acquired from the commercial MRI system. However, we can find that alias happens. This is because of the synchronization problem will not be emphasized in this testing.

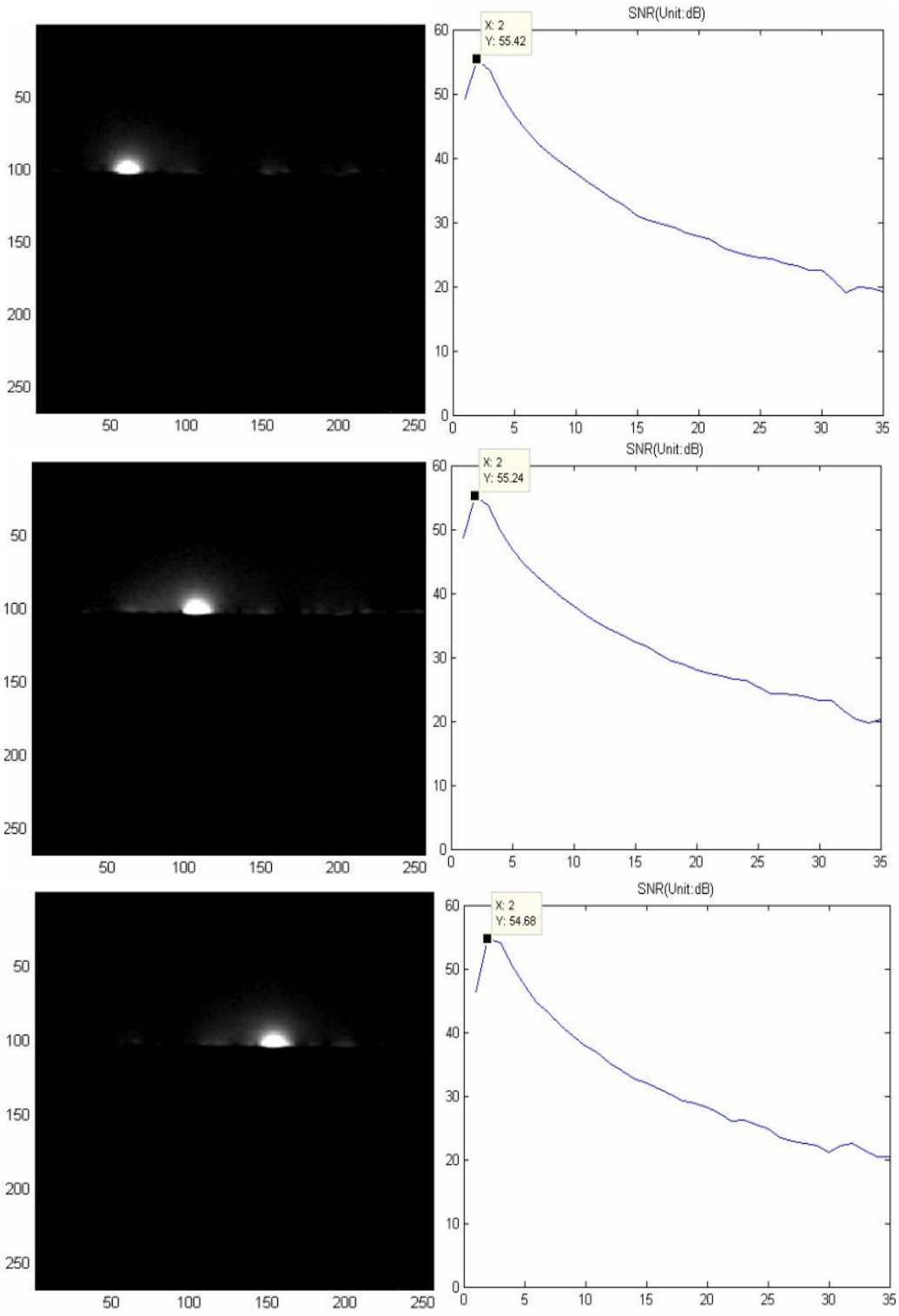


Figure 5.21 Images and SNR of the Images Acquired from the Receiver Prototype before Being Multiplexed

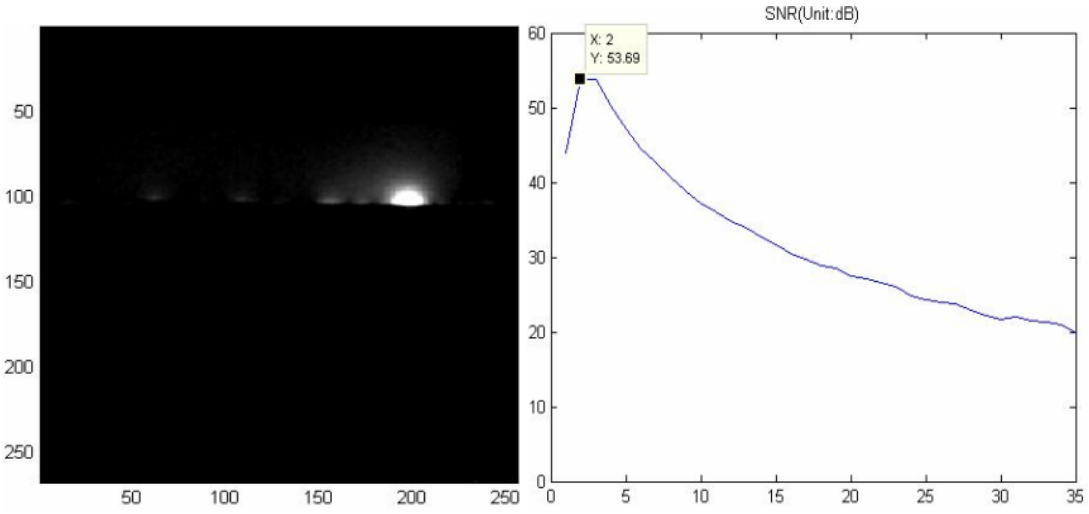


Figure 5.21 (Continued)

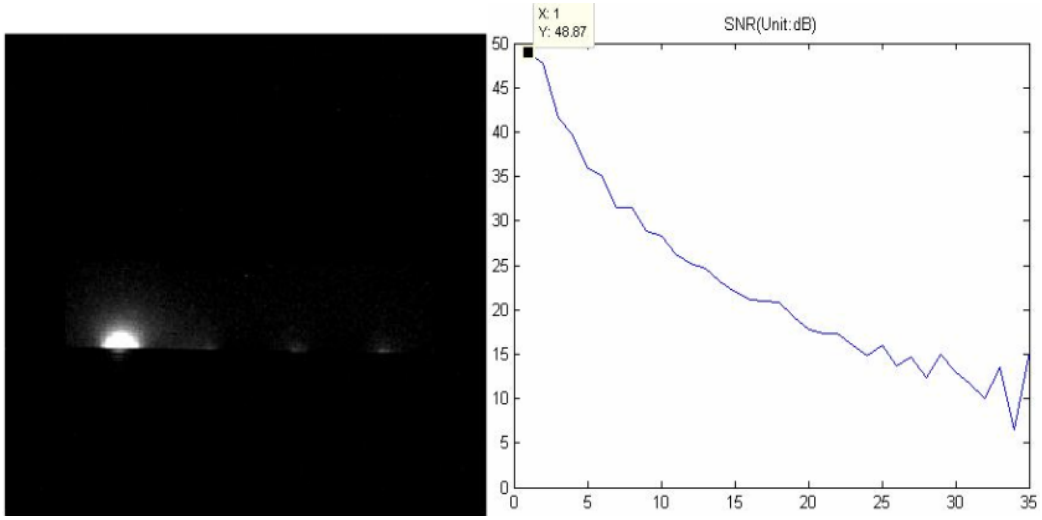


Figure 5.22 Images and SNR of the Images Acquired from Commercial MR System

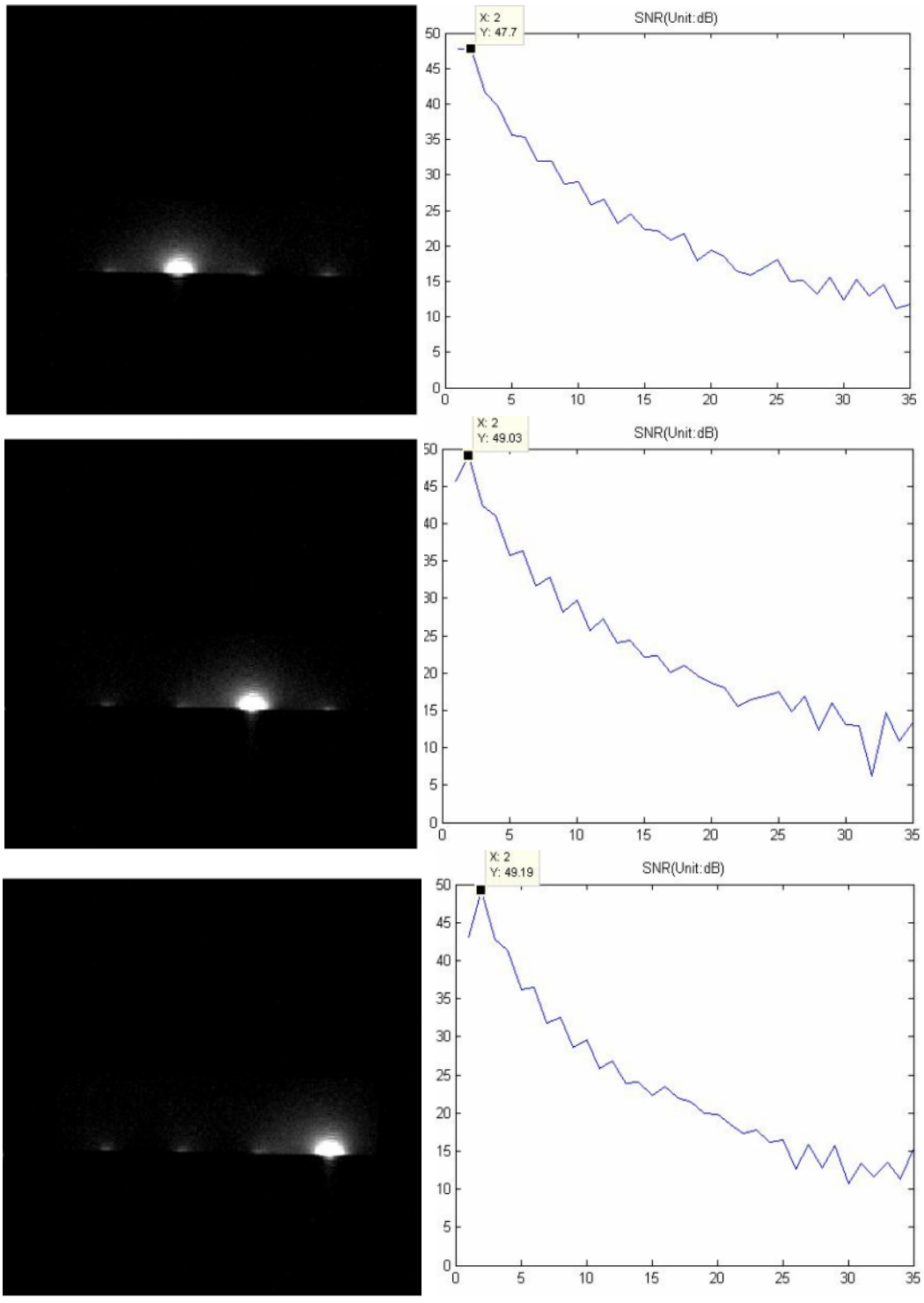


Figure 5.22 (Continued)

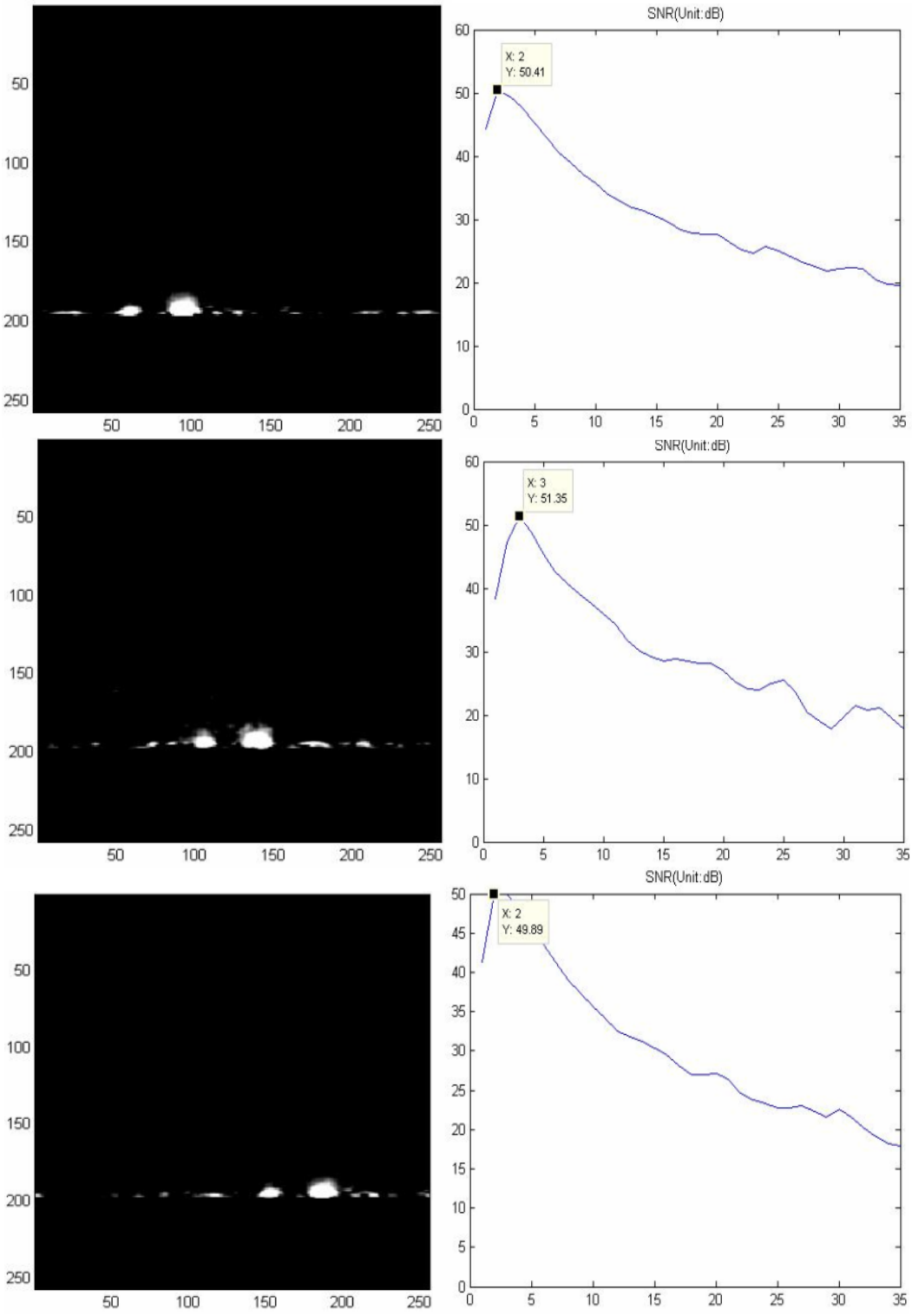


Figure 5.23 Images and SNR of the Images Acquired from the De-Multiplexed Singles

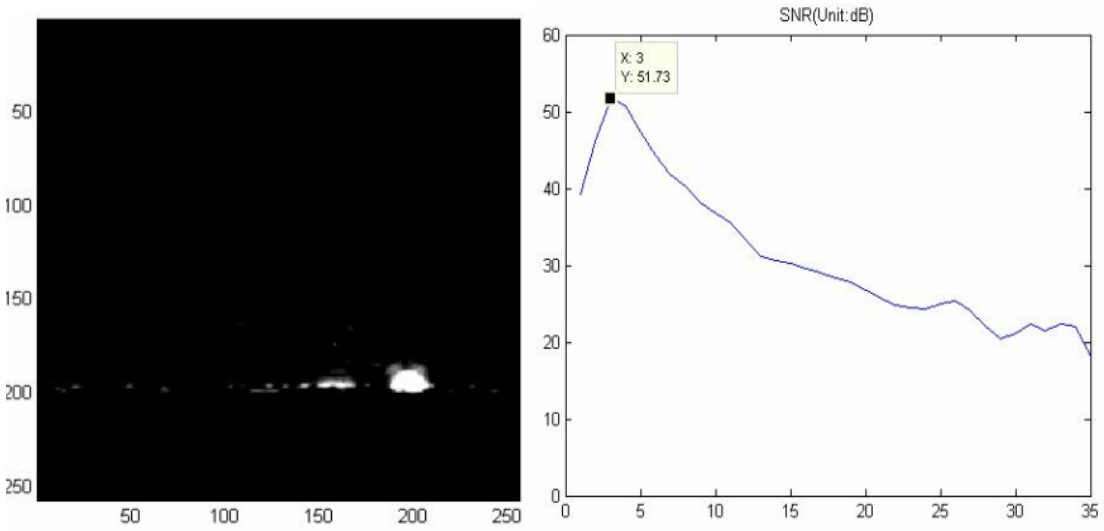


Figure 5.23 (Continued)

5.5.3 Parallel MR Imaging with the Four-channel Receiver inside the Magnet

In order to explore the feasibility of mounting the receiver together with the receiver coil on the same circuit board toward the idea of digital coil, the receiver was mounted together with the receive coils on a plastic board as shown in Figure 5.24. The receive coils were mounted inside the volume coil which is the transmit coil. The receiver prototype was mounted about 30cm away from the coils. The coils and the input of the receivers were connected by RG174 coaxial cables. After the coils and the receiver prototype were mounted, they were placed inside the magnet bore.

Then the images were acquired from the output of the receiver and were shown in Figure 5.25.

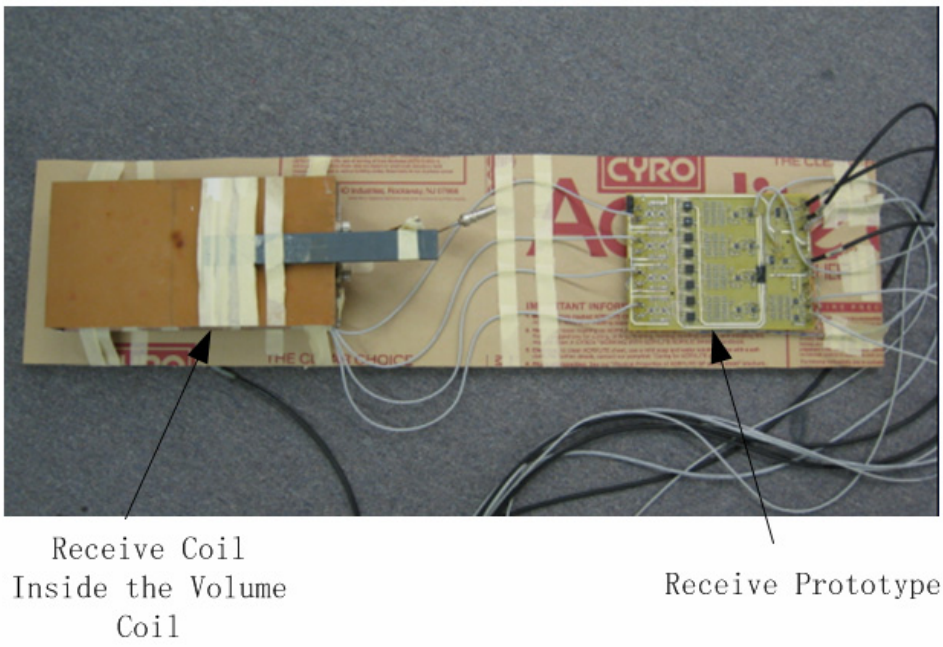


Figure 5.24 Receiver Prototype Mounted together with the Receive Coils on a Plastic Board

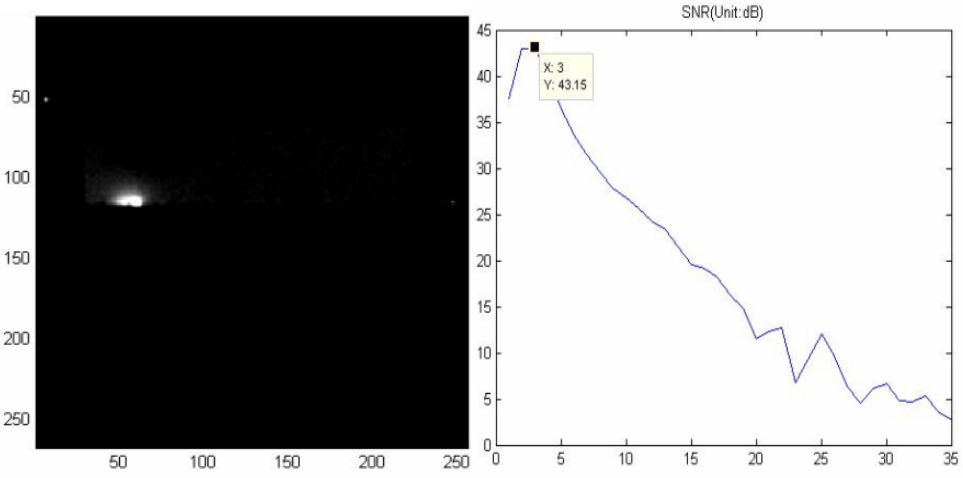


Figure 5.25 Images and SNR of the Images Acquired from the Receiver Prototype inside the Magnet

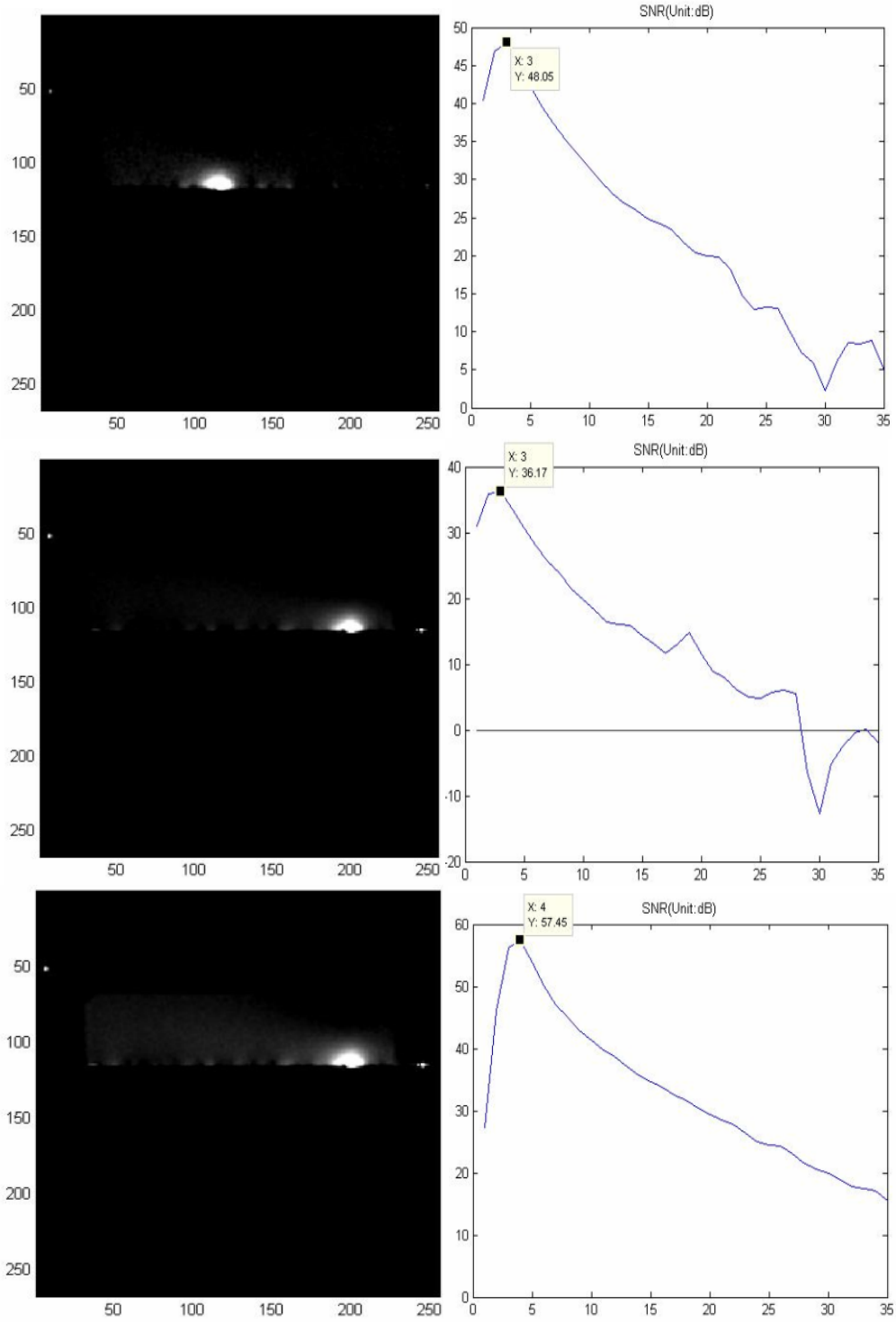


Figure 5.25 (continued)

Discussion:

1. There are two small white spots at about (10, 50), and (240, 120). It may be some leakage from the LO frequency. Since the LO signal differential, there exists two spot with same frequency but different phase.
2. The SNRs from each channel are un-even.

However, we still can see the feasibilities of placing the receiver inside the magnet for parallel MR imaging.

CHAPTER VI

FUTURE WORK AND CONCLUSIONS

Parallel magnetic resonance imaging has been considered to be the most effective method to allow for simultaneous analysis of multiple biological samples, to improve other valuable factors, such as enlarging the field-of-view, increasing signal-to-noise ratio, and especially to facilitate faster image acquisition. The conventional method of stacking multi-channel of RF receivers with very low level of integration has been expensive and cumbersome.

In the work of this dissertation, architecture has been proposed to satisfy fully on-chip design of a whole receiver front-end including low noise preamplifier, image rejection down-converter, low-pass filter and variable gain amplifier. This architecture also satisfies four channels of receiver front-end to be designed on a single chip and provides possibility of higher level of integration while acquire ultra low noise, small size and low power consumption. In order to further increase the compactness and decrease the power consumption, in this work, the bandwidth of the digitizer has been efficiently exploited by using the time domain multiplexing technique which multiplexes multi-channel of down-converted MR signals from the output of multi-channel receiver front-end into a sequence of consecutive time slots of a single channel so that multi-channel of MR signals can be digitized by a single digitizer.

In the purpose for demonstration, a four-channel RF receiver front-end was designed using TSMC 0.18μm technology on a single chip. Each channel of the RF

receiver includes an ultra low noise amplifier, a passive mixer a quadrature generator and polyphase filter, a low-pass filter, another low-pass filter which also acts as a variable gain amplifier (VGA). The receiver has an over NF of 0.935dB, variable gain from about 80dB to 90dB, power consumption of 30.8mW, and chip area of 6mm^2.

Also in the purpose for demonstration, a prototype of the four-channel receiver front-end using the proposed architecture with TDM was designed on a Single PCB with dimension of 20.5cm in length and 15cm in width. The dielectric of the PCB is FR4 with a thickness of 62mil, and the thickness of the copper layer is 1oz and it is silver plated. Bench-tested was done and images were acquired. The testing and magnetic resonance imaging results verify the proposed ideal.

First design of fully integrated multi-channel receiver front-end in literature was done in this work. It starts a new research field to explore the limitation of reducing the size, cost, and power consumption of receivers for parallel MRI. First, success of this designed and testing turns the original design of parallel MRI receivers from the size of about half cubic meter in dimension into the size of about a finger nail while improving the performance. Second, this design also discards the large bunch of cables and furthers increases the compactness of the system. Third, this work introduces the possibility of the idea of “Digital Coil Array” in which the Parallel MR signals are analog processed, multiplexed and digitized, and finally, at the output of the “Digital Coil Array”, digitized parallel MR signals are sent to the computer for image recovering. Fourth, if digital signal processing (DSP) chip and liquid crystal display (LCD) are also integrated, the

conventional receiver system can be expected to be turned into a hand-held MRI movie system.

In the first step of future work, design with higher level of integration is suggested by the author for future research. First, a high speed, high resolution digitizer is to be designed on the same chip of the receiver front-end. Second, the multiplexing switch is replaced by a new topology of sample-and-hold circuit which works as the sample-and-hold of the digitizer while works as the multiplexing switch. Third, the receiver architecture is further optimized and the noise figure is further decreased.

In the second step of future work, DSP circuits are designed on the same PCB of the receivers and images are recovered real-time and the recovered images are converted to optical signal by laser diode and transmitted by fiber optic to the photodiode at LCD display system for reception and display.

As a concept to start a new field, the unanticipated and unimaginable future contributions of the work of this dissertation possibly exist.

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