SOFT SWITCHED HIGH FREQUENCY AC-LINK CONVERTER

A Thesis

by

ANAND KUMAR BALAKRISHNAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2008

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Soft Switched High Frequency Ac-Link Converter. (December 2008)

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Variable frequency drives typically have employed dc voltage or current links for power distribution between the input and output converters and as a means to temporarily store energy. The dc link based power conversion systems have several inherent limitations. One of the important limitations is the high switching loss and high device stress which occur during switching intervals. This severely reduces the practical switching frequencies. Additionally, while the cost, size, and weight of the basic voltage sourced PWM drive is attractive, difficulties with input harmonics, output dV/dt and over-voltage, EMI/RFI, tripping with voltage sags, and other problems significantly diminish the economic competiveness of these drives. Add-ons are available to mitigate these problems, but may result in doubling or tripling the total costs and losses, with accompanying large increases in volume and weight.

This research investigates the design, control, operation and efficiency calculation of a new power converter topology for medium and high power ac-ac, ac-dc and dc-ac applications. An ac-link formed by an inductor-capacitor pair replaces the conventional dc-link. Each leg of the converter is formed by two bidirectional switches. Power transfer from input to output is accomplished via a link inductor which is first charged from the input phases, then discharged to the output phases with a precisely controllable current PWM technique. Capacitance in parallel with the link inductor produces low turn-off losses. Turn-on is always at zero voltage as each switch swings from reverse to forward bias. Reverse recovery is with low dI/dt and also is buffered due to the link capacitance.

To my Grandma

ACKNOWLEDGMENTS

First, I thank my advisor Dr. Hamid Toliyat for his valuable guidance, constant encouragement, awesome teaching, financial support, abundant lab facilities, and what not. I also thank my committee members Dr. Prasad Enjeti, Dr. Shankar Bhattacharyya and Dr. Won-jong Kim for their valuable time. I have thoroughly enjoyed the useful courses they have taught. I express my thanks to Mr. William Alexander, Ideal Power Converters Ltd., Austin, TX for constantly monitoring the progress of the project and for providing crucial guidance whenever it was needed. I thank Tammy Carda, Janice Allen and Linda Currin for their help. I also thank my labmates Salman Talebi, Salih Baris Ozturk, Jeihoon Baek, Behrooz Nikbakhtan, Robert Vartanian, Mahshid Amirabadi, Anil Kumar Chakali, Seungdeog Choi and Nicolas Frank. They created the right fun-filled learning atmosphere in the lab. I also thank my friends Easwaran, Haritha, Pradeep, Shyam, Somasundaram and Suresh. I specially thank Mirunalini Chellappan for her valuable help during the start of this project. I also thank the Thesis Office at Texas A&M University for their help in refining the thesis layout and contents.

Finally, I thank my parents, brothers and sister for their love and for backing me with all the career decisions I have taken.

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CHAPTER I

INTRODUCTION

A. Introduction

The utility provides ac voltage at constant amplitude and frequency. However many industrial applications require voltage at variable amplitude and frequency at various power levels. This has to be achieved through power electronic converters which accept power from the utility in its fixed from and deliver power in other forms as required by the loads.

While the pulse width modulated voltage source inverter (PWM-VSI) configuration has been industry's work horse for over 30 years, significant advances in power semiconductor device technology has resulted in a number of cheaper, compact and more efficient power converters [1–5]. In general, the following characteristics can be considered desirable in power converters used as interface converters in the high frequency link systems [6]:

1) high efficiency for increased system efficiency and for reduced size and weight of the heat dissipating components;

2) inherent bidirectional power flow capability (not requiring substantial modifications in the power circuit for reverse power flow);

3) low distortion output waveform with fundamental frequencies as high as 1000 Hz for increased power density of associated mechanical systems;

4) simple and reliable means of controlling converter output voltage and frequency;

5) minimum voltage or frequency disturbances in the link;

6) adaptability to different types of loads/sources for a higher level of uniformity and

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reliability in the system.

B. Discussion of existing power converter topologies

A matrix converter performs direct ac-ac power conversion from ac utility to ac load, with neither intermediate dc conversion nor dc energy storage elements [7]. Thus, the converter can be realized with greatly reduced size and volume in its structure, compared to the indirect ac-ac power converters grounded on dc-link components. Six-step current-fed converters based on thyristors are favorable in high power applications, because of no PWM operation, very reliable topologies with inexpensive high-power thyristors, and very low switching losses [8]. Controlled converter type utility interface such as a PWM voltage source rectifier (PWM-VSR), or an active power filter (APF) can be employed to solve the harmonic pollution problems of the uncontrolled diode rectifier type interface [9, 10]. Some popular topologies are discussed below.

1. Pulse width modulated voltage source inverters

Here, there are two power conversion stages with intermediate energy storage. Fixed ac from the utility is converted to fixed dc through the uncontrolled rectifier. The link capacitor stores this energy. This is then converted back to ac by the inverter which typically switches at high frequency. Power conversion in this case is said to be indirect as the entire power is transferred through the intermediate ac stage.

The pulse width modulated voltage source inverter is probably the most widely used configuration for dc to ac inverter applications in the 10 W to 500 kW power range. The attractiveness of the VSI topology stems from its extremely simple power structure and the need for only six unidirectional switches as seen in Fig. 1. The

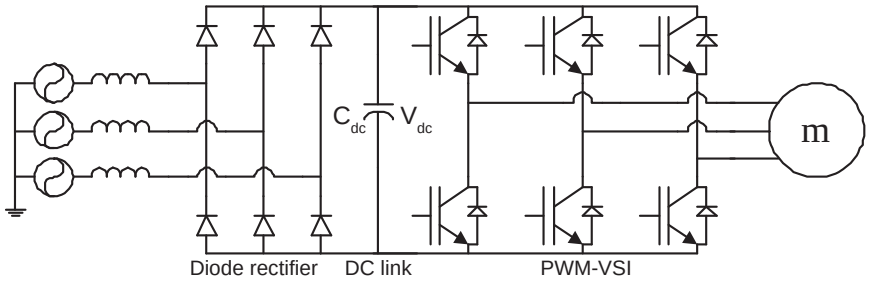

Fig. 1. PWM-VSI

antiparallel diodes required are typically mounted in the same device package for minimum lead inductance and ease of assembly. The control strategy is reasonably simple and provides a fully regenerative interface between the dc source and the ac load. However, given the limitations on the characteristics of available gate turn-off devices, the following problems can also be identified with the topology.

1) The power electronic devices face high voltage and current stress during switching intervals. Hard switching at high frequency increases the junction temperature of the devices. This reduces practical switching frequency and/or also calls for overrated devices. This also results in low-amplifier bandwidth and poor load-current waveform fidelity (harmonics).

2) High $\frac{dv}{dt}$ on the output generates interference due to capacitive coupling.

3) Diode reverse recovery and snubber interactions cause high device stresses under regeneration conditions.

4) Device stresses require large SOA specifications and compromise reliability.

5) Acoustic noise at the inverter switching frequency can be very objectionable.

6) The generation capability into the ac line is poor.

7) The input current to such a converter is highly polluted by harmonics. The diodes conduct only when the instantaneous line voltage is greater than the link voltage. This is only a small percentage of the total cycle time which makes the input current

highly spiky.

8) The dc-link capacitors are inevitably bulky due to their required high power handling. Being electrolytic, they also limit the operating temperature of the system to about 300 ^{o}C.

9) The fault recovery characteristics are poor [11].

Increasing proliferation of power converters fed from the diode rectifiers results in increasing power quality concerns of utility distribution systems. This has led to standards to regulate utility power quality, such as IEEE-519 (American standard) and IEC EN 61000-3 (European standard). In 1993, the IEEE published a revised draft standard limiting the amplitudes of current harmonics [12]. The harmonic limits set by this are based on the ratio of the fundamental component of the load current to the short circuit current at the point of common coupling at the utility. Stricter limits are imposed on large loads than on smaller loads. Tables I and II give the acceptable harmonic levels in current and voltage as prescribed in the standard.

Table I. IEEE-519 maximum odd harmonic current limits for general distribution systems, 120V through 69kV

$\frac{I_{sc}}{I_L}$	n<11	11≤n<17	17≤n<23	23≤n<35	35≤n	THD
<20	4%	2%	1.5%	0.6%	0.3%	5%
20-50	7%	3.5%	2.5%	1%	0.5%	8%
50-100	10%	4.5%	1.5%	0.6%	0.7%	12%
100-1000	12%	5.5%	5%	2%	1%	15%
>1000	15%	7%	6%	2.5%	1.4%	20%

Numerous methods have been introduced from passive filter approaches through multiple-pulse rectifiers to converter type utility interface to solve the power quality

Table II. IEEE-519 voltage distortion limits

Bus voltage at PCC	Individual harmonics	THD
<69 kV	3%	5%
69001-161 kV	1.5%	2.5%
>161 kV	1%	1.5%

degradation problems. Controlled converter type utility interface achieves harmonic-free power system with active approach to shape supply current by power converters.

One topology is to replace the diode rectifier by the PWM voltage source rectifier (PWM-VSR) that has a built-in solution of input harmonic problems, shown in Fig. 2.

The front-end PWM-VSR performs ac-dc power conversion as well as draws sinusoidal current waveforms from the utility. The other configuration is to connect the active power filter (APF) in parallel with the diode rectifier. The APF, illustrated in Fig. 3 injects both harmonic and reactive current components to the diode rectifier. Consequently, the utility can provide the only sinusoidal supply current with unity displacement factor.

Although both converters perform unity power factor operation with sinusoidal input currents, the operational principles are quite different. The PWMVSR is based

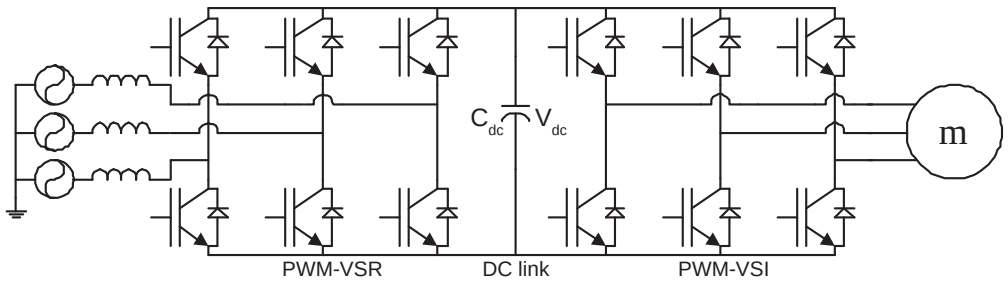

Fig. 2. PWM-VSR

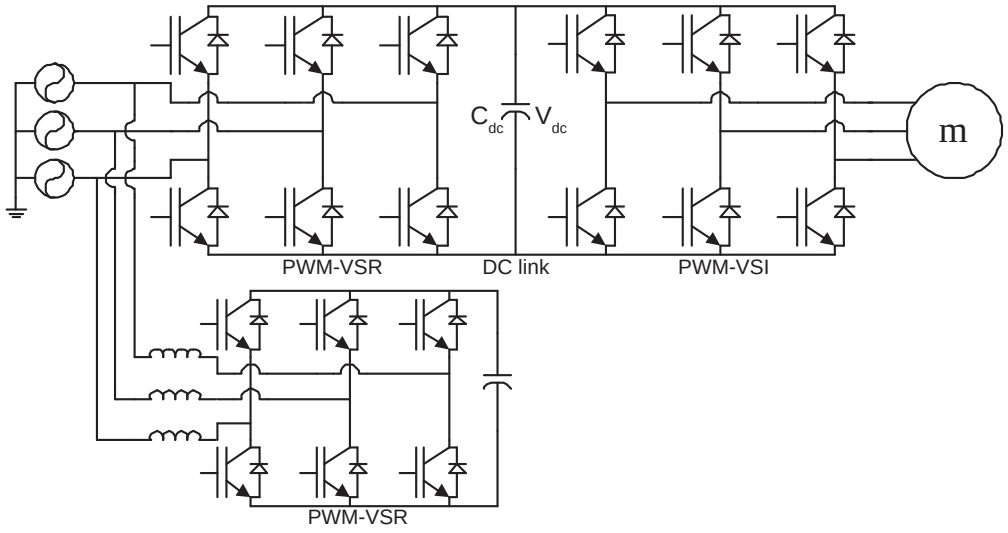

Fig. 3. PWM-VSI with APF

on direct sinusoidal current generation, whereas the APF works on the principle of load harmonic compensation. As a consequence, the PWM-VSR deals with the real power, whereas the reactive and harmonic powers of the diode rectifier are supplied by the APF.

2. Direct ac-ac conversion

The matrix converter is a direct ac-ac power converter, which connects supply ac utility to output ac load through only controlled bi-directional switches. The output ac signals with adjustable magnitude and frequency are constructed by single-stage power conversion process. The direct ac-ac power conversion principle of the matrix converter leads to the distinct structure with no large dc-link energy storage components. Consequently, the matrix converter topology can be implemented with compact size and volume compared with the diode rectifier based PWM-VSI, where the dc-link capacitor generally occupies 30 to 50 % of the entire converter size and volume. This feature is very promising to the modern low-volume converter trend

with high silicon integration. A three-phase matrix converter is shown in Fig. 4.

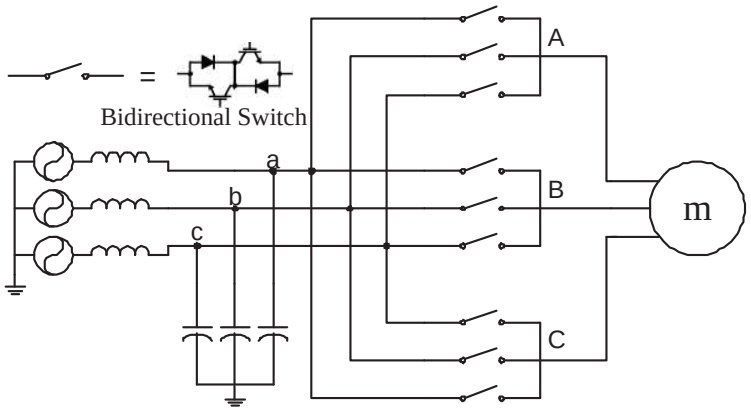

Fig. 4. Matrix converter

In addition to its compact design, it can draw sinusoidal input currents with unity displacement factor as well as sinusoidal output currents. The converter provides inherent bi-directional power flow capability so that load energy can be regenerated back to the supply. Moreover, the matrix converter can operate at high temperature surroundings due to the lack of dc electrolytic capacitors, which is very vulnerable in high temperature. The converter also has a long lifetime with no limited-lifetime capacitors [13]. The converter configuration consists of nine bi-directional switches, which are arranged to connect any of input terminals a, b, and c to any of output lines A, B, and C.

As the matrix converter structure is an array of switching devices connecting input source and output load, input and output sides are directly linked, in contrast with the diode rectifier based PWM-VSI separated by the dc-link capacitor. This aspect makes the modulation control of the matrix converter quite different and complicated, compared to other indirect ac-ac power converters. As a result, modulation techniques to control the matrix converter have been, last two decades, intensively

researched and reported since the advent of Venturinis early method [14]. Two switching control strategies, Venturini method and Space Vector Modulation method (SVM) have been well established to obtain satisfactory input/output performances [14, 15].

In spite of numerous merits presented, the industrial acceptance of the matrix converter has been held back because it is not suitable for use with standard loads on standard supplies due to its maximum input/output transfer ratio limited to 86%. In addition, many switching devices and gate drives, expensive system realization, increased complexity of control and current commutation, and sensitivity to input voltage disturbance have limited industrial interest in the matrix converter [13]. Therefore, the matrix converter has been expected to realize in practice for special applications where its advantages can offset the drawbacks, rather than general-purpose ac-ac power converter. Most potential practical implementation of the matrix converter has been considered aerospace, navy, and military applications, where reduced space and weight along with high-temperature operation are at a premium over cost and complexity penalty [16].

3. Six-step current fed converter

The converter power rating is closely tied to switching devices used in the converter topology. Even if gate-turn-off switching devices have been considerably improved, the switching characteristics are still far from being ideal, resulting in high switching losses from high-frequency hard switching operation.

Thyristors (or silicon-controlled-rectifier), invented by Bell Laboratory in 1956, possess the largest power handling capability and are indispensable in high-power, low-frequency applications [2]. Power converter topologies with basis of thyristors have been traditionally used in high power utility system and multi-MW ac drive applications for which IGBT-based topologies with PWM operation are impractical

due to device limitations. It appears that the dominance of thyristor in high power areas will not be challenged at least in the near future [4].

Thanks to thyristor characteristics and its soft switching operation, the thyristor based topologies have performance merits including simplicity, easy control, high efficiency, reliability, cost effectiveness, and very low switching losses [17–19]. Moreover, because of its current-source inverter structure, it holds inherent advantages of CSI:
1) short-circuit protection: the output current is limited by the regulated dc-link current
2) high converter reliability, due to the unidirectional nature of the switches and the inherent short-circuit protection
3) instantaneous and continuous regenerative capabilities due to the controlled rectifier [18].
Because of all these features, the thyristor-based converters have been, so far, the favorable power converter topology in high power applications, with available switching devices at high power rating.

A basic schematic configuration of a six-step current-fed converter based on thyristors is shown in Fig. 5. It consists of a three-phase controlled rectifier at input side and a current source inverter (CSI) at the output side with a dc-link inductor. The amplitude of the currents supplied to three-phase ac loads is controlled by adjusting the firing angle of the phase-controlled rectifier. The dc-link inductor reduces the current harmonics and ensures that the input of the CSI and hence, to the load appears as a current source. The thyristor-based inverter can control only the fundamental frequency of load currents by selecting the gating instances of thyristors. The thyristors in the inverter turn on and off only once per cycle of the load current, and consequently, the inverter operates in the six-step mode.

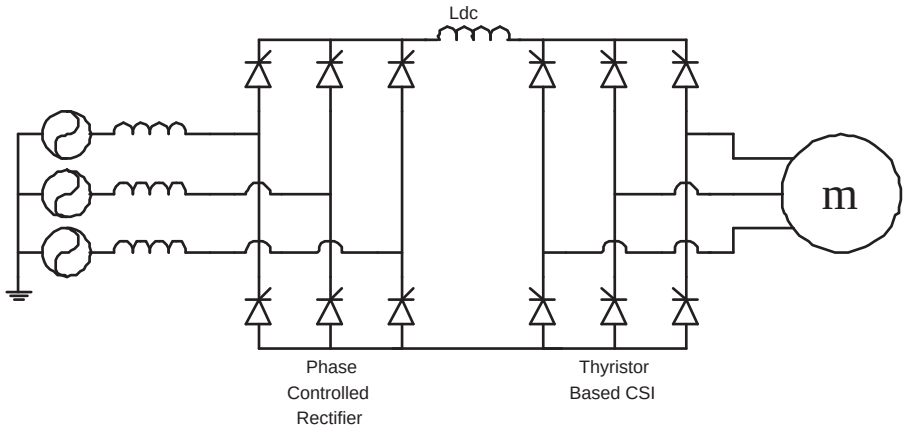

Fig. 5. Six step current fed converter

C. Ac-link converters

High frequency ac-link converters have been suggested as an improved alternative to dc-link converters. Here, the traditional dc-link is replaced by a resonant ac-link formed by an inductance and a capacitance in parallel. Fig. 6 gives a block diagram representation of a general ac-link converter.

A high-frequency link allows the flexibility of adjusting the link voltage to meet the individual needs of the source and load sides and at the same time provides isolation between the two [20]. High frequency link converters improve the speed of response, and if the frequency is outside the audible range, reduce acoustic noise [6]. Because of the typically high frequency of operation of the link, their component sizes are small.

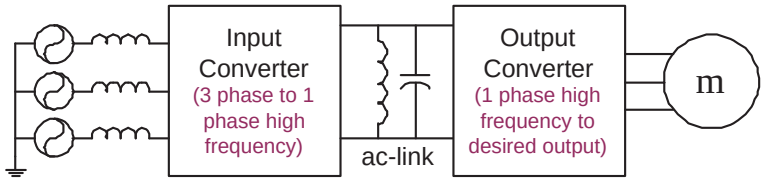

Fig. 6. Block diagram representation of typical ac-link converter

1. Converter requirements for ac-link topologies

High frequency link power converters are receiving increasing attention as an alternative to the more conventional dc link power conversion systems. Use of a high frequency ac voltage link in a power conversion system permits adjustment of the link voltage to meet the individual needs of loads/sources in the system, allows stepping up of the voltage in sections, and realizes electrical isolation. By operating the link at a high frequency, the system can be made compact because of the large reduction in the size and weight of transformers and other passive components needed for filtering and temporary energy storage functions.

Converters not designed specifically for operation from a high-frequency link are unlikely to perform adequately as interface converters for high frequency link systems. Consider, for example, the phase controlled converters (cycloconverter) which is frequently used when one-step pwer conversion from an ac voltage source is required. A major limitation of such a converter in a high-freqeuncy link system would be the excessive switching losses resulting from a high switching rate (forty thousand switches per second for a 20-kHz link) and an inherently high loss per switching of the phase-angle control scheme. In addition, phase-controlled converters cause a varying (and lagging, if naturally commutated) current to be returned to the link, making it more difficult to regulate the link, and contain objectionable levels of $\frac{dV}{dt}$'s in the generated voltage waveforms.

Intermediate dc link converters are possible which might operate by converting the high-frequency link power to an intermediate dc form from which another dc input converter would then generate the desired low-frequency ac or adjustable amplitude dc. However, such two-stage topologies are inherently less efficient and tend to have limited capabilities in such aspects of converter performance as output frequency

limit, converter bandwidth, ease of protection, reliability, and others due to the hard switching used in dc link converters.

2. Development of ac-link converters

High frequency link power conversions have been employed very successfully in dc-to-dc converters. Their enormous success has demonstrated the benefits and to some extent the difficulties of working at high frequencies. In particular, problems arise from the limitations of both the components and the circuit topologies. As the demand has grown and the technology has matured, there has been a large improvement in the quality of components. High quality capacitors, good magnetic materials for design of compact low-loss inductors and semiconductor devices designed especially for high-power applications have become available. This trend can be expected to continue with further improvements in performance and even larger gains in the cost and availability of these components.

Ac-ac and dc-ac converters employing high frequency ac links have also been reported [21–24]. Most of these converters are designed for specific type of source/loads. Reference [20] reported a topology that provided one-step bidirectional power conversion for different kinds of loads/sources. This configuration used twelve bidirectional switches and employed Pulse Density Modulation (PDM) as a means to control the currents. The use of PDM reduces the system response because of usage of integral pulses of currents. Topologies that make use of twelve unidirectional switches, by providing a dc offset to the dc link, have also been suggested. Reference [25] proposes a topology with twelve unidirectional switches, without the dc offset. Fig. 7 shows this topology.

It consists of a 6 switch input converter and a 6 switch output converter. Fig. 8 shows the link waveforms for this converter. Input phases charge the link and

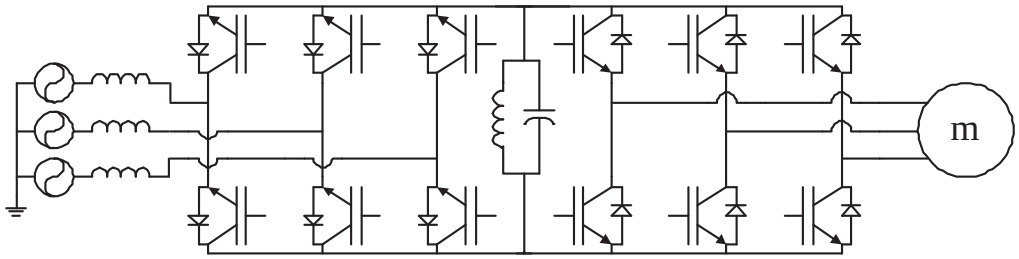

Fig. 7. Ac-link topology with unidirectional switches

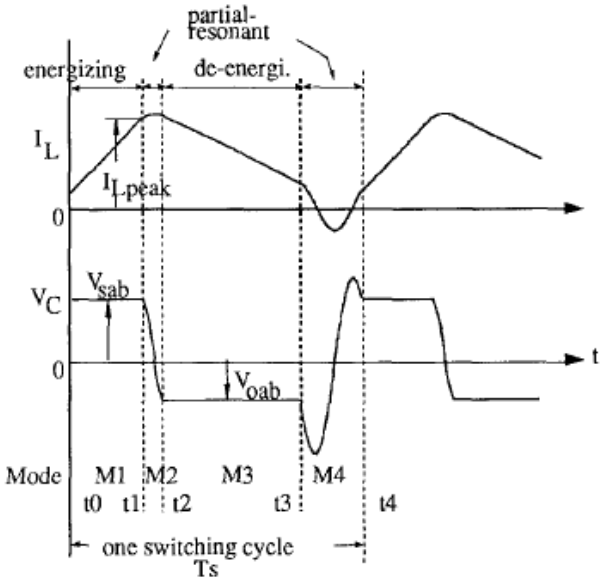

Fig. 8. Waveforms explaining operation of topology in Fig. 7

it discharges into the output. Input and output currents pulses are modulated so as to result in a sinusoidal shape on filtering. Because of the links unidirectional nature, there is a large dead time due to the resonant 'fly back' which reduces the power capability by about 30%. It is also limited in operation response due to its inability to supply output current at low voltages or power factors, at link frequencies sufficiently high to avoid input/output filter resonances.

D. Research objective

A new ac-link converter topology is proposed. It uses 12 bidirectional switches for a three phase to three phase topology with an ac-link formed by an inductor capacitor pair.

The objective of this thesis is to develop a control scheme for the ac-link converter. The suggested control scheme will have complete soft switching with high input power factor and power quality. At the start a very specific switching sequence that gives satisfactory operation will be developed. Satisfactory operation here means high efficiency and close to unity input power factor. This will later be used to develop a more general switching and control scheme that works well with different operating conditions.

Design of the converter components along with the design of filters and corresponding damper circuits will be done. The proposed topology uses anti-series IGBTs to form the bidirectional switches. IGBTs have a long tailing current at turn off that leads to significant switching losses. The effect of the value of link capacitance on this will be studied along with detailed loss calculations to accurately predict the efficiency of the prototype under construction.

The suitability of this topology for ac-dc and dc-ac applications will also be shown.

E. Thesis outline

This thesis is organized into five chapters. The first chapter discusses existing converter topologies for ac to ac power conversion and also discusses the development of high frequency link converters. In the second chapter, the proposed topology is looked at. Design, principle of operation and the switching algorithm are looked at in this chapter. Performance evaluation of the converter in terms of efficiency is discussed in the third chapter. The fourth chapter discusses suitability of the converter for wind and solar power applications. The final chapter discusses simulation and preliminary experimental results of the converter.

CHAPTER II

PROPOSED SOFT SWITCHING AC-LINK CONVERTER

A. Introduction

In this thesis, work done on the development of a novel soft switching ac-link converter is presented. Fig. 9 shows a simple schematic of the converter. Each leg of

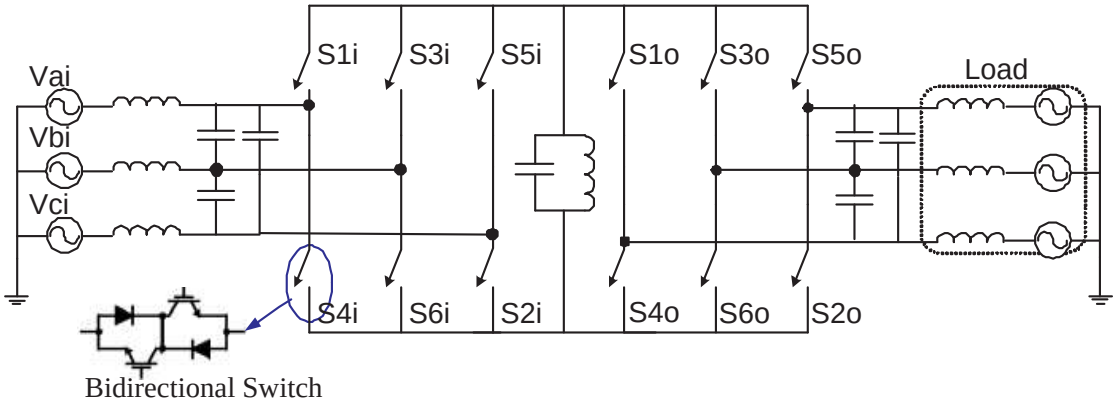

Fig. 9. Schematic of proposed topology

the converter uses 2 bidirectional switches.

The link is formed by a low reactance inductor-capacitor pair. The converter operates by charging the link from the inputs and then discharging the stored energy to the output. Bidirectional switches could be realized by anti-series IGBTs and diodes for lower power configurations. SGCTs or IGBTs rated to 5500 V or more could be used for medium voltage (2300 VAC and up) high power applications. For voltages greater than 2700 V, switches could be operated in series.

B. Principle of operation

To put it simply, the link is charged by the input phases and the link thus charged, discharges into the output phases. Charging and discharging take place alternately. This frequency of charge/discharge is called the link frequency and is typically much higher than the input/output line frequency. For example, with the semiconductor devices currently available, a 20 HP drive which operates from a 60 Hz utility supply can have a link frequency of about 10 kHz. The resulting input and output current pulses have to be precisely modulated such that when filtered, they achieve unity power factor at the inputs while meeting the output references. Fig. 10 shows a block diagram representing the functioning of the system. The converter is fed with output current references. The link is charged to an amount which makes the discharging current exactly meet these references. Charging and discharging take place separately, hence, an estimate of how much the link needs to be charged to supply the output correctly is required. The controller handles this by translating the output references to input references. The input reference is derived by the simple equation that

$$Input\ power = Output\ Power + Losses \tag{2.1}$$

This is described in Fig. 10. RMS values of the output reference currents, output and input voltages are used to determine the RMS of the input currents for an ideal converter. A loss component is added to this from the loss estimator to get the exact input command currents as in (2.1).

The instantaneous value of the output reference commands could be phase shifted with respect to the output voltages as the load demands. Normally, the instantaneous values of the input current commands are in phase or are phase adjusted with respect to the input voltages so as to achieve unity power factor.

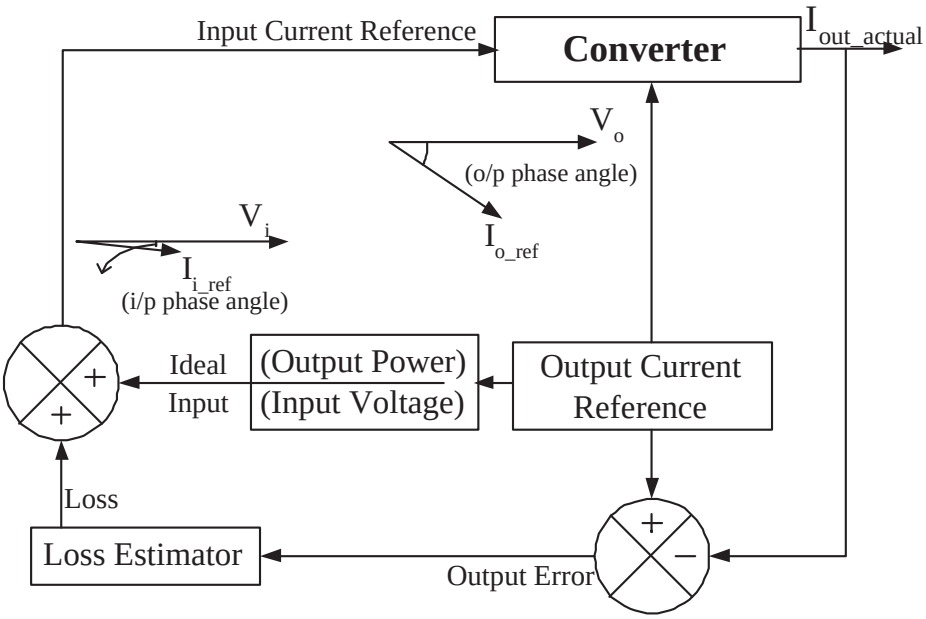

Fig. 10. Deriving input current reference

1. Phase selection and switching sequence

While charging the link, the converter works with the input current references, while during discharge, it works with the output current references. During charge or discharge, appropriate switches are turned on so that the line voltage of the selected 'phase pair' is directly applied across the link. Phases that charge and discharge the link for each link cycle are chosen using some fundamental properties of 3 phase waveforms. As a general case, a situation where the voltages and respective current references are out of phase is considered. The following example is for charging the link. It is easy to use this to explain choice of phases for discharging as well. Consider the case shown in Fig. 11. In this, consider the instant shown by the vertical black line in Fig. 12.

At this instant, Iaref = 12 A, Ibref = -4 A and Icref = -8 A. The link cycle at this instant (link frequency << line frequency) must be such that the charging currents

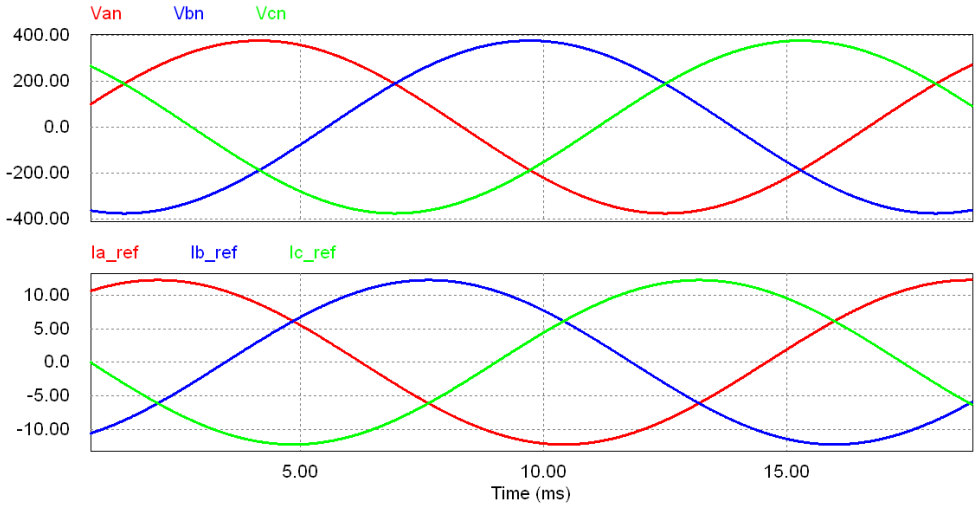

Fig. 11. Voltage and phase shifted current references

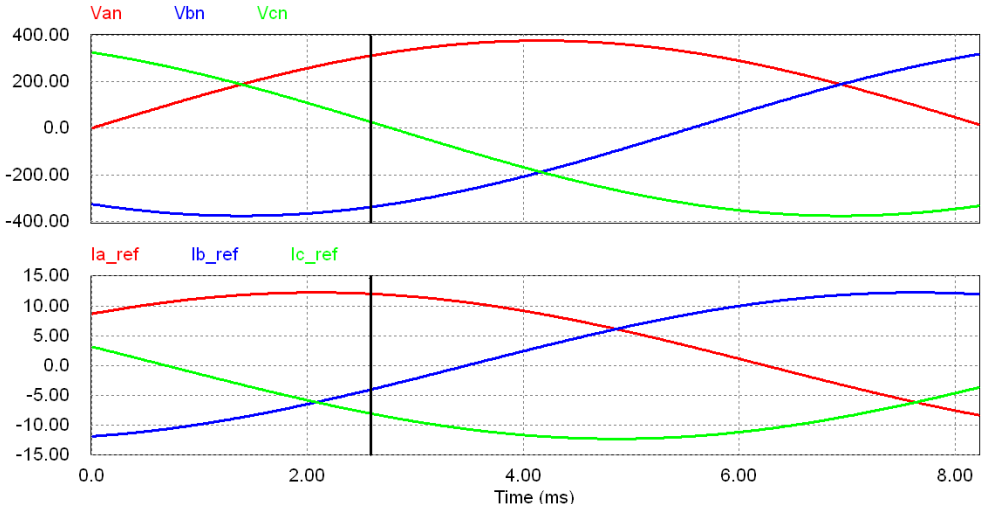

Fig. 12. Instant under consideration

are split up to meet the reference values given by Iaref, Ibref and Icref. If the link is charged by line AB till phase B delivers -4 A on average and by line AC till phase C delivers -8 A on average, then phase A would have delivered 12 A on average. Computation of average current is made simpler by handling these reference currents in terms of reference charge. The reference and actual currents are integrated to give the respective charges. Charging takes place till their difference of these charges reaches zero. Hence the phase pairs that charge are decided based on the reference currents at the start of the link cycle.

The link is charged and discharged alternatively. Based on the discussion in the previous section, charging/discharging is has to be done with two pairs of phases. In the example above, AB and AC are the chosen phase pairs based on the instantaneous current reference values. Note that BA and CA would have been the chosen phase pairs if the reference currents were Iaref = -12 A, Ibref = 4 A and Icref = 8 A. Fig. 13 shows Vab and Vac along with the phase voltages.

Here it is seen that at the instant under consideration, Vab > Vac. Vab is in this case chosen as the first phase pair that charges the link. Once charge reference of phase B meets the actual charge taken from phase B, charging from AB is stopped. Next the link is charged from Vac till charge reference of C is met. How the logic exactly works and why this particular sequence is chosen is explained in the next section.

C. Modes of operation

Each link cycle is divided into 16 modes. There are 8 power transfer modes wherein power is transferred to or from the link and 8 partial resonant modes where there is no power transferred to (from) the link from (to) the input (output). Fig. 14

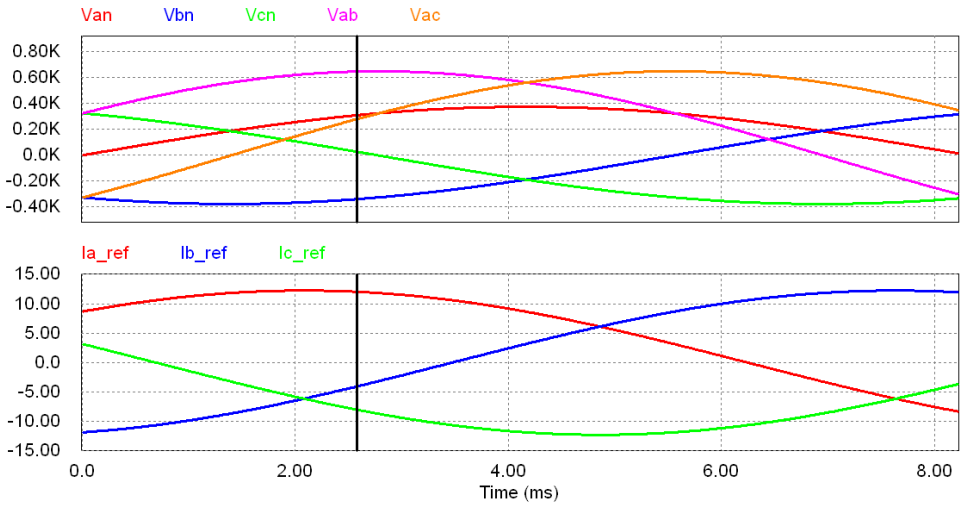

Fig. 13. Phase sequencing

shows the important current and voltage waveforms over one link cycle. There are three basic operations taking place through the 16 modes: energizing, partial resonance and de-energizing. The link is energized from the inputs during modes 1, 3, 9 and 11 and is de-energized to the outputs during modes 5, 7, 13 and 15. Modes 2, 4, 6, 8, 10, 12, 14 and 16 are the partial resonant modes and as evident from Fig. 14, they make up only a very small fraction of the link cycle time. The various operating modes are explained below.

Mode 1 (*Energizing*): As discussed in section xyz, of the chosen phase pairs, the one having the highest instantaneous voltage charges the link first. The link is connected to this input voltage pair via switches which charge it in the positive direction. For the waveforms shown in Fig. 14, the link is connected to input phase pair BC through switches S3i and S2i. The link charges till the charge reference of phase B

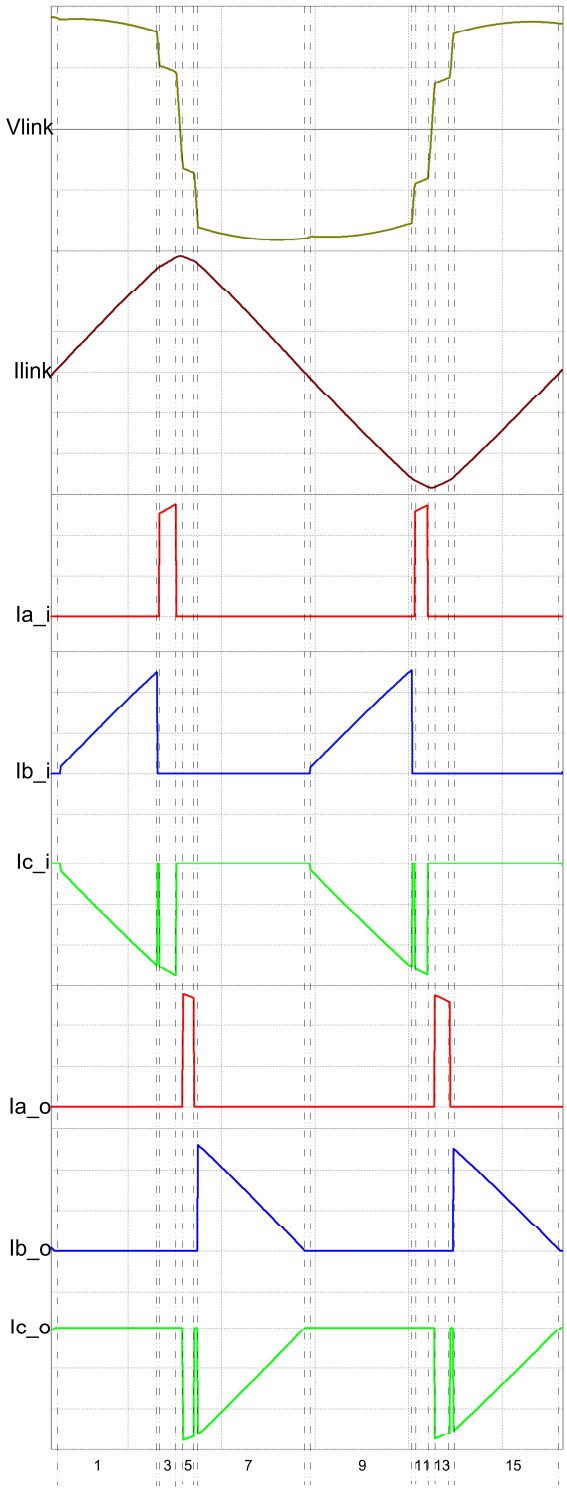

Fig. 14. Typical waveforms illustrating the operating principles of the proposed converter

meets the actual charge into the link. The switches are then turned off.

Mode 2 (*Partial resonance*): The link capacitance acts as a buffer across the switches during turn off. This results in low turn off losses. All switches remain turned off and the link resonates till its voltage becomes equal to the voltage of the second chosen phase pair. This is the phase pair the link charges next from. In the example shown in Fig. 14, the link resonates till the link voltage becomes equal to Vaci.

Mode 3 (*Energizing*): Switches are turned on to allow the link to continue charging in the positive direction from the second input phase pair. At the end of mode 2, the link voltage equals the voltage of this phase pair. Hence at the instant of turn on, the voltage across the corresponding switches is zero. This implies that the turn on occurs at zero voltage as the switches transition from reverse to forward bias. In the example in Fig. 14, The link charges till the charge reference of phase C meets the actual charge into the link. The switches are then turned off.

Mode 4 (*Partial resonance*): During this mode the link is allowed to swing to one of the output line voltages. To explain how the sequence of chosen phases is selected, the logic behind the selection of the phases is explained here again. The sum of the output reference currents at any instant is zero. One of them is the highest in magnitude and of one polarity while the two lower ones are of the other polarity. The converter uses this simple property to avoid any resonant swing back in the link. It is desired to keep the partial resonant periods as small as possible to increase the net power transfer. Hence, it is important to avoid complete resonant swings in the link. The charged link transfers power to the output by discharging into two output phase pairs. The two phase pairs are the one formed by the phase having the highest ref-

erence current and the second highest reference current, and the one formed by the phase having the highest reference current and the lowest reference current, where the references are sorted as highest, second highest and lowest in terms of magnitude alone. For example, if $Iao = 10$ A, $Ibo = -7$ A and $Ico = -3$ are the three output reference currents then phase pairs AB and AC are chosen to transfer power to the output. If Vab_o and Vac_o are the instantaneous voltages across these phases and Vlink is the link voltage, the phase pair whose voltage has minimum difference with respect to Vlink is chosen as the first one to discharge to. For example if $Vlink = 500$ V, $Vab_o = 400$ V and $Vac_o = 300$ V, AB is chosen as the first phase pair to discharge to. This generally translates to choosing the phase pair having the highest instantaneous voltage of the two selected pairs.
Fig. 15 shows the circuit conditions for modes 1 through 4.

Mode 5 ($De - energizing$): The output switches are turned on at zero voltage to allow the link to discharge to the chosen phase pair till the reference charge of the lower phase is met.

Mode 6 ($Partialresonance$): All switches are turned off and the link is allowed to swing to the voltage of the other output phase pair chosen during Mode 4. For the example discussed before, the link voltage swings from Vaco to Vbco. This is also illustrated in Figure 6.

Mode 7 ($De-energizing$): During mode 7, the link discharges to the selected output phase pair till there is just sufficient energy left in the link for it to swing to the input phase pair having the highest voltage. When the losses are determined accurately, this would mean that the output references are accurately met. Any deviation from

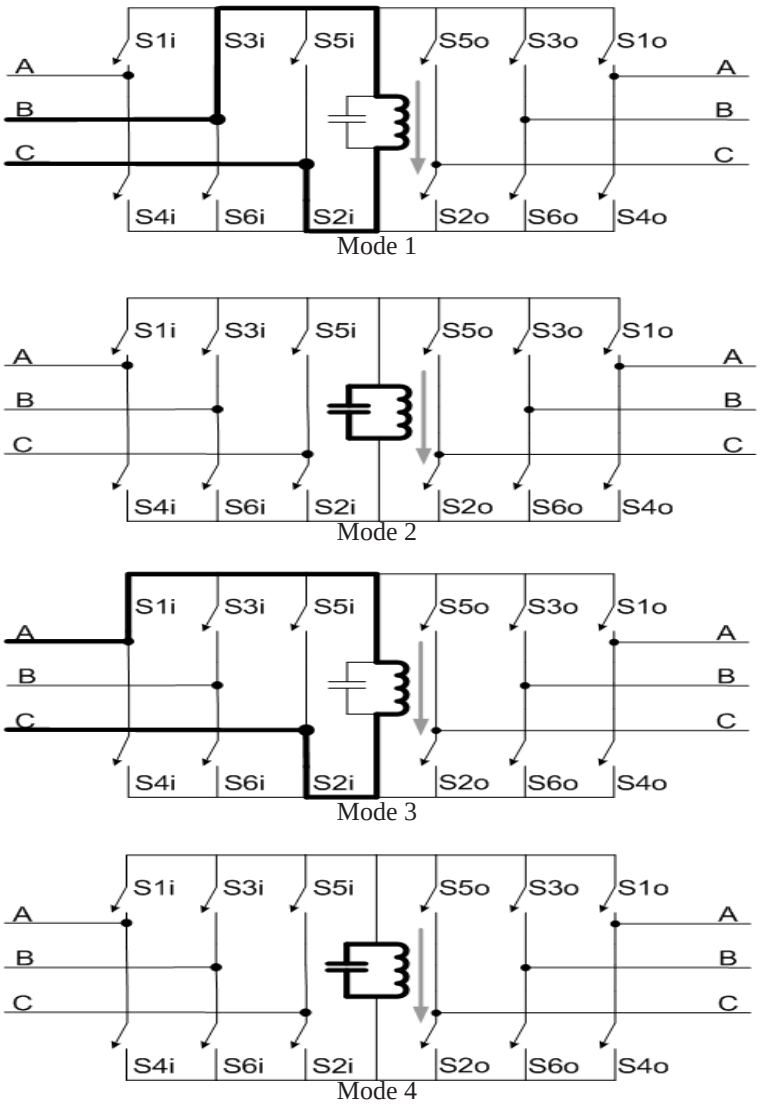

Fig. 15. Modes 1 to 4 of operation

this is detected and the losses re-estimated to eliminate this error.

Mode 8 (*Partialresonance*): The link swings to the input phase pair having the highest voltage to be ready to charge the link in the reverse direction. Fig. 16 shows the circuit conditions for modes 1 through 4.

Modes 9 through 16 are similar to modes 1 through 8, except that the link charges and discharges in the reverse direction. For this, the complimentary switch in each leg is switched when compared to the ones switched during modes 1 through 8. This is seen comparing Fig. 15 and Fig. 16 with Fig. 17 and Fig. 18.

It is observed that the input is never directly connected to the output resulting in proper isolation between the two. Fully galvanic isolation can be achieved by using an isolation transformer in place of the link inductor. It can also be observed that the converter can operate without that link capacitor. However, since the topology is tolerant to such capacitance, a low cost, light weight, and efficient link inductor with high parasitic capacitance can be used. The inductor being used in a 15 kW three phase prototype weighs less than 5 Kg, with less than 3 Kg for the input line reactance, as compared to over 70 Kg for the input and output filters alone for a 15 kW VS-PWM drive required to produce comparable low harmonics on the input and output. Additional capacitance may be advantageously added to buffer turn-off losses, with the optimal link capacitance determined by balancing reduced turn-off losses against the resulting slight decrease in power throughput.

The converter can also operate consistently during input voltage sags. As can be noticed, for lower input voltages, the charging period of the link will increase to allow the link to charge sufficiently. Though this will result in slightly lower link frequency during the sag, it is still sufficient to supply the outputs with acceptable precision.

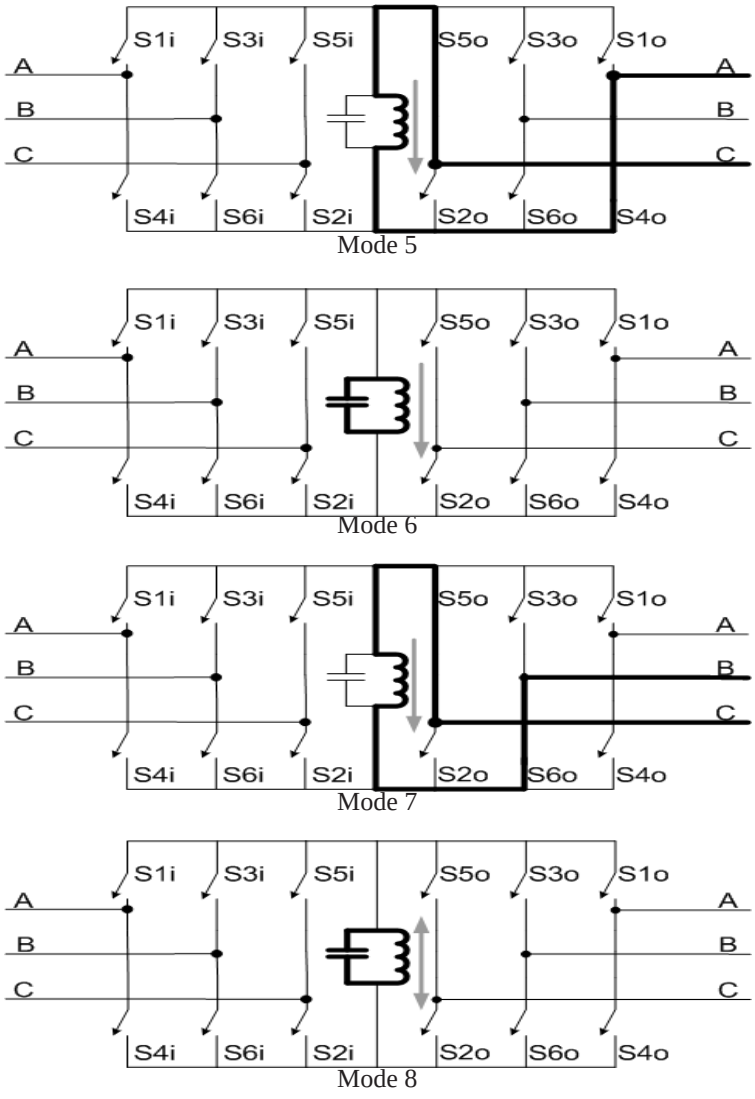

Fig. 16. Modes 5 to 8 of operation

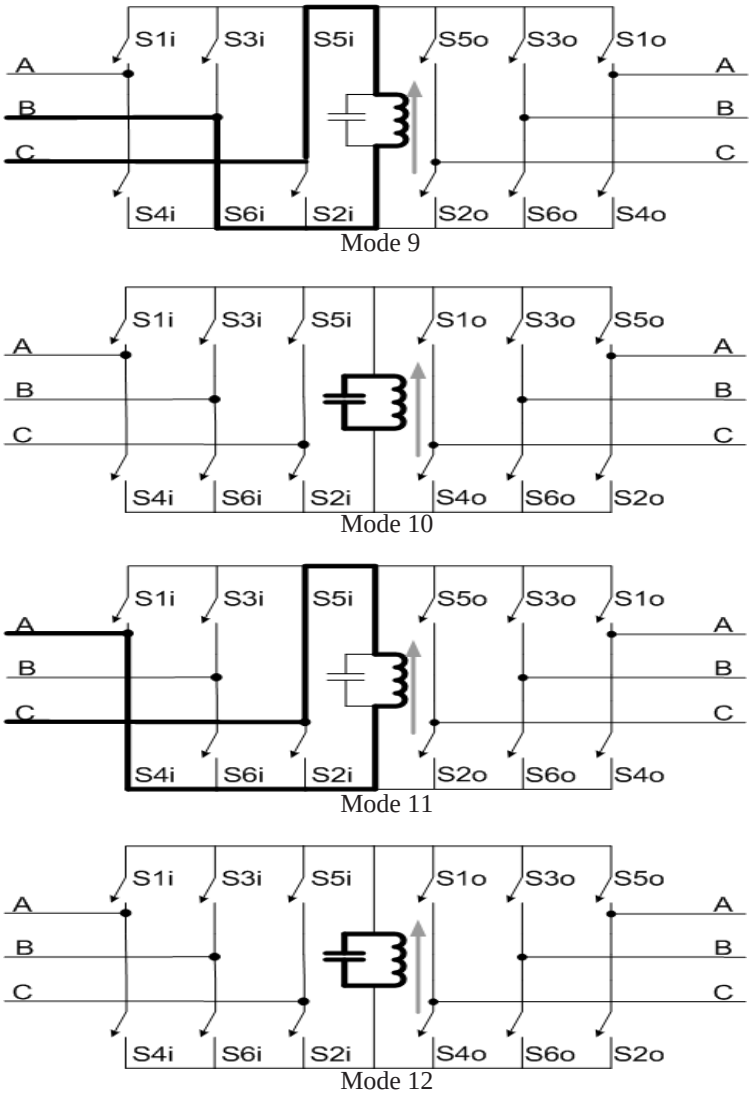

Fig. 17. Modes 9 to 12 of operation

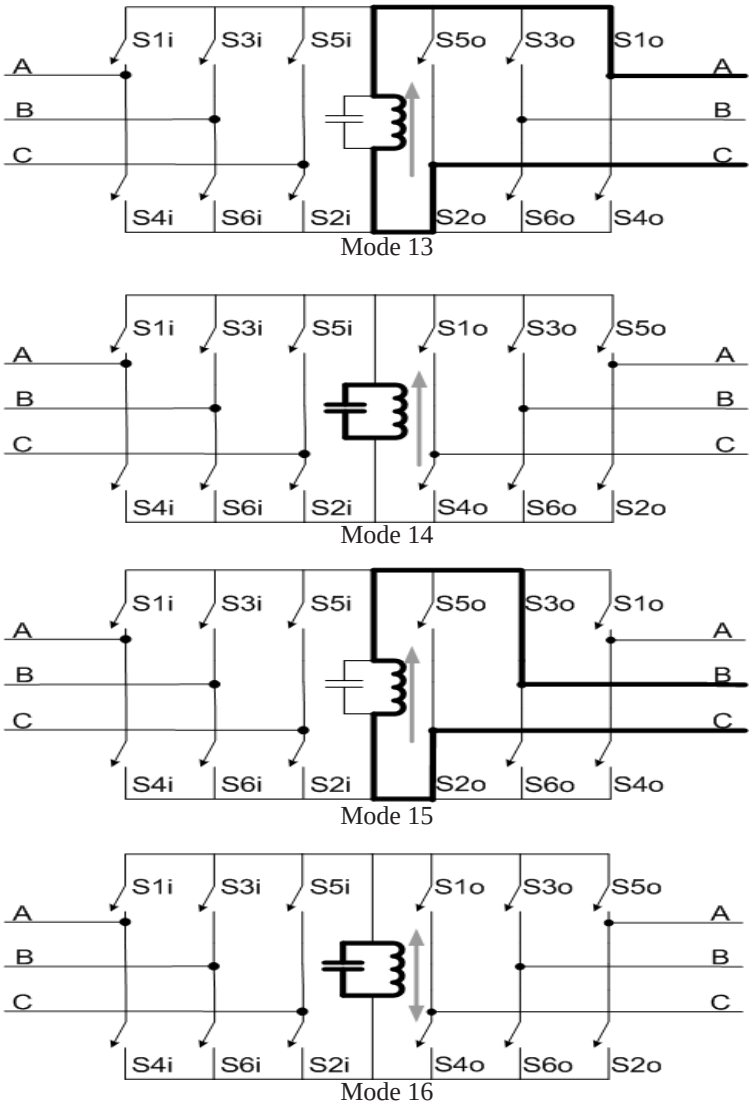

Fig. 18. Modes 13 to 16 of operation

D. Development of a generic control scheme

Initial simulations that were carried out utilized a lot of CPU time as the logic continually polled for the different modes of operation. Later on, a new and simpler method was developed and its working proved. This method also has an advantage that all switch turn on events occur whenever the particular switch goes from reverse bias to forward bias. To be more clear, gating pulse is provided while the switch is reverse biased; hence it does not turn on. The gate signal is held till circuit conditions make the switch forward biased and eventually turns on. This results in a diode like turn of the switch resulting in the lowest turn on losses.

At the start of the link cycle, depending on the sign of the reference currents for each phase, the lower or upper switch for each phase is held on. As the link voltage swings, only two switches get forward biased while the others are reverse biased. These switches are automatically turned on and the link is charged via these as in mode 1. Of the two phases that charge the link, one of them meets its reference value first. The switch corresponding to this phase is turned off to allow the link to swing as in mode 2. As it swings, it forward biases the other two switches to charge the link via the other phase pair as in mode 3. During this, when the other reference current is met, both switches are turned off to enter mode 4.

During the start of the link cycle itself, it is good to keep even three output switches gated on. Again, these three switches are based on the polarity of the output phase reference currents. The converter enters modes 5 through 8 similar to modes 1 through 4 explained above.

As it is seen, the control is simplified to a great extent because all that needs to be taken care of is turning 1 or 2 switches off when their particular reference is met. Turning on of the switches occurs automatically as the switches get forward biased

resulting in very low turn on losses.

E. Design of components

This section discusses the design of the proposed converter. Power semiconductor switches for the required level have to be first chosen. With their characteristics in mind, the link frequency, link components and filters are designed.

1. Design of power electronic switches

Switches have to be rated considering the maximum voltage and current they have to withstand. While the voltage on each switch does not exceed twice the peak of line to neutral voltage, each switch has to be rated to carry at least four times the RMS of the input or output currents. This is because of two things. Firstly, charging (discharging) from takes place only for one half of the link cycle. Secondly, average of a triangular wave is half its peak.

To summarize, switches have to be rated to withstand twice the peak phase voltage and carry four times the RMS of the phase currents.

2. Choice of link frequency

Based on the switching capability of available devices for the required power range a suitable link frequency is chosen. With presently available switches as 15 kW converter can have a link frequency of 10 kHz and a 2 MW converter can have a link frequency of about 3 kHz. The link inductance is chosen based on the voltage and power level so as to satisfy the simple equation that V=Ldi/dt. The link capacitance is chosen so as to keep the partial resonant periods less than 5% of the link cycle period.

3. Design of link inductor and capacitor

As an example, a three phase 15 kW, 460 V system is considered. Link frequency is chosen as 10 kHz. As seen with the different modes of operation, the link is charged by two phase pairs. To handle this, the average voltage resulting from a three phase supply is considered. This is 1.35 times the rms line to line voltage as in (2.2).

$$\begin{aligned} V_{avg} &= 1.35 \times V_{LL} \\ &= 1.35 \times 460 \\ &= 621V \end{aligned} \tag{2.2}$$

For simplicity, the system is designed for equal input and output voltages. The first step is to design the link inductor. For this the simple equation that the rate of change of current times the inductance is the voltage applied is used.

$$\begin{aligned} V_{avg} &= L \times \frac{dI}{dt} \\ &= L \times \frac{I_{peak}}{T/4} \\ &= 4fLI_{peak} \end{aligned} \tag{2.3}$$

For a 15 kW, 460 V three phase system, the peak phase current is 26.62 A. Considering the first half of the link cycle in Fig. 14, it is seen that output is supplied only during one half of it. It is a fairly accurate to assume that the current rises and falls linearly. With respect to the peak link current, average value of current discharged is halved once due to output being supplied only during one half of the time, and halved for the second time since the current is linearly increasing. Hence, peak link current is calculated as in (2.4).

$$I_{peak} = 4 * 26.62 = 106.48A \tag{2.4}$$

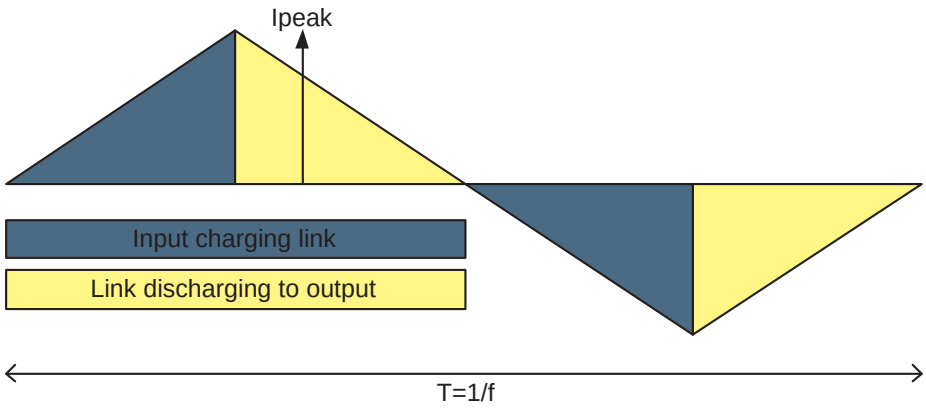

Fig. 19. Charging and discharging of link during a link cycle

From the value of chosen link frequency and (2.2),(2.3) and (2.4), link inductance is calculated as given in (2.5).

$$\begin{aligned} L &= \frac{V_{avg}}{4 f I_{peak}} \\ &= \frac{621}{4 \times 10k \times 106.48} \\ &= 145\ \mu H \end{aligned} \tag{2.5}$$

The link inductor carries high frequency and high magnitude currents. To handle these it is suggested to use an air core inductor as it avoids core loss as well as saturation. Resistance of the conductors used to wind the inductor can result in extra losses. Skin effect additionally increases the effective resistance of the winding at high frequencies of operation. To minimize this, it is suggested to use Litz wire to construct the inductor. Fig. 20 shows the link inductor used for a 15 kW prototype under construction. It is a spiral wound coil of Type 8 Litz wire with a dc resistance of 15 mΩ, and inductance of 100 μH, and a resulting free-air Q-factor of 125.

It is important to consider the boost capability of the converter. Theoretically, the output voltage can be Q-factor of link inductor times the input voltage. However,

Fig. 20. 100 μH link inductor for 15 kW prototype

on-resistance of the switches and other practical resistances in series with the link inductor reduce the equivalent Q factor.

Link capacitor is chosen so as to keep the resonating periods within 5% of the link cycle. As can been seen from the modes of operation, when the partial resonant modes are alone put together, the is one complete cycle. Choosing this period to be 3.33% of the link period, capacitance can be calculated as in (2.7).

$$\begin{aligned} f_{LC} &= \frac{1}{2\pi\sqrt{LC}} \\ &= 300\ kHz \end{aligned} \tag{2.6}$$

$$\begin{aligned} &OR \\ C &= \frac{1}{4\pi^2 f_{LC}^2 L} \\ &= \frac{1}{4\pi^2 300k^2 \times 145\mu} \\ &= 0.19\ \mu F \end{aligned} \tag{2.7}$$

4. Design of filters and dampers

The proposed converter generates current harmonics that are injected back into the ac system. These current harmonics can result in voltage distortions that affect the operation of the ac system. An input filter must be used for reducing these harmonics. Fig. 21 shows typical input current pulses.

The current pulses have a frequency of twice the link frequency as there are two

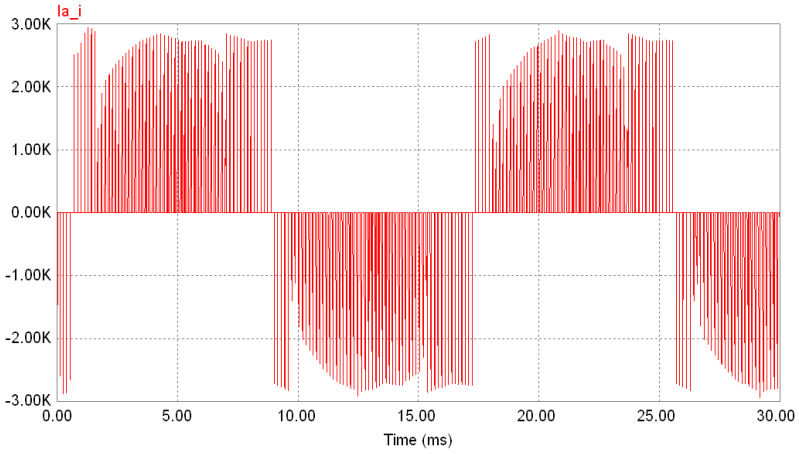

Fig. 21. Unfiltered phase current

sets of discharges into the phases (modes 5, 7, 13 and 15) during a link cycle. Fig. 22 shows the typical spectrum of unfiltered input currents. As seen in Fig. 22 there is a fundamental, switching components and its harmonics. Between the fundamental and the switching components exists a dead band in the harmonic spectrum where theoretically the harmonics are insignificant.

Practically, small harmonics exist in this band. The reasons for appearance of this unwanted harmonics are asymmetry in practical gating signals, switching delays,

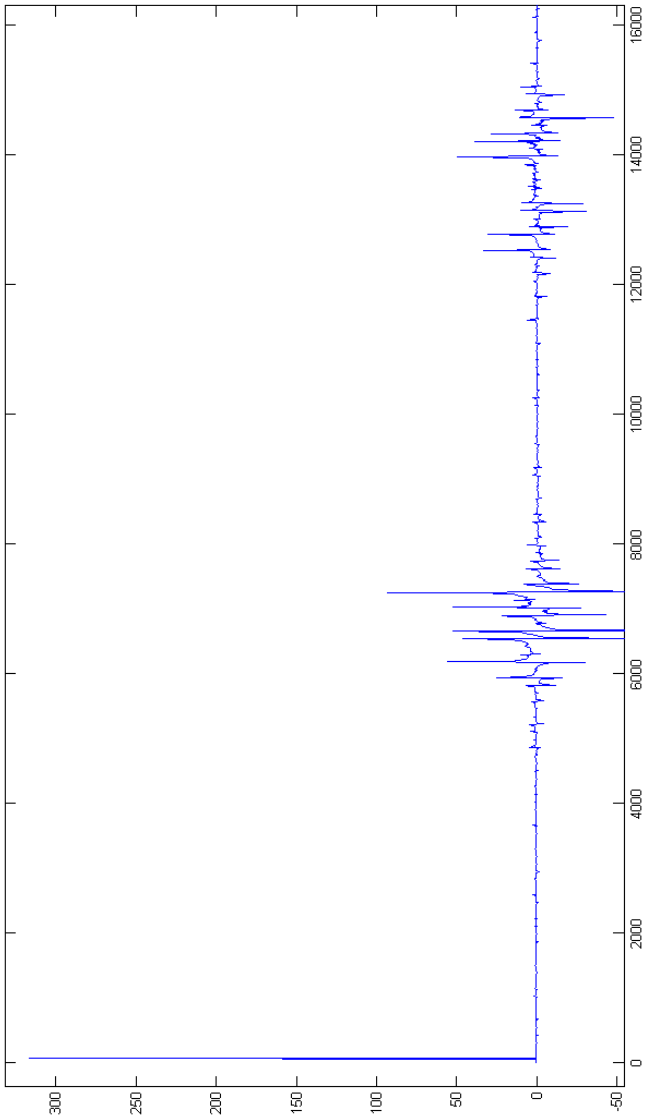

Fig. 22. Frequency spectrum of unfiltered phase current

asynchronism in the modulation method and other inaccuracies in the practical implementation of the control algorithm.

One method to prevent harmonics from affecting the utility is to use an LC filter. The reason for this choice is the simplicity of passive LC filters and their potential to meet the desired specifications with higher efficiency, small size and low cost. The capacitors provide a low impedance path for the high frequency ripple current and thus attenuate the content of current ripple in the utility current.

The main requirements an input filter has to meet are the following: required switching noise attenuation, keeping the input voltage from changing significantly during each PWM cycle, low input displacement angle between filter input voltage and current and overall system stability.

For this converter, cut-off frequency of the LC-filters is chosen to be less than at least one half of the link frequency. The final value is chosen after a trade off between the harmonic levels and the physical size limitations. For this example a cut-off frequency of 1500 Hz gives $L_f = 563\ \mu H$ and $C_f = 20\ \mu F$.

In order to avoid amplification of the residual harmonics in the dead-band region, damping of the LC filter is required. Proper filter pole dumping is important for achieving low filter output impedance for all frequencies and thus overall system stability and for avoiding amplification of the residual harmonics in the dead band.

For this converter, an damper circuit is added parallel to the filter capacitance. It is composed of an inductor, capacitor and resistor in series. The inductor and capacitor are chosen to have the same cut-off frequency as the original filter. For designing the resistor a Q factor, say 5, is first chosen. Now the inductor, capacitor and resistor are designed so as to satisfy three conditions in all: damper L-C should have the same cut-off as filter L-C; resistor should result in a Q factor greater than designed value; resulting total dissipation in the resistor is less than X % where X is

another design value, say 5 %.

Fig. 23 shows the frequency spectrum of the input current upon filtering. As it can be seen, the filter is successful is removing unwanted harmonics.

Calculation of harmonics using this plots results is a THD of 2.58 %. The filter capacitors carry harmonic currents at the switching frequency. The capacitors must withstand at least the peak line-neutral voltages. After deciding on the value of the capacitance needed for filtering, loss due to their equivalent series resistance (ESR) is calculated based on the level of the harmonic currents.

F. Summary

This chapter discussed the proposed converter in detail. The converter is constructed by bidirectional switches and an ac-link formed by a low reactive rating inductance-capacitor pair. Principle and different modes of operation were explained with relevant waveforms. Design of the converter and filter was also discussed.

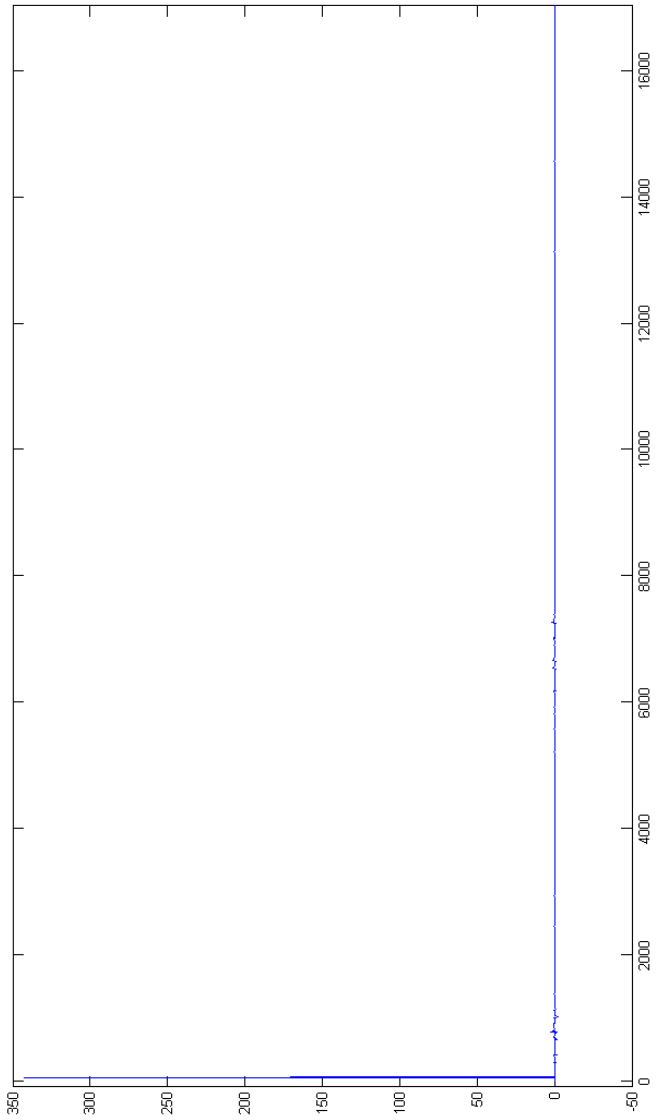

Fig. 23. Frequency spectrum of filtered phase current

CHAPTER III

LOSS ESTIMATION AND EFFICIENCY CALCULATION

A. Introduction

Loss estimation and efficiency calculation was done for a three phase to three phase, 2 MW, 2300 V converter. Knowing the voltage and current levels for the converter, a nominal link frequency is chosen based on the switching characteristics of commercially available switches and stray inductances. The chosen link frequency, the peak voltage and the peak current set the link inductance value. Link capacitance is chosen so as to limit the total partial resonant periods to about 5% of the link cycle. For the 2MW, 2300V medium voltage drive simulated, the parameters are chosen as in Table III.

Since all power is transferred through the link inductor power transferred

Table III. 2 MW converter parameters

Link frequency (f_l)	3500 Hz
Peak link current (I_p)	2800 A
Link Inductance (L_l)	73 μ H
Peak link current	2800 A

through the converter is simply the power through the inductor. With two power transfers per link cycle, this can be calculated with knowledge of the link frequency, the link inductance and the peak inductor current, given by (3.1).

$$\begin{aligned} P &= f_l L_l I_p^2 \\ &= 3500 \times 73\mu \times 2800^2 \\ &= 2003\ kW \end{aligned} \tag{3.1}$$

B. Conduction losses

Calculation of conduction losses is straightforward. Examination of the operating modes shows that only two switches conduct at any given time and the current is triangular, always linearly increasing or decreasing (ignoring the brief partial resonant periods). Conduction loss is given by the switch threshold voltage and the average current, and the switch incremental resistance with the rms current during the conduction interval as in (3.2).

$$\begin{aligned} P_{conduction} &= 2 \times (V_{sw} \times \frac{I_p}{2} + R_{sw} \times (0.577 \times I_{swpeak})^2) \\ &= 2 \times (3.5 \times \frac{2800}{2} + 0.0036 \times (0.577 \times 2800)^2) \\ &= 28.59\ kW\ (1.42\%) \end{aligned} \tag{3.2}$$

where, V_{sw} is the switch threshold voltage and R_{sw} is the switch resistance. This analysis assumes that the higher conduction loss fast recovery diodes in the module are replaced with low loss rectifier grade diodes, as fast recovery is not needed. For example, for normal motoring operation, reverse recovery does not occur at all until $\frac{1}{4}$ of a link cycle (71 μs for a 3.5 kHz link) after the recovering diodes have stopped conducting. Standard reverse recovery only occurs when the converter is boosting voltage from input to output, and then occurs at very low $\frac{dI}{dt}$ with the link capacitance buffering the reverse voltage drop after the diode starts blocking reverse voltage.

C. Parasitic inductance losses

Parasitic inductance losses occur due to the inductance of the link and link capacitors, the switch module, and connecting circuitry. Very low inductance laminated bus, low inductance modules and low inductance capacitors minimize this loss given by (3.3).

$$\begin{aligned} P_{ind} &= f_L \times 8 \times 0.5 \times L_{stray} \times I_p^2 \\ &= f_L \times 8 \times 0.5 \times 30\ nH \times 2800^2 \\ &= 3.28\ kW\ (0.163\%) \end{aligned} \tag{3.3}$$

Where 8 is the approximate number of stray inductance events per link cycle. As can be seen, losses due to stray inductance form a small percentage of the total power.

D. Turn off transition losses

Turn off losses were computed for ABBś 6500 V, 600 A IGBTs. The resulting hard turn-off waveform to match the datasheet turn-off energy of 3.15 J at 125 ^{o}C is shown in Fig. 24.

When the equations are applied to soft turn-off, under the conditions stated above for the 2 MW, 2300 V converter, the current and voltage shown in Fig. 25 (10% Ramp Time) occur.

This has only 180 mJ loss despite having about 4 times higher current at turn-off. Ramp time is the time required for the switch voltage to reach nominal link voltage, and may be expressed as a percentage of the nominal link charging time. A 10% ramp time is 5% of the link cycle time.

For comparison, the I-V waveforms for a 2% ramp time case is also shown. It is seen that very little current flows through the switches at turn-off, and the little current that does flow does so over a low voltage and decays to near zero before the voltage rises much. This results in very low turn-off losses of only 0.18% at the effective switching frequency of 7 kHz as shown in (3.4).

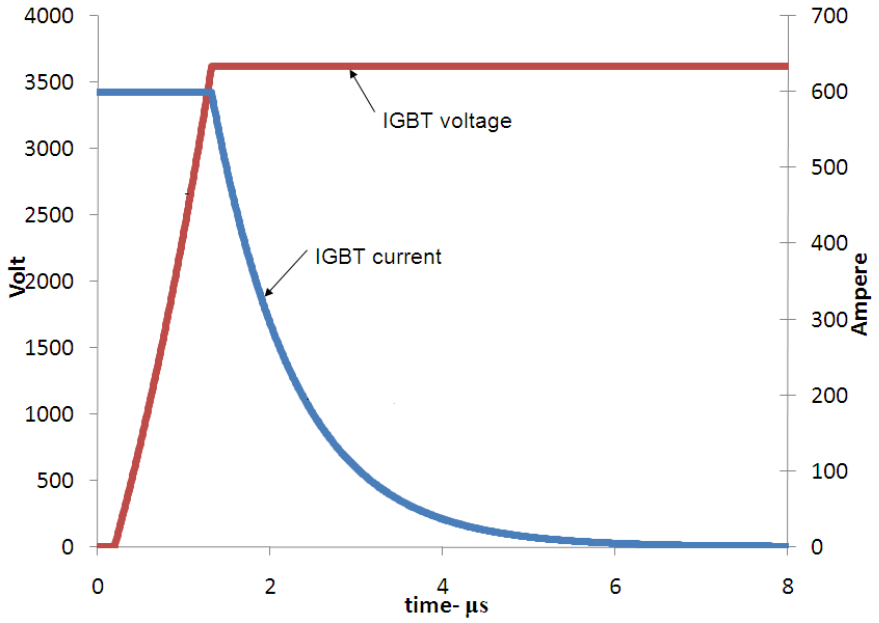

Fig. 24. Hard turn-off of the 6500V, 600A ABB IGBT - by equations

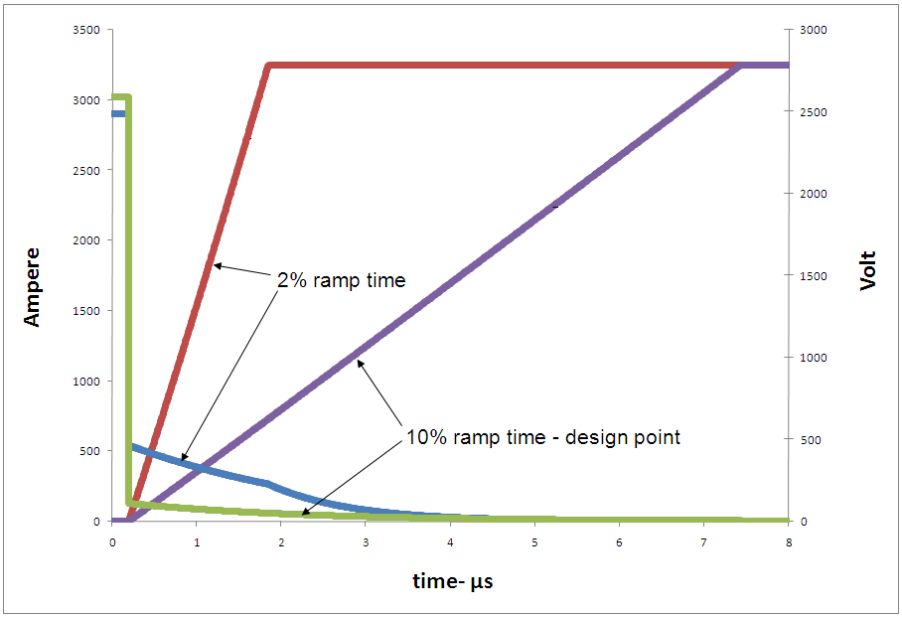

Fig. 25. Soft turn-off of the 6500V, 600A ABB IGBT - by equations

An indication of the validity of this soft turn-off model is to compare its behavior to a physical device simulation based on solving the Poisson's equations for a two dimensionally described IGBT, as implemented in Silvaco Inc's Atlas. Using a physical IGBT model already present in the Atlas example library, a 60 A inductive soft turn-off into a 300 V bus, with a 0.35 μF "snubber" capacitor across the IGBT was simulated. The punch-through IGBT had a carrier lifetime of 100 ns. After selecting the model parameters to best match the simulation results, the current and voltage curves at turn-off were a near perfect match to the simulation, as shown in Fig. 26.

Total turn-off losses are then as given in (3.4).

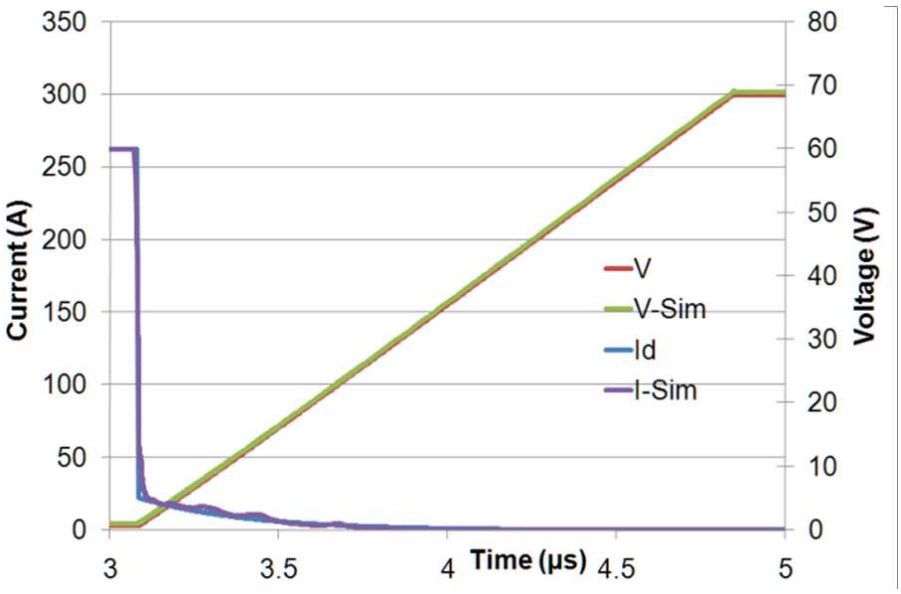

Fig. 26. Match of model to simulation

$$\begin{aligned} P_{turnoff} &= f_L \times 6 \times E_{turn} \\ &= f_L \times 6 \times E_{turn} \\ &= 3.78\ kW\ (0.18\%) \end{aligned} \tag{3.4}$$

E. Link losses

The link inductor has to carry a high amount of current and high frequency. Under this condition, it is not practical to use an inductor with a solid core. A solid core would have to be very big to avoid saturation. Heat generated due to core losses will also making cooling a big problem. The other option is to use an air core inductor with more number of turns as it is much more efficient and more manageable in terms of cooling requirements.

For an air core inductor, link losses are primarily due to the ac resistance of the inductor. A type 8 Litz wire around a coiroidal air core could be used for the link inductor. Litz wire is designed to reduce the skin effect and proximity effect losses in conductors. It consists of many thin wires, individually coated with an insulating film and twisted or woven together, following a carefully prescribed pattern often involving several levels (groups of twisted wires are twisted together, etc.). Due to this the ac resistance is negligibly higher than the dc resistance, and with 70% copper fraction, the coil has a relatively low resistance.

The Inductance to Resistance ratio (L/R) of each coil, along with the link frequency, determines the efficiency of the link inductor. The L/R depends on the geometry of the coils, with larger coils having a higher L/R. The L/R of the 15 kW prototype is 200 μH/20 mΩ, and results in 0.5% total loss when operated at 7 kHz link frequency. Doubling the diameter doubles the L/R, which maintains the 0.5% total loss number when the link frequency is reduced to 3.5 kHz as it is for the 2 MW medium voltage converter examined here. With an L/R, then, of 400 μH/20 mΩ, and a total inductance of 75 μH, the resistance of the medium voltage link inductor is only 4.5 mΩ, so the loss is as given in (3.5).

$$\begin{aligned} P_{link} &= (1 - 0.05) \times 0.0045\Omega \times (0.577 \times 2800)^2 \\ &= 11131\ W\ (0.55\%) \end{aligned} \tag{3.5}$$

Total loss is simply the loss of individual components. Total predicted efficiency is 97.67%. This is a big number considering the power level and the switching frequency.

F. Summary

Rigorous and fairly accurate estimation of losses in the converter was made. Because of the inherent soft switching nature of the converter, switching losses are very less. Reduction of switching losses is very important in higher power converters and the proposed topology features that. This results in a predicted efficiency of higher than 97%.

CHAPTER IV

OTHER APPLICATIONS

The previous chapters dealt with a three phase ac-ac configuration. Because of its fundamentally simple operating principle, the application is not restricted to (three phase) ac-ac alone. This chapter discusses some other applications this ac-link converter can be put to.

A. Wind power converter

The oil crisis in the early 70's and the steadily increasing environmental concern have initiated a major interest for the exploitation of renewable sources of energy for the generation of electrical power. Most promising among them appear to be the wind and, at a second level, the solar energy. The main characteristic of these sources, compared with the conventional ones, is that the primary energy flow is stochastic in nature and thus uncontrolled and continuously fluctuating, which is particularly true for the wind. Therefore, special schemes and control procedures have to be developed and implemented for the regulation of the produced electrical power and the maximization of the capture of the available energy. With the recent developments in the power electronics, low-cost and high-reliability and efficiency converters are available for wind turbine (WT) and photovoltaic (PV) applications. The utilization of advanced power conversion schemes and sophisticated controllers presents an increasing interest, since it improves the energy production and the quality of operation of the plants.

The topology presented in this research can be successfully applied for wind energy converters. It presents itself very well for this application. For high power applications, symmetrical gate controlled thyristors (SGCTs) would be used as the

switches as show in Fig. 27.

The converter is essentially current sourced, although all link current flows are

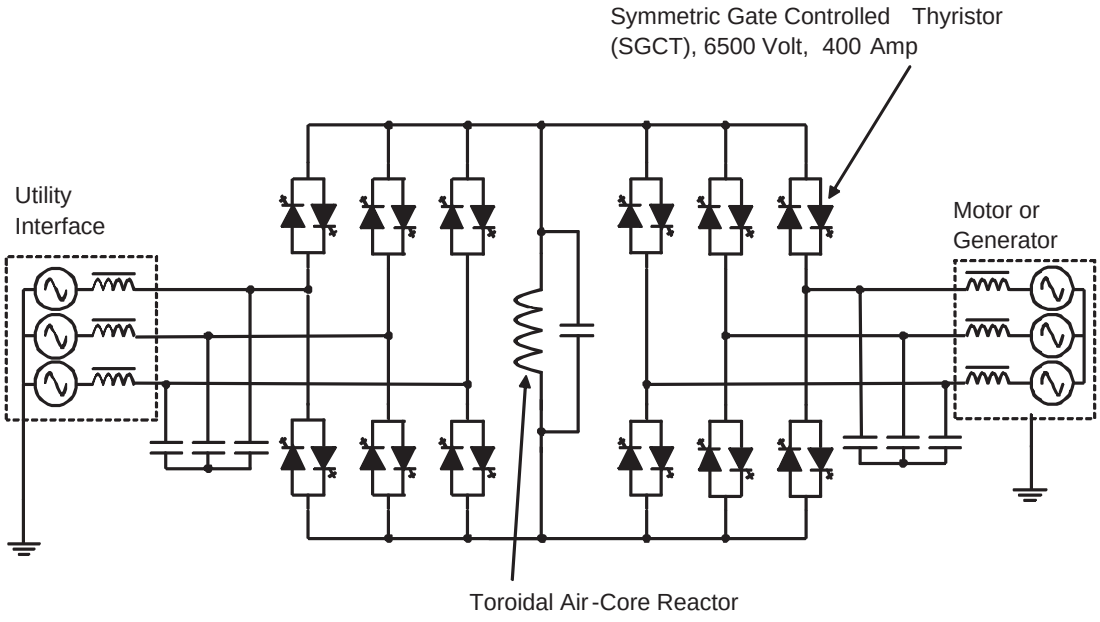

Fig. 27. Three phase converter for wind power application

AC. At no time is the output directly connected to the input and hence there is isolation between the two, allowing for transformer-less operation with the neutral points of both input and output grounded, thereby eliminating offset common-mode voltages. Additionally, full galvanic isolation between input and output may be achieved by using a dual, interleaved winding version of the link inductor.

Converters of this topology for wind power applications that have much higher power ratings will use even lower per unit weight self shielded toroidal air core reactors. Link capacitance may be advantageously added to buffer turn-off losses, with the optimal capacitance determined by balancing reduced turn-off losses against the resulting slight decrease in power throughput. The input/output line filters are composed of compact film capacitors with a small line reactor on the utility side.

An important feature of the converter that makes it very suitable for wind power applications is its ability to perform buck or boost operations, allowing it to operate to or from any voltage level and/or power factor within the voltage and current constraints of the converter. Thus it can boost a generators output, with unity power factor and low harmonics, to the utility interface voltage, at any power factor being demanded by the utility. Its ability to change voltage levels between the input and output is due to the partial resonant period between the charging and the discharging modes (Mode IV).

During this mode, the charged link is simply allowed to resonate. With this, the link voltage can rise to values much higher than the input voltage, the level restricted only by the Q factor of the LC circuit. Turning on the output switches at the desired voltage level allows any input-output voltage ratio.

B. Solar inverter

It is necessary to decrease the specific costs ($/kW installed) of renewable energy forms. This not only involves capturing the renewable energy cheaply, but also interfacing it to the power grid in a cost effective way. Photovoltaic sources deliver voltage and current in DC and hence are not suited for direct grid integration. It is necessary to convert the variable DC power from these to a constant frequency AC form via power electronic converters to facilitate integration to the electric grid. Different power converter topologies have been proposed to a PV to the AC grid [26–28]. Fig. 28 illustrates these topologies.

The topology shown in Fig. 28a consists of a boost DC/DC converter that provides a DC link for the inverter. But using a non-isolated DC/DC converter would

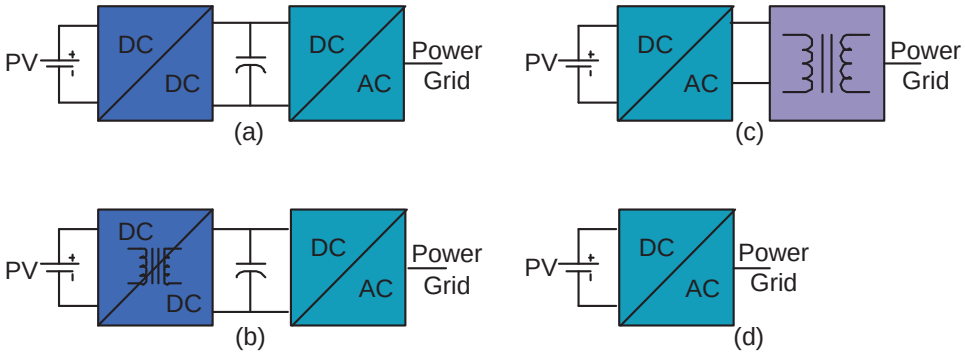

Fig. 28. Different topologies for PV to ac grid integration

require additional precaution for safety and potential EMI must be considered [3]. One approach to avoid these problems is to use an isolation transformer as illustrated in Fig. 28b. Fig. 28c illustrates a scheme where a DC/AC converter converts the power from the PV array to a low voltage AC which is stepped up using a bulky power transformer. Another solution that has been proposed is shown in Fig. 28d. It's a simple VSI that's controlled to deliver the output in the required form. However for proper operation of this, the input DC voltage must be higher than the peak to peak grid voltage. This is tough to achieve because of the variable voltage coming from the PV array. All of these solutions require expensive and lossy output filters.

1. Proposed topology

Using the ac-link and bidirectional switches, a single stage converter without the shortcomings of the above mentioned topologies is proposed. It's a DC/AC converter that uses a high frequency AC link between the input and the output. Inputs never connect directly to the output and hence there is inherent isolation between the two which allows neutral grounding of both the AC and the DC stages. A schematic of the same is shown in Fig. 29.

There are 2 bidirectional switches per leg of the converter. The AC link is

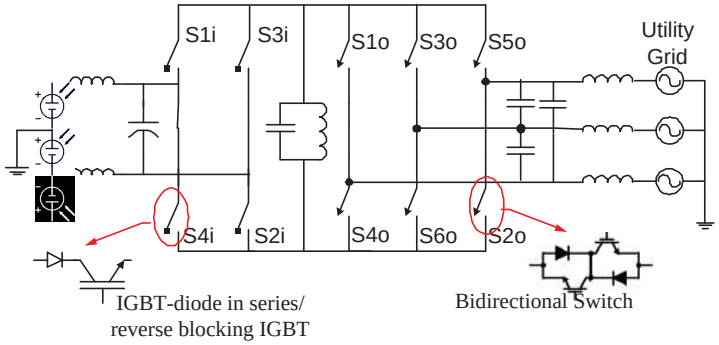

Fig. 29. Proposed configuration for solar inverter

formed by a low reactive rating inductor-capacitor pair. The DC input from the PV panels charges the link inductor. This is then discharged to the output phases. The output current pulses are controlled precisely using a pulse width modulation scheme that ensures less than 1.5% harmonics below twice the link frequency. With the available commercial switches a link frequency of 5 kHz or higher may be achieved. All turn-on's are at zero voltage and turn off losses are low because of the capacitive buffer across them. The converter is essentially a PWM current source although all link flows are AC with no DC offset.

2. Modes of operation

Mode 1: During this mode, depending on the polarity of the link current, S1i and S2i or S3i and S4i are turned on to allow the link to charge to a required level. In the example shown in Fig. 30, switches S1i and S2i are turned on. The link current rises to the amount required to extract maximum power from the PV panel, as shown in Fig. 31.

Mode 2: At the end of mode 1, all the switches are turned off and the converter enters

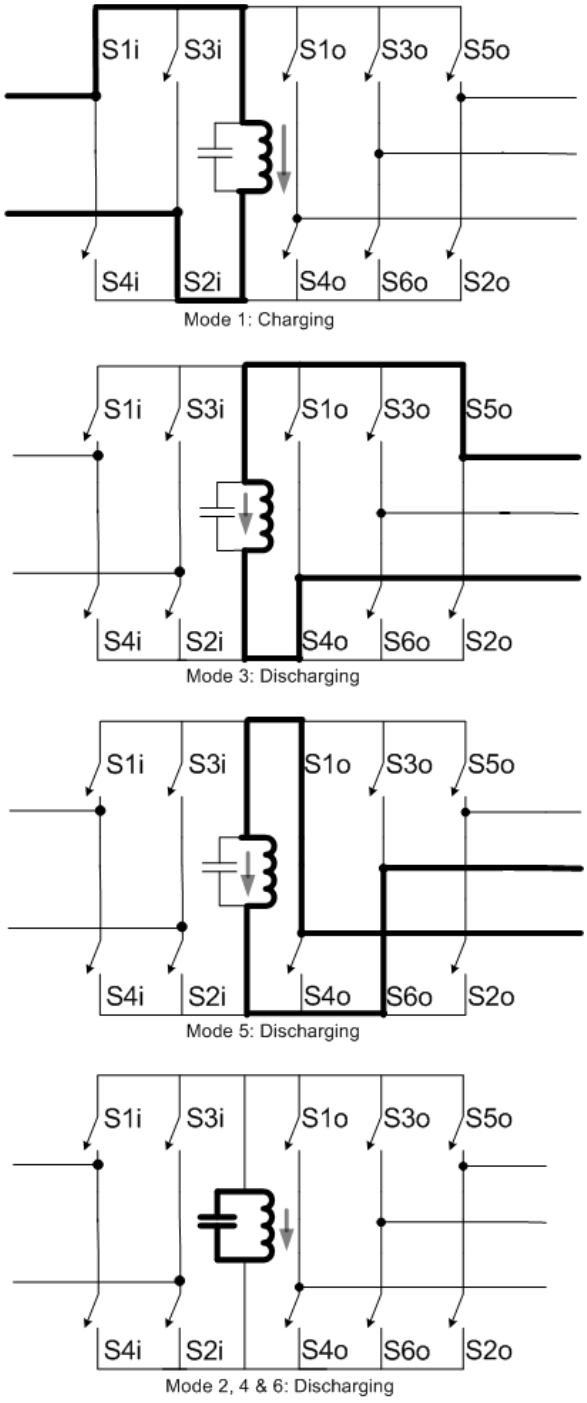

Fig. 30. Modes of operation of proposed converter

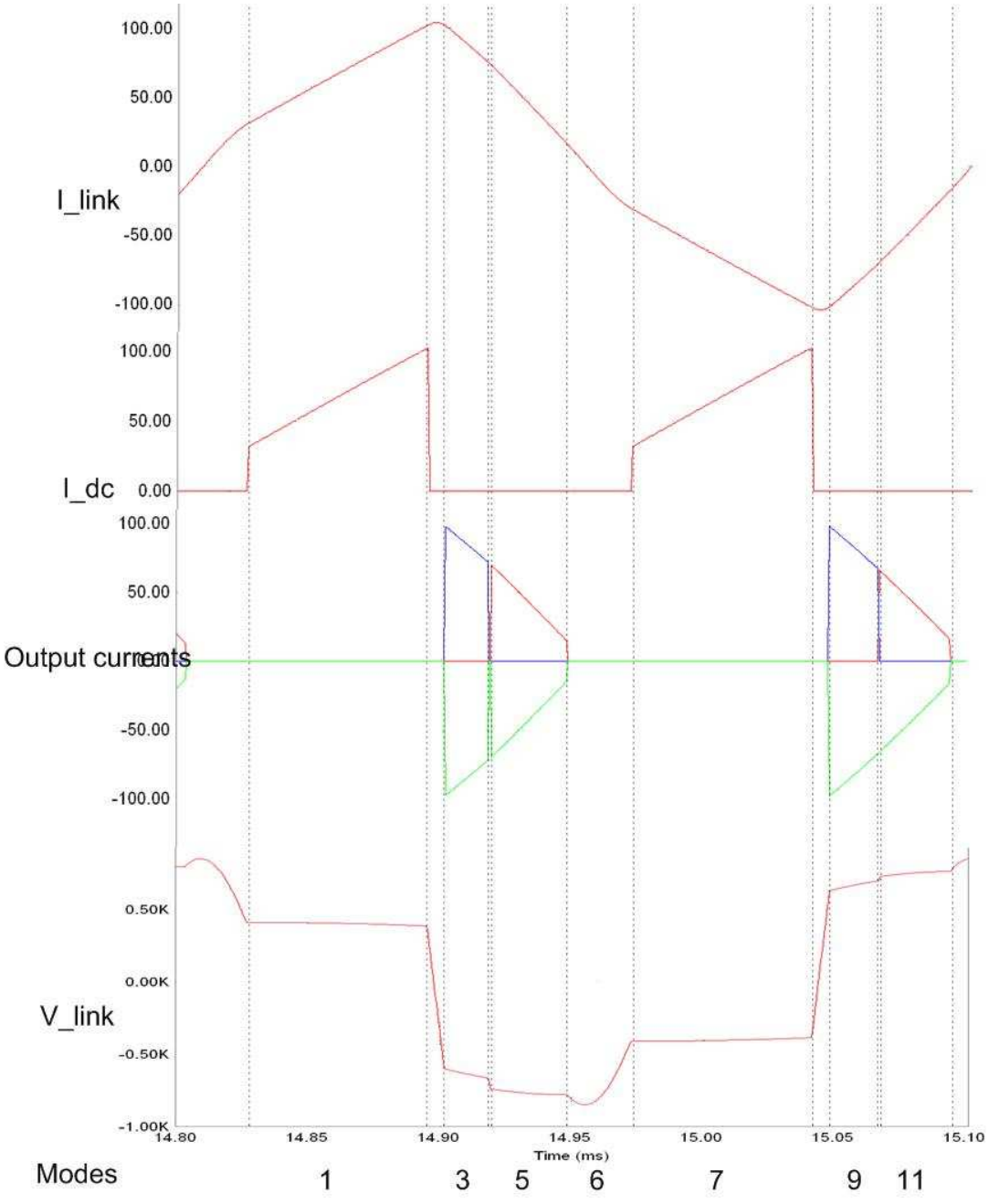

Fig. 31. Significant waveforms during different modes of operation of converter

mode 2. During this mode, the link resonates partially until its voltage swings to the first output phase pair.

As mentioned earlier, the link then discharges into the grid in two different modes to proportionately power the three output phases. The fact that the instantaneous sum of three phase phases is zero is used to advantage here. Making simplifying assumptions that the output filter results in zero phase shift between voltage and current, and that link frequency is much greater than the line frequency, the following example is considered.

If instantaneous phase voltages are Van=100 V, Vbn=-70 V, Vcn=-30 V and the link charges to 10 A during mode 1, the link would discharge to lines AB and AC to equivalently supply 7 A and 3 A respectively. This makes the output currents in phase with the output voltages resulting in unity power factor. This would be done to extract maximum real power from the PV cells. The output discharge occurs in order of decreasing instantaneous line voltage to minimize the partial resonant periods.

The actual algorithm, as expected, removes the assumptions made to handle real scenarios.

Mode 3: Previously enabled output switches, corresponding to the selected phase pair, turn on at zero voltage as they become forward biased by the rising link voltage. The link then discharges to the output until specific system generated references are met. Again, the references are generated so as to achieve unity power factor at the output while maintaining strict harmonic levels. In the example shown in Fig. 30 and Fig. 31, switches S1o and S6o are turned on to allow the link to discharge to phase BC.

Mode 4: Switches are turned off to allow the link to resonate till its voltage becomes equal to the second output phase pair it will discharge to.

Mode 5: Switches become forward biased to allow the link to discharge to the second

phase pair. In the example shown in Fig. 30 and Fig. 31, switches S4o and S5o are enabled and then turn on to allow the link to discharge to phase AC.

Mode 6: The link is allowed to partially resonate back to the input voltage to start the next charging cycle.

Modes 7 to 10 are identical to modes 1 to 5 except that the link current is in the reverse direction. This can be seen in Fig. 31.

At full array voltage and power, the DC input voltage is nominally equal to the AC average output voltages. At reduced array voltage and power, the converter boosts the array voltage to the required AC output voltage. Current from the array is increased or decreased for MPPT by controlling the amount of current charge that the link receives from the input.

C. Summary

While the above two applications showed the converters capability to perform buck-boost and dc-ac conversion, the applications are not restricted to these alone. Because the converter utilizes bidirectional switches, handling of ac waveforms is made very straightforward. The list below suggest some alternative applications for the proposed topology:

1) Variable Speed Motor Drives low voltage 10 to 1000 kW, medium voltage 200 kW to 20 MW and higher

2) Solar grid-tied inverters

3) Wind energy converters

4) High power density ship board drives and power converters

5) High Voltage Direct Current (HVDC) power converters

6) Electric vehicle power converters.

CHAPTER V

RESULTS AND SUMMARY

Extensive simulations were carried out initially for a 15 kW, 460 V converter with a link frequency of 10 kHz. This design was used to arrive at a suitable switching scheme to operate the converter. The algorithm derived using this converter was extended to operate a 2 MW, 2300 V converter with a link frequency of 3500 Hz. The 2 MW converter with a lower link frequency made visible smaller control issues which helped in refining the switching algorithm. The link inductance was 73 μH and the link capacitance was 5.75μF.

A. 15 kW converter simulation results

Table IV shows the parameters used for simulating the 15 kW converter. The parameters were designed using the procedure explained previously.

Fig. 32 shows the simulated output currents and voltages for converter. Fig. 33 shows the input current waveforms for the same. Input current ripple with a 1500 Hz filter as seen is so small as to be almost imperceptible. The simulated results showed a current THD of less than 1.5%.

Table IV. 15 kW converter parameters

Link frequency	10 kHz
Peak link current	110 A
Link Inductance	140 μH
Link Capacitance	0.2 μH

Fig. 34 demonstrates the ability of the converter to operate with differing input and output common mode levels. Input and output voltages are phase shifted by

about 50^o.

B. 2 MW converter simulations

As mentioned earlier, successful results from the 15 kW converter simulations with a high link frequency acted as a stepping stone for higher power, lower link frequency converter. Operating with a lower link frequency enables refining finer control issues.

Fig. 35 shows the schematic of the circuit used for simulation. Simulations were carried out in PSIM software with an embedded C code to carry out the switching algorithm.

Fig. 36 and Fig. 37 show the link current and voltage waveforms. Fig. 38 shows the converter input current pulses. Current pulses are precisely modulated so as to result in a sinusoidal shape upon filtering as shown in Fig. 39. Calculations on the input currents results in a highly acceptable THD of 1.38% below the 7 kHz ripple frequency, and a ripple magnitude that contributes an additional 1% THD, for less than 2.5% total THD. It is believed that slight imperfections in the switching control are responsible for the distortion below 7 kHz, and that further work can mostly eliminate these very low amplitude harmonics. Fig. 40 shows the filtered input voltage. The harmonic level on this are also at a highly acceptable level of 4.1%. Resulting output voltages and currents are seen in Fig. 41 and Fig. 42.

C. Preliminary experimental results

The 15 kW proof-of-principle prototype shown in Fig. 43 and uses 24, 1000 V, 60A rated NPT IGBTs with diodes to form the 12 ac switches needed for its

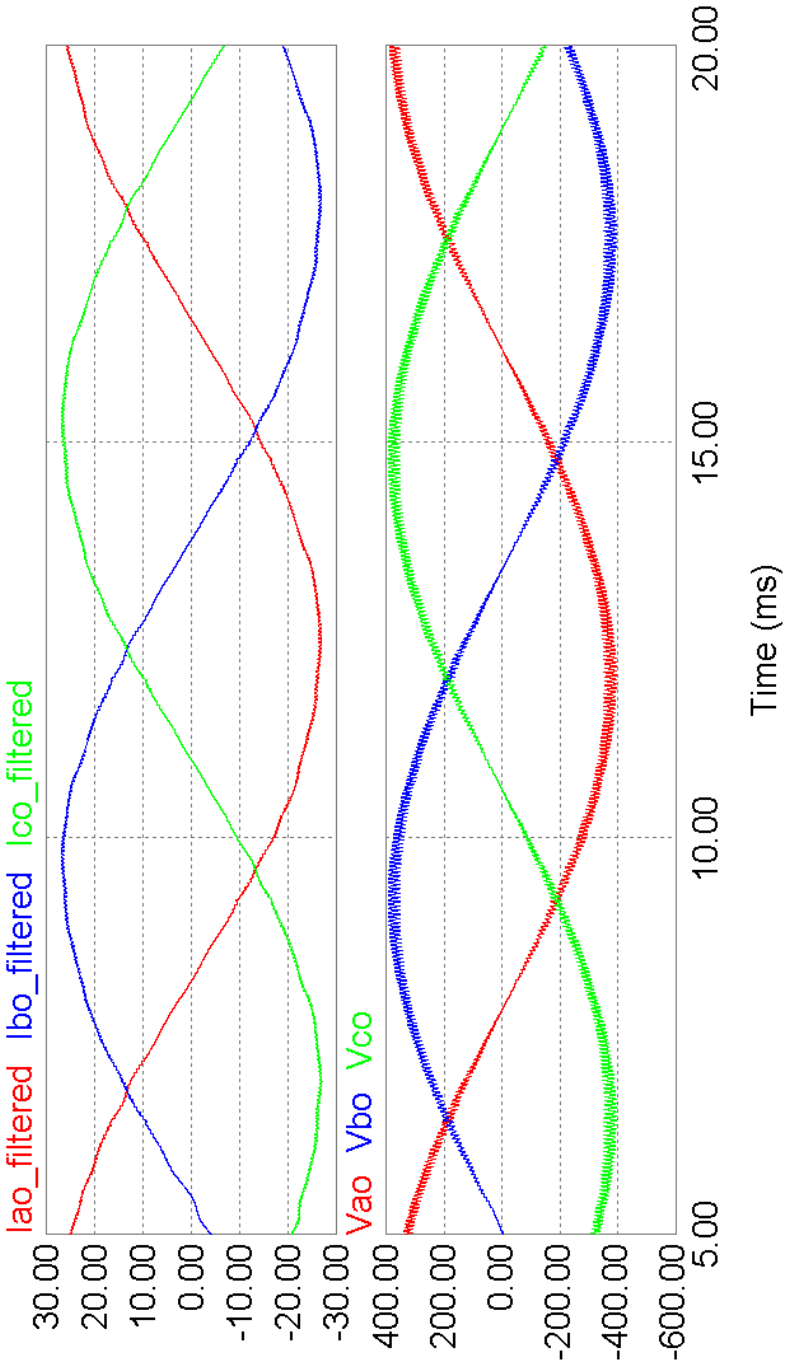

Fig. 32. Output current and voltage for 15 kW converter

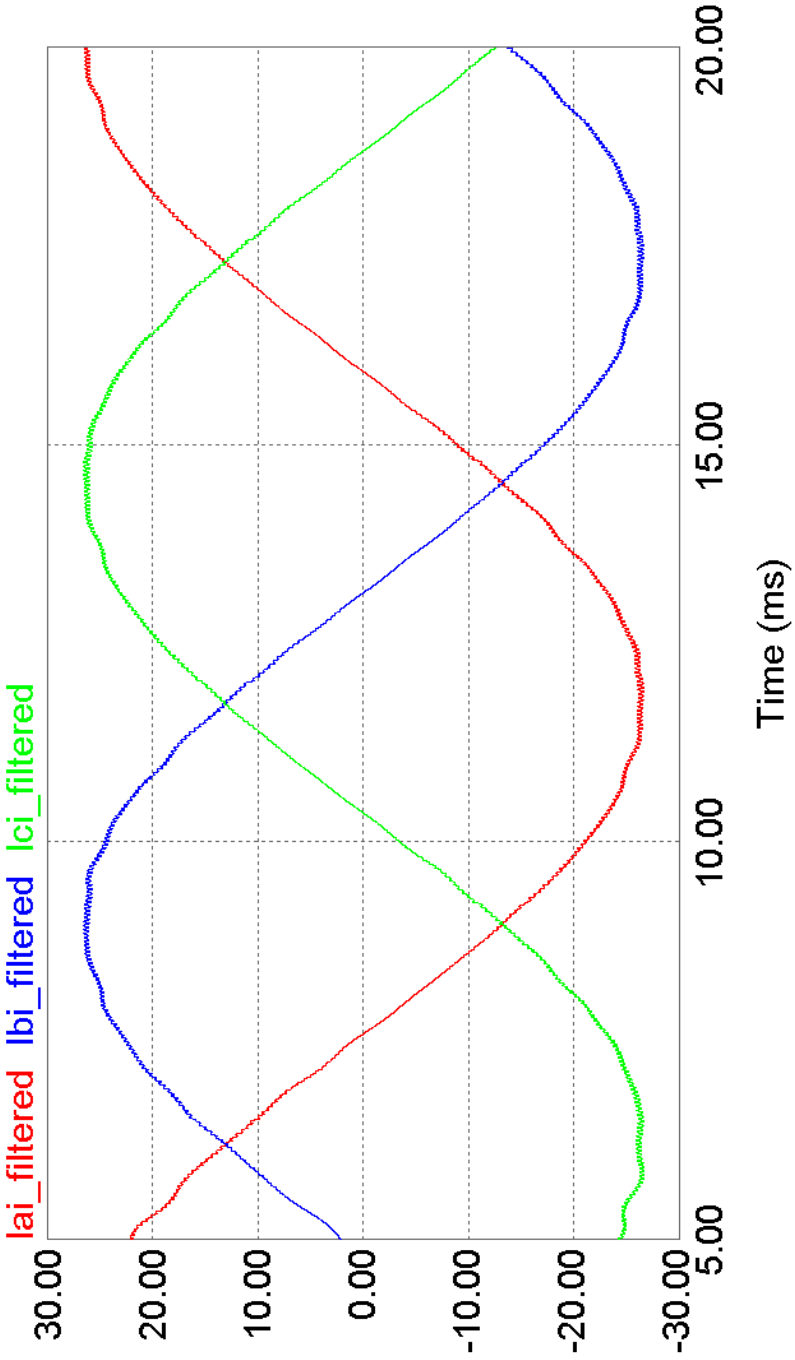

Fig. 33. Input currents for 15 kW converter

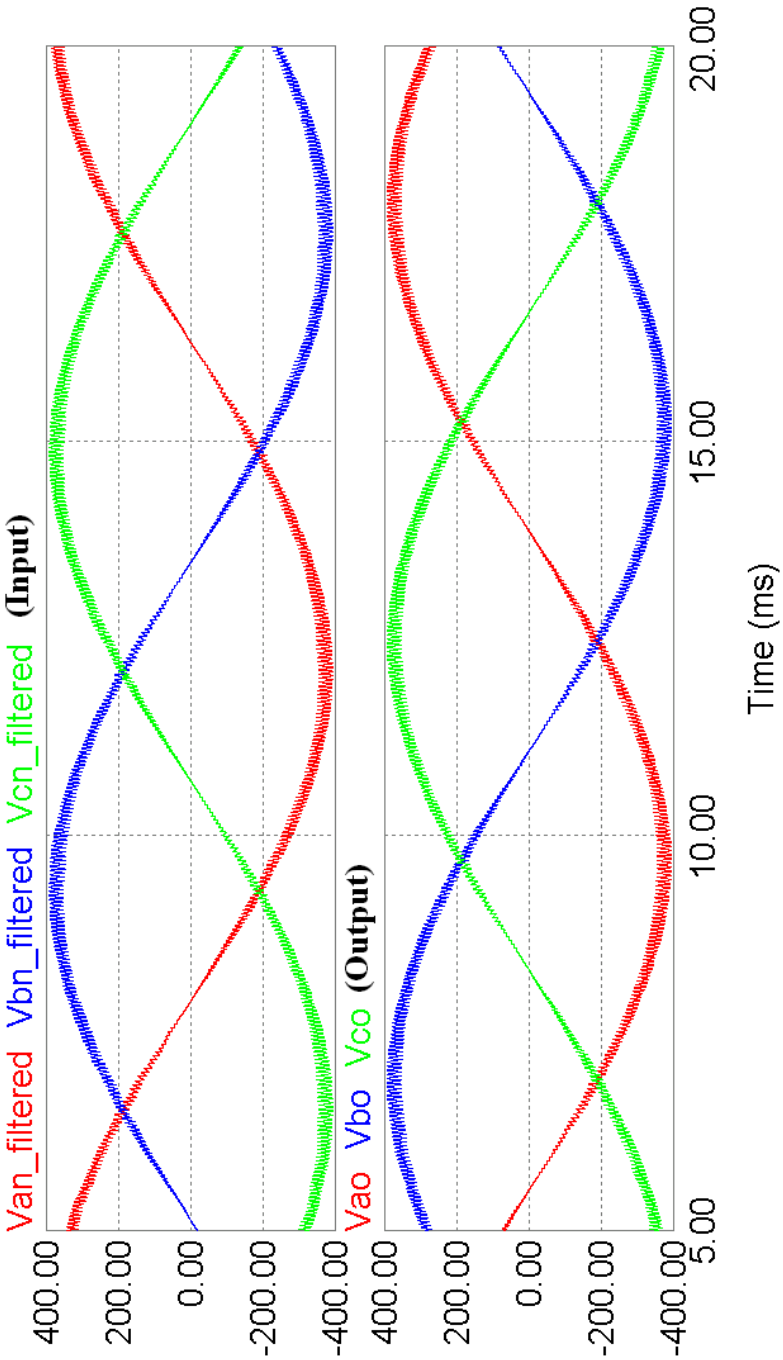

Fig. 34. Input and output voltages phase shifted to demonstrate isolation between input and output

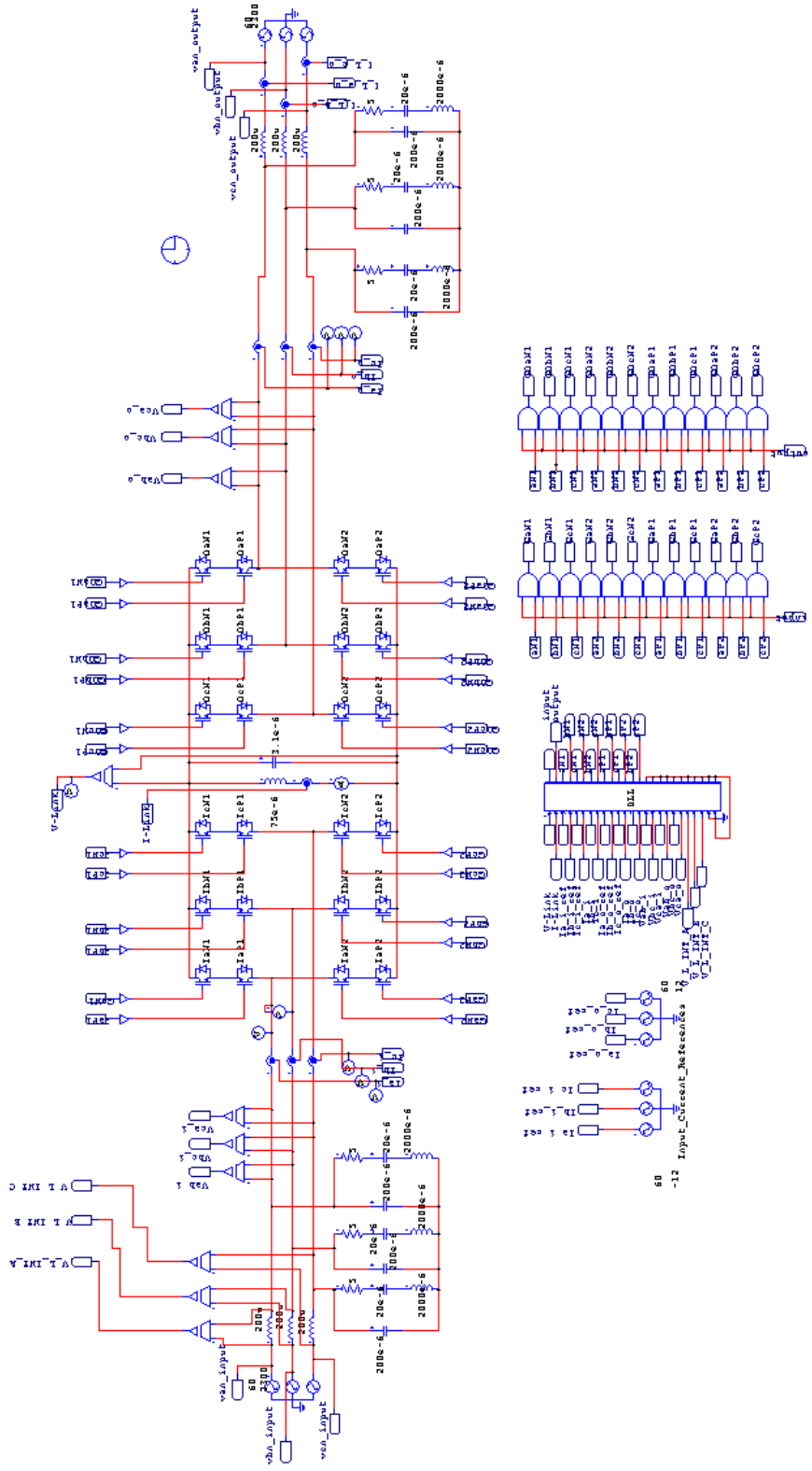

Fig. 35. PSIM schematic of circuit used for simulations

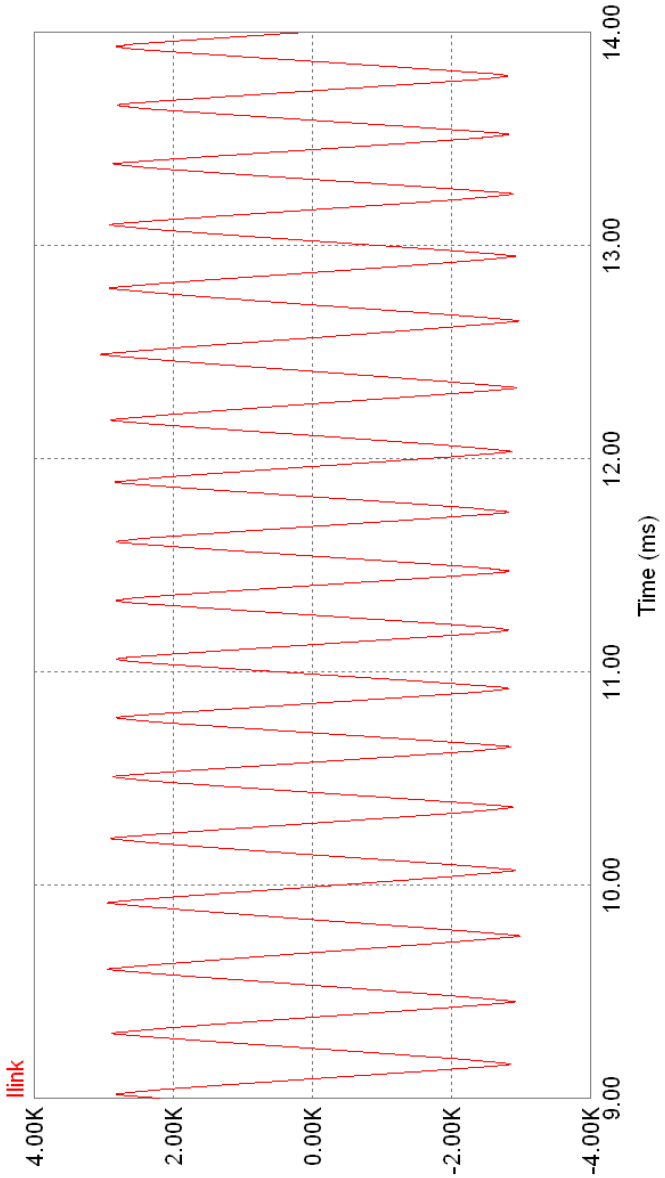

Fig. 36. Link current for 2 MW converter

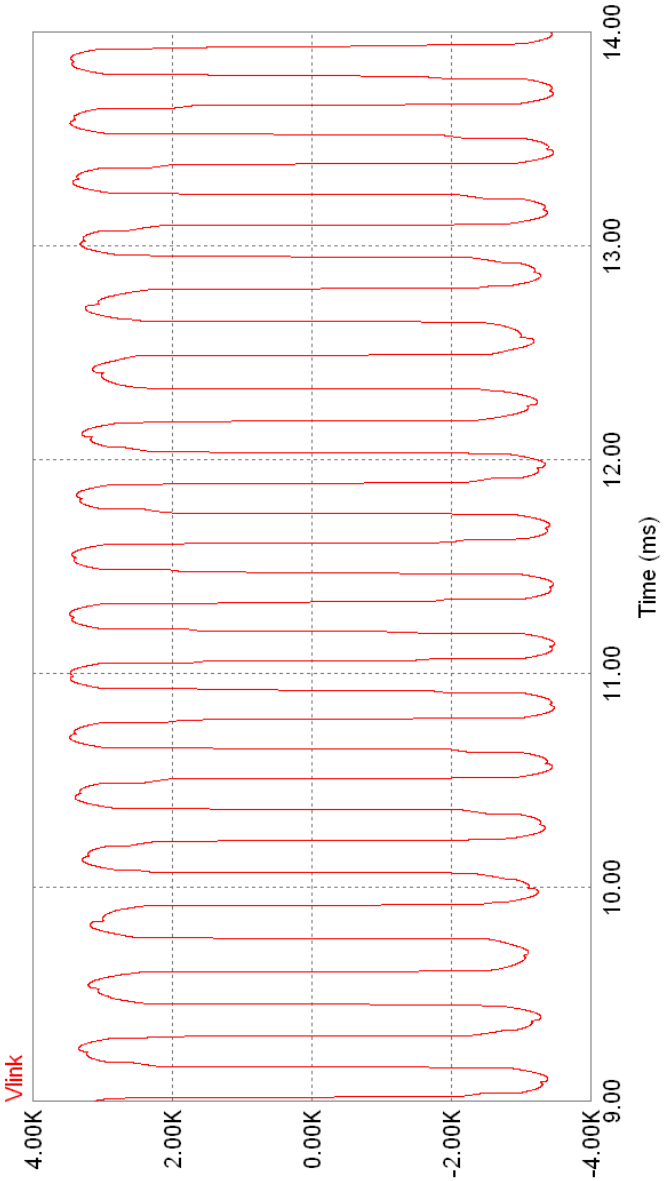

Fig. 37. Link voltage for 2 MW converter

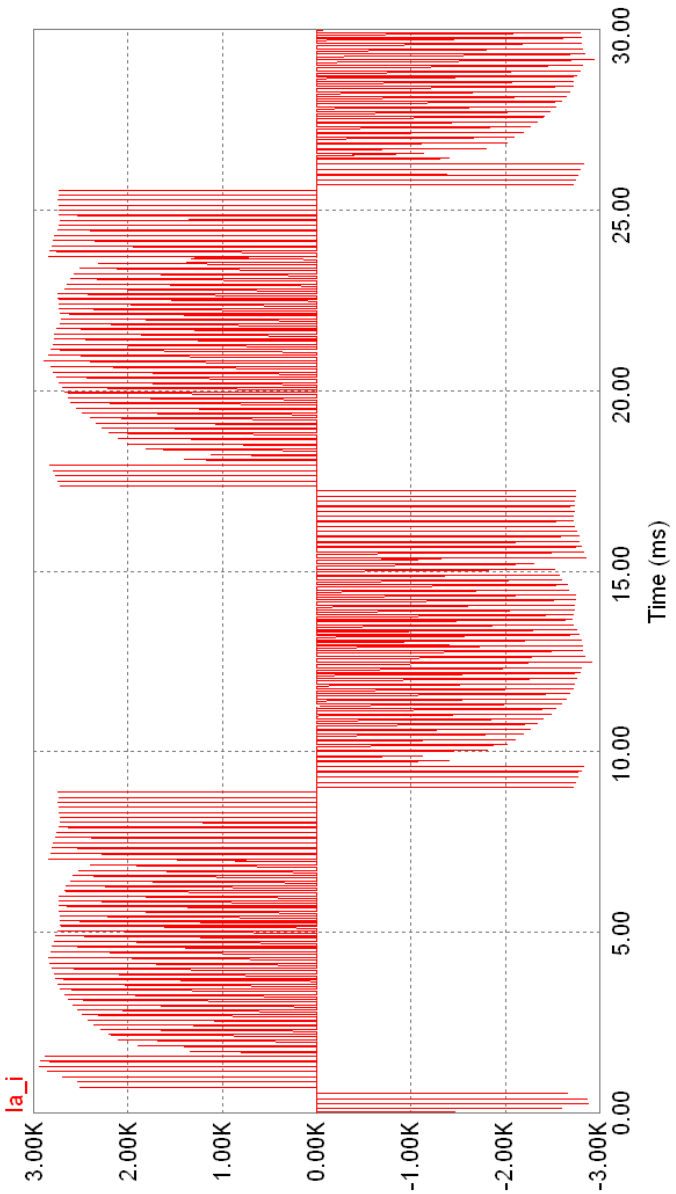

Fig. 38. Converter input currents

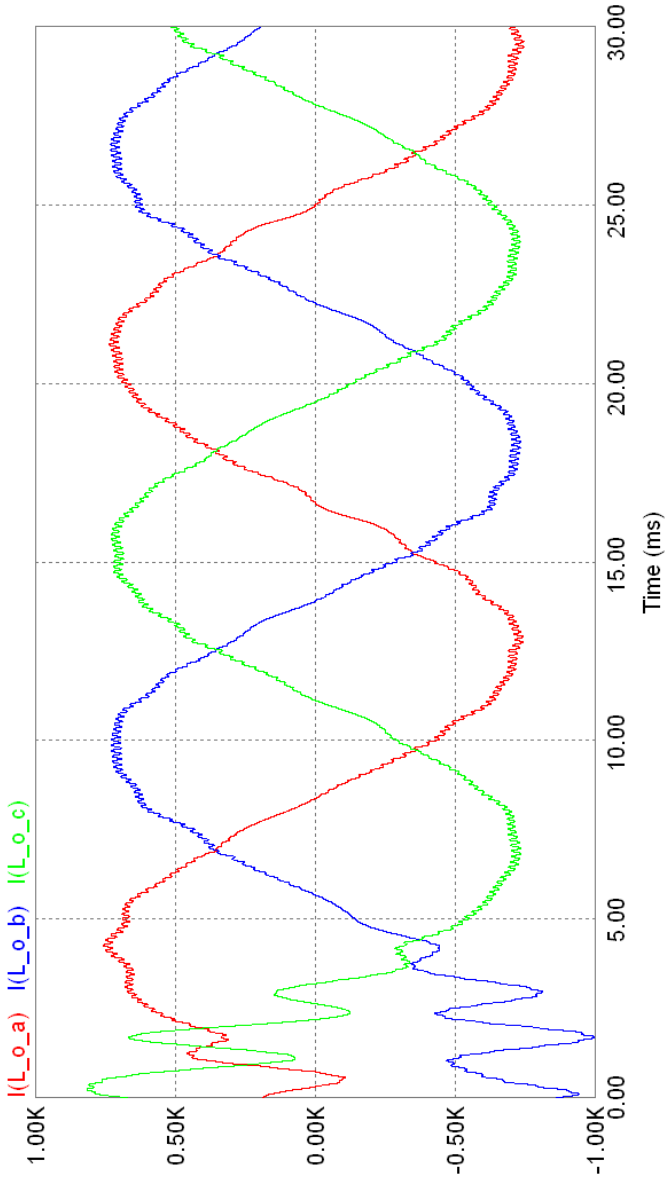

Fig. 39. Filtered input currents

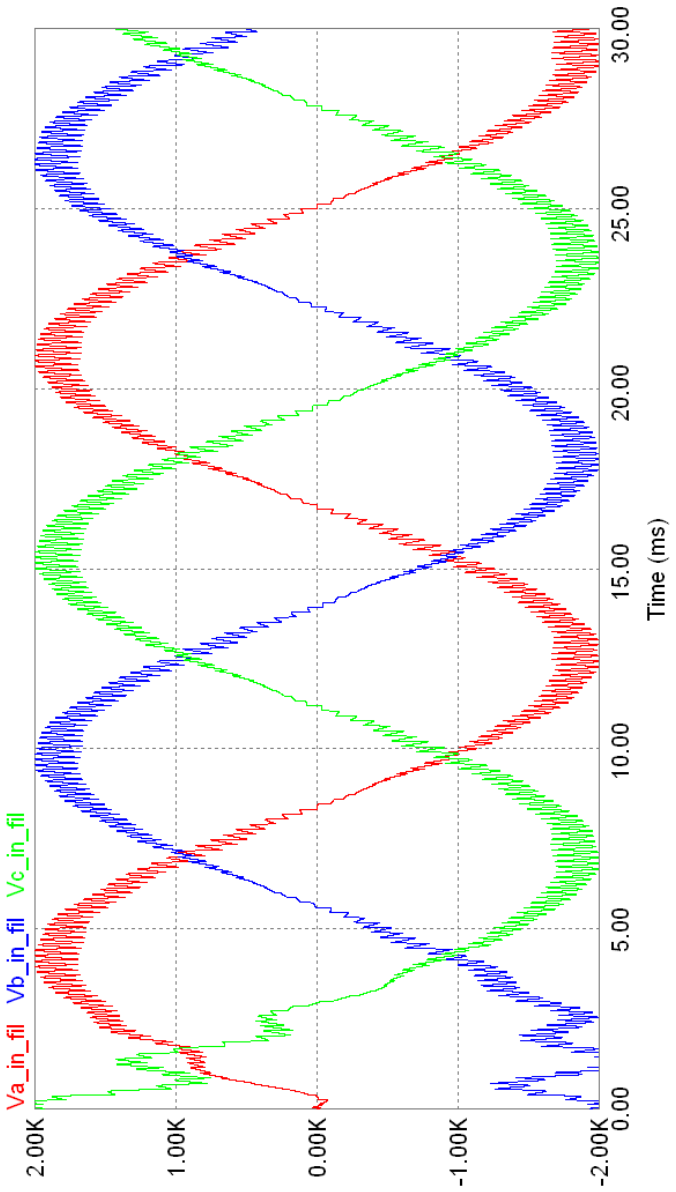

Fig. 40. Filtered input voltages

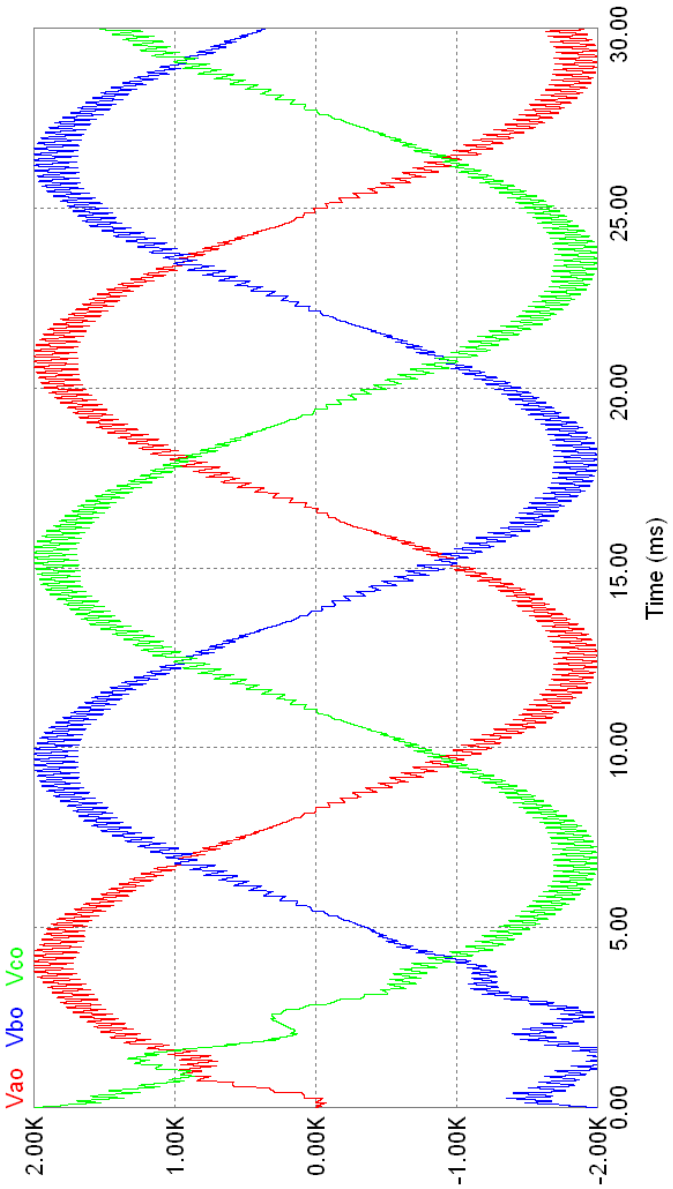

Fig. 41. Filtered output voltages

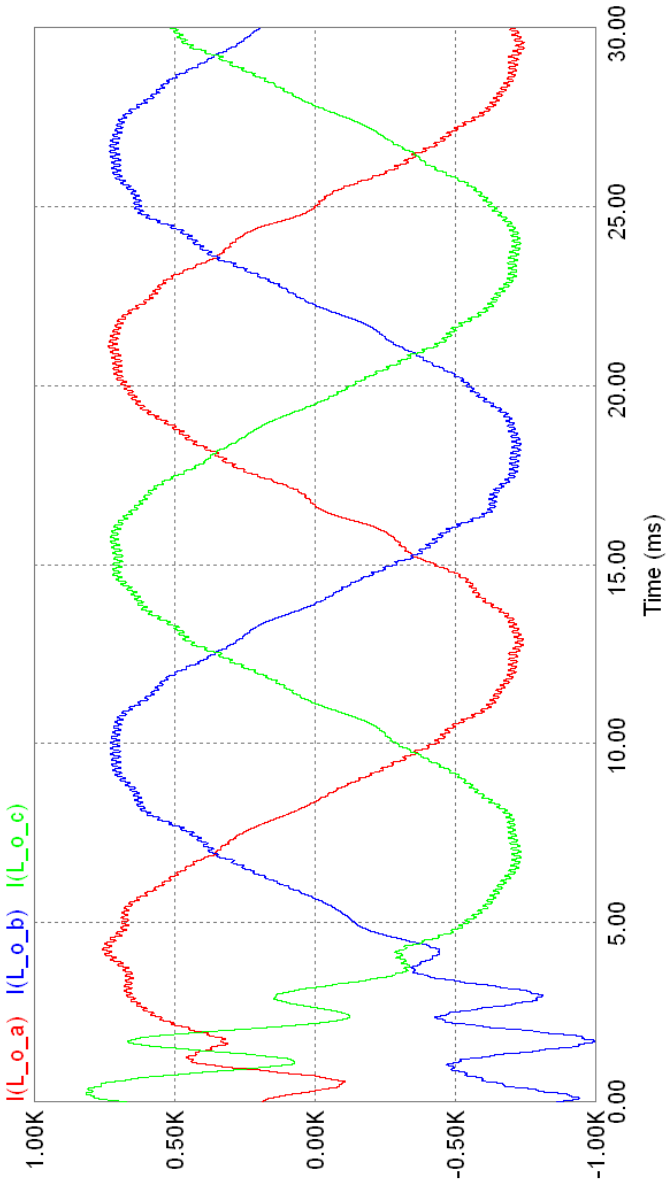

Fig. 42. Filtered output currents

three-phase ac to three-phase ac operation. Low level control is through an FPGA programmed in AHDL with circuit sensing provided by 8, 3 MBPS, 12 bit, ADCs. Three 20 μF film capacitors are connected line-to-line across each of the input and output lines. The link inductor is a spiral wound coil of Type 8 Litz wire with a dc resistance of 15 mΩ, and inductance of 100 μH, and a free-air Q-factor of 125. When placed in the ferrite C-core shielded link inductor assembly, the inductance rises to about 190 μH, as determined by the measured 6400 Hz link frequency, the 600V average peak link voltage, and the 120A peak current as measured by the dV/dt on the 0.3 μF link capacitance during the partial resonance period.

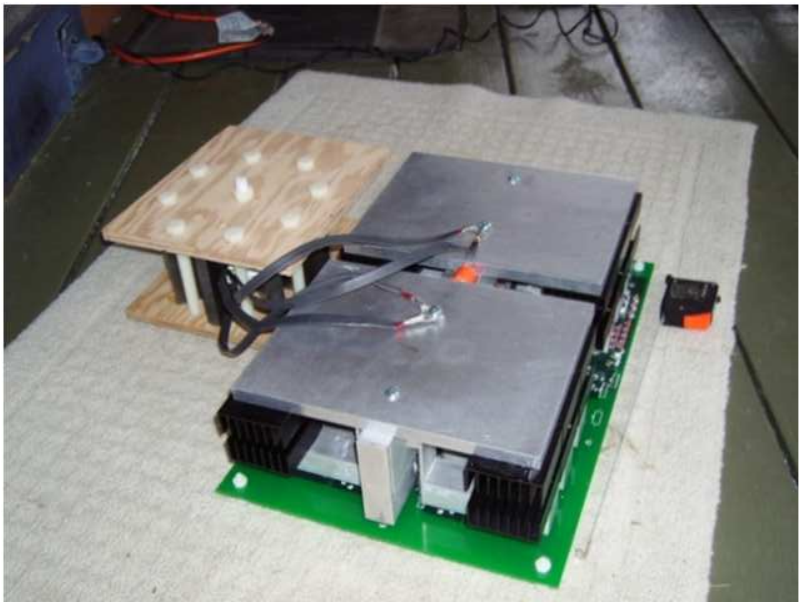

Fig. 43. 15 kW prototype with link inductor

Fig. 44 below shows the converter running in a simple test as a self-powered dc-dc converter, running off only the energy in the input line capacitors charged to 600 volts. Converter operation was terminated after 10 power cycles (5 link cycles), at the 900 μs mark. From the know link inductance, voltage, and frequency, the link

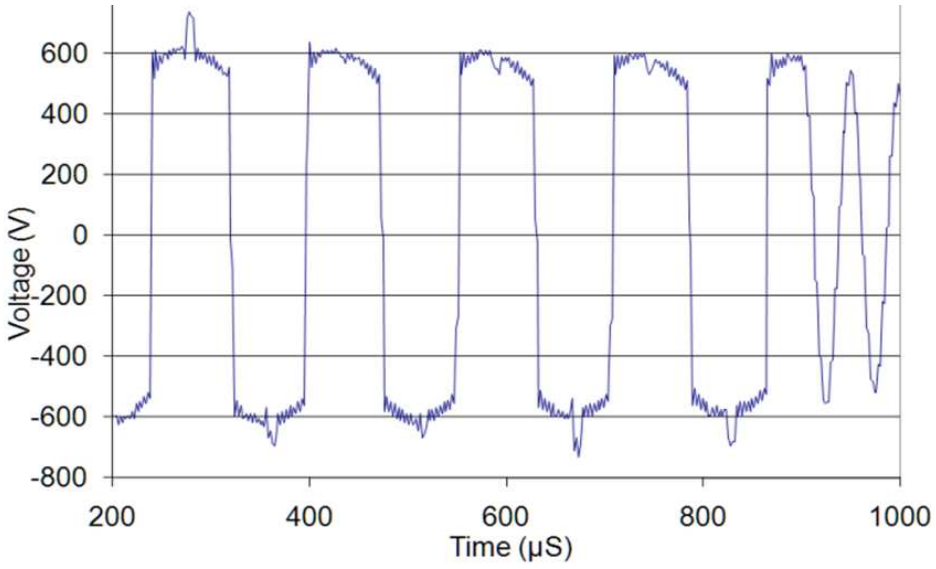

Fig. 44. Link voltage for waveform of prototype

current may be estimated at 120 amps peak, which is supported by the dV/dt at turnoff shown in Fig. 44 of 400 V/μs. Each switch sees half of this, or 200 V/μs. The resulting power level is 17 kW. Efficiency may be estimated from the voltage drop of the link over the 10 power cycles (as in Fig. 45, and is computed at 93%. The loss model at this power level predicts 95.4% efficiency, with an assumed turn-off loss, so there is apparently about 2.4% of additional unaccounted for losses. These may be from excessively long IGBT tail current, as some IGBTs have that characteristic, or the loss could be from one or more of the other converter components.

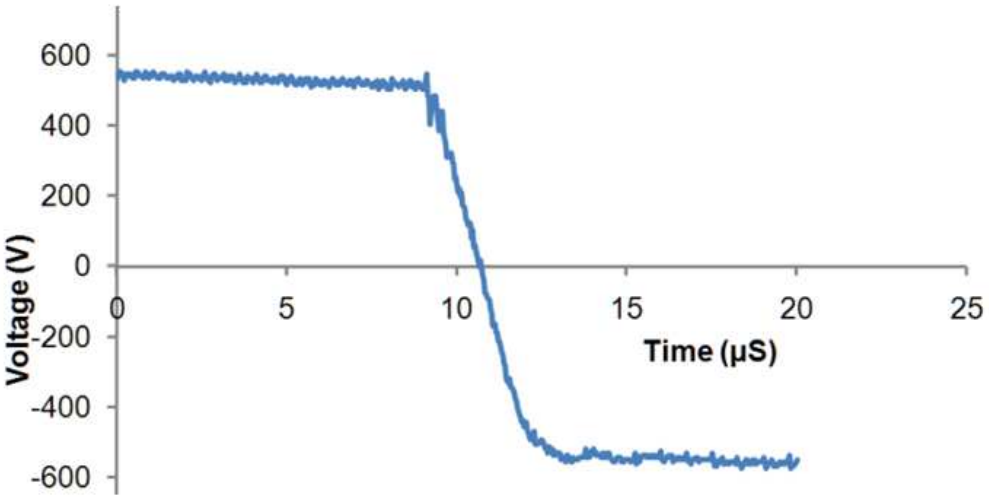

Fig. 45. Input capacitor voltage to measure efficiency

D. Summary

The Soft Switched Ac-Link Converter may be utilized in a wide variety of applications ranging from low and medium voltage motor drives, to transformer-less solar inverters, large wind power converters, isolated ac-dc bi-directional converters, and many other applications that may benefit from its conversion versatility, soft-switching efficiency, input-output isolation, and high power quality. The topology is expected to offer relatively low cost, low weight, compact and efficient power converters and motor drives

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