RADIO-FREQUENCY INTEGRATED-CIRCUIT DESIGN FOR CMOS SINGLE-CHIP UWB SYSTEMS

A Dissertation

by

YALIN JIN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2008

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Cam Nguyen
Committee Members,	José Silva-Martínez
	Laszlo Kish
	Mark Everett
Head of Department,	Costas N. Georghiades

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ABSTRACT

Radio-Frequency Integrated-Circuit Design for CMOS Single-Chip UWB Systems. (May 2008)

Yalin Jin, B.S., Xi'an Jiaotong University, China;

M.S., Chinese Academy of Sciences

Chair of Advisory Committee: Dr. Cam Nguyen

Low cost, a high-integrated capability, and low-power consumption are the basic requirements for ultra wide band (UWB) system design in order for the system to be adopted in various commercial electronic devices in the near future. Thus, the highly integrated transceiver is trended to be manufactured by companies using the latest silicon based complimentary metal-oxide-silicon (CMOS) processes. In this dissertation, several new structural designs are proposed, which provide solutions for some crucial RF blocks in CMOS for UWB for commercial applications.

In this dissertation, there is a discussion of the development, as well as an illustration, of a fully-integrated ultra-broadband transmit/receive (T/R) switch which uses nMOS transistors with deep n-well in a standard 0.18-μm CMOS process. The new CMOS T/R switch exploits patterned-ground-shield on-chip inductors together with MOSFET's parasitic capacitances in order to synthesize artificial transmission lines which result in low insertion loss over an extremely wide bandwidth. Within DC-10 GHz, 10-18 GHz, and 18-20 GHz, the developed CMOS T/R switch exhibits insertion

loss of less than 0.7, 1.0 and 2.5 dB and isolation between 32-60 dB, 25-32 dB, and 25-27 dB, respectively. The measured 1-dB power compression point and input third-order intercept point reach as high as 26.2 and 41 dBm, respectively.

Further, there is a discussion and demonstration of a tunable Carrier-based Time-gated UWB transmitter in this dissertation which uses a broadband multiplier, a novel fully integrated single pole single throw (SPST) switch designed by the CMOS process, where a tunable instantaneous bandwidth from 500 MHz to 4 GHz is exhibited by adjusting the width of the base band impulses in time domain. The SPST switch utilizes the synthetic transmission line concept and multiple reflections technique in order to realize a flat insertion loss less than 1.5 dB from 3.1 GHz to 10.6 GHz and an extremely high isolation of more than 45 dB within this frequency range.

A fully integrated complementary LC voltage control oscillator (VCO), designed with a tunable buffer, operates from 4.6 GHz to 5.9 GHz. The measurement results demonstrate that the integrated VCO has a very low phase noise of –117 dBc/ Hz at 1 MHz offset. The fully integrated VCO achieves a very high figure of merit (FOM) of 183.5 using standard CMOS process while consuming 4 mA DC current.

ACKNOWLEDGEMENTS

This dissertation would not have been possible without the help and support of many people. First, I would like to thank Dr. Cam Nguyen, my dissertation advisor, and express my most sincere appreciation to him for directing me to this wonderful field of research and directing me. I am also indebted to him for helping me gain industry RFIC design practice that broadened my research knowledge and capability. His instruction and direction were instrumental in my efforts, as I pursued my research and experiments, by which I ultimately was able to produce through careful analysis the design for the world's first high-power, high-linearity, ultra-compact CMOS T/R switch for UWB applications and propose the new power-efficient UWB transmitter. He believed in me from the beginning and has been a constant source of encouragement throughout the duration of the dissertation process.

I sincerely thank my committee members, Dr. Silva and Dr. Kish, for their time, as well as for generously making themselves available to me and offering me many valuable suggestions during the course of my work. I am also very grateful to them for all that I learned from their courses on broadband systems and low noise circuitry. I am also indebted to Dr. Mark Everett who taught me about the many intricacies associated with EMI sensors.

The people at Alereon Inc. played important roles in the design of the first worldwide LO generator of all-band WiMedia MB-OFDM UWB and helped me with my work. Mark Cavin provided insights into the operations of the LO generator for a

direct conversion system. Bo Liang helped me avoid the pitfalls in electrical engineering that only experienced professors can understand. Oliver Werther and Angelika Schneider brought their insights to bear on my research and helped me understand the many difficulties in this field, which are a mystery to many engineers. Bob Renninger provided Verilog AD converters and helped me resolve the difficulties associated with band decoding.

My colleagues at Texas A&M University provided me with a great deal of technical assistance, enriched my experiences by their advice, and provided me with their friendship. Xin Guan shared with me his novel idea on broadband LNA. Rui Xu worked out with me the first carrier gated UWB covering 3.1 to 10.6 GHz, and Meng Miao helped with many practical matters, especially circuit layout and measurements. Mohan Chirala contacted the foundry and helped package the chip as well.

I would like to thank my parents and my elder brother for their love, support, and encouragement during my many years in the graduate schools. Finally, I would like to express my love and gratitude to my beloved wife, Jianli Wei, and my daughter, Grace Sicheng Jin, for the endless care and the happiness that they brought me throughout my graduate studies.

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TABLE OF CONTENTS

CHAPTER Page

Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

When the Federal Communications Commission (FCC) agreed in February 2002 to allocate 7500 MHz of spectrum for unlicensed use of ultra-wideband (UWB) devices for communication applications in the 3.1-10.6 GHz frequency band [1], the move represented a victory in a long hard-fought battle that dated back decades. With its origins in the 1960s, when it was called time-domain electromagnetic, UWB came to be known for the operation of sending and receiving extremely short burst of RF energy. With its outstanding ability for applications that require precision distance or positioning measurements, as well as high-speed wireless connectivity, the largest spectrum allocation every granted by the FCC is unique because it overlaps other services in the same frequency of operation.

Previous spectrum allocations for unlicensed use, such as the Unlicensed National Information Infrastructure (UNII) band, have opened up bandwidth dedicated to unlicensed devices based on the assumption that "operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation." This means that the devices using unlicensed spectrum must be designed to coexist in an uncontrolled environment.

The style and format follow *IEEE Transactions on Microwave Theory and Techniques.*

Devices utilizing UWB spectrum operate according to similar rules, but they are subject to more stringent requirements because UWB spectrum co-exists with other existing licensed and unlicensed allocations. In order to optimize spectrum use and reduce interference to existing services, the FCC's regulations are very conservative and require very low emitted power from UWB devices.

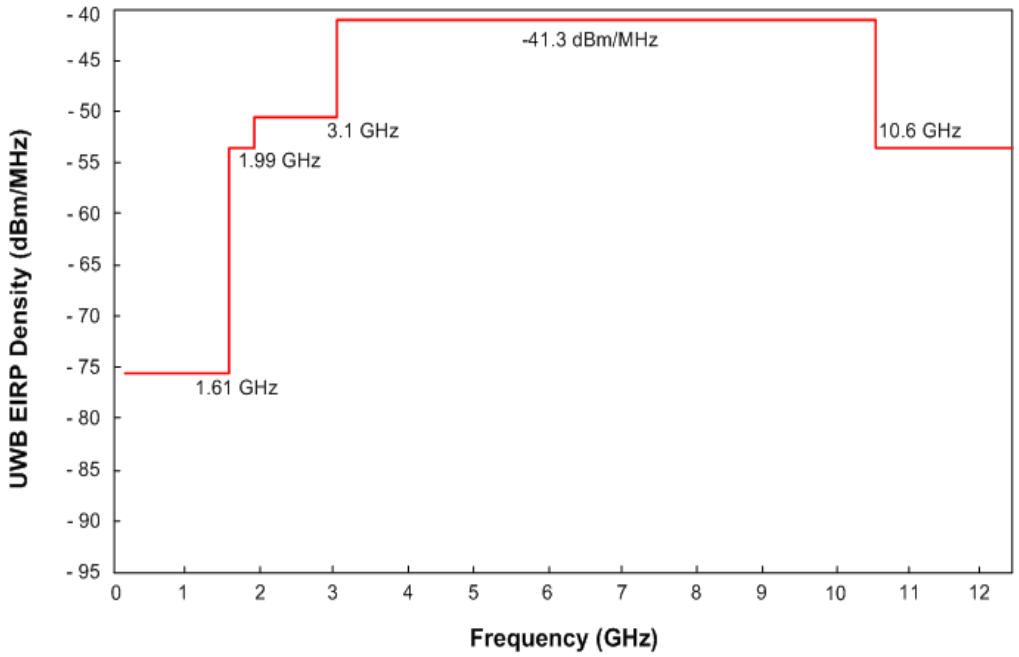


Figure 1. 1 FCC UWB EIRP spectrum mask. EIRP means Equivalent Isotropically Radiated Power from the transmitter antenna.

The FCC requires that UWB devices occupy more than 500 MHz of bandwidth in the 3.1-10.6 GHz band, according to the spectrum mask in Fig. 1.1. The power spectral density (PSD) measured in 1-MHz bandwidth must not exceed the specified -41.24 dBm, which is low enough not to cause interference to other **services, such** as

Wireless Fidelity (WiFi) operating under different rules, but sharing the same bandwidth within the UWB frequency range.

This presents a serious challenge to any UWB system because other services sharing the same band of operation on licensed or unlicensed bands are likely to have a much higher transmit power and, therefore, would subject UWB receivers (RXs) to considerable interference.

This spectral allocation has initiated an extremely productive activity for industry and academia. Wireless communications experts now consider UWB an available spectrum to utilize with a variety of techniques, and not specifically related to the generation and detection of short RF pulse as in the past.

One of the most innovative techniques involves utilizing only 500-MHz instantaneous bandwidth (the minimum amount allowed by the FCC ruling) and dividing that frequency band into smaller simultaneously transmitted sub-carriers. Such systems present high regulatory flexibility for worldwide operation because they enable independent control of portions of the emitted spectrum to adapt for different environments. A design based on this idea is the most acceptable technical solution for very high bit-rate, low-cost, and low-power wireless networks for personal computing (PC), consumer electronics (CE), and mobile applications. These applications can be satisfied by relatively short-range systems, within a user's personal space, assuming that all other performance requirements is met. Systems developed to date, such as IEEE 802.11b, 11a, or 11g, do not address this market because they are designed to integrate longer-range wireless networks and are integrated on devices that can support higher

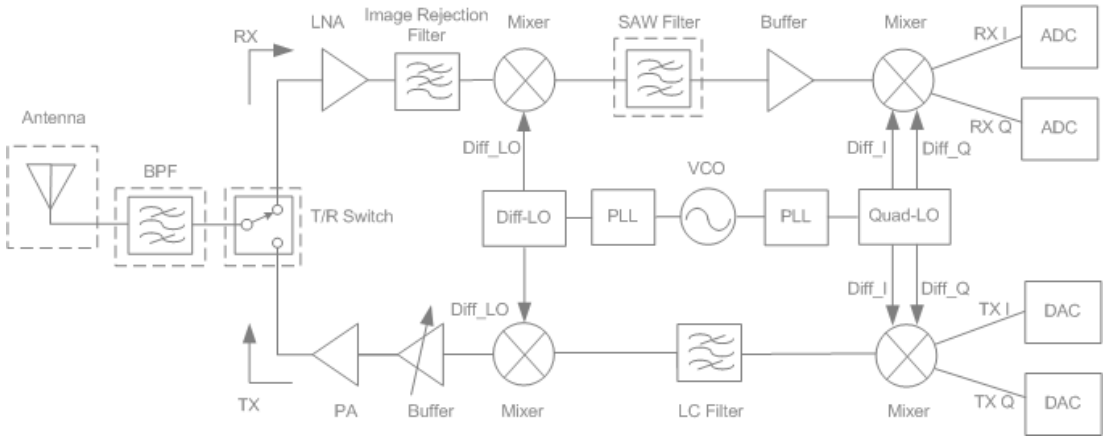
power consumption and cost. A specification is emerging today, led by the Multiband Orthogonal Frequency-Division Multiplexing alliance (MBOA), which is optimized to support these applications. The purpose of this standard is to provide a specification for wireless connectivity among devices within or entering the personal operating space. The data rate must be high enough (greater than 110 Mb/s) to satisfy a set of CE and multimedia industry needs for wireless personal area network (WPAN) communications. The standard also addresses the quality of service (QoS) capabilities required to support multimedia data types and mobile scenarios. There is also an extremely strong interest for even higher throughput and shorter range, up to 480 Mb/s, to support applications such as Wireless Universal Serial Bus (USB) or Wireless 1394 [2].

Devices included in the definition of personal area networks (PANs) are those that are carried, worn, or located near the body. Specific examples include devices that are thought of as traditionally being networked, such as computers, personal digital assistants (PDAs), handheld personal computers (HPCs), and printers. Also included are devices such as digital imaging systems, microphones, speakers, headsets, bar-code readers, sensors, displays, and pagers, as well as cellular and personal communications service (PCS) phones.

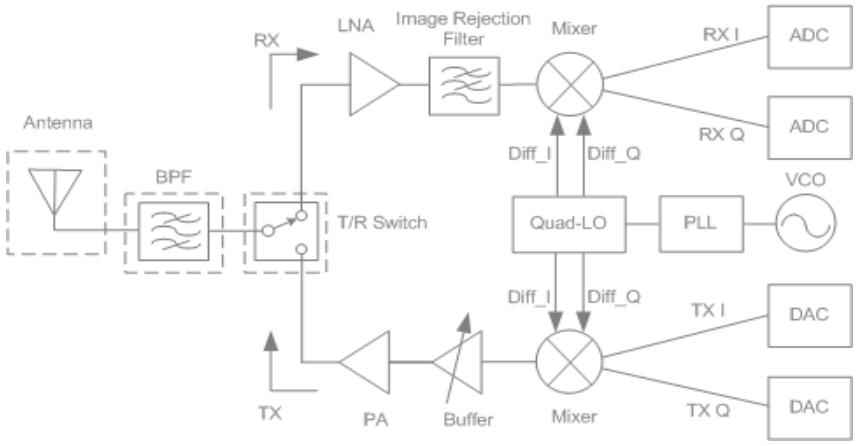
The long-term vision for these products is to enable personal devices with integrated wireless connectivity. Market considerations require that products be implemented in CMOS in order to achieve low-power and low-cost integration with other devices [3]. This is the best ticket to fulfilling the vision of integrated connectivity.

1.1 High Integration Trend of Wireless Product Circuitry

The synergism between economics and technological evolution, in hardware and software, drives wireless communication products to higher integration. If fact, the cost and ease of implementation of handsets becomes more critical, requiring aggressive reduction of the number of components. This evolution continues ultimately towards the radio frequency system on single-chip (RF-SoC) or the radio frequency system in single-package (RF-SiP) for all wireless products. The high integration trend requires architectural and technological innovations. For instance, the RF part of mobile phone has already move from super heterodyne to direct conversion architecture and in 2006 direct conversion has taken over 95% of the handsets. Technology has already moved from Gallium arsenide (GaAs) to silicon and is moving towards the most cost-effective solution using Complementary Metal-Oxide-Semiconductor (CMOS) process at RF frequencies (CMOS-RF or RF-CMOS). Although disbelievers claim that CMOS-RF will only be chosen for low-end, low-cost systems, while the much more powerful SiGe BiCMOS technology remains the choice for high-end systems, it has already been shown that CMOS has become the major process for most current wireless products, such as Global System For Mobile Communication (GSM), Code-Division Multiple Access (CDMA) and WiFi.



(a)



(b)

Figure 1.2 Simple RF transceiver architectures (a) Heterodyne or IF-based, and (b) Homodyne or direct conversion. The component count is significantly lower for homodyne system. The dashed blocks are currently external parts of integrated transceivers.

1.2 Direct Conversion Transceivers

The wireless products consist of functionally two parts: the radio-frequency (RF) and analog front-end and base band digital back-end. The back-end of modern wireless products is already highly integrated. The RFIC design industry is increasingly looking at direct conversion architecture to facilitate higher integration by reducing the number of external components**,** which are, on the other hand, required by the traditional heterodyne RF architecture.

A sample heterodyne RF transceiver front-end is shown in Fig. 1.2 (a). In this architecture, the receive RF signals are first passed through a band pass filter, and then switched to a low-noise amplifier (LNA). Due to its gain, the LNA essentially sets the signal-to-noise ratio of the receiver chain. The amplified signals are filtered for improved image-rejection and down converted to an intermediate frequency (IF) with a mixer. The signals at IF are then filtered for channel-selection and shifted in frequency to baseband by a second mixer. The transmit process is complementary to the receive process. During transmission, the signals at baseband are upconverted to the RF frequency using an IF stage. A power amplifier (PA) is used to drive the antenna. A transmit-receive (T/R) switch is used to connect/disconnect the antenna during the transmit and receive processes respectively.

In the direct conversion or homodyne architectures, as in Fig. 1.2 (b), the receiver mixes the incoming RF signals with the carrier frequency to generate signals directly at

baseband. Similarly, the signals are directly upconverted to the RF carrier using only one mixing step during transmission.

Recently, the RF front-end has switched from conventional 90 years old super-heterodyne receiver topology to direct conversion receiver. It is indicated that by 2007 a direct conversion receiver was used in 95% of all GSM cellular phones up from 40% in 2001. This is due to the fact that switching to direct conversion in GSM handsets and CDMA cellular phones reduces component costs as much as 30% and 70%, respectively [4].

Different flavors of direct conversion architectures exist in the receive as well as the transmit patch. Direct conversion receivers are zero-IF [5] and low-IF receivers [6]. Both architectures feature single-stage quadrature downconvesion without high Q filters. The architectures also fully exploit the digital circuitry capability of CMOS to include specially designed digital circuits in the chip to help improve the analog functions, such as image rejection, channel selection and demodulation. For instance, a digital circuit may adjust the phase of the I and Q channels of an image rejection mixer to help improve the image rejection. The bottlenecks of zero-IF receivers are $1/f$ noise, process mismatch-related offset, and self-mixing related offset that corrupt the wanted signal at low frequencies. The low-IF receiver alleviates this problem by setting the IF frequency to typically half the channel bandwidth [6]. If the external high Q, area expensive filters are removed, then higher demands on the analog building block performance are required, thus increasing the power consumption. For instance, if the filter is removed, then the differential mixer needs to be replaced with a quadrature

mixer so that good image rejection can be obtained, which leads to higher current consumption.

Direct conversion transmitters are mostly Cartesian I/Q modulators, which are in fact the equivalent of the zero-IF receive architecture. Quadrature up-conversion alleviates the need for high Q filters. Another direct conversion transmitter that is emerging is the direct modulation of a fractional-N synthesizer by the digital data, which presents an elegant and highly integrated solution [7].

1.3 RFIC in CMOS Processes

In the early 1980s, the GHz spectrum was mainly the territory of III-V compound semiconductors. Since the cost of silicon wafers is much lower than that of GaAs, silicon technologies become increasingly utilized in the market in the late 80s. Nowadays, SiGe bipolar transistor improved its current gain cut off frequency, f_T, to more than 100 GHz in 0.13 μm process. In the total semiconductor revenue for digital and RF, GaAs only takes up 1% while silicon (Bipolar and CMOS) takes up 99% [8].

Among the currently used processes for RF front-end, i.e. CMOS, SiGe BiCMOS, SiGe Biploar and GaAs, the cost of a CMOS wafer is the lowest. Meanwhile, CMOS can benefit from a high-volume market, which aggressively scales technology to improve the digital performance, which at the same time improves the RF performance. The International Technology Roadmap for Semiconductors (ITRs) [9] predicts a transition to another process technology every 3 years. In reality, this happens every 2

years! While industry has maintained Moore's law for almost 30 years, some saturation in the scaling is expected when fundamental limits are reached, e.g. gate oxide thicknesses at atomic level. But performance can still be increased by advanced techniques, i.e. new materials like Cu interconnects, materials with small dielectric constants relative to silicon dioxide (low-dielectric-constant dielectrics) and more metal layers, all of which are at the same time beneficial for the RF performance of CMOS technology.

The main reason to favor CMOS for RF integration is certainly the cost. It has been estimated that RF-CMOS increases the wafer cost compare to pure CMOS by around 15%, due to Metal-Insulator-Metal (MIM) capacitances, resistances, and etc. But SiGe-BiCMOS increases the wafer cost by more than 40% [10]. In SiGe-BiCMOS, performance with low power is more easily obtained, but because of the lack of competition in this industry compared to CMOS, the price is not likely to decrease. Together with the compatibility of CMOS with the digital back-end, CMOS is an attractive cost-effective solution for integration of RF front-ends, with as goal full RF-SoCs.

It is worth examining the historic road maps of the RFIC developing towards CMOS and Direct-Conversion. The trend towards higher degrees of integration in the most cost-effective technology can be retraced in the history of mobile transceiver, presented by key publications. In the early years of mobile communications, all RF front-end ICs for cellular and cordless phones were integrated in Si bipolar, with good

examples as [11] in 1993 and [5] in 1994, where people already thought of a highly integrated solution by using zero-IF architectures [5].

In the following years, publications emerged with transceiver building blocks in BiCMOS due to the continuing improvement of mainly the bipolar transistor. In 1995, the first GSM transceiver ICs were published, [12] in BiCMOS and [13] in Si bipolar, both with superheterodyne architectures with external Surface Acoustic Wave (SAW) filter and LC-tank, loop filters.

In the same year CMOS made its entry in the GHz range with a 900 MHz low-IF receiver [6] and a high performance 1.8 GHz VCO [14]. From then on research for RF-CMOS took off rapidly. In 1998, the first single-chip CMOS transceiver, demonstrating the feasibility of achieving cellular specifications in CMOS, was presented by KULeuven [15]. The integrated circuit (IC) was intended for Digital Cellular System at 1800 MHz (DCS-1800) and combined a highly integrated low-IF receiver with a direct conversion transmitter, using an up-converter with a very low input IF and an on-chip VCO. Meanwhile, [16] [17] presented a 900 MHz single-chip transceiver for the Industrial, Scientific and Medical (ISM) band by RF-CMOS. In 1999, [18] demonstrated a single-chip transceiver for 900 MHz spread-spectrum cordless telephone with a direct conversion transceiver. A 5 GHz Wireless Local Area Network (WLAN) CMOS chip-set with direct conversion transceiver was published by Bell Labs in 2000 [19]

It was in 2000 that the highly demanded technical barrier of the GSM cellular phone was overcome by the use of RF-SOC in CMOS. [20] presented a 2 V supply voltage CMOS cellular transceiver front-end for DCS-1800. This IC was the first single-

chip CMOS transceiver front-end with a complete on-chip PLL, including VCO and loop filter, that achieved all the requirements of the stringent DCS-1800 cellular system. Industry, on the other hand, mainly employed Bi-CMOS and bipolar, but became convinced of the feasibilities of the RF-CMOS, which is reflected in the first commercial CMOS transceiver chip set for GSM [21] [22].

In parallel, the integration of RF WLAN transceivers in CMOS gained more and more attention with a full session at the International Solid-State Circuit Conference (ISSCC) in 2001 on WLAN, featuring two CMOS Bluetooth transceivers [23], [24] and one CMOS Bluetooth SoC [25]. In 2002, more Bluetooth transceivers and a CMOS IEEE 802.11a transceiver [26] were published and even Universal Mobile Telecommunications System Third Generation (UMTs 3G) [27] and Wideband CDMA (WCDMA) [28] transceiver blocks in CMOS, were presented, proving the increasing interest and belief in RF-CMOS for research as well as commercial use.

Becoming a full session at ISSCC from 2005, UWB research, including Direct Sequence UWB (DS-UWB), gated pulses, and MB-OFDM, is mainly credited by universities. Industry was simultaneously launching UWB RF front-ends by SiGe Bi-CMOS [29] and RF-CMOS [30]. It is fore casted that MB-OFMD will exhibit a very fast development at the beginning of 2008. Also, in 2008, the first worldwide MB-OFDM UWB transceiver was published by industry [31]. Though still built by SiGe Bi-CMOS, it is no doubt that RF-CMOS is the utmost goal for UWB for various consumer electronics products because of its low cost, high-integration capability, and fairly good performance.

1.4 Dissertation Organization

This dissertation aims to demonstrate some strictly required building blocks and investigate new methods of designing RF switches for UWB radar and communication applications, with very impressive performances, in conventional RF-CMOS processes. A new way to generate timing gated multiple pulses for UWB is also presented for sensing applications, which diversifies the current UWB regimes. Chapter II discusses the detailed specifications that integrated CMOS switches need to meet so that they would be a viable alternative to the existing GaAs MESFETs. Then we propose a broadband alternative using MOSFET in tripe well whose substrate is biased using resistors. The focus of Chapter III is the ultra-wide band transmit/receive switch (T/R switch) design. A broadband topology with low loss, high linearity and compact layout is presented in detail with simulation and experiment. The measured results shows the best overall performance among the reported CMOS switches to date, and it is the first CMOS switch able to provide less than 1 dB loss over the entire UWB frequency span. In Chapter IV, a Time-gated Carrier-based UWB generation is presented with very low power consumption, and it's feasible of meeting FCC regulations. The key block of the transmitter, a single pole single throw switch (SPST) functioning as a multiplier in time domain, is discussed from the point of view of topology, simulation and experimental testing. Also the UWB signal generation method is demonstrated. Another key block of the UWB transmitter, a low phase noise, low harmonic integrated CMOS VCO, is the

main topic of Chapter V. The key parameters of VCO associated with the topologies are discussed in detail and a new transistor level optimization method is proposed. Lastly, conclusions are summarized in Chapter VI.

CHAPTER II

CMOS RF SWITCH AND INTEGRATED INDUCTOR

RF switch is an important building block in wireless transceivers. Operating at deep triode region with a small channel resistance, MOSFET is a very feasible device to implement integrated switches for various applications. For instance, a Transmit-Receive switch is the first block in the UWB integrated transceiver connecting external components like BPF or Antenna. The main consideration of the RF switch design is extremely broadband impedance matching with very low insertion loss in ON path and high isolation in the OFF patch. In this chapter, starting with a review of MOSFET physics functioning as a switch, a synthetic transmission line concept is presented by lump elements. Finally, design of high quality integrated monolithic inductors in CMOS process is analyzed.

2.1 Switch Devices

In digital application, a switch device is characterized by metrics such as its switching speed, and input capacitance, etc. It must be noted that the switching speed is also affected by the loading capacitance caused by the subsequent component to the switch. For RF application, a switching device is commonly characterized with the help of the circuits of Fig. 2.1 in a 50-Ohms network. When the switch is closed and the signal passes through, some power is lost in the switch due to its imperfections. This loss

is commonly referred to as the insertion loss (IL) of the switch. In the close-sate, the linearity of the switch is specified by its one dB compression point, P_{1dB}. In the open-state, the switch blocks the signal from passing to the load and the attenuation by the switch is characterized as the isolation (ISO) of the switch. Insertion loss, linearity, and isolation are key metrics of a RF switch. Moreover, the RF switch, like the other RF blocks, must provide good input and output matching over the specific frequency range.

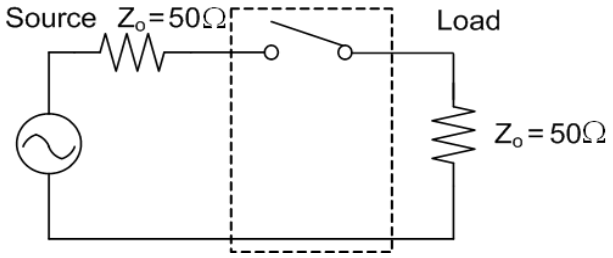


Figure 2.1 Network to characterize a RF switch. The impedances of the source and load are 50 Ohms. IL and linearity are measured when the switch is closed while the ISO is measured when the switch is open. The input and output matching are characterized by return losses.

2.2 MOSFET and MESFET

MESFETs are majority carrier devices, which make them suitable for high speed and high frequency operation. It can be implemented using silicon, GaAs, and InP. MESFETs implemented in silicon are incapable of handling large powers and typically are slower than those implemented using other materials, such as GaAs. MESFETs

implemented using GaAs are commonly used for high-power and high frequency applications. GaAs has a large band gap, and hence a large breakdown voltage that permits high-voltage operation without reliability concerns. Moreover, the high low-field mobility of GaAs enhances the usable bandwidth of the device. GaAs MESFETs also use a semi-insulating substrate, which further lowers loss in the device. The performance of GaAs switches currently achieves very low loss (< 1dB at 2 GHz) [32], high power (>1W) [32], and high frequency (20 GHz) [33].

The silicon-based MOSFET is currently the cheapest of all the switch options and it also enables to implement an RF switch integrated with other blocks to build a system on chip. The on-resistance of the silicon MOSFET, however, is significantly worse than a GaAs MESFET due to poor electron and hole channel-mobilities at low electric fields. Modern CMOS processes provide very small channel length MOSFETs with a good $R_{on} \times C_{off}$ product, where R_{on} is the on-resistance while C_{off} is off-capacitance of the MOSFET respectively. Meanwhile, the thin gate oxide and small channel length permit a low voltage operation only, thus limiting the linearity and power handling capability. CMOS switches cannot be used for high-power RF applications. The normal performance of MOSFET switch at RF is poor compared to its GaAs counterparts. Various researches in CMOS switches have been widely pursued recently to improve the performance as the size of the MOSFET scaling down [34] [35].

Fig. 2.2 shows an equivalent-circuit model of the MOSFET for RF applications. The gate resistance, R_G, is very small because of the multiple figure structure of MOSFET is normally implemented in the latest CMOS process resulting in a parallel

poly gate resistance. The channel resistances, R_{C1} and R_{C2}, and the substrate resistances, R_{B1}, R_{B2} and R_{B3}, are the main sources of loss in the MOSFET. The substrate resistance, R_{B3}, can be reduced by grounding the substrate as close to the device as possible. The voltage controlled current source, $g_m V_{gs}$, stands for the capability of the MOSFET to convert the gate to source voltage, V_{gs}, into the current from drain to source, where g_m is the transconductance of the MOSFET. The low quality factor of the source and drain parasitic junction capacitors, C_{SB} and C_{DB}, can also lead to significant losses, especially as the frequency of operation increases. The linearity of the MOSFET switch is limited for large signal swings due to conductivity modulation caused by a changing gate-source (Vgs) and drain-source (Vds) voltage for a large signal input. Another cause of non-linearity is the parasitic source and drain junction diodes which can clip the signal at about 0.7 V above the power supply (i.e., 0.7 V + Vdd) or 0.7 V below ground.

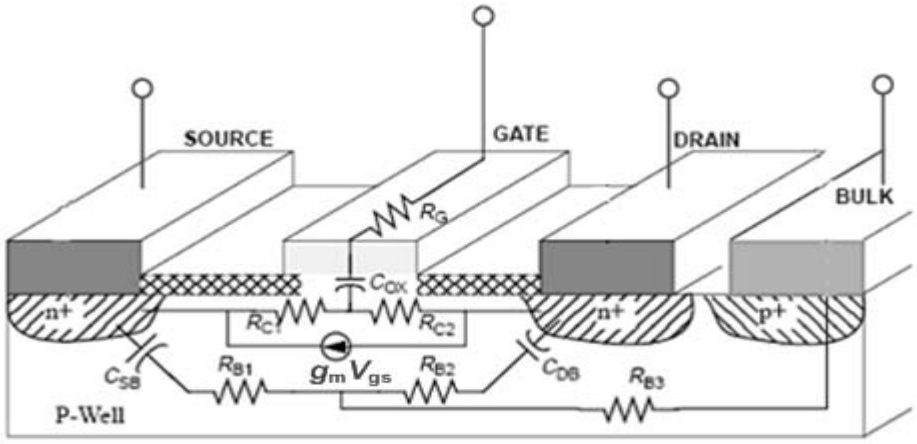


Figure. 2.2 Simplified MOSFET cross-section and physical origin of main RF small signal equivalent circuit elements.

2.3 MOSFET with Floating Bulk

In order to reduce the loss of the MOSFET switch, much work was done to optimize the size of MOSFET devices to compromise the on resistance and parasitic capacitance [34] [35]. Moreover, for a given size device, it might be noted that the loss caused by the substrate can be reduced by making the substrate resistance, R_{B3}, very small, or making it extremely large [34]. The former idea induced the practice of shorting the substrate by paralleling hundreds of vertical contacts connecting bulk and P^- substrate [34]. The later thought is realized by making the substrate float at RF frequency [35].

Floating the bulk also helps to improve the linearity. In the MOSFET switch the gate is normally biased by a large resistor and hence the gate becomes a floating node. The gate voltage V_{gs} remains approximately constant and is always higher than the source and drain voltages, which are equal, by the control voltage applied to the gate. The source/drain junction diodes can still turn on and distort the incoming signal with large voltage swings. When the source/drain diodes are turned on, the bootstrapping fails. While the floating bulk can be realized by an inductive bulk bias as shown in Fig. 2.3, [35], the parallel integrated LC tank connecting the substrate resistance, shown in Fig. 2.3, provides a high impedance at resonant frequency of the tank and thus enables the bulk floating at this frequency. The DC potential, on the other hand, is the same as the ground because there is no DC current flowing through the external bias inductor and the internal substrate resistor. Apparently, this technique is not acceptable for a

broadband switch as the LC tank resonates at a fixed frequency, thus limiting this to a very narrow band use.

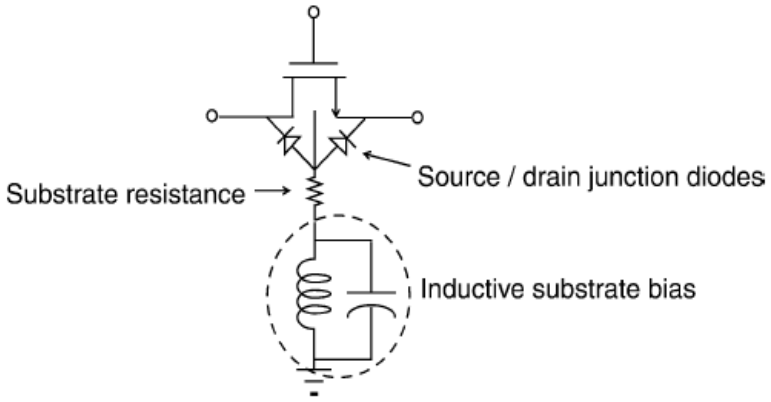


Figure 2.3 MOSFET with inductive substrate bias.

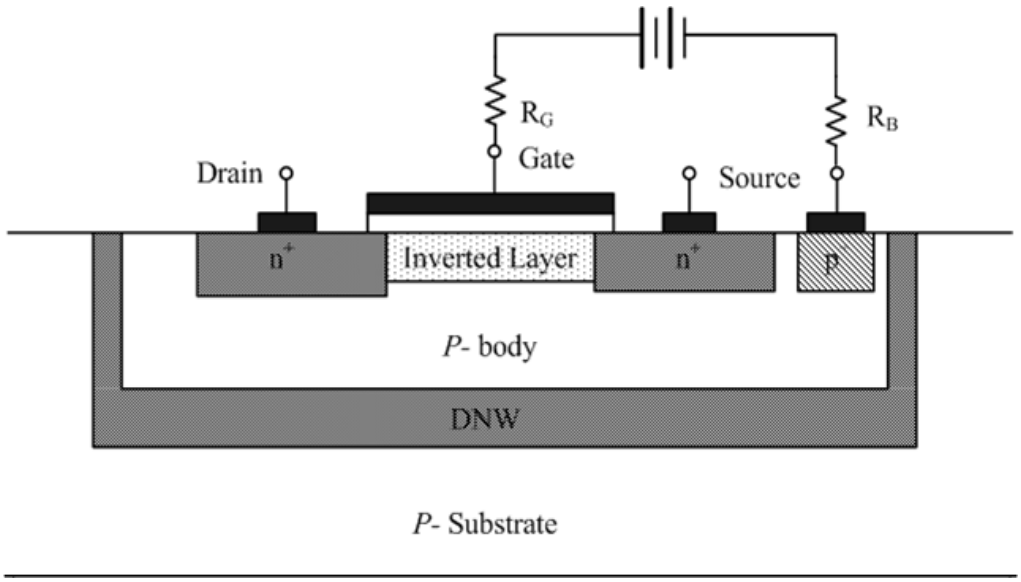
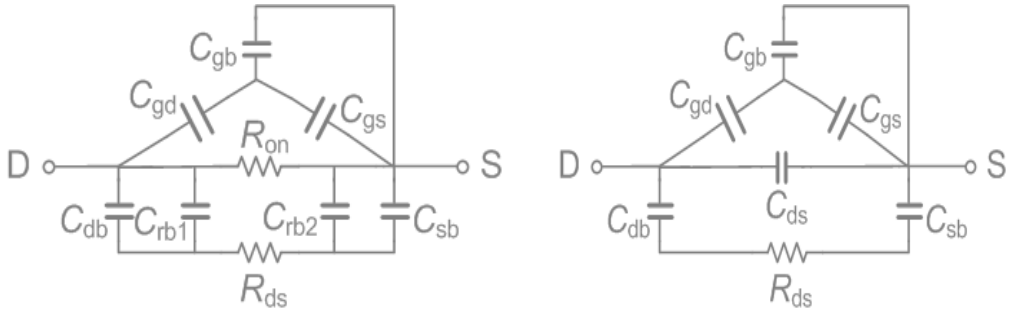


Figure 2.4 Simplified physical structure of nMOS transistors with Deep N Well (DNW) under on state.

Resistively floating the bulk is made practical for broadband switch by using the triple well device provided by majority of commercial CMOS foundries [36]. Fig. 2.4 shows a simplified geometry of these nMOS transistors with the gate biased so that the devices are operated under on-state. The deep N well (DNW) separates the bulk of the nMOS transistors from the p-substrate. The p-n junctions between the p-bulk and n+ regions form a pair of parasitic drain-bulk (or drain) and source-bulk (or source) diodes. With DNW, large resistors can be applied directly to the bulk of nMOS devices, making it float at high frequencies without latch-up problems that would result in RF ICs consisting of both nMOS and pMOS without DNW.



(a) (b)

Figure 2.5 Simplified small-signal equivalent-circuit models for MOSFETs with the bulk and gate floated under on-state (a) and off-state (b). D and S stand for the drain and source, respectively.

Floating the bulk forces the bulk resistance, R_{B3} in Fig. 2.2, underneath the source and drain junctions open with respect to the ground, leading to a much smaller resistive loss in the conductive p-bulk than with the bulk grounded. Fig. 2.5 shows simplified small-signal equivalent-circuit models for the on and off states of floating-bulk MOSFETs when the gate is floated with a large resistor. R_{ds} represents the resistive loss in the p-bulk between the source and drain. Using large gate widths for advanced sub-micron CMOS devices can produce R_{ds} within several ohms, thereby resulting in low loss in the bulk. C_{gs} and C_{gd} represent the gate-source and gate-drain capacitances due to the overlapping between the gate and diffusion areas. C_{gb} represents the gate-bulk capacitance. C_{db} and C_{sb} are the junction capacitances between the drain-bulk and source-bulk, respectively. C_{rb1} and C_{rb2} in Fig. 2.5 (a) represent the distributed capacitances between the inversion layer and bulk. C_{ds} in Fig. 2.5 (b) is the source-drain diffusion capacitance in a multi-finger MOSFET.

2.4 Distributed Structure and Synthetic Transmission Line

Synthetic transmission lines can be used to alleviate the bandwidth limitation in

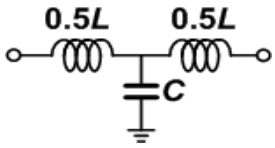


Figure 2.6 Lumped-element network representing one element of the artificial transmission line.

RFICs [37]. A synthetic transmission line can be created by cascading multiple sections of an identical series inductor and shunt capacitor, shown in Fig. 2.6, whose inductance and capacitance can be properly chosen to realize a particular characteristic impedance and velocity. Such a synthetic transmission line approximates a transmission line over a finite bandwidth. The characteristic impedance of the artificial transmission line and its phase velocity can be found, respectively, as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.1}$$

Where Z_0 is the characteristic impedance of the artificial transmission line.

$$v_P = \sqrt{LC} \tag{2.2}$$

Where v_P is the phase velocity of the artificial transmission line.

For $f << f_C$, where f_C is the cut-off frequency of the artificial transmission line, which normally determines the bandwidth of the distributed structures, given as

$$f_c = \frac{1}{\pi \sqrt{L \cdot C}} \tag{2.3}$$

If the desired characteristic impedance Z_0 of the transmission line is fixed, the cut-off frequency f_C can be expressed as

$$f_c = \frac{1}{\pi \cdot C \cdot Z_0} \tag{2.4}$$

(2.4) shows that the bandwidth of an artificial transmission line decreases as the value of the capacitance C increases.

Distributed amplifier is well known to have broadband gain flatness by using the artificial transmission lines [38]. The basic design principle of distributed amplifiers is based on forming two artificial transmission lines at the input and output ports of the constituting gain cells by periodically combining serial inductive components with the parasitic capacitors of the gain cells. Essentially, the input and output capacitances are absorbed into the artificial transmission lines, resulting in an extremely wideband performance.

This concept inspires the design of the broadband RF switch in CMOS, where the MOSFET transistor normally has various parasitic capacitances, such as C_{gb}, C_{gs}, C_{gd}, C_{db} and C_{sb}, is shown in Fig. 2.5.

2.5 Coplanar Spiral Inductor in CMOS

The high-quality inductor is one of the important passive structures for RFIC design. One way to realize high quality inductors with large inductances is gold bonding

wires [14], which are readily available in the IC assembly process. Since gold is highly conductive, the resistive loss of the bonding wire is very low. The parasitic capacitance is limited and mainly due to the bonding pads. However, due to lack of yield and repeatability (variations of $\pm 6\%$) the technique is less popular for mass production.

For monolithic integration, planar spiral inductors laid out in standard metal routing levels of the IC remain the desired topology of designer looking for inductors. The cost of this solution is lower that that of bonding wire inductors and the die area is reduced with an order of magnitude. Most importantly, the yield and repeatability is almost perfect since processing accuracy (< 0.1 μm) is negligible with respect to the inductor size (100×100 μm^2). Although the integrated planar inductor is the most elegant solution, its quality is limited by several parasitics. The most important one is the metal resistance, which increases for higher frequency due to the skin effect and eddy currents, and substrate losses, especially for highly doped CMOS substrates. To decrease the series resistance, multi-level and extra thick metallization, which is a standard feature in most modern deep-submicron processes, are used. To eliminate substrate losses, the substrate is selectively etched away underneath the inductor [39]. However, the extra post-processing steps associated with the etching undermine the main advantage of the planar integrated inductor, i.e. its low cost.

Therefore, the following section focuses on the integration and analysis of optimal high-quality planar inductors in standard CMOS technology, without tuning, trimming, or extra post-processing steps.

2.5.1 First-Order Planar Inductor Model

Integrated planar inductors are mostly designed using a spiral-shaped metal connection routed in one or more of the standard available metal levels. A general reference for extensive calculations of planar rectangular micro-electronic inductors is given in [40]. The famous Greenhouse article presents a method for accurately calculating the inductance value, based on summing or subtracting of the appropriate self- and mutual inductance values of the different segments of the inductor. Calculation of the total inductance value of a full spiral inductor involves the calculation of every mutual inductance between every possible couple of segments. Due to the large number of calculations, the formulas can be embedded in a custom computer program, yielding quite accurate results for the calculated inductance value. Unfortunately, the Greenhouse method does not support segments with 45^0 angles and does not provide calculation for the parasitic losses in the inductor.

In [37], several crude (0th order) calculations are given for integrated spiral inductors. These formulas are only useful for quick hand-calculations as a starting point for inductor design prior to verification with a field solver. This formula is used for the construction of a square spiral inductor:

$$L \approx \mu_0 n^2 r = 4\pi \cdot 10^{-7} n^2 r \qquad (2.5)$$

With μ_0 the magnetic permeability of free space, n the number of turns and r the radius of the spiral in m. Again, the calculations are only valid for rectangular inductors.

Quality factor, Q, is normally used to describe the quality of the inductor and is generally defined as:

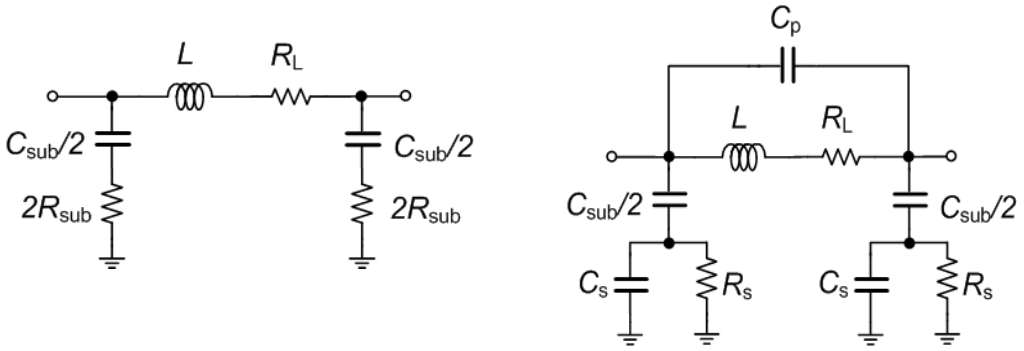
$$Q = 2\pi \cdot \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} \qquad (2.6)$$

Where the energy stored in the magnetic field is of importance, not the electrical energy, which is counterproductive for an inductor. The higher the Q, the better the inductor.

It is known that the circular shape inductor has the best Q among the various shapes of spiral inductors because it has the shortest winding metal and hence smallest series resistance. But to today, any 0th order formula does not provide accurate calculations to the circular spirals. On the other hand, today's CMOS processes support 45^0 angles winding, enabling the integration of octagonal inductors, which better approximate the Q of a circular inductor.

Generally, a complete passive inductor can be modeled by the simple equivalent circuits shown in Fig. 2.7 (a). The inductor L has a parasitic resistance R_L and a capacitance C_{sub} to ground, mainly the oxide capacitance, in series with the substrate resistance R_{sub}. An extension to the simple model is shown in Fig. 2.7 (b). Shunt capacitance C_p over the inductor mainly takes into account the capacitance of the cross-

under metal line to connect the inner turns to the outside world. This capacitance is alleviated by balanced or differential inductor design. C_{ox} is the actual oxide capacitance between the inductor and the substrate. C_s and R_s are the capacitance and the losses of the actual substrate, including loss current through the oxide and eddy currents induced in the substrate by magnetic fields. This extended model can be fitted onto the measured data of almost every integrated spiral inductors up to 20 GHz [41].



(a) (b)

Figure 2.7. First order models for passive integrated inductors: (a) simple and (b) extended.

Based on the first order model of the inductor shown in Fig. 2.7, the formula of quality factor of the inductor, Q, is given by

$$Q = \frac{\omega L}{R_L} \cdot \left[1 - \left(\frac{\omega}{\omega_0} \right)^2 \right] \tag{2.7}$$

Where L is the inductance, R_L is the series resistance, and ω_0 is the self-resonance frequency of the inductor. Note that Q is zero at the DC and self-resonance frequency, and has a peak value at one midrange frequency. By making the derivative of (2.7) as zero, the peak Q value, Q_{max}, and the frequency giving a peak Q, ω_{max}, can be derived as

$$Q_{max} = \frac{2}{3} \cdot \frac{\omega_0 L}{R_L} \quad \text{and} \quad \omega_{max} = \frac{\omega_0}{\sqrt{3}} \tag{2.8}$$

Though the losses mechanisms are more complicated and will be described in the following section, the first order model helps in designing high Q planar inductor by optimizing the layout for low loss and high self-resonance frequency.

2.5.2 Losses in Integrated Planar Inductors.

2.5.2.1 Metal Loss

For lower operating frequencies, the series resistance of the inductor is the DC resistance of the metal tracks, i.e. the product of the sheet resistance of the metal and number of squares of the metal tracks. Therefore, multiple metal layers should be used as much in parallel as possible to reduce the DC resistance of the metal. But this stacked parallel does lower the self-resonance frequency due to lower layers bringing larger

parasitic capacitance. At high frequencies, there are two effects causing a non-uniform current distribution in the metal tracksresulting in increased metal losses: the skin effect and eddy currents. The skin effect pushes the current to the outside of the conductor, such that 63% of the current is contained within a skin depth, δ, defined by (2.9), where σ_M is the conductivity of the metal and μ_0 is the magnetic permeability of free space which is very close to that of aluminum and copper. The effective area of the conductor is reduced so that the current flows and hence the resistance increases. Due to the skin effect, the current density is $J = J_s \cdot e^{-x/\delta}$, where J is the current density of at the depth x and Js is the surface current density. So the effective depth with uniform Js density can be estimated as Eq. (2.10), where d is the effective depth and T is the actual thickness of the metal.

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma_M}} \tag{2.9}$$

$$d = \int_0^T J_s \cdot e^{-x/\delta} dt \Big/ J_s \tag{2.10}$$

The effective depth can then be calculated roughly as $\delta\left(1-e^{-T/\delta}\right)$. The effective resistance of the metal can then be described by Eq. (2.11).

$$R_{L,\delta} \approx \frac{L}{W \cdot \sigma_M \cdot \delta\left(1-e^{-T/\delta}\right)} \tag{2.11}$$

Where L and W are the length and width of the metal and $R_{L,\delta}$ is the effective resistance of the metal due to the skin effect. For aluminum used for IC interconnects, $\sigma_{Al} = 3.33 \cdot 10^{-7}\, 1/(\Omega \cdot m)$, such that the skin depth is approximately $\delta_{Al} \approx 1.95 \mu m$ at 2 GHz and $0.87 \mu m$ at 10 GHz. For copper, $\sigma_{Cu} = 5.95 \cdot 10^{-7}$ $1/(\Omega \cdot m)$, such that the skin depth is approximately $\delta_{Cu} \approx 1.46 \mu m$ at 2 GHz and $0.65 \mu m$ at 10 GHz. It is apparent that due to the skin effect very wide metal tracks are useless in high-frequency inductors, since only a small part of the conductor is actually used, especially for better conductive material.

A second effect is eddy currents generated in the metal by the magnetic field of the inductor. The situation is depicted in Fig. 2.8 for one side of the inductor with 4 turns carrying a counter-clockwise current $I_{ind}(t)$. This current generates a magnetic field $\vec{B}_{ind}(t)$, which is most intensive in the center of the inductor. The magnetic field is perpendicular to the page and pointing out in the center e . For an inductor with traces in the inner turns, the magnetic field goes through the inner turns instead of through the center of the inductor. It induces eddy currents in these inner turns, which induce an opposite magnetic field $\vec{B}_{eddy}(t)$. The counteracting field decreases the inductance significantly at higher frequencies. Moreover, the eddy current I_{eddy} causes a non-uniform current distribution dramatically in the inner conductors: At the outer side of the conductor, the eddy currents cancel the inductor current, i.e. the total current is pushed to the inside of the conductor. As a result, at higher frequencies, the resistance of the inner

turns increases dramatically. To maintain the inductor quality, “hollow” inductors should be designed with no inner turns.

Since the losses with these two effects are too complex to calculate analytically, a full Electromagnetic (EM) Simulator is necessary for high frequency inductor optimization.

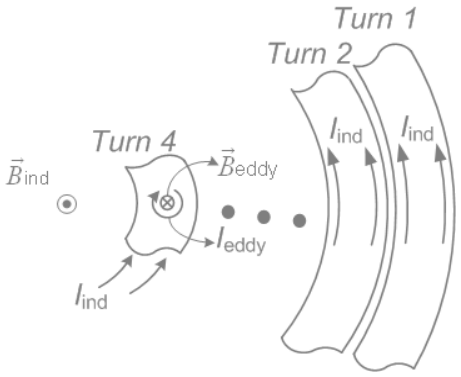


Figure 2.8 Eddy current in the inner turns of planar inductors.

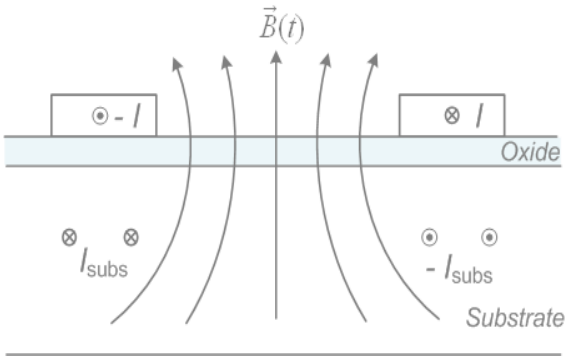


Figure 2.9 Substrate currents underneath planar inductors.

2.5.2.2 Substrate Loss

Previous CMOS technologies use epi-wafers with a heavily doped and low resistive substrate. Although beneficial for digital design, it is a killer for analog and GHz RF circuits' design. In highly conductive substrates, current induced by the magnetic field of the inductor are free to flow, causing extra resistive losses in the substrate and degradations of both inductance and quality factor. Fig. 2.9 gives a typical cross section of a one turn planar inductor on a silicon substrate. The inductor carries a current I at one moment in time (direction denoted by $\odot$, out of page and $\otimes$ into the page), inducing a magnetic field $\vec{B}$. According to Daraday-Lenz, this field induces counteracting currents in the substrate, I_{subs}. The larger the inductor, the larger the magnetic field penetration in the substrate and the more currents, and thus losses are

induced. In addition, these substrate currents induce a magnetic field opposite to the magnetic field of the inductor, and as a result, the total inductance of the inductor is reduced.

Fortunately, most of today's CMOS processes use relative high-resistive substrate. The magnetic field causes much less substrate currents in these substrates, greatly reducing the effect on the losses in the substrate and the reduction of the inductance. Again, an analytic calculation of the substrate losses is cumbersome, and simulations by EM simulators are thus unavoidable.

There are some techniques that can be applied to reduce the substrate losses, but each of them should be verified by EM simulation since the modeling of the influences is very challenging. First, when substrate losses are an issue, it is best to stay away from the substrate by using only the top metal years, if possible. Secondly, especially in the case of highly-conductive substrates, the metal layers of the technology can be laid out in series instead of parallel (stacked multiple layer inductor). As a result, the area of the inductor and thus the substrate losses is greatly reduced for the same inductance. The disadvantage is that the DC series resistance of the inductor increases seriously compared to a single layer structure with the same inductance. A third, more elegant solution is the use of patterned ground shields [42]. To cancel energy dissipation in the substrate a short or an open must be realized. The open is using high-resistive substrates or etching out the substrate, the short is realized by shielding the substrate from the inductor. Highly conductive shields on aluminum layer (solid or patterned) present low electrical losses, but decrease the inductance because of the counteracting eddy current.

A patterned poly-silicon ground shield is better than a solid Al shield for increasing the quality factor, Q, with 33% (at optimal frequency) [42]. The ground shield replaces the lossy, frequency-variant C_{sub}, shown in Fig. 2.7 (b), with a larger, but lossless and frequency-invariant capacitance. This reduces the self-resonance frequency of the inductor, but also decreases the losses in the substrate, resulting in higher Q.

2.5.3 Integrated Planar Inductor Design Guidelines

The optimization process of designing integrated frequency inductors on silicon is done normally by EM simulations, but some design guidelines can be offered by distilling and summarizing the discussions in the previous sections.

The shape of the winding track: For a given inductance, circular shape spiral gives the best Q_L and thus the closer to circular shape is more preferable. Typically, an octagonal inductor is available in latest CMOS processes.

The width of the metal tracks: For higher frequencies, the width of the metal tracks must be limited; wider tracks means that the inner turns of the inductor become smaller in diameter and contribute less to the inductance, but more to the resistance. To counter this effect, the radius must be increased, which also increases the DC metal resistance. Secondly, the skin effect limits the area use of the track, so that wide inductors lose their advantage. For intermediate frequencies, wide metal lines can still be more effective than narrower ones.

Spacing between adjacent tracks: the smaller the spacing, the larger the mutual inductance of the inductor and hence the larger the overall inductance.

Hollow inductor design: At high frequencies, eddy currents blow up the resistance of inner turns of the inductor, while the inductance contribution is small. They should be omitted and this results in a hollow inductor. At intermediate frequencies and high substrate resistance, filling the inductor has only a minor effect on the performance.

The loss of the substrate: For low-resistive substrates, the area of the inductor must be limited, since the penetration depth of the magnetic field is proportional to the inductor area. The area can be limited by using series connections of the metal layer. The loss caused by substrate can be further reduced by shielding the inductor from the substrate by poly-Si patterned ground shields. The inductor, using only top metal layers, can push the structure far away from the substrate and thus minimize the coupling losses.

CHAPTER III

INTEGRATED BROAD BAND CMOS T/R SWITCH

Silicon-based CMOS technology has fast become one of the most favorable processes for RF ICs due to its low cost and highly integrative capacity. Owing to low mobility, high substrate conductivity, low break-through voltage, and various parasitic parameters of CMOS processes, it is very challenging to design CMOS switches to achieve low insertion loss, high isolation, wide bandwidth, and high power handling comparable to their GaAs counterparts [34][43]. Various CMOS Transmit/ receive switches (T/R switches) have been developed at different frequencies within 900 MHz to 15 GHz [34], [35], [44]-[48]. Fully integrated CMOS T/R switches, operating over extremely wide bandwidths up to tens of GHz with high linearity and power handling, have not yet been reported. As the bandwidths of radar and communication systems are pushed wider or required to cover multi-bands to address newly emerging applications, the need of these ultra-wideband CMOS T/R switches becomes more critical.

In this chapter, a fully integrated DC-20 GHz T/R switch is presented and several new techniques are discussed to improve the switch's bandwidth, Insertion Loss (IL), Isolation (ISO), and linearity. The designed switch exhibits the best overall performance among the reported CMOS switches, e.g. the widest bandwidth, the lowest loss, and the highest isolation. Moreover, the topology is very feasible for application with fully UWB integrated transceivers as the first stage within the chip boundary connecting with the Electrostatic Discharge (ESD) structures and packages.

3.1 Integrated Transmit-Receive Switch for UWB Transceivers

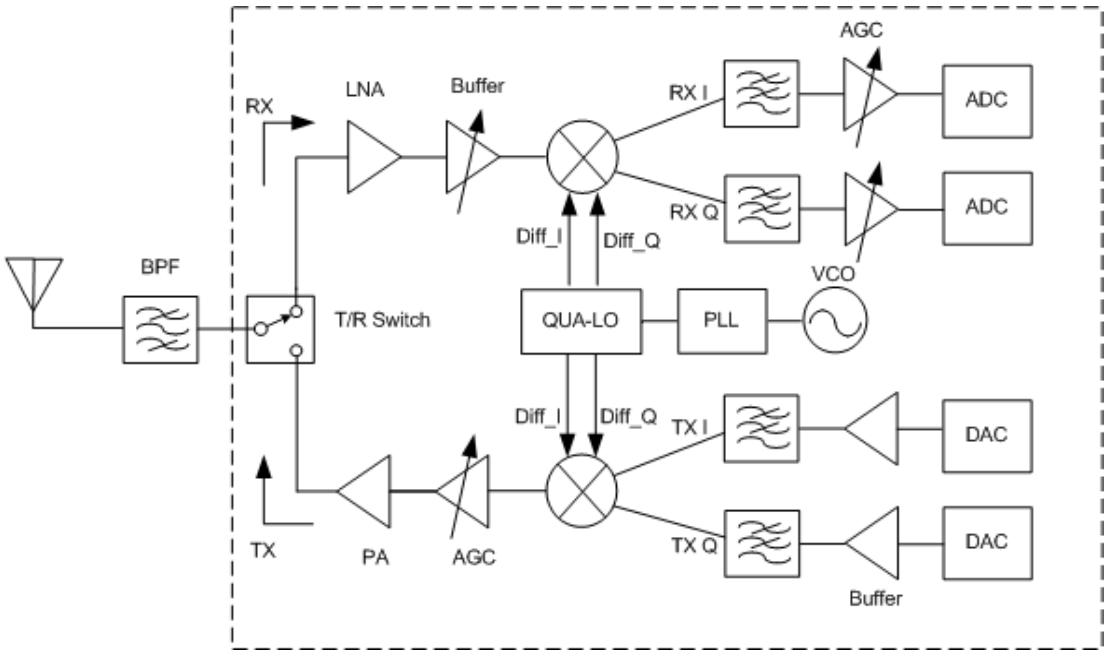


Figure 3.1 Simple direct conversion transceivers for MB-OFDM UWB. The effect of integrating the T/R switch is to push the chip-to-board boundary closer to the antenna.

A fully integrated homodyne (direct conversion) RF transceiver architecture contains very few blocks, which are routinely implemented off-chip using alternative technologies, as shown in Fig.3.1, where those in dashed blocks are built in a single die. This is different, as illustrated in with Fig. 2.2, by an integration of a high performance T/R switch. Addressed in [49], the design of every block in the dashed blocks is challenging for 3.1 GHz to 10.6 GHz wide frequency span, particularly integrated in a

single CMOS die. To present, excluding this work [50], no other broad band T/R switch is reported to meet strict MB-OFDM UWB requirements.

Any UWB transceiver implements time-division duplex and transmitter and receiver work at the same frequency, but different timing slot. The purpose of the T/R switch is to alternately couple the antenna to either the transmitter or the receiver, and to protect the receiver while transmitting high power. Shown in Fig. 3.1, the switch operates in either the transmit (TX) mode, in which power is transmitted from the power amplifier (PA) to the antenna, or the receiver (RX) mode, when power is delivered from the antenna to the LNA.

3.1.1 Performance Metrics for T/R Switch

For UWB applications, the performance of the T/R switch characterized by several parameters can be listed briefly below.

1. Insertion Loss (IL): For an ideal switch, no power is lost in the switch. Insertion loss is the power lost in the T/R switch, and is given by $P_{out}(dB) - P_{in}(dB)$ under matched conditions. UWB prefer a very low IL broad band T/R switch in order to maintain a good signal-to-noise ratio (SNR). For instance, [49] addresses that whole receiver chain should have a noise figure (NF) less than 8, and hence needs a less than 1 dB IL switch to drive a less than 3 dB NF LNA.

2. Isolation (ISO): Isolation is a measure of the signal attenuation from the signal port to the unused port, e.g., in the TX mode and is measured from the TX port to the unconnected RX port. Although isolation is usually in the negative dB range, it is common practice to use its positive value. Isolation greater than 30 dB is desirable to protect the unused port from high power and minimize loss.
3. Return Loss: This parameter is a measure of the input and output matching conditions. Similar to the isolation parameter, the return loss is usually expressed in positive value terms even though the actual value is usually in the negative dB range. Typically, T/R switch' input ports and output ports need to matched to 50 Ohm characteristic impedance so that can efficiently deliver power from antenna to LNA (Rx mode) or from PA to antenna (Tx mode). A return loss greater than 10 dB usually indicates acceptable power delivery conditions.
4. Linearity: Linearity or power handling capability is a measure of the ability of the T/R switch to operate without distorting the signal at high input power levels. The desired value of this parameter depends on the maximum input and output power of the application. The 1dB compression point, P_{1dB}, is a common measure of linearity in T/R switch.
5. Power: Static power dissipation must be kept as low as practical.

6. Integratability: As the first block within the chip boundary, T/R switch design takes into account the facilitation of the ESD structure, bonding pad parasitic capacitance, and bonding wire (with package lead) inductance impacts.

Other practical requirements of the T/R switch include robustness with respect to antenna mismatch. Also, control voltage level used to toggle the state of the switch must be available in the system. The turn-on and turn-off times typically must be less than about 10 ns to enable rapid transition between TX and RX modes.

3.1.2 Previous Works

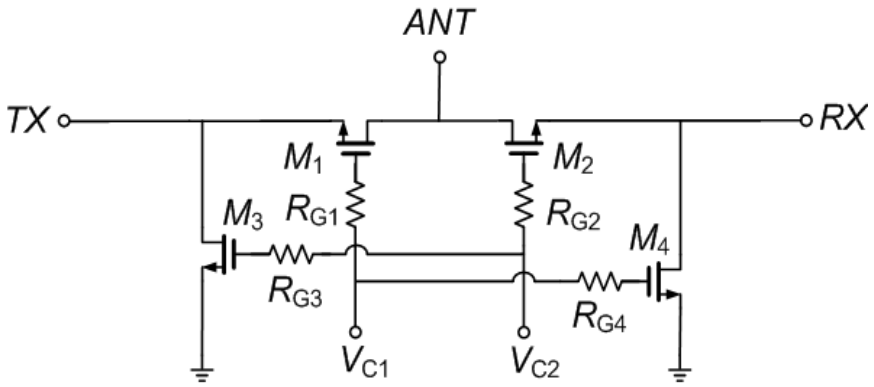


Figure 3.2 A series-shunt T/R switch topology using N type MOSFETs.

The series-shunt T/R switch with two identical arms is perhaps the most commonly used topology, as shown in Fig. 3.2. In this topology, ANT to RX path is on and TX to ANT is off when V_{C1}, V_{C2} are set 0, V_{DD}, and vice versa. The series nMOS devices, M_1 and M_2, and shunt nMOS devices, M_3 and M_4, dominate the insertion loss and isolation, respectively. In order to decrease loss in the substrate, [34] decrease the substrate resistance by placing ground connections as close to the transistors as possible. This design achieves an IL of 0.8 dB at 900 MHz, but suffers from the lower linearity, P1dB < 12 dBm. This topology typically suffers performance degradation at frequencies greater than about a gigahertz due to the substrate resistance and the parasitic source/drain junction capacitances. A 0.25-μm CMOS T/R switch operating from 0.45 MHz to 13 GHz has been developed based on synthetic transmission lines implemented by using on-chip coplanar waveguide (CPW) together with the MOSFETs' capacitances [46]. This T/R switch, however, exhibits insertion loss not as good as its GaAs counterparts due to the high loss of CPW realized on the conductive silicon substrate and the loss associated with the MOSFETs. CMOS switches normally have low power handling capability as compared to their GaAs counterparts due to low breakthrough voltages and parasitic diodes existing underneath the drain and source of the MOSFET structure [44], [45]. Floating bulk was used in [35] and [36], [48] to keep the parasitic diodes from being forward-biased under large input signals, hence improving the linearity and power handling of CMOS T/R switches. An input 1-dB power compression point, P1dB, of 21 dBm, was achieved with a series-shunt topology by resistively floating the bodies of the transistors [36], [48]. A 28-dBm P1dB was obtained

using a series MOSFET with the bulk floated by an LC tuned network for narrow-band applications [35]. The power handling was also improved using an impedance transformer network (ITN) implemented using an external [44] and on-chip [45] LC matching networks. The LC matching network, however, limits the switch's operating bandwidth due to its relatively strong frequency dependence. Moreover, the ITN causes relatively high insertion loss even though external high-Q components are used [44].

As discussed previously, the strict requirements of UWB applications challenge the conventional T/R switch topology. So far, no previously reported CMOS switch is highly qualified for UWB applications and new topology providing unprecedented performance is urgently needed.

3.2 T/R Switch Design

3.2.1 Broad Band Topology

For the typical series-shunt topology shown in Fig. 3.2, low insertion loss and high isolation can be achieved by using properly compromised large devices due to their small on-state resistances, which are scaled down approximately as L/W with L and W being the gate length and width, respectively, in advanced sub-micrometer CMOS processes. Large devices, however, have significant parasitic capacitances, causing considerable effects to circuit matching and eventually limiting the switch's bandwidth, especially in the high frequency regions. These parasitic capacitances are more

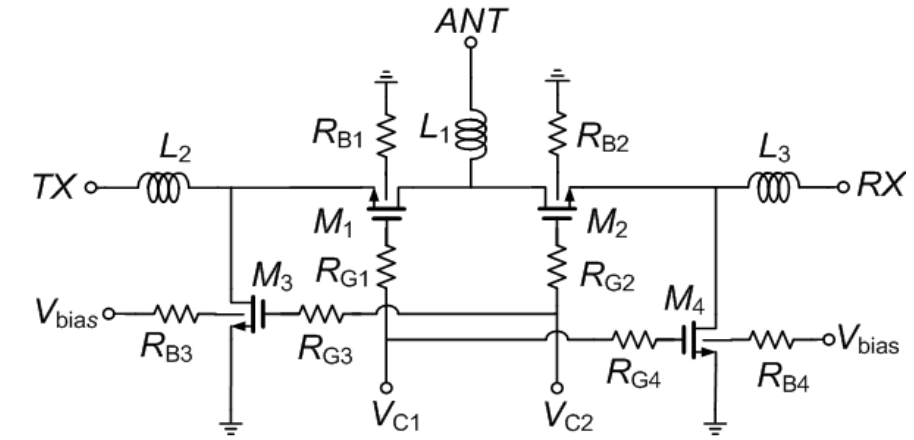
pronounced in sub-micrometer CMOS processes. In practical switching circuits, the effects of parasitic capacitances are much more severe than the on-resistances in large sub-micrometer CMOS devices, particularly at high frequencies.

IL presents the small signal power loss through the switch when it is turned on. Insertion loss is qualitatively measured by the forward transmission coefficients, $|S_{21}|^2$, when both source and load are terminated by characteristic impedance, Z_0, which is normally 50 Ohm. For a lossless switch loaded by Z_0, the power available from the source always consisted of two parts, one is the power delivered to the circuit and the other is the power reflected back because of impedance mismatching. Described by scattering parameters as

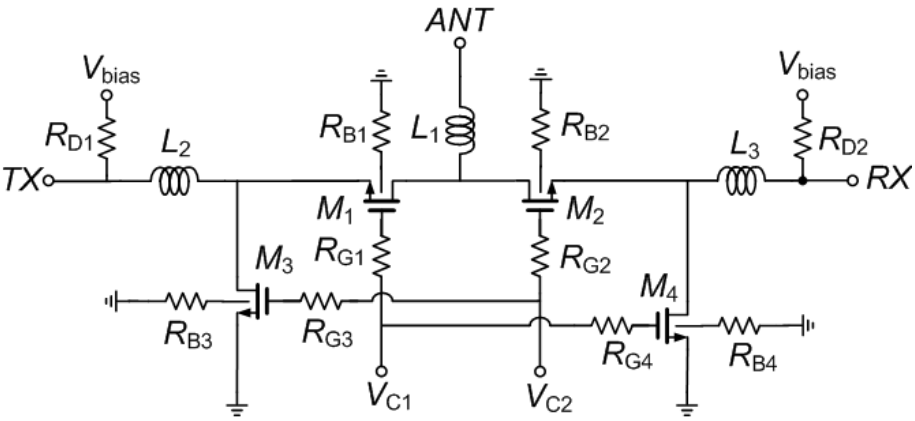
$$|S_{11}|^2 + |S_{22}|^2 = 1 \tag{3.1}$$

Where S_{11} is the reflection coefficient at source port and S_{21} is the transmission coefficient from the source to the load.

In practical switch realizations to reach tens of GHz bandwidth, the effort to reduce the IL highlights the importance of impedance matching as well as minimizing the intrinsic losses of the devices [46].



(a)



(b)

Figure 3.3 Schematics of the CMOS T/R switch implemented using synthetic transmission lines with negative bias to the bulk (a) and positive bias to the drain (b) of the shunt nMOS devices. ANT, TX, and RX stand for the (input) antenna, (output) transmitter, and (output) receiver ports, respectively.

Fig 3.3 shows the topologies of the developed CMOS T/R switch. These topologies are identical except for the different bias schemes for the shunt transistors (bulk bias in Fig. 3.3 (a) and drain bias in Fig. 3.3 (b)) used to enhance the switch's linearity and power handling -to be discussed in next section- can be implemented using the same switch. Synthetic transmission lines, realized using two series (M_1 and M_2) and two shunt (M_3 and M_4) nMOS transistors, and three series on-chip spiral inductors (L_1, L_2, and L_3), are used to achieve a very wide bandwidth. The bias resistors (R_{G1}, R_{G2}, R_{G3}, R_{G4}, R_{D1}, and R_{D2}) have large resistances in order to isolate the DC bias voltages from the RF signals. Large bulk resistors (R_{B1}, R_{B2}, R_{B3}, and R_{B4}) are used to make the transistors floating at high frequencies reduce the substrate loss and increase the switch's linearity and power handling capability. Large series and shunt nMOS transistors with gate widths in the order of several hundred μm are used to obtain small on-resistances and hence low insertion loss and high isolation for the switch, besides enhancing the linearity and power handling capability. These devices, although are much larger than those used in recently published CMOS T/R switches [44], [45], [47], and [48], still result in extremely wide bandwidth due to the use of the synthetic transmission-line technique.

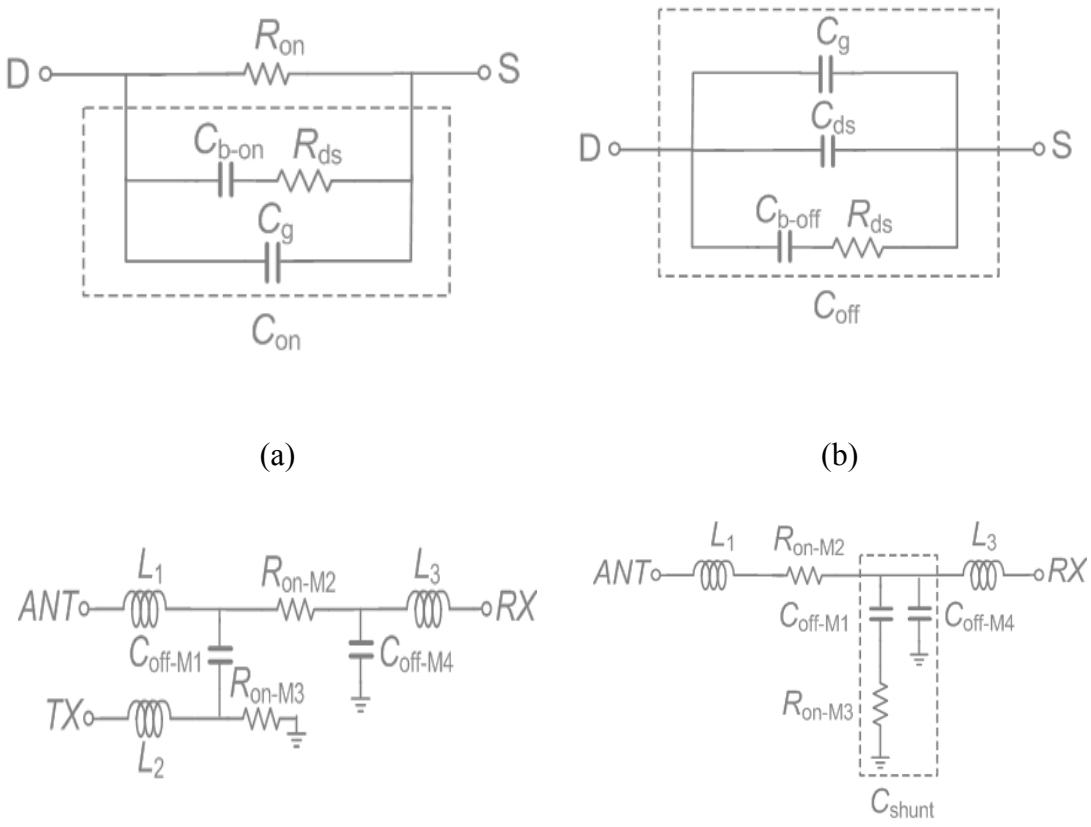


Figure 3.4 Small-signal equivalent-circuit models of the MOSFETs under on (a) and off (b) conditions, the T/R switch with ANT-RX on and ANT-TX off (c), and the ANT-RX on-path (d).

Fig. 3.4 (a) and (b) show the simplified small-signal equivalent-circuit models of the MOSFETs under on and off conditions deduced from Fig. 2.5 (a) and (b), respectively. The on-model includes the on-resistance Ron in parallel with the on-capacitance C_{on}, which represents the total capacitance C_g seen at the gate consisting of

C_{gb}, C_{gd} and C_{gs} in Fig. 2.5 (a), the on-state bulk capacitance $C_{b\text{-}on}$ consisting of C_{db}, C_{sb}, C_{rb1} and C_{rb2} in Fig. 2.5 (a), and the drain-source resistance R_{ds}. The off-model is represented by the off-capacitor C_{off}, which consists of the total capacitance C_g seen at the gate consisting of C_{gb}, C_{gd} and C_{gs} in Fig. 2.5 (b), the off-state bulk capacitance $C_{b\text{-}off}$ consisting of C_{db} and C_{sb} in Fig. 2.5 (b), the drain-source capacitance C_{ds}, and the drain-source resistance R_{ds}. Fig. 3.4 (c) shows the small-signal equivalent circuit of the T/R switch, assuming the ANT-RX and ANT-TX paths are on and off, respectively, and considering the fact that C_{on} has a relatively large impedance as compared to R_{on} below 20 GHz. As can be seen, the isolation between the ANT and TX ports is mainly determined by the on-resistance $R_{on\text{-}M3}$ of the shunt MOSFET M3. Fig. 3.4 (d) shows the small-signal equivalent circuit of the on-path between the ANT and RX ports, where C_{shunt} represents the combined off-capacitances $C_{off\text{-}M1}$ of M_1 and $C_{off\text{-}M4}$ of M_4, and $R_{on\text{-}M3}$ of M_3.

It is clearly noticed that the small signal equivalent circuit of ANT to RX path (RX mode) is actually a lossy artificial transmission line, consisting of a lossy LC segment shown in Fig. 2.6 and losses contributed by both series transistor, M_2, and shunt transistor, M_3. This indicates that the IL can be minimized by increasing the sizes of the series and shunt MOSFETs. Meanwhile, the larger parasitic capacitances' impacts can be removed by well-designed monolithic inductors.

3.2.2 Linearity and Power Handling Enhancement

Typical series-shunt CMOS switches have poor linearity and power handling, primarily due to the resultant forward-bias of the drain and source parasitic diodes of the shunt MOSFET device under operation, even with small transient voltage swings. In order to overcome the forward-bias problem, and hence increasing the switch's linearity and power handling capability, the bulk can be floated and negatively biased simultaneously as shown in Fig. 3.2 (a). Due to small on-resistance of the series MOSFETs, the source and drain are kept approximately at the same potential under the on-state. The parasitic drain and source diodes are thus always kept reverse-biased even when there are strong voltage swings at the drain and source, respectively. However, because the sources of the shunt MOSFETs are grounded, a negative voltage swing on the drain can push the two back-to-back parasitic diodes into a forward-bias region. Consequently, the voltage on the drain is clamped to a certain value in the negative region by these forward-biased diodes, leading to distortion in the output signal and, consequently, degrading the insertion loss, linearity, and power handling.

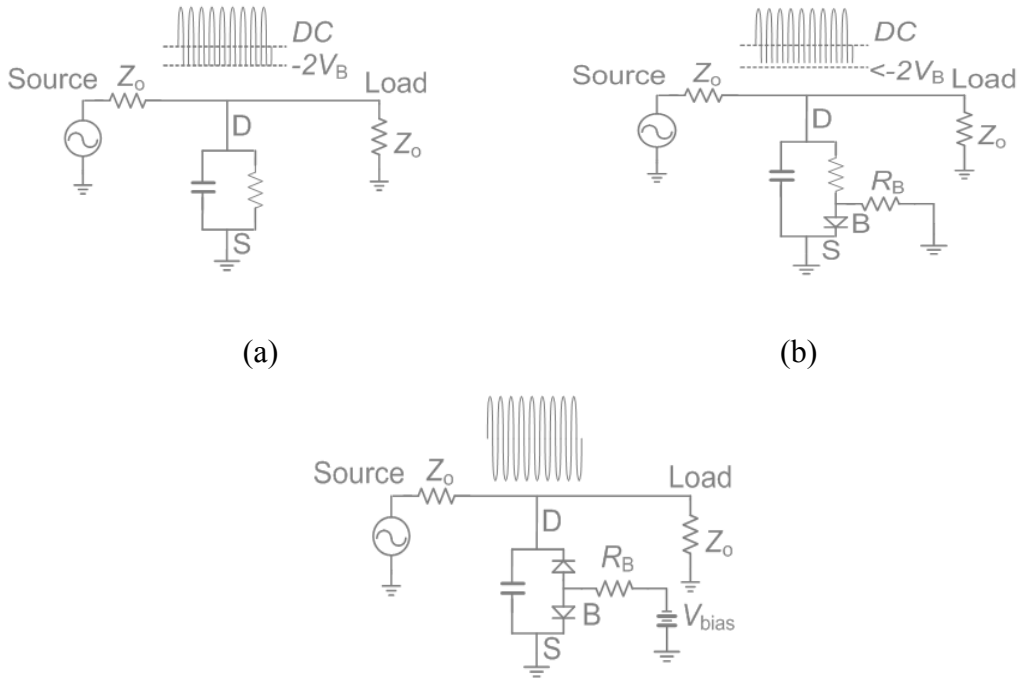


Figure 3.5 Simplified large signal models for a shunt MOSFET with bulk grounded (a), floated (b), and negatively biased (c) for different linearity and power handling conditions. The sinusoidal signal is at the drain.

Fig. 3.5 illustrates three conditions for a shunt MOSFET, which result in different linearity and power handling capabilities. In Fig. 3.5 (a), the bulk of the MOSFET is grounded directly. When the RF voltage swing at the drain is lower than $-2V_B$, where V_B is the forward pinch-on voltage of the parasitic diodes, the back-to-back parasitic diodes are all forward-biased and, consequently, the MOSFET functions as a

small forward-biased resistor in parallel with the capacitor Coff. The output voltage of the switch is then approximately clamped to $-2V_B$. Fig. 3.5 (b) shows the MOSFET with the bulk floated through a grounded resistor. A voltage swing reaching $-V_B$ at the drain would push the drain parasitic diode forward biased, but the large resistor at the bulk keeps a high impedance between the drain and ground and the source parasitic diode reverse-biased, thus improving the power handling capability. It was reported that the 1-dB compression point P_{1dB} is improved by 2 dB using this technique [48]. Fig. 3.5 (c) demonstrates a new technique to further improve the linearity and power handling. It shows the floating bulk of the shunt MOSFET is biased using a negative DC voltage via the bulk bias resistor R_B. This technique is implemented in the topology shown Fig. 3.3 (a). Since there is no current flow through R_B, the DC potential of the bulk node is kept the same as the negative bias. Therefore, the source parasitic diode is always in the reverse bias and the drain parasitic diode can withstand a strong negative voltage swing to $-(V_B + V_{Bias})$. Using the negative bulk-bias technique can, therefore, lead to larger power handling for CMOS switches than the other two methods shown in Fig. 3.3 (a) and (b). It may be noted that, due to no output current required for the negative voltage source, a negative voltage reference can be implemented in fully integrated systems without any noise and stability issues.

The linearity and power handling capability can also be improved by generating a positive DC potential between the drain and the bulk of the shunt MOSFETs. This is achieved by applying a positive bias to the drain of the shunt MOSFETs and grounding the bulk resistors, as seen in the topology shown in Fig. 3.3 (b). This positive-drain bias

technique is especially attractive when the RF signal entering the receiver or leaving the transmitter port has a positive DC offset, because no DC blocks would be needed. Using the same CMOS T/R switch, both the negative-bulk and positive-drain bias techniques give the same large signal equivalent circuits and thus have the same linearity and power handling.

3.2.3 Circuits Design

The CMOS T/R switch was designed and fabricated using the TSMC 0.18-μm CMOS triple-well process [51] with nMOS transistors and on-chip spiral inductors. On-chip inductors in silicon-based RF ICs contribute considerable insertion loss and size because of their limited quality factor (Q) and relatively large size. To achieve a very low insertion loss for the switch, the total resistance of the switch's on-path, consisting of both on-resistances of the MOSFETs and self-resistances of the on-chip inductors, needs to be designed to be as small as possible. These on-chip inductors were designed using patterned ground shields (PGS) implemented on the poly-silicon layer [42]. Fig. 3.6 shows the structure of the 0.3 nH high Q inductor and EM simulation setup in IE3D, a 2.5 dimensional full EM simulator [52]. The octagonal spiral is on the top most metallization layer, which is the thickest among the five metallization layers, resulting in smaller series resistance and smaller parasitic capacitance. Fig. 3.7 shows the 3 dimensional view of the inductor. PGS implemented on a poly-silicon layer, 7 μm underneath the spiral, gives higher Q than the use of a metal layer PGS due to its

relatively low conductivity that results in less eddy currents. The PGS underneath each spiral prevents or partly prevents the electric fields generated by the current flowing along the spiral from penetrating into the lossy silicon substrate. This not only results in significantly reduced coupling between on-chip inductors through the substrate, but also electrical loss due to the substrate, particularly at high frequencies [53]. On-chip spiral inductors with PGS can, therefore, have high Q and be located close to each other while keeping sufficient isolation between them, effectively resulting in very low insertion loss and small die area for the switch.

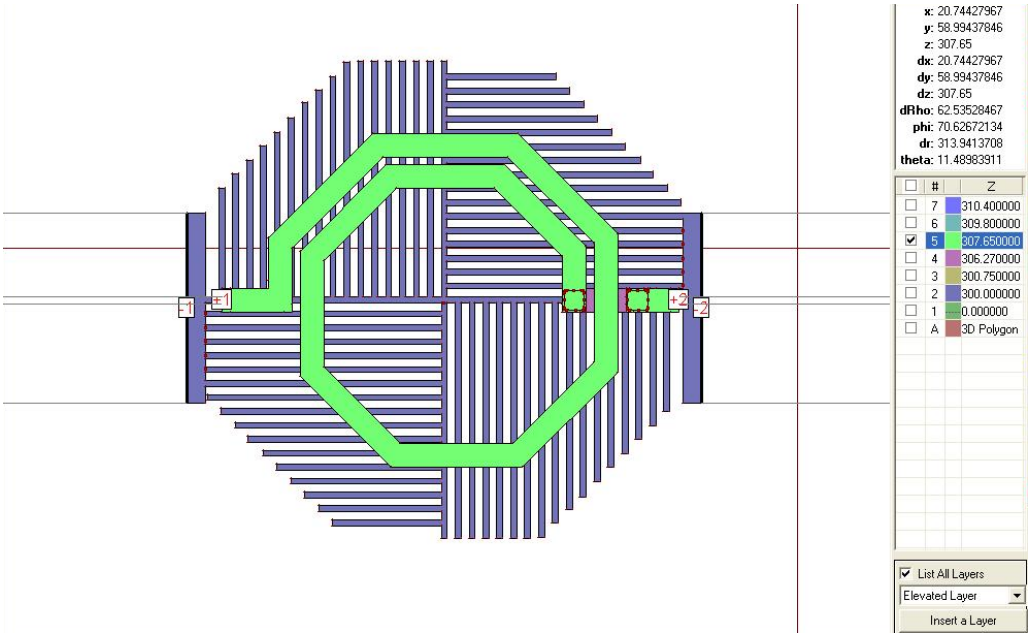


Fig. 3.6 Two-port S-parameter simulation of an inductor with PGS in IE3D. Differential 50 Ohm ports are applied on the spiral and shield, respectively. In the right column, the "#" sub-column shows the numbers of the multiple dielectric layers and "Z" sub-column describes the coordinates of each dielectric layers in z direction.

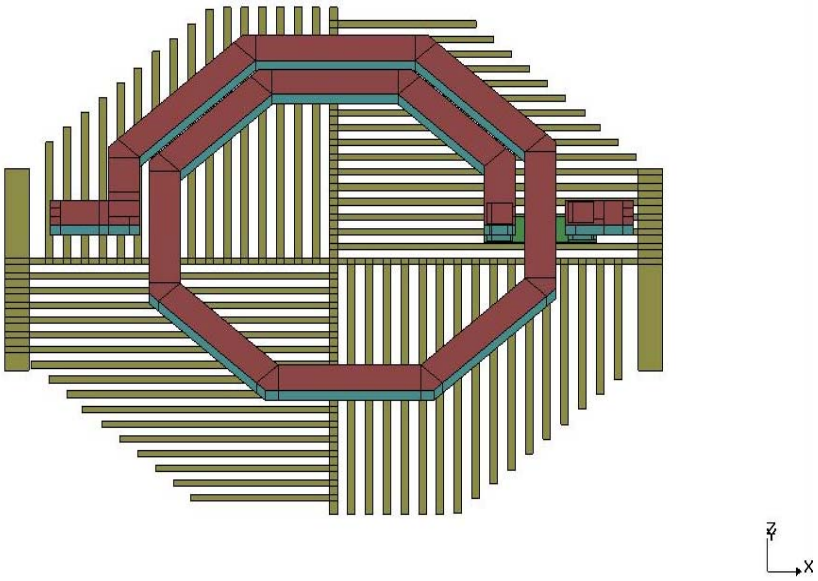


Fig. 3.7 3-dimensional layout of the high Q inductor. The spiral was on the top thickest metal layer and PGS is on the poly-silicon layer.

Fig. 3.8 compares the Q of the designed 1.5-turn spirals with and without PGS calculated using the EM simulator IE3D. The Q was determined using $Q = \mathrm{Im}(Z_{in}) / \mathrm{Re}(Z_{in})$, where Z_{in} is the input impedance of the lumped-element π-equivalent-circuit model of the spiral, in Fig. 2.7 (b), with one port grounded. As can be seen, the Q of the PGS inductor is improved up to about 37 GHz with a maximum

around 20 GHz. By fitting the calculated S-parameters with the one-order equivalent model, shown in Fig. 2.7 (b), the PGS spiral has approximately 0.85-Ω series resistance below 5 GHz and about 1.67 Ω at 20 GHz.

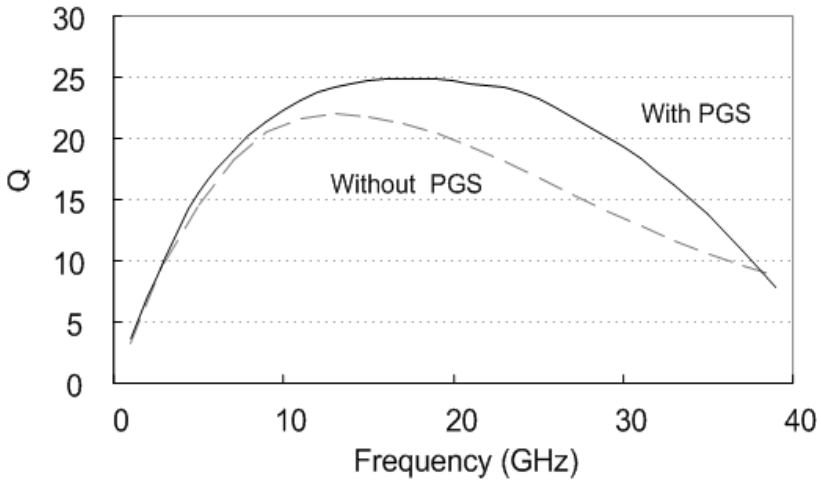


Fig. 3.8 Calculated Q of on-chip spiral inductors with and without PGS.

Several remarks need to be made at this point concerning the CMOS T/R switch design. As implied in Eq. (2.2), small transistors should be employed to achieve a wide bandwidth for the switch. On the other hand, large series and shunt devices are needed to produce low insertion loss and high isolation, respectively. A trade-off is thus needed not only in the switch topology, but also in the device size, in order to achieve simultaneously an ultra-wide bandwidth along with low insertion loss and high isolation.

Particularly for the selected T/R switch topology, the inductance and Q of the on-chip spirals versus frequency should be optimized together with C_{shunt}, as well as the combined off-capacitances of the series and shunt devices. The spiral inductance and Cshunt dictate the bandwidth while the Q affects the insertion loss.

Table 3.1 lists the parameters of the designed CMOS T/R switch. All the bias resistors are realized on the poly-silicon layer to achieve small layouts. The on-resistance R_{on} is about 4 and 11 Ω for the employed series and shunt nMOS, respectively. The combined off-capacitance of the series and shunt nMOSs is about 280 fF.

Fig. 3.9 shows the micrograph of the CMOS T/R switch, including on-wafer RF and DC probe pads with the TX port terminated by an on-chip 50-Ω resistor. The actual area of the switch is measured only 230 × 250 μm2, with the inductors occupying approximately 60% of the chip area.

3.3 T/R Switch Performance

Measurements were conducted on-wafer using a probe station, vector network analyzer, and frequency synthesizers. Calibration was performed using a full two-port calibration process and the calibration standards built on the same chip. These calibration circuits have the same RF pads as those in the switch in order to allow accurate de-embedding of the pads. The control and bias voltages were applied through DC probes directly.

TABLE 3.1
SUMMARY OF THE CMOS T/R SWITCH'S DESIGNED PARAMETERS

Circuit Element		Element Value
M_1, M_2		304-μm gate width
M_3, M_4		184-μm gate width
L_1, L_2, L_3		0.35 nH, 1.5 turns
R_{G1}, R_{G2}, R_{G3}, R_{G4}		10 KΩ
R_{B1}, R_{B2}, R_{B3}, R_{B4}		10 KΩ
With Bulk Bias	V_{bias}	-1.8 V
	V_{C1}	1.8 V (on), -1.8 V (off)
	V_{C2}	-1.8V (on), 1.8 V (off)
With Drain Bias	V_{bias}	1.8 V
	V_{C1}	3.6 V (on), 0 V (off)
	V_{C2}	0 V (on), 3.6 V (off)
Without Bulk/Drain Biases	V_{bias}	0 V
	V_{C1}	1.8 V (on), 0 V (off)
	V_{C2}	0 V (on), 1.8 V (off)

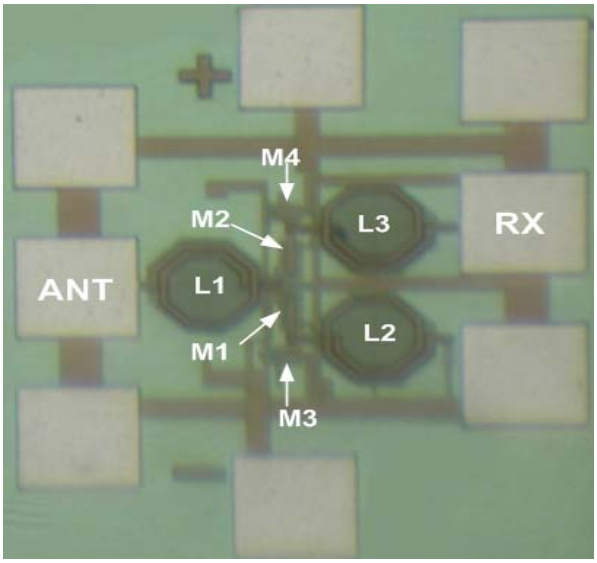
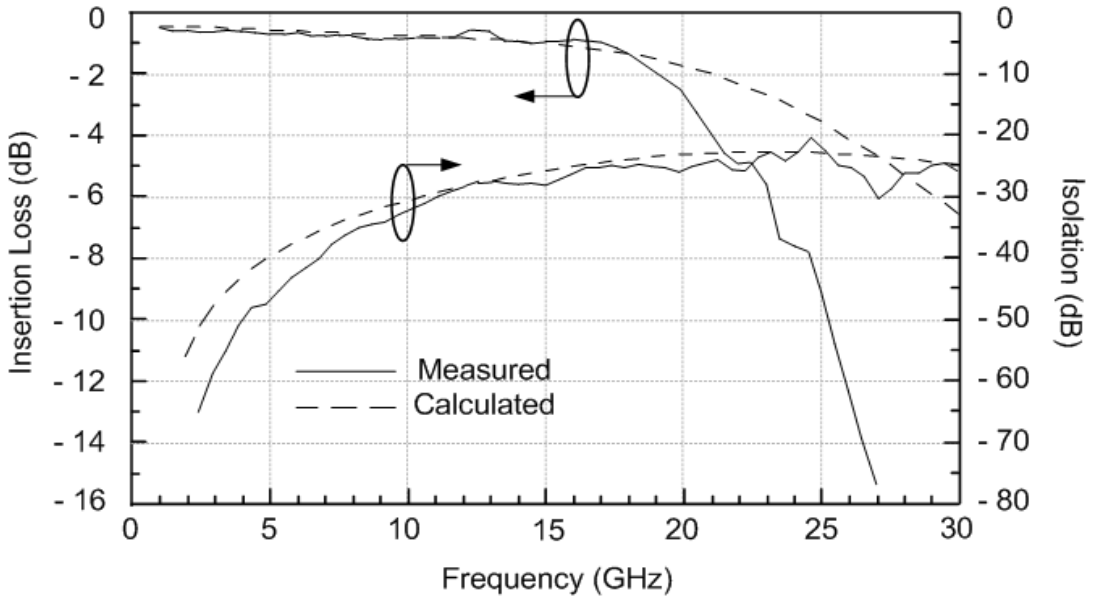


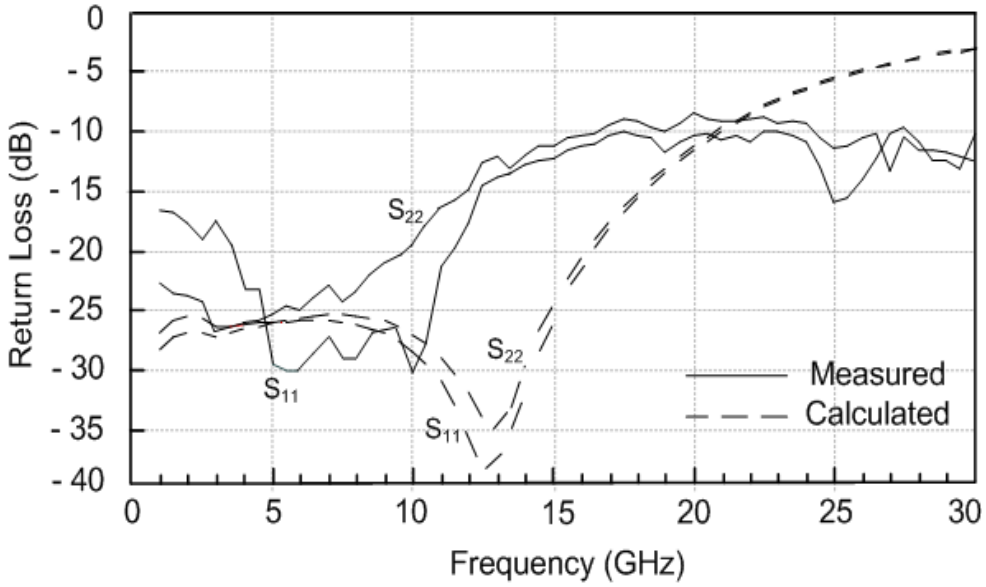
Figure 3.9 Microphotograph of the CMOS T/R switch. The die area without pads is 0.06 mm^2.

3.3.1 Small Signal Measurements

S-parameter measurements to obtain small-signal IL, ISO and return loss were carried out using a Vector Network Analyzer. The output power of the Vector Network Analyzer was –10 dBm. Full two-port calibration, using on-wafer short, open, load, and thru calibration standards, was performed to correct for the effects of the probes, cables, contact resistances, and pads capacitance so that the switch alone performance was concisely characterized. Port 1 and port 2 refer to ANT port and RX port, respectively, as shown in Fig. 3.9, and a 50-Ohm on chip resistor terminated TX port. Due to the symmetric structure, the arm from ANT port to TX port exhibits the same characterizatiocharacterization. Fig. 3.10 shows the measured and calculated insertion loss, isolation, and return loss of the developed CMOS T/R switch. It exhibits insertion losses of less than 0.7, 1, and 2.5 dB from DC to 10 GHz, 10 to 18 GHz, and 18 to 20 GHz, respectively. The measured isolation varies from 32-60 dB, 25-32 dB, and 25-27 dB between DC-10 GHz, 10-18 GHz, and 18-20 GHz, respectively. The measured return losses at the antenna and receiver/transmitter ports are better than 15 and 10 dB from DC to 10 GHz, 10 to 18 GHz, and 18 to 20 GHz, respectively. The measured isolation varies from 32-60 dB, 25-32 dB, and 25-27 dB between DC-10 GHz, 10-18 GHz, and 18-20 GHz, respectively. The measured return losses at the antenna and receiver/transmitter



(a)



(b)

Figure 3.10 Measured and calculated insertion loss and isolation (a) and return loss at the antenna (S_{11}) and TX/RX (S_{22}) ports (b).

ports are better than 15 and 10 dB from DC to 10 GHz and 10 to 18 GHz, respectively. These results are the same for the three different bias conditions listed in Table 3.1.

As can be seen in Fig. 3.10 (a), the measured and calculated insertion losses agree very well to approximately 18 GHz, beyond which the measured insertion loss significantly drops below the simulated result. This discrepancy above 18 GHz has been observed in several chips and is mainly caused by the inaccuracy of the transistors' available model. We believe that this inaccuracy is due to the parameters of the model, which characterize the silicon substrate loss. The employed transistor model also leads to the discrepancy between the measured and simulated isolation and return loss seen in Fig. 3.10.

3.3.2 Linearity and Power Handling Measurements

Linearity of the switch is characterized by either the third-order intercept point (IP3) or 1-dB compression point (P_{1dB}). For UWB applications, it is very necessary to study both of them to investigate in-band inter-modulation as well as off-band blocker immunity. IP3 was measured by a two-tone test recording the signals of the fundamental output and the third order modulation output, while P_{1dB} was measured by a one-tone test, but the input power was enhanced up to 2 Watts by a power amplifier. The cable loss calibration, the contact resistance elimination and the pad capacitance subtraction were carried out during the measurement procedures for IP3 and P1dB. Fig. 3.11

records the measured IP3 at 5.8 GHz with –1.8 V bulk bias voltage. Fig. 3.12 shows the measured input IP3 (IIP3) variation versus bulk bias voltage at 5.8 GHz. As can be seen, the IIP3 can reach as much as 41 dBm by increasing the negative bias voltage. Fig. 3.13 compares the simulated P1dB and measured P1dB, both at 5.8 GHz and with –1.8 V bulk bias. There is a 3 dB discrepancy when the input power was around 1 Watt. The foundry verified that the large signal model lacked accuracy. Fig. 3.14 compares the P_{1dB} measurement without bulk bias (bulk bias resistor is grounded) and with bulk bias at –1.8 V. The P_{1dB} with the bulk biased is more than 25 and 20 dB from 1 to 11.5 GHz and 11.5 to 19 GHz, respectively, reaching 26.2 dBm at around 4 GHz. It is seen that by applying a negative bias to the bulk, the power handling capability of the switch is increased by approximately 4 dB.

Similar performance for the IIP3 and P_{1dB} were also obtained when the drain was biased with a positive voltage as discussed in Section 3.1.2.

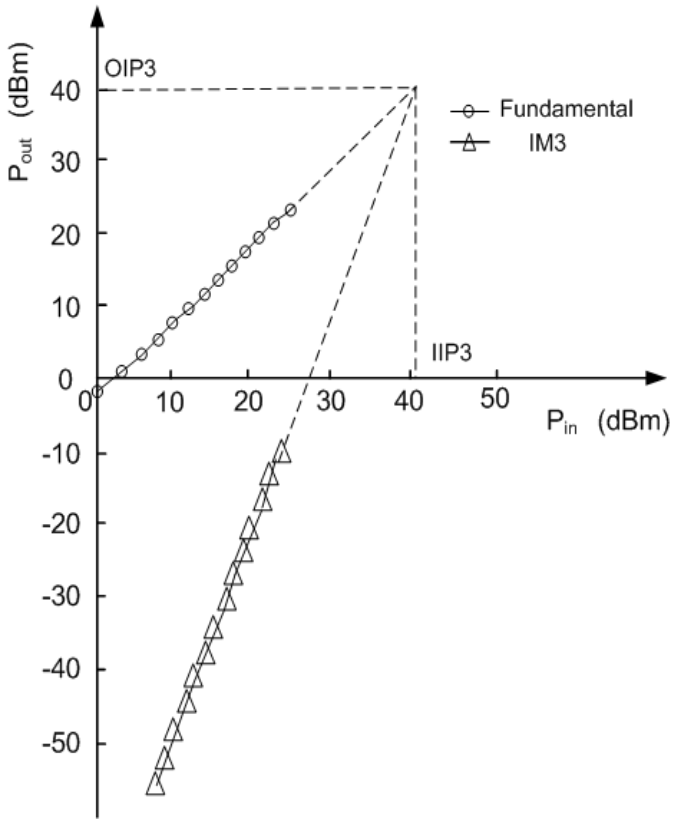


Figure 3.11 IP3 measurements at 5.8 GHz by two-tone testing. The two tone frequencies are 5.8 GHz and 5.85GHz respectively and input powers are identical, the bulk bias voltage is applied using -1.8 V.

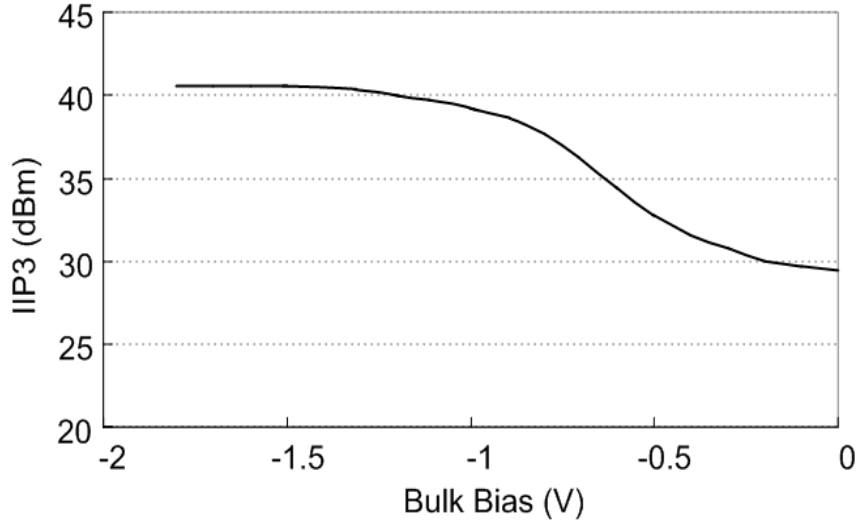


Figure 3.12 Measured IIP3 at 5.8 GHz versus bulk bias voltage.

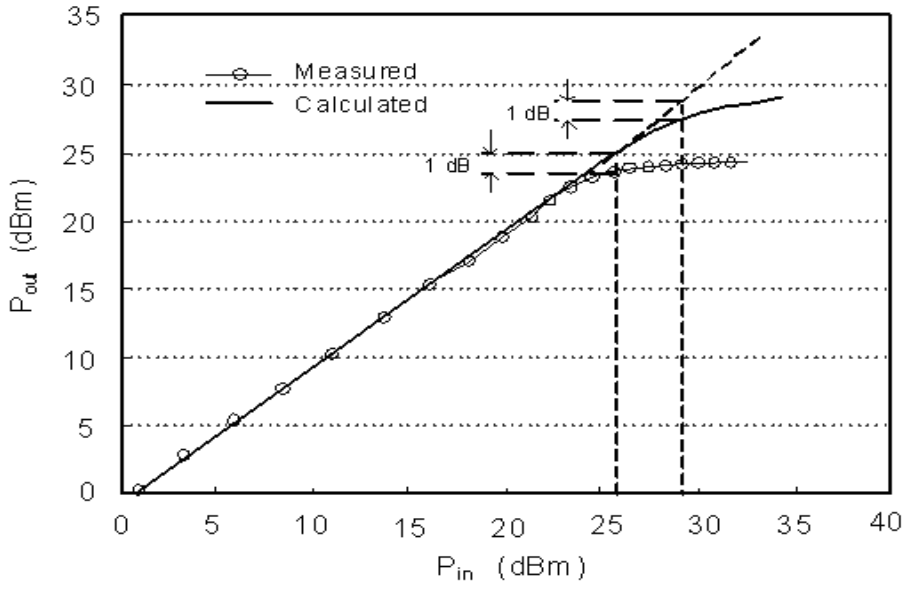


Figure 3.13 P1dB testing at 5.8 GHz, the bulk bias voltage is -1.8 V.

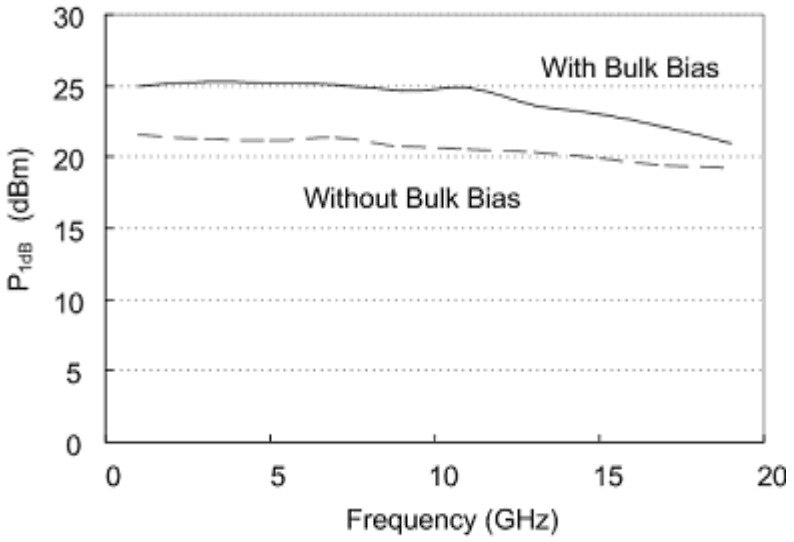


Figure 3.14 Measured P_{1dB} with 0- and -1.8-V bulk bias voltage.

3.3.3 Overall Performance Evaluation

Table 3.2 compares the performance of the developed CMOS T/R switch with those recently published. The new switch demonstrates the widest bandwidth, highest frequency, lowest insertion loss, highest isolation, and strongest power handling among the integrated series-shunt CMOS switches [34], [36], [45], [47], and [48]. It also shows wider bandwidth, higher frequency, lower insertion loss, and higher isolation as compared to the series CMOS switch [44]. Moreover, the measured IIP3 is highest among those reported [34], [36], [45], [47], and [48]. The developed switch is also the

first fully integrated CMOS T/R switch providing very low insertion loss (below 0.7 dB) for UWB communication systems covering 3.1-10.6 GHz.

It is to be noted, the T/R switch using proposed broadband topology is very feasible for serving as the first block on chip because the chip to the board boundary comprises of a bonding wire, a package leak and a bonding pad with ESD structure. Using modern package (Micro Lead Frame package), the bonding wire from the chip to the package and the package pin normally bring around 0.3 nH inductance and the pads with underneath ESD circuits functions as a shunt small capacitance (around 50 fF). Hence, it is practical to replace the L_1 in Fig. 3.4 (d) by the bonding-wire and package (pin) inductor and optimize the size of the transistors so that the pad capacitance can be combined into C_{shunt}. Moreover, T/R switches using the proposed topology can have lower loss and higher bandwidth by more advanced CMOS processes (lower $R_{on} \times C_{off}$), e.g. 0.13 μm or 90 nm.

3.4 Summary

The developed CMOS T/R switch represents the first CMOS switch, implementing on-chip spiral inductors with patterned ground shields to simulate transmission lines for ultra-broadband performance with miniaturization and simultaneously floating the bulk with negative bulk or positive drain bias, to achieve high linearity and power handling capability. These broadband and high-linearity/power-handling techniques can also be utilized for other kinds of CMOS switches. Particularly,

the developed CMOS T/R switch, with a die area of less than 0.06 mm^2, less than 0.7-dB insertion loss, and more than 20-dB return loss and 30-dB isolation from 3.1 to 10.6 GHz, also provides the best T/R switch to date for the emerging ultra-wideband (UWB) wireless communication systems operating over that frequency range. The developed CMOS T/R switch with its full integration feature paves the way for full-integration into a complete CMOS system-on-chip.

TABLE 3.2
SUMMARY OF CMOS T/R SWITCHES

	Technology	Topology	Frequency (GHz)	Loss (– dB)	Isolation (– dB)	$P_{1\text{-}dB}$ (dBm)	IIP3 (dBm)	Actual Chip Size (mm^2)
[34]	0.5-µm CMOS	Narrow band, Off-chip CAP	0-1.0	0.73	41.8	17.2	39.2	0.1
[44]	0.18-µm CMOS	Narrow band, Off-chip ITN	0.9, 2.4	0.97, 1.1	35.4, 20.6	26.3	38.7, 30.9	0.28
[35]	0.18-µm CMOS	Narrow band, LC-tuned substrate biased, fully integrated	2.4, 5.2	TX 1.52	TX 30	28	NA	0.56
				RX 1.42	RX 15	11.5	NA	
[36],[48]	0.18-µm CMOS	Broad band, fully integrated	0-6	1.1	27	20	NA	0.03
[45]	0.13-µm CMOS	Broad band, fully integrated	0-10	1.1	25	15	NA	0.2
[45]	0.13-µm CMOS	Narrow band, integrated ITN, fully integrated	15	1.8	17.8	21.5	34.5	0.25
[47]	0.18-µm CMOS	Broad band, fully integrated	0-6	0.8, 1.0	28, 30	17	33	0.2
This Work	0.18-µm CMOS	Extremely broad band, fully integrated	0-10	0.5-0.7	32-60	25.4-26.2	37-41	0.06
			10-18	0.7-1.0	25-32	22.6-25.4	34-37	
			18-20	1.0-2.5	25	19.8-22.6	31.5-34	

CHAPTER IV

INTEGRATED SINGLE-POLE SINGLE-THROW SWITCH AND TIME-GATED CARRIER-BASED UWB TRANSMITTER

In this chapter, a new transmitter for power efficient Time-Gated Carrier-based UWB is proposed to provide an emerging wireless technique for communications, precise localization, and Radio Frequency Identification (RFID) and radar applications. A fully integrated high performance CMOS single-pole single-throw switch (SPST) is demonstrated as a time-domain multiplier to generate UWB signals from 3.1 GHz to 10.6 GHz with very low power consumption. Section 4.1 presents a new fully integrated CMOS UWB transmitter and Section 4.2 discusses the design of the SPST switch, in detail. The measurements of the SPST switch are analyzed in section 4.3. Section 4.4 demonstrates the power efficiency to generate UWB signals compliant with FCC regulations.

4.1 Carrier-based UWB

4.1.1 Carrier-based UWB Transmitter

Carrier-based UWB signals have been widely used in various radar and communication applications [54], [55]. Compared with carrier-free impulse/mono-pulse signals, carrier-based UWB signals hold the advantage of more convenient spectrum

management and less distortion through antennas [56]. Moreover, the use of carrier-based signals facilitates the design of all components including antennas in the system because of the signals' much narrower bandwidth. Essentially, a carrier-based UWB signal is generated by multiplying an impulse signal with a single-tone carrier signal. Therefore, the bandwidth and central frequency of the generated signal can be manipulated by adjusting the pulse width of the impulse signal and the frequency of the single tone.

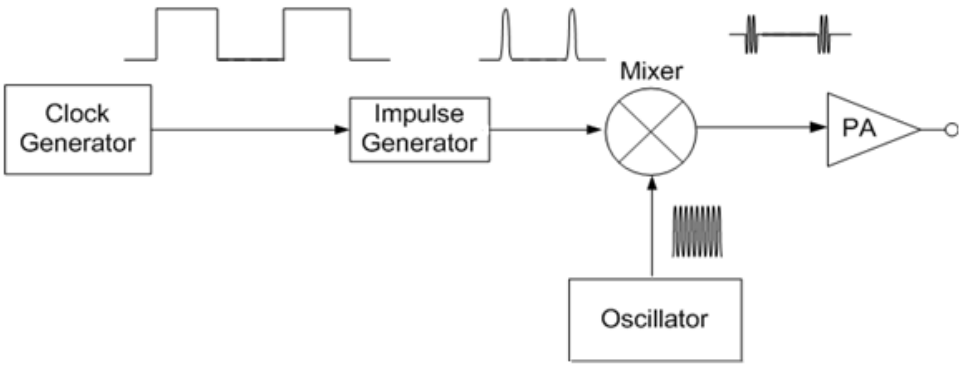


Figure 4.1 Block diagram of a typical carrier-based UWB transmitter

Fig. 4.1 shows a typical carrier-based UWB transmitter. The clock generator is usually composed of timing-control digital circuits and sends out a clock signal that can include modulation information. The impulse generator produces an impulse signal whose pulse width is inversely proportional to the bandwidth of the required signal. The

mixer performs a multiplication between the impulse and a single-tone signal generated by the oscillator. The up-converted signal is then sent to the wideb and power amplifier (PA) to achieve required amplitude. In this approach, the oscillator is required to generate multiple tones if the transmitter needs to operate over multiple frequency bands. This carrier-based UWB technique suffers from two major disadvantages. First, the PA design in the last stage is a challenging issue. This PA needs to supply enough gain and has reasonable power efficiency and good output matching over a wide frequency range. Second, in UWB radar applications, low pulse repetition frequency (PRF) is often utilized. Since the transmitted signal duration is usually very short, the resultant peak-to-average power ratio is extremely high. This means no signal needs to be transmitted during most of the time. However, because the PA and other circuits of the transmitter are 'on' all the time, a large amount of power is wasted, rendering the approach power-inefficient. Various carrier-based UWB transmitters using CMOS and BiCMOS SiGe processes have been developed [57]-[59], but it is still very necessary to investigate power-efficient solutions for various sensor applications.

To this end, we have proposed a new architecture for carrier-based UWB transmitters that is not only power-efficient but also reduces power consumption, enhances switching speed and isolation, and reduces circuit complexity. In addition, we also demonstrate the workability and performance of a new transmitter, covering the entire 3.1-10.6 GHz UWB band, using a CMOS chip, consisting of an impulse generator integrated with a SPST switch, and an external synthesizer. The demonstration shows a very small input signal is needed to drive SPST to meet the FCC UWB regulations, and

hence makes it very feasible to integrate the entire transmitter into a single die in CMOS. Moreover, the broadband SPST switch provides a very good match to the antenna port and thus remove the difficulty of designing the broadband PA.

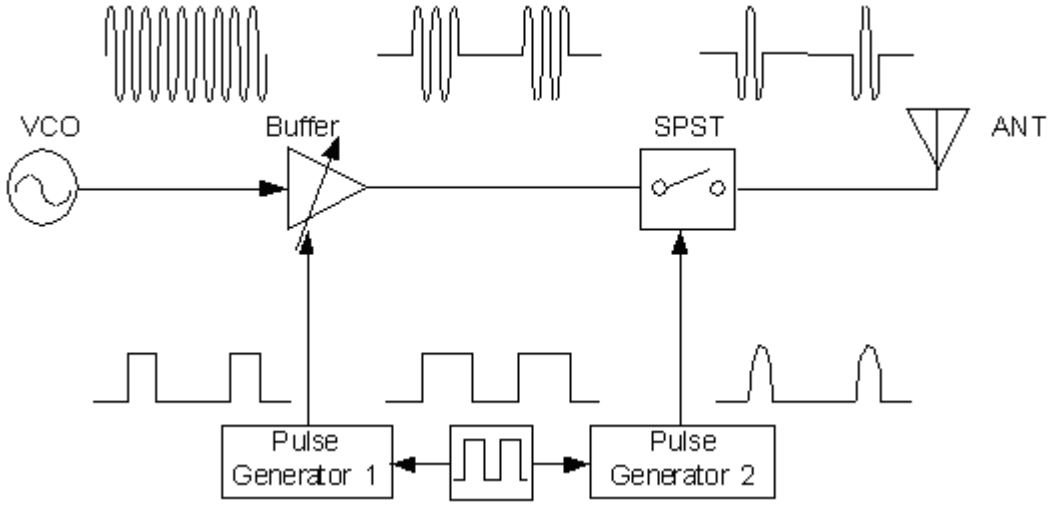


Figure 4.2. The proposed carrier-based UWB transmitter topology.

Fig. 4.2 shows the block diagram of the newly proposed carrier-based UWB transmitter, consisting of a voltage-control oscillator (VCO), a tunable gain buffer, a SPST switch, and two pulse generators, In this model, power switching is used to perform the signal multiplication, instead of mixing as used in the more typical UWB transmitter structure shown in Fig. 4.1 and those in [57]-[59]. The transmitter's principle is based upon the concept of generating a carrier-based UWB signal by gating a single-

tone signal with a small time window, thereby only producing signal during a small time period. A double-stage switching procedure, using two pulse generators of wide and narrow pulses, and two switches, is adopted in the proposed transmitter to remedy the switching speed limitation of the buffer, inherent in CMOS circuits, to achieve sub-nanosecond gating required in UWB signal generation. The VCO generates carrier signals that define the center frequencies of UWB signal to feed the buffer in order to realize sufficient transmitted power and proper output impedance matching. The buffer is gated through its internal switch (first-stage switching) using a wide pulse produced by the pulse generator 1, which should be wide enough to allow the buffer to start and reach stabilization. The second-stage switching, performed by the SPST switch and pulse generator 2 generating narrower pulses, is then used to reduce the pulse width of the generated signal, making it an UWB signal which has spectrum bandwidth of at least 500 MHz as defined by FCC [1]. Pulse generators 1 and 2 are synchronized using a common clock generator as shown in Fig. 4.3.

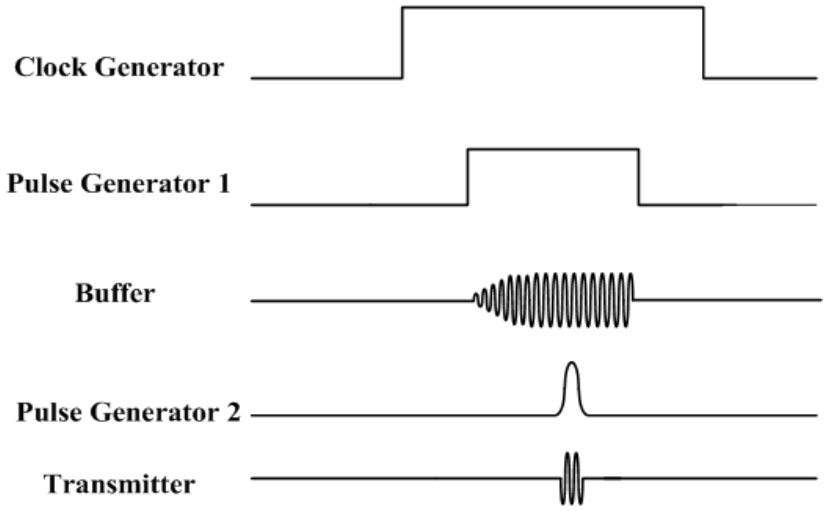


Figure 4.3. Waveforms for the building blocks in the proposed UWB transmitter.

To cover the entire 3.1 to 10.6 GHz UWB bandwidth, a switch-able LC tank VCO is the best choice in terms of low phase noise, low time jittering, and 7.5 GHz wide tuning range. The tunable gain buffer drive a broadband SPST switch, providing a high input impedance interface to VCO at the same time, bring no loss to the VCO tank circuitry in order to have good phase noise performance. The bias circuits enable the buffer to alternatively work into amplifier-mode and stand-by mode triggered by pulse generator 1. The fast SPST switch is triggered by pulse generator 2. Both the input

impedance and output impedance of the switch need to be matched to 50 Ohm for the maxim power delivery to transmitter antenna.

4.1.2 Broad Band Single Generation

The fundamental concept used to generate a Time-gated Carrier-based UWB signal is quite simple and can be described as in Fig. 4.4. The product of combining a single frequency sinusoid wave with a Gaussians impulse is a multiple-cycle pulse in time domain. Characterized by a linear time-invariant (LTI) system, the output frequency spectrum of the multiple-cycle pulse is uniquely determined by the convolution integral of the frequency responses of the sinusoid wave and the impulse, producing an upconversion of the impulse's spectrum (rectangular function) to the frequency of the sinusoid due to the Delta impulse response of the sinusoid in frequency domain. Moreover, the output signal's bandwidth is tunable by controlling the width of the Gaussian impulse in time domain.

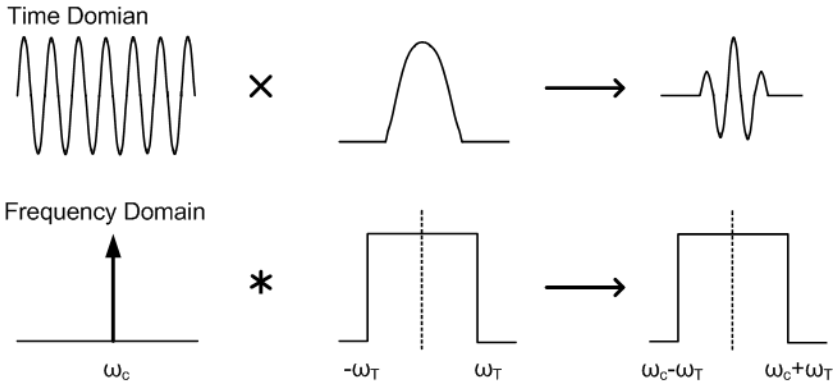


Figure 4.4 Time-gated Carrier-based UWB single generation.

For circuitry realization, one stage time-gated multiplexing (switching) provides a challenge for meeting the FCC spectrum regulation caused by the LO power leakage. Fig. 4.5 shows the effects of power leakage and demonstrates the need for two switching stages. In Fig. 4.5(a), only the second-stage switching is used. T_s stands for the pulse width of the UWB signal, while T_i is the interval between two consecutive pulses. During the time the second-stage switching is off, the LO signal (i.e., the VCO's signal) still manages to arrive at the transmit antenna due to limited SPST switch isolation. Although this LO leakage has much smaller amplitude than the transmitted UWB signal, it can still accumulate sufficiently large power over the duration T_i to over-drive the UWB signal on the transmitted spectrum. When this happens, a high-power single tone would be observed at the carrier frequency above the UWB signal spectrum. To avoid

this problem, the signal-to-leakage ratio should be much higher than T_i/T_s. For instance, for a 1-ns UWB signal pulse to be transmitted at 10-KHz PRF with negligible power leakage, the ratio *Ti/Ts* is roughly about 10^5 and an isolation of much more than 50 dB is thus required to satisfy the leakage requirement if only one switching stage was used (i.e., the second stage). This level of isolation is very difficult to achieve in CMOS switches. In Fig. 4.5(b), both switching stages were applied. The LO leakage only appears during the time the buffer is on; i.e., within the time widow T_L, which is usually no longer than 10 ns. The isolation of the second-stage switching is only required to be larger than T_L/T_s. In this case, 30-dB isolation is sufficient to ensure small LO leakage regardless of the PRF used. For CMOS switching, 30-dB isolation is a modest requirement and can be achieved by careful design.

As the timing alignment of pulse generator 1 and pulse generator 2 shown in Fig. 4.3, the tunable buffer always works at the stand-by mode. The SPST switch is triggered to work in the switching transition. The input impedance variations of the switch during the transition thus would cause pushing and pulling issues to the VCO because of the high reverse isolation provide by the buffer.

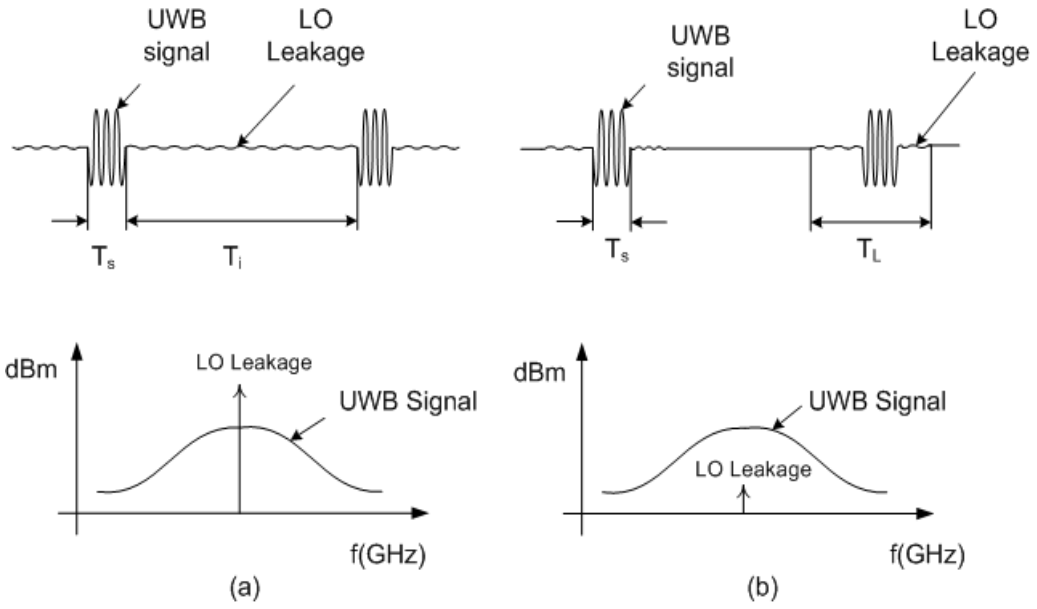


Figure 4.5 Effects of power leakage using: (a) Single- and (b) double-stage switching.

4.2 SPST Switch Design

A low IL, high ISO, broadband SPST switch is the key block of the Time-gated Carrier-based UWB transmitter. It functions to multiply the input sinusoid with the gated impulse in time domain. To meet the FCC frequency mask [1], the switch should exhibit a very flat low IL during on state spanning from 3.1 GHz to 10.6 GHz, while reject the LO leakage by a very high isolation during off state. In time domain the switching

between the two static sates should be very fast and bring symmetric falling and rising edges of transient waveform shown Fig. 4.5.

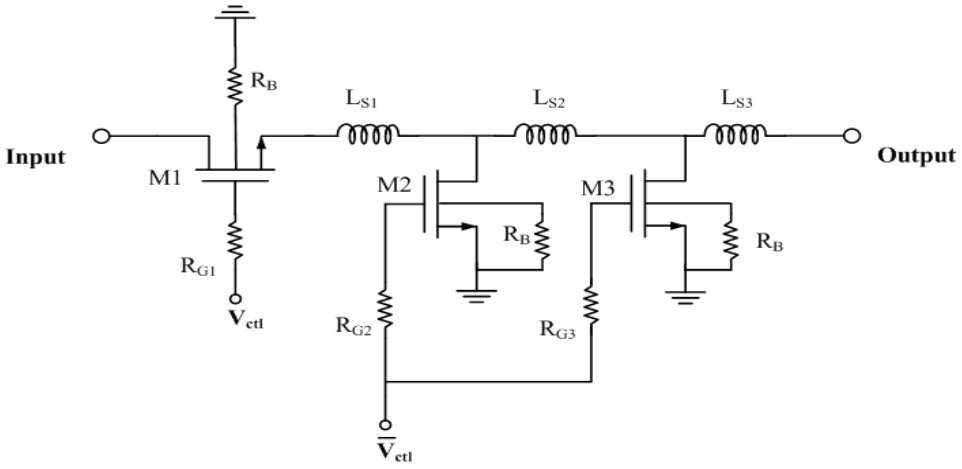


Figure 4.6 Schematic of the broadband SPST switch.

CMOS switch is the best choice of low power consumption to meet above requirements since the MOSFET devices operating deep triode region functions like a passive device, as discussed in Chapter II. Fig. 4.6 shows the schematic of the CMOS SPST switch. One series and two shunt nMOSs are used to provide compromise between insertion loss and isolation. Biasing resistors are used in lieu of RF chokes to minimize the chip area. In order to achieve an ultra-wide bandwidth, on-chip inductors between adjacent transistors are combined with the transistors' capacitances to form a synthetic transmission line between the input and output of the SPST switch. The bulk terminals of the transistors are floated by grounded on chip resistors to improve the power-

handling ability and insertion loss [48]. The SPST's on and off states are obtained when the control signals control signals V_{ctrl}, $\overline{V_{ctrl}}$ are set to V_{dd}, zero and zero, V_{dd}, respectively. To ensure wideband performance, the sizes of the series and shunt transistors need to be carefully determined. The series transistor particularly plays an important role in the switch's insertion loss, while the shunt transistors enhance the isolation when the switch is off. Shunt devices, however, inadvertently aggravate the insertion loss due to their parasitic drain to ground capacitance. For the series-connected transistor, as the gatewidth is increased, the on resistance reduces, resulting in low insertion loss in the low-frequency region. The gate–source capacitance, however, increases, thus degrading the insertion loss at high frequencies. The design strategy will be discussed in detail in the following sections.

4.2.1 On-state

When the V_{ctrl}, $\overline{V_{ctrl}}$ are set to V_{dd}, zero respectively, the SPST switch works at on state. The input signal goes through. A flatten and low IL at on state is achieved from 3.1 GHz to 10.6 GHz since the switch is designed according to a synthetic transmission line concept, discussed in Chapter II. When both gate and bulk of each nMOS are floated by large resistors, a simplified lumped-element equivalent network can be derived as shown by Fig. 4.7.

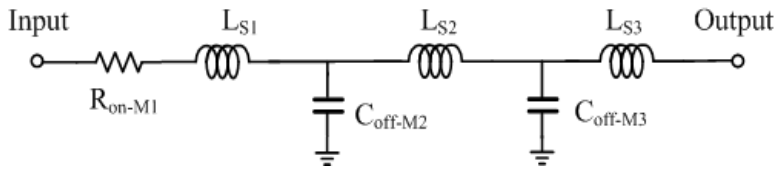


Figure 4.7 Equivalent network of the SPST switch working at on state.

Shown in previous Chapter II by Fig. 2.4 (a), the equivalent lump element network of transistor M_1, working in deep triode region, includes an on resistance from drain to source and a parallel lossy on-capacitance, which is combined by all the gate-related capacitances and bulk related capacitances. The impedance of the on-capacitance is much larger than the on-resistance under 20 GHz so it is removed from the equivalent network. Off-capacitances, C_{off_M2} and C_{off_M2}, represent the off-states of transistor M_2 and M_3 respectively. The C_{off} of each transistor is a lossy capacitor as described in Fig. 2.4 (b), which combines the total capacitance C_g seen at the gate, including C_{gb}, C_{gd} and C_{gs}, and the off-state bulk capacitance $C_{b\text{-}off}$, consisting of C_{db} and C_{sb}, the drain-source capacitance C_{ds}, and the drain-source resistance R_{ds}.

By selecting M_2 and M_3 of the same sizes and, therefore, having the same off-capacitances, and choosing the three series inductors in Fig. 4.6 as $L_{S1} = L_{S3}$ and $L_{S2} = 2L_{S1}$, the equivalent lump elements network of the SPST switch is clearly a series network consisting of an on-resistance, R_{on_M1}, and a synthetic transmission line built by

cascading two L-C-L segments shown in Fig. 2.5. Given a 50 Ohm Characteristic Impedance, an extremely broadband low IL can be achieved by properly sizing M_2 and M_3 and optimizing the inductor's values accordingly. Eq. (2.1) indicates that the inductors' values need to be selected based on C_{off_M1} in order to achieve 50-Ohm Characteristic Impedance. Eq. (2.4) shows that the bandwidth is merely in reversely proportional to C_{off_M1} (or C_{off_M2}).

As will be explained in the following section, the shunt transistors with larger gate width help high isolation at high frequencies when the SPST switch works at off state. It is clearly shown that there is a very straightforward trade-off between bandwidth and isolation. In addition, it is obvious that a larger size of the series transistor, M_1, always helps to achieve a low insertion loss when the gate of the transistor is biased through large resistor. But the size of the M_1 needs to be optimized to compromise IL and switching speed of the switch. This optimization process will be investigated in the section 4.2.3.

4.2.2 Off-state

When the V_{ctrl}, $\overline{V_{ctrl}}$ are set to zero, V_{dd} respectively, the SPST switch works at off state. The input oscillation signal is isolated from the output port. Fig. 4.8 shows the simplified lump elements equivalent network at this condition. The off-capacitance of transistor M_1 helps block the input at low frequencies, but the feed through of the signal aggravates proportionally with the increase of the frequency. High isolation at high

frequencies is realized by multiple reflections of the input power by two stages of impedances mismatch caused by the on resistances of M_2 and M_3.

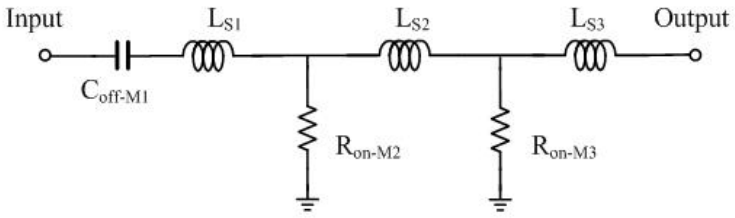


Figure 4.8 Equivalent network of the SPST switch working at off state.

Fig. 4.9 presents the mechanisms of the power reflection using the transmission line theory. When a transmission line of characteristic impedance Z_0 feeding a line of different characteristic impedance, Z_1, only some part of the input power will be transmitted to the second line and the other part will be reflected back.

The amplitude of the reflected voltage wave normalized to amplitude of the incident voltage wave is defined as the voltage refection coefficient, Γ, and Γ is given by [60] as following equations:

$$\Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{4.1}$$

The transmission coefficient, T, is the amplitude of the transmitted voltage wave normalized to amplitude of the incident voltage. Eq. (4.1) and (4.2) are valid when the transmission lines are both lossless. They describe the fact that an entire power transmission happens when two transmission lines have identical characteristic impedances and there is no reflection back at the interface. The Γ and T under this perfect impedance matching condition are 0 and 1 respectively. On the other hand, different characteristic impedances generate power reflection at the interface and hence lower the transmitted power to the second line accordingly.

$$T = 1 + \Gamma = \frac{2Z_1}{Z_1 + Z_0} \tag{4.2}$$

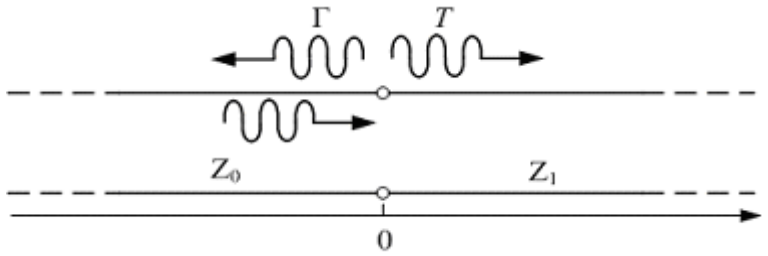


Figure 4.9 Reflection and transmission at the junction of two transmission lines with different characteristic impedances.

Eq. (4.1) and (4.2) are also valid for lossless lump element networks at any frequencies. Ignoring the series off-capacitance of MOSFET M_1, the equivalent network in Fig. 4.8 can be seen as cascading two identical "T" shape lump networks, shown in Fig. 4.10.

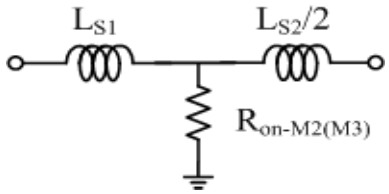


Figure 4.10 T shape lump elements network consisting of two series inductors and a shunt MOSFET transistor.

The T shape network in Fig. 4.10 can be seen as a special case of a normal loss transmission line built by series L, R and shunt C, G lump elements, in which $L = L_{S1}$, $R = 0$, $C = 0$, and $G = 1/ R_{on\_M2\ (/M3)}$, then the characteristic impedance of the T shape network is given by [60]

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{j\omega L_{S1} R_{on\_M2(M3)}} \qquad (4.3)$$

Eq. (4.3) shows that the characteristic impedance of the equivalent network in Fig. 4.9 is a complex number, hence never be conjugately matched with 50 Ohm. The reflections always happen at the junction of input port and the first T shape network and the junction of the second T shape network and the output load. The transmission coefficients of both junctions are identical, given by

$$T = \frac{2Z_1}{Z_1 + Z_0} = \frac{2\sqrt{j\omega L_{S1} R_{on\text{-}M2(M3)}}}{\sqrt{j\omega L_{S1} R_{on\_M2(M3)}} + 50} \qquad (4.4)$$

Due to the fact there is no reflection at the junction of the two identical T shape networks, the isolation of the SPST switch provided by the three inductors and two shunt transistors, excluding M_1, can be derived as

$$ISO = -20\log(2T) = -20\log\left(\frac{4\sqrt{j\omega L_{S1} R_{on\text{-}M2(M3)}}}{\sqrt{j\omega L_{S1} R_{on\_M2(M3)}} + 50}\right) \qquad (4.5)$$

It is interesting to notice that adding more T shape networks in Fig. 4.10 will not bring higher isolation because of the fact that no reflection happens at any junction of two identical T shape networks, assuming there is many identical networks. When the frequency is at middle range and where the impedance of the L_{S1} is much smaller than $R_{on\_M2\ (M3)}$, the inductors' effect can be ignored and thus function as short connections.

Under these conditions, cascading more T shape networks in Fig. 4.10 actually approaches paralleling more shunt on-resistances, and thus brings a much smaller combined shunt resistance. Based on Eq. (4.2), smaller shunt resistance, Z_1, brings smaller transmission coefficient, and thus makes the SPST switch higher isolation within this frequency range.

4.2.3 Fast Switching

Typical SPST transistor switch structures are only suitable for slow switching because the transistor's gate uses a large biasing resistor to make the gate floating at RF so that the switch performance is not affected. This gate-biasing resistor, however, leads to a large RC constant, effectively slowing down the control signal applied to the control terminal connecting to the gate via the resistor. Fig. 4.11 demonstrates the effect of the gate-biasing resistor, assuming an ideal step-signal is applied to the control terminal. Due to the gate resistor R_g and gate-to-ground parasitic capacitance C_p, the rising edge of the resultant gate voltage V_g is slowed down. This is actually a RC charging effect and the falling edge is slowed down as well since the gate voltage is discharging with the same time constant. For a given size of MOSFET, a larger gate resistor gives a slower rising edge, leading to slower switching speed. From Fig. 4.11, it is apparent that in order to maintain the fidelity of the control sub-nanosecond pulse signals, the gate resistance should be less than a few hundred ohms. Although this may aggravate the insertion loss and return loss of the switch, the switch is expected to have reasonably

good performance by optimizing its other components, while maintaining the rising/falling edge of the control pulse signal.

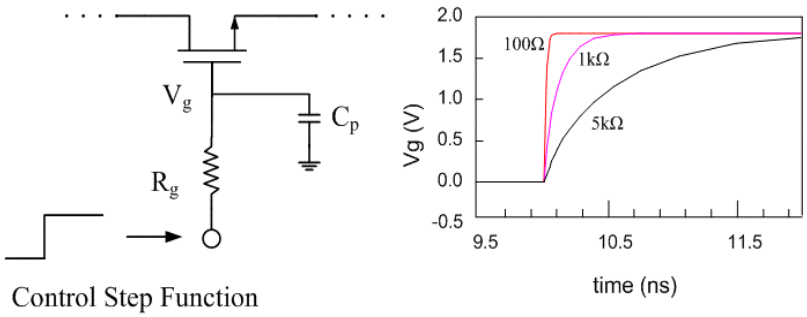


Figure 4.11 Schematic of the broadband SPST switch. Cp presents the entire Gate parasitic capacitance regarding to ground.

The gate-to-ground capacitance is estimated as 0.5 pF, whereas the calculated gate–source (C_{gs}) and gate–drain (C_{gd}) capacitances are each between 0.2–0.3 pF. Numerically, C_p is thus approximately equal to C_{gs} and C_{gd} in parallel, which is actually expected from the MOSFET's equivalent circuit. Using the estimated value of C_p and the input control signal, the optimal value for the gate resistor, that produces the required 300-ps rising/falling time for the SPST's output pulse, can thus be determined as 100.

The fast broadband SPST switch was designed and fabricated using the TSMC 0.18-µm CMOS process [51]. Table 4.1 summarizes the designed circuit elements.

TABLE 4.1
SUMMARY OF THE DESIGNED SPST'S COMPONENTS

Circuit Element	Element Value
M1	320-μm gate width
M2, M3	360-μm gate width
L_{S1}	0.3 nH
L_{S2}	0.6 nH
L_{S3}	0.3 nH
R_{G1}	100 Ω
R_{G2}	100 Ω
R_{G3}	100 Ω
R_B	20 KΩ
V_{ctrl} , $\overline{V_{ctrl}}$	1.8 V, 0 V (on) 0 V, 1.8 V (off)

Fig. 4.12 shows the microphotograph of the SPST switch with the measurement RF pads. Transistors M_1, M_2 and M_3 are implemented by multiple finger structures. Integrated inductors L_{S1}, L_{S2}, and L_{S3}, on the topmost thickest metallization, have no pattern ground shield (PGS) underneath each spiral, but the physical parameters of each inductor including the diameters and spiral widths, were optimized for high Q. Thus the

losses caused by the inductors are much smaller than the on-resistance of M_1 from 3.1 to 10.6 GHz. The gate bias resistors and bulk bias resistors are all implemented with poly-silicon resistors for the smallest layout areas.

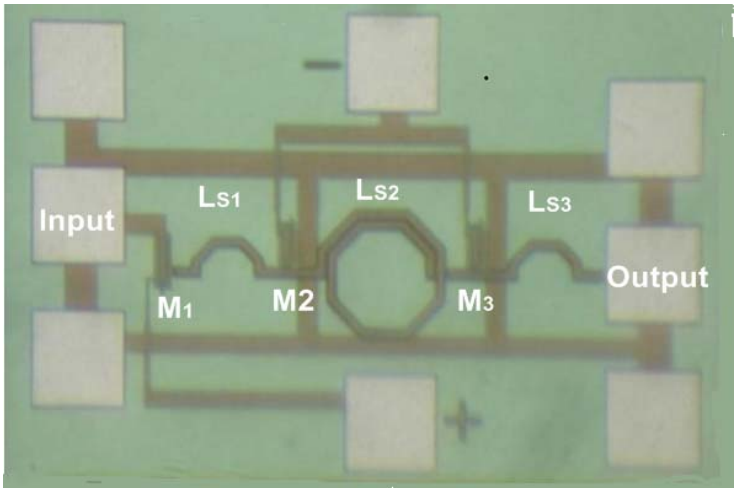


Figure 4.12 Microphotograph of the CMOS SPST switch. The die area without pads is 0.08 mm^2.

4.3 SPST Switch Performance

4.3.1 Measurements

S-parameters of the SPST switch has been measured on-wafer using a probe station and a vector network analyzer. Full two-port calibration, using on wafer short, open, load and thru standards, was performed to correct for the effects of the probes and cables. Since the on-wafer calibration standards were built with the same pads as those implemented by the switch, the elimination of pad capacitance and contact resistance were carried out at both input and output ports. The vector network analyzer's output power was 10 dBm. V_{ctrl}, $\overline{V_{ctrl}}$ ports were connected to DC power supply through very short cables, which brought negligible inductance impacts.

The SPST switch exhibits measured insertion loss less than 1.5 dB, return loss greater than 18 dB, shown in Fig. 4. 13, across the entire UWB band of 3.1–10.6 GHz. A 0.5 dB variation of IL from DC to 10 GHz is achieved and the roll off of the S_{21} beyond 10.5 GHz is caused by the gate leakage of the transistors, where the gate is terminated with a resistor of only 100 ohms, and substrate loss. The very high return loss at input and output ports helps to reduce the reflections at input and output ports from DC to 15 GHz, hence increasing the delivery of the incident power.

Isolation of the SPST switch at off state was measured by the same on-wafer setup process. The SPST switch exhibits isolation greater than 50 dB from DC to 9 GHz, and greater than 40 dB from 9 GHz to 11 GHz, as given by Fig. 4.14. This extremely

high isolation is given by the blocking of M_1 and reflections at input port and output port, studied in the previous section 4.2.2. It is shown from Fig. 4.13 that both measured S11 and S22 are very close to 0 dB, suggesting that most of the incident wave power is reflected back by the two impedance mismatched ports.

The strong incident wave refection and the input impedance mismatching does not bring a pushing and pulling problem to the VCO, shown in Fig. 3.13, since the tunable buffer has already worked into standby mode during the SPST switching transitions. The buffer at standard up mode provides high reverse isolation to VCO and keeps a constant loading to VCO even during the two stage switching transitions, and thus guarantees a stable oscillation.

4.3.2 Linearity Measurement

Linearity of the switch, P_{1dB}, is measured by one-tone test, using a signal generator along with an external power amplifier as explained in the previous chapter on T/R switch measurements. Also, the cable losses, probe contact resistance, and pad parasitic capacitance effects were carefully calibrated out. The output power was measured by a spectrum analyzer.

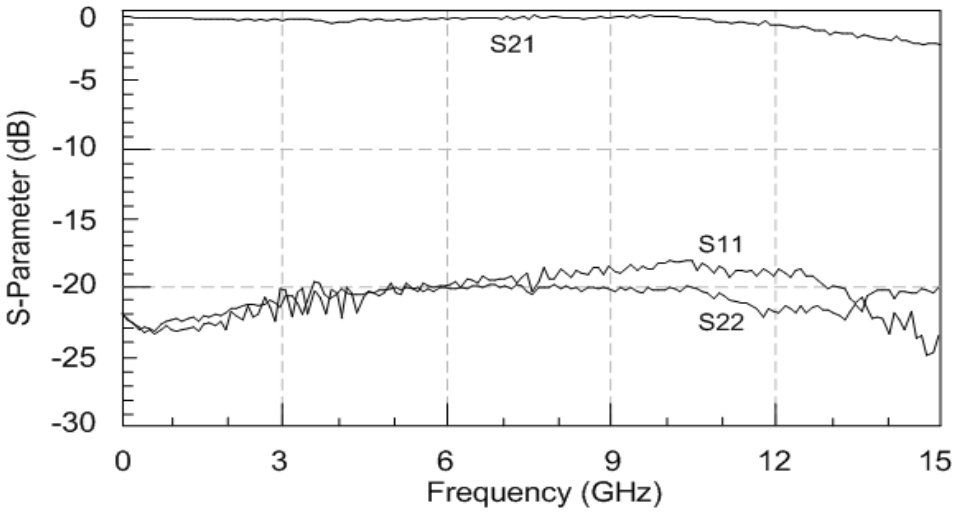


Figure 4.13 Measured S-parameters when the SPST switch is on.

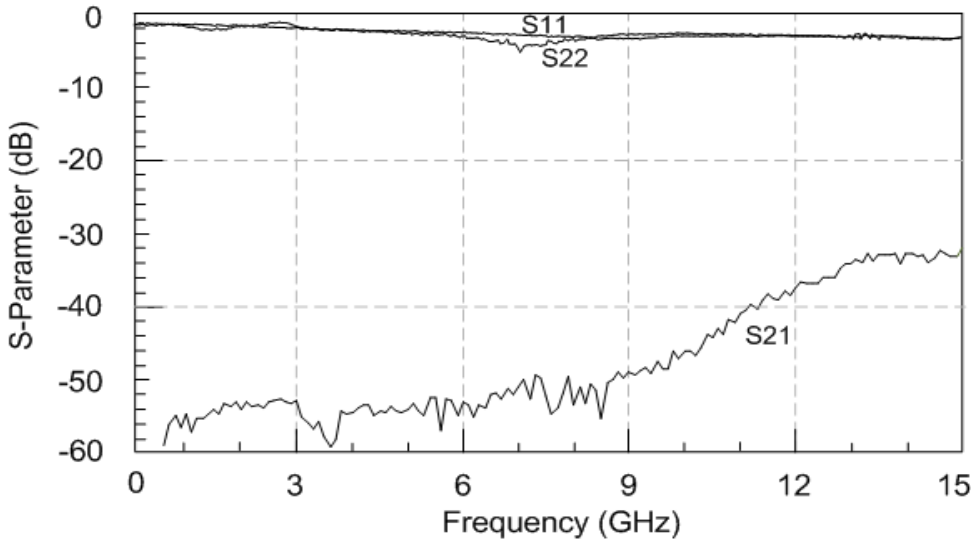


Figure 4.14 Measured S-parameters when the SPST switch is off.

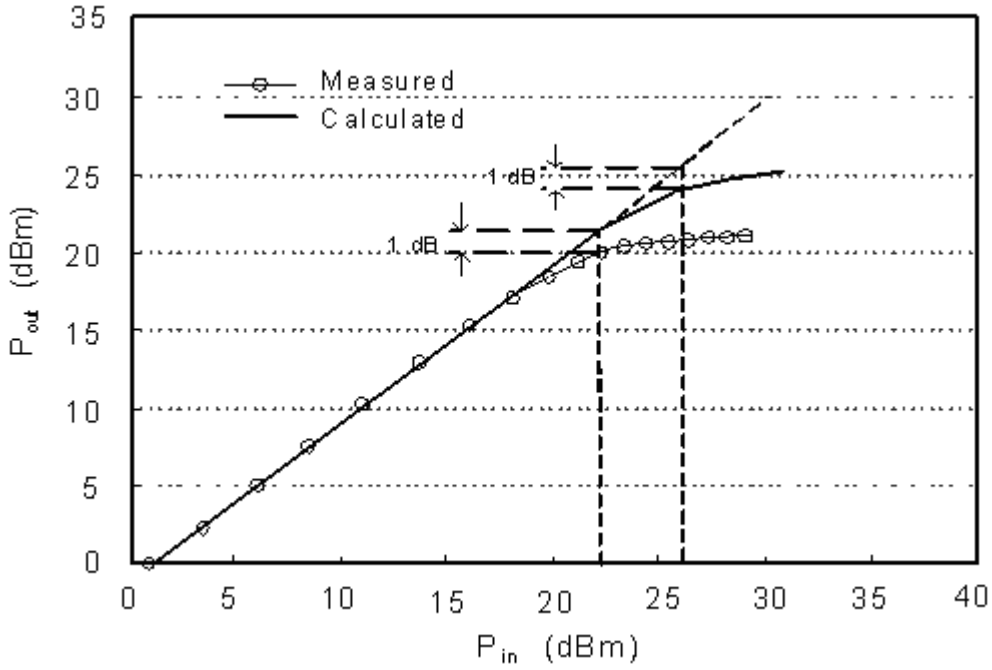


Figure 4.15 Simulated P1dB and measured P1dB of the SPST switch at on state at 5.8 GHz.

Fig. 4.15 compares the measured P1dB and simulated P1dB at 5.8 GHz. The discrepancy is found to be -4.5 dB. The simulated P1dB by ADS at this frequency is 26.5 dBm while the measured value is 22 dBm. The reason for the discrepancy is the inaccuracy of the large signal model of the triple well nMOS, especially when the bulk of the transistors are disconnected with their sources, i.e., the floating technique is applied by large bulk resistors. Moreover, the measured 22 dBm P_{1dB} without any bulk bias, 4 dB lower than the T/R switch with negative bulk bias, confirms the fact that the

major source of the non-linearity is the forward-biased drain diode of the shunt nMOS devices and not any other source.

Nevertheless, the SPST switch exhibits a strong power handling capability to be integrated by the proposed Time-gated Carrier-based UWB transmitter. With a measured P_{1dB} 60 dB higher than the FCC's EIRP emission density, -41.24 dBm/MHz, the switch can generate any instantaneous bandwidth of UWB signals without any distortion. For instance, a UWB signal having 7.5 GHz bandwidth of the FCC mask will transmit a maximum power as

$$\text{EIRP} = -41.3\,\text{dBm} + 10\log(7500)\,\text{dB} = -2.55\,\text{dBm}$$

With a power handling capability over 24 dB higher than the UWB maximum emissions, the integrated switch prove its feasibility to serve as the linear multiplexing block in time domain proposed in Fig. 4.2.

4.4 UWB Signal Generations

UWB transmitter. The CMOS chip's microphotograph is shown in Fig. 4.16. The die area of the whole circuit is 850 μm by 700 μm including input and output on-wafer pads. The measurement was conducted on-wafer. The frequency synthesizer supplied the LO signal feeding the input port of the pulse generator–SPST switch chip. The output transient signal was measured by a microwave digitized oscilloscope through a 50-Ohm cable and the instantaneous spectrum corresponding to a single pulse was converted from the saved transient data by Fourier Transform. It is noted that although the parasitic capacitance and the contact resistance of the probing pads could not be removed during the test, the impedance mismatching did not reduce the amplitude of the signal significantly, which indicates a fact that the reflections caused by the pads is negligible compared to the transmission signal.

A 15-MHz clock was used to drive the on-chip pulse generator. The whole circuit consumes less than 1-mA dc current.

Fig. 4.17 displays the time-domain waveform and the spectrum of a measured UWB signal. The UWB signal has a 3-dB pulsewidth of 4 ns and a 10-dB bandwidth of 500 MHz at 5-GHz center frequency, which conforms to the FCC's minimum UWB bandwidth requirement. The UWB signal amplitude is 2 V (peak-to-peak) and its amplitude at 5 GHz is 20 dBm. The 2-V peak-to-peak voltage is the maximum voltage level corresponding to the SPST when turned on completely. The sidelobe level is below 15 dBc.

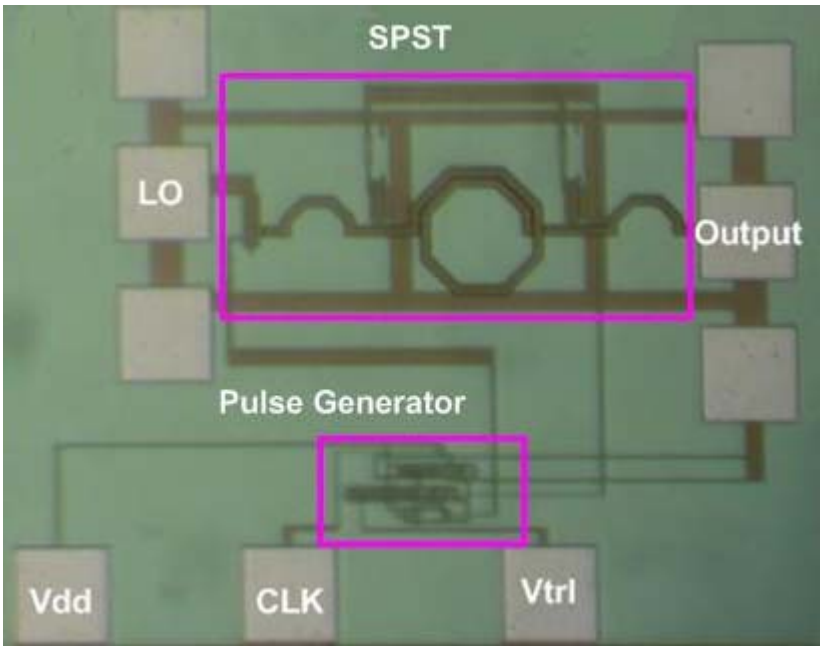
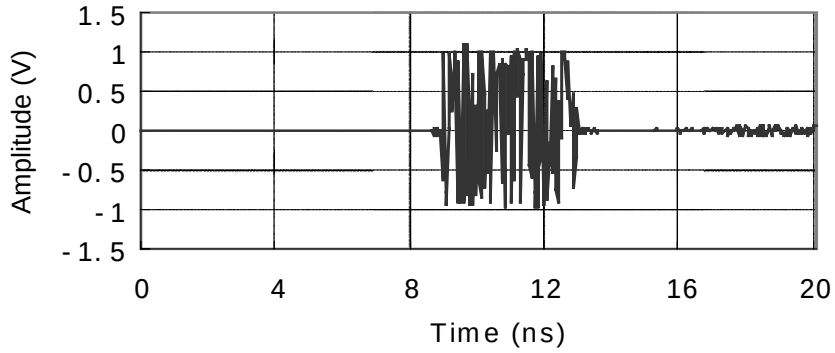
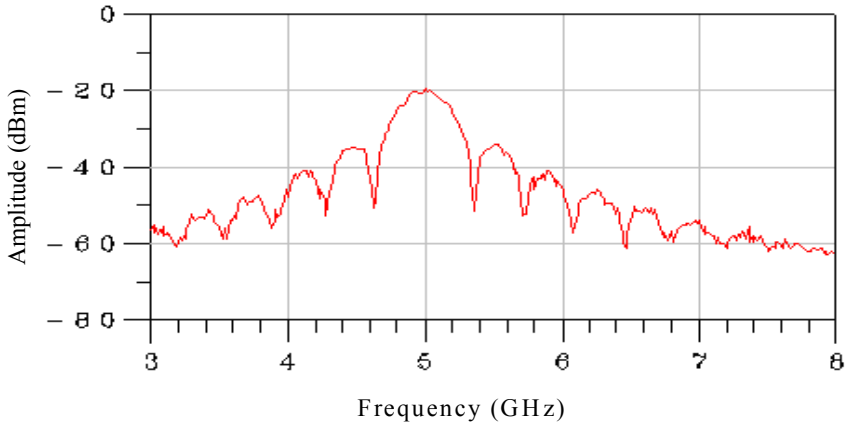


Figure 4.16 Microphotograph of the 0.18-um CMOS UWB demonstration chip integrating the pulse generator and the SPST switch.



(a)



(b)

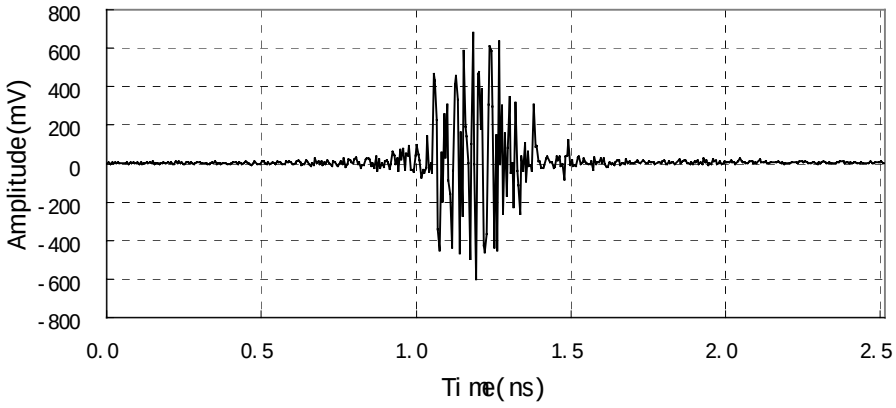
Figure 4.17 Measured UWB signal having 500MHz bandwidth. (a) Time-domain Waveform, (b) spectrum.

Apparently, the spectrum shown in Fig. 4.17 (b) fails the FCC ERIP emission density limit, -41.24 dBm/MHz, by 50 dB higher. To generate a 500 MHz instantaneous UWB bandwidth entirely compliant with the FCC power density mask, it is a practical to

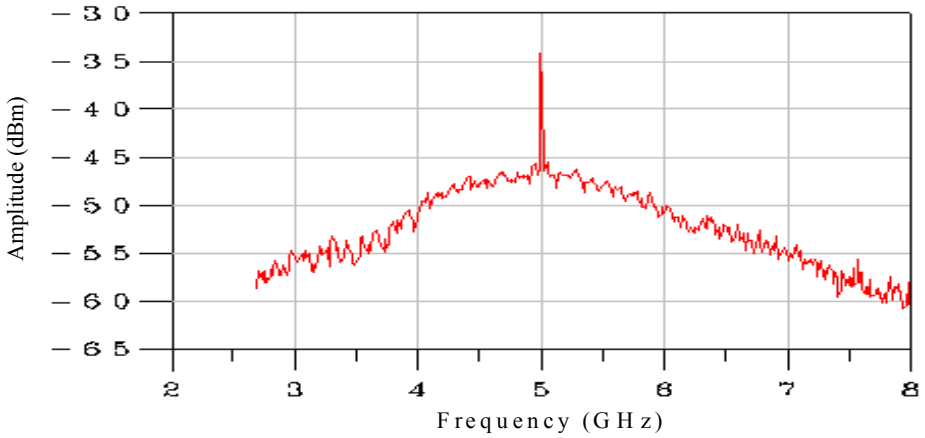
lower the emission power by attenuating down the input 5 GHz oscillation wave 50 dB, while keep the pulse width of the control signals to the SPST switch. The function of attenuation can be easily achieved by tuning the buffer's bias current such that the input wave swing to the switch is refined around 6 mV (peak to peak).

By increasing the external biasing voltage for the pulse generator and hence narrowing the pulsewidth of the control signal to the SPST switch, the pulsewidth of the UWB signal is reduced consequently. When the pulsewidth is reduced to a certain value, the amplitude of the UWB signal, however, diminishes because the SPST switch cannot be completely turned on any more, which results in partial reflections of the carrier signal. When the amplitude of the UWB signal decreases to half of its maximum value (2 V), the corresponding duration is defined as the minimum pulsewidth. This minimum pulsewidth is measured as 0.5 ns.

Fig. 4.18 displays the UWB signal with this minimum pulsewidth, generating the maximum instantaneous bandwidth at the same time. The peak-to-peak output voltage amplitude is around 1 V. The 10-dB bandwidth is around 4 GHz. The LO leakage overshooting can be clearly seen from the spectrum of this signal because only a single-stage switching is used here. This LO leakage confirms experimentally the need of a double-stage switching for the carrier-based UWB transmitters (Fig. 4.2), as explained in Section 4.1. With another stage of switching, making the buffer standby within majority partition of period, the LO leakage can be reduced to a negligible level.



(a)



(b)

Figure 4.18 Measured UWB signal having 4 GHz bandwidth. (a) Time-domain waveform, (b) spectrum.

The 4 GHz broadband spectra in Fig. 4.18 (b), with a maximum output power density 25 dB higher than the FCC limit, -41.3 dBm/MHz, requires that the input wave amplitude be reduced from 2 V peak-to-peak to 110 mV peak-to-peak.

The pulsewidth of the obtained UWB signal can be further reduced, hence achieving wider signal bandwidth than 4 GHz. This, however, is obtained at the expense of its signal amplitude due to the aggravated reflection of the SPST switch working at fast transient without being completely turned on.

With both levels of switching, the efficiency of the transmitter will not be reduced due to the added power consumptions of the VCO and buffer, with the former particularly dominating the efficiency owing to its larger power consumption. The VCO is always on, hence consuming power, in order to deliver a fixed oscillation during both switching transitions. Apparently, the demonstrations of generating minimum bandwidth, 500 MHz, and maximum bandwidth, 4 GHz, quantifies experimentally the requirements of the very small output amplitudes from the tunable buffer, 6 mV and 110 mV respectively. These weak output waves suggest that the buffer will consume very small amount of current and primarily attenuate the strong oscillation from the VCO. And thus whole RF front-end circuitry, including the VCO, buffer and SPST switch, is of high power efficiency.

It is relatively easy, given a fixed carrier frequency, to achieve much higher power efficiency since the VCO and the buffer can be optimally designed with a very narrow band in the vicinity frequency range of the carrier.

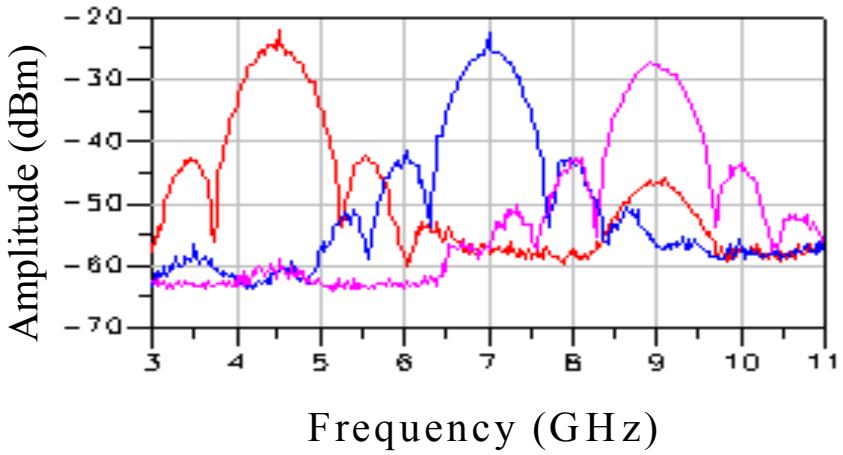


Figure 4.19 Measured spectrums of UWB signals covering the 3.1–10.6-GHz

Fig. 4.19 shows the measured spectrums of different UWB signals, obtained by varying the carrier frequency at a certain bias voltage for the pulse generator in order to have the same instantaneous 500 MHz UWB bandwidth, demonstrating that the entire UWB band of 3.1–10.6 GHz can be achieved with the developed CMOS chip by using a multiband signal source. While the signal source output amplitude was kept constant during frequency sweeping, it should be noted that there is around 3 dB output power reduction at higher frequencies. This is not due to the flatness of the insertion loss of the switch, but the parasitic capacitances effects from the RF pads. The capacitances of the RF pads cannot be removed out during the demonstrations, and hence the impedances were not perfectly matched with the impedances of the input source, a signal generator and the output measurement, a digital oscilloscope. The reflections aggravated when

frequencies went higher, which resulted in smaller transmission power detected by the digital oscilloscope.

Moreover, it is shown that the effective emission power at the transmitter's output will be compliant with FCC's EIRP density limits by lowering down the input wave to the switch after the tunable buffer. The next chapter will present the feasibility of the tuning attenuation of the buffer in detail.

CHAPTER V

INTEGRATED LC VCO AND TUNABLE BUFFER

Voltage Controlled Oscillators (VCOs) are essential building blocks in wireless communication systems and are used as local oscillators to up and down-convert signals. One of the major applications for VCO is for a frequency synthesizer, which is a core building block in wireless communication transceivers to provide multiple frequencies. In this application, the VCO provides sinusoidal or pulse signals that are predetermined frequencies that are precisely controllable by digital bits. Design of integrated oscillators has posed many challenges to circuit designers since they involve simultaneous optimization of multiple variables, such as frequency tuning range, phase noise, harmonic distortion, output power and power consumption [61].

Due to their relatively good phase noise, ease of implementation and differential operation, cross-coupled inductance-capacitance (LC) oscillators play an important role in high-frequency circuits design. This kind of oscillator is widely used in many well-known wireless communications, where high sensitivity, low phase noise, and differential operation are needed, such as GSM, Blue tooth, and 802.11g. It also has the most potential applications for our proposed time domain carrier-based UWB, where low jittering of timing is required [62].

5.1 Theory of Oscillators

A simple oscillator produces a periodic output, usually in the form of voltage. As such the circuit has no input while sustaining the output indefinitely. To start an oscillation for a unity-gain negative feedback circuit given by Fig. 5.1, the close loop gain described by Eq. (5.1) would exhibit an infinity value in order to initiate the oscillation from noise level.

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{5.1}$$

Where $H(s)$ is the open loop gain and we have

$$s = j\omega_0, \; H(j\omega_0) = -1 \tag{5.2}$$

This indicates that the overall feedback shown in Fig. 5.1 becomes positive and any noise components at ω_0 experiences an infinity gain and thus start up oscillation at frequency, ω_0.

Defined as "Barkhansen criteria" [63], if a negative-feedback circuit has a loop gain that satisfies two conditions:

$$\left|H(j\omega_0)\right| \geq 1 \tag{5.3}$$

And

$$\angle H(j\omega_0) = 180^0 \tag{5.4}$$

Then the circuit may oscillate at ω_0.

However, indicated by [64], these two conditions are necessary, but not sufficient. In order to ensure oscillation in the presence of temperature, supply voltage, noise and process variations, the loop gain is normally set to be at least twice or three times the start up value [65].

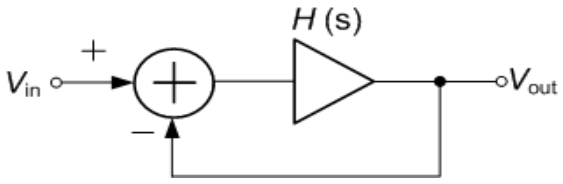
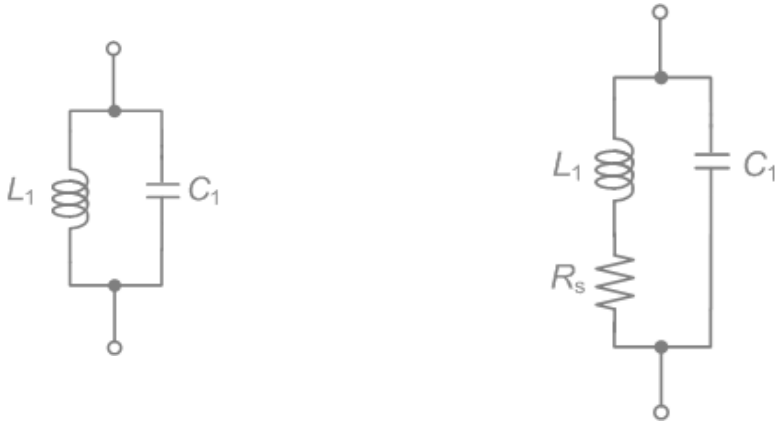


Figure 5.1 A feedback system.

5.2 LC Oscillators

Monolithic inductors have gradually appeared in bipolar and CMOS technologies in the past decade, making it possible to design integrated oscillators based on passive resonant circuits comprising a parallel LC network.

As shown in Fig. 5.2 (a), an ideal parallel LC resonator has an infinite impedance at resonant frequency $\omega_0 = 1/\sqrt{L_1 C_1}$ due to the fact that the impedances of the inductor, $j\omega_0 L_1$, and the capacitor, $1/j\omega_0 C_1$, are equal and opposite in polarity. In reality, the monolithic passive components suffer from the resistive losses, especially the commonly used integrated planar inductor [41]. The spiral inductor used in bipolar and CMOS processes can be represented by adding a series resistance as shown in Fig. 5.2 (b). The equivalent impedance of the LC tank is given by Eq. (5.5) as



(a) (b)

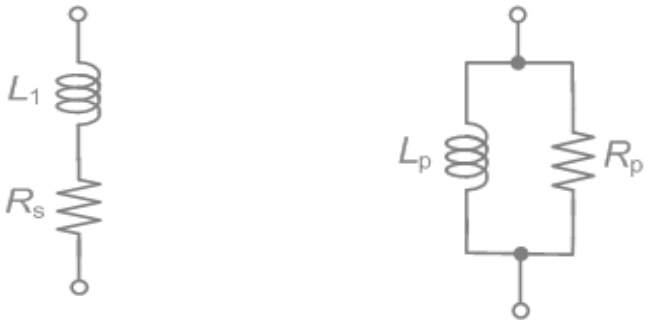
Figure 5.2 (a) Ideal and (b) realistic LC tank

$$Z_{eq}(s) = \frac{R_s + L_1 s}{1 + L_1 C_1 s^2 + R_s C_1 s} \tag{5.5}$$

and hence,

$$\left|Z_{eq}(s=j\omega)\right|^2 = \frac{R_s^2 + L_1\omega^2}{(1-L_1C_1\omega^2)^2 + R_s^2C_1^2\omega} \tag{5.6}$$

The magnitude of Z_{eq} given in Eq. (5.6) does not go to infinity at any ω and reaches a peak in the vicinity of $\omega = 1/\sqrt{L_1C_1}$. It is noted here that the actual resonance frequency has some dependences on R_s. This dependency can be more clearly analyzed by transforming the network in Fig. 5.2 (b) into an equivalent RLC parallel network.



(a) (b)

Figure 5.3 Conversion of a series LR network (a) to a parallel LR network (b).

For a narrow frequency range, it is possible to convert the series LR shown in Fig. 5.3 (a), into parallel LR in Fig. 5.3 (b) without losing accuracy. Within the vicinity of the interested frequency, the two impedances need to be equivalent:

$$L_1 s + R_s = \frac{R_p L_p s}{R_p + L_p s} \tag{5.7}$$

Replacing s by $j\omega$, (5.7) can be rewritten as

$$(L_1 R_p + L_p R_s) j\omega + R_s R_p - L_1 L_p \omega^2 = R_p L_p j\omega \tag{5.8}$$

Eq. (5.8) must hold for all values of ω within narrow band vicinity, mandating that

$$L_1 R_p + L_p R_s = R_p L_p \tag{5.9}$$

and

$$R_s R_p - L_1 L_p \omega^2 = 0 \tag{5.10}$$

Calculating R_p form Eq. (5.10) and substituting it into Eq. (5.9), we have

$$L_p = L_1 (1 + \frac{R_s^2}{\omega^2 L_1^2}) \tag{5.11}$$

Since the quality factor of the monolithic spiral inductor can be greater than 5 in mostly used advanced processes. Thus

$$L_p \approx L_1(1+1/Q^2) \approx L_1 \tag{5.12}$$

And from Eq. (5.10), R_p can be expressed as,

$$R_p \approx \frac{L_1{}^2 \omega^2}{R_s} \tag{5.13}$$

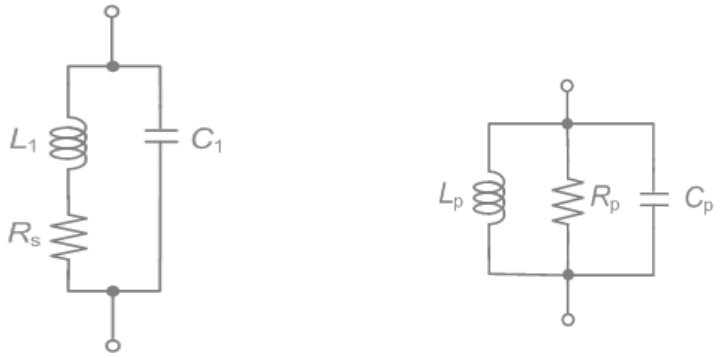
We have

$$R_p \approx Q^2 R_s \tag{5.14}$$

Where

$$Q = L_1\omega \big/ Rs \tag{5.15}$$

The above transformation allows the conversion of the network in Fig. 5.4 (a) to a parallel RLC network shown in Fig. 5.4 (b), where $C_p = C_1$, and L_p, C_p are lossless reactive components.



(a) (b)

Figure 5.4 Conversion of a tank (a) to a parallel LRC network (b).

The insight gained from the parallel LRC network in Fig. 5.4 (b) is that at $\omega = 1/\sqrt{L_p C_p}$ the tank reduces to a simple resistor, and the phase difference between the voltage and current of the tank drops to zero.

More intuitively, when a "negative resistor" equal to -R_p is placed in parallel with R_p, shown in Fig. 5.5, the tank oscillates indefinitely as a result of parallel impedance becoming infinity, $R_p // (-R_p) = \infty$. As a consequence, the oscillation frequency is merely determined by L_p and C_p, as

$$\omega_0 = 1/\sqrt{L_p C_p} \tag{5.16}$$

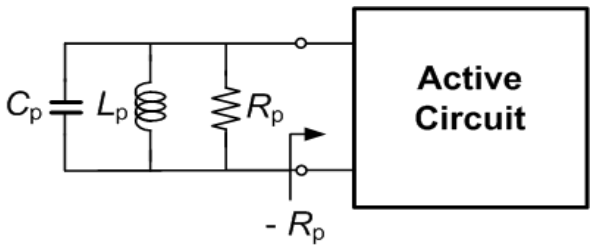


Figure 5.5 Use of an active circuit to provide negative resistance.

A negative resistance can be achieved by a positive feedback. The output impedance of the feedback active network shown in Fig. 5.1 is given by [64],

$$Z_{out\_loop} = \frac{Z_{out\_open}}{1 + H(s)} \tag{5.17}$$

where Z_{out_loop} is the output impedance with the feedback (close loop), Z_{out_open} is the output impedance without feedback (open loop), and $H(s)$ is the loop gain of the feedback system.

Thus, at resonance frequency given by (5.16), if the loop gain is sufficiently negative (i.e., the feedback is sufficiently positive), a negative resistance is achieved for Z_{out_loop}. To sustain a stable oscillation, the negative resistance is typically make as -3 R_p [61], [64], and [66].

5.3 Voltage-Controlled Oscillators

Most applications require that oscillators be tunable, i.e., their output frequency be a function of a control input, normally a DC voltage. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage (Fig. 5.6):

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont} \tag{5.18}$$

Here, ω_0 represents the intercept corresponding to $V_{cont} = 0$ and K_{VCO} denotes the gain of the VCO, expressed in rad/s/V (or sometimes in Hz/V) measuring the conversion from DC voltage to frequency. The achievable range, $\omega_2 - \omega_1$, is called the tuning range.

It is worthy of summarizing the important performance parameters of VCOs:

Center Frequency The center frequency, for instance the midrange value in Fig. 5.6, is determined by the system in which the VCO is used.

Tuning Range The required tuning range is dictated by two parameters: (1) the variation of the VCO center frequency with process and temperature and (2) the frequency range required by the system application. In advanced CMOS processes, the center frequency of some VCO may need to be designed to cover twice of the desired frequency range to allow variations of process and temperature, thus mandating a sufficiently wide ($\geq 2\times$) tuning range to guarantee that the VCO output frequency can be driven to the desired value.

Output Amplitude It is desirable to achieve a large output oscillation amplitude, thus making the waveform less sensitive to noise. The amplitude trades with power dissipation, supply voltage, and even the tuning range.

Power dissipation As with other RF circuits, VCO suffers from trade-offs between speed, power dissipation, and noise. Typical CMOS VCO drains 1 to 10 mW of power.

Supply and Common-Mode Rejection VCOs are quite sensitive to noise, especially if they are realized in single-ended form. The design of VCOs for high noise immunity is a difficult challenge. Note that noise may be coupled to the control line of a VCO as well. So, it is always preferable to employ differential paths for both the oscillation signal and the control line.

Output signal purity Even with a constant control voltage, the output waveform of a VCO is not perfectly periodic. The electronic noise of the devices in the oscillator and supply noise lead to noise in the output phase and frequency. These effects are quantified by “jitter” and “phase noise” and determined by the requirements of each application.

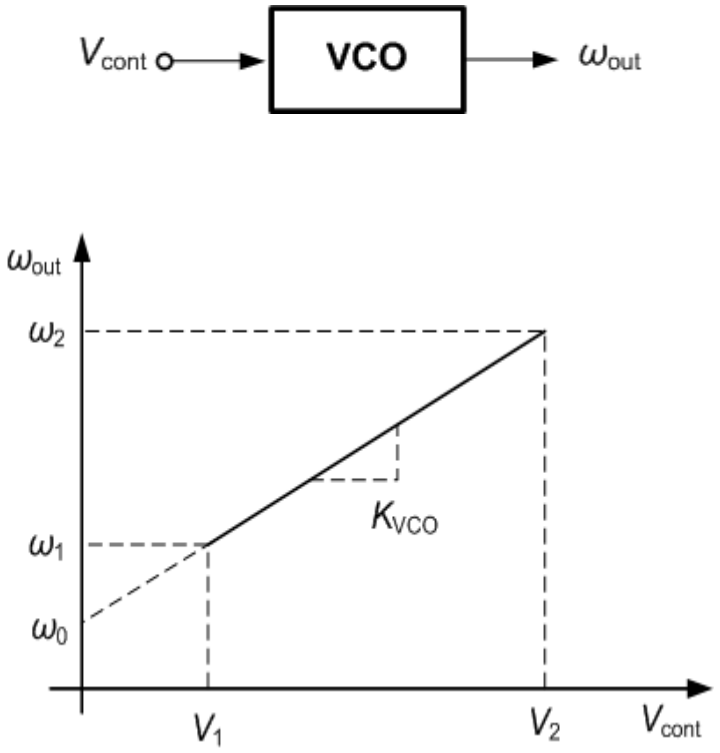


Figure 5.6 Definition of a VCO

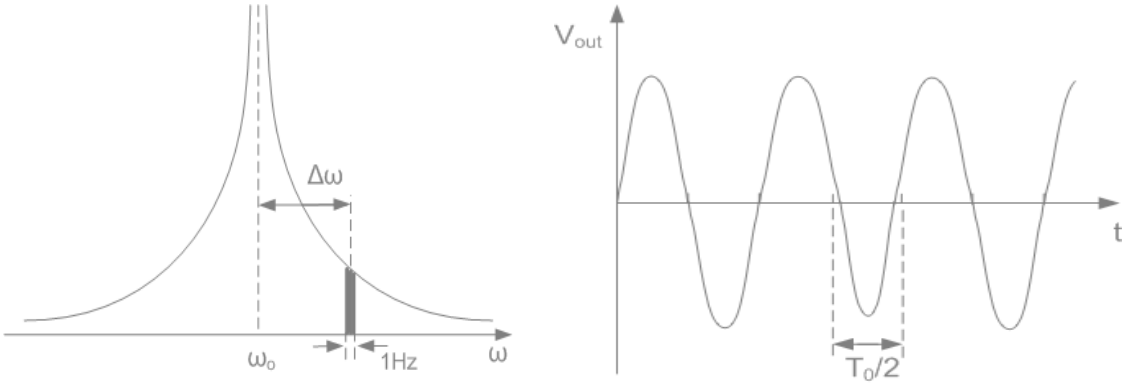
5.4 Phase Noise

5.4.1 Definition of Phase Noise

The output of an ideal oscillator is a perfect sinusoidal wave of frequency ω_0, i.e. $Vout(t) = A \cdot \sin(\omega_0 + \theta)$ with A the amplitude and θ a fixed phase reference. In the frequency domain this corresponds to a Dirac impulse at ω_0, $\delta(\omega_0)$. In a real oscillator,

noise generates fluctuation on the phase and the amplitude of the signal. The output signal becomes

$$V_{out}(t) = (1 + a(t)) \cdot A \cdot \sin(\omega_0 + \theta(t)) \tag{5.19}$$



(a) (b)

Figure 5.7 The frequency (a) and time (jitter) (b) representation of phase noise in an oscillator at ω_0.

Due to the fluctuations on phase and amplitude, $\theta(t)$ and $a(t)$, the output spectrum is no longer a Dirac impulse, but exhibits sidebands close to the oscillator frequency, as shown in Fig. 5.7 (a). Since well-designed, high-quality oscillators are usually very amplitude stable, $a(t)$ can be considered constant over time. To quantify phase noise $\theta(t)$, the noise power in a unit bandwidth at a certain offset frequency $\Delta\omega$

from ω_0 is considered and divided by the carrier power. The result is a single sided spectral noise density in unit dBc/Hz:

$$L\{\Delta\omega\} = 10\log\left(\frac{\text{noise power in a 1Hz band at } \omega_0 + \Delta\omega}{\text{carrier power}}\right) \quad (5.20)$$

Moreover, the noise on the phase of a sinusoidal signal translates to a phase noise skirt in the oscillator's output spectrum. The phase noise is random noise, which is difficult to analyze. So, for simplicity, we suppose that the phase fluctuation in Eq. (5.19) is a single sinusoidal tone described as $\theta(t) = \theta_m \cdot \sin(\omega_m t)$ with $\omega_m t = 1$, where ω_m is the offset from the carrier. Based on (5.19) and ignoring $a(t)$, the output signal can be described as

$$V_{out}(t) = A \cdot \sin\left[\omega_o + \theta_m \cdot \sin(\omega_m t)\right] \quad (5.21)$$

Eq. (5.21) can be further expanded as

$$V_{out}(t) = A \cdot \sin(\omega_o t) \cdot \cos\left[\theta_m \sin(\omega_m t)\right] + A\cos(\omega_0 t) \cdot \sin\left[\theta_m \cdot \sin(\omega_m t)\right] \quad (5.22)$$

Since $\omega_m t = 1$, then the output of the oscillator becomes:

$$V_{out}(t) \approx A \cdot \sin(\omega_o t) + A \cdot \frac{\theta_m}{2} \cdot \left\{\sin\left[(\omega_o + \omega_m)t\right] + \sin\left[(\omega_o - \omega_m)t\right]\right\} \quad (5.23)$$

The output spectrum of the oscillator consists of a narrow-ban FM signal with θ_m the modulation index, resulting in a strong component at ω_0 and two small side lobes at $\omega_0 \pm \omega_m$. Therefore, the oscillator output voltage power spectral density (PSD) is directly related to the phase noise PSD which can be obtained by taking the FFT of those time domain expressions. The PSD of the fluctuation $\theta(t) = \theta_m \cdot \sin(\omega_m t)$ then can be converted into following equation by taking the real part of the FFT

$$S_\theta(\omega) \approx \frac{{\theta_m}^2}{2} \cdot \delta(\omega - \omega_m) \tag{5.24}$$

Where $S_\theta(\omega)$ is the PSD of the phase fluctuation $\theta(t) = \theta_m \cdot \sin(\omega_m t)$, and $\delta(\omega - \omega_m)$ is the Delta function. The oscillator output voltage power spectral density (PSD) is obtained from Eq. (5.23) as

$$S_{Vout}(\omega) \approx \frac{A^2}{2} \cdot \left[\delta(\omega - \omega_0) + \frac{1}{2} S_\theta(\omega - \omega_0) + \frac{1}{2} S_\theta(\omega_0 - \omega) \right] \tag{5.25}$$

and it is directly related to the phase noise PSD, as in Eq. (5.24).

Eq. (5.24) is the phase noise PSD of single tone. The real signal consists of continuous frequencies offset from the carrier and so the phase noise spectrum can be seen as a sum of sinusoid waves. Therefore, the total phase noise skirt is directly

translated to noise side lobes at both sides of the carrier frequency, as shown in Fig. 5.8. The actual phase noise at an offset ω_m is then:

$$L\{\omega_m\} = 10\log\left(\frac{S_{Vout}(\omega_0+\omega_m)}{A^2/2}\right) = 10\log\left(\frac{S_\theta(\omega_m)}{2}\right) \qquad (5.26)$$

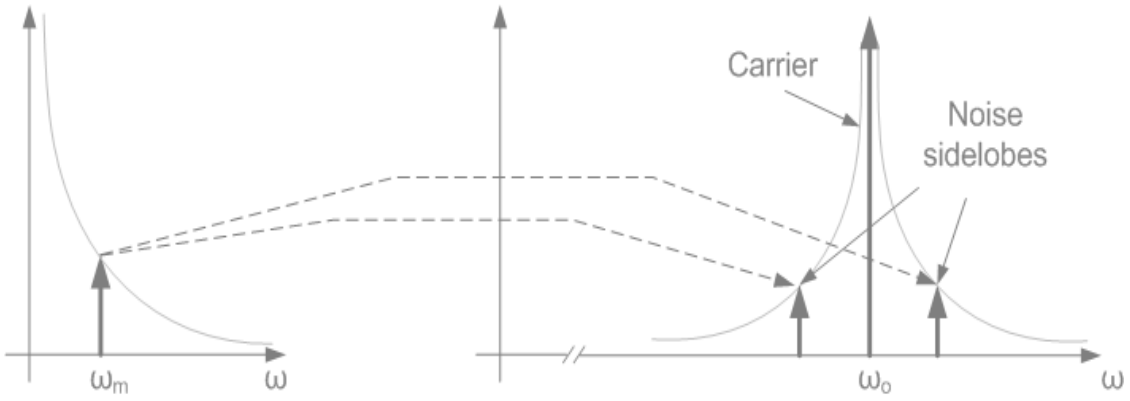


Figure 5.8 From noise on the phase to the oscillator output spectrum.

Phase noise is related to the PSD of instantaneous frequency deviations $\Delta f(t)$, since frequency is the derivative of phase as $\Delta f(t) = d[\omega(t)]/dt$. So, the phase noise in frequency domain can be derived directly using PSD in phase domain as $S_{\Delta f}(\omega) = \omega^2 \cdot S_\theta(\omega)$, and from Eq. (5.26), we have

$$S_{\Delta f}(\omega) = 2\omega^2 \cdot 10^{L\{\omega m\}/10} \qquad (5.27)$$

The noise seen in the frequency spectrum has also an effect in the time domain. Due to the noise related phase/frequency deviations, there is uncertainty on the zero-crossing of the oscillator signal: the exact time of one period of the sine wave differs from period to period, as shown in Fig. 5.7 (b). Since θ_m is small, the waveform is almost periodic, with an average period of T_0, corresponding to ω_0 and a timing error $\Delta\tau$. Several measures for the timing error exist such as *cycle-to-cycle* jitter, i.e. the difference between two consecutive periods, or as *absolute* jitter, i.e. the timing error between two periodic waveforms with the same frequency. Since the phase noise is considered stationary, and Gaussian, the standard deviation or effective variance of the timing error, $\sigma_{\Delta\tau}$ of $\Delta\tau$**, is** the *rms* value of the timing error. A first-order formula to relate jitter to phase noise is to assume white noise dominating the phase noise, and so the white phase noise can be derived from the more general definition for jitter [67], with T_0 the period of the oscillator signal:

$$L\{\omega_m\} = 10\log\left[\frac{2\pi\omega_0}{\omega_m^2}\cdot\left(\frac{\sigma_{\Delta\tau}}{T_0}\right)^2\right] \tag{5.28}$$

As mentioned before, the phase noise limits the quality of different communication systems. Typically, in a communication system a small wanted signal must be detected in the presence of large unwanted signals. In the receive path, the wanted signal is down converted by the local oscillator signal. If a noisy oscillator is used, the large unwanted signal is down converted by the phase noise at the offset

frequency of the unwanted signal, as illustrated in Fig. 5.9, which may not be filtered out. The dark box represents unwanted noise in the wanted signal band. If the phase noise at the given offset frequency is not sufficiently low, the unwanted noise in the signal band seriously degrades the signal-to-noise ratio (*SNR*). In the transmit path, the high-power output signal must satisfy a given power mask, such that the transmitted noise does not drown other transmitted signals. Therefore, the output spectrum of the oscillator must comply with the same power mask, **so** that the up-converted signal does too. Usually, this requirement is much less stringent than the one imposed by the reception quality.

5.4.2 Phase Noise Modeling

For now, it is known that there are typically three noise regions. At high offset frequencies, a white phase noise floor can distinguish. From there, the phase noise rises in reverse proportion to the square of the offset frequency (ω^{-2}). This noise is in fact white noise that is frequency modulated around the carrier in the VCO circuit. The –20 dB/dec slope originates from the fact that frequency is the derivative of phase. Close to the carrier, frequency modulated 1/f noise determines the ω^{-3} region. The typical 1/f noise corner is not equal to the $1/f^3$ noise corner, but depends on non-linearity in the VCO amplifier. If the amplifier is linear, these two corners are the same.

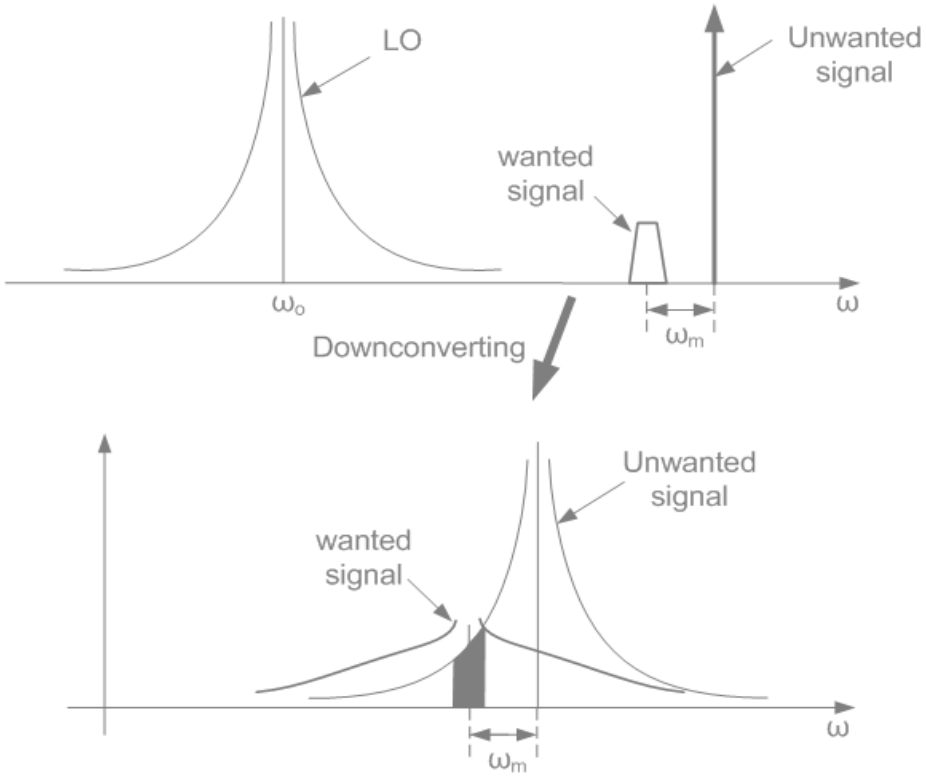


Figure 5.9 The effect of phase noise on the reception quality of a communication system.

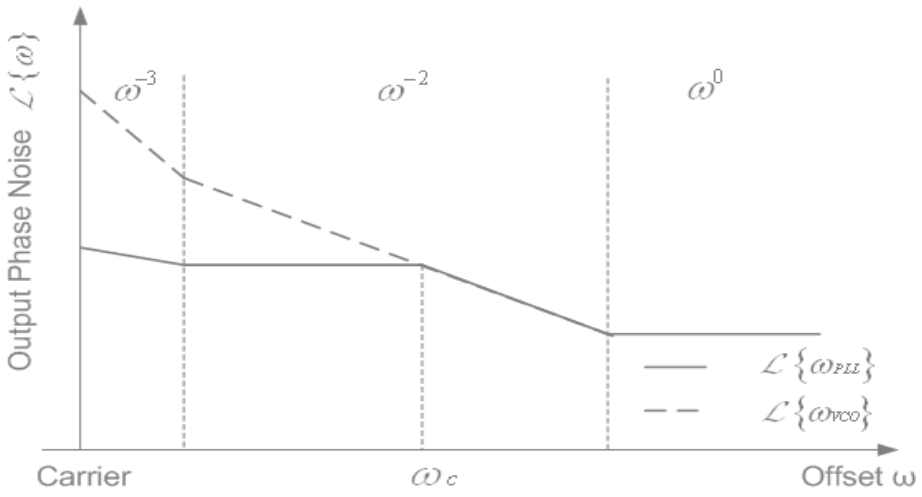


Figure 5.10 The phase noise transfer functions in a PLL frequency synthesizer.

Fig. 5.10 shows the typical PLL frequency synthesizer output phase noise versus offset frequencies in phase domain, where ω_c is the 3-dB cut-off frequency of the closed loop response of the PLL, $L\{\omega_{PLL}\}$ and $L\{\omega_{VCO}\}$ are phase noise of the PLL and VCO in phase domain respectively. It is shown that due to the low path filter of the PLL loop, the high offset frequency noise of the VCO passes unaltered. While at the low offset frequencies of the VCO, e.g. from carrier to ω_c, the phase noise is successfully suppressed. Therefore the phase noise of the VCO at low offset frequencies on the dashed-line in Fig 5.10, from the carrier to ω_c, does not appear at output of the frequency synthesizer. As a result, at the -low offset frequencies, form carrier to ω_c, phase noise of

the carrier, the output of the frequency synthesizer, is mainly contributed by the other parts of the PLL, including reference clock, phase detector, charge pump and etc.

The most well-known and oldest phase noise theory is the empirical derivation by Leeson [68] of the expected spectrum of an oscillator:

$$S_{\phi,\,Lees}(\omega_o + \Delta\omega) = \left(\frac{\omega_o}{2Q}\right)\cdot\frac{2KTF}{P_S}\cdot\Delta\omega^{-2} \qquad (5.29)$$

Where F is the effective noise figure of the oscillator and $P_s = V_A^2/(2R_p)$ is the rms signal power in Watts caused by a resistor R_p with V_A AC amplitude applied to it. By multiplying the signal power by R_p, the signal power in rms is found. Replacing the P_s in Eq. (5.29) by $V_A^2/(2R_p)$, Leeson's formula becomes:

$$L_{\,Lees}\{\Delta\omega\} = 4kTR_p\cdot F\cdot\left(\frac{1}{2Q}\right)^2\left(\frac{\omega_0}{\Delta\omega}\right)^2\cdot\frac{2}{V_A{}^2} \qquad (5.30)$$

And $$F = 1+\gamma n G_M R_p$$

where k is the Boltzmann constant, T is temperature, γ is the excess noise of the active element ($\gamma = 2/3$ for long-channel MOSFET devices), n takes into account bulk transconductance modulation by channel thermal noise ($n \approx 1.5$ for long channel devices [69]), meaning that $\gamma n \approx 1$, G_m is the transconductance of the amplifier

transistor, the R_p the effective loss resistance of the tank, Q the quality factor of the tank, ω_0 oscillation frequency, $\Delta\omega$ the offset frequency, and V_A the amplitude of oscillation.

In fact, Leeson does not make the distinction between phase noise and amplitude noise, such that he predicted noise a factor 2 too high. By including the amplitude noise, contributing roughly 3 dB, Leeson incorporates another 3 dB noise multiplication in phase noise calculation, which was surmised later as a result of the nonlinearity of the active devices of the oscillator [70].

Another linear phase noise theory is the one presented by Granincks [69]. His phase noise formula states:

$$L_{Cran}\{\Delta\omega\} = 4kT\,\mathrm{R}_{eff}\cdot(1+A)\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\cdot\frac{2}{{V_A}^2} \qquad (5.31)$$

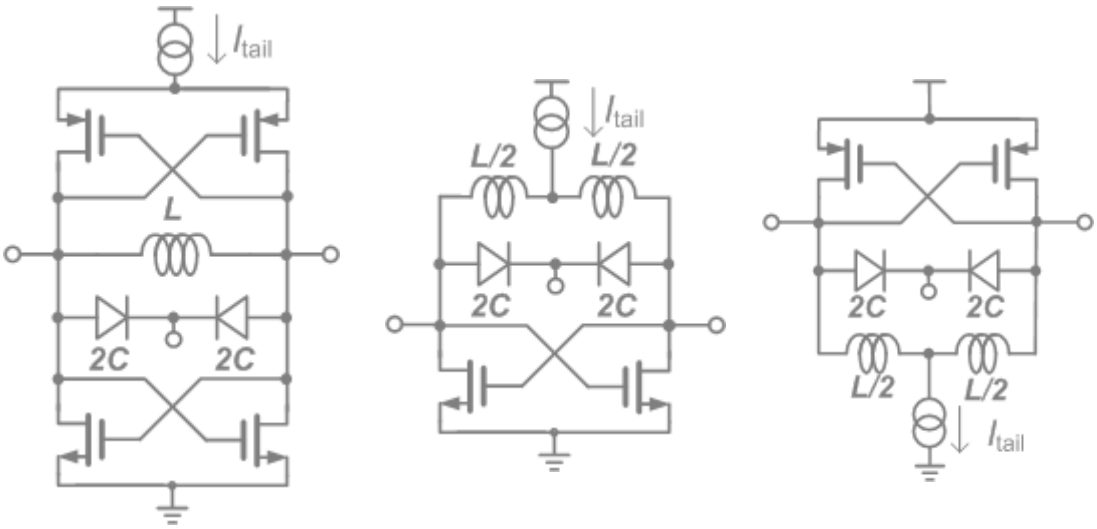
With R_{eff} the effective tank resistance in series with the inductor, which is defined as $R_{eff} = \frac{R_p}{Q^2} = \frac{(\omega L)^2}{R_p}$. And coefficient $A = \gamma n G_M R_p$. This formula unfortunately could not include the non-linearity realities of the amplifiers and varactors in CMOS oscillators and thus still 3 dB higher than the actual phase noise.

A more general phase noise theory, which takes into account the non-linear behaviors of the active element and therefore noise conversion, is the theory of Hajimiri [70], where Hajimiri works with the real small-signal transfer function, called as Impulse Sensitivity Function (*ISF*) Γ_x. The *ISF* is periodic and can be written as a Fourier series to reflect the fact that all odd harmonics of the oscillation are related with noise

upconversion to fundamental. As a result the predicted phase noise is more accurate. But the phase noise calculations do not yield a direct relationship between circuit design parameters and the phase noise, and the circuits design still relies on an accurate simulation for each design procedure.

5.5 CMOS LC VCO

The active circuit of an oscillator must provide a negative resistance to provide a negative loop resistance to sustain the oscillation. One transistor suffices for this task, but for a balanced design minimum 2 transistors are necessary. The common source structure uses two cross-coupled transistors to provide the required positive feedback. Several implementation flavors exist: nMOS-only, pMOS-only or complementary with nMOS and pMOS cross-coupled transistors (Fig. 5.11). To provide current biasing, additional transistors to form current sources are needed which have no influence on the performance in a perfectly balanced design.



(a) (b) (c)

Figure 5.11 VCO topologies. (a) Complementary, (b) nMOS-only and (c) pMOS-only

5.5.1 Current-limited Regime and Voltage-limited Regime

Two modes of operation, namely current- and voltage-limited regimes, can be identified for a typical LC oscillator, considering the bias current as the independent variable [61]. In the current-limited regime, the oscillations amplitude linearly grows with the bias current according to until the oscillator enters the voltage-limited regime. In the voltage-limited regime, the amplitude is limited to some value, V_{limit}, which is determined by the supply voltage and/or a change in the operation mode of active devices (e.g., MOS transistors entering triode region). Thus, can be expressed as

$$V_A = \begin{cases} I_{tail} \cdot R_p & (I-\text{limited}) \\ V_{\text{limit}} & (V-\text{limited}) \end{cases} \tag{5.32}$$

In the current-limited regime, the bias current determines the amplitude of the oscillator. In Fig. 5.12, the influence of the current on the phase noise is calculated for an nMOS-only (solid) and a complementary topology (dashed), using RF spectra simulator in Cadence, where the LC tank has a typical quality factor, $Q = 10$, and 0.25 μm CMOS transistor parameters are chosen for a Vdd of 1.8 V at 5 GHz. The triangle signs (Δ) present the boundaries between the current-limited regime and the voltage-limited regime, which were obtained by calculations using Cadence. When the bias current was lower than the triangle signs, the current source devices were always working within saturation regions. However, increasing the bias current beyond the triangle signs pushes the current source devices into triode region due to the larger oscillation swings. In the complementary topology, the amplitude is fixed by the power supply and the phase noise increases due to noise upconverstion. For low power supply voltages, the lowest phase noise is attainable with an nMOS- or pMOS-only topology at the expense of high current for both modes. It is noted that for the complimentary topology, the bias current should be such that the VCO operates at the boundary between the current-limited and the voltage-limited regime, which is the optimal design point for good phase noise with low power consumption (the triangle sign in Fig. 5.12 on the dashed curve).

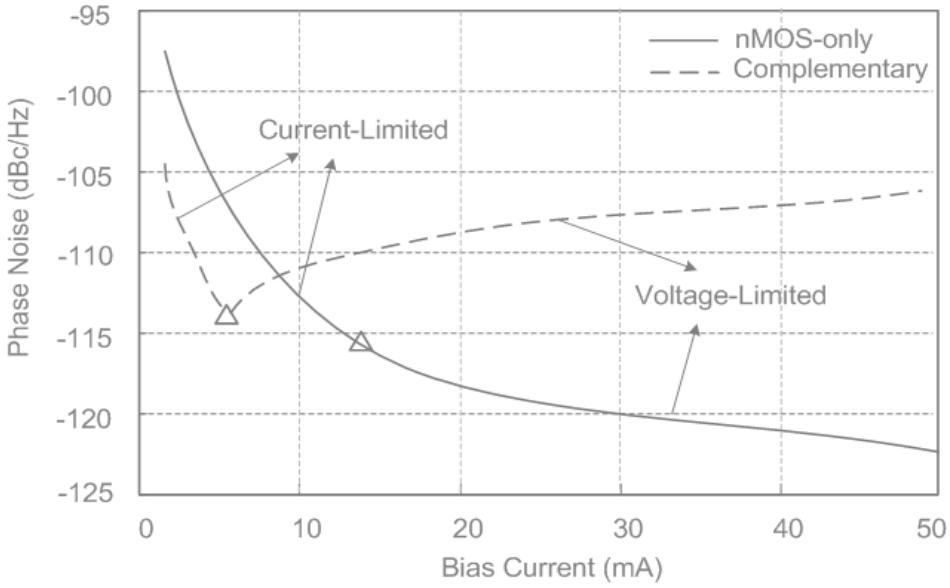


Figure 5.12 Calculated phase noise at 1MHz offset versus the bias current for typical LC-tank and transistor parameters and V_{DD} = 1.8 V at 5 GHz.

5.5.2 Complementary MOS vs. nMOS (pMOS) -only VCO

To compare the performance of different VCO topologies in Fig. 5.11, it is assumed that the bias conditions and the LC-tanks are all the same. The transistors are assumed to be fully switched on during one half period and off during the other half as an ideal switch without any transient, such that the drain current of the transistors is a square wave [65].

In the complimentary topology shown in Fig. 5.11 (a), the transconductances of the nMOS and pMOS must be equal for balance and the sum of both transconductances is equal to G_M, while for the nMOS-only topology shown in Fig. 5.11 (b) $G_M = g_{m,n}/2$. In the complementary case, the bias current I_{tail} is drawn through the LC tank twice every period [65], while in the nMOS-only case the current is drawn through half of the tank in each period.

Fig. 5. 13 (a) shows the current switching behavior in the complimentary VCO topology with the assumption that all the transistors operate as ideal switches during steady state oscillation, and Fig. 5.13 (b) shows the current switching in the nMOS-only VCO topology, which has the same LC tank as Fig. 5.13 (a), but the current source feeds at the center point of the tank inductor. In Fig. 5.13 (a), when the differential outputs OSC_1 and OSC_2 performance positive oscillation swing and negative oscillation swing respectively, transistor M_1 and M_4 are switched on but M_2 and M_3 are switched off, the bias current, I_{tail}, flows from the bias current source, through M_1, LC tank, and M_4 and then to the ground. While OSC_1 and OSC_2 have negative oscillation swing and positive swing respectively, the bias current, I_{tail}, flows through M_2, LC tank, and M_3 to the ground and transistors M_1 and M_4 are switched off in this half period. Denoting the differential oscillation voltage as the transient voltage potential at OSC_1 in relation to OSC_2 and positive current direction from OSC_1 to OSC_2 , the oscillation voltage and current switching of Fig. 5.13 (a) can be described by Fig. 5.13 (c). The tank current exhibits a rectangular waveform due to the ideal switching of the transistors and the peak currents are I_{tail} and $-I_{tail}$. The output oscillation voltage, on the other hand, is not

rectangular shape, but approximates a sinusoid waveform, because the LC tank suppresses higher harmonics voltages and only the fundamental voltage, therefore, appears at the two terminals of the tank. Fig. 5.13 (c) can also describe the oscillation voltage and current switching transients of nMOS-only VCO in Fig. 5.13 (b), where it is interesting to note that the bias current I_{tail} flows through only half of the LC tank and results in the same tank current swing but half peak oscillation voltage as the topology in Fig. 5.13 (a).

For the complimentary VCO, a current swing in Fig. 5.13 (a) on the tank resistor, R_p, generates a rectangular voltage swing waveform. The peak-to-peak voltage is $V_A = 2R_pI_{tail}$. Due to the filtering impact of the LC tank, only the fundamental component can pass through at the output terminals and higher order harmonics are significantly suppressed. Hence, the differential output voltage amplitude can be derived by taking only the fundamental component, as

$$V_A = \frac{4}{\pi} R_pI_{tail} \tag{5.33}$$

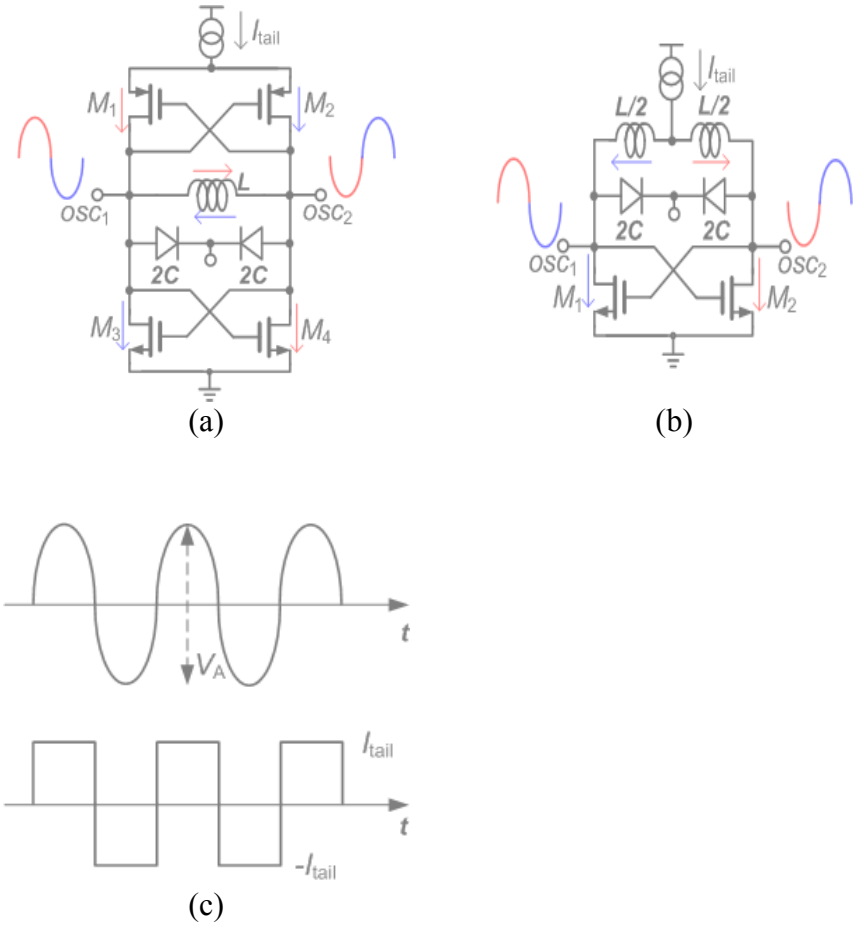


Figure 5.13 (a) Current switching in complementary LC VCO, (b) current switching in nMOS-only LC VCO, (c) output oscillation voltage and tank current waveforms.

Where V_A is the voltage peak to peak amplitude of the oscillation, R_p is the equivalent loss resistance of the tank, and I_{tail} is the bias current drawn from the current source. $\frac{2}{\pi}$ is given by the Fourier coefficient of the fundamental frequency. The

amplitude of the nMOS-only topology is half due to the fact that current is flowing half of the tank per cycle.

$$V_A = \frac{2}{\pi} R_p I_{tail} \tag{5.34}$$

This means that the complementary topology has an intrinsic 6 dB better phase noise for the same current if the amplitude is current-limited, as can be calculated from Eq. (5.30). In the voltage-limited region, the amplitude of the complementary VCO is limited by the power supply voltage V_{DD}, while the amplitude of the nMOS-only (pMOS-only) topology is limited by the V_{GS} of the nMOS transistor.

From calculation results shown by Fig. 5.12, it can be concluded that if the power supply voltage is sufficiently high, the complementary VCO presents the best power efficient solution for a comparable good phase noise. When the power supply voltage is low, i.e. lower than 1.8 V, nMOS-only topology can achieve lower phase noise at the expense of the higher current.

5.5.3 $1/f^3$ Phase Noise Mechanisms and Minimization

Compared to bipolar transistors, CMOS transistors generate more flicker noise, which in oscillators is upconverted to $1/f^3$ shaped phase noise close to the carrier. Consequently, the $1/f^3$ phase noise is higher in CMOS VCO compared to other processes and can become an issue. Flicker noise upconversion determines the phase

noise of oscillators at small offset frequencies. For a well designed oscillator used in a PLL frequency synthesizer, its $1/f^3$ corner frequency should be below the lower frequency of the PLL's bandwidth, and hence the noise can be low-pass filtered and does not appear at the output of the synthesizer. However, when the oscillator is not carefully designed, flicker noise can deteriorate the phase noise at higher offset frequencies. For instance, in communication systems, $1/f^3$ corner should be lower than 600 kHz [70].

The mechanism of flicker noise upconversion can be explained as follows [65]. When a VCO circuit is unbalanced, an oscillation appears at the common mode node of the current source at twice the oscillator frequency, ω_0, because the current source is pulled every time one of the CMOS transistors switches on while the other is off. Through channel length modulation, the noise of the tail current source is upconverted to $2\omega_0$. The upconverted noise enters the LC-tank and is mixed with the fundamental frequency, resulting in phase noise sidebands at the oscillator frequency and the 3rd harmonic. Therefore, to minimize the upconversion of flicker noise from the tail current source, balance must be preserved, meaning that all even harmonics must be suppressed. Odd harmonics have little importance for flicker noise upconversion because they do not affect the symmetry of the voltage oscillation across the LC tank obviously

Flicker noise from the tail current source is the main contributor to $1/f^3$ phase noise. The CMOS Gm transistor functions as current switching during steady state oscillation, and therefore its contribution to noise is small during the steady state oscillation. Flicker noise is a sort of correlated noise and can only exist in nonlinear time

variant systems. When transistors are ideally switched (on and off), all initial condition determined transition and consequently the flicker noise is removed [71]. In reality, the switching is unfortunately not ideal, a small amount of the Gm CMOS transistor flicker noise in also upconverted.

Another $1/f^3$ phase noise mechanism, which in fact doest not originate from $1/f$ noise, is parametric noise [72], such as nonlinearity of the varactors. Since the large sinusoidal VCO signal changes the varactor capacitance within one oscillation period, it also affects the instantaneous oscillation frequency while the steady state oscillation frequency remains the same. Due to the strong swing of the signal across the varcator, the capacitance changes $C_0(t) = C_0 + C(t)$ and thus the frequency changes $f_0(t) = f_0 + \Delta f(t)$ in which $\Delta f(t)$ is noise on the frequency. This noise usually has a flicker noise-like power spectral density. An increase in capacitance means a decrease in frequency, and this resultant frequency change behaves as noise around the oscillation frequency. This noise is not caused by noise but by the nonlinearity of the varactor. As a result, this kind of parametric noise merges with the flicker noise of the bias current source. The parametric noise and its relative contribution to $1/f^3$ noise are hard to predict and model by straightforward equations such that can only minimize by complicated simulations using software.

5.5.4 Figure of Merit (FOM) of VCO

Figure of Merit (FOM) [73] of VCO, given by Eq. (5.35), is commonly used as a means to evaluate the overall performance of a VCO. The higher the value of FOM, the better the VCO design.

$$FOM = -L\{\Delta\omega\} + 10\log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{P}\right] \tag{5.35}$$

Where ω_0 is the oscillation frequency of the VCO, $\Delta\omega$ is the offset, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$ and P is the power consumption in mW. The FOM normalizes the phase noise to oscillation frequency and offset frequency and indicates how efficiently the consumed power is used to achieve the given phase noise performance. FOM values of fully integrated VCOs in latest CMOS processes are normally higher than 170. Only VCOs with an external inductor, un-commercial techniques, such as customized metal layer thickness [74], or bias current source filtering [75] are able to reach FOM higher than 190.

Though commonly used to compare different VCOs, it may be noted that FOM is actually mislead two important aspects associating CMOS VCO design [76].

Firstly, FOM favors high-frequency VCO design in the latest CMOS processes due to the fact that high Q inductors are easier to implement at higher frequencies and hence enable lower phase noise of the VCO, described by Eq (5.31). Modern technologies have a high substrate resistance and multiple metal layers with a thick top

metal. Thus, engineers can easily design a high Q monolithic inductor such that the $Q = \omega L / R$ keeps increasing with frequency up to a certain frequency which is determined by the self-resonance frequency. In addition, the small inductor leads to a small DC series resistance, and small diameter of the inductor brings a small substrate loss at high frequencies because of small coupling effect [41]. It is found that the limiting factor in high-frequency VCO design, such as 40 GHz, is in fact the low Q of implemented varactor, e.g., less than 20[77].

Secondly, the FOM of Eq. (5.35) relates phase noise and power consumption, but ignores the tuning range of the VCO specification [78]. Nevertheless, the tuning is related to power and phase noise directly. A high frequency tuning range at low power supply voltage requires a high VCO gain, where gain is given in Eq. (5.18), which makes the VCO much more sensitive to voltage induced phase noise. At other hand, the extra tuning devices to enlarge the tuning range will further degrade the noise performance due to their non-zero resistance. Obviously, wide tuning range and low phase noise are contradictory demands for a given power consumption, Thus, it is more applicable to take tuning range into account with other most important VCO specifications, i.e. phase noise, frequency and power efficient [76].

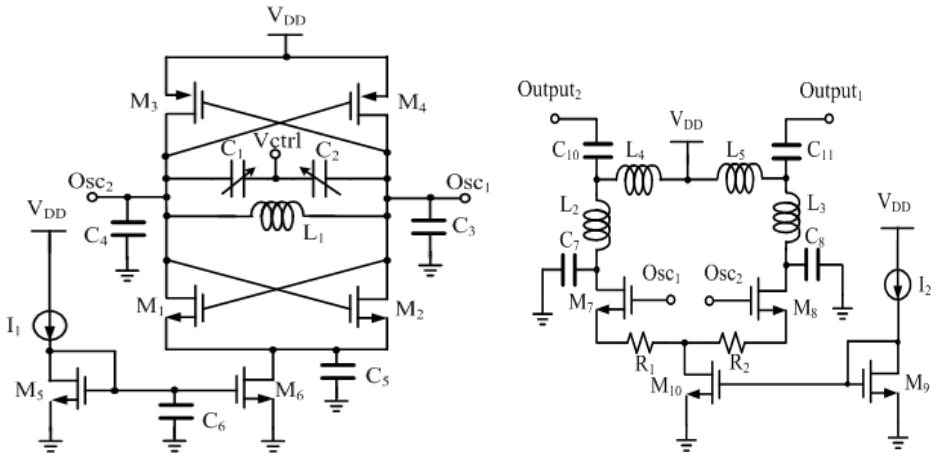
5.6 Complementary LC VCO Design

Differential LC VCO has better phase noise and less harmonic distortion than single-ended VCO, so that can bring a stable frequency source with high spectrum

purity. Complementary LC VCO is a better choice for the proposed Time-gated Carrier-based UWB transmitter in terms of good phase noise and small current consumption when the VDD of the transmitter is 1.8 V, as shown in figure 5.12. Another advantage of a complementary LC VCO is that it provides the largest tuning frequency range for a given LC tank [65] as the AC current goes through the entire tank inductor, resulting in broadband multiple carriers generated by a single VCO circuitry.

5.6.1 Design Strategy

The design goal of the Complementary LC VCO is to achieve the largest tuning frequency range and good phase noise by a minimum current consumption at 5.8 GHz. Figure 5.14 shows the topologies of the core VCO with an output buffer, where the buffer drives a pair of 50 Ohm loads, e.g. measurement equipments and SPST switch, without any impact on the tuning range and phase noise of the VCO. The tank of the VCO consists of an integrated high quality inductor, L_1, and a varactor pair, C_1 and C_2. A cross-coupled nMOS pair, M_1 and M_2, combines with a cross-coupled pMOS pair, M_3 and M_4, to form a positive feedback network and sustain the oscillations. The bias current, I_{tail}, is mainly determined by the current mirror comprises of M_5 and M_6.



(a) (b)

Figure 5.14 Topologies of LC VCO and output buffer. (a) Complementary LC VCO circuitry, (b) differential output buffer.

Though there are 6 transistors and a LC tank needs to be successfully designed, and since all the parameters of those are interrelated to affect the overall performance of the VCO, it is apparent that the design requires a high-quality factor LC tank, where the loss of the tank is mainly caused by the integrated spiral inductor, L_1, at 5.8 GHz, due to the fact that the losses in the tank are the dominant factor of the phase noise, as discussed in previous section. Moreover, the four cross-coupled transistors need to be optimized with the bias current to reach the optimal operating point, shown in figure

5.12 by "Δ" on the dashed curve. Finally, the flicker noise upconversion from the current bias transistor, M_6, needs to be minimized.

5.6.2 Design Optimization

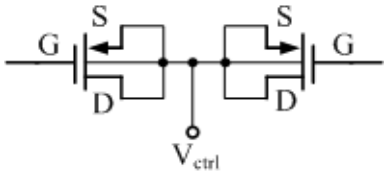


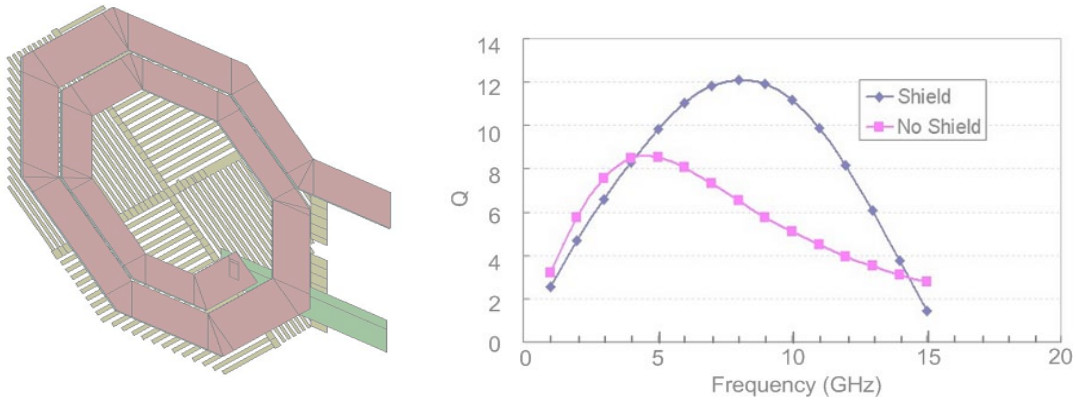
Figure 5.15 Varactor pair.

The varactors, C_1 and C_2 in Fig. 5.14 (a), are implemented by a pair of pMOS transistors with source, drain and bulk connected, as shown in Fig. 5.15. The capacitance of each varactor is determined by the DC voltage drop between the gate and bulk (connected with V_{ctrl}), where the DC bias voltage V_{gs} of the gate is kept constant by the operating points of the VCO core circuitry. And thus changing the V_{crtl} varies the capacitance of the tank, resulting in a tuning of oscillation frequency.

In the circuitry realization, the largest size of varactor was chosen for the largest tuning range of the capacitance, C_{max}-C_{min}. The bulks of the two PFET are connected with the DC control voltage, V_{ctrl}, and the gates are connected with the strong oscillation nodes (Osc_1 and Osc_2 in Fig. 5.14). Though the same capacitance can be reached by a

reverse connection (i.e., gate connecting to V_{ctrl} instead of drain), it causes much loss when a strong RF voltage oscillates on the bulk, which is the VCO's output, because of its conductive substrate, and hence the oscillation amplitudes would be lower and the phase noise would be worse due to the loss of the varactor in the tank. Since the physical loss is associated with the bulk, it is called "dirty node". Connecting the "dirty node" of the two identical pFETs as shown in Fig. 5.15, the feed through of balanced differential oscillation voltages combine out of phase at the nodes of the bulks and cancel each other so that the "dirty node" is "clean" at RF frequencies.

The bulk-gated PFETs have a high quality factor at 5 GHz, $Q_C > 30$ [75].



(a) (b)

Figure 5.16 (a) Tank inductor with PGS, (b) calculated quality factor of the inductor.

A high quality factor integrated spiral inductor is designed for the parallel LC tank. Fig. 5.16 (a) shows the layout of the octagonal spiral inductor on the top thick metallization layer with a PGS on poly-silicon layer. The track width, spacing and diameter were optimized in such a way that the spiral without shield has a peak Q_L (around 8.3) at 5 GHz, as in Fig. 5.16 (b). The Q_L of the inductor with PGS is boosted to over 10 from 5. 8 GHz to 11 GHz due to reduction of electrical loss in the substrate. The extra capacitance caused by the PGS lowers the self-resonance frequency of the inductor to some extent, but the frequency is kept 3 times higher than the interested band.

VCO bias transistor, M_6 in Fig. 5.14 (a), was chosen with a very large size, 0.75/500 (L/W in μm), for little flicker noise. A current ratio of 10 is achieved by sizing the nMOS transistor M_5 as 0.75/50 μm. A large capacitor, C_5, is connected with the drain of M_6 to provide an AC short of the common mode current ($2\omega_0$) to the ground so that the even harmonics is blocked from injecting into the LC tank and hence minimize the noise upconversion.

The nMOS cross-coupled amplifier pairs, M_1 and M_2, were identically sized for good differential balance, the pMOS pairs, M_3 and M_4, were particularly sized such that $G_{Mp} = G_{Mn} = 3/2R_p$ at 5.8 GHz, where G_{Mp} is the transconductance of the pMOS and G_{Mn} is the transconductance of the nMOS, resulting in a symmetric oscillation in which the positive peak and negative peak amplitudes of the voltage are identical. These differential symmetric balanced oscillations inject less noise into the LC tank from the

amplifier transistors than any un-balance oscillations [65]. The combination of the G_M by the nMOS pairs, and pMOS pairs were 3 times the loss in the LC tank in order to sustain a stable oscillation.

The bias current, I_{tail}, was optimized along with sizing the cross-coupled nMOS and pMOS pairs to reach the optimal operating point, as show in Fig. 5.12 by the "Δ" on the dashed line. Unwisely increasing I_{tail} over the optimal value results in stronger oscillation amplitude, but worse phase noise.

Differential oscillation outputs, Osc_1 and Osc_2 in Fig. 5.14, are DC coupled to the input ports of the differential buffer, the gates of the M_7 and M_8, respectively, and shown in Fig. 5.14 (b). In order to kept the quality factor of the LC tank unaffected by the low input impedance of the buffer, which is actually a differential common source amplifiers pair, two on-chip MIM (Metal-Insulator-Metal) capacitors, C_3 and C_4, are parallel with the input ports of the buffer, and thus the loading of the VCO is dominated by these capacitances, which are high impedances at 5.8 GHz.

The VCO and buffer were designed by TSMC 0.25 μm CMOS process [79]. Table 5.1 lists the parameters of the designed CMOS complementary LC VCO.

TABLE 5.1
SUMMARY OF THE CMOS VCO'S DESIGNED PARAMETERS

Circuit Element	Element Value
M_1, M_2	120-μm gate width 0.25-μm gate length
M_3, M_4	200-μm gate width 0.25-μm gate length
M_5	50-μm gate width 0.75-μm gate length
M_6	500-μm gate width 0.75-μm gate length
C_1, C_2	PMOS, 180-μm gate width 0.75-μm gate length
L_1	1 nH
C_3, C_4	MIM, 200 fF
C_5, C_6	MIM, 20 pF
V_{DD}	1.8 V
I_{tail}	4 mA

After optimizations, the partitions of each noise contributor to the phase noise at 1 MHz offset@5.8 GHz oscillation are summarized by Table 5.2.

TABLE 5.2
SPECTRERF SIMULATIONS ON THE NOISE CONTRIBUTIONS. 5.8 GHZ CARRIER FREQUENCY WITH A BIAS CURRENT OF 4 MA (IN V^2_{rms} / Hz).

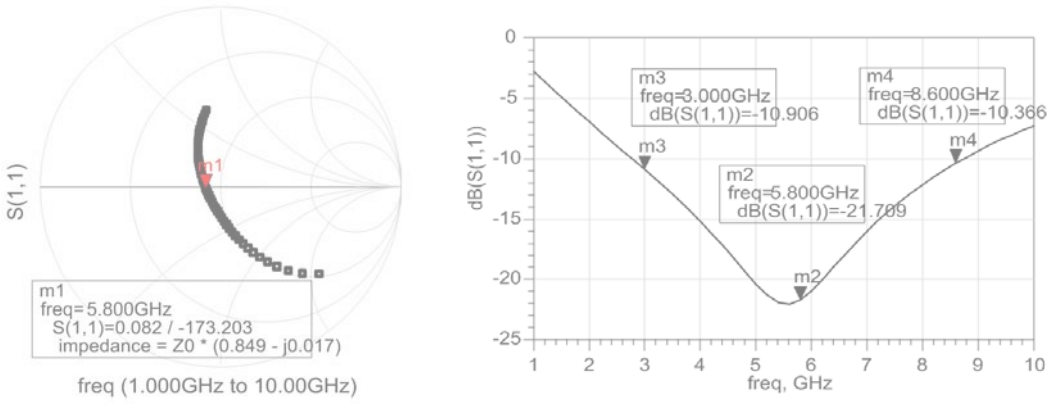
Circuit Element	Noise Contributed	Percentage
R_p	$6.05 \cdot 10^{-15}$	42.9%
M_1, M_2	$2.98 \cdot 10^{-15}$	21.2%
M_3, M_4	$5.06 \cdot 10^{-15}$	35.9%
M_6	N/A	N/A
V_A	980 $mV_{Diff\text{-}Peak}$	
$L\{1MHz\}$	-119 dBc/Hz	

The differential common source takes very little current and mainly attenuates the strong oscillation input swings to certain level output to drive the SPST switch, so that the output power does not exceed the FCC requirement. To this end, the M_7 and M_8, shown in Fig. 5.14 (b), are chosen small gate width for small G_M. 50 Ohm impedance matching at 5.8 GHz and is achieved by the matching networks comprising of the MIM capacitors, C_7 and C_8, and integrated inductors, L_2, L_3, L_4 and L_5. Source degeneration resistors, R_1 and R_2, help to keep the oscillation undistorted at output port when there is a strong oscillation at the input port of the buffer.

Table 5.3 lists the parameters of the CMOS buffer and Fig 5.17 shows the output matching of each output port to 50-Ohm impedance.

TABLE 5.3
SUMMARY OF THE CMOS BUFFER'S DESIGNED PARAMETERS

Circuit Element	Element Value
M_7, M_8	20-μm gate width 0.25-μm gate length
M_9	50-μm gate width 0.75-μm gate length
M_{10}	2500-μm gate width 0.75-μm gate length
R_1, R_2	Poly resistor 12 Ohm
C_7, C_8	MIM, 120 fF
L_2, L_3	2.3 nH
L_4, L_5	3.7 nH
C_6, C_{10}	MIM, 2 pF
V_{DD}	1.8 V
I_{tail}	tunable



(a) (b)

Figure 5.17 (a) Output matching on Z-chart, (b) calculated return loss at the output port of the buffer.

Fig. 5.18 shows the microphotograph of the integrated LC VCO with output buffer, where one of the outputs of the buffer is terminated by an on-chip 50 Ohm resistor. The circuitry in Fig. 5.18 was measured to characterize the performance of the VCO, using 50 Ohm impedance microwave equipments.

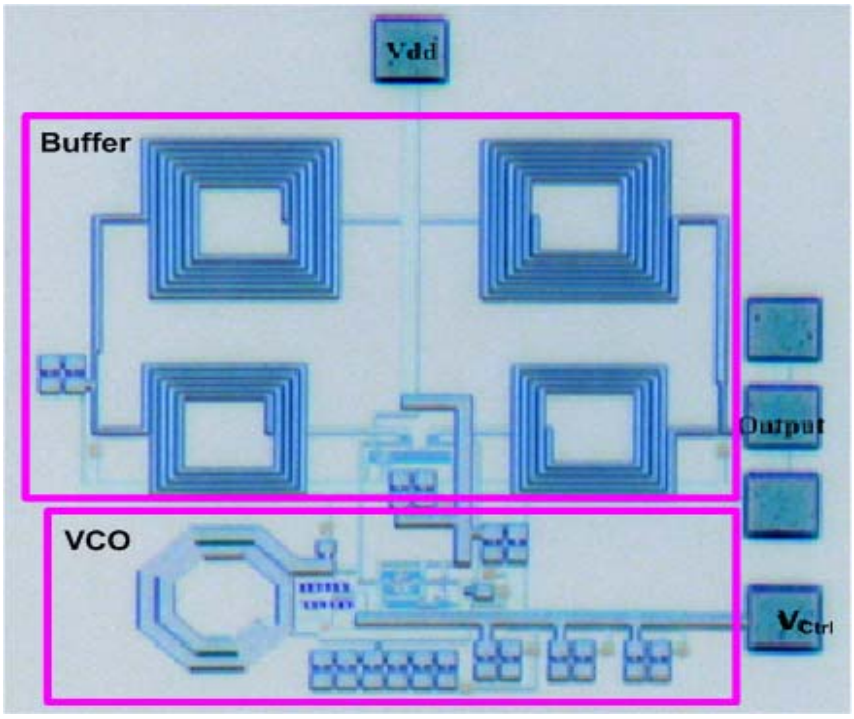


Figure 5.18 Microphotograph of the complementary LC VCO and buffer. The die area without pads is 320 μm by 300 μm.

5.6.3 Measurements

To measure the phase noise of the LC VCO alone, no PLL was implemented to lock the VCO to any external frequency references. The output spectrum of the free running VCO was captured by a spectrum analyzer which was set up with very low visional bandwidth (VBW), VBW = 100 KHz. By this setup, the spectrum analyzer brought a small number of measurement averages of instantaneous spectrum, thus avoiding the frequency jittering measurement problems when the VCO was not locked to an external frequency stable reference source, and it was able to display an accurate

instantaneous spectrum of the free running VCO. On wafer measurements was performed on the circuit shown in Fig. 5.18, and a 20 dB external high linear amplifier was used to make the output spectrum of the buffer much higher than the noise floor of the spectrum analyzer. The V_{DD} and V_{ctrl} were connected to two DC power suppliers directly through short cables. Fig. 5.19 records the output spectrum.

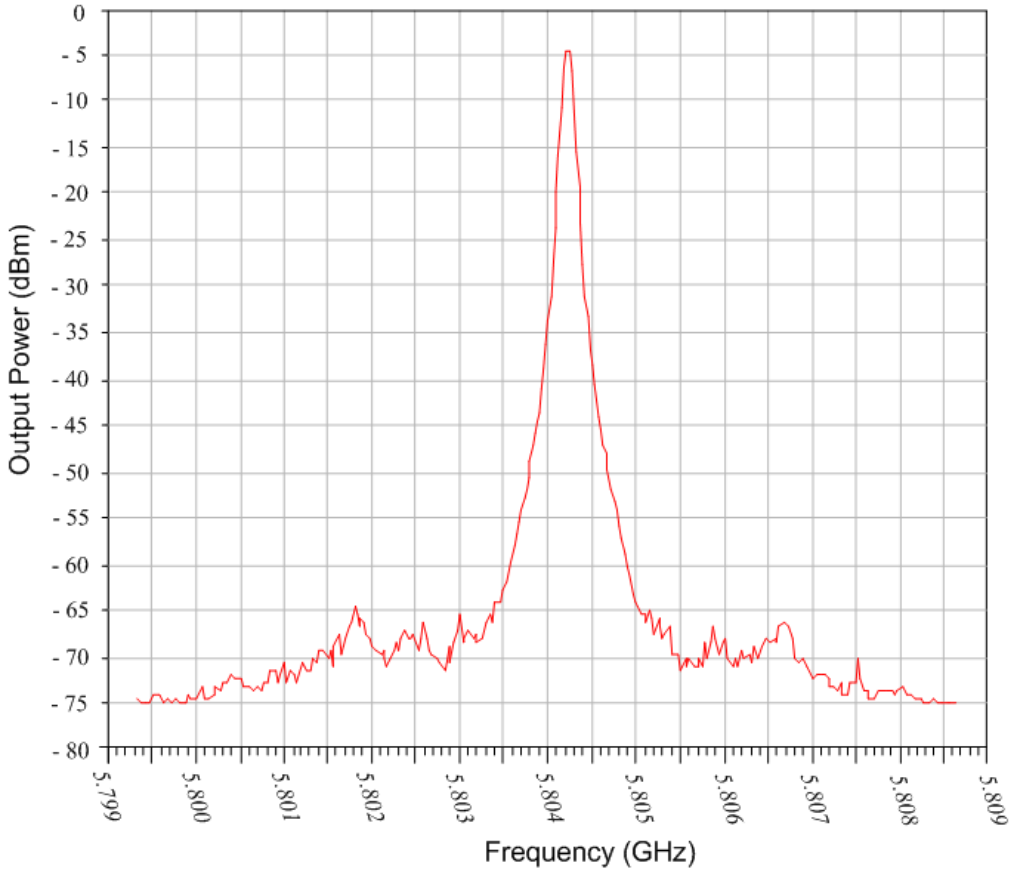


Figure 5.19 Output sepectrum with VDD = 1.8 V, Vctrl =1.75 V. The Resolution Band Width of the spectrum was set as 100 KHz.

Fig. 5.20 shows the measured phase noise at 5.8 GHz, where the phase noise at 1 MHz is –117 dBc/Hz, 2 dB lower than the calculation. The $1/f^3$ corner frequency is around 500 KHz offset. Fig. 5.21 presents the measured tuning range versus control voltage. It is shown that the center frequency of the VCO is 5.2 GHz, 600 MHz lower than the simulation. The reason would be that extra inductances caused by the connecting tracks between the spiral inductor and two varactors in the LC tank did not extracted precisely by Cadence at high frequencies, but physically exist in the circuitry, resulting in a lower resonance frequency than expected. This Cadence-related issue may be overcome by complicated EM simulations or by giving 10% margin to the Cadence calculation. The measured tuning range is 25% of the center frequency, 4.6 to 5.9 GHz for a tuning voltage range of 0 – 2 V.

Based on (5.35), the FOM of measured VCO is 183.7, among the best reported CMOS VCO. Meanwhile, the 25 % tuning range is among the widest reported VCOs.

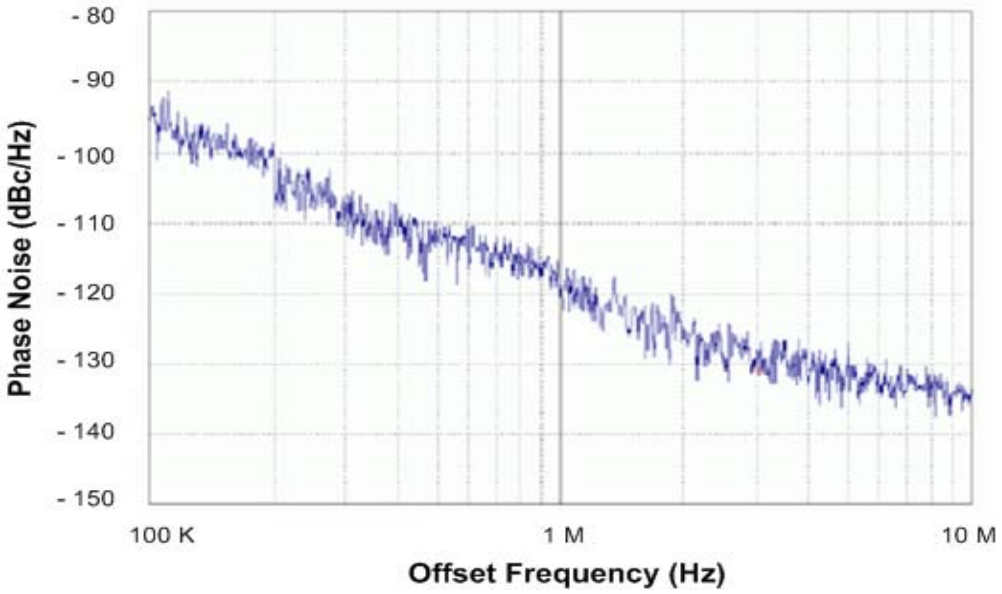


Figure 5.20 Measured phase noise at 5.8 GHz.

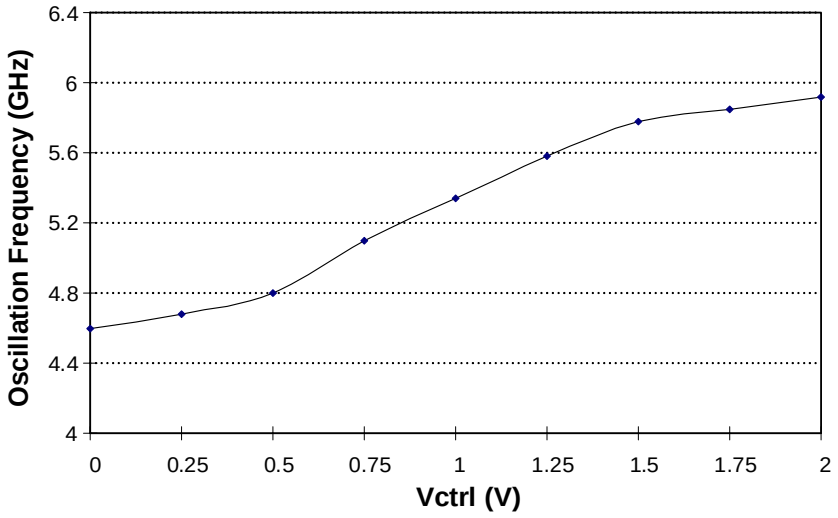


Figure 5.21 Measured VCO tuning range versus control voltage.

CHAPTER VI

SUMMARY AND CONCLUSION

UWB has experienced an emerging growth in the last few years, and this trend is expected to continue. In this dissertation, efforts were made to implement novel fully integrated topologies and structures both on RF blocks and RF front end for UWB applications using standard CMOS processes.

As for short rang high-date rate application, the competing standards of DS-UWB and MB-OFDM had occurred as the result of a failure to create a single UWB standard under the auspices of the IEEE 802.15.3a task group. In January 2006, the IEEE announced that the 802.15.3a task group was abandoning its effort to create a single, high-data rate UWB standard. However, the key DS-UWB advocator, Freescale, was ultimately unable to deliver its UWB silicon to market at a reasonable cost, and so the company abandoned its UWB effort. That left the other standard, MB-OFDM, as the sole UWB solution on the market.

In addition, much of the last few years have been spent getting the necessary worldwide regulatory solutions in place in order to bring UWB to market. It is apparent that most countries outside of the US intend to allow use of some fractions of the frequency span of FCC defined carriers, but with more restrictive radiation regulations. For instance, UWB is allowed to use between 3.4 and 4.8GHz of the frequency band in Japan, where detect and avoid (DAA) is required between 3.4 and 4.2GHz and not necessary between 4.2 and 4.8GHz. In the high bands, UWB is allowed between 7.25

and 10.25GHz. Figure 6.1 shows the regulated radiation mask in Japan, where the band spurious radiation is required lower than 30 dBc.

Worldwide frequency regulation in other countries present difficulties globally for broad adoption and marketing of DS-UWB and impulse UWB, since they take the full 7.5 GHz spectrum span instantaneously. Therefore, it shows the practical importance the development of the career-based UWB for various wireless applications is of practical importance. Therefore, locating, identifying, and communicating, where the carrier and bandwidth can be adjusted to meet different countries' specific regulations is of tantamount importance.

Moreover, new circuitry and architectures are actively studied, using silicon-based CMOS technology, in this dissertation in order to achieve low cost and highly integrated UWB systems. A case is advanced to provide prove that the CMOS technique can decrease the system cost by integrating the RF blocks on chip, thus decreasing the number of board-level components without sacrificing performance.

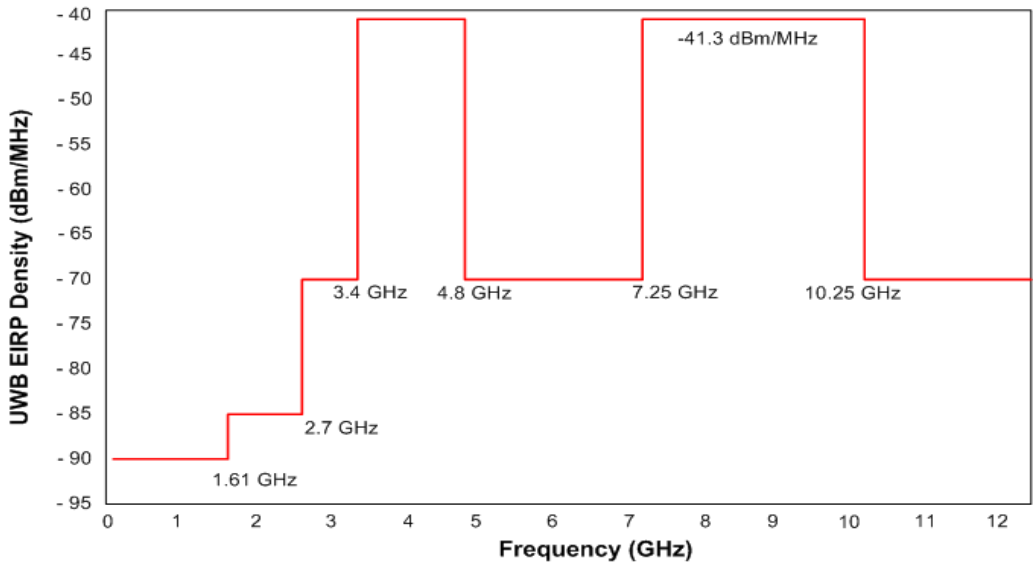


Figure 6.1 UWB EIRP frequency mask regulation by Japan

In Chapter II of this dissertation, the switching devices by GaAs MESFETs and silicon based MOSFETs are compared. Though high performance and high frequency, GaAs MESFETs do not enable a low cost, small form factor solution. Resistive floating the substrate of the MOSFET improves the performance of MOSFET as a switch in broadband applications. It allows negative voltages to be applied at the body of the MOSFET without causing any reliability concern. In this chapter, the scientific case for the feasibility of using synthetic transmission line concept to initiate design of broadband CMOS switches is presented and proposed.

In Chapter III of this dissertation, an ultra broadband transmit-receive switch design is presented to illustrate the benefits of absorbing the parasitic capacitances of

MOSFETs by synthetic transmission line technique. Measured results show that performance of the switch is comparable to its GaAs counterparts in the market. The switch shows an insertion loss less than 0.7 dB within the UWB spectrum span and less than 1.5 dB up to 15 GHz, which is the best among the reported CMOS switches in the literature. Since one of the integrated coplanar inductors can be replaced by bonding wires, the design also provides a practical on-chip alternative as the first integrated block within the chip boundary.

In Chapter IV of this dissertation, a detailed study of a new method to realize the time-gated carrier-based UWB in CMOS is presented and is enhanced by the use of a model of a tunable transmitter. The multiplying function of RF carrier and baseband impulses is firstly demonstrated by using an ultra broad band high performance SPST switch designed in CMOS. The invention of the physical mechanism under discussion in this dissertation paves the way that manufacturers can meet the strict requirements of the transmitter. Based on the concept of the synthetic transmission line with the SPTS switch explored in this dissertation, the SPST switch has been proven to exhibit a very broadband frequency span with less than 1.5 dB measured insertion loss. The multiple reflections at input and output ports enable the switch to have an extremely high isolation, greater than 45 dB from measurements, within the UWB 7.5 GHz frequency span.

In Chapter V of the dissertation, focusing on study of the utilization of low phase noise, and low jittering integrated LC VCO in CMOS, the design of a high performance integrated VCO and tunable buffer, which are key blocks of the proposed UWB

transmitter, is presented. Various differential LC VCO topologies are analyzed in terms of phase noises, output swings and current consumptions. Optimizing progresses has thus far entailed the design of an integrated Complementary LC VCO. The measured FOM of the VCO is among the best-reported CMOS VCOs in the literature. The tunable output buffer brings a large dynamic range and broadband driven capabilities, enabling the transmitter to be used by broadcasters in compliance with FCC radiation regulations.

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VITA

Yalin Jin received his B. S. degree in 1995 from Xi'an Jiaotong University, Xi'an, China, and M. S. degree in 1998 from the Chinese Academy of Sciences, Beijing, China, both in Electrical Engineering. Prior to his study with Dr. Cam Nguyen for his Ph.D. degree, he worked as a RF design engineer with XinWei Telecom, Beijing, China, from 1998 to 2001 on SCDMA systems and as a senior RF design engineer with Motorola Electronics (China), Beijing, China, on GSM mobile phones. From May 2006 to December 2006 and from May 2007 to August 2007 he worked as a RFIC designer intern with Alereon Inc. in Austin, Texas, designing the first worldwide all-band MB-OFDM UWB transceiver. His research interests are high frequency radio frequency integrated circuit and system design.

He can be reached through Professor Cam Nguyen at the Department of Electrical and Computer Engineering of Texas A&M University, College Station, Texas 77843-3128.