HIGH PERFORMANCE BUILDING BLOCKS FOR WIRELESS RECEIVER: MULTI-STAGE AMPLIFIERS AND LOW NOISE AMPLIFIERS

A Dissertation

by

XIAOHUA FAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	César O. Malavé
	Weiping Shi
	José Silva-Martínez
Head of Department,	Costas N. Georghiades

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ABSTRACT

High Performance Building Blocks for Wireless Receiver:

Multi-Stage Amplifiers and Low Noise Amplifiers. (December 2007)

Xiaohua Fan, B.S., Tsinghua University;

M.S., Chinese Academy of Sciences

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Different wireless communication systems utilizing different standards and for multiple applications have penetrated the normal people's life, such as Cell phone, Wireless LAN, Bluetooth, Ultra wideband (UWB) and WiMAX systems. The wireless receiver normally serves as the primary part of the system, which heavily influences the system performance. This research concentrates on the designs of several important blocks of the receiver; multi-stage amplifier and low noise amplifier.

Two novel multi-stage amplifier typologies are proposed to improve the bandwidth and reduce the silicon area for the application where a large capacitive load exists. They were designed using AMI 0.5 μm CMOS technology. The simulation and measurement results show they have the best Figure-of-Merits (FOMs) in terms of small signal and large signal performances, with 4.6MHz and 9MHz bandwidth while consuming 0.38mW and 0.4mW power from a 2V power supply.

Two Low Noise Amplifiers (LNAs) are proposed, with one designed for narrowband application and the other for UWB application. A noise reduction technique is proposed for the differential cascode Common Source LNA (CS-LNA), which reduces the LNA Noise Figure (NF), increases the LNA gain, and improves the LNA linearity. At the same time, a novel Common Gate LNA (CG-LNA) is proposed for UWB application, which has better linearity, lower power consumption, and reasonable noise performance.

Finally a novel practical current injection built-in-test (BIT) technique is proposed for the RF Front-end circuits. If the off-chip component Lg and Rs values are well controlled, the proposed technique can estimate the voltage gain of the LNA with less than 1dB (8%) error.

To my parents, sister and beloved wife Xiaoyan.

In memory of my grandfather.

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My experience in the Analog and Mixed Signal Center was both an important and enjoyable part of my life. At Texas A&M University (TAMU), I learned a great deal about analog circuit design, meeting many nice professors, while making many good friends. I will always remember the time that I experienced there, no matter where I will be in the future.

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TABLE OF CONTENTS

Page

CHAPTER Page

CHAPTER Page

CHAPTER Page

LIST OF FIGURES

Page

Page

Page

Page

Page

Page

Page

Page

Page

LIST OF TABLES

Page

Page

CHAPTER I

INTRODUCTION

The huge demand for the wireless devices in the market place has driven research in wireless communication systems and circuits for the last one and a half decades. Wireless applications reduce the distance between people，simplifying the world by removing most of the wires. Voice and video are transmitted through different wireless applications, including cell phone (GSM and CDMA), global positioning systems (GPS), wireless local area networks (WLAN), and data communication systems (Bluetooth and Ultra-wideband). The wireless receiver is an important part of the wireless systems. The basic direct conversion wireless receiver as an example is shown in Fig. 1.1 [1]-[2]. The incoming signal is first amplified by the Low Noise Amplifier (LNA) and then down converted to baseband by the Mixer. The signal channel is selected by the Phase Locked Loop (PLL). The low pass filter (LPF) and variable gain amplifier (VGA) processes the baseband signal in the analog domain to remove the unwanted frequency signal and adjust the signal level. The Analog-to-Digital converter (ADC) converts the analog baseband signal to a digital signal, then processed by the digital signal processing (DSP) circuits. The power management part provides the accurate voltage and current references for all the circuits. The multistage amplifiers are an important building block of base band signal processing and of the power management circuits. Built-In-Test (BIT) loopback technique used to diagnose the error in the transceiver.

This dissertation follows the style of *IEEE Journal of Solid State Circuits.*

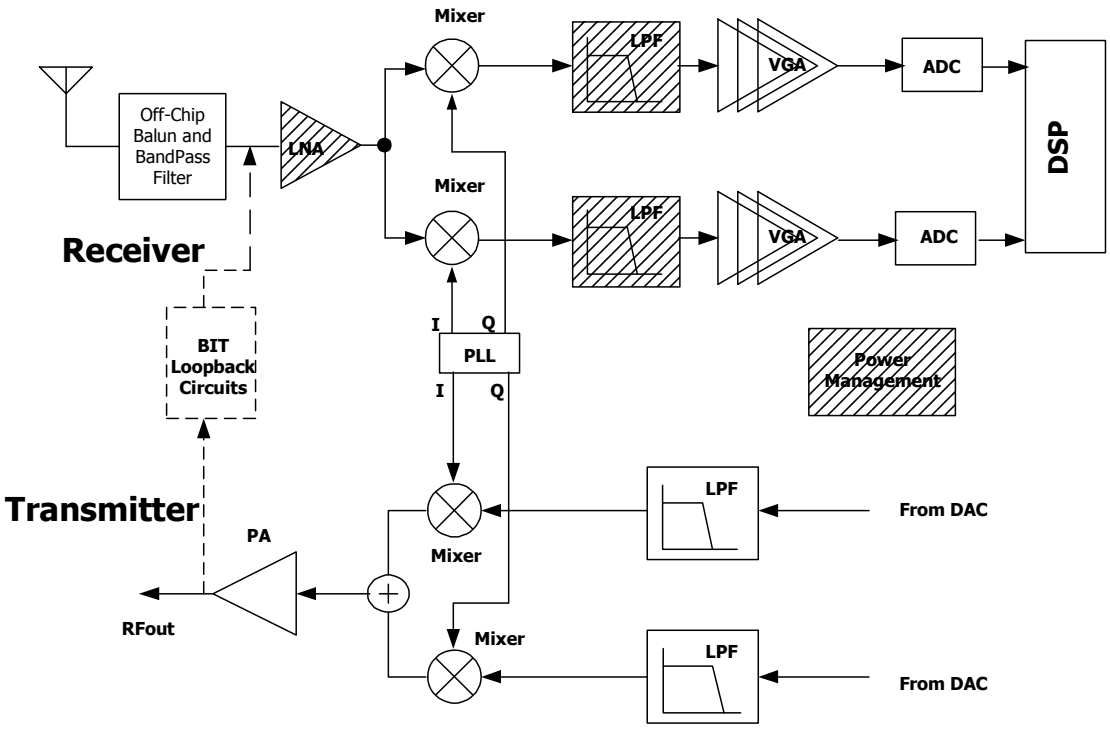


Fig. 1.1 Block diagram of the basic direct conversion transceiver

1.1 Motivation

Wireless communication systems are rapidly developing due to the fast growing demands for the wireless consumer electronic devices. Early wireless receiver utilized GaAs, SiGe bipolar and CMOS RF and baseband circuits. The feature size of the CMOS device has continued to decrease while the operating frequency of the CMOS device increases. Although from a cost and easy integration point of view, CMOS designs become more and more attractive, the CMOS designs still face many challenges in practice. Lower power consumption, smaller silicon area and higher performances are always needed for wireless devices. The complexity of the transceiver has grown considerably. Testing of

integrated transceivers has become a difficult and expensive task. For the traditional RF production test approach, expensive automatic test equipment (ATE) and long test times are required. The cheaper and faster testing method is desired without sacrificing the testing accuracy.

In this research, several building blocks for the integrated transceiver are designed as shown in Fig.1.1 with the dashed diagrams.

The LNA works in the highest frequency of the wireless receiver and is often directly connected to the antenna as shown in Fig.1.1. It needs to provide power amplification, while contributing less noise and providing enough of a dynamic region. According to the operating frequency bandwidth, the LNAs can be divided into Narrowband LNA and Wideband LNA. In this research, two novel LNAs are proposed, analyzed and designed for both applications. For the Narrowband LNA, a novel approach to reduce the noise and improve the linearity was proposed for a differential cascode common source LNA (CS-LNA). For the Wideband LNA, a novel Common-Gate LNA is proposed, which has lower power consumption and higher linearity and can be used for the Ultra-wideband application.

The analog circuits normally need accurate, temperature independent voltage/current supply and references. Multistage amplifiers are widely used in active RC filters and in the power management circuits, where high gain, fast settling times, and small area are desired. Two multistage amplifiers are proposed in this research using a single Miller capacitor approach, which is suitable for the applications with large capacitive load. They dramatically reduce the area and increases the bandwidth compared with the existing topologies.

To reduce the testing cost and testing time, different Built-In Testing (BIT) methods are proposed in the literatures. In this work, a current based BIT method is proposed for RF Front-Ends. Different from the typical voltage based BIT method. A current signal is injected into the gate of the LNA. Two power detectors are used to exam the input current and the out voltage. Using the proposed testing technique, the LNA gain can be accurately estimated with less than 1dB error from the conventional LNA simulated gain even when the input network exists there.

Overall, in this research, different circuit topologies are proposed for the design and the testing of important building blocks of the wireless receivers.

1.2 Dissertation Organization

The dissertation is organized as follows. Chapter I discusses the research motivation and dissertation organization. Chapter II discusses the multi-stage amplifier design background and presents two novel amplifier structures, which are very efficient for large capacitive load applications. In Chapter III, an overview of narrowband LNA architecture and wideband LNA architecture is given. A noise reduction technique for a differential cascode narrowband LNA is proposed and analyzed in Chapter IV. Chapter VI describes the proposed low power UWB common gate LNA. A novel Built-In-Test (BIT) technique for RF Front-ends is described in Chapter VI and Chapter VII summarizes the works of this dissertation.

CHAPTER II

LOW POWER MULTI-STAGE AMPLIFIER DESIGN*

2.1 Motivation

Large demand for low-power, portable, battery-operated electronic devices [3], such as mobile phones and laptop computers, provides the impetus for further research towards achieving higher on chip integration and lower power consumption. High gain, wide bandwidth amplifiers driving large capacitive loads serve as error amplifiers in low-voltage low-drop-out (LDO) regulators [4]-[5] in portable devices as shown in Fig. 2.1 (a). V_{in} of the LDO serves as the power supply of the error amplifier. Another application of the amplifier is in low frequency active RC filters as shown in Fig. 2.1(b).

With the scaling down of device feature size and voltage, single stage cascode or telescopic amplifiers are not suitable for high gain, wide bandwidth amplifiers. A low power, low area, and frequency compensated multistage amplifier capable of driving large capacitive loads is necessary. Multistage amplifiers [6]-[18] require a robust frequency compensation scheme due to their potential closed loop stability problems. Different frequency compensation schemes have been proposed in the literatures.

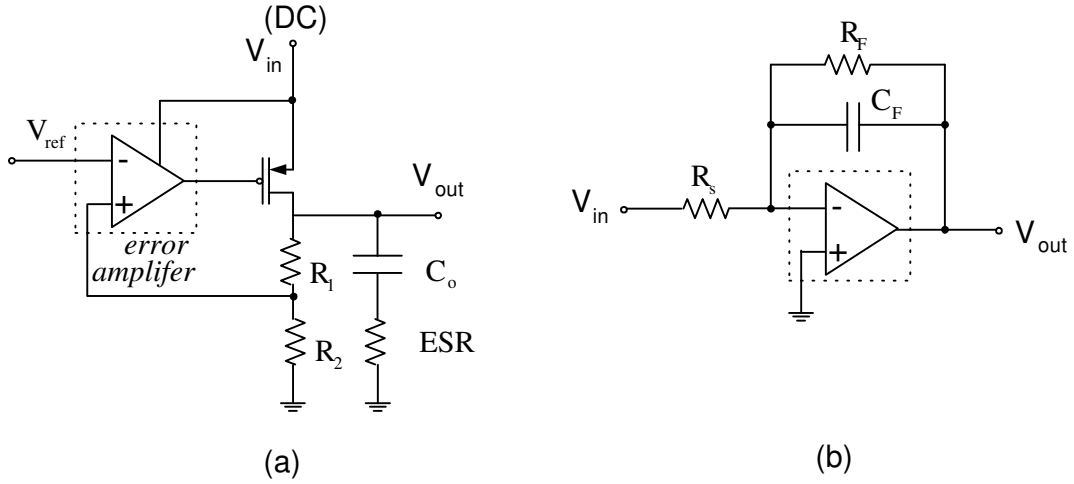


Fig. 2.1 Applications of amplifiers (a) Structure of a classical LDO (b) Active RC filter

2.2 State of the Art Amplifiers

The error amplifier in Fig. 2.1 needs to drive the large Pass transistor for the LDO regulator. It needs to provide large DC gain and bandwidth so that the LDO regulator has smaller output impedance and settling fast to the final result. Although the telescopic cascode amplifier can obtain large DC gain with only single stage topology, it needs more voltage headroom. With the advanced process, the power supply voltage keeps reducing. And thus there is not enough voltage headroom for a single stage having too many cascode transistors. The multistage amplifier distributes the DC gain through several stages and obtains the high DC gain. There are multiple poles and zeros in the multistage amplifier, which may cause the stability issues of the amplifiers used in the close loop. Different multistage amplifier topologies are proposed to stabilize the multistage amplifier in the literatures. The following discussion is a brief overview of the different proposed techniques and topologies. The

evaluations of them are aimed for the error amplifier with higher on chip integration and low-power consumption while driving large capacitive loads.

2.2.1 Nested Miller Compensation Amplifier (NMC).

Nested Miller Compensation (NMC) [6] uses two Miller Capacitors between every two poles to separate the pole locations and stabilize the amplifier. Fig. 2.2 shows the block diagram of a three stage NMC amplifier, where $Z_{oi}^{-1} = g_{oi} + sC_{pi}$.

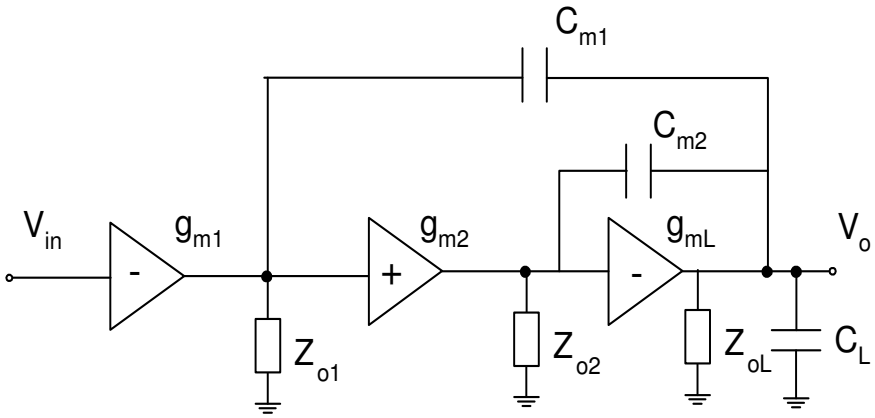


Fig. 2.2 Three stage NMC amplifier [6]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

The transconductance, output conductance, and the parasitic capacitance at the output of each stage are given by $g_{m(1,2,L)}$, $g_{o(1,2,L)}$ and $C_{p(1,2,L)}$ respectively. C_L represents the amplifier load. C_{m1} and C_{m2} are the compensation capacitors. Assuming that $g_{m(1,2,L)} >> g_{o(1,2,L)}$ and $C_{L,m_1,m_2} >> C_{P(1,2,L)}$, the transfer function of the NMC amplifier [11] is given by (2.1)

$$A_v(s) = \frac{\left(\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left(1 - s\frac{C_{m2}}{g_{mL}} - s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{\left(1 + s\frac{C_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left[1 + s\frac{C_{m2}(g_{mL} - g_{m2})}{g_{m2}g_{mL}} + s^2\frac{C_L C_{m2}}{g_{m2}g_{mL}}\right]} \tag{2.1a}$$

$$Z_{1,2} = \frac{-\frac{g_{m2}}{C_{m1}} \pm \sqrt{\frac{g_{m2}^2}{C_{ml}^2} + 4\frac{g_{m2}g_{mL}}{C_{m1}C_{m2}}}}{2} \tag{2.1b}$$

With an additional assumption of $g_{mL} >> g_{m(1,2)}$, the zeros of the transfer function can be fairly neglected and the transfer function reduces to

$$A_v(s) \cong \frac{\left(\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)}{\left(1 + s\frac{C_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left[1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_L C_{m2}}{g_{m2}g_{mL}}\right]} \tag{2.2}$$

The root locus plot of the NMC amplifier with and without the Miller compensation is shown in Fig. 2.3.

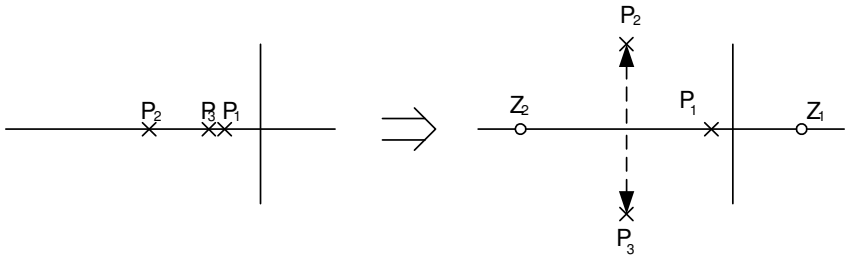


Fig. 2.3 Root locus of the NMC amplifier (a) Before connecting Cm1 and Cm2. (b) After placing Cm1 and Cm2

The DC gain is given by $A_v(0) = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$ and the stability condition (Rooth-Hurwitz) as per the separate pole approach [11] is given by $GBW \le \frac{1}{2}p_2 \le \frac{1}{4}p_3$. This implies that $\frac{g_{m1}}{C_{m1}} \le \frac{1}{2}\frac{g_{m2}}{C_{m2}} \le \frac{1}{4}\frac{g_{mL}}{C_L}$, which results in the following values for the compensation capacitors: $C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ and $C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right)C_L$.

This yields large compensation capacitors for large load capacitors. Large load capacitors limit the GBW to a great extent as $GBW = \frac{g_{m1}}{C_{m1}} = \frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$. Thus smaller compensation capacitors results in larger values of g_{mL}. However the stability of the NMC amplifier is ensured by a larger value for g_{mL} [6], which is not suitable for low-power design, especially when driving large capacitive loads.

This means that Nested Miller Compensation (NMC) amplifier requires large value Miller capacitor, which reduces the small signal responses (bandwidth) and the large signal responses (settling time and slew rate). The Miller capacitor in NMC amplifier increases proportionally with the load capacitor and hence is not suitable for higher integration. These drawbacks lead to other compensation schemes.

Observe that by placing Cm2 around gm2, the location of the zero can significantly change but the pole location can be forced to be the same.

2.2.2 Damping Factor Control Frequency Compensation Amplifier (DFCFC)

From section 2.2.1, one drawback of NMC amplifier is the large size of the compensation capacitor, which is proportionally to the very large load capacitor. The DFCFC uses a damping-factor-control (DFC) [10] block to replace the passive compensation capacitor in NMC as shown in Fig. 2.4

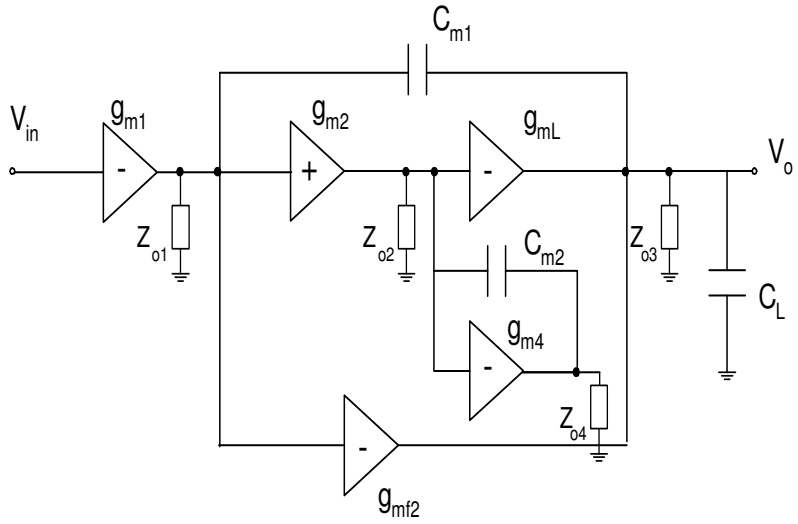


Fig. 2.4 Three stage DFCFC amplifier [10]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

The small signal frequency response of DFCFC amplifier is

$$A_v(s) \cong \frac{A_{dc}\left(1+s\frac{C_{p2}g_{mf2}-C_{m1}g_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}-s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_Lg_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}+g_{mf2}g_{m4}}\right)} \quad (2.3a)$$

$$Z_{1,2} = \frac{\frac{C_{p2}g_{mf2} - C_{m1}g_{m4}}{C_{m1}C_{p2}} \pm \sqrt{\frac{\left(C_{p2}g_{mf2} - C_{m1}g_{m4}\right)^2}{C_{m1}^2 C_{p2}^2} + 4\frac{g_{m2}g_{mL} + g_{m4}g_{mf2}}{C_{m1}C_{p2}}}}{2} \tag{2.3b}$$

Where $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}}$ and $p_{-3dB} = \frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{mL}}$.

After the stability conditions are established, the Miller capacitor becomes

$$C_{m1} = \frac{1}{\beta} \cdot \left[4\left(\frac{g_{m1}}{g_{mL}}\right) C_L \right] \tag{2.4}$$

where $\beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2}}{g_{mL}}\right)}$.

And the bandwidth of the DFCFC is

$$GBW_{DFCFC} = \frac{g_{m1}}{C_{m1}} = \beta \cdot \left[\frac{1}{4}\left(\frac{g_{mL}}{C_L}\right) \right] = \beta \cdot GBW_{NMC} \tag{2.5}$$

From (2.4) and (2.5), DFCFC reduces the Miller capacitor value and improves the bandwidth of the amplifier. For the damping control block (DFC), it is a gain stage (gm4) with high output impedance. Due to the process variation and the offset, the node voltage can be pulled up to VDD or pulled down to GND. A local feedback circuitry is needed to control the dc operating point of the node [10]. Since the zeros of DFCFC amplifier is in the higher frequencies than the poles of the amplifier, the effects from the zeros can be neglected and they will not influence the stability criteria of the amplifier much [10].

2.2.3 Active Feedback Frequency Compensation Amplifier (AFFC)

To further reduce the compensation capacitor value, the AFFC amplifier was proposed [13]. It uses active feedback and feedforward to reduce the required compensation capacitor value and improve the small and large signal performance of the amplifier, the AFFC circuit is depicted in Fig. 2.5.

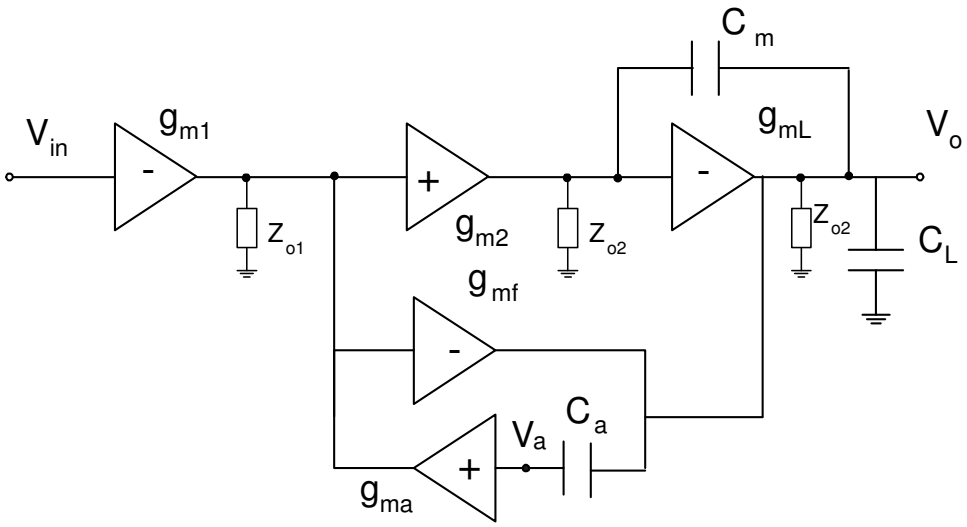


Fig. 2.5 Three stage AFFC amplifier [12]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

It uses an active capacitor to replace a passive one, resulting in smaller capacitor sizes. The effective capacitor can be roughly estimated by $C_{eff}=C_a \times g_{ma} \times r_a$, where r_a is the output impedance of the feedback stage. It also uses a high-speed block with a feed forward path to enhance the bandwidth and the transient response of the amplifier. The small signal frequency response of AFFC amplifier is

$$A_v(s) \cong \frac{A_{dc}\left(1+s\frac{C_a}{g_{ma}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_1 g_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_1 C_L}{g_{ma}(g_{mf}-g_{m2})}\right)} \tag{2.6}$$

where $A_{dc}=\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}}$ and $p_{-3dB}=\frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{mL}}$.

Note that (2.6) has a single real zero in contrast to previous structures. After the stability conditions are established, the Miller capacitor yields:

$$C_{m(AFFC)}=C_a=\frac{1}{N}\cdot\left[4\left(\frac{g_{m1}}{g_{mL}}\right)C_L\right]=\frac{1}{N}C_{m(NMC)} \tag{2.7}$$

where $N=\sqrt{8\left(\frac{C_L}{C_1}\right)\left[\frac{g_{m1}(g_{mf}-g_{m2})}{g_{mL}^2}\right]}$ and $g_{mf} > g_{m2}$. And the bandwidth of the AFFC is

$$GBW_{AFFC}=\frac{g_{m1}}{C_m}=\sqrt{\frac{g_{mL}(g_{mf}-g_{m2})}{2Cp_1C_L}}=N\frac{g_{m1}}{4C_{L:}}=N\cdot GBW_{NMC} \tag{2.8}$$

From (2.7) and (2.8), AFFC reduces the Miller capacitor value and improves the bandwidth of the amplifier by a factor N. A typical value of N [12] is 10.

2.2.4 Dual Loop Parallel Compensation Amplifier (DLPC)

The DLPC uses a damping-factor-control (DFC) [14] block to replace the passive compensation capacitor in AFFC and implements two high-speed paths to extend the bandwidth and improve the transient performance. In other words, g_{ma} allows the feedback and avoids the unwanted feedforward path. Its circuit is shown in Fig. 2.6.

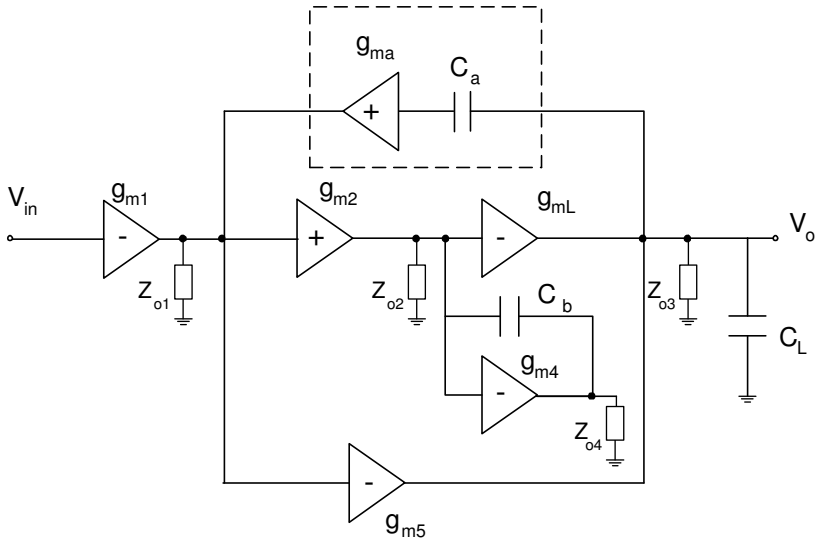


Fig. 2.6 Three stage DLPC amplifier [14]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

$$A_v(s) \cong \frac{A_{dc}}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s(\frac{1}{p_2}+\frac{1}{p_3})+\frac{s^2}{p_2 p_3}\right)} \tag{2.9a}$$

$$\left|p_{2,3}\right| = \sqrt{\left(\frac{g_{ma}}{C_1 C_L}\right)\left(\frac{g_{m2}g_{mL}}{g_{m4}}+g_{m5}\right)} \tag{2.9b}$$

The zeros in the transfer function is in the higher frequency and ignored in (2.9).

The DC gain and the poles of the DLPC are

$$A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}} \tag{2.10}$$

$$p_{-3dB} = \frac{g_{o1}g_{o2}g_{o3}}{C_a g_{m2}g_{mL}} \tag{2.11}$$

The Miller capacitor and bandwidth are

$$C_a = C_b = \sqrt{2\left(\frac{g_{m1}g_{m4}}{g_{m2}g_{mL}+g_{m4}g_{m5}}\right)C_{p1}C_L} \tag{2.12}$$

$$GBW = \sqrt{\left(\frac{g_{m1}}{2g_{m4}}\right)\left(\frac{g_{m2}g_{mL} + g_{m4}g_{m5}}{Cp_1C_L}\right)} \tag{2.13}$$

From (2.12) and (2.13), it can be seen by choosing higher g_{m2}, g_{mL} and g_{m5} with a smaller g_{m4}, DLPC reduces the Miller capacitor value while improving the bandwidth of the amplifier.

For the topologies discussed above, two capacitors are always used to stabilize the multistage amplifiers for large capacitive loads. In this research discussed in section 2.3, a single Miller capacitor compensation approach is introduced to reduce the area and improve the small signal and large signal performance of the amplifiers.

2.2.5 Recent Multi-stage Amplifier Research

2.2.5.1 AC Boosting Compensation Amplifier (ACBC)

ACBC adds an AC path in the internal stage of the conventional multistage amplifier [15], which improves the Figure of Merit in the small signal performance and the large signal performance. Its topology is shown in Fig. 2.7.

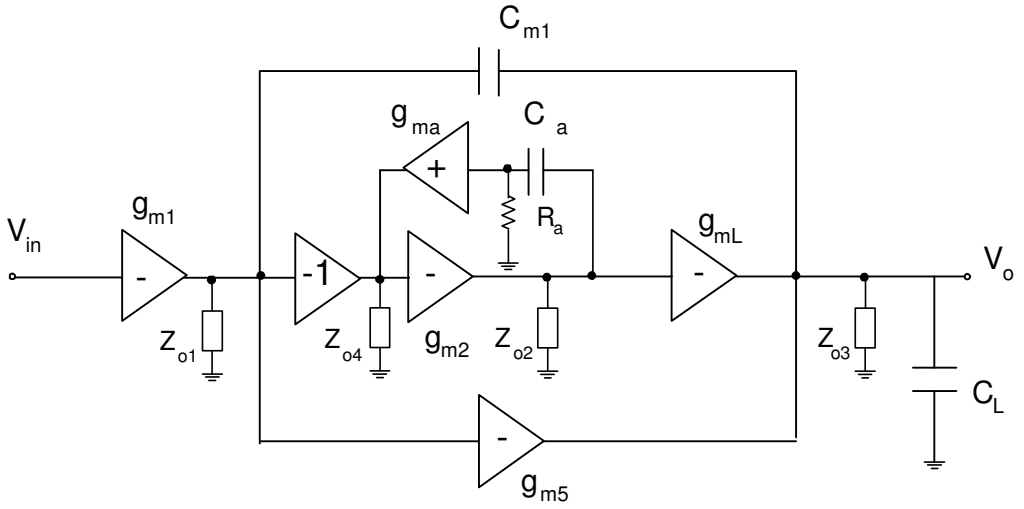


Fig. 2.7 Three stage ACBC amplifier [15]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

Neglecting Z_{04}, the DC gain and the poles of the ACBC can be approximated:

$$A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}} \tag{2.14}$$

$$p_{-3dB} = \frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{mL}} \tag{2.15}$$

The Miller capacitor and bandwidth are

$$C_m = \frac{2g_{m1}}{(g_{m2} + g_{ma})R_a g_{mL} + g_{mf}} C_L \tag{2.16}$$

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{2.17}$$

From (2.16), the required Miller capacitor value is reduced, which leads to larger bandwidth and faster small signal performance.

2.2.5.2 Transconductance with Capacitances Feedback Compensation Amplifier (TCFC)

This topology can be seen as moving the g_{ma}-C_a-R_a loop to output, thus avoiding Z_{04}. TCFC uses a transconductance stage and two capacitors to implement negative feedback for the three stage amplifier [16]. The transfer function of TCFC does not follow the Butterworth frequency responses. The stability of the amplifier is analyzed using Routh stability criterion, which does not need the Butterworth frequency responses. All the non-dominant poles are places much higher than the unity gain frequency to assurance the stability. This topology is shown in Fig. 2.8

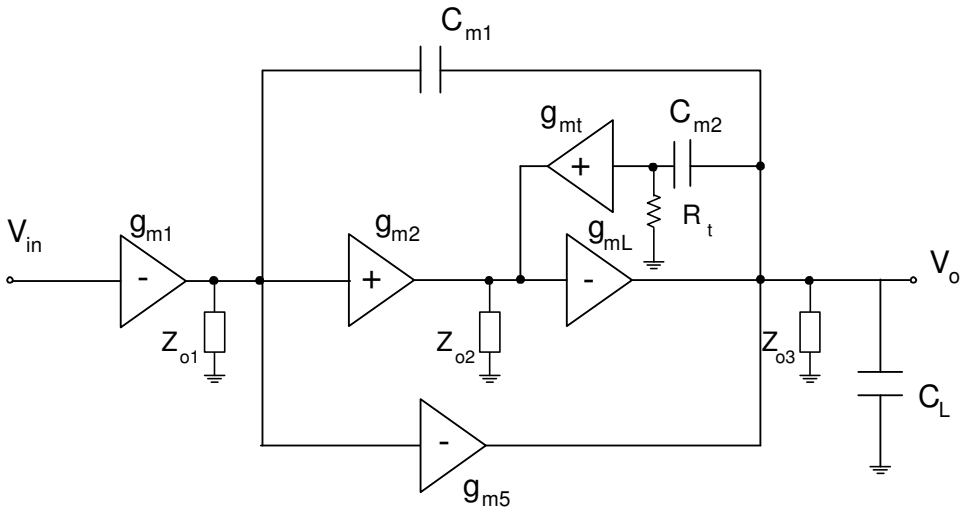


Fig. 2.8 Three stage TCFC amplifier [16]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

The small-signal transfer function of the TCFC amplifier is [16]

$$A_v(s) \cong \frac{A_{dc}\left(1+\frac{s}{\omega_4}+\frac{s^2}{\omega_4\omega_5}+\frac{s^3}{\omega_4\omega_5\omega_6}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}+\frac{s^3}{\omega_1\omega_2\omega_3}\right)} \tag{2.18a}$$

$$p_{-3dB} = \frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{mL}} \tag{2.18b}$$

$$\omega_1 = \frac{1}{1+K_t}\frac{g_{m2}}{C_{m2}} \tag{2.18c}$$

$$\omega_2 = (1+K_t)\frac{C_{m2}}{C_2}\frac{g_{m3}}{C_L} \tag{2.18d}$$

$$\omega_3 = \frac{1}{K_t}\frac{g_{m2}}{C_{m2}} \tag{2.18e}$$

$$\omega_4 = \frac{1}{K_t}\frac{g_{m2}}{C_{m2}} \tag{2.18f}$$

$$\omega_5 = -\frac{1}{K_t}\frac{C_{m2}}{C_2}\frac{g_{m2}}{g_{m1}}\omega_o \tag{2.18g}$$

$$\omega_6 = \frac{1}{K_t}\frac{g_{m2}}{C_{m2}} \tag{2.18h}$$

$$K_t = \frac{g_{m2}}{g_{mt}} \tag{2.18i}$$

The DC gain of the TCFC is $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}}$ (2.19)

The bandwidth is $GBW = \frac{g_{m1}}{C_{m1}}$ (2.20)

2.2.5.3 Reversed Nested Miller Compensation with Nulling Resistor (RNMCNR)

This structure in comparison with the NMC has the feedback from the output of each block to the input, plus a compensation resistor R_c. RNMCNR uses the Miller capacitors C_{m1} and C_{m2}, the resistor R_c, and the feedforward stage g_{mf} to implement the compensation for the three stage amplifier [17]. This topology is shown in Fig. 2.9

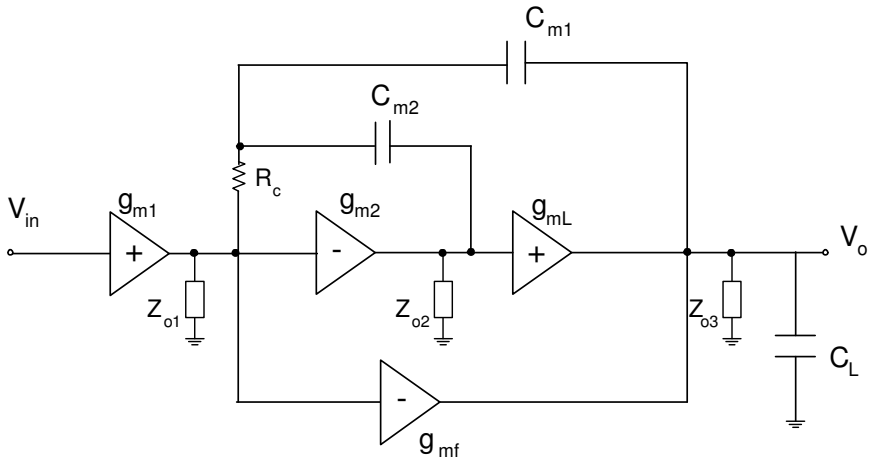


Fig. 2.9 Three stage RNMCFNR amplifier [17]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

The transfer function of RNMCFNR is

$$A_v(s) \cong \frac{A_{dc}\left(1 + s\frac{C_{m1} + C_{m2}}{g_{m2} + g_{m3}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_{m1} + C_L}{g_{m3}C_{m1}}C_{m2} + s^2\frac{C_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{2.21a}$$

$$p_{-3dB} \approx \frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{m3}} \tag{2.21b}$$

$$\left|p_{2,3}\right| = \frac{\frac{g_{m2}(C_{m1}+C_L)}{C_{m1}C_L} \pm \sqrt{\frac{g_{m2}^2(C_{m1}+C_L)^2}{C_{m1}^2C_L^2} - 4\frac{g_{m2}g_{m3}}{C_{m2}C_L}}}{2} \tag{2.21c}$$

$$Z_1 = -\frac{g_{m2}+g_{m3}}{C_{m1}+C_{m2}} \tag{2.21d}$$

The DC gain of the RNMCFNR is

$$A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}} \tag{2.22}$$

The bandwidth is

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{2.23}$$

The gm1 of the amplifier size is obtained through the noise and the offset requirements. The Miller capacitor C_{m1} is calculated using (2.23). The Miller capacitor C_{m2} and the nulling resistor R_c are

$$C_{m2} \approx \frac{2g_{mL}g_{m1}^2}{g_{m2}C_L GBW^2} \tag{2.24}$$

$$R_C = \frac{1}{g_{m2}+g_{mf}} \tag{2.25}$$

2.2.5.4 Reversed Active Feedback Frequency Compensation (RAFFC)

RAFFC uses a current buffer in the outer compensation loop of the typical Reversed Nested Miller Compensation (RNMC) topology. The Miller capacitors C_{m1} and C_{m2}, current

buffer g_{mb}, and the feedforward stage g_{mf} form the compensation network for RAFFC to implement the three stage amplifier [17]. This topology is shown in Fig. 2.10

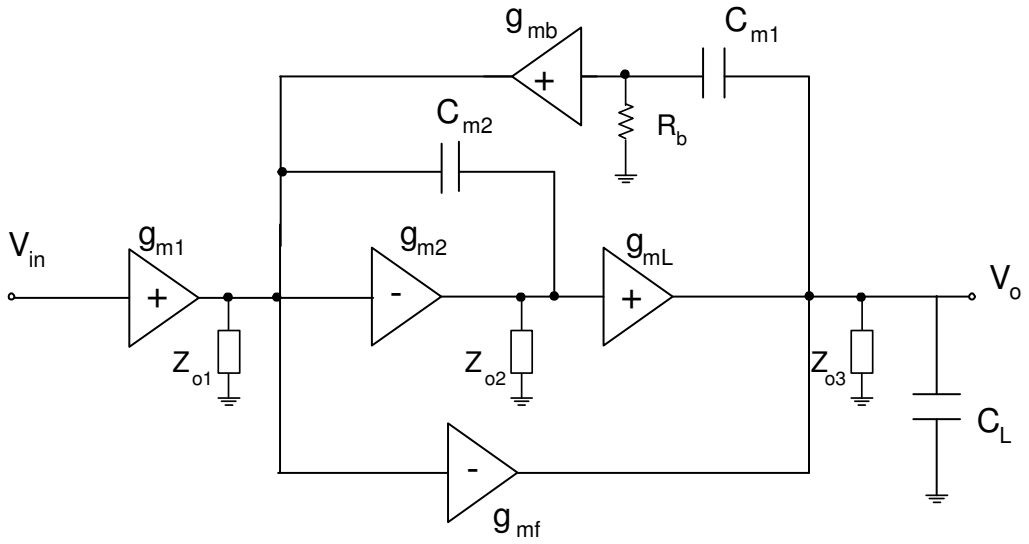


Fig. 2.10 Three stage RAFFC amplifier [17]. $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

The transfer function of RNMCFNR is

$$A_v(s) \cong \frac{A_{dc}\left(1+s\frac{C_{m1}}{g_{mb}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_{m1}+C_L}{g_{m3}C_{m1}}C_{m2}+s^2\frac{C_{m2}C_L}{g_{mb}g_{m3}}\right)} \tag{2.26a}$$

$$p_{-3dB} \approx \frac{g_{o1}g_{o2}g_{o3}}{C_{m1}g_{m2}g_{m3}} \tag{2.26b}$$

$$\left|p_{2,3}\right| = \frac{\frac{g_{mb}(C_{m1}+C_L)}{C_{m1}C_L} \pm \sqrt{\frac{g_{mb}^2(C_{m1}+C_L)^2}{C_{m1}^2C_L^2} - 4\frac{g_{mb}g_{m3}}{C_{m2}C_L}}}{2} \tag{2.26c}$$

$$Z_1 = -\frac{g_{mb}}{C_{m1}} \tag{2.26d}$$

The DC gain of the RNMCFNR is

$$A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{o3}} \tag{2.27}$$

The bandwidth is

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{2.28}$$

The Miller capacitor C_{m2} and the current buffer g_{mb} are

$$g_{mb} = \frac{1}{R_b} \tag{2.29}$$

The inequalities needed for stability is

$$GBW < \frac{C_{m2} + C_L}{C_L}\frac{g_{mb}}{C_{m1}} \approx \frac{g_{mb}}{C_{m1}} \tag{2.30a}$$

$$C_{m2} \approx \frac{2g_{mL}g_{m1}^2}{g_{mb}C_L GBW^2} \tag{2.30b}$$

2.2.6 Summary of the Compensation Technique While Driving Large Capacitive Load

The DC gain, Bandwidth and the stability condition are summarized for the reported compensation topologies.

Table 2.1 Summary of the amplifier capable driving a large capacitive load

Topology	DC gain	Bandwidth	Miller Capacitor
NMC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{1}{4}\frac{g_{mL}}{C_L}$	$C_{m1} = 4\frac{g_{m1}}{g_{mL}}C_L$ $C_{m2} = 4\frac{g_{m2}}{g_{mL}}C_L$
DFCFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{\beta}{4}\frac{g_{mL}}{C_L}$ $\beta > 1$	$C_{m1} = \frac{4}{\beta}\frac{g_{m1}}{g_{mL}}C_L$ $C_{m1} >> C_{m2} > C_{p2}$ where $\beta = 1 + \sqrt{1 + 2(\frac{C_L}{C_{p2}})(\frac{g_{m1}}{g_{mL}})}$
AFFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$N\frac{1}{4}\frac{g_{mL}}{C_L}$ $N > 1, \text{for } g_{m1} > g_{m2}$	$C_{m1} = \frac{4}{N}\frac{g_{m1}}{g_{mL}}C_L$ $C_{m1} >> C_{m2} > C_{p2}$ where $N = \sqrt{8(\frac{C_L}{C_{p2}})[\frac{g_{m1}(g_{m1} - g_{m2})}{g^2_{m3}}]}$
DLPC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$GBW = \sqrt{\left(\frac{g_{m1}}{2g_{m4}}\right)\left(\frac{g_{m2}g_{m3} + g_{m4}g_{m5}}{Cp_1C_L}\right)}$	$C_a = C_b = \sqrt{2\left(\frac{g_{m1}g_{m4}}{g_{m2}g_{m3} + g_{m4}g_{m5}}\right)C_{p1}C_L}$
ACBC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{g_{m1}}{Cm1}$	$C_{m1} = \frac{2g_{m1}}{(g_{m2} + g_{ma})R_a g_{m3} + g_{mf}}C_L$
TCFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{g_{m1}}{Cm1}$	$C_{m2} \approx \frac{C_2C_LGBW}{g_{m3}}$
RNMCNR	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{g_{m1}}{Cm1}$	$C_{m2} \approx \frac{2g_{mL}g^2_{m1}}{g_{m2}C_LGBW^2}$
RAFFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{01}g_{02}g_L}$	$\frac{g_{m1}}{Cm1}$	$C_{m2} \approx \frac{2g_{mL}g^2_{m1}}{g_{mb}C_LGBW^2}$

From Table 2.1, all the compensation techniques use two Miller capacitors, including TCFC and ACBC, to stabilize the amplifiers. In this research, a single Miller capacitor compensation technique is proposed.

2.3 Proposed Single Miller Capacitor Compensation (SMC) and Single Miller Capacitor Feedforward Frequency Compensation (SMFFC) Amplifiers Design

In this work, a single Miller capacitor compensation approach is introduced to reduce the area and improve the small and large signal performance of the amplifiers [18]-[19]. In multistage amplifiers with a large capacitive load, the pole at the output is at low frequency which is located very close to the dominant pole. This is the pole of the output at the first stage. The amplifiers have to be stabilized by removing the effect of the pole at the output. This can be done via pole-splitting using compensation capacitors or pole-zero cancellation using feedforward paths. Low frequency pole-zero doublets will appear if the feed forward path does not cancel the pole properly, which may cause the amplifier to be unstable and deteriorate the settling time of the amplifier [20]. Therefore the pole-splitting technique is more suitable for the design of amplifiers with large capacitive loads.

2.3.1 Single Miller Capacitor Compensation Amplifier (SMC)

2.3.1.1 Structure

The proposed SMC structure is shown in Fig. 2.11.

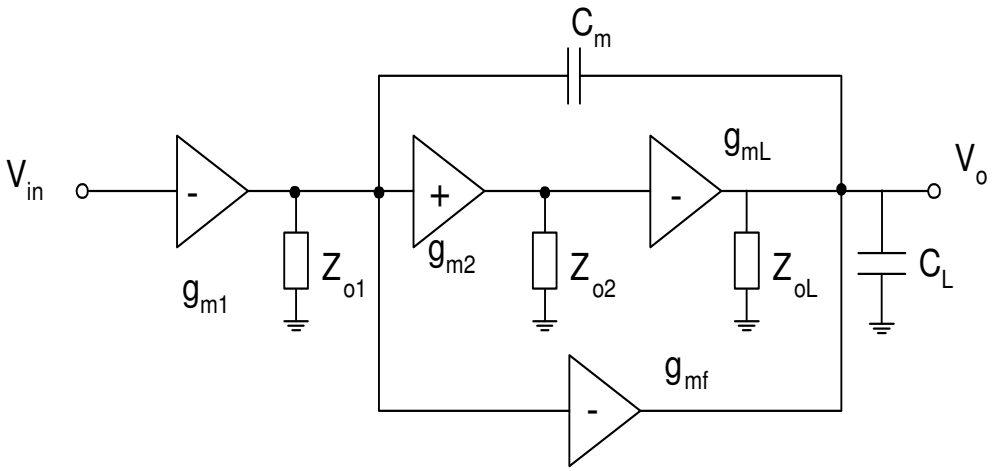


Fig. 2.11 Topology of single Miller capacitor compensation amplifier (SMC).

$Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

A larger bandwidth can be obtained by using only one capacitor for compensation instead of two. The structure has three gain stages with only one compensation capacitor. It has an additional feedforward transconductance stage, g_{mf} from the output of the first stage to the final output. This forms a push-pull stage at the output that helps in improving the transient response of the amplifier. A single Miller compensation capacitor (C_m) is used to split the first pole (p_1) and the third pole (p_3). The position of the second non-dominant pole (p_2) is dictated by the gain of the second stage, which decides the stability of the amplifier. In fact,

as will be shown later, a judicious distribution of the total gain among the three stages can stabilize the amplifier with the use of a single compensation capacitor.

2.3.1.2 Small Signal Analysis

Small signal analysis is carried out using the following assumptions: 1) the gains of all the stages are much greater than 1; 2) parasitic capacitances C_{p1}, C_{p2} and C_{pL} are much smaller than the Miller capacitor C_m and the load capacitor C_L; 3) The transconductance of the feedforward stage, g_{mf}, is equal to that of the third gain stage, g_{mL}. Thus, the transfer function is given by (2.31)

$$A_{v(SMC)}(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{A_{dc}\left(1 + s\frac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{2.31}$$

where $A_{v(SMC)}(0) = A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$ is the dc gain of the amplifier, and is the dominant pole of the amplifier. Hence the gain-bandwidth $p_{3-dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$ product is given by $GBW = A_{dc} \cdot p_{3-dB} = \frac{g_{m1}}{C_m}$. From the transfer function, the amplifier has two non-dominant poles and two zeros.

2.3.1.3 Stability Analysis, Gain-Bandwidth Product, Phase Margin and Dimension Conditions

The stability condition of the SMC amplifier can be determined by analyzing the closed-loop transfer function with a unity-gain feedback configuration. Since the zeros are located at a higher frequency, they are neglected. The closed-loop transfer function $A_{cl(SMC)}(s)$ is shown as below:

$$A_{cl(SMC)}(s) \cong \frac{1}{1+\left(\frac{sC_m}{g_{m1}}\right)\left(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} = \frac{1}{a_0 s^3 + a_1 s^2 + a_2 s + a_3} \tag{2.32}$$

where

$$a_0 = \frac{C_{p2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{2.33}$$

$$a_1 = \frac{g_{o2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{2.34}$$

$$a_2 = \frac{C_m}{g_{m1}} \tag{2.35}$$

$$a_3 = 1 \tag{2.36}$$

From the equation (2.32), the order of the numerator of $A_{cl(SMC)}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator.

Applying the Routh-Hurwitz stability criterion (see Appendix A) to the characteristic equation of transfer function (2.32), it yields

$$a_1 a_2 - a_0 a_3 > 0 \tag{2.37}$$

$$\Rightarrow \frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m} = GBW \tag{2.38}$$

If and only if the condition in (2.38) is satisfied, the system is unconditionally stable.

For large capacitive loads, the stability analysis of the amplifier can be done using the separate pole approach [18]. Assuming that the zeros of the amplifier are located at higher frequencies and hence can be neglected, the non-dominant poles of the amplifier are calculated as follows.

As indicated in the transfer function, the non-dominant poles are located in the left-half plane. The complex poles and resulting frequency peaking are avoided if $\left(\frac{g_{o2}}{C_{p2}}\right)^2 >> 4\frac{g_{m2}g_{mL}}{C_{p2}C_L}$, resulting in the condition $\frac{g_{m2}}{g_{o2}} < \frac{1}{2}\sqrt{\frac{g_{m2}C_L}{g_{mL}C_{p2}}}$. The non-dominant poles are given by $p_2 = \frac{G_{meff}}{C_L}$ and $p_3 = \frac{g_{o2}}{C_{p2}} - \frac{G_{meff}}{C_L}$, where $G_{meff} = \frac{g_{m2}g_{mL}}{g_{02}}$. To stabilize the amplifiers, the second and third pole should satisfy the condition, $GBW \le \frac{1}{2}p_2 \le \frac{1}{4}p_3$ which implies $\frac{g_{m1}}{C_m} \le \frac{1}{2}\frac{G_{meff}}{C_L} \le \frac{1}{4}\left(\frac{g_{o2}}{C_{p2}} - \frac{G_{meff}}{C_L}\right)$ or $3\frac{C_{p2}}{g_{02}} \le \frac{C_L}{G_{meff}} \le \frac{C_m}{2g_{m1}}$. So that $C_m = \frac{2g_{m1}C_L}{G_{meff}}$ or $C_m = \frac{2g_{m1}g_{o2}C_L}{g_{m2}g_{mL}}$. The value of the compensation capacitor becomes

$$C_m = \frac{1}{A_{v2}}\left(2\frac{g_{m1}}{g_{mL}}C_L\right) \tag{2.39}$$

It results in a very small compensation capacitor C_m. Thus, it can be seen that with a suitable choice for the second stage gain $A_{v2} = \frac{g_{m2}}{g_{o2}}$, the value of the compensation capacitor can be reduced. So that the requirement of $g_{mL} >> g_{m1}$ no longer needs to be satisfied, helping to reduce the power consumption of the amplifier. The zeroes of the amplifier depend on the second order equation in the numerator which depends on C_m. Since the value of C_m is very small, all the zeroes are located at high frequencies and can be ignored in the stability analysis.

The phase margin (PM) is given by

$$PM = 180^o - \tan^{-1}(\frac{GBW}{p_1}) - \tan^{-1}(\frac{GBW}{p_2}) - \tan^{-1}(\frac{GBW}{p_3}) \quad (2.40)$$

Under the above conditions on $\frac{GBW}{p_1}$, $\frac{GBW}{p_2}$ and $\frac{GBW}{p_3}$, the phase margin becomes 50^o

2.3.1.4 Slew Rate and Setting Time

The transient response of the amplifier is comprised of the slewing and settling behavior of the amplifier in closed loop condition [18]. The slew rate of the amplifier depends on the amount of the charging current, and the size of the capacitors to be charged. The slew rate solely depends on the size of the compensation capacitor if the available charging current is fixed by the low power constraint. The significant increase in the slew rate of SMC as compared to that of NMC under the same power constraint is due to the reduction in the size

of the compensation capacitor by a factor of $2\frac{g_{m2}}{g_{o2}}$. An improved settling response is obtained by maximizing the phase margin and avoiding pole-zero doublets in the pass band of the amplifier [18]. In the proposed amplifier, there are no pole-zero doublets in the passband, and the calculated phase margin is 50^{o}. In order to increase the phase margin considerably, a LHP zero is introduced with the help of a feedforward stage as shown in the following enhanced amplifier structure.

2.3.2 Single Miller Capacitor Feedforward Frequency Compensation Amplifier (SMFFC)

2.3.2.1 Structure

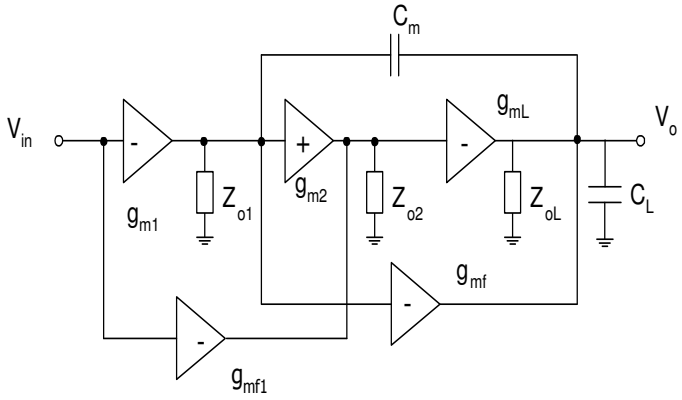


Fig. 2.12 Topology of single Miller capacitor feedforward frequency compensation amplifier (SMFFC). $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, i=1, 2, L

Although, the first non-dominant pole in SMC is designed to be at a relatively higher frequency, it still influences the frequency response to some extent. To provide the further

increases in GBW, and to reduce the compensation capacitor size, the proposed SMFFC is shown in Fig. 2.12. A feedforward path is utilized to provide a LHP zero to compensate the first non-dominant pole, which also adds current at the second stage output, which increases the output conductance of the stage and pushes the pole at the output of the second stage to a higher frequency. The LHP zero is placed near the first non-dominant pole, providing a positive phase shift that compensates for the negative phase shift due to the non-dominant poles.

2.3.2.2 Small Signal Analysis

Solving the small signal circuit model using the same assumptions as that of SMC, the transfer function is given by (2.41)

$$A_{v(SMFFC)}(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{A_{dc}\left(1 + s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{2.41}$$

where the dc gain of the amplifier is $A_{v(SMFFC)}(0) = A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$ and $p_{3-dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$ is the dominant pole of the amplifier. Hence the gain-bandwidth product is given by $GBW = A_{dc} \cdot p_{3-dB} = \frac{g_{m1}}{C_m}$.

2.3.2.3 Stability Analysis, Gain-Bandwidth Product, Phase Margin and Dimension Conditions

The stability analysis utilizes the same theory as that of SMC. Neglecting the effect of the RHP zero in (2.42), the closed-loop transfer function $A_{cl(SMFFC)}(s)$ is given by

$$A_{cl(SMFFC)}(s) \cong \frac{1+s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}}{1+s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}+\frac{sC_m}{g_{m1}}\left(1+s\frac{C_Lg_{o2}}{g_{m2}g_{mL}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{2.42}$$

From the equation (2.42), the order of the numerator of $A_{cl(SMFFC)}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator. The Routh-Hurwitz stability criterion provides the following condition:

$$\frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m}\left(\frac{1}{1+g_{mf1}/g_{m2}}\right) \tag{2.43}$$

For a large capacitive load, the stability analysis of the amplifier is done using the separate pole approach [18]. Since the s^2 term in the numerator of (2.42) is negative and the s term is positive, this implies that there is a LHP zero and a RHP zero. The LHP zero occurs at a lower frequency than the RHP zero. This helps to improve the frequency response. From the transfer function, the non-dominant poles are exactly the same as those of SMC, and the zeroes of the amplifier are

$$z_{LHP} = \frac{g_{m1}g_{m2}}{g_{mf1}C_m} \tag{2.44}$$

$$z_{RHP} = \left(\frac{g_{mf1} g_{mL}}{g_{m1} C_{p2}} + \frac{g_{m1} g_{m2}}{g_{mf1} C_m} \right) \approx \frac{g_{mf1} g_{mL}}{g_{m1} C_{p2}} \tag{2.45}$$

Since $C_m >> C_{p2}$, the RHP zero is at a very high frequency and does not cause stability problems.

The phase margin (PM) is calculated as per equation (2.46)

$$PM = 180^o - \tan^{-1}(\frac{GBW}{p_1}) - \tan^{-1}(\frac{GBW}{p_2}) - \tan^{-1}(\frac{GBW}{p_3}) + \tan^{-1}(\frac{GBW}{z_{LHP}}) \tag{2.46}$$

In our particular case, PM yields 75^o.

The above calculation of phase margin assumes exact pole-zero cancellation, which implies

$$p_2 = z_{LHP} \Rightarrow g_{mf1} = \frac{1}{A_{V2}} \frac{g_{m1} g_{m2} C_L}{g_{mL} C_m} \tag{2.47}$$

where $p_2 = \frac{g_{m2} g_{mL}}{g_{02} C_L}$ and $z_{LHP} = \frac{g_{m1} g_{m2}}{g_{mf1} C_m}$. If there is a mismatch in the pole-zero cancellation, the pole-zero doublets will appear. Since it occurs at high frequency (around twice the bandwidth), the amplifier performance is not significantly disturbed.

2.3.2.4 Slew Rate and Settling Time

In the case of SMFFC the obtainable phase margin obtainable is close to 75^o. Hence the compensation capacitor C_m can be further reduced to achieve a still higher bandwidth without sacrificing the stability of the amplifier. This helps to improve the slew rate of the

amplifier because the slew rate is inversely proportional to the size of the compensation capacitor under a fixed power constraint. In the proposed topology, pole-zero doublets are not present in the pass band. This is because both the pole and the zero are at higher frequencies and can be placed outside the pass band of the amplifier at almost twice the unity gain bandwidth. High frequency pole-zero doublets do not degrade the settling time [18] as much as low frequency doublets, as a result, the settling time is not significantly affected by the introduction of the LHP zero.

The pole-zero locations for the amplifier with and without feedback is shown in Fig. 2.13. Where the zeros in the uncompensated and SMC amplifier are in the higher frequency than the poles and ignored in the plot. In SMFFC, a left half plate zero Z_{LHP} is generated to cancel the second non-dominant pole of the SMFFC.

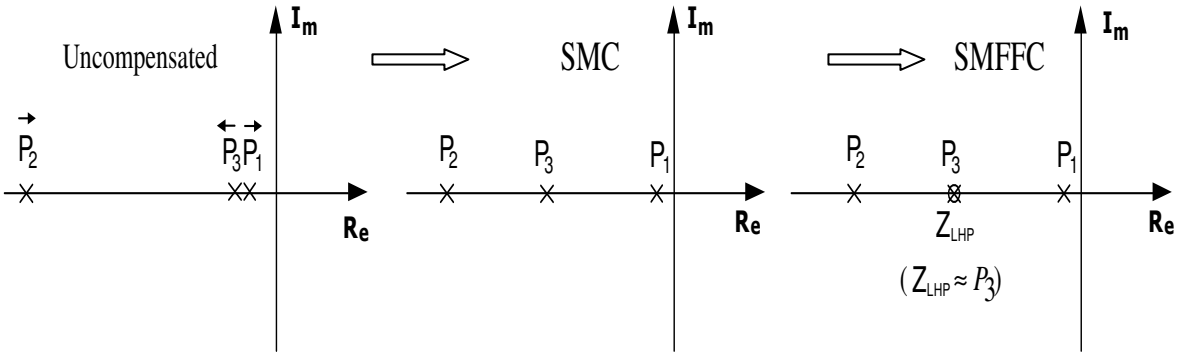


Fig. 2.13 Root locus for uncompensated, SMC and SMFFC amplifiers with 120pF load

2.3.3 Design Considerations, Circuit Implementation and Design Procedure

The circuit implementations of the SMC and SMFFC amplifiers are shown in Fig.2.14 and Fig.2.15 respectively. Transistors M_1-M_8 form the first gain stage. Transistors M_{f1} and

M_{f2} form the feedforward transconductance stage, g_{mf1} in the SMFFC amplifier. The second gain stage of the amplifier is comprised of transistors M_9–M_{12}. The output stage is comprised of a feedforward stage (g_{mf} in SMC and g_{mf} in SMFFC) and the third gain stage, g_{mL} forming a push-pull stage. The third gain stage is realized by transistor M_{13} whereas the feedforward stage is realized by transistor M_{14}.

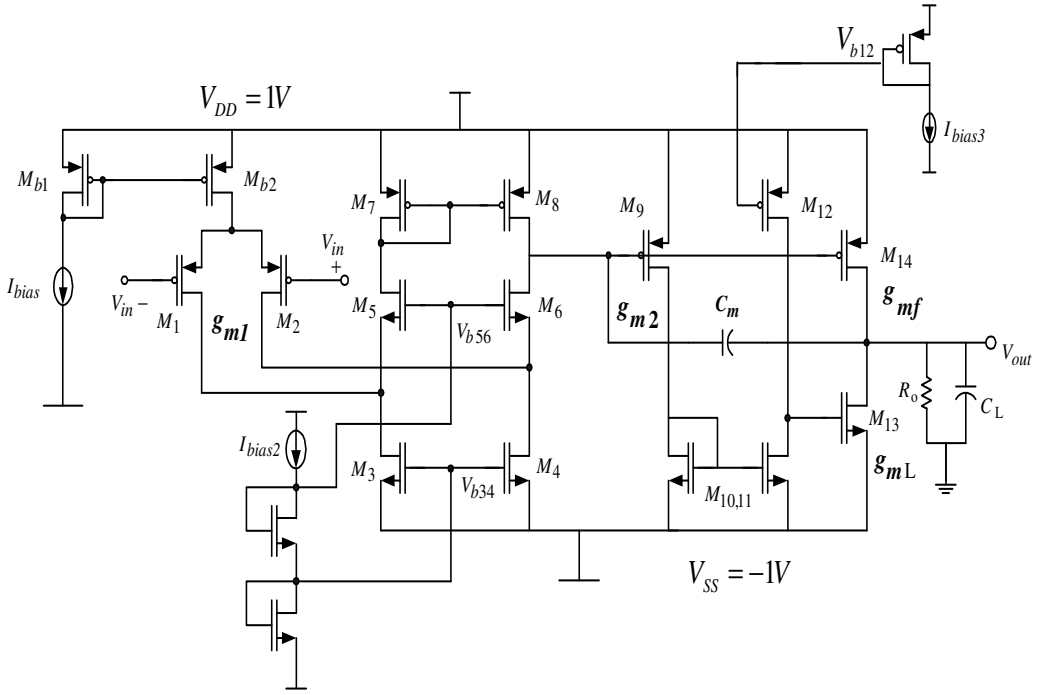


Fig. 2.14 Schematic of the SMC amplifier

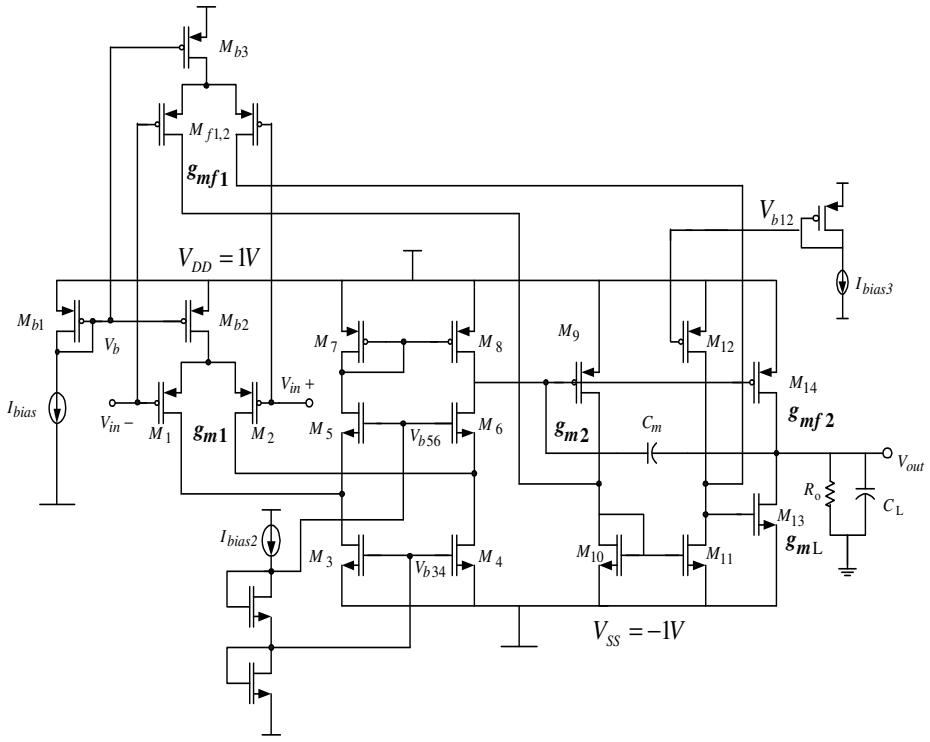


Fig. 2.15 Schematic of the SMFFC amplifier

2.3.3.1 Design Procedure

The design procedure for the SMC and SMFFC amplifiers is almost the same except that the SMC amplifier does not have the feedforward stage from the input to the output of the second stage. Hence we show the design procedure of SMFFC in Fig. 2.16. Although there is clear design procedure available, the circuit implementation ultimately requires tuning of transistor sizes, bias currents and compensation capacitors.

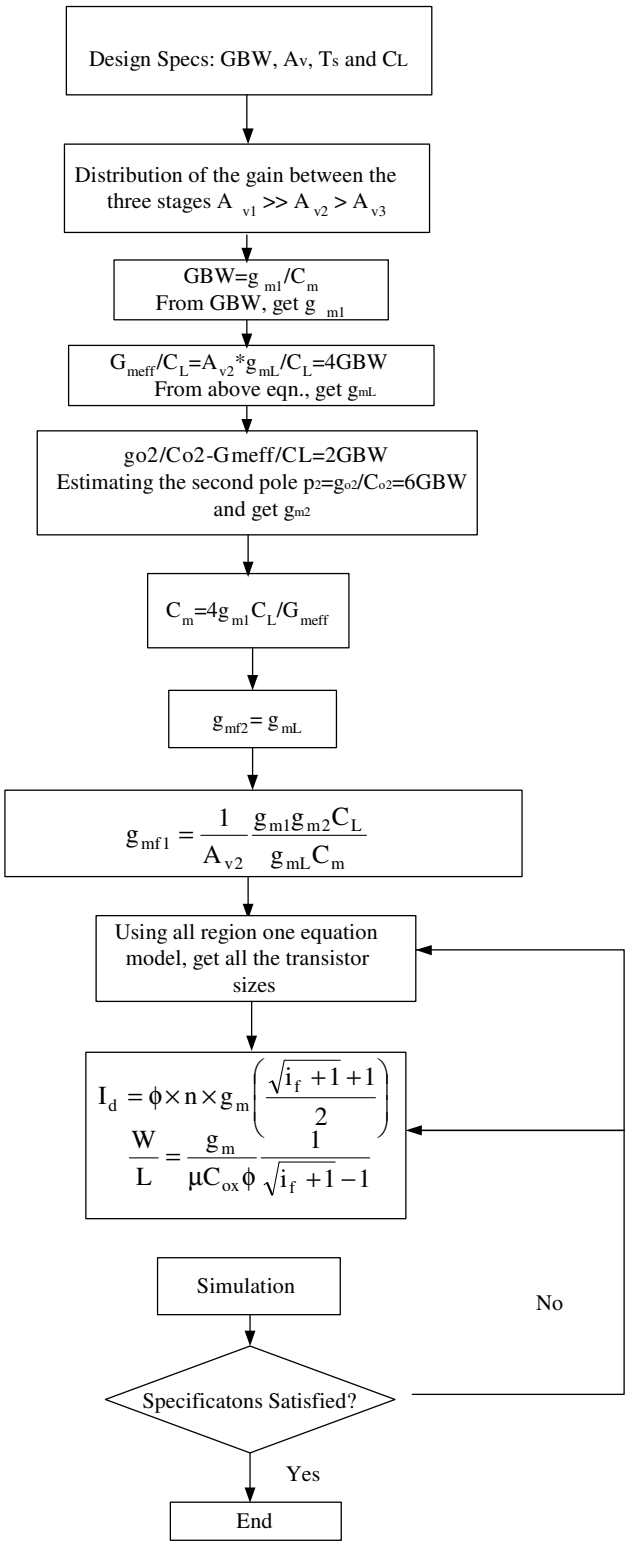


Fig. 2.16 Design procedure for SMFFC

First, distribute judiciously the gain among the three stages. For high gain amplifiers (>100 dB) the gain is distributed such that $A_{v1} >> A_{v2} > A_{v3}$. The gain of the first stage is maximized, with the second stage having moderate gain and the final stage having a relatively small gain, i.e, A_{v1}=50dB, A_{v2}=30dB and A_{v3}=20dB. This results in the second and third pole of the amplifier being located at higher frequencies due to the high output conductance of the second and third stages. This results in a roughly single pole system. Second, assume a value of the Miller capacitance (C_m), the transconductance of the first stage can be obtained through the Gain-Bandwidth Product (GBW). The first stage g_{m1} can be estimated by the desired GBW and C_m. For 9MHz GBW and 4pF C_m, g_{m1} is calculated as g_{m1}=GBW×C_m=226μA/V. And then, the output stage transconductance is obtained. Since $G_{meff}/C_L=A_{v2}\times g_{mL}/C_L$=4GBW, g_{mL}=4GBW×C_L/A_{v2}=858μA/V. Next, the transconductance of the second stage can be estimated using the estimated parasitic capacitance and the required second stage gain. Since g_{o2}/C_{o2}=6GBW, g_{o2}=6GBW×C_{o2}. The second stage gain is $A_{v2}=g_{m2}/g_{02}$, and $g_{m2}=A_{v2}\times g02=A_{v2}\times$6GBW×$C_{o2}$=300μA/V. Following that, the feedforward stage can be easily calculated. $g_{mf2}=g_{mL}$=858μA/V. $g_{mf1}=\frac{1}{A_{v2}}\frac{g_{m1}g_{m2}C_L}{g_{mL}C_m}=80\mu A/V$. And then, using the all range one equation or BSIM model to estimate the transistor size. Finally, perform the simulation to verify the specifications of the amplifier.

In order to achieve this, the first stage uses a folded cascode topology to enhance the output impedance. A moderate gain at the second stage helps in reducing the required compensation capacitor to a great extent. For example a 100dB gain from three stages can be

distributed as 60dB, 30dB and 10dB for first, second and third stages respectively. Thus, A_{v2}= 30dB ≈ 30V/V resulting in a reduction of the required C_m by a factor of 2×30=60 compared to that of NMC while maintaining stability.

From the calculation and simulation of SMC, $g_{m1} = 274.7\mu A/V$ $g_{m2} = 271.1\mu A/V$ $g_{mL} = 695.9\mu A/V$ and $g_{mf} = 758\mu A/V$. For SMFFC, $g_{m1} = 274.7\mu A/V$, $g_{m2} = 269.4\mu A/V$, $g_{mL} = 757.1\mu A/V$, $g_{mf} = 799\mu A/V$, and $g_{mf1} = 175.3\mu A/V$. Transistors M_{b1} – M_{b3} form the bias and tail current sources respectively. V_{b34} , V_{b56} and V_{b12} shown in the amplifier schematics are dc bias voltages and are implemented with current mirrors and current sources. The transistor sizes for both the circuits are provided in Table 2.2.

2.3.4 Experimental Results, Testing Setup and Comparison

The proposed SMC and SMFFC amplifiers were implemented using AMI 0.5µm CMOS technology. Fig. 2.17 and Fig. 2.18 show the chip micrograph of the amplifiers.

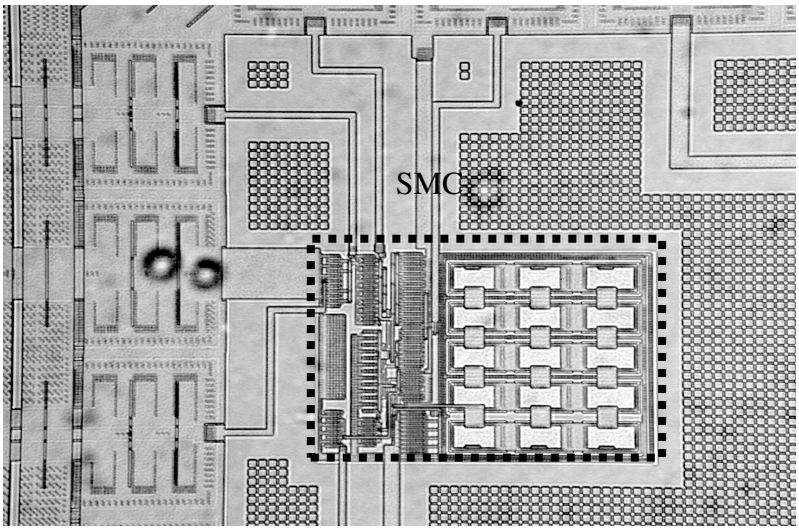


Fig. 2.17 Chip micrograph of the SMC amplifier

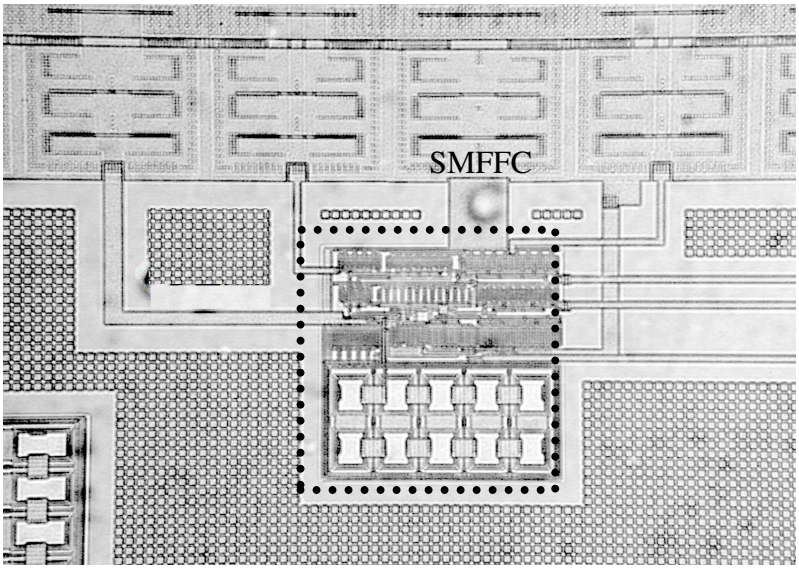


Fig. 2.18 Chip micrograph of the SMFFC amplifier

The testing board of the amplifier is shown in Fig. 2.19. The input and output of the amplifier is connected using BNC connector.

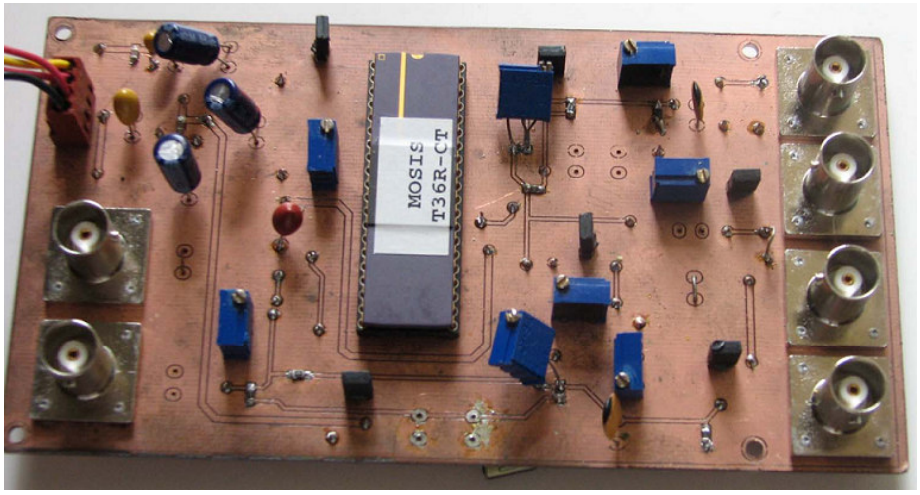


Fig. 2.19 Testing board of SMC and SMFFC amplifiers

The AC response of the amplifier is tested using HP89410A Vector Signal Analyzer. The testing set-up is shown in Fig. 2.20.

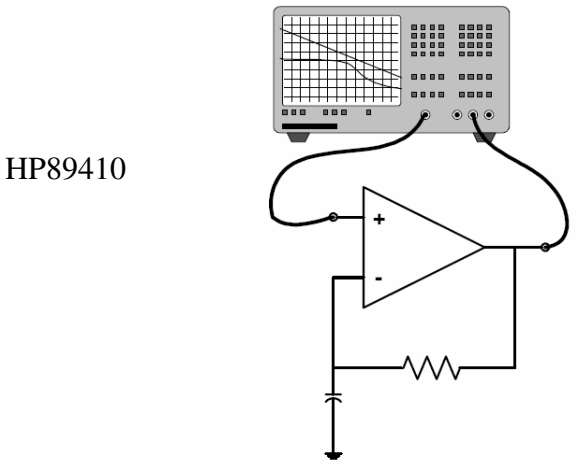


Fig. 2.20 AC response testing setup of SMC and SMFFC amplifiers

The transient response of the amplifier is tested with the unit gain configuration by using a step input signal. The transient response is observed the output signal using oscilloscope. The testing set-up is shown in Fig. 2.21.

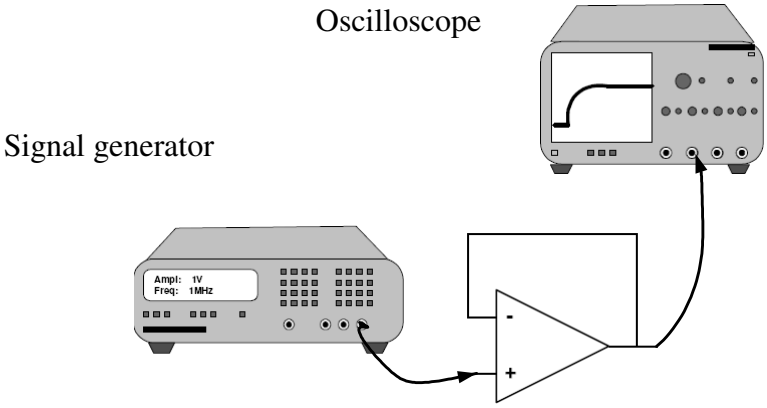


Fig. 2.21 Transient response testing setup of SMC and SMFFC amplifiers

Table 2.2 Transistor sizes of SMC and SMFFC

Transistor	SMC	SMFFC
Mb1	2×(5.55/1.05)	2×(5.55/1.05)
Mb2	8×(5.55/1.05)	8×(5.55/1.05)
M1,2	8×(6.15/0.6)	8×(6.15/0.6)
M3,4	6×(10.05/1.05)	6×(10.05/1.05)
M5,6	2×(10.05/1.05)	2×(10.05/1.05)
M7,8	6×(6.15/1.95)	6×(6.15/1.95)
M9	6×(6.3/0.6)	6×(6.3/0.6)
M10,11	2×(9/0.75)	2×(9/0.75)
M12	6×(5.55/0.6)	6×(5.55/0.6)
M14	10×(10.05/0.6)	10×(10.05/0.6)
M13	2×(9.3/0.6)	2×(9.3/0.6)
Mf1,2	-	6×(5.55/0.75)
Mb3	-	6×(5.55/1.05)
Total Active Area (W×L)	167μm×122μm	122μm×122μm

The measured results and the simulated frequency response of the SMC amplifier are shown in Fig.2.22 and Fig.2.23. The measured results and the simulated frequency response of the SMFFC amplifier are shown in Fig. 2.24 and Fig. 2.25. Deviations between experimental and simulated results are within 15%. Fig. 2.26 shows the transient response for both amplifiers. Both the results above are with a $25k\Omega/120pF$ load.

A comparison table (Table 2.3) is provided to show the advantages and drawbacks of the proposed and previous topologies. According to Table 2.3, the proposed topologies have improved frequency and transient behavior as compared to the existing topologies (except the recent publications). Since the area of the circuit is mainly comprised of the compensation capacitor, a much lower area is obtained for the proposed amplifier topologies.

Compared to the NMC, DFCFC, and AFFC when driving a 120pF load, the proposed SMC and SMFFC amplifiers improve the GBW while greatly reducing the area without compromising on power. The GBW of the SMC and SMFFC amplifiers is 22.5 and 11.5 times that of the NMC respectively. The average slew rates of the amplifiers are 24 and 16.4 times that of NMC amplifier respectively. Without significant increase in power consumption as compared to NMC the SMC and SMFFC amplifiers occupy almost 7 and 9.3 times less silicon area respectively.

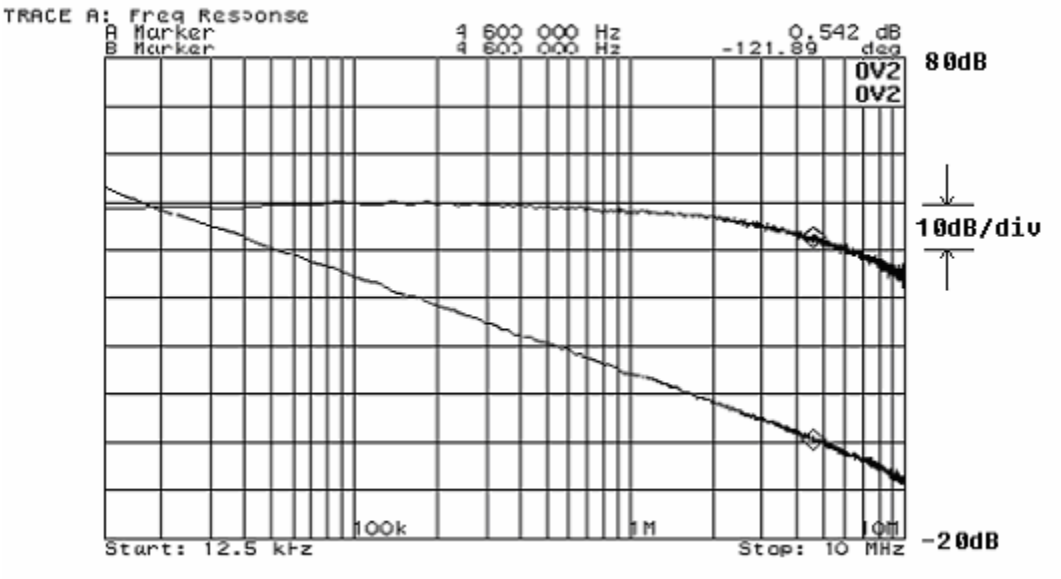


Fig. 2.22 Frequency response of SMC amplifier with 120pF/25kΩ load (measurement result) with GBW=4.6MHz, and PM=58.1^{o}

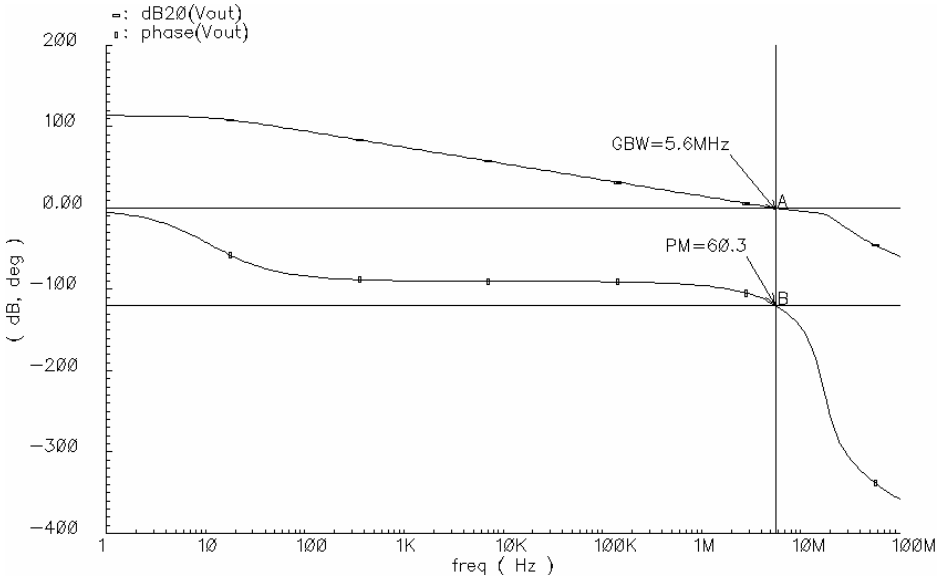


Fig. 2.23 Frequency response of SMC amplifier with 120pF/25kΩ load (simulation result)

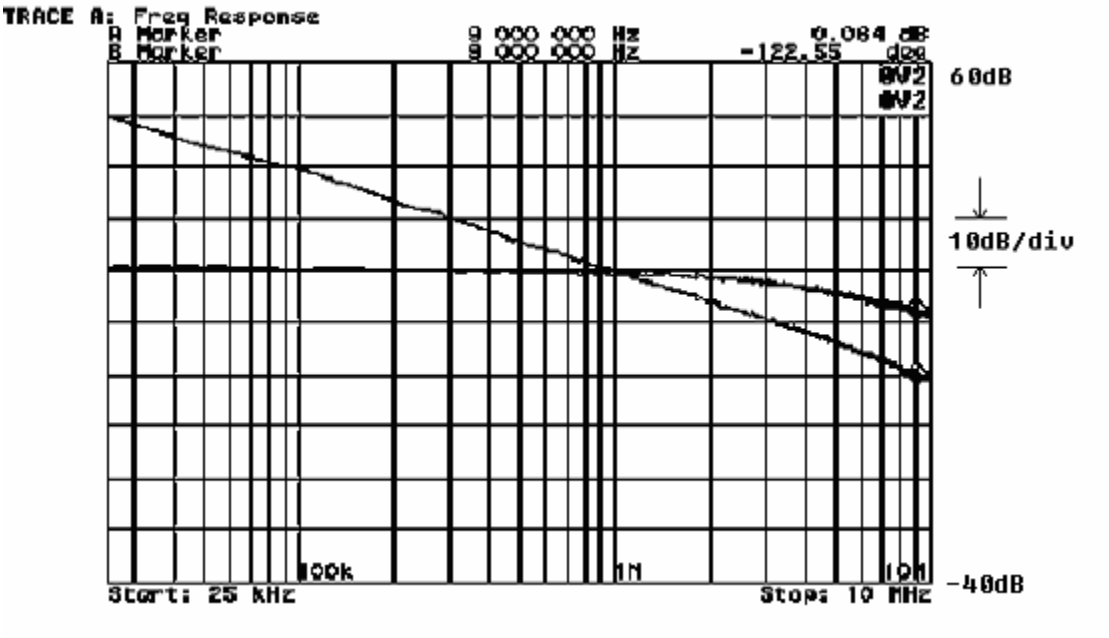


Fig. 2.24 Frequency response of SMFFC amplifier with 120pF/25kΩ load (measurement result) with GBW=9MHz, and PM=57.4^{o}

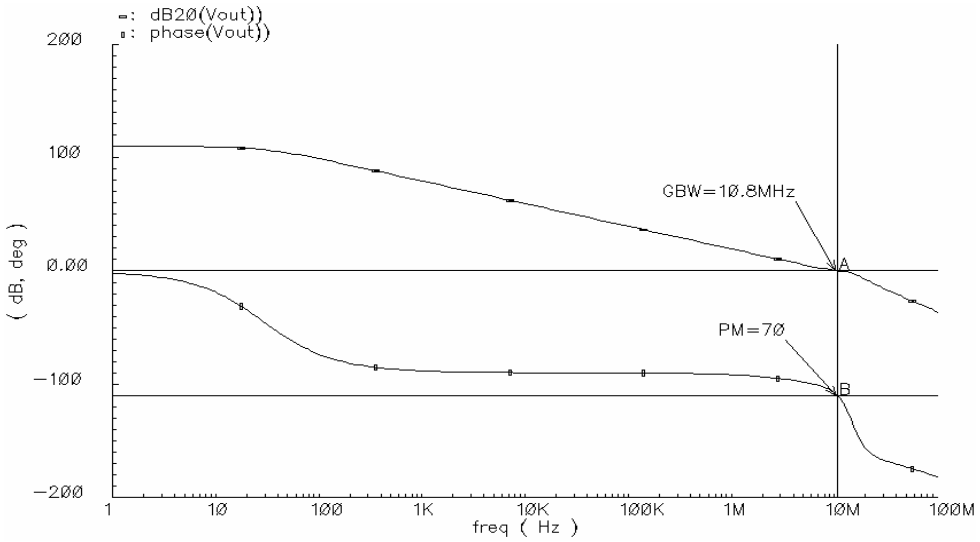


Fig. 2.25 Frequency response of SMFFC amplifier with 120pF/25kΩ load (simulation result)

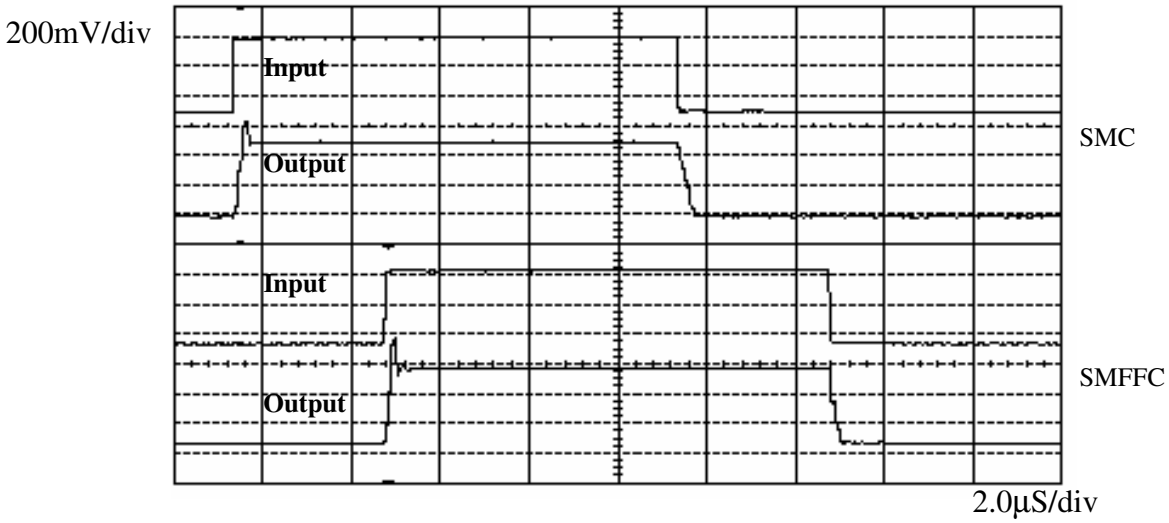


Fig. 2.26 Experimental transient response of the amplifiers with 120pF/25kΩ load

For a 400 KHz $0.2V_{p\text{-}p}$ input signal, SMC has $HD_3 = 60.9dB$, and for a 400 KHz $0.2V_{p\text{-}p}$ input signal, SMFFC has $HD_3 = 65.17dB$, which is shown in Fig. 2.27 and Fig. 2.28.

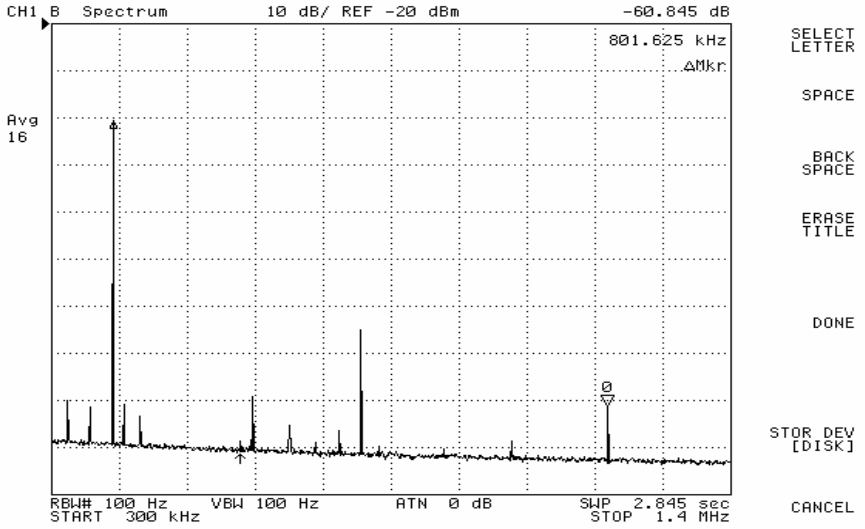


Fig. 2.27 Harmonic distortion of SMC with a 400 kHz $0.2V_{p\text{-}p}$ input signal

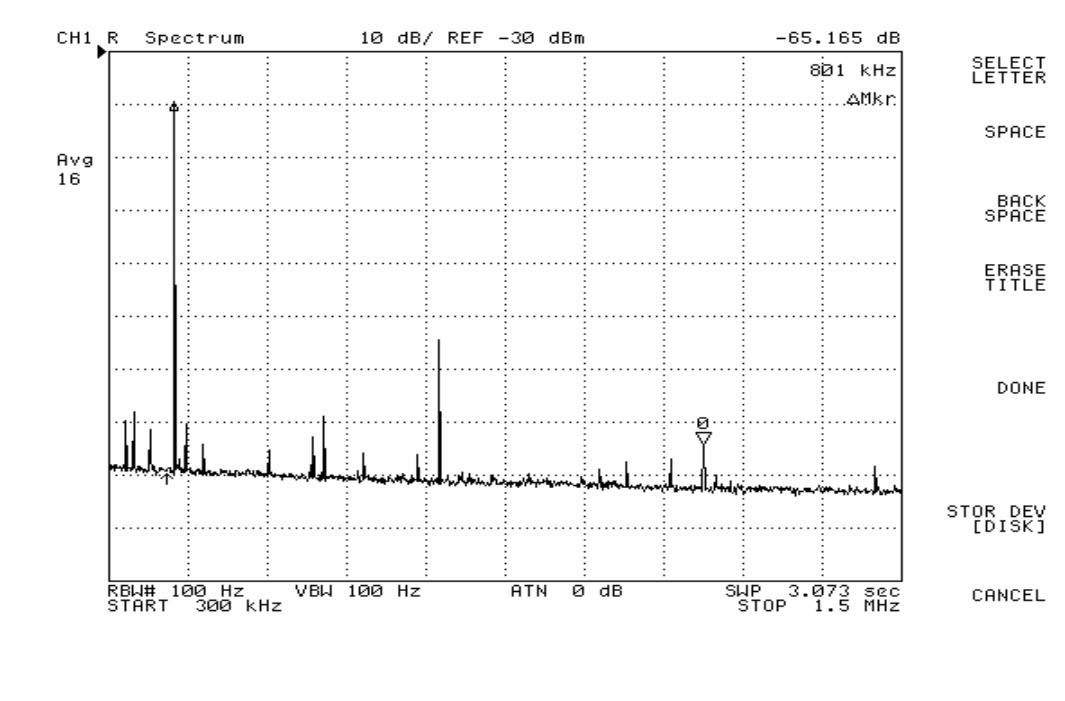


Fig. 2.28 Harmonic distortion of SMFFC with a 400 kHz, $0.2V_{p\text{-}p}$ input signal

The proposed SMC and SMFFC amplifiers were designed for $25k\Omega/120pF$. For smaller load capacitors, the circuit is also stable if the design satisfies the condition (2.38) or (2.43). For our design, the system is stable even for 10pF according to the Routh-Hurwitz stability criterion. The difference between the small load capacitor and the large load capacitor is that the system has real pole for large load capacitors and the system has complex poles for small load capacitors. All the poles in both conditions are located in the left half plane, which means that the system is stable for both small and large load capacitors. Observe that for the small load capacitors, it is not proper to use the separate pole approach to perform the analysis because of the existence of complex poles.

Since the pole from the load is pushed to a higher frequency as the first non-dominant pole, variations in the large load capacitor does not linearly influence the GBW. For much larger load capacitor, the Miller capacitor value needs to be increased to push the pole at the output far from the unity gain frequency. Increasing the value of Miller capacitor C_m from 4pF to 8pF, with a 500pF load capacitor, SMFFC achieves 4.64MHz GBW, and 59^o phase margin with the same power consumption as that for $25k\Omega/500pF$ load.

Table 2.3 Comparison of different multistage amplifiers with large capacitive loads

Parameter	NMC [13]	DFCFC [10]	AFFC [13]	DLPC [14]	ACBC [15]	TCFC [16]	RNMCNR [17]	RAFFC [17]	This work SMC	This work SMFFC
Load pF/kΩ	120/25	100/25	120/25	120/25	500/25	150/25	500/25	500/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100	>100	>100	>100	>100
GBW(MHz)	0.4	2.6	4.5	7	1.9	2.85	2.4	2.4	4.6	9
Phase margin	61^o	43^o	65^o	46^o	52^o	58.6^o	58^o	58^o	58^o	57^o
Power (mW@Vdd)	0.38 @2	0.42 @2	0.4 @2	0.33@1 .5	0.33@ 2	0.045@ 1.5	0.255@3	0.315@3	0.38@2	0.41@2
Capacitor value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	C_m=3 C_a=7	C_a=4.8 C_b=2.5	C_m=10 C_a=3	C_{m1}=1.1 C_{m2}=0.9	C_{m1}=11.5 C_{m2}=0.35	C_{m1}=11 C_{m2}=0.3 5	C_m=7 (one)	C_m=4 (one)
SR+(V/μS) SR-(V/μS)	0.15 0.13	1.32 1.27	0.78 2.20	2.2 4.4	0.8 1.2	0.96 1.11	1.8 1.8	2.1 1.8	3.28 1.31	4.8 2
+1% TS (μs) -1% TS (μs)	4.9 4.7	0.96 1.37	0.42 0.85	0.315 0.68	1.9 1.2	2.8 1.7	0.74 0.81	0.50 0.56	0.53 0.4	0.58 0.43
FOM_S (MHz.pF/mW)	127	619	1350	2545	2932	9500	4706	3810	1453	2634
FOM_L (V/μs.pF/mW)	45	308.3	447	1200	1543	3450	3529	3095	726	996
FOM_S^* (MHz.pF/mW.pF)	1.28	29.5	135	348.6	225	4702	397	336	207.6	658
FOM_L^* (V/μs.pF/mW.pF)	0.45	14.7	44.7	164.4	118.7	1725	298	273	103.7	249
Area(mm^2)/0.015	9.3	7.3	4	3.33	1.33	1.33	1.67	1.6	1.33	1
Technology	0.8μm CMOS	0.8μm CMOS	0.8μm CMOS	0.6μm CMOS	0.35μ m CMOS	0.35μm CMOS	0.5μm CMOS	0.5μm CMOS	0.5μm CMOS	0.5μm CMOS

Note: average value of the slew rate is used in the calculation of FOM_L and FOM_L^* parameter

2.3.5 Summary of the SMC and SMFFC Amplifiers

Two compensation topologies for low-power multistage amplifiers with large capacitive loads were introduced, SMC and SMFFC. It was shown that with only a small compensation capacitor, the area of the amplifier was reduced significantly, the gain bandwidth product is improved and the stability condition is established. The separate pole approach is used to perform the analysis for large capacitive loads. A feedforward path is added to the SMFFC amplifier to further improve the GBW and to reduce the silicon area. Based on a comprehensive comparison of the proposed amplifiers against other reported structures with large capacitive loads, the proposed compensation techniques demonstrate superior performance.

CHAPTER III

LOW NOISE AMPLIFIER (LNA) DESIGN OVERVIEW (NARROWBAND LNA AND WIDEBAND LNA)

The LNA serves as the first stage of the wireless receiver [1] [2]. The incoming wireless signal from the antenna is fed to the input of LNA, which is normally very weak normally in the region -100dBm to -70dBm. The LNA needs to amplify the weak signal so that the following Mixer can process it. Thus, the LNA needs to have a certain power gain. The noise generated by LNA is directly added in the signal in the amplifying procedure and reduces the signal to noise ratio (SNR) of the signal. In contrast, the noise contribution from the following stages of the receiver is attenuated by LNA gain. To satisfy the system noise requirement, the noise contribution from the LNA should not be large. Finally, due to the nonlinear performance of the LNA, the out-of-band signal can generate in-band interference, which will reduce the overall system linearity performance and dynamic region. Different metrics and topologies of the LNA are discussed in the following sections.

3.1 Basic Metrics of the LNA

3.1.1 S-parameters of the LNA

The scattering parameters are widely used in RF and microwave circuits to represent the scattering or reflection functions of the traveling wave when the n-port network is inserted

into a transmission line. They are helpful for component modeling and circuit design. There are also other representations using impedance (Z) and or admittance (Y) parameters. At the low frequency, the Z parameters can be easily obtained using the open-circuit approach. The Y parameters can be easily obtained using the short-circuit approach. At the high frequency, it is difficult to provide adequate shorts or opens, and the active circuits may resonate when terminated in short or open circuits. S-parameter, in the contrary, measures the traveling wave, which does not need nor allow the short or open connections. Since a line terminated in its characteristic impedance generates no reflections, S-parameter can measure the device, which has some distance from the instrument and is connected using a low-loss transmission lines. The s-parameters involve measuring power versus others two-port parameters that involve measuring the current or voltage.

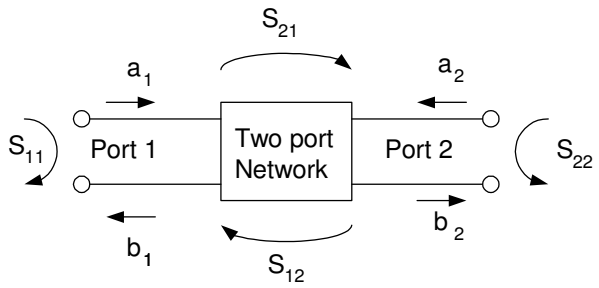


Fig. 3.1 Two port network and its S-parameter

A two-port network in Fig. 3.1 is used to explain the definition of the S-parameters, where a_1 and a_2 represent the incident waves and b_1 and b_2 represents the reflected waves.

The S-parameters are given by

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.2}$$

The S-parameters are defined as

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{3.3}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{3.4}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{3.5}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{3.6}$$

$a_1 = 0$ means that the port 1 is grounded and there are no incident waves from port 1.At that time, the port one is loaded with a resistance of Z_L=Z_o. $a_2 = 0$ means that the port 2 is grounded and there are no incident waves from port 2. At that time, port two is loaded with a resistance of Z_L=Zo. S_{11} and S_{22} represent the reflection coefficients at port 1 and 2. S_{21} and S_{12} represent the transmission coefficients from port 1 to port 2 and from port 2 to port 1. The ideal values of S_{11} and S_{22} are -∞, so that the port 1 and port 2 are perfectly matched, resulting in no reflection. The ideal value of S_{12}, that is the power at port 1 due to the power from port 2, is -∞ so that the port 1 and port 2 are perfectly isolated. The S_{21} typically represents the power gain of the system, which needs to be designed according to the system requirement. For a Low Noise Amplifier (LNA), it is typically designed between 15dB-25dB.

The stability factor of LNA is defined as [1]

$$K = \frac{1 + |\Delta|^2 - |S11|^2 - |S22|^2}{2|S21||S12|} \tag{3.7}$$

where $\Delta = S11S22 - S12S21$

The unconditionally stable of LNA is K>1 and $|\Delta| < 1$. When the input and output of the LNA are matched to the source and load impedance, S11 and S22 are almost 0. With the decreasing of the S12, $|\Delta|$ reduces, which means the better stability of the LNA.

3.1.2 Impedance Matching of the Low Noise Amplifier (LNA)

The signal from the antenna, here represented by V_s and Z_s, is transferred to the input of the LNA and is amplified by the LNA.

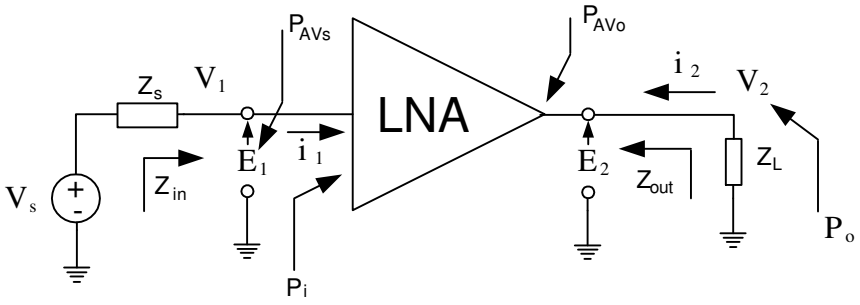


Fig.3.2 (a) LNA in the network

where P_{AVs} is available power from the source to a conjugate-matched circuits and P_{in} is the input power from the source to the network, which is not necessary matched to the source impedance.

Power gain (G) is the ratio of the power delivered to the load to that delivered by the source.

$$G = \frac{P_o}{P_i} \tag{3.8}$$

where the output power is P_o and P_{in} is the input power. Transducer power gain G_T is the ratio of the power delivered to the load by the power available from the source.

$$G_T = \frac{P_o}{P_{AVs}} \tag{3.9}$$

where P_{AVs} is the power available from the source to a conjugate-matched circuits

Available power gain G_A is the ratio of the power available at the output of a network by the power available from the source.

$$G_A = \frac{P_{AVo}}{P_{AVs}} \tag{3.10}$$

where P_{AVo} is the power that the circuit can deliver to a conjugate-matched load.

For the network shown in Fig. 3.2, the power transfer to the input of the LNA is calculated as

$$P_i = P_{in\_LNA} = V_1 i_1 = \frac{V_1^2}{|Z_{in}|} = \frac{V_s^2 |Z_{in}|}{(|Z_{in} + Z_s|)^2} \tag{3.11}$$

when $Z_{in} = Z_s^*$, the input network has the maximum transferred power

$$P_{AVs} = P_{in\_LNA} = \frac{V_1^2}{|Z_{in}|} = \frac{V_s^2}{2\,\mathrm{Re}(Z_s)} = \frac{P_{in}}{2} \tag{3.12}$$

LNA usually require a matching network to connect to the antenna, as shown in Fig. 3.2b.

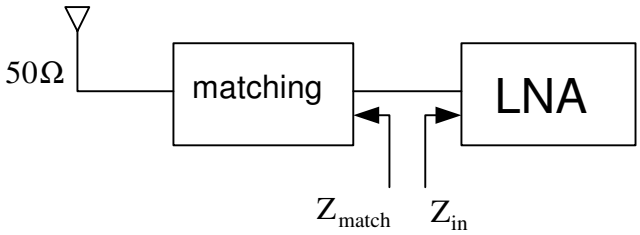


Fig.3.2 Continued. (b) Conceptual idea of LNA connected to the antenna

To achieve the maximum power transfer, the input impedance of the LNA (Z_{match}) should be designed to match the complex conjugate impedance (Z_{in}) of the previous stage as shown in Fig. 3.2b and expressed in (3.13), which is normally the antenna or the off-chip filter with a 50Ω impedance.

$$Z_{match} = Z_{in}^{*} \tag{3.13}$$

where Z_{in}^{*} is the complex conjugate of the previous stage impedance (Z_{in}). In practice, this matching $Z_{match} + Z_{in}^{*}$ yields $2\,\mathrm{Re}(Z_{in})$

S-parameters are widely used to represent the performance of the RF LNA.

The input S11 of the LNA can be calculated by

$$S_{11\_LNA} = 20\log\left(\left|\frac{Z_{in} - Z_s}{Z_{in} + Z_s}\right|\right) \tag{3.14}$$

S_{11_LNA} often is designed to be less than -10dB (0.3) in practice, which means for the traveling wave, three tents (0.3) of the signal is reflected back to the source due to the impedance mismatch. For $Z_s = 50\Omega$, if Z_{in} is real impedance, $\mathrm{Re}(Z_{in})$ needs to be between

26Ω and 96Ω to achieve the input matching $S_{11\_LNA} < -10\text{dB}$. For $S_{11\_LNA} = -12\text{dB}$, if Z_{in} is real impedance, $\text{Re}(Z_{in})$ needs to be 30Ω or 86Ω.

The output S22 of the LNA can be calculated as

$$S_{22\_LNA} = 20\log\left(\left|\frac{Z_{out} - Z_1}{Z_{out} + Z_1}\right|\right) \tag{3.15}$$

For the standalone LNA, the output needs to be matched to the off-chip load impedance R_1. For the integrated receiver, the following stage of LNA is normally the on-chip Mixer. The input impedance of the Mixer is normally capacitive impedance with around hundreds of femto farads (fF). The output of the LNA is always designed as a resonate network. Since in the on-chip wireless receiver, the distance between the LNA and Mixer is normally smaller than the wavelength, which is around 76mm at 2GHz. Thus, there is less microwave effect from the interconnections; there is no need to match the output impedance.

The S21 represents the power gain of the amplifier.

$$S21 = G = \frac{P_o}{P_i} \tag{3.16}$$

The S12 is the reverse isolation parameter. It determines the level of feedback from the output of the LNA to the input of the LNA. In practice, the S12 is normally smaller than -30dB (0.03). The S-parameter of LNA for different standards and applications is illustrated with other specifications of the LNA as shown in Table 3. 1.

Table 3.1 LNA typical S-parameter

	Bluetooth/802.11b[21]	802.11a[22]	CDMA[23]
S11(dB)	-7	-15	-30
S21(dB)	14.7	12.5	13
S12(dB)	-25	~	-22
S22(dB)	-10	-9	-8.5
NF(dB)	2.88	3.7	1.65
IIP3(dB)	-1.5	-0.45	3
Bias current(mA)	14.7	8	5.4
Process	0.25µm CMOS	0.18µm CMOS	0.35µm BiCMOS

The above LNA results in Table 3.1 are from the published literature. We can find that all the different standards need S11 better than -10dB although some results does not satisfy this requirement. The power gain (S21) requirement of LNA is typical from 10dB to 25dB, which heavily depends on the communication system design requirement. If the following blocks of the system are very noisy, to have a better overall system noise, the LNA needs to have large gain. The S22 is not very critical for LNA (except the standalone LNA) in the wireless system. Typically the LNA is on-chip and followed by an on-chip Mixer. There is a small transmission line for the interconnect wire with short distance in silicon, and thus it is not necessary for the output of LNA to match the input of the Mixer. In this case, we can think the output load C_{L_LNA} is part of the output network of the LNA and the input of the mixer. C_{L_LNA} is dominated by the input capacitance of the Mixer C_{mixer}. If the S22 is still required to

calculate, replace the Z_L with C_{mixer} in (3.15) to calculate S22. The S12 represents the isolation of the LNA, which is typically better than -20dB (0.01).

3.1.3 Impedance Matching Network

As shown in Fig. 3.2b, a matching network is needed for the input impedance Z_{in} to match the antenna impedance 50Ω. Typically to transform the impedance from Z_1 to Z_2 for the impedance matching, different matching network can be applied [1], such as L matching network, π matching networks, and T matching network. The Smith Chart can also be used to accomplish the impedance matching.

First, the series RLC network to parallel RLC network conversion is analyzed. The networks are shown in Fig. 3.3. For Fig. 3.3(a), the impedance of the network is calculated as

$$Z_{in} = j\omega L_s + R_s = (j\omega L_p) // R_p = \frac{j\omega L_p R_p}{j\omega L_p + R_p} \tag{3.17}$$

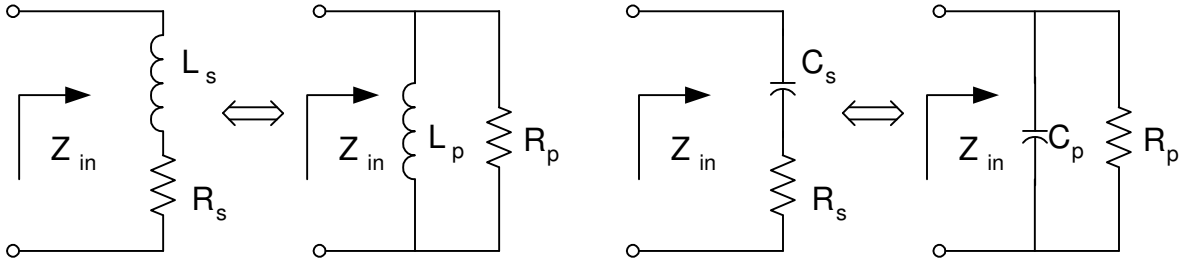


Fig. 3.3 Series connection to parallel connection conversion (a) LC network (b) RC network

When the real and the imaginary parts are equated, yields

$$R_p = R_s(Q^2+1) \tag{3.18}$$

$$L_p = L_s\left(\frac{Q^2+1}{Q^2}\right)\Bigg|_{Q>>1} \equiv L_s \tag{3.19}$$

where $Q = \frac{\omega_o L_s}{R_s} = \frac{R_p}{\omega_o L_p}$.

Similar results can be obtained for Fig. 3.3(b) following the same procedure.

When the real and the imaginary parts are equated, yields

$$R_p = R_s(Q^2+1) \tag{3.20}$$

$$C_p = C_s\left(\frac{Q^2}{Q^2+1}\right)\Bigg|_{Q>>1} \equiv C_s \tag{3.21}$$

where $Q = \frac{1}{\omega_o C_s R_s} = \omega_o C_p R_p$.

A). L matching network

The L matching network is used to transform real impedance to an arbitrary value, typically 50Ω. The total imaginary part will equal to zero after the matching network. The L-matching upward transform network is shown in Fig. 3.4 and it is to increase the equivalent value from R_s to $R_1=aR_s$, where a>1. R_1 is connected to L_s, C_1 and R_s, and L_s and C_1 are the matching network. Assuming the quality factor $Q = \omega_0 L_s / R_s$, the impedance relations between R_s and R_p in Fig.3.4 can be get from (3.18) as:

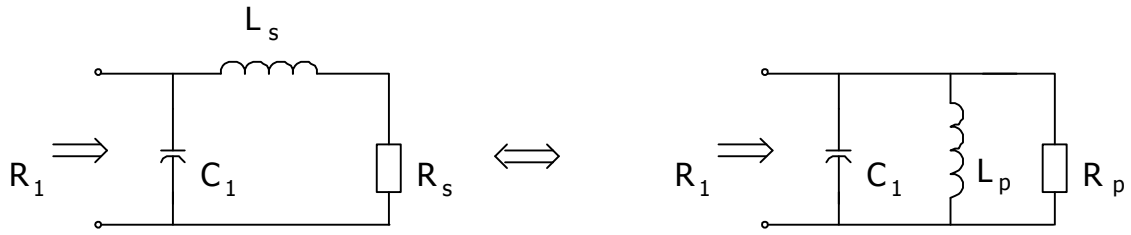


Fig. 3.4 L-matching upward transform network (a) Partial series (b) Equivalent parallel

The typical L match network from R_s to R_1 is shown in Fig. 3.4 and Fig. 3.5

$$R_1 = R_p = R_s(Q^2+1) \approx R_s Q^2 = R_s \frac{\omega_o^2 L_s^2}{R_s^2} = \frac{1}{R_s}\frac{L_s^2}{L_s C_1} = \frac{1}{R_s}\frac{L_s}{C_1} \tag{3.22}$$

The L-matching downward transform network is shown in Fig. 3.5 and it is to decrease the equivalent value from R_p to $R_1=aR_p$, where a<1.

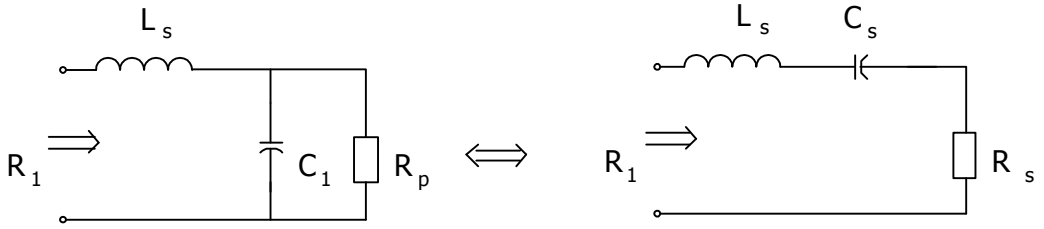


Fig. 3.5 L-matching downward transform network (a) Partial parallel (b) Equivalent series

Assuming the quality factor $Q = \omega_0 C_1 R_p$, the impedance relations between R_p and R_s in Fig.3.5 can be obtained from (3.19) as:

$$R_1 = R_s = \frac{R_p}{Q^2+1} \approx \frac{R_p}{Q^2} = \frac{R_p}{\omega_o^2 C_1^2 R_p^2} = \frac{L_s C_1}{C_1^2 R_p^2} = \frac{C_1}{L_s R_p} \tag{3.23}$$

Using the L-matching network, R_1 can be amplified or attenuated Q^2 times to R_p.

For the upward L-matching network in Fig. 3.4, the quality factor from (3.22) of the matching network relation with R_1 and R_s is

$$Q^2 \approx \frac{R_1}{R_s} \tag{3.24a}$$

For the downward L-matching network in Fig. 3.5, the quality factor from (3.23) of the matching network relation with R_1 and R_p is

$$Q^2 \approx \frac{R_p}{R_1} \tag{3.24b}$$

B). π matching network

The quality factor Q of the matching network is fixed for L matching network as seen in (3.24). If the difference between R_1 and R_2 is very large, it results in a large Q and smaller matching frequency bandwidth and may also vary a lot over the temperature or process variation. The π match network is an alternative that has an additional degree of freedom to choose the Q. The typical π match network from R_2 to R_1 is shown in Fig. 3.6.

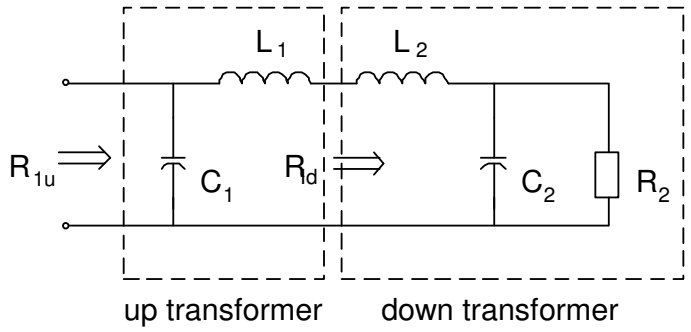


Fig. 3.6 π-matching network

Consider the cascade of two L matching network with the right L matching network. First the impedance R_2 is downward transformed to intermediate resistance R_{1d} by C_2 and L_2 as shown in Fig. 3.5. And then, R_{1d} is upward transformed to final resistance R_{1u} by L_1 and C_1 as shown in Fig. 3.4. The quality factor (Q_{right}) of the downward transformation from R_2 to R_{1d} by L_2 and C_2 can be obtained from (3.23) as

$$Q_{right} = \frac{\omega_o L_2}{R_{1d}} = \sqrt{\frac{R_2}{R_{1d}} - 1} \tag{3.25}$$

The quality factor (Q_{left}) of the upward transformation from R_{1d} to R_{1u} by L_1 and C_1 can be obtained from (3.22) as

$$Q_{left} = \frac{\omega_o L_1}{R_{1d}} = \sqrt{\frac{R_{1u}}{R_{1d}} - 1} \tag{3.26}$$

The π-matching network in Fig. 3.6 can be transformed to Fig. 3.7 to analyze the quality factor of the overall matching network.

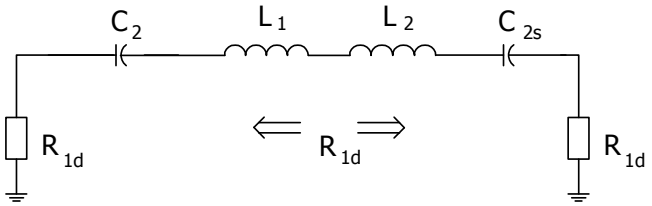


Fig. 3.7 π-matching equivalent network of Fig. 3.6

Either the left side resistance or the right side resistance is considered for the energy dissipation. Thus, the quality factor Q of the overall matching network is calculated as

$$Q = \frac{\omega_0 (L_1 + L_2)}{R_{1d}} = \sqrt{\frac{R_{1u}}{R_{1d}} - 1} + \sqrt{\frac{R_2}{R_{1d}} - 1} \tag{3.27}$$

The relation between R_{1d} and R_2 from (3.25) is

$$R_{1d} \approx \frac{R_2}{Q_{right}^{\ 2}} = R_2 \frac{C_2}{L_2} \tag{3.28}$$

The relation between R_{1d} and R_{1u} from (3.26) is

$$R_{1u} \approx Q_{Left}^{\ 2} R_{1d} = R_{1d} \frac{L_1}{C_1} \tag{3.29}$$

From (3.28) and (3.29), the relation between R_{1u} and R_2 is

$$R_{1u} \approx \frac{Q^2_{Left}}{Q^2_{right}} R_2 = R_2 \frac{L_1}{C_1} \frac{C_2}{L_2} \tag{3.30}$$

The advantage of (3.30) over (3.22) or (3.23) lies in that there is more freedom to choose quality factor of the impedance matching network, which can results in a wider bandwidth or robust matching network.

C). T matching network

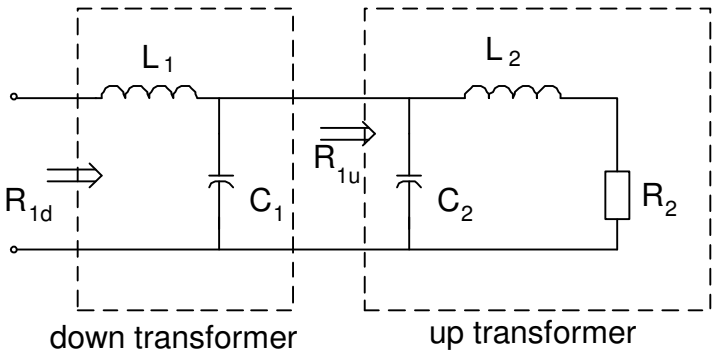


Fig. 3.8 T-matching network

The T matching network is obtained by cascading two L matching network in a different way from the π matching network. It is shown in Fig. 3.8.

It can be seen that the cascade of two L matching network is different from π-matching in Fig. 3.6. First the impedance R_2 is upward transformed to intermediate resistance R_{1u} by L_2 and C_2 as shown in Fig. 3.4. And then, R_{1u} is downward transformed to final resistance R_{1d} by C_1 and L_1 as shown in Fig. 3.5.

The quality factor (Q_{right}) of the upward transformation from R_2 to R_{1u} by L_2 and C_2 can be obtained from (3.22) as

$$Q_{right} = \omega_o C_2 R_I = \sqrt{\frac{R_{1u}}{R_2} - 1} \tag{3.31}$$

The quality factor (Q_{left}) of the upward transformation from R_{1u} to R_{1d} by L_1 and C_1 can be obtained from (3.23) as

$$Q_{left} = \omega_o C_1 R_I = \sqrt{\frac{R_{1u}}{R_{1d}} - 1} \tag{3.32}$$

The quality factor Q of the overall matching network is obtained similarly to π-matching.

$$Q = R_{1u}\omega_0 (C_1 + C_2) = \sqrt{\frac{R_{1u}}{R_{1d}} - 1} + \sqrt{\frac{R_{1u}}{R_2} - 1} \tag{3.33}$$

The relation between R_{1u} and R_2 is

$$R_{1u} \approx Q_{right}{}^2 R_2 = R_2 \frac{L_2}{C_2} \tag{3.34}$$

The relation between R_{1u} and R_{1d} is

$$R_{1u} \approx \frac{R_{1d}}{Q_{Left}{}^2} = R_{1d} \frac{C_1}{L_1} \tag{3.35}$$

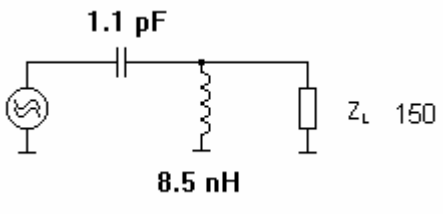
From (3.34) and (3.35), the relation between R_{1u} and R_2 is

$$R_{1d} \approx \frac{Q^2_{right}}{Q^2_{left}} R_2 = R_2 \frac{L_2}{C_2} \frac{C_1}{L_1} \tag{3.36}$$

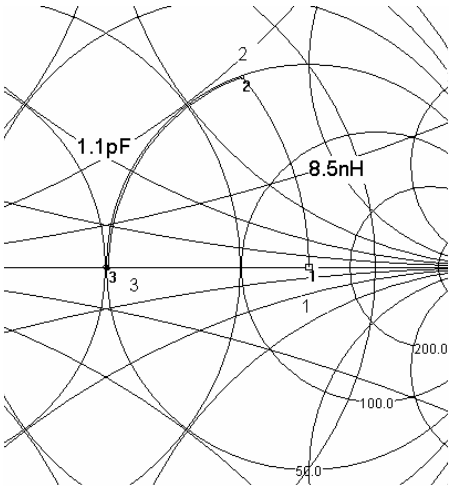
The impedance matching of (3.30) and (3.36) has the same function with the different connection with the network. The π network can absorb the parasitic capacitance and the T network can absorb the parasitic inductance.

The impedance matching can also be obtained using the graphic matching method, i.e. Smith Chart [1]. The Smith Chart is plotted on the complex reflection coefficient plane in two dimensions and is scaled in normalized impedance and/or normalized admittance. It can be used to present the impedance and also help to design the matching network, which is given in the following examples.

For example, to match a 150Ω resistor to a 50Ω resistor at 2GHz, it can be accomplished by Smith Chart method as show below:



(a)

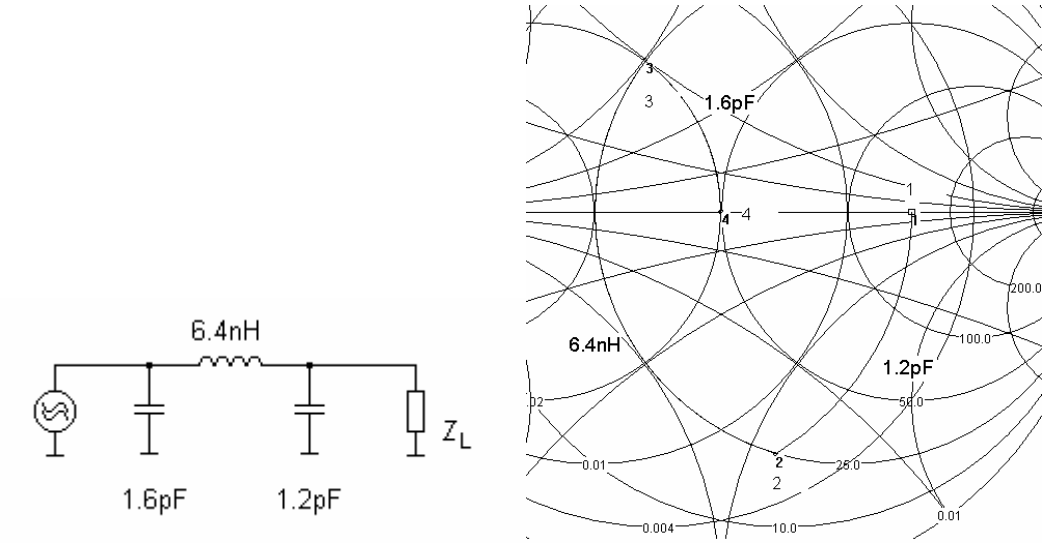


(b)

Fig. 3.9 (a) L-matching network and (b) Its Smith Chart

To transfer the resistance from point 1(150Ω) to point 3(50Ω) at 2GHz in Fig. 3.9(b), first a parallel inductor is added to transfer the impedance from point 1 to point 2 in the admittance circle. And then a series capacitor is added to transfer the impedance from point 2 to point 3 in the resistance circle. The resulting L-matching network is shown in Fig. 3.9(a).

It also can be down using the π-matching network as below:



(a) (b)

Fig. 3.10 (a) π-matching network and (b) Its Smith Chart

To transfer the resistance from point 1(150Ω) to point 4(50Ω) at 2GHz in Fig. 3.10(b), first a parallel capacitor (1.2pF) is added to transform the impedance from point 1 to point 2 in the admittance circle. And then a series inductor (6.4nH) is added to transfer the impedance from point 2 to point 3 in the resistance circle. Finally, a parallel capacitor (1.6pF) is added to transform the impedance from point 3 to point 4 in the admittance circle. It is a π-match network in Fig. 3.10(a). There are other alternative impedance matching networks, which are explained elsewhere [1].

3.1.4 Noise Figure of the LNA

A) Noise Figure Definition

The quality of the signal can be evaluated by signal-to-noise ratio (SNR), which is defined as the ratio of a signal power to the noise power corrupting the signal.

$$\mathrm{SNR} = \frac{P_{signal}}{P_{noise}} \tag{3.37}$$

During the amplification, RF LNA also adds noise in the signal which further corrupts the signal. The noise performance of the RF LNA is evaluated through the noise factor (F) or noise figure (NF). The noise factor describes the degradation of the incoming signal SNR due to the LNA. It is defined as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{\frac{S_{in}}{N_o}}{\frac{S_{out}}{N_{out}}} = \frac{S_{in}N_{out}}{S_{out}N_o} = \frac{N_{out}}{AN_o} \tag{3.38}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratio (SNR) at the input and the output, respectively. N_o (N_{out}) is the noise power at input (output).

The noise figure (NF) is the logarithm form of the noise factor (F) and used for the convenience.

$$NF = 10\log(F) \tag{3.39}$$

For illustration purposes, the NF of LNA for different applications is shown in Table 3.1.

B) Noise Factor of Two-port Network

A two port network model is very useful to calculate the noise of the system, which is shown in Fig. 3.11.

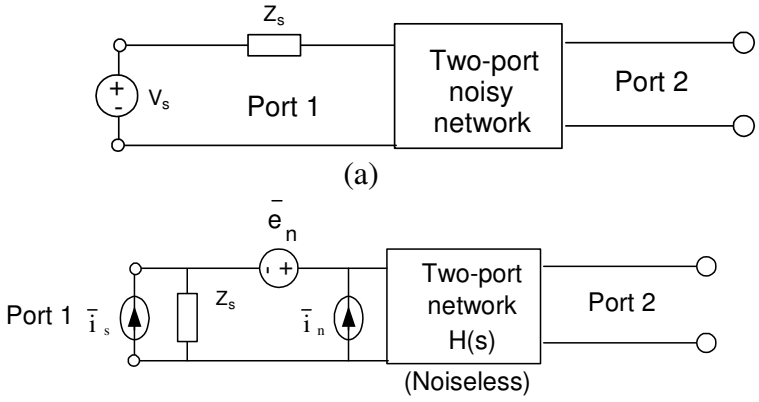


Fig.3.11 Two-port network noise model (a) Representation. (b) Equivalent two port with noise sources

The noisy two-port network is represented as a noiseless two-port network with external noise voltage source $\overline{e_n}$ and noise current source $\overline{i_n}$; and $\overline{i_s}$ is the equivalent shunt connected noise current of the source.

The noise factor can also be defined as

$$F = \frac{N_{out}}{AN_o} = \frac{\text{total output noise power}}{\text{output noise due to the input source}} = \frac{E_{out}}{E_{in}} \tag{3.40}$$

The total output noise power at port 2 due to the noise sources at port 1 and the noise sources in the circuits is

$$E_{out} = \left(\frac{\overline{i_s^2} + \overline{\left|i_n + e_n Y_s\right|^2}}{\left|Y(s)\right|^2}\right)\left|H(s)\right|^2 \tag{3.41}$$

where H(s) is the transfer function of the two-port network.

The noise power due to the input source is

$$E_{in} = \frac{\overline{i_s^2}}{\left|Y(s)\right|^2}\left|H(s)\right|^2 \tag{3.42}$$

The noise factor of the network shown in Fig. 3.11 is calculated as

$$F = \frac{E_{out}}{E_{in}} = \frac{\overline{i_s^2} + \overline{\left|i_n + e_n Y_s\right|^2}}{\overline{i_s^2}} \tag{3.43}$$

Assume that part of i_n is correlated with e_n, which is i_{cn}. The independent noise current is i_{un}.

$$i_n = i_{cn} + i_{un} \tag{3.44}$$

The source admittance Y_s and the correlation admittance Y_C are expressed as below

$$Y_s = G_s + jB_s \tag{3.45}$$

$$Y_C = G_C + jB_C \tag{3.46}$$

Using (3.44), (3.45) and (3.46), the noise factor in (3.43) can be rewritten as

$$F = \frac{\overline{i_s^2} + \overline{\left|i_n + e_n Y_s\right|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{\left|i_{un} + e_n (Y_c + Y_s)\right|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_{un}^2} + \left|(Y_c + Y_s)\right|^2 \overline{e_n^2}}{\overline{i_s^2}} \tag{3.47}$$

The source thermal noise current i_s can be expressed in term of the source conductance (G_s=1/R_s) as

$$\overline{i_s^2} = 4KTG_s\Delta f \tag{3.48}$$

where K is the Boltzmann constant, T is the absolute temperature and Δf is the frequency band which is often normalized to 1 rad/s.

The noise voltage e_n of the network can be expressed in term of the equivalent noise resistor R_n as

$$\overline{e_n^{\,2}} = 4KTR_n\Delta f \tag{3.49}$$

The independent noise current i_{un} of the network can be expressed in term of the equivalent noise conductance G_{un} as

$$\overline{i_{un}^{\,2}} = 4KTG_{un}\Delta f \tag{3.50}$$

Applying (3.48)-(3.50), (3.47) becomes

$$F = 1 + \frac{G_{un} + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \tag{3.51}$$

For (3.51), there is an optimum condition where noise factor F reaches the minimum value, where the system has the best noise performance. Taking the first derivative of (3.51) with respect to the Gs, and the optimum condition is obtained by setting the derivative to zero.

$$\begin{cases} B_s = -B_c \\ G_s = \sqrt{\dfrac{G_{un}}{R_n} + G_C^{\,2}} \end{cases} \tag{3.52}$$

Applying (3.52), the minimum noise factor (F_{min}) in (3.51) is obtained as

$$F_{min} = 1 + 2R_n[\sqrt{\frac{G_{un}}{R_n} + G_C^{\,2}} + G_c] \tag{3.53}$$

The impedance designed to satisfy (3.52) can make the system having minimal noise factor F, which is called noise matching. The impedance designed to satisfy (3.13) can make the system having maximum power, which is called power matching. The best design implies satisfying simultaneously the noise matching and the power matching. The practical design always involves the tradeoffs among the matching, noise, linearity, gain and power consumption.

C) Noise Figure of MOSFET Transistor

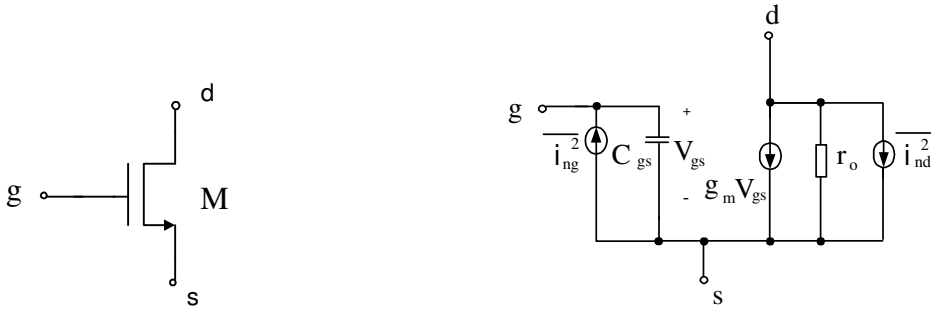


Fig. 3.12 (a) MOSFET transistor and (b) Noise model of the transistor

The MOSFET and its noise model are shown in Fig. 3.12, where

$$\overline{i_{nd}^2} = 4KT\gamma g_{d0}\Delta f \tag{3.54}$$

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \tag{3.55}$$

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \tag{3.56}$$

where K is the Boltzmann constant, T is the temperature, g_{do} is the drain source conductance at zero drain-source biasing, γ is 2/3 for long channel device in the saturation region and is

around 2-3 or even higher for short channel device, δ is typically around 4~6 [1]. For a given gate bias voltage V_{gs}, the g_{do} is simulated by the DC simulation with the drain terminal of the transistor is grounded. The operating point of the transistor M1 gives the drain source conductance g_{do} at zero drain-source biasing with $g_{do} = \left.\frac{\partial(I_d)}{\partial(V_{DS})}\right|_{V_{DS}=0}$.

The correlation coefficient C between the gate noise and the thermal noise is

$$C = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \tag{3.57}$$

The parameter c needs to be measured to know the exact relation between the thermal noise the gate induced noise. The procedure can be found in [24]-[25].

Here the number from the published books and literature are borrowed to analyze the noise of the circuits [1]. For the MOS transistor in the RF LNA which operates at high frequency, the flicker noise influence is usually ignored. Using the same approach as two-port network noise analysis in section 3.14-B, the following results can be obtained [1].

$$R_n = \frac{\gamma g_{d0}}{g_m^2} \tag{3.58}$$

$$Y_c = j\omega C_{gs}(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{3.59}$$

$$G_{un} = \frac{\delta\omega^2 C_{gs}^2(1-|c|^2)}{5g_{d0}} \tag{3.60}$$

where $\alpha = \frac{g_m}{g_{do}}$.

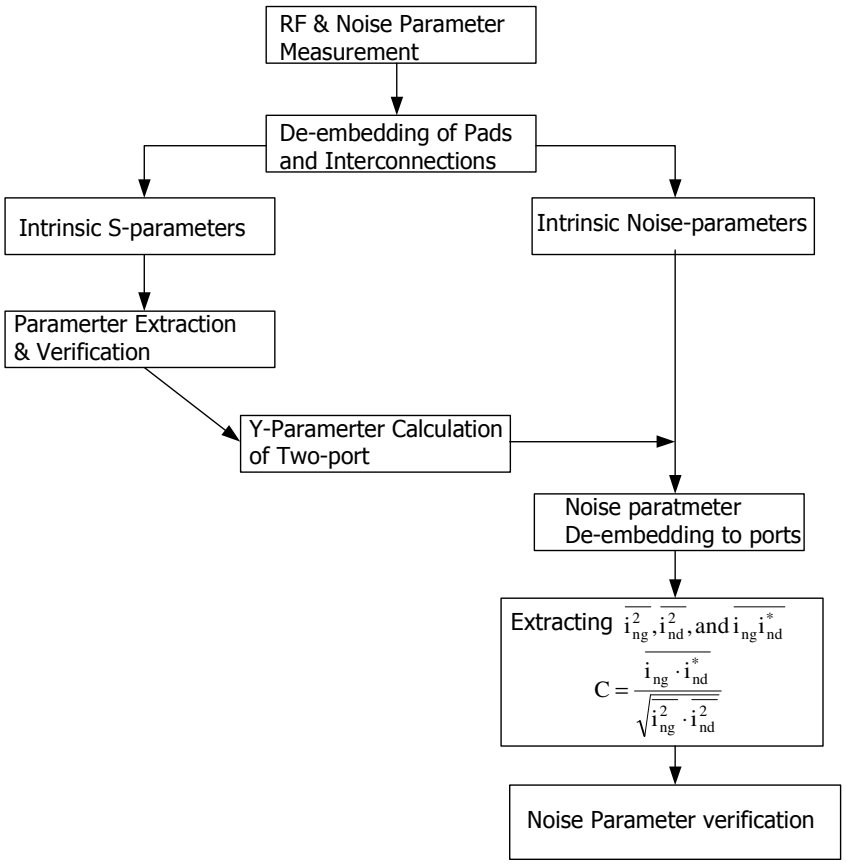


Fig. 3.13 Noise source extraction [24]-[25]

The noise factor becomes

$$F = 1 + \frac{G_{un} + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \tag{3.61}$$

The noise matching condition is

$$B_{opt} = -B_c = -\omega C_{gs}(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{3.62}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \alpha\omega C_{gs}\sqrt{(1 - |c|^2)\frac{\delta}{5\gamma}} \tag{3.63}$$

The minimal noise factor is

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] \approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{3.64}$$

The F_{min} vs ω for 0.5μm and 0.18μm are plotted in Fig. 3.14.

For $0.18\mu m, \alpha = 0.75, \gamma = 2.5, \delta = 5, c = -0.5j$, and $f_T = 56GHz$. For $0.18\mu m, \alpha = 1$, $\gamma = 2/3$, $\delta = 4/3$, $c = -0.395j$ and $f_T = 13GHz$.

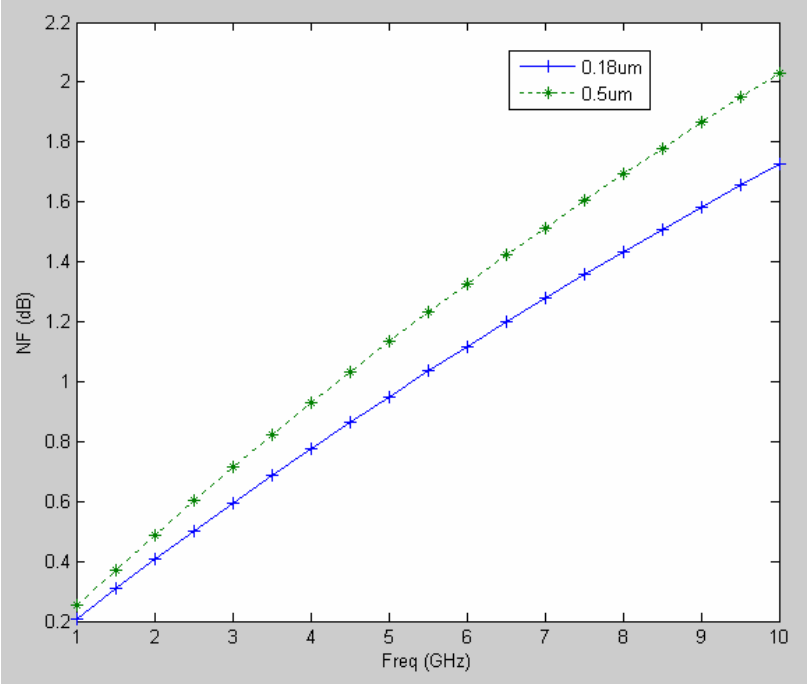


Fig. 3.14 NF_{min} vs ω for 0.5μm and 0.18μm

From (3.62), the optimum noise condition needs an inductive type source susceptance. The MOSFET transistor input impedance is capacitive. Thus, for the single MOSFET transistor, the noise matching (3.62)-(3.63) can not be achieved. Different typologies are proposed for LNA to achieve the optimum noise condition, which are discussed later.

D) The Influence of Noise Factor of LNA in the Cascade System

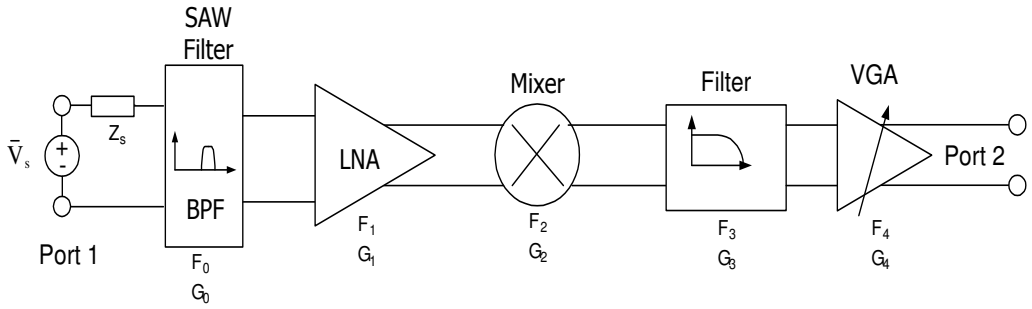


Fig.3.15 Cascode network for noise factor calculation

The SAW bandpass filter (BPF) is a passive circuit with loss a. The matching network before the LNA now is included in the LNA and becomes part of the LNA.

The BPF is modeled as shown in Fig. 3.16 with the equivalent input impedance R_{in} and the output impedance R_{out} [2].

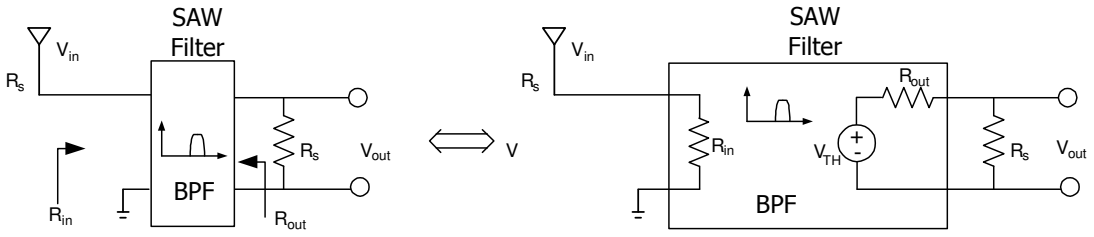


Fig.3.16 (a) Bandpass filter for noise calculation (b) Its equivalent circuit

The available input source power is

$$P_{avs} = \frac{V_{in}^2}{4R_s} \tag{3.65}$$

The output voltage is $V_{out} = \frac{R_s}{R_{out} + R_s} V_{TH}$ and the available output power is

$$P_{out} = \frac{V_{TH}^2}{4R_{out}} \tag{3.66}$$

where V_{TH} is the output voltage of the filter. The filter loss is decided by V_{TH} combined with V_{in}, R_{in}, and Rout.

The insertion loss is defined as

$$a = \frac{P_{in}}{P_{out}} = \frac{R_{out}}{R_s} \frac{V_{in}^2}{V_{TH}^2} \tag{3.67}$$

The output noise power is

$$V_{n,out}^2 = 4KT \frac{R_{out} R_L^2}{(R_L + R_{out})^2} \tag{3.68}$$

The voltage gain of the filter is

$$A_v = \frac{V_{TH}}{V_{in}} \frac{R_L}{R_L + R_{out}} = \frac{V_{out}}{R_s} \frac{(R_s + R_{out})R_L}{R_L + R_{out}} \tag{3.69}$$

The noise factor is calculated as

$$\begin{aligned} F &= \frac{\text{total output noise power}}{\text{output noise due to the input source}} = \frac{V_{n,out}^2}{4KTR_s A_v^2} \\ &= \frac{R_{out}}{R_s} \frac{V_{in}^2}{V_{TH}^2} = a \end{aligned} \tag{3.70}$$

From (3.70), the noise factor of the passive circuits or attenuator equals the loss in dB.

The RF system includes several blocks such as BPF, LNA, Mixer, Filter and VGA. For a cascade network shown in Fig. 3.15, the overall noise factor is calculated as

$$F = F_0 + \frac{F_1 - 1}{G_0} + \frac{F_2 - 1}{G_0 G_1} + \frac{F_3 - 1}{G_0 G_1 G_2} + \frac{F_4 - 1}{G_0 G_1 G_2 G_3} \tag{3.71}$$

where F_n and G_n (n=1, 2, 3, 4) are the noise factor and power gain of each stage. The gain G_0 and G_3 of the filter is negative in dB (or equivalent less than one in magnitude) due to the loss nature of these blocks. From (3.71), the noise factor of the LNA is almost directly added to the overall noise performance and the following stage noise contribution is attenuated by the previous stage gain. For instance, if the loss of the SAW filter is ignored, then F becomes

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \tag{3.72}$$

Thus the noise performance of the LNA largely influences the overall system noise performance. The examples of different system noise performances will be given together with the linearity performances later.

3.1.5 Linearity of the LNA

The nonlinearity of the LNA generates harmonics which are mixed at later stages with ω_{LO} and among the interferer signals. That is why a minimum of harmonics is desired for LNA. The linearity is an important design consideration, which is typically evaluated through harmonic distortion, 1dB compression point and the third order intercept point (IIP3).

A) Harmonic Distortion

For a nonlinear system, it is assumed with the following function up to 3rd order

$$Y_t = a_0 + a_1 X_t + a_2 X_t^{\,2} + a_3 X_t^{\,3} \tag{3.73}$$

where X_t is the input, Y_t is the output and a_n (n=0, 1, 2 and 3) are the coefficients.

If $X_t = A\cos(\omega t)$, the output signal Y_t is

$$\begin{aligned} Y_t &= a_0 + a_1 A\cos(\omega t) + a_2 (A\cos(\omega t))^2 + a_3 (A\cos(\omega t))^3 \\ &= a_0 + \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4} A\cos(3\omega t) \end{aligned} \tag{3.74a}$$

$$= b_0 + b_1\cos(\omega t) + b_2\cos(2\omega t) + b_3\cos(3\omega t) \tag{3.74b}$$

In (3.72) ignoring b_0, the term of $\cos(\omega t)$ is the fundamental frequency and the others are harmonic terms. The harmonic distortion factor (HD_i) is defined as the ratio of the output signal power of i^{th} harmonic term to that of the fundamental signal.

$$HD_i = \frac{b_i}{b_1} \tag{3.75}$$

For the nonlinear system as (3.71), assuming that $a_1 A >> \frac{3a_3 A^3}{4}$, we can get

$$HD_2 = \frac{b_2}{b_1} = \frac{a_2 A}{2a_1} \tag{3.76}$$

$$HD_3 = \frac{b_3}{b_1} = \frac{a_3 A^2}{4a_1} \tag{3.77}$$

B) 1dB Compression Point

The 1dB compression point is the input power level where the power gain from the input to the output reduces 1dB. It is shown in Fig. 3.17. Note that for this definition, we are not assuming that $a_1 A >> \frac{3a_3 A^3}{4}$.

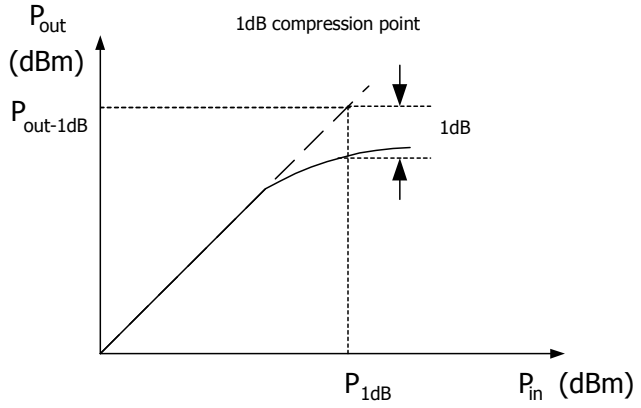


Fig.3.17 Definition of 1dB compression point

For the 1-dB compression point, it can be calculated from (3.74) and (3.78).

$$20\log\left|a_1 + \frac{3}{4}a_3 A_{1dB}^2\right| = 20\log|a_1| - 1 \tag{3.78}$$

$$P_{1-dB} = A_{1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \tag{3.79a}$$

The larger $P_{1\text{-}dB}$ is, the better linearity is expected.

The output 1-dB compression point is the output signal power when the input reaches the 1-dB compression point. It can be calculated as

$$P_{out-1dB} = a_1 \times P_{1-dB} = \sqrt{0.145\left|\frac{a_1^{\,3}}{a_3}\right|} \tag{3.79b}$$

C) Intermodulation and The Third-Order Intercept Point (IIP3)

While harmonic distortion is often used to describe the nonlinearity of analog circuits, there are certain cases where several input signals at different frequencies are applied to the nonlinear block, in those cases, the intermodulation of those frequencies become the linearity figure of merit. Thus, the intermodulation distortion in a two-tone test is introduced to characterize the linearity of the circuits. The LNA is a nonlinear operating device. When two tones signals at f_1 and f_2 are applied to the nonlinear device, there are also many other components besides the harmonic distortion factors, which are the intermodulation products.

For a nonlinear system, it is assumed with the following function up to 3rd order

$$Y_t = a_0 + a_1 X_t + a_2 X_t^{\,2} + a_3 X_t^{\,3} \tag{3.80}$$

If $X_t = A\cos(\omega_1 t) + A\cos(\omega_2 t)$, the output signal Y_t becomes

$$\begin{aligned} Y_t &= a_0 + a_1 A[\cos(\omega_1 t) + \cos(\omega_2 t)] + +a_2[A\cos(\omega_1 t) + A\cos(\omega_2 t)]^2 + a_3[A\cos(\omega_1 t) + A\cos(\omega_2 t)]^3 \\ &= (a_0 + a_2 A^2) + (a_1 A + \frac{9a_3 A^3}{4})\cos(\omega_1 t) + (a_1 A + \frac{9a_3 A^3}{4})\cos(\omega_2 t) + (\frac{a_2 A^2}{2})\cos(2\omega_1 t) \\ &\quad + (\frac{a_2 A^2}{2})\cos(2\omega_2 t) + (a_2 A^2)\cos((\omega_1 + \omega_2)t) + (a_2 A^2)\cos((\omega_1 - \omega_2)t) \\ &\quad + (\frac{3a_3 A^3}{4})\cos((2\omega_1 - \omega_2)t) + (\frac{3a_3 A^3}{4})\cos((2\omega_2 - \omega_1)t) + (\frac{3a_3 A^3}{4})\cos((2\omega_1 + \omega_2)t) \\ &\quad + (\frac{3a_3 A^3}{4})\cos((\omega_1 + 2\omega_2)t) + (\frac{a_3 A^3}{4})\cos(3\omega_1 t) + (\frac{a_3 A^3}{4})\cos(3\omega_2 t) \end{aligned} \tag{3.81}$$

The third-order intermodulation (IM3) is obtained from the coefficient of signals containing $(2\omega_1 \pm \omega_2)$ and $(2\omega_2 \pm \omega_1)$. According to (3.77) and (3.81), the IM3 is

$$\mathrm{IM3} = \frac{3a_3 A^2}{4a_1} = 3\mathrm{HD3} \tag{3.82}$$

From (3.81), assuming $a_1 A >> \frac{9a_3 A^3}{4}$ IIP3 can be calculated as

$$a_1 A_{\mathrm{IIP3}} = \left(\frac{3a_3 A_{\mathrm{IIP3}}^3}{4} \right) \tag{3.83}$$

$$A_{\mathrm{IIP3}} = \sqrt{\frac{4a_1}{3a_3}} \tag{3.84}$$

Second order intercept point (IIP2) is similar to the IIP3 and the second-order intermodulation (IM2) is obtained from the coefficient of signals containing $(\omega_1 - \omega_2)$ when $\omega_1 \geq \omega_2$. For two nearby interferers at ω_1 and ω_2, a low frequency signal $(\omega_1 \pm \omega_2)$ appears at the receiver output, which may influence the receiver system performance. The nonlinearity expression of a nonlinear system is summarized in Table 3. 2

Table 3.2 Nonlinearity expression for system with $Y_t = a_0 + a_1X_t + a_2X_t^2 + a_3X_t^3$

One tone signal input. $X_t = A\cos(\omega t)$	
Fundamental tone term	$a_1A + \frac{3a_3A^3}{4}$
Second order harmonic term	$\frac{a_2A^2}{2}$
Third order harmonic term	$\frac{a_3A^3}{4}$
HD_2	$\frac{a_2A}{2a_1}$
HD_3	$\frac{a_3A^2}{4a_1}$
P_{1dB}	$\sqrt{0.145\left\|\frac{a_1}{a_3}\right\|}$
$P_{out\text{-}1dB}$	$\sqrt{0.145\left\|\frac{a_1^3}{a_3}\right\|}$
Two tone signal input. $X_t = A\cos(\omega_1 t) + A\cos(\omega_2 t)$	
Fundamental tone term	$a_1A + \frac{9a_3A^3}{4}$
Second order harmonic term $(2\omega_1, 2\omega_2)$	$\frac{a_2A^2}{2} + \frac{3a_4A^4}{2}$
Second order intermodulation term $(\omega_1 + \omega_2, \omega_1 - \omega_2)$	$a_2A^2 + \frac{3a_4A^4}{2}$
Third order harmonic term $(3\omega_1, 3\omega_2)$	$\frac{a_3A^3}{4}$
Third order intermodulation term $(2\omega_1 + \omega_2, \omega_1 + 2\omega_2$, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$	$\frac{3a_3A^3}{4}$
IIP_3	$\sqrt{\frac{4a_1}{3a_3}}$
IM_3	$\frac{3a_3}{4a_1}A^2$

They are generated according to $mf_1 + nf_2$ (m, n=0, ±1, ±2, ±3…). The third-order intermodulation implies (m+n=3) (IM3) $2f_1 - f_2$ and $2f_2 - f_1$ fall into the signal band and are difficult to remove in the following analog and digital processing. The signal located in $2f_1+f_2$, $2f_2+f_1$ falls around twice the signal frequency, which can be easily filtered and are not important, as shown in Fig. 3.18.

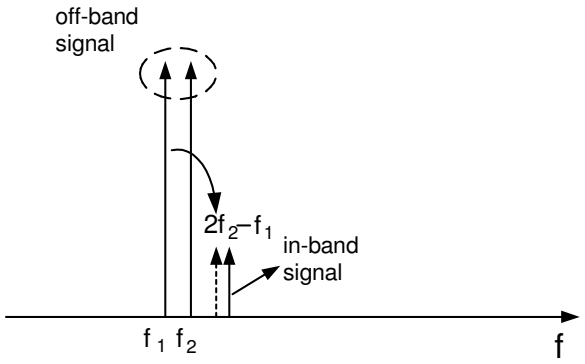


Fig. 3.18 Third-order intermodulation of two tones f_1 and f_2

The overall spectrum of the output signal if two tones ($A\cos(\omega_1 t)$ and $A\cos(\omega_2 t)$) are applied to the nonlinear amplifier is shown in Fig. 3.19. There is spectrum located at frequency $mf_1 + nf_2$ (m, n=0, ±1, ±2, ±3…) due to the harmonic or intermodulation.

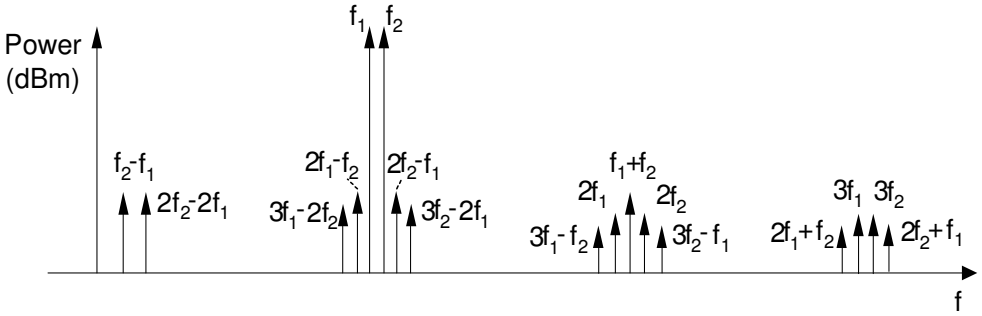


Fig. 3.19 Output signal spectrum with two tones signal inputs at f_1 and f_2

The third-order intercept point (IIP3) is the theoretical point where the desired signal and the third-order distortion have equal magnitudes. With two tone input at f_1 and f_2, the third-order intermodulation (IM) distortion is the power level at the output tone $2f_1$-f_2 and $2f_2$-f_1 due to the nonlinearity of the circuits. The IM3 and IIP3 are plotted in Fig. 3.20.

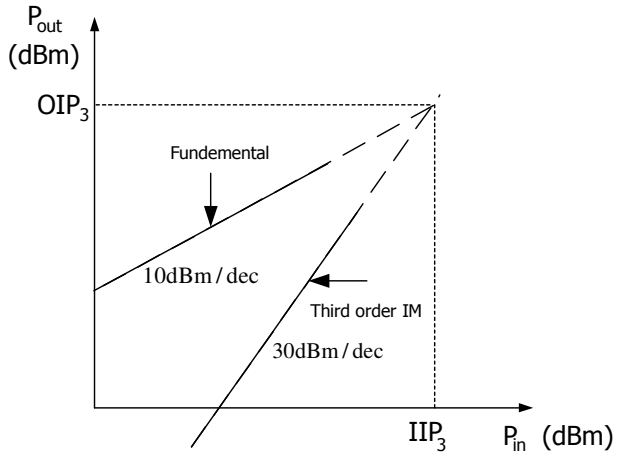


Fig. 3.20 Definition of third order intercept point (IIP3)

D) Dynamic Range (DR) and Spurious-Free Dynamic Range (SFDR):

Dynamic range (DR) is defined as the ratio of the maximum input signal level that the circuit can tolerate to the minimum input level [2]. The spurious-free dynamic range (SFDR) is defined as the ratio of the fundamental signal tone and the highest spur in the bandwidth of interest. The dynamic range is calculated using (3.85)

$$DR_{1dB} = P_{1dB} - P_{mds} \tag{3.85}$$

where P_{mds} is the minimal detectable signal, which is defined as

$$P_{mds} = -174\text{dBm} + 10\log B + NF \tag{3.86}$$

The SFDR is calculated using (3.87)

$$SFDR = \frac{2}{3}(IIP3 - P_{mds}) \tag{3.87}$$

The SFDR is plotted in Fig. 3.21.

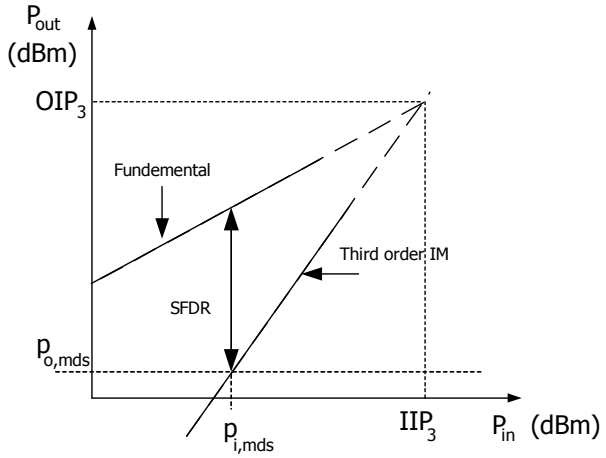


Fig. 3.21 Definition of spurious-free dynamic range (SFDR)

E) Influence of the LNA Linearity in the Cascade System

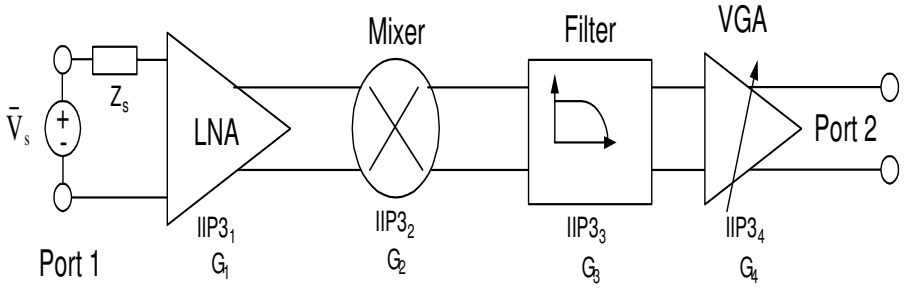


Fig. 3.22 (a) Cascade network for IIP3 calculation

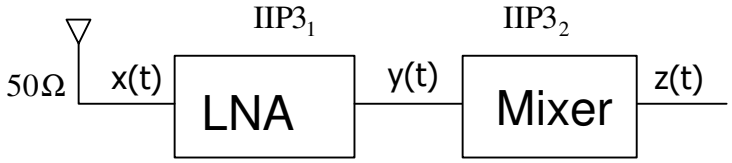


Fig. 3.22 Continued. (b) The first two stage cascade network for IIP3 calculation

If the input-output relation of the LNA and Mixer are

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{3.88}$$

$$z(t) = b_1 y(t) + b_2 y^2(t) + b_3 y^3(t) \tag{3.89}$$

z(t) can be obtained as

$$\begin{aligned} z(t) &= c_1 x(t) + c_2 x^2(t) + c_3 x^3(t) + c_4 x^4(t) + c_5 x^5(t) + c_6 x^6(t) + c_7 x^7(t) + c_8 x^8(t) + c_9 x^9(t) \\ &= b_1[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)] + b_2[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)]^2 + b_3[a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)]^3 \\ &= b_1 a_1 x(t) + \left(b_1 a_1 + b_2 a_1^2\right) x^2(t) + \left(b_1 a_3 + 2a_1 a_2 b_2 + a_1^3 b_3\right) x^3(t) + \left(b_2 a_2^2 + 2a_1 a_3 b_2 + 3a_1^2 a_2 b_3\right) x^4(t) \\ &+ \left(2b_2 a_2 a_3 + 2a_1^2 a_3 b_3 + 3a_1 a_2^2 b_3\right) x^5(t) + \left(b_2 a_3^2 + a_2^3 b_3 + 6a_1 a_3 a_3 b_3\right) x^6(t) + \left(3a_1 a_3^2 b_3 + 3a_2 a_3^2 b_3\right) x^7(t) \\ &+ 3a_2 a_3^2 b_3 x^8(t) + a_3^2 b_3 x^9(t) \end{aligned} \tag{3.90}$$

We can define

$$c_1 = a_1 b_1 \tag{3.91}$$

$$c_3 = a_3 b_1 + 2a_1 a_2 b_2 + a_1^3 b_3 \tag{3.92}$$

According to (3.84), the IIP3 of the two stage cascode network is

$$\frac{1}{A_{IP3}^2} = \frac{3}{4}\frac{|c_3|}{|c_1|} = \frac{3}{4}\frac{|a_3 b_1| + 2|a_1 a_2 b_2| + |a_1^3 b_3|}{|a_1 b_1|} \tag{3.93}$$

Since a_1, b_1 are the largest, the second term in the nominator is ignored, thus (3.93) becomes

$$\frac{1}{A_{IP3}^2} = \frac{3}{4}\frac{|a_3 b_1| + |a_1^3 b_3|}{|a_1 b_1|} = \frac{1}{A_{IP3_1}^2} + \frac{a_1^2}{A_{IP3_2}^2} \tag{3.94a}$$

$$\frac{1}{A_{IP3_1}^2} = \frac{3}{4}\frac{|a_3|}{|a_1|} \tag{3.94b}$$

$$\frac{1}{A_{IP3_2}^2} = \frac{3}{4}\frac{|b_3|}{|b_1|} \tag{3.94c}$$

where a_1 is the voltage gain of the LNA and A_{IP3} is the input IP3 point (voltage quantities).

In power quantities, the relation between A_{IP3} and IIP3 is

$$IIP3 = \frac{A_{IP3}^2}{4R_s} \tag{3.95a}$$

where R_s is the source impedance. (3.94) becomes

$$IIP3 = \left(\frac{1}{IIP3_1} + \frac{G_1}{IIP3_2}\right)^{-1} \tag{3.95b}$$

where $IIP3_n$ and G_n (n=1, 2) are the third order input intercept point (IIP3) and the gain of each stage.

By induction, for the cascade network in Fig. 3.22(a), the overall IIP3 is calculated as

$$IIP3 = \left(\frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \frac{G_1 G_2 G_3}{IIP3_4}\right)^{-1} \tag{3.96}$$

where $IIP3_n$ and G_n (n=1, 2, 3, 4) are the third order input intercept point (IIP3) and the gain of each stage. The IIP3 of the BPF of Fig. 3.15 is typically very large due to the linear passive components and thus is not considered.

From (3.96), the linearity of the receiver is heavily influenced by the stages after the LNA. The signal is amplified by LNA which makes the nonlinearity of the following stage more dominant.

Note that noise and linearity have contradictory goals, i.e. increasing G1 and G2 will improve the noise according to (3.72), but will degrade the linearity according to (3.96).

As an example, the noise and linearity for Bluetooth and Wi-Fi receiver are summarized in Table 3.3 [26].

Table 3.3 NF and linearity distribution in Bluetooth/Wi-Fi mode [26]

	Bluetooth			Wi-Fi		
	NF(dB)	IIP3(dBm)	IIP2(dBm)	NF(dB)	IIP3(dBm)	IIP2(dBm)
LNA	3	-8	11	3	-8	11
Mixer	20	5	48	15	5	48
Filter	36	23	64	32	23	64
VGA	30	10	31	30	10	31
ADC	57	10	41	65	10	41
System	9.49	-13.5	26.7	6.46	-13.5	26.7

The IIP3 and IIP2 in Table 3.3 are same for [26]. Since it is dual-mode (Bluetooth-WiFi) receiver architecture, the worst case is used to decide the specification of each block, which can satisfy both standards. In the reality, it is not necessary the same for different standards.

3.2 LNA Topologies

According to its operating frequency bandwidth, the impedance matching network and its application, the LNA can be roughly divided into narrowband LNA and wideband LNA. If the impedance matching network is narrowband, it is called narrowband LNA. If the impedance matching network is wideband, it is called wideband LNA. The narrowband LNA is first discussed in the following sections.

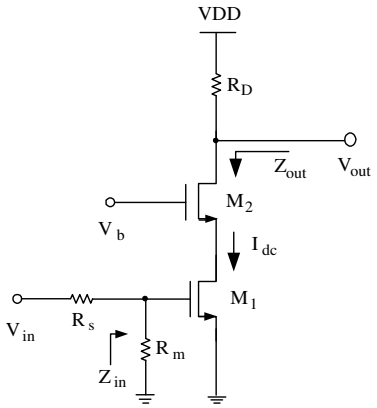
3.2.1 Narrowband LNA

Many wireless applications are narrowband applications, such as GSM, Bluetooth and Wireless LNA. The frequency bandwidth for GSM is 200kHz in 900MHz frequency [27]. The frequency band for Bluetooth is 83.5MHz (2400MHz-2483.5MHz) [28]. The frequency band for 802.11b and 802.11g is 83.5MHz (2400MHz-2483.5MHz) [28]. The frequency band for 802.15.4 ZIGBEE is 26MHz (902MHz-928MHz) and 78MHz (2402MHz-2480MHz) in North America [29].

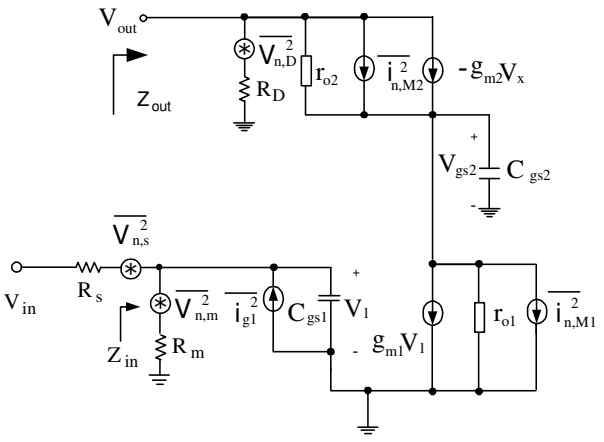
There are different topologies suitable for narrowband applications, among which the simplest one is the resistive termination LNA [1] and the most popular one is inductively degenerated common source LNA (CS-LNA) [1], [30] because it uses a noiseless component to achieve the input resistance matching and thus has better noise performance.

3.2.1.1 Resistive Termination LNA

The simplest LNA is a resistive termination LNA, shown in Fig. 3.23. The shunted resistor R_m is added to achieve the input impedance matching, (R_m=R_s). This LNA can be used in both narrowband and wideband applications.



(a)



(b)

Fig. 3.23 Resistive termination LNA (a) Circuits diagram and (b) Equivalent circuit for noise computation

The minimum power supply required for the resistive termination LNA is calculated as

$$VDD \geq V_{dsat1} + V_{dsat2} + R_D \times I_{dc} + V_{om} \tag{3.97}$$

where V_{om} is the output maximum voltage swing. For example, in an example for 0.35μm CMOS LNA: V_{dsat1}=0.2V, V_{dsat2}=0.2V, I_{dc}=3mA, R_D=200Ω, the maximum output swing is 0.2V, then the power supply voltage becomes $VDD \geq 1.2V$.

Since the LNA using the noisy resistor to implement the input matching, it has the worse noise performance among LNA topologies. The noise factor of the LNA is derived as below:

The output noise due to the noise source resistor, R_s, is

$$V_{n,s}^2 = KTR_s A_v^2 \left(\frac{g_{m2}}{g_{m2} + sC_{gs2}} \right)^2 = KTR_s (g_{m1} R_D)^2 \left(\frac{g_{m2}}{g_{m2} + sC_{gs2}} \right)^2 \tag{3.98}$$

where $A_v \cong g_{m1} R_D$ and $R_D << Z_{out}$.

The output noise due to the noise match resistor $R_m(=R_s)$ is

$$V_{n,m}^2 = KTR_s (g_{m1} R_D)^2 \left(\frac{g_{m2}}{g_{m2} + sC_{gs2}} \right)^2 \tag{3.99}$$

The output noise due to the thermal noise of M1 is

$$i_{n,m1}^2 = 4KT \frac{\gamma}{\alpha} g_{m1} \left(\frac{g_{m2}}{g_{m2} + sC_{gs2}} \right)^2 \tag{3.100}$$

where γ is 2/3 for long channel device in the saturation region and is around 2-3 or even higher for short channel device [1]. $\alpha = \frac{g_m}{g_{do}}$, which is typically 1 for long channel device and smaller than one for short channel device.

The output noise due to the load resistor, R_D, is

$$V_{n,s}^2 = KTR_D \tag{3.101}$$

The output noise due to the thermal noise of M2 is

$$i_{n,m2}^2 = 4KT\frac{\gamma}{\alpha}g_{m2}\left(\frac{sC_{gs2}}{g_{m2}+sC_{gs2}}\right)^2 \tag{3.102}$$

where K is the Boltzmann constant, T is the temperature, and g_{do} is the drain source conductance at zero drain-source biasing. If Cgs2 is smaller and $g_{m2}=g_{m1}$, then $i_{n,m2}^2 << 1$.

The noise voltage from R_D is attenuated by the LNA gain. The noise voltage transfer function of M2 is smaller due to the source degeneration of M_1 in M_2. Both of them are ignored for simplicity. The noise factor of the LNA yields

$$F = \frac{\text{total output noise}}{\text{noise due to the source resistor}} \geq \frac{V_{n,s}^2 + V_{n,m}^2 + V_{n,m1}^2 + V_{n,D}^2 + V_{n,m2}^2}{V_{n,s}^2} \tag{3.103}$$

The noise form the output resistor R_D is attenuated by the LNA gain A_v. The noise contribution for the cascode transistor M_2 relies on the ratio of g_{m2}/sC_{gs2}, which is typically smaller and ignored. If $V_{n,D}^2$ and $V_{n,m2}^2$ are ignored, (3.103) becomes

$$F = 1 + \frac{R_m^2}{R_s^2} + \frac{4\gamma}{\alpha g_{m1} R_s} \tag{3.104}$$

From (3.104), we can find the noise factor improves with the decreasing of the matching resistor R_m. The power gain of the LNA reduces with the decreasing of the matching resistor R_m. There is a tradeoff between the noise and the power transfer.

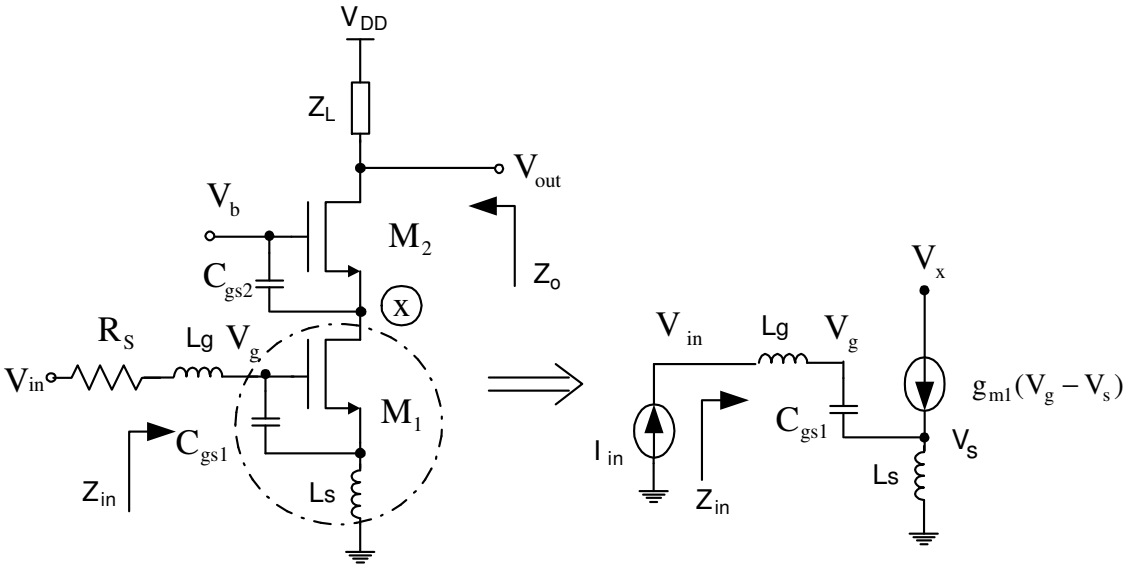
If the input impedance R_m is matched to R_s, the noise factor has following relation.

$$F \geq 2 + \frac{4\gamma}{\alpha g_{m1} R_s} \tag{3.105}$$

It has very good input impedance matching while has a NF greater than 6dB. This characteristic limits its application.

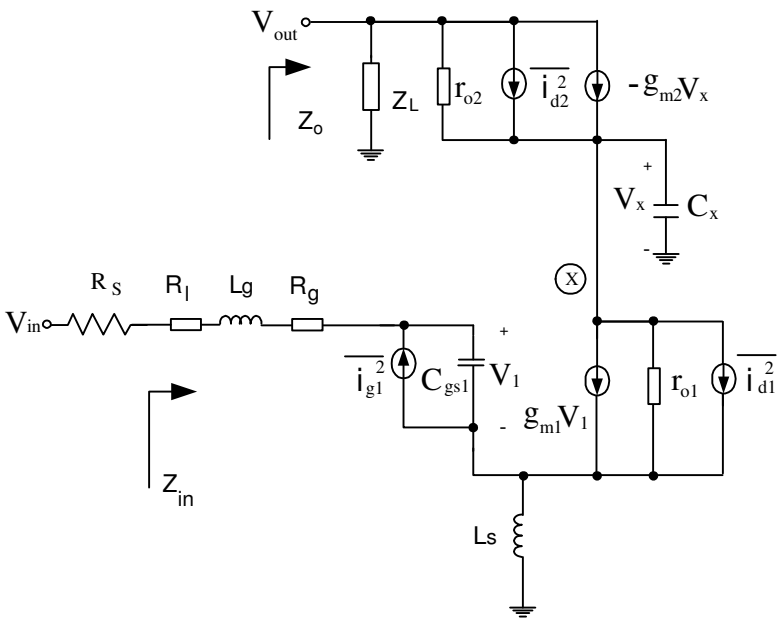
3.2.1.2 Common Source LNA (CS-LNA)

The typical inductively degenerated CS-LNA [1] [30] is shown in Fig. 3.24. In Fig. 3.24, all parasitic capacitances other than the gate-source capacitances of M_1 and M_2 are ignored for simplicity.



(a) (b)

Fig. 3.24 (a) Inductively degenerated cascode CS-LNA (b) Equivalent small signal model of the LNA input network



(c)

Fig. 3.24 Continued. (c) Noise equivalent circuit

The minimum power supply required for the resistive termination LNA is calculated as

$$VDD \geq V_{dsat1} + V_{dsat2} + V_{L_s} + V_{Z_L} + V_{om} \tag{3.106}$$

where V_{Ls} is the voltage drop across the inductor L_s, V_{ZL} is the voltage drop across the LNA load Z_L, and V_{om} is the maximum output signal swing.

For example, in an example for 0.35µm CMOS LNA: V_{dsat1}=0.2V, V_{dsat2}=0.2V, I_{dc}=3mA, the load R_D=200Ω, which is typically parallel with a inductor L_D and consumes no voltage headroom, the voltage headroom from the source degenerated inductor L_s, the maximum output swing is 0.2V, then the power supply voltage becomes $VDD \geq 0.6V$. This LNA can be fit for Vdd=1V.

It uses an inductor L_s to generate the real impedance to match the input impedance of 50Ω, which results in good noise performance [1]-[2], [30]-[32]. If the resistive losses in the signal path, gate resistance, and parasitic capacitances except gate-source capacitances are ignored, the overall input impedance of CS-LNA can be derived from Fig. 3.24(b).

Applying KCL and KVL to the equivalent circuit in Fig. 3.24(b), we can get

$$V_{gs} = \frac{I_{in}}{sC_{gs1}} \tag{3.107}$$

$$V_{in}(s) = I_{in}(s)(sL_g + \frac{1}{sC_{gs1}} + sL_s) + I_{in}(s)g_{m1}\frac{L_s}{C_{gs1}} \tag{3.108}$$

The equivalent input impedance $Z_{in}(s)$ is obtained as

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = sL_g + sL_s + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}} \tag{3.109}$$

where g_{m1} is the transconductance of M_1.

Since the noise voltage source at the gate terminal of M2 has large source impedance degeneration by the output impedance of M1, the noise of M2 does not transfer to the LNA output. If the noise contribution from the cascode stage is ignored, the noise factor of the cascode CS-LNA of Fig. 3.24(c) becomes [30]-[32]

$$F_{CS} = 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\frac{\omega_o}{\omega_T} \tag{3.110}$$

$$\chi = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + {Q_L}^2) \tag{3.111}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g}^2 \overline{i_d}^2}} \tag{3.112}$$

$$Q_L = \frac{Q}{2} = \frac{\omega_o (L_s + L_g)}{R_s} = \frac{1}{\omega_o C_{gs} R_s} \tag{3.113}$$

where R_s is the input voltage source resistance, R_1 represents the series resistance of the inductor L_g, R_g is the gate resistance of M_1, ω_o is the operating frequency, and α, γ and δ are bias-dependant parameters [30]-[32].

If R_1 and R_g are ignored, applying (3.18), (3.110) becomes

$$\begin{aligned} F_{CS} &= 1 + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\frac{\omega_o}{\omega_T} = 1 + \frac{\gamma}{\alpha}\frac{\omega_o}{\omega_T}\frac{1}{Q_L}\left(1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L{}^2)\right) \\ &= 1 + (\frac{\omega_o}{\omega_T})\frac{\gamma}{\alpha}\frac{1}{2Q}(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2) \end{aligned} \tag{3.114}$$

where $\chi_d = \alpha\sqrt{\frac{\delta}{5\gamma}}$ and $Q = \frac{Q_L}{2} = \frac{1}{2R_s\omega_o C_{gs1}}$

The difference between Q and QL is that the Q considers the source impedance R_s and Q_L does not consider Rs.

Typically γ is 2/3 for long channel device in the saturation region and is around 2-3 or even higher for short channel device [1]. $\alpha = \frac{g_m}{g_{do}}$, which is typically 1 for long channel device and smaller than one for shout channel device. δ is typically around 5. c is typically -0.395j for long channel and larger for short channel device [1] [30]. Also typical values of R_g, R_s, Q_L and χ is 1-2Ω, 50Ω, 2~5 and 4 respectively.

3.2.1.2.1 CS-LNA Design Procedure

First, a design example for LNA is given and then the design flow is summarized in Fig. 3.29. In this design example, an inductively degenerated Common Source LNA (CS-LNA) will be designed using a 0.18µm CMOS technology to show the LNA design procedure. The design target is to have an LNA working at 2.4 GHz band with less than 2 dB Noise Figure (noise factor: 1.58), -10dBm IIP3, voltage gain greater than 15 dB and consuming less than 18mW, that is 10mA current from a 1.8 V power supply.

Step 1: Calculate Q

For the design, the Noise Figure (NF) should be used as a design parameter to be satisfied. Here, we just try to identify the best Noise Figure that the CS-LNA can be obtained and use that condition to design the LNA. The specified NF LNA design can also be done following the same procedure.

The noise factor of the inductively degenerated CS-LNA of Fig. 3.24(a) is

$$F_{CS} = 1 + \left(\frac{\omega_o}{\omega_T}\right)\frac{\gamma}{\alpha}\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right) \tag{3.115}$$

where

$$\chi_d = \alpha\sqrt{\frac{\delta}{5\gamma}} \tag{3.116}$$

$$Q = \frac{1}{2R_s\omega_o C_{gs1}} \tag{3.117}$$

The noise factor scaling coefficient is given by

$$\kappa_{nf} = \frac{\gamma}{\alpha}\frac{1}{2Q}(1-2|c|\chi_d + (4Q^2+1)\chi_d^2 \tag{3.118}$$

The noise factor in (3.115) can be rewritten as

$$F_{CS} = 1 + (\frac{\omega_o}{\omega_T})\kappa_{nf} \tag{3.119}$$

From (3.119), the noise factor scaling coefficient is the main influence term of the noise factor. Since the NMOS transistor M1 in Fig. 3.24a is normally a multi-finger transistor, the NMOS transistor W=1μm and L=0.18μm is used to estimate ω_T. The transistor size (W=1μm and L=0.18μm) and the gate bias voltage V_g (0.8V) is used just to get an estimation. From the simulation of the NMOS transistor (W=1μm and L=0.18μm) with gate bias voltage V_g at 0.8V, we can get $g_u=g_{m1}/W=444\mu S$ and $C_u=C_{gs1}/W=1.26fF$. The g_m and C_{gs1} is estimated in first order as

$$g_m = \sqrt{\mu_n C_{ox}\frac{W}{L}I_D(1+\lambda V_{ds})} \tag{3.120}$$

$$C_{gs1} = \frac{2}{3}\mu_n C_{ox} WL \tag{3.121}$$

The transconductance can be estimated from

$$\omega_T \approx \frac{g_u}{C_u} = \frac{g_{m1}}{C_{gs1}} = 2\pi(56GHz) \tag{3.122a}$$

or

$$g_{m1} = \omega_T C_{gs1} \tag{3.122b}$$

Here the gm and Cgs1 are obtained using the simulation. The complex device model is avoided in the design. The design will be corresponding modified through the circuit

simulation, since the transistor size used in the circuit will be much larger than the unit transistor size (W=1μm and L=0.18μm).

Here, we use the parameters values as α=0.75, γ=2.5, δ=5 and c=-0.5j [1]. And then $\chi_d = \alpha\sqrt{\frac{\delta}{5\gamma}} = 0.47$. These numbers are assumptions for 0.18 μm CMOS process according to the experience and the published literature. The design will be modified through the simulation.

For the LNA operating in 2.4GHz, the relation between the noise factor scaling coefficient and Q is shown in Fig. 3.25. The expression used is (3.115).

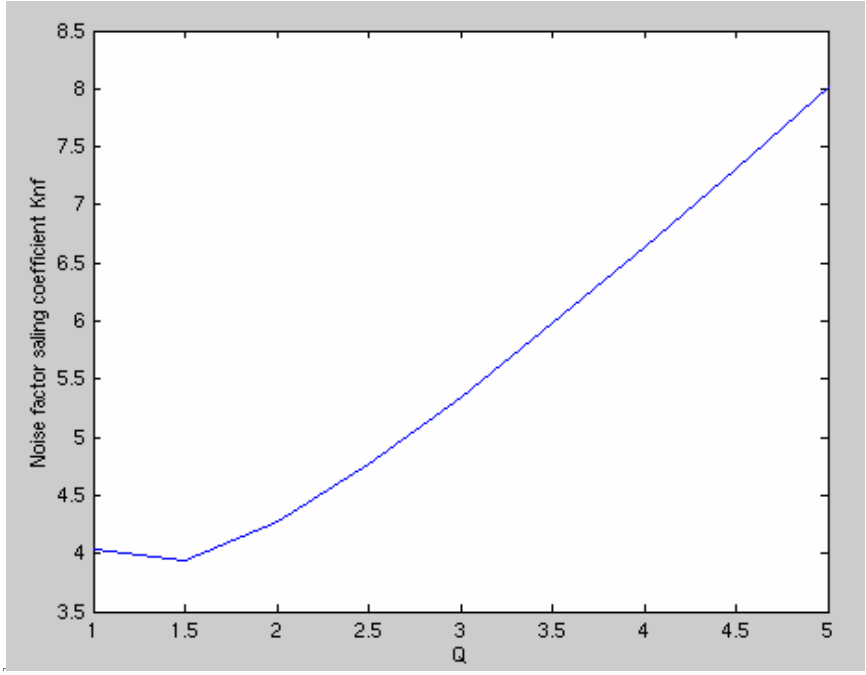


Fig. 3.25 Noise factor scaling coefficient versus Q of CS-LNA (see 3.112)

From Fig. 3.25, the noise factor scaling coefficient κ_{nf} has the minimal value at Q=1.5. From Fig. 3.25 and (3.96), the LNA has minimal noise factor when Q is chosen as 1.5. Now, only the Q is fixed. We need to calculate the C_{gs1} and W of the transistor.

Step 2: Calculate C_{gs1}, L_s and L_g

The quality factor of the input matching network is Q=1.5.

Using (3.117), the required C_{gs1} of transistor M_1 is

$$C_{gs1} = \frac{1}{2\pi R_s \omega_o Q} = 140\text{fF} \tag{3.123}$$

According to (3.111), the input impedance matching condition for LNA is

$$\omega_o\left(L_g + L_s\right) - \frac{1}{\omega_o C_{gs1}} = 0 \tag{3.124}$$

$$R_s = g_{m1}\frac{L_s}{C_{gs1}} \approx \omega_T L_s \tag{3.125}$$

From (3.125), the degenerated inductor value is

$$L_s = \frac{R_s}{\omega_T} = 0.14\text{nH} \tag{3.126}$$

From (3.124), the gate inductor value is calculated as

$$L_g = \frac{1}{\omega_o^2 C_{gs1}} - \frac{R_s}{\omega_T} = 31\text{nH} \tag{3.127}$$

Step 3: Transistor M_1 Size and Bias Current of M_1

From the DC simulation of the NMOS transistor as in step 1, by measuring the DC operating point of the transistor, we can get the unit $C_u=C_{gs1}/W$ of a NMOS transistor (W=1μm and L=0.18μm). It is around 1.26fF. According to (3.123), Cgs1=140fF is required for Q=4. The transistor size is calculated as

$$W = \frac{C_{gs1}}{C_u} = \frac{140}{1.26} \approx 110\mu m \tag{3.128}$$

From the DC simulation, by measuring the operating point of the transistor, we can obtain the unit bias current ($I_u=I_{bias}/W$). Through the simulation of a normalized NMOS transistor (W=1μm and L=0.18μm), the unit bias current (I_u) of a NMOS transistor is 85μA/μm. And then the bias current is calculated as

$$i_{bais} = I_u \times W = 85 \times 110\mu A = 9.4mA \tag{3.129}$$

Step 4: LNA Load (Z_L)

The equivalent input network of the CS-LNA is shown in Fig.3.25.

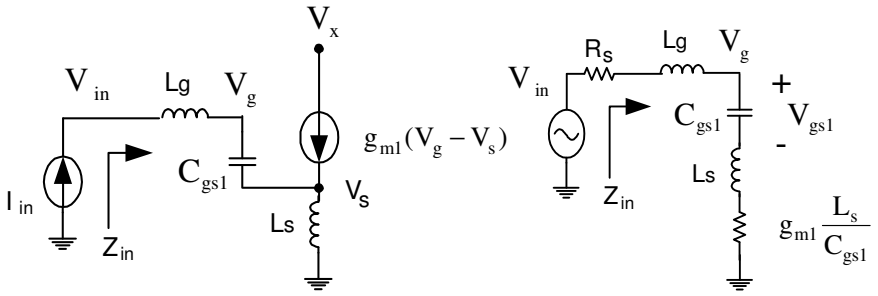


Fig.3.26 The input stage of the CS-LNA (a) Small signal model (b) Equivalent input network

From Fig. 3.26, the overall output current of the CS-LNA is calculated as

$$i_{d\_M1} = g_{m1} V_{gs1} = g_{m1} V_{in} \frac{\frac{1}{sC_{gs1}}}{R_s + s(L_g + L_s) + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}}} \tag{3.130}$$

The overall transconductance of the CS-LNA is

$$G_{CS-LNA} = \frac{i_{d\_M1}}{V_{in}} = \frac{g_{m1} V_{gs1}}{V_{in}} = g_{m1} \frac{\frac{1}{sC_{gs1}}}{R_s + s(L_g + L_s) + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}}} \tag{3.131}$$

When the input of the CS-LNA is matched at frequency ω_o, equations (3.124)-(3.125) hold true. Applying (3.124)-(3.125), (3.131) becomes

$$G_{CS-LNA} = g_{m1} \frac{1}{2R_s \omega_o C_{gs1}} = \frac{\omega_T}{2R_s \omega_o} = g_{m1} Q \tag{3.132}$$

where Q is the quality factor of the input network of the CS-LNA and $\omega_T \approx \frac{g_{m1}}{C_{gs1}}$ is the process dependant parameter.

The load is a resonant network with resonant impedance as Z_L. The LNA voltage gain is now calculated as

$$|A_v| = G_{CS-LNA} Z_L = g_{m1} Q Z_L = \frac{1}{2}\frac{\omega_T}{\omega_0}\frac{Z_L}{R_s} \tag{3.133}$$

The load Z_L is obtained by

$$Z_L = \frac{|A_v|}{G_{CS-LNA}} = \frac{2|A_v|\omega_o R_s}{\omega_T} \tag{3.134}$$

To obtain 15dB voltage gain, the Z_L is calculated as 24Ω.

The above procedure is based on the minimum Noise Factor. If instead a specified NF is desired, we just follow the same design procedure. The Noise Figure of the designed LNA is calculated using (3.119)

$$NF_{CS} = 10 \times \log(F_{CS}) = 10 \times \log(1 + (\frac{\omega_o}{\omega_T})\kappa_{nf}) = 10 \times \log(1 + \frac{2.4}{56} \times 4) = 0.69\text{dB} \qquad (3.135)$$

where κ_{nf} =4 is from Fig. 3.25 at Q=1.5.

Step 5: Simulation Verification

The design target and the simulated performance of the LNA are summarized in Table 3.4. The circuit's parameters are summarized in Table 3.5. The simulated S11, voltage gain and noise figure of the LNA are given in Fig. 3.27. The linearity of the LNA is shown in Fig. 3.28. $\omega_o = 2.4\text{GHz}$, $\omega_T = 56\text{GHz}$, α=0.75, γ=2.5, δ=5 and c=-0.5j are the corresponding parameters for 0.18μm technology [34].

Table 3.4. Summary of the design targets and the simulated results of CS-LNA

	Design target	Simulation results
S11@2.4GHz	<-10dB	-32dB
S21	>15dB	15.7dB
NF	<2dB	~0.62dB
IIP3	>-10dBm	-6.85dBm
Current consumption	<10mA	1.47mA
Power supply	1.8V	1.8V
Process	0.18µm CMOS	0.18µm CMOS

Table 3.5. Inductively degenerated CS-LNA parameters

	Calculation values	Modified simulation values
M_1	110µm/0.18µm	110µm/0.18µm
M_1	110µm/0.18µm	110µm/0.18µm
L_g	31nH	20nH
L_s	0.14nH	0.28nH
L_d	4.3nH	4.3nH
R_d	24Ω	26Ω
i_{bias}	9.4mA	8.6mA

The S11 is satisfied when matching equations (3.124)-(3.125) are satisfied. The inductor value of L_g in the simulation is smaller than the calculated value. It is because in the calculation, only the gate-source parasitic capacitance is considered. Due to the existence of the gate-drain capacitance, the required inductor L_g value reduces from 31nH to 20nH. The Gain is considered using (3.133)-(3.134). The NF in this design is trying to find the best noise performance of the CS-LNA. It is achieved through (3.119) and Fig. 3.25. The linearity in this design is not given the design equation. The design verification is processed to check the linearity of the CS-LNA. If the design satisfies the linearity requirement, we just use the design parameters. If the design does not satisfy the linearity requirement, we need to increase the bias current to satisfy it. The simulation procedure of the LNA is summarized in Appendix B. From table 3.4, the designed LNA satisfied the design target, which proves the validity of the design procedure. The design procedure of inductively degenerated CS-LNA is now summarized and shown in Fig. 3.29.

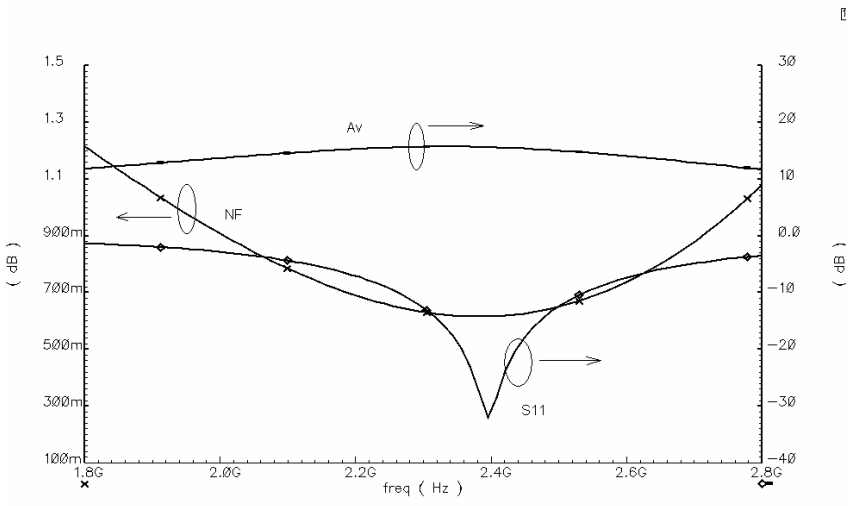


Fig. 3.27 Simulated voltage gain (Av), S11 and NF of CS-LNA

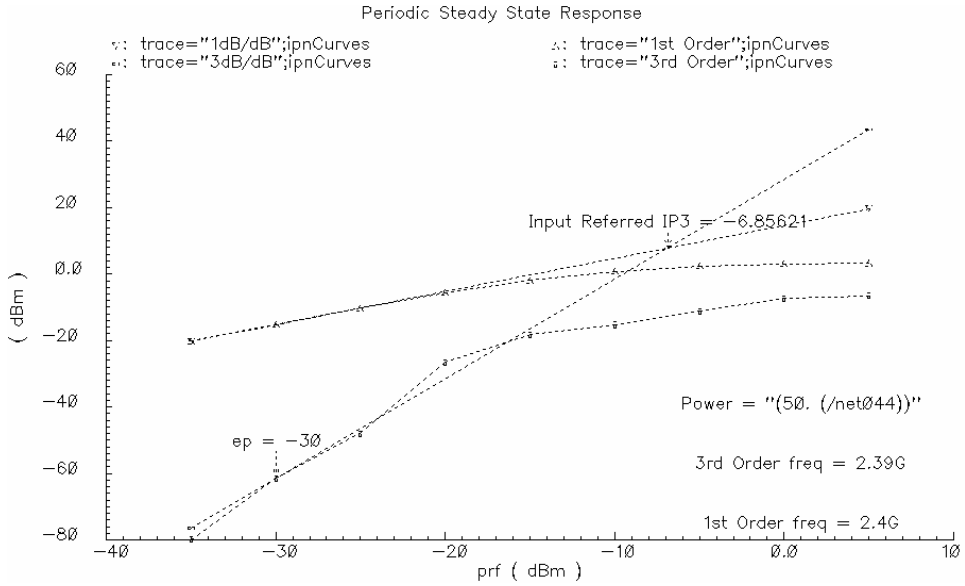


Fig. 3.28 Simulated LNA IIP3 of CS-LNA

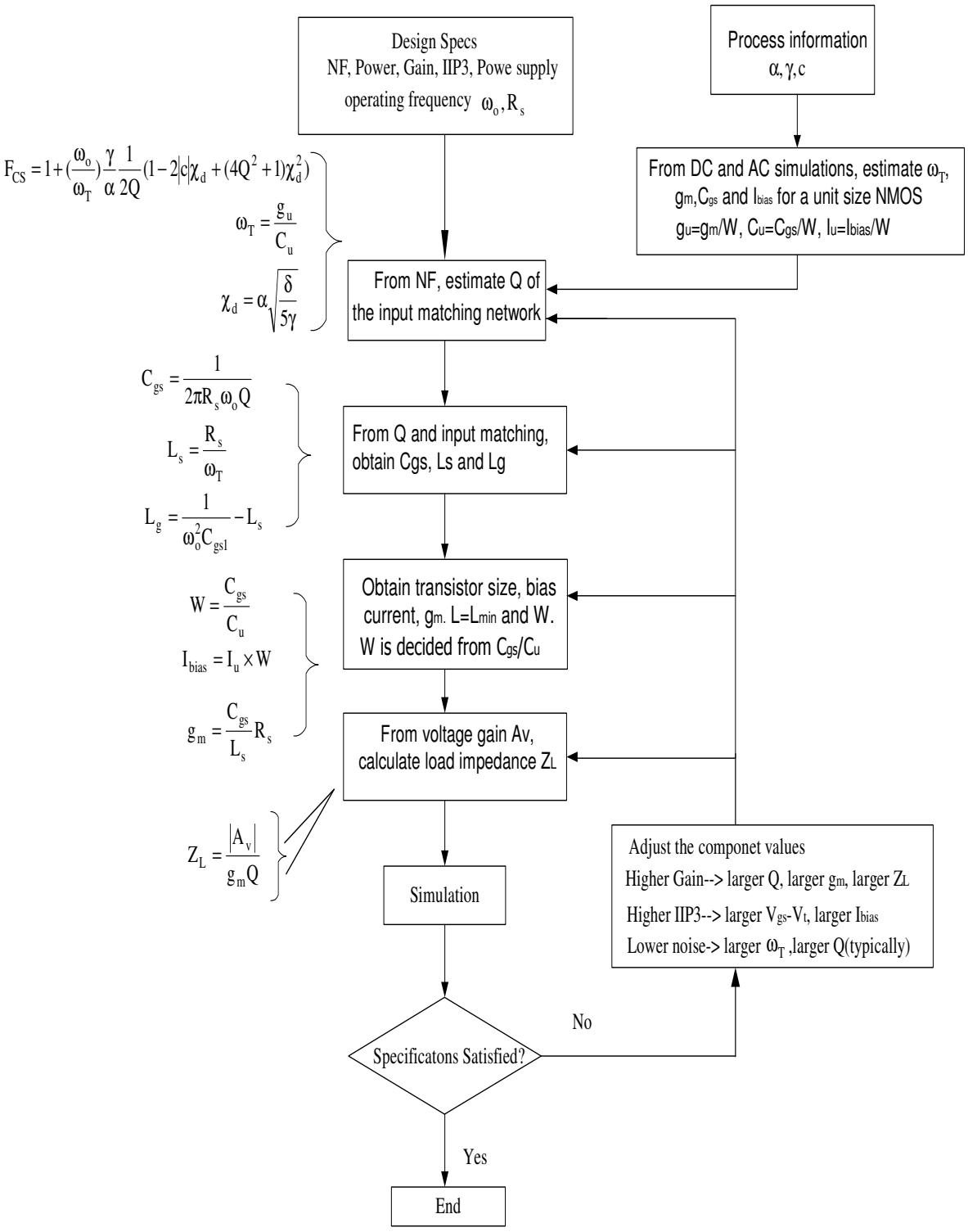


Fig. 3.29 Design procedure for inductively degenerated CS-LNA

3.2.1.3 Common Gate LNA (CG-LNA)

The CG-LNA can be used both in narrowband application and in wideband application. In the multi-band and multi-mode application, the CG-LNA is easily used for the matching requirement. For the narrowband application, according to the noise, gain, linearity and power requirement, the CG-LNA can also be used.

The typical CG-LNA circuit is shown in Fig. 3.30 [33]-[34].

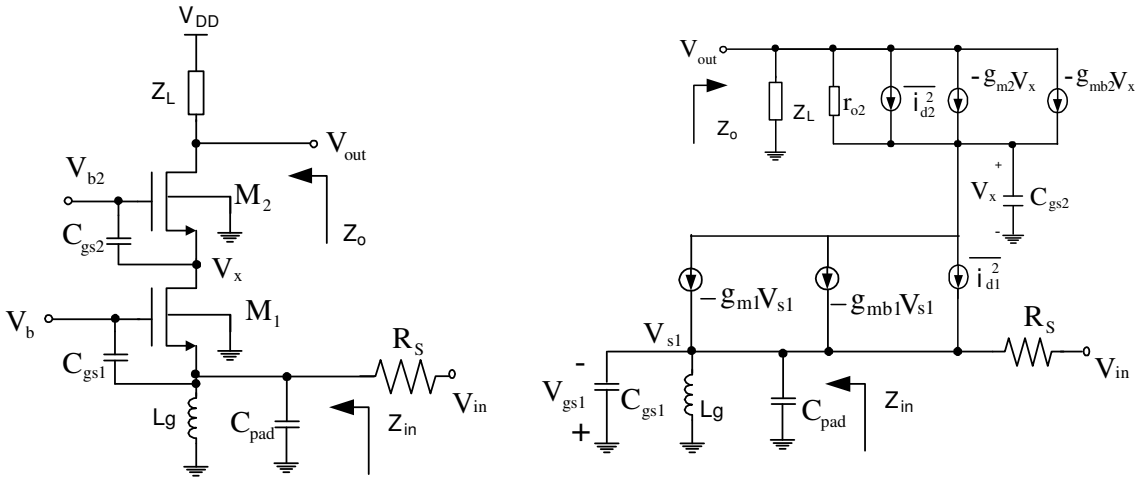


Fig. 3.30 (a) Typical common gate LNA (CG-LNA) and (b) Its equivalent input network

The input impedance of the CG amplifier in Fig. 3.30 yields

$$Z_{in}(j\omega) = \frac{1}{g_{m1} + g_{mb1} + j\omega C_{gs1} + j\omega C_{pad} + \dfrac{1}{j\omega L_g}} \tag{3.136}$$

For the operating frequency (ω_o), the following condition should be satisfied for the input impedance to be matched.

$$j\omega_o C_{gs1} + j\omega_o C_{pad} + \frac{1}{j\omega_o L_g} = 0 \tag{3.137}$$

$$Z_{in}(j\omega) = \frac{1}{g_{m1} + g_{mb1}} \tag{3.138}$$

The input impedance matching of the LNA has to be matched to the 50Ω. The shunt inductor L_g is added in the input to resonate with C_{gs1} and C_{pad} to have a good impedance matching in the designed frequency. The difference from the CS matching network lies that it is a parallel resonant network. Due to the lower quality factor of the resonant network, it is more robust against the process, electrical variation [34]. Due to the omission of C_{gd1} path from the input to the output, the CG LNA shows better reverse isolation (S12) and stability versus CS-LNA.

The overall transconductance of the CG-LNA is estimated as

$$G_{m,CG}(j\omega) = \frac{i_d}{V_{in}} = (g_{m1} + g_{mb1})\frac{V_{gs1}}{V_{in}} = (g_{m1} + g_{mb1})\frac{Z_{in}}{Z_{in} + R_s} \tag{3.139}$$

where Z_{in} is given in (3.136). When the input impedance of the CG-LNA is matched, (3.136) becomes (3.138) and (3.139) changes to

$$G_{m,CG}(j\omega) = \frac{g_{m1} + g_{mb1}}{2} \tag{3.140}$$

The noise performance of the CG-LNA if the noise from the cascode transistor is neglected becomes:

$$F_{CG} = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega_o}{\omega_T}\right)^2 \approx 1 + \frac{\gamma}{\alpha} \tag{3.141}$$

where R_s is the input voltage source resistance, ω_o is the operating frequency, and α, γ and δ are bias-dependant parameters [33]-[34]. α is typically around 1, γ is between 2 and 4, δ is around 5 and ω_T is greater than 50GHz for 0.18 μm CMOS technology. If we assume α=0.75, γ=2.5, δ=5 and ω_T=50GHz [34], $\frac{\delta\alpha}{5}\left(\frac{\omega_o}{\omega_T}\right)^2$ is 0.002 at 2.4GHz and $\frac{\gamma}{\alpha}$ is 3.3. It proves the validity of the approximation in (3.141).

The noise factor of CS-LNA (3.115) and the noise factor of CG-LNA (3.141) using the 0.18μm CMOS process are plotted in Fig. 3.31. with α=0.85, γ=2, δ=4, c=-0.5j, ω_T=56GHz and Q=2 for CS-LNA. These parameters are just used to demonstrate the different from the CS-LNA and CG-LNA. They are a little different from those used in the CS-LNA example given in previous section to clearly show the trends.

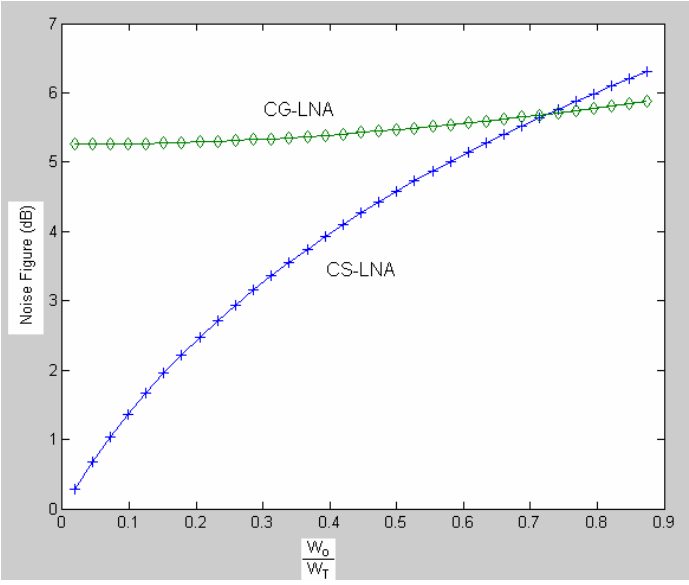


Fig. 3.31 Noise figure of CS-LNA and CG-LNA versus ω_o/ω_T for 0.18μm CMOS process

The noise factor of CS-LNA (3.115) and the noise factor of CG-LNA (3.141) using the 0.6μm CMOS process are plotted in Fig. 3.32, with α=1, γ=2/3, δ=4/3, c=-0.395j, ω_T =13GHz and Q=2 for CS-LNA. These parameters are just used to demonstrate the different from the CS-LNA and CG-LNA. They are a little different from those used in the CS-LNA example given in previous section to clearly show the trends.

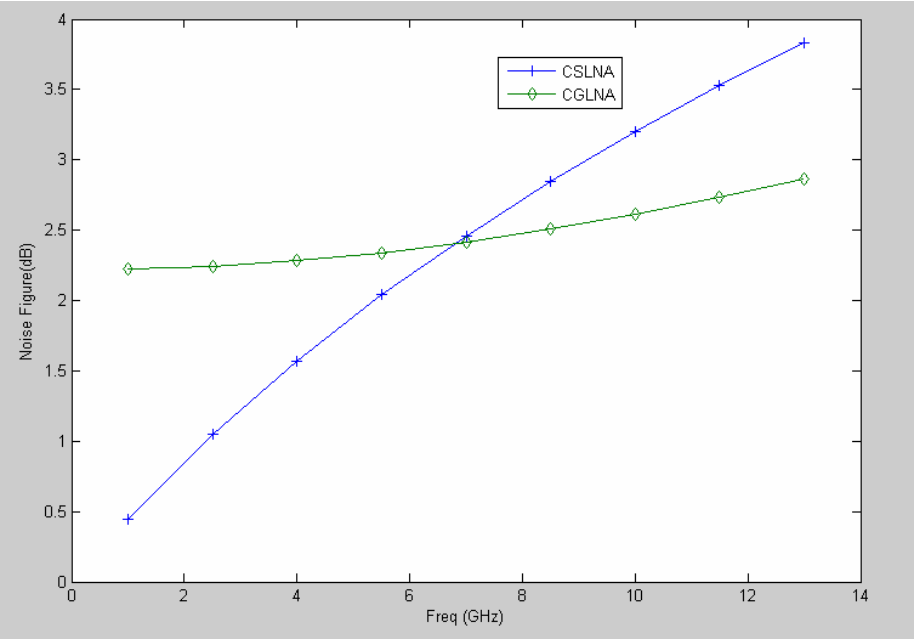


Fig. 3.32 Noise figure of CS-LNA and CG-LNA versus f_o for 0.5μm CMOS process

The noise factor of CS-LNA (3.115) and the noise factor of CG-LNA (3.141) using the 0.13μm CMOS process are plotted in Fig. 3.33, with α=0.9, γ=2.5, δ=5, c=-0.5j, ω_T =100GHz and Q=2 for CS-LNA. These parameters are just used to demonstrate the different from the CS-LNA and CG-LNA. They are a little different from those used in the CS-LNA example given in previous section to clearly show the trends.

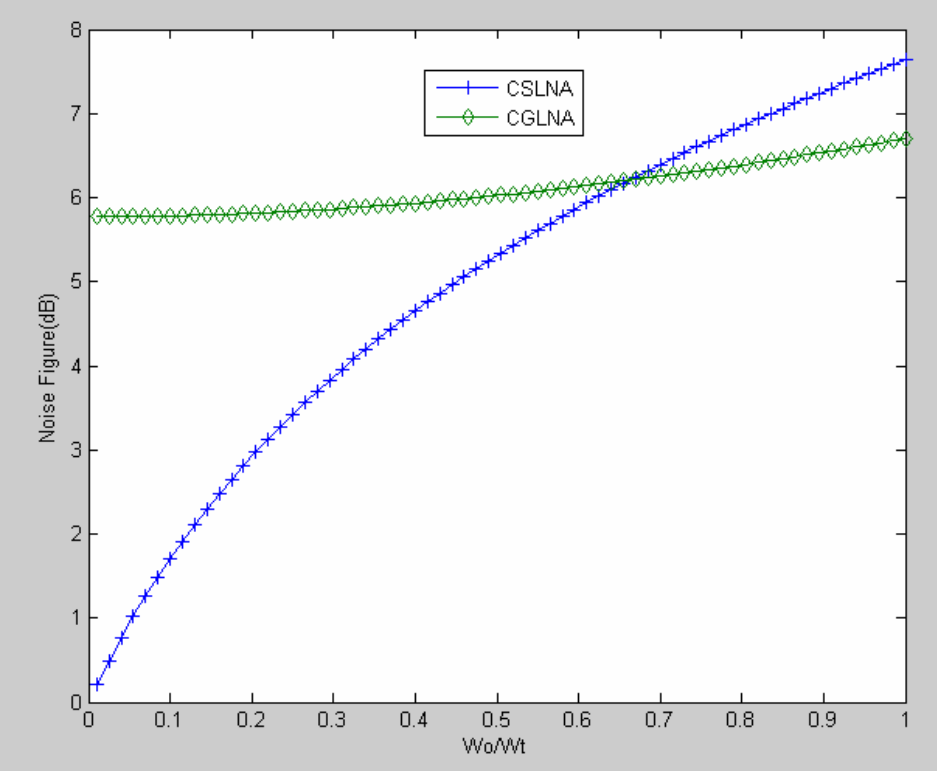


Fig. 3.33 Noise figure of CS-LNA and CG-LNA versus ω_o/ω_T for 0.13μm CMOS process

From (3.30)-(3.31), same as discussed in [34], the noise factor of CG LNA is nearly constant with respect to ω_o / ω_T, and the noise factor of CS LNA is linearly dependent with ω_o / ω_T. Normally, the CS-LNA has better noise performance than the CG-LNA. The CG-LNA outperforms CS-LNA at higher frequency $\frac{\omega_o}{\omega_T}$. The CS-LNA benefits from the higher f_T for the advanced technology and has better noise performance in the same operating frequency. The CG-LNA has less dependence on the f_T. It has worse noise performance due to the large $\frac{\gamma}{\alpha}$ used in the noise figure calculation for the advanced process.

3.2.1.3.1 CG-LNA Design Procedure

First a particular design example is presented. After that, a general design procedure for CG-LNA is introduced. In this design example, a common gate LNA (CG-LNA) will be designed using a 0.18μm CMOS technology to show how the LNA design procedure is carried-out. The design target is to have an LNA working at 2.4GHz band with less than 4 dB Noise Figure, -5dBm IIP3, greater than 12dB voltage gain and consuming less than 9mW, that is 5mA current from a 1.8V power supply.

Step 1: Calculate g_{m1}

To match the input impedance as Rs=50Ω, the transconductance of the transistor M1 is

$$g_{m1} \approx \frac{1}{R_s} \tag{3.142}$$

The Noise Factor can be calculated as

$$F_{CG} \approx 1 + \frac{\gamma}{\alpha} g_{m1} R_s \approx 1 + \frac{\gamma}{\alpha} \tag{3.143}$$

The noise performance of the CG-LNA is bounded by the process parameters. From (3.143), we also can find that certain degree of mismatch in the input also can help the noise performance. The noise factor F_{CG} of the CG-LNA is proportional to the g_{m1} of the transistor M_1. The smaller g_{m1} is, the better noise performance of the CG-LNA is. If the input impedance ($1/g_{m1}$) does not equal to R_s, the input network has the mismatch. Here g_{m1} is chosen as 20mA/V to perfect match the input impedance.

Step 2: Obtain Transistor M_1 Size and Bias Voltage V_b

According to (3.142), g_{m1} is chosen as 20mA/V. The transconductance ($g_{mu}=g_m/W$) versus bias current density (I_{bu}=Ibias/W) and bias voltage with NMOS device (W=1μm and L=0.18μm) is shown in Fig. 3.34 and Fig. 3.35. V_{th0} is 0.49V and $K_p(C_{ox}\mu_n/2)$ is 176 $\mu A/V^2$. According to the Fig. 3.34 and Fig. 3.35, there are different combination of the transistor size and the bias voltage (bias current) can achieve this target. The length (L) is fixed to the minimal length, L=0.18μm, for faster speed and smaller parasitic capacitance. For the transistor working in the saturation region,

$$g_{m1} = \mu_n C_{ox} \frac{W}{L} V_{dsat} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{dc}} \tag{3.144}$$

$$\frac{g_{m1}}{W/L} = \sqrt{2\mu_n C_{ox} \frac{I_{dc}}{W/L}} \tag{3.145}$$

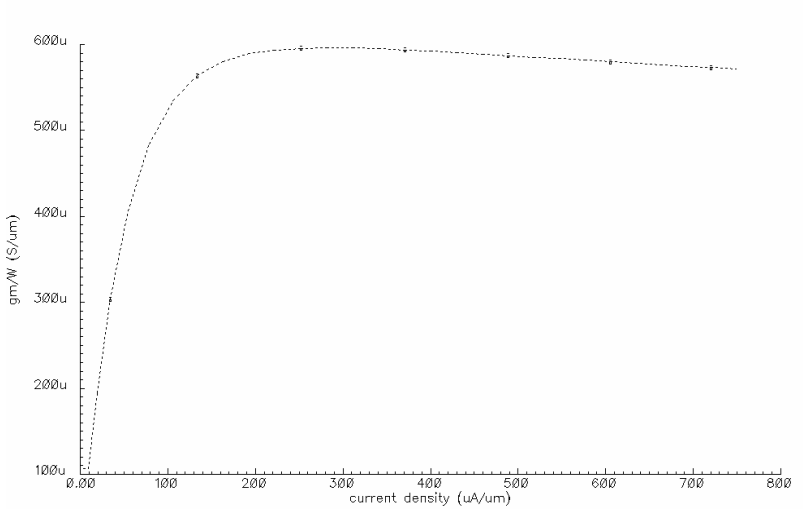


Fig. 3.34 g_m/W versus current density of the transistor (L=0.18μm)

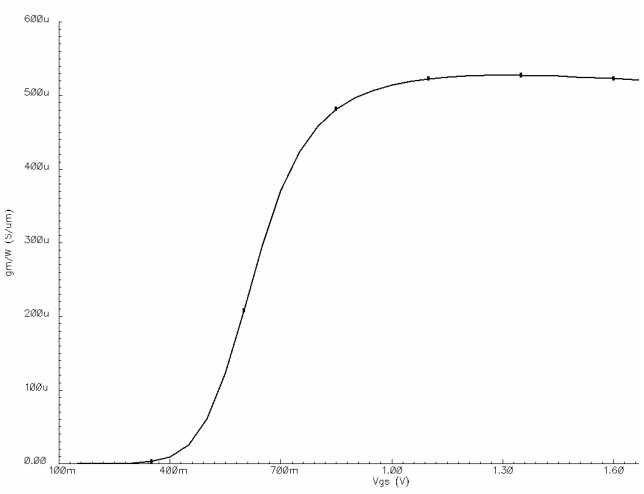


Fig. 3.35 g_m/W versus bias voltage (V_{gs}) of the transistor

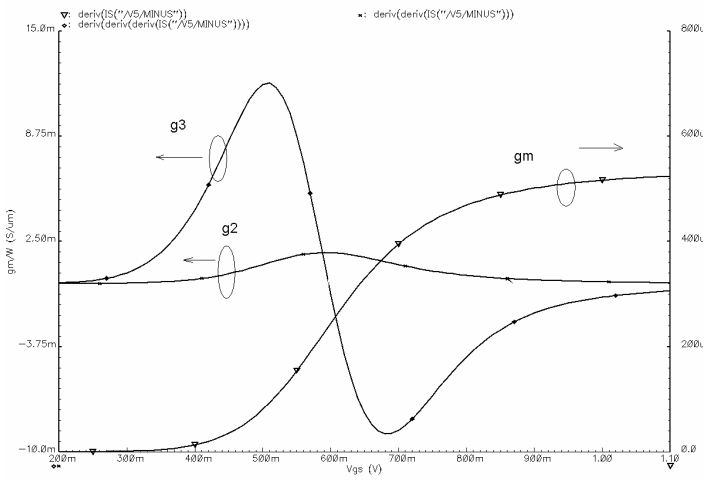


Fig. 3.36 Transistor g_m, g_2 and g_3 versus bias voltage V_{gs} of transistor

Fig. 3.36 is obtained through the simulation. First sweep the bias voltage V_{gs} during DC and obtain the drain current I_d. I_d can be expressed as up to third order

$$I_d = I_{DC} + g_m v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 \tag{3.146}$$

The transconductance g_m is obtained by $g_m = \frac{d(I_d)}{d(V_{gs})}$, the second nonlinear term g_2 is obtained by $g_2 = \frac{d^2(I_d)}{d(V_{gs})^2}$ and the third nonlinear term g_3 is calculated as $g_3 = \frac{d^3(I_d)}{d(V_{gs})^3}$.

The linearity performance of the transistor is inspected to help choose the transistor size and the bias voltage (current). For a unit transistor, its transconductance, second order effect (g_2) and the third order effect (g_3) are shown in Fig. 3.36.

From Fig. 3.36, the transistor M_1 has minimal g_3 around 0.6V bias voltage and thus the bias voltage (V_{gs}) is chosen as 0.6V, and the corresponding I_{DC} becomes 1.5mA.

From Fig.3.36, the normalized transconductance g_{mu} is around 220μS for (W=1μm and L=0.18μm) and desired g_m value is 0.2mS. The width transistor M_1size for L=0.18μm is chosen as

$$W \approx \frac{g_m}{g_{mu}} = \frac{0.2\times10^{-3}}{220\times10^{-6}}\mu m = 91\mu m \qquad (3.147)$$

Through the DC simulation, the width (W) is adjusted to 83μm. It is because the W=91μm NMOS transistor has the unit transistor (W=9.1μm) and multiple number=10, which is different from the unit transistor in step 2 (W=1μm).

Step 3: Calculate L_g and The LNA Load Network (Z_L)

From bias voltage V_{gs}=0.6V and the transistor M_1 size (W=83μm and L=0.18μm), through the DC simulation, the parasitic capacitor is around 90fF, which can be estimated as

$C_{gs} \approx \frac{2}{3}\mu_n C_{ox}\frac{W}{L}$. Assuming the pad and other interconnect contributes 1PF capacitance, to operating at 2.4GHz, the L_g is calculated as

$$L_g = \frac{1}{\omega_o^{\ 2}(C_{gs} + C_{pad})} \approx 4\text{nH} \tag{3.148}$$

The cascode device M_2 is chosen same as the main transistor M_1 for simplicity. In practice, the transistor M_2 also influences the LNA noise performance and the linearity performance. It will be explained in Chapter IV.

The LNA load (Z_L in Fig. 3.30) is a resonant network at 2.4GHz as the resonance frequency as shown in Fig.3.37.

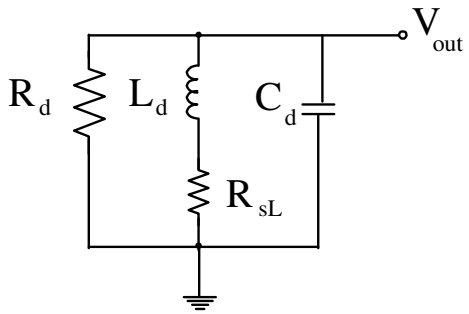


Fig. 3.37 Equivalent AC output network of CG-LNA

The LNA voltage gain is calculated as

$$A_v = g_{m1}R_d \tag{3.149}$$

The L_d and C_d needs to resonant at the operating frequency.

$$sL_d + \frac{1}{sC_d} = 0 \tag{3.150}$$

The absolute value of the inductor L_d is also decided by the bandwidth of the LNA.

$$BW = \frac{\omega_o}{Q_{load}} \tag{3.151}$$

$$Q_{load} = \frac{R_{sL}}{\omega_o L_d} = \frac{\omega_o}{BW} \tag{3.152}$$

where Q_{load} is the quality factor of the load network.

Here the load inductor is just chosen a reasonable value 4.3nH and the load capacitor is chosen as corresponding 1pF.

The circuit's parameters are summarized in Table 3.6. The simulated performance is summarized in Table 3.7.

Table 3.6. CG-LNA parameters

	Calculated values	Modified simulation values
M_1	83µm/0.18µm	86µm/0.18µm
M_1	83µm/0.18µm	83µm/0.18µm
L_g	4nH	3.37nH
L_d	4.3nH	4.3nH
V_b	0.6V	0.6V
V_{b2}	1.8V	1.8V

Table 3.7 The summary of the design targets and the simulated results of CG-LNA

	Design target	Simulation results
S11@2.4GHz	<-10dB	-40dB
S21	>12dB	19.5dB
NF	~4dB	~3.9dB
IIP3	>-5dBm	-1.7dBm
Current consumption	<5mA	1.47mA
Power supply	1.8V	1.8V
Process	0.18µm CMOS	0.18µm CMOS

The simulation results are shown in Fig. 3.38 and Fig. 3.39. The simulation procedure of the CG-LNA is same as that of the CS-LNA, which is given in the Appendix B.

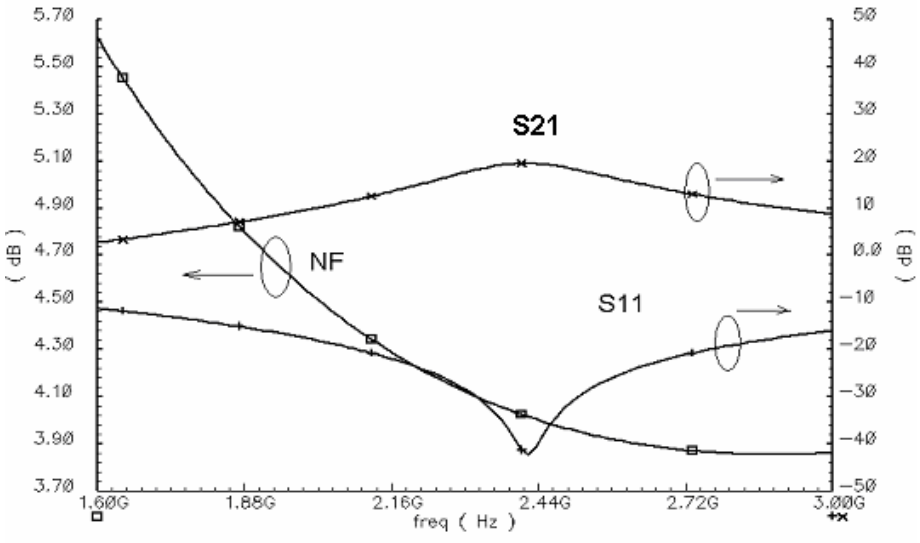


Fig. 3.38 Simulated S21, S11 and NF of the CG-LNA

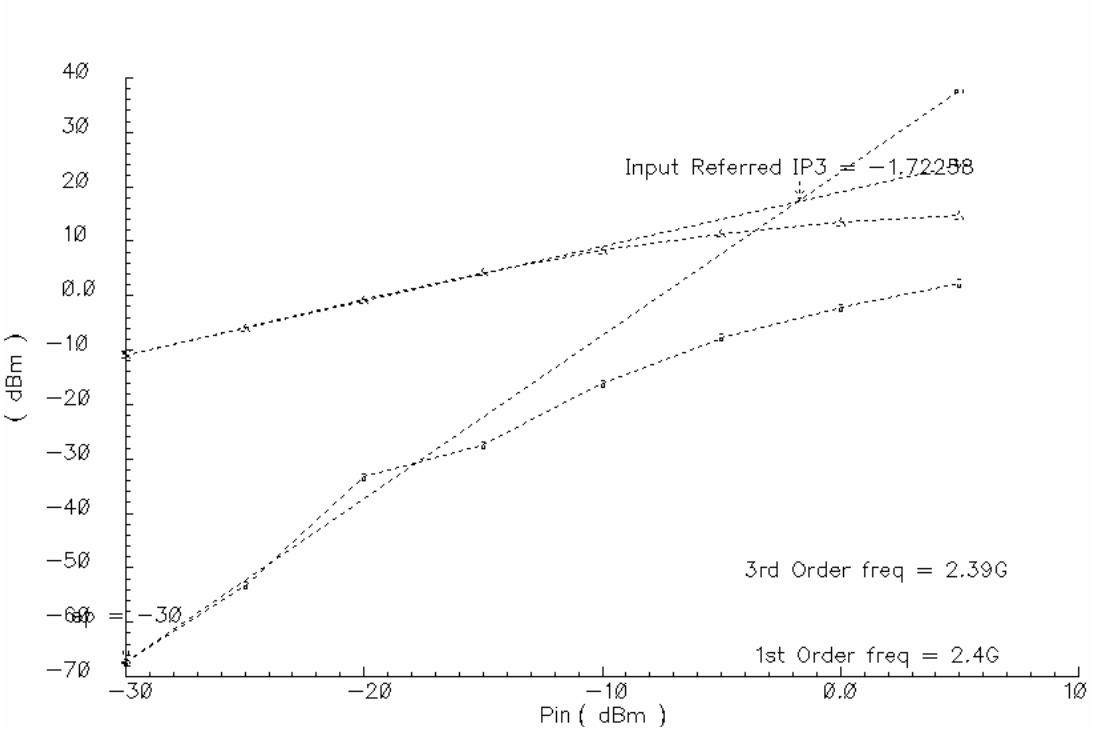


Fig. 3.39 Simulated IIP3 of CG-LNA

The design flow for CG-LNA is shown in Fig. 3.40.

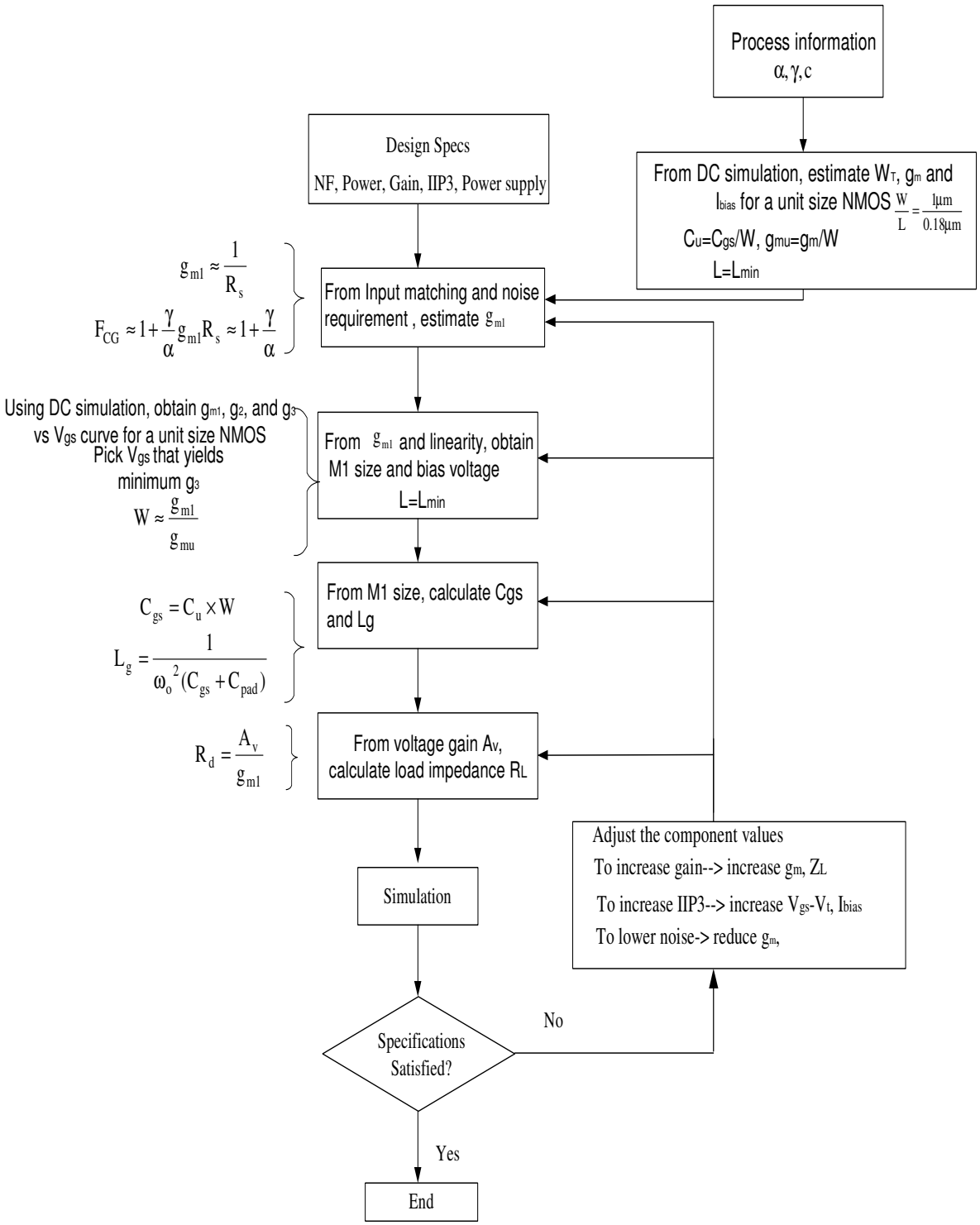


Fig. 3.40 Design procedure for CG-LNA

3.2.1.4 Feedback LNA

The negative feedback network can be used to implement the input impedance matching, is shown in Fig. 3.41. The conceptual circuit diagram, equivalent block diagram and a simple implementation are depicted in this Fig. 3.41.

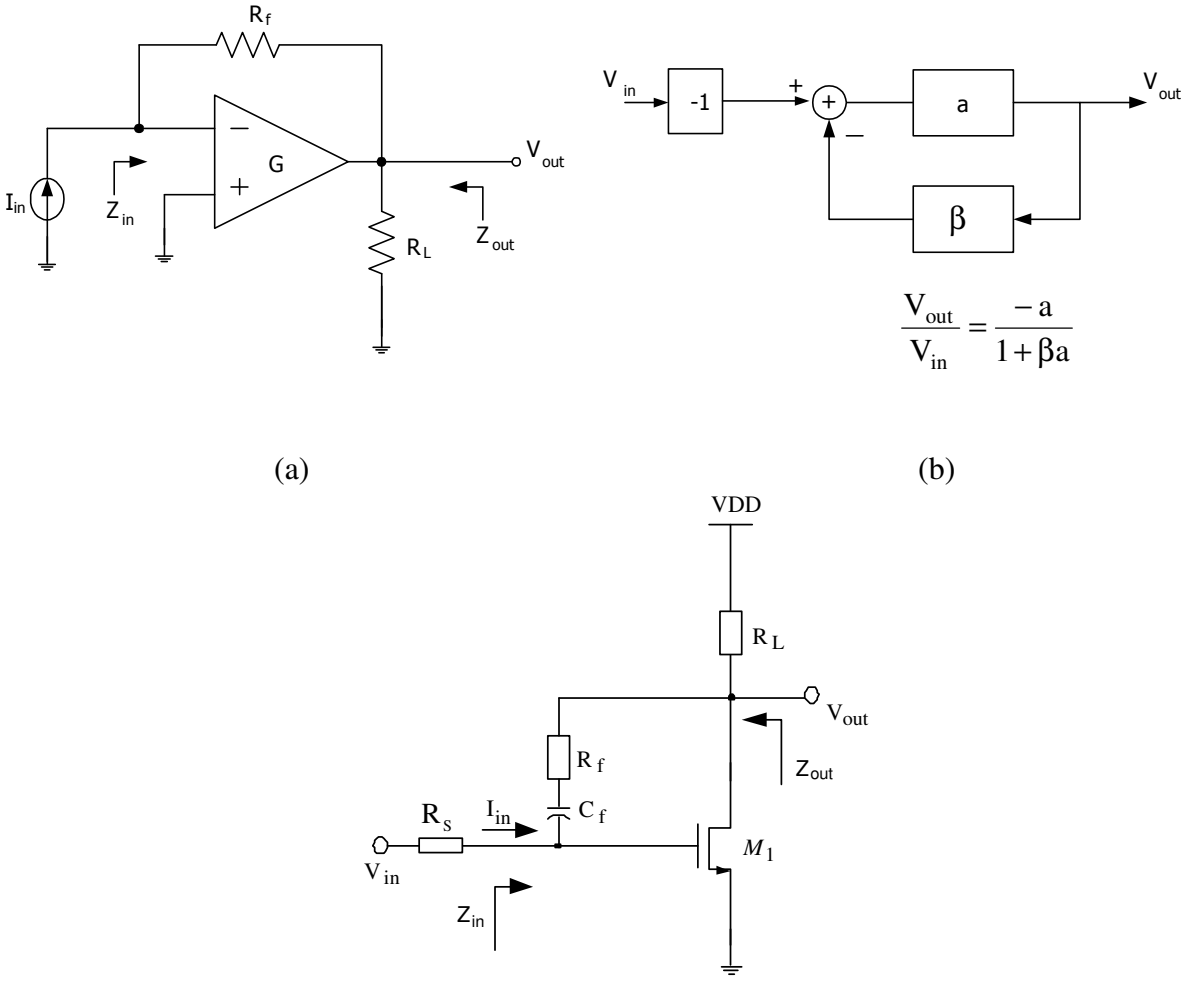


Fig. 3.41 (a) Negative feedback system (b) Equivalent block diagram c) A simple implementation

The feedback factor is

$$\beta = -\frac{1}{R_f} \tag{3.153}$$

The forward gain can be derived as

$$a = \frac{V_{out}}{I_{in}} = G\frac{R_f^2 R_L}{R_f + R_L} \tag{3.154}$$

The open loop gain can be derived as

$$T = a\beta = G\frac{R_f R_L}{R_f + R_L} \tag{3.155}$$

The close loop transfer function is

$$H_{closed} = \frac{V_{out}}{V_{in}} = \frac{-a}{1+a\beta} = \frac{-a}{1+T} = \frac{-G\dfrac{R_f^2 R_L}{R_f + R_L}}{1+G\dfrac{R_f R_L}{R_f + R_L}} \approx R_f \tag{3.156}$$

The closed loop input impedance is shown in (3.157), where $Z_{in} = R_f$

$$Z_{in\_cl} = \frac{Z_{in}}{1+T} = \frac{Z_{in}}{1+a\beta} = \frac{R_f}{1+G\dfrac{R_f R_L}{R_f + R_L}} \approx \frac{R_f + R_L}{GR_L} \tag{3.157}$$

The closed loop output impedance is shown in (3.158), where $Z_{out} = R_f \,//\, R_L$

$$Z_{out\_cl} = \frac{Z_{out}}{1+T} = \frac{\dfrac{R_f R_L}{R_f + R_L}}{1+G\dfrac{R_f R}{R_f + R_L}} \approx \frac{1}{G} \tag{3.158}$$

A commonly used feedback amplifier is shown in Fig. 3.42 [35]-[36] where C_f is the DC block capacitor.

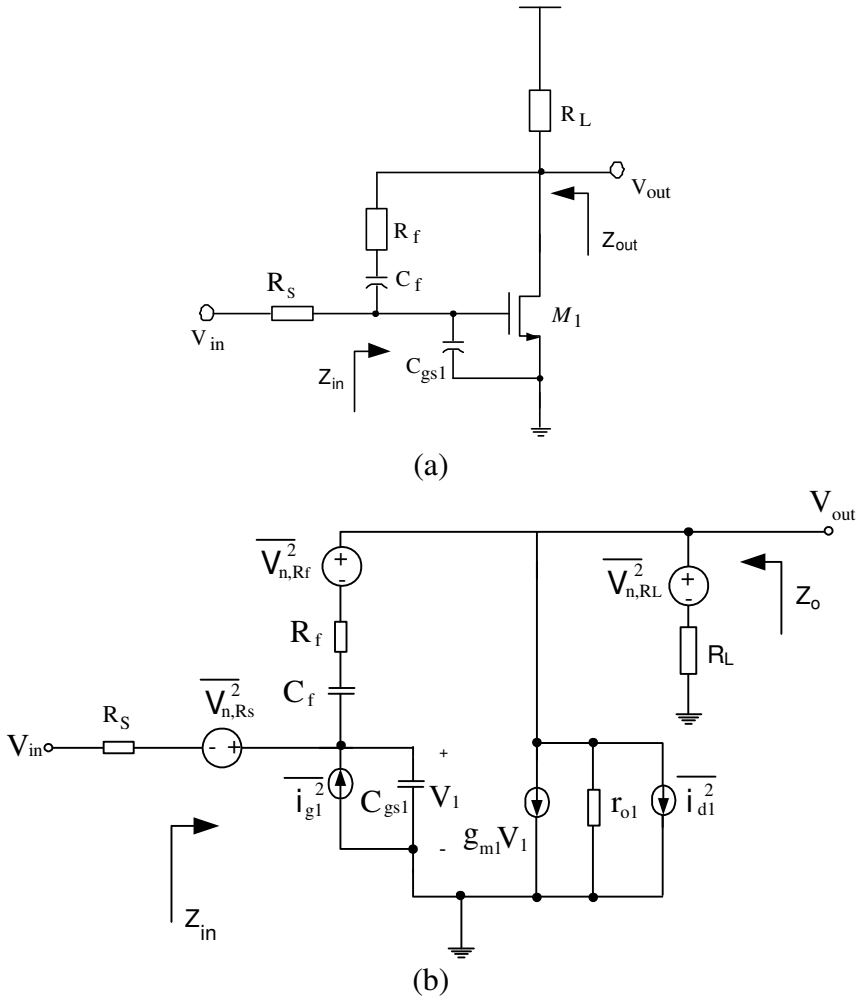


Fig. 3.42 Typical resistive shunt-feedback LNA [35]-[36] (a) Circuit diagram and (b) The equivalent noise circuit

The input impedance of the resistive shunt-feedback LNA is calculated as

$$Z_{in} = \frac{R_f + R_L}{g_{m1} R_L} // \frac{1}{sC_{gs1}} \tag{3.159}$$

Through properly selecting the open loop gain and the resists values, the input impedance can be matched to voltage source impedance Rs.

The noise factor [1] in Fig. 3.42 can be calculated as

$$F = 1 + \frac{R_f}{R_s}\left(\frac{1+g_{m1}R_s}{1-g_{m1}R_f}\right)^2 + \frac{1}{R_s R_L}\left(\frac{R_f + R_s}{1-g_{m1}R_f}\right)^2 \quad (3.160)$$

When $g_{m1} = \frac{1}{R_f}$, the output due to the input voltage source is zero. It represents an infinite noise factor. The resistive shunt-feedback LNA can be used in narrowband application and also in wideband application. The input impedance of this LNA is determined by open loop gain and the resistor values (R_f, R_L), which are easily controlled. The drawback is that the resistor is a noise component and the LNA has moderate noise performance. For instance, a 0.18μm CMOS feedback LNA is used here to demonstrate the performances. The parameter is shown in Table 3.8. And the simulation results are summarized in Table 3.9.

Table 3.8 Feedback LNA component values

Component	Value
$R_f(\Omega)$	250
$M_1(\mu m/\mu m)$	220/0.18
$I_{bias}(mA)$	9
$R_L(\Omega)$	150
$C_f(pF)$	2
VDD(V)	1.8

Table 3.9 Feedback LNA simulated performance

Parameter	Value
f_o(GHz)	2.4
S11(dB)	-14.6
S21(dB)	12.5
NF(dB)	2.84
IIP3(dBm)	3.2
Power(mW)	16
Process	0.18μm CMOS

3.2.1.5 Table of Comparison

The comparison is summarized in Table 3.10.

From table 3.10, the inductively degenerated CS-LNA has better noise performance. It is widely used in narrowband application. The CG-LNA and the feedback LNA have stable input matching network. The CG-LNA consumes less power than the feedback LNA. The resistive termination uses the terminated resistor to achieve the input impedance matching. The main transistor has more freedom to choose the transistor size and the bias voltage. It has worst noise performance but has stable input matching network, very wide region of the noise and linearity performance.

Table 3.10 Narrowband LNA comparison

	Resistive termination LNA Fig. 3.23	CS-LNA Fig. 3.24	CGLNA Fig. 3.30	Feedback LNA Fig. 3.42
Noise Figure(dB)	>6	~2	3~5	2.8~5
LNA gain(dB)	10~20	15~25	10~20	10~20
LNA sensitivity to parasitic	less sensitivity	large sensitivity	Less sensitivity	less sensitivity
Input matching	easy matching network	complex matching network	easy matching network	easy matching network
Linearity (IIP3) (dBm)	Variable (-10~10)	-10~0	-5~5	-5~5
Power dissipation (mW)	Variable (1-50)	>10	~5	>15

3.2.2 Wideband LNA

Besides the narrowband system, there are many other wireless applications with wide signal bandwidth, such as digital video broadcast (DVB-H) and ultra-wideband (UWB) system. The digital video broadcast frequency bandwidth is from 470MHz-862MHz [37]-[38]. The frequency bandwidth for UWB system is 3.1GHz-10.6GHz [39]-[41]. The frequency bandwidth for WiMAX is 2.5GHz-2.69GHz, 3.4GHz-3.6GHz, and 5.725GHz-5.85GHz [42]. The LNA needs to amplify the incoming wideband signal varied from hundreds MHz to several GHz region. The wideband LNA faces a broadband incoming signal. It needs to have the wideband impedance matching and amplify the signal with a flat

gain performance. The UWB LNA, whose signal bandwidth is greater than 500MHz, is an example for the Wideband LNA design.

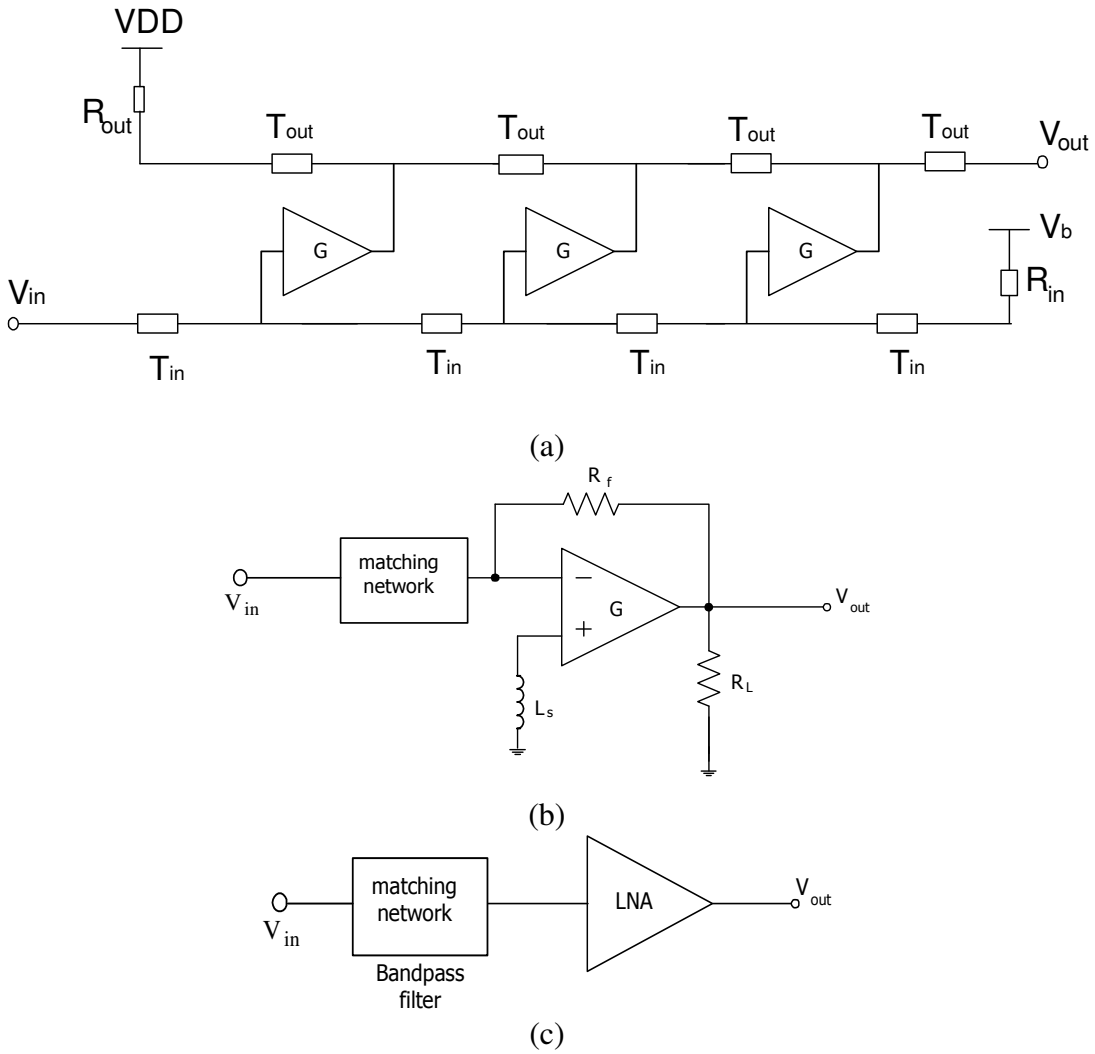


Fig. 3.43 Conceptual ideas of the wideband LNA (a) Distributed LNA (b) Feedback LNA (c) Bandpass filter based LNA

There are different topologies to design the wideband LNA: distributed amplifier [43]-[48] as shown in Fig. 3.43(a), feedback amplifier [49] as shown in Fig. 3.43(b), and filter based common source amplifier [50]-[51] as shown in Fig. 3.43(c). The concepts of

them are shown in Fig. 3.43. They will be discussed later and the conceptual idea of these LNA will be shown in the following sections.

3.2.2.1 Distributed LNA

Wideband LNA requires broadband impedance matching and also the flat gain over the frequency band. The typical CMOS transistor is bounded by the gain bandwidth trade-off: to work in the higher frequency, the gain will drop. As shown in Fig. 3.43(a), the distributed architecture uses the transmission line to absorb the parasitic capacitance in the input and the output of the transistor and provides several signal paths from the input to the output, which can achieve wideband operation. The parasitic capacitance of the transistor is a frequency dependant component, which changes the impedance over the frequency.

The typical single transistor wideband amplifier is shown in Fig.3.44

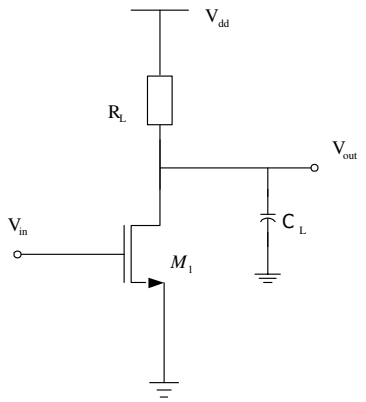


Fig.3.44 Single transistor CS amplifier

The DC gain of amplifier in Fig.3.44 is

$$A_{vo} = g_{m1}(R_L // r_o) \tag{3.161}$$

The dominant pole is

$$p_o = \frac{1}{C_L(R_L // r_o)} \tag{3.162}$$

Thus

$$A_v(s) = \frac{A_{v0}}{1 + s/p_o} = \frac{p_o A_{vo}}{s + p_o} = \frac{GB}{s + p_o} \tag{3.163}$$

The gain-bandwidth product is

$$GBW = \frac{g_m}{C_L} \tag{3.164}$$

For the fixed load, the amplifier has lower gain at the higher frequencies.

The distributed amplifier can conquer the drawback of the single transistor common source amplifier. It adopts the transmission concept to achieve the wideband flat gain operation.

The transmission line technique is widely used in microwave circuits. It can absorb the parasitic capacitance of the transistor and achieve the wideband impedance matching. The distributed amplifier (DA) achieves the wideband operation by applying the transmission line technique to absorb the parasitic capacitance of the transistor [43]-[47]. A typical distributed LNA is shown in Fig. 3.45.

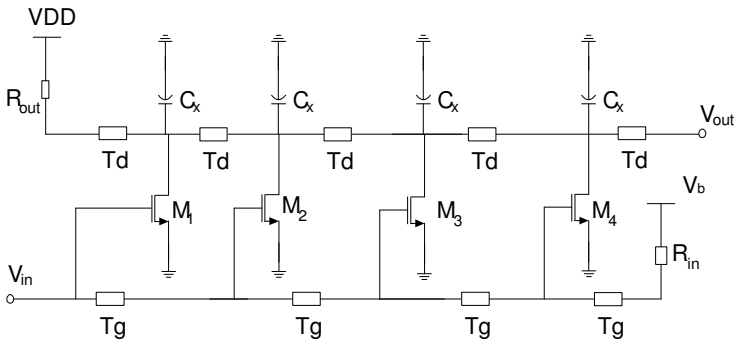


Fig.3.45 Typical distributed amplifier

Where T_g is the transmission line connecting all the gate terminals of the transistors, Td is the transmission line connecting all the drain terminals of the transistors and all the transistors have the same size (M_1=M_2=M_3=M_4).

The impedance of the transmission line is

$$Z_0 = \sqrt{L_u / C_u} \tag{3.165}$$

where L_u and C_u are the unit inductance and the unit capacitance of the transmission line.

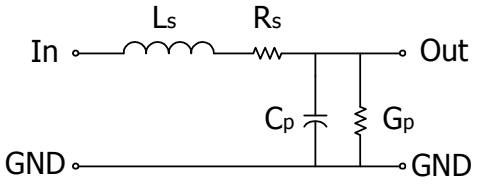


Fig.3.46 Lumped RLC model of the transmission line segment

The lumped RLC model of the transmission line segment is shown in Fig. 3.46, where L_g, R_g, C_g and G_g are the series inductance and resistance and parallel capacitance and conductance of the transmission line per segment.

The impedance of the transmission line with the load capacitance (C_x) for the gate line is

$$Z_g = \sqrt{\frac{j\omega L_g + R_g}{j\omega(C_g + \frac{C_{gs}}{l_g}) + G_g}} \tag{3.166}$$

where L_g, R_g, C_g and G_g are the series inductance and resistance and parallel capacitance and conductance of the gate transmission per unit length, l_g is the transmission line length and C_{gs} is the parasitic gate capacitance of the transistor.

The impedance of the transmission line with the load capacitance for the drain line is

$$Z_d = \sqrt{\frac{j\omega L_d + R_d}{j\omega(C_d + \frac{C_x}{l_d}) + G_d}} \tag{3.167}$$

where L_d, R_d, C_d and G_d are the series inductance and resistance and parallel capacitance and conductance of the drain transmission per unit length, l_d is the transmission line length and C_x is the additional capacitor added in the drain of the transistor. The equivalent circuit of the transmission lines is shown as below.

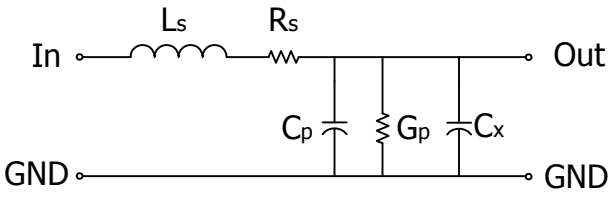


Fig.3.47 Lumped RLC model of the transmission line segment with Cx

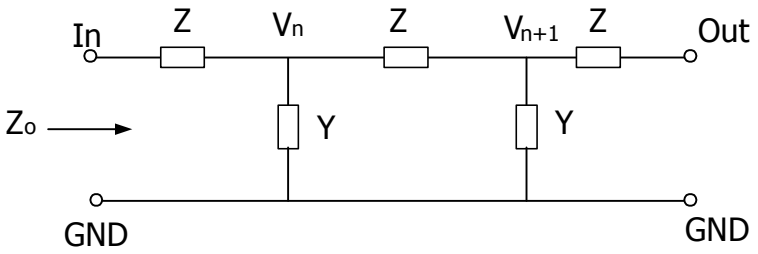


Fig.3.48 Lumped transmission line network

Consider the voltage V_n and V_{n+1}, we can get the following relation [1].

$$V_{n+1} = V_n \left[\frac{Z_o \,//(\frac{1}{Y}dz)}{Zdz + Z_o \,//(\frac{1}{Y}dz)} \right] \tag{3.168}$$

From (3.168), we can get

$$\frac{V_{n+1}}{V_n} = \frac{Z_o}{Z_o ZY(dz)^2 + Z_o + Zdz} \approx \frac{Z_o}{Z_o + Zdz} = \frac{1}{1 + \frac{Z}{Z_o}dz} \approx 1 - \frac{Z}{Z_o}dz \tag{3.169}$$

$$\frac{V_{n+1} - V_n}{dz} = -\frac{Z}{Z_o}V_n \tag{3.170}$$

where Z_o is the characteristic impedance $Z_o = \sqrt{\frac{Z}{Y}}$.

When dz is near zero, V_{n+1} equals to V_n and (3.170) changes to

$$\frac{d(V)}{dz} = -\sqrt{ZY}V \tag{3.171}$$

Solving the equation (3.171), we can get the voltage as

$$V(z) = V_o e^{-\sqrt{ZY}z} \tag{3.172}$$

where V_o is the voltage at the starting point and z is the location, which is different from Z.

The RF signal at the k^{th} gate tapping point [43] is expressed as

$$V_{gRF\_K}(s) = V_{RF}(s)e^{-(k-1/2)\gamma_{RF}l_{RF}} \tag{3.173}$$

where $\gamma_{RF} = \sqrt{ZY}$ is the propagation constant.

The RF signal at the k^{th} drain tapping point is expressed as

$$V_{dRF\_K}(s) = -g_m \frac{Z_d(s)}{2} V_{gk}(s) = -g_m \frac{Z_d(s)}{2} V_{RF}(s)e^{-(k-1/2)\gamma_g l_g} \tag{3.174}$$

The signal at the output of the distributed LNA is calculated as

$$\begin{aligned} V_d(s) &= \sum_{k=1}^{n} V_{dRF\_K}(s)e^{-(n-k+1/2)\gamma_d l_d} = -g_m \frac{Z_d(s)}{2} V_{RF}(s) \sum_{k=1}^{n} e^{-(k-1/2)\gamma_g l_g} e^{-(n-k+1/2)\gamma_d l_d} \\ &= -g_m \frac{Z_d(s)}{2} V_{RF}(s)e^{-(\gamma_d l_d - \gamma_g l_g)/2} \frac{e^{-n\gamma_d l_d} - e^{-n\gamma_g l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \end{aligned} \tag{3.175}$$

If the phase is synchronized in the gate transmission line and the drain transmission line as follows

$$\gamma_g l_g = \gamma_d l_d = \gamma l \tag{3.176}$$

The distributed LNA gain is

$$G_{DA} = \frac{V_d}{V_{RF}} = -ng_m \frac{Z_d}{2} \tag{3.177}$$

The application of the distributed amplifier includes the communication systems, microwave instrumentation and optical systems where the wideband flat gain response and good impedance matching over several gigahertz ranges are the requirements.

3.2.2.1.1 Distributed LNA Design Procedure

The design flow for distributed amplifier [48] is shown in Fig. 3.49.

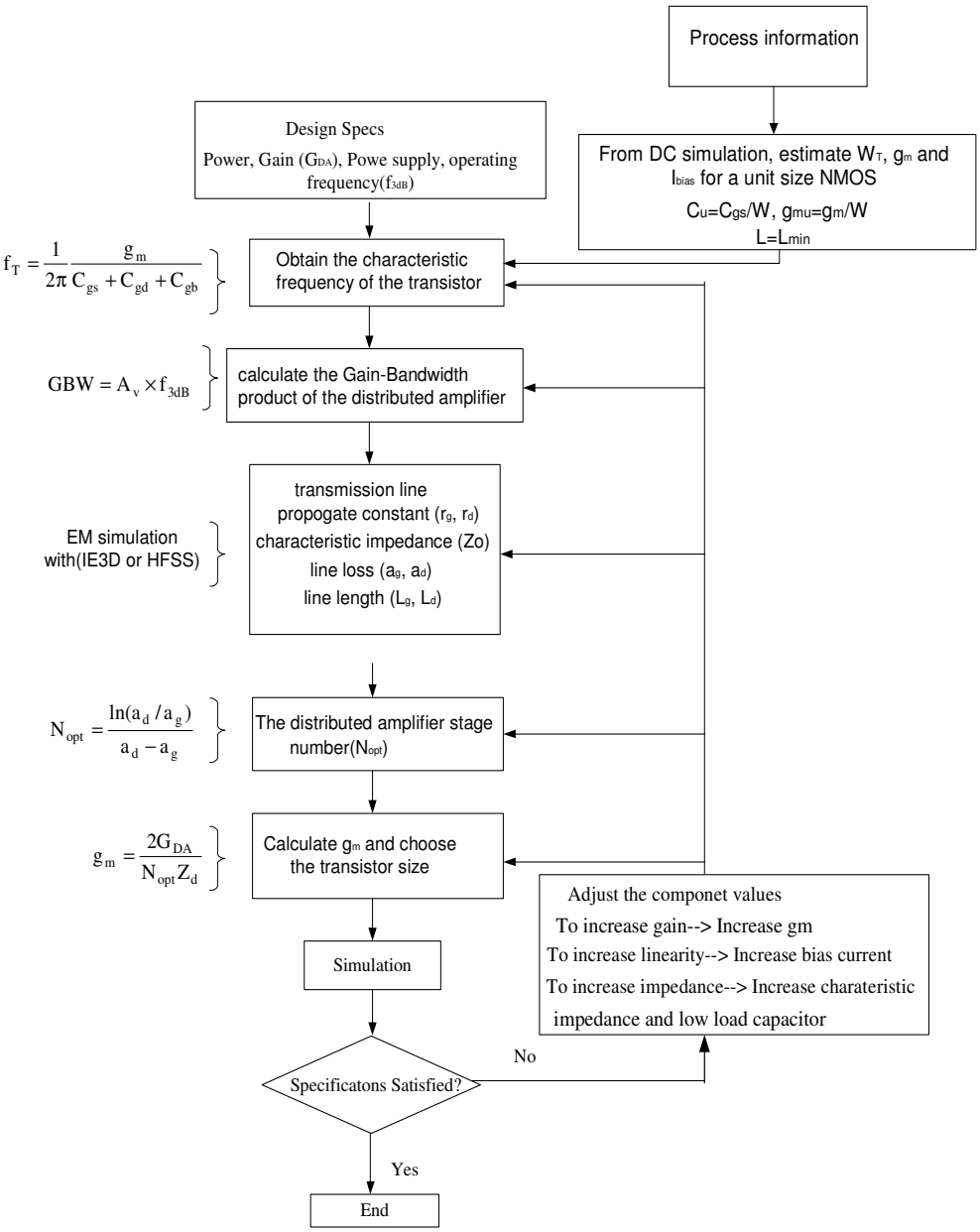


Fig. 3.49 Design procedure of the distributed amplifier

First, the unit size transistor is simulated to estimate the cut-off frequency of the process.

Second, the EM simulation software is used to simulate the transmission line. The property of the on-chip transmission line is obtained, which includes the transmission line loss, the propagation constant of the line, the transmission line length and also the characteristic impedance.

Third, according to the simulated transmission line loss, estimate the optimum distributed amplifier stage number N_opt.

And then, according to the gain requirement of the distributed amplifier, calculate the single stage amplifier transconductance.

Following that, do the simulation and verify the performance [44].

3.2.2.2 Feedback UWB LNA

The resistive shunt-feedback-based amplifier can be used for wideband applications, but suffers from poor noise figure and large power consumption.

The typical inductively degenerated common source LNA is a narrowband LNA. Its circuit and the input network are shown in Fig. 3.50.

The quality factor Q of the inductively degenerated LNA from (3.117) and Fig. 3.50 is

$$Q = \frac{1}{(R_s + \omega_T L_s)\omega C_{gs1}} \tag{3.178}$$

For narrowband application, Q is typically higher for higher gain and low noise figure, which leads to a smaller 3dB bandwidth. And thus it is unsuitable for wideband application.

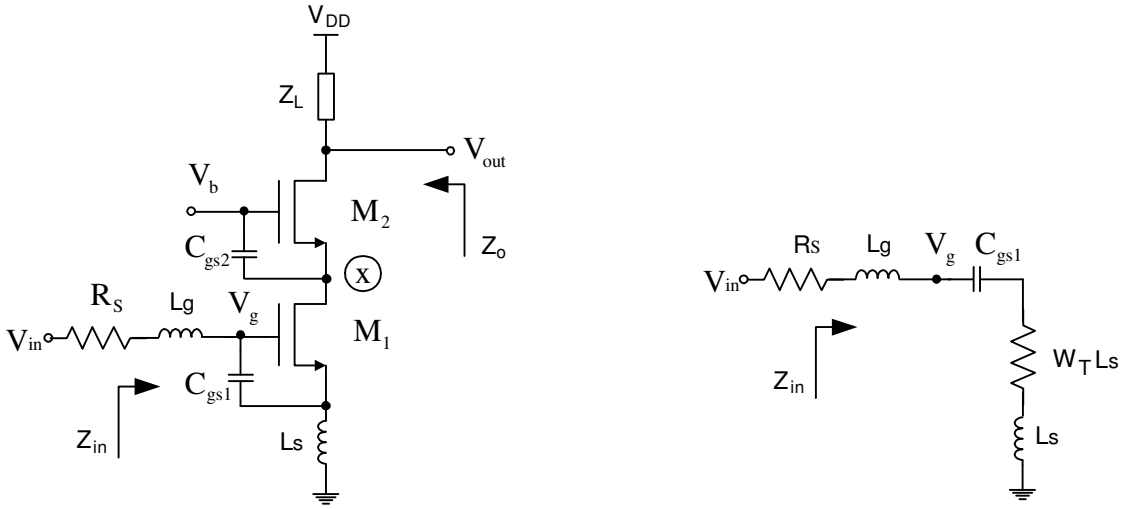


Fig. 3.50 (a) Inductively degenerated CS-LNA (b) Its equivalent input network

A modified shunt-feedback-based amplifier was proposed in [49].

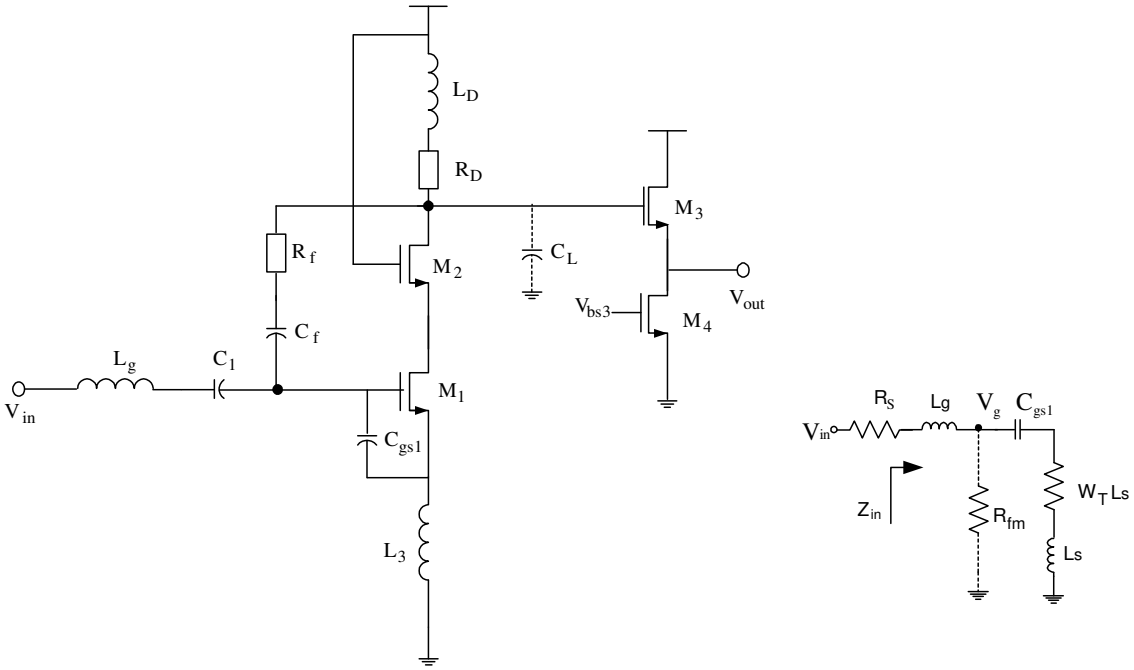


Fig. 3.51 (a) Feedback UWB LNA (b) Its equivalent input network

For a typical RLC series resonant network, the 3dB bandwidth BW is inversely proportional to the Q-factor of the network: $BW=\omega_o/Q$. For a typical narrowband CS-LNA with Q=2 and ω_o=3GHz, the 3dB bandwidth of the RLC network is 1.5GHz, which is not suitable for wideband application. Differing from the typical narrowband inductively degenerated CS-LNA, the LNA shown in Fig.3.51(a) uses a resistive feedback to lower the quality factor of the input network as in Fig.3.51(b).

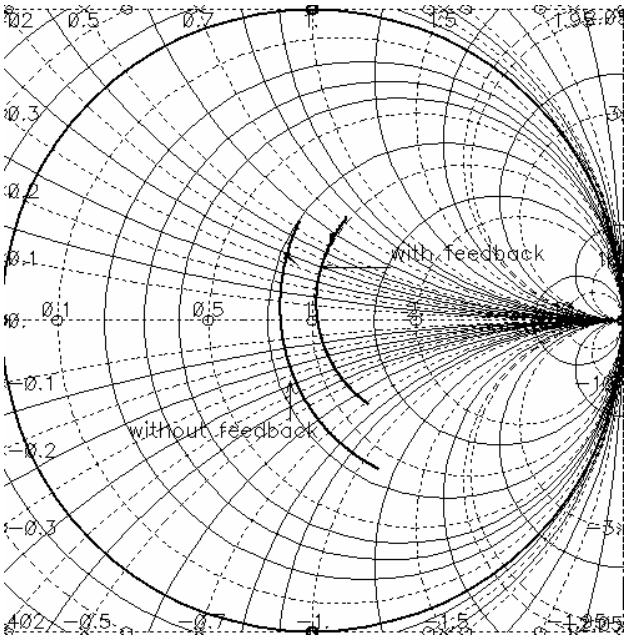


Fig. 3.52 The simulated LNA input matching with and without the feedback

From Fig. 3.52, with the feedback technique, the impedance varies less over the same frequency region due to the low Q factor network. Since the real impedance of the input network is determined by $\omega_T L_s$, the feedback resistor can be chosen larger than the typical resistive feedback LNA.

The open loop gain of the feedback network is

$$A_v \approx \frac{-\frac{1}{\omega C_{gs}}}{\left|\frac{1}{j\omega C_{gs}} + \omega L_s + \omega_T L_s\right|}\left|(j\omega L_D + R_D) // \frac{1}{j\omega C_L}\right| \tag{3.179}$$

The Miller resistor can be calculated as below, where a R_f value is assumed known.

$$R_{fm} = R_f /(1 - A_v) \tag{3.180}$$

where C_L is the overall load capacitance of the LNA.

The input network is readjusted to calculate the quality factor of the input. The parallel R_{fm} is approximately transferred to series resistor as shown in Fig. 3.53.

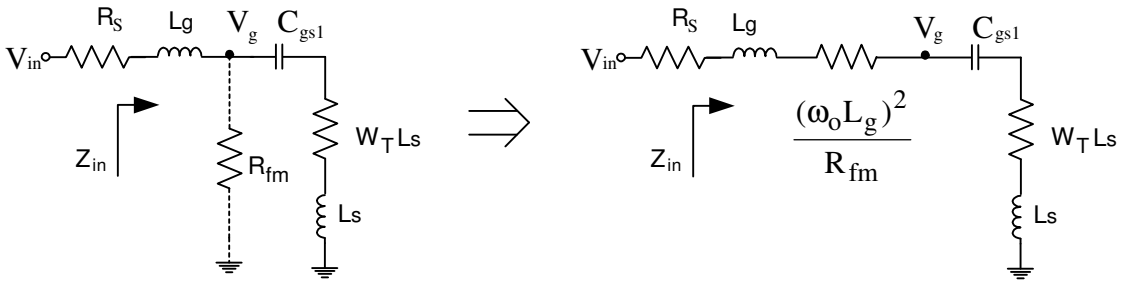


Fig. 3.53 Feedback UWB LNA input network and its transformed network

The Q of the input network is approximately as below

$$Q \approx \frac{1}{\left[R_s + \omega_t L_s + \frac{(\omega_o L_g)^2}{R_{fM}}\right] \cdot \omega_o C_{gs}} \tag{3.181}$$

where $R_{fM} = R_f /(1 - A_v)$ represents the Miller equivalent input resistance of R_f. If properly selecting the value of R_f, the input matching network can achieve the wideband matching.

For instance, a 0.18µm CMOS feedback UWB LNA [49] is used here to demonstrate the performances. The parameter is shown in Table 3.11[49]. And the simulation results are summarized in Table 3.12.

Table 3.11 Feedback UWB LNA component values

Component	Component	Value	Value
$R_f(\Omega)$	1500	L_g(nH)	2.5
M_1(µm/µm)	320/0.18	L_s(nH)	0.6
I_{bias}(mA)	7	C_f(pF)	C_f(pF)
$R_D(\Omega)$	50	VDD(V)	VDD(V)
L_D(nH)	1.3		

Table 3.12 Feedback LNA simulated performance

Parameter	Value	Parameter	Value
Freq(GHz)	3GHz-7GHz	S11(dB)	<-10
S21(dB)	14~15	NF(dB)	1.55-3.63
IIP3(dBm)	5 at 4GHz	Power(mW)	12
Process	0.18µm CMOS		

3.2.2.3 Filter based Common Source UWB LNA

Typical narrowband CS-LNA uses one inductor to resonate with the parasitic capacitor in the designed frequency, which makes the inductively degenerated CS-LNA work in the narrowband frequency region. The band pass filter uses multiple LC sections to achieve the broadband operation. A bandpass filter based UWB CMOS CS-LNA is proposed in [50], as shown in Fig. 3.54. The bipolar version is shown in [51].

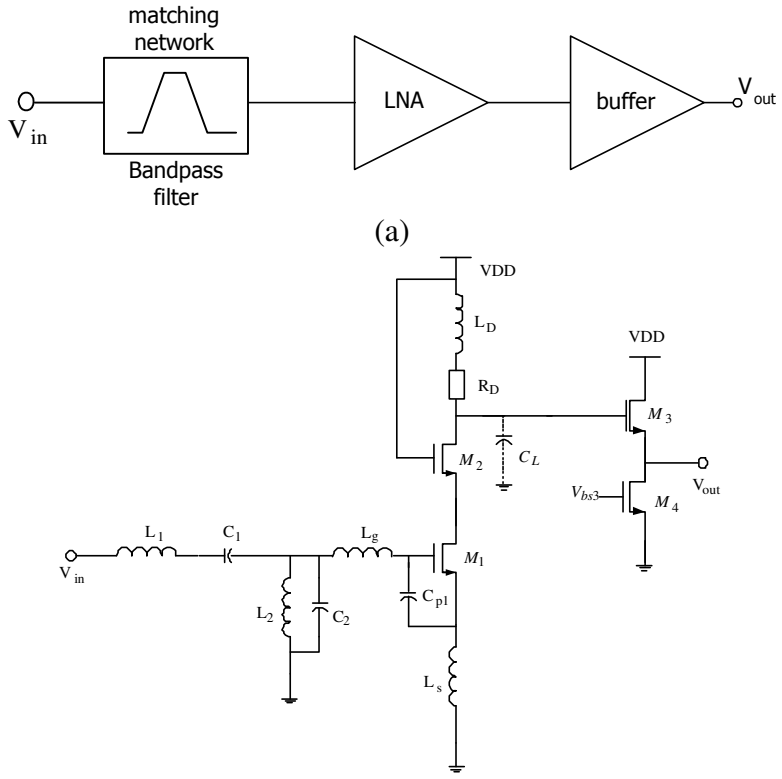


Fig. 3.54 Filter based UWB CS-LNA [50] (a) Conceptual diagram (b) LNA circuit

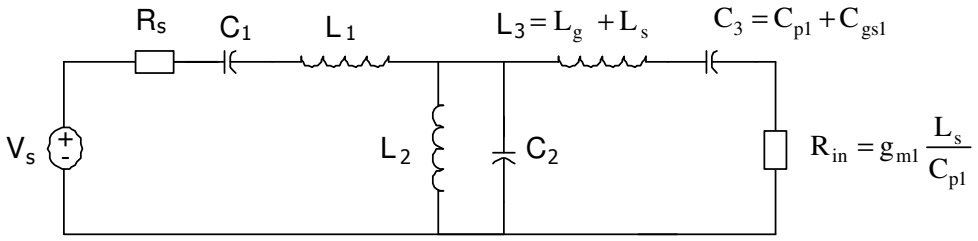


Fig. 3.55. 6th order bandpass filter

where C_L is the overall load capacitance in Fig. 3.54. The C_{p1} is added to give some freedom to pick C_{gs1} and satisfy the filter requirement.

The input forms a bandpass filter network to achieve the broadband matching shown in Fig.3.54. The bandpass filter provides a nearly constant gain ($G \approx 1$) over the operating frequency. If the filter passband has 0dB power loss, the input impedance of the circuit in Fig.3.54 can be estimated as a first order

$$R_{in} \approx g_{m1} \frac{L_3}{C_{p1} + C_{gs1}} \tag{3.182}$$

where g_{m1} is the transconductance of the transistor M_1 and C_{gs1} is the parasitic gate source capacitance of M_1.

The input network can be matched to 50Ω by implementing the bandpass filter network and designating the R_{in} as 50Ω over the wide frequency region.

Assuming the filter transfer function is $W(s)$, The UWB LNA voltage gain is

$$Z_{in} \approx -\frac{g_{m1}}{s(C_{gs1} + C_{p1})R_s} \cdot Z_L(s) \tag{3.183}$$

where $Z_L(s)$ is the overall output impedance of the load network and C_{p1} is added capacitor component in the circuits.

$$Z_{out}(j\omega) = \frac{R_D + j\omega L_D}{1 + j\omega C_L (R_D + j\omega L_D)} = \frac{R_D + j\omega L_D}{1 - \omega^2 C_L L_D + j\omega C_L R_D} \quad (3.184)$$

3.2.2.3.1 UWB CS-LNA Design Procedure

The design flow for bandpass filter based UWB LNA [50] is shown in Fig. 3.56.

First, choose the input bandpass filter type and obtain the filter components values to satisfy the corner frequency requirements. Use the filter design software, i.e. “Filter free”, to design the input network. [76]. For the given corner frequency, in this case 3GHz and 10GHz, the software can give different filter type to satisfy the requirement. According to the component values for different type filter, choose one filter type, which has practical inductor and capacitor values. Second, the input transistor is chosen to satisfy the required transconductance requirement of the input matching network. And then through the simulation, obtain the optimum transistor M1 size for minimal noise contribution. Third, the cascode device M2 size is chosen to be smaller to reduce the parasitic capacitance of the M2 transistor. It is also limited by the noise contribution of the M2. After that, the load network, which uses inductor peaking technique, is designed to achieve the gain and bandwidth requirements. The resistor R_D is chosen larger to increase the DC gain. R_D is limited by the voltage headroom. The inductor L_D is chosen to set the zero frequency to the lower frequency. Finally the simulation is processed to verify the design specifications. [50]

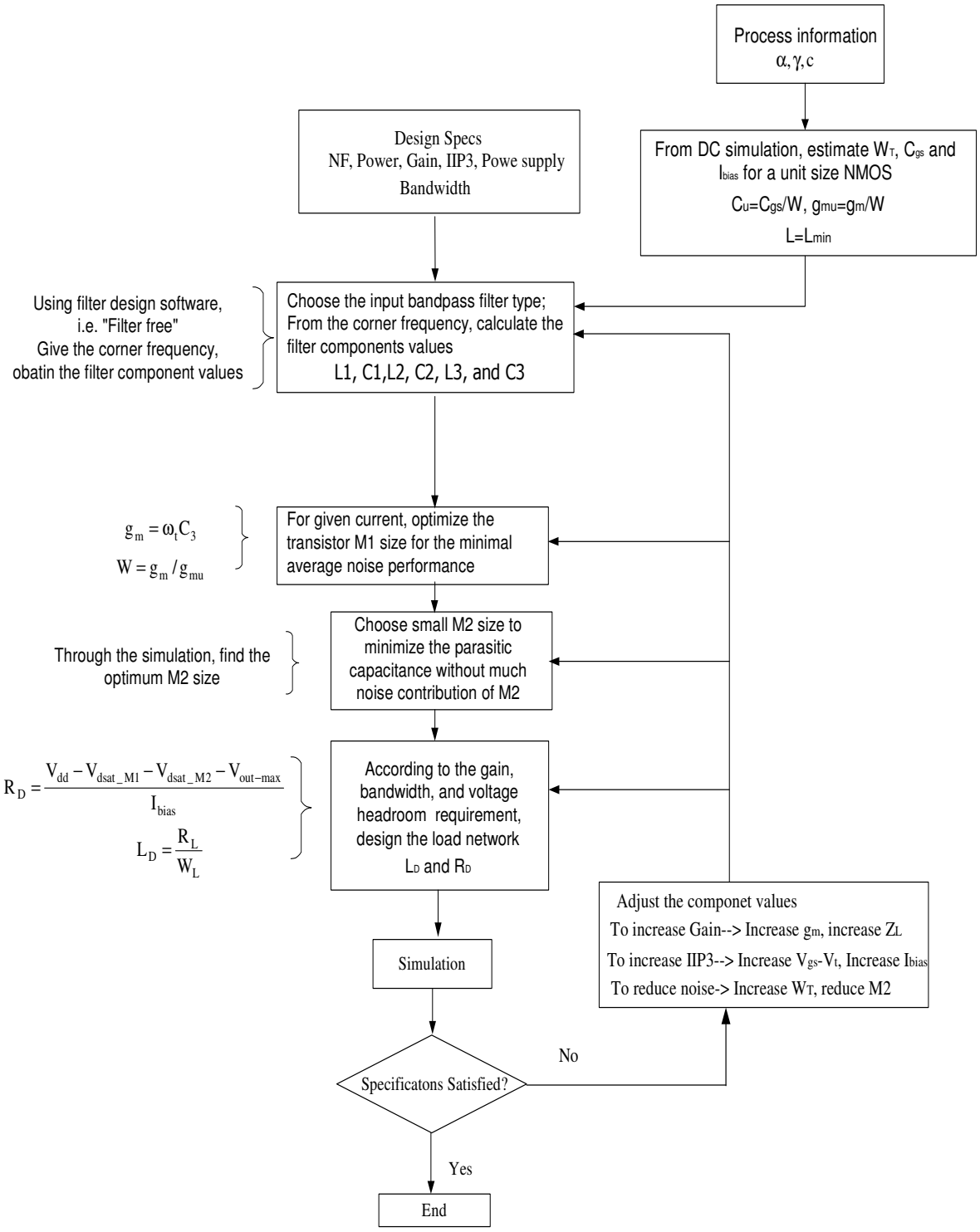


Fig. 3.56 Design procedure for filter based UWB CS-LNA

For instance, a 0.18µm CMOS filter based UWB LNA [50] is used here to demonstrate the performances. The parameter is shown in Table 3.13[50]. And the simulation results are summarized in Table 3.14.

Table 3.13 Filter based UWB LNA component values

Component	Component	Value	Value
L_1(nH)	1.33	L_2(nH)	1.6
C_1(pF)	0.65	C_2(pF)	0.49
L_g(nH)	1.4	L_s(nH)	0.68
C_{p1}(pF)	0.1	L_D(nH)	2.6
R_D(Ω)	90	M_1(µm/µm)	240/0.18
M_2(µm/µm)	60/0.18	I_{bias}(mA)	5

Table 3.14 Filter based UWB LNA simulated performance

Parameter	Value	Parameter	Value
Freq(GHz)	3GHz-10GHz	S11(dB)	<-8.5
S21(dB)	14.3~19.6	NF(dB)	3.17-6.58
IIP3(dBm)	1 at 5GHz	Power(mW)	9
Process	0.18µm CMOS		

3.2.2.4 Table of Comparison

From the previous chapters, we can get the following comparison table, Table 3.15, regarding to the distributed LNA, Feedback LNA and Filter based Cs-LNA. The distributed LNA is suitable for much wider bandwidth and much higher frequency operation. It consumes most power and occupies largest area. The feedback LNA is suitable for moderate bandwidth operation with better noise and reasonable power consumption. The filter based CS-LNA is proper choice for 3-10GHz operation. It occupies large area due to the large number of inductors.

Table 3.15 Ultra-wideband LNA comparison

	Distributed-LNA[47]	Feedback UWB LNA[49]	Filter based CS-LNA[50]
Bandwidth	>10GHz	<10GHz	Around 10GHz
Noise Figure	>5dB	>2.5dB	>3dB
LNA gain	~10dB	10~15dB	10~20dB
Input matching	Transmission line	Feedback Q reduction matching	Bandpass filter matching network
Linearity	>5dBm	-2~5dBm	-5~2dBm
Power	20~80mW	10mW	9-27mW
Area	large area	small area	moderate area

CHAPTER IV

PROPOSED NOISE REDUCTION NARROWBAND LNA*

4.1 Background

Due to the low cost and easy integration, CMOS is widely used to design wireless systems especially in the radio frequency region. Low Noise Amplifier (LNA) serves as the first building block of the wireless receiver. It needs to amplify the incoming wireless signal without adding much noise and distortion. The noise performance of the LNA dramatically influences the overall system noise performance. The inductively degenerated CS-LNA [1]-[2], [30]-[32] is widely used due to its superior noise performance. A common gate LNA (CG-LNA) can easily achieve the input impedance matching, but suffers from poor noise performance [33]. The capacitive cross-coupling technique for CG-LNA [51]-[54] partially cancels the noise contribution of the common gate transistor at the output, which improves the overall noise performance of the CG-LNA. On the other hand, due to the existence of the parasitic capacitance at the source of the cascode transistor, the cascode transistor's noise influences the overall noise performance of the CS-LNA [55]-[59]. In [57], a layout technique to merge the main transistor and the cascode transistor can reduce the cascode transistor noise contribution. Additional inductors can be added at the drain of the main

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transistor to cancel the effect of the parasitic capacitance, thus improving the noise performance of the LNA [56]-[58] at the cost of larger area for the on-chip inductors.

In this chapter, a noise reduction inductor combined with the capacitive cross-coupling technique is proposed to improve the noise and linearity performance of the differential cascode LNA. It can reduce the noise and nonlinearity contributions of the cascode transistors with smaller inductor compared with the typical inductor based technique. The capacitive cross-coupling technique used in the cascode transistors increases the effective transconductance of the cascode transistors, further improves the linearity of the LNA, and also reduces the Miller effect of the gate drain capacitance of the main transistor.

The basic inductively degenerated CS-LNA is described in Chapter III. Here we analyze the noise influence of the cascode transistors, and shows the conventional inductor based noise improvement technique. After discussing the original capacitive cross-coupling technique [52]-[54] for CG-LNA, we propose its application combined with the inductor in the cascode transistors of the differential cascode CS-LNA.

4.2 Typical Inductive Degenerated CS-LNA

The LNA noise performance dominates the overall noise performance of the receiver. The inductively degenerated CS-LNA is widely used due to its superior noise performance.

The typical inductively degenerated CS-LNA is shown in Fig. 4.1, where all parasitic capacitances other than the gate-source capacitances of M_1 and M_2 are ignored for simplicity. Only two parasitic capacitance (C_{gs1} and C_{gs2}) are drawn in the Fig. 4.1

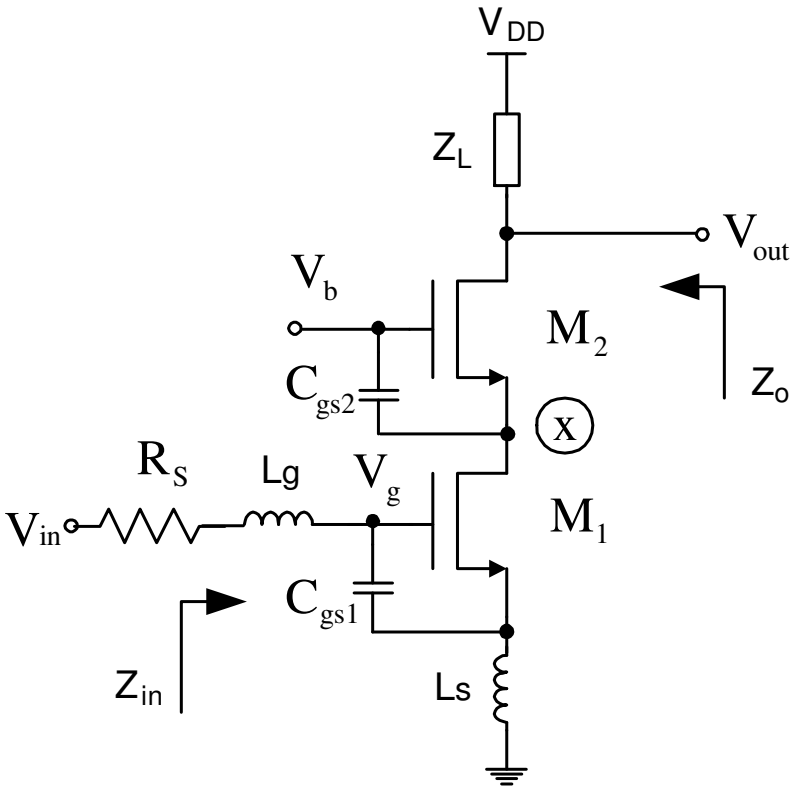


Fig. 4.1 Inductively degenerated cascode CS-LNA

The inductively degenerated CS-LNA uses an inductor L_s to generate the real impedance to match the input impedance to 50Ω, which results in good noise performance [1]-[2], [30]-[32]. If the resistive losses in the signal path, the gate resistance, and the parasitic capacitances except gate-source capacitances are ignored, the inductor loss of L_s and L_g are ignored the overall input impedance of CS-LNA can be simplified to (4.1) [1], where g_{m1} is the transconductance of M_1.

$$Z_{in}(s) \approx sL_g + sL_s + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}} \tag{4.1}$$

If the inductor L_s and L_g losses (R_{Ls} and R_l) are considered, the input impedance of CS-LNA is derived as

$$Z_{in}(s) \approx s(L_g + L_s) + \frac{1 + g_{m1}R_{Ls}}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}} + R_l \tag{4.2}$$

Since L_s is typically a small value inductor and sometimes implemented as high Q bonding wire inductor, R_{Ls} is a small value resistor associated to L_s and normally ignored in the analysis.

The small signal model of the inductively degenerated cascode CS-LNA is shown in Fig. 4.2, where C_{gd} and g_{mb} of the transistors are ignored for simplicity.

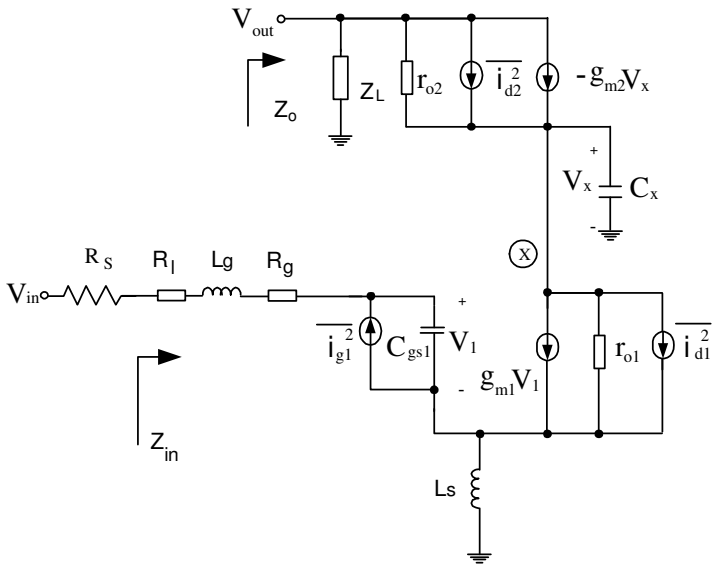


Fig. 4.2 Small signal model of cascode CS-LNA for noise analysis

where R_g is the gate resistor. The input impedance Z_{in} in (4.1) doesn't includes R_l, R_g and the loss of L_s for simplicity. Fig. 4.2 is used to analyze the noise of the CS-LNA

The capacitor C_x represents all the parasitic capacitances at node X, which include $C_{gs2}, C_{gd1}, C_{db1}$ and C_{sb2}. It is estimated as

$$C_x \approx C_{gs2} + C_{sb2} + C_{gd1} + C_{db1} \tag{4.3}$$

If the noise contribution from the cascode stage is ignored, the noise factor of the cascode CS-LNA becomes as below. The noise from the cascode stage will be discussed later.

$$F_1 = 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\frac{\omega_o}{\omega_T} \tag{4.4}$$

$$\chi = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L{}^2) \tag{4.5}$$

$$Q_L = \frac{\omega_o(L_s + L_g)}{R_s} = \frac{1}{\omega_o C_{gs} R_s} \tag{4.6}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g{}^2}\,\overline{i_d{}^2}}} \approx -0.395j \tag{4.7}$$

where (4.7) is obtained from [1] [30]-[31], R_s is the input voltage source resistance, R_g is the gate resistance of M_1, ω_o is the operating frequency, and α, γ and δ are bias-dependant parameters [1]-[2], [30]-[32].

The existence of the parasitic capacitance C_x reduces the gain of the first stage, which makes the noise contribution from the cascode stage (F_c) larger. Thus, the noise factor of the cascode CS-LNA [55] becomes

$$F = F_1 + F_c \approx F_1 + 4R_s\gamma_2 g_{do2}\left(\frac{\omega_o{}^2 C_x}{\omega_T g_{m2}}\right)^2 \tag{4.8}$$

where $\omega_T = g_{m1} / C_{gs1}$, g_{do2} is the zero-bias drain conductance of M_2 and γ_2 is the bias-dependent factor [1]. Same as in [55], the noise sources of the first stage include the gate induced noise and drain noise sources, but only the drain noise of the second stage is modeled. Including all other noise sources of the second stage only complicates the derivations while adding little accuracy to the derived formulas [51]-[56]. From (4.3) and (4.8), it can be observed that C_x increases the noise factor of the LNA. The exact percentage of noise contribution of M_2 in the overall LNA needs to simulate. For the design shown later, the M_2 contribute around 0.5dB noise degradation for the overall 2.5dB LNA NF.

The transistor M_2 helps to reduce the Miller effect of the Cgd1 of M1, to improve the input output isolation, and to increase the output impedance.

The output impedance of Fig.4.1 without the cascode transistor is

$$Z_o = Z_L // g_{m1} r_{o1} \omega L_s \tag{4.9}$$

The output impedance of Fig.4.1 with the cascode transistor is

$$Z_o = Z_L // g_{m1} r_{o1} r_{o2} \omega L_s \tag{4.10}$$

The output is a RLC resonant network as shown in Fig. 4.3. L_D is the load inductor, R_D is the parasitic resistance of L_D and C_L is the overall capacitance at the output. At the resonant frequency ω_o , Z_L can be derived as

$$Z_L = \omega_o L_D Q_L \tag{4.11}$$

where Q_L is the quality factor of the load inductor L_D.

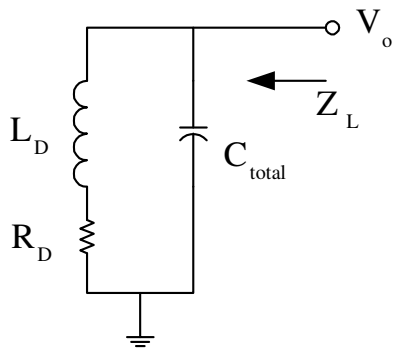


Fig. 4.3 Typical load of the CS-LNA

4.3 Existing Solution to Reduce the Noise of the Cascode Transistor

The parasitic capacitance C_x can be reduced by merging the main transistor and the cascode transistor in the layout [58]. It is depicted in Fig. 4.4 [58].

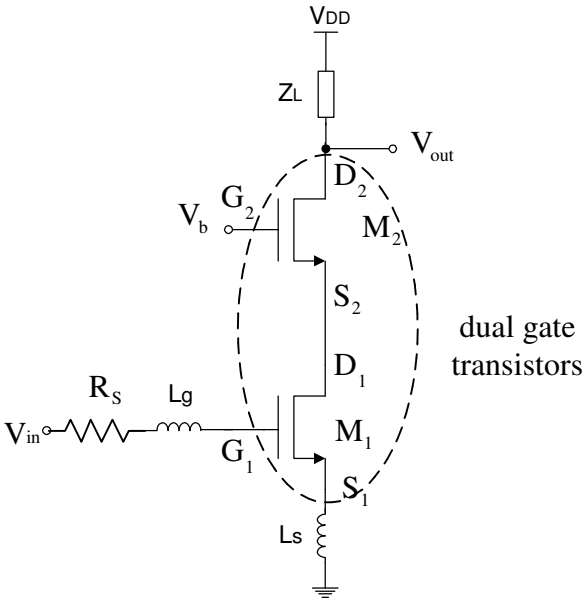


Fig. 4.4(a) CS-LNA schematic

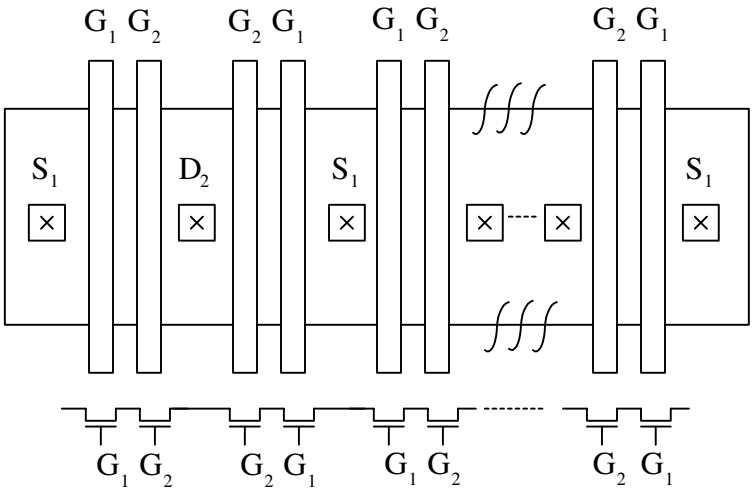


Fig. 4.4(b) Continued. Dual gate transistors layout

For the transistor M_1 and M_2, with the dual gate transistor layout, the source terminal area of M_2 and the drain terminal area of M_1 are combined. It reduces the interconnect wires between two transistors and helps to reduce the parasitic capacitor of interconnect. The parasitic capacitance of the interconnect wire is not included in the following analysis. Before the combination, C_x can be estimated as $C_{gs2}+C_{gd1}$. After the dual gate layout technique, Cx is around C_{gs2}. If Cgs2 is twice the value of C_{gd1}, one third of the C_x is reduced.

An additional inductor L_{add} was added to cancel the effect of C_x at the frequency of interest [56]-[58].

$$\omega_o^2 = \frac{1}{L_{add} C_x} \tag{4.12a}$$

or

$$C_x = \frac{1}{L_{add} \omega_o^2} \tag{4.12b}$$

where ω_o is the operating frequency of the LNA.

The basic concept is shown in Fig. 4.5.

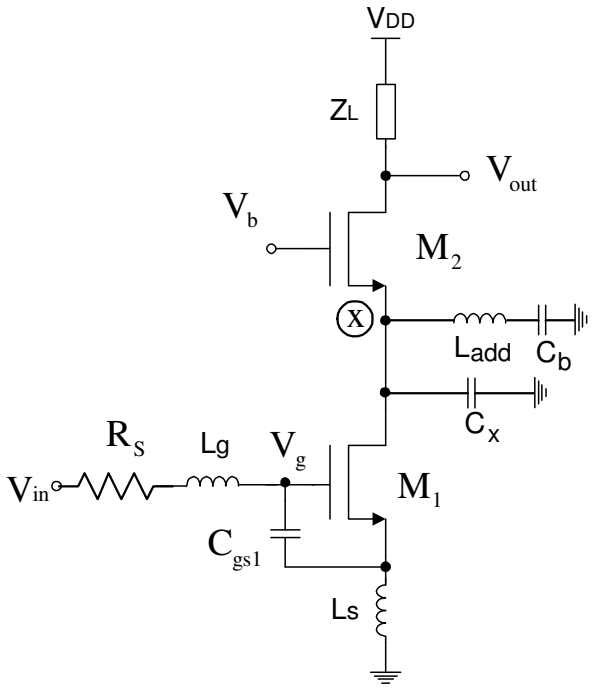


Fig. 4.5 Typical inductor based technique for cascode CS-LNA

C_b is a DC blocking capacitor, which has to be large to reduce its effect at the operating frequency of the LNA. As a result, if the r_{o1} and r_{o2} of M_1 and M_2 are large enough, the noise current generated by the cascode transistor M_2 adds negligible noise current to the output.

The large area requirement of on-chip inductor is a big concern for on-chip integration. For a typical 0.35μm CMOS technology, the parasitic capacitance for a 200μm/0.4μm NMOS transistor is nearly 0.3pF. Thus, it requires an inductor around 14nH to resonate at 2

GHz. In the advanced CMOS technology, it requires even larger inductor values. In addition, the poor quality factor of the on-chip inductor increases the overall noise figure of the LNA.

In this chapter, we propose a technique to significantly reduce the noise and nonlinearity contribution of the cascode transistors as well as the value of L_{add}.

The linearity of the LNA in Fig. 4.5 is dominated by the voltage to current conversion of the transistor M_1 [1]-[2], [64]-[65]. The added inductor L_{add} resonates with the parasitic capacitance C_x, which eliminates the linearity degradation due to the transistor M2. The linearity degradation of transistor M2 will be explained later in section 4.4.4.

4.4 Proposed Noise Reduction Technique for a Cascode LNA

4.4.1 Capacitive Cross-Coupling Technique for CG-LNA

The CG-LNA can achieve wideband input impedance matching, but suffers from poor noise performance. To alleviate this problem, a capacitive cross-coupling technique was proposed in [49]-[51] for CG-LNA. It can boost the transistor transconductance with passive capacitors, as shown in Fig.4.6. Before applying the capacitive cross-coupling technique, the original transconductance and the input capacitance are expressed as g_m and C_{gs}.

If the gate-bulk and gate-drain capacitances are ignored, the effective transconductance and input capacitance of the LNA are here derived as (4.13) and (4.14).

$$G_{m,eff} = \frac{2C_c}{C_{gs}+C_c} g_{m1} = \frac{C_{in}}{2C_{gs}} g_{m1} \tag{4.13}$$

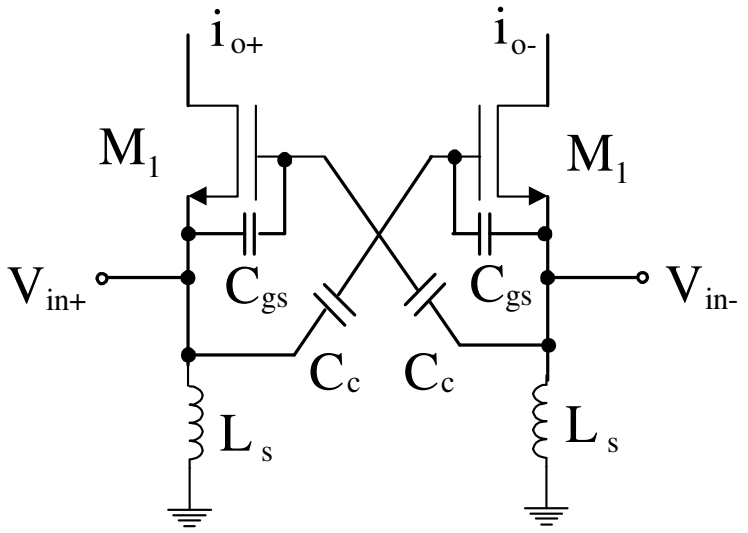


Fig. 4.6 A capacitive cross-coupled differential CG-LNA

$$C_{in} = \frac{4C_c}{C_{gs} + C_c} C_{gs} = 2\frac{G_{m,eff}}{g_{m1}} C_{gs} \tag{4.14}$$

When $C_c >> C_{gs}$, the effective transconductance is doubled, and the input capacitance is increased by four times.

It the input of the typical CG-LNA satisfies the matching condition $\frac{1}{g_{m1}R_s} \approx 1$, the noise performance of the CG-LNA without the capacitive cross-coupling technique is [54].

$$F_{CG-LNA} = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega_o}{\omega_T}\right)^2 \approx 1 + \frac{\gamma}{\alpha} \tag{4.15}$$

With the capacitive cross-coupling technique, the input of the CG-LNA should satisfy the matching condition $\frac{1}{2g_{m1}R_s} \approx 1$. The noise performance of the CG-LNA with the capacitive cross-coupling technique is

$$F_{CG-LNA\_CCC} \approx 1 + \frac{\gamma}{2\alpha} \tag{4.16}$$

From (4.15) and (4.16), the noise performance of the CG-LNA improves.

The linearity of the CG-LNA with and without the capacitive cross-coupling technique can be derived as [52]

$$IIP3_{CG-LNA} = 8\sqrt{\frac{2 \cdot G_s}{3 \cdot \left| -3K_{3gm} + K_{2gm}{}^2 / G_s \right|}} \tag{4.17}$$

$$IIP3_{CG-LNA\_CCC} = 4\sqrt{\frac{G_s}{3 \cdot \left| 3K_{3gm} \right|}} \tag{4.18}$$

where G_s is the source conductance, K_{3gm} is the 3rd order nonlinearity of M_1 and K_{2gm} is the 2nd order nonlinearity of M_1. The IIP3 is calculated using (41.7) and (4.18). It is decided by the value of K_{3gm} and K_{2gm}. An example using the 0.18µm CMOS process is given below. For a NMOS transistor with W=83µm and L=0.18µm, biased with 0.58V V_{gs}, through the simulation, its K_{3gm} is 0.44 and its K_{2gm} is 0.14. At this condition, the IIP3 of the CG-LNA is calculated as 1.58dBm using (4.17), and the IIP3 of the CG-LNA with the capacitive cross-coupling technique is calculated as 0.28dBm using (4.18). The typical CG-LNA has better linearity. For a NMOS transistor with W=83µm and L=0.18µm, biased with 0.61V V_{gs}, through the simulation, its K_{3gm} is -0.031 and its K_{2gm} is 0.144. At this condition, the IIP3 of the CG-LNA is calculated as 0.89dBm using (4.17), and the IIP3 of the CG-LNA with the capacitive cross-coupling technique is calculated as 1.07dBm using (4.18). The CG-LNA with the capacitive cross-coupling technique has the better linearity by 0.18dBm.

4.4.2 Proposed Noise Reduction Cascode CS-LNA

The inductively degenerated cascode CS-LNA can be considered as a CS-CG two stage LNA. The CS stage is designed to achieve the input impedance matching and also to obtain best noise performance. The input voltage signal is converted to current through the CS transistor. The cascode transistor works as a CG stage. It is designed mainly to reduce the Miller effect of the parasitic gate-drain overlap capacitance in the CS transistor. It also helps to increase the output impedance and to improve the input-output isolation.

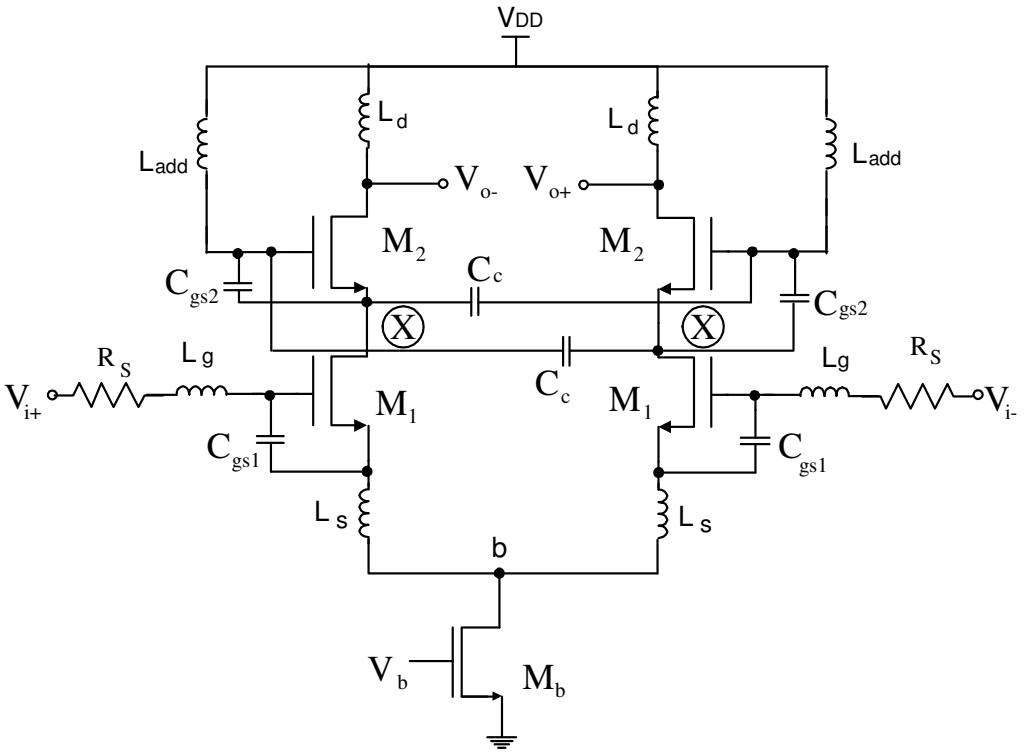


Fig. 4.7 The inductor combined with capacitive cross-coupling technique in a fully-differential cascode CS-LNA

An additional inductor L_{add} combined with the capacitive cross-coupling technique is applied to the cascode transistors of the differential LNA to reduce the noise. The proposed topology is implemented in a fully-differential inductively degenerated CS-LNA as shown in Fig. 4.7.

4.4.3 Noise Effect of the Proposed Noise Reduction Technique for a Differential Cascode CS-LNA

The effective transconductance of the cascode transistor in Fig. 4.7 is expressed as

$$G'_{m,eff} = \frac{2\omega C_c - \frac{1}{\omega L_{add}}}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} g_{m2} \tag{4.19}$$

The equivalent input susceptance at node X is not purely capacitive, which is derived as

$$B'_{eff} \cong \frac{4\omega C_c}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} \omega C_{gs2} + \frac{(\omega C_c + \omega C_{gs2}) \times (-\frac{1}{\omega L_{add}})}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} + \omega C_{db2} + \omega C_{gd1} + \omega C_{sb2} \tag{4.20}$$

where the other parasitic capacitances are ignored. If $\omega C_c >> \omega C_{gs2}$ and $\omega C_c >> \omega C_{gs2} - \frac{1}{\omega L_{add}}$, the effective transconductance is doubled and the equivalent susceptance becomes

$$B_{eff}^{'} \cong \frac{\omega C_c (4\omega C_{gs2} - \frac{1}{\omega L_{add}})}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1} \tag{4.21}$$

When (4.21) equals to zero, the capacitive effect at node X is mainly eliminated, which leads to

$$L_{add} \approx \frac{1}{\omega_o{}^2 (4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})} \tag{4.22}$$

Using the small signal model, the noise figure of the cascode LNA yields

$$F^{'} = F_1 + F_c^{'} = F_1 + 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o B_{eff}^{'}}{\omega_T G_{m,eff}^{'}} \right)^2 \tag{4.23}$$

Since the effect of the parasitic capacitance at node X is cancelled as in (4.21)-(4.23), the noise of the cascode transistors F_c is negligible.

The inductor L_{add} can be implemented with either on-chip inductor or bonding wire inductor. Its value is reduced by a factor of 3 with respect to the typical inductor based technique [56]. Here L_{add} is implemented as a bonding wire inductor. Since now the gates of M_2 are connected out of the chip using the bonding wire inductor, it is desired to add ESD protection structures for these pads. In this design, to verify the proposed concept and to get the optimal results, there are no ESD protection structures for these pads. If the ESD protection circuit [58] is used, it can be modeled in first order as a grounded capacitor parallel with the bonding wire inductor. The parallel LC network should be used to replace the L_{add} in the analysis used in this paper.

The LNA in Fig. 4.7 is designed with TSMC 0.35μm CMOS technology and the noise performance is shown in Fig. 4.8. L_g is an ideal inductor, while L_s and L_d are on-chip spiral inductors, which are modeled as pi model using ASITIC software [60]-[61]. The proposed technique reduces the differential cascode CS-LNA NF from 2.22dB to 1.87dB. It will be more significant for the LNAs working at higher frequency. At the lower frequency, L_{add} short circuited the gates of the cascode transistors to V_{DD} supply (AC ground). In that case, the total capacitive effects at node X in Fig. 4.7 are not zero and the LNA has worse noise performance.

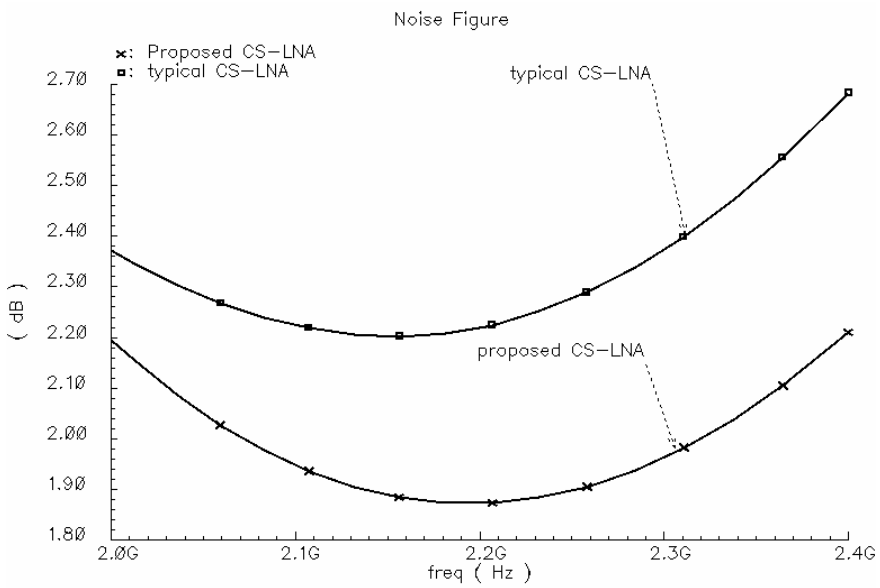


Fig. 4.8 Simulation results of the differential cascode CS-LNA with/without L_{add} and C_c

The bonding wire inductance has different PVT values. Assume the L_{add} value has 10% variation denoted as ΔL_{add}. From (4.21)-(4.23), at the operating frequency, we can get

$$\Delta G'_{m,eff} = G'_{m,eff}(L_{add} + \Delta L_{add}) - G'_{m,eff}(L_{add}) \cong 0 \tag{4.24}$$

$$\Delta B'_{eff} = B'_{eff}(L_{add} + \Delta L_{add}) - B'_{eff}(L_{add}) \cong \frac{1}{\omega_o L_{add}} \times \frac{\Delta L_{add}}{L_{add}} \tag{4.25}$$

$$\begin{aligned} \Delta F' &= F'(L_{add} + \Delta L_{add}) - F'(L_{add}) \cong 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o \Delta B'_{eff}}{\omega_T G'_{m,eff}} \right)^2 \\ &= 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o (4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})}{\omega_T G'_{m,eff}} \right)^2 \times \left(\frac{\Delta L_{add}}{L_{add}} \right)^2 \end{aligned} \tag{4.26}$$

From (4.24)-(4.26), even with 10% variation in L_{add} value, the proposed technique can achieve around 96% noise reduction for the cascode device, assuming the ideal L_{add} can entirely eliminates the cascode transistor noise contribution. The noise performance of the LNA with varied inductor L_{add} value is shown in Fig. 4.9. The NF varied less than 0.01dB.

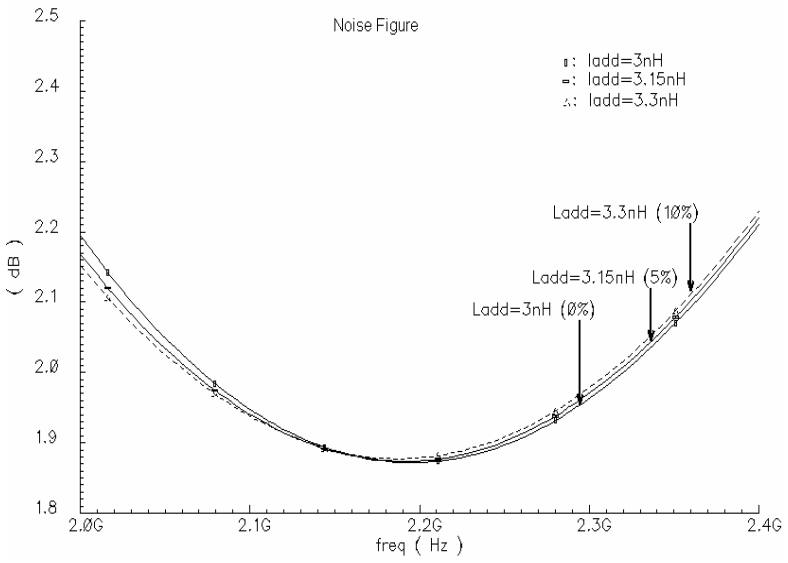


Fig. 4.9 Simulated NF of the differential cascode CS-LNA with the inductor L_{add} value varied from 0% to 10%

The LNA NF varies with temperature. The noise reduction with the proposed technique through temperature variation is summarized in Table 4.1.

Table 4.1 NF improvement versus temperature

	-45°C	27 °C	85 °C
NF without proposed technique	1.59dB	2.22dB	3.22dB
NF with proposed technique	1.42dB	1.87dB	2.4dB
NF improvement	0.17dB (11%)	0.35dB (16%)	0.82dB (27%)
nominal NF	2.22dB		

Since the noise of the transistor increases with the increasing temperature, the absolute value of the cascode transistor noise contribution also increases. Thus if it is ideally eliminated, the absolute noise reduction value becomes larger at higher temperature.

4.4.4 LNA Linearity Improvement with the Proposed Technique

The LNA linearity is normally dominated by the voltage to current conversion transistor in CS stage. If the gain of the first stage is greater than one, the second stage linearity plays a more important role [59]. Since the cascode CS-LNA can be treated as a CS-CG two stage amplifier, the linearity of the proposed topology is analyzed in two parts: 1) the linearity of the first voltage to current conversion stage; 2) the linearity of the cascode stage.

The linearity of the common source MOS transistor or common emitter bipolar transistor is well documented in the literature [62]-[67]. The linearity of the first voltage to current conversion stage is analyzed based on Fig.4. 10.

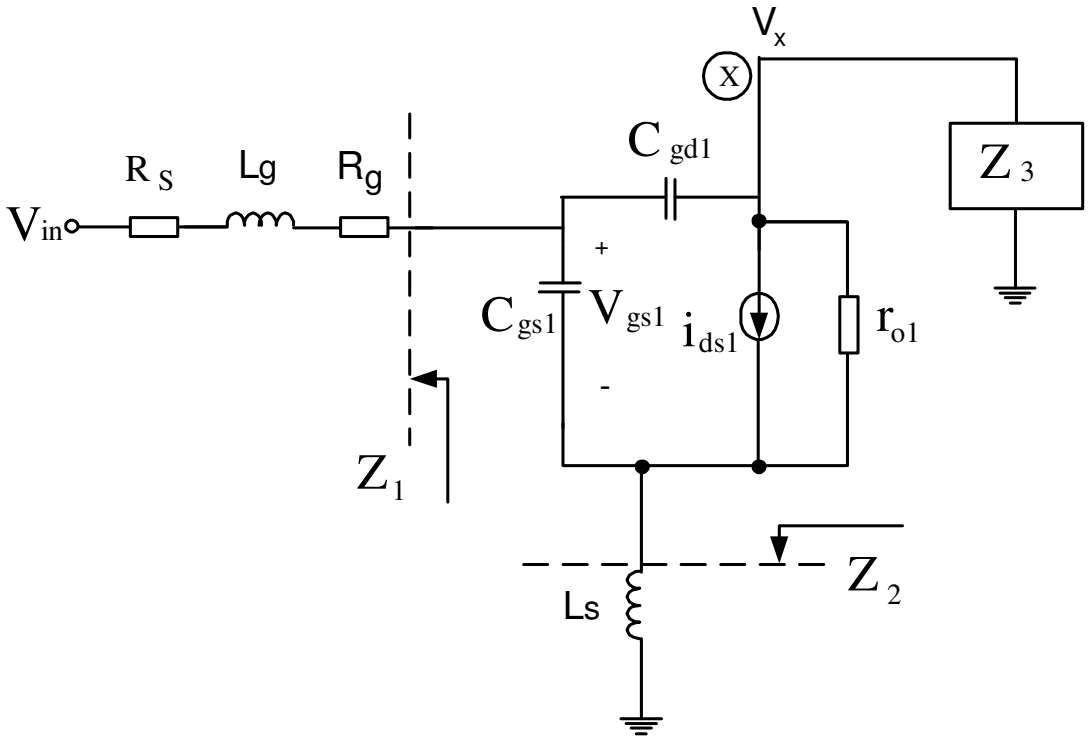


Fig. 4.10 Analyzed CS stage of cascode CS-LNA equivalent circuit

The drain currents of M1 and M2 in Fig.4.7 can be expressed as below up to 3rd order

$$i_{ds} \approx I_{DC} + g_m V_{gs} + g_2 V_{gs}^{\ 2} + g_3 V_{gs}^{\ 3} \tag{4.27}$$

The IIP3 of the first voltage to current conversion stage can be derived using Volterra series as [59]-[61] [see Appendix C]

$$IIP_3 = \frac{1}{6R_s \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|} \tag{4.28}$$

$$\varepsilon(\Delta\omega,2\omega) = g_3 - g_{oB} \tag{4.29}$$

$$g_{oB} = \frac{2}{3} g_2^2 \left[\frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)}\right] \tag{4.30}$$

$$g(\omega) = \frac{1 + j\omega C_{gd}[Z_1(\omega) + Z_3(\omega)] + j\omega C_{gs}[Z_1(\omega) + Z_x(\omega)]}{Z_x(\omega)} \tag{4.31}$$

$$Z_x(\omega) = Z_2(\omega) + j\omega C_{gd}[Z_1(\omega)Z_2(\omega) + Z_1(\omega)Z_3(\omega) + Z_2(\omega)Z_3(\omega)] \tag{4.32}$$

where ω is the center frequency of two input tones: ω_1 and ω_2, $\Delta\omega = |\omega_1 - \omega_2|$, $|H(\omega)|$ relates the equivalent input IM3 voltage to the IM3 response of the drain current non-linear terms, $A_1(\omega)$ is the linear transfer function from the input voltage V_{in} to the gate-source voltage V_{gs1}. $\varepsilon(\Delta\omega,2\omega)$ shows the nonlinear contributions from the second and third order terms in (4.25). For a MOS transistor, it can be found that g_3 and g_{oB} have different signs. From (4.26)-(4.28), the reduction of g_3 and g_{oB} can improve the IIP3.

Z_3 is the impedance looking out of the drain of the main transistor M_1. For the conventional cascode CS-LNA, its relation with the cascode transistor M_2 is described as

$$Z_3(\Delta\omega) \approx \frac{1}{g_{m2}} \tag{4.33}$$

$$Z_3(2\omega) \approx \frac{1}{g_{m2} + j2\omega C_{gs2}} \tag{4.34}$$

From (4.17)-(4.18), for our proposed LNA, the above values become

$$Z_3'(\Delta\omega) = \frac{1}{G'_{m,eff}(\Delta\omega) + B'_{eff}(\Delta\omega)} \approx \frac{1}{g_{m2}} \tag{4.35}$$

$$Z_3'(2\omega) = \frac{1}{G'_{m,eff}(2\omega) + B'_{eff}(2\omega)} \approx \frac{1}{2g_{m2} + j8\omega C_{gs2}} \tag{4.36}$$

Z_3 is the same at $\Delta\omega$, and is smaller at 2ω for the proposed LNA. From (4.28)-(4.36), we can find that the proposed LNA reduces the load impedance of the main transistor M_1 and therefore reduces g_{oB} and $\varepsilon(\Delta\omega,2\omega)$, resulting in a higher IIP3.

The linearity of the cascode stage is next analyzed based on Fig. 4.11, where currents i_{1+} and i_{1-} are the differential input signals and i_{d+} and i_{d-} are the differential output signals.

For the cascode stage without the proposed technique, we can express i_d as

$$i_d = i_1 - g(\omega) \cdot V_{gs2} \tag{4.37}$$

where i_1 is the differential input current ($i_{1+} - i_{1-}$), i_d is the differential output current ($i_{d+} - i_{d-}$), V_{gs2} is the gate-source voltage of the cascode transistor, and

$$g(\omega) = j\omega C_{gs2} \tag{4.38}$$

From (4.37)-(4.38), due to C_{gs2}, the nonlinearity of transistor M_2 influences the overall linearity of the LNA. The A_{IIP3} of the cascode stage without the proposed technique can be derived using Volterra series as

$$A_{IIP_3}^2 = \frac{4}{3} \cdot \frac{1}{|H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega,2\omega)|} \tag{4.39}$$

where $\varepsilon(\Delta\omega,2\omega)$ and g_{oB} are defined the same as in (4.29) and (4.30).

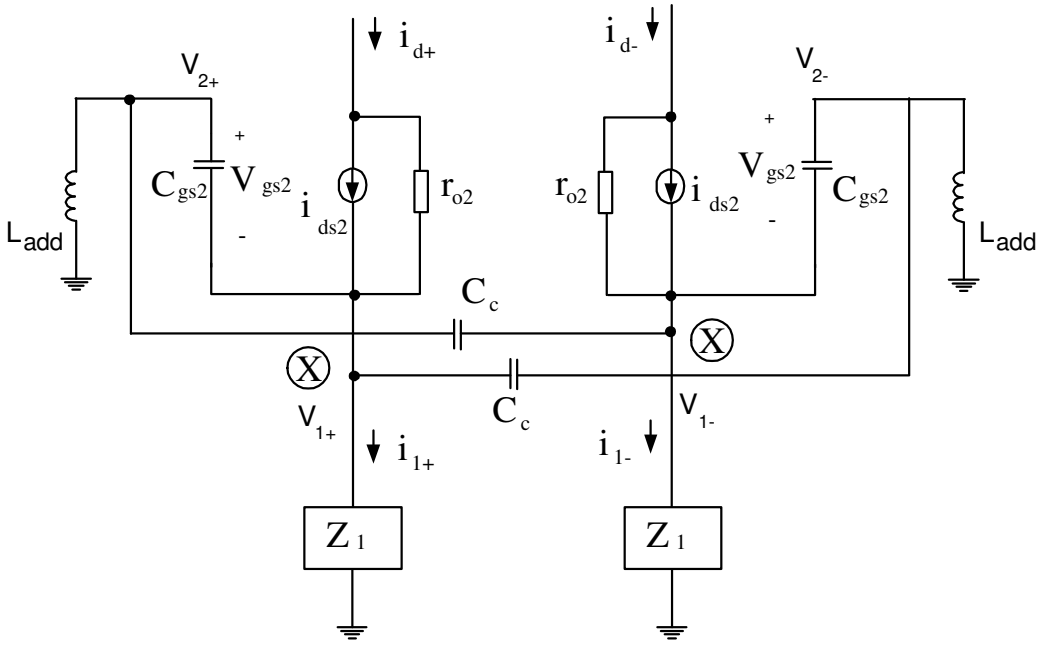


Fig. 4.11 Analyzed cascode stage equivalent circuit

$$H(\omega) = \frac{g(\omega)}{g_m} \tag{4.40}$$

$$A_1(\omega) = \frac{1}{g_m + g(\omega)} \tag{4.41}$$

For the cascode stage with the proposed technique, we can get

$$i_d = i_1 - g'(\omega) \cdot V_{gs2} \tag{4.42}$$

$$g'(\omega) = \frac{4j\omega C_{gs2} \cdot j\omega C_c + \frac{1}{j\omega L_{add}}(j\omega C_{gs2} + j\omega C_c)}{2j\omega C_c + \frac{1}{j\omega L_{add}}} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1} \tag{4.43}$$

If $\omega C_c >> \omega C_{gs2}$, $\omega C_c >> \omega C_{gs2} - \frac{1}{\omega L_{add}}$ and inductor L_{add} resonates with the effective capacitance at node X, (4.43) changes to

$$g'(\omega) \approx \frac{1}{j\omega L_{add}} + 4j\omega C_{gs2} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1} \approx 0 \tag{4.44}$$

and (4.40) changes to

$$i_d = i_1 - g'(\omega) \cdot V_{gs2} \approx i_1 \tag{4.45}$$

According to (4.45), there is no linearity degradation from the cascode stage.

A_{IIP_3} of the cascode stage with the proposed technique has the same expression as (4.34) but with different $g(\omega)$ defined as in (4.44). From the simulation, the proposed technique increases the linearity by 2.35dBm as shown in Fig. 4.12.

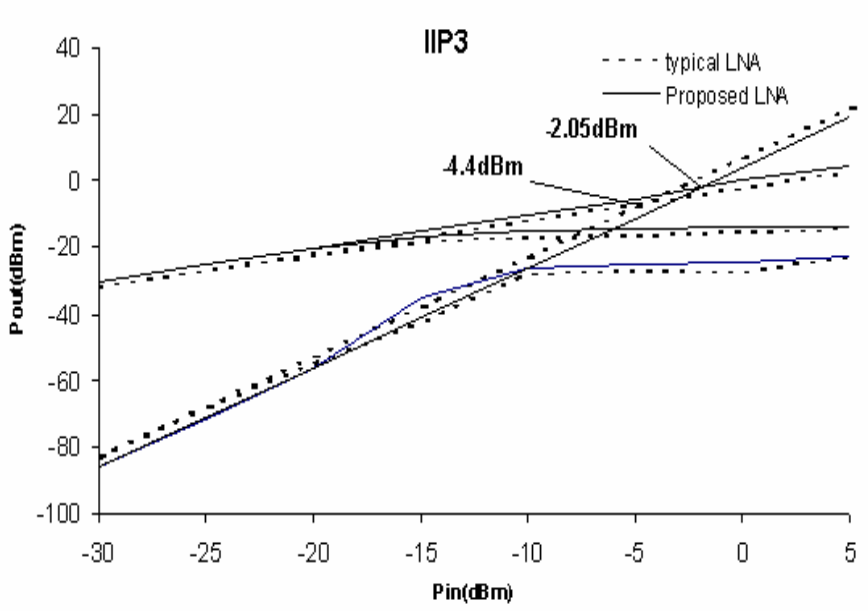


Fig. 4.12 IIP3 of the differential cascode CS-LNA with and without L_{add} and C_c

Table 4.2 IIP3 versus L_{add}

	Typical LNA	Proposed LNA with varied L_{add}		
		3nH (0%)	3.15nH (5%)	3.3nH (10%)
IIP3(dBm)	-4.4	-2.05	-2.3	-2.5
IIP3 improvement(dBm)	~	2.35(53%)	2.1(48%)	1.9(43%)

From (4.42)-(4.45), the inductor L_{add} is better to resonate with the effective capacitance at node X to completely remove the nonlinearity contribution from the cascode transistor M_2. The linearity improvement will vary with different L_{add} values due to the PVT variation. The IIP3 of LNA is shown in Table.4.2. It varied less than 1.2dBm with inductor value varied from 0% to 10%. From (4.28)-(4.45), we can draw the conclusion that the capacitive cross-coupling technique increases the effective transconductance of the cascode stage, reduces the load impedance of the main transistor M_1 and thus improves the linearity of CS stage of the LNA. The inductor L_{add} removes the capacitive effects at node X and therefore eliminates the nonlinearity contribution from the cascode stage. In sum, the proposed technique improves the cascode CS-LNA linearity.

4.4.5 Effects of the Technique on the LNA S11

For the typical cascode CS-LNA, C_{gd1} of the transistor M_1 reflects Miller impedance at the gate of M_1. It is not purely capacitive and its susceptance is derived as

$$B_{mil1}(j\omega) = (1 + Av(j\omega)) \times sC_{gd1} = \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \dfrac{L_s}{C_{gs1}} - L_s C_{gs1}} \times \frac{1}{g_{m2} + j\omega C_x} \tag{4.46}$$

where $Av(j\omega)$ is the voltage gain from the gate to the drain of M1, and C_x is defined in (4.3). For the proposed LNA, it changes to

$$B_{mil1}'(j\omega) = (1 + Av'(j\omega)) \times sC_{gd1} = \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \dfrac{L_s}{C_{gs1}} - L_s C_{gs1}} \times \frac{1}{G'_{m,eff} + jB'_{eff}} \tag{4.47}$$

where $G'_{m,eff}$ and B'_{eff} are defined in (4.19)-(4.20). According to (4.46)-(4.47), since the effective transconductance of the cascode stage increases, the gain of the first stage reduces, which leads to less Miller effect of C_{gd1} of transistor M_1. Therefore the input matching is not very sensitive to the variations of the inductor L_{add}. According to Fig. 4.13, the input resonant frequency varied less than 1% for 10% variation in L_{add} value.

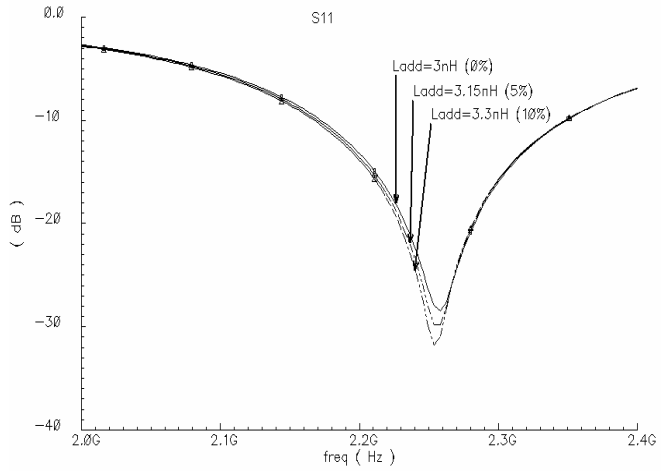


Fig. 4.13 Simulated S11 of the CS-LNA with the inductor L_{add} value varied from 0% to 10%

4.4.6 Effects of the Technique on the LNA Voltage Gain

Under the input impedance matched condition, the voltage gain of the inductively degenerated cascode CS-LNA can be derived from Fig.4.1 and Fig. 4. 2.

$$\begin{aligned} A_v(j\omega) &= g_{m1}\frac{1}{2R_s\omega_o C_{gs1}}\frac{g_{m2}}{\sqrt{(g_{m2})^2+(\omega_o C_x)^2}}Z_o \\ &= g_{m1}Q_{in}Z_o\frac{g_{m2}}{\sqrt{(g_{m2})^2+(\omega_o C_x)^2}} \end{aligned} \tag{4.48}$$

where $Q_{in}=\dfrac{1}{2R_s\omega_o C_{gs1}}$ is the quality factor of the LNA input network and Z_o is the overall output impedance. With the proposed technique, the cascode CS-LNA gain of Fig. 4.7 becomes

$$A_v(j\omega) = g_{m1}Q_{in}Z_o\frac{G'_{m,eff}}{\sqrt{\left(G'_{m,eff}\right)^2+\left(B'_{eff}\right)^2}} \tag{4.49}$$

$G'_{m,eff}$ and B'_{eff} are defined in (4.19)-(4.20).

The gain of the designed fully-differential CS-LNA is shown in Fig. 4.14, where the LNA drives 50Ω resistor. According to (4.48)-(4.49) and simulation results in Fig. 4.14, the proposed technique increases the overall LNA gain by around 2dB. In most of the wireless transceivers, the following stage of the LNA is a mixer. It is a capacitive load rather than 50Ω, which is the case in this simulation. A source follower buffer is added after the LNA to drive the 50Ω load. Since the buffer provides a 250fF capacitive load rather than 50Ω resistive load, the LNA voltage gain increases to 20.4dB as shown in Fig. 4.15.

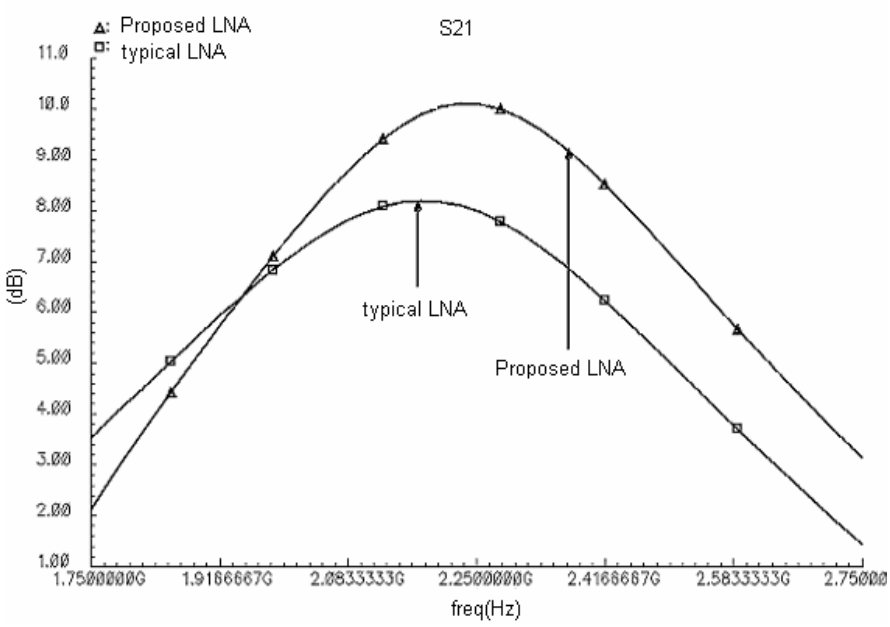


Fig. 4.14 S21 simulation results of the fully-differential cascode CS-LNA with and without L_{add} and C_c

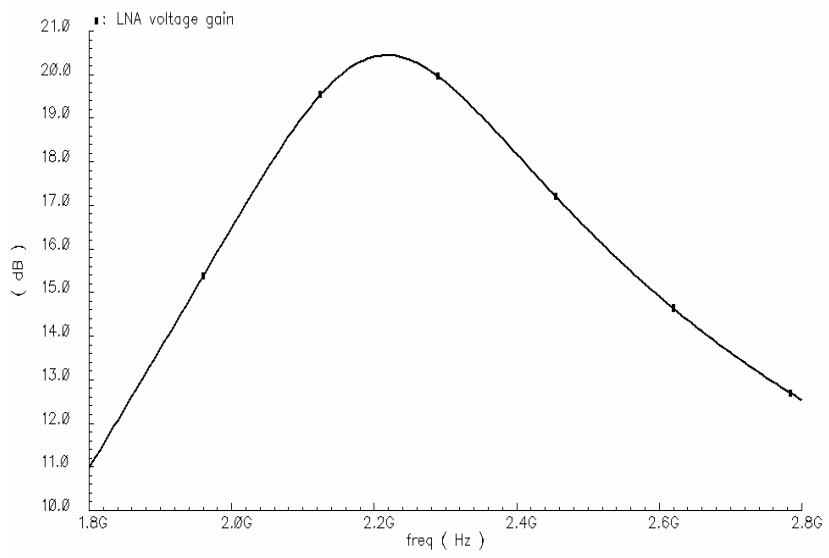


Fig. 4.15 Voltage gain simulation results of the fully-differential cascode CS-LNA with only a load capacitance of 250fF

4.4.7 Effects of the Technique on the LNA S12

The S12 reflects the input output isolation of the LNA. Compared with the typical LNA, the added inductor Ladd in the gate of the cascade transistor M2 along with the inherent capacitances provides a low impedance path for the output signal feedback to the input, which helps to improve the input output isolation [68]. The cross-coupling capacitor Cc forms a signal path from the gate of the cascade transistor M2 to the source of M2, which reduces the isolation effect of the transistor M_2. The proposed technique presents an overall comparable isolation effect with the typical LNA, as shown in Fig. 4.16. The proposed LNA has around 3dB worse S12 value.

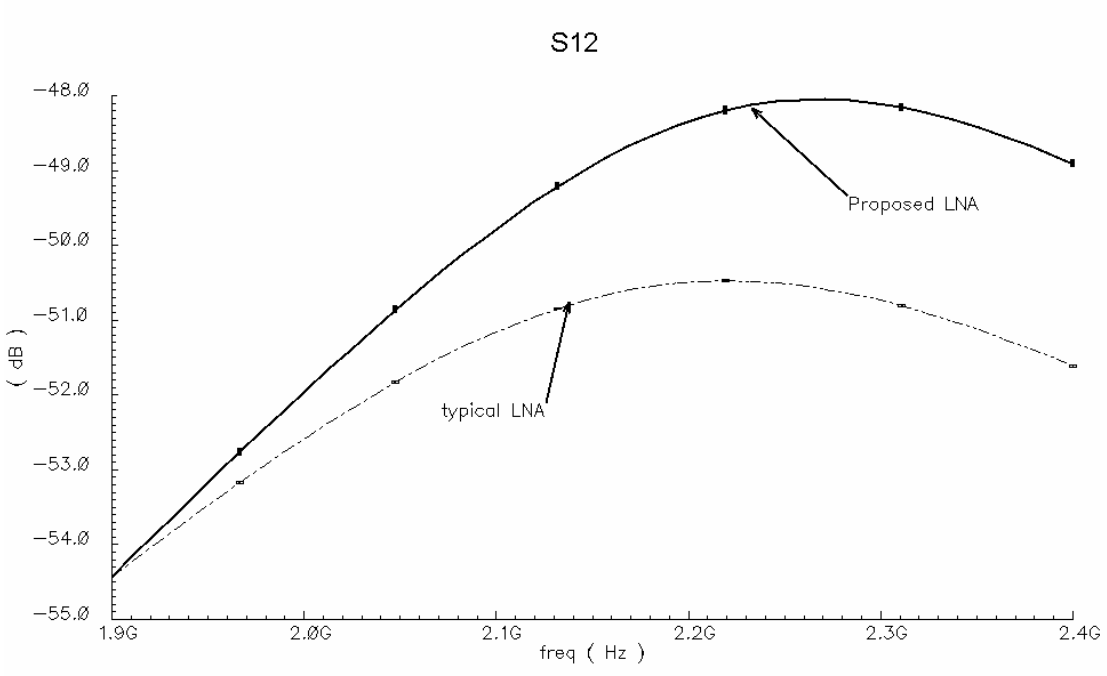


Fig. 4.16 S12 simulation results of the fully-differential cascode CS-LNA with and without L_{add} and C_c

Table 4.3 Comparison of the proposed CS-LNA with the conventional CS-LNA

Parameters	Conventional	Proposed
Frequency(GHz)	2.2Hz	2.2GHz
S11(dB)	<-10	<-10
S21(dB)	8	10
NF(dB)	2.22	1.87
IIP3(dBm)	-4.4	-2.05
Power (mW)	16.2	16.2
Process	0.35µm CMOS	0.35µm CMOS

The comparison of the proposed CS-LNA with the conventional CS-LNA is summarized in Table 3. The proposed CS-LNA reduces the noise contribution of the cascode transistor M_2, and therefore improves the noise performance of the LNA. The voltage to current conversion through the transistor M_1 linearity is improved due to the lower impedance seen out of the drain of the main transistor M_1. After apply the proposed technique, the nonlinearity degradation due to the cascode transistor M2 is also eliminated. The overall linearity performance of the proposed CS-LNA is better than the conventional CS-LNA. There is also gain improvement of the proposed CS-LNA.

4.5 Circuit Design Consideration, Design Procedure , Testing Setup and Experiment Results

4.5.1 Design Procedure

A fully-differential cascode CS-LNA was designed and fabricated using a proposed inclusive noise reduction and linearity improvement technique. Its design procedure is similar to the typical inductively degenerated CS-LNA design procedure in Fig. 3.26 except the cascode stage. The design procedure of the proposed LNA is shown in Fig. 4.17. It shares the same procedure to design the input network, the transistor M_1, and the LNA load network. The only difference lies in the cascode stage with cross coupling capacitor C_c and the added inductor L_{add}. The main target of this design is to verify the proposed technique in the cascode stage and the comparison between the conventional CS-LNA and the proposed CS-LNA is focused in the cascode stage. For this purpose, the conventional CS-LNA and the proposed CS-LNA share the same input stage. The performance of the input stage does not hurt the validation of the proposed technique.

First, input stage is designed following the design procedure of the typical inductively degenerated CS-LNA in Fig. 3.16. From the noise figure versus Q relation, get the Q of the input network. Q is chosen 4.8 to obtain the noise figure less than 2dB.

Second, from the Q of the input network, obtain the C_{gs1}, L_s and L_g.

$$C_{gs1} = \frac{1}{2\pi R_s \omega_o Q} = 300\text{fF} \tag{4.50}$$

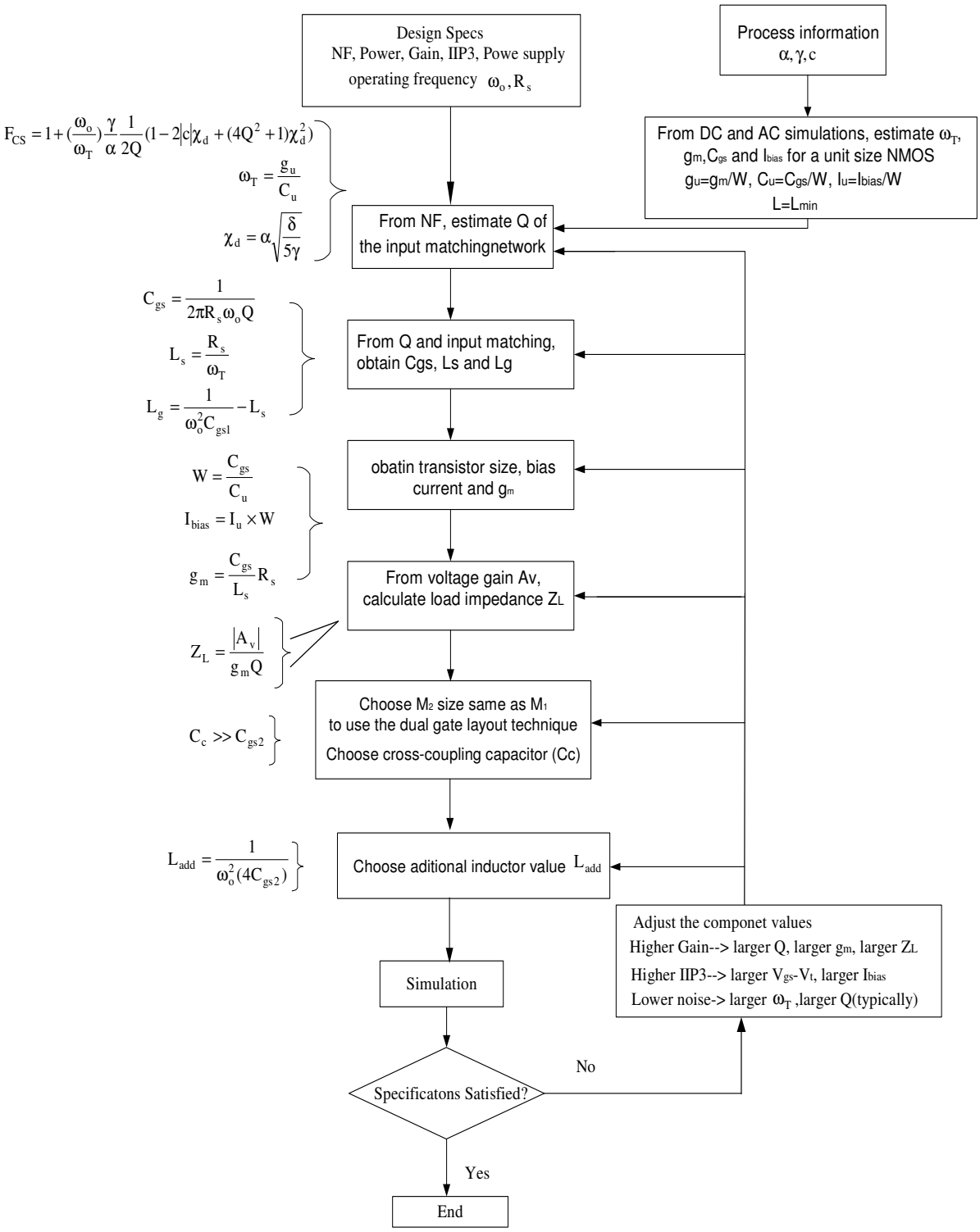


Fig. 4.17 Design procedure for the noise reduction and linearity improvement CS-LNA

$$L_s = \frac{R_s}{\omega_t} = 0.5\text{nH} \tag{4.51}$$

$$L_g = \frac{1}{\omega_o^2 C_{gs1}} - L_s = 16.5\text{nH} \tag{4.52}$$

Third, the transistor M_1 size is obtained by fixing the C_{gs1} and g_{m1}

$$g_{m1} = \frac{C_{gs1}}{L_s} R_s = 22\text{mS} \tag{4.53}$$

According to the g_{m1} and C_{gs1}, we get the transistor M_1 size as 200µm/0.35µm with 5.35bias current. The transistor M_2 size is chosen same as M_1 size as 200µm/0.35µm to implement the dual gate layout technique as explained in Fig. 4.4. The cross-coupling capacitor needs to be greater than 10 times C_{gs2}, which is around 0.29pF. Now C_C is chosen as 6pF. The inductor Ladd needs to resonate with $C_x = 4C_{gs2} + C_{gd1} + C_{db1} + C_{sb2} + C_x$ at the operating frequency. Though the simulation, C_x is 1.7pF.

$$L_{add} = \frac{1}{\omega_o^2 C_x} = \frac{1}{\omega_o^2 (4C_{gs2} + C_{gd1} + C_{db1} + C_{sb2} + C_x)} = 3\text{nH} \tag{4.54}$$

Following that, the load network is designed to achieve LNA gain and bandwidth requirement. The overall load capacitor is C_L=1.8pF and L_D is calculated as

$$L_d = \frac{1}{\omega_o^2 C_L} = 2.9\text{nH} \tag{4.55}$$

Finally the simulation is processed to verify the design specifications.

The inductor L_g is an off-chip inductor. The added inductor L_{add} (around 3nH) is a bonding wire inductor. The inductors L_s (0.5nH) and L_d (2.9nH) are on-chip spiral

inductors, with $Q \approx 3$. The design was implemented using TSMC 0.35 μm CMOS technology. The chip micrograph is shown in Fig. 4.18. The LNA occupies 1300μm×1000μm active area, with the LNA core using 850μm×850μm active area. L_g value is adjusted in the measurement to achieve the input impedance matching at the desired frequency.

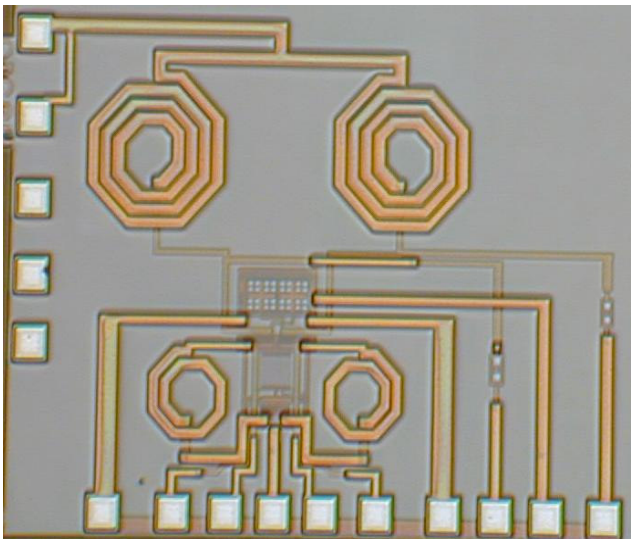


Fig. 4.18 Chip micrograph of the differential cascode CS-LNA

4.5.2 Testing Setup

The testing board photo is shown in Fig. 4.19. The PCB is fabricated using FR4 material. The LNA input SMA connector is put close to the chip. The input and the output are connected to the chip through the off-chip balun.

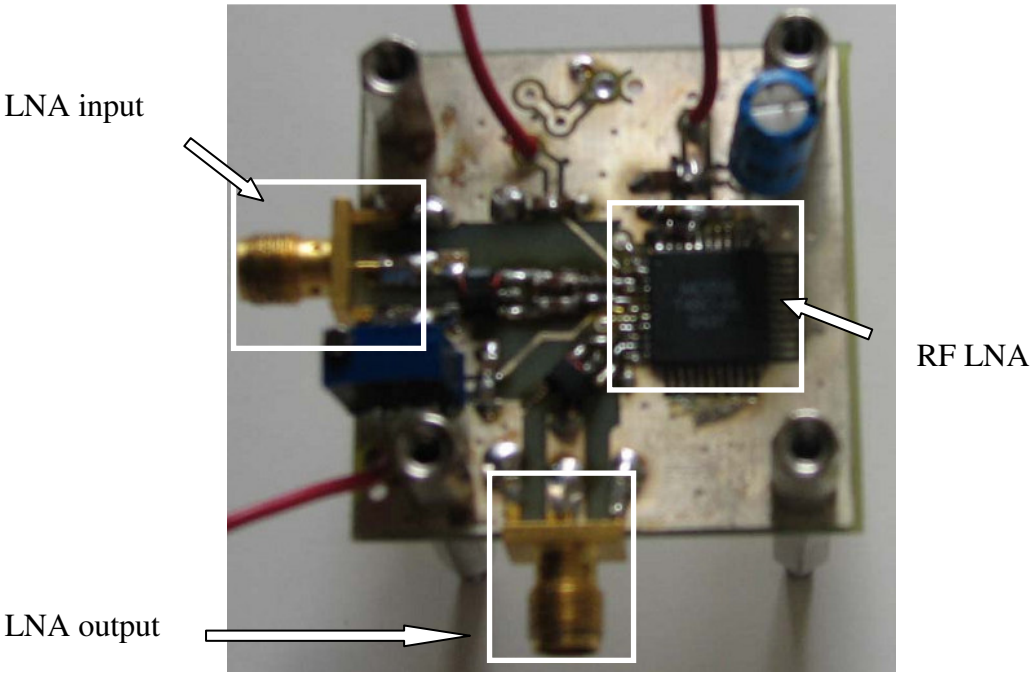


Fig. 4.19 RF LNA testing board

The testing of the S-parameter of the LNA is using HP8719ES S-parameter network analyzer (50MHz~13.5GHz). The testing setup is shown in Fig. 4.20

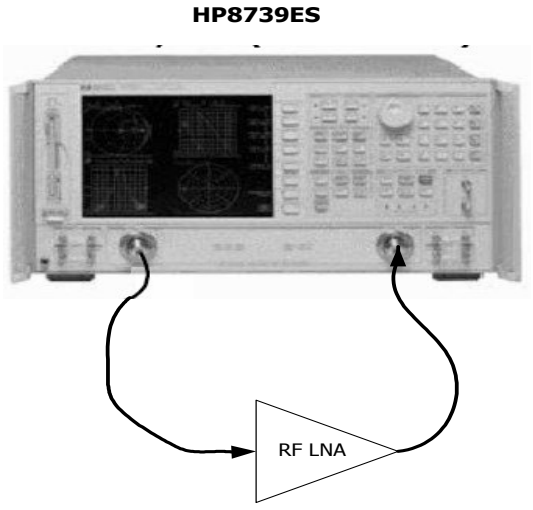


Fig. 4.20 RF LNA S-parameter testing setup

The testing of the LNA NF is using the spectrum analyzer FSEB30 from Rohde & Schwarz and NC346B noise source. The testing setup is shown in Fig. 4.21

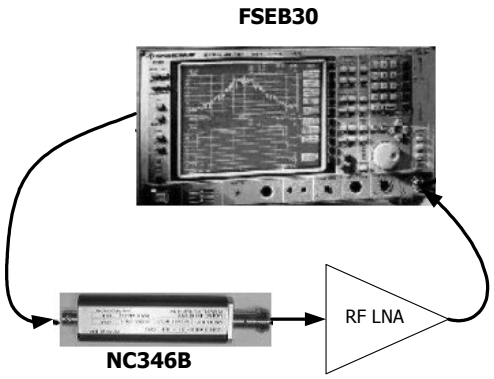


Fig. 4.21 RF LNA NF testing setup

The testing of the LNA IIP3 is using two signal generators SMIQ03 and the spectrum analyzer FSEB30 from Rohde & Schwarz. The testing setup is shown in Fig. 4.22

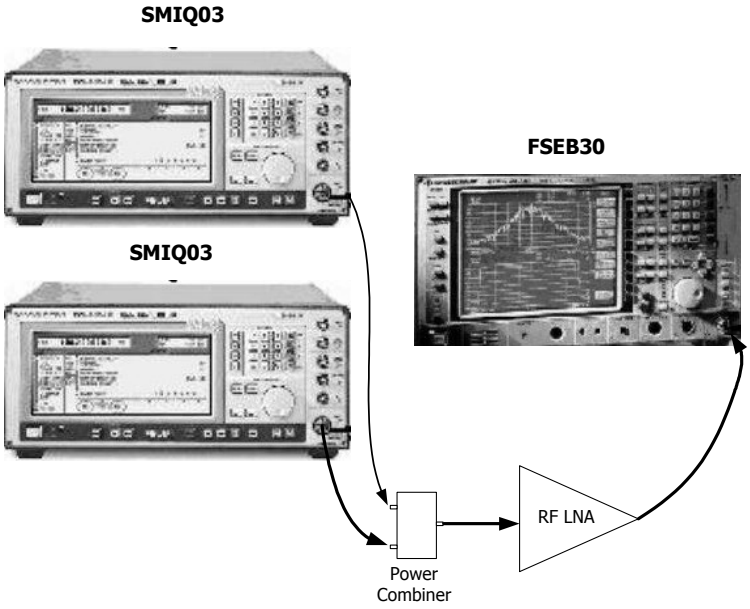


Fig. 4.22 RF LNA IIP3 testing setup

4.5.3 Experiment Results

Fig. 4.23 shows the measured S11, S21 and S12. The LNA power gain is 8.4dB at 2.2GHz. If followed by a buffer, the LNA output impedance is larger than 50Ω and the LNA gain increases up to 20.4dB in simulation. S11 is less than -13 dB. And S12 is less than -30dB. Fig. 4.24 shows the measured NF of the LNA. The LNA has 1.92dB NF. The third-order input intercept point (IIP3) was measured using a two-tone test: 2.2GHz and 2.22GHz. It is shown in Fig. 4.25. The IIP3 is -2.55dBm. The core LNA draws 9mA from a 1.8V power supply.

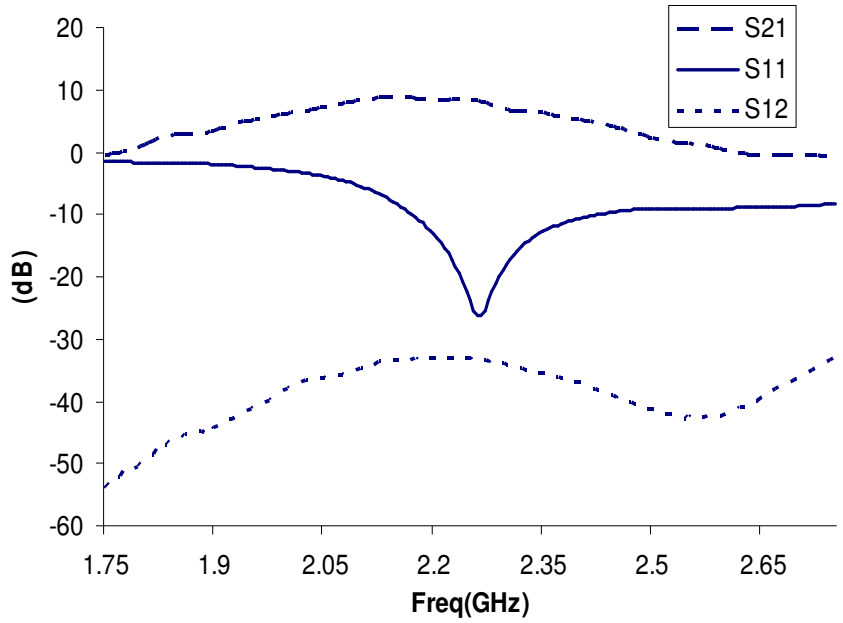


Fig. 4.23 Measured S11, S12 and S21 of the differential cascode CS-LNA

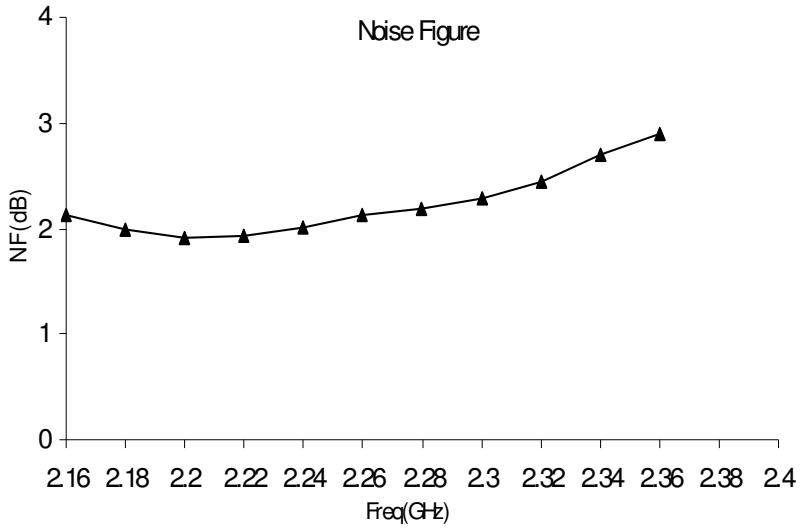


Fig. 4.24 Measured NF of the differential cascode CS-LNA

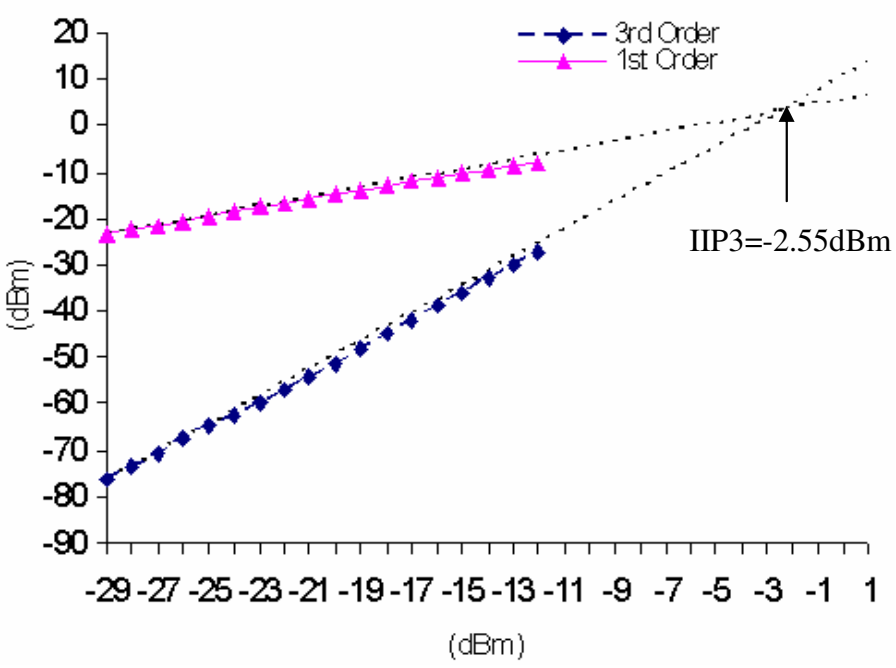


Fig. 4.25 Measured IIP3 of CS-LNA, with two tones at 2.2GHz and 2.22GHz

The comparison of this LNA with the published literatures is summarized in Table 4.4. The figure of merit (FOM) includes the power, linearity and noise. It is defined as below

$$\mathrm{FOM} = \frac{\mathrm{IIP_3[mW]]}}{\mathrm{P_{dc}[mW]} \times (\mathrm{F}-1)} \tag{4.56}$$

Table 4.4 Performances compared with the prior published cascode CS-LNAs

Parameters	[69]	[70]	[71]	[72]**	This work	
					Simulated	Measured
Frequency (GHz)	2.45	2.46	2.4GHz	2.4GHz	2.2	2.2
S11(dB)	<-14.2	<-18.4	-10.1	-19	<-13	<-13
S21(dB)	15.1*	14	10.1	20	10 (20.4)+	8.6
NF(dB)	2.88	2.36	2.9	2.4	1.87	1.92
IIP3(dBm)	2.2	-2.2	4	-3.4	-2.05	-2.55
Power (mW)	24.3	4.65	11.7	7.26	16.2	16.2
Vdd (V)	3	1.5	1.8	3.3	1.8	1.8
FOM×10^3	73	180	226	85	72	62
Topology	Single ended	Single ended	Single ended	Differential	Fully-differential	Fully-differential
Process	0.25µm CMOS	0.15µm CMOS	0.25µm CMOS	0.25µm CMOS	0.35µm CMOS	0.35µm CMOS

*: In fact in [69] they reported the transducer gain.

+: 20.4 dB is obtained when an output buffer is used instead of 50Ω load.

** Simulation results are given in [72]

Although the designed LNA is a fully-differential structure in 0.35μm process, it provides better noise performance. The published LNAs consume less bias current because of the single-ended structure and more advanced technology. The differential LNA in [72] consumes much smaller power consumption with 3.3V. It has no special technique to reduce the power consumption. There is no clue why it can have that less bias current. The gain is not included in the figure of merit since the proposed LNA has much larger voltage gain up to 20dB if followed by a buffer. Most important thing is that for the same input stage CS-LNA, with the proposed technique, the LNA performance significantly improves as shown in Table 4.2, which verifies the proposed concept. The linearity in [69] is higher due to the higher bias current and more voltage headroom for the transistors. Although the current source of the designed fully-differential LNA reduces the voltage headroom, it still achieves comparable linearity with respect to [70]. The LNA gain is proportional to the inductor quality factor and the inductor value as shown below [70]

$$\text{Gain} \propto R_p \propto Q_d^2 R_d \propto \omega_o Q_d L_d \tag{4.57}$$

where R_d is the series resistance of L_d, R_p is the parallel resistance of L_d obtained from the series to parallel transformation, and Q_d is the quality factor of L_d. The LNA is designed in 0.35μm process with a low Q on-chip inductor, which results in a smaller gain. After adding a buffer (with similar input impedance of a typical CMOS Gilbert Cell) after the LNA, the LNA can achieve around 20.4dB voltage gain, which is sufficient for wireless application.

4.6 Summary of the Proposed Noise Reduction LNA

In this chapter, a noise reduction and linearity improvement technique for a differential cascode CS-LNA was proposed. The inductor connected at the gate of the cascode transistor and the capacitive cross-coupling are strategically combined to reduce the noise and nonlinearity contributions of the cascode transistors. It is the first time that the capacitive cross-coupling technique is applied to the cascode transistors of the CS-LNA. It increases the effective transconductance of the cascode transistor, reduces the impedance seen out of the drain of the main transistor, and thus improves the linearity of the CS stage in the LNA. The inductor L_{add} resonates with the effective capacitance at the drain of the main transistor with smaller value compared with the typical inductor based technique. It ideally removes the noise and linearity influences from the cascode transistor. Finally it results in lower LNA NF, better LNA linearity and higher LNA voltage gain. The proposed technique is theoretically formulated. From simulation, it reduces the LNA NF by 0.35dB, and improves the LNA IIP3 by 2.35dBm. A 2.2GHz LNA was fabricated using TSMC 0.35μm CMOS process. Experiment results show 1.92dB NF, -2.55dBm IIP3, and 8.4dB power gain, with the core LNA consuming 9mA current from a 1.8V power supply.

CHAPTER V

PROPOSED WIDEBAND COMMON GATE LNA*

5.1 Background

In February, 2002, Federal Communications Commission (FCC) allocated the frequency (3.1GHz-10.6GHz) to unlicensed use. The research and commercial activities in UWB system and circuit design increased rapidly. The frequency spectrum allocation of the UWB system is drawn in Fig. 5.1

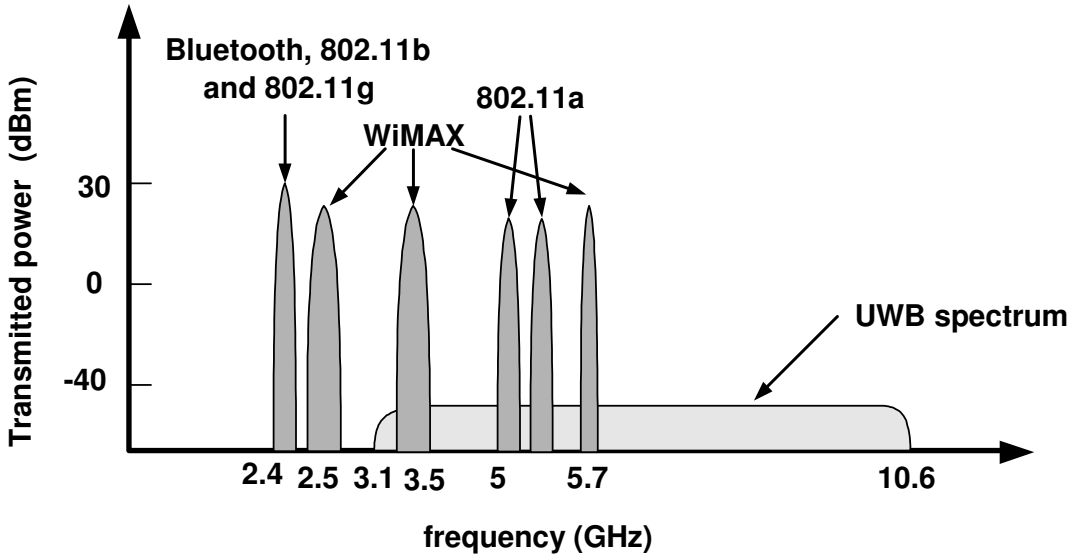


Fig. 5.1 Frequency spectrum of the UWB system

*©[2007] IEEE. Reprinted, with permission, from "A 3GHz-10GHz Common Gate Ultrawideband Low Noise Amplifier", by Xiaohua Fan, Edgar Sánchez-Sinencio, and Jose Silva-Martinez, *IEEE International MIDWEST Symposium on Circuits and Systems*, pp.631-634, August 2005

Table 5.1 Summary of characteristics of different wireless communication standard

Characteristic	Bluetooth	IEEE802.11b	IEEE 802.11g	IEEE802.11a	UWB
Maximum distance	10-100m	100m	100m	50m	10m
Frequency allocation	2.4GHz (ISM)	2.4GHz (ISM)	2.4GHz (ISM)	5GHz (UNII)	3.1-10.6GHz
Number of RF channels	79	3	3	12(US)	1-15
Modulation	GFSK	QPSK(CCK)	OFDM	OFDM	BPSK,QPSK
Maximum RF power	0~20dBm	30dBm(US)	30dBm(US)	17dBm(US)	-41.3dBm/MHz
Receiver sensitivity	-70dBm	-76dBm for 11Mb/s	-74dBm for 33Mb/s	-64dBm for 54Mb/s	-70.4dBm for 480Mb/s

The different standards are summarized in Table 5.1 [73].

Two major proposals are now the candidates for the IEEE 802.15.3 standard [39]: Direct Sequence (DS)-UWB approach [40] and Multi-Band OFDM UWB approach [41]. The DS-UWB approach is a single band approach that uses narrow UWB pulses and time-domain signal processing. The Multi-Band OFDM UWB approach divided the 7400MHz frequency band into multiple smaller bands with bandwidths greater than or equal to 500MHz. The Multi-Band OFDM UWB approach is similar to the narrowband frequency-hopping technique. The Multi-Band UWB can avoid some wireless application bands, such as 802.11a at 5GHz. The DS-UWB approach has simpler system architecture than the Multi-Band OFDM approach. The Wideband LNA servers as an important building block for

the UWB receiver. It needs to provide constant gain for the input signal through the entire bandwidth, which is 3GHz~10GHz fro UWB receiver. The requirement of UWB LNA for the DS-UWB approach and the Multi-Band OFDM UWB system are similar. The UWB LNA needs to have flat and large gain, good impedance matching, lower Noise Figure, good linearity, and lower power consumption are desired.

Different typologies have been proposed to design the UWB LNA. (a) Distributed amplifier (DA) [43]-[45]: Distributed amplifier absorbs the parasitic capacitance of the input transistor as part of the transmission line, which leads to a broadband operating performance. DA needs several amplifier unit connected by the transmission line to form multiple signal paths from the input to the output. Due to the large area and much more power consumption, it is unsuitable for the UWB LNA design. (b) Feedback configuration: LNA with the feedback configuration can achieve the Wideband performance. Because of the existence of parasitic capacitance in the transistor, the LNA with feedback configuration doesn't perform well in the high frequency [49]. (c). Filter configuration: The source inductance degeneration is widely used in the narrow band LNA design. The extension of this narrow band LNA to UWB LNA is achieved using filter theory concepts with the filter configuration [50]-[51]. The common source (CS) and common gate (CG) typologies are two popular architecture choices for the narrow band LNA design. The common source typology with the source inductor degeneration achieves the input impedance matching with the noiseless components, which leads to a smaller Noise Figure. The common gate typology has inherent Wideband operating performance, and good linearity and input-output isolation property [34]. The parasitic capacitance of the transistor degrades the CGLNA performance in the higher

frequency. The CG-LNA with the filter typology can solve this problem and achieve the broadband operating property, which also holds the same beauties of the original CG LNA architecture at the same time. In this research, a common gate (CG) UWB LNA is first proposed, discussed. Previous UWB LNA normally is common source design. The CG-LNA has inherent wideband input matching property, better linearity, better input and output isolation, less process variation than the CS-LNA design. The proposed UWB CG-LNA has overall better performance during that time.

A direct-conversion UWB receiver architecture is shown in Fig. 5.2 [74]-[75]

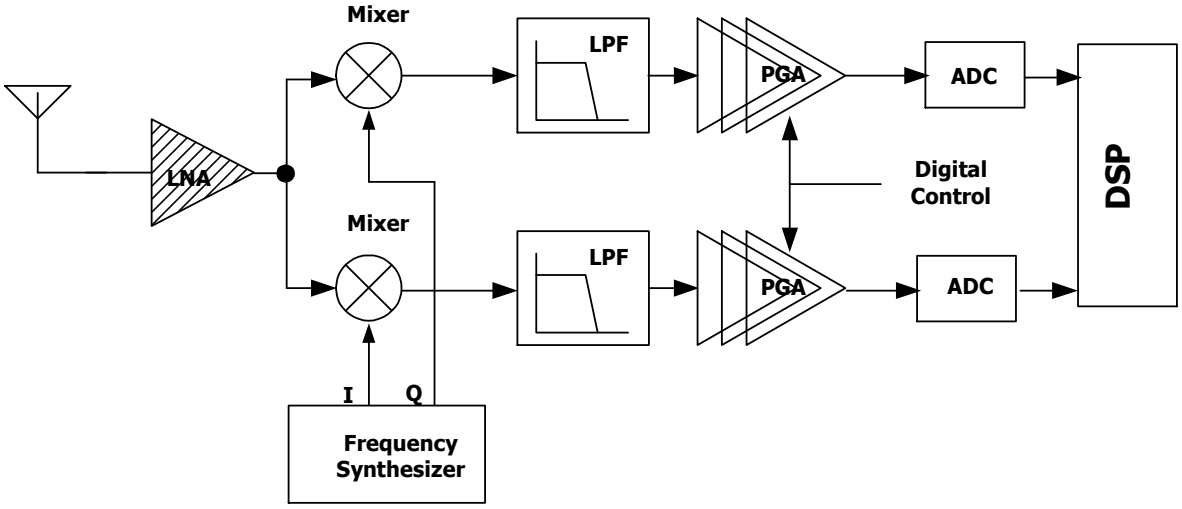


Fig.5.2 A direct-conversion UWB receiver topology

The specifications of the building blocks of the receiver is summarized in Table 5.2 [74]-[76]

Table 5.2 Specifications of the UWB receiver building blocks

Parameter	LNA	Mixer	VGA1	Filter	VGA2
NF(dB)	3	15	12	36	25
Max. Gain(dB)	15	15	6	0	42
Min. Gain(dB)	15	15	0	0	0
IIP3(dBm)	-10	5	20	18	12
Power consumption(mW)	12.5	5	10	37.5	20

*The frequency synthesizer consumes 200mW power.

The UWB receiver in [74]–[75] is designed using SiGe 0.25μm CMOS technology. For the CMOS LNA, the typical specifications are listed below.

Table 5.3 Specifications of the typical UWB LNA

Parameter	LNA
Frequency(GHz)	3.1~10.6
NF (dB).	<4.5
IIP3(dBm)	>-5dBm
S11(dB)	<-10
S21(dB)	>10
S12(dB)	>-30
Power(mW)	<10

One important property of the UWB LNA is the wideband impedance matching. The UWB LNA input needs to be matched to 50Ω from 3GHz to 10GHz.

The other UWB LNA topologies can be found in section 3.2.2. In this research, the UWB CG-LNA is first proposed. Different from the typical approach that uses the CS-LNA, the CG-LNA is proposed to design the UWB LNA. The proposed UWB CG-LNA has better linearity, lower power and overall better performance than the other topologies.

In the following sections, first the typical common gate LNA is described. Second, the bandpass filter design is presented to implement the input impedance matching of the LNA. Following that, the proposed UWB CG-LNA is explained and in the end, the simulation results and the comparison are given to prove the superiority of the proposed architecture.

5.2 Proposed Filter Based Common Gate UWB LNA

5.2.1 Common Gate LNA(CG-LNA)

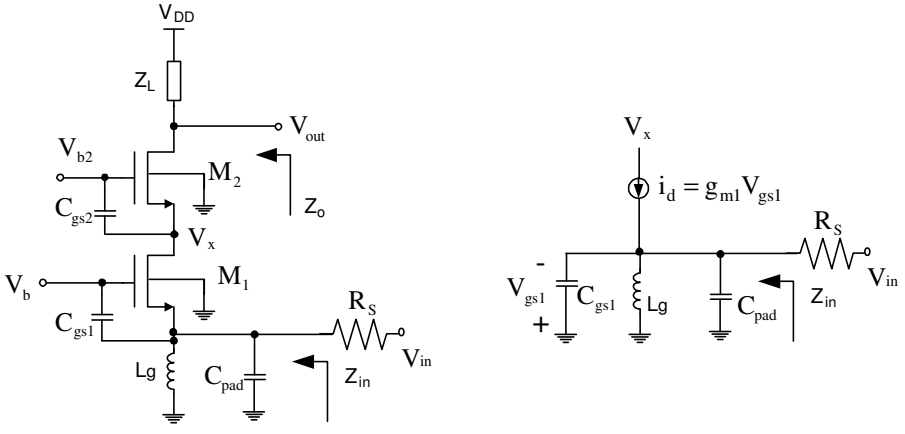


Fig. 5.3 (a) A common gate LNA (CG-LNA) (b) Its equivalent input network

The typical common gate LNA (CG-LNA) is shown in Fig.5.3.

There are two important factors to design the wideband LNA: wideband impedance matching and flat voltage gain. The UWB LNA needs to have a wideband input matching network, which can match to the source impedance of the previous block, which is typically 50Ω, over the whole interested bandwidth.

The typical common gate transistor can provide real impedance parallel with a parasitic capacitance. The real impedance is matched to 50Ω, and the parasitic capacitance is absorbed to the bandpass filter network. Following this approach, the CG-LNA is designed to a wideband LNA.

Without the shunt inductor L_g and pad capacitor C_{pad}, the input impedance of the common gate transistor M_1 is calculated as below:

$$Z_{inM1}(j\omega) = \frac{1}{g_m + j\omega C_{gs}} \tag{5.1}$$

In the low frequency, the input impedance of M_1 is approximately as $Z_{in}(j\omega) = \frac{1}{g_m}$. It has to be matched to the 50Ω. With the increasing of the operating frequency, the parasitic transistor capacitance C_{gs} starts playing a key role, which degrades the amplifier performance in the high frequency. In the narrow band application, a shunt inductor L_g is added in the input to resonate with C_{gs} to have a good impedance matching in the designed frequency.

With the shunt inductor Lg, the input impedance of the CG-LNA becomes

$$Z_{in}(j\omega) = \frac{1}{g_m + j\omega C_{gs} + \frac{1}{j\omega L_g}} \tag{5.2}$$

The difference from the CS matching network lies that it is a parallel resonant network. Due to the lower quality factor of the resonant network, it is more robust against the process, electrical variation [32]. Due to the missing of the C_{gd} path from the input to the output, the CG LNA shows better reverse isolation and stability versus CS-LNA. As discussed in [32], the noise factor of CG LNA is constant with respect to ω_o / ω_T, and the noise factor of CS LNA is linear with ω_o / ω_T. The CG LNA outperforms CS LNA in the higher frequency.

To make the CG LNA working for the UWB receiver, CG LNA needs to achieve the broadband impedance matching. The parasitic C_{gs} of the input transistor has to be taken care of. The distributed circuit configuration is one way to absorb it. Since distributed circuits occupy large area, and consume more power, they are unsuitable for UWB LNA design. The filter theory can be used to absorb the parasitic capacitor C_{gs}, make the CG-LNA working in the broadband range, and holds the beauties of the original CG amplifier. Different from [47]-[48], the 3rd Butterworth filter is chosen in this typology.

5.2.2 Proposed UWB Common Gate LNA (CG-LNA)

A UWB LNA, using a common gate topology, is first proposed in this research. It inherits the advantage of the CG-LNA: low power consumption, high linearity, good input-output

isolation and stable matching condition. The proposed Common Gate (CG) UWB LNA is shown in Fig. 5.4.

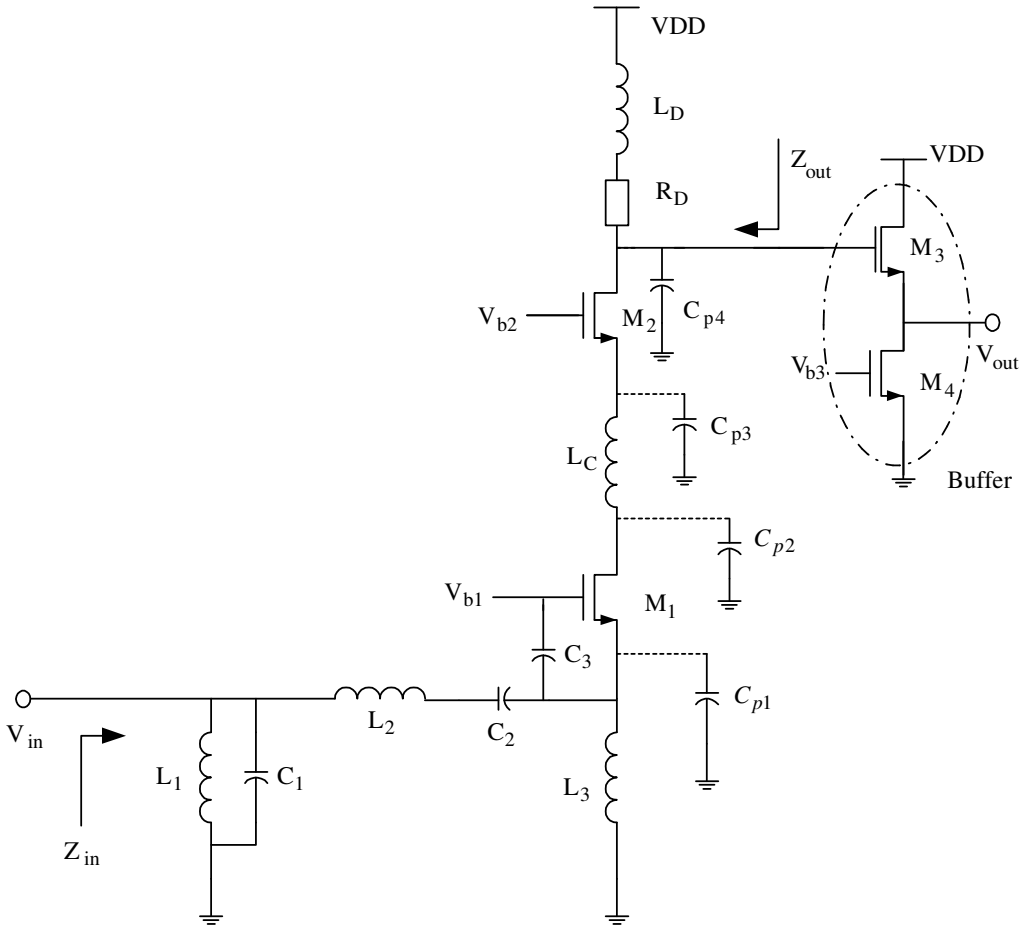


Fig. 5.4 The proposed UWB common gate LNA

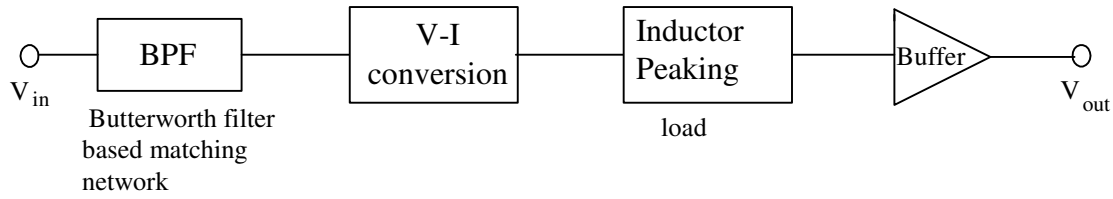


Fig. 5.5 The conceptual topology of the proposed UWB common gate LNA

The input parasitic capacitor C_{gs1} is absorbed as the part of the band pass filter (C_3). The input real impedance of the common gate transistor is designed to implement the resistance ($R_{in} = 50\Omega$). The conceptual topology is shown in Fig. 5.5. The 6^{th} order bandpass Butterworth filter is used to implement the broadband matching. The transistor M_1 converts the incoming voltage signal to the current signal. The inductor peaking load helps to achieve a flat LNA voltage gain over the operating frequency band.

The 6^{th} order Butterworth filter configuration guarantees the input stage as a broadband input impedance matching network. The inductor L_1, C_1, L_2, C_2, L_3, C_3 and input impedance of transistor M_1 form a 6^{th} Butterworth filter configuration. The capacitor C_3 is added to make the choosing of the transistor size of M_1 more flexible. The bandpass filter is explained in the next part.

5.2.3 6^{th} order Bandpass Butterworth Filter

The filter theory is used to implement the broadband matching for the UWB LNA [50]-[51]. Several filter types can be used to achieve the broadband performance. Since the input stage of the CGLNA is the parallel connection, the 6^{th} order Butterworth band pass filter is easier to be used to implement the broadband impedance matching in this design. The filter circuit is shown in Fig 5.6.

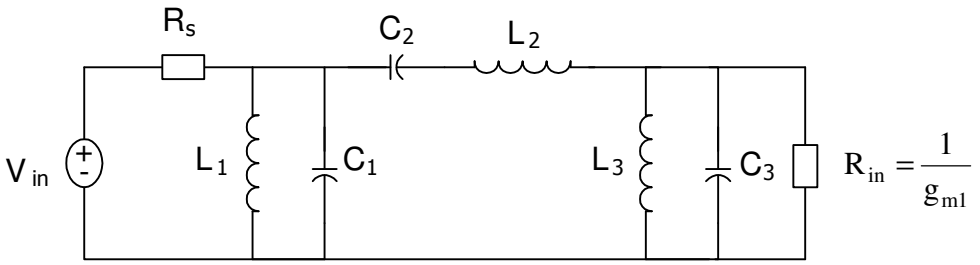


Fig. 5.6 6th order bandpass Butterworth filter

The choice of reactive components in the filter is decided by the corner frequency. The filter type is chosen as 6th order bandpass Butterworth filter. The component value of the 6th bandpass filter is obtained using Filter Free design software [76]. Using the Filter Free software, first, the filter is chosen as 6th order bandpass Butterworth filter. Second, the corner frequency is chosen as 2GHz-13GHz to cover the UWB frequency range (3.1GHz-10.6GHz). After that, the voltage source is chosen with 50Ω as the resistance. Finally, the filter is synthesized using the Filter Free software [76]. According to the bandwidth requirement and also the available reasonable component value, the Filter Free software [76] gives the components values as shown in Table 5.4.

Table 5.4 Components values for a 6th order bandpass Butterworth filter

Components	L1	C1	L2	C2	L3	C3	Rin
Values	3.367nH	289.4fF	1.447nH	673.3fF	3.367nH	289.4fF	50Ω

The transfer function of the 6th order bandpass Butterworth filter using the components value shown in Table 5.4 is (5.3), where H(s) is the insertion loss.

$$H(s) = \frac{3.3\times10^{32}s^3}{s^6 + 1.382\times10^{11}s^5 + 1.263\times10^{22}s^4 + 6.139\times10^{32}s^3 + 1.297\times10^{43}s^2 + 1.456\times10^{53}s + 1.08\times10^{63}} \quad (5.3)$$

The root locus of the filter is shown in Fig 5.7.

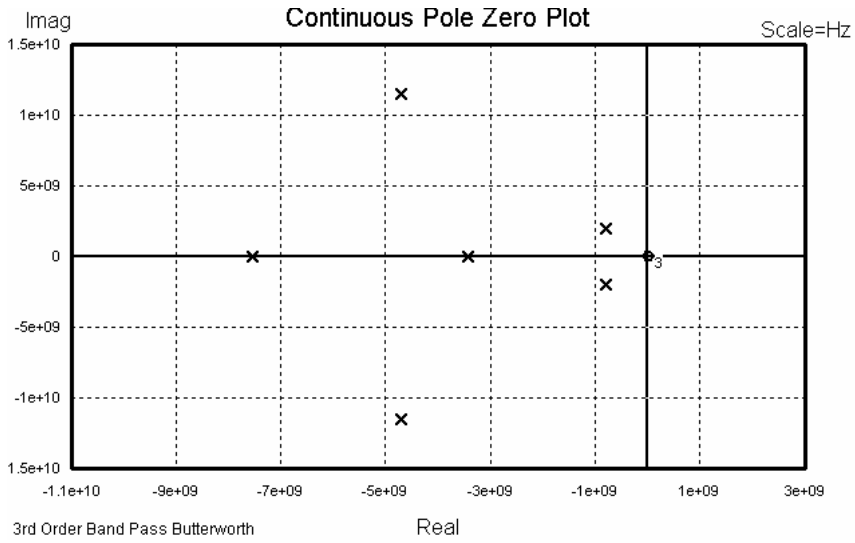


Figure 5.7 Root locus of the 6th order bandpass Butterworth filter

The poles of a Butterworth lowpass filter are located on a circle with radius ω_c and are spaced apart by an angle $180^o/n$ in which n is the order of the filter (number of poles). After the lowpass filter to bandpass filter transformation, the poles are not around the circle as shown in Fig. 5.7.

The insertion loss is the attenuation of the pass band caused by the insertion of the filter. It equals to the difference in dB power measured at the filter input and at the filter output. The lower the value for Insertion Loss, the better the filter is. The insertion loss (gain) of the filter

is shown in Fig. 5.8. The filter itself shows the flat magnitude response within 3GHz-10GHz frequency range.

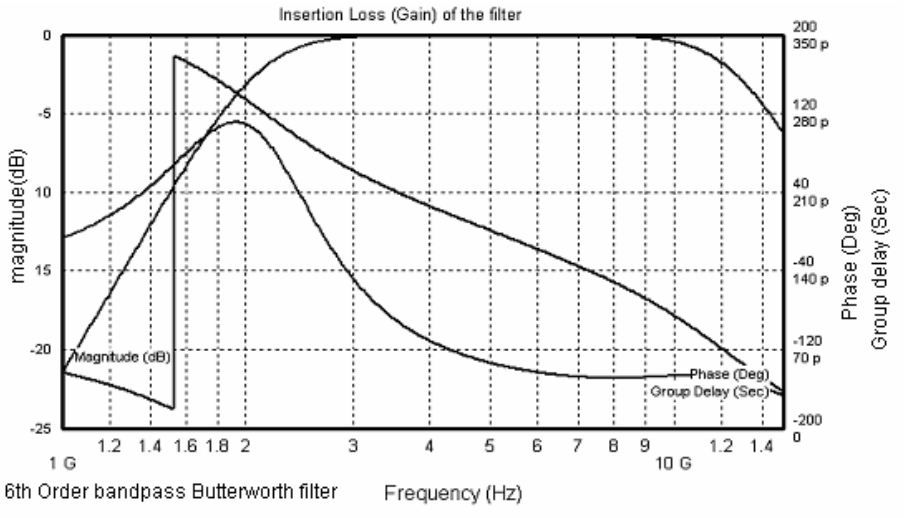


Fig. 5.8 Insertion loss frequency response of the filter

A filter's reflection coefficient is defined as the ratio of the reflected wave to incident wave at point of reflection. A filter's return loss is the dB value of the absolute reflection coefficient, which refers to the attenuation of reflected signals within the pass band. Here, the filter source resistance and the load resistance are set as 50Ω. The filter's return loss is the S11 of the LNA in the first order. The higher the return loss, the better the filter's impedance match and the lower the reflected signals that occur when signals pass from the line through the filter. A filter system is shown in Fig. 5.9

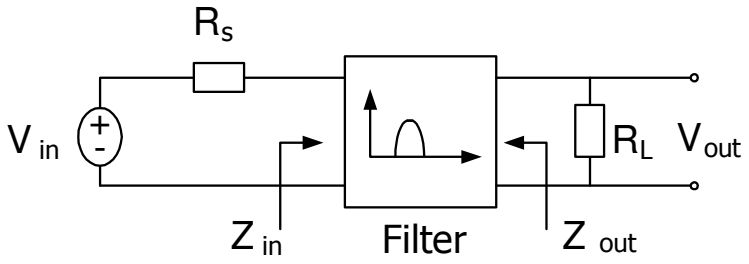


Fig. 5.9 Two port filter network

Where V_{in} is the input voltage signal and R_s is the impedance of the voltage source $V_{in.}$

The return coefficient Γ is defined as

$$\Gamma = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \tag{5.4}$$

The return loss RL is defined as

$$RL = 20\log(\Gamma) = 20\log(\frac{Z_{in} - Z_s}{Z_{in} + Z_s}) \tag{5.5}$$

The return loss of the filter is shown in Fig.5.10. It is less than –10 dB within 3GHz-10GHz frequency range.

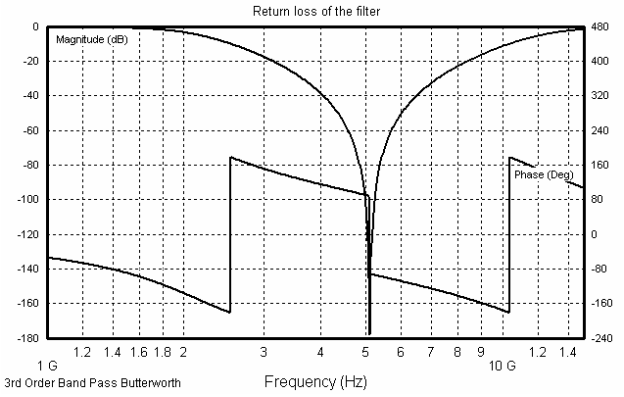


Fig. 5.10 Return loss of the filter

5.3 Circuit Analysis and Design

5.3.1 Design Procedure

The design procedure is similar as the one for the filter based UWB CS-LNA in Fig. 3.29. It is shown in Fig. 5.11.

The input component values are got from the filter design simulation software [76]: Filter Free. Using the Filter Free software, first, the filter is chosen as 6^{th} order bandpass Butterworth filter. Second, the corner frequency is chosen as 2GHz-13GHz to cover the UWB frequency range (3.1GHz-10.6GHz). After that, the voltage source is chosen with 50Ω as the resistance. Finally, the filter is synthesized using the Filter Free software [76]. According to the bandwidth requirement and also the available reasonable component value, the Filter Free software [76] gives the components values as shown in Table 5.4. L1=3.367nH, C1=289.4fF, L2=1.447nH, C2=673.3fF, L3=3.367nH and C3=289.4fF.

The input impedance is the parallel of the LC Butterworth filter and real impedance g_{m1}. According to Fig. 5.4, filter has unit gain transfer function in band, and smaller gain out of band.

The input transistor M_1 needs to provide 289.3fF parasitic capacitance. To give more freedom to choose the M_1 size, a real capacitor is added parallel with the C_{gs1} of M_1.The input impedance for the LNA is approximated as $\frac{1}{g_{m1}}$ in band, which has to equal to 50Ω to achieve the impedance matching.

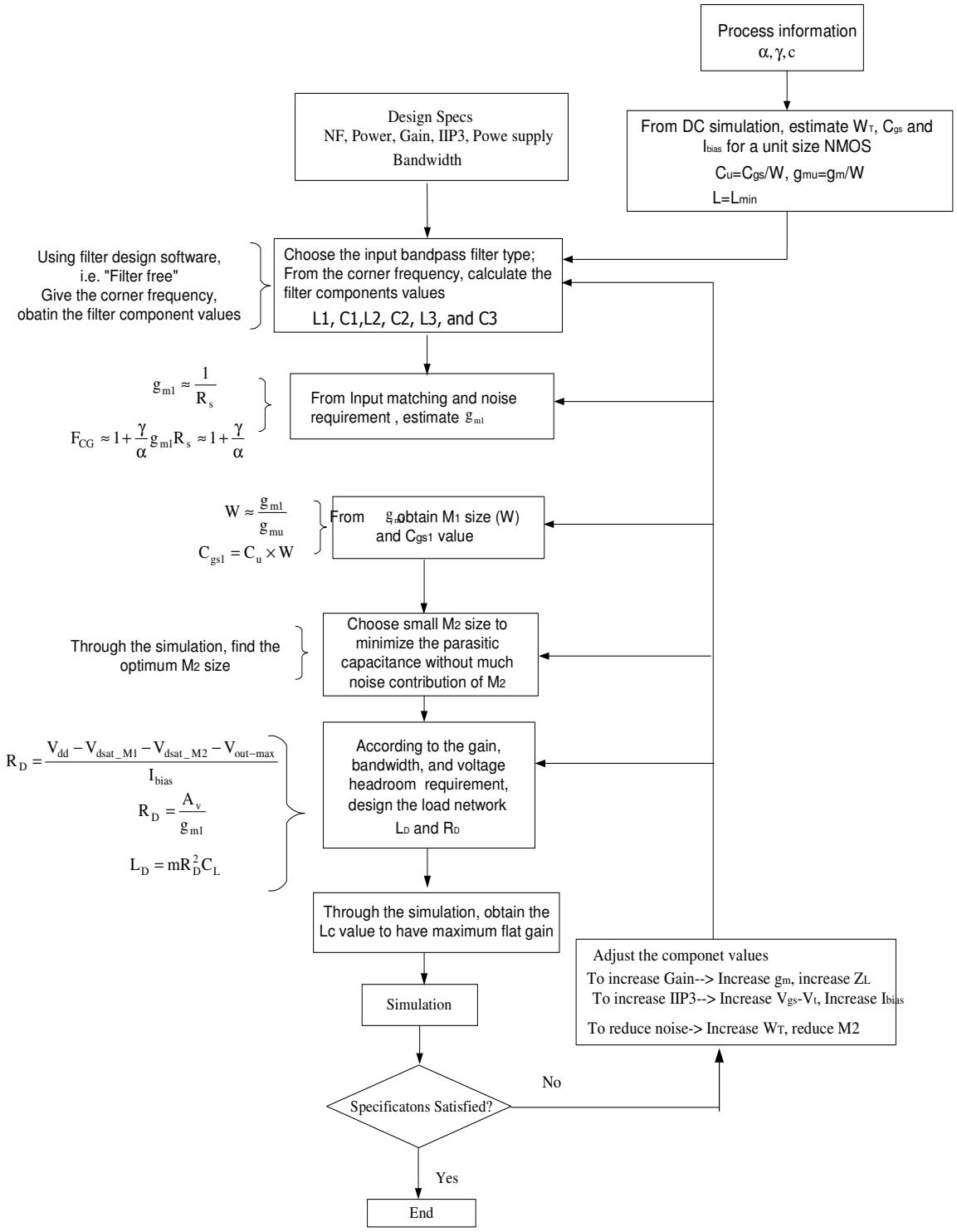


Fig. 5.11 Design procedure for the filter based UWB CG-LNA

The transconductance of the transistor M_1 is

$$g_{m1} = \frac{1}{R_s} = \frac{1}{50} = 0.02\,S \tag{5.6}$$

g_{m1} of M_1 can be estimated by

$$g_{m1} = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t) \tag{5.7}$$

For 0.18μm CMOS process, $\mu_n C_{ox}$ is around $352\mu A/V^2$, and V_t is around 0.49V. According to (5.7), there are different combination of V_{gs} and W/L of M_1 that can generate 20mS transconductance. According to Fig. 3.30 and Fig. 3.31, bias voltage 0.6V is chosen for better linearity. The transistor size W/L of M1 is obtained through the simulation to obtain 20mS transconductance. In this design, the size of the M_1 is 160μm/0.18μm, and it has 231fF parasitic capacitor. To satisfy the requirement of the filter C3=289.4fF, an additional real capacitor is added with 58fF value.

Transistor M_2 mainly serves as the isolation between the input and output. The smaller the size of transistor M_2 is, the smaller parasitic capacitance is. Transistor M_2 also influences the overall LNA noise performance as explained in Chapter IV. The parasitic gate source capacitor C_{gs2} of M_2 combined with the gate drain capacitor C_{gd1} of M_1 contributes a pole in the signal path and damage the flat gain requirement of the UWB LNA. A series inductor Lc will be added to compensation this roll-off effect. To obtain a flat gain ladder filter from Lc C_{gs2} and C_{gd1}, the size of transistor M_2 is chosen as half of the transistor M_1's. M_2 size is 80μm/0.18μm.

Another important factor for UWB LNA design is the flat gain over the full bandwidth. The transistor M_1 serves as a V-I conversion. The current is translated back to voltage at the load.

In Fig.5.4, the current converted from the input by the transistor M_1 should completely transfer to output. The parasitic capacitors of M_1 and M_2 provide additional paths for the signal current. The parasitic capacitance C_{gd} of the transistor M_1 and the parasitic capacitance C_{gs} of the transistor M_2 degrade the broadband performance of the LNA. A passive inductor L_c is added between the transistor M_1 and M_2 to absorb the influences of the parasitic capacitances [77]. C_{gd} of M_1 and C_{gs} of M_2 form a broadband π section LC network. Proper choice of inductor L_c can resonate with the parasitic capacitor and show a broadband operating property. In general, it is computationally difficult to calculate the component values for the optimizing the LC network directly. Here, the experiment approach is used to decide the inductor Lc. Through the simulation, it is found that when the inserted inductor L_C=1.82nH, the LNA has flat gain over the frequency band. It is chosen in this design as 1.82nH.

5.3.2 Inductor Peaking Technique

The capacitive load impedance of the amplifier reduces with the increasing of the operating frequency. To compensate the influence of the capacitance load, the inductance peaking configuration is used as the load of the LNA [78]-[79]. The inductor peaking

impedance increases with the increasing of the operating frequency. The inductor (L_D) peaking technique for a simple transistor M_2 is shown in Fig. 5.12 and Fig.5.13 [78]-[79].

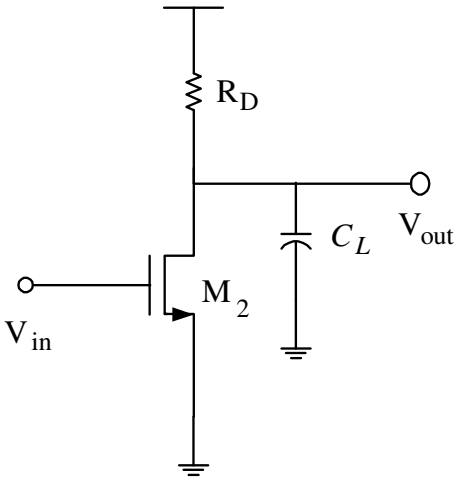


Fig. 5.12 Simple common source amplifier with resistor as the load

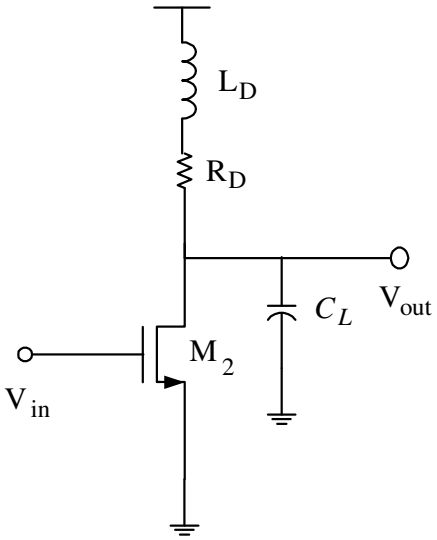


Fig. 5.13 Simple common source amplifier with inductor peaking as the load

The output impedance of the amplifier in Fig. 5.12 is

$$Z_{out}(j\omega) = \frac{R_D}{1 + j\omega R_D C_L} \tag{5.8}$$

With the inductor peaking technique, the output impedance of the amplifier in Fig. 5.13 is

$$Z_{out}(j\omega) = \frac{R_D + j\omega L_D}{1 + j\omega C_L (R_D + j\omega L_D)} = \frac{R_D + j\omega L_D}{1 - \omega^2 L_D C_L + j\omega C_L R_D} \tag{5.9}$$

From (5.8), the typical common source amplifier has a pole at $1/(R_D C_L)$, which determines the bandwidth of the amplifier. The inductor peaking technique in (5.9) has one zero at R_D / L_D at two poles. An example is used to explain the function of the inductor peaking. In the first order, the CG-LNA gain (A_v) is calculated as

$$A_v = g_{mt} R_D \tag{5.10}$$

To obtain 12dB voltage gain, the load resistor is chosen as $R_D = 200\Omega$. The capacitor C_L is the overall parasitic capacitance and the load capacitor, which emulates the mixer load for the LNA in the wireless receiver. The overall capacitance C_L is assumed around 400fF. The inductor peaking L_D is defined as $L_D = mR_D^2 C_L$, where m is the scaling factor. The frequency and phase response is as following.

Table 5.5 Inductor peaking performance versus m factor

Factor(m)	ω_{3dB} Normalized	factor(m)	ω_{3dB} Normalized
0	1	0.6	1.87
0.2	1.32	0.8	1.87
0.4	1.73	1	1.84

Where $m = L_D /(R_D^2 C_L)$ and ω_{3dB} is normalized as $\frac{\omega_{3dB}}{\omega_{3dB}(m=0)}$.

From Fig. 5.14, the 3dB cut-off frequency (ω_{3dB}) of the load impedance is extended through the inductor peaking technique. The results are summarized in Table 5.5

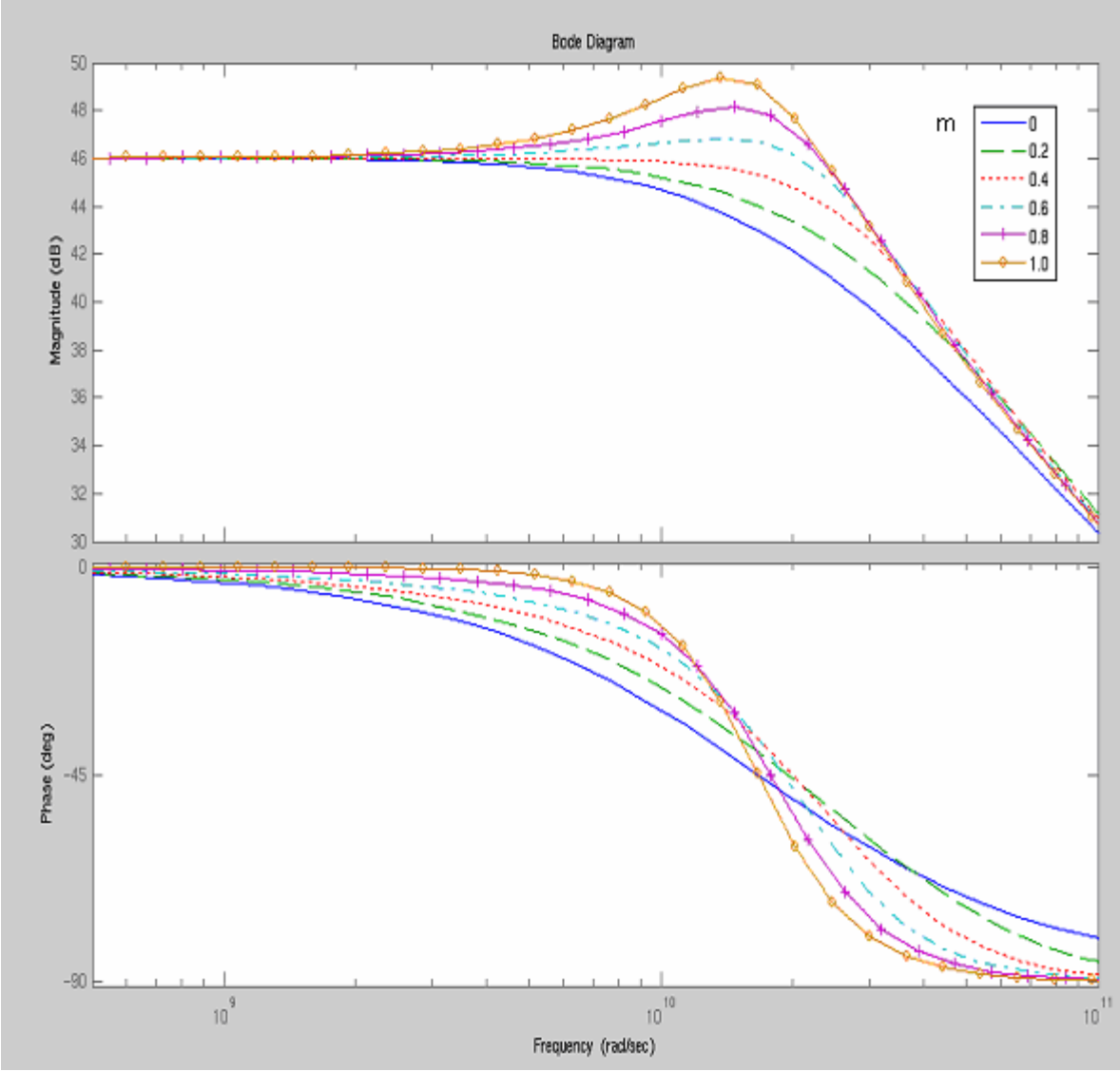


Fig. 5.14 Magnitude and phase response of the inductor peaking technique

From Table 5.5, the maximum flat appears when m is 0.4. According to Fig. 5.14, the large the m value is, the more peaking in the frequency response. The load resistor R_D is added to increase the low frequency gain. The resistor is limited by the voltage headroom. In Fig. 5.4, the transconductance g_{m1} is 0.02S to match the input impedance. The R_D is obtained from the LNA gain requirement.

$$R_D = \frac{A_v}{g_{m1}} \tag{5.11}$$

To have 14dB voltage gain, RD is chosen as 250Ω. The overall capacitance is simulated around 150fF. The peaking inductor is calculated using

$$L_D = mR_D^2 C_L \tag{5.12}$$

Using m=4, R_D=250Ω, C_L=150fF, L_D is 3.75nH. In this design, the inductor L_D is chosen as 3.82nH, to have some peaking in the load impedance to compensate the rolling-off.

The inductor peaking load and the shunt insertion inductor together can achieve the best the best flatness of the LNA gain. The inductor in the design used the inductor provided by TSMC 0.18μm, including the inductor model and layout.

A buffer is added at the output to drive the output testing equipment and also the output pad capacitance. It is composed of transistors M_3 and M_4. The output impedance is designed to be 50Ω to achieve the output impedance matching. The parasitic capacitance of the transistor M_3 serves as the load of the UWB LNA, which emulates the input impedance of the following MIXER in the UWB receiver. The buffer also emulates the equivalent load as the Mixer. The transistor size is chosen as 80μm/0.18μm for M_3 and M_4. The current for the source follower buffer is 2.78mA to have output impedance as 50Ω. The buffer is separately

characterized and removed from the final performance. Its absolute performance does not matter much since it is only used for testing and characterization.

The parameters of the LNA are summarized in Table 5.6

Table 5.6 Component values of the UWB LNA

Component	Value	Component	Value
M_1(μm/μm)	40*(4/0.18)	M_2(μm/μm)	40*(2/0.18)
M_3(μm/μm)	40×(2/0.18)	M_4(μm/μm)	40 ×(2/0.18)
L_1, L_3(nH)	3.37	L_2(nH)	1.447
C_1(fF)	289.4	C_2(fF)	673.3
C_3(fF)	50	L_C(nH)	1.82
L_D(nH)	3.8	R_D(Ω)	250

5.3.3 UWB LNA Noise Performance

If the input bandpass filter has no insertion loss, using the small signal model of the CG-LNA, the noise figure of the proposed UWB CG-LNA can be calculated as

$$F = 1 + \frac{\gamma}{\alpha} g_{m1} R_s + \frac{\delta}{5\alpha}\left(\frac{\omega}{\omega_T}\right)^2 + \frac{R_D}{\left(\omega^2 L_D^2 + R_D^2\right)} g_{m1}^2 \left(\frac{Z_{in}}{Z_{in} + R_s}\right)^2 \qquad (5.13)$$

where γ, α, and δ are conventional process dependent parameters [1]-[2], the 2nd term is the thermal noise contribution, the 3rd term is the gate induced noise contribution, the 4th term is the noise contribution of the load resistor and the noise from the other inductors are ignored

for simplification. The noise contribution from the cascode transistor is smaller compared to others and also can be reduced by the inserted inductor L_c, thus it is ignored for simplicity. The noise is mainly dominated by the thermal noise (2^{nd} term), which is frequency-independent. The noise contribution of the gate induced noise is frequency-dependent due to the noise property [1]-[2]. This mainly leads to the variation of the LNA noise factor over the frequency range. Although the resistor noise is frequency independent, the noise transfer function is frequency dependent.

5.3.4 UWB LNA Linearity Performance

The drain current of a MOS transistor can be modelled in terms of its gate-source voltage up to 3^{rd} order terms as below:

$$i_{ds} = I_{DC} + g_{m1} v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ... \tag{5.14}$$

where g_{m1}, g_2 and g_3 are the main transconductance, the 2^{nd} order, and the 3^{rd} order nonlinearity coefficients respectively.

The small signal model used to analyze the LNA linearity is shown in Fig. 5.15, where Z_{M2} is the impedance looking out of the drain of the transistor M_1.

Since the input bandpass filter gain is ideally one, using the Volterra Series theory, the linearity [63]-[65] of the input stage can be calculated as below:

$$IIP_3 = \frac{1}{6R_s \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|} \tag{5.15}$$

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - g_{oB} \tag{5.16}$$

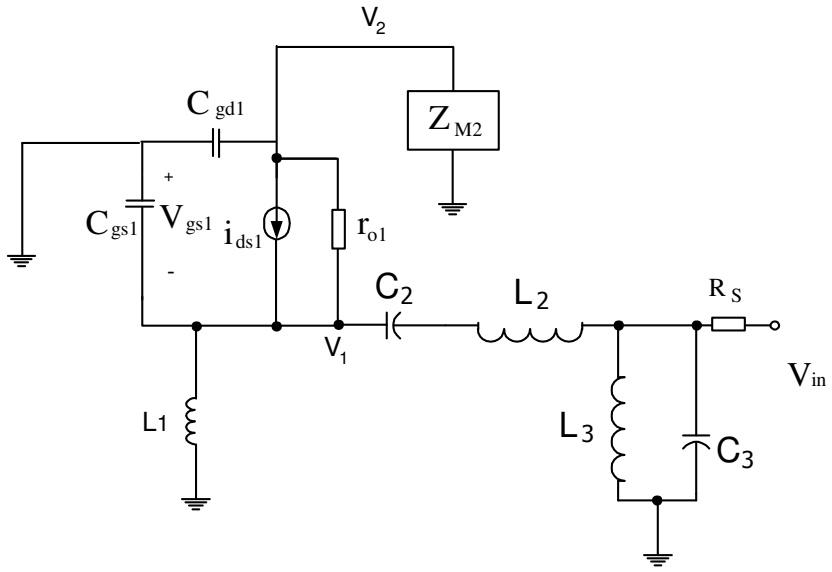


Fig. 5.15. Analyzed input stage of UWB CG-LNA equivalent circuit

$$g_{oB} = \frac{2}{3} g_2^2 \left[\frac{2}{g_{m1} + g(\Delta\omega)} + \frac{1}{g_{m1} + g(2\omega)} \right] \tag{5.17}$$

$$g(\omega) = \frac{1}{R_s} + \frac{1}{j\omega L_g} + j\omega C_{gs1} \tag{5.18}$$

$$H(\omega) = \frac{g_{m1} + g(\omega)}{g(\omega)} \tag{5.19}$$

In the optimum matching condition, the input network impedance Z_{in} is estimated as $1/g_{m1}$, and LNA transconductance is calculated as

$$G_m = \frac{g_{m1}}{1 + g_{m1} R_s} \tag{5.20}$$

Equation (5.20) is the same as for the resistive source degenerated transistor, which helps to improve the voltage-current conversion linearity. Therefore, the linearity benefit of the resistive degenerated transistor still holds true for the CG-LNA. Furthermore, the gate

terminal of M_1 is AC grounded, which helps to reduce the interdependence between the 2nd and 3rd order nonlinearities. This dependence is due to the gate-drain overlap parasitic capacitance, C_{gd1}, which degrades the CS-LNA linearity [64]. All the above reasons lead to a better linearity for the CG-LNA than the CS-LNA.

5.4 Simulation Results

The UWB LNA is simulated using Cadence Specter RF. The LNA s-parameters and Noise Figure are obtained using the Cadence s-parameter simulation [see Appendix B]. The IIP3 of the LNA is simulated using the Cadence PSS simulation with two tone inputs. The LNA operates with the 1.8V power supply. Fig. 5.16 shows the S11 and gain of the LNA without the output buffer. The input impedance matching S11 is less than –8.27dB over the whole band. The LNA achieves 14.5~15.3dB gain within the bandwidth, which doesn't consider the loss of the output buffer. Fig. 5.17 shows the S22 and S12 of the LNA. The output impedance matching is less than –10dB within the bandwidth. The isolation S12 is less than –50dB over the bandwidth. Fig. 5.18 shows the Noise Figure of the LNA. The NF of the LNA is 3.57dB~4.27dB from 3GHz to 10GHz. The linearity is checked in 5GHz with 5.1GHz and 5GHz two-tone inputs. Fig. 5.19 shows the IIP3 of the LNA. The IIP3 of the LNA is 3.43dBm.

The simple drain current (I_D) expression can be expressed as (5.21) [80]

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{x^2}{1+\theta x} \tag{5.21}$$

The power consumption can be calculated as

$$P_D = VDD \times I_D = VDD \times \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{x^2}{1+\theta x} \tag{5.22}$$

where

$$x = 2\eta\theta_t \ln\left(1 + e^{\frac{V_{gs}-V_{th}}{2\eta\phi_t}}\right) \tag{5.23}$$

V_{th} is the threshold voltage, ϕ_t is the thermal voltage $\frac{KT}{q}$, θ is the normal field mobility degradation factor, and η is the rate of exponential increase of drain current with gate-source voltage in sub-threshold region and the size of the moderate inversion region. θ is typically 0.3~0.7 V^{-1}.

In this design, the power consumption of the LNA is 4.3mW without the output buffer.

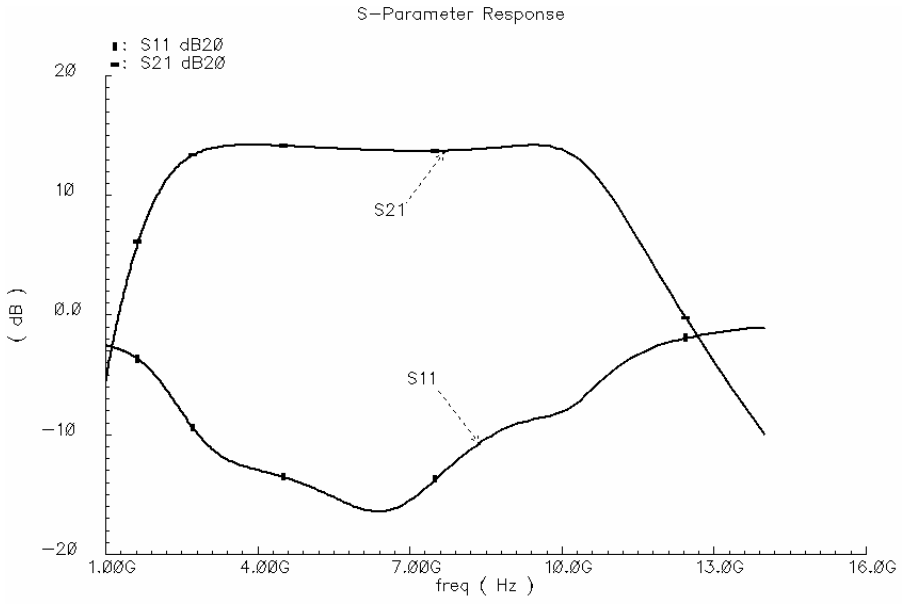


Fig. 5.16 Simulated S11 and voltage gain of the LNA

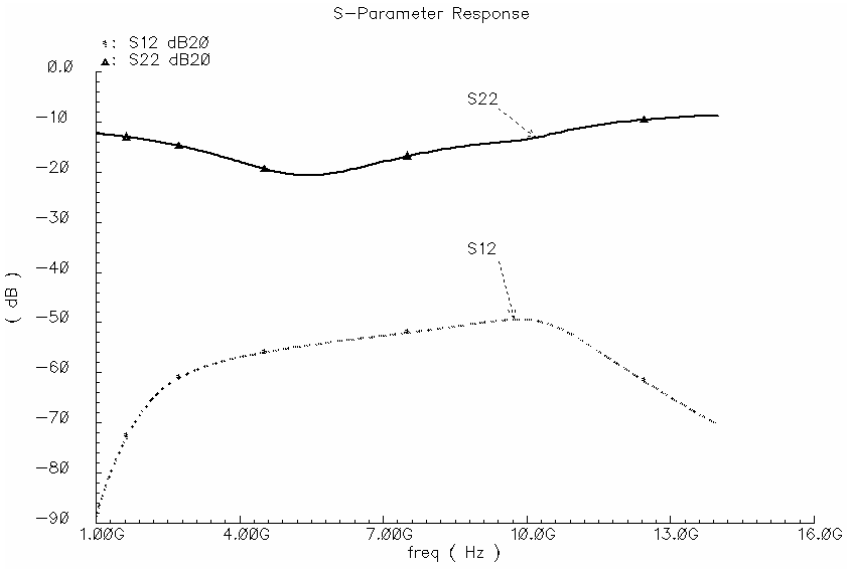


Fig. 5.17 Simulated S12 and S22 of the LNA

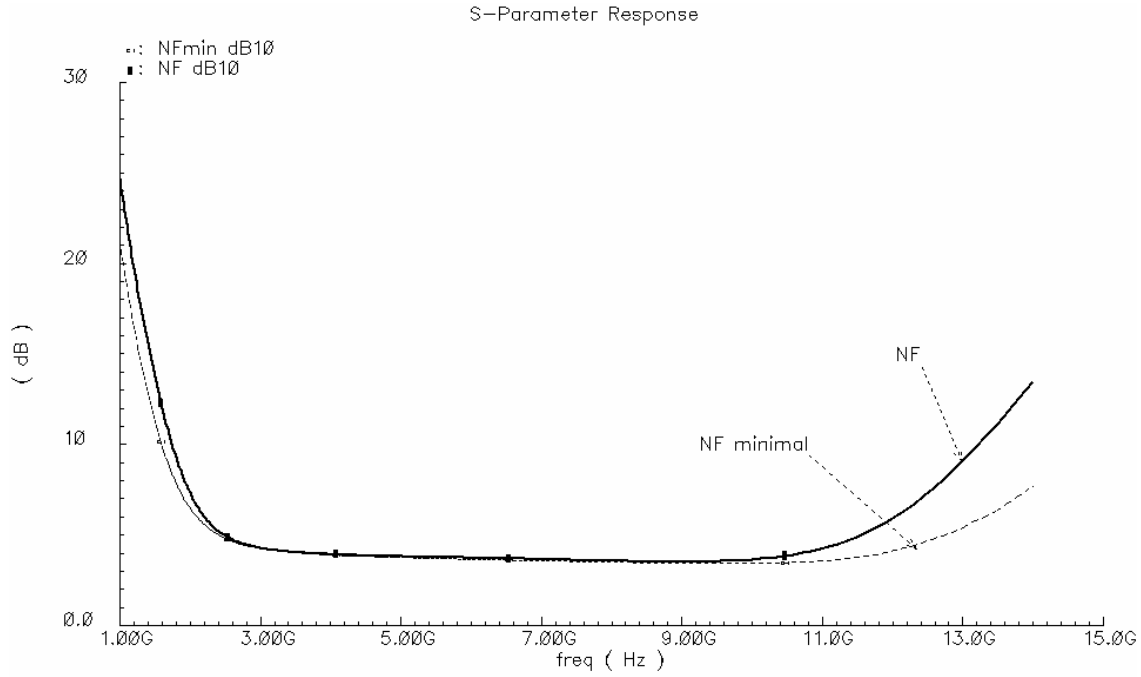


Fig. 5.18 Simulated NF of the LNA

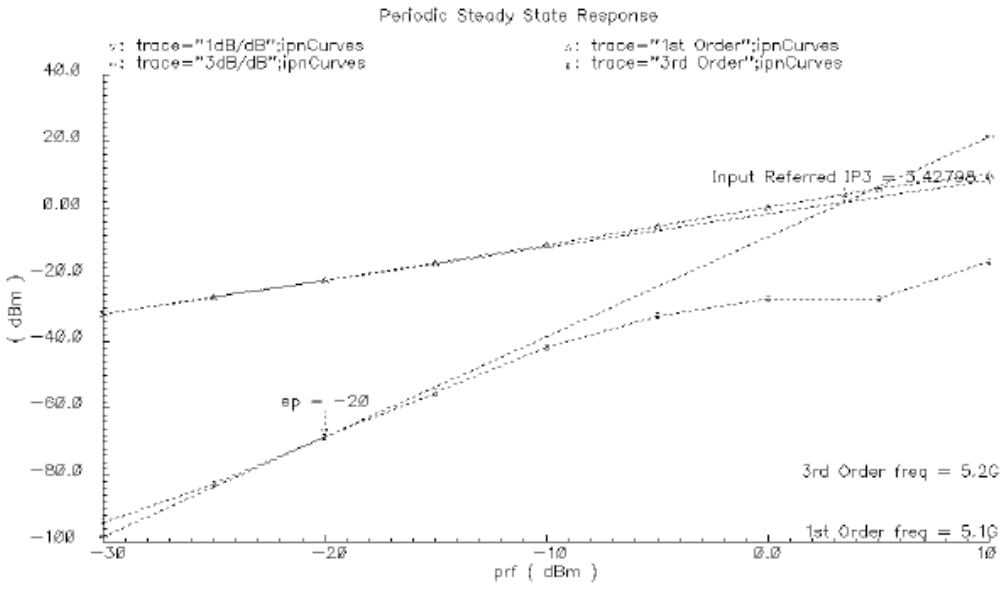


Fig. 5.19 Simulated IIP3 of the LNA

The designed LNA is compared with the design targets, which is shown in Table 5.7

Table 5.7 Simulation results compared with the design targets

Parameters	Design targets	Simulation results
Frequency(GHz)	3.1~10.6	3~10
S11(dB)	<-10	<-8.28
S21(dB)	>10	14.5~15.3
NF(dB)	<4.5	3.57~4.27
IIP3(dBm)	>-5dBm	3.43
Power(mW)	<10	4.43
Power supply(V)	1.8	1.8
Topology	Filter based CG-LNA	Filter based CG-LNA
Process	0.18μm CMOS	0.18μm CMOS

From Table 5.7, the designed UWB CG LNA satisfies most of the specifications. The input matching is a little worse than the design targets due to the low Q on-chip inductors and capacitors. The common gate UWB LNA topology consumes less power and achieves higher linearity. The designed LNA performances in different frequencies are summarized in Table 5.8.

Table 5.8 Simulation results in different frequency bands

Parameters	Simulation results			
Frequency (GHz)	3.5	5.5	7.5	10
S11(dB)	-13.5	-17.8	-15.5	-8.8
S21(dB)	8.49	8.7	8.7	6.7
NF(dB)	4.72	4.48	4.28	4.5
IIP3(dBm)	4.16	3.08	6.4	3.3
Power(mW)	4.43	4.43	4.43	4.43
Power supply(V)	1.8	1.8	1.8	1.8
Topology	Filter based CG-LNA	Filter based CG-LNA	Filter based CG-LNA	Filter based CG-LNA
Process	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS

The comparison of the proposed UWB LNA performance and the published LNA's performances is shown in Table 5.9. From Table 5.9, the proposed UWB LNA consumes minimal power consumption, has the best linearity performance and also has reasonable flat noise performance over the frequency region.

Table 5.9 Performances compared with the prior published UWB CS-LNAs

Parameters	[49]	[50] TW LNA	[51]	[74]	[81]	[82]	This work
Frequency (GHz)	2-4.6	2.4-9.5	2-10	2-10	2-5.2	2-10	3~10
S11(dB)	<-9	<-9.4	<-10	<-10	<-9	<-7	<-8.28
S21(dB)	9.8	6.3-10.4	21~17	21	16	11.5-13.5	14.5~15.3
NF(dB)	2.3-4	4.2-9	2.5-4.5	4.7-5.7	4.7-5.7	3.3-3.5	3.57~4.27
IIP3(dBm)	-7	-8.8	-5.5	-4	~	-7.5	3.43
Power (mw)	12.6	95×1.8	27	12.5	38	9.6	4.43
Power supply(V)	1.8	1.8	3	2.5	2	2.4	1.8
Topology	Feedback CS-LNA	Filter based CS-LNA	Filter based CE-LNA	Filter based CE-LNA	Feedback CS-LNA	Feedback CE-LNA	Filter based CG-LNA
Process	0.18µm CMOS	0.18µm CMOS	0.18µm SiGe BiCMOS	0.25µm SiGe BiCMOS	0.13µm CMOS	0.18µm SiGe BiCMOS	0.18µm CMOS

5.5 Summary of the Proposed Common Gate UWB LNA

The UWB LNA faces a wideband incoming signal from 3GHz to 10GHz, which is different from the typical Narrowband LNA. To be suitable for the portable device, the LNA should consume less power. It also needs to have small Noise Figure, large gain and high linearity. The Common Gate LNA for the UWB application has been introduced, analyzed and simulated. The proposed technique UWB CG-LNA extends the typical narrowband CG-LNA to UWB CG_LNA using the bandpass filter based technique. The obtained UWB

CG-LNA consumes less power consumption, achieves higher linearity with similar gain and noise figure performance. The Butterworth filter configuration is effectively used in the input stage to absorb the parasitic capacitance of the common gate transistor, achieving broadband input impedance matching (S11<-8.28dB from 3GHz-10GHz). The combination of the shunt inductor insertion and the load inductor peaking achieves the flat gain over the whole bandwidth of the interest. The LNA is designed in standard 0.18μm CMOS technology. The simulation results verify the design procedure of the LNA.

CHAPTER VI

PROPOSED CURRENT INJECTION BASED BUILT-IN-TEST TECHNIQUE FOR RF FRONT-END*

6.1 Background

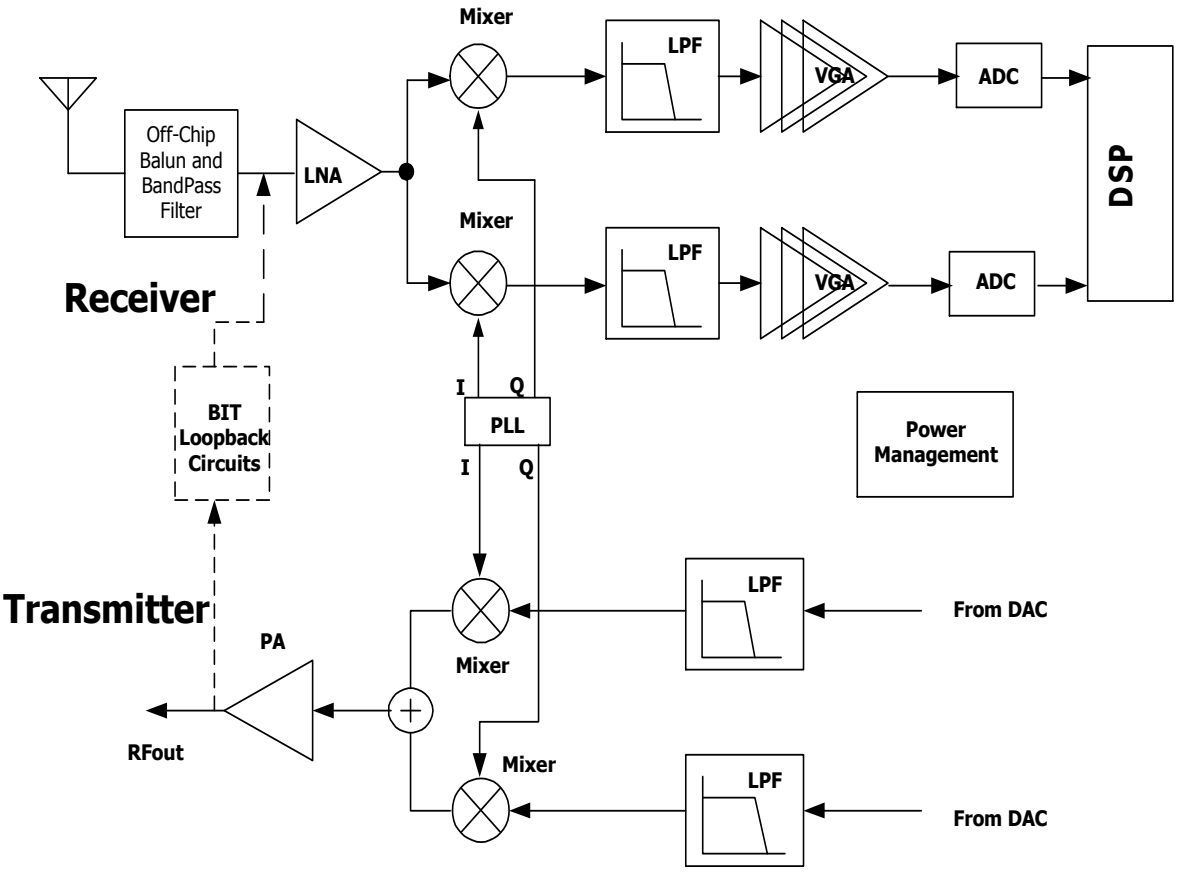


Fig. 6.1 BIT technique for the wireless transceiver

*©[2007] IEEE. Reprinted, with permission, from "A Current Injection Built-In Test Technique for RF Low-Noise Amplifiers", by Xiaohua Fan, Marvin Onabajo, Felix Fernandez, Jose Silva-Martinez and Edgar Sánchez-Sinencio, submitted to *IEEE Transactions on Circuits and Systems I:* Regular paper.

In recent years, the complexity of integrated wireless communication systems has grown considerably. One of them, the transceiver, is the interface between the antenna and the digital signal processor. It includes the RF front-end, analog baseband, and mixed-signal data conversion circuits. Testing of integrated transceivers has become a difficult and expensive (about the same as the design cost) task that makes up a significant portion of the total production cost due the rising level of integration and high operating frequencies [83]. Expensive automatic test equipment (ATE) and long test times are required with the traditional RF production test approach. Therefore, it is important to develop efficient and low-cost test procedures [84]. According to [85], a state of the art ATE in the year 2000 applies test vectors at clock rates up to 500MHz. Its cost is around $4.272M.The test cost is around 4.5 cents/second.

Built-in test (BIT) techniques can reduce the test cost by shortening test time as well as enabling the utilization of less costly measurement equipment and interface hardware. The BIT technique for the transceiver is shown in Fig. 6.1. Without the dashed block and connections, it is a typically wireless transceiver. For the conventional testing approach, to test the receiver, the signal is fed from the off-chip testing instrument and the output of the receiver blocks and system is fed to the off-chip testing instrument. Same is the transmitter. It costs a lot of time and the testing instrument is expensive. BIT technique uses the signal out of the transmitter and feeds it to the receiver through the loopback circuits. The power detectors are added at the input and output of each block to test the functionality and the performance. Therefore, less off-chip testing instruments are needed.

Among the recently reported RF BIT methods is the on-chip loopback, which was presented and modeled in [86]-[89]. For the on-chip loopback system as in Fig. 6.1, the signal from the transmitter is fed back to the receiver through the loopback circuits, which typically includes the switch, the attenuator, and the offset mixer. The signal out of the receiver is used to diagnose the functionality and the performance of the transceiver. There is another approach which uses the on-chip power detector at the input and the output of each building block to diagnose the functionality of each building block of the transceiver. In [88], for instance, the test input was obtained from a voltage signal and a preamplifier that drives the receiver through switches and an attenuator. Another RF BIT scheme for which an extra test amplifier and two power detectors are needed to characterize a low-noise amplifier (LNA) was reported in [90]. In the aforementioned works, block-level characterization was performed with input and output signals in the voltage domain, which is adequate for on-chip gain measurements. However, voltage-mode testing of impedance-matched RF circuits involves some previously unaddressed concerns discussed in the next section. Extending BIT capability to include off-chip components of the matching network has the benefit that the same BIT can be re-used at stages subsequent to wafer test.

From Table 6.1, all the previous reported topologies are either not suitable or area consuming for LNA S21 measurement with off-chip matching. In this research, a BIT technique is proposed for the LNA S21 estimation with the off-chip impedance matching.

In following sections, we examine the restrictions associated with the voltage-mode gain estimation and provide an expression applicable under ideal input impedance matching conditions. We also present a current injection based RF BIT technique as an alternative to

using a voltage input signal. The conceptual figure for the BIT technique of Table 6.1 is shown in Fig. 6.2, where the LNA and Mixer are used for illustration. The input signal comes from the on-chip voltage source V_{tx}. The power detectors at the gate of the LNA and the output of the LNA are used to estimate the LNA gain.

Table 6.1 Summary of the reported BIT techniques

	[88]	[90]	[91]
Approach	Using the voltage input drive through a switch and an attenuator	Using additional RF amplifier and two peak detectors	Using the switch to close the transceiver and using several power detectors to estimate the RF circuits gain.
Advantage	Good for loop back technique and good on-chip voltage gain measurement	Good LNA S21 measurement	Good for loop back technique and good on-chip gain measurement
Drawback	Not suitable for LNA S21 measurement with off-chip matching	Large area requirement and not identical signal path for the RF LNA and the additional RF amplifier	Not suitable for LNA S21 measurement with off-chip matching

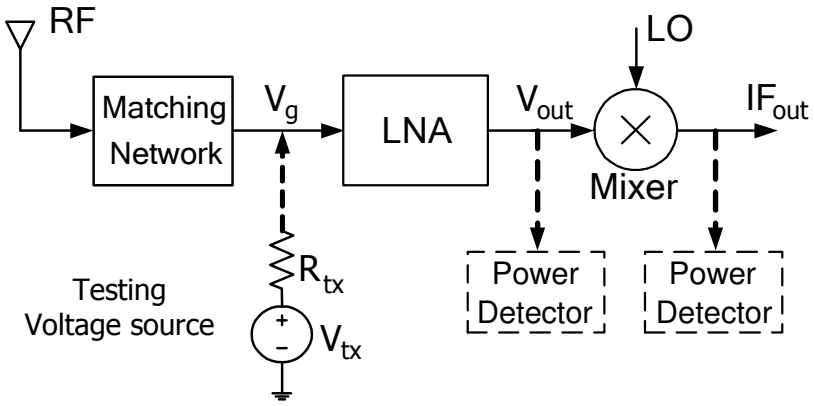


Fig. 6.2 Typical on-chip RF BIT configuration

6.2 RF Front-End BIT Issues

The transceiver topology using the Built-in-Test (BIT) is shown in Fig. 6.1. Minimization of die area, the number of additional test input/output pins, and test time are essential for cost efficient BIT. While considering these constraints, it is also desirable to integrate as much measurement and processing capability on-chip in order to utilize low-cost ATE during production testing. One of the most critical devices to be characterized in the front-end is the LNA. In this section, the feasibility of the proposed approach is demonstrated for its characterization. In a practical application, the incoming RF signal of the RF LNA is coming from the antenna with the off-chip matching network. The typical voltage mode BIT usually applies two power detectors at that gate terminal of the input transistor and the output of the LNA. It uses the different of the power level between two detection locations, which is not sensitive to the input matching network. And thus the typical voltage mode BIT can not accurately estimate the LNA gain with the off-chip components. In this research, fist a modified voltage based BIT method is proposed and also a current based BIT method is

proposed. The modified voltage based BIT method can estimate the LNA gain with the perfect input matching condition. If the input network of the LNA is not matched, it can not accurately estimate the LNA gain. Using the current injection technique, the gain estimation of the LNA does not depend on the input impedance matching condition of the LNA. It can estimate the LNA gain with the off-chip matching network.

In the following sections, first, the typical inductively degenerated CS-LNA is analyzed. Second, the conventional voltage based on-chip testing method is analyzed and the drawback is presented when testing the packaged LNA circuits. And then the current injection based BIT technique is proposed and analyzed. Following that, the implementation of the proposed scheme is discussed. Finally, the simulation results are given to verify the proposed concept.

6.2.1 Inductively Degenerated CS-LNA

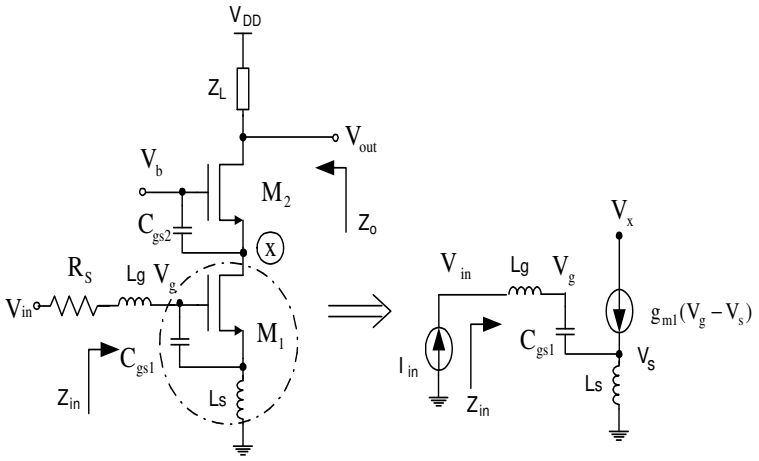


Fig. 6.3 (a) Inductively degenerated cascode CS-LNA (b) Equivalent circuit of the LNA input network

For the CS-LNA, the gain estimation is a very important target for the built-in-test method. Most RF front-ends have some off-chip components as part of the input matching network to fulfill the low noise requirement and to absorb the impedance of the package bonding wire. Thus, it is necessary to preserve the impedance matching conditions for final test (in-package or board-level). The inductor- degenerated common-source LNA (CSLNA) in Fig. 6.3 has an inductor at the source, which allows generation of real impedance at the input to achieve impedance matching and significant noise figure (NF) improvement [1] [30]-[32].

It can be derived that the equivalent input impedance of the LNA is

$$Z_{in}(s) = s(L_s + L_g) + \frac{1}{sC_{gs}} + g_m \frac{L_s}{C_{gs}} \tag{6.1}$$

where gm is the transconductance of M_1 and s=jω. The input impedance Z_{in} must be matched to R_s (normally 50Ω) at the operating frequency.

The quality factor (Q_{in}) of the CS-LNA input matching network is calculated as

$$Q_{in} = \frac{\omega(L_g + L_s)}{2R_s} = \frac{1}{2\omega C_{gs} R_s} \tag{6.2}$$

The overall voltage gain, G, of the CSLNA can be expressed as

$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{R_s + g_m \frac{L_s}{C_{gs}} + s(L_g + L_s) + \frac{1}{sC_{gs}}} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{R_s + Z_{in}} \tag{6.3}$$

where Z_o is the equivalent output impedance at the drain of M_2.

Only under impedance-matched conditions at ω_o, when $\omega_o(L_g + L_s) = 1/(\omega_o C_{gs})$ and $R_s = g_m L_s / C_{gs}$, (6.3) reduces to

$$|G(j\omega)| = \left| \frac{g_m Z_o}{j2R_s \omega_o C_{gs}} \right| = g_m Q_{in} |Z_o| \tag{6.4}$$

If the noise contribution from the cascode stage is ignored, the noise factor of the cascode CS-LNA becomes [30]-[32]

$$F_1 = 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\frac{\omega_o}{\omega_T} \tag{6.5}$$

$$\chi = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L{}^2) \tag{6.6}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g{}^2}\,\overline{i_d{}^2}}} \approx -0.395j \tag{6.7}$$

$$Q_L = \frac{\omega_o(L_s + L_g)}{R_s} = \frac{1}{\omega_o C_{gs} R_s} \tag{6.8}$$

where R_s is the input voltage source resistance, R_1 represents the series resistance of the inductor L_g, R_g is the gate resistance of M_1, ω_o is the operating frequency, and α, γ and δ are bias-dependant parameters [30]-[32]. Typically γ is 2/3 for long channel device in the saturation region and is around 2-3 or even higher for short channel device [1]. $\alpha = \frac{g_m}{g_{do}}$, which is typically 1 for long channel device and smaller than one for shout channel device. δ is typically around 5.

Since the quality factors of on-chip inductors are low, L_g is often implemented with off-chip inductor and bonding wire inductance to minimize the noise figure of the LNA; hence, it is reasonable to assume that its value is well-controlled. Being part of the test interface hardware, R_s is also external and its value is reliable. However, due to process-voltage-temperature (PVT) variations, it is very difficult to accurately predict the values of other relevant parameters such as g_m, C_{gs}, and L_s.

6.2.2 Typical (Voltage-Mode) On-Chip Testing

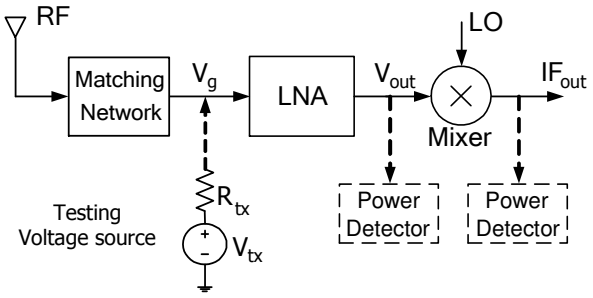


Fig. 6.4 Typical on-chip RF BIT configuration

Previously reported RF BIT testing techniques use on-chip voltage generators with 50Ω impedances, which can come from the transmitter through the switch and the attenuator or come from the on-chip frequency synthesizer. But unfortunately the signal cannot be connected at the input of the matching network unless this is done externally, which would require an extra pad and add interconnect parasitics. It is typically connected to the gate terminal of the LNA. In [88], an available signal source as shown in Fig. 6.1 was used to generate the test tone by employing switches and a 50Ω attenuator circuit that adjusts the

signal power to a satisfactory level according to the LNA input specification. A simplified diagram of that approach is shown in Fig. 6.4. Power detectors are used to monitor the power level at the LNA's output and other relevant nodes for full testing and better fault coverage.

In the voltage-mode BIT for the LNA, the test voltage signal is applied at the gate of the input transistor, which leads to loading of the input matching network by the low output impedance of the source. As a result, the off-chip matching network is bypassed because the gate voltage is forced by the test voltage source regardless of the passive component values. It can be shown that the estimated gain from V_{tx} to V_{out} in this case is given by

$$G_{tested}(s) = \frac{V_{out}}{V_{tx}} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{\left(1+\frac{R_{tx}}{R_s+sL_g}\right)\left(g_m\frac{L_s}{C_{gs}}+sL_s+\frac{1}{sC_{gs}}\right)+R_{tx}} \tag{6.9}$$

$$G_{tested}(s) = \frac{V_{out}}{V_{tx}} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{\left(1+\frac{R_{tx}}{R_s+sL_g}\right)\left(Z_{in}-R_s-sL_s\right)+R_{tx}} \tag{6.10}$$

where R_{tx} is the terminal impedance of the on-chip test voltage source and Z_o is the LNA output impedance. The magnitude of equation (6.9)-(6.10) is quite different from the voltage gain in (6.3), which complicates the assessment of the LNA performance. Unfortunately, the 50Ω output impedance of the on-chip signal generator has unfavorable effects on the input matching properties that are crucial for the signal processing in the RF front-end. The impedance matching is dependent on the carefully-designed resonant circuit at the gate of the LNA, but the loading effect of the 50Ω source impedance inserted in test mode alters the

equivalent impedance at the input gate node. For better LNA characterization, it is desirable that the test source does not significantly load the impedance matching network.

Nevertheless, two power detectors allow measuring the voltage gain from the gate of transistor M1 to the drain of M2 (Fig. 6.3):

$$\frac{V_{out}}{V_g} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{g_m \frac{L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}} \tag{6.11}$$

With ideal input matching, (6.4) and (6.11) can be combined and rearranged as:

$$\left|G(s)\right| = \frac{V_{out}}{V_{in}} = \left|\frac{V_{out}}{V_g} \times \frac{R_s - sL_g}{2R_s}\right| \tag{6.12}$$

The positive aspect of using (6.12) to estimate the gain for frequencies close to ω_o is that the highly process dependent parameters are measured with V_{out}/V_g [equation (6.11)], while the parameters of the correction factor in (6.12) are usually well-controlled. Still, a drawback of the above estimation is that impedance matching is required for the expression to be valid. As demonstrated by the results later, the above estimation methodology fails when the matching network is influenced by parasitic effects and unanticipated leakage paths due to process variation or defects. Assuming the input matching network impedance Z_{in} has a ΔZ mismatch from R_s, thus (6.12) changes to

$$\left|G + \Delta G\right| = \frac{V_{out}}{V_{in}} = \left|\frac{V_{out}}{V_g} \times \frac{R_s - sL_g + \Delta Z}{2R_s + \Delta Z}\right| \tag{6.13}$$

If $\left|\Delta Z\right| << R_s$, (6.13) can be derived as

$$|G+\Delta G| = \frac{V_{out}}{V_{in}} \approx \left| \frac{V_{out}}{V_g} \times \frac{R_s - sL_g}{2R_s} (1 - \frac{\Delta Z}{2R_s}) \right| \tag{6.14}$$

where $\Delta G \approx -\frac{V_{out}}{V_g} \times \frac{R_s - sL_g}{2R_s} \times \frac{\Delta Z}{2R_s} = -G \times \frac{\Delta Z}{2R_s}$.

From (6.14), the estimated LNA gain accuracy is influenced by the input network mismatch. Only when the input network has the perfect matching, the modified voltage based method can accurately estimate the LNA gain. For a LNA with G=20dB gain, if the input impedance is changed from 50Ω to 70Ω, ΔG is 1.6dB.

6.3 Proposed Current Injection Based RF BIT Technique

Accurate performance prediction of the circuit during final test requires that the front-end is properly terminated by the matching network. For a RF front-end BIT to be re-used during package and board test, its fault coverage must include the defects in the matching network in the presence of package parasitics.

6.3.1 RF Front-End BIT with Current Injection

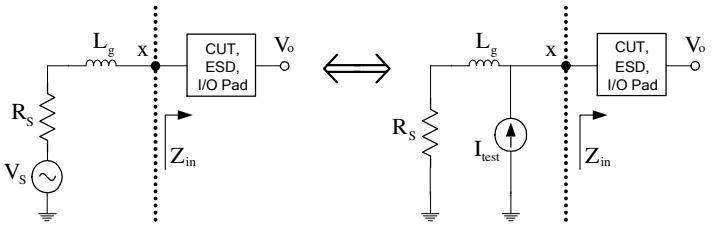


Fig. 6.5 (a) Equivalent voltage domain test input signal and (b) Equivalent current domain input test signal.

Notice that the current injection approach is comparable to the standard characterization method used in expensive RF network analyzers. Fig. 6.5 visualizes the Thévenin-Norton transformation to obtain a current source from a voltage source with a series resistor (R_s) and an inductor (L_g) at the input of the circuit. The transformation is independent of the elements at the right of the dotted line, which usually include the circuit under test (CUT), electrostatic discharge (ESD) circuitry, and parasitic elements due to the input/output (I/O) bonding pad.

The equivalent Thévenin voltage (V_s) and the voltage gain can be expressed in terms of the output voltage and the input current source as follows:

$$V_s = I_{test} \times (R_s + j\omega L_g) \tag{6.15}$$

$$G = \frac{V_{out}}{V_s} = \left(\frac{1}{R_s + j\omega L_g} \right) \left(\frac{V_{out}}{I_{test}} \right) \tag{6.16}$$

It can be verified as below.

The voltage at node X in Fig. 6.5a should equal to that in Fig. 6.5b.

It can be obtained that the voltage at node X in Fig. 6.5a is

$$V_x = V_s \frac{Z_{in}}{R_s + j\omega L_g + Z_{in}} \tag{6.17}$$

where Z_{in} is the equivalent input impedance to the right of the dash line in Fig. 6.5.

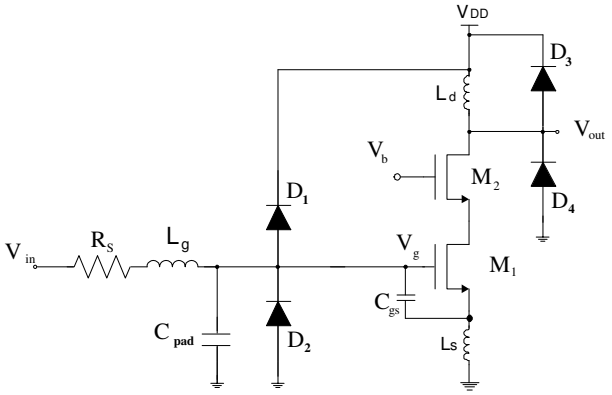
The voltage at node X in Fig. 6.5a is obtained as

$$V_x = I_{test} \times (R_s + j\omega L_g) // Z_{in} \tag{6.18}$$

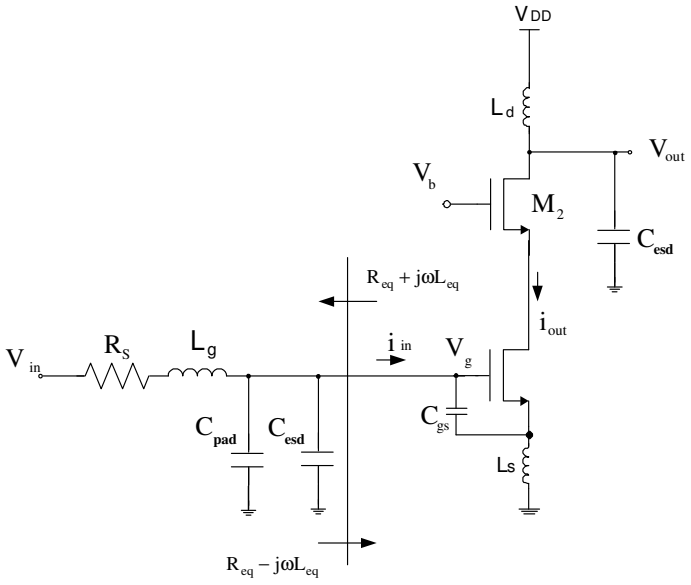
From (6.17) and (6.18), we also can get the following relation

$$V_s = I_{test} \times (R_s + j\omega L_g) \tag{6.19}$$

Thus, to fully characterize the circuit, it is necessary to measure the test current and the output voltage. In the following derivation it will be exemplified how the gain of the LNA can be estimated. ESD circuitry [92] and I/O bonding pads [92] are not included in the mathematical expressions for simplicity, but it will be shown that the final results are valid in the general case if the appropriate models for ESD and I/O parasitics are included.



(a)



(b)

Fig. 6.6(a) ESD protected LNA and (b) Equivalent circuit

A conventional ESD protected RF LNA and its input stage are shown in Fig. 6.6 [92]. The gate terminal of the transistor M1 is protected by two diodes: D1 and D2. Due to the existence of D1, the gate voltage of M1 can not exceed V_{max}=Vdd+V_{on}, where V_{on} is the turn on voltage of D1. Similarly, the gate voltage of M1 can not be lower than V_{min}=GND-V_{on}. The ESD diodes in Fig. 6.6a are replaced by a grounded capacitor C_{esd} in Fig. 6.6b.

The equivalent impedance seen to the left of the reference plate is R_{eq}. R_{eq} and L_{eq} are given by

$$R_{eq} = \frac{R_s}{\omega_o^2 C_{leak}^2 R_s^2 + (1-\omega_o^2 C_{leak} L_g)^2} \tag{6.20}$$

$$L_{eq} = \frac{L_g - C_p(\omega_o^2 L_g^2 + R_s^2)}{\omega_o^2 C_{leak}^2 R_s^2 + (1-\omega_o^2 C_{leak} L_g)^2} \tag{6.21}$$

where $C_{leak} = C_{pad} + C_{esd}$

The impedance matching condition changes to

$$R_{eq} = \frac{R_s}{\omega_o^2 C_{leak}^2 R_s^2 + (1-\omega_o^2 C_{leak} L_g)^2} = g_{m1}\frac{L_s}{C_{gs}} \tag{6.22}$$

$$\omega L_{eq} + \omega L_s - \frac{1}{\omega C_{gs}} = \omega \frac{L_g - C_p(\omega_o^2 L_g^2 + R_s^2)}{\omega_o^2 C_{leak}^2 R_s^2 + (1-\omega_o^2 C_{leak} L_g)^2} + \omega L_s - \frac{1}{\omega C_{gs}} = 0 \tag{6.23}$$

In this research, we want to estimate the LNA gain with the off-chip matching network. Since the current injection technique does not significantly loading the LNA input network, and it can estimate the LNA gain using the Thévenin-Norton transformation, the proposed technique has the advantage over the voltage mode technique. The proposed RF BIT approach is displayed in Fig. 6.7.

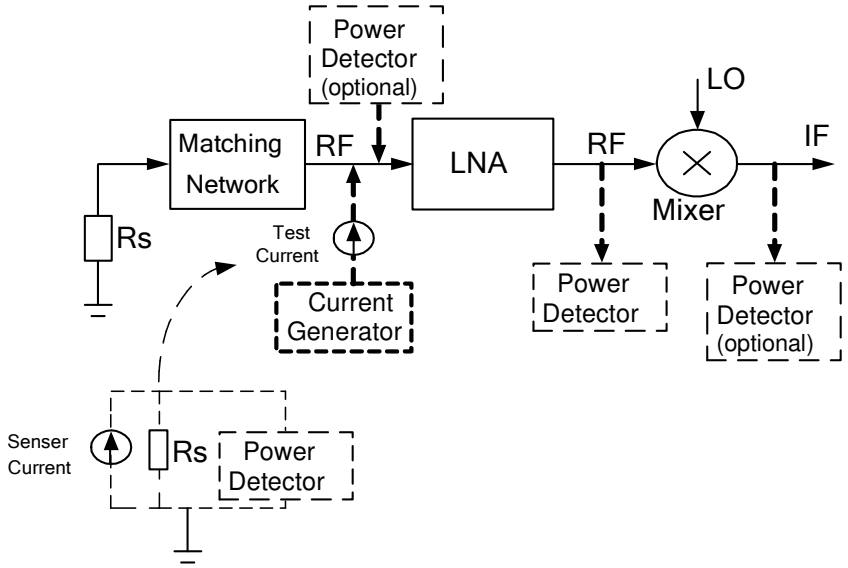


Fig. 6.7 Proposed RF BIT with current injection

It is based on current injection with all components of the matching network in place. External resistor R_s from the ATE interface hardware has a dependable value. If it is desired to check the components that are implemented on-chip during wafer test without matching network, the current injection method can also be applied with a minor modification as explained later.

An on-chip current signal is injected at the gate of the LNA using a current generator with high output impedance to avoid loading effects at the injection node. Two power or peak detectors such as the ones reported in [93] and [94] are required for this BIT. Similar to other previously reported techniques, power detectors can be placed at relevant testing points of the transceiver to increase fault coverage. The power detectors typically sense the root mean square (RMS) of the signal amplitude. The peak detectors measure the maximum signal amplitude. The power detector dynamic region needs to cover the LNA input and output

signal power level region. In this design, 25dB dynamic region is desired for the power detector. The current generator accuracy is not critical because the BIT scheme uses the power detector to estimate the input current signal level. It is only required for the output current to be large enough to satisfy the requirement of the power detector.

6.3.2 Implementation of the Current Injection BIT Scheme

The proposed testing scheme applied to LNA characterization is shown in Fig. 6.8.

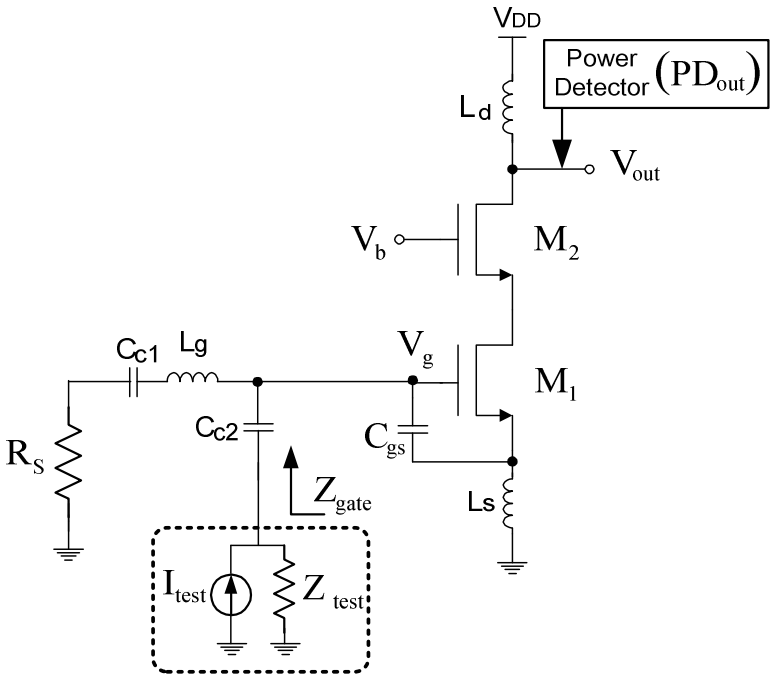


Fig. 6.8 CSLNA test with on-chip current injection (C_{c1} and C_{c2} are DC blocking capacitors)

The current generator poses high impedance (Z_{test}) at the test node. Z_{test} of the current generator is a network of resistor and capacitor, which is presented later. Assuming that the

gate inductor value (L_g) and external (R_s) are accurate; the LNA's gain can be predicted based on the following derivation. Z_{gate} represents the reactive impedance seen out of the testing voltage source, which including the contributions of C_{c1}, C_{c2}, R_s, L_g, L_s and C_{gs}. Z_{gate} and Z_{test} should satisfy (6.24) in the operating frequency, so that the current source does not load the input matching network too much.

$$Z_{test} >> Z_{gate} \tag{6.24}$$

Let us consider the magnitude of the transimpedance gain, Z_M, defined as

$$|Z_M| = \left|\frac{V_{out}}{I_{test}}\right| = \frac{\left(\frac{1}{\omega C_{gs}}\right)\left(\sqrt{R_s{}^2 + (\omega L_g)^2}\right)\left(g_m|Z_o|\right)}{\sqrt{(R_s + g_m\frac{L_s}{C_{gs}})^2 + (\omega(L_g + L_s) - \frac{1}{\omega C_{gs}})^2}} \tag{6.25}$$

where Z_o is the overall output impedance of the LNA and Z_{test} is large enough to be ignored as discussed in section IV. From (6.3) and (6.25) it follows that the voltage gain, ideally given by (6.3), can be measured using the current input signal if the following de-embedding function is employed:

$$|G| = \left|\frac{V_{out}}{V_{in}}\right| = \left|\frac{V_{out}}{I_{test}}\right| \left|\frac{1}{R_s + sL_g}\right|_{s=j\omega} = \frac{|Z_M|}{\sqrt{R_s{}^2 + (\omega L_g)^2}} \tag{6.26}$$

According to (6.26), if $\sqrt{R_s{}^2 + (\omega L_g)^2}$ is determined by the reliable external components, then finding $Z_M = V_{out}/I_{test}$ allows the calculation of the LNA's gain. Contrary to (6.12), equation (6.26) is valid even when the input is not impedance-matched.

In a Cadence simulation, the gain of the LNA in Fig. 6.9 is determined from the output voltage and the voltage after R_s of the s-parameter port. Because the input is matched to 50Ω,

the terminal voltage is attenuated 6dB relative to the source voltage within the port. Using the conditions mentioned above and removing the units, (6.26) becomes

$$S_{21,dB} = Z_{M,dB} - 10\log(R_s{}^2 + (\omega L_g)^2) + 6 \tag{6.27}$$

Since the control over the external components R_s and L_g is typically good enough, the accuracy of (6.27) relies on the precision of the Z_M measurement, which is addressed in the next section.

6.3.3 RF Current Generation and Testing

RF voltage test input signals can be produced on-chip using the voltage-controlled oscillators already present in integrated transceivers. If necessary, the power of the input signal can be adjusted with passive attenuators as demonstrated in [88]. In this paper it is assumed that the RF voltage signal is available on-chip; the goal is to generate and measure the test current.

The proposed RF test current generator for the current injection BIT is shown in Fig. 6.9. where Zgate is the impedance seen to the gate terminal of the LNA, which is typically the parallel connection of R_s+sL_g and the inductively degenerated transistor M_1.

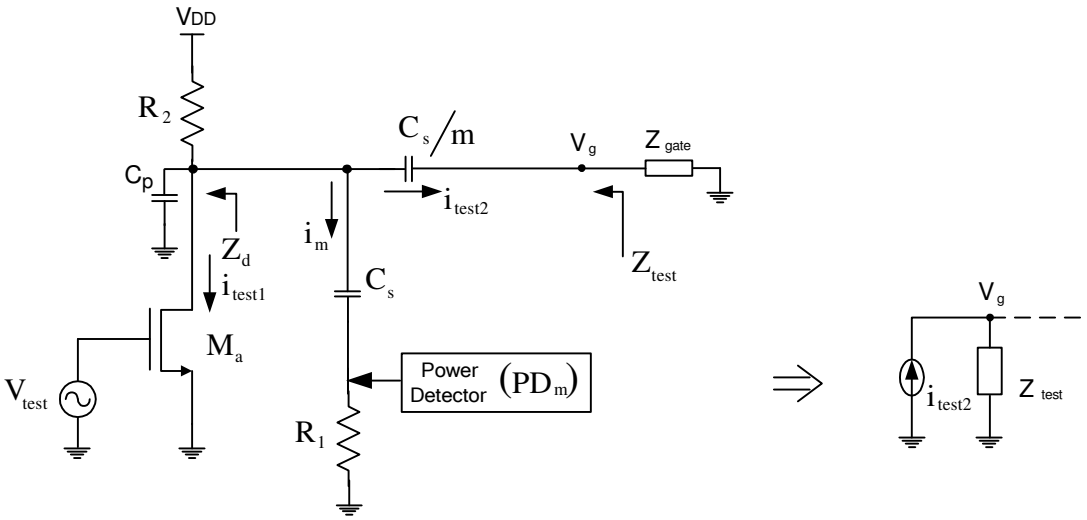


Fig. 6.9 RF test current generator (a) Circuit diagram (b) Equivalent circuit

Transistor M_a in this circuit performs the conversion of the voltage signal to current; the resulting current flows through the load components, leading to current components flowing through R_2, C_p, i_m and i_{test2}. The linearity of the current is not an issue; it can be shown [83] that proper AC characterization can be done even if the total harmonic distortion is as high as 10%. The current of interest is i_{test2}, which must be measured for proper CUT characterization. For that purpose a bank of capacitors and a termination resistor R_1 are used to generate the auxiliary current i_m. An important design consideration that is needed to accurately characterize the CUT is: $Z_{test} >> Z_{gate}$. Under this condition, the ratio of the test current (i_{test2}) and the measured current (i_m) relies predominantly on the matching of the unit capacitors (Cs/m and Cs in Fig. 6.9), having the advantage of robustness to process variations. The measured current and test current are related according to:

$$\frac{I_m(j\omega)}{I_{test}(j\omega)} = m\left(\frac{\frac{Z_{gate}}{m}+\frac{1}{j\omega C_s}}{R_1+\frac{1}{j\omega C_s}}\right)\Bigg|_{\frac{R_1}{m}=|Z_{gate}|} \cong m \qquad (6.28)$$

For a current division magnitude equal to m; good precision in predicting i_{test} by measuring i_m is obtained if R_1 is selected to be m times smaller than the impedance looking into the LNA gate node (Z_{gate}). Under the aforementioned conditions, the ratio of these two currents depends on the parameter m. The impedance seen at the gate of the LNA (Z_{gate}) in Fig. 6.8 is equal to the equivalent impedance of the resonant circuit at the desirable frequency. In the LNA being used, the magnitude of Z_{gate} at resonance is approximately 1.2kΩ.

The magnitude of i_{test} can be accurately predicted by measuring the voltage across R_1, as shown in Fig. 6.9. When the output of the root-mean-square (RMS) voltage detector reported in [93] is used for measurements of i_{test} (through the voltage across R_1) and v_{out} of the CUT, and then the measurement error due to the power detector is cancelled, except for the errors due to the unavoidable mismatches between the two detectors. These errors, however, do not significantly affect the precision of the characterization. In [91], this differential method was used to achieve less than 5% deviation between the measured RMS voltages and the theoretical values. The impedance at the drain of M_a without including the capacitor banks is $R_2 \| r_o \| 1/s\omega_o C_p$, where r_o is the output resistance of M_a. The overall impedance seen by the CUT at the resonant frequency is

$$Z_{test} \approx \frac{m}{j\omega_0 C_s} + \left(\left(R_1+\frac{1}{j\omega_0 C_s}\right) \| R_2 \| r_o \| \frac{1}{j\omega_0 C_p}\right) \qquad (6.29)$$

The small-sized series capacitors used to inject the current into the CUT allow to achieve high output impedance ($Z_{test}>10\times Z_{gate}$). This leaves sufficient freedom to optimize M_a and R_2 for the test current magnitude, voltage headroom, and noise performance.

Assuming that the RF current generator is utilized as part of the BIT configuration in Fig. 6.8 and power detectors are used for finding the magnitudes of i_{test} and v_{out}, $i_{m\_rms} = v_{m\_rms}/R_1$ can be substituted into equation (6.21). Thus, S_{21} can be predicted as follows:

$$S_{21,dB} = 20\log\left(mR_1 \times \frac{v_{out\_rms}}{v_{m\_rms}} \right) - 10\log\left(R_s{}^2 + (\omega L_g)^2\right) + 6 \tag{6.30}$$

where v_{m_rms} is the voltage measured by PD_m in Fig. 6.8. Alternatively, the RF current through R_1 could be measured using the approach described in [95], in which a sense amplifier and peak detector are utilized together with other processing circuitry in a self-calibration scheme. The conceptual diagram is shown in Fig. 6.10. The current is sensed by resistor R_{test} and processed by the sense amplifier and peak detector after the follower.

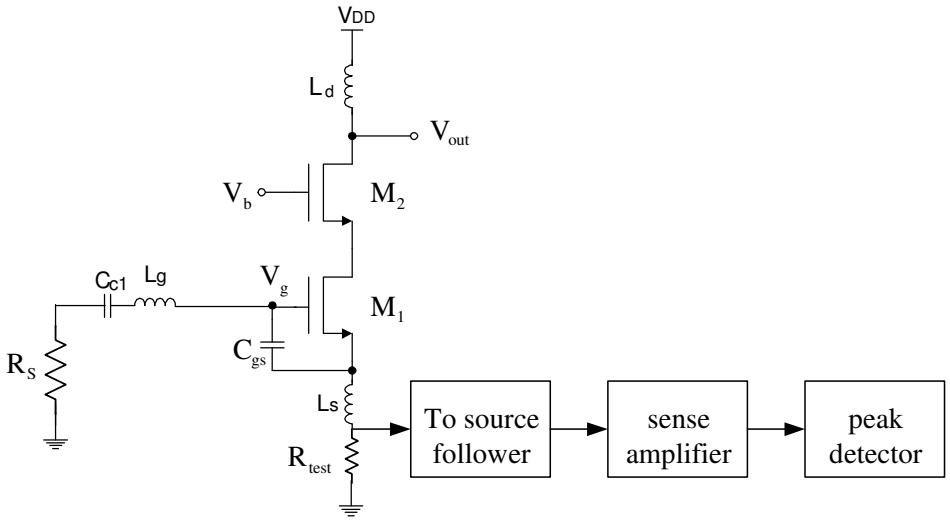


Fig. 6.10 Conceptual diagram of the current sensing approach [95]

The absolute value of the on-chip R_1 within typical variations (30%) may introduce errors of the order of 2.5 dB in equation (6.30). For this reason, the proposed BIT should be preceded by a quick DC measurement of a replica of R_1 with the ATE. Internal mismatches due to process tolerances and temperature gradients between the R_1 used in the BIT and the replica may not exceed 5%; therefore the measurement error will not exceed 0.4dB. The calibration resistor R_1 could be connected to a multiplexed test bus for DC measurements such as quiescent current tests to avoid the cost of an extra pin. In the remainder of the discussion, it is assumed that the value of R_1 has been determined prior to the BIT with an error low enough to be disregarded (<0.5 dB).

The typical voltage based method is shown in Fig. 6.2. The difference between two power detectors is used to estimate the LNA gain. Since the off-chip matching network L_g and R_s are bypassed, the conventional voltage based method can not accurately estimate the real LNA gain. The modified voltage based method is proposed, which use (6.12) to estimate the LNA gain. If the input network is perfectly matched, (6.12) can estimate the LNA gain. The proposed current injection method is summarized in Table 6.2.

Table 6.2 Summary of the proposed methods

Method	Proposed current injection method	Proposed modified voltage based method
Assumption (requirements)	A voltage source, two power detector and a well controlled off-chip inductor	A voltage source, two power detector, and a perfect input matching condition
Estimation equation	$S_{21,dB} = Z_{M,dB} - 10\log(R_s^2 + (\omega L_g)^2) + 6$ $\lvert Z_M \rvert = \left\lvert \frac{V_{out}}{I_{test}} \right\rvert = \frac{\left(\frac{1}{\omega C_{gs}}\right)\left(\sqrt{R_s^2 + (\omega L_g)^2}\right)(g_m \lvert Z_o \rvert)}{\sqrt{(R_s + g_m \frac{L_s}{C_{gs}})^2 + (\omega(L_g + L_s) - \frac{1}{\omega C_{gs}})^2}}$	$\lvert G \rvert = \frac{V_{out}}{V_{in}} = \left\lvert \frac{V_{out}}{V_g} \times \frac{R_s - sL_g}{2R_s} \right\rvert$ $\frac{V_{out}}{V_g} = -\frac{\frac{g_m Z_o}{sC_{gs}}}{g_m \frac{L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}}$

6.3.4 Design Procedure

The design of the current injection based testing circuits is as shown in Fig. 6.11

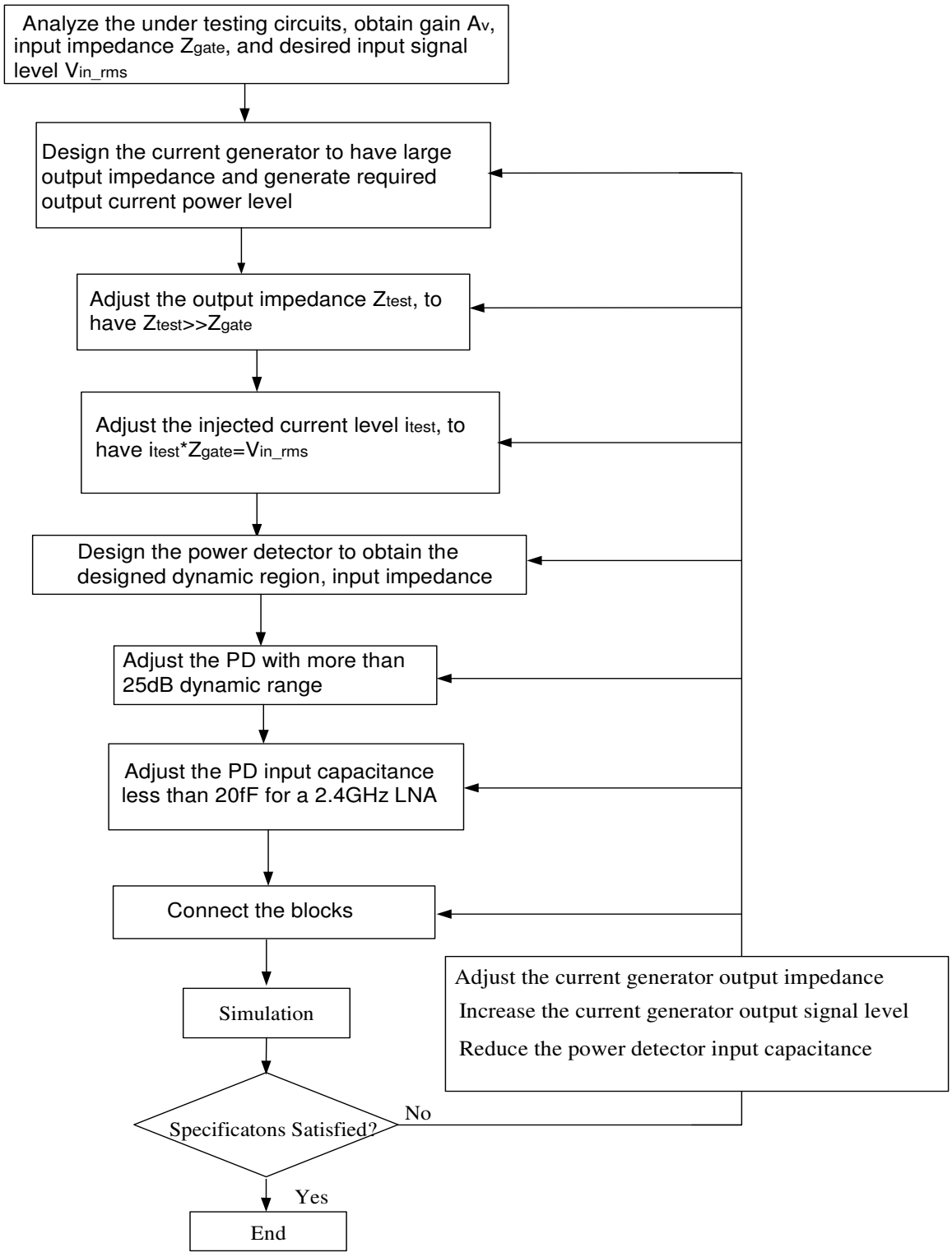


Fig. 6.11 Design procedure of the current injection based testing technique

6.4 Simulation Results

6.4.1 LNA and Current Generator Design and Performance

Table 6.3 Component values of RF BIT

LNA (Fig. 6.6)		Current Generator (Fig. 6.9)	
Component	Value	Component	Value
M_1(μm)	120/0.18	M_a(μm)	4.32/0.18
M_2(μm)	120/0.18	R_1(Ω)	150
L_g (off-chip)(nH)	23	R_2(kΩ)	2.7
L_s(bonding wire)(nH)	0.288	C_u(fF)	40
L_d(on-chip)(nH)	3	m	8
I_{M1}(mA)	4.22		
Bias Circuit		I_B(μA)	260
M_b(μm)	4.32/0.18	R_B(kΩ)	9

First, the under testing circuits are obtained. In this case a 2.4GHz CS-LNA is used as the under testing circuits. Second, analyze the desired signal level at the input and the input impedance of the under testing circuits. After that, the current generation circuit is designed to satisfy the signal power level requirement and high output impedance not to load the input of the testing too much. And then the power detector is designed with enough dynamic range according to gain and the linearity requirements of the under testing circuits. It needs to have larger than 25dB dynamic range and less than 20dF input capacitance. Following that, connect all the blocks and use the simulation to verify the concepts.

A 2.4GHz CSLNA was designed using TSMC 0.18μm CMOS technology to validate the proposed method. It is designed following the same procedure as the design procedure shown in Fig. 3.26. The detail step by step design procedure of LNA is not included here. In the simulation setup, the output of the current generator (Fig. 6.8) was injected at the gate of the LNA as shown in Fig. 6.7. The inductor L_g was assumed to be an off-chip component to minimize the noise figure; The inductor L_s was a bonding wire inductor and L_d is implemented with on-chip spiral inductor from the design kits, which can also be modeled using ASITIC [60]-[61]. The circuit parameters for the LNA and current generator are listed in Table 6. 3. The requirements for the test current generator design depend on the available voltage source, the typical input power level of the CUT, and the dynamic range of the on-chip power detectors. From the simulation, the impedance of the LNA at the gate of the transistor M_1 (gate) is around 1.2KΩ. The Z_{test} should be ten times great than Z_{gate}.

$$Z_{test} = \frac{m}{\omega C_u} >> Z_{gate} \tag{6.31}$$

From (6.31), according to the practical consideration, m=8 and C_u=40fF.

The resistor R_1 is used to sense the current flowing though the LNA. To satisfy (6.28), the following relation should hold true

$$\frac{\frac{Z_{gate}}{m} + \frac{1}{j\omega C_s}}{R_1 + \frac{1}{j\omega C_s}} = 1 \tag{6.32}$$

R_1 was selected equal to $Z_{gate}/m \cong 150\Omega$.

The current generated should flow to the LNA rather than R_2 in Fig. 6.9. R2 needs to be very large and satisfy

$$R_2 << \left(\frac{Z_{gate}}{m} + \frac{1}{j\omega C_s} \right) // R_1 + \frac{1}{j\omega C_s} \qquad (6.33)$$

Since the current will be measured by R_1, the absolute value of R_2 is not very important. The R_2 is chosen to be 2.7KΩ in consideration of the voltage headroom.

In the discussed case, a -15dBm input signal from on-chip loop-back or an attenuator fed by a local oscillator is expected and the value of the output current was selected to generate approximately 10mV_RMS at the gate of the LNA for compatibility with the RMS detector reported in [94]. The transistor M1 needs to provide the desired transconductance. From the simulation, it is chosen as 4.32μm/0.18μm. It needs 0.28mA bias current and has 1.74mS transconductance.

R_1 was selected equal to $Z_{gate}/m \cong 150\Omega$. Under these conditions, the power levels at the LNA gate and across R_1 are comparable so that the dynamic range of the power detectors PD_{out}-PD_m only has to cover the gain from the gate of M_1 to the drain of M_2 in Fig. 6.6. The 89.6$\mu A_{_RMS}$ measurement current through R_1 creates a voltage drop of 13.4$mV_{_RMS}$, which corresponds to -24.5dBm to be detected by PD_m. Table 6.3 summarizes the Cadence SpectreRF simulation results for the performance parameters of the standalone LNA and the test current generator with the equivalent load of 1.2kΩ at the resonant frequency.

LNA is an example used to verify the proposed testing method. The specifications of the LNA are not the design target. Its performance is shown in Table 6.4. The current generator circuit needs to provide an injected current with high output impedance. The injected current

is measured using the power detector, which is explained in [93]. The power detector has more than 25dB dynamic range and less than 20fF input capacitance. In this design, the signal level is measured directly using the simulator tools rather than a real power detector. In a similar design in UMC 0.13µm technology, a power detector is used, which is similar as that in [93]. Its basic conceptual diagram is shown in Fig. 6.12

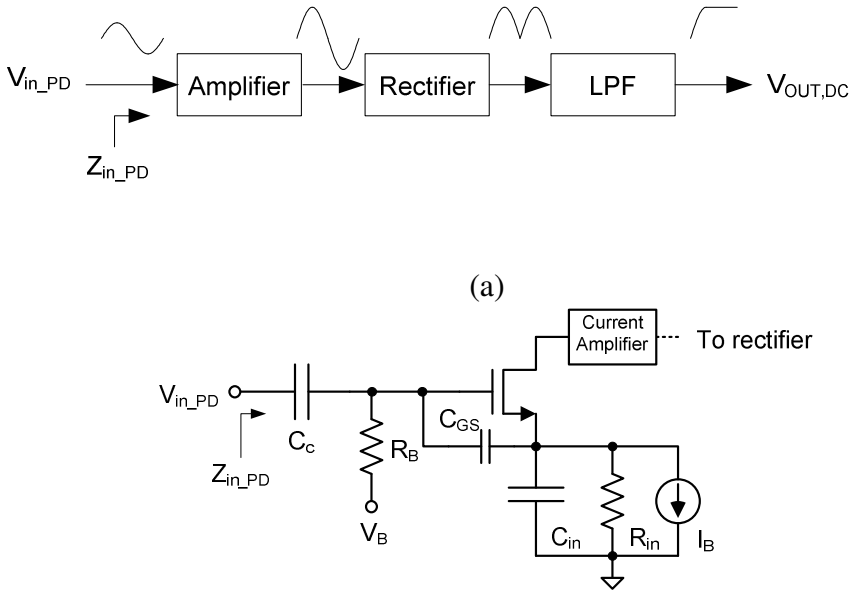


Fig. 6.12 (a) Power detector conceptual block diagram and (b) Power detector equivalent input (amplifier) stage

The basic concept behind the pseudo-RMS power detection is visualized in Fig. 12a. First, the input stage senses the RF signal and amplifies it to a desired level at which further manipulation is achievable. This signal is then rectified and finally low-pass filtered to generate a pseudo-RMS equivalent DC output element [93]. The relation between $V_{out,DC}$ as a function of $V_{in\text{-}PD}$, Amplification is shown in Fig. 6.13 using a 0.13µm design as an example.

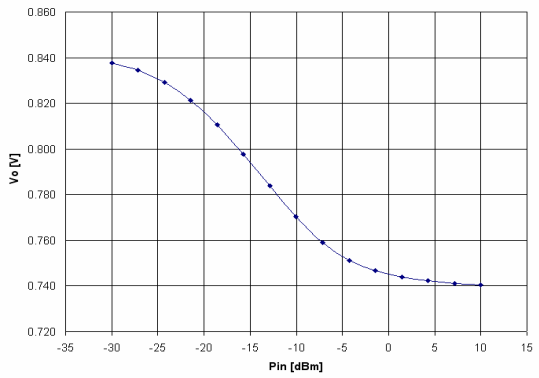


Fig. 6.13 Power detector DC voltage output vs. input power in dBm

The input stage of the PD is conceptually depicted in Fig. 6.12b. The noise of the power detector is typical in the range of microvolt and does not limit the dynamic range.

Table 6.4 Simulated LNA and current generator specifications

LNA (Fig. 6.8)		Current Generator (Fig. 6.9)	
Parameter	Value	Parameter	Value
S_{21} @2.4GHz	15.4dB	$g_{meffective}$ (i_{test} / v_{in})	142µS
NF @2.4GHz	1.24dB	IIP3	0.94dBm
S_{11} @2.4GHz	-23.3dB	1dB Comp. Point	-9.0dBm
S_{22} @2.4GHz	-13.9dB	Spot Noise @2.4GHz	1.93×10^{-17} V^2/Hz
Supply	1.8V	Supply	1.8V
Power	7.6mW	Power	0.97mW
Technology	0.18µm CMOS	Technology	0.18µm CMOS

To test the CUT at different power levels, several options exist: i) the current division ratio can be changed by using a digital control and switches to alter m; ii) the power of the input signal (V_{in} in Fig. 6.9) can be adjusted through a programmable attenuator; iii) a variable resistor can be used for R_2 in Fig. 6.6 to vary to test current, which would be the most efficient option since a PMOS transistor operating in triode region may serve for that purpose. In this design, the current i_{test} (~11μA_RMS) was adjusted such that V_g=11mV_RMS at the LNA gate, which is chosen to match the same power level when the input of the LNA is -30dBm power level signal. The spot noise measured at the gate of the LNA was around 1.93×10^{-17} V^2/Hz at 2.4GHz; consequently, the SNR in the presented scenario is approximately 130dB–10×log(BW), where BW is the channel bandwidth defined by the targeted communication standard, i.e. for Bluetooth, BW=83.5MHz (2400MHz-2483.5MHz) [28]. There is sufficient room for attenuation of the current generator input signal and added noise from an attenuator circuit to generate voltages down to several micro-volts at the LNA gate.

6.4.2 Voltage Gain Estimation Using the Proposed Modified Voltage Based Method and the Current Injection Based Method

This section uses the simulation to verify the proposed testing topology. First, the equation used to estimate the LNA gain is repeated. Second, the LNA gain, the estimated LNA gain using the current injection method, which is calculated using (6.17) and the estimated LNA gain using the proposed modified voltage mode method, which is calculated using (6.12), are compared. Finally the summary is achieved.

For the proposed method, an example is given for a numerical example. Assuming R_l=150Ω, L_g=23nH, and R_s=50Ω are either accurately known or determined with a DC test prior to the BIT as suggested earlier; the estimated gain (G_I) using the proposed current injection methodology can be determined by substituting the known values into (6.30):

$$G_{I,dB} = 20\log\left(1200\times\frac{V_{out\_rms}}{V_{m\_rms}}\right) - 10\log\left(50^2 + (\omega\times 23e^{-9})^2\right) + 6 \tag{6.34}$$

The predicted gain with the voltage-mode approach (G_V) based on equation (6.12) is

$$G_{V,dB} = 20\log\left(\frac{V_{out\_rms}}{V_{g\_rms}}\times\frac{\sqrt{50^2+(\omega\times 23e^{-9})^2}}{2\times 50}\right) + 6 \tag{6.35}$$

A comparison among the LNA S_{21} vs. frequency and the estimated gains using the current method (6.34) and the proposed modified voltage method (6.35) is plotted in Fig. 6.14.

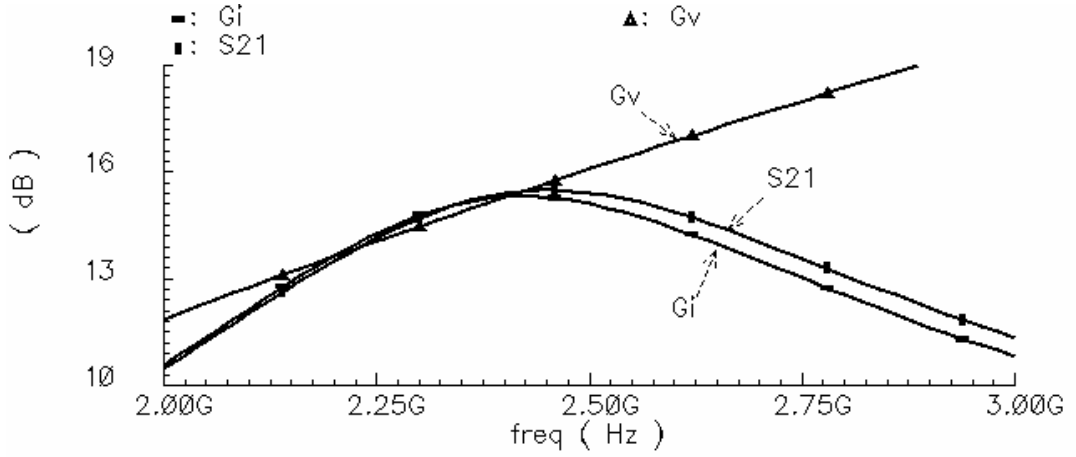


Fig. 6.14 Comparison of S_{21} and the estimated gains: proposed current technique with (6.34) and proposed modified voltage mode technique with (6.35)

The error of the estimation using the current method (6.34) and the proposed modified voltage method (6.35) is plotted in Fig. 6.15.

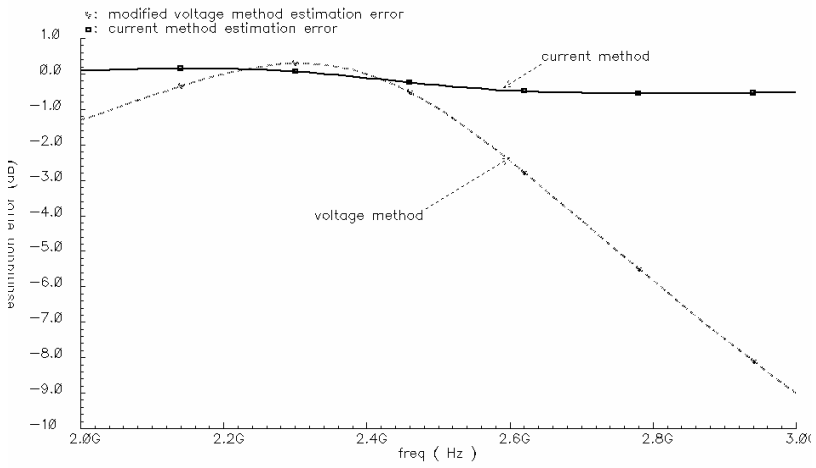


Fig. 6.15 Comparison of estimation error of the proposed current technique with (6.34) and the proposed modified voltage mode technique with (6.35)

According to the Cadence simulation results at 2.4GHz, the error between S21 and the estimated gain using the current-mode BIT system was less than 0.15dB. Additional errors will be introduced from mismatch and intrinsic linearity limitations of the power detectors. Taking 0.5dB mismatch error into account, the gain of the LNA at the operating frequency can still be estimated within 0.65dB using the proposed technique. As a reference, the results of the testing technique based on voltage-mode are depicted for the case where perfect impedance matching and de-embedding techniques are used. Notice in this plot that the current-mode testing technique is able to predict S21 over a wide frequency range.

Since the voltage-mode prediction is based on the assumption that the circuit is at resonance, the estimation error is very frequency-dependent and remains smaller than 1dB

only within 100MHz of the resonant frequency. The measurement accuracy decreases much less when the test is conducted through the current injection because the matching network is not significantly affected during characterization. The frequency-dependent error was approximately 0.5dB at 3GHz; testing at frequencies far away from the operating frequency is rarely needed. Current injection characterization error is caused by high-frequency parasitic effects and by the load impedance change at the output of the current generator when the LNA input matching circuit is not at resonance. The accuracy of the characterization is further affected by the ratio i_m/i_{test}.

The ideal ratio of these currents is 8 in this design, but it changed from 7.71 to 8.40 over the 2-3GHz frequency range. The fact that the deviation of the ratio was within 5% of the ideal value can be credited to the accuracy of the capacitor banks used in the in the current divider together with the proper selection of R_1. In addition to being minimally affected by process variation, the ratio of the capacitor impedances in the divider remains constant over frequency. The noise of the current generator is injected into the LNA same as the injected testing signal. The spot noise is very small as shown in Table 6.4, which results in a large SNR testing signal. The injected current is also measured by the power detector. And then the noise of the current injection has very small influence. The noise of the power detector is typical in the range of microvolt and does not limit the dynamic range. The detail of the power detector is as shown in Fig. 6.12 before.

6.4.3 Effect of Component/Process Variations

Equations (6.12) and (6.35) rely on the accuracy of the off-chip inductor value L_g. However, L_g varies according to its tolerance specification.

The sensitivity of the inductor L_g in the input impedance of the source inductively degenerated LNA is

$$S_{L_g}^{Z_{in}} = \frac{\partial Z_{in}}{\partial L_g}\frac{L_g}{Z_{in}} = \frac{sL_g}{Z_{in}} \tag{6.36}$$

In order to assess the sensitivity of the two methods to L_g variation, simulations were conducted with L_g values in the test setup that deviate ±5% from the value used in equations (6.12) and (6.36). The results are summarized in Table 6.5.

Table 6.5 Gain estimation at 2.4GHz with ±5% Lg tolerance

L_g	Simulation		Estimation (voltage-mode)		Estimation (current-mode)	
	S_{21}	S_{11}	G_V	Error* (S_{21} vs. G_V)	G_I	Error* (S_{21} vs. G_I)
23.0nH	15.4dB	-23.3dB	15.3dB	0.06dB	15.3dB	0.11dB
24.2nH	15.4dB	-19.6dB	15.3dB	0.03dB	15.5dB	-0.17dB
21.9nH	15.2dB	-12.4dB	15.3dB	-0.17dB	14.7dB	0.44dB

* Excludes ~0.5dB power detector error.

It can be observed from the results in Table 6.5 that the current injection approach can tolerate ±5% discrepancy between the assumed gate inductor and actual value while ensuring an error less than 0.44dB. Since L_g is an off-chip 23nH inductor, it normally can have better than ±5% tolerance according to the inductor manufacturer information. It can be observed from Table 6.5 that the current injection approach can tolerate ±5% inductor variation from the ideal inductor value with an error less than 0.5dB. From Table 6.5, we also can find that during this condition, although the proposed modified voltage mode method can not detect the variation of the gate inductor, it has better accuracy. The conventional voltage mode method can not accurately estimate the LNA gain with the existence of the input matching network. In a similar design using 0.13µm CMOS process, due to the lower Q of the input matching network, the proposed current injection based technique shows better accuracy over the proposed based technique. The drawback of the proposed modified voltage mode method will be explained further in the section later.

The typical voltage mode technique can not estimate accurately the LNA voltage gain with the existence of the off-chip matching network. The modified voltage-mode expression in equation (6.35) was proposed in this work to estimate S_{21} of the LNA even with the off-chip matching network. Its estimation is based on the perfect input matching condition (S11=-∞). From Fig. 6.14, the proposed voltage mode method can not estimate the LNA gain in the wide frequency range. It heavily relies on the perfect input impedance matching condition. In practice, the S_{11} requirement might up to -10dB. For example, for another design with the same topologies, the accuracy of the voltage-mode estimation degraded approximately 0.5dB for the re-designed LNA (S_{11}=-15.8dB) in 0.13µm technology in

comparison with the previous design (S_{11}=-23.3dB). From the table, the voltage-mode estimation technique is not able to predict the variations of L_g

Table 6.6 Gain estimation at 2.4GHz with process corner models (L_g =23nH)

Model Type	Simulation	Estimation (voltage-mode)		Estimation (current-mode)	
	S_{21}	G_V	Error* (S_{21} vs. G_V)	G_I	Error* (S_{21} vs. G_I)
Typical	15.4dB	15.3dB	0.06dB	15.3dB	0.11dB
Slow	13.4dB	13.2dB	0.21dB	13.2dB	0.23dB
Fast	17.6dB	17.8dB	-0.24dB	17.5dB	0.04dB

* Excludes ~0.5dB power detector error.

The robustness to process variation of the proposed technique was evaluated by simulating the circuits in the test setup with the fast and slow process corner models for the active and passive components of the LNA and RF current generator. In the presence of process variations, the estimated gain matches with the simulated gain of the LNA within 0.24dB in both cases; the results are provided in Table 6.6. The conventional voltage mode method can not estimate LNA gain with the existence of the input matching network. Although the proposed modified voltage mode method can estimate the LNA gain when the input is perfectly matched, it can not sense the variation of the gate inductor and thus can not detect the defects of the input network. It may be accurate than the proposed current injection method when the input network has a high quality factor and in some frequencies. The

current injection technique can detect the variation of L_g value and thus detects the defects of the input matching network. The current injection based method shows better accuracy in a wide frequency region.

6.4.4 Accounting for Parasitics

For a product in the high-volume production phase, the external inductor L_g must be selected to meet the specification targets for the design. This is done by choosing the value for L_g taking into account the ESD [92] protection circuitry as well as bonding pad and package parasitics. ESD protection diodes (perimeter = 40μm) were added to the test setup (Fig. 6.16) with the goal to evaluate the effectiveness of the current injection BIT when designers include the parasitic models along with the CUT in simulations.

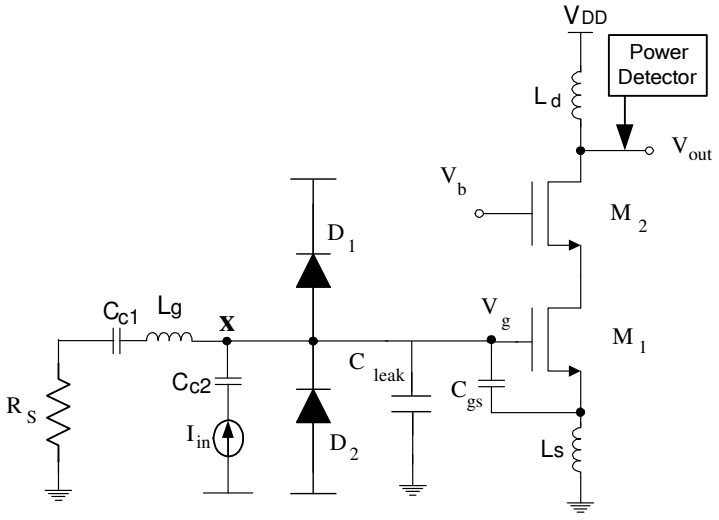


Fig. 6.16 Current injection BIT with ESD protection diodes (D_1, D_2) and an undesired leakage capacitance (C_{leak})

A capacitor can be used to roughly model bonding pad effects and unanticipated parasitics. Let us suppose that an unexpected leakage path to ground exists due to fabrication defects or variations. This leakage can be introduced by connecting a grounded capacitor (C_{leak}) between the inductor terminal and the circuitry under test. The bonding wire inductance is lumped with the L_g in this model.

Since all the parasitic elements affect the CUT impedance matching, the current-mode BIT technique is sensitive to them while voltage-mode BIT cannot detect these faults due to the low sensitivity to the variation of components in the matching network. The voltage mode can not detect the variation of the input matching network and thus can not detect the defects of the input matching network. The proposed modified voltage mode method may be more accurate in a low Q input network and in a small frequency region than the current injection based method. Fig. 6.17 shows the plots of S_{21} and the estimated gains at 2.4GHz from simulations with a sweep of the leakage capacitor value.

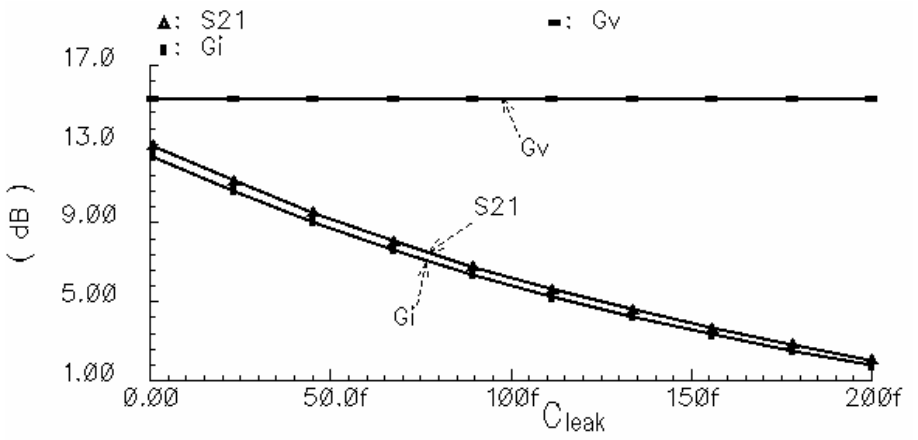


Fig. 6.17 Comparison of S_{21}, G_V, and G_I at 2.4GHz with ESD protection diodes and leakage variation (modeled by sweeping C_{leak} at node "x" in Fig. 6.16)

As S_{21} degraded from 12.9dB to 2.1dB, it was tracked correctly by G_I with a maximum error of 0.53dB. This result confirms that the transformation in Fig. 6.4 is valid regardless of the circuitry to the right of node "x". In contrast, G_V from the voltage-mode projection was unaffected by the alteration of the matching conditions at the input, resulting in errors of 2.5dB or more. If the matching is optimal, the proposed modified voltage mode method has better accuracy. The only error comes from the mismatches of the power detector at the input and the output. The current injection method has the current sensing error plus the mismatch error of the power detectors at the input and the output.

6.4.5 Impedance Termination Options

Current injection can also be used with the same circuitry for on-wafer testing or other test scenarios in which the matched impedance termination is not practical or expensive to realize. With an accurate 50Ω termination from the ATE interface hardware without L_g, equation (6.34) predicts the voltage gain when L_g=0. Thus, it is possible to perform a functionality check of the on-chip components at the wafer test stage. Likewise, L_g=0 was substituted into the voltage-mode correction factor in (6.35). S_{21} and G_I plots in Fig. 6.14 were obtained by removing L_g from the circuit in Fig. 6.17 and repeating the simulations with a sweep of the leakage capacitor at node "x" as in the previous subsection.

G_V is not included in the figure because the error was more than 5dB, but the results from the corner simulations are listed in Table 6.7. As expected, simulation results without the gate inductor demonstrated the shortcoming of the voltage-mode estimation to detect changes in

the impedance-matching network. The underlying assumption to extrapolate S_{21} using expression (6.12) is that the input matching network is fault-free, which is not guaranteed with potential fabrication and packaging defects.

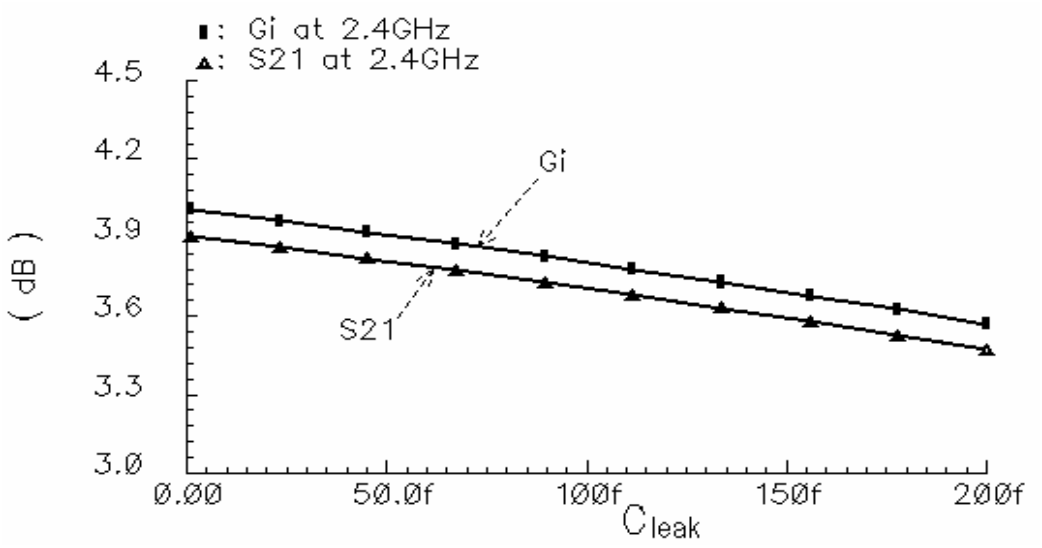


Fig. 6.18 Comparison of the simulated S_{21} with a 50Ω impedance termination vs. G_I using L_g=0 in the estimation (simulated at 2.4GHz with ESD protection diodes and leakage variation)

The plots in Fig. 6.18 show that the gain reduction effect due to unexpected capacitance (C_{leak}) is less significant and therefore more difficult to detect with a 50Ω termination because the input network is not at resonance. In this case, the equivalent impedance at node "x" in Fig. 6.16 is dominated by the 50Ω resistor, which is significantly lower than the equivalent impedance of the parallel leakage capacitor at 2.4GHz. Defects and parametric variation of M_1 and subsequent devices in the signal path are still detectable as indicated by the results from the corner simulations in Table 6.7. On the other hand, the maximum difference between S21 and G_I with the current-mode BIT was 0.12dB. S21 is the LNA

power gain. G_I is the estimated gain using the current injection method (6.34). Gv is the estimated gain using the proposed modified voltage mode method (6.35).

Table 6.7 Impedance termination (R_s=50Ω, L_g=0)
[Gain estimation at 2.4GHz with process corner models]

Model Type	Simulation	Estimation (voltage-mode)		Estimation (current-mode)	
	S_{21}(dB)	G_V(dB)	Error*(dB) (S_{21} vs. G_V)	G_I(dB)	Error* (dB) (S_{21} vs. G_I)
Typical	3.96	-1.57	5.53dB	4.06dB	-0.10dB
Slow	1.75	-3.77	5.52dB	1.86dB	-0.11dB
Fast	6.34	0.82	5.52dB	6.46dB	-0.12dB

* Excludes ~0.5dB power detector error.

Table 6.8 Comparison of gain estimation accuracy for the LNA (With process variation)

Test Goals / Conditions	Intended Application	Voltage-Mode (Estimation Error) Magnitude/%	Current Injection (Estimation Error) Magnitude/%
On-chip voltage gain measurement	On-wafer test	0.5dB[1]/3.25%	0.62dB/4.02%
S_{21} estimation with perfect input impedance-matching[2]	hypothetical scenario[3] (for comparison)	0.74dB/4.55%	0.73dB/4.74%
S_{21} measurement with degraded impedance-matching[4]	In-package/ board-level test	not suitable	1.17dB/7.6%

[1] Due to power detector mismatch only. Other results in this table include the 0.5dB power detector error discussed in section V.

[2] Without L_g variation and parasitics at the LNA input gate node.

[3] Error corrections for non-ideal matching could be explored by combining the voltage-mode S_{21} estimation with an input-match BIT such as the one in [12].

[4] Test coverage for effects of L_g variation and unexpected leakage due to parasitics/defects.

Table 6.8 contains an overview of the results from the comparison of the two techniques under investigation. From Table 6.8, both the proposed modified voltage mode method and the current injection based technique can estimate the LNA gain with the less than 5% estimation error. In the condition that the input impedance is not perfectly matched and is degraded, the current injection based technique is more suitable to use.

The power, area overhead of the BIT circuits are provided in Table 6.9. The data is coming from the similar design in a standard 0.13μm CMOS process

Table 6.9 Power, area overhead of BIT circuits

Block	Current Generator	Power detector	Total BIT circuits
Area (mW)	0.002	0.010	0.023
Area overhead (%)	1.3%	6.3%	14.4%
Power (mW)	0.4mW	0.6mW	1.6mW
Power overhead (%)	7.14%	10.7%	28.6%

This work is to verify the validity of the proposed techniques; the signal power level is obtained through the simulator rather than the power detector. The power detector power,

area and overhead are borrowed from a similar design in UMC 0.13µm CMOS process. The power detector circuit diagram is similar to Fig.6.12 [93]. The detail circuit and the component values are not included here.

The BIT area and power consumption used for RF LNA testing will be even smaller if integrated in the wireless transceiver.

The current generator needs 3 pins besides the power supply and ground pins. The power detector needs 7 pins besides the power supply and ground pins.

6.5 Summary of the Proposed Current Injection BIT Technique for RF LNA

A BIT technique that involves current injection into the RF front-end has been presented. With this approach, the input matching network is not significantly affected; neither in testing mode nor under normal operation. The current injection circuit has large output impedance (more than ten times of the impedance seen at the gate of the LNA). The power detector has a small input capacitance (less than 20fF capacitance). The BIT circuits cause less than 5dB S11changes. A remarkable benefit of the proposed approach is that the same BIT can be used during on-wafer test without proper matching and during package or board-level test with the impedance termination network.

A suitable current generation circuit with high output impedance was utilized along with a robust measurement methodology that requires two RMS or power detectors. The components of the current generator would only require a small chip area overhead of approximately $0.6\times10^{-3}mm^2$ and each of the two referenced power detectors less than

$0.02mm^2$. It was demonstrated that the ratio of the injected and measured currents does not deviate more than 5% from the ideal value between 2GHz and 3GHz.

Valid gain estimation for the LNA example was achieved on the basis of a simple formula that can be evaluated by the ATE in a production test environment. The feasibility of the current injection BIT scheme was demonstrated with the characterization of a 2.4GHz LNA using simulations in Cadence. The measured S_{21} gain and the gain estimation with the BIT circuitry matched with an error of less than 1.2dB (8%) for all corner parameters. The proposed testing methodology is suitable for on-wafer good-die characterization as well as for good chip package identification.

CHAPTER VII

CONCLUSIONS

7.1 Conclusion

In this thesis, several building blocks of the wireless receiver are examined. The existing design techniques are reviewed and their problems are pointed out. Several novel high performance circuits are proposed.

Two low power, low area and large bandwidth amplifier architectures are proposed, using a single Miller capacitor to stabilize the amplifier, which reduce the area, increase the bandwidth, and improve the settling time and slew rate performance of the amplifiers.

A noise reduction technique is proposed for a differential cascode RF LNA to reduce the noise contribution of the cascode transistor and improve the linearity performance of the LNA. The noise and linearity influence of the cascode transistor in the RF LNA is detailed analyzed. A capacitive cross-coupling technique combined with the inductor is applied to improve the RF LNA noise and linearity performance. With the propose technique, the RF LNA has 0.35dB NF and 3dB IIP3 improvement. A differential cascode CS-LNA is designed and fabricated to verify the concepts.

A filter based CG LNA is proposed for Ultra-wideband application. The input matching is obtained through the bandpass filter concept. The input stage is based on common gate LNA, which inherits the advantages of the CG-LNA for UWB application. The designed

LNA has lower power consumption, with better linearity, isolation and less sensitivity to process variation. The simulated results verify the concept.

A BIT technique is proposed for RF Front-Ends, which utilizes a current injection technique rather than typical voltage based technique to test the gain of the LNA. With the proposed technique, the LNA gain can be estimated with less than 8% error even with 10% inductor value variations. The estimated accuracy is immune to the pad capacitance and the ESD of the circuits. The proposed technique is theoretically analyzed and verified using simulation.

7.2 Future Work

A promising direction for multi-stage amplifier design lies in the low voltage and power amplifier designs in advanced CMOS technology design, such as 90nm, 60nm, 45nm and 32nm processes. In most advanced processes, the gain of the transistor is smaller while the process variation is larger, and the flicker noise corner frequency is higher. Novel amplifier circuits and design procedures are needed.

The Low Noise Amplifier design research falls in the following categories: 1) Fundamental improvement of the LNA in noise and the linearity. The noise reduction technique used in feedback LNA and CG-LNA reduces the thermal noise contributions of the transistor in LNA [35]-[36]. Meaning there should be a similar noise reduction design topology for the gate induced noise for CS-LNA. Typical linearity improvement techniques use the multiple transistors working in different regions to cancel the nonlinearity of the LNA

and improve the linearity. Almost all of the techniques use the transistor working in the weak inversion region. Since a transistor working in the weak inversion region has a lower frequency performance, it is desirable to propose an improved technique for LNA working in the higher frequency. Since the reported linearity improvement LNA were only designed for a narrowband LNA, it is desired to propose some linearity improvement techniques for the wideband LNA in the applications such as DTV Tuner and UWB. 2) LNA designs for different applications. Many wireless applications have been proposed and will reach the markets. The LNA designs for different wireless application systems are needed to satisfy the requirements. 3) Millimeter-wave LNA designs. Since the operating frequency of the wireless systems are increasing higher and higher while the bandwidth wider and wider, the LNA designs using the microwave components are attracting a lot of research effort. The noise performance of the transistor in millimeter-wave frequency regions needs to be analyzed. Millimeter-wave LNA design provides a new challenge for the researchers and the designers.

The RF circuits testing costs a lot in terms of both testing time and expense. The integration of the BIT circuits in the design reduces both the testing time and the testing cost. Typical RF BIT technique tests the gain and the 1dB compression point of the RF circuits. It will be very useful to explore the possibility of testing all the specifications of the RF circuit's on-chip in addition to the gain and 1dB compression point, such as the noise performance and inter-modulation distortion performance of the RF circuits. The power detector serves as an important building block for the BIT system. It is desired to design the

high performance power detector, which has the better resolution, occupies the less area, consumes the less power and has the larger dynamic region.

Finally, tunable RF circuits are a good direction for research. They can be integrated into the testing system. The performance of the RF circuits are detected and compared with the required specifications. The RF circuits are tuned or corrected accordingly using an analog and/or digital approach to satisfy system requirements. Novel algorithms and circuits are needed in this area.

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APPENDIX A

ROUTH-HURWITZ STABILITY CRITERIA AND STABILITY OF SMC AND SMFFC AMPLIFIERS

A.1 Routh-Hurwitz Stability Criteria

The Routh-Hurwitz stability criterion is a method to analyze the stability of the system. For a given system with single input and single output, if the characteristic equation of the closed loop transfer function is given as a polynomial, using the coefficients of that polynomial can have the idea if the system is stable or not. The characteristic equation is

$$H_{cl}(s) = a_n s^n + a_{n-1} s^{n-1} + ... + a_1 s^1 + a_o \qquad (A.1)$$

Rule 1: All the coefficients in (A.1) need to be positive (same sign) and can not be zero.

Rule 2: The Routh array in Table A.1 should be positive

Table A.1 Routh array

s^n	a_n	a_{n-2}	a_{n-4}	a_{n-6}	…
s^{n-1}	a_{n-1}	a_{n-3}	a_{n-5}	a_{n-7}	…
	b_{n-1}	b_{n-3}	b_{n-5}	b_{n-7}	…
	c_{n-1}	c_{n-3}	c_{n-5}	c_{n-7}	…
s^0	…				

In Table A.1, a_i is the coefficient of (A.1); b_i and c_i is obtained from (A.2) - (A.5)

$$b_{n-1} = \frac{1}{a_{n-1}}(a_{n-1}a_{n-2} - a_n a_{n-3}) \tag{A.2}$$

$$b_{n-3} = \frac{1}{a_{n-1}}(a_{n-1}a_{n-4} - a_n a_{n-5}) \tag{A.3}$$

…..

$$c_{n-1} = \frac{1}{b_{n-1}}(b_{n-1}a_{n-3} - a_{n-1}b_{n-3}) \tag{A.4}$$

$$c_{n-3} = \frac{1}{b_{n-1}}(b_{n-1}a_{n-5} - a_{n-1}b_{n-5}) \tag{A.5}$$

…..

Stability conditions impose that all coefficients are greater than zero. i.e. $b_{n-1} > 0$ or $a_{n-1}a_{n-2} > a_n a_{n-3}$.

A.2 Stability of the SMC Amplifier

The Close loop transfer function of SMC is

$$A_{cl(SMC)}(s) \cong \frac{1}{1 + \left(\frac{sC_m}{g_{m1}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} = \frac{1}{a_0 s^3 + a_1 s^2 + a_2 s + a_3} \tag{A.6}$$

where

$$a_0 = \frac{C_{p2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{A.7}$$

$$a_1 = \frac{g_{o2} C_L C_m}{g_{m1} g_{m2} g_{mL}} \tag{A.8}$$

$$a_2 = \frac{C_m}{g_{m1}} \tag{A.9}$$

$$a_3 = 1 \tag{A.10}$$

The stability condition of the SMC amplifier can be determined by analyzing the closed-loop transfer function with a unity-gain feedback configuration. From the equation (A.6), the order of the numerator of $A_{cl(SMC)}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator.

The Routh Array of the SMC amplifier is given in Table A.2

Table A.2 Routh array of SMC

s^3	a_0	a_2
s^2	a_1	a_3
s^1	$b_1 = (a_1 a_2 - a_0 a_3)/a_1$	
s^0	$c_1 = (b_1 a_3)/b_1 = a_3$	

Applying the Routh-Hurwitz stability criterion rule 2 to the characteristic equation of transfer function (A.6), all the coefficients in Table A.2 should be positive to stabilize the system. It yields

$$a_1 a_2 - a_0 a_3 > 0 \tag{A.11}$$

$$\Rightarrow \frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m} = GBW \tag{A.12}$$

A.2 Stability of the SMFFC Amplifier

The stability analysis utilizes the same theory as that of SMC. Neglecting the effect of the RHP zero in (2.26), the Close loop transfer function of SMFFC is

$$A_{cl(SMFFC)}(s) \cong \frac{1 + s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}}{1 + s\frac{g_{mf1}C_m}{g_{m1}g_{m2}} + \frac{sC_m}{g_{m1}}\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{A.13}$$

and

$$a_0 = \frac{C_{P2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{A.14}$$

$$a_1 = \frac{g_{o2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{A.15}$$

$$a_2 = \frac{C_m}{g_{m1}} + \frac{C_m g_{mf1}}{g_{m1}g_{m2}} \tag{A.16}$$

$$a_3 = 1 \tag{A.17}$$

From the equation (A.7), the order of the numerator of $A_{cl(SMFFC)}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator.

The Routh Array of the SMFFC amplifier is same as that given in Table A.2

The Routh-Hurwitz stability criterion provides the following condition:

$$a_1 a_2 - a_0 a_3 > 0 \tag{A.18}$$

$$\Rightarrow \frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m}\left(\frac{1}{1+g_{mf1}/g_{m2}}\right) \tag{A.19}$$

APPENDIX B

CADENCE SIMULATION PROCEDURE OF THE LNA

The LNA simulation includes the s-parameter simulation, noise simulation and the linearity simulation.

A common source LNA is used to demonstrate the simulation procedure.

The LNA and the setup for the s-parameter and noise simulation are shown in Fig. B.1.

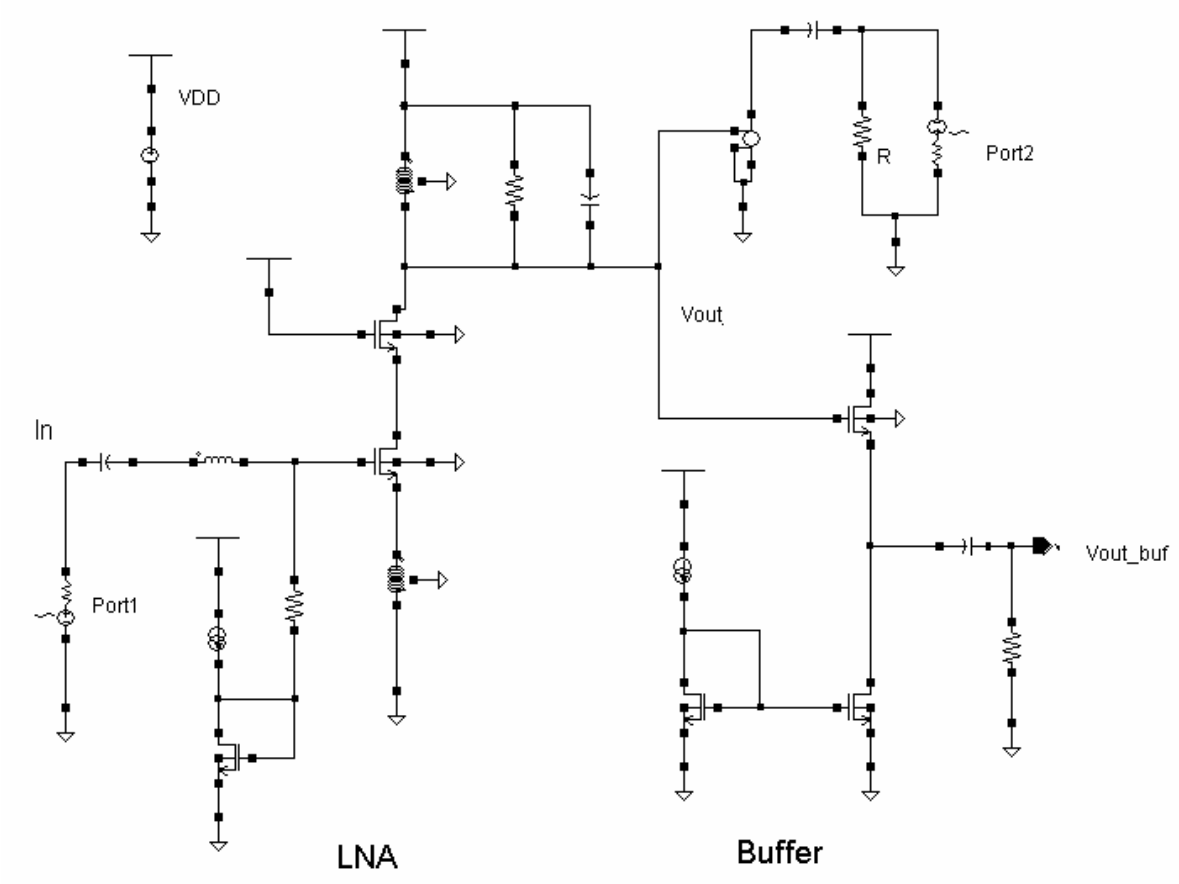


Fig. B.1 S-parameter simulation and noise figure simulation setup

A) The Simulation of S-Parameter and Noise Figure of LNA

The input is a power source “psin”, PORT1. Typically, the buffer following the LNA drives the off-chip 50Ω impedance. Here, to obtain the voltage gain and the noise figure of the LNA, a VCVS voltage source is used to sense the output voltage of the LNA and transform the output voltage signal to a power port, PORT2. A 50 Ω resistance R is placed in parallel with the PORT2 for matching purpose. The setup for PORT1 is shown in Fig. B.2. Its source type is “sine” with a 50Ω resistance.

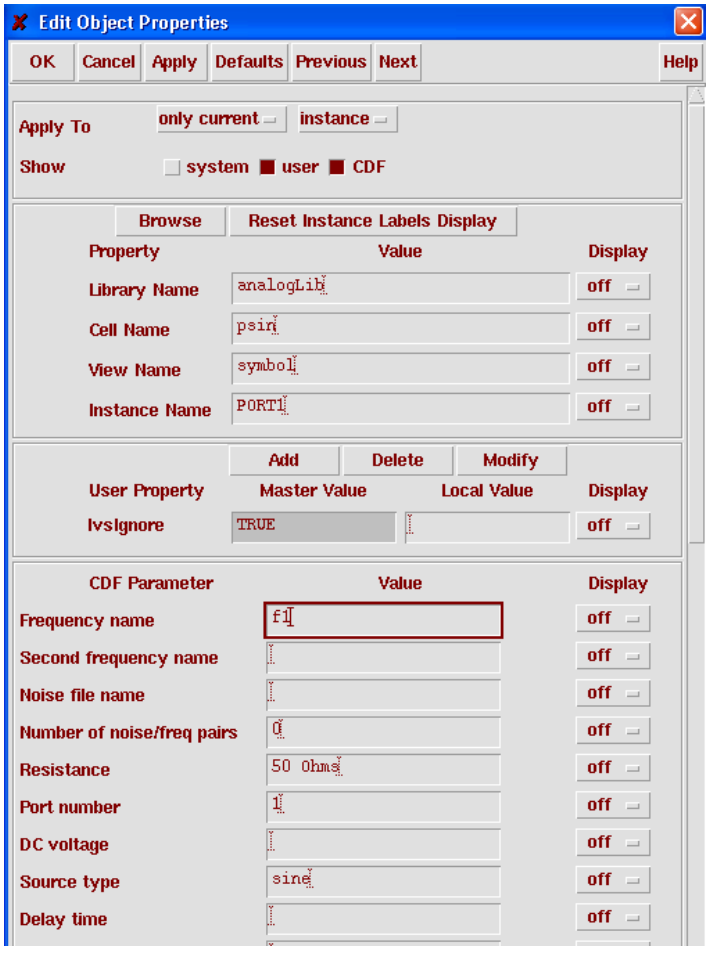


Fig. B.2 PORT1 setup

Port 2 source type is DC with a 50Ω resistance. It is shown in Fig. B.3

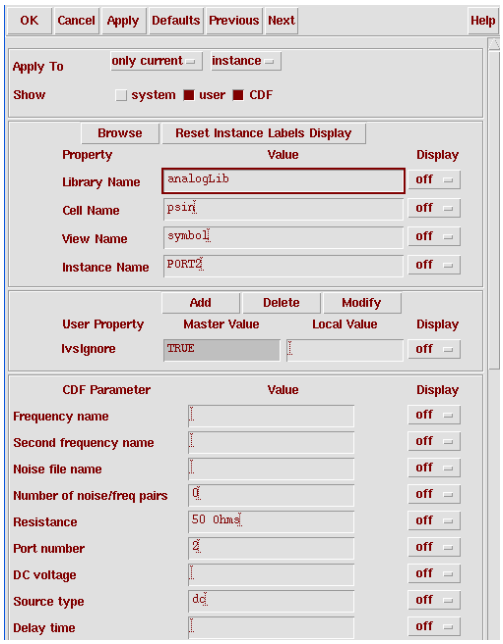


Fig. B.2 PORT2 setup

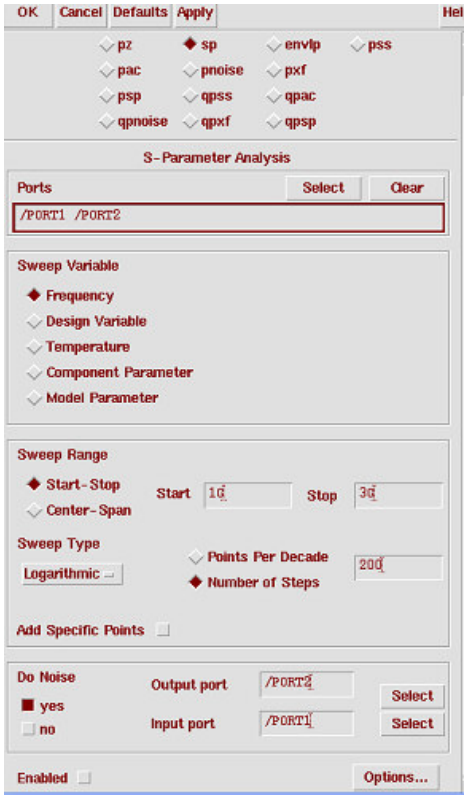


Fig. B.3. SP analysis setup

In the simulation window, select sp analysis. The ports are PORT1 and PORT2. The sweep region is the interested frequency: from 1GHz to 3GHz in this case. The noise analysis is activated. The output port is PORT2, and the input port is PORT1. The sp simulation setup is shown in Fig. B.3. Results can be shown in Analog Artist: Results/Direct Plot/Main Form/. The form of s-parameter results and that of the noise results are shown in Fig. B.4(a) and in Fig.B.4(b). The simulated s-parameter plot is shown in Fig. B.5 and Fig. B.6 shows the simulated noise figure plot. The LNA has 15.6dB voltage gain, -31dB S11 and 0.62dB NF.

Fig. B.4. (a) Form of the s-parameter results (b) Form of the noise results

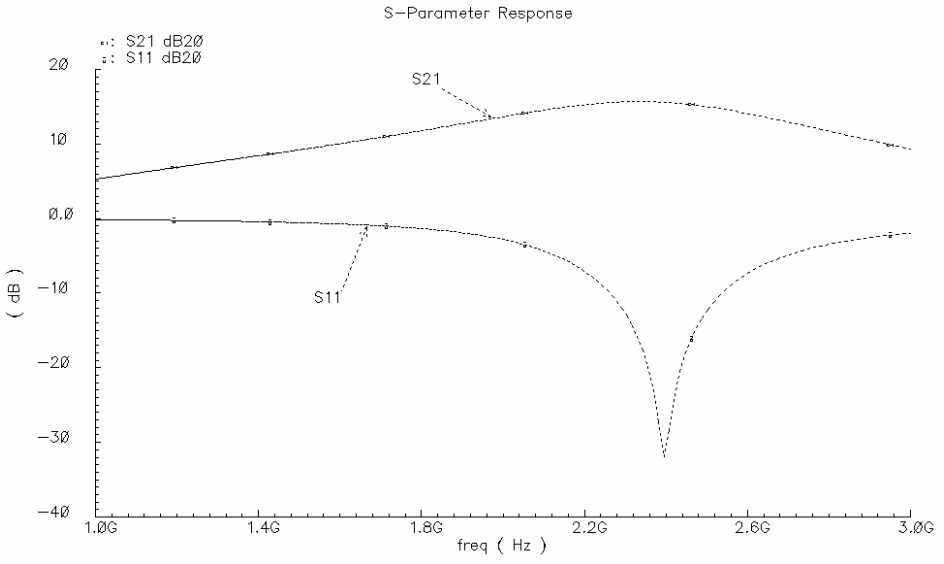


Fig. B.5 S-parameter plot of LNA

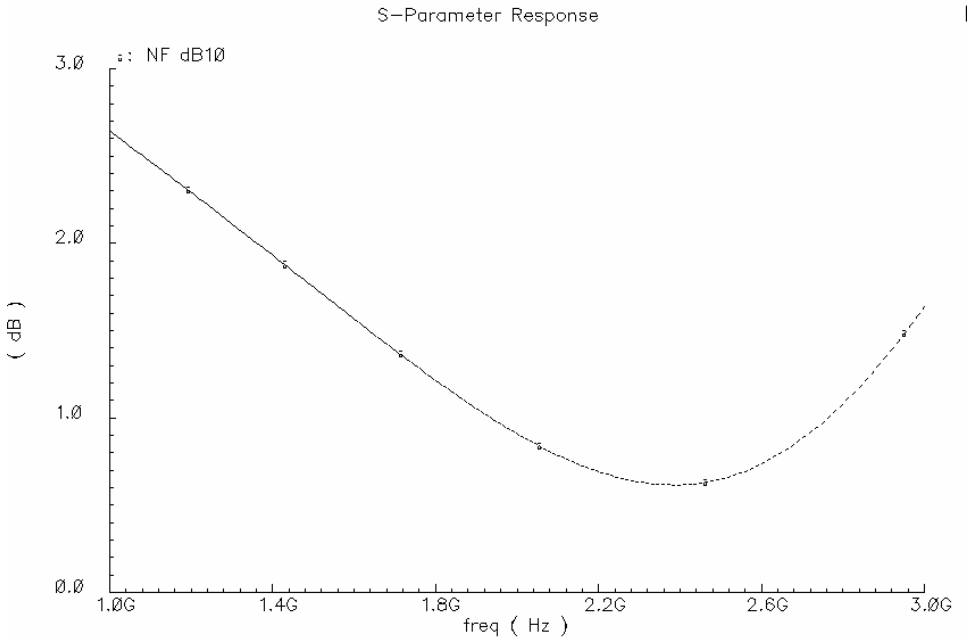


Fig. B.6 NF plot of LNA

B) The Linearity Simulation of LNA (IIP3 and 1dB Compression Point)

The IIP3 and 1dB compression point is simulated using SPSS analysis. The power source, PORT1, is set as in Fig B.7

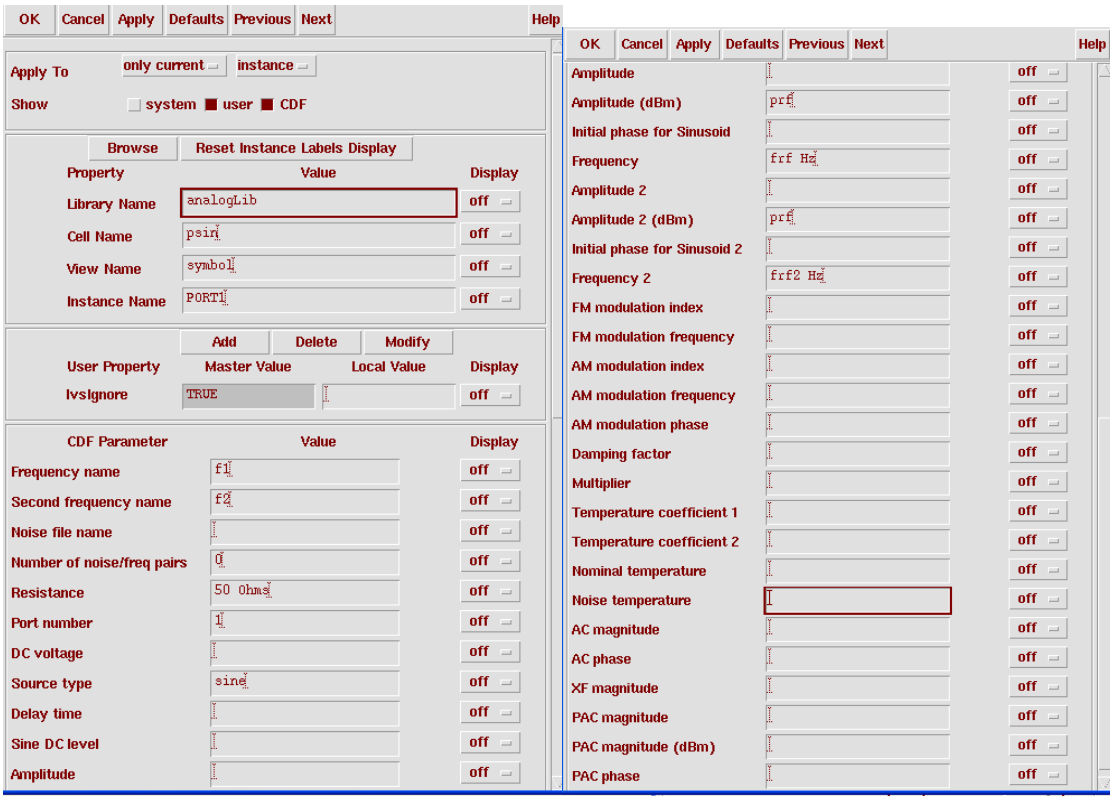


Fig. B.7 PORT1 setup for IM3 simulation

The PORT1 has two input tones at frq (2.4GHz) and frq2 (2.41GHz). The input signal power at frq and frq2 is set equal to a variable prf, which is swept from -35dBm to 5dBm in the IIP3 and 1dB compression point simulation.

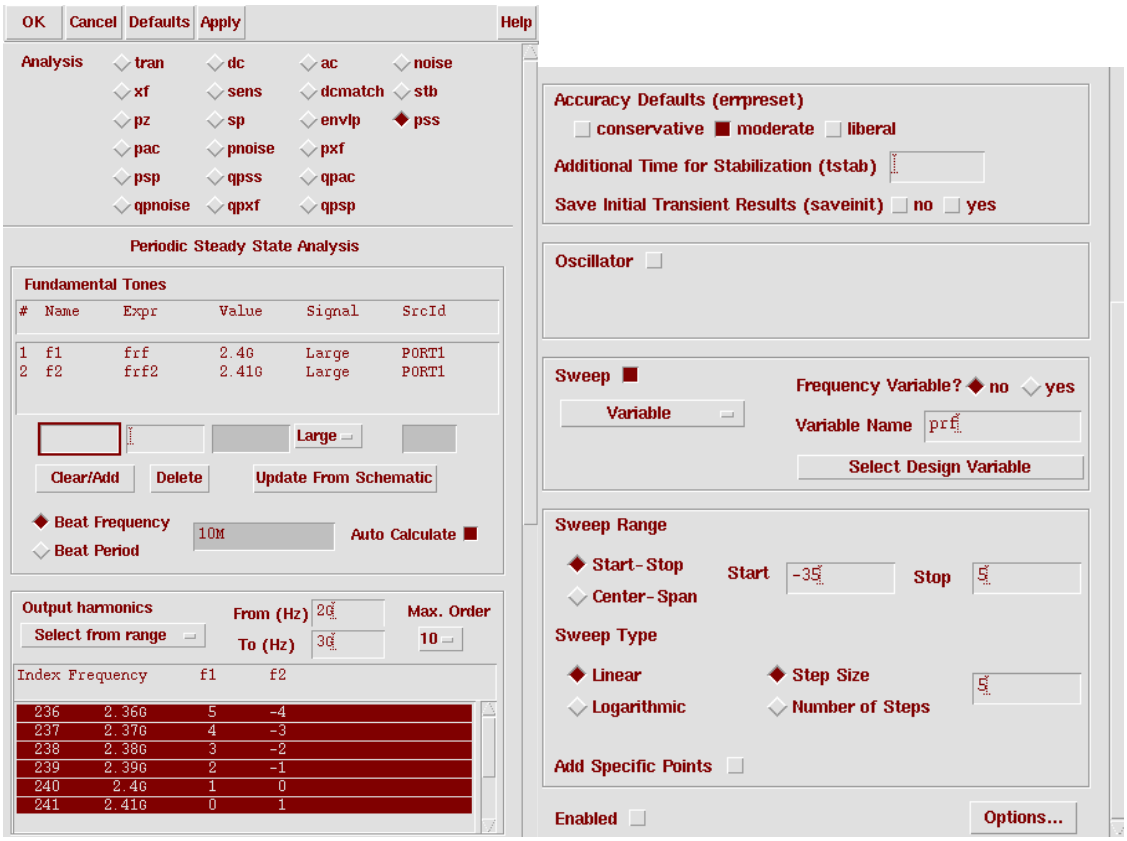


Fig. B.8 PSS analyze setup for IM3 simulation

The PSS analyze setup in shown in Fig. B.8. The beat frequency is the highest frequency common to two inputs. In the sweep section, the IIP3 simulation needs to sweep prf from -35dBm to 5dBm. The output harmonics is chosen from 2GHz to 3GHz up to 10^{th} order to save the disk space. Run the simulation. The results of IIP3 can be observed from Analog Artist: Results/Direct Display/Main Form/PSS. The results form is shown in Fig. B.9. IPN curve is chosen to show the IIP3 curve. The 1^{st} order harmonic is at 2.4GHz and the 3^{rd} intermodulation is at 2.39GHz. The output power is variable sweep, “prf”. The input power extrapolation point is selected at -30dBm. For the output, select net (specify R} and then in the schematic, click the interest net to show the IIP3 curve at that node. The simulated IIP3 of the LNA is shown in Fig. B.10. The IIP3 of the LNA is -6.85dBm.

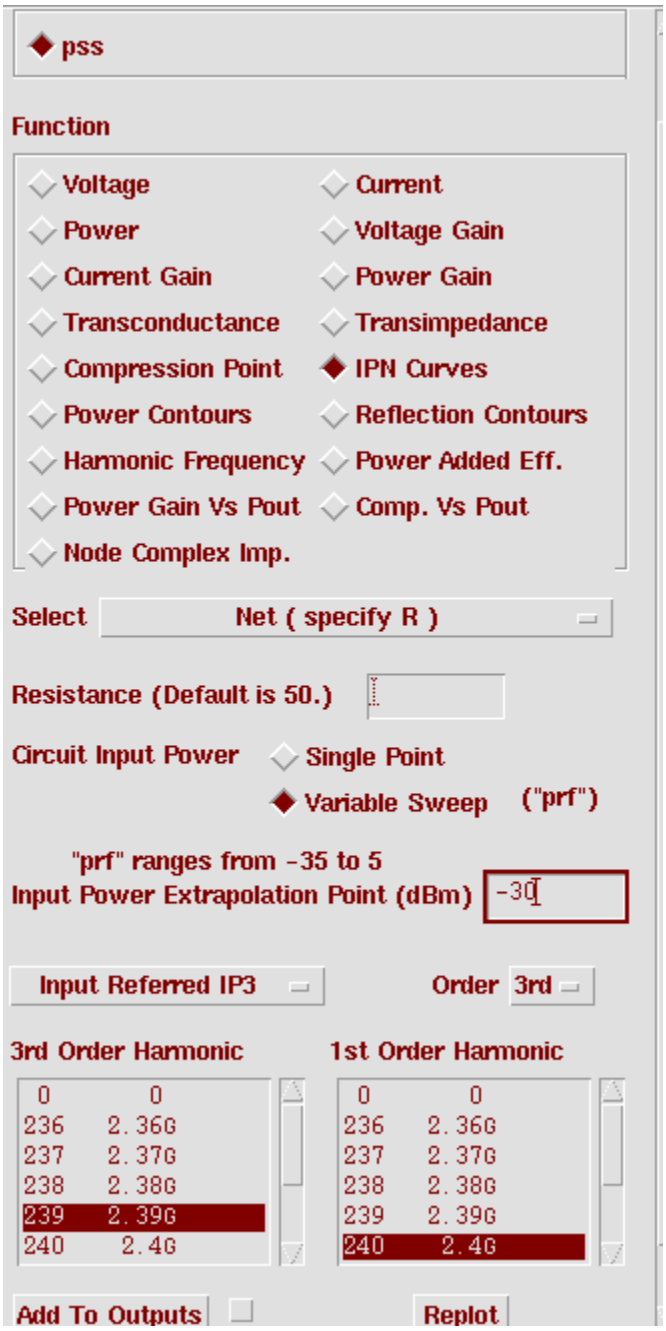


Fig. B.9 Results form of the PSS simulation

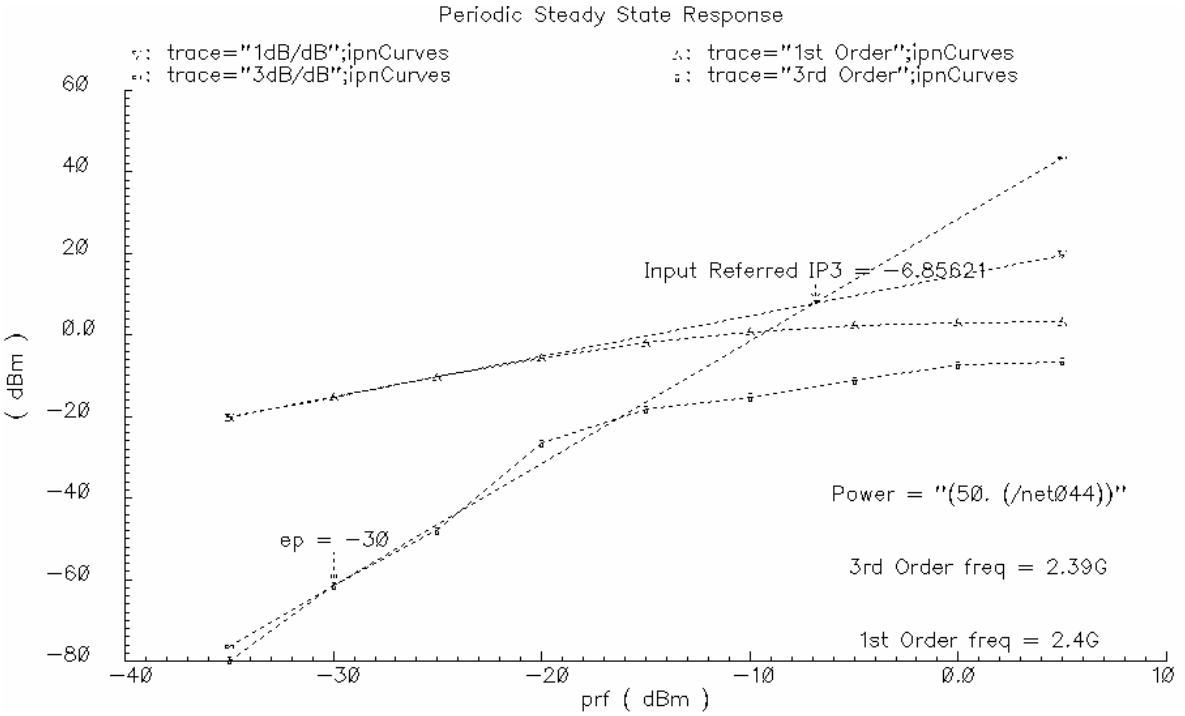


Fig. B.10 Simulated IIP3 of the LNA

Similarly, the results of 1dB compression point can be observed from Analog Artist: Results/Direct Display/Main Form/PSS. The results form is shown in Fig. B.11. Compression point is chosen to show the 1dB compression point. The gain compression is selected as 1dB. For the output, select net (specify R}. The input power extrapolation point is selected at -30dBm. The 1st order harmonic is at 2.4GHz. And then in the schematic, click the interest net to show the IIP3 curve at that node. The simulated 1dB compression point of the LNA is shown in Fig. B.12. The 1dB compression point of the LNA is -17.5dBm.

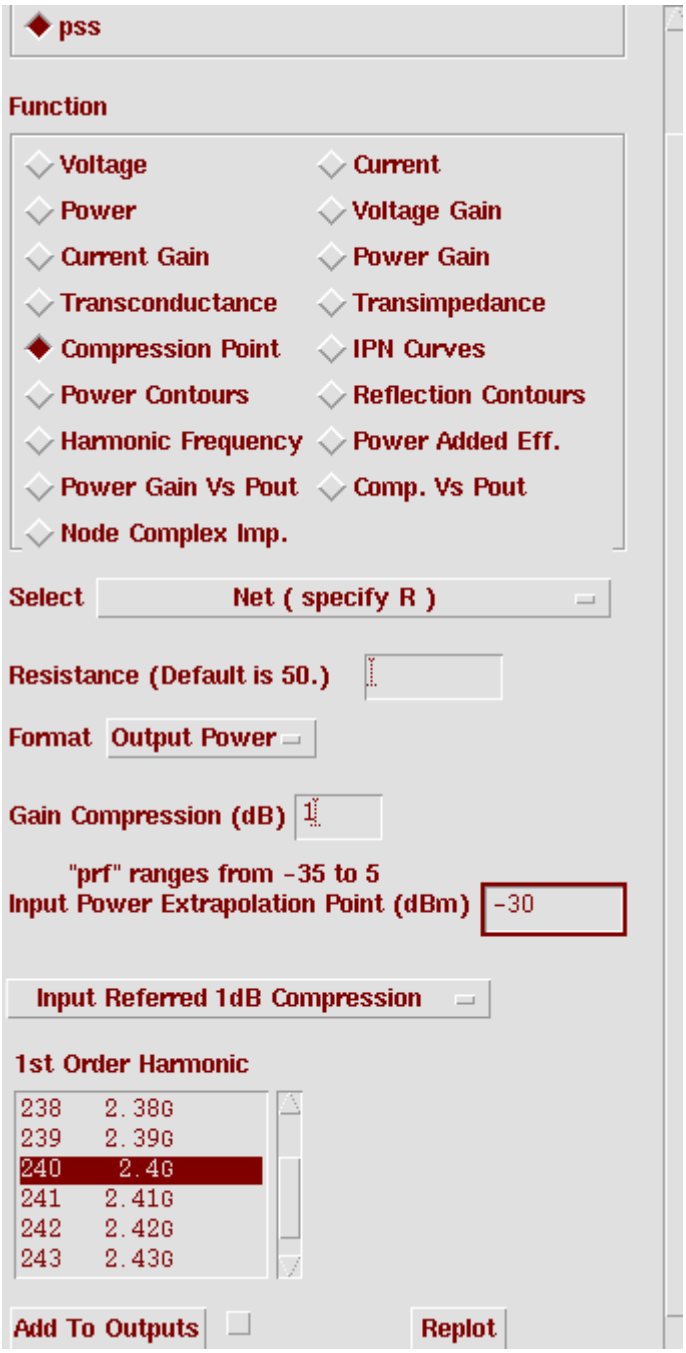


Fig. B.11 Result form of 1dB compression point

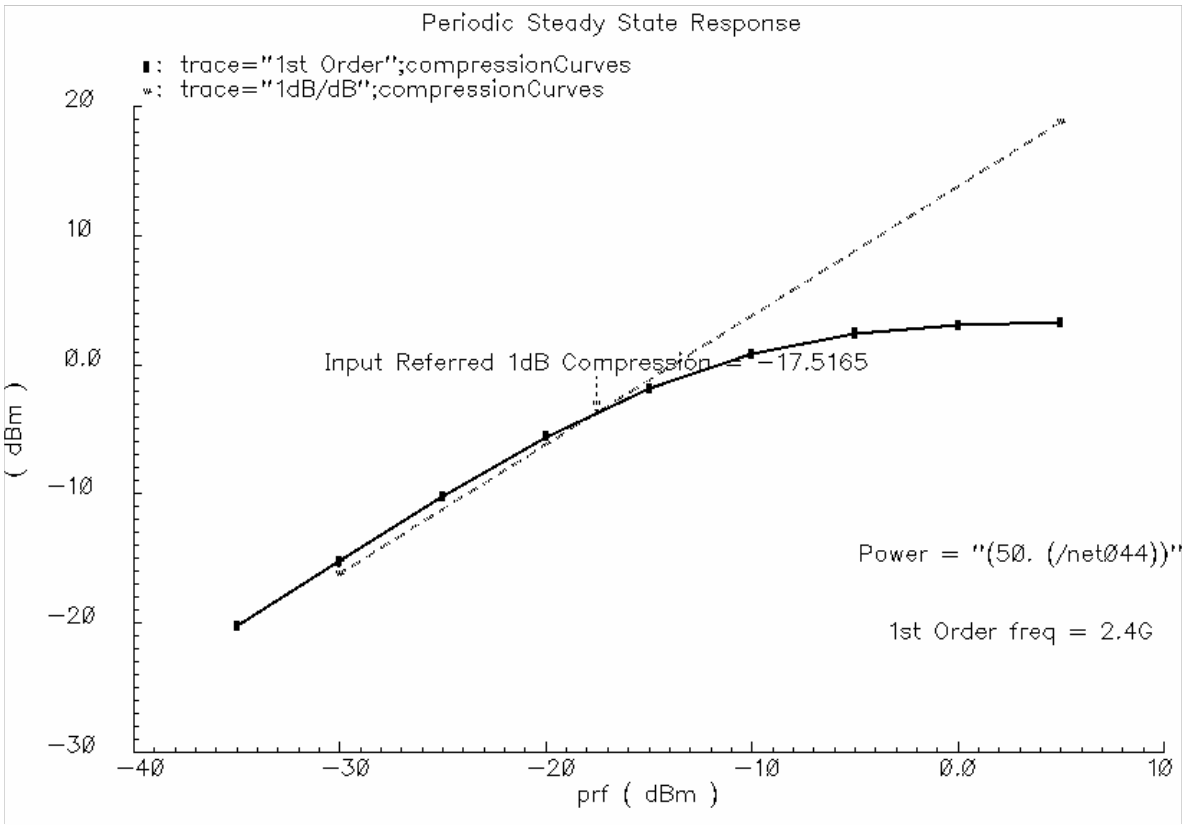


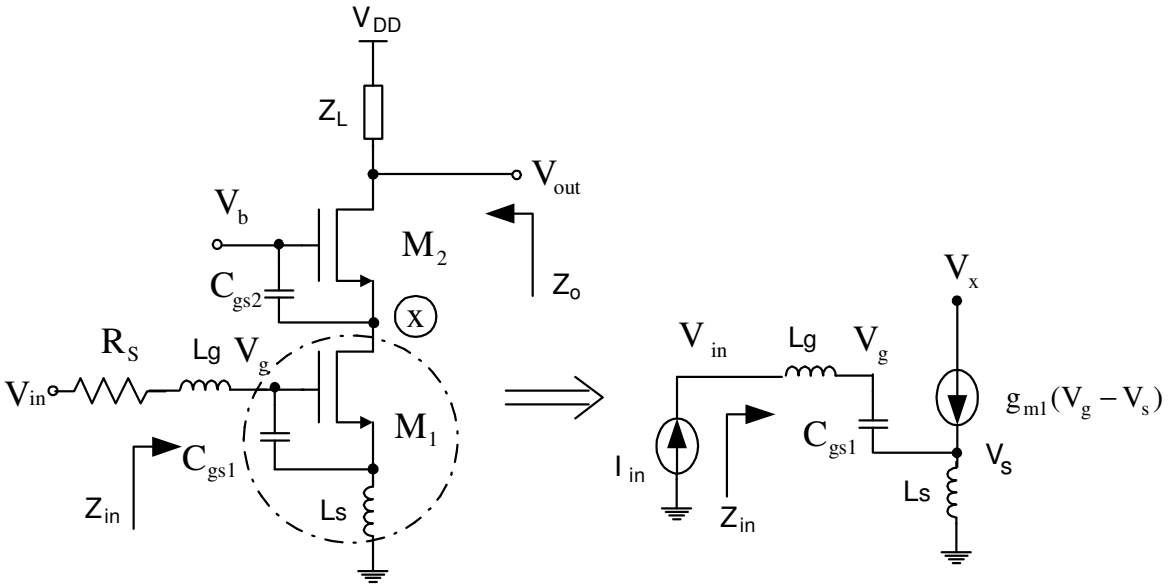
Fig. B.12 Simulated 1dB compression point of the LNA

APPENDIX C

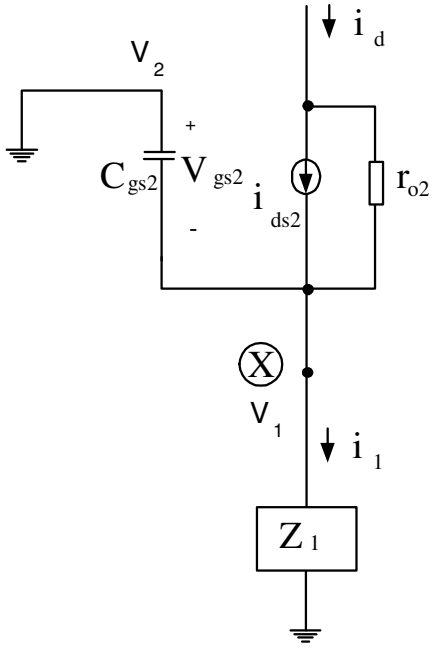
VOLTERRA ANALYSIS OF THE PROPOSED NOISE REDUCTION AND LINEARITY IMPROVEMENT LNA

Volterra series theory is widely used to analyze the nonlinearity of the frequency dependant circuits and systems.

The typical inductively degenerated CS-LNA is shown in Fig. 3.10. The analyzed cascode stage equivalent circuit is shown in Fig. C.1.



(a) (b)



(c)

Fig.C.1 (a) Inductively degenerated cascode CS-LNA (b) Equivalent small signal model of the LNA input network. (c) Analyzed cascode stage equivalent circuit

Here the Volterra series theory is applied to the cross-coupled cascode stage of the proposed CS-LNA in Fig. C.1

Applying KCL to the each node of the model in Fig.C.1, we can get

$$SC_{gs2}(V_2 - V_1) + i_d = SC_{gs2}V_{gs2} + i_d = i_1 \tag{C.1}$$

$$V_1 = i_1 \times Z_1 \tag{C.2}$$

i_1 is the input, and i_d is the output. We need to derive the relation between i_1 and i_d up to 3rd order

$$i_d = i_{ds2} = f(i_1) = c_1 i_1 + c_2 i_1^2 + c_3 i_1^3 \tag{C.3}$$

The drain currents M2 relation with the gate source voltage V_{gs2} in Fig.3.10 can be expressed up to 3rd order

$$i_{ds2} \approx g_m V_{gs2} + g_2 V_{gs2}^{\ 2} + g_3 V_{gs2}^{\ 3} \tag{C.4}$$

Assuming the relation between V_{gs2} and the input i_1 can be expressed up to 3rd order using Volterra series as

$$V_{gs2} \approx a_1(s) i_1 + a_2(s_1, s_2) i_1^{\ 2} + a_3(s_1, s_2, s_3) i_1^{\ 3} \tag{C.5}$$

where $a_1(s)$ is the first order coefficient term with one input frequency $a_2(s_1, s_2)$ is the second order coefficient term with two input frequencies and $a_3(s_1, s_2, s_3)$ is the third order coefficient term with three input frequencies. They represent the mixed nonlinear effect for multiple input frequencies. $a_1(s)$, $a_2(s_1, s_2)$ and $a_3(s_1, s_2, s_3)$ can be obtained by solving (C.1)-(C.5) by equating the same order tem of i_1 at both side of the equations.

Substituting (C.4) into (C.5), we can get

$$\begin{aligned} i_d \approx i_{ds2} \approx g_m a_1(s) i_1 &+ [g_1 a_2(s_1, s_2) + g_2 a_1(s_1) a_1(s_2)] i_1^{\ 2} \\ &+ [g_1 a_3(s_1, s_2, s_3) + 2 g_2 \overline{a_1(s_1) a_2(s_2, s_3)} + g_2 a_1(s_1) a_1(s_2) a_1(s_3)] i_1^{\ 3} \end{aligned} \tag{C.6}$$

where

$$\overline{a_1(s_1) a_2(s_2, s_3)} = \frac{1}{3}[a_1(s_1) a_2(s_2, s_3) + a_1(s_2) a_2(s_1, s_3) + a_1(s_3) a_2(s_1, s_2)] \tag{C.7}$$

Substituting (C.5), (C.6) into (C.1), we can get

$$\begin{aligned} &SC_{gs2}\left(a_1(s) i_1 + a_2(s_1, s_2) i_1^{\ 2} + a_3(s_1, s_2, s_3) i_1^{\ 3}\right) + g_m a_1(s) i_1 + \left(g_1 a_2(s_1, s_2) + g_2 a_1(s_1) a_1(s_2)\right) i_1^{\ 2} \\ &+ \left(g_1 a_3(s_1, s_2, s_3) + 2 g_2 \overline{a_1(s_1) a_2(s_2, s_3)} + g_2 a_1(s_1) a_1(s_2) a_1(s_3)\right) i_1^{\ 3} = i_1 \end{aligned} \tag{C.8}$$

For the harmonic input method, (C.8) needs to hold true for 1st order term, 2nd order term and 3rd order term. With a single input tone, $i_1 = e^{st}$, equating the coefficients of e^{st} of (C.8), we can get

$$a_1(s) = \frac{1}{g_m + sC_{gs2}} \tag{C.9}$$

Applying the two tones input, $i_1 = e^{s_1 t} + e^{s_2 t}$, to (C.8) and by equating the coefficient of the term $e^{(s_1+s_2)t}$, we can get

$$a_2(s) = -\frac{-g_2 a_1^2(s)}{g_m + sC_{gs2}} \tag{C.10}$$

Applying the three tones input, $i_1 = e^{s_1 t} + e^{s_2 t} + e^{s_3 t}$, to (C.8) and by equating the coefficient of $e^{(s_1+s_2+s_3)t}$, we can get

$$a_3(s) = -\frac{-2g_2 \overline{a_1(s_1)a_2(s_1,s_2)}}{g_m + sC_{gs2}} \tag{C.10}$$

Substituting (C.8)-(C.10) into (C.4), we can get

$$c_1(s) = g_1 a_1(s) \tag{C.11}$$

$$c_2(s) = g_1 a_2(s_1,s_2) + g_2 a_1(s_1)a_1(s_2) \tag{C.12}$$

$$c_3(s) = g_1 a_3(s_1,s_2,s_3) + 2g_2 \overline{a_1(s_1)a_2(s_2,s_3)} + g_2 a_1(s_1)a_1(s_2)a_1(s_3) \tag{C.13}$$

The third order intermodulation is the coefficient value when $s_1 = s_2 = s_a$ and $s_3 = -s_b$.

The A_{IIP3} of the cascode stage can be derived as

$$A_{IIP3}^2 = \frac{4}{3} \cdot \frac{1}{|H(\omega)| \cdot |a_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|} \tag{C.14}$$

$$g(\omega) = j\omega C_{gs2} \tag{C.15}$$

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - g_{oB} \tag{C.16}$$

$$g_{oB} = \frac{2}{3} g_2^2 [\frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)}] \tag{C.17}$$

$$H(\omega) = \frac{g(\omega)}{g_m} \tag{C.18}$$

For the cascode stage with the proposed technique shown in Fig.4.4, the analyzed cascode stage equivalent circuit is shown in Fig. 4.8.

Applying KCL to every node of the model in Fig.4.8,

$$SC_{gs2}(V_{2+} - V_{1+}) + i_{d+} + SC_c(V_{2-} - V_{1+}) = i_{1+} \tag{C.19}$$

$$SC_c(V_{1-} - V_{2+}) = SC_{gs2}(V_{2+} - V_{1+}) + sL_{add} V_{2+} \tag{C.20}$$

$$V_{1-} = -V_{1+} \tag{C.21}$$

$$V_{2-} = -V_{2+} \tag{C.22}$$

$$i_{1-} = -i_{1+} \tag{C.23}$$

$$i_{d-} = -i_{d+} \tag{C.24}$$

For the cascode stage with the proposed technique, we can get

$$i_d = i_1 - g'(\omega) \cdot V_{gs2} \tag{C.25}$$

$$g'(\omega) = \frac{4j\omega C_{gs2} \cdot j\omega C_c + \frac{1}{j\omega L_{add}}(j\omega C_{gs2} + j\omega C_c)}{2j\omega C_c + \frac{1}{j\omega L_{add}}} + \omega C_{sb2} + \omega C_{gd1} + \omega C_{db1} \tag{C.26}$$

Replacing (C.14) with (C.26), all the other results from (C.13) to (C.17) are still valid.

For the proposed technique, if (C.26) equals to zero, the current generated by M_1 will all flow to the output without nonlinearity degradation. It helps to improve the LNA linearity.

For the typical CS-LNA with a cascode transistor, the nonlinearity degradation can be evaluated by (C.14). From DC simulation, calculate the gate source capacitance C_{gs2}, the 1st order transconductance gm, the 2nd order nonlinearity term g2 and the 3rd order nonlinearity term g3. Calculate $g(\omega)$, g_{oB}, $\varepsilon(\Delta\omega,2\omega)$ and $H(\omega)$ using (C.15)-(C.18). Calculate the input 3rd order intermodulation using (C.14).

VITA

Xiaohua Fan received his B.S. from Tsinghua University and M.S. from Chinese Academy of Sciences in 1998 and 2001 respectively. He completed his Ph.D. degree under the supervision of Dr. Edgar Sánchez-Sinencio in the Analog and Mixed Signal Center, Electrical and Computer Engineering Department, Texas A&M University. From May 2005 to August 2005, Fan worked for Analog Devices in Wilmington, MA for his internship. From May 2006 to August 2006, Fan worked for Linear Technology in Colorado Springs, CO for his internship. Fan's research interests are focused on integrated radio frequency circuits design for wireless receiver. He held a Department of Electrical Engineering Fellowship in 2002, an Analog and Mixed Signal Fellowship in 2004 and 2005, and a Texas Instrument Excellent Fellowship in 2003 and 2006. He has been an IEEE student member since 2002.

He can be reached through the Department of Electrical and Computer Engineering Department, Texas A&M University, College Station, TX, 77843-3128. His email address is xhfan@ieee.org.

The typist for this thesis was Xiaohua Fan.