A LOW POWER LOW NOISE INSTRUMENTATION AMPLIFIER FOR ECG RECORDING APPLICATIONS

A Thesis

by

JESSE COULON

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2012

Major Subject: Electrical Engineering

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Approved by:

Co-Chairs of Committee,	Kamran Entesari
	Edgar Sanchez-Sinencio
Committee Members,	Aniruddha Datta
	Debjyoti Banerjee
Head of Department,	Costas N. Georghiades

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ABSTRACT

A Low Power Low Noise Instrumentation Amplifier for ECG Recording Applications.

(May 2012)

Jesse Coulon, B.Sc., Kwame Nkrumah University of Science and Technology

Co-Chairs of Advisory Committee: Dr. Kamran Entesari
Dr. Edgar Sanchez-Sinencio

The instrumentation amplifier (IA) is one of the crucial blocks in an electrocardiogram recording system. It is the first block in the analog front-end chain that processes the ECG signal from the human body and thus it defines some of the most important specifications of the ECG system like the noise and common mode rejection ratio (CMRR). The extremely low ECG signal bandwidth also makes it difficult to achieve a fully ECG recording integrated system.

In this thesis, a fully integrated IA topology is presented that achieves low noise levels and low power dissipation. The chopper stabilized technique is implemented together with an AC coupled amplifier to reduce the effect of flicker noise while eliminating the effect of the differential electrode offset (DEO). An ultra low power operational transconductance amplifier (OTA) is the only active power consuming block in the IA and so overall low power consumption is achieved. A new implementation of a large resistor using the T-network is presented which makes it easy to achieve a fully integrated solution. The proposed IA operates on a 2V supply and consumes a total

current of 1.4μA while achieving an integrated noise of 1.2μV_{rms} within the bandwidth. The proposed IA will relax the power and noise requirements of the analog-to-digital converter (ADC) that immediately follows it in the signal chain and thus reduce the cost and increase the lifetime of the recording device.

The proposed IA has been implemented in the ONSEMI 0.5μm CMOS technology.

DEDICATION

To my parents and my two little siblings, Gifty and Benjamin.

ACKNOWLEDGEMENTS

First of all, I would like to express my gratitude to the Lord Jesus Christ for granting me the strength and the knowledge to complete this work.

I would also like to thank my advisor and committee chair, Dr. Kamran Entesari, for his guidance and supervision throughout the period of my thesis work. Meeting with him on a weekly basis gave me invaluable insights into my research and analog circuit designing in general. I would also like to thank my committee members; Dr. Edgar Sanchez-Sinencio, Dr. Aniruddha Datta and Dr. Debjyoti Banerjee for their time and support.

I am indebted to Texas Instruments for sponsoring my Master's program. I am also grateful to my parents and siblings for their love, support and encouragement throughout the thick and thin. I also extend my appreciation to my church family in Dallas for the love and support during this time. I would also like to thank my friends, office colleagues and roommates for their support throughout my stay in College Station.

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1. INTRODUCTION

1.1 Background

Biopotential signal monitoring and recording is an important part of medical diagnosis and modern clinical practice requires these signals to be routinely recorded. It is usually the practice that patients are connected to cumbersome recording devices for the purpose of acquiring signals from the body to aid in diagnosis. This affects their mobility and causes general discomfort for them. Acquisition time reduces as a result of this and prevents the continuous monitoring of the patients which affects the general diagnosis of ailments [1].

Consequently, there has been the growing demand for low-noise and ultra low-power, miniature ambulatory biopotential acquisition devices. This has necessitated extensive research in the design of such interfaces and the eventual objective is to be able to design a biopotential miniature recording system that is comfortable, with long-term power autonomy, has high signal quality and can be configured to make it useful for many biomedical applications [1-7].

The design of such systems to monitor biopotential signals is challenging owing to the unique electrical properties of these signals. Typically, these signals have amplitudes ranging from a few tens of microvolts to a few millivolts. Again, depending on the type of biopotential signal that is to be monitored, it will have different frequency

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This thesis follows the style of the *IEEE Journal of Solid-State Circuits.*

bands from sub-hertz to a few hundred hertz and this makes it difficult to design one system for monitoring the different biopotential signals.

To be able to design a suitable system to monitor and record biopotential signals, the properties of the signal need to be clearly understood. Figure 1 [8] shows a diagram of the signal amplitudes and the frequencies of the various biopotential signals. These properties will be discussed in detail for electrocardiogram (ECG) systems which is the focus of this work. Electromyogram (EMG), electrocorticogram (ECoG), and electroencephalogram (EEG) are the other medical standards that are based on biopotential signals. Also shown in the plot in Figure 1 are the local field potentials and the action potentials.

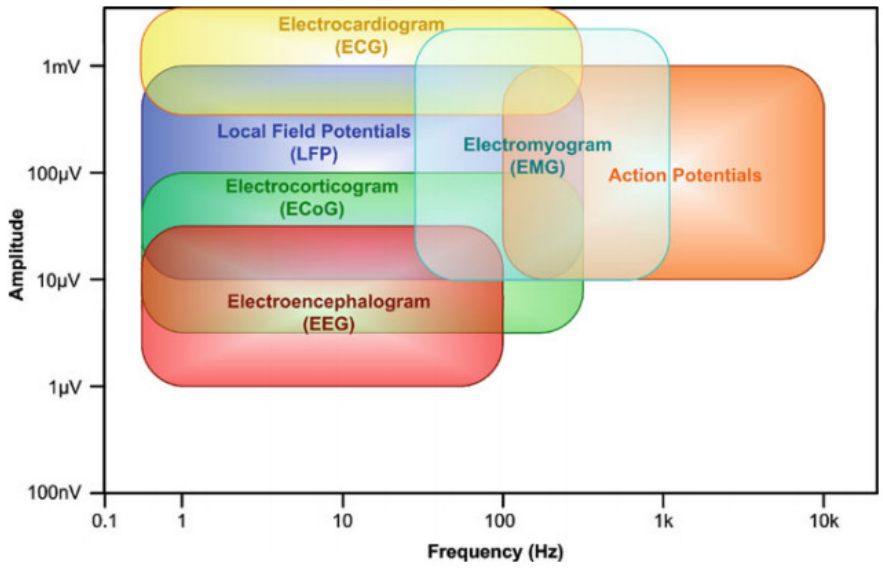

Figure 1 Properties of different biopotential signal

Electrocardiography is one of the most common types of biopotential signal monitoring. It essentially deals with the monitoring of human heart signals to determine heart related diseases. The holter monitors and the portable arrhythmia monitors are examples of portable devices that are used for monitoring the heart activity. These devices are unsuitable for long-term monitoring of the heart activity of a patient, albeit not very bulky. In the light of these conditions, fully integrated systems which have good power capability for long-term monitoring are desirable.

1.2 Overview of the ECG Monitoring System

Figure 2 shows a typical ECG monitoring system. It consists of the electrostatic discharge (ESD) and defibrillator protection, multiplexer (MUX), the front-end instrumentation amplifier (INAMP), the analog-to-digital converter (ADC), then subsequently a wireless transceiver.

In modern ECG systems, a defibrillator protection is implemented together with the ESD protection circuit before the analog front-end to enhance the safety of the patient, the user of the device and the device itself in the event of discharges and emergencies.

The multiplexer immediately after the ESD protection selects the channels to feed the instrumentation amplifiers.

Immediately after the MUX is the instrumentation amplifier (indicated INAMP in Figure 2). This amplifies the signal and filters out-of-band frequencies in the presence of very little noise. The skin-electrode interface also generates offset which also has a

potential to saturate the blocks in the signal chain if not dealt with. To alleviate this offset, the instrumentation amplifier is designed to have a high pass response to filter out

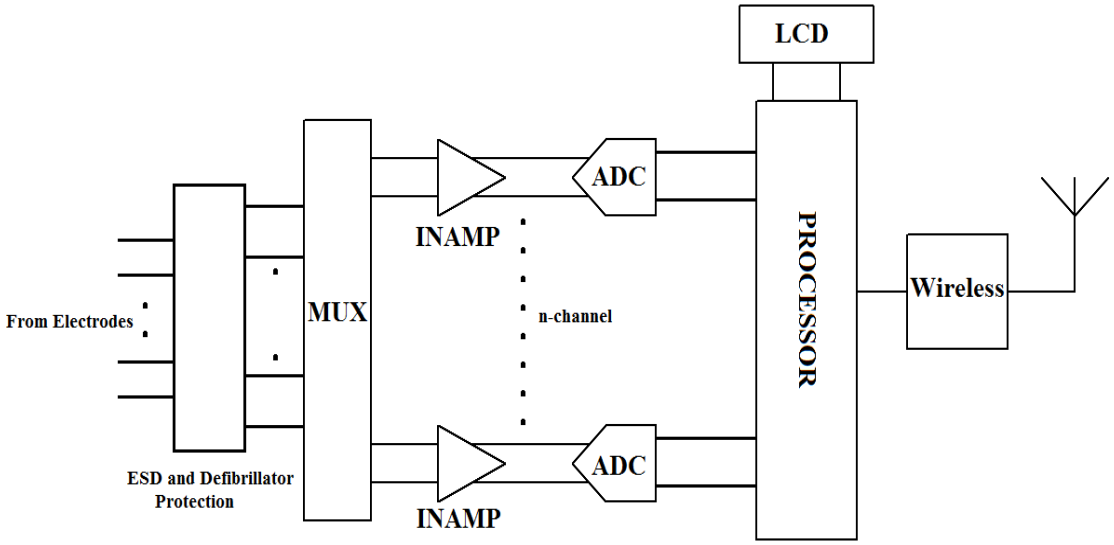

Figure 2 Block diagram of an ECG recording system

the DC offset. Interference due to electromagnetic fields, electrostatic fields and power mains are considered common mode signals and thus the instrumentation amplifier should be designed to have a high common mode rejection ratio (CMRR) to be able to reject as much of this common mode interference as possible. The low frequency nature of the ECG signal means the instrumentation amplifier should have very low flicker noise. The overall power consumption of the system is significantly dependent on the power consumption of this block and thus requires circuit techniques to reduce power as much as possible.

Next after the instrumentation amplifier is the ADC which digitizes the signal before it is transmitted. For an ECG with a maximum dynamic range of 60dB, a 10-bit ADC is required. A good choice for this resolution of the ADC and the low frequency sampling is the successive approximation ADC. This can be achieved while dissipating reasonably small amount of power.

The digitized data is then processed in a central processing unit, where the data is displayed through the LCD and/or transmitted to a base station where the data is received. This received data is analyzed by the physician to determine the condition of the patient.

1.3 Thesis Organization

This thesis describes the design of a low power low noise instrumentation amplifier for ECG recording applications. The challenge is to achieve low power dissipation, low noise and to have a fully integrated system with reasonably small capacitors. A simple chopped AC coupled topology is proposed to achieve the desired specification. A new implementation of large resistors is also proposed to make it easier to fully integrate the system in complementary metal-oxide semiconductor (CMOS) process.

Section 2 introduces the concept of electrocardiography. The section begins with defining electrocardiography and highlighting the historical background to it. The generation of the signal and its electrical properties are then discussed. The section closes with mentioning a few applications of ECG.

Section 3 discusses the details about designing biopotential instrumentation amplifiers. Key features of such amplifiers are mentioned. The noise considerations of such amplifiers are talked about subsequently. The section ends with discussing a few topologies of the instrumentation amplifier found in literature.

Section 4 talks about the proposed solution. It begins with stating the problem to be tackled and then talks about the architecture showing mathematical analysis and simulations results to justify the architecture.

Sections 5 talks about the actual transistor level design of the instrumentation amplifier. The design considerations for the various blocks are discussed and the design parameters are highlighted. The complete schematic is then presented.

Section 6 highlights the critical layout considerations and shows the layout of some individual blocks and the whole chip. The section also shows the final post layout simulation results and presents the comparison of results of this work to other state-of-the-art instrumentation amplifier performance.

Section 7 presents the conclusion of this thesis.

2. ELECTROCARDIOGRAPHY

2.1 Definition of Electrocardiogram

The electrocardiogram (ECG) or elektrocardiogram (EKG) is a medical standard for testing the human heart for defects and diseases [9]. It is a simple non-invasive method to record electrical activity of the heart. Together with clinical symptoms, electrocardiogram forms the initial diagnosis for most heart related diseases [10].

2.2 Background and History of Electrocardiography

The idea of studying effects of electricity on biological tissue dates back to 1786 when Luigi Galvani began some study into animal electricity. But it was Marey who in 1867 conducted the first electrical measurement from the heart. Augustus D. Waller later published the first recorded human ECG in 1887. Subsequently in 1893 Willem Einthoven introduced the term electrocardiogram, and then in 1912 invented the Einthoven triangle which formed the basis for most ECG recording systems [11]

Electrocardiography is the best way to measure and diagnose abnormal rhythms of the heart [12], particularly abnormal rhythms caused by damage to the conductive tissue that carries electrical signals or electrolyte imbalance [13]. In a myocardial infarction (MI), the ECG can identify damages in specific areas in the heart muscle, though not all areas of the heart are covered [14]. Other pathological conditions that can be seen in the ECG are hypocalcaemia, coronary ischemia, among others. These are

detected based on how the actual ECG signal from the body of the patient varies with the typical ECG signal [15]. The properties of the ECG signal will be discussed in the next section.

2.3 The ECG Signal and Its Properties

2.3.1 Generation of the ECG

The human heart consists of four compartments namely the left and right atria (upper chambers) and the left and right ventricles (lower chambers) as shown in Figure 3 [9]. The action of these chambers manages blood flow to and from the lungs and to the circulatory systems.

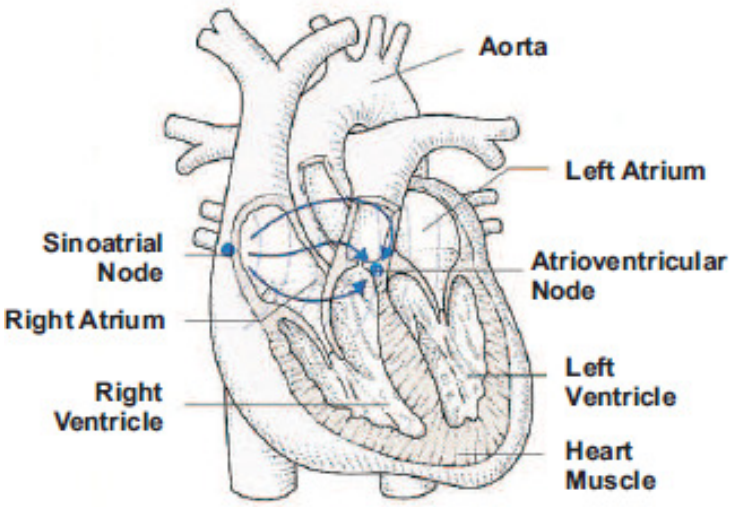

Figure 3 The human heart

The right atrium pumps blood to the right ventricle which provides blood to the lungs. Correspondingly, the left atrium pumps blood to the right ventricle and from there blood is pumped throughout the body [16].

The source of the human heart beat is an electrical pulse that is generated by a cluster of cells within the heart called the sinoatrial (SA) node or the pacemaker. The pulse from the pacemaker, which is generated at regular intervals, travels though the surrounding cells and the heart to the atrioventricular (AV) node. The AV node serves as the medium to allow the atria to complete contraction before the pulse moves to the ventricles [9]. As different heart cells are excited by these signals, they are depolarized thus resulting in a change in the cells chemical balance. The changes in the cells chemical balance can be translated into a voltage called the action potential. These periodic changes results in the ECG wave [16].

Generally, twelve leads are used to monitor cardiac signals with the most prevalent signal coming from the second lead [17]. A typical signal from the lead two is shown in Figure 4. The various segments of the signal and their sources are shown in Table 1.

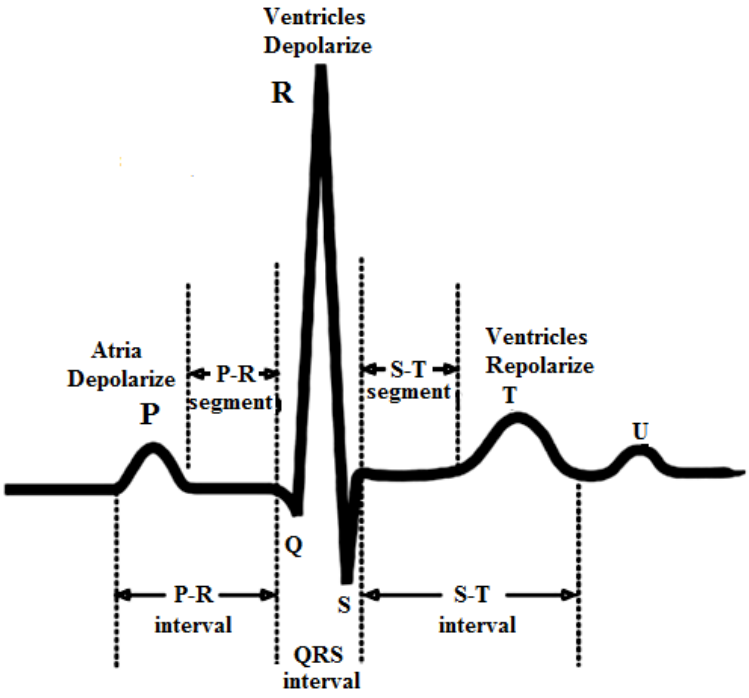

Figure 4 A typical ECG signal showing the various segments of the signal

Table 1 Sections of ECG signal and their sources.

Segment of ECG Signal	Source
P-Wave	Atria Depolarization
QRS-Complex	Atria repolarization and Ventricle depolarization
T-Wave	Ventricle repolarization
P-Q Interval	Depolarization timing delay

The ECG signal that comes from the body through the electrode is composed of three main components namely the actual differential ECG signal, the differential electrode offset (DEO) and the common mode signals [18].

The actual differential ECG signal has amplitudes ranging from about 100µV to 5mV and has frequencies ranging from about 0.1Hz to a little over 100Hz. These two properties of the ECG signal determine the dynamic range and bandwidth requirements of the analog front end [18].

The differential DC electrode offset which is inherent in the ECG signal results from the mismatch in the half cell potentials generated at the electrode skin interfaces. This offset voltage can be very large and so need to be eliminated to prevent saturation of the blocks in the signal chain. AC coupled systems [19] and current feedback techniques are some of the ways to reduce the effect of this DEO. Figure 5 shows an equivalent RC circuit at the skin-electrode interface and the half cell potential that give rise to the electrode offset.

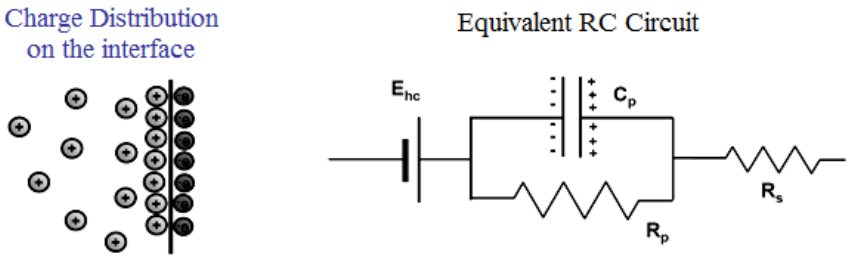

Figure 5 Charge distribution and equivalent RC circuit at electrode skin interface

- C_p and R_p represent the impedance associated with the electrode/electrolyte interface [8].
- E_{hc} is the half cell potential (HCP) resulting from the charge distribution in the electrode/electrolyte interface
- R_s is the resistance of electrolyte solution [1].

The mismatch between the HCPs at the two electrodes interfaces is the differential DC offset.

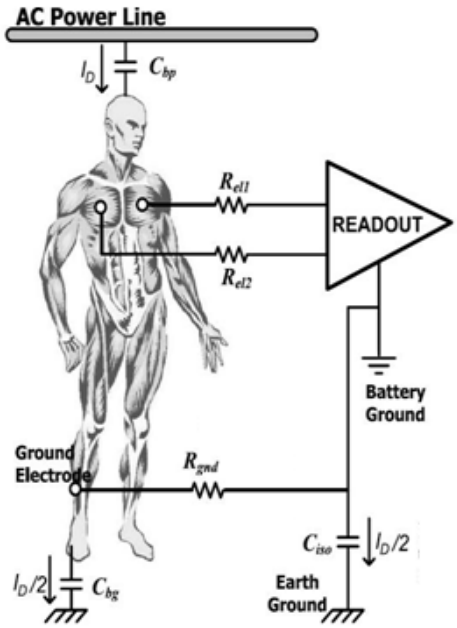

Figure 6 Sources of ECG signal errors and interference

Common mode signals which are picked up by the human body interfere with the ECG signals. Among these sources of common mode interference are signals from 60Hz power lines which are capacitively coupled to the body creating a displacement current which flows through body. This results in an AC common mode signal at the input of the front-end amplifier. Electromagnetic signals and electrostatic signals from other devices in the hospitals and homes induce EMF in the leads that connect the electrode to the input of the amplifier resulting in common mode signals at the input of the amplifier.

Differential systems with high CMRR help to significantly reduce this interference. The right leg drive is another way to cancel the common mode signals.

Figure 6 [1] shows a representation of the sources of interference and how they couple to the human body and the readout circuit. The 60Hz power line is capacitively coupled to the body through C_{bp} creating a displacement current which splits between C_{iso} and C_{bg} [8].

Thus the common mode voltage due to this displacement current is given by:

$$V_{CM} = \frac{I_D}{2} \times R_{gnd} \quad \textbf{(1)}$$

R_{gnd} is resistance connected from the amplifier ground to the right leg electrode.

This common mode that appears at the inputs of the amplifier is significantly reduced if a fully-differential amplifier is used. In some cases, inverting amplifier is connected from the common mode of the amplifier to the right leg to eliminate this common mode voltage [20].

However if there is mismatch between the two impedances R_{e1} and R_{e2}, a differential signals given by

$$\Delta V_{diff} = \frac{R_{e1} - R_{e2}}{R_{in}} \times V_{CM} \quad (2)$$

is amplified and appears at the output of the amplifier together with the amplified ECG signal [8]. Thus the amplified version of this differential signal interferes with the actual ECG differential signal. R_{in} is the input resistance of the amplifier.

2.3.2 Other Sources of Errors in the ECG Signal

Other sources of interference with the ECG signals are motion artifacts and pacer pulses. In particular involuntary muscle contractions of the muscle pectoralis major in the anterior chest wall can cause an artifact in the ECG that stimulates atria flutter. Proper positioning of the electrode can reduce these artifact [21]. These forms of interference need to be filtered either in the analog domain in the analog frontend or in the digital domain after the ADC [18].

2.4 Applications of ECG

ECG recording find applications in professional health care and consumer products. In professional healthcare, ECG is used in embedded systems like the ambulatory cardiac event recorders, ambulatory long-term monitoring devices, vital signs monitoring equipment, holter monitors, automated external defribrillators (AED),

and for general diagnostics [22]. In the consumer market, ECG systems are used in commercial fitness equipment, and some home health and wellness devices. Most treadmills used in the gyms have a heart rate monitor which records the heart signals by handgrip or wirelessly through a chest strap. In more recent applications, training shoes and iPods worn on the arms provide another means of monitoring the heart rate.

3. BIOPOTENTIAL INSTRUMENTATION AMPIFIERS

3.1 Introduction

The demand for long term power autonomy and high signal quality in biopotential recording devices puts strict design constraints on the analog front-end circuit. This makes the front-end instrumentation amplifier a very critical block in the whole biopotential acquisition system. Due to fact that it is the first block in the signal chain, it defines the noise level and the CMRR of the overall system [23]. It should also have a technique to filter the differential DC electrode offset. It is usually the most power consuming building block of the analog frontend [1] and the design efforts should be focused on keeping a good trade-off between noise and power.

3.1 General Properties and Design Challenges

The instrumentation amplifier acquires, amplifies and records the biopotential signal with very small noise and interference so that the subsequent blocks can process the acquired signal. As mentioned earlier, the ECG signal typically has amplitudes between 0.1mV – 5mV and are very low frequency as well (0.1-100Hz). Because of the nature of the signal, the dominant flicker (1/f) noise of MOS transistors will greatly limit the minimum detectable signal if not dealt with [24]. Furthermore, there is a problem of DC offset generated at the skin electrode interface [18]. Metal-oxide semiconductor (MOS) transistors also show poor input DC offset performance.

In addition to the above, the problem of common-mode interference due to 60Hz coupling correlate with the ECG signals. This even becomes more significant in wired systems.

In the light of these challenges, the biopotential amplifier should be designed to have the following characteristics [1]:

1. It should have high input impedance. The skin electrode interface has equivalent impedance which may be high within the bandwidth. To be able to transfer the ECG signal without any attenuation, the analog interface should have high input impedance.
2. It should have a high CMRR to reject common mode interference. This is typically achieved using a fully differential amplifier. However in most fully differential biopotential amplifiers, mismatches degrade the CMRR. In most recent publications, the current feedback approach has been used to greatly maximize the CMRR of the instrumentation amplifier.
3. It should have a high pass filtering characteristics to reduce the effect of differential electrode offset. This can be achieved using an AC coupled network [19] and in some cases, using a feedback to sense this offset and feeding it back to cancel the effect. The high pass characteristic requires a very low cut off frequency to pass the required signals while rejecting the DC offsets as well. This mostly requires very large capacitors and resistors to implement the large time-constant of this frequency making it difficult to achieve a fully integrated system.

4. It should achieve low-noise response for high signal quality. The chopper stabilized technique has been used in most instrumentation amplifiers to greatly reduce the flicker noise. But in some few cases, the autozeroing technique is used as well. These two techniques will be discussed later on this section.
5. It should be designed to have low power dissipation for longer battery life and enhanced continuous monitoring. This is usually achieved at the expense of noise. The design approach where transistors are designed to operate in weak and moderate inversion is suitable for low power designs.
6. It should have programmable gain and bandwidth to make it useable for different biopotential signals and different applications [1].

3.2 Noise Consideration in Instrumentation Amplifiers

The three main noise sources in instrumentation amplifiers are the flicker and thermal noise of the amplifier circuit itself, electromagnetic and electrostatic signals coupling through the cables and the human body, and the electrode noise.

Using shorter length of cables of the leads greatly minimizes the problem of noise coupling through cables. The coupling to human body can also be minimized by designing a high CMRR instrumentation amplifier.

The electrode impedance by itself will generate some noise which corrupts the signal being detected. The type of electrode used, its chemical makeup and the surface of

the human body determine the value of this impedance and the noise voltage it produces [8].

The circuit noise consists of the thermal noise and flicker noise. The thermal noise is defined by the transconductance of the amplifier. For a large *gm,* a lower noise voltage is obtained. The flicker noise is more dependent on process. Increasing the gate area reduces the flicker noise [25]. To have a good signal-to-noise ratio (SNR), the 1/f noise component which is the most significant noise component in biopotential instrumentation amplifiers must be lower than the smallest signal of interest [8]. For this reason most topologies used in such instrumentation amplifiers employ additional techniques to deal with the noise.

In the design of instrumentation amplifiers, the target is to achieve both low noise and low power characteristics. But usually it is difficult to achieve both. The trade-off between noise and power plays an important role in the design of such blocks and the aim of modern biopotential amplifiers is to increase the noise efficiency factor (NEF) which quantifies the power efficiency in terms of noise [26]. The NEF describes how many times the noise of a system with the same total current and bandwidth is higher compared to the ideal case.

The NEF of an amplifier with a 3-dB Bandwidth of *BW* and input referred noise voltage $V_{in,rms}$ is given by:

$$\mathrm{NEF}=\mathrm{V_{in,rms}}\sqrt{\frac{2\times\mathrm{I_{tot}}}{\pi\times\mathrm{V_t}\times 4\mathrm{kT}\times\mathrm{BW}}} \qquad \textbf{(3)}$$

I_{tot} is the total current used in the amplifier, V_t is the thermal voltage of the transistor, k is the Boltzmann's constant and T is the absolute temperature.

A lower value of NEF means that for a given noise level the amplifier can achieve a lower power dissipation [8].

3.3 Noise and Offset Reduction Techniques in Instrumentation Amplifiers

3.3.1 The Chopper Stabilization Technique

Chopper stabilization is a technique used to minimize the effect of flicker noise and offset. It uses the principle of modulation and demodulation to shift the low frequency flicker noise band and DC offset to higher frequency in a manner such that, applying a filter subsequently attenuates the effect of the flicker noise and the input offset of the amplifier.

Unlike the sampling techniques discussed later in the section, chopping works by multiplying the noise by a square wave and thus produces harmonics of the noise spectrum at odd multiples of the chopping frequency.

The operation of the chopper stabilization technique as applied to amplifiers is described in Figure 7. To prevent aliasing the bandwidth of the signal must be smaller than one half of the chopping frequency [1]. For an input signal, $x(t)$ applied to a chopper amplifier, the signal is first modulated using a square wave, $m(t)$ having a frequency of f_{chop}. This results in a frequency spectrum with the input signal $X(f)$ shifted

to the odd harmonics of the chopping frequency. The up-converted input signal and the 1/f noise *N(f)* are then amplified. At the output of the amplifier, the amplified version of

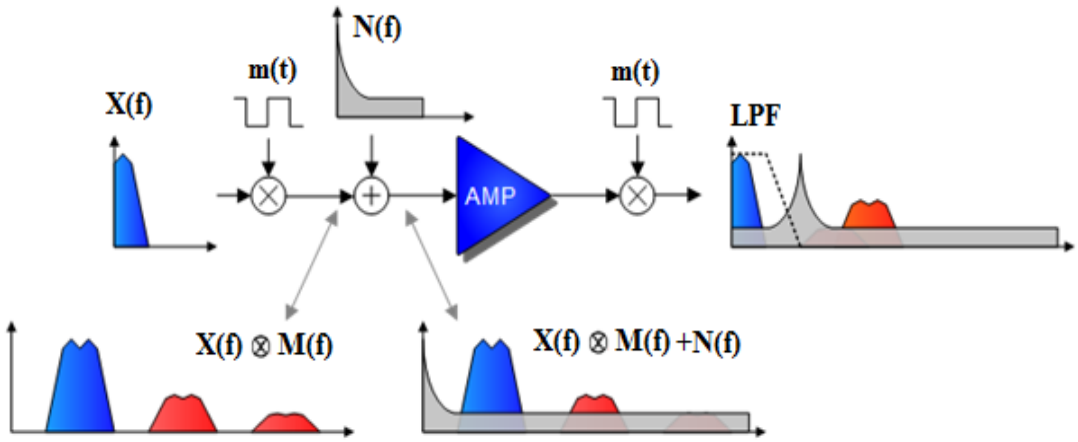

Figure 7 The chopping operation as applied to an amplifier

X(f) is demodulated with *m(t)* while the 1/f noise is modulated. Replicas of the amplified input signal as well as the 1/f noise remain at odd harmonics of f_{chop}. These unwanted signals can be filtered by a low pass filter (LPF). By this DC offsets and flicker noise can be greatly reduced in the amplifier [27].

The following shows the mathematical concept of the chopper amplifiers [28]. The modulation signal *m(t)* can be expanded in a fourier series as follows:

$$m(t) = \frac{2}{j\pi} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n} \exp\left(\frac{j2\pi nt}{T}\right) \quad \textbf{(4)}$$

with an equivalent frequency transform given by:

$$|M(f)|^2 = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \delta\left(f - \frac{n}{T}\right) \quad \textbf{(5)}$$

For a random input signal, *x(t)* that is amplified by a gain of *A(f)* and chopped by *m(t)*, the resulting power spectral density at the output is obtained by convolving the amplified random signal and chopping signal as follows:

$$S_{yy}(f) = [S_{xx}(f)\ |A(f)|^2\ ] \otimes |M(f)|^2 \quad \textbf{(6)}$$

Substituting *M(f)* into the above:

$$S_{yy}(f) = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \left|A\left(f - \frac{n}{T}\right)\right|^2 S_{xx}\left(f - \frac{n}{T}\right) \quad \textbf{(7)}$$

- ***Effect of Chopping on White Noise***

For an amplifier with a first order response given by:

$$A(f) = \frac{1}{1 + j\frac{f}{f_o}} \quad \textbf{(8)}$$

The power spectral density of the noise at the output, where

$$S_{xx}(f) = S_{white} \quad \textbf{(9)}$$

is given by:

$$S_{yy}(f) = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \frac{S_{white}}{1 + \left(\frac{fT - n}{f_o T}\right)^2} \tag{10}$$

Simplifying using the Poisson summation [29] results in

$$S_{yy}(f) \approx S_{white} \quad \text{for } f_o T \gg 1 \tag{11}$$

Thus for bandwidth of the amplifier greater than the chopping frequency, chopping has very little influence on the white noise.

- ***Effect of Chopping on Flicker Noise***

For flicker noise,

$$S_{xx}(f) = \frac{c}{f} \tag{12}$$

where *c* is a constant that depends on process and the dimensions of the transistors.

The power spectral density at the output after chopping will thus be:

$$S_{xx}(f) = \frac{c}{f} \tag{13}$$

$$S_{yy}(f) = cT \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \frac{1}{|fT - n|} \frac{1}{\left[1 + \left(\frac{fT - n}{f_o T}\right)^2\right]} \tag{14}$$

For $f_o T$ greater than 1, the power spectral density is greatly reduced at low frequencies.

The effect of chopping on the flicker noise is the same effect it has on the input referred offset voltage of the amplifier and thus the offset of chopper amplifiers is also reduced by chopping.

Chopping is beneficial in reducing flicker noise but it has one key drawback. For a chopper stabilized amplifier in closed loop, the input voltage will exhibit residual offset which is mainly from clock skew in the chopper clocks and parasitic capacitance imbalance in the choppers [30].

3.3.2 The Principle of Autozeroing

Autozeroing is a principle that is used to reduce the effect of offset and noise in amplifiers. It generally consist of two phases; the storage phase, during which the offset or noise voltage is estimated and stored on a capacitor and the cancellation phase, during which the signal is amplified and the offset or noise is subtracted from the signal [31].

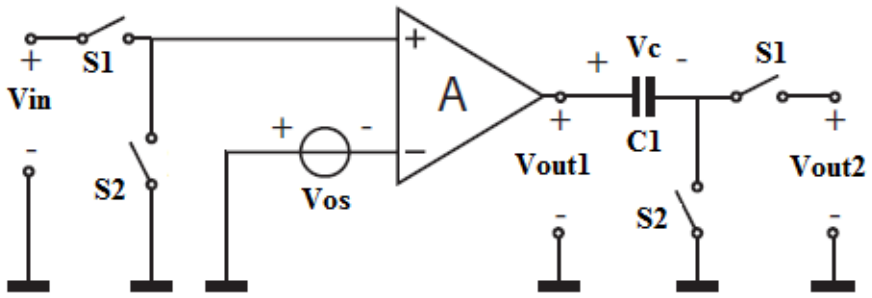

Figure 8 Schematic of autozeroing technique with output offset storage

Two ways to implement the storage phase of the autozero technique are the output offset storage and the input offset storage [31].

In Figure 8 [31], capacitor C_1 is used to store the output referred offset in one clock phase and subtract it from the signal in the second clock phase. This is called the open-loop offset cancellation [27].

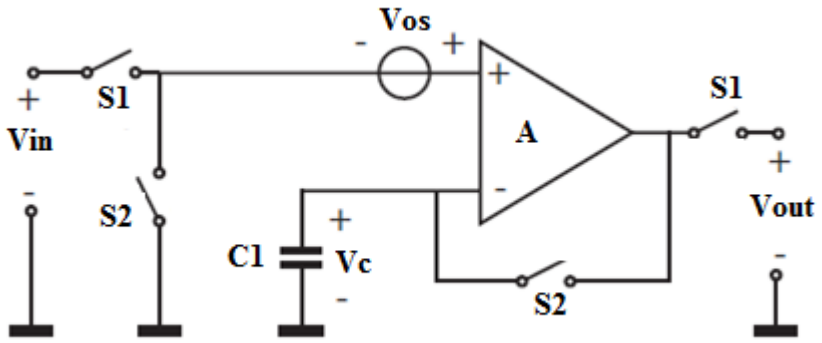

Figure 9 Schematic of autozeroing technique with input offset storage

Figure 9 [31] shows a simple schematic of the autozero technique with input offset storage. This is also called the closed loop offset cancellation [27] and it is the more common approach used in instrumentation amplifiers for biomedical application.

In the sampling phase, the voltage that is stored on capacitor C_1 is given by

$$V_c = \frac{A}{A+1} V_{os} \quad \textbf{(15)}$$

During the subtraction or cancellation phase the net output voltage is given by

$$V_{out} = \left(V_{in} + \frac{1}{A+1} V_{os} \right) A \quad \textbf{(16)}$$

For a high gain amplifier, the effect due to the offset is almost zero.

The autozeroing approach has the same effect on the 1/f noise as it has on the input offset.

The effect of autozeroing on thermal noise is however different. The under-sampling of thermal noise results in noise folding and so in essence the autozero techniques improves DC offset and flicker noise at the expense of higher thermal noise at baseband frequencies [32].

Besides the issue of noise folding, autozero technique also suffers from residual offset due to charge injection when using MOS switches. Mismatches in the switches causes a significant increase in the residual offset and thus a compensation of the increase in the autozero capacitor is required which is not always desirable.

A third method that has been used to deal with the 1/f noise, is the correlated double sampling (CDS) [32]. This method also uses sample and hold circuitry to estimate and subtract the sampled noise from the input signal so that ideally, the output will be free of the offset voltage and the low frequency noise. This suffers from the problem of noise fold over as in the autozero technique.

3.4 Existing Instrumentation Amplifier Topologies

A well known topology of biopotential amplifiers is the three operational amplifier (opamp) instrumentation amplifiers [33-35] shown in Figure 10. This topology has a high input impedance, and the gain of the system is obtained from the ratio of the feedback resistors [35]. The CMRR of this topology depends on the matching of the resistors [36]. In standard CMOS technology, the matching of resistors can be made accurate by laser trimming but this is expensive. This topology is simple to implement but not very efficient in low noise and low power applications. On the other hand, an additional circuitry is required for the DC electrode offset elimination and a low pass filter to define the high cut-off frequency. This further increases the power and complexity of the circuit as well. Also the three opamps required results in high power dissipation in this topology.

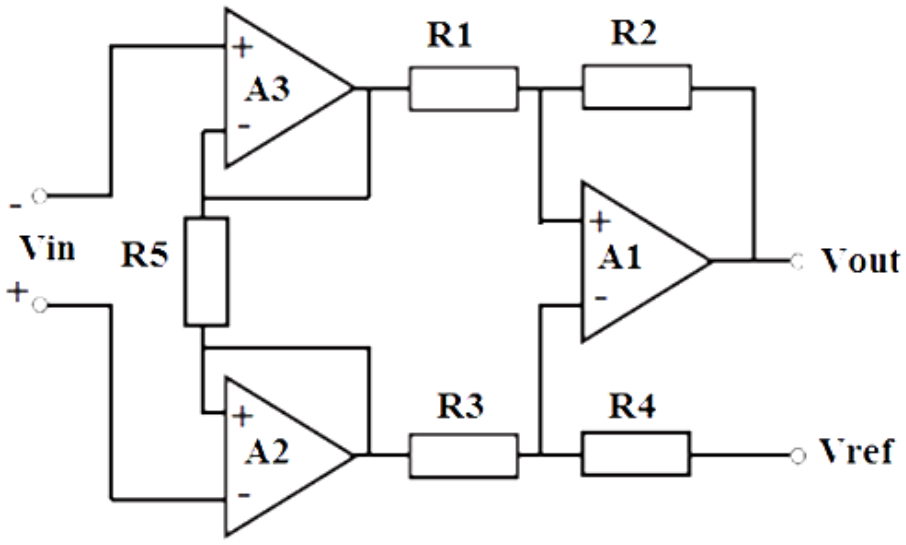

Figure 10 The schematic of the three opamp instrumentation amplifier

Another topology of instrumentation amplifiers is based on switched-capacitor (SC) circuits shown in Figure 11 [37]. The SC amplifier architectures have an inherent autozero mechanism and thus capable of eliminating the 1/f noise of the CMOS amplifiers. It however suffer from noise fold-over above the Nyquist frequency [27]. This results in a significant increase in the thermal noise level. To be able to still achieve good noise performance for the SC amplifiers, more power has to be dissipated. Hence the SC instrumentation amplifier topology is not power efficient approach for low noise systems. It also has reduced input impedance due to the sampling mechanism at the input of the amplifier.

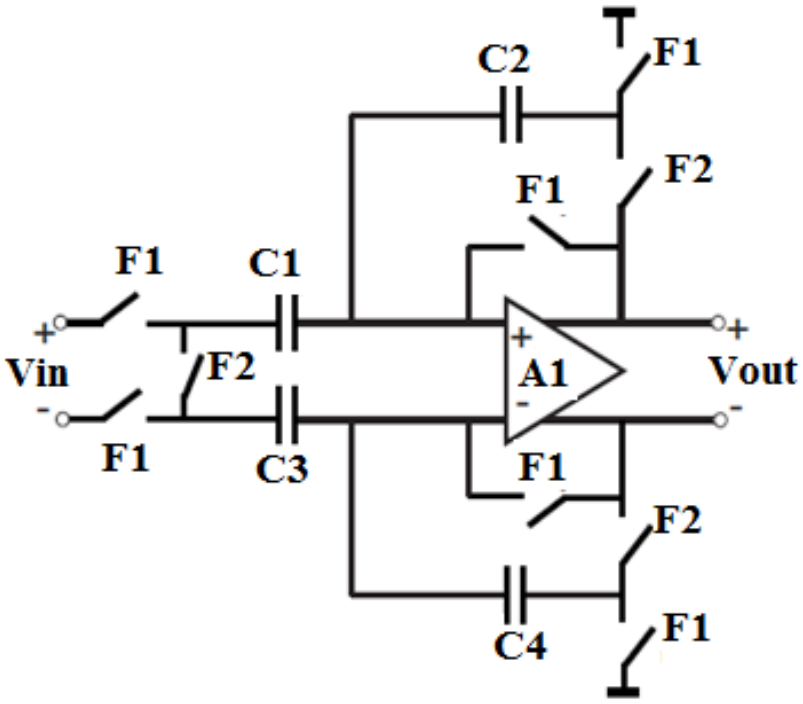

Figure 11 The schematic of a switched capacitor instrumentation amplifier

The current balancing (current feedback) instrumentation amplifier (CBIA) [38-40] is another topology for implementing biopotential IAs. In this topology, the ratio of two resistors, R_1 and R_2 is the overall gain of the instrumentation amplifier as shown in Figure 12. This topology eliminates the stringent need for matched resistors for high CMRR and the need for low output impedance [1]. Thus very high CMRR can be achieved with this implementation. This implementation is different from the conventional current-mode open-loop instrumentation amplifier because it has a feedback current, I_1 flowing through R_1 rather than the input buffers. In this way, the currents of the input buffers are balanced by the current from the feedback and so the buffers are essentially only buffering the input [8]. Unlike the open loop current-mode instrumentation amplifiers, R_1 is not limited by the output resistance of the input stage and this becomes important for low noise applications [41]. Power consumption is however high in CBIAs.

In [39], a low noise amplifier is proposed which implements the CBIA and chopping modulation [27] to reduce the 1/f noise of the noise of the system. This system is however not fully integrated since very large capacitors are required in the implementation which is not feasible in most CMOS processes.

In [19], a biopotential amplifier is designed with capacitive coupled network to reject the DC electrode offset. This has been employed in different other works. This provides a simple topology to achieve the desired frequency response as well as the input impedance required for recording biopotential signals. The ratio of capacitors determines the gain of the system. It has the advantage of an extremely low power

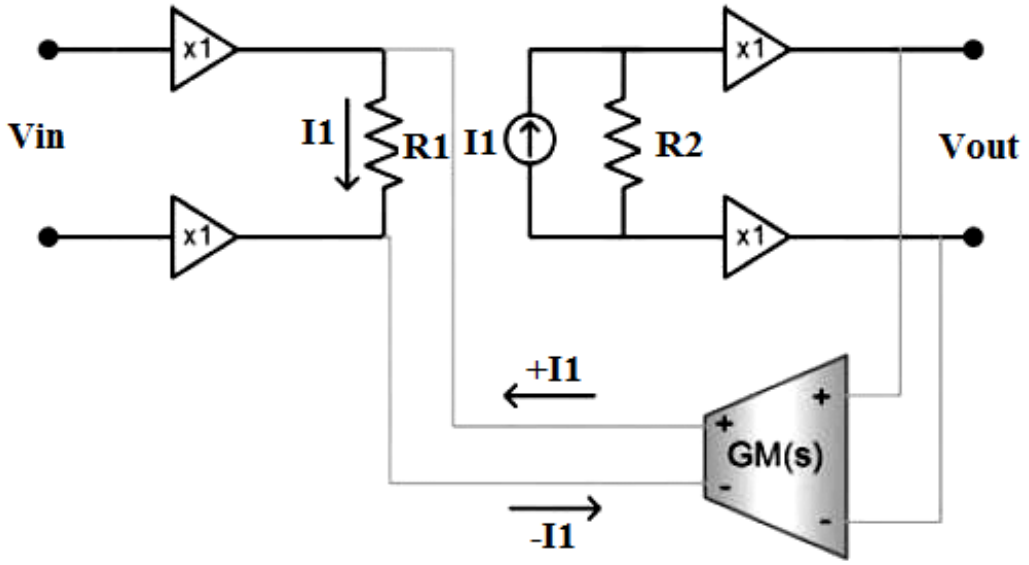

Figure 12 The schematic of a current feedback instrumentation amplifier

dissipation because it only requires a simple amplifier which can be designed for low power applications. Also a pseudo resistive network is implemented with MOS to have a large resistance and hence relaxes the constraint on the size of the capacitors and so makes it easy to fully integrate the amplifier. However the disadvantage of this topology is the very high noise response because no additional circuitry is implemented to reduce the flicker noise.

In [42] an instrumentation amplifier is proposed for the front-end of an EEG system. This system implements a chopper stabilized low noise amplifier. The chopping at the virtual nodes of the amplifier results in a parasitic resistance which reduces the overall input impedance of the amplifier. This effect is corrected by a feedback which uses an OTA and a capacitor and resistor. This system requires a low pass filter to limit

the bandwidth to the desired frequency. The front-end is low power and low noise. It is however not fully integrated since the capacitors required are not achievable in CMOS processes.

4. PROPOSED SOLUTION

4.1 Definition of Problem

In section 3, the noise-power trade off in instrumentation amplifiers was discussed. In many of the publications on this subject, emphasis is placed on one of these parameters (noise and power dissipation), while the other is minimized as much as possible. However the demand for low power and low noise ECG systems is the driving force of research recently.

Also the need for a fully integrated system that can adequately cover the entire frequency band of an ECG signal is desired. This requires large resistors and capacitors to implement the large time-constant for the high pass characteristic. A number of ways to implement large resistors has been proposed but most of these still require a large capacitor to be integrated in addition to realize this time constant.

The problem is to design a fully integrated ECG instrumentation amplifier which achieves both low noise for enhanced signal detection and low power for continuous monitoring.

4.2 Architecture

In this work, the chopper stabilized technique is used together with the AC coupled technique to achieve overall better performance. The objective is to achieve the

desirable features of the two techniques while dealing with the issues of combining the two techniques.

The configuration in Figure 13 shows a chopper stabilized operational transconductance amplifier (OTA) with an AC coupled feedback system which has a band pass response desired for such systems. The ratio of the input and feedback capacitor provides the mid-band gain for the system. The input capacitors eliminate the effect of the differential electrode offset that is inherent in the biopotential signal.

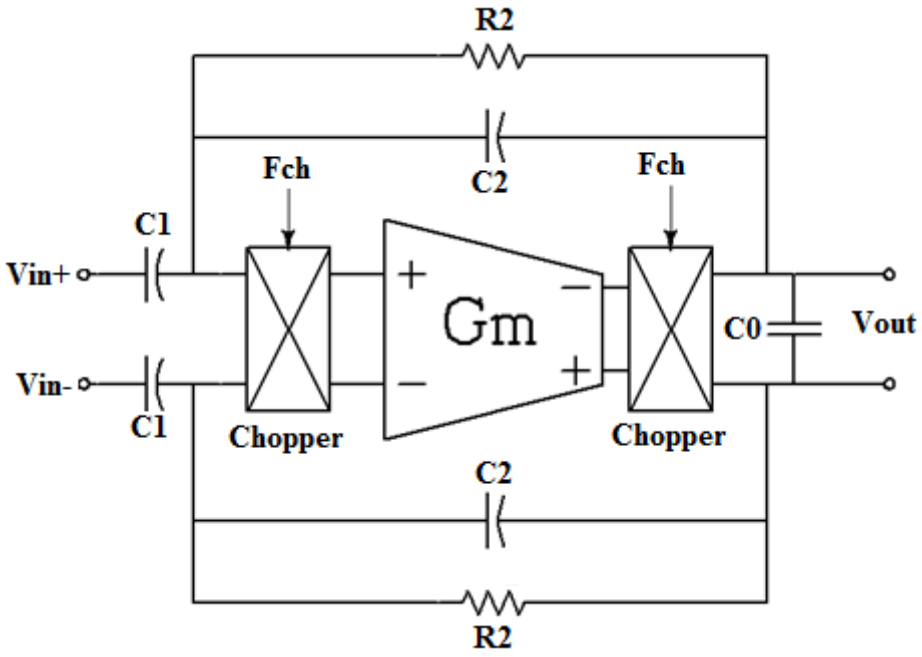

Figure 13 Block diagram of the proposed architecture

The resistor R_2 and capacitor C_2 combine to determine the low cut off frequency, whereas the transconductance of the OTA, the mid-band gain and the output capacitance

together determine the high cut off frequency. An OTA is used instead of an opamp to eliminate the need of an additional filtering stage at the output of the second chopper. In this way the output chopper operates on the output current of the OTA before this current is integrated by the output capacitor. This topology has the advantage of lower power, lower noise and ease of design since the OTA is the only active block.

In the topology used in [19], the input impedance of the system is very high and that is one key requirement of any instrumentation amplifier. In the case of the proposed system, the chopping at the virtual ground nodes of the OTA generates a parasitic resistor which is not desirable. The equivalent circuit for the parasitic resistor is shown in Figure 14. This resistor acts in parallel with the input impedance of the OTA to reduce its overall input impedance.

The lower this resistance, the lower the overall input impedance and hence the more the system deviates from ideal behavior. System level derivations and analysis further discusses this problem and the proposed solution.

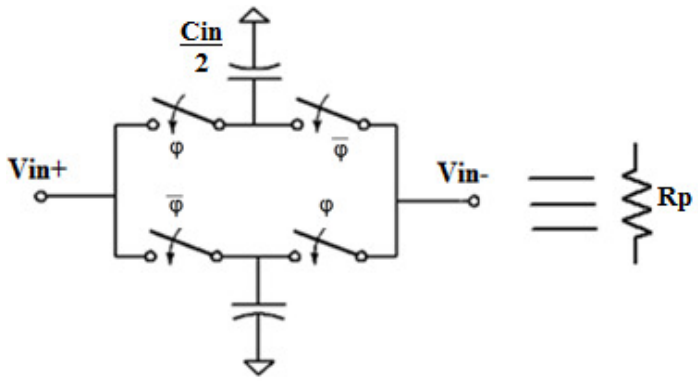

Figure 14 The switched capacitor resistor

Also in this work, a new implementation of the large resistor R_2 using the T-network [43] with pseudo resistors is proposed. This relaxes the constraint of having a high parasitic resistance to achieve desired performance and makes it easier to achieve a fully integrated solution on chip.

The CMRR of this topology is mainly determined by the proper matching of the two input and two feedback capacitors. There is systemic common mode gain that is also inherent in the topology. The common mode rejection (CMR) is defined as the ratio of the differential voltage at the output of the amplifier due to common mode input signal to the common mode signal itself.

Chopping at the virtual node of the OTA has a drawback of the reduced CMRR [42] since a small mismatch in the input capacitors can result in the common mode signal appearing as a large differential signal at the output.

4.3 Justification for the Architecture

4.3.1 Frequency Response and Noise Analysis of the Topology

Figure 15 shows a single-ended equivalent circuit of the proposed architecture. R_p is used to represent the parasitic resistor from the switched capacitor effect at the virtual node of the OTA. Figure 16 is a mathematical model of the single-ended to analyze the frequency response and noise of the architecture. The mathematical model shows the ideal transfer function in the block diagram from the summing node (the non-inverting terminal) to the output.

This ideal transfer function is given by:

$$T(f) = \frac{1}{C_1\left(s + \frac{1}{R_p C_1}\right)\left(s + \frac{G_m}{C_{out}}\right)} \quad \textbf{(17)}$$

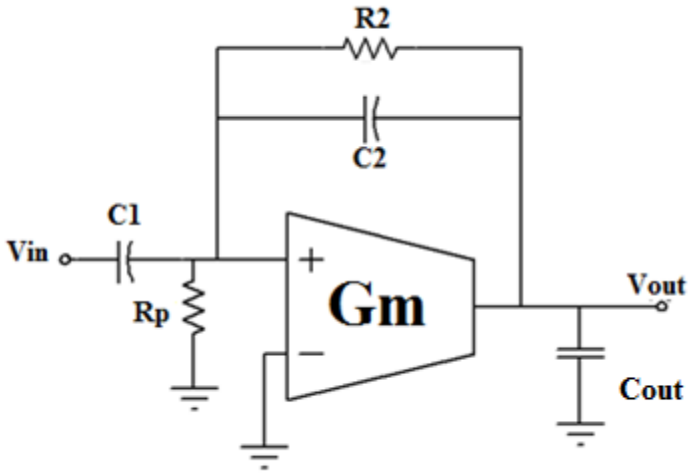

Figure 15 Single-ended version with the switched capacitor resistor

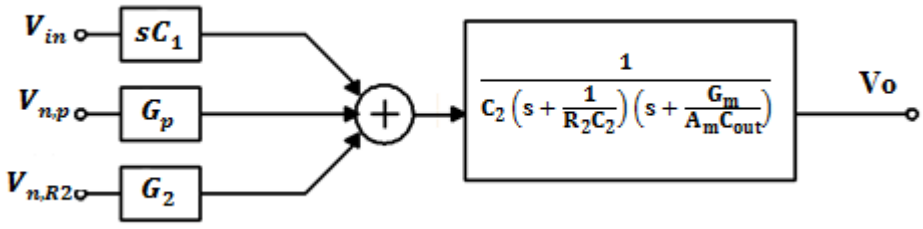

Figure 16 Model to analyze the system for stability and noise

- ***Loop Gain***

The loop gain of the system is obtained by multiplying the feedback factor by the open loop gain. This is given by:

$$LG(s) = \frac{A_{ol}\left(s + \frac{1}{R_2C_2}\right)\left(s + \frac{G_m}{A_mC_{out}}\right)}{C_1\left(s + \frac{1}{R_pC_1}\right)\left(s + \frac{G_m}{C_{out}}\right)} \quad \textbf{(18)}$$

A_{ol} is the open loop gain which is simply the DC gain of the OTA which is given by:

$$A_{ol} = G_m R_{out} \quad \textbf{(19)}$$

The overall transfer system transfer function is obtained from a general closed loop system as:

$$H(s) = \frac{A_{ol}}{1 + LG(s)} \quad \textbf{(20)}$$

Substituting (17) and (18) into (19) results in the closed loop transfer function given by:

$$H(s) = \frac{A_m s}{\left(s + \frac{1}{R_2C_2}\right)\left(s + \frac{G_m}{A_mC_{out}}\right)} \quad \textbf{(21)}$$

A_m is the midband gain of the closed loop transfer function given by:

$$A_m = \frac{C_1}{C_2} \quad \textbf{(22)}$$

The closed loop response has low cut-off frequency *(ω_{LCF})* and high cut-off frequency *(ω_{HCF})* located at:

$$\omega_{LCF} = \frac{1}{R_2 C_2} \tag{23}$$

$$\omega_{HCF} = \frac{G_m}{A_m C_{out}} \tag{24}$$

- ***Noise Transfer Functions***

1. Resistors

The noise of the parasitic resistor and feedback resistor are analyzed in a similar way using the model in Figure 16. The noise transfer function is obtained by multiplying the noise voltage and the ideal transfer function in equation 17.

The noise transfer function of the feedback resistor is given by:

$$H_{n,R2} = \frac{s}{C_2 R_2 \left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{G_m}{A_m C_{out}}\right)} \tag{25}$$

The noise spectral density at the output is obtained by multiplying the noise transfer function by the noise power due to R2, v^2_{n2}.

$$S_{R2}(f) = v_{n2}^2 \left(\frac{s}{C_2 R_2 \left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{G_m}{A_m C_{out}}\right)} \right)^2 \tag{26}$$

The input referred noise spectral density is found by dividing equation 26 by the square of the ideal transfer function from the summing node to the output.

$$S_{R2,input}(f) = v_{n2}^2 \left(\frac{1}{sC_2R_2}\right)^2 \quad \textbf{27}$$

Similarly, the input referred noise spectral density of Rp is given by

$$S_{Rp,input}(f) = v_{np}^2 \left(\frac{1}{sC_2R_2}\right)^2 \quad \textbf{28}$$

The noise is inversely proportional to the value of the resistance. This makes the noise of R_p is significantly larger than that of R_2.

2. OTA

This is the biggest contributor of noise in the system. The flicker noise of the OTA is significantly reduced by the chopping operation. The noise is thus modeled as white noise as follows;

The noise transfer function is:

$$H_{n,Gm} = \frac{sA_m\left(s+\frac{1}{R_pC_1}\right)}{R_x\left(s+\frac{1}{RC_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)} \quad \textbf{(29)}$$

The noise spectral density at the output is thus given by:

$$S_{Gm} = \left(\frac{sA_m\left(s+\frac{1}{R_pC_1}\right)}{R_x\left(s+\frac{1}{RC_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)}\right) v_{n,Gm}^2 \quad \textbf{(30)}$$

where $v_{n,GM}$ is the noise power of the OTA

The input referred spectral noise density is thus given by:

$$S_{Gm,input} = \left(\frac{s + \frac{1}{R_p C_1}}{s} \right)^2 v_{n,Gm}^2 \quad \textbf{(31)}$$

The white noise of the OTA is shaped by the transfer function above. The shaping effect is minimized by choosing $\frac{1}{R_p C_1}$ to be smaller than frequency band of interest.

4.3.2 Simulation Results from Mathematical Model

The transfer function for the proposed instrumentation amplifier is given by:

$$\frac{V_o}{V_{in}} = \frac{sC_1}{\left[\frac{s^2 C_{out}}{G_m}(C_1 + C_2) - s\left(\frac{C_{out}}{G_m}\left(\frac{1}{R_p} + \frac{1}{R_2} \right) + C_2 \right) - G_2 \right]} \quad \textbf{(32)}$$

For an infinite value of R_p, the ideal transfer function is given by:

$$\frac{V_o}{V_{in}} = \frac{C_1 s}{C_2 \left(s + \frac{1}{R_2 C_2} \right)\left(s + \frac{C_2 G_m}{C_1 C_{out}} \right)} \quad \textbf{(33)}$$

This transfer function is plotted in MATLAB for different values of the parasitic resistance and the feedback resistance.

In the simulation, the mid-band gain (given by the ratio of C_1 and C_2) is chosen to be 40dB. C_1 and C_2 are chosen to be 20pF and 200fF respectively to be able integrate in CMOS process. C_{out} is chosen to be 20pF and the G_m is chosen accordingly to obtain low pass bandwidth of 100Hz.

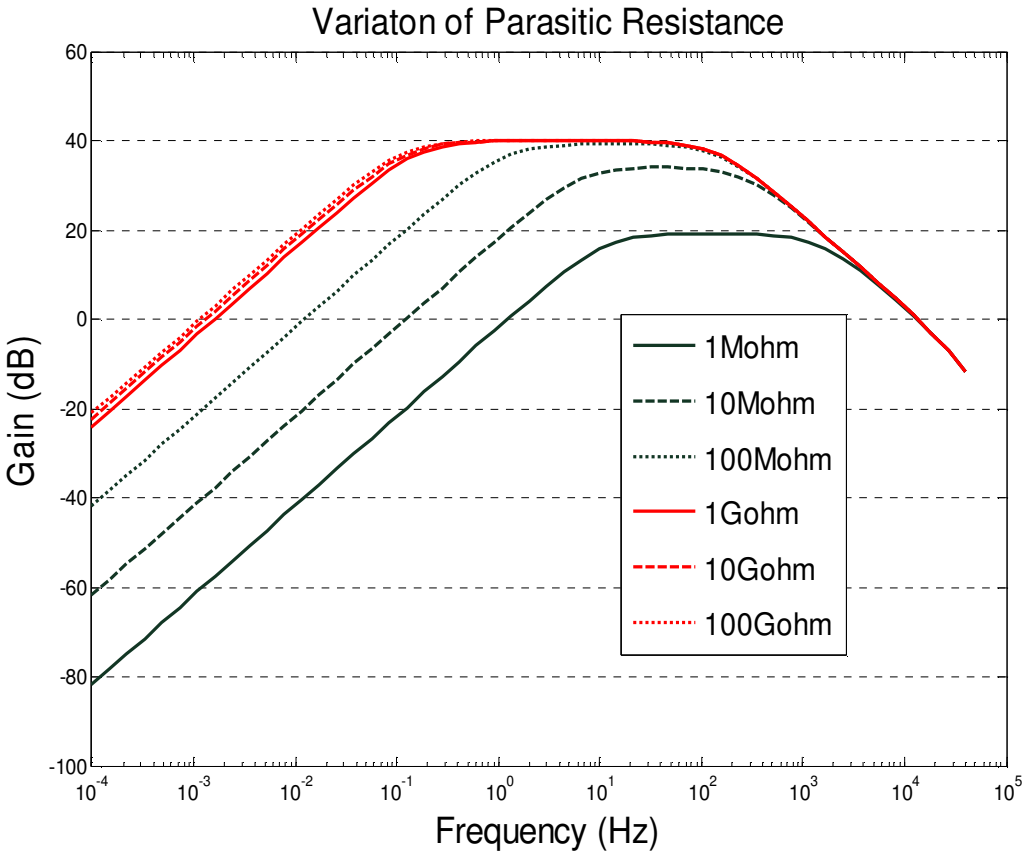

Figure 17 Frequency response of the IA for different values of the parasitic resistance

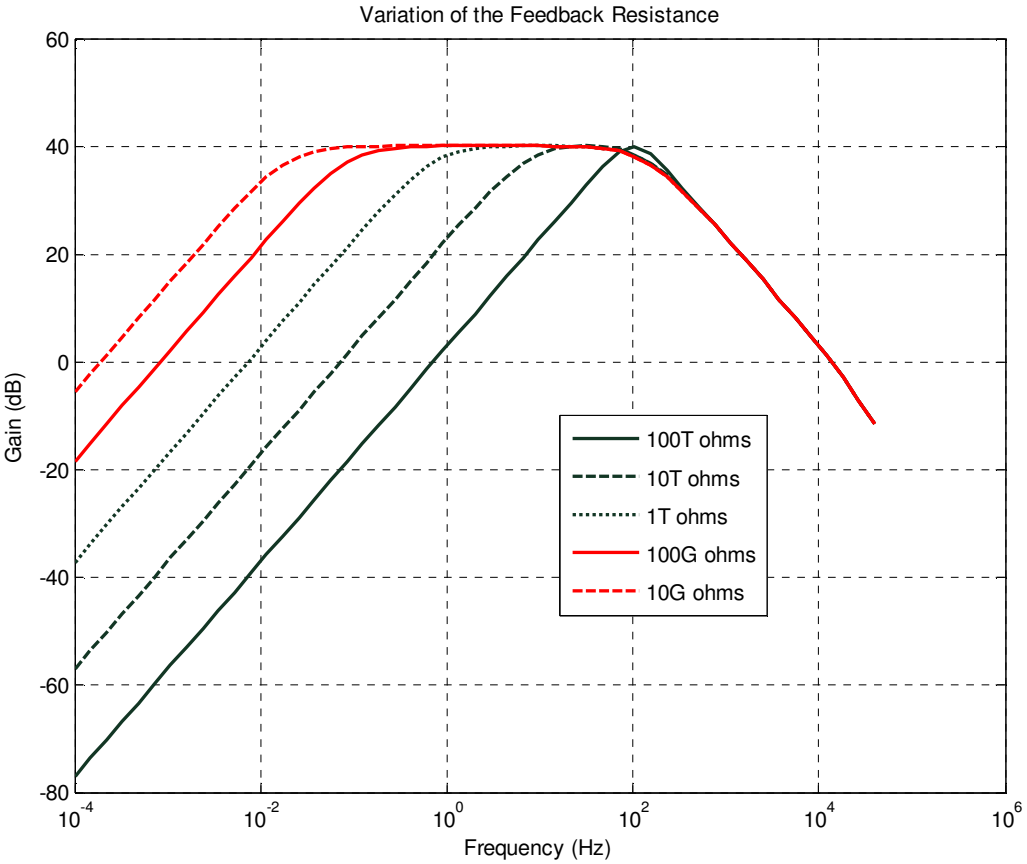

Figure 18 Frequency response of the IA for different values of the feedback resistors

4.3.3 Discussion of Mathematical Model Results

The plot in Figure 17 shows the frequency response obtained for different values of the parasitic resistance for a given fixed feedback resistance of 1 TΩ. For values of the parasitic resistance greater than 500 MΩ, a very good response is obtained. The value of this resistor is dependent on the chopping frequency and the input capacitance of the OTA. Proper choice of these parameters results in better overall response. This

also places limits on the chopping frequency; the chopping frequency should be chosen to be greater than the 3dB frequency of the OTA and also greater than the flicker noise corner. Details of this are discussed later in this section.

The plot in Figure 18 shows the variation of the frequency response with the value of the feedback resistance for a given value of the parasitic resistance. From this plot, it is observed that the greater the value of the feedback resistor, the better the response. For the given parasitic resistance of 1 GΩ, a feedback resistor greater than 1 TΩ is required to obtain the desired frequency response. This however comes at the cost of the size of the input capacitor to provide the gain for the circuit. This necessitates an implementation of a large resistor which is discussed later in this section.

4.3.4 Macromodel Simulation

In this system-level implementation in the CADENCE analog environment, the macromodel of the fully differential OTA shown in Figure 19 is used. One important parameter that is modeled is the input capacitance, C_{in} of the OTA since this directly affects the size of the parasitic resistor. R_{nd} and C_{nd} model the non-dominant pole, R_{out} is the output resistance of the OTA. In this system, a very large feedback resistance is used in the order of 1 TΩ.

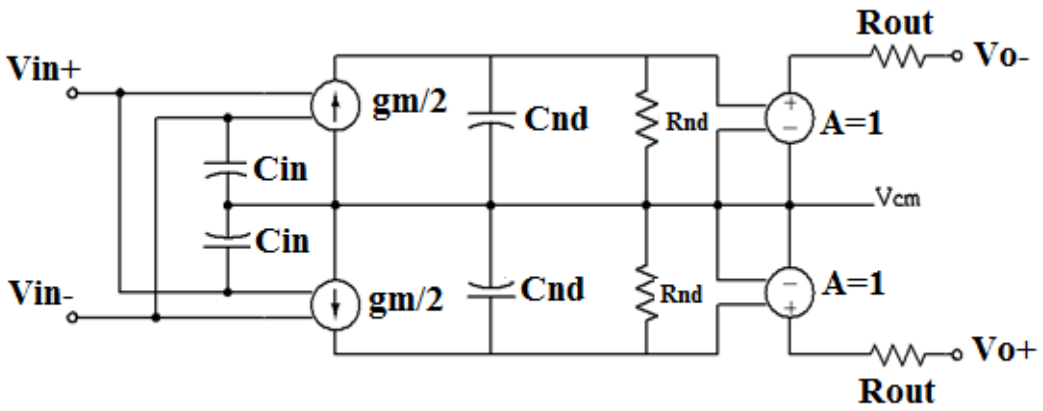

Figure 19 OTA macromodel

The objective of this simulation is to determine the minimum value of the parasitic resistor that will ensure the proper operation of the circuit. This is done by optimizing the input capacitance (which is largely dependent on parasitics) and the chopping frequency. The value of the parasitic resistor for one half of the switched capacitor network in Figure 14 is shown in Figure 20.

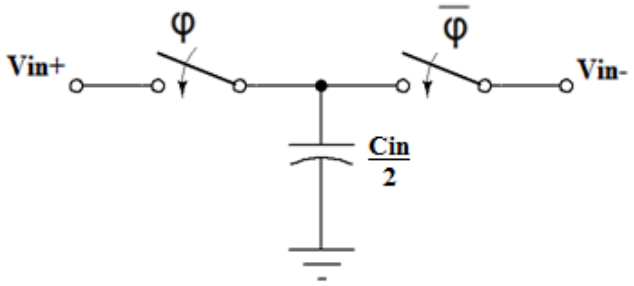

Figure 20 Switched capacitor equivalent half circuit

The switched capacitor resistance of the half circuit is found by calculating the charge transfer from V_{in+} to V_{in-} in one clock cycle. This results in an effective resistance given by:

$$R_p = \frac{2}{C_{in} \times f_{chop}} \quad \textbf{(34)}$$

where C_{in} is the input impedance of the OTA and f_{chop} is the chopping frequency of the OTA.

4.3.5 Design Considerations on the Chopping Frequency

To ensure that the chopped signal is not filtered out by the frequency response of the OTA, the chopping frequency is chosen to be smaller than 3-dB bandwidth of the amplifier [44]. The smallest noise is achieved when chopping frequency is chosen to be equal to the amplifier corner frequency [27]. To ensure that the whole flicker noise band is modulated and thus prevent issues of noise folding back to DC, the chopping frequency is chosen to be greater than the flicker noise corner of the amplifier.

4.3.6 Design Considerations on the Input Capacitance

The input capacitance of the amplifier is largely accounted for by the parasitics. Much effort is required in the layout to minimize this capacitance.

The input capacitance depends on the sizing of the transistors. The larger the area, the larger the parasitics and hence the input capacitance. In low noise amplifier

designs, the input transistors are sized as large as possible to achieve very small noise. This comes at the cost of the parasitic capacitance.

The choice of the input capacitance also has a direct effect on the frequency of the spikes due to charge injection. The higher the input capacitance, the larger the time constant of the spikes and the lower the frequency of the spikes which increases the residual offset. Thus the input capacitance should be minimized to reduce this effect.

4.3.7 Design Consideration on the Input Modulator

One of the critical issues in the design of this amplifier is the design of the input modulator. The effect of charge injection and parasitic coupling causes spikes in the output of the input modulator as mentioned earlier. The spikes are amplified and demodulated resulting in residual offset at the main output. However, the energy of the spikes will be located at high frequency and so if the OTA is designed to have a bandwidth less than the frequency of the spikes, the spikes will be significantly attenuated before demodulation. The residual offset will thus be significantly reduced [45]. Using an OTA with a very wide bandwidth is desirable, but that will also have a very large input offset since the spectral components of the spikes will all contribute [27].

The time constant for the charge injected signal is determined by the switch *ON* resistance of the modulator and the input capacitance of the amplifier. This is made small such that frequency component of the spikes are higher than the OTA's bandwidth and thus result in a significantly low residual offset.

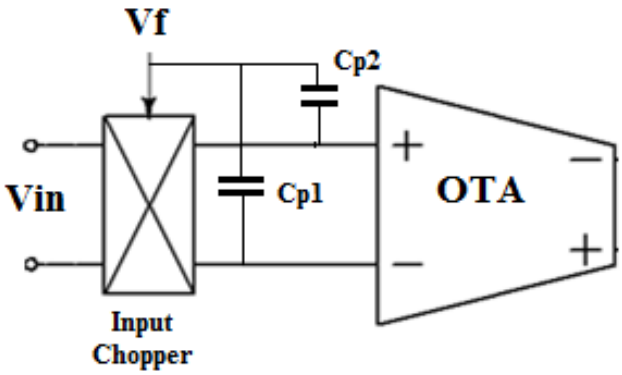

Figure 21 Model for evaluating the residual offset of the amplifier

Figure 21 shows a model for evaluating the residual offset due to mismatch imbalance in the input chopper. The residual offset that results due to charge injection is given by the expression below [31].

$$V_{os} = 2\,(R_1 + R_2)(C_{P1} - C_{P2})\,V_f \times F_{chop} \qquad \textbf{(35)}$$

R_1 and R_2 are the switch ON resistance of the input switches. C_{p1} and C_{p2} are the parasitic capacitance due to the two inputs. V_f is the amplitude of the square wave chopping signal and f_{chop} is the chopping frequency.

The equation above shows the importance of careful layout of the input chopper. Minimizing the mismatches in the parasitics results in a significantly lower residual offset. Using a lower chopping frequency also reduces the residual offset as can be seen in the equation.

Another consideration on the input modulator is noise. The thermal noise of the input modulator should be much smaller than the thermal noise of the OTA so that it would not significantly increase the thermal noise floor of the system. The input modulator switches should thus be designed to have a lower thermal noise. The thermal noise of the output chopper is not critical and should be sized to reduce parasitics.

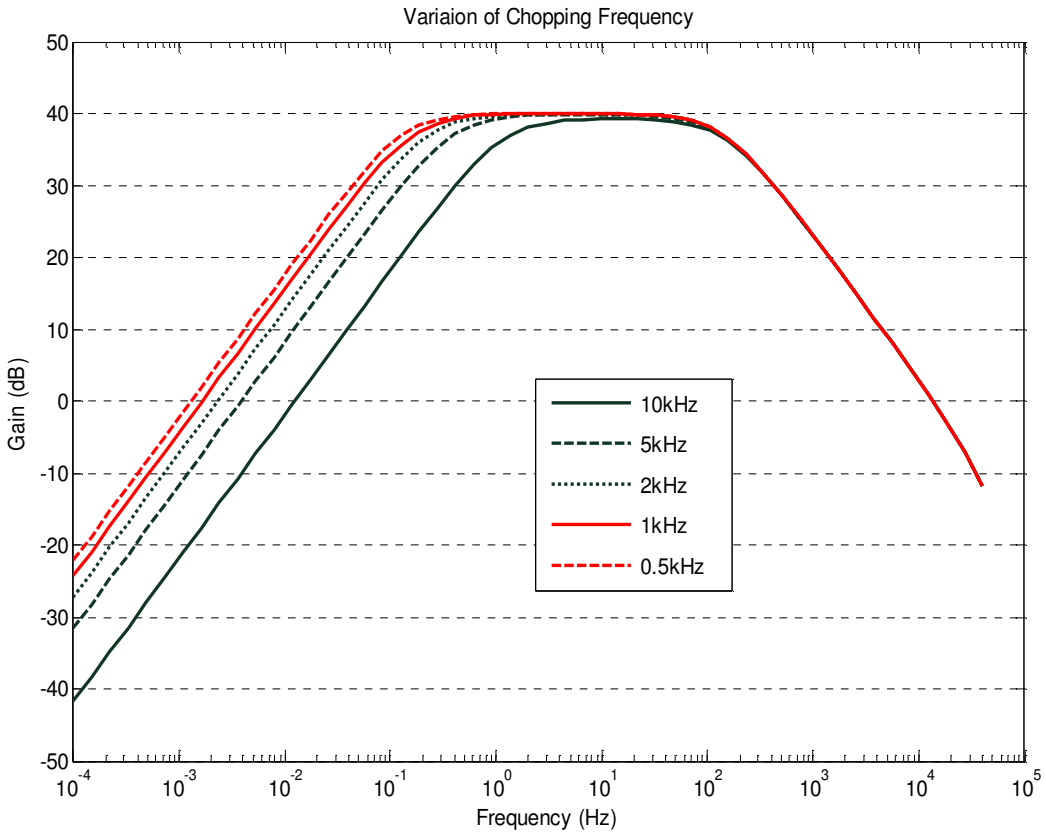

Figure 22 Frequency response of the IA for different chopping frequencies

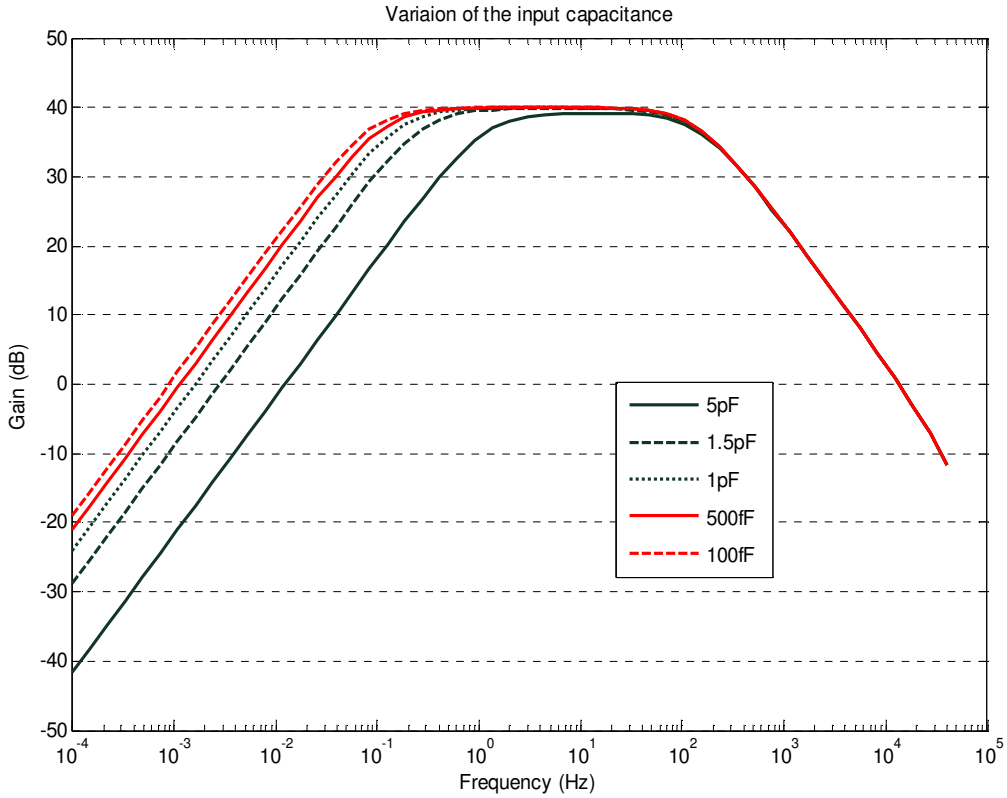

Figure 23 Frequency response of the IA for different values of the input capacitance

4.3.8 Discussion of the Macromodel Simulation Results

As already predicted by the model in earlier in the section, the desired response is obtained when the value of the parasitic resistance is maximized. The chopping frequency and the input capacitance of the OTA are chosen and designed based on the value of parasitic resistance obtained from the MATLAB simulations. Figures 22 and 23 show the variation of the frequency response with the chopping frequency and the input capacitance of the OTA respectively. For high chopping frequencies and large input

capacitance we obtain a much deviated response from the ideal situation. Better results are obtained by minimizing both of these parameters.

4.4 Trade-off Between Input Impedance and Noise

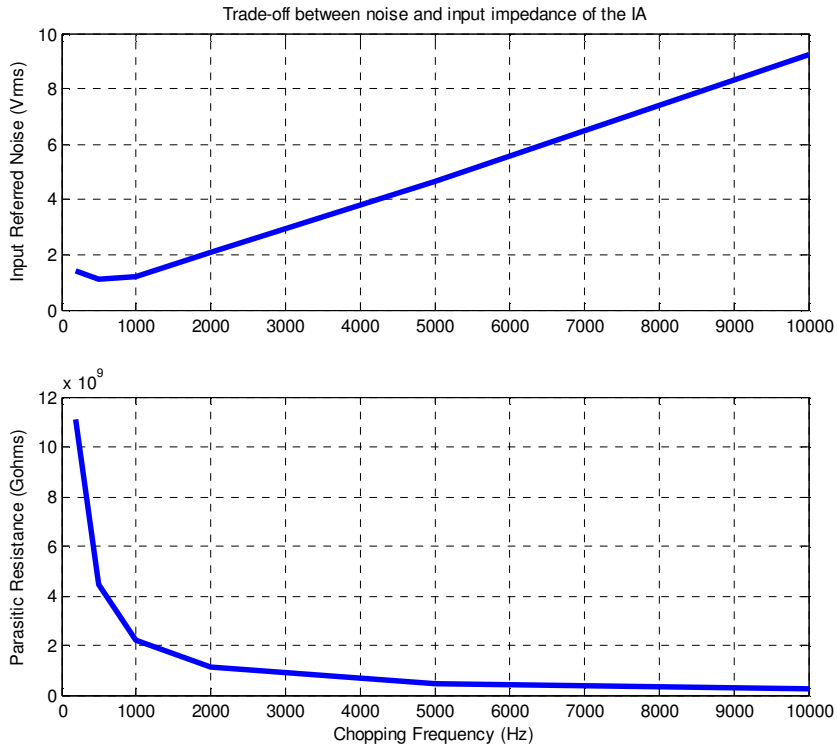

Figure 24 Plot showing tradeoff between input capacitance and input referred noise

Figure 24 shows plots of the variation in chopping frequency versus the input referred noise and the parasitic resistance. The parasitic resistance determines the input

impedance of the instrumentation amplifier. The chopping frequency varies inversely with the parasitic resistance for a fixed input capacitance of the OTA. Thus the higher the chopping frequency, the less the input impedance which causes a reduction in the overall gain of the instrumentation amplifier. Reduced gain of the instrumentation amplifier results in a higher input referred noise as can be seen in the input noise versus chopping frequency plot.

For chopping frequencies less than the flicker noise corner of the OTA, the input referred noise rises slightly as can be seen in the plot. This is because the modulation of the flicker noise happens for only part of the flicker noise band and thus a slight increase in the noise at very low chopping frequencies.

4.5 Proposed Implementation of Large Resistor

The T-network has been used to implement a continuous impedance multiplier in [43].

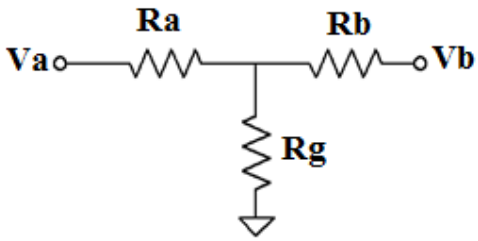

Figure 25 T-network of resistors

The effective resistance of a T-network of resistors shown in Figure 25 is determined as follows.

Assuming either V_a or V_b is at approximately zero potential, the effective resistance seen across the T-network can be calculated as:

$$R_{eff} = R_a + R_b + \frac{R_a R_b}{R_g} \quad \textbf{(36)}$$

Proper choice of R_a, R_b and R_g can result in a very large resistance. Using a poly resistor will result in a very significant increase in the noise of the circuit. To prevent this issue, a diode connected transistor is used to implement the resistors R_a and R_b. The diode connected transistor can implement a very large resistance by itself [19], so using it in this configuration will even make the resistance significantly larger. R_g can be implemented using a simple poly resistor with a very small resistance value or a transistor in triode region.

The diode connected transistor is used to generate the resistor because the voltage variations across the amplifier results in very small current through the diode resulting in very large resistance in the range of 1TΩ. If the diode connected transistor is used in the T-network, an equivalent resistance greater than 10TΩ can be achieved. This relaxes the specification of the parasitic switched capacitor resistor. The proposed implementation is shown in Figure 26.

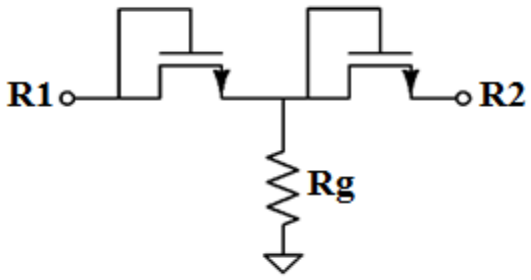

Figure 26 T-network implementation using the diode connected NMOS

5. TRANSISTOR LEVEL IMPLEMENTATION

5.1 Operational Transconductance Amplifier

The current mirror OTA is a popular OTA topology. Compared with the folded cascode and telescopic topologies, the current mirror OTA is advantageous in terms of headroom and so for applications which require low power, the voltage supplies can be reduced with little effect on the design. Figure 27 shows the schematic of the fully differential current mirror OTA.

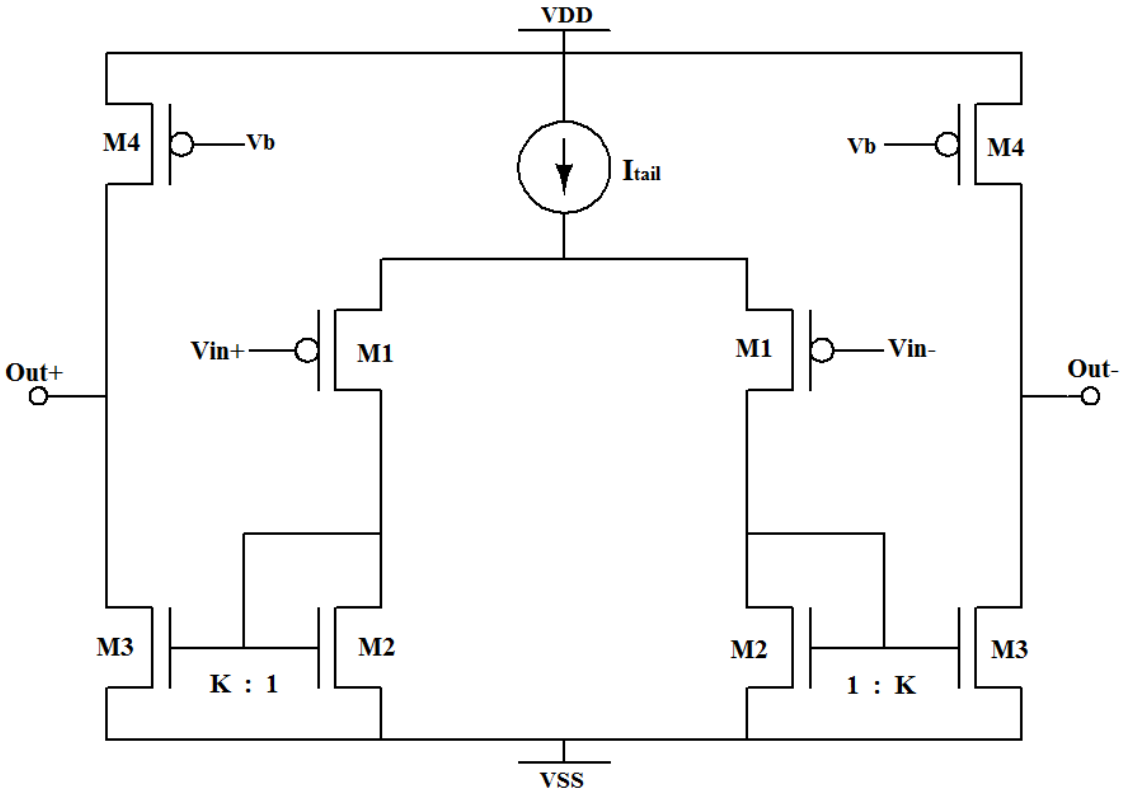

Figure 27 The fully differential current mirror OTA

5.1.1 General Design Consideration

- ***DC Gain***

The DC Gain for the OTA is given by:

$$A_o = G_m R_{out} \tag{37}$$

where the Transconductance for a given mirroring factor, K is given by:

$$G_m = Kg_{M1} \tag{38}$$

The frequency dependent Transconductance of the OTA is given by

$$G_m = \frac{Kg_{M1}}{1 + \frac{s}{w_{ND}}} \tag{39}$$

where w_{ND} is a non-dominant pole which is located at:

$$w_{ND} = \frac{g_{M2}}{C_{GS2}(1 + K)} \tag{40}$$

The G_m depends on the mirroring ratio, denoted K. The higher the mirroring ratio, the more the G_m that can be obtained and hence the greater the DC gain. However the increase in K results in a proportional increase in the size of the output transistor of the mirror and hence an increase in the parasitics at the mirroring node, and thus a reduction in the bandwidth. Also increasing the K factor means increasing the power consumption of the OTA.

The output resistance of the OTA is mainly determined by the sizing of the output transistors and the amount of current in the output arms. The lengths of the transistors can be increased to obtain a higher resistance but that will also result in

increasing the parasitic at the output node. To boost the output resistance, a set of cascode transistors can be used at the output but this will come at the cost of voltage headroom. The cascode devices will also introduce an additional pole that will reduce the bandwidth of the OTA.

- ***Input Referred Noise***

The input referred thermal noise of the OTA is given by:

$$v_n^2 = \frac{16kT}{3g_{M1}}\left(1 + \frac{g_{M2}}{g_{M1}} + \frac{g_{M3} + g_{M4}}{K^2 g_{M1}}\right) \quad \textbf{(41)}$$

It is observed from equation 41 that, the most important parameter for the noise is the *gm* of the input devices. Increasing the *gm* will reduce the noise but this requires an increase of bias current, transistor dimensions or both. Again using a *K* factor greater than one also reduces the noise. This however increases the power consumption and also results in larger parasitics at the non-dominant pole location.

Flicker noise is minimized by using PMOS input devices with much lower flicker coefficient, and sizing them as well to have a larger area and reduce the noise.

- ***Power Consumption and Maximum Signal Swing***

The power consumption and maximum signal swing of this topology are given by:

$$P = (1 + K)\, I_{tail} \times (V_{dd} - V_{ss}) \quad \textbf{(42)}$$

$$V_{swing} = (V_{dd} - V_{ss}) - 2V_{dsat} \quad \textbf{(43)}$$

5.1.2 Designing Using the ACM All Region Equation

The current mirror OTA topology is a standard topology for driving capacitive loads as in our case [19], but to ensure a very low noise and very low power design, much effort is required in the design of the transistors to ensure the required low power and noise. For the design, important features of the ACM transistor model (named after the three individuals that formulated the model – Ana, Carlos, Marcio) [46] is exploited to properly optimize the noise and power of the OTA.

The ACM model is a very attractive model of the transistor that allows transistors to be designed for any inversion level; weak, moderate or deep inversion, using the same set of equations. In this case where very low power is desired, it is obvious that most of the transistors will be operating in weak or moderate inversion since very small bias currents are used. To properly characterize the behavior of these transistors, it is more appropriate to use the all region ACM model.

The ACM model for the MOS transistor is defined by the following equations.

$$I_d = g_m \times n \times \emptyset_t \frac{1 + \sqrt{1 + i_f}}{2} \quad \textbf{(44)}$$

$$W/L = \frac{g_m}{\mu C_{OX} \emptyset_t} \left(\frac{1}{\sqrt{1 + i_f} - 1} \right) \quad \textbf{(45)}$$

$$f_T = \frac{\mu \emptyset_t}{2\pi L^2}\left(2\sqrt{1 + i_f} - 1\right) \quad \textbf{(46)}$$

I_d is the transistor drain current, *gm* is the transconductance in saturation region, *n* is the slope factor which is typically chosen as 1, i_f is the inversion level or coefficient, *W* and *L* are the width and lengths of the transistor, μ is the mobility of the holes or electrons of the transistor, φ_t is the thermal voltage of the transistor and f_T is the intrinsic cut-off frequency of the transistor.

If i_f is greater than one, the device operates in strong inversion and the *gm* is proportional to the square root of I_d. If i_f is much less than one, the device operates in weak inversion and the *gm* is proportional to I_d. By appropriately setting these parameters a much optimized design solution is obtained. Table 2 summarizes design parameters of the OTA.

Table 2 Summary of the ACM design of the OTA

Device	**Dimensions (W/L)**	**I_D**	**Inversion coefficient**	**G_m efficiency (G_m/I_D)**
M1	5µm/0.6µm	150n	0.2178	22.67
M2	20 µm /10 µm	150n	0.24	20.70
M3	20 µm /10 µm	150n	0.24	20.73
M4	30 µm /10 µm	150n	1.8	18.48
M(I_{tail})	10 µm /2 µm	300n	10.2	4.0

As shown in the Table 2, most of the transistors used in this OTA are designed to operate in the weak inversion. This allows us to use very small bias current and still get a good *gm* efficiency and hence good performance for the OTA for the application. A tail current of 300nA was used. Minimum channel length was used for the input devices to minimize the gate capacitance to keep the parasitic resistance at the desired value. The output devices were designed to have large L to increase the output resistance and hence the DC gain of the OTA.

5.2 The Common Mode Feedback Circuit

In fully differential amplifiers, a common mode feedback circuit (CMFB) is required to stabilize the output DC level of the amplifier. This is necessary because for a small mismatch in currents in the two arms, owing to the large output impedance, the equivalent DC voltage difference between the two outputs is significantly large and can throw the amplifier off balance and thus degrade the performance drastically.

A typical CMFB circuit has a common mode detector which is used to determine the common mode voltage level of the amplifier. This voltage is compared with the desired reference and the error voltage is fed back into the amplifier to correct the error.

In this topology of the CMFB used shown in Figure 28, the two output are individually compared to the desired reference, in this case, GND, then the individual errors are summed up and fed back to the tail current to correct the error.

This is a simpler way to implement the CMFB without using large resistors and capacitors as common detectors which takes up some area as well. The disadvantage is

that to obtain the same loop performance of the CMFB loop as the original amplifier, the same amount of power used in the amplifier is needed in the two differential pairs.

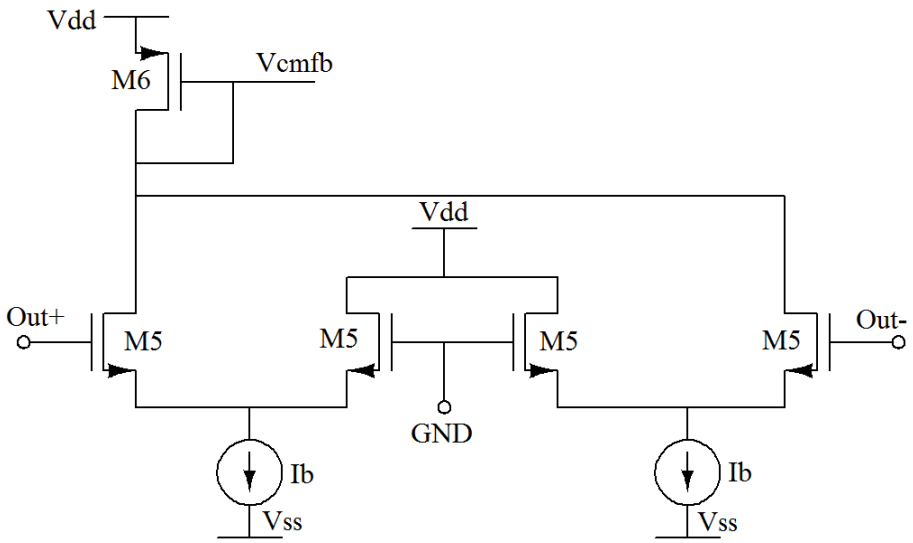

Figure 28 The common mode feedback circuit

Table 3 Device dimension of the CMFB

Device	**Dimensions (W/L)**	**I_D**
M5	5µm/0.6µm	150n
M6	10 µm /2 µm	Error Current
M(I_{tail})	10 µm /5 µm	300n

Table 3 summarizes the design parameters of the CMFB. It is designed to have the same AC behavior as the OTA.

5.3 T-network Pseudo Resistor

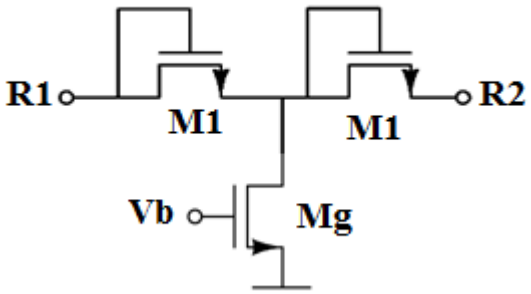

Figure 29 T-network pseudo resistor

Figure 29 shows the T-network pseudo resistor. Grounded resistor R_g is implemented using a transistor, M_g with a gate bias and sized to realize the required resistance.

The equivalent resistance, given by the source-drain resistance, R_{ds} of the transistor is derived from:

$$R_{ds}=\frac{L}{\mu C_{ox} W(V_{GS}-V_T-V_{DS})} \quad (47)$$

Table 4 shows the dimensions of the transistors used in the implementation of the T-network.

Table 4 Device dimension for T-network

Device	Dimension (W/L)
M_1	5µm/2.5µm
Mg	160µm/0.6µm

5.4 The Chopper

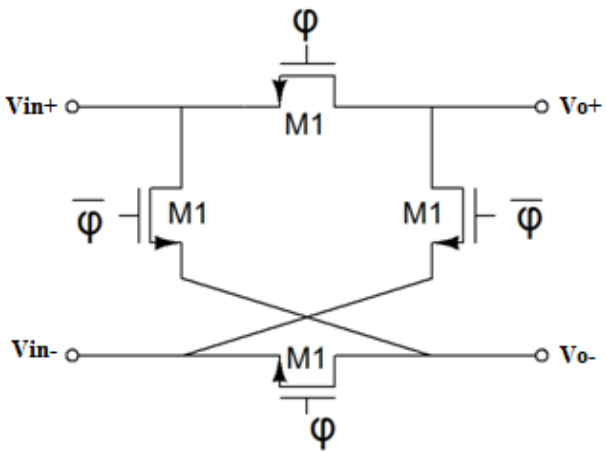

Figure 30 Schematic of the modulator

Figure 30 shows the schematic of the chopper modulator. The chopper should be driven with a non-overlapping clock to prevent noise leakage. On the other hand the duty cycle of the clock should be almost 50% to have proper modulation [32].

In designing the transistors for the chopper, the main considerations are the *ON* resistance, and the parasitic capacitance of the switches of the modulator. To obtain a small *ON* resistance which is desirable to reduce significantly the residual offset, a small

device length is required. Also, a small *ON* resistance ensures higher frequency of the chopping spikes which reduces the resulting residual offset. The switch resistance is also a noise source and thus should be reduced as much as possible.

The implementation of the switches is another issue of critical importance. To reduce the charge injection which results in residual offset, a CMOS switch will be preferred to either an NMOS or a PMOS switch. However this also adds some more parasitic capacitance because of the number of devices. Thus a choice of a simple NMOS is chosen which provides a good trade-off between the two limitations.

The switch dimensions used in the chopper is shown in Table 5.

Table 5 Device dimension for chopper

Device	W/L
M1	2.5µm/0.6µm

5.5 Non-Overlapping Clock Generator

The two phase non-overlapping clock generator is implemented using the schematic in Figure 31. It basically consists of two NAND and seven NOT gates. The logic gates are designed to minimize parasitic capacitance as much as possible to minimize the delay. This also ensures a duty cycle for both phases being approximately 50%.

The non-overlapping clock phases are shown in Figure 32. They exhibit very fast rise and fall times as well as approximately 50% duty cycle.

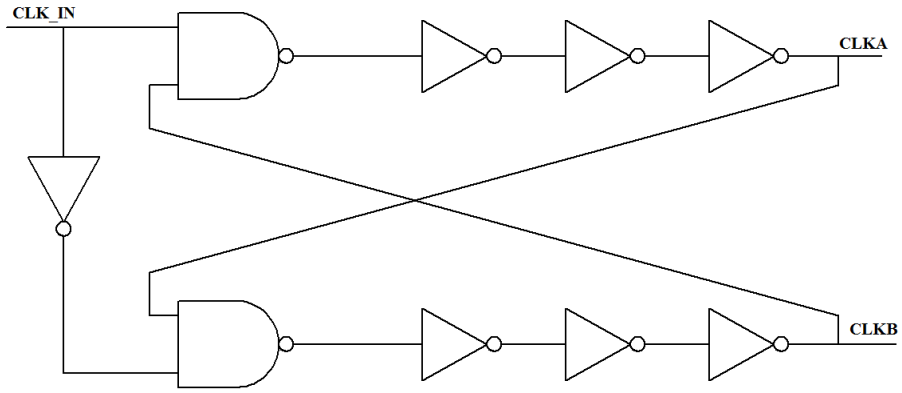

Figure 31 The two phase non-overlapping clock generator

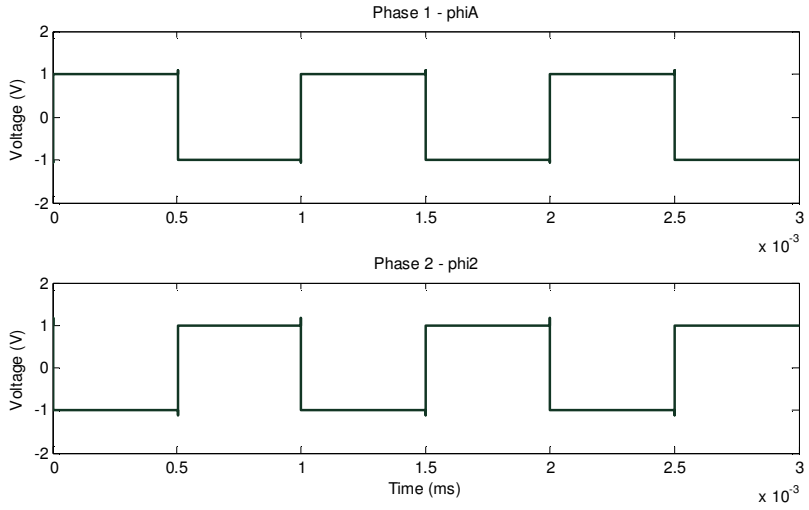

Figure 32 The two clock phases generated by the clock generator

5.6 The Buffers

Buffers are designed to drive the outputs of the instrumentation amplifier. This is implemented using a unity gain feedback configuration of an opamp.

A two stage opamp with miller compensation was designed for this purpose. The main requirement here was a very large DC gain and a large gain bandwidth product (GBW) as well to be able to ensure good performance when used in feedback.

Figure 33 shows the schematic of the opamp used to implement the buffer. Table 6 shows the device dimensions used for the design of the opamp.

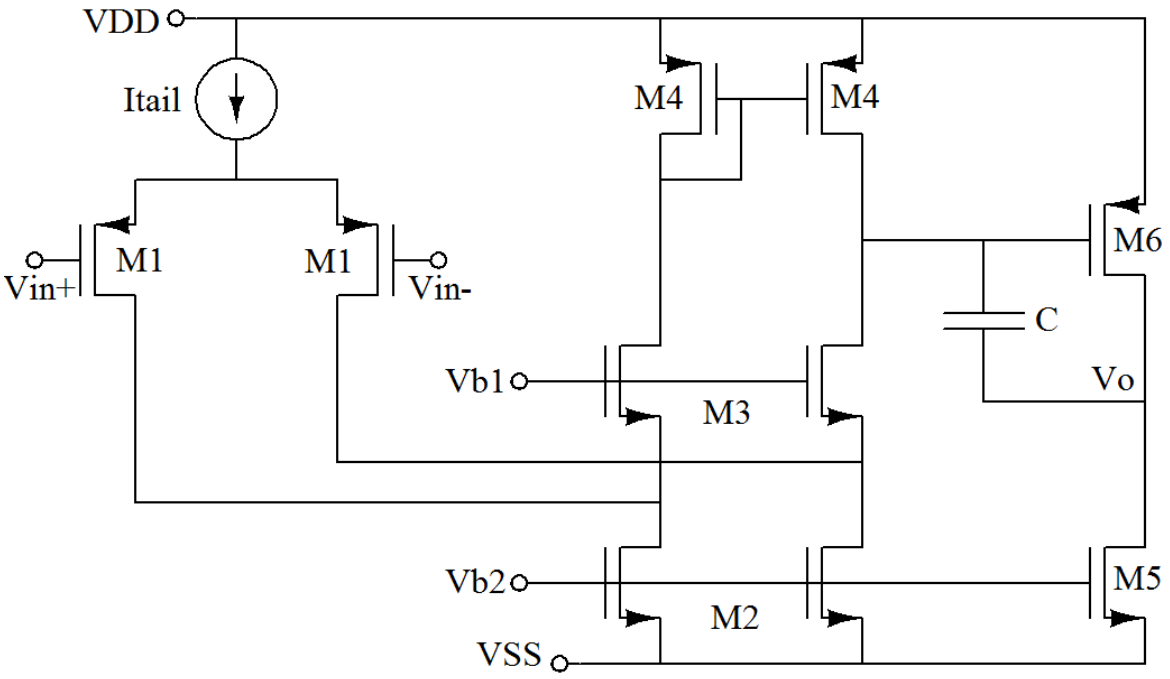

Figure 33 Two stage operational amplifier with miller compensation

Table 6 Deviced dimension for Opamp for buffer implementation

Device	Dimension (W/L)	I_D(A)
M1	25µm/0.6µm	100n
M2	10 µm /1 µm	100n
M3	10 µm /1 µm	200n
M4	20 µm /2 µm	200n
M5	50µm/1µm	200n
M6	20µm/1µm	200n
M(Itail)	20 µm /2 µm	200n

5.7 Complete Schematic

The complete schematic is shown in Figure 34. Results from simulating the whole system is be discussed in section 6.

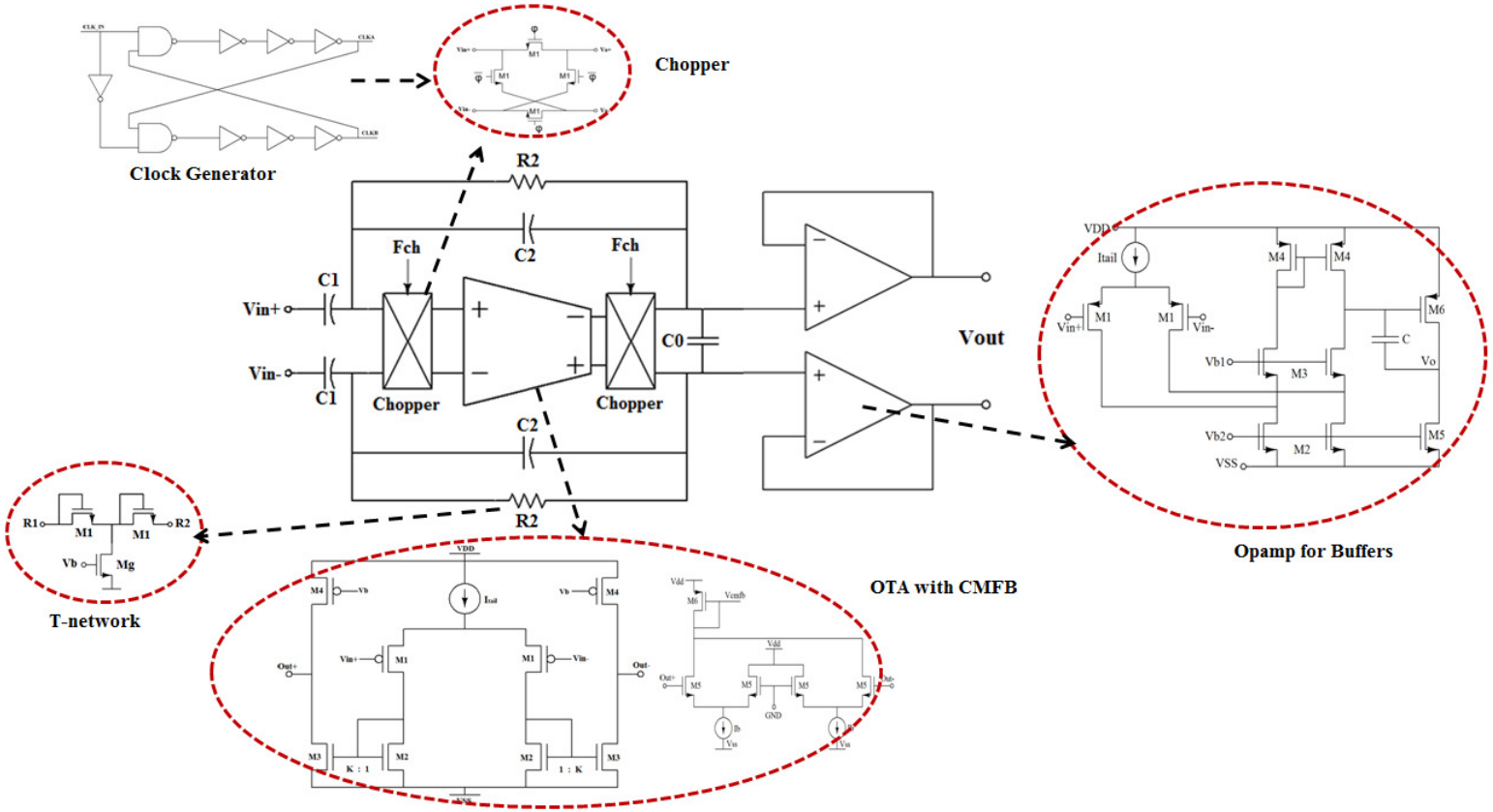

Figure 34 Complete schematic

6. LAYOUTS AND POST-LAYOUT SIMULATION RESULTS

6.1 Critical Layout Issues

The most critical considerations in the layout are the parasitics of the input chopper, the matching of the two input and feedback capacitors and the layout of the OTA.

For the input chopper, much effort is spent in reducing parasitic mismatches by making the layer routings the same for all the switches. The mismatches in the parasitic capacitance of the input chopper will lead to larger chopping spikes and more significant residual offsets.

Another important aspect of the layout of the OTA is managing the input capacitance due to parasitics. The objective here is to reduce the parasitics as much as possible to ensure the accurate performance of the topology. The input capacitance as was discussed earlier, directly affects the parasitic resistance due to chopping at the virtual nodes. This in turn affects the value of the chopping frequency that is chosen.

The third most critical section of the layout is the matching of the two inputs and feedback capacitors. Proper matching of this is very essential to achieve a good CMRR and power supply rejection ratio (PSRR).

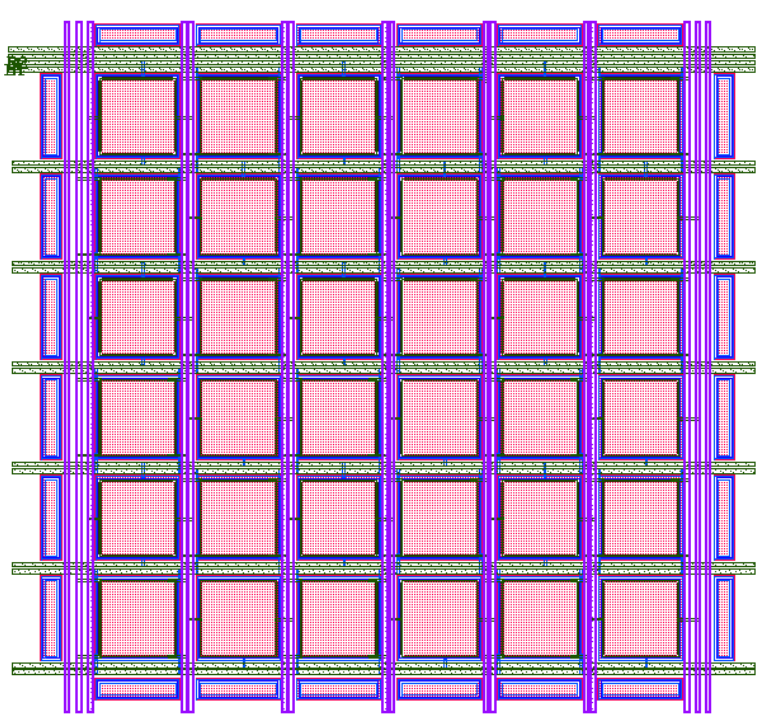

Figure 35 Layout of the two input capacitors

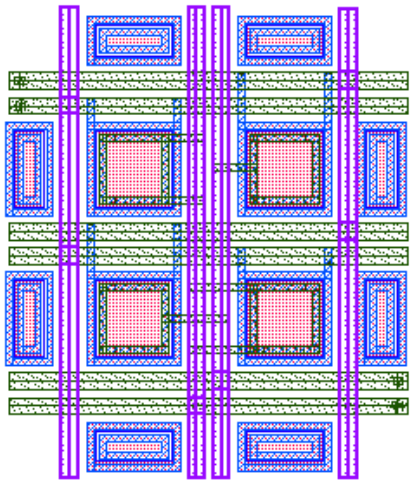

Figure 36 Layout of two feedback capacitors

Figures 35 and 36 show the layouts of the two input and two feedback capacitors respectively. The common centroid and inter-digitized layout approach are adopted in both layouts to ensure a proper matching of the two capacitors.

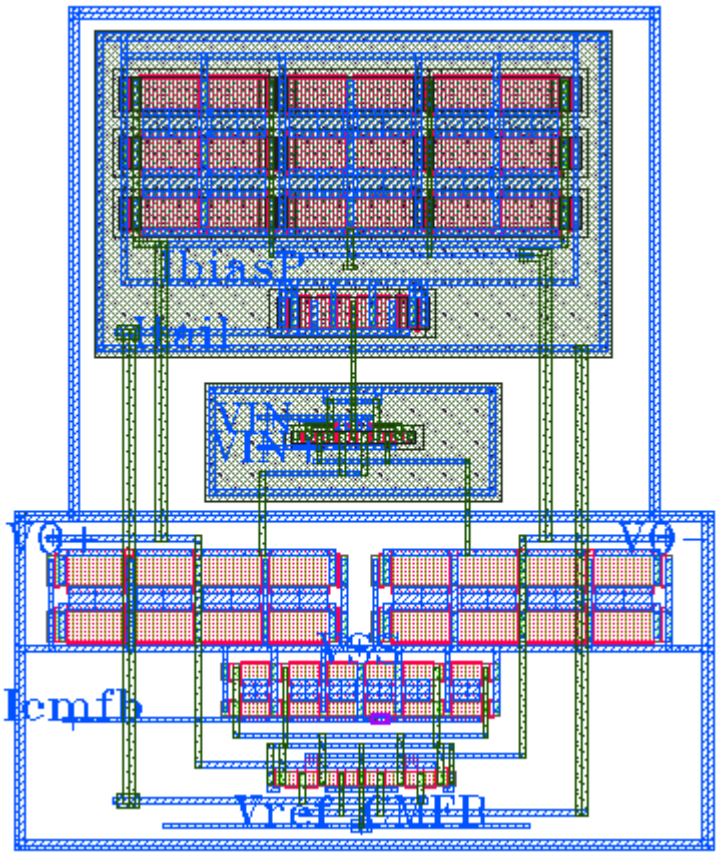

Figure 37 Layout of the OTA

Figure 37 shows the final layout of the OTA. Inter-digitization is used in the layout of all the devices. The layout of the input differential pair is done to minimize parasitics as much possible.

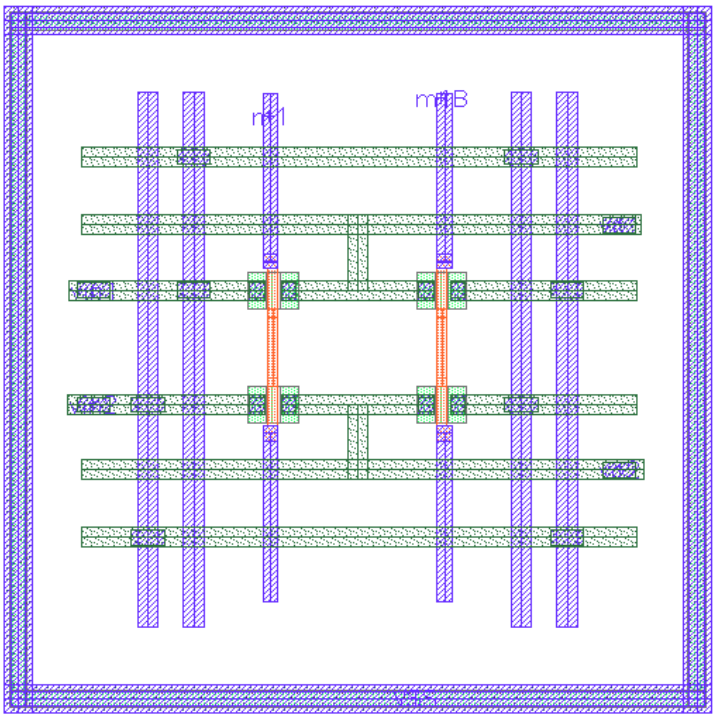

Figure 38 Layout of the input chopper

Figure 38 shows the layout of the input chopper. As shown the metal routings are made as symmetric as possible to minimize the mismatch in the parasitics.

6.2 Complete Layout

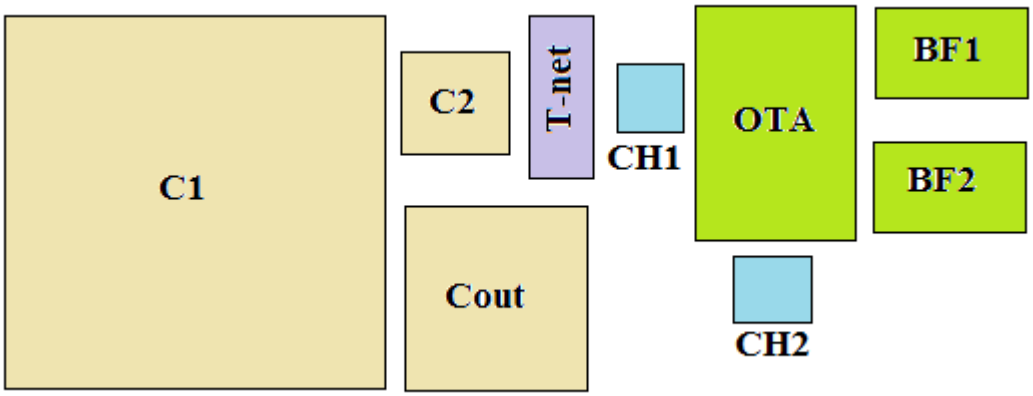

Figure 39 Floor plan of the layout

The floor plan for the final layout is shown in Figure 39. A large portion of the layout is taken by the two 20pF input capacitors. Figure 40 shows the complete layout without the pins. It covers an area of *0.45mm X 1mm*. The final chip layout with all the pins is shown in Figure 41. The dimension of the chip is *1.5mm X 1.5mm*.

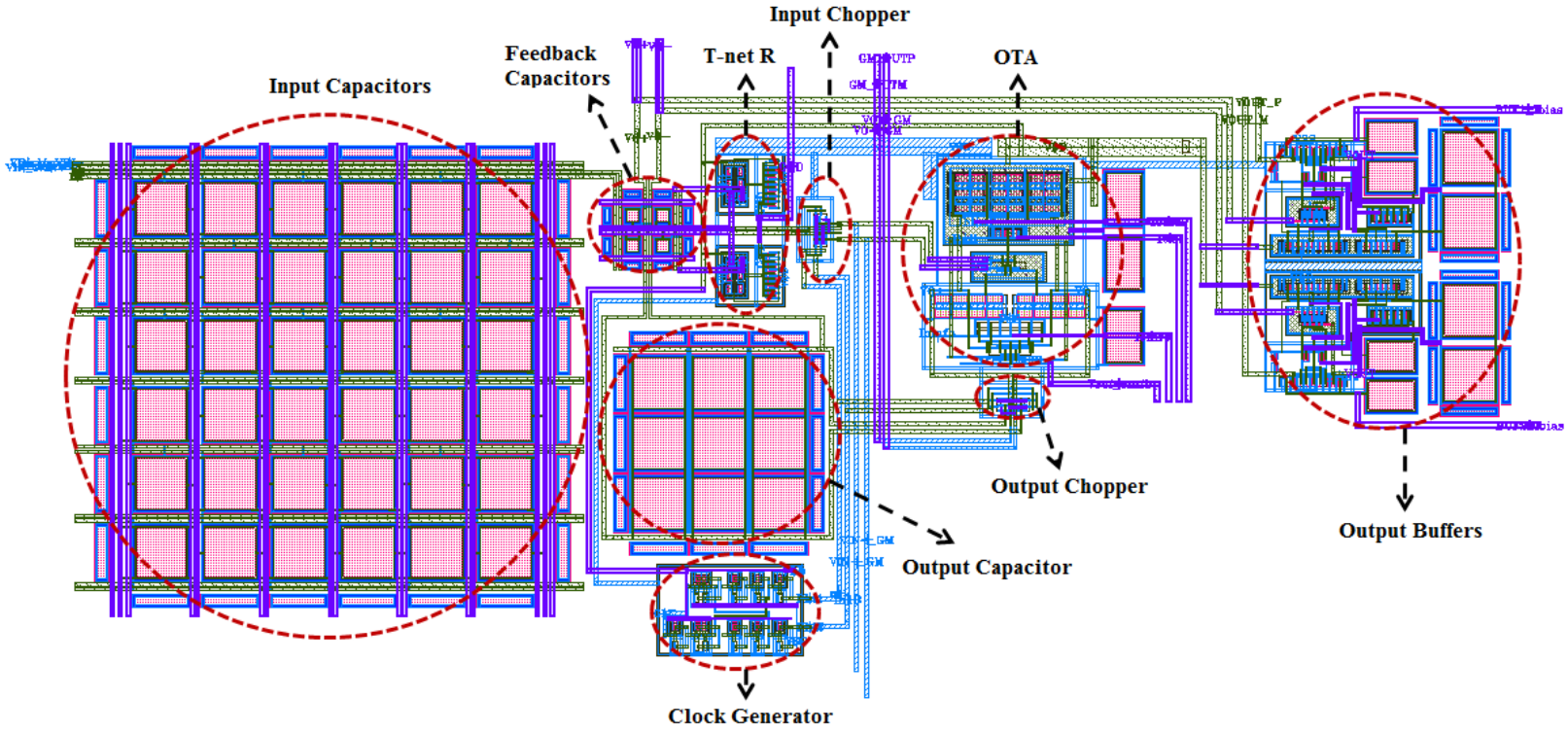

Figure 40 Complete layout

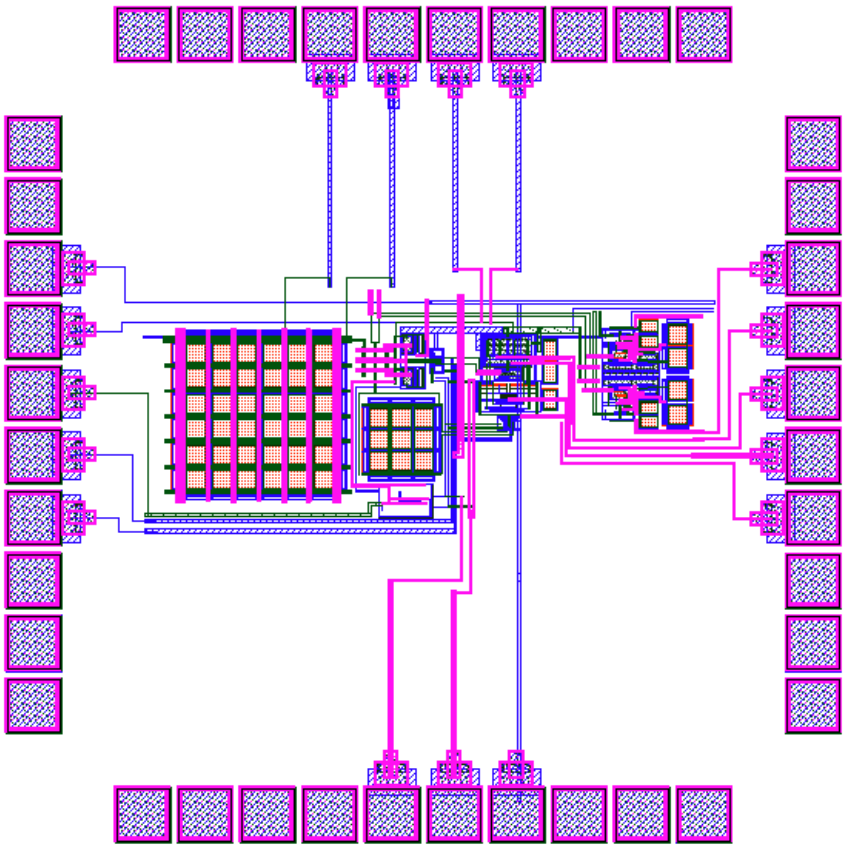

Figure 41 Final chip layout with pins

6.3 Post Layout Simulation Results

6.3.1 The OTA

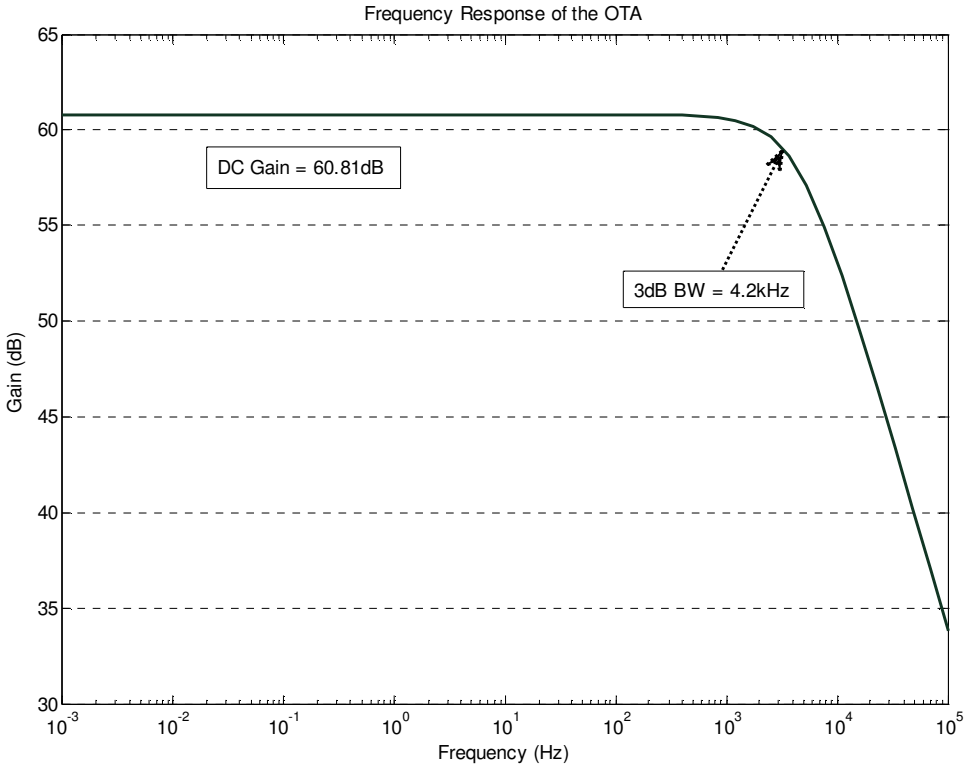

Figure 42 The frequency response of the OTA

The post layout simulation shows that the DC gain of the OTA is 60.8dB as shown in Figure 42. The required *Gm* is 1.4uA/V. This results in the high cut off frequency of the overall instrumentation amplifier of 100Hz. The power consumption of the OTA exclusively determines the power consumption of the instrumentation amplifier. By using the ACM model to design the OTA, power consumption was greatly reduced. Also the topology of the OTA allows the use of a 2V supply. The noise of the

OTA is the most significant noise source in the whole instrumentation amplifier so efforts were made to minimize this. The spot noise at 100Hz was 720nV/√Hz as shown in the input referred noise plot in Figure 43. This value is dominated by flicker noise since the flicker noise corner is 1 kHz. The OTA performance is summarized in Table 7.

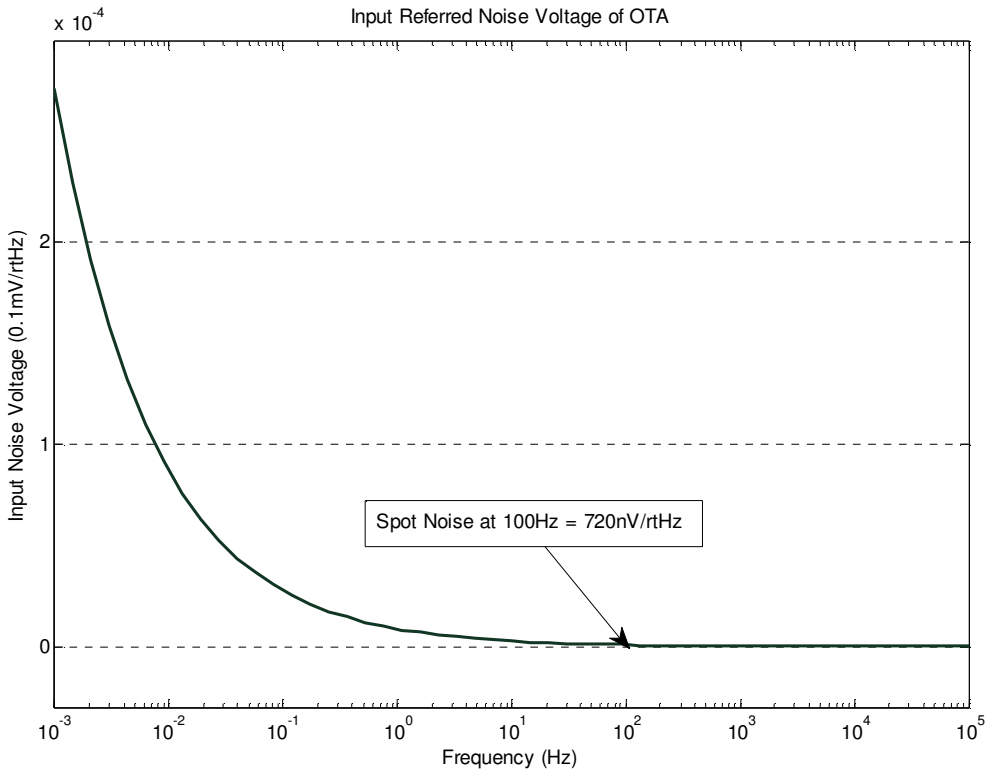

Figure 43 The input referred noise of OTA

Table 7 Summary of OTA performance

Parameter	Result
DC Gain	60.81dB
3-dB Bandwidth	4.2kHz
Spot Noise @100Hz	720nV/rtHz
Current Consumption	1.4uA
Supply	2V

6.3.2 The Buffers

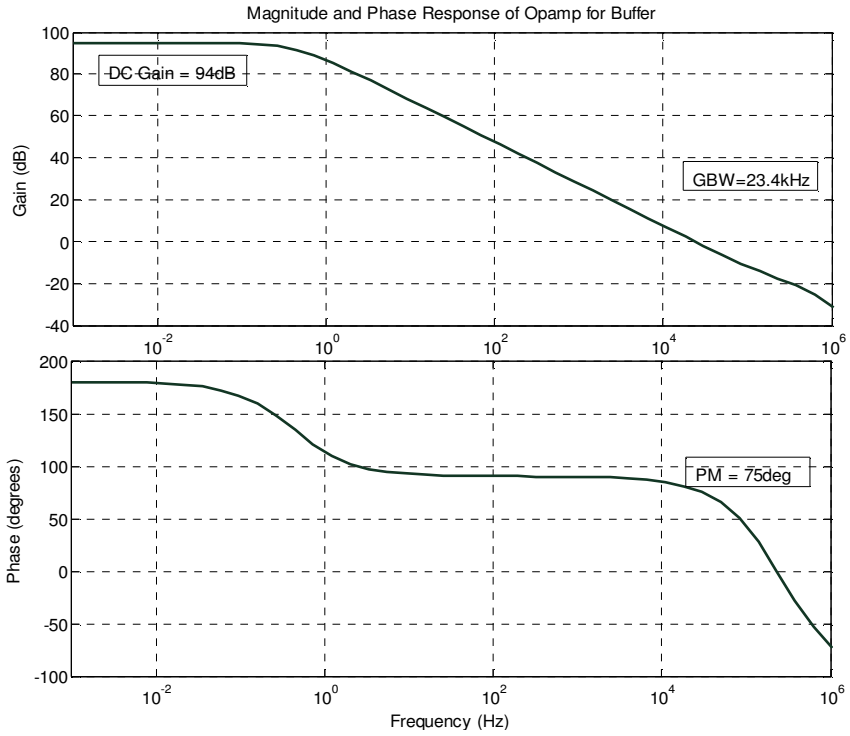

Figure 44 The magnitude and phase response of the opamp used for buffers

Table 8 Summary of the Opamp performance

Parameter	Result
DC Gain	94dB
Gain Bandwidth Product	23.4kHz
Phase Margin	75deg
Power consumption	1.2uW

The magnitude and phase response of the opamp used to implement the buffer is shown in Figure 44. The table summarizing the performance is also shown in Table 8. It has a gain of 94dB and a GBW of 23 kHz which is much larger than requirement for this application. The phase margin is 75 degrees and the power consumption of 1.2μW.

6.3.3 The Final Results

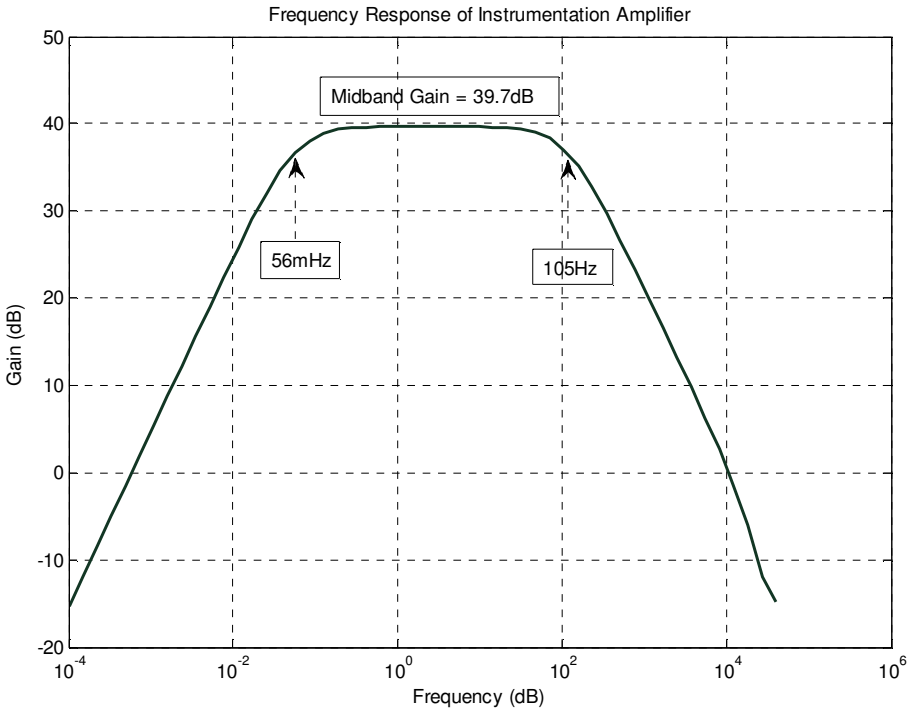

Figure 45 Overall frequency response of the instrumentation amplifier

Figure 45 shows the frequency response of the complete instrumentation amplifier. It shows the expected mid-band gain of 40dB with the bandwidth from 0.06Hz to 100Hz which is the expected bandwidth range for ECG applications. The low frequency of this is however limited by the parasitic resistance due to the chopping. The frequency response of the system without chopping shows the same mid-band gain but the low cutoff frequency is 0.006Hz which is a decade smaller than that with chopping. The frequency response of the instrumentation amplifier without chopping is shown in Figure 46.

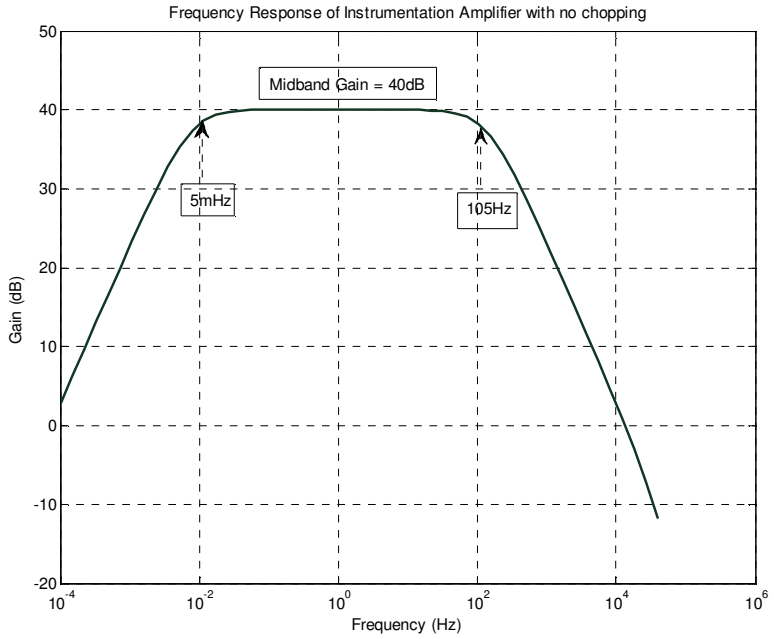

Figure 46 Frequency response of instrumentation amplifier without chopping

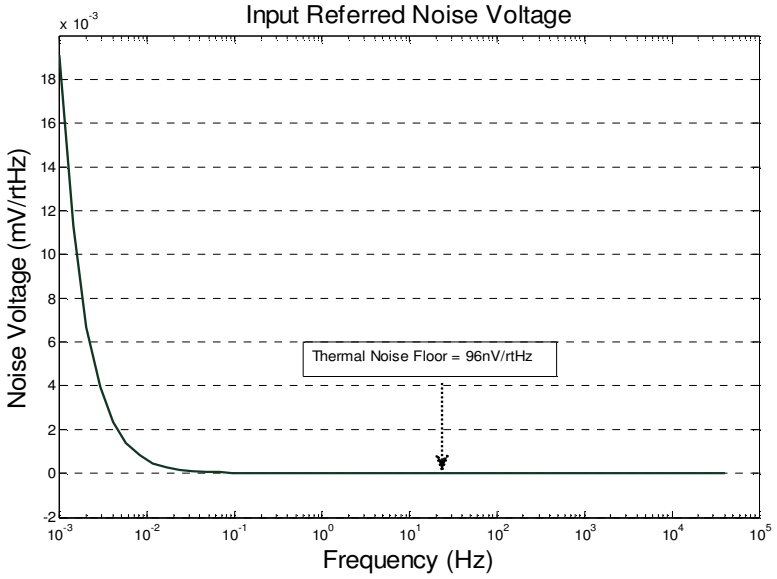

Figure 47 Input referred noise voltage of the instrumentation amplifier

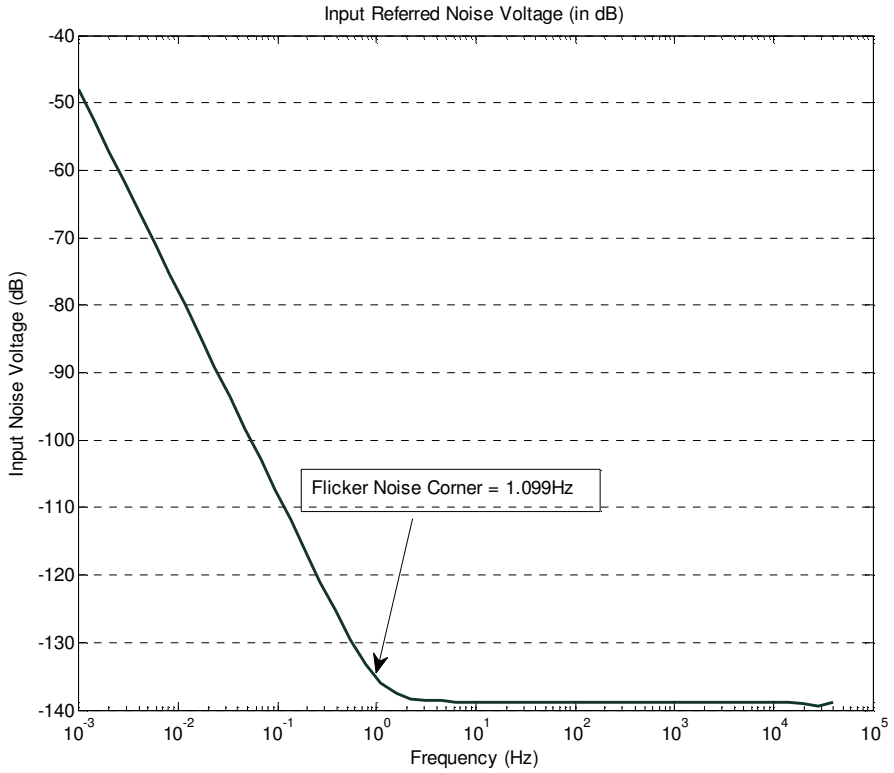

Figure 48 Input referred noise voltage (dB) of the instrumentation amplifier.

Figures 47 and 48 shows the input referred noise voltage in absolute and decibel (dB) respectively. The noise response for the system shows a thermal noise floor of 96nV/√Hz and a flicker corner of 1Hz. This greatly reduces the overall integrated noise in the bandwidth. The flicker noise corner for the system with no chopping shown in Figure 49 is about 1kHz and so the overall integrated noise within the given bandwidth will be much greater than the case with chopping. This reduces the integrated noise in the bandwidth to 1.2μVrms.

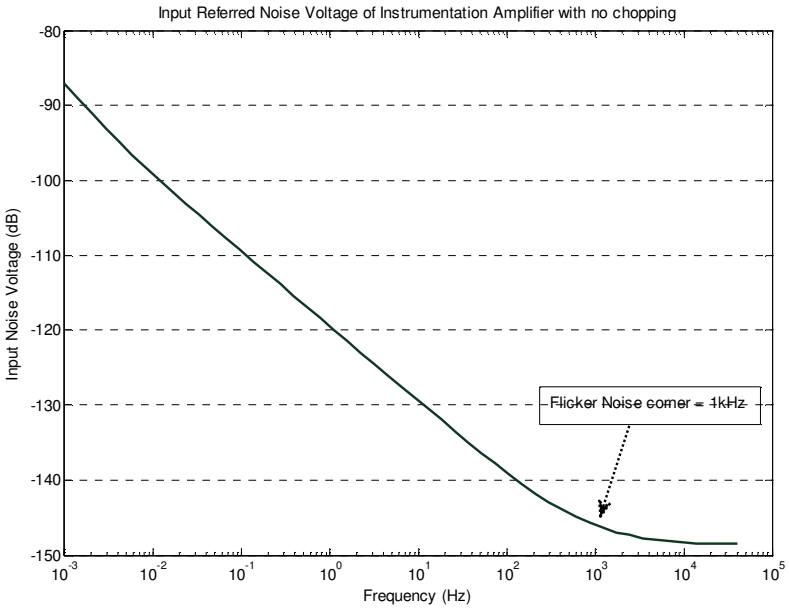

Figure 49 Input referred noise of instrumentation amplifier without chopping

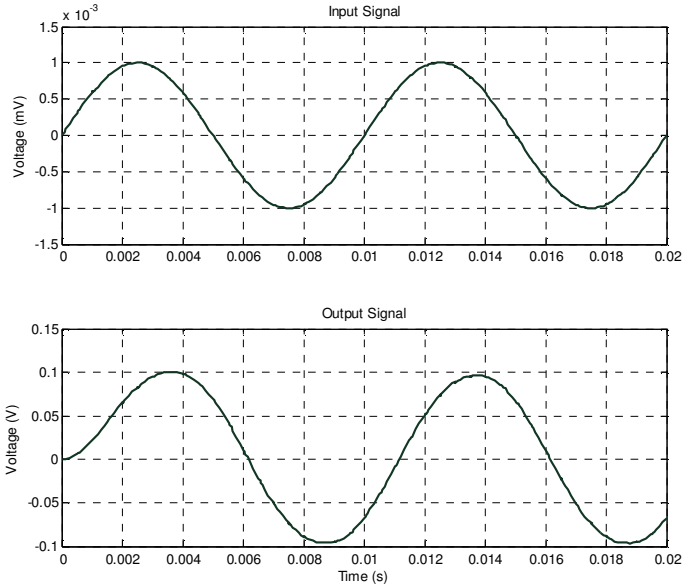

Figure 50 Transient output test using a 2mVpp Sine Signal

The response of the instrumentation amplifier when a 2mVpp sinusoidal signal at 10Hz is applied is shown in Figure 50. It shows the signal correctly amplified by a gain of 100V/V and very clean with barely any noise.

The CMRR plot of the system is shown in Figure 51. Its values range from 78dB to 95dB for the given bandwidth. This is good enough for this application. Better CMRR is achievable with current feedback instrumentation amplifiers. The PSRR is the measured for VDD and VSS and the results are shown in Figures 52 and 53. Its values range from 63dB to 95dB within the bandwidth of interest.

The overall power consumption is 2.8µW which makes it good for continuous monitoring systems.

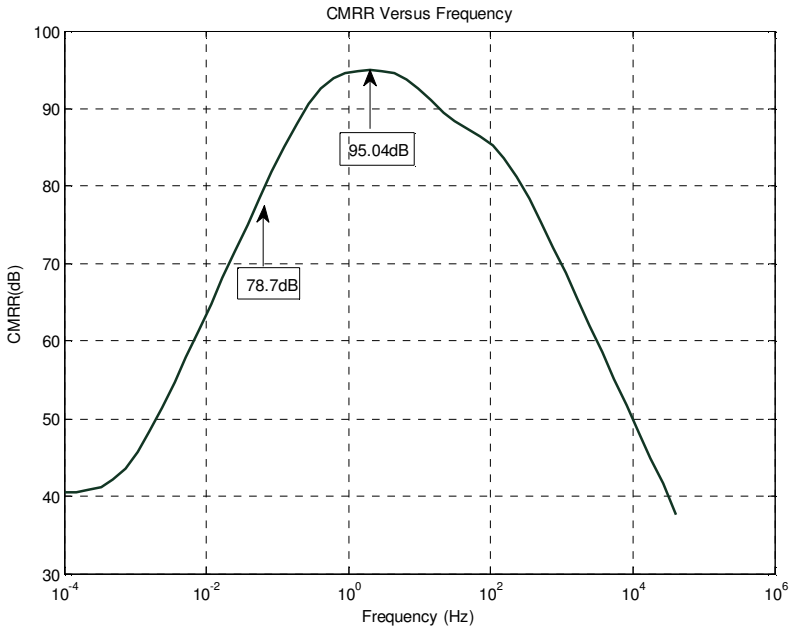

Figure 51 CMRR of the instrumentation amplifier

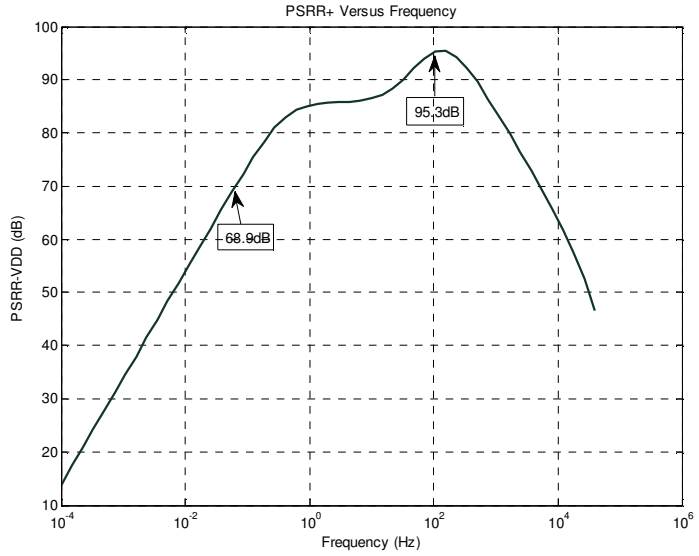

Figure 52 PSRR+ of the instrumentation amplifier

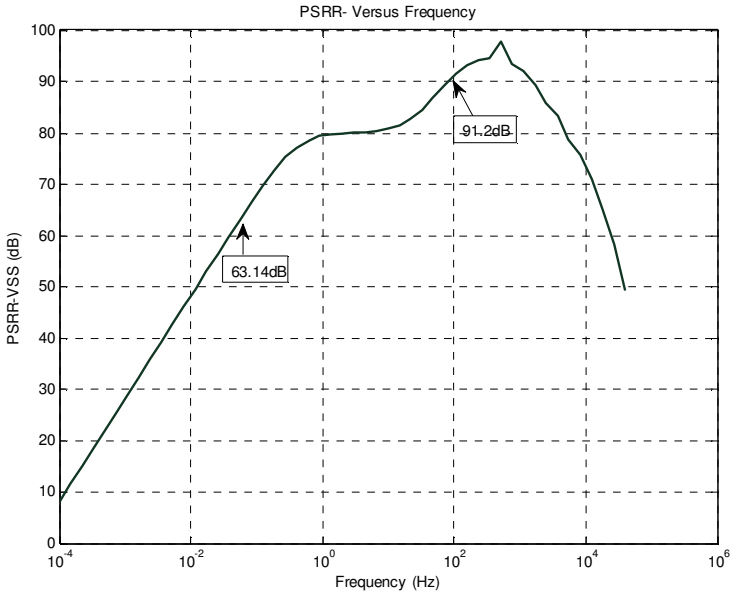

Figure 53 PSRR- of the instrumentation amplifier

Table 9 Summary of performance of the instrumentation amplifier

Parameter	Results
Mid-band Gain	40dB
Bandwidth	0.05-100Hz
CMRR	>75dB
PSRR	>65dB
Input Referred Noise, Vrms (0.1-100Hz)	1.2μVrms
Flicker Noise Corner	1Hz
Supply	2V
Total Current Consumption	1.4μA
Power Consumption	2.8μW
Output Swing	500mV

Table 9 shows a final summary of the performance of the instrumentation amplifier. Table 10 shows the comparison between this work and other state-of-the-art instrumentation amplifiers for biomedical application in the literature.

Table 10 Comparison of results

Parameter	[19]	[39]	[42]	This Work
Gain	40dB	51-68dB	60dB	40dB
Power	0.9µW	60µW	3.5µW	2.8µW
Bandwidth	(2.2 – 30)Hz	0.3 Hz -100*	<1Hz – 100Hz	0.05-150Hz
CMRR	88dB	>110dB	>60dB	>75dB
PSRR	80dB	>78dB	-	>60dB
Integrated Noise (0.5 – 100Hz)	2.4µVrms	0.67µVrms	1.3µVrms	1.1µVrms**
External caps	No	Yes	Yes	No

* The high cut-off frequency in this paper is programmable

** This is the integrated noise for bandwidth 0.5 – 100Hz for the purpose of comparison.

7. CONCLUSION

An instrumentation amplifier for ECG recording has been proposed in this thesis. It implements an AC coupled with a chopper stabilized OTA to achieve low power and low noise. A new approach to implement extremely large resistors using a T-network with pseudo-resistors is also proposed. By this new approach a very low high pass response can be obtained in this instrumentation amplifier which is desirable for this application.

The instrumentation amplifier has a mid-band gain of 40dB with a bandwidth of 0.05 to 100Hz while consuming 2.8uW of power. The integrated noise within the bandwidth is 1.2μVrms with a flicker noise corner reduced from 1kHz to 1Hz by chopping.

The performance of this amplifier is however limited by the parasitic resistance which results from the chopping operation at the virtual node of the OTA. Proper choice of input capacitance and chopping frequency reduces the effect of this parasitic resistance on the amplifier. However there is a trade-off between this and noise and a very good balance is needed to achieve optimized performance.

The instrumentation amplifier has been designed in ON semiconductor 0.5μm CMOS process.

This instrumentation amplifier can find applications in many ECG monitoring and recording system as the front end amplifier to process the heart signals in the presence of very low noise and also achieve very long lifetime.

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VITA

Name: Jesse Coulon

Address: Texas A&M University, Department of Electrical Engineering
College Station, TX 77843-3128

Email Address: jcoulon7@yahoo.com

Education: B.Sc., Electrical & Electronic Engineering, Kwame Nkrumah University of Science and Technology, 2009
M.S., Electrical Engineering, Texas A&M University, 2012.