A CURRENT BALANCING INSTRUMENTATION AMPLIFIER (CBIA) BIOAMPLIFIER WITH HIGH GAIN ACCURACY

A Thesis

by

EBENEZER POKU DWOBENG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2011

Major Subject: Electrical Engineering

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Bioamplifier with High Gain Accuracy

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Approved by:

Co-Chairs of Committee,	Edgar Sanchez-Sinencio
	Kamran Entesari
Committee Members,	Deepa Kundur
	Walker Duncan Henry
Head of Department,	Costas Georghiades

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ABSTRACT

A Current Balancing Instrumentation Amplifier (CBIA)

Bioamplifier with High Gain Accuracy. (December 2011)

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Co-Chairs of Advisory Committee: Dr. Edgar Sanchez-Sinencio
Dr. Kamran Entesari

Electrical signals produced in the human body can be used for medical diagnosis and research, treatment of diseases, pilot safety etc. These signals are extracted using an electrode (or transducer) to convert the ion current in the body to electron current. After the electrode, the very low amplitude extracted signal is amplified by an analog frontend that typically consists of an instrumentation amplifier (IA), a programmable gain amplifier (PGA), and a low pass filter (LPF). The output of the analog frontend is converted to digital signal by an analog to digital converter (ADC) for subsequent processing in the digital domain.

This thesis discusses the circuit design challenges of the analog frontend instrumentation amplifier, compares existing circuit topologies used to implement the IA and proposes a new frontend IA. The proposed circuit uses the Current Balancing Instrumentation Amplifier (CBIA) topology to achieve high gain accuracy over a wide range of the output impedance. In addition it uses common circuit design techniques such as chopper modulation to achieve low flicker noise corner frequency, high common

mode rejection (CMR) and low noise efficiency factor (NEF). The proposed circuit has been implemented in the 0.5um CMOS ON-semiconductor process and consumes 16uW of power. The post-layout simulated gain accuracy is better than 94% for gain values from 20dB to 60dB, measured NEF is 7.8 and CMRR is better than 100dB.

DEDICATION

I dedicate this thesis to my mother, Rose Kusi and my entire family.

ACKNOWLEDGEMENTS

I would like to thank God for protecting me over the years I spent on Texas A&M campus.

I will also like to thank my advisor, Dr Edgar Sanchez-Sinencio for his technical guidance and the support he offered me during my course of study. Special thanks also to the members of my advisory committee, Dr Kamran Entesari, Dr Deepa Kundur and Dr Walker Duncan Henry for their input to my research.

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Finally I want to thank my entire family for all the love they showed me.
This day will not have materialized without all of you. THANK YOU VERY MUCH!!!

NOMENCLATURE

CBIA	Current Balancing Instrumentation Amplifier
IA	Instrumentation Amplifier
NEF	Noise Efficiency Factor
DEO	Differential Electrode Offset
PSD	Power Spectral Density
PGA	Programmable Gain Amplifier
UGF	Unity Gain Frequency
LPF	Low Pass Filter
BJT	Bipolar Junction Transistor

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1. INTRODUCTION:

BIOLOGICAL SIGNAL MONITORING SYSTEMS

Several electrical signals can be found in the body and they can be classified based on where they are generated. EEG, ECG and EMG are common extracted biological signals that are generated in the brain, heart and skeletal muscles respectively. A block diagram of a complete system for extracting these signals is shown in Figure 1.

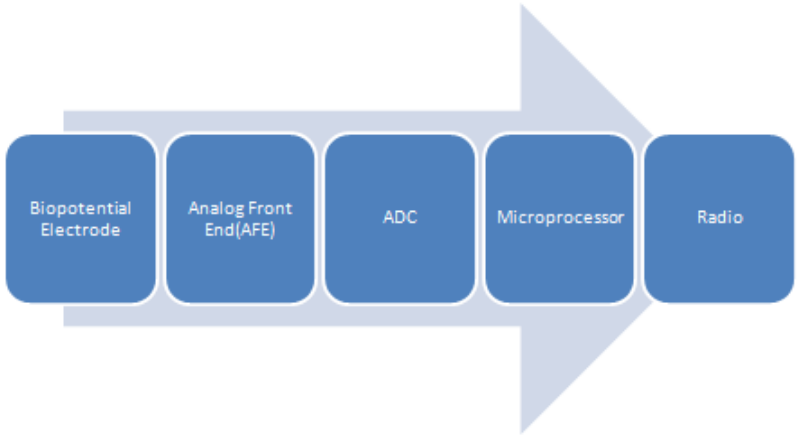

Figure 1: Block diagram of a complete biopotential monitoring system

The biological signal monitoring system consists of a transducer (or electrode),

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This thesis follows the style of *IEEE Journal of Solid- State Circuits*.

an analog readout frontend, an analog to digital converter, a microprocessor and an optional radio for transmission in wireless systems [1]. The analog readout frontend is used to amplify the biological signal of interest and reject out of band signals and in-band interferences. A typical analog readout frontend consists of an instrumentation amplifier (IA), a lowpass filter and a Programmable gain amplifier (PGA). The design requirements of the frontend instrumentation amplifier in the analog readout frontend include accurate gain, dc rejection, high common mode rejection, low power and high input impedance.

1.1) Design Requirements of the Frontend Instrumentation Amplifier

1.1.1) Gain

Perhaps the most important attribute of instrumentation amplifiers is that they have a well defined gain. The gain of the frontend IA must be large enough to amplify the input signal above the noise level of the following stages in the signal acquisition system. The gain must also be constant over the entire input signal's amplitude and frequency range to minimize distortion. An adjustable gain is preferred over a fixed gain because the former allows the input dynamic range of the IA to be optimized for various types of biological signals. The gain of IA's is set by the ratio of resistors or capacitors so it can be adjusted easily by varying this ratio.

The gain accuracy of an instrumentation amplifier is how close the measured gain (or actual gain) is to the ideal gain as defined by the resistor or capacitor ratio. It is calculated by taking the ratio of the measured gain to the ideal gain. Gain accuracies

close to 1 (or 100%) are desirable because the gain will then be insensitive to process, voltage and temperature (PVT) variations.

1.1.2) DC Rejection

The contact electrodes used to extract biological signals are equivalent to a chemical half cell (or an electrode-electrolyte system). As a result of the chemical reactions between the electrode and the electrolyte in the body, a dc voltage called half cell potential develops. When biological signals are extracted differentially, the difference in this half cell potential developed by the two electrodes creates a differential dc offset voltage known as differential electrode offset (DEO). Also very low frequency signals are created by motion artifacts at the skin-electrode interface. DEO and motion artifacts usually have very large amplitudes that can saturate the analog readout frontend. Consequently the frontend IA should have a high pass frequency response with corner frequency that can be as low as 0.01Hz to filter out DEO and motion artifacts. Table 1 shows the bandwidth requirements of some common biological signals.

Several techniques for rejecting dc and low frequency motion artifacts in bioamplifiers exist. Bioamplifiers based on operational amplifiers in voltage feedback with capacitors as the feedback elements [2] have an inherent dc rejection that can be implemented on-chip but they suffer from low common mode rejection that is dependent on the matching of the capacitors. Other on-chip dc rejection methods use a dc servomechanism [3,4]. These methods increase the power consumption of the frontend amplifier, degrade the input impedance and have a maximum DEO limit they can reject.

As a result DEO rejection is usually done with an off-chip high pass filter [1] which for multichannel biological signal recording, increases the external component count exponentially.

Table 1: Bandwidth requirements of common biological signals

Biological Signal	Bandwidth
Electroencephalogram (EEG)	0.5-42Hz
Electrocardiogram (ECG)	0.67-40Hz
Electromyogram (EMG)	2-500Hz
Electrogastogram (EGG)	0.01-0.55Hz

1.1.3) High Common Mode Rejection Ratio (CMRR)

In differential signal processing, the difference between two signals at the input is amplified and their sum (or common mode) is rejected. The ratio of the differential signal gain to the common mode signal gain is the common mode rejection ratio (CMRR). In biological signal recording systems, the most important common mode signal is due to 50/60Hz coupling from the power lines (or mains). This common mode signal can be larger than the desired biological signal. Thus some recording systems use a separate notch filter centered at 50/60Hz to remove this common mode interference [5]. This approach increases the power consumption and complexity of the front-end IA.

To improve the common mode rejection, other bioamplifiers incorporate body

potential drivers [5]. Body potential drivers use a differential amplifier to compare the output common mode signal to a zero reference signal. The differential amplifier produces an error signal that is injected to the input common mode point to force the output common mode signal to zero. Since body potential drivers involve injecting signals into the patient's body, care must be taken not to exceed safe current limits defined by the UL544 standard [6].

Chopper modulated bioamplifiers also achieve very high CMRR. In every differential amplifier, mismatches in the circuit elements results in the conversion of common mode signals to differential signals at the output that degrades the CMRR. In a chopper modulated bioamplifier, the output chopper up-converts this undesirable differential signal to a higher frequency and away from the desired operating frequency band. This is illustrated in Figure 2

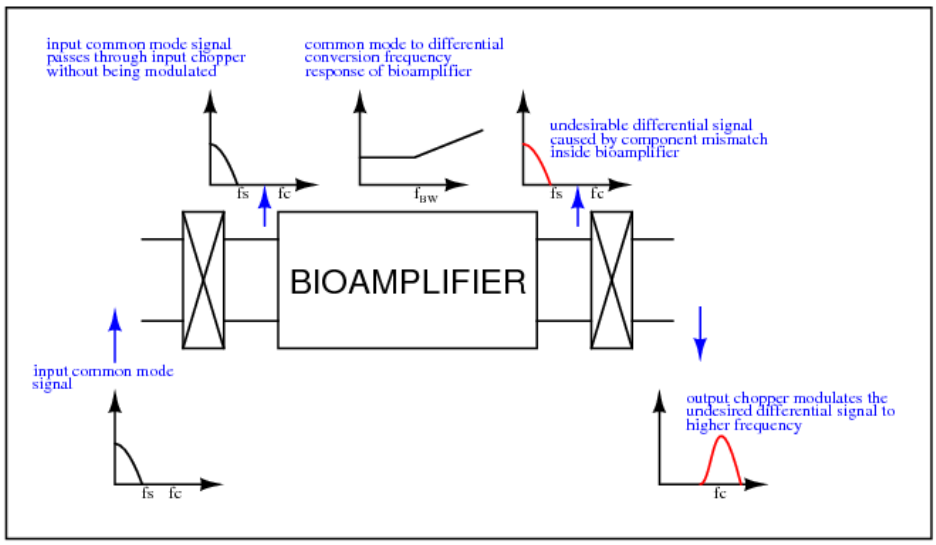

Figure 2: Illustration of high CMRR in chopper modulated bioamplifiers

1.1.4) Low Noise

Noise refers to the random amplitude signals that appear at the output of a circuit when no signal is present at the input. Noise can be classified into two; thermal noise and flicker noise based on how it is generated. Thermal noise is caused by the thermal agitation of the charge carriers (electrons and holes) and it has a white spectrum. In MOS devices, flicker noise is caused by charge carriers being trapped in cavities in the oxide layer. Because flicker noise power reduces as the signal frequency increases, it is commonly referred to as 1/f noise [7].

The frontend IA's noise sets a limit on the minimum input signal amplitude that can be processed. Because the amplitude of biological signals is very small, the noise of the IA has to be low. The noise of most bioamplifiers is dominated by the low frequency flicker noise of MOS devices. Thus these MOS devices in bioamplifier circuits have large areas to minimize their flicker noise contribution. Also some bioamplifiers use chopper modulators to upconvert the low frequency biological signal to a higher frequency where the effect of flicker noise is negligible. Subsequently after amplification, the modulated signal is demodulated to the original frequency at the output of the bioamplier.

Current splitting techniques [8]-[10] can be used to improve the transconductance of a conventional differential pair and thus reduce the input referred thermal noise but at the cost of reduced slew rate and phase margin. Source degeneration [8] can also be used to reduce the thermal noise current of CMOS active loads by

reducing their transconductance but at the cost of reduced voltage headroom. Table 2 compares some of the common noise reduction techniques:

Table 2: Comparison of various techniques to reduce circuit noise

	chopper modulation	current splitting	source degeneration
Reduces Thermal noise	no	yes	yes
Reduces Flicker noise	yes	no	no
Does not reduce circuit speed	yes	no	yes
Does not reduce voltage headroom	yes	yes	no

1.1.5) High Input Impedance

High input impedance ensures the maximum transfer of voltage to the input of the bioamplifier and also minimizes the current flowing through the input circuit. Depending on the type of electrode used to extract the biopotential signal, the input impedance requirements of the bioamplifier can range from a few kilo-ohms to several giga-ohms [11].

1.1.5.1) Biopotential Electrodes

Because the charge carriers in the biological medium (ions) and the bioamplifier circuit (electrons) are different, a transducer is required to transfer the biological signals

to the frontend circuit. This transducer is the biopotential electrode and it converts ionic current (in the body) to electron/hole current (in the bioamplifier). Shown in Figure 3 is the electrical equivalent circuit of a biological electrode. It comprises of a resistor and capacitor in parallel [11]. This impedance forms a voltage divider with the input impedance of the bioamplifier and causes signal attenuation. Apart from the electrode, the impedance of the skin also causes further attenuation of the input signal. For an area of $1cm^2$, the skin impedance is in the range of 200kΩ at 1Hz to 200Ω at 1MHz [5]. In some applications, special treatment of the skin may be required to further reduce its impedance and thus minimize signal attenuation.

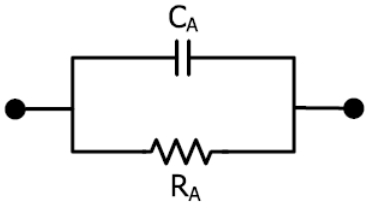

Figure 3: Electrical equivalent circuit of a biopotential electrode

A biopotenial electrode may be classified as wet, dry or non-contact electrode. Wet electrodes, such as Ag/AgCl electrodes are mostly resistive (purely resistive electrodes are referred to as non-polarizable electrodes) whiles non-contact electrodes are mostly capacitive (purely capacitive electrodes are referred to as polarizable electrodes) [11]. Table 3 shows typical impedances of some common biopotential electrodes [12].

Table 3: Impedance of some common biopotential electrodes

Electrode	$R_A(\Omega)$	C_A
Wet (Ag/AgCl)	350k	25nF
Metal plate	1.3M	12nF
Thin film	550M	220pF
Cotton	305M	34pF

1.1.6) NEF and Power Consumption

Noise efficiency factor (NEF) is a common figure of merit used to compare different bioamplifiers. It is the ratio of the total input referred noise of an IA to the total input referred noise of a common emitter BJT amplifier that consumes the same power as the IA. It was first proposed by [13] and is calculated from the expression;

$$NEF=v_{in_{rms}}\sqrt{\frac{2I_{total}}{\pi 4kT(v_{th})BW}} \tag{1.1}$$

Figure 4 is a chart showing the relative power consumption and noise contribution of the various blocks of a typical biopotential monitoring system [1]. The power consumed by the analog frontend accounts for about 2% of the total power consumption, hence the absolute power consumed by the front end IA is not very critical. Likewise because the noise power of the ADC and the radio gets divided by the square of the gain of the frontend amplifier, their noise contributions are also not very critical. Usually front-end instrumentation amplifiers are compared using their NEF and

not their absolute power consumption or noise contribution. The ideal value of NEF is 1.

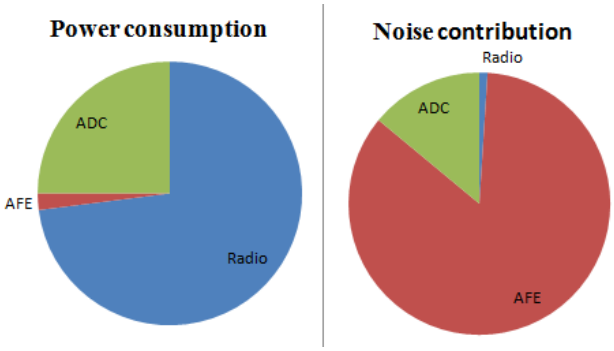

Figure 4: Distribution of power consumption and noise of a complete monitoring system

In summary, the frontend instrumentation amplifier must extract very weak biopotential signals in the presence of high polarizing dc voltage (or differential electrode offset (DEO)), circuit noise and large common mode interference caused by 50/60 Hz coupling from the mains. The IA should provide minimum signal distortion consume minimum power and amplify the very weak biopotential signals above the noise floor of the following signal processing stages. To achieve these performances, the frontend IA must be designed to have high common mode rejection ratio (CMRR), low noise, dc rejection, high input impedance and high gain accuracy. Table 4 gives the standard requirements (defined by AAMI ANSI) of a frontend bioamplifier suitable for the extraction of ECG signals [1].

Table 4: AAMI ANSI standard requirements for bioamplifiers suitable for extracting ECG signals

Input dynamic range	**± 5mV**
Input referred noise	< 60uVpp
Input impedance	> 2.5MΩ
CMRR	> 80dB
DEO filtering range	> ±300mV

2. INSTRUMENTATION AMPLIFIER ARCHITECTURES

Three commonly used instrumentation amplifiers are the 3-Opamp IA, switched capacitor IA and the current balancing instrumentation amplifier (CBIA).

2.1) 3-Opamp IA

Operational amplifiers (OPAMP) are not often used in open loop because their open loop gain is not stable (very sensitive to process, voltage and temperature (PVT) variations). Instead they are used in closed loop and the gain of the closed loop system is set by the ratio of resistors (or capacitors). Shown in Figure 5 below is a difference amplifier consisting of an OPAMP in feedback.

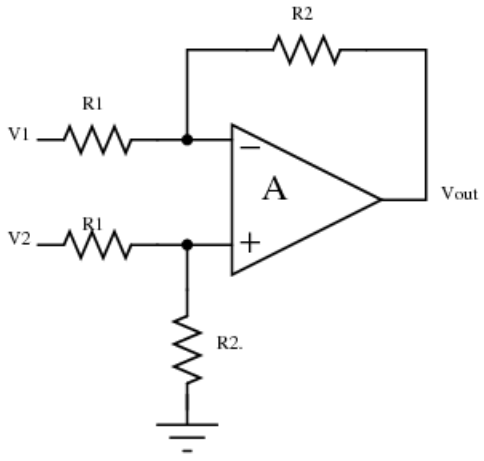

Figure 5: Circuit diagram of a difference amplifier

If A is the OPAMP gain, then the actual gain of the closed loop system for differential signals (A_{vd}) is given by

$$A_{vd} \cong \frac{R2}{R1}\left(1-\frac{1}{A}\left(1+\frac{R2}{R1}\right)\right) \tag{2.1}$$

For large open loop gain (A), the gain of the feedback system approaches the resistor or capacitor ratio $\left(\frac{R2}{R1}\right)$. However increasing the gain of the Opamp destabilizes the closed loop system and the bandwidth has to be reduced accordingly to ensure stability.

2.1.1) Effect of resistor mismatch on the Common Mode Rejection

With perfectly matched resistors, the common mode gain of the difference amplifier in Figure 5 is zero and consequently it achieves a theoretical CMRR of infinity. However, due to process variations, the resistor values are not perfectly matched in an actual implementation.

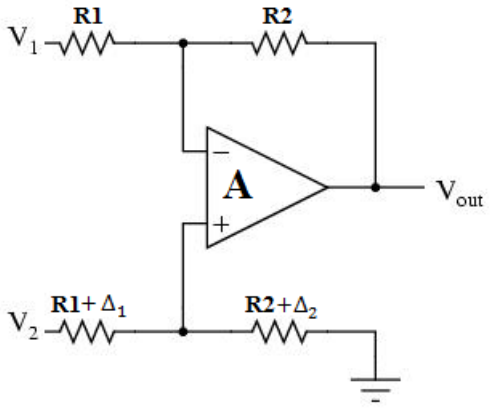

Figure 6: Difference amplifier with mismatch in the values of the resistors

Shown above in Figure 6 is a circuit diagram of a difference amplifier with mismatch in the resistor values. The signal flow block diagrams of the difference amplifier for differential and common mode input signals are given below in Figure 7 and Figure 8 respectively:

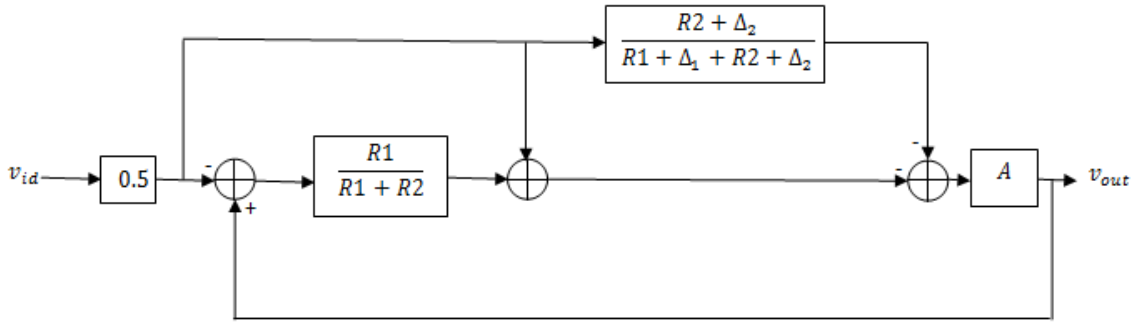

Figure 7: Block diagram of difference amplifier with mismatch (for differential input signals)

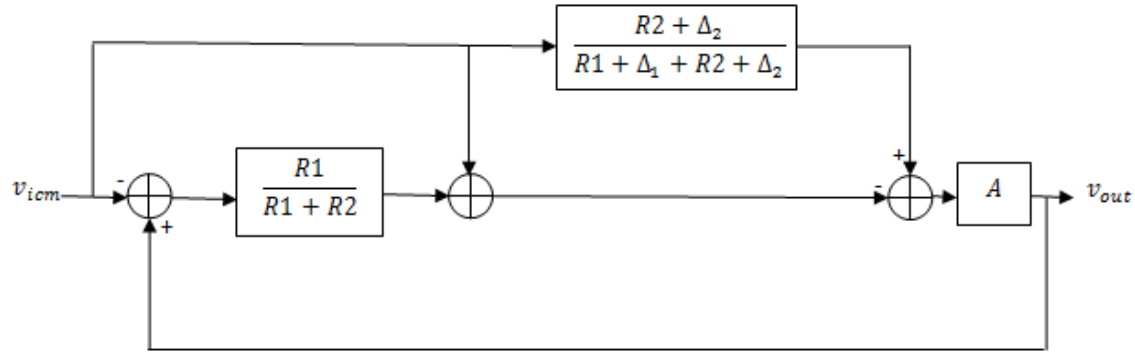

Figure 8: Block diagram of difference amplifier with mismatch (for common mode input signals)

Applying Masons gain rule [14] to the block diagrams above

$$\frac{v_{out}}{v_{id}} = \frac{1}{2}\left[\frac{\frac{R1A}{R1+R2} - A - \frac{(R2+\Delta_2)A}{R1+R2+\Delta_1+\Delta_2}}{1+\frac{R1A}{R1+R2}}\right] \tag{2.2}$$

$$\frac{v_{out}}{v_{icm}} = \left[\frac{\frac{R1A}{R1+R2} - A + \frac{A(R2+\Delta_2)}{R1+R2+\Delta_1+\Delta_2}}{1+\frac{R1A}{R1+R2}}\right] \tag{2.3}$$

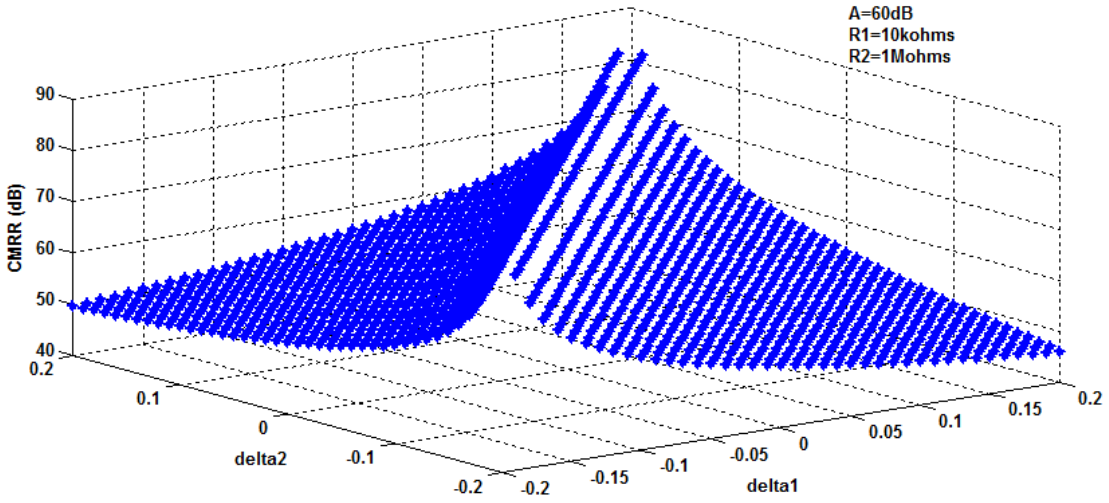

Figure 9: Variation of CMRR in a difference amplifier with resistor mismatch

Shown in Figure 9 above is a plot of the common mode rejection ratio for resistor mismatch values (Δ_1 and Δ_2) between -20% to +20% of their ideal values. The CMRR increases as the difference between Δ_1 and Δ_2 decreases and the maximum CMRR occurs when this difference is zero (i.e. $\Delta_1=\Delta_2$). Thus to obtain a high CMRR in the

difference amplifier requires that the resistors are carefully matched so as ensure minimum and uniform errors in the resistor values.

The difference amplifier shown in Figure 6 has very low input impedance ($Z_{in} \cong R1+R2$) that may not be adequate for most biopotential signal acquisition systems. Thus two voltage buffers are added as shown in Figure 10 to increase the input impedance. This circuit is the 3-Opamp IA. The gain of the 3-Opamp IA is given by

$$A_v = \left(1 + \frac{2R}{R_{gain}}\right)\frac{R2}{R1} \tag{2.4}$$

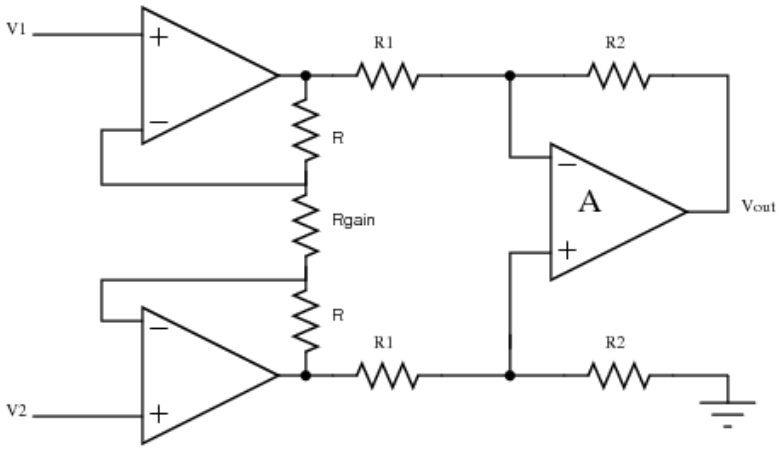

Figure 10: Circuit diagram of 3-opamp instrumentation amplifier

This circuit has an additional advantage that the gain can be varied by changing the value of a single resistor (R_{gain}). However, because of the high power consumption and noise level, the 3-Opamp IA is not suitable for biological signal recording where the

signal amplitudes are low and the device has to be used for a very long time (especially in implantable devices).

An alternate difference amplifier configuration with capacitors as the feedback elements are better suited for biological signal recording. Several reported bioamplifiers are based on this architecture [2, 8]. The inherent ac coupling effectively rejects differential electrode offset voltages (DEO). Also because the Opamp drives capacitive loads, it can be replaced with low power and low noise operational transconductance amplifiers (OTA). However the common mode rejection of this configuration is very poor and requires precise matching of the capacitors. It is difficult to achieve CMRR greater than 70dB with this architecture. Also varactors are not practical to implement at the low operating frequencies of bioamplifiers so they are normally designed for a fixed gain using parallel plate capacitors. Another disadvantage of this configuration is the tradeoff between area and gain; the higher the gain, the larger the capacitors and the larger the area consumed. Because of this, these circuits are rarely designed for gain values in excess of 40dB.

2.2) Switched Capacitor IA

After signal acquisition with the frontend IA, the extracted signal is digitized with an ADC for subsequent processing in the digital domain. Switch capacitor IA's have the advantage that because they are sampled data systems, a separate sample and hold circuit is not required during analog to digital conversion. Also offset and low

frequency noise reduction techniques such as autozeroing and correlated double sampling [15] can be implemented in switch capacitor IA's.

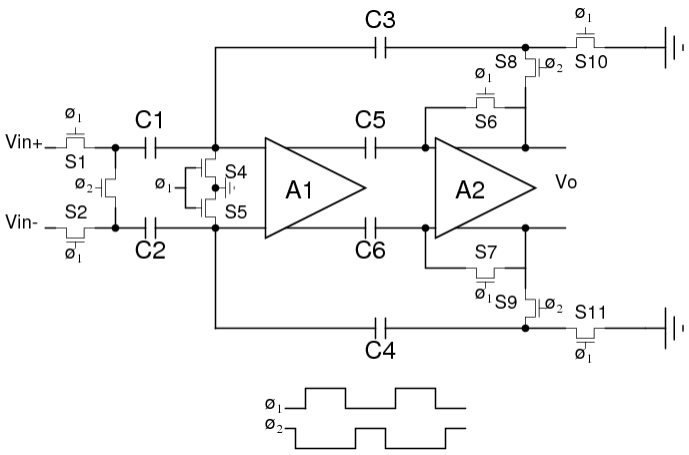

Figure 11: Circuit diagram of a switched-capacitor IA

Shown in Figure 11 is a switch capacitor IA proposed by [16]. The circuit operates in two phases ($\emptyset_1$and $\emptyset_2$). During phase 1, the sampling capacitors (C1 and C2) are charged to the value of the input voltage, the gain setting capacitors (C3 and C4) are discharged to ground and the offset storage capacitors (C5 and C6) store the output offset of amplifiers A1 and A2. The gain of A1 is designed to be low so that it does not get saturated by its offset voltage during phase 1. Charge redistribution occurs during phase 2. The gain setting capacitors (C3 and C4) get charged by the charge difference between C1 and C2. Common mode signals are thus rejected. If C1 equals C2 and C3 equals C4, the gain of this circuit is given by the ratio of C3 to C1 (or C4 to C2).

From the principle of charge conservation, the total charge in phase 1 must be equal to the total charge in phase 2.

$$\text{Total charge during phase 1 } (Q_{total1}) = v_{in}C1 \tag{2.5}$$

During phase 2, the feedback loop forces the voltage across C1 to zero and consequently, C1 looses all the charge it acquired to C3.

$$v_o C3 = v_{in} C1 \tag{2.6}$$

$$\frac{v_o}{v_{in}} = \frac{C3}{C1} \tag{2.7}$$

In practice, several sources of non-idealities such as mismatch in the capacitors, charge injection, clock feedthrough and finite open loop gain cause errors in the voltage gain expression given by (2.7).

2.2.1) Charge Injection and Clock Feedthrough

In Figure 11, as the phase 1 switches turn on, the phase 2 switches turn off and vice versa. When the phase 2 MOS switches are turning off, the charge stored on their parasitic capacitances are discharged unto the sampling capacitors (C1 and C2) and this causes an error in the sampled input voltage. This phenomenon is referred to as charge injection.

The clock signal can also cause errors in the sampled voltage through a process called clock feedthrough. The gate to source (and gate to drain) parasitic capacitance of the MOS switches form a voltage divider with the effective capacitance from their respective source terminals to ground (or drain terminals to ground). Consequently the

clock signal can cause undesired variations in the sampled signal. Errors due to charge injection and clock feedthrough can be reduced with a balanced architecture.

2.2.2) Autozeroing and Correlated Double Sampling

Autozeroing (AZ) and Correlated double sampling (CDS) are common techniques used to reduce the offset and low frequency noise in sampled data systems. In autozeroing, during the sampling phase, the output offset is measured and a control signal is generated that is used to force the offset voltage to a very small value. This offset nulling control signal is stored. Consequently during the signal amplification stage, the sampled signal is amplified by an amplifier with very low offset. In CDS, the amplifier's offset voltage is sampled and stored during the sampling phase. During the amplification stage, the input signal plus the offset are sampled and the stored offset voltage is subtracted from this value. Both techniques are effective at reducing the dc offset and low frequency noise of the amplifier. However they result in an increase in the thermal noise floor because high frequency noise are undersampled causing them to fold-over to lower frequencies [15].

2.3) Current Balancing Instrumentation Amplifier (CBIA)

2.3.1) General Theory of CBIA

Figure 12 shows the general topology of a current balancing instrumentation amplifier (CBIA). It consists of an input transconductance stage driving an output impedance stage.

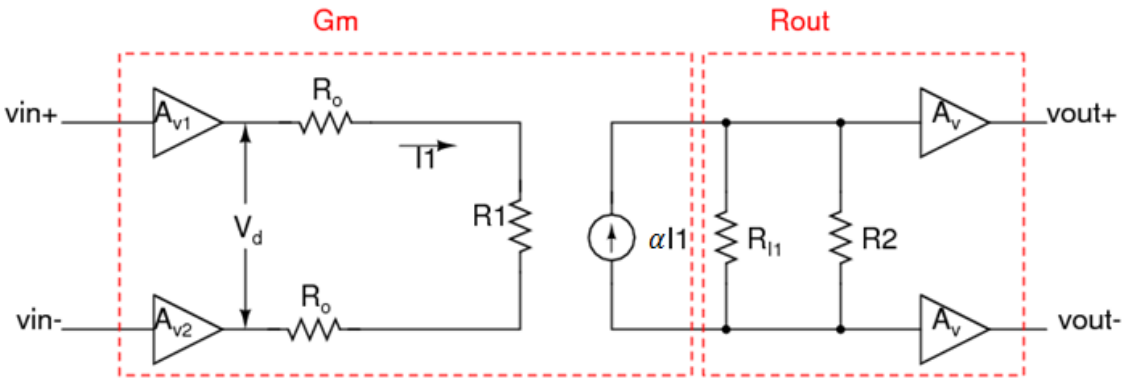

Figure 12: General topology of CBIA

Where Ro→ output impedance of the input buffers;R_{I1}→finite output impedance of the current source (I_1); αI_1→ ratio of current in the output stage to the current in the input stage; R1 and R2→ gain setting resistors; A_v→ finite gain of input and output buffers

From the circuit above in Figure 12, the output voltage is given by,

$$(v_{out}^{+}-v_{out}^{-})=A_v[\alpha I1(R_{I1}\|R2)] \text{ and } I1=A_v\left(\frac{v_d}{R1+2R_o}\right)$$

$$v_{out}=(v_{out}^{+}-v_{out}^{-})=\alpha A_v v_d\left(\frac{R2\|R_{I1}}{R1+2R_o}\right) \quad (2.8)$$

$$=G_m R_{out} v_d$$

$$G_m=\left(\frac{\alpha}{R1+2R_o}\right)\cong\frac{1}{R1}\left[\alpha\left(1-\frac{2R_o}{R1}\right)\right] \text{ for small } R_o \quad (2.9)$$

$$R_{out}=A_v(R2\|R_{I1})\cong R2\left[A_v\left(1-\frac{R2}{R_{I1}}\right)\right] \text{ for large } R_{I1} \quad (2.10)$$

where G_m→Effective transconductance and R_{out}→Output impedance

Substituting (2.9) and (2.10) into (2.8),

$$v_{out}=(v_{out}^{+}-v_{out}^{-})=\frac{R2}{R1}\alpha A_v v_d\left(\frac{1}{1+\frac{R2}{R_{I1}}}\right)\left(\frac{1}{1+\frac{2R_o}{R1}}\right)$$

$$=\frac{R2}{R1}\alpha A_v v_d\left(\frac{1}{1+\frac{R2}{R_{I1}}+\frac{2R_o}{R1}+\frac{R2}{R_{I1}}\frac{2R_o}{R1}}\right)$$

$$v_{out}\cong\frac{R2}{R1}\alpha A_v v_d\left[1-\left(\frac{R2}{R_{I1}}+\frac{2R_o}{R1}+\frac{R2}{R_{I1}}\frac{2R_o}{R1}\right)\right] \quad (2.11)$$

Also, the input signals can be expressed as the sum of the differential signal and common mode signal;

$$v_i^{+}=\frac{v_{id}}{2}+v_{icm};\ \text{and}\ v_i^{-}=-\frac{v_{id}}{2}+v_{icm}$$

$$\text{where}\ v_{id}=v_i^{+}-v_i^{-}\ \text{and}\ v_{icm}=\frac{v_i^{+}+v_i^{-}}{2}$$

Assuming that due to circuit mismatch, the gains of the input buffers are not equal and

$$A_{v2}=A_{v1}+\gamma$$

where γ is the mismatch in the gains of the input buffers

Applying superposition at the input of Figure 12,

$$v_d=v_{id}\left(A_{v1}+\frac{\gamma}{2}\right)+\gamma v_{icm} \quad (2.12)$$

Substituting (2.12) in (2.11)

$$v_{out} \cong \frac{R2}{R1} \alpha A_v \left[v_{id} \left(A_{v1} + \frac{\gamma}{2} \right) + \gamma v_{icm} \right] \left[1 - \left(\frac{R2}{R_{I1}} + \frac{2R_o}{R1} + \frac{R2}{R_{I1}} \frac{2R_o}{R1} \right) \right] \tag{2.13}$$

From (2.13), the differential gain is given by

$$\frac{v_{out}}{v_{id}} \Big|_{v_{icm}=0} = \frac{R2}{R1} \alpha A_v \left[A_{v1} + \frac{\gamma}{2} \right] \left[1 - \left(\frac{R2}{R_{I1}} + \frac{2R_o}{R1} + \frac{R2}{R_{I1}} \frac{2R_o}{R1} \right) \right] \tag{2.14}$$

In the ideal CBIA with ideal circuit elements, the voltage gain of the input and output buffers (A_v) and the current gain (α) are equal to 1. The output impedance (R_o) of the input buffers is zero and the output impedance (R_{I1}) of the current source (I1) is infinite. Thus the ideal differential voltage gain is given by.

$$\left[\frac{v_{out}^+ - v_{out}^-}{v_{in}^+ - v_{in}^-} \right]_{ideal} \cong \frac{R2}{R1} (1)(1) \left(1 + \frac{0}{2} \right) \left[1 - \left(\frac{R2}{\infty} + \frac{2(0)}{R1} + \frac{2(0)R2}{\infty(R1)} \right) \right]$$

$$= \frac{R2}{R1}$$

From (2.13), the common mode gain is also given by

$$\frac{v_{out}}{v_{icm}} \Big|_{v_{id}=0} = \frac{R2}{R1} \alpha A_v \gamma \left[1 - \left(\frac{R2}{R_{I1}} + \frac{2R_o}{R1} + \frac{R2}{R_{I1}} \frac{2R_o}{R1} \right) \right] \tag{2.15}$$

For common mode signals, the gain is directly proportional to the mismatch in the gain of the input buffers. If the input buffers are well matched, similar voltages appear across R1 (i.e. v_d=0). Consequently I1 is zero and the common mode signal is not transferred to the output. Since active devices can be well matched using layout techniques such as common centroid and interdigitization this IA topology has an inherent high common mode rejection. The above results for the general CBIA circuit are summarized in Table 5.

Table 5: Analytical expressions for the general CBIA circuit

Parameter	Expression
Transconductance (G_m)	$\frac{1}{R1}\left[\alpha\left(1-\frac{2R_o}{R1}\right)\right]$
Output Impedance (R_{out})	$R2\left[A_v\left(1-\frac{R2}{R_{I1}}\right)\right]$
Differential gain	$\frac{R2}{R1}\alpha A_v\left[A_{v1}+\frac{\gamma}{2}\right]\left[1-\left(\frac{R2}{R_{I1}}+\frac{2R_o}{R1}+\frac{R2}{R_{I1}}\frac{2R_o}{R1}\right)\right]$
Common mode gain	$\frac{R2}{R1}\alpha A_v\,\gamma\left[1-\left(\frac{R2}{R_{I1}}+\frac{2R_o}{R1}+\frac{R2}{R_{I1}}\frac{2R_o}{R1}\right)\right]$

To summarize the above discussions on the various instrumentation amplifier architectures, Table 6 compares the 3-OPAMP IA, the switched capacitor IA and the CBIA when used as the front-end amplifier in a biopotential acquisition system. The relevant properties compared are the power consumption, common mode rejection, input impedance and noise performance. Table 6 shows that the CBIA architecture is the most suitable front-end amplifier. When the CBIA is used with chopper modulators, the effect of low frequency 1/f noise can be significantly reduced. Also circuit layout techniques such as interdigitization, common centroid and the use of dummies can significantly reduce the effects of transistor mismatch.

Table 6: Comparison of different instrumentation amplifier topologies

Property	Three Opamp IA	SC IA	CBIA
Power Consumption	high	high	low
Common mode Rejection	dependent on matching of both passive elements and transistors	dependent on matching of both passive elements and transistors	dependent on matching of transistors only
Input Impedance	high	low	high
Noise	high	high	moderate

2.3.2) Equivalence of CBIA and a Common Source Amplifier

The small signal equivalent circuit of a common source amplifier with a transconductance of $\frac{1}{R_{in}}$ and an output impedance of R_{out} is shown below in Figure 13. The impedance parameters (Z-parameters) describing the general CBIA circuit in Figure 12 and the common source amplifier small signal equivalent circuit in Figure 13 are similar. This means that when the same input signal is applied to both circuits, their outputs will be the same. For both circuits in Figures 12 and 13,

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \infty & \frac{1}{R1} \\ \infty & R2//r_o \end{bmatrix} \tag{2.16}$$

$$Z_{11} = \frac{V_{in}}{i_{in}}\Big|_{i_{out}=0} \rightarrow \text{input impedance};\quad Z_{21} = \frac{V_{out}}{i_{in}}\Big|_{i_{out}=0} \rightarrow \text{transimpedance}$$

$$Z_{12} = \frac{V_{in}}{i_{out}}\Big|_{i_{in}=0} \rightarrow \text{transconductance};\quad Z_{22} = \frac{V_{out}}{i_{out}}\Big|_{i_{in}=0} \rightarrow \text{output impedance}$$

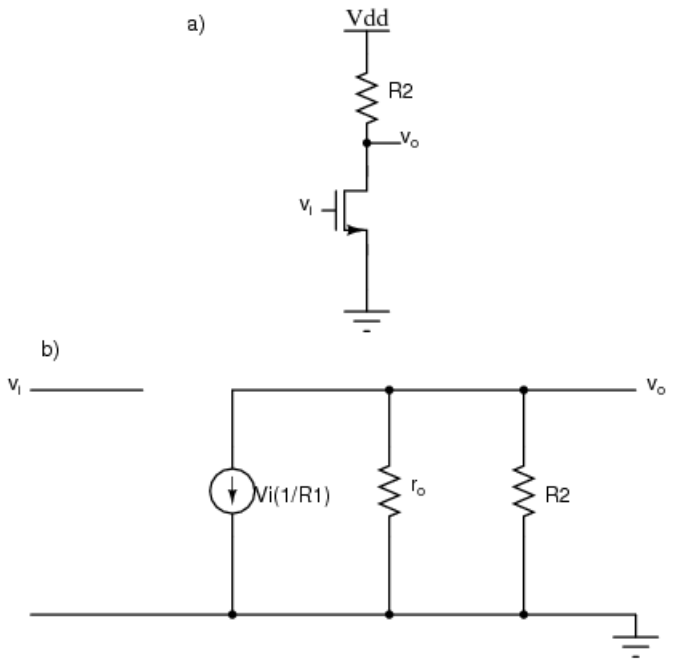

Figure 13: Common source amplifier circuit diagram (a) and small signal equivalent circuit (b)

However, unlike the common source amplifier, the transconductance and output impedance of a CBIA are not dependent on bias voltages, device dimensions or technology parameters such as carrier mobility or oxide capacitance. Instead the transconductance and output impedance of a CBIA are accurately set by resistor values.

2.4) Previous Work on CBIA in the Literature

2.4.1) CBIA Implementation by H. Krabbe [17]

Figure 14 shows the basic principle of operation of the CBIA circuit proposed in [17]. The difference voltage at the input of amplifier A1 is amplified by A1 and A2. The amplified voltage at the output of A2 (V_x) controls two identical voltage controlled

current sources (I1 (V_x)). With enough gain in the feedback loop, the input signal (v_i) at the positive terminal of A1 is pulled to the negative terminal. At steady state,

$$v_i = I1(R1) \tag{2.17}$$

where I1 is the steady state current of the current source I1(V_x)

Similarly with enough loop gain, the output voltage (v_o) gets pulled to the negative terminal of amplifier A2. At steady state

$$v_o = I3(R2) \tag{2.18}$$

where I3 is the steady state current of the current source I3(V_x)

From (2.18) and (2.19)

$$\frac{v_o}{v_i} = \frac{I3(R2)}{I1(R1)} \tag{2.19}$$

Thus, provided I1 is equal to I3, the voltage at the negative input terminal of A2 is given by

$$\frac{v_o}{v_i} = \frac{R2}{R1} \tag{2.20}$$

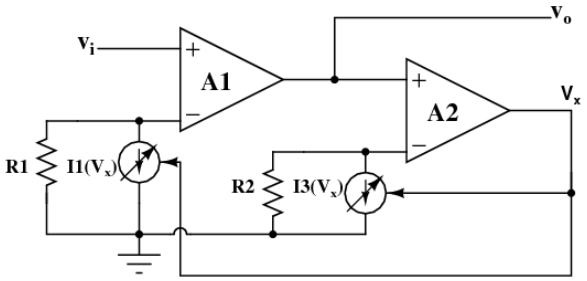

Figure 14: Concept of CBIA circuit by H. Krabbe

Shown in Figure 15 is the circuit implementation. For differential signals, the transfer function from the input to the output is given by

$$\frac{v_o}{v_i} = \frac{R2(I3\text{-}I4)}{R1(I1\text{-}I2)} \tag{2.21}$$

Consequently provided that I1 is matched to I3 and I2 is matched to I4, the voltage gain is the ratio of R2 to R1.

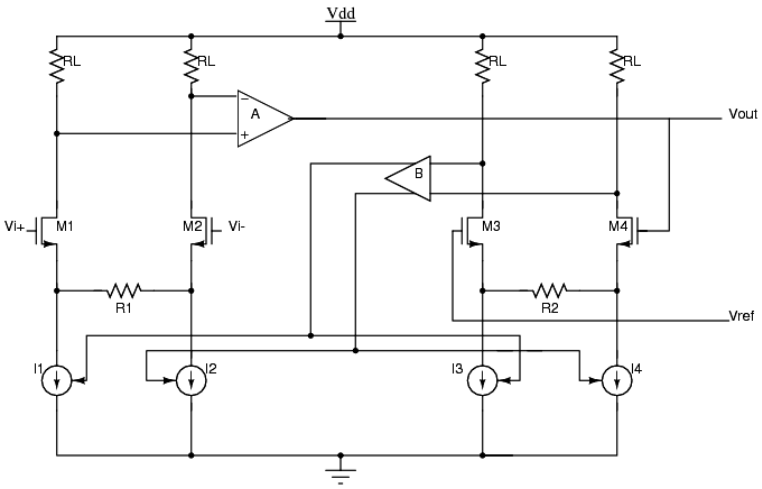

Figure 15: CBIA circuit implementation by H. Krabbe

2.4.2) CBIA implementation by P. Brokaw [18]

The circuit topology proposed by Krabbe in Figure 15 has a closed loop amplifier in the feedback path of another closed loop amplifier. This makes the frequency compensation very challenging [18]. A new circuit proposed by [18] solves this problem and improves the settling characteristics of the CBIA. This circuit is shown conceptually in Figure 16.

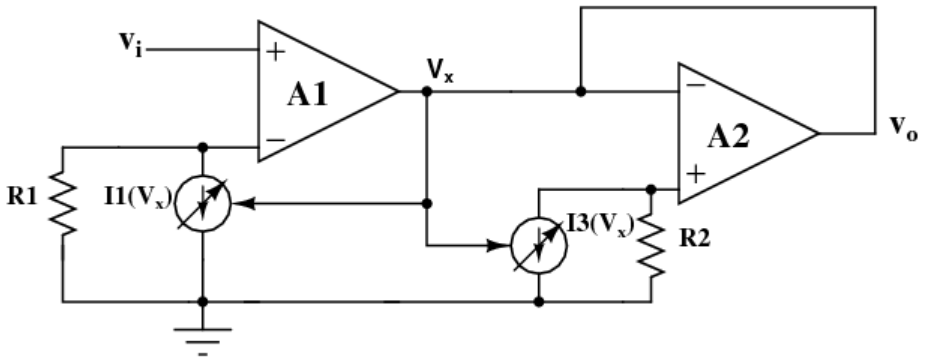

Figure 16: Concept of CBIA circuit by P. Brokaw

The principle of operation is similar to the concept in Figure 14. However, this implementation controls the current sources I1 and I3 from the output of the amplifier A1 instead of A2. Consequently, the gain of amplifier A1 (in Figure 16) must be equal to the product of A1 and A2 (in Figure 14) for the same gain accuracy. The circuit implementation is shown below in Figure 17:

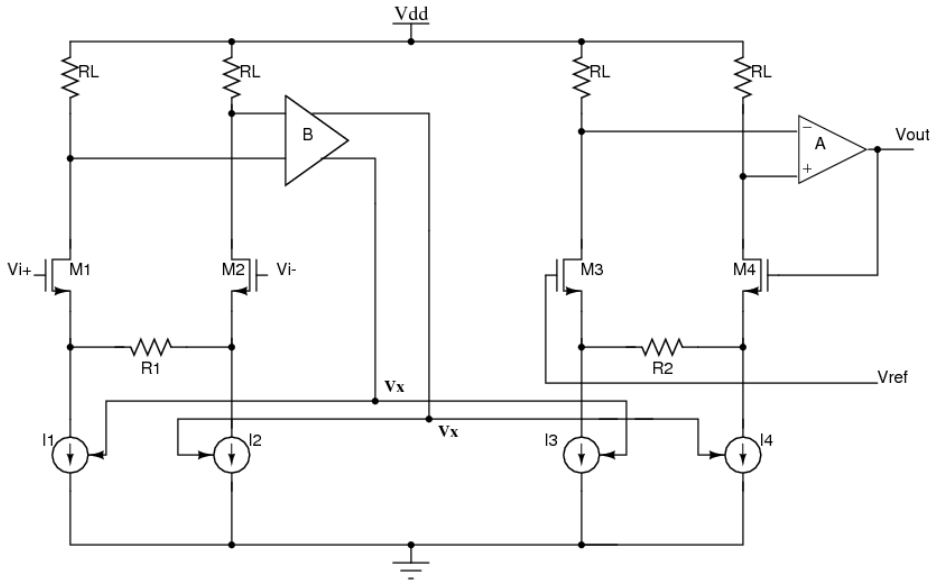

Figure 17: CBIA circuit implementation by P. Brokaw

2.4.3) CBIA implementation by M. Stayaert [13]

Another CBIA implementation is shown conceptually in Figure 18. The circuit proposed in [13] operates on this principle. The feedback loop forces the input signal at the positive terminal to be equal to the signal at the negative terminal of amplifier A1. At steady state

$$v_i = R1(g_m v_o) \tag{2.22}$$

where g_m is the transconductance of the voltage controlled current source ($I1(V_o)$)

From (2.22)

$$\frac{v_o}{v_i} = \frac{(1/g_m)}{R1} \tag{2.23}$$

The above expression in equation (2.23) implies that, if the transconductance (g_m) of the voltage controlled current source ($I1(V_o)$) is accurately set by a resistor $\left(\text{i.e.} g_m = \frac{1}{R2}\right)$ then the voltage transfer function from input to output is given by

$$\frac{v_o}{v_i} = \frac{R2}{R1} \tag{2.24}$$

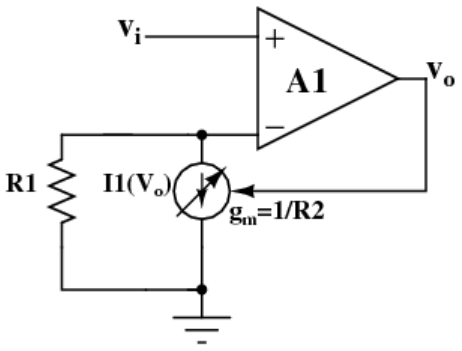

Figure 18: Concept of CBIA circuit by M. Stayaert

The advantage of this circuit is that the gain does not depend on the matching of current sources. To accurately set the gain as a resistor ratio $\left(\frac{R2}{R1}\right)$, the gain of amplifier A1 must be large enough to create a virtual short at its inputs and the transconductance of I1 must be accurately set to $\frac{1}{R2}$. The implementation in [13] is shown below in Figure 19. Transistors M2, M6, M8 and M10 form the amplifier A1 and M4 is the voltage controlled current source (I1). Resistor R2 is used to source degenerate transistor M4 and

thus set the transconductance of M4 to the value of R2. The transconductance of M4 is given by,

$$G_{m4}=\frac{1}{\frac{1}{g_{m4}}+\frac{R2}{2}}$$

$$\text{If } g_{m4} \gg \frac{2}{R2}, \text{ then } G_{m4}=\frac{2}{R2}$$

This condition leads to high power consumption if high gain accuracy is needed. Also the circuit consumes very large headroom due to the stacking of transistors and the diode connected transistors, M5 and M6. The OPAMPs and the external capacitor C_{ext} are used to set a high pass corner frequency for the circuit.

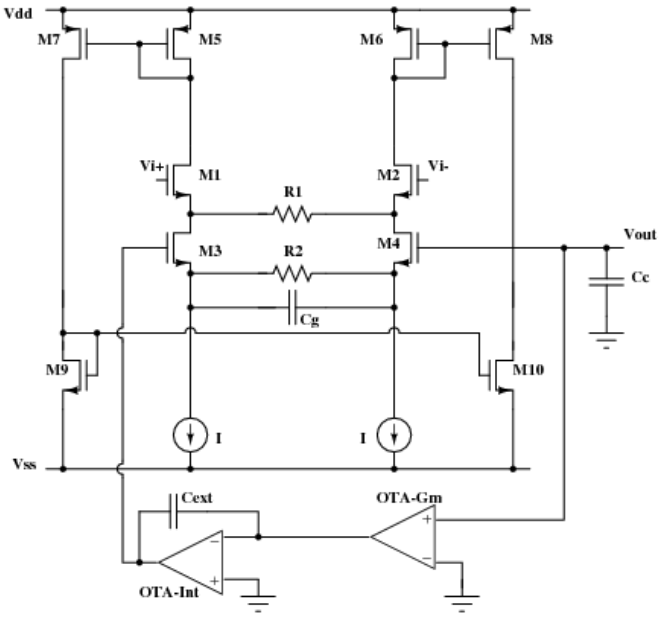

Figure 19: CBIA circuit implementation by M. Stayaert

2.4.4) CBIA implementation by R.F. Yazicioglu et al [4]

Shown in Figure 20 is the concept of implementation of the CBIA in [4]. The output of amplifier A1 (v_x) is used to drive a floating voltage controlled current source (I1 (v_x)).

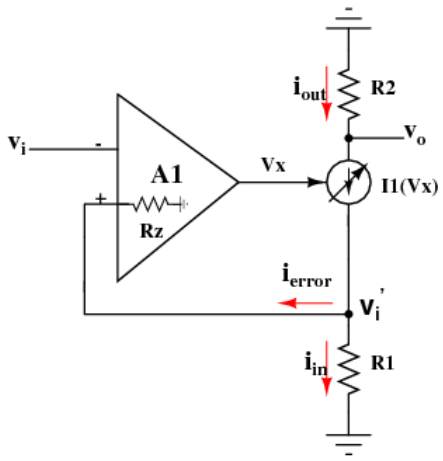

Figure 20: Concept of CBIA circuit by Yazicioglu et al

For the circuit in Figure 20, at steady state;

$$v_o = v_x g_{m,I1} R2 \tag{2.25}$$

where $g_{m,I1}$ is the small signal transconductance of $I1(v_x)$

$$\text{But } v_x = A1\left(v_i' - v_i\right) \tag{2.26}$$

$$\text{and } \left(v_i' - v_i\right) A1 g_{m,I1} (R1 // R_z) = v_i' \tag{2.27}$$

Solving for v_i' in equation (2.27),

$$v_i' = v_i \frac{A1 g_{m,I1}(R1 // R_z)}{1 + A1 g_{m,I1}(R1 // R_z)} \tag{2.28}$$

Substituting (2.28) into (2.26) and simplifying the resulting expression,

$$v_x = v_i \left(\frac{-1}{1 + A1 g_{m,I1}(R1 // R_z)} \right) \tag{2.29}$$

Substituting (2.29) into (2.25) and solving for the voltage gain $\left(\frac{v_o}{v_i}\right)$

$$\left(\frac{v_o}{v_i}\right) = - \frac{g_{m,I1} R2 A1}{1 + A1 g_{m,I1}(R1 // R_z)} \tag{2.30}$$

$$\cong - \frac{R2}{R1} \qquad \text{if } A1 g_{m,I1} R1 \gg 1 \text{ and } R_z \gg R1$$

For the conceptual circuit in Figure 20 to be stable, the transistor used to implement the voltage controlled current source I1 (v_x) must be connected such that the drain terminal is connected to resistor R1 and the source terminal is connected to resistor R2. Because of the inversion from the gate to the drain of a transistor, this ensures the feedback loop is negative. However, because the impedance at the drain of a transistor is high, this connection causes the error current (i_{error}) to be large and the overall gain accuracy of the circuit is reduced. The implementation of this CBIA concept in [4] is shown in Figure 21

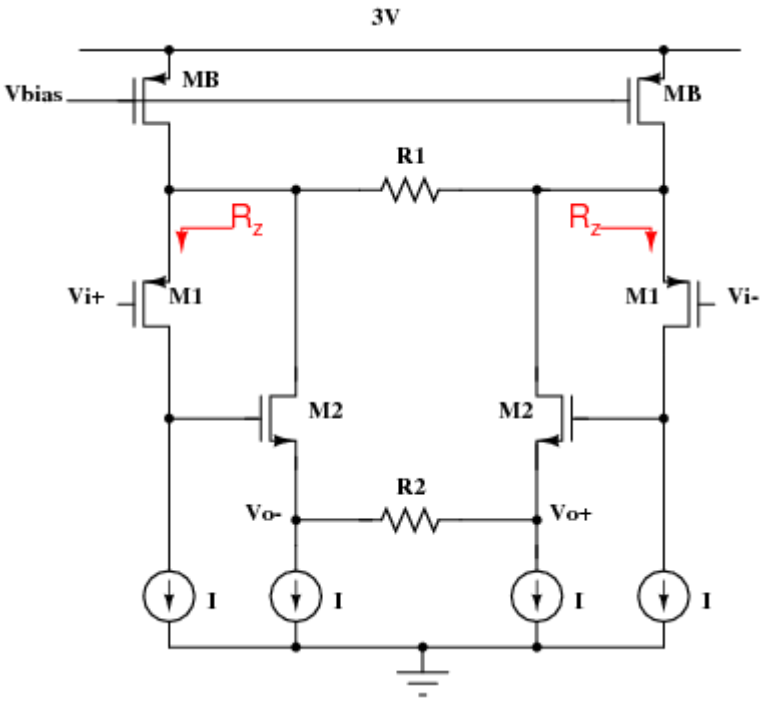

Figure 21: Simplified proposed CBIA implementation by Yazicioglu et al

For the implementation in Figure 21 above of the conceptual circuit in Figure 20, transistor M2 is the voltage controlled current source $I1(v_x)$ and the amplifier A1 is implemented with transistor M1 and current source I. The gate of M1 is the negative input, the source is the positive input and the drain terminal is the output of the amplifier A1. Consequently;

$$A1=g_{m1}r_{o1} \tag{2.31}$$

$$\text{and } g_{m,I1}=\frac{g_{m2}}{1+g_{m2}R2} \tag{2.32}$$

Substituting (2.31) and (2.32) into (2.30) and simplifying the resulting expression;

$$\frac{v_o}{v_i} = \frac{g_{m1} r_{o1} g_{m2} R2}{1 + g_{m1} r_{o1} g_{m2} R1 + g_{m2} R2}$$

$$\frac{v_o}{v_i} = -\frac{R2}{R1}\left[\frac{1}{1 + \frac{1}{R1 g_{m1} r_{o1}}\left(\frac{1}{g_{m2}} + R2\right)}\right]$$

$$\cong -\frac{R2}{R1}\left(1 - \frac{1 + g_{m2} R2}{g_{m2} R1 g_{m1} r_{o1}}\right) \qquad (2.33)$$

Shown below is a plot of the ideal gain, the simulated gain and the gain obtained from hand calculations for different values of the output resistor R2. The plots show that the gain accuracy (the ratio of the simulated (or actual) gain to the ideal gain) is very low if the circuit is designed for gain values higher than 10.

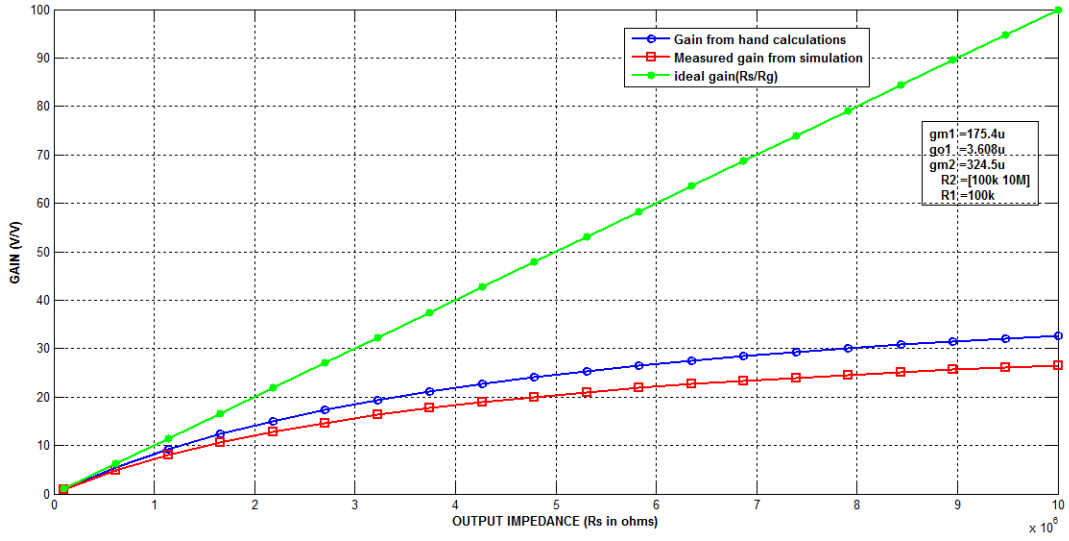

Figure 22: Ideal, simulated and hand calculated gain versus output impedance (R2) of CBIA by Yazicioglu et al

2.5) Proposed CBIA Circuit

2.5.1) Motivation

The proposed CBIA implementation in [4] suffers from poor gain accuracy when the ratio of R2 to R1 is greater than 10 (or 20dB) as seen in Figure 22. The goal of the proposed CBIA implementation is to solve this problem so that high gain accuracy is achieved for a wider range of $\frac{R2}{R1}$ in excess of 100 (or 40dB). If such high accuracy is achieved over the proposed range, the programmable gain amplifier (PGA) that is used to vary the gain of the analog frontend will no longer be necessary and this saves power, design time and reduces the complexity of the analog frontend.

2.5.2) Concept

Figure 23 shows the main idea behind the proposed circuit. To improve the gain accuracy, an inverting gain stage A2 has been added to the circuit in [4] causing the loop gain to increase and the difference signal at the input of A1 to reduce. Also because the signal is inverted by A2, the transistor used to implement the voltage controlled current source I1 (v_x) can be connected with the source terminal to resistor R1 and the drain terminal connected to resistor R2. Since the impedance seen at the source of a transistor is lower than the impedance seen at the drain terminal, this connection reduces the error current (i_{error}) and thus improves the gain accuracy of the implementation in [4]. For the conceptual circuit in Figure 23, the voltage gain $\left(\frac{v_o}{v_i}\right)$ is given by

$$\left(\frac{v_o}{v_i}\right) = -\frac{g_{m,I1} R2A1A2}{1+g_{m,I1} A1A2(R1//R_z)} \tag{2.34}$$

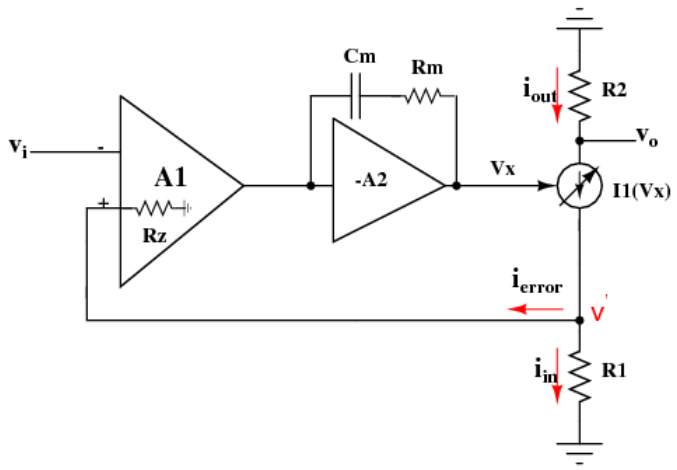

Figure 23: Concept of proposed CBIA circuit

2.5.3) Implementation

The implementation of the proposed circuit is shown in Figure 24. The floating voltage controlled current source I1 (v_x) in the conceptual circuit in Figure 23 is implemented with transistor M4 and the amplifier A1 is implemented with transistors M1 and M5. Transistors M2, M6, M3 and resistor (R_{I2}) form the amplifier A2. The resistor R_{I2} is the output impedance of a PMOS current source. Consequently,

$$g_{m,I1} = \frac{g_{m4}}{1+R1 g_{m4}} \tag{2.35}$$

$$A1=\frac{g_{m1}}{g_{o1}+g_{o5}} \tag{2.36}$$

$$A2=\left(\frac{g_{m2}}{g_{o2}+g_{o6}}\right)\left(\frac{g_{m3}R_{I2}}{1+g_{m3}R_{I2}}\right) \tag{2.37}$$

Substituting (2.35), (2.36) and (2.37) into (2.34)

$$\left(\frac{v_o}{v_i}\right)=-\frac{R2\left[\frac{g_{m4}}{1+R1g_{m4}}\right]\left[\frac{g_{m1}}{g_{o1}+g_{o5}}\right]\left[\left(\frac{g_{m2}}{g_{o2}+g_{o6}}\right)\left(\frac{g_{m3}R_{I2}}{1+g_{m3}R_{I2}}\right)\right]}{1+[R1//R_z]\left[\frac{g_{m4}}{1+R1g_{m4}}\right]\left[\frac{g_{m1}}{g_{o1}+g_{o5}}\right]\left[\left(\frac{g_{m2}}{g_{o2}+g_{o6}}\right)\left(\frac{g_{m3}R_{I2}}{1+g_{m3}R_{I2}}\right)\right]} \tag{2.38}$$

Assuming that $R_z \gg R1$;

$$\cong-\frac{R2}{R1}\left(1-\frac{1}{R1\left[\frac{g_{m4}}{1+R1g_{m4}}\right]\left[\frac{g_{m1}}{g_{o1}+g_{o5}}\right]\left[\left(\frac{g_{m2}}{g_{o2}+g_{o6}}\right)\left(\frac{g_{m3}R_{I2}}{1+g_{m3}R_{I2}}\right)\right]}\right) \tag{2.39}$$

Comparing equations (2.39) and (2.33), the error in the voltage gain of the proposed CBIA circuit is independent on the value of the output resistance (R2) whiles the voltage gain error in the implementation in Figure 22 increases with increasing R2. Consequently, the proposed implementation can achieve high gain accuracy over a wider range of the output resistance (R2) than the implementation in [4].

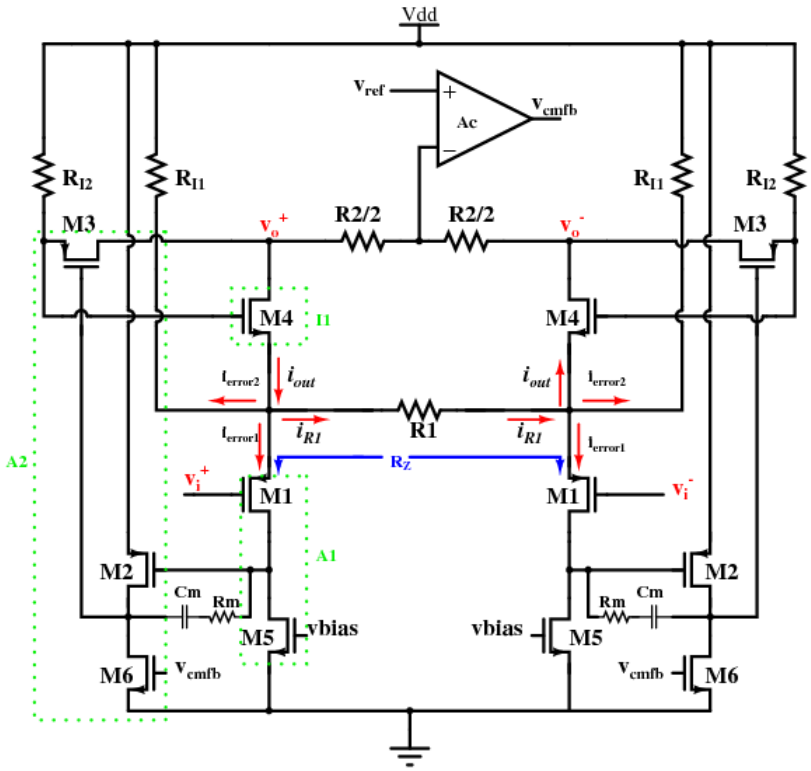

Figure 24: Implementation of proposed CBIA circuit

2.5.4) Tradeoffs

From Figure 23, the added gain stage A2 causes the loop gain to increase and this improves upon the gain accuracy of the CBIA. However, because of the increased loop gain, the circuit becomes unstable and some form of frequency compensation is required to achieve stability. Also because the drain of the voltage controlled current source $\left(I1(v_x)\right)$ is connected to the output, a common mode feedback circuit is needed to define the dc bias at the output. The added amplifier A2 and the common mode feedback circuit A_c cause the power consumption of the bioamplifier to increase. However, these

design tradeoffs can be justified because the need for a programmable gain amplifier (PGA) in the analog frontend can be avoided because of the high gain accuracy that can be achieved over a wide range with the proposed CBIA implementation. This helps to save power in the entire analog frontend circuit.

3. THEORY OF PROPOSED CIRCUIT:

SMALL SIGNAL ANALYSIS

The small signal analysis below uses the half circuit of the fully balanced fully differential circuit in Figure 24 to derive expressions for the small signal output impedance, transconductance and voltage gain of the proposed CBIA circuit. The half circuit is obtained by drawing a line of symmetry through the fully differential circuit and connecting the nodes that intersect the line of symmetry to ground.

3.1 Output Impedance

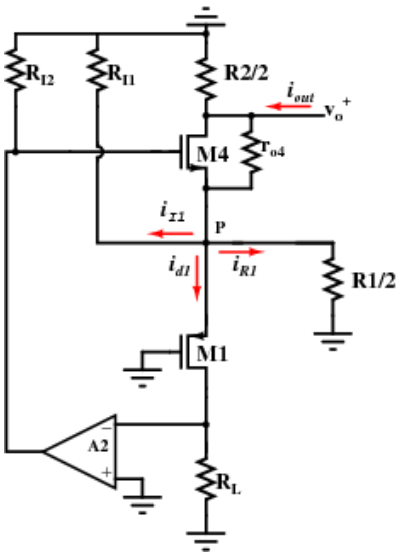

Figure 25: Small signal equivalent half circuit for determining the output impedance of proposed CBIA circuit

The small signal output impedance (R_{out}) is the ratio of the output voltage (v_o) to the output current (i_{out}) when the input node is connected to ac ground.

$$R_{out}=\frac{v_o}{i_{out}}\Big|_{v_i=0} \tag{3.1}$$

When the gate of M1 is connected to small signal ground (as shown in Figure 25), the feedback loop forces the voltage at the source of M1 (node P) also to ground. Consequently the voltage across and the current through R1 are forced to zero. The current flowing to the output node is then given by

$$i_{out}=\frac{v_o}{\left(\frac{R2}{2}\right)}+\frac{v_o}{r_{o4}}+v_{gs_{(M4)}}g_{m4} \tag{3.2}$$

$$\text{But}\quad \frac{v_o}{r_{o4}}+v_{gs_{(M4)}}g_{m4}=I_{R1}=0 \tag{3.3}$$

Substituting (3.3) into (3.2)

$$i_{out}=\frac{v_o}{\left(\frac{R2}{2}\right)}$$

$$R_{out}=\frac{v_o}{i_{out}}=\frac{R2}{2} \tag{3.4}$$

A more detailed analysis of the output impedance that takes into account the finite gain of the feedback loop (A_{loop}) gives the following expression for the output impedance

$$R_{out}=\frac{R2}{2}\|r_{o4}\left(\frac{A_{loop}}{2+R1g_{o4}}\right) \tag{3.5}$$

$$\text{where} \quad A_{loop}=\left[\frac{g_{m4}\left(\frac{R1}{2}\right)}{1+g_{m4}\left(\frac{R1}{2}\right)}\right]\left[g_{m1}(r_{o1}\|R_L)\right]A2 \tag{3.6}$$

The plot below in Figure 26 is a comparison of the output impedance as a function of resistor R2 from equation (3.5) and from circuit simulation results (measured).

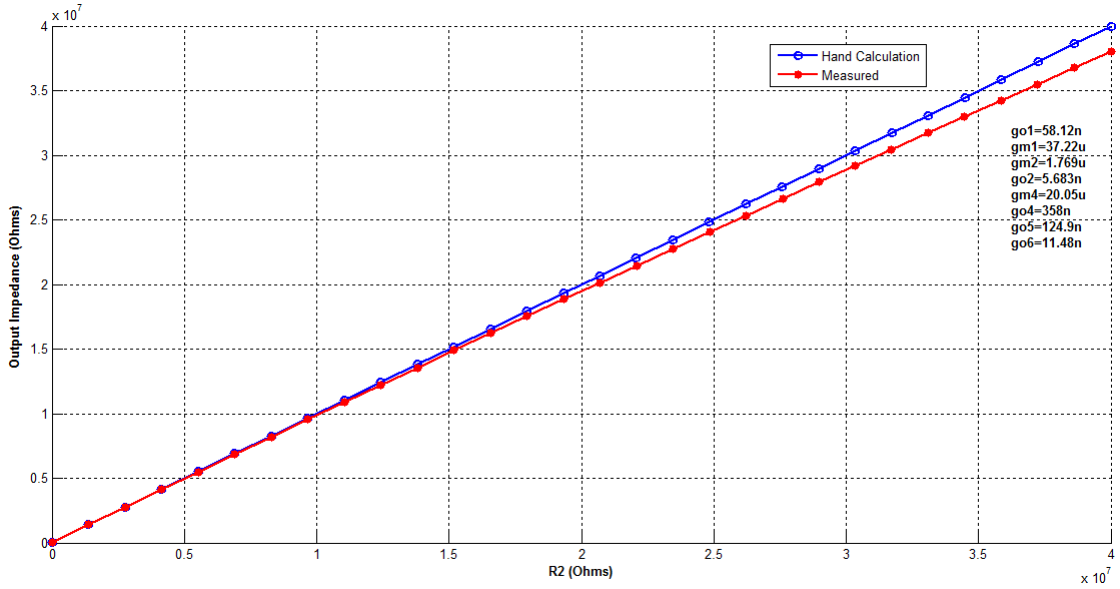

Figure 26: Small signal output impedance from hand calculations and schematic simulation results versus R2 of proposed CBIA circuit

3.2) Transconductance

The small signal transconductance (G_m) is defined as the ratio of the output current (i_{out}) to the input voltage (v_{in}) when the output node is connected to ground.

$$G_m = \frac{i_{out}}{v_{in}}\Big|_{v_o=0} \tag{3.7}$$

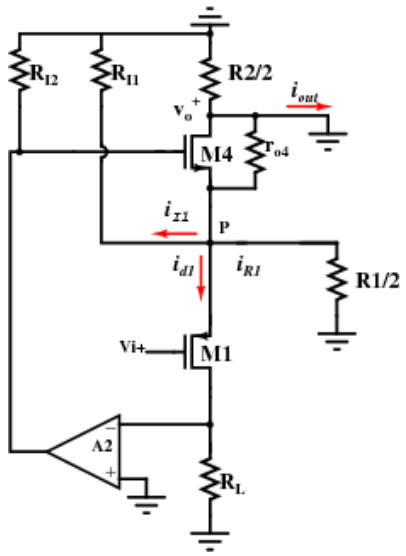

Figure 27: Small signal equivalent circuit for determining the transconductance

From Figure 27, if v_p is the voltage at node P, then

$$i_{out} = \frac{v_p}{\left(\frac{R1}{2}\right)} + \frac{v_p}{R_{I1}} + \frac{v_p}{r_{o4}} + i_{d1} \tag{3.8}$$

Under ideal operating conditions (A_{loop} is infinite), when the voltage at the gate of M1 is v_i, the feedback loop forces the voltage at node P (v_p) to be equal to v_i. Subsequently, the output current is given by

$$i_{out} = \frac{v_i}{\left(\frac{R1}{2}\right)} + \frac{v_i}{R_{I1}} + \frac{v_i}{r_{o4}} + i_{d1} \tag{3.9}$$

$$i_{d1}=0 \text{ since } v_{gs_{(M1)}}=0 \ (v_{g,M1}=v_{s,M1})$$

$$\frac{i_{out}}{v_i}=\frac{2}{R1}+\frac{1}{R_{I1}}+\frac{1}{r_{o4}}$$

$$\frac{i_{out}}{v_i}=\frac{2}{R1}\left(1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}\right)\right) \tag{3.10}$$

If the loop gain (A_{loop}) is finite, the voltage at node P (v_p) is given by

$$v_p=\frac{v_i}{1+\frac{1}{A_{loop}}} \tag{3.11}$$

The current i_{d1} is also given by

$$i_{d1}=g_{m1}v_{gs_{(M1)}}=g_{m1}\left(v_i-\frac{v_i}{1+\frac{1}{A_{loop}}}\right)$$

$$i_{d1}=v_i\left(\frac{1}{1+A_{loop}}\right) \tag{3.12}$$

Substituting (3.11) and (3.12) in (3.8) and simplifying the resulting expression for transconductance,

$$G_m=\frac{i_{out}}{v_{in}}\cong\frac{2}{R1}\left[1-\frac{1}{A_{loop}}\right]\left[1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\right] \tag{3.13}$$

Shown below in Figure 28 is a plot of the transconductance versus resistor R1 from equation (3.13) and from schematic simulation results (measured).

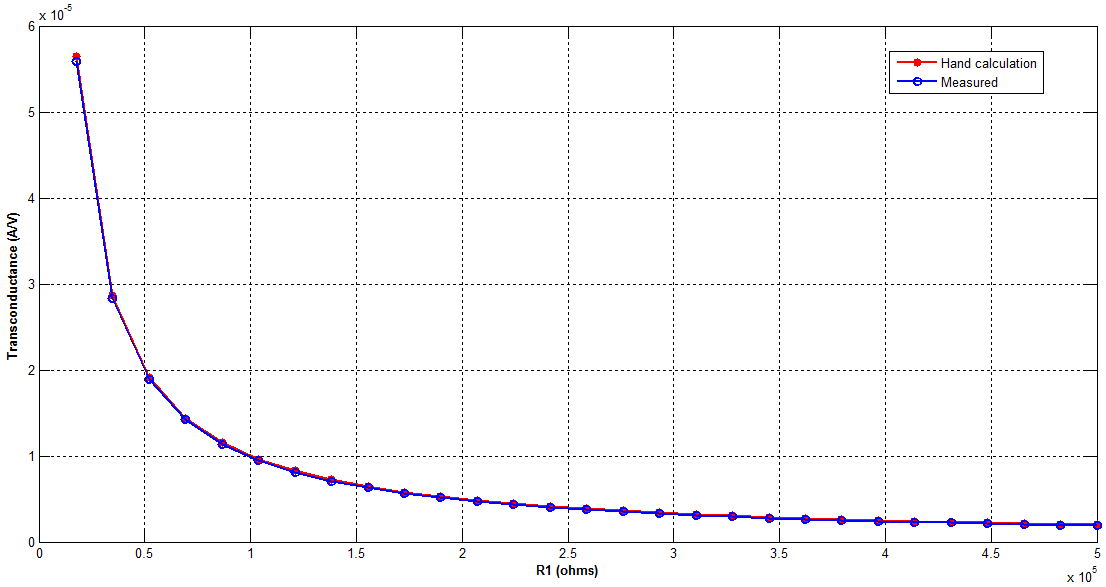

Figure 28: Small signal transconductance from schematic simulation results and hand calculations versus R1 of proposed CBIA circuit

3.3) Voltage Gain

From the above analyses, the voltage gain can be found by taking the product of the transconductance and the output impedance.

$$\frac{v_o}{v_i} = G_m R_{out} \tag{3.14}$$

Substituting (3.5) and (3.13) into (3.14)

$$\frac{v_o}{v_i} \cong \frac{R2}{R1}\left[1-\frac{1}{A_{loop}}\right]\left[1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\right]\left[1-\frac{R2(2+R1g_{o4})}{r_{o4}A_{loop}}\right] \tag{3.15}$$

For large loop gain (A_{loop}), large output impedance of the current source (R_{I1}) and large intrinsic output impedance of M4 (r_{o4}), (3.15) can be approximated as

$$\frac{v_o}{v_i} \cong \frac{R2}{R1} \tag{3.16}$$

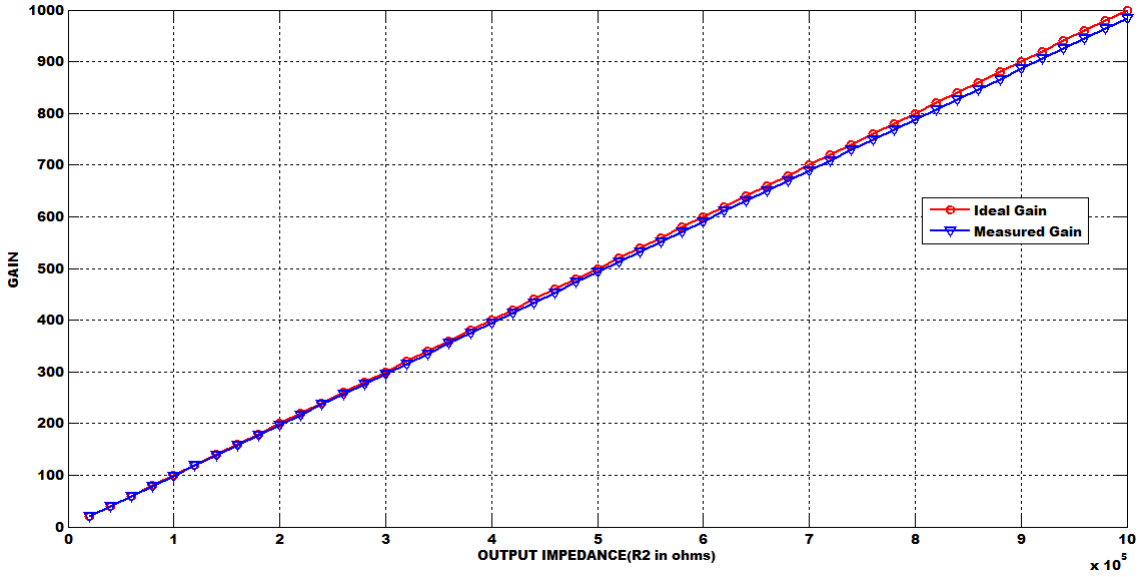

Figure 29: Ideal and simulated voltage gain for different values of the output impedance (R2) of proposed CBIA circuit

The plot in Figure 29 compares the ideal gain $\left(\frac{R2}{R1}\right)$ to the measured gain from circuit simulation results. The above results for the small signal voltage gain, output impedance and transconductance are summarized below in Table 7:

Table 7: Expressions for the small signal output impedance, transconductance and voltage gain for the proposed CBIA circuit

Parameter	Expression
Output Impedance	$\frac{R2}{2}\left[1-\frac{R2(2+R1g_{o4})}{r_{o4}A_{loop}}\right]$
Transconductance	$\frac{2}{R1}\left[1-\frac{1}{A_{loop}}\right]\left[1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\right]$
Voltage gain	$\frac{R2}{R1}\left[1-\frac{1}{A_{loop}}\right]\left[1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\right]\left[1-\frac{R2(2+R1g_{o4})}{r_{o4}A_{loop}}\right]$

3.4) Gain Accuracy

The gain accuracy of the proposed circuit is defined as the ratio of the real gain to the ideal gain (ideal gain is the ratio of R2 to R1).

$$\text{Accuracy}=\frac{\text{Real gain}}{\text{Ideal gain}}=\frac{\text{Real gain}}{(R2/R1)} \tag{3.17}$$

Substituting (3.15) into (3.16),

$$\text{Accuracy}=\left[1-\frac{1}{A_{loop}}\right]\left[1+\frac{R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\right]\left[1-\frac{R2(2+R1g_{o4})}{r_{o4}A_{loop}}\right] \tag{3.18}$$

$$\cong[1-\varepsilon_1][1-\varepsilon_2][1-\varepsilon_3],$$

$$\varepsilon_1=\frac{1}{A_{loop}};\ \varepsilon_2=\frac{-R1}{2}\left(\frac{1}{R_{I1}}+\frac{1}{r_{o4}}+\frac{g_{m1}}{A_{loop}}\right)\ \text{and}\ \varepsilon_3=\frac{R2(2+R1g_{o4})}{r_{o4}A_{loop}}$$

3.5) Frequency Compensation

From Figure 30, the uncompensated circuit has three low frequency poles at nodes p1, p2 and p3. The poles at p1 and p2 occur in the path of the feedback loop from node s_1 to s_2 and have to be compensated to ensure stability when the loop is closed. Miller compensation [19] is chosen because it does not include active devices and hence it does not consume power. Capacitor C_m is used to split the poles at p1 and p2. After compensation, the open loop frequency response from node s1 to s2 can be described by the one-pole system

$$A(s)_{open}=\frac{A_{loop}}{1+\frac{s}{\omega_{p1,old}}} \tag{3.19}$$

where A_{loop} is given by (3.6) and $\omega_{p1,old}$ is the pole at node p1 when the feedback loop from node s1 to s2 is open.

$$\omega_{p1,old}=\frac{(g_{o2}+g_{o6})^2}{g_{m2}C_m}\,\text{rads}^{-1} \tag{3.20}$$

When the loop from s1 to s2 is closed, the closed loop frequency response can be described by the following expression;

$$A(s)_{closed}=\frac{A(s)_{open}}{1+A(s)_{open}} \tag{3.21}$$

Substituting (3.19) into (3.21),

$$A(s)_{closed}=\frac{\left(\frac{A_{loop}}{1+\frac{s}{\omega_{p1,old}}}\right)}{1+\left(\frac{A_{loop}}{1+\frac{s}{\omega_{p1,old}}}\right)}$$

$$A(s)_{closed}=\left[\frac{A_{loop}}{1+A_{loop}}\right]\left[\frac{1}{1+\frac{s}{(1+A_{loop})\omega_{p1,old}}}\right] \quad (3.22)$$

From equation (3.22) when the loop is closed, the pole location moves to a higher frequency by a factor of $(1+A_{loop})$. Thus the pole at node p1 for the closed loop system is located at

$$\omega_{p1}=(1+A_{loop})\frac{(g_{o2}+g_{o6})^2}{g_{m2}C_m}\text{rads}^{-1} \quad (3.23)$$

where Aloop is given by equation (3.6)

Increasing Cm moves this pole to a lower frequency, causing the bandwidth and the unity gain frequency (UGF) to reduce and thus improving the phase margin and the closed loop stability. Also Rm and Cm forms a left hand plane zero at $\frac{1}{2\pi R_m C_m}$ Hz. If the value of R_m is chosen to be equal to $\frac{1}{g_{m2}}$, this zero can be used to cancel the effect of the parasitic right hand plane zero located at $\frac{g_{m2}}{2\pi C_m}$ Hz.

To measure the open loop frequency response from node s_1 to s_2, the input node should be grounded and a test signal (v_{test}) should be injected as shown in Figure 30. The inductor and capacitor values are chosen to be very high so that they are essentially

open and short circuits respectively at 1Hz. This loop should be compensated to obtain a phase margin of 45^{o} or better so as to ensure the stability of the circuit.

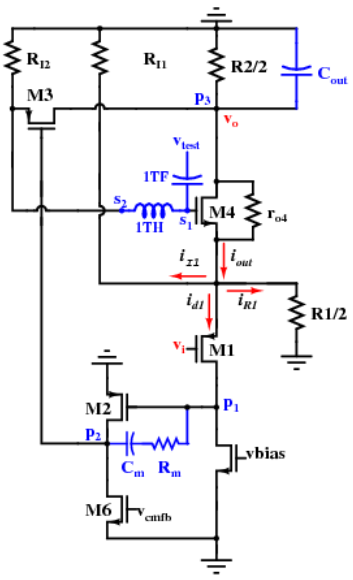

Figure 30: AC equivalent half circuit of proposed CBIA

3.6) Noise Analyses

The small signal noise model in Figure 31 and block diagram in Figure 32 are used to analyze the noise performance of the proposed circuit. The block diagram shows the impact of the noise from each circuit element on the input signal.

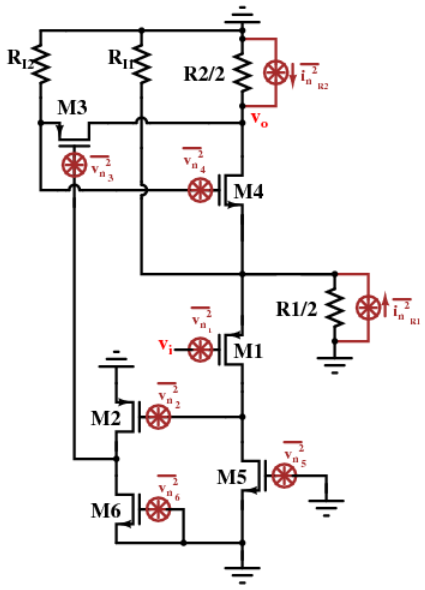

Figure 31: Small signal noise model of proposed CBIA circuit

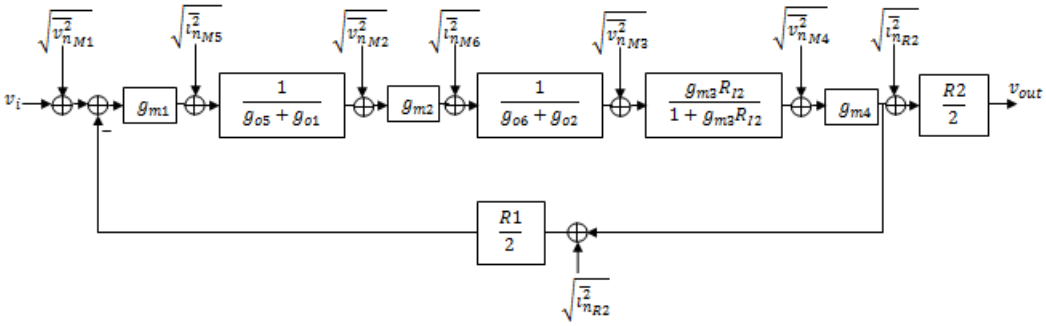

Figure 32: Signal flow block diagram of noise model of proposed CBIA circuit

where g_{m_i} →small signal transconductance of transitor M_i;

g_{o_i} →small signal output conductance of transistor M_i

$\overline{v_{n_i}^2}$ →gate referred mean square voltage noise of M_i

$\overline{i_{n_i}^2} \rightarrow$ mean square current noise of M_i

$\overline{i_{nR_i}^2} \rightarrow$ mean square current noise of resistor R_i

If the loop gain is given by $\left(\frac{g_{m1}}{g_{o5}+g_{o1}}\right)\left(\frac{g_{m2}}{g_{o6}+g_{o2}}\right)\left(\frac{g_{m3}R_{I2}}{1+g_{m3}R_{I2}}\right)(g_{m4})\left(\frac{R1}{2}\right) \gg 1$

Then the total input referred mean square noise $\left(\overline{v_{n_{total}}^2}\right)$ is given by

$$\overline{v_{n_{total}}^2} = \overline{v_{nM1}^2} + \frac{\overline{i_{nM5}^2}}{g_{m1}^2} + \left(\frac{g_{o5}+g_{o1}}{g_{m1}}\right)^2 \left[\overline{v_{nM2}^2} + \frac{\overline{i_{nM6}^2}}{g_{m2}^2} + \left(\frac{g_{o2}+g_{o6}}{g_{m2}}\right)^2 \left(\overline{v_{nM3}^2} + \left(\frac{1+g_{m3}R_{I2}}{g_{m3}R_{I2}}\right)^2 \overline{v_{nM4}^2}\right)\right]$$
$$+ \left(\frac{R1}{2}\right)^2 \left(\overline{i_{nR2}^2} + \overline{i_{nR1}^2}\right) \quad (3.24)$$

Also if $\left(\frac{g_{o5}+g_{o1}}{g_{m1}}\right)^2 \ll 1$, equation (3.24) can be approximated as

$$\overline{v_{n_{total}}^2} \cong \overline{v_{nM1}^2} + \frac{\overline{i_{nM5}^2}}{g_{m1}^2} + \left(\frac{R1}{2}\right)^2 \left(\overline{i_{nR2}^2} + \overline{i_{nR1}^2}\right) \quad (3.25)$$

From equation (3.25), the total input referred noise is dependent on the thermal and flicker noise of transistors M1 and M5 as well as the thermal noise of resistors R1 and R2.

From the empirical new SPICE2 noise model [20],

$$\text{Channel current thermal noise} = \frac{8}{3} kTg_m \left(\frac{3}{2} - \frac{\min(Vds, Vdsat)}{2Vdsat}\right)$$

$$\Longrightarrow \text{Thermal noise} = \frac{4}{3} kTg_m \quad \text{in the saturation region where } Vds > Vdsat \quad (3.26)$$

$$\text{Also, Flicker noise}=\frac{K_F I_{ds}^{af}}{C_{ox}L_{eff}^2 f^{ef}} \tag{3.27}$$

Substituting (3.26) and (3.27) into (3.25), the total input referred noise for the half circuit in Figure 31 is given by

$$\overline{v_{n_{total}}^2}\cong\frac{4}{3}\frac{kT}{g_{m1}}+\frac{4}{3}\frac{kTg_{m5}}{g_{m1}^2}+\frac{K_F}{C_{ox}f^{ef}}\left(\frac{I_{ds1}^{af}}{L_{eff_1}^2}+\left(\frac{g_{m5}}{g_{m1}}\right)^2\frac{I_{ds5}^{af}}{L_{eff_5}^2}\right)+4kT\left(\frac{R1}{2}\right)^2\left(\frac{1}{\left(\frac{R2}{2}\right)}+\frac{1}{\left(\frac{R1}{2}\right)}\right)$$

For R2>>R1;

$$\overline{v_{n_{total}}^2}\cong\frac{4}{3}\frac{kT}{g_{m1}}\left(1+\frac{g_{m5}}{g_{m1}}\right)+4kT\left(\frac{R1}{2}\right)+\frac{K_F}{C_{ox}f^{ef}}\left(\frac{I_{ds1}^{af}}{L_{eff_1}^2}+\left(\frac{g_{m5}}{g_{m1}}\right)^2\frac{I_{ds5}^{af}}{L_{eff_5}^2}\right) \tag{3.28}$$

3.6.1) Theoretical Thermal Noise Limit

From the ACM model [21]

$$g_m=\frac{2I_D}{\phi_{th}\sqrt{1+i_f}+1}$$

where $I_D\rightarrow$drain current, $\phi_{th}\rightarrow$thermal voltage, $i_f\rightarrow$inversion level

$$\text{if } I_f=\frac{2}{\sqrt{1+i_f}+1},\ \text{then } g_m=\frac{I_D I_f}{\phi_{th}},\ 0\le I_f\le 1 \tag{3.29}$$

Substituting (3.29) into (3.28), the input referred thermal noise is given by

$$\left(\overline{v_{n_{total}}^2}\right)_{thermal}=\frac{4}{3}\frac{kT\phi_{th}}{I_{D1}I_{f1}}\left(1+\frac{I_{D5}I_{f5}}{I_{D1}I_{f1}}\right)+4kT\left(\frac{R1}{2}\right) \tag{3.30}$$

Also, $I_{D1}=I_{D5}$ (drain current of M1=drain current of M5)

For a given drain current (I_{D1}), the theoretical thermal noise limit is obtained when I_{f1}=1 (or the inversion level of transistor M1 is zero and it operates very deep in the subthreshold region) and I_{f5}=0 (or the inversion level of transistor M5 is very large and it operates in very strong inversion). Substituting I_{f1}=1 and I_{f5}=0 into equation (3.30), the theoretical noise limit for the proposed circuit for a given drain current (I_{D1}) is given by

$$\text{ie}\lim\left(\overline{v_{n_{total}}^2}\right)_{thermal} = \frac{4}{3}\frac{kT\phi_{th}}{I_{D1}} + 4kT\left(\frac{R1}{2}\right) \tag{3.31}$$

where I_{D1} → drain current of transistors M1and M5

In summary, the following can be deduced from the above noise analyses for the proposed circuit;

a) The inversion level of transistor M1 must be as small as possible for low noise design. This means M1 should be biased to operate in the weak inversion region (i_{f1}<1). However, operating M1 in weak inversion (or subthreshold) region means very large device area and increased parasitic capacitances.
b) The inversion level of transistor M5 must be as large as possible for low noise design. This means M5 should be biased to operate in very strong inversion (i_{f5}>8). However, operating M5 in strong inversion means increased power consumption.
c) The value of resistor R1 should be made as small as possible for low noise design. However reducing R1 also reduces the gain accuracy.

Thus a design tradeoff exists between the input referred noise of the proposed circuit and its area, power consumption, and gain accuracy. From equation (3.18), increasing the value of R1 causes the loop gain (A_{loop}) to increase and the gain accuracy of the circuit to improve but at the cost of increased noise and reduced closed loop stability. Also from equation (3.30), increasing the drain current (I_{D1}) of transistor M1 and reducing the inversion level (i_{f1}) causes the circuit noise to reduce but at the cost of increased power consumption and device area.

4. CHOPPER MODULATION:

A LOW FREQUENCY NOISE REDUCTION TECHNIQUE

4.1) Description of Chopper Modulation

Chopper modulation [15] is a common technique used to reduce the effect of low frequency imperfections (noise and dc offset) in continuous time circuits. It involves upconverting the input signal to a higher frequency before amplification and downconverting the amplified output signal to the original frequency of the input signal. The chopper modulation circuit consists of four MOS switches connected as shown in Figure 33 below:

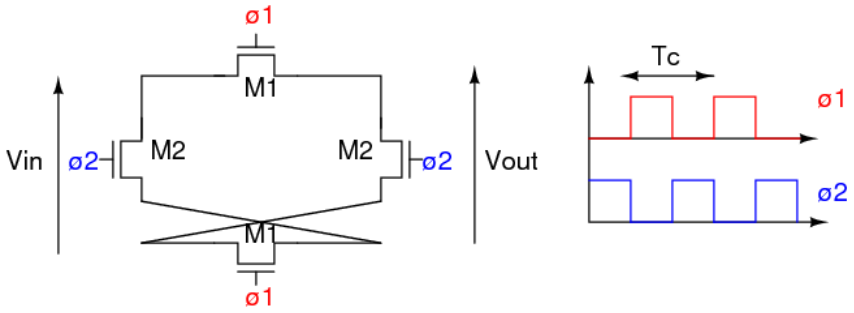

Figure 33: Chopper circuit and switch gate signal

The operation of the chopper circuit above can be described in the time domain as

$$v_{out}(t)=\begin{cases} v_{in}, & 0 \le t < T_c/2 \\ -v_{in}, & T_c/2 \le t < T_c \end{cases} \qquad (4.1)$$

During the first half of the chopping period (T_c) the output signal is equal to the input signal (switches M1 turn on and M2 turn off) and during the last half of the chopping period, the output signal is equal to the negative of the input signal (switches M2 turn on and M1 turn off). This is equivalent to multiplying the input signal with a higher frequency square wave or the sequence {1, -1, 1, -1, 1, -1…} as shown in Figure 34 below.

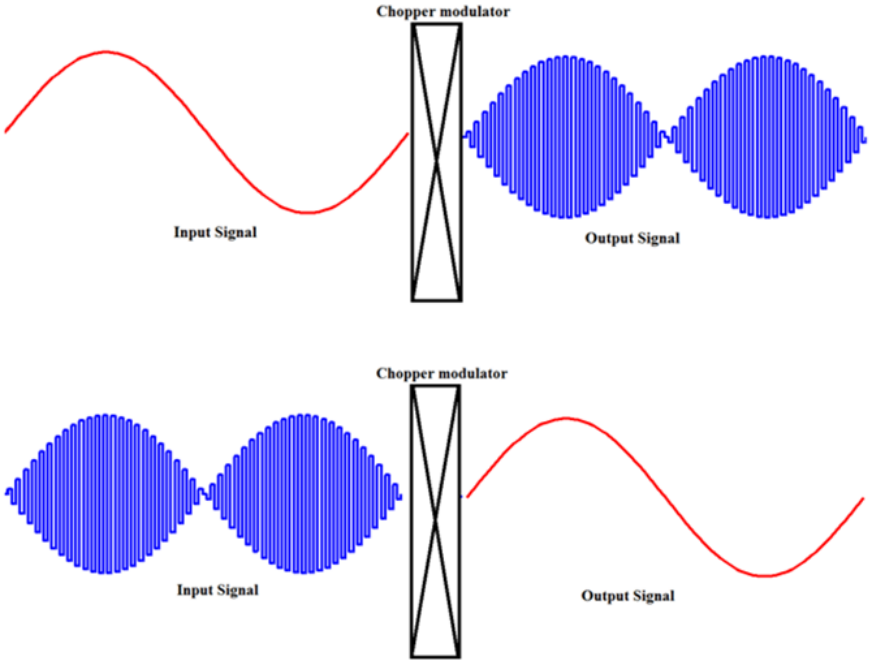

Figure 34: Effect of chopper modulation in the time domain

The effect of chopping in the frequency domain is obtained by taking the Fourier series transform of equation (4.1)

$$S_{out}(f)=\frac{8}{\pi^2}\sum_{\substack{n=0\\ n\ odd}}^{\infty}\frac{1}{n^2}S_{in}(f-nf_c) \tag{4.2}$$

S_{in}→input spectrum, f_c→chopping frequency

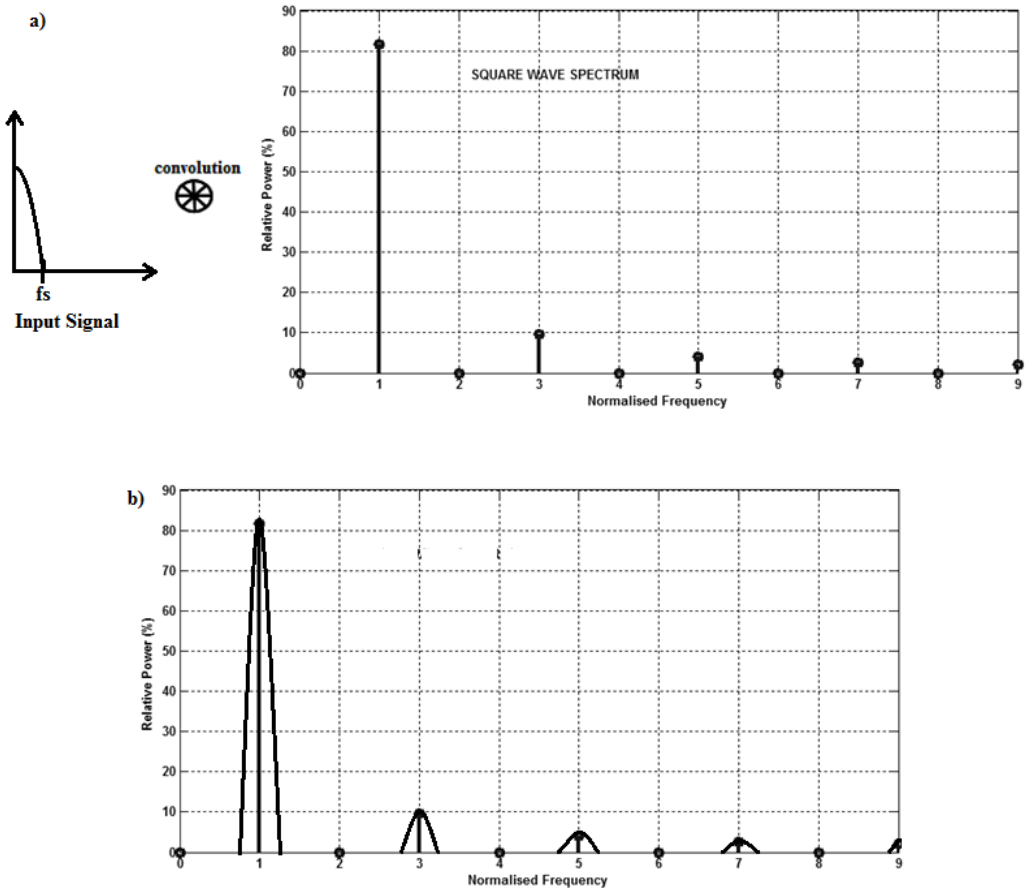

Figure 35: a) Chopping in the frequency domain b) Chopper output spectrum showing the relative powers of the signal at different frequencies

From (4.2), chopping in the frequency domain is equivalent to the convolution of the input signal spectrum with the spectrum of a square wave which causes the input

spectrum to shift to the chopping frequency and its odd harmonics. This is illustrated in Figure 35.

4.2) Effect of Chopper Modulation on Circuit Noise

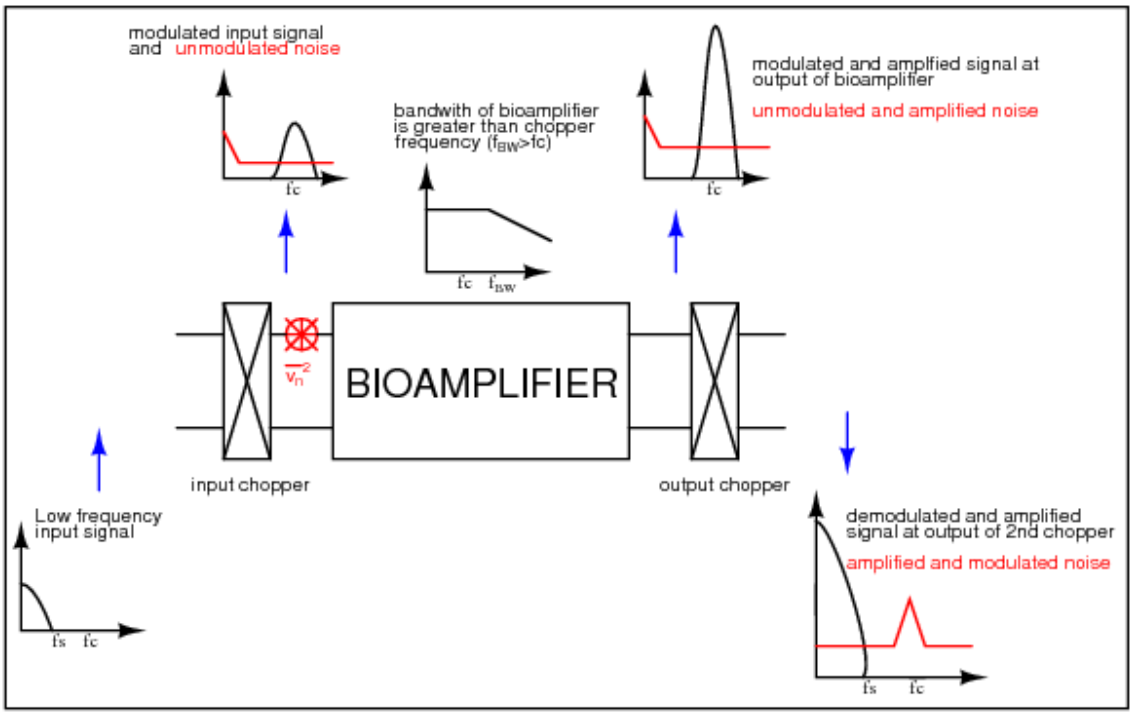

Figure 36: Illustration of the effect of chopper modulation on the input signal and noise

The input chopper modulates the input signal (v_i) to a higher frequency. Subsequently, this high frequency modulated input signal is combined with the un-modulated circuit noise ($\overline{v_n^2}$) at the input of the bioamplifier. The combined signal and noise is then amplified to the output of the bioamplifier. At the output, a second chopper

circuit operating at the same frequency as the input chopper modulates the amplified signal and noise. Thus the circuit noise of the bioamplifier $(\overline{v_n^2})$ is modulated only by the output chopper whiles the desired input signal is modulated by both the input and output choppers. Since the circuit noise is modulated only once by the output chopper, it is upconverted at the output to a higher frequency that is outside the frequency band of interest. This is illustrated in Figure 36. Detailed analyses of the effect of chopper modulation on the flicker and thermal noise of the bioamplifier is given below:

4.2.1) Effect of Chopper Modulation on the Flicker Noise

If the flicker noise power spectral density ($S_{1/f,in}$) at the input is given by

$$S_{1/f,in}(f)=\frac{S_o f_k}{f} \tag{4.3}$$

$S_o \rightarrow$thermal noise PSD and $f_k \rightarrow$noise corner frequency,

then the output PSD ($S_{1/f,out}$) after chopping is obtained by substituting (4.3) into (4.2)

$$(S_{1/f,out})=\frac{8}{\pi^2}\sum_{\substack{n=0\\ n\rightarrow odd}}^{\infty}\frac{1}{n^2}\frac{S_o f_k}{(f-nf_c)}$$

$$=\frac{8S_o f_k}{\pi^2 f_c}\sum_{\substack{n=0\\ n\rightarrow odd}}^{\infty}\left(\frac{1}{n^3}\right) \qquad \text{if } f_c \gg f \tag{4.4}$$

$$(S_{1/f,out})=\frac{8S_o f_k}{\pi^2 f_c}\left[1+\frac{1}{3^3}+\frac{1}{5^3}+\frac{1}{7^3}+\frac{1}{9^3}+\frac{1}{11^3}+\ldots\right]$$

$$(S_{1/f,out})=0.8512\frac{S_o f_k}{f_c} \quad (\text{if } f \ll f_c) \tag{4.5}$$

The resulting expression in (4.5) shows that at frequencies that are much less than the chopping frequency(i.e. $f \ll f_c$), the effect of flicker noise can be significantly reduced if the chopping frequency is chosen to be much larger than the noise corner frequency (f_k).

4.2.2) Effect of Chopper Modulation on the Thermal Noise

Since the thermal noise PSD at the input (S_o) is noise shaped by the frequency response of the bioamplifier, the thermal noise PSD at the output (S_{out}) of the bioamplifier is given by the expression

$$S_{out}(f)=\frac{S_o}{1+\left(\frac{f}{f_{BW}}\right)^2} \tag{4.6}$$

where f_{BW} is the -3dB bandwidth of the bioamplifier

Consequently, the effect of chopper modulation on the thermal noise is obtained by substituting (4.6) into (4.2)

$$(S_{out,th})=\frac{8}{\pi^2}\sum_{\substack{n=0 \\ n\rightarrow odd}}^{\infty}\frac{1}{n^2}\left[\frac{S_o}{1+\left(\frac{f-nf_c}{f_{BW}}\right)^2}\right] \tag{4.7}$$

From [15], at frequencies that are much less than the chopping frequency(i.e. $f \ll f_c$) the infinite series in (4.7) can be approximated by the closed form expression

$$\left(S_{out,th}\right)=S_o\left[1-\frac{\tanh\left(\frac{\pi}{2}\frac{f_{BW}}{f_c}\right)}{\frac{\pi}{2}\frac{f_{BW}}{f_c}}\right] \tag{4.8}$$

$$\text{But } \tanh\left(\frac{\pi}{2}\frac{f_{BW}}{f_c}\right)=\frac{e^{\pi\frac{f_{BW}}{f_c}}-1}{e^{\pi\frac{f_{BW}}{f_c}}+1} \cong 1, \text{ if } \frac{f_{BW}}{f_c}\geq 1 \tag{4.9}$$

From (4.8) and (4.9)

$$\left(S_{out,th}\right)\cong S_o\left[1-\frac{2}{\pi\frac{f_{BW}}{f_c}}\right] \quad (\text{if } f_{BW}\geq f_c) \tag{4.10}$$

It follows from (4.10) that at frequencies that are much less than the chopping frequency(i.e. $f\ll f_c$), if the bandwidth of the bioamplifier is very much greater than the chopping frequency(i.e. $f_{BW}\gg f_c$) then chopper modulation has negligible effect on the thermal noise of the bioamplifier.

4.3) Selecting the Chopping Frequency

From the results of the above analyses on the effects of chopper modulation on the flicker noise and thermal noise, since chopping has negligible effect on the thermal noise of the bioamplifier, the choice of an appropriate chopping frequency should be guided by equation (4.5). Consequently the most important factors to consider when choosing the chopping frequency are the bandwidth of the bioamplifier (f_{BW}) and the noise corner frequency (f_k). From (4.5), to reduce the effect of low frequency flicker noise, the chopping frequency should be very much greater than the noise corner frequency. However, choosing a very high chopping frequency has undesirable

consequence on the effective gain and input impedance of the bioamplifier.

Selecting a high chopping frequency reduces the effective gain due to the limited bandwidth of the bioamplifier. This is because the higher order harmonics of the input signal produced by the input chopper (see Figure 35) will be attenuated by the amplifier and cannot be demodulated by the output chopper. Figure 37 shows the effect of the chopping frequency and the amplifier's bandwidth on the attenuation of the input signal. Generally, choosing a chopping frequency less than one-third of the amplifier's bandwidth ensures that this signal attenuation is less than 10% of the ideal signal amplitude if the bandwidth of the amplifier was infinite.

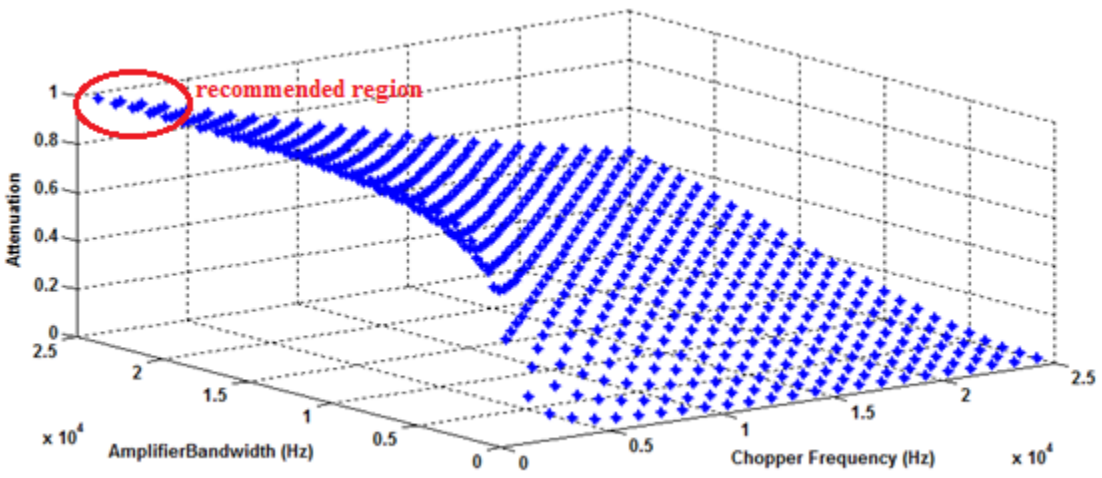

Figure 37: Effect of the chopping frequency and the amplifier bandwidth on signal attenuation

Another undesirable effect of choosing a high chopping frequency is the reduction in the effective input impedance of the bioamplifier which increases the attenuation of the input signal. Shown in Figure 38 is an equivalent circuit at the input of a bioamplifier with chopper modulators. Since the input impedance forms a voltage divider with the electrodes, bioamplifiers with purely capacitive input impedance are desirable because their impedance is very high at the low frequencies of biological signals. This ensures that the biological signal is transferred from the electrode to the input of the bioamplifier without attenuation.

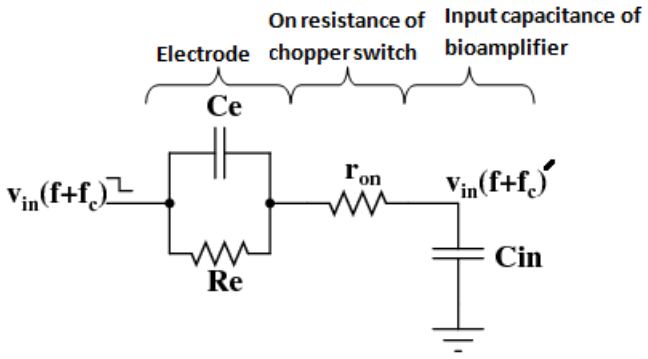

Figure 38: Equivalent circuit at the input of a chopper modulated bioamplifier

Assuming that the on resistance of the chopper switch (r_{on}) is very small,

$$\text{Attenuation}=\frac{v_{in}(f+f_c)'}{v_{in}(f+f_c)}=\frac{1+(f+f_c)C_eR_e}{1+(f+f_c)R_e(C_e+C_{in})} \tag{4.11}$$

Thus increasing the chopping frequency causes the attenuation of the input signal to increase. Shown in Figure 39 is the magnitude (in dB) of the attenuation of the input signal as the chopper frequency (f_c) is increased

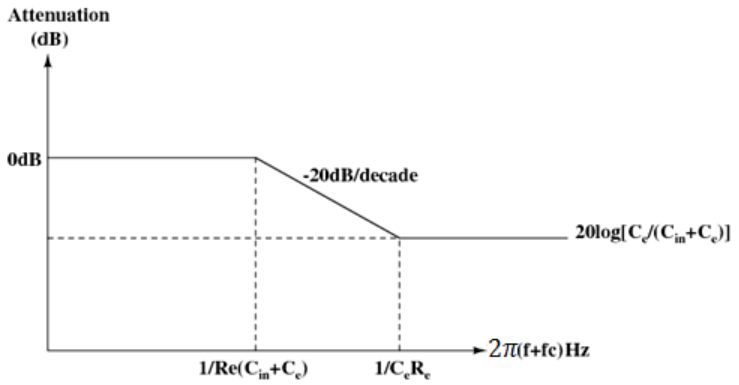

Figure 39: Effect of chopper frequency, electrode impedance and input impedance of the bioamplifier on the attenuation of the input signal

Table 3 gives the typical values of resistance (R_e) and capacitance (C_e) of some common biological electrodes and can be used with equation (4.11) to determine the appropriate chopping frequency that minimizes the attenuation of the input signal.

4.4) Differential Electrode Offset (DEO) Rejection Techniques

DEO is a dc signal that is created as a result of mismatch in the electrodes used in biological signal extraction. It may be several times larger than the desired low frequency biological signal and it can cause the front-end amplifier to saturate. As a result, the biological electrodes are ac coupled to the frontend amplifier to remove this

undesired effect. Two common methods are used to ac couple the extracted biological signal to the frontend amplifier; the use of high time constant off chip passive filters and the use of a dc servo mechanism on chip.

The most common way to achieve ac coupling is to filter the incoming signal with off chip high pass filters. To avoid degrading the CMRR due to mismatch in the external passive components, a floating high pass filter architecture was used in [1]. Off chip filtering of DEO with passive elements does not consume power but it increases the circuit noise by $\frac{kT}{C}$ and also increases the external component count.

Alternatively a dc servo mechanism may be used by low pass filtering the amplifier's output to select the dc component and subtracting it from the signal at the input [2],[3] or at an internal node [4]. Subtracting the signals at an internal node helps to avoid degrading the high input impedance. Because high time constant low pass filters are easy to implement on-chip using pseudoresistors, this method is the most common for on-chip ac coupling implementations. However, the dc servo path increases the power consumption and noise of the frontend amplifier.

5. DESIGN PROCEDURE AND RESULTS

The Advanced Compact MOSFET (ACM) model [21] enables the operation of the MOSFET in all regions (weak, moderate and strong inversion) to be described by a single equation. Based on this model, the aspect ratio $\left(\frac{W}{L}\right)$, transconductance-to-current ratio $\left(\frac{g_m}{I_D}\right)$ and saturation voltage (V_{dsat}) of a MOS device can be described by the following relations:

$$\left(\frac{W}{L}\right)_{normalised} = \frac{\left(\sqrt{2}-1\right)}{\sqrt{1+i_f}-1} \tag{5.1}$$

$$\left(\frac{g_m}{I_D}\right)_{normalised} = \frac{\sqrt{1+i_f}+1}{\left(\sqrt{2}+1\right)} \tag{5.2}$$

$$(V_{dsat})_{normalised} = \sqrt{1+i_f}+3 \tag{5.3}$$

where i_f is the inversion level defined as the ratio of the drain current (I_D) to a technology parameter (I_s). Shown below in Figure 40 is a plot of equations (5.1), (5.2) and (5.3) versus the inversion level (i_f).

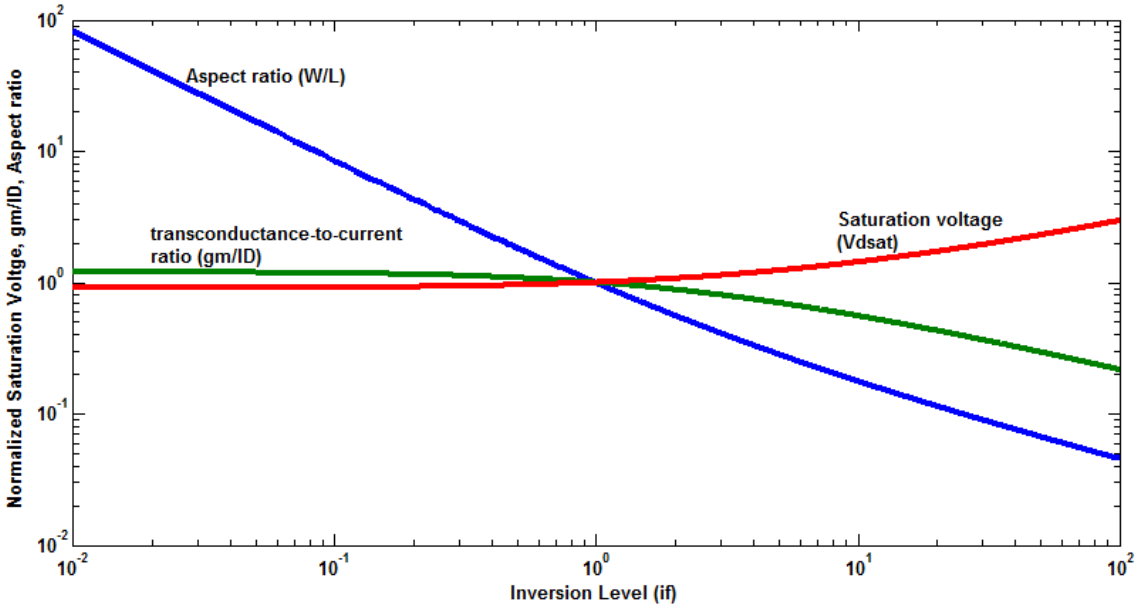

Figure 40: Normalized saturation voltage, transconductance-to-current ratio and aspect ratio versus the inversion level

5.1) Design Procedure

The most important design considerations are noise, power consumption, gain accuracy, and closed loop stability from node s1 to node s2 (see Figure 41). The basic design procedure is outlined below. Since it involves the optimization of several parameters, the basic steps may have to be iterated to obtain the desired performance.

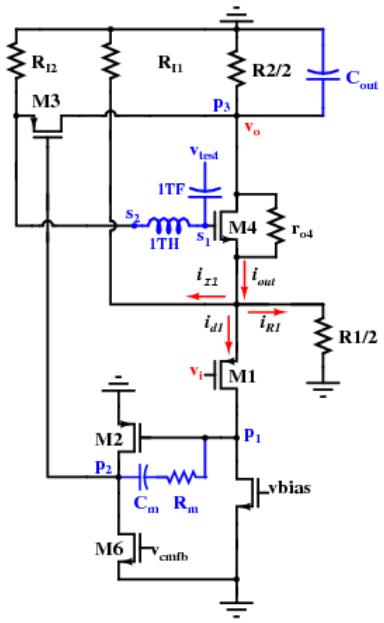

Figure 41: Small signal half circuit of proposed CBIA

The design procedure is based on the design specifications given in Table 8.

Table 8: Design specifications for proposed CBIA circuit

Specification	Target
Input referred thermal spot noise	<60nV/$\sqrt{Hz}$
Total current	<10uA
Gain(A_v)	40dB
Accuracy	>95%
Supply voltage	2V

[1] Select an inversion level for M1 (i_{fM1}) such that $\frac{g_m}{I_D}$ is maximized. This ensures that the voltage noise contribution from M1 is minimized. From Figure 40, $\frac{g_m}{I_D}$ changes very little for i_f between 0.1 and 1 but the $\frac{W}{L}$ increases drastically. As a result i_{fM1} is chosen as 0.2

[2] Since M5 is used as an active load, select an inversion level for M5 (i_{fM5}) such that $\frac{g_m}{I_D}$ is minimized (to ensure the minimum current noise contribution from M5) and V_{dsat} is minimized (to ensure the maximum voltage swing across M5). From figure 40, for i_f between 1 and 10, V_{dsat} begins to rise sharply and $\frac{g_m}{I_D}$ begins to fall sharply. As a result i_{fM5} is chosen as 6.

[3] From (3.29), determine the bias current for M1 and M5 needed to meet the given noise specification.

$$I_{D1}=\frac{\frac{4}{3}\frac{kT\phi_{th}}{I_{f1}}\left(1+\frac{I_{D5}I_{f5}}{I_{D1}I_{f1}}\right)}{\left(\overline{v_n^2}_{total}\right)_{thermal}} \tag{5.4}$$

From (3.28)

$$I_{f1}=\frac{2}{\sqrt{1+0.2}+1}=0.9544$$

$$I_{f5}=\frac{2}{\sqrt{1+6}+1}=0.5486$$

$$I_{D1}=\frac{\frac{4}{3}\frac{\left(1.38\times10^{-23}\right)(298)(0.026)}{0.9544}\left(1+\frac{0.5486}{0.9544}\right)}{\left(60\times10^{-9}\right)^2}$$

$$=3.92uA$$

[4] With the values of the drain current (I_{D1}) and inversion levels (i_{fM1} and i_{fM5}) obtained above, calculate the aspect ratios of M1 and M5 from the equation below [21].

$$\left[\frac{W}{L}\right]=\frac{I_D}{i_f\left[\mu_{P/N}C_{ox}n\frac{\phi_t^2}{2}\right]} \tag{5.5}$$

where $C_{ox}=2.48\times10^{-7}Fcm^{-1}$; $\mu_P=201.36cm^2V^{-1}s^{-1}$;

$\mu_N=453.22cm^2V^{-1}s^{-1}$; $n=1$; $\phi_t^2=0.026mV$

$$\left[\frac{W}{L}\right]_{M1}=\frac{3.92\times10^{-6}}{0.2\left[(201.36)\left(2.48\times10^{-7}\right)(1)\frac{0.026^2}{2}\right]}=1161.2$$

$$\left[\frac{W}{L}\right]_{M5}=\frac{3.92\times10^{-6}}{6\left[(453.22)\left(2.48\times10^{-7}\right)(1)\frac{0.026^2}{2}\right]}=17.2$$

[5] Based on the power consumption specification and with I_{D1} known, distribute the remaining current among the other branches of the circuit based on the following KCL relations:

$$I_{D1}=I_{DI1}+I_{D4}$$

$$I_{TOTAL}=I_{D1}+I_{D2}$$

Since I1 is a current source, its drain current (I_{DI1}) is chosen to be 600nA to obtain a high output impedance so as to minimize errors in the gain accuracy of the overall circuit.

$$I_{DI1}=0.6\mu A$$

$$I_{D4}=3.92\mu-0.6\mu=3.32\mu A$$

$$I_{D2}=5\mu-3.92\mu=1.08\mu A$$

[6] Select an inversion level for M4 such that $\frac{g_m}{I_D}$ is maximized. From (3.17), this ensures high gain accuracy but at the cost of reduced voltage swing at the output due to increased V_{dsat}.

$$i_{fM4}=0.05$$

Since the noise contribution from M2, M3 and M6 are not critical select their inversion levels so that V_{dsat} is minimized. This ensures a large output impedance to maximize the gain accuracy and the voltage swing at the output

$$i_{fM2}=2;\ i_{fM3}=3;\ \ i_{fM6}=1$$

[7] With the drain currents and inversion levels obtained for M2, M3, M4 and M6, repeat step 4 to determine their respective aspect ratios.

[8] Determine the minimum value of R1 that ensures the desired gain accuracy is achieved. Open the loop at nodes s1 and s2 and inject a test signal (vtest) as shown in Figure 41. The magnitude of the AC response (A_{loop}) obtained determines the gain accuracy of the circuit.

$$\text{Accuracy}\cong 1-\frac{1}{A_{loop}}$$

$$\text{For Accuracy}>0.95,\ A_{loop}>\frac{1}{0.05}=20$$

Adjust the value of resistor R1 to obtain the desired loop gain (A_{loop}) for the desired accuracy.

[9] With R1 determined, R2 is given by

$$R2=A_vR1$$

[10] Plot the open loop response from node s1 to s2 by opening the loop with a large inductor (L=1TH) and injecting a test signal (v_{test}) through a large capacitor (C=1TF) as shown in Figure 41. Increase the value of the compensation capacitor (C_m) until the phase margin of this loop is better than 45° to guarantee stability when the loop is closed. Select resistor $R_m=\frac{1}{g_{m,M2}}$ to cancel the right hand plane zero created by C_m. Figure 42 shows plots of the open loop frequency response from node s_1 to s_2 before and after frequency compensation. The phase margin obtained is 180-[-180-(-298)]=62°.

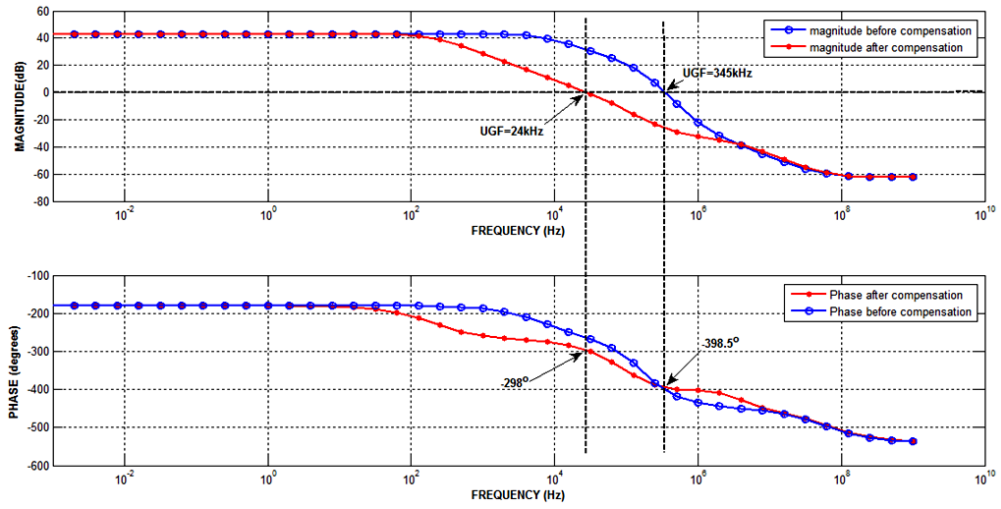

Figure 42: Open loop magnitude and phase from node s1 to s2 before and after compensation of the proposed CBIA circuit

[11] The bias voltage at the output is set by Vref via a common mode feedback circuit (Figure 24). The amplifier Ac is a low power OTA used to boost the gain of the common mode feedback loop. The capacitor C_{out} is used to define the dominant pole of the common mode feedback circuit and thus stabilize this loop.

$$C_{out}=5pF;\ V_{ref}=1V$$

The above results are summarized below in Tables 9 and 10.

Table 9: Device dimensions and inversion levels

Device	W/L(µm/µm)	Multiplier	Inversion level(i_f)
M1	25.05/4.95	100	0.21
M2	1.5/7.95	1	2.1
M3	1.5/7.5	22	3.16
M4	30/4.95	4	0.046
M5	1.5/19.95	3	6.17
M6	1.5/10.05	1	1.18

Table 10: Values of passive devices

Device	Value
C_m	1.5pF
R_m	500kΩ
C_{out}	5pF

The layout of the circuit in the 0.5um CMOS ON-Semiconductor process is shown in Figure 43 below. The layout consists of two circuits, one with choppers and the other without choppers.

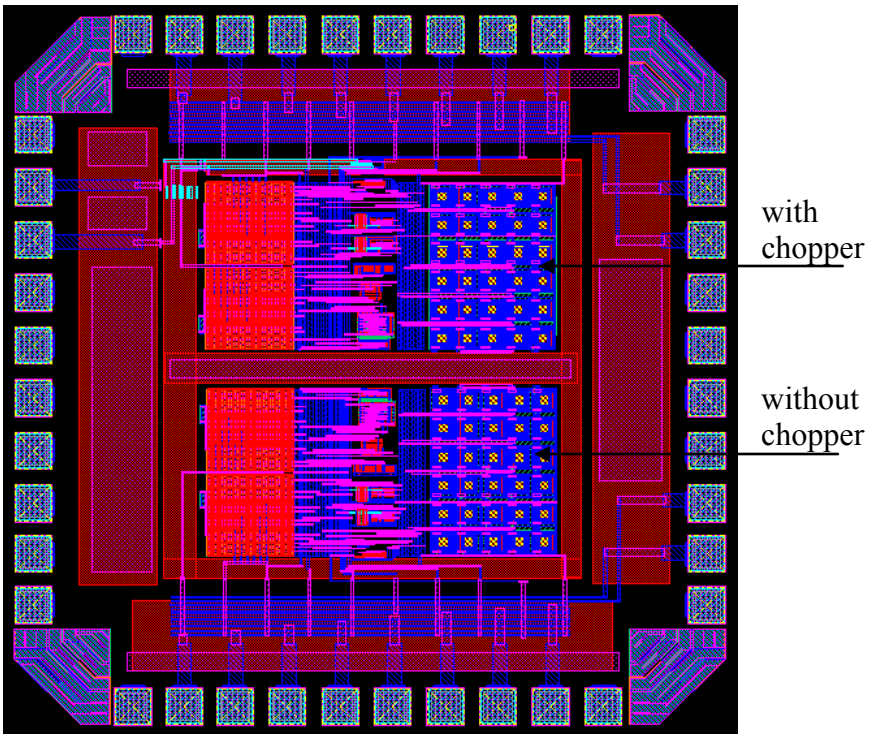

Figure 43: Layout of proposed CBIA circuit

5.2) Schematic and Post Layout Simulation Results

5.2.1) Gain Accuracy

The plot below in Figure 44 shows the ideal and simulated gain of the proposed circuit for different values of the output impedance (R2). The horizontal axis is labeled

control voltage because the output resistor is implemented with a PMOS device operating in the triode region. The resistance of this active resistor is varied by changing the gate voltage (the gate voltage of this active resistor is labeled as the control voltage).

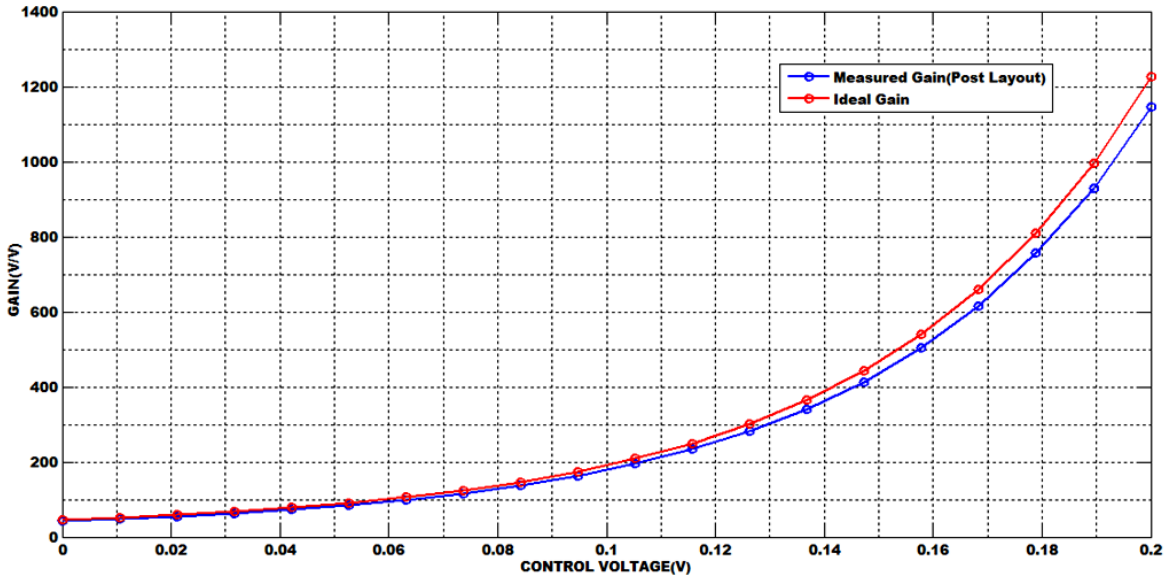

Figure 44: Ideal gain and simulated gain (post layout) of proposed CBIA

Shown below in Figure 45 is a plot of the gain accuracy for both schematic and post layout. The accuracy was measured by the taking the ratio of the simulated gain to the ideal gain. For the schematic, gain accuracy is greater than 98% and is greater than 93% for the post layout.

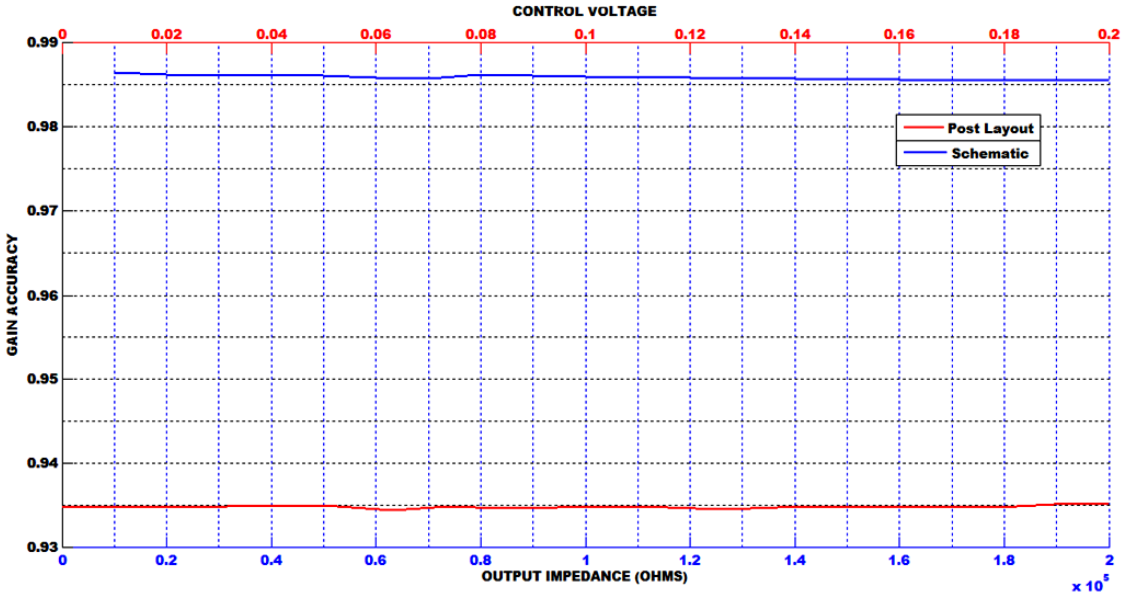

Figure 45: Gain accuracy for post layout and schematic of proposed CBIA as the output impedance (R2) is varied

5.2.2) Frequency Response

The frequency response plot in Figure 46 shows a second order roll off. The two most important poles occur at the output (p_{out}) and at node p1 (p_{p1}) (see Figure 41).Their locations are given by the expressions:

$$p_{out} = \frac{1}{2\pi R2 C_{out}} \text{Hz}; \qquad p_{p1} = \frac{(g_{o1}+g_{o5})^2}{2\pi g_{m2} C_m}(1+A_{loop}) \text{Hz}$$

where Aloop is given by equation (3.6)

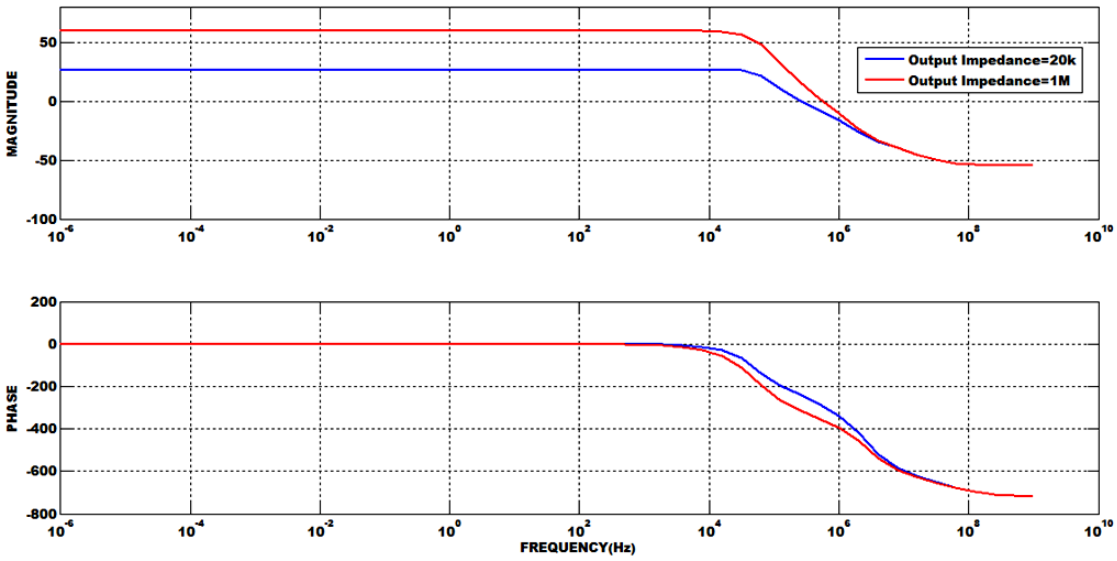

Figure 46: Magnitude and phase response of proposed CBIA circuit

5.2.3) Noise

The noise spectrum of the circuit is shown below in Figure 47 for both schematic and post layout of the proposed circuit.

5.2.3.1) Noise Efficiency Factor (NEF)

The circuit achieves $37.63\text{nV}/\sqrt{\text{Hz}}\left(41.73\text{nV}/\sqrt{\text{Hz}}\text{-for postlayout}\right)$ thermal noise. The total current consumption is 9.26uA (10.91uA-for post layout). Minus current consumed by the biasing circuits, the total current consumption is 6.3uA (7.95uA-for post layout). The NEF is given by

$$\text{NEF}=\frac{v_{in_{rms}}}{\sqrt{\text{BW}(\pi/2)}}\sqrt{\frac{2I_{total}}{\pi 4kT(v_{th})}};$$

$$\left(\frac{v_{in_{rms}}}{\sqrt{BW(\pi/2)}}\right) \rightarrow \text{spot noise} = 37.63\text{nV}/\sqrt{\text{Hz}}$$

$$NEF = (37.63\times10^{-9})\sqrt{\frac{2(9.26\times10^{-6})}{4\pi(1.38\times10^{-23})(300)(0.026)}}$$

$$= 5.5 \text{ (6.6 for post layout)}$$

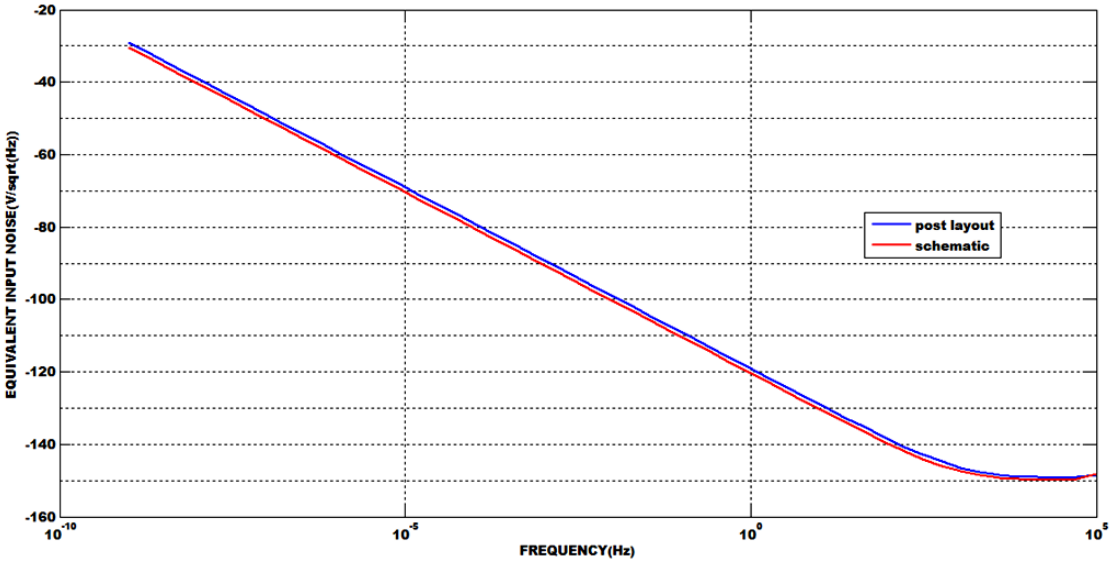

Figure 47: Input referred noise for schematic and post layout of proposed CBIA circuit

5.2.4) Gain versus Input Common Mode Level

Shown below in Figure 48 is a plot of the gain versus the input common mode dc level. The plot is obtained by measuring the gain of the circuit for different values of the input common mode dc level. For both schematic and post layout the input common mode range is ±50mV.

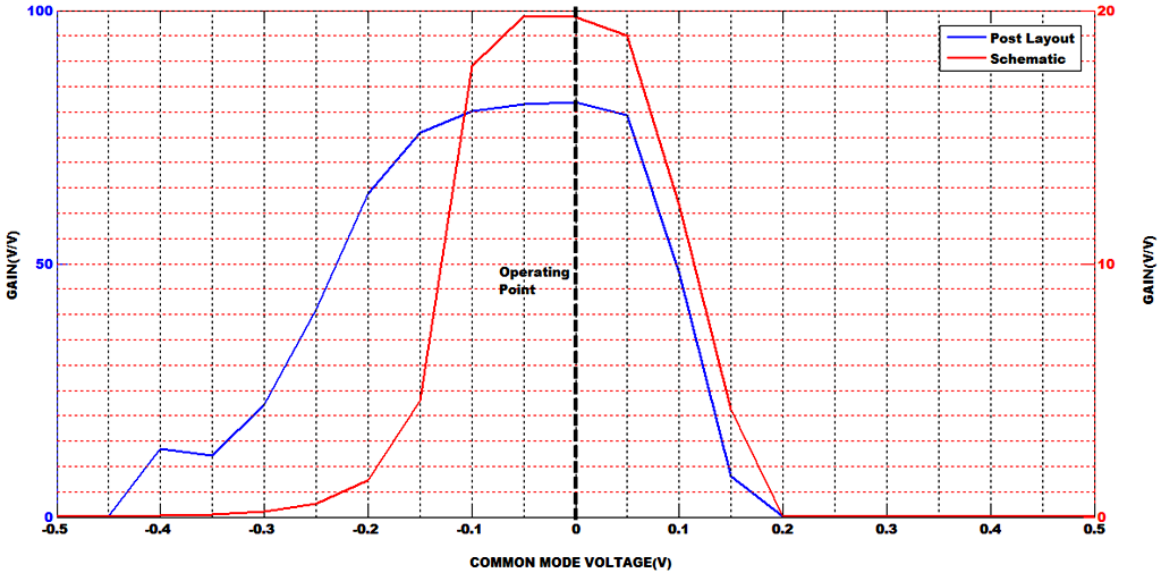

Figure 48: Effect of dc common mode voltage variations on the gain of proposed CBIA circuit

5.2.5) Input Impedance

The input impedance is equivalent to a capacitance of 1.6pF for both the schematic and the post layout of the proposed circuit. The plot of the input impedance is shown below in Figure 49.

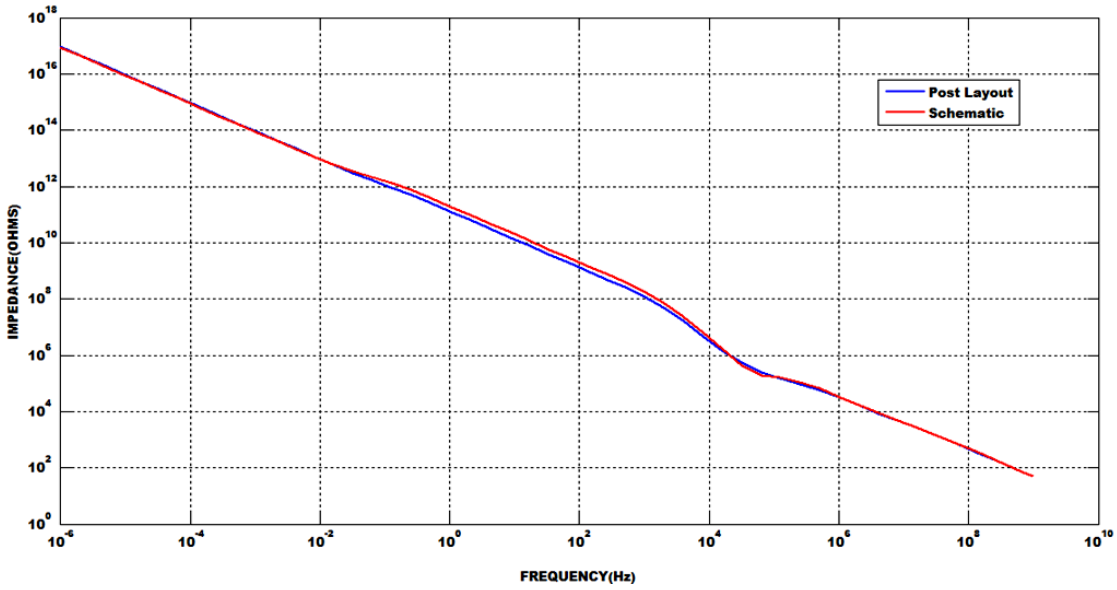

Figure 49: Input impedance for schematic and post layout of proposed CBIA circuit

The above simulation results are summarized in Table 11.

Table 11: Comparison of post layout and schematic simulation results

Parameter	Post Layout	Schematic
Gain Accuracy	94%	98%
Current	10.91uA	9.26uA
Thermal noise	41.73nV/√Hz	37.63nV/√Hz
Common mode input range	±50mV	±50mV
NEF	6.6	5.5
Input capacitance	1.6pF	1.6pF

5.2.6) Effect of Chopper Modulation on Circuit Performance

Shown below in Figure 50 is the dynamic response of the impedance of the switches used to implement the input and output choppers. The input signal is chopped at a frequency of 4 kHz. The impedance of the input chopper switch goes from 9kΩ (when it is in the ON state) to 4MΩ (when it is in the OFF state). For the output chopper switches, the ON impedance is 701MΩ and the OFF impedance is 4.8TΩ. Because the clock signals controlling the choppers overlap, it is possible for all the chopper switches to turn on during the overlap phase. The very high ON impedance of the output chopper switches ensures that the output impedance of the amplifier remains constant and equal to R2 during the overlap phase.

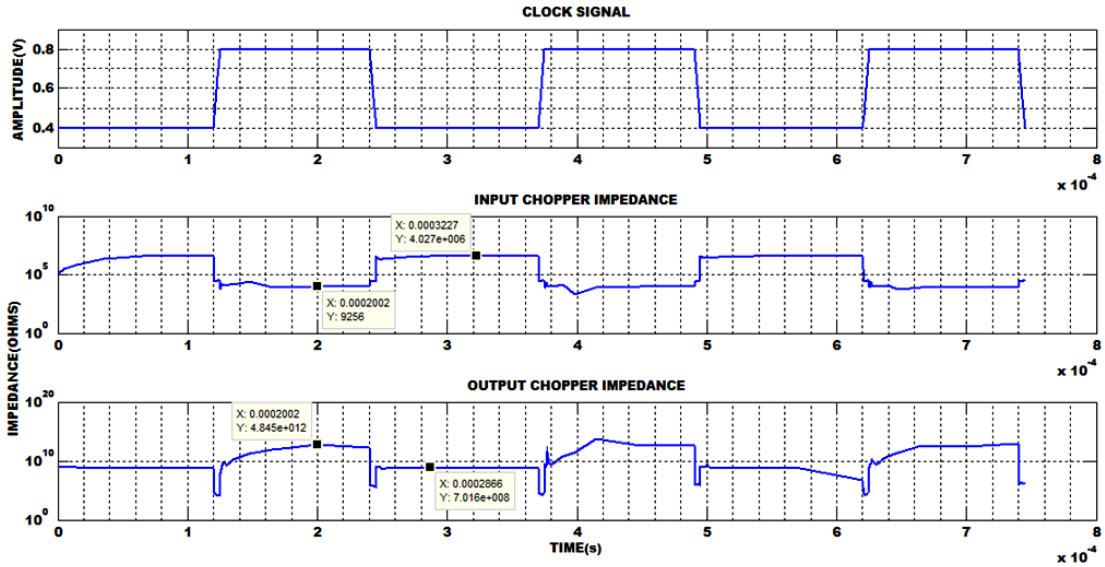

Figure 50: Dynamic response of the impedance of chopper switches

The effects of chopper modulation on the performance of the amplifier are discussed below. All results were obtained from post layout circuit simulations.

5.2.6.1) Effect of Chopping on Input Impedance

The effect of chopping on the input impedance is shown below in Figure 51. Because the input impedance is capacitive, increasing the chopping frequency reduces the effective input impedance of the amplifier. The input impedance of the proposed circuit, after chopping at 4 kHz, was 1.5MΩ.

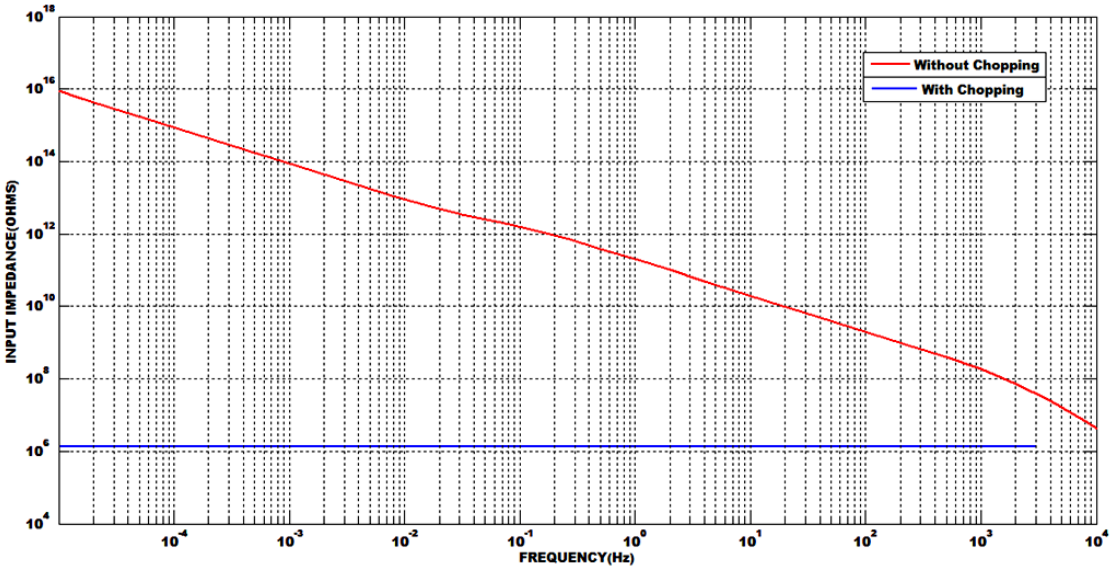

Figure 51: Effect of chopping on the input impedance of proposed CBIA circuit

5.2.6.2) Effect of Chopping on the Input Referred Noise

One of the principal reasons for using chopper modulators is to reduce the low frequency input referred noise of the amplifier. The effect of chopping at 4kHz on the input referred noise PSD of the proposed circuit is shown below in Figure 52:

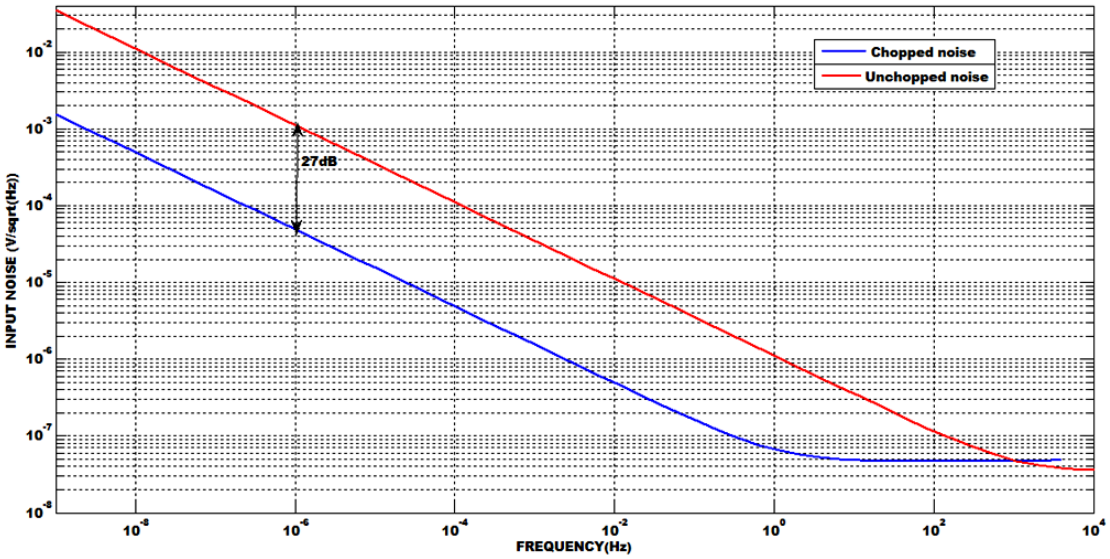

Figure 52: Effect of chopping on the input referred noise of proposed CBIA circuit

Chopping at 4kHz caused the noise corner frequency to reduce to 1Hz from 1kHz. This resulted in a 27dB reduction in the low frequency flicker noise.

5.2.6.3) Effect of Chopping on the Gain

Gain reduction in chopper modulated amplifiers is due to finite amplifier bandwidth and output signal distortion. Because of the finite bandwidth, signal energy at

high frequencies is attenuated and cannot be recovered by the output chopper. Also, distortion in the output signal spreads the signal energy at baseband to higher frequencies that are filtered out by subsequent stages. The amplifier gain reduced by approximately 10% when choppers were used as shown below in Figure 53.

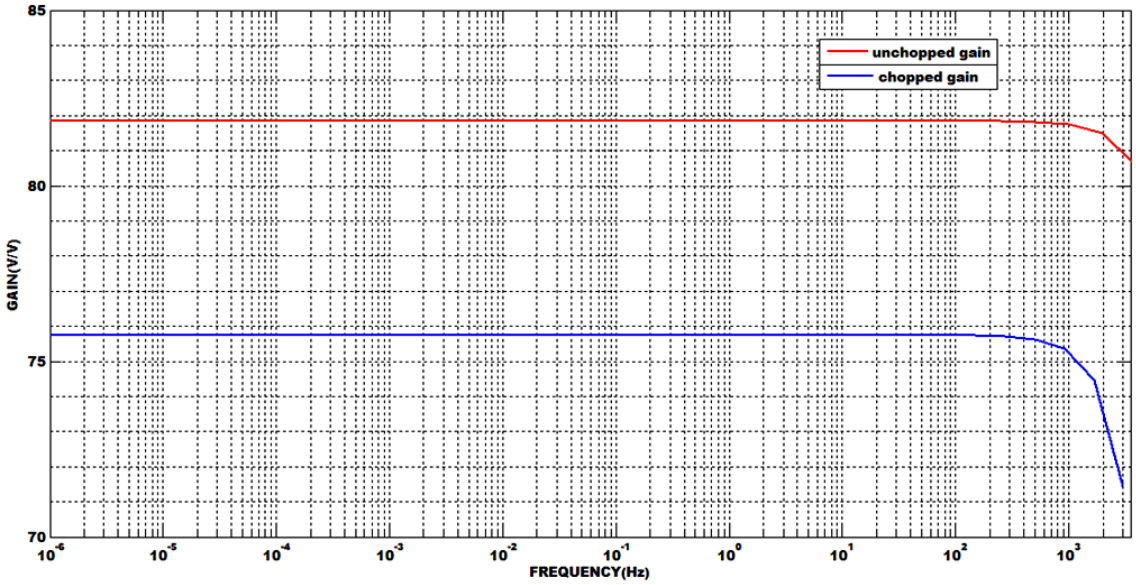

Figure 53: Effect of chopper modulation on the gain of proposed CBIA circuit

5.2.6.4) Effect of Chopping on Common Mode Rejection Ratio (CMRR)

The very high common mode rejection ratio of chopper modulated amplifiers is explained as follows: the input common mode signals pass through the input chopper without being upconverted. Due to mismatches in the amplifier, the common mode signals will be converted to differential signals at the output. The output chopper will

then upconvert these undesired low frequency differential signals to higher frequencies whiles the desired differential input signals are downconverted to baseband. The common mode rejection ratio of the proposed circuit (post layout) when used with chopper modulators at 4kHz is shown below in Figure 54.

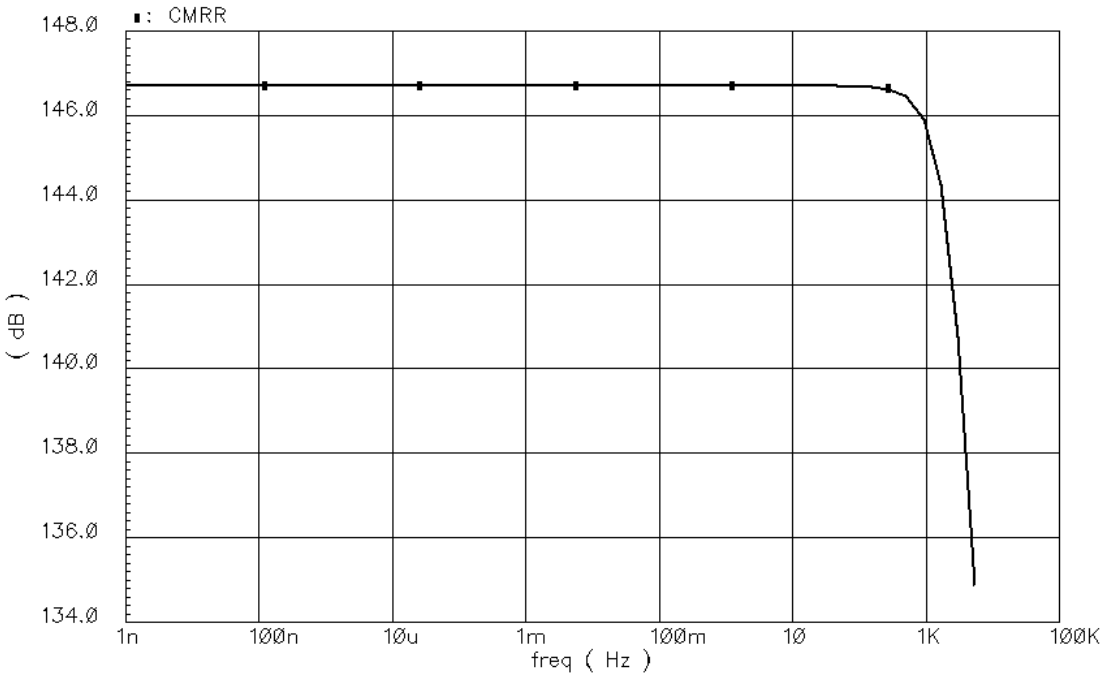

Figure 54: CMRR of proposed CBIA circuit when used with choppers

5.2.6.5) Effect of Chopping on the Output Signal Distortion

Distortion occurs in chopper modulated amplifiers if the circuit delay and the delay between the input and output chopper clock signals are not matched [15]. It causes the signal energy to spread to higher frequencies and reduces the effective gain of the

amplifier as a result. These higher frequency distortion components occur at the chopping frequency and its harmonics and can be easily removed by low pass filtering. Figure 55 shows the input and distorted output signals after chopping.

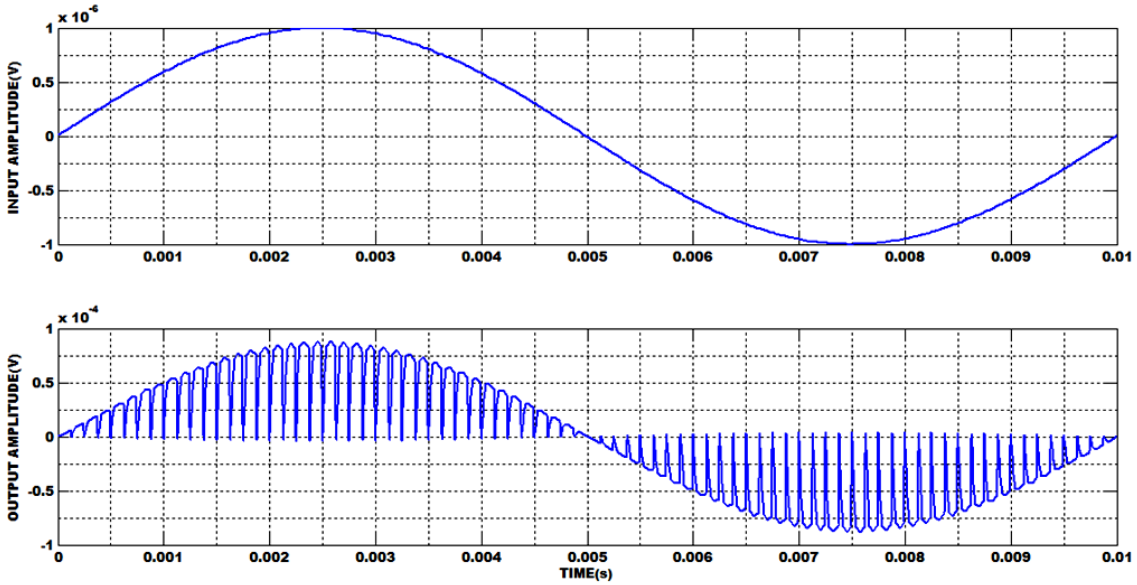

Figure 55: Input and output signals of chopper modulated CBIA showing distorted output signal

From the above results, chopping suppressed the low frequency flicker noise by 27dB and shifted the noise corner frequency from 1kHz to 1Hz. Also the amplifier achieved a very high CMRR of 148dB when choppers were added. However chopping degraded the input impedance to 1.5MΩ, reduced the gain accuracy to 84% and increased the output signal distortion. The above results for the effect of adding choppers to the proposed circuit are summarized in Table 12.

Table 12: Comparison of post layout results with and without chopper modulation

Parameter	With Chopper	Without Chopper
Input Impedance	1.5MΩ	Equivalent of 1.6pF capacitor
Noise corner frequency	1Hz	1kHz
Thermal noise	$46nV/\sqrt{Hz}$	$41.73nV/\sqrt{Hz}$
Gain accuracy	84%	94%
CMRR	148dB	N/A
Distortion	Yes	No

5.3) Experimental Results

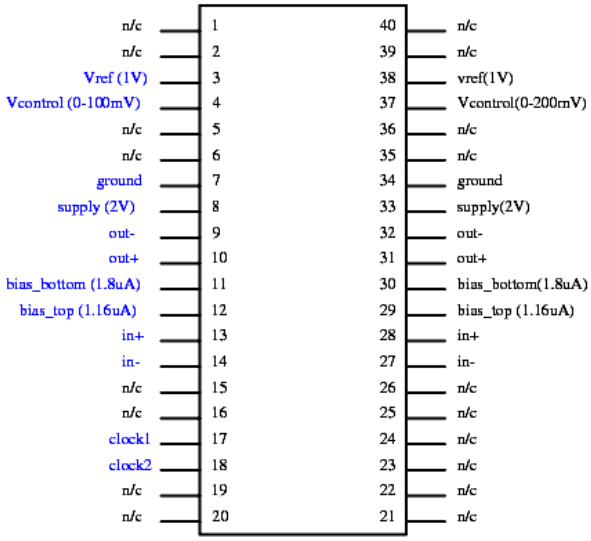

Figure 56: Pin description for chip prototype (DUT)

The device under test (DUT) is shown below in Figure 56. The DUT has 40 pins and contains two circuits, a CBIA circuit with chopper modulators (blue labeled pins)

and a CBIA circuit without chopper modulators (black labeled pins). A brief description of the pins is given in Table 13.

Table 13: Pin description of DUT

Pin Name	Description
Supply	2V dc supply
Ground	ground pin for the circuit
bias_top	1.16uA current source for biasing
bias_bottom	1.8uA current source for biasing
Vcontrol	Variable dc voltage used to vary the output impedance and hence the gain of the circuit
Vref	1V dc voltage used to set the dc level of the output
in+, in-	Positive and negative input signal
out+,out-	Positive and negative output signal
clock1,clock2	300mVpp clock signal for the chopper switches. Clock1 and Clock2 should be complementary, i.e. when clock1 is maximum, clock2 is minimum and vice versa.
n/c	Not connected

5.3.1) Transient Response

The DUT was connected to an hp89410a as shown in Figure 57 below. The hp89410a can be used as a signal source, an oscilloscope and a spectrum analyzer. The

input of the DUT was connected to the signal source and the output was connected to channel 2 of the oscilloscope.

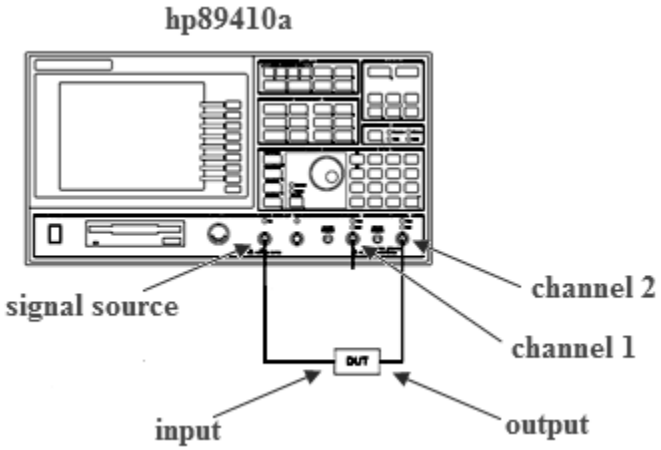

Figure 57: Test setup for transient measurements

An output signal of $3.2mV_{rms}$ was obtained when an input signal of $25\mu V_{rms}$ was applied. The time and frequency domain plots for the input and output signals are shown below in Figure 58 and Figure 59 respectively.

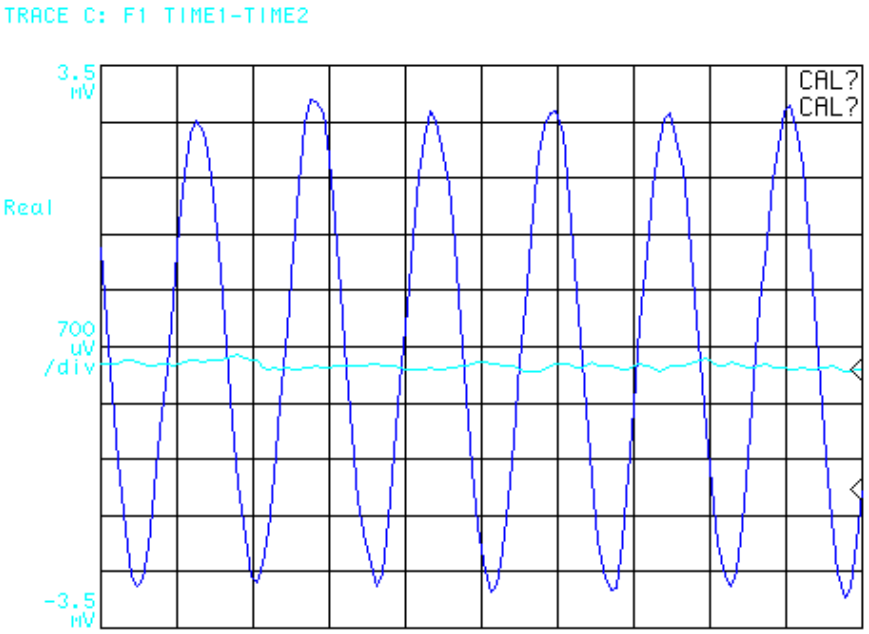

Figure 58: Time domain plot of input signal and amplified output signal

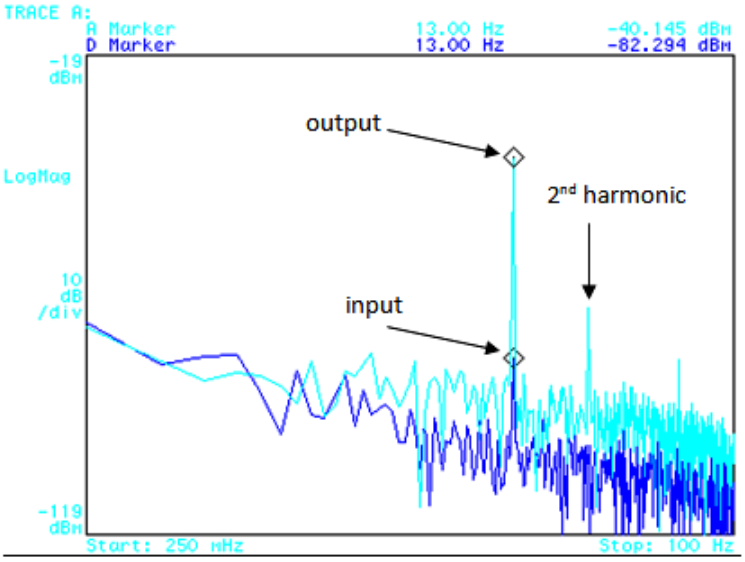

Figure 59: Spectral plots of input and output signals

5.3.2) Frequency Response

The test setup for obtaining the frequency response is shown in Figure 60 below. Details of how to perform this measurement can be found in [22]. The input of the DUT is connected to the signal source from the hp89410a and the output is connected to channel 2 of the spectrum analyzer. Also the signal source is connected to channel 1 of the spectrum analyzer via a BNC connector as shown in Figure 60.

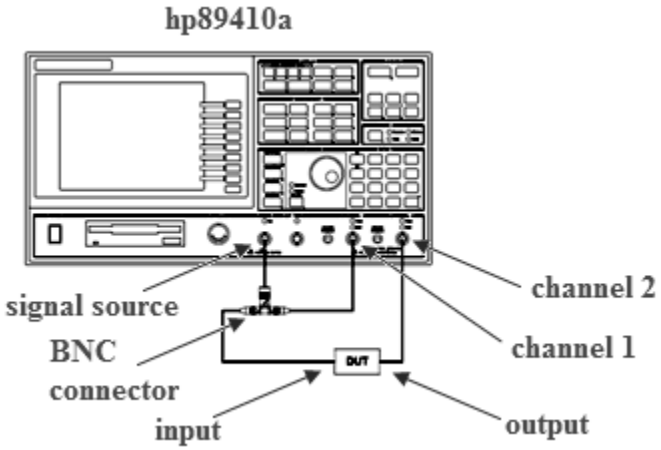

Figure 60: Test setup for frequency response measurement

The plot below in Figure 61 shows a low frequency gain of 39.635dB and a -3dB bandwidth of 13.6 kHz. The low frequency gain can be varied by adjusting the voltage on pin 37 (or Vcontrol).

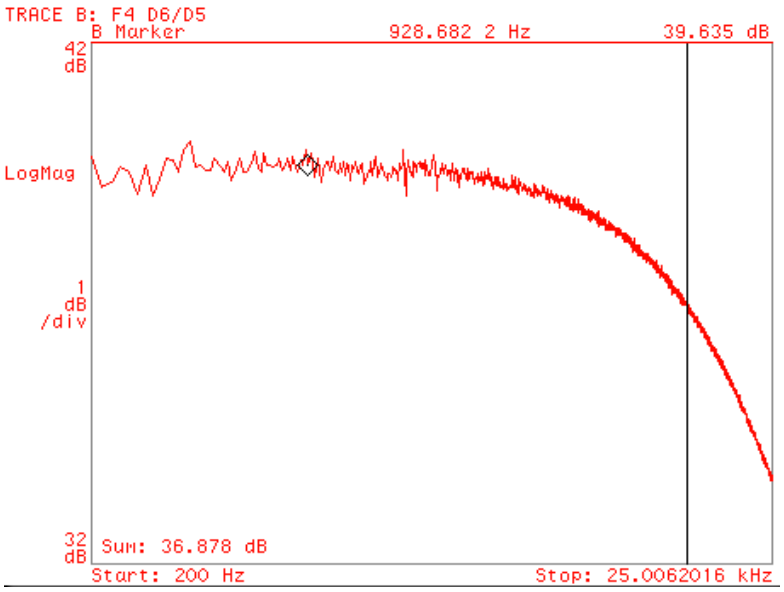

Figure 61: Measured frequency response

5.3.4) Noise

The setup in Figure 60 was used for the noise measurement. With no input signal, the spectral plot of the input referred noise of the DUT is shown in Figure 62 below. The total thermal noise from 4kHz to 8kHz is measured as $3.15\mu V_{rms}$. Within the same 4kHz bandwidth, the noise floor of the hp89410a was measured as $0.715\ \mu V_{rms}$. Thus the input referred thermal spot noise (v_{ni}) can be estimated from the expression

$$\int_{4k}^{8k} (v_{ni}^2)df = (3.15\mu)^2 - (0.715\mu)^2$$

$$v_{ni} = \frac{3.07\mu V_{rms}}{\sqrt{4000}} = 48.5n\ V_{rms}/\sqrt{Hz}$$

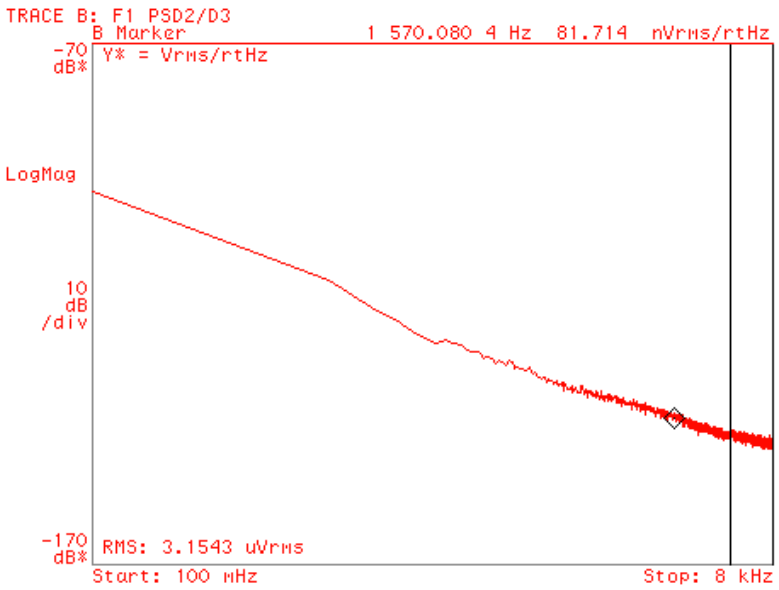

Figure 62: Measured input referred noise PSD

5.3.4.1) Noise Efficiency Factor (NEF)

The DUT consumes a total current of 11.3uA. Consequently the NEF is given by

$$NEF=v_{in_{rms}}\sqrt{\frac{2I_{total}}{\pi 4kT(v_{th})BW}} \;;\quad v_{in_{rms}}=v_{n_{(spot)}}\sqrt{BW(\pi/2)}$$

$$=(48.5\times10^{-9})\sqrt{\frac{(11.3\times10^{-6})}{4(1.38\times10^{-23})(300)(0.026)}}$$

$$NEF=7.8$$

5.3.5) Common Mode Response

The spectral plot below in Figure 63 shows the output differential signal when the signal at the input is common mode. The rejection of common mode signals is important to eliminate high amplitude common mode signals at the input that can saturate the amplifier.

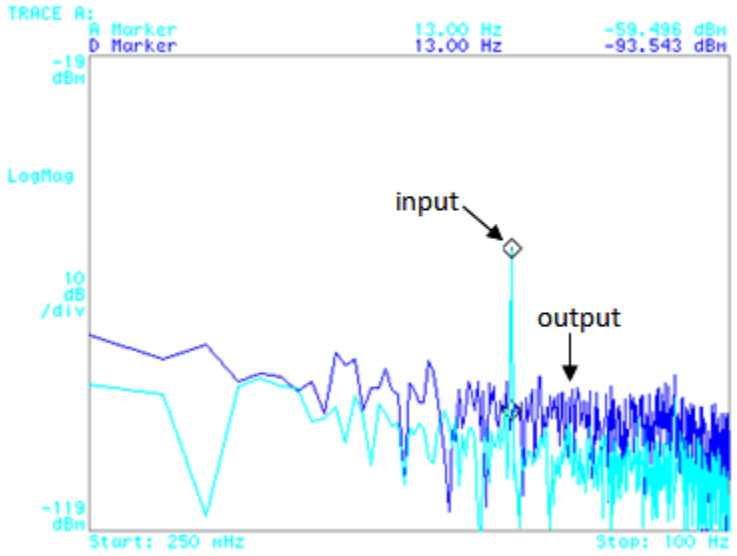

Figure 63: Measured input common mode signal to output differential signal conversion

6. CONCLUSIONS

The Current Balancing Instrumentation Amplifier is the most suitable frontend instrumentation amplifier architecture for biological signal acquisition systems. This is because of its high common mode rejection that is independent on matching of passive elements and its low power consumption. The CBIA architecture has evolved over the years from the first implementation by H. Krabbe [17] towards low voltage and low noise implementations whiles maintaining the gain accuracy and low power consumption. The CBIA implementation proposed in this work improves upon the gain accuracy of the original implementation in [4] by adding an extra gain stage in the forward path of the voltage feedback loop. However, the added gain stage causes the circuit to be unstable and Miller compensation is employed to stabilize it.

Because bioamplifiers are required to process very low amplitude signals at frequencies that can be as low as 500mHz (for EEG signals), the MOS devices used have long channel lengths to reduce their flicker noise. However because silicon area is expensive and parasitic capacitances increase with device area, the channel lengths cannot be increased indefinitely. Instead chopper modulators are used to upconvert the signal at the input to frequencies above the noise corner frequency. After amplification, the upconverted signals are downconverted at the output with chopper modulators to the original baseband frequencies.

The proposed CBIA circuit was implemented in the 0.5um ON semi process. When used with chopper modulators it achieves a gain accuracy of 84%, consumes

11.3uA from 2V supply and achieves input referred noise of 48.5nV/$\sqrt{Hz}$ and a noise corner frequency of 1Hz. A summary of the performance of the proposed chopper modulated CBIA and a comparison with other reported works in the literature is given in Table 14.

Table 14: Performance comparison with other reported works in the literature

Parameter	**This work**	**[1]-2011**	**[4]-2006**	**[2]-2002**	**[3]-2007**
Process	**0.5um**	**0.5um**	**0.5um**	**1.5um**	**0.8um**
Topology	**CBIA**	**CBIA**	**CBIA**	**OPAMP in feedback**	**Folded cascode**
Supply Voltage	**2V**	**2V**	**3V**	**±2.5**	**1.8**
NEF	**7.8**	**5.0**	**9.2**	**4.8**	**4.6**
CMRR *	**>100dB**	**>105dB**	**>110dB**	**>86dB**	**>100dB**
DC OFFSET REJECTION	**Off chip**	**Off chip**	**50mV (on chip)**	**On chip**	**50mV (on chip)**
INPUT NOISE	**48.5nV/√Hz**	**85nV/√Hz**	**60nV/√Hz**	**231nV/√Hz**	**97.5nV/√Hz**
GAIN	**Variable**	**Variable**	**variable**	**Fixed=39.8dB**	**Fixed=41dB**
ACCURACY*	**84%**	**N/A**	**N/A**	**97.7%**	**N/A**
INPUT IMPEDANCE	**10Mohm (off chip resistor)**	**10Mohm (off chip resistor)**	**N/A**	**High**	**5Mohm**
Current	**11.3uA**	**1.35uA**	**11.1uA**	**180nA**	**1uA**
Chopped	**Yes**	**Yes**	**Yes**	**No**	**Yes**

***values are from post layout simulation results**

Compared with other works in the literature, the proposed circuit achieves the lowest thermal spot noise and has the best accuracy among all the CBIA implementations.

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