

**DESIGN OF A WIDE BANDWIDTH CONTINUOUS-TIME LOW-PASS
SIGMA-DELTA MODULATOR**

A Thesis

by

CHENG-MING CHIEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2011

Major Subject: Electrical Engineering

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Approved by:

Co-Chairs of Committee, Aydin I. Karsilayan
Jose Silva-Martinez

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Duncan M. Walker

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ABSTRACT

Design of a Wide Bandwidth Continuous-time Low-pass Sigma-delta Modulator.

(December 2011)

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Co-Chairs of Advisory Committee: Dr. Aydin I. Karsilayan
Dr. Jose Silva-Martinez

The emergence of bandwidth-intensive services has created a need for high speed and high resolution data converters. Towards this end, system level design of a continuous-time sigma-delta modulator achieving 11 bits resolution over 100 MHz signal bandwidth by using a feed-forward topology is presented. The system is first built in the Simulink environment in MATLAB. The building blocks in the loop filter are modeled with non-idealities, and specifications for these blocks are obtained by simulations. An operational transconductor amplifier (OTA) with 100 mS transconductance, 70 dB linearity, and 34.2 mW power dissipation is designed to be used in the loop filter. Simulation results indicate that the 5th order loop filter implemented in the feed-forward architecture in transistor level shows lower power consumption, 105 mW, compared to the loop filter implemented by feedback architecture, 152 mW.

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1. INTRODUCTION

Receivers for wireless communications are becoming more and more digital, where analog functions are being realized by digital processors. As a result, analog-to-digital converters (ADC) are gradually moving towards the antenna. However, this places much higher requirements of bandwidth and dynamic range on the ADCs. In addition, the quest for higher data rates is leading to the rise of standards with larger signal bandwidths. This further increases the need for wide bandwidth ADCs. Fig. 1 shows the traditional super-heterodyne receiver architecture and software defined radio.

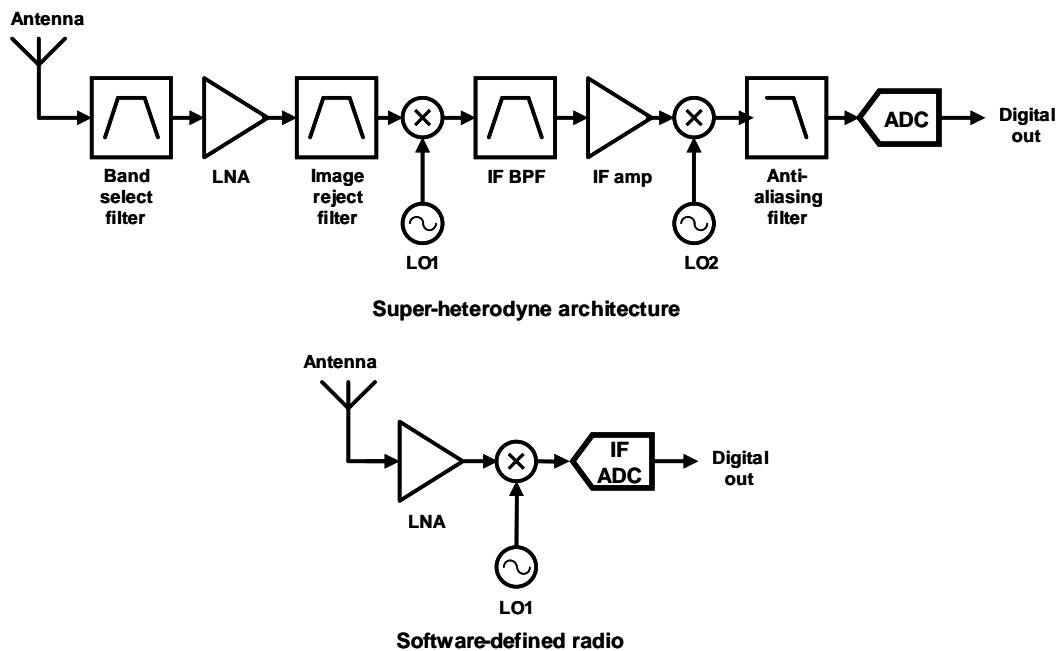


Figure 1: Comparison of radio architectures

As can be seen in Fig. 1, in the traditional architecture, analog to digital conversion is preceded by significant analog processing. In the more digital-intensive software-defined radio architecture, the signal is digitized much earlier, enabling filtering and amplification operations in digital domain.

This thesis follows the style of *IEEE Journal of Solid State Circuits*.

1.1 Nyquist ADCs

Analog-to-digital converters are the interface between the real world which is continuous-time and continuous-amplitude in nature (e.g., voice, audio or video) and the digital world where only discrete-time and discrete-amplitude signals exist. Fig. 2 shows the major blocks involved in analog-to-digital conversion process.

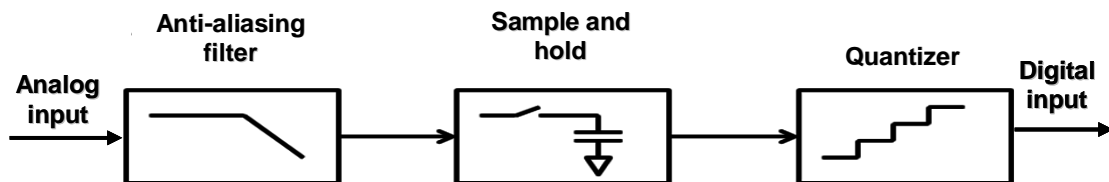


Figure 2: Signal processing chain

Assume the input analog signal has useful content up to a frequency of f_b . The sample-and-hold block shown in Fig. 2 performs the operation of converting the continuous-time signal into a discrete-time signal. The sampling frequency (f_s) has to satisfy the Nyquist criterion shown in the following equation in order to avoid losing information when sampling:

$$f_s \geq 2 \cdot f_b \quad (1.1)$$

The anti-aliasing filter (AAF) shown in Fig. 2 removes any signal with frequencies higher than f_b to prevent aliasing. Therefore, the AAF is prior to the sample-and-hold block in the signal chain.

The quantizer shown in Fig. 2 performs the conversion from continuous to discrete amplitudes. Although the discretization process in time domain is lossless, the quantization process is inherently lossy. The error introduced by the quantization process is dependent on the number of bits of the quantizer.

For a quantizer with a full-scale value of $\pm V_{ref}$ and output of N digital bits, the step size, Δ , of the quantizer is given by,

$$\Delta = \frac{2V_{ref}}{2^N} \quad (1.2)$$

The quantization error, ϵ , introduced in the quantization operation at every sampling instant stays in the range $(-\Delta/2, \Delta/2)$. If the input signal of a quantizer is sufficiently ‘busy’, then the behavior of the quantization error can be considered a white noise process with the probability density function shown in Fig. 3 [1].

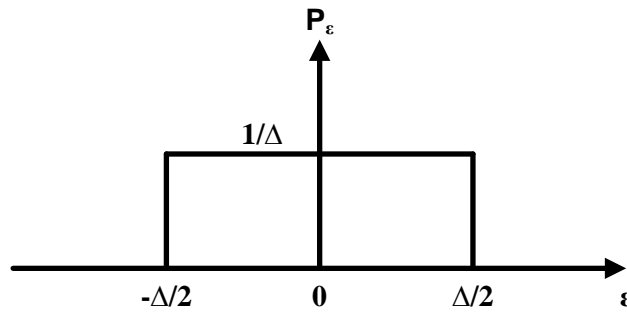


Figure 3: Quantization noise probability density function

The quantization noise introduced can be calculated as:

$$\sigma_{\epsilon}^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \epsilon^2 \frac{1}{\Delta} d\epsilon = \frac{\Delta^2}{12} \quad (1.3)$$

For a full-scale sine-wave as the input of the quantizer, the power of this sine wave is given by $(V_{ref}^2/2)$. Knowing the input signal and quantization noise power level, the signal to quantization noise can be obtained as:

$$SQNR = \frac{(2^{N-1} \Delta)^2}{\frac{2}{\frac{\Delta^2}{12}}} = \frac{3}{2} \cdot 2^{2N} \quad (1.4)$$

For the more familiar expression relating SNR with an equivalent number of bits, equation (1.4) can be expressed in dB as:

$$SQNR(dB) = 6.02N + 1.76 \quad (1.5)$$

ADCs with sampling rate equal to twice the signal bandwidth are called Nyquist-rate ADCs.

1.2 Oversampling ADC

The expression for quantization noise power was obtained in the previous section. Since this noise is considered as a white noise process, the power is distributed equally across all frequencies from DC to half the sampling rate. If the signal were to be sampled at a higher rate than the Nyquist rate, the same quantization noise power is spread over a higher frequency range. Thus, the in-band noise gets reduced, and the signal-to-quantization noise ratio (SQNR) is improved as shown in Fig. 4 [1].

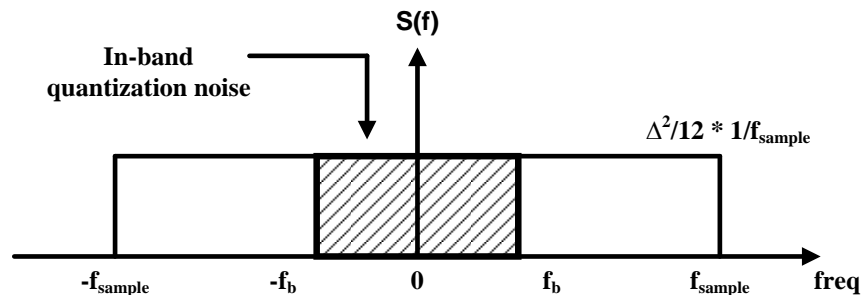


Figure 4: Oversampled quantization noise power spectral density profile

The improvement in SQNR due to oversampling is quantified by [2],

$$SQNR(dB) = 6.02N + 1.76 + 10\log_{10} OSR \quad (1.6)$$

where $OSR = \frac{f_{sample}}{2f_b}$

Based on equation (1.6), doubling OSR improves SQNR around 3 dB.

1.3 Sigma-delta ($\Sigma\Delta$) ADC

Improving SQNR only by increasing OSR is an expensive and inefficient method. A more efficient way is by using some method that could shape the quantization noise from signal band to outside the band of interest. This is the principle of sigma-delta ADC. A simple block diagram of a first order sigma-delta converter is shown in Fig. 5.

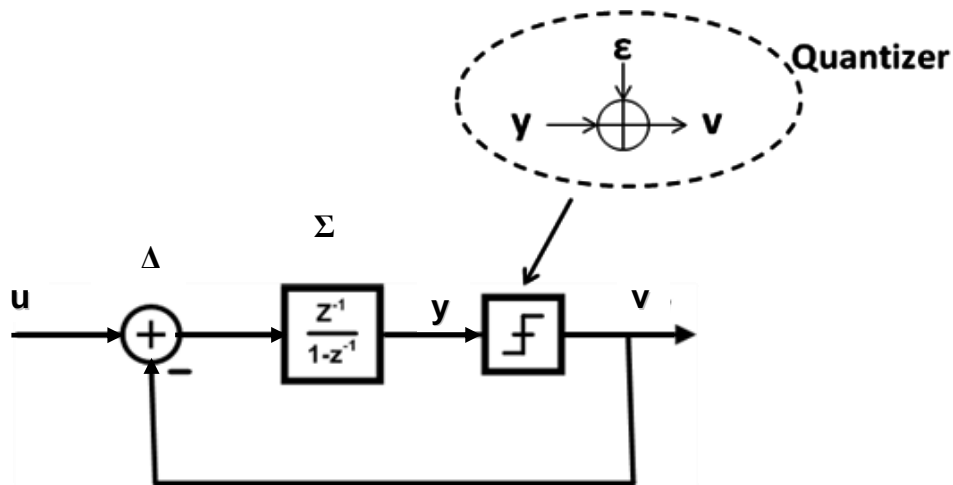


Figure 5: First order sigma-delta modulator

Assume that quantization noise is an additive noise. Fig. 5 shows a linear system with two inputs and single output. The output can be expressed as:

$$v = STF \cdot u + NTF \cdot \epsilon \quad (1.7)$$

where signal transfer function (STF) and noise transfer function (NTF) are defined as:

$$STF = \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \quad (1.8)$$

$$NTF = \frac{V(z)}{E(z)} = \frac{1}{1+H(z)} = 1-z^{-1} \quad (1.9)$$

Based on equation (1.8), the signal appears unchanged at the output with just a delay. However, the noise is shaped as shown in Fig. 6.

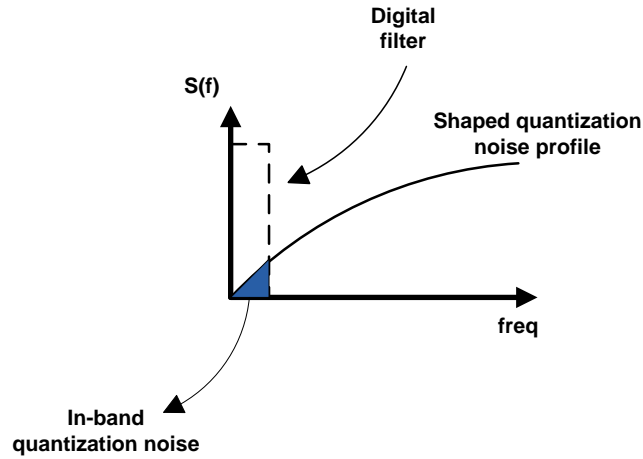


Figure 6: First order modulator quantization noise profile

In the above example, the quantization noise is shaped out-of-band by a first order transfer function. In order to further improve SQNR, higher orders of the loop filter can be used. By using an L order loop filter, the NTF can be obtained as:

$$NTF = (1 - z^{-1})^L \quad (1.10)$$

The SQNR in such a case is calculated as [2],

$$SQNR_{\max} [dB] = 6.02N + 1.76 + (20L + 10) \log_{10} OSR - 10 \log_{10} \frac{\pi^{2L}}{2L+1} \quad (1.11)$$

Therefore, the SQNR improves by increasing the order of the loop filter of sigma-delta ADC.

1.4 Thesis organization

The organization of this thesis is highlighted in this section.

Section 2 presents the system design of a continuous-time sigma-delta ADC, the loop filter implementation, and the simulated results using Simulink. The specifications of the loop filter components are derived based on the simulated results of the Simulink macro-model by adding non-idealities.

Section 3 presents the design of operational transconductor amplifier (OTA). The non-linear small signal model is built for optimizing power consumption. The noise and frequency response are analyzed by using small signal models as well. At last, the performances of OTAs implemented in transistor level are presented.

Section 4 presents simulated results of the loop filter and system simulated results with the loop filter in transistor level.

Section 5 presents a summary of this research with some directions for future work.

2. SYSTEM LEVEL DESIGN OF $\Sigma \Delta$ MODULATOR

Continuous-time $\Sigma \Delta$ ADCs are becoming more popular recently than discrete-time $\Sigma \Delta$ ADCs primarily because of their reduced settling time requirements that results in better power efficiency shown in Fig. 7. In addition, they have some other advantages such as inherent anti-aliasing and reduced sample-and-hold requirements. However, they do have some disadvantages such as higher sensitivity to clock jitter and susceptibility to time-constant variations. In spite of these disadvantages, there has been a tremendous interest in continuous-time $\Sigma \Delta$ ADCs as seen by papers published in the recent literature [3], [4].

In the past decades, the design methodologies of discrete-time sigma-delta modulators have been thoroughly studied, and many good design tools are available, e.g. the $\Delta \Sigma$ MATLAB toolbox by Richard Schreier [5]. It is very common to obtain a discrete-time loop transfer function first, and then to use the impulse-invariant transformation to convert it to a continuous-time loop transfer function [6]. In this work, this approach is followed as well. However, it should be noted that this approach is not the only way to design a continuous-time $\Sigma \Delta$ modulator. The loop filter can be directly synthesized in the continuous-time domain [7], [2].

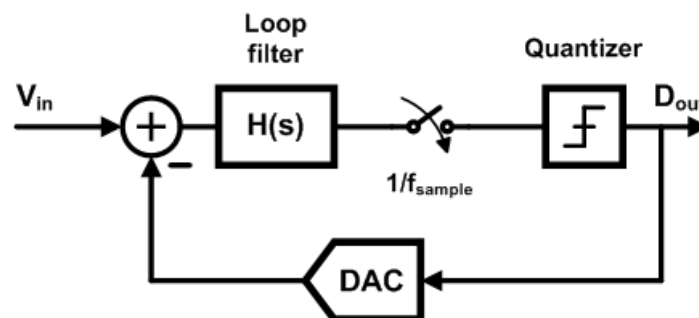


Figure 7: Continuous-time $\Sigma \Delta$ modulator

2.1 Design considerations

The target of this work is to realize a continuous-time $\Sigma\Delta$ modulator with the specifications given in Table 1 using Jazz 0.18 μm technology.

Table 1: $\Sigma\Delta$ Modulator Target Specifications

Performance parameter	Target specification
Bandwidth	100 MHz
Resolution	11 bits
Power consumption	< 500 mW

The first step of the design process is to obtain a noise transfer function (NTF) for the target specifications. In order to use the MATLAB toolbox by Richard Schreier to obtain a NTF, some variables for system level design are required [8]. The required variables for system-level design are over-sampling ratio (OSR), number of levels in the internal quantizer (N_L), order of the loop filter (L) and out-of-band gain of the NTF (NTF_{max}).

The signal-to-quantization ratio (SQNR) of an L^{th} order modulator with an N-bit internal quantizer and working at an oversampling ratio OSR is given by.

$$SQNR_{\max} [dB] = 6.02N + 1.76 + (20L + 10) \log_{10} OSR - 10 \log_{10} \frac{\pi^{2L}}{2L + 1} \quad (2.1)$$

Based on equation (2.1), increasing over-sampling ratio (OSR), number of bits in the internal quantizer (N), or order of the loop filter (L), improves the SQNR. However, each of the parameters has its limitation for realistic designs as discussed below.

First, increasing the OSR gives better SQNR. However, the maximum speed of operation is usually limited by technology to some finite value. Also, operation at higher speeds leads to higher power consumption.

Second, increasing number of bits of the internal quantizer obtaining smaller quantization noise improves the SQNR. However, increasing number of bits of the internal quantizer also increases the power and area of the implementation of the quantizer exponentially. Also, the number of bits of digital-to-analog converter (DAC) used in the feedback path increase simultaneously with increasing number of bits of the internal quantizer, which increases the area and complexity of the DAC design. In addition, parasitic capacitance of the internal quantizer increases when the number of bits of the quantizer increases and this may affect stability.

Third, increasing the order of the modulator leads to higher SQNR. However, higher order modulators are more difficult to stabilize, and usually the order of a practical system is limited to 5 [9].

Finally, increasing the maximum gain of the NTF outside the signal band (NTF_{\max}) reduces the noise inside the signal band and improves SQNR. However, higher values of NTF_{\max} degrade the performance of the modulator when high frequency noise such as clock jitter is present in the system.

Based on simulations in MATLAB using Richard Schreier $\Sigma\Delta$ toolbox, the above mentioned variables were picked for the targeted SQNR as shown in Table 2, The discrete-time NTF is given by:

$$NTF(z) = \frac{z^5 - 4.433z^4 + 7.992z^3 - 7.320z^2 + 3.406z - 0.644}{z^5 - 2.680z^4 + 3.207z^3 - 2.035z^2 + 0.677z - 0.093} \quad (2.2)$$

Table 2: Noise transfer function parameters

Parameters	Value
OSR	10
Quantizer bits (N)	3
Order (L)	5
NTF_{\max}	3.4

Figure 8 shows the magnitude plot of (2.2).

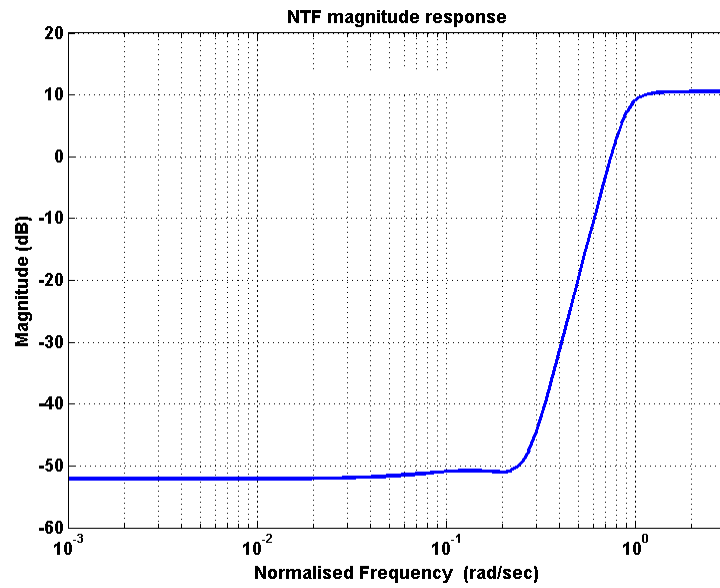


Figure 8: Noise transfer function

The zeros and poles of NTF located in Z-domain are shown in Fig. 9

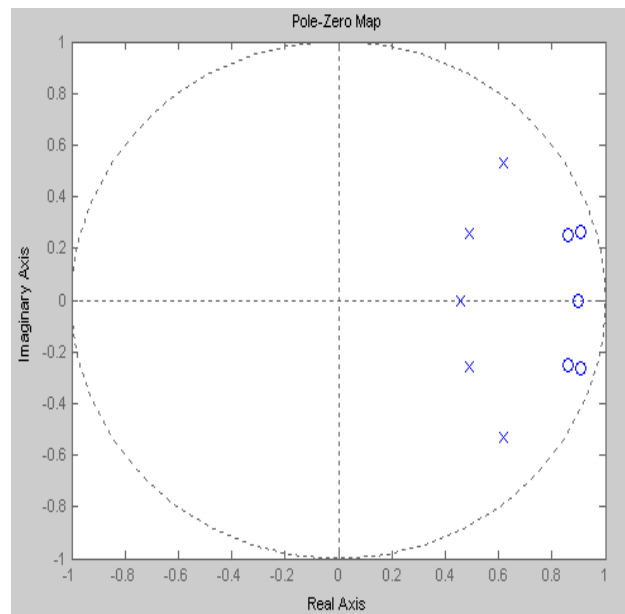


Figure 9: Zero and pole locations of NTF

The second step is to obtain the discrete-time loop transfer function (LTF). Once the NTF is known, the LTF of the modulator can be obtained as:

$$LTF = \frac{1}{NTF} - 1 \quad (2.3)$$

The corresponding loop transfer function is

$$LTF(z) = \frac{2.253z^4 - 5.539z^3 + 5.727z^2 - 2.801z + 0.539}{z^5 - 4.387z^4 + 7.797z^3 - 7.016z^2 + 3.196z - 0.589} \quad (2.4)$$

Usually, one clock cycle is needed for the operation of the quantizer and DAC. Therefore, z^{-1} (representing one cycle delay) is factored out from the LTF, which then becomes

$$H(z) = \frac{2.253z^5 - 5.539z^4 + 5.727z^3 - 2.801z^2 + 0.539z}{z^5 - 4.387z^4 + 7.797z^3 - 7.016z^2 + 3.196z - 0.589} \quad (2.5)$$

The last step is to obtain the continuous-time loop filter transfer function, $H(s)$, by converting $H(z)$ using Impulse-Invariant transformation [9].

Impulse-Invariant Transformation: The equivalence of discrete-time and continuous-time $\Sigma\Delta$ modulators is illustrated in Fig. 10. The main difference between two modulators is that signal is sampled at the input for a discrete-time $\Sigma\Delta$ modulator, but, for a continuous-time $\Sigma\Delta$ modulator, signal is sampled inside the loop before the quantizer. By breaking the loops at the digital-to-analog converter (DAC) inputs of discrete-time and continuous-time modulators, the corresponding open loop structures are obtained as shown in Fig. 10. For the same input, the outputs of the two open loops at the sampling instants should be the same if the two loops are identical:

$$x(n)_d = x(t)\Big|_{t=nT_s} \quad (2.6)$$

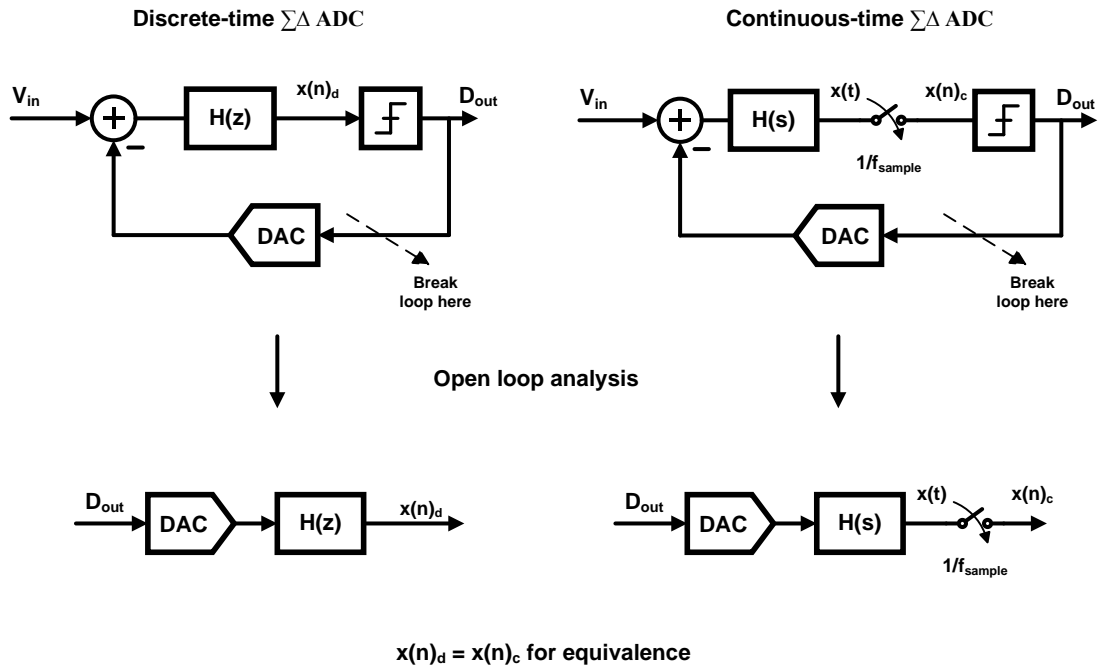


Figure 10: Equivalence of continuous and discrete-time modulators

If the impulse responses of the two loops are the same, then equation (2.6) can be rewritten as:

$$Z^{-1}[H(z)] = L^{-1}[H_d(s) * H(s)] \quad (2.7)$$

where Z^{-1} and L^{-1} are inverse Z and Laplace transforms, respectively. $H_d(s)$ represents the frequency response of the DAC in the feedback loop.

In the time domain, equation (2.7) can be expressed as:

$$h(n) = \{h_d(t) * h(t)\} \Big|_{t=nT_s} \quad (2.8)$$

where $h(n)$, $h_d(t)$ and $h(t)$ represent the impulse responses of the discrete-time loop filter, the DAC and the continuous-time loop filter, respectively.

Based on equation (2.8), different DAC pulses result in different $H(s)$ for a given $H(z)$. Therefore, it is necessary to determine the shape of the feedback DAC waveform first.

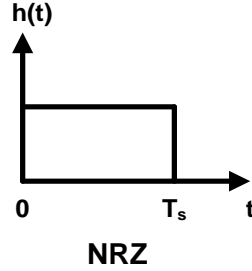


Figure 11: NRZ DAC pulses

In this work, the non-return-to-zero (NRZ) DAC waveform shown in Fig. 11 is used for its better jitter tolerance. The return-to-zero (RZ) DAC waveforms have more number of transitions on average in each clock cycle. As a result, they are more sensitive to clock jitter than the NRZ DAC pulse shape.

For the case of the NRZ DAC, the impulse invariant transformation is available in MATLAB using the built-in function 'd2c'. Then, the corresponding continuous-time loop filter transfer function is obtained as follows:

$$H(s) = \frac{2.253s^5 + 8.716 \times 10^9 s^4 + 1.719 \times 10^{19} s^3 + 2.212 \times 10^{28} s^2 + 1.811 \times 10^{37} s + 7.571 \times 10^{45}}{s^5 + 1.056 \times 10^9 s^4 + 9.471 \times 10^{17} s^3 + 4.115 \times 10^{26} s^2 + 1.418 \times 10^{35} s + 1.881 \times 10^{43}} \quad (2.9)$$

2.2 Loop filter implementation

In continuous-time $\Sigma\Delta$ modulators, two popular architectures are widely used: feedback and feed-forward architectures. Both of them have their own advantages and disadvantages. For feedback architectures, the advantages are a large adder is not required before the quantizer as compared to feed-forward architecture. However, for low-power design, the feed-forward architecture is preferred because the input swing of the first stage transconductor in the feed-forward loop filter is much smaller than that of the feedback counterpart. This significantly reduces the power requirement of the first stage transconductor, which is usually the major part of the total power consumption of the loop filter. However, the feed-forward architecture has its drawbacks as well. The out-of-band peaking in the signal transfer function of the feed-forward loop filter reduces the dynamic range of the modulator [10], [1].

In this work, the feed-forward architecture is chosen because of its low-power consumption property. Comparison of simulated results and discussion between feedback and feed-forward architectures will be shown in Section 4.

In continuous-time $\Sigma\Delta$ modulators, the loop filters are generally implemented as a cascade of integrators or resonators comprised of biquads. Consequently, when the bandwidth of interest in a modulator implementation increases, the power consumption in the amplifier within the integrators or biquads rises to have room for the higher frequency signal. Therefore, the use of passive filters comprised of LC sections is explored in this work.

In order to implement the loop transfer function (2.9) by cascading biquads, first, the denominator of the loop transfer function (2.9) can be rearranged as:

$$(s + 2.11 \times 10^8)(s^2 + 2.35 \times 10^8 s + 3.36 \times 10^{17})(s^2 + 4.35 \times 10^8 s + 3.71 \times 10^{17}) \quad (2.10)$$

From equation (2.10), we can see that there are two second order polynomials and one first order polynomial which can be implemented by cascading two biquads and one RC low-pass filter. A biquad to be used for feed-forward architecture must include both band-pass and low-pass output nodes for the same input node. The suitable biquad is shown in Fig. 12.

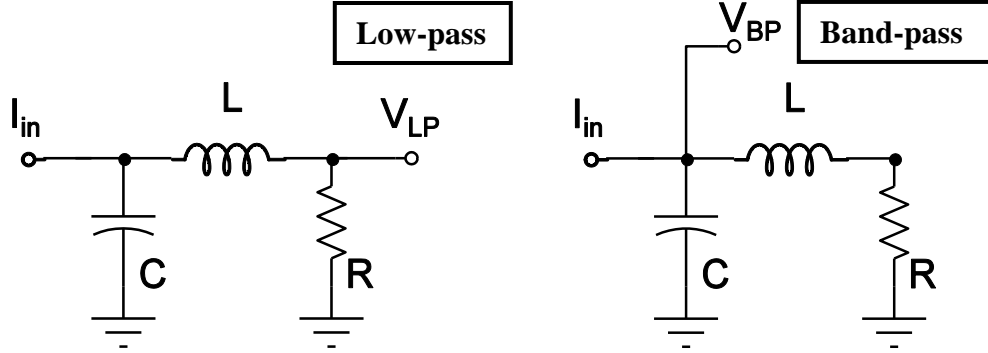


Figure 12: Low-pass and band-pass nodes of biquad

The corresponding transfer functions from I_{in} to V_{LP} and V_{BP} can be found as:

$$\frac{V_{LP}(s)}{I_{in}(s)} = \frac{R\omega_n^2}{s^2 + s\left(\frac{\omega_n}{Q}\right) + \omega_n^2} \quad (2.11)$$

$$\frac{V_{BP}(s)}{I_{in}(s)} = \frac{s\left(\frac{1}{C}\right) + R\omega_n^2}{s^2 + s\left(\frac{\omega_n}{Q}\right) + \omega_n^2} \quad (2.12)$$

where $\omega_n = \frac{1}{\sqrt{LC}}$ and $Q = \frac{\omega_n L}{R}$

Next, the numerator of the loop transfer function (2.9) is implemented. Because the numerator has six coefficients from 5th order to constant, it requires six independent paths to implement it. However, with an implementation consisting only of two biquads,

which gives four paths and one fast-path directly from output of quantizer to the input of quantizer, the sum of the total number of paths is only five. Therefore, an additional feedback path is required for feed-forward LC loop filter implementation. The additional path is chosen from output of quantizer feeding back current to the first order RC section before the quantizer, which increases its denominator order by one compared to the fast-path. A single-ended representation of the proposed low-pass loop filter with feed-forward paths included is shown in Fig. 13.

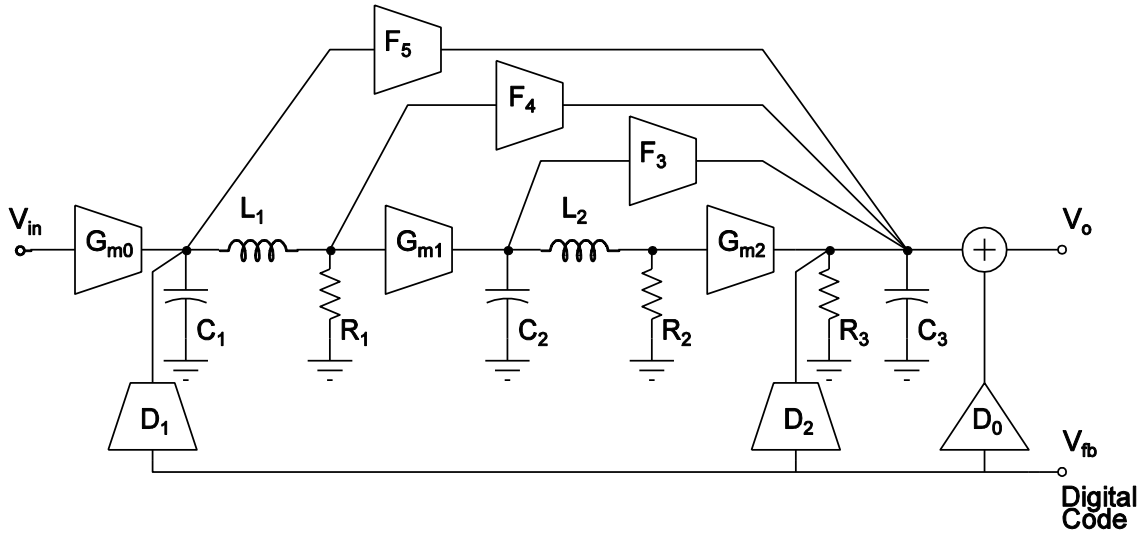


Figure 13: Proposed low-pass feed-forward LC loop filter

The loop transfer function of the filter in Fig. 13 is given by,

$$\begin{aligned} \frac{V_o(s)}{V_{fb}(s)} = & D_0 + \frac{1}{C_3} \frac{D_2}{s + \omega_3} + \frac{D_1}{C_3} \frac{F_5}{s + \omega_3} \frac{\left(\frac{s}{C_1} + R_1 \omega_1^2 \right)}{s^2 + s \left(\frac{\omega_1}{Q_1} \right) + \omega_1^2} + \frac{D_1}{C_3} \frac{F_4}{s + \omega_3} \frac{R_1 \omega_1^2}{s^2 + s \left(\frac{\omega_1}{Q_1} \right) + \omega_1^2} \\ & + \frac{D_1}{C_3} \frac{F_3}{s + \omega_3} \frac{R_1 \omega_1^2}{s^2 + s \left(\frac{\omega_1}{Q_1} \right) + \omega_1^2} \frac{G_{m1} \left(\frac{s}{C_2} + R_2 \omega_2^2 \right)}{s^2 + s \left(\frac{\omega_2}{Q_2} \right) + \omega_2^2} + \frac{G_{m2}}{C_3 (s + \omega_3)} \frac{G_{m1} R_2 \omega_2^2}{s^2 + s \left(\frac{\omega_2}{Q_2} \right) + \omega_2^2} \frac{R_1 \omega_1^2 D_1}{s^2 + s \left(\frac{\omega_1}{Q_1} \right) + \omega_1^2} \end{aligned} \quad (2.13)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L_1 C_1}} \quad \omega_2 = \frac{1}{\sqrt{L_2 C_2}} \quad \omega_3 = \frac{1}{R_3 C_3} \quad Q_1 = \frac{\omega_1 L_1}{R_1} \quad Q_2 = \frac{\omega_2 L_2}{R_2}$$

Now, it is time to calculate all the parameters of the loop filter. First, based on the equation (2.10) and the denominator of the equation (2.11), the biquad component values can be calculated. Since the inductor values (\mathbf{L}_1 and \mathbf{L}_2) are fixed to 100 nH, chosen to be the maximum value from the technology of Coilcraft, the capacitor values (\mathbf{C}_1 and \mathbf{C}_2) and resistor values (\mathbf{R}_1 and \mathbf{R}_2) are also fixed based on equation (2.10) and (2.11). The resistor value (\mathbf{R}_3) is determined by DC gain of the loop transfer function (2.9). Then, the capacitor values (\mathbf{C}_3) can be calculated from equation (2.10). G_{m0} in Fig. 13 only performs unit voltage to current conversion, which value is 30 mS.

Next, in order to calculate the feedback and feed-forward coefficients in Fig. 13, by comparing the coefficients of the numerator of equation (2.9) to equation (1.13), each term with the same order in the numerator of equation (2.13) should be put together to form six polynomials from 5th order to constant as follows:

- The 5th order terms in the numerator of equation (2.13) is shown in the polynomial,

$$D_0 s^5 \quad (2.14)$$

- The 4th order terms in the numerator of equation (2.13) is shown in the polynomial,

$$\left[D_0 \frac{\omega_1}{Q_1} + D_0 \frac{\omega_2}{Q_2} + D_0 \omega_3 + \frac{D_2}{C_3} \right] s^4 \quad (2.15)$$

- The 3rd order terms in the numerator of equation (2.13) is shown in the polynomial,

$$\left[D_0 \omega_1^2 + D_0 \frac{\omega_1}{Q_1} \frac{\omega_2}{Q_2} + D_0 \omega_2^2 + D_0 \omega_3 \frac{\omega_1}{Q_1} + D_0 \omega_3 \frac{\omega_2}{Q_2} + \frac{D_2}{C_3} \frac{\omega_1}{Q_1} + \frac{D_2}{C_3} \frac{\omega_2}{Q_2} + \frac{D_1}{C_3} \frac{F_5}{C_1} \right] s^3 \quad (2.16)$$

- The 2nd order terms in the numerator of equation (2.12) is shown in the polynomial,

$$\left[D_0 \omega_1^2 \frac{\omega_2}{Q_2} + D_0 \omega_2^2 \frac{\omega_1}{Q_1} + D_0 \omega_3 \omega_1^2 + D_0 \omega_3 \frac{\omega_1 \omega_2}{Q_1 Q_2} + D_0 \omega_3 \omega_2^2 + \omega_1^2 \frac{D_2}{C_3} + \frac{D_2}{C_3} \frac{\omega_1 \omega_2}{Q_1 Q_2} \right. \\ \left. + \omega_2^2 \frac{D_2}{C_3} + \frac{D_1 F_5}{C_3 C_1} \frac{\omega_2}{Q_2} + F_5 R_1 \omega_1^2 \frac{D_1}{C_3} + F_4 R_1 \omega_1^2 \frac{D_1}{C_3} \right] s^2 \quad (2.17)$$

- The 1st order terms in the numerator of equation (2.13) is shown in the polynomial,

$$\left[D_0 \omega_1^2 \omega_2^2 + D_0 \omega_3 \omega_1^2 \frac{\omega_2}{Q_2} + D_0 \omega_3 \omega_2^2 \frac{\omega_1}{Q_1} + \omega_1^2 \frac{D_2}{C_3} \frac{\omega_2}{Q_2} + \omega_2^2 \frac{D_2}{C_3} \frac{\omega_1}{Q_1} + F_5 R_1 \omega_1^2 \frac{D_1}{C_3} \frac{\omega_2}{Q_2} \right. \\ \left. \omega_2^2 \frac{D_1 F_5}{C_3 C_1} + F_4 R_1 \omega_1^2 \frac{D_1}{C_3} \frac{\omega_2}{Q_2} + R_1 \omega_1^2 G_{m1} \frac{D_1 F_3}{C_3 C_2} \right] s \quad (2.18)$$

- The constant terms in the numerator of equation (2.13) is shown in the polynomial,

$$D_0 \omega_3 \omega_1^2 \omega_2^2 + \omega_1^2 \omega_2^2 \frac{D_2}{C_3} + F_5 R_1 \omega_1^2 \omega_2^2 \frac{D_1}{C_3} + F_4 R_1 \omega_1^2 \omega_2^2 \frac{D_1}{C_3} + F_3 R_1 \omega_1^2 G_{m1} R_2 \omega_2^2 \frac{D_1}{C_3} \\ + G_{m1} R_2 \omega_2^2 R_1 \omega_1^2 D_1 \frac{G_{m2}}{C_3} \quad (2.19)$$

By comparing the coefficients of the numerator of equation (2.9) to polynomials (2.14) - (2.19), each equation only has one unknown which is either feedback or feed-forward coefficient. Thus, all unknown coefficients can be solved. The parameters of the modulator obtained after performing the comparison mentioned above shown in Table 3. The model of the system built in MATLAB Simulink is shown in Fig. 14.

Table 3: Modulator component values

D₀	0.45	L₁	100 nH	L₂	100 nH
D₁	6.9 mS	C₁	36 pF	C₂	31 pF
D₂	1.5 mS	R₁	33 Ω	R₂	51 Ω
F₃	1.7 mS	G_{m1}	100 mS	G_{m2}	1.3 mS
F₄	6.0 mS	R₃	4 kΩ	C₃	1.2 pF
F₅	2.4 mS				

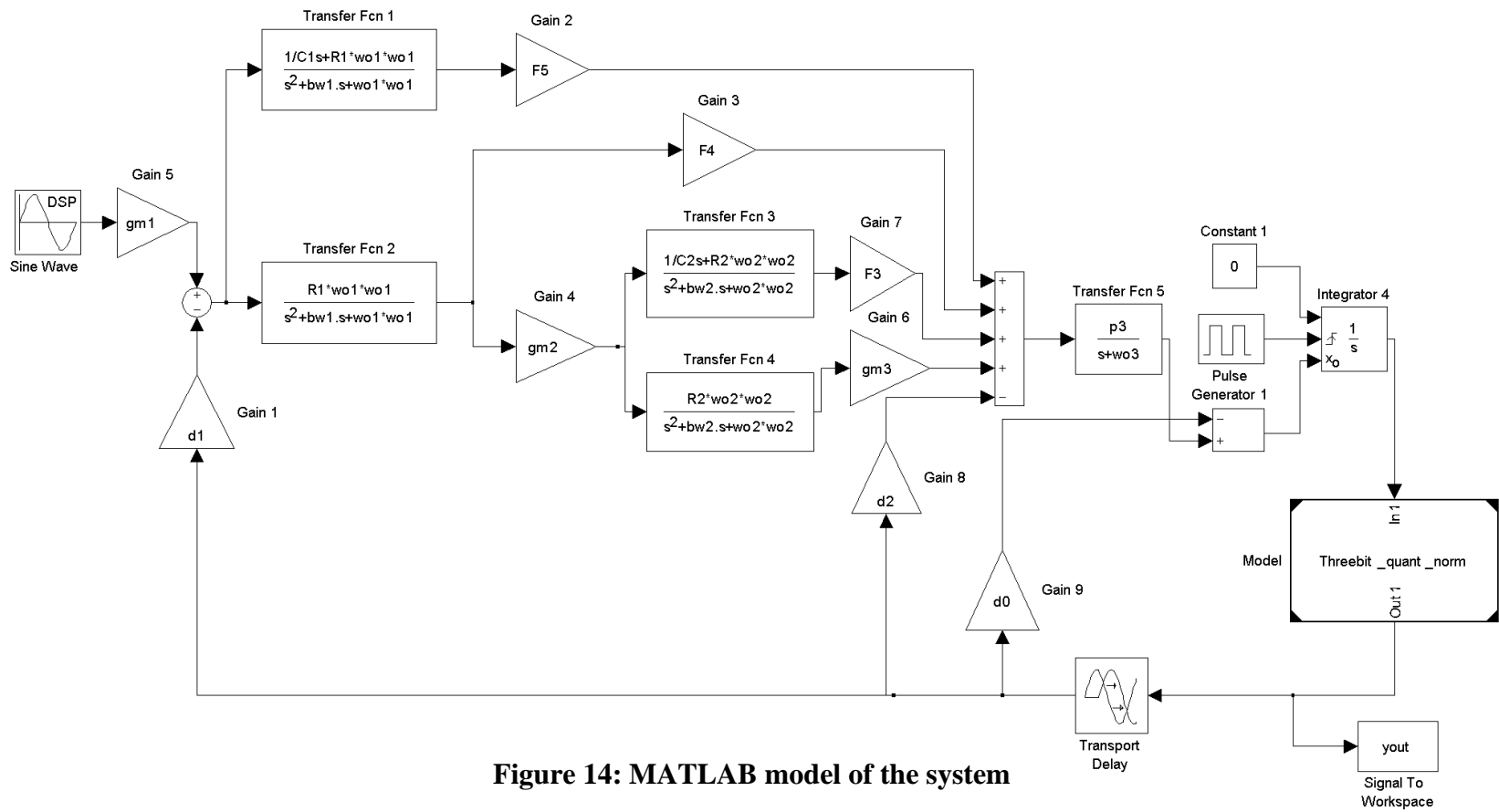


Figure 14: MATLAB model of the system

2.3 Simulation results

A macro-model of the system was built in MATLAB using Simulink. The output obtained from a simulation of the system is shown in Fig. 15. The input is a -3 dBFS sine wave at 25 MHz and the SQNR is computed over a bandwidth of 100 MHz.

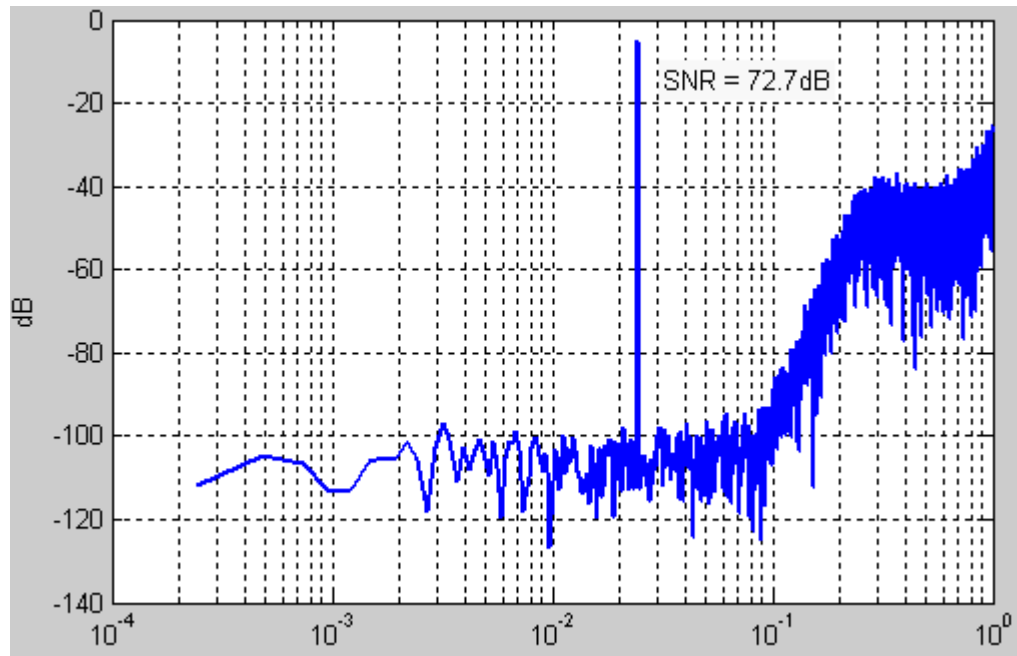


Figure 15: Output spectrum from ideal behavioral model

The closed loop transfer functions from the input to internal nodes of the loop filter were also obtained using Simulink. Fig. 16 shows the loop filter, and signal transfer function from V_{in} to internal nodes are shown in Figs. 17 - 21.

Based on Figs. 17 - 20, the gain of STF to each node is less than unity. However, in Fig. 21, the response shows 4.5 dB magnitude peaking at 212 MHz. In wireless applications, the desired signal may be accompanied by a strong out-of-band interferer. Out-of-band peaking actually translates into a reduction of the dynamic range by limiting the maximum stable amplitude of the modulator.

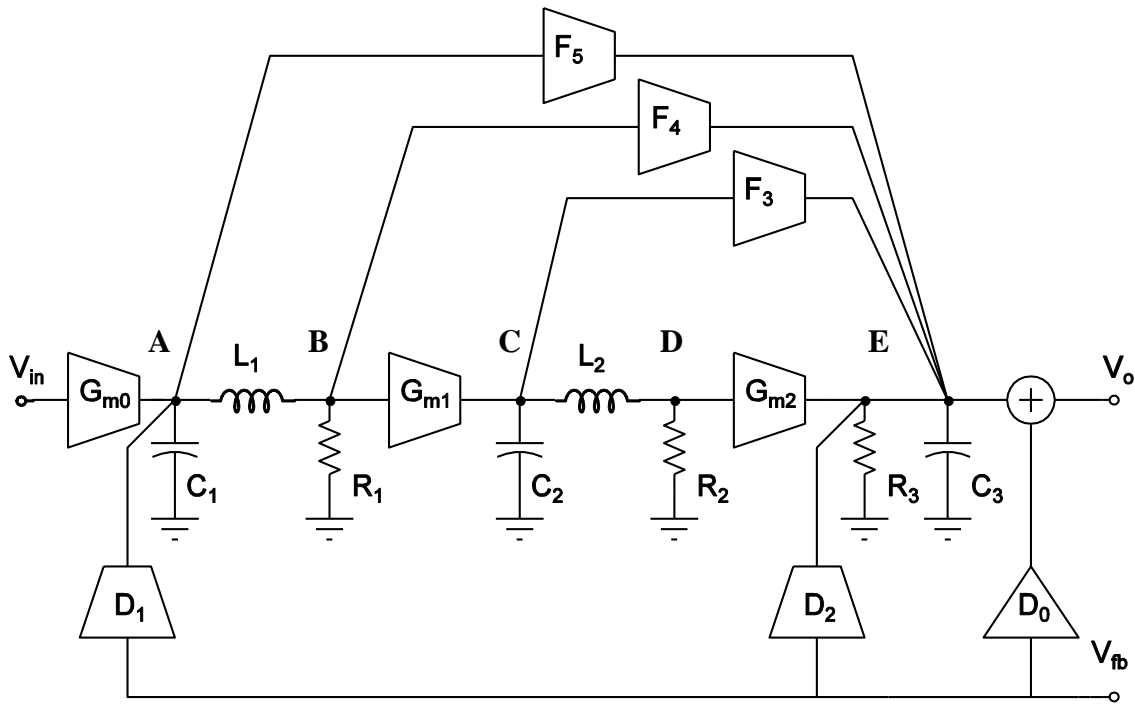


Figure 16: Loop filter

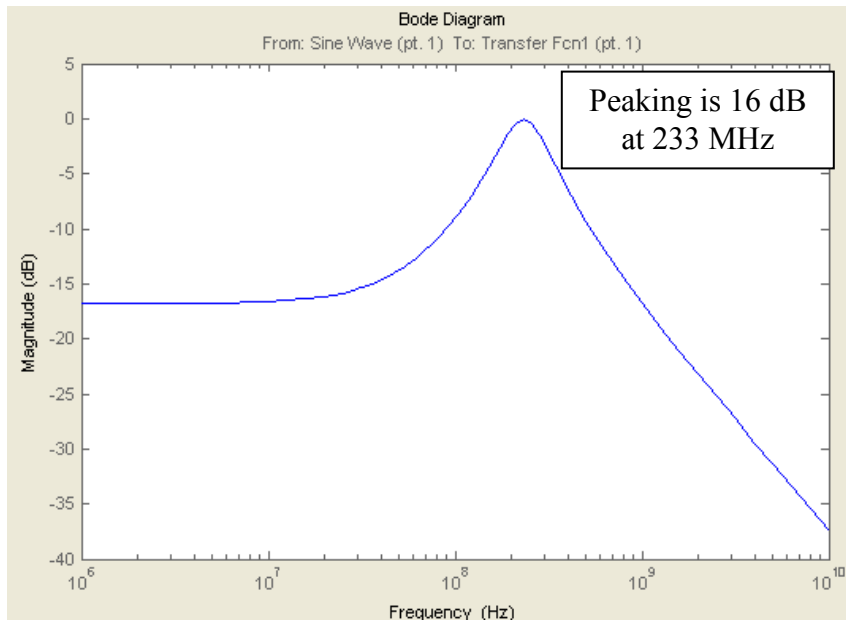


Figure 17: STF from V_{in} to node A

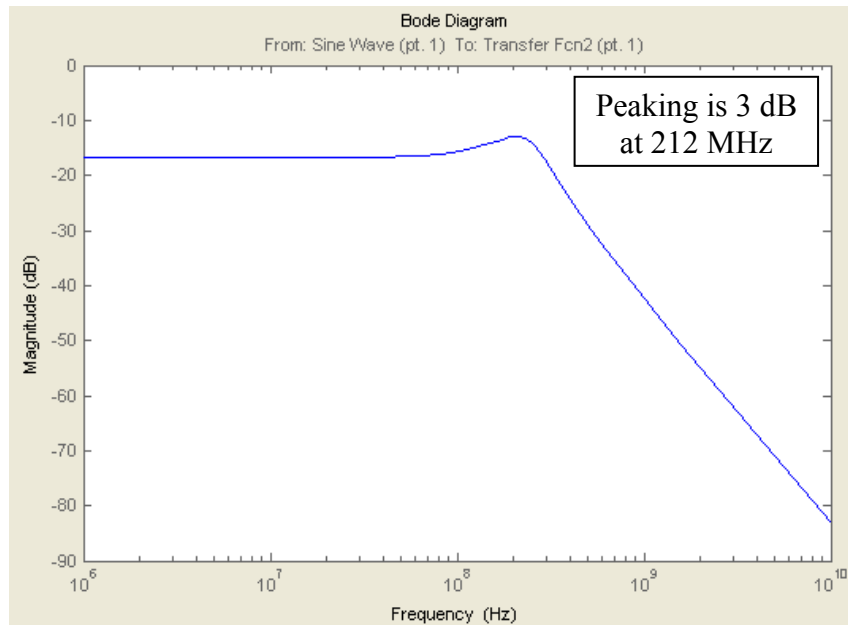


Figure 18: STF from V_{in} to node B

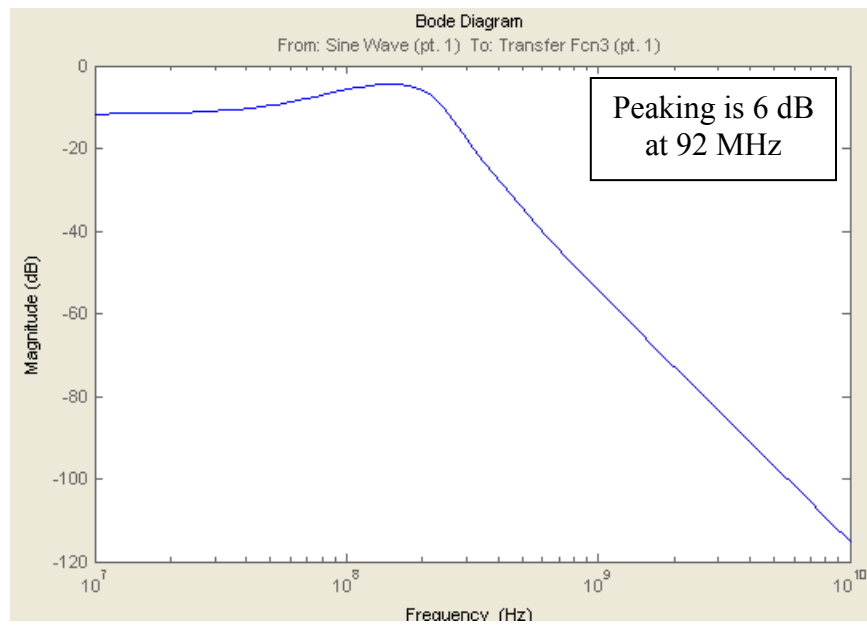


Figure 19: STF from V_{in} to node C

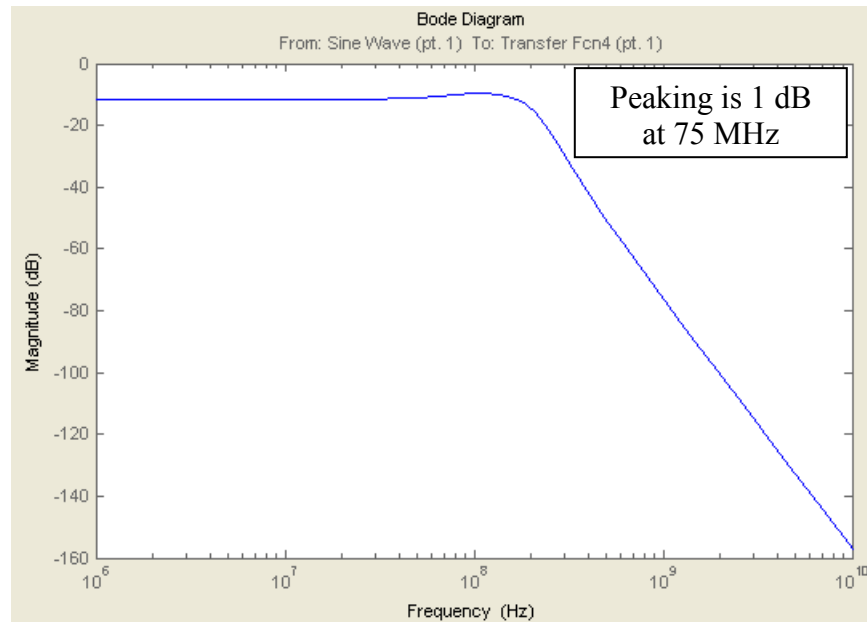


Figure 20: STF from V_{in} to node D

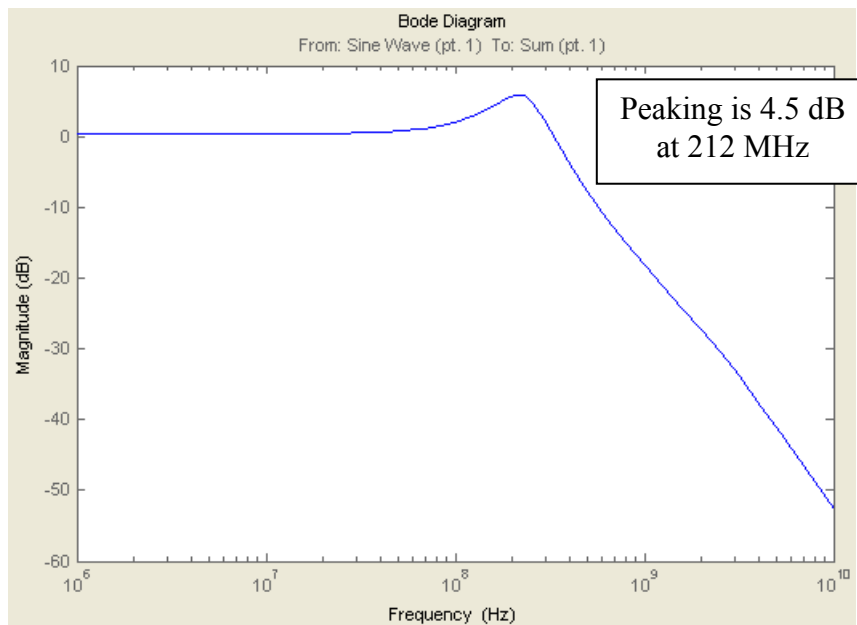


Figure 21: STF from V_{in} to node E

2.4 Non-ideal models of the transconductors

In the previous section, the design process assumed that all components used in the loop are ideal and behaved exactly as assumed in the model, and the simulation for the $\Sigma\Delta$ modulator was performed at the system level using Simulink. However, for real cases, this is not true. Many non-idealities are associated with different components in the loop. Therefore, in this section, the major non-idealities of transconductors in the loop filter will be discussed first, and then the specifications of transconductors in the loop filter will be given by simulations.

The first non-ideality of transconductors is non-linearity. Although the proposed architecture in this work uses passive components in signal paths to obtain the filtering action, which is inherently linear, a sufficient amount of gain is still required in the forward path requiring some active circuits. In this work, transconductors are the components providing gain in signal paths.

For a transconductor, the non-linearity can be expressed as follows:

$$i = c_1 \cdot v + c_3 \cdot v^3 \quad (2.20)$$

where i is the output current of the transconductor, v is the input voltage of the transconductor, c_1 is the linear transconductance coefficient, and c_3 is the third order non-linear transconductance coefficient of the transconductor.

Because of differential operation in this work, only odd-order non-linearities are considered here and even-order terms are neglected. From Fig. 16, the transconductors, G_{m1} , F_4 and F_5 do not have any gain components before them and hence any non-linearity introduced by those transconductors, when reflected back to the input, will appear without any attenuation. This non-linearity will then directly appear at the output due to the feedback action. Therefore, those transconductors require high linearity specification.

Conversely, the signal received by the transconductors, G_{m2} and F_3 in Fig. 16, has already been amplified by transconductor, G_{m1} . Consequently, their non-linearities are not as critical. The non-linear model in MATLAB using equation (2.20) is shown in Fig. 22.

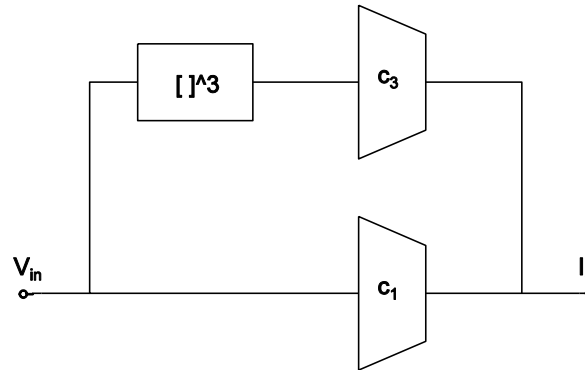


Figure 22: Transconductor MATLAB model

Using the non-linear model for all transconductors, system simulations were performed, and IM3 specifications were derived for each transconductor to obtain an overall system IM3 of 70 dB. The results are shown in Table 4.

Table 4: Transconductor non-linearity specifications

Transconductor (Fig. 16)	Input swing (mV)	IM3 specification (dB)
G_{m1}	30	68
G_{m2}	60	55
F_3	90	55
F_4	30	68
F_5	60	68

The second non-ideality of transconductors is finite bandwidth. In the model of the transconductors considered so far, it is assumed that the transconductors have infinite bandwidth, which means the gain of the transconductors have the same value at all

frequencies. However, the gain of the transconductors starts to reduce at the frequency of the internal pole. In this work, the transconductors are modeled as single-pole systems as:

$$i = \frac{g_m}{1 + \frac{s}{\omega_p}} \cdot v \quad (2.21)$$

where ω_p represents the dominant pole of the transconductor.

Because the sigma-delta modulator is a closed loop system, excess delay due to transconductor blocks can cause the loop to become unstable. The poles within the transconductor block introduce additional delay in the signal path. Therefore, to make sure that the delay introduced is not high, the minimum specifications for the dominant poles of the transconductors were obtained as shown in Table 5.

Table 5: Transconductor dominant pole specifications

Transconductor (Fig. 16)	Dominant pole (GHz)
G_{m1}	1.8
G_{m2}	0.9
F_3	0.9
F_4	1.8
F_5	2.8

3. TRANSISTOR LEVEL DESIGN OF TRANSCONDUCTOR

For high frequency operation, operational transconductance amplifiers (OTA) have proven to be the best candidate for implementation of continuous-time filters compared to active-RC or switched capacitor topologies. This is because integrators based on OTA work in open loop instead of closed loop. The major disadvantage of OTAs is the input stage non-linearity at higher differential input voltages due to the non-linear characteristics of the input stage transistors. This problem causes inter-modulation distortion components at the output and degrades achievable dynamic range. Several techniques have been reported trying to improve the linearity of OTAs [11]. In this section, the design of OTAs used in wideband continuous-time sigma-delta modulator is presented in detail.

3.1 Design considerations

Based on the simulated results from Section 2, the target specifications of OTAs are shown in Table 6. The implementation requires use of minimum power and area in Jazz 0.18 μm technology with supply voltage of 1.8 V.

Table 6: Transconductor specifications

Transconductor (Fig. 16)	Transconductance (mS)	Linearity (dB)	Bandwidth (GHz)
G_{m1}	100	68	1.8
G_{m2}	1.3	55	0.9
F_3	1.7	55	0.9
F_4	6.0	68	1.8
F_5	2.4	68	2.8

Based on Table 6, it is clear that the OTA G_{m1} requires extremely high transconductance and high linearity.

An easy way to improve the linearity of an OTA is using source degeneration topology. For low-distortion operation, large bias currents are required that consume power and increase transistor thermal noise, and large degeneration resistors reduce OTA output swing and increase layout area. The OTA shown in Fig. 23 presented in [11] is chosen in this work. In this topology, the amplifier forces the input voltage across the degeneration resistor, creating a differential current that flows in the primary BJTs (B_1 , B_2) and is replicated at the output by identical BJTs.

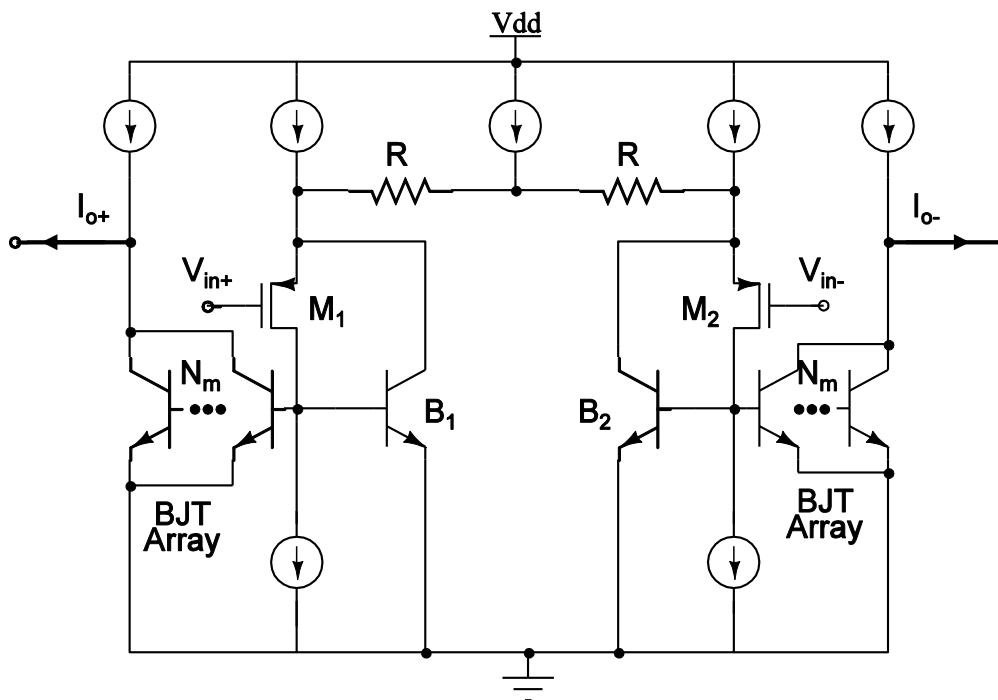


Figure 23: Transconductor topology

3.2 Design procedure

In order to find the relationship between input voltage and output current, a small-signal model of the OTA is created as shown in Fig. 24.

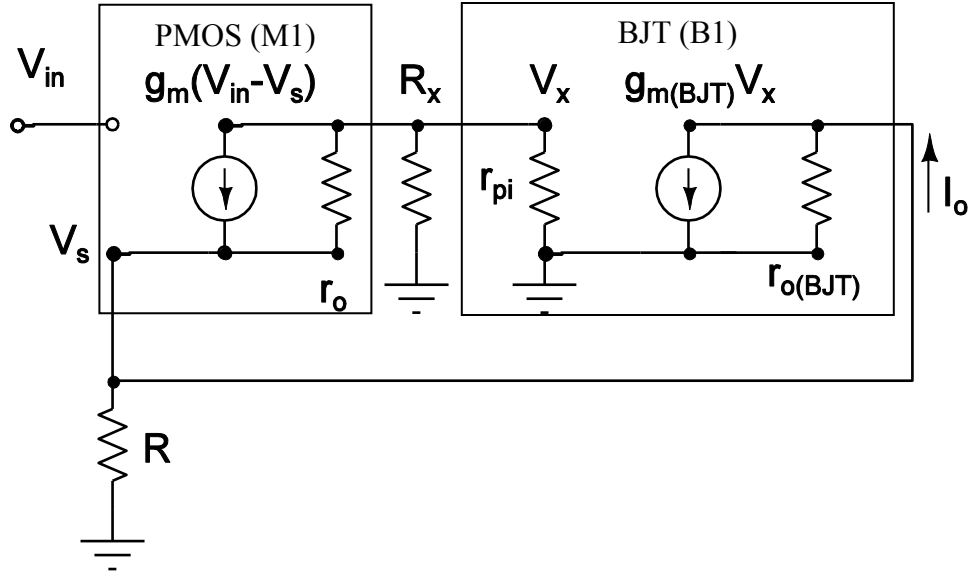


Figure 24: Small-signal model of the OTA

In Figure 24, R_x is the output resistance at the drain node of PMOS transistor (M_1), R is the degeneration resistor, g_m is the transconductance of input PMOS transistor (M_1), and $g_{m(BJT)}$ is the transconductance of BJT (B_1).

Ignoring the channel-length modulation of input PMOS and BJT, the transconductance of the OTA is obtained as:

$$G_m = \frac{-g_m g_{m(BJT)} R_x N_m}{1 + g_m R + g_m g_{m(BJT)} R R_x} \quad (3.1)$$

where N_m is the output mirroring factor.

For $g_m g_{m(BJT)} R R_x \gg g_m R \gg 1$, the transconductance of the OTA can be approximated as:

$$G_m \approx \frac{N_m}{R} \quad (3.2)$$

Based on equation (3.2), in order to achieve high G_m values, the degeneration resistor should be chosen as small as possible. However, when the size of the degeneration resistors reduces, the required collector biasing current of BJTs increases in order to keep the same linearity specification of the OTA. At the mean time, the increased collector biasing current is copied to the output by factor N_m , which significantly increases the total current consumed by the OTA, especially when N_m is large for high G_m case. Therefore, in order to find the optimum degeneration resistor size, which can achieve specifications with minimum power, the relationship between the degeneration resistor sizes and BJT collector biasing current required for the linearity specification needs to be found shown as followed.

Non-linear model of the OTA

Assume that the BJT (B_1) is the main source of non-linearity. Since the base node of the BJT (B_1) is a high impedance node as shown in Fig. 23, the base-emitter voltage increases significantly when the small-signal drain current of PMOS (M_1) increases, which makes most of the small signal current to flow through BJT (B_1). Since the drain current of PMOS (M_1) only has small variation, the assumption that the PMOS (M_1) is linear is reasonable. The third order harmonic source is added into BJT (B_1) in the small-signal model shown in Fig. 25.

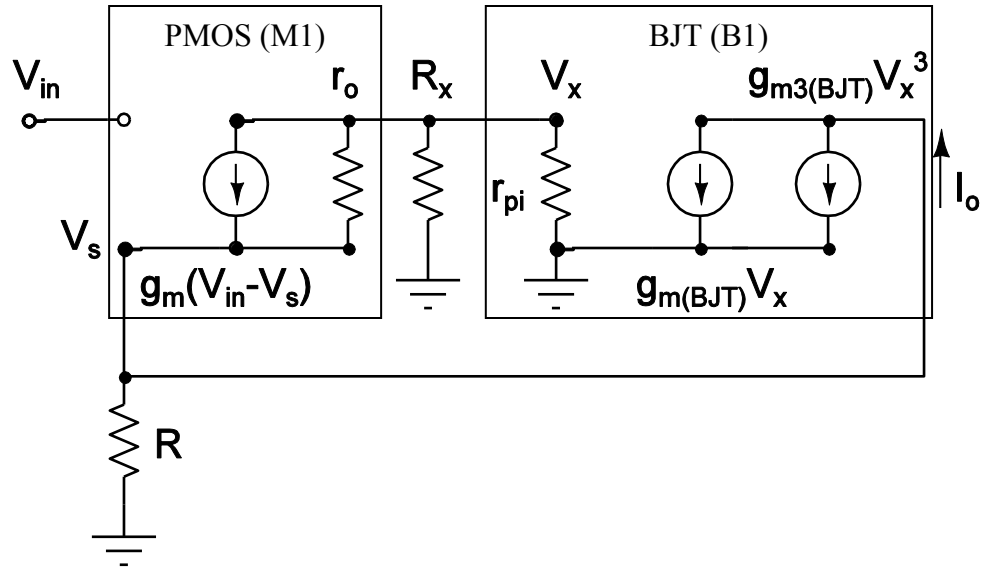


Figure 25: Non-linear model of the OTA

In Fig. 25, $g_{m3(BJT)}$ is the third order harmonic transconductance of BJT (B₁).

Assume the input signal of the OTA is a pure sine wave as:

$$V_{in} = A \sin(\omega t) \quad (3.3)$$

Considering only the third order harmonic distortion, the output current of the OTA can be expressed as:

$$I_o = a \sin(\omega t) + b \sin(3\omega t) \quad (3.4)$$

where a is the fundamental output signal amplitude and b is the third order harmonic tone amplitude.

Based on Fig. 25, the output current of the OTA can be expressed as:

$$I_o = g_{m(BJT)} V_x + g_{m3(BJT)} V_x^3 \quad (3.5)$$

The PMOS (M_1) node (drain and source) equations can be expressed as:

$$-(V_{in} - V_s)g_m R_x = V_x \quad (3.6)$$

$$(V_{in} - V_s)g_m - I_o R = V_s \quad (3.7)$$

From equations (3.6) and (3.7), the expression of V_x can be obtained as:

$$V_x = \frac{-V_{in}g_m R_x - I_o R g_m R_x}{(1 + g_m R)} \quad (3.8)$$

Substituting equation (3.8) into equation (3.5),

$$I_o = g_{m(BJT)} \left[\frac{-V_{in}g_m R_x - I_o R g_m R_x}{(1 + g_m R)} \right] + g_{m3(BJT)} \left[\frac{-V_{in}g_m R_x - I_o R g_m R_x}{(1 + g_m R)} \right]^3 \quad (3.9)$$

Then, substituting equation (3.3) and (3.4) into equation (3.9) gives,

$$I_o = g_{m(BJT)} \left[\frac{(-Ag_m R_x - aRg_m R_x) \sin(\omega t) - bRg_m R_x \sin(3\omega t)}{1 + g_m R} \right] + g_{m3(BJT)} \left[\frac{(-Ag_m R_x - aRg_m R_x) \sin(\omega t) - bRg_m R_x \sin(3\omega t)}{1 + g_m R} \right]^3 \quad (3.10)$$

Combining all coefficients of $\sin(\omega t)$ term from equation (3.10), which should be equal to the coefficient a :

$$a = \frac{-g_m g_{m(BJT)} R_x A - aRg_m g_{m(BJT)} R_x}{1 + g_m R} \quad (3.11)$$

From equation (3.11), find a expression shown as:

$$a = \frac{-g_m g_{m(BJT)} A R_x}{1 + g_m R + Rg_m g_{m(BJT)} R_x} \quad (3.12)$$

Combining all coefficients of $\sin(3\omega t)$ term from equation (3.10), which should be equal to the coefficient b :

$$b = \frac{-bRg_{m(BJT)}g_mR_x}{1+g_mR} - \frac{A^3}{4}g_{m3(BJT)} - \frac{3}{2}\frac{A^2bRg_mR_xg_{m3(BJT)}}{1+g_mR} \quad (3.13)$$

From equation (3.13), find b expression shown as:

$$b = -\frac{A^3}{4} \frac{g_{m3(BJT)}(1+g_mR)}{(1+Rg_mg_{m(BJT)}R_x + \frac{3}{2}A^2Rg_mR_xg_{m3(BJT)})} \quad (3.14)$$

The third order harmonic distortion (HD3) of the OTA can be calculated as:

$$HD3 = 20\log_{10}\left(\frac{b}{a}\right) \quad (3.15)$$

Based on the equations (3.12), (3.14) and (3.15), third order harmonic distortion, HD3, can be plotted as a function of collector current for different sizes of degeneration resistances, which is shown in Fig. 26.

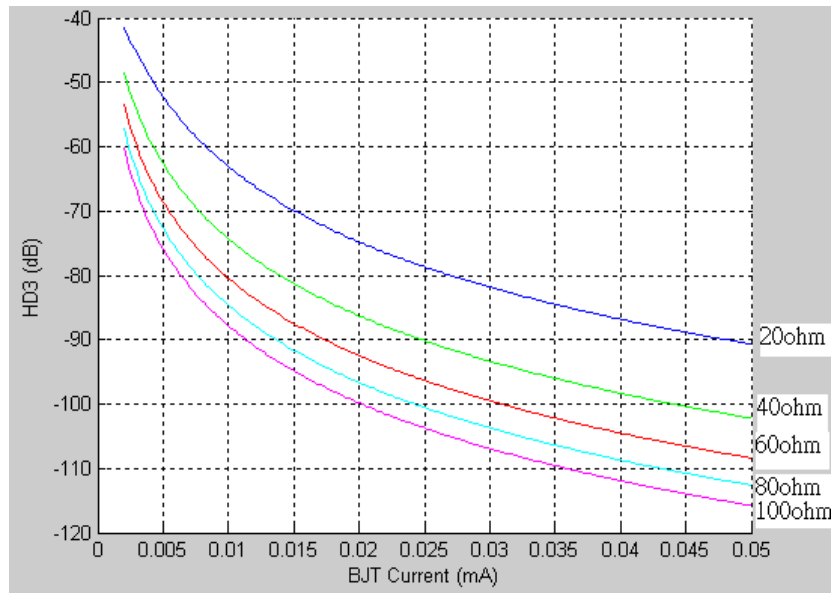


Figure 26: HD3 plot of the OTA

It can be seen from Fig. 26 that, for the same linearity, the required collector current of BJT increases when the degeneration resistor size decreases.

Once the collector current of the BJT is decided, the total current consumed by OTA is approximately equal to $I_c N_m$. The total power consumed by OTA for differential amplifier case is

$$Power = 2I_c(1 + N_m)V_{DD} \quad (3.16)$$

where I_c is the collect current of the BJT (B_1), N_m is the mirroring factor, and V_{DD} is the supply voltage.

In order to optimize the total power consumed by the OTA, the mathematical model can be created by using MATLAB based on equation (3.12), (3.14), (3.15) and (3.16). Then, the relationship between the total power consumption of the OTA and the degeneration resistor size can be obtained by sweeping the degeneration resistor sizes as shown in Fig. 27.

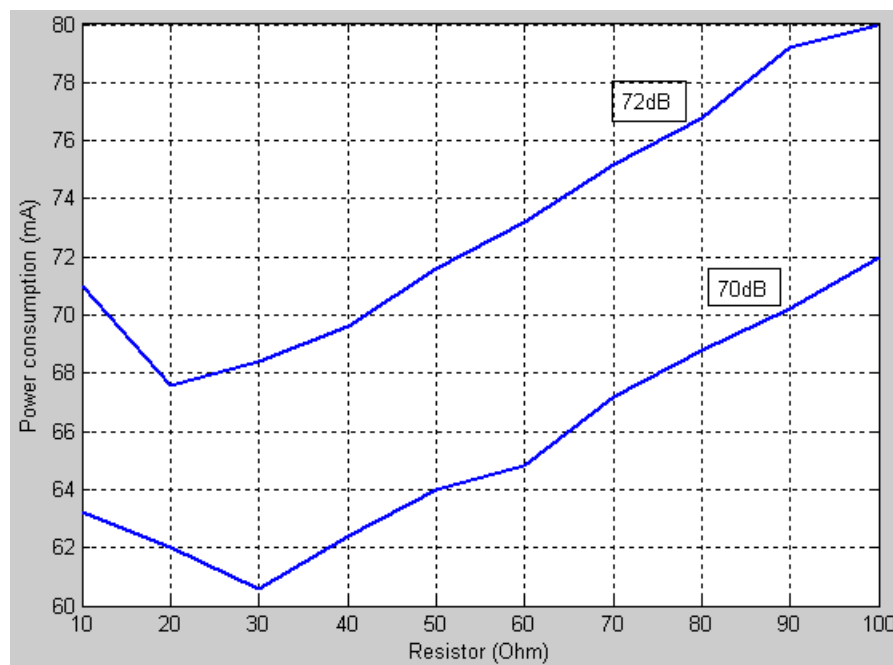


Figure 27: Power consumption of the OTA V.S. degeneration resistor

Based on Fig. 27, the degeneration resistor size is chosen to be 30 ohms for this work based on minimum power required to achieve the linearity specification compared to other degeneration resistor sizes. Since the degeneration resistor size and the collector current of BJT have been determined from power optimization, the next step of the OTA design is to decide transistor sizes. However, transistor sizes affect the OTA speed and noise. For large transistor sizes, parasitic capacitor will increase time-constant. For small BJTs size, the thermal noise of BJTs increase. Therefore, building a mathematical model for the noise and frequency performance of the OTA in terms of the circuit components is essential.

Noise model of the OTA

The noise sources of the OTA comes from the thermal noise of the current sources (M_3) (M_4) (M_5) and (M_6), the shot noise (I_{cn}) of the BJTs (B_1) and (B_2), the thermal noise (V_{bn}) of the BJTs (B_1) and (B_2), and the thermal noise of the degeneration resistors (R). Fig. 28 shows the OTA with dominant noise sources.

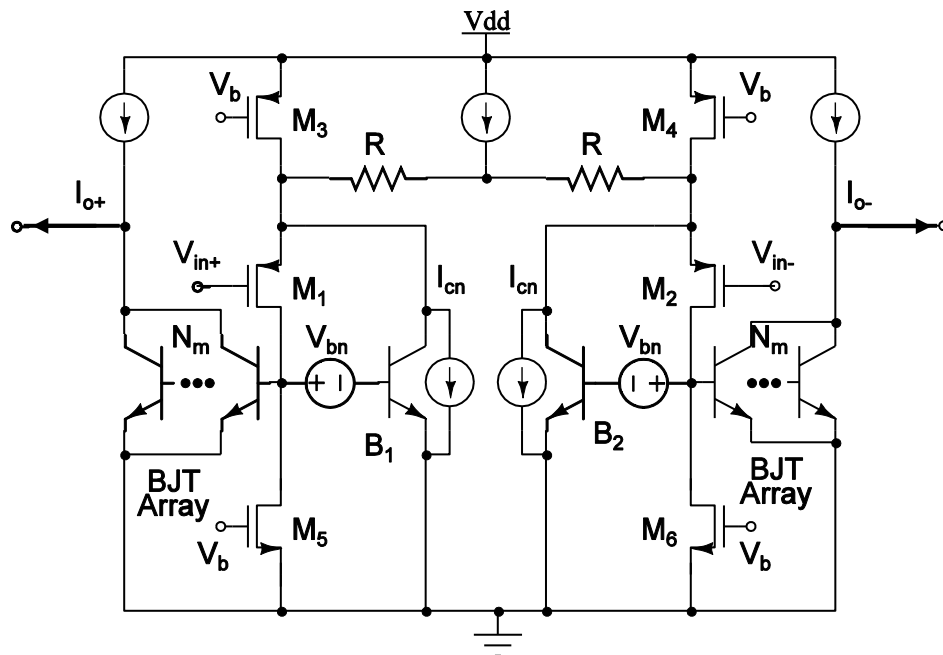


Figure 28: OTA with dominant noise sources

To calculate the total input referred noise of the OTA, assume that the noise sources are uncorrelated. Therefore, the superposition concept is applied when calculating the input referred noise of each component. Comparisons between the mathematical model of the input referred noise of each noise source and the simulated results will be presented later in this section.

(1) Shot noise of the BJT (B1 and B2)

The shot noise of the BJT is proportional to the collector current of BJT. The expression of the shot noise is given by

$$I_{cn} = \sqrt{2qI_c} \quad (3.17)$$

where I_c is the collector current of the BJT and q is the charge of an electron. The shot noise of the BJT presented in the small signal model of the OTA is shown in Fig. 29.

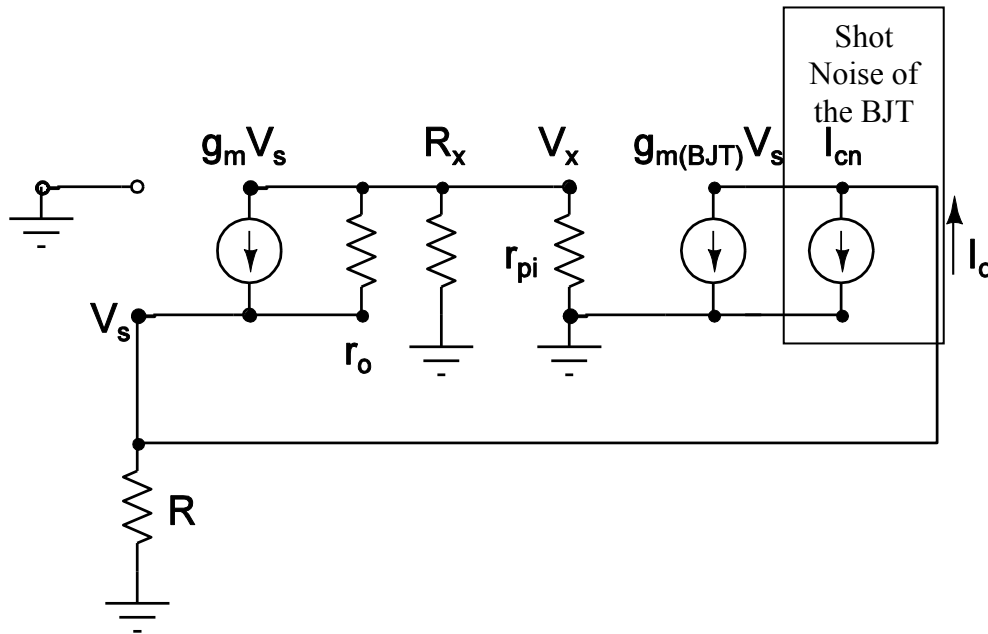


Figure 29: Shot noise of BJT presented in the OTA

Based on Fig. 29, the input referred noise due to shot noise from BJT (B₁) can be obtained as:

$$\overline{V_n} = \frac{\sqrt{2qI_c}(1 + g_m R + g_m g_{m(BJT)} R R_x)}{-g_m g_{m(BJT)} R_x} \quad (3.18)$$

If $g_m g_{m(BJT)} R(R_x // r_\pi) \gg g_m R$ and $g_m R \gg 1$, the equation (3.19) can be simplified as:

$$\overline{V_n} = -\sqrt{2qI_c} R \quad (3.19)$$

Based on equation (3.19), in order to minimize the shot noise from BJT, the collector current and degeneration resistor should be chosen as small as possible. However, the collector current and the degeneration resistor have been fixed when optimizing the power consumption of the OTA.

(2) Thermal noise of the BJT (B1 and B2)

The thermal noise of the BJT is proportional to the internal resistance at the base node of the BJT. The expression of the thermal noise is:

$$V_{bn} = \sqrt{4kTR_b} \quad (3.20)$$

where R_b is the internal resistance at base node of the BJT, T is the absolute temperature, and k is Boltzmann constant.

The thermal noise of the BJT presented in the small signal model of the OTA is shown in Fig. 29.

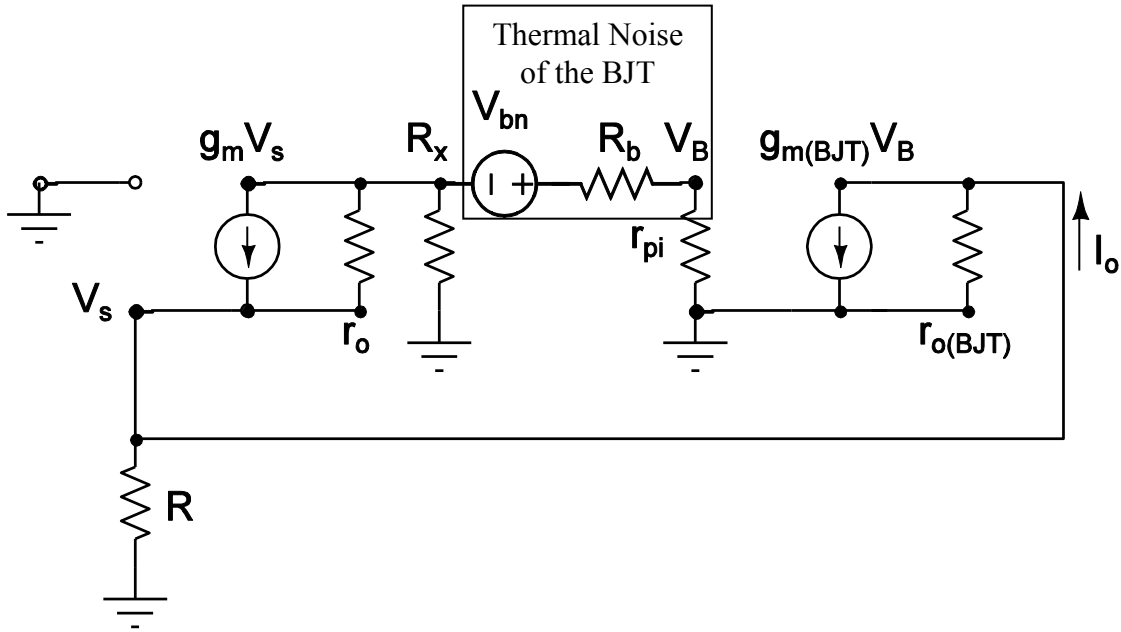


Figure 30: Thermal noise of BJT presented in the OTA

Based on Fig. 30, the input referred noise of the thermal noise from BJT can be obtained as:

$$\overline{V_n} = -\frac{V_{bn}(R_x + g_m R R_x + g_m g_{m(BJT)} R r_i R_x)}{(r_i - R_x + r_i g_m R - g_m R R_x + g_m g_{m(BJT)} R r_i R_x)(g_m g_{m(BJT)} R_x)} \quad (3.21)$$

where $r_i = r_\pi + R_b$. Based on equation (3.22), in order to minimize the thermal noise from BJTs, the internal resistance at its base node should be maximized. However, the BJT sizes are confined by technology. In addition, maximizing the base resistance increases the base capacitance, which decreases the OTA speed, and the OTA speed are given by the specifications obtained in Section 2.

(3) Thermal noise of the transistor (M_1 to M_6)

MOS transistors exhibit thermal noise. For long channel MOS devices operating in saturation, the channel noise is proportional to the transconductance of transistor and can be modeled by current source connected between the drain and source terminal. The expression of the thermal noise of MOS transistor is

$$I_{cn} = \sqrt{4kTg_m\gamma} \quad (3.22)$$

where γ is 2/3 for long channel device.

The input referred noise equations are coded in MATLAB. Comparison between the calculations in MATLAB and the simulated results obtained from CADENCE is shown in Table 7.

(4) Thermal noise of the degeneration resistor (R)

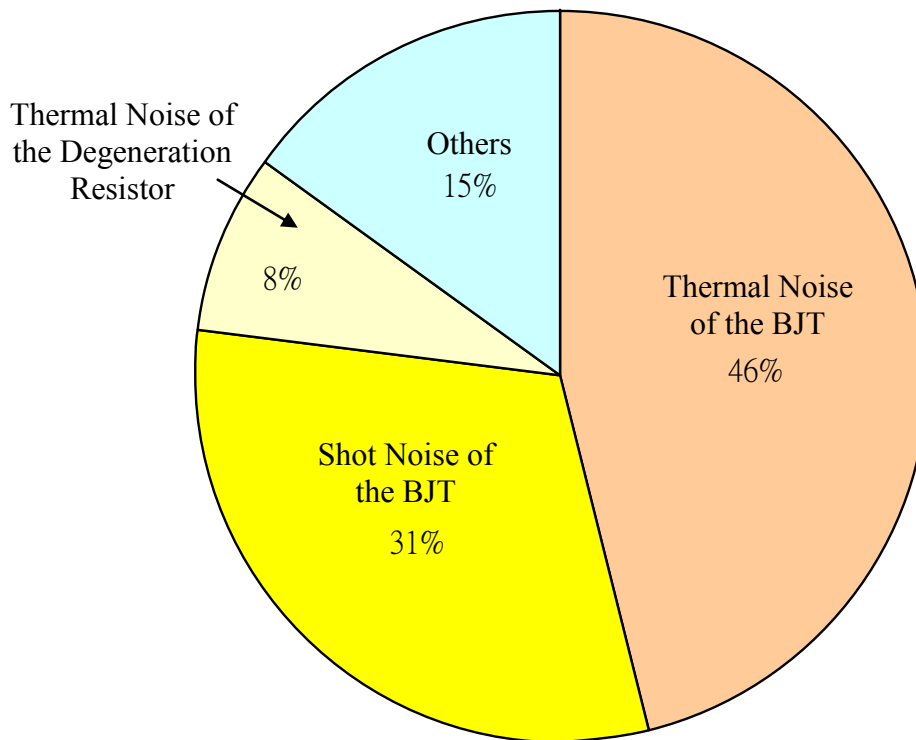
The noise spectrum of a resistor is proportional to the absolute temperature and resistor value as:

$$V_{bn} = \sqrt{4kTR} \quad (3.23)$$

Noise integrated from 1 MHz to 100 MHz are calculated in MATLAB and simulated in CADENCE. The comparison between the two is also shown in Table 7. Fig. 31 shows noise distribution.

Table 7: Comparisons between noise models and CADENCE simulations

Noise Source	Noise models (uV)	Simulations (uV)
Shot noise of the BJT	2.9	3.0
Thermal noise of the BJT	5.2	5.1
Thermal noise of the degeneration resistor	1.7	1.5
Thermal noise of the input PMOS transistor	0.96	0.94

**Figure 31: Noise distribution**

Based on Table 7, for the topology of the OTA, over 50% of the noise comes from the BJTs. The thermal noise of the BJTs traded off with OTA speed, while the shot noise of the BJT traded off with OTA power. Therefore, when choosing the BJT sizes and biasing conditions, these trade-offs should be considered based on the specifications of each OTA.

Frequency Response Model of the OTA

In order to estimate the OTA speed limitation, knowledge of the OTA pole locations is essential. Since the chosen topology for the OTA is based on a closed loop, we can break the loop at the BJT base node, and calculate the pole at each node. The small signal model with parasitic capacitors is shown in Fig. 32.

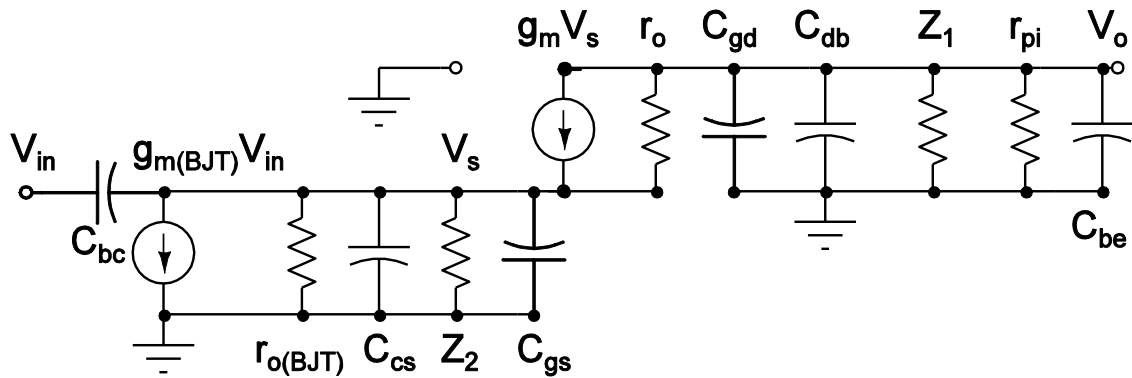


Figure 32: The small signal model for frequency response.

In Fig.32, C_{be} is the total parasitic capacitors from base to emitter terminal of BJT (B_1) and BJT array, C_{bc} is the parasitic capacitor from base to collector terminal of BJT (B_1), C_{cs} is the parasitic capacitor from collector to substrate terminal of BJT (B_1), C_{gs} is the parasitic capacitor from gate to source terminal of PMOS (M_1), C_{gd} is the parasitic capacitor from gate to drain terminal of PMOS (M_1), C_{db} is the parasitic capacitor from drain to bulk terminal of PMOS (M_1), Z_1 is the resistance at the drain node of PMOS (M_1), and Z_2 is the resistance at the source node of PMOS (M_1). The values of the

parasitic capacitors are extracted from CADENCE. After the small signal model is created, the pole locations are obtained. The dominant pole is located at the base node of the BJT and the first non-dominant pole is located at source node of the input PMOS. Thus, in order to increase the OTA speed, the size of the BJTs and NMOS current mirrors are chosen as small as possible. However, for smaller BJT sizes, the thermal noise of BJT increases because the internal resistance increases at the same time. Therefore, there is a trade off between OTA speed and noise for choosing BJT sizes.

CMFB (common mode feedback)

In high gain fully differential amplifiers, the output common mode level is quite sensitive to mismatches and it cannot be stabilized by means of differential feedback. Thus, a common-mode feedback network must be added to sense the common mode level of the two outputs and accordingly adjust one of the bias currents in the amplifier. The tasks of the CMFB network is first sensing the output common mode level, comparison with a reference, and returning the error to the amplifier's bias network. The CMFB used in this work is shown in Fig. 33.

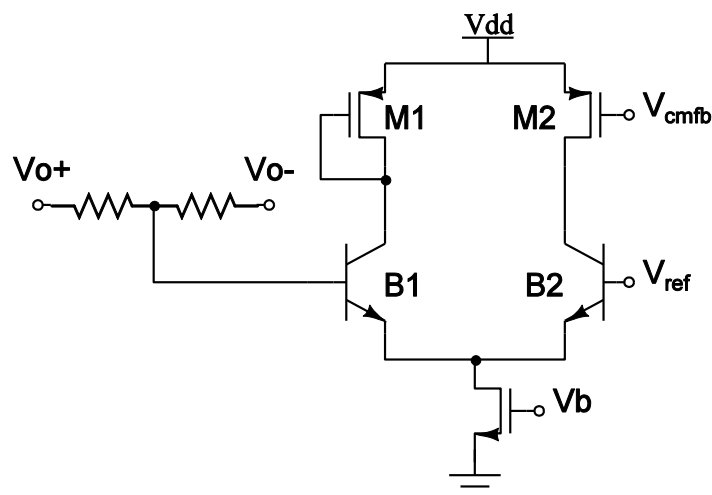


Figure 33: CMFB circuit

3.3 Results

Based on power, noise and speed specifications, each OTA component sizes are determined. The performance summaries of each OTA are shown in Tables 8 - 10. Fig. 34 shows the two tone test of OTA G_{m1} .

Table 8: Performance summary of the OTAs G_{m1} and G_{m2}

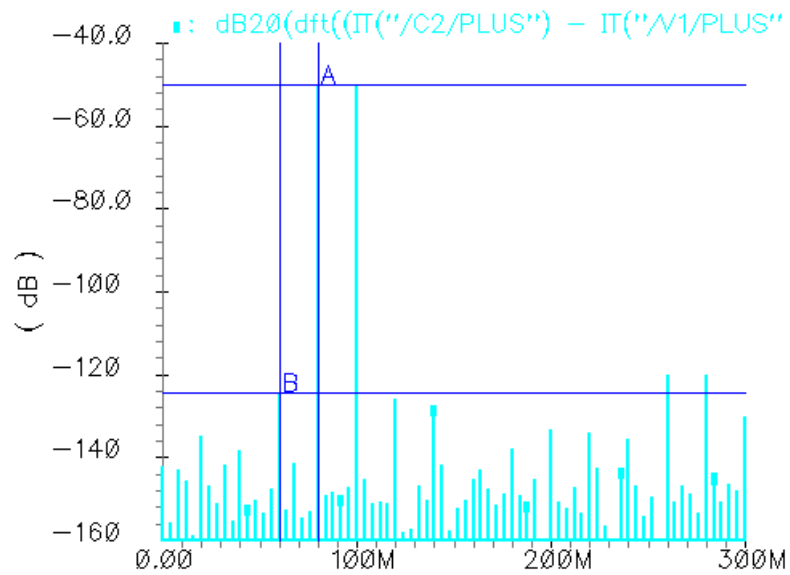
OTA	G_{m1}	G_{m2}
Transconductance	101.7 mS	1.3 mS
IM_3	70.9 dB	58.1 dB
Power consumption	34.2 mW	14.1 mW
Input referred noise Integration bandwidth	5.2 uV (1MHz~100MHz)	18 uV (1MHz~100MHz)

Table 9: Performance summary of the OTAs F_3 and F_4

OTA	F_3	F_4
Transconductance	1.7 mS	6.0 mS
IM_3	56.5 dB	70.2 dB
Power consumption	14.6 mW	16.4 mW
Input referred noise Integration bandwidth	18 uV (1MHz~100MHz)	5.2 uV (1MHz~100MHz)

Table 10: Performance summary of the OTA F₅

OTA parameters	F ₅
Transconductance	2.4 mS
IM ₃	70.1 dB
Power consumption	25.4 mW
Input referred noise	15 uV
Integration bandwidth	(1MHz~100MHz)

**Figure 34: Two tone test of OTA-Gm1 (71 dB)**

4. SIMULATION RESULTS

This section mainly shows the measurements from the CADENCE simulations for both the loop filter in transistor level and the system with the loop filter in transistor level.

4.1 Filter simulation results

After all OTAs implemented in transistor level, the filter can be built following the loop filter design in Section 2. The schematic of the loop filter is shown in Fig. 35 and the magnitude and phase response of the loop filter is shown in Fig. 36 and Fig. 37. The performance summary of the loop filter is shown in Table 11.

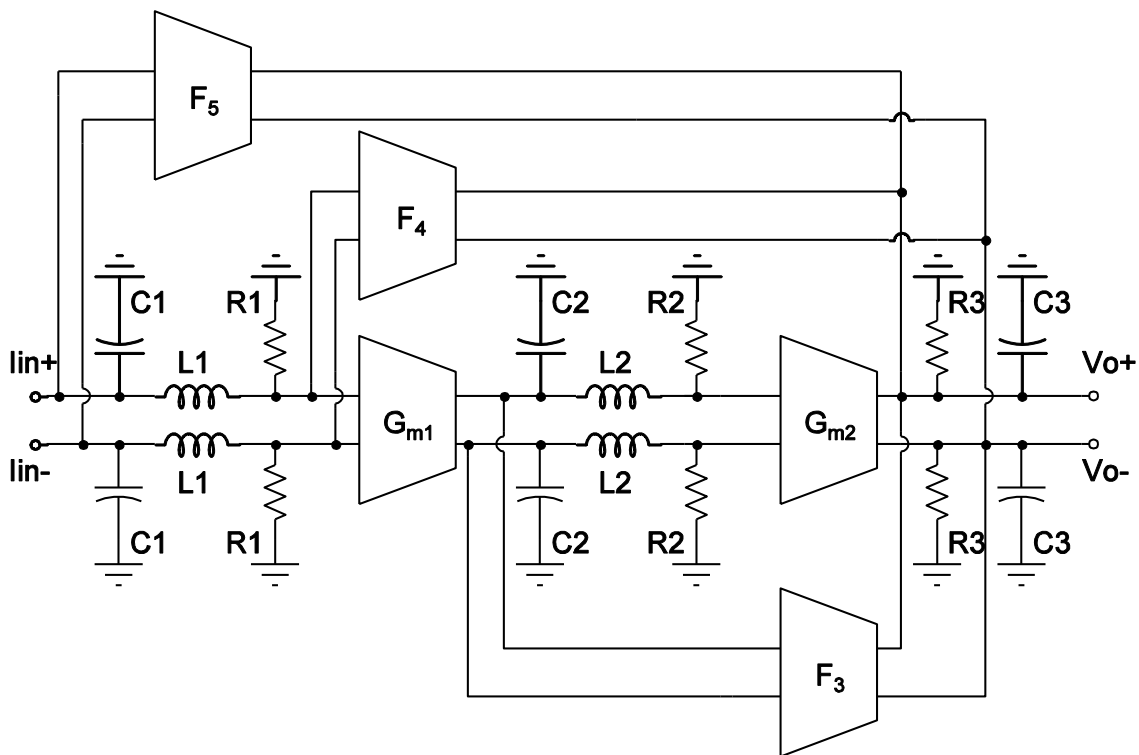


Figure 35: Loop filter schematic

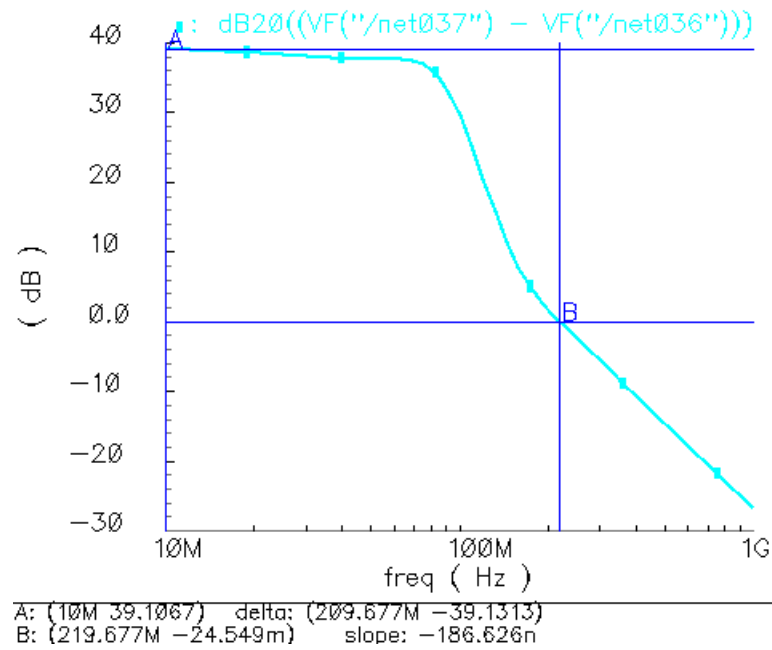


Figure 36: The loop filter magnitude response

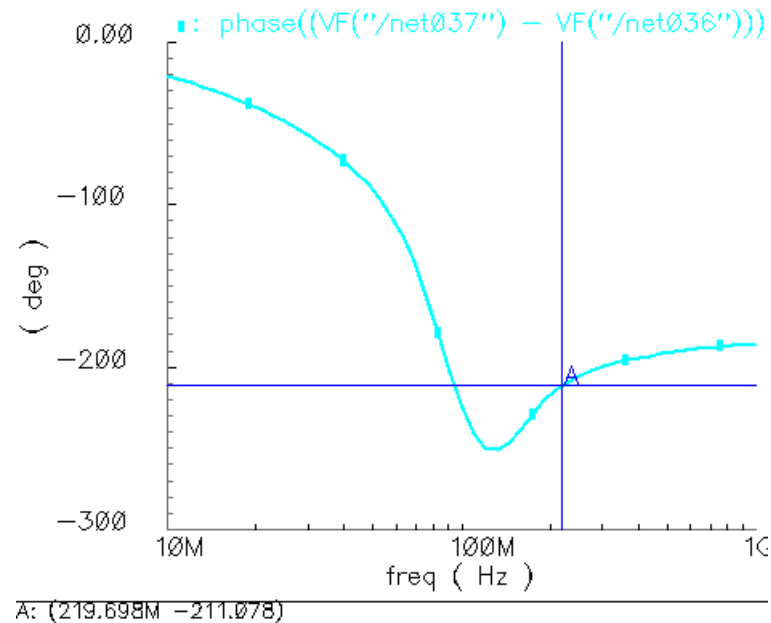


Figure 37: The loop filter phase response

Table 11: Performance summary of the Filter

Filter Parameters	Values
Order	5
DC gain	40 dB
Bandwidth	100 MHz
Power consumption	105 mW
Power supply	1.8 V
Technology	Jazz 0.18 um

4.2 System simulation results

Fig. 38 shows system simulation with the loop filter in transistor level. The simulated data in CADENCE are extracted, and then calculated in MATLAB shown in Fig. 39.

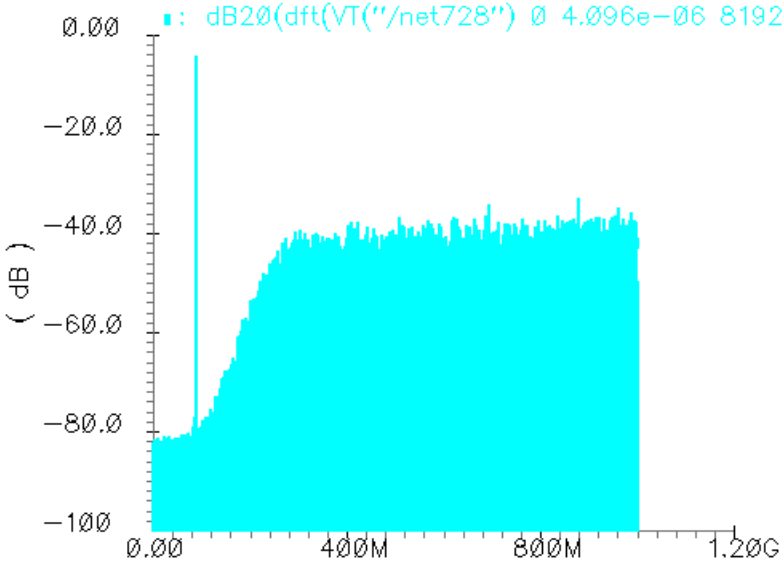


Figure 38: System simulation with filter in transistor level

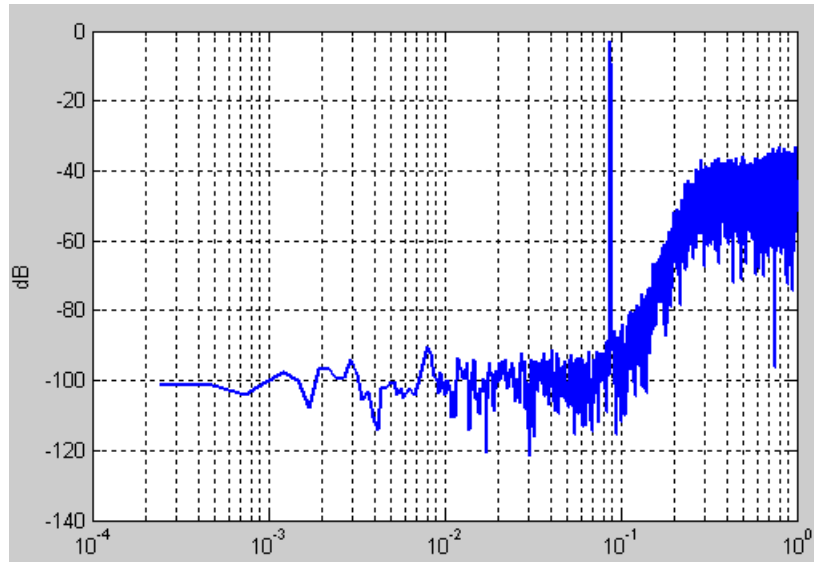


Figure 39: SNR calculation in MATLAB (SNR= 68 dB)

4.3 Comparisons

The comparison between feedback and feed-forward topologies is shown in Table 12. Based on Table 12, the feed-forward topology has the advantage of lower power consumption. However, feed-forward topology also suffers from low blocker rejection. In addition, another drawback of feed-forward topology is out-of-band peaking discussed in Section 2. Table 13 shows the comparisons between this work and other wide bandwidth $\Sigma\Delta$ ADCs in specifications, power consumption and figure of merit (FOM).

Table 12: Comparison between feedback and feed-forward topologies

Filter topology	Feed-forward	Feedback [9]
Power consumption (filter only)	105 mW	152 mW
Blocker rejection (attenuation)	-4 dB @ 350 MHz -8 dB @ 450 MHz	-26 dB @ 350 MHz -37 dB @ 450 MHz

Table 13: Brief summary of wide bandwidth $\Sigma\Delta$ ADC

Year	Technology	Sampling Frequency	Bandwidth	SNDR (dB)	Power (mW)	FOM pJ/conv
1998 [12]	InGaAs HEMT	5 GHz	100 MHz	39	400	31.2
2001 [13]	InGaAs HBT	18 GHz	500 MHz	42	1500	11.7
2003 [14]	InP HBT	8 GHz	250 MHz	40	1800	56.2
2006 [15]	SiGe HBT	20 GHz	313 MHz	-	490	
2009 [3]	SiGe HBT	40 GHz	1 GHz	37	350	2.9
2011 [4]	45 nm CMOS	4 GHz	125 MHz	70	256	0.5
This Work	BiCMOS	2 GHz	100 MHz	67.6	300 (estimated)	0.7

5. CONCLUSIONS

In this thesis, a 100 MHz bandwidth 11-bit resolution $\Sigma\Delta$ ADC employing LC filter sections in a feed-forward topology was presented. The system was designed in MATLAB using the $\Sigma\Delta$ toolbox considering the various design variables and the trade-offs among them. The specifications of the individual building blocks were obtained taking into account the non-idealities. A high transconductance (100 mS) and high linearity (70 dB) OTA was designed for use in the loop filter with 34.2 mW power consumption in transistor level. The 5th order loop filter was implemented consuming less power (105 mW) compared to the loop filter implemented in the feedback topology (152 mW). The proposed topology shows 4 dB attenuation at 350 MHz and 8 dB attenuation at 450 MHz.

5.1 Future work

A couple of approaches to improve on the work presented in this thesis are noted below.

The out-of-band peaking inherent in feed-forward topology reduces the dynamic range of the ADC. Methods to reduce the peaking in the ADC need to be investigated.

The resolution of the ADC is limited primarily by the jitter of the clock signal in the feedback path. Approaches to mitigate the effect of jitter in the modulator need to be explored.

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VITA

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