

MULTI-LOOP-RING-OSCILLATOR DESIGN AND ANALYSIS  
FOR SUB-MICRON CMOS

A Dissertation

by

ERIK PANKRATZ

Submitted to the Office of Graduate Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2011

Major Subject: Electrical Engineering

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## ABSTRACT

Multi-Loop-Ring-Oscillator Design and Analysis  
for Sub-Micron CMOS. (December 2011 )

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Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Ring oscillators provide a central role in timing circuits for today's mobile devices and desktop computers. Increased integration in these devices exacerbates switching noise on the supply, necessitating improved supply resilience. Furthermore, reduced voltage headroom in submicron technologies limits the number of stacked transistors available in a delay cell. Hence, conventional single-loop oscillators offer relatively few design options to achieve desired specifications, such as supply rejection. Existing state-of-the-art supply-rejection-enhancement methods include actively regulating the supply with an LDO, employing a fully differential or current-starved delay cell, using a hi-Z voltage-to-current converter, or compensating/calibrating the delay cell. Multiloop ring oscillators (MROs) offer an additional solution because by employing a more complex ring-connection structure and associated delay cell, the designer obtains an additional degree of freedom to meet the desired specifications.

Designing these more complex multiloop structures to start reliably and achieve the desired performance requires a systematic analysis procedure, which we attack on two fronts: (1) a generalized delay-cell viewpoint of the MRO structure to assist in both analysis and circuit layout, and (2) a survey of phase-noise analysis to provide a bank of methods to analyze MRO phase noise. We distill the salient phase-noise-analysis concepts/key equations previously developed to facilitate MRO and other non-conventional oscillator analysis. Furthermore, our proposed analysis framework demonstrates that all these meth-

ods boil down to obtaining three things: (1) noise modulation function (NMF), (2) noise transfer function (NTF), and (3) current-controlled-oscillator gain ( $K_{\text{ICO}}$ ).

As a case study, we detail the design, analysis, and measurement of a proposed multiloop ring oscillator structure that provides improved power-supply isolation (more than 20dB increase in supply rejection over a conventional-oscillator control case fabricated on the same test chip). Applying our general multi-loop-oscillator framework to this proposed MRO circuit leads both to design-oriented expressions for the oscillation frequency and supply rejection as well as to an efficient layout technique facilitating cross-coupling for improved quadrature accuracy and systematic, substantially simplified layout effort.

## DEDICATION

To God and to my family.

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Firstly, I am grateful to my advisor Dr. Sánchez-Sinencio for his guidance and counsel during my time in graduate school. I feel I have grown both technically and professionally through my experiences working with Dr. Sánchez at AMSC, and I have been fortunate to learn in such an environment inculcated by an advisor who respects and guides his students.

I am also privileged to have met and worked with a group of colleagues whose technical skill as well as character are extraordinary. Thus, I would like to extend my gratitude to my friends and colleagues Hesam, Raghavendra, Joselyn, Félix, Chinmaya, Heng, Mohammed, Didem, Mohamed, Ed, Ramy, Jusung, Praveen, and countless other friends, whose continual help and support—both technical and otherwise—have enabled me to complete this work.

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## 1. INTRODUCTION

### 1.1 Motivation

Ring oscillators act as voltage-controlled oscillators (VCOs) for numerous microprocessor applications. Their small size and compatibility with digital processes makes them ideally suited to provide clocks for microprocessors, and they can provide multi-phase outputs for applications such as clock/data-recovery (CDR) circuits [1,2] and fractional-N frequency synthesizers [3–5]. Multi-loop ring oscillators (MROs) in particular can provide precise phase relationships [4–10] and can offer increased oscillation frequency over single-loop equivalents [3, 11–19]. However, ring oscillators' lack of a resonant LC circuit means that their frequency depends primarily on semiconductor parameters and biasing. In this fashion, internal device noise on supply-voltage and bias lines corrupts the frequency of oscillation, leading to phase noise. Phase noise and jitter describe an oscillator's spectral purity and timing accuracy. These qualities determine local-oscillator leakage in transceivers, determine the signal-to-noise ratio (SNR) of angle-modulation systems, and limit the synchronization of clocked devices. The strongly nonlinear action of oscillator circuits and large-signal-amplitude swing cause noise behavior to deviate significantly from conventional small-signal analysis about an assumed constant operating point. Moreover, noise on the supply line such as that from high-speed logic switching often dominates ring oscillators' internal device noise, especially in digitally intensive systems [20–23], thus requiring improved oscillator supply rejection.

The most prevalent class of ring oscillator is a single loop of inverting delay stages, each of which can be either a single-ended CMOS inverter (possibly current starved) or a fully differential source-coupled pair. Older technologies' plentiful voltage headroom (sometimes in excess of 5V) allowed the designer sufficient degrees of freedom to meet target specifications such as static supply sensitivity and frequency tuning range. Single-

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This dissertation follows the style of *IEEE Journal Solid-State Circuits*.

loop ring oscillators' (SROs') simple structures mean that once the SRO delay cell and number of stages is chosen, the overall oscillator performance is essentially fixed. On the other hand, this topological simplicity greatly facilitates determining the oscillation frequency  $f_{osc}$  and in many cases, the phase noise [24]. To prevent oxide breakdown of nanometer-scale devices, newer technologies restrict the amount of available voltage headroom. This headroom reduction limits the number of vertically stacked devices that can be biased in a useful region of operation, thus restricting designers' SRO delay-cell choices essentially to simple CMOS inverters.

We can regain the design degrees of freedom by employing MROs, which can improve the speed of oscillation by connecting ordinary SRO delay cells in more elaborate configurations [11], or as we shall see in this investigation, can allow for new delay cells to oscillate that would not otherwise do in a simple single-loop structure. Enabling these wider ranges of available unit delay cells can provide performance benefits, such as increased supply rejection by allowing a ring of source-follower cells to oscillate.

However, with the benefits of these multiloop structures come the added challenges of increased analysis and, ostensibly, physical circuit layout complexity, which complicate the task of making reliable, manufacturable designs. While the analyses of SROs [24] and certain classes of MROs [25] with basic CMOS delay cells have been presented, it heretofore remains an open problem to have a systematic design/analysis procedure to determine  $f_{osc}$  and phase noise of more advanced MROs. The phase noise in particular can be difficult to analyze for ring/relaxation oscillators because the large-signal, hard-switching behavior creates noise-modulation (etc.) effects not at all modeled by conventional small-signal ("AC") noise analysis. While straightforward cookbook formulas/design procedures exist for SRO phase-noise analysis [24], much of the phase-noise theory applicable to oscillators with more complex structures is geared toward CAD and numerical simulation [26], yielding few design formulas. Thus, MROs do not fit into these typical formulas, and moreover, MROs employing atypical delay cells are not at all addressed by the present ana-

lytical theory. We therefore additionally propose to organize previous phase-noise analysis techniques to provide a unified approach rooted in first principles that will allow both intuitive and hand-calculation of phase noise of MRO structures that do not lend themselves to typical formulas.

This dissertation hence contributes two key items:

1. Design and systematic analysis of multi-loop CMOS ring oscillators, and development of a method for improved supply rejection.
2. Catalogue of extant phase-noise-analysis theories and a proposed, unified, first-principles analysis approach applicable to oscillators in general and in particular to MROs, which do not fit the mold of most cookie-cutter analytic phase-noise formulas.

The proposed low-voltage-delay-cell MRO intrinsically rejects the supply even without calibration or additional voltage regulation. To mitigate supply dependence, we employ a source-follower structure, which isolates the supply with its saturation output resistance. The source follower is naturally insensitive to voltage fluctuations at its drain. This intrinsic resilience to supply voltage gives designers the flexibility either to use the oscillator by itself without regulation or calibration, or, in applications where extremely low sensitivity is required, designers could combine the proposed oscillator with calibration and regulation for even greater supply rejection. However, source followers conventionally are not gain stages, so when connected in a ring, they will not provide enough gain for reliable oscillation. Therefore, we employ a multi-loop structure to provide an additional gain path and permit oscillation. We show that by exploiting these properties of multi-loop structures, we can create a quadrature oscillator from a source-follower stage, allowing superior supply-noise rejection; supply sensitivity is more than 20 dB lower than that of conventional CMOS-inverter-based delay cells. Moreover, by viewing the multi-loop oscillator as an architecture of  $N_{stage}$  generalized “delay cells,” each of which has  $M > 2$  ports,

we obtain both a systematic analysis framework as well as an efficient, straightforward scheme to lay out multiloop interconnection of ostensibly complicated interstage loops. In addition to minimizing layout complexity, this proposed layout technique also facilitates common-centroid cross-coupled layout, which improves matching among the differential I/Q paths.

In addition, with the results of the unified phase-noise analysis approach and compilation of techniques, the designer can learn what error is incurred by common phase-noise-analysis assumptions and what behavior each successively complex analysis method reveals. Knowing both simpler, hand-calculation-oriented techniques as well as the calculation procedure for more accurate CAD-oriented techniques (i) gives the designer intuition into how large-signal operation modulates device noise into phase noise, (ii) provides knowledge of simulator operation, enabling more effective use of the tool, and (iii) allows sound simplification of the circuit to include the exact noise-contribution effect desired to facilitate simple design-oriented analysis.

## 1.2 Organization

This dissertation is organized in the following manner. We begin in Section 2 with a discussion of oscillator fundamentals including steady-state, startup, and oscillator spectral purity/phase noise. Section 3 then goes on to present a classification of oscillators into resonant, ring, and relaxation oscillators along with a survey of the extant oscillator ring topologies to illustrate their common patterns. The section also includes design tradeoffs and common oscillator specifications. We furthermore examine the critical special case of supply-noise-induced jitter/phase noise as well as common techniques used in the past to avoid it or mitigate its effects. As discussed previously, supply noise plays a crucial role in state-of-the-art integrated systems because the large amount of digital circuitry integrated along with the clock-generation circuitry generates switching noise that can easily corrupt

the system clock if not properly designed. Moreover, resonant supply noise can also prove to be an issue.

Based on the previous discussion and survey of MRO and supply-rejection techniques, Section 4 proposes an MRO architecture that achieves improved supply rejection by creating an unconventional source-follower delay cell. Embedding this delay cell in a multi-loop structure enables oscillation and quadrature generation. We next present frameworks to facilitate design and analysis of this nonconventional delay cell in Section 5. Both a conceptual symmetry-based generalized delay-cell viewpoint as well as a unified phase-noise-analysis flow are presented to facilitate design and analysis of the proposed oscillator.

To elaborate on the unified phase-noise flow, Section 6 includes synopses of six categories of phase-noise analysis techniques and explains when each is applicable/most suitable to certain classes of oscillators. The techniques are discussed in terms of our proposed general framework and illustrated with an LC differential cross-coupled oscillator as well as a single-loop ring oscillator in order to demonstrate the salient points of each method with simple numerical/algebraic examples.

Section 7 then applies the theory developed over the previous sections to our proposed source-follower-delay-cell-based quadrature MRO. We employ both the generalized delay-cell and phase-noise analysis approaches discussed previously to demonstrate how the proposed oscillator achieves improved supply rejection as well as to obtain oscillation frequency and startup design-oriented equations. We also present the transistor-level design/layout of the proposed oscillator as well as its experimental results.

Finally, Section 8 summarizes and concludes the thesis.

## 2. OSCILLATOR FUNDAMENTALS

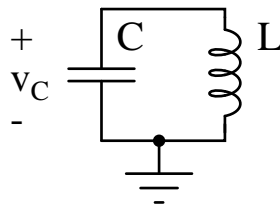
An oscillator ideally provides a periodic output with well-defined amplitude and frequency of oscillation without any input signal present:

$$V_{ideal}(t) = V_{osc} \cos(2\pi f_{osc}t + \phi_0) \quad (2.1)$$

where  $V_{osc}$  denotes the peak fundamental amplitude,  $f_{osc}$  denotes the [fundamental] frequency of oscillation, and the steady-state (constant) phase  $\phi_0$  is determined by the oscillator startup conditions. In many respects, the frequency and amplitude are the two most important aspects of an electronic oscillator.

### 2.1 Linear or Nonlinear?

Linear circuits obey the superposition principle, so without any input, a linear circuit must have zero output. Even allowing initial conditions, the “linear LC oscillator” (e.g. in Fig. 2.1,  $C \frac{d^2 v_C}{dt^2} + \frac{v_C}{L} = 0$ ) can oscillate at different amplitudes, but in practice, oscillators have just one amplitude. Oscillations typically start as exponentially growing

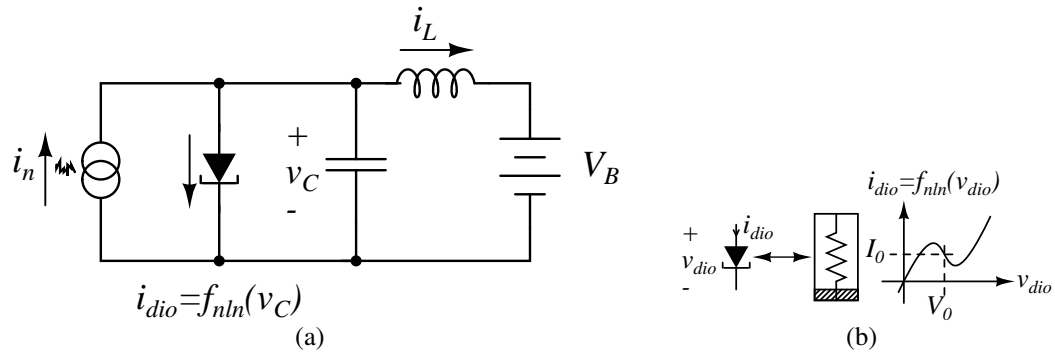


**Figure 2.1.:** “Linear” Oscillator: Initial Conditions Determine Amplitude of Oscillation (Not Physically Realistic)

sinusoids, but device nonlinearity (e.g. FET leaving saturation) eventually limits the exponential growth (see below for mathematical treatment). Nonlinearity allows for a unique oscillation amplitude. By *nonlinear* we mean that the *voltages, currents, and charges* are

nonlinearly related, e.g. as a reverse-biased silicon diode has  $I_{dio}(V) = I_S(e^{V/\phi_t} - 1)$  and  $Q(V) = Q_0\sqrt{1 - \frac{V}{V_0}}$  [27]. The ability of a nonlinear circuit to discriminate between different-amplitude signals allows it to correct amplitude error in the steady-state oscillation waveform.

The simplest electrical-oscillator model properly capturing physical startup and steady-state behavior is an LC oscillator with cubic nonlinearity (“van der Pol’s oscillator” [28]) such as that shown in Fig. 2.2. The (nonlinear) differential equation describing the oscil-



**Figure 2.2.:** Van der Pol Nonlinear Oscillator Model: (a) Schematic, (b) Negative Nonlinear Resistor I-V Characteristic

lator is

$$C \frac{d}{dt} v_C + \frac{1}{L} \int v_C dt + f_{nln}(v_C) = i_n(t) = q_0 \delta(t) \quad (2.2)$$

where  $f_{nln}(v_C) \equiv I_0 - g_1(v_C - V_0) + g_3(v_C - V_0)^3$  as illustrated in Fig. 2.2(b). We assume  $V_B = V_0$  for simplicity, and the “noise” current  $q_0 \delta(t)$  represents an impulse excitation to initiate oscillation<sup>1</sup>. This nonlinear I-V characteristic is similar to that displayed in a Gunn diode and is thus a reason for their use in microwave oscillators. For small deviations of  $v_C$  from  $V_0$ , the system behaves in an approximately linear fashion:

$$sC \tilde{v}_C(s) + \frac{1}{sL} \tilde{v}_C(s) - g_1 \tilde{v}_C(s) = q_0 \quad (2.3)$$

<sup>1</sup>In a practical oscillator, thermal noise often provides this stimulus.

Hence, the “small-signal” linear system displays an exponentially growing sinusoidal voltage across the capacitor:

$$v_C(t) = V_B + \frac{q_0}{C} e^{+\frac{t}{\tau}} \cos \left( \omega_{lti} t - \text{atan} \left( \frac{1}{\omega_{lti} \tau} \right) \right) \quad (2.4)$$

where  $\tau \equiv \frac{2C}{g_1}$  and  $\omega_{lti} \equiv \sqrt{\frac{1}{LC} - \left(\frac{g_1}{2C}\right)^2}$ .

For a “high-Q” tank such that  $Q \equiv (g_1 R_0)^{-1} \gg 1$  and  $R_0 \equiv \sqrt{\frac{L}{C}}$ , we have  $\frac{1}{\tau} \ll \frac{1}{\sqrt{LC}} \approx \omega_{lti}$ , and the amplitude exponential envelope is said to be “slowly varying.”<sup>2</sup> This situation allows us to substitute  $v_C = V_B + V_{osc} a(t) \cos(2\pi f_{osc} t)$  where the normalized amplitude function  $a(t)$  is roughly constant during a single oscillation cycle,  $2\pi f_{osc} \approx \frac{1}{\sqrt{LC}}$ , and the quantity  $V_{osc}$  is defined as follows<sup>3</sup>

$$V_{osc}^2 \equiv \frac{4}{3} \frac{g_1}{g_3} \quad (2.5)$$

We then multiply by  $\cos(2\pi f_{osc} t)$  and average the nonlinear differential equation in (2.2) over one oscillation period to obtain the somewhat simpler (but still nonlinear) equation for the envelope,

$$\tau \frac{d}{dt} a - a(1 - a^2) = 0; \quad a(t=0) = a_0 \equiv \frac{q_0}{CV_{osc}} \quad (2.6)$$

where the effect of the impulse current is shown as the initial conditions on the amplitude.

Solving, we obtain

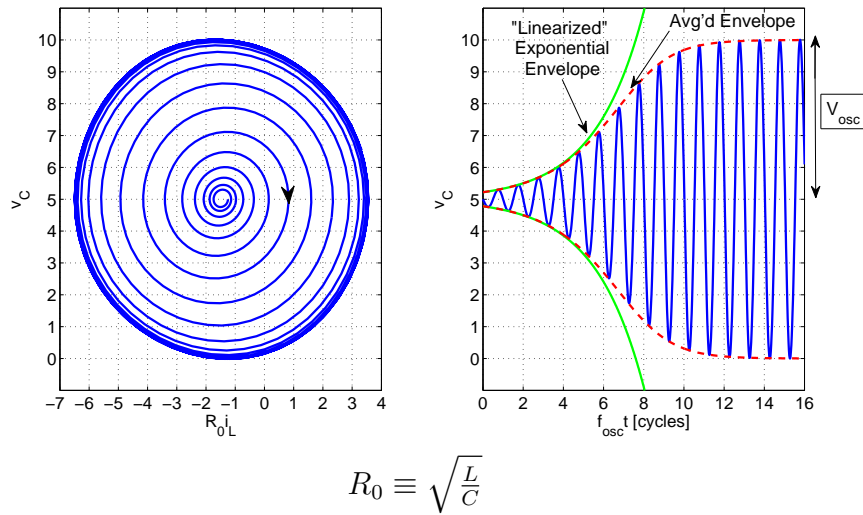
$$a^2(t) = \left( 1 + [a_0^{-2} - 1] e^{\frac{-2t}{\tau}} \right)^{-1} \quad (2.7)$$

The solution to this equation is plotted on Fig. 2.3 (“avg’d envelope”) along with the linearized system’s exponential envelope and the instantaneous oscillation waveform.

<sup>2</sup>We shall revisit this slowly varying assumption in the context of modulation-method phase-noise analysis in Section 6.1.2.

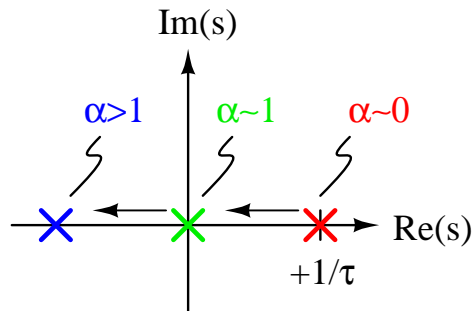
<sup>3</sup>It is shown in the subsequent discussion that this quantity is the steady-state amplitude of oscillation.





**Figure 2.3.:** Van der Pol Oscillator Phase Portrait, Startup Waveforms, and Envelope

Examining the averaged equation (2.6), we note that for small amplitude  $a \ll 1$ , the amplitude system has a single right-half-plane (RHP) pole ( $s_0 = \frac{\pm 1}{\tau}$ ), corresponding to the initial exponentially growing amplitude; however, as the amplitude approaches the steady-state value ( $a \rightarrow 1$ ), the pole moves to the origin ( $s_1 = 0$ ), as shown in Fig. 2.4, indicating a constant steady-state amplitude. Furthermore, if the amplitude is perturbed to be larger



**Figure 2.4.:** Root Locus for Averaged Amplitude (Envelope) System of Van der Pol Oscillator

than the steady-state value  $V_{osc}$ , then the pole moves into the left-half plane (LHP), and the

amplitude decays until it again reaches the steady-state value  $V_{osc}$ . This behavior indicates an “orbitally stable” oscillator. Graphically, we can visualize orbital stability on a phase portrait, which plots one oscillator “state variable” versus the other. For example, the oscillator of Fig. 2.2(a) has two state variables, viz. the capacitor voltage and the inductor current, which correspond to the y- and scaled x-axes, respectively, shown on the oscillator phase portrait in Fig. 2.3. The plotted trajectory illustrates the oscillator startup plot for an initial capacitor voltage of 5V and initial inductor current of -76.51 mA (corresponding to  $q_0 = 1.074$  pC and  $a_0 = 0.04409$ ). For reference, the corresponding time-domain waveform of the capacitor voltage is horizontally aligned with the phase portrait in Fig. 2.3 to show the relationship with each other. We scale the inductor current by the resonator characteristic resistance  $R_0 \equiv \sqrt{\frac{L}{C}}$  so that all plotted values are voltages and so that the steady-state trajectory (called a *limit cycle* [29]) is roughly circular. Note that the “radius” of that circle is the oscillation amplitude  $V_{osc}$ . An orbitally stable oscillator always returns to this limit cycle if perturbed off of it. We will return to the concept of a limit cycle when discussing phase noise and spectral purity later in this section.

While the voltages, currents, and charges *must* be nonlinearly related, lest the oscillation amplitude be undetermined, the question remains whether the device-noise-to-*phase* relationships are at least approximately linear. The question of voltage/current to phase transfer relationship is critically important to phase-noise analysis, as we shall see in Section 2.5. The concept is also important in angle-modulation systems and in phase-locked-loop (PLL) analysis. Furthermore, it has been shown [30–32] that to properly describe injection locking (“entrainment”)<sup>4</sup> behavior, a nonlinear voltage/current-to-phase relationship is required. We shall see a method of phase-noise analysis that is closely related to the methods employed in injection-locking analysis [31,32], and is often termed the “modulation method” (cf. Section 6.1.2). Nonetheless, many phase-noise analysis techniques

<sup>4</sup>Injection locking is the synchronization of two oscillators by injecting a “master” oscillator’s waveform as an input into a “slave” oscillator circuit so that the slave a a result runs at the same frequency as the master [32].

treat the transfer characteristic from device noise to phase as linear but time varying, and this approximation yields reasonable results in many cases of interest, as we shall see in Section 6.1.

Oscillator design consists of selecting a circuit topology and appropriate component values to adjust the aforementioned oscillator attributes—oscillation frequency, oscillation amplitude, and phase noise—to the desired/specified values. (See Section 3 for a detailed discussion of oscillator design tradeoffs and performance metrics.) We continue our present discussion with the two main classes of oscillator topologies from which to begin the design procedure: resonant and relaxation oscillators.

## 2.2 Types of Oscillators: Resonant v. Relaxation

In his 1934 compendium of nonlinear oscillator theory, Balthazar van der Pol classified oscillators as either "resonant" or "relaxation" depending on the resonator quality factor [28], or alternatively how quickly the oscillation amplitude grew relative to the oscillation frequency itself. At that time most oscillators comprised LC tanks and vacuum tubes, and given the availability of relatively low-loss discrete passives, a relatively high Q could be achieved, implying the oscillation amplitude grew slowly compared to the frequency of oscillation<sup>5</sup>. Indeed van der Pol often employed the "slowly varying phase/amplitude assumption" [28,33], akin to the envelope analysis (cf. previous section) in which only the slow-varying components of the system response are examined.

Resonant oscillators typically have a nearly sinusoidal output waveform with relatively few harmonics<sup>6</sup>, while relaxation oscillators' output often resembles either a square wave

<sup>5</sup>This slow amplitude time constant compared to a relatively high oscillation frequency is related to the quality factor through the intuitive pseudo-Q definition "full-width/half-max":  $\bar{Q} \equiv \frac{\Delta f}{f_0}$ , where  $\Delta f$  denotes the half-power bandwidth of the resonator, and  $f_0$  denotes the resonator center frequency

<sup>6</sup>The nearly sinusoidal approximation most closely parallels van der Pol's cubic nonlinear analysis for the oscillation amplitude and frequency [28], while a hard-switching approximation is quite useful for ring/relaxation oscillators.

(for ring oscillators), or a triangle wave (often seen across the timing capacitor of so-called “multivibrators” – see Section 3 for examples).

As previously mentioned, the oscillator frequency and amplitude are an oscillator’s two most common attributes of interest. Perhaps equally important is the question of whether the oscillator will start running (“startup”), and finally, the question of “how accurately” the oscillator runs (the issue of phase noise/jitter) also proves critical in many applications. The following sections will demonstrate how to ascertain these oscillator characteristics for both resonant and relaxation/ring oscillators by means of simple examples.

### 2.3 Steady-State Frequency and Amplitude (“Large Signal”)

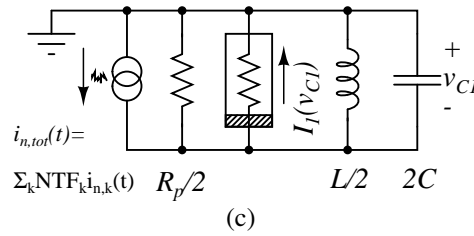
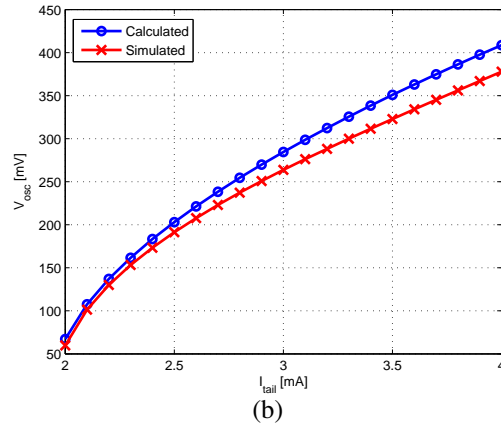
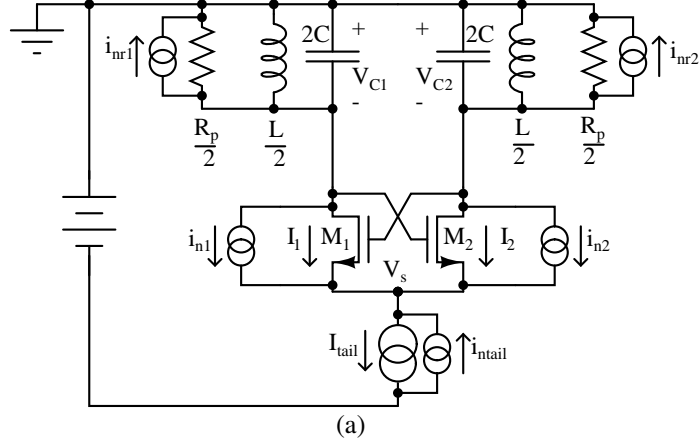
**Table 2.1:** Component values: (a) LC NMOS Oscillator, (b) Ring Oscillator

(a)								
$L$	$C$	$R_p$	$\mu_n$	$C_{ox}$	$W/L$	$V_{tn}$	$I_{tail}$	$\gamma$
[nH]	[pF]	[ $\Omega$ ]	[ $\frac{\text{cm}^2}{\text{Vs}}$ ]	[ $\frac{\text{fF}}{\mu\text{m}^2}$ ]	[ $\frac{\mu\text{m}}{\mu\text{m}}$ ]	[V]	[mA]	[-]
1.3	4.87	326	481.5	4.209	$32 \times (1.05/0.35)$	0.5	2.2	2/3

(b)							
$\mu_n = \mu_p$	$C_{ox}$	$V_{tn} = V_{tp}$	$(\frac{W}{L})_n = (\frac{W}{L})_p$	$V_{DD}$	$N_{stage}$	$\gamma$	$K_f$
[ $\frac{\text{cm}^2}{\text{Vs}}$ ]	[ $\frac{\text{fF}}{\mu\text{m}^2}$ ]	[V]	[ $\frac{\mu\text{m}}{\mu\text{m}}$ ]	[V]	[-]	[-]	[ $(\mu\text{V})^2\text{pF}$ ]
200	3	0.5	$10 \times (10/0.1)$	1	7	2/3	3

The following sections demonstrate how to solve for the oscillator periodic steady state for two simple “extreme” cases: (1) an LC resonant oscillator which is nearly sinusoidal (shown in Fig. 2.5(a)), and (2) a single-loop ring oscillator that exhibits nearly ideal hard switching (illustrated in Fig. 2.6(a)). Table 2.1 lists representative numerical component values of the two oscillators for sample calculations as we proceed.

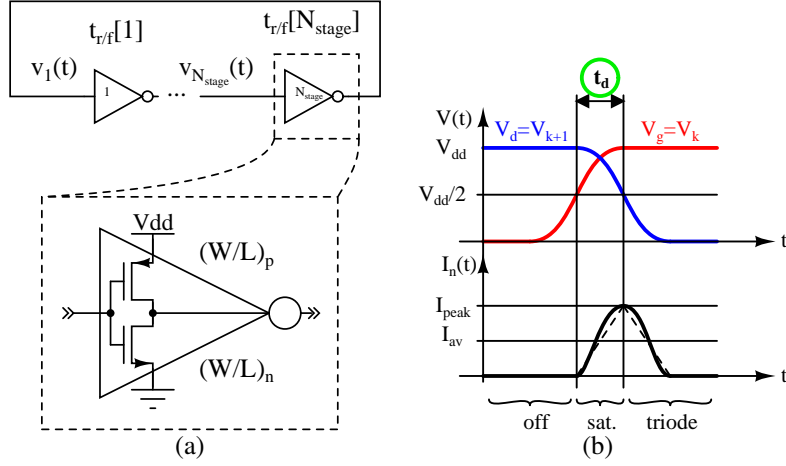


**Figure 2.5.:** Cross-Coupled LC oscillator (a) Schematic, (b) Peak Amplitude v.  $I_{tail}$ , and (c) Simplified Half Circuit

### 2.3.1 LC-Oscillator

The following equations describe the oscillator circuit shown in Fig. 2.5(a):

$$\left[ \frac{2}{R_p} + 2C \frac{d}{dt} + \frac{2}{L} \int dt \right] V_{C1,2} = I_{1,2} + i_{nr1,2} + i_{n1,2} \quad (2.8)$$



**Figure 2.6.:** Ring Oscillator: (a) Schematic, (b) Voltage/Current Waveforms for Single Stage

$$I_{1,2} = \frac{K}{2}(0 - V_{C2,1} - V_S - V_{tn})^2; I_1 + I_2 = I_{tail} - \underbrace{(i_{ntail} + i_{n1} + i_{n2})}_{i_n} \quad (2.9)$$

where  $K = \mu_n C_{ox} \frac{W}{L}$ ,  $I_{1,2}$  are the drain currents of  $M_{1,2}$ , and  $i_{nr1,2}/i_{n1,2}$  are the noise currents from the resistors/transistors, respectively, as indicated in Fig. 2.5(a). Eliminating  $V_S$ , we obtain

$$I_{1,2} = f(V_{C1,2} - V_{C2,1}, i_n)$$

$$f(V_{dm}, i_n) \equiv \frac{I_{tail} - i_n}{2} (1 + 2x\sqrt{1 - x^2}) \quad (2.10)$$

$$x \equiv \frac{V_{dm}}{2\sqrt{(I_{tail} - i_n)/K}}$$

$$\Rightarrow g_{m1,2} \equiv \frac{\partial I_{1,2}}{\partial V_{gs1,2}} = \sqrt{K(I_{tail} - i_n)} (\pm x + \sqrt{1 - x^2}) \quad (2.11)$$

Assuming  $v_{C1} \approx -v_{C2}$  yields a single-terminal nonlinear resistor on each side of the oscillator, so we can decouple the problem into half circuits as shown in Fig. 2.5(c). Evaluating a Taylor series of (2.10),

$$I_1(v_{C1}) \approx \underbrace{\frac{I_{tail}}{2}}_{g_0} + \underbrace{\sqrt{KI_{tail}}}_{g_1} V_{C1} + \underbrace{0}_{g_2} V_{C1}^2 - \underbrace{\frac{K}{2} \sqrt{\frac{K}{I_{tail}}}}_{g_3} V_{C1}^3 \quad (2.12)$$

For systematic harmonic-balance analysis, turn off the noise sources, and assume a “harmonic” solution  $v_{C1,2}(t) = \pm V_{osc} \cos(2\pi f_{osc} t)$ . Next, substitute into (2.8), and solve for  $V_{osc}$  and  $f_{osc}$  by neglecting higher-order harmonics and setting each harmonic coefficient on the LHS to zero (“balancing” with the RHS). This single-harmonic method is sometimes called a “describing-function” method [34]; in this case, the describing function is an equivalent admittance at the  $v_{C1}$  node:

$$Y_{describe}(V_{osc}, 2\pi j f_{osc}) \equiv \frac{1}{V_{osc}} \int_{2\pi} \frac{d\theta}{2\pi} e^{-j\theta} \left\{ \begin{aligned} & -[2\pi f_{osc}] 2C V_{osc} \sin(\theta) + \frac{V_{osc} \sin(\theta)}{[2\pi f_{osc}] L/2} - I_1(V_{osc} \cos(\theta)) \\ & + \frac{2}{R_p} V_{osc} \cos(\theta) \end{aligned} \right\} \quad (2.13)$$

Setting the describing function equal to  $0 + j0$  yields the following two oscillation conditions [35], sometimes termed the “Barkhausen self-excitation condition:”

$$\begin{aligned} \operatorname{Re} \{Y_{describe}(V_{osc}, 2\pi j f_{osc})\} &= 0 \quad \text{“Energy-Balance”} \\ \operatorname{Im} \{Y_{describe}(V_{osc}, 2\pi j f_{osc})\} &= 0 \quad \text{“Resonance”} \end{aligned} \quad (2.14)$$

Substituting into the describing function (2.13) yields  $V_{osc} \approx \sqrt{\frac{4}{3} \frac{g_1 - 2/R_p}{g_3}} = 137 \text{ mV}_{\text{peak}}$  and  $f_{osc} \approx 1/(2\pi\sqrt{LC}) = 2.00 \text{ GHz}$  for the values in Table 2.1—within about 5% of the simulated values. For reference, Fig. 2.5(b) plots the simulated and calculated peak amplitude as a function of  $I_{tail}$  with other components fixed at the values in Table 2.1. Note that

because the peak amplitude  $V_{osc} < V_{tn}/2$  for the chosen values, our implicit assumption that the switch transistors M1,2 remain in saturation is valid.

### 2.3.2 Ring Oscillator

For the ring oscillator in Fig. 2.6(a), we use hard-switching analysis to find the oscillation frequency and amplitude. For simplicity, we assume that  $\mu_n = \mu_p = \mu$ ,  $V_{tp} = V_{tn} = V_t$ , and  $V_{DD}/V_t = 2$ . Hence, we have a delay-cell trip point of  $V_{trip} = V_{DD}/2$  as shown in the waveforms of Fig. 2.6(b). Approximating the current as a triangle wave as sketched in the figure,

$$\begin{aligned} t_d &= \frac{CV_{trip}}{I_{av}} = \frac{(2C_{ox}WL)(V_{DD}/2)}{\frac{1}{4}\mu C_{ox}(V_{DD}-V_t)^2} \\ \Rightarrow f_{osc} &= \frac{1}{2N_{stage}t_d} = \frac{1}{8N_{stage}} \frac{\mu}{L^2} V_{DD} \left(1 - \frac{V_t}{V_{DD}}\right)^2 = 89.3 \text{ MHz} \end{aligned} \quad (2.15)$$

for the component values in Table 2.1, and we have defined

$$C \equiv 2C_{ox}WL; I_{peak} \equiv \frac{\mu C_{ox}}{2}(V_{DD} - V_t)^2; I_{av} \approx \frac{1}{2}I_{peak} \quad (2.16)$$

Note that assuming  $V_{DD}/V_t = 2$  ensures the transistor remains in saturation until the waveform reaches the trip point as labeled on Fig. 2.6(b). The simulated value is 90.0 MHz (< 1% error). Similarly,

$$P \approx I_{av}V_{DD} \approx 37.5 \mu\text{W} \quad (2.17)$$

within 1% of the simulated value of 37.83  $\mu\text{W}$ . This power expression reflects the fact that only a single inverter is active at a time (“class B operation” [36]). Finally, the peak fundamental amplitude is, assuming a square-wave from 0 to  $V_{DD}$ ,

$$V_{osc} = \frac{4}{\pi} \frac{V_{DD}}{2} \approx 637 \text{ mV}_{\text{peak}} \quad (2.18)$$

within 7.5% of the simulated value (600  $\text{mV}_{\text{peak}}$ ).



## 2.4 Startup Analysis

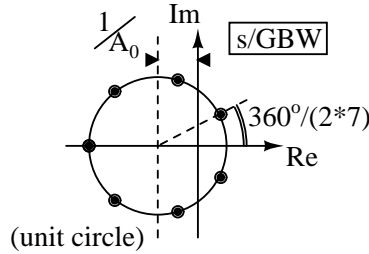
Having an unstable linearized DC operating point (i.e. characteristic roots in the RHP) allows an oscillator to start. For example, linearizing the ring-oscillator circuit in Fig. 2.6(a) assuming that all oscillation nodes are at  $V_{DD}/2$ , we obtain the characteristic equation:

$$1 - \underbrace{\left( \frac{-A_0}{1 + \frac{A_0 s}{GBW}} \right)^{N_{stage}}}_{=T(s)=\text{loop gain}} = 0 \quad (2.19)$$

where  $A_0 \equiv (g_{mp} + g_{mn})(r_{op} || r_{on})$  and  $GBW \equiv \frac{g_{mp} + g_{mn}}{C_{gp} + C_{gn}}$ . Solving yields the characteristic roots, written algebraically in (2.20) and illustrated graphically for  $N_{stage} = 7$  in Fig. 2.7:

$$\frac{s}{GBW} = - \left( 1^{1/N_{stage}} + \frac{1}{A_0} \right) \quad (2.20)$$

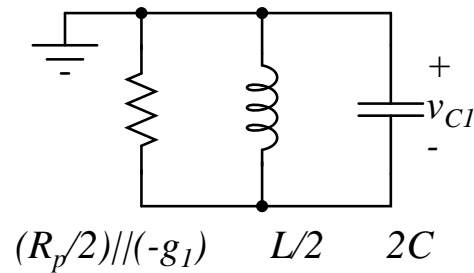
where  $1^{1/N_{stage}}$  denotes one of the  $N_{stage}$  complex  $N_{stage}$ -th roots of unity. As illustrated



**Figure 2.7.:** Single-Loop Ring Oscillator Startup: Characteristic Roots

in the figure, the poles shift towards the LHP by  $1/A_0$ , so the gain must be sufficiently large, i.e.  $A_0 > \sec\left(\frac{360^\circ}{2N_{stage}}\right)$ , for the oscillator to start. Note that as  $N_{stage}$  increases,  $\sec\left(\frac{360^\circ}{2N_{stage}}\right) \rightarrow 1$ , and the gain requirement relaxes.

Likewise for the LC oscillator of Fig. 2.5(a), linearizing about the balanced DC operating point, we obtain the half circuit in Fig. 2.8, where  $g_1$  is given by (2.12). Hence, the LC circuit starts for  $g_1 > \frac{2}{R_p}$ .



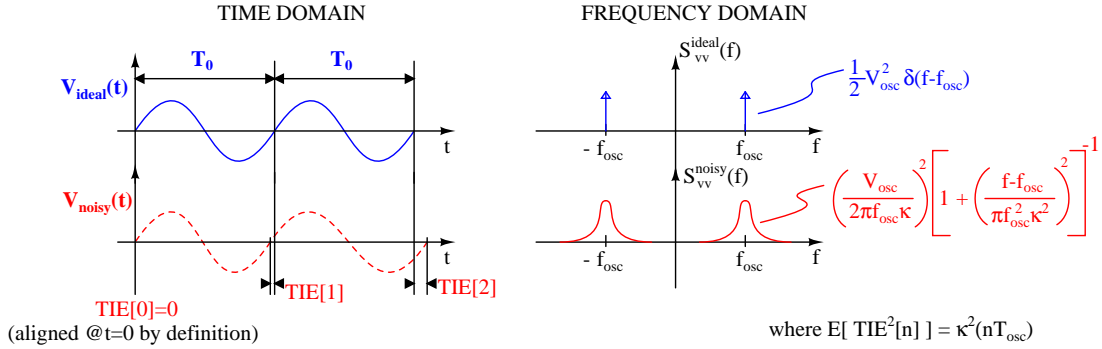
**Figure 2.8.:** LC-Oscillator Startup: Linearized Half Circuit

## 2.5 Spectral Purity

The frequency of oscillation and its accuracy and consistency are among the most important attributes of oscillators. The frequency can be measured in the "time domain" by counting the number of cycles in a given precisely-determined reference interval (or conversely by measuring the time taken to reach a certain number of cycles) [24, 37, 38]. Ideally, the number of counts increases linearly with the reference time interval; however, the presence of device and supply noise corrupts the zero-crossing instants of the oscillator output waveform, changing the times at which the oscillation cycles are completed. Relating one oscillator cycle to a single rotation of a mechanical wheel, we intuitively term the *phase* as our position on the wheel relative to the angle where we started, taking into account how many revolutions (cycles) we have completed. This viewpoint coincides with the common oscillator theoretical construct of a limit cycle, which plots a closed contour in the oscillator state space.

Alternatively, one can measure the power spectrum in the "frequency domain" with a swept-frequency heterodyne analyzer and infer the frequency from the fundamental spectral peak. An ideal oscillator without noise, disturbances, or component aging would have a single infinitesimally narrow peak (for an ideal spectrum analyzer with zero resolution bandwidth). Thus, measuring frequency accuracy involves determination of threshold-crossing instants of the oscillator's output voltage in the time domain, or requires deter-

mining the spectrum of the oscillator in the frequency domain. Fig. 2.9 illustrates the ideal and noisy oscillator waveforms in both the time and frequency domain. See Section 2.5.2 for further derivation and discussion of the oscillator output-voltage spectrum  $S_{vv}(f)$ .



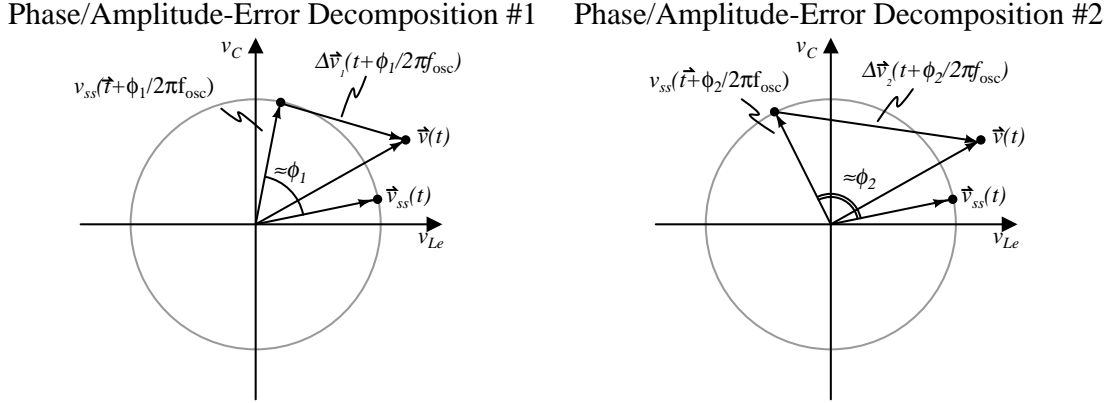
**Figure 2.9.:** Oscillator Frequency Error Measurement in Time and Frequency Domain

While radio-frequency (RF) applications typically describe this quality of the oscillation frequency as spectral purity in the frequency domain (typically called *phase noise*), microprocessor applications look at the performance in the time domain (typically called *jitter*). Phase noise and jitter both describe the underlying phenomenon of spectral purity/timing accuracy. Before delving further into metrics of spectral purity, the following section elaborates on the concept of *phase*, as different works in the literature often make varying assumptions/definitions as to what it means.

### 2.5.1 What “Phase” Means

Free-running oscillators, i.e. those not in a phase-locked loop (PLL), have no synchronization input (e.g. the PLL’s reference clock), so the  $\phi_0$  in (2.1) depends on startup conditions. Thus, free-running oscillators cannot correct phase error. Any phase error introduced by noise remains indefinitely, and the effects of phase perturbation accumulate over time, becoming arbitrarily large. For instance, consider the oscillator in Fig. 2.2(a), with state voltages  $\vec{v} \equiv [v_C, v_{Le}]^T$ , where we define  $v_{Le} \equiv i_L \sqrt{\frac{L}{C}}$  so that all state variables

are voltages. As mentioned in Section 2.1, if we plot of the oscillation waveform on axes  $v_C$  vs.  $v_{Le}$ , we obtain a *phase portrait* as shown in Fig. 2.10, and the steady-state waveforms  $\vec{v}_{ss}(t)$  correspond to the roughly circular trajectory in the figure called a *limit cycle* [29].



**Figure 2.10.:** Gunn-Diode-Oscillator Phase Portrait, Limit Cycle, and Illustration of Phase-Definition Ambiguity: Two “Arbitrary” Decompositions into Amplitude ( $\Delta\vec{v}$ ) and Phase ( $\phi$ ) Error

With noise, the oscillation waveforms deviate from  $\vec{v}_{ss}(t)$ , becoming

$$\vec{v}(t) \equiv \begin{pmatrix} v_C(t) \\ v_{Le}(t) \end{pmatrix} = \vec{v}_{ss} \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) + \Delta\vec{v} \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) \quad (2.21)$$

where  $\phi(t)$  indicates phase error (“along the limit cycle” because  $\phi(t)$  shifts the position on the steady-state limit-cycle contour  $\vec{v}_{ss} \left( \tilde{t} \equiv t + \frac{\phi(t)}{2\pi f_{osc}} \right)$ ), and  $\Delta\vec{v}(\tilde{t})$  indicates amplitude error (“away from the limit cycle” as shown in Fig. 2.10). The vectors  $\vec{v}_{ss}(t)$  and  $\vec{v}(t)$  are the same in both diagrams and represent the steady-state and noisy oscillation voltages, respectively. The two pictures show two different selections of  $\phi$  and  $\Delta\vec{v}$ , indicating that the *choice* of these two error functions  $\phi(t)$ ,  $\Delta\vec{v}(\tilde{t})$  is not unique, and how we choose them (1) determines whether  $\phi(t)$  or  $\Delta\vec{v}(\tilde{t})$  are “small” w.r.t.  $1 \text{ rad}$  or  $\vec{v}_{ss}(\tilde{t})$ , respectively, and (2) affects the spectra [35].

The multiple methods of phase-noise that will be discussed in Section 6 have different definitions for phase, and sometimes they assume  $\phi(t)$  is “small” to simplify calculation. While *not* true for free-running oscillators, this approximation gives reasonable results for white device-noise currents [30, 35, 39, 40]. The most precise definition of phase is the “position on the limit cycle [26, 41]<sup>7</sup>,” because this allows the instantaneous amplitude perturbations to remain small, consistent with experimental observation. This theoretical position on the limit cycle is difficult to measure, although we can infer when this “phase” has crossed integer multiples of  $2\pi$  by monitoring when a single state variable, say capacitor voltage, has a rising-edge zero crossing. Comparing the ( $n^{\text{th}}$ ) such zero crossing to a nearly ideal atomic clock will in fact show that the zero-crossing error with respect to the *corresponding* ( $n^{\text{th}}$ ) good clock edge grows without bound and eventually exceeds one oscillator period (on average) [42]. Such experimental observations confirm that free-running oscillator phase noise is not small, but accumulates to arbitrarily large values (on average). Locking the oscillator to a cleaner clock reference in a PLL will mitigate this effect.

### 2.5.2 Phase Spectrum vs. Voltage Spectrum

Consider the capacitor voltage  $v_C$  of the LC oscillator Fig. 2.2 mentioned above; device noise will cause both amplitude and phase fluctuations:

$$v_C(t) = V_{osc} [1 + a(t)] \cos(2\pi f_{osc}t + \phi(t)) \quad (2.22)$$

where  $a(t)$  is the normalized amplitude fluctuation for the capacitor voltage, and  $\phi(t)$  is the phase fluctuation (ideally unique irrespective of the node at which the phase is measured [43–45]). (The quantity  $V_{osc}a(t) \cos(2\pi f_{osc}t + \phi(t)) = \Delta v_C \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right)$  in (2.21).) Thus, we technically have three different spectra: phase noise  $S_\phi$ , output oscil-

<sup>7</sup>For theoretically precise definition, see Section 6.1.6 or [26, 41].

lator total voltage noise  $S_{v_C}$ , and normalized amplitude noise  $S_a$ . The units of  $S_\phi$ ,  $S_{v_C}$ , and  $S_a$  are  $\text{rad}^2/\text{Hz}$ ,  $\text{V}^2/\text{Hz}$ , and  $1/\text{Hz}$ , respectively. Neglecting the amplitude noise  $a(t)$ , because typically  $a(t) \ll 1$  (cf. Section 2.5.1 and below)<sup>8</sup>, we can obtain the capacitor voltage spectrum given the phase-noise spectrum:

$$S_{v_C}(f) \equiv \mathcal{F}_{\tau \rightarrow f} \left[ \lim_{T \rightarrow \infty} \int_{-T/2}^{T/2} \frac{dt}{T} \{R_{v_C}(t, \tau)\} \right] \quad (2.23)$$

where  $\mathcal{F}_{\tau \rightarrow f}$  denotes the Fourier Transform, and  $R_{v_C}$  is the capacitor-voltage autocorrelation:

$$R_{v_C}(t, \tau) \equiv \mathbb{E} [v_C(t + \tau/2)v_C(t - \tau/2)] = \frac{V_{osc}^2}{4} \mathbb{E} [e^{j[2\pi f_{osc}\tau + \phi(t+\tau/2) - \phi(t-\tau/2)]} + \dots] \quad (2.24)$$

where “...” indicates other similar terms from substituting a complex-exponential expansion of (2.22) (with  $a(t) \rightarrow 0$ ) into (2.24), and ensemble average  $\mathbb{E}[\cdot]$  is defined in the appendix. We shall see in Section 6.1.6 that the phase noise  $\phi(t)$  is asymptotically Gaussian for large  $t$  (considering white device noise alone) and has autocorrelation [35, 40, 46–48]:

$$R_\phi(t, \tau) \equiv \mathbb{E} [\phi(t + \tau/2)\phi(t - \tau/2)] = (2\pi f_{osc}\kappa)^2 \min(t + \tau/2, t - \tau/2) \quad (2.25)$$

for a “jitter constant”  $\kappa$  [ $units = \sqrt{sec}$ ], assuming white device noise only (see Section 6.1.3). Hence, using the characteristic function for Gaussian variables [49],

$$\mathbb{E} [e^{j[\phi(t+\tau/2) - \phi(t-\tau/2)]}] = e^{-\frac{1}{2}[R_\phi(t+\tau/2,0) + R_\phi(t-\tau/2,0) - 2R_\phi(t, \tau)]} = e^{-\frac{1}{2}(2\pi f_{osc}\kappa)^2|\tau|} \quad (2.26)$$

The time-averaged capacitor voltage autocorrelation  $\overline{R}_{v_C}$  is hence

$$\overline{R}_{v_C}(\tau) = \frac{V_{osc}^2}{2} \cos(2\pi f_{osc}\tau) e^{-\frac{1}{2}(2\pi f_{osc}\kappa)^2|\tau|} \quad (2.27)$$

<sup>8</sup>For some subtleties of amplitude-noise behavior, especially when Floquet normalization (cf. Section 6.1.6) is not employed, see [45].

This *output-voltage* autocorrelation corresponds to a “Lorentzian” spectrum (magnitude-squared response of 1st-order RC low-pass filter) [26, 50]<sup>9</sup>:

$$S_{v_C}(f) = \frac{V_{osc}^2}{2} \frac{2}{(2\pi f_{osc}\kappa)^2} \left[ \frac{1}{1 + \left(\frac{f-f_{osc}}{\pi f_{osc}^2 \kappa^2}\right)^2} + \frac{1}{1 + \left(\frac{f+f_{osc}}{\pi f_{osc}^2 \kappa^2}\right)^2} \right] \quad (2.28)$$

where  $f_{osc}$  denotes the oscillation frequency [Hz], and we have given the one-sided (positive frequencies only) spectrum. However, the *phase* spectrum is *not* Lorentzian, but on the contrary increases without bound for lower frequencies. Taking the time average of (2.25) with respect to  $t$  and then Fourier transforming<sup>10</sup>, we obtain

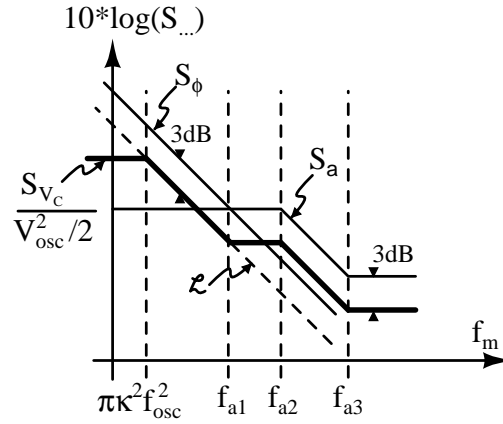
$$S_\phi(f_m) = \kappa^2 \frac{f_{osc}^2}{f_m^2} \quad (2.29)$$

where  $f_m$  is the offset from the carrier frequency  $f_m = f - f_{osc}$ . This unbounded “spectrum” at low frequencies reflects the fact that the free-running oscillator has no phase reference, so its phase becomes arbitrarily distant, on average, from the reference phase for large times. Fig. 2.11 plots typical curves for the phase-noise  $S_\phi$ , [normalized] output voltage  $S_{v_C}$ , amplitude-noise spectra  $S_a$ , and the quantity  $\mathcal{L}$  (defined below), where  $S_\phi(f_{a1}) = S_a(f_{a1})$  [34,39,40,45,54–62], and we have sketched a “typical” amplitude spectrum with corner frequencies  $f_{a2,3}$  [34, 39, 45]. For small  $f_m$ , phase noise dominates the voltage spectrum. While the phase-noise spectrum is proportional to  $f_m^{-2}$  for white device noise, the shape of the amplitude spectrum depends on the specific oscillator, the output node measured, and the phase/amplitude decomposition as discussed above [45]. Because for most practical oscillators, the amplitude noise is negligible compared to the phase noise

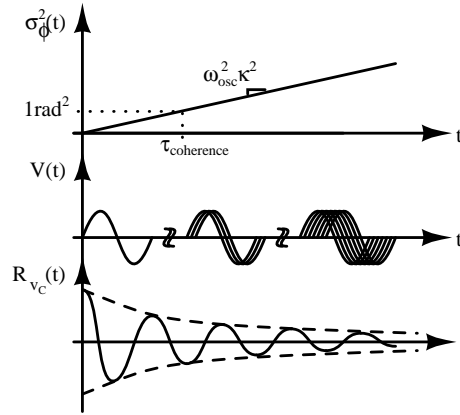
<sup>9</sup>When flicker noise is included, the voltage spectrum changes to a “Voigt profile,” Lorentzian at large frequency offsets, and  $\propto e^{-(f_m/f_{voigt})^2}$  at small offsets [51, 52].

<sup>10</sup>N.B. technically, defining spectra for  $\phi$  proves problematic, as it is not stationary and, what is worse, not bounded. This is in fact one reason why the Allan Variance is used [53, 54]. Moreover, not all random processes even have well-defined spectra. It is possible to “fudge” the spectra of unbounded signals by taking the limit of a Laplace transform  $S(p)$ :  $S_{eff}(\omega) \equiv \lim_{\epsilon \rightarrow 0} [S(\epsilon + j\omega) + S(\epsilon - j\omega)]$ , e.g.  $\mathcal{F}_{\tau \rightarrow f}(-|\tau|) = 2/(2\pi f)^2$  [43].

for offsets  $f_m$  of interest, we do not consider it further for brevity's sake. Comparing the



**Figure 2.11.:** Phase, Amplitude, and Output-Voltage Spectra:  $S_\phi$ ,  $S_a$ , and  $S_{V_C}$ , respectively (cf. [34, 39, 40, 45, 54–62]) in presence of white noise alone



**Figure 2.12.:** “Virtual Damping” due to unbounded free-running-oscillator phase noise [39, 63, 64]

phase and normalized capacitor-voltage spectra equations, for  $f_m \gg \pi(f_{osc}\kappa)^2$ , we get

$$\frac{S_{v_C}(f_{osc} + f_m)}{V_{osc}^2/2} \approx \frac{1}{2}S_\phi(f_m) \tag{2.30}$$



The plot thus demonstrates the relationship between  $S_\phi$ ,  $S_{v_e}$ , and  $S_a$  and shows that  $S_\phi(f_m)$  can be obtained by measuring the oscillator output spectrum  $S_{v_c}(f_{osc} + f_m)$  provided that  $\pi f_{osc}^2 \kappa^2 \ll f_m \ll f_{a1}$ , where  $f_{a1}$  indicates the frequency at which the amplitude and phase-noise spectra have comparable magnitude. Inferring the phase noise from the output-voltage spectrum under these constraints is the “direct-spectrum” phase-noise-measurement technique [57].

Experimentally, the effect of increasingly bad phase error can be observed by triggering multiple periods of oscillation on an oscilloscope and averaging the records together [63, 64]<sup>11</sup>. Fig. 2.12 plots this “virtual damping” effect along with the increasing phase variance  $\sigma_\phi^2(t)$ .

Phase-noise notation abounds in the literature. The current IEEE standard on time metrology [54] dicatates that the symbol  $\mathcal{L}$  refers to phase noise alone :

$$\mathcal{L}(f_m) \equiv \frac{1}{2} S_\phi(f_m) \quad (2.31)$$

However, in the past the convention *used to be* to normalize the voltage spectrum to total carrier power [54]:

$$\mathcal{L}_{old}(f_m) \equiv \frac{S_{v_c}(f_{osc} + f_m)}{\int_0^\infty S_{v_c}(f) df} \quad (2.32)$$

i.e. “single-sideband noise due to phase modulation.” Commonly, phase-noise units are quoted as “dBc[arrier]/Hz,” alluding to the older carrier-normalization definition; however, a more accurate notation would be  $\text{dB}(\text{rad}^2/\text{Hz})$ .

### 2.5.3 Sources of Phase Noise

Much of the discussion above has described white device noise, which typically arises from Johnson thermal noise [49]. However, for ring oscillators in particular, two other

<sup>11</sup>N.B. One could also perform Monte-Carlo transient simulations and average the runs to determine phase-noise properties [65].

noise sources are often dominant: flicker noise, bias noise, and often more significantly, supply noise.

Flicker device noise is theorized to arise from oxide interface traps in complementary metal-oxide-semiconductor (CMOS) devices [27]. The noise spectrum typically is significant at lower frequencies; however, as we shall discuss in Section 6, mixing effects generated by the large-signal switching action of the oscillator often convert this noise to around the frequency of oscillation, so that the flicker noise can dominate oscillator phase noise close to the carrier.

Power-supply noise arises from fluctuations to the oscillator's voltage supply. In modern microprocessors and application-specific integrated circuits, copious digital logic is integrated together with the oscillator, and the switching of this digital logic causes glitches on the supply, which in turn lead to oscillator phase noise. A ring oscillator's frequency is directly related to stage delay, which conventionally was a strong function of the supply-voltage level. Hence, developing methods to combat this dependence has become crucial to ensure that digital switching noise does not induce substantial jitter in the oscillator's zero-crossing points. Based on the oscillator fundamentals developed in this section, the next section surveys state-of-the-art oscillators and identifies design tradeoffs; the section also includes a dedicated discussion of state-of-the-art supply-noise rejection techniques, given the increasing importance of this phenomenon in modern integrated circuits with ring-oscillator-based clocks.

### 3. OSCILLATOR DESIGN TRADEOFFS

#### 3.1 Overview of State-of-the Art Resonant & Relaxation Oscillators

Since Balthazar van der Pol's time, the varieties of oscillators have exploded, with an increasing emphasis on the "relaxation" flavor, as these oscillators require no resonator and are therefore area efficient. This attribute makes them compatible with modern integrated-circuit CMOS processes and has led to their wide use in microprocessor and clock generation/recovery applications. Table 3.1 summarizes the main varieties of oscillators along with a taxonomy of the main distinguishing attributes among various types of ring oscillators. We next survey the recent literature to illustrate the variety of single/multiloop ring as well as LC oscillators and to provide a rough idea of their circuit attributes (frequency tuning/supply voltage/etc.).

First, consider the fully differential ring oscillator category [66–70]—Table 3.2 illustrates several different single-loop topologies with different voltage-controlled resistor (VCR) loads. Some topologies also have included a latch to sharpen the edges, improving slew rate (SR) and hence phase noise as well [12, 67, 68, 71–74]. Table 3.3 shows some examples of fully differential relaxation oscillators with multivibrator “delay cells” [75, 76]; often, multivibrators have just one “stage” as shown in the table. Next, Table 3.4 includes several illustrative multiloop, fully differential ring oscillators [6, 13, 67, 77], most notably Maneatis' array oscillator [6], which achieves sub-gate-delay timing resolution from its multiloop structure.

**Table 3.1:** Oscillator Taxonomy: (a) Overall (b) Ring/Relaxation-Oscillator Attributes

(a)		
Type	Signalling	
<ul style="list-style-type: none"> <li>• Resonant/LC</li> <li>• Relaxation/Ring</li> </ul>	<ul style="list-style-type: none"> <li>• Fully Differential</li> <li>• Pseudo Differential</li> <li>• Single Ended</li> </ul>	
(b)		
Loops	Delay Cell	Freq. Tuning
<ul style="list-style-type: none"> <li>• Single</li> <li>• Multi</li> </ul>	<ul style="list-style-type: none"> <li>• Simple CMOS</li> <li>• Current Starved               <ul style="list-style-type: none"> <li>– Saturated Starving Transistor</li> <li>– Triode Starving Transistor</li> </ul> </li> <li>• Resistor/VCR Load</li> <li>• Multivibrator</li> </ul>	<ul style="list-style-type: none"> <li>• Supply Voltage</li> <li>• Current</li> <li>• VCR</li> <li>• Capacitor</li> <li>• Delay Interpolation</li> </ul>

Tables 3.5-3.6 demonstrate several “single-loop” pseudo-differential ring oscillators [10, 71–74, 78–80]. The cases listed coincidentally are all quadrature oscillators. Quadrature oscillators are especially common, especially for half-rate clock-recovery circuits. In addition, Mirzaei et al. have shown that one can create a low-power, wide-locking range injection-locked frequency divider from a multi-loop ring-oscillator structure [81] provided that differential, quadrature outputs are available from an external VCO. Table 3.7 includes multi-loop pseudo-differential ring oscillators. We also note that even “single-loop” pseudo-differential ring oscillators could be considered multi loop if the latch path were considered as an alternate signal path instead.

Table 3.8 contains some representative single-ended MROs [13, 77, 82–84]. First, note the “skewed-negative-delay” oscillator proposed by Lee et al. [82]. We also include examples of delay-interpolation-tuned oscillators (cf. Section 3.6 for more details).

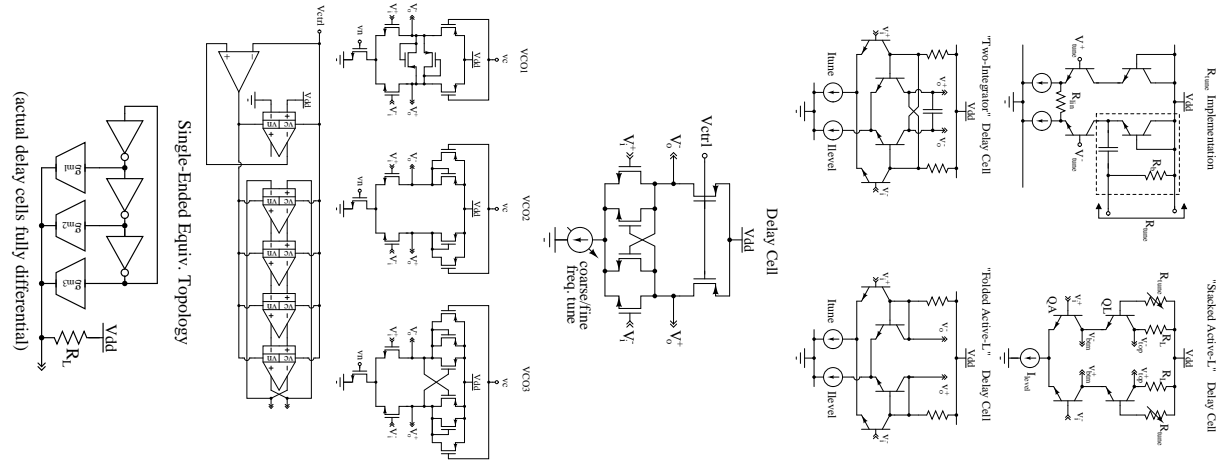
Finally, some “ring” oscillators use parasitic or explicit inductors to extract harmonics of the oscillation frequency—Table 3.9 has two examples [85–87]. While these oscillators could technically be listed as resonant oscillators, the frequency of oscillation and phase-noise performance more closely resemble that of ring oscillators because the resonator is “not in the loop,” i.e. the LC circuit acts as a post filter rather than as a part of the oscillator core.

**Table 3.2: Fully-Differential Oscillators: Single-Loop**

Reference		[70]	[69]/VCO1	[68]	[66]
<b>Frequency</b>	[GHz]	6	0.2	.15	9.8-11.5
<b>Power</b>	[mW]	60**	1.6	49.5**	75
$V_{DD}$	[V]	2	3.3	3.3	2.7
<b>PN<sup>†</sup></b>	[dBc/Hz]	-135**	-75	138	89
<b>Technology</b>	[ $\mu\text{m}$ ]	1***	0.5	.35	***
<b>Tuning Method</b>		VCR+Inductive Load	VCR	VCR	VCR+Inductive Load

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

Sketch



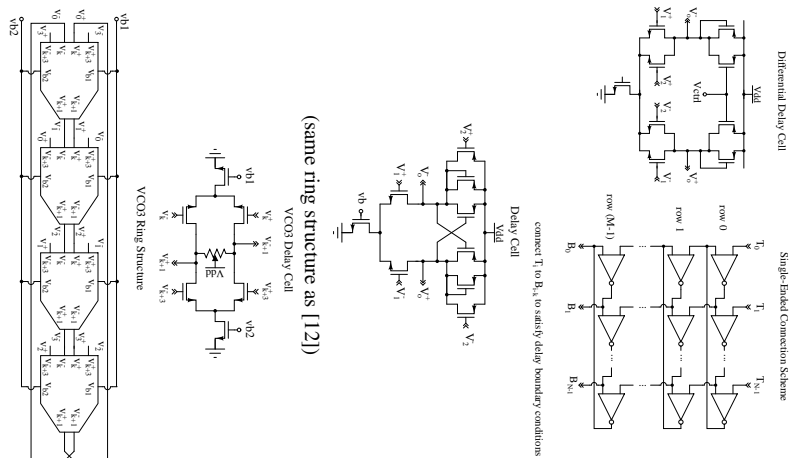
**Table 3.3: Fully Differential Multivibrators**

<b>Sketch</b>			
	Reference	[76]	[75]
Frequency	[GHz]	4.3-6.1	.3-1
Power	[mW]	80	3.5
$V_{DD}$	[V]	2	2.5
PN <sup>†</sup>	[dBc/Hz]	85	n/a
Technology	[ $\mu\text{m}$ ]	.18	.35
Tuning Method		Current	Current

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

**Table 3.4:** Fully Differential Oscillators: Multi-Loop

Sketch

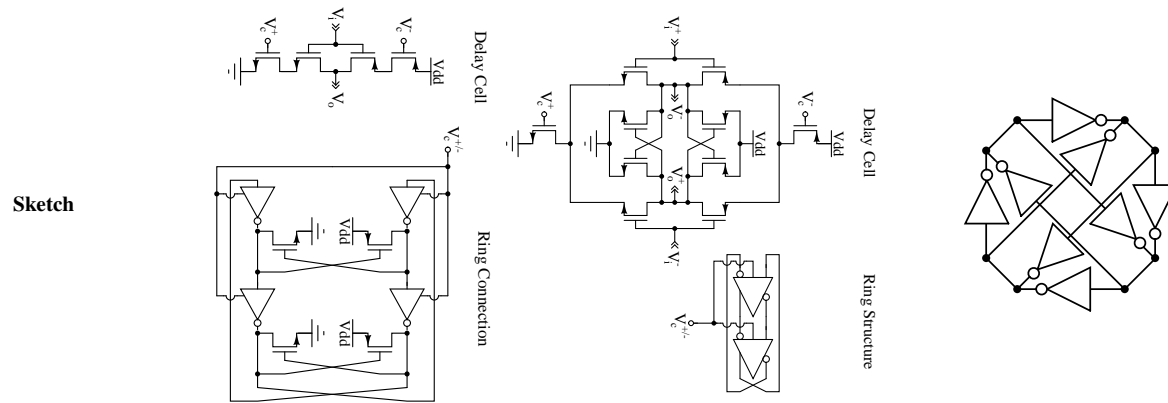


Reference		[13, 77]	[67]	[6]
Frequency	[GHz]	.4-2	.05-1.1	.005-.07
Power	[mW]	3	1.09	155
$V_{DD}$	[V]	3.3	1	2.5
PN <sup>†</sup>	[dBc/Hz]	89	n/a	n/a
Technology	[ $\mu$ m]	.5	.18	2
Tuning Method		Delay Interpolation	VCR	VCR

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS



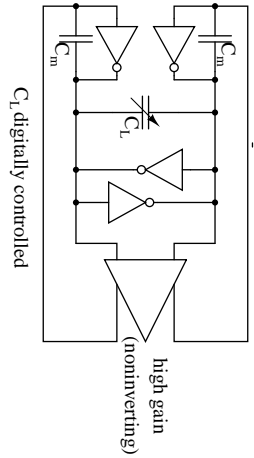
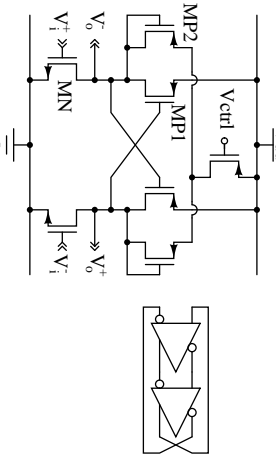
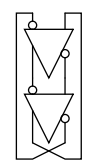
**Table 3.5:** Pseudo-Differential Single-Loop Oscillators (1/2)



Reference		[79]	[71–73]	[10]	[78]
Frequency	[GHz]	.65-1.04	.973	0.1-3.5	1.2-4.5
Power	[mW]	19	79.2	.16-16.2	n/a
$V_{DD}$	[V]	2	3.3	1.8	1.8
PN <sup>†</sup>	[dBc/Hz]	113	117	102-94	n/a
Technology	[ $\mu$ m]	.18	.35	0.18	.08
Tuning Method		VCR (current-starve/triode)	VCR (current-starve/triode)	Current	Supply

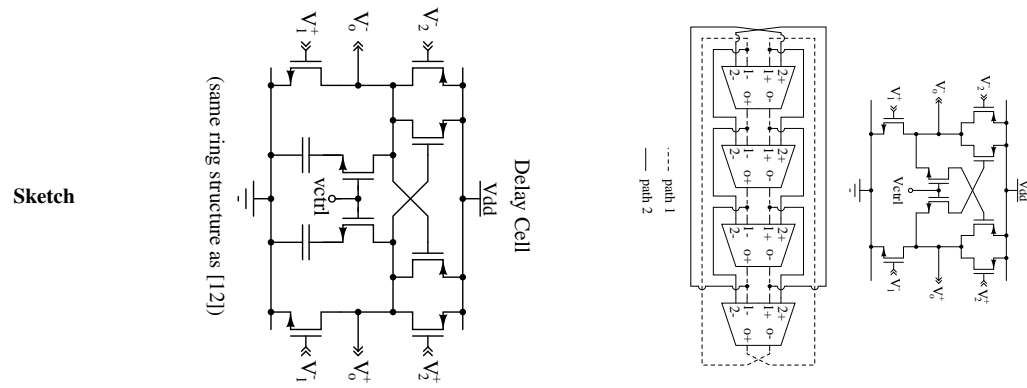
<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

**Table 3.6:** Pseudo-Differential Single-Loop Oscillators (2/2)

	Sketch		Reference				
			[80]	[74]	[74]	[74]	[74]
							
							
<b>Frequency</b>	[GHz]	.82-1.09	.797-1.58	.662-1.27	.495-.899	.291-.471	
<b>Power</b>	[mW]	6.12	26-33	15-18	7-7.7	2.2-2.25	
<b>V<sub>DD</sub></b>	[V]	1.2	3.0	2.5	2.0	1.5	
<b>PN<sup>†</sup></b>	[dBc/Hz]	113	125-128	126-129	127-129	127-128	
<b>Technology</b>	[μm]	.13	.25	.25	.25	.25	
<b>Tuning Method</b>		Capacitor (digital)	VCR (latch strength)				

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

**Table 3.7:** Pseudo-Differential Multi-Loop Oscillators



Reference		[15]	[16] 9-stage	[16] 3-stage	[12]
Frequency	[GHz]	.356-.931	1.1-1.86	5.16-5.93	0.75-1.2
Power	[mW]	30	n/a	n/a	30
$V_{DD}$	[V]	2	1.8	1.8	3
PN <sup>†</sup>	[dBc/Hz]	116	-105	n/a	-121
Technology	[ $\mu\text{m}$ ]	.5	0.18	0.18	0.6
Tuning Method		Capacitor (lead/lag "eff." cap.)		VCR (latch strength)	

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

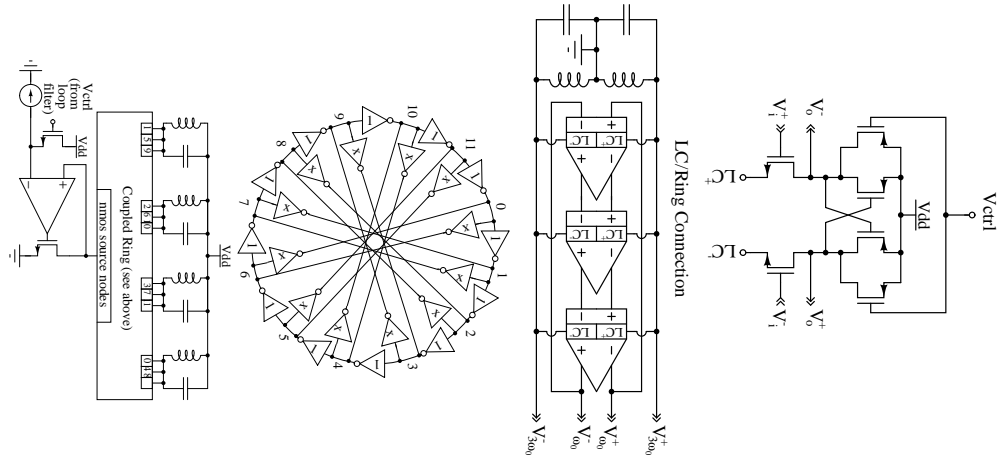
**Table 3.8:** Single-Ended MROs

	Sketch			
	<p>The sketch section contains four circuit diagrams. From left to right: 1. A VCO1 Delay Cell with nodes labeled <math>V_k</math>, <math>V_{k+1}</math>, <math>V_{k+2}</math>, and <math>V_{k+3}</math>, and a frequency <math>f_{osc}</math> (time) label. 2. A VCO1 Ring Structure consisting of a chain of inverters. 3. A Conceptual Delay Cell showing a PMOS and NMOS transistor network. 4. An Actual (5-Stage) structure showing a more complex multi-stage delay cell.</p>			
<b>Reference</b>		[13, 77] VCO1	[83, 84]	[82]
<b>Frequency</b>	[GHz]	.8-1.28	.163-.275	1.27
<b>Power</b>	[mW]	6	n/a	13.2
<b><math>V_{DD}</math></b>	[V]	3.3	5	5
<b>PN<sup>†</sup></b>	[dBc/Hz]	100	n/a	n/a
<b>Technology</b>	[ $\mu\text{m}$ ]	.5	1	0.8
<b>Tuning Method</b>		Delay Interpolation	Delay Interpolation	Supply

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

**Table 3.9: LC+Ring-Oscillator**

Sketch



<b>Reference</b>		[87]	[85, 86]
<b>Frequency</b>	[GHz]	2.4	0.92
<b>Power</b>	[mW]	4.2	.273
$V_{DD}$	[V]	1.5	1.3
<b>PN<sup>†</sup></b>	[dBc/Hz]	93	94
<b>Technology</b>	[ $\mu\text{m}$ ]	.18	.24
<b>Tuning Method</b>		Supply	VCR

<sup>†</sup> norm. to 1MHz assuming 20dB/dec slope, \*\* for tot. PLL, \*\*\* BiCMOS

### 3.2 Oscillator Specifications

An oscillator is an autonomous circuit which has no input yet generates a periodic output. Therefore, the oscillator characteristics such as frequency depend on the oscillator circuit parameters, and the design goal to have a frequency-stable oscillator is to control those parameters upon which the oscillation frequency depends as much as possible [24]. The most critical integrated-circuit VCO specs are typically frequency tuning range, phase noise/jitter, VCO gain  $K_{VCO}$  [GHz/V], power consumption, and area. Additionally, supply rejection or “pushing” as discussed previously is becoming increasingly important as more and more digital circuitry is integrated into the chip. Table 3.10 lists these specifications along with a few other oscillator performance metrics sometimes required.

**Table 3.10:** Typical Oscillator/VCO Specifications

Spec.	Description
$f_{osc}$ & TR	frequency tuning range
$\mathcal{L}(f_m)$	Phase Noise typically specified for RF/LC VCOs
$t_j$	Jitter (same phenomenon as phase noise) typically specified for micro-processor applications; specific jitter metrics often include period jitter and cycle-to-cycle jitter)
$K_{VDD}$	Static power-supply sensitivity $K_{VDD} \equiv \frac{V_{DD}}{f_{osc}} \frac{\partial f_{osc}}{\partial V_{DD}}$
$PSRR$	[dynamic] power-supply ripple rejection
$P$	time-average oscillator power consumption
$K_{VCO}$	VCO gain [GHz/V]; also its variation over control voltage range $V_{ctrl}^{min/max}$ as well as any associated settling time or input capacitance at the VCO control terminal may be important for PLL dynamics
$A$	oscillator die area
$P_{out}$	output level/power: dictates whether level shifter/low-to-high-swing buffer required for integrated VCOs
drift	variation of frequency over (say) temperature
harmonics	purity of the output spectrum/harmonic levels [dBc] less important for microprocessor clock generators than for pure-tone generators.

### 3.3 Oscillator Figures of Merit (FOMs)

Table 3.11 itemizes several VCO figures of merit (FOMs) found in the literature, with the more commonly used FOMs listed at the top [25, 88–97]. By far the most commonly reported is the standard VCO FOM ( $FOM_{std}$  listed in the first row), which conveys the phase noise of the oscillator  $\mathcal{L}(f_m)$  normalized by both the relative offset from the oscillation or “carrier” frequency  $\left(\frac{f_{osc}}{f_m}\right)$  and the power in [mW]. This normalization assumes that the phase noise is dominated by white device noise so that the phase noise  $\mathcal{L}(f_m)$  rolls off with respect to  $f_m$  at a rate of -20 dB/dec (as discussed in Section 2). The next common performance metric is oscillation frequency for a given power consumption  $FOM_{power}$ , which is often important in microprocessors for mobile applications. This performance could also be particularly important for the real-time clock (RTC), as this component often must run when the remainder of the chip is in sleep mode and hence must be quite power efficient. The last two FOMs ( $FOM_A$  and  $FOM_T$ ) are slight variants on the standard VCO FOM to account for oscillator area and percentage tuning range, respectively.

### 3.4 State-of-the-Art Multi-Loop Ring-Oscillator Performance Survey

To give an idea of achievable performance, Table 3.12 lists the salient attributes of state-of-the-art ring-oscillator VCOs from the last 10 years [2, 10, 13–15, 18, 19, 22, 71, 74, 76, 79, 93, 95, 98–106]. Phase-noise numbers marked with an asterisk (\*) indicate that the equivalent free-running VCO phase noise was inferred from a closed-loop PLL jitter measurement, assuming white noise [24]. The number of phases indicates the number of equivalent single-ended stages in the ring. From these data, we see that most ring-oscillator VCOs achieve figures of merit in the range of 140-160 dBc/Hz. LC VCOs have higher  $FOM_{std}$  because their resonator Q improves the phase noise without any power penalty—the amount by which their FOM exceeds typical ring-oscillator FOMs (assuming

**Table 3.11:** (a) Summary of VCO Figures of Merit (FOMs) Found in the Literature, (b) Formula Term Definitions

(a)

Name	Definition	Units	Comments	Ref.
$FOM_{(std)}$	$\frac{1}{\mathcal{L}(f_m)} \left( \frac{f_{osc}}{f_m} \right)^2 \frac{1 \text{ mW}}{P}$	[Hz]	most commonly reported for VCOs	[25, 88–90]
$FOM_{power}$	$\frac{P}{f_{osc}}$	[W/Hz]	for microprocessor/controller PLLs and RTCs	[91]
$FOM_A$	$\frac{1}{\mathcal{L}(f_m)} \left( \frac{f_{osc}}{f_m} \right)^2 \frac{1 \text{ mW}}{P} \frac{1 \text{ mm}^2}{A}$	[Hz]	accounts for VCO area	[92–94]
$FOM_T$	$\frac{1}{\mathcal{L}(f_m)} \left( \frac{f_{osc}}{f_m} \right)^2 \frac{1 \text{ mW}}{P} \frac{10}{TR}$	[Hz]	accounts for VCO % tuning range	[95–97]

(b)

Name	Units	Description
$f_{osc}$	[Hz]	[nominal] frequency of oscillation
$\mathcal{L}(f_m)$	[1/Hz]	SSB “Phase Noise” $\mathcal{L}(f_m) \equiv \frac{1}{2} S_\phi(f_m)$ (often quoted in [dBc/Hz])
$f_m$	[Hz]	offset from $f_{osc}$ for Phase Noise
$P$	[mW]	oscillator average power consumption
$A$	[mm <sup>2</sup> ]	oscillator active area
$TR$	[unitless]	normalized frequency tuning range $TR \equiv \frac{f_{osc}^{max} - f_{osc}^{min}}{f_{center}}$



same process) depends on the achievable inductor Q; however, FOMs from around 170-190 dBc/Hz have typically been reported [89, 92].

**Table 3.12:** Performance Comparison of State-of-the-Art Ring-Oscillator VCOs over Last 10 Years

	$f_{osc}^{tune}$ [MHz]	$V_{DD}$ [V]	P [mW]	$\mathcal{L}(1 \text{ MHz}) @ f_{osc}$ [dBc/Hz]	$f_{osc}$ [MHz]	$FOM_{std}$ [dBc/Hz]	$\#\phi$ [-]	Tech. [ $\mu\text{m}$ ]	Area [ $\text{mm}^2$ ]
[71]	100-973	3.3	79	-117	973	157.8	4	0.35	n/a
[15]	356-931	2	30	-113.6	856	157.5	8	0.5	2 <sup>‡</sup>
[98]	500-2000	1	6.8	-89.5*	1400	144.1	8	0.13	0.064
[13]	880-1648	3.3	109	-83.23*	1250	124.8	8	0.35	1 <sup>‡</sup>
[22]	130-1600	2.5	2	-84.71*	1000	141.7	8	0.25	0.028 <sup>‡</sup>
[10]	100-3500	1.8	0.162	-93.96	3500	172.7	4	0.18	n/a
[99]	2250-2750	1.3	2.86	-95.4	2500	158.8	2	0.13	0.006
[100]	1800	1	0.087	-83.87	2005	160.5	3	0.09	0.013
[19]	1770-1920	1.8	13	-102	1770	155.8	8	0.18	0.002
[101]	3140-3890	1.2	2	-93	2400	157.6	6	0.13	0.001
[95]	160-2500	0.5	1.157	-87	2240	153.4	8	0.09	0.002
[102]	1100-1450	3.3	19.8	-88	1250	137	4	0.13	0.003
[103]	2240-2650	2.5	19.2	-96	2481	151.1	4	0.28	0.007
[14]	2500-9000	1.8	135	-82	5000	134.7	4	0.18	0.003
[104]	350-616	0.5	0.21	-114	550.9	175.6	6	0.13	0.017
[2]	2050-2850	3.3	10	-76.02	2500	134	4	0.4	320000
[105]	0.004-1100	3.3	10	-105.8	900	154.9	6	0.35	0.002
[18]	7300-7860	1.5	60	-103.4	7640	163.3	6	0.13	0.009
[76]	4300-6100	2	80	-85	5000	139.9	10	0.18	0.276
[74]	661.5-1270	2.5	15.4	-109.9	900	157.1	4	0.5	0.013
[79]	650-1040	2	18.95	-121	913	167.4	4	0.18	0.007
[106]	549-756	1.8	15.34	-114	700	159.1	8	0.18	0.007
[93]	3100-10600	1.2	13	-88.5	10600	157.9	4	0.13	0.013

$$* \mathcal{L} = 4\pi LBW_{PLL} \left( \frac{f_{osc}^{rms}}{f_m} \right)^2, \quad \ddagger \text{ Area of entire PLL}$$

### 3.5 Topology Selection

The first step in the design procedure is to select an oscillator topology. Selection between LC and ring oscillators is primarily decided by (1) phase noise for a given power budget, (2) tuning range, and (3) area. Compared to LC oscillators, ring oscillators typically have order of magnitude higher phase noise for a given power, order of magnitude higher tuning range, and order of magnitude lower area.

Fully differential ring oscillators offer better supply and other common-mode-noise immunity, but are less power efficient to achieve a given phase noise [24, 107]. This is because the single-ended ring oscillator uses current more efficiently by burning the peak current one delay cell at a time only during a transition (class B operation [36]), whereas the fully differential ring oscillator always burns  $I_{tail}$  in *every* delay cell *simultaneously* (class A operation). Also, due to its tail current source, the fully differential oscillator requires more headroom than the single-ended oscillator.

Finally, the fully differential delay cell suffers from tail-current noise. Integrated LC oscillators are typically differential cross-coupled structures like the one previously shown in Fig. 2.5(a). Additional LC-oscillator topologies are discussed in detail in [108].

## 3.6 Frequency-Tuning Method

### 3.6.1 Ring Oscillators

Ring oscillators can be tuned in a variety of ways:

- **Supply:** Changing the supply voltage of a simple CMOS ring oscillator adjusts its frequency. The technique is quite common in smaller size technologies where low voltage headroom constrains oscillator topologies essentially to simple single-loop CMOS ring oscillators. Note that this method requires a level shifter or low-to-high swing output buffer, as the oscillation amplitude changes along with the frequency.

- **Current:** The idea is to adjust the current available to charge a fixed load capacitance:
  - This method is used in current-starved ring oscillators with saturation-region starving transistors. The technique has the advantage of better supply rejection due to the output resistance of the starving transistor; however, the tradeoff is the reduced swing (and hence diminished phase-noise performance) along with reduced maximum oscillation frequency due to the reduced switching current available. For this reason, the current-starved topology typically employs fewer stages ( $N_{stage}$ ) to obtain a given  $f_{osc}$  than would a supply-tuned oscillator. It may still be advantageous to use a larger number of stages for low oscillation frequencies (instead of adding an explicit load capacitor) either (1) if the area consumed by the additional stages is less than that needed to add the explicit load capacitor for each stage, or (2) if the delay cell needed to track over process variations with, say, a logic gate which would not have such a capacitor [24].
  - Some digital PLLs have also tuned the oscillation frequency by digitally enabling how many parallel inverters are active to drive a fixed capacitive load [109]—this likewise amounts to a current-tuning scheme of sorts.
- **Voltage-Controlled Resistor (VCR):** Assuming the stage delay is an RC product, a voltage-controlled resistor can adjust the oscillation frequency. This method is employed in both fully-differential rings [110] and in current-starved rings with the starving transistor in triode [24].
- **Load Capacitor:** Conversely, the capacitor can be adjusted either digitally [80], with a series resistor to change the “effective” capacitance (really a lead/lag network) [15], or with a varactor.

- **Delay Interpolation:** The delay-interpolation method is somewhat older and suffers from inherent  $K_{VCO}$  variation assuming linear delay interpolation with respect to tuning voltage [24]. It has also been recommended [83, 84] that outer loop delay should be less than twice inner loop delay to avoid phase ambiguity (analogous to spurious modes of oscillation—cf. [6]).

### 3.6.2 LC Oscillators

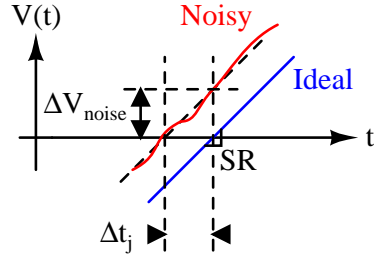
LC oscillators are almost always varactor tuned [111], often combined with a switched array of capacitors to broaden the tuning range as MOS varactors typically only vary by 30%. Similar to the ring-oscillator case, newer digital PLLs sometimes forgo the varactor altogether to yield a digitally controlled oscillator (DCO) driven by a digital loop filter [112].

## 3.7 Oscillation Frequency, Power, and Phase Noise

Oscillation frequency, power, and phase noise are closely tied together in oscillators. Timing error or jitter is inversely proportional to the slew rate and directly proportional to the voltage noise using the *jitter slew-rate equation* (3.1), as illustrated conceptually in Fig. 3.1:

$$\Delta t = \frac{\Delta V_{noise}}{SR \equiv \left. \frac{\partial V}{\partial t} \right|_{\text{zero crossing}}} \quad (3.1)$$

These relationships are derived more rigorously in Section 6.1.3. Because slew rate is typically given by the ratio of a current to a capacitance, we intuitively conclude that better phase noise typically requires increased power consumption, which is indeed the case for both ring and LC oscillators [24, 36, 107, 113, 114]. Larger oscillation amplitude for a given frequency also yields improved slew rate and hence better jitter, assuming noise remains the same in both cases. Furthermore, it can be shown [24] that in the presence of



**Figure 3.1.:** Jitter-Slew-Rate Equation Conceptual Illustration

white noise only, the jitter  $\sigma_j^2(T)$  and phase noise  $S_\phi(f_m)$  of any free-running oscillator take the form

$$\sigma_j^2(T) \equiv \mathbb{E} [t_j^2(T)] = \kappa^2 T; S_\phi(f_m) = \kappa^2 \left( \frac{f_{osc}}{f_m} \right)^2 \quad (3.2)$$

for some  $\kappa$ , where  $T$  is the time between the initial and final observed zero crossings of the oscillator waveform. Finally, it will be shown in Section 6.1.5 that conversion of flicker noise to phase noise/jitter is related to the *DC level* of the slew rate. Thus, symmetric rise/fall characteristics are desired for low flicker-noise-induced phase noise [107, 113, 114]. These phase-noise issues yield the following design guidelines/tradeoffs for ring/resonant-LC oscillators.

### 3.7.1 Ring Oscillators

The power,  $f_{osc}$ , and phase noise of single-loop ring oscillators are completely determined by the characteristics of a single delay cell and by the number of such cells. In the single-loop oscillator,  $f_{osc}$  is increased by either reducing the load capacitance for fixed transistor drive strength or by increasing the drive strength. For a simple CMOS ring, this involves reducing  $L$  with  $W$  held fixed. The tradeoff is increased flicker noise [107]. To the first order, changing the width  $W$  with  $L$  held fixed will not affect the  $f_{osc}$  because capacitance and peak current both scale linearly with  $W$  [24]. Similarly, one could explic-

itly add capacitance to each delay stage to reduce  $f_{osc}$  instead of having a large number of stages. This action makes the oscillation frequency depend less on transistor parasitics, yielding improved predictability.

By symmetry of the ring, one can show that the jitter number  $\kappa$  does not depend on the number of stages, so the accuracy of the oscillator to resolve time and hence the jitter depends on the unit-delay cell's accuracy alone and *not* on the number of stages [24]. However, further examining (3.2), we note that because  $f_{osc}$  is inversely proportional to the number of stages  $N_{stage}$  (as derived in Section 2.3.2), the phase noise for a fixed  $f_m$  will change w.r.t.  $N_{stage}$  assuming the delay cell remains the same. We will revisit this focus on the unit delay cell in Section 5 when discussing our proposed general approach to multi-loop ring-oscillator design and analysis.

To optimize phase-noise performance for fully differential oscillators, minimize the number of stages, as this allows the most power per stage and hence the lowest phase noise [24, 36, 107]. Because single-ended ring oscillators only burn power one delay cell at a time, their phase-noise performance is largely unchanged as  $N_{stage}$  changes assuming fixed power and  $f_{osc}$  (shown rigorously in Section 6.1.3).<sup>1</sup> To maximize the slew rate and improve phase noise, increase the transistor drive strength by choosing the lowest threshold voltage  $V_t$  devices and by using the maximum power available in the budget (achieved by either increasing  $I_{tail}$  or  $(\frac{W}{L})$  in the fully differential or single-ended cases, respectively). Also, choose the maximum possible supply voltage to maximize swing. Inclusion of a latch helps to sharpen the edges and improve jitter performance. To sharpen the waveform transition and enhance the slew rate, some have proposed to include a latch even in a fully differential oscillator that would not otherwise need one to sustain oscillation [12, 67, 68, 71–74]; however, it has been noted that adding a latch does not always yield phase-noise

<sup>1</sup>The above guideline assumes *thermal/white* phase noise dominates; if flicker noise dominates instead, a larger number of stages will yield less noise for a fixed  $f_{osc}$  and overall power for both single-ended and fully differential rings (cf. Section 6.1.4) [24, 36, 107].

performance improvement [24]. Symmetric rise/fall times are achieved by choosing the appropriate sizing ratio  $\frac{(W/L)_p}{(W/L)_n}$  (typically  $\approx 3$ ) to compensate for the fact that  $\mu_p < \mu_n$ .

### 3.7.2 LC Oscillators

LC-oscillator frequency is fixed by inductor/capacitor selection; however, the oscillation amplitude and with it the phase noise improve as either the tank Q or tail current is increased. While the tail current remains in saturation, the oscillator is “current limited,” and  $V_{osc} = \frac{2}{\pi} R_p I_{tail}$ , where  $R_p$  is the equivalent parallel resistance of the *differential* tank seen by both switching transistors. However, for higher currents, the tail source begins to enter the triode region; the oscillation amplitude is roughly  $V_{DD}$ ; and the oscillator becomes “voltage limited” [115]. Phase-noise-improvement marginal returns for increased power (i.e.  $I_{tail}$ ) diminish once the oscillator enters the voltage-limited regime, as the amplitude no longer appreciably increases with additional increases in current, so typically, the efficient design point for optimal phase-noise performance under a given power budget is right around the boundary between the current- and voltage-limited regimes, as this maximizes  $V_{osc}$  for a given  $I_{tail}$  [113, 115].

Furthermore, complementary switching transistors (i.e. NMOS+PMOS) are recommended because (1) higher small-signal  $g_m$  and correspondingly better slew rate for a give power is achieved; (2) the single-ended waveforms have improved symmetry (causing less flicker-noise-induced phase noise); and (3) less voltage drop appears across each individual transistor (reducing short-channel effects, SCEs) [113]. LC oscillators have numerous other minor tweaks to improve phase noise further [116], most notably

1. minimize the analog component of  $K_{VCO}$ , and rely on discretely switching a capacitor bank as much as possible to minimize control-noise-to-phase-noise conversion [61, 117].

2. Filter the (tail) bias with an additional series LC resonator at  $f_{reson} = 2f_{osc}$ , as the source node of the switching transistors has a strong second-harmonic component [118].
3. Feed the tail current into a center-tapped inductor (part of the oscillator's resonator) to isolate high-frequency signals from reaching the tail source, thereby reducing flicker-noise upconversion [116, 118].
4. Also, a capacitor can be placed in parallel with the tail current source to shape the current pulses delivered to the switching transistors and reduce the phase noise by 4.5 dB or so [113, 119]. A potential tradeoff is increased capacitive coupling to the supply and with it degraded supply-noise rejection.

### 3.8 Supply-Noise Rejection

In older technologies, designers favored source-coupled delay cells because their differential operation and tail current source provided supply rejection; adding a replica biased, linearized voltage-controlled-resistor (VCR) load in each delay cell could also help the supply isolation [120, 121]. Another technique to increase VCOs' supply rejection is combining a high-impedance voltage-to-current (V/I) converter to supply the oscillator core (now effectively a current-controlled oscillator) [122]. By a similar token, each delay cell can be current starved: so long as the top/bottom "starving" transistors remain in saturation (requiring headroom), supply rejection would be improved [71, 120]. Additionally, laying out ring stages as symmetrically as possible causes the supply noise to be correlated so that only noise near integer multiples of  $N_{stage}f_{osc}$  is significant [71, 72, 107].

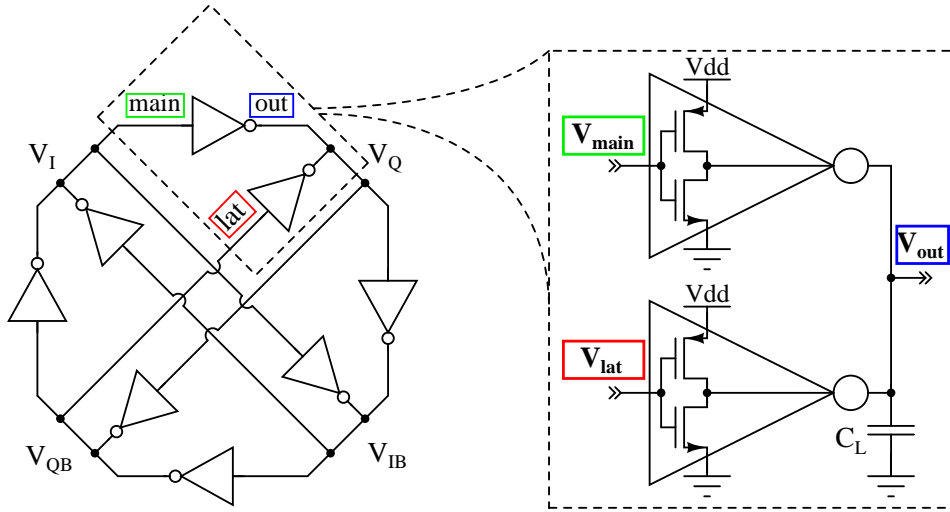
Newer technologies' reduced headroom has driven designers to consider simple CMOS-inverter rings to limit the number of stacked devices. These CMOS ring oscillators' frequency  $f_{osc}^c$  is determined by the number  $N_{stage}$  of stages and the delay time  $t_D$  to charge



a transistor's gate capacitance  $C_G$  to a switching threshold  $V_{th}^{sw}$  with an approximately constant current  $I_D$  from the previous stage:

$$f_{osc}^c \approx \frac{1}{2N_{stage}t_D} \approx \frac{I_D}{2N_{stage}C_GV_{th}^{sw}} = \frac{\frac{\mu C_{ox}}{2} \frac{W}{L} (V_{DD} - V_t)^2}{2N_{stage}(C_{ox}WL)(V_{DD}/2)} \quad (3.3)$$

Multi-loop ring oscillators (MROs) have more complex frequency expressions; however, if the MRO delay cell has transistors with their source terminal connected to the supply, i.e. the supply connected with a low-impedance path to the output such as that illustrated in the conventional CMOS-delay-cell quadrature oscillator of Fig. 3.2, then the frequency again heavily depends on supply. While allowing low-voltage designs with wide tuning



**Figure 3.2.:** Conventional CMOS-Delay-Cell Quadrature Oscillator [10, 78]

range, this supply dependence makes the circuit extremely sensitive to supply noise. These oscillators often need a dedicated regulator, and moreover, the regulator typically acts to buffer the PLL's charge pump voltage to tune the oscillator with the VCO "virtual" supply voltage, improving the oscillator's PSRR by that of the LDO. However, the LDO's poles then hinder the PLL's transient response, requiring either large regulator power to make the LDO agile, or more complicated split-tuned dual-loop PLL architectures to stabilize

the PLL [23, 121, 123–126]. Finally, recent works have compensated delay cells' supply dependence by carefully calibrating positive and negative delay-cell supply-sensitivity components to cancel each other [20, 22, 98, 100, 127]. Fig. 3.3 graphically summarizes these supply-rejection methods and illustrates each one with a conceptual schematic.

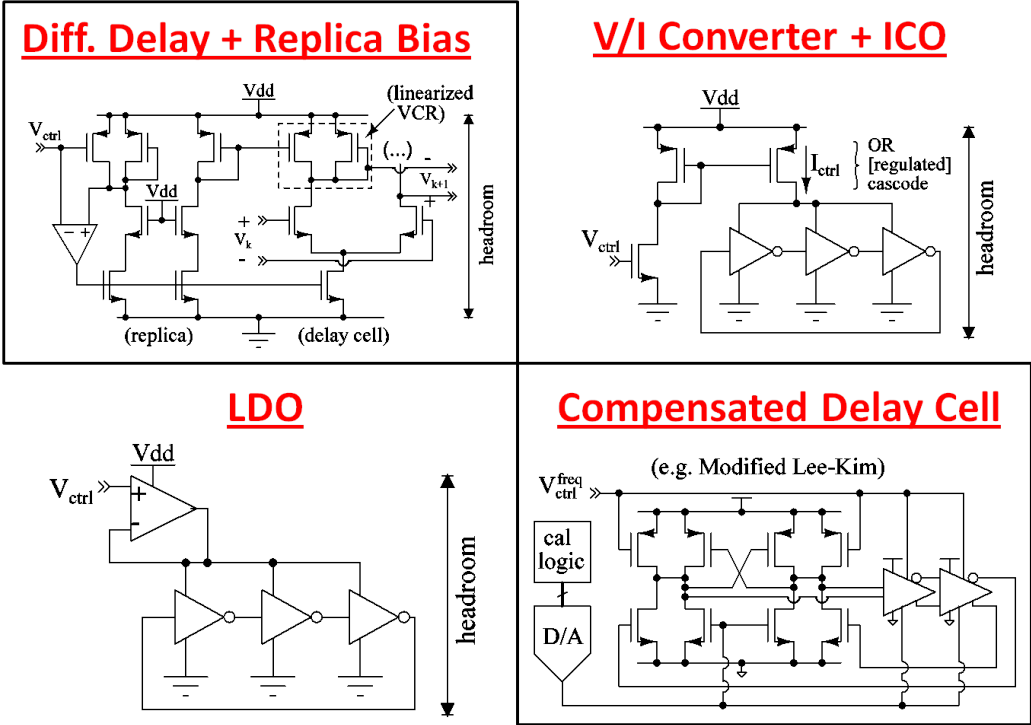
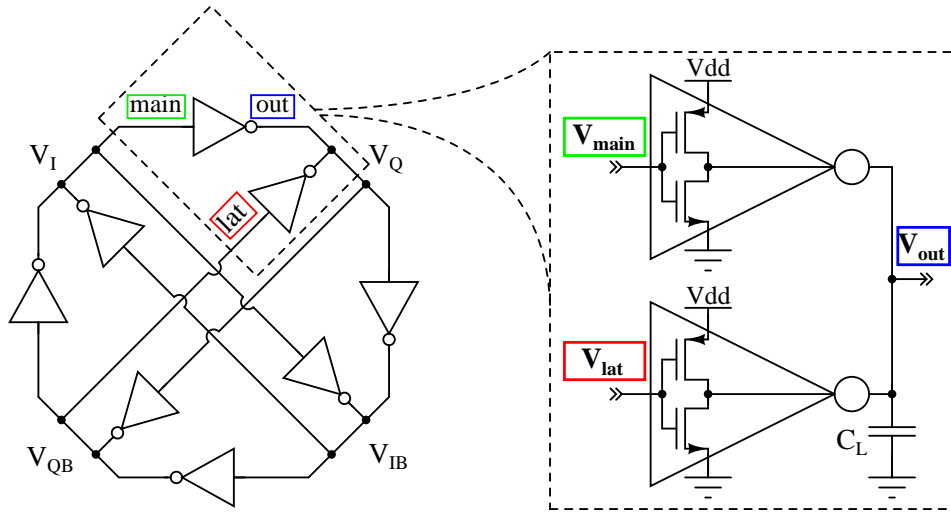


Figure 3.3.: Summary of Previous Supply-Rejection Methods

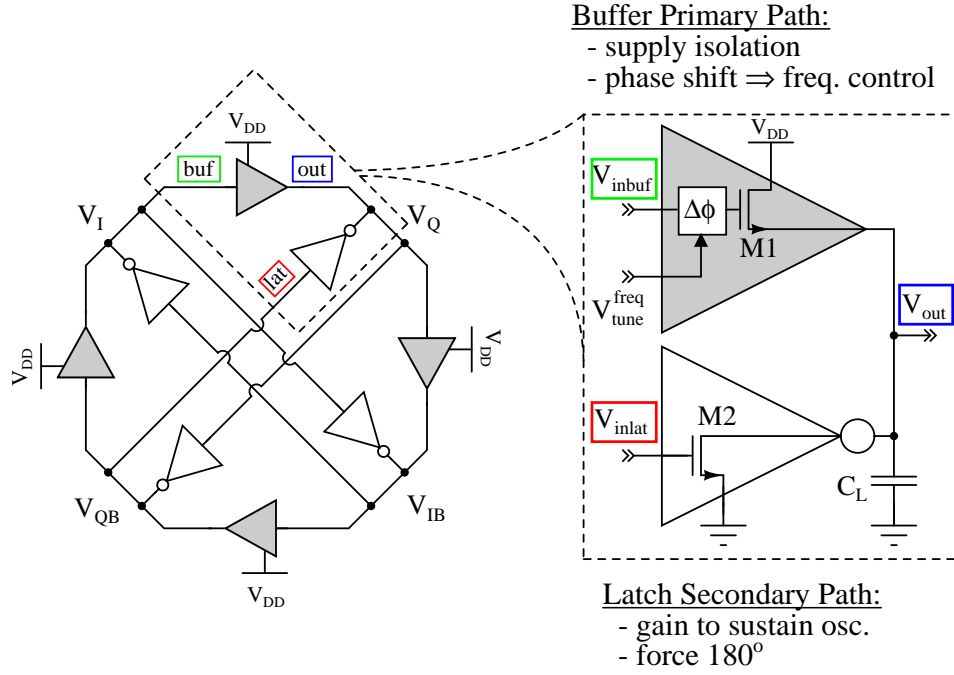
#### 4. PROPOSED MRO ARCHITECTURE TO IMPROVE SUPPLY REJECTION

First, consider the conventional quadrature oscillator formed from CMOS-inverter delay cells illustrated in Fig. 4.1. The source terminal is connected directly to  $V_{DD}$ , so



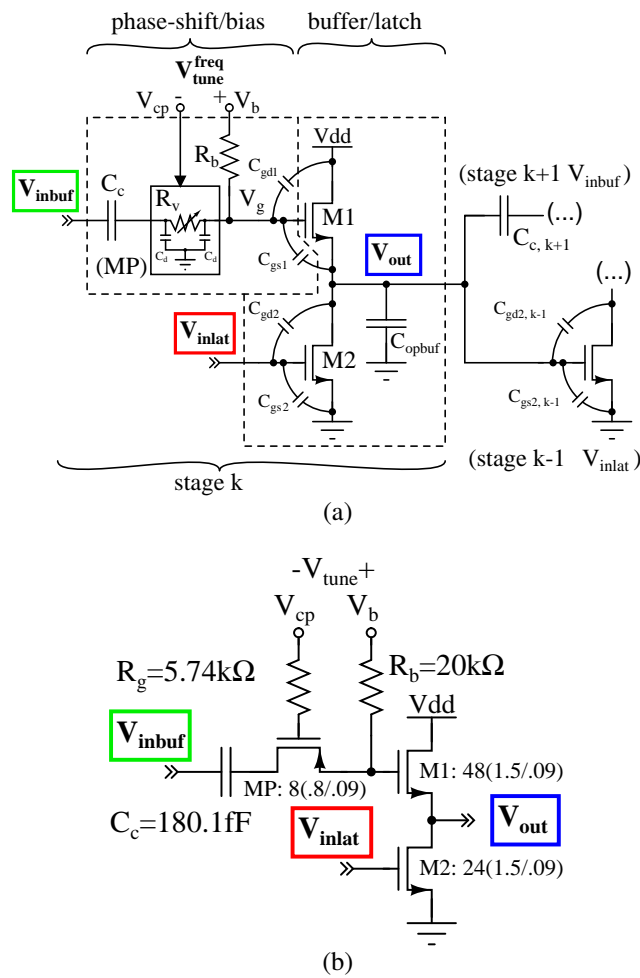
**Figure 4.1.:** Conventional CMOS-Delay-Cell Quadrature Oscillator [10, 78]

the conventional structure offers no intrinsic isolation of the supply, and its static supply sensitivity  $\frac{V_{DD}}{f_{osc}} \frac{\partial f_{osc}}{\partial V_{DD}}$  is nearly unity. To enhance the intrinsic delay-cell supply isolation, we replace the PMOS transistors with an NMOS source follower so that its saturation drain-source resistance ( $r_{ds}$ ) provides supply isolation, as shown in Fig. 4.2. The primary source-follower path (input  $V_{inbuf}$  through transistor M1) provides supply isolation, while an inverting-latch secondary path (input  $V_{inlat}$  through transistor M2) intuitively provides the voltage gain necessary to sustain the oscillation, forcing complementary nodes to be  $180^\circ$  out of phase. Use of this multi-loop architecture enables the source-follower structure to sustain oscillation and simultaneously provide supply rejection governed by transistor M1's saturation drain-source resistance. With the supply now isolated from the oscillator core, we add a phase-shift/bias network (shown conceptually as " $\Delta\phi$ " in Fig. 4.2) to bias the source follower in saturation and provide frequency tuning. Fig. 4.3(a) shows the cor-

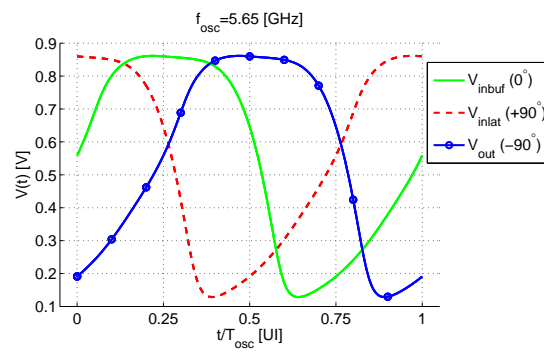


**Figure 4.2.:** Proposed Oscillator: Conceptual Block Diagram

responding circuit-level schematic of the unit delay cell. The frequency  $f_{osc}$  is controlled by the phase-shift/bias network; adjusting differential tuning voltage  $V_{tune}^{freq} = V_b - V_{cp}$  changes variable resistor  $R_v$ , which is implemented by a PMOS transistor MP in triode, as shown in Fig. 4.3(a) and (b). The capacitance  $C_{opbuf}$  is the capacitance of the output buffer to drive 50-ohm equipment;  $C_{c,k+1}$  is the AC coupling capacitance to the next buffer stage in the primary loop, and  $C_{gd/s2,k-1}$  are the gate capacitances of the  $180^\circ$  coupling latch. We arrange four buffer cells in a ring to establish a quadrature oscillator through symmetry. Fig. 4.4 demonstrates typical waveforms at the three delay-cell nodes  $V_{inbuf}$ ,  $V_{inlat}$ , and  $V_{out}$  to illustrate the relative phases (quadrature/etc.) from transistor-level SPECTRE simulation. To analyze the multiloop structure, we propose a generalized delay-cell viewpoint along with a unified phase-noise-analysis framework, which are presented in the next two sections. The circuit-level design, analysis, and measurement of this proposed MRO architecture is subsequently presented as a case study in Section 7.



**Figure 4.3.:** Unit Cell of Proposed Quadrature Oscillator: (a) Circuit Implementation with Parasitics, and Fig. 4.3(b) Component Values

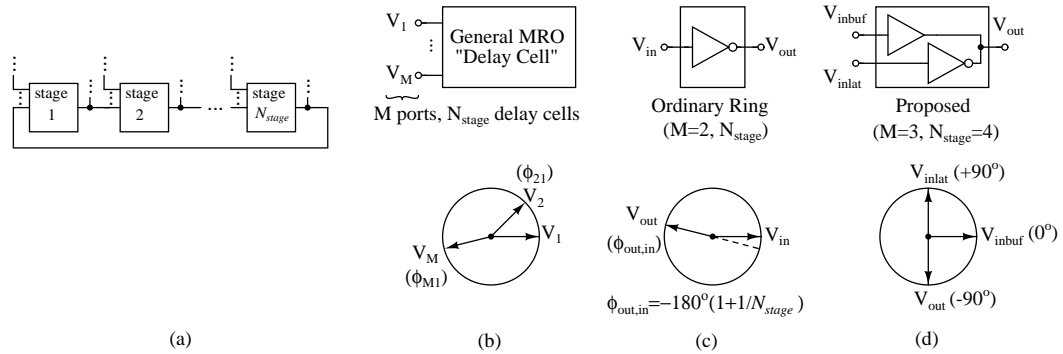


**Figure 4.4.:** Proposed Oscillator: Typical Waveforms of Delay Cell showing phase relationship

## 5. FRAMEWORKS FOR MRO DESIGN/ANALYSIS

### 5.1 Generalized Delay-Cell Viewpoint

To analyze the oscillator frequency tuning and steady-state response, we view the multiloop oscillator as a generalized  $N_{stage}$  oscillator illustrated in Fig. 5.1. Fig. 5.1(a) shows a ring of  $N_{stage}$  unit delay cells, and Fig. 5.1(b) indicates the general case for an MRO with  $M$  ports, where the number of ports  $M$  and the number of stages  $N_{stage}$  do not necessarily have any relation to each other ( $M \neq N_{stage}$ ). The number of stages and the relative connections of the ports determines the phase relationships among the ports, shown conceptually in the phasor diagram in Fig. 5.1(b). For instance, for 1 input and 1 output ( $M=2$ ), Fig. 5.1(c) shows the delay cell for a single-loop oscillator; assuming inverting delay cells and odd  $N_{stage}$ , the single-loop case has  $\phi_{out} = \phi_{in} - 180^\circ (1 + 1/N_{stage})$ , as shown in the phasor diagram in Fig. 5.1(c). For our oscillator, the latches force  $180^\circ$  between the differential nodes  $V_I/V_{IB}$  and  $V_Q/V_{QB}$  in Fig. 4.2 to avoid the DC latching condition. The phase shift through the primary path and the symmetry of the structure hence cause  $90^\circ$  lag between each successive stage, as illustrated in the phasor diagram in Fig. 5.1(d).



**Figure 5.1.:** Proposed Viewpoint of Multi-Loop Oscillator with  $M$ -Port Generalized Delay Cells and Phase Relationship among Ports (a) Ring Structure, (b) General Delay Cell, (c) Special Case: Single-Loop Ring Oscillator, (d) Special Case: Proposed Oscillator

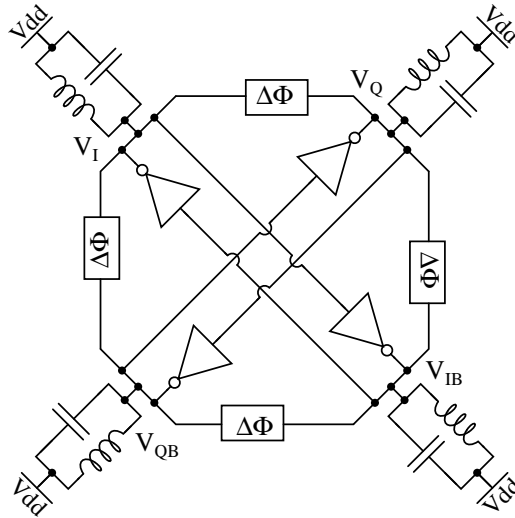
Further exploiting symmetry, the waveform at each node has the same shape even if it has harmonic content, as seen previously in Fig. 4.4 (see also [81]). Hence, denoting the oscillator periodic waveform as  $v_p(t)$  with period  $T_{osc}$ , one unit cell of our oscillator has the following phase relationships:

$$\begin{aligned} V_{inbuf}(t) &= v_p(t) && \equiv V_I(t) \\ V_{inlat}(t) &= v_p(t + T_{osc}/4) && \equiv V_{QB}(t) \\ V_{out}(t) &= v_p(t - T_{osc}/4) && \equiv V_Q(t) \end{aligned} \tag{5.1}$$

Other unit cells have analogous phase relationships. Identifying these relationships allows us to focus design, analysis, and layout efforts on a single delay cell as we shall show with a design case-study example in Section 7. In addition, as Mirzaei et al. noted [81], when configuring a ring oscillator with auxilliary injection paths to operate as an injection-locked frequency divider (ILFD), the relative phases among stages also play a crucial role in determining the locking/divide range. More specifically, Mirzaei demonstrates that, to maximize locking range, signals injected into adjacent stages should possess the same relative-phase progressions as those of the ring oscillator itself [81]. Furthermore, LC-quadrature oscillators' phase-noise levels and sensitivity to component mismatch depend on the phase shift between the injected coupling current and the main oscillator signal [128].

We also note that LC quadrature oscillators could be viewed as “ring” oscillators of sorts except that they contain resonant-tank circuits, which filter noise at the expense of IC area. Indeed, given sufficient area, one could also form a ring of resonant oscillators coupled together by phase-shift networks, such as that shown conceptually in [129]. Fig. 5.2 illustrates one such configuration where two differential LC oscillators are coupled together by phase-shift networks, and we have represented the cross-coupled negative-gm cells as back-to-back inverters to emphasize the analogy with ring oscillators [128, 130]. In our proposed multi-loop ring oscillator, the phase-shift network provides frequency





**Figure 5.2.:** Illustration of “Ring” of LC Oscillators Coupled by Phase-Shift Networks

tuning. On the other hand, in quadrature LC oscillators, the phase shift is ideally adjusted to 90 degrees to improve phase-noise performance and to reduce sensitivity to component mismatch [128], as the LC oscillator’s frequency is primarily determined by the resonant tank.

## 5.2 Phase-Noise Analysis

### 5.2.1 Background

The earliest work on oscillator noise assumed slowly varying amplitude/phase fluctuations in the form of a complex envelope and solved averaged differential equations (following Balthazar van der Pol’s at the time recent compendium of nonlinear oscillator theory [28]) to recover the amplitude/phase from the [nonlinear] voltage/current equations [31, 34, 40, 45, 55, 131–149] [150]. These methods fall into the “Fokker-Planck-Equation (FPE)” and “Modulation-Method” analysis categories of Sections 6.1.6 and 6.1.2, respectively.

Later treatments focused on Leeson’s analogy of phase noise to phase-modulation (PM) voltage-spectrum sidebands, attempting to apply conventional small-signal noise analysis despite the large-signal oscillation amplitude [60–62, 151–163]. While high-Q resonant oscillators yielded reasonable results, this linear, time-invariant (LTI) approach not only proves numerically inaccurate for ring/relaxation oscillators, but also can provide qualitatively incorrect trends/design intuition, as we shall see in Section 6.1.3. Modifying the approach to include linear periodically time varying (LPTV) effects can yield more accurate results [56, 164–174] (see LTI/LPTV “Mixer-Conversion-Gain” method in Section 6.1.1).

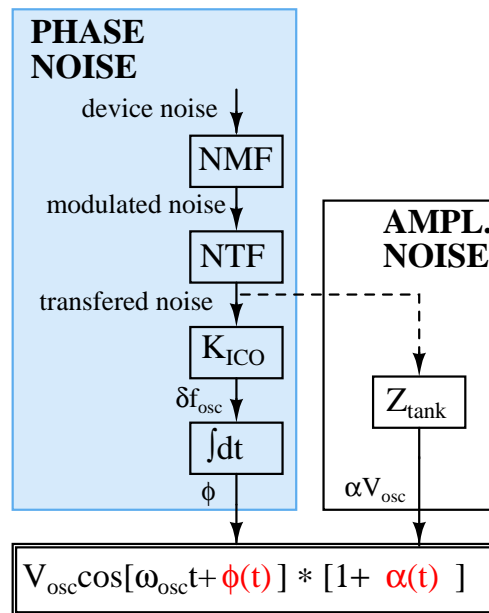
Various more rigorous techniques more oriented towards computer-aided design (CAD) either solve nonlinear stochastic differential equations (SDEs) [26, 30, 35, 41, 43, 46–48, 63, 64, 150, 175–188] (the FPE method) or determine the sensitivity of the oscillator phase to noise at different times during the oscillation cycle [44, 58, 69, 71–73, 107, 113–115, 130, 189–198] (the “Phase-Sensitivity Method” in Section 6.1.5). Such methods can predict the phase noise quite accurately, even for hard-switching ring oscillators, but involve complicated mathematics and can be difficult for the practicing engineer to use for circuit analysis or to obtain tractable, closed-form analytical expressions suitable for design intuition or trade-off analysis. To remedy this difficulty, we analyze simple, practical circuits with the techniques and relate the mathematics to physical circuit parameters.

A final class of analysis geared specifically to ring/relaxation oscillators can provide simple yet accurate phase-noise expressions and design recipes for certain ring-oscillator configurations (the Jitter [24, 36, 39, 199–215] and Direct ICO [21, 51, 216–220] methods of Sections 6.1.3 and 6.1.4).

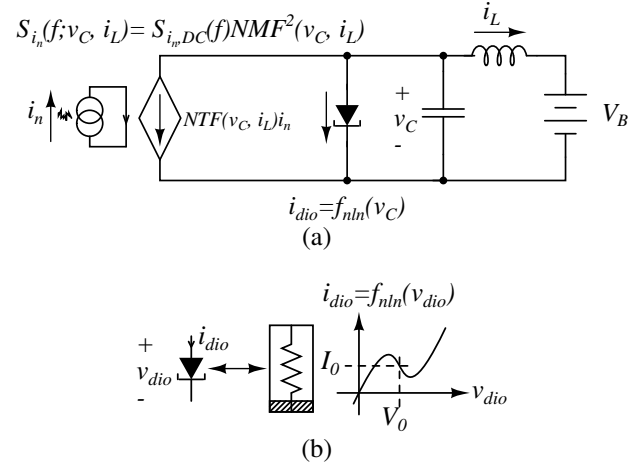
### 5.2.2 Unified Flow

Despite these multifarious, ostensibly different procedures, phase-noise analysis of an oscillator at its heart is identifying (i) a current-controlled oscillator gain ( $K_{ICO}$ ),

(ii) device-noise modulation functions (NMFs), and (iii) device-noise transfer functions (NTFs), as conceptually illustrated in Fig. 5.3. Fig. 5.4 shows a Gunn-diode LC oscillator as a concrete example of the flowchart’s block diagram. Device noise is referred to an “output node” (more accurately to the state variables) through a noise transfer function  $NTF = i_{tank}/i_n$  (loosely), where  $i_{tank}$  denotes the noise entering the “output node” (e.g.  $v_C$  in Fig. 5.4(a)). The effect of periodically-changing bias conditions on noise statistics (viz. spectrum  $S_{in}(f; v_C, i_L)$ ) is included in the noise-modulation function NMF. The sensitivity of the oscillator frequency/phase to the noise at the “output node” can be interpreted as a VCO/ICO gain ( $K_{ICO}$ ), which is generally time varying. The different analysis techniques mentioned in Section 5.2.1 fit into this general paradigm; however, some of the simplified methods neglect various aspects—for instance, applying typical noise analysis to oscillators is tantamount to neglecting noise modulation and assuming that the NTF and  $K_{ICO}$  blocks are ordinary time-invariant linear filters (cf. Section 6.1.1; “mixer conversion-gain method/LTI”).



**Figure 5.3.:** Conceptual VCO/ICO Viewpoint of Oscillator-Phase-Noise Computation



**Figure 5.4.:** (a) Gunn-Diode Oscillator to Illustrate Overall PN-Analysis Flow, (b) Example Nonlinear Current Relationship

Based on the block diagram in Fig. 5.3, we outline the following framework to find  $S_\phi$  common to all the different analysis techniques of Section 6. Section 6.1 will then discuss each technique separately but will follow these steps.

1. **Periodic Steady State (PSS):** Find the PSS response, most importantly the [fundamental] amplitude  $V_{osc}$  and frequency  $f_{osc}$  of oscillation, both of which are necessary to compute phase noise—this step is common to all the phase-noise analysis procedures in Section 6.1. Two common approaches to find the PSS include Harmonic Balance (HB) and Hard Switching approximations (as previously discussed in Section 2.3).
2. **Perturbation Model:** Choose a perturbation model that describes how the device noise turns into amplitude/phase errors from the ideal PSS waveforms. This step is specific to each technique in Section 6.1.

3. **Noise Modulation Function (NMF):** Account for the effect of [periodically] varying device bias points on noise statistics (“cyclostationarity”)<sup>1</sup>:

(a) Given that a device has stationary noise with spectrum  $S(f; \vec{V}_{bias})$  for constant  $\vec{V}_{bias}$ , its noise is cyclostationary when  $\vec{V}_{bias}(t)$  is periodic.

(b) The noise modulation function (NMF) is given by [133, 164, 182]

$$NMF(2\pi f_{osc}t) \equiv \sqrt{\frac{S(f; \vec{V}_{bias}(2\pi f_{osc}t))}{\max S(f; \vec{V}_{bias})}} \quad (5.2)$$

For example, given a diode with stationary, white shot-noise PSD  $S_i(f) = 2qI_S(e^{V/\phi_t} - 1)$ ,  $V(t) = V_0 + V_{osc} \cos(2\pi f_{osc}t)$ , and

$$NMF(\theta) = \sqrt{\frac{e^{[V_0 + V_{osc} \cos(\theta)]/\phi_t} - 1}{e^{[V_0 + V_{osc}]/\phi_t} - 1}}.$$

4. **Noise Transfer Function (NTF):** Refer device noise to the oscillator “output” (or state variables).

5. **Current-Controlled-Oscillator Gain  $K_{ICO}$ :** Extract the equivalent ICO gain based on a given technique’s approximation for phase—this can be done either in the frequency domain or in the time domain.

6. **Spectrum:** To obtain the spectrum  $S_\phi$  for  $\phi(t)$ , either substitute parameter values into a known form of the spectrum, most commonly  $S_\phi(f_m) = \kappa^2 \left(\frac{f_{osc}}{f_m}\right)^2$ , or use  $S_\phi(f) = \mathcal{F}_{\tau \rightarrow f} [\overline{R}_\phi(\tau)]$ .

The following section presents the principal results of each phase-noise-analysis technique discussed in Section 5.2.1 and works through a practical example in each case to illustrate how to apply these methods to design/analysis.

<sup>1</sup>The noisy free-running oscillator is not truly periodic, but cyclostationary analysis captures the effect of changing bias point/mixing action on noise statistics.

## 6. SYNOPSIS OF PHASE-NOISE-ANALYSIS TECHNIQUES

Each of the following subsections presents the analysis techniques of Table 6.1 by example of either the LC cross-coupled oscillator of Fig. 2.5(a) or the CMOS ring oscillator of Fig. 2.6(a), as some of the techniques are better suited to one or the other. We assume the same numerical component values as previously listed in Table 2.1. For reference, Appendix B also enumerates how to generalize all these procedure to other oscillators. Finally, Section 6.2 compares the methods to one another and provides a selection guide of when each analysis method is most accurate or useful. Numerical values for all these techniques using the component values in Table 2.1 are summarized and compared in Section 6.2.3.

### 6.1 Specific Phase-Noise-Analysis Methods

#### 6.1.1 Mixer Conversion-Gain Method

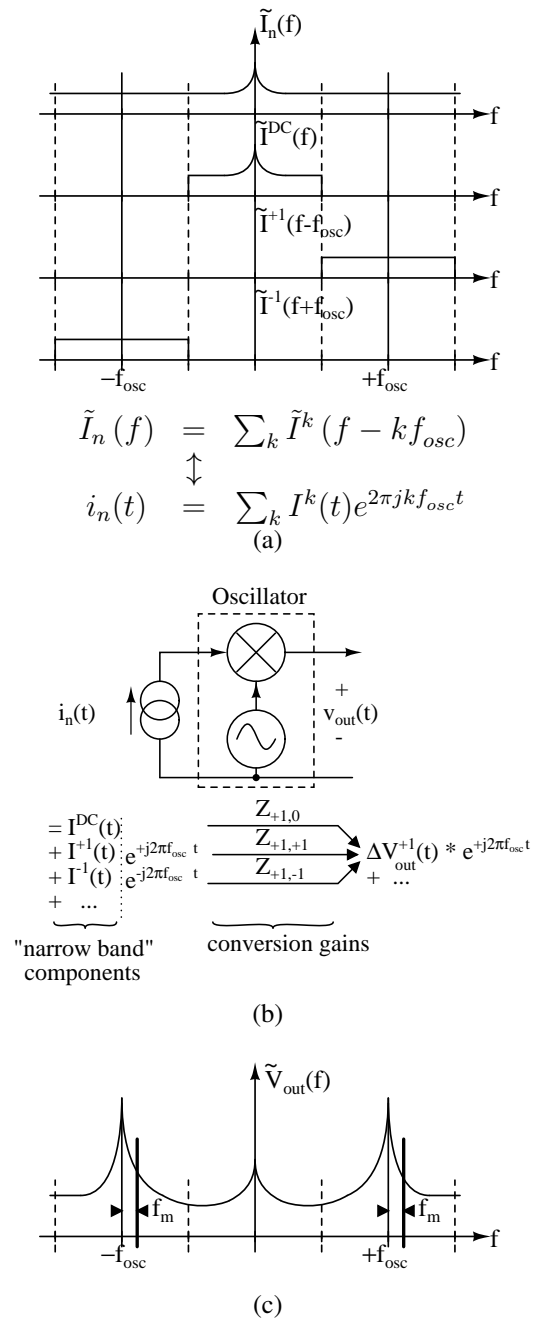
##### Description

The mixer conversion-gain method treats noise  $i_n(t)$  as a sum of narrow-band modulated sinusoids at harmonics of the carrier frequency [221] as shown in Fig. 6.1(a). We denote the spectrum of each equivalent narrowband noise process about the  $k^{th}$  harmonic as  $I^k(f)$ . These noise sources are considered as parasitic “RF” inputs to a mixing network driven by the oscillator’s own large-signal switching action, as illustrated in Fig. 6.1(b). In this fashion, we view the oscillator as a self-oscillating mixer, and the noise sources experience “conversion gains”  $Z_{1,k}$  from around the  $k^{th}$  harmonic to the fundamental at the oscillator “output node” as shown in Fig. 6.1(b). The frequency-shifted noise then appears at the oscillator output as depicted in Fig. 6.1(c).

**Table 6.1:** Phase-Noise-Analysis Categories

Section	Method	Complexity*	Brief Reference List
6.1.1	Conversion	1	[60–62, 151–163]
6.1.2	Modulation	3-5	[31, 34, 40, 45, 55, 131–149]
6.1.3	Jitter	2	[24, 36, 39, 199–215]
6.1.4	Direct-KICO	2	[21, 51, 216–220]
6.1.5	Phase-Sensitivity	4	[44, 58, 69, 71–73, 107, 113–115, 130, 189–198]
6.1.6	Fokker-Planck Equation	5	[26, 30, 35, 41, 43, 46–48, 63, 64, 150, 175–188]

\* 1=least, 5=most complex



**Figure 6.1:** Mixer Conversion-Gain Method: (b) Conceptual Illustration, (a) Broadband noise as sum of narrowband components, (c) Corresponding Output-Voltage



Using the “RHS” offset  $\pm f_{osc} + f_m$  as highlighted in Fig. 6.1(c), we decompose the overall voltage  $\tilde{V}_{out}$  into phase/amplitude-modulation (PM/AM) sidebands [155]. First consider the (more important) PM sidebands; assuming small  $\phi_{pk} \ll 1$ ,

$$\begin{aligned} V_{out}^{PM} &= V_{osc} \cos(2\pi f_{osc} t - \phi_{pk} \sin(2\pi f_m t)) \\ &\approx V_{osc} [\cos(2\pi f_{osc} t) + \phi_{pk} \sin(2\pi f_m t) \sin(2\pi f_{osc} t)] \\ &= \frac{V_{osc}}{2} [e^{2\pi j f_{osc} t} - \frac{\phi_{pk}}{2} (e^{2\pi j [f_{osc} + f_m] t} - e^{2\pi j [-f_{osc} + f_m] t}) + \mathbb{C}^*] \end{aligned} \quad (6.1)$$

where  $\mathbb{C}^*$  denotes corresponding complex-conjugate terms. Likewise, it can be shown that AM sidebands take the form

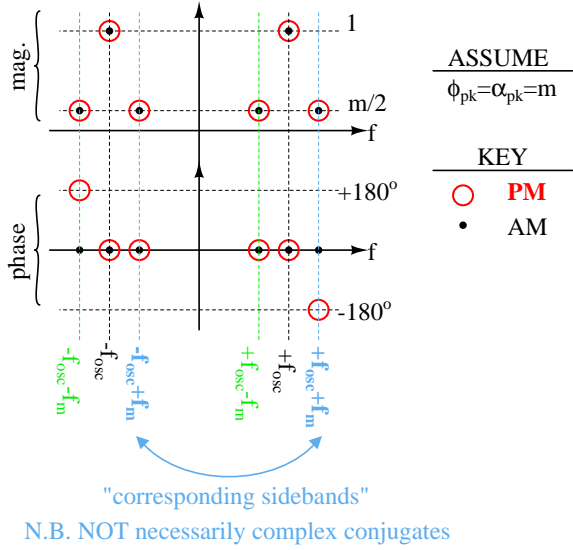
$$V_{out}^{AM} = \frac{V_{osc}}{2} [e^{2\pi j f_{osc} t} + \frac{a_{pk}}{2} (e^{2\pi j [f_{osc} + f_m] t} + e^{2\pi j [-f_{osc} + f_m] t}) + \mathbb{C}^*] \quad (6.2)$$

Thus, we see that by subtracting the complex amplitudes of the  $+f_{osc} + f_m$  component of the output voltage  $\tilde{V}_{out}$  from that of the  $-f_{osc} + f_m$  component<sup>1</sup>, we extract the PM sideband component while nulling the AM sideband component. The Fourier-series plot of Fig. 6.2(a) illustrates these relations for the special case of  $\phi_{pk} = a_{pk} = m$ . One can also visualize the PM/AM sidebands as a phasor sum with “counter-rotating” modulation phasors as illustrated in Fig. 6.2(b). Note that the PM phasors add to produce a component in quadrature with the main carrier phasor (corresponding to  $\phi$  being multiplied by  $\sin(2\pi f_{osc} t)$  while the carrier is  $\cos(2\pi f_{osc} t)$  in (6.1))<sup>2</sup>.

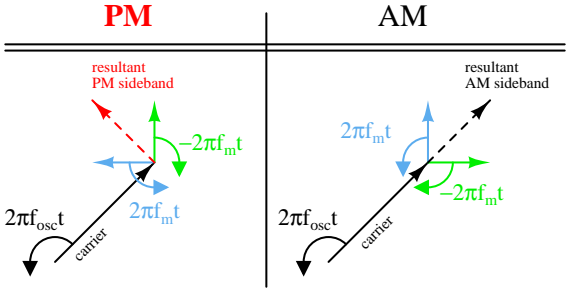
Two “flavors” of conversion analysis exist, depending on whether one employs a linear time-invariant (LTI) model [60–62, 151–163], or a linear periodically time varying (LPTV) model [56, 164–174]. LPTV hand analysis with a single harmonic is sometimes called the “phasor method,” and CAD approaches using multiple harmonics are commonly termed “conversion analysis” (cf. Section 6.1.2: “modulation analysis”).

<sup>1</sup>Note that we single out  $\pm f_{osc} + f_m$  and not  $+f_{osc} \pm f_m$ .

<sup>2</sup>Note that pure phase modulation with no accompanying amplitude modulation would require an infinite number of sidebands at  $\pm f_{osc} \pm k f_m$ ,  $k \in \mathbb{Z}$  (sideband magnitudes given by Bessel functions [155]); however, for small  $\phi_{pk}$ , we can consider only  $\pm f_{osc} \pm f_m$ .



(a)



(b)

**Figure 6.2.:** Phase/Amplitude Modulation: (a) Fourier-Series Mag./Phase, (b) “Rotating Phasor” Illustration

Procedure/Example

1. **Perturbation Model:** We choose the capacitor voltage  $v_{C1}$  of Fig. 2.5(a) as our “output,” and for simplicity consider the “half circuit” of Fig. 2.5(c). Model the effect of noise currents as *additive* voltage noise on top of large harmonics at fixed frequencies:

$$v_{C1}(t) = \left[ \frac{V_{osc}}{2} + \Delta V_{C1}^{+1}(t) \right] e^{j2\pi f_{osc}t} + \left[ \frac{V_{osc}}{2} + \Delta V_{C1}^{-1}(t) \right] e^{-j2\pi f_{osc}t} \quad (6.3)$$

where we assume  $\Delta V_{C1}^{\pm 1}(t)$  is much smaller than the fundamental and slowly varying with respect to the fundamental frequency, allowing the narrowband decomposition illustrated in Fig. 6.1(a). Hence, for each of the noise sources, the circuit is described by

$$\vec{V}(f_m) = \begin{pmatrix} V^{-2}(f_m) \\ V^{-1}(f_m) \\ V^{+0}(f_m) \\ V^{+1}(f_m) \\ V^{+2}(f_m) \end{pmatrix} = \underline{Z}(f_m) \underline{NTF}_n \vec{I}_n \quad (6.4)$$

where  $V^k(f_m)$  is the narrow-band voltage perturbation about the  $k^{th}$  harmonic, and  $\vec{I}_n$  has a similar decomposition.  $\underline{NTF}$  is determined in a later step, and  $\underline{Z}(f_m)$  is a matrix of conversion-gain impedances:  $Z_{k,j}(f_m)$  denotes the conversion-gain impedance mixing the output-node current around the  $j^{th}$  harmonic to the  $k^{th}$  har-

monic of the output-voltage<sup>3</sup> perturbation as illustrated in Fig. 6.1(b). For LPTV analysis, linearize the circuit about the ‘‘PSS’’ operating point  $V_o(t) = V_{osc} \cos(2\pi f_{osc} t)$ :

$$\begin{aligned}
 g(t) &= \left. \frac{\partial I_1}{\partial v_{C1}} \right|_{PSS} \\
 &= - \underbrace{\left( g_1 - \frac{2}{R_p} \right)}_{g'_1} + \frac{3g_3}{2} V_{osc}^2 (1 + \cos(2[2\pi f_{osc} t])) \\
 &= \left( g_1 - \frac{2}{R_p} \right) [1 + 2 \cos(2\theta)]
 \end{aligned} \tag{6.5}$$

where we use  $V_{osc}^2 \approx 4(g_1 - 2/R_p)/(3g_3)$  to simplify expressions.  $\underline{Z}$  for LPTV analysis is given by

$$\underline{Z}(f_m) \approx \begin{pmatrix} -2jG_0 & 0 & g'_1 & 0 & 0 \\ 0 & g'_1 + 2jG_0 \frac{f_m}{f_{osc}} & 0 & g'_1 & 0 \\ g'_1 & 0 & -jG_0 \frac{f_{osc}}{f_m} & 0 & g'_1 \\ 0 & g'_1 & 0 & g'_1 + 2jG_0 \frac{f_m}{f_{osc}} & 0 \\ 0 & 0 & g'_1 & 0 & 2jG_0 \end{pmatrix}^{-1} \tag{6.6}$$

$$\Rightarrow Z_{\pm 1,0} = 0, Z_{\pm 1,\pm 2} = 0, (Z_{1,\pm 1} - Z_{-1,\pm 1}) \approx \frac{\pm f_{osc}}{2j f_m G_0} \tag{6.7}$$

For LTI analysis, we perform the same except about a DC operating point and consider only  $Z_{k,k}(f_m)$  for  $k = \pm 1$ , which is the tank impedance evaluated at  $f = \pm f_{osc} + f_m$ .

2. **NMF:** For each noise source, we apply definition (5.2) from Section 5.2.2. In LTI analysis,  $NMF = 1$  because the bias point is constant; the results for LPTV are summarized in Table 6.2(a) for the LC NMOS oscillator.<sup>4</sup>

<sup>3</sup>N.B. Phase noise should not depend upon the node at which it is measured [43, 44]); however, because the conversion method infers phase noise from PM voltage-noise sidebands, there could be some small dependence.

<sup>4</sup>cf. slightly different technique in [24, 170, 174].

3. **NTF:** To obtain the noise-transfer functions, we use the intuition that the differential action of the tank is most significant—hence, we seek  $NTF_k = \frac{i_d=i_1-i_2}{i_{noise,k}}$ , where  $i_{1,2}$  indicate the small-signal versions of  $I_{1,2}$ . For instance,

$$\begin{aligned} A_i(\theta) &\equiv \left. \frac{\partial(I_1-I_2)}{\partial i_{ntail}} \right|_{\text{operating point}} = \frac{i_1-i_2}{i_{ntail}} \\ &= -\frac{1-\frac{g_{m2}(\theta)}{g_{m1}(\theta)}}{1+\frac{g_{m2}(\theta)}{g_{m1}(\theta)}} = \begin{cases} 0 & , \text{ LTI} \\ \approx -\frac{V_{osc}}{\sqrt{I_{tail}/K}} \cos(\theta) & , \text{ LPTV} \end{cases} \end{aligned} \quad (6.8)$$

and  $g_{m1,2}$  are given in (2.11). Table 6.2(a) summarizes the NTFs for the LC NMOS oscillator for both the LTI and LPTV cases. Note that for LTI analysis, we evaluate the NTF about the DC operating point  $V_{C1,2} = 0$ , whereas for LPTV, we evaluate at the periodic steady-state  $V_{C1,2} = \pm V_{osc} \cos(\theta)$ .

4.  $K_{ICO}$ : Subtracting the noise around  $f_{osc} + f_m$  from that around  $-f_{osc} + f_m$  to extract the PM sideband as indicated in (6.1), we obtain  $K_{ICO}$ :

$$\vec{K}_{ICO} = \frac{2\pi j f_m}{2V_{osc}} \begin{pmatrix} Z_{1,-2}(f_m) - Z_{-1,-2}(f_m) \\ Z_{1,-1}(f_m) - Z_{-1,-1}(f_m) \\ Z_{1,0}(f_m) - Z_{-1,0}(f_m) \\ Z_{1,1}(f_m) - Z_{-1,1}(f_m) \\ Z_{1,2}(f_m) - Z_{-1,2}(f_m) \end{pmatrix} \quad (6.9)$$

where we use  $2V_{osc}$  because we computed the NTFs for the differential tank. N.B. we normalize w.r.t. peak fundamental oscillation amplitude  $V_{osc}$  and not the RMS value because the PM sideband approximation normalizes to the peak sinusoid component in (6.1). For LTI,  $Z_{k,j} = 0$  unless  $k = j$ , i.e. no conversion among frequencies:

$$\vec{K}_{ICO}^\dagger \approx \frac{-2\pi j f_m}{2V_{osc}} \frac{1}{-g_1' + j2\frac{f_m}{f_{osc}} G_0} [0, 1, 0, -1, 0] \quad (6.10)$$

**Table 6.2:** Conversion-Method (a) NTFs & NMFs, and (b) Fourier-Series Coefficients

(a)

noise	$NTF^\dagger$	$NMF_{LPTV}$
$R_{p1,2}$	$\mp 1$	1
switch1,2	$\mp 1 - A_i(\theta)$	$\sqrt{\frac{gm_{1,2}(\theta)}{g_{max}}} \approx \sqrt{\frac{1 \pm \frac{V_{osc}}{\sqrt{I_{tail}/K}} \cos(\theta)}{1 + \frac{V_{osc}}{\sqrt{I_{tail}/K}}}}$
tail	$-A_i(\theta)$	1

†  $A_i$  defined in (6.8)

(b)

$k$	0	$\pm 1$	$\pm\{2, 3, 4\}$
$T_{sw1}^k$	-1	$\frac{1}{2} \frac{V_{osc}}{\sqrt{I_{tail}/K}}$	$\approx 0$
$M_{sw1}^k$	$\frac{1}{\sqrt{1 + \frac{V_{osc}}{\sqrt{I_{tail}/K}}}}$	$\frac{1}{4} \frac{V_{osc}}{\sqrt{I_{tail}/K}} \frac{1}{\sqrt{1 + \frac{V_{osc}}{\sqrt{I_{tail}/K}}}}$	$\approx 0$
$T_{tail}^k$	0	$\frac{1}{2} \frac{V_{osc}}{\sqrt{I_{tail}/K}}$	$\approx 0$
$M_{tail}^k$	1	0	0

$NTF(\theta) = \sum_{k=-\infty}^{+\infty} T^k e^{jk\theta}, \quad NMF(\theta) = \sum_{k=-\infty}^{+\infty} M^k e^{jk\theta}$

where  $G_0 \equiv 2\sqrt{\frac{C}{L}}$  corresponds to the characteristic conductance of each tank. For the LPTV case, substituting expressions from (6.7), we obtain:

$$\vec{K}_{ICO}^\dagger \approx \frac{2\pi j f_m}{2V_{osc}} \frac{f_{osc}}{2j f_m G_0} [0, 1, 0, -1, 0] \quad (6.11)$$

### 5. Spectrum: For each noise source

$$S_\phi(f_m) = \frac{1}{(2\pi f_m)^2} \vec{K}_{ICO}^\dagger(f_m) \times \underline{NTF} \times \underline{NMF} \times \underline{S}(f_m) \times \underline{NMF}^\dagger \times \underline{NTF}^\dagger \times \vec{K}_{ICO}(f_m) \quad (6.12)$$

where  $\underline{NTF}$  and  $\underline{NMF}$  are matrices with the NTF/NMF Fourier coefficients from Table 6.2(b) arranged in a so-called ‘‘Toeplitz Conversion Matrix’’ (TCM) pattern [164], i.e.

$$\underline{TCM} = \begin{pmatrix} C^{+0} & C^{-1} & C^{-2} & C^{-3} & C^{-4} \\ C^{+1} & C^{+0} & C^{-1} & C^{-2} & C^{-3} \\ C^{+2} & C^{+1} & C^{+0} & C^{-1} & C^{-2} \\ C^{+3} & C^{+2} & C^{+1} & C^{+0} & C^{-1} \\ C^{+4} & C^{+3} & C^{+2} & C^{+1} & C^{+0} \end{pmatrix} \quad (6.13)$$

and  $C^k$  could denote either  $T^k$  or  $M^k$  for  $\underline{NTF}$  or  $\underline{NMF}$ , respectively. The LTI and LPTV expressions are hence

$$S_\phi^{LTI}(f_m) = \frac{1}{(g_1')^2 + \left(2G_o \frac{f_m}{f_{osc}}\right)^2} \frac{4k_B T}{V_{osc}^2} \left( \frac{1}{R_p} + \frac{\gamma}{2} \sqrt{KI_{tail}} \right) \quad (6.14)$$

$$S_\phi^{LPTV}(f_m) \approx \frac{k_B T}{\left(G_o V_{osc} \frac{f_m}{f_{osc}}\right)^2} \left( \frac{1}{R_p} + \frac{\gamma \sqrt{KI_{tail}}}{2} \left[ 1 - \frac{1}{96} \left( \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right)^2 + \frac{1}{64} \left( \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right)^4 \right] + \gamma g_{d0}^{tail} \left[ \frac{1}{4} \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right]^2 \right) \quad (6.15)$$

We see that LPTV method captures additional amplitude ( $V_{osc}$ ) dependence and includes tail-current noise, which LTI analysis could not. We also see the true  $f_m^{-2}$  close-in behavior.<sup>5</sup>

### 6.1.2 Modulation Method

#### Description

The modulation method [31, 34, 40, 45, 55, 131–149] assumes solutions of the form  $[V_0 + \Delta V(t)] \cos [2\pi f_{osc}t + \phi(t)]$  where  $\Delta V$ ,  $\phi$  are slowly varying with respect to the oscillation frequency. This slowly-varying assumption facilitates extraction of the amplitude/phase equations by averaging over one cycle. As Mirzaei et al. observed [31, 128], this analysis closely parallels that of Robert Adler in injection-locked oscillators [32]. Moreover, Mirzaei’s generalization of Adler’s equation to large-signal injection facilitates application of the modulation method to evaluate mode stability, as demonstrated for quadrature LC oscillators [128]. This technique has since been extended to CAD harmonic-balance noise analysis [35, 133], and this HB formulation can also obtain the *voltage* spectrum  $S_{v_C}(f)$  for close-in phase noise [51, 149].

#### Procedure/Example

1. **Perturbation Model:** Consider the half circuit of Fig. 2.5(c). For simplicity, consider only tank-resistor noise, and convert to an equivalent differential tank:

$$v_C(t) \equiv v_{C1} - v_{C2} = (2V_{osc} + \Delta V_C(t)) \cos(2\pi f_{osc}t + \phi(t)) \quad (6.16)$$

<sup>5</sup>Some formulations of conversion analysis [164] arbitrarily set the imaginary part of one harmonic to zero. In large-signal analysis, this is necessary to solve for the solution uniquely, because the circuit is autonomous. However, this phase ambiguity is what allows phase-noise to accumulate [35]—hence arbitrarily setting the imaginary part to zero removes the singularity at  $f_m = 0$ , which could make conversion analysis less accurate for close-in phase noise. Thus, in our analysis above, we preserve the singularity at  $f_m = 0$ .



where  $\Delta V_C$ ,  $\phi$  are slowly varying with respect to the oscillation frequency  $f_{osc}$ , and  $V_{osc}$  denotes the *single-ended* oscillation peak amplitude as derived in Section 2.3.

2. **NMF and NTF:** For the tank resistor,  $NMF = 1$  because it is bias independent, and  $NTF = 1$  as derived in Section 6.1.1.
3. “ $K_{ICO}$ ” To extract the phase/amplitude equations, consider the differential equation describing the oscillator:

$$\frac{dv_C}{dt} + \frac{v_C/R_p - I_1(v_C/2) + i_{nR}(t)}{C} + (2\pi f_{osc})^2 \int_{t_0}^t d\tau \{v_C(\tau)\} = 0 \quad (6.17)$$

- (a) Because the amplitude/phase perturbations vary slowly, we can approximate the capacitor and inductor currents [34] as follows by integrating by parts:

$$\begin{aligned} & \frac{dv_C(t)}{dt} \\ &= -2\pi f_{osc} [2V_{osc} + \Delta V_C(t)] \left[ 1 + \frac{1}{2\pi f_{osc}} \frac{d\phi(t)}{dt} \right] \sin(2\pi f_{osc} t + \phi(t)) \\ & \quad + \frac{d\Delta V_C}{dt} \cos(2\pi f_{osc} t + \phi(t)) \\ & (2\pi f_{osc})^2 \int_{t_0}^t d\tau \{v_C(\tau)\} \\ & \approx +2\pi f_{osc} [2V_{osc} + \Delta V_C(t)] \left[ 1 - \frac{1}{2\pi f_{osc}} \frac{d\phi(t)}{dt} \right] \sin(2\pi f_{osc} t + \phi(t)) \\ & \quad + \frac{d\Delta V_C}{dt} \cos(2\pi f_{osc} t + \phi(t)) \end{aligned} \quad (6.18)$$

- (b) Substituting (6.18) into (6.17), multiplying by  $\sin(2\pi f_{osc} t + \phi(t))$ , and integrating over one period to obtain the phase expression, we have

$$\Delta\omega \equiv \frac{d\phi(t)}{dt} \approx \frac{1}{2CV_{osc}} \int_{t-T_{osc}}^t \frac{d\tau}{T_{osc}} \{i_n(\tau) \sin(2\pi f_{osc} \tau + \phi(\tau))\} \quad (6.19)$$

Mirzaei noted that by treating noise  $i_n$  as a sum of sinusoids with random phase/amplitude, the above equation becomes Adler’s equation for oscillator injection locking [31]. This nonlinear relation hence displays a parasitic frequency-control relationship from the noise.

#### 4. Spectrum:

- (a) We first show that the frequency noise is roughly white, and then integrate to obtain the phase spectrum:

$$\bar{R}_{\Delta\omega}(\tau) \equiv \lim_{T \rightarrow \infty} \int_0^T \frac{dt}{T} \{R_{\Delta\omega}(\tau, t)\} \quad (6.20)$$

where

$$\begin{aligned} R_{\Delta\omega}(t, \tau) &= \mathbb{E}[\Delta\omega(t)\Delta\omega(t+\tau)] = \\ &= \frac{1}{(2CV_{osc})^2} \int_{t-T_{osc}}^t \int_{t+\tau-T_{osc}}^{t+\tau} \frac{dx dy}{T_{osc}^2} \{ \\ &= \mathbb{E}[i_w(x)i_w(y) \sin(2\pi f_{osc}x + \phi(x)) \sin(2\pi f_{osc}y + \phi(y))]\} \end{aligned} \quad (6.21)$$

and  $i_w(t)$  represents Gaussian white noise with  $\mathbb{E}[i_w(t)i_w(t+\tau)] = 2k_B T \frac{1}{R_p} \delta(\tau)$  because we consider the equivalent differential tank for simplicity in this example.

- (b) It can be shown that by assuming  $\phi(t)$  is roughly Gaussian, the above expressions evaluate to

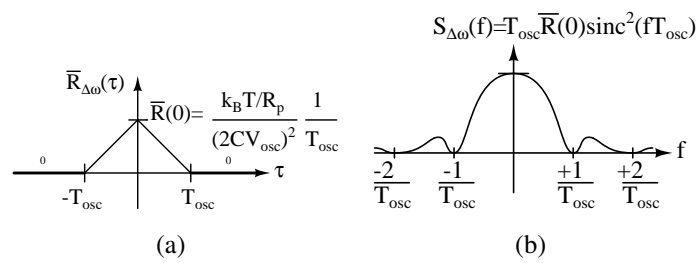
$$\bar{R}_{\Delta\omega}(\tau) = \frac{k_B T / R_p}{(2CV_{osc})^2} \frac{1}{T_{osc}} \text{tri}\left(\frac{\tau}{T_{osc}}\right) \quad (6.22)$$

where  $\text{tri}(\cdot)$  is the triangle function as shown in Fig. 6.3. Provided that

$f \ll f_{osc}$ ,  $S_{\Delta\omega}(f) \approx \text{constant}$ , and hence roughly white.

- (c) Thus, we have a spectrum

$$S_\phi(f_m) \approx S_{\Delta\omega}(0) / (2\pi f_m)^2 \quad (6.23)$$

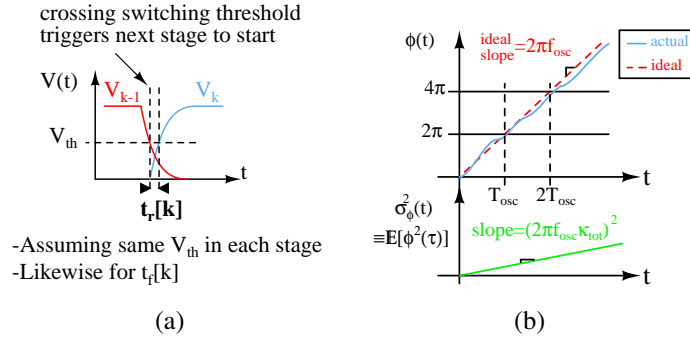


**Figure 6.3.:** Frequency-Perturbation (a) Autocorrelation and (b) Spectrum

### 6.1.3 Jitter Method

#### Description

The jitter method analyzes switching/ring/relaxation oscillators in the time domain [24, 36, 39, 199–215]. Considering only white noise sources, the phase variance of a free-running oscillator monotonically increases with time:  $\sigma_\phi^2(t) = (2\pi f_{osc} \kappa_{tot})^2 t$  for some constant  $\kappa_{tot}^2$ —the jitter method seeks this constant. This technique best applies to single-loop  $N_{stage}$  ring oscillators, such as the one in Fig. 2.6(a), where each of the (not necessarily identical) delay cells<sup>6</sup> has rise/fall times  $t_{r/f}[k]$ , respectively, and  $k = 1 \dots N_{stage}$  denotes which stage, so  $f_{osc} = [\sum_{k=1}^{N_{stage}} (t_r[k] + t_f[k])]^{-1}$ . Fig. 6.4(a) illustrates the definition of “rising/falling times” in this context. Therefore, rising-edge zero cross-



**Figure 6.4.:** Jitter Method: (a) Rising/Falling Times, (b) Phase Random Walk and Variance

ings of the  $k^{th}$  node correspond to the phase  $\phi(t)$  crossing an integer multiple of the  $2\pi + k\pi(1 + 1/N_{stage})$ .<sup>7</sup> Fig. 6.4(b) illustrates this definition of phase as the integral of instantaneous frequency and displays the variance of phase as a function of time assuming only white noise sources. N.B. the fact that the variance changes with time indicates that the phase noise is nonstationary.

<sup>6</sup>These “delay cells” could also be interpreted as different regions of operation within a single delay cell, e.g. if a transistor enters triode [215].

<sup>7</sup>The extra  $\pi$  is because each delay stage is assumed inverting.

### Procedure/Example

1. **Perturbation:** Break up the oscillation period into segments based on the ideal switching approximation. During each segment, construct an equivalent model for the switched-on part of the circuit; e.g. the simplified current and voltage waveforms for a single stage of the ring oscillator are shown in Fig. 2.6(b). The capacitor (timing) voltage waveform  $v_k(t)$  becomes  $v_k(t + t_j(t))$  with noise, where  $\mathbb{E}[t_j^2(t)] = \kappa^2 t$ .
2. **NMF:** Within a single switching interval, we find the mean-squared NMF due to changing bias point of the white-noise source by applying (5.2) as follows:

$$NMF_{rms}^2 \equiv \int_0^{t_d} \frac{g_{d0}(V_{gs})}{g_{d0,max}} \frac{dt}{t_d} = \int_0^{t_d} \frac{K \left( \frac{V_{DD}}{2} \left( 1 + \frac{t}{t_d} \right) - V_t \right)}{K(V_{DD} - V_t)} dt = \frac{\frac{3}{4}V_{DD} - V_t}{V_{DD} - V_t} \quad (6.24)$$

Hence, the accumulated timing voltage due to the noise and associated standard deviation is (assuming  $t_r = t_f = t_d$ )

$$V(t) = \int_0^{t_d} \frac{i_p(t)}{C} dt \quad (6.25)$$

where  $C \equiv 2C_{ox}WL$  is the total gate capacitance of both transistors. Thus,

$$\begin{aligned} \sigma_v^2(t_d) &\equiv \mathbb{E}[V^2(t)] = \int_0^{t_d} \int_0^{t_d} \underbrace{2k_B T \gamma g_{d0}^{eff} \delta(x-y)}_{=\mathbb{E}[i_p(x)i_p(y)]} \frac{dx dy}{C^2} \\ &= \frac{2k_B T \gamma \mu C_{ox} (3/4 V_{DD} - V_t)}{C^2} t_d \end{aligned} \quad (6.26)$$

3. **NTF:** For the ring oscillator shown, the noise currents are already referred to the timing voltage node, so  $NTF = 1$ .

4. “ $K_{ICO}$ ”–the **Jitter Slew-Rate Equation**: Approximating the slew rate right before the switching instant  $SR \approx I_{peak}/C$ , we obtain

$$\kappa^2 \equiv \frac{\sigma_v^2(t_d)}{SR^2(t_d) \times t_d} = 2 \frac{8k_B T \gamma \left(\frac{3}{4}V_{DD} - V_t\right)}{\mu C_{ox} (V_{DD} - V_t)^4} \quad (6.27)$$

where the initial factor of two is to account for the noise from both NMOS & PMOS transistors in the inverter, and  $C$ ,  $I_{peak}$  are in (2.16).

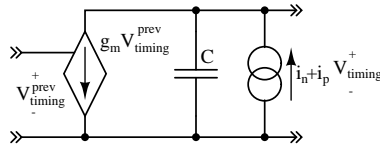
5. **Spectrum**: Substituting expressions for  $P$  from (2.17) and  $I_{peak}$  from above, we obtain

$$S_\phi(f_m) = \kappa^2 \frac{f_{osc}^2}{f_m^2} \approx \frac{4k_B T \gamma}{P} \frac{f_{osc}^2}{f_m^2} \quad (6.28)$$

Jitter-Method analysis thus correctly predicts that phase noise due to white [thermal] noise is independent of the number of stages for single-ended ring oscillators, assuming fixed power and frequency of oscillation. The analysis works because it explicitly takes into account the hard switching, time-varying nature of the oscillator.

#### CAVEAT about using LTI analysis with Ring Oscillators

To illustrate the inadequacies of the LTI method for hard-switching oscillators, model each delay stage as shown in Fig. 6.5. By symmetry of the oscillator, the effective  $K_{ICO}$



**Figure 6.5.:** Ring-Oscillator LTI Delay-Cell Model

for LTI Conversion analysis for each noise source  $k = 0, \dots, N_{stage} - 1$  is

$$K_{ICO,k}(f_m) = \frac{H^k(f_{osc} + f_m)}{1 - T(f_{osc} + f_m)} \frac{2\pi j f_m}{2\pi j (f_{osc} + f_m) C V_{osc}}; \quad H \equiv \frac{-g_m}{2\pi j f C}; \quad T \equiv H^{N_{stage}} \quad (6.29)$$

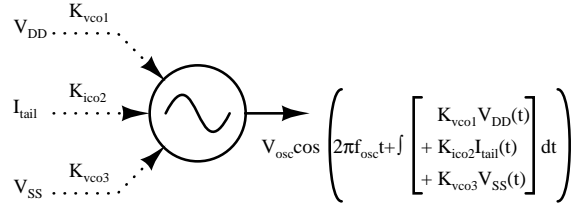
Loop gain  $T(f_{osc}) = 1 \angle 0^\circ$  to satisfy the oscillation conditions, so  $|H|^k \approx 1$ . Thus, all noise sources contribute roughly equally, according to LTI analysis. Approximating the loop gain with a Taylor series (cf. [156]) for  $f_m \ll f_{osc}$ , we obtain

$$S_\phi(f_m) = \sum_k \frac{|K_{ICO,k}|^2}{[2\pi f_m]^2} S_{I,k} \approx \frac{N_{stage} S_I}{|2\pi f_{osc} C V_{osc}|^2} \frac{1}{\left| \frac{\partial T}{\partial f} \right|_{f_{osc}} f_m^2} \quad (6.30)$$

where  $V_{osc}$  denotes the peak fundamental amplitude of a given ring-oscillator node and  $S_I \equiv 2k_B T(\gamma_n + \gamma_p)g_m$ . Substituting the above expressions for  $C$ ,  $P$ ,  $V_{osc}$ , and  $f_{osc}$ , and using  $g_m \approx \mu C_{ox} \frac{1}{2} V_{DD}$ , we have

$$S_\phi(f_m) = \frac{k_B T(\gamma_n + \gamma_p)}{2P} \frac{f_{osc}^2}{f_m^2} N_{stage} \quad (6.31)$$

so for a fixed power and oscillation frequency, LTI analysis predicts that phase noise worsens as the number of stages  $N_{stage}$  increases. This result is incorrect [36, 107]. The error occurs because LTI analysis assumes that  $|H|^k \approx 1$  and hence that all noise sources contribute to phase noise *at all times* during the oscillation cycle. This incorrect assumption neglects the large-signal hard switching of the oscillator—once a stage has “switched,” it is no longer sensitive to noise sources influencing its timing voltage. LTI analysis fundamentally cannot capture this *time-varying* behavior.



**Figure 6.6.:** Conceptual Illustration of Direct-KICO Method

#### 6.1.4 Direct KICO Method

##### Description

With “Direct-KICO” analysis, for noise concentrated at low frequencies, such as flicker noise, we obtain a constant  $K_{ICO}$  by directly differentiating the expression for the oscillation frequency (from periodic-steady-state (PSS) analysis of Section 2.3) with respect to a given noise quantity [21, 51, 216–220], hence directly obtaining the current-controlled oscillator gain as conceptually illustrated in Fig. 6.6. For ring-oscillator supply noise or tail-current noise, this technique works quite well (cf. [36, 216]); however, for LC oscillators, the method is harder to apply unless one can obtain higher-order corrections to  $f_{osc}$  (e.g. for varactor-tuned oscillators see [217, 219]).

##### Procedure/Example

1. **Perturbation:** In the presence of low-frequency noise, the delay-cell voltage  $v_k(t) = p(f_{osc}t + \int_{t_0}^t d\tau \{K_{ICO}i_{noise}(\tau)\})$ , where  $p(f_{osc}t)$  denotes a squarewave.
2. **NMF:** Because only one delay cell is on at a time, the effective spectrum for a single noise source assuming  $g_{mp} = g_{mn}$  is

$$S_{ip,n}^{eff, single}(f) = \frac{1}{N_{stage}} S_{i,1/f}(f) \Rightarrow S_i^{eff, tot} = \frac{K_f}{(C_{ox}WL)f} g_m^2 \quad (6.32)$$



where the (two-sided–positive/negative frequency) flicker-noise spectrum of each transistor is [27]

$$S_{i,1/f}(f) = \frac{1}{2} \frac{K_f}{C_{ox} W L f} g_m^2 \quad (6.33)$$

3.  **$K_{ICO}$  and NTF:** We find both the NTF and the  $K_{ICO}$  gain [for low-frequency noise] at once by differentiating the oscillation frequency with respect to the noise source in question:

$$\begin{aligned} K_{ico}^{direct} &= \left. \frac{df_{osc}}{di_n} \right|_{i_n=0} = \frac{d}{di_n} \frac{2}{CV_{DD}} \left[ \sum_{k=1}^{2N_{stage}} \frac{1}{I+i_k} \right]^{-1} \\ &= \frac{1}{2N_{stage}^2 CV_{DD}} = \frac{f_{osc}}{2N_{stage} I_{av}} \end{aligned} \quad (6.34)$$

where  $C$ ,  $I_{peak}$  are given in (2.16).

4. **Spectrum:** Hence, the phase noise due to flicker noise is

$$S_\phi(f_m) = \frac{K_{vco,LF}^2}{f_m^2} S_i^{eff}(f_m) \approx \frac{8K_f}{N_{stage} P} \frac{f_{osc}^2}{f_m^3} \quad (6.35)$$

where  $P$  is given in (2.17). Thus, flicker noise performance improves as  $N_{stage}$  increases for fixed frequency of oscillation and power [36, 107].

CAVEAT: the direct-KICO method does NOT work for white noise, e.g. were we to use the low-frequency VCO gain for white noise, we would get the following incorrect result:

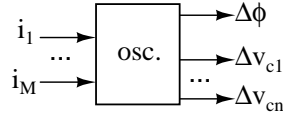
$$\begin{aligned} S_\phi^{white,VCO[wrong]}(f_m) &= \frac{K_{vco,LF}^2}{f_m^2} S_i^{white} \\ &= \frac{k_B T (\gamma_p + \gamma_n)}{4N_{stage}^2 P} \frac{f_{osc}^2}{f_m^2} \end{aligned} \quad (6.36)$$

which predicts phase noise  $\propto 1/N_{stage}^2$ , but the phase noise is actually independent of  $N_{stage}$  (cf. Section 6.1.3).

### 6.1.5 Phase-Sensitivity Method

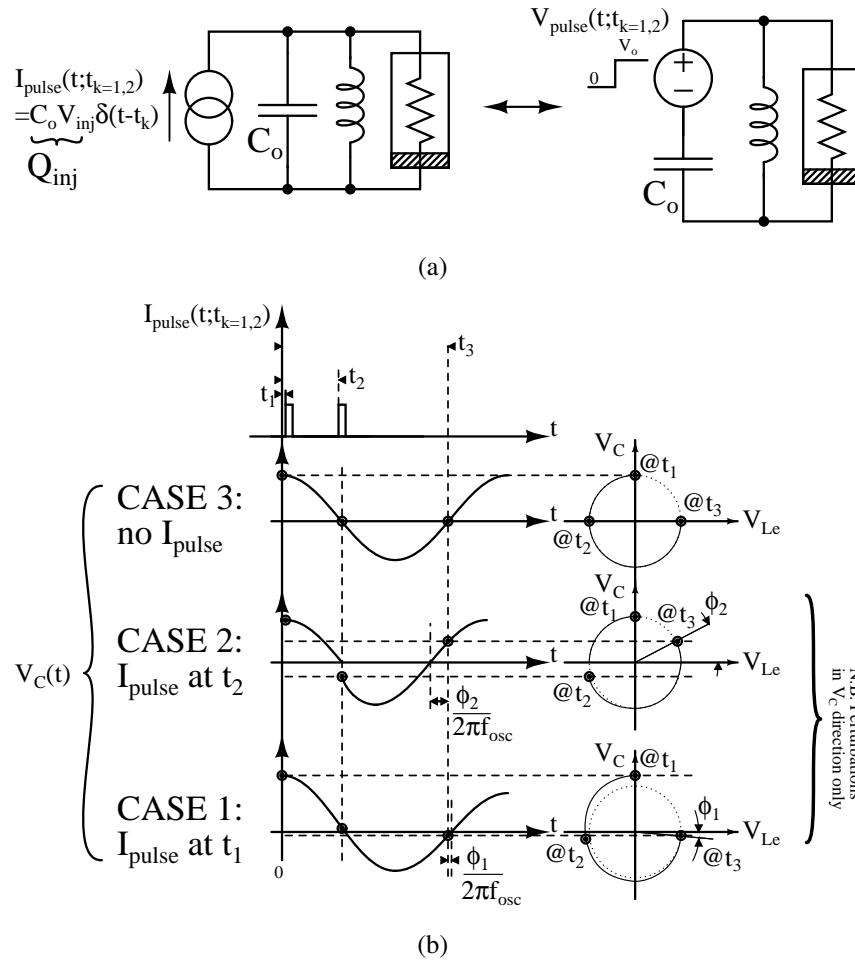
#### Description

The Phase-Sensitivity Method [44, 58, 69, 71–73, 107, 113–115, 130, 189–198] views the oscillator as a system converting (noise) inputs into phase/amplitude (perturbations), as shown in Fig. 6.7. To be consistent with Section 6.1.1, we show  $M$  noise inputs, one



**Figure 6.7.:** Phase-Sensitivity Method Oscillator Model

phase output, and  $n$  amplitude perturbations, corresponding to the  $n$  [capacitor-voltage] state variables of the oscillator. For the simplified model of the NMOS LC oscillator in Fig. 2.5(c), we have two state variables  $V_C$  and  $V_{Le} \equiv \sqrt{\frac{L}{C}}i_L$ , as illustrated on the “phase portrait” of  $V_C$  *v.*  $V_{Le}$  in Fig. 6.8 that juxtaposes the phase portrait with corresponding time-domain waveforms. As shown in the figure, an impulse, i.e. an instantaneous change to one of the state variables, leads to amplitude and phase error. Intuitively, perturbations near zero crossings cause greater steady-state phase perturbation, while those occurring when the given state variable is maximum cause little phase perturbation but more amplitude perturbation. Generalizing to all points within the oscillation cycle, the “impulse-sensitivity function” (ISF)  $\Gamma^{C_o}(2\pi f_{osc}t)$  weights the contributions of noise sources depending on when during the cycle they occur—e.g. in Fig. 6.8,  $\Gamma^{C_o}(2\pi f_{osc}t_1) \approx 0$ , while at  $t_2$ ,  $|\Gamma^{C_o}(2\pi f_{osc}t_2)|$  is roughly maximum. Thus, phase sensitivity to impulse perturbation depends on the time within the cycle that the impulse occurs. Hajimiri and Lee [114] also demonstrated with simulation that the steady-state phase shift is nearly proportional to the state-variable perturbation at a given time during the cycle, provided that the perturbation is much less than the state variable’s maximum value.



**Figure 6.8.:** Oscillator Phase-Perturbation: (a) Impulse Current Injection, (b) Corresponding Capacitor-Voltage Waveforms

### Procedure/Example

1. **Perturbation:** From the above observations, Hajimiri and Lee proposed the following linear, periodically time-varying (LPTV) model for the response of the oscillator's phase:

$$\Delta\phi(t) \equiv \sum_k \int_{t_0}^t d\tau \left\{ \frac{\Gamma_k^{C_0}(2\pi f_{\text{osc}}\tau) i_k(\tau)}{q_{\text{max}}} \right\} \quad (6.37)$$

where  $q_{max} \equiv C_o V_{osc}$ ,  $V_{osc}$  is the peak fundamental amplitude across  $C_o$ , and  $\Gamma_k^{C_o}$  is a unitless, periodic ( $2\pi$ ) function that captures the periodically changing sensitivity of the phase over each cycle. The subscript  $k$  indicates that each noise source in general has a different sensitivity function because it is located in a different place in the circuit. Superscript  $C_o$  indicates that all noises' effects are referred to the capacitor voltage  $V_{C_o}$ .

2. **NMF, NTF:** Calculated in same fashion as discussed in Section 6.1.1 (see Table 6.2(a)).
3. **" $K_{ICO}$ :"** For the LC NMOS oscillator, using the equivalent differential tank,  $q_{max} \equiv C_o V_{pk,fund} = C(2V_{osc})$ . Hence, for differential capacitor  $C_o = C$ , we can approximate [44, 114]:<sup>8</sup>

$$\Gamma^{C_o}(\theta) \approx \frac{q_{max}}{C_o} \frac{\frac{d}{d\theta} V_{C_o}}{\sum_k (\frac{d}{d\theta} V_{C_k})^2} = \frac{\sin(\theta)}{-2} \quad (6.38)$$

(cf. [114] and Appendix B.6 for more accurate procedures to find  $\Gamma$ ). The overall ISF is

$$\Gamma_k^{C_o}(\theta) \equiv \Gamma_{eff}(\theta) = \Gamma^{C_o}(\theta) NTF_k(\theta) NMF_k(\theta) \quad (6.39)$$

Thus, we can intuitively think of  $K_{ICO} = \frac{\Gamma^{C_o}(x)}{q_{max}}$  as weight in time (during the cycle) for the noise sources, the NTF as weight due to circuit placement of the noise sources, and the NMF as an adjustment to the noise statistics based on changing bias.

4. **Spectrum:** To obtain  $S_\phi(f_m)$  using (6.37), suppose the "noise" is

<sup>8</sup>Note, however, that using the derivative ("tangent") approximation for the ISF, while often good for LC oscillators, can prove extremely misleading for ring oscillators. In fact, for a 3-stage ring oscillator, Srivastava and Roychowdhury obtained an analytic expression for sensitivity obtained with the FPE method, demonstrating that a node's phase sensitivity is in fact maximum when the *next* node undergoes a sharp transition [186].

$i_n(t) = I_k(f_m) \cos[2\pi(kf_{osc} + f_m)t]$  with  $f_m/f_{osc} \ll 1$  and expand the sensitivity function  $\Gamma_k^{C_o}$  in a Fourier series—for simplicity assume that it is an even function:  $\Gamma_k^{C_o}(\theta) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\theta)$ . Substituting the expansion into (6.37):

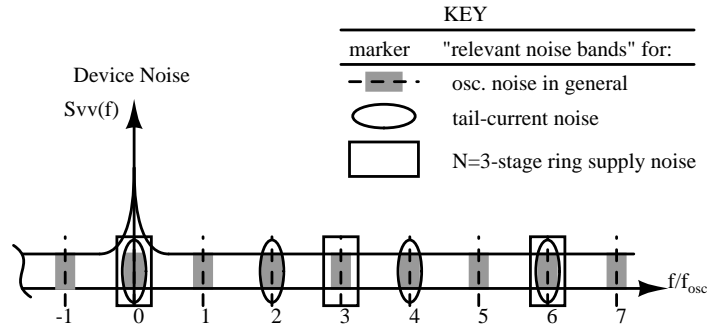
$$\phi(t) \approx \underbrace{\frac{c_n I_n(f_m)}{2q_{max}[2\pi f_m]}}_{\phi_{peak}} \sin(2\pi f_m t) \quad (6.40)$$

$$\frac{P(f_{osc} + f_m)}{P(f_{osc})} = \frac{V_{SB,peak}^2/2R}{V_{carrier,peak}^2/2R} = \left( \frac{\phi_{peak} = \sqrt{2}\phi_{rms}}{2} \right)^2 \leftrightarrow \frac{1}{2} S_\phi(f_m) \quad (6.41)$$

Interpreting  $\mathbb{E}[|I_n(f_m)|^2] = 2S_i(nf_{osc} + f_m)$  (cf. Section 6.1.1), the total single sideband power due to phase modulation is given by

$$\frac{P_{tot}(f_{osc} + f_m)}{P(f_{osc})} = \frac{2}{(4q_{max}[2\pi f_m])^2} \sum_{n=0}^{\infty} c_n^2 \underbrace{2S_i(nf_{osc} + f_m)}_{\mathbb{E}[|I_n|^2]} \quad (6.42)$$

where the first factor of two is to account for both  $nf_{osc} \pm f_m$ . This noise mixing action intuitively means that only noise near integer multiples of  $f_{osc}$  matters. Further symmetry in the ISF, such as that for ring-oscillator supply noise or differential-pair tail-current noise, lessens the number of harmonics that matter, as illustrated in Fig. 6.9. Thus,



**Figure 6.9.:** Frequency-Conversion Viewpoint of ISF [114]

$$\frac{P_{tot}(f_{osc} + f_m)}{P(f_{osc})} \approx \frac{1}{2(q_{max}[2\pi f_m])^2} \left\{ \begin{array}{ll} \Gamma_{rms}^2 S_{i,const} & , \text{white} \\ \Gamma_{DC}^2 S_{i,flicker}(f_m) & , \text{flicker} \end{array} \right\} \approx \frac{1}{2} S_\phi(f_m) \quad (6.43)$$

where  $\Gamma_{rms}^2 \equiv \int_{2\pi} \frac{d\theta}{2\pi} \{ \Gamma_{eff}^2(\theta) \}$ ,  $\Gamma_{DC} \equiv \int_{2\pi} \frac{d\theta}{2\pi} \{ \Gamma_{eff}(\theta) \}$ . Comparing to the jitter method, we find  $\kappa^2 = \frac{\Gamma_{rms}^2 S_{i,white}}{(q_{max}[2\pi f_{osc}])^2}$ . Table 6.3 lists the values of  $\Gamma_{rms}^2$  for the LC NMOS oscillator. Substituting these values, we obtain

$$\begin{aligned} S_\phi(f_m) = & \frac{k_B T}{(2C V_{osc}[2\pi f_m])^2} \left( \frac{1}{R_p} \right. \\ & + \frac{1}{2} \left( 1 - \left[ \frac{1}{2} \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right]^2 \right) \gamma \sqrt{K I_{tail}} \\ & \left. + \frac{1}{4} \left( \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right)^2 \gamma g_{d0tail} \right) \end{aligned} \quad (6.44)$$

Note the analytic confirmation of the intuitive behavior that for small amplitudes, the switch transistors' noise is more significant because they act like a differential class-A amplifier, while the tail noise is less significant because it appears as "common mode." However, for larger amplitudes, we see that their roles reverse: intuitively, the switch transistors appear as a cascode device when fully switched, and the tail current noise feeds directly to the output [113].

**Table 6.3:** Effective  $\Gamma_{rms}^2$

$R_{p1,2}$	$M_{sw1} + M_{sw2}$	$I_{tail}$
$\frac{1}{8}$	$\frac{1}{4} \left( 1 - \left[ \frac{1}{2} \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right]^2 \right)$	$\frac{1}{32} \left( \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right)^2$
	$\frac{1}{1 + \frac{V_{osc}}{\sqrt{I_{tail}/K}}}$	

## 6.1.6 Fokker-Planck-Equation (FPE) Method

### Description

The FPE Method first defines amplitude/phase perturbations to ensure that amplitude noise remains small but that phase noise is accumulated [35, 43, 47, 175]<sup>9</sup>. The technique then shows that the phase distribution is asymptotically Gaussian and solves for constants that characterize that distribution and can be substituted into a known form for the spectrum  $S_\phi$ . The Fokker-Planck equation describes the *distribution* of a random process, rather than the process itself. Ham/Hajimiri [63, 64] also form a Fokker-Planck equation for the phase distribution, but instead of rigorously solving the math, they obtain the spectrum constant with an intuitive argument based on the phase-sensitivity method and a comparison to Einstein's Brownian motion paper [49], arguably the first application appearance of the FPE method.

### Procedure/Example

1. **Perturbation:** Noise perturbs the oscillator's amplitude and phase:

$$\vec{v}(t) = \vec{v}_{ss} \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) + \Delta \vec{v} \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) \quad (6.45)$$

<sup>9</sup>Kaertner's original paper [175] chose to decompose perturbations into components orthogonal and parallel to the oscillator limit cycle, and Li et al. provide an intuitive discussion for a transmission-line oscillator with this orthogonal projection [187]; however, most later formulations typically use the Floquet decomposition to decouple phase and amplitude responses, making the phase response independent of the choice of state variables [41, 43]. The Floquet decomposition can also be generalized for injection-locked oscillators [188].

where the vector  $\vec{v}$  denotes the state-variables of the oscillator, e.g. the state-variable formulation (6.46) of the LC-NMOS oscillator derived from (2.8)-(2.9) including noise sources is

$$\underbrace{\frac{d}{dt} 2C \begin{pmatrix} V_{C1} \\ V_{L1e} \\ V_{C2} \\ V_{L2e} \end{pmatrix}}_{\vec{q}(\vec{v})=2C\vec{v}} = \underbrace{\begin{pmatrix} \frac{-2V_{L1e}}{\sqrt{L/C}} - \frac{2V_{C1}}{R_p} + f(V_{C1} - V_{C2}, i_n) + i_{n1} + i_{r1} \\ \frac{2V_{C1}}{\sqrt{L/C}} \\ \frac{-2V_{L2e}}{\sqrt{L/C}} - \frac{2V_{C2}}{R_p} + f(V_{C2} - V_{C1}, i_n) + i_{n2} + i_{r2} \\ \frac{2V_{C2}}{\sqrt{L/C}} \end{pmatrix}}_{-\vec{i}_{nl n}(\vec{v}, \vec{i}_{noise})} \quad (6.46)$$

$$\vec{i}_{noise} \equiv \begin{pmatrix} i_{n1}(t) \\ i_{n2}(t) \\ i_{ntail}(t) \\ i_{nr1}(t) \\ i_{nr2}(t) \end{pmatrix}$$

where  $i_n = i_{n1} + i_{n2} + i_{ntail}$  and  $f(V_{dm}, i_n)$  is given by (2.10). Substituting (6.45) into (6.46), neglecting 2<sup>nd</sup>-order term  $\frac{d\phi(t)}{dt} \frac{d}{dt} \Delta\vec{v}(\tilde{t})$ , and setting  $\tilde{t} \equiv t + \frac{\phi(t)}{2\pi f_{osc}}$ , we obtain<sup>10</sup>

$$\begin{aligned} \frac{d\phi(t)}{dt} \frac{d}{dt} \vec{v}_{ss}(\tilde{t}) + \frac{d}{dt} \Delta\vec{v}(\tilde{t}) &\approx \\ \underline{C}^{-1}(\vec{v}_{ss}(\tilde{t})) \underline{G}(\vec{v}_{ss}(\tilde{t})) \Delta\vec{v}(\tilde{t}) + \underline{C}^{-1}(\vec{v}_{ss}(\tilde{t})) \underline{NTF}(\vec{v}_{ss}(\tilde{t})) \vec{i}_{noise} & \end{aligned} \quad (6.47)$$

where

$$\underline{C}(\vec{v}) \equiv \frac{\partial \vec{q}}{\partial \vec{v}}, \quad \underline{G}(\vec{v}) \equiv \frac{\partial \vec{i}(\vec{v}, \vec{i}_{noise})}{\partial \vec{v}}, \quad \underline{NTF}(\vec{v}) \equiv \left. \frac{\partial \vec{i}(\vec{v}, \vec{i}_{noise})}{\partial \vec{i}_{noise}} \right|_{\vec{i}_{noise}=\vec{0}} \quad (6.48)$$

<sup>10</sup>Swain [181] has solved the special case of Coram's 2D oscillator for high noise levels by solving for the distribution exactly without neglecting these higher-order terms.



Scalar  $\phi(t)$  denotes phase error, and vector  $\Delta\vec{v}(\tilde{t})$  denotes amplitude error in all  $n$  capacitor voltages/inductor currents.

2. **NMF/NTF**: Calculated similarly to previous methods, except now, we explicitly include all state variables:

$$\underline{NMF}\sqrt{S_{max}} \equiv \sqrt{2k_B T \gamma} \begin{pmatrix} \sqrt{g_{d0;1}(\theta)} & 0 & 0 & 0 & 0 \\ 0 & \sqrt{g_{d0;2}(\theta)} & 0 & 0 & 0 \\ 0 & 0 & \sqrt{g_{d0tail}} & 0 & 0 \\ 0 & 0 & 0 & \sqrt{\frac{2}{\gamma R_p}} & 0 \\ 0 & 0 & 0 & 0 & \sqrt{\frac{2}{\gamma R_p}} \end{pmatrix} \quad (6.49)$$

$$g_{d0;1,2}(\theta) \approx g_{m1,2} = \sqrt{K I_{tail}} \left( x_{1,2} + \sqrt{1 - x_{1,2}^2} \right) \quad (6.50)$$

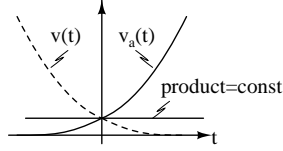
$$x_{1,2} \equiv \frac{V_{dm}}{2\sqrt{I_{tail}/K}} = \frac{\pm V_{osc} \cos(\theta)}{\sqrt{I_{tail}/K}}$$

$$\underline{NTF} \equiv \frac{\partial \vec{i}_{nl}}{\partial \vec{i}_{noise}} \Big|_{\vec{i}_{noise}=\vec{0}, \vec{v}=\vec{v}_{ss}(\theta/2\pi f_{osc})}$$

$$= - \begin{pmatrix} 1 + A_{i1}(\theta) & A_{i1}(\theta) & A_{i1}(\theta) & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ A_{i2}(\theta) & 1 + A_{i2}(\theta) & A_{i2}(\theta) & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \quad (6.51)$$

$$A_{i1,2} \equiv \frac{\partial I_{1,2}}{\partial i_n} \Big|_{i_n=0, \vec{v}=\vec{v}_{ss}(\theta/2\pi f_{osc})} = \frac{-1}{2} \left( 1 + \frac{x_{1,2}}{\sqrt{1 - x_{1,2}^2}} \right) \quad (6.52)$$

3.  $K_{ICO}$ : Conceptually, we want to “divide” by the phase coefficient  $\frac{d}{dy} \vec{v}_{ss}(\tilde{t})$  in (6.47). This feat is accomplished by multiplying by a solution to the *adjoint* linear companion system [47]. Intuitively, the adjoint system has the same behavior as the forward system, except with the time axis reversed, e.g. the linear system  $\frac{dv}{dt} = \frac{-1}{RC} v$  has associated adjoint system  $\frac{dv_a}{dt} = \frac{+1}{RC} v_a$ —their product is a constant, as shown in Fig. 6.10. Hence, the adjoint linear companion system is



**Figure 6.10.:** Adjoint System Response Illustration

$$\frac{d}{d\tilde{t}} \Delta \vec{v}_a^T(\tilde{t}) = -\Delta \vec{v}_a^T(\tilde{t}) \underline{\Omega}(\vec{v}_{ss}(\tilde{t})) \quad (6.53)$$

$$\underline{\Omega}[\vec{v}_{ss}(\tilde{t})] \equiv \left[ \frac{\partial \bar{q}}{\partial \vec{v}} \right]^{-1} \frac{\partial \vec{i}_{nltn}}{\partial \vec{v}} \Big|_{\vec{v}=\vec{v}_{ss}(\tilde{t})} = 2\pi f_{osc} \left( \begin{array}{cc|cc} \frac{-1}{Q_p} + \frac{1}{Q_a} & -1 & -\frac{1}{Q_a} & 0 \\ 1 & 0 & 0 & 0 \\ \hline -\frac{1}{Q_a} & 0 & \frac{-1}{Q_p} + \frac{1}{Q_a} & -1 \\ 0 & 0 & 1 & 0 \end{array} \right) \quad (6.54)$$

$$\frac{1}{Q_p} \equiv \frac{2}{R_p G_0}, \quad \frac{1}{Q_a} \equiv \frac{\sqrt{KI_{tail}}}{2G_0} \frac{1-2x^2}{\sqrt{1-x^2}} \quad (6.55)$$

where  $G_0 \equiv 2\sqrt{\frac{C}{L}}$  and  $x$  is given in (6.52). Assuming negligible harmonics ( $Q_{a,p} \rightarrow \infty$ ), we obtain

$$\begin{aligned} \vec{K}_{ico}^T(\theta) &\approx A[\cos(\theta), \sin(\theta), -\cos(\theta), -\sin(\theta)] \\ &+ B[\sin(\theta), -\cos(\theta), -\sin(\theta), \cos(\theta)] \end{aligned} \quad (6.56)$$

Next, normalize:  $\vec{K}_{ico}^T \frac{d\vec{q}_{ss}(\tilde{t})}{d(2\pi f_{osc} \tilde{t})} = 1 \Rightarrow A = 0, B = -1/(4CV_{osc}) [rad/s/A]$ . This vector  $\vec{K}_{ico}^T(t)$  is actually a ‘‘Floquet eigenvector,’’ which is in general not exactly tangent to the oscillator limit cycle [47, 183, 222, 223] (recall the picture of the limit cycle in Fig. 2.10); often the tangent vector is a good approximation, but not always [176, 179]. As mentioned in Section 2.5.1, using these (n+1) quantities  $\phi(t)$ ,  $\Delta \vec{v}(\tilde{t})$  to describe n state-variable deviations allows more than one *choice* of perturbations. We choose that the amplitude perturbations satisfy  $\vec{K}_{ico}^T(\tilde{t}) \Delta \vec{v}(\tilde{t}) = 0$ . Hence, mul-

tipling by this periodic solution to the “time reversed” or adjoint linear companion equation decouples the amplitude and phase:

$$\frac{d\phi(t)}{dt} = \vec{K}_{ico}^T(\tilde{t}) \underline{NTF}(\vec{v}_{ss}(\tilde{t})) \vec{i}_{noise} \quad (6.57)$$

$$\frac{d}{d\tilde{t}} \Delta \vec{v}(\tilde{t}) = \underline{\Omega}(\vec{v}_{ss}(\tilde{t})) \Delta \vec{v}(\tilde{t}) \quad (6.58)$$

Note that the equation for the phase is still nonlinear in  $\phi$  because  $\tilde{t} = t + \frac{\phi(t)}{2\pi f_{osc}}$ , but the amplitude equation is linear. Furthermore, it can be shown that defining amplitude perturbations in this fashion ensures that  $\Delta \vec{v}(\tilde{t})$  remains small as long as the instantaneous noise currents  $\vec{i}_{noise}$  remain small, while  $\phi(t)$  can grow without bound [47]. This situation properly reflects physical oscillator behavior, as discussed in Section 2.5.1.

4. **Spectrum:** The goal is to show that the phase distribution is asymptotically (for large  $t$ ) Gaussian and hence easy to deal with. Therefore, we want to show that  $\phi$  has characteristic function  $\Phi(\xi, t) \equiv \mathbb{E} [e^{j\xi\phi(t)}] \approx e^{j\xi\mu(t) - \frac{1}{2}\xi^2\sigma^2(t)}$  for large  $t$ . For simplicity, we show the case for white noise; however, the corresponding case for flicker noise can also be shown [26].

(a) First, re-write (6.57) in standard stochastic-differential-equation (SDE) form [49]:

$$d\phi(t) = \vec{p}^T \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) d\vec{W}(t) \quad (6.59)$$

$$\begin{aligned} \vec{p} &= \left[ \vec{K}_{ICO}^T \times \underline{NTF} \times \underline{NMF} \times \sqrt{S_{max}} \right]^T \\ &= \frac{\sin(\theta)}{4CV_{osc}} \begin{pmatrix} (1 + A_{i1}(\theta) - A_{i2}(\theta))\sqrt{S_{M1}(\theta)} \\ (-1 + A_{i1}(\theta) - A_{i2}(\theta))\sqrt{S_{M2}(\theta)} \\ (+A_{i1}(\theta) - A_{i2}(\theta))\sqrt{S_{tail}} \\ \sqrt{S_{Rp/2}} \\ -\sqrt{S_{Rp/2}} \end{pmatrix} \end{aligned} \quad (6.60)$$

where  $\vec{p}$  has units  $1/\sqrt{sec}$ . Roughly speaking  $\frac{d}{dt}\vec{W}(t) = \vec{i}_{noise}^{unmod}$ , i.e. unmodulated white noise, and the Wiener process  $\vec{W}(t)$  has the following properties:

- $\mathbb{E} \left[ \vec{h}^T(t) d\vec{W}(t) \right] = 0$  (zero mean)
- $\mathbb{E} \left[ \vec{h}^T(t) d\vec{W}(t) d\vec{W}^T(t) \vec{h}(t) \right] = \vec{h}^T(t) \vec{h}(t) dt$ ; roughly “ $dW(t) \approx \sqrt{dt}$ ”
- Given  $i_{white}(t)$  with two-sided spectrum  $\frac{2k_B T}{R}$ , the corresponding scaled Wiener process is  $\sqrt{\frac{2k_B T}{R}} dW(t)$ .

(b) Hence, we have  $\frac{\partial}{\partial t} \mathbb{E} [e^{j\xi\phi(t)}] = \frac{1}{dt} \mathbb{E} \left[ j\xi e^{j\xi\phi(t)} d\phi(t) - \frac{\xi^2}{2} e^{j\xi\phi(t)} (d\phi(t))^2 \right]$  where we include up to second-order derivatives in  $\phi(t)$  because the derivatives involve white noise, which is not smooth. Applying the properties above, we have

$$\begin{aligned} \frac{\partial}{\partial t} \mathbb{E} [e^{j\xi\phi(t)}] &= \mathbb{E} \left[ -\frac{\xi^2}{2} e^{j\xi\phi(t)} \vec{p}^T \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) \vec{p} \left( t + \frac{\phi(t)}{2\pi f_{osc}} \right) \right] \\ &= -\frac{\xi^2}{2} \sum_{k,n} \mathbb{E} \left[ \vec{P}_k^T \vec{P}_n^* e^{j[(\xi+k-n)\phi(t)+(k-n)2\pi f_{osc}t]} \right] \end{aligned} \quad (6.61)$$

where  $\vec{P}_k$  denote the Fourier coefficients of periodic vector function  $\vec{p}$ .

(c) Substituting the characteristic function  $\Phi(\xi, t) \equiv \mathbb{E} [e^{j\xi\phi(t)}]$ , we obtain

$$\frac{d}{dt} \Phi(\xi, t) = -\frac{\xi^2}{2} \sum_{k,n} \vec{P}_k^T \vec{P}_n^* \Phi(\xi + k - n, t) e^{j(k-n)2\pi f_{osc}t} \quad (6.62)$$

By substituting the characteristic function<sup>11</sup> for a Gaussian random variable  $\Phi_g(\xi, t) = e^{j\xi\mu(t) - \frac{1}{2}\xi^2\sigma^2(t)}$ , one finds that the equation is approximately satisfied for large t and furthermore that [47]

$$\mu(t) \approx constant, \quad \sigma^2(t) \approx (2\pi f_{osc} \kappa)^2 t \quad (6.63)$$

$$\kappa^2 2\pi f_{osc}^2 = \sum_k \vec{P}_k^T \vec{P}_k^* = p_{rms}^2 = \int_{2\pi} \frac{d\theta}{2\pi} \left\{ \vec{p}^T \left( \frac{\theta}{2\pi f_{osc}} \right) \vec{p} \left( \frac{\theta}{2\pi f_{osc}} \right) \right\} \quad (6.64)$$

<sup>11</sup>It can be shown that (6.62) corresponds to the following Fokker-Planck equation  $\frac{\partial D}{\partial t} = \frac{1}{2} \frac{\partial}{\partial \phi^2} [\vec{p}^T (t + \phi/2\pi f_{osc}) \vec{p} (t + \phi/2\pi f_{osc}) D]$  where  $D$  is the probability distribution function.

(d) Again using the properties of the Wiener processes mentioned above, we find that asymptotically [26],

$\mathbb{E}[\phi(t)[\phi(t+\tau) - \phi(t)]] = 0$  and that  $\mathbb{E}[\phi(t)\phi(t+\tau)] = (2\pi f_{osc}\kappa)^2 \min(t, t+\tau)$ , which is the autocorrelation function<sup>12</sup> so  $S_\phi(f_m) = \kappa^2 \left(\frac{f_{osc}}{f_m}\right)^2$ .

(e) Evaluating the integral above and neglecting the higher-order terms yields roughly

$$\begin{aligned}
S_\phi(f_m) &= \frac{k_B T}{(2C V_{osc} [2\pi f_m])^2} \left( \frac{1}{R_p} \right. \\
&\quad \left. + \frac{1}{2} \left( 1 - \left[ \frac{1}{2} \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right]^2 \right) \gamma \sqrt{K I_{tail}} \right. \\
&\quad \left. + \frac{1}{4} \left( \frac{V_{osc}}{\sqrt{I_{tail}/K}} \right)^2 \gamma g_{d0tail} \right)
\end{aligned} \tag{6.65}$$

For small oscillation amplitude,  $A_{i1}(\theta) - A_{i2}(\theta) \approx 0$ , and we recover the LTI expressions of Table 6.2(a)– in particular, the tail-current noise plays only a small role for small-amplitude oscillations. Flicker-noise expressions are analogous to those derived in Section 6.1.5 cf. also Appendix B.7. Thus, we see the FPE method simplifies to the LPTV conversion method (1) when we consider the same number of harmonics and (2) when the limit-cycle tangent is a good approximation for the Floquet eigenvector (adjoint solution).

## 6.2 Summary and Comparison

### 6.2.1 Discussion

Table 6.4 compares the analysis techniques and indicates which aspects they include/omit. LTI analysis is the simplest, but cannot capture noise-modulation effects. The FPE method is the most rigorous and gives the most systematic procedure to write phase-noise equations, albeit the most complicated. The Cadence PNOISE analysis is derived from the FPE method; however, amplitude noise  $\Delta \vec{v}$  is sometimes included in the plotted values

<sup>12</sup>Thus, we know that  $\phi(t)$ ,  $\phi(t+\tau)$  are individually Gaussian, and the increments  $\phi(t)$ ,  $[\phi(t+\tau) - \phi(t)]$  are uncorrelated. Uncorrelated Gaussian variables are independent, so the two must also be jointly Gaussian.

**Table 6.4:** Comparison of Analysis Methods

	Conversion/LTI	Conversion/LPTV	Modulation	Jitter	Direct KICO	Phase Sensitivity	Fokker-Planck
<b>Types of Noise Effects Captured</b>							
white	1	1	1	1	0	1	1
flicker	0	1	1	0	1	1	1
<b>Oscillator Nonidealities</b>							
NMF (changing device bias point)	0	1	1	1	0*	1	1
NTF mixing	0	1	1	1	0	1	1
<b>Equation for Phase</b>							
Equation Type <sup>‡</sup>	LTI	LPTV	NLN	LPTV	LTI	LPTV	NLN
Assume small device noise	1	1	1	1	1	1	1
Assume small $\phi(t)$	1	1	0	0	0	1	0
<b>Analysis</b>							
Easiest Oscillator to Analyze	LC	LC	LC	RO	RO	ALL	ALL
Complexity (1=least, 5=most)	1	2 – 4 <sup>†</sup>	3 – 5 <sup>†</sup>	2	2 – 3 <sup>†</sup>	4	5
Most Common Use	HAND	HAND	CAD	HAND	HAND	CAD	CAD

\* Not explicitly, but can find "effective" spectrum

† depending on # harmonics included and whether NTF/NMF included

‡ Equation for phase  $\phi$  is either LTI, LPTV or nonlinear (NLN).

[182]. The harmonic-balance (HB) formulation of the modulation method is equivalent to the FPE method provided that Floquet normalization is used and sufficient harmonics are considered (cf. Appendix B.3 and [35, 139]). The “small phase” assumption effectively means that only the nonlinear *phase equations* of the Modulation/Fokker-Planck methods can capture injection-locking behavior [30]; however, the LPTV phase equation is sufficient to capture most noise of interest, including flicker.

For hand calculation, the conversion method is simplest for LC oscillators, while the Jitter method and direct-KICO method are most straightforward for ring/relaxation oscillators. Furthermore, the Jitter Method is extremely accurate when the ring oscillator exhibits hard switching [24]; this is precisely the case when the conversion method is the least accurate, so these two methods complement each other.

### 6.2.2 When to Use Which Method

1. **Conversion/LTI:** Resonant oscillators with little noise modulation (e.g. LC-tank-resistor noise and noise whose noise transfer function does *not* involve any switching networks).
2. **Conversion/LPTV:** Resonant oscillators and noise sources whose (1) bias points are modulated (e.g. switch/negative-resistance transistors in differential LC oscillator), or (2) transfer function to the output involves passing through a switching network (e.g. tail current of differential LC oscillator).
3. **Modulation:** Chiefly for accurate simulation of resonant oscillators; however, the “slowly varying” assumption is useful for mode analysis [19, 33] and squegging analysis [196].
4. **Jitter:** Ring oscillators’ white noise sources

5. **Direct KICO:** Ring oscillators' flicker noise sources and supply noise sources [216] (assuming  $f_{vdd-noise}^{max} \ll f_{osc}$ ).
6. **Phase Sensitivity:** The tangent approximation for the ISF is useful for resonant oscillators [44, 192, 193, 196, 197] with a small caveat about coupled LC quadrature oscillators [193]. Also, the sensitivity viewpoint gives useful design insight [113, 115].
7. **FPE:** Mainly for accurate simulation; however, sketching the equations as illustrated in Section 6.1.6 can yield insight into what type of modulation to expect and hence can guide simplification of the oscillator to the simplest possible model while still capturing the desired behavior (noise modulation, flicker upconversion, etc.). This information can then be used to apply a simpler approach for hand calculation, such as the Conversion Method, and can indicate how many harmonics to consider or what degree of noise modulation to include.

### 6.2.3 Phase-Noise Numerical Examples

Table 6.5 lists the numerical phase-noise results obtained by substituting the values from Table 2.1 on page 12 into the corresponding equation listed in the table columns. Noise contributions are subdivided by noise source.

Because we have employed a single-harmonic approximation for the LC-NMOS oscillator, the LPTV, modulation, phase-sensitivity, and FPE methods all yield nearly identical results. Numerical simulation in Cadence SPECTRE (MMSIM7) agrees with these methods to within 1dB, indicating the accuracy of these methods and of the harmonic approximation for the LC oscillator considered. On the other hand, we see that the LTI method has a large error, and even if we fudge the result by neglecting the  $g'_1$  term, LTI analysis still cannot capture tail-current noise.



**Table 6.5:** Phase Noise  $S_{\phi}(10kHz)[dB(rad^2/Hz)]$  (a) LC NMOS Oscillator, (b) Ring Oscillator

(a)

	Conversion			Mod.	Ph. Sens.	FPE	SPECTRE <sup>†</sup>
	LTI	LTI(smart)	LPTV				
Equation	(6.14)	(6.14) <sup>‡</sup>	(6.15)	(6.23)	(6.44)	(6.65)	n/a
$R_{p1,2}$	-137.88	-87.43	-87.43	-87.43	-87.43	-87.43	-86.96
$M_1 + M_2$	-139.36	-88.91	-89.05	n/c	-89.10	-89.10	-88.70
$I_{tail}$	*	*	-112.14	n/c	-112.14	-112.14	-111.71

(b)

	Jitter	Direct-KICO	SPECTRE <sup>†</sup>
Equation	(6.28)	(6.35)	n/a
Thermal	-76.29	**	-76.78
Flicker	**	-65.85	-66.20

\* = method would predict no phase noise

n/c = not calculated, but method can account for this noise

\*\* = method cannot calculate this noise

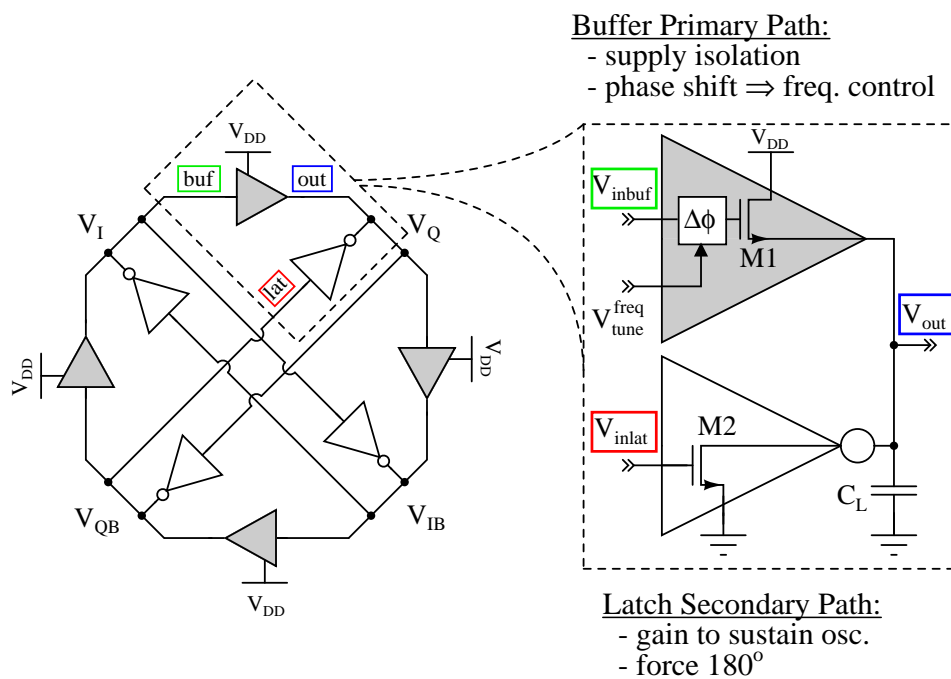
† = results of PNOISE “jitter” analysis and dividing by two for “two-sided”  
(positive/negative frequencies) spectrum

‡ = fudge by setting  $g'_1 = 0$

Table 6.5(b) shows the white and flicker phase noise components for the ring oscillator whose values are give in Table 2.1(b). Again, we see that for ring oscillators, the phase noise due to both flicker and thermal noise can be accurately predicted by a combination of the Jitter and Direct-KICO methods (<1dB discrepancy with SPECTRE numerical simulation).

## 7. DESIGN/ANALYSIS CASE STUDY: HIGH-PSR, QUADRATURE MRO IN 90-NM CMOS

This section details the design-oriented analysis of our proposed high-power-supply-rejection (PSR) quadrature multi-loop ring oscillator, shown in Fig. 7.1, to demonstrate both the application of the MRO analysis framework to design as well as the potential performance benefits that multi-loop ring oscillators can attain.



**Figure 7.1.:** Proposed Oscillator: Conceptual Block Diagram

Intuitively, the source-follower delay-cell structure isolates the oscillator core from the supply through the transistor's saturation drain-source resistance  $r_{ds}$ . The oscillation amplitude is established by the latch transistor entering the triode region. As long as the peak oscillation amplitude  $V_{osc}$  satisfies  $V_b + V_{osc} < V_{DD} + V_{t1}$  (where  $V_b$  is shown in Fig. 4.3(a)), the source-follower transistor M1 will remain in saturation, have a high drain-source impedance, and therefore provide improved supply rejection.

## 7.1 Oscillation Frequency

To derive these relationships more rigorously, we subdivide the unit delay cell into the phase-shift and nonlinear buffer/latch components as indicated in Fig. 4.3(a). These sections determine the steady-state oscillation frequency  $f_{osc}$  by analyzing the LTI phase-shift network ( Section 7.1.1) and the nonlinear buffer/latch (Section 7.1.2).

### 7.1.1 Phase-Shift Network

#### Overview

The following analysis will show that the phase shift network has a transfer function  $H = V_g/V_{inbuf}$  with magnitude response  $\approx -3dB$  and phase response  $\approx -\arctan\left(\frac{f}{f_2}\right)$  where

$$f_2 = \frac{0.159}{R_v C_c || [C_{gs1} + C_{gd1} + C_d]} \quad (7.1)$$

and where coupling capacitance  $C_c$ , gate capacitances  $C_{gs/d1}$ , drain capacitance  $C_d$ , and variable resistance  $R_v$  are in Fig. 4.3(a). For  $f_{osc} \in [0.1, 10]f_2$ , we hence obtain a roughly flat-magnitude phase-shift network.

#### Derivation

First, consider the bias/phase-shift network in Fig. 4.3(a) and (b). Because we adjust the frequency by tuning control voltages  $V_b$  and  $V_{cp}$  differentially, we consider the two extremes of the tuning range: (i) high oscillation frequency ( $R_v \ll R_b$ ) and (ii) low oscillation frequency ( $R_v \gg R_b$ ).

Treating the bias network as linear and performing superposition, we obtain the transfer functions from the  $V_{inbuf}$  ( $V_I$ ) and  $V_{out}$  ( $V_Q$ ) nodes to the gate voltage  $V_g$ :

$$\begin{aligned} H_I(s) &\equiv \frac{V_g}{V_I} = \frac{1}{1 + \frac{R_v + 1/sC_c}{R_b \|(1/s[C_{gs1} + C_{gd1} + C_d])}} = \frac{1}{1 + \frac{Z_s}{Z_L}} \\ H_Q(s) &\equiv \frac{V_g}{V_Q} = \frac{1}{1 + \frac{1/sC_{gs1}}{R_b \|(1/s[C_{gd1} + C_d]) \|(R_v + 1/sC_c)}} \end{aligned} \quad (7.2)$$

Thus, the composite response is the ‘‘quadrature sum’’ of the two transfer functions:

$$V_g = H_I V_I + H_Q V_Q = \underbrace{(H_I - jH_Q)}_{H_{net}} V_I \quad (7.3)$$

In case (i) ( $R_v \ll R_b$ ), we define  $f_v \equiv 0.159/(R_v C_c) \gg f_b \equiv 0.159/(R_b [C_{gs1} + C_{gd1} + C_d])$ . For the component values in Table 7.1 and  $V_{tune}^{freq} = 1$  V for high-frequency,  $R_v^{-1} = K_p(V_{tune}^{freq} - V_{tp}) = 4.32\text{m}\Omega$ , so  $f_b = 71$  MHz and  $f_v = 3.8$  GHz, which indeed satisfies our assumption. Adding the two component transfer functions  $H_{I,Q}$  in quadrature yields Fig. 7.2. The net response is hence roughly a first-order high pass magnitude with a two-pole phase response. For the component values in Table 7.1 and approximating  $C_{gs1} \approx \frac{4}{5}C_{ox}(WL)_1$  and  $C_{gd1} \approx \frac{1}{5}C_{ox}(WL)_1$ , the pass-band gains of  $H_I$  and  $H_Q$  are  $\left(1 + \frac{C_{gs1} + C_{gd1} + C_d}{C_c}\right)^{-1} \approx -4.19$  dB and  $\left(1 + \frac{C_{gd1} + C_d}{C_{gs1}}\right)^{-1} \approx -2.58$  dB, respectively, so we can approximate  $|H_{net}| \approx -3$  dB and  $\angle H_{net} \approx -\arctan\left(\frac{f}{f_2}\right)$ ,  $f_2 = \frac{0.159}{R_v C_c \|[C_{gs1} + C_{gd1} + C_d]}$ .

In case (ii) ( $R_v \gg R_b$ ), the analysis is similar, except now  $f_v \ll f_b$ . It can be shown that the net response takes the same form as before except now,  $f_2 = \frac{0.159}{R_b [C_{gs1} + C_{gd1} + C_d]}$ , so the phase response is not sensitive to  $R_v$ . Because our frequency-tuning scheme depends on adjusting the phase shift into the buffer cell, we must ensure  $R_v \leq R_b$  so the tuning response remains a strong function of  $R_v$ .

**Table 7.1:** Proposed-MRO Component and Parasitic Values

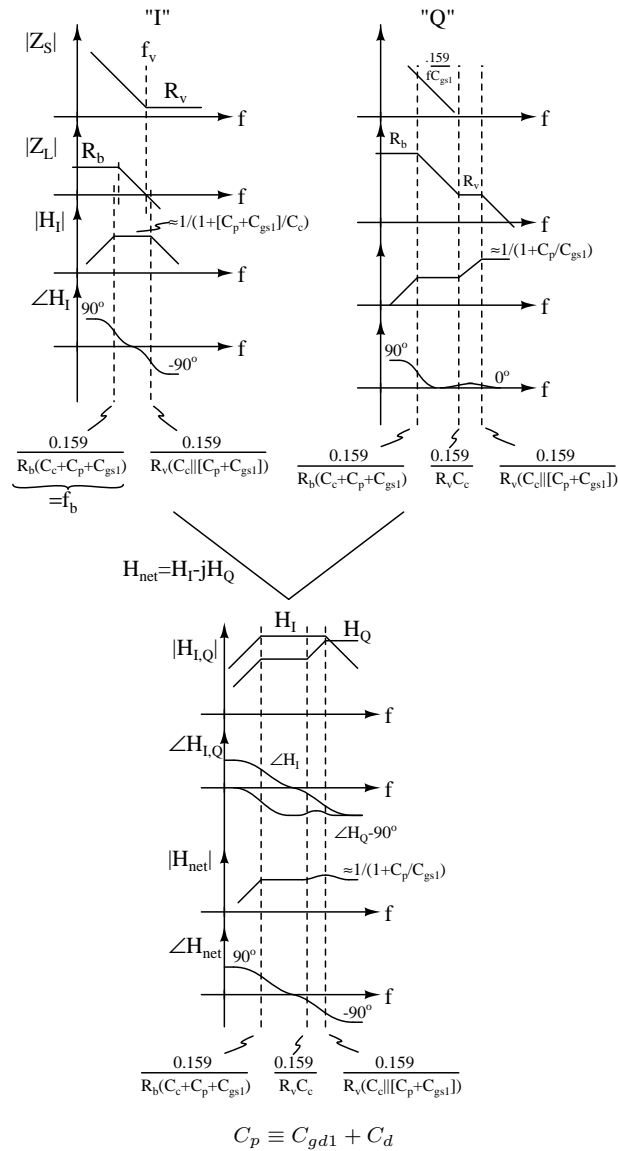
$R_b$	[k $\Omega$ ]	20
$R_g$	[k $\Omega$ ]	5.74
$C_c$	[fF]	180.1
$C_{opbuf}$	[fF]	50
$K_p$	[mA/V <sup>2</sup> ]	5.43
$(W/L)_p$	[ $\mu\text{m}/\mu\text{m}$ ]	8(.8/.09)
$V_{tp}$	[V]	0.205
$C_{oxP}$	[fF/ $\mu\text{m}^2$ ]	14
$C_{d/s}$	[fF]	8
$K_1$	[mA/V <sup>2</sup> ]	131.8
$(W/L)_1$	[ $\mu\text{m}/\mu\text{m}$ ]	48(1.5/.09)
$V_{t1}$	[V]	0.3165
$K_2$	[mA/V <sup>2</sup> ]	65.92
$(W/L)_2$	[ $\mu\text{m}/\mu\text{m}$ ]	24(1.5/.09)
$V_{t2}$	[V]	0.2743
$C_{oxn}$	[fF/ $\mu\text{m}^2$ ]	16
$V_A$	[V]	1.05
$K_x \equiv \mu_x C_{ox} \left(\frac{W}{L}\right)_x$		

### 7.1.2 Buffer/Latch Nonlinear Analysis

#### Overview

Next, to determine the steady-state frequency of oscillation, we consider the nonlinear buffer/latch component of the delay cell. Substituting the results for the phase-shift network shown in Fig. 4.3(a), approximating the equivalent lumped capacitance to ground seen by the delay cell  $C_L$  as

$$C_L \approx C_{opbuf} + C_{gs2} + 4C_{gd2} + C_{gs1} || (C_c + C_{gd1} + C_d) + C_c || (C_{gs1} + C_{gd1} + C_d) \quad (7.4)$$



**Figure 7.2.:** Phase-Shift Network Response:  $H_{net} = H_I - jH_Q$  “Algebra on the Graph” (case (i) shown)

and performing harmonic balance (HB) analysis with a modified square-law model of the FETs, we will obtain the oscillation frequency:

$$f_{osc} \approx \frac{f_2}{1 + \frac{f_2}{f_0}} \tag{7.5}$$

where

$$f_0 = 0.159 \frac{K_1}{C_L} (V_b - V_{DC} - V_{t1}) \left( 1 + \frac{V_{DD}}{V_A} \right) \frac{|H|}{\sqrt{2}} \quad (7.6)$$

in which  $|H| \approx 0.707$ ;  $K_1 = \mu_n C_{ox} \left(\frac{W}{L}\right)_1$ ;  $V_{DC}$  is the DC level of the oscillator waveform (derived in Section 7.1);  $V_{t1}$  is the threshold voltage of M1; and  $V_A$  is the ‘‘Early Voltage’’ s.t.  $r_{ds1} = \frac{V_A}{I_D}$  [224].

### Details

Examining Fig. 4.3(a), and exploiting the quadrature symmetry of the circuit as described by (5.1), we have the following single-harmonic approximation for the node voltages:

$$\begin{aligned} V_I(\theta) &= V_{DC} + V_{osc} \cos(\theta + 90^\circ) \\ V_g(\theta) &= V_b + |H(f_{osc})| V_{osc} \cos(\theta + 90^\circ + \angle H(f_{osc})) \\ V_{Q,QB}(\theta) &= V_{DC} \pm V_{osc} \cos(\theta) \end{aligned} \quad (7.7)$$

where  $V_{osc}$  denotes the fundamental amplitude of oscillation,  $H(f_{osc}) = H_{net}(f_{osc})$  from (7.3), and  $V_{DC}$  denotes the DC level of the oscillator output voltages.

Applying Kirchoff’s Current Law (KCL) to the  $V_{out}$  node in the delay-cell inset of Fig. 4.2,

$$\begin{aligned} C_L \frac{d}{dt} V_Q - \frac{K_1}{2} (V_g - V_Q - V_{T1})^2 \left( 1 + \frac{V_{DD} - V_Q}{V_A} \right) \\ + K_2 f_{mos}(V_{DC} - V_{t2}, V_{QB}, V_{t2} + V_Q) = 0 \end{aligned} \quad (7.8)$$

where  $V_{g,Q,QB}$  are given above,  $V_A$  denotes the ‘‘Early Voltage’’ s.t.  $r_{ds} \equiv V_A/I_D$ , and  $f_{mos}$  is a function to model transistor drain current at the edge of the triode and saturation regions (explained below).

To model the behavior of a transistor at the edge of triode and saturation, we note that the square-law model for a MOSFET, neglecting channel-length modulation and short-

channel effects, can be written as  $I_D = K (V_{ov} V_x - \frac{1}{2} V_x^2)$ , where  $V_{ov} \equiv V_{gs} - V_T$  and  $V_x = \min(V_{ov}, V_{ds})$ . Approximating  $\min(x, y) \approx \sqrt{xy}$ , we can write

$$I_D \approx K V_{ov} \left( \sqrt{V_{ov} V_{ds}} - \frac{1}{2} V_{ds} \right) \approx K f_{mos}(V_0, \Delta V_{ov}, \Delta V_{ds}) \equiv \sum_{i,j} a_{i,j} \frac{(\Delta V_{ov})^i}{i!} \frac{(\Delta V_{ds})^j}{j!} \quad (7.9)$$

at the border between triode and saturation, where  $a_{ij} \equiv \frac{\partial^{i+j} I_D}{\partial V_{ov}^i \partial V_{ds}^j}$  are Taylor-series coefficients evaluated about  $V_{ds} = V_{ov} = V_0$ . Substituting up to 3<sup>rd</sup>-order Taylor-series terms to be able to find the oscillation amplitude [28] and performing HB analysis [225], we obtain the fundamental-component:

$$\begin{aligned} & -\frac{K_1 \mu_x V_{osc}}{2} [V_b - V_{DC} - V_{T1}] \left[ 1 + \frac{V_{DD}}{V_A} \right] \\ & -\frac{K_1 \mu_x^2 V_{osc}^3}{2 \cdot 8 \cdot V_A} \\ & -\frac{K_2}{2} (V_{DC} - \frac{V_{t2}}{2}) V_{osc} \\ & + \frac{K_2 V_{osc}}{V_{DC} - V_{t2}} \left[ \frac{9}{64} V_{osc}^2 + \frac{3}{16} V_{t2}^2 \right] \\ & + \frac{j 2\pi f_{osc} C_L V_{osc}}{2} \\ & = 0 \end{aligned} \quad (7.10)$$

$$\mu_x \equiv jH(f_{osc}) - 1 \quad (7.11)$$

Substituting  $H_{net}(f_{osc})$  from (7.3) into (7.10), solving the imaginary part for the frequency yields (7.5), where the DC component is obtained from DC analysis (neglecting effect of even-order harmonics on the DC level):

$$V_{DC} \approx \frac{\sqrt{\frac{K_1}{K_2}} (V_b - V_{t1}) + V_{t2}}{1 + \sqrt{\frac{K_1}{K_2}}} \quad (7.12)$$

Hence, with the values in Table 7.1 and using  $V_{tune}^{freq} = 0.25 \rightarrow 1V$ , we obtain

$f_{osc} \approx 0.159 \frac{K_p (V_{tune} - V_{tp})}{C_c || [C_{ox} n(WL)_1 + C_{d/s}]} = 0.564 \rightarrow 9.96 \text{ GHz}$ , which is within around 20% of the measured values (0.63-8.1 GHz). More importantly, the equation captures the  $f_{osc} - V_b - V_{cp}$



“plane” contour shape visible in the measured curve of Fig. 7.17(a), so we have the proper trends for design.

## 7.2 Supply Sensitivity

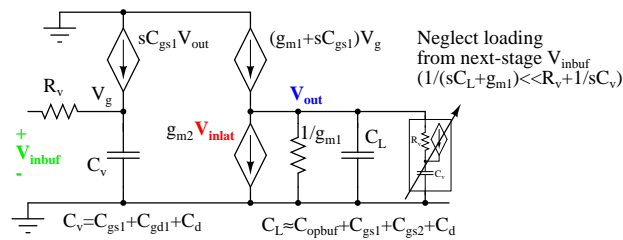
Based on the discussion in Section 6.1.4, the phase noise due to supply noise can be obtained by differentiating the expression for  $f_{osc}$  with respect to  $V_{DD}$  to obtain the equivalent VCO gain. To obtain a normalized metric of the oscillator frequency’s sensitivity to the supply voltage, we then multiply by the supply voltage and divide by the nominal oscillation frequency:

$$\text{Static Sensitivity} \equiv \frac{V_{DD}}{f_{osc}} \frac{\partial f_{osc}}{\partial V_{DD}} \approx \frac{f_{osc}}{f_0} \frac{1}{1 + \frac{V_A}{V_{DD}}} \quad (7.13)$$

Therefore, as we predicted intuitively in Section 4, the output resistance  $r_{ds} = \frac{V_A}{I_D}$  of the transistor improves supply rejection.

## 7.3 Startup Analysis

To answer the question of startup, consider the model of the delay cell in Fig. 4.3(a); for simplicity we assume coupling capacitor  $C_c = \infty$ ,  $R_b = \infty$ , and  $C_{gd2} \approx 0$ . By



**Figure 7.3.:** Oscillator Startup Analysis: Delay-Cell Simplified LTI model

symmetry of the structure and performing equivalent circuit analysis, we obtain Fig. 7.3. We hence obtain the following “equivalent unilateral gains:”

$$\begin{aligned}
V_{out} &= \frac{\frac{1 + \frac{sC_{gs1}}{g_{m1}}}{1 + sC_v R_v} V_{inbuf} - \frac{g_{m2}}{g_{m1}} V_{inlat}}{\left(1 + \frac{sC_L}{g_{m1}}\right) \left(1 - \frac{1 + \frac{sC_{gs1}}{g_{m1}}}{1 + sC_v R_v} \frac{sC_{gs1} R_v}{1 + \frac{sC_L}{g_{m1}}}\right)} \\
&\approx \frac{\frac{1}{1 + \frac{s}{\omega_2}} V_{inbuf} - r V_{inlat}}{\left(1 + \frac{s}{\omega_0}\right) \left(1 - \frac{\frac{s}{\omega_2}}{\left(1 + \frac{s}{\omega_2}\right) \left(1 + \frac{s}{\omega_0}\right)}\right)} \\
&= \underbrace{\frac{1}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0 \omega_2}}}_{H_{buf}(s)} V_{inbuf} - \underbrace{\frac{r \left(1 + \frac{s}{\omega_2}\right)}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0 \omega_2}}}_{H_{lat}(s)} V_{inlat}
\end{aligned} \tag{7.14}$$

where  $C_v$  and  $C_L$  are indicated in Fig. 7.3; the relative latch strength  $r \equiv \frac{g_{m2}}{g_{m1}}$ ; and we have neglected the  $\frac{sC_{gs1}}{g_{m1}}$  terms because we assume  $\omega_2 \equiv (R_v C_v)^{-1} < \omega_0 \equiv \frac{g_{m1}}{C_L}$  and  $\omega_2 \ll \frac{g_{m1}}{C_{gs1}}$ .

Examining the delay-cell connections in Fig. 4.2, we obtain

$$\begin{pmatrix} 1 & 0 & H_{lat}(s) & -H_{buf}(s) \\ -H_{buf}(s) & 1 & 0 & H_{lat}(s) \\ H_{lat}(s) & -H_{buf}(s) & 1 & 0 \\ 0 & H_{lat}(s) & -H_{buf}(s) & 1 \end{pmatrix} \begin{pmatrix} V_I \\ V_Q \\ V_{IB} \\ V_{QB} \end{pmatrix} = A(s) \vec{v} = \vec{0} \tag{7.15}$$

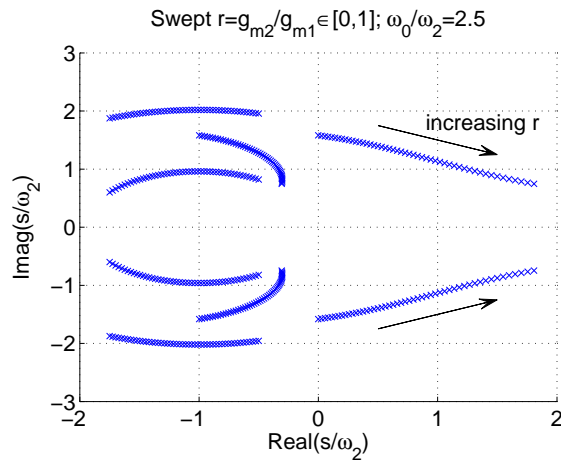
Computing the determinant yields the following characteristic equation for the system poles:

$$(1 - H_{lat}^2(s))^2 + H_{buf}^2(s) (4H_{lat}(s) - H_{buf}^2(s)) = 0 \tag{7.16}$$

To determine the range of latch strengths that allow reliable startup, we set  $\frac{\omega_0}{\omega_2} = 2.5$  based on the discussion in Section 7.4.1 and sweep the relative latch strength  $r$ .<sup>1</sup> Fig. 7.4 plots the root locus obtained from setting  $\det A(s) = 0$  in (7.15) for relative latch strength

<sup>1</sup>We also modify  $H_{buf}(s)$  to include an attenuation term  $m = -4$  dB to account for attenuation from  $C_c < \infty$  and other unmodeled parasitics based on the analysis in Section 7.1.2.

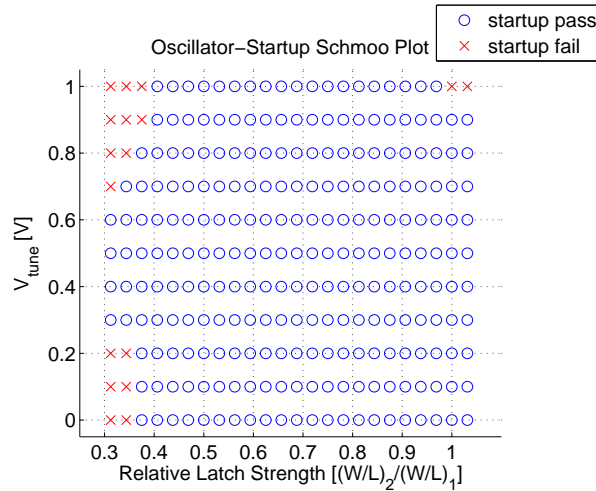
$r \in [0, 1]$ . For  $r \approx 0$  (no latch), we see that the poles are barely in the LHP, while for larger



**Figure 7.4.:** Oscillator Startup: Root Locus for Relative Latch Strength  $r \in [0, 1]$

$r$ , the complex-conjugate poles move further into the RHP (allowing startup). In addition, the imaginary part decreases, possibly indicating a reduced oscillation frequency.

However, too large a value of  $r$  could also damp oscillation, even though the above small-signal analysis does not show it. Intuitively, if the latch is too strong, the buffer cannot overpower it to turn around the waveform at the peaks and sustain oscillation. Fig. 7.5 displays a schmo plot from transistor-level SPECTRE simulations indicating whether the oscillation starts for different latch sizes and tuning-voltage values. From the plot, we see that between  $r > 0.4$  and  $r < 1.0$ , the oscillator successfully starts. Also, from simulation the maximum oscillation frequency decreases from around 9 GHz near  $r = 0.4$  to 2.5 GHz for  $r = 1.0$ , consistent with the small-signal-analysis trend predictions above. Therefore, we select  $r = 1/2$  for margin, higher oscillation frequency, and ease of common-centroid/interdigitized layout as discussed in Section 7.4.1.



**Figure 7.5.:** Oscillator Startup: Transistor-Level SPECTRE Simulation Schmo Plot

## 7.4 Transistor-Level Design of the Proposed MRO

### 7.4.1 Source-Follower/Latch Design

To operate the oscillator at high frequency, we use the simplest possible buffer and latch cells – a single-transistor NMOS source-follower buffer and a single NMOS latch transistor. We size the transistors at minimum length ( $L=90\text{nm}$  in this prototype) also to maximize speed performance. If flicker noise is a greater concern than speed, larger lengths could be employed. We select the transistor aspect ratio  $(\frac{W}{L}) \leftrightarrow K$  so that  $f_0$  from (7.6) satisfies  $f_0 \geq 2.5f_{osc}^{max}$  so that  $f_{osc}$  is a strong function of  $f_2$  (given in (7.1)) for a good tuning response.

To determine the relative size of the latch and buffer transistors  $r \equiv \frac{(W/L)_2}{(W/L)_1}$ , we note that intuitively, the relative latch strength  $r$  must be  $> 0$  for startup to provide the additional regenerative feedback for the circuit to oscillate. However, relative latch strength should be  $< 1$  because the buffer must be able to drive the latch. We select  $r = 1/2$  as a mid-point value because larger latch size also tends to reduce the frequency due to increase in

parasitic loading. Transistor-level SPECTRE simulation shows that relative latch strength  $> 0.4$  and  $< 1$  successfully starts up (for details as well as small-signal analysis, see Section 7.3). Thus, choosing  $r = 0.5$  provides margin, and this ratio of 1:2 also allows for simple interdigitized, common-centroid layout of the latch/buffer transistors.

#### 7.4.2 Phase-Shift/Bias Network Design

Designing the phase-shift/bias network shown in Fig. 4.3(a) and (b) determines the high-frequency performance of the oscillator, requiring minimal parasitics. The following sections discuss its tradeoffs.

##### Phase-Shift Variable Resistor $R_v$

The variable resistor  $R_v$  is implemented with a PMOS transistor in triode as shown in Fig. 4.3(b). Adjusting the differential control voltage  $V_{tune}^{freq} = V_b - V_{cp}$  changes the (triode) resistance

$R_v \approx \left[ \mu_p C_{ox} \left( \frac{W}{L} \right)_p \left( V_{tune}^{freq} - V_{tp} \right) \right]^{-1}$  before arriving at the gate of the source follower. As indicated in (7.5), modifying this phase shift changes the frequency of oscillation. Smaller resistance (requiring a wider PMOS transistor) tends to yield a higher frequency; however, the PMOS transistor should be sized appreciably smaller than the source follower and latch transistor (e.g.  $(W/L)_p \approx 0.1 \times (W/L)_1$ ), lest its parasitic capacitance load the preceding source-follower stage and reduce the oscillation frequency.

##### Bias Resistor $R_b$ and Coupling Capacitor $C_c$

We bias the source-follower transistor at  $V_b$  through a large-value resistor  $R_b$ . The resistor  $R_b$  should be sufficiently large so that  $R_b \gg R_v$  to have a good tuning characteristic (cf. Section 7.1) but not so large that it would contribute parasitic capacitance to the

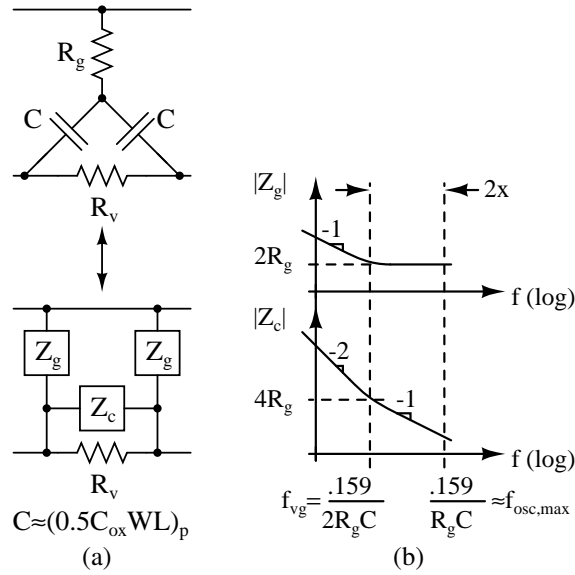
substrate or consume excessive area. The source follower is AC coupled to the preceding stage's output node through  $C_c$  so that it can be biased in saturation. Since "MIMCAPs" (metal-insulator-metal capacitors) are not available in this pure logic process, we select  $C_c$  to be a "MOMCAP" (metal-oxide-metal capacitor) formed by a fingered hairpin structure using the inter-layer dielectric (ILD). Though making the coupling capacitor larger ideally eliminates its impact on the oscillation frequency, it also creates more parasitic capacitance to the substrate, which could load the oscillator and lower the oscillation frequency. The coupling capacitor is therefore increased to the point where its parasitic capacitance to ground (roughly 5% of the desired floating capacitance in our case) is on the order of the parasitic drain capacitance of the PMOS transistor MP in Fig. 4.3(b).

#### Bias Resistor $R_g$

To reduce the loading effects of the gate capacitance of the PMOS transistor MP, we add a resistor  $R_g$  in series with the gate as shown in Fig. 4.3(b). The resistor has the added benefit of creating a low-pass filter with the gate capacitance, so in a typical PLL, the resistor could help filter high-frequency noise from the charge pump. We select  $R_g \approx \frac{0.159}{f_{osc}^{max}(0.5C_{ox}WL)_p}$  ( $\approx 4k\Omega$  in our case) so that at the maximum oscillation frequency the resistor's value is roughly equal to the (triode) gate-drain/source reactance. To visualize the effect on loading from the resistor  $R_g$ , we apply the Wye-Delta transform as shown in Fig. 7.6(a). Fig. 7.6(b) illustrates the equivalent "grounded" and "coupling" parasitics  $Z_g$  and  $Z_c$ , respectively, which are given by

$$Z_g = 2R_g \left( 1 + \frac{1}{2R_g C_s} \right), \quad Z_c = \frac{2}{sC} \left( 1 + \frac{1}{2R_g C_s} \right) \quad (7.17)$$

where  $C \equiv 0.5(C_{ox}WL)_p$ . Assuming the control node is grounded (e.g. large capacitor from a PLL loop filter or low-impedance buffer), the impedance to ground is increased (i.e. less loading) from  $0.159/(f_{osc}C)$  to  $2R_g$  for  $f > f_{vg} \equiv 0.159/(2R_gC)$  (see Fig.



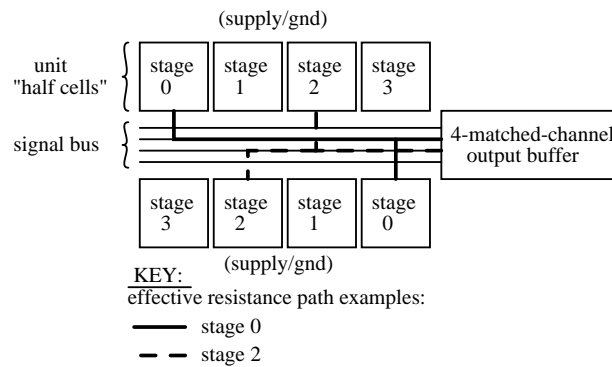
**Figure 7.6.:**  $R_g$  (of Fig. 4.3(b)) Parasitic Effects: (a) Wye-Delta Transform, (b)  $Z_{g,c}$  Frequency Response

7.6(b)), while there is some additional parasitic coupling on the order of  $(2 \rightarrow 4)R_g$  for  $f \in [1, 2]f_{vg}$ . Because  $f_{vg} \approx f_{osc}^{max}/2$  by design, and for large  $f_{osc}$ ,  $R_v$  is typically small ( $< 1k\Omega$  in our design), the additional coupling parasitics for  $R_g \geq 4k\Omega$  are negligible. Though even larger  $R_g$  would in principle provide less loading, making  $R_g$  too large could introduce parasitic capacitance from the resistor itself and could slow down the VCO's response to the tuning voltage.

Also, dummy transistors (not shown in Fig. 4.3) are placed at the edge of the PMOS transistor to reduce variability among stages and to mitigate stresses due to shallow-trench-isolation (STI) oxides [226]. We selected a larger number of fingers (8 strips) so the unit finger is smaller, and hence the parasitics from the dummy transistors do not significantly contribute to the response.

## 7.5 Layout Considerations

To minimize phase imbalance and maintain symmetry, the layout of the multi-loop ring oscillator should have identical routing parasitics for each delay stage [6]. Furthermore, we want commensurate supply routing so that supply noise at frequencies near non-integer multiples of  $N_{stage} \times f_{osc}$  is rejected [107]. To maintain this required symmetry in the presence of complex multi-loop structures, we propose a layout technique based on the generalized delay cell viewpoint discussed in Section 5.1. Given the unit delay cell of Fig. 4.3(b), we need only to connect the ports to the appropriate output bus line to maintain the desired phase relationship. To cancel process gradients to the first order, we split each unit delay cell in half and arrange them in a cross-coupled pattern with the output signal bus in the center as shown in Fig. 7.7; Fig. 7.8 indicates the corresponding signal connection scheme. The signal bus then feeds directly into a 4-matched-channel output open-drain



**Figure 7.7.:** Routing Floorplan Sketch

buffer whose layout follows a similar pattern to preserve I/Q channel matching. This cross-coupled arrangement helps to cancel first-order process and stress gradients, and moreover, the oscillator output nodes have no systematic error due to routing capacitance, i.e. drawing an analogy to the single-loop case, we avoid the asymmetric “wrap-around” wire connecting the Nth stage to the first. Fig. 7.9 displays the die micrograph of the proposed oscillator demonstrating the proposed layout technique described above.

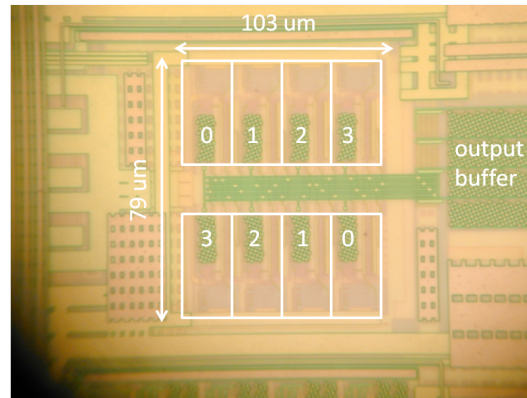


unit half cells →		0						1						2						3					
		-	B	-	L	-	O	-	B	-	L	-	O	-	B	-	L	-	O	-	B	-	L	-	O
signal bus	I		*	*							*					*			*			*			
	IB					*		*		*				*	*				*			*		*	
	Q	*				*			*				*			*			*		*		*		
	QB				*				*		*		*		*		*		*		*		*		
unit half cells →		B - L - O -						B - L - O -						B - L - O -						B - L - O -					
		3						2						1						0					

**KEY**

0-3	I	IB	Q	QB	B	L	O	-
“stage” 0-3	$V_I$	$V_{IB}$	$V_Q$	$V_{QB}$	$V_{inbuf}$	$V_{inlat}$	$V_{out}$	no connect

**Figure 7.8.:** Routing Connection Scheme



**Figure 7.9.:** Die Micrograph of Proposed Quadrature Oscillator

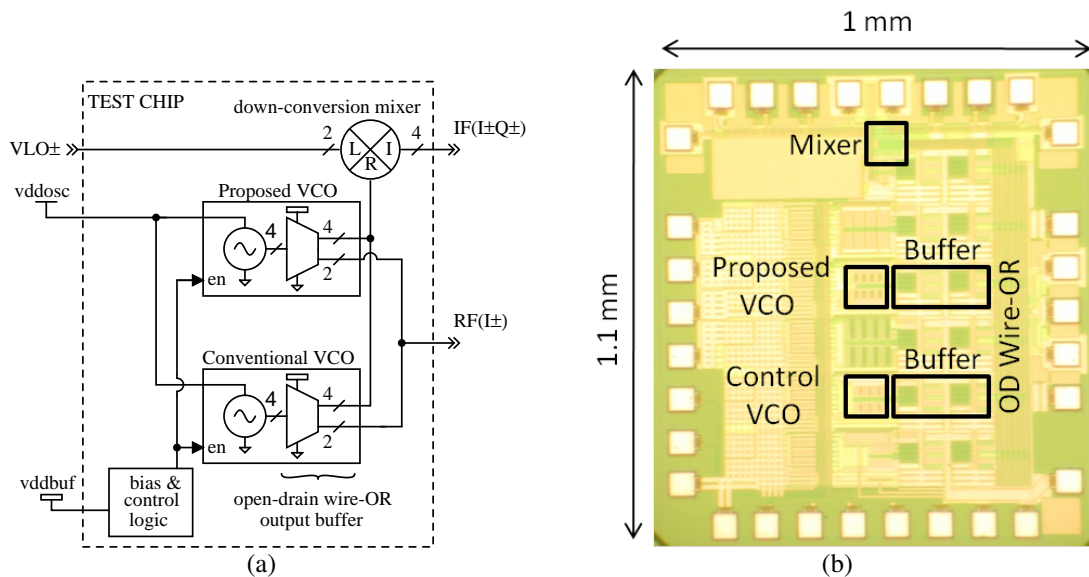
Some residual systematic mismatch exists due to differing parasitic wire resistance as indicated by the dark solid and dashed lines in Fig. 7.7. The effect is mitigated due to the cross-coupled arrangement, and we use upper metal (7-8 of a 9-metal process) to have lower sheet resistance. We also strap two adjacent metal layers together to reduce resistance further. There is a tradeoff in speed to use this layout technique. We simulated the layout parasitic extracted (LPE) output buffer for two cases: (1) laid out with separate channels (standard technique) and (2) laid out with the proposed technique, and the 3-dB frequency reduced from 10.1GHz to 9.0GHz. Minimum-width ground wires are placed around the signal wires to isolate the different channels, and signals are ordered so that to the extent possible, the next adjacent signal wire is 180 degrees out of phase to obtain differential signalling, as indicated in Fig. 7.8. In LPE simulations of the output buffer, we see channel-to-channel isolation between 32-40dB; for instance, LPE simulations show that applying a 347mV step at one channel yields a parasitic glitch of roughly 3.5mV in the adjacent channel. The proposed and conventional quadrature oscillators are both laid out using this technique, and occupy roughly the same area:  $103 \times 79$  and  $88 \times 69 \mu\text{m}^2$ , respectively.

Finally, we note that this layout technique could be applied to more complex multi-loop structures, and the routing area only scales with the number of output phases, not

with the number of loops. The complexity of the layout is hence no longer a function of the complexity of the multi-loop-oscillator ring structures. This is important because a unit delay cell with  $M$  ports can be designed to achieve either improved supply rejection as shown in this paper or to obtain increased frequency [11], and the layout effort to implement these structures remains quite straightforward and systematic.

## 7.6 Experimental Results

The proposed oscillator of Fig. 4.2 and the conventional CMOS-delay-cell quadrature oscillator in Fig. 4.1 are fabricated on the same test chip for more meaningful comparison at the same technology node, United Microelectronics Corporation (UMC) 90nm logic CMOS with no analog features, as shown in Fig. 7.10(a) and 7.10(b). The conventional



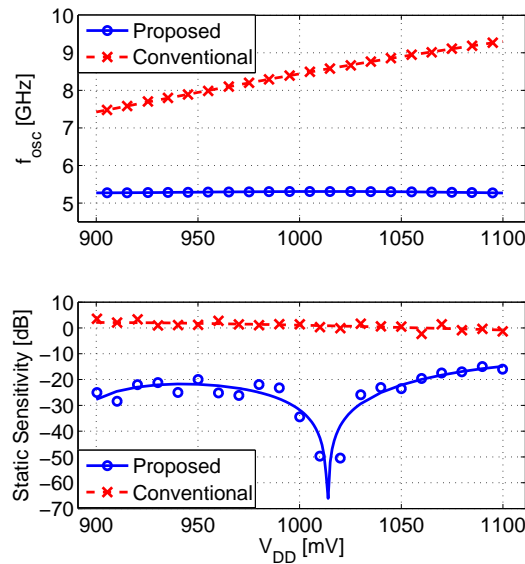
**Figure 7.10.:** (a) Test Circuitry on Chip for Multiple Oscillators (b) Corresponding Die Micrograph

oscillator serves as a control case to evaluate the supply-rejection performance. Each oscillator drives a 4-channel matched output buffer that can either output two differential

oscillator waveforms at full rate, or can output all four quadrature signals through a down-conversion mixer as shown in Fig. 7.10(a). The buffers and the dual I/Q mixers are laid out using the same principles as the quadrature oscillator described in the previous section to ensure that I/Q (+/-) channels are matched. Fig. 7.10(b) shows the die micrograph of the test chip. The chip was encapsulated in a QFN24 package, and measurements were performed on the two open-loop VCOs (proposed and conventional).

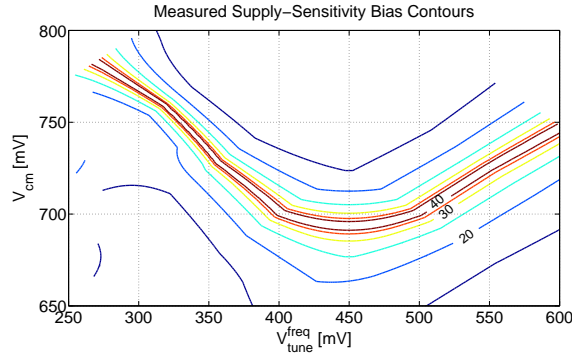
### 7.6.1 Supply Rejection

Fig. 7.11 compares the measured supply sensitivity of the proposed oscillator to that of the conventional-CMOS-delay-cell quadrature oscillator fabricated alongside (cf. conventional schematic in Fig. 4.1). At  $V_{DD}=1V$ , the proposed oscillator achieves static sup-



**Figure 7.11.:** Measured Supply Rejection: Comparison of Proposed and Conventional Oscillator Delay Cells:  $f_{osc}$  and Static Sensitivity ( $\equiv \frac{V_{DD}}{f_{osc}} \frac{\partial f_{osc}}{\partial V_{DD}}$ ) v.  $V_{DD}$

ply sensitivity of 0.019 [%-change  $f_{osc}$ /%-change  $V_{DD}$ ] (-34 dB) compared to 1.176 %/% (1 dB) for the conventional CMOS inverter-based delay cell. The proposed oscillator also

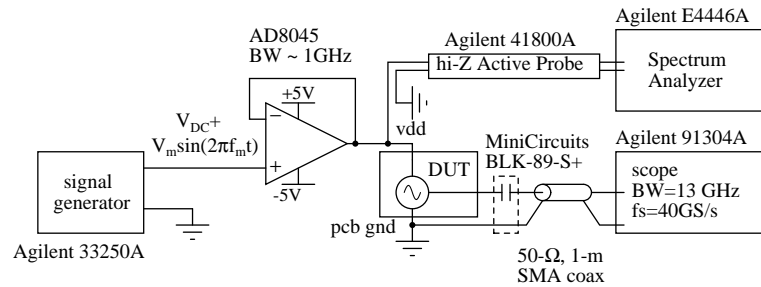


**Figure 7.12.:** Measured Static-Sensitivity [dB] Contour Plot v.  $V_{tune}^{freq}$  v.  $V_{cm}$

attains a minimum measured sensitivity of 0.003 %/‰ (-50 dB) at  $V_{DD}=1.02V$ . The sensitivity curve is obtained by sweeping  $V_{DD}$  with a step size of 10 mV. The slope of the proposed oscillator's frequency varies from -0.86 to 0.24 GHz/V when  $V_{DD}$  varies from 900 to 1100 mV, while that of the conventional delay cell varies from 7.72 to 10.53 GHz/V over the same range. The proposed multiloop ring oscillator topology is hence capable of >20 dB improvement in supply rejection over conventional ring topologies. Furthermore, as discussed in [98, 127], calibration of the supply level is also possible, so improved supply rejection could if desired be achieved by adjusting the supply voltage near the local extremum shown in Fig. 7.11.

We also characterized the variation in supply sensitivity over the oscillator's tuning range and with respect to the common-mode level  $V_{cm} \equiv \frac{1}{2} (V_b + V_{cp})$ . Fig. 7.12 displays the measured contour plot showing the supply sensitivity levels varying from -15dB to -40 dB in steps of 5 dB. The v-shaped curve illustrated on the figure indicates the required common-mode bias to obtain supply sensitivity <-40dB. The common-mode-level bias circuit is not included in this prototype for simplicity; however, by employing appropriate common-mode bias, the measured data show that superior supply sensitivity below -40dB can be achieved across the VCO tuning range without any voltage regulator.

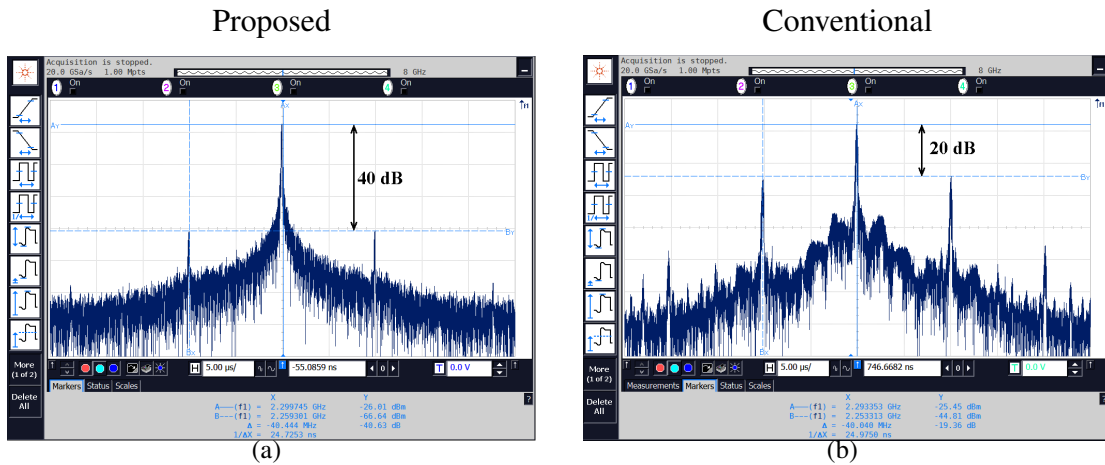
The proposed technique also displays improved dynamic supply rejection, or power-supply ripple rejection (PSRR). To measure the oscillator PSRR, we drive the power supply with a unity-gain opamp, which is driven by a sinusoidal voltage source, as shown in Fig. 7.13. We monitor the supply ripple reaching the device under test on a spectrum



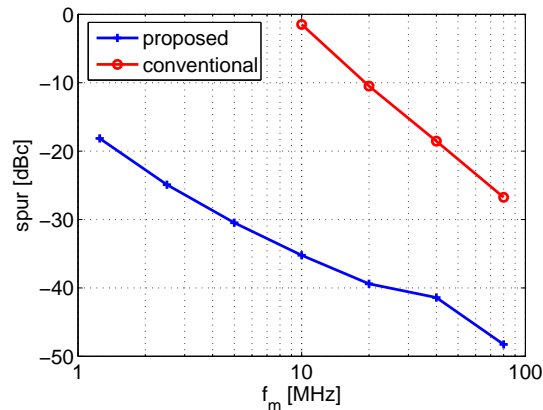
**Figure 7.13.:** Power-Supply-Ripple-Rejection Measurement Setup

analyzer through an active probe connected to the supply pin. We then measure the oscillator output voltage with a 40-GS/s oscilloscope and fast-Fourier-transform (FFT) the result to obtain the modulated spectrum. Measured modulated spectra for both the proposed and conventional CMOS oscillators are shown in Fig. 7.14(a) and Fig. 7.14(b), respectively, where the proposed oscillator provides 20 dB reduction in the spur due to supply modulation over the conventional oscillator. To compare the ripple rejection of the proposed oscillator to the conventional CMOS-inverter-based ring oscillator, we tune both to  $f_{osc}=2.31$  GHz and measure the sideband spur resulting from the supply-modulating tone for several modulation frequencies  $f_m$ <sup>2</sup>. As shown in Fig. 7.15, the proposed oscillator achieves superior ripple rejection over the conventional CMOS delay cell by a factor of more than 30 dB at  $f_m=10$  MHz and more than 20 dB for  $f_m=1.25$  to 80 MHz. While the PSRR curve does degrade at higher oscillation frequencies, as shown in Fig. 7.16, in all cases, the measured response of the proposed oscillator achieves improved ripple rejection over that of the conventional oscillator.

<sup>2</sup>We apply an approximately -58dBm signal to the supply pin to avoid large-signal-nonlinear frequency-modulation effects such as carrier nulling over as wide a range of modulation frequencies ( $f_m$ ) as possible when comparing to the conventional ring oscillator, which is highly sensitive to supply variations.



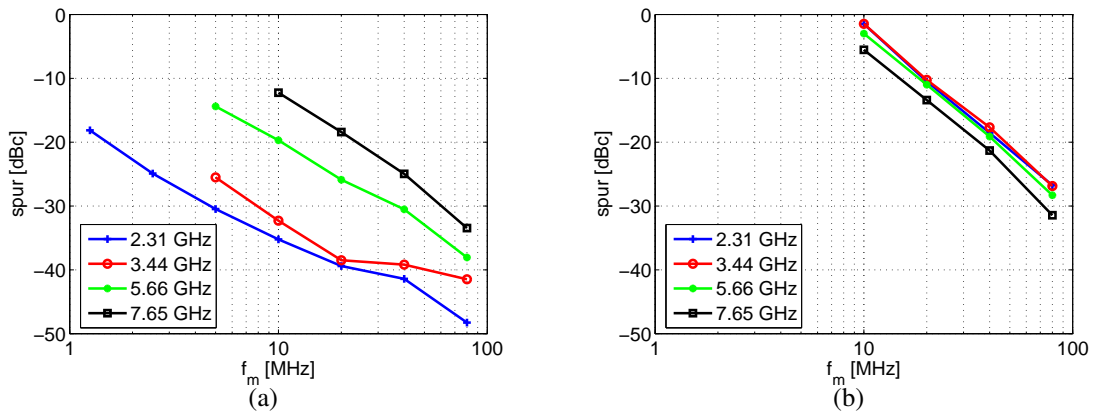
**Figure 7.14.:** Measured Modulated Spectrum of (a) Proposed Oscillator (-40 dB rejection at  $f_m=40\text{MHz}$ ) and (b) Conventional CMOS Oscillator (-20 dB rejection at  $f_m=40\text{MHz}$ )



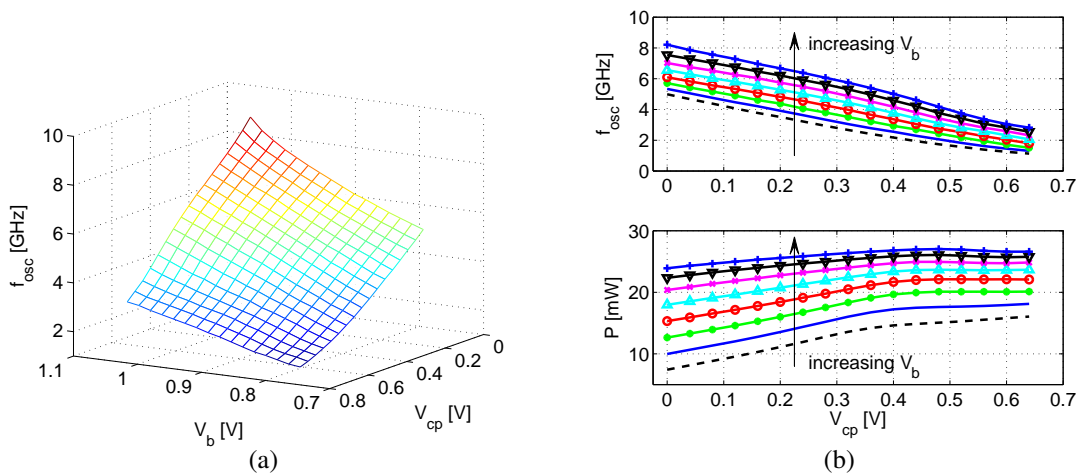
**Figure 7.15.:** Measured PSRR Sideband Spur: Proposed v. Conventional Quadrature Delay Cell for  $f_{osc}=2.31\text{GHz}$

## 7.6.2 Frequency Tuning

Fig. 7.17(a) displays the 3-D contour plot of the measured tuning response  $f_{osc}$  v.  $V_{cp}$  v.  $V_b$ . Tuning the frequency with differential control signal  $V_{tune} = V_b - V_{cp}$  could be employed to reject common-mode noise. Fig. 7.17(b) displays the equivalent family of curves for the 3-D contour and also indicates the corresponding power curves. Higher  $V_b$



**Figure 7.16.:** Measured PSRR (spur) v.  $f_m$  v.  $f_{osc}$  (inset legend indicates  $f_{osc}$ ): (a) Proposed, (b) Conventional



**Figure 7.17.:** Measured Frequency Tuning: (a)  $f_{osc}$  v.  $V_{cp}$  v.  $V_b$  (b) Equivalent Family of Curves and Power Information

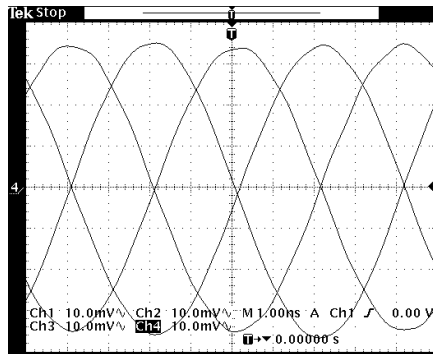
values yield increased power consumption because of the increased gate bias. Additionally, high oscillation frequency ( $>5$  GHz) is possible for  $P < 10$  mW at lower  $V_b$  values. From these data,  $K_{VCO} \approx 8.57$  GHz/V, and the overall tuning range is 0.63-8.1 GHz. The conventional oscillator displays a similar frequency range (0.536 to 8.5 GHz for  $V_{DD} = 0.35$



to 1.0V), and consumes 0.3 to 59 mW over that range. Hence, the proposed oscillator achieves comparable frequency-tuning range for about the same power consumption.

### 7.6.3 Quadrature Accuracy

Quadrature accuracy is required for CDRs employing either half-rate or frequency-discriminator-based architectures. The quadrature error is measured by downconverting the oscillator waveforms to roughly 125 MHz with the on-chip Gilbert-cell mixer, and recording the waveforms in an oscilloscope; Fig. 7.18 displays the measured downconverted quadrature waveforms. From these data, we compute the average difference in zero

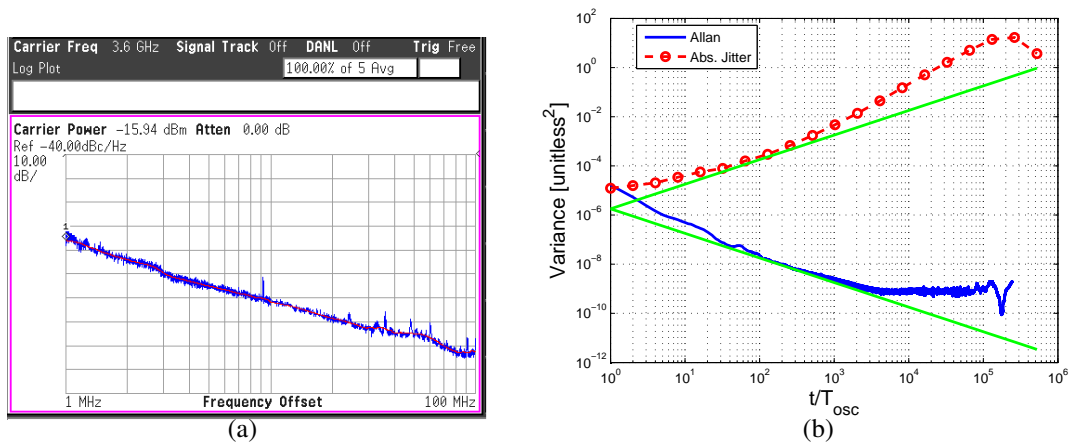


**Figure 7.18.:** Measured Quadrature Imbalance ( $1.98^\circ$ )

crossing of the I/Q waveforms and normalize to the downconverted period ( $1/(125\text{MHz}) \leftrightarrow 360^\circ$ ). Quadrature imbalance is measured to be less than 2 degrees without any trim at a frequency of  $\approx 1$  GHz. Measured quadrature error includes effects of mismatch from routing from oscillators to mixer and on PCB. The signal was downconverted on chip so that these routing errors and packaging/PCB imbalance would be relatively small.

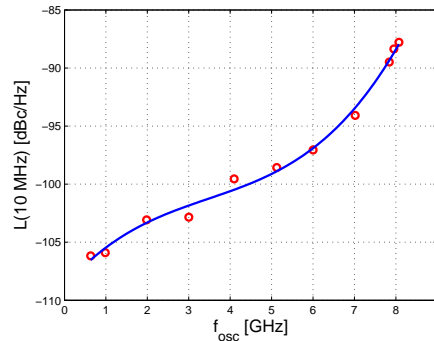
### 7.6.4 Phase-Noise

To characterize the phase-noise/jitter performance of the proposed oscillator, we perform both direct spectrum phase-noise measurements with the Agilent E4446A spectrum analyzer and perform time-interval-error (TIE) measurements with the Agilent DSA91304A oscilloscope. We postprocess the TIE measurements to compute both the Allan Variance [54] and an estimate of the absolute jitter [24]. Fig. 7.19(a)-(b) illustrate one such direct-spectrum measurement for  $f_{osc}=3.6$  GHz and the corresponding post-processed TIE data showing the Allan variance and absolute-jitter variance (normalized to the oscillation period). The horizontal axis of the jitter plot represents the spacing between TIE measure-



**Figure 7.19.:** Measured Phase-Noise Data: (a) Direct-Spectrum  $\mathcal{L}$  v.  $f_m$  (yields -100dBc/Hz at 10MHz) (b) Corresponding TIE Measurements: Allan-Variance/Absolute-Jitter Curves (yields -101 dBc/Hz at 10MHz)

ments normalized to the oscillation period. The diagonal lines correspond to best-fit  $\kappa^2$ , where  $\mathcal{L} = \kappa^2 \left( \frac{f_{osc}}{f_m} \right)^2$ . The phase-noise values across tuning range are obtained using measured TIE/Allan-variance data because the free-running oscillator drift makes direct-spectrum measurements less reliable at higher oscillation frequencies. Fig. 7.20 displays the variation of phase noise across the tuning range. At around 650MHz, the proposed



**Figure 7.20.:** Measured Phase Noise Variation across Tuning Range:  $\mathcal{L}(10 \text{ MHz})$  v.  $f_{osc}$

oscillator has a measured phase noise of  $-106\text{dBc/Hz}$  at  $10\text{MHz}$  offset, while the conventional oscillator has a phase noise of  $-119\text{dBc/Hz}$  at  $10\text{MHz}$  and the same oscillation frequency. In this design, we did not optimize the proposed oscillator for phase noise due to device noise, with the assumption that supply-noise-induced phase noise would be a larger concern than device-noise-induced phase noise.

### 7.6.5 Comparison

Table 7.2 compares the proposed oscillator supply-rejection performance to that of the conventional CMOS-delay-cell quadrature oscillator along with that of state-of-the-art ring-oscillator VCOs in the literature from the past 10 years. Our measured static-supply-sensitivity performance is among the best reported, and we have used no voltage regulator or PLL in the measured prototype. The table also indicates common supply-rejection improvement techniques employed by previous works, namely low-dropout-voltage (LDO) voltage regulation, compensation by adjusting positive/negative supply dependence to cancel each other (“Compensation”), calibration, fully-differential delay cells with tail current source, isolation of the VCO core with a high-impedance voltage-to-current converter (“ICO”), and replica-bias delay cells. By employing our proposed multiloop delay cell that intrinsically rejects the supply, the designer has the freedom either to use the oscilla-

**Table 7.2:** Supply-Rejection Comparison (Last 10 yr)

	Static Sensitivity ( $\equiv \frac{V_{DD}}{f_{osc}} \frac{\partial f_{osc}}{\partial V_{DD}}$ ) [%/%]	$f_{osc}$ [MHz]	$V_{DD}$ [V]	Tech. [ $\mu\text{m}$ ]	LDO	Compensation	Calibration	Diff. Delay	ICO	Replica Bias
<b>This Work</b>	<b>0.0030</b>	<b>5650</b>	<b>1</b>	<b>0.090</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
Conventional	1.579	5650	0.74	0.090	0	0	0	0	0	0
[22]	0.0200	1000	2.5	0.250	0	1	0	0	0	0
[20]	0.0077	5120	0.84	0.065	0	1	0	0	0	0
[98]	-1.1 to 0.5*	1400	1	0.130	0	1	1	0	0	0
[127]	0.0260**	1500	1.8	0.180	0	1	1	0	0	0
[105]	0.1450	900	3.3	0.350	0	0	0	0	0	0
[121]	0.0220	500	3.3	0.350	1	0	0	1	1	1

\* sens. after calibration not given; cal. range is -1.1 to 0.5 %/%, \*\* cal. step size is 0.026 %/%; cal. range is -0.4 to 0.4 %/%

tor alone without a regulator or to combine our approach with other techniques, such as regulation or calibration, to yield extremely low supply sensitivity. Additionally, we note that combining the proposed oscillator with a regulator would *not* entail placing the voltage regulator in the tuning loop, as the proposed oscillator is tuned by a separate phase-shift network. Hence, the voltage regulator could have low-frequency poles and hence consume less power than would a voltage regulator that needed to buffer the charge-pump voltage. Our technique hence supplements these existing methods. Finally, Table 7.3 summarizes the performance of the proposed oscillator.

**Table 7.3:** Proposed-Oscillator Performance Summary

Technology	90nm CMOS	
Area	[ $\mu\text{m}^2$ ]	103 $\times$ 79
Static Supply Sensitivity:		
minimum measured	[dB]	-50
over $\pm 10\% V_{DD}$ (0.9 to 1.1 V)	[dB]	-50 to -15
$V_{DD}$	[V]	1
Phase Noise @ $f_m=10$ MHz	[dBc/Hz]	-106 to -88
Freq. Tuning Range	[GHz]	0.63-8.1
Power	[mW]	7-26
Quadrature Accuracy	[deg.]	<2

## 8. CONCLUSION

This dissertation has discussed the theory, design, and measurement of multi-loop ring oscillators. In short, this work provides the following:

1. a design/analysis case study of MROs in sub-micron CMOS achieving improved supply rejection to combat the increasing levels of [switching] supply noise as well as illustrating a generalized-delay-cell viewpoint that simplifies MRO design and layout; and
2. a systematic, unified procedure for phase-noise analysis that furthermore catalogues and organizes previous phase-noise-analysis techniques, indicating their limitations and approximations, and illustrating their use with practical oscillator hand-calculation and numerical examples.

The merit of this work lies in enhancing the design of ring oscillators, which provide a central role in creating timing circuits for today's mobile devices as well as desktop computers.

We outlined the dichotomy of resonant and relaxation oscillators, describing the various flavors of ring oscillators including fully/pseudo differential and single ended as well as multi-loop/skewed-delay-based structures. This document also provided background on the nature of oscillator frequency error/spectral purity, and itemized the sources of these errors, especially supply noise.

Based on this discussion of previous MRO designs and the need for rejection of this supply noise, we next proposed an MRO architecture based on source-follower delay cells to improve supply-noise rejection. The appreciable switching activity in next-generation microprocessors and digitally-intensive integrated circuits necessitates this oscillator resilience to power-supply fluctuations. The source-follower arrangement isolates the supply through the output resistance of the transistor. Measurements have shown supply rejection

improvements in excess of 20dB over a conventional CMOS-inverter-based quadrature-oscillator delay-cell structure, and furthermore, a "sweet-spot" bias exists that allows even further reduction of supply sensitivity—ideally to zero incremental sensitivity. The multi-loop oscillator structure allows the source follower to oscillate by providing multiple paths: a source-follower path to isolate the supply and an inverting-latch path to provide regenerative positive feedback to sustain oscillation as demonstrated in this work.

The more complex nature of MROs compared to their single-loop equivalents further requires a systematic design and analysis approach, which we addressed with both a generalized-delay-cell viewpoint of MROs to facilitate their overall analysis, as well as a unified phase-noise analysis flow and organized comprehensive synopsis of techniques to apply within that flow. With these analysis-framework contributions, designers can systematically approach MRO analysis. We also presented a layout technique based on viewing the MRO as a collection of these M-port generalized delay cells with the ports connected to maintain a target phase relationship. This layout technique enables effective manufacturable production of ostensibly more complex oscillator configurations with substantially simplified layout effort. Furthermore, first-order process gradients can be partially compensated by splitting the unit delay cells into half-units and cross coupling.

Furthermore, the phase-noise-analysis-technique synopsis allows the designer to choose a phase-noise analysis method most suitable to the particular MRO delay cell and type of noise in question, providing both insight into how noise translates into oscillator phase noise in non-cookie-cutter oscillator structures as well as methods to perform hand calculations with suitable simplifications based on this intuition of which noise sources will be dominant.

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## APPENDIX A: MATH NOTATION

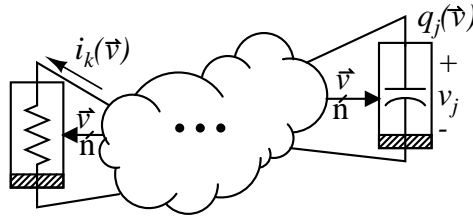
Table A.1 summarizes the math notation used throughout the document.

<b>Table A.1: Math Notation</b>	
<b>Definition</b>	
$\vec{v}$	$n_{rows} \times 1$ column vector
$\underline{M}$	$n_{rows} \times n_{cols}$ matrix
$\underline{M}^T$	transpose of $\underline{M}$
$\underline{M}^\dagger$	conjugate-transpose of $\underline{M}$
$\frac{\partial \vec{i}}{\partial \vec{v}}$	derivative of vector w.r.t. vector yields matrix
$\text{diag}(\dots)$	diagonal matrix with $(\dots)$ along main diagonal
$\mathcal{F}_{\tau \rightarrow f}(x(\tau))$	Fourier Transform: $X(f) \equiv \mathcal{F}_{\tau \rightarrow f}[x(\tau)] \equiv \int_{-\infty}^{\infty} d\tau \{x(\tau)e^{-2\pi j f \tau}\}$
$\mathbb{E}[x(t)]$	ensemble average of random process $x(t)$ : $\mathbb{E}[x(t)] \equiv \int_{-\infty}^{\infty} dx \{xp(x, t)\}$ , where $p(x, t)$ is the probability distribution of the process $x$ at time $t$ . N.B. average w.r.t. $x$ , NOT $t$ -i.e. ensemble average, NOT time average.
$R_x(t, \tau)$	Autocorrelation of random process $x(t)$ : $R_x(t, \tau) \equiv \mathbb{E}[x(t + \frac{\tau}{2})x(t - \frac{\tau}{2})]$
$S_x(f)$	"power" spectral density of random process $x$ ; <i>units</i> = $[(\text{units of } x)^2 / \text{Hz}]$ : $S_x(f) \equiv \lim_{T \rightarrow \infty} \mathbb{E} \left[ \frac{ \mathcal{F}_{\tau \rightarrow f}\{x(\tau)[u(\tau + \frac{T}{2}) - u(\tau - \frac{T}{2})]\} ^2}{T} \right]$ $= \mathcal{F}_{\tau \rightarrow f} \left\{ \lim_{T \rightarrow \infty} \int_{-T/2}^{T/2} \frac{dt}{T} \{R_x(t, \tau)\} \right\}$ where $T$ can be interpreted as the time over which the random process is measured and the final equality (the generalization of the Wiener-Khinchin-Einstein Theorem) holds so long as the process is approximately stationary.
$u(t)$	Heaviside unit step function: $u(t) \equiv \begin{cases} 1 & , t \geq 0 \\ 0 & , \text{else} \end{cases}$
$\delta(t)$	Dirac delta "function": $\forall \epsilon > 0, \int_{-\epsilon}^{\epsilon} dt \{f(t)\delta(t)\} = f(0)$
$\delta[k]$	Kroeneker delta function: $\delta[k] \equiv \begin{cases} 1 & , k = 0 \\ 0 & , \text{else} \end{cases}$

## APPENDIX B: PHASE-NOISE-CALCULATION PROCEDURES FOR ARBITRARY OSCILLATOR

The following sections trace through the methods to find the periodic steady-state solution and the phase noise spectrum for an “arbitrary” oscillator, illustrated conceptually in Fig. B.1. The polarized resistor/capacitor symbols represent n-terminal nonlinear transresistors and transcapsitors, i.e. the current/charge is nonlinearly related to n terminal voltages:

$$i_k(\vec{v}) = f_{I,k}^{nl_n}(v_1, \dots, v_n), \quad q_j(\vec{v}) = f_{Q,j}^{nl_n}(v_1, \dots, v_n) \quad (\text{B.1})$$



**Figure B.1:** Conceptual Arbitrary Oscillator

### B.1 PSS: Harmonic Balance

1. Write the node-voltage equations for an “arbitrary” oscillator such as Fig. B.1:

$$\vec{i}(\vec{v}(t), \vec{i}_{noise}(t)) + \frac{d}{dt} \vec{q}(\vec{v}(t)) = \vec{0} \quad (\text{B.2})$$

where  $\vec{i}$  and  $\vec{q}$  are  $n \times 1$  vectors denoting the device currents and charges at the  $n$  nodes and  $\vec{i}_{noise}$  is an  $m \times 1$  vector of noise currents. When  $\vec{i}_{noise} = \vec{0}$ , the oscillator runs in periodic steady state, and  $\vec{v}(t) = \vec{v}_{ss}(t)$ .



2. Expand the oscillation waveform in a Fourier series  $\vec{v}_{ss}(t) = \sum_{k=-\infty}^{\infty} \vec{V}_k e^{jk2\pi f_{osc}t}$ . Considering  $N_H$  harmonics, represent the  $n$  state variables (capacitor voltages/inductor currents) with the  $n(2N_H + 1) \times 1$  vector  $\vec{V}$ :

$$\vec{V}^T \equiv ( \underbrace{V_{c1}^{-N_H}, \dots, V_{cn}^{-N_H}}_{\text{(neg.) } N_H^{th} \text{ harmonic}}, \dots, \underbrace{V_{c1}^{-1}, \dots, V_{cn}^{-1}}_{\text{(neg.) fund.}}, \underbrace{V_{c1}^{DC}, \dots, V_{cn}^{DC}}_{\text{DC}}, \underbrace{V_{c1}^{+1}, \dots, V_{cn}^{+1}}_{\text{(pos.) fund.}}, \dots, \underbrace{V_{c1}^{+N_H}, \dots, V_{cn}^{+N_H}}_{\text{(pos.) } N_H^{th} \text{ harmonic}} ) \quad (\text{B.3})$$

where  $V_{ck}^m$  = the  $m^{th}$  harmonic of the  $k^{th}$  capacitor voltage. Because the oscillator is autonomous, one of the harmonic components' phases can be chosen arbitrarily, and the frequency of oscillation is solved for in its place.<sup>1</sup>

3. Hence, the frequency of oscillation and the harmonic components are obtained by solving the following nonlinear algebraic equation:

$$\vec{I}(\vec{V}) + 2\pi j f_{osc} \underline{K} \vec{Q}(\vec{V}) = \vec{0} \quad (\text{B.4})$$

which is the "frequency-domain" version of (B.2), and  $\underline{K}$  generates harmonic multiples of  $2\pi f_{osc}$ :

$$\underline{K} \equiv \text{diag}(-N_H, \dots, \underbrace{-1, \dots, -1}_{n \text{ elems}}, \underbrace{0, \dots, 0}_{n \text{ elems}}, \underbrace{+1, \dots, +1}_{n \text{ elems}}, \dots, +N_H) \quad (\text{B.5})$$

where the vectors  $\vec{I}, \vec{Q}$  are vectors of current/charge harmonics corresponding to nodal analysis and in general are nonlinear functions of the voltage harmonics  $\vec{V}$ .

<sup>1</sup>Early treatments by Rizzoli [164] nulled the imaginary part of one harmonic. As discussed in Section 6.1.4 and 6.1.6, a better choice is to choose relative phases that would decouple the amplitude and phase perturbations (Floquet decomposition) [48].

## B.2 Conversion Method

1. **Perturbation Model:** We model the perturbed oscillator capacitor voltages as

$$\vec{v}_k(t) = \sum_k (\vec{v}_{ss,k} + \Delta\vec{v}_k(t)) e^{jk2\pi f_{osc}t} \quad (\text{B.6})$$

where  $\Delta\vec{v}_k(t) \equiv (\Delta v_{c1}^k(t), \dots, \Delta v_{cn}^k(t))^T$  is again assumed to be slowly varying and much less than the corresponding steady-state harmonic components. Perturbing HB equation (B.4):

$$\left[ \underbrace{\left. \frac{\partial \vec{I}}{\partial \vec{V}} \right|_{ss}}_{\underline{G}_{eq}} + 2\pi j(f_{osc}\underline{K} + f_m\underline{1}) \underbrace{\left. \frac{\partial \vec{Q}}{\partial \vec{V}} \right|_{ss}}_{\underline{C}_{eq}} \right] \Delta\vec{V}(f_m) = \vec{I}_{noise} \quad (\text{B.7})$$

where  $n(2N_H + 1) \times 1$  vector  $\Delta\vec{V}(f_m)$  follows the same pattern as B.3 and contains the time-limited fourier transforms of the perturbations to each harmonic component of each state variable.

2. **NTF:** For the “arbitrary oscillator case, the noise is referred to “state variables” (capacitor voltages) based on (B.2):

$$\underline{NTF}_{LTI,LPTV} \equiv \left. \frac{\partial \vec{i}(\vec{v}, \vec{i}_{noise})}{\partial \vec{i}_{noise}} \right|_{DC,PSS} \quad (\text{B.8})$$

where the LTI/LPTV NTF is evaluated at the DC/periodic-steady-state (PSS) operating point, respectively. Determine the fourier coefficients; denoting the derivative of the  $k^{th}$  state-variable [capacitor current] with respect to the  $l^{th}$  noise current as follows:

$$\left. \frac{\partial i_k(\vec{v}, \vec{i}_{noise})}{\partial i_{noise,l}} \right|_{\vec{v}=DC/PSS} \equiv T_{k,l}(\theta) = \sum_p T_{k,l}^p e^{jp\theta} \quad (\text{B.9})$$

where for LPTV analysis, the NTF is periodically varying, while for LTI analysis, only the  $p = 0$  coefficient remains. Arrange in matrix form:

$$\underline{NTF}^{TCM} \equiv \left( \begin{array}{c|ccc} -N_H \underline{T}_1 & \dots & -N_H \underline{T}_m \\ \hline \vdots & \ddots & \vdots \\ \hline +N_H \underline{T}_1 & \dots & +N_H \underline{T}_m \end{array} \right); \quad {}^k \underline{T}_j \equiv \begin{pmatrix} T_{1,j}^{k+N_H} & \dots & T_{1,j}^{k-N_H} \\ \vdots & \ddots & \vdots \\ T_{n,j}^{k+N_H} & \dots & T_{n,j}^{k-N_H} \end{pmatrix} \quad (\text{B.10})$$

where  ${}^k \underline{T}_j$  matrix relates the  $j^{\text{th}}$  noise source to the  $k^{\text{th}}$  harmonic of the state variables. Note that for the LTI case, we only retain fundamental components, and there is no conversion gain between frequencies.

3. **NMF:** For LPTV case (LTI cannot capture), compute the fourier coefficients for each noise source's NMF:

$$NMF_k(\theta) = \sum_n M_k^n e^{jn\theta} \quad (\text{B.11})$$

Arrange in Toeplitz matrices as follows:

$$\underline{NMF} = \begin{pmatrix} \underline{M}_1 & \underline{0} & \dots & \underline{0} & \underline{0} \\ \underline{0} & \underline{M}_2 & & & \\ \vdots & & \ddots & & \vdots \\ \underline{0} & & & \underline{M}_{m-1} & \underline{0} \\ \underline{0} & \underline{0} & \dots & \underline{0} & \underline{M}_m \end{pmatrix} \quad (\text{B.12})$$

$$\underline{M}_k \equiv \begin{pmatrix} M_k^{+0} & M_k^{-1} & \dots & M_k^{1-2N_H} & M_k^{-2N_H} \\ M_k^{+1} & M_k^{+0} & & M_k^{2-2N_H} & M_k^{1-2N_H} \\ \vdots & & \ddots & & \vdots \\ M_k^{2N_H-1} & M_k^{2N_H-2} & & M_k^{+0} & M_k^{-1} \\ M_k^{2N_H} & M_k^{2N_H-1} & \dots & M_k^{+1} & M_k^{+0} \end{pmatrix} \quad (\text{B.13})$$

where  $\underline{M}_k$  denotes the TCM for the  $k^{th}$  noise source.

#### 4. $\mathbf{K}_{ICO}^\dagger$

$$\equiv \frac{2\pi j f_m}{V_{osc}} [0, \dots, 0, +1, 0, \dots, 0, -1, 0, \dots] \times [\underline{G}_{eq} + 2\pi j (f_{osc} \underline{K} + f_m \underline{1}) \underline{C}_{eq}]^{-1} \quad (\text{B.14})$$

where the  $\pm 1$  components correspond to the  $\pm 1$  harmonics of the chosen output voltage, respectively.

#### 5. Spectrum:

$$S_\phi(f_m) = \frac{1}{(2\pi f_m)^2} \vec{K}_{ICO}^\dagger(f_m) \times \underline{NTF} \times \underbrace{\underline{NMF} \times \underline{S}(f_m) \times \underline{NMF}^\dagger}_{\underline{S}_{mod}} \times \underline{NTF}^\dagger \times \vec{K}_{ICO}(f_m) \quad (\text{B.15})$$

where

$$\underline{S}(f) = \text{diag}(\underbrace{S_1(-N_H f_{osc} + f), \dots, S_1(+N_H f_{osc} + f)}_{2N_H + 1 \text{ components}}, \dots, S_m(+N_H f_{osc} + f)) \quad (\text{B.16})$$

and  $S_k(f)$  denotes the [maximum over periodic bias points] spectrum of the  $k^{th}$  noise source.

### B.3 Modulation Method

1. **Perturbation:** The oscillator waveforms in the presence of noise are modeled as

$$\vec{v}(t) = \sum_k [\vec{v}_{k,ss} + \Delta \vec{v}_k(t)] \exp(jk [2\pi f_{osc} t + \phi(t)]) \quad (\text{B.17})$$

Note the difference in this decomposition with the conversion method is that here, we explicitly include a phase perturbation  $\phi(t)$ .

2. **NTF/NMF:** Obtain matrices exactly as in Section 6.1.1.
3.  $K_{ICO}$ : Generalizing the derivation outlined Section 6.1.2,

$$[\underline{G}_{eq} + j(2\pi f_{osc}\underline{K} + \frac{d}{dt})\underline{C}_{eq}]\Delta\vec{V}(t) + j\frac{d\phi(t)}{dt}\underline{K}\vec{Q}_{ss} = -\underline{NTF}\vec{I}_{noise}(t)e^{-j\underline{K}\phi(t)} \quad (\text{B.18})$$

where  $\underline{G}_{eq}$  and  $\underline{C}_{eq}$  are the same as those in Section 6.1.1. Choose  $\vec{K}_{ico}^T$  to satisfy the following three conditions:

- (a)  $\vec{K}_{ico}^T \times (\underline{G}_{eq} + 2\pi j f_{osc}\underline{K} \times \underline{C}_{eq}) = \vec{0}$
- (b)  $\vec{K}_{ico}^T j\underline{K}\vec{Q}_{ss} = 1$
- (c)  $\vec{K}_{ico}^T \frac{d}{dt}\Delta\vec{V}(t) = 0$ ; this condition is analogous to choosing the amplitude noise to be orthogonal to the Floquet vector  $\vec{K}_{ico}^T(t)$ , as discussed in Section 6.1.6. Also, because HB implicitly accounts for multiple harmonics, this  $K_{ico}$  can capture higher-frequency noise effects as well because it includes components corresponding to conversion gains from multiple frequencies.

4. **Spectrum:** The phase-noise spectrum is obtained with

$$S_\phi(f_m) = [2\pi f_m]^{-2} \vec{K}_{vco}^\dagger \underline{S}_{mod}(f_m) \vec{K}_{vco}, \text{ where } \underline{S}_{mod} \text{ is defined in (B.15).}$$

#### B.4 Jitter Method

The analysis does not have a perfectly general form, as it is geared towards single-loop ring oscillators; however, the following expresses the general flow for single loop of  $N_{stage}$  delay stages.

1. **Perturbation:** Given unperturbed oscillator waveforms  $\vec{v}(t)$ , the perturbed waveforms are  $\vec{v}_{perturb}(t) = \vec{v}(t + t_{jitter}(t))$ ,  $\phi(t) = 2\pi f_{osc} t_{jitter}(t) = 2\pi \int f_{instant}(t) dt$ .
2. **NMF/NTF/ $K_{ICO}$ :**

- (a) Break up the oscillation period into segments based on the ideal switching approximation. During each segment  $k$ , construct an equivalent model for the switched-on part of the circuit:
- i. Identify the “timing node voltage”  $v_{timing}(t)$  i.e. the voltage that will trigger the next switching instant. For instance, in the ring oscillator of Fig. 2.6(a), the  $v_{timing} = v_k(t)$  until the inverter trip point is reached, at which point,  $v_{timing}(t)$  becomes  $v_{k+1}(t)$ .
  - ii. Compute the convolution  $v_{timing}(t) = h_k(t) \otimes i_k(t)$ , where  $h_k(t)$  is the impulse response of the timing voltage to the [white] noise source  $i_k$ . The impulse response  $h_k$  is the combination of the NTF and the  $K_{ICO}$  gain.
  - iii. To account for noise modulation, compute an effective PSD intensity by performing a time average over the switching interval.
  - iv. To account for switch noise, average over the whole period (their contributions will mostly be during transitions) [24, 170, 174].
- (b) Compute the variance (squared RMS voltage):  $\sigma_{v_k}^2(t_{r/f}[k]) = \mathbb{E} [v_k^2(t_{r/f}[k])]$ , i.e. evaluate the variance just before the trigger point<sup>2</sup>. The variance depends on time (nonstationary) because the system may not reach steady state within a switching interval. (For simplicity, often assume zero initial conditions at beginning of switching interval, e.g.  $v(0) = 0$ ).
- (c) Jitter Slew-Rate Equation:

$$\sigma_j^2(t_{r/f}[k]) = \frac{\sigma_v^2(t_{r/f}[k])}{SR^2(t_{r/f}[k])} \quad (\text{B.19})$$

<sup>2</sup>Note that the rise/fall delay themselves are random variables (because of jitter!); however, because the instantaneous jitter accumulated within a single delay  $t_d$  is typically much less than that delay  $t_d$ , the approximation incurs small error. An alternate approach using the “last passage of time” provides a first-order correction [208].

(d) Normalize w.r.t. delay:

$$\kappa_{r/f}^2[k] \equiv \frac{\sigma_j^2(t)}{t} = \frac{\sigma_v^2(t_{r/f}[k])}{SR^2(t_{r/f}[k])t_{r/f}[k]} \quad (\text{B.20})$$

(e) Repeat for other noise sources, and take weighted average:

$$\kappa_{tot}^2 = f_{osc} \sum_{k=1}^{N_{stage}} (\kappa_r^2[k]t_r[k] + \kappa_f^2[k]t_f[k]).$$

3. **Spectrum:**  $S_\phi(f_m) = \kappa_{tot}^2 \left(\frac{f_{osc}}{f_m}\right)^2$

## B.5 Direct KICO Method

1. **Perturbation Model:** The oscillator output waveforms are assumed to take the form

$$\vec{v}(t) = \vec{v}_{ss} \left( t + \frac{1}{2\pi f_{osc}} \int_0^t K_{ICO} i_{noise,LF}(t) dt \right) \quad (\text{B.21})$$

where  $\vec{v}_{ss}$  denotes the steady-state waveform for the “arbitrary” oscillator of Fig. B.1, and  $f_{osc}$  denotes the nominal oscillation frequency

2. **NMF:** The noise-modulation function is not explicitly included in this technique. However, applying the results of the Phase-Sensitivity Method (see Section 6.1.5), we could obtain an effective noise spectrum at the parasitic frequency-control input by substituting the steady-state oscillation waveforms into the expression in (5.2) and averaging over one cycle.

3.  **$K_{ICO}$  and NTF:** For the Direct KICO method, the “ $K_{ICO}$ ” quantity captures the noise transfer function for the low-frequency noise explicitly because the expression for the frequency is already written in terms of the noise quantity in question:

$$K_{ICO}^{direct} \equiv \left. \frac{\partial f_{osc}}{\partial i_{noise}} \right|_{i_{noise} = \mathbb{E}[i_{noise}] = 0} \quad (\text{B.22})$$

4. **Spectrum:**  $S_\phi(f_m) = \frac{(K_{ico}^{direct})^2}{f_m^2} S_{inoise}(f_m)$ , where  $S_{inoise}(f_m)$  indicates the averaged noise spectrum from the previous step.

## B.6 Phase-Sensitivity Method

1. **Perturbation:** Given the “arbitrary oscillator’s” steady-state waveforms  $\vec{v}_{ss}(t)$ , with noise, the phase perturbations shift the waveforms to become  $\vec{v}_{ss}(t + \phi(t)/[2\pi f_{osc}])$ , where

$$\phi(t) = \sum_k \int_0^t \frac{\Gamma_k(2\pi f_{osc}\tau)}{q_{max}} NMF_k(2\pi f_{osc}\tau) i_k^{unmod}(\tau) d\tau \quad (\text{B.23})$$

where  $NMF_k(2\pi f_{osc}\tau)$  accounts for cyclostationary noise modulation as discussed in Section 6.1.1.

2.  $\Gamma_{eff}$  **and**  $K_{ICO}$ : for each noise source  $k$ ,

$$\Gamma_k^{eff}(x) = \underbrace{\Gamma^{Co}(x) NTF(x)}_{\Gamma_k(x)} NMF_k(x) \quad (\text{B.24})$$

where  $NTF(x)$  refers the noise source to the capacitor voltage  $V_{Co}$ , and fitting this technique into the general paradigm,

$$K_{ICO}(x) = \frac{\Gamma^{Co}(x)}{q_{max}} \quad (\text{B.25})$$

3. **NMF:** substitute the steady-state device voltages into the device’s spectrum equation as discussed in Section 6.1.1.
4.  $\Gamma_k$  (**NTF and**  $K_{ICO}$ ):
- (a) **METHOD1 (Numerical Simulation):**

- i. Simulate the unperturbed oscillator and save the “reference” waveform.
- ii. Resimulate the oscillator with an impulse current source located where the noise current would be. Have the source inject a short pulse of current  $i(t) \approx$



$q_{inj}\delta(t - t_{ss} - \tau)$  as illustrated in Fig. 6.8, where  $t_{ss}$  is large enough that the oscillator has reached steady state by the time of injection, and  $\tau \in [0, T_{osc}]$ .

iii. Measure the zero-crossing time-interval error:

$$TIE(\tau, q_{inj}) = t_N^{ref} - t_N^{perturbed}(\tau, q_{inj}) \quad (\text{B.26})$$

where  $t_N$  denotes the time of the Nth rising-edge zero crossing after  $t_{ss}$  (N should be sufficiently large, say 20 cycles, to allow the oscillator to settle back into periodic steady state). Fig. 6.8 illustrates the concept for N=1.

iv. Normalize to obtain the sensitivity function:

$$\Gamma_k(2\pi f_{osc}\tau) = \frac{q_{max}}{q_{inj}} 2\pi f_{osc} TIE(\tau, q_{inj}) \quad (\text{B.27})$$

v. Repeat for other values of  $\tau \in [0, T_{osc}]^3$ .

(b) METHOD 2 (Slope/NTF):

i. Approximate [72, 107]:

$$\Gamma_{C_o}(x) \approx \frac{q_{max}}{C_o} \frac{\frac{dV_{C_o}(t)}{d(2\pi f_{osc}t)}}{\sum_k \left( \frac{dV_{C_k}(t)}{d(2\pi f_{osc}t)} \right)^2} \approx \frac{q_{max}}{C_o} \frac{\frac{dV_{C_o}(t)}{d(2\pi f_{osc}t)}}{\sum_k \max \left( \frac{dV_{C_k}(t)}{d(2\pi f_{osc}t)} \right)^2} \quad (\text{B.28})$$

The approximation works best when state variables are properly normalized—e.g. for tank inductors, use  $V_{Leff} = \sqrt{\frac{L}{C}} i_L$  [44]. For nearly sinusoidal oscillators and  $V_{C_o} \approx V_{osc} \cos(\theta)$ ,  $\Gamma_{C_o}(x) \approx -\frac{\sin(x+\xi)}{N_R}$ , where  $N_R = \#$  resonators and  $\xi \approx 0$ , except for quadrature coupled oscillators [193].

ii. To determine the NTF from noise source k to  $V_{C_o}$ , linearize the circuit about the periodic operating point and perform time-domain analysis. (Andreani/Mazzanti/et al. have several illustrative examples [44, 192, 193, 196,

<sup>3</sup>N.B. With the numerically obtained function, one can also perform a fit to obtain an approximate closed-form solution, e.g. see [107].

197]; N.B. Andreani’s “noise-modulation function” often corresponds to  $NTF_k(t)NMF_k(t)$  in our notation).

iii. Therefore,  $\Gamma_{eff,k}^2(x) = \underbrace{\Gamma_{C_o}^2(x)NTF_k^2(x)NMF_k^2(x)}_{\Gamma_k^2(x)}$

5. **Spectrum:** Compute the RMS, DC values of  $\Gamma_k^{eff}(x)$  and substitute into (6.43).

## B.7 Fokker-Planck Method

1. **Perturbation/Phase Definition:** The *nonlinear* equation for phase perturbations is

$$d\phi(t) = \underbrace{\vec{K}_{ico}^T(\tilde{t}) \underline{NTF}[\vec{v}_{ss}(\tilde{t})] \underline{NMF}[\vec{v}_{ss}(\tilde{t})]}_{\vec{p}^T(\tilde{t})} \sqrt{S_{noise,max}} d\vec{W}(t) \quad (\text{B.29})$$

where  $\tilde{t} \equiv t + \frac{\phi(t)}{2\pi f_{osc}}$ , and  $\vec{p}^T$  is periodic ( $T_{osc}$ ) and has units  $[1/\sqrt{sec}]$ .

2. **NMF/NTF:** Obtain using equations (5.2) and (6.51).

3.  $K_{ICO}$ :

(a) Solve (typ. numerically) for the *periodic* solution to the adjoint linear companion equation:

$$\frac{d}{d\tilde{t}} \vec{K}_{ico}^T(\tilde{t}) = -\vec{K}_{ico}^T(\tilde{t}) \underline{\Omega}(\vec{v}_{ss}(\tilde{t})) \quad (\text{B.30})$$

and normalize  $\vec{K}_{ico}^T(\tilde{t}) \frac{1}{2\pi f_{osc}} \frac{d}{d\tilde{t}} \vec{q}_{ss}(\tilde{t}) = 1$ .

(b) Obtain the parameters for the Gaussian distribution:

(a) white noise:

$$[2\pi f_{osc} \kappa_{white}]^2 = RMS^2 = \int_{T_{osc}} \vec{p}^T(t) \vec{p}(t) \frac{dt}{T_{osc}} \quad (\text{B.31})$$

(b) flicker noise <sup>4</sup>:

$$[2\pi f_{osc} \kappa_{f,k}]^2 = DC^2 = \left[ \int_{T_{osc}} p_k(t) \frac{dt}{T_{osc}} \right]^2 \quad (\text{B.32})$$

where  $p_k(t) = \vec{K}_{ico}^T(t) \underline{C}^{-1}(\vec{v}_{ss}(t)) \underline{NTF}_k[\vec{v}_{ss}(t)] \underline{NMF}_k[\vec{v}_{ss}(t)]$  and  $\underline{NTF}_k$  denotes the noise-transfer function for the  $k^{th}$  flicker noise source (assumed to be independent of all white noise sources and of all other flicker noise sources).

#### 4. Spectrum:

$$S_\phi(f_m) = \begin{cases} \kappa^2 \left( \frac{f_{osc}}{f_m} \right)^2 & , \text{ white} \\ \kappa_{f,k}^2 \left( \frac{f_{osc}}{f_m} \right)^2 S_k(f_m) & , \text{ flicker} \end{cases} \quad (\text{B.33})$$

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<sup>4</sup> [227, 228] discuss second-order corrections for non-power-law colored noise.

## VITA

Erik Pankratz received the B.S. degree (summa cum laude) from the University of Texas at Austin in spring 2006 and the Ph.D. degree in analog circuit design at Texas A&M University in fall 2011. Mr. Pankratz's previous research work has included highly programmable analog filters, and his thesis work focuses on multi-loop ring-oscillator design and jitter/phase-noise analysis.

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