INTEGRATED CIRCUIT BLOCKS FOR HIGH PERFORMANCE BASEBAND AND RF ANALOG-TO-DIGITAL CONVERTERS

A Thesis

by

HONGBO CHEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Aydin I. Karsilayan
	Peng Li
	Jay R. Porter
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ABSTRACT

Integrated Circuit Blocks for High Performance Baseband and RF Analog-to-Digital Converters. (December 2011)

Hongbo Chen, B.S., Xi'an Jiaotong Univerisity; M.S., Tsinghua University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Nowadays, the multi-standard wireless receivers and multi-format video processors have created a great demand for integrating multiple standards into a single chip. The multiple standards usually require several Analog to Digital Converters (ADCs) with different specifications. A promising solution is adopting a power and area efficient reconfigurable ADC with tunable bandwidth and dynamic range. The advantage of the reconfigurable ADC over customized ADCs is that its power consumption can be scaled at different specifications, enabling optimized power consumption over a wide range of sampling rates and resulting in a more power efficient design. Moreover, the reconfigurable ADC provides IP reuse, which reduces design efforts, development costs and time to market.

On the other hand, software radio transceiver has been introduced to minimize RF blocks and support multiple standards in the same chip. The basic idea is to perform the analog to digital (A/D) and digital to analog (D/A) conversion as close to the antenna as possible. Then the backend digital signal processor (DSP) can be programmed to deal

with the digital data. The continuous time (CT) bandpass (BP) sigma-delta ($\sum\Delta$) ADC with good SNR and low power consumption is a good choice for the software radio transceiver.

In this work, a proposed 10-bit reconfigurable ADC is presented and the non-overlapping clock generator and state machine are implemented in UMC 90nm CMOS technology. The state machine generates control signals for each MDAC stage so that the speed can be reconfigured, while the power consumption can be scaled. The measurement results show that the reconfigurable ADC achieved 0.6-200 MSPS speed with 1.9-27 mW power consumption. The ENOB is about 8 bit over the whole speed range.

In the second part, a 2-bit quantizer with tunable delay circuit and 2-bit DACs are implemented in TSMC 0.13um CMOS technology for the 4^{th} order CT BP $\sum\Delta$ ADC. The 2-bit quantizer and 2-bit DACs have 6dB SNR improvement and better stability over the single bit quantizer and DACs. The penalty is that the linearity of the feedback DACs should be considered carefully so that the nonlinearity doesn't deteriorate the ADC performance. The tunable delay circuit in the quantizer is designed to adjust the excess loop delay up to $\pm$10% to achieve stability and optimal performance.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deep appreciation to my advisor Dr. Jose Silva-Martinez for having accepted me into his group, his invaluable guidance, insightful thinking, kindness and support throughout my graduate study. Without his patient support and encouragement, this work would not have been completed. I would also like to thank all my committee members, Dr. Aydin I. Karsilayan, Dr. Peng Li and Dr. Jay R. Porter Walker for their time, support and valuable suggestions.

I would like to thank my team members John Mincey and Yung-Chung Lo, in the CT BP ∑Δ data converter project, Heng Zhang, Junhua Tan and Chao Zhang in the reconfigurable ADC project, for their cooperation, valuable advice and making the project a great experience. Special thanks go to Yung-Chung Lo who supported and helped me a lot not only in academic field, also in my personal life. I would like to thank all my friends, especially Dr. Xin Guan, Shan Huang, Jackie Zou, Yang Liu, Dr. Zhuizhuan Yu, Dr. Xi Chen, Jun Yan, Jiayi Jin, Cheng Li, Haoyu Qian, Xuan Zhao, Cheng-Ming Chien, Yuan Luo, Chang-Joon Park, Hemasundar Geddada, Hajir Hedayati, Ehsan, Jusung Kim, for all the valuable discussions, encouragements and friendship. I also want to thank Ella and Tammy for their assistance.

Finally, I would like to express my deepest gratitude to my parents for their unconditional love, constant encouragement and support. I couldn't have gone this far without their support.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 Research motivation

Mobile and wireless communications have been moving towards the 4G wireless communication system, which integrates multiple wireless standards to provide more services for the end users. As shown in Fig. 1.1, a typical 4G wireless device is expected

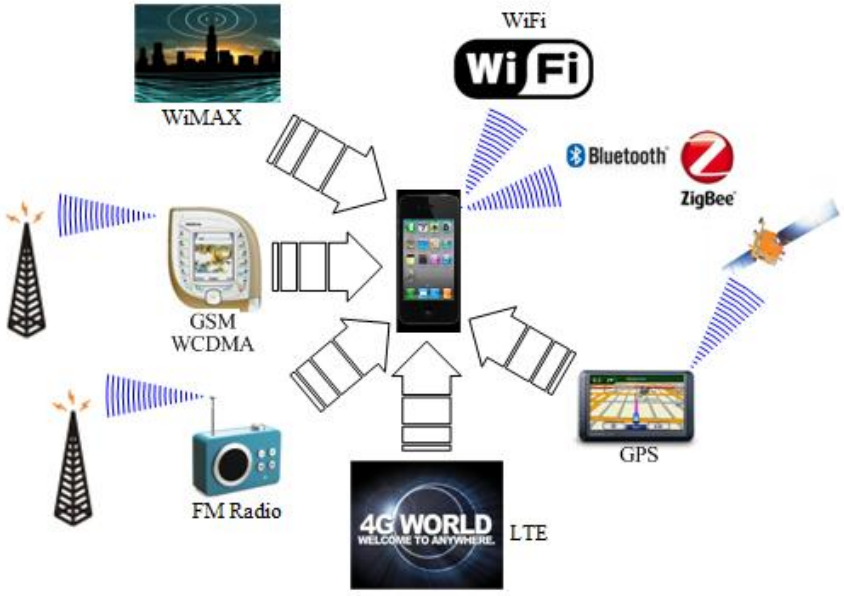

Fig. 1. 1. 4G wireless device

to support these features simultaneously: 1) Cell phone standards: GSM (Global System for Mobile communications), CDMA (Code Division Multiple Access), LTE (Long Term Evolution); 2) Wireless connecting standards: WiFi (Wireless Fidelity, i.e. IEEE 802.11a/b/g/n), Zigbee (i.e. IEEE 802.15.4), WiMAX (Worldwide Interoperability for

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This thesis follows the style of *IEEE Journal of Solid State Circuits.*

Microwave Access); 3) Satellite communication: GPS (Global Positioning System); 4) Entertainment service: FM/XM radio and DVB-T/H (Digital Video Broadcasting – Terrestrial/Handheld).

In mobile and wireless communication system, the frequency spectrums are shown in Fig. 1.2. Since multiple standards with different specifications need to be supported, it

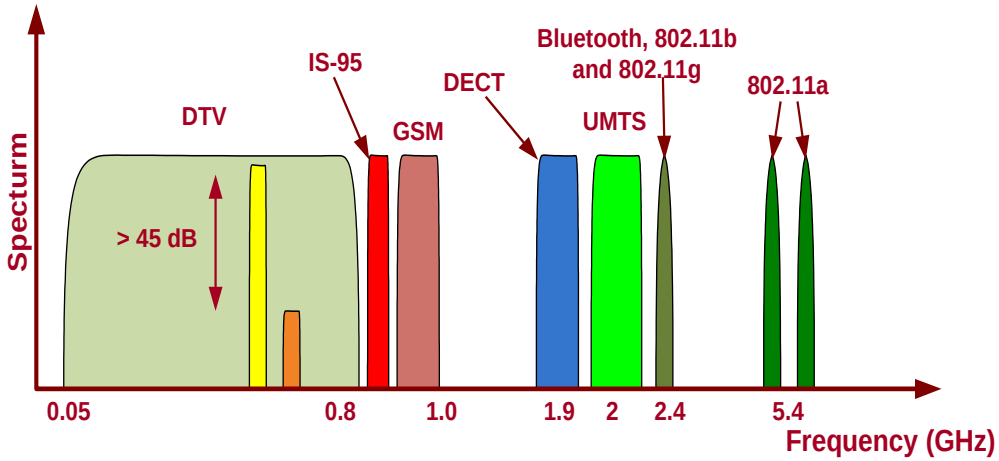


Fig. 1. 2. Frequency spectrums of wireless applications

is desirable to integrate them into a single chip to save power and area. A versatile and cost effective solution is to adopt the reconfigurable direct conversion wireless receiver architecture as shown in Fig. 1.3 [1]. It is composed of two main blocks: shared RF front-end and reconfigurable baseband. In the front-end block, the wideband low noise amplifier (LNA) and wideband mixer with wide tuning range phase locked loop (PLL) are introduced to convert the RF signal into baseband signal. In the baseband block, the tunable low pass filter (LPF) and variable gain amplifier (VGA) filter out the unwanted frequency components and adjust the signal power to the dynamic range of the following

tunable ADC. The ADC with satisfied resolution and speed converts the analog baseband signal into digital domain so that the digital signal processor (DSP) can deal with.

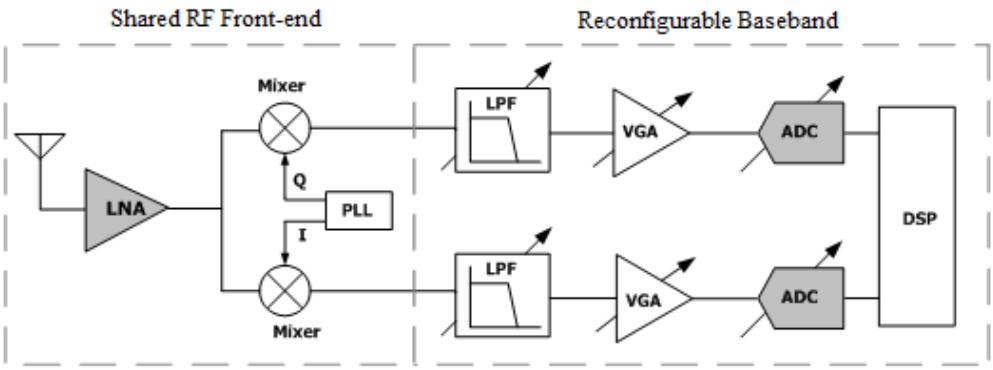


Fig. 1. 3. Block diagram of a reconfigurable direct conversion receiver [1]

Another promising solution is the software radio receiver as shown in Fig. 1.4. The RF filter removes the outside channel signals and the broadband LNA amplifies the incoming signal to the following RF ADC, which converts the RF signal into digital domain directly. Then the digital modulator demodulates the digital signal and the unwanted signal is filtered out using digital filter. Finally the DSP acquires the data and recovers the transmitted baseband signal. The basic idea of the software radio receiver is to place the ADC as close to the antenna as possible so that the analog mixers are avoided [2], [3].

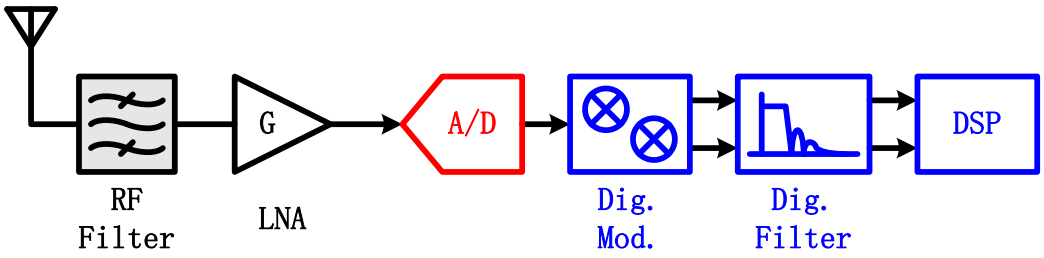


Fig. 1. 4. Block diagram of a software radio receiver

1.2 Research goals

The main aim of this research is to design high performance integrated circuit blocks for baseband and RF analog-to-digital converters that can be used in wireless communication system. The first part of this research presents the design of a 0.6-200 MSPS speed reconfigurable power scalable 10-bit ADC in UMC 90nm CMOS technology. The "global cyclic" technique was proposed to reconfigure the speed and scale the power consumption at the same time without sacrifice the ADC performance. The proposed ADC only needs one external sampling clock, which simplifies the system requirement. Moreover, the bias currents in the ADC at different speeds are kept constant, which eliminates the reliability issue. The measurement results show that the reconfigurable ADC achieved 0.6-200 MSPS speed with 1.9-27 mW power consumption. The ENOB is about 8 bit over the whole speed range.

The second part of this research deals with the design of a 2-4 GHz 4^{th} order CT BP $\sum\Delta$ ADC. A 2-bit quantizer with tunable delay circuit and 2-bit DACs are implemented in TSMC 0.13um CMOS technology. The 2-bit quantizer and 2-bit DACs have 6dB SNR improvement and better stability over the single bit quantizer and DACs. The penalty is that the linearity of the feedback DACs should be considered carefully so that the nonlinearity doesn't deteriorate the ADC performance. A tunable delay circuit is designed to adjust the excess loop delay up to $\pm$20% to achieve stability and optimal performance.

1.3 Thesis organization

This thesis is composed of six sections.

Section 1 provides a brief introduction of receiver architectures for the wireless communication system. The main goals of this thesis are also presented.

Section 2 presents the proposed “global cyclic” reconfigurable 10-bit ADC, covers the system design, state machine circuit implementation and measurement results. The measurement results show that the proposed ADC achieve 8-bit ENOB at 0.6-200 MSPS speed with 1.9-27 mW power consumption.

Section 3 discusses the basics and features of the continuous time ∑Δ modulators. Some important nonidealities are also explained, followed by a brief description, specifications and circuit parameters of the proposed CT BP ∑Δ ADC.

Section 4 explains the proposed 2-bit quantizer with tunable delay of the proposed CT BP ∑Δ ADC. The circuit implementation details and the layout of the quantizer are also presented. Several postlayout simulations are employed to verify the quantizer.

Section 5 discusses several typical techniques for improving the linearity of multi-bit DACs. Then the proposed 2-bit DACs topology, transistor level implementations, layout and postlayout simulation are well explained in this section.

Section 6 summarizes the research in this thesis and discusses the future work.

2. SPEED RECONFIGURABLE POWER SCALABLE ADC

2.1 Introduction

The emerging multi-format video processors and multi-standard wireless receivers have created a great demand for integrating multiple design specifications into a single chip [4], [5]. Flexible RF and analog baseband blocks that can meet various specifications with minimum hardware implementation are required in such systems. An "adaptive figures of merit (AFOM)" is proposed in [4]. When it comes to ADCs, a power- and area-efficient reconfigurable ADC with variable bandwidth and dynamic range is a promising solution [6]–[14]. Customized ADCs have power optimized for only one specification, while a reconfigurable ADC can scale its power at different specifications, enabling minimal power consumption over a broad range of sampling rates and resulting in a more power-efficient design.

On the other hand, time-to-market pressure and increased design complexity create a "design gap" for SoCs. The "design-reuse methodology" has been successfully applied to digital systems; therefore the analog part of the SoC dominates the overall design time, cost, and risk. The ADC is one of the most important analog units, and a reconfigurable ADC provides IP reuse, which can be targeted for a wide range of applications with different specifications, thus reduces design efforts, development costs, and time to market.

This work targets display and imaging systems. Most multi-format video processors for HDTV, SDTV, and PC graphic require ADCs with fixed resolution (i.e. effective number of bits (ENOB) > 8bit) for accurate color reproduction. However, the

sampling rate and effective resolution bandwidth (ERBW), as a function of the number of pixels and the refresh rate, vary with the standards. Table 2.1 summarizes the ADC requirement for component video, PC graphic, and some popular communication standards. To cover the mainstream display/imaging system standards, the ADC must have a wide range of 1MSPS-200MSPS, which presents a new challenge.

Table 2. 1. Summary of the ADC specifications

(a) Communication

Standard	Sampling rate (MSPS)*	Resolution(bit)
GPS	4	10
WCDMA	8	9-10
WLAN	44	8-10
WiMAX	10~40	8-10

(b) Component video

Standard	Pixel rate (MSPS)
480p	8.1
480i	18.41
576p	20.736
576i	20.736
720p	22.12 – 55.3
1080p	49.77 – 124.42
1080i	49.72 – 124.30

(c) PC graphic

Standard	Pixel rate (MSPS)**
VGA	21.5
SVGA	28.8
XGA	47.19
XGA+	59.72
SXGA	78.64
SXGA+	88.20
UXGA	115.20
QXGA	188.74

The Sigma-Delta ADC is an attractive solution for multi-standard wireless receivers [15]-[17]. It can be configured to achieve larger bandwidth with lower resolution or smaller bandwidth with higher resolution by programming its digital decimation filter. However, the over-sampling feature limits the use of a Sigma-Delta ADC in wide bandwidth applications, such as video processors.

On the other hand, the pipeline ADC has inherently higher operating speed, thus it is more suitable for medium to high speed applications. Furthermore, its sampling rate and resolution can be programmed independently, which is desired for multi-format video processors where various sampling rate are needed while the same resolution is required. However, a pipeline ADC is more difficult to program than the sigma-delta. Therefore, this research work explores an efficient implementation of a reconfigurable ADC based on the pipeline architecture with medium to high sampling rate to cover all the video standards.

Section 2.2 addresses the challenge of analog power scaling, and discusses reconfiguration methodologies for ADCs. Section 2.3 presents the proposed reconfigurable ADC architecture. Section 2.4 describes the circuit implementation for each building block. Measurement results and conclusions are presented in section 2.5 and section 2.6, respectively.

2.2 ADC reconfiguration methodology

2.2.1 Analog power scaling

For a power-optimized ADC, just enough power is consumed to ensure the required accuracy at a specific clock frequency. A popular ADC FOM [17] is:

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} \tag{2.1}$$

where f_s is the ADC sampling rate. This FOM is proportional to the power/speed ratio; therefore, it is essential to have good power scalability when programming the speed in order to keep a comparable FOM with dedicated ADCs at each setting.

To explore the power scalability, we can recall the power consumption expressions for digital and analog circuits shown below.

$$Power_{\text{digital}} = \frac{1}{2} CV^2 f_s \tag{2.2}$$

$$Power_{\text{analog}} = V \cdot I \tag{2.3}$$

where V is the supply voltage, C is the load capacitance, and I is the total current drawn from the supply. For digital circuits, the average power automatically scales with sampling frequency. In analog circuitry, the power is not an explicit function of frequency. Furthermore, V is kept constant in most cases. To make the power track the clock frequency, it is desirable to make the current as a function of frequency, i.e.: $Power_{\text{analog}}(f) = V \cdot I(f_S)$.

2.2.2 Bias current scaling

Previous works programmed the pipeline ADC power by scaling the biasing current of the active building blocks (i.e. OTAs) [18]-[21]. However, this approach achieved fairly limited power/speed programmability because a wide programming range mandates a correspondingly large current-scaling ratio. Changing the current by such a large amount drives the transistors far away from the intended bias point, worsening yield.

Furthermore, multi-format video processors only need to configure the speed, while keeping the resolution constant. However, bias current variations affect the open-loop DC gain and the maximum output voltage swing of the amplifier: both the open-loop gain and maximum output voltage swing typically decrease with increasing bias current, especially for an OTA with cascode stages. Therefore, biasing current scaling makes the design more difficult.

In [18] and [21], which simply employ the bias current scaling method, good power scalability is reported, but with small speed programming ratio (<7). These results indicate that bias current scaling can only achieve very limited speed/power programmability.

2.2.3 Architecture-level reconfiguration

An architecture level reconfiguration/innovation is desired to address the challenge of achieving simultaneous large programming ratio in speed and power with robust performance (i.e. minimum bias current variations) over PVT variations.

A reconfigurable ADC can be viewed as an ADC with a configurable switch matrix, which adjusts the ADC topology to minimize power consumption at each point in the performance space. Trying to make an ADC “reconfigurable” usually results in compromised linearity and/or noise performances, due to the higher-order effects induced by extra switches and control units for programmability functions. Therefore, a big challenge is to reduce these degradations, and show comparable power consumption at each performance node compared with a dedicated ADC.

Fig. 2.1 shows the diagram of a conventional n-stage pipeline ADC. It passes the residue voltage (Vres) from one stage to the next. The Multiplying DAC stage (MDAC) includes a sub-ADC, a sub-DAC, and a residue amplifier. The pipeline ADC is fast since it has n stages working concurrently. The effective speed of a pipeline ADC can be reduced by configuring it into cyclic ADC mode. [9] reported a hybrid pipeline/cyclic reconfigurable ADC, where two residue feedback loops are introduced to operate some stages as cyclic ADCs during certain clock cycles. However, amplifiers in the MDAC stages see different loadings when driving succeeding/preceding stages, and stage scaling cannot be efficiently applied to optimize power as in a typical pipeline ADC. Therefore a better reconfigure method is needed to fully leverage the potential of pipeline ADC.

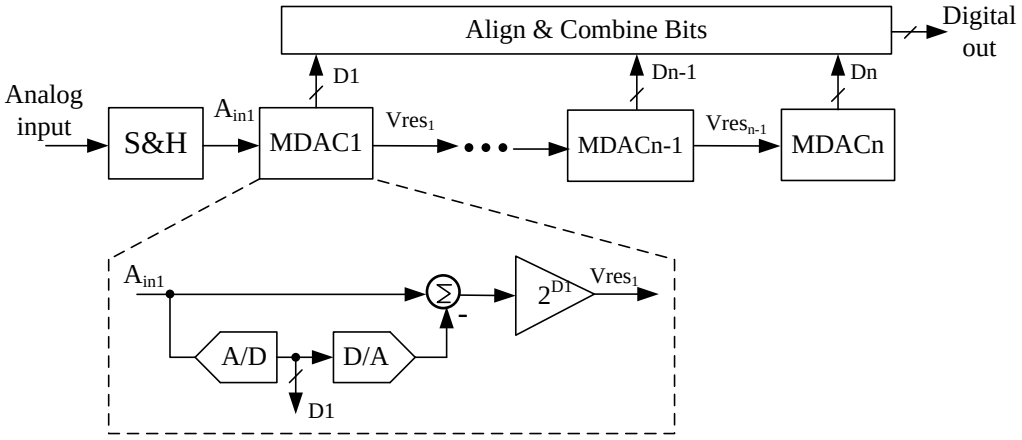


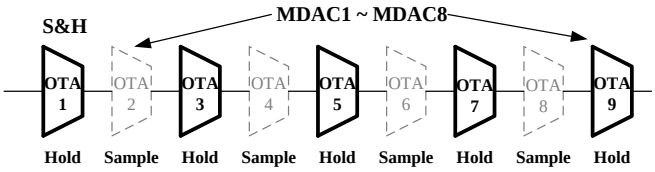
Fig. 2. 1. Block diagram of a n-stage pipeline ADC

2.3 Proposed reconfiguration architecture

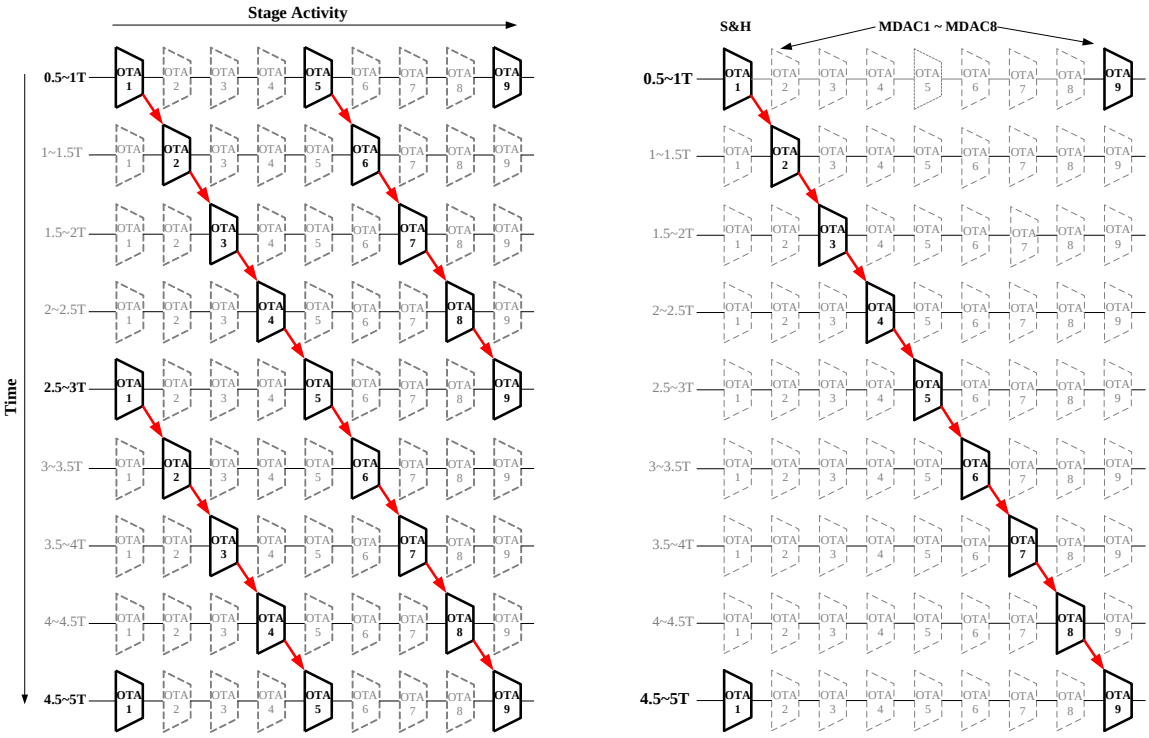
2.3.1 Proposed reconfiguration technique

Fig. 2.2 presents a conceptual diagram of the proposed ADC. The architecture incorporates a sample-and-hold (S&H), eight 1.5-bit MDAC stages, and a 2-bit flash

ADC as the last stage. For simplicity, the S&H and each MDAC stage is represented by an OTA symbol. A solid line around an OTA means that the stage is turned on (amplification phase); while a dashed line means that it is turned off (tracking phase). To save power, the OTA is only powered on in the amplification phase. Although charge injection is worse for passive sampling, transmission gates are used to relieve SNDR degradation. To compute the average power, assume each stage consumes a normalized power of 1 and average the number of OTAs in amplification phase over time T=1/fs. While configured in full-speed mode fs, the input is sampled every period T; hence, from Fig. 2.2 (a), Pavg,norm= 5 × ½ + 4 × ½ = 4.5.While configured at half-speed mode fs/2, the input is sampled every 2T (i.e. at time instants 0.5T, 2.5T, 4.5T). Note that there is only one physical row, but we are expanding it in time (the vertical axis) to illustrate the operation. The diagonal arrows represent the pipelining of an analog input. Shortly before one stage powers off, the subsequent stage powers on and enters the amplification phase to ensure that the input continuously travels through the entire pipeline chain. The digital outputs from each stage are latched before the stage powers off. Thus, the average power in fs/2 mode is: 3 × 1/4 + 2 × 3/4 = 2.25. While configured in the fs/4 mode, the input is sampled every 4T with an average power of: 2 × 1/8 + 1 × 7/8 = 1.125. In this mode, it essentially operates as a cyclic ADC because only one stage is working at a time. Table 2.2 illustrates the power scaling for the proposed reconfiguration technique. Theoretically the power scales at the same ratio as the speed scales, keeping a constant power/speed ratio and FOM.



(a)



(b) (c)

Fig. 2. 2. Proposed reconfigurable technique: (a) full speed mode (Fs) (b) Fs/2 speed mode (c) Fs/4 speed mode

Table 2. 2. Power scaling for the proposed reconfigurable technique

Speed	N	Sampling Interval	Average Power	Normalized Power
Fs	1	T	5* 1/2 + 4* 1/2 = 4.5	1
Fs/2	2	2T	3* 1/4 + 2* 1/4 = 2.25	1/2
Fs/4	4	4T	2* 1/8 + 1* 7/8 = 1.125	1/4
Fs/8	8	8T	2* 1/16 + 1* 7/16 = 0.5625	1/8
.....				
Fs/N		NT	2* 1/2N + 1* 7/2N = 9/2N	1/N

Fig. 2.3 depicts a comparison between the proposed technique and the typical "current scaling" techniques. For the "current scaling", the ADC is always "ON", and power is scaled by adjusting the sampling clock period and the bias current at the same ratio. For the proposed technique, the bias current is kept constant (i.e. same pulse width, same setting time/accuracy) thus the ADC performs conversions at a constant maximum rate. The effective speed is programmed by varying the ADC's "ON" time. The same averaged power consumption is achieved between these two approaches, but the proposed technique programs the power/speed on the architectural level, thereby circumventing the large variations in bias currents. Consequently, the transistors remain optimally biased because the amplifier bias currents remain unchanged across the power/speed programming range. The proposed reconfigurable ADC also has two advantages over the previous "pipeline/cyclic reconfiguration [9]": 1) it combines well with pipeline stage scaling; 2) apart from the state machine, no extra digital logic is needed for the cyclic mode.

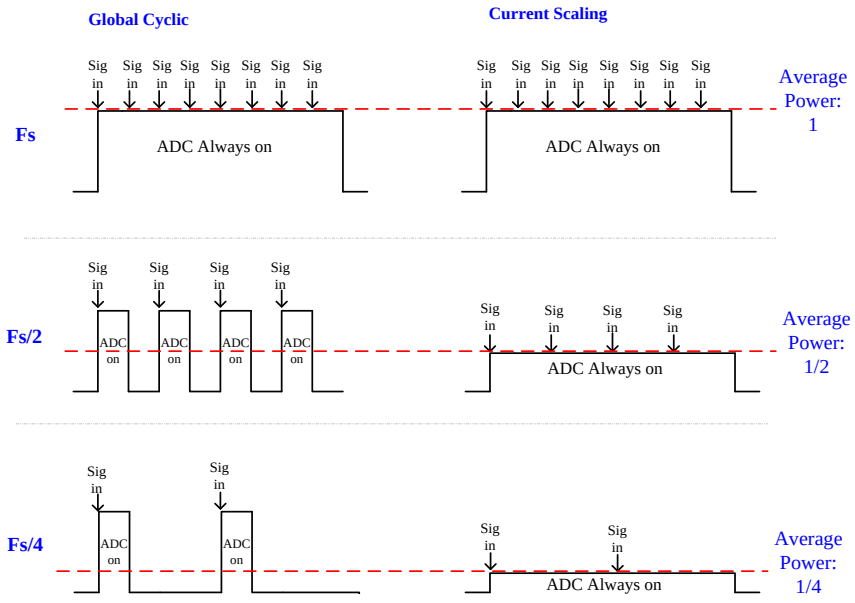


Fig. 2. 3. Proposed technique vs. current scaling

Fig. 2.4 shows the block diagram of the proposed reconfigurable ADC. It has two unique features: 1) a state machine generates the power on/off timing signals to achieve different effective sampling rates. 2) The duty cycle of each MDAC stage is programmable. The capacitances and bias currents in MDAC2-5 are scaled down by a factor of 0.55 compared to the 1st stage, and those in MDAC6-8 are further scaled down by 0.52 to reduce the power.

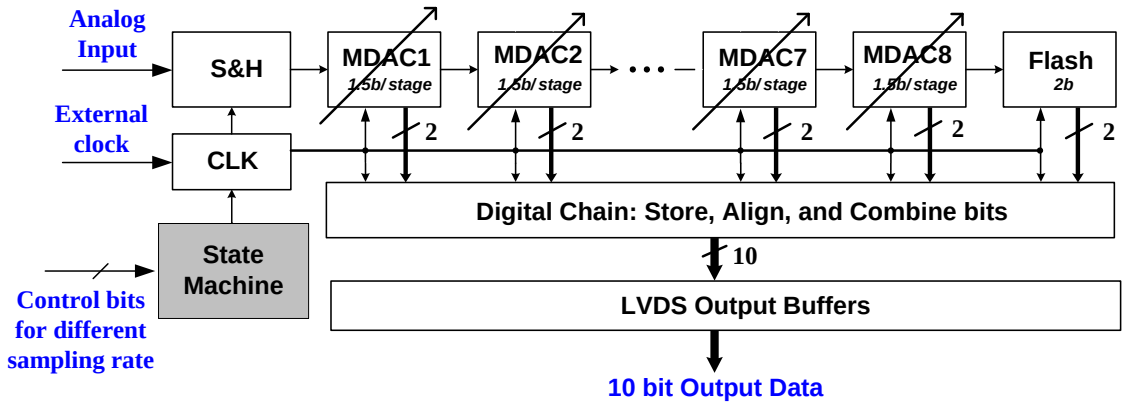
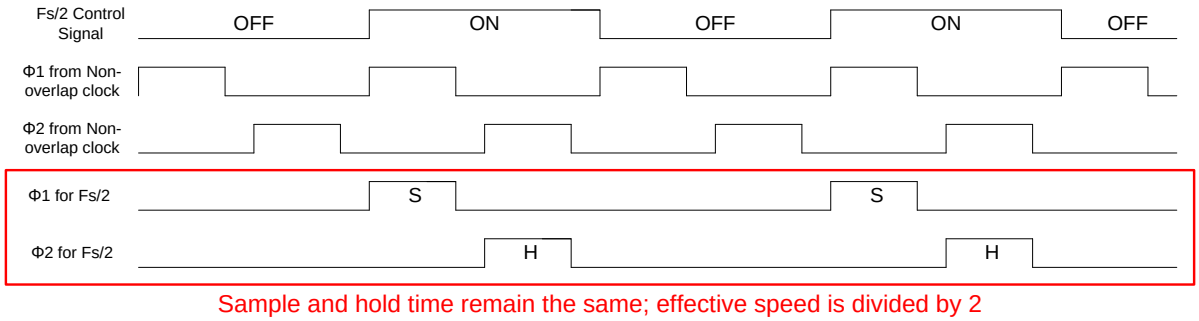


Fig. 2. 4. System diagram of the proposed reconfigurable ADC

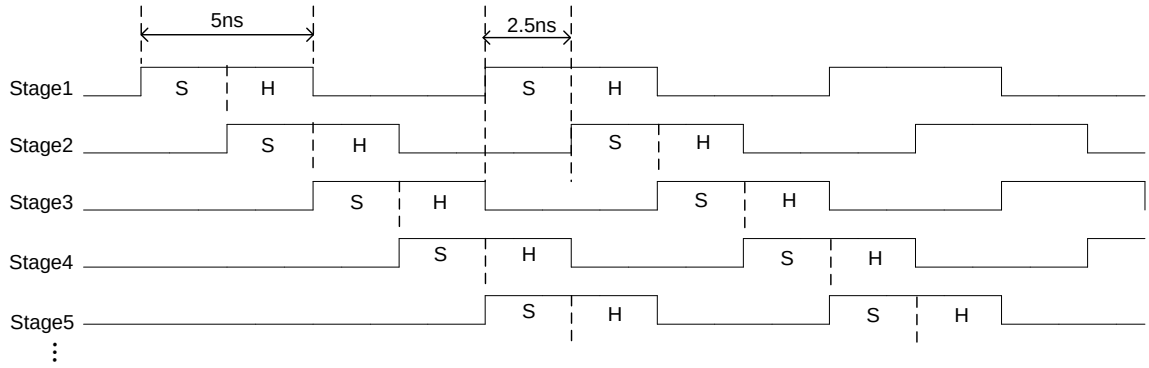
2.3.2 State machine

The state machine is one of the key blocks to achieve reconfigurable speed and scalable power, and it generates different control signals according to various sampling rate requirements, i.e. Fs, Fs/2, Fs/4…Fs/256. The control signals are fed into "AND" gates together with the non-overlapping clock generator's outputs to generate the actual clocking control signals for the switches in each stage. Fig. 2.5 (a) shows an example of how the control signals from the state machine and the clock signals from non-overlapping clock generator generate the actual clocking signals for Fs/2. Fig. 2.5 (b) shows the state machine control signals for stages 1-10 at Fs/2, and Fig. 2.5 (c) shows the

state machine control signals for one stage at various sampling rates. Note that there is a larger latency (largest for Fs/256) for the control signal at lower effective sampling rate.



(a)



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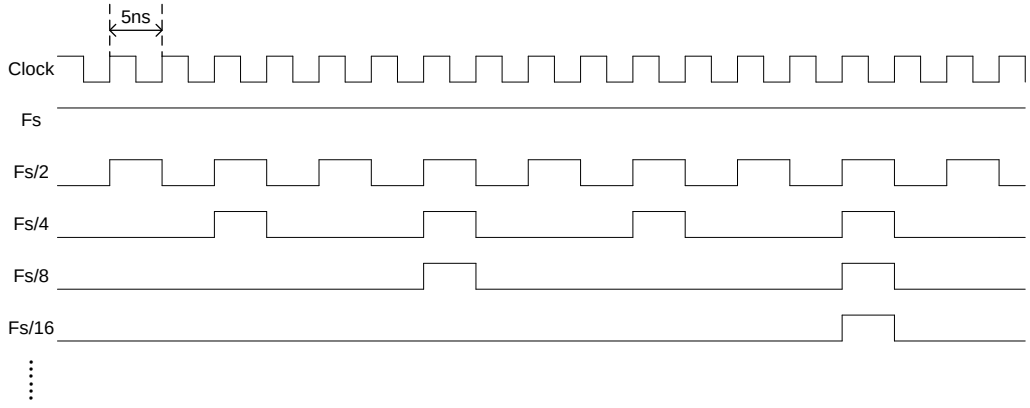


(c)

Fig. 2. 5. State machine output: (a) sampling rate: Fs/2 (b) control signal for stage 1-10 @ Fs/2 (c) control signal for various sampling rates (Fs, Fs/2, Fs/4, etc) for one stage.

One challenge of achieving good power scalability is that a portion of the digital control logic is always kept active, which ultimately limits further scaling down of power consumption [5].

2.4 Building block design

2.4.1 Non-overlapping clock generator

For typical pipeline ADCs, a two-phase, non-overlapping clock signal is generated for all the pipeline stages. All the odd stages sample during phase ϕ_2 and provide a valid residue output to the next stage during phase ϕ_1. All the even stages work on the opposite phases, so that all stages operate concurrently. For the proposed reconfigurable ADC, a non-overlapping clock generator is also needed. But the non-overlapping signals do not go to each stage directly. Instead, they are ANDed with the outputs of the stage machine first and then present to each stage. Fig. 2.6 shows the non-overlapping clock generator used in this project [22]. The input CLK is driven by an external 50% duty-cycle reference clock. The non-overlapping clock signals are shown in Fig. 2.7.

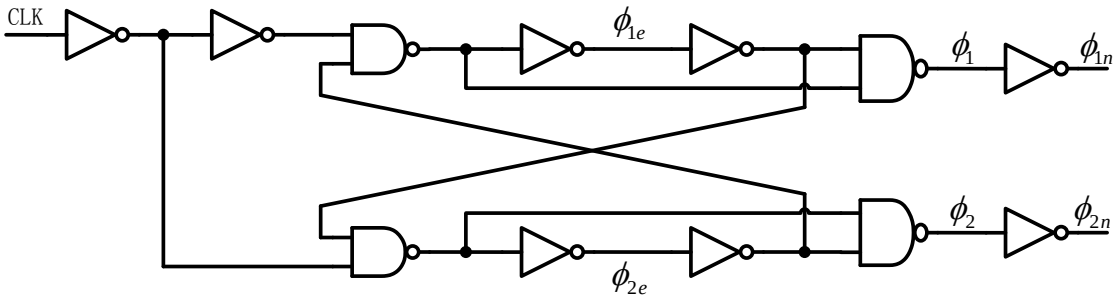


Fig. 2. 6. Non-overlapping clock generator

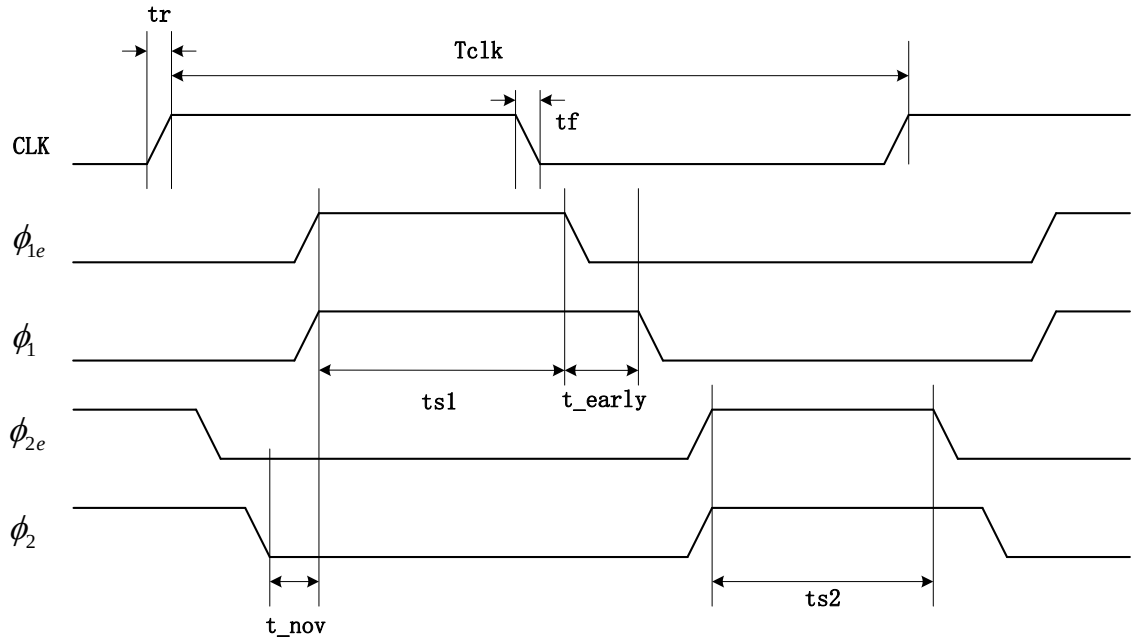


Fig. 2. 7. Non-overlapping clock timing

At the top of the figure the reference clock CLK is shown with a period of Tclk and rise and fall times of tr and tf respectively. The duration of the dependent phases is a function of the propagation delays of the various gates in the clock generator. By adjusting these delays, the designer can allocate the time spent in each of the phases. The ts1 is the opamp settling time for pipeline stages that generate an output during phase ϕ_1. The ts2 is the opamp settling time for pipeline stages that generate an output during phase ϕ_2. Typically these are designed to be as equal as possible. The t_early is the time between the early clock ϕ_{1e} and the regular clock ϕ_1. This delay ensures that the bottom plate switch of the sample and hold is opened first to reduce signal-dependent charge injection. The t_nov is the non-overlapping interval during which neither phase is active. For proper operation of the two-phase circuits this overlap must be non-zero.

2.4.2 Stage machine

As shown in Fig. 2.4, a state machine generates the signals for controlling the duty cycles of each MDAC stage. Fig. 2.8 (a) shows how the control signal of the first stage is generated. An 8-bit asynchronous counter and a three-to-eight decoder are designed to configure the sampling rate. The counter is composed of eight falling edge-triggered D flip-flops (DFFs). Phase Φ2 from the non-overlapping clock generator is used as the clock for the first DFF. For each DFF, output $\bar{Q}$ connects to its own input D and also to the clock of its following DFF. The output of the three-to-eight decoder controls eight DFFs to select different sampling rate. For example, all of the eight DFFs are disabled for the sampling rate of Fs. For Fs/2, only the first DFF is enabled and the other seven DFFs are disabled. For Fs/4, the first two DFFs are enabled and the other six DFFs are disabled, and so on. Notice that the control signal has an variable duty cycle, which is 50% for Fs/2, 25% for Fs/4, 12.5% for Fs/8, etc. Also, the delay of the circuit is determined only by the first DFF and its following logic gates since the output only changes when the first DFF output changes from 0 to 1. Thus, the delay time is fixed during different sample rates.

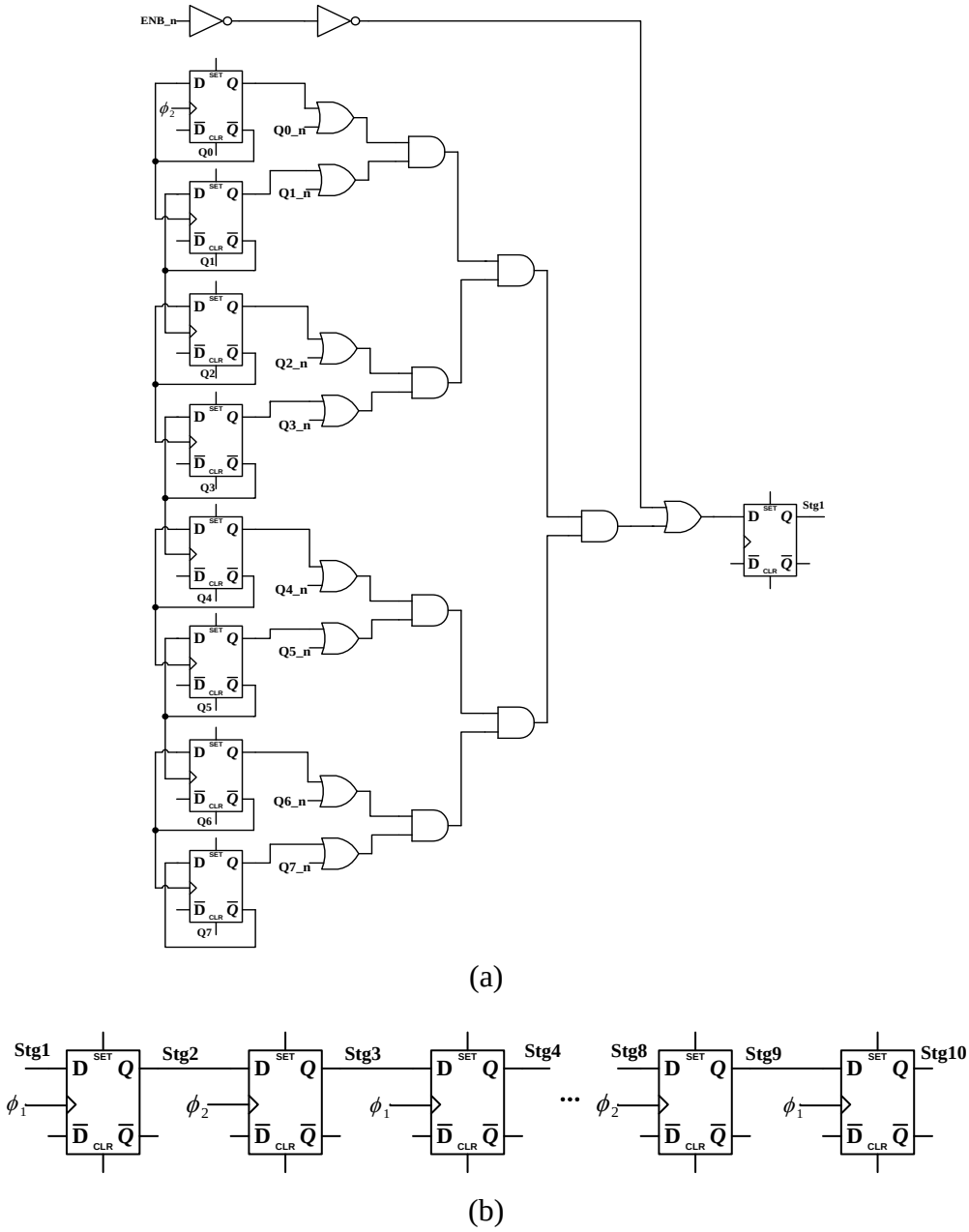


Fig. 2. 8. Control bit generator: (a) for stage 1 (b) for other stages.

Fig. 2.8 (b) shows the control signal generator for stages 2-10. The signal of each stage is delayed by Ts/2 compared to its previous stage. For each stage, there is one

falling-edge-triggerred DFF whose input is the control signal of the previous stage. The hold phase clock of each stage serves as the clock for the corresponding DFF.

2.5 Measurement results

The ADC was designed and fabricated in UMC 90nm Logic/Mixed mode CMOS process. Fig. 2.9 shows the chip micrograph. The active area occupies 1.6mm by 0.95mm.

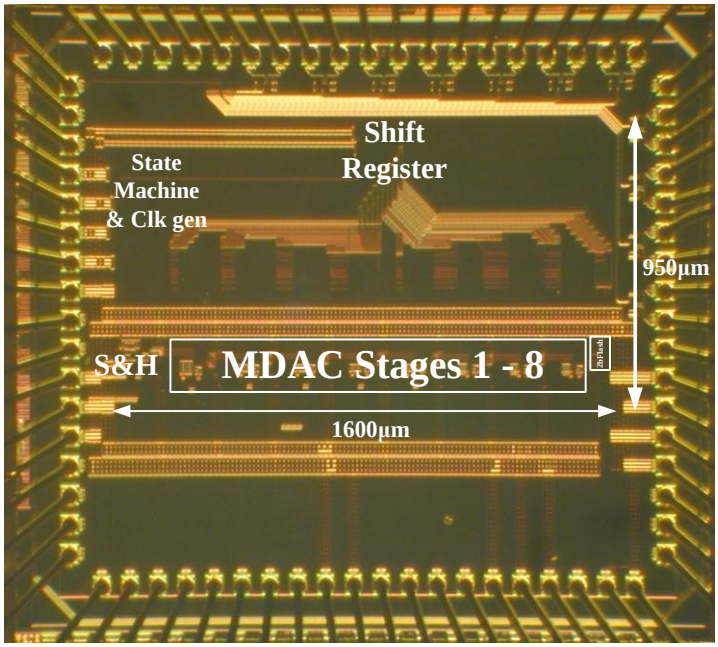
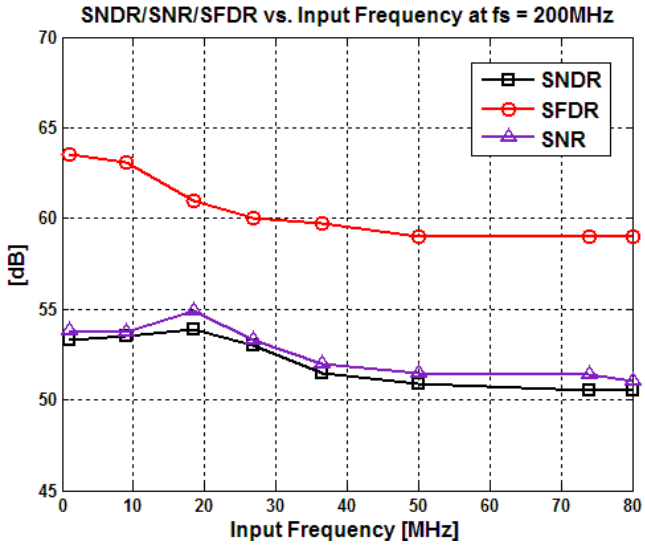


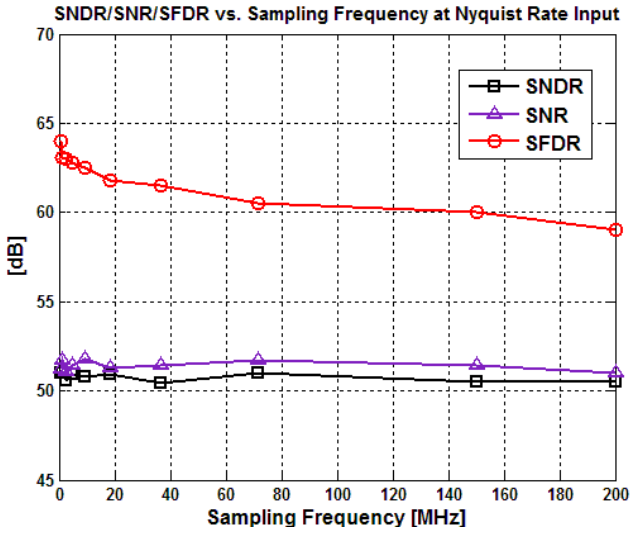
Fig. 2. 9. Chip micrograph

Fig. 2.10 shows the measured SNR, SNDR, and SFDR of the ADC versus sampling rate for Nyquist-rate inputs. Fig. 2.10 also shows the SNR, SNDR, and SFDR of the ADC versus input frequency at fs = 200MHz, which is the upper end of the ADC speed-reconfiguration range. The SNDR varies less than 3dB within the entire speed programming range, while the SFDR varies less than 4dB. This consistent performance over a wide speed range is as expected because the bias current are kept constant when we are programming the ADC speed, therefore the circuit works robust. The measured

DNL is less than -0.6/+0.76LSB, and the measured INL is less than -2.1/+1.5 LSB, as shown in Fig. 2.11. During these measurements the input signal swing was 1Vpp at 1.1V supply, and the power was scaled from 1.9mW to 27mW. This power includes the ADC core power (amplifiers, biasing circuits, comparators, clock generator, and digital logic), excluding reference.

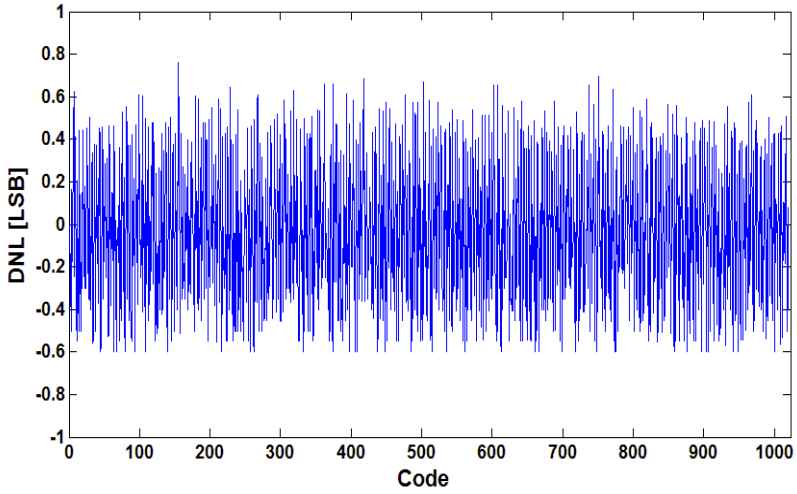


(a)

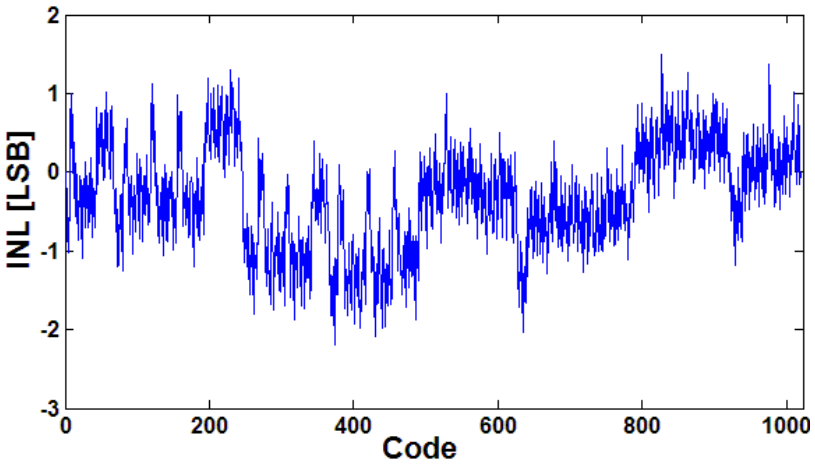


(b)

Fig. 2. 10. Measured dynamic performance summary (a) SNDR/SFDR/SNR vs. Input Frequency at Fs = 200MHz; (b) SNDR/SFDR/SNR vs. Fs



(a) DNL @ 200MSPS: -0.6/+0.76LSB.



(b) INL @ 200MSPS: -2.1/+1.5LSB.

Fig. 2. 11. Measured static performance summary (a) DNL (b) INL

The proposed ADC can adapt its power consumption to the required speed. Fig. 2.12 plots the power dissipation vs. speed (sampling rate fs), with fs swept from 0.58MSPS to 200MSPS. Note that the power is proportional to the effective sampling frequency. Fig. 2.12 also compares this work with the state-of-art reconfigurable 10bit pipelined ADCs, the proposed reconfigurable ADC obtains the widest speed

programming ratio with the highest sampling rate among state-of-the-art reconfigurable ADCs, while achieving a competitive FOM.

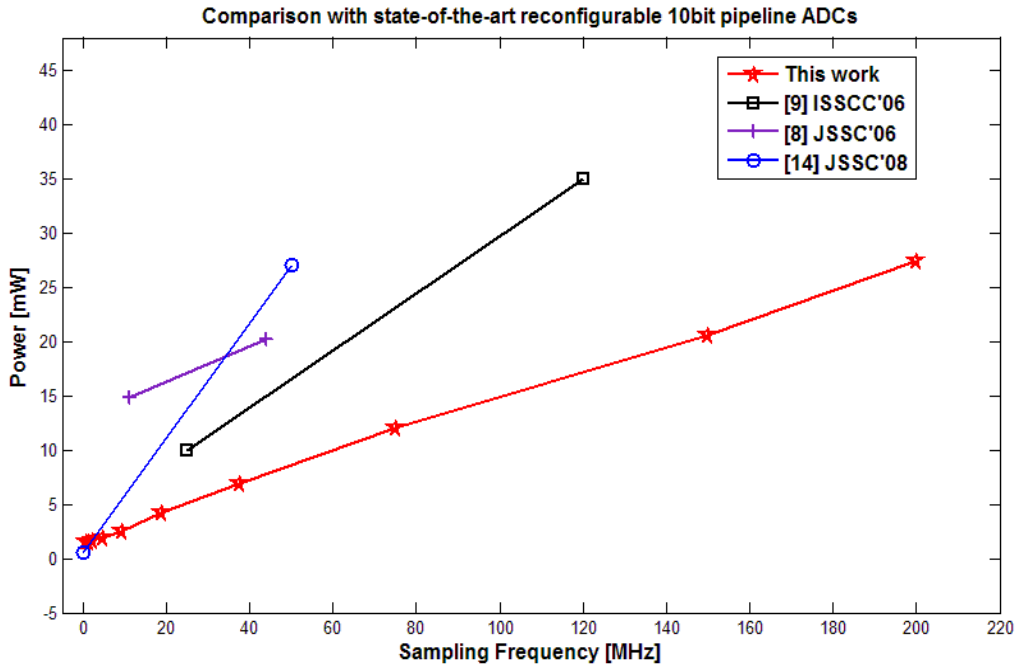


Fig. 2. 12. Power vs. sampling rates and Comparison with state-of-the-art reconfigurable 10bit pipeline ADCs

A comparison of state-of-art reconfigurable ADCs is listed in Table 2.3. The current scaling technique yields good power stability, but limited speed programming range. The hybrid pipeline/cyclic approach has sub-optimal power consumption because there is no stage scaling; the time-interleave technique also has limited speed programming range, and it requires complex clock distribution and involves mismatch problem for increased number of parallel branches. The proposed reconfiguration technique achieves a wide speed program ratio with the highest sampling rate.

Table 2. 3. Comparison of state-of-art reconfigurable ADCs

	Resolution	Speed (MSPS)	Power	Process	Technique
This Work	10bit	0.58-150	1.9-27mW	90nm	
[7]	10bit	25-120	0.3mW/Msample	90nm	Current Scaling
[19]	10bit	3-220	90mW@120M 135mW@220M	0.13µm	Current Scaling
[9]	6-10bit	20/40/80	30.3/52.6/93.7mW	0.18µm	Hybrid Pipeline/Cyclic
[5]	10bit	0.001-50	15µW-35mW*	0.18µm	Sleep mode + Current scaling
[8]	10bit	11/44	14.8/20.2mW	0.25µm BiCMOS	Time interleave +current scaling

* The digital power is not included

3. THE CONTINUOUS TIME SIGMA-DELTA MODULATORS

3.1 Introduction

Analog to digital converters are widely used mixed-signal devices that convert analog signals (continuous in time and amplitude) to digital signals (discrete in time with finite amplitude), which serve as a bridge between analog and digital signals. According to the ratio of sampling frequency and Nyquist sample rate, ADCs can be classified as Nyquist rate ADCs and oversampled ADCs. For Nyquist ADCs, the sampling frequency is two times the input signal frequency. However, the sampling frequency of oversampled ADCs is much greater than (usually >10) the bandwidth of the input signal. The continuous time sigma-delta modulators belong to oversampled ADCs.

Modern wireless communication systems require A/D converters with increasing bandwidth and resolution to support new standards with higher data rates [23]. [24]-[26] show CT ∑Δ modulators have high resolutions with low power consumption. Moreover, CT ∑Δ modulators provide inherently anti-alias filtering function so that an anti-alias filter can be removed in the receiver. Another advantage is that CT ∑Δ modulators can work much faster because of the relaxed requirements of high speed OPAMPs and the settling time of the circuitry.

In this section, the fundamentals of CT ∑Δ modulators are presented, followed by the non-idealities in designing CT ∑Δ modulators. Finally, a proposed CT BP ∑Δ modulator for wireless communication systems is discussed.

3.2 Basics of CT sigma delta modulators

3.2.1 Quantization noise

When the continuous time analog signal is approximated with the nearest smaller reference level, it generates quantization error, which is the difference between the original input and the digitized output [27]. The quantization error can be modeled as additive noise with uniformly distributed between $\pm V_{LSB}/2$. The quantization noise power can be expressed as [27]:

$$\overline{\varepsilon_q^2} = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} \varepsilon_q^2 \, d\varepsilon_q = \frac{\Delta^2}{12} \tag{3.1}$$

where $\Delta = V_{LSB}$. The signal-to-quantization noise (SQNR) is given by [27]:

$$SQNR = 6.02N + 1.76\ dB \tag{3.2}$$

where N is the number of bits of a ADC.

3.2.2 Oversampling advantage

Oversampling occurs when the sampling frequency f_s is larger than two times of the signal bandwidth f_0, or $f_s > 2f_0$. The oversampling ratio (OSR) is defined as [28]

$$OSR \equiv \frac{f_s}{2f_0} \tag{3.3}$$

For a system as shown in Fig. 3.1, a low pass filter is introduced after the N-bit quantizer to eliminate quantization noise (together with any other signals) greater than f_0. So the quantization noise of oversampling ADCs is less than that of Nyquist ADCs:

$$P_{Q,oversampling} = \frac{P_{Q,Nyquist}}{OSR} \tag{3.4}$$

The SQNR can be expressed as [29]

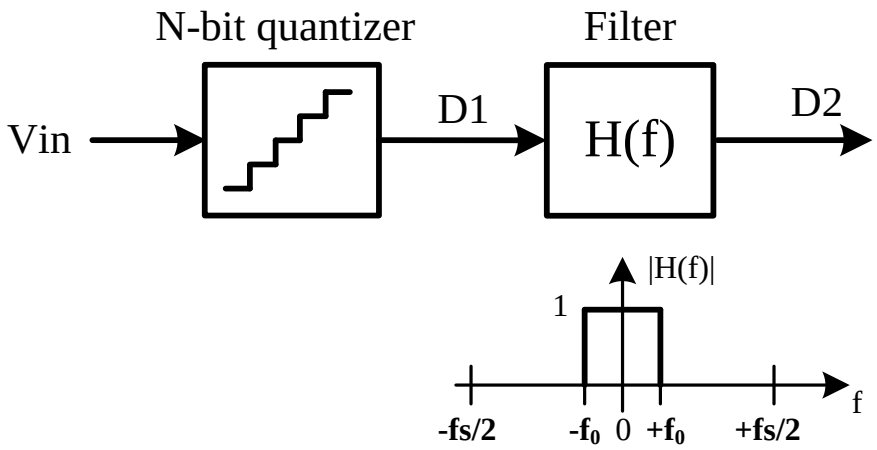


Fig. 3. 1. A oversampling system without noise shaping

$$SQNR = 10\log\left(\frac{P_S}{P_Q}\right) = 6.02N + 1.76 + 10\log(OSR) \tag{3.4}$$

This equation shows the main oversampling advantage: SQNR is improved by 3dB when doubling the sampling frequency.

3.2.3 Noise shaping

A single loop CT ∑Δ modulator is shown in Fig. 3.2. The ∑Δ modulator is a closed-loop negative feedback system, which is composed of a loop filter, a quantizer and a feedback digital-to-analog converter (DAC). Assuming small signal condition, then a linearized model can be used for the non-linear quantizer, and a unity gain for the quantizer and feedback DAC, therefore, the modulator output is obtained [28]

$$D_{out} = STF \times V_{in} + NTF \times Q_n \tag{3.5}$$

where STF and NTF are the signal and noise transfer functions, and Qn is the equivalent quantization noise. The STF and NTF can be expressed as:

$$STF = \frac{D_{out}}{V_{in}} = \frac{H(s)}{1+H(s)} \tag{3.6}$$

$$NTF = \frac{D_{out}}{Q_n} = \frac{1}{1+H(s)} \tag{3.7}$$

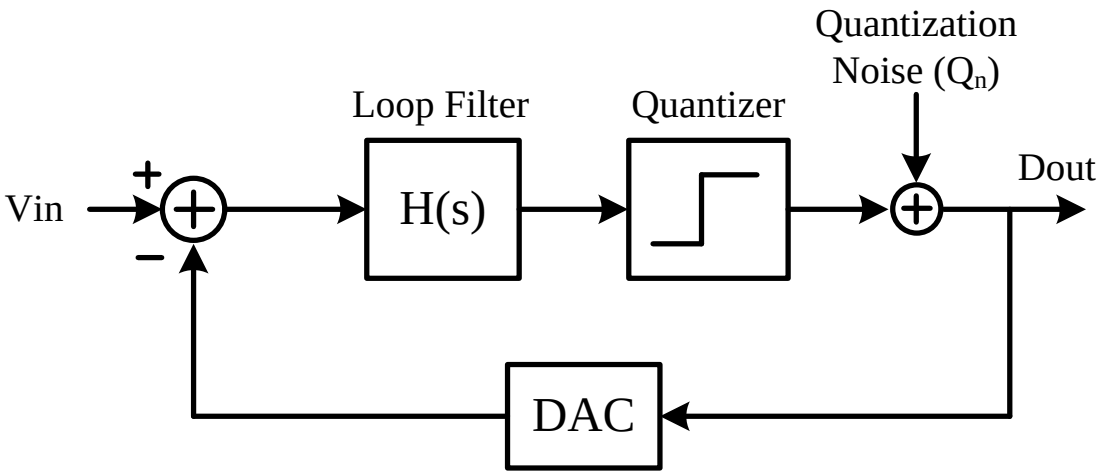


Fig. 3. 2. Diagram of single loop CT ∑Δ modulator

The digital output D_{out} then passed through decimation and digital filter blocks, where the out of band noise is filtered out and down sampling is performed to achieve the final output. As long as the in-band |H(s)|>>1, $STF \approx 1$ and $NTF \approx 0$. This means that the quantization noise is attenuated by the loop filter, while the input signal appears at the output of the modulator without any attenuation in the bandwidth of interest.

In summary, the noise shaping attenuates the quantization noise further and increases the SQNR of CT ∑Δ modulators as shown in Eq. (3.8)

$$SQNR = \left[\frac{STF \bullet V_{in}}{NTF \bullet Q_n}\right]^2 \cong \left|H(s)\right|^2 \left[\frac{V_{in}^2}{Q_n^2}\right] \tag{3.8}$$

3.2.4 Inherent anti-aliasing filtering

Due to the sampling operation, any input frequency f_{in} which is larger than half the sampling frequency f_s will reflect into the frequency range $0 < f < \frac{f_s}{2}$, which is the know problem of aliasing [30]. DT ∑Δ modulators usually require an extra analog filter in front of the sampler to bandlimit the input signal and hence reduce the aliasing effect. However, the sampling in CT ∑Δ modulators occurs at the output of the CT loop filter. Thus the loop filter operates as an anti-aliasing filter and there is no need for an anti-aliasing filter in front of CT ∑Δ modulators. The inherent anti-aliasing filtering is another important advantage of CT ∑Δ modulators. The frequency response of the inherent anti-aliasing filter in typical CT ∑Δ modulators is given by [31]

$$F_{aa}(\omega) = \frac{\hat{H}(j\omega)}{H(e^{j\omega T})} \tag{3.9}$$

where $\hat{H}$ is the CT modulator loop filter and H is its DT equivalent.

3.3 Non-idealities in continuous time sigma-delta modulators

The NTF is degraded by non-idealities in a CT ∑Δ modulator which result in an increase in the integrated noise power over the required signal bandwidth and a decrease in SNR at the modulator output. The non-idealities may also lead to loss of loop stability in certain cases (e.g. clipping in the internal nodes). So it is necessary to take the non-

idealities into account during the design process.

3.3.1 Clock jitter

The ideal clock signal is periodic in nature with consecutive rising and falling edges separated in time from each other by exactly T_s seconds. However, due to circuit non-idealities (thermal noise, cross-coupling etc.), the clock signal deviates from ideal behavior and the clock edges occur at time instants of [N∗T_s+σ t] seconds (N is an integer). The deviation of edges from ideal behavior every cycle (σ t) is known as clock jitter and it is usually specified as rms (root mean square) value by considering the jitter samples over a large number of clock cycles. Typically, rms clock jitter can be less than 1ps in modern technology.

The clock jitter causes a random variation in the pulse widths of feedback DACs and adds a random phase noise to the output bit stream. Since the first DAC output is added to the input analog signal directly, the clock jitter degrades the ADC performance. If a non-return-to-zero (NRZ) DAC is used, jitter only affects when the output changes. However, in a return-to-zero (RZ) or a half-return-to-zero (HRZ) DAC, the pulse has both rising and falling edge during every clock cycle. So the error term due to NRZ DAC is much lower than the error term due to RZ/HRZ DAC.

3.3.2 Excess loop delay

In a CT ∑Δ modulator, the output of quantizer drives feedback DACs and the output of DACs inject current or voltage back to the filter and close the loop. Ideally, the

outputs of DACs respond immediately to the quantizer clock edge. However, transistors in DACs and comparator cannot switch instantaneously. The excess loop delay is caused by the fact that the time from the sampling clock edge in the quantizer until the output is fed back to the filter is not the specified clock period delay. A time delay (T_d seconds) block can be represented as e^{-sT_d} in CT domain and as z^{-T_d/T_s} in DT domain. The delay effect can be modeled by including the delay block representation in cascade with the loop transfer function. The excess loop delay modifies the loop transfer function and may cause SNR degradation and even stability problem [32][33].

Another harmful effect of excess loop delay is that it increases the order of the modulator, which leads to stability problems when the delay time is high [33]. [34][35] reported several techniques (DAC pulse tuning, feedback coefficient tuning and additional feedback parameters) to resolve excess loop delay problems.

3.3.3 Linearity

Transconductance nonlinearity introduces harmonic distortions, especially the third harmonic distortion. The harmonics will generate harmonic tones, increase in-band noise floor and decrease the system SNDR [32][36]. The major contribution of distortion comes from the nonlinear behavior of transistors in the loop filter, thus transconductances used in such block need to be highly linear to achieve high SNDR performance. Increasing the V_{dsat} of the input transistors improves the linearity and reduces the distortion. The penalty is that the input voltage headroom is reduced. Source degenerated differential pairs are mostly used in the transconductor's input to improve the integrator linearity. The suppression of distortion will inevitably come at the cost of power

consumption [37].

3.3.4 Comparator metastability

The comparator is usually implemented as a cascade of a gain amplifier and a regenerative latch. The regenerative latch is a positive feedback circuit which amplifies the voltage difference at the input to a level that can be consider digital. The regenerative circuit of the digital latch can be modeled as two identical single pole inverting amplifiers each with a small signal gain of $-A_0$ ($A_0 > 0$) and a characteristic time constant of τ_0 [27]. The voltage difference at the input increases exponentially with a time constant that is inversely proportional to the gain bandwidth (GBW) product of the latch. When the input to the comparator is very small, the regeneration time of the latch becomes a significant part of the clock period and the output of the comparator cannot reach the decision levels. This causes the zero crossing time of the output (propagation delay of the latch) to be variable function of the input signal. This effect is called metastability and it causes uncertainty in the comparator output. The comparator output drives the DAC's and the comparator metastability has the same effect as clock jitter in that it causes a random variation of the rising/falling edges and increases the noise floor. The most common approach to overcome this problem is to use a cascade of latch stages in order to provide more positive feedback (gain) for the regeneration process, which results in lower uncertainty of the digital output [38]. The main drawback of this approach is that an additional half cycle delay ($z^{-1/2}$) in the feedback loop results by the addition of two digital latch stages, each driven by opposite differential clock phases. However, this can be resolved by tuning the feedback parameters [34].

3.3.5 Quality factor of the loop filter

The definition of quality factor (Q) of an energy storage system can be expressed as

$$Q = 2\pi * \frac{energy\ stored\ per\ cycle}{energy\ dissipated\ per\ cycle} \tag{3.10}$$

Q is dimensionless and indicts the amount of loss in the system. When the value of Q is high, the loss in the system is low and vice versa. The quality factor of an LC tank is given by

$$Q_{LC\_tank} = \frac{R}{\omega_0 L};\ \omega_0 = \sqrt{\frac{1}{LC}} \tag{3.11}$$

where *R* is the series resistance. In a CT BP ∑Δ modulator, the Q of the bandpass filter will affect the noise transfer function (NTF). This can be illustrated by considering a second order CT BP ∑Δ modulator. Its NTF is given by [33]

$$NTF = \frac{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2 + As} \tag{3.12}$$

The magnitude of the NTF at the center frequency is given by

$$\left|NTF\right|_{s=j\omega_0} = \frac{\omega_0}{\omega_0 + AQ} \tag{3.13}$$

The value of (3.13) approaches zero for very high values of Q, which means the modulator can achieve better SNR performance with higher Q. However, higher Q increases the gain of the bandpass filter at its center frequency $\frac{AQ}{\omega_0}$. Thus the signal swing in the internal nodes of the modulator is increased, which may clip the voltages

and result in unstable behavior. So, the optimum value of Q is a tradeoff between the maximum attainable SNR and stable operation.

3.4 Proposed CT bandpass ∑Δ ADC

The proposed CT bandpass ∑Δ ADC is targeted for the software radio receiver. The input frequency range covers 2-4 GHz RF carrier signal modulated with over 20 MHz bandwidth baseband signal. The specifications are shown in Table 3.1.

Table 3. 1. Specifications of the proposed CT bandpass ∑Δ ADC

Parameter	Value
Input frequency (f_0)	2 - 4 GHz
Clock frequency ($4*f_0$)	8 - 16 GHz
Bandwidth	≥20 MHz
ENOB	10 bits
Power consumption	< 500 mW
Technology	TSMC 0.13um CMOS

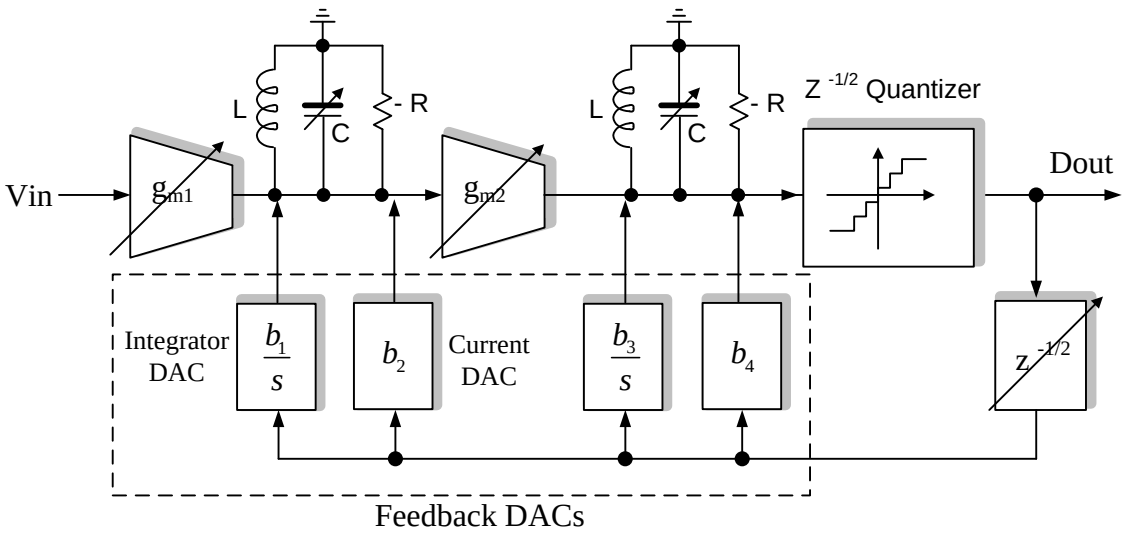


Fig. 3. 3. Block diagram of the proposed CT bandpass ∑Δ ADC

The block diagram of the proposed CT bandpass ∑Δ ADC is shown in Fig. 3.3. The loop filter in the forward path is a fourth order continuous time LC bandpass filter that is implemented as a cascade of two second order LC filters. The LC tank shunts with a Q enhancement block (negative resistor, -R) to compensate the losses in the inductor and capacitor. The transconductance blocks, g_{m1} and g_{m2}, are used to convert the input voltage into current, which is then injected into the LC tank. The comparator samples the filter output and gives a two-bit digital bit stream as output. The feedback path is a linear combination of four paths; two quasi-lossless integrator DAC paths and two current DAC paths. The DAC blocks convert the digital output to current (analog domain), which is injected back into the LC tank. The main difference between a current DAC and the integrator DAC is that the gain of the latter is frequency dependent, which is evident from its transfer function.

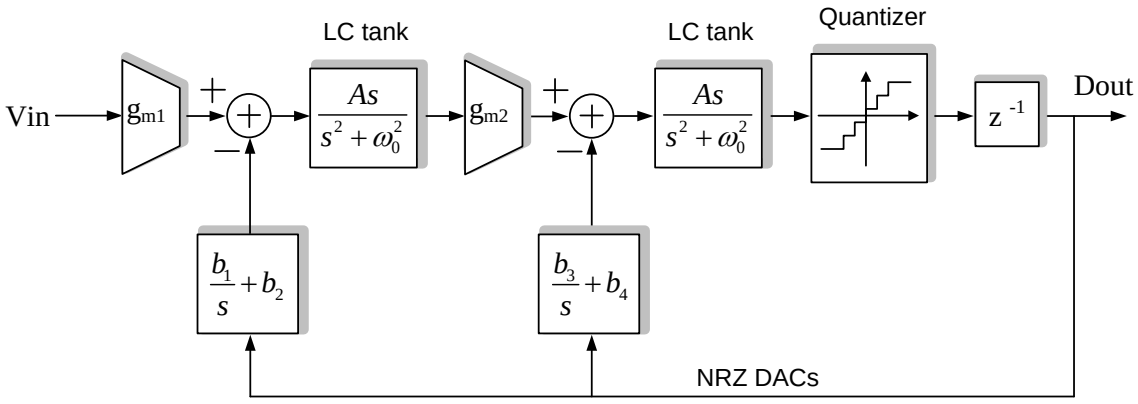


Fig. 3. 4. System diagram of the proposed CT bandpass ∑Δ ADC

The system diagram of the proposed CT bandpass ∑Δ ADC is shown in Fig. 3.4. The open loop transfer function can be obtained [33]:

$$H_{loop}(s)=\frac{s^3Ab_4+s^2(A^2g_{m2}b_2+Ab_3)+s(A^2g_{m2}b_1+A\omega_0^2b_4)+A\omega_0^2b_3}{(s^2+\omega_0^2)^2} \tag{3.10}$$

where

$$\begin{cases} A=\dfrac{1}{C} \\ \omega_0^2=\dfrac{1}{LC} \end{cases} \tag{3.11}$$

From Eq. (3.9) we can see that the transconductance of the first stage, g_{m1}, doesn't affect the loop transfer function. It is used to transfer the input voltage into current and inject into the bandpass filter. The value of g_{m1} also defines the dynamic range of the ADC. The role of g_{m2}, the transconductance of the second stage, is more important. The transconductor g_{m2} not only determines the output signal swing, also affects the loop transfer function. Its value should be chosen carefully considering linearity, signal swing,

noise and power consumption. The center frequency (f_0) of the bandpass filter, which can be tuned from 2 to 4 GHz, is defined by both the inductance L and the capacitance C. The inductance L is fixed and its value depends on technology and geometry. The capacitance C is implemented by a capacitor bank with wide tuning range. The parameters at several typical frequencies can be calculated as shown in Table 3.2 [39].

Table 3. 2. Parameters at several typical frequencies

Parameters	Center frequency		
	f_0 = 2.0 GHz	f_0 = 2.5 GHz	f_0 = 3.0 GHz
L (nH)	2.0	2.0	2.0
C (pF)	3.17	2.03	1.41
b1 (Amps*rad/Volt*sec)	2.53×10^8	2.03×10^8	1.69×10^8
b2 (Amps/Volt)	0.020157	0.012901	0.008959
b3 (Amps*rad/Volt*sec)	3.75×10^8	3.75×10^8	3.75×10^8
b4 (Amps/Volt)	0.033456	0.026765	0.022304
g_{m2} (mA/V)	25	25	25

The circuit implementation of the 2-bit quantizer and feedback DACs are discussed in section 4 and section 5, respectively.

4. DESIGN OF A 2-BIT QUANTIZER WITH TUNABLE DELAY

4.1 Introduction

The quantizer samples and digitizes the filter output. Here a 2-bit quantizer is implemented for the 2-4 GHz tunable CT BP ∑Δ converter. The sampling clock can be tuned from 8-16 GHz which is four times the loop resonant frequency. The block diagram of the quantizer is shown in Fig. 4.1. The quantizer is composed of three identical branches. Each branch includes preamplifier, latched comparator, latch 2, latch 3 and latch/buffer stages. The preamplifier amplifies the difference between differential input signal and differential reference voltage. It can also reduce the kickback noise from the latched comparator. Since the sampling frequency is really high, CML type comparator is chosen for the latched comparator. The CML circuits have fast speed and low output voltage swing instead of rail-to-rail logic swing. However, the power consumption is much higher than the static logic circuits.

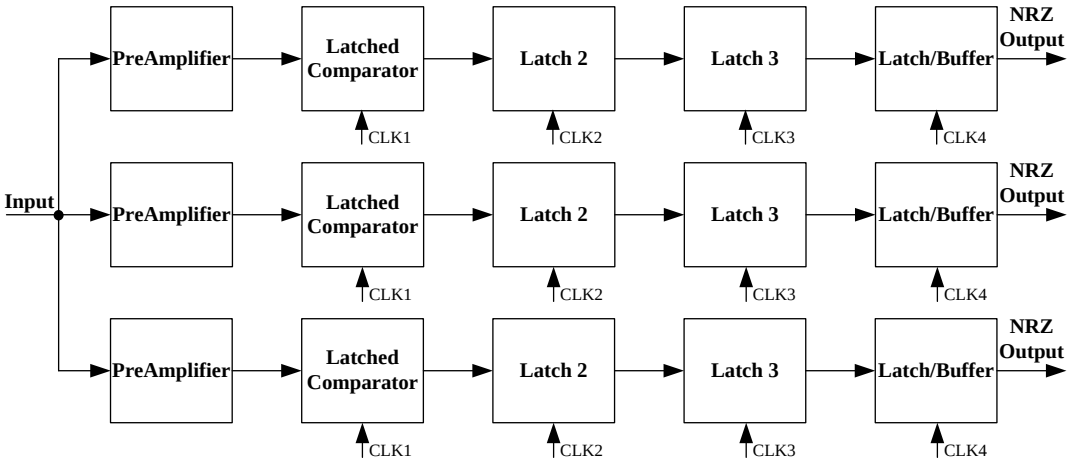


Fig. 4. 1. Block diagram of the 2-bit quantizer

The latched comparator works in two phases – tracking and regeneration phase – which are controlled by CLK1. When CLK1 is high, it works in tracking phase where the comparator tracks the input signal. When CLK1 is low, it works in regenerations phase where the comparator regenerates the input signal. Another two cascade latches – latch 2 and latch 3 – are introduced for two reasons: 1) The regeneration gain is increased a lot so that the metastability of the comparator is reduced. 2) The excess loop delay can be tuned by adjusting the clocks CLK2 and CLK3. The last stage is a reconfigurable latch/buffer stage which is controlled by CLK4. At high frequency, CLK4 is always high and the last stage is a buffer. At low frequency, CLK4 is a clock signal and the last stage is a latch. It is because latch has more time delay than the buffer. There is not enough delay time margin for the last stage at high frequency.

4.2 Circuit implementation of quantizer building blocks

4.2.1 Preamplifier stage

The preamplifier is the first stage of the quantizer. It is composed of two differential pairs, load resistors and shunt peaking inductor, which is shown in Fig. 4.2. The preamplifier provides amplified difference voltage between the differential input and the differential reference to the following latched comparator. The preamplifier also isolates the bandpass filter with the latched comparator to reduce the kickback noise [27]. The main concerns in the design of the preamplifier are bandwidth, gain, loading effect to the previous bandpass filter and offset.

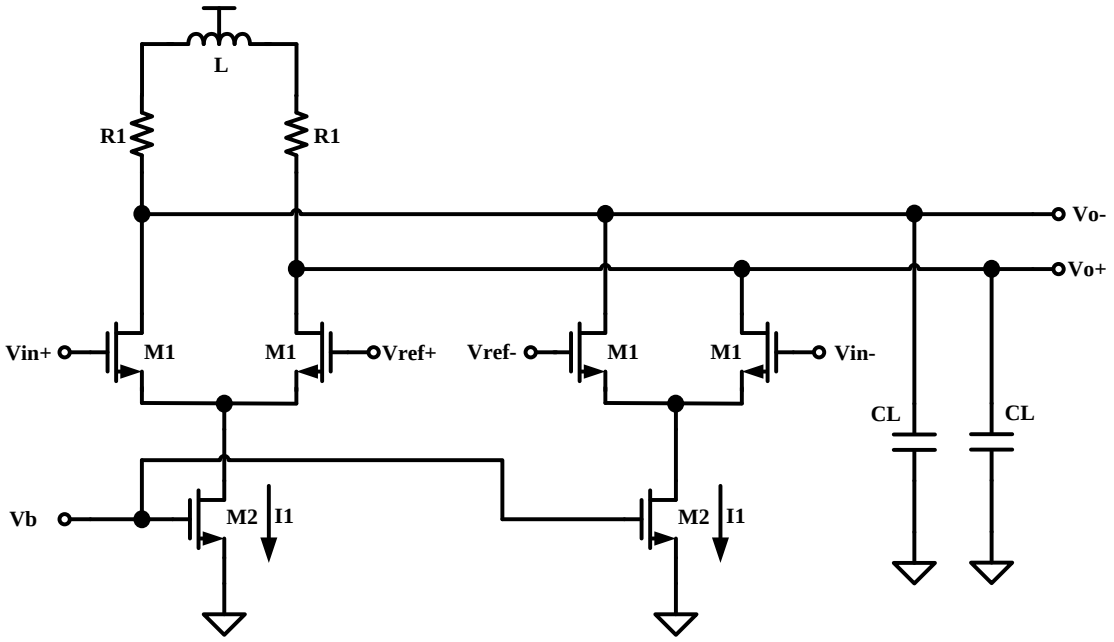


Fig. 4. 2. Schematic of the preamplifier

Considering small-signal equivalent circuit of the preamplifier without shunt peaking inductor,

$$\begin{aligned} V_{o+} - V_{o-} &= g_{m1}\left(V_{in+} - V_{ref+} + V_{ref-} - V_{in-}\right) R_1 \| C_L \\ &= \frac{g_{m1}R_1}{1+sR_1C_L}\left[\left(V_{in+} - V_{in-}\right) - \left(V_{ref+} - V_{ref-}\right)\right] \end{aligned} \tag{4.1}$$

Then we have

$$A(s) = \frac{V_{o+} - V_{o-}}{\left(V_{in+} - V_{in-}\right) - \left(V_{ref+} - V_{ref-}\right)} = \frac{g_{m1}R_1}{1+sR_1C_L} \tag{4.2}$$

The low frequency gain and bandwidth are given by

$$\left|A_{DC}\right| = g_{m1}R_1 \tag{4.3}$$

$$\omega_{-3dB} = \frac{1}{R_1C_L} \tag{4.4}$$

The bandwidth of the pre-amplifier should be high enough to reduce the signal delay. Since the clock frequency is very high and our technology is not that advanced, a shunt peaking inductor is introduced to improve the bandwidth [40]

$$\frac{\omega_{-3dB,with\ peaking}}{\omega_{-3dB,without\ peaking}} = \sqrt{\left(-\frac{m^2}{2}+m+1\right)+\sqrt{\left(-\frac{m^2}{2}+m+1\right)^2+m^2}} \tag{4.5}$$

where

$$m = \frac{RC}{L/R} \tag{4.6}$$

The bandwidth can be improved by more than 50% by choosing appropriate value of *m*. The AC performance comparison with and without shunt peaking inductor (*m*=3) is shown in Fig. 4.3. The bandwidth is increased by 56% by implementing shunt peaking inductor in the preamplifier.

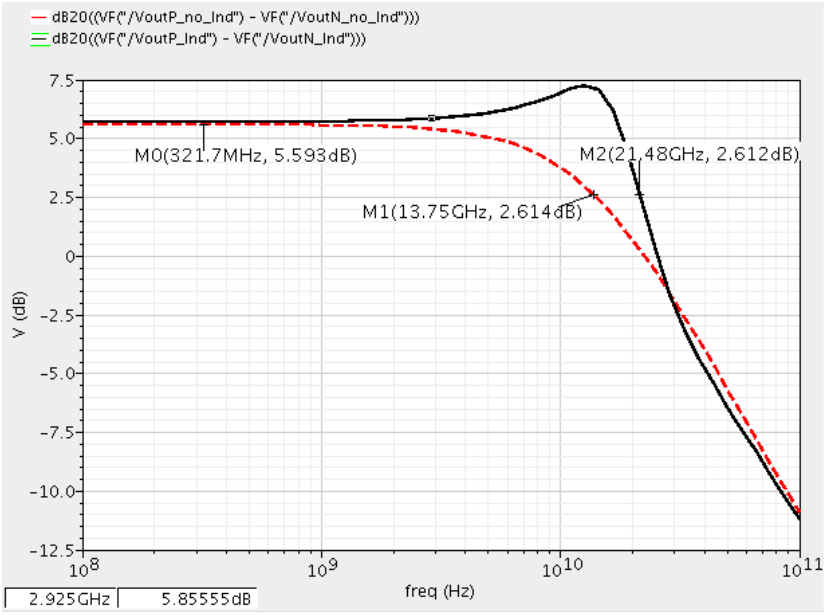


Fig. 4. 3. AC simulation results of the preamplifier

Another requirement of the preamplifier is the input-referred offset voltage, which can be expressed as [41]

$$V_{os,in}^2 = (\frac{V_{GS} - V_{TH}}{2})^2 \left\{ \left(\frac{\Delta R_D}{R_D} \right)^2 + \left(\frac{\Delta(W/L)}{(W/L)} \right)^2 \right\} + \Delta V_{TH}^2 \quad (4.7)$$

where R_D is the load resistor, W and L are the width and length of the MOSFETs, respectively. In order to reduce the input-referred offset voltage, we can make V_{GS}-V_{TH} smaller, increase the transistor dimensions while keeping the bias current constant and employ good matching techniques in the layout. For the quantizer in this project, 1 LSB=50 mV so that the $V_{os,in}$ should be less than 0.5LSB, which is 25 mV.

The final design of the pre-amplifier yields a gain of 5.6 dB, with 21.5 GHz bandwidth and input-referred offset voltage 1.6 mV. The component values and parameters are listed in Table 4.1. The reference voltages for different branches are shown in Table 4.2.

Table 4. 1. Transistor sizes and bias conditions for the pre-amplifier

Parameters	Value
M1 (W/L/NF)	2um/0.13um/18
M2 (W/L/NF)	12.5um/0.5um/32
R1	90 ohms
L	0.96 nH
I1	5 mA
VDD	1.8 V

Table 4. 2. Reference voltages for each branch

Branch	Vref+ (V)	Vref- (V)
2	0.95	0.85
1	0.9	0.9
0	0.85	0.95

4.2.2 Latched comparator

The schematic of the latched comparator is shown in Fig. 4.4. A shunt peaking inductor is also added to improve the speed of the comparator [40]. When the differential clock signal is high, the latched comparator works in the tracking phase as shown in Fig. 4.5. The differential pair formed by transistors M1 is active and it amplifies the input signal. At the time instant of the falling clock edge, the signal is sampled and the value at this time instant becomes the initial condition for the next clock phase. When the clock is low, the latched comparator works in the regenerative phase as shown in Fig. 4.6. The cross coupled differential pair formed by transistors M2 is active and the output reaches either logic 0 or 1.

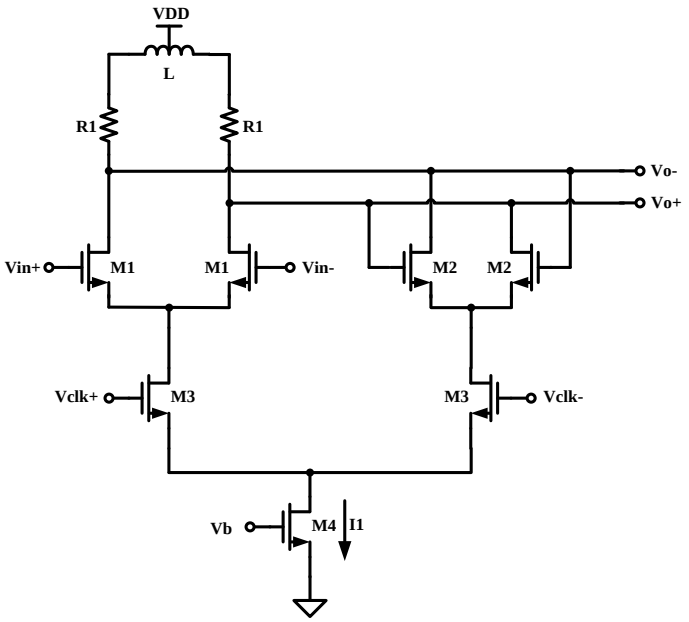


Fig. 4. 4. Schematic of the latched comparator

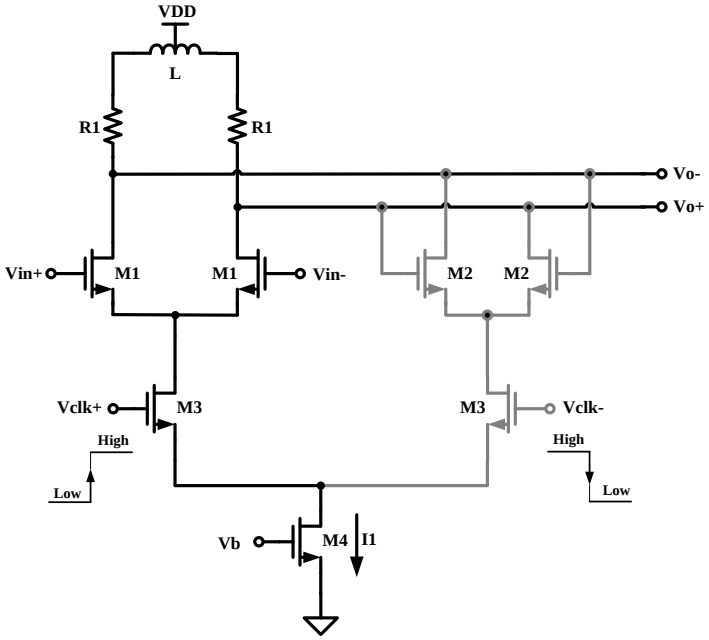


Fig. 4. 5. Latched comparator in the tracking phase (Transistors in gray are off)

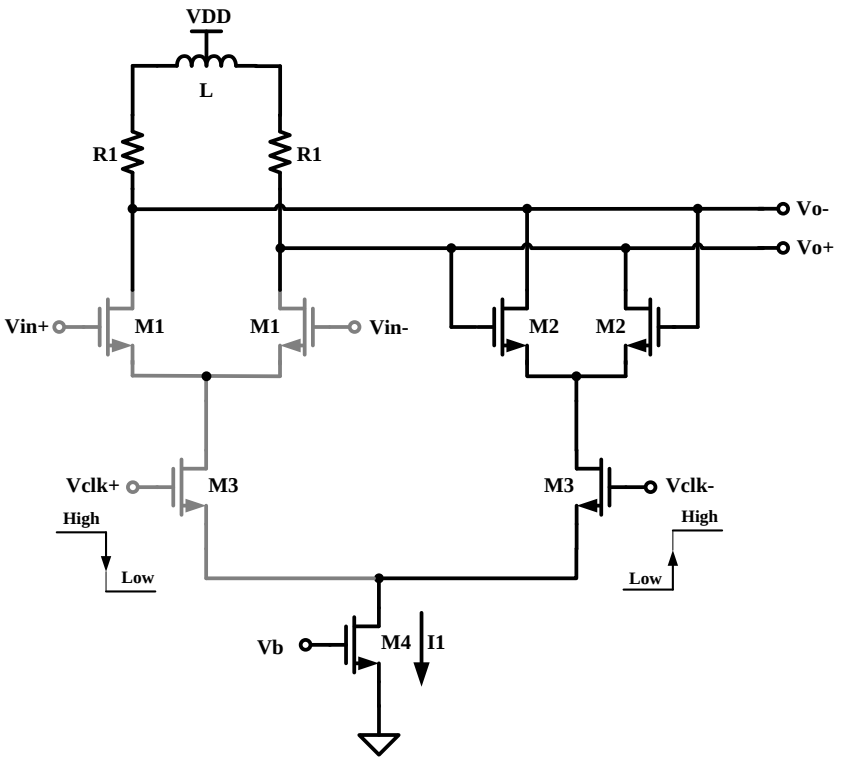


Fig. 4. 6. Latched comparator in the regenerative phase (Transistors in gray are off)

The speed of the latched comparator is determined by the tracking time constant (τ_{tr}) and the regenerative time constant (τ_{reg}), the less τ_{tr} and τ_{reg}, the higher speed of the comparator. Introducing inductor in series with the load resistors can reduce both the time constants so that it can improve the speed performance [40]. As we have already known, the shunt peaking inductor increases the bandwidth of the comparator during the tracking phase and reduces the τ_{tr}. In order to understand how the inductor reduces the regenerative time constant τ_{reg}, let's take a look at the loading of the comparator as shown in Fig. 4.7 (a). The output impedance is given by

$$Z_{out} = \frac{1}{\frac{1}{R + j\omega L} + j\omega C} \tag{4.2}$$

So,

$$Y_{out} = \frac{1}{R + j\omega L} + j\omega C = \frac{R}{R^2 + \omega^2 L^2} + j\omega\left(C - \frac{L}{R^2 + \omega^2 L^2}\right) \tag{4.3}$$

From Eq. (4.3), the equivalent loading of the comparator is shown in Fig. 4.7 (b). The equivalent resistance and capacitance are obtained,

$$R_{eq} = R + \frac{\omega^2 L^2}{R} \tag{4.4}$$

$$C_{eq} = C - \frac{L}{R^2 + \omega^2 L^2} \tag{4.5}$$

The Eq. (4.4) and (4.5) show that the R_{eq} is always greater than the R and the C_{eq} is always less than the C. Since the regenerative time constant τ_{reg} is given by [42]:

$$\tau_{reg} = \frac{C_{eq}}{g_m - 1/R_{eq}} \tag{4.6}$$

The latched comparator with the series inductor has smaller time constant τ_{reg} than the latched comparator without the inductor.

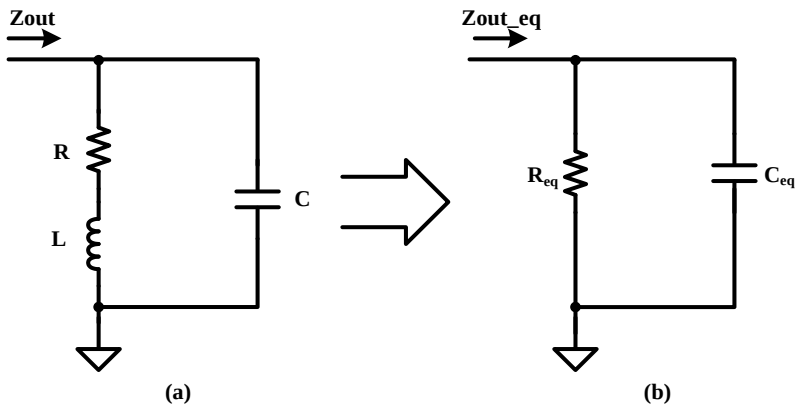


Fig. 4. 7. Loading of the latched comparator (a) Real loading (b) Equivalent loading

In MOS CML, the minimum swing ΔV_{MIN} is determined from the condition that the MOS differential pair is fully switched [43]

$$\Delta V_{MIN} = 2\left[V_{GS}\left(I_T\right) - V_{GS}\left(\frac{I_T}{2}\right)\right] \tag{4.7}$$

where I_T is the value of the tail current. The measured ΔV_{MIN} corresponding to the minimum delay bias is approximately 400 mV in the 0.13um CMOS technology [43]. Here ΔV was chosen to be about 450 mV. Typically transistors M1 and M2 are chosen the same dimension, which should also be biased at the peak f_t for high speed operation. Then f_t vs. $\frac{g_m}{I_D}$ and $\frac{I_D}{W}$ plots were used to determine the dimensions of the transistors [43]. The component values and parameters are listed in Table 4.3.

Table 4. 3. Transistor sizes and bias conditions for the latched comparator

Parameters	Value
M1 (W/L/NF)	2um/0.13um/14
M2 (W/L/NF)	2um/0.13um/14
M3 (W/L/NF)	2um/0.13um/10
M4 (W/L/NF)	10um/0.5um/40
R	90 ohms
L	0.84 nH
I1	5 mA
VDD	1.8 V

4.2.3 D flip flop

The DFF in this quantizer is composed of two cascade current mode logic latches as shown in Fig. 4.8. The DFF not only provides half period time delay, but also increases the voltage gain and reduces the metastability problem of the quantizer. The resistor R1 is relatively small such that the bandwidth of the latch during sampling phase is big enough. The differential output swing is about 800 mV. The method discussed in 4.2.2 was used to determine the dimensions of the transistors. The component values are shown in Table 4.4.

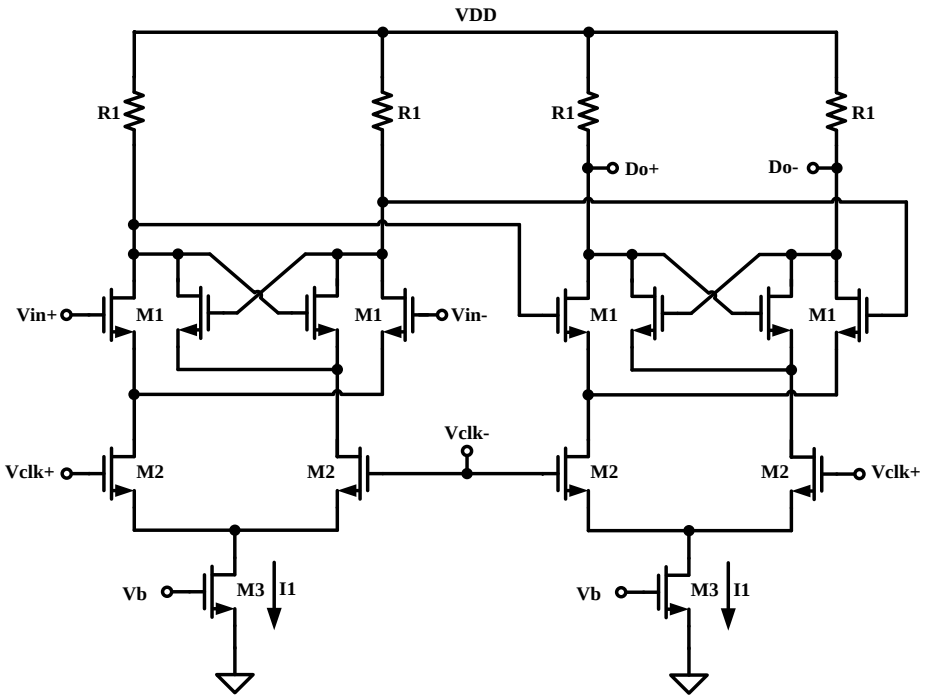


Fig. 4. 8. Schematic of DFF

Table 4. 4. Transistor sizes and bias conditions for the DFF

Parameters	Value
M1 (W/L/NF)	2um/0.13um/14
M2 (W/L/NF)	2um/0.13um/10
M3 (W/L/NF)	10um/0.5um/40
R1	90 Ohms
I1	5 mA

4.3 Layout of the 2-bit quantizer

The layout of the 2-bit quantizer for one branch circuit is shown in Fig. 4.9. There are two inductors for the pre-amplifier and latched comparator stages to improve the speed of the quantizer. The octagonal spiral inductor in the library of the TSMC 0.13um

CMOS technology was used in the layout directly. The penalty is that the inductors consume a large chip area. Decoupling capacitors are introduced for the power supply and reference voltages to reduce the noise and glitches. Fig. 4.10 shows the layout of the whole 2-bit quantizer.

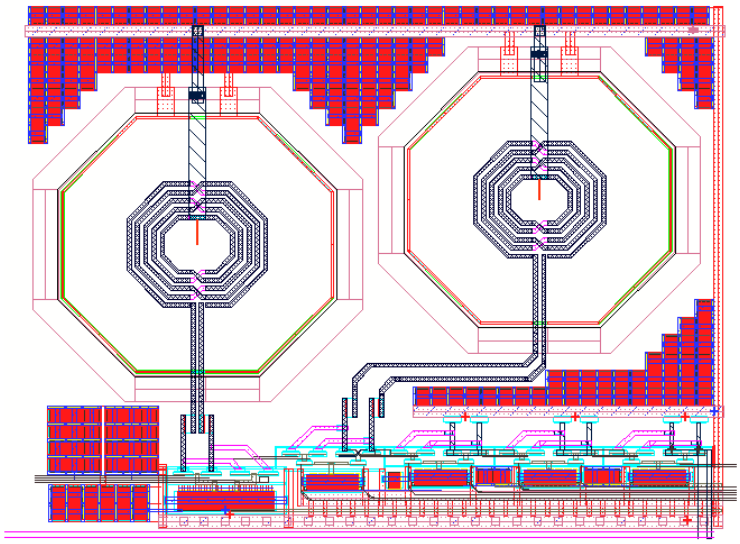


Fig. 4. 9. Layout of the 2-bit quantizer for one branch circuit

4.4 Simulation results

The testbench diagram used to characterize the 2-bit quantizer is shown in Fig. 4.11. The quantizer compares the input voltage with the reference voltages and digitizes the difference at certain clock frequency and generates the digital word.

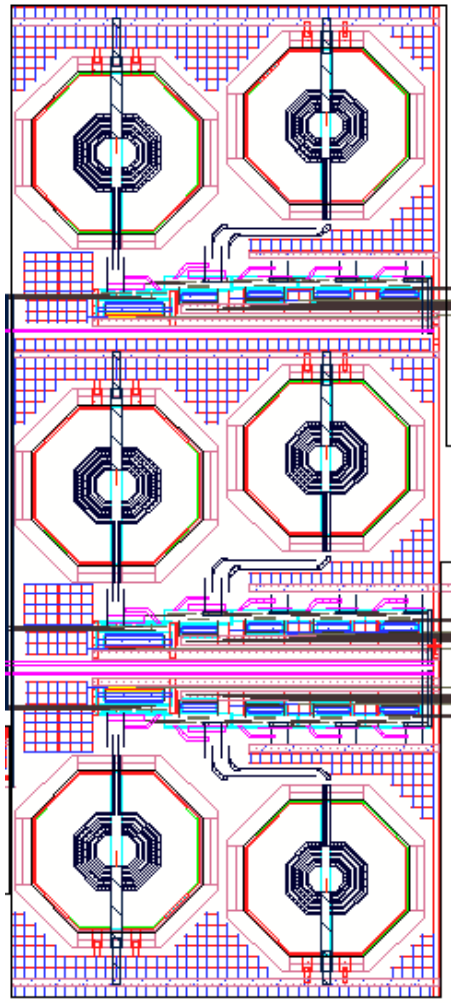


Fig. 4. 10. Layout of the 2-bit quantizer

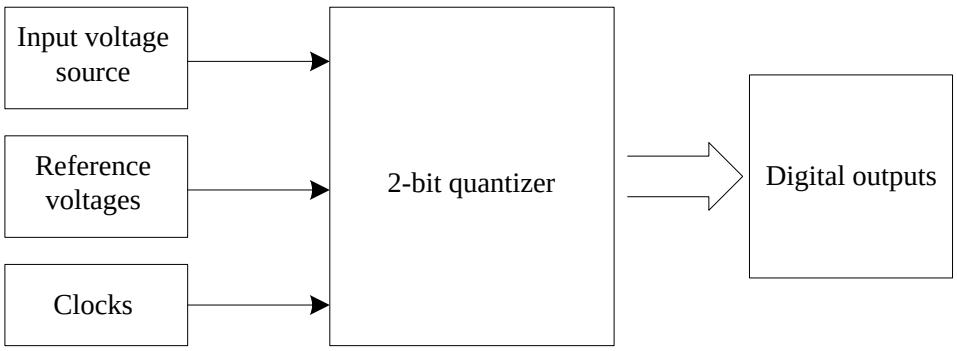


Fig. 4. 11. Testbench diagram of the 2-bit quantizer

4.4.1 Ramp input test

A linear ramp input voltage is used to measure the static performance of the quantizer. The differential ramp voltage is from -0.2 to 0.2V. The clock frequency is 8 GHz. The simulation results are shown in Fig. 4.12. The quantization levels of the 2-bit quantizer are: -90.12mV, 10.79mV, 110.7mV. The distances between each transition are: 100.91mV and 99.91mV. So the maximum DNL of the quantizer is:

$$DNL_{\max} = \frac{100.91}{100} - 1 = 0.0091\ LSB$$

The simulation results demonstrate that the 2-bit quantizer achieves excellent static performance and meets the requirement, which needs to be less than 0.5 LSB.

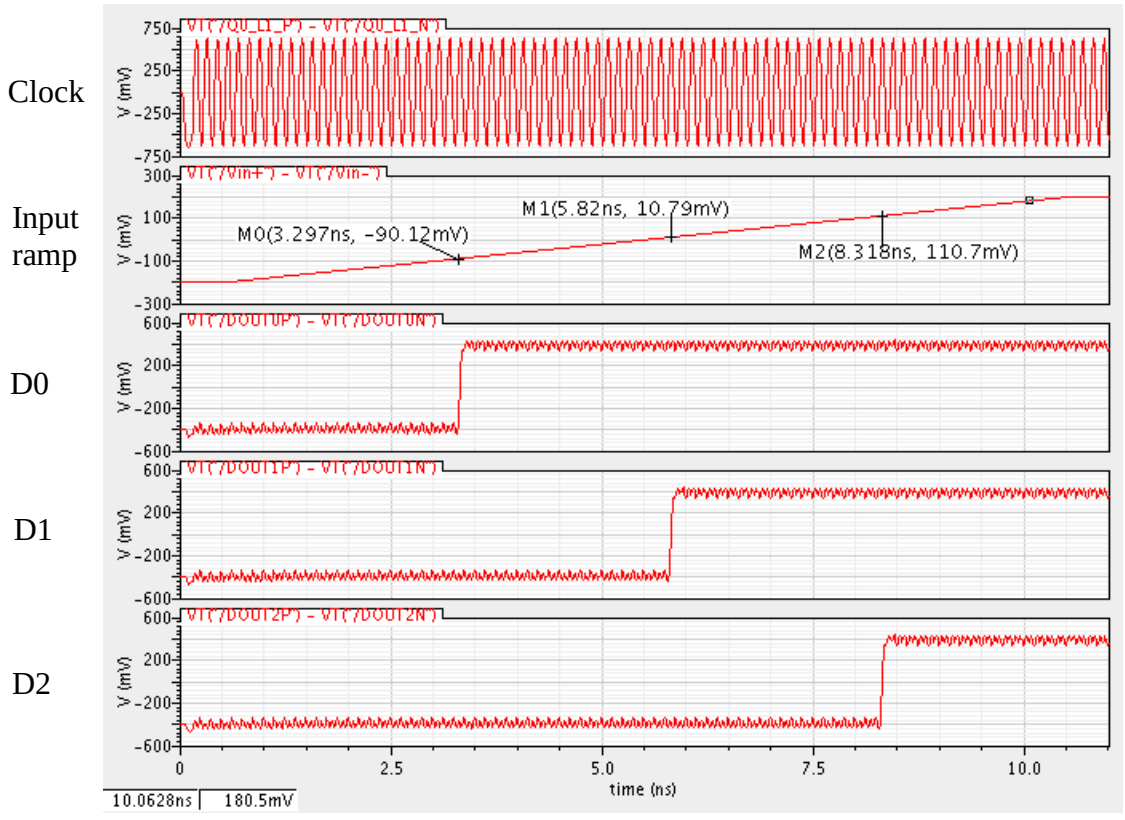


Fig. 4. 12. Ramp test – output bit transitions with differential input ramp from -0.2 to 0.2V (Quantization transition levels: -90.12mV, 10.79mV, 110.7mV)

4.4.2 Sinusoidal input test

For the CT BP ∑Δ ADC in this work, the input signal frequency f_{in} and the resonant frequency of the bandpass filters are one quarter of the sampling frequency f_S. So the sinusoidal signals with frequency $\frac{f_S}{4}$ are added at the input to test the dynamic performance of the quantizer. The simulation results at 8 GHz clock frequency are shown in Fig. 4.13.

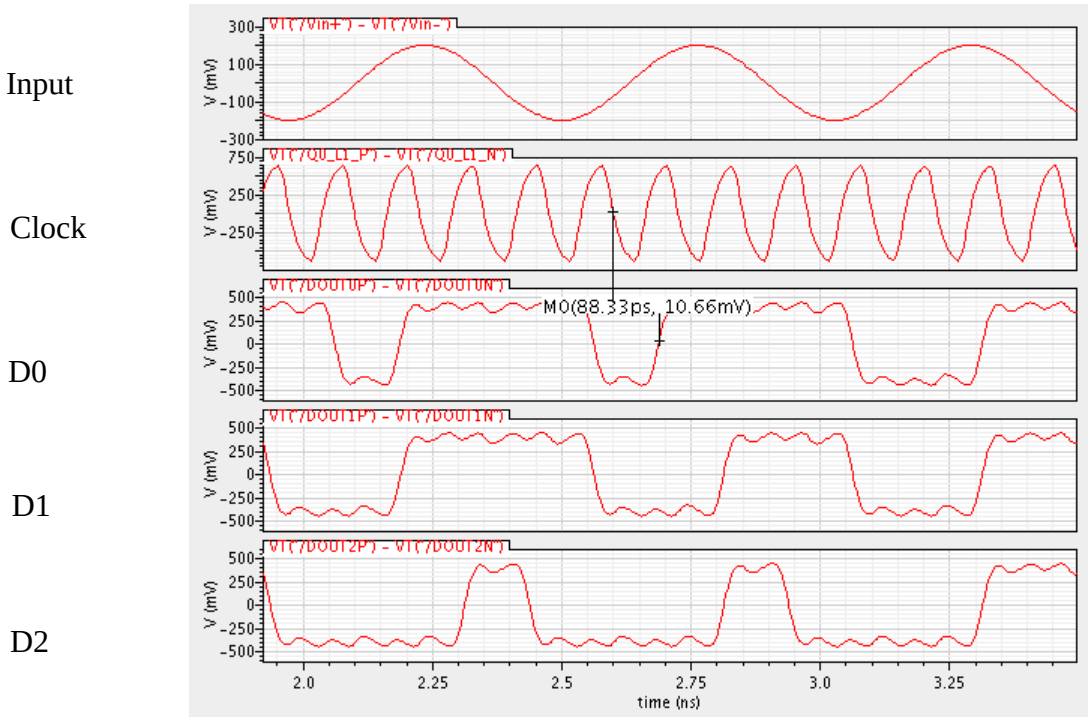


Fig. 4. 13. Simulation results @ f_S = 8 GHz

The sinusoidal differential input signal (400mVp-p) is compared with the reference voltages during the negative half period of the clock and generates thermometer code outputs D0, D1 and D2 as shown in Fig. 4.13. The digital output drives the 2-bit DACs and feedback into the sigma-delta modulator. Since the clock frequency is 8 GHz, which

is very high, the waveform of the clock signal is alike a sinusoidal wave instead of a square wave. The simulation result shows that the time delay of the quantizer is 88.33ps. As we mentioned before, the total time delay from the input of the quantizer to the output of the feedback DACs should be about one clock period, which is 125ps for 8 GHz clock frequency. There are about 36ps margin for the propagation delay and DACs' delay. Moreover, the clock phases can be tuned about $\pm 10\%$ so that the excess loop delay can be adjusted to obtain the best performance.

The simulation results at 12 GHz clock frequency are shown in Fig. 4.14. The last stage latch is reconfigured as a buffer to reduce the delay time. The simulation result shows the delay time is 55.73ps, which is about 28ps less than the 83.3ps clock period.

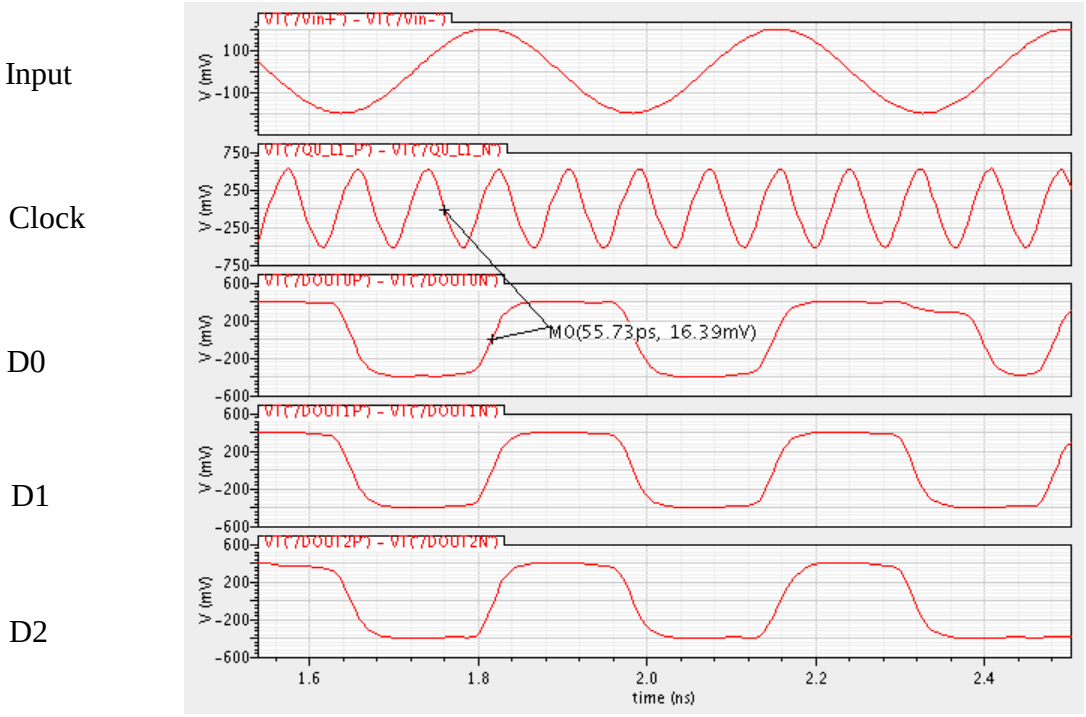


Fig. 4. 14. Simulation results @ f_S = 12 GHz

The delay tunability of the quantizer is shown in Table 4.5, which is 71%-92% at 8 GHz and 67%-90% at 12 GHz. The tunable delays are designed to be about 10 ps less than the clock period to compensate the DAC transition delay and transmission delay from the quantizer to the DACs. The power consumption of the quantizer is about 162 mW.

Table 4. 5. Delay tunability of the quantizer

Frequency (GHz)	Period (ps)	Tunable Delay (ps)	Tunability Compare to the Period
8	125	88.33-115.3	71%-92%
12	83.3	55.73-75.1	67%-90%

5. DESIGN OF 2-BIT DACS

5.1 Introduction

The main challenge of the CT BP ∑Δ ADC is to achieve high resolution in a wide bandwidth in order to support multiple standards in a single chip. For this work, the signal bandwidth is quite large, about 20 MHz and the sampling frequency is four times of the input signal frequency. The OSR, which is determined by the sampling frequency and the signal bandwidth, cannot be changed arbitrarily. So it is not feasible to achieve a higher SNR by increasing the OSR in this work. Increasing the order of the loop filter is another way to improve the SNR [44]. However, the order of the loop filter is seldom more than 5^{th} because it is very difficult to guarantee the stability of the modulator. The primary advantage of using a multi-bit instead of single-bit quantizer is that the SNR can be dramatically increased, typically by 6dB per additional bit. However, a multi-bit DAC, due to the element mismatch, is not inherently linear, which a single-bit DAC has. The nonlinearities of the feedback DACs introduce distortion or raise the noise floor of the modulator, which degrades the Signal-to-Noise and Distortion Ratio (SNDR) of the modulator. Therefore, several techniques are being used to eliminate errors caused by element mismatch in the DAC, such as Dynamic Element Matching (DEM), calibration and so on [45]-[52]. However, since the sampling frequency is more than 8 GHz, DEM is not feasible in this work. In this section, the most common topology for feedback DACs will be discussed firstly. Then, calibration methods for improving the linearity of feedback DACs will be described.

5.1.1 Feedback DACs topology

There are several requirements between feedback DACs in ∑Δ modulators and the typical DACs. The main difference is the accuracy requirement. For a typical DAC, the required accuracy is on the order of ± 0.5 LSB, while it should be no less than the accuracy of the modulators for feedback DACs since noise and harmonic components generated in the DAC are not shaped by the loop. Another difference is that feedback DACs require less output levels, usually no more than 4 bits. Although a great deal of circuit topologies can be used to implement feedback DACs, a typical architecture is using $2^N - 1$ parallel unit elements, which is shown in Fig. 5.1. In this architecture, the N-bit binary digital input is firstly converted into $M = 2^N - 1$ thermometer codes. Then, the thermometer codes are used to control M unit elements. The *K*th output level is generated by activating *K*-1 equal-valued elements (typically resistors, transistor current sources, or capacitors) and summing up their charges or currents. Although the thermometer-type DAC is not practical to provide more than 4 bits output levels, these output levels can be extremely accurate. The overall accuracy of the thermometer-type DAC is much greater than the accuracy of an individual unit element.

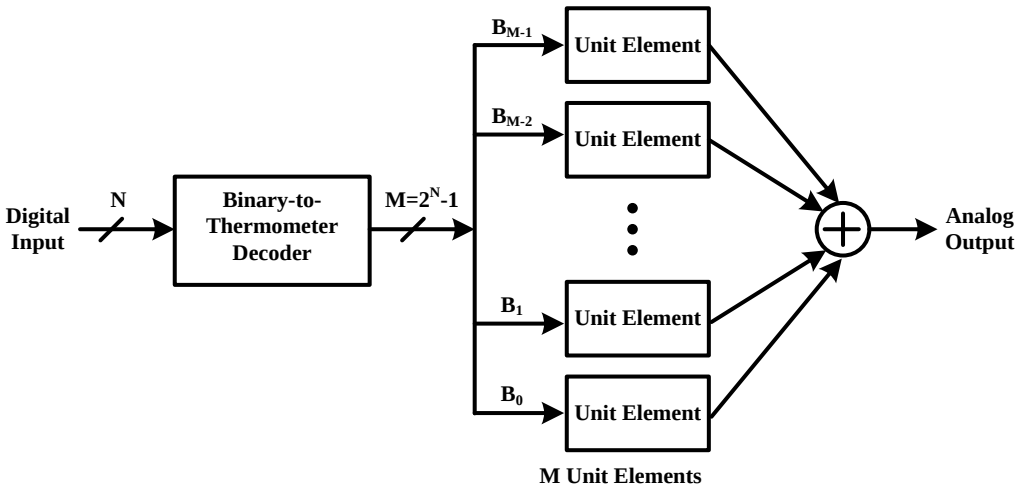


Fig. 5. 1. Block diagram of parallel unit element DAC

Assume without loss of generality that the unit element is current source and all of the current sources have an identical Gaussian probability distribution with a mean I and a standard deviation of ΔI. The standard deviation of the output current for a digital code K is given as

$$\Delta I_O = \sqrt{(\Delta I)^2 \times K} = (\Delta I)\sqrt{K} \tag{5.1}$$

The standard deviation of the output current can be described as a fraction of the full-scale current:

$$\frac{\Delta I_O}{I_O} = \frac{(\Delta I)\sqrt{K}}{I \times M} \tag{5.2}$$

where, $M = 2^N - 1$ and N is the number of bit for the feedback DAC. The largest error happens at the largest value of K, which is M. However, a small error in the overall scale factor is not critical in most data conversion applications. Instead, deviation of each output value from a best fitting straight line is commonly used.

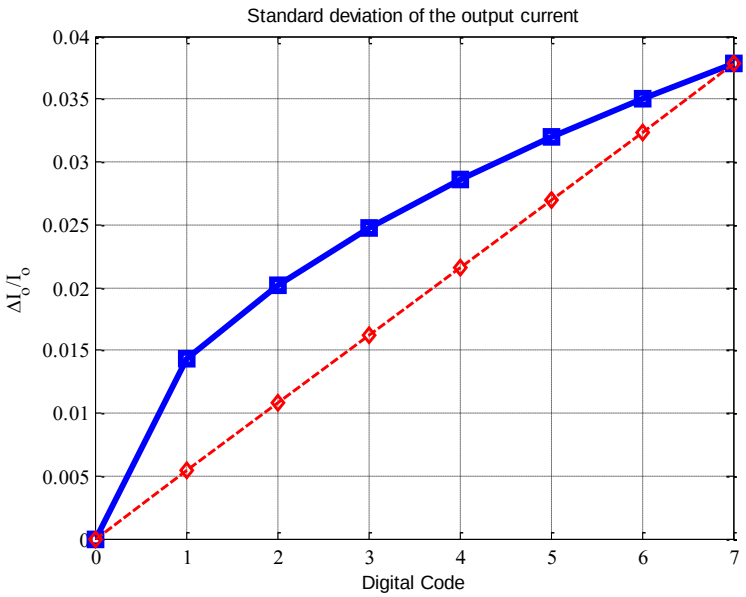


Fig. 5. 2. Typical deviation of the output current

As shown in Fig. 5.2, the solid line is the standard deviation of the output current for a 3-bit DAC. The dashed line, which is defined by the zero output and the full-scale output, is used as the best fitting straight line. The worst-case standard deviation of the normalized output comes at $K = \frac{M+1}{2}$ and it can be expressed as [53]:

$$\sigma\left[\frac{\Delta I_O(worst)}{I_O(M)}\right] = \frac{1}{2\sqrt{M+1}}\sigma\left[\frac{\Delta I_i}{I}\right] \tag{5.3}$$

Since M is bigger than 1, the worst case current standard deviation of the feedback DAC is improved, which is $\frac{1}{2\sqrt{M+1}}$ the standard deviation of the unit current.

5.1.2 Calibration

The nonlinearity of feedback DACs introduces distortion or increase the noise floor of the ∑Δ modulator so that the SNR is limited. Typically, digital CMOS technologies can provide the matching accuracy up to 10-bit, which means the highest resolution of the entire ∑Δ modulator can be no more than 10-bit. In order to achieve a higher resolution, current calibration has been presented. The conventional current calibration principle is described in Fig. 5.3 (a) [45]. It is composed of the reference current source I_{REF}, switches S_{OUT} and S_{CAL}, a unit DAC cell which is provided by transistors M1 and M2, and mirrored transistor M_B. I_{REF} and M_B are shared by all current sources. The conventional DAC current calibration circuit works in two modes: normal mode and calibration mode. In calibration mode, switch S_{OUT} connects to I_{REF} and S_{CAL} closes. The current I_{REF} flows through M1 and M2. Since the drain current of M1 is fixed, about 0.9~0.97I_{REF}, the rest of current is forced to flow through M2, with a certain V_{GS} on M2. In normal mode, the switch S_{CAL} is open and S_{OUT} is connected to I_{O+} or I_{O-} according to the digital input. As V_{GS} of M2 is preserved on C_{CAL}, the drain current of M2 remains unchanged, thus the total current through M1 and M2 remains equal to I_{REF}. An extra spare current source is added as shown in Fig. 5.3(b), which takes the position of the current source that is being calibrated, thus operation of the DAC is not interrupted. All the current sources, including the spare one, are calibrated one by one continuously and periodically by the same reference current source I_{REF} [45]. Although calibration method is widely used to improve the linearity of feedback DACs, it increases the circuit complexity and power consumption. Moreover, it is not necessary in this work since the required linearity is just 10 bits.

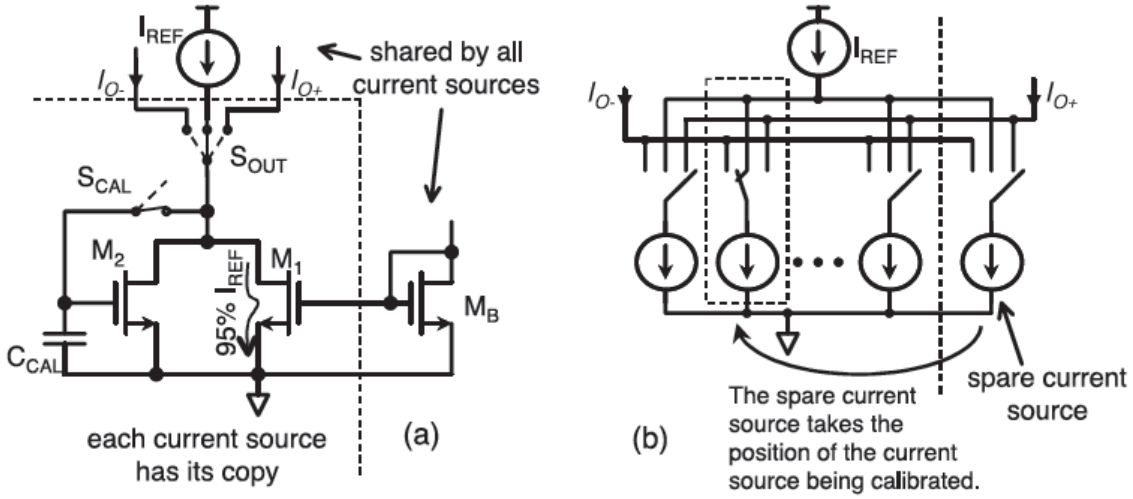


Fig. 5. 3. Conventional DAC current calibration (a) Calibration principle

(b) DAC overall structure [45]

5.1.3 Proposed DAC topology

In this project, the resolution of the proposed CT BP ∑Δ ADC is 10-bit and 2-bit quantizer and feedback DACs are chosen to achieve better stability and SNR. Linearity is one of the major concerns for implementing multi-bit feedback DACs, which should be better than 10-bit accuracy in this ADC. According to Eqn. (5.3), the accuracy of current sources in the parallel unit element DAC can be calculated:

$$\sigma\left[\frac{\Delta I_i}{I}\right] = 2\sqrt{3+1}\times\sigma\left[\frac{\Delta V_O(worst)}{V_O(M)}\right] = 4\times 0.1\% = 0.4\%$$

Since 0.4% accuracy can be easily achieved in modern digital CMOS technologies, the parallel unit element DAC topology without using DEM or calibration is feasible for this project.

Clock jitter in the feedback DACs will also affect the SNR of a CT BP ∑Δ ADC. The SNR for a CT BP ∑Δ ADC with only NRZ DAC is given by [33]

$$SNR_{NRZ} = 10\log_{10}\left(\frac{OSR \times V_{in}^2 \times \mathrm{sinc}^2\left(\frac{\omega_0 T_s}{2}\right)}{4\left(\frac{\sigma_j}{T_s}\right)^2}\right) \tag{5.4}$$

where OSR is the oversampling ratio, V_{in} is the amplitude of the input signal, ω_0 is the center frequency of the bandpass filter, T_s is the time period of sampling clock. In this work, the clock jitter should be better than 0.5ps to achieve 60dB SNR.

The proposed 2-bit DAC topology is shown in Fig. 5.4, which is composed of three unit current sources I1 and three differential pairs M1. The B0~B2 are three CML level differential input signals so that the differential pairs M1 work as CML switches. There are three benefits for this: (1) CML circuit can work at very high speed. (2) Since the swing of the input signal is much smaller than that of the digital signal, the clock feedthrough effect is less. (3) When the transistor is ON, it works in saturation region so that the output impedance is higher, which reduces the loading effect to the following stage.

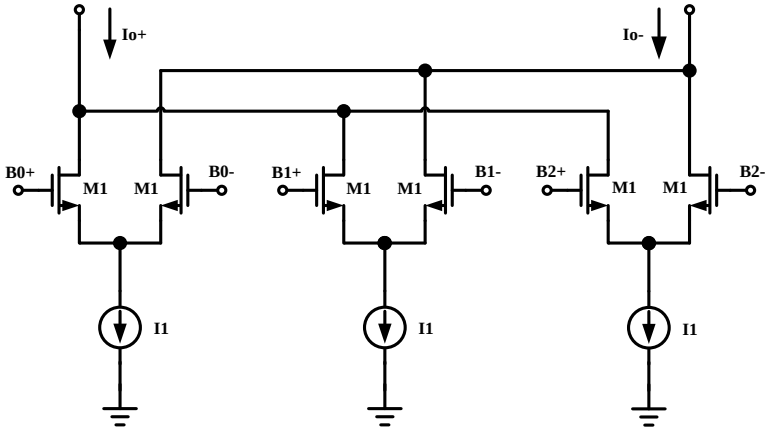


Fig. 5. 4. Proposed 2-bit DAC topology

5.2 Circuit implementation of DACs building blocks

5.2.1 Current steering DACs

The schematic of 2-bit NRZ current steering DAC is shown in Fig. 5.5. The transistors M2 provide current and the differential pairs M1 act like simple switches. The digital 2-bit NRZ bit stream from the quantizer outputs is converted into current by the differential pairs M1, and the current is directly injected into the LC resonator. The current steering DAC coefficient can be tuned by directly changing the value of current I1. The component and current values for the current steering DACs are listed in Table 5.1.

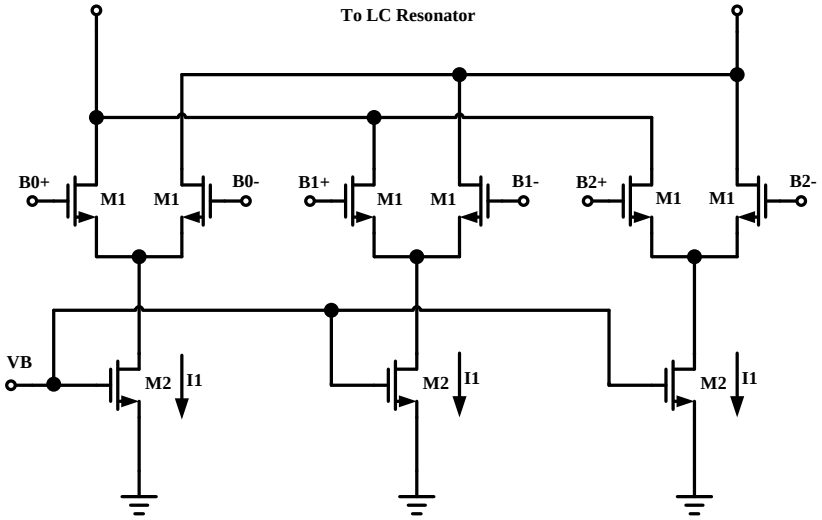


Fig. 5. 5. 2-bit NRZ current steering DAC

Table 5. 1. Component and current values for the current steering DACs

Parameters	CDAC connected to the first resonator	CDAC connected to the second resonator
M1 (W/L/NF)	1.2um/0.13um/3	1.2um/0.13um/5
M2 (W/L/NF)	4um/1.6um/12	4um/1.6um/40
I1	0.466 mA	0.83 mA

In order to meet the high speed requirement, the minimal length is chosen for the differential pairs. While a much larger length is used for transistors M2 to reduce current mismatch. Current mismatch is usually normalized to the average value as [41]:

$$\frac{\Delta I_D}{I_D} = \sqrt{\left(\frac{\Delta(\mathrm{W/L})}{\mathrm{W/L}}\right)^2 + 4\left(\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}\right)^2} \tag{5.6}$$

For the 1.2V NMOS in TSMC 0.13um CMOS technology,

$$\begin{cases} \dfrac{\Delta L}{L} = \dfrac{0.216\%}{\sqrt{W*L}} \\ \dfrac{\Delta W}{W} = \dfrac{0.216\%}{\sqrt{W*L}} \\ \Delta V_{TH} = \dfrac{2.536}{\sqrt{W*L}} \end{cases} \tag{5.7}$$

So the current mismatch can be obtained:

$$\left(\frac{\Delta I_D}{I_D}\right)_{CDAC1} = \sqrt{\left(\frac{0.216\%}{\sqrt{4*1.6*12}}\right)^2 + \left(\frac{0.216\%}{\sqrt{4*1.6*12}}\right)^2 + 4\left(\frac{2.536}{240\times\sqrt{4*1.6*12}}\right)^2} = 0.42\%$$

$$\left(\frac{\Delta I_D}{I_D}\right)_{CDAC2} = \sqrt{\left(\frac{0.216\%}{\sqrt{4*1.6*40}}\right)^2 + \left(\frac{0.216\%}{\sqrt{4*1.6*40}}\right)^2 + 4\left(\frac{2.536}{180\times\sqrt{4*1.6*40}}\right)^2} = 0.26\%$$

Although the current mismatch 0.42% is slightly larger than the 0.4% requirement, the matching will be improved using common centroid and interdigitize layout techniques.

5.2.2 Integrator DACs

The schematic of the integrator DAC is shown in Fig. 5.6. The digital NRZ bit stream from the quantizer outputs is converted into current by the differential pairs formed by transistors M1, and the current is integrated by capacitors C. The loss resistors R are added to realize soft clipping and improve the operating range. The output of the integrator is in voltage mode. A linearized Gm cell is added to convert the voltage into current and the current is injected into the LC resonator. The integrator DAC coefficient can be tuned by changing the value of current I1. The component and current values for the integrator DACs are listed in Table 5.2.

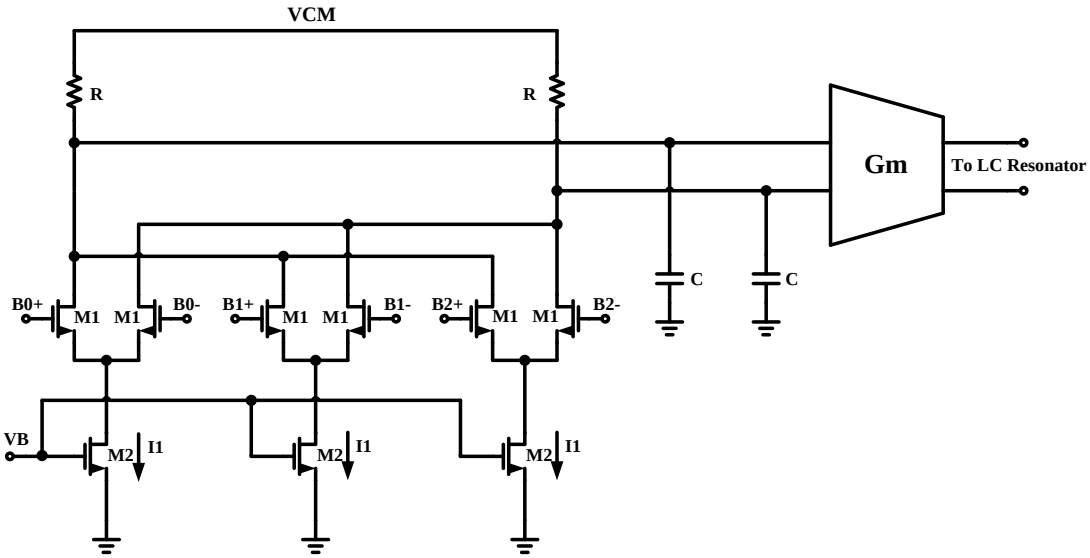


Fig. 5. 6. 2-bit integrator DAC

Table 5. 2. Component and current values for the integrator DACs

Parameters	IDAC connected to the first resonator	IDAC connected to the second resonator
M1 (W/L/NF)	1.2um/0.13um/4	1.2um/0.13um/6
M2 (W/L/NF)	4um/1.6um/20	4um/1.6um/48
I1	0.7 mA	0.966 mA
R	200 ~ 700 Ohms	200 ~ 700 Ohms
C	2 pF	2 pF
VCM	0.9 V	0.9 V

A 5-bit binary weighted resistor bank is implemented to cover the wide and fine tuning range of the resistor. The diagram of the resistor bank is shown in Fig. 5.7. The unit resistor R is 1.75 KOhms and the resistance in the range of 200~700 Ohms is shown in Table 5.3.

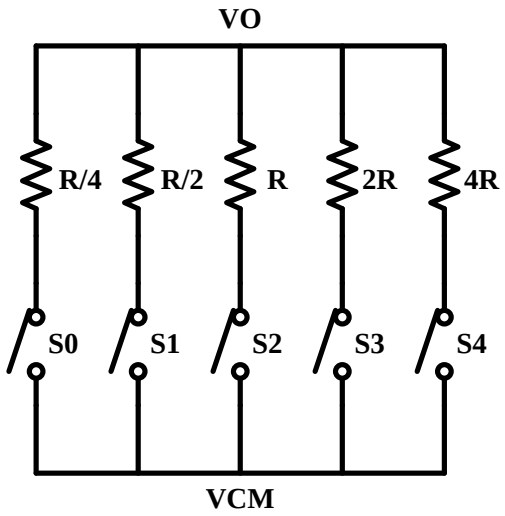


Fig. 5. 7. 5-bit binary-coded resistor bank

Table 5. 3. Resistance in the range of 200~700 Ohms

$S_0S_1S_2S_3S_4$	Resistance (Ohms)	$S_4S_3S_2S_1S_0$	Resistance (Ohms)
11111	225.8	10100	350
11110	233.3	10011	368
11101	241.4	10010	389
11100	250	10001	412
11011	259	10000	438
11010	269	01111	467
11001	280	01110	500
11000	292	01101	538
10111	304	01100	583
10110	318	01011	636
10101	333	01010	700

5.2.3 Buffer

Source follower is inserted between the quantizer and DACs to reduce the loading effect of DACs. It also provides level shift functionality. The schematic of the buffer is

shown in Fig. 5.8. The gate of transistor M1 is connected to the output of the quantizer and the source of M1 is connected to the input of the DAC. The bulk and source of M1 are tied together to eliminate the body effect. The component and current values are shown in Table 5.4.

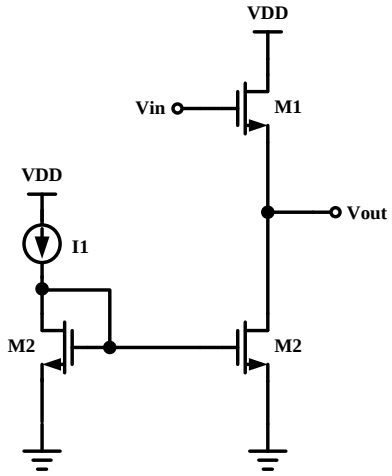


Fig. 5. 8. Buffer

Table 5. 4. Component and current values for the buffer

Parameters	Values
M1 (W/L/NF)	2um/0.13um/5
M2 (W/L/NF)	1um/0.2um/12
I1	1 mA
VDD	1.8 V

5.3 Layout of the 2-bit DACs

The layout of the 2-bit DACs is shown in Fig. 5.9. CDAC1 and IDAC1 are put as close as possible because their outputs are both connected to the first resonator. So do

CDAC2 and IDAC2 which are connected together to the second resonator. The digital input signals come from the right side, while the analog output is placed at the left side to reduce the coupling from digital signals. The linearity of feedback DACs can be improve-

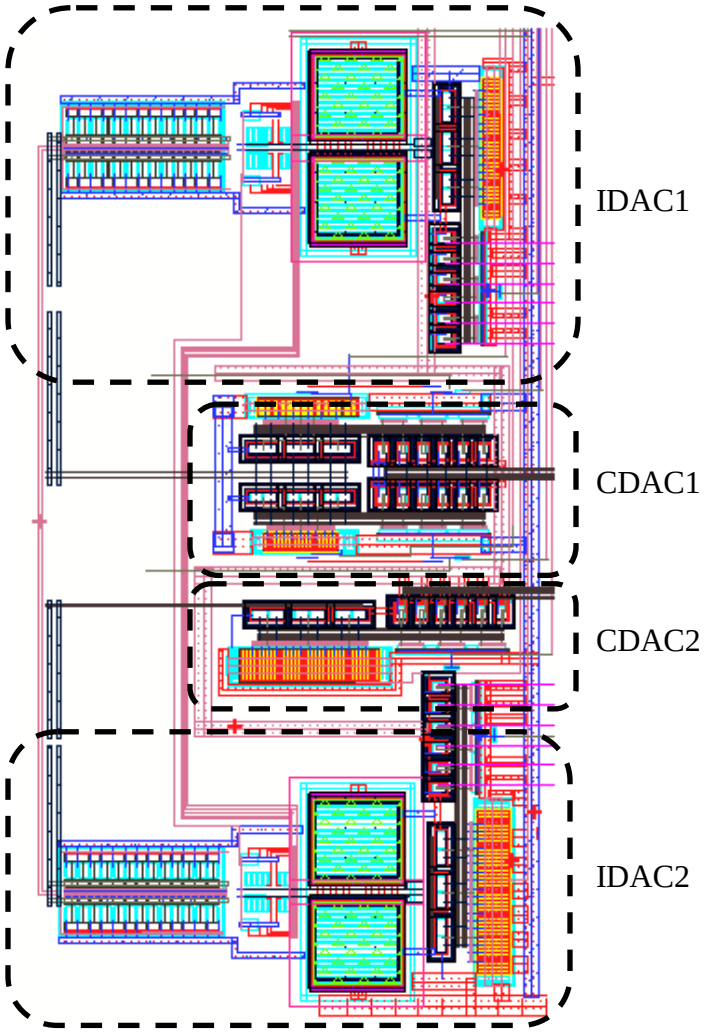


Fig. 5. 9. Layout of 2-bit DACs

d by reducing the mismatch among the current sources. Common-centroid and interdigitized layout techniques [41] are employed for the current sources to minimize the mismatch.

5.4 Simulation results for 2-bit DACs

Fig. 5.10 shows the postlayout simulation results of the CDAC when clock frequency is 8 GHz. The upper figure is a random differential input voltage and the lower one is the differential current output. The simulation result shows the delay of the DAC is about 1.2 ps and the current output of the CDAC follows the input correctly.

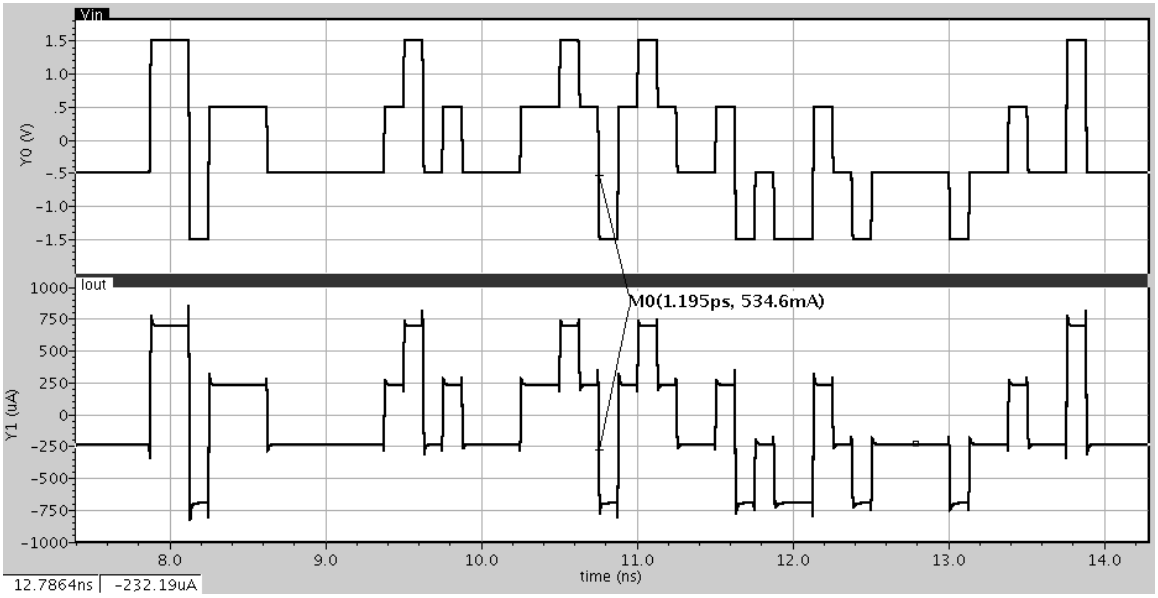


Fig. 5. 10. Current output of the CDAC

The noise shaping spectrums comparison between the ∑Δ modulator with ideal DACs and the modulator with real DACs is shown in Fig. 5.11. The spectrums are obtained by taking an FFT of the modulator output bit stream. The SNDR of the modulator with real DACs in 20MHz bandwidth is 48.9dB, while the SNDR of the modulator with ideal DACs is 59.7dB. The SNDR for the real case is dropped about 11dB compare to the ideal case. The main reason is that the modulator parameters, such as the center frequency, quality factor of the resonators and excess loop delay, have been

modified from the optimal values after replacing the ideal DACs with real DACs. This will definitely deteriorate the performance of the modulator. In order to recover the performance, the modulator parameters have to be tuned, which is extremely painful and time consuming for the postlayout simulation. However, this can be easily realized after the chip is fabricated since the tuning and data-capture can be finished in a short time.

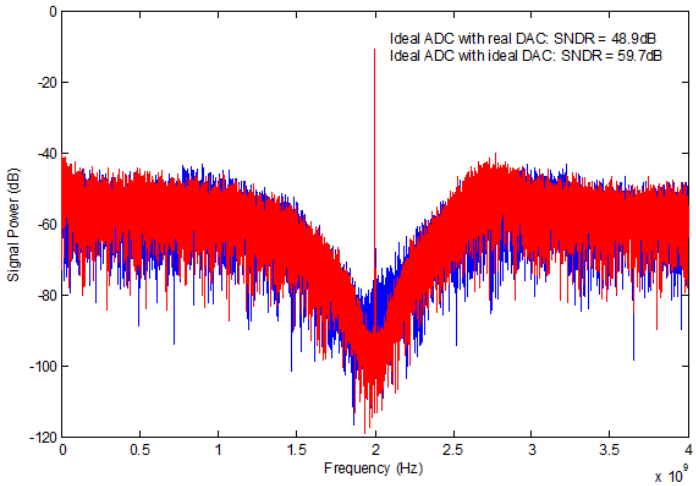


Fig. 5. 11. Noise shaping spectrums of the ∑Δ modulator

The performance summary of the DACs is shown in Table 5.5. The ADC with real DACs can achieve 48.9 dB SNDR at 20 MHz bandwidth. The power consumption of the DACs is 15 mW and the transition delay is about 2 ps.

Table 5. 5. Performance summary of the DACs

Item	SNDR (dB)	Power Consumption (mW)	Transition Delay (ps)
Value	48.9	15	~2

6. CONCLUSIONS AND FUTURE WORK

A 0.6-to-200 MSPS speed reconfigurable and 1.9-to-27mW power scalable 10-bit pipelined ADC has been designed and fabricated using UMC 90nm CMOS technology. The proposed technique configures the ADC architecture for optimal power at a specific speed, while maintaining constant biasing current for each stage. The principal advantage of this approach is that speed programming is effected on the architectural rather than the circuit level, obviating large bias-current variations inherent in conventional approaches. The measurement results show that the SNDR variation is within 3dB over the entire programmable range and the FOM is better than 0.49pJ/conversion.

A 2-to-4 GHz fourth-order CT BP ∑Δ modulator has been designed and fabricated in TSMC 0.13um CMOS technology. The 2-bit quantizer with tunable delay has been implemented to achieve better stability and higher SNR performance. However, the 2-bit quantizer requires 2-bit feedback DACs, which introduce nonlinear issue in the modulator. In order to minimize the nonlinear effect, parallel unit element DACs with common centroid and interdigitized current sources have been implemented. Postlayout simulation shows that the modulator achieves a SNDR of 48.9dB in 20 MHz bandwidth. The SNDR performance can be improved by tuning the modulator parameters after the chip is fabricated.

Since the clock frequency of the CT BP ∑Δ modulator is up to 16 GHz, it is difficult to implement this modulator in 0.13um CMOS technology, especially for the quantizer. Although CML circuits and inductors are introduced to improve the tracking and regeneration time, they consume a large area and power. Moreover, more time delay is introduced since long metal lines are needed to connect the output of the quantizer and

the input of feedback DACs, which will also degrade the ADC performance. In the future, more advanced technologies, for example 90nm or even 45nm CMOS technology, may be used to realize the modulator so that the circuits can be optimized and the overall performance can be improved.

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