DESIGN OF A 20MHZ TRANSIMPEDANCE AMPLIFIER WITH EMBEDDED LOW-PASS FILTER FOR A DIRECT CONVERSION WIRELESS RECEIVER

A Thesis

by

CHARLES PROF SEKYIAMAH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Aydin Karsilayan
Committee Members,	Jose Silva-Martinez
	Henry Pfister
	Rainer Fink
Head of Department,	Costas Georghiades

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ABSTRACT

Design of a 20MHz Transimpedance Amplifier with Embedded Low-pass Filter for a Direct Conversion Wireless Receiver.

(August 2011)

Charles Prof Sekyiamah, B.Sc., Kwame Nkrumah University of Science and Technology

Chair of Advisory Committee: Dr. Aydin Karsilayan

Accelerated growth in wireless communications in recent years has led to the emergence of portable devices that employ several wireless communication standards to provide multiple functionality such as cellular communication, wireless data communication and connectivity, entertainment and navigation, within the same device.

Industry drive is towards reduction of the number of radio frequency (RF) front-end receivers required to cater to the various standards/bands within a single device to reduce cost, size and power consumption. The current trend is to use broadband/multi-standard or reconfigurable RF front-ends to cater to two or three standards at a time for cost-effective RF front-end solutions. The direct conversion receiver architecture has become attractive as it offers a full on-chip front-end solution without the need for expensive external components. Passive current-mode mixers are used in these receivers to eliminate mixer flicker noise. The in-band current signals are typically in the micro-amp range after mixer downconversion.

Transimpedance amplifiers are used to convert the downconverted current signals to voltage, and they provide amplification in the process. Because of the co-existence of multiple-radios within each device, large blocker currents downconvert close to the channel bandwidth after the mixer. Conventionally, single-pole transimpedance amplifier (TIA) filters are used to provide out-of-band (OOB) signal filtering. This requires high resolution analog-to-digital converters (ADCs) later in the receiver chain for signal processing. Providing higher order filtering before the ADC relaxes its specifications and this reduces the ADC and ADC calibration cost and complexity.

Typically, an extra filtering stage is provided in the form of a cascaded filtering block after the single-pole TIA.

In this work, higher order filtering is embedded within the TIA in the form of active feedback. In addition to relaxing the ADC specifications, this proposed TIA provides improved large signal linearity such as P1dB compression point. Furthermore, since the extra-circuitry is not in the signal path, in-band flicker noise and linearity are not degraded.

The proposed TIA filter has been designed in IBM 90nm technology with a supply voltage of 1.2V. It can tolerate close-in blocker magnitudes of 4.5mA at 60MHz and higher before in-band 1dB compression is reached.

DEDICATION

To my wonderful mother, Mrs. Cynthia Asabea Osei-Kofi

To the memories of my late grandfather and great-grandmother

ACKNOWLEDGEMENTS

To God be the glory for a successful journey through my master's program; in my darkest hours, his light shone brightly through (Psalm 23).

I would like to express many thanks to my advisor, Dr. Aydin Karsilayan, for guiding me through my master's program. His valuable input into making this thesis possible cannot go without mention.

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Also, my deep thanks go to my mother, Cynthia, my brothers, Luther and Kojo, and my girlfriend, Lorraine. Their thoughts and prayers have been with me throughout the duration of my master's.

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1. INTRODUCTION

RF Front-end receivers find widespread application in this age of tremendous growth in wireless communication: from smartphone platforms, notebook computers, PDAs to handheld portable games such as the Playstation Portable (PSP). Several wireless communication standards have emerged as a result, adding to the traditional standards that already existed. Now we have GSM900, DCS1800, PCS1900 and WCDMA standards for cellular communication; WLAN a/b/g/n + WiMax , UWB Bluetooth standards for wireless data connectivity and communication; GPS for navigation; and FM/XM radio standards for entertainment [1], [2].

Usually in the aforementioned platforms- smartphones, notebook computers, PDAs - multiple wireless communication standards/radios coexist, resulting in the coined term multi-radio (multi-standard) platforms, e.g., today's smartphone will require GSM for cellular communications, Wi-fi/WLAN for internet connectivity, Bluetooth for short range connectivity and data transfer between itself and another phone, and GPS for navigation. The challenge is to find a way to integrate all these radios in these multi-radio platforms for cost-effective solutions; a reduction in the number of front-end receivers per device is the way to go.

There is the widespread notion that a single reconfigurable front-end architecture could be the ultimate cost-effective solution to cater to all standards in these multi-radio platforms. However, the argument in [3] is that the huge compromises which will have to be made in terms of performance and power dissipation makes this an unacceptable solution. The authors in [3] further contend that, multiple radios/standards will need to operate simultaneously for some period of time thus nullifying this solution as plausible, e.g., in a smartphone, a user can be surfing the internet (making use of WLAN radio)

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while talking on the phone (making use of GSM).

What is practical and is the current trend now, is to use broadband/multi-standard or reconfigurable front-ends that cater to two or three standards/bands at a time, thus reducing the number of front-end receivers in a practical manner, e.g., a dual-standard RF front-end receiver is built for W-LAN 802.11b/g (2.4–2.48 GHz) and W-CDMA-FDD (2.11-2.17 GHz) wireless standards in [2], a multi-standard direct-conversion RF front-end receiver is designed to cater to the WiMax and WiFi standards in the 4.9-6GHz range in [4], and a dual-band CMOS transceiver is designed for use in both IEEE 802.16e (mobile WiMAX) standard and WLAN standards in [5]. These multi-standard receivers suffer from out-of-band (OOB) interferer problems. Simply, when one standard is being utilized, signals in an adjacent standard/band, become OOB interferers or what is known as blockers, e.g., Bluetooth signals become interferer signals (blocker signals) when employing the GSM standard for communication between one cellphone user and another. Blockers are simply interferers that are large enough to de-sensitize the receiver chain. In addition, these multi-radio platforms suffer from other interference mechanisms such as OOB transmitter noise and limited switch isolation [3]. Some of these interferers down-convert as large blocking signals near the desired channel through the mixer.

The homodyne receiver, otherwise known as the zero-IF architecture, is the RF front-end architecture of choice in these multi-standard front-end receivers because of its many advantages over the heterodyne architecture in terms of cost and complexity. A heterodyne RF front-end receiver conversion flow is shown in Fig. 1.1 [6].

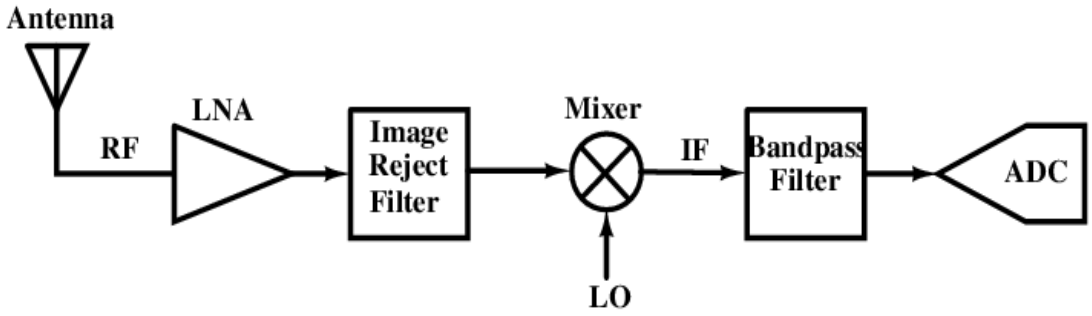


Figure 1.1 Heterodyne RF Front-End Receiver.

Heterodyne receivers convert the RF signal to an intermediate frequency (IF). This architecture gives rise to what is known as the image problem [6] and the half-IF problem [6], thus the inclusion of an image reject (IR) filter in the front-end path to stem this issue. The IR filter is implemented as an external discrete passive component and this increases size and cost of the front-end receiver. Also, since the RF signal is converted to IF, a baseband bandpass filter is required after the mixer. In practice this filter is implemented using high Q off-chip SAW filters due to its stringent OOB attenuation requirements [6].

The homodyne receiver circumvents the aforementioned problems encountered in the heterodyne architecture. Firstly, the RF signal is converted directly to DC by the mixer and this solves the image problem [6]. Thus, the off-chip IR filter is not needed. Secondly, since the RF signal is directly converted to DC instead of IF by the mixer, an on-chip active low-pass filter can be used in the baseband path instead of the high Q off-chip SAW filter used for baseband filtering in the heterodyne architecture. This allows for a full monolithic (on-chip) RF front-end solution without the need for expensive discrete external devices and ultimately culminates in cost savings, thus making the homodyne receiver more amenable to multi-standard front-end receiver design.

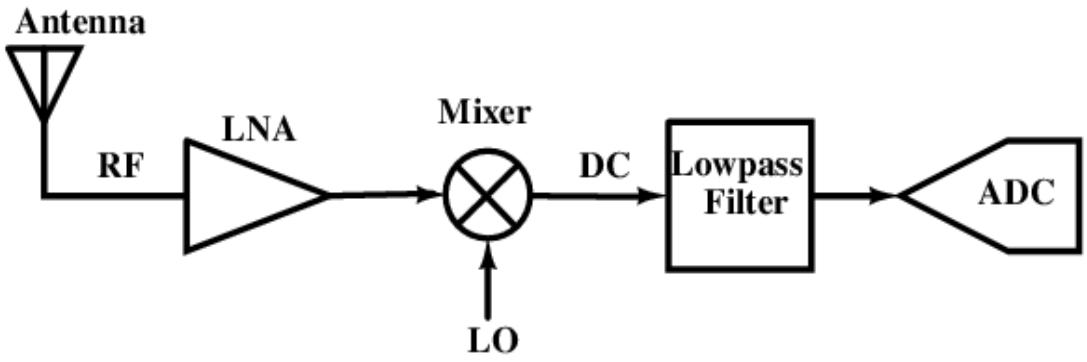


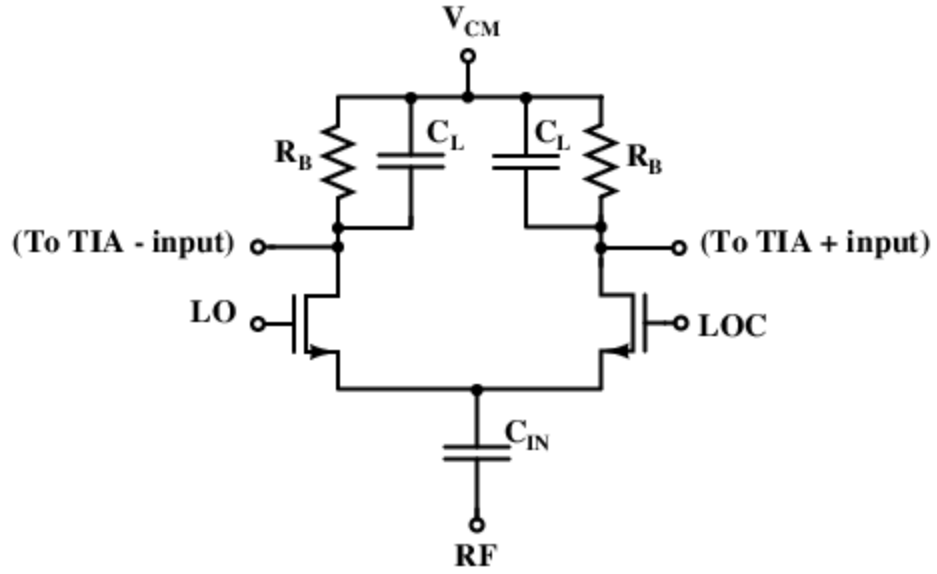
Figure 1.2 Homodyne RF Front-End Receiver.

The disadvantage with the homodyne receiver topology shown in Fig. 1.2 is that it is hugely impacted by device flicker noise owing to the conversion of the RF input signal directly to DC after the mixer. Since the mixer is the first block in baseband, its flicker noise contribution is the most important. If flicker noise in the mixer can be reduced or eliminated altogether, the sensitivity of the receiver can be improved significantly.

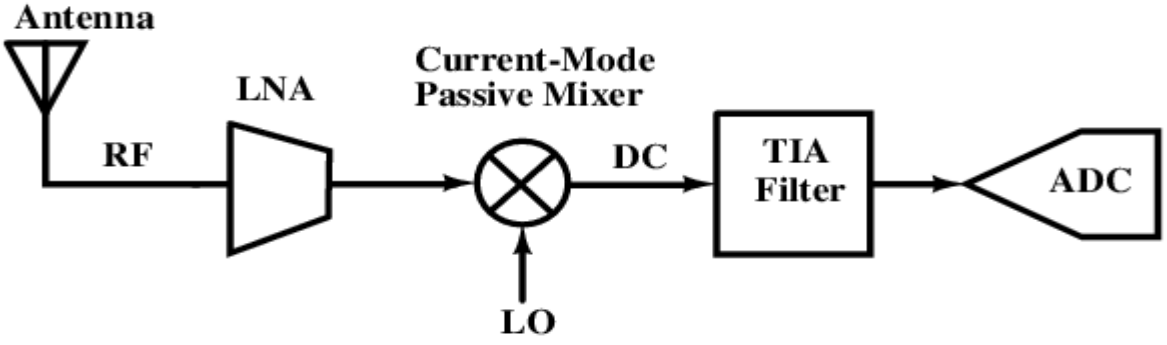
Flicker noise of a MOS transistor is proportional to its DC bias current as [7]:

$$V_n{}^2{}_{1/f} = \frac{K_f I_{ds}^{af}}{C_{ox} L^2} \frac{1}{f^{ef}} \tag{1.1}$$

where C_{ox} is the unit oxide capacitance, K_f is a device specific constant, L is the length of the device, I_{ds} is the DC bias current, af and ef are current and frequency indices respectively.



(a)



(b)

Figure 1.3 (a) Simplified Schematic of a Single-Balanced Passive Mixer. (b) Direct-Conversion Wireless Receiver with Current-Mode Passive Mixer.

From (1.1), by adopting a passive mixer, flicker noise can be removed during frequency conversion because there is no DC biasing current. A mixer configuration that achieves this is the current-mode passive switching mixer [7] shown in Fig. 1.3(a). It eliminates the DC biasing current in the conventional Gilbert cell active mixer [8]. Using the

current-mode mixer, this leads to a different configuration for the homodyne receiver architecture, and this is shown in Fig. 1.3(b). The LNA becomes a transconductance, converting RF voltage input from the antenna into current, which is fed to the passive current-mode mixer and after down-conversion, a transimpedance amplifier (TIA) is used to convert this base band current to voltage which is eventually fed to the ADC or other succeeding blocks.

Usually the in-band signal current (wanted signal) from the mixer can be anywhere from a few micro-amps to hundreds of micro-amps. It is the job of the TIA to amplify this small in-band current signal to a large enough output voltage, which can be accurately detected and processed by the ADC or any other block following the TIA. The TIA must also be capable of rejecting the large OOB blockers that exist at close-in frequencies. These blockers can be as large as 20dB greater in magnitude than the in-band signal current from the mixer.

While the TIA provides amplification for small in-band signals and attenuation for OOB blockers, its input voltage swing must be very small, and its input impedance must ideally approach zero. This is because the transistors in the current-mode mixer shown in Fig. 3(a) are operated in triode region. As long as the drain-source voltage (V_{DS}) of the mixer transistors is small, the channel resistance is very linear. However, as V_{DS} increases, the transistors approach the saturation region and the channel resistance becomes very non-linear. The drains of the MOS switching devices in the current-mode mixer are connected directly to the input of the TIA. Thus it is necessary to keep the voltage swing at the TIA input at a minimum to preserve the linearity of the mixer, and this means the TIA's input impedance must be kept at a minimum.

Traditionally, TIAs in the receiver chain have been implemented as single-pole filters since it is assumed that large OOB blockers will be handled by the ADC, e.g., in [4] a single-pole RC filter characteristic is used for the TIA because the blockers are accommodated by an oversampling, high dynamic range ADC later in the receiver chain.

An example of a conventional single-pole response for a TIA having an in-band gain of 60dB and a 20MHz bandwidth is shown in Fig. 1.4.

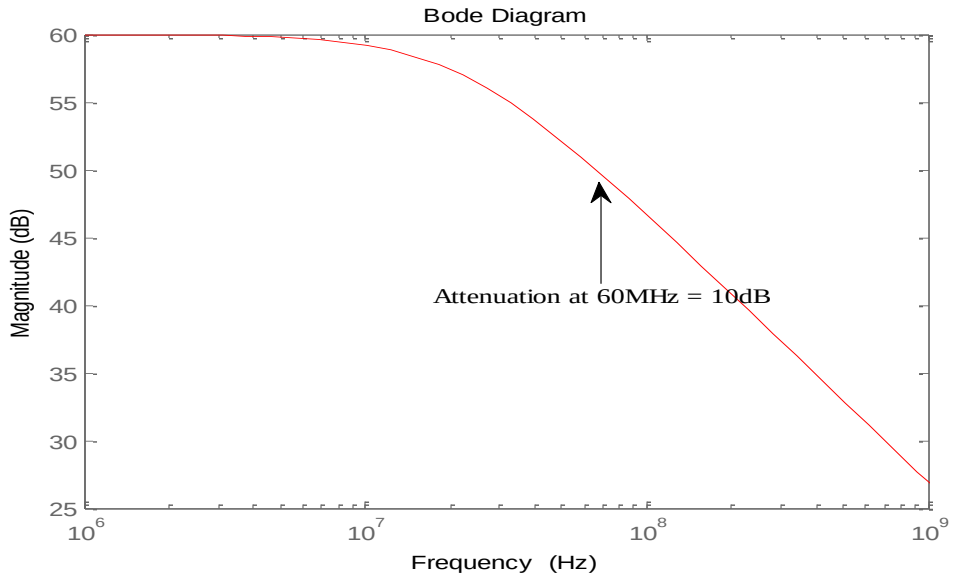


Figure 1.4 Single-Pole TIA with 60dBΩ In-Band Gain and a Bandwidth of 20MHz.

The focus of this work is to provide higher order filtering before the ADC, and specifically to embed this filtering within the TIA. Higher order filtering before the ADC has the following advantages:

a) It reduces the resolution of the ADC required in the frontend receiver, resulting in a lower number of bits for the ADC, reduced cost and complexity of the ADC.
b) It reduces the cost and complexity of the ADC calibration circuitry
c) It can potentially reduce the RF front-end receiver cost

In this work a 3rd order feedback TIA filter is proposed for multi-standard/reconfigurable/ broadband direct conversion RF receiver front-ends with a 60dBΩ in-band gain and a bandwidth of 20MHz. It offers 17.5dB more OOB attenuation

over the conventional single-pole TIA for close-in blockers at 60MHz and beyond. This feedback topology at the same time offers improved large signal linearity performance over the conventional single-pole TIA. Because the additional feedback circuitry is not in the signal path, the in-band performance of the single-pole TIA is not degraded; input impedance, flicker noise and in-band linearity are not sacrificed. The advantages of using a feedback topology for the proposed TIA filter are further explained in Section 2.

2. THE BASIC TRANSIMPEDANCE AMPLIFIER FILTER

The basic single-ended transimpedance amplifier is shown in Fig. 2.1. The input current I_{in} is converted to voltage at its output, V_{out} through the feedback impedance Z_f. This conversion is linear due to the fact that Z_f is implemented as a passive impedance.

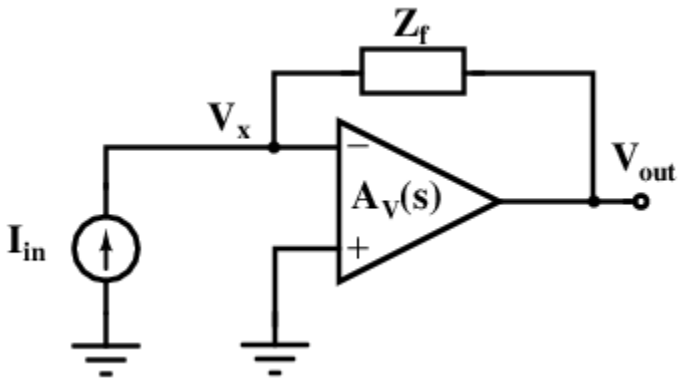


Figure 2.1 The Basic Transimpedance Amplifier.

2.1 Transimpedance Amplifier Parameters

The basic parameters that characterize the transimpedance amplifier shown in Fig. 2.1 are the transimpedance gain and the input impedance. A brief discussion of these parameters is given as follows.

2.1.1 Transimpedance Gain

This parameter characterizes the output voltage to input current gain and has the unit of ohms (Ω). For the circuit of Fig. 2.1 and with an op-amp open-loop gain of A_v *(s)*, writing the nodal equation at the op-amp inverting input node gives:

$$I_{in} = \frac{V_x - V_{out}}{Z_f} \tag{2.1}$$

where :

$$V_x = -\frac{V_{out}}{A_v(s)} \tag{2.2}$$

Substituting (2.2) into (2.1) gives :

$$I_{in} = -\frac{{}^{V_{out}}/_{A_v(s)} + V_{out}}{Z_f} \tag{2.3}$$

After algebraic manipulation, the transimpedance gain is obtained as :

$$\frac{V_{out}(s)}{I_{in}(s)} = -Z_f \left[\frac{A_v(s)}{1 + A_v(s)}\right] \tag{2.4}$$

For $|A_v(j\omega)| \gg 1$, the transimpedance gain reduces to :

$$\frac{V_{out}(s)}{I_{in}(s)} \approx -Z_f \tag{2.5}$$

which shows that the transimpedance gain is simply given by the value of the feedback impedance Z_f for sufficiently large values of op-amp open-loop gain $A_V(s)$.

2.1.2 Input Impedance

The input impedance of the TIA is critical for preserving mixer linearity, as discussed in Section 1. Substituting $V_{out} = -A_v(s)\, V_x$ into (2.1), we obtain:

$$I_{in} = \frac{V_x(1 + A_v(s))}{Z_f} \tag{2.6}$$

The input impedance is obtained as :

$$Z_{i,TIA}(s) = \frac{V_x}{I_{in}} = \frac{Z_f}{\left(1 + A_v(s)\right)} \tag{2.7}$$

Ideally, the Opamp gain A_v (s) $\rightarrow\infty$ and thus $Z_{i,TIA} \rightarrow 0$ implying $V_x \rightarrow 0$ from (2.7), which is what is desired. It can be recalled that a small TIA input impedance is desirable to keep the voltage swing V_x, which appears across the non-linear channel resistance of the mixer switching transistors at a minimum to preserve the mixer linearity. In practice, op-amps are not ideal and have finite open-loop gain, A_v (s) with a number of poles. Representing the op-amp in Fig. 2.1 as a single-pole op-amp for simplicity, its voltage gain can be expressed as:

$$A_v(s) = \frac{A_{vo}}{1 + s/\omega_p} \tag{2.8}$$

where A_{vo} is the DC gain and ω_p is the -3dB frequency of the op-amp. When (2.8) is substituted into the input impedance expression obtained in (2.7) the following is obtained :

$$Z_{i,TIA}(s) = \frac{Z_f\, s + Z_f\, \omega_p}{s + \omega_p(1 + A_v(s))} \tag{2.9}$$

2.2 The Conventional Single-Pole Transimpedance Filter

TIAs are employed as both an amplifier for in-band signals and a filter for OOB interferers in RF-front-end direct-conversion receiver chains as shown in Fig. 2.2.

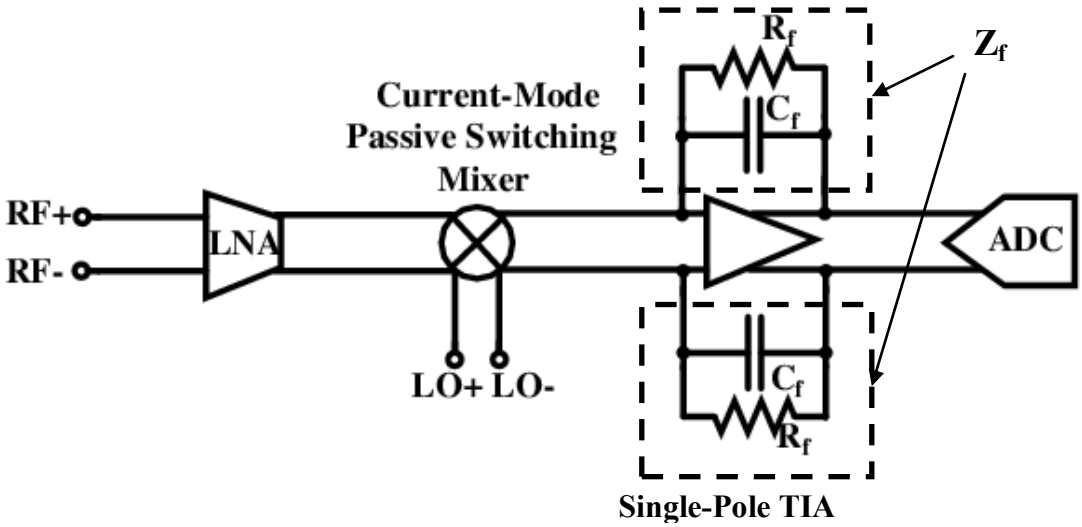


Figure 2.2 Fully-Differential Direct-Conversion Wireless Receiver Block Diagram.

In Fig. 2.2 the feedback impedance Z_f, is implemented as a parallel combination of a capacitor C_f and resistor R_f thus forming a single-pole filter with a cut-off frequency (-3dB bandwidth) given by :

$$\omega_{tia} = {}^{1}/_{R_f C_f} \tag{2.10}$$

This conventional TIA topology is employed in [3] where it provides current-to-voltage conversion in a multi-standard receiver chain. As stated in the previous section, interference mechanisms inherent in multi-standard/broadband receivers produce large close-in OOB blockers. In [4] this first-order TIA filter is used because the blockers produced are accommodated by an oversampled, high dynamic range ADC later in the receiver chain.

2.2.1 Input Impedance of the Conventional Single-Pole TIA Filter

As discussed before, a low TIA input impedance is desirable for good mixer linearity. In conventional TIA filters, Z_f is made up of a resistor in parallel with a capacitor. Substituting (2.10) into the input impedance expression from (2.9) we obtain:

$$Z_{i,TIA}(s) = \frac{\left(\omega_{tia} R_f\right)s + \omega_p \omega_{tia} R_f}{s^2 + \left(\omega_{tia} + \omega_p(1 + A_{vo})\right)s + \omega_{tia}\omega_p(1 + A_{vo})} \tag{2.11}$$

$Z_{i,TIA}(s)$ has two poles, a dominant pole, $\omega_d = \omega_{tia}$ and a high frequency pole $\omega_{nd} = \omega_p(1+Av)$; and one zero, $\omega_z = \omega_p$. The DC input impedance is given by :

$$Z_{i,TIA,DC} = \frac{R_f}{(1 + A_{vo})} \tag{2.12}$$

Fig. 2.3 shows the input impedance plot, $Z_{i,TIA}(s)$ of a single-pole TIA filter. The TIA has a DC transimpedance gain of 1kΩ (R_f = 1kΩ) and a bandwidth, ω_{tia} of 20MHz. The TIA op-amp has a low frequency gain, A_{vo} of 1000V/V and a Gain-Bandwidth Product (GBW) of 1GHz. The op-amp -3dB frequency ω_p is calculated to be 1MHz from the following :

$$GBW = A_{vo}\, \omega_p \tag{2.13}$$

Also shown in Fig. 2.4 is a plot of $Z_{i,TIA}(s)$ for a TIA with a feedback impedance $Z_f = R_f = 1k\Omega$.

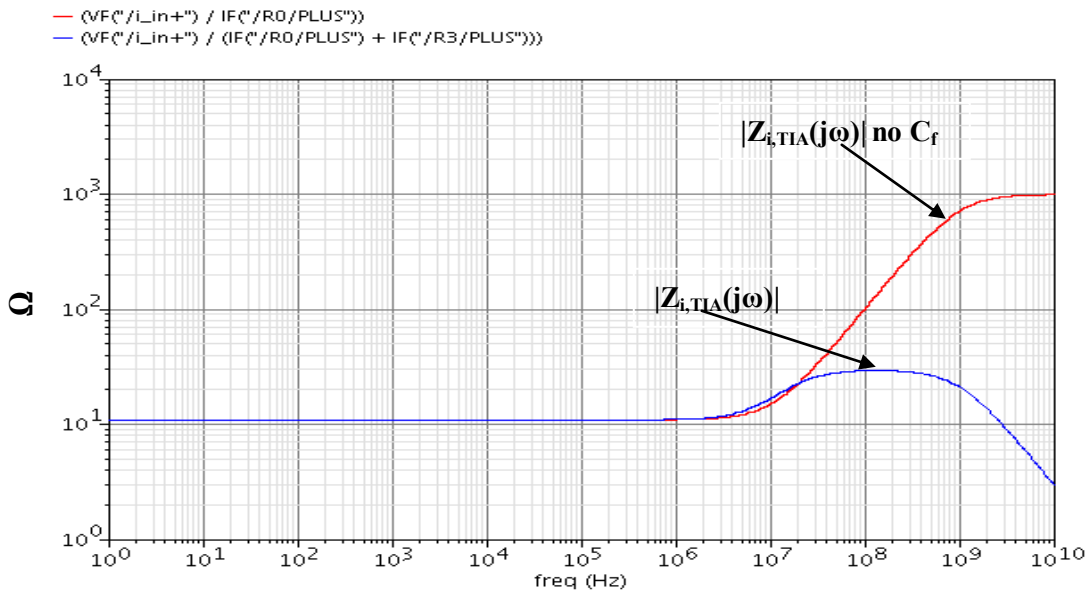


Figure 2.3 TIA Input Impedance Plotted for $Z_f = R_f$ and $Z_f = R_f||C_f$.

From Fig. 2.3, the TIA input impedance magnitude starts at 1Ω at DC and remains at this value until 1MHz. The zero of $Z_{i,TIA}(s)$ is located at this frequency and it causes $|Z_{i,TIA}(s)|$ to increase/rise with a 20dB/decade slope. This rise in $|Z_{i,TIA}(s)|$ from 1MHz onwards is cancelled out by the dominant pole, ω_d of $Z_{i,TIA}(s)$ at 20MHz and $|Z_{i,TIA}(s)|$ flattens out until the higher frequency pole of $Z_{i,TIA}(s)$ is encountered at 1GHz. From this point onwards $|Z_{i,TIA}(s)|$ decreases with a -20dB/decade slope. It can be noted from Fig. 2.4 that with just resistive feedback R_f, the input impedance continues to increase from 1MHz frequency until it eventually reaches the value of R_f at high frequencies since in this case the dominant pole of $Z_{i,TIA}(s)$ formed by ω_{tia} ceases to exist and $Z_{i,TIA}(s)$ will have only one pole at high frequency.

For the same TIA op-amp DC gain, the higher the GBW of the op-amp, the higher the zero frequency of $Z_{i,TIA}(s)$ and the lower the rise in $Z_{i,TIA}(s)$ before ω_d takes effect to flatten the magnitude response of $Z_{i,TIA}(s)$. Thus the higher the GBW value of the TIA op-amp , the lower the TIA filter input impedance and this is demonstrated in Fig. 2.4 where GBW figures of 1GHz, 2GHz and 3GHz are used for the TIA op-amp

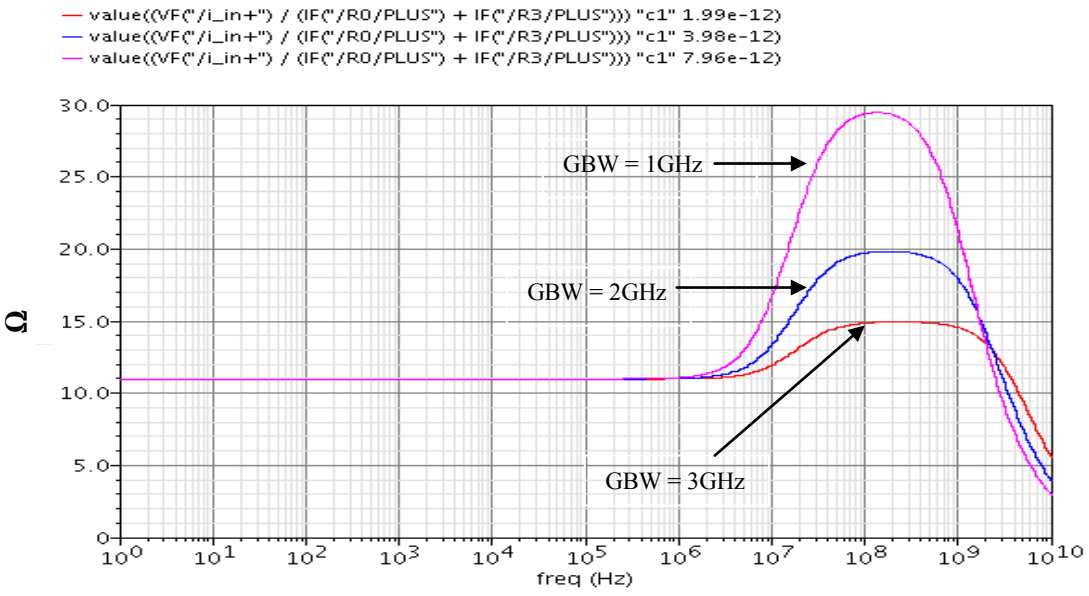


Figure 2.4 Comparison of TIA Input Impedance for Different Values of Op-amp GBW.

In this work a GBW of 1GHz is used for the TIA op-amp. This GBW value gives an acceptable input impedance value (comparable to input impedance levels in published works) across the full-spectrum of signals expected to be processed while keeping power consumption low.

2.2.2 Drawbacks of the Conventional Single-Pole TIA

The transfer function of the conventional single-pole response for a TIA having an in-band gain of 60dB and a 20MHz bandwidth was shown in Fig. 1.4. For close-in OOB

blockers at 60MHz, this filter produces 10dB of attenuation. Typically blockers of up to ±10mA can be expected at such frequencies. Using a single pole TIA filter, this produces a TIA output voltage swing of ±2.8V. Assuming a maximum in-band signal level of ±1mA is to be expected from the mixer, the output voltage swing of the TIA will be ±1V. If no additional filtering is done before the ADC, the in-band signal will represent 36% of the full-scale ADC input level. With additional OOB filtering before the ADC, the in-band signal level will represent a greater percentage of the full-scale ADC input voltage. The advantage in this is that, a lower resolution ADC which has lower number of bits will be required for processing of the baseband signals in the receiver chain. This will reduce the ADC and ADC calibration circuitry cost and complexity and offer a potential savings in power and cost of the receiver chain.

A number of publications have sought to provide extra OOB blocker attenuation (higher order filtering) by cascading filtering blocks to the single-pole TIA as shown in Fig. 2.5. In [5] a filter is cascaded to a gain-programmable TIA and in [9] a biquadratic transimpedance response is implemented as a cascade of two stages.

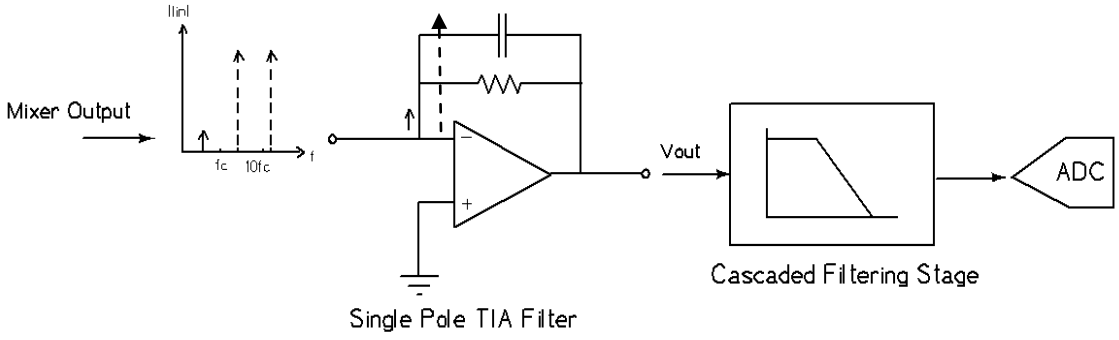


Figure 2.5 Extra OOB Blocker Attenuation through Cascading.

While cascading can provide the extra OOB attenuation required before the ADC to relax its specifications, it offers no relaxation for the large signal linearity requirements

of the single-pole TIA. This is because the same signal swings will appear at the output of the single-pole TIA filter op-amp with or without an additional cascaded filtering stage. And since the TIA op-amp is the source of non-linearity of the single-pole TIA filter, there will be no improvement in its large signal linearity performance.

If we can embed the extra filtering within the TIA filter in the form of feedback, we can achieve the task of relaxing the ADC specifications while at the same time providing improved TIA large signal linearity performance. This will improve receiver linearity and sensitivity and can potentially provide a savings in power and cost of the receiver chain. This argument assumes that the additional power required for the active feedback will be offset by the savings in power of employing a lower resolution ADC for signal processing. Also, since the added feedback block is not in the signal path, the in-band performance of the single-pole TIA is not degraded; input impedance, flicker noise and in-band linearity are not sacrificed. Additionally, it allows for design of the baseband section of the RF front-end receiver at lower supply voltages.

3. PROPOSED TIA FILTER

The proposed TIA filter employs an inverse Chebyshev 3rd order filter approximation in a feedback topology and is shown conceptually in Fig. 3.1. The main idea is to divert large OOB signals that appear at the input nodes of a single-pole TIA filter into an active feedback circuit. This topology provides improved OOB blocker attenuation over the single-pole TIA filter without degrading the in-band performance of the single–pole TIA. Furthermore, this feedback topology allows for design of the baseband section of the front-end receiver chain with low supply voltages and offers improved large-signal linearity over the single-pole TIA filter.

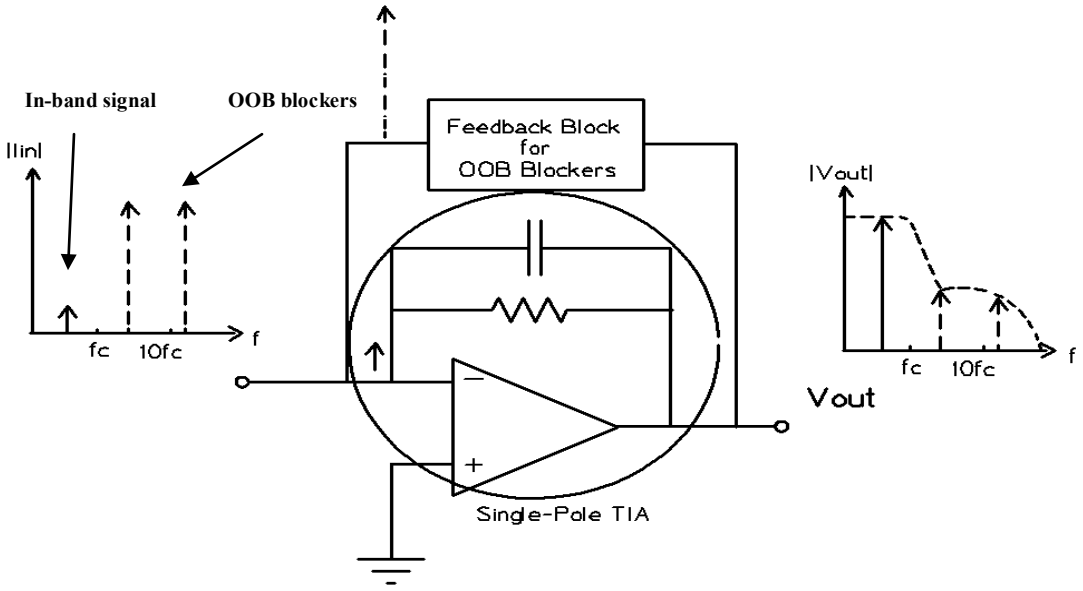


Figure 3.1 Conceptual View of the Proposed TIA Using Active Feedback.

3.1. Conventional Filter Approximations

An inverse Chebyshev filter approximation is chosen for the proposed TIA filter realization. Its features make it the ideal choice over other conventional filter approximations for the purpose of this work.

3.1.1. Lowpass Filter Design Fundamentals

Fig. 3.2 shows an idealized brick-wall low-pass filter. It has full transmission of signals in the pass band, characterized by the bandwidth, ω_p, and has complete attenuation in the stop-band, with an abrupt pass to stop band transition. The pass band denotes the -3dB bandwidth of the desired signal band while the stop band denotes OOB signals (unwanted interferer signals) that the filter is required to attenuate.

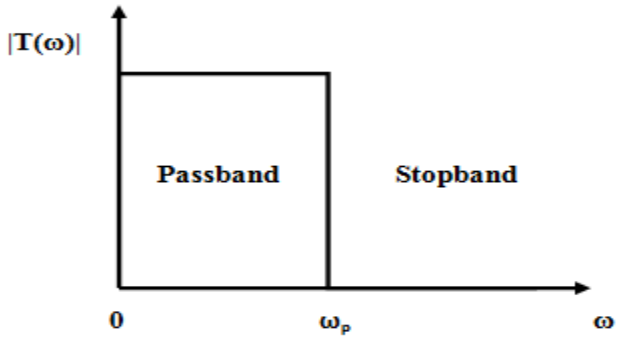


Figure 3.2 Idealized Brick-Wall Filter.

In practice a brick-wall response cannot be achieved and thus OOB signals close to the bandwidth ω_p are not completely attenuated. In practical filter design, specifications are given to define the passband frequency, ω_p; maximum attenuation that can be tolerated within the passband, α_{MAX} ; closest out-of-band signal frequency, ω_s ; and the minimum attenuation desired at this frequency and beyond, α_{MIN} . This is illustrated by Fig. 3.3. It should also be noted that a non-abrupt transition band exists for the practical filter given by the frequency range ω_s to ω_p, something which is non-existent in the brick-wall filter.

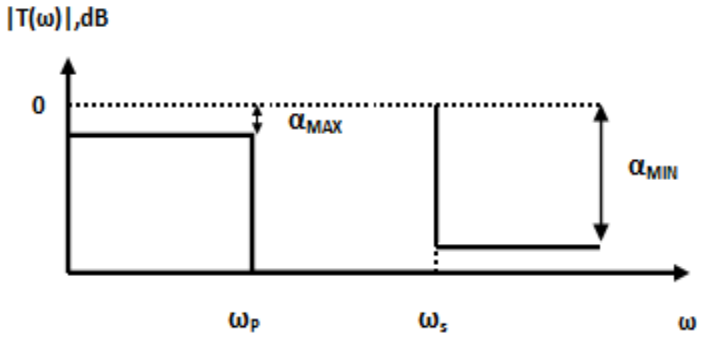


Figure 3.3 Practical Lowpass Filter Design Parameters.

3.1.2. Comparison of Lowpass Filter Approximations

The conventional practical filter approximations that exist are :

a. Butterworth
b. Chebyshev
c. inverse Chebyshev
d. Elliptic

In addition to the practical filter design specifications given in the previous section, a parameter which is often used to compare these filter approximations is group delay. Ideally a linear phase response within the pass band is desirable in analog filters to avoid distortion of the in-band signals. However in practical filter approximations such as the above, the phase deviates from this linear response. The group delay, which is defined as the derivative of the phase response of the filter with respect to angular frequency, can be used to quantify the distortion in the desired in-band signal introduced by phase differences for different frequencies within the filter.

For the same order of filtering, stop-band attenuation at close-in frequencies increases in the following order :

Butterworth< Chebyshev/inverse Chebyshev < Elliptic.

Whereas for the same order of filtering, in-band group delay variation decreases in the following order:

Elliptic< Chebyshev < inverse Chebyshev < Butterworth.

Fig. 3.4 shows a comparison of the magnitude plots of the aforementioned filter approximations. From the discussion in Section 1, a filter is required which is capable of providing maximum attenuation at close-in frequencies. For the same order of filtering, the elliptic filter would be the best possible choice with regards to stop band attenuation only. However, the inverse Chebyshev filter represents the best possible combination of stop band attenuation (desired for OOB blocker attenuation) and in-band group delay (small group delay variation is desirable for minimal in-band signal distortion arising from non-linear phase). Since the inverse Chebyshev filter has no in-band ripples, it is chosen over the elliptic filter in the design of the proposed TIA filter. A third order filter design is targeted to provide adequate close-in OOB blocker attenuation.

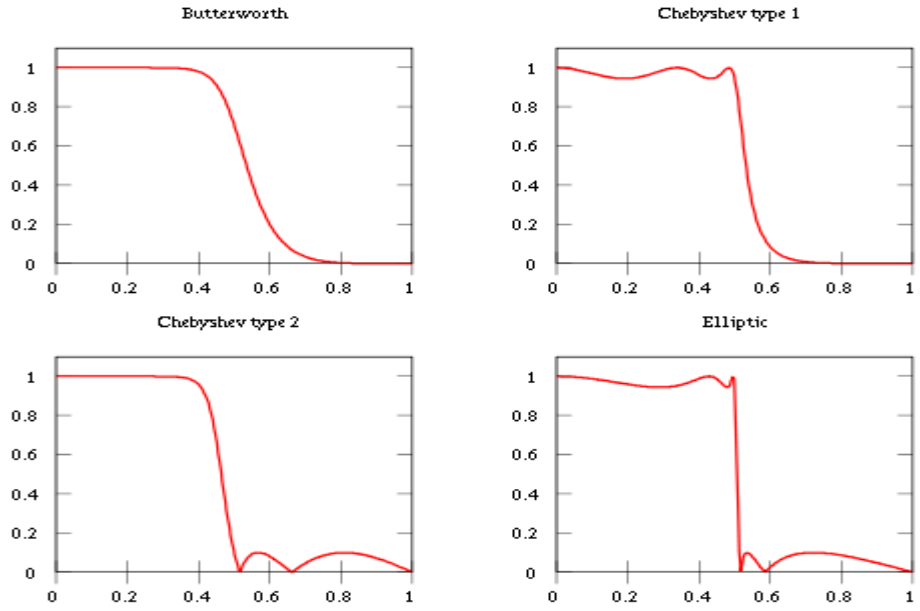


Figure 3.4 Comparison of Filter Approximations; All Filters are Fifth Order.

3.2 System Level Design of 3rd Order Inverse Chebyshev Feedback Filter with Bandwidth of 20MHz and Notch at 60MHz

The block diagram for the proposed feedback TIA is shown in Fig. 3.5. The transfer function of this system is given by :

$$T(s) = \frac{I(s)}{V(s)} = \frac{A(s)}{1 + A(s)H(s)} \tag{3.1}$$

where *A(s)* represents the single-pole TIA filter and *H(s)* represents the active feedback network required for improved OOB attenuation. The closed-loop system transfer function, *T(s)*, is obtained from a 3rd order inverse Chebyshev filter approximation. Since the filter approximation equations are stable, ideally *T(s)* will be inherently stable.

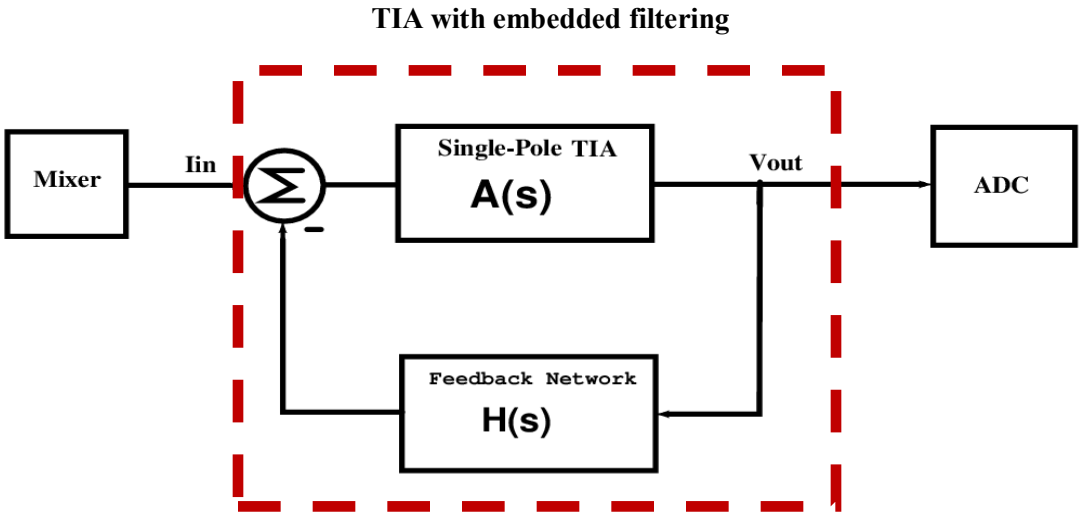


Figure 3.5 The General Feedback Structure.

A 3rd order inverse Chebyshev filter is synthesized using MATLAB. Generally for a fixed notch frequency (in this case 60MHz), the greater the α_{MIN}, the lower the -3dB bandwidth of the filter as shown in Fig. 3.6.

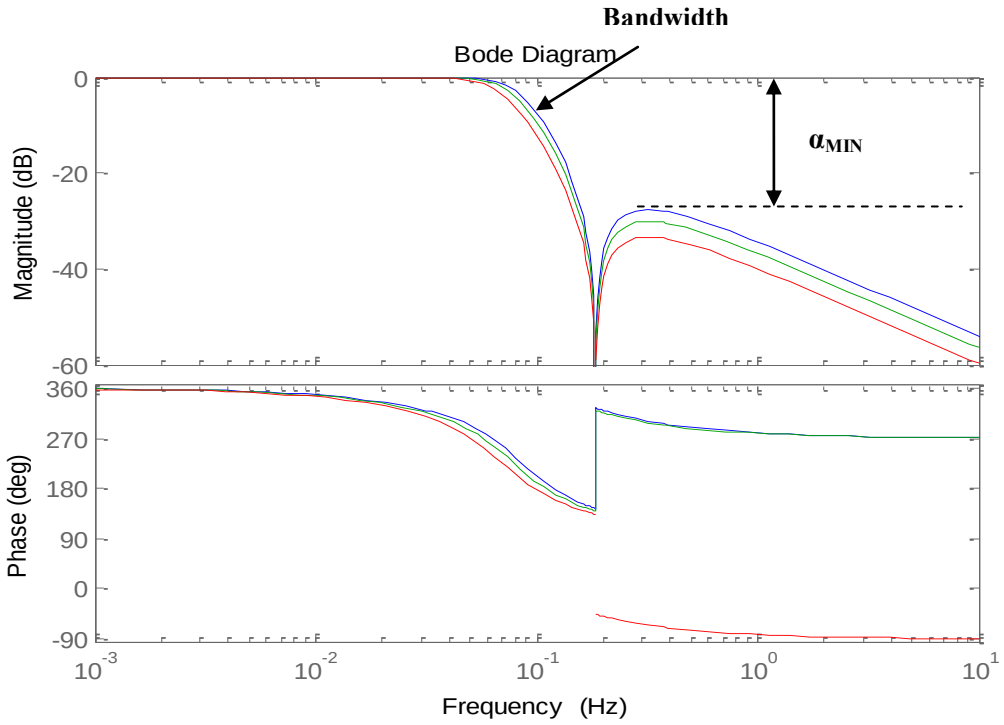


Figure 3.6 Trade-Off between Bandwidth and Stop-Band Attenuation for a Fixed Notch Frequency.

For a bandwidth of 20MHz with a 60MHz notch, the largest α_{MIN} achievable is 35.5dB as shown in Fig. 3.7. The corresponding normalized inverse Chebyshev transfer function is given as :

$$T(s) = A.\frac{1}{s + 0.425}\left(\frac{s^2 + 1.333}{s^2 + 0.3743\,s + 0.1591}\right) \tag{3.2}$$

where:

$$A = \frac{0.1591 \times 0.425}{1.333} \tag{3.3}$$

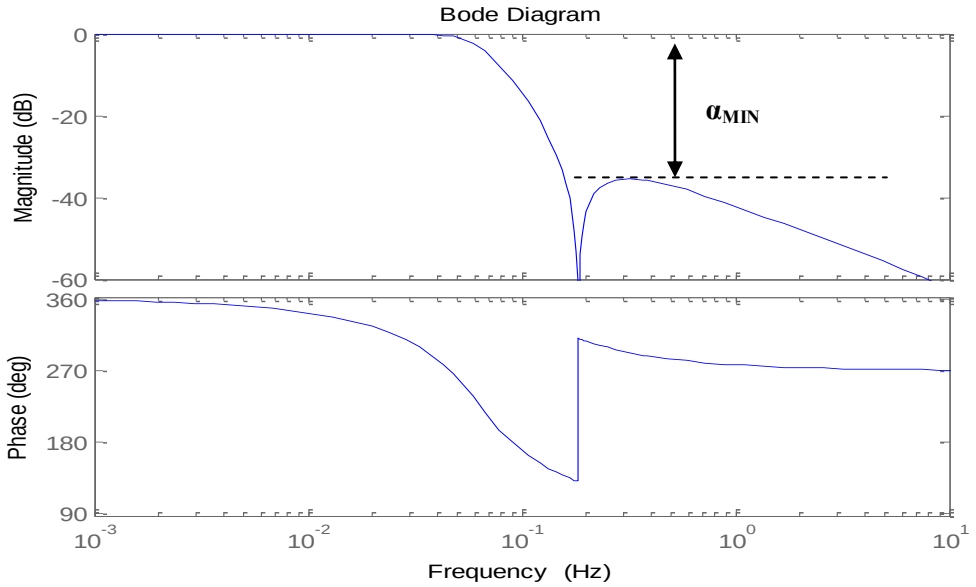


Figure 3.7 Magnitude and Phase Plot of the Synthesized 3rd Order Inverse Chebyshev Filter.

Note that (3.3) is required to scale the passband gain of (3.2) to 0dB. The coefficients in (3.2) are replaced with variables as follows :

$$T(s) = \frac{A}{s + D}\left(\frac{s^2 + n}{s^2 + B\,s + C}\right) \tag{3.4}$$

where n *=1.333; B = 0.3743; C = 0.1591; D = 0.4250*

Magnitude and frequency scaling of *T(s)* to give a low frequency gain of 60dBΩ (1000 Ω), a bandwidth of 20MHz and a notch frequency of 60MHz gives :

$$T(s) = \left(\frac{s^2 + n{\omega_o}^2}{s^2 + B\,\omega_0\,s + C\,{\omega_o}^2}\right)\left(\frac{A_\omega}{s + D\omega_0}\right) \tag{3.5}$$

where A_ω= *-1000CDω₀/n* and $\omega_0 = \sqrt{n} \times 60e6$. Note that the magnitude scaling factor A_ω is negative since the TIA has a negative gain as derived in (2.4) . The frequency response of (3.5) is shown in Fig. 3.8.

In (3.5), the 2nd term in brackets represents the single-pole TIA filter function, A(s). From (3.5) :

$$T(s)|_{s=0} = -1000\Omega \tag{3.6}$$

$$A(s)|_{s=0} = -\frac{1000C}{n} = -R_f \tag{3.7}$$

Clearly (3.6) and (3.7) are different, meaning that for a closed-loop TIA DC gain $T(s)|_{s=0}$ of 60dBΩ the feedback resistor, R_f, of the single-pole TIA will need to be 119Ω from (3.7). This value of R_f will increase the input referred noise current density of the single-pole TIA filter by the ratio $(C/n)^2$ A^2 /Hz. Also, since we do not want to alter the small-signal in-band characteristics of the conventional single-pole TIA, R_f is kept at 1KΩ. This requires us to introduce a scaling factor, X into (3.5) such that (3.6) will equal (3.7) :

$$T(s) = \left(\frac{1}{X}\,\frac{s^2 + nw_o{}^2}{s^2 + B\,w_0\,s + C\,w_o{}^2}\right)\left(\frac{-A_w KX}{s + Dw_0}\right) \tag{3.8}$$

where $X = n/C$. (3.8) gives the desired transimpedance function we want to synthesize. Thus (3.8) is equated to (3.1) as shown :

$$T(s) = \left(\frac{1}{X}\,\frac{s^2 + nw_o{}^2}{s^2 + B\,w_0\,s + C\,w_o{}^2}\right)\left(\frac{-A_w KX}{s + Dw_0}\right) = \frac{A(s)}{1 + A(s)H(s)} \tag{3.9}$$

As stated before, $A(s)$ represents the conventional single-pole TIA filter and forms the forward path of the closed-loop system. What remains then, is to derive the feedback transfer function $H(s)$ from (3.9) as :

$$H(s) = \frac{I(s)}{V(s)} = \frac{as^3 + b\,s^2 + c\,s + d}{s^2 + p} \tag{3.10}$$

where :

$$a = (X - 1)\,Y \tag{3.11}$$

$$b = \big(XB + D(X - 1)\big)\,Y\omega_0 \tag{3.12}$$

$$c = (C - n + DB)\, XY\omega_0^3 \tag{3.13}$$

$$d = D\,(XC - n)\, Y\omega_0^3 \tag{3.14}$$

$$p = n\omega_0^2 \tag{3.15}$$

$$Y = A_\omega \tag{3.16}$$

(3.10) gives the feedback function we need to implement. *H(s)* in essence is a high pass transfer function as shown in Fig. 3.9. It can be thought of as being transparent to in-band signals and only being active when OOB signals are present.

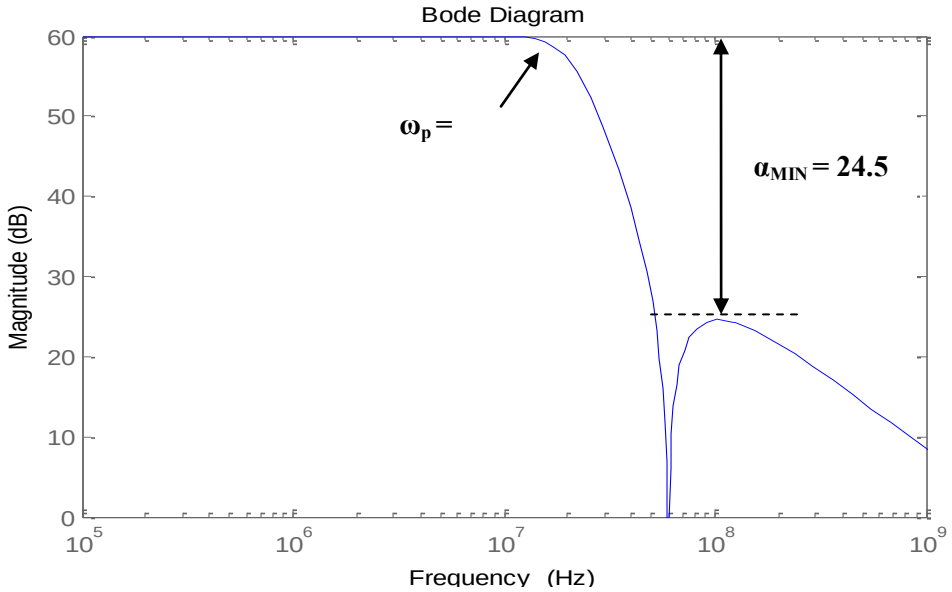


Figure 3.8 Synthesized Inverse Chebyshev Magntiude Plot with a Passband Gain of 60dBΩ, a Bandwidth of 20MHz with a 60MHz Notch.

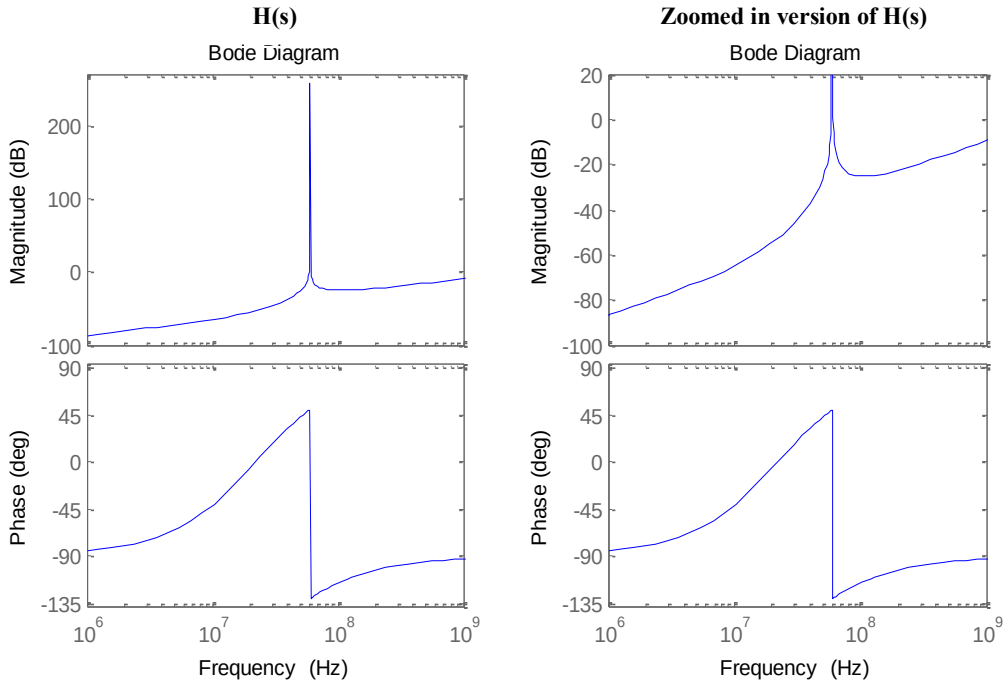


Figure 3.9 Magnitude and Phase Plot of H(s).

3.2.1 Approximation of *H(s)* for Practical Circuit Implementation

It is possible to implement *H(s)* in several different ways, however the choice of implementation may introduce low frequency poles into the feedback loop thus making the proposed TIA unstable. For our application, we want to be able to implement *H(s)* as a voltage input, voltage output biquad (two pole function with 2 zeros) in which the voltage to current conversion is done through a capacitor. Thus we factor out *'as'* from (3.10) to obtain :

$$H(s) = H_1(s)H_2(s) = \frac{I}{V}\frac{V}{V} = as\left(\frac{s^2 + {}^{b}/_{a}\,s + {}^{c}/_{a} + {}^{d}/_{a}\,s}{s^2 + p}\right) \qquad (3.17)$$

where '*as*' is realised by a capacitance. The term in brackets constitutes the voltage in, voltage out biquad, which is denoted as $H_2(s)$. It is not in a form that can be readily implemented at circuit level. By eliminating the last term in the numerator of $H_2(s)$, we obtain a biquad function which can be easily implemented:

$$H'(s) = H_1(s)\, H_2'(s) = \frac{I}{V}\,\frac{V}{V} = as\left(\frac{s^2 + {}^{b}/_{a}\, s + {}^{c}/_{a}}{s^2 + p}\right) \qquad (3.18)$$

Now (3.18) is in a form which is amenable to circuit implementation. Matlab pole-zero plots in Fig. 3.10 show that the zero locations of (3.17) and (3.18) are different. However, a look at the frequency response plots of (3.17) and (3.18) in Fig. 3.11 show that they are the same. A step response in Fig. 3.12 obtained after substituting (3.17) and the modified form in (3.18) into (3.1) shows that the TIA filter stability is not affected. Thus from this point on, (3.18) is used.

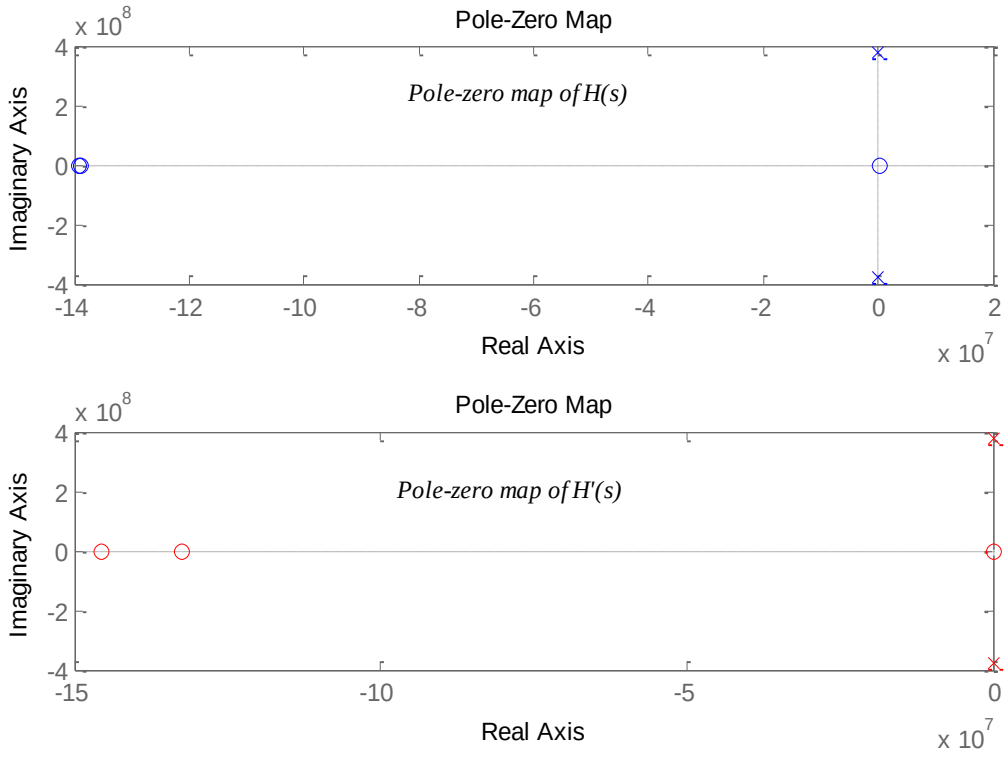


Figure 3.10 Pole- Zero Map of *H(s)* and *H'(s)*.

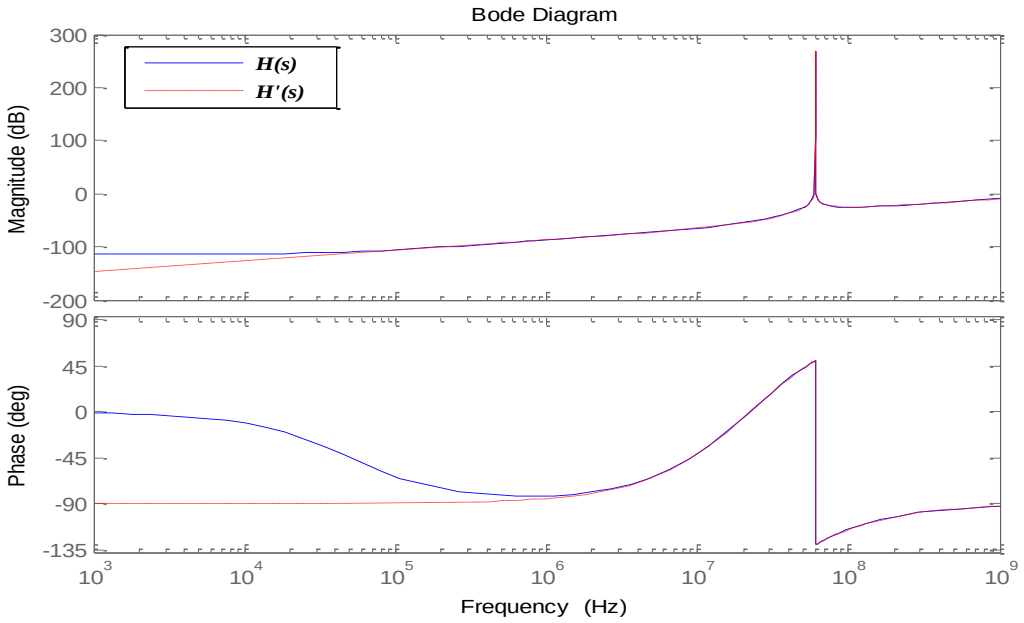


Figure 3.11 Matlab Frequency Response of *H(s)* and *H'(s)*.

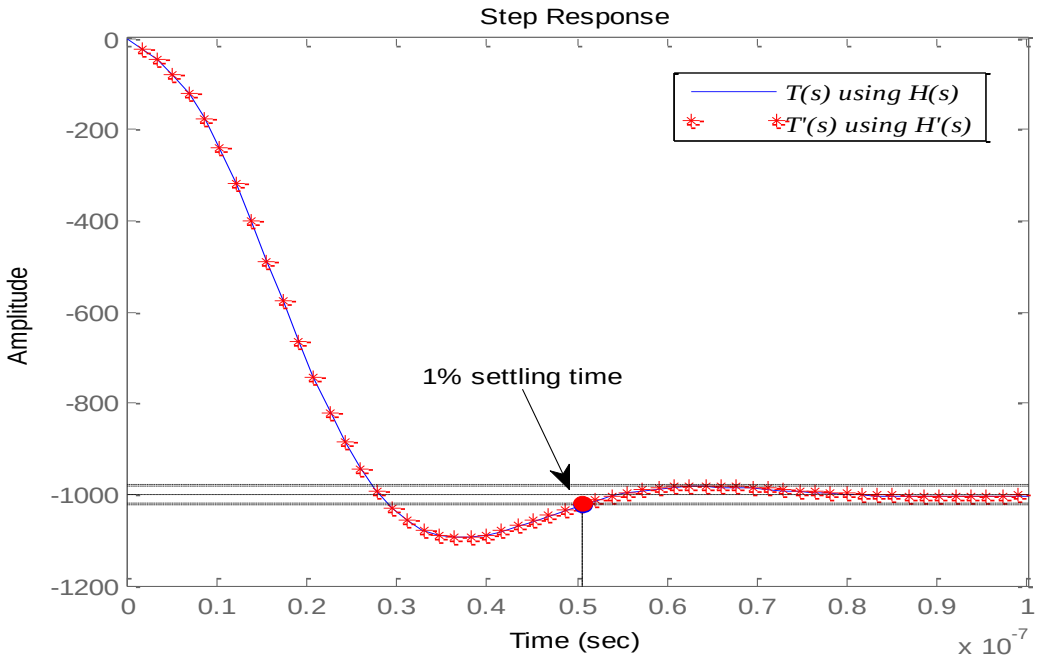


Figure 3.12 TIA Step Response Obtained by Substituting *H(s)* and *H'(s)* into (3.1).

Substituting the values of the variables *a,b,c,* and *p* into (3.18) gives :

$$H'(s) = H_1(s)\,H_2'(s) = 53 \times 10^{-12}\, s \left(\frac{s^2 + 2.78 \times 10^8 s + 1.93 \times 10^{16}}{s^2 + 1.42 \times 10^{17}} \right) \quad (3.19)$$

The general form of a biquadratic transfer function with arbitrary zeros is given by:

$$B(s) = \frac{a\,s^2 + b\,s + c}{s^2 + \frac{w_0}{Q}\,s + {w_0}^2} \quad (3.20)$$

Comparing (3.19) to the general form in (3.20) shows that *H'(s)* is an infinite Q function. This is evident in the plots of Fig. 3.11 where we see that there is infinite peaking in (3.19). This peaking is due to the 60MHz notch of the inverse Chebyshev filter. In the front-end receiver, OOB blockers are not confined to a single frequency and what we seek to do in this work is to provide attenuation to OOB blockers from 60MHz and beyond. What is important is that the designed filter provides adequate attenuation for the full-scale blocker signal magnitudes expected at 60MHz and higher frequencies. Thus, the 60MHz notch is not necessary. By removing this notch, the peaking in *H'(s)* can be eliminated. Ultimately, the entire feedback function, *H'(s)*, with the peaking removed becomes :

$$H''(s) = \frac{I(s)}{V(s)}\,\frac{V(s)}{V(s)} \quad (3.21a)$$

$$H''(s) = H_1(s)\,H_2''(s) \quad (3.21b)$$

$$H''(s) = 53 \times 10^{-12}\, s \left(\frac{s^2 + 2.78 \times 10^8 s + 1.93 \times 10^{16}}{s^2 + 3 \times 10^8 s + 1.42 \times 10^{17}} \right) \quad (3.21c)$$

MATLAB plots of the closed-loop system magnitude responses, *T''(s)* and *T(s)*, are shown in Fig. 3.13. Also superimposed is the transfer function of the single-pole TIA filter for comparison. It will be shown in later sections that though the notch at 60MHz is removed, the modified TIA filter provides adequate attenuation for the close-in OOB blockers (full-scale magnitude of 4.5mA) that this design targets. Although by removing

the notch, the bandwidth of the TIA is reduced, it is trivial to extend the bandwidth back to 20MHz by frequency scaling or to compensate for this loss by adjusting the value of the TIA feedback capacitor, C_f.

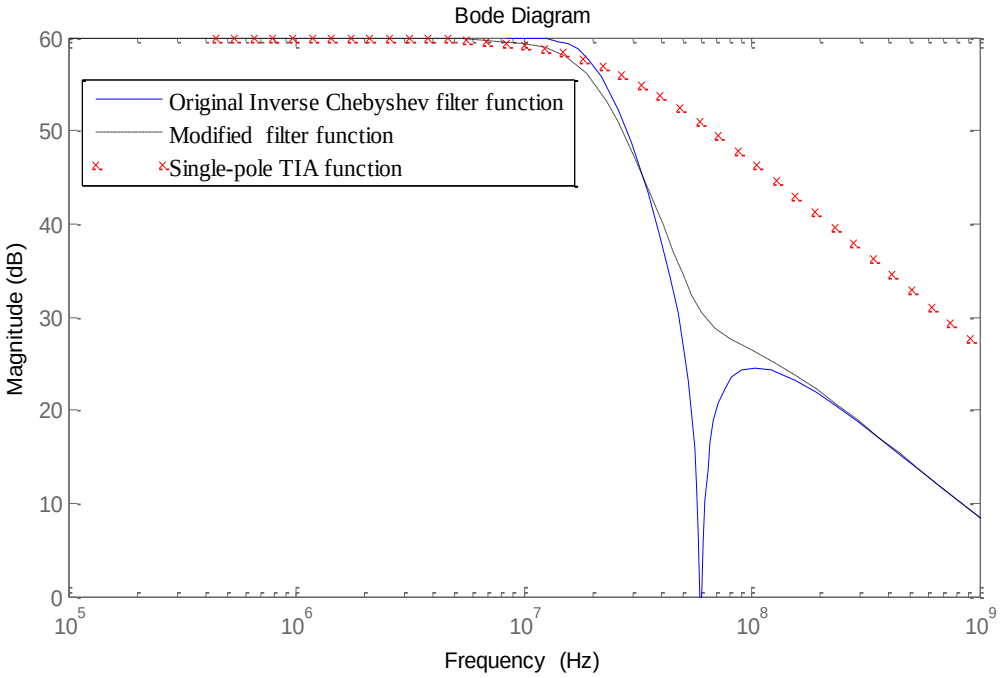


Figure 3.13 Comparison of Original Inverse Chebyshev Filter, Modified Filter and Single-Pole Filter Functions.

H''(s) in (3.21) is essentially a biquad which is divided into $H_1(s)$ and $H_2''(s)$. $H_1(s)$ represents a voltage-to-current converter and its form means it can readily be implemented with a 53pF capacitor.

In the circuit realization of $H_2''(s)$, the first target is to minimize its power consumption. This means utilizing a biquad topology with a minimal number of op-amps. Also, the biquad architecture chosen must be capable of implementing arbitrary transmission zeros

as the numerator of $H_2''(s)$ demands. A biquad topology that uses the lowest number of op-amps possible and at the same time implements arbitrary transmission zeros is a feedforward Tow-Thomas biquad. $H_2''(s)$ is thus implemented with this biquad topology.

3.3. Tow-Thomas Based Implementation of $H_2''(s)$

The Tow-Thomas fully-differential biquad is shown in Fig. 3.14 . $H_2''(s)$ from (3.21c) is given as:

$$H_2''(s) = \frac{s^2 + 2.78 \times 10^8 s + 1.93 \times 10^{16}}{s^2 + 3 \times 10^8 s + 1.42 \times 10^{17}} \tag{3.22}$$

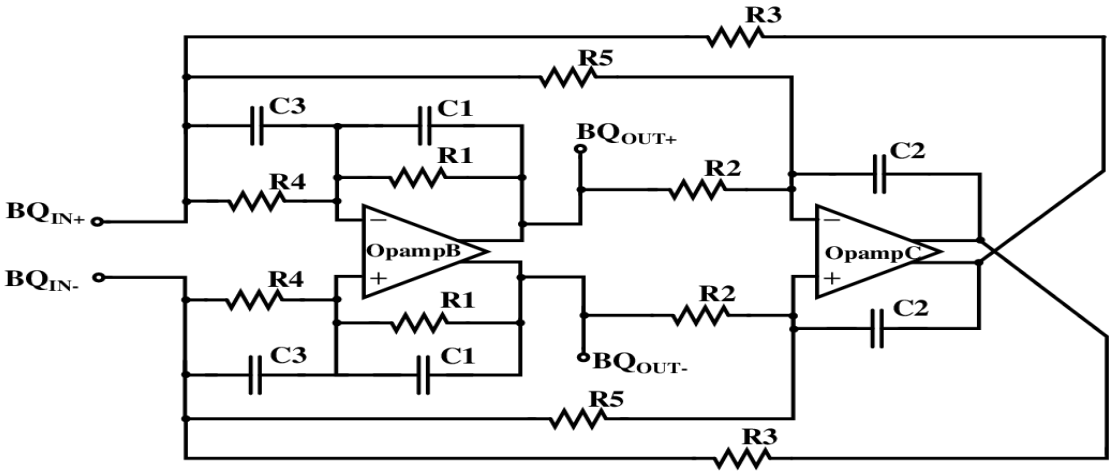


Figure 3.14 Fully-Differential Tow-Thomas Biquad for Implementing Second Order Functions with Arbitrary Transmission Zeros.

The transfer function for the feedforward Tow-Thomas of Fig. 3.14 is given as :

$$H_2''(s)_{TT} = -\frac{(C_3/C_1)\, s^2 + s/R_4C_1 + 1/R_5 R_3 C_2 C_1}{s^2 + s/R_1C_1 + 1/R_2R_3C_2C_1} \tag{3.23}$$

3.4 Macro-Modeling of the Proposed TIA Filter in Cadence

Equating the constant terms in the denominators of (3.20), (3.22) and (3.23) gives :

$$\omega_0 = \frac{1}{R_2 R_3 C_2 C_1} = 1.42 \times 10^{17} \tag{3.24}$$

A choice of 1KΩ is made for R_2 and R_3. Also, C_1 and C_2 are chosen to have the same value and their value is calculated from (3.24) to be 2.65pF. Now equating the other coefficients of the numerator and the denominator terms of (3.20), (3.22) and (3.23) gives the values of R_1, R_4, R_5, and C_3.

The proposed TIA filter is implemented in Cadence using ideal op-amps with capacitors and resistors. The top-level system is shown in Fig. 3.15. Fig. 3.16 shows the AC response of the TIA and this response is compared with that of the single-pole TIA filter, which is superimposed in the plot. The list of component parameters calculated from (3.20), (3.22) and (3.23) is given in Table 3.1.

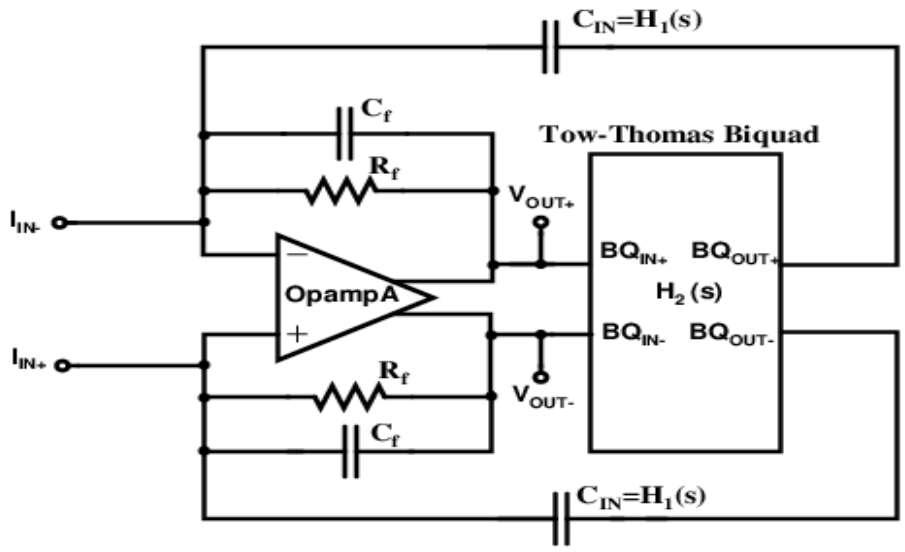


Figure 3.15 Macro-Model of Proposed TIA Filter Using Ideal Op-amps in Cadence.

Table 3.1 Component Values for Macro-Model Simulations.

Simulation Conditions:OpampA, OpampB and OpampC have 60dB DC Gain, GBW = infinite			
Component	**Value**	**Component**	**Value**
C_F	7.2pF	R_1	1.26KΩ
R_F	1KΩ	R_2	1KΩ
C_{IN}	52.98pF	R_3	1 KΩ
C_1	2.65pF	R_4	1 KΩ
C_2	2.65pF	R_5	7.39 KΩ
C_3	2.65pF		

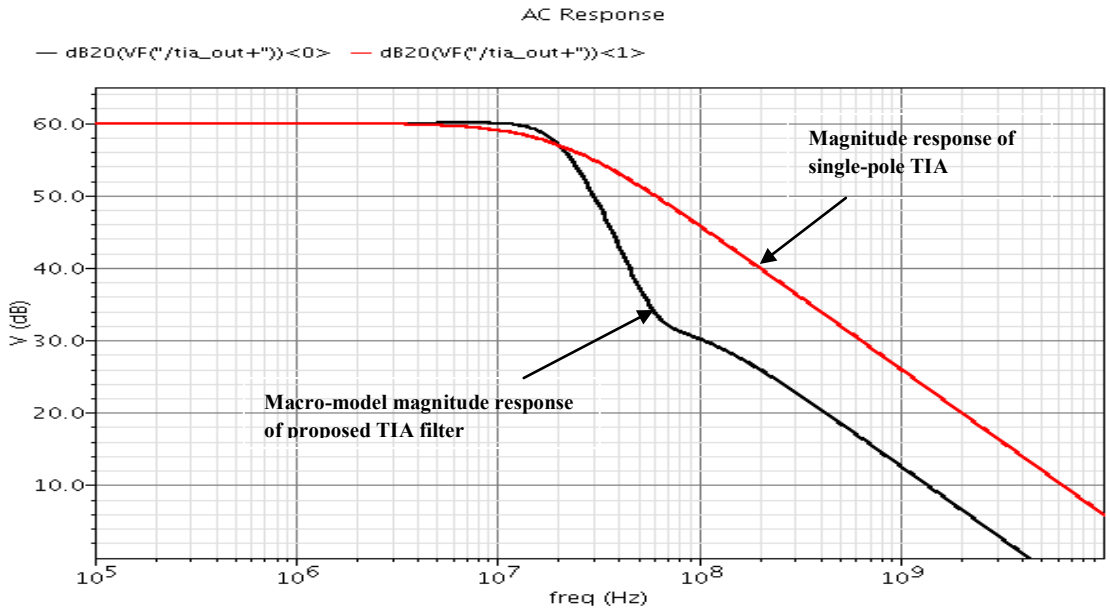


Figure 3.16 Proposed TIA Filter Magnitude Response Using Ideal Op-amps with Infinite GBW.

3.4.1 Macro-Modeling Using Single-Pole Op-amps with Finite Gain and Finite GBW

In the previous section, macro-modeling was done in Cadence using op-amps with finite gain of 60dB and infinite GBW. However, practical op-amps have GBW limitations and this leads to deviation from the ideal filter frequency response, especially at high frequencies. Although the rule of thumb is to use GBW values of $10 \times f_{3dB}$, we note that for the proposed TIA filter, it is important to determine how much the high frequency response deviates from the ideal response in Fig. 3.16, since the filter is required to process high frequency OOB blockers in addition to the in-band signals. Also, since we are dealing with a feedback system, it is important to examine how the loop stability will be affected by the finite GBW of the op-amps within the loop.

A detailed look at the op-amp GBW limits in this section then is important to prevent over-design since the higher the GBW, the greater the power consumption. Thus, we can use the minimum possible GBW values for the op-amps to keep power consumption at a minimum without distorting the filter shape at high blocker frequencies. It will be recalled from section 2 that the GBW of OpampA is important for keeping the input impedance of the TIA at a minimum, and a minimum of 1 GHz GBW was determined for this op-amp. Therefore, the GBW of OpampA is fixed at 1GHz. What remains is to determine the acceptable GBW values for OpampB and OpampC. A single-pole model is used for the op-amps.

Firstly, we look at the effect of finite GBW of OpampB on the filter shape. An infinite GBW is used for OpampC and the GBW of OpampB is varied from 250MHz – 2GHz and the resulting TIA magnitude response is plotted in Fig. 3.17.

Secondly, we look at the effect of finite GBW of OpampC on the filter shape. An infinite GBW is used for OpampB and the GBW of OpampC is varied from 250MHz – 2GHz and the resultant filter magnitude response is plotted in Fig. 3.18.

Two observations can be made from the simulation plots of Fig. 3.17 and Fig. 3.18 :

a) Decreasing the GBW of OpampB in the biquad has the primary effect of decreasing α_{MIN}. As a secondary effect, the bandwidth of the filter decreases as OpampB GBW is decreased .

b) As the GBW of OpampC is decreased, the bandwidth of the filter decreases. GBW variation in OpampC does not have a significant effect on the OOB attenuation of the filter.

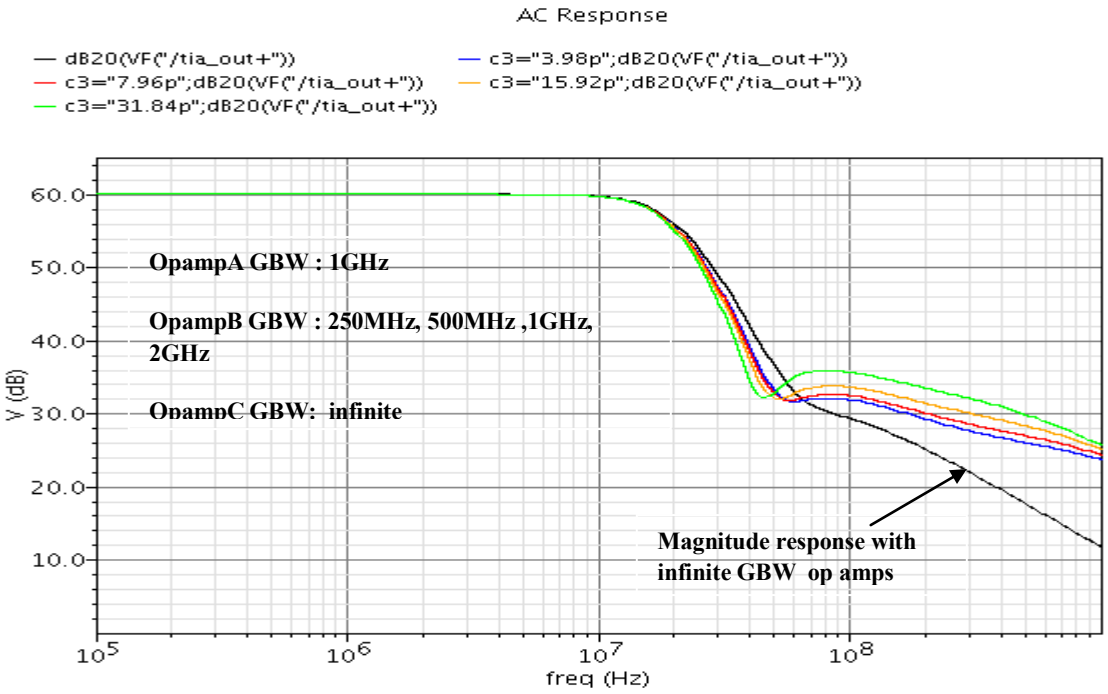


Figure 3.17 Proposed TIA Filter Response for the Following Op-amp GBW Conditions: OpampA - 1GHz, OpampC - Infinite, OpampB - 250MHz, 500MHz, 1GHz, 2GHz.

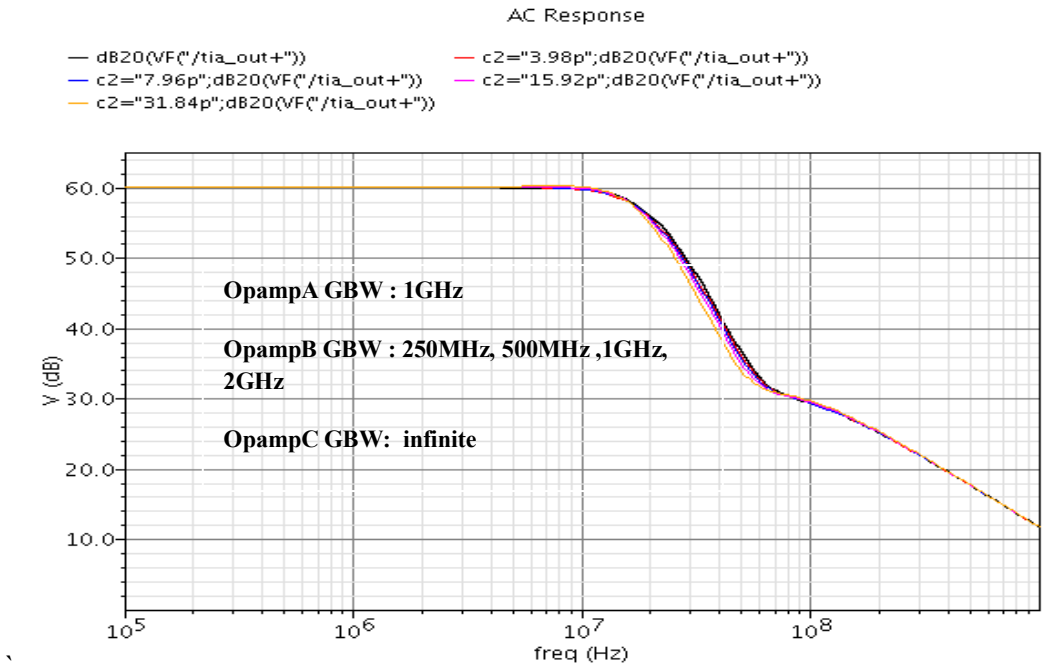


Figure 3.18 Proposed TIA Filter Response for the Following Op-amp GBW Conditions: OpampA -1GHz, OpampB - Infinite, OpampC - 250MHz, 500MHz, 1GHz, 2GHz.

3.4.2 Effect of Finite Op-amp GBW on Stability

Fig. 3.19 shows the loop gain of the proposed TIA filter for op-amp gain of 60dB and infinite GBW. It can be seen that the loop gain does not exceed 0dB and thus we have a stable system.

Next we look at the effect of finite op-amp GBW on the loop gain and stability of the proposed TIA filter. As stated before a GBW of 1GHz is chosen for OpampA. In the previous section we varied the GBWs of both OpampB and OpampC from 250MHz-2GHz independently using single-pole models for the amplifiers. These GBW values are typical, and can be easily achieved in sub-micron processes such as IBM 90nm. In this section, both OpampB and OpampC GBWs are swept from 250MHz-2GHz and Fig. 3.20 plots the variation in the loop gain.

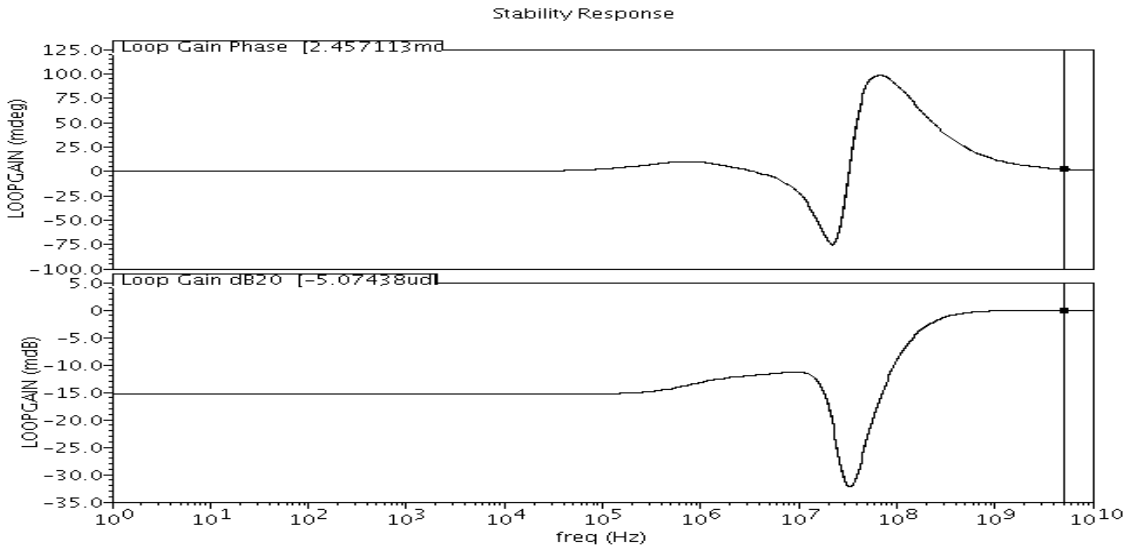


Figure 3.19 Proposed TIA Filter Loop Gain Magnitude and Phase Response Using Op-amps with 60dB Gain and Infinite GBW.

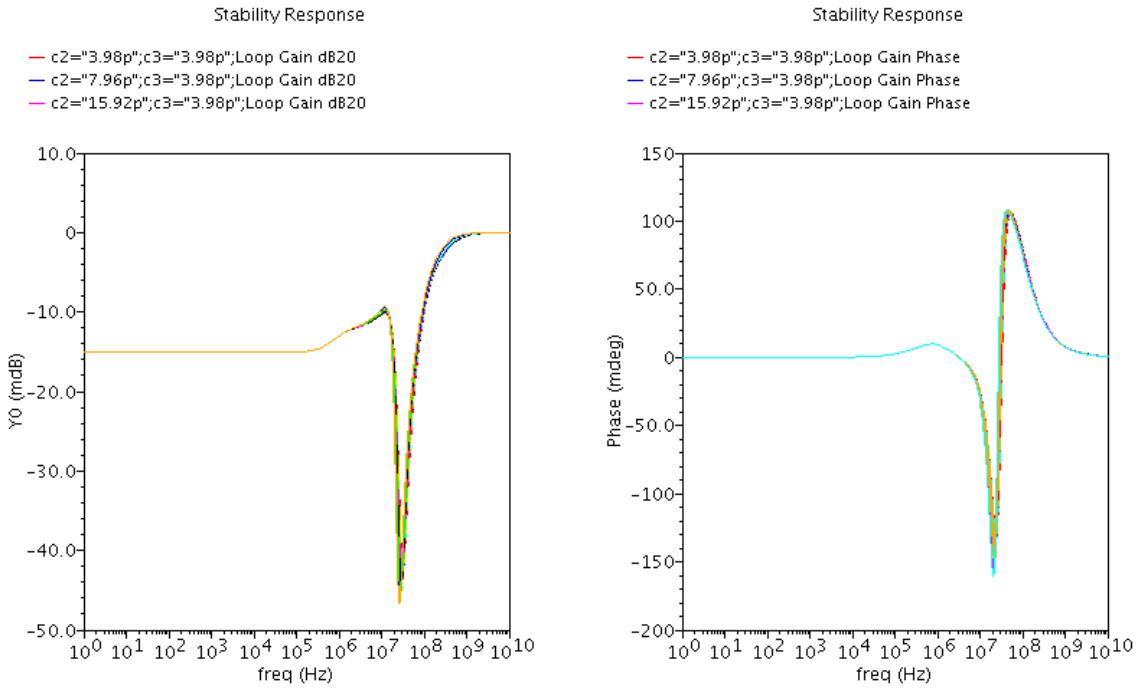


Figure 3.20 Loop Gain Magnitude and Phase Response for a Parametric Sweep of OpampB and OpampC GBWs : 250MHz- 2GHz.

We see from Fig. 3.20 that for the range of GBW values that can be achieved in IBM 90nm process, the loop gain phase response does not vary by more than 1degree and hence the TIA filter is stable for these typical GBW values. Therefore stability is not critical in the implementation of the proposed TIA filter in this work. However, it must be noted that the single-pole amplifier macro-models used in this study of stability is a bit too simplistic. Real op-amps have higher frequency poles. But transient simulations done at transistor level provided in Section 5 show a stable system, thus the single-pole amplifiers used in macro-modeling offer a good approximation for stability.

3.5. Transistor Level Design Specifications and Considerations

Macro-modeling has been done in the previous section to determine the op-amp GBW limits that can be tolerated in the design. In this section transistor level design specifications and considerations will be outlined.

This work is implemented in IBM 90nm CMOS process with a supply voltage of 1.2V. The maximum output voltage swing requirement for the TIA filter is ± 200mV single-ended. The target OOB blocker magnitude to be processed by this filter is ±4.5mA single-ended at 60MHz and higher frequencies. Table 3.2 shows the loading for OpampA, OpampB, and OpampC .

Table 3.2 Amplifier Loading.

Amplifier	Loading
OpampA	R_f //C_f = 1KΩ//7.2pF
OpampB	R1||C1||C_{IN} = 1.26KΩ//55.63pF
OpampC	C2 = 2.65pF

As determined before, OpampA GBW is 1GHz. OpampC GBW is also selected to be 1GHz. We notice from Fig. 3.14 and Fig. 3.15 that OpampB's capacitive load of 55.63pF is close to 8 times the capacitive loading of OpampA. To obtain similar GBW

values for OpampB with its capacitive load specification, significant amount of power needs to be dissipated. We therefore look at ways of reducing the loading on this amplifier. C_{IN} can be reduced to reduce the loading on OpampB. Fig. 3.21 shows the effect of C_{IN} on the filter response. A reduction of C_{IN} by half (from 52.98pF to 26.49pF) reduces the TIA OOB attenuation by 6dB. Reducing C_{IN} increases the filter bandwidth as well, but this can be compensated for easily by increasing the value of C_f.

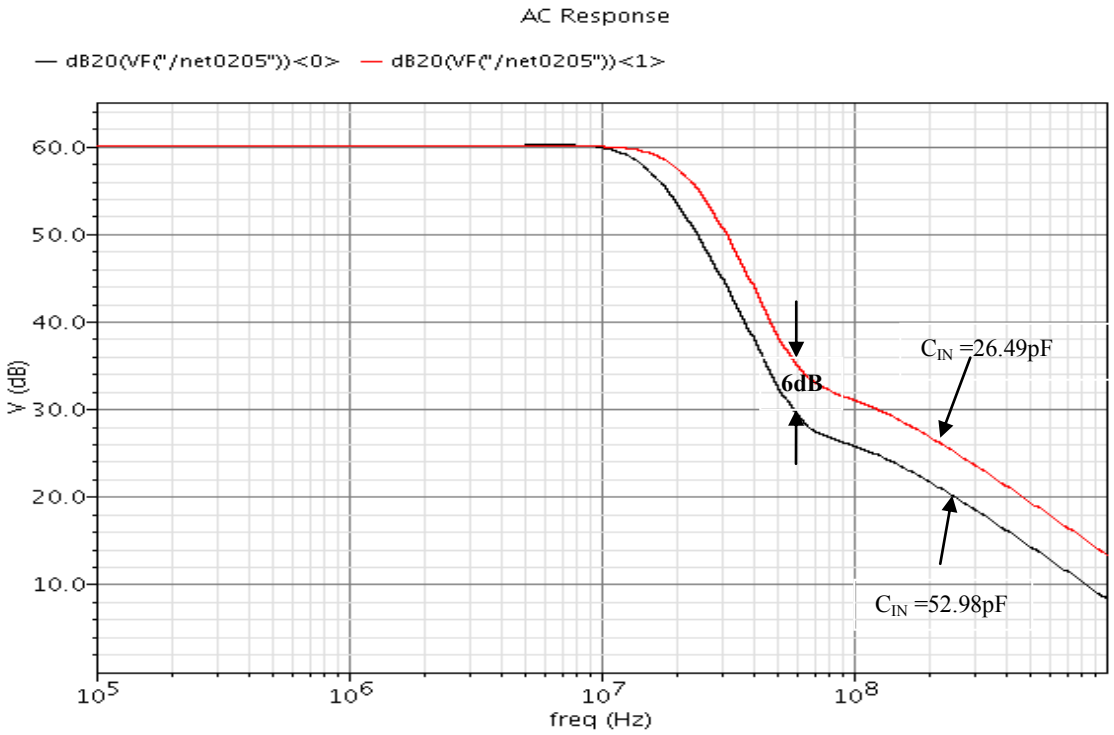


Figure 3.21 Variation of Proposed TIA Filter OOB Attenuation with C_{IN}.

To determine how low the value of C_{IN} can be set, one needs to look at two issues. Firstly, the loss in OOB attenuation that can be tolerated by the system and secondly the increase in voltage swing at the output of OpampB as a result of the reduction of C_{IN}.

We note that a fullscale blocker current of 4.5mA needs to be tolerated at 60MHz. OpampB needs to be able to source/sink this blocker current through C_{IN} . It can be seen

from Fig. 3.14 and Fig. 3.15 that while one terminal of C_{IN} is connected to the output of OpampB the other terminal of C_{IN} connects to the input of OpampA which is a virtual ground and therefore OpampB can considered as driving a ±4.5mA current through a shunt capacitor, C_{IN}. A single-ended representation of OpampB within the TIA is shown in Fig. 3.22.

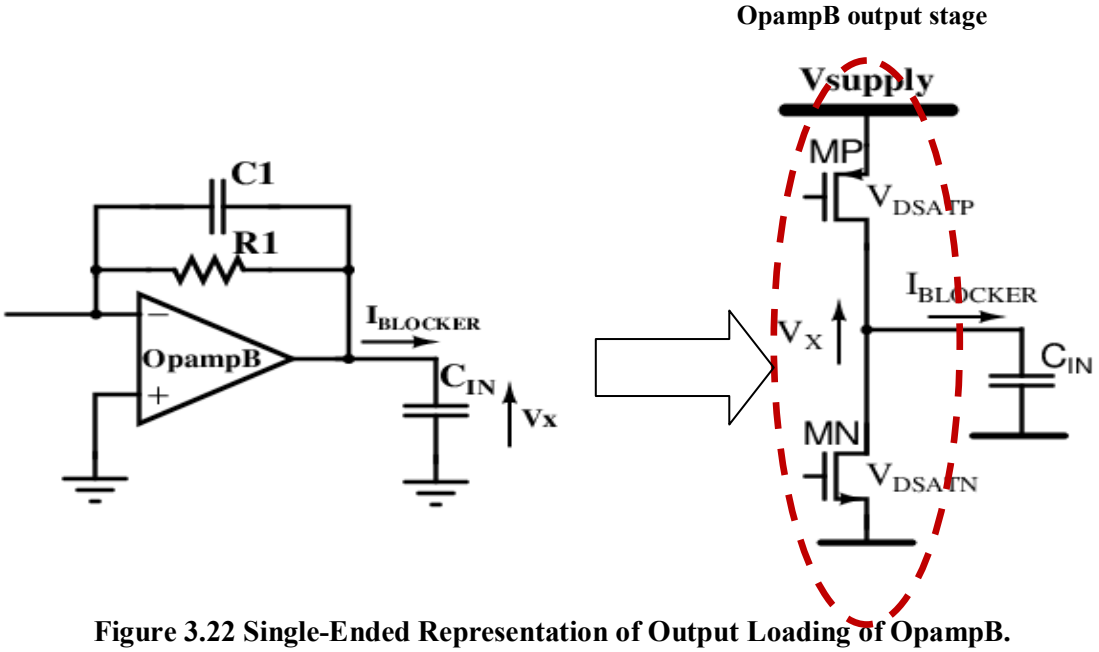


Figure 3.22 Single-Ended Representation of Output Loading of OpampB.

The voltage swing at the output of OpampB when it sources/sinks a full-scale blocker current of 4.5mA at 60MHz can be calculated as:

$$V_x = \frac{I_{BLOCKER}}{\omega C_{IN}} \tag{3.23}$$

where $\omega = 2\pi \times 60 \times 10^6$ *rad/s* and $I_{BLOCKER} = 4.5mA$. If C_{IN} is reduced by half to 26.49pF then $V_x = \pm 460mV$. Since we have a supply voltage of 1.2V, this voltage swing leaves only 280mV across the drain-source of the output transistors. OpampB's output stage will consist of both NMOS and PMOS transistors, MN and MP as shown in Fig. 3.23. This effectively leaves a V_{DS} of 140mV across each device (MN/MP). Large devices

will need to be used to reduce $V_{DSATN/P}$ to below 140mV to ensure the devices stay in saturation, and this will add more parasitic capacitance at the output node, a situation which is undesirable as we already have a large output capacitance which we are trying to reduce to decrease power consumption. Also a $V_{DSATN/P}$ of less than 140mV simply does not provide enough margin across process and temperature. We desire to have a $V_{DSATN/P}$ of at least 200mV to keep MN and MP in saturation across process and temperature during the processing of fullscale blocker currents of 4.5mA. Since we have a supply voltage of 1.2V,

$$V_{x,max} = V_{supply} - V_{DSATN} - |V_{DSATP}| = 1.2V - 200mV - 200mV = \pm 400mV \quad (3.24)$$

From (3.23), for $V_{x,max} = \pm 400mV$, $C_{IN,MIN} \approx 30pF$. From here on, $C_{IN} = 30pF$ is used in the design and this gives 27dB of attenuation at the closest OOB blocker frequency of 60MHz and a plot of the corresponding filter magnitude response is shown in Fig. 3.23. This attenuation value of 27dB translates to ±400mV differential output voltage swing for the TIA for a full-scale blocker current of 4.5mA. With C_{IN} of 30pF the loading on OpampB is approximately 5 times that of OpampA. A 500MHz GBW is targeted for OpampB to minimize its power consumption.

Table 3.3 provides a summary of the TIA filter specifications along with op amp specifications to be used for the transistor level design of the TIA filter. Fig. 3.24 shows the macro-model magnitude plot of the proposed TIA filter AC response obtained using these specifications and compares it to the single-pole TIA filter response.

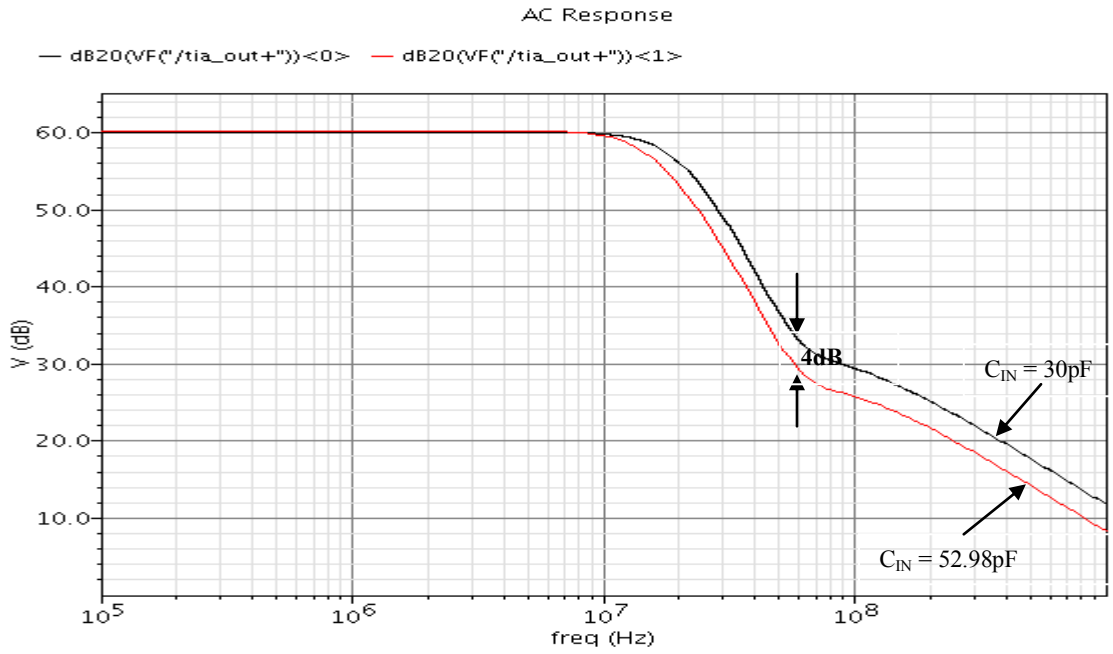


Figure 3.23 Proposed TIA Filter α_{MIN} Reduction for a Change of C_{IN} to 30pF.

Table 3.3 Summary of TIA Transistor Level Design Target Specifications and Op-amp Target Specifications.

Parameter		**Value**	**Unit**
DC Transimpedance Gain		**60**	**dB**
Output Voltage Swing (single-ended)		**±200**	**mV**
Closest OOB Blocker		**±4.5mA at 60MHz**	
Amplifier Target Specifications			
Amplifier	**Gain**	**GBW**	**Loading**
OpampA	**50-60dB**	**1GHz**	**7.2pF||1KΩ**
OpampB	**50-60dB**	**1GHz**	**2.65pF**
OpampC	**50-60dB**	**500MHz**	**30pF||2.65pF||1K Ω**

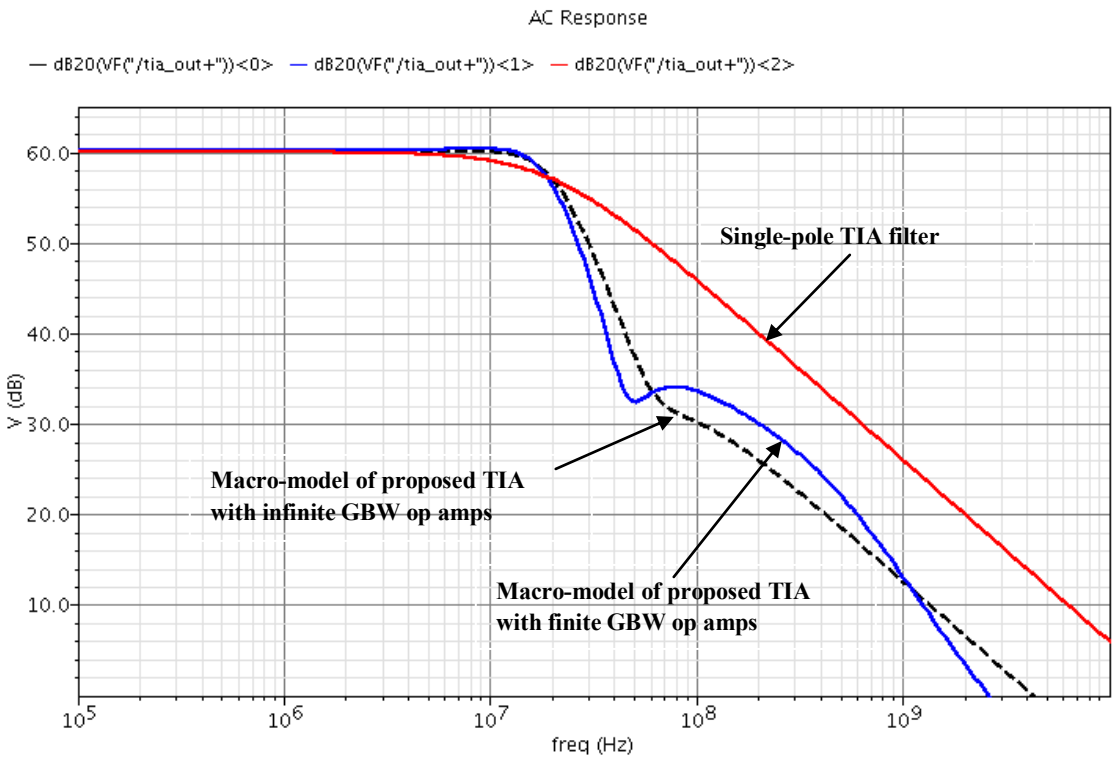


Figure 3.24 Targeted TIA Filter Magnitude Response.

3.5.1 Determination of Amplifier Slew-Rate Specifications

Slew-rate is an important parameter that needs to be considered for processing of high frequency signals by amplifiers. As the frequency of the input current signals to the TIA increases, the voltage at each op-amp output is slew-limited, leading to heavy distortion. For this reason, the op-amps used in the TIA must be designed such that they have enough slewing capability to accommodate the high frequency signals to be processed (60MHz and higher).

For a sinusoidal voltage signal given by :

$$V_O = \hat{V}_{MAX} sin\omega t \tag{3.25}$$

the minimum slew rate of the op amps required to process such a signal is equal to the maximum slope of (3.25) which is given by :

$$\frac{dV_O}{dt}|_{max} = \hat{V}_{MAX}\omega \tag{3.26}$$

As stated before, the full-scale blocker current expected at the TIA inputs is 4.5mA at 60MHz and beyond. The maximum output voltage swing of each of the op-amps occurs for this input blocker magnitude. In Fig. 3.25, the transimpedance gain from the TIA input to each op-amp output is plotted as a function of frequency, which shows a low-pass response. We consider the maximum OOB transimpedance gain at each op-amp output, and multiply this gain by 4.5mA to give the op-amp maximum output voltage swing, $\hat{V}_{MAX}$, for a full-scale blocker magnitude. Noting the frequency at which $\hat{V}_{MAX}$ the maximum at the output of each op-amp occurs, the minimum slew-rate is calculated using (3.26).

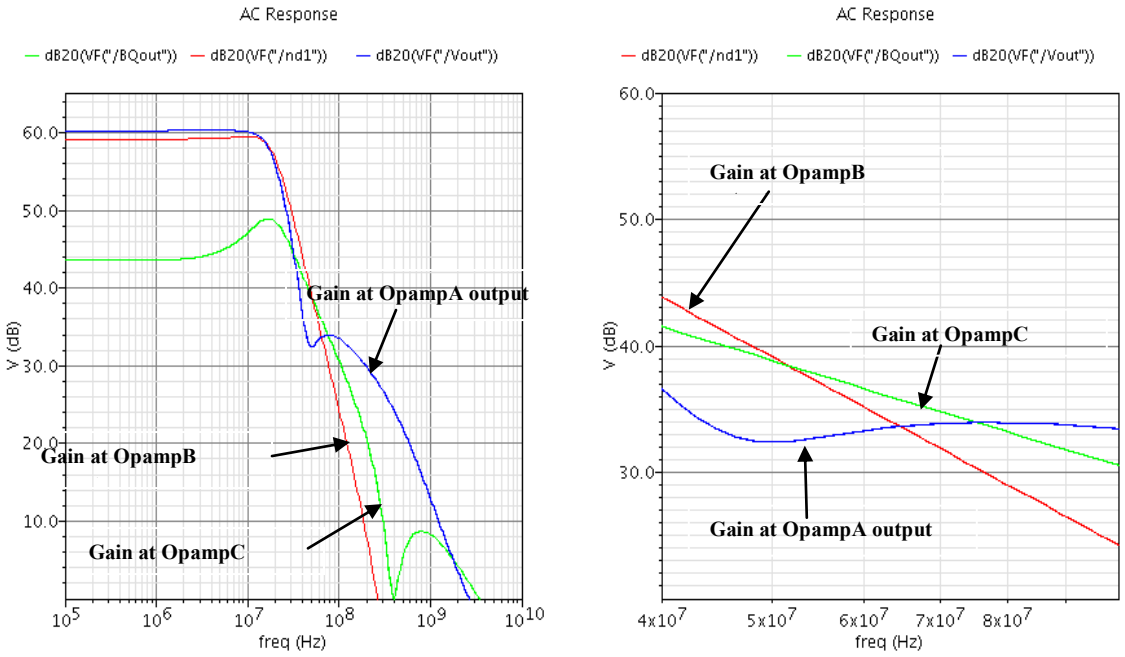


Figure 3.25 Transimpedance Gain from the Proposed TIA Input to Each Op-amp Output.

Table 3.4 shows each amplifier slew-rate specification calculated from (3.26) and Table 3.5 provides a summary of the proposed TIA filter specifications along with op-amp specifications from macro-modeling to be used for the transistor level design of the proposed TIA filter.

Table 3.4 Amplifier Slew-Rate Specifications.

	Maximum output voltage swing (for $I_{BLOCKER}$ =4.5mA)	**Frequency at which maximum output voltage swing occurs**	**SR_{MIN}**
Units	**Mv**	**MHz**	**V/µs**
OpampA	**200**	**85**	**± 107**
OpampB	**400**	**60**	**± 150**
OpampC	**250**	**60**	**± 94**

Table 3.5 Full Summary of TIA Transistor Level Design Specifications and Op-amp Target Specifications.

Parameter		**Value**	**Unit**	
DC Transimpedance Gain		**60**	**dBΩ**	
Maximum Output Voltage swing (single-ended)		**±200**	**mV**	
Closest OOB Blocker			**±4.5mA at 60MHz**	
	Amplifier Target Specifications			
Amplifier	**Gain (dB)**	**GBW (GHz)**	**SR (V/µs)**	**Loading**
OpampA	**50-60**	**1**	**104**	**7.2pF||1KΩ**
OpampB	**50-60**	**1**	**150**	**2.65pF**
OpampC	**50-60**	**0.5**	**94**	**30pF||2.65pF||1K Ω**

4. TRANSISTOR LEVEL DESIGN

Using the specifications obtained in the last section, a transistor level design of the proposed TIA filter is implemented in this section.

4.1 Amplifier Design

We recognize the need for high speed, high gain amplifiers in the design of the TIA as shown by macro-modeling in Table 3.5 from the previous section. Also, we recognize the high OOB blocker current which will need to be sourced/sunk by OpampB. Thus class AB biasing will be employed in the output stage of OpampB so as to maximize its power efficiency. OpampA and OpampC will be implemented with class A output stages since they are not required to provide large load currents.

In [10], a high gain, high bandwidth class A amplifier topology is presented that makes use of feedforward compensation for stability. This obviates the need for large Miller compensation capacitors. The trade-off is that while power consumption is increased area is reduced. OpampA and OpampC employ the architecture in [11] (trade off power for smaller area) while OpampB employs a conventional two-stage Class AB topology with Miller compensation (trades off area for reduced power), thus providing a balance of area and power consumption.

4.1.1 High Gain, High Bandwidth Operational Amplifier - OpampA and OpampC

Table 3.5 in the previous section shows the gain and GBW target specifications for OpampA and OpampC. These op-amps are essentially high gain, high GBW amplifiers. In the design of a high gain and high GBW amplifier, the designer is presented with a fundamental design trade off. While high gain amplifiers require cascode (vertical approach) and/or multi-stage (cascade approach) architectures with long channel devices and low bias currents, high bandwidth amplifiers use single stage architectures, large bias currents and short channel devices. The signal swing in cascode amplifiers is constrained by the power supply voltage which is a problem for low voltage designs, and particularly in this work where a supply of 1.2V is used. In cascaded amplifiers which

are the alternate option for high gain, each amplifier stage contributes a pole and Miller compensation schemes are required for stability. These schemes however, are based on the fundamental principle of creating a dominant pole with 20dB/decade roll-off to the unity gain frequency, trading off bandwidth for stability.

To achieve high gain without sacrificing bandwidth, a two-stage op amp with a feedforward compensation scheme which does not use Miller capacitors is used [10]. This feedforward compensation technique is known as no-capacitor feedforward (NCFF) compensation. The technique uses the positive phase shift of left-half-plane (LHP) zeros caused by a feedforward path to cancel the negative phase shift of poles to achieve a good phase margin. A two-stage (cascade) design gives high, low-frequency gain and the feedforward stage makes the circuit faster. The amplifier bandwidth is not compromised due to the absence of the traditional pole-splitting effect of Miller compensation, resulting in a high-gain, wide-band (large GBW) amplifier with a fast step response. However, in practical circuits the pole-zero cancellation may not be exact and this leads to the formation of pole-zero pairs (doublets) which may degrade the settling time of the amplifier. In this work, the settling time requirement is not critical since we are dealing with a continuous-time filter.

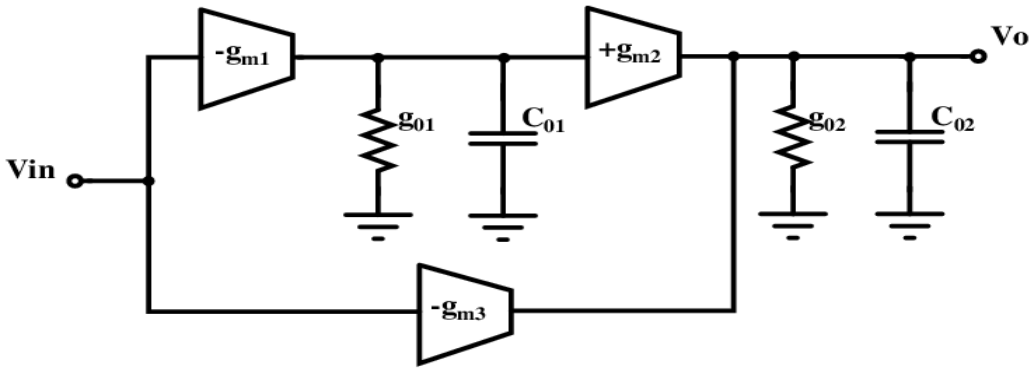


Figure 4.1 Block Diagram of a Two-Stage Amplifier with No-Capacitor Feed-Forward (NCFF) Compensation.

The block diagram of the feedforward compensation scheme is shown in Fig. 4.1. A_{V1}, A_{V2} and A_{V3} define the dc gains of the first, second and feedforward stages of the amplifier. The first stage pole is located at $\omega_{p1} = (go1/C_{01})$ and the second and feedforward stages have a common pole at $\omega_{p2} = (go2/C_{02})$. The overall amplifier voltage gain is given by :

$$A_{VT}(s) = \frac{-(A_{V1}A_{V2} + A_{V3})\left(1 + \frac{A_{V3}s}{(A_{V1}A_{V2} + A_{V3})\omega_{p1}}\right)}{\left(1 + {}^{s}/_{\omega_{p1}}\right)\left(1 + {}^{s}/_{\omega_{p2}}\right)} \tag{4.1}$$

which has two poles and a LHP zero created by the feedforward path. The DC gain is given by:

$$A_{VTO} = A_{V1}A_{V2} + A_{V3} \tag{4.2}$$

and the dominant pole is located at ω_{p1}. The location of the LHP zero is :

$$\omega_z = -\omega_{p1}\left(1 + \frac{A_{V1}A_{V3}}{A_{v2}}\right) \cong -\frac{g_{m1}}{C_{01}}\frac{g_{m2}}{g_{m3}} \tag{4.3}$$

The second and feedforward stages are designed such that the negative phase shift due to ω_{p2} is compensated by the positive phase shift of ω_z.

4.1.2 High Gain, High Bandwidth Operational Amplifier Design Procedure

The design procedure of the two-stage NCFF amplifier is discussed next. The design equations, which form the basis for the design procedure, are given as follows:

$$GBW = A_{VT}\omega_{p1} \tag{4.4}$$

$$A_{V1} = g_{m1}r_{01} \tag{4.5}$$

$$A_{V2} = g_{m2}r_{02} \tag{4.6}$$

$$A_{V3} = g_{m3}r_{02} \tag{4.7}$$

$$\omega_{p1} = \frac{1}{r_{01}C_{01}} \tag{4.8}$$

$$\omega_{p2} = \frac{1}{r_{02}C_{02}} \tag{4.9}$$

$$\omega_Z = -\frac{g_{m1}}{C_{01}}\left(\frac{g_{m2}}{g_{m3}}\right) \tag{4.10}$$

i) The GBW specification for both OpampA and OpampC is 1GHz. A DC gain, A_{VT0} of 50-60dB is also targeted. The dominant pole frequency, ω_{p1}, is determined from (4.3). Given ω_{p1}, C_{01} is determined using (4.7) based on the process technology values of r_{01} which is the effective parasitic resistance lumped at the output of the first stage.

ii) The first gain stage is required to be a high gain stage. The gains of the first and second stages are apportioned as : A_{V1} = 40dB and A_{V2} = 10dB. From (4.5) and (4.6), g_{m1} and g_{m2} are determined.

iii) C_{02} is equal to the output load capacitor C_{LOAD} (C_{LOAD} is 7.2pF for OpampA and 2.65pF for OpampC). With g_{m1}, g_{m2}, C_{01} and C_{02} known, g_{m3} is determined by equating the zero frequency, ω_Z to the second stage pole frequency, ω_{p2} .Thus (4.9) is equated to (4.10) to obtain g_{m3} .

iv) For the amplifiers in this work, the load capacitor C_{LOAD} is larger than the capacitance at the output of the first stage, C_{01} . Since the second stage is implemented as a differential pair with a tail current, it is the slew limiting stage of the amplifier. Hence from the slew rate specification of the amplifiers, the minimum bias current of the second stage is determined as follows :

$$I_{B2} \geq g_{m2} \times C_{LOAD} \tag{4.11}$$

where I_{B2} is the tail current source of the second stage input differential pair.

4.1.3 High Gain, High GBW Operational Amplifier Circuit Implementation

The two-stage amplifier using the NCFF compensation has the following design considerations :

i) The second and feedforward stages should not have any non-dominant pole before the overall unity gain frequency of the amplifier [10].

ii) The pole–zero cancellation should occur at high frequencies for best settling-time performance [10].

The above design considerations can be met by designing the first stage to have a high gain. The second and feedforward stages are designed to have optimum bandwidth and medium gain. The options that readily come to mind for the first stage are the folded-cascode and the telescopic amplifiers [8cc]. Though the telescopic amplifier is a better option when considering speed and current efficiency for the same trans-conductance of the first stage differential pair, the folded-cascode topology is used for the first stage design owing to its lower headroom requirement which will allow more swing at its output. The headroom requirement of the folded-cascode is a $V_{DSATN,P}$ lower than that of the telescopic amplifier. In the second and feedforward stages, simple differential pairs with active loads are used for medium gain and large bandwidth. The schematic implementation of this amplifier is shown in Fig. 4.2.

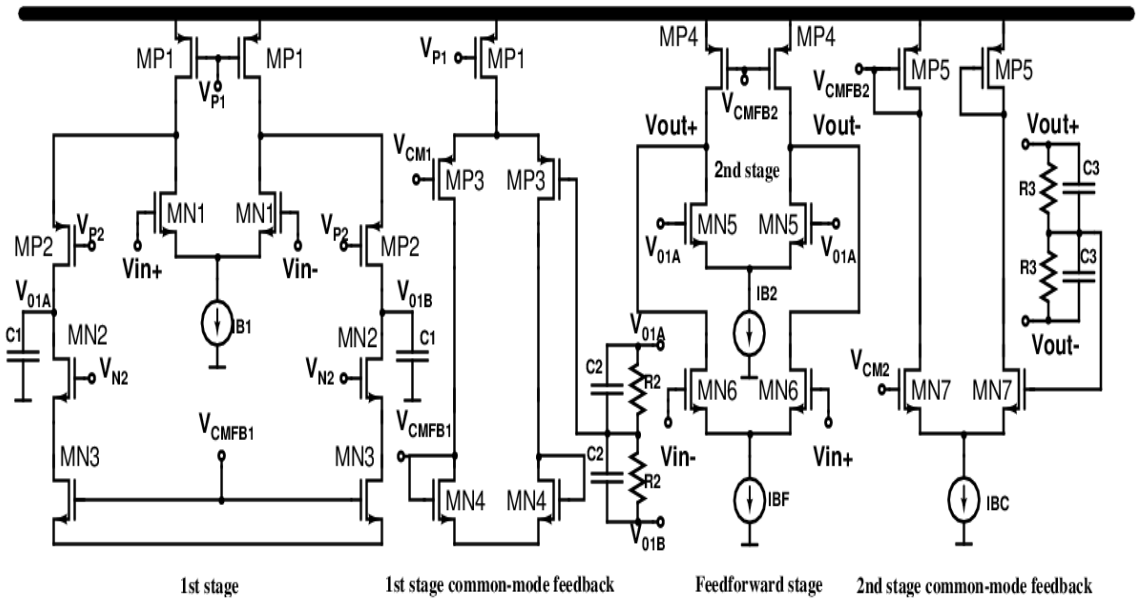


Figure 4.2 Schematic of Two-Stage Amplifier Using NCFF Compensation.

The first stage (MN1, MP1) of the amplifier is designed to have a high gain and a dominant pole at its output which also creates a dominant pole for the 1st stage common-mode feedback circuit (MN4,MP3) which is required for stability of the common-mode feedback loop. Since the second stage (MN5, MP4) and feed-forward stage (MN6) are optimized for high bandwidth and medium gain performance, the transconductances of the second and feed-forward stages are made as large as possible to push poles to higher frequencies.

Common-mode feedback is required for both the first and second amplifier stages. The common-mode feedback circuit for the first stage is formed by (MN4, MP3) while the common-mode feedback circuit for the second stage is formed by (MN7, MP5). The common-mode level is kept at 600mV for maximum swing at the output of the second stage by the reference voltage source V_{CM2}. The first stage output common-mode level is 650mV and this is set by the reference voltage V_{CM1}. The common-mode levels at both the outputs of the first stage and second stage are detected using resistive-averaging. The stability of the two common-mode loops is enhanced by adding small capacitors C2 and C3 which introduce LHP zeros in the two common-mode feedback paths. Large signal swings are expected at the output stages of the amplifiers in the implementation of the TIA filter. Hence the second stage output transistors are sized to have low V_{DSAT} to accommodate the high signal swings. Also, most of the gain of the amplifier comes from the first stage (≈40dB) and thus the swing at the output of this stage will be significant during maximum amplifier output swing. Therefore, MN1, MN2, MN3, MN5, MN6, MP1, MP2 and MP4 are all sized to have low V_{DSAT}. Table 4.1 shows the transistor dimensions, device values and bias currents used in the design of OpampA and OpampC.

Table 4.1 Transistor Dimensions, Device Values and Bias Conditions for OpampA and OpampC.

Device	Dimensions		Device	Value	
	OpampA	OpampC		OpampA	OpampC
MN1	160µ/600n	160µ/600n	IB1	800µA	800uA
MN2	320µ/1µ	320µ/1µ	IB2	1.5mA	1.5mA
MN3	80µ/1µ	80µ/1µ	IBF	6.5mA	6.5mA
MN4	80µ/1µ	80µ/1µ	IBC	9.2mA	9.2mA
MN5	200µ/600n	200µ/600n	V_{P2}	600mV	600mV
MN6	2m/1µ	1m/1µ	V_{N2}	500mV	500mV
MN7	400µ/1µ	400µ/1µ	C1	2pF	2Pf
MP1	480µ/1µ	480µ/1µ	C2	100fF	100fF
MP2	320µ/1µ	320µ/1µ	R2	100KΩ	100KΩ
MP3	160µ/1µ	160µ/1µ	R3	200KΩ	100KΩ
MP4	960µ/1µ	960µ/1µ	C3	100fF	100fF
MP5	960µ/1µ	960µ/1µ			

4.1.4 Class AB Amplifer Design

A class AB amplifier is employed in the design of OpampB. The topology used is a simple PMOS differential pair input stage, the schematic of which is shown in Fig.4.3, and a class AB output stage. Miller compensation is employed for stability. A common source configuration is chosen for the class AB output stage to provide gain.

For a two-stage Miller compensated op-amp, the GBW is given by:

$$GBW = \frac{G_m}{C_C} \tag{4.12}$$

where G_m is the transconductance of the input stage and Cc is the Miller compensation capacitance required for stability. Also, to meet the slew rate specification for OpampB, the input stage bias current is chosen such that:

$$I_{BIAS} \geq SR \times C_C \tag{4.13}$$

A conventional Monticelli class AB bias circuit is used for the class AB output stage. A class AB output stage architecture provides improved efficiency over a class A output stage for sourcing/sinking large load currents. OpampB is required to source and sink the fullscale OOB blocker current of 4.5mA. Using a class A stage shown in Fig. 4.4(a), this means the output transistor MN must be permanently biased with at least 4.5mA of current.

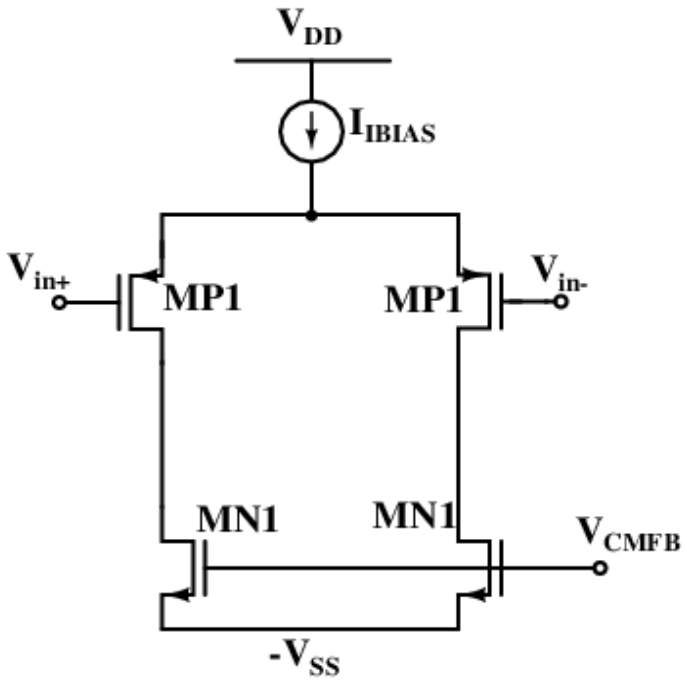


Figure 4.3 Simple PMOS Differential Pair Input Stage.

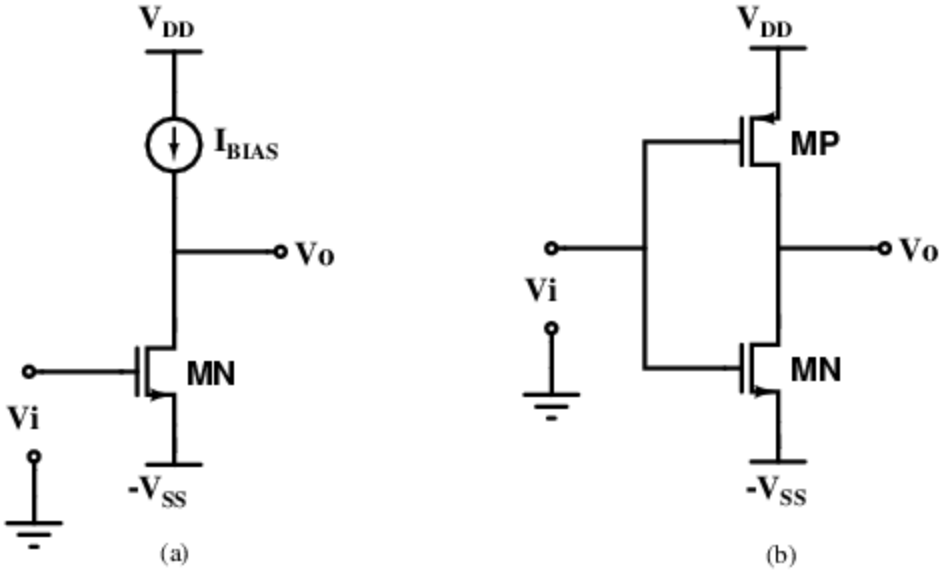


Figure 4.4 (a) A Class A Common-Source Output Stage. (b) A Class B Common-Source Output Stage.

The power conversion efficiency of a power amplifier is defined as the ratio of the power delivered to the load to the average power drawn from the supplies. For a class A stage as in Fig. 4.4(a), the power efficiency is given by [11]:

$$\eta_C = \frac{1}{4}\left(1 - \frac{V_{DSATN}}{V_{DD}}\right) \tag{4.14}$$

In (4.14), V_{DSATN} is the drain-source saturation voltage of the class A output device, MN. Clearly we see that if $V_{DSATN} << V_{DD}$, then the power efficiency of the class A stage approaches 25%.

An output stage that has improved efficiency over the class A architecture is the class B output stage shown in Fig. 4.4(b). This output stage alleviates the low efficiency of the class A output stage by having essentially zero power dissipation with zero input current. Two active devices, MN and MP are used to deliver the output load instead of one as in the class A stage. MN and MP conduct for alternate half-cycles of the input voltage signal V_i . When the input signal becomes positive, MN conducts and when it is negative

MP conducts. Assuming a sinusoidal input signal, the power conversion efficiency of this stage is given by [11]:

$$\eta_C = \frac{1}{4} \hat{V}_O \Big/ V_{DD} \tag{4.15}$$

where, $\hat{V}_O V$ is the zero-to-peak amplitude of the output sinusoidal voltage. The maximum power efficiency approaches 78.6% for rail-to-rail output voltage operation [11]. However there is a deadband as shown by Fig. 4. 5. At zero input signal $V_i = 0$, both devices are off. As V_i becomes positive, the output voltage is still zero until V_i becomes equal to the threshold voltage of MN given by V_{TN}. For $V_i \geq V_{TN}$, MN conducts and produces an output. The same happens when V_i starts becoming negative. This deadband causes cross-over distortion in the output signal V_o. The effect of this distortion becomes reduced as the input signal becomes larger since the deadband increasingly represents a smaller fraction of the magnitude of the signal. Thus class B output stages have very high distortion at low signal levels.

A way to prevent this distortion is to keep both MN and MP conducting a small quiescent current even when there is no input signal to this stage. This eliminates cross-over distortion. Such an output stage is known as the class AB output stage. The class AB output stage is shown in Fig. 4.6.

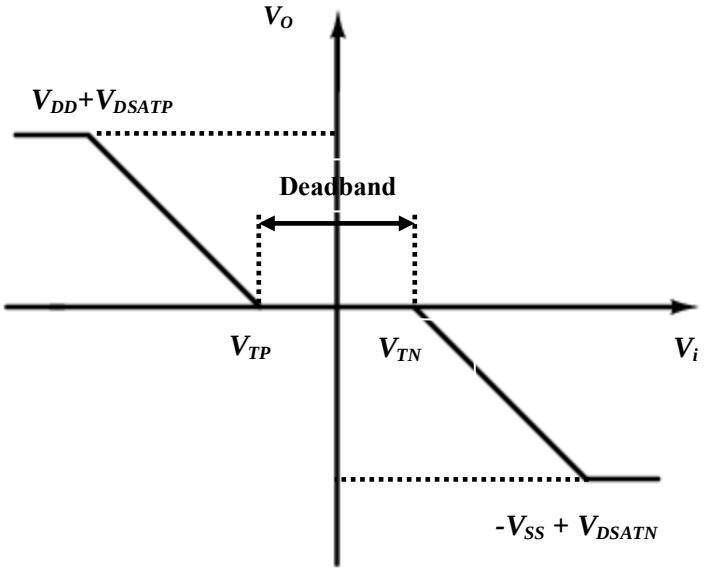


Figure 4.5 Class B Output Characteristic Plot.

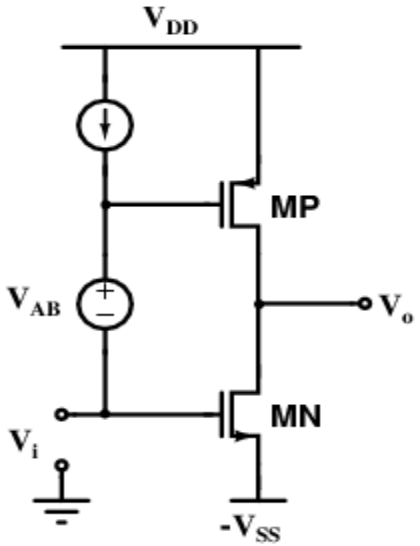


Figure 4.6 The Class AB Output Stage [11].

To set the quiescent current in Fig. 4.6, the sum of the gate-to-source voltages of MN and MP can be controlled in such a way that it is equal to the sum of a reference NMOS

gate-source voltage, $V_{GS,N}$ and a PMOS gate-source voltage $V_{GS,P}$, and this is obtained by setting V_{AB} as follows :

$$V_{AB} = V_{DD} + V_{SS} - V_{GS,N} - |V_{GS,P}| \quad (4.16)$$

Sufficient quiescent current is required in the output stage to ensure a smooth switch-over from one transistor to the next, thus avoiding cross-over distortion because the output transistors are switched on and off gradually. The output current drive of the class AB stage is essentially limited by the supply voltage. This is because high output currents require large transistor gate-to-source voltages and (4.16) provides the limiting equation.

Fig. 4.7 shows the implementation of the class AB output stage. The output devices MN and MP are replaced by MN5 and MP5. The voltage source V_{AB} is implemented using two complementary head-to-tail connected transistors MP4 and MN4 along with biasing transistors MP2,MP3,MN2,MN3. The biasing of MP5 and MN5 is controlled by two trans-linear loops formed by MP5, MP4, MP2, MP3 and MN5, MN4, MN2, MN3, which fix a well-defined quiescent current. MP4 and MN4 are designed to have equal transconductance in the quiescent state.

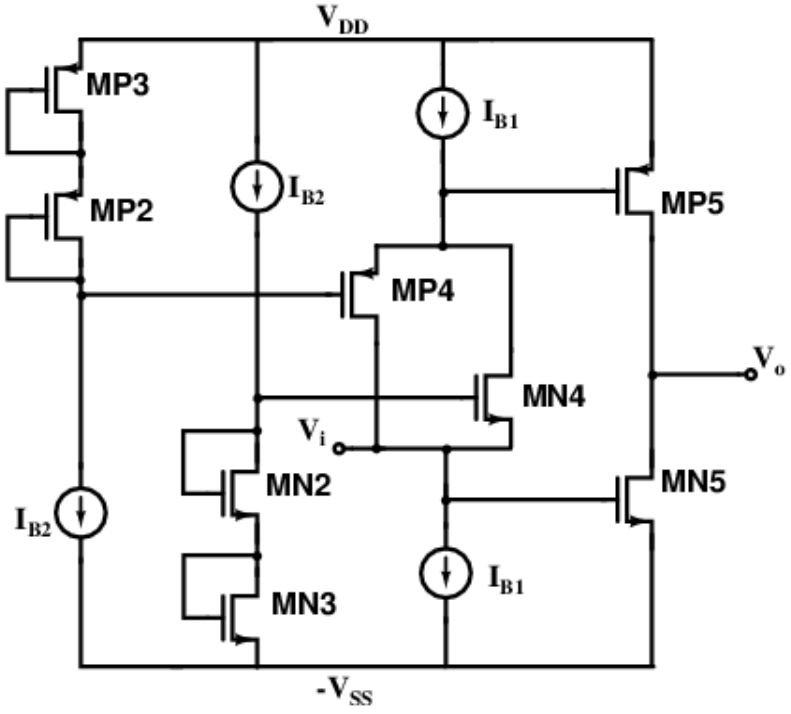


Figure 4.7 Monticelli Class AB Output Stage.

In the quiescent state of operation, MN4 and MP4 are both on and present a low impedance to the gates of MP5 and MN5. For large overdrive of MN5 (MP5), MN4 (MP4) turns off and MP4 (MN4) acts as a cascade transistor. This presents a large impedance to the gates of MP5 and MN5 and this serves to clamp the gate-source voltage of the weakly conducting transistor MP5 (MN5), thus leaving a minimum current flowing through it and preventing cut-off.

Miller compensation is used to compensate OpampB, the schematic of which is shown in Fig. 4.8. Since OpampB is pseudo-differential, there are two class AB output stages, one for each differential output. A common-mode feedback circuit, the same topology used for the input stage of OpampA and Opamp C, is used to fix the common-mode output voltage of OpampB at 600mV. The common-mode output voltage of the class AB stage is detected using a resistive detector, and the common-mode feedback control voltage is fed to MN1. The dominant pole at the output of the class AB stage serves as

the dominant pole of the common-mode feedback circuit and ensures stability of the common-mode feedback loop.

Table 4.2 gives transistor dimensions, device values and bias currents used in the design of OpampB. Finally, Table 4.3 provides a summary of the performance parameters of OpampA, OpamB and OpampC.

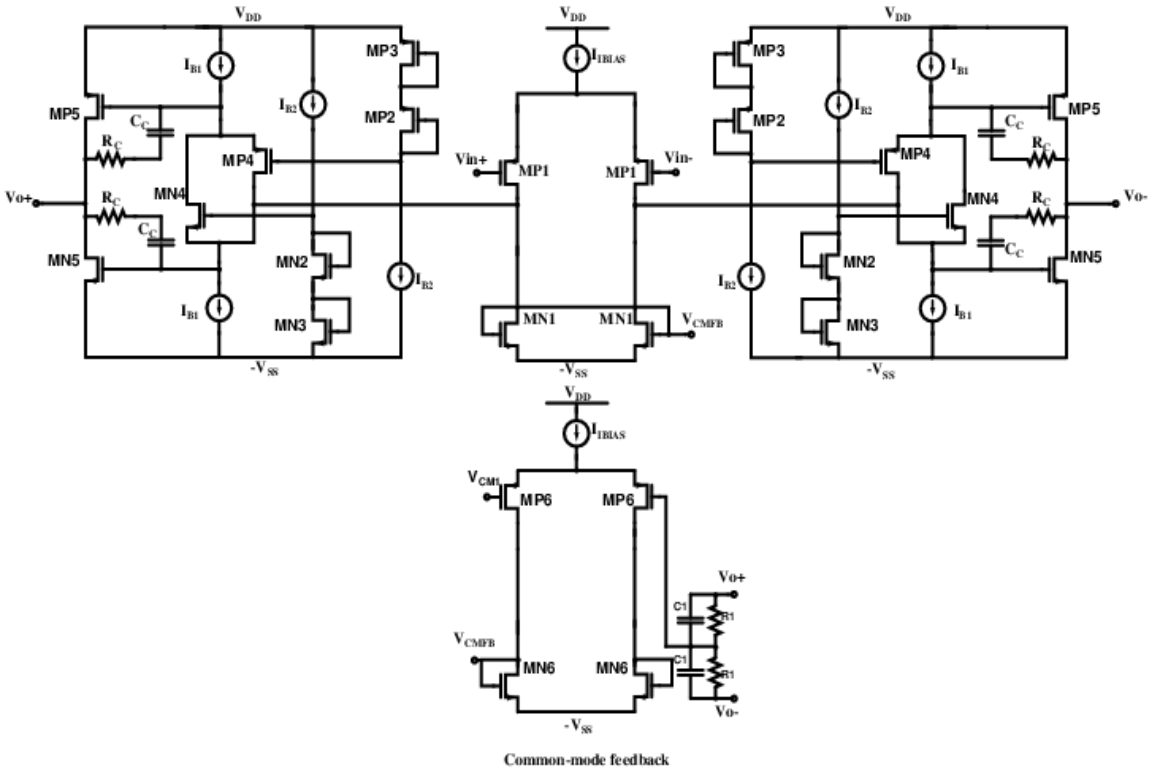


Figure 4.8 Schematic of Miller-Compensated Two-Stage Op-amp with Class AB Output Stage.

Table 4.2 Transistor Dimensions, Device Values and Bias Conditions for OpampB.

Device	Dimension	Device	Value
MN1	**160µ/600n**	**IB1**	**800µA**
MN2	**320µ/1µ**	**IB2**	**1.5mA**
MN3	**80µ/1µ**	**IBF**	**6.5mA**
MN4	**80µ/1µ**	**IBC**	**9.2mA**
MN5	**200µ/600n**	**V_{P2}**	**600mV**
MN6	**4m/900n**	**V_{N2}**	**500mV**
MP1	**400µ/1µ**	**C1**	**2pF**
MP2	**480µ/1µ**	**C2**	**100fF**
MP3	**320µ/1µ**	**R2**	**100KΩ**
MP4	**160µ/1µ**	**R3**	**20KΩ**
MP5	**900µ/1.2**	**C3**	**1pF**
MP6	**1m/1µ**		

Table 4.3 Summary of Amplifier Performance Parameters.

	DC Gain (dB)	GBW (Hz)	PM(°)	SR (V/µs)
OpampA	51.8	1.5G	58.5	**80**
OpampB	48	300M	40	**100**
OpampC	56.4	2.48G	46	**100**

4.1.5 Full Transistor Implementation of TIA Filter

The amplifiers designed in the previous section are used in the design of the proposed TIA filter. Fig. 4.9 provides a top-level view of the transistor level implementation that is designed and simulated. A shunt capacitor, C_X of 110pF is placed across the inputs of

the TIA filter to provide more OOB attenuation at very high frequencies where the op-amp gains have dropped significantly.

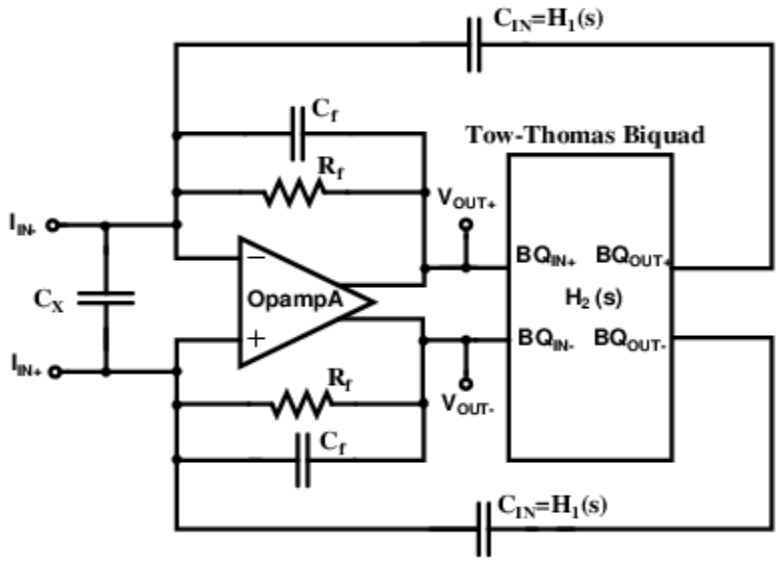


Figure 4.9 (a) Top Level TIA Filter Transistor Implementation

4.1.6 Layout of Proposed TIA Filter

The layout of the TIA filter is provided in Fig. 4.10. Since the TIA is fully-differential, careful matching of differential halves of the op-amps is ensured to minimize mismatch which would otherwise degrade the common-mode rejection performance of the TIA filter. Mismatch in the differential halves of the TIA also causes distortion of the output voltage signal waveform from the TIA. Thus the transistors forming the differential halves are matched using inter-digitated and common-centroid techniques. It is ensured that dummy transistors are not connected to signal nodes as this will increase the parasitic capacitances at these nodes and can degrade the speed and high frequency performance of the TIA amplifiers and hence the TIA filter as a whole. Also, capacitors and resistors on the differential halves are matched.

For the Tow-Thomas biquad, capacitors and resistors in the biquad form the coefficients of the second order transfer function. The ratios of these capacitors and resistors are critical in ensuring that the biquad transfer function is not altered. The three capacitors in the biquad (counting each differential half) C_1, C_2 and C_3 have the same value and are matched using common-centroid techniques. R_1, R_2 ,R_3, R_4, and R_5 are matched using interdigitated techniques.

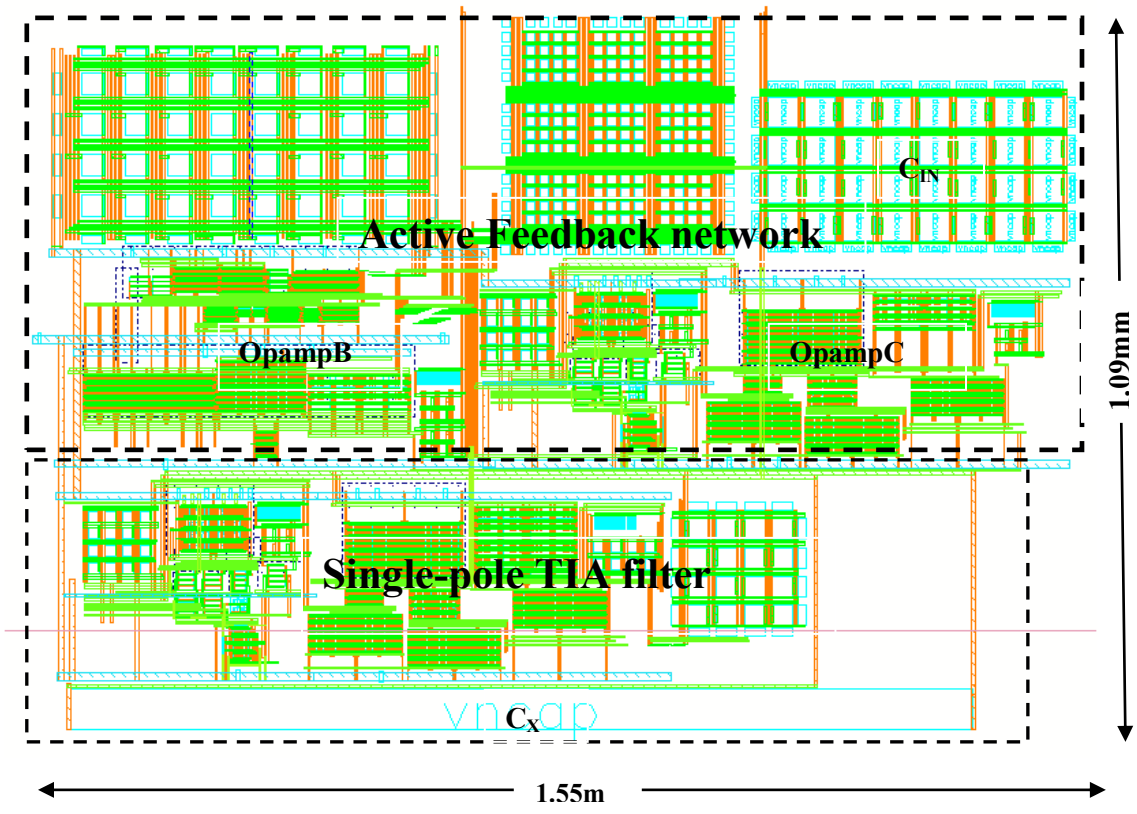


Figure 4.10 Layout of the Proposed TIA Filter.

5. SIMULATION RESULTS

The proposed TIA filter is designed and simulated in IBM 90nm CMOS technology. In this section the simulation results of the proposed filter are presented and compared with those of the conventional single-pole TIA filter. Schematic level plots are presented first and post-layout simulation results are presented after. Owing to parasitic capacitors and resistors, the schematic level plots differ slightly from the post-layout simulation plots.

5.1 Schematic Simulation Results

Both the small-signal performance parameters and the large-signal parameters of the proposed filter schematic level implementation are characterized and plotted in this section. Simulation plots of the conventional single-pole filter are provided for comparison. Also, simulation plots of the proposed TIA filter transfer function are provided as a reference in some of the plots to show how closely the transistor level design follows from the theoretical derivations of Section 3.

5.1.1 Schematic Level Small-Signal Characterization

In Fig. 5.1 the schematic level magnitude response of the proposed TIA filter is presented and compared with that of the single-pole TIA filter. The ideal transfer function of the proposed TIA is also shown. We observe the vast improvement in OOB attenuation at frequencies as close as 48MHz and higher. At 60MHz, which is our closest OOB frequency of interest, the proposed filter schematic level plot provides 27.5dB attenuation which is 22.5dB more than what the single-pole filter can offer. This means that the proposed filter should be able to handle an OOB blocker level of 4.74mA at 60MHz before the output voltage swing of the filter reaches its maximum value of ±200mV single-ended. This value is 240uA more than the 4.5mA value which was targeted during macro-modeling. However, the TIA was designed for a blocker level of

4.5mA at 60MHz and higher and its op-amps will be slew-limited for interferer levels greater than 4.5mA, thus distortion figures are expected to be high for interferer levels of 4.74mA. Also, increasing the blocker robustness of this TIA to 4.74mA may cause the output transistors of the class AB output stage to move into triode region of operation across process and temperature. The bandwidth of the TIA schematic simulation is 24MHz. It is expected that parasitic capacitors in the layout will reduce the bandwidth back to 20MHz. The improvement in attenuation at 200MHz and higher for the proposed filter schematic implementation over its ideal transfer function is as a result of C_X placed across the input terminals of the proposed TIA.

In Fig. 5.2, the input impedance of the proposed TIA filter is plotted. The proposed filter shows a 26.7 Ω peak input impedance at 20MHz which is greater than the peak input impedance of 25 Ω of the single-pole filter which occurs at 65MHz. As noted through this work, the input impedance of the TIA filter needs to be low to preserve mixer linearity across both in-band signal and OOB blocker frequencies. However, the critical frequencies are 60MHz (closest OOB frequency) and beyond where large blocker magnitudes of 4.5mA are expected. At 60MHz, the proposed filter provides 3.5Ω input impedance and this rises until it peaks at 7 Ω at 190MHz. Beyond 190MHz, the input impedance drops off until it ultimately falls to 0 Ω at 10GHz and beyond. Thus the proposed filter enhances mixer linearity much better than the single-pole filter.

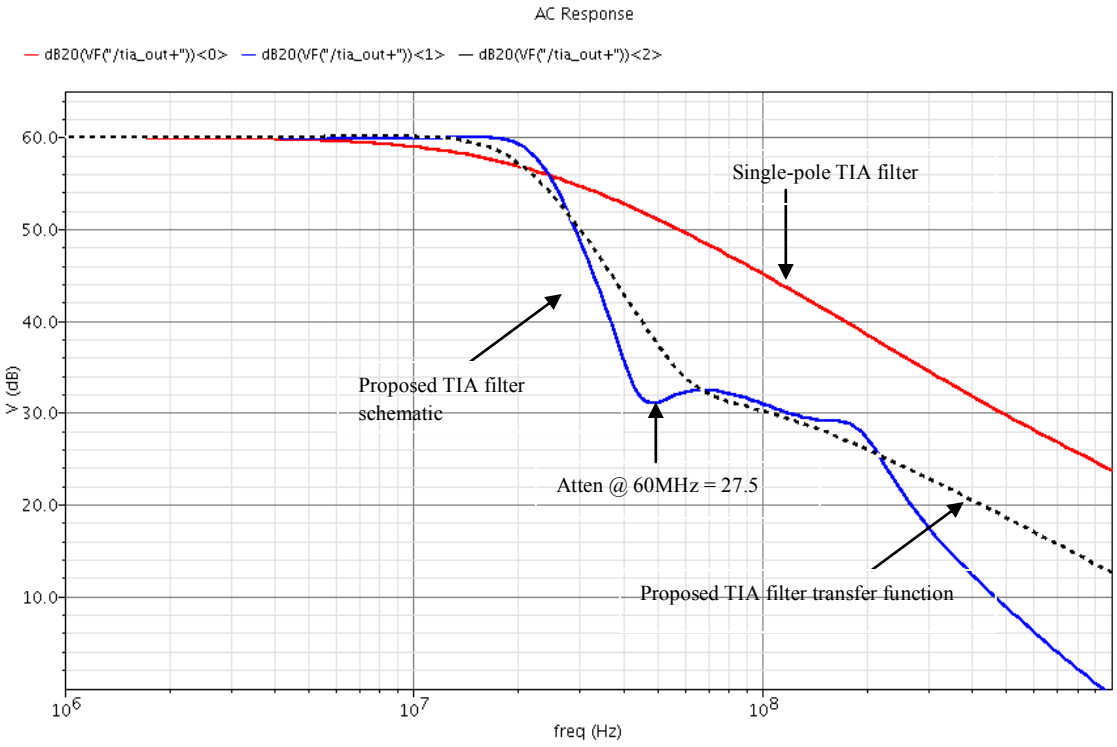


Figure 5.1 Schematic Level AC Magnitude Response of the Proposed TIA Filter.

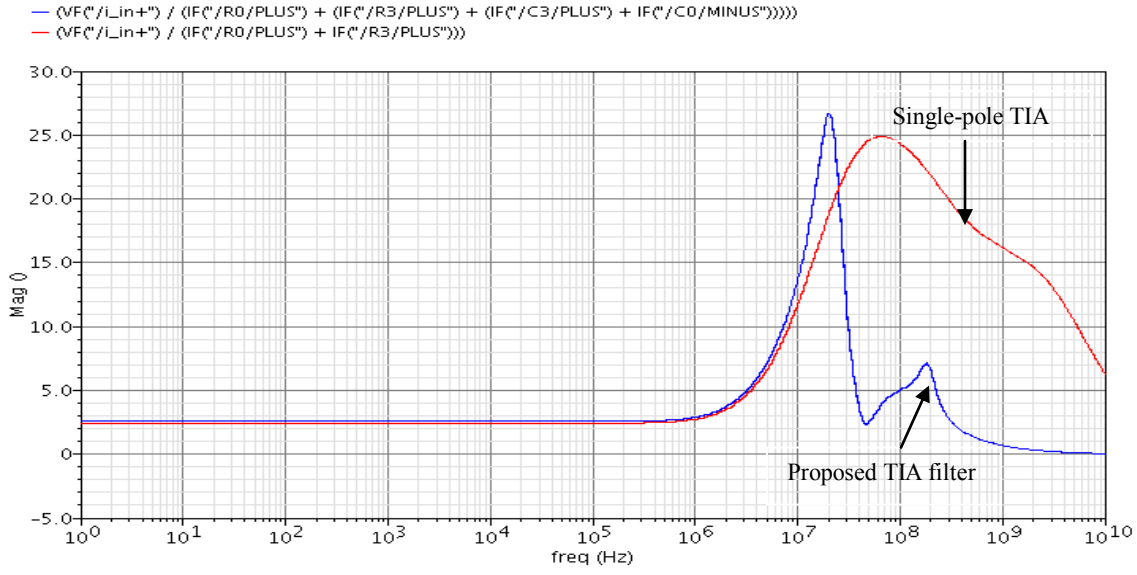


Figure 5.2 Schematic Level Small-Signal Input Impedance.

Fig. 5.3 shows the group delay variation of the proposed filter and that of the single-pole filter. As noted in earlier sections, minimizing group delay variation within the bandwidth of the filter is important for keeping distortion of the in-band signals, which arises from non-linear phase, as low as possible. The group delay plot of the ideal filter transfer function is also provided. As expected the group delay variation of the proposed filter is greater than that of the single-pole TIA.

Noise performance of the proposed TIA is shown and compared with that of the single-pole TIA in Fig. 5.4. Flicker noise performance of the proposed TIA filter is comparable to that achieved using the conventional single-pole TIA. As the frequency increases the small-signal noise performance of the proposed TIA filter increases. However, only the in-band noise performance of the TIA filter is critical to obtain a good signal-to-noise ratio for the TIA since the in-band signal is typically small-signal and in the microamp range. Table 5.1 provides the noise summary of the proposed TIA filter and the conventional single-pole TIA.

Table 5.1 TIA Input-Referred Integrated Noise Current.

	Units	Single-pole TIA filter	Proposed TIA filter
Input integrated noise current (1Hz – 20MHz)	nA	34	213

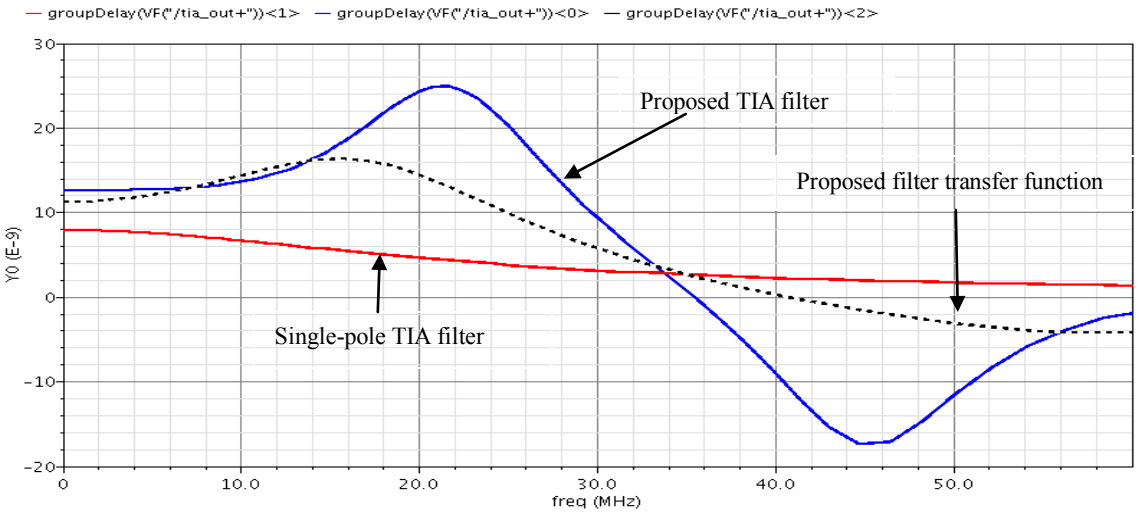


Figure 5.3 Schematic Level In-Band Group Delay Variation.

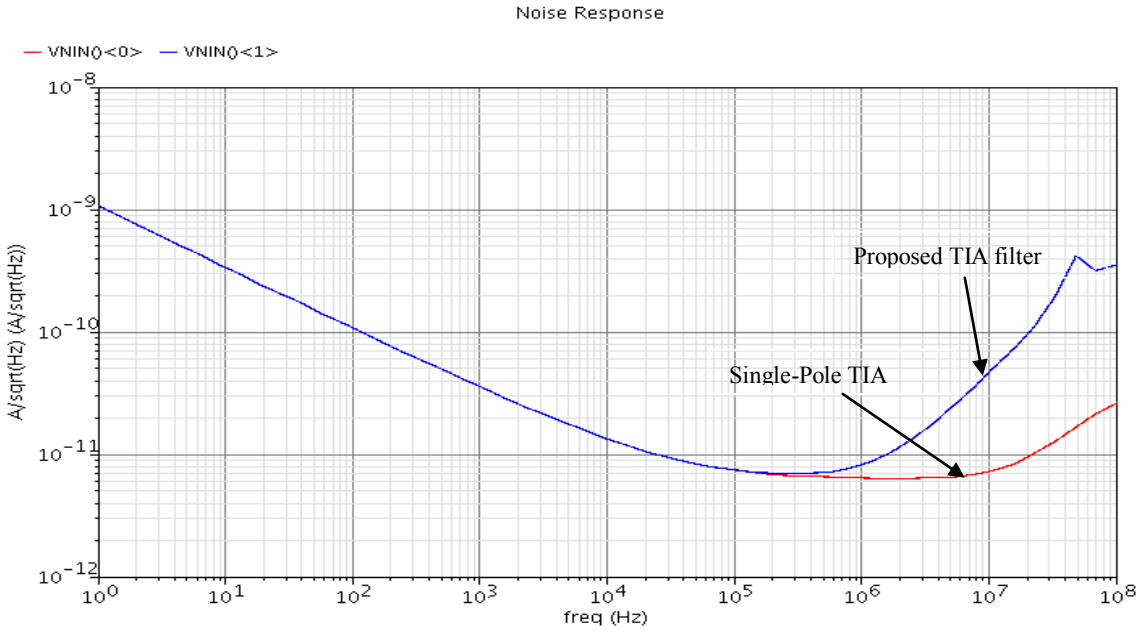


Figure 5.4 Schematic Level Input-Referred Noise Current Density.

5.1.2 Schematic Level Large-Signal Characterization

In Fig. 5.5 the transient response of the filter to a 4.5mA OOB blocker at 60MHz is shown. A settling time of 120ns is observed for the proposed TIA filter. The transient response of the proposed TIA filter is shown next for an in-band signal magnitude of 10uA at 10MHz in the presence of a large blocking signal of 4.5mA at 60MHz in Fig. 5.6.

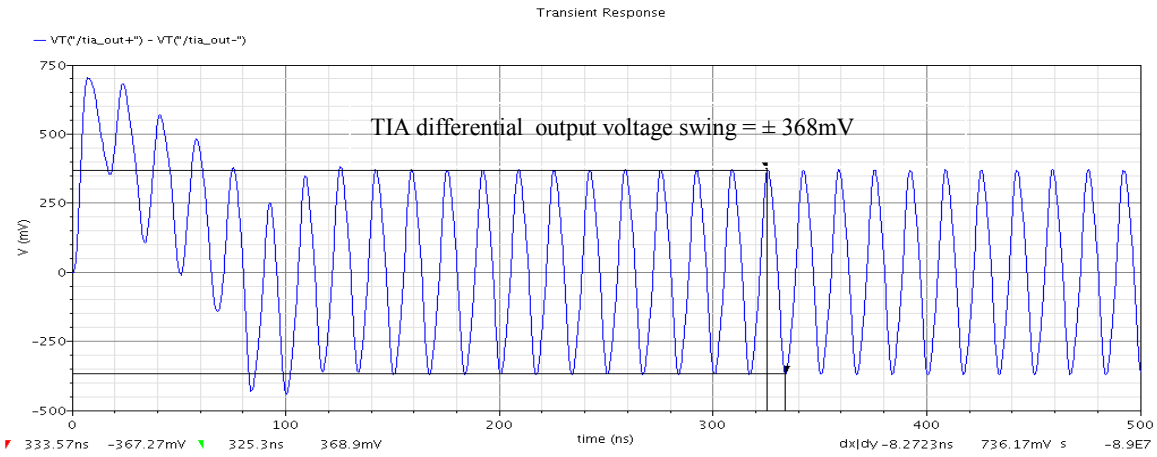


Figure 5.5 Schematic Transient Response of Proposed TIA Filter to OOB Blocker of 4.5mA at 60MHz.

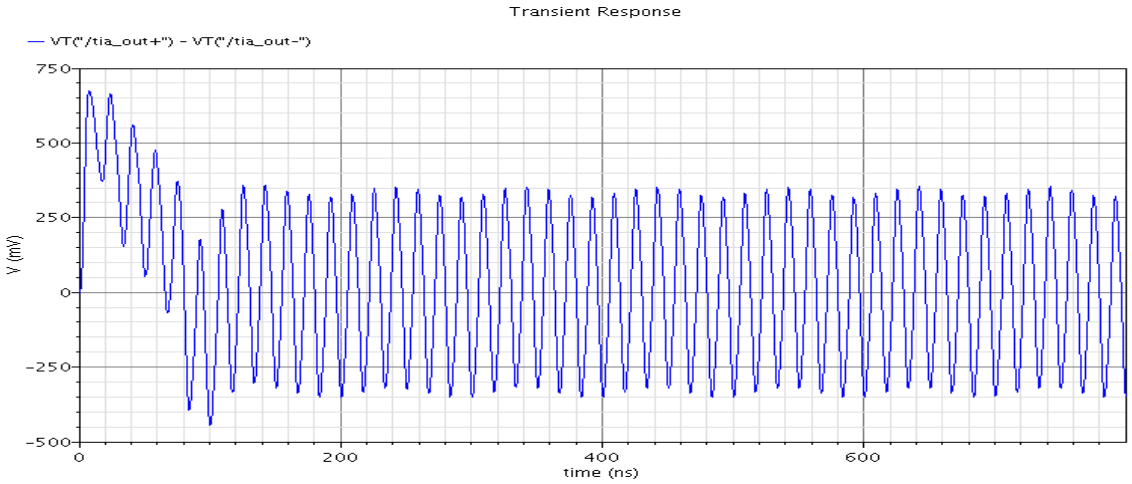


Figure 5.6 Schematic Transient Response of Proposed TIA Filter to an In-band Signal of 10µA at 10MHz in the Presence of an OOB Blocker of 4.5mA at 60MHz.

Next we look at the ability of the proposed TIA filter to withstand in-band signal distortion due to gain compression arising from large close-in OOB blocker current signals as is the case of multi-radio platforms where multiple-radios operate simultaneously. Owing to the phenomenon of gain compression [7], when both the weak in-band signal and large OOB blocker currents are processed by the TIA filter, there is the risk of transfer of modulation (noise) on the amplitude of the blockers onto the small in-band signal and this is known as cross-modulation [6]. Cross-modulation distorts the in-band signal and thus degrades the linearity of the RF receiver chain. Also, gain compression arising from large blockers can cause desensitization of the TIA and if these blockers are large enough, complete blocking of in-band small signals may occur (however this is theoretical and does not occur in practice because the TIA output will saturate first). Gain compression is typically characterized by the 1dB compression point, which measures the magnitude of the input signal that causes the small-signal gain of the TIA to drop by 1dB.

Fig. 5.7 plots the single-tone 1dB compression point. It shows the amplitude of the input current signal that causes 1dB gain compression of the TIA across frequency. The 1dB compression point performance of the single-pole TIA filter is also shown. As can be seen, the proposed TIA filter can handle 4.11mA of blocker current at 60MHz before the transimpedance gain drops by 1dB. This value is greater than that which can be handled by the single pole-filter by 3.9mA. From 60MHz onwards the input P1dB point increases to 5mA at 70MHz and gradually drops to 4.3mA at 100MHz following the shape of the magnitude plot of the filter. From 100MHz onwards the tolerance to blocker signals increases monotonically.

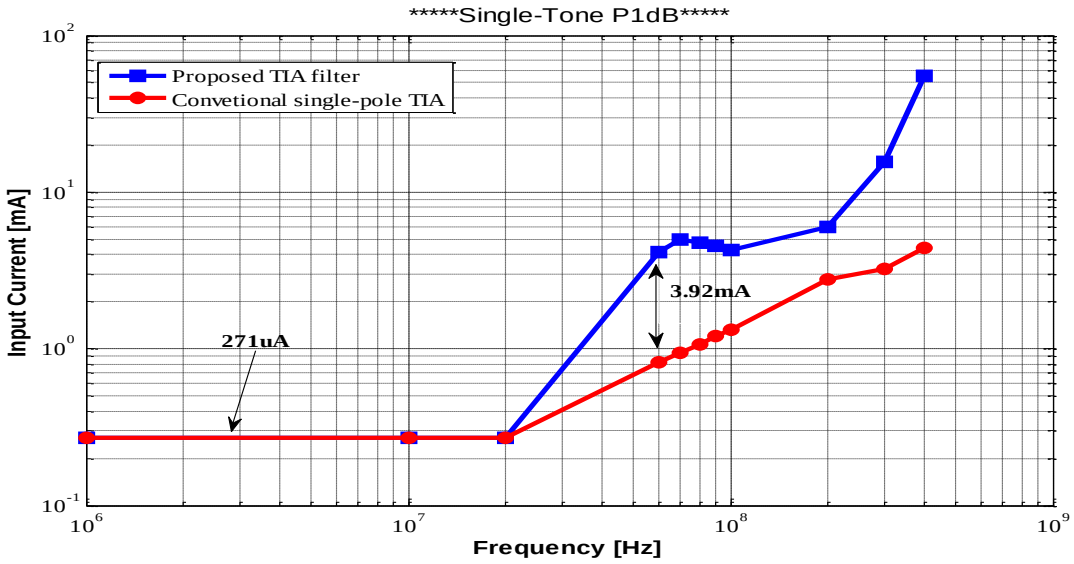


Figure 5.7 Schematic Level Single-Tone 1dB Compression Point.

In Fig. 5.8, the ability of the proposed TIA to withstand blocking/de-sensitization of in-band signals due to large OOB blockers is checked by measuring the 1dB compression point of an in-band small-signal current of 10uA at f = 6MHz in the presence of large close-in OOB tones across frequency.

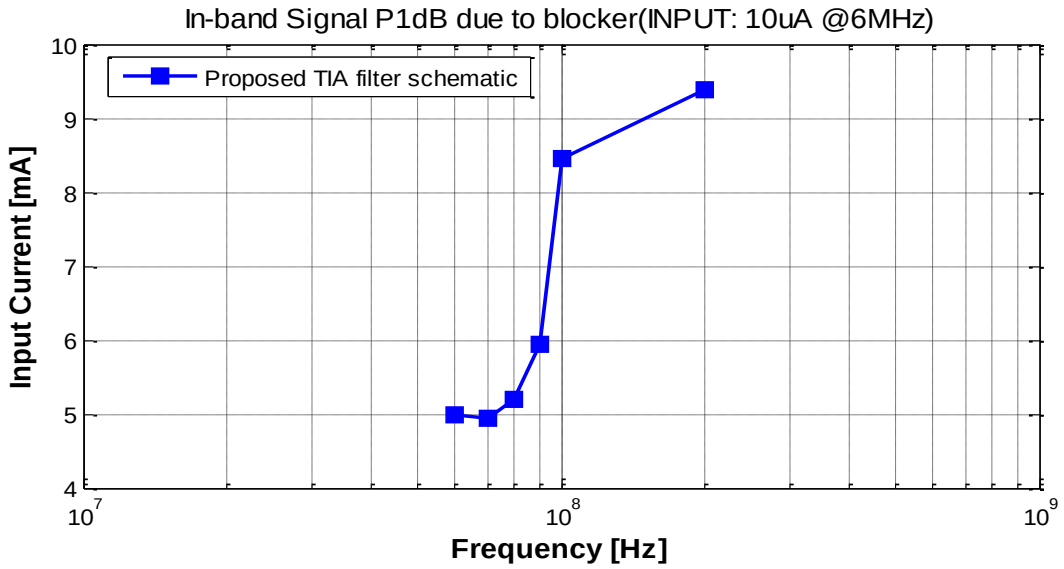


Figure 5.8 Schematic Level In-Band Signal 1dB Compression due to OOB Blocker Signal.

5.2 Layout Simulation Results

Just as in the previous section, both small signal and large signal plots are presented from layout simulation. The plots are compared with those obtained in the schematic level simulations to show how closely the layout matches the schematic level results.

5.2.1 Layout Small-Signal Characterization

In Fig. 5.9, the layout and schematic AC magnitude response plots of the proposed TIA filter are compared. Superimposed in the plot is the layout AC magnitude response for the conventional single-pole TIA filter. There is a loss in attenuation from 200MHz and beyond in the layout AC magnitude response for the proposed TIA filter. This arises from the fringe capacitors used in the layout for the 110pF input shunt capacitor. The schematic AC magnitude response was designed to obtain greater bandwidth of 23MHz for the proposed TIA because it was anticipated that the layout parasitic capacitors will reduce the bandwidth back to 20MHz, and as can be seen the bandwidth from layout simulation is 20MHz. Also, the layout magnitude plot shows slightly greater attenuation at the critical close-in frequencies of 60MHz all the way to 100MHz.

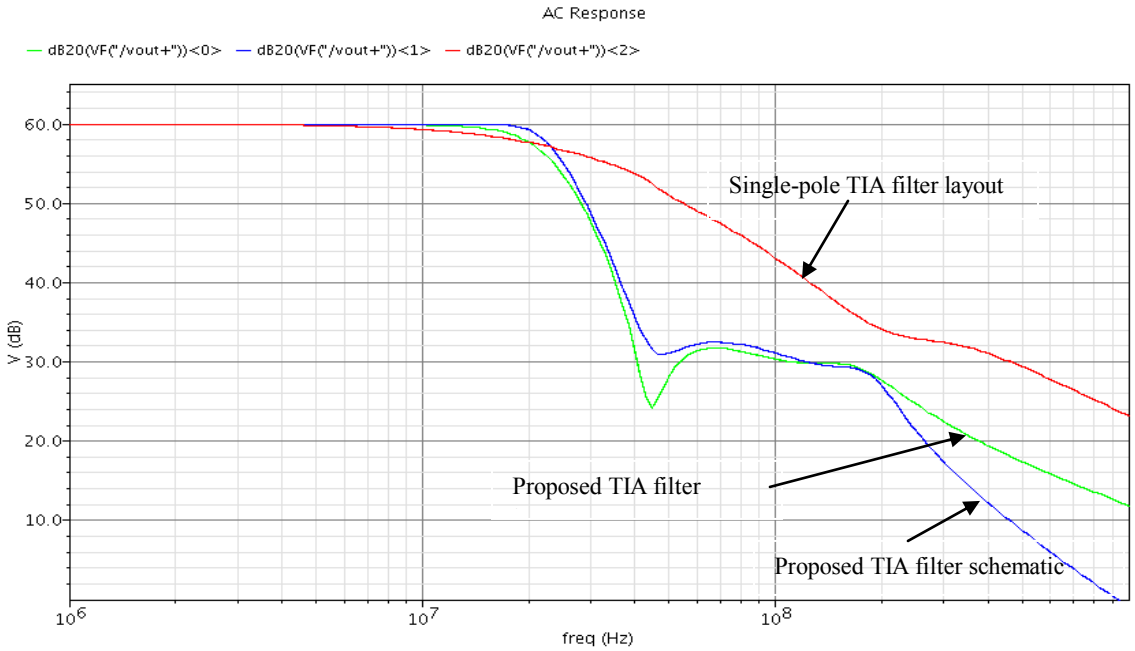


Figure 5.9 Layout AC Magnitude Response of the Proposed TIA Filter.

Fig. 5.10 shows the the input impedance plot. The proposed TIA filter layout provides 24 Ω peak input impedance at 20MHz and it has 7.2Ω input impedance from 60MHz and beyond.

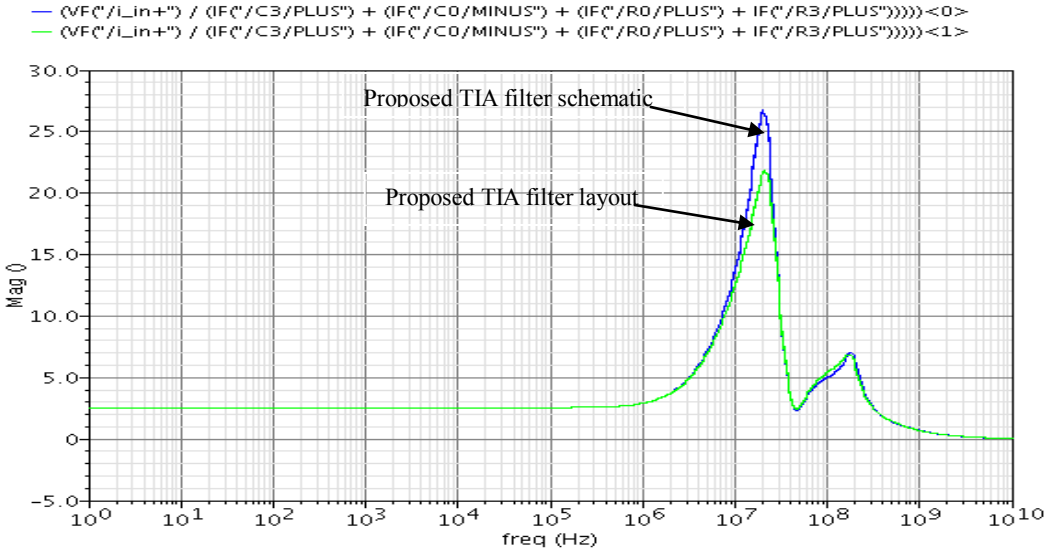


Figure 5.10 Layout Input Impedance of Proposed TIA Filter.

The in-band group delay performance of the layout of the proposed TIA filter shows less variation than for the schematic level group delay performance. Beyond the bandwidth of the filter, the schematic level group delay performance is better, however it is within the bandwidth of the filter that group delay variation matters most. These results are shown in Fig. 5.11.

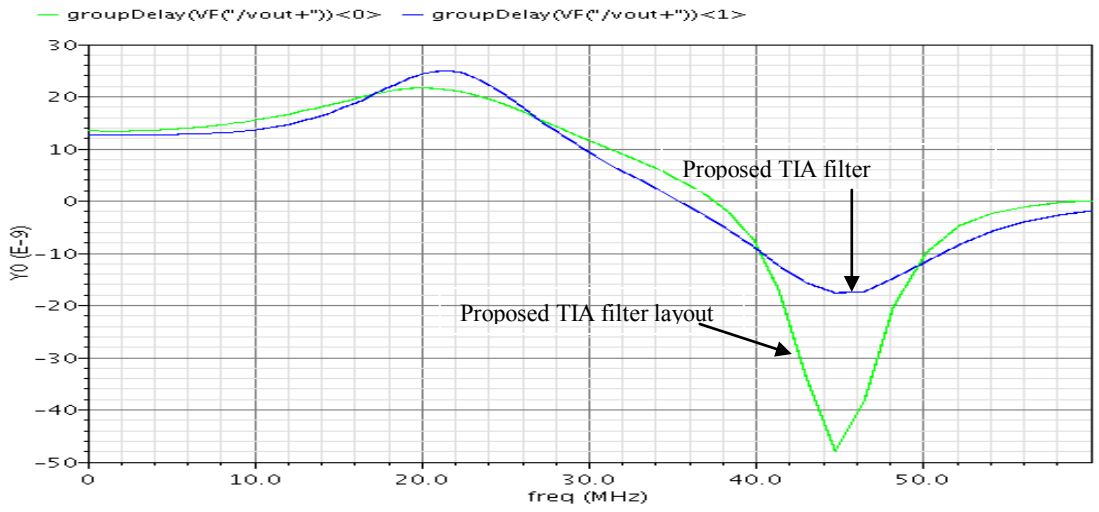


Figure 5.11 Layout In-Band Group Delay Variation.

In Fig. 5.12 the noise performance from layout simulations is plotted and compared with that of schematic level simulations. The noise performance from layout simulations is identical to that of the schematic level simulations. The extracted parasitic resistances do not add significant noise to the TIA filter.

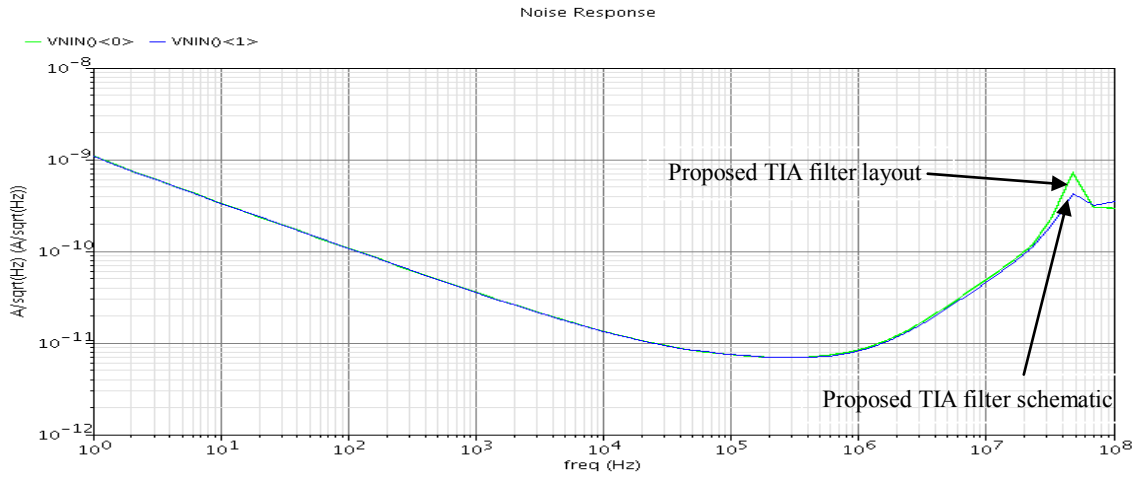


Figure 5.12 Layout Input-Referred Noise Current Density.

5.2.2 Layout Large-Signal Characterization

As with the schematic level simulations, Fig. 5.13 shows the response of the post-layout TIA filter to a 4.5mA OOB blocker at 60MHz .A settling time of 120ns is again observed in the layout transient simulation. The right-hand plot, which is a zoomed-in version of the left-hand plot, clearly shows there is no visible distortion for a full-scale blocker current of 4.5mA at 60MHz.

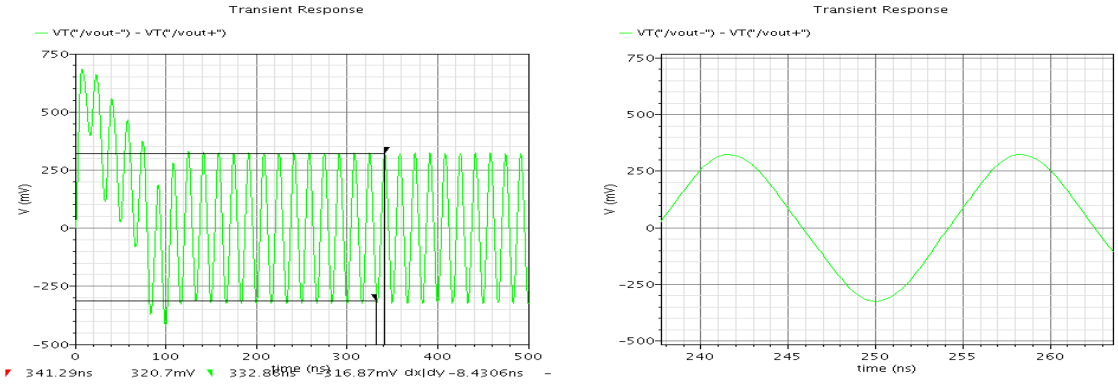


Figure 5.13 Layout Transient Response of Proposed TIA Filter to OOB Blocker of 4.5mA at 60MHz.

Next the transient response of the proposed TIA filter is shown for an in-band signal magnitude of 10uA at 10MHz in the presence of a large blocking signal of 4.5mA at 60MHz in Fig. 5.14.

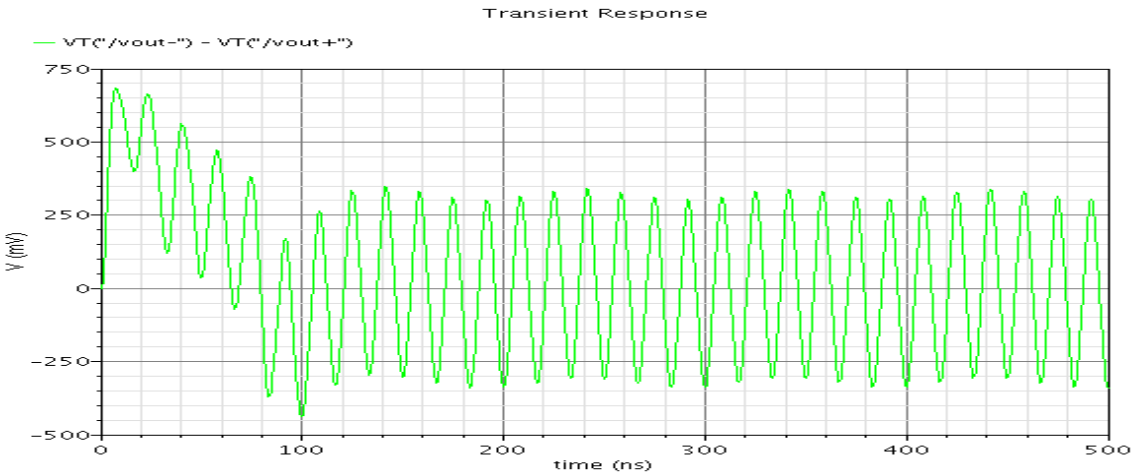


Figure 5.14 Layout Transient Response of Proposed TIA Filter to an In-Band Signal of 10µA at 10MHz in the Presence of an OOB Blocker of 4.5mA at 60MHz.

Fig. 5.15 characterizes the single-tone 1dB compression point of the proposed TIA and Fig. 5.16 characterizes the measured in-band signal 1dB compression due to blocker signal tones. Finally, Table 5.2 gives a summary of the performance of the proposed TIA filter in comparison to the single-pole TIA filter.

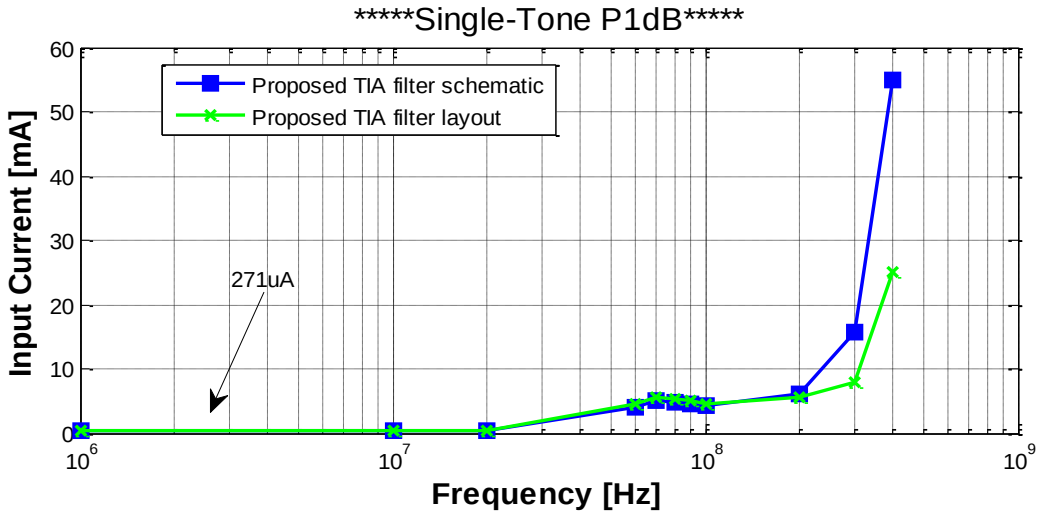


Figure 5.15 Layout Single-Tone 1dB Compression Point.

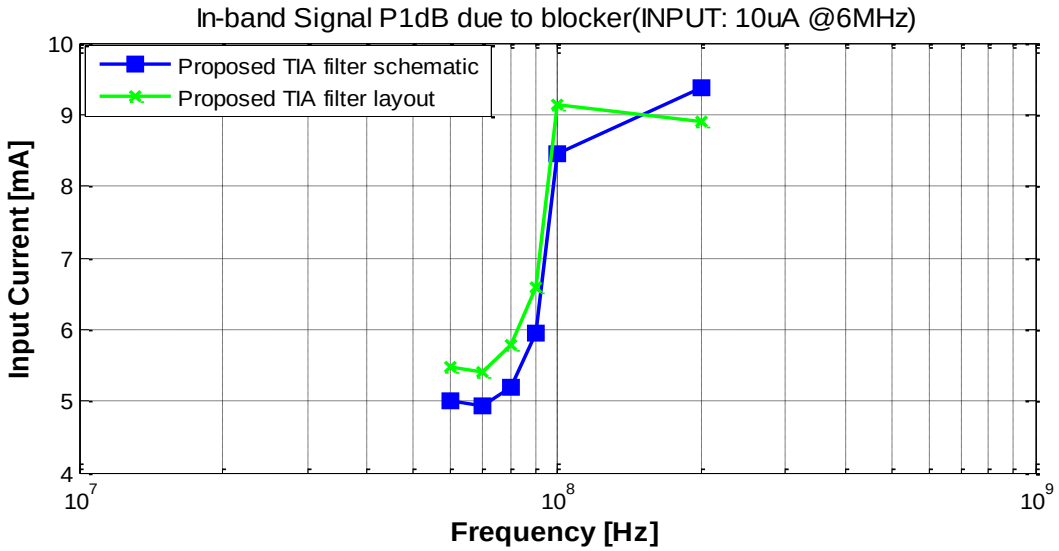


Figure 5.16 Layout In-Band Signal 1dB Compression due to OOB Blocker Signal.

Table 5.2 Proposed TIA Performance Summary.

Parameter	Units	Single-Pole TIA	Proposed TIA
Transimpedance gain	dBΩ	60	60
f_{3dB}	MHz	20	20
$Z_{i,TIA}$, single-ended (60MHz and beyond)	Ω	< 25	< 7.2
1dB compression level for single OOB tone	mA	0.82	4.5
Inband 1dB compression level due to OOB blocker	mA	-	5.4
Vsupply	V	1.2	1.2
Total current consumption	mA	27.9	65
Maximum output voltage swing (single-ended)	mV	±200	±200
Max interferer level at 60MHz	mA	0.63	5
Input referred integrated noise (1Hz - 20MHz)	nA	34	213
Area	mm^2	1.40m x 0.36m	1.55m x 1.09m

6. CONCLUSIONS

In this work, a 20MHz TIA filter is proposed and designed in IBM 90nm CMOS technology for use in multi-standard/multi-band direct conversion receivers which find applications in multi-radio platforms. This filter offers improved attenuation to OOB blockers at close-in frequencies of 60MHz and higher, in contrast to the conventional single-pole TIA filters which are typically used in these front-end receivers. Whereas the single-pole TIA is capable of tolerating blocker magnitudes of 630μA, the proposed TIA filter is capable of tolerating OOB blocker currents of 4.5mA at 60MHz and higher.

The concept presented involves providing an alternate path to large OOB blockers in the form of an active feedback circuit around a single-pole TIA filter which sets the channel bandwidth and typical in-band characteristics such as transimpedance gain, input impedance and noise. The result is that greater attenuation is obtained at close-in OOB frequencies without sacrificing in-band characteristics.

A 3^{rd} order inverse Chebyshev approximation is chosen for the proposed filter due to its double advantage of providing large stop-band attenuation and small in-band group delay variation over the other conventional filter approximations. The first order section of the inverse Chebyshev approximation represents the single-pole TIA while the 2^{nd} order section becomes the active feedback network.

The advantage of providing higher order filtering before the ADC is to relax the ADC specifications; reduced ADC number of bits reduces cost and complexity of the ADC and its required calibration circuitry. This can potentially reduce the cost and complexity of the receiver chain if the extra power dissipated in the TIA is offset by the savings in power in the ADC as a consequence of its lower resolution. As a second advantage, embedding the extra OOB filtering within the TIA increases receiver sensitivity and linearity in the presence of large blockers. This is evidenced by the improvement of in-band 1dB compression point from the simulations results provided in Table 5.2; the

proposed TIA can tolerate 4.5mA of blocker current while the single-pole TIA can only tolerate 820μA of blocker current at 60MHz before in-band gain is compressed by 1dB.

A number of bottlenecks arise in the implementation of the proposed TIA filter. One major design challenge is that, the class AB amplifier (denoted as OpampB in this work) in the biquad employed in the feedback network has to be capable of sourcing/sinking the full-scale blocker current of 4.5mA through a large 30pF capacitor. Two issues arise here. The first is that, to be able to process larger blocker currents, a larger supply voltage is required in order not to saturate the output of OpampB. A second issue as witnessed through macro-modeling is that a GBW limitation in the OpampB results in loss of close-in OOB attenuation of the filter. Thus, to reduce this effect the GBW of OpampB must be maximized. And since it drives a 30pF capacitor, a significant amount of power will need to be dissipated in this op-amp. The proposed TIA filter dissipates 2.4 times more current than the single-pole TIA filter. It has degraded input integrated noise performance due to the additional circuitry and the chip area is 3.4 times the area of the single-pole filter.

As this proposed TIA filter is a prototype design, chiefly to test the feasibility of the theoretical concept presented, later designs should aim at providing voltage to current conversion in the feedback network using an OTA to eliminate the large 30pF capacitor, and reducing the number of op-amps within the biquad to reduce power consumption and area, as well as lowering in-band integrated noise.

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