A DUAL-SUPPLY BUCK CONVERTER WITH IMPROVED LIGHT-LOAD EFFICIENCY

A Thesis

by

CHAO ZHANG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sanchez-Sinencio
Committee Members,	Samuel Palermo
	Peng Li
	Duncan M. Walker
Head of Department,	Costas N. Georghiades

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ABSTRACT

A Dual-Supply Buck Converter with Improved Light-Load Efficiency. (May 2011)

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Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

Power consumption and device size have been placed at the primary concerns for battery-operated portable applications. Switching converters gain popularity in powering portable devices due to their high efficiency, compact sizes and high current delivery capability. However portable devices usually operate at light loads most of the time and are only required to deliver high current in very short periods, while conventional buck converter suffers from low efficiency at light load due to the switching losses that do not scale with load current. In this research, a novel technique for buck converter is proposed to reduce the switching loss by reducing the effective voltage supply at light load.

This buck converter, implemented in TSMC 0.18μm CMOS technology, operates with a input voltage of 3.3V and generates an output voltage of 0.9V, delivers a load current from 1mA to 400mA, and achieves 54% ~ 91% power efficiency. It is designed to work with a constant switching frequency of 3MHz. Without sacrificing output frequency spectrum or output ripple, an efficiency improvement of up to 20% is obtained at light load.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to my advisor, Dr. Sanchez, who gave me the opportunity to pursue my MS degree under his guidance. I am very grateful for his professional advisement and support throughout my graduate study. I would also like to thank Dr. Samuel Palermo, Dr. Peng Li and Dr. Duncan M. Walker for severing on my committee. And thanks to Dr. Rabi N. Mahapatra for substituting for my defense.

Thanks also go to my colleagues at AMSC group for giving me valuable experience. Special thanks to Heng Zhang. Being part of her ADC project was a precious learning exercise, not only because she shared her valuable design and layout knowledge with me, but also her serious scientific attitude, professional thought, hardworking spirit has inspired me during my whole graduate life. I would like to thank my team members in buck converter project, Miguel A. Rojas-González, Joselyn Torres and Adrian Colli-Menchi, for their cooperation, great advice and making the project a great experience. I would like to thank all my other friends in AMSC group for their support and company. Studying together with them, discussion questions and sharing ideas are joyful memories for me. I also want to thank Ella and Tammy for their assistance.

Finally, I would like to express my deepest gratitude to my parents for their encouragement and unconditional love. I couldn’t go this far without their support.

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1. INTRODUCTION

1.1 Research Motivation

Over the years as the portable device industry developing, different requirements are brought out such as increased battery lifetime, small size, cheap cost, and brighter, full-color displays. An ever increasing demand from power systems has placed power consumption at the primary concern. To keep up with these demands, engineers have dedicated tremendous work towards developing efficient conversion techniques. High efficiency conversion of power supplies helps to reduce power consumption for battery-operated applications, and increases the devices operating time. In addition, if the power devices dissipate a fairly large amount of power, they have to be adequately cooled by mounted on heat sinks. Thus the heat can be transferred to the surrounding air. Heat sinks and provision for cooling make the regulator bulky and large. Reduced power dissipation in the power supply will reduce the need for heat sinks and relax thermal design considerations. These benefits have resulted in the popularity of switching converters which have fairly high efficiency and compact size.

Buck converter or step-down converter is the most widely used switching converter in powering up the portable applications. The efficiency of buck converter is expressed by [1]-[3]:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}\, I_{out}}{V_{in}\, I_{in}} \tag{1.1}$$

This thesis follows the style of *IEEE Journal of Solid State Circuits.*

where P_{out} is the power output to the load, V_{out} is the output voltage, I_{out} is the load current, P_{in} is the total power supplied by the input voltage source, V_{in} is the input voltage, I_{in} is the current drawn from the supply.

Buck converters provide very high efficiency, approaching 100% as the components are made more ideal. Considering the parasitic, the efficiency of buck converters with practical components can still achieve above 80% in most of the cases. However, the efficiency is not always maximized, but varies according to the size of load. The typical efficiency curve for a conventional buck converter, which is optimized for a medium load range, is shown in Figure 1 [4]. It shows that the efficiency decreases as load becomes lighter or heavier, and especially at light load (where the load current is small), the efficiency drops to extremely low very quickly. Since the portable devices are operating in low-power standby mode or sleep mode for a majority of the time when they are on, which is in the light load region, the poor light-load efficiency can severely limit the battery lifetime. Hence improving light-load efficiency is critical for portable devices. The main objective of this work is to propose a new method to improve light-load efficiency.

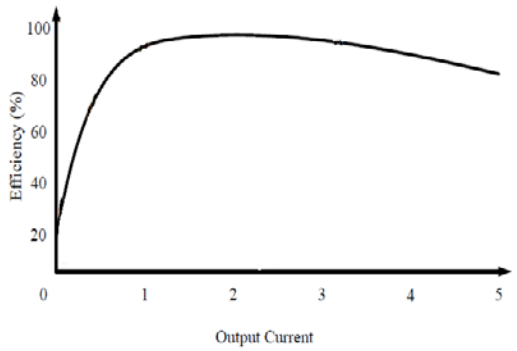


Figure 1. Buck converter efficiency vs output current

1.2 Thesis Organization

This thesis consists of eight sections.

Section 1 presents the motivation of this project and sets objectives for the research contribution.

Section 2 introduces the fundamentals of switching converters, especially buck converter and boost converter, addresses the open problems in buck converters, and analyzes the power losses.

Section 3 overviews the light-load efficiency improving techniques existing in literature and industry, proposes a new method, and demonstrates the strengths and weaknesses of the proposed method.

Section 4 implements the proposed buck converter in TSMC 0.18um CMOS process. System architecture and system level design are described.

Section 5 covers the transistor level implementation of each building block.

Section 6 verifies the proposed idea with simulation results, and compares them with previous work.

Section 7 reveals the preliminary lab measurement results, and analyses the existing problems and possible reasons.

Section 8 summarizes this research and discusses the future work.

2. FUNDAMENTALS

2.1 Introduction of Switching Converters

A switching converter or switch mode power converter is a power electronic system which converts one level of electrical energy into another level of electrical energy at the load, by switching action [1]. Switching converters have been in existence since the 1950s, and then became a popular choice in power supplies in the 1970s due to the emergence of modern power semiconductor devices (e.g., power MOSFET, GTR). Nowadays, the applications of switching converters are expanding quickly. The power levels encountered range from milliwatts such as in battery-operated portable equipment, to megawatts such as in variable-speed motor drives.

In general, a switching converter, as illustrated in Figure 2, contains power input and output ports, and a control block to regulate output voltage in the presence of varied input voltage and output current [2]. Switching converters can be classified into four categories according to the input and output voltage forms:

1) A DC-DC converter converts a DC input voltage to a regulated output voltage with a larger or smaller magnitude, and opposite polarity is possible.
2) A DC-AC inverter converts DC input voltage to AC output voltage with controllable magnitude and frequency.
3) An AC-DC rectifier produces a DC output from an AC input.
4) An AC-AC cycloconverter can be used to change the level and/or frequency of an AC signal.

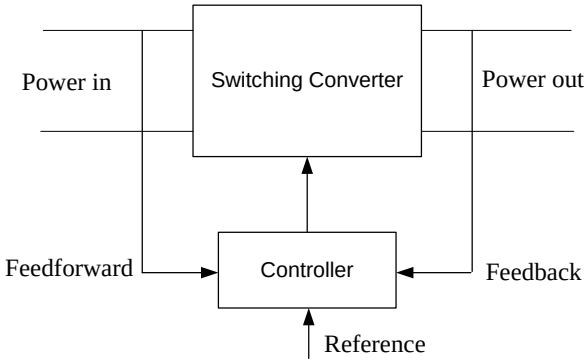


Figure 2. Switching converter block diagram [2]

2.2 DC-DC Switching Converters

2.2.1 Introduction

DC-DC switching converters are very popular used as power supplies in portable electronic devices such as cellular phones, digital cameras, laptop computers etc. Often in these electronic devices, several sub-circuits with different voltage and current requirements exist. Instead of using multiple batteries, DC-DC converters are able to generate different supplies for each sub-circuit with its required voltages, currents and power ratings from a single battery source, therefore saving a lot of space. Additionally, the battery voltage drops with time. DC-DC converters offer a method to generate regulated output voltage from an unregulated DC voltage source [3], [5].

In a DC-DC switching converter, the transistor operates as an electronic switch by being completely on or completely off. In Figure 3, assuming that the switch is ideal, then the output voltage is the same as input when the switch is on, and the output is zero when the switch is off. When the switch is on, there is no voltage drop across it; when the switch is off, there is no current across it. So the power dissipated on the switch is zero.

In other words, all power is absorbed by the load, and the power efficiency is 100%. In practical circuit, there will be some losses, but the efficiency is still high. Drawbacks of switching converters include complexity, noise and electromagnetic interference (EMI).

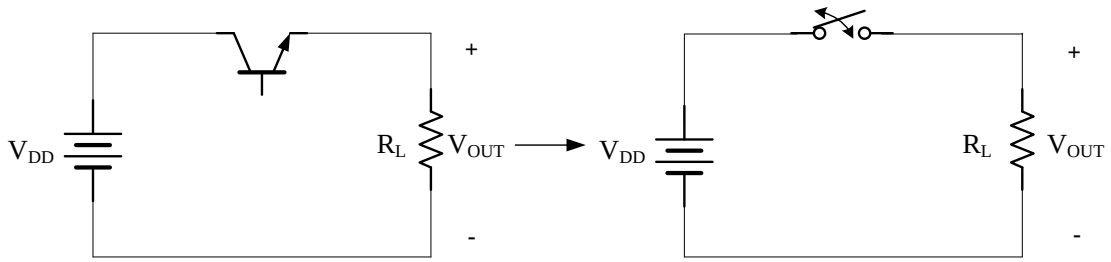


Figure 3. A basic DC-DC switching converter

Before discussing DC-DC switching converters, it is useful to understand the motivation for an alternative to linear DC-DC converters (or linear regulators) and switched-capacitor converters.

2.2.2 Comparison with Linear Regulators and Switched-Capacitor Converters

2.2.2.1 Linear Regulators

Although there is trend that linear regulations are replacing with switching converters, linear regulators remain a basic building block used in almost every power supply design. It offers a simple, low cost solution for delivering stable, low noise DC voltage to power analog and digital circuits. Additionally, it is available in fixed and adjustable output voltage versions, and also positive and negative voltage output versions to meet different application requirement.

The linear regulator, conceptually illustrated in Figure 4 [6], operates based on active devices, such as bipolar junction transistor (BJT) or filed effect transistor (FET), working in their linear region. The active device acts as a viable resistor to maintain constant output voltage by adjusting a voltage divider network.

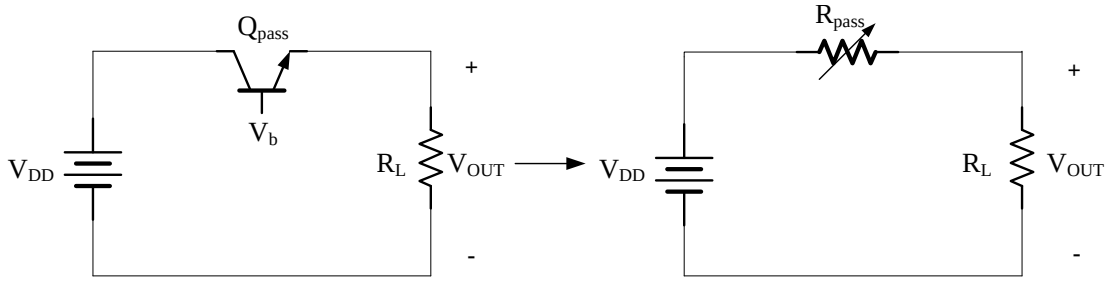


Figure 4. A basic linear regulator

All types of linear regulators use the similar control technique to regulator the output voltage. As shown in Figure 5, the feedback loop combines a reference voltage, an error amplifier and an active device. The output voltage V_{OUT} is monitored through a resistor divider which is consisted of R1 and R2. By comparing the sensed voltage with a reference voltage to adjust the input to the active device, sufficient load current is provided to maintain constant output voltage. C_L is an external capacitor used for compensation, and R_L is the load resistor.

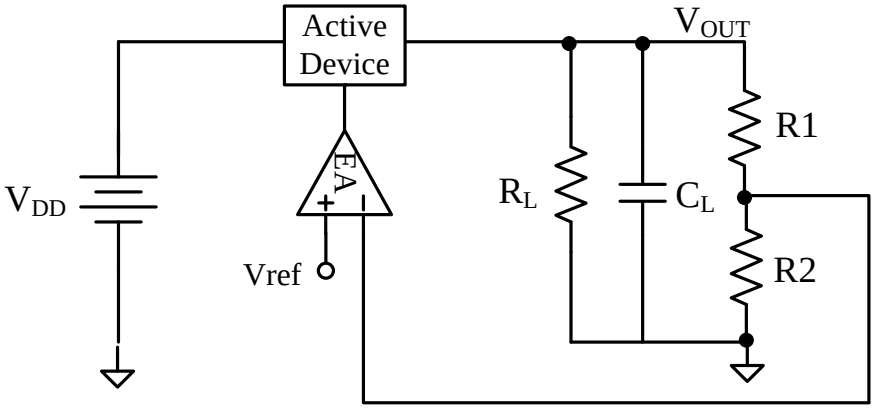


Figure 5. Basic close loop linear regulator

Linear regulators can be grouped into three types according to their different dropout voltages: standard regulators, low-dropout (LDO) regulators, and Quasi-LDO regulators [7]-[8]. Standard regulators use the NPN Darlington configuration for the active device, and have the highest dropout voltage. LDO regulators use one PNP transistor for the active device, and have the lowest dropout voltage. Quasi-LDO regulators use an NPN transistor and a PNP transistor as the active device, and their dropout voltages are between standard and LDOs. Lower dropout voltage usually means higher efficiency, because less power is dissipated internal. From application point of view, the standard regulator is usually best for AC-powered applications where dropout voltage is not critical compared with voltage across the regulator, and the low cost and high load current make it the ideal choice. The LDO regulator is best suited for battery-operated applications where the lower dropout voltage makes it more efficient [7].

The good thing about linear regulator is that it can provide a very low noise output voltage, which is suitable for powering noise sensitive low power analog and radio frequency circuits. But linear regulators can only output lower voltage than input. Also

they are less efficient when the voltage conversion ratio is large because the highest efficiency η_{max} attainable with an ideal linear regulator is given by:

$$\eta_{max} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{DD} \cdot I_{IN}} = \frac{V_{OUT}}{V_{DD}} \tag{2.1}$$

where P_{IN} is the input power consumption, P_{OUT} is the output power consumption, V_{DD} is the regulator input voltage, I_{IN} is the input current, V_{OUT} is the regulator output voltage, and I_{OUT} is the output current, which is equal to input current I_{IN}.

While a switching converter can easily provide more than 30A of current at voltages as low as 3V, for the same voltage and current, a linear regulator would be very bulky and heavy due to the heat sinks it needed. Thus linear regulators are not normally used for large-drop high-current applications. Current trends of linear regulators include lower dropout voltages, lower operating voltages, smaller packages, and thermally efficient packages [8].

2.2.2.2 Switched-Capacitor Converter

A switched-capacitor converter, also called charge pump, is a kind of DC-DC converters. It uses a combination of switches and capacitors to produce an output voltage that either higher or lower than the input voltage as well as polarity reversal. SC converters are capable of high efficiencies, sometimes as high as 90% ~ 95%. They are useful for small output power applications that do not require isolation between input and output, such as LCD or white LED drivers, supplying non-volatile memory circuits (flash and electrically erasable programmable read only memories) and so on. The main advantage of the SC converters is the absence of bulk inductors and transformers, making possible a complete integration of the switching converter [1].

The operation of SC converter relies on periodically charging or discharging capacitors. A typical SC converter with ideal switches is shown in Figure 6 [9]. It consists of four clock-controlled switches S_1 to S_4, two capacitors C_1 and C_2, an input voltage source V_{IN}, and the load. During phase φ_1, switches S_1 and S_4 are turned on (mode 1) out of phase with S2 and S3 for half of the period (50% duty cycle), as illustrated in Figure 7. During phase φ_2, switches S_2 and S_3 are turned on (mode 2) out of phase with S_1 and S_4 for the other half of period, as illustrated in Figure 8. The output voltage V_{OUT} is $V_{IN}/2$ when capacitor C_1 is equal to C2.

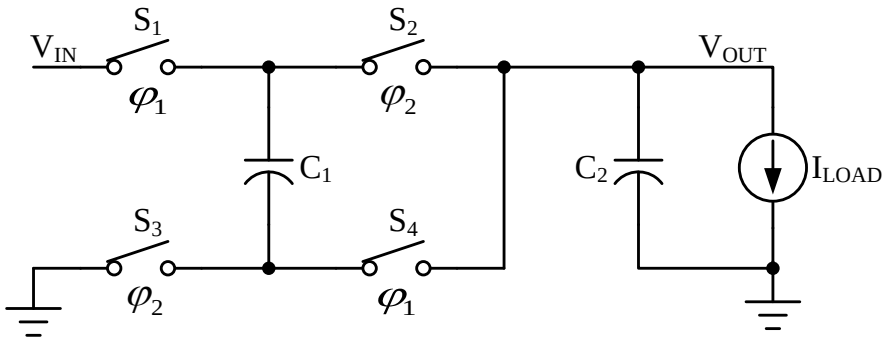


Figure 6. Typical switched-capacitor voltage divider (single phase)

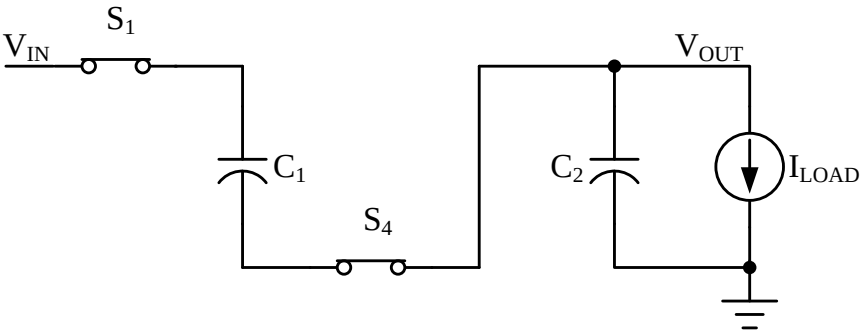


Figure 7. Simplified SC converter during phase φ_1 (mode 1)

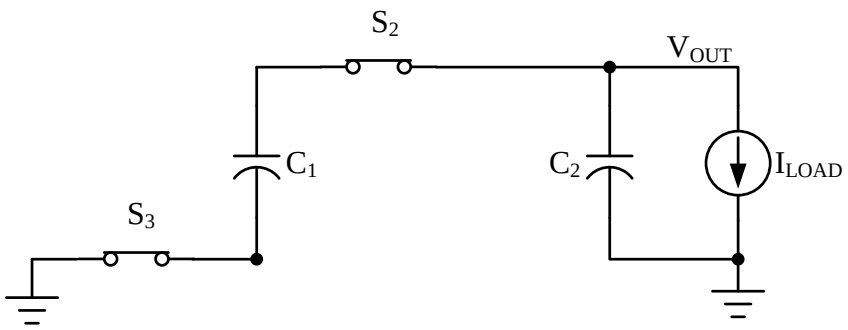


Figure 8. Simplified SC converter during phase φ_2 (mode 2)

2.2.2.3 Comparison

The comparison between DC-DC switching converter, linear regulator and switched-capacitor converter is summarized in Table 1. The three types of converters all have their own advantage and disadvantage. The choice between the three types is depending on applications.

Table 1. Comparison between switching converter, linear regulator and switched-capacitor converter

	Switching converter	Linear regulator	Switched-capacitor converter
Function	Step up/down, even reversed polarity	Step down	Step up/down, even reversed polarity
Voltage Regulation	Good	Good	Poor
Efficiency	High	V_{OUT}/Vin; usually low	Low
Current Rating	High	Low	Medium
Complexity	High, requiring inductor, capacitor and sometimes diode	Low	High, requiring more switches and capacitors
Size	Large	Small	Medium
Ripple/Noise	High; ripple at switching frequency	Low; no ripple, low noise	High
Total Cost	High; mainly due to off-chip components	Low	Medium

2.2 Introduction of Buck and Boost Converters

DC-DC switching converter can be divided into two types, the non-isolated one and isolated one.

Non-isolated converters are simplest, including Buck converter, Boost converter, Buck-Boost converter, Cuk converter, Sepic converter, Zeta converter and so on. They have similar topologies which are consisted of two switches, inductors, capacitors and the load. By connecting these components in different ways, different voltage conversion functions can be obtained. Buck converter converts an input voltage to a lower output voltage. Boost converter converters an input voltage to a higher output voltage. Buck-

Boost converter, Cuk converter, Sepic converter and Zeta converter are all able to provide an output voltage with both higher and lower value than the input voltage, which combine the functions of buck converter and boost converter in one circuit.

Isolated converters are bulky due to the use of transformers, but in some cases that the primary power supply operates at a relatively high voltage and/or is very noise, isolation of the load from the input supply is necessary to maintain reliable operation of the load. Common isolated converters are Flyback converter, Forward converter, Push-pull converter, Full-bridge converter, Half-bridge converter and so on. The Flyback converter is based on the Buck-Boost converter, and Forward converter is based on the Buck converter. Their conversion ratios are *n* times larger than the nonisolated versions, where *n* is the transformer turns ratio. Push-pull converter, Full-bridge converter and Half-bridge converter are converters with conversion rations of *nD* (for Push-pull converter and Full-bridge converter) or *0.5nD* (for Half-bridge converter), where *n* is still the transformer turns ratio, and *D* is duty cycle. Figure 9 shows an example of Flyback converter with ideal switch.

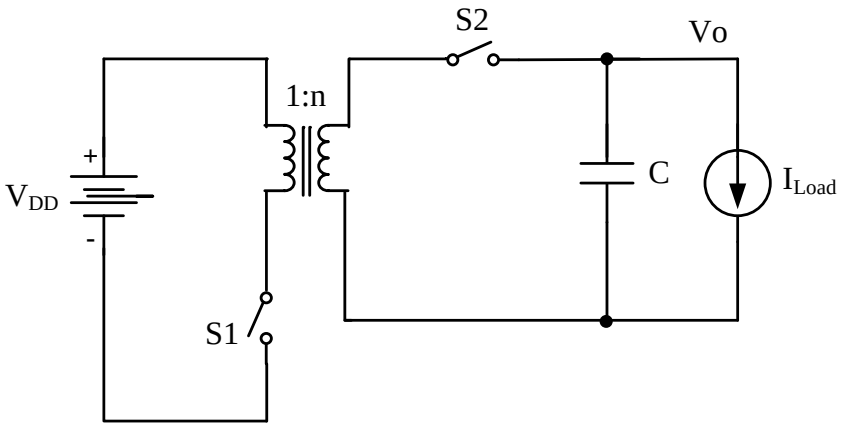


Figure 9. Flyback converter

Among these varies types, Buck converter and Boost converter are the two most widely used DC-DC converters. Their basic topology and working principles will be introduced in this section.

2.2.1 Basics of Buck Converter

Buck converter is a step-down DC-DC switching converter, whose basic functionality is to convert an input DC voltage to a lower DC output voltage. As shown in Figure 10, it is consisted of switch S, inductor L, capacitor C, input DC voltage source V_{DD} and resistive load. The switch alternates periodically between connecting to node 1 and node 2, resulting in a square wave V_{sw}, as shown in Figure 11. V_{sw} equals to V_{DD} when the switch S is connected to voltage source, and drops to zero when S is connected to ground. The inductor and capacitor forms a low pass filter to obtain the DC component of Vx. The output voltage of buck converter V_o is expressed as:

$$V_o = D \cdot V_{DD} \tag{2.2}$$

where D is called duty cycle, and represents the fraction of time that the switch connects to source voltage. The switching frequency f_s, which equals to the inverse of the switching period T_s, generally lies in several kilo Hz to several Mega Hz.

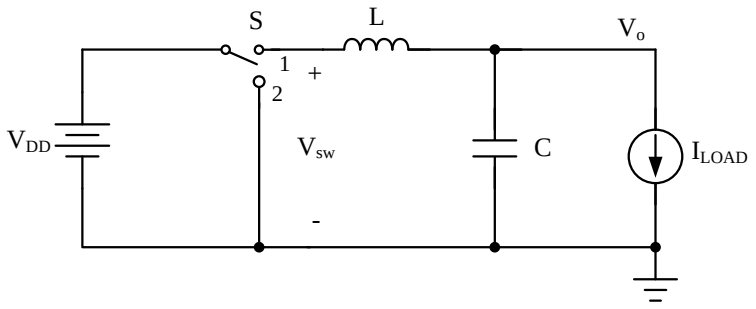


Figure 10. Buck converter with ideal switch model

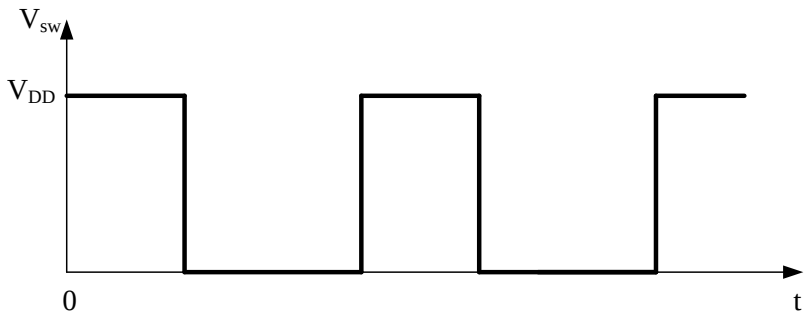


Figure 11. Voltage waveform at the switching node

The operation of buck converters can be classified according to the continuity of the current flowing through the output inductor. If the inductor current flow is continuous of charge and discharge during a switching period, it is called Continuous Conduction Mode (CCM) operation. If the inductor current has an interval of time staying at zero during a switching period, it is called Discontinuous Conduction Mode (DCM) operation. CCM and DCM operation waveforms of inductor current are illustrated in Figure 12. The zero inductor current in DCM operation usually results from the single direction current flow characteristic of switch.

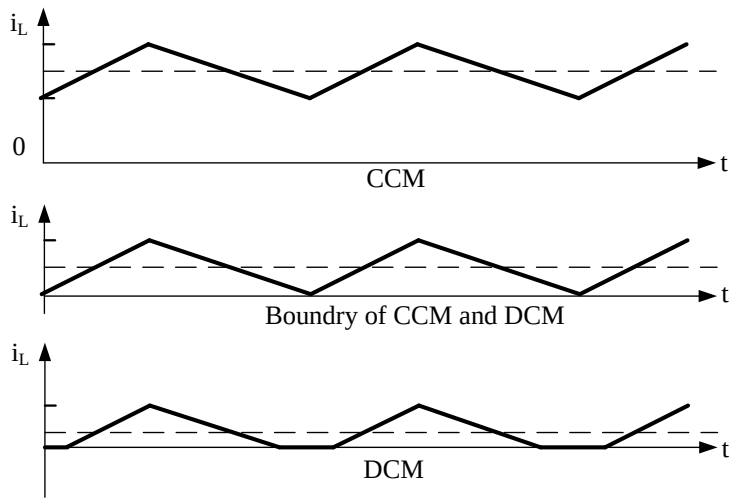


Figure 12. Illustration of CCM and DCM

Based on different implementations of power switches in the power stage, the buck converter is classified as asynchronous and synchronous structures (Figure 13(a) and (b)). As shown in Figure 13(a), asynchronous buck converter is comprised of a PMOS transistor, a diode, an inductor and a capacitor. The diode behaves as a unidirectional switch, as the current of the diode can only flow from anode to cathode. The only difference of synchronous buck converter is the replacement of diode with MOSFET. The second MOSFET is known as a synchronous rectifier, also called a low-side MOSFET. In Figure 13(b), when S2 is on and S1 is off, current flows upward out of the drain of S2. The advantage of this configuration is that the rectifier has a much smaller voltage drop across it compared to a diode, resulting in higher efficiency. The mathematical comparison of the power loss on a diode and a MOSFET is given by

$$P_{MOS} = I_{out}^2 \cdot R_{ds} \cdot (1 - D) \tag{2.3}$$

$$P_{Diode} = I_{out} \cdot V_{Fwd} \cdot (1 - D) \tag{2.4}$$

where I_{out} is average output current, R_{ds} is the MOSFET on-resistance, V_{Fwd} is the diode forward voltage drop. Since V_{Fwd} is normally around 0.7V, and R_{ds} can be as small as several hundred milliohms, the power loss difference in low power applications can be very large. Thus, in this project, synchronous buck converter scheme is preferred.

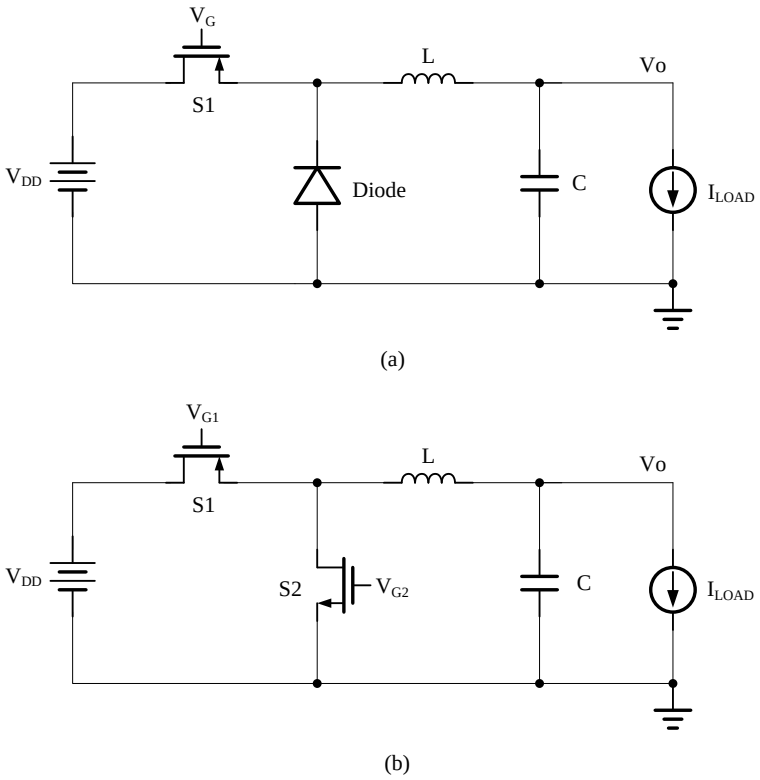


Figure 13. (a). Asynchronous buck converter (b). Synchronous buck converter

Synchronous buck converter always operates in the CCM because the low-side MOSFET is a bi-direction switch, which allows inductor current going to negative, as shown in Figure 14. The following analysis is based on CCM operation.

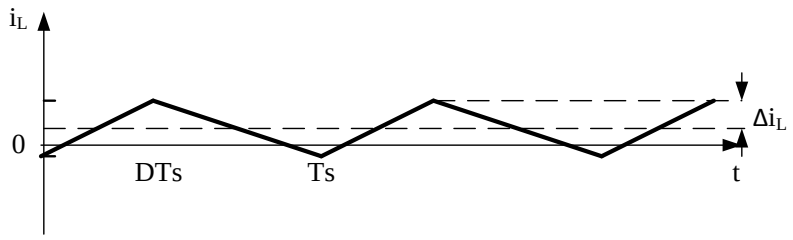


Figure 14. Inductor current goes to negative

Assume the circuit is operating in CCM, steady state, and the components are ideal. For steady state operation, the analysis is based on the following two principles: the inductor current change over one period much be zero, and the capacitor voltage change over one period much be zero. The waveforms of voltage across inductor V_L and inductor current i_L are shown in Figure 15, where i_L can be obtained from:

$$V_L(t) = L\frac{di_L(t)}{dt} \tag{2.5}$$

Thus,

$$i_L(t) = \int \frac{V_L(t)}{L}dt = \begin{cases} \dfrac{\mathrm{V_{DD}} - \mathrm{V_o}}{\mathrm{L}} \cdot \mathrm{t} & 0 < t < D\mathrm{T_s} \\ \dfrac{\mathrm{V_{DD}} - \mathrm{V_o}}{\mathrm{L}} \cdot \mathrm{DT_s} - \dfrac{\mathrm{V_o}}{\mathrm{L}} \cdot (\mathrm{t} - \mathrm{DT_s}) & \mathrm{DT_s} < t < \mathrm{T_s} \end{cases} \tag{2.6}$$

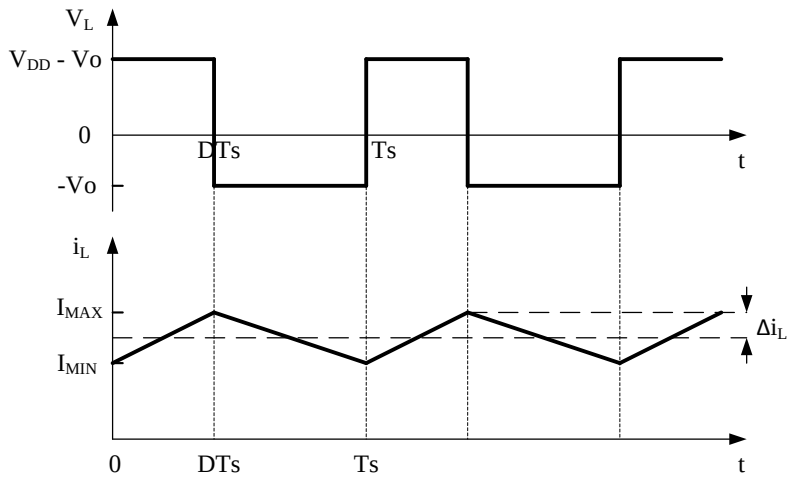


Figure 15. Inductor voltage *Vx* and inductor current i_L waveforms

The inductor peak-to-average current ripple Δi_L is given by:

$$\Delta i_L = \frac{I_{MAX} - I_{MIN}}{2} = \frac{V_o}{2L}(1-D)T_s = \frac{V_{DD} - V_o}{2Lf_s} \cdot D \tag{2.7}$$

where I_{MAX} is the maximum inductor current, and I_{MIN} is the minimum inductor current.

It is undesirable to allow Δi_L becoming too large. Doing so would increase the peak currents of the inductor and of the switching device, and would increase their size and cost.

In practice, the output voltage ripple cannot be kept perfectly constant with a finite capacitance. The variation in output voltage or output voltage ripple ΔV_o is given by:

$$\Delta V_o = \frac{q}{2C} = \frac{\frac{1}{2}\Delta i_L \frac{T_s}{2}}{2C} = \frac{\Delta i_L}{8Cf_s} = \frac{(1-D)D}{16LCf_s^2} \cdot V_{DD} \tag{2.8}$$

where q is the charge on output capacitor.

The two MOSFETs must not be on at the same time to prevent a short circuit across the source, so a “dead time” is built into the switching control-one MOSFET is turned off

before the other is turned on. The waveforms of gate control signals are illustrated in Figure 16.

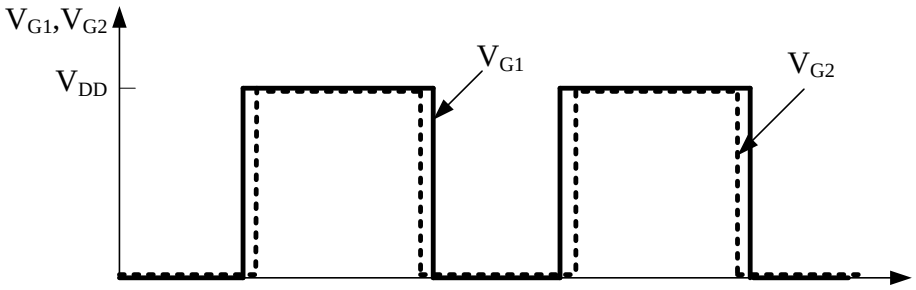


Figure 16. Gate control signals for synchronous buck converter

Discontinuous mode operation is not as frequently used as continuous mode. This is because, in discontinuous mode, the circuit model becomes non-linear, increasing control complexity. It is desirable to design the buck converter to operate either in continuous mode or discontinuous mode, avoiding the change from one mode of operation into the other during normal operation, which may lead to serious stability problems [1]. But since DCM can obtain better circuit efficiency than CCM in light load, some designs employ both CCM and DCM operation. Detailed discussion will be provided in Section 3.

As mentioned in Section 2.1, Electronic magnetic interference (EMI) is one of the main drawbacks of the switching converter. For buck converter, EMI is caused by the pulsating current injected into the power source, as shown in Figure 17, which contains harmonics at multiples of the switching frequency. The large high-frequency current harmonics can interfere with television and radio reception, and can disrupt the operation of nearby electronic equipment. To limit EMI, an input filter can be added to attenuate

the current harmonics produced by the converter. The schematic with input filter and input current waveform is shown in Figure 18 [2].

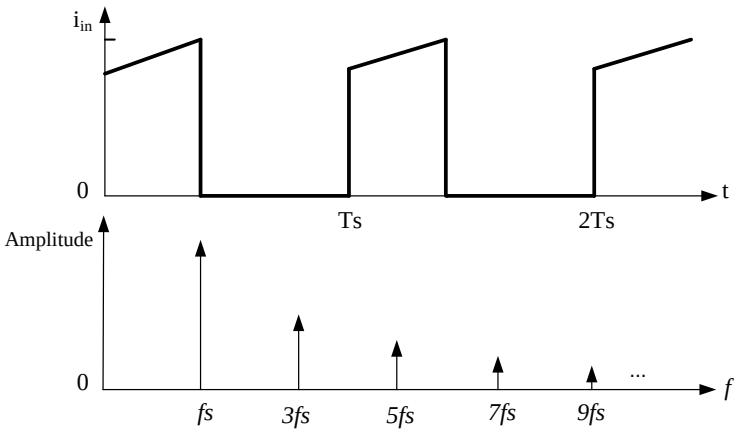


Figure 17. Buck converter input current time domain and frequency domain waveform

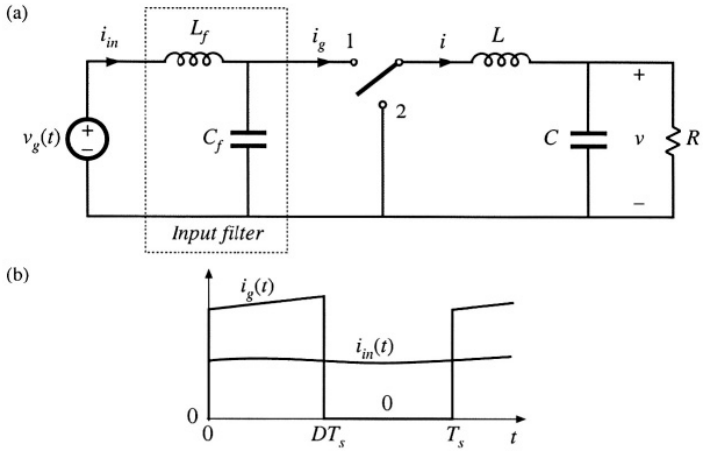


Figure 18. Buck converter with input filter (a). schematic (b). input current waveform

2.2.2 Basics of Boost Converter

The boost converter, also known as step-up converter, is capable of providing an output voltage which is larger than the input voltage. The basic Boost converters with

ideal switch and with power MOSFET and diode as the switching components are shown in Figure 19. The key idea behind achieving a higher output voltage lies in the inductor's ability to resist changes in current. When being charged, the inductor stores energy, and when being discharged, the inductor acts as an energy source (somewhat likes a battery). The output capacitor is very large to keep the output voltage constant during steady-state.

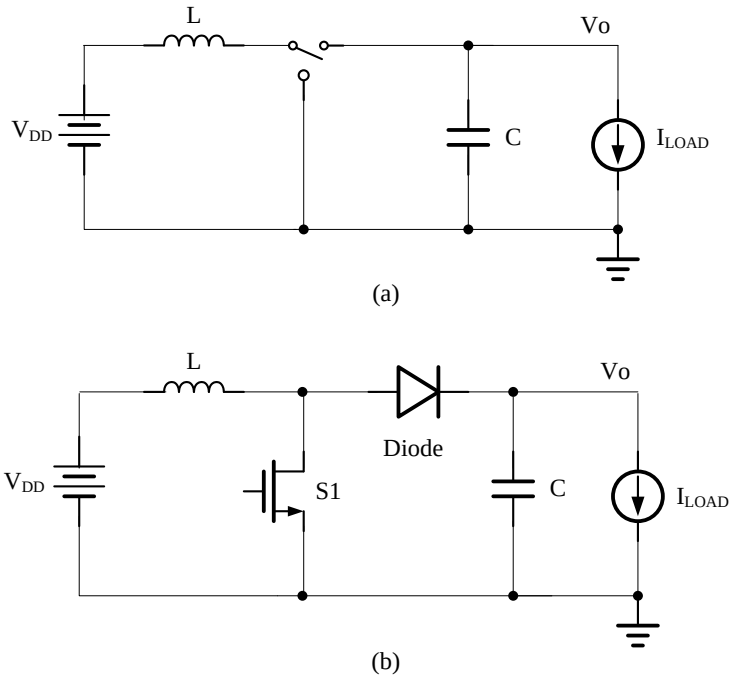


Figure 19. Boost converter topology

(a). with ideal switch (b). with realistic components: power MOSFET and diode

Boost converter also has the synchronous topology which replaces the diode in Figure 19(b) with another power MOSFET. Synchronous boost converter is popular for high efficiency applications [10]-[12].

Similar to Buck converter, the operation of boost converter can be divided into continuous current mode and discontinuous current mode. In CCM, under steady-state condition, the input voltage V_{DD}, output voltage V_o and duty cycle of the switches D have the following relationship [1]-[2], [6]:

$$V_o = \frac{V_{DD}}{1 - D} \tag{2.9}$$

This equation shows that if the switch is always open, which means D is zero, the output will be same as input. As the duty cycle approaches one, the output goes to infinity. However, this equation is based on the assumption of ideal switch. Practical components will have losses and prevent such an occurrence.

The inductor current ripple Δi_L is given by:

$$\Delta i_L = \frac{I_{MAX} - I_{MIN}}{2} = \frac{\frac{V_{DD}}{L} \cdot DT_s}{2} = \frac{V_{DD}}{2Lf_s} \cdot D \tag{2.10}$$

where I_{MAX} is the maximum inductor current, and I_{MIN} is the minimum inductor current. L is the inductance of input inductor, and f_s is the switching frequency. This equation can be used to choose inductance when the spec for Δi_L is provided.

The voltage ripple ΔV_o is given by:

$$\Delta V_o = \frac{\frac{I_o}{C} \cdot DT_s}{2} = \frac{\frac{V_o}{R} \cdot DT_s}{2C} = \frac{D}{2RCf_s} \cdot V_o \tag{2.11}$$

where I_o is the output current, R is the load resistance, and C is the output capacitance. This equation can be used to choose output capacitance when the spec for ΔV_o is provided.

Boost converter will also operate in discontinuous current mode. In some cases, this mode is desirable for control reasons in the case of a regulated output. In DCM, the input and output relationship is given by:

$$V_o = \frac{1+\sqrt{1+\frac{4D_1^2}{K}}}{2} \cdot V_{DD} \tag{2.12}$$

where D_1 stands for the power MOSFET duty cycle, and $K = \frac{2L}{Rf_s}$.

2.3 Open Problems in Buck Converters

As a popular used converter, tremendous effort has been dedicated to improve the performance of buck converter. The evolutionary trend in modern power supplies toward low voltage, high current, high power density, reduced volume, lower cost, and faster transient response poses new challenges for buck converter design. The recent trends and popular problems in buck converter are briefly introduced in the following section.

2.3.1 High Efficiency

Efficiency is the most critical and important parameter for any power supply. A lot of work has been published in the field of improving efficiency. Since the efficiency of buck converter drops both at light load and at heavy load, the research divided into two directions depending on different applications. Applications such as battery-powered portable devices need to be designed for high efficiency over entire load ranges extended from light load to heavy load, and especially at the light load range, since they operate at this region most of the time. This project is targeting at these applications and working on improving light-load efficiency. Other applications maximize efficiency at heavy load with less concern of light-load efficiency in order to minimize the heat generated inside the converter [10]-[14].

There are various kinds of techniques for improving efficiency of buck converter. Among all these techniques, soft switching techniques, especially zero-voltage-switching

(ZVS) and zero-current-switching (ZCS) are very popular in high power applications. In ZCS technique, an inductor is placed in series with converter main switch or main diode to provide soft switching condition at switch turn-on instant. Before switch turn-off instant, an auxiliary switch is turned on and the main switch current is reduced to zero. In ZVS technique, a capacitor is placed in parallel with the main switch to provide soft switching condition for switch turn-off [15]-[17]. Figure 20 shows the example of ZVS implementation for diode turn-off transition, where *Cr* is added in parallel with the diode [2]. In this technique, soft switching condition for switch turn-on is achieved by an auxiliary switch, which discharges the snubber capacitor across the main switch. Soft-switching techniques typically increase the current and/or voltage stresses in the semiconductor devices. ZVS techniques typically increase the voltage stress of the active switches, and ZCS techniques increase current stresses. Furthermore, the auxiliary large and lossy inductor and capacitor make these techniques poor candidates for on-chip implementation applications.

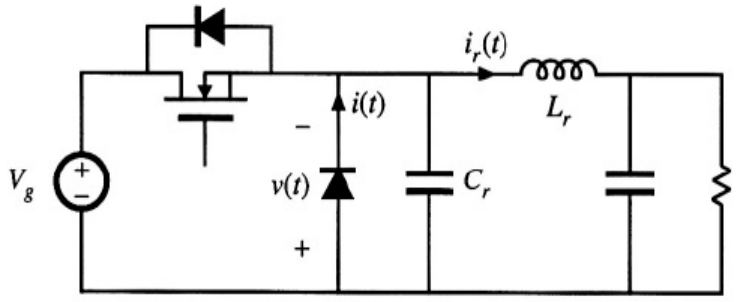


Figure 20. Buck converter schematic with ZVS turn-off [2]

2.3.2 Control Schemes

To improve the output transient response of buck converter, numerous control topologies are proposed for different applications. Faster recovery time and/or smaller voltage overshoot/undershoot, as well as simpler implementations and smaller sizes are targeted.

Traditional control techniques, such as pulse width modulation (PWM) and pulse frequency modulation (PFM), still have margin for improvement. For example, [18] propose a pseudo-Type III compensation for PWM voltage-mode buck converter, which mimics the frequency response of a Type III compensator. Type III compensator provides two zeroes and two poles by adding large value resistors and capacitors to stable the loop, which is area consuming. The pseudo-Type III compensation in [18] is able to be implemented without resistors and capacitors, thus tremendously reduces the chip area and power consumption. Hysteretic control techniques are also popular due to advantages in their simplicity, immediate response to a line/load transient and unconditional stability under all operation conditions. Their main disadvantages are switching frequency varies with design parameters, and the inductor current may go beyond the current limit of the power switches during large signal transient response [19]-[21].

Although analog controllers are still the mainstream control schemes, digital control has gained popularity recent years due to its robustness to noise, lower sensitivity to parameter variations and programmability along with its ability to implement sophisticated control schemes [22]-[23]. The main concern in digital control is how to match the dynamic performance of their analog counterparts [23]-[26]. ADC which

digitizes the error signal and digital PWM generator (DPWM) are the main building blocks and the most challenging circuits to design digital control [27]-[31].

2.3.3 Fully Integration

In recent years, there is a growing interest in power-supply-on-a-chip (PSoC) or power-supply-in-a-package (PSiP) for DC-DC converters. The idea of integrating all active and passive components in a switching converter would provide smaller area and lower cost, fewer connections and less parasitics, and also, it reduces losses through connections and increases reliability. The main challenge of a fully integrated buck converter is to find an effective way to integrate the output filter. Typical values for the filter inductor and filter capacitor are in the order of μH and μF, respectively, which are too large to integrate on chip.

One way to reduce the filter size is increasing the switching frequencies. The higher is the switching frequency, the smaller the physical size and component value. However, there is an upper frequency limit where either magnetic losses in the inductor or switching losses in the converter reduce efficiency to an impractical level. [32], [33] and [34] reported switching frequencies as high as 102MHz, 660MHz and 3GHz respectively to enable the integration of filter, and power losses reduction techniques are employed to achieve better efficiency.

Multiphase interleaved buck converter is another well-known solution to enable smaller filter size [35]-[39]. As shown in Figure 21, multiphase buck converter combines N stages of buck converters in parallel with a common output filter capacitor. By applying a 360°/N phase shift between the control signals of adjacent power stages, the output current ripple can be cancelled out, therefore the required output inductance is

reduce. The effective output frequency is increased to N times of the switching frequency in a single stage and a smaller capacitance is required at the output. Current sharing, current unbalance, phase interleaving, and better controller are the major concerns of multiphase buck converter [21], [38], [40]-[41].

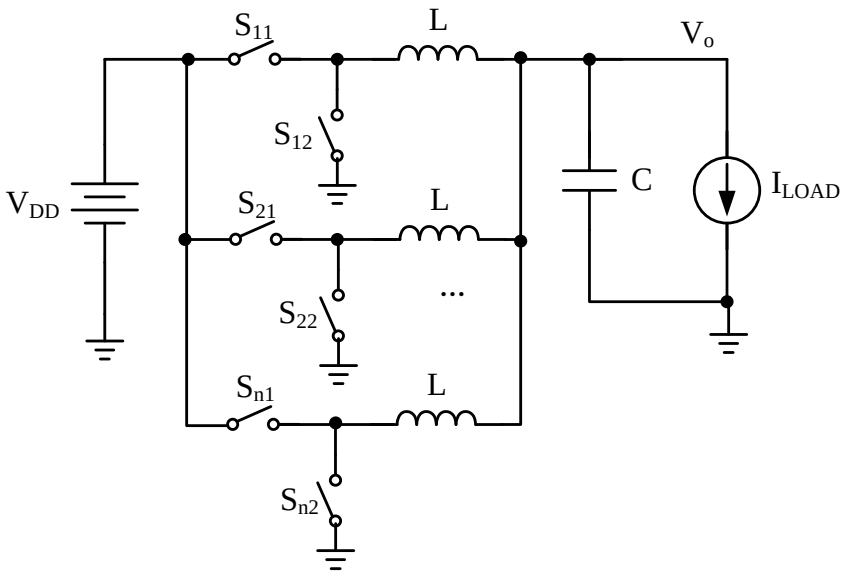


Figure 21. Schematic of a synchronous n-phase buck converter

The reported efficiencies of fully integrated buck converters are usually around 50%, which are much lower than off-chip buck converters. However, they still have a significant improvement over linear regulators such as LDOs which are also on chip. Except high switching frequency, low Q of on-chip inductor (typically 5 to 10) is also a limiting factor for the integrated converter achieving good efficiency. In [42], in-package bondwires with and without ferrite epoxy glob cores are used as the filter inductor in buck converter, showing very high saturation current and low DCR.

2.3.4 Single Inductor Multiple Output

Single inductor multiple output (SIMO) buck converter, which is shown in Figure 22, use only one inductor to generate several different voltage/current levels, thus it is a very suitable solution for power-management ICs where multiple voltage/current levels are required. Design challenges in this field include system stability, power efficiency, and cross regulation [43]-[45].

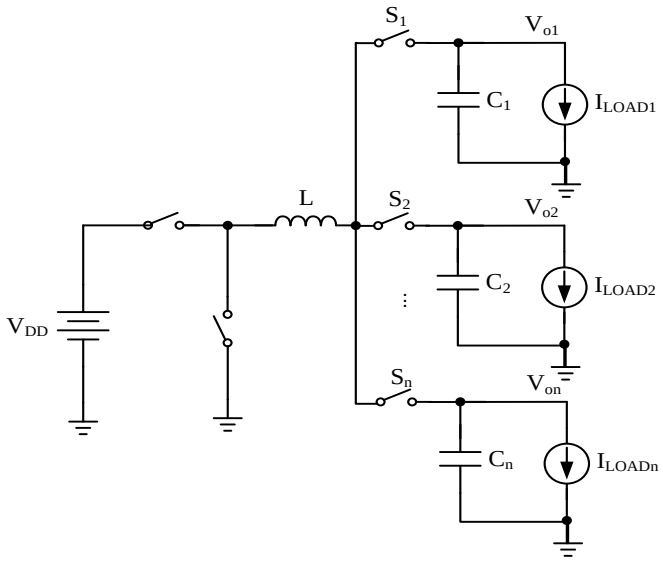


Figure 22. Schematic of single input multiple output buck converter

2.4 Light-Load Efficiency of Buck Converters

In order to optimize the efficiency in light load, the power loss mechanisms in the buck converter are discussed in the following sub-section.

2.4.1 Power Losses Analysis of Basic Buck Converter

The power losses of a basic buck converter are a combination of the losses caused by the power MOSFETs, output filter, control circuits and traces. Usually the power consumption of the control circuits is very small compared to the power consumption of the power train (including the power MOSFETs, MOSFET gate drivers, and output filter). Therefore, only the power losses of the power train components are considered in the following efficiency analysis. To help with the analysis, a parasitic circuit model has been presented in Figure 23 [3], [32], [4]-[49].

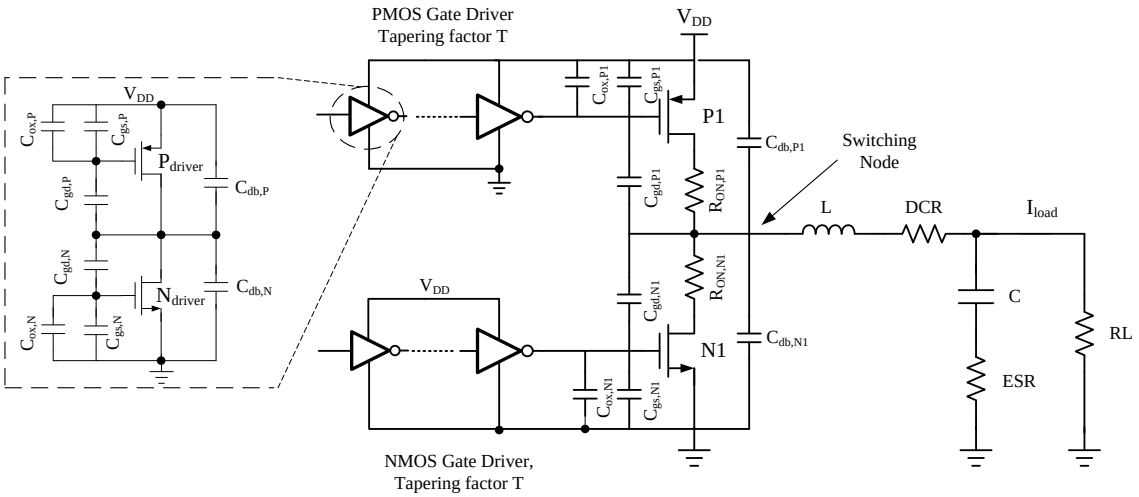


Figure 23. Circuit model for basic buck converter with parasitics

2.4.1.1 Power Stage Related Power Losses

Power stage includes power transistors and gate drivers. The power transistors are typically large in size with high parasitics. To control the operation of the power transistors, a chain of MOSFET gate drivers are required, which are tapered with a taping

factor T. The gate driver loss and power transistors loss will be analyses separately in the following.

Assuming that the control signal applied to P1 and N1 are non-overlapping, no short-circuit current flows through P1 and N1 during transition. The short-circuit power dissipated in the gate drivers is also neglected assuming the transition times of the input signal applied at each gate drivers are smaller than the output transition time [50].

The gate drivers consist of a chain of inverters. It is well known that the power dissipation of an inverter can be written as

$$P_{inv} = f_s C_p {V_{DD}}^2 \tag{2.13}$$

where f_s is the switching frequency, C_p is the parasitic capacitance, V_{DD} is the inverter supply voltage. Thus the gate drivers' loss can be expressed as

$$P_{driver} = f_s C_{driver} {V_{DD}}^2 \tag{2.14}$$

where C_{driver} is the total capacitance in driver chain, which includes transistor's gate oxide capacitor, gate-to-source/drain overlap capacitor, and drain-to-body junction capacitor. The largest portion in C_{driver} is the power transistor gate input capacitance.

The power losses of power MOSFETs in Buck converter are dominant by conduction losses and switching losses. Conduction loss is caused by the on-resistance of the transistors operating in linear region. When the MOSFET is on, it does not behave as an ideal switch with zero impedance, but it behaves as a small resistor, denoted by R_{on}. This loss can be expressed by:

$$P_c = i_{rms,P}^2 R_{on,P} + i_{rms,N}^2 R_{on,N} \tag{2.15}$$

$$i_{rms,P} = I_{load} \sqrt{D} \tag{2.16}$$

$$i_{rms,P} = I_{load}\sqrt{1-D} \tag{2.17}$$

where $i_{rms,P}$ and $i_{rms,N}$ are the root-mean-squared current through PMOS power transistor and NMOS power transistor respectively, $R_{on,P}$, $R_{on,N}$ denote the PMOS power transistor and NMOS power transistor on-resistance, D is duty cycle, and I_{load} is the load current. It is obvious that the conduction loss will be more significant at higher currents.

Switching losses occur as a result of the power required during the switches turn on and off. The dominant switching loss in power transistors *Ps,cap* is due to the dynamic power charging and discharging the parasitic capacitors of the switch node, which is given by:

$$P_{s,cap} = f_s C_p {V_{DD}}^2 \tag{2.18}$$

where C_p is the parasitic capacitance of power switches. Figure 23 shows that the parasitic capacitors contain the gate-to-drain overlap (Miller) capacitor, drain-to-body junction capacitor, and parasitic capacitance associate with the connection of off-chip inductor, which include a bonding pad, bonding wire, pin, and board interconnect capacitance.

The total power dissipation in power stage is given by a combination of the above described losses:

$$P_{tot} = P_{drv,P} + P_{drv,N} + P_c + P_{s,cap} \tag{2.19}$$

where $P_{drv,P}$ and $P_{drv,N}$ are the power dissipation of the driver circuit for PMOS power switch and NMOS power switch respectively.

2.4.1.2 Output Filter Related Power Losses

Some part of the total power losses in buck converter are due to the series resistance of the filter inductor and the effective series resistance (ESR) of the filter capacitor, as

shown in Figure 24. These parasitic resistances are in the range of several hundred milliohms, and contributing to i^2R losses [5]. In this project, the output filter uses off-chip components, whose parasitics are relatively fixed, thus this part of loss can only be reduced by selecting components with lower parasitics.

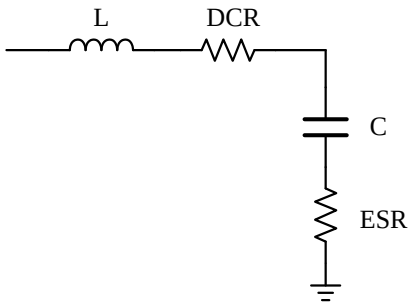


Figure 24. Output filter with parasitic resistance

2.4.2 Light-Load Efficiency

Through the power loss analysis, we know that as load decreases, the conduction losses reduces together with the square of load current, but the switching losses are a fixed amount of power irrespective of the load size. Therefore, the rapid drop during light load condition is mainly caused by switching losses. As stated in Section 2.3.3, higher switching frequencies are preferred to reduce the off-chip inductor and capacitor sizes, which however increase the switching losses (Figure 25), and make the efficiency in light load even worse.

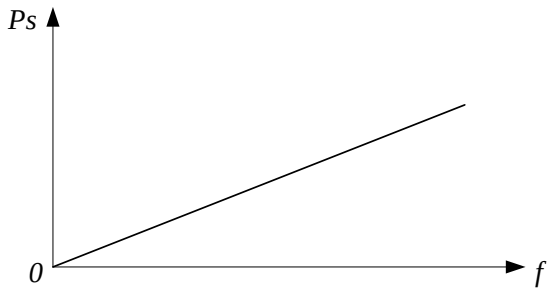


Figure 25. Switching losses vs switching frequency

3. METHODS TO IMPROVE LIGHT-LOAD EFFICIENCY

3.1 Previous Methods

Improving power efficiency of buck converters during light load becomes an essential requirement for battery-powered portable devices in order to gain power saving and extend battery life. Many techniques have been developed to mitigate this poor light-load efficiency problem. A review of several popular techniques is presented in the following.

3.1.1 PFM

The most frequently used method to improve light-load efficiency is to employ pulse frequency modulation (PFM) control mode [46], [51]-[59]. Since switching loss is proportional to switching frequency, by scaling down the switching frequency together with load current, PFM mode is able to reduce the switching losses, and maintains high light-load efficiency.

The main problem with PFM mode is high noise introduced by the changing switching frequencies. The varying switching frequency causes more severe EMI, making it unsuitable for noise-sensitive RF circuits in portable devices.

Usually both PFM mode and PWM mode are employed in one circuit. PFM mode is only used at light load, while at medium and heavy load, PWM mode is still preferred.

3.1.2 Pulse Skipping Mode

Another prevailing method in industry is pulse skipping modulation (PSM) [60]-[62]. As shown in Figure 26, in PSM mode, control signal will skip some clock cycles as the load decreases. Consequently, the equivalent switching frequency is reduced, resulting in

increased light-load efficiency. In this mode, each pulse cycle is still synchronized by the PWM clock, thus it has better EMI characteristic. Compared to PWM and PFM mode, PSM mode also has faster response speed, but the voltage ripple is larger, and the actual switching frequency of power transistors is easy to enter the audible noise range due to skipped cycles.

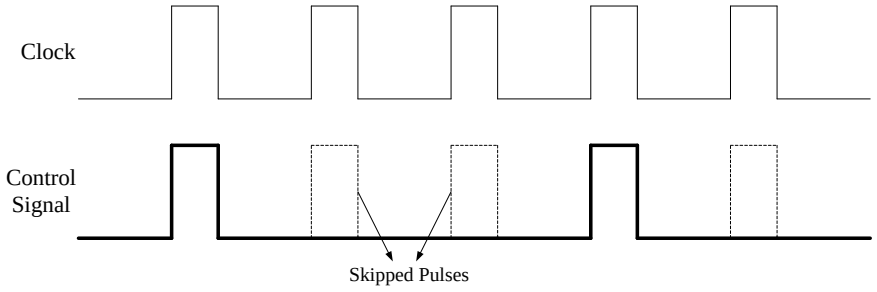


Figure 26. Pulse skipping mode

3.1.3 Burst Mode

Burst mode technique is also commonly used in improving light-load efficiency [63]. When configured for this mode and during light load, the converter will alternate between ON and OFF state. The control signal waveform is illustrated in Figure 27 [64]. During ON state, the controller bursts out a few pulses to maintain the charge voltage on the output capacitor. During OFF stare, it turns off the converter and goes into sleep mode with most of internal circuits shut down. Because no power is transferred during OFF stage, the output voltage begins to droop. The controller monitors the output voltage and after reaching a specified value, the converter eventually enters ON state delivering more current to replenish the output voltage. The action of switching transistors and other

unneeded portions of the converter circuit remain OFF significantly reduces power losses. One drawback of burst mode is an additional low frequency ripple added on the output voltage during ON state, as shown in Figure 28.

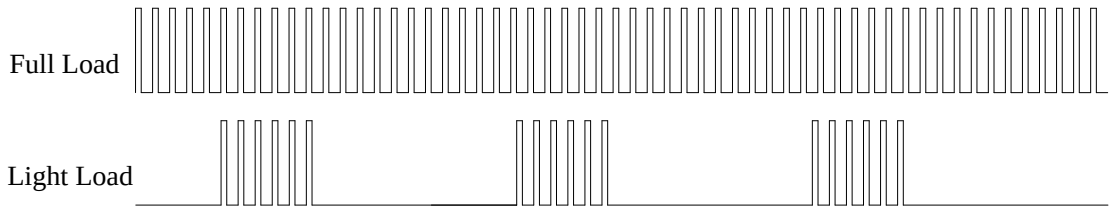


Figure 27. Burst mode control signal at light load

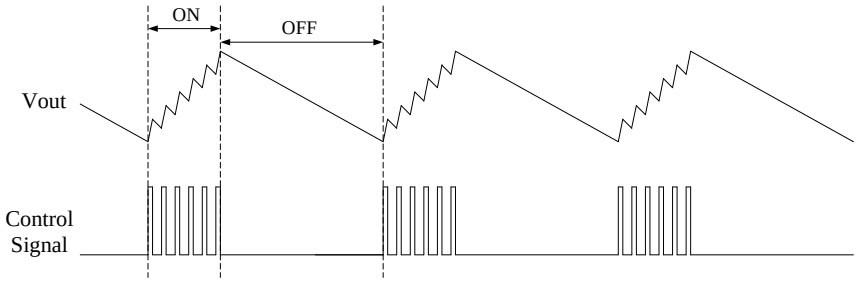


Figure 28. Burst mode output signal

3.1.4 Mode-Hopping

In mode-hopping technique, the buck converter operates in both synchronous and asynchronous modes. Under medium to heavy load conditions, it operates in synchronous mode which also means in continuous conduction mode (CCM), where the inductor current does not reach or go below zero. Under light load condition, it operates in asynchronous mode or in another word discontinuous conduction mode (DCM), by

turning off the synchronous rectifier when negative inductor current is detected, to mainly reduce conduction losses [46], [61], [65]-[66]. However, conduction losses are not the dominant power loss under light load condition, thus the efficiency improvement by this technique itself is limited. In addition, the changes in the buck converter model may lead to serious regulation or stability problem. To avoid this problem, design complexity is increased.

3.1.5 Gate Drive Technique

This technique is more popular in literature than in industry products [32], [67]-[77]. In [32], [67]-[68], a gate drive technique was presented whereby the gate voltage swing statically reduced or dynamically scales with load current such that the gate drive loss reduces at light load. In [69]-[73], resonant gate drivers were presented in order to recover the power loss due to gate charge, which has a significant efficiency improvement in high frequency converters, but generally requires components, such as inductors, capacitors, or transformer, that increase cost and hard to be integrated in standard CMOS processes. Presented in [34], [74]-[77], gate charge recycling doesn't reduce any factor that affect the gate drive loss directly, but it involves storing a portion of the gate charge in a capacitor during discharge phase, then re-using it during charging phase. The main problem with this technique is that it only reduces the gate-drive loss, but not the switching loss due to switch the switching node.

3.1.6 Other Techniques

There are several other techniques to get power loss reduction at light load condition, such as width controlling technique [47], [78]-[80], dead-time controlling technique [80]-[83].

In width controlling technique, the width of power MOSFET and the size of the driver are adjusted dynamically depending on load condition to save power. Since the device parasitics generally decrease linearly with decreased gate width, the switching loss can be reduced by using smaller width at light load. Figure 29 shows an example of how the width controlling is implemented.

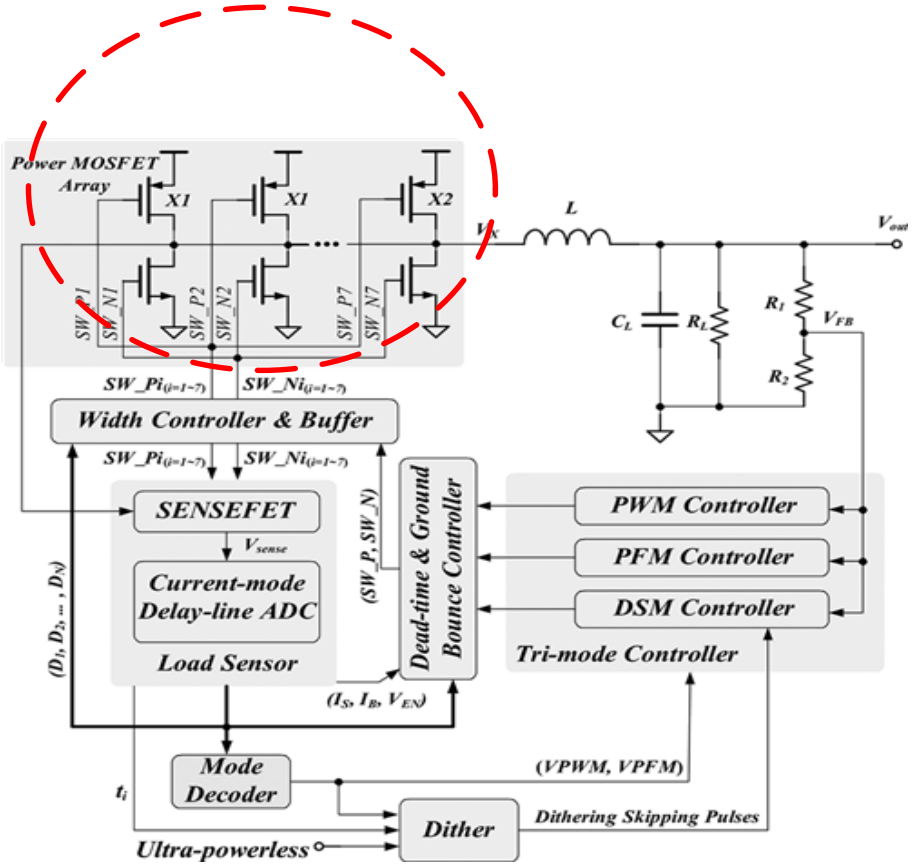


Figure 29. Buck converter with width controlling technique [80]

In dead-time controlling technique, since too short dead time turns power NMOS transistor on too early, leaking the energy directly to ground, not to load, while too long dead time conducts body diode of the NMOS power switch, increasing loss, optimum

dead time exists. Adjusting dead time according to the variation of load can optimize the power efficiency.

There is also technique which doesn't rely on control or active circuit variation, but increases the value of the filter inductor at light load, thereby achieving smaller inductor current ripple to reduce both conduction loss and switching loss [84].

3.2 Proposed Method

The basic idea of the proposed method is shown in Figure 30. The circuit topology is very similar with the conventional buck converter, only adds another voltage source VL between the source node of NMOS power switch and ground. We call the new topology a dual-supply buck converter.

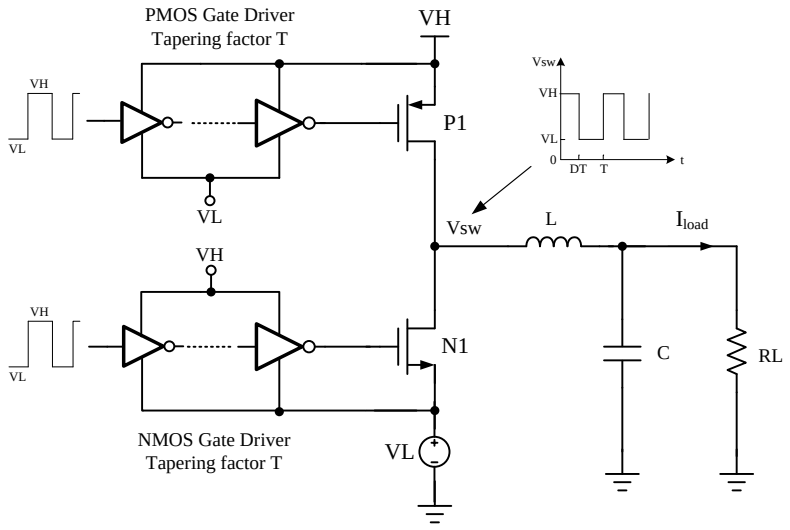


Figure 30. Basic idea of proposed dual-supply buck converter

As shown in Figure 30, now we have two voltage sources which are denoted as *VH* and *VL* respectively. Under medium and heavy load condition, the proposed buck

converter works exactly the same as conventional buck converter with $VH=V_{DD}$, and $VL=0$. Under light load condition, the operation of this buck converter is divided into two regions according to the output voltage:

(a). When output voltage is smaller than $V_{DD}/2$, let $VH=V_{DD}/2$, $VL=0$. The switching node voltage, as well as the gate driving voltage, is switching between 0 and $V_{DD}/2$.

(b). When output voltage is between $V_{DD}/2$ to V_{DD}, let $VH=V_{DD}$, $VL=V_{DD}/2$. The switching node voltage, as well as the gate driving voltage, is switching between $V_{DD}/2$ and V_{DD}.

With a switched capacitor converter providing the supply voltage of $V_{DD}/2$, the above operation can be simply described with Figure 31.

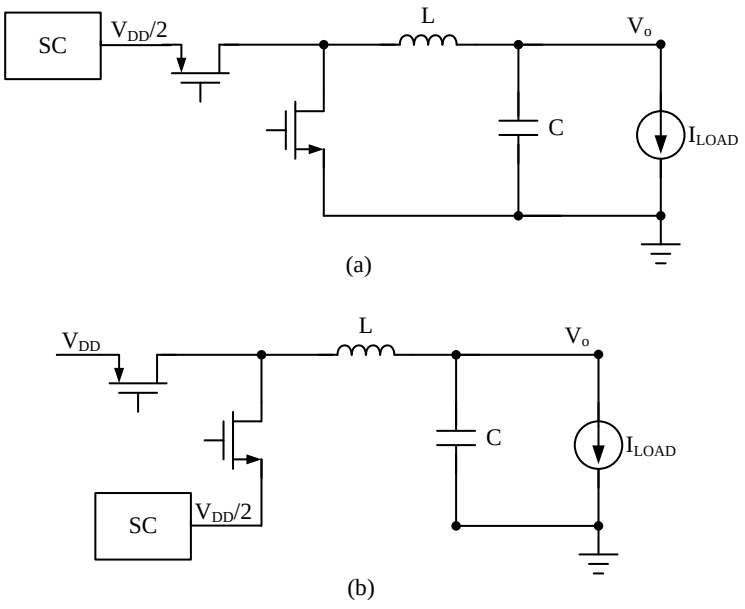


Figure 31. Simplified proposed buck converter schematic under light-load condition: (a). $Vo < V_{DD}/2$ (b). $V_{DD}/2 < Vo < V_{DD}$

The reason behind adding another voltage source to improve power efficiency can be explained according to the power stage losses expression which is given by Equation (2.19). The equations of three switching losses components, including $P_{s,cap}$, $P_{drv,P}$ and $P_{drv,N}$, should be modified when applied for this topology:

$$P_{s,cap} = f_s C_p (VH - VL)^2 \tag{3.1}$$

$$P_{drv,P} = f_s C_{driver,p} (VH - VL)^2 \tag{3.2}$$

$$P_{drv,N} = f_s C_{driver,N} (VH - VL)^2 \tag{3.3}$$

Between these three parts of switching losses, $P_{s,cap}$ is the dominant one, since the driver size is usually much smaller than the power transistor size, resulting in a much smaller parasitic capacitance than C_p. For power transistors, C_p can easily go to pF range.

Under light load condition, switching losses are dominant. In this project, both of the two working regions (region (a) and (b)) at the light load have reduced V_{DD} to *VH-VL*, which equals to $V_{DD}/2$. Thus switching losses quadratically reduce to ¼ of the original value, improving light-load efficiency. The following is an example of rough estimation of switching loss and efficiency. Assume C_p is 20pF, f_s is 1MHz, $VH - VL$ is 1V, then the switching loss is around 20μW. Also assuming load current is 0.1mA, output voltage is 0.5V, and MOSFET on-resistance is 0.2ohm, the efficiency will be 71.23%. While for a conventional Buck converter, under the same condition, switching loss will be 80μW, and efficiency will drop to 38.4%. The efficiency difference is as large as 32.83%.

Under medium and heavy load conditions, the power loss is dominant by conduction losses, which is given by Equation (2.15). In this equation, the MOSFET on-resistance R_{on} is given by:

$$R_{on} \propto \frac{1}{V_{gs} - V_{th}} = \frac{1}{VH - VL - V_{th}} \tag{3.4}$$

where V_{gs} is the voltage difference between transistor gate and source, and V_{th} is the transistor threshold voltage.

Equation (3.4) shows that smaller *VH-VL* is no longer good for efficiency if conduction losses dominant, because when V_{gs} reduces, R_{on} will increase, thereby deteriorating the efficiency at the medium and heavy load. To compensate for this, at the point where the buck converter with $VH\text{-}VL = V_{DD}/2$ is about to have lower efficiency than the one with $VH\text{-}VL = V_{DD}$, we switch the topology to conventional buck converter, that is to let $VH = V_{DD}$, and $VL = 0$.

3.3 Strengths and Weaknesses of Proposed Method

Compared with previously discussed method, the strengths of this proposed method lie in several points. First, the efficiency at light load is improved significantly. The results showing in Section 6 and Section 7 will confirm this argument. Secondly, the switching frequency in this project keeps constant, therefore smaller noise and EMI is achieved comparing with varying switching frequency. Thirdly, PWM method is employed over the entire load range, rather than changing to other control techniques at light load, simplifying the control design. Finally, the lower supply at light load will result in both smaller output voltage ripple and smaller inductor current ripple, thus a cleaner supply is obtained.

Besides, the proposed method is similar to gate swing scaling technique. As shown in Figure 32, compared to gate swing scaling technique, the proposed method not only scales the gate voltage by two, but also reduces the swing at the switching node to half of

the original value. Thus the switching loss due to charging and discharging the switching node is decreased, and improve the efficiency in further.

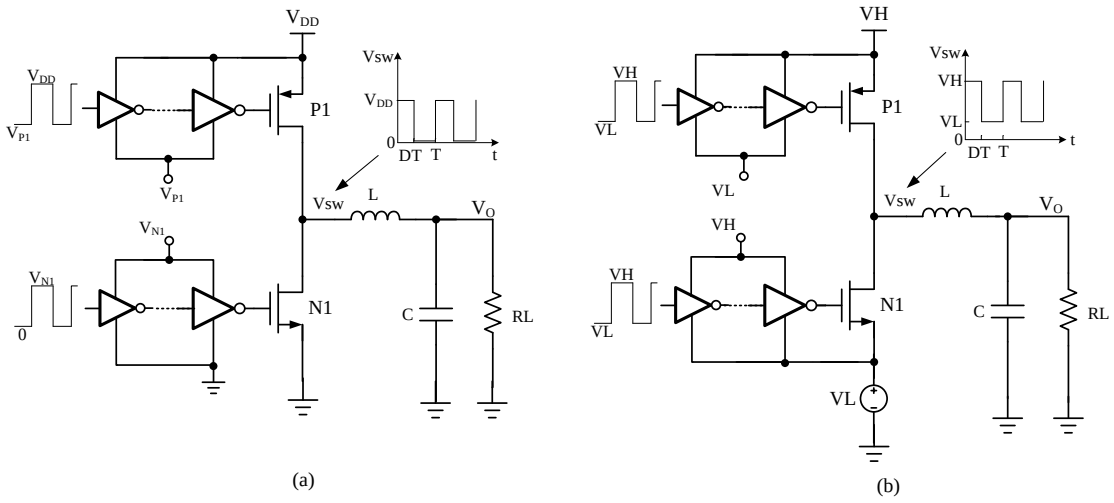


Figure 32. Buck converter with (a) gate swing scaling technique (b) proposed dual-supply technique

The weaknesses of this method show in several aspects. The design is more complicated due to the additional loop and SC converter. Two different supply voltage levels exist in the circuit and increase the complexity. Additionally, due to the transition between light load and medium load, the circuit transient response becomes slower.

4. SYSTEM ARCHITECTURE

4.1 Specifications

A buck converter with fixed input and output voltage is designed in this project with TSMC 0.18μm CMOS technology. The norminal supply for I/O transistors of TSMC 0.18μm technology, which is 3.3V, is chosen to be the input voltage. The output voltage is chosen to be 0.9V, thus the circuit is working in the first region mentioned before (*VH=VDD/2*, *VL=0*). If it operates in the second region, the circuit will be very similar, with main changes of SC circuit's output connection.

4.1.1 Choice of Switching Frequency

The range of switching frequency of buck converter changes from several kilo Hz to several Mega Hz. As switching frequency increases, the minimum size of the inductor to produce continuous current and the minimum size of the capacitor to limit output ripple both decrease. Therefore, high switching frequency is desirable to reduce the size of both the inductor and the capacitor. The tradeoff for using high switching frequency is the increased power loss in switches, which has been discussed in Section 2. In this project, switching frequency is chosen to be 3MHz.

4.1.2 Output Ripple

Output ripple is determined by the filter inductor and filter capacitor. The expression for inductor current ripple and output voltage ripple is given by Equation (2.7) and Equation (2.8) respectively. Ripple is undesired for generating a clean supply, since ripple in supply can cause clock jitter, increasing PSRR requirement for analog circuit. Filter with larger size in buck converter is able to achieve smaller the ripple, but it can

never suppress ripple to zero. Considering the trade-off between filter size (large filter means large area) and ripple amplitude, this design allows an output voltage ripple of around 1% of the average output voltage, and an inductor current ripple of around 1% of the maximum load current.

4.1.3 Load Regulation

Load regulation is a very important figure-of-merit in switching converters. Load regulation is defined as the change in the output voltage corresponding to sudden change in the load from minimum current to maximum current or the opposite direction.

When there is a step in the load current, controller will response to the change, and adjust the duty cycle to keep constant output voltage. The transient waveform of output voltage corresponding to the sudden current change is shown in Figure 33. When load current goes from minimum to maximum, the duty cycle needs to increase to compensate for the increased conduction losses. However, the change of duty cycle needs some time, the lower duty cycle results in an output voltage undershoot. Similarly, when load current drops from maximum value to minimum value, the extra current provided by source will flow to the output capacitor, resulting in an output voltage overshoot. The output voltage recovery time is determined by the controller speed. The undershoot/overshoot voltage is given by:

$$V_{shoot} = \frac{I_{MAX} - I_{MIN}}{C} \cdot \Delta t + (I_{MAX} - I_{MIN}) \cdot ESR \tag{4.1}$$

where I_{MAX} is the maximum load current, I_{MIN} is the minimum load current, C is the output capacitance, Δt is the time that the load current changes from minimum to maximum or the other way around, and ESR is the parasitic resistance of the output capacitor.

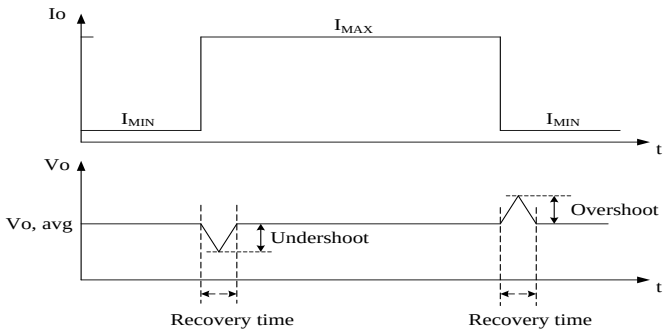


Figure 33. Load transient response

4.1.4 Specifications Summation

Table 2 sums the specifications of the proposed buck converter.

Table 2. Specifications of the proposed buck converter

Parameters	Specs	
Technology	TSMC 0.18μm CMOS	
V_{DD}	3.3V	
V_{OUT}	0.9V	
Fs	3MHz	
I_O	1mA ~ 400mA	
Δi_L	40mA	
Δv	10mV	
Load Regulation	Undershoot/Overshoot	50mV
	Recovery time	50μs

4.2 System Architecture

This section describes the architecture of the proposed buck converter. Figure 34 is the proposed buck converter system. As described in the previous section, at medium and heavy load, supply voltage is V_{DD}, and at light load, supply voltage is $V_{DD}/2$. The simplified schematic is shown in Figure 35.

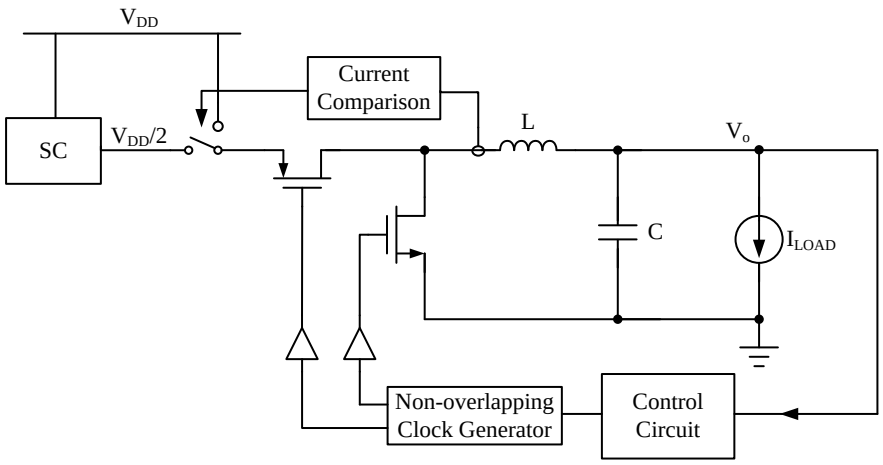


Figure 34. System architecture of the proposed buck converter

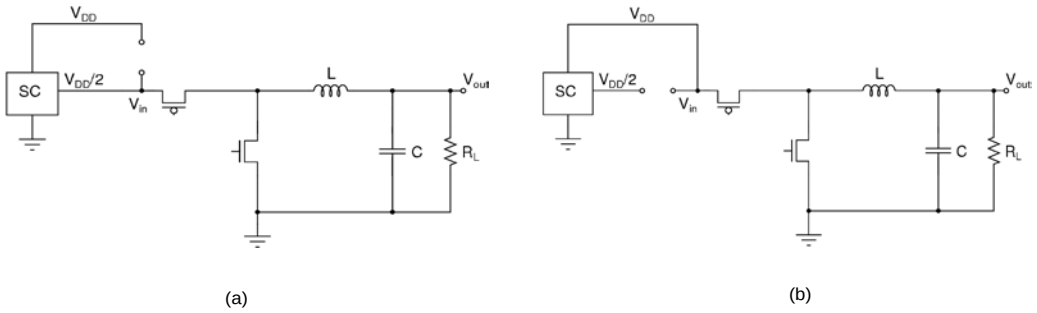


Figure 35. Simplified buck converter schematic at (a). light load (b). medium and heavy load

In Figure 34, the buck converter has a voltage control loop and a current control loop. The voltage control loop is employed to keep output voltage constant. It should provide good loop stability and good load transient performance. The current control loop compares the buck converter output current with a certain reference current to switch the supply between $V_{DD}/2$ and V_{DD}, which means switching between proposed topology with the conventional one according to load condition. The current threshold is set to optimize efficiency over the entire load range. The switched-capacitor (SC) converter is used to provide the $V_{DD}/2$ supply the circuit needs.

Assume the efficiency of buck converter with supply V_{DD} is η_1, and with supply $V_{DD}/2$ is η_2. Also assuming the SC converter efficiency is η_{SC}, the efficiency of overall system is given by:

$$\eta = \begin{cases} \eta_2 \cdot \eta_{SC} & \text{light load;} \\ \eta_1 & \text{medium and heavy load} \end{cases} \tag{4.2}$$

From Equation (4.2), the SC circuit should design at very high efficiency to minimize extra power losses in the whole system. The following section talks about some basics of SC converter.

4.3 PWM Mode and Control Method

The control circuit in switching DC-DC converters is used to regulate the voltage variation in the load by modulating the duty cycle. In ideal converters, the output voltage is only a function of the input voltage and duty cycle. But in practical circuits with non-ideal components, the output is also a function of the load current because of the parasitic resistance in series with the components.

There are mainly two kinds of pulse modulation techniques in DC-DC converters: pulse width modulation (PWM) and pulse frequency modulation (PFM). PWM is a kind of method that keeping constant frequency during the operating, while changing the switch's on time. PFM keeps constant switch's on time, while changes the switching frequency. Both of the methods can change duty cycle, thus changing the output voltage. The major problem with PFM is the unpredictable EMI due to the varying switching frequencies. PWM is more popular because the harmonics in output voltage is constant, and much easier to be filtered out.

In PWM mode, depending on the control signals required, the control methods are divided into two kinds: voltage mode and current mode. Voltage mode control derives its control signal from the output voltage of the switching converters, and it is simple to implement, but has slower loop response. Current mode control utilizes information from both the output voltage and the inductor current to determine the desired duty cycle. Due to the direct feedback path from inductor current, current mode has faster response, but it is more complicated and more sensitive to noise. In this project, voltage mode control is adopted, since fast response is not a must here.

Voltage mode control compares the converter's output voltage with a reference and converters the error to a duty cycle. The simplified diagram is shown in Figure 36. If the converter output voltage tends to be greater than the reference voltage, the output voltage of the error amplifier will drop and the duration for which the output of comparator remains at high will decrease. Thus the duty cycle reduces and the output of the converter would fall. This is how this negative feedback control loop maintains the output at the desired value. Figure 37 explains the way that the PWM waveform is generated through

the comparison of error voltage and the triangle wave. And it also shows that the PWM waveform frequency, which also means the switching frequency, is determined by the triangle wave frequency.

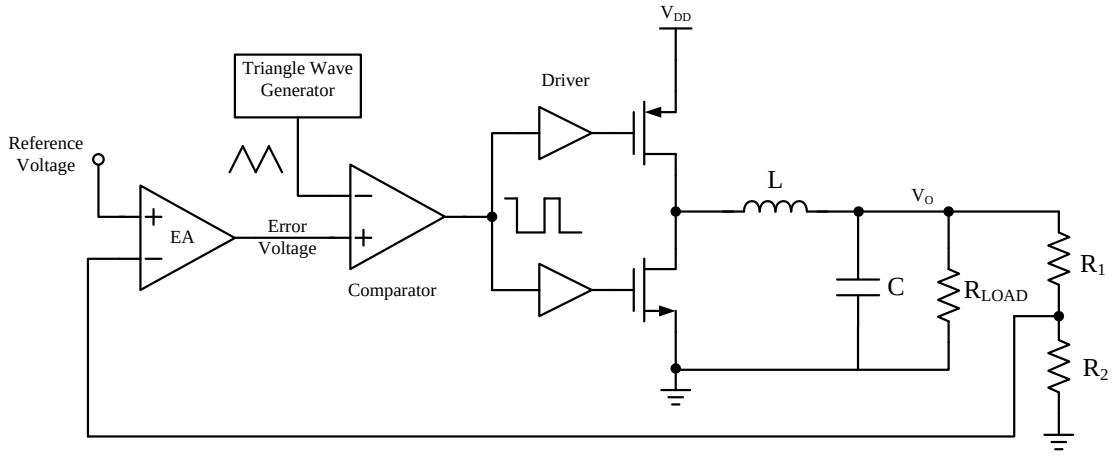


Figure 36. Voltage mode control diagram

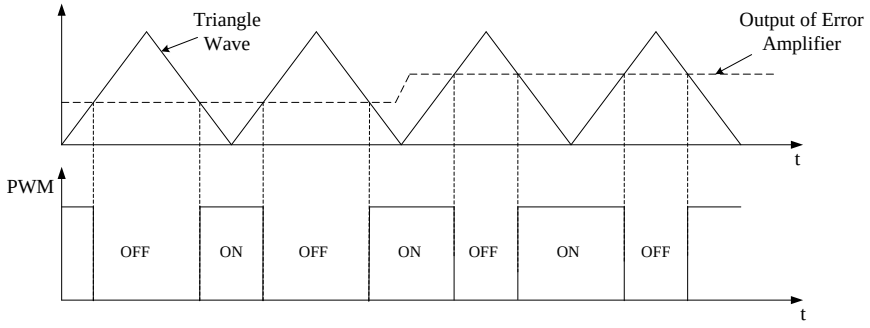


Figure 37. PWM waveform

For a negative feedback loop, loop stability needs to be checked. In open loop, a phase margin of at least 45^o is a commonly used criterion for good stability. In addition, sufficient bandwidth must be designed to assure that the converter will have good

transient response. Start the analysis from the output filter in the power stage, which is a second order filter consisting of an inductor and a capacitor. After including the DC resistance (DCR) of the inductor and Equivalent Series Resistance (ESR) of the capacitor, the equivalent circuit of output filter is shown in Figure 38.

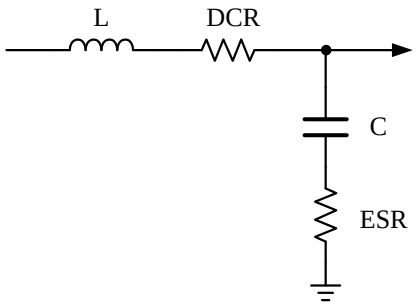


Figure 38. Output filter with parasitic resistance

The transfer function of filter can be expressed by

$$H(s)_{filter} = \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot (ESR + DCR) \cdot C + s^2 \cdot L \cdot C} \tag{4.3}$$

All the other circuit in the loop excluding the output filter can be modeled as a simple gain stage. Assume the amplitude of the triangle wave is ΔV_{osc}, and the supply for the switch is V_{DD}, then the gain stage transfer function is given by

$$H(s)_{gain} = \frac{V_{DD}}{\Delta V_{osc}} \tag{4.4}$$

Thus, the overall open loop transfer function is

$$H(s)_{loop} = \frac{V_{DD}}{\Delta V_{osc}} \cdot \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot (ESR + DCR) \cdot C + s^2 \cdot L \cdot C} \tag{4.5}$$

Since the parasitic resistance ESR and DCR are relatively small, the loop can be approximated as having double poles f_{LC} at

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \tag{4.6}$$

and one zero f_{ESR} at

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C} \tag{4.7}$$

Figure 39 shows the open loop frequency response. The gain is flat at DC, and then due to the double poles effect, the gain begins to roll off at -40dB/decade, and phase curve falls down towards –180°. After reaching this point where a zero is located, the gain curve slope changes to –20 dB/decade and the phase curve turns back towards –90°. The zero frequency f_{ESR} is much higher than f_{LC}, resulting in a poor phase margin. The low DC gain, poor phase margin, and small bandwidth problem necessitate the compensation network.

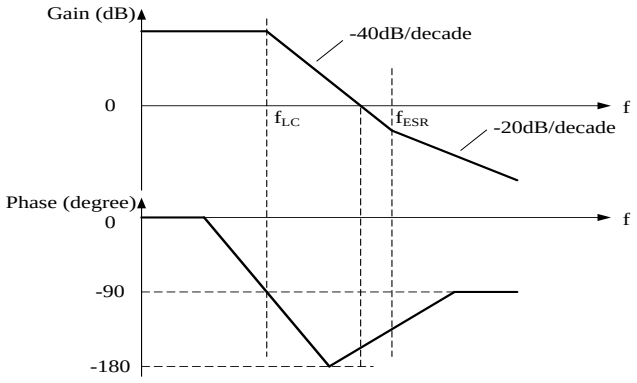


Figure 39. Frequency response of the open loop buck converter

In this project, type III compensation [85]-[88], which can give superior transient response, is implemented. The compensation circuit is given in Figure 40. It is realized

by adding resistors and capacitors around the error amplifier. The transfer function of type III compensation is:

$$H(s)_{TYPEIII} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot (s + \frac{1}{(R_1 + R_3) \cdot C_3})}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot (s + \frac{1}{R_3 \cdot C_3})} \tag{4.8}$$

Figure 41 gives the frequency response of type III compensation network. The pole at the origin provides high DC gain. Two zeros boost the phase by 180^o, and then a pole cancels the ESR zero. A final pole rolls off the high frequency gain.

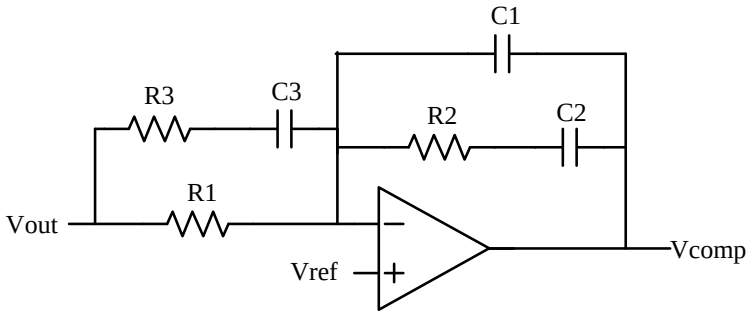


Figure 40. Type III compensation network

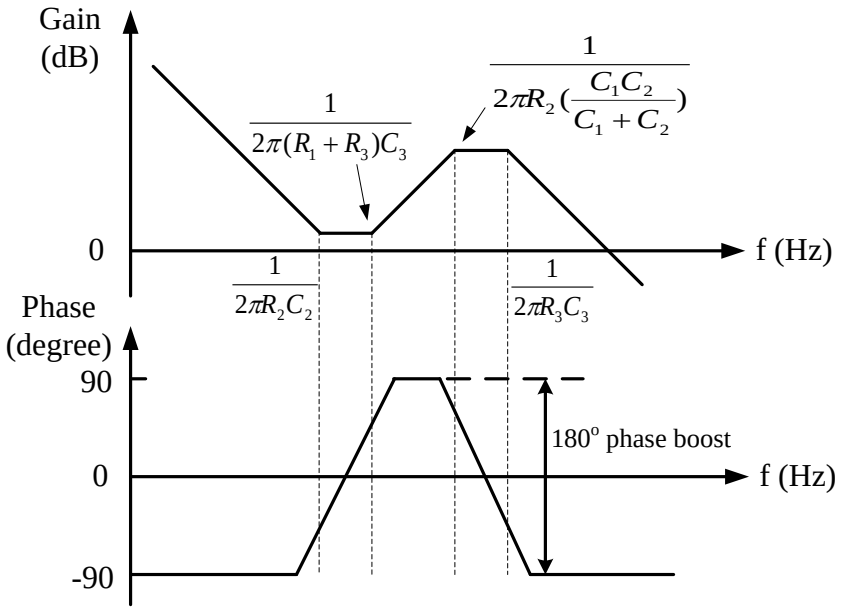


Figure 41. Frequency response of type III compensation network

Figure 42 shows the close loop circuit after adding compensation. By positioning the poles and zeroes at proper places, the overall loop bandwidth can be extended, and phase margin can be larger than 45 degree. In general, the loop bandwidth should be high enough to provide good dynamic regulation and low enough to avoid sub-harmonic instability and noise amplification [88]. Practically, the loop cutoff frequency *fc* is desired to be 1/5 to 1/10 of switching frequency *fs*.

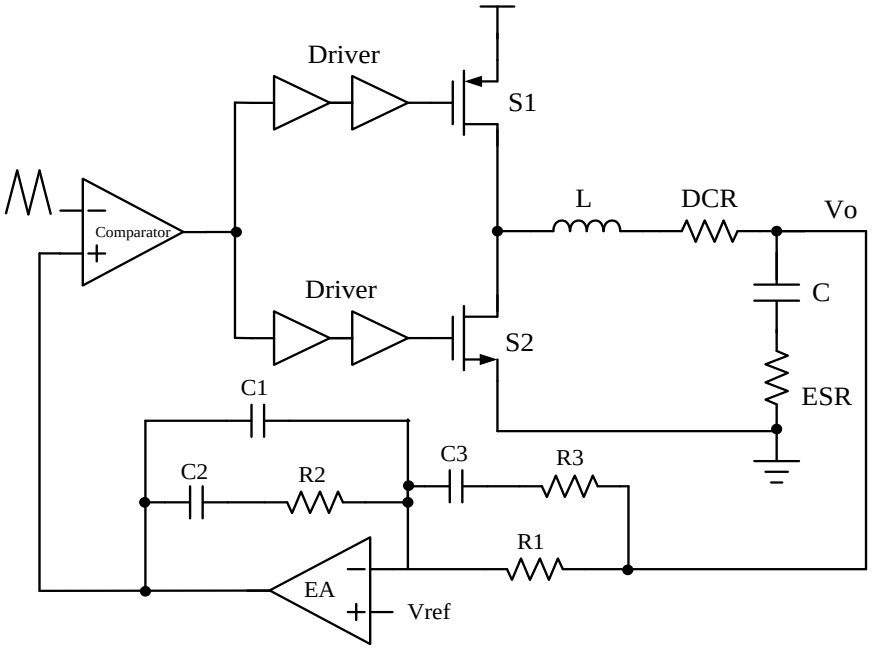


Figure 42 Close loop buck converter

[86] provides a guideline for positioning the poles and zeroes and for calculating the value of compensation resistances and capacitances. Following those steps, the frequency response after compensation as shown in Figure 43 can be obtained.

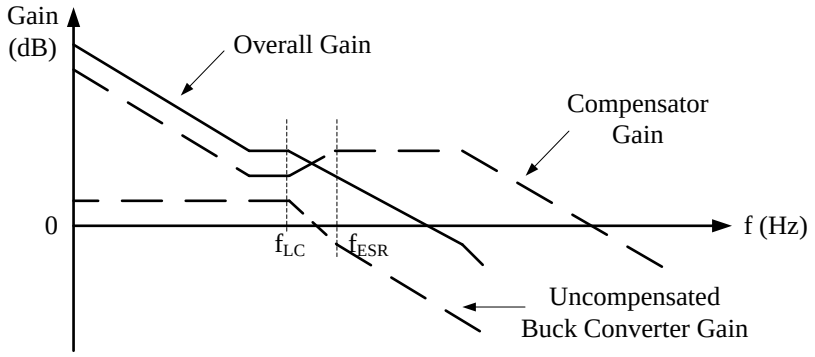


Figure 43. Frequency response after compensation

4.4 Current Sensing Technique

Current sensing technique is widely used in buck converters. It is usually used for current-mode and boundary control, over-current protection, current sharing etc. Depending on applications, the average, peak, root mean square, or total waveform of the current signal needs to be measured. In this project, the value of average load current is needed. The followings summarize the commonly used current sensing techniques, and the advantages and disadvantages are compared.

A. Series sense resistor

This method is the most conventional way for current sensing. In Figure 44, a resistor Rsense is placed in series with the inductor. If the value of the resistor is known, the current flowing through the inductor is determined by sensing the voltage cross it:

$$i_L(t) = \frac{V_{sense}(t)}{R_{sense}} \tag{4.9}$$

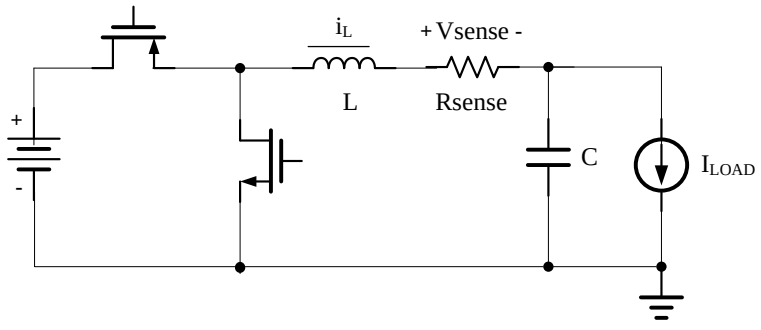


Figure 44. Current sensing with series sense resistor

This method is used in power factor correction and over current protection due to its simplicity and accuracy. The drawbacks of this technique are the power loss by Rsense,

poor accuracy, providing no measurement isolated from transient voltage potentials on the load, etc.

B. R_{DS} sensing

A lossless MOSFET drain-source resistor (R_{DS}) method for current sensing is depicted in Figure 45. MOSFETs act as resistors when they are “on”, and the equivalent resistance is known as:

$$R_{DS} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{4.10}$$

where μ is the mobility, C_{ox} is the oxide capacitance, and V_{th} is the MOSFET threshold voltage. Therefore, it is possible to determine its current by measuring its drain-source voltage:

$$i_L = \frac{V_{sense}}{R_{DS}} \quad (when\ MOSFET\ is\ on) \tag{4.11}$$

When MOSFET is on, the inductor current is equal to the measured MOSFET current. When the MOSFET is off, if needed, a sample-and-hold circuit can be added to reconstruct the inductor current.

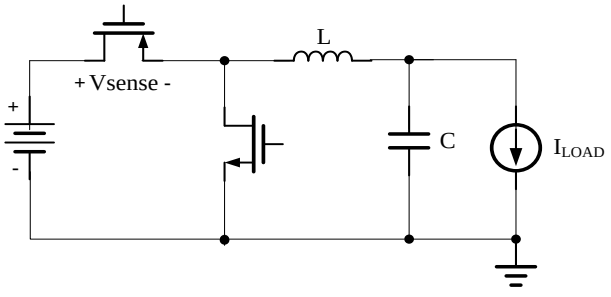


Figure 45. Current sensing with R_{DS} of MOSFET

This technique eliminates the need of additional sensing resistor. The main drawback is the nonlinearity of R_{DS}, which may have a variance of -50% to 100% across process and temperature because of μC_{ox} and V_{th}, resulting in poor sensing accuracy.

C. Filter based current sensing

This technique is based on the equivalent series resistance of inductor, known as DCR. As shown in Figure 46, an RC filter is added in parallel with the inductor.

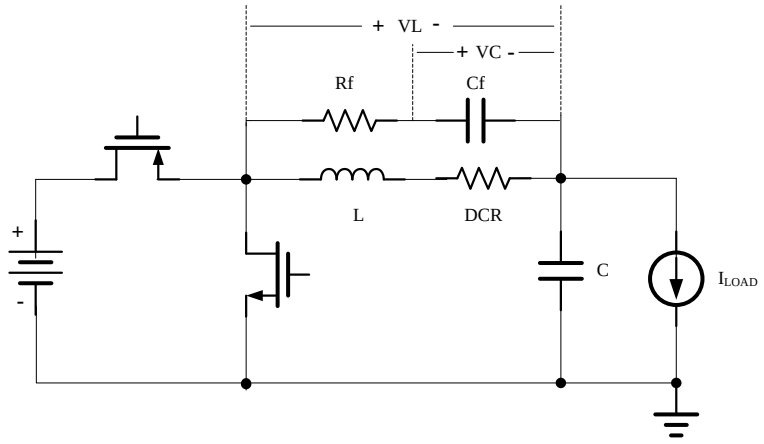


Figure 46. Current sensing with filter

The voltage across the inductor is given by

$$VL = (sL + DCR) \cdot i_L \tag{4.12}$$

The voltage across the capacitor Cf is

$$\begin{aligned} VC &= \frac{VL}{1 + s \cdot Rf \cdot Cf} = \frac{(sL + DCR) \cdot i_L}{1 + s \cdot Rf \cdot Cf} = DCR \cdot \frac{1 + s(L/DCR)}{1 + s \cdot Rf \cdot Cf} \cdot i_L \\ &= DCR \cdot \frac{1 + sT}{1 + sT_1} \cdot i_L \end{aligned} \tag{4.13}$$

where $T=L/DCR$, and $T_1=Rf*Cf$. Forcing $T=T_1$, yields $VC=DCR*i_L$ and VC would be directly proportional to i_L.

This technique is popular due to its accuracy, losslessness, low noise sensitivity, and high bandwidth, continuous current measurement, and low cost. The drawback of this technique is that the value of L and DCR need to be known to choose proper Rf and Cf, which makes this technique only fit for converter with off-chip inductor. Another drawback of this technique is the small value of sensed signal. For example, VC can be in the range of several millivolt, which is hard to process.

D. Filter based average current sensing

This technique is applied to applications where only the information of average inductor current is needed. As shown in Figure 47, the RC filter is connected across the low-side switch S2.

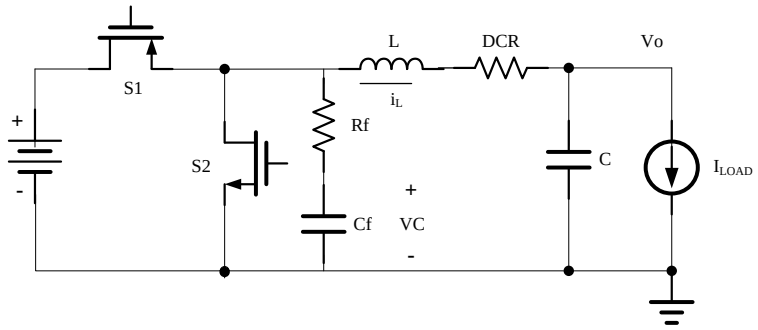


Figure 47. Filter based average current sensing

Under steady state, the average voltage on Rf is zero, thus the output average current is derived as

$$I_o = \overline{I_L} = \frac{\overline{VC} - V_o}{DCR} \tag{4.14}$$

where $\overline{VC}$ is the average voltage across *Cf*. The measurement result is only dependent on the value of *DCR*. The value of *Rf* must be selected to be much greater than the internal resistance of the switches. Another requirement is to make sure that

$$Rf \cdot Cf \gg switching\ frequency \tag{4.15}$$

The drawback of this technique is DCR should be known, and it provides information only about average current.

E. SENSEFETs

As shown in Figure 48, a sensing FET (SENSEFET, S1') is built in parallel with the power MOSFET (S1). Switch S1' has the same length as S1 and relatively smaller width to provide a small sensing signal proportional to the switch S1 current. N is the predetermined width ration of the switch S1' to switch S1, and is on the order of 100-1000. When N increases, the sensing accuracy decreases due to mismatch between transistors. When N decreases, the power loss caused by switch S1' will increase.

$$I_{sense} = \frac{I_{s1}}{N} \tag{4.16}$$

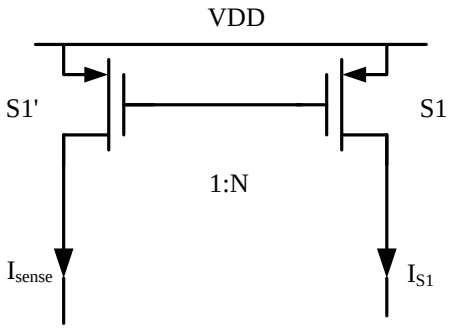


Figure 48. SENSEFET

In Buck converter, S1 can be either high-side switch or low-side switch. A complete current sensing circuit by sensing high-side switch current is shown in Figure 49. The OpAmp is added to force the drain voltages of both switches equal, therefore the current mirror non-ideality resulting from channel length modulation would be eliminated. When connecting the OpAmp inputs, the loop stability should be considered. The sensed current is feed into a resistor Rsense to convert into voltage.

$$V_{sense} = R_{sense} \times I_{sense} \tag{4.17}$$

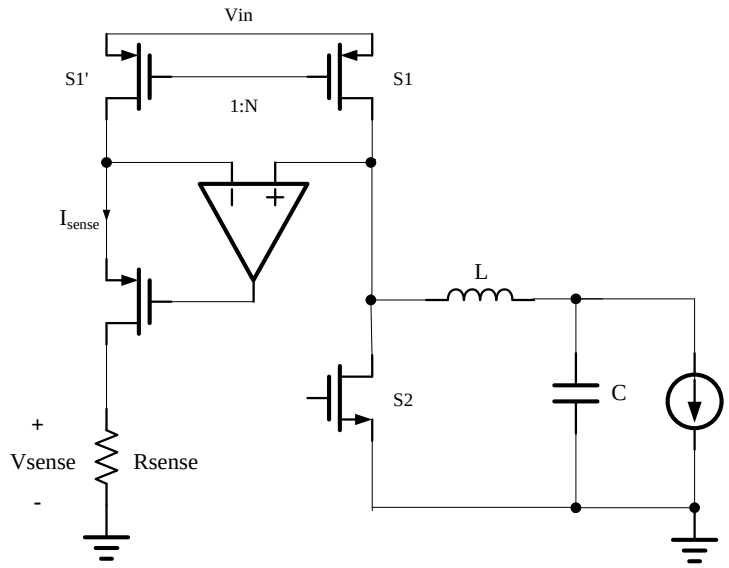


Figure 49. A more accurate circuit using SENSEFET technology

In this project, the requirements for the current sensing circuit are sensing average output current, and small power consumption. The accuracy requirement is not so critical, since the sensed current would be compared with a current threshold which is provided from off-chip, and can be adjusted.

Considering the above mentioned technologies, a modified version of SENSEFET technology is employed in this project [89]. As shown in Figure 50, currents of both PMOS power transistor and NMOS power transistor are sensed. For PMOS power transistor current sensing, when the aspect ratio of power switch to the sense transistor is *N:1*, the sensing current I_{ps} is proportional to the output current I_{pp} and can be described as:

$$\frac{I_{ps}}{I_{pp}} = \frac{1}{N} \tag{4.18}$$

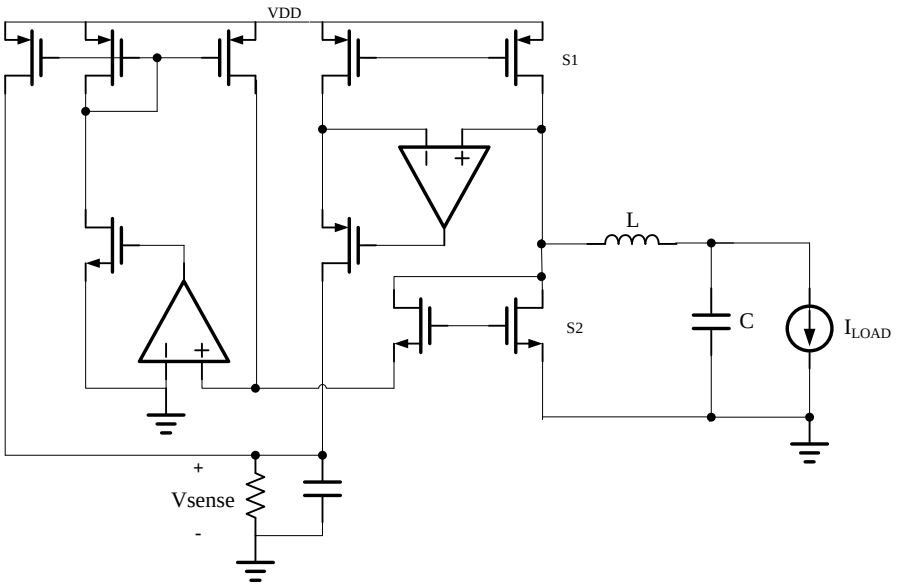


Figure 50. Current sensing circuit used in this project

For NMOS power transistor current sensing, when the aspect ratio of power switch to the sense transistor is N-1:1, the sensing current I_{ns} is proportional to the output current I_{np} and can be obtained as:

$$\frac{I_{ns}}{I_{np}} = \frac{1}{N} \tag{4.19}$$

Then output current of sensing circuit I_{sense} is the summation of currents I_{ps} and I_{ns}, and can be written as:

$$\frac{Isense}{I_L} = \frac{I_{ps} + I_{ns}}{I_{pp} + I_{np}} = \frac{1}{N} \tag{4.20}$$

The resistor converts sensing current into voltage. The capacitor filters out the current ripple to get average current.

4.5 Switched-Capacitor Converters

Figure 51 shows the double phase architecture switched-capacitor voltage divider. It is an improved version of the single phase architecture as mentioned in Section 2.2.2.2. Two basic SC cells connected in parallel between input and output. The two cells are operated in anti-phase, which means when one cell is in mode 1, the other cell is in mode 2, and vice versa. Theoretically, output voltage ripples caused by two cells will cancel each other, as shown in Figure 52, thus by using interleaving, input current and output voltage waveforms with small ripple are obtained. The average output voltage V_{OUT} is given by:

$$V_{OUT} = \frac{C_1}{C_1 + C_2} \cdot V_{IN} \tag{4.21}$$

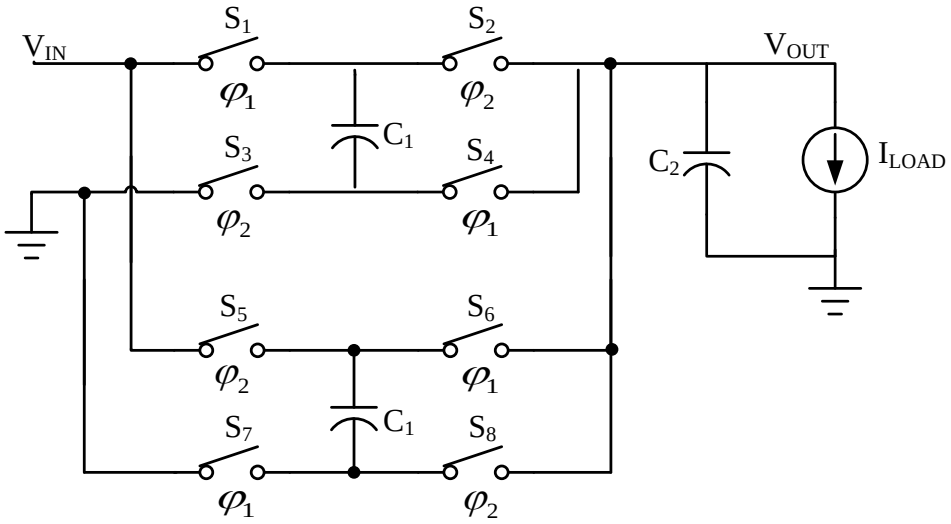


Figure 51. Typical switched-capacitor voltage divider with interleaved operation

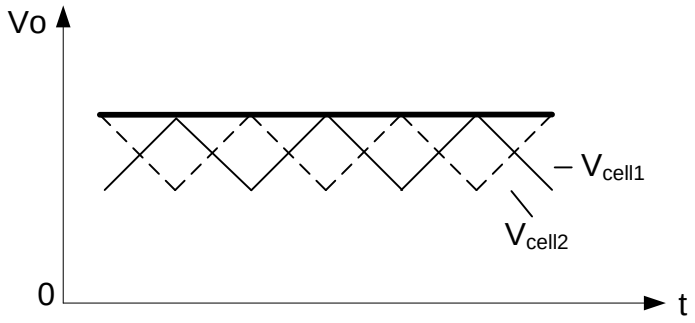


Figure 52. Output ripple cancellation with interleaved operation

5. CIRCUIT IMPLEMENTAION

This section discusses the design details of the proposed buck converter. In TSMC 0.18um process, two kinds of transistors exist. One is transistor with nominal supply of 3.3V, which is able to handle high voltage, and the other is transistor with nominal supply of 1.8V, which has smaller minimum width and length, thus can achieve smaller parasitic capacitance and faster speed.

In this buck converter, three voltage domains exist, VDDH (3.3V), VDDH/2 (1.65V), and VDDL (1.8V). VDDH and VDDL are directly provided from off chip, VDDH/2 is generated from SC converter. Most control circuits are working under VDDL domain, with low voltage transistors, for faster speed. The power stage and SC converter are working either in VDDH domain (at medium and heavy load) or VDDH/2 domain (at light load), and built with high voltage transistors. For these circuits changing between different voltage domains, level shifter is needed.

5.1 Power Train

Redraw the power train part in Figure 53. It includes the gate drivers, power transistors, output inductor and output capacitor as mentioned before.

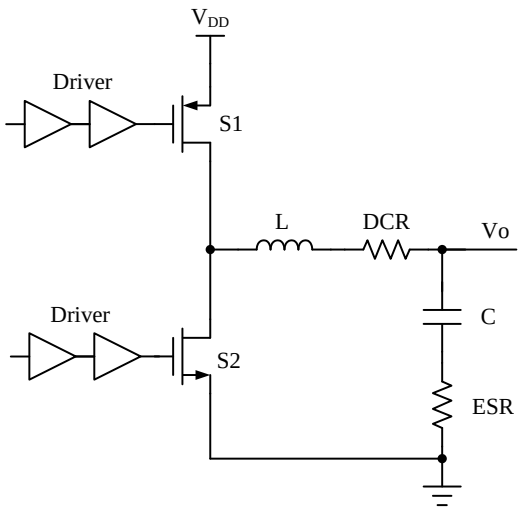


Figure 53. Power chain

5.1.1 Power Stage Design

The power stage consists of power switches and their gate drivers. It is well known that minimum propagation delay can be achieved when the tapering factor is the constant e. However, for a buck converter power stage design, the main concern lies not in the propagation delay of the gate drivers, but the energy dissipation. According to the power losses analysis in Section 2, the efficiency of buck converter is directly related to the sizes and taping factor of power switches and drivers. The trade-off is: if large area devices are chosen, they have smaller on-resistance, and thus smaller conduction loss, but switching loss will increase due to the large parasitic capacitance, and vice versa. Thus, for a specific load current and switching frequency, optimum sizes and stages of these transistors exist. In this project, switching frequency is fixed; however, load current has a wide range, from 1mA to 400mA. To achieve high efficiency over the entire load range, the design is optimized for medium load, which means peak efficiency is at 200mA.

According to [90], the power efficiency (η) can rewrite as a function of PMOS power transistor width *Wp* and duty cycle *D* (minimum transistor length is used):

$$\eta(W_p, D) = \frac{P_{out}(D)}{P_{out}(D) + P_c(W_p, D) + P_s(W_p, D) + P_q} \tag{5.1}$$

where P_q is the quiescent power consumed by control circuit.

Maximum efficiency can be achieved when

$$\frac{\partial}{\partial W_p}\eta(W_p) = 0 \tag{5.2}$$

According to [90], it is desirable to design the power stage optimized to a range of duty cycles. The average power efficiency over the range of *D1* to *D2* is

$$\eta_{ave}(W_p) = \frac{1}{D_2 - D_1}\int_{D_1}^{D_2} \eta(W_p, D)dD \tag{5.3}$$

Solving the following equation

$$\frac{\partial}{\partial W_p}\eta_{ave}(W_p) = 0, \tag{5.4}$$

the PMOS power transistor width can be obtained. In this project, Equation (5.4) is solved with the aid of Matlab, the optimized PMOS transistor width is 16mm, with an on resistance of 0.25 ohm, and the taping factor is 43. According to the ratio between PMOS and NMOS in a given process, which is 3 here, NMOS power transistor width can be calculated. Finally, according to the taping factor T, the sizes of drivers are determined.

Significant current will flow through the power transistors, therefore special attention should be paid on layout of the power transistors. Metal paths between drain and source should be minimized, since the metal resistance will add up to the power transistors' on resistance, and result in higher power loss. In this project, same width and same length are used for PMOS and NMOS unit cells. Due to the potential large

magnitude of substrate current injection, every six unit cells are grouped together, surrounded with their own guard ring to eliminate latch-up. The floorplan is illustrated in Figure 54.

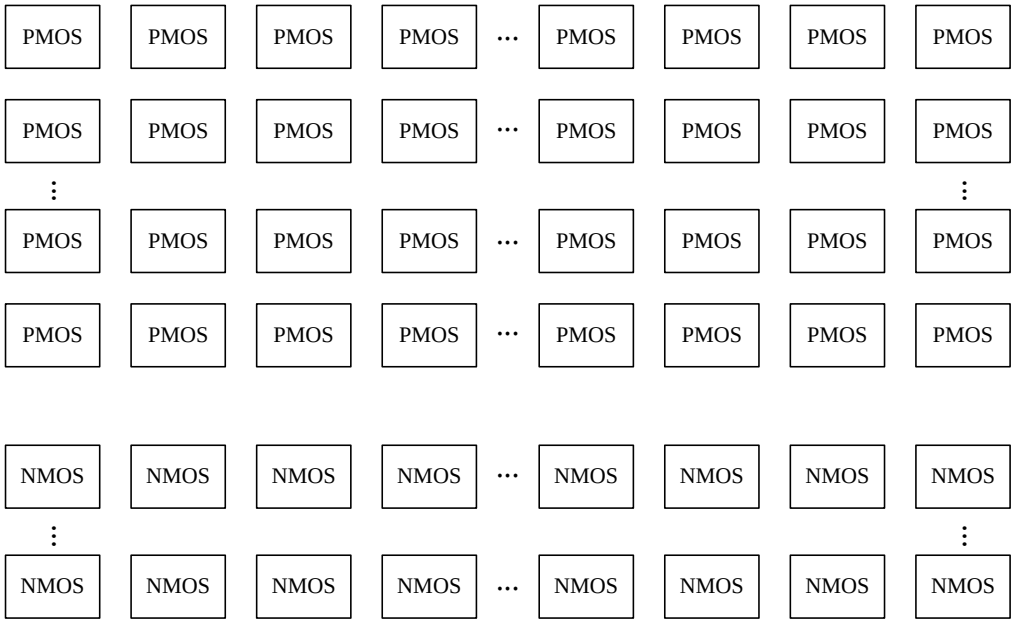


Figure 54. Layout floorplan of power transistors

Further adjust the transistor sizes according to the layout requirement, and the finalized transistor sizes are listed in Table 3.

Table 3. Transistor sizes of the buck converter power stage

Transistor	W (μm)	L (μm)	Multiplier
S1	5.92	0.35	2844
S2	5.92	0.35	948
Driver (first stage) PMOS	0.89	0.35	6
Driver (first stage) NMOS	0.89	0.35	2
Driver (second stage) PMOS	5.92	0.35	54
Driver (second stage) NMOS	5.92	0.35	18

5.1.2 Output Filter Design

Output filter consists of output inductor and output capacitor. According to the analysis in Section 2, the inductor value can be chosen based on the required current ripple Δi_L:

$$L = \frac{V_{DD}(1-D)}{2 \cdot \Delta i_L \cdot f_s} \cdot D \tag{5.5}$$

Output inductor should be larger than or at least equal to the value calculated by Equation (5.5).

The output capacitor is selected to meet the output voltage ripple specification and to provide storage for load transients. According to output voltage ripple requirement, the capacitor value can be calculated by

$$C = \frac{(1-D)D}{16L\Delta V_o f_s^2} \cdot V_{DD} \tag{5.6}$$

According to undershoot/overshoot voltage during load transient, since the Equivalent Series Resistance (ESR) of the output capacitance also contributes to the undershoot/overshoot voltage, the voltage is given by

$$\Delta V = \frac{\Delta i_C \cdot \Delta t}{C} + \Delta i_C \cdot ESR \tag{5.7}$$

A larger value capacitor is chosen to fulfill both Equation (5.6) and Equation (5.7). We can see lower ESR is preferred for lower undershoot/overshoot voltage. Compared with aluminum electrolytic and tantalum capacitors, ceramic capacitors are more often used because of their small size, low ESR, and high RMS current capability.

Equivalent Series Inductance (ESL) of the output capacitor can be a problem at high frequencies (>1MHz), because at higher frequency, the capacitor no longer behaves as a capacitor. This problem can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

The characteristic of selected inductor and capacitor are summarized in Table 4.

Table 4. Output filter size

Component	Value	Parasitic Resistance
L	3.6 µH	85 mΩ
C	12 µF	30 mΩ

5.2 Voltage Control Loop

Figure 55 shows the circuit implementation of buck converter with voltage control loop. The main building blocks include compensator (error amplifier, resistors and capacitors), comparator, triangle wave generator, non-overlapping clock generator and level shifters. This section will explain the function and show the transistor level schematic of each block.

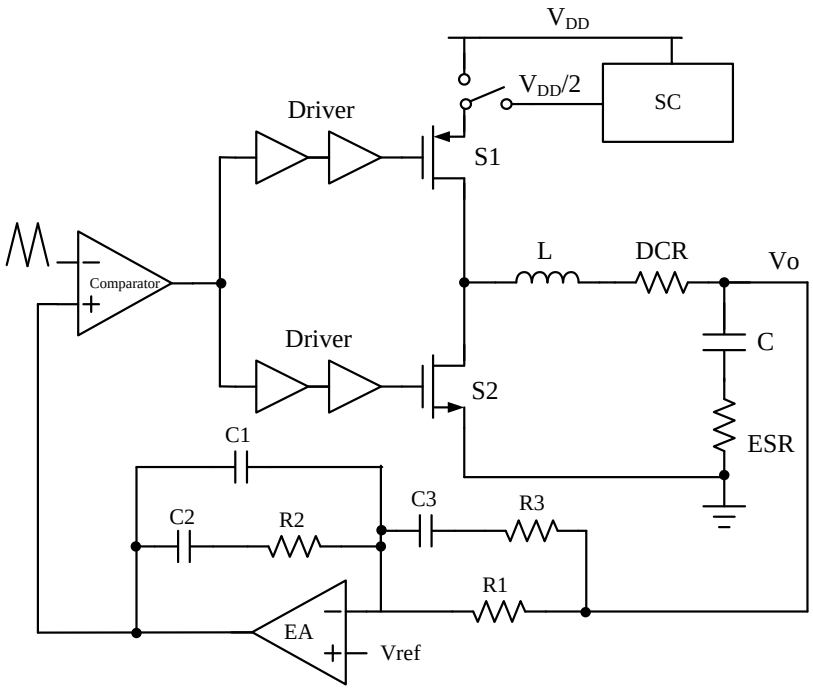


Figure 55. Buck converter with voltage control loop

Following the procedure provided in [86], the voltage control loop can be designed easily. In this project, the loop bandwidth is set to 1/10 of the switching frequency, which is 300 KHz. Notice that, according to the loop transfer function, the loop is affected by the supply, which is a varied value (3.3V or 1.65V) in this project. With a higher supply, the loop gain and loop bandwidth will be higher, resulting in a smaller phase margin. Thus the loop is designed with V_{DD} equal to 3.3V to guarantee its stability under both supply levels. To get feasible resistors' and capacitors' values for on-chip implementation, triangle wave amplitude is designed to be 0.5V. The compensation components' values are listed in Table 5.

Table 5. Compensation components value

Component	Value
R1	320KΩ
R2	1.03MΩ
R3	16KΩ
C1	3.2pF
C2	12.8pF
C3	16pF

5.2.1 Voltage Loop Macromodel

Before going to transistor level design, setup a macromodel for the buck converter with voltage control loop will help to decide specifications for each block. As shown in Figure 56, the macromodel is built in Cadence. It is mainly used for examining the AC performance of the loop. The voltage source *Vdc* in Figure 56 is added only for simulation purpose. *Cb* is a decoupling capacitor used to block DC. Figure 57 shows the macromodel of error amplifier, in which the voltage-control-voltage-source (VCVS) gain is the amplifier DC gain, and *Ramp* and *Camp* determine the amplifier bandwidth. The comparator and power stage are modeled with a VCVS, whose gain is given by

$$H_{gain} = \frac{V_{DD}}{\Delta V_{osc}} \tag{5.8}$$

where ΔV_{osc} is the triangle wave amplitude, which is 0.5V; V_{DD} is the supply voltage.

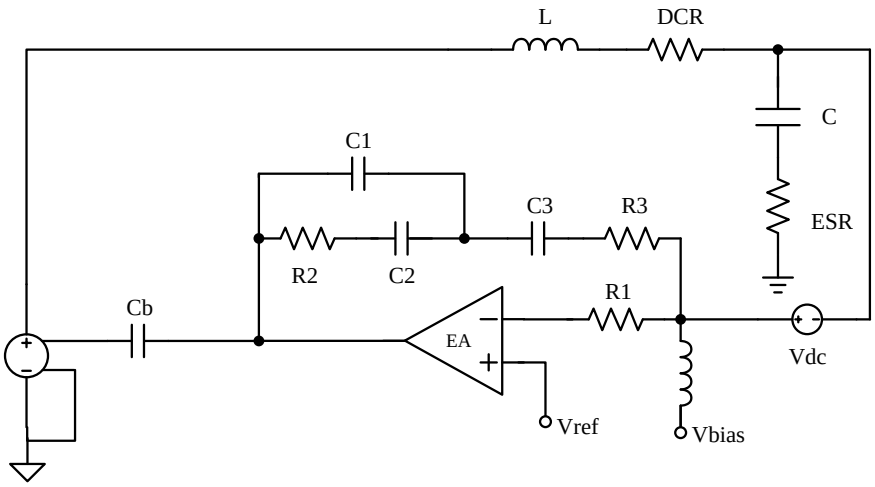


Figure 56. Buck converter voltage loop macromodel

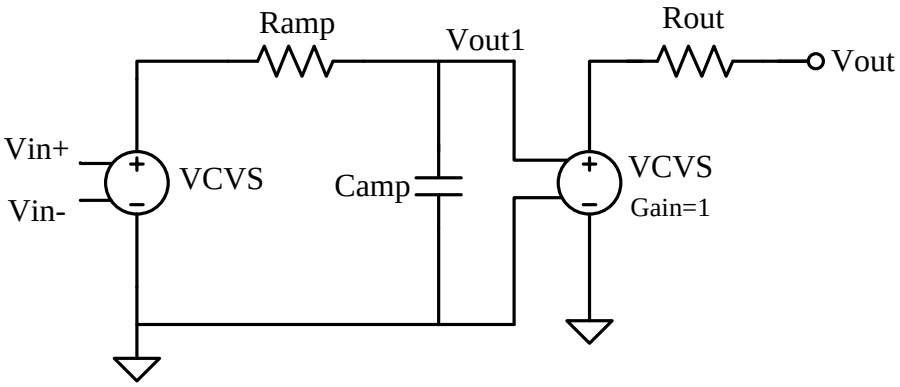
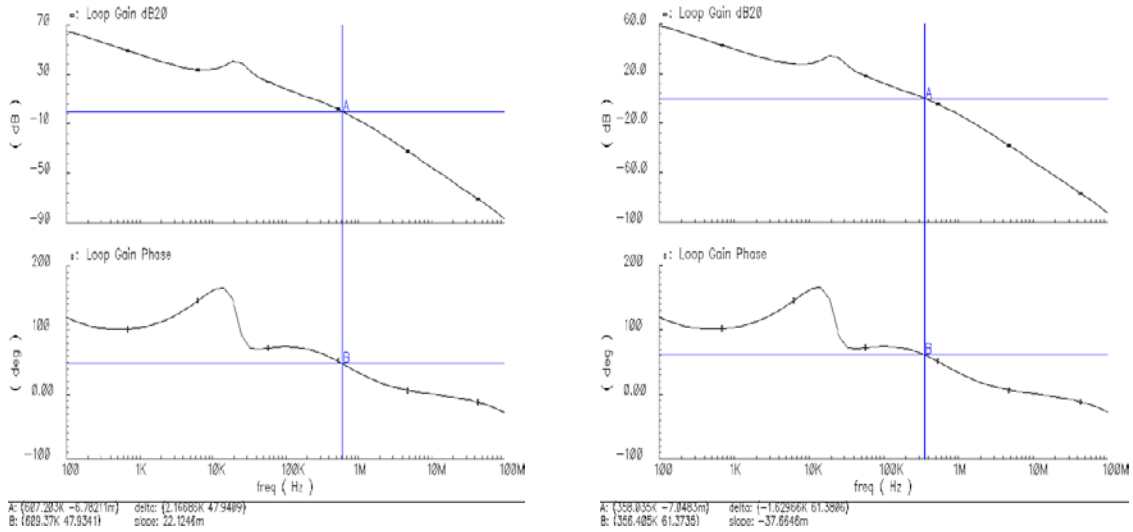


Figure 57. Opamp macromodel with one dominant pole

The AC response given in Figure 58 shows good loop performance with high gain, appropriate bandwidth and enough phase margin. The simulation results for both supply levels are summarized in Table 6. As expected, a higher bandwidth and smaller phase margin under 3.3V supply than under 1.65V supply are observed. To achieve this performance, the error amplifier is assumed to have a gain of 60dB and GBW of 150MHz.



(a) (b)

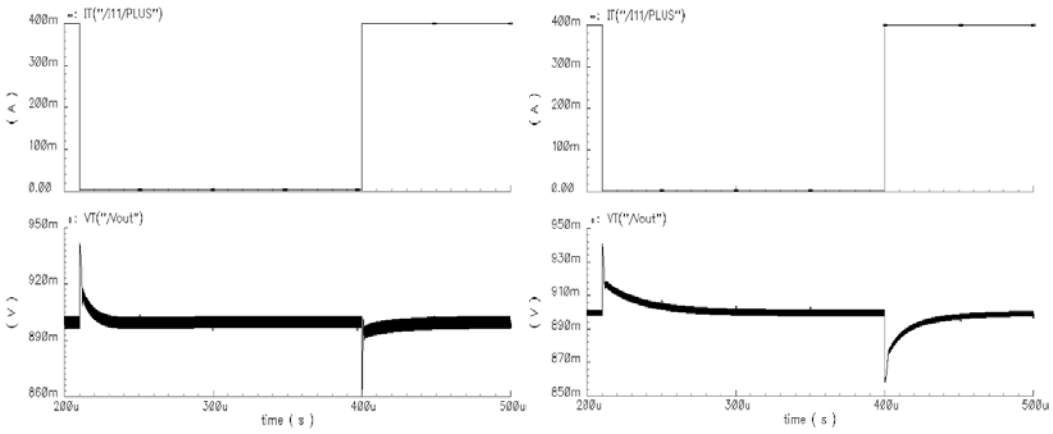
Figure 58. AC response of the voltage control loop

(a). Supply is 3.3V (b). Supply is 1.65V

Table 6. AC performance of the voltage control loop

Supply	GBW	Phase Margin
3.3V	607KHz	48°
1.65V	358KHz	61°

The loop performance is further justified through transient analysis with the power transistors and drivers in transistor level, while the error amplifier and comparator in ideal model. Assuming the load is changed from minimum (1mA) to maximum (400mA) or from maximum to minimum in 50ns, the transient responses under both supply levels are tested respectively, as shown in Figure 59.



(a) (b)

Figure 59. Transient response of voltage control loop

(a). Supply is 3.3V (b). Supply is 1.65V

Table 7 and Table 8 summarize the transient performance. The recovery time of 1.65V supply is longer than that of 3.3V, due to the smaller loop bandwidth.

Table 7. Load transient of conventional converter (3.3V)

Overshoot voltage	41.6mV	Recovery time (1%) (400mA→1mA)	5.5μs
Undershoot voltage	37.2mV	Recovery time (1%) (1mA→400mA)	0.57μs

Table 8. Load transient of proposed converter (1.65V)

Overshoot voltage	40.6mV	Recovery time (1%) (400mA→1mA)	17μs
Undershoot voltage	40.6mV	Recovery time (1%) (1mA→400mA)	17μs

The loop response meets all the requirements. The blocks in transistor level design will be shown in the following sections.

5.2.2 Error Amplifier

Error amplifier is implemented by folded-cascode architecture [91]. The schematic is shown in Figure 60. It is a one stage amplifier with high DC gain. Only one dominant pole is located at the output node, thus no compensation is needed for stability. The small-signal voltage gain is

$$A_v = \frac{G_m R_o}{1 + \frac{s}{\omega_0}} \tag{5.9}$$

where G_m is the transconductance, R_o is the output resistance, and ω_0 is the dominant pole.

The transconductance G_m is given by:

$$G_m = g_{m1} = g_{m2} \tag{5.10}$$

where $g_{m1}$and g_{m2} are the transconductance of transistor M1 and M2 respectively.

The output resistance R_o is given by:

$$R_o \approx [g_{m8}(r_{o2}||r_{o10})r_{o8}]||(g_{m6}r_{o4}r_{o6}) \tag{5.11}$$

where $g_{m6}$and g_{m8} are the transconductance of transistors M6 and M8 respectively, r_{o2}, r_{o4}, r_{o6}, r_{o8}, and r_{o10} are the output resistance of transistors M2, M4, M6, M8 and M10 respectively.

The dominant pole ω_0 is located at:

$$\omega_0 = \frac{1}{R_o C_L} \tag{5.12}$$

where C_L is the amplifier load capacitance.

Table 9 shows the simulation results of the error amplifier.

Table 9. Performance summary of error amplifier

Parameter	Specs
DC Gain	72dB
GBW	131MHz
Phase Margin	45^{o}
PSRR	104dB
Current Consumption (Without Bias Circuit)	30µA

In this project, PMOS input pair is preferred over NMOS input pair for better noise performance. Also the PMOS input pair bulks are connected to source to isolate noise from substrate.

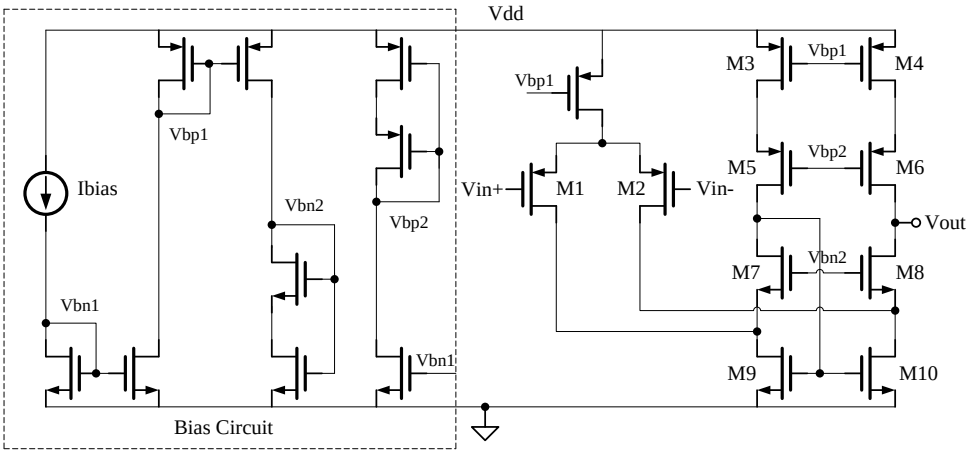


Figure 60. Error amplifier

5.2.3 Ramp Generator

Ramp generator is divided into two kinds: saw tooth wave generator [92]-[95] and triangle wave generator [96], [97]. Figure 61 shows the basic topology of saw tooth wave generator. Assume the saw tooth wave frequency is f_{st}, and its period is T_{st} ($1/f_{st}$). In one period, the circuit charges a capacitor C by constant current *I*, and discharge very quickly through a transistor. The charging rate is given by the following equation:

$$\frac{du}{dt} = \frac{I}{C} \tag{5.13}$$

Thus, if the output voltage amplitude is fixed, the switching frequency can change by tuning the bias current *I*.

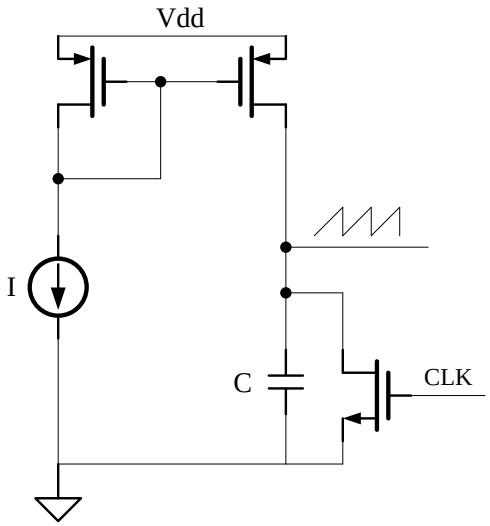


Figure 61. Saw tooth wave generator

Triangle wave generator is the one employed here. To generate a triangle wave, the only change from saw tooth wave generator is to control the output voltage charging and

discharging symmetric. As shown in Figure 62, the current mirror mirrors same amount of current to the discharging path as to the charging path. Since the current and load capacitor determine output voltage changing rate, the charging and discharging rate will be equal. The subsequence digital circuits provide the control signals for the switches, thereby setting the upper limit (VH) and lower limit (VL) of the triangle wave amplitude, the peak to peak value is given by

$$V_{pp} = VH - VL \tag{5.14}$$

If the triangle wave period is *Ts*, then according to Equation (5.13), we can get:

$$\frac{V_{pp}}{\frac{Ts}{2}} = \frac{I}{C} \tag{5.15}$$

The triangle wave frequency *fs* is given by:

$$f_s = \frac{2I}{C \cdot V_{pp}} \tag{5.16}$$

The two comparators in Figure 62 are hysteresis comparators, which will be described in the next section.

Reset signal is a startup signal that helps the circuit to start oscillation. By forcing reset to be “1”, OR gate output is set to “1”, and then forcing reset to be “0”, OR gate output will only be determined by input from SR latch, and starts to oscillate.

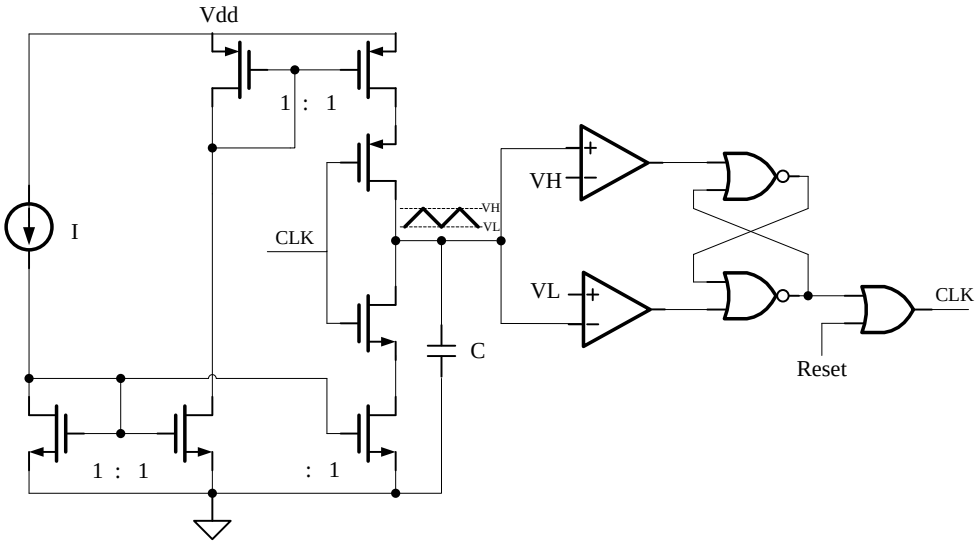


Figure 62. Triangle wave generator

5.2.4 Hysteresis Comparator

For a comparator, a small amount of noise or interference combined with input signal can cause undesirable rapid changes in output. Therefore, a comparator with hysteresis is always needed to improve the stability and noise immunity. Hysteresis means in the comparator, the input threshold voltage changes as a function of the input level. As illustrated in Figure 63, the input starts from negative and goes to positive, the output does not change until it reaches the positive threshold *Vth+*. When the input returns in the negative direction, the output does not switch until it reaches the negative threshold *Vth-*. The advantage of hysteresis can be illustrated in Figure 64. The one with hysteresis is more immune to noise.

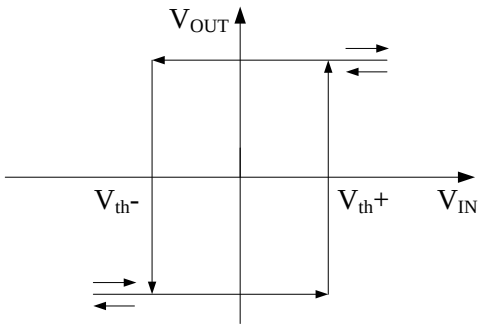


Figure 63. Comparator transfer function curve with hysteresis

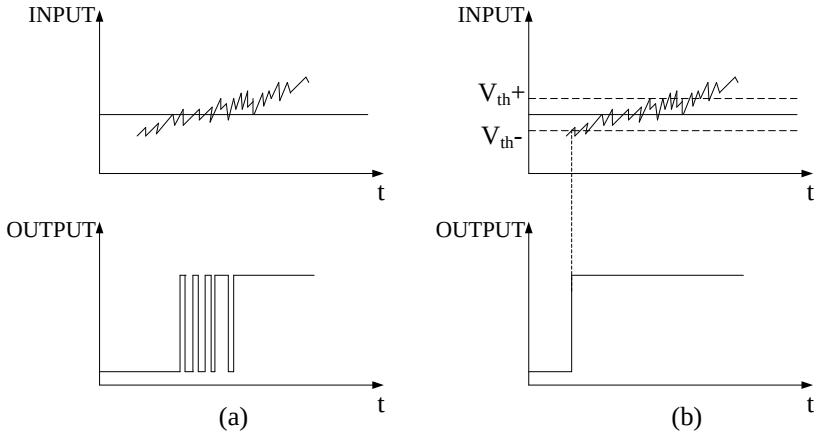


Figure 64. Comparator response to a noisy input (a).without hysteresis (b). with hysteresis

In this project, hysteresis comparators are used in the modulator in voltage control loop, the triangle-wave generator circuit and in current sensing loop. Figure 65 shows a 2-stage, high-gain, open-loop hysteresis Comparator, which is implemented by source-coupled differential input pair with internal positive feedback [92], [98]-[99]. In this circuit, there are two paths of feedback; one is negative feedback which is current-series feedback through the common-source node of transistor, and the other one is positive

feedback which is the voltage-shunt feedback through the gate-drain connections of transistor M6 and M7. When the positive feedback is stronger than the negative-feedback, the overall feedback will be positive and hysteresis will result. Hysteresis window is set by the positive feedback gain mirror load, and determined by the ratio α, where $\alpha = (\frac{W}{L})_5/(\frac{W}{L})_3$. The gain of the positive feedback gain stage is given by

$$A_v = \sqrt{\frac{\mu_p(\frac{W}{L})_1}{\mu_n(\frac{W}{L})_3}} \cdot \frac{1}{1-\alpha} \tag{5.17}$$

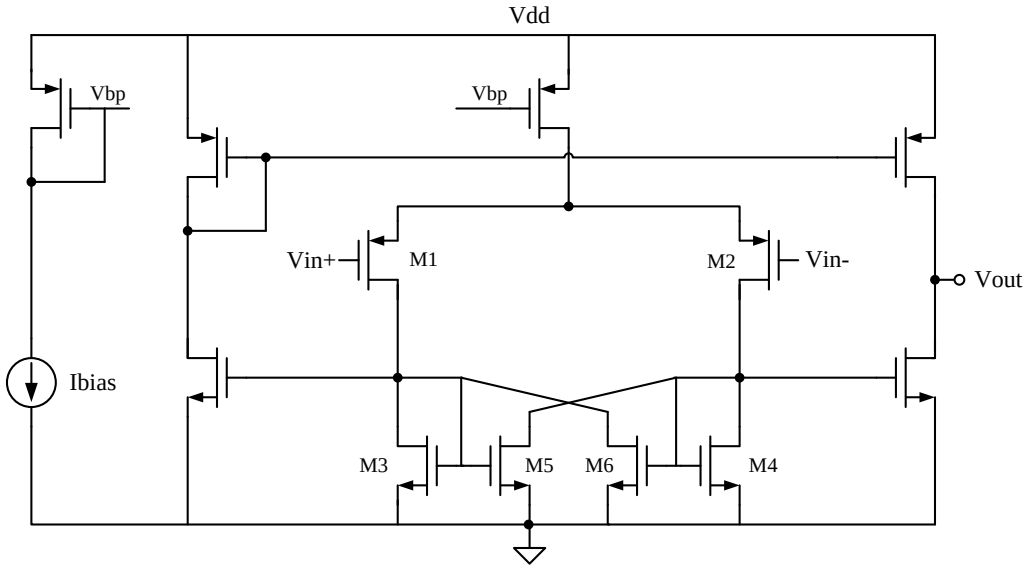


Figure 65. Hysteresis comparator

Figure 66 shows the simulated hysteresis window, which is 42mV in this project.

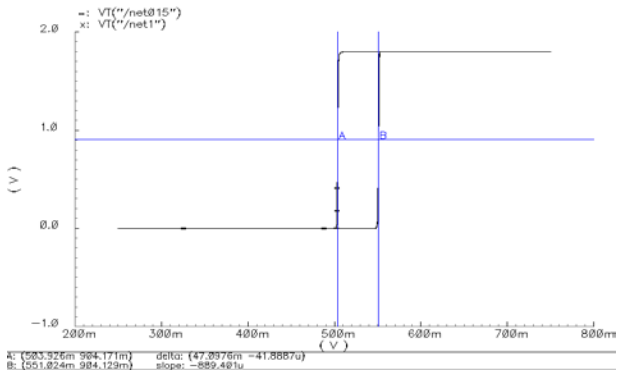


Figure 66. Simulated comparator hysteresis window

5.2.5. Non-Overlapping Clock Generator

The PMOS power switch and NMOS power switch cannot be closed at the same time, or the voltage source will be shorted to ground, and generating current large enough to burn the transistors. To avoid the above situation, “non-overlapping” clocks are needed for driving the two power switches. Since the two power switches belong to different types (P-type and N-type), the clocks are not traditional non-overlapping signals with opposite phase, but are in-phase signals with different rising and falling edges. The required clock waveforms are shown in Figure 67. Clock for PMOS switch turns high before clock for NMOS switch turns high, and turns low after clock for NMOS switch turns low. This means PMOS switch turns off before NMOS switch turns on, and PMOS switch turns on after NMOS switch turns off.

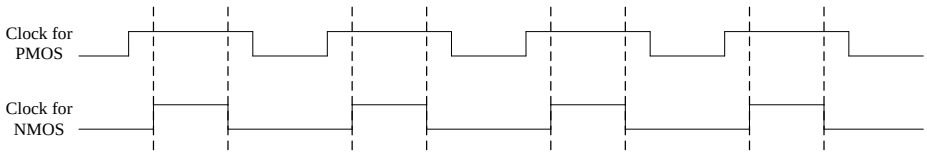


Figure 67. Clocks for power switches

Figure 68 shows the circuit which is used to generate the above waveforms. This circuit takes one clock signal *Clkin*, and generates a 2-phase non-overlapping clocks *Clk'* and *Clk_n*. The operation is based on the fact that the rising edge of the input clock passes immediately through the NOR gate, while the falling edge has to pass through the other NOR gate and the cascaded delay elements. The non-overlapping time equal to the sum of the delays at the NOR gate and the delay elements. Here the non-overlapping time is designed to be at several nanoseconds, and is dominant by the delay elements. The delay element is implemented by inverter-C delay cells. Adding an inverter after *Clk'*, the waveform in Figure 67 will be obtained.

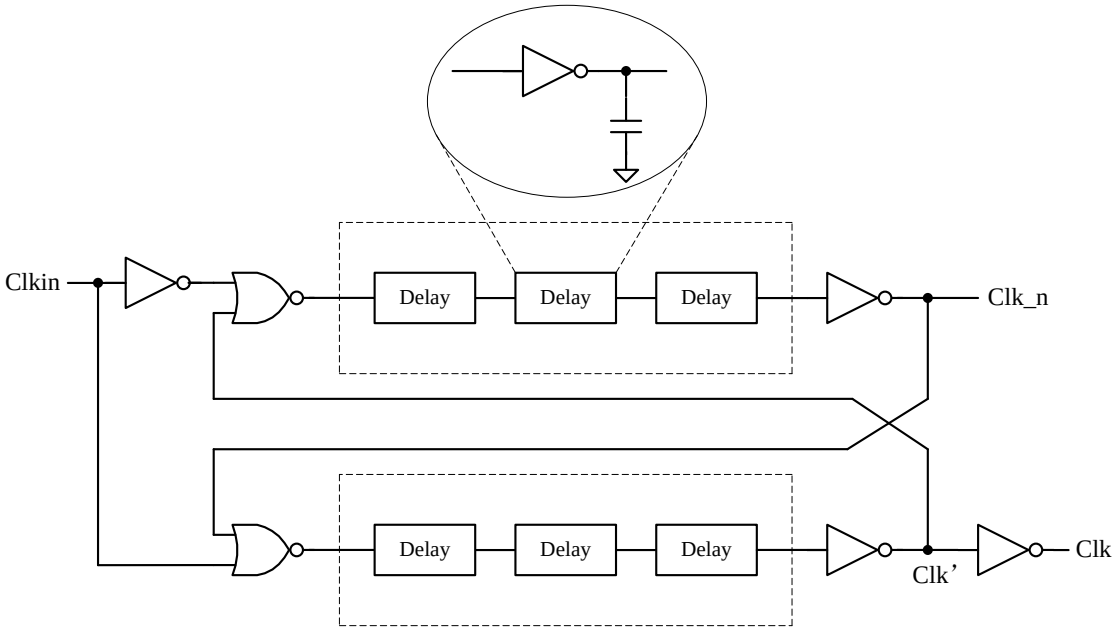


Figure 68. Non-overlapping clock generator

5.2.6 Level Shifter

Level shifter is used here to transform a signal with amplitude of one voltage level to another voltage level. The relationship between input and output voltage is shown in Figure 69.

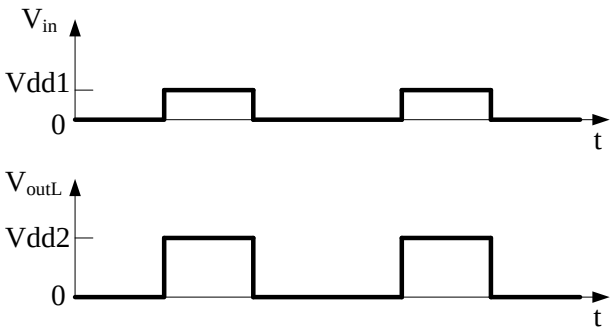


Figure 69. Waveforms of input voltage and output voltage

The one using cross-coupled PMOS load is shown in Figure 70 [100]. The operation of the circuit is as follows. When the input signal *Vin* is at the *Vdd1* level, *Vinb* is at the GND level, MN1 turns on and MN2 turns off, thus pulls the *Voutb* signal to GND. This transition of the *Voutb* signal turns on MP2, which pulls up the $Vout_L$ signal to the *Vdd2* level. When *Vin* is at GND, *Vinb* is at the *Vdd1* level, MN1 is off and MN2 is on, which turns on MP1. MP1 pulls up *Voutb* to *Vdd2* level.

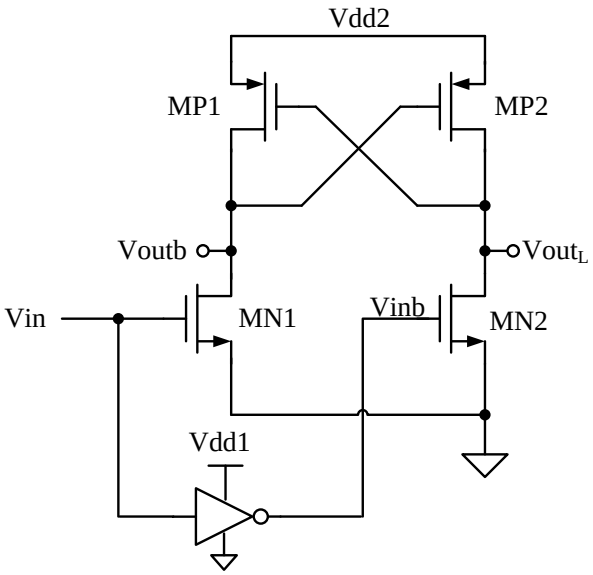


Figure 70. Level shifter

5.3 Current Sensing Loop

The main task for current sensing loop is to select the proper supply level for certain load condition. In other words, it selects lower supply for light load, and higher supply for medium and heavy load.

Through rough simulation with power chain and voltage control loop, the efficiency curves under 1.65V supply and 3.3V supply intersect when load current is around 20mA. To obtain high efficiency over the entire load range, set 1mA to 20mA to be light load region, working under 1.65V supply, and 20mA to 400mA to be medium and heavy load region, working under 3.3V supply.

The current sensing technique has been shown in Section 4 Figure 50, which senses the output current and converts the current into voltage through a resistor. After sensing output current, as illustrated in Figure 71, the current sensing loop compares the sensed

voltage with a fixed reference voltage by a hysteresis comparator. The reference voltage is set to equal to 20mA load current. If the output current is higher than the current threshold, the switch which is connected to higher supply S1 is controlled to be on, while if the output current is lower than the reference, the switch S2 which is connected to lower supply is controlled to be on. Higher supply is generated directly from off chip, and the lower supply is generated from SC circuit. Here the two switches are implemented by PMOS transistors. The gate control voltages of the two switches should be non-overlapping signals to avoid shorting of supplies, that's why non-overlapping clock generator is added after comparator. The level shifters adjust the control signals to required voltage levels, and then driving circuits are inserted to drive the switches. Another switch S3 is added on top of S2 to pull the SC circuit output to high, such that SC circuit will be shut down when not being used. The AND gate between comparator and non-overlapping clock generator is used to force the supply to be high when the buck converter powers on, therefore a faster start-up can be accomplished. A 20pF MIM cap is added at the output to reduce supply fluctuation.

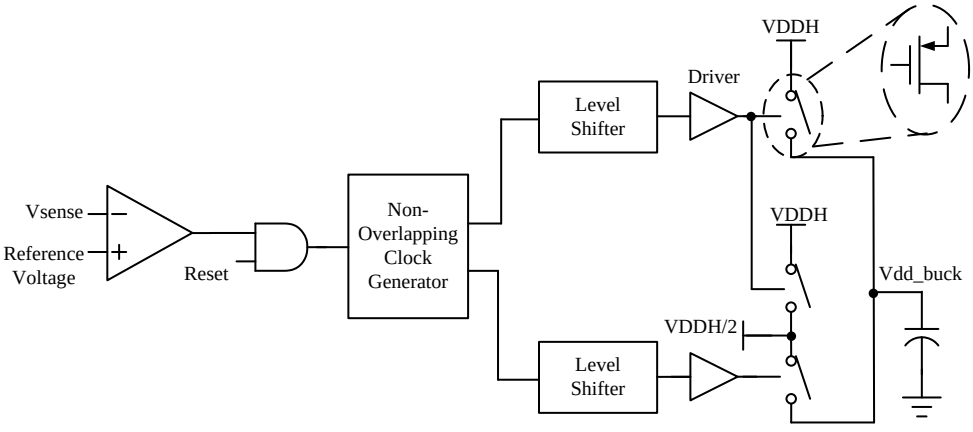


Figure 71. Current sensing loop

For the current sensing circuit design, the ratio of power transistor to the sense transistor is set to be 400:1, thus the sensing current is in the range of 2.5μA~1mA. The resistor value needs to be large enough for comparator input, and not too large to higher than the circuit supply voltage, and is finally chosen to be 3Kohm. It is implemented by poly resistor for its higher sheet resistance, good linearity and tighter tolerances. The capacitor, which is used to minimize the current ripple, is preferred to have larger value. If not, with large ripple, the comparator output may have undesirable changes, which causing the converter supply jumping between higher supply and lower supply. In this design, the capacitance is 40pF, and implemented by metal-insulator-metal (MIM) cap.

5.4 Switched-Capacitor Converter

The schematic for switching capacitor converter is shown in Figure 72. It is a double phase architecture switching capacitor converter as introduced in Section 4. The switches' sizes and drivers' sizes can be determined by the same method used for buck converter power stage design. C1 and C2 are off-chip 1μF capacitors, and better for high efficiency compared to on-chip capacitors.

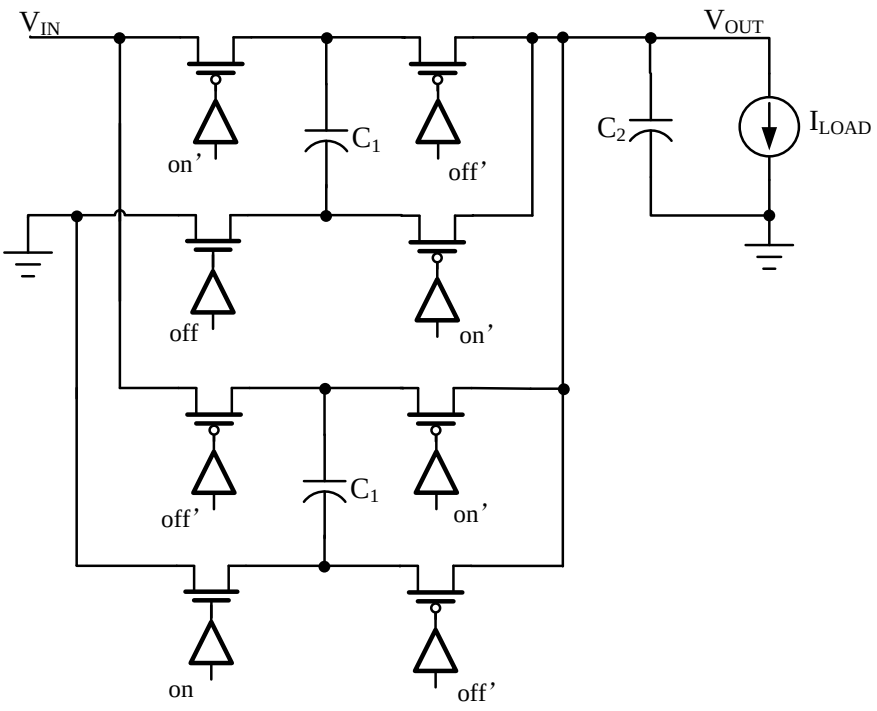


Figure 72. Switching capacitor converter schematic

Figure 73 shows the circuit which generates clock signals for the switching capacitor converter. The original clock is obtained from the triangle wave generator, which is the CLK signal in Figure 62. This clock frequency is divided by 8 through 3 series-connected D flip-flops. By reducing the clock frequency, thus reducing the switching losses, higher SC converter efficiency can be achieved. After non-overlapping clock generator and inverters, all required clocks are generated. On' and off' signals are interleaved signals for the two paralleled cells. On and off signals are needed since NMOS is used as switch instead of PMOS. "EN" is a control signal, which will disable SC converter when SC converter is not needed, therefore saving total power consumption in further.

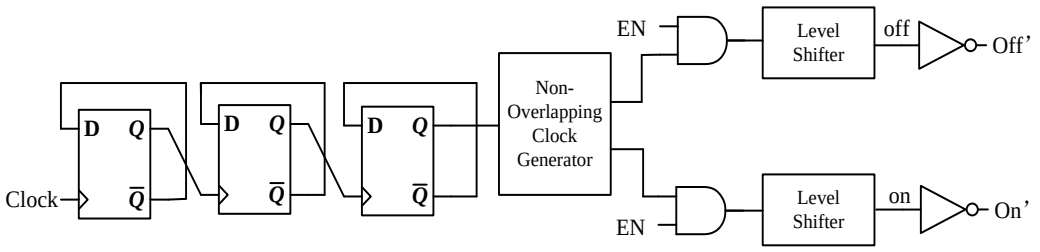
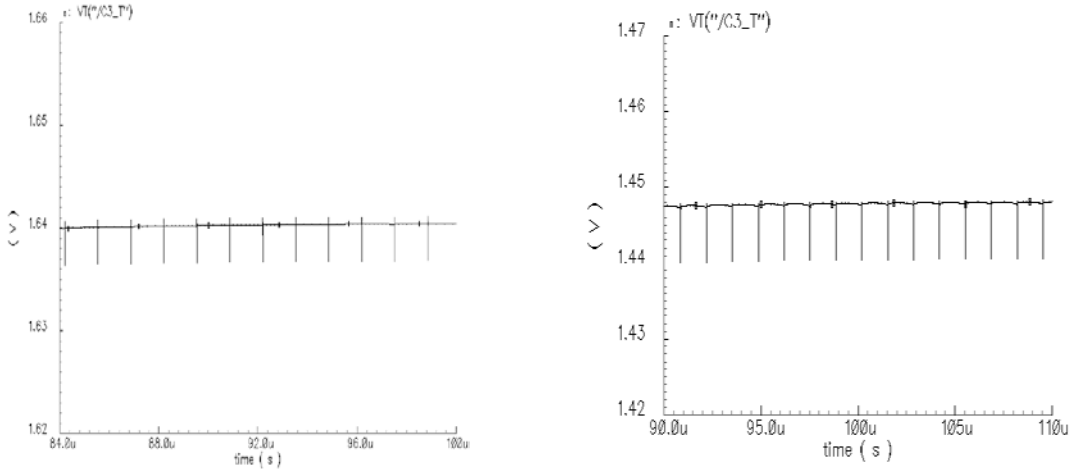


Figure 73. Clock signals generator for switching capacitor converter

Figure 74 shows the simulated output voltage waveform with resistive load. The output voltages are very clean. Since there is no regulation for the output, output voltage drops when load current increases. This is mainly caused by the increasing voltage drop across switches. When load current is 1mA, the output voltage is 1.64V. When load current is 20mA, the output voltage is 1.448V.



(a) (b)

Figure 74. SC converter output voltage waveforms (a). load current is 1mA (b). load current is 20mA

6. SIMULATION RESULTS AND COMPARISON

The main measurements of buck converter conclude steady-state measurements and transient response measurements. In steady-state measurements, the circuit basic operation will be verified with fixed resistive load, such as output average voltage, output voltage ripple, inductor current ripple, switching frequency, and most importantly in this project, the efficiency. In transient response measurements, the voltage control loop stability is verified. This testing is usually done by applying a step load current and measuring the output voltage recovery time and overshoot/undershoot voltages. Figure 75 shows the load transient simulation setup in Cadence. If the load current step is replace with a resistor, it is the setup for stead-state simulation, as shown in Figure 76.

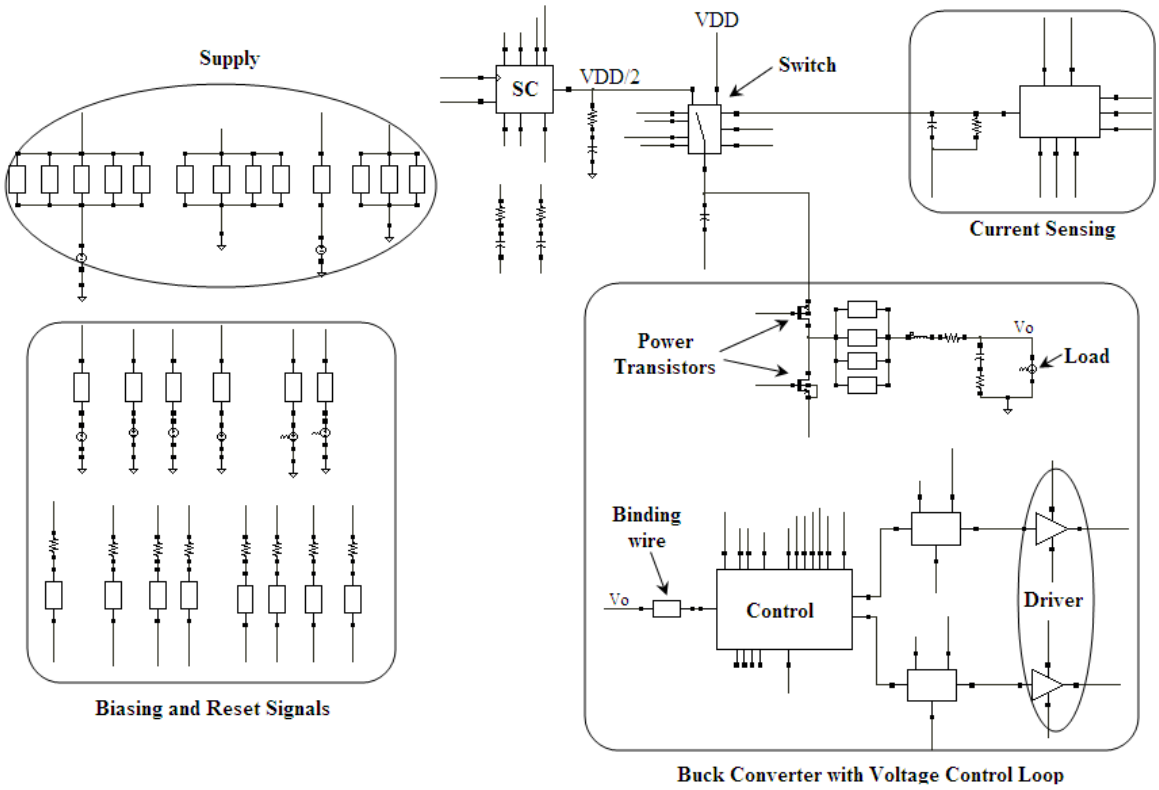


Figure 75. Load transient simulation setup in cadence

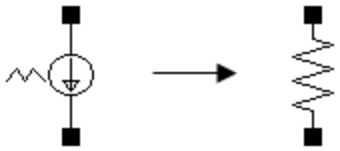


Figure 76. Setup change from load transient simulation to steady-state simulation

6.1 Simulation Results of Steady-State Condition

Under steady-state condition, the load is fixed. Simulations are done at different load points. The triangle wave generator output is shown in Figure 77. This signal is important because it determines the switching frequency, and it will not be affected by load.

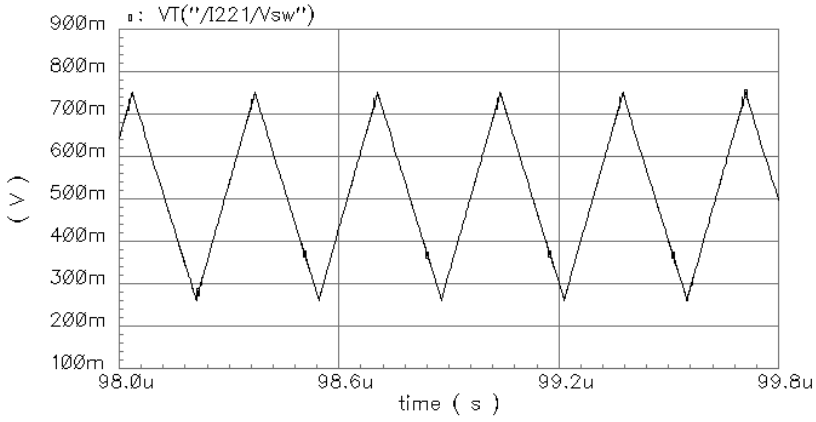


Figure 77. Triangle wave generator output

Figure 78 shows an example of PWM control signals for both NMOS power transistor and PMOS power transistor. Dead time exists.

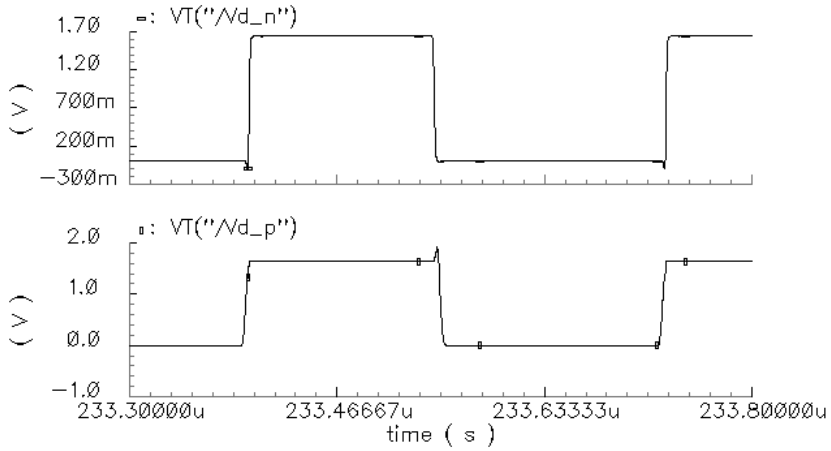


Figure 78. PWM signals (top: for NMOS; bottom: for PMOS)

The following sub-sections show some simulation results when load currents are 1mA, 18mA, 22.5mA, and 400mA respectively. Results under 18mA and 22.5mA are showed because they are close to the threshold (20mA). The supply voltage, output voltage, and inductor current waveforms are plotted and brief explanations are presented.

6.1.1 I_{out}=1mA

Figure 79 shows the buck converter supply voltage. The average voltage is not exactly 1.65V, but around 1.64V due to the load at switched capacitor converter. The glitch is caused by the switching of power transistors. When PMOS power transistor is off, SC converter output is 1.64V, while when PMOS power transistor is on, drawing large amount of current out of SC converter, the voltage experiences glitch.

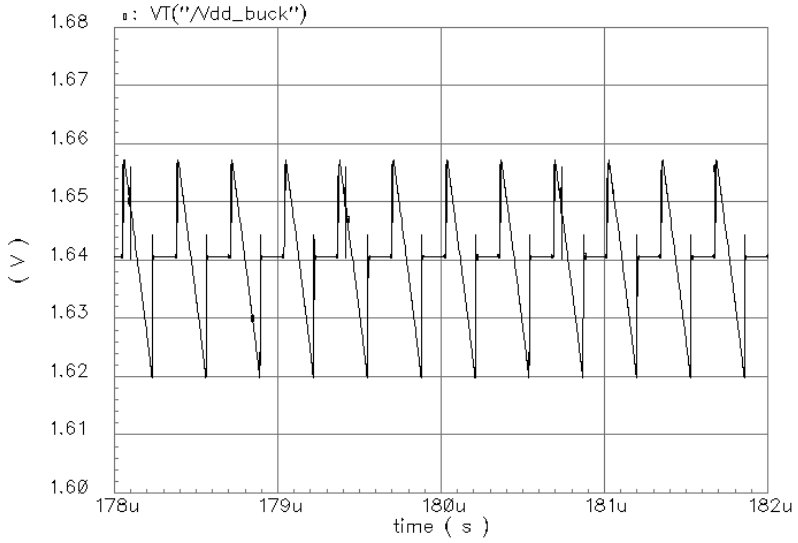


Figure 79. Buck converter supply voltage waveform when load current is 1mA

Figure 80 gives the output voltage waveform and inductor current waveform. The average output voltage is 0.90016V, very close to 0.9V. Peak to peak output voltage ripple is 0.9mV, and peak to peak inductor current ripple is 37mA.

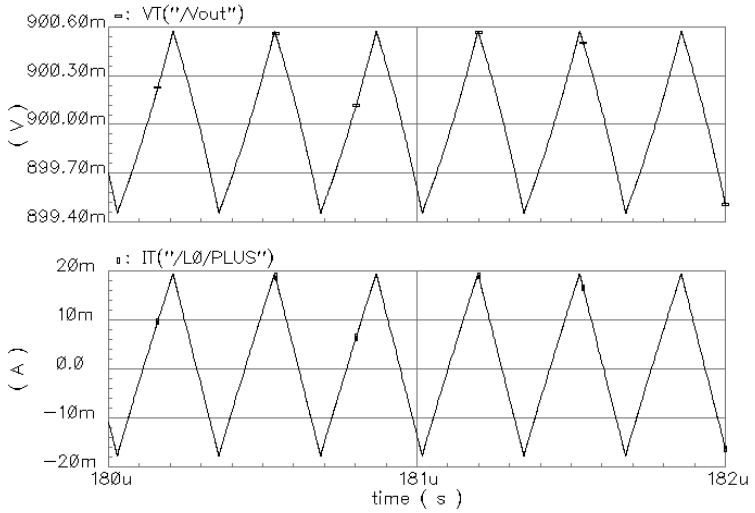


Figure 80. Output voltage (top waveform) and inductor current (bottom waveform) when load current is 1mA

6.1.2 I_{out}=18mA

In Figure 81, the output current is slightly lower than the threshold current (20mA), and the supply voltage is still 1.65V. The voltage drop is greater than the one showed in Figure 79 due to larger load current. In Figure 82, the average output voltage is 0.90005V, peak to peak output voltage ripple is 1mV, and peak to peak inductor current ripple is 33.5mA.

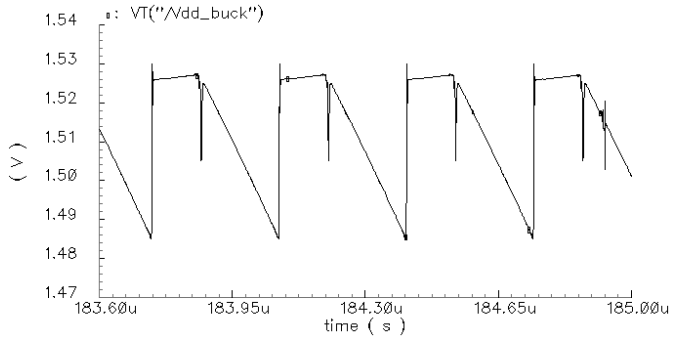


Figure 81. Buck converter supply voltage waveform when load current is 18mA

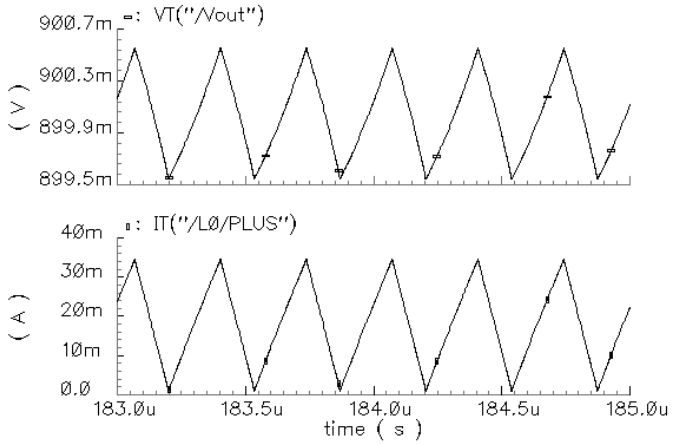


Figure 82. Output voltage (top waveform) and inductor current (bottom waveform) when load current is 18mA

6.1.3 I_{out}=22.5mA

In Figure 83, the supply voltage is 3.3V, since the output current is larger than the threshold current (20mA). Same as powered by SC converter, the voltage drops when the PMOS switch is on. In Figure 84, the average output voltage is 0.90018V, peak to peak output voltage ripple is 1.8mV, and peak to peak inductor current ripple is 60mA. The ripples are double than the ones when supply is 1.65V.

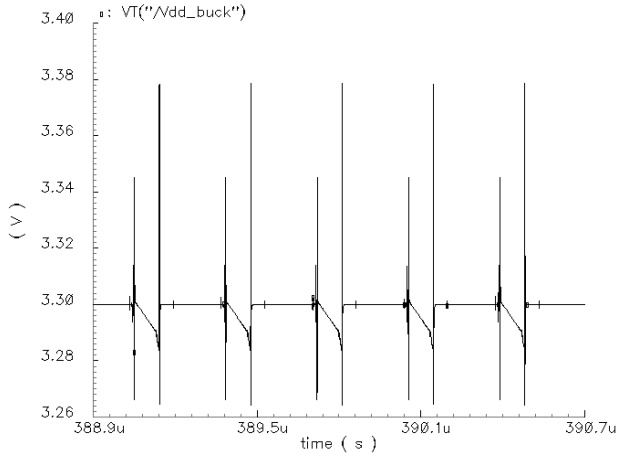


Figure 83. Buck converter supply voltage waveform when load current is 22.5mA

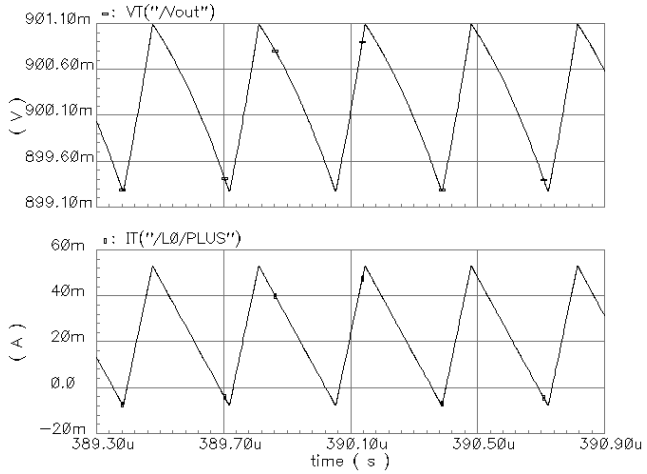


Figure 84. Output voltage (top waveform) and inductor current (bottom waveform) when load current is 22.5mA

6.1.4 I_{out}=400mA

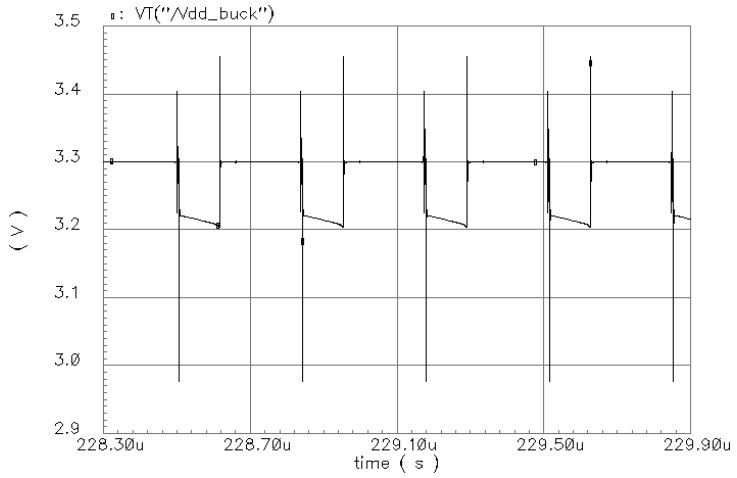


Figure 85. Buck converter supply voltage waveform when load current is 400mA

In Figure 86, the average output voltage is 0.90004V, very close to 0.9V. Peak to peak output voltage ripple is 1.9mV, and peak to peak inductor current ripple is 66mA. The ripples are slightly larger than the ones when load current is 22.5 mA, this is because in heavier load, the duty cycle becomes larger to compensate for larger conduction losses.

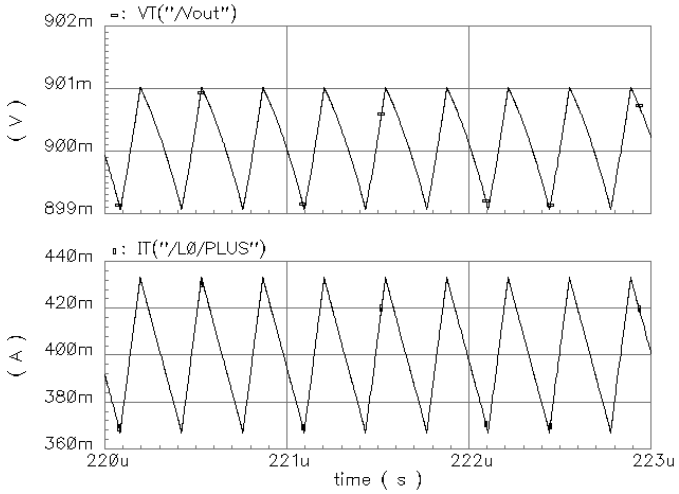


Figure 86. Output voltage (top waveform) and inductor current (bottom waveform) when load current is 400mA

6.1.3 Efficiency

The efficiency curves are shown in Figure 87. The solid line represents the efficiency of proposed buck converter, while the dash line represents the efficiency of the conventional buck converter. A maximum efficiency of 91% is attained. The total power dissipation of the proposed buck converter is reduced by 20% at minimum load current.

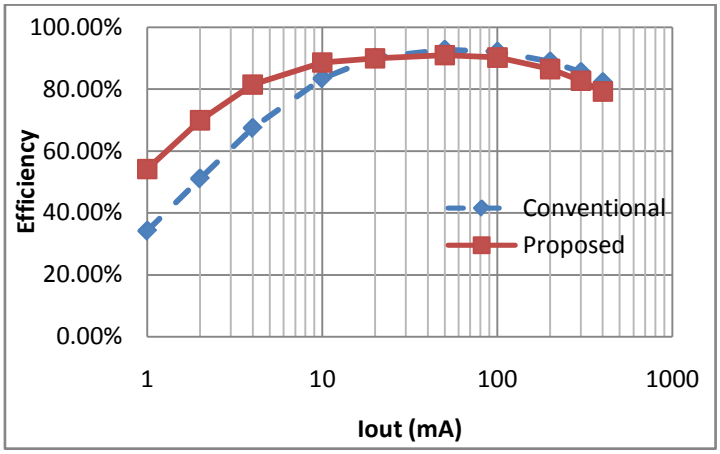


Figure 87. Efficiency vs output current

Table 10 and Table 11 give the hand calculation results of the power consumption when load current is 1mA and 400mA respectively. Switching loss, conduction loss, and quiescent loss are estimated according to the parameters extracted from simulation. The calculated efficiencies match the simulated ones, just that they are slightly larger than the simulation due to some small ignored power losses.

Figure 88 and Figure 89 show more clearly the distribution among each portion. When load current is 1mA, switching loss is much larger than conduction loss, as we expected. The quiescent loss, which is ignored during most of the analysis, turns out to be the largest power loss. It can be reduced by several techniques, for example, shutting

shown some blocks. When load current is 400mA, the distribution chart shows a dominant power loss of conduction loss. Switching loss can be ignored here.

Table 10. Power consumption summary (load current is 1mA)

Output Power	0.9mW
Quiescent Loss	0.245mW
Switching Loss	0.22mW
Conduction Loss (Rds=1.1ohm, DRC=0.1ohm)	1.2uW

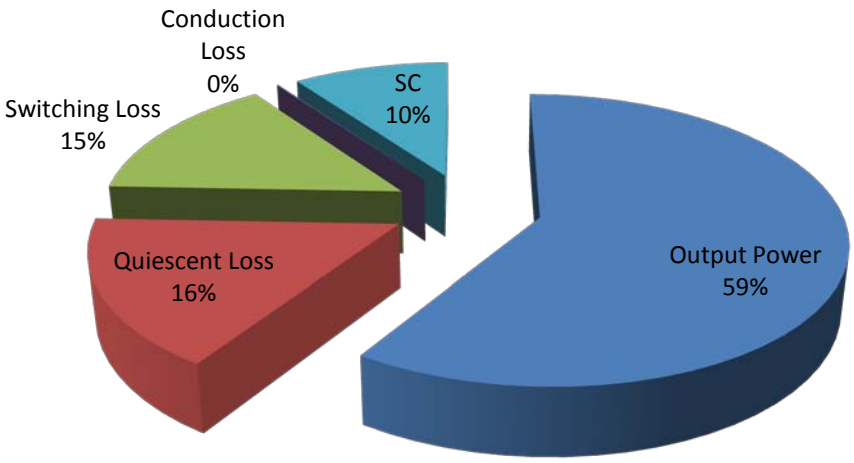


Figure 88. Power consumption distribution chart (load current is 1mA)

Table 11. Power consumption summary (load current is 400mA)

Output Power	0.36W
Quiescent Loss	0.23mW
Switching Loss	0.88mW
Power Transistor Conduction Loss (Rds=0.4ohm)	0.064W
Inductor DCR Loss (DCR=0.1ohm)	0.016W

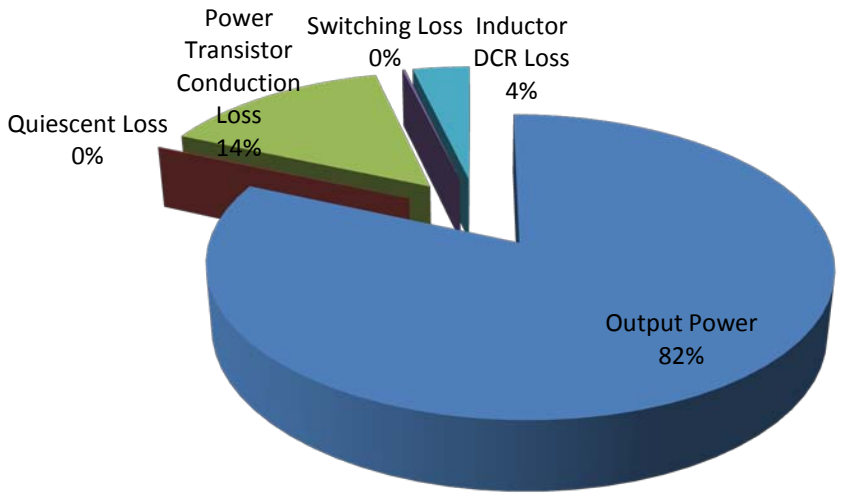


Figure 89. Power consumption distribution chart (load current is 400mA)

6.2 Simulation Results of Transient Condition

Transient simulation is done by replace load with a current source. Giving a current step with 50ns rising/falling time, the transient response is shown in Figure 90. When the load current switches between 1mA and 400mA, the buck converter supply voltage follows the changes quickly.

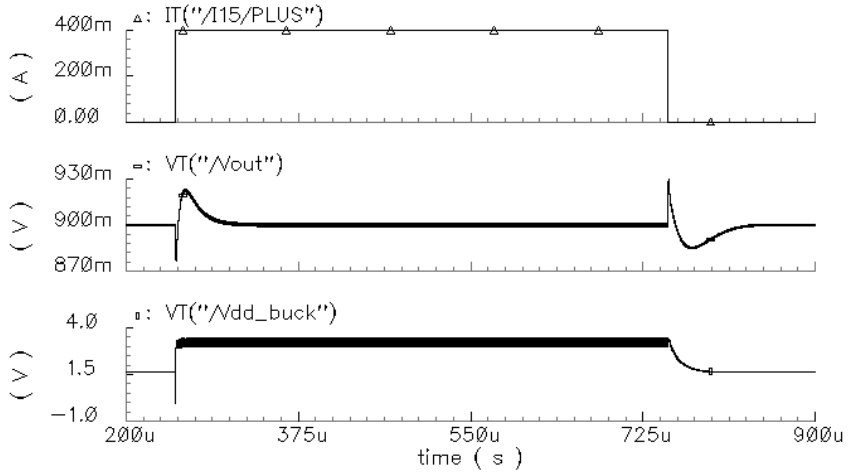


Figure 90. Transient response of the proposed buck converter

The detailed performance is listed in Table 12. Compared with Table 7 and Table 8, the recovery time becomes longer due to the switching action between two voltage supply levels.

Table 12. Transient performance summary of the proposed buck converter

Undershoot voltage	46.1mV	Recovery time (1%) (1mA→400mA)	27µs
Overshoot voltage	44.4mV	Recovery time (1%) (400mA→1mA)	45µs

6.3 Performance Summary

Table 13 summarizes the key performance for the proposed buck converter.

Table 13. Performance summary

Parameters	**Spec**
Technology	0.18μm
V_{DD} (V)	3.3
V_{out} (V)	0.9
I_{MIN} (mA)	1
I_{MAX} (mA)	400
F_s (MHz)	3
L (μH)	3.6
C (μF)	12
η	54%~91%
η Improvement (max)	20%

6.4 Results Comparison and Discussion

Table 14 and Table 15 compare this work with some similar academic work and industry products which are all aim to achieve high light-load efficiency. This work has similar performance with them.

In the two ISSCC papers, the first one employ gate charge modulation and recycling technique, which only reduce the gate drive loss, and have no effect to the switching loss due to charging and discharging the switching node. Only 5% improvement is achieved. The second one employs auto-selectable-frequency technique, which scales down switching frequency at light load. By pre-defining the switching frequency to be binary-weighted multiples of a fundamental frequency, the output spectrum doesn't change much with load. 27% efficiency improvement can be achieved. However, as shown in Figure 91, its efficiency curve is not smooth, but drops a lot between using two adjacent

switching frequencies since the frequency is not continuously changing. Also, although the maximum efficiency improvement in this work is slightly smaller than the one in [51], if compare the efficiency at 10mA, which is the minimum load current of [77], [77] achieves an efficiency of 66%, [51] achieves an efficiency of 70%, while in this work, the efficiency is as high as 88.7%.

Table 14. Comparison with previous work

Parameters	**ISSCC07 [77]**	**ISSCC08 [51]**	**This work**
Technology	0.5µm	0.35µm	0.18µm
V_{DD} (V)	3.6	1.8~3	3.3
V_{out} (V)	1~1.8	0.9	0.9
I_{MIN} (mA)	10	5	1
I_{MAX} (mA)	400	500	400
F_s (MHz)	3	2	3
L (µH)	3.3	2.2	3.6
C (µF)	4.7	2.2	12
η	66%~89%	55%~89%	54%~91%
η Improvement (max)	5%	27%	20%
Method Used	Gate Charge Modulation & Recycling	Auto-Selectable-Frequency PWM	Dual-supply

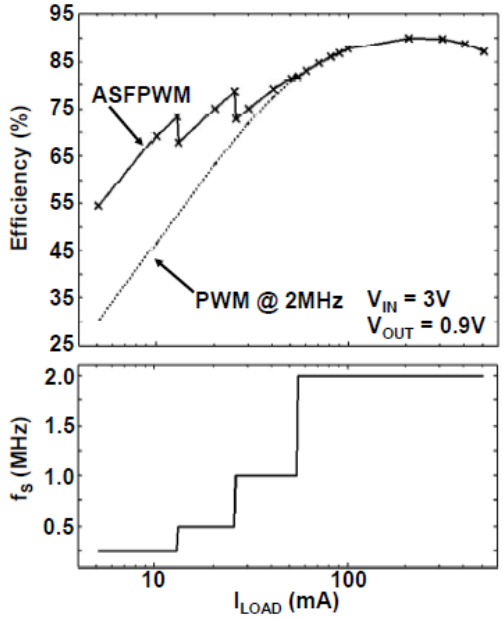


Figure 91. Efficiency curve of [51]

Industry products have higher efficiency because several efficiency-enhancing techniques are combined together in these circuits. While in this project, in order to observe the efficiency improvement brought out by the proposed method, on other efficiency-enhancing techniques are used. Most of the industry products minimize the losses mainly by reducing effective switching frequency at light load. This work, however, works at constant switching frequency, therefore having a lower output noise and EMI. Besides, this converter is operating under PWM mode over the entire load range, other than changing to other control methods at light load, which reduces control circuit complexity. Another benefit is that the lower supply at light load results in both smaller inductor current ripple and smaller output voltage ripple.

Table 15. Comparison with similar industry products

Product	V_{IN}	V_{OUT}	I_{OUT}	f_S	Efficiency (η)
TI (TPS62320) [53]	3.6 V	1.2 V	1~400 mA	3MHz	60%~86%
Analog Devices (ADP2108) [54]	3.6 V	1.0 V	1~600 mA	3MHz	65%~84%
Micrel Inc. (MIC23031) [46]	4.2 V	1.2 V	1~400 mA	4MHz	68%~82%
Linear Technology (LTC3542) [55]	4.2 V	1.2 V	1~500 mA	2.25MHz	75%~88%
Maxim (MAX8560) [56]	3.6 V	0.9 V	1~500 mA	4MHz	70%~85%
This Work	3.3 V	0.9 V	1~400 mA	3MHz	54%~ 91 %

7. TESTING RESULTS

The basic equipment used during Buck converter testing includes voltage source, inductor, capacitor, load resistor, sensing resistors, multimeter, and oscilloscope.

7.1 Testing Setup

Figure 92 shows the chip micrograph. Figure 93 shows the Buck converter testing setup. When switch S_A is on and S_B is off, steady-state testing is performed; When S_A is off and S_B is on, load transient testing is performed. Small resistors are added in series with supply and load respectively to measure the input and output current.

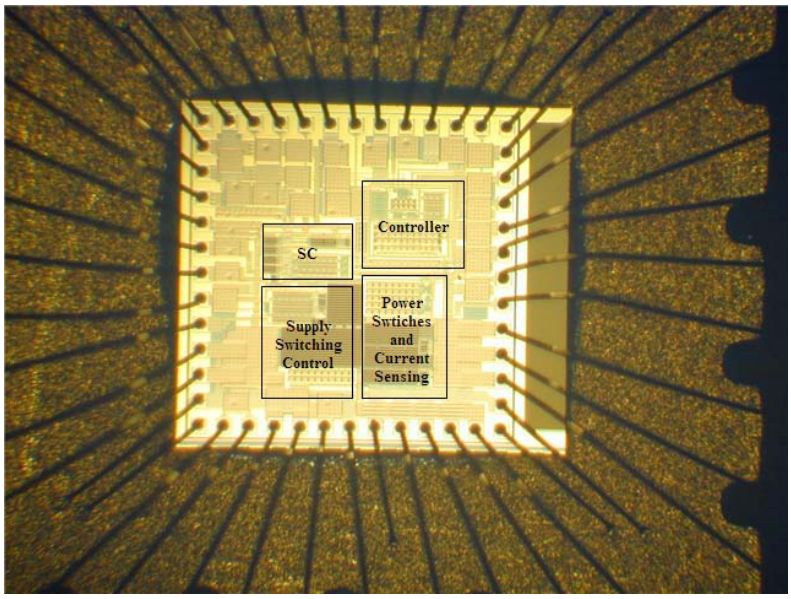


Figure 92. Chip micrograph of buck converter

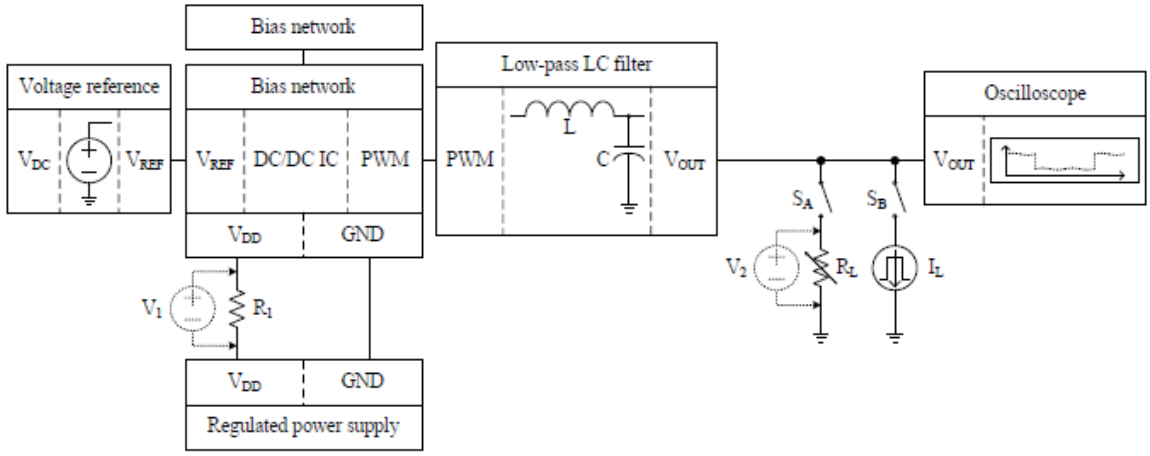


Figure 93. Testing setup of the buck converter [35]

Figure 94 explains the testing method for the transient response. A power transistor is employed as a switch. When the power transistor is turning on, a sudden current is drawn from R_{load2} with a current step of V_{out}/ R_{load2}. The output voltage is regulated at 0.9V, and a load current step that changes from 1mA to 400mA then back to 1mA is required. The resistance of R_{load1} and R_{load2} is 900ohm and 2.25ohm respectively.

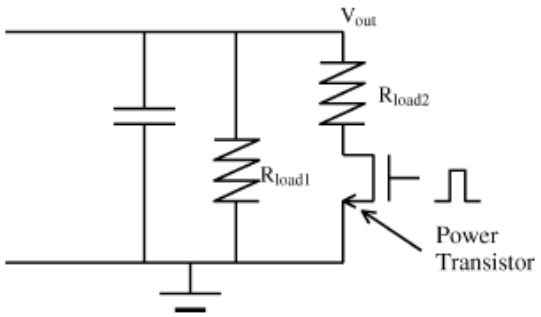


Figure 94. Load response testing setup

Figure 95 shows the lab measurement picture. This is the testing of converter with triangle wave generator removed out from chip, thus the triangle wave is provided by a clock source. Due to the equipment limitation, only 1MHz triangle wave can be obtained, which means the converter is working with 1MHz switching frequency. The triangle wave has 500mV peak to peak amplitude and an average value of 500mV.

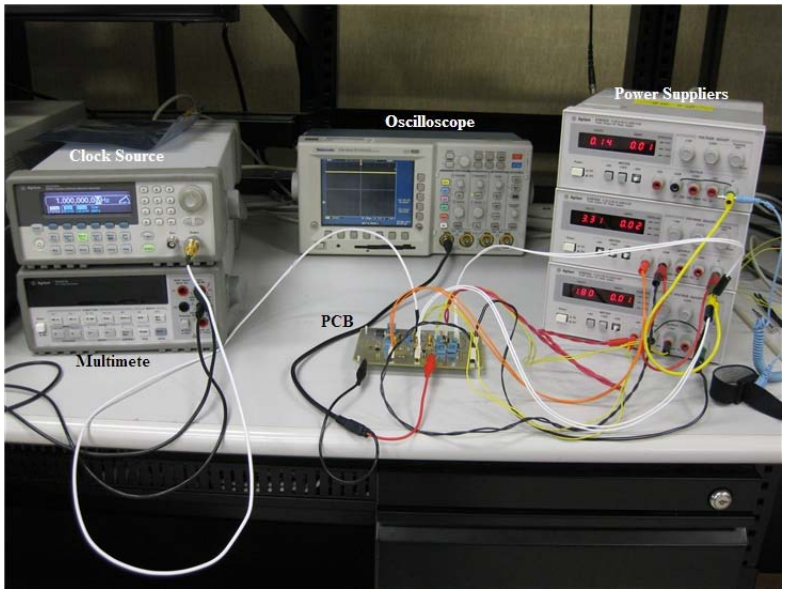


Figure 95. Lab measurement picture

7.2 Preliminary Testing Results

This section shows the testing results obtained so far. More results will be measured later. The tested output voltage follows the reference voltage well. When output voltage is 0.9V, the difference between output voltage and reference voltage is around 4mV. Average input/output voltage and input/output current are measured to get the efficiency. Figure 96 shows the efficiency comparison result with 1MHz switching frequency. The

overall efficiency is lower than simulated one, but the efficiency improvement is still large. The peak efficiency is 83.5% at 100mA, and maximum efficiency improvement is 26.1%.

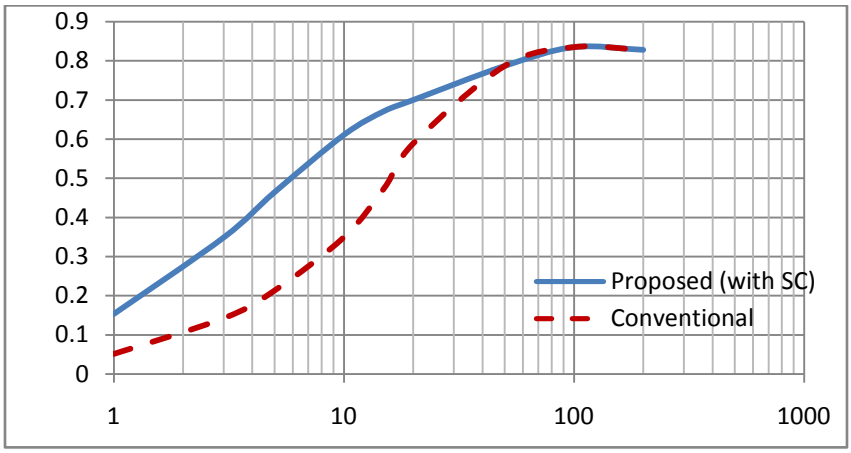


Figure 96. Tested efficiency of both conventional and proposed converter

7.3 Problems Analysis

Existing problems include:

(1). Transient simulation is unable to obtain since the supply couldn't change automatically when load changes. Even when the reference voltage for determining supply reduces to zero, the supply is still stay at *VDD/2* under 40mA load current.

(2). Chips are sensitive and easy to be broken. Fifteen dies are sent out for packaging, but the working situations between different chips are not the same. For some chips, the circuit even didn't work at all.

(3). Tested efficiency is lower than simulation, especially at light load.

The first two observed abnormal operations all have something to do with signals connected to transistor gate, for example, the reference voltage for determining supply level connects to the input transistor gate of a comparator. The possible reason is the gate is broken during fabrication or packaging or testing. Because the taped-out chip has no ESD protection, thus it is sensitive. What is worse, the antenna rule is violated during layout.

The tested efficiency is lower than the simulated one. The reasons can be due to the loss on (a). power metal and output metal in layout, (b). bondwire. The efficiency measure is tricky when the power consumption is very low, since the input current, output current and output voltage are all not purely DC, small measurement error can result in large calculated efficiency difference. Thus, more accurate way to measure the input/output current need to be further explored.

8. CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

In this project, a buck converter is implemented and fabricated in TSMC 0.18um process with 1.6*1.6mm^2 die area. With dual-supply operation, it achieves an efficiency of 54%~91% over a wide load range from 1mA to 400mA. At light load condition, the buck converter can automatically reduce the effective supply to optimize efficiency. The idea is simple and useful for high frequency converters to improve their light-load efficiency.

8.2 Future Work

There are several improvements can be made in the project.

Firstly, ESD protection is better to be added inside chip. Even it is not added, at least each time when there is a transistor gate connecting to pad cell, a resistor should be placed between pad and gate.

Secondly, before the buck converter output signal is fed back to error amplifier, a resistor divider is better to be added. One of the reasons is to protect the input transistor of error amplifier, since during testing the output voltage may go as high as 3.3V in some improper situation, which can burn the input transistor which is working under 1.8V domain. Changing the input transistor to a 3.3V domain transistor is another solution.

Thirdly, in this project, the lower supply level *VL* is directly set to be *VDD/2*. This value is chosen by considering the implementation simplicity and efficiency of the supply circuit. However, this value can be further optimized to improve the overall efficiency. A topology with intelligent supply level decision will be explored in the future.

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