THIN FILM SOLAR CELLS WITH LIGHT TRAPPING TRANSPARENT CONDUCTING OXIDE LAYER

A Thesis

by

TIANLIN LU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Haiyan Wang
Committee Members,	Chin B. Su
	Xing Cheng
	Xinghang Zhang
Head of Department,	Costas N. Georghiades

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ABSTRACT

Thin Film Solar Cells with Light Trapping Transparent Conducting Oxide Layer.

(May 2011)

Tianlin Lu, B.S., Huazhong University of Science and Technology

Chair of Advisory Committee: Dr. Haiyan Wang

Thin film solar cells, if film thickness is thinner than the optical absorption length, typically give lower cell performance. For the thinner structure, electric current loss due to light penetration can offset the electric current gain obtained from higher built-in electric field. Light trapping schemes can increase the effective optical absorption length and thus enhance the electric current for thinner solar cells. Here a new light trapping scheme based on light trapping transparent conducting oxide layer (LT-TCO) is proposed to enhance the performance of thin film solar cells. Three different configurations of integrating the LT-TCO layer in solar cells are proposed and evaluated. This research aims to develop the LT-TCO layer with surface texture and good conductivity by pulsed laser deposition (PLD) technique at low temperature. The LT-TCO layer is fabricated by PLD deposition of Al-doped ZnO to achieve multilayer films by tuning oxygen pressure. The light trapping effect is examined by optical transmittance measurement and the surface texture is characterized by transmission electron microscopy (TEM) technique. The conductivity of LT-TCO layer is measured by resistivity measurement. Thin film CdTe/CdS solar cells are fabricated by PLD

technique to develop baseline solar cells for integration of LT-TCO layer. The as-deposited thin film solar cells show relatively low performance and are further processed with various post-deposition treatments to seek efficiency enhancement. The effects of different processes on cell performance are examined by electrical, optical, and microstructure studies. Air annealing of CdS layer and $CdCl_2$ treatment of CdTe layer combined are found to yield the best cell performance. The fabrication issues that limit the cell performance are discussed and future optimizations in fabrication processes are suggested.

DEDICATION

This thesis is dedicated to my dear father, mother, and sister who have always encouraged me to acquire self improvement through higher education and supported my decision to pursue solar energy research during my master's program at Texas A&M University.

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Haiyan Wang, and my committee members, Dr. Chin B. Su, Dr. Xing Cheng, and Dr. Xinghang Zhang, for their guidance throughout the course of this research. I deeply appreciate Dr Wang's support in helping me establish the experimental setup for thin film solar cell research. Her encouragements have always motivated me to face the difficulties, work hard and stay optimistic on this meaningful research.

I would like to give my special thanks to my research colleagues, Joon Hwan Lee and Aipeng Chen, for their support in TEM and SEM characterization important to failure analysis of thin film solar cells. I also want to extend my gratitude to other research colleagues who have maintained our fabrication facilities well.

Thanks also go to my friends and colleagues and the department faculty and staff for making my time at Texas A&M University a rewarding experience. I also appreciate Dr. Fred Strieter and Dr. Rusty Harris for their supervison over my graduate teaching assistantship.

NOMENCLATURE

V_{oc}	Open-Circuit Voltage
I_{sc}	Short-Circuit Current
J_{sc}	Short-Circuit Current Density
FF	Fill Factor
η	Efficiency
J-V	Current Density-Voltage
LT	Light Trapping
TCO	Transparent Conducting Oxide
AZO	Al-doped Zinc Oxide
CdTe	Cadmium Telluride
CdS	Cadmium Sulfide
PLD	Pulsed Laser Deposition
PVD	Physical Vapor Deposition
XRD	X-ray Diffraction
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy

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1. INTRODUCTION

1.1 History and Overview of Solar Cells

The photovoltaic effect was first discovered by A. E. Becquerel in 1839 at the time increased current was observed when the electrolytic cell was exposed to light [1]. In 1877, the discovery of photoconductivity in selenium led to fabrication of the first selenium solar cell by W. G. Adams [2]. In 1954, Chapin demonstrated a single crystal silicon solar cell with 6% efficiency [3]. In the same year, the first all thin film Cu_2S/CdS heterojunction solar cell with 6% efficiency was reported by Reynolds [4]. In 1956 Jenny reported a GaAs solar cell with 4% conversion efficiency [5]. In 1963, D. A. Cusano fabricated the first thin film CdTe solar cell based on CdTe/ Cu_2Te heterojunction with 6% efficiency [6]. Bonnet and Rabenhorst reported a thin film CdTe/CdS solar cell in 1972 with 6% efficiency [7]. In 1974, S. Wagner *et al.* reported a thin film $CuInSe_2$/CdS heterojunction solar cell with 12% conversion efficiency [8]. In the last three decades, the efficiencies of solar cells based on different materials have gained significant improvements as shown in Fig. 1 [9]. Solar cells, depending on materials and applications, are typically divided in four major categories which include crystalline silicon solar cells, thin film solar cells, space and concentrator solar cells, organic and dye sensitized solar cells [10].

This thesis follows the style of Solar Energy Materials & Solar Cells.

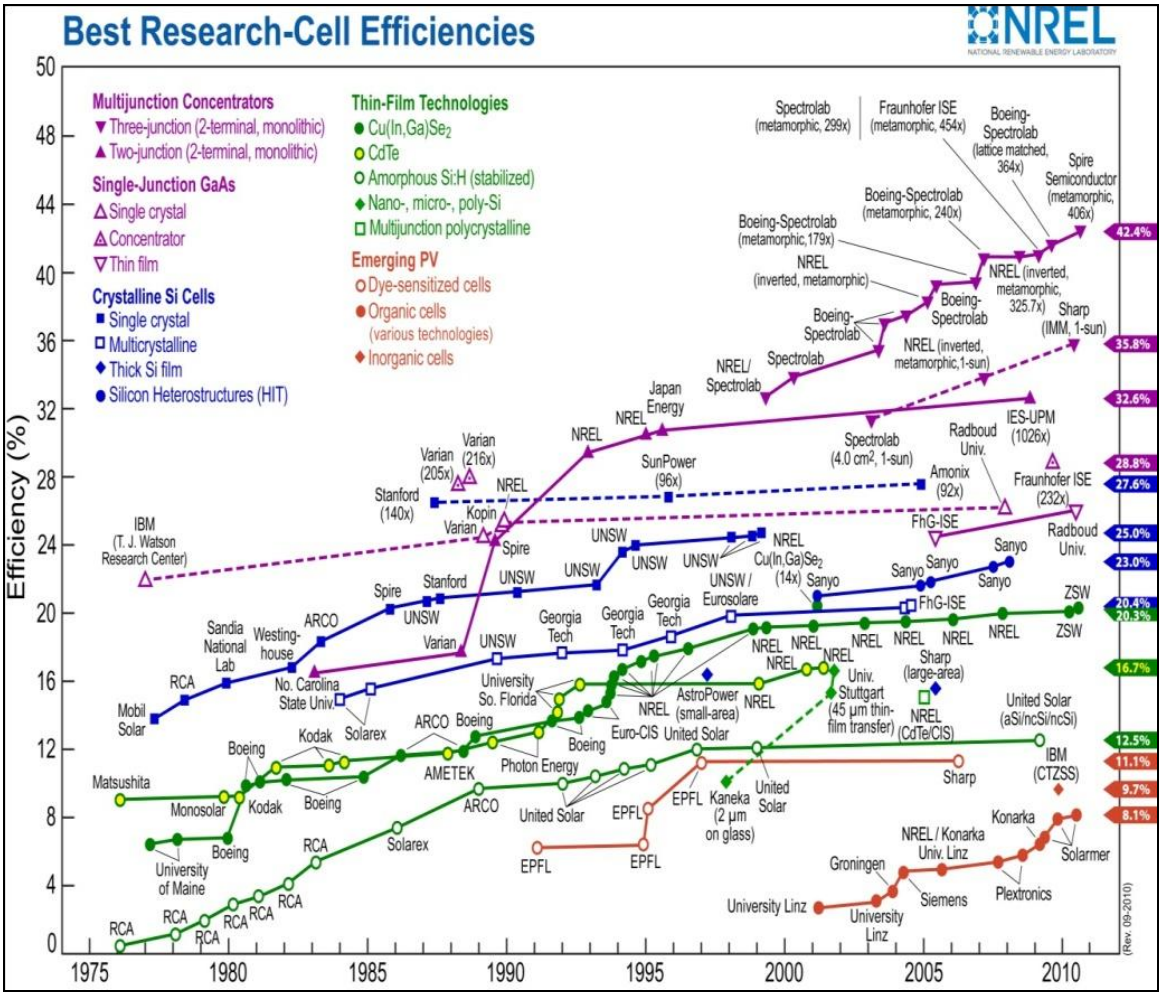

Fig. 1. Research cell efficiencies reported and summarized by NREL [9].

To meet the power demand of a specific application, solar cells are assembled into solar modules to output specific voltage and current [10]. The electric power generated by the solar modules (or solar panels) is referred to as solar power [10]. Among renewable energies, solar power has the highest power density and generates no pollution during operation [10]. Solar power is superior to power grid connection or fuel transport for providing electric power in remote areas in regard to cost and convenience

[10]. Compared to existing power technologies, solar power system requires little maintenance and incurs very low operation costs [10]. The advantages of solar power have driven the developments of various solar power applications such as solar power plants, solar power buildings, solar-charged vehicles, and solar powered satellites [10].

Solar energy has grown by an average of 30% per annum accompanied with rapid decline in costs over the past 20 years [11]. This decline in cost has been driven by economies of manufacturing scale, manufacturing technology improvements, and the increased efficiency of solar cells [11]. The cost is proportional to the area for solar modules [10]. Improvement in efficiency of each solar cell in a module means the reduced number of solar cells needed to output the same power [10]. However, solar power accounted for less than 1% of the total energy matrix of which 78% was dominated by fossil fuels in 2010 [11]. The main barrier for the wider deployment of solar energy is the relative higher production costs of solar energy compared to fuel energy [10]. Improving efficiency and reducing cost are on the same level of importance to make solar energy more attractive on the market. Crystalline silicon modules dominated 95 percent of the photovoltaics (PV) market in 2005 but the costs reduction has been limited by the expensive silicon wafers [11]. Since then thin film modules have steadily increased their market share and have taken over 25% of the PV market in 2010 [12]. Compared to silicon based modules that have 12 to 18% conversion efficiencies, thin film modules have conversion efficiency of 6 to 11% [12]. The production cost of thin film modules is 20% less than that of silicon based modules and is expected to continue dropping [12]. Owning to the cost advantage and the greater potential of

efficiency improvement, thin film solar technology has gained significant attention from researchers and has become a promising solution for achieving low cost and efficient solar energy applications [11].

1.2 Principles of Solar Cells

1.2.1 Photovoltaic Process of Solar Cells

Solar cells are solid state devices based on p-n junction which is designed and constructed to efficiently convert light energy into electrical energy [13]. The p-n junction is made by bringing n-type semiconductor and p-type semiconductor together to form a metallurgical junction [13]. An energy band diagram depicted in Fig. 2 is used to illustrate the photovoltaic process that converts light into electric current in a solar cell [13]. The first step involves the absorption of light in semiconductor and generation of carriers—electrons and holes [13]. The second step involves the separation of the carriers by the electric field of the junction. The separated carriers move in a specific direction and contribute to the electric current [13]. The energy of photons E_λ is dependent on the wavelength λ and is given by

$$E_\lambda = \frac{hc}{\lambda} \tag{1.1}$$

where h is Plank's constant and c is the speed of light [13]. Only the photon with energy greater than the semiconductor band gap (E_g) can generate an electron-hole pair and contributes to the photovoltaic process [13]. Thus the match between the semiconductor band gap (E_g) and spectral nature of sunlight is an important consideration in the design of efficient solar cells [13].

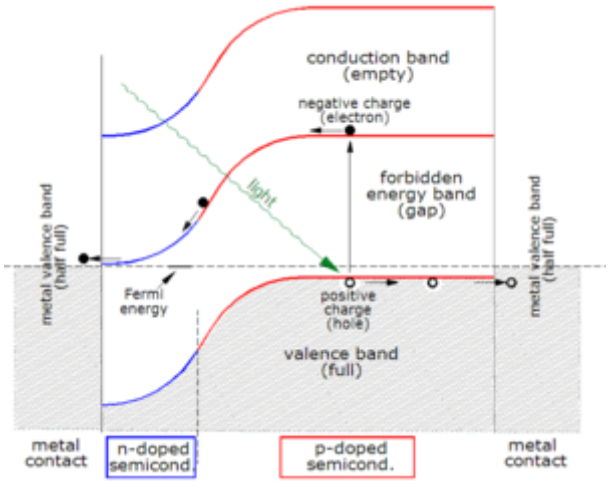

Fig. 2. Energy band diagram of a p-n junction solar cell [14].

The concentration of carriers generated by the photovoltaic process tends to relax back from non-equilibrium values toward equilibrium values through recombination [13]. The recombination mechanisms include recombination through traps (defects) in the forbidden gap, radiative (band-to-band) recombination, and Auger recombination [13]. The recombination through traps is commonly related to the carrier lifetimes given by

$$\tau = \frac{1}{\sigma \upsilon_{th} N_T} \tag{1.2}$$

where σ is the capture loss section, υ_{th} is the thermal velocity of the carrier, and N_T is the concentration of the traps [13]. The capture loss section can be imagined as the size of the traps present to a carrier traveling through the semiconductor at velocity υ_{th} [13]. Small carrier lifetimes correspond to high rates of recombination [13]. Radiative recombination is the emission of photons through recombination of electron-hole pair

[13]. In Auger recombination, the energy of a carrier is given to another carrier which then releases its excess energy and momentum to phonons [13]. Interfaces between two dissimilar materials have a high concentration defect due to the abrupt termination of the crystal lattice [13]. These interfaces act as a continuum of traps within the forbidden gap at the surface where carriers can recombine through them just as with bulk traps [13]. These recombination processes are therefore the sources of electrical loss in solar cells.

1.2.2 Current-Voltage Characteristics of Solar Cells

A solar cell is evaluated by four parameters obtained from its current-voltage (I-V) characteristic under illumination [13]. These four parameters include: open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}) in mA/cm^2, fill factor (FF), and efficiency (η) [13]. The short-circuit current density (J_{sc}) is obtained from the short-circuit current I_{sc} divided by the effective area of the solar cell [13]. The I-V characteristic of the solar cell is derived by solving the minority carrier diffusion equation with appropriate boundary conditions [13]. The current is given by equation

$$I = I_{sc} - I_{o1}(e\frac{qV}{kT} - 1) - I_{o2}(e\frac{eV}{2kT} - 1) \tag{1.3}$$

where I_{sc} is the sum of the photocurrent contributed from the n-type region, the depletion region, and the p-type region [13], I_{o1} is the dark saturation current owing to recombination in the quasi-neutral region [13], I_{o2} is the dark saturation current due to recombination in the space-charge region [13], q is the elementary charge 1.6 x 10^{-19} Coulombs, k is a constant of value 1.38 x 10^{-23} J/K, T is the cell temperature in Kelvin, and *V* is the measured cell voltage [13]. A solar cell is typically modeled by an ideal

current source in parallel with two diodes – one with an ideality factor of 1 and the other with an ideality factor of 2 as shown in Fig. 3 [13].

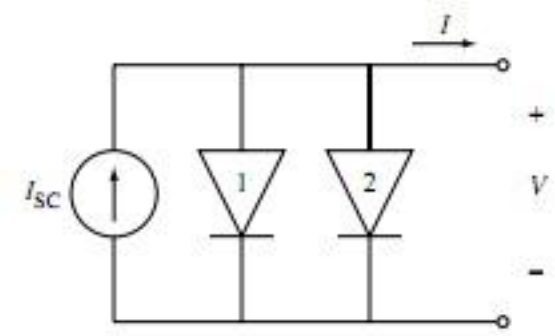

Fig. 3. Simple solar cell circuit model [13].

The current-voltage characteristic of a silicon solar cell is plotted in Fig. 4 [13]. For simplicity, the dark current due to depletion region (diode 2) is ignored, then at open circuit (I=0), all the light generated current, I_{sc}, flows through diode 1, so the open-circuit voltage is written as

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{I_{sc} + I_{o1}}{I_{o1}}\right) \approx \frac{kT}{q}\ln\left(\frac{I_{sc}}{I_{o1}}\right) \tag{1.4}$$

where $I_{sc} >> I_{o1}$.

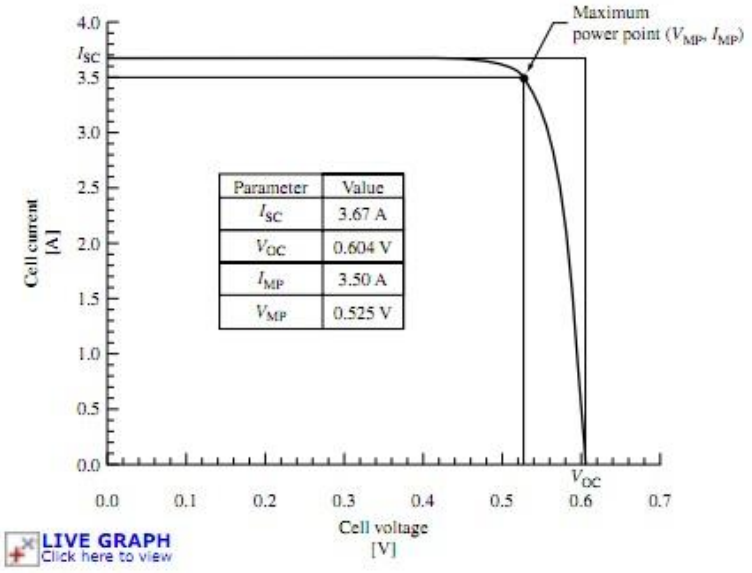

Fig. 4. Current-voltage characteristic of a silicon solar cell [13].

The maximum power point defines the largest rectangular for any point on the I-V characteristic with an area given by $P_{mp} = V_{mp}I_{mp}$ [13]. The fill factor, FF, is used to measure the squareness of the I-V characteristic and is always less than one [13]. The FF is given by

$$FF = \frac{P_{mp}}{V_{oc}I_{sc}} = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \tag{1.5}$$

The most important figure of merit for the solar cell is the power conversion efficiency, η, which is defined as

$$\eta = \frac{P_{mp}}{P_{in}} = \frac{FFV_{oc}I_{sc}}{P_{in}} \tag{1.6}$$

where P_{in} is taken as the product of irradiance of incident light measured in W/m^2 [13]. The standard Global AM 1.5 Illumination, equivalent to power density of 1000 W/cm^2, is commonly used in calculating efficiency [13]. The efficiency is not only affected by the above parameters but also affected by various conditions such as temperature, light intensity and light spectrum [13].

In reality a solar cell typically has series resistance and shunt resistance [13]. A simplified circuit model which includes the diode ideality factor n, the series resistance R_s and the shunt resistances R_{sh} is shown in Fig. 5 [13]. The previous equation for defining current is expanded and becomes

$$I = I_{sc} - I_{o1}(e\frac{q(V+IR_s)}{kT} - 1) - I_{o2}(e\frac{e(V+IR_s)}{2kT} - 1) - \frac{V+IR_s}{R_{sh}} \qquad (1.7)$$

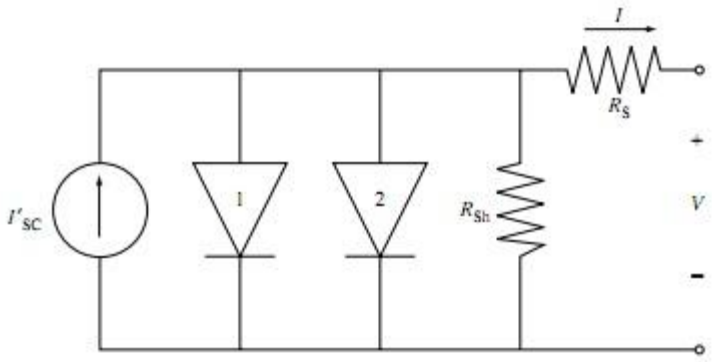

Fig. 5. Solar cell circuit model including series resistance R_s and shunt resistance R_{sh} [13].

The cell efficiency is limited mostly by R_s and R_{sh} which are measure of the loss originated from the recombination processes in solar cells [13]. The effect of R_s on I-V characteristic of a solar cell is shown in Fig. 6 [14]. R_s of large values over 1 Ω/cm^2 significantly reduces the current and fill factor. Fig. 7 shows the effect of R_{sh} on I-V characteristic [14]. Low R_{sh} drastically reduces current, voltage, and fill factor. High efficiency solar cells typically show very small R_s (typically less than 1 Ω/cm^2) and large R_{sh} (from several hundred to over a thousand Ω/cm^2) [13].

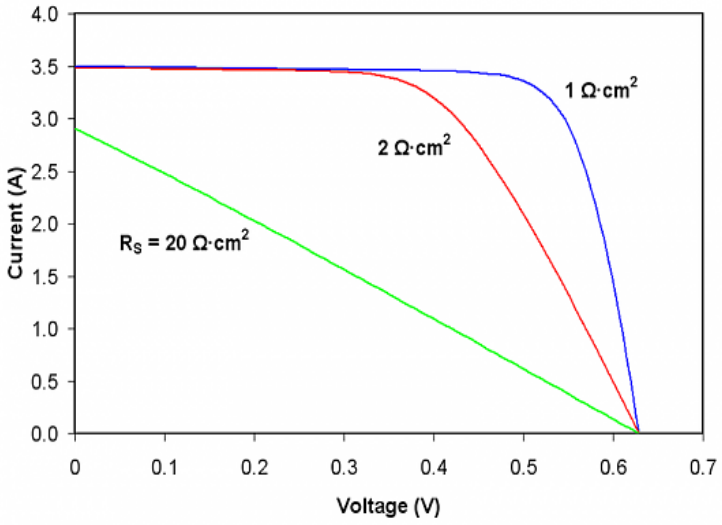

Fig. 6. Effect of the series resistance on I-V characteristic [14].

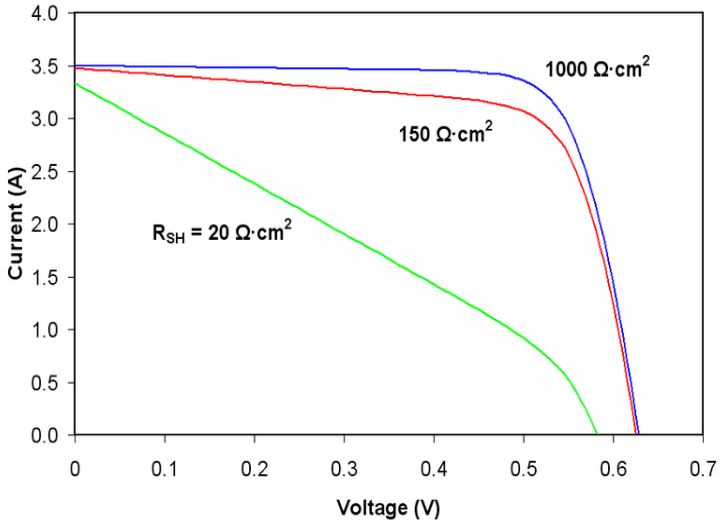

Fig. 7. Effect of the shunt resistance on I-V characteristic [14].

1.2.3 Homojunction and Heterojunction

Typically, the p-n junction of solar cells can be homojunction or heterojunction which depends on the materials that form the junction between the window layer and absorber layer [13]. Homojunction uses the same material for absorber layer and window layer [13]. Silicon solar cells are mostly based on homojunction because silicon can be doped both n-type and p-type. The energy band diagram of a homojunction solar cell is shown in Fig. 8 [13]. One advantage of the homojunction is perfect alignment of energy band in the p-n junction that prevents formation of barriers resulting in interface states [13]. The window layer must be thinned down to reduce photon loss, but very thin window layer can encounter increased surface recombination [13].

Most efficient thin film solar cells to date utilize heterojunction. The energy band diagram of heterojunction is shown in Fig. 8 [13]. Heterojunction is superior to homojunction in that wide band gap material can be used for window layer and low band gap material can be chosen for absorber layer [13]. Heterojunction is convenient when certain semiconductor materials are difficult to be doped both types [13]. However, the band bending in heterojunction results in the formation of barrier [13]. Heterojunction suffers from interface states issue and contaminants due to interdiffusion between the two dissimilar materials [13]. The complexities such as intermediate compositions, different phases, lattice mismatch makes analysis of heterojunction solar cells more difficult than that of homojunction by current available models [13].

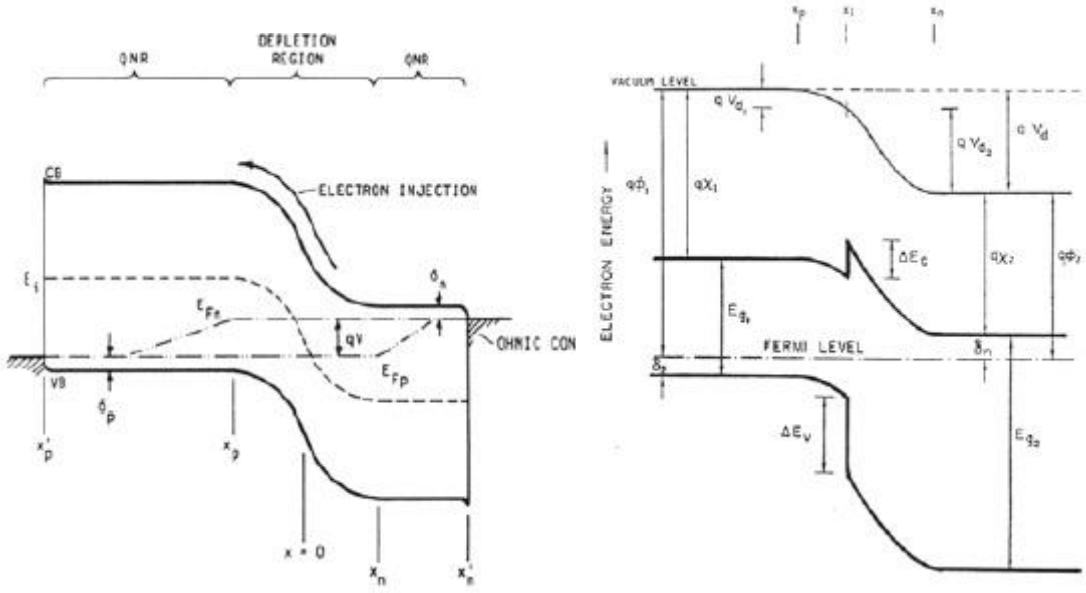

Fig. 8. Energy band diagram of the homojunction (left) and the heterojunction (right) [13].

1.3 Challenges of Solar Cells

1.3.1 Efficiency Limit of Solar Cells

The inevitable loss mechanisms such as black body emission, spectrum loss, and recombination impose a theoretical efficiency limit on solar cells [13]. Improving the efficiency of solar cells toward the theoretical efficiency limit is an everlasting task in solar cell research. Many researchers have attempted to predict the theoretical limit since 1954 [13]. One of such acknowledged prediction is the detailed balance limit described by William Shockley *et al.* in 1961 [15]. The approach used by Shockley *et al.* is the calculation of efficiency as a function of band gap for hypothetical semiconductors with step function optical absorptions [15]. In this approach, only radiative recombination was included with spectrum loss and black body emission as loss mechanisms for calculation [15]. Another important prediction was developed by M. Wolf and D. Redfield in early 1980s [16-17]. In their approach, the efficiency was calculated on an optimized device of a particular device structure from the properties of materials [16-17]. These two earlier approaches were further corrected by T. Tiedje *et al*. with inclusion of free carrier absorption and Auger recombination in loss mechanisms for calculation [18]. T.Tiedje *et al.* predicted the limiting efficiency for crystalline silicon solar cells is 29.8% under AM 1.5 for a 100 μm silicon solar cell [18]. The thickness reduction was predicted to enhance built-in electric field and carrier collection in solar cells [18]. This has driven solar cell researchers to constantly reduce the solar cell thickness not only for achieving lower cost but also for higher efficiency.

Fig. 9 shows the calculated theoretical efficiency limit and best confirmed efficiency as a function of the band gap of the absorber materials in a simple p-n junction solar cell [19]. For the determination of the efficiency limit, important assumptions include: first, the surface is textured to allow full randomization of the incident light for maximum enhancement of the optical absorption through light trapping; second, the front surface has a perfect antireflection coating and back surface has a perfect reflecting coating [18]. The determination, however, exclude the loss mechanisms such as surface recombination and effect of the carrier concentration [18]. The efficiency gap is thus a measure of how well a solar cell can be constructed to match the ideal condition of these assumptions and minimize loss originated from above recombination processes.

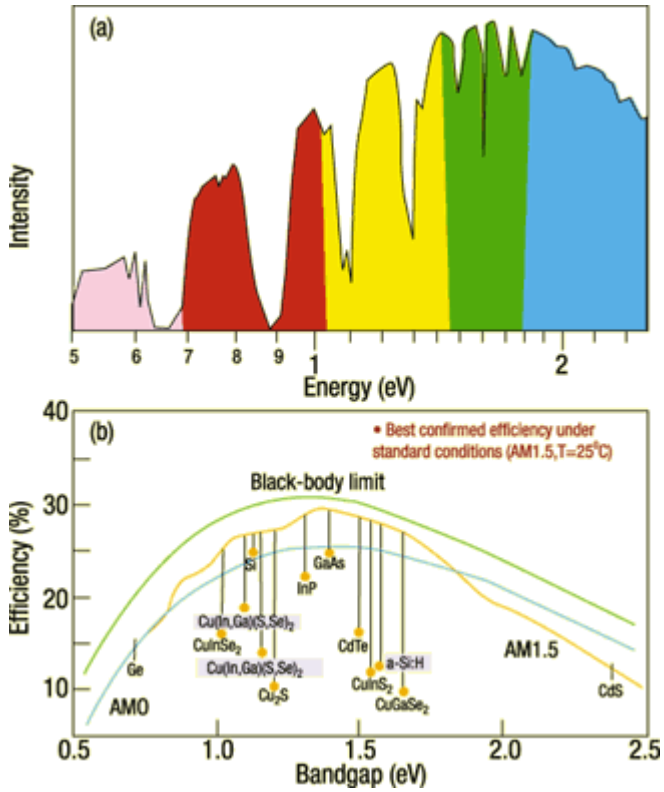

Fig. 9. Efficiency as a function of band gap for solar cells [19].

1.3.2 Issues in Thin Film Solar Cells

Light trapping, as one of the assumptions made for determining the efficiency limit, has driven the development of light trapping schemes for solar cells. The light trapping scheme deflects the incident light away from the angle of incidence at the interface and traps light inside the absorber material [20]. Light trapping scheme can increase the optical absorption path inside the material from 2L to $4n^2L$, where L is the thickness of the absorber layer and n is the refractive index of the absorber material [20].

The light trapping has been experimented to increase current density by 10% for crystalline silicon solar cells [21].

For thin film solar cells, light trapping scheme has not been researched as extensive as other optimization schemes for absorber layer, window layer, transparent electrodes, and back contact layer [13]. The thickness of most high efficiency thin film solar cells are thick enough to allow complete absorption which eliminate the need of light trapping scheme [13]. For example, the 16.5% efficient thin film CdTe solar cells made by X. Wu *et al*. as well as other high efficiency CdTe solar cells typically utilized an absorber layer of 8 to 10 μm thickness [22, 33]. Ultra thin film solar cells with absorber layer of less than 1 μm thickness typically yield lower efficiency [23]. For example, A. D. Compaan *et al.* achieved 11.2% efficient CdTe solar cells with 0.7 μm thick absorber layer [23]. The lower efficiency in thinner CdTe solar cells could be caused by deep penetration loss, pinholes, weak diodes, fully depleted layers, and proximity of front and back contacts [24]. The penetration loss means the current loss associated with the semi-transparency for the longer wavelength when the absorber layer is thinner than 1 μm [24]. Therefore compensation of penetration loss necessitates the use of light trapping scheme in thin film solar cells.

1.4 Scope of the Work

1.4.1 New Light Trapping Scheme

The light trapping scheme has been experimentally proven effective to enhance cell performance. Representative light trapping schemes include “inverted pyramid” and

"honeycomb" surface texturing in silicon solar cells, silicon nanowire arrays, and V-shaped layer structure [25-27]. The former two schemes rely on etching and photolithography which add substantial costs and complexity in fabrication. The latter scheme requires a large bending angle of substrate and could be problematic when applying to conventional thin film solar cells which use glass substrate.

In this research, a new light trapping scheme based on light trapping transparent conducting oxide (LT-TCO) layer for thin film solar cells is proposed. This LT-TCO layer features surface texture, good conductivity, and high transmittance. The surface texture of the LT-TCO layer is achieved by deposition technique only. Fig. 10 shows three different configurations proposed to incorporate the LT-TCO layer in thin film solar cells. These three configurations are different in the number of LT-TCO layer utilized and the position of the LT-TCO layer. In the case of crystalline silicon solar cells, the short-circuit current density as a function of cell thickness for different light trapping schemes has been calculated by P. Cambell *et al.* [28] and summarized in Table 1. The calculation shows that cells with random surface texture for both top and rear surfaces have the highest current density [28]. Cells with surface texture for only one surface have higher current density than cells without surface texture [28]. The cell integrated with single LT-TCO layer as back electrode could have improved current by enhanced back reflection. The cell integrated with single LT-TCO layer as front electrode is projected to have higher current density than the cells with single LT-TCO layer as back electrode. Finally, the cell integrated with two LT-TCO layers is expected to have the strongest light trapping effect and thus highest current density.

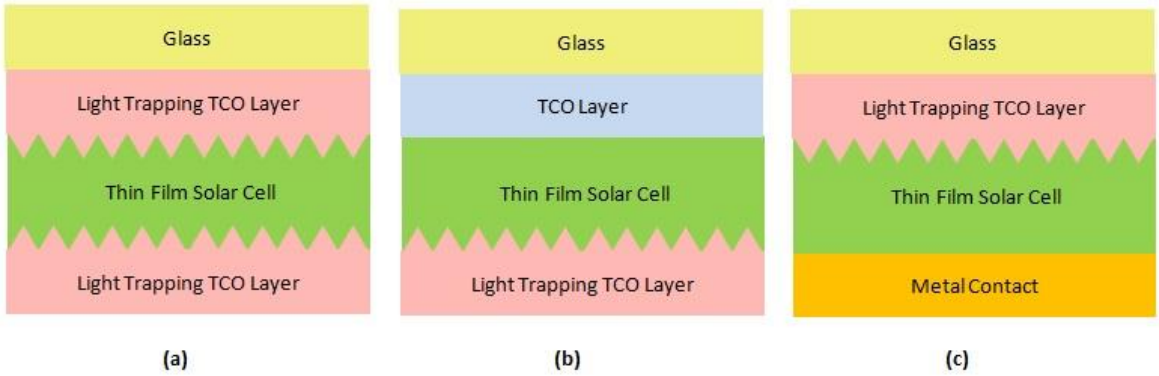

Fig. 10. New configurations of LT-TCO layer for thin film solar cells: (a) double LT-TCO layers; (b) back LT-TCO layer; (c) front LT-TCO layer.

Table 1 Calculated limits on silicon solar cell short-circuit current densities in mA/cm^2 for different light trapping schemes. The rear surface reflectivity, R, has a value of unity except where indicated otherwise [28].

	Short-circuit current (mA/cm^2)	
Light Trapping scheme	80-μ cell	320-μ cell
Polished (top and rear)		
R=0	35.9	40.1
R=1	37.6	40.2
Pyramids (top surface only)		
Regular	39.0-39.5	41.1-41.4
Random	40.0	41.7
Pyramids (top and rear)		
Regular	41.0	42.4
Random	41.6	42.7

1.4.2 Pulsed Laser Deposition

Pulsed laser deposition (PLD) is a physical vapor deposition (PVD) process [29]. Fig. 11 shows the schematic diagram of a typical PLD system [30]. The pulsed laser with ultraviolet wavelength and nanosecond pulse width is focused onto a rotating target of material at an incident angle of 45°. With sufficient high energy density, each laser pulse ablates a small amount of the material and forms a plasma plume [29]. This plume consists of atomic, diatomic, and other low-mass species with kinetic energy dependent on the laser energy density [29]. The ablation plume supplies the material flux for thin film growth [29]. The substrate is attached intimately with a surface parallel to the target surface at optimal target-to-substrate distance [29]. The substrate is usually heated to specific temperature in couple with optimal laser energy density to obtain desired properties of thin films [29]. The laser beam is scanned over a sufficiently large target area in order to minimize the modification of target surface [29]. Multi-layers with desired thickness can be achieved by simply adjusting the number of laser pulses and repetition rate of laser [29].

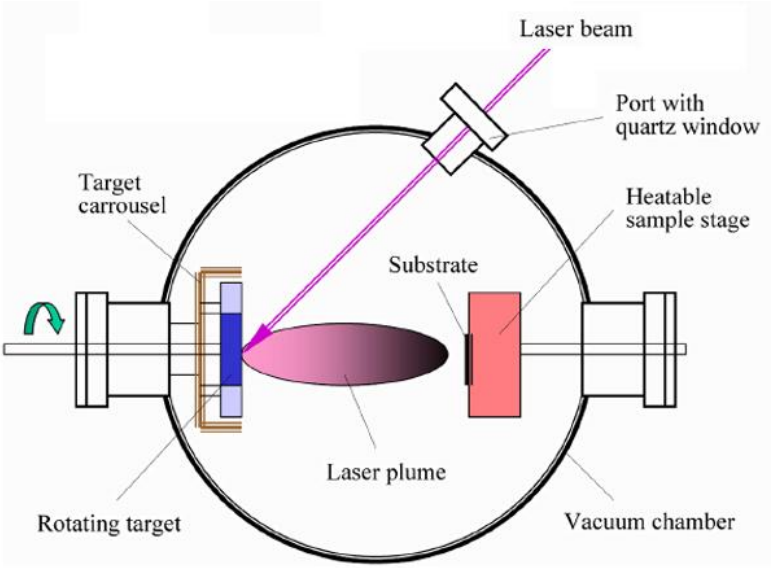

Fig. 11. Schematic diagram of PLD [30].

PLD has been chosen in this research to fabricate the thin film solar cells with LT-TCO layer for several reasons. First, PLD can deposit different layers from oxide materials for TCO layer to semiconductor materials for p-n junction formation within one chamber. Second, PLD can tune the thin film properties by controlling the background pressure from ultra high vacuum (UHV) to 1 Torr [31]. The gas ambient can be changed among vacuum, oxygen, and argon to suit the growth of specific materials [31]. Third, PLD is advantageous in transferring the stoichiometry of target to that of thin film irrespective of different vapor pressures of the elements [31]. Finally, PLD is a cost efficient deposition because the small laser spot of the focused laser beam allows for using targets of small diameter and efficient usage of materials [31].

1.4.3 Research Design

In the first phase of this research, the LT-TCO layer was fabricated by PLD deposition of Al doped ZnO material (AZO). The AZO thin films are suitable for making the LT-TCO layer because the surface morphology of AZO films can be controlled by oxygen pressure during PLD deposition. This unique feature of AZO film has been demonstrated by J. H. Lee *et al*. [32]. The AZO deposited with oxygen was found to have higher resistivity and surface roughness [32]. The AZO deposited without oxygen was found to have lower resistivity and smooth surface [32]. Multilayer structure has been chosen to combine these two different AZO films for making the LT-TCO layer. The light trapping function of the LT-TCO layer was examined by optical transmittance measurement. The conductivity of LT-TCO layer was measured by resistivity measurement. Microstructure of the LT-TCO layer was characterized by X-ray Diffraction (XRD) and Transmission Electron Microscopy (TEM).

In the second phase of this research, baseline thin film CdTe/CdS heterojunction solar cells are fabricated for integration of the LT-TCO layer. CdTe layer is the p-type absorber layer and CdS layer is the n-type window layer. The thin film CdTe/CdS solar cells were fabricated by PLD at low temperature. The thickness of the CdTe absorber layer is intentionally set to 1 μm to allow ~10% light penetration. The solar cells fabricated were further processed with various post-deposition treatments such as air annealing, argon annealing, vacuum annealing, and $CdCl_2$ treatment. These treatments have been reported effective in improving cell efficiency for previous high efficiency CdTe/CdS solar cells. The effects of post-deposition treatments were analyzed by I-V

characteristics of solar cells. The effects of these treatments were examined through a series of microstructure analysis by XRD, Scanning Electron Microscopy (SEM), and TEM.

2. LIGHT TRAPPING TRANSPARENT CONDUCTING OXIDE LAYER

2.1 Introduction to LT-TCO Layer

There exist various transparent electrodes that differ in the type of materials used. The most notable transparent electrodes use Tin-doped Indium Oxide (ITO), Fluorine-doped Tin Oxide (SnO_2:F), and Al-doped Zinc Oxide (AZO) [33]. AZO film has replaced the more expensive ITO film as preferential transparent electrode for thin film CIGS [Cu(In, Ga)Se_2] solar cells and thin film amorphous silicon solar cells [33]. The AZO, with higher transmittance and better conductivity, in replacement of SnO_2:F has been demonstrated to improve J_{sc} in thin film CdTe solar cells [34].

Besides of the low cost, high transmittance, and competitive conductivity, surface roughness of AZO film promise AZO film as a strong candidate for making the LT-TCO layer with surface texture and low resistivity. Transparent electrodes for solar cells typical require sufficient low resistivity of least less than 10^{-3} Ω-cm [10]. The resistivity of AZO films with desired surface roughness deposited at high temperature, however, has relatively high values from 0.01 to 0.1 Ω-cm [32]. Such AZO film with thicker film thickness is required for making a transparent electrode of sufficient low resistance. The photon loss associated with the thicker film thickness can offset the photon gain from light trapping effect.

In this research, PLD deposition of AZO film at low temperature has been explored to improve the conductivity and to obtain the surface texture by tuning the oxygen pressure. AZO film deposited with oxygen is denoted by OAZO film and AZO

film deposited in vacuum is denoted by VAZO film. The OAZO film with surface texture is combined with the more conductive VAZO film in a multilayer film to form the LT-TCO layer. Fig. 12 shows the OAZO/VAZO multilayer film and the VAZO/OAZO multilayer film fabricated. Fabrication and characterizations of these two potential LT-TCO layers will be discussed in parallel with the VAZO single layer film and the OAZO single layer film.

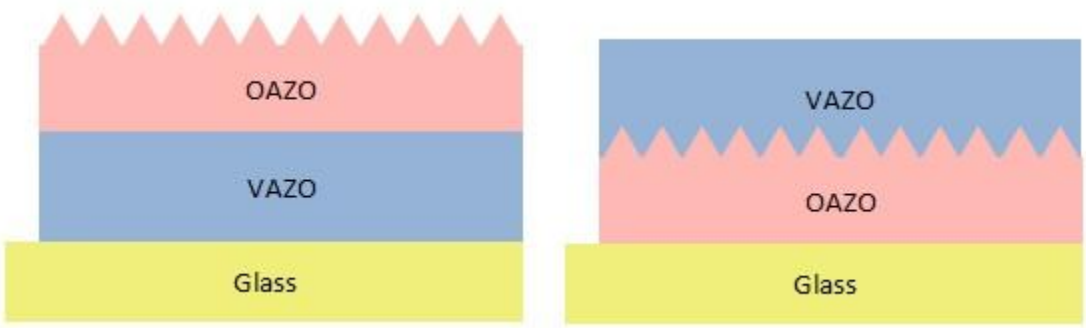

Fig. 12. Structure of the OAZO/VAZO multilayer (left) and the VAZO/OAZO multilayer (right).

2.2 Material Properties

AZO is ZnO doped with Al impurities. ZnO is a II-VI n-type semiconductor with a direct wide band gap of about 3.3 eV at room temperature and a hexagonal wurzite structure as shown in Fig. 13 [10]. The AZO films are wide band gap semiconductors (E_g = 3.4 to 3.9 eV) which show good optical transmittance in the visible and near-infrared regions [35]. The doping of ZnO with Al improves the stability and electrical conductivity [35]. Resistivity of AZO has been reported to be 2 to 5 x 10^{-4} Ω-cm [35]. In

addition, ZnO is nontoxic, inexpensive, and abundant on earth [35]. The cost advantage and excellent electrical and optical properties of AZO have been the driving force behind the developments of AZO films with better conductivity, transmittance, and stability.

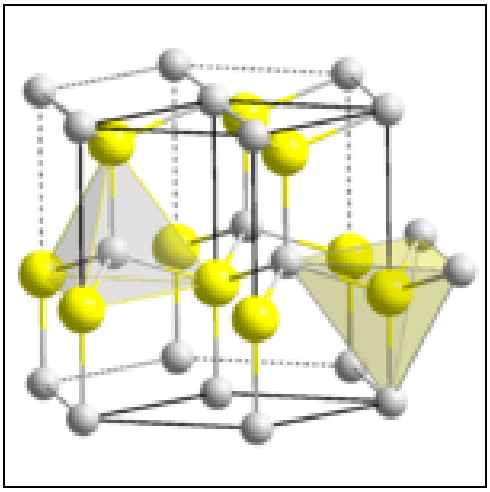

Fig. 13. Atomic structure of ZnO [10].

2.3 Fabrication of LT-TCO Layer

2.3.1 Target Preparation

The AZO target was made by mixing ZnO (99.999%) powder with 2 wt% Al_2O_3 powder. The powder mix was ball milled for 90 minutes and pressed at 8.7 x 10^6 Pascal to form a dense circular disk target of 1 inch diameter. The target was immediately sintered at 1050 °C in flowing oxygen (0.15 sccm) for 6 hours. Both of the VAZO thin films and the OAZO thin films were deposited using this target.

2.3.2 OAZO and VAZO Single Layer

The OAZO single layer film and the VAZO single layer film were deposited on glass substrate as shown in Fig. 14. Both of the OAZO layer and the VAZO layer were deposited by a KrF laser (248 nm) with laser energy density fixed at $2J/cm^2$ and repetition rate of 5 Hz. The substrate temperature was fixed at 300 °C. The background pressure was 1×10^{-6} Torr for deposition of the VAZO layer. The background pressure was 0.2 Torr of oxygen for the deposition of OAZO layer. Deposition rate is 1 Å/laser pulse for the OAZO layer and is 0.8 Å/laser pulse for the VAZO layer. The OAZO single layer was 100 nm and the VAZO single layer was 365 nm. Fig. 15 shows the appearance of the 100 nm OAZO film and 365 nm VAZO film.

Fig. 14. Structure of the OAZO single layer (left) and the VAZO single layer (right).

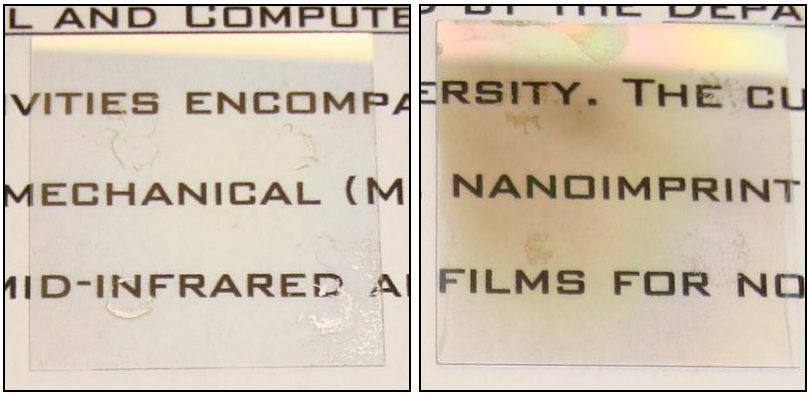

Fig. 15. Appearance of the OAZO single layer (left) and the VAZO single layer (right).

2.3.3 OAZO/VAZO and VAZO/OAZO Multilayer

Film structure of the OAZO/VAZO multilayer and the VAZO/OAZO multilayer deposited on glass substrate is shown in Fig. 16. The OAZO/VAZO multilayer was fabricated by sequential deposition of the VAZO layer followed by the OAZO layer. The OAZO/VAZO multilayer has 100 nm OAZO deposited on the 300 nm VAZO. The VAZO/OAZO multilayer was deposited by sequential deposition of the OAZO layer followed by the VAZO layer. The OAZO layer The VAZO/OAZO multilayer has 300 nm OAZO film deposited on the 100 nm VAZO film. Fig. 17 shows the appearances of the OAZO/VAZO multilayer and the VAZO/OAZO multilayer of which total thickness was around 400 nm.

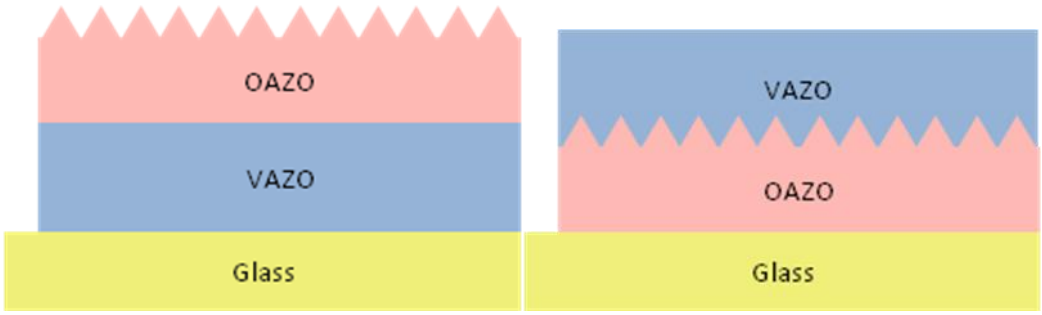

Fig. 16. Structure of the OAZO/VAZO multilayer (left) and the VAZO/OAZO multilayer (right).

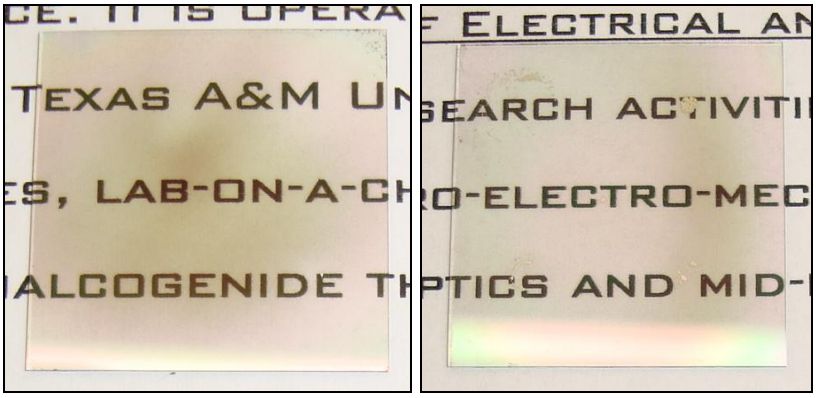

Fig. 17. Appearance of the OAZO/VAZO multilayer (left) and the VAZO/OAZO multilayer (right).

2.4 Results and Discussion

2.4.1 Optical Properties

Optical transmittance measurements were conducted on the four types of AZO films that differ in oxygen pressure and film structures. Fig. 18 shows optical transmittance spectra (%) versus wavelength for these AZO films. The 365 nm VAZO film shows 50 to 75% transmittance in the range from 400 nm to 800 nm. The 100 nm OAZO film has 80 to 100% transmittance in the similar range which indicates growth of

AZO in oxygen results in better crystallinity and high transmittance. The OAZO film shows evident transmittance reduction in the range from 500 nm to 1100 nm. The transmittance reduction is quite uniform and independent of the wavelength. The assumption is that the surface texture of OAZO film reflects and scatters incident light resulting in transmittance reduction. The transmittance reduction is also observed in the VAZO film but starts at longer wavelength (900 nm). This transmittance reduction, however, could be in part due to the absorption of free-carriers in the VAZO film.

The transmittance spectrum of the VAZO film shows an absorption edge at around 320 nm and a smooth wave form right after the absorption edge. This smooth waveform suggests that the VAZO film has smooth surface and high epitaxial quality. The spectrum of the OAZO layer shows an absorption edge at 340 nm and a form with one wave after the absorption edge which indicates the film has rough surface. The blue shift of the absorption edge observed in the VAZO film suggests higher carrier concentration and wider band gap. The sharper absorption edge observed in the OAZO film indicates that the film has lower defect density and film stoichiometry close to intrinsic ZnO.

The spectrum of OAZO/VAZO multilayer film shows 5 to 10% transmittance reduction in the visible wavelength and evident 15% transmittance reduction after 800 nm in comparison to that of the VAZO film. The 300 nm VAZO film in the OAZO/VAZO multilayer structure has higher transmittance than the 365 nm VAZO film. Therefore the transmittance reduction is estimated much higher than the observed values shown by the spectrum. This transmittance reduction is assumed to be originated

from the OAZO cap layer that provides enhanced reflection and scattering important to light trapping effect. In sharp contrast, the spectrum of the VAZO/OAZO multilayer film shows overall increased transmittance in comparison to that of the VAZO single layer. The absorption edge of the VAZO/OAZO multilayer film is observed to be sharper than that of the OAZO/VAZO multilayer film. The different waveform observed in the VAZO/OAZO multilayer film suggests smooth surface consistent with the VAZO cap layer.

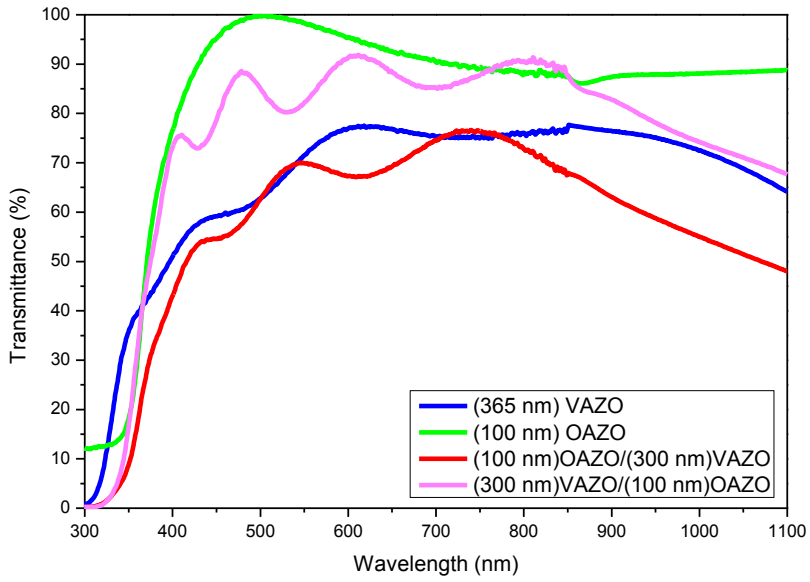

Fig. 18. Optical transmittance spectra of the VAZO single layer, the OAZO single layer, the OAZO/VAZO multilayer, and the VAZO/OAZO multilayer.

2.4.2 Electrical Properties

Resistivity of AZO thin films was measured by four-point probe at room temperature and plotted as a function of oxygen pressure in Fig. 19. The resistivity was varied from 4 x 10^{-4} Ω-cm for the VAZO film to 8 x 10^{-3} Ω-cm for the OAZO film. The higher resistivity of OAZO film is as assumed to be caused by compensation of the zinc interstitials and oxygen vacancies by oxygen during the film growth resulting in lower carrier concentration. The higher carrier concentration of the VAZO film is supported by the blue shift of transmittance spectrum and free-carrier absorption observed in the transmittance spectrum. PLD deposition of AZO with lower oxygen pressure and lower substrate temperature results in lower resistivity. The resistivity of 8 x 10^{-3} Ω-cm for OAZO films deposited with 0.2 Torr at 300 °C is much lower than 0.106 Ω-cm for AZO films deposited with 0.25 Torr at 750 °C [32]. The resistivity of the OAZO/VAZO multilayer film is found to be slightly higher than that of the VAZO film and is controlled by the more conductive VAZO film. The VAZO/OAZO multilayer film has the lowest resistivity of 1.5 x 10^{-4} Ω-cm, close to 1.3 x 10^{-4} Ω-cm for commercial ITO film. The VAZO/glass film has a low resistivity of 4 x 10^{-4} Ω-cm which is better than 7 x 10^{-4} Ω-cm for SnO_2. The resistivity of VAZO layer is reduced when it is grown on the existing OAZO film than on the glass substrate.

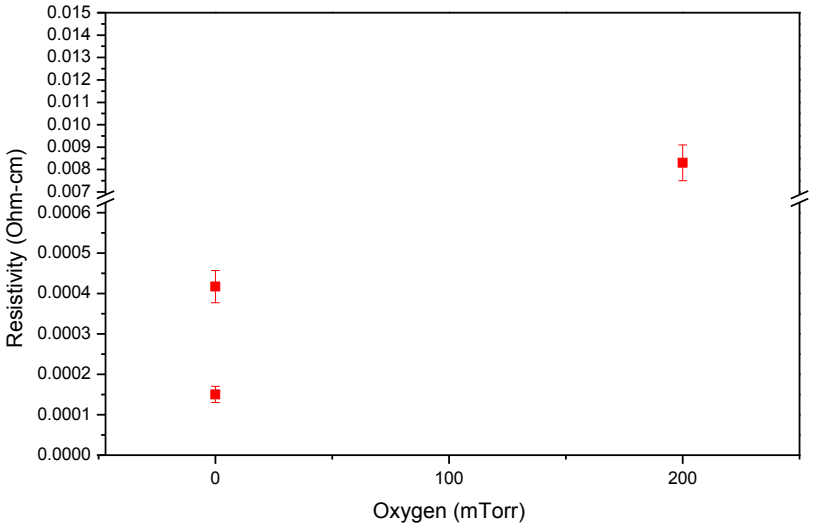

Fig. 19. Resistivity of AZO films as a function of oxygen pressure.

Argon annealing has been conducted on the VAZO films to examine film stability at elevated temperature. The VAZO films were annealed at different temperatures in argon of 1 atmosphere for 20 minutes. The resistivity of VAZO films was plotted as a function of annealing temperature in Fig. 20. In Fig. 20, there is minimal change of the resistivity at room temperature and that after annealing at 300 °C. The resistivity of the VAZO film increases slightly from 6 x 10^{-4} Ω-cm to 7 x 10^{-4} Ω-cm after annealing at 400 °C. Resistivity is further raised up to 1 x 10^{-3} Ω-cm after annealing at 500 °C. The resistivity of VAZO film after argon anneal at 400 °C is still close to that of doped SnO_2 [32]. These results demonstrate that the electrical conductivity of the VAZO film is compatible to subsequent fabrication process at 400 °C without evident degradation.

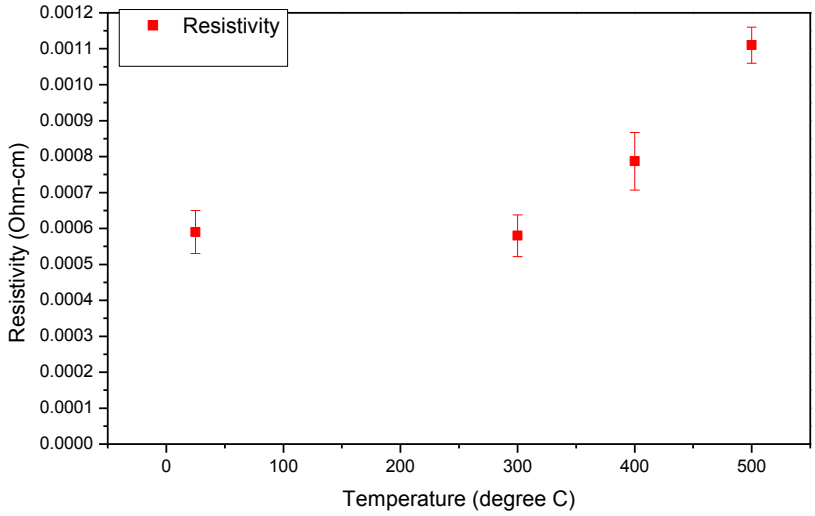

Fig. 20. Resistivity of AZO films as a function of annealing temperature.

2.4.3 Microstructure Properties

XRD scans of AZO single layer films and multilayer films are plotted in Fig. 21. All AZO thin films, despite of different structures, have the same preferred growth along [0002] direction. The peak position of ZnO(0002) shifts from 34.39° to 34.57° as the oxygen pressure changes from vacuum to 0.2 Torr. This peak shift corresponds to the reduction of the d-spacing of the ZnO(0002) from 2.605 Å to 2.593 Å as the oxygen pressure increases. Compared with the bulk value, $d_{ZnO(0002)}$ = 2.603 Å, the VAZO film deposited in vacuum with $d_{ZnO(0002)}$ of 2.605 Å is in tension out of plane and in compression in-plane. The OAZO film with $d_{ZnO(0002)}$ of 2.593 Å is compressive out of plane and in tension in-plane. The compressive in-plane strain in VAZO film could be in

part due to deficiency of the oxygen atom in the lattice. The tensile in-plane strain in the OAZO film could be interpreted to accommodation of the oxygen atom in the lattice.

The XRD pattern of the OAZO/VAZO multilayer film is very similar to that of AZO single layer film except that the ZnO(0002) peak splits into two distinguishable peaks. This two peaks confirms the OAZO/VAZO grow as multilayer structure with different d-spacing values. These two d-spacing values are calculated to be 2.590 Å for OAZO layer and 2.626 Å for VAZO layer respectively. The first peak at $2\theta = 34.\ 11°$ is close to that of VAZO layer deposited in vacuum. The second peak at $2\theta = 34.\ 60°$ is close to that of OAZO layer deposited in oxygen. The VAZO/OAZO multilayer has only one peak at $2\theta = 34.20°$ with a calculated d-spacing value of 2.620 Å. The d-spacing of the VAZO/OAZO multilayer is slightly higher than that of the VAZO single layer. The assumption is that the d-spacing difference in VAZO films deposited on amorphous glass and on polycrystalline OAZO layer results in different strains that affect the electrical and optical properties of the VAZO film.

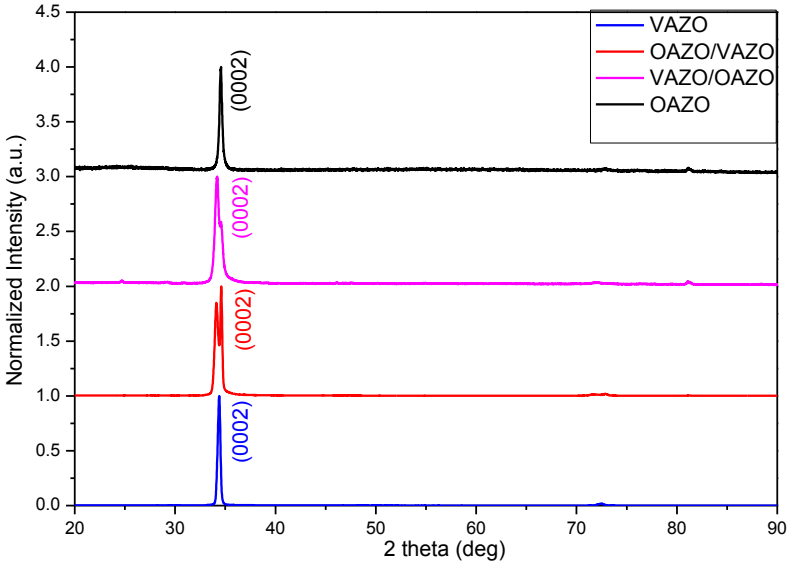

Fig. 21. XRD pattern of the VAZO single layer, the OAZO single layer, the OAZO/VAZO multilayer, and the VAZO/OAZO multilayer.

In order to fully understand the microstructures of AZO films with different optical and electrical properties, a detailed cross-sectional TEM study was conducted for the VAZO and the OAZO/VAZO multilayer. Fig. 22 shows the cross-sectional TEM image of the VAZO single layer with a Silicon cap layer deposited by PLD. The VAZO film grows as continuous layer with uniform thickness and smooth surface. The surface roughness of the VAZO film is estimated to be less than 5 nm as shown in Fig. 23. The low surface roughness of the VAZO film is typically favored for making conventional TCOs because of less recombination centers and pinholes.

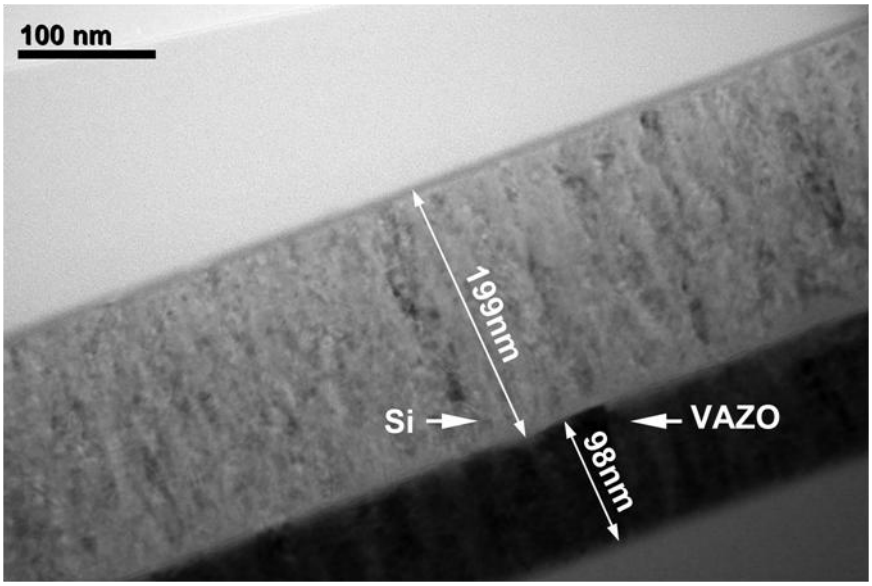

Fig. 22. Cross-sectional TEM image of the VAZO single layer with Si cap layer.

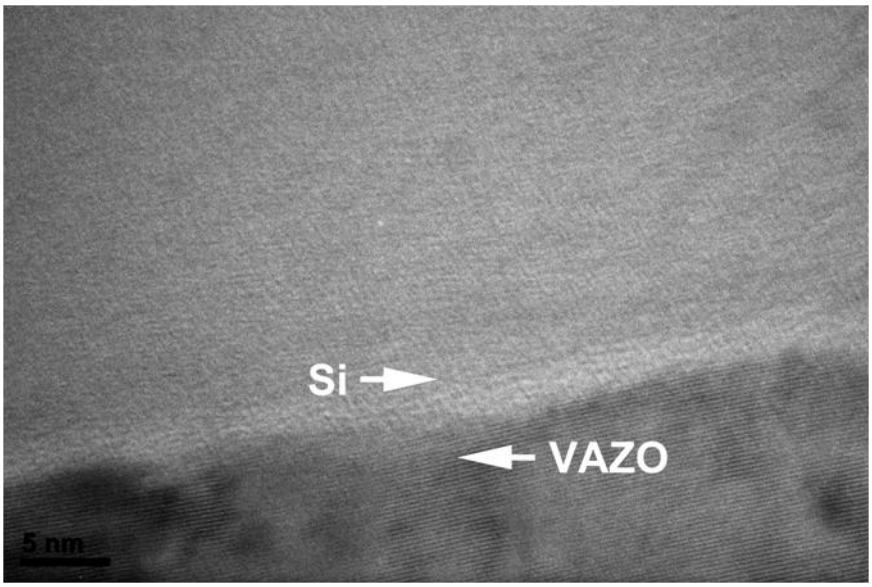

Fig. 23. Cross-sectional TEM image of the Si/VAZO interface.

Fig. 24 shows the cross-sectional TEM image of the OAZO/VAZO multilayer. The OAZO/VAZO multilayer film has a rough OAZO film deposited on top of the smooth VAZO film. The surface roughness of the OAZO cap layer is estimated to be ~10 nm to 20 nm. The surface roughness of OAZO/VAZO multilayer supports the transmittance reduction in OAZO single layer shown in previous optical data. Fig. 25 shows the TEM image of the OAZO cap layer. It is observed that the OAZO grain grows as nanorods with an average diameter of ~20 nm. The surface of nanorods develops a pyramid-like surface texture which resembles the "inverted pyramid" surface texture achieved in previous light trapping scheme [21]. The TEM image of OAZO layer confirms that the formation of the desired surface roughness for the light trapping scheme proposed in this research.

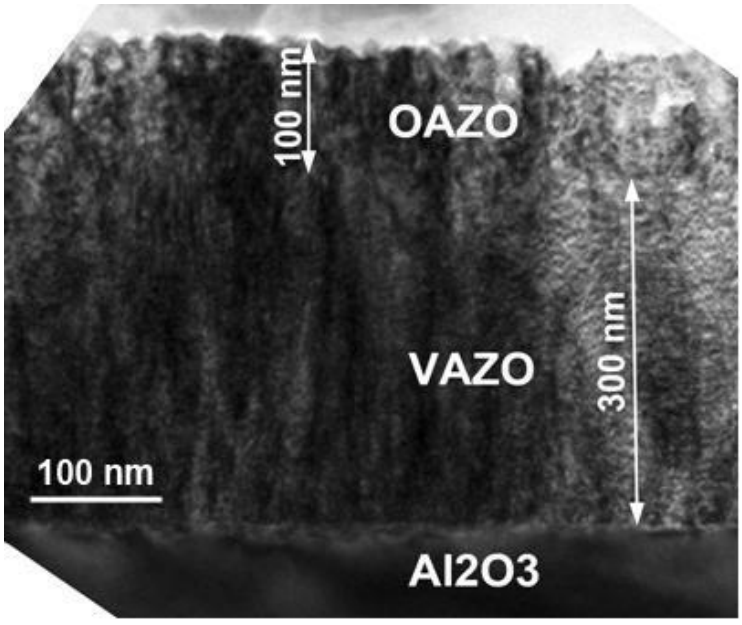

Fig. 24. Cross-sectional TEM image of the OAZO/VAZO multilayer film.

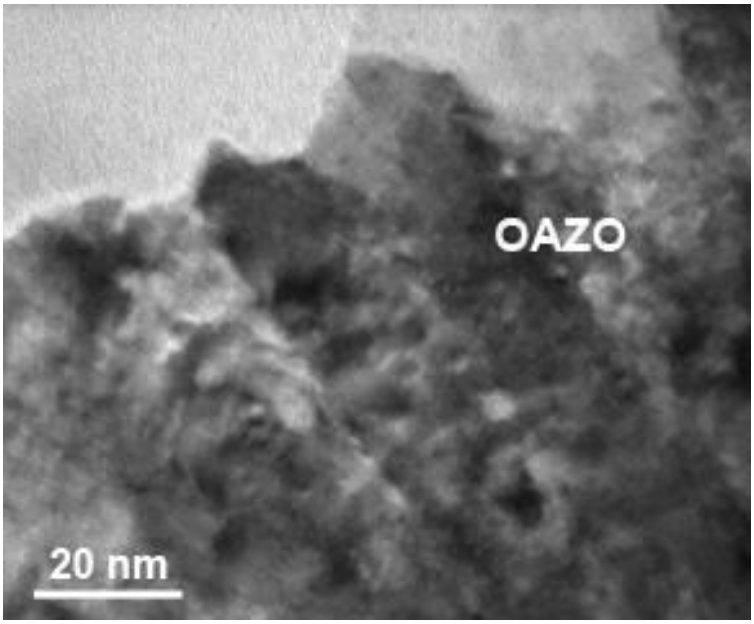

Fig. 25. Cross-sectional TEM image of the OAZO cap layer.

2.5 Summary of LT-TCO Layer

VAZO single layer films have been demonstrated by PLD deposition of AZO at 300 °C in vacuum. The VAZO films have smooth surface, good transmission, good conductivity that can be applied as transparent electrodes for solar cells. The VAZO film is stable and compatible to fabrication processes at temperature less than 500 °C without significant degradation of conductivity. OAZO single layer films have been achieved by PLD deposition of AZO at 300 °C in oxygen of 0.2 Torr. The OAZO films grow as nanorods with rough surface texture confirmed by TEM study. The surface texture and transmittance reduction corroborates the presence of light trapping function.

The OAZO/VAZO multilayer films have been fabricated by sequential PLD deposition of the OAZO layer on the VAZO layer with control of oxygen pressure. The

OAZO/VAZO multilayer film has transmittance reduction which indicates its potential as a LT-TCO layer. When integrating the OAZO/VAZO multilayer as the transparent electrode in thin film solar cells, the rough surface of OAZO layer is expected to provide enhanced light reflection and light scattering to increase the effective optical path of the film. The low resistivity of the VAZO layer ensures efficient carrier transport for solar cells. The VAZO/OAZO multilayer films have been produced by sequential PLD deposition of the VAZO layer on the OAZO layer. The VAZO/OAZO multilayer films show improved transmittance and excellent conductivity. The VAZO/OAZO multilayer would serve as high quality and cost efficient TCO for flat panel displays and solar cell applications.

3. THIN FILM CADMIUM TELLURIDE SOLAR CELLS

3.1 Introduction to Thin Film CdTe Solar Cells

Thin film solar technologies promise to reduce the manufacturing cost of solar modules in part due to conservative material and simpler series connection of cells than conventional silicon solar technologies [33]. There exist various thin film solar technologies that typical uses amorphous Si, CdTe and CIGS as the absorber material [13]. In this work, thin film solar cells for integrating the LT-TCO layer is based on CdTe/CdS heterojunction. CdTe and CdS makes efficient heterojunction owning to similar II-VI group structure, small electron affinity difference, and small TEC mismatch [33]. CdS, with a wide band gap of 2.4 eV, tends to grow as n-type under usual film deposition techniques [33]. CdTe have been chosen over Si and CIGS to make the absorber layer based on several considerations. First, the energy gap of CdTe has the best match with solar spectrum [33]. Second, the absorption spectrum of CdTe (below 800 nm) matches with the spectrum of AZO based LT-TCO layer which shows transmittance reduction and potential light trapping effect. Third, the direct band gap and high absorption coefficient of CdTe facilitate efficient laser deposition of CdTe layer [33]. Fourth, CdTe, as II-VI compound with strong tendency to grow as stoichiometric, allows easier control of composition in target and in thin films than CIS.

The superstrate configuration as shown in Fig. 26 is conventional for the thin film CdTe/CdS solar cells fabricated on rigid glass substrate. In the preferred arrangement, ITO coated glass was used as the substrate. The CdTe/CdS heterojunction

is formed by sequential deposition of a thinner CdS n-type window layer followed by the deposition of a thicker CdTe p-type absorber layer. Finally Au layer, as back contact electrode, is deposited onto the CdTe to complete the solar cell device. The thickness of CdS layer was fixed at around 0.25 μm (250 nm) for reliability. The thickness of the CdTe layer was fixed at around 1 μm (1000 nm) to obtain ~10% light penetration for examination of the LT-TCO layer. The deposition of p-n junction was done by PLD at 250 °C and $CdCl_2$ treatment was used to activate the p-n junction for efficiency enhancements. Various post-deposition treatments were conducted on the CdTe layer and the CdS layer respectively to improve cell performance.

Fig. 26. The superstrate configuration of a thin film CdTe solar cell.

During the operation of the solar cell, light enters the cell through the glass substrate and transverse the ITO layer and CdS layers. The ITO layer and the CdS layer are not active in the photovoltaic process and have some-unwanted absorption. Most of electron-hole pairs are generated close to the CdTe/CdS junction within the CdTe absorber layer. The electrons are driven by the built-in field through the interface into the n-CdS film. The holes remain in the CdTe and join the holes within the space charge

region promoting the p-type conduction of CdTe and finally have to leave the cell via the Au electrode. The ITO electrode and the Au electrode serve to extract electric current from the solar cell to external circuit.

3.2 Material Properties

3.2.1 CdTe

CdTe is an ideal semiconductor material for making absorber layer because its energy band gap of 1.45 eV ideally matches with the solar spectrum [13]. CdTe has a very high absorption coefficient of 10^5 cm^{-1} in the visible wavelength from 400 nm to 700 nm. Theoretically, 90% of the incident light can be absorbed within 1 μm of CdTe and 99% of the light can be absorbed within 2 μm of CdTe [33]. CdTe has a cubic crystal structure as shown in Fig. 27 and lattice constant a = 6.481 Å [36-38]. The deviation of stoichiometry has been reported to change the lattice parameter of CdTe giving values of 6.480 and 6.488 for crystals grown at high temperatures from Cd-rich and Te-rich melts [38]. The Temperature-composition (T-x) diagram of CdTe is shown in Fig. 28 [39]. CdTe has a melting point at 1365 K and thermal expansion coefficient (TEC) of 5.9×10^{-6}/K at 293 K [40]. In the conditions of high temperature and vacuum, CdTe is decomposed to Cd atoms and Te atoms which have a vapor pressure ratio of 2 to 1 [13]. At high temperature, CdTe would tend to become Cd deficient so that p-type CdTe is readily formed at high temperature. CdTe has been reported to have electron mobility of ~300 cm^2/V-sec and hole mobility of ~30 cm^2/V-sec [41]. Doping in CdTe is difficult because of self-compensation effect, vapor pressure difference between Cd and

Te, and low solubility of impurity atoms in CdTe [13]. Typically the doping level for CdTe is within the range from 10^{14} to 10^{15} cm^{-3} [13]. The activation energy for n-type impurities has been reported to be much smaller than the activation energy for p-type impurities in doping CdTe [41].

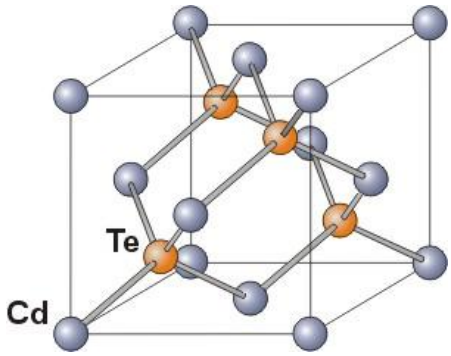

Fig. 27. Atomic structure of CdTe [36].

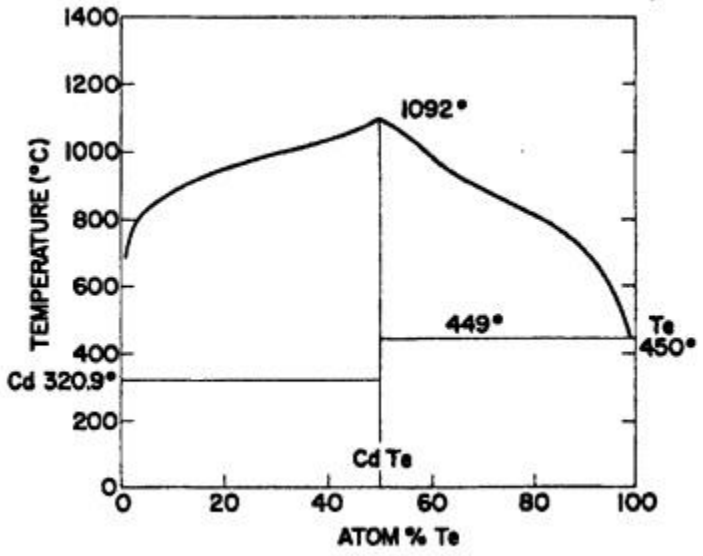

Fig. 28. T-x project of the II-VI binary system Cd-Te [39].

3.2.2 CdS

Cadmium Sulfide (CdS) is an important semiconductor material for making window layer because of its direct wide band gap of 2.4 eV and tendency to grow as n-type by most fabrication techniques. CdS has a very high absorption coefficient within the value from 10^4 to 10^5 cm^{-1} in the visible wavelength [13]. The CdS occurs in nature with two different crystal structures: hexagonal and cubic. The energy gap for thin film CdS has been reported to be 2.56 eV for hexagonal phase and 2.51 eV for cubic phase [42]. Fig. 29 shows the atomic structure of these two different phases for CdS [43]. The hexagonal CdS has a lattice constant of a = 4.1367 Å and c = 6.7161 Å, whereas cubic CdS has a lattice constant of 5.825 Å [44]. The melting point for both phases of CdS is 1748 K [45]. The structural phase transition of CdS from cubic phase to hexagonal phase was found to occur at 300 °C [46]. Electron mobility is reported to be 390 cm^2/V-sec for hexagonal CdS and 70 - 85 cm^2/V-sec for cubic CdS [47-48]. Since the electron affinity is reported to be 4.5 eV for hexagonal CdS and 4.28 eV for CdTe [49], the CdS readily forms low barrier junction with CdTe. The TEC of 3.6 x 10^{-6}/K for CdS also matches well with that of 5.9 x 10^{-6} /K for CdTe [13].

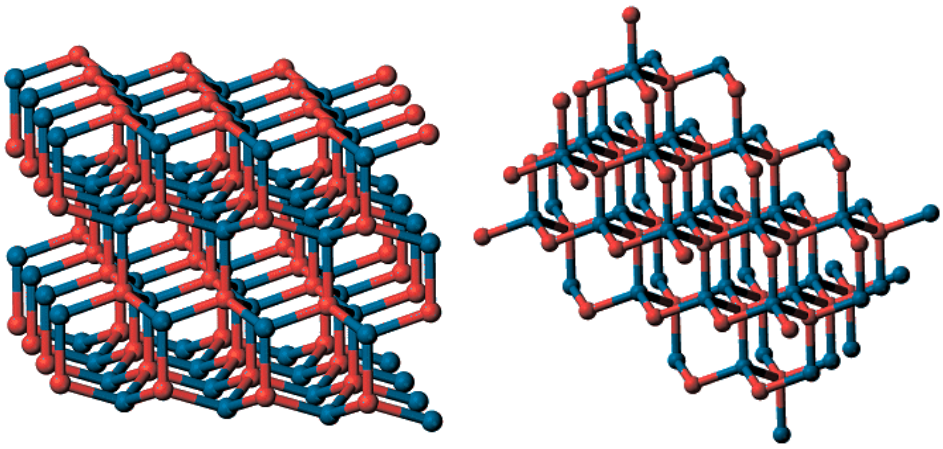

Fig. 29. Atomic structure of the hexagonal CdS (left) and the cubic CdS (right) [43].

3.3 Fabrication and Characterizations of Thin Films

3.3.1 CdTe Thin Film Deposition

CdTe thin films were deposited on glass substrate by PLD technique with a KrF excimer Laser (Lambda Physik Compex Pro 205, λ = 248 nm). The laser beam was focused on the target to obtain laser energy density of 2 J /cm^2 at an incidence angle of 45°. The CdTe target was prepared by pressing the CdTe powder of 99.999% purity into a circular disk of 1 inch diameter. An optimized substrate temperature at250 °C and back pressure of argon of 0.03 Torr were maintained during the deposition. Typical deposition rate was 1.15 Å/pulse with a repetition rate of 10 Hz. The CdTe films typically have thickness of 700 nm resulted from 6000 laser pulses of deposition.

3.3.2 CdS Thin Film Deposition

CdS thin films were deposited on glass substrate with the laser energy density of 2J/cm^2 and back pressure of 0.03 Torr of argon at substrate temperature of 250 °C. The CdS targets were prepared from the CdS powder of 99.999% purity by the same method used to prepare the CdTe target. Typical deposition rate was 0.55 Å/pulse for a repetition rate of 10 Hz. The CdS thin films typically have thickness of 250 nm resulted from 4500 pulses of deposition.

3.3.3 Optical Properties

Optical transmittance measurements were conducted on CdTe films and CdS films. Fig. 30 shows the plot of optical transmittance spectra (%) versus wavelength for the CdTe films and the CdS films. The absorption edge of the CdTe films is observed to be ~800 nm (E_g = 1.55 eV). The energy band gap of CdTe films agrees well with that of bulk CdTe (1.45 eV). The absorption edge of CdS film is observed to be ~500 nm (E_g = 2.48 eV) which matches with that of bulk CdS (E_g = 2.42 eV). The absorption edge of the CdS films at 500 nm is consistent with that of hexagonal phase CdS (500 nm for hexagonal CdS and 515 nm for cubic CdS) [42]. The optical transmittance data confirms that the above PLD receipt has resulted in cubic phase CdTe thin films and hexagonal phase CdS thin films.

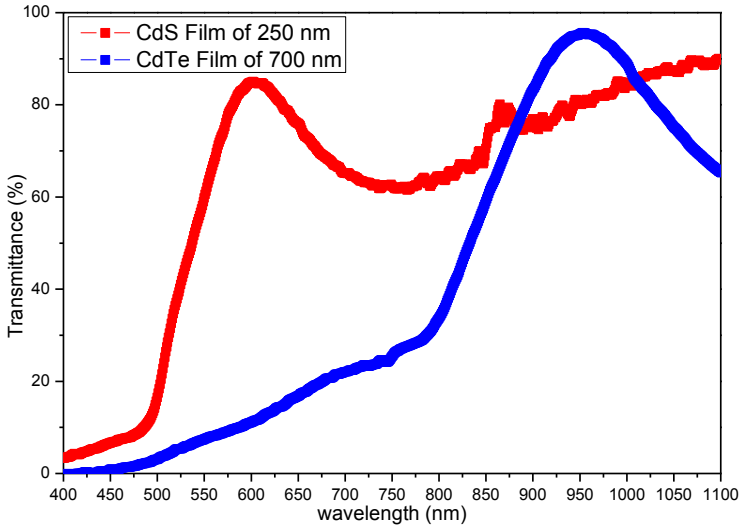

Fig. 30. Optical transmittance spectra of the CdTe film and the CdS film.

3.3.4 Electrical Properties

Electrical resistivity of thin films was measured by a four-point probe system at room temperature. The sheet resistance of CdTe thin film was not measurable by the four-point probe with a maximum measurement range of $10^5\Omega$/sq. The thickness of the CdTe films was ~500 nm measured by a profilometer. The resistivity of CdTe was thus estimated to be higher than 5000 Ω-cm. The high resistivity of the CdTe films suggests that CdTe film grows as stoichiometric using the above PLD receipts. For the CdS thin film, the measured resistivity of 250 nm CdS film was ~0.47 Ω-cm which is sufficient for making the as-deposited CdS layer a suitable window layer.

3.3.5 Microstructure Properties

The crystallographic structure of the thin films and the targets was characterized by XRD technique. XRD θ-2θ scans of the CdTe thin films and the CdTe target is plotted in Fig. 31. The XRD pattern of the CdTe target shows multiple peaks and matches well with that of bulk CdTe. The XRD pattern of the CdTe thin film shows single CdTe(111) peak, which suggests CdTe film grows preferentially along the (111) direction. The peak position of CdTe(111) is found to be 23.76° with a calculated d-spacing of 3.742 Å. The d-spacing of CdTe(111) peak exactly matches the d-spacing value of CdTe(111) peak for bulk CdTe. The dominance of the CdTe(111) peak in the crystallographic structure of the CdTe film is consistent with that of CdTe prepared by PVD technique at low temperature [33].

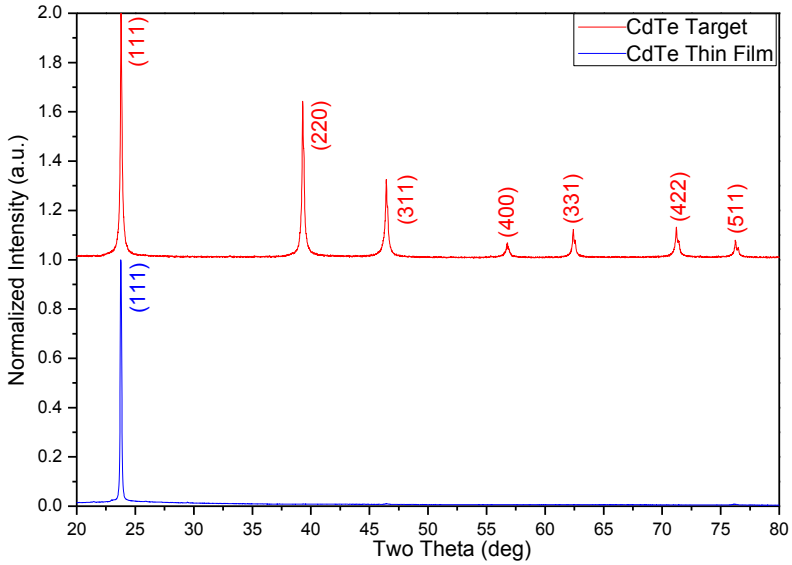

Fig. 31. XRD pattern of the CdTe target and the CdTe thin film.

XRD θ-2θ scan of the CdS thin films and CdS target is plotted in Fig. 32. The XRD pattern of the CdS target agrees exactly with that of bulk CdS. The single CdS(002) peak observed in the XRD pattern of the CdS films suggests CdS film grows as highly textured along (002) direction. The peak position of CdS(002) is found to be 26.76° with a calculated d-spacing of 3.328 Å. The d-spacing value of the CdS thin film is close to 3.341 Å for hexagonal CdS(002) peak. The XRD pattern and the transmittance data corroborate the formation of hexagonal phase CdS thin film.

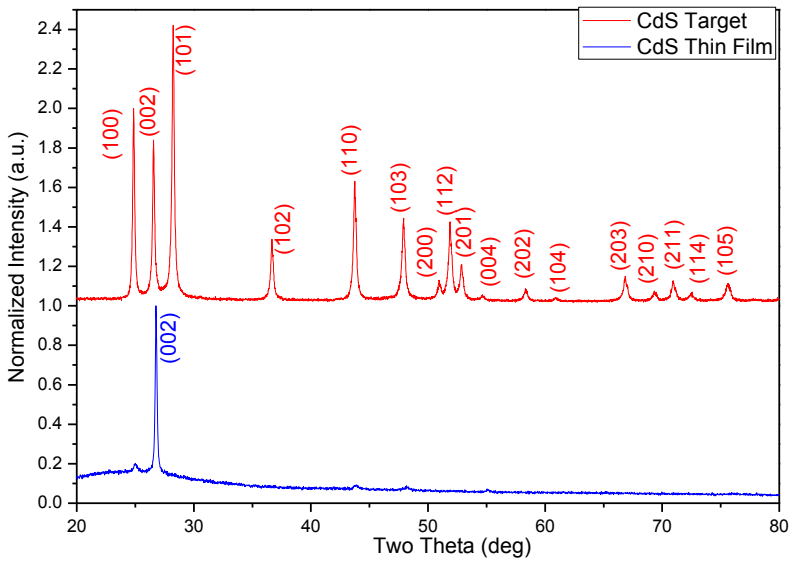

Fig. 32. XRD pattern of the CdS target and the CdS thin film.

3.4 Fabrication of Thin Film CdTe Solar Cells

3.4.1 Solar Cell Device

Fig. 33 shows device structure of the thin film CdTe solar cells. The ITO/Glass has an ITO coating of 0.2 µm and serves as the substrate for CdS deposition. The CdS window layer of 0.25 µm was deposited by PLD deposition. The CdTe absorber layer of 1 µm was deposited by PLD deposition. The Au layer of 0.1 to 0.2 µm was deposited by dc sputter to complete the solar cell. Fig. 34 shows a fabrication flow chart for making the solar cell device. The flow chart shows the fabrication of solar cell device from the substrate to a finished solar cell in multiple steps. Post-deposition treatments were applied on the CdS window layer and the CdTe absorber layer. The fabrication and measurement procedures of solar cells are described later in detail. The results and discussion about the effects of post-deposition treatments on cell performance are provided.

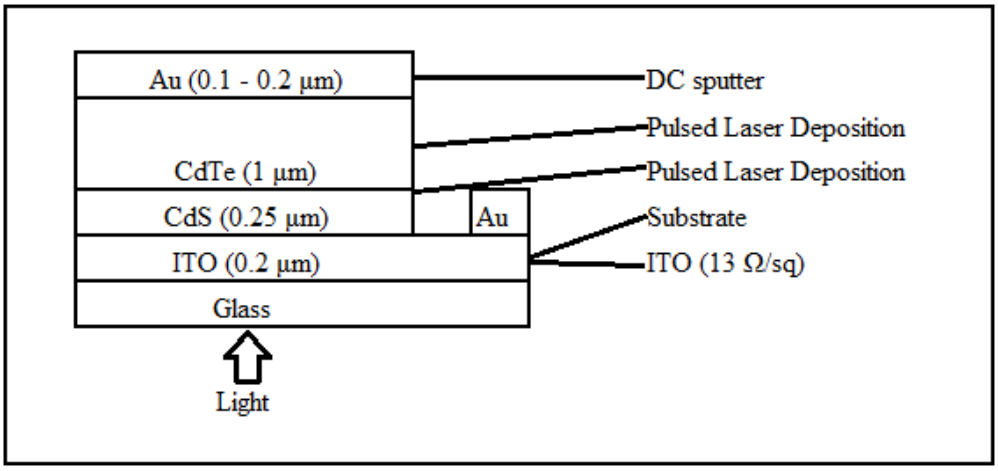

Fig. 33. Device structure of the thin film CdTe solar cells.

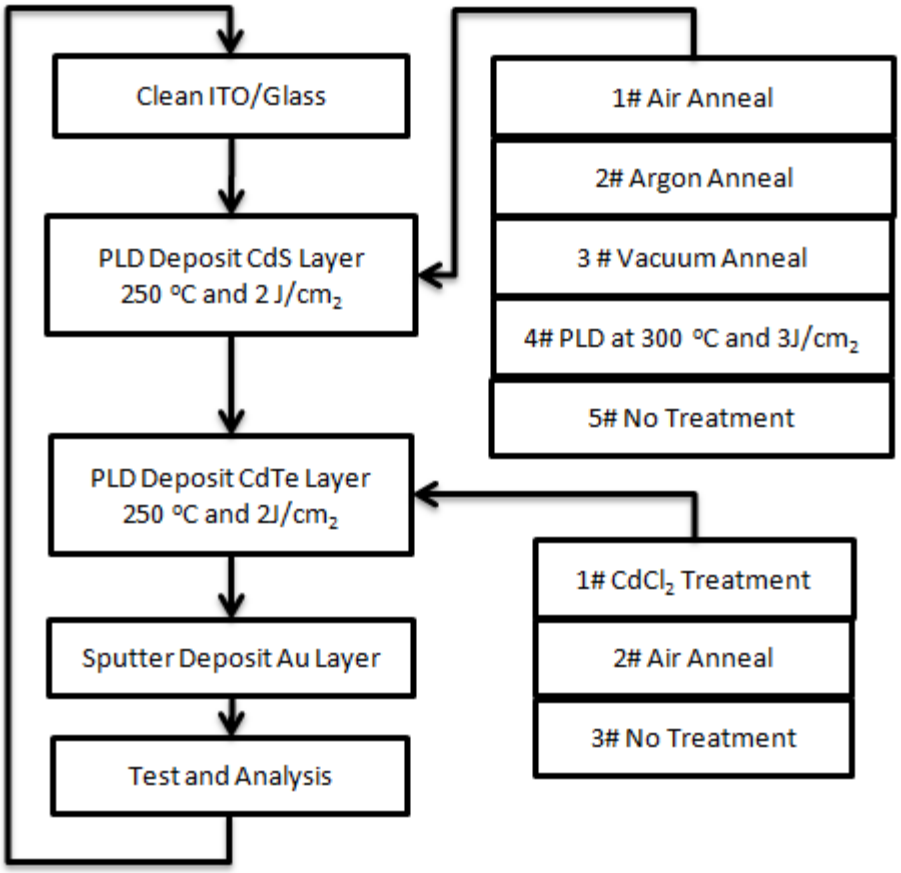

Fig. 34. Fabrication flow chart for the thin film CdTe solar cells.

3.4.2 ITO Substrate Preparation

The substrate used was 76 x 76 x 0.7 mm Indium-Tin-Oxide (ITO) coated glass plates from MTI Corporation. The ITO thin film has a sheet resistance of 13 Ω/sq and resistivity of 1.3 x 10^{-4} Ω-cm. The substrate was first cut into 10 x 10 x 0.7 mm pieces with a diamond pen. The substrate of area of ~1 cm^2 was cleaned sequentially in acetone and in methanol each for 10 minutes and blew dry before attaching to the substrate holder. Silver conductive paint was applied to ensure good attachment and heat

conduction between the substrate and the holder. After loading the substrate into the PLD system, the chamber was first pumped down to vacuum by a mechanical pump. The substrate was heated at 150 °C in vacuum to evaporate out residual solvents of silver paint and cooled down to room temperature. The PLD system was then pumped down to high vacuum by a turbo molecular pump.

3.4.3 CdS Window Layer

The base pressure of PLD deposition was 2 to 3 x 10^{-6} Torr. The back pressure of argon of 0.03 Torr was maintained during the deposition. The substrate temperature was fixed at 250 °C. The CdS layer was deposited on ITO substrates with a KrF excimer laser operated at a repetition rate of 10 Hz and with laser energy density of 2 J/cm^2. The total deposition time was around 450 seconds equivalent to 4500 laser pulses to obtain a CdS layer of 250 nm. Fig. 35 shows the as-deposited CdS film colored in orange on the ITO substrate.

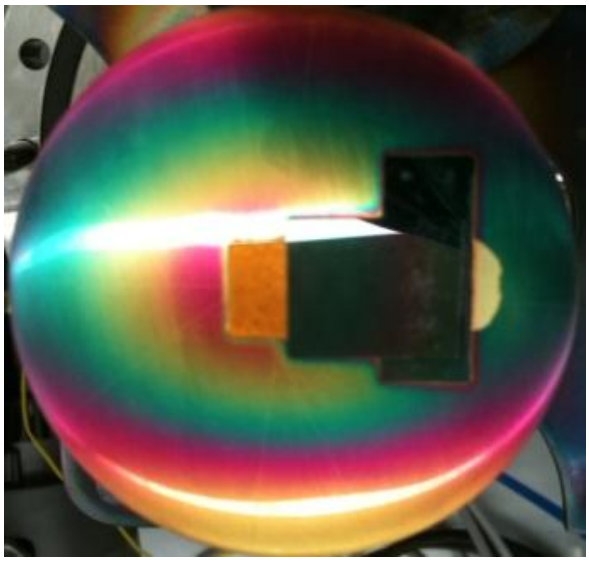

Fig. 35. Appearance of the as-deposited CdS layer.

After the CdS deposition, the CdS/ITO sample was deposited with CdTe layer or further processed with four different treatments prior to CdTe deposition. These four treatments include air annealing, argon annealing, vacuum annealing, and $CdCl_2$ treatment. For the air annealing, the CdS/ITO substrate was heated at 400 °C for 10 min in air. For the argon annealing, the CdS/ITO substrate was heated at 400 °C for 10 min in argon of 0.03 Torr. For the vacuum annealing, the CdS/ITO substrate was heated at 400 °C for 10 min in vacuum. For the $CdCl_2$ treatment, the CdS/ITO substrate was first coated with $CdCl_2$ and then heated at 400 °C for 10 min in air. Deposition of CdS with laser energy density of 3 J/cm^2 and substrate temperature of 300°C has been referred to as the optimized PLD conditions and used to prepare some CdS/ITO samples.

3.4.5 CdTe Absorber Layer

CdTe thin film was deposited on CdS/ITO substrates with a KrF excimer laser operated at a repetition rate of 10 Hz and with a laser energy density of 2 J/cm^2. The total deposition time was around 800 seconds equivalent to 8000 laser pulses to obtain a CdTe layer of around 1 μm. Fig. 36 shows the as-deposited CdTe film colored in black on the CdS/ITO substrate.

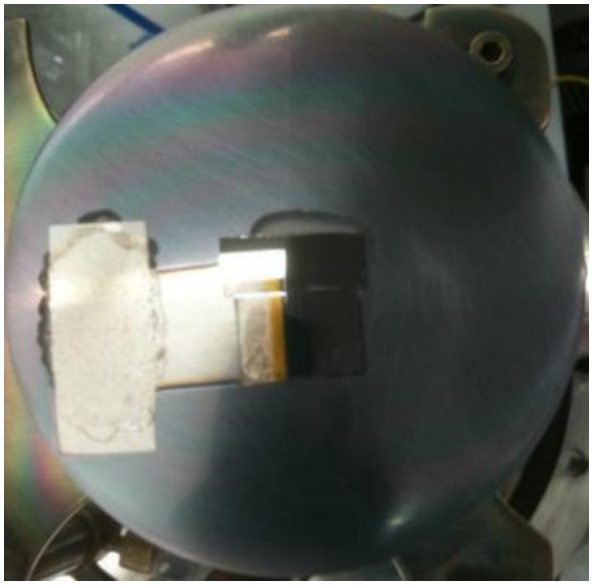

Fig. 36. Appearance of the as-deposited CdTe layer.

After the CdTe layer deposition, the CdTe/CdS/ITO samples were either directly deposited with Au contacts or further processed with two post-deposition treatments. These two treatments were air annealing and $CdCl_2$ treatment. For the air annealing, the

CdTe/CdS/ITO sample was heated at 390 °C for 10 min in air. For the $CdCl_2$ treatment, the CdTe/CdS/ITO sample was first coated with a thin layer of $CdCl_2$ and then heated at 390 °C for 10 min in air. The $CdCl_2$ treatment has been reported to eliminate the fast-recombination centers in the CdTe film, reduce recombination centers in the junction, and eliminate small grains in the grain boundaries [50]. The $CdCl_2$ treatment performed in this research was modified from the methods reported by D. H. Rose *et al*. [50]. In the modified $CdCl_2$ treatment, the CdTe solar cells were soaked in a saturated $CdCl_2$: methanol solution (0.11 g in 10 mL methanol). The soak lasted for 5 minutes in a covered beaker on a hot plate heated to near the boiling point of methanol (55-60 °C). After that soak, the samples were taken out of the solution and left dry to evaporate excess methanol. The samples were loaded into a tube furnace. The furnace was heated to 390 °C and left for 10 min in air. After cooling to below 50 °C, the samples were rinsed in DI water to remove excess $CdCl_2$ and blew dry before metallization.

3.4.6 Au Layer

The Au layer was deposited by DC sputter at room temperature. Prior to sputter, Kapton tape (3M 5413 polymide film) was used to mask the edge of the CdTe/CdS/ITO sample and the region between the ITO substrate and CdTe layer. This mask step is to ensure deposition of Au electrodes just on the defined areas on the ITO surface and CdTe surface. The sample was loaded into a DC magnetron sputtering system (Kurt J. Lesker TORUS 2 inch) which was then pumped down to 3×10^{-6} Torr. The back pressure of argon of 5.5×10^{-3} Torr was maintained during the sputtering. The Au layer

was sputtered with power density of 7.4 W/cm^2 and target-to-substrate distance of 5.5 cm. Deposition rate was 20 Å/sec and the total deposition time was ~50 seconds to obtain 100 nm Au layer. After the deposition of Au layer, the CdTe/CdS/ITO samples became complete thin film CdTe solar cells ready for measurements. Fig. 37 shows the appearance of a finished solar cell.

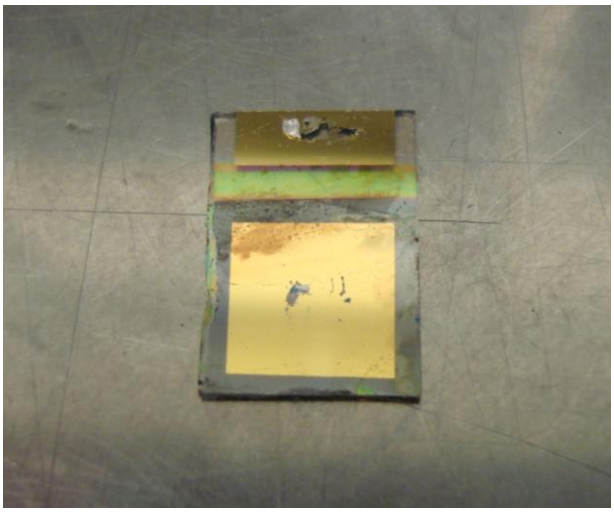

Fig. 37. Appearance of the complete thin film CdTe solar cell.

3.4.7 Solar Cell Measurements

The thin film CdTe solar cells were measured using a homemade solar cell measurement system as shown in Fig. 38. The solar cell measurement system consists of a solar simulator from Newport, a magnetic based probe station with four micromanipulators, a test station with cooling function, and a SourceMeter (2440) from Keithley. The output power density P_{in} of the solar simulator was calibrated by a

reference monocrystalline silicon solar cell with a meter equipped with thermocouple. The P_{in} was measured to be ~95 mW/cm^2 under the Global AM 1.5 illumination at ~25 °C and is used for calculation of solar cell efficiency.

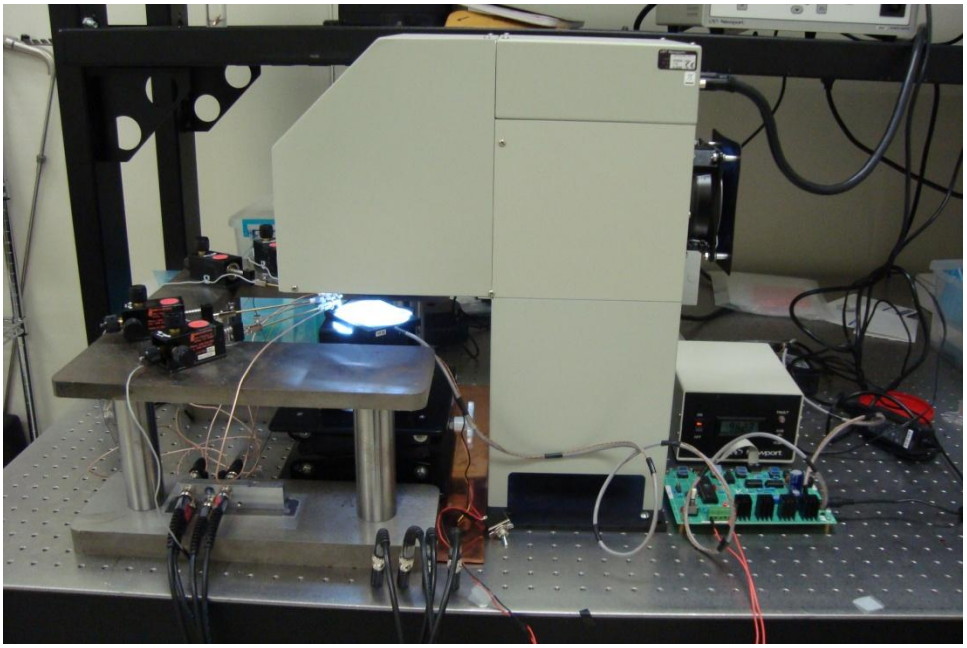

Fig. 38. Appearance of the solar cell measurement system.

Prior to solar cell measurement, a test plate was made by sputtering Au on a masked glass slide to form two Au electrodes. Copper wires were used to connect the solar cell and the Au electrodes using indium solder as shown in Fig. 39. The test plate with the solar cell was situated in the work plane of the solar simulator and on the test station. The test station was made with a heat sink and air cooled by a fan. During the measurement, the temperature of the solar cell was maintained at 25 to 30 °C.

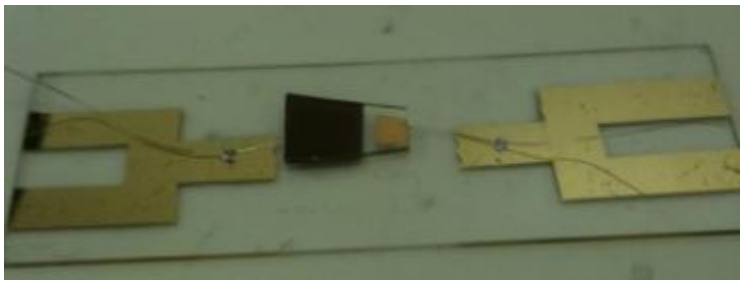

Fig. 39. Appearance of a solar cell soldered to the test plate.

To extract the current readings and the voltage readings from the solar cell under illumination, electrical connections between the solar cell and the SourceMeter were made. The cables completed the electrical connections by connecting the probe tips of the micromanipulator to the SourceMeter. The probe tips made contacts with the Au electrodes of the test plate so that the current flows from the solar cell into the SourceMeter. Voltage was applied to the solar cell and current was measured by the SourceMeter for plotting the I-V characteristic. Solar cell measurement typical generates the light I-V characteristic and the dark I-V characteristic. The light I-V characteristic can be used to extract the V_{oc}, J_{sc}, FF, and efficiency of the solar cell [13]. The dark I-V characteristic can be used to extract the shunt resistance R_{sh}, the diode factor, the energy and concentration of the dominant recombination center, the lifetime of charge carriers [13].

3.5 Results and Discussion

3.5.1 Summary of Solar Cell Performance

Thin film CdTe solar cells have been fabricated by PLD and processed with different CdS treatments and CdTe treatments. The CdTe treatments include air annealing and the $CdCl_2$ treatment. The CdS treatments include air annealing, argon annealing, vacuum annealing, and the $CdCl_2$ treatment. CdS layer in some cells was deposited with the optimized PLD condition. Representative solar cells are grouped into four categories for analysis of the effect of the above fabrication processes on cell performance as shown in Fig. 40. These solar cells were measured to obtain their light J-V characteristics and dark J-V characteristics. The performance parameters and processes of representative solar cells are summarized in Table 2.

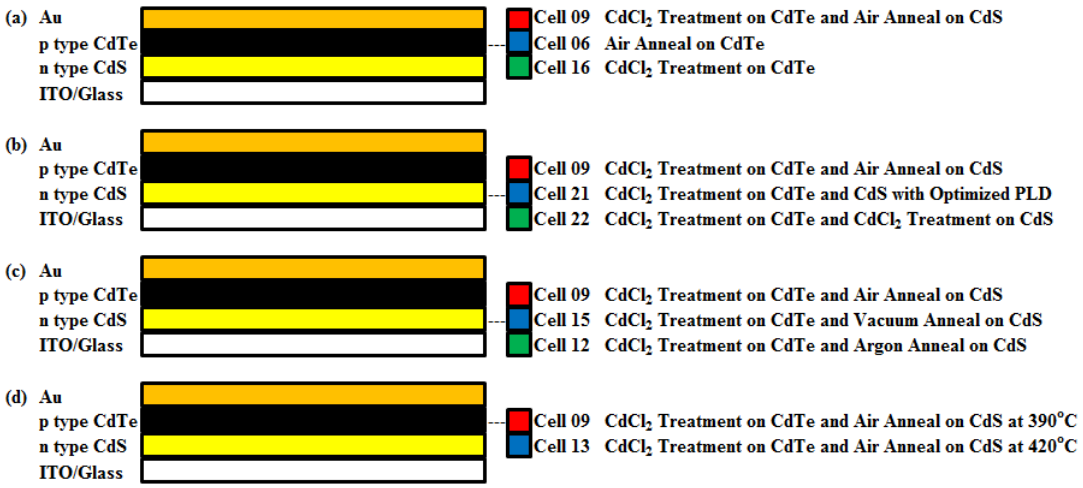

Fig. 40. Grouping of solar cells for analysis of (a) effect of CdTe treatments; (b) effect of CdS treatments; (c) effect of oxygen; (d) effect of annealing temperature.

Table 2 A list of performance parameters and treatments of representative CdTe solar cells.

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	η	CdS Treatments	CdTe Treatments
TL09	390	6.4	0.44	1.2%	Air Annealing	$CdCl_2$ Treatment
TL13	460	5.8	0.26	0.7%	Air Annealing	$CdCl_2$ Treatment
TL20	46	4	0.25	0.05%	Air Annealing	$CdCl_2$ Treatment
TL22	120	5.78	0.25	0.18%	$CdCl_2$ Treatment	$CdCl_2$ Treatment
TL06	320	2.5	0.25	0.2%	/	Air Annealing
TL08	200	0.38	0.25	0.02%	/	/
TL16	112	0.31	0.25	0.009%	/	$CdCl_2$ Treatment
TL12	5	0.62	0.25	0.0008%	Argon Annealing	$CdCl_2$ Treatment
TL21	2.5	0.6	0.25	0.0004%	Optimized PLD condition	$CdCl_2$ Treatment
TL15	0.24	0.31	0.25	0.00002%	Vacuum Annealing	$CdCl_2$ Treatment

3.5.2 Effect of CdTe Treatments

Solar cell TL08, without treatments, has V_{oc} of 200 mV, J_{sc} of 0.38 mA/cm^2, FF of 0.25. The low performance of the as-deposited cell indicates the as-deposited cell has low built-in electric field and inefficient carrier transport correlated with low FF, high R_s and low R_{sh}. Fig. 41 shows three cells with different CdTe treatments for improving R_s and R_{sh} of the CdTe layer. Fig. 42 compares the light J-V characteristics of these three

cells. For cell TL09, CdS layer received air annealing and CdTe layer received $CdCl_2$ treatment. The cell TL 09 has V_{oc} of 390 mV, J_{sc} of 6.4 mA/cm^2, and FF of 0.44. For cell TL16, CdS layer was left as-deposited and CdTe layer received $CdCl_2$ treatment. The cell TL16 has V_{oc} of 112 mV, J_{sc} of 0.3 mA/cm^2, FF of 0.25. For cell TL06, CdS layer was left as-deposited and CdTe layer received air anneal. The cell TL06 has V_{oc} of 320 mV, J_{sc} of 2.5 mA/cm^2, and FF of 0.25.

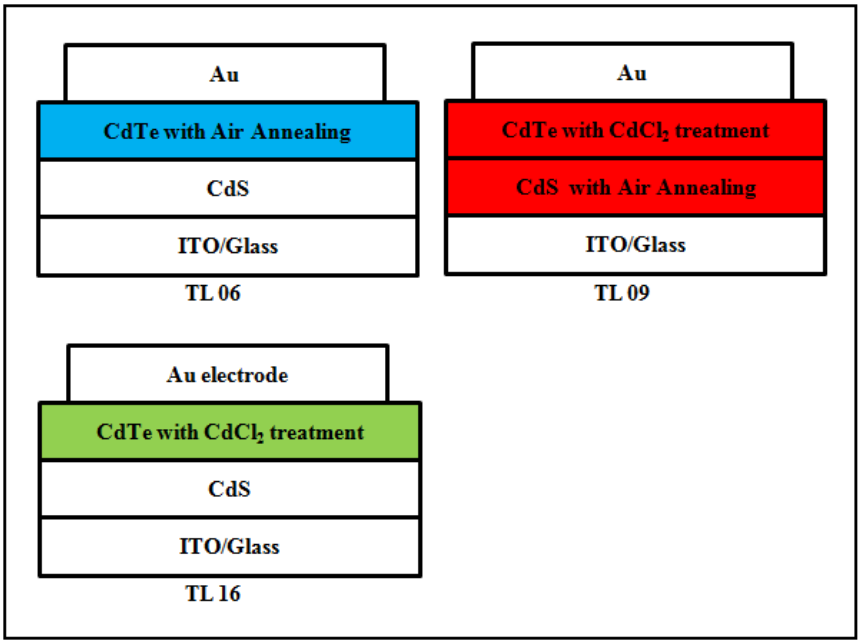

Fig. 41. Structures of the solar cells TL09, TL16, and TL06.

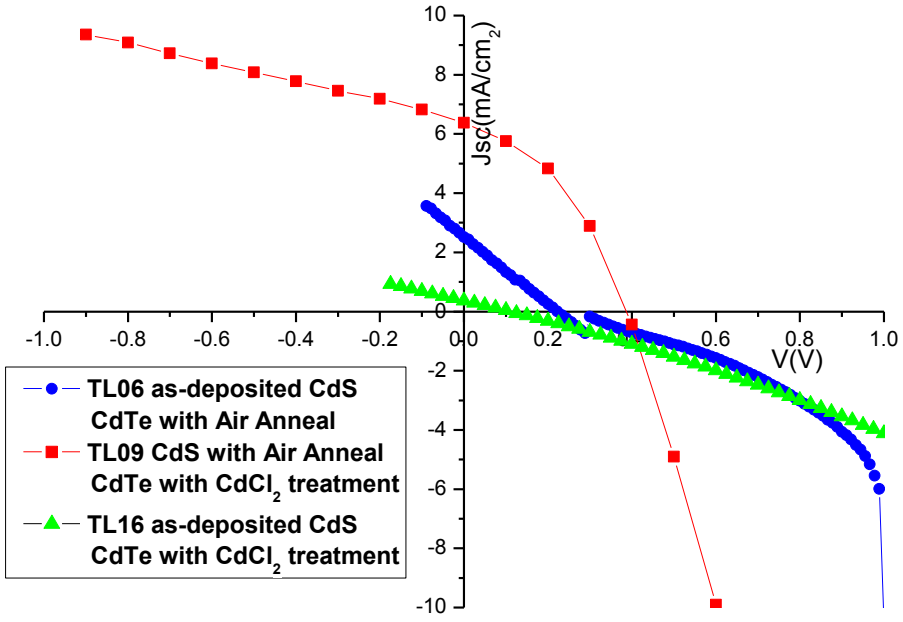

Fig. 42. Light J-V characteristics of the solar cells TL06, TL09, and TL16.

The comparison between the performance parameters of the cell TL16 and that of the cell TL08 shows that $CdCl_2$ treatment reduces the V_{oc} from 200 mV to 112 mV without changing J_{sc} and FF. The lowered V_{oc} suggests the degradation of built-in electric field in the p-n junction caused by $CdCl_2$ treatment. The $CdCl_2$ treatment, however, does not further reduce the J_{sc} which indicates minimal change in carrier generation and carrier transport in the CdTe layer. The degradation of V_{oc} is opposed to overall enhancement in V_{oc}, J_{sc} and FF typical in CdTe solar cells processed by the $CdCl_2$ treatment in previous reports [33]. It has been reported that solar cells fabricated by PLD necessitate $CdCl_2$ treatment to achieve good performance [51]. The assumption

is that the $CdCl_2$ treatment results in degradation mainly in the CdTe/CdS interface due to interdiffusion between CdTe and CdS.

Air annealing of the CdTe layer for the cell TL06 increases the V_{oc} from 200 mV to 320 mV and improves J_{sc} from 0.38 mA/cm^2 to 2.5 mA/cm^2. However, air annealing does not improve the FF. The increased V_{oc}, however without improvements in FF, suggest there is unlikely change in the junction quality. The increased J_{sc} suggests that air annealing may enhance the p-type conductivity of CdTe layer resulting in lower R_s. Air annealing is considered to cause formation of Te-rich CdTe layer near the surface resulting in the back surface field. This back surface field can assist the carriers transport toward the junction so that J_{sc} is enhanced by V_{oc}. The enhanced V_{oc} by air annealing is consistent with earlier report by P. K. Raychaudhuri [52]. It has been reported that heating of CdTe in an oxygen containing atmosphere alters the surface of the CdTe to contain Tellurium oxide (TeO_2) phase [52]. The air annealing has been reported to convert the n-type CdTe to p-type CdTe by S. S. Ou *et al.* [53]. The p-type CdTe film has been characterized to have higher absorption coefficient than n-type CdTe film [53]. This suggests that air annealing could cause the type-conversion in the as-deposited CdTe layer. The as-deposited CdTe layer could be high stoichiometric without sufficient p-type conductivity that results in high resistivity and low cell performance.

With air annealing of the CdS layer and $CdCl_2$ treatment of the CdTe layer, the cell TL09 outperform other cells with V_{oc} of 390 mV, J_{sc} of 6.4 mA/cm^2, and FF of 0.44. If the CdTe layer is assumed to be of similar electrical properties after $CdCl_2$ treatment, air annealing of CdS layer is found to significantly improve cell performance. The

improved V_{oc} suggests that the CdTe/CdS heterojunction has higher built in electric field. The air annealing of CdS and air annealing of CdTe are considered to improve cell performance in a different way. The former improves the built-in electric field in the junction and the latter enhances the back surface field. The higher J_{sc} of cell TL09 suggests that enhancing carrier collection near the junction leads to more efficient carrier collection. The benefit of air annealing to CdTe/CdS heterojunction is corroborated by Y. S. Tyan's report on closed space sublimation (CSS) growth of CdTe solar cells with oxygen [54]. It has been reported that CdS deposited in oxygen leads to an improvements in cell efficiency more than 1% versus CdS deposited in oxygen-deficient ambient [54]. The evident increase of FF and slope change of I-V characteristic suggests that cell TL09 has improvement in R_s and R_{sh}. The reduced R_s caused by air annealing of CdS is consistent with earlier reports on photo conductivity of CdS by Kolomiets *et al*. [55]. It has been reported that annealing of CdS in air improved photoconductivity of CdS by conversion of CdS to CdO [55].

3.5.3 Effect of CdS Treatments

The air annealing of CdS layer has been confirmed to improve cell performance. However, resistivity measurement shows that air annealing increases the in-plane resistivity of the CdS layer by a factor of 3 as well as the resistivity of ITO substrate. Therefore optimizations in the PLD deposition and alternative post-deposition treatments have been experimented to improve the conductivity of the CdS layer. Here the cell TL09 is used as reference to compare with cell TL21 and cell TL22. The reference Cell

TL09 has V_{oc} of 390 mV and J_{sc} of 6.4 mA/cm^2, and FF of 0.44. Fig. 43 shows these three cells with different CdS treatments. Fig. 44 compares the light J-V characteristics of these cells. For the cell TL21, the CdS layer and the CdTe layer were deposited with optimized PLD condition and CdTe layer was processed with $CdCl_2$ treatment. Cell TL 21 has V_{oc} of 2.5 mV, J_{sc} of 0.6 mA/cm^2, and FF of 0.25. For the cell TL22, both of the CdS layer and the CdTe layer were processed with the $CdCl_2$ treatment. Cell TL 22 has J_{sc} of 5.78 mA/cm^2, V_{oc} of 120 mV, and FF of 0.25. The dark J-V characteristics of three cells are shown in Fig. 45.

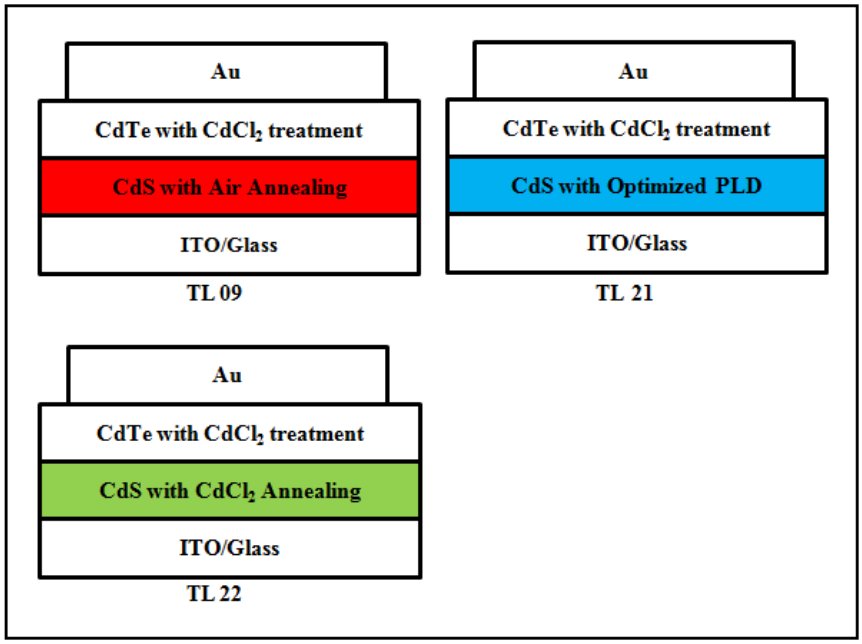

Fig. 43. Structures of the solar cells TL09, TL21, TL22.

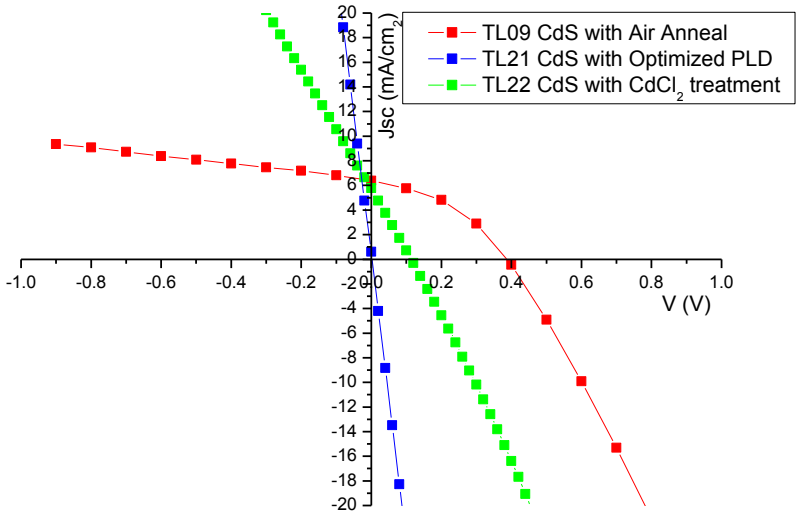

Fig. 44. Light J-V characteristics of the solar cells TL09, TL21, and TL22.

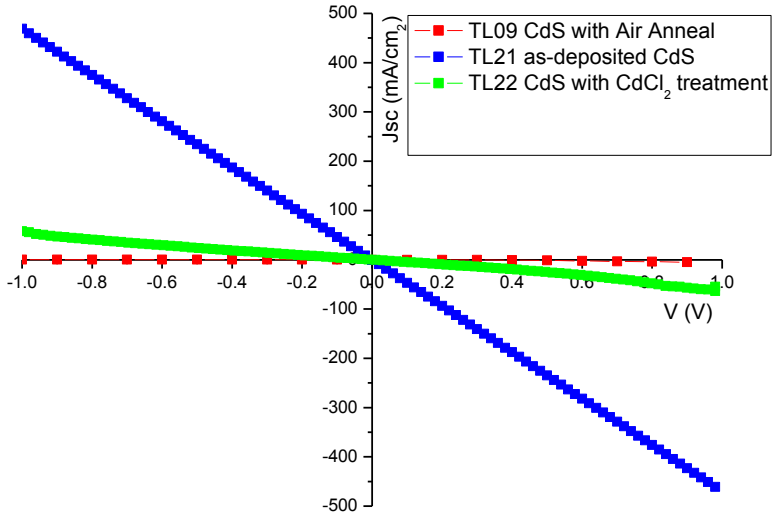

Fig. 45. Dark J-V characteristics of the solar cells TL09, TL21, and TL22.

The optimized PLD condition is found to degrade cell performance. The slopes of dark J-V characteristic in the range of 0 to 40 mV suggest the cell TL22 has much lower low R_{sh} than other cells. By comparing the cell TL21 and the cell TL16, the optimized PLD reduced the V_{oc} from 112 mV to only 2.5 mV and merely improves the J_{sc} from 0.3 mA/cm^2 to 0.6 mA/cm^2. The substrate temperature of 250 °C is confirmed to be better than 300 °C for fabrication of the CdTe/CdS heterojunction. This is consistent with the earlier reports by O. M. Hussian *et al*. [56]. It has been reported that the substrate temperature can affect the stoichiometry of CdTe films prepared by PLD technique [56]. The CdTe films deposited at temperature less than 250 °C shows p-type, CdTe films deposited at temperature higher than 330 °C shows n-type, and CdTe films deposited in the temperature between 250 °C and 330 °C shows intrinsic [56]. The degradation induced by higher substrate temperature is interpreted as that the stoichiometry of CdTe could shift from intrinsic at 300 °C to slightly p-type at 250 °C. Therefore deposition of CdTe layer at temperature lower than 250 °C could promote the formation of p-type CdTe and lead to better efficiency.

The cell TL22 with CdS processed with $CdCl_2$ treatment has J_{sc} of 5.78 mA/cm^2 which is comparable to 6.4 mA/cm^2 for CdS with air annealing. However, the cell TL22 has lower V_{oc} of 120 mV and FF of 0.25 compared to cell TL09. The air annealing is found better than $CdCl_2$ treatment in improving V_{oc} and FF. The $CdCl_2$ treatment suppresses the leakage current and increases R_{sh} to some extent but is not as good as air annealing. In consideration of the comparable J_{sc} with relatively low V_{oc} and low FF, it is found that $CdCl_2$ treatment increases the conductivity of CdS layer. This is consistent

with the earlier reports by A. Romeo *et al.* on $CdCl_2$ treated HVE-CdS (high vacuum evaporated CdS) [57]. It has been reported that $CdCl_2$ treatment causes crystallization in CdS and increases the grain size resulting in better mobility and higher conductivity [57].

3.5.4 Effect of Oxygen

Annealing of the CdS layer with and without $CdCl_2$ in air has been found to improve R_{sh} and increase J_{sc}. To further illustrate the effect of oxygen and the effect of annealing on cell performance, alternative post-deposition treatments such as vacuum annealing and argon annealing have been conducted on the CdS layer. Fig. 46 shows the three cells with different CdS treatments. Fig. 47 compares the light J-V characteristics of these cells. For the reference cell TL09, the CdS layer received air annealing and the CdTe layer received $CdCl_2$ treatment. The reference Cell TL09 gives V_{oc} of 390 mV, J_{sc} of 6.4 mA/cm^2, and FF of 0.44. For the cell TL12, the CdS layer received argon annealing and the CdTe layer received $CdCl_2$ treatment. The cell TL12 has V_{oc} of 5 mV, J_{sc} of 0.6 mA/cm^2, and FF of 0.25. For the cell TL15, the CdS layer received vacuum annealing and the CdTe layer received $CdCl_2$ treatment. The cell TL15 has V_{oc} of 0.24 mV, J_{sc} of 0.3 mA/cm^2, and FF of 0.25.

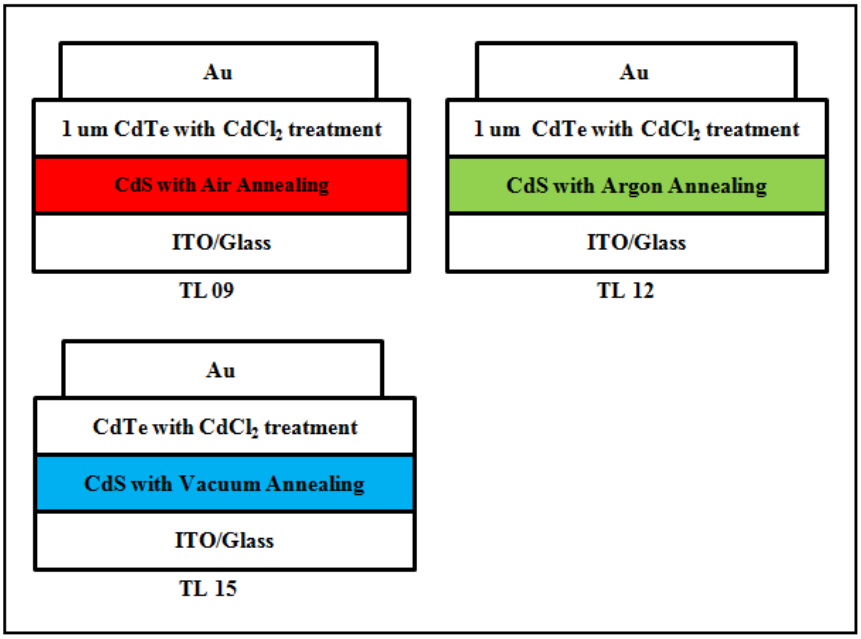

Fig. 46. Structures of the solar cells TL09, TL12, and TL15.

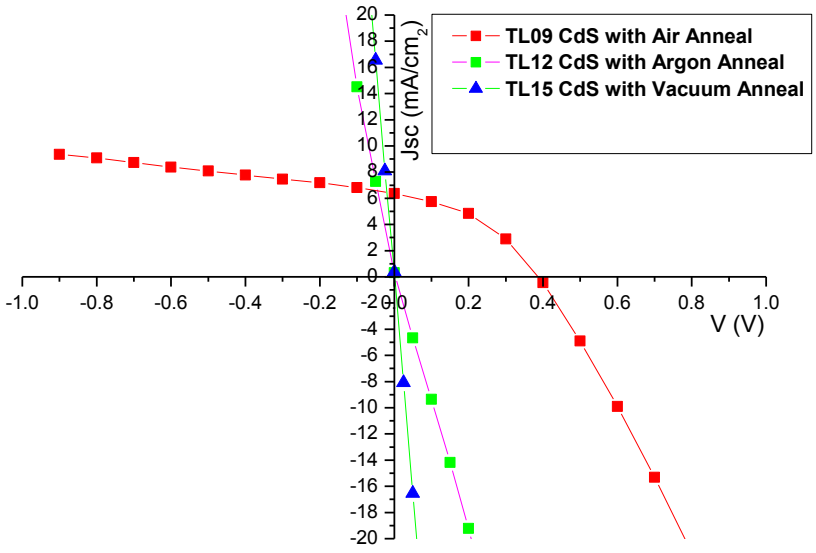

Fig. 47. Light J-V characteristics of the solar cells TL09, TL12, and TL15.

Both argon annealing and vacuum annealing are found to degrade the cell performance similar to the case of optimized PLD condition. The annealing of the CdS layer in presence of oxygen and without presence of oxygen is found to have huge impact on cell performance. The degradation is interpreted as the loss in stoichiometry of CdS due to evaporation of Sulfur (S) at elevated temperature. The non-stoichiometry CdS could lead to deteriorated CdTe/CdS interface that has very low built-in electric field and low V_{oc}. Vacuum annealing of the CdS layer is found to yield even lower V_{oc} and J_{sc} than argon annealing of the CdS layer. This is related to more aggressive evaporation of S in the vacuum than in the argon of 0.03 Torr. The effect of annealing temperature on stoichiometry of CdS is supported by the previous report by N. Romeo *et al*. [58]. The substrate temperature at 150 °C has been suggested for depositing HVE-CdS to prevent the very high evaporation rate of S [58].

The comparison among three cells does shed some light on the understanding of the oxygen effect on the stoichiometry of CdS, as well as the quality of the CdTe/CdS junction. If the CdS layer is annealed in the presence of oxygen, the formation of CdO phase on the surface of CdS may act as a passivation layer preventing the evaporation of S. Therefore, annealing in air is confirmed so far the optimal CdS treatment for thin film CdTe/CdS cells prepared in argon by PLD deposition. The quality of CdS layer could be further improved by deposition of CdS layer at 150 °C instead of 250 °C to promote the stoichiometry of CdS layer.

3.5.5 Effect of Annealing Temperature

The air annealing of CdS and $CdCl_2$ treatment of CdTe combined have been confirmed to achieve the highest efficiency in solar cells fabricated in this research. The insufficient $CdCl_2$ treatment has been suggested as the cause of limited cell performance. Therefore solar cell, with air annealing of CdS layer, received $CdCl_2$ treatment for the same annealing time but at higher temperature was experimented to seek efficiency enhancement. Fig. 48 shows cell TL13 and cell TL09 with the CdS layer received air anneal and CdTe layer received $CdCl_2$ treatment at 420 °C and 390 °C respectively. The argon pressure during the PLD deposition of CdS and CdTe layer was 0.018 Torr which resulted in thinner CdS layer and CdTe layer due to lower deposition rate. Fig. 49 and Fig. 50 compare the light J-V characteristics and dark J-V characteristics for these two cells. Cell TL09 has V_{oc} of 400 mV, J_{sc} of 6.4 mA/cm^2, FF of 0.44, and η of ~1.2%. Cell TL13 has V_{oc} of 460 mV, J_{sc} of 5.8 mA/cm^2, FF of 0.26, and η of ~0.7%.

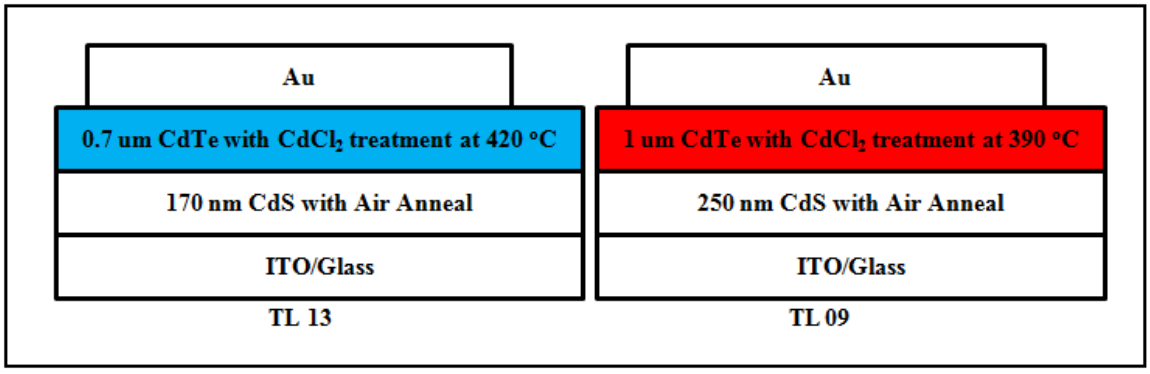

Fig. 48. Structures of the solar cells TL09 and TL13.

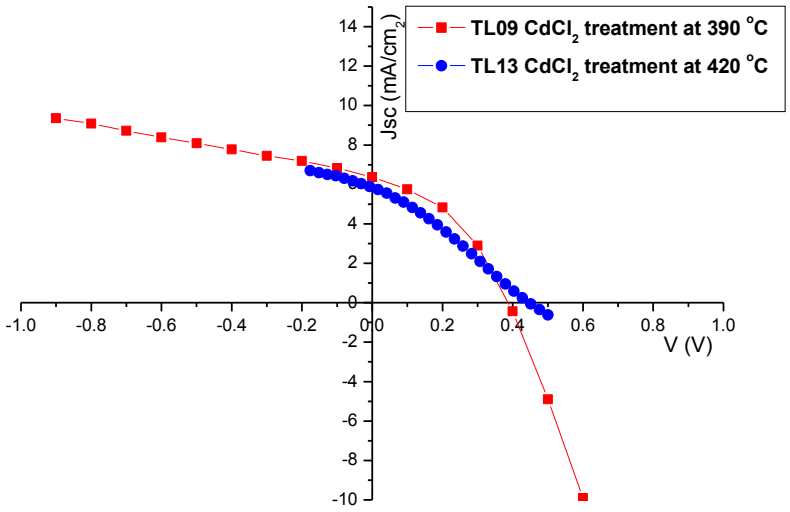

Fig. 49. Light J-V characteristics of the solar cells TL09 and TL13.

The higher temperature of the $CdCl_2$ treatment is found to enhance the V_{oc} by over 50 mV even the CdS layer is 80 nm thinner in cell TL13. The thinner CdS layer typically improves J_{sc} owning to reduced photon loss, but reduces V_{oc} and FF due to shunting effect. The dark J-V characteristics of solar cells TL09 and TL13 are very different. The slope of the dark I-V characteristic in the range of 0 to 40 mV range is indicating cell TL13 has lower R_{sh} corresponding to lower FF. The reasons for lower R_{sh} could be in part due to the thinner CdS layer or the $CdCl_2$ treatment at elevated temperature. $CdCl_2$ treatment at elevated temperature could cause the excess interdiffusion between CdTe and CdS that consumes the CdS layer during the treatment. This influence of thickness of the CdS layer on cell performance is supported by A. D.

Compaan *et al.*'s report [51]. The cells with 0.15 μm CdS have V_{oc} of 0.764 V, J_{sc} of 20.69 mA/cm^2, and FF of 0.66 [51]. The cells with 0.6 μm CdS have V_{oc} of 0.815 V, J_{sc} of 17.61 mA/cm^2, and FF of 0.73 [51]. It has been reported that PVD grown CdS of typically 0.2 to 0.5 μm thick are needed for reliability [59]. The better FF in cell TL09 suggests that the thicker CdS layer of 250 nm is more resistant to interdiffusion during the treatment.

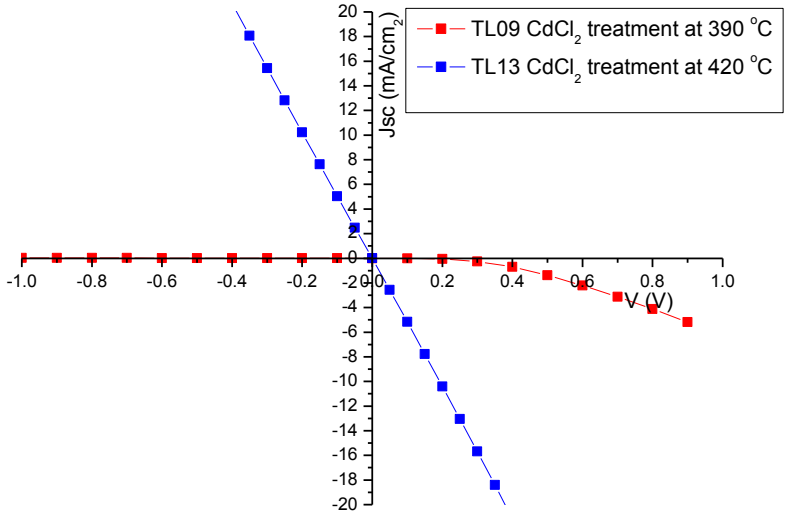

Fig. 50. Dark J-V characteristics of the solar cells TL09 and TL13.

3.5.6 XRD Analysis

XRD θ-2θ scans of thin film CdTe/CdS solar cells before and after the $CdCl_2$ treatment is plotted in Fig. 51. The effect of $CdCl_2$ treatment is examined by the change of crystallographic structure in the CdTe/CdS heterojunction. XRD patterns show that

$CdCl_2$ treatment causes a complete rearrangement of the crystallographic structure of the CdTe films. Before the treatment, CdTe layer has a single CdTe(111) peak with preferential orientation. In sharp contrast, after the treatment, the CdTe layer develops multiple peaks which resemble that of polycrystalline bulk CdTe. This change in crystallographic orientation of the CdTe layer matches well with the observation by H. R. Moutinho *et al*. [60] on PVD CdTe sample processed with $CdCl_2$ treatment. The CdTe(111) peak shifts from 23.781° to 23.87°. This peak shift corresponds to a reduction in the CdTe lattice parameter from 6.481 Å to 6.451 Å. The reduction of lattice parameter supports the interdiffusion between CdS and CdTe resulting in the formation of a mixed CdS_xTe_{1-x} layer with smaller lattice. This is consistent with the formation of alloy between CdTe and CdS observed by B. E. McCandless *et al*. [61]. For the CdS layer, XRD patterns indicated sharpened CdS reflection, and peak shift of CdS(002) from 26.63° to 26.49°. This peak shift also corroborates that the alloy formation in the CdS layer due to interdiffusion between CdS and CdTe.

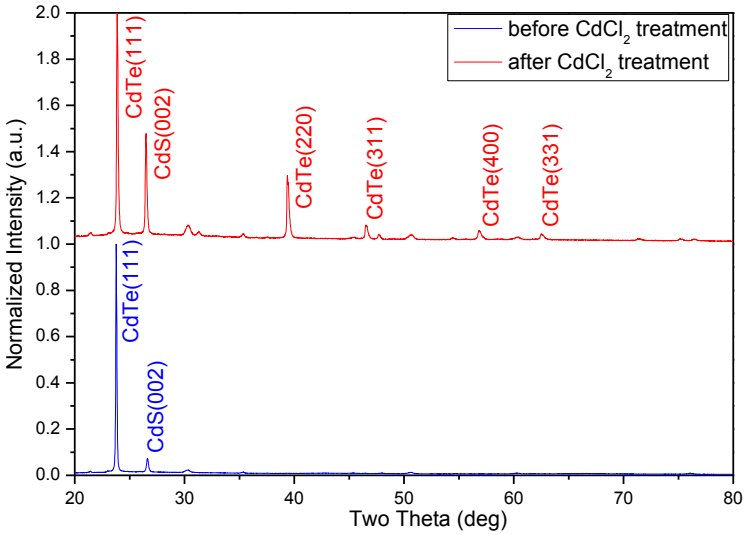

Fig. 51. XRD pattern of a CdTe solar cell before and after $CdCl_2$ treatment.

3.5.7 Cross-sectional SEM Analysis

Cross-sectional SEM images were obtained for solar cells with CdS of different conditions which include air annealing, optimized PLD condition, and $CdCl_2$ treatment. Fig. 52 and Fig. 53 show the cross-sectional SEM images of the cell TL20 with CdS processed with air annealing. The cell has continuous and uniform CdTe/CdS heterojunction on top of ITO substrate. The grain size of CdTe is observed to be close to 1 μm in some area but the diameter of grains in majority is by less than 0.2 μm. It is found that the CdS layer is only ~123 nm thick which accounts for low V_{oc} of 46 mV and FF of 0.25 measured in this cell.

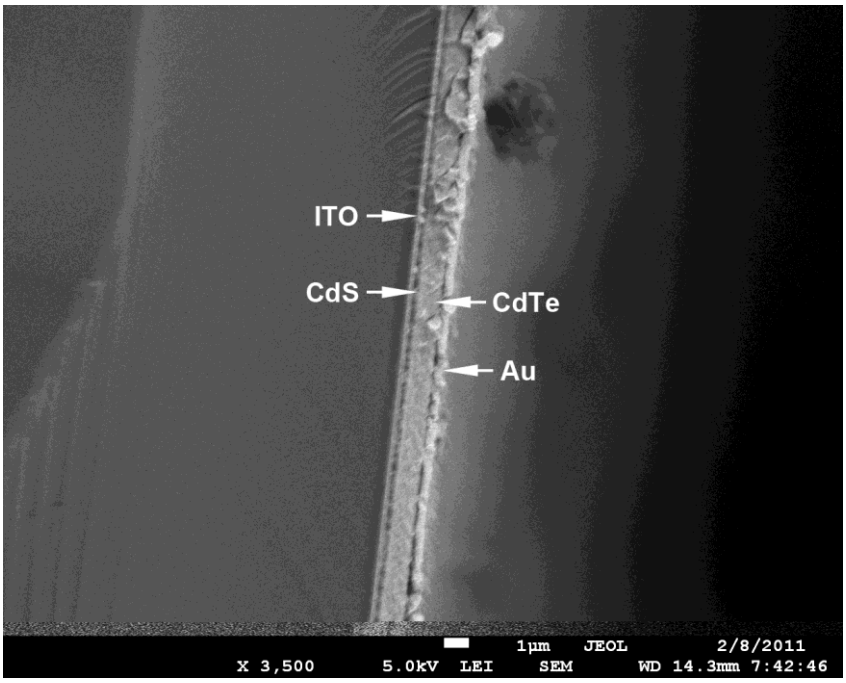

Fig. 52. Cross-sectional SEM image of the solar cell TL20 (low-magnification).

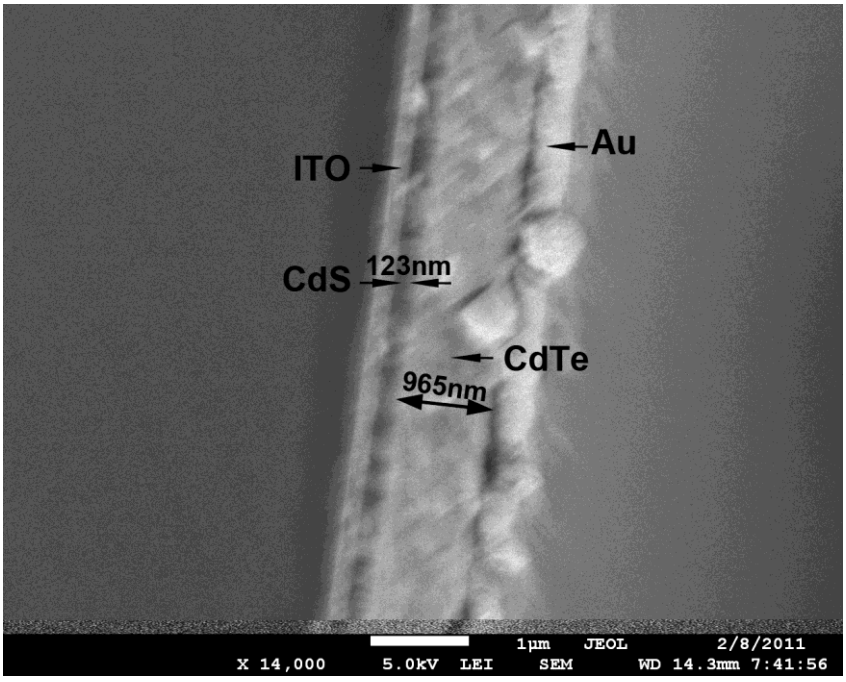

Fig. 53. Cross-sectional SEM image of the solar cell TL20 (high-magnification).

Fig. 54 and Fig. 55 show cross-sectional SEM images of the cell TL21 with CdS deposited with optimal PLD conditions without annealing. Fig. 54 show the cell has continuous and uniform CdTe/CdS layer on top of ITO substrate. The delamination between the ITO substrate and the CdTe/CdS junction is in part due to poor adhesion of the as-deposited CdS. Both the CdTe layer and the CdS layer have quite similar columnar grains with average grain size of 100 nm. It is evident that the small grain size and high density of grain boundaries accounts for high R_s and small R_{sh}. Fig. 55 shows the local region of CdTe/CdS junction. It is worth to note that thickness of the CdS layer is close to 400 nm in some area but is reduced significantly to only less than 200 nm in some area. The non-uniformity and thickness reduction in CdS layer is responsible for degradation in V_{oc} and FF. Moreover, CdS layer, although with thickness of at least 200 nm, still results in low V_{oc} and FF which could be in part due to shunting in the grain boundaries.

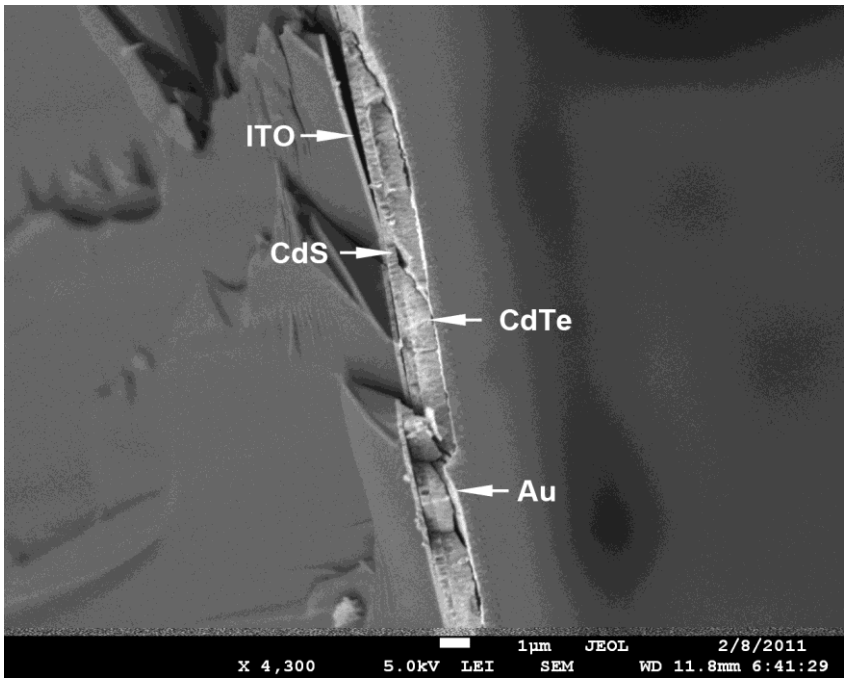

Fig. 54. Cross-sectional SEM image of the solar cell TL21 (low-magnification).

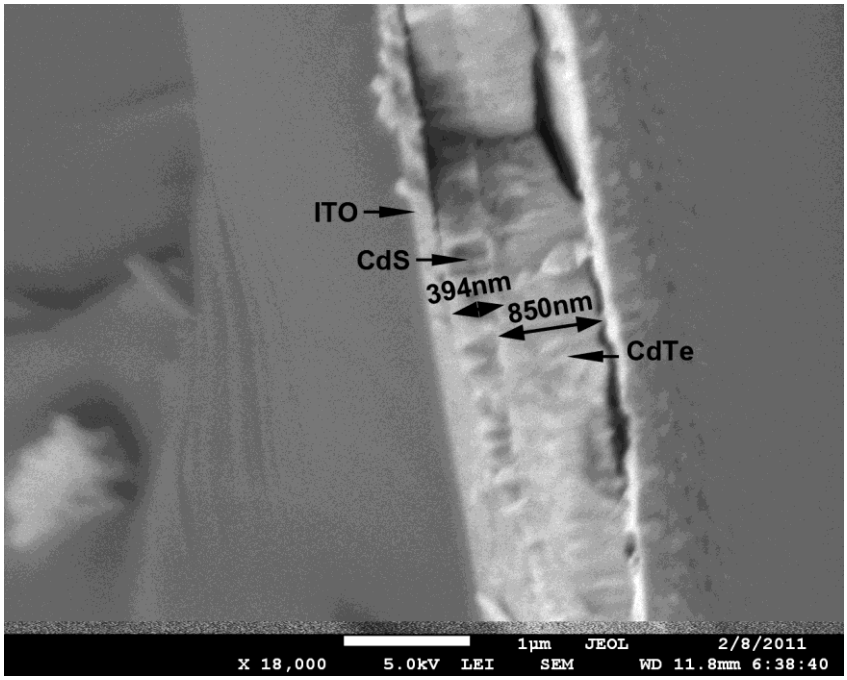

Fig. 55. Cross-sectional SEM image of the solar cell TL21 (high-magnification).

Fig. 56 and Fig. 57 show cross-sectional SEM images of the cell TL22 with CdS processed with $CdCl_2$ treatment. The cell has continuous and uniform CdTe/CdS layer. The $CdCl_2$ treatment of CdS is similar to air annealing in maintaining the uniform and continuity of the CdS layer. However, the CdS grains of larger size are not observed in the $CdCl_2$ treated CdS. The integrity of the CdS layer is related to the better J_{sc} and R_{sh} as shown in the J-V characteristic. Fig. 57 shows that cell TL22 has 250 nm CdS layer which accounts for the better V_{oc} of 120 mV among these three cells characterized by SEM. Both of the air annealing and $CdCl_2$ treatment have been confirmed to effective suppress the consumption of CdS due to CdTe/CdS intermix during the $CdCl_2$ treatment. This is consistent with report by B. E. McCandless *et al*. [62] in that $CdCl_2$ treatment of CdS restructures the CdS layer and making CdS resistant to Te diffusion.

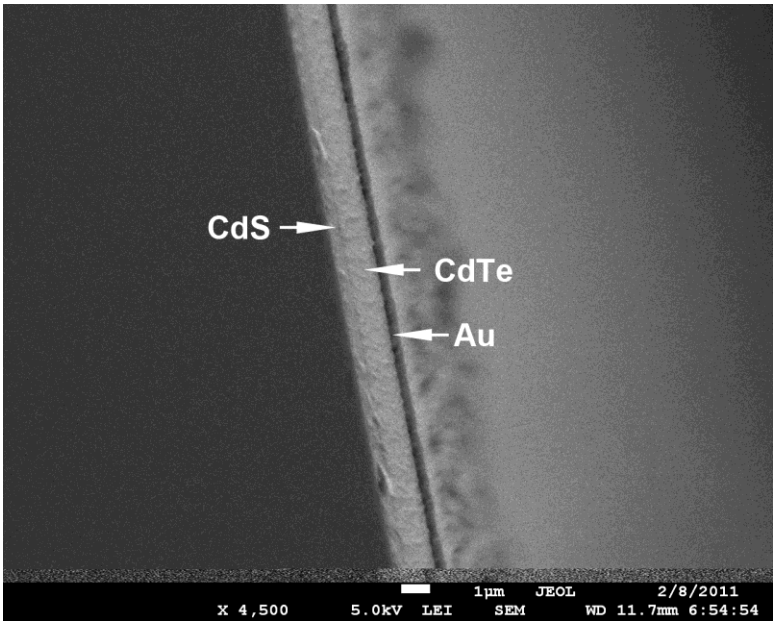

Fig. 56. Cross-sectional SEM image of the solar cell TL22 (low-magnification).

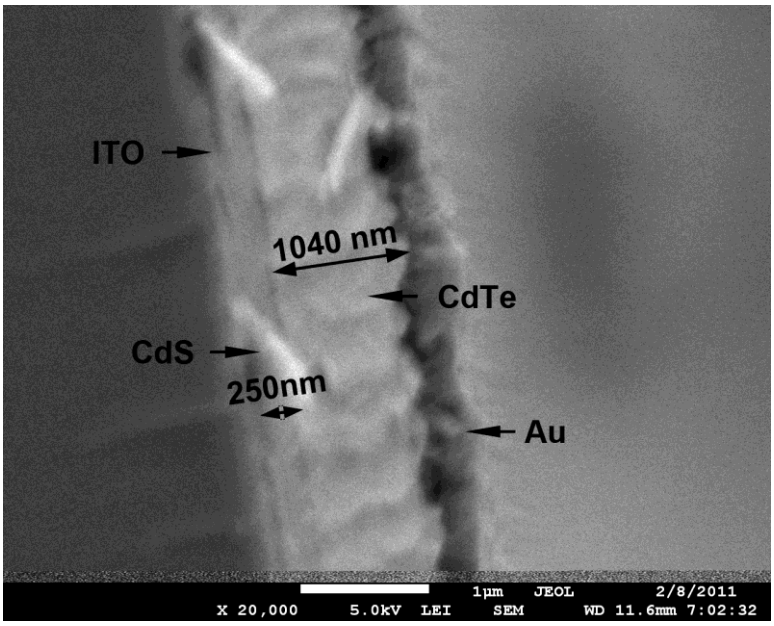

Fig. 57. Cross-sectional SEM image of the solar cell TL22 (high-magnification).

3.5.8 Cross-sectional TEM Analysis

To further understand the origin of high R_s and low R_{sh} for further optimization of cell performance, cross-sectional TEM study was conducted on the 1.2% efficient solar cell TL09. Fig. 58 shows that the cell TL09 has a uniform and continuous CdTe/CdS junction formed between the CdTe layer of ~913 nm and the CdS layer of 260nm. The TEM image is consistent with the SEM images in showing no presence of ITO/CdTe junction due to consumption of CdS layer by the $CdCl_2$ treatment. The average grain size of the CdTe layer is observed to be in the range of 100 to 200 nm. This grain size is significantly smaller than that of 1 to 2 μm observed in CdTe layer of high efficiency CdTe cells deposited at high temperature or received effective $CdCl_2$ treatment [33]. Small grain size is equivalent to high density of grain boundary resulting

in high density of efficient recombination centers that sink photo generated carriers and reduce J_{sc} [13]. The defects such as twins and dislocations are observed in high density as shown in the Fig. 58. The defects within CdTe grains act as traps that capture the carriers and reduce the carrier lifetimes [13]. The grain boundaries, defects, and grain size within CdTe layer and CdS layer revealed by the TEM image are confirmed as the origins of R_s and R_{sh}.

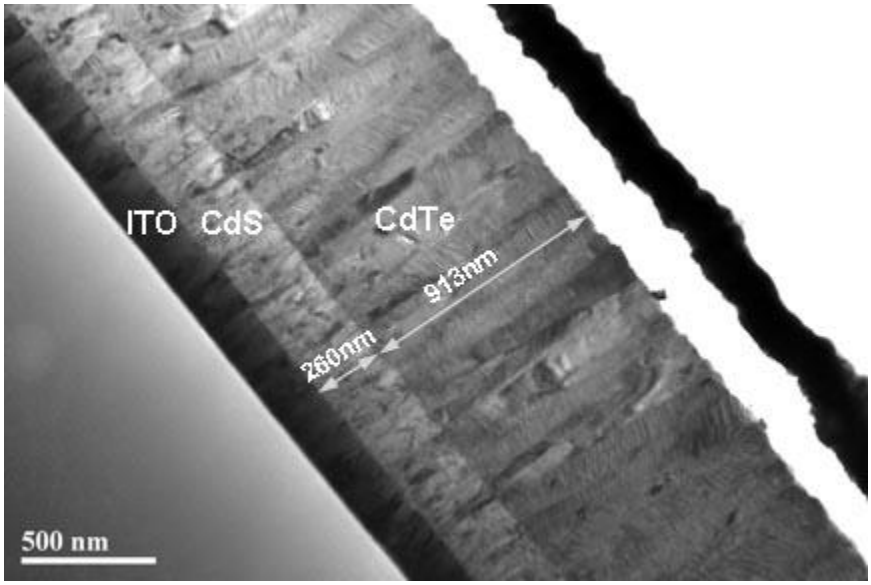

Fig. 58. Cross-sectional TEM image of the solar cell TL09.

Fig. 59 shows the TEM image of the CdTe/CdS interface. The observed domain match in the interface region indicates the presence of interface states due to lattice mismatch between CdTe and CdS. The interface states could act as effective surface

recombination centers that sink the carriers traveling across the junction [13]. The $CdCl_2$ treatment is confirmed by TEM to be insufficient to repair these interface states. Dislocations are observed in the CdTe/CdS interface as shown in Fig. 60. The density of these dislocations could be a measure of the effectiveness of $CdCl_2$ treatment. A discontinuous oxide phase is found near the interface. The oxide phase can be originated from the interaction between CdS and oxygen during the air annealing. The oxide phase could cause non-uniformity in spatial current flows across the CdTe/CdS junction. The possible oxide trace on CdS surface can be removed by dilute HCl etching or hydrogen annealing to improve J_{sc} [50, 63].

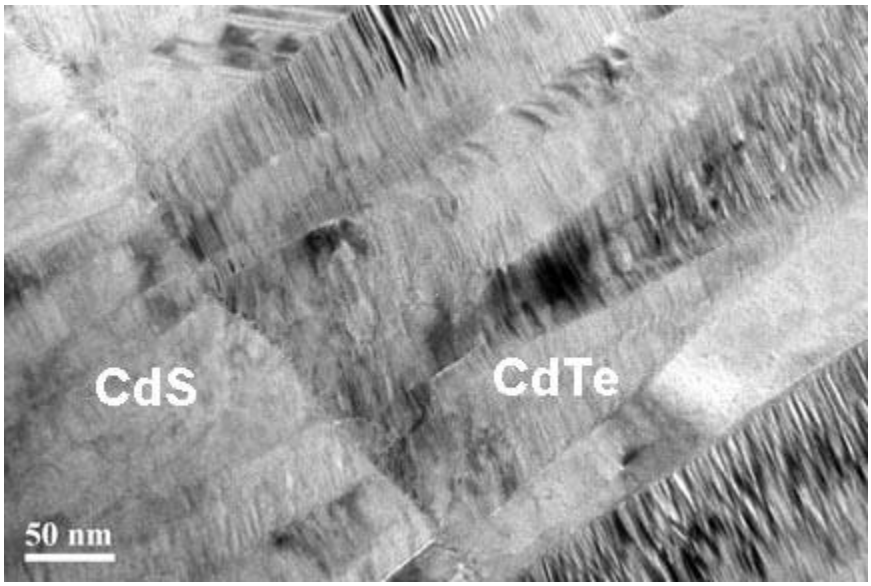

Fig. 59. Cross-sectional TEM image of the CdTe/CdS interface.

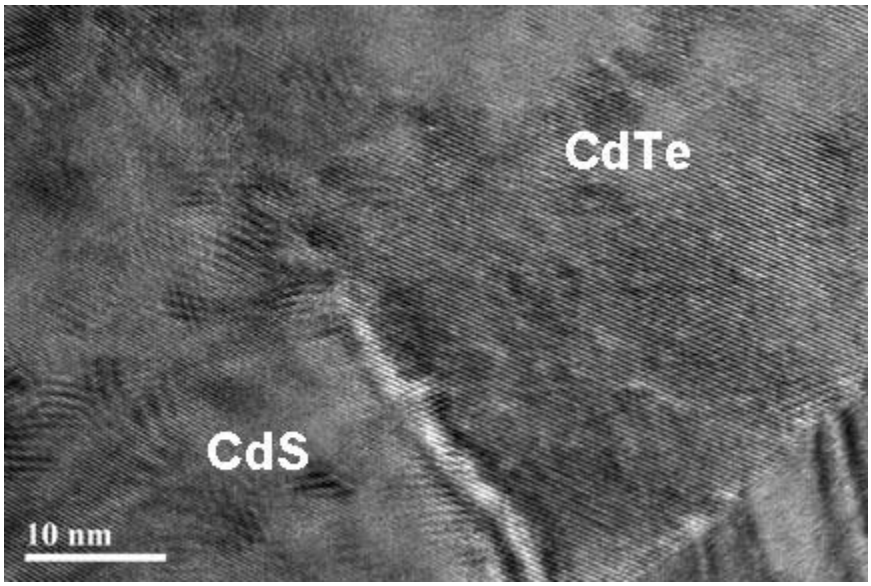

Fig. 60. Cross-sectional TEM image of the dislocations and the oxide phase.

Fig. 61 shows an area of interest in the CdTe grain where twins of high density are observed. The lamellar twins of double directions match with the observation by Y. Yan *et al*. [64]. It has been reported that the double-positioning twin boundaries have Te dangling bonds and Cd dangling bonds [64]. These dangling bonds, if left without passivation, are effective carrier traps that sink photogenerated carriers. It has been reported that the twins create energy states in the band gap that harm electronic property of CdTe [64]. The CdS grain is found to have dislocations but not twins of high density. The origin of twins was explained by A. W. Vene *et al*. in that twinning is an intrinsic property of the zinc blend structure in CdTe single crystal [65]. The abundance of twinning was determined by the ionicity of the lattice [65]. The formation of twins may be originated from vapor-solid interface during the growth. The presence of these defects

suggests that insufficient $CdCl_2$ treatment is limiting the cell performance by not effectively reducing the density of these defects in CdTe layer and CdS layer.

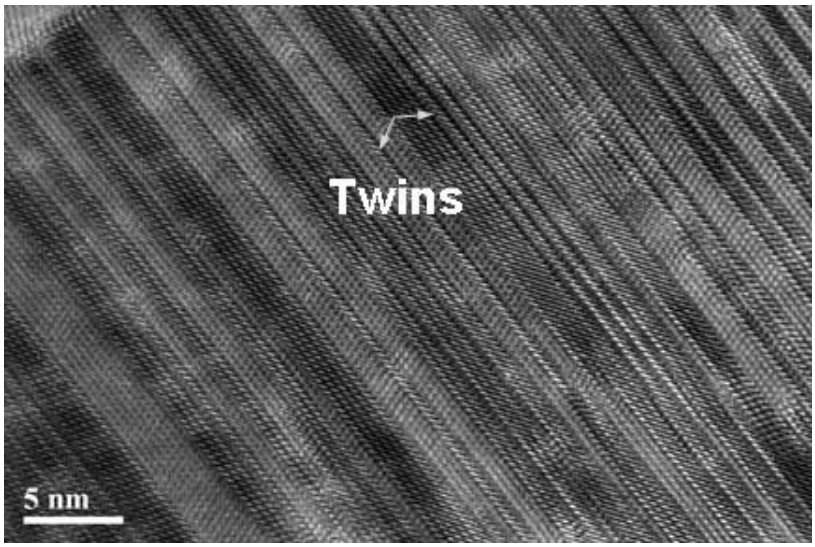

Fig. 61. Cross-sectional TEM image of twins in CdTe.

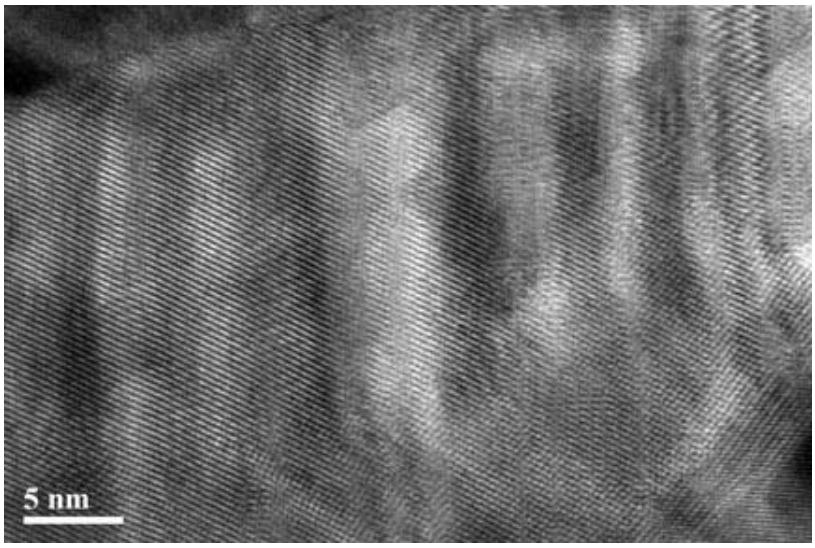

Fig. 62. Cross-sectional TEM image of defects in CdS.

3.5.9 Analysis of $CdCl_2$ Treatment

The J-V characteristics and microstructure studies have confirmed insufficient $CdCl_2$ treatment could be the key limiting factor for relatively low cell performance. The $CdCl_2$ treatment used in this research is compared with previous reported $CdCl_2$ treatments to clarify the issues of $CdCl_2$ treatment. The solar cell TL09 with insufficient $CdCl_2$ treatment and the PVD cell without $CdCl_2$ treatment is similar in microstructure as shown in Fig. 63 [66]. In Fig. 64, the PVD cell, without effective $CdCl_2$ treatment, actually has V_{oc} of ~400 mV and J_{sc} of 4 mA/cm^2. This PVD cell before treatment is similar in performance as the cell TL09 after treatment. In sharp contrast, the effective $CdCl_2$ treatment improved J_{sc} by a factor of 5 and V_{oc} by a factor of 2 for the same PVD cell as shown in Fig. 64 [66]. This correlates with microstructure changes such as growth of grain size by a factor of 10, and evident reduction in the density of the defects as well as grain boundaries in the CdTe/CdS heterojunction as shown in Fig. 63 [66]. This suggests the current thin film CdTe cells have room to improve provided the effective $CdCl_2$ treatment.

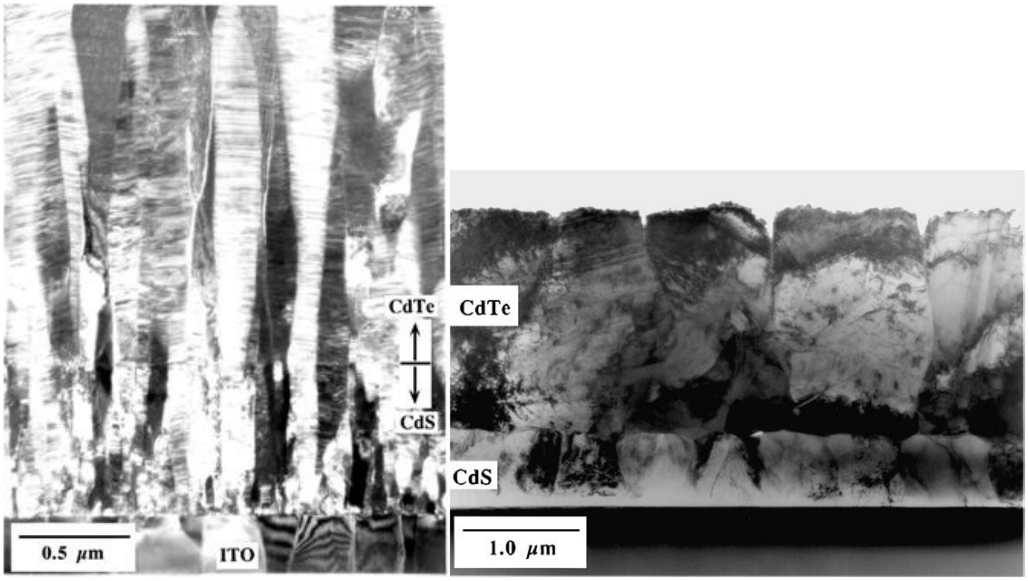

Fig. 63. Cross-sectional of TEM image of the PVD CdTe/CdS cell before $CdCl_2$ treatment (left) and after $CdCl_2$ treatment (right) [66].

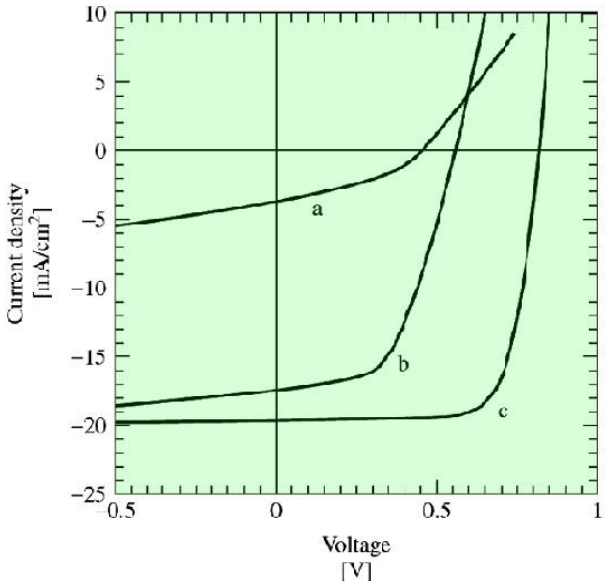

Fig. 64. Current density-voltage characteristic of a PVD CdTe/CdS cells as-deposited (curve a), after air annealing (curve b), and after $CdCl_2$ treatment (curve c) [66].

The issue of insufficient $CdCl_2$ treatment is considered to be the annealing profile. In this research, the annealing profile of the $CdCl_2$ treatment is heating at 390 °C for 10 minutes. Table 3 summarizes the annealing profiles of representative effective $CdCl_2$ treatment with respect to different CdTe layer thickness by previous results [23, 50, 66]. The $CdCl_2$ treatment at 390 °C for 10 min has been reported optimal for 1 μm rf sputtered CdTe cell by A. D. Compaan *et al*. [23]. However, it has been confirmed in this research that this annealing profile results in insufficient $CdCl_2$ treatment for 1 μm PLD deposited CdTe cells under similar deposition conditions. The electrical data and microstructure results show that CdTe solar cells prepared by PLD require longer annealing time for the same temperature and CdTe layer thickness. This is consistent with the annealing time of 30 minutes suggested for the 1 to 2 μm PVD deposited cell fabricated by R.W. Birkmire *et al.* [66]. It is confirmed that current PLD cell has similar quality as the PVD cell which requires the $CdCl_2$ treatment with longer annealing time to achieve the desired change in microstructure and electrical properties.

Table 3 A List of representative $CdCl_2$ treatments receipts.

Research Groups	Temp (°C)	Time (min)	CdTe (μm)	CdS (μm)	Efficiency (%)	CdTe layer fabrication	CdS layer fabrication
D. H. Rose [50]	400	40	8 – 10	0.08	12.6	CSS	CBD
R.W. Birkmire [66]	400	30	2	1-2	9.6%	PVD	PVD
A. D. Compaan [23]	390	10	1	0.06	12%	Sputter	Sputter

3.5.10 Analysis of Oxygen Incorporation

Introduction of oxygen during the fabrication is suggested to further improve cell performance. Oxygen incorporation in CdS by air annealing has been demonstrated essential to reproducibly achieve the 0.73% and 1.2% efficient solar cells in this research. Fabrication of CdTe solar cells by PLD technique is considered similar to the case of cells produced by CSS technique—oxygen incorporation is beneficial to the formation of efficient CdTe/CdS heterojunction. It has been demonstrated that CSS deposition of CdTe/CdS junction at high temperature requires sufficient amount of oxygen to improve V_{oc} by several hundred mV and results in 8.9 % efficient cell [67]. The deposition of CdS layer in appropriate amount of oxygen could allow for the use of thinner CdS layer without degradation of R_{sh} because oxygen effective passivates the grain boundaries of CdS. It has been reported that the incorporation of oxygen in the CdS deposition was found to create CdO or $CdSO_3$ phase which passivates the grain boundaries of CdS and suppress Te diffusion [58]. X. Wu *et al*. reported 15.5% efficient cell utilizing a 50 nm CdS layer rf sputtered in Argon containing 2% oxygen at room temperature [68]. Therefore oxygen incorporation in fabrication is considered crucial to improve the cells by PLD deposition.

3.6 Summary of Thin Film CdTe Solar Cells

In summary, a process has been demonstrated to fabricate thin film CdTe/CdS solar cells with efficiency exceeding 1% by PLD technique. Two post-deposition treatments have been demonstrated to improve the cell performance significantly. The

first treatment is air annealing on CdS layer and the second treatment is $CdCl_2$ treatment on CdTe layer. These two treatments combined have been proven to improve the current, voltage, and fill factor to a greater extent than that achieved in the sample with only the air annealing of CdTe layer. The air annealing of CdS layer is more effective than $CdCl_2$ treatment of CdS in improving the cell voltage and fill factor. Other post-deposition treatments such as vacuum annealing and argon annealing have been found to degrade cell performance. The possible reasons of high series resistance and shunt resistance in current CdTe solar cells by PLD have been identified by the microstructure analysis. The $CdCl_2$ treatment at 390 °C for 10 min is insufficient to achieve desired grain growth and reduction of defect density in solar cells fabricated by current PLD receipt. The adjustment of $CdCl_2$ treatment as well as oxygen incorporation during the fabrication has been proposed to further enhance the cell performance.

4. SUMMARY AND CONCLUSIONS

4.1 Conclusions

In this thesis, new thin film solar cells with light trapping transparent conducting oxide layer has been proposed with three new configurations in the first section. The potential LT-TCO layer with good conductivity and desired surface texture has been demonstrated in the second section. The baseline thin film CdTe solar cells with efficiency exceeding 1% have been achieved and discussed in the third section.

For the development of LT-TCO layer, AZO thin film has been found to be a good candidate. Two AZO multilayer films have been fabricated and shown different optical and electrical properties. The OAZO/VAZO multilayer shows reduced transmittance and surface texture, and is a promising LT-TCO layer that provides the light trapping function and the sufficient low resistivity of ~4 x 10^{-4} Ω-cm. The VAZO/OAZO multilayer shows smooth surface, high transmittance of ~85%, and improved resistivity of ~1.5 x 10^{-4} Ω-cm. By reducing the resistivity of VAZO layer through tuning the PLD parameter, the thickness of the LT TCO layer can be further reduced to minimize the photon loss. Meanwhile, the surface texture and surface roughness of the OAZO layer can be further tuned to achieve better light trapping effect.

For the baseline thin film CdTe solar cells, thin film CdTe solar cells with conversion efficiency of 1% and 0.7% have been demonstrated by PLD deposition. The CdTe/CdS heterojunction cells were deposited at low temperatures followed by optimized post-deposition treatments. The air annealing is found to significantly enhance the overall cell performance. The $CdCl_2$ treatment requires longer annealing time to

achieve the desired microstructure and lead to the enhancement for thin film solar cells. The oxygen back pressure during deposition is proven to be beneficial to thin film CdTe solar cells prepared by PLD. However further optimization of the oxygen pressure during the deposition of CdTe/CdS heterojunction is needed for achieving high efficiency solar cells.

4.2 Future Research Plans

In order to further optimize cell performance, adjustments in PLD conditions and in post-deposition treatments are proposed for future research. Deposition of the CdS layer at low temperature such as 150 °C could ensure the stoichiometry and mitigate the loss of Sulfur. Higher laser energy density is suggested to compensate the kinetic energy of adatoms to assist the diffusion of adatoms at lower substrate temperature. These adjustments are expected to increase the carrier concentration of CdS resulting in built-in electric field of the CdTe/CdS heterojunction. Deposition of CdTe at the substrate temperature of 200 °C is suggested to promote the p-type conductivity of CdTe layer. In addition, optimization in the CdTe target deserves consideration. By adding appropriate amount of Te in the CdTe target, the excess Te in CdTe target could promote the formation of Te-rich p-type CdTe film. The optimizations in target preparation and substrate temperature are expected to improve the p-type conductivity of CdTe as well as the built in electric field.

Optimization in post-deposition treatments aims to improve the crystallinity of the CdTe/CdS heterojunction deposited at low temperature. Higher annealing

temperature such as 450 °C is proposed to promote re-crystallization of the CdS layer. The larger grain size and lower density of grain boundaries in CdS layer assisted by annealing at higher temperature could achieve thin CdS layer with sufficient high R_{sh}. The $CdCl_2$ treatment shall be explored more in the future. The annealing time is suggested to be at least 20 minutes or longer to seek complete microstructure change and efficiency enhancement. Meanwhile alternative $CdCl_2$ vapor treatment shall be examined. This method is expected to reduce the residual $CdCl_2$ on CdTe surface that could be detrimental to the contact between the CdTe layer and Au electrode.

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