DIGITALLY ASSISTED MULTI-CHANNEL RECEIVERS

A Thesis

by

KRISHNA ANAND SANTOSH SRIKANTH PENTAKOTA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Sebastian Hoyos
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	Donald Friesen
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ABSTRACT

Digitally Assisted Multi-Channel Receivers. (August 2010)

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This work presents a data estimation scheme for wide band multi-channel charge sampling receivers with *sinc* filter banks together with a complete system calibration and synchronization algorithm for the receiver. A unified model has been defined for the receiver containing all first order mismatches, offsets and imperfections and a technique based on least mean squares algorithm is employed to track these errors. The performance of this technique under noisy channel conditions has been verified. The *sinc* filter bank is compared with the conventional analog filter banks and it is shown that the *sinc* filter banks have very low computational complexity in data estimation

Nextly, analytical tools for the design of clock-jitter tolerant multi-channel filter-bank receivers have been developed. Clock-jitter is one of the most fundamental obstacles for the future generation of wideband receivers. Additionally all the trade-offs and specifications of a design example for a multi-channel receiver that can process a 5 GHz baseband signal with 40 dB of signal-to-noise-ratio (SNR) using sampling clocks that can tolerate up to 5 ps of clock-jitter standard deviation are presented. A novel bandwidth optimization technique has been presented. As a part of it the bandwidth of the filters

present in each path is optimized thereby improving the performance of the receiver further in the presence of sampling clock jitter. The amount of bandwidth reduction possible depends on the order of the filter and the noise amplification provided by the reconstruction matrix. It has been shown that 3^{rd} order filters of bandwidth 1 GHz can be replaced with 1^{st} order filters of bandwidth 100 MHz without any depreciation in the output resolution, implying huge power savings.

To Amma and Naana

ACKNOWLEDGEMENTS

I would like to express my sincere appreciation and gratitude to my advisor, Dr. Sebastian Hoyos, for the guidance and support he has given me throughout my graduate studies at Texas A&M University. He encouraged critical thinking and reasoning which I believe will help me a lot in my career ahead. Technical discussions with him improved my thought process and strengthened my technical abilities. I am grateful to Dr. Hoyos for giving me an opportunity to work with his group on some very interesting and innovative projects.

Next, I would like to thank my committee member, Dr. Silva, whose courses taught me the basics of circuit design and helped sharpen my skills of analysis and design of circuits. Special thanks to Dr. Peng Li and Dr. Friesen for serving on my committee and supporting my thesis work.

Thanks also go to my project colleagues, Pradeep, Ehab, Xi and Hemanth, for their company, support and feedback on my work. Special thanks to my friends and roomies who have shared all my joys and sorrows and made my stay at TAMU a memorable and enjoyable experience.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

The increasing interest towards the realization of multi-standard radios [1]-[7] has created a tremendous pressure on the analog to digital converter. Also the problem of overloading of the available bandwidth hasn't been worse and the steep rise in the number of users gaining access to wireless devices isn't helping the situation either. These trends are pushing the product development groups around the world to engineer digital intensive communication systems which can process very high bandwidths and also support multiple communication standards. To achieve such systems the ADC which was at the end of the receiver chain is being continually shifted towards the antennae, therefore high dynamic range ADC's capable of handling huge bandwidths are needed. The farthest the ADC can be pushed is right after the antennae and this architecture was first defined by Mitola as the Software Defined Radio [8], the SDR processed the entire bandwidth using a high resolution and high speed ADC and remaining operations were done in DSP. The current trend in SDRs is to design highly reconfigurable analog front ends which can handle narrow-band and wideband standards, one at a time. In-order to develop a SDR the main bottleneck is the ADC which needs to have high bandwidths as well as good dynamic range. Achieving both high sampling rates and dynamic range is a huge task since improving one parameter greatly degrades the other parameter.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

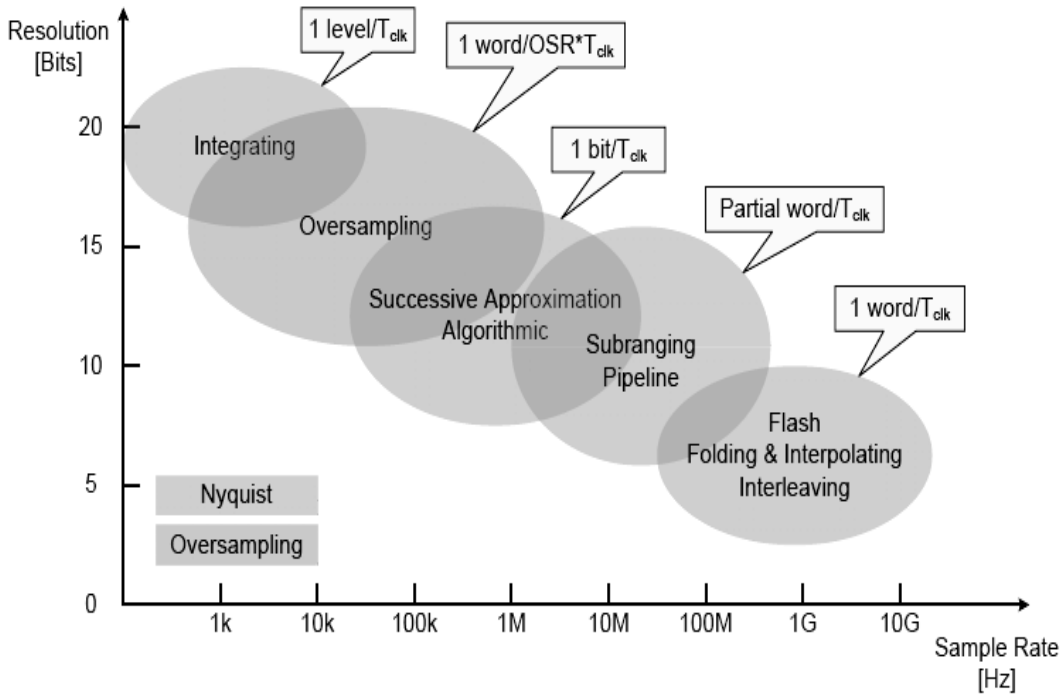

Fig. 1. Dynamic Range versus Sample Rate Trade-off.

Fig. 1 clearly depicts the problem designers around the world are facing in-order to build better ADC's. Because of the high level of complexity involved in this problem the realization of software defined radios has generally been referred to as something which is improbable.

The best way to go around this problem is by parallelizing the ADC architecture. In fact the development and use of such architectures has been greatly researched into and various multi channel architectures have been developed which achieve good resolution and sampling rates. The time-interleaved bank of ADCs is one such popular technique which aims at reducing the sampling speed of each ADC. For very-high-

speed applications, time interleaving increases the overall sampling speed of a system by operating two or more data converters in parallel.

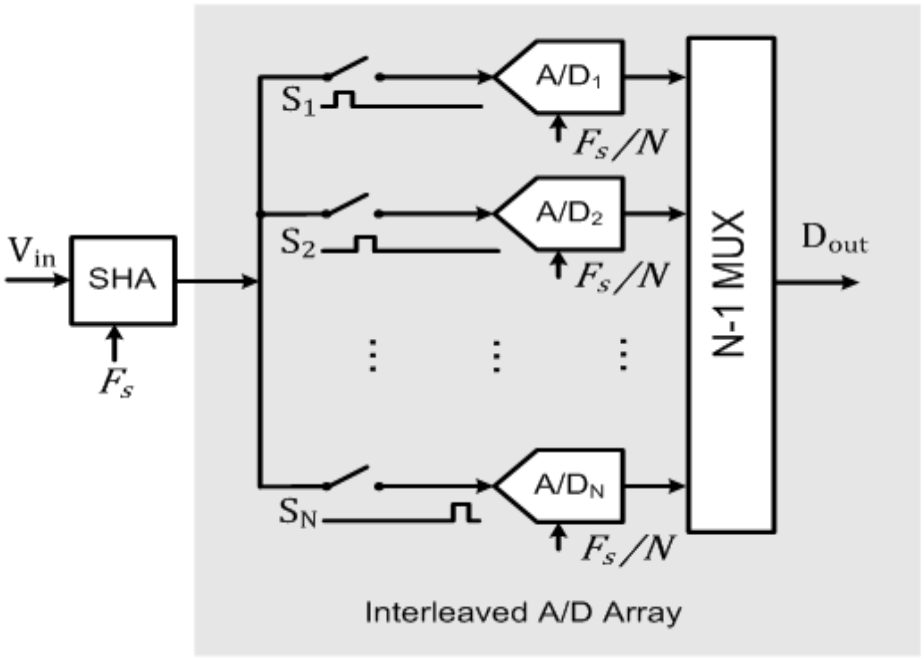

Fig. 2. Conventional Time Interleaved ADC.

This sounds reasonable and straight forward but actually requires much more effort than just paralleling two ADCs. Before discussing this arrangement in detail, compare the sampling rate of a time-interleaved system with that of a single converter. As a rule of thumb, operating N number of ADCs in parallel increases the system's sampling rate by approximately a factor of N. Thus, the sampling (clock) frequency for an interleaved system that hosts N ADCs can be described as follows:

$$f_{system-clock} = \sum_{k=1}^{N} f_{ADC}(k)$$

The simplified block diagram in Fig. 2 illustrates a single-channel, time-interleaved ADC system in which *N* ADCs increase the system's sampling rate. Fig. 2 illustrates 1-to-*N* analog multiplexing scheme where *N* switches are clocked by *N* uniformly spaced clock phases. Each clock is running *N* times slower than the Nyquist rate, which relaxes the sampling rate of the *N* parallel ADCs but still requires a front-end sample-and-hold amplifier (SHA) sampling at full Nyquist rate (Fs).

This rate f_{system_clock} is a clock signal at N times the rate of each ADC $f_{Clk1} = f_{Clk2} = f_{Clk3}..=f_{ClkN}=f_S/N$. Because f_{Clk1} is delayed with respect to f_{Clk2} by the period of f_{System_Clk}, the N ADCs sample the analog input signal sequentially , producing an overall sample rate equal to f_{System_Clk}.

Time Interleaving can be done in many ways like different type of ADCs can be used in multiple steps –coarse and fine. Pushing the operational limits of interleaved ADCs can be very attractive, but various limitations and considerations must be taken into account before turning this method into a successful experiment.

1.1 Bandwidth Limitations

Applications that call for higher sampling speeds usually deal with higher-frequency input tones, so a data converter with an input bandwidth of half the sampling speed would not be suitable for interleaving, the input bandwidth has to be much lesser than that. Also the front end of such ADC’s have a track and hold amplifier in most cases to make the received signal full scale, such amplifiers should be having small signal power much greater than the input bandwidth and should be able to deliver full power in the frequency range of interest. Fortunately, most high-speed data converters

include track/hold (T/H) amplifiers whose full-power and small-signal bandwidths are significantly higher than that called for by the Nyquist ($f_{SAMPLE}/2$) criteria.

1.2 Offset and Gain Errors

The channel-to-channel matching of offset and gain in separate ADCs is not trimmed, so gain and offset mismatches between ADCs are parameters of concern in a time-interleaved system. If one ADC shows an offset and the other a gain error, the digitized signal represents not only the original input signal but also an undesired error in the digital domain. An offset discrepancy causes a signal phase shift in the digitized signal, and gain mismatches show up as differences in signal amplitude. For interleaving designs, you should therefore choose ADCs with integrated gain and offset correction or include external circuitry that allows you to correct these mismatches.

1.3 Nonlinearities

Integral nonlinearity(INL) is described as the deviation of the actual transfer function from a straight line, either in LSBs or in percent of full-scale range (%FSR). INL errors of ±1LSB are quite common for individual ADCs, but in an interleaving system such errors can easily double, causing output-code errors that resemble the offset and gain problems discussed above. The appearance of nonlinearity introduces distortion into the system, which degrades dynamic parameters such as signal-to-noise and distortion ratio (SINAD) and effective number of bits (ENOB).

1.4 Clock Phase Jitter and Noise

The signal used as a system clock should have the lowest possible phase noise. Introducing a D-type flip-flop in a divide-by-two configuration reduces the otherwise stringent requirement for a precise 50% duty cycle. One should choose a clock circuit commensurate with the signal source's frequency range, amplitude, and slew rate.

A low slew rate on the digitized signal relaxes the jitter requirement on the clock. If this slew rate is large, however, the clock jitter must be minimized. For a full-scale-amplitude sinusoidal input signal, the maximum suggested signal-to-noise ratio (SNR) due to clock jitter only is

$$SNR_{dB(MAX)} = 20\log_{10}\log_{10}[1/(2\pi * f_{in} * \sigma_{jitter})] \quad (1)$$

The fact that each ADC still sees the entire signal bandwidth places stringent requirements on the track-and-hold circuitry thus increasing the power consumption. Another approach is to split the entire signal bandwidth into smaller sub-bands using a bank of analog bandpass filters. The filter outputs are sampled by ADCs at a fraction of the Nyquist rate. However, the need for the digital reconstruction of the signal before processing greatly increases the complexity of the system and hence power consumption.

The approaches described above do relax the requirements placed on the ADC but their real life performance is severely limited by ‘jitter’ which is also referred to as the uncertainty in the edges or the sampling instants. We know that the performance of sample hold circuits which are the basic building block of any converter define the systems performance. A known figure of merit of data converters states that the

bandwidth and precision of converters increases with decrease in the length of the devices. This pushes us to use lower technologies for high speed and high precision ADC's. Also the major issue with going multi-channel is mismatches between the paths which manifest in the output and significantly decrease the achievable resolutions. As we know any analog circuit is bugged with mismatches. There can be variety of issues which can cause mismatches in analog design, some of them being the threshold mismatches, temperature gradients along the die, linear gradient effects and lots of other effects. Most of the mismatches tend to increase with technology scaling which makes it all the more difficult to take proper advantage of technology scaling.

Innovative multi-channel ADC architectures that parallelize the process of sampling and thereby provide better resolution than the existing architectures are to be developed. Also techniques which can avoid or relax the problem of jitter have to be developed without increasing the complexity of the system. Nextly, appropriate techniques have to be developed either in the front end or in the digital background which can assist the 'dirty analog circuits' and enhance the performance of such multi-channel architectures in the presence of static gain and phase mismatches.

2. TRANSFORM DOMAIN RECEIVER

The basic principle of a Transform-Domain (TD) receiver [9] is to expand the signal over a basis set and operate on the basis co-efficients. An analog computation of the basis coefficients efficiently parallelizes the signal for digital processing, relaxing the sampling requirements and enabling parallel digital processing at a much lower rate.

When a large number of parallel paths are deployed in the test environment and each path is designated to expand the source signal over a single basis function, collaborative processing of the signals from each path in the receiver presents scalable bandwidths depending on the number of individual paths involved in the reception of the signal. Fig. 3 shows the transform domain receiver, it consists of a front end LNA which amplifies the input signal. This amplified signal is converted to current through a independent G_m stages and this current is now integrated on capacitors which effectively forms a *sinc* type of filter [9]-[12]. This *sinc* filtering not only provides anti aliasing but also samples the signal, more light will be thrown on *sinc* filters later. The samples are quantized and collected. These collected samples as we know are not representative of the time domain samples, therefore we need some kind of additional digital processing which can convert the samples collected to time domain samples and thereby reconstructing the time domain signal.

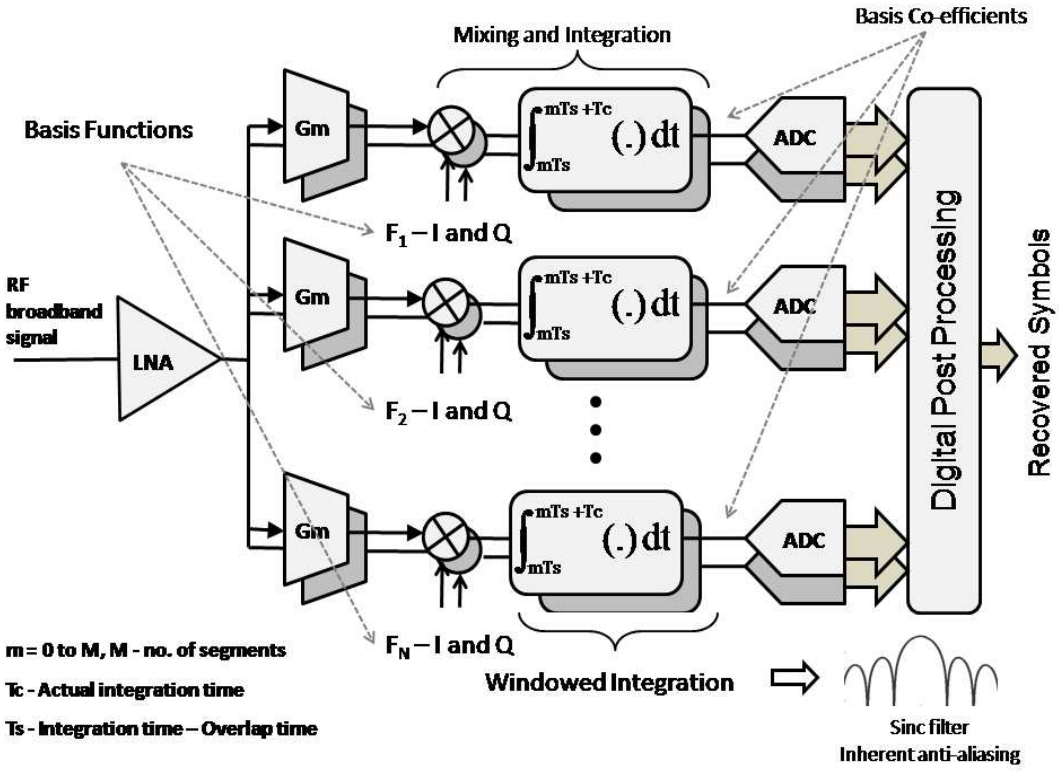

Fig. 3. Multi-Channel Transform Domain Receiver.

As a particular case we consider the system to be working on OFDM signals. This means the input signal will be data superimposed on practical carriers which are spaced in each channel of the multi-channel *sinc* filter bank, the input signal is mixed with a local-oscillator (LO) signal and integrated in a window of duration T_c seconds. The windows are overlapped by a small amount T_{ov}. The overlap is exploited to create a superior anti-aliasing filter while giving the required decimation [9].

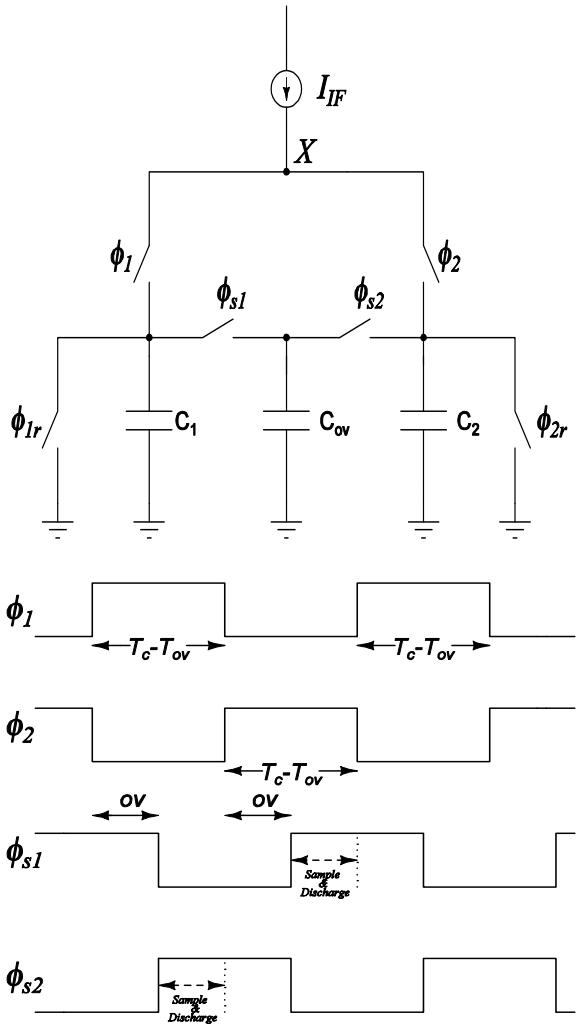

Fig. 4. *Sinc* Filter Used in the Receiver.

Fig. 4 shows the filter that was employed in the multi-channel receiver. It is modification of the general time interleaved *sinc* filter with a better anti aliasing capabilities. The clocks needed to operate this type filter are also shown. A brief operational theory behind the above overlap *sinc* filter can be initiated with the operation

of a generic *sinc* filter. We know that a generic filter has a transconductance stage (G_m) which converts the input voltage signal to a current signal and then this current is accumulated over a capacitor for a finite amount of time. This accumulation creates a *sinc* type of filter and if we have a sampled kind of operation we achieve sampling and anti aliasing in the same stage, a motivation for the usage of charge sampling filters. Similarly one can start analyzing the above filter by eliminating the overlap capacitor (C_{ov}) used, initially the current from the transconductance stage is pumped into a capacitor where charge accumulates for a finite amount of time and then it is read out, during the read out time of this capacitor the current is diverted for accumulation into another capacitor using proper clocks and switches. This creates an efficient combination of FIR filter and sampling operation. We know that the type of filter can achieve depends on the shape of the integration window. To achieve a better anti aliasing we would need a $sinc^2$ filter which has -40dB/decade out of band roll off. A sampled operation $sinc^2$ would mean that the integration window needs to be in triangular shape, we can try to reach a triangular type of integration window by weighting every sample in a particular fashion.

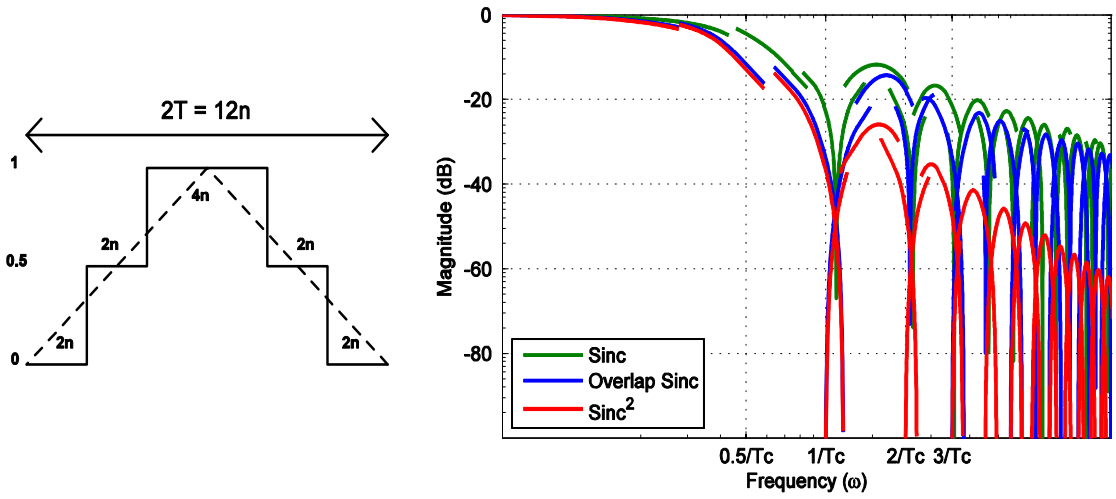

Fig. 5. Integration Window and Filter Response.

The simplest case of weighting would dividing the integration window into three parts in the ratios of 1:2:1. Such type of filter would approximate a *sinc*^{2} filter till the first null and would have a roll off slightly better than a normal *sinc* filter. Fig. 5 shows window shaping and filter response.

Assume there are *N* paths and in each path *M* samples are collected. The *M* overlapped windows that cover the entire signal block provide a total of *MN* samples $Y(m,n)\Big|_{m=0}^{M-1}\Big|_{n=0}^{N-1}$ given by,

$$Y_{m,n} = \int_{mT_S}^{mT_S+T_C} x(t)\Phi_n^*(t)\,dt \qquad (2)$$

where T_s=T_c - T_{ov}, $x(t)$ is the received signal, $\Phi_n(t)$ is the basis function onto which the input signal is expanded in the n^{th} path, m=0 to *M-1* indicates the m^{th} segment in each channel and n=0 to *N-1* refers to the n^{th} channel. Each channel operates only on a

fraction of the input signal bandwidth which relaxes the tracking bandwidth requirements for the ADC that quantizes the analog samples thus minimizing power consumption. These quantized samples are processed digitally to estimate the symbols directly using a least squares (LS) estimator.

The sampled data, given by (2), can be represented in the form of a vector *y* as shown below,

$$\bar{y} = [Y_{0,0}\ ,\ Y_{0,1}\ ,\ \ldots\ Y_{0,N-1}\ ,\ Y_{1,0}\ ,\ Y_{1,1}\ ,\ \ldots Y_{M-1,N-1}\ ]^T \tag{3}$$

Here $Y_{m,n}$ is a complex number representing both the in-phase and quadrature components, if the in-phase and quadrature components are represented separately in $\bar{y}$, then the size of $\bar{y}$ is $2NM\times 1$. The input signal is a multi-carrier OFDM signal with *K* sub-carriers and is given by the following expression,

$$x(t) = \mathrm{Re}\sum_{k=1}^{K}\left[a(k)e^{-j2\pi F_C(k)t}\right]$$

$$= \sum_{k=1}^{K}[a_i(k)\cos\cos\left(2\pi F_c(k)t\right) + a_q(k)\sin\sin\left(2\pi F_c(k)t\right)] \tag{4}$$

In the above expression, $a_i(k)$and $a_q(k)$ represent the in-phase and quadrature components of the data $a(k)$ modulated on the k^{th} sub-carrier. $F_c(k)$ corresponds to the carrier frequency of the k^{th} sub-carrier. The data that is modulated on all the sub-carriers can be represented in the vector form as shown below,

$$\left[a_i(0), a_q(0), a_i(1), a_q(1), \ldots . a_i(K), a_q(K)\right] \tag{5}$$

It can be seen that the entire system that generates the vector $\bar{y}$ from $\vec{a}$ can be represented by a linear matrix equation as,

$$G\vec{a} = \vec{y} \tag{6}$$

Each element in G corresponds to the integration of the k^{th} carrier (in-phase/quadrature) mixed with the n^{th} LO signal (in-phase/quadrature) observed at the end of the m^{th} segment. The elements in G are given by,

$$G_m(n_i, k_i) = \int_{mT_S}^{mT_S+T_C} \cos\left[2\pi F_c(k)t\right]\cos\left[2\pi f_{LO}(n)t\right]dt \tag{7}$$

where $f_{LO}(n)$ corresponds to the frequency of the n^{th} LO signal. The subscript i in $G_m(n_i, k_i)$ refers to the in-phase component. As the real and imaginary components of both the carrier and the LO signal are represented separately inside the matrix, G becomes a $2NM \times 2K$ matrix. The data $\vec{a}$ can be reconstructed from the received vector $\bar{y}$ using the LS estimator. If R is defined as the reconstruction matrix, the LS solution for the forward problem of (6) for the case when $NM >= K$ is given by [13] ,

$$R = (G^H G)^{-1} G^H \tag{8}$$

With the knowledge of the reconstruction matrix R and the received vector $\bar{y}$, the data transmitted can be estimated using the equation,

$$\vec{a} = R\vec{y} \tag{9}$$

3. COMPLETE SYSTEM CALIBRATION

3.1 Mismatches, Imperfections and Offsets in the System

The TD receiver has been modeled mathematically and a method for recovering the transmitted symbols has been outlined in the previous section. This was possible only because the transformation of the input symbols to the output collected samples is a linear operation, facilitating the mathematical modeling and the use of least squares solution. The main assumption behind this modeling was that there are no mismatches or non-idealities in the system and therefore the forward transformation matrix *G* makes an accurate representation of the system. In reality this is seldom the case since there are a lot of sources of error and non-idealities which make the forward transformation matrix G inaccurate. Since the forward transformation matrix itself has lot of errors, the inverse transformation matrix which is used to recover the symbols is also inaccurate and therefore the symbols recovered are erroneous. In order to improve the performance of the said receiver we need to accurately model the errors entering the system and also propose a method to reduce the same. To be able to model the errors various sources of the errors are identified.

There are several offsets and mismatches present in the transmitter, the channel and the receiver that deteriorate the system performance. There are different ways to compensate the errors that our system has been affected with. One key ingredient in building flexible radios is the efficient use of digital signal processing (DSP). DSP has been employed heavily in communication systems to counter the affect of various non-

idealities [14]-[20]. Various signal processing algorithms have been put to use in order to improve the performance of front ends and ADC's. We also adopt a DSP technique as a mean to relax the accuracy with which front ends need to be built, and thereby save considerably complexity and design time.

The affect of various non-idealities on different communication systems has been analyzed previously and mathematical models necessary to cancel them have been built [21]-[27]. But the classification of non-idealities has not been reported in the literature in the context of multi-channel receivers. Here we highlight the main non-idealities in a *sinc* filter bank based OFDM receiver. Fig. 6 gives a brief outline of all the mismatches that could be present in a multi-channel communication system. The major sources of error in a multi-channel receiver are the mismatches between the paths. Due to the random variations in threshold of transistors in each path, there is no proper matching between the gain input signal sees in each path. Apart from the threshold mismatches, there are other effects like leakage currents, voltage and temperature variations, process parameter variation on the die. All these mismatches severely effect the performance of the multi- channel receiver as they introduce a variable gain and phase offset between the paths. Also the multi-carrier signal generated by the IFFT block at the transmitter is modulated by a local oscillator signal to RF frequencies. Ideally, this LO frequency should be perfectly synchronized with the LO signal at the receiver. However, there will always be a small frequency offset between the two signal sources. The wireless channel between the transmitter and receiver introduces a gain and phase variation to each sub-carrier in the multi-carrier signal. A certain time delay for the input signal arriving at the

receiver introduces different initial phase-delays for each sub-carrier. The LNA and Gm stage could introduce gain and phase offsets as said above among the different paths primarily due to the variations in the process and imperfections in the implementation of each channel. There could be variations in the capacitors used in the charge sampling filter which would result in an additional gain error. If square LO signals are used for mixing, the waveform could have an exponential rise and decay due to the finite bandwidth of the circuit. Further, the LO signals are subject to frequency and phase offsets. However, this is avoided by generating all the LO signals and the sampling clocks from a single reference in the receiver.

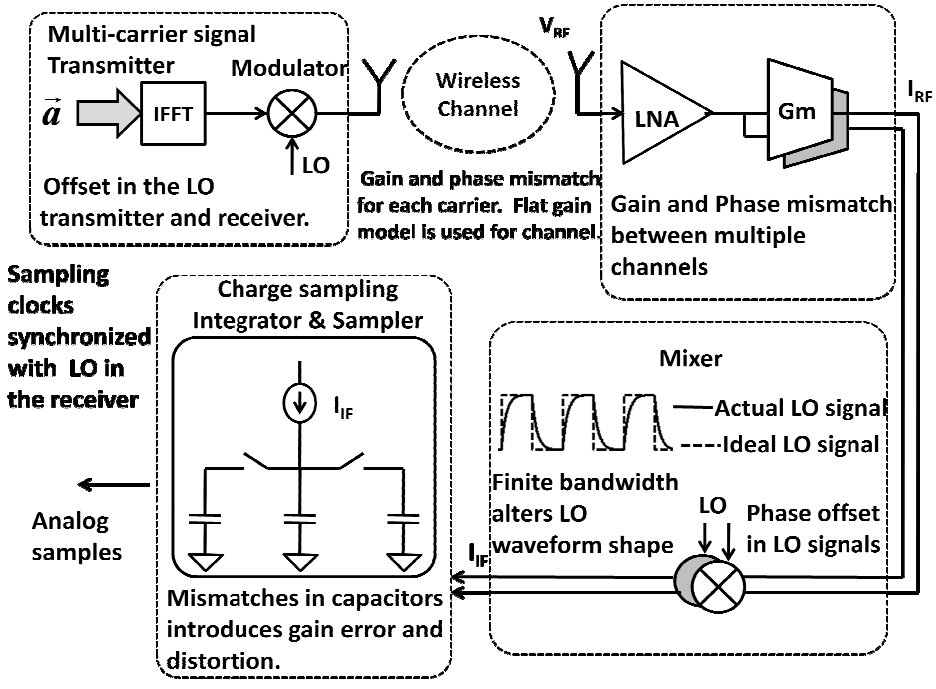

Fig. 6. Mismatches and Imperfections in a Typical Multi-Channel System.

In the presence of all these mismatches and offsets, it is clear that the *R* matrix defined earlier would be unable to detect the symbols, thus the need for a calibration technique to learn these mismatches and offsets.

3.2 Calibration Algorithm

In general whenever a calibration technique is to be applied to a system, the errors have to be completely identified and then their effect on the output has to be mathematically modeled. Once the errors effect on the output has been mathematically modeled, we can apply an inverse operation on the output to make it free from the error. In the case of our receiver instead of modeling each error separately, we employ a simpler approach to get rid of the errors. Since we know that the entire transformation the input symbols undergo can be mathematically represented in terms of a matrix *G*, if we can optimize this transformation matrix we can get rid of the errors and improve the receiver's performance.

In OFDM systems as we all know there is specific relation between the carrier spacing and the duration of the transmitted symbol. The signal for a particular pattern of transmitted symbols should be as wide as the inverse of the frequency spacing, if this condition is not satisfied there would permanent destructive interference between the carriers thereby leading to loss of transmitted data. Apart from this condition if there is any offset in the frequency of the modulating carrier wave, it would create a time varying error to be introduced into the system as the phase of the signal keeps accumulating with time.

Since the frequency offset causes the symbols to rotate periodically, in the presence of the frequency offset it is extremely difficult to apply any optimization algorithm to optimize the transformation matrix as the frequency offset introduces a time varying error and it is difficult to correct for such an errors with adaptive algorithms are most of them deal with minimizing static errors. Several techniques have been proposed to estimate the frequency offset in OFDM systems. Initially the frequency offset in the LOs at the transmitter and receiver is estimated using a maximum-likelihood estimator which is explained below.

The front end *sinc* filter bank structure as seen in the following discussion, allows the frequency offset to be factored out from the received signal $\bar{y}$ despite the presence of several mismatches.

The expression for the sampled data, $Y(m,n)\Big|_{m=0}^{M-1}\Big|_{n=0}^{N-1}$, is defined in (2) and is re-written here for convenience.

$$Y_{m,n} = \int_{mT_S}^{mT_S+T_C} x(t)\Phi_n^*(t)\,dt \tag{10}$$

Here L represents the block number. $\Phi_n(t)$ is the n^{th} LO signal in the multi-channel receiver and combining the in-phase and quadrature components, it can be represented as follows, LO being a square wave it contains all the odd harmonics till infinity,

$$\Phi_n(t) = e^{-j\left[2\pi f_{lo}(n)t+\Phi_{LO}(n)\right]} - \frac{1}{3}e^{-j3*\left[2\pi f_{lo}(n)t+\Phi_{LO}(n)\right]} + \frac{1}{5}e^{-j5*\left[2\pi f_{lo}(n)t+\Phi_{LO}(n)\right]} \tag{11}$$

where $x_L(t)$ is the input multi-carrier signal corresponding to the L^{th} block and is given by,

$$x_L(t) = \mathrm{Re}\left\{\sum_{k=1}^{K} a e^{-j2\pi F_c^{'}(k)t + \Phi_c(k) + 2\pi\Delta F_c(L-1)T}\right\} \tag{12}$$

where $F_c^{'}(k) = F_c(k) + \Delta F_c$, ΔF_c is the carrier frequency offset, $\Phi_c(k)$ is the initial phase offset of carrier k and $2\pi\Delta F_c(L-1)T$ is the accumulating phase offset in block L that results from ΔF_c. Substituting (11) and (12) in (10),

$$Y_{m,n,L} = A_n e^{j\Theta_n} \int_{mT_S+\Delta T}^{mT_S+T_C+\Delta T} \left[\mathrm{Re}\sum_{k=1}^{K} a e^{-j2\pi F_c^{'}(k)t + \Phi_c(k) + 2\pi\Delta F_c(L-1)T}\right] \times [e^{-j\left[2\pi f_{lo}(n)t + \Phi_{LO}(n)\right]} - .....] \tag{13}$$

where $A_n e^{j\Theta_n}$ is the lumped complex constant representing the gain and phase mismatch in the nth channel. $\Phi_{LO}(n)$ is the initial phase offset in the n^{th} LO signal and ΔT is the offset in the integration window. The offset in the integration window, ΔT, can be brought inside the integration as a phase offset in the signals. $\Phi^{'}{}_c(k)$ and $\Phi^{'}{}_{LO}(n)$ are defined as follows,

$$\Phi_c^{'}(k) = \Phi_c(k) + 2\pi F_c^{'}(k)\Delta T + 2\pi\Delta F_c(L-1)T \tag{14}$$

$$\Phi_{LO}^{'}(n) = \Phi_{LO}(n) + 2\pi f_{LO}(n)\Delta T \tag{15}$$

Incorporating the above equations, (13) becomes,

$$Y_{m,n,L} = A_n e^{j\Theta_n} \int_{mT_S}^{mT_S+T_C} \left[\mathrm{Re}\sum_{k=1}^{K} a e^{-j2\pi F_c^{'}(k)t + \Phi_c^{'}(k)}\right] \times [e^{-j\left[2\pi f_{lo}(n)t + \Phi_{LO}^{'}(n)\right]} - .....] \tag{16}$$

The term inside the integral contains tones at several frequencies including the desired tone at $f_{LO}(n)-F_c^{'}(k)$ and higher order harmonics at $f_{LO}(n)+F_c^{'}(k)$, $3f_{LO}(n)\pm F_c^{'}(k)$ and so on. However, the charge sampling *sinc* filter attenuates these high frequency tones. The phase term $\Phi_c^{'}(k)$ is expanded and $e^{2\pi j\Delta F_c(L-1)T}$, is factored out and further simplification of the above expressions is done to get the following expression,

$$Y_{m,n,L}=e^{2\pi j\Delta F_c(L-1)T}A_n e^{j\Theta_n}\int_{mT_S}^{mT_S+T_C}\sum_{k=1}^{K}[\frac{a_i(k)}{2}+\frac{a_q(k)}{2j}]e^{j[2\pi F_c^{'}(k)t+\Phi_c(k)+2\pi F_c^{'}(k)\Delta T-2\pi f_{LO}(n)t+\Phi_{LO}^{'}(n)]}dt \tag{17}$$

If it is assumed that the same data set is transmitted in successive blocks, it can be noticed that the only term that will vary in $Y_{m,n,L}$ is the term outside the integral. Fig.7 shows one element of the vector *Y* when the same data is transmitted every time. We can notice that the element varies sinusoidally from block to block.

The simplest way to remove this error is by estimating the frequency of this sinusoid and multiplying the output data with the inverse sinusoid which would remove the time varying nature of the data. In order to estimate the frequency of the sinusoid we employ the following method,

Let $Y_{m,n,L}=\alpha_{m,n}e^{j\beta_{m,n}}$, then $Y_{m,n,L+1}$ is given by,

$$Y_{m,n,L+1}=e^{2\pi j\Delta F_c T}\times\alpha_{m,n}e^{j\beta_{m,n}} \tag{18}$$

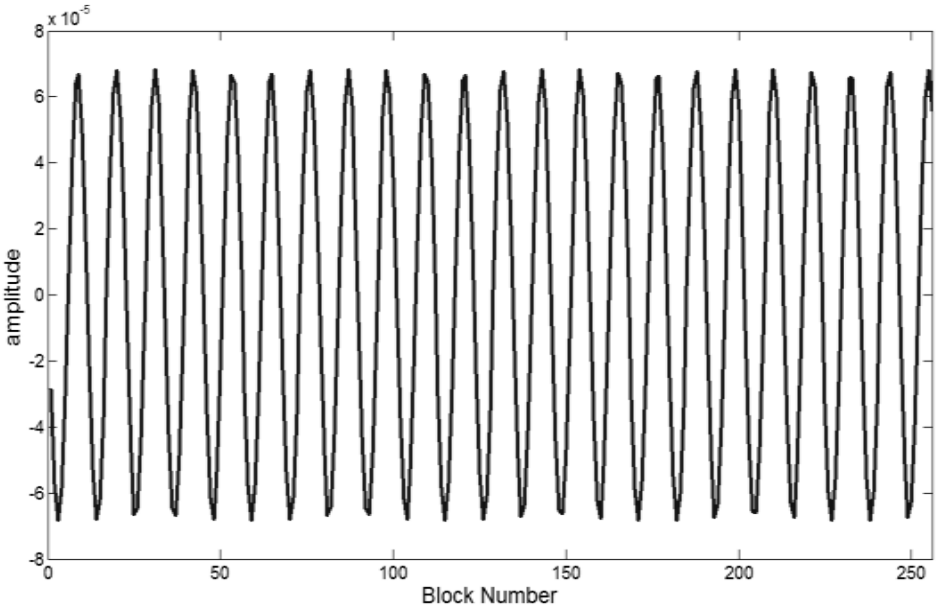

Fig. 7. Sampled Values Varying Sinusoidally due to Frequency Offset.

From (18), it is clear that the offset in frequency can be factored out and this facilitates the use of Maximum Likelihood (ML) to estimate the frequency offset in the OFDM case. The ML estimate of ΔF_c is obtained by taking mean of the argument over B consecutive blocks and is given by,

$$\Delta F_c = \frac{1}{2\pi T}\tan^{-1}[\sum_{L=1}^{B} Im(Y_{m,n,L+1}Y_{m,n,L}^{*}) / \tan^{-1}[\sum_{L=1}^{B} Im(Y_{m,n,L+1}Y_{m,n,L}^{*}) / \sum_{L=1}^{B} \mathrm{Re}\left(Y_{m,n,L+1}Y_{m,n,L}^{*}\right)] \tag{19}$$

The choice of B depends on the noise present in the system and the desired accuracy of estimate. This estimate of the frequency offset ΔF_c is used to make a correction in the received vector $\bar{y}_L$. The corrected vector $\bar{y}_L(update)$ is given by,

$$y_L\left(update\right) = y_L e^{-j2\pi\Delta F_C(L-1)T} \tag{20}$$

Now once we have corrected for the time varying error caused by the frequency offset, we can go for use of any conventional adaptive algorithm to optimize the forward or inverse transformation matrix and thereby correcting for the static offsets and non-idealities present in the system. The adaptive algorithm we chose for this purpose is the least mean squares (LMS). LMS algorithm based calibration has been employed in many receivers to assist the non-ideal analog front-end to their simplicity and robustness [28]-[29].

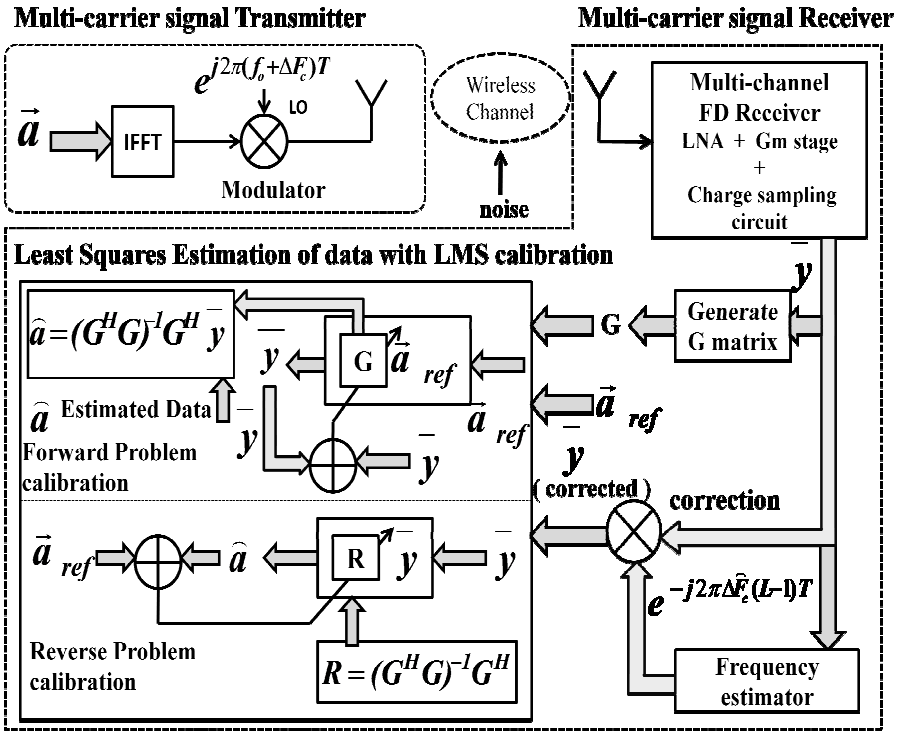

Fig. 8. Complete Multi-Channel Receiver System with Offset Correction.

We have used the normalized least mean squares (NLMS) algorithm, as its convergence speed is potentially superior to that of LMS [30] and is also much less sensitive to the properties of the input signal than are those of LMS indicating more predictable behavior over a wide range of conditions. Once the frequency offset in the carriers is estimated, the problem is reduced to calibration of static mismatches and offsets in a communication system. Fig. 8 shows the complete system calibration we have adopted.

The equation for the estimation of the transmitted data $\hat{a}$, is given by,

$$\vec{a} = R\vec{y}$$

$$= (G^H G)^{-1} G^H \vec{y} \qquad (21)$$

where R is the least squares solution of the system and $\vec{y}$ contains the sampled output. For the best performance the matrix R must match the actual circuit implementation of the system perfectly.

An intuitive way of understanding these equations from the perspective of adaptive algorithms is by viewing them graphically. In the entire process of this optimization what we actually want is a way to represent the transformation the input symbols undergo from the input to the output *i.e.* we want to identify the system that is actually transforming the symbols to received samples. This is similar to the system identification problem in signal processing areas. Fig. 9 shows such a system identification system.

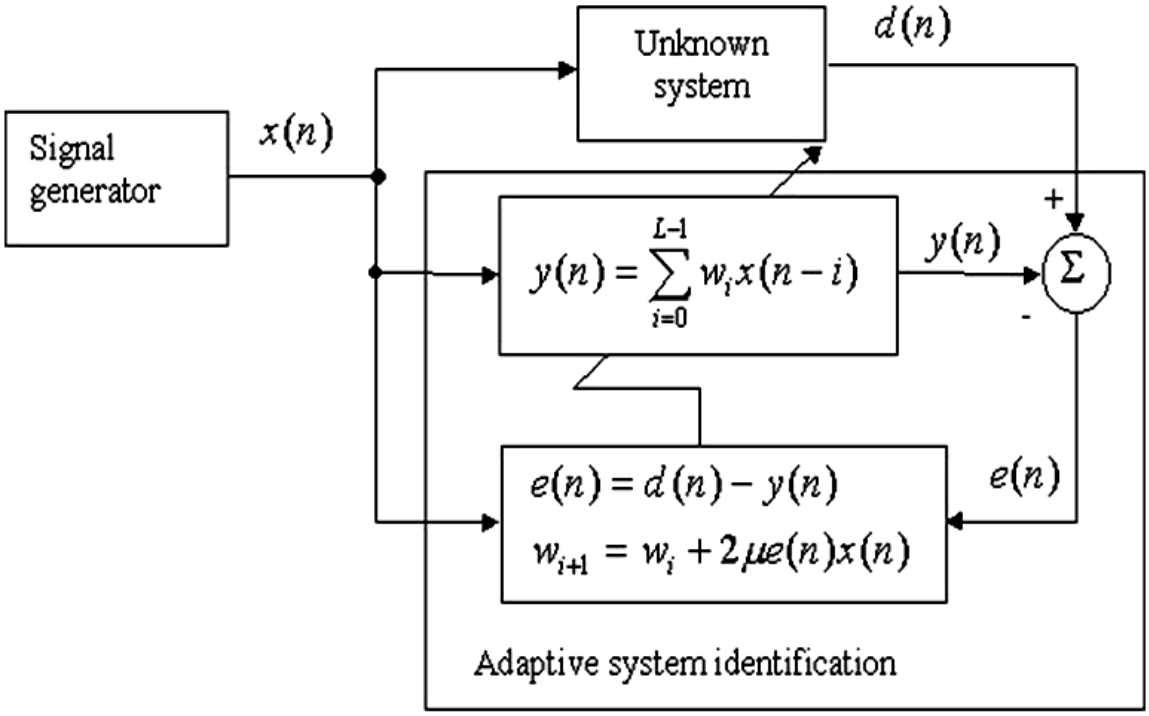

Fig. 9. System Identification Algorithm.

In system identification problem the system is modeled in terms of weights and these weights are trained according to the error. Fig. 9 shows the basic algorithm of any system identification problem. The only difference from one problem to another will be the algorithm used to minimize the error and optimize the system weights. As we have explained previously we are trying to represent our system in terms of a matrix *G*. The system is actually nothing but a two dimensional set of weights defining the multi-channel receiver system.

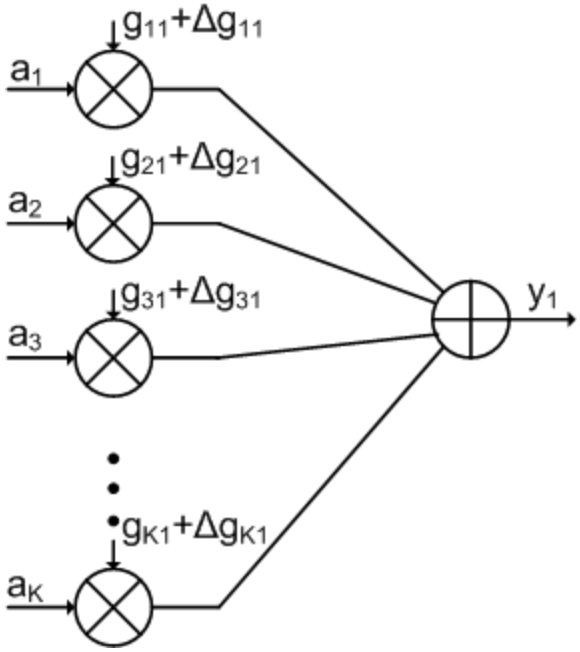

Fig. 10. Graphical Representation of a Row of *G* Matrix.

Fig. 10 shows a graphical representation of the forward transformation matrix. Similarly a representation for the inverse transformation matrix can be formed too. As we see from the figure each output sample is a weighted sum of all the input symbols. In order to accurately identify the receiver system we need to find the accurate weights transforming the input to output.

Fig. 8 illustrated two techniques to identify the transformation system accurately. The first method involves calibration of the *G* matrix or the forward weights (forward problem) and in the second method, the *R* matrix or the inverse weights is calibrated (reverse problem). The normalized least mean squares (NLMS) algorithm is used for

calibration in both techniques. The update equation for the *R* matrix in the reverse problem calibration is based on the normalized LMS algorithm and is given by

$$R(L+1) = R(L) + \vec{e_a}(\mathrm{L}) * \frac{\vec{y}}{\| \mathrm{y} \|^2}$$

where $\vec{e_a}$ is the error in $\vec{a}$. It is shown that updating the forward matrix gives savings, so the LMS update is applied to *G* matrix by considering the forward problem $\vec{y} = G\vec{a}$,

$$G(L+1) = G(L) + \vec{e_y}(L) * \frac{\vec{a}}{\| \mathrm{a} \|^2} \tag{22}$$

where $\vec{e_y}$ is the error in $\vec{y}$.

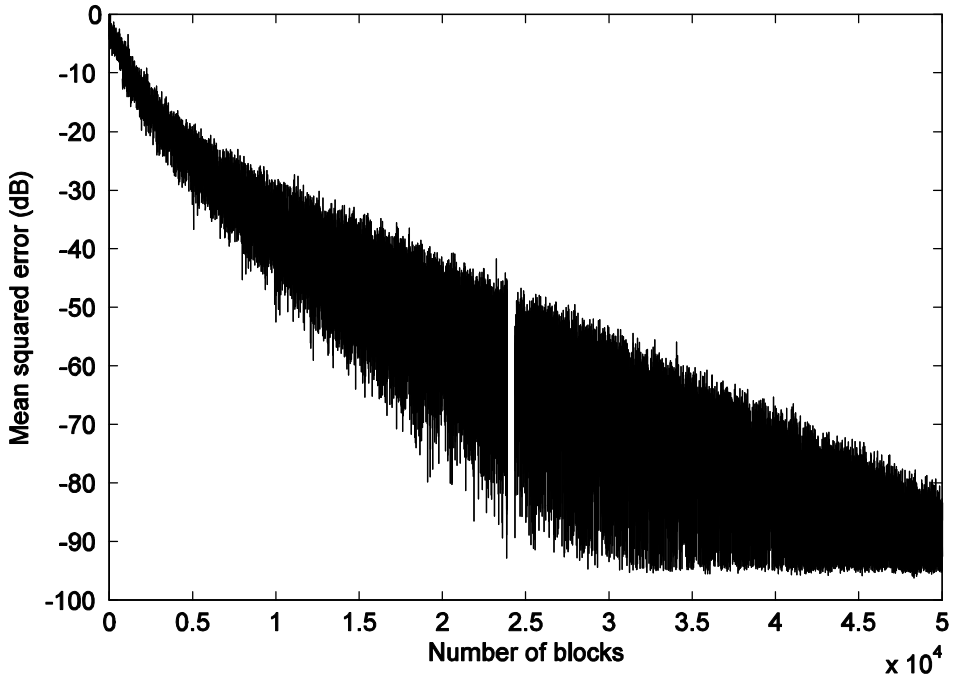

Fig. 11. Convergence of the LMS Algorithm with a Random Initial G Matrix Estimate.

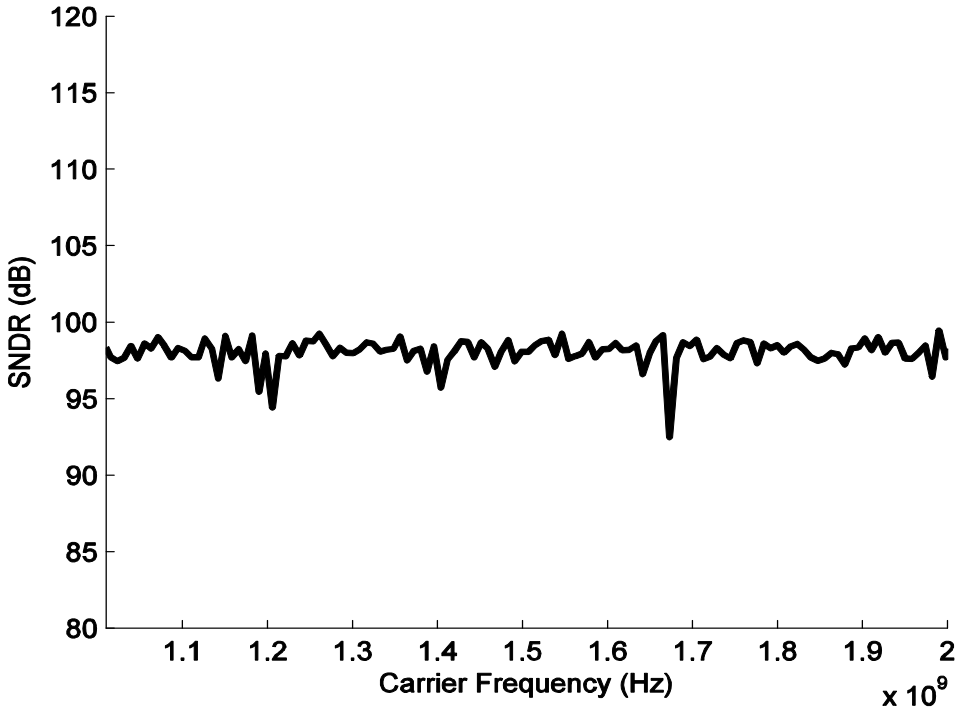

Fig. 12. SNDR after Signal Reconstruction.

From the updated values of G matrix, $(G^H G)^{-1}$ and $G^H G$ are computed for the next block. The NLMS algorithm tracks the system mismatches and over a period of time converges to the ideal solution. The two techniques of calibration are similar from a performance point of view.

3.3 Matrix Initialization

The update equations (11) and (12) need an initial estimate *R(0)* and *G(0)*, choosing an arbitrary *R* matrix could result in slow convergence as shown in Fig. 11 Though we are able to achieve good resolution at the output after the algorithm converges as seen Fig. 12 shows that the number of iterations required is around 50000,

which means a huge wastage of computational power. There is a need to start the LMS calibration with an initial *R* matrix that is close to the desired solution. The linear matrix equation that represents the forward problem is given by (7).

The mathematical model for the forward matrix can be used to form the initial estimate for *R* matrix according to (8), but as shown in Fig. 11 a large number of iterations are required for this matrix to converge. Since performing so many iterations in real time on hardware is improbable, we go for scanning of carries for forming the initial estimate of *R* matrix. Since we know that each output sample collected is a weighted sum of all the input symbols, we can directly get the value of each weight by sending a particular input pattern.

If the transmitted data $\vec{a}$ is given by $\vec{a}$ = [1000…..], then the received vector $\bar{y}$ is the first column of matrix *G* along with a noise term. The transmitted vector $\vec{a}$ is repeated in sequence [1000…..], [0100…..], [00100…..] and so on, to compute each column of the *G* matrix. After traversing through all the elements of $\vec{a}$, the entire *G* matrix is formed. From the *G* matrix, $(G^H G)^{-1}$ and G^H are computed which are used for symbol detection based on the LS estimate (9). Fig. 13 shows the initialization and training procedures. However, this does not represent the ideal solution because the $\bar{y}$ vector is contaminated by the noise present in the circuit. Using this *G* matrix as the initial starting point LMS algorithm can be used to quickly converge to the ideal solution. It appears that the drawback of this method is that an inverse operation $(G^H G)^{-1}$ needs to be performed. However, the sparsity of the $G^H G$ matrix is exploited to drastically reduce the complexity of inverse computation.

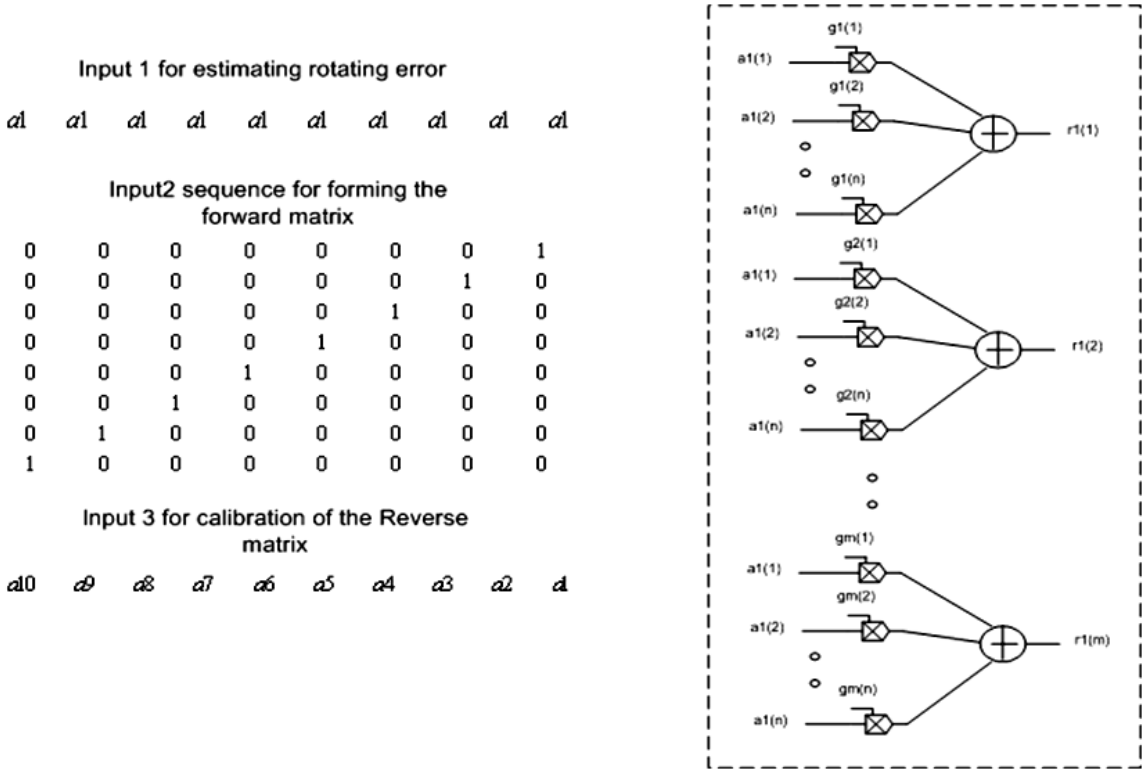

Fig. 13. Matrix Initialization.

Fig. 14 shows the error and the output SNR achieved when the above matrix initialization procedure is adopted instead of using the mathematical model as the initial estimate for the *R* matrix. We see that the number of iterations required is drastically reduced and the matrix initialization procedure now makes it feasible for the implementation of this system on hardware with minimum processing and memory capabilities.

Simulation results are presented to show LMS calibration and frequency offset estimation of the system. A system model is created in *MATLAB*. The input to the

system is a QPSK modulated signal of 128 carriers with bandwidth of 1GHz from 1-2GHz. The receiver model used in this example has 5 parallel I & Q channels. The frequencies of the mixing signals (I & Q) used in each channel are chosen such that they are uniformly spaced around the center frequency of 1.5GHz and also are orthogonal to each other in a signal block of duration *T*.

The output of the mixer is integrated over a time window of duration 6ns. The integrated outputs are processed digitally to recover the data. An overlap of 2ns is introduced in between the integration windows. So, the effective time duration between samples is 4ns i.e. the sampling frequency is 250MHz. The detection of the symbols is carried out using the Lease Squares estimator. *AWGN* noise is added to the input signal such that the SNR = 100dB. The system mismatches and offsets discussed earlier are introduced in this model. There is a random delay ΔT in the arrival of the signal block. Each sub-carrier '*k*' has a random initial phase offset. Each channel has a random gain and phase mismatch $A_n e^{j\Theta_n}$. All the in-phase and quadrature LO signals have a random initial phase offset. A finite rise and fall time is introduced in all the clocks including the LO signals.

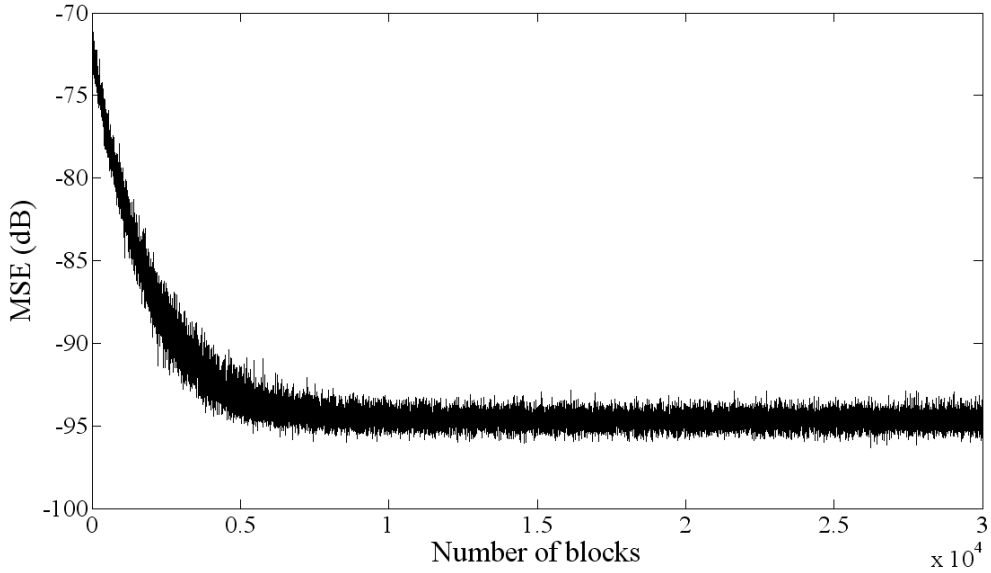

Fig. 14. Convergence of the MSE with Initial *R* Matrix Initialized through Training.

It is assumed that the LO signals and the sampling clocks are aligned as they are generated from a single reference source. The initial *R* matrix is formed by the matrix initialization technique described. Fig. 14 shows variation of mean square error versus iterations and Fig. 15 shows the SNDR across the sub-carriers after convergence is achieved. SNDR here implies ratio of the signal power to the total error on each sub-carrier due to noise and other residual non-idealities after calibration. As expected the LMS algorithm could calibrate all the static mismatches and the mean SNDR across carriers is close to the input signal SNR of 100dB.

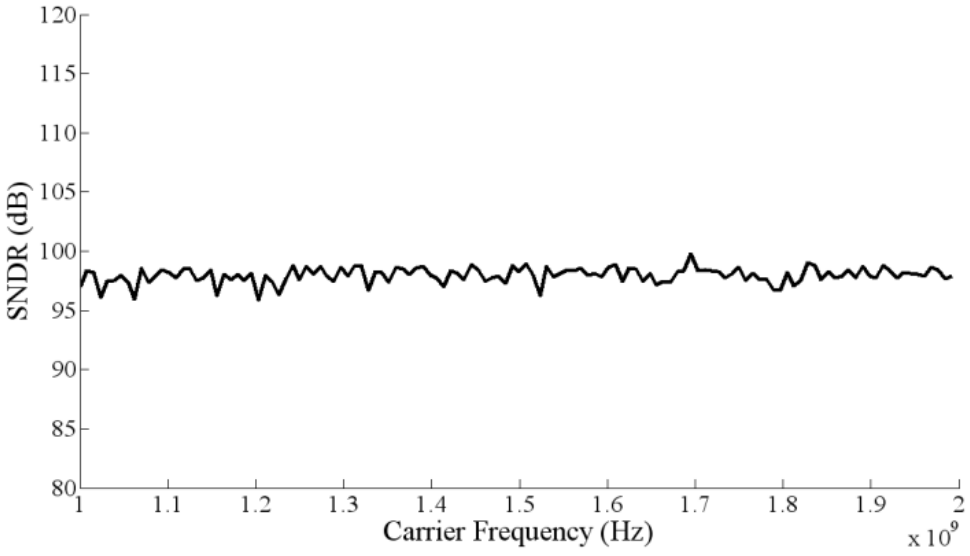

Fig. 15. Receiver Performance Post LMS Calibration with Trained Initial Estimate.

Further, when the SNDR is better than 20dB, data transmission can be started and in the background LMS calibration can be continued by taking hard decisions on the received data and computing the error. This is possible because for an SNDR greater than 20dB, the bit-error-rate (BER) is low enough to calibrate in a blind fashion. In the case of noisy channels, the SNR of the input signal is limited by the disturbances added to the signal. The convergence of the LMS algorithm is verified for the case of noisy channels. Post convergence the SNDR is expected to reach the input SNR of the signal which is clearly evident in the following figures. Simulation results for two different cases are provided in Fig. 16 and Fig. 17. In each case the output SNDR approaches the input SNR and the corresponding convergence of the LMS algorithm has been provided.

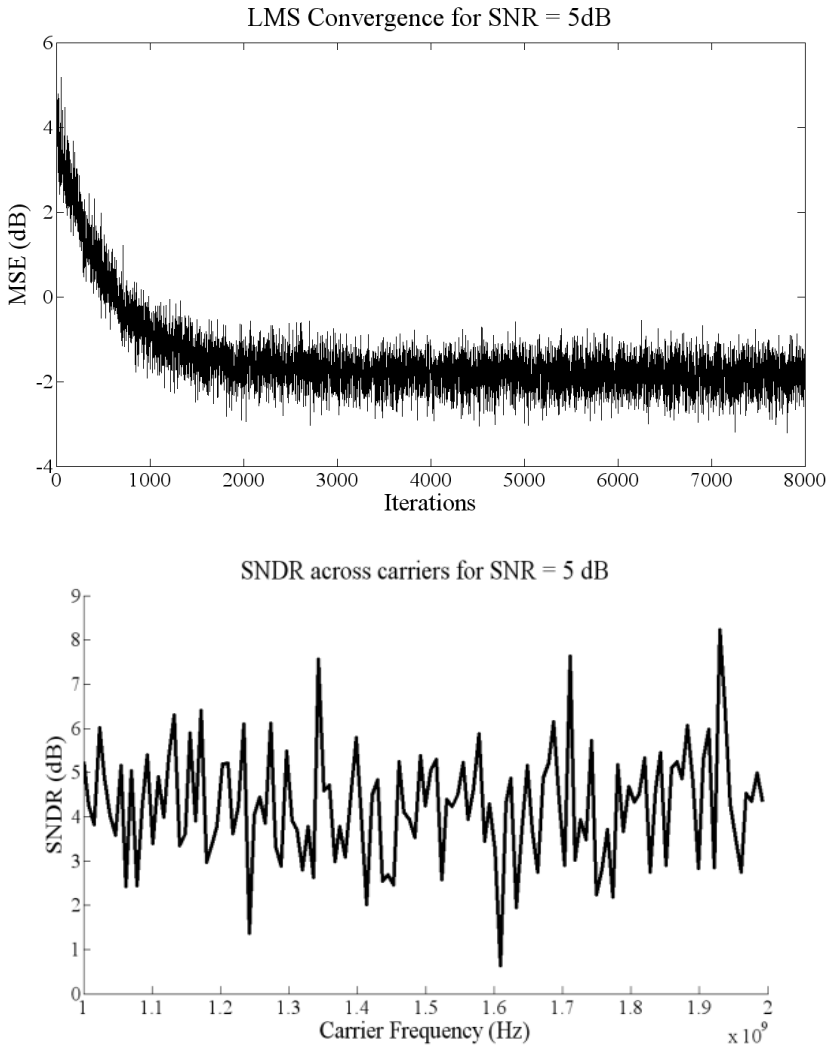

Fig. 16. LMS Convergence for SNR =5dB.

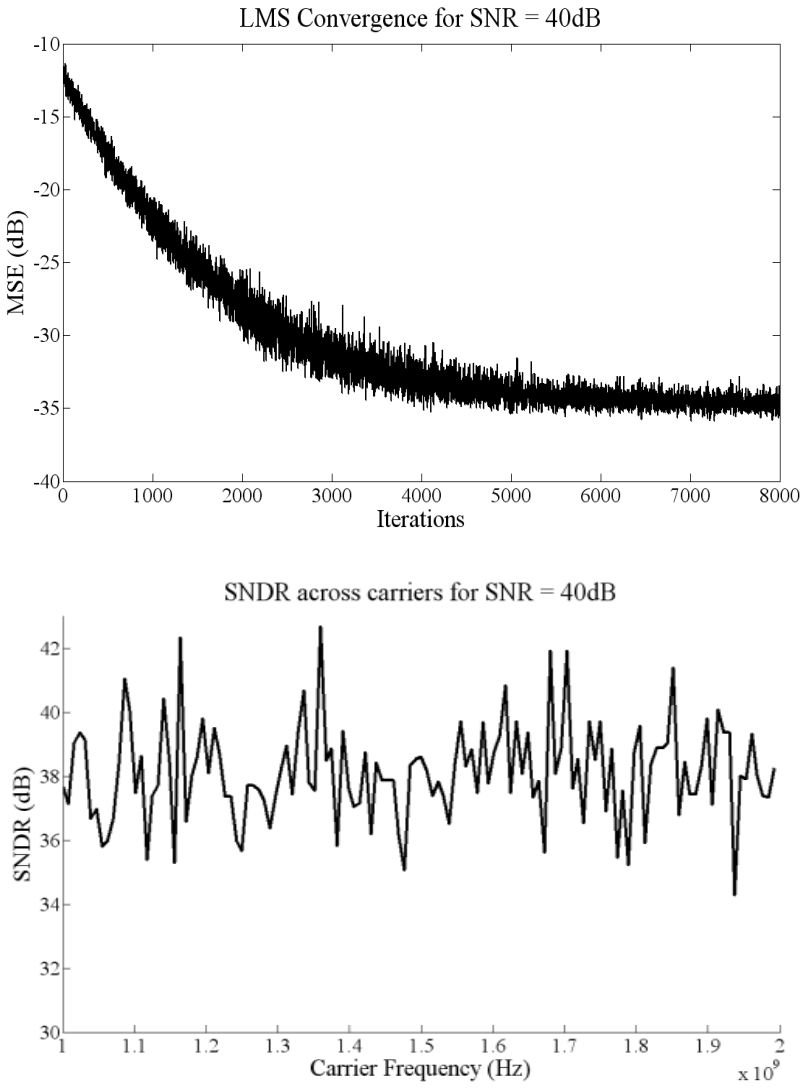

Fig. 17. LMS Convergence for SNR =40dB.

3.4 Digital Complexity Analysis

An analysis is presented on the computational complexity in the digital processing block of the multi-channel *sinc* filter bank. The whole analysis is centered on the sparsity of the $G^H G$ matrix which is exploited to drastically reduce the complexity of symbol estimation.

The first step is to analyze the complexity of the symbol estimation which is given by $\vec{a} = R\vec{y}$. Using the least squares solution for R $\vec{a} = (G^H G)^{-1} G^H \vec{y}$. This computation is decomposed into two steps, which reduces complexity. First $\vec{p} = G^H \vec{y}$ is obtained, and then $\vec{a} = (G^H G)^{-1} \vec{p}$ is used to estimate the symbols. In obtaining $\vec{p}$, the complex representations are retained for *G* and *y* for clarity in the analysis. The resultant complex $\vec{p}$ can be expanded to contain only real values and used in the second step. In this discussion, it is assumed that frequency offset in the carriers has already been corrected. The other static offsets and mismatches are also omitted for sake of clarity, however, including them does not alter the analysis. Each element in *G* is given by,

$$G_m(n,k) = \int_{mT_s}^{mT_s+T_c} e^{-j2\pi F_c(k)t} \Phi_n(t)\, dt$$

$$= e^{-j2\pi F_c(k) mT_s} \int_0^{T_c} e^{-j2\pi F_c(k)t} \Phi_{m,n}(t) dt \qquad (23)$$

where $\Phi_{m,n}(t)$ is the *m*th segment of $\Phi_n(t)$. Without loss of generality, the LO signals $f_{LO}(n)$ can be chosen such that $f_{LO}(n)T_s$ is an integer which means the basis functions

$\Phi_n(t)$ are periodic with respect to T_S. So $\Phi_{m,n}(t)$ is a periodic repetition of $\Phi_{0,n}(t)$ and (23) becomes,

$$G_m(n,k) = e^{-j2\pi F_c(k)mT_s} \int_0^{T_c} e^{-j2\pi F_c(k)t} \Phi_{0,n}(t)dt$$

$$= e^{-j2\pi F_c(k)t} Q_{k,n} \tag{24}$$

where $Q_{k,n} = \int_0^{T_c} e^{-j2\pi F_c(k)t} \Phi_{0,n}(t)\,dt$. The carrier frequency is given by, $F_c(k) = F_0 + k/T$

where $F_0 T_s$ is an integer and since $MT_s = T$, $e^{-j2\pi F_c(k)mT_s} = e^{-j2\pi km/M}$ and hence (24) becomes,

$$G_m(n,k) = e^{-j2\pi km/M} Q_{k,n} \tag{25}$$

Using (23) each element of $\vec{p}$ can be written as,

$$p_k = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} G^*_{m,n,k} Y_{m,n}$$

$$= \sum_{n=0}^{N-1} Q^*_{k,n} \sum_{m=0}^{M-1} Y_{m,n} e^{j2\pi km/M}$$

$$= \sum_{n=0}^{N-1} Q^*_{k,n} T_{k,n} \tag{26}$$

$T_{k,n}$ in (26) is periodic in *k* with a period *M*, and similar to an *M* point FFT, the complexity of computation of the complete $T_{k,n}$ is *o*(*NMlogM*). The total complexity of computation of $\vec{p}$ includes an additional *NK* multiplications and is given by *o*(*NMlogM*)+*o*(*NK*). However, this involved all complex multiplications and taking into account the fact that each complex multiplication involves 4 real multiplications, the

complexity of computation of $\vec{p}$ is $o(4S(N+logM))$. Next step is to determine the complexity of $(G^H G)^{-1}\vec{p}$ It can easily shown that $G^H G$ is a sparse matrix with only $2N$ non-zero elements in each row. It can be seen that the inverse of $G^H G$ is also a sparse matrix. Fig. 18 and Fig. 19 reflect the sparsity of the matrices. So, the complexity of $(G^H G)^{-1}\vec{p}$ is $o(2N*2K)=o(4NK)$. It is to be noted that all computations in this step are real multiplications and used in this step is expanded to contain only real terms. Putting it all together, the total complexity of symbol estimation $\hat{a}=Ry$ is $o(4K(N+logM))+o(4NK)$.

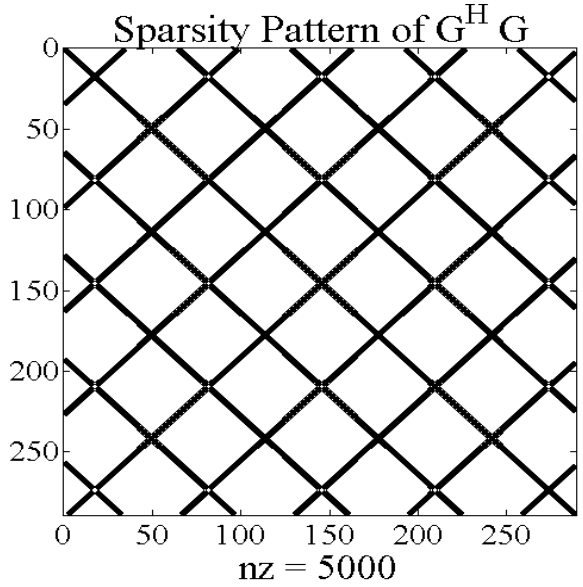

Fig. 18. Sparsity Pattern of G^H G.

It must be noted that the simplification in (23) is possible due to the reset in integration windows in charge sampling circuits. In the case of multi-channel analog filter banks (such as integrators without reset), the complexity of symbol detection for the same specifications is $o(4NMK)$.

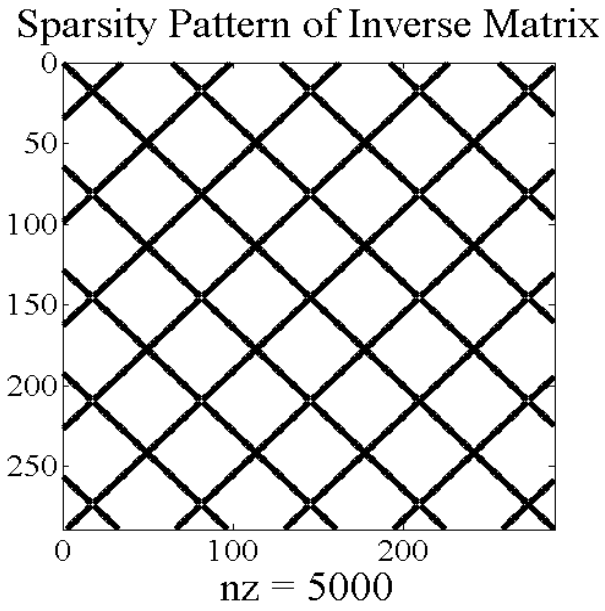

Fig. 19. Sparsity Pattern of $(G^H G)^{-1}$.

The multi-carrier example described is considered to compare the complexity of LS estimate of a multi-channel receiver with *sinc* and analog filter banks and the conventional FFT used in OFDM receivers. The complexity of an K point FFT in terms of real multiplications it is $o(4KlogK)$.

In this example, N=5,M=32 and K=128,

Complexity of FFT: $o(4Klog128)=o(28K)$

Complexity of LS estimate :

Sinc filter bank: $o(4K(5+log32))+o(20K)=o(60K)$

Analog filter bank: $o(4NMK)=o(4*160K)=o(640K)$

It can be seen that in the case of the *sinc* filter bank, the complexity of symbol detection is only marginally higher than the conventional FFT. However, in the case of the analog filter bank, the complexity of detection is significantly higher than the FFT. Next, the complexity of symbol detection for the *sinc* filter bank in the calibration phase is compared for the forward problem and reverse problem calibration scenarios. In the forward problem calibration, the *G* matrix is updated after each block. In the case of reverse problem calibration, the *R* matrix is updated for every block. Considering the above example, the complexity of symbol detection in the calibration mode for the two cases is as shown below: Complexity of LS estimate (calibration phase)

Forward Problem: $o(400K)+o(40K)+o(20K)=o(460K)$

Reverse Problem: $o(4NMK)=o(640K)$

It can be seen that there is a reduction in complexity when using the forward problem calibration compared to the reverse problem calibration. Table 1 summarizes the complexity analysis of the *sinc* filter bank and the analog filter bank.

Table 1: Comparison between Analog and *Sinc* Filter Bank.

	Sinc Filter Bank	Analog Filter Bank
Analog front end complexity	Filter is easily reconfigurable	Filter is not reconfigurable
Analog power consumption	Less	High
Digital Complexity (Estimation)	$o(4K(N+\log M)) + o(4NK)$ Ex: $o(60K)$	$o(4NMK)$ Ex: $o(640K)$
Digital Complexity (Calibration)	$o(16N^2K) + o(4K(1+\log M)) + o(4NK)$ Ex: o(460K)	$o(4NMK)$ Ex: o(640K)
Digital Power Consumption	Significant power reduction	10 times more power than *sinc* filter

4. JITTER TOLERANT MULTI-CHANNEL ADC

Timing jitter is the unwelcome companion of all electrical systems that use voltage transitions to represent timing information. Historically, electrical systems have lessened the ill effects of timing jitter (or, simply “jitter”) by employing relatively low signaling rates. As a consequence, jitter-induced errors have been small when compared with the time intervals that they corrupt. The timing margins associated with today’s high-speed communication systems and data links reveal that a tighter control of jitter is needed throughout the system design. As signaling rates climb above 2 GHz and voltage swings shrink to conserve power, the timing jitter in a system becomes a significant percentage of the signaling interval. Under these circumstances, jitter becomes a fundamental performance limit.

The total jitter (TJ) is separated into two categories, random jitter (RJ) and deterministic jitter (DJ). The deterministic jitter is further subdivided into several other sub-categories which is avoided in this discussion of jitter the reason for which will evident in following paragraphs.

Random jitter is timing noise that cannot be predicted, because it has no discernable pattern. A classic example of random noise is the sound that is heard when a radio receiver is tuned to an inactive carrier frequency. While a random process can, in theory, have any probability distribution, random jitter is assumed to have a Gaussian distribution for the purpose of the jitter model. One reason for this is that the primary source of random noise in many electrical circuits is thermal noise (also called Johnson

noise or shot noise), which is known to have a Gaussian distribution. Another, more fundamental reason is that the composite effect of many uncorrelated noise sources, no matter what the distributions of the individual sources, approaches a Gaussian distribution according, to the central limit theorem. The Gaussian distribution, also known as the normal distribution, has a PDF that is described by the familiar bell curve. For a Gaussian variable, the peak value that it might attain is infinite. That is, although most samples of this random variable will be clustered around its mean value, any particular sample could, in theory, differ from that mean by an arbitrarily large amount. So, there is no bounded peak-to-peak value for the underlying distribution. The more samples one takes of such a distribution, the larger the measured peak-to-peak value will be. Frequently, efforts are made to characterize such a distribution by sampling it some large number of times and recording the peak-to-peak value that results. One should use caution with this approach. The peak-to-peak value of a set of N observations of a random variable is itself a random variable, albeit one with a lower standard deviation.

Using such a random variable as a pass-fail criterion for quality screening, for example, requires that the pass threshold be raised to account for the uncertainty in the measurement, resulting in some acceptable units being failed. In most of the simulations we use the Signal to Noise distortion ratio as the parameter to gauge the performance of the systems in presence of jitter. Though this may seem to be faulty since the error added due to random jitter is unbounded, in reality the error added can still be defined statistically similar to the other noise sources we know and therefore signal to noise ratio holds credibility as long as the number of data blocks under test is sufficiently high. We

ensure this by running montecarlo simulations wherein we simulate the system for hundreds of data blocks and average the SNR performance of the system over all the blocks.

Deterministic jitter is timing jitter that is repeatable and predictable. Because of this, the peak-to-peak value of this jitter is bounded, and the bounds can usually be observed or predicted with high confidence based on a reasonably low number of observations. This category of jitter is further subdivided into categories like periodic jitter, duty cycle jitter etc. In any case the name itself implies this kind of jitter can be determined and when the sources of the jitter are determined, appropriate measures can be taken to reduce the effect of error added due to such jitter. For example, the sampling clock could be modulated by a sine wave interference from the power supply, this is a kind of deterministic jitter. By theory we know the frequency of such an interferer and by placing a decoupling capacitor the modulation of the sampling clock can be eliminated. In most cases by theory or by observation we can identify such deterministic errors and by using proper filtering mechanisms we can get rid of most of the deterministic jitter added to the sampling clock. Therefore we concentrate our efforts mainly on Gaussian distributed random noise which cannot be estimated and negated owing to its nature of randomness.

As we know the deterministic jitter added due to sampling clocks can be nullified in a number of ways like the use of decoupling capacitors and therefore we concentrate on the effect of random jitter on a ADC output and the way in which multi-channel ADC’s can increase receivers tolerance towards jitter.

A receiver chain can be split into three main parts: the radio-frequency (RF) front-end, the analog baseband, and the digital baseband. The analog-to-digital converter (ADC) provides the interface between the analog and digital basebands. Parallelization in the design of receivers has been conventionally realized using sampling multiplexing through the time-interleaved ADC architecture. Fig. 20 shows the signal-to-noise-ratio performance of some of the latest reported single channel and time-interleaved ADCs [31]-[42]. The Figure shows also a line with the theoretical maximum achievable SNR for 1 ps and 5 ps of clock-jitter standard deviation in the SHA. The plot shows that the clock-jitter has become an impediment in the design of practical high performance ADCs and some of the latest reported implementations demand the standard deviation to be better than 1 ps, which requires prohibitively high power consumption in the clock generation circuits.

ADCs operating with sub-pico second clock-jitter are demonstrated using cutting-edge bulky equipment and in stand-alone configuration to avoid interference from adjacent devices. This setup is not practical in any of the envisioned transformative applications which require high levels of integration and miniaturization. The lack of robustness to jitter in the sampling clocks of time interleaved-ADCs has become a critical problem for parallel channel ADCs that are envisioned to support the future generation of wideband systems.

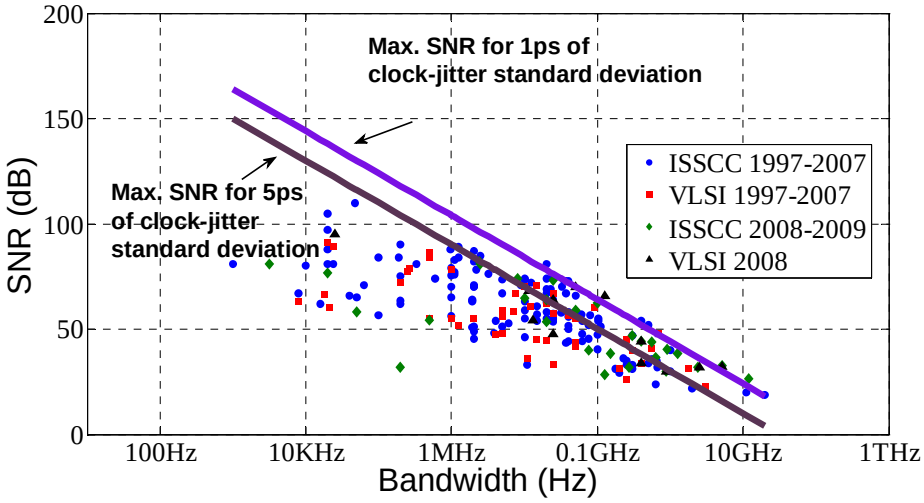

Fig. 20. Achievable SNR vs Jitter with State of Art Receivers.

4.1 The Fundamental Limitation: Clock-Jitter

The fundamental clock-jitter limitation can be understood and quantified by a well known equation in the field of data converters. If an ADC is sampling a sinusoidal signal running at full Nyquist rate (F_s=2BW), a sampling clock-jitter of variance σ_j^2 introduces an equivalent additive noise of variance $\sigma_n^2 = \left(2\pi BW\sigma_j\right)^2$ [43] . Therefore the signal quality degrades quadratically with the signal frequency. This leads to very stringent requirements on the clock-jitter for the next generation of signal bandwidths and resolutions. For instance consider a baseband signal bandwidth of $BW = 5\text{GHz}$ and $b = 7$ bits of resolution, which using the fundamental data converters relationship $\text{SNR} = 6.02b + 1.76\text{dB}$, is equivalent to an SNR requirement of around 44 dB. The SNR

dependence on the clock-jitter can be written directly as $\mathrm{SNR} = 1 \Big/ \left(2\pi BW\sigma_j\right)^2$. Solving for σ_j, we obtain 201 fs (201×10^{-15} seconds). Note, this is also an issue in medium-bandwidth high-resolution applications, with the same jitter specification obtained for *BW*=50 MHz and SNR=84 dB ($b \sim 14$ bits of resolution). Such a jitter standard deviation requirement, if not impossible to achieve in many circuit technologies, will greatly increase area and power consumption of the phase-locked-loop (PLL) circuit and buffers that generate and drive the sampling clocks. It is important to note that the above simple clock-jitter requirement analysis is valid only for a single tone signal that drives any Nyquist rate ADC such as time-interleaved ADC or a single channel ADC topology such as pipelined, flash, and successive approximation ADCs . Although the sampling clocks of a time-interleaved ADC run at a fraction of the Nyquist rate frequency, every channel still sees the full bandwidth of the input signal which will produce aliasing of noisy high frequency components when sample d with a jittered clock. Therefore, although the sampling rate in each channel of a time-interleaved ADC is relaxed by the number of channels, the jitter requirement is the same as in a single channel ADC. This issue has become one of the fundamental obstacles that are preventing transformative specifications in wideband data communication receivers.

The receiver we discussed in the previous section is another kind of multi-channel receivers but the tolerance it offers to jitter is poor because the ADC at the end of the each path is still seeing huge amount of high frequency quantity. This is because each path has a *sinc* filter integrated in it and the filter is of first order. As we know first

order filters have a roll-off of 20dB/decade and this implies that if each path is processing 250 MHz of signal the unwanted signal at 2.5GHz would only see an attenuation of 20dB. Because of this poor attenuation offered to high frequency unwanted signal the tolerance we obtain to jitter is poor. In order to improve the jitter performance, the receiver is modified and re-presented below,

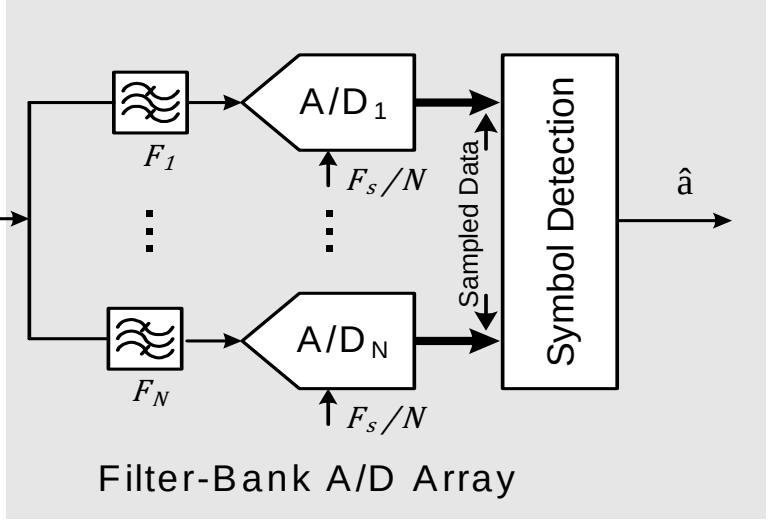

Fig. 21. Multi-Channel Filter Bank Type of Receiver.

Consider the general *N*-channel receiver structure in Fig. 21. The filters F_1,F_2…F_N channelize the input signal bandwidth into *N* bands and down-convert the signal to baseband. For an ideal "brick-wall" type of filter, the signal bandwidth in each channel is reduced *N* times leading to an additive noise variance that can be obtained directly from the elementary equation $\sigma_n^2 = \left(2\pi\sigma_j BW / N\right)^2$, which is N^2 times lower than the one for a time-interleaved ADC. However, filters with finite roll-offs do not

separate the channel's spectrum perfectly and each channel still sees a spectrum full of energy, although with some out of band attenuation. The remaining out of band spectrum energy produces noisy aliasing into the signal band when it is sampled with a jittered clock. This has been considered a serious drawback of filter banks in the data conversion community. Indeed, it is easy to show that if a signal is uniformly channelized with *N* first order filters, each with bandwidth *BW/N*, the effect of clock-jitter is worse than if a single channel or time-interleaved ADC is used. This is what happens when we use the *sinc* filter bank receiver as the high frequency content is not sufficiently attenuated. Sadly enough, the lack of rigorous analytical tools that would allow taking a closer look at this architecture and its intricacies has discouraged the use of analog baseband multi-channel filters to obtain clock-jitter robustness.

From the above paragraphs it is clear that lesser the amount of high frequency content in each path lesser is the error introduced due to jitter. Achieving a brick wall filter is impossible so we try to analyze the system's performance by increasing the filter order in each path and later we support these results with analytical derivations. The analysis is developed in the context of orthogonal-frequency-division-multiplexing (OFDM) [44]-[48] signals which are the preferred signaling scheme of wideband standards such as ultra-wideband (UWB) and 60 GHz ECMA-387. Clock-jitter in conventional single channel OFDM systems has been analyzed in [49] which provides preliminary foundation that will be adopted for the evaluation and comparison of the results obtained from analysis/simulations.

As we have discussed the tolerance to jitter depends on the amount of high

frequency signal or the bandwidth being processed in each path, and therefore by the use of brickwall filters or really high order filters in each path we can improve the receiver's performance in the presence of sampling clock jitter. We first need to establish this is what happens in the case of receivers built for OFDM signals as well. The derivation supporting the improvement achieved by channelizing the signal into multiple paths in regards to an OFDM receiver is presented below.

4.2 Analytical Derivation of the Sampled Data SNR

There are two figures of merit that fully characterize and provide the basic analytical tools to understand the tolerance to clock-jitter of the multi-channel receiver: the sampled data SNR and the symbol detection SNR. The sampled data SNR measures the data quality at the output of the samplers' right before the digital baseband. The symbol detection SNR measures the data quality after the digital baseband. Both SNRs will be obtained in the context of OFDM signals with emphasis on their dependence on the number of channels *N*, which is the fundamental design parameter of the proposed receiver.

Fig. 22 shows the basic block diagram used for modeling the OFDM signal transmission and reception.

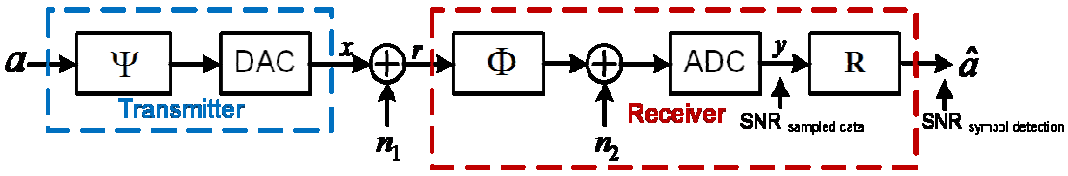

Fig. 22. Model for the OFDM Transmission and Reception Mechanism.

To facilitate the analysis, the model is introduced with a matrix notation. The transmitted signal is given by:

$$\mathbf{x} = \mathbf{\Psi a}, \tag{27}$$

where $\mathbf{a} = [a_1, a_2, \ldots, a_S]^T$, $\mathbf{\Psi} = [\Psi_1, \Psi_2, \ldots, \Psi_S]^T$. This model is valid for any arbitrary transmitter that simultaneously sends *S* symbols. In the particular and important case of OFDM, the matrix $\mathbf{\Psi}$ is the set of complex exponential functions that represent the IDFT operation with N points of an OFDM transmitter. The received signal is given by:

$$\mathbf{r} = \mathbf{x} + \mathbf{n_1}, \tag{28}$$

where, $\mathbf{n_1}$ is the noise added during the transmission. Consider an OFDM signal composed of *M* sinusoidal signals: $x(t) = \sum_{m=1}^{M} A_m \sin(m\Delta\omega t)$, where A_m is the symbol of the m^{th} tone, $\Delta\omega$ is the tone frequency spacing which is equal to *BW/M*. This signal is sampled at instances $t_n = nT_s + \delta t$ by clocks of frequency $F_s = 1/T_s$ and clock-jitter δt with variance σ_j^2. The uncertainty produced by the clock-jitter on the OFDM signal can be expressed as:

$$x(t) = \sum_{m=1}^{M} A_m [\sin(m\Delta\omega t)\cos(m\Delta\omega\delta t) + \cos(m\Delta\omega t)\sin(m\Delta\omega\delta t)]$$

which for a small δt can be approximated as:

$$x(t) \cong \sum_{m=1}^{M} A_m \sin\sin(m\Delta\omega t) + \sum_{m=1}^{M} m\Delta\omega\delta t A_m \cos(m\Delta\omega t) \tag{29}$$

The error produced by the clock-jitter is approximately given by:

$$\varepsilon(t) = x(t) - \sum_{m=1}^{M} A_m \sin\sin(m\Delta\omega n T_s) \cong \sum_{m=1}^{M} m\Delta\omega\delta t A_m \cos(m\Delta\omega t) \tag{30}$$

The variance of this additive error can be expressed as:

$$\sigma_n^2 = \overline{\varepsilon^2(t)} = \overline{\delta t^2}\,\frac{\Delta\omega}{2\pi}\int_0^{\frac{2\pi}{\Delta\omega}}\left[\sum_{m=1}^{M} m\Delta\omega A_m \cos\left(m\Delta\omega t\right)\right]^2 dt \tag{31}$$

which, owing to the orthogonal nature of the OFDM signal, can be re-written as:

$$\sigma_n^2 = \sigma_j^2\,\frac{\Delta\omega}{2\pi}\sum_{m=1}^{M}\int_0^{\frac{2\pi}{\Delta\omega}}\left[m\Delta\omega A_m \cos\left(m\Delta\omega t\right)\right]^2 dt \text{ , where } \sigma_j^2 = \overline{\delta t^2}$$

This expression simplifies to:

$$\sigma_n^2 = \sigma_j^2\sum_{m=1}^{M}\frac{m^2\Delta\omega^2 A_m^2}{2} = \frac{1}{2}\sigma_j^2\Delta\omega^2\sum_{m=1}^{M} m^2 A_m^2 \tag{32}$$

The SNR is found to be given by:

$$\text{SNR} = \sum_{m=1}^{M}\frac{A_m^2}{2}\Bigg/\left[\frac{\sigma_j^2\Delta\omega^2}{2}\sum_{m=1}^{M} m^2 A_m^2\right] = \sum_{m=1}^{M} A_m^2\Bigg/\left[\sigma_j^2\Delta\omega^2\sum_{m=1}^{M} m^2 A_m^2\right]$$

Assuming $A_m = A$ for $m=1,\ldots,M$, the sampled data SNR final expression is:

$$\text{SNR}_{\text{sampled data}} = \frac{M}{\sigma_j^2\Delta\omega^2\sum_{m=1}^{M} m^2} \tag{33}$$

Therefore, the sampled data SNR is inversely proportional to the clock-jitter variance, the squared value of the OFDM frequency spacing and the term $\sum_{m=1}^{M} m^2$. This last term is critical in the performance enhancement of the multi-channel receiver. For instance, consider a 4-channel system using ideal brickwall type of filters. The original OFDM signal has 128 tones that are split into 4-channels with 32 tones each, defining SNR_{128} and SNR_{32} as the SNR for the original signal and 4-channel signal, the SNR enhancement of the multi-channel approach is given by:

$$\mathrm{SNR}_{\mathrm{Enhancement}} = \mathrm{SNR}_{32} - \mathrm{SNR}_{128} = 10\log\left(\frac{32}{128}\right) - 10\log\left(\frac{\sum_{m=1}^{32} m^2}{\sum_{m=1}^{128} m^2}\right) \approx 12\mathrm{dB}$$

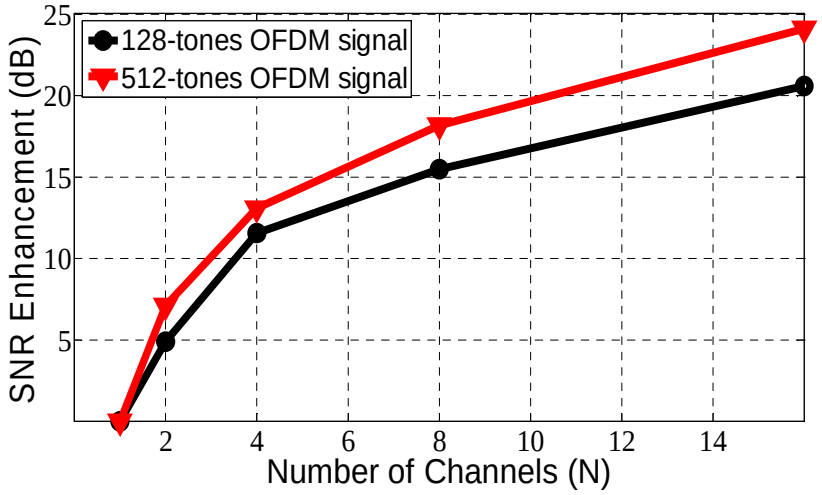

Fig. 23. SNR Enhancement as a Function of Channels.

4.3 Analytical Derivation of the Symbol Detection SNR

Without loss of generality, the receiver diagram in Fig. 22 only models the analog and digital baseband processing and Fig. 23 shows the SNR enhancement achieved before reconstruction as function of number of paths. The matrix Φ represents the analog filter bank transformation. For N channels, Φ will have N columns, one per channel. The number of rows of Φ corresponds to the number of samples per channel that the ADC takes for one block of K symbols. The sampling rate should comply with the Nyquist sampling theory, i.e., the number of samples should be no less than K. The receiver can be represented by the following linear transformation:

$$\mathbf{y} = \mathbf{\Phi r} + \mathbf{n_2} = \mathbf{\Phi(\Psi a} + \mathbf{n_1)} + \mathbf{n_2} \tag{34}$$

where, $\mathbf{n_2}$ is the noise during sampling. Note that the effects of clock-jitter are included in $\mathbf{n_1}$ and $\mathbf{n_2}$ and therefore the DAC/ADC in the diagram are ideal. That the clock-jitter variance and the corresponding additive noise variance were derived in (32). For brevity, (34) is rewritten as:

$$\mathbf{y = Ga} + \mathbf{n}, \tag{35}$$

where $\mathbf{G = \Phi\Psi}$, and $\mathbf{n = \Phi n_1} + \mathbf{n_2}$. This is an over determined system, and the least squares (LS) estimation of $\mathbf{a}$ is given by:

$$\mathbf{\hat{a} = Ry = a} + \mathbf{Rn}, \tag{36}$$

where $\mathbf{R} = \mathbf{G}^{\dagger} = (\mathbf{G}^H\mathbf{G})^{-1}\mathbf{G}^H$. The matrices $\mathbf{G}$ and $\mathbf{R}$ are the *Generation Matrix* and *Symbol Detection Matrix*, respectively. Depending on the receiver's architecture, $\mathbf{G}$ and $\mathbf{R}$ vary, which results in different amplification of the noise $\mathbf{n}$ as shown below:

$$E\left[\left\|\mathbf{Rn}\right\|^2\right] = E\left[\mathbf{n}^H\mathbf{R}^H\mathbf{Rn}\right] = E\left[\mathbf{n}^H\mathbf{Q}^H\Lambda\mathbf{Qn}\right]$$
$$= E\left[\left(\sum_{i=1}^{S}\lambda_i n_i^*\mathbf{q}_i^H\right)\left(\sum_{j=1}^{S}n_j\mathbf{q}_j\right)\right] = E\left[\sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i n_i^* n_j\mathbf{q}_i^H\mathbf{q}_j\right]$$
$$= \sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i E(n_i^* n_j)\mathbf{q}_i^H\mathbf{q}_j = \sum_{i=1}^{S}\lambda_i E(n_i^* n_i)\mathbf{q}_i^H\mathbf{q}_i$$
$$= \sum_{i=1}^{S}\lambda_i E(\left\|n_i\right\|^2)$$

where $\mathbf{Q} = [\mathbf{q}_1^T, \mathbf{q}_2^T, \ldots, \mathbf{q}_S^T]$, $\mathbf{q}_i^T$ is the eigenvector of $\mathbf{R}^H\mathbf{R}$ corresponding to the eigenvalue λ_i, i.e., the singular value of $\mathbf{R}$, and $\mathbf{Q}^H\mathbf{Q} = \mathbf{I}$. Assuming that the noise is Gaussian with zero mean and variance σ^2_{n}, then

$$E\left[\left\|\mathbf{Rn}\right\|^2\right] = \sigma_n^2 \sum_{i=1}^{S} \lambda_i \tag{37}$$

Therefore, the noise amplification of different multi-channel receiver architectures is determined by the singular values of the reconstruction matrix $\mathbf{R}$. In the muti-channel architecture proposed here, the type of filters will change $\mathbf{G}$ which in turn changes $\mathbf{R}$ leading to a different digital and analog receiver structure.

Now, replacing σ^2_{n} by the expression in (37), the SNR of the detected symbols can be expressed as:

$$\mathrm{SNR} = \frac{\left\|\mathbf{a}\right\|^2}{\frac{1}{2}\sigma_j^2 \Delta\omega^2 \sum_{\mathrm{m}=1}^{\mathrm{M}} m^2 A_m^2 \sum_{\mathrm{i}=\mathbf{1}}^{\mathrm{S}} \boldsymbol{\lambda}_{\mathrm{i}}} \tag{38}$$

Fig. 24 shows the SNR versus power of jitter for the case of 1 and 4 paths. The derivation and the results presented make it clear that the channelizing the OFDM signal into separate bands gives a definite amount of improvement in the SNR achievable. But as pointed out earlier this improvement can be achieved only if we completely attenuate the signal outside the band of interest. Practical implementation of brickwall filters, as we know is impossible and therefore we try to achieve the some improvement by increasing the filter order in each path.

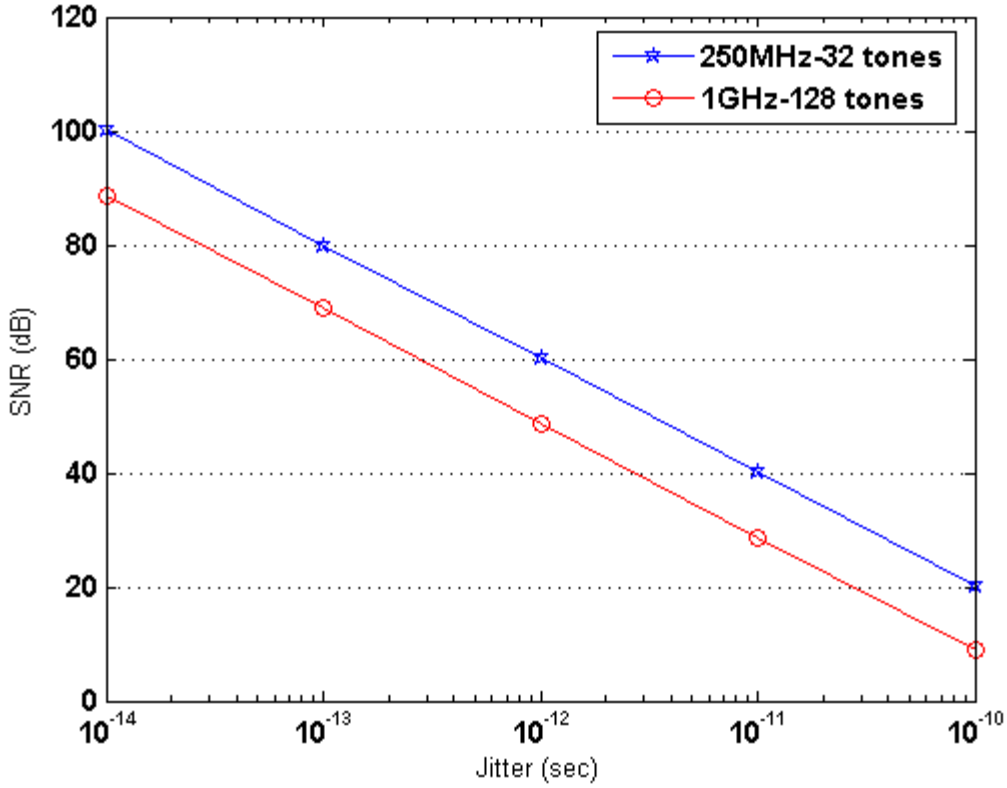

Fig. 24. SNR Plotted as Function of Jitter from the Mathematical Derivation.

As we keep increasing the filter order we expect the out of band signal to be attenuated more and therefore the receiver to perform better in terms of jitter tolerance.

4.4 System Setup

In order to prove the above hypothesis we build a multi-channel OFDM receiver in Matlab and present the results. The input to the receiver is an OFDM complex signal with S=128 carriers and bandwidth BW = 5GHz. The receiver has 5 paths and the LO is each path is 4GHz, 2GHz, 0, -2GHz and -4GHz. Figure below shows the model of the receiver used for simulation purpose.

Fig. 25 shows the block diagram of the multi-channel receiver with 5 parallel channels, an aggregated sampling rate of I&Q 10GS/s. The LO generation is also showed in the figure. In reality the since we sampling both the I&Q paths, the sampling rate required in I&Q separately is only 1GS/s, the total sampling rate achieved is 10GS/s. We use analog filter banks in each path. Note that each path can be using *sinc* type of filters as described in previous sections. Such a modeling of the receiver would no doubt provide additional advantages of lowering digital complexity and saving power consumption. But here we use analog filter banks as it is easier to simulate real time higher order filters. The jitter tolerance that is achieved here by increasing the order of the filter can easily be extended to the *sinc* filter bank type of receivers. The receiver was simulated with first, second and third order filters in each path. We observed that the performance of the 3^{rd} order filters was very close to that of the performance expected for brickwall filters.

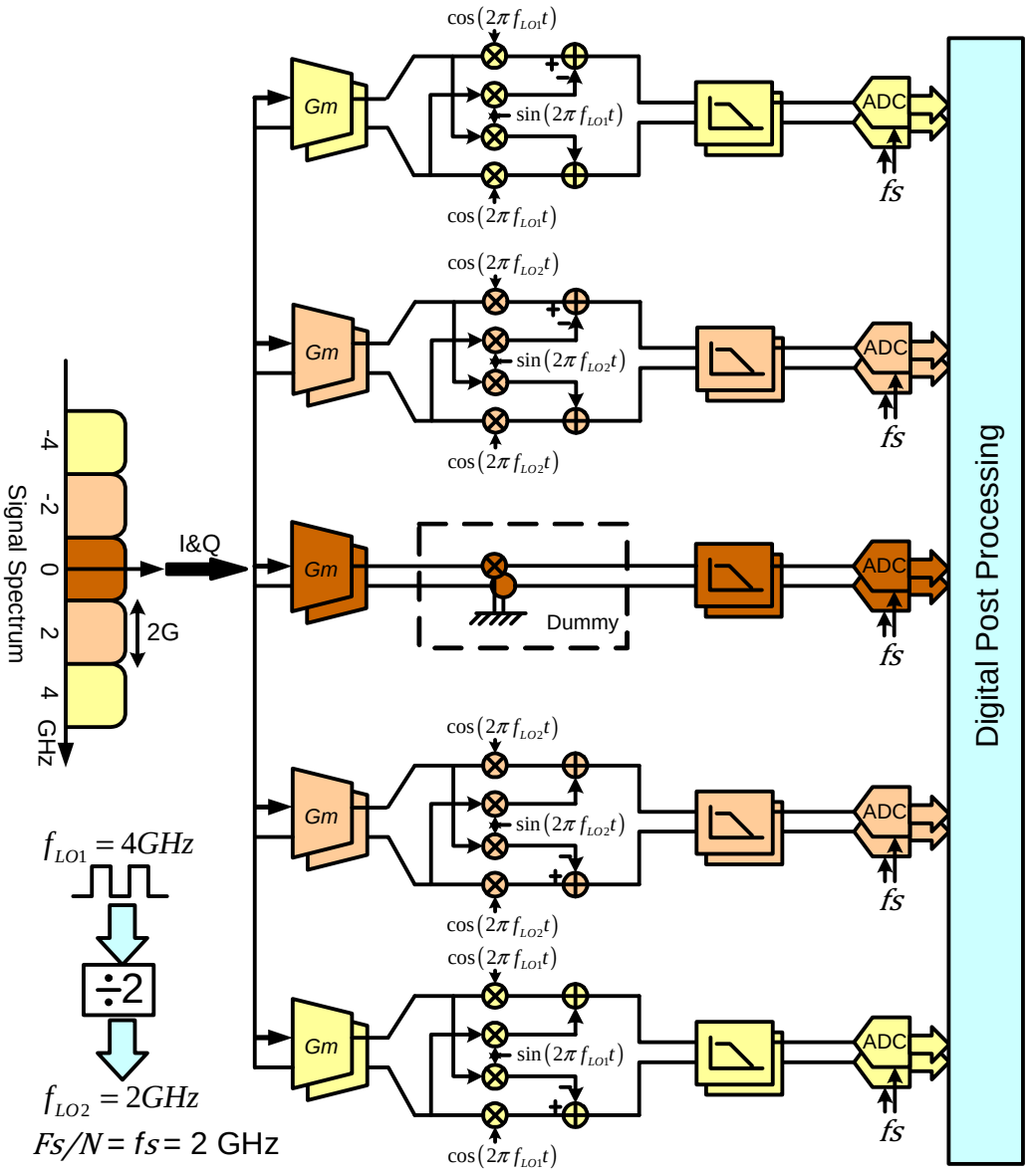

Fig. 25. Jitter Tolerant Multi-Channel Receiver.

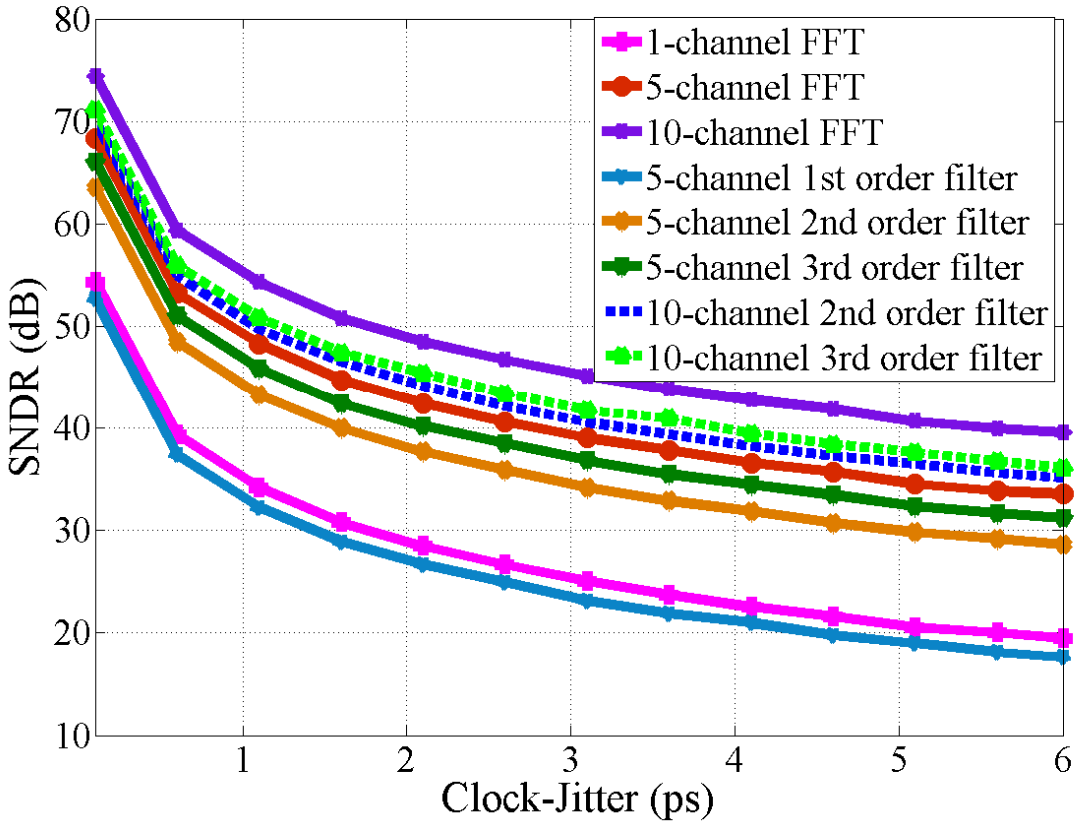

Fig. 26. Output SNDR for Different Filter Orders and Number of Channels vs Jitter.

The results, obtained by Monte Carlo simulations, are presented in Fig. 26 which shows the SNR at the output of the receiver (the symbol detection SNR) versus the clock-jitter standard deviation for the conventional 1-channel OFDM receiver and multi-channel receiver topology with N=5 and N=10 channels. The figure shows that the ideal 10-channel brickwall filter approach offers a 20 dB SNR enhancement, and a practical 2nd order multi-channel receiver performs very close to the ideal curve. The plot also reveals that to achieve 7 bits of resolution (44 dB), the conventional OFDM receiver based on a time-interleaved ADC, or some other single channel conventional ADC,

requires a 0.345 ps clock-jitter, whereas the 5-channel receiver approach can tolerate 1.36 ps of clock-jitter standard deviation. Moreover, a 10-channel receiver can tolerate 3.5 ps. Additionally, the plot reveals that if an SNR of 40 dB is sufficient, the 10-channel receiver approach can tolerate up to 5 ps of standard deviation whereas the single channel counterpart needs roughly 0.5 ps, a 10X improvement in clock-jitter tolerance. This degree of clock-jitter tolerance will enable several transformative wireless high-speed data communication applications that are very difficult to achieve with conventional single channel and time interleaved topologies.

Monte Carlo simulations depicted in Fig. 26 illustrate this important result as it was previously discussed. An additional design specification that is highly relaxed in the multi-channel approach is the SNR sensitivity to variations in the clock-jitter. It is shown that for SNR=40 dB, the single channel approach has an SNR sensitivity of -20 dB/ps whereas the 10 channel approach has -2 dB/ps. This 10 times lower senstivity to clock-jitter variations is crucial to obtaining robustness to episodic clock-jitter spikes produced by interference or other unpredictable events.

The input signal as already pointed out is baseband OFDM, with 5 GHz of bandwidth and 128 tones signal. This signal has the capability of providing the high data rates of the future generation of wideband data communication needed to enable several transformative applications such as millimeter-wave radios, cognitive-radios, software-defined radios and massive parallel RF coils for fast magnetic resonance imaging.

4.5 Clock Generation

The new multi-channel receiver is achieved with low complexity clock generation, as it requires clock at 4 GHz (see Fig. 26). A simple divide-by-2 circuit generates the 2 GHz clock for the second set of mixers and for the ADC sampling clocks. Note that in a time-interleaved architecture, the front-end sample-and-hold amplifier requires a 10 GHz sampling clock. This overall lower clock frequency translates into critical power savings in the proposed multi-channel receiver. The middle channel is already centered at DC (0 Hz) and does not require frequency translation although a dummy mixer could be used for matching purposes. Simple analysis and simulations show that the effect of jitter on the local oscillator (LO) clocks is negligible in comparison with the clock-jitter in the sampling clocks. Thus, all the clocks will have the very relaxed clock-jitter specifications discussed throughout this paper. For the adopted receiver, a simple frequency divider by 2 is needed. This is evidence of the low overhead in the extra LOs needed in the proposed approach.

4.6 Digital Reconstruction

Calibration of the analog imperfections of the multi-channel system is a fundamental objective for successfully accomplishing a fully functional multi-channel receiver. All multi-channel systems are sensitive to mismatches in key blocks.

We have discussed and derived a calibration scheme for the multi-channel *sinc* filter bank receivers. A similar calibration scheme can be employed in this case as well to get rid of the many errors that are introduced into the multi-channel system. Some of the primary sources of the error in multi-channel analog filter bank receiver are gain and

phase mismatches between the paths produced due to the imperfect matching in the design of the various circuits. The mismatches in the gain of the filters in each path also create error.

Since the transformation of the input symbols transmitted to the samples collected at the output of the multi-channel receiver is linear, we can represent the transformation mathematically as below-

Assume there are *N* paths and in each path *M* samples are collected. The *M* samples collected in each path amount to a total of *MN* samples $Y(m,n)\Big|_{m=0}^{M-1}\Big|_{n=0}^{N-1}$ given by,

$$Y_{m,n} = x(mT_s)\Phi_n^*(mT_s)$$

where T_s is the sampling period, $x(t)$ is the received signal, $\Phi_n(t)$ is the basis function onto which the input signal is expanded in the n^{th} path, m=0 to *M-1* indicates the m^{th} segment in each channel and n=0 to *N-1* refers to the n^{th} channel. The basis function here is formed by the mixing operation followed by analog filtering. These quantized samples are processed digitally to estimate the symbols directly using a least squares (LS) estimator.

The sampled data, can be represented in the form of a vector *y* as shown below,

$$\overline{y} = [Y_{0,0}\ ,\ Y_{0,1}\ ,\ \ldots\ Y_{0,N-1}\ ,\ Y_{1,0}\ ,\ Y_{1,1}\ ,\ \ldots Y_{M-1,N-1}\ ]^{\mathrm{T}}$$

The data that is modulated on all the sub-carriers can be represented in the vector form as shown below,

$$\left[a_i(0), a_q(0), a_i(1), a_q(1), \ldots . a_i(K), a_q(K)\right]$$

It can be seen that the entire system that generates the vector $\bar{y}$ from $\vec{a}$ can be represented by a linear matrix equation as,

$$G\vec{a} = \vec{y}$$

As the real and imaginary components of both the carrier and the LO signal are represented separately inside the matrix, G becomes a $2NM \times 2K$ matrix. The data $\vec{a}$ can be reconstructed from the received vector $\bar{y}$ using the LS estimator.

$$R = (G^H G)^{(-1)} G^H$$

With the knowledge of the reconstruction matrix R and the received vector $\bar{y}$, the data transmitted can be estimated using the equation,

$$\vec{a} = R\vec{y}$$

As a starting point, preliminary back-end digital least mean squares (LMS) calibration algorithm to learn the static mismatches has been tried out which is a well-understood, simple and effective way to correct these problems. The uniqueness of the approach is that the algorithm is developed in the context of OFDM signals, where a set of known training symbols is used to update the receiver matrix R. In this way there will be no analog overhead to obtain a reference signal.

Using the same OFDM transmitter and multi-channel receiver explained in Fig. 26, a simulation result is provided in Fig. 27 which shows the LMS algorithm performance for several iterations. The digital back-end both detects the symbols from the ADC output and has the LMS algorithm learning the receiver analog blocks mismatches. The calibration can be performed on the forward transformation matrix – G

or the reverse transformation matrix – *R*. The matrix initialization and frequency offset corrections procedures are to be followed as pointed in earlier sections before calibration can be kicked off on the transformation matrix.

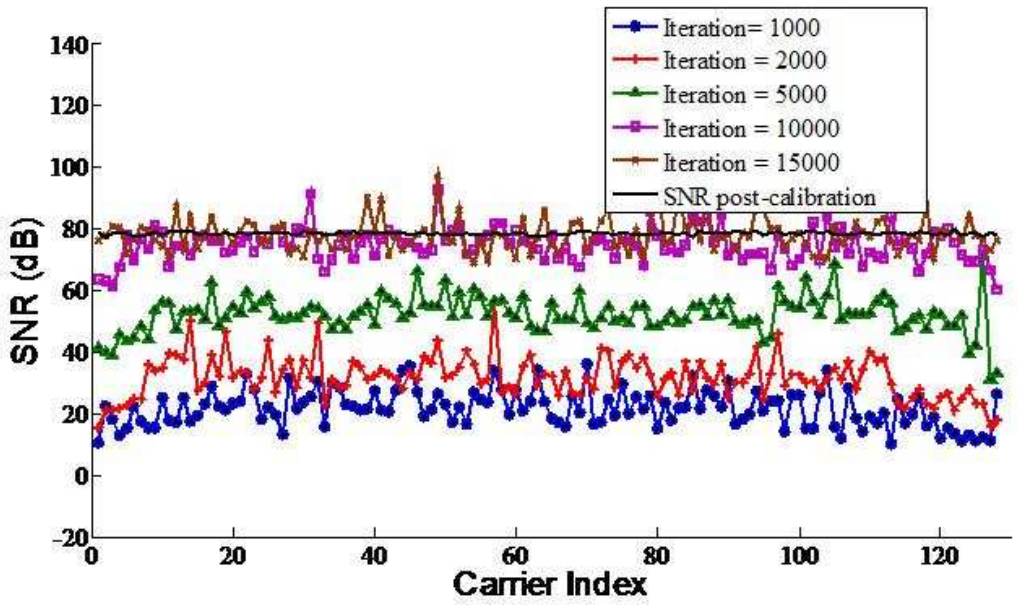

Fig. 27. Improvement from Calibration.

In the simulation, controlled mismatches are introduced between the different channels. The gain variations between paths are 10-20 % and the phase mismatch is 10 to 15 %. Additionally, there is a mismatch in the type of the local oscillator (LO) signal. The digital post processing block assumes the LO signals to be ideal square waves. However, in the receiver model, the square waves have an exponential rise and decay due to the RC filter in the clock routing network. As shown in Fig. 27 , the calibration algorithm dramatically improves the receiver performance from 20 dB to 80 dB. The

calibration literally heals the highly impaired RF and analog receiver frontend. Table 2 summarizes the jitter tolerance achieved.

Table 2: Summary of Jitter Tolerance Achieved.

Parameter	10-Channel Receiver	5-Channel Receiver	1-Channel Receiver
Signal Band	-5GHz - 5GHz(I and Q)	-5GHz - 5GHz(I and Q)	-5GHz - 5GHz(I and Q)
Modulation Scheme	QPSK-OFDM	QPSK-OFDM	QPSK-OFDM
No. of Carriers	128	128	128
Carrier Spacing	78.125MHz	78.125MHz	78.125MHz
Number of Paths	10	5	1
Sampling frequency in each path	1.25GHz(I and Q)	2.5GHz(I and Q)	12.5GHz(I and Q)
Number of Samples collected in each path	16	32	160
Jitter Tolerance @ ENOB=7	3.5ps	1.36ps	0.345ps

5. BANDWIDTH OPTIMIZATION

In this section we will try to improve the jitter tolerance of our receiver structure without the overhead of increasing the filter band order. Just to recap the receiver architecture the signal is down converted first by use of mixing operation and then low passing the signal selects different frequency bands in each path. Assuming the low pass filters are perfect brick wall filters the ADC in each path works at only $2*f_{max}/N$. Also the maximum frequency component seen in each path is only f_{max}/N where N is the number of paths. If it is a pure sinusoidal signal then the SNR according to the previous equation is expected to get better by N^2 times. But note that this is true only in the presence of ideal Brick wall filters which are unrealizable in practice. What we have in reality are filters of finite roll off, which means we need very high order filters to replace the Brick wall filters, and even if we use such high order filters some part of the outer band of frequency is seen in each path though with reduced amplitude. Such a signal when sampled at $2*f_{max}/N$ with a jittery clock results in noisy aliasing of the outer band of frequencies which are present in every path due to finite roll off. It has been found out in the previous sections that even in the presence of such noisy aliasing there is significant improvement in jitter tolerance when higher order filters are used.

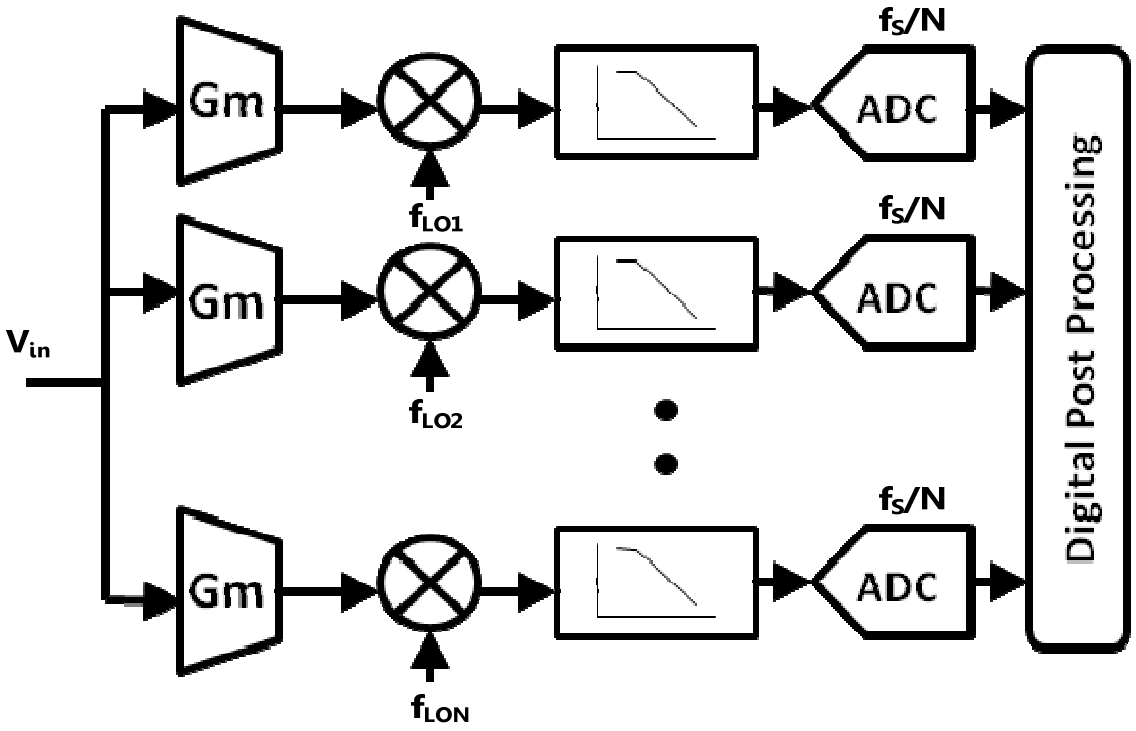

Fig. 28. Receiver Structure Used for Bandwidth Optimization.

5.1 Bandwidth and Filter Order Trade-Off

To understand the effect of bandwidth and filter order on the receiver one needs to understand the digital reconstruction of the symbols done at the backend. Mean square algorithm is used for the detection of symbols without actually reconstructing the signal. This saves a lot in terms of complexity and makes the reconstruction problem straightforward. Fig. 28 shows the receiver structure we will be using for analyzing the trade-off.

The signal transformation from the transmitter end to the signal detection end can be mathematically represented. *a* is the vector of symbols that need to be transmitted. These symbols go through the transmitter and receiver chain and are recovered in the *y* vector. The transformation from vector *a* to *y* can be represented by a matrix *G*.

$$G * \vec{a} = \vec{y}$$

Now *G* which is called the forward matrix is formed by sending a sequence of input symbols through the system, this can also be thought of as scanning the carriers. We can notice that this way of forming the forward matrix catches all the errors in amplitude and phase occurring across the carriers. Then for the Mean square estimation of the symbols from next transmission we invert the Forward matrix to form ***R*.**

$$R = (G^H G)^{-1} G^H$$

This reconstruction matrix corrects for all the amplitude and phase errors which manifest as errors in the weights. This feature of the symbol estimation can be exploited in our receiver to reduce the power consumption. Given that the low pass filters we have used are Butterworth filters, these filters manipulate the Gain and Phase of the input signal. Ideally in the pass band the Gain of the filter is unity and in the stop band the gain drops across the frequencies and also there is a phase shift caused by the filter. The rate of gain drop and phase shift depend on the order of the filter. The gain drop and phase shift the filter introduces can be considered as gain and phase errors and given that out digital reconstruction scheme can correct for these errors we can lower the bandwidth of the filters that we are using. Also one can easily understand that if the gain error is so high that the power of carriers becomes discernable from noise it cannot be

corrected and there would be evident signal loss. This places a limit on the extent to which the bandwidths can be reduced.

Fig. 29 shows the effect of varying the cutoff frequency on different orders of filters in the presence of sampling clock jitter. These simulations were done with a input complex signal of bandwidth 5 GHz with 10 paths. Therefore each path is expected to process 1/10 of the bandwidth that is 0.5 GHz. As we have seen before the performance of first order filters in the presence of sampling clock jitter is bad because of the finite roll off of the filter out of band carriers are not attenuated to a satisfactory level. Now since the Mean square estimation can reconstruct the data on carriers which are slightly in the stop band of the filter, we reduce the pass band frequency of the filters. The amount of attenuation on the carriers beyond 0.5 GHz increases therefore the error added due to jittery sampling of out of band decreases. This is evident in the figure when a first order filters cut off is decreased. The performance of the multi-channel receiver with first order filters gets better and keeps increasing as we decrease the bandwidth.

In case of second order filters, which have higher attenuation, the previous argument holds good and the performance gets better but when the bandwidth is decreased further owing to the sharp roll off of the filter the in band signal loss is greater and dominates the benefit of reduced aliased noise, therefore the SNR decreases as a whole. When it comes to the case of third order filters the attenuation is so large that the reconstruction matrix cannot correct for the gain error that creeps into the system and due to loss of in band signal the SNR achievable in the presence of jitter drops.

As we know the higher order filters consume a lot more power than the lower order counterparts. Therefore instead of using higher order filters to have better performance against sampling clock jitter in multi-channel receivers we can use a lower order Butterworth filter with reduced cutoff frequency. This gives drastic savings in power consumption and complexity of the receiver.

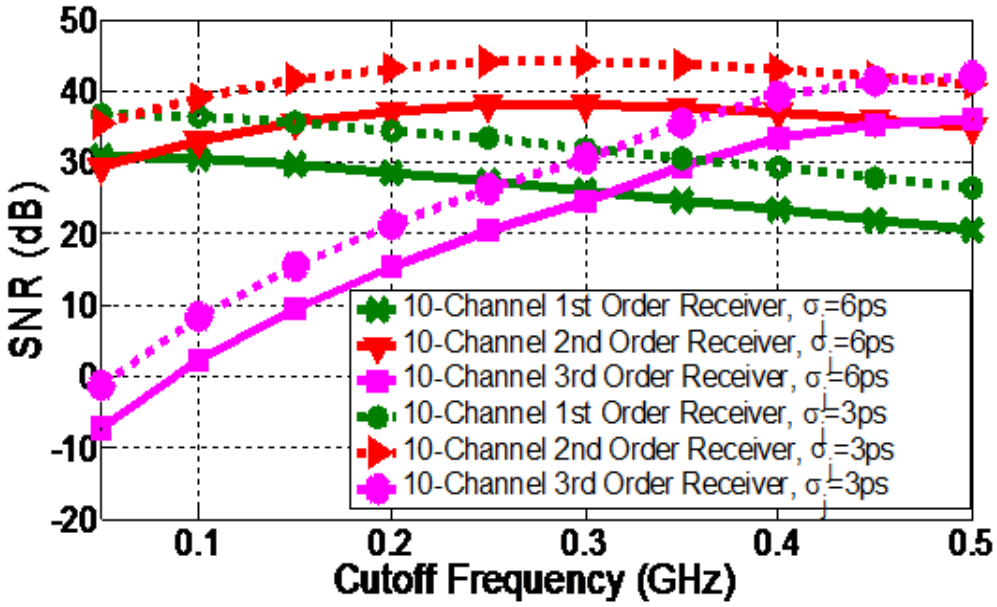

Fig. 29. Effect of Varying the Filter Bandwidth.

5.2 Analysis of Bandwidth Optimization Using Mathematical Models

Here we revisit the derivation we did in the previous section in order to be able to prove the concept of bandwidth optimization of lower order filters. As we have defined previously SNR_{SD} measures the data quality after the digital baseband. SNR_{SD} is obtained

in the context of OFDM signals with emphasis on their dependence on the number of channels, N. The transmitted signal was defined as:

$$\mathbf{x} = \mathbf{\Psi a},$$

where $\mathbf{a} = [a_1, a_2, \ldots, a_S]^T$, $\mathbf{\Psi} = [\Psi_1, \Psi_2, \ldots, \Psi_S]^T$ and the received signal is given by:

$$\mathbf{r} = \mathbf{x} + \mathbf{n_1},$$

where $\mathbf{n_1}$ is the noise added during the transmission. Given that the samples are collected satisfying the nyquist rate the output of the receiver can be represented as below for simplicity-

$$\mathbf{y} = \mathbf{Ga} + \mathbf{n},$$

This is an over determined system, and the least squares (LS) estimation of $\mathbf{a}$ is given by:

$$\hat{\mathbf{a}} = \mathbf{Ry} = \mathbf{a} + \mathbf{Rn},$$

where $\mathbf{R} = \mathbf{G}^{\dagger} = (\mathbf{G}^H\mathbf{G})^{-1}\mathbf{G}^H$. The matrices $\mathbf{G}$ and $\mathbf{R}$ are the *Generation Matrix* and *Symbol Detection Matrix*, respectively. Depending on the receiver's architecture, $\mathbf{G}$ and $\mathbf{R}$ vary, which results in different amplification of the noise $\mathbf{n}$ as shown in the previous section. Assuming that the noise is Gaussian with zero mean and variance σ^2_n, then

$$E\left[\, \|\mathbf{Rn}\|^2 \,\right] = \sigma_n^2 \sum_{i=1}^{S} \lambda_i \tag{39}$$

Therefore, the noise amplification of different multi-channel receiver architectures is determined by the singular values of the reconstruction matrix $\mathbf{R}$. In the

multi-channel architecture proposed here, the type of filters will change **G** which in turn changes **R** leading to a different digital and analog receiver structure.

Neglecting noise added due to transmission and assuming jitter noise only to calculate σ^2_n, consider an OFDM signal composed of M complex sinusoidals of bandwidth BW applied to the N-channel system in Fig. 28.

Without loss of generality, assume Butterworth filtering with magnitude $|H(j\omega)|^2 = \frac{1}{1+\left(\frac{\omega}{\omega_c}\right)^{2\alpha}}$ and phase $\varphi(\omega)$, where ω_c is the cutoff frequency and α is the filter order. After mixing and filtering, the signal in path *i* is given by

$$v_i(t) = \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{LOi})t}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{LOi}}{\omega_c}\right)^{2\alpha}}} \tag{40}$$

where A_m is the symbol of the m^{th} tone, $\Delta\omega$ is the tone frequency spacing which is equal to *BW/M*, and ω_{LOi} is LO frequency in path *i* . This signal is sampled at instances $t_n = nT_s + \delta(nT_s)$ by clocks of frequency $F_s = 1/T_s$ and clock-jitter $\delta(nT_s)$ with variance σ_j^2. The uncertainty produced by the clock-jitter on the OFDM signal can be obtained as:

$$v_i(n) = \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{LOi})nT_s} e^{j(m\Delta\omega-\omega_{LOi})\delta(nT_s)}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{LOi}}{\omega_c}\right)^{2\alpha}}} \tag{41}$$

which for a small $\delta(nT_s)$ can be approximated as:

$$v_i(n) \approx \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{LOi})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{LOi}}{\omega_c}\right)^{2\alpha}}} + \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{LOi})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{LOi}}{\omega_c}\right)^{2\alpha}}} j(m\Delta\omega-\omega_{LOi})\delta(nT_s)$$

(42)

The error produced by the clock-jitter is approximately given by:

$$\varepsilon_i(n) = v_i(n) - \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{osc})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{osc}}{\omega_c}\right)^{2\alpha}}} \approx \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{osc})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{osc}}{\omega_c}\right)^{2\alpha}}} j(m\Delta\omega-\omega_{osc})\delta(nT_s)$$

(43)

The variance of this additive error in the i^{th} path can be expressed as:

$$\overline{\varepsilon_i^{\,2}(n)} = \frac{T_s\Delta\omega}{2\pi} \sum_{n=0}^{\frac{2\pi}{T_s\Delta\omega}} \left|\varepsilon_i(n)\right|^2 \tag{44}$$

For the N paths, the total variance is given by

$$\overline{\varepsilon^2(n)} = \sum_i \overline{\varepsilon_i^{\,2}(n)} \tag{45}$$

Replacing the value of the error calculate from the above formula in (44) gives the total error introduced after symbol detection.

Eq. (39) defines the amount of noise amplification that the reconstruction of the symbols causes. The reconstruction matrix varies with the cut-off frequency of the filter as it tries to correct for the gain and phase error introduced in each path due to low cut-off frequency of the filter. Fig. 30 shows the variation of noise amplification with cut-off frequency of the filter. Similarly (43)-(45) define the dependence of the error added due to jitter as a function of the cut-off frequency. Fig. 31 shows the variation of the error due to jitter with the cut-off frequency of the filter.

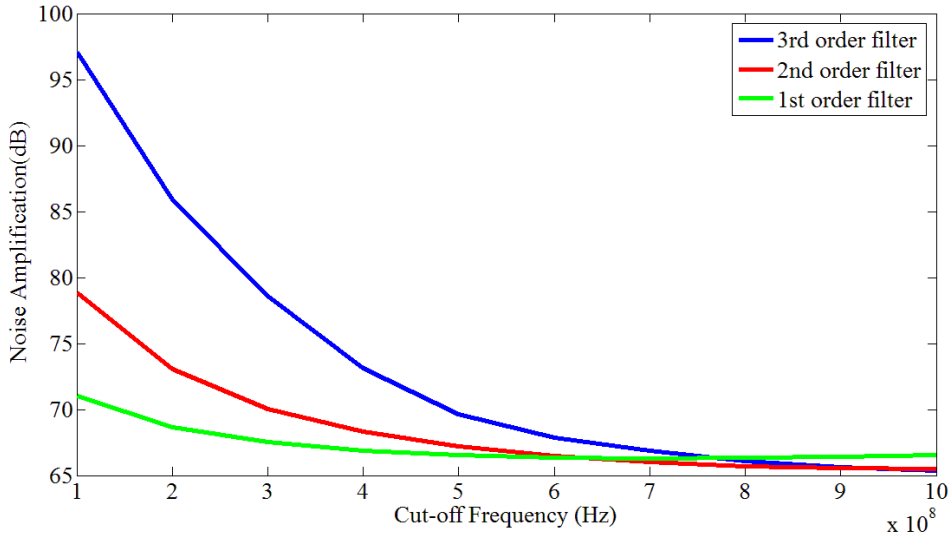

Fig. 30. Noise Amplification versus Cut-off Frequency.

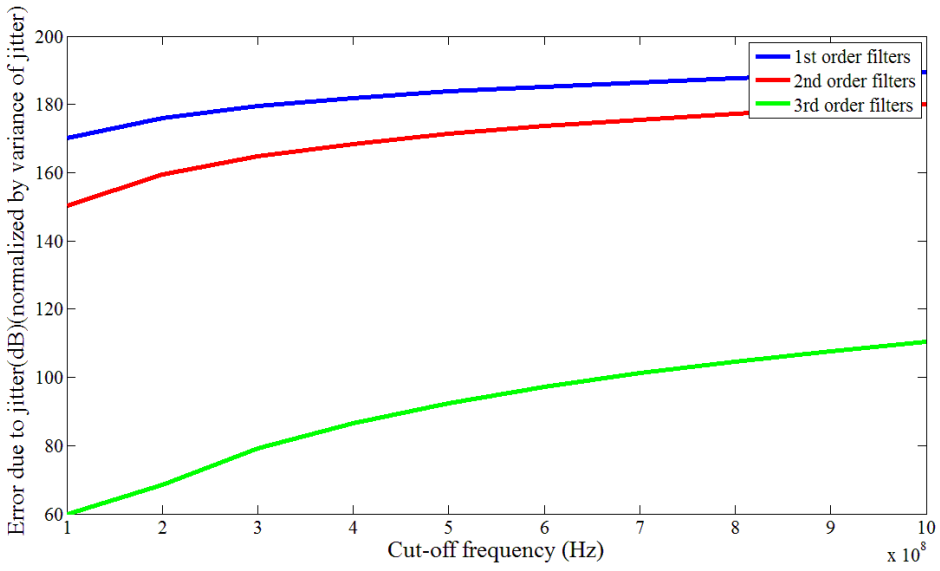

Fig. 31. Variation of Error Added due to Jitter with Cut-off Frequency.

It is clear from Fig. 30 and Fig. 31 that the cut-off frequency effects the two types of errors present in the system in different ways and clearly creates space for an optimization problem wherein the resolution or the SNR achievable can be maximized. SNR at the output can be written as follows-

$$SNR = f(f_{cutoff}, order, \sigma_{jitter})$$

For any given amount of jitter we would want to maximize the performance of the receiver of the SNR achievable at the output of the receiver. The optimization problem here clearly depends on the cut-off frequency and order of the filter and the variance of jitter added to sampling clocks is responsible only for scaling of the value of the function.

Therefore the Objective Function can be written as –

$$SNR = k * f_o(f_{cutoff}, order)$$

where ‘k’ is a scaling function depending on the variance of jitter

Therefore-

Optimization Problem-

maximize	$f_o(f_{cutoff}, order)$
subject to:	order={1, 2, 3}
	$0 < f_{cutoff} \leq f_s / N$

The above optimization problem, if feasible, should have an optimal value of f_0^* at $f_{cutoff,optimal}$ and $order_{optimal}$ within the constraints specified. The above problem can be optimized just as a function of cut-off frequency for a particular order of the filter. This would result in 3 different optimal points, one each for different order of the filters used.

Now looking at the two parts of the derivation we can clearly explain the improvement achieved in the performance of the receiver by lowering the cutoff frequency of the filters. According to equation (reverse) the symbols are reconstructed using the least squares solution.

$$\hat{\mathbf{a}} = \mathbf{Ry} = \mathbf{a} + \mathbf{Rn}, \tag{46}$$

When we lower the cutoff frequency of the filters in each path, this attenuates the signal in the band of interest and thereby creates a gain error on the symbols, this gain error reflects as an erroneous co-efficient in the forward transformation matrix ***G.*** When the inverse of this matrix is calculated to recover the transmitted symbols, these gain errors are corrected and we get back the actual symbols transmitted but note from the equation above that the noise also gets multiplied by the ***R*** matrix and therefore by virtue of the erroneous coefficients amplifies the noise. This noise amplification defines the lowest cutoff frequency of the filters that can be used in the receiver.

Now looking at the formula for the error introduced in each path due to jitter-

$$\varepsilon_i(n) = v_i(n) - \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{osc})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{osc}}{\omega_c}\right)^{2\alpha}}} \approx \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{LOi})} e^{j(m\Delta\omega-\omega_{osc})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{osc}}{\omega_c}\right)^{2\alpha}}} j(m\Delta\omega-\omega_{osc})\delta(nT_s)$$

(47)

We can see that the error introduced can be reduced by increasing the order of the filters which would attenuate the error more and thereby increase the tolerance to jitter. This is what was done in the previous section to obtain jitter tolerant receivers. Now instead of increasing the order of the filters which involves higher area, power consumption and complexity we can play with another parameter present in the above formula. It is the cut off frequency of the filters, by reducing the cut-off frequency of the filter the denominator of the error increases and therefore the overall error reduces. But as we have noted previously itself, thought the error is being attenuated the signal also gets attenuated, and this implies that the reconstruction matrix causes more noise amplification. In the case of first order filters we observed that the noise amplification is not much and we can achieve an improvement in the jitter performance by reducing the filter cut off frequency to as low as 50MHz and the receiver system with first order filters with said cut off had a performance similar to 2nd order filters with a cut off frequency of 500MHz. Similarly we can improve the performance of the receiver by reducing the cut off frequencies of 2nd order filters. We see that for a 10 Channel case we can reduce the cut off frequency till 250MHz and reducing it below this value would drop the performance implying that the attenuation of the signal is so much that the noise amplification due to reconstruction dominates the improvement in jitter tolerance

achieved, thereby decreasing the overall performance. For a 3rd order filter the attenuation of out of band signal was so much that any decrease in the cutoff frequency amplified noise to an extent where the improvement in jitter tolerance was not visible.

Fig. 32 shows that the theoretical results obtained from the mathematical derivation done in this section match pretty well with the simulation results that we achieved for the multi-channel receiver with 5 paths and a total sample rate of 10Gs/s. Each channel uses butterworth filters and the cutoff is varied to find an optimum point where the output resolution maximizes.

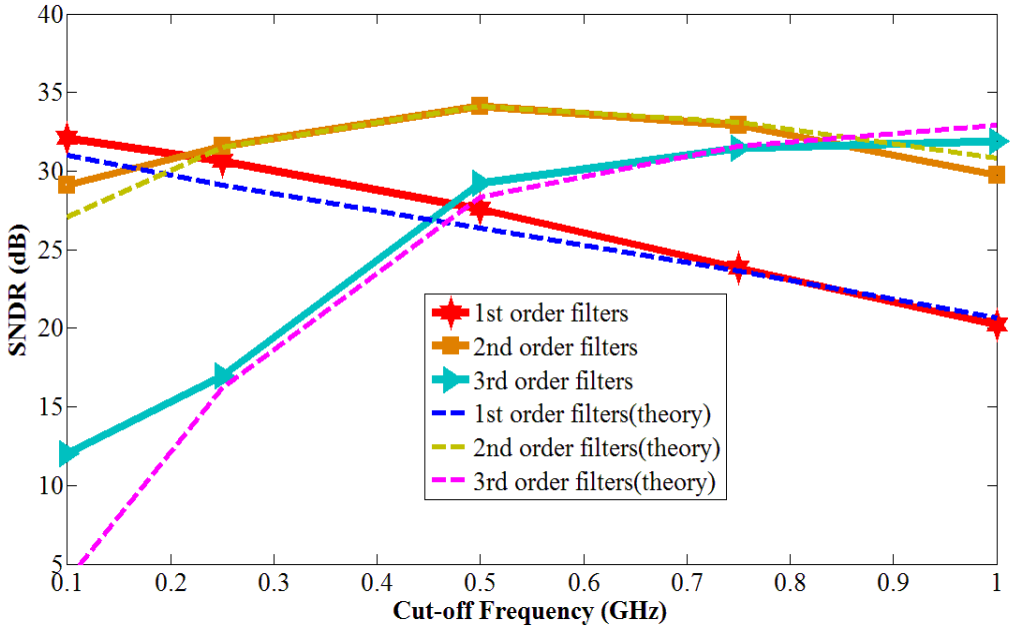

Fig. 32. Practical Simulation Results and Theoretical Results for 5 Channel Case.

Table 3 summarizes the results for the bandwidth optimized 5 channel receiver. It is evident from the table that a 3rd order filter of 1GHz bandwidth can be replaced by a 1st order filter of 100MHz without significant loss in the output resolution. This implies a huge amount of power savings in the receiver design.

Table 3: Summary of Performance Enhancement.

5-Channel Receiver with Optimized Filter Bandwidth (5 ps of jitter std. dev.)			
Parameter	Case-1	Case-2	Case-3
No. of Carriers	128	128	128
Carrier Spacing	78.125MHz	78.125MHz	78.125MHz
Sampling frequency in each path	2.5GHz(I and Q)	2.5GHz(I and Q)	2.5GHz(I and Q)
Filter order	1	2	3
Filter Cut-Off Frequency	100MHz	500MHz	1GHz
ENOB	4.697 bits	5.546 bits	4.7 bits

6. EFFECT OF LOCAL OSCILLATOR JITTER

As we have seen till now a multi-channel receiver has been proposed to improve the tolerance to jitter in the sampling clock. We have not taken into consideration the effect of jitter in the Local Oscillator (LO) signal. In this section we will analyze the effect of jitter in the LO's through simulations and ways to improve the receiver performance in the presence of LO jitter.

There are two basic types of LO signals that can be used in the receiver system, one is sinusoidal and other is square LO's. The effect of LO jitter will be analyzed in both the cases and different techniques will be put forward to make the LO jitter less dominant. The main issue with the LO jitter being dominant is that we lose the advantage we get by going multi-channel. Going multi-channel and then processing a band of the entire signal in each path at baseband gave the improvement in the tolerance to jitter and has increased the resolution achieved by the receiver. In the multi-channel receiver proposed in the previous sections, low pass filtering is followed by mixing operation which down converts different bands of signal to baseband. Then signal in each path goes through an ADC operating at a fraction of the total sampling rate. The improvement in the performance of the receiver depends on two factors, the amount of filtering applied to the out of band signal and number of paths used. We have seen that there was a clear relation between the order and bandwidth of the filter used in each path and the resolution achieved. The performance improvement that we achieved either by increasing filter order or reducing bandwidth was due to the reduction in the amount of high frequency content passing through the ADC at the end of the receiver chain reduced

the effect of jittery sampling clocks. This performance improvement would not be possible if some other noise source in the receiver dominates the effect due to sampling clock jitter.

The other possible noise source is the jitter or phase noise of the LO signals. When sinusoidal LO's are used we observed that the jitter in the LO does have an effect on the output resolution but effect of the jittery sampling clocks dominates it and therefore the performance improvement achieved by going multipath or in other words by reducing the amount of high frequency signal through the ADC is still intact.

Fig. 33 shows a comparative plot showing the effect of jitter in the sampling clock and sinusoidal LO separately. This was simulated for a 10 Channel case and the standard deviation of the jitter added is varied from 1ps to 6ps.

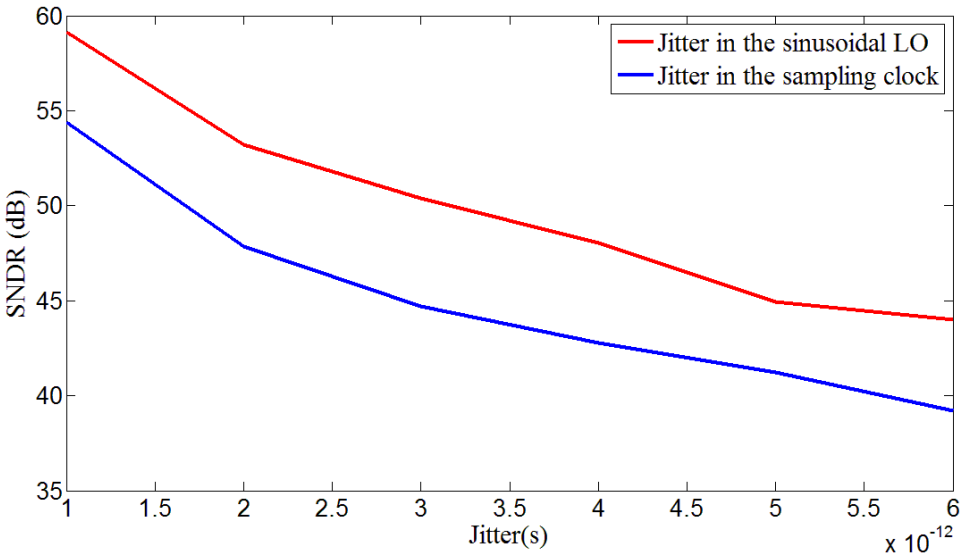

Fig. 33. Comparison of the Effect of Sinusoidal LO Jitter and Sampling Clock Jitter.

We can clearly see from Fig. 33 that when sinusoidal LO's are used the jitter in the sampling clocks dominates by a large amount and this would form the major source of error. Since the sampling clock jitter is the major source of error going multi-channel and attenuating the high frequency signal by use of high order filters improves the system's tolerance to jitter. As pointed out earlier the tolerance to jitter increases with the increase in number of paths.

As we know the mixers are easier to implement for square or switching LO. We now try to implement jitter in a square LO. Jitter is added to a square LO by added random gaussian distributed uncertainty in the significant edges of the signal or the rising and falling edges. Also practical cases would have a finite rise time for the square LO's and this is implemented by filtering the square LO by a butterworth filter of certain Bandwidth.

Fig. 34 shows the jittered LO's used in the receiver. The figure shows a square wave in red and a jittered square wave with finite rise time of 10 pico seconds in blue. In order to generate the jittered square wave we first generate a pure square and then find the zero crossings, once we have the zero crossings we add Gaussian amplitude distributed random noise of zero mean and the standard deviation we want the simulation to be done. This would generate the jittered LO but in order to implement finite rise time we need to filter the jittered LO and the best way to control the rise time without having to guess the bandwidth of the filter is to use a single pole Butterworth filter and by using the relation between rise time and bandwidth given below we can generate different LO signal with different rise times.

$$t_r = 0.35/BW$$

where t_r is the rise time and BW is the bandwidth of the Butterworth filter used.

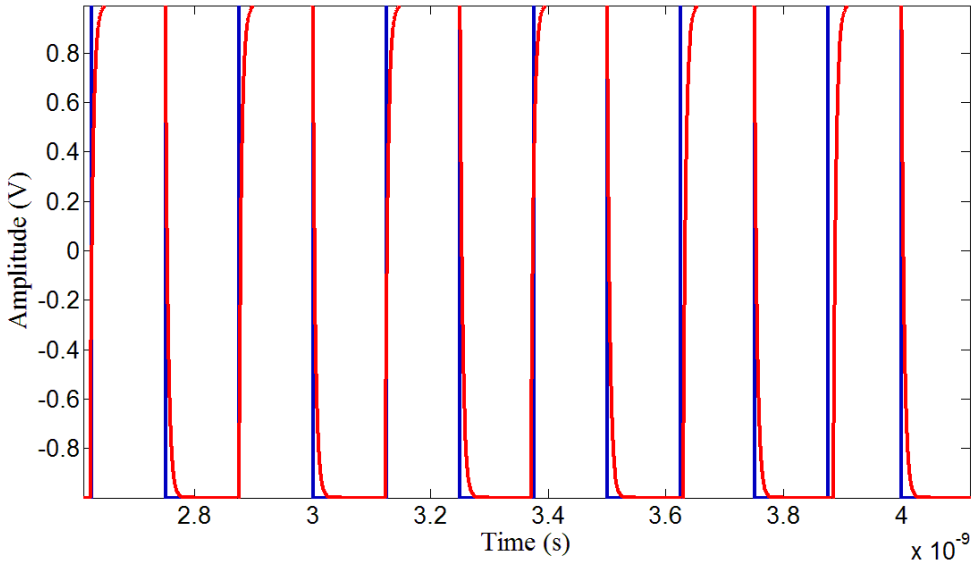

Fig. 34. Blue Shows the Ideal Square LO and Red the Jittered LO with Finite Rise-time.

Now using the jittery square LO's the receiver is simulated and we observed that the jitter in the square LO's dominates the resolution achievable at the output. In this case the tolerance we were able to get to sampling clock jitter would still be intact but it would be dominated by the error caused by the LO jitter.

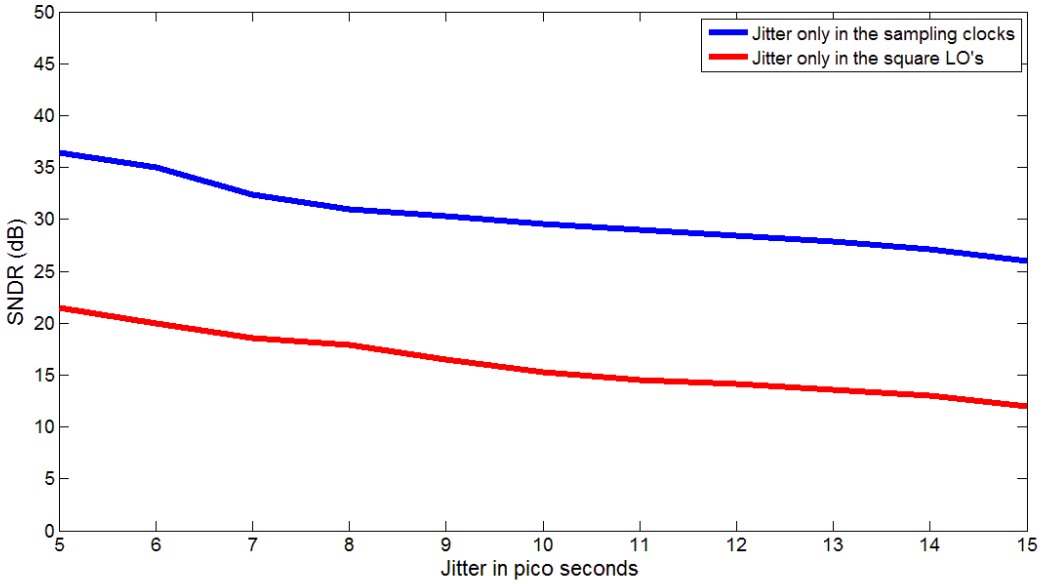

Fig. 35. Comparison of the Effect of Jitter in Square LO's and Jitter in Sampling Clocks.

Fig. 35 shows the comparative plot between the effect of jitter in the sampling clocks and LO's for a 10 Channel case with 2^{nd} order filters used in each path. We observe that for a 10 Channel case the LO jitter dominates the sampling clock by 15 dB. In this case going multi-channel for tolerance to sampling clock jitter would not be beneficial since the performance of the receiver is dominated by the jitter in the LO.

To prove this we compare the two receivers with 5 channels and 10 channels and with 2^{nd} order butterworth filters in each path. With the increase in the number of channels we would be expecting an increase in the output resolution but since the performance of the receiver is dominated by the jitter in the LO's there is no difference in the output resolution of the two receivers.

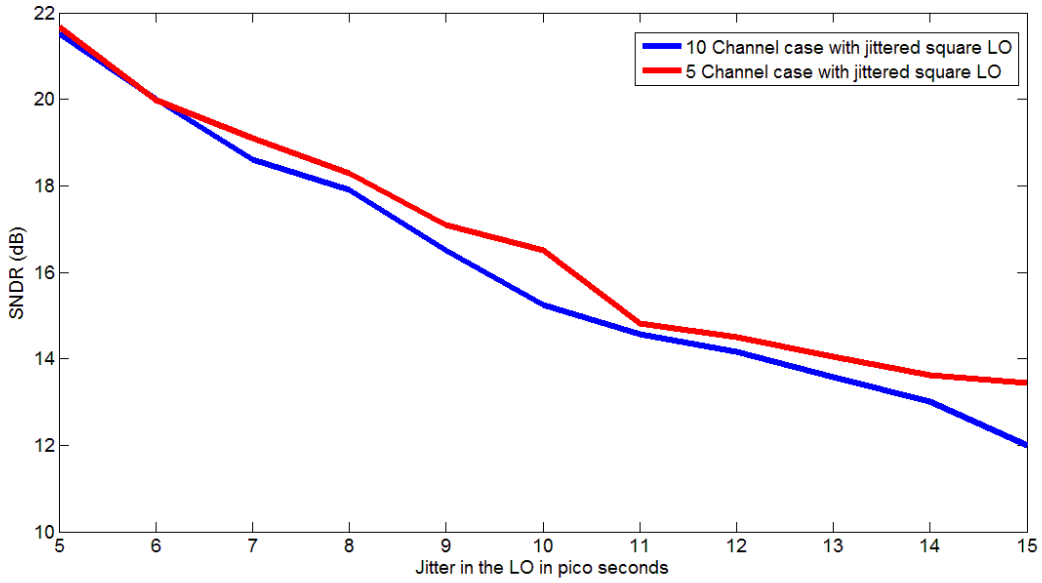

Fig. 36. Output Resolution vs Jitter with Square LO's for 5 and 10 Channel Receivers.

As Fig. 36 shows, the advantage of going multi-channel is negated by the huge impact the jitter in the LO has on the output resolution. In order to obtain better receivers which are tolerant to jitter we need to soften the effect of the square LO jitter on the output. For doing this a different implementation of the LO is required and care should be taken that the LO envisioned is still practically implementable. As we have seen performance of the receiver was mainly dictated by sampling clock jitter when the LO is sinusoidal, we can try to generate LO's which are neither square nor sinusoidal and are in between the two. For this we decided to implement a 3 bit LO which has 8 level in all. Such LO's have been implemented previously using multiple phases.

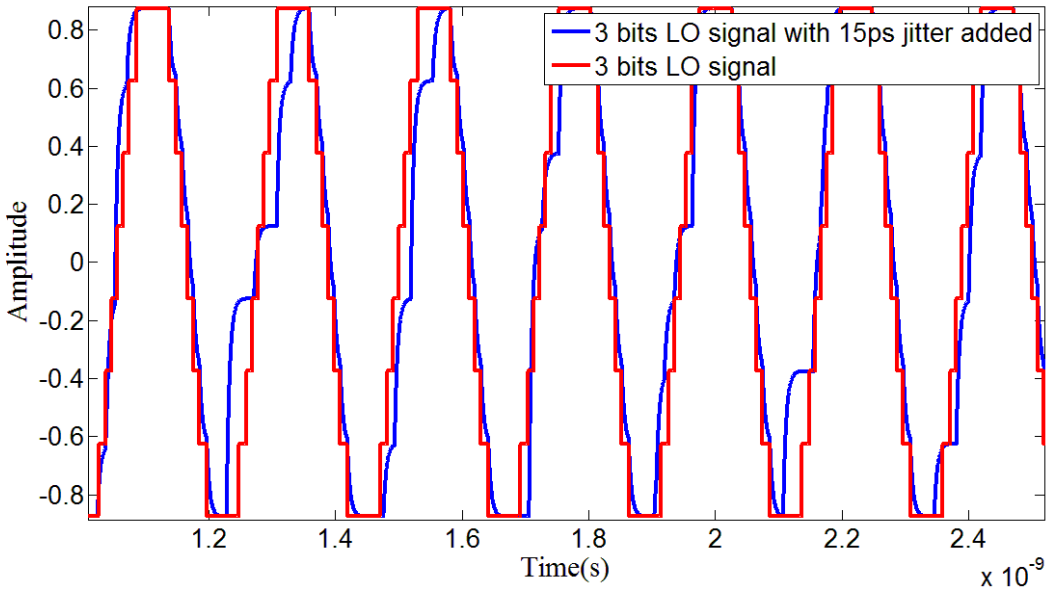

Fig. 37. 3 bit LO with 15ps Jitter and 10 ps Rise-time.

The LO jitter dominated when we used square LO's , this was mainly due to huge harmonic content of the square LO's and all the harmonics were responsible for noisy down conversion of the signal and thereby introducing lot of error in the system. In order to reduce this noisy aliasing due to harmonics of the LO we have to implement LO's with less harmonic content. Fig. 37 shows one such 3 bit LO generated with each of the multiple edges having a rise time of 10ps. In the practical implementation of such an LO , a number of switches would be operating to produce the required 3 bit LO and each of the switches would be adding some uncertainty in timing and therefore we attempt to model such uncertainty by added random timing jitter at each of the edges of such a signal. Such an LO would ideally have lesser harmonics when compared to the

square LO's and therefore leads to lesser noisy aliasing and increases the receiver's tolerance to jitter in LO.

Once we added the jitter and appropriate rise times for each of the edges we can now use the LO's in the receiver. Using the 3 bit LO's increased the output resolution of the receiver in the presence of LO jitter and made the effect of LO jitter and sampling clock jitter similar. Since the tolerance to LO jitter has been increased, going multi path would increase the resolution of the output and the increasing tolerance to sampling clock jitter with the increase in number of paths becomes clearly evident.

Fig. 38 shows the output resolution for a 5 channel receiver for the case of 3 bit LO's. We see that the performance of the receiver to jitter in LO and sampling clock are within 2 dB .

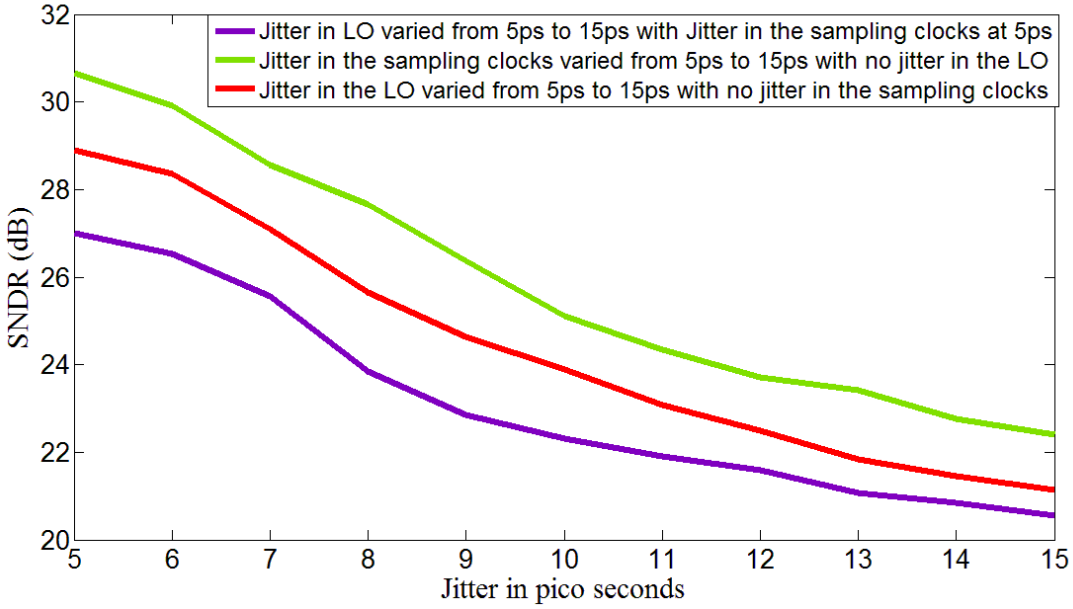

Fig. 38. Output Resolution as a Function of Jitter in LO and Sampling Clocks.

7. CONCLUSION

In this thesis, a complete system calibration scheme has been presented for the multi-channel Frequency-domain receiver based on *sinc* filter banks. This comprises of a Maximum-likelihood (ML) estimation of the frequency offset in the carriers followed by a normalized LMS calibration of all the static gain and phase mismatches in the receiver. It is shown that the reset in integration windows greatly simplifies the computation of the least squares (LS) estimate for the detection of symbols. Its complexity is comparable to that of the conventional FFT unlike multi-channel receivers with continuous filters where the computational complexity of the DSP block is several times higher than the multi-channel *sinc* filter bank.

Then a variation of the receiver structure is presented to exploits the relaxation of the clock-jitter specifications offered by multi-channel filter-banks. The new tools developed allow the optimal design of baseband multi-channel receivers with robustness to one of the most fundamental limitations in wideband communication receivers: clock-jitter. The design example of a multi-channel receiver can process a 5 GHz baseband signal with 40 dB of signal-to-noise-ratio (SNR) with sampling clocks that can tolerate up to 5 ps of clock-jitter standard deviation, enabling several transformative data communication applications. Existing architectures based on time-interleaving require 0.5 ps of clock-jitter standard deviation for those specifications, which has become a roadblock for future wideband communication receivers. Additionally, the receiver digital signal processing provides very low complexity multi-channel digital background calibration techniques that compensate critical circuit impairments.

The filters used in each of the paths of the receiver are bandwidth optimized to give the best performance. It was observed reducing the bandwidth of the filters in each path added a gain and phase error to the signal, which could be corrected through digital calibration, but increased the attenuation on the high frequency content of the incoming signal thereby improving the receiver's tolerance to jitter. The limit on the improvement that can be achieved through bandwidth reduction is placed by the noise amplification provided by the reconstruction problem which offsets the improvement in jitter tolerance.

The performance of the receiver with different types of Local Oscillator signals has also been verified. Use of square local oscillators made the jitter in the LO dominant when compared to the jitter in the sampling clock. This negates the improvement that can be achieved by having multiple channels, therefore a 3 bit LO is presented as a potential candidate which would have lesser harmonics and therefore lesser noisy aliasing and would therefore make the jitter in the sampling clocks and LO equivalent.

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