SHORT-TIME SCALE DYNAMIC FAILURE MODES IN A THROUGH-SILICON-VIA (TSV) FLIP-CHIP CONFIGURATION

A Thesis

by

CHANG-CHIA HUANG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2009

Major Subject: Mechanical Engineering

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Approved by:

Chair of Committee,	Chii-Der S. Suh
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ABSTRACT

Short-Time Scale Dynamic Failure Modes in a Through-Silicon-Via (TSV) Flip-Chip Configuration. (August 2009)

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The demand for high performance microelectronic products drives the development of 3-D chip-stacking structure. By the introduction of through-silicon-via (TSV) into 3-D flip-chip packages, microelectronic performance is improved by increasing circuit capacity and diminishing signal delay. However, TSV-embedded structure also raises concerns over many reliability issues that come with the steep thermal and mechanical transient responses, increasing numbers of bi-material interfaces and reduced component sizes. In this research, defect initiation induced by thermal-mechanical phenomena is studied to establish the early failure modes within 3-D flip-chip packages. It is found that low amplitude but extremely high frequency thermal stress waves would occur and attenuate rapidly in the first hundreds of nanoseconds upon power-on. Although the amplitude of these waves is far below material yielding points, their intrinsic characteristics of high frequency and high power density are capable of compromising the integrity of all flip-chip components. By conducting spectral analysis of the stress waves and applying the methodology of accumulated damage evaluation, it is demonstrated that micron crack initiation and interconnect

debond are highly probable in the immediate proximity of the heat source. Such a negative impact exerted by the stress wave in the early, while brief, transient period is recognized as the short time scale dynamic effect. Researched results strongly indicate that short-time scale effects would inflict very serious reliability issues in 3-D flip-chip packages. The fact that 3-D flip-chip packages accommodate a large amount of reduced-size interconnects makes it vulnerable to the attack of short time scale propagating stress waves. In addition, the stacking structure also renders shearing effect extremely detrimental to 3-D flip-chip integrity. Finally, several guidelines effective in discouraging short-time scale effects and thus improving TSV flip-chip package reliability are proposed.

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I also sincerely appreciate the valuable advice from my committee members, Dr. Muliana and Dr. Hurlebaus. Their insight and encouragement have helped define a roadmap for my future study.

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CHAPTER I

INTRODUCTION: SIGNIFICANCE OF RESEARCH

1.1 3-D Microelectronic Package with Through-Silicon-Via (TSV)

Over the past few decades, microelectronic package was driven by the demand for lower cost, smaller footprint, and increased electrical performance. The rationale to meet this need was to improve the circuit density in its limited packaging size. This has led to the 3-D microelectronic packaging technology. The 3-D microelectronic packaging technology based on chip-on-chip stacking and integration had the potential to provide high-performance integration of very-large-scale-integration (VLSI) semiconductor chips. Many product applications, such as the flip-chips and the system-on-package (SOP) products, were based on such technology.

When very high I/O interconnections are needed to interconnect these stacked chips, traditional packaging technologies such as advanced wire-bond chip stack packages do not support the I/O interconnection level needs. One of the new approaches to attain a 3-D structure and high-density I/O interconnections is the use of through-silicon-via (TSV) between the chips and silicon substrate. TSV, which is usually filled with copper, not only permits efficient area array signal, power, and ground interconnection through thin silicon wafers but also overcomes the RC delays of long,

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This thesis follows the style of Journal of Electronic Packaging.

in-plain wire connection by providing shorter out-of-plane path with less electrical blocks.

3-D microelectronic package based on the TSV technology provides several advantages in modular chip design flexibility and integration of heterogeneous technologies with performance exceeding that of single-chip integration. With a silicon carrier, each chip can be individually optimized for system performance and manufacturing yield. It also provides the foundation for new SOP products with electro-optic technology. The features of such packaging technology are both applicable and beneficial in commodities [1].

1.2 Reliability Issues in Flip-Chip Packages

High performance microelectronic devices with high density I/O interconnections operating at several giga-Hertz clock speed inevitably suffer serious heat dissipation which raises important reliability concerns. Due to the miniaturized component size and complex structures in 3-D flip-chip packages, the possibility for microcracking and delaminating is relatively high within packaged devices or along the dissimilar material interfaces when subjected to thermal-mechanical effect resulting from microelectronic operation. Such multiphysical coupling effect has been understood as the major reason for causing mechanical discontinuities that lead to eventual electronic disruptions. In order to improve packaging reliability and manufacturing yields, several testing methods are conducted to study the failure modes of IC package. Among the most commonly used methods are thermal cycling test and power cycling

test, in which IC packages are underwent pre-defined upper-lower bound temperature cycling in several hours to imitate practical microelectronic operation situation.

Recently, a new approach studying the correlation between early failure modes of IC package and thermal-mechanical phenomena during the first few sub-microseconds upon power-on is developed. Since damages observed in the new approach occur in such a short duration before the device reaching the steady-state operation temperature, these transient dynamic phenomena can be termed as the "short-time scale effects," while the long-time scale effects define the influences coming out after certain amount of operation cycles. A comparison of failure mechanism within flip-chip package referring to long-time and short-time scale effect is discussed in the followings.

1.3 Long-Time Scale Effect - Thermal Cycling Test

Thermally induced stresses have long been recognized as the crucial factor to the reliability of microelectronic packages. Most research on the reliability analysis of flip-chips argues that the accumulation of thermal stresses resulting from the mismatch of components with different coefficients of thermal expansion (CTE) causes IC packages failure. Based on the mainstream notation that the main mode of failure is a function of CTE, study about flip-chip reliability largely relies on the thermal cycling tests to quantify thermal stresses experienced by microelectronic products during their operational life span. Thermal cycling tests are carried out by thermally cycling IC packages in an environmentally heating chamber. A common cycle setting has the low

temperature set to -40°C and the high temperature to 135°C. However, environmentally heating chamber provides isothermal conditions in the whole package, which is far from the realistic electronic operation condition where internal heat dissipation of devices is locally distributed due to their compact size, modular construction and novel cooling solutions. Thus, an alternative test, power cycling test, was developed. In power cycling test, non-uniform heat is electrically generated by nature in the internal package assemblies. SEM is applied to inspect for thermally induced failures in samples after the cycling test.

In the past decades, many studies had been engaged in addressing thermal reliability issues of the 3-D electronic packages with running thermal cycling tests. Guatao Wang et al. [2] combined 3-D finite element analysis (FEA) based on a multilevel sub-modeling approach with high resolution Moire interferometry to investigate the interfacial delaminations under a thermal loading set from -55°C to 125°C. It was shown that packaging process induced thermal stresses could grow pre-existed cracks and lead to interconnect delamination - a severe reliability problem. R.G. Filippi et al. [3] conducted a thermal cycling test to study the failure mode of a stacked copper via structure in which cooper via failed resulting from the crack shearing through the entire via after 525 cycles. M. C. Hsieh et al. [4] employed an FEM model to demonstrate that packaging induced interfacial cracks in 3-D ICs significantly affect the distribution of thermal stresses in the TSV structure and could have prominent influence on their reliability.

1.4 Short-Time Scale Effect - Transient Analysis

However, thermal stresses obtained from thermal cycling tests show a level of merely a few thousands Pascal even subject to the most severe operating temperature, which is far from the yield point for the initiation of microcrack or bi-material interfacial delamination. Furthermore, several common failure mechanisms such as electromigration and solder joint fatigue are complex functions depending on spatial and temporal gradients of temperature [5]. Thus, any study of microelectronic package reliability without considering the effects from temporal and spatial gradient of temperature would be insufficient to describe the realistic physical phenomena. Several researchers have demonstrated the importance of performing transient analysis to microelectronic packages. Y.J. Min and Arthur L. Palisoc [6] studied transient temperature distribution of two-layer semi-infinite structures with embedded rectangular heat sources and predicted transient thermal response with respect to single and repeated impulse heat input. Lei L. Mercado et al. [7] adopted computational fluid dynamics (CFD) to obtain the thermal boundary conditions surrounding the plastic ball grid array which then were applied to evaluate the transient effects of thermal shock on die cracking. The transient analysis showed high stress distribution in the die due to thermal shock. Cemal Basaran et al. [8] presented an analytical model to predict stresses in multilayered microelectronic packaging devices subjected to thermal gradient loading and showed a higher stress level than the results obtained from isothermal conditions.

As the current development in microprocessors continuously increasing in clock speed and decreasing in component size, these high clock speed microelectronics are

subject to extremely large thermal gradient and temperature transient during power-on, which may cause considerable effects on the reliability of electronic packages. Thus, transient analysis of the reliability of IC packages needs to be narrowed to the time period of the first few sub-microseconds upon power-on. When clock speed approaches the gigahertz range, the cycle time would be as short as a fraction of a nanosecond, which implies that the thermal sweep associated with oscillatory current passing through the IC element requires a thorough thermo-mechanical analysis. It has been observed that the dynamic thermal-mechanical phenomena generated by short-time disturbances exhibit wave nature [9]. Mechanical fields induced by transient thermal input also perform in waveform. When the time scale is in the nanoseconds range, the generated thermal stress wave behaves as a high frequency shock wave which is capable of initiating micron cracks or interfacial adhesion flaws that would result in eventual electrical disruption and failure of the package when subject to operation cycling. Comparing to studies dealing with long-time scale effects, researches about how short-time scale effects correlate to the reliability of flip-chip packages are still comparably rare. Guo and Xu [10] studied the effect of non-Fourier heat conduction in IC chips and found that very short heat pulses led to large thermal failure rate. Ilegbusi, Coskun and Yener [11] conducted a thermal analysis on nanoscale electronic devices and concluded that short time scale thermal effects were significant in devices with feature lengths in the micron scale and would render the devices vulnerable. They also indicated that short-time scale effects may cause a sharp increase in the operating voltage and corresponding heat generation rate in nanoscale electronic devices. Włodzimierz Kalita

et al. [12] studied the dynamic temperature changes caused by electric pulses with high energy and short duration in microelectronic layered circuit and showed the pulse contributed to the local heating of the microstructure and resulted in the change of material properties or ultimate damage. Mahavir and Suh [9] indicated that short-time scale stress waves with high oscillating frequency carry extremely high volumetric power, termed as power density, that could initiate micron cracking along bi-material interface. Their results showed good correspondence with the prominent failure modes observed in IC chips. Yoonchan and Suh [13] studied short-time scale wave motions using a set of coupled electrical-thermal-mechanical field equations and evaluated the possibility of damage occurrence in flip-chip packages by relating the concept of power density to high-cycle fatigue test.

1.5 Research Objectives

The primary objective of this research is to establish and demonstrate that short-time scale effects induced during power-on dominate the early failure within the high performance 3-D TSV flip-chip package configuration. Failure mode and effect analysis (FMEA) of TSV flip-chip package as a result of thermal shock wave propagation will be studied. The theory of generalized thermoelasticity is employed to study the coupled thermo-mechanical waves in the TSV flip-chip package. A 2-D Green-Lindsay (GL) numerical model based on the generalized thermoelasticity is created to investigate the propagation of thermal and mechanical waves generated by a temperature impulse. The concept of power density (in Watt per cubic meter volume, $Watt/m^3$) and the

Accumulated Damage Evaluation method [13] is applied to predict the failure potential of the package. Finally, suggestions for negating short-time scale effects in TSV flip-chips is made to ensure improved reliability for 3-D IC packages.

CHAPTER II

THEORY OF THERMO - ELASTODYNAMICS

2.1 Basic Formulation

When a solid body is non-uniformly heated, each element in the body will expand by a different amount proportional to its own temperature rise. As the body must remain continuous and each element must restrain the distortions of its neighbors, the so-called thermal stresses arise. Based on the concepts of thermodynamics and mechanics, thermoelasticity is the subject studying the interaction of thermal stresses and temperature variation in a solid elastic body.

In order to fully demonstrate the thermo-elastodynamic phenomena in a TSV flip-chip package subjected to short-time scale effects, the theory of generalized thermoelasticity is employed in the research. The procedures of how generalized thermoelasticity is derived by modifying classical thermoelasticy is described in this chapter.

To incorporate the effect of temperature variation on stress distributions, first consider the equation of motion in the Cartesian coordinate:

$$\sigma_{ij,j} + \rho F_i = \rho \ddot{U}_i \tag{2-1}$$

where σ_{ij} is the stress tensor; ρ the density; F_i the body force vector; and U_i the displacement component. Assuming a linear relationship, the thermally induced strain is related to temperature variation as

$$\varepsilon_{ij}^{\ thermal} = \alpha_{ij}\theta \tag{2-2}$$

where $\varepsilon_{ij}^{thermal}$ is the thermally induced strain tensor; α_{ij} the coefficient of thermal expansion; $\theta = T - T_0$ is the temperature variation, with T being the absolute temperature and T_0 the datum temperature.

From the Hook's law, the mechanically induced strain in a linear elastic, isotropic, homogeneous material is:

$$\varepsilon_{ij}^{mechanical} = \frac{1}{2\mu}\sigma_{ij} - \frac{\lambda}{6\mu K}\sigma_{kk}\delta_{ij} \tag{2-3}$$

where $\varepsilon_{ij}^{mechanical}$ is the mechanically induced strain tensor, $\lambda = \frac{E\nu}{(1+\nu)(1-2\nu)}$ and $\mu = \frac{E}{2(1+\nu)}$ are Lame's constants; $K = \frac{E}{3(1-2\nu)}$, the bulk modulus, with Young's modulus, E , Poisson's ratio, ν , and the Kronecker delta, δ_{ij} .

The total strain is the sum of the thermally and mechanically induced strains:

$$\varepsilon_{ij} = \varepsilon_{ij}^{mechanical} + \varepsilon_{ij}^{thermal} = \frac{1}{2\mu}\sigma_{ij} - \frac{\lambda}{6\mu K}\sigma_{kk}\delta_{ij} + \alpha_{ij}\theta \tag{2-4}$$

By inverting the stress-strain relationship, a modified Hook's law is obtained:

$$\sigma_{ij} = \lambda\delta_{ij}\varepsilon_{kk} + 2\mu\varepsilon_{ij} - \beta\delta_{ij}\theta \tag{2-5}$$

where $\beta = (3\lambda + 2\mu)\alpha$ is the thermoelastic coupling constant. Assuming small deformations, so that

$$\varepsilon_{ij} = U_{k,l} \tag{2-6}$$

Substitution of the stress and strain tensors in Eq. (2-1) by Eqs.(2-5) and (2-6), Eq.(2-1) becomes:

$$(\lambda+\mu)U_{k,ki}+\mu U_{i,kk}-\beta\theta_{,i}+\rho F_i=\rho\ddot{U}_i \tag{2-7}$$

To include the effect of temperature variation on stress distributions, the theory of thermodynamics must be considered. First introduce the law of conservation of energy:

$$\sigma_{ij}\dot{\varepsilon}_{ij}-q_{i,i}=\rho\dot{e} \tag{2-8}$$

where $\dot{\varepsilon}_{ij}$ is the strain rate; q_i the heat flux vector; and e the internal energy density. The free-energy, φ, which is a function of strain tensor and temperature, is defined as

$$\varphi(\varepsilon_{ij},\theta)=e(\varepsilon_{ij},\theta)-\theta\eta(\varepsilon_{ij},\theta) \tag{2-9}$$

with η being the entropy density. For a body in rest, Eq.(2-8) can be expressed as

$$-q_{i,i}=\rho\theta\dot{\eta}=\rho\theta\left(\frac{\partial\eta}{\partial\varepsilon_{ij}}\dot{\varepsilon}_{ij}+\frac{\partial\eta}{\partial\theta}\dot{\theta}\right) \tag{2-10}$$

Substitution of $\dot{\varepsilon}_{ij}=0$, Eq.(2-10) becomes

$$-q_{i,i}=\rho\theta\dot{\eta}=\rho\theta\frac{\partial\eta}{\partial\theta}\dot{\theta}=\rho c_E\dot{\theta} \tag{2-11}$$

where c_E is the specific heat of the elastic material.

Substitution of Eqs.(2-9) and (2-10) into Eq.(2-8) leads to

$$\left(\sigma_{ij}-\rho\frac{\partial\varphi}{\partial\varepsilon_{ij}}\right)\dot{\varepsilon}_{ij}-\rho\left(\eta+\frac{\partial\varphi}{\partial\theta}\right)\dot{\theta}=0 \tag{2-12}$$

For a homogeneous isotropic material, the heat flux vector is:

$$q_i=-k\theta_{,i} \tag{2-13}$$

where k is the thermal conductivity. From Eq.(2-12), assuming $\sigma_{ij} = \rho \frac{\partial \varphi}{\partial \varepsilon_{ij}}, \eta = -\frac{\partial \varphi}{\partial \theta}$ and taking account of Eq.(2-13) leads Eq.(2-10) to the form:

$$k\theta_{,ii} = \rho c_E \dot{\theta} + \beta T_0 \dot{U}_{i,j} \tag{2-14}$$

Using del (∇) and Laplacian operator (∇^2), Eqs.(2-7) and (2-14) can be expressed as follows to define displacements and temperature variations in a thermal-elasto coupling field in the absence of body force,

$$\mu \nabla^2 U + (\lambda + \mu) \nabla \nabla \cdot U - \beta \nabla \theta = \rho \ddot{U} \tag{2-15}$$

$$\rho c_E \dot{\theta} + \beta T_0 \nabla U + \nabla \ddot{U} = k \nabla^2 \theta \tag{2-16}$$

2.2 Generalized Thermoelasticity

The conventional thermoelasticity, based on the classical Fourier's conduction law to describe heat transfer, allows the assumption of heat conduction with infinite speed in rigid materials. Such an assumption is physically inadmissible. Thus, Fourier's law fails to model rapid transient conduction process involving very short time scale or large temperature gradients as we are dealing with. In order to remedy the deficiency, wave-like thermal propagation of finite speed was proposed referred to as the second sound was proposed. In 1967, Cattaneo and Vernotte [14] modified the Fourier's law into a hyperbolic form by introducing a parameter called the thermal relaxation time to define thermal waves of finite propagation speed, which enables the modified conduction law to investigate physical thermal transport. Thermal relaxation time interprets the time-lag needed to reach the steady-state of heat conduction in a material

when a temperature gradient is suddenly imposed on it. For most common engineering materials, the value of relaxation time is found to be of the order of picoseconds that are comparably significant to the cycle time of microprocessors.

The concept of non-Fourier heat conduction law led to the theory of generalized thermoelasticity. Unlike the classical thermoelasticity, the novel theory derived from the knowledge of hyperbolic heat conduction imparts finite propagation speeds to thermal and mechanical waves generated by transient heat source. In 1972, Green and Lindsay introduced two different relaxation times for the mechanical and thermal waves to remedy the paradox of infinite heat wave propagation speed [15]. The modified relations among strain, stress, temperature variation, and entropy are listed below :

$$\begin{aligned} \sigma_{ij} &= \lambda\delta_{ij}\varepsilon_{kk} + 2\mu\varepsilon_{ij} - \beta\delta_{ij}(\theta + \tau_1\dot{\theta}) \\ q_i + \tau_2\dot{q}_i &= -k\theta_{,j} \\ \eta &= \eta_0 + c_E\theta + c_E\tau_2\dot{\theta} + \frac{1}{\rho}\beta\varepsilon_{ij} \end{aligned} \tag{2-17}$$

where η_0 is the entropy density at a reference state and τ_1 and τ_2 are relaxation times. By substituting Eq.(2-17) into Eqs.(2-1) and (2-10), the result is the Green-Lindsay (G-L) model of the theory of generalized thermoelasticity, which can be written as:

$$\begin{aligned} \rho\ddot{U} - (\lambda+\mu)\nabla\nabla\cdot U - \mu\nabla^2 U + \beta(\nabla\theta + \tau_1\nabla\dot{\theta}) = 0 \\ \rho c_E\tau_2\ddot{\theta} + \rho c_E\dot{\theta} - k\nabla^2\theta + \nabla\ddot{U} + \beta T_0\nabla\dot{U} = 0 \end{aligned} \tag{2-18}$$

The G-L model is characterized by a system of partial differential equations. It is seen in the model that the entropy and heat flux depend not only on the temperature variation but also on the temporal gradient of the temperature. That is, the model is

sensitive to transient temporal variation, thus selected for the study of short-time scale effect.

2.3 Discussions

Besides the G-L model reviewed above, several thermoelastic models have been developed to describe the thermal-mechanical coupling phenomena over the past few decades [14]. Lord and Shulman first introduced in 1967 a model with a single thermal relaxation time before Green and Lindsay presented theirs. In 1996, Hetnarski and Ignaczak modified the classical heat conduction of the Fourier law by introducing a low-temperature parameter to study thermoelastic waves propagating in a low-temperature media. The model by Green and Naghdi admitting the propagation of undamped thermoelastic waves was named thermoelasticity without energy dissipation [16]. The dual-phase-lag model proposed by Chandrasekharaiah and Tzou [17] replaced the Fourier's law by a Taylor series approximation of the modified Fourier's law with two different time translations - a phase-lag coefficient of heat flux and a phase-lag coefficient of the temperature gradient. In a recent publication, an additional phase-lag coefficient of displacement gradient following Chandrasekharaiah and Tzou's was interpreted by S. K. Roy Choudhuri to formulate a three-phase-lag thermoelastic model [17].

Although all admit coupled thermo-mechanical waves propagating with finite speed, the feasibility of these models is controversial on account of the conformity with the fundamental laws of thermodynamics and the agreement with the physically realistic

conditions. Wegner et al. [18] and Suh and Burger [19] argued that the L-S model violates the entropy inequality at the fundamental level while the G-L model does not. Chandrasekharaiah [14] observed a discontinuity of displacement when the material was subjected to a continuous mechanical load which violates the continuum hypothesis. The G-N model does not provide physical relevance to the existence of undamped thermal waves when most engineering materials possess a high damping rate [16].

In this research, the G-L model is adopted since it does not violate the entropy inequality and considers the attenuation of waves, unlike the L-S and G-N models. Moreover, comparing to the difficulty of obtaining the phase-lag coefficients in the C-T model, the G-L model is the only theory that has been shown to provide a manner to attain physically admitted magnitudes of the thermal and mechanical relaxation times [19]. The G-L model have been successfully used to predict short-time scale heat transfer in many areas, such as laser heating and wave propagation in IC package [9, 19, 20].

CHAPTER III

DESCRIPTION OF FINITE ELEMENT MODEL

3.1 Model Geometry and Constituent Materials

Although various kinds of experimental approach, such as the thermal cycling test, and power cycling test, were designed to study the thermally induced reliability issues in IC packages, it is still infeasible to conduct an experimental analysis on short-time scale effects due to the practical deficiency of technology to capture waveforms propagating in a IC package at the giga-hertz level. Hence, a finite element analysis (FEA) model is required to "virtually" study the topic. In this research, an FEA model of a 4-layer stacked flip-chip package with TSVs is established to study short-time scale wave propagation in 3-D microelectronics.

The structure of 4-layer stacked flip-chip package configuration adopted from Ref. 21 is shown in Fig. 3.1. Four ultra-thin (50 μm) silicon dies are vertically stacked and attached to the silicon substrate with lead-free Sn/Ag/Cu micro-bumps. The silicon substrate is directly attached to a PCB testboard by Sn/Ag/Cu solder balls. The TSVs, which are filled with copper, are designed to connect micro-bumps between two adjacent silicon dies directly. The micro-bumps are enclosed by underfills which fill the gaps between silicon dies. Geometric dimensions and constituent material properties of the 4-layer stacked flip-chip package are shown in Table 3.1 and 3.2 respectively.

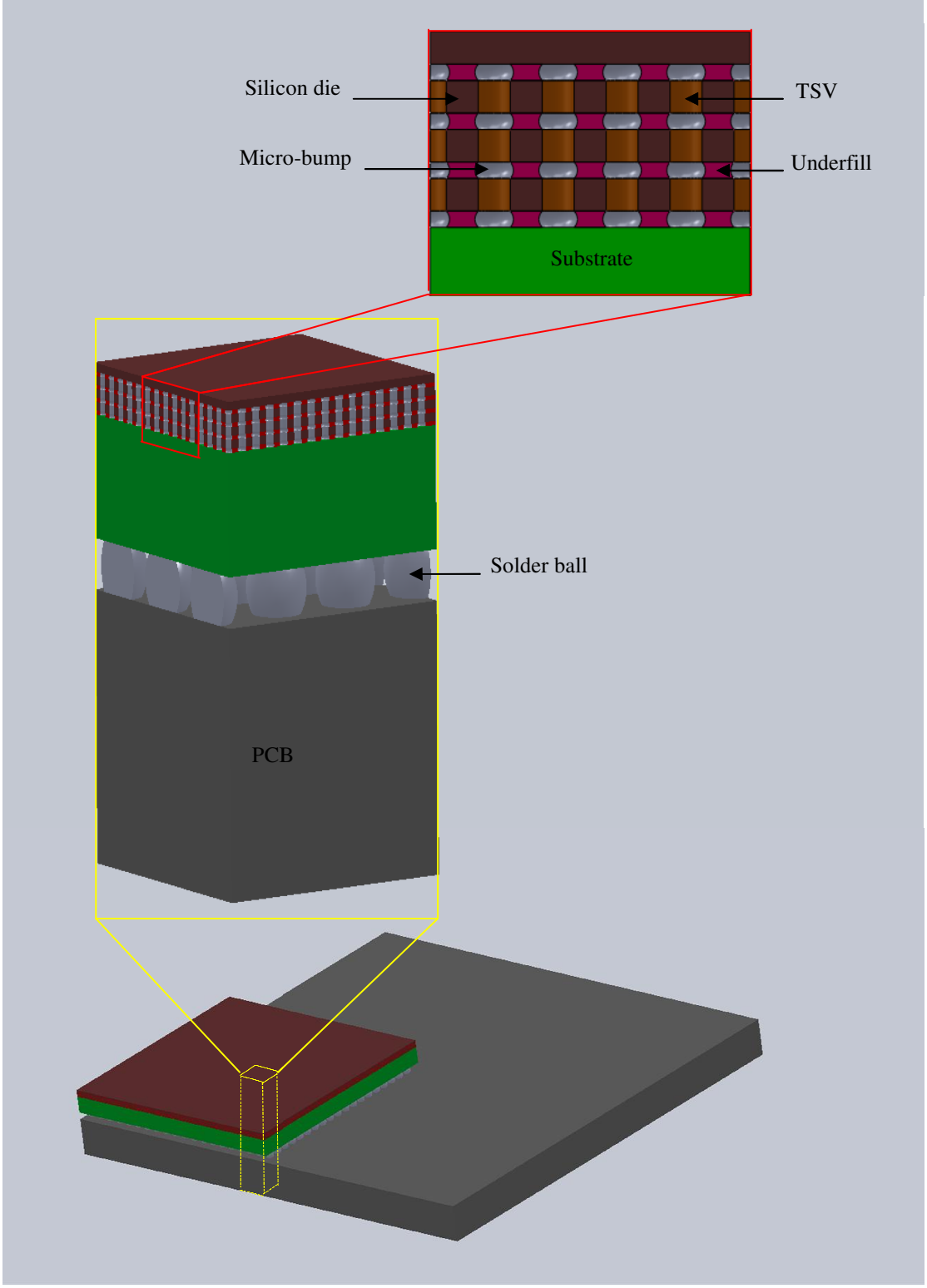

Fig. 3.1 4-layered TSV flip-chip package configuration

Table 3.1 Geometric dimensions

Dimensions	Length (mm)	Width (mm)	Height (mm)
Silicon die	10	10	0.05
Substrate (silicon)	10	10	0.725
PCB testboard	20	20	1.6
Dimensions	Diameter (mm)	Height (mm)	Pitch (mm)
Micro-bump	0.05	0.025	0.1
Solder ball	0.3	0.3	0.5
TSV	0.05	0.05	0.1

Table 3.2 Material properties

Material Properties	Cu	Si	Solder	Underfill	Substrate
CTE ($ppm/°K$)	17	2.3	21	20	18
E (GPa)	120.5	165	32	6	22
Poisson's Ratio	0.35	0.22	0.4	0.35	0.28
Density (kg/m^3)	8940	2330	8470	6080	1938
Specific heat ($j/kg \cdot K$)	380	700	151	674	879
Thermal Conductivity ($W/m \cdot K$)	401	155	51	1.6	13

3.2 Assumptions Made

Ideally, a whole 3-D FEA model can provide a complete visualization of the short-time scale phenomena in the TSV flip-chip package. However, the memory requirements for small integration time steps and complex-structure simulation are extreme. Thus, an idealized 2-D FEA model is employed instead. The hexahedral section having two of its sides along the planes of symmetry of the 4-layer TSV flip-chip configuration as seen in Fig. 3.2 is selected for defining the model domain. The governing equations of the 2-D FEM model can be derived from the G-L model as:

$$\begin{aligned}
&\rho c_E \tau_2 \frac{\partial^2 \theta}{\partial t^2} + \rho c_E \frac{\partial \theta}{\partial t} - k\left(\frac{\partial^2 \theta}{\partial x^2} + \frac{\partial^2 \theta}{\partial y^2}\right) + \frac{\partial^2}{\partial t^2}\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right) + T_0 \beta \frac{\partial}{\partial t}\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right) = 0 \\
&\rho \frac{\partial^2 u}{\partial t^2} - (\lambda + 2\mu)\frac{\partial^2 u}{\partial x^2} - \mu \frac{\partial^2 u}{\partial y^2} - (\lambda + \mu)\frac{\partial^2 v}{\partial x \partial y} + \beta \frac{\partial}{\partial x}\left(\theta + \tau_1 \frac{\partial \theta}{\partial t}\right) = 0 \\
&\rho \frac{\partial^2 v}{\partial t^2} - (\lambda + 2\mu)\frac{\partial^2 v}{\partial y^2} - \mu \frac{\partial^2 v}{\partial x^2} - (\lambda + \mu)\frac{\partial^2 u}{\partial x \partial y} + \beta \frac{\partial}{\partial y}\left(\theta + \tau_1 \frac{\partial \theta}{\partial t}\right) = 0
\end{aligned} \tag{3-1}$$

where u and v are displacement variables in direction-1 and 2, and θ is the variable of temperature variation.

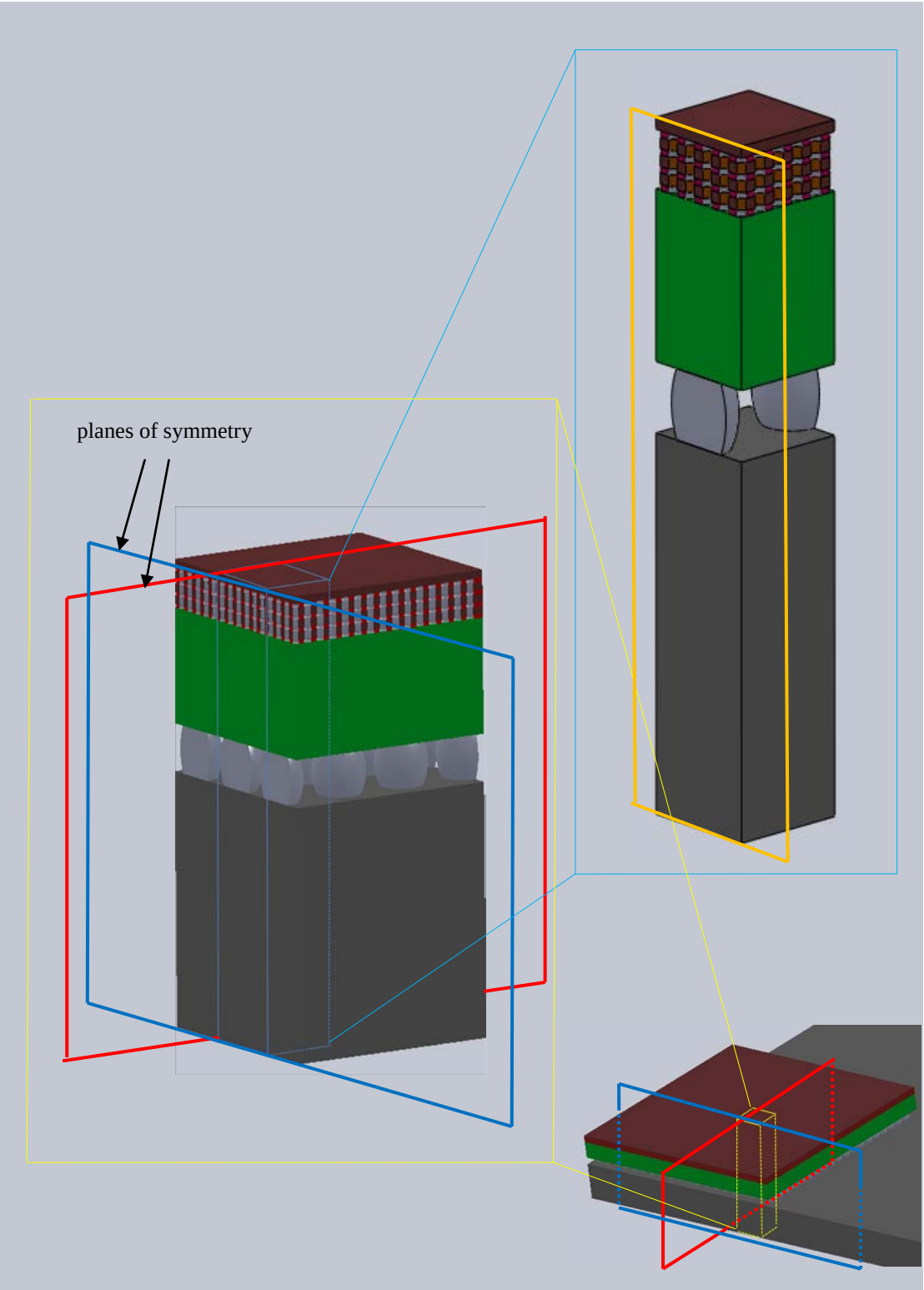

Fig. 3.2 Model simplification for numerical analysis

It should be noted that although silicon is anisotropic, the isotropic assumption made of the 2-D silicon model is valid given its small thickness. As they do not respond to thermal stress waves of very high frequency, the viscoelastic underfill material is assumed to be elastic.

A temporal-temperature impulse shown in Fig. 3.3 is chosen to model the joule heating from electrical junctions during power-on. The temperature profile of the heat source is characterized by a Gaussian function as follows

$$f(t) = ae^{-\frac{(x-b)^2}{2c^2}} \tag{3-2}$$

where a and c are constants chosen to control the peak amplitude, and b is the rise time of the function. Assuming a 2.5 GHz microprocessor clock speed, the time period of the joule heating is thus 0.4 ns. The heat source is assumed to reach a peak temperature at $0.001\,°C$ at 0.2 ns.

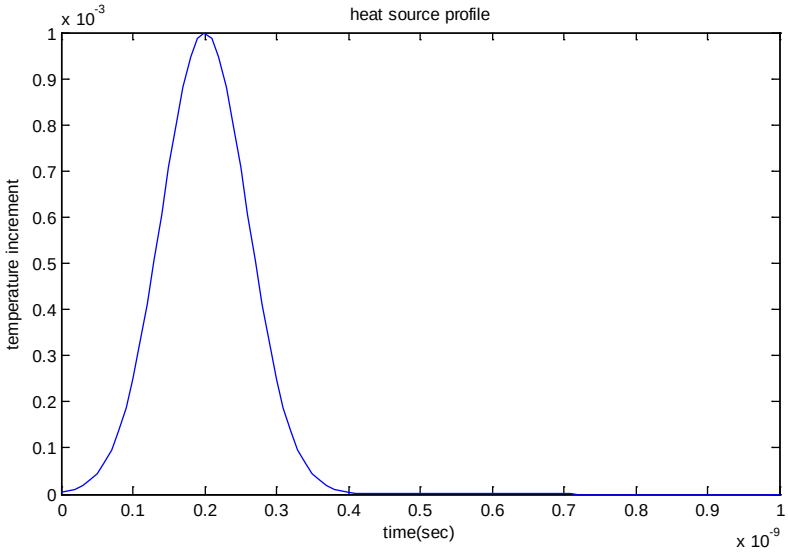

Fig. 3.3 Gaussian heat impulse

In this research, COMSOL MULTIPYSICS, a commercial FEM software marketed by Comsol Inc., is employed to conduct numerical simulation. Unlike most commercial FEM software, COMSOL MULTIPYSICS allows the users to define governing equations in the model domain. COMSOL MULTIPYSICS also do well in solving PDE problems, which facilitate the studying of the G-L model equations since the objective of this research is to investigate the physical phenomena in the flip-chip package, not in the mathematical realm.

3.2.1 Boundary Conditions

Appropriately setting boundary conditions can improve calculating efficiency and keep the result closer to the realistic situation. There are 4 types of boundary in the 2-D FEM model in this research. The considerations in accordance with the boundary conditions are shown in Fig. 3.4 and specified as follows:

1. Left-hand-side boundary: since the boundary is on the plan of symmetry, the horizontal displacement, u, is therefore zero.
2. Right-hand-side boundary: no constraints are imposed on this side to keep the temperature and displacement fields continuous.
3. Top and bottom faces and the exposed faces of solder balls: temperature waves are expected to be negligible when arriving at these exterior boundaries. It is valid to assume that there is no temperature variation along these boundaries. A datum temperature T_0 $(\theta = 0)$ is given to them.
4. Interior boundaries: no constraints are imposed.

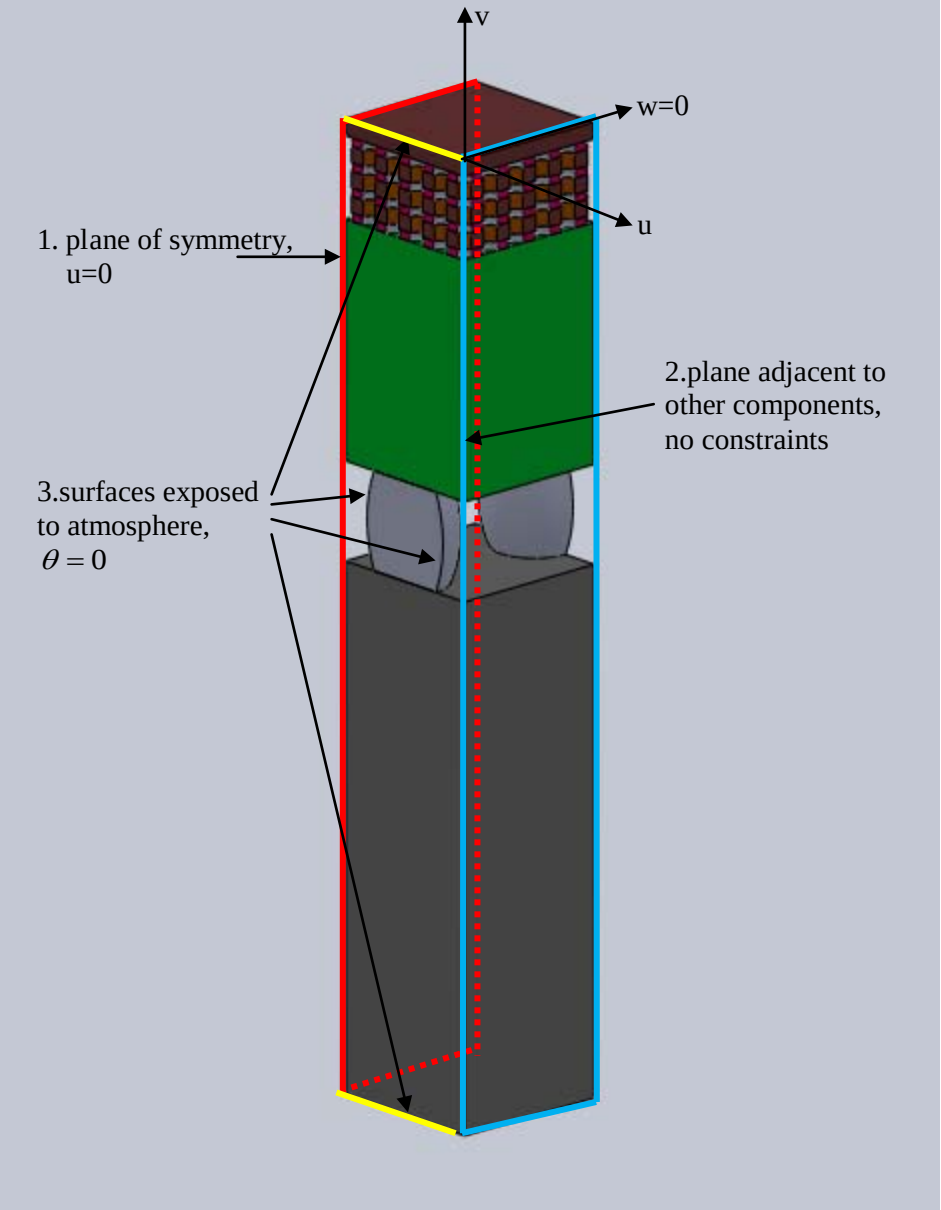

Fig. 3.4 Boundary conditions of the 2-D FEM model

3.2.2 Time Step Chosen

A time window of 0.1 microseconds is chosen to investigate the short-time scale effects in the TSV flip-chip model configuration upon power-on. A rigorous time step of 1 picosecond is followed to ensure solution convergence when solving Eq. (3-1).

3.2.3 Convergence Tolerance

The software built-in convergence condition dictates that the solution of a time step calculation is accepted if $(\frac{1}{N}\sum_i(\frac{|E_i|}{A_i + R|U_i|})^2)^{\frac{1}{2}} < 1$, where U_i is the variable, N is the number of steps, E_i is the solver's estimate local error, A_i is the absolute tolerance at DOF i, and R is the relative tolerance. The absolute tolerance is chosen to be 1.0E-11 and the relative tolerance is 0.0001.

3.2.4 Model Validation

Before proceeding to generate numerical results, it is important to validate the established FEM model. Although the TSV flip-chip configuration is a complex structure consisting of five materials, the model can be validated by simply checking if the calculated speeds of the longitudinal waves agreed with the theoretical values. The longitudinal wave propagation speed in a semi-infinite isotropic elastic material can be estimated using $C = \sqrt{E/\rho}$, where E is the elastic modulus and ρ is the material density. The longitudinal wave speed in silicon material for which E = 131 GPa and ρ = 2330 kg/m^3 is therefore 7498.2 m/s. Thus, the theoretical time of flight for the longitudinal

wave to cover the propagation path shown in Fig. 3.5 is 3.33ns. The longitudinal stress waveform σ_{22} acquired at the end of the 0.025 mm propagation path is seen to arrive at approximate 3ns in Fig. 3.6, thus validating the FEM model.

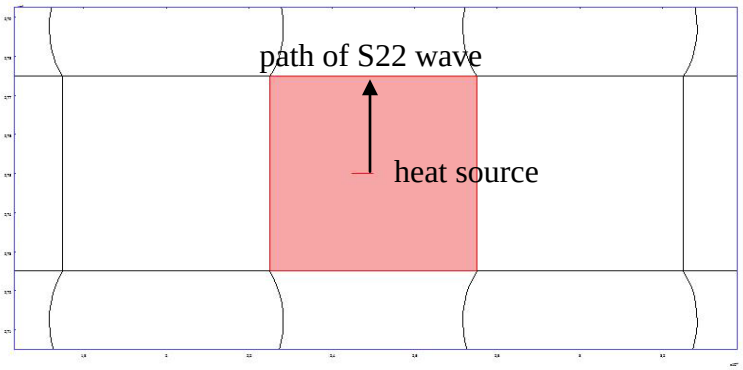

Fig. 3.5 Acquisition point and propagation path for model validation

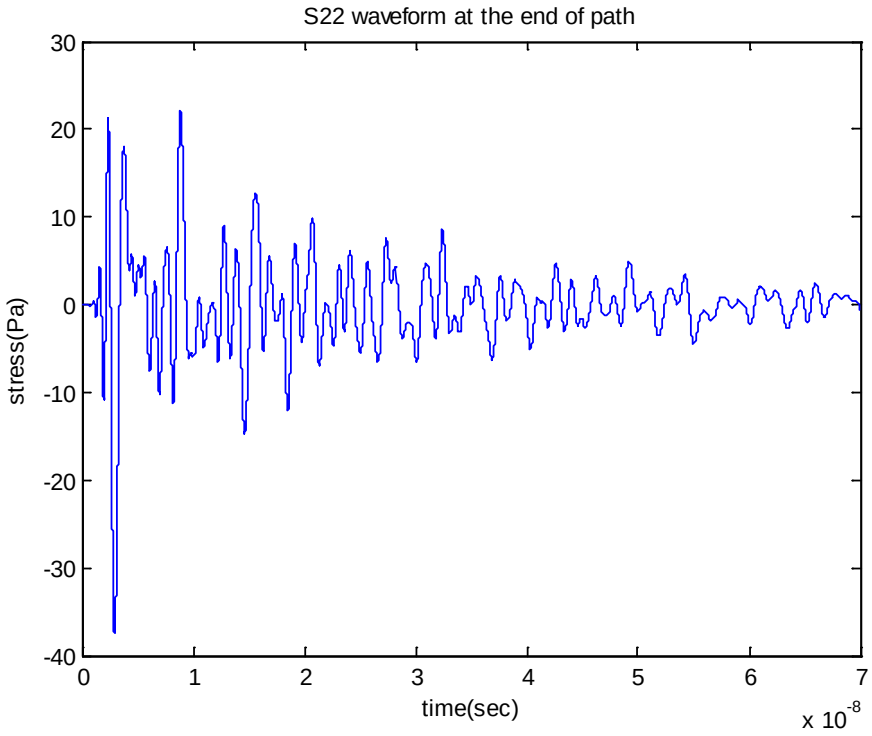

Fig. 3.6 Acquired σ_{22} waveform for model validation

CHAPTER IV

SHORT-TIME SCALE EFFECTS IN TSV FLIP-CHIP CONFIGURATION

4.1 Selection of Waveform Acquisition Position

In Fig. 4.1, a heat source is placed at the center of the third silicon die. Thermal-mechanical disturbances resulting from the heat impulse are studied to characterize short time scale effects in the TSV flip-chip configuration. To obtain fully developed waveforms, 24 waveform acquisition locations in two neighboring TSVs along with their connected micro-bumps shown in Fig.4.1 are chosen to investigate the behaviors of stress waves and the corresponding power density waves. The temperature, shear and normal stress waveforms, T, S12, and S22, respectively, are acquired at locations where the probability of low reliability is high. Twelve bi-material interfaces shown in Fig. 4.2 are selected to conduct shear stress analysis where dominant delaminating damages might result from mismatch of dissimilar materials. Locations 1, 3, 4, 6, 7, 9, 10 and 12 are along the interfaces of four constituent materials; namely, the silicon die, TSV, micro-bump, and underfill. Locations 2, 5, 8, and 11 also need to be concerned with since former researches have indicated that the bonding of TSV with micro-bumps might be fragile due to being on the electrical path which is directly impacted by current flow. Fig. 4.3 indicates the locations where failure might initiate due to normal stresses in direction-2. Because the distribution of TSV flip-chip components in Fig. 4.1 is symmetric about the heat source location, stress waves acquired at mirrored locations will be of identical characteristics. To study the detail of wave behaviors in such a

transient period, the observing time window is limited to 0.1 microseconds. The acquired waveforms for the full duration at each location are shown in the following sections.

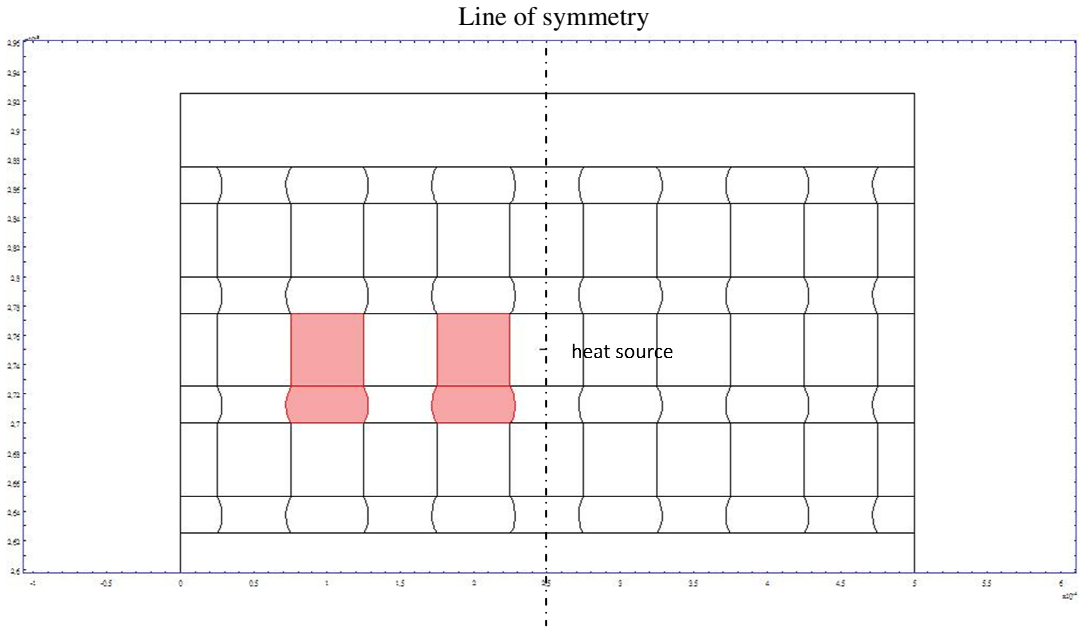

Fig. 4.1 Selected components in TSV flip-chip for waveform acquisition

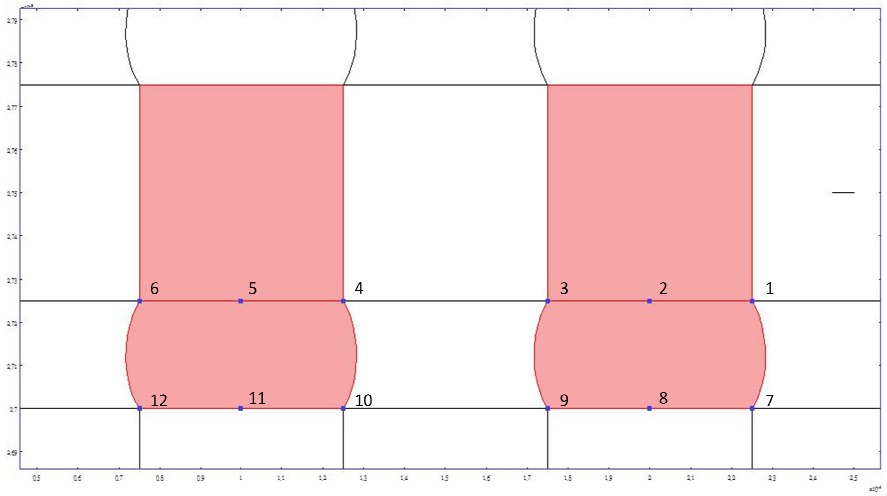

Fig. 4.2 Shear stress wave acquisition locations

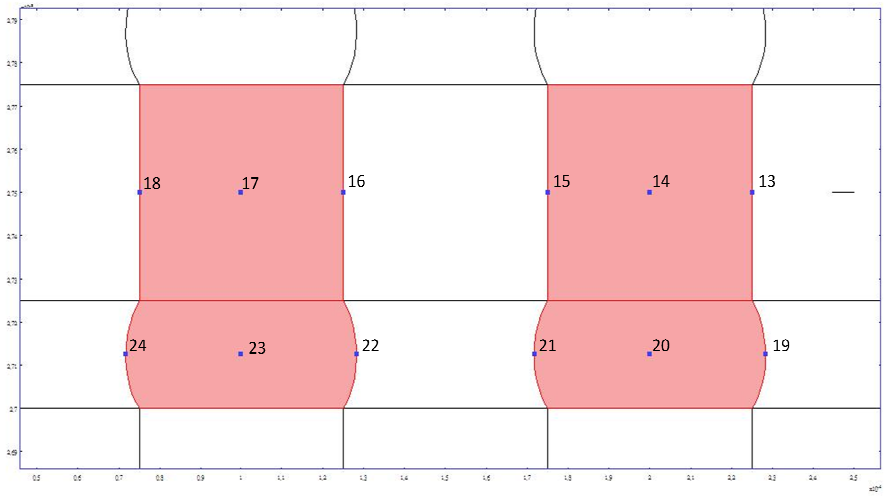

Fig. 4.3 Normal stress wave acquisition locations

4.2 Temperature Waves

Figs. 4.4 and 4.5 give the thermal waves acquired at Locations 13 and 16. It can be seen that the magnitude of temperature increment in the TSV flip-chip configuration is small - a mere $3\times10^{-7}\ ^{\circ}C$ in magnitude at Location 13 when subjected to a $0.001\ ^{\circ}C$ thermal impulse. Thermal waves also attenuate quickly in approximately 20 nanoseconds. Thermal waves acquired at other locations display similar characteristics. Since temperature distribution has long been recognized as the reliability parameter of microelectronics, short-time scale effects have not been taken seriously before due to their low-magnitude and rapid-attenuative temperature waves. However, when temperature variation in time is considered, the corresponding power ($\frac{\partial\theta}{\partial t}$) generated by such a temporal oscillation is prominent. Figs 4.6 and 4.7 show the corresponding $\frac{\partial\theta}{\partial t}$ at Locations 13 and 16. The peak power at Location 13 is in the MW range and is in average two order-of-magnitudes higher than that of Location 16. Temporal thermal gradient - the essence of short-time scale effects, provides a different perspective of the otherwise seemly harmless thermal wave propagation. One might be deceived into arguing that given its fast attenuation, the high power is inconsequential, thus not to be concerned with. It will be seen in the following sections that the temporal oscillations of the thermally induced stresses are so prominent that, though also highly attenuative, they are high both in frequency and power density, and thus extremely detrimental to the TSV design.

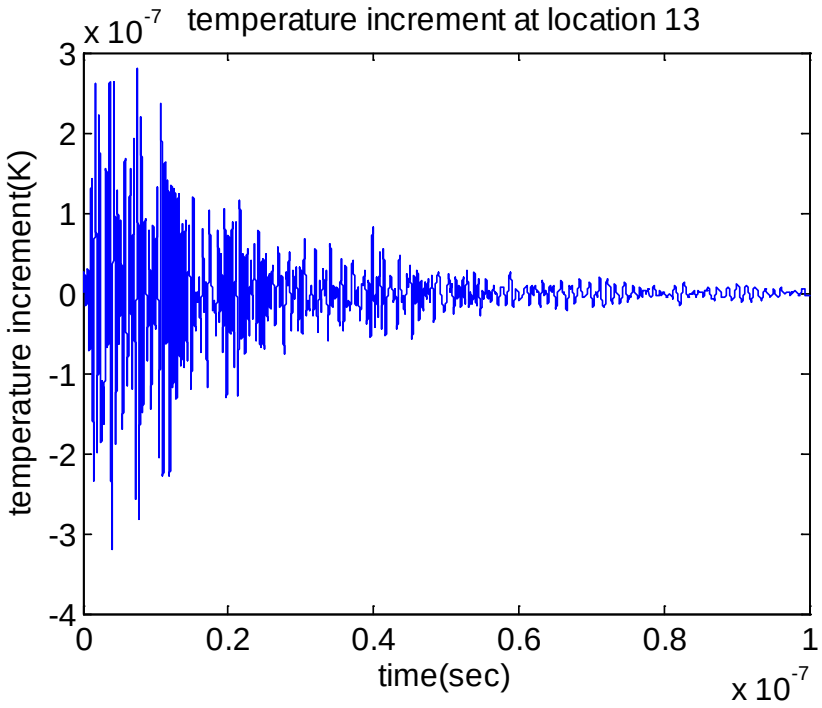

Fig. 4.4 Temperature increment at Location 13

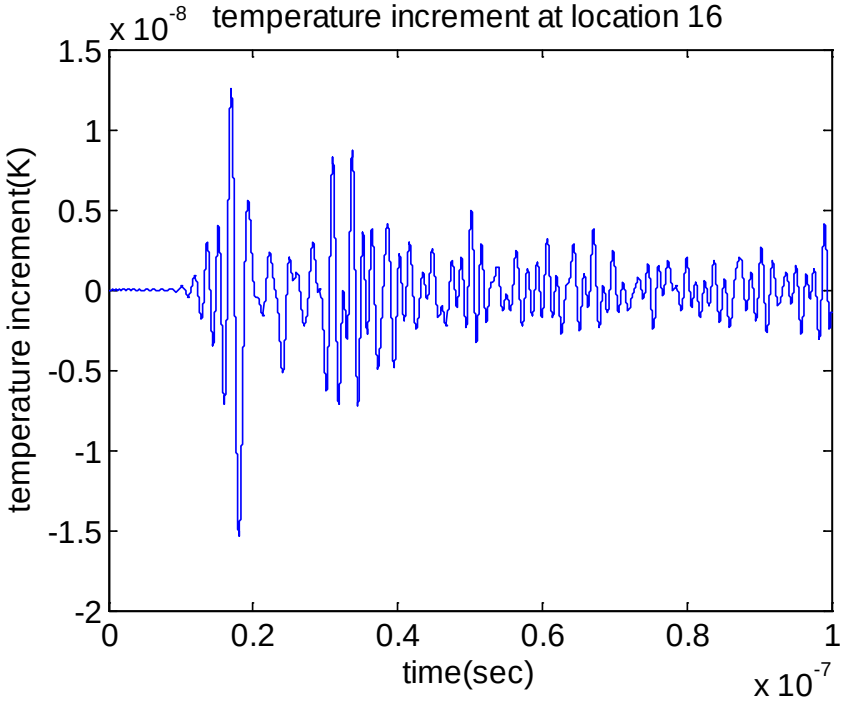

Fig. 4.5 Temperature increment at Location 16

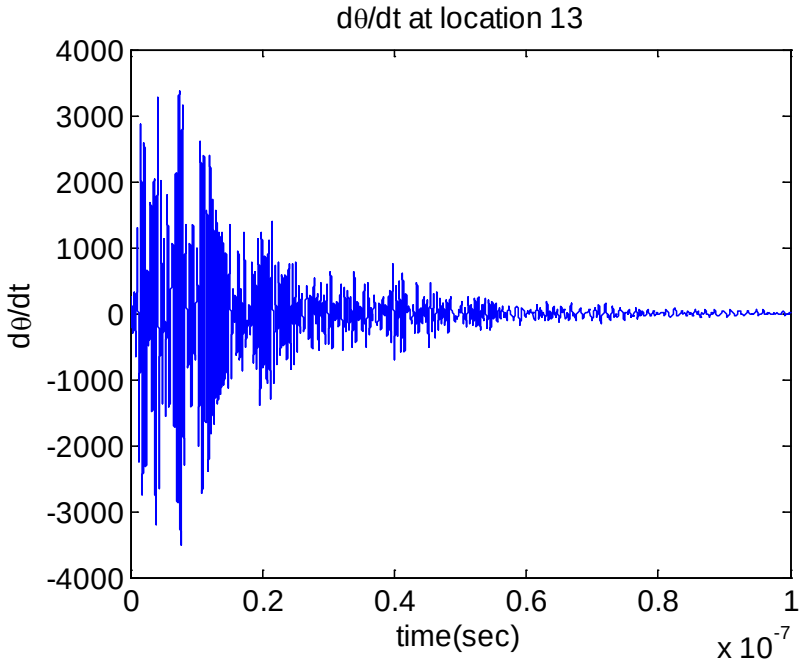

Fig. 4.6 Temporal thermal oscillation $\frac{\partial \theta}{\partial t}$ at Location 13

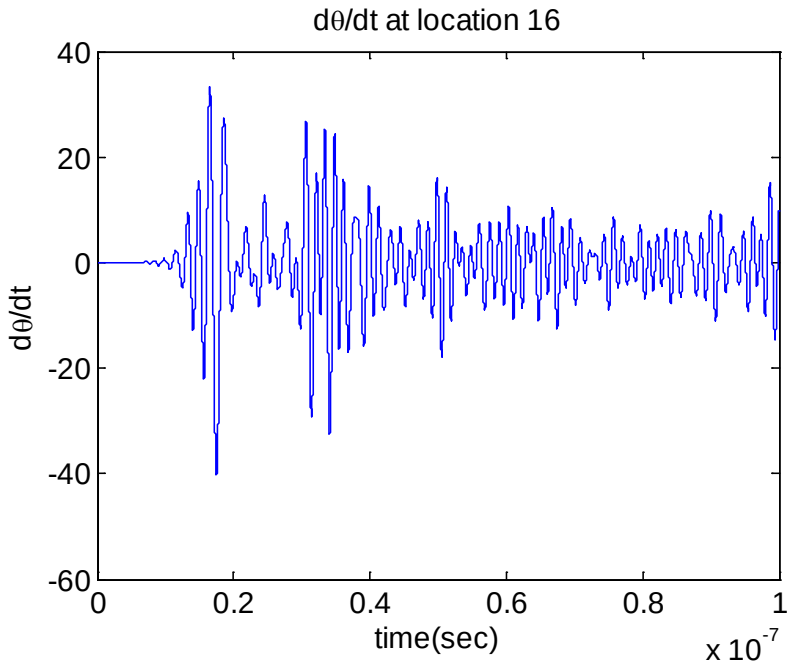

Fig. 4.7 Temporal thermal oscillation $\frac{\partial \theta}{\partial t}$ at Location 16

4.3 Stress Waves Propagation

4.3.1 Short-Time-Fourier-Transform (STFT) Analysis

In Chapter I it was established that there were dispersive and rapid-attenuating stress waves propagating in electronic package within a very short duration upon power-on. As thermal waves are small in magnitude, one expects the same of the thermal stress waves in the TSV flip-chip configuration. To extract more information from the acquired stress waves, it is necessary to conduct time-frequency analysis to the time waveforms. The Short-Time Fourier Transform (STFT) is employed in the research for its innate good temporal and spectral resolutions. A brief review of the STFT is given below. For a given function $f(t)$, STFT first modulates $f(t)$ by a window function $\phi(t)$ at a specific time $t = b$ to produce a windowed function $f(t)\phi(t-b)$ and then takes the

Fourier Transform of the modulated function. The STFT of function $f(t)$ using a Gaussian window function can be mathematically expressed as:

$$F(\omega_n, b_m) = \int_{-\infty}^{+\infty} f(t)\phi(t-b_m)e^{-iw_n t}d \equiv \sum_{k=0} f(k\Delta t)\phi(k\Delta t - b_m)e^{-iw_n(k\Delta t)}\Delta t$$

where $\phi(t) = \frac{1}{\sqrt{2\pi\sigma}}e^{\frac{-t^2}{2\sigma^2}}$ and $\int_{-\infty}^{+\infty}\phi(t)dt \neq 0$, with σ being the width of the window function. The Fourier Transform of $f(t)\phi(t-b_m)$ is taken as the window sliding along the time axis, resulting in a temporal-spectral representation of the signal.

4.3.2 Shear and Normal Stress Waves

Figs. 4.8 through 4.19 are shear stress (σ_{12}) waveforms and their STFTs at Locations 1 to 12. The maximum shear stress induced by the heat shock is 6 Pa and as expected attenuates quickly in several nanoseconds. The highest frequency approximately 1 GHz arrives in 4 ns at Location 1 then disperses rapidly to about 500 MHz. A peak frequency around 500 MHz can be seen in all figures. In Figs. 4.14 through 4.17, more than one peak frequency is observed in the time window, signifying that the waves are followed by their reflections from the dissimilar material boundaries.

Figs. 4.20 through 4.31 are normal stress (σ_{22}) waveforms in direction 2 and

their STFTs at Locations 13 to 24. The maximum value of normal stress is approximately 15 Pa at Location 13. Through these figures, it is evident that the normal stress waves attenuate rapidly as the traveling distance increases. Since it is hit by the thermal shock wave directly, the magnitude of the stress registered at Location 13 is much larger than all other locations. The maximum peak frequency shown in the figures is approximately 2 GHz appearing in 3 ns at location 13. The peak frequency at other acquisition locations falls in the range between approximately 400-600 MHz.

The results indicate that the thermally induced stresses in the TSV flip-chip package are of low magnitude, but broad band, with extremely high frequency. When the microprocessor operates at the clock speed of 2.5 GHz, its closest TSV will undergo an impact from the approximate 2 GHz normal stress which might be fatal to the TSV structure. The power density wave analysis and accumulated damage evaluation will be conducted in the following section to make a thorough study on how these low amplitude but high frequency waves affect the reliability of the package.

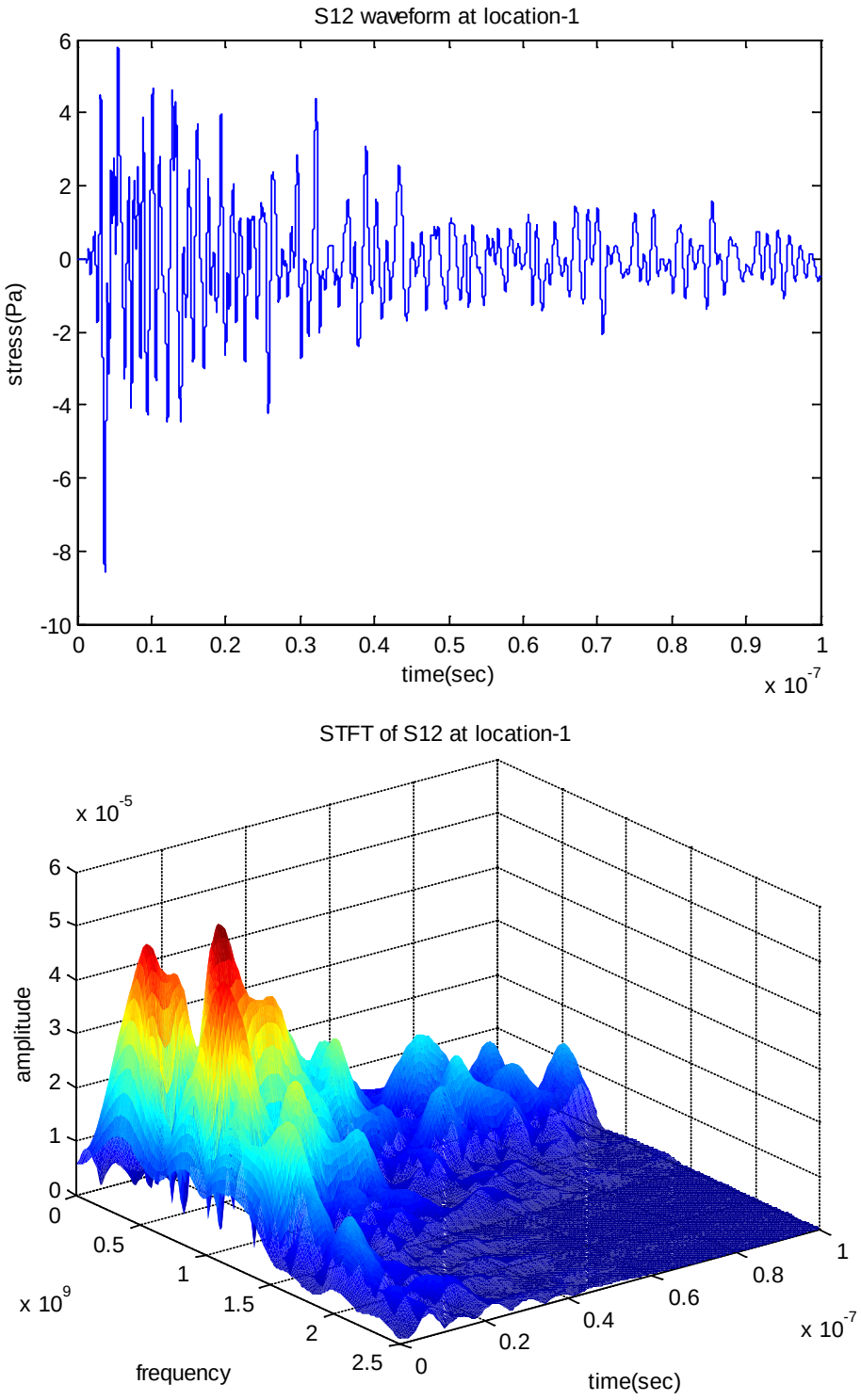

Fig. 4.8 Waveform and associated STFT of σ_{12} at Location 1

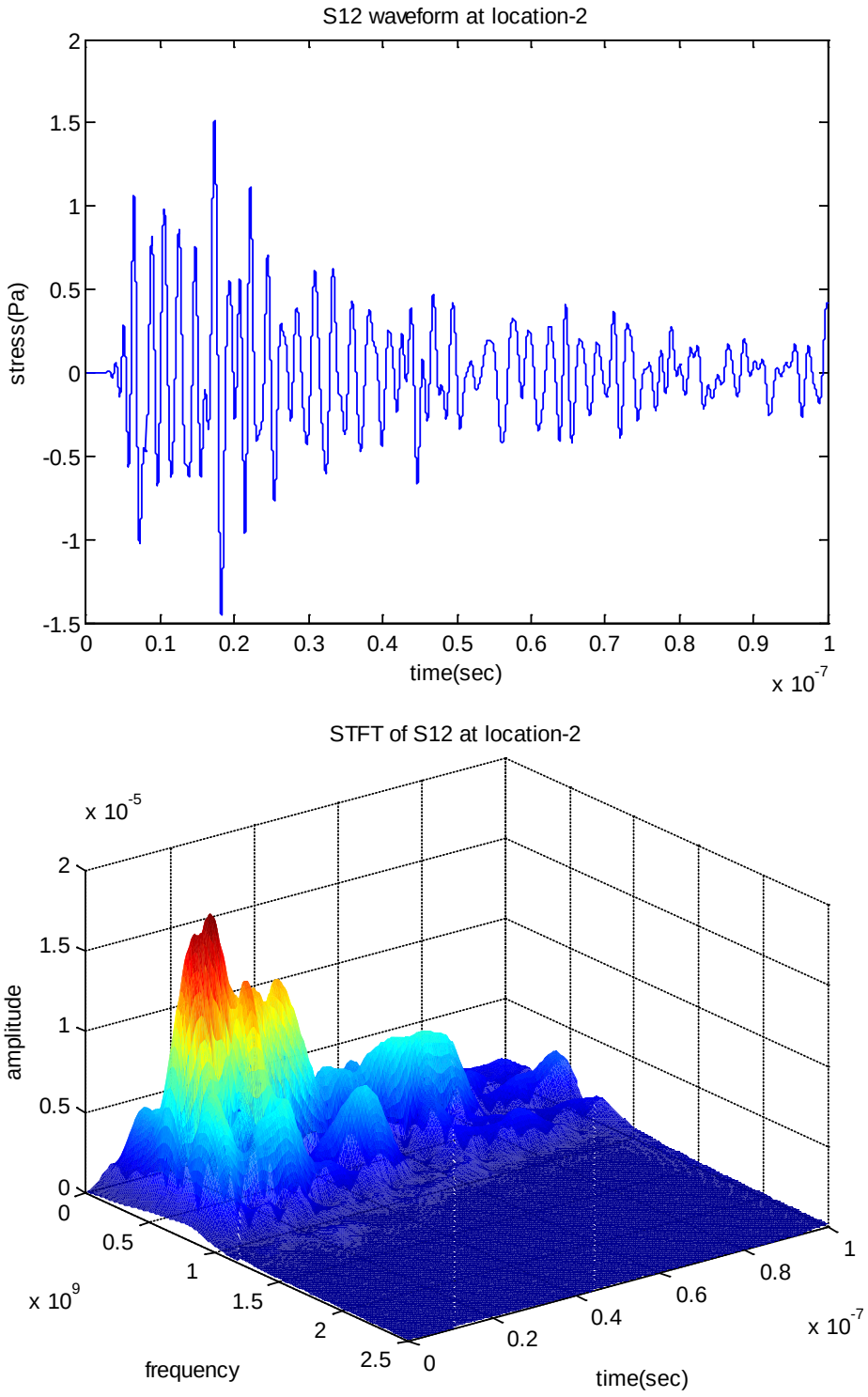

Fig. 4.9 Waveform and associated STFT of σ_{12} at Location 2

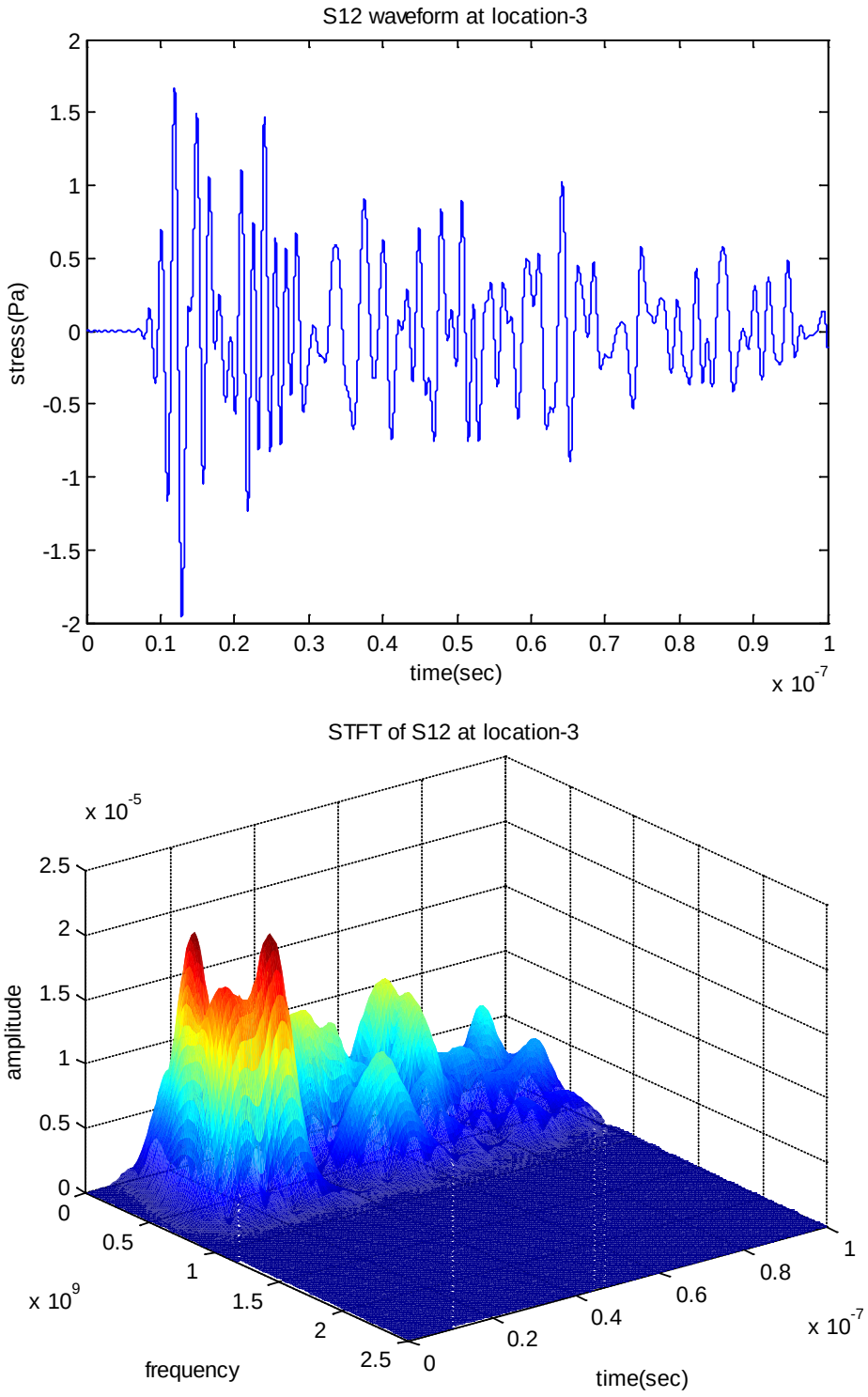

Fig. 4.10 Waveform and associated STFT of σ_{12} at Location 3

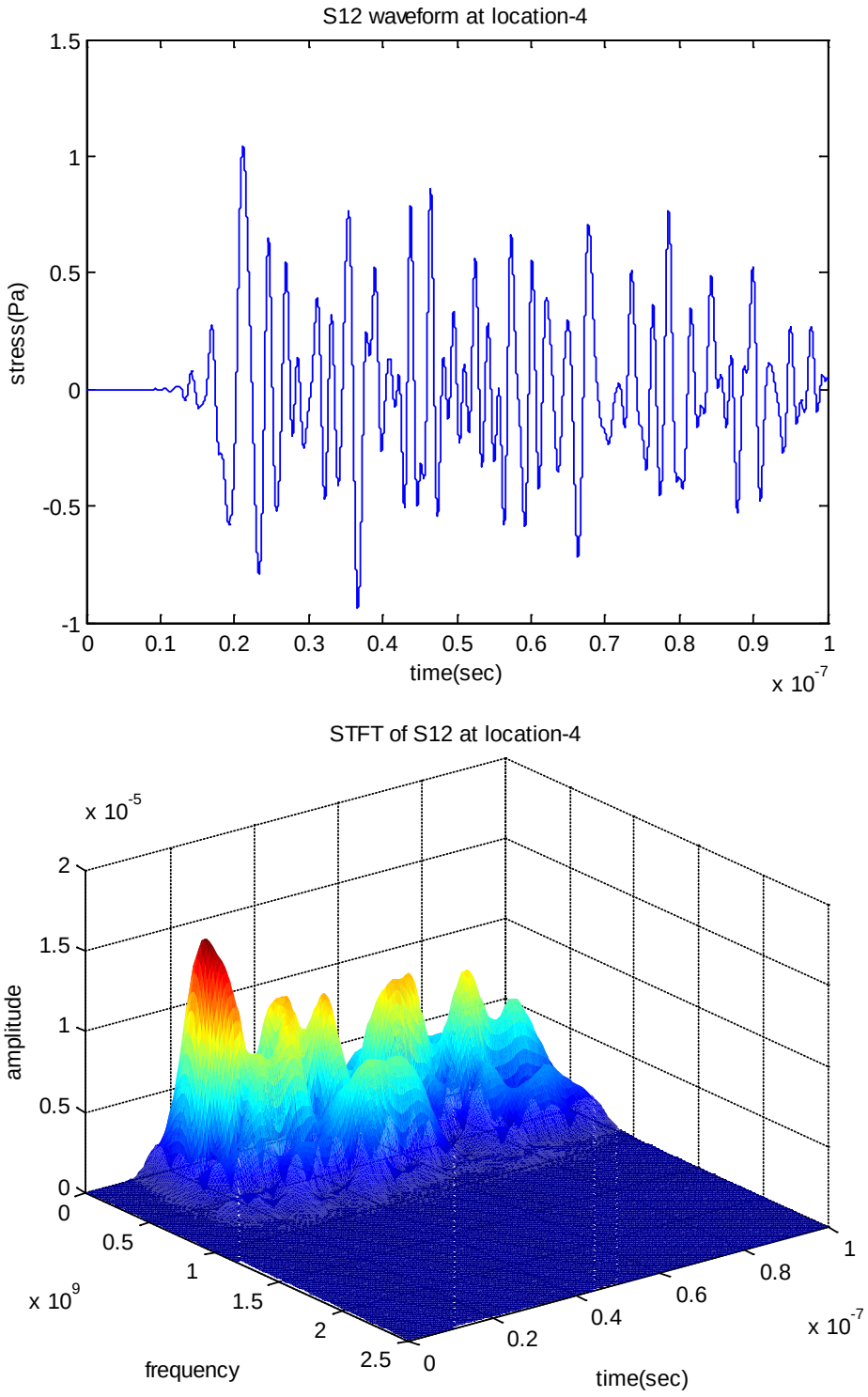

Fig. 4.11 Waveform and associated STFT of σ_{12} at Location 4

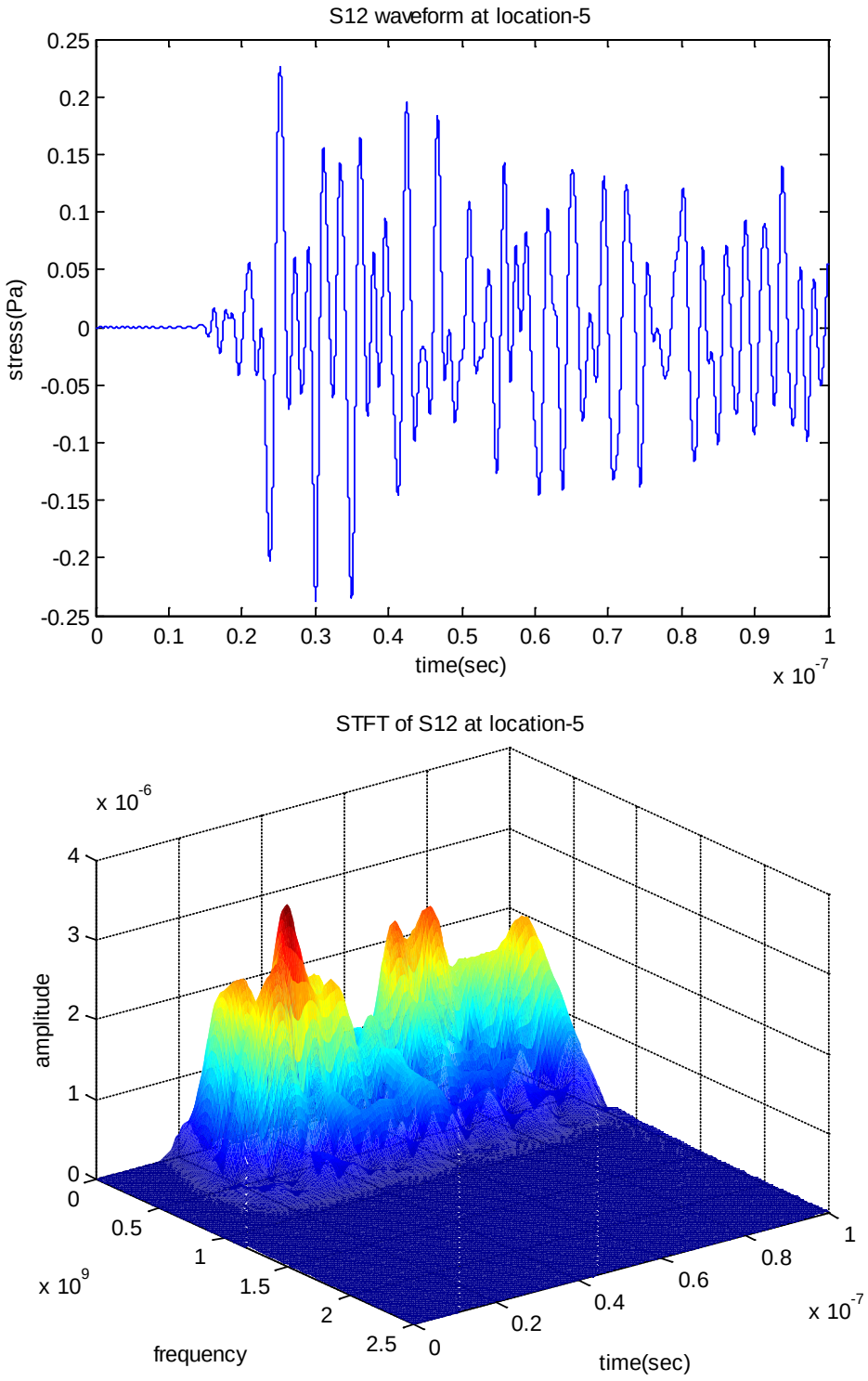

Fig. 4.12 Waveform and associated STFT of σ_{12} at Location 5

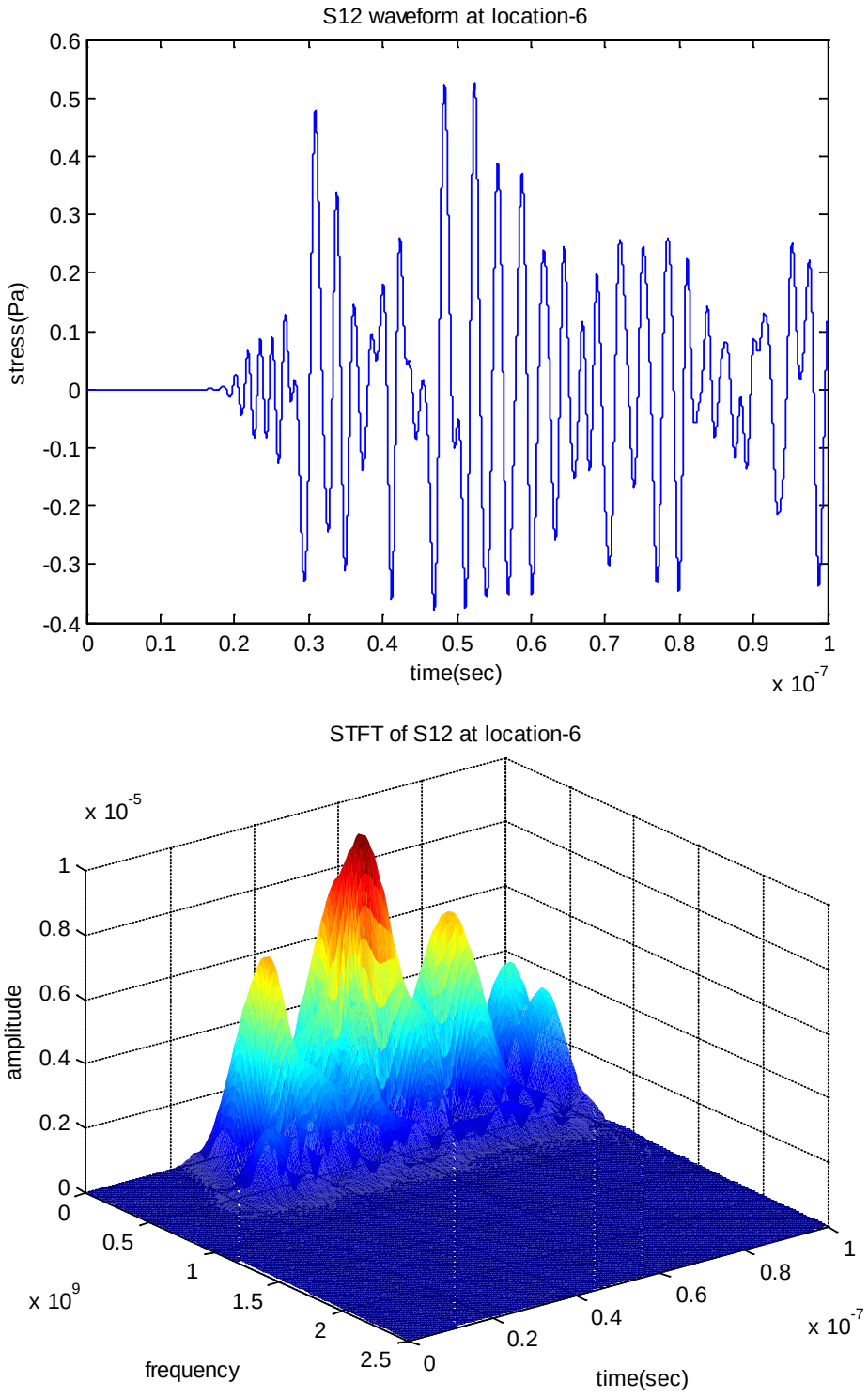

Fig. 4.13 Waveform and associated STFT of σ_{12} at Location 6

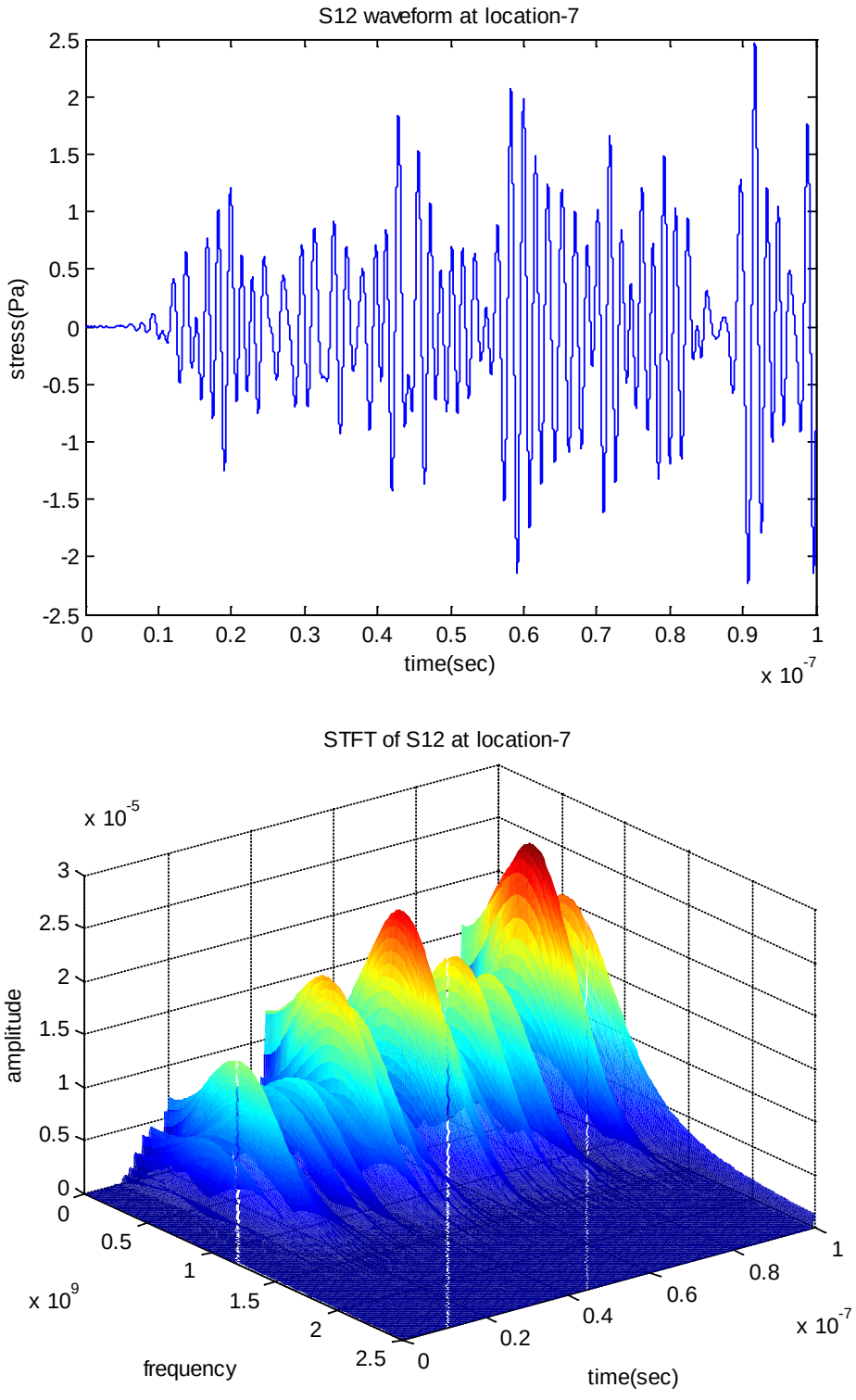

Fig. 4.14 Waveform and associated STFT of σ_{12} at Location 7

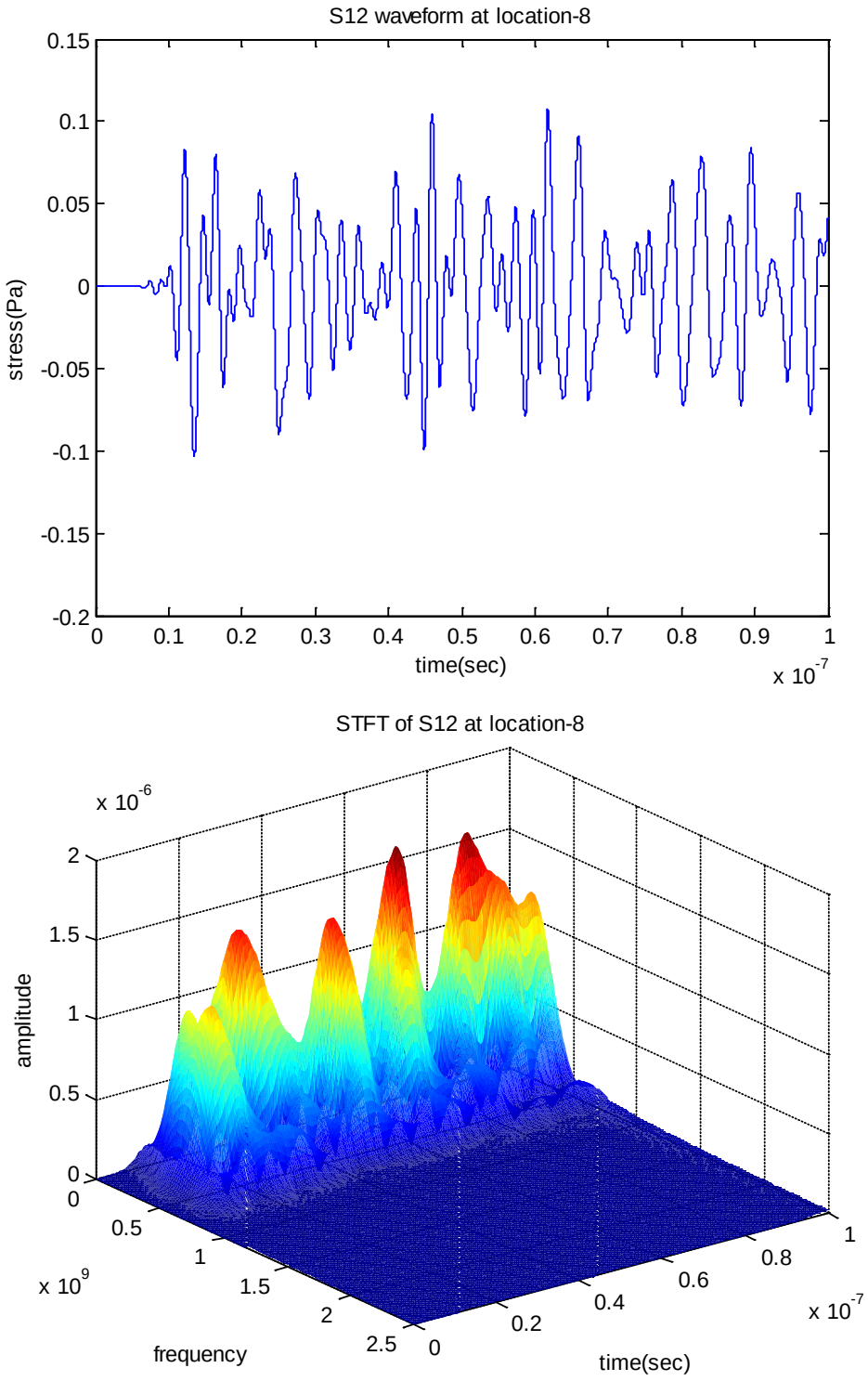

Fig. 4.15 Waveform and associated STFT of σ_{12} at Location 8

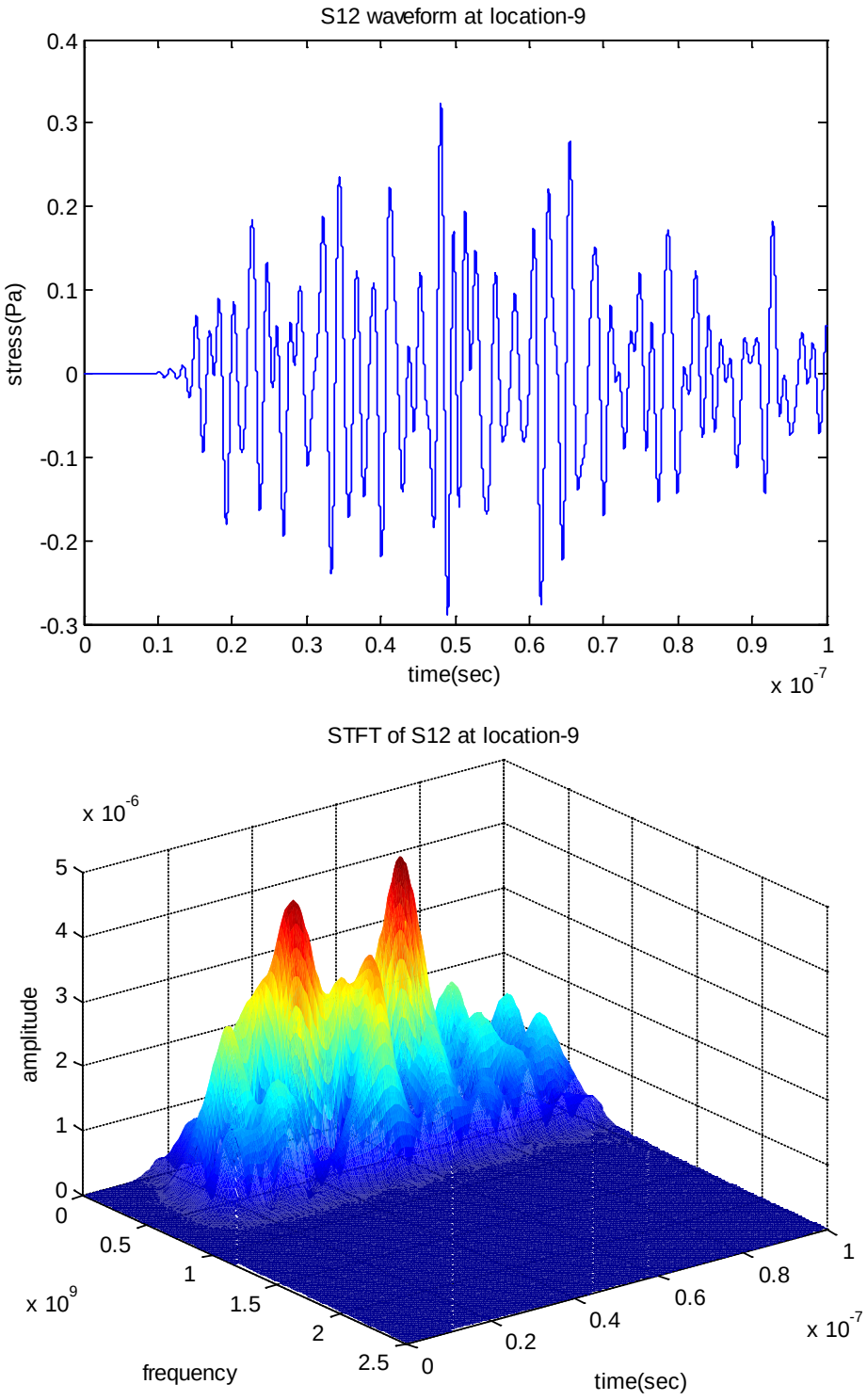

Fig. 4.16 Waveform and associated STFT of σ_{12} at Location 9

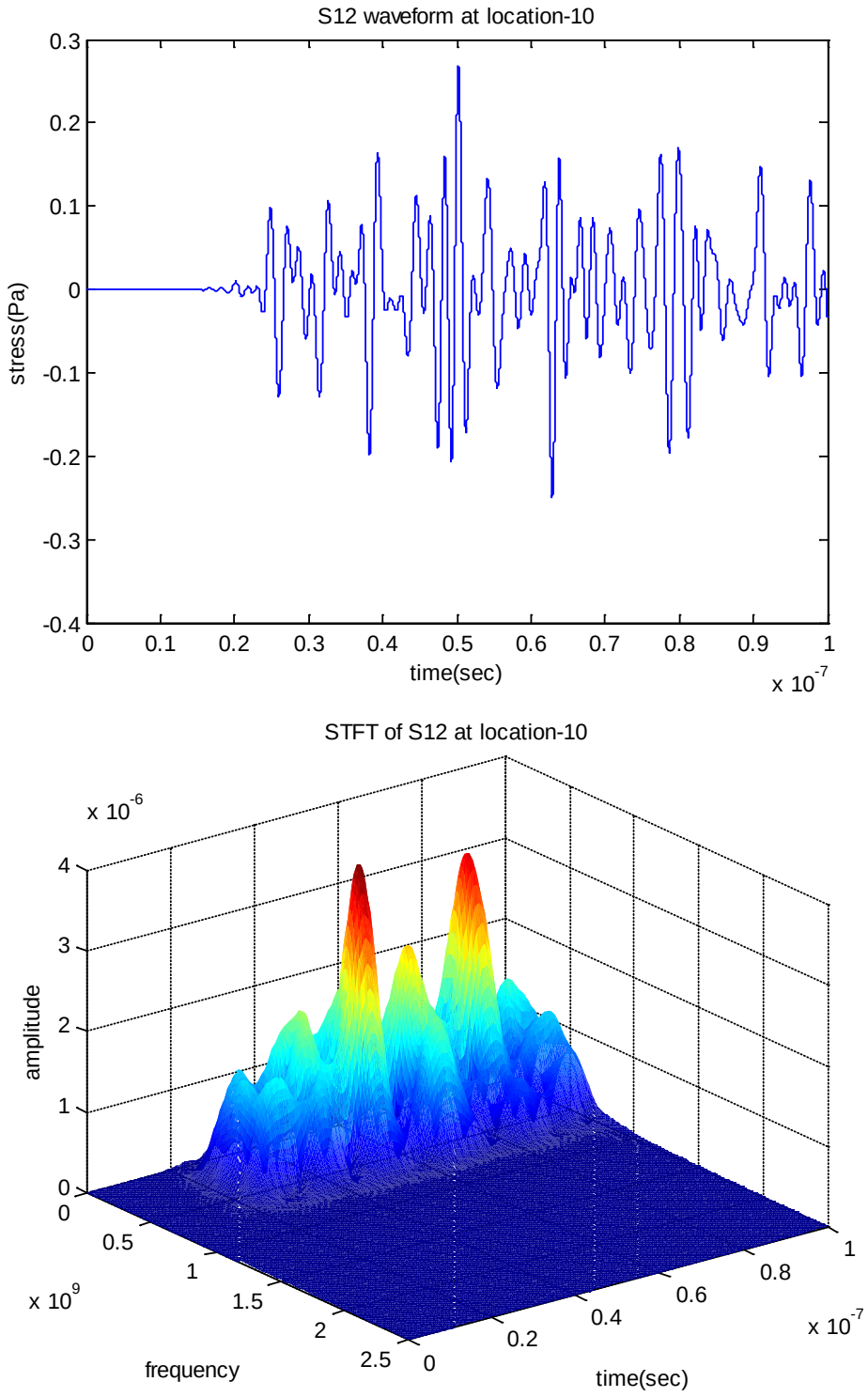

Fig. 4.17 Waveform and associated STFT of σ_{12} at Location 10

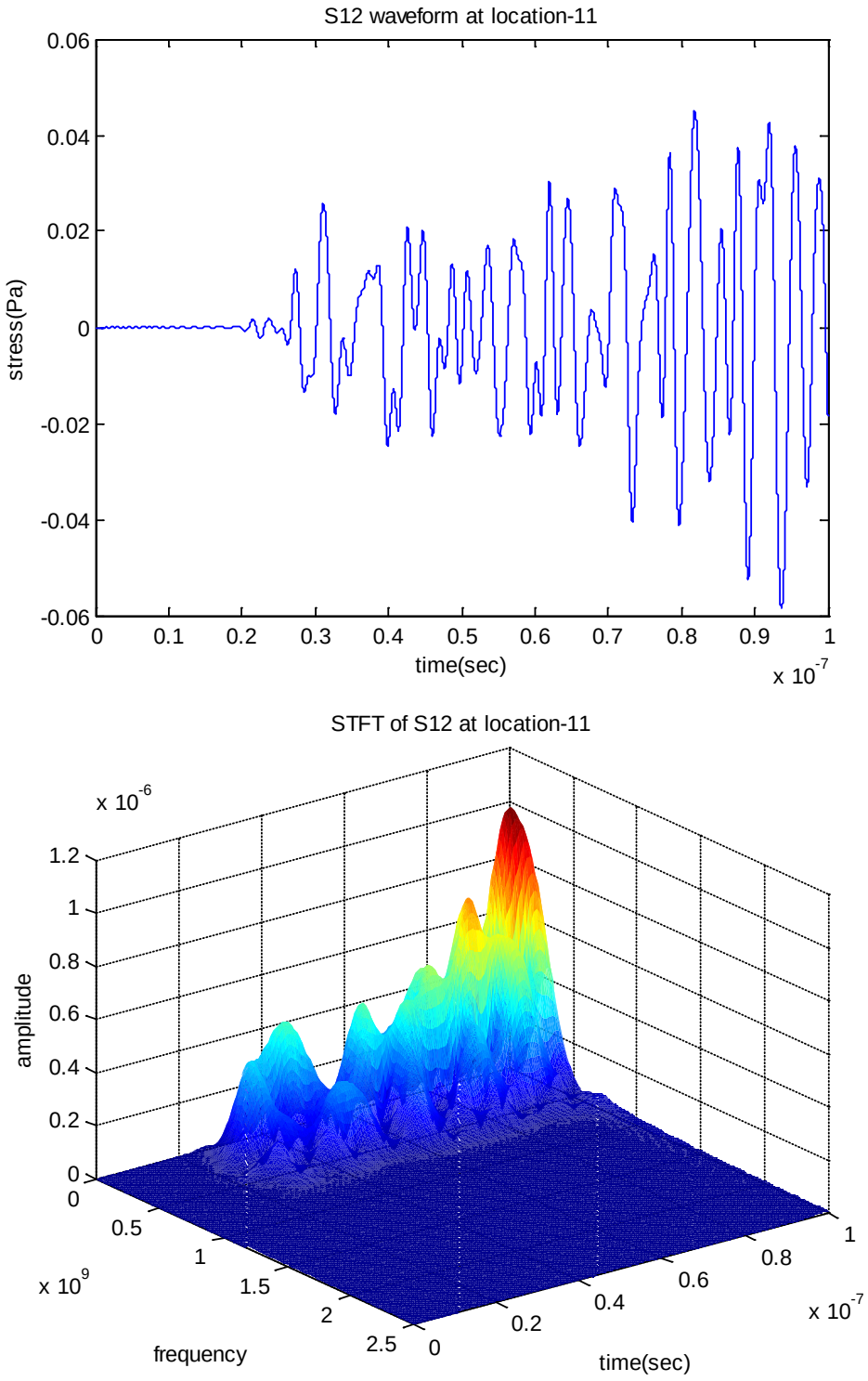

Fig. 4.18 Waveform and associated STFT of σ_{12} at Location 11

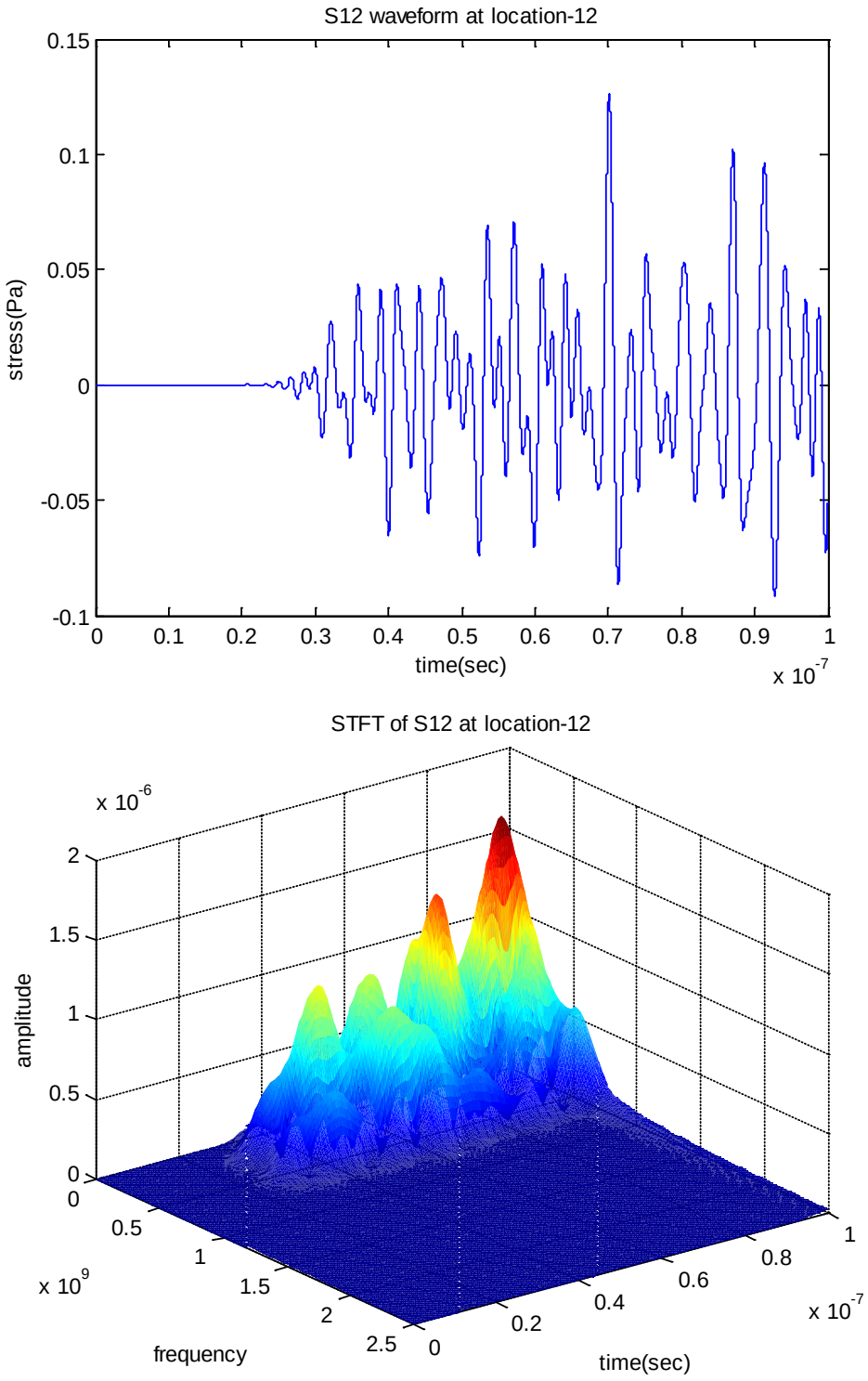

Fig. 4.19 Waveform and associated STFT of σ_{12} at Location 12

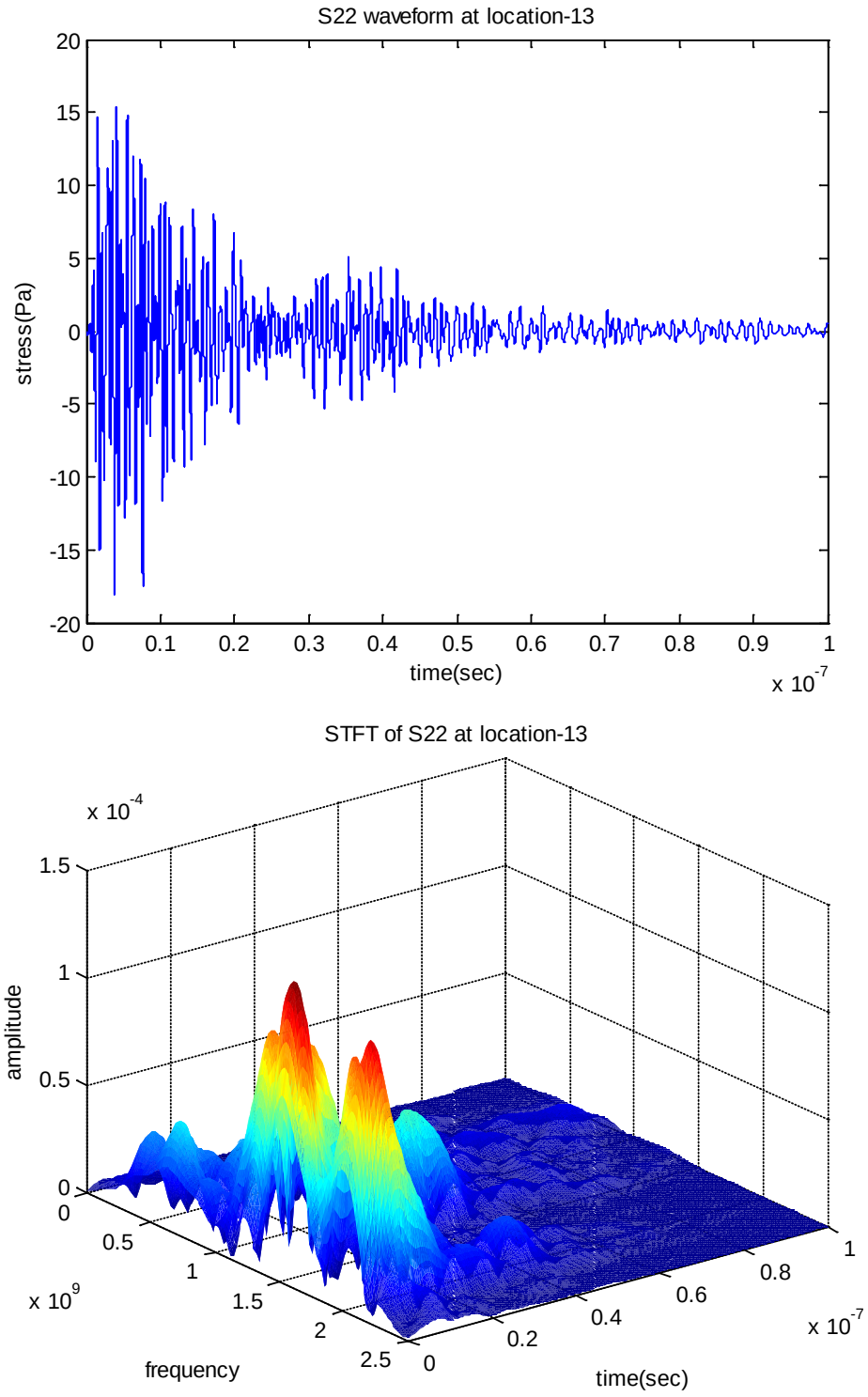

Fig. 4.20 Waveform and associated STFT of σ_{22} at Location 13

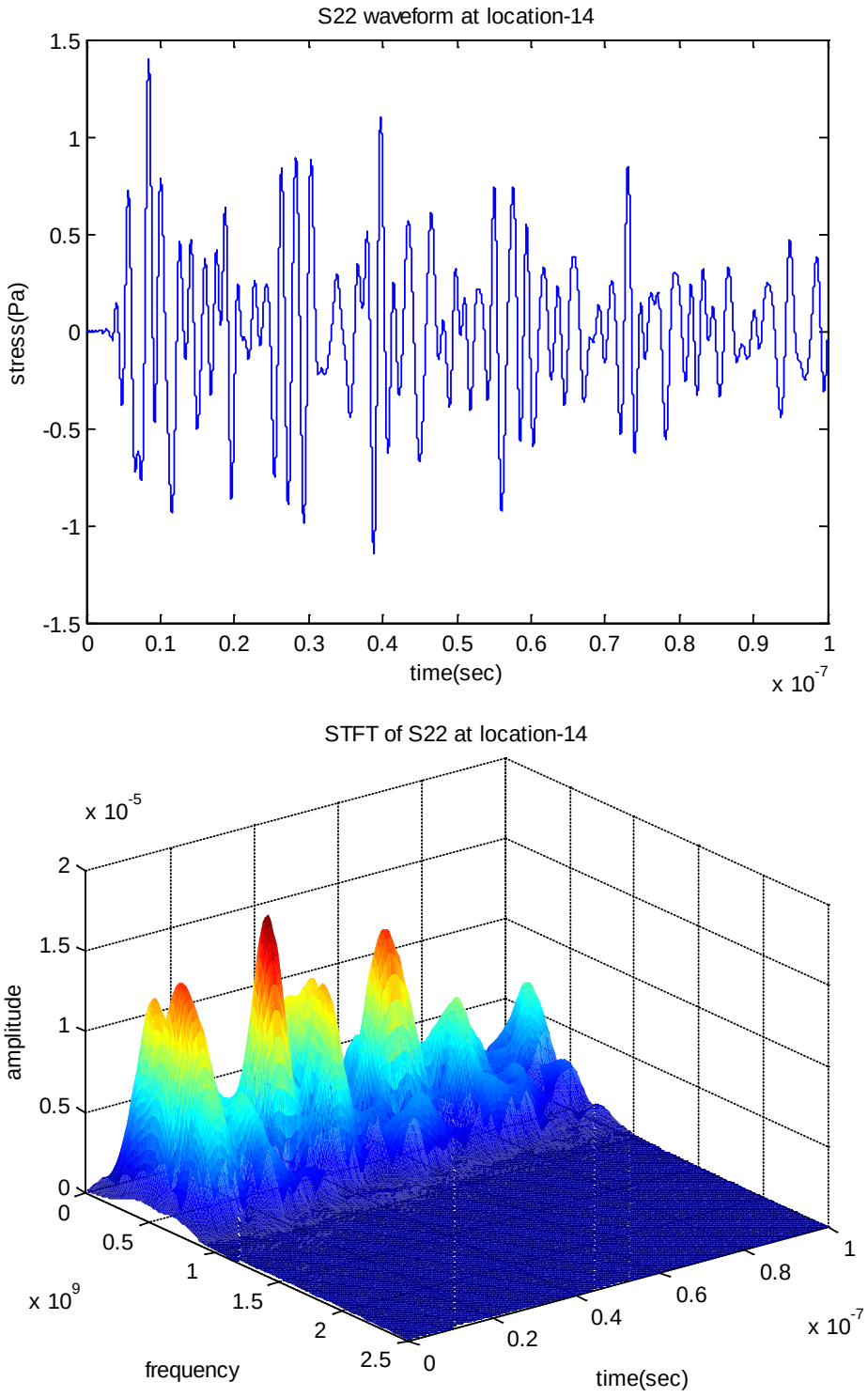

Fig. 4.21 Waveform and associated STFT of σ_{22} at Location 14

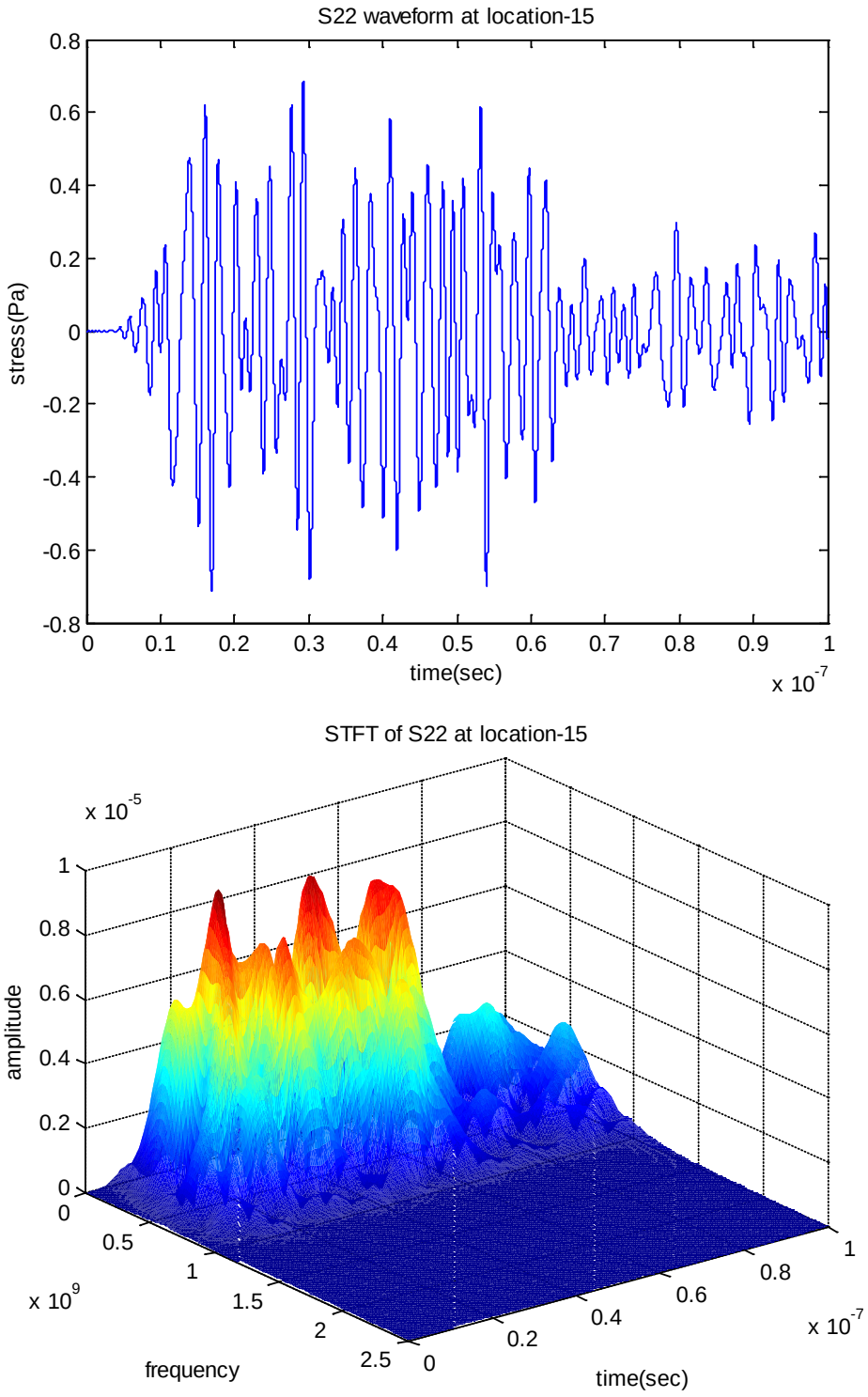

Fig. 4.22 Waveform and associated STFT of σ_{22} at Location 15

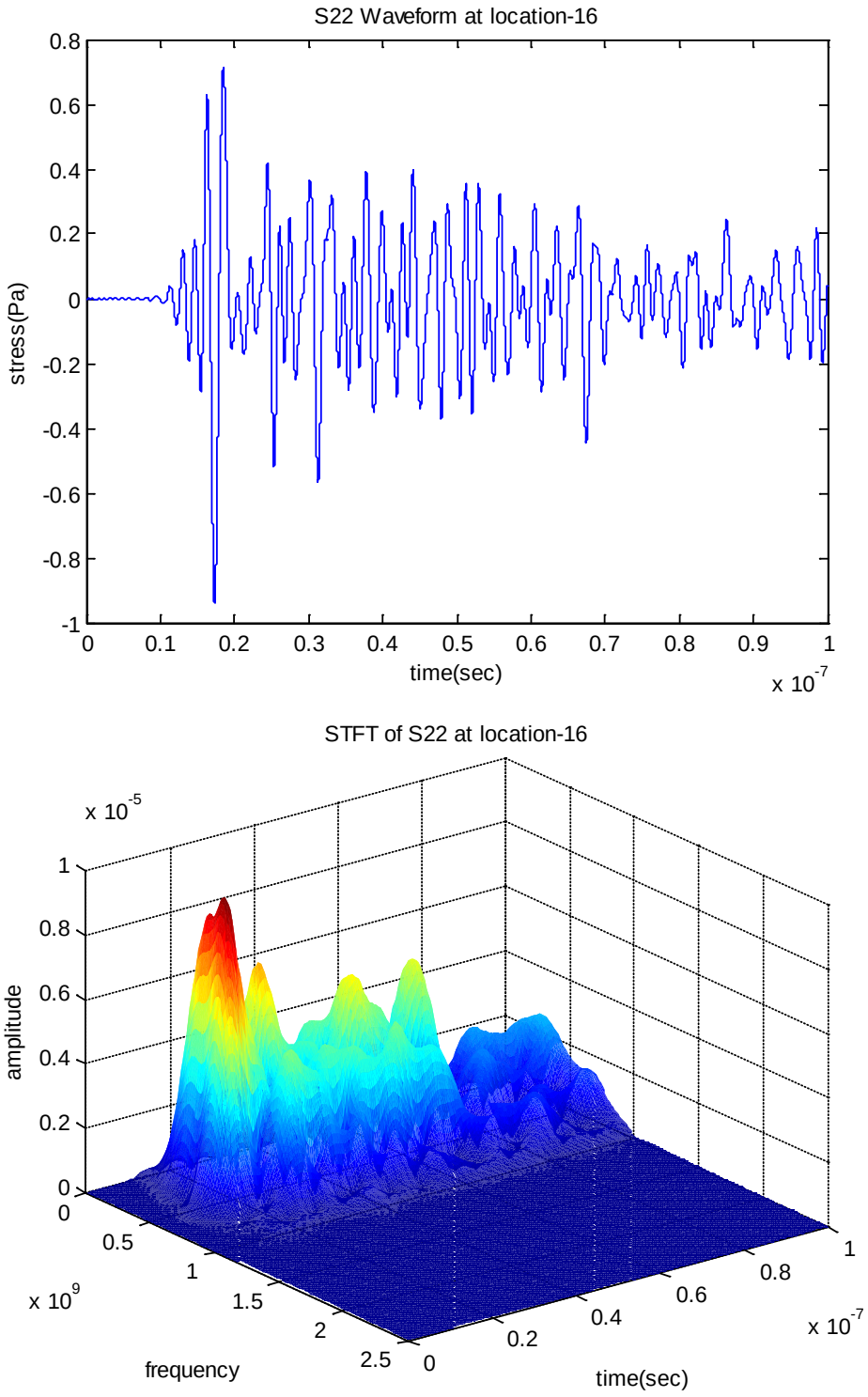

Fig. 4.23 Waveform and associated STFT of σ_{22} at Location 16

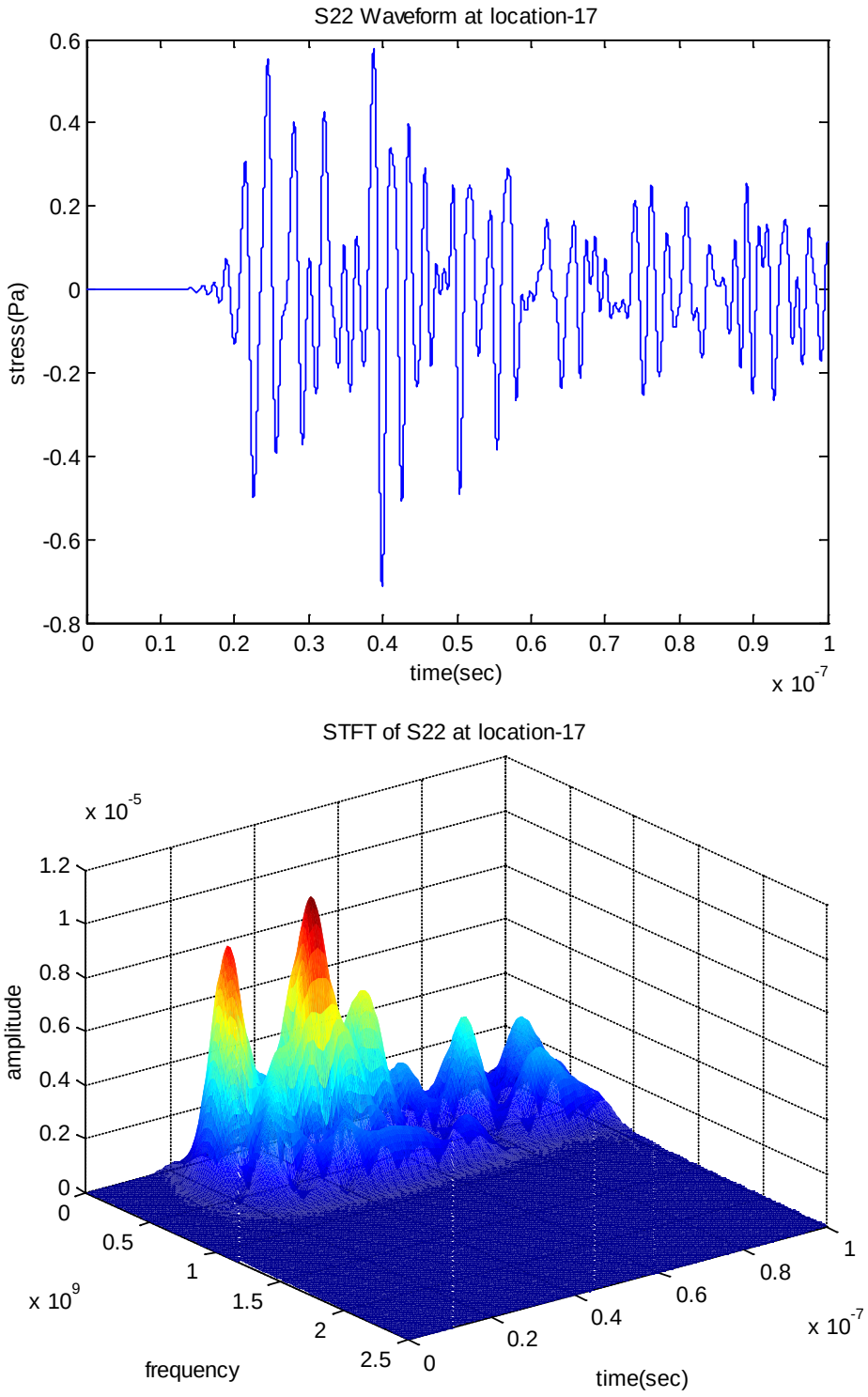

Fig. 4.24 Waveform and associated STFT of σ_{22} at Location 17

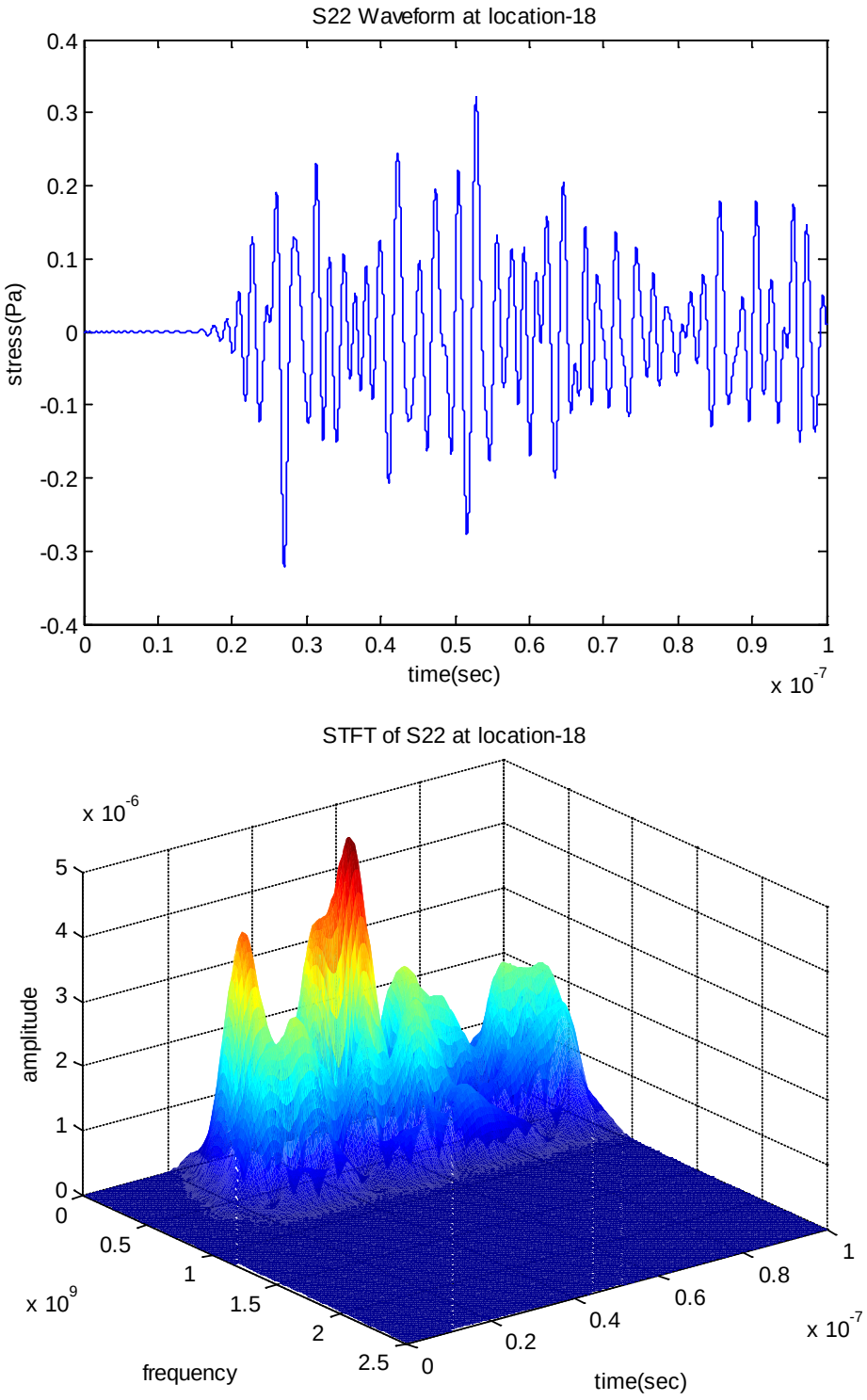

Fig. 4.25 Waveform and associated STFT of σ_{22} at Location 18

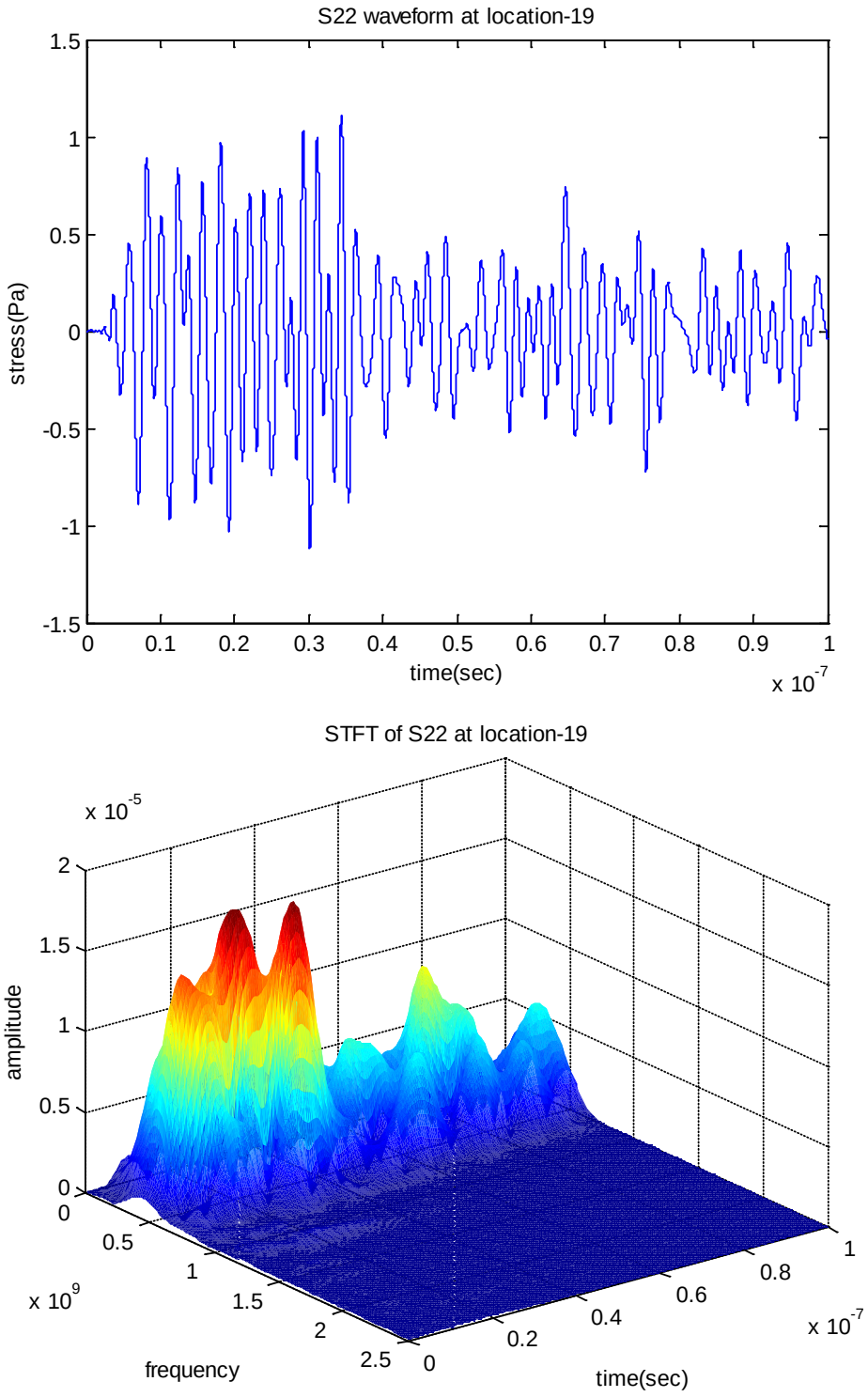

Fig. 4.26 Waveform and associated STFT of σ_{22} at Location 19

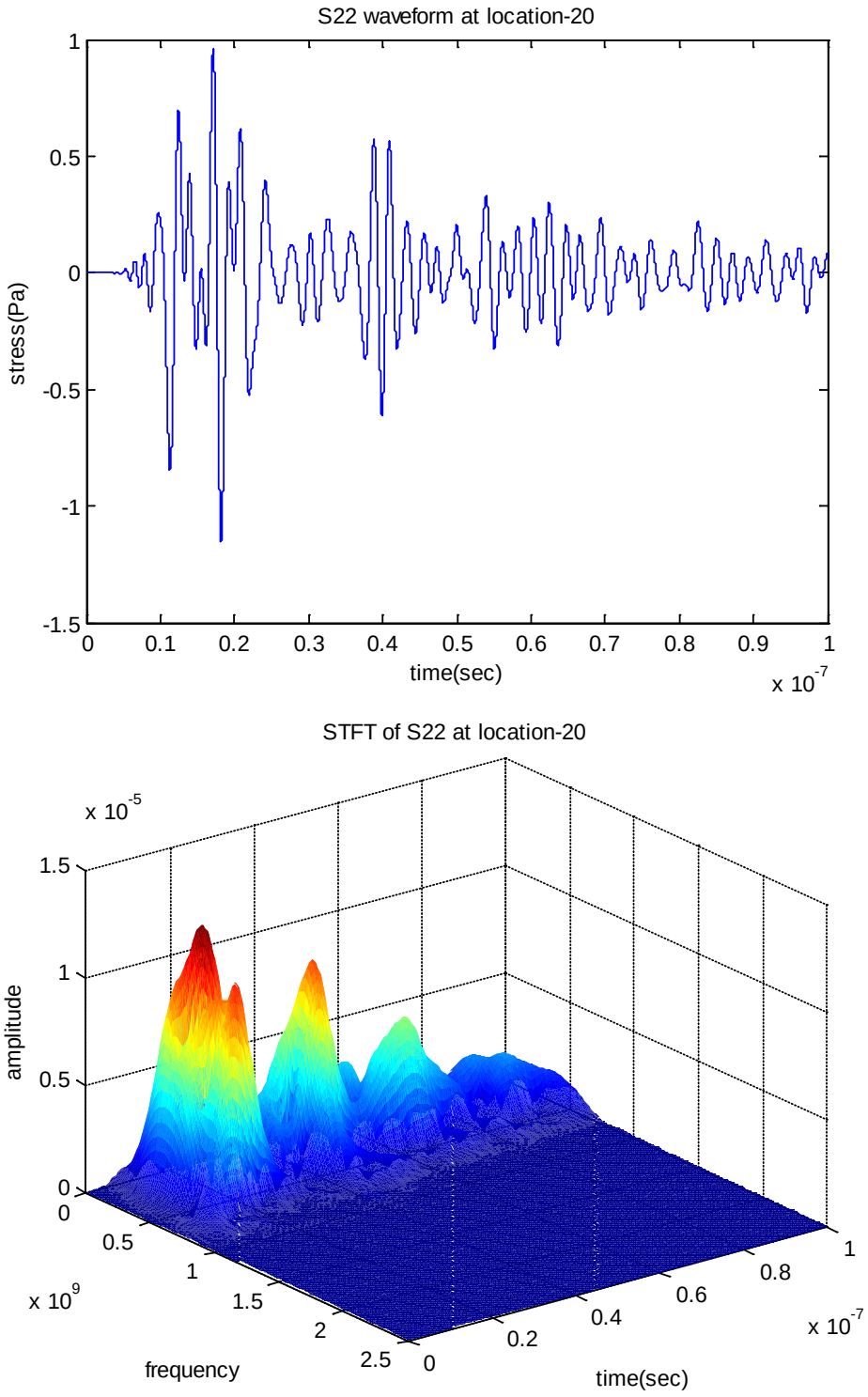

Fig. 4.27 Waveform and associated STFT of σ_{22} at Location 20

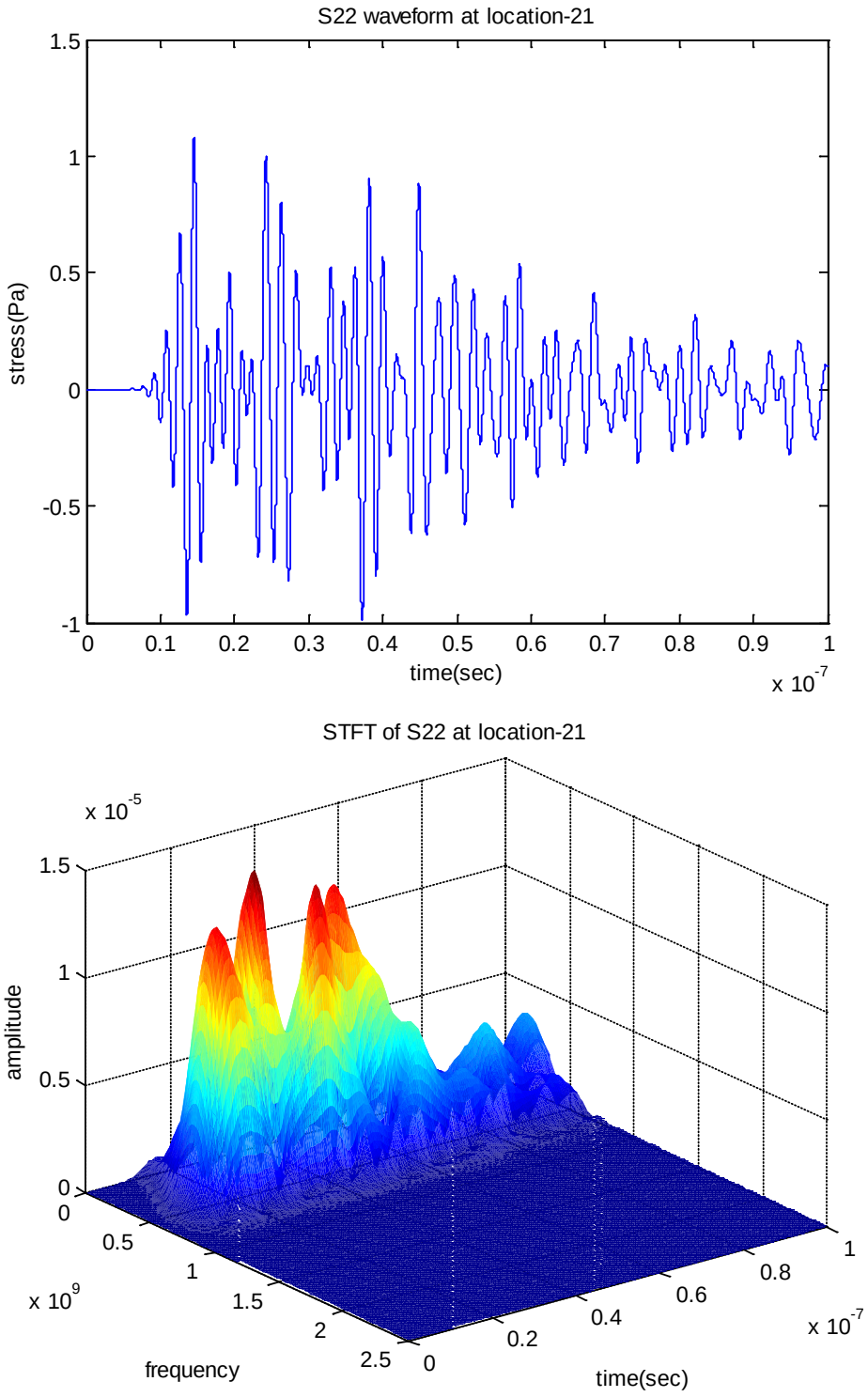

Fig. 4.28 Waveform and associated STFT of σ_{22} at Location 21

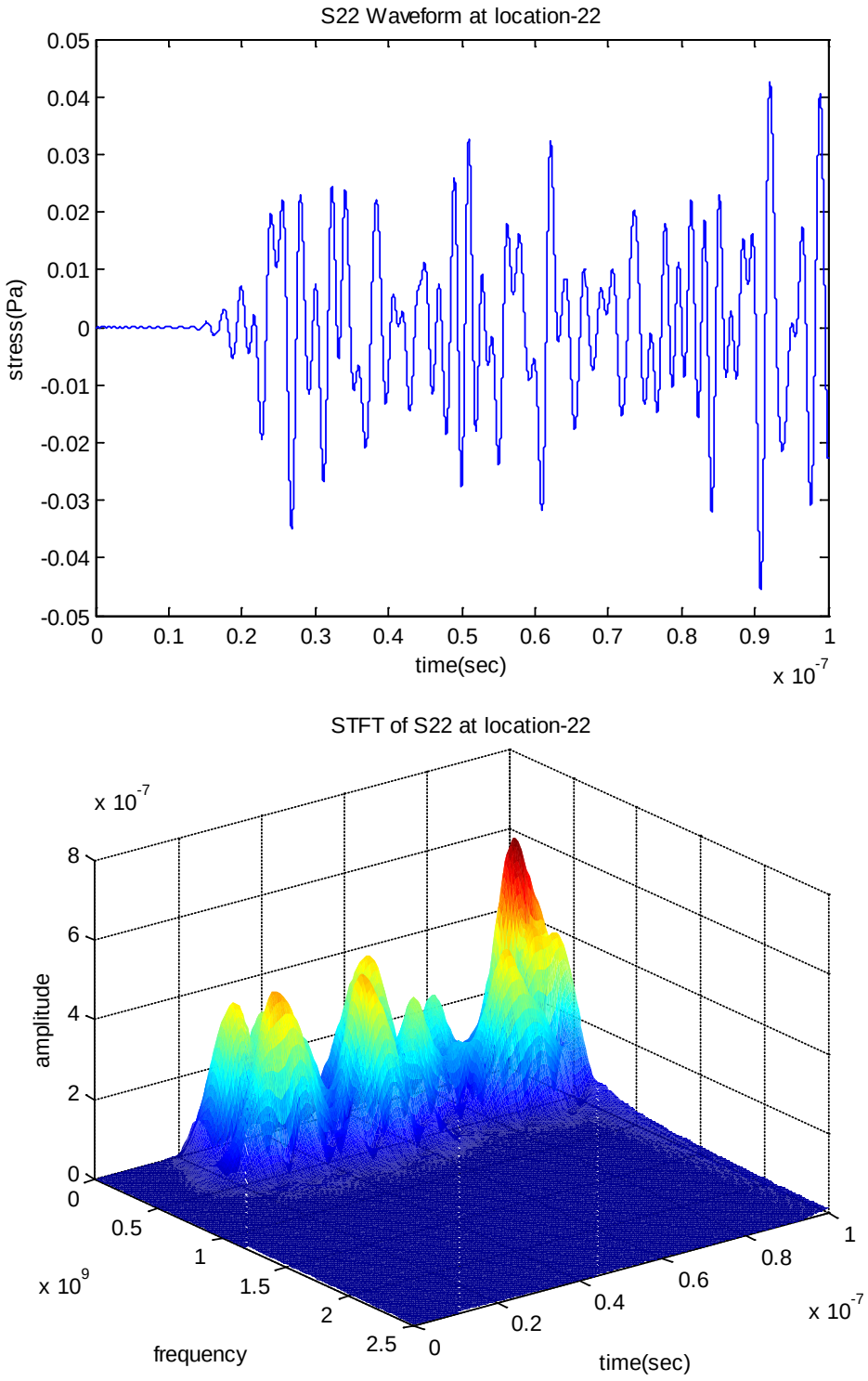

Fig. 4.29 Waveform and associated STFT of σ_{22} at Location 22

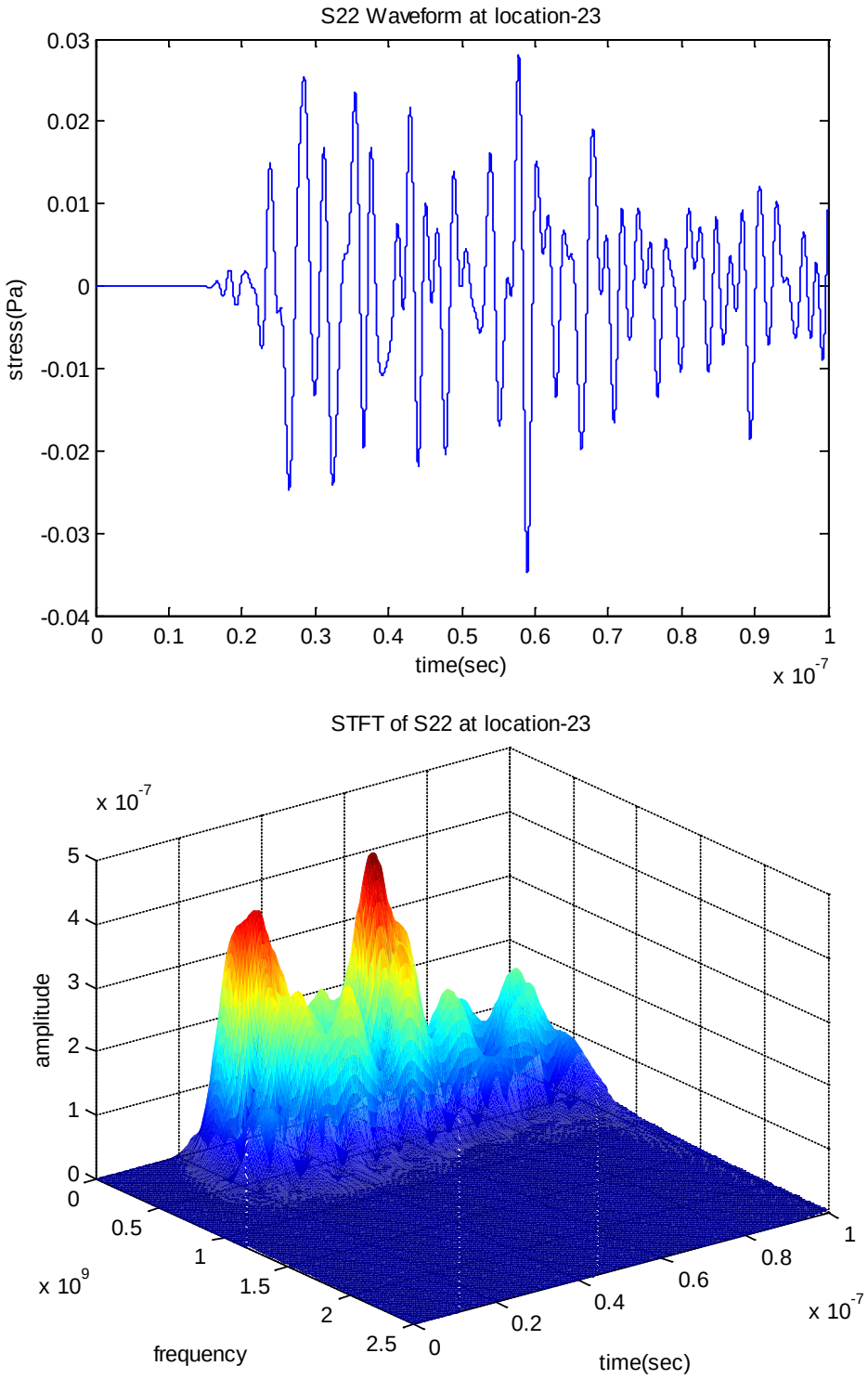

Fig. 4.30 Waveform and associated STFT of σ_{22} at Location 23

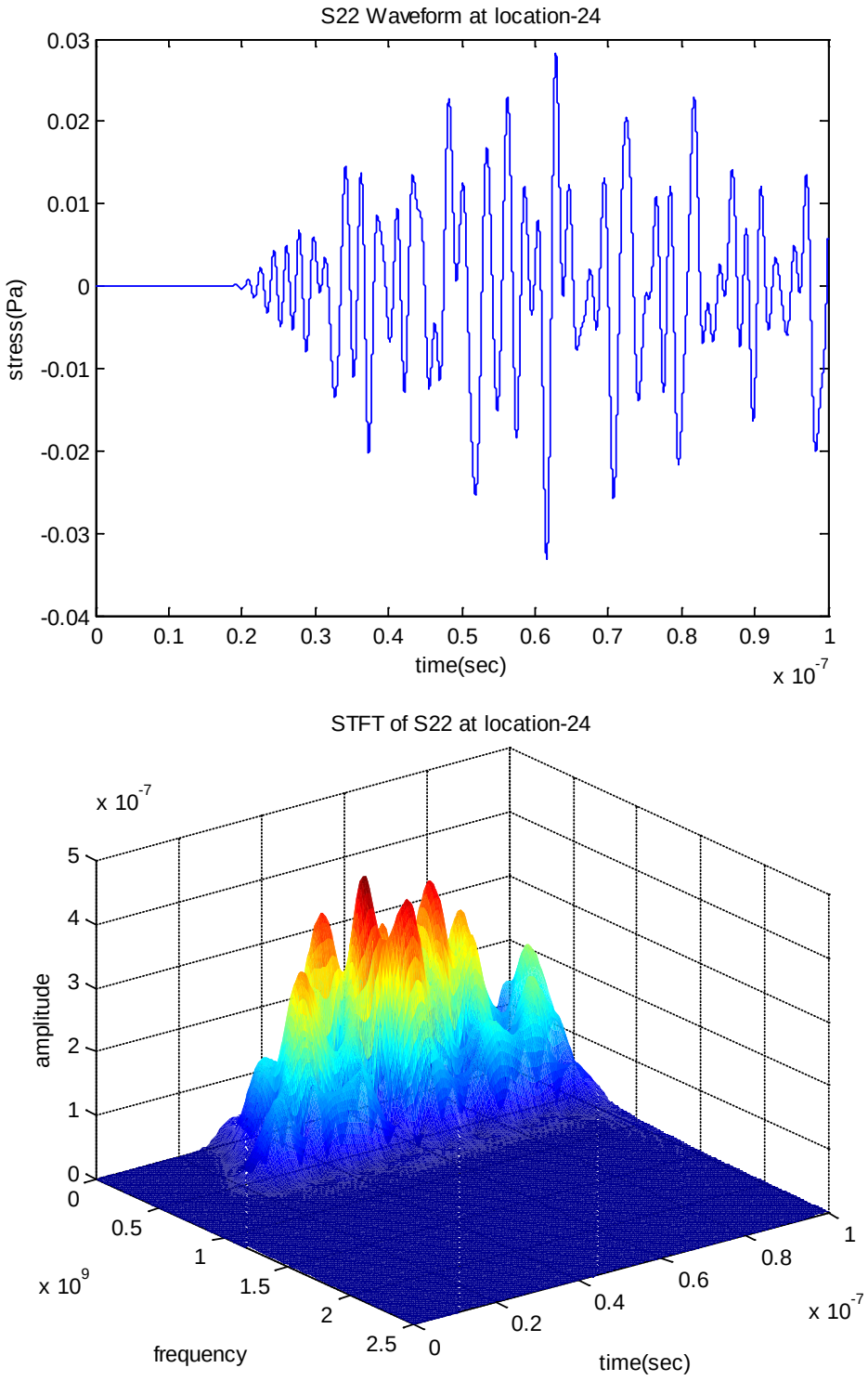

Fig. 4.31 Waveform and associated STFT of σ_{22} at Location 24

4.3.3 Power Density Waves

Since the magnitudes of the stress waves are too small to be directly related to packaging failure, the feature of mega-hertz frequency carried by these stress waves should be taken seriously when dealing with the reliability of IC packages. In order to demonstrate how these high frequency stresses impact the TSV flip-chip package, the term "power density (W / m^3)" is introduced. The idea of power density comes from material fatigue test, where a specimen is cycled by two predefined stress values at a constant loading frequency. Mechanical fatigue occurs when a certain number of cycles are completed. The number of cycles until fatigue depends nonlinearly on the amplitude of the predefined testing stresses. Usually the higher stress applied in the test will result in fewer number of cycles until failure. The SI units conversion of a time-varying stress can be shown to be equivalent to power per unit volume as

$$\left[\frac{\partial \sigma}{\partial t}\right] \equiv \left[\frac{N}{m^2 s}\right] \equiv \left[\frac{N \cdot m}{m^3 s}\right] \equiv \left[\frac{J}{m^3 s}\right] \equiv \left[\frac{W}{m^3}\right]$$

During power-on, components in the TSV flip-chip package can be treated as

undergoing non-periodic loading as shown in Figs. 4.10 through 4.33. The power density discussed here is defined as the temporal gradient of stresses, which can be referred to as a parameter quantifying the power per unit volume resulting from the oscillating loading.

Figs. 4.32 through 4.43 are shear stress power density waves, $\frac{\partial \sigma_{12}}{\partial t}$ (P12), and their STFTs at Locations 1 to 12. Figs. 4.44 through 4.55 are normal stress power density waves, $\frac{\partial \sigma_{22}}{\partial t}$ (P22), and their STFTs at Locations 13 to 24. The hundred-giga Watts magnitude of power density at Location 13 is considerably high. From the STFT analyses, the power density waves disperse rapidly within the time window. The dominant frequency of the power density waves starts with approximately 2 GHz at Location 13 and then reduces to 500 MHz in other locations with its bandwidth reduced down to 500 MHz.

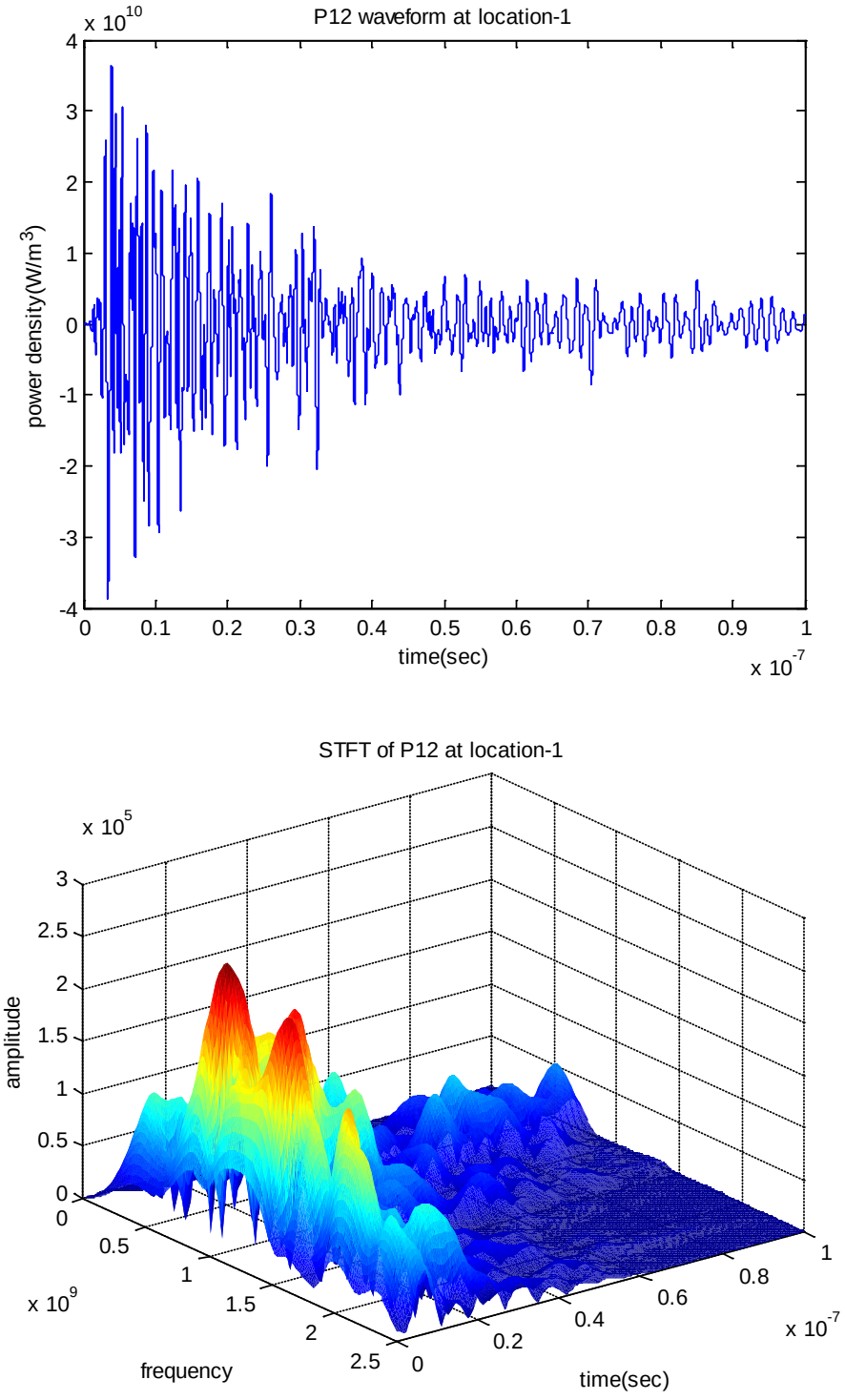

Fig. 4.32 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 1

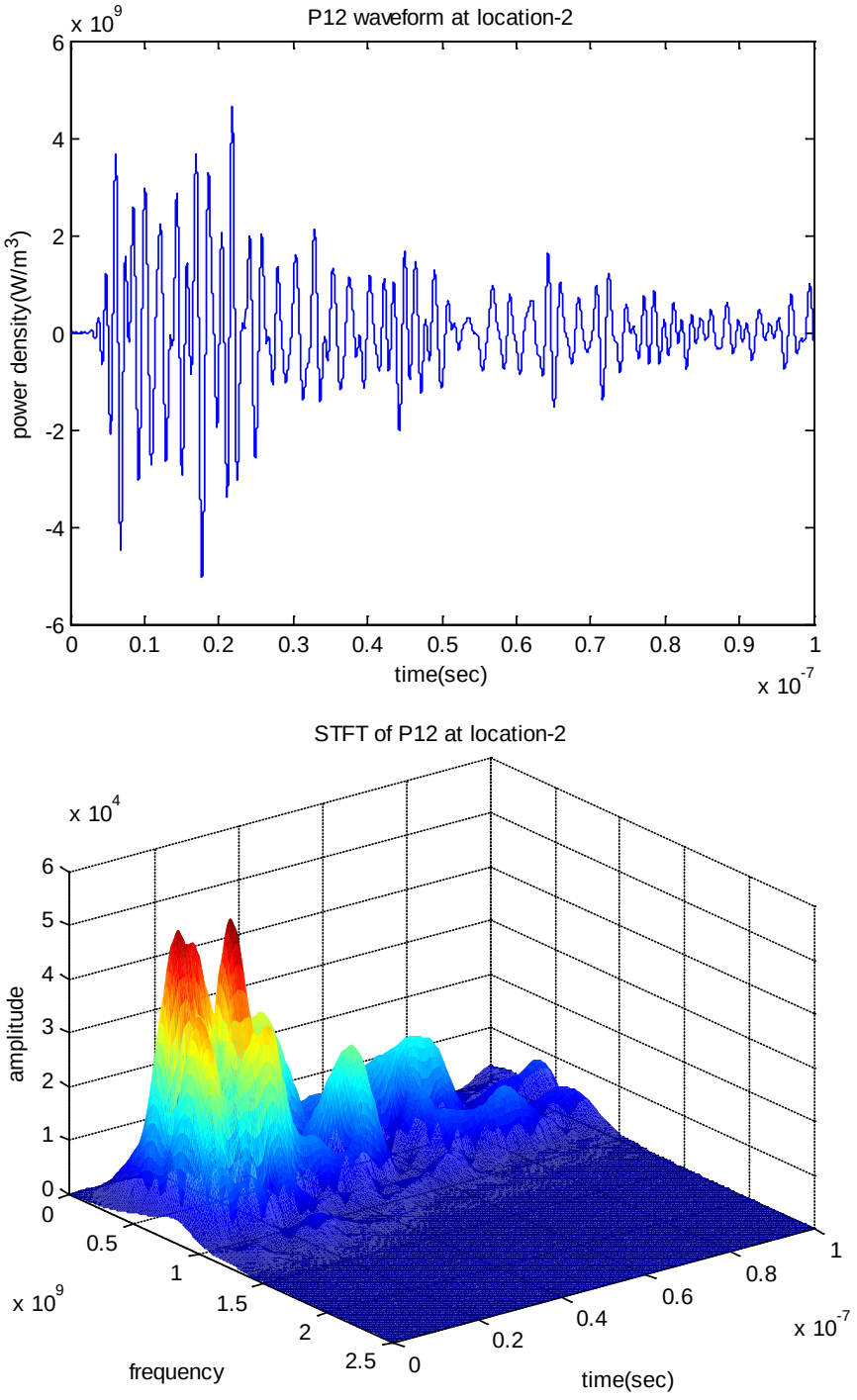

Fig. 4.33 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 2

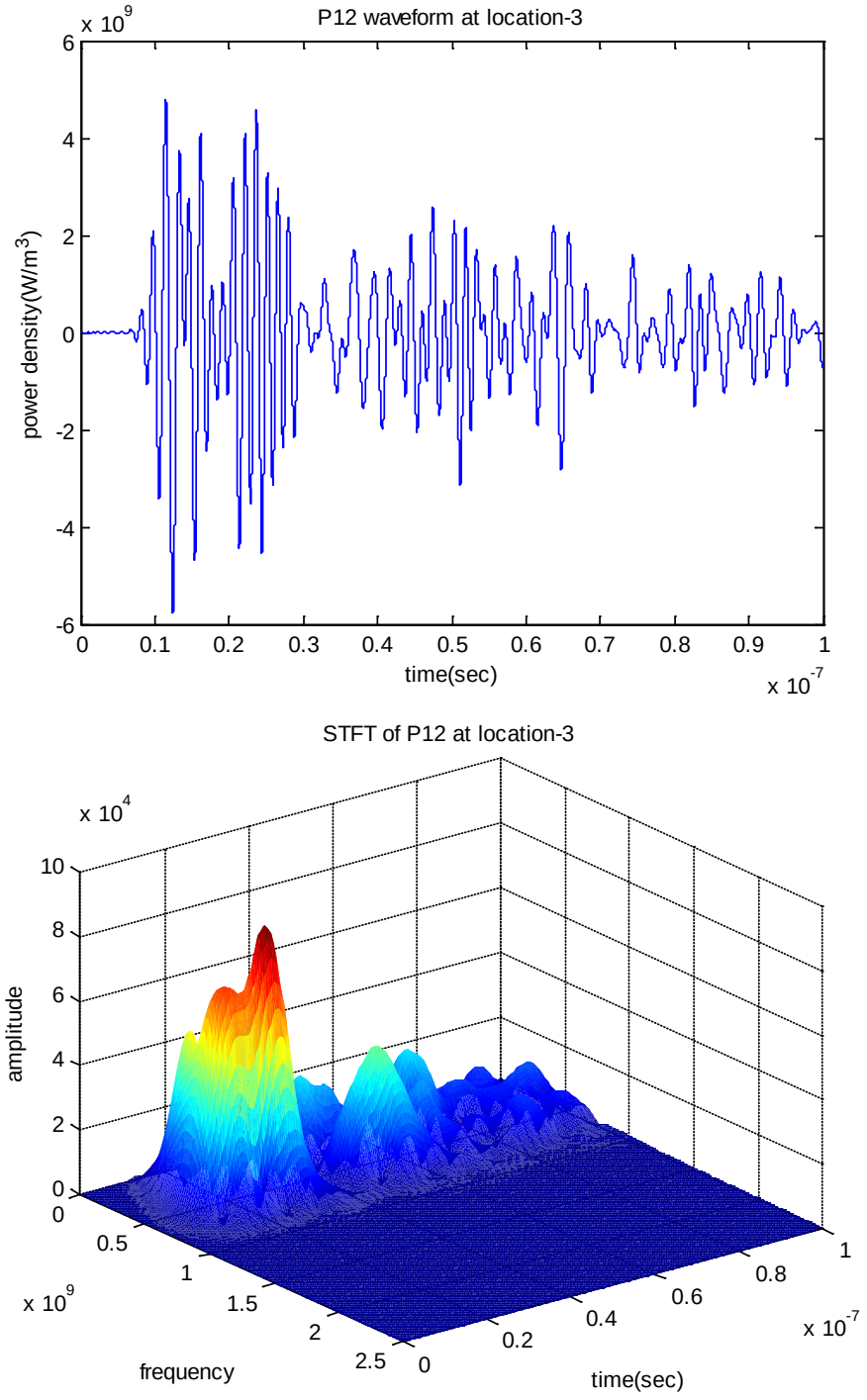

Fig. 4.34 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 3

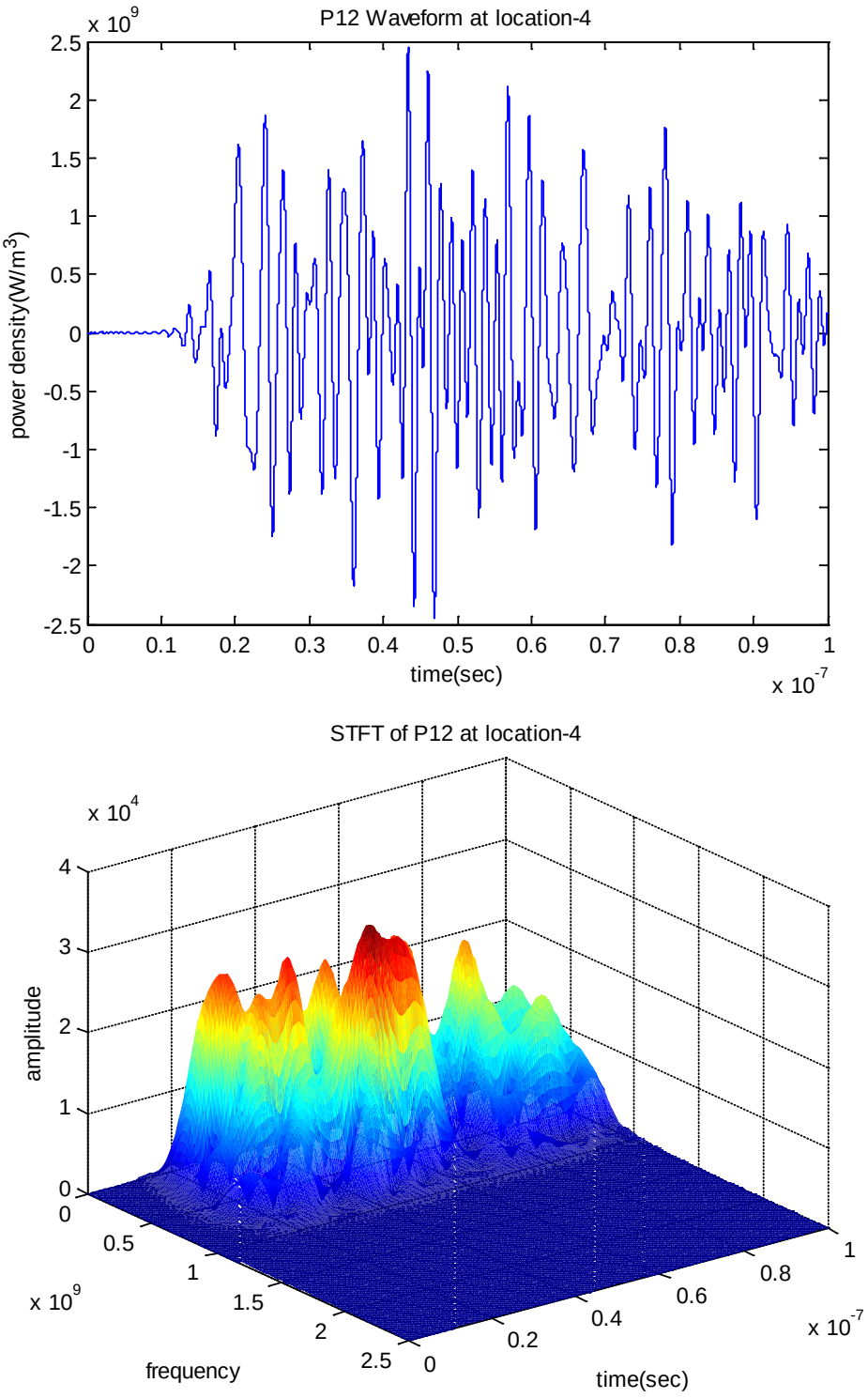

Fig. 4.35 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 4

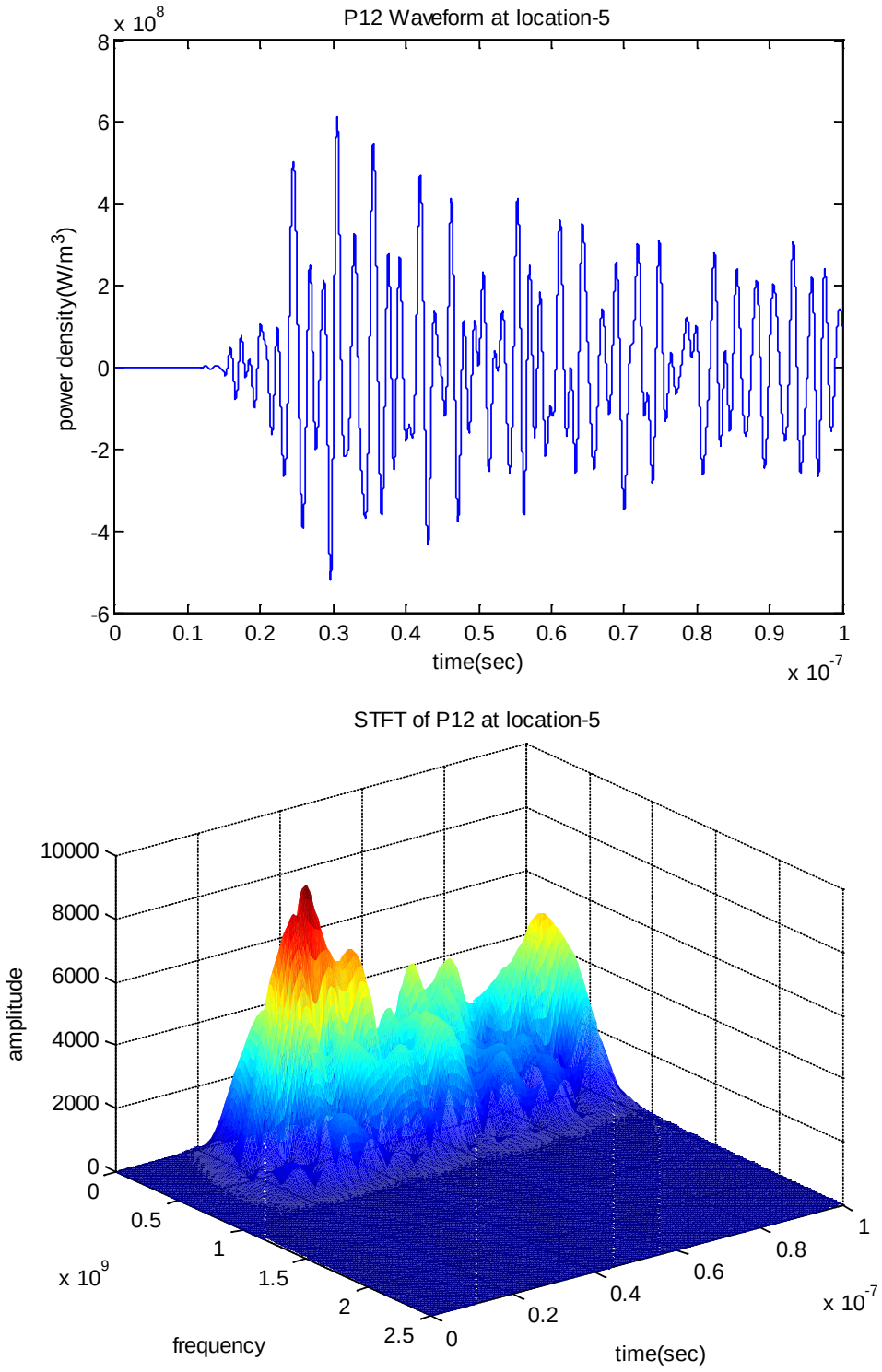

Fig. 4.36 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 5

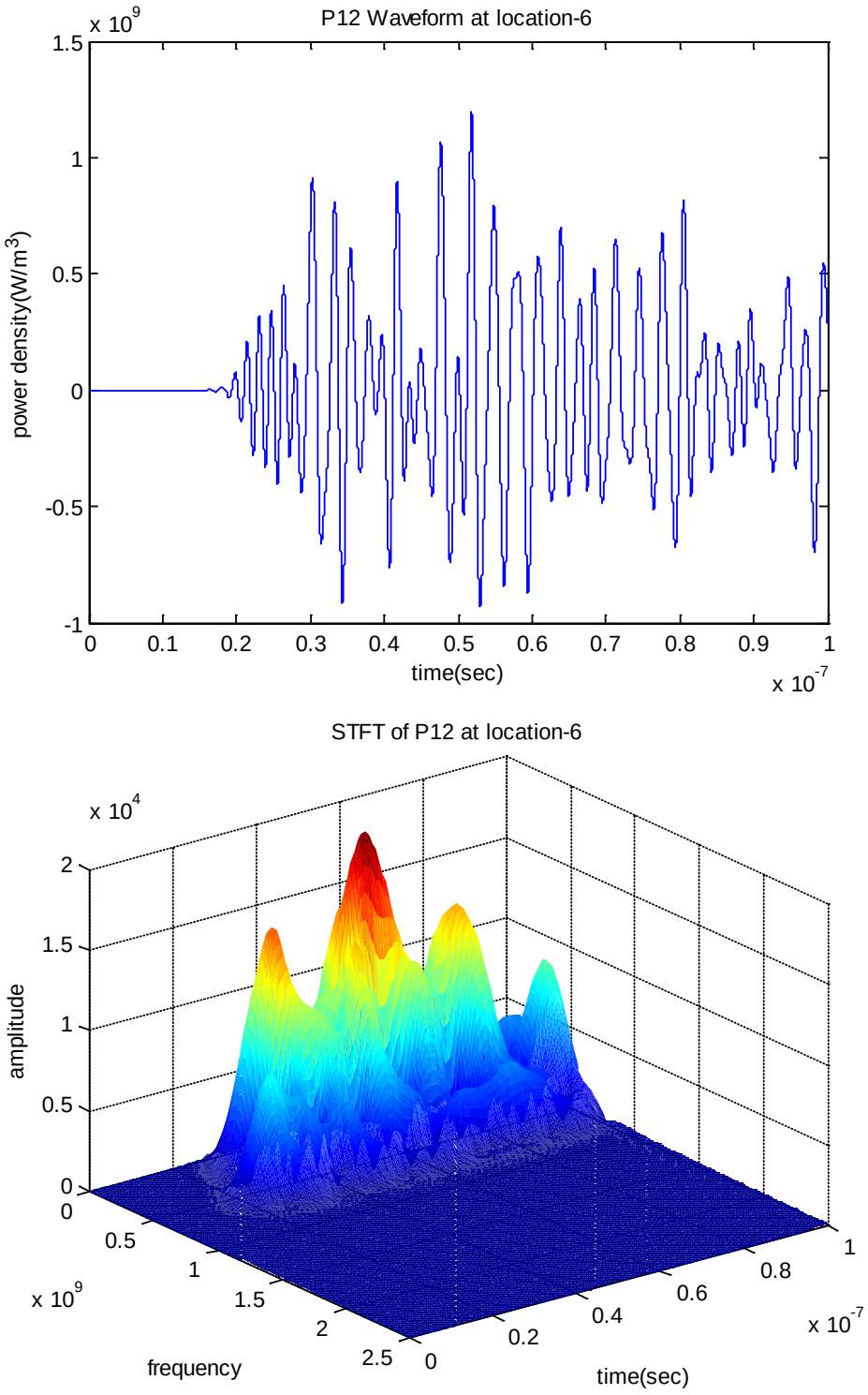

Fig. 4.37 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 6

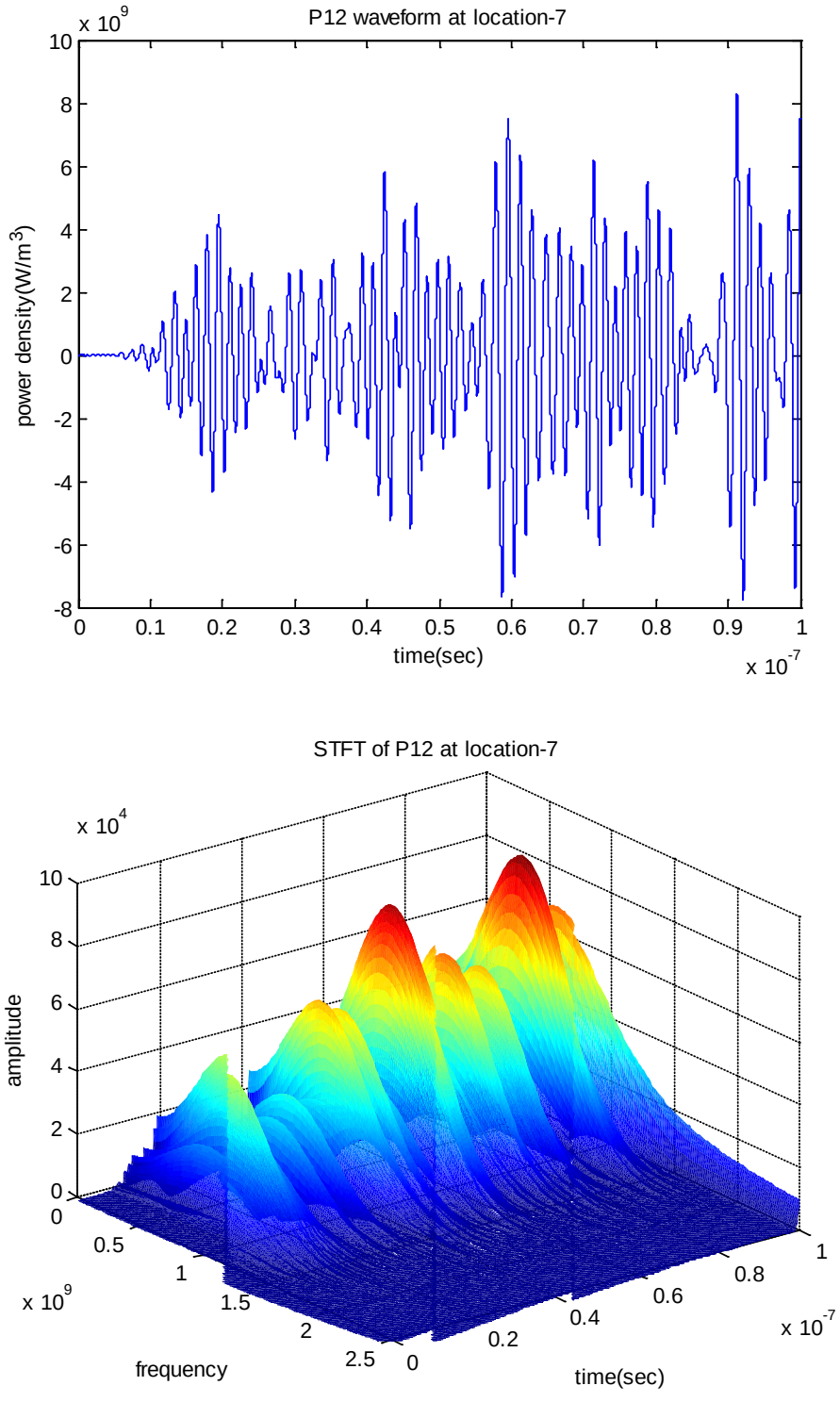

Fig. 4.38 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 7

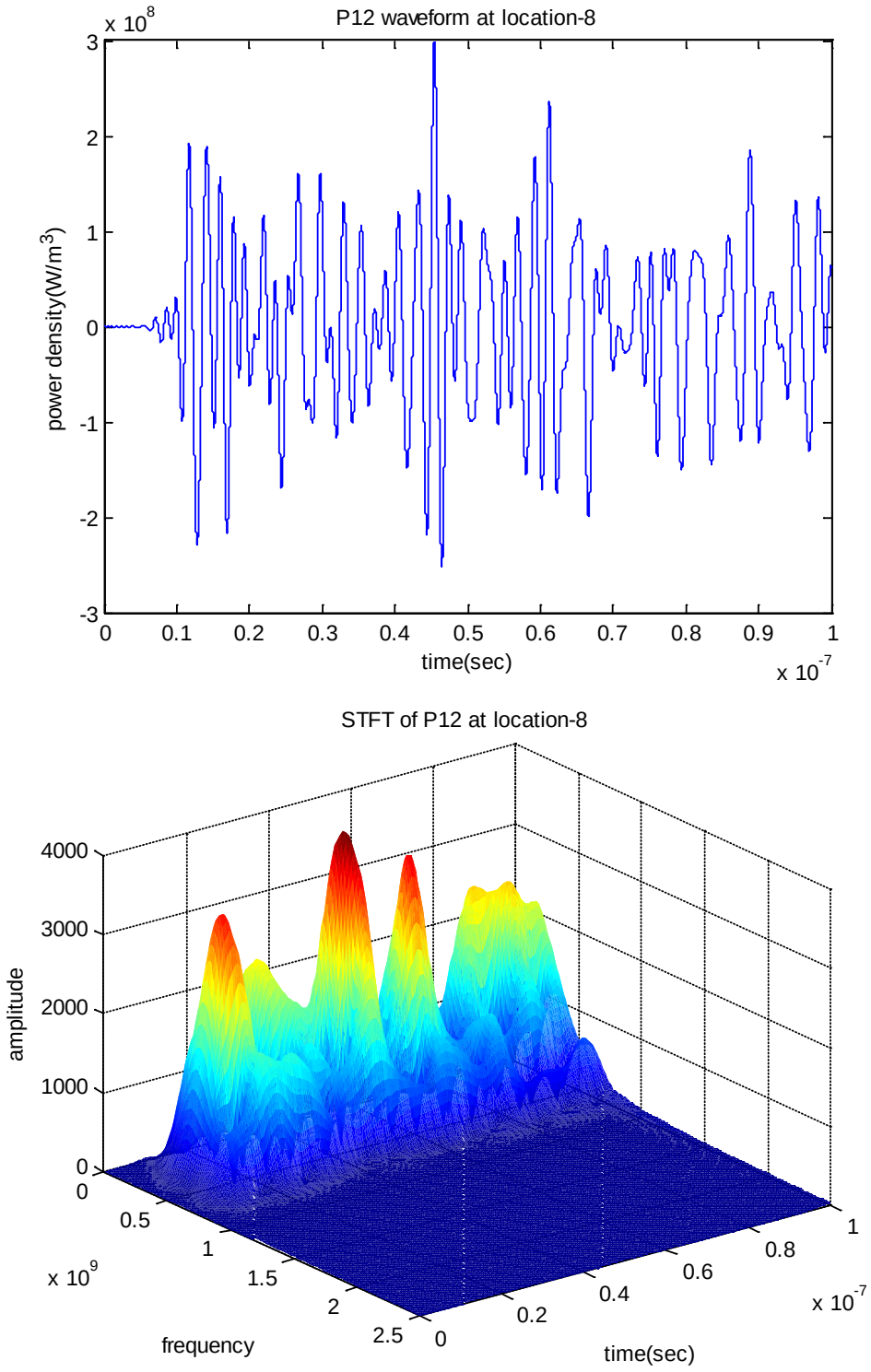

Fig. 4.39 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 8

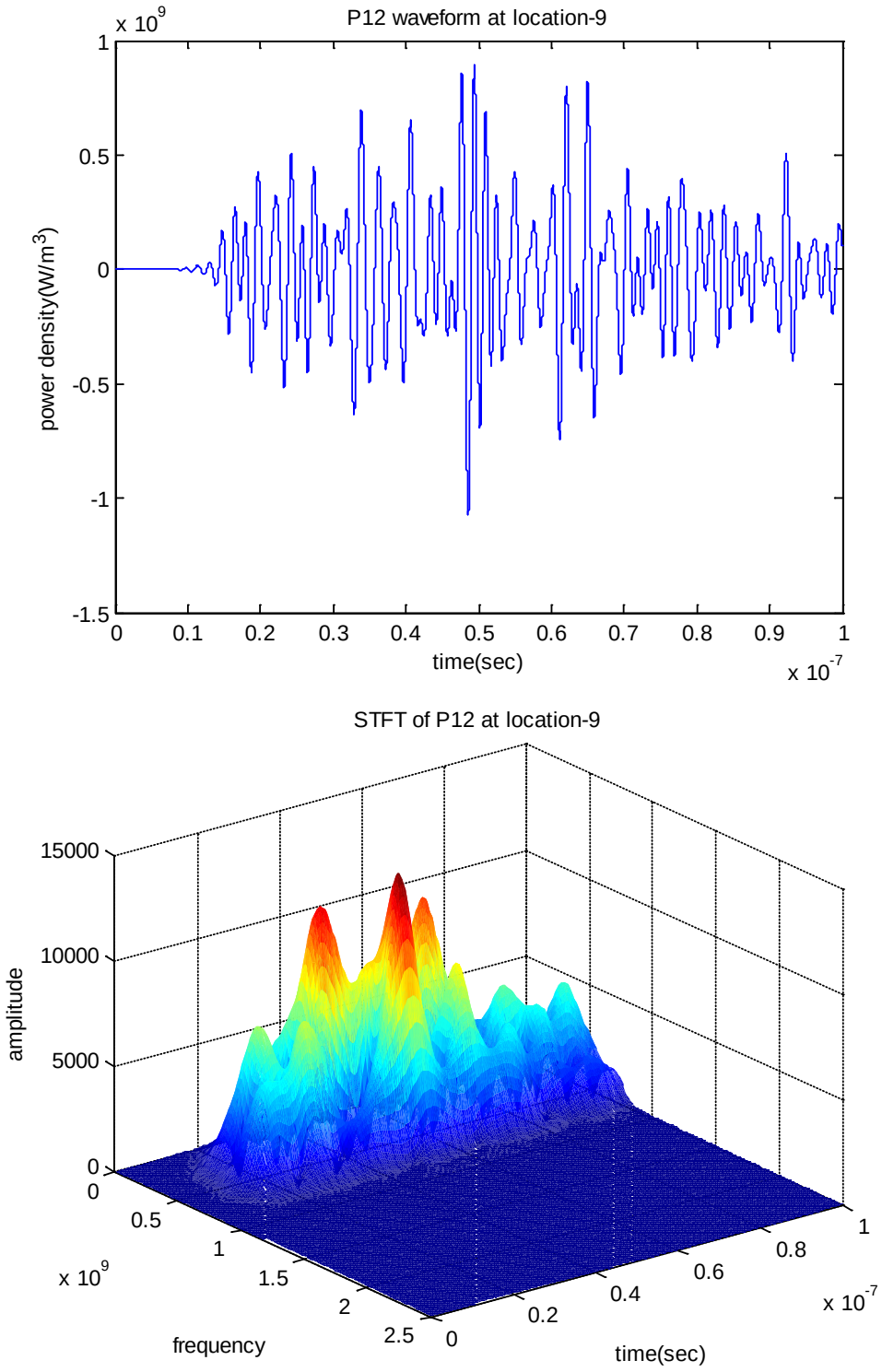

Fig. 4.40 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 9

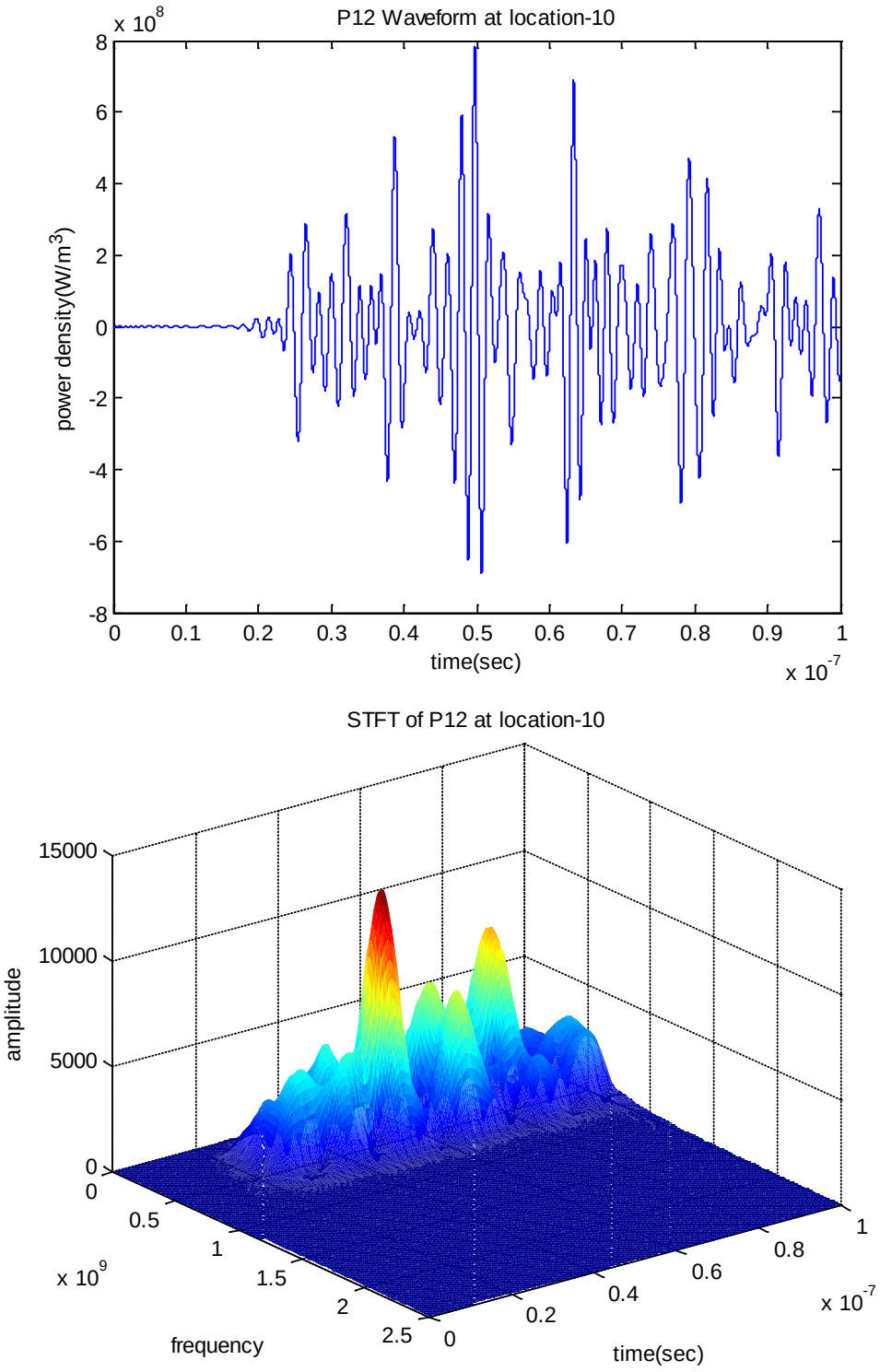

Fig. 4.41 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 10

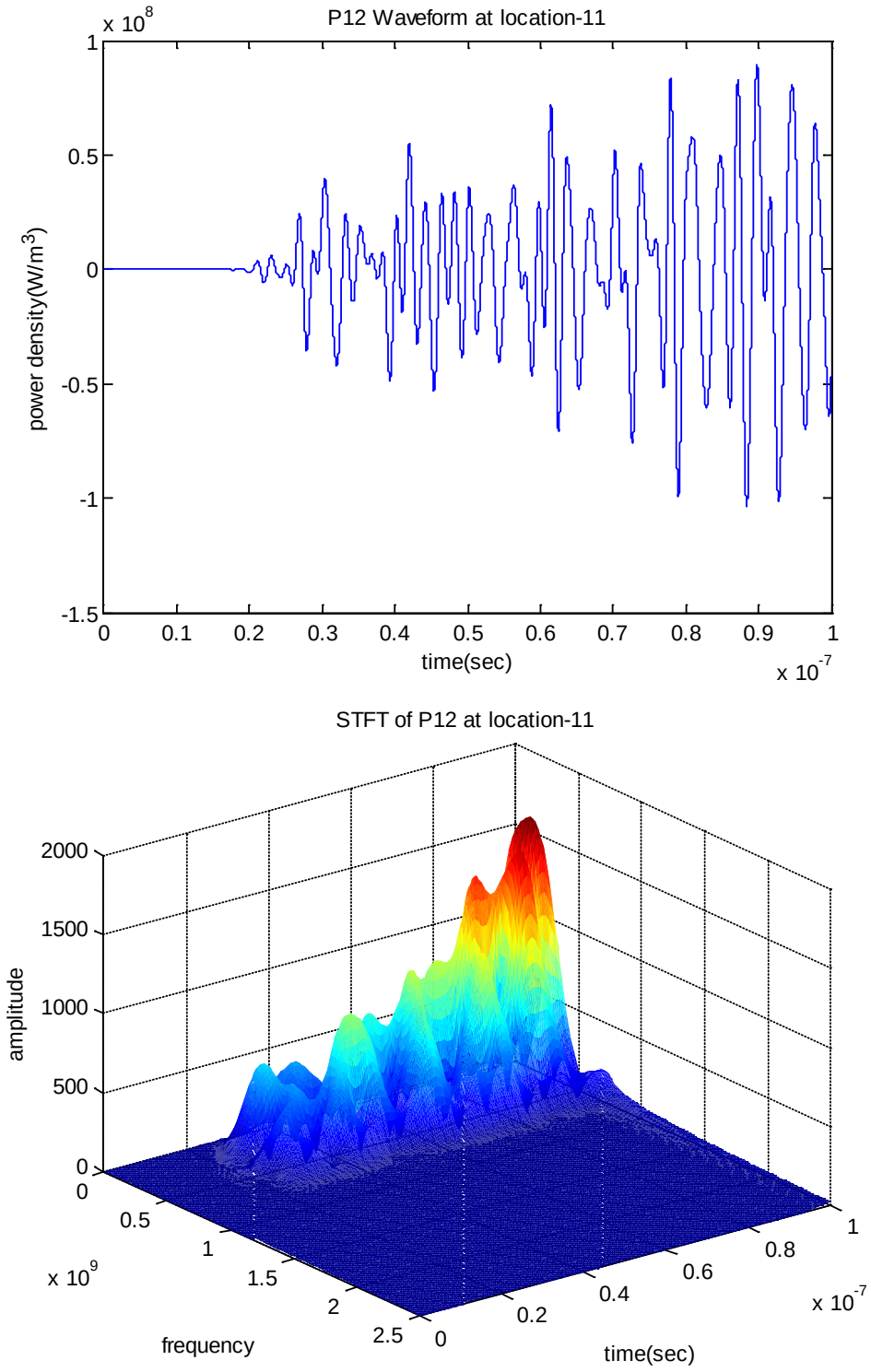

Fig. 4.42 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 11

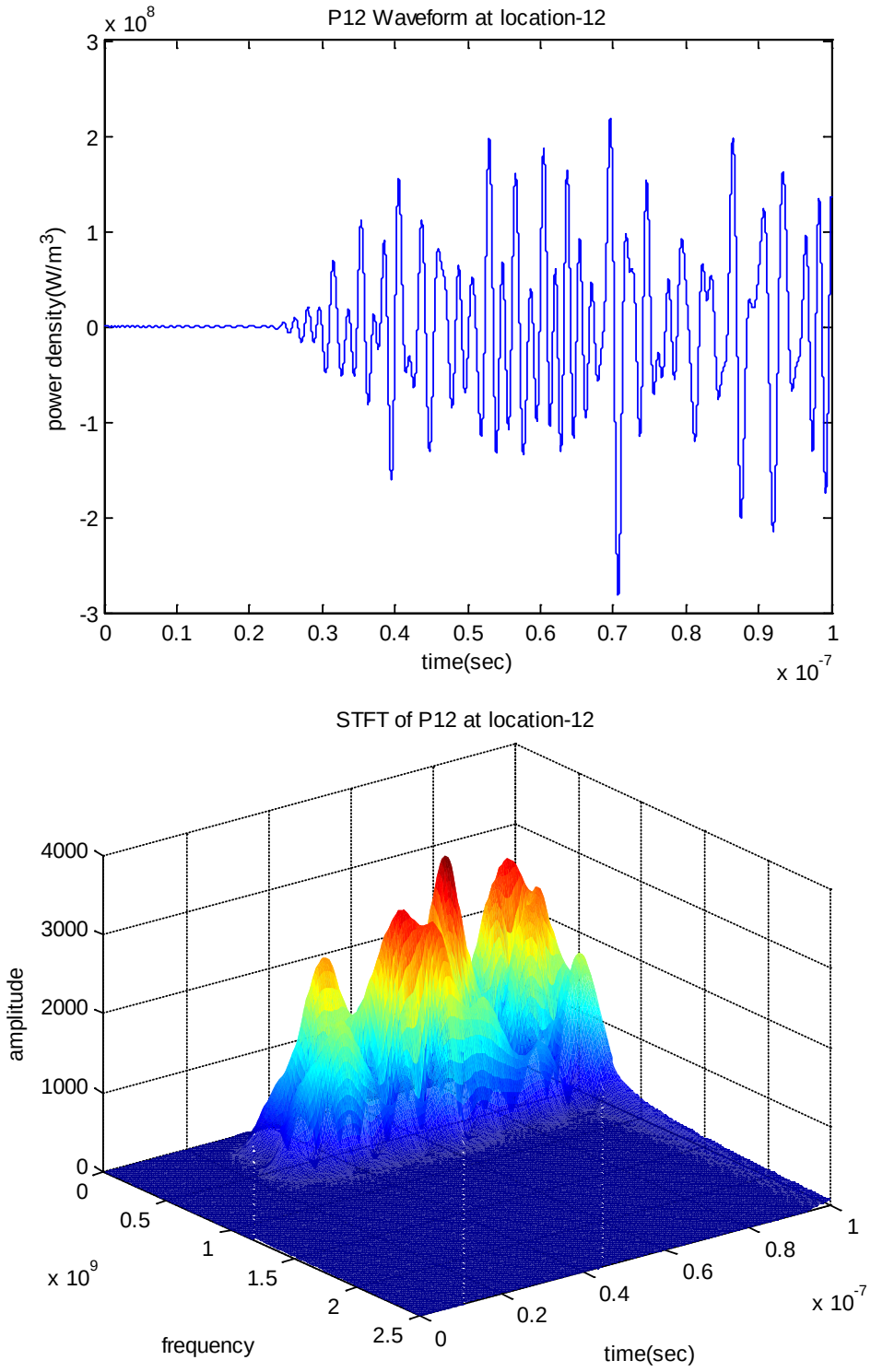

Fig. 4.43 Waveform and associated STFT of $\frac{\partial \sigma_{12}}{\partial t}$ at Location 12

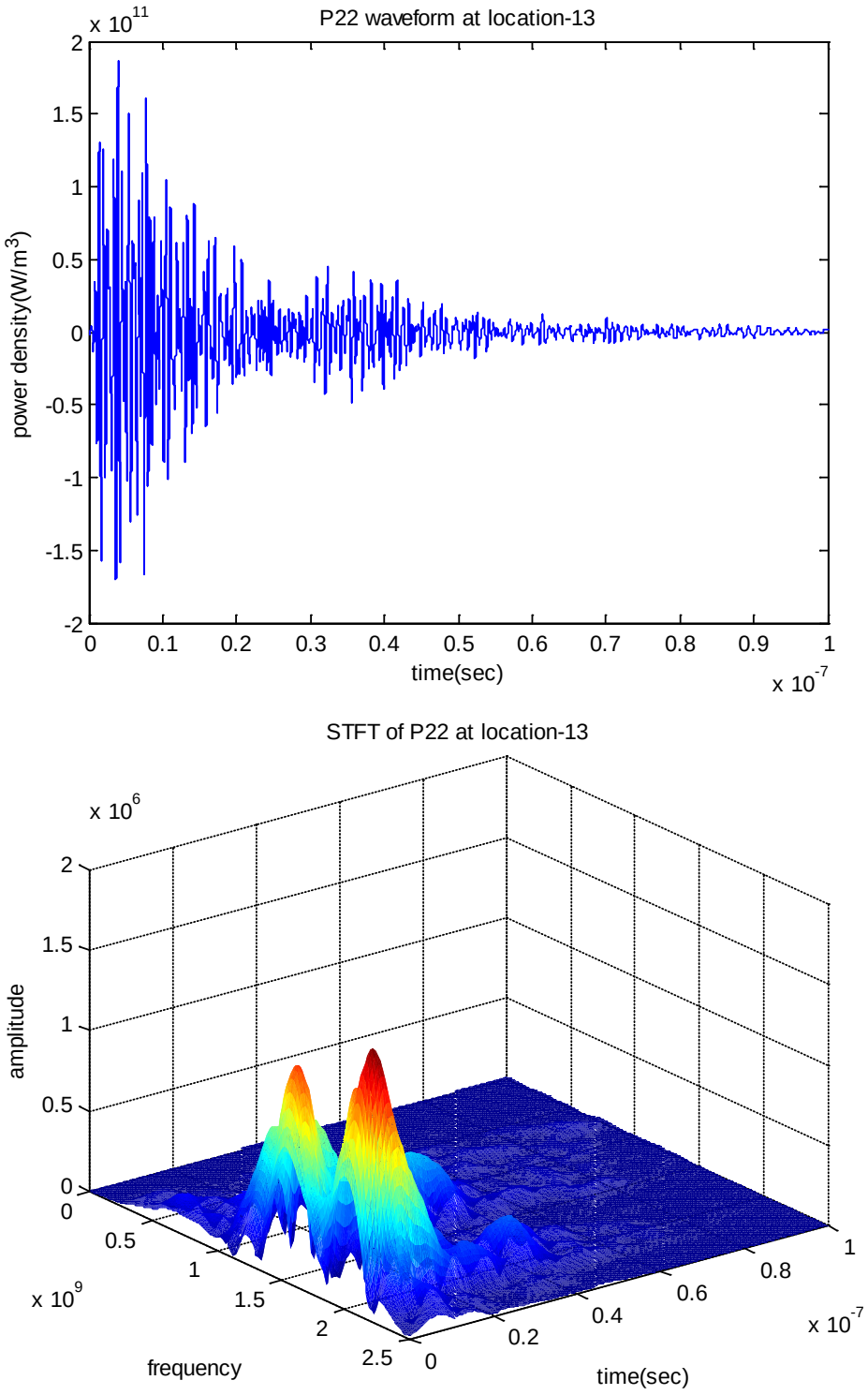

Fig. 4.44 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 13

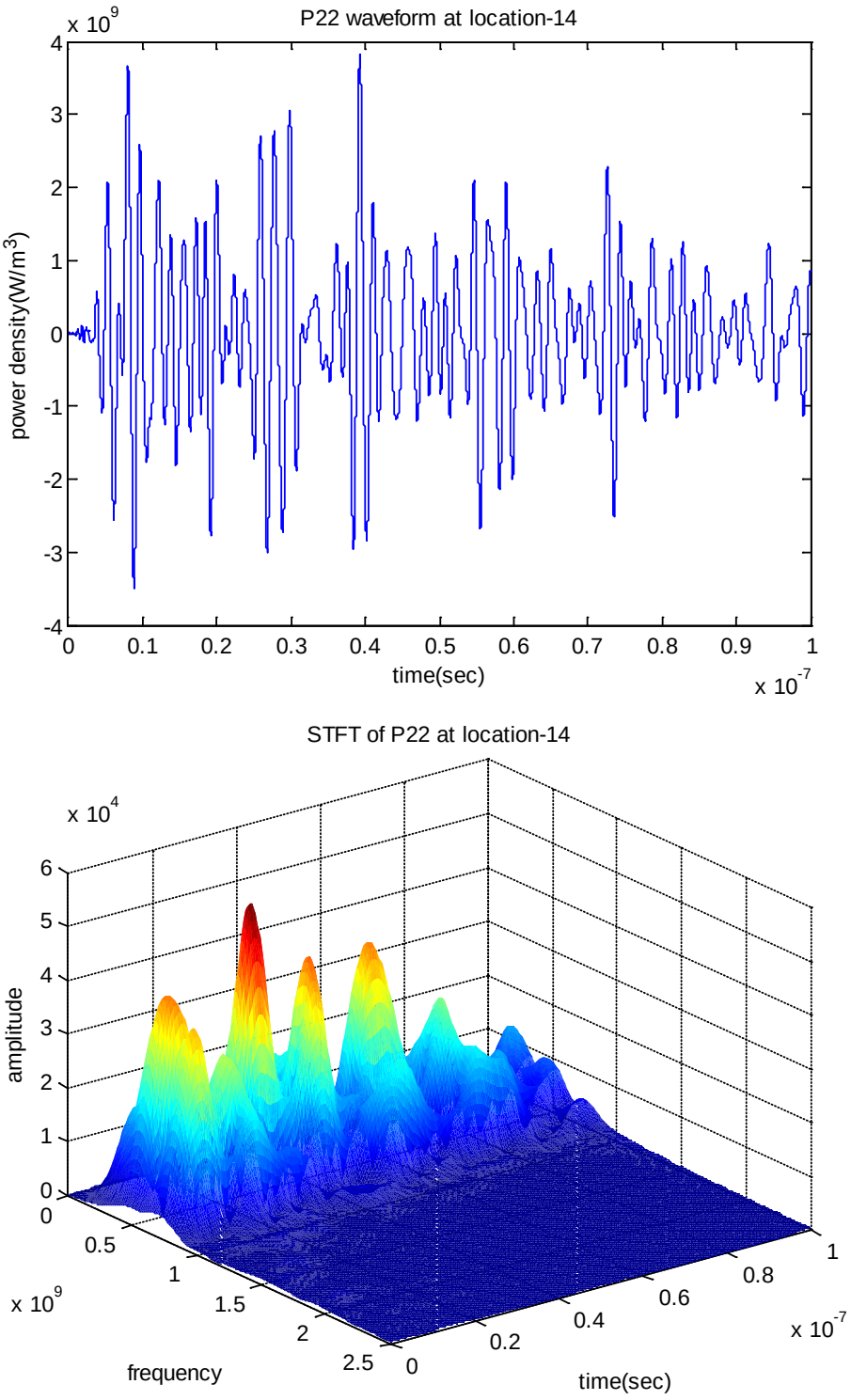

Fig. 4.45 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 14

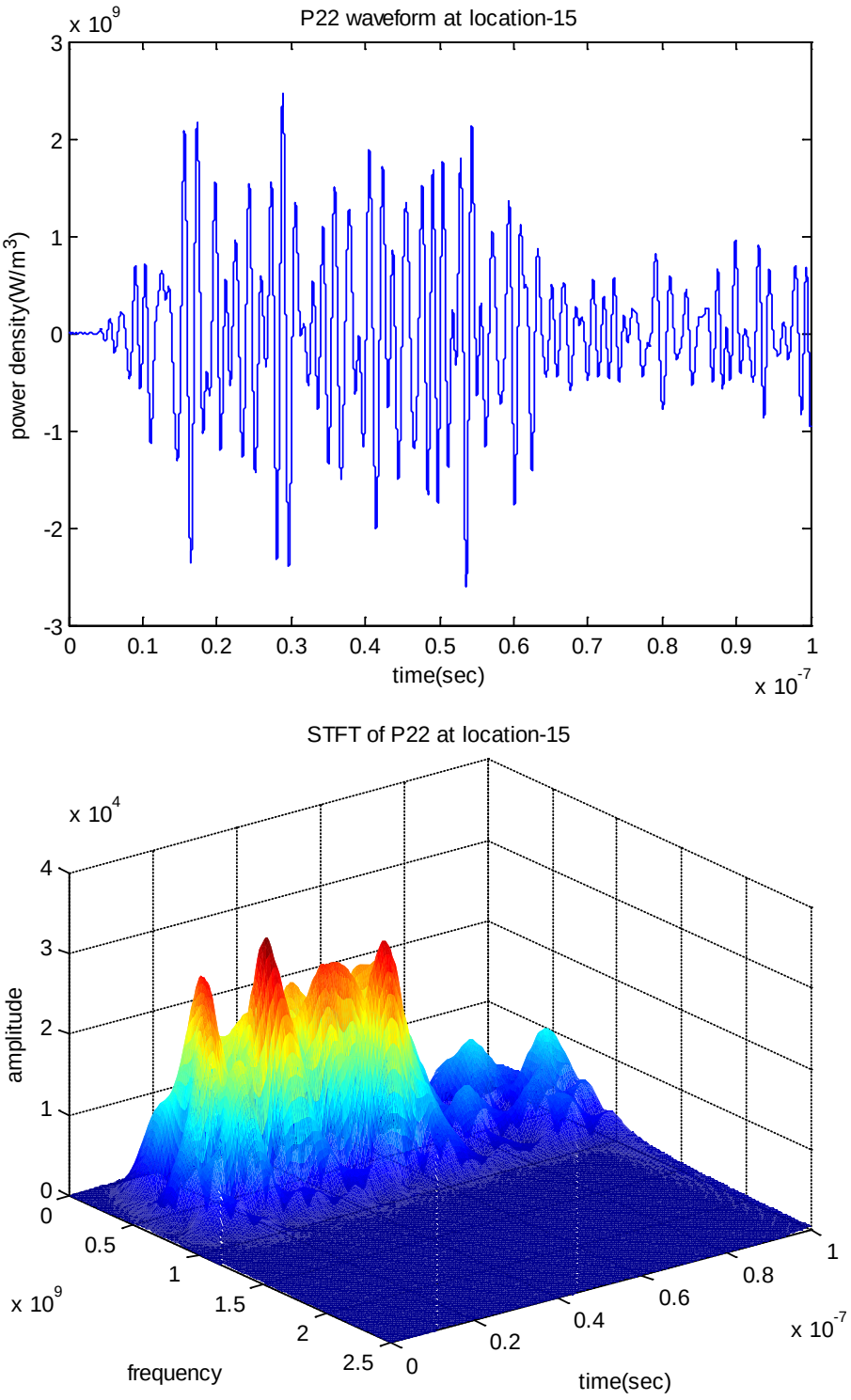

Fig. 4.46 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 15

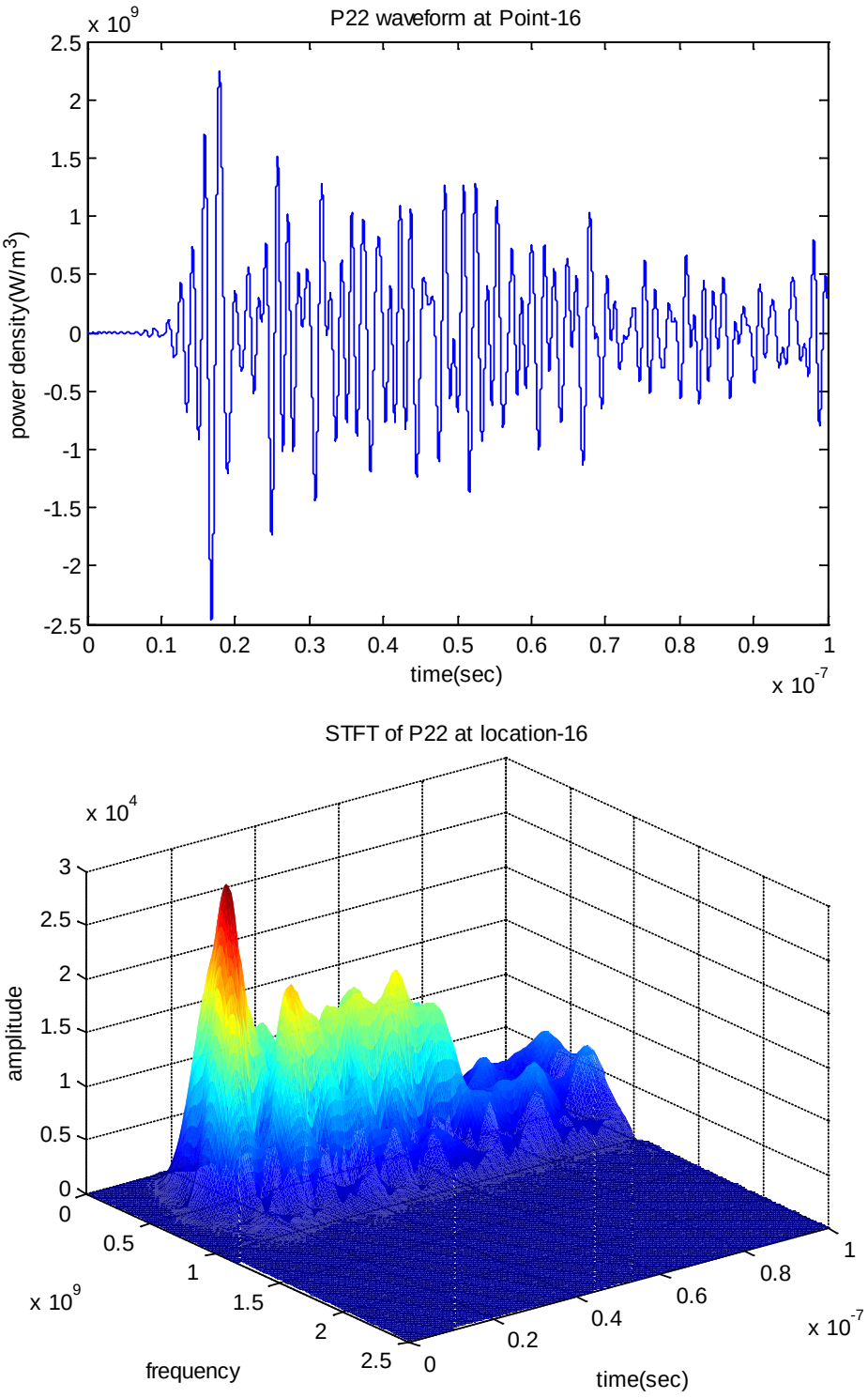

Fig. 4.47 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 16

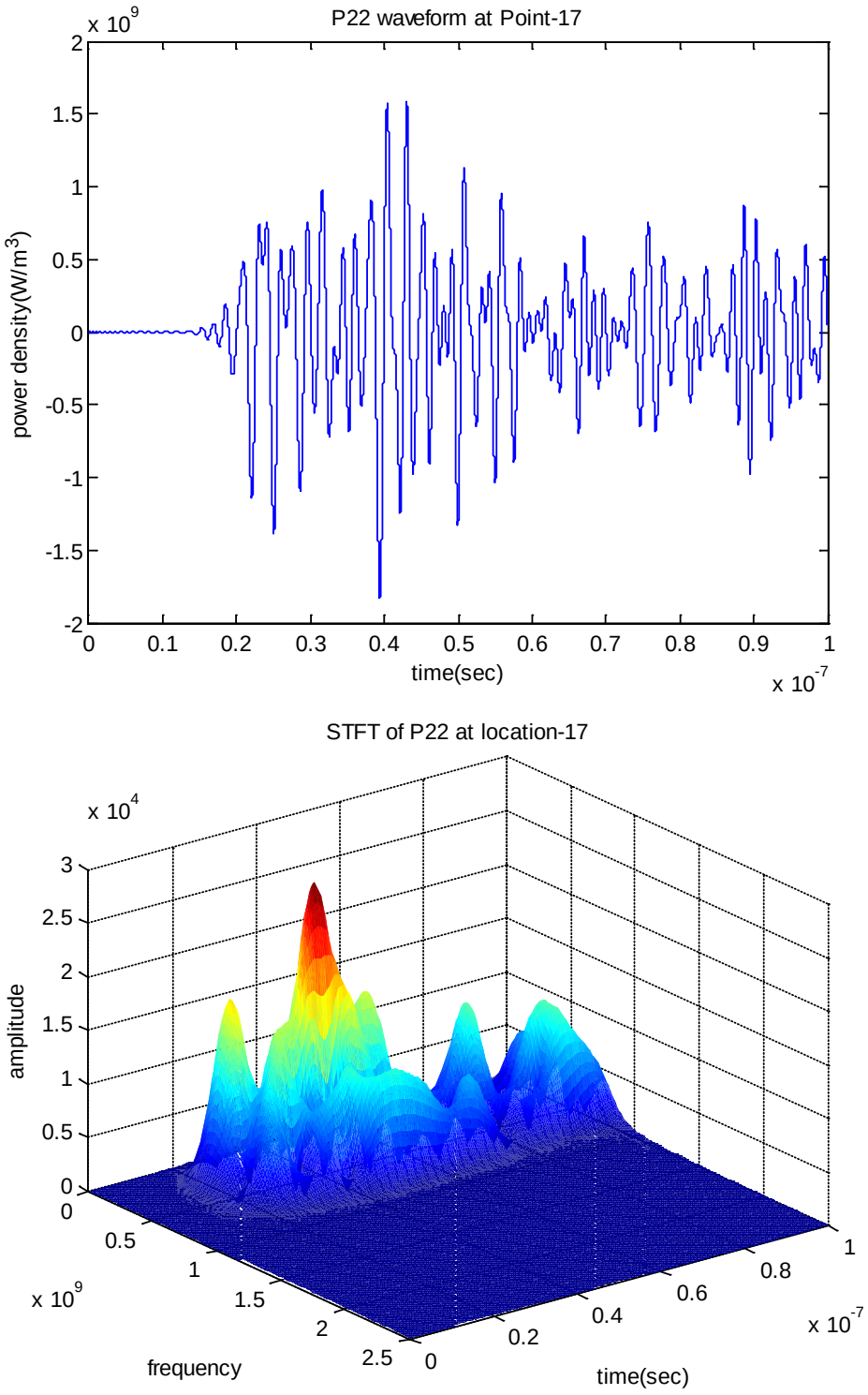

Fig. 4.48 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 17

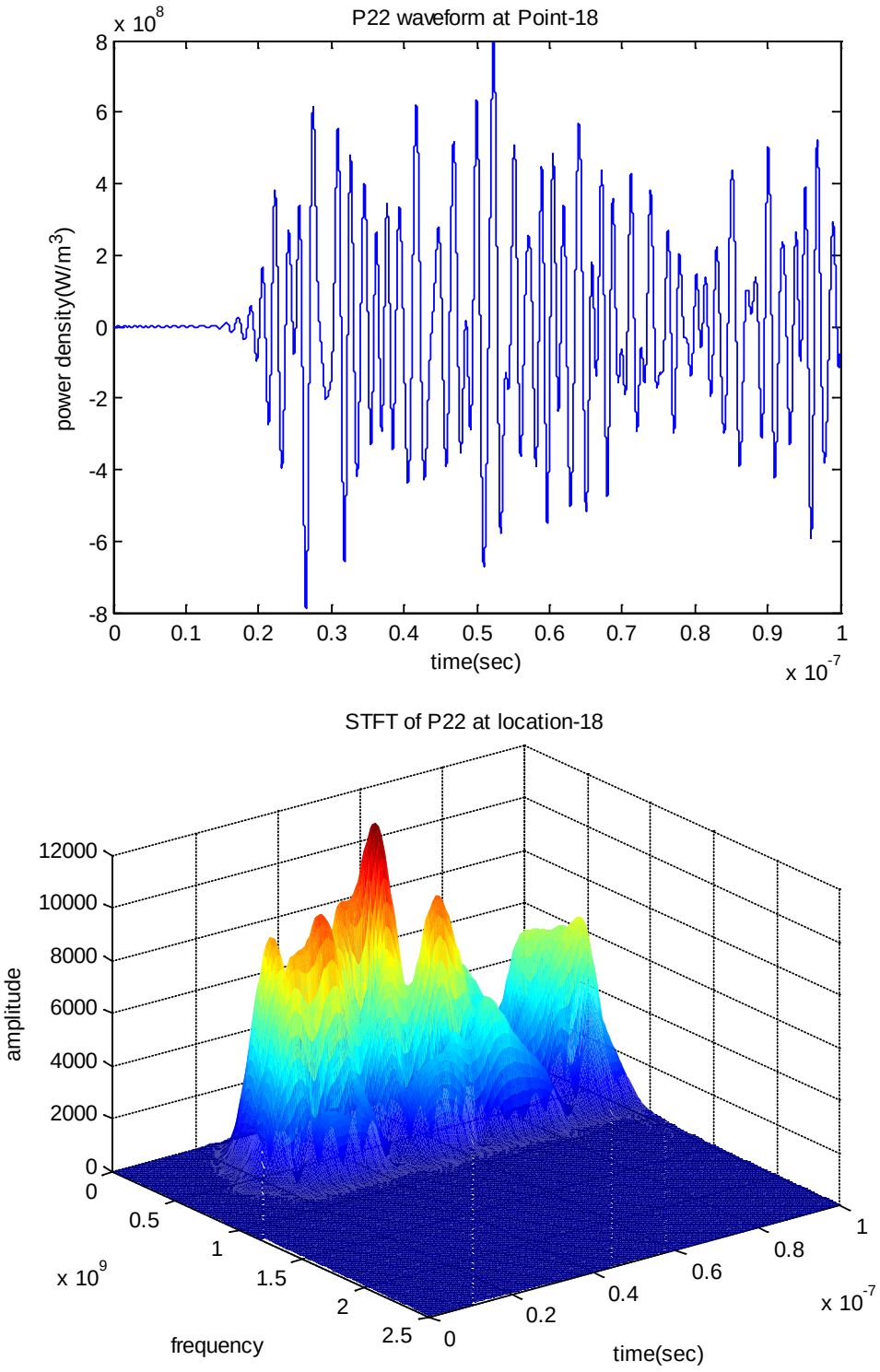

Fig. 4.49 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 18

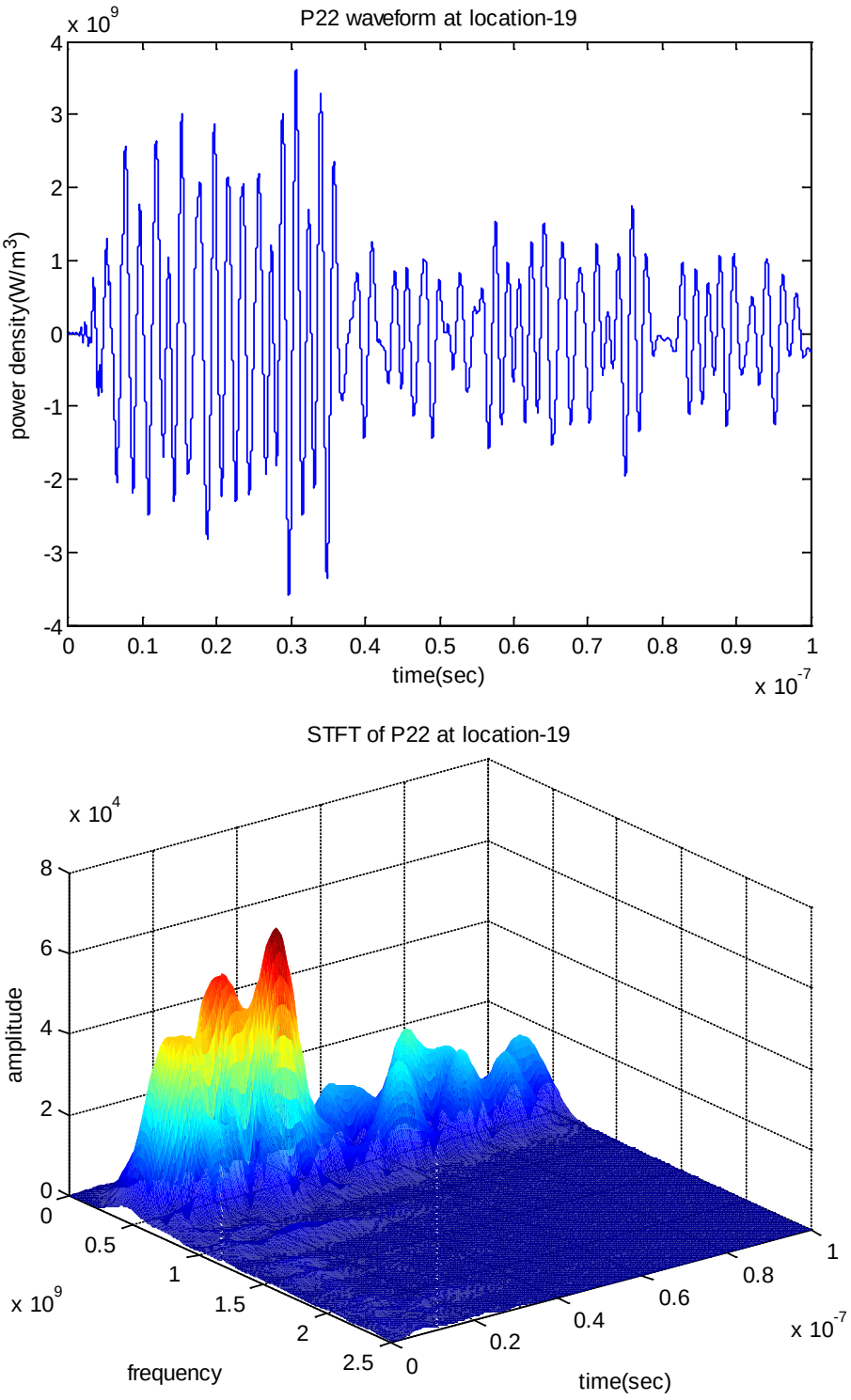

Fig. 4.50 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 19

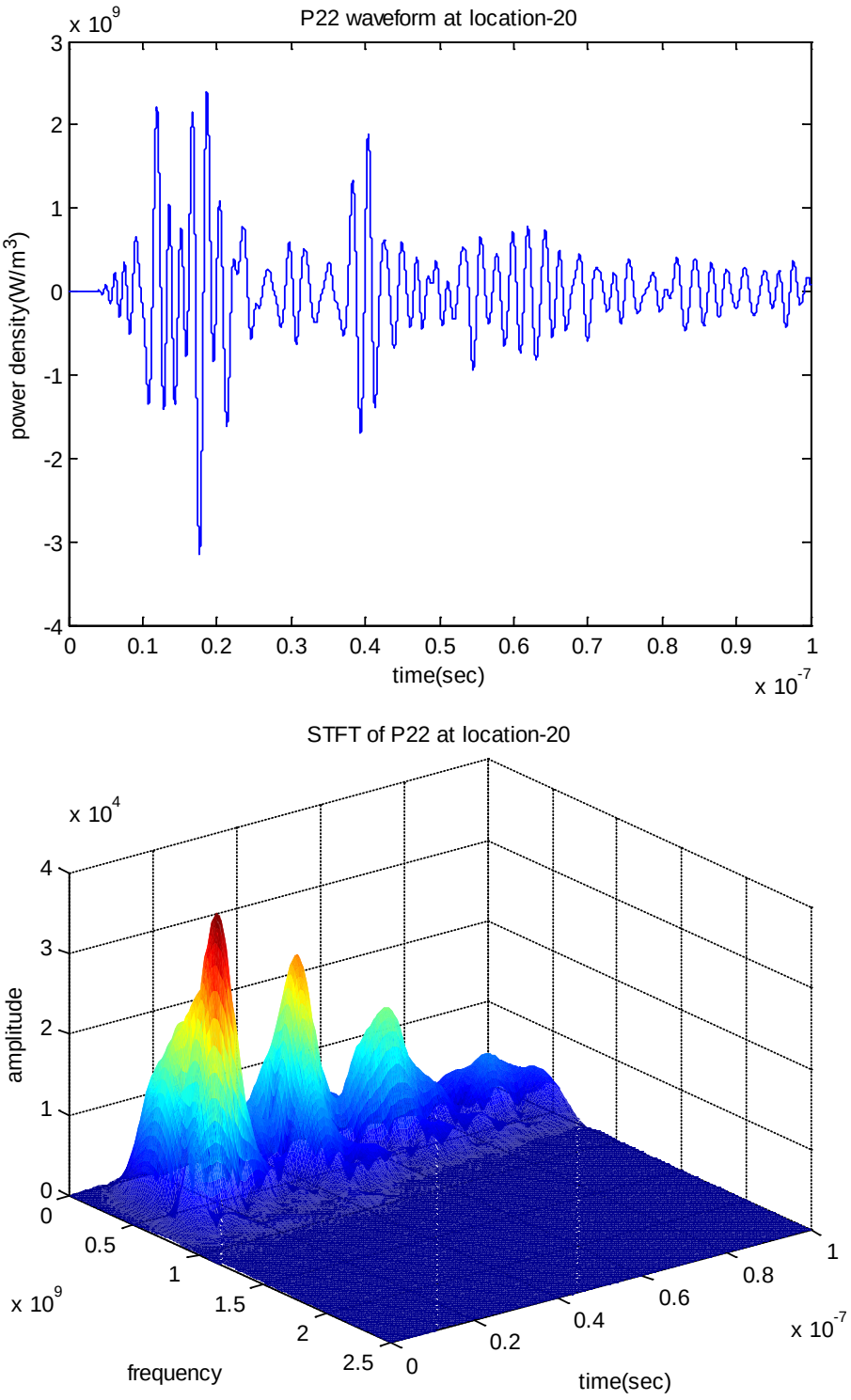

Fig. 4.51 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 20

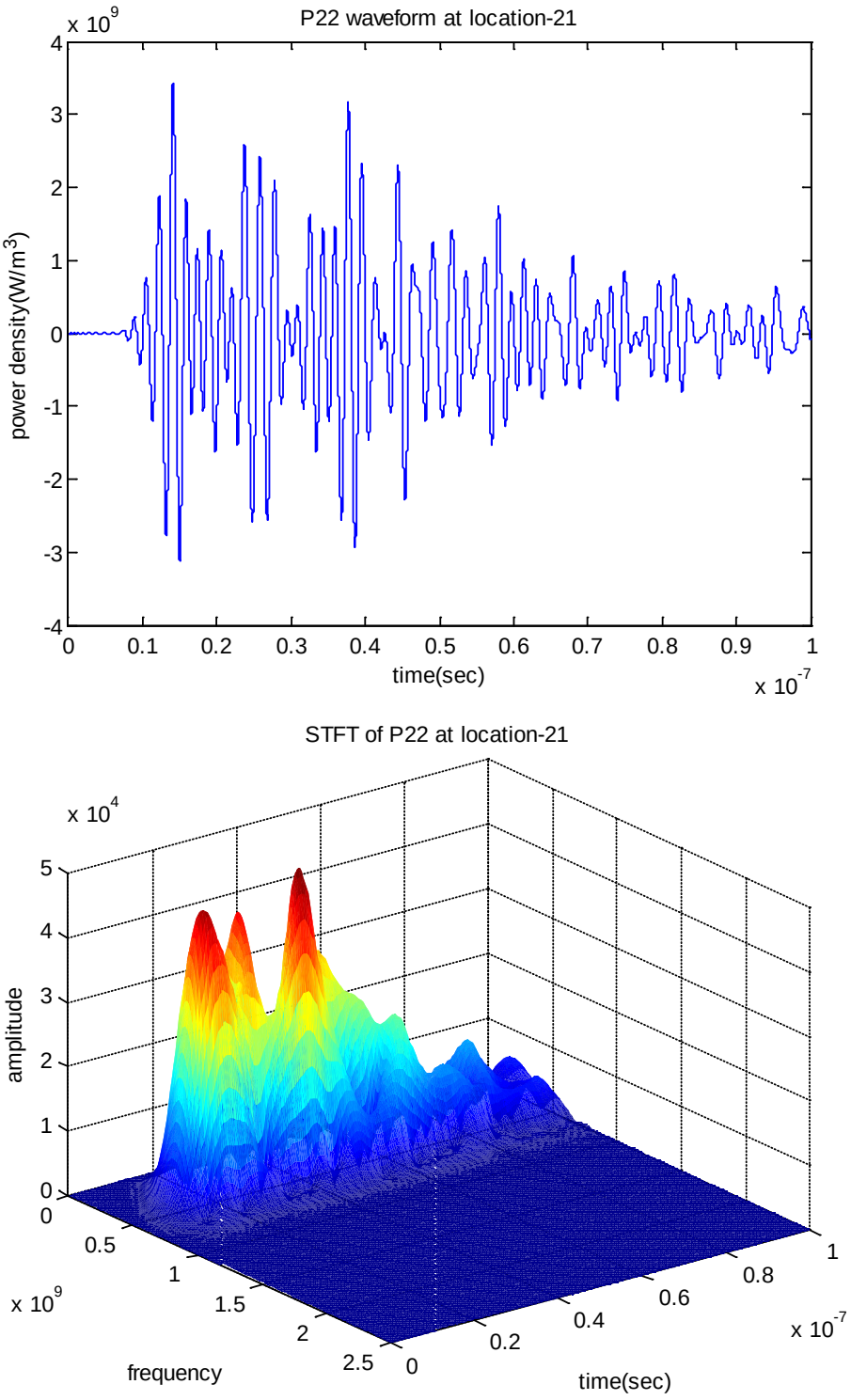

Fig. 4.52 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 21

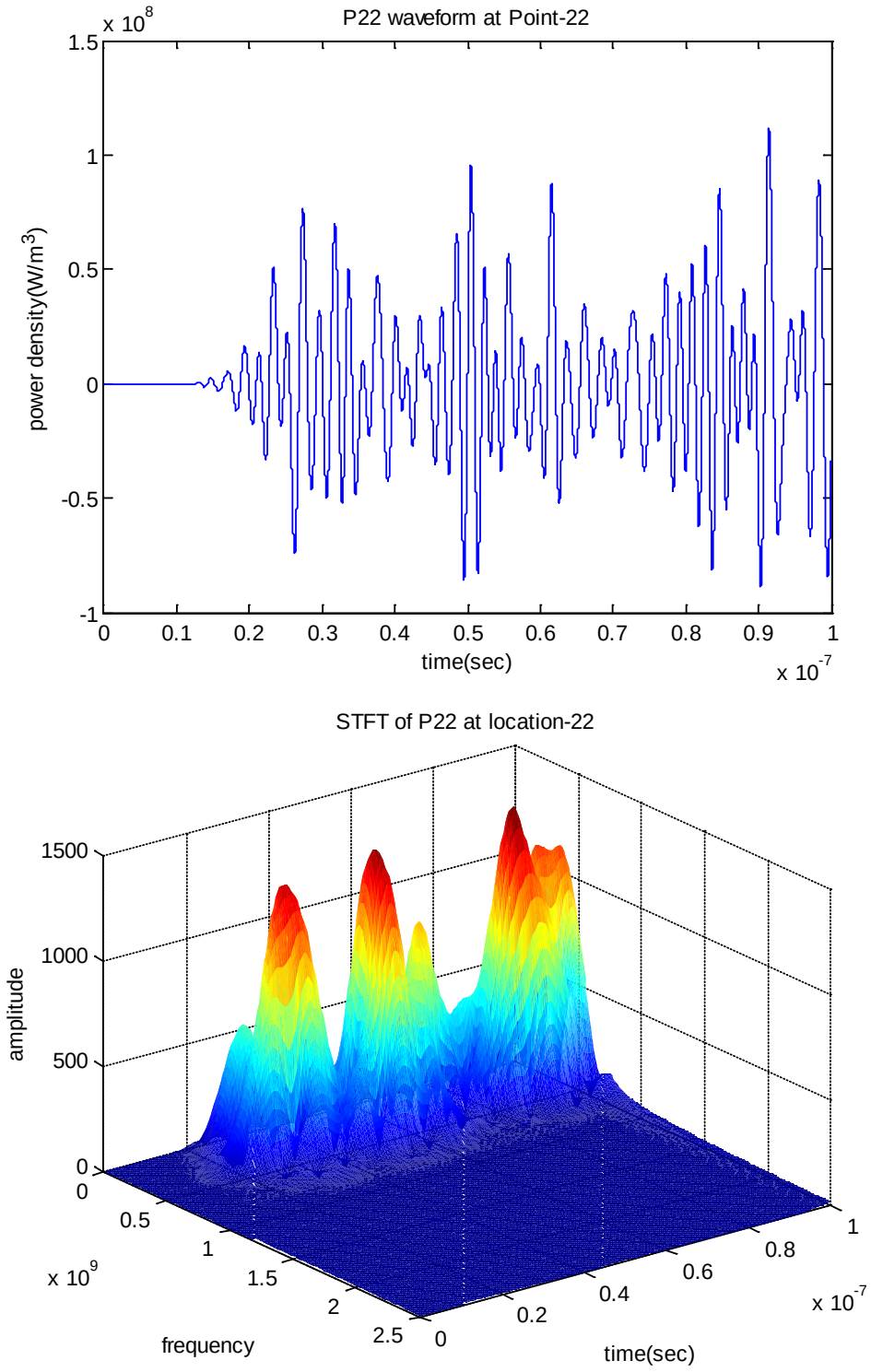

Fig. 4.53 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 22

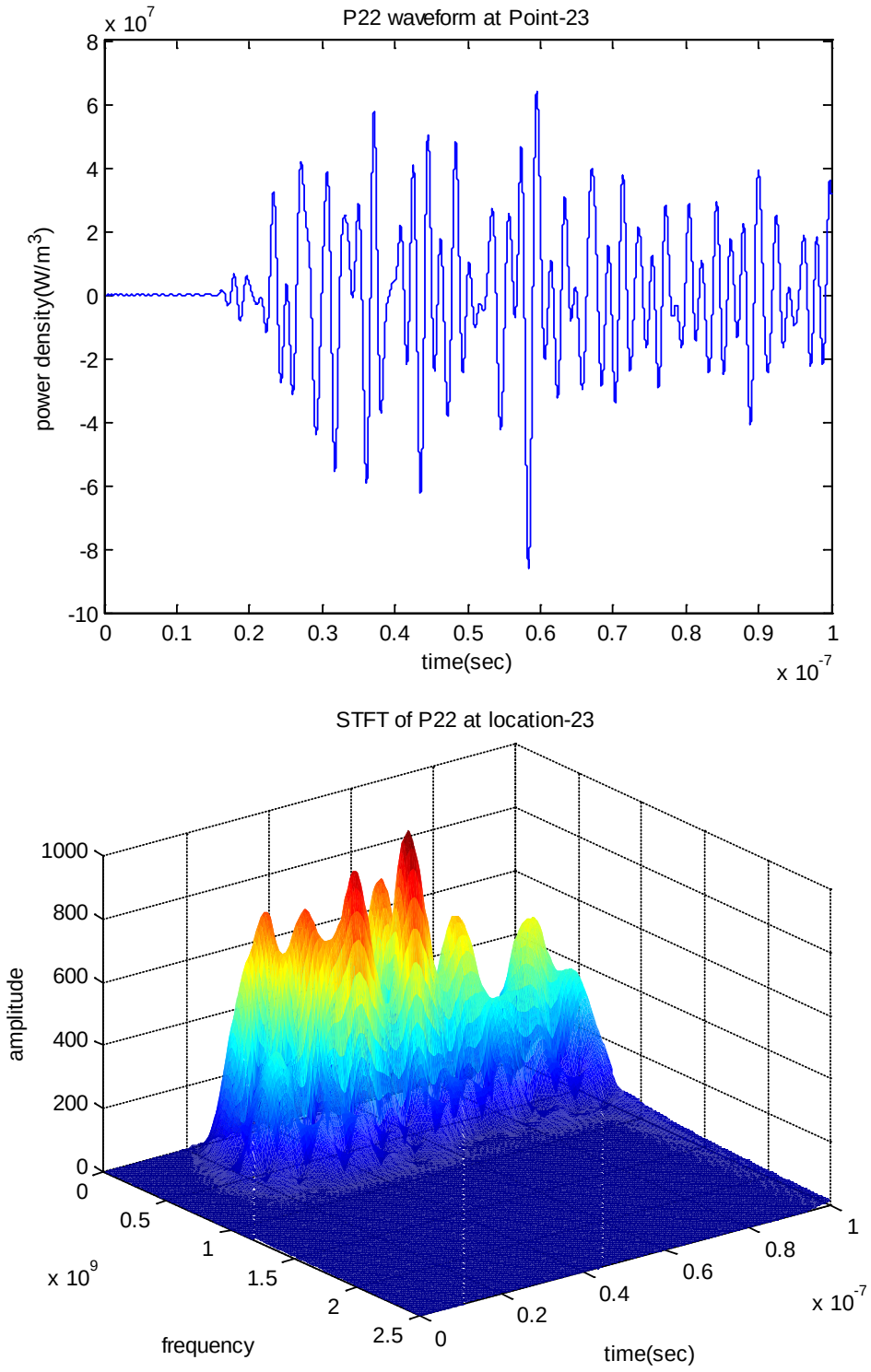

Fig. 4.54 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 23

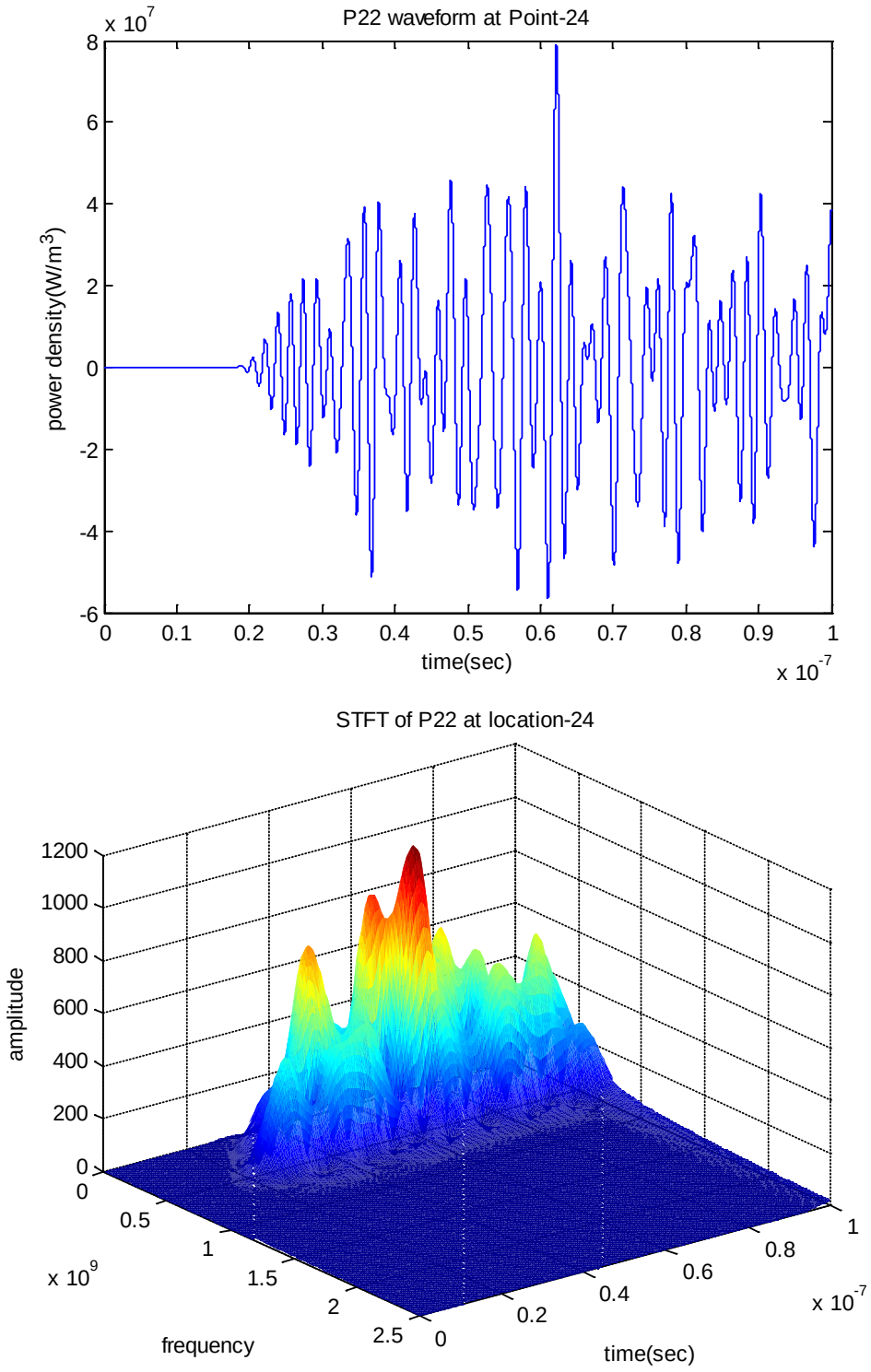

Fig. 4.55 Waveform and associated STFT of $\frac{\partial \sigma_{22}}{\partial t}$ at Location 24

4.4 Accumulated Damage Evaluation

4.4.1 Power Density and Fatigue Testing S-N Curve

The previous section presented that low amplitude but high frequency stress waves propagating in electronic devices contain extremely high power per unit volume. However, it is not obvious as to how the power density waves can be related to mechanical failure in the package. Besides, fatigue cycling tests usually proceed under the condition of MPa in stress magnitude with constant loading frequency, which is not readily applicable to correlating the failure mode resulted from short-time scale oscillating stresses. Thus, an alternative method is developed to investigate failure probability inside the package by comparing the generated stress waves with experimental fatigue test data [13].

Take eutectic solder for example. Eutectic solder is thought to be the part with high failure concern in flip-chips. The experimental S-N curve for eutectic solder using 1 Hz triangular profile loading can be expressed as:

$$S = (349.1 - 68.6 \log N) \cdot 10^6 \text{(Pa)} \tag{4.1}$$

where S is the stress magnitude and N is the number of cycling until failure occurs. Since the triangular loading is of 1 Hz, variation of S with respect to time can be approximated as:

$$\frac{dS}{dt} = 4 \cdot 10^6 \cdot (349.1 - 68.6 \log N) \text{(Pa/s)} \tag{4.2}$$

From Eq. (4.2), N can be expressed as a function of dS / dt with 99.9% reliability:

$$N_{solder} = 10^{[5.089 - 2.423 \cdot 10^{-9} \cdot dS/dt]} \tag{4.3}$$

Here dS/dt is the temporal gradient of the alternating stress, which is defined as "Power Density" in the previous section. The same procedure can be employed to obtain the dS/dt -N relation for copper, which is the TSV material used in the flip-chip. The S-logN relation of copper can be obtained from curve-fitting the experimental data in [22].

$$S = (-14.33 \log N + 188.2) \cdot 10^6 (Pa) \tag{4.4}$$

The N- dS/dt of copper is:

$$N_{copper} = 10^{[13.133 - 6.978 \cdot 10^{-9} \cdot dS/dt]} \tag{4.5}$$

4.4.2 Methodology of Accumulated Damage Evaluation

The time-frequency analysis showed that the short-time scale stress waves were broadband and their bandwidth varied with time. However, experimental data from fatigue cycling test does not offer a direct relationship between the multi-frequency loading and the number of cycles till failure. Thus, it is necessary to extract frequency components from the stress waves and study the damage caused by individual loading frequency. Acumulated damage evaluation is to predict the total possible damages caused by each loading frequency component. Since fatigue cycling test usually applies a sinusoidal load to test specimens, the magnitude of stress $S(t)$ expressed in the time domain is:

$$S(t) = S_{\max} \cdot \sin(2\pi ft) \tag{4.6}$$

where $S_{\max}$ is the maximum loading amplitude and f is the loading frequency.

Taking the time derivative of Eq. (4.6), the power density in fatigue test is then

$$dS / dt = M \cdot \cos(2\pi ft) \tag{4.7}$$

where M is the amplitude.

The first step of the accumulated damage evaluation is to determine the frequency component and the corresponding amplitude of the power density wave in each time step. Assume at a given time, $t = t_0$, the power density $(dS / dt)_{t_0}$ can be decomposed into a series of cosine signals:

$$(dS / dt)_{t_0} = \sum_i A_i \cos(f_i \Delta t) \tag{4.8}$$

where f_i is the component frequency of $(dS / dt)_{t_0}$, A_i is the amplitude corresponding to each cosine function of f_i, and Δt is the time interval within which power density is being determined. Since f_i can be obtained from the STFT of $(dS / dt)_{t_0}$, A_i can be derived by comparing the summation of each individual cosine signal multiplied by its corresponding STFT amplitude with the $(dS / dt)_{t_0}$ value. Take the STFT of $(dS / dt)_{t_0}$ in Fig. 4.56 for example, the component frequencies of $(dS / dt)_{t_0}$ are f1 to f5 and the corresponding amplitude of these frequencies are B1 to B5. Thus, $(dS / dt)_{t_0}$ can be expressed as:

$$\begin{aligned}(d\ \ Sd\ )t_0 = A \cdot [&B1 \cdot \cos(\Delta t \cdot f1) + B2 \cdot \cos(\Delta t \cdot f2) + B3 \cdot \cos(\Delta t \cdot f3) \\ &+ B4 \cdot \cos(\Delta t \cdot f4) + B5 \cdot \cos(\Delta t \cdot f5)]\end{aligned} \tag{4.9}$$

Comparing Eqs. (4.5) and (4.6), we obtain:

$$A_i = A \cdot Bi \tag{4.10}$$

where $A = \dfrac{(dS/dt)_{t_0}}{\sum_j Bj \cdot \cos(\Delta t \cdot fj)}$

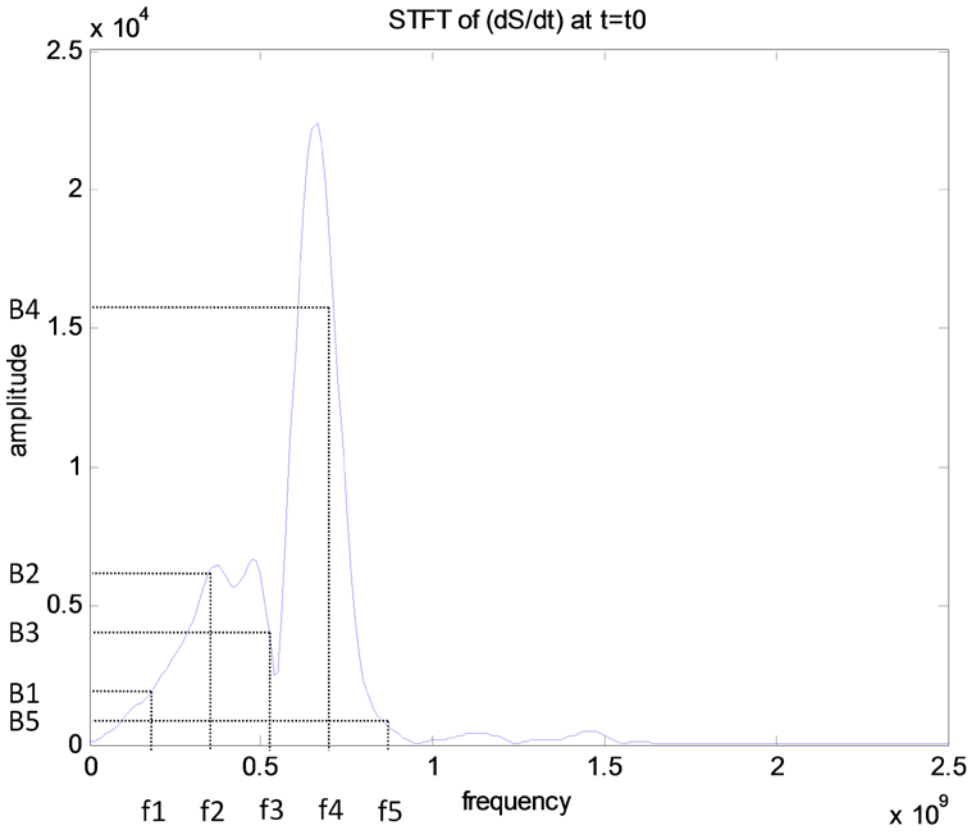

Fig. 4.56 STFT of $(dS/dt)_{t_0}$

The accumulated damage (A.D.) at the specific time $t = t_0$ within the time interval Δt is defined as the summation of the damages caused by all component frequency, f_i as

$$\text{A.D.}: \sum_i \frac{N_i}{(N_f)_i} \qquad (4.11)$$

where N_i is the number of cycles at loading frequency f_i within the time interval Δt, $N_i = f_i \cdot \Delta t$ and $(N_f)_i$ is the number of fatigue cycles associated with A_i until failure, which can be calculated from Eq. (4.3).

For a given time period divided into j time steps, the total accumulated damage (T.A.D.) over the period can be expressed as

$$\text{T.A.D.}: \sum_j \sum_i \frac{N_i}{(N_f)_i} \tag{4.12}$$

The criterion for crack initiating in a material is defined by:

$$\text{T.A.D.}: \sum_j \sum_i \frac{N_i}{(N_f)_i} \geq 1 \tag{4.13}$$

4.4.3 TSV Flip-Chip Package Accumulated Damage Evaluation

Since crack initiation is the dominant mechanical failure mode in high-cycle, low-stress fatigue tests, the assumption relating oscillating loading in the TSV flip-chip package to high cycle fatigue test is valid. The S-N curves considered herein represent curve-fitting results from scattered experimental data. There is always uncontrolled variations affecting the N_f value in different experiments when subjected to the same magnitude of loading S. So accumulated damage values should always be regarded as a

probability indicator where the larger value implies the higher probability for submicron crack nucleation to exist.

Fig. 4.57 shows the locations at which accumulated damage evaluation caused by the $\partial\sigma_{22}/\partial t$ waves are considered. Fig. 4.58 is the T.A.D. plot showing the probability of crack formation with respect to time in the 1st and 2nd TSVs. Accumulated damage evaluation indicates that cracks occur in each observation location within 40 ns. Fig. 4.59 shows the probability of crack formation in the 1st and 2nd solders. Cracks could occur at 17ns in the 1st solder, but no crack formation would be expected in the 2nd solder. It is not surprising that the closer to the heat source, the faster and higher probability cracking would initiate. Those locations where cracks are indicated to exist correspond to at least an order of magnitude higher of the power density waves than those without cracks.

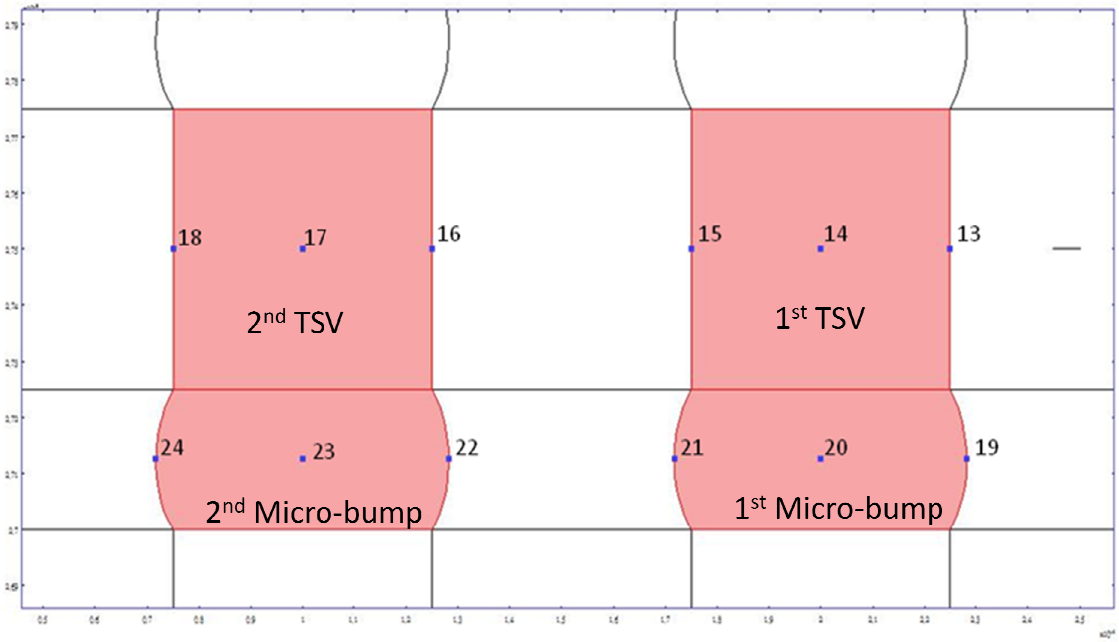

Fig. 4.57 Locations for accumulated damage evaluation inflicted by $\partial\sigma_{22}/\partial t$

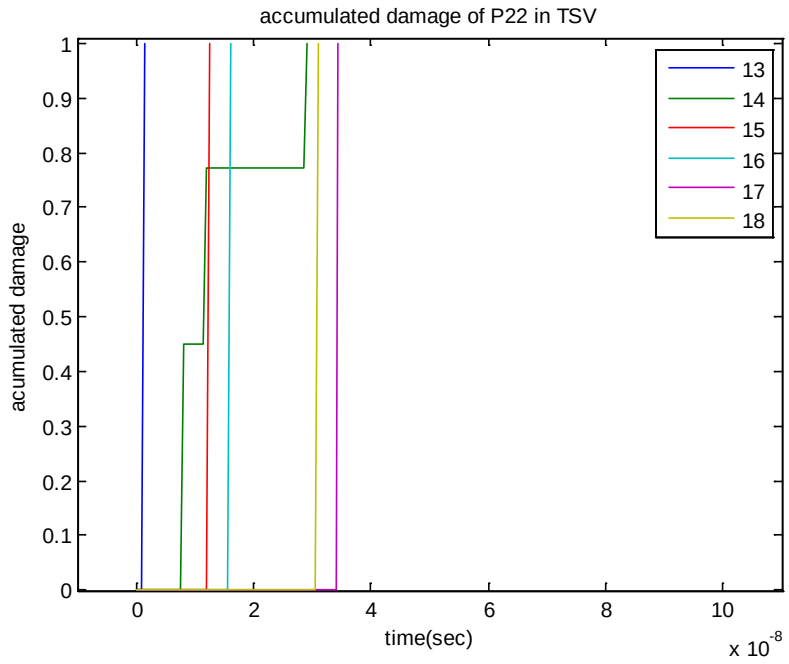

Fig. 4.58 A.D within 1st and 2nd TSVs by $\partial\sigma_{22}/\partial t$

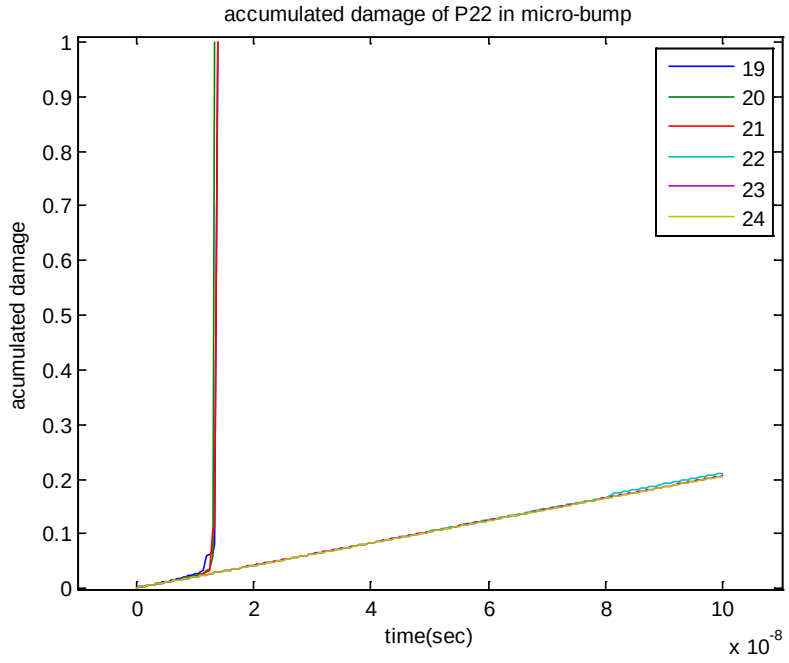

Fig. 4.59 A.D within 1st and 2nd Micro-bumps by $\partial\sigma_{22}/\partial t$

The same procedure is applied to predict the failure mode at dissimilar material interface based on the assumption that accumulated damage caused by the $\partial\sigma_{12}/\partial t$ power density waves would lead to delamination. Since there is no available experimental data on failure test at interface between dissimilar materials, the dS/dt -N curve of solder is modified by assuming the number of cycles until failure occur at dissimilar material interface to be one order of magnitude lower than the solder material employed before when subjected to the same magnitude of load. Thus,

$$N_{\text{interface}} = 10^{[6.089 - 2.423 \cdot 10^{-9} \cdot dS/dt]} \tag{4.11}$$

To more accurately predict the crack formation at bi-material interface using the above approach, experimental data will be needed. Fig. 4.60 gives the locations at which accumulated damage evaluation due to $\partial\sigma_{12}/\partial t$ power density waves are considered. The results are presented in Figs 4.61 and 4.62. From the evaluated data, delamination would probably be seen at most dissimilar material interfaces except for Locations 8, 11, and 12. The reason why the predicted accumulated damage values at Locations 8 and 11 are merely 2.7% can be explained as follows. The comparatively lower stiffness of the solder material and further attenuation of the wave together result in lower power density, thus less accumulated damage.

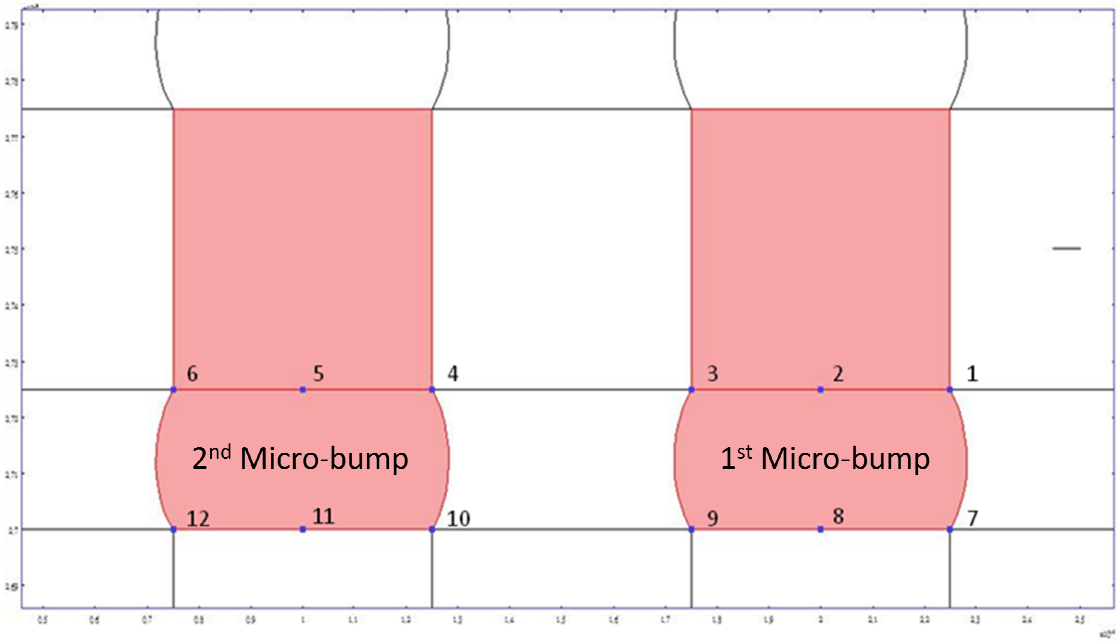

Fig. 4.60 Locations for accumulated damage evaluation inflicted by $\partial\sigma_{12}/\partial t$

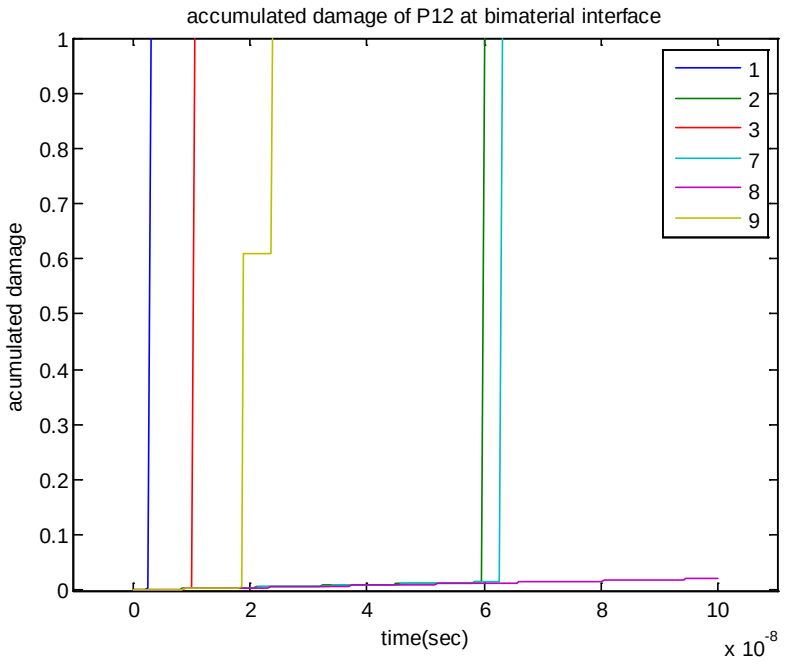

Fig. 4.61 A.D at interface of 1st solders by $\partial\sigma_{12}/\partial t$

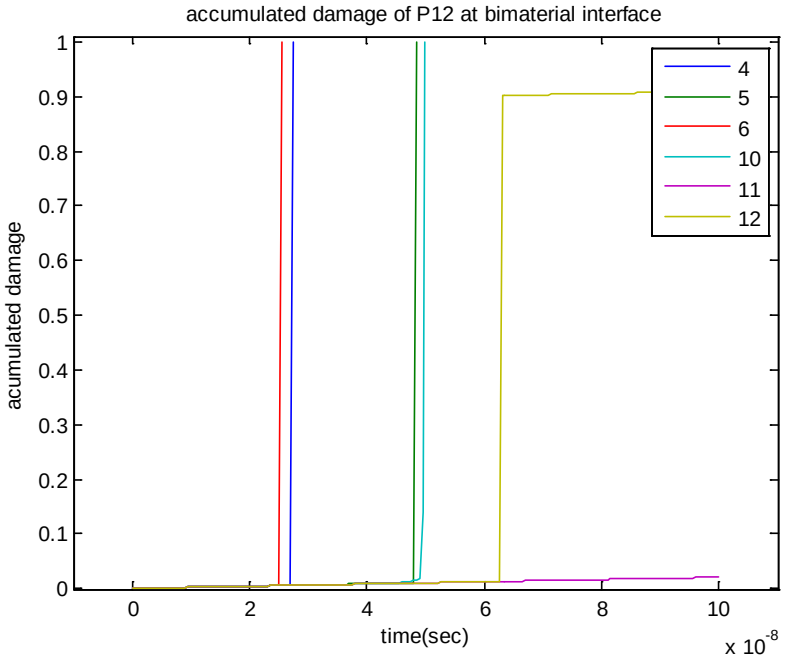

Fig. 4.62 A.D at interface of 2nd solders by $\partial\sigma_{12}/\partial t$

Table 4.1 Crack initiation time at each location

Location	Crack initiation time (ns)
1	3
2	60
3	10.5
4	27.5
5	48.5
6	25.5
7	63
8	No failure
9	24
10	50
11	No failure
12	No failure
13	1.5
14	29
15	12.5
16	16
17	34.5
18	31
19	14
20	13.5
21	14
22	No failure
23	No failure
24	No failure

4.5 Discussions

The crack initiation time at each location obtained from accumulated damage evaluation is shown in Table 4.1. In summary, since directly hit by power density waves of large magnitude, the probability for micron crack formation is extremely high at Locations 13 through 15 within the 1st TSV. When power density waves pass through high stiffness silicon wafer, there is no obvious attenuation in the 2nd TSV, thus, both TSVs fast exhibit micron crack generation upon power-on. The 1st micro-bump is also subjected to the infliction of high power density waves and micron cracking could occur at the same time when they appear in the 1st TSV. Furthermore, delamination at the four-material interfaces is anticipated, even the farthest Location 12 receives a 90% accumulated damage, which might eventually lead to crack initiation if the investigated time window were extended. Debonding between two the TSVs and their connected solder balls is also expected. When long-time scale effect becomes prominent, the local area of the silicon die where heat source is located will possibly lose electric connection to other components.

CHAPTER V

CONCLUSION AND FUTURE WORK

5.1 Research Conclusion

A simplified 2-D FEA model was employed to study the dynamic thermal-mechanical coupling phenomena within a transient period in a 4-layer stacked TSV flip-chip configuration. The failure modes resulting from the short-time scale stress waves were predicted drawing upon the established knowledge of fatigue cycling test.

The simulation results displayed in Chapter IV demonstrated that the thermal waves arisen by the $0.001^{\circ}C$ heat impulse were of very low amplitude and fast attenuation. These tiny temperature variations induced low amplitude but high frequency stress waves attenuating significantly in several nanoseconds upon power-on. Although the maximum estimated stress is a mere 15 Pa, the extremely high temporal gradient of the stress, thus the power density, was observed and related to address the reliability of the package configuration. By evaluating accumulated damage caused by high frequency oscillating stresses in the transverse direction, it was concluded that the probability of micron crack formation within the TSVs and micro-bumps was extremely high. By performing the accumulated damages induced by shear power density waves at dissimilar material interface, the probability of delamination and debonding was interpreted to be particularly high especially at locations close to the heat source.

In conclusion, the short-time scale failure mode dominated by power density waves would initiate micron cracks and flaws s at certain weak locations. When the flip-

chip TSV package reaches the steady-state operational temperature, long-time scale effects as dictated by the thermal cycling test will play the role of opening and expanding the existing cracks and lead to eventual mechanical and electric disruptions.

5.2 Contribution and Future Work

As the need for high clock speed microelectronic products increase, flip-chip packaging technology has progressed from 2-D to 3-D chip-stacking with dramatically improved circuit capacity and quality of signal communication. However, with the computational results discussed in Chapter IV, the 3-D TSV-embedded flip-chip packages have numerous structural weaknesses when subjected to high thermal transient and large spatial gradients hit. As mentioned in Chapter I, Ref. 13 demonstrated that short-time scale effects initiated defects within the solder ball grid array (BGA). Certain sizes of crack within the BGA will result and lead to package failure. Similar failure modes can be expected in 3-D flip-chip packages as well. In contrast to the 2-D case, 3-D flip-chip packages are found to be more sensitive to the impact of short-time scale effects. The reasons are of two-fold. First, 3-D flip-chip packages adopt much more interconnects, thus rendering higher probability of micron cracks initiation. Furthermore, due to the reduced component size, cracks in 3-D flip-chip packages might be easily opened to the critical size that affect signal relay when long time scale effects are involved. Since interconnects are the integral parts of the logic circuits, electrical disruption occurring in a single component is able to cause logic error and break down the whole package. Thus, the use of large amounts of TSVs and micro-bumps makes 3-

D flip-chip packages more vulnerable than 2-D's. Second, the chip-stacking structure increases the dissimilar material interfaces that are susceptible to shearing effect. As seen in Chapter IV, defects at bonding interfaces occurred rapidly, indicating that the 3-D flip-chip packages could suffer serious interfacial disconnection when operation temperature is reached. In summary, 3-D flip-chip packages inherently give rise to more reliability concerns.

Despite the reliability concern attributable to short-time scale effects, the potential of 3-D flip-chip packages in realizing improved circuit density and performance and thus low fabrication cost is being vigorously explored in semiconductor industry. Therefore, to improve packaging reliability by negating or minimizing short-time scale effects should dominate the future design of 3-D flip-chip packages. Drawing from the knowledge established and conclusion made, the followings are provided to help achieve better packaging reliability.

- Since the high frequency stress wave is the primary parameter attributed to high potential for micron crack formation, a substitute material for underfill that can quickly respond to high oscillation frequency and attenuate it to several orders of magnitude lower in magnitude will help reduce the impact from the short-time scale effects.
- Investigate long-time scale effect associated with the thermal cycling test on the weak points demonstrated in Chapter IV and optimize the dimensions of TSVs and micro-bumps, to minimize the long-time scale failure, i.e., electric disruption.
- Optimize circuit design in TSV flip-chip packages to encourage destructive

interference of the short-time scale stress waves, thus reducing the short-time scale effects.

- Review and evaluate all constituent materials for TSV packages for their integral performance against both the short time scale and long time scale effects, with the objective of identifying substitute interconnect materials that are effective in discouraging stress wave propagation.

In spite of the list above, there are still several issues to be addressed. To more thoroughly understand the short-time scale effects in the TSV flip-chip package, a comprehensive 3-D FEM model is required. Simplification of silicon material from being anisotropic to isotropic and unavailability of material S-N curves for shear loading necessarily rendered the computational results qualitative. A study of 3-D coupled electrical-thermal-mechanical phenomena induced by multiple joule heating should provide a deeper insight into the short-time scale effects within the 3-D TSV flip-chip package. However, a comprehensive 3-D FEM analysis is not probable if not entirely impossible nowadays due to the limitation on available memory and the support from present computational hardware. In summary, results obtained in this research provided explanations for the probable early failure modes in the TSV flip-chip package. Suggestions made drawing from the results should prove viable for the improvement of TSV packaging reliability.

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