

**INTEGRATION OF MICRO PATTERNING TECHNIQUES INTO VOLATILE
FUNCTIONAL MATERIALS AND ADVANCED DEVICES**

A Dissertation

by

JUNG MOO HONG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jun Zou
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	Hong Liang
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Major Subject: Electrical Engineering

ABSTRACT

Integration of Micro Patterning Techniques into Volatile Functional Materials and

Advanced Devices. (May 2009)

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Chair of Advisory Committee: Dr. Jun Zou

Novel micro patterning techniques have been developed for the patterning of volatile functional materials which cannot be conducted by conventional photolithography. First, in order to create micro patterns of volatile materials (such as bio-molecules and organic materials), micro-contact printing and shadow mask methods are investigated. A novel micro-contact printing technique was developed to generate micro patterns of volatile materials with variable size and density. A PDMS (Polydimethylsiloxane) stamp with 2-dimensional pyramidal tip arrays has been fabricated by anisotropic silicon etching and PDMS molding. The variable size of patterns was achieved by different external pressures on the PDMS stamp. A novel inking process was developed to enhance the uniformity and repeatability in micro-contact printing. The variable density of patterns could be obtained by alignment using x-y transitional stage and multiple stamping with a z-directional moving part.

Second, for direct patterning of small molecule organic materials (e.g. pentacene), a novel shadow mask method has been developed with a simple and accurate alignment system. To make accurate dimensions of patterning windows, a silicon wafer was used

for the shadow mask since a conventional semiconductor process gives a great advantage for accurate and repeatable fabrication processes. A sphere ball alignment system was developed for the accurate alignment between the shadow mask and the silicon substrate. In this alignment system, four matching pyramidal cavities were fabricated on each side of the shadow mask and silicon wafer substrate using an anisotropic silicon bulk etching. By placing four steel spheres in between the matching cavities, the self-alignment system could be demonstrated with 2-3 μ m alignment accuracy in x-y directions. For OTFT (Organic thin film transistor) application, an organic semiconducting layer was directly deposited and patterned on the substrate using the developed shadow mask method.

On the other hand, novel embedding techniques were developed for enabling conventional semiconductor processes including photolithography to be applied on the small substrate. The polymer embedding method was developed to provide an extended processing area as well as easy handling of the small substrate. As an application, post CMOS (Complementary metal–oxide–semiconductor) integration of a relatively large microstructure which might be even larger than the substrate was demonstrated on a VCO (Voltage-controlled oscillator) chip. In addition, micro patterning on the optical fiber was demonstrated by using a silicon wafer holder designed to surround and hold the optical fiber. The micro Fresnel lens could be successfully patterned and integrated on the optical fiber end.

To my parents

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1. INTRODUCTION

Microfabrication, the generation of small-scale structures, is essential to much of modern science and technology [1-3]. Micro patterning is one of the most important fabrication steps in the micro devices to determine the critical dimension of desired patterns [4-6]. So far, several micro patterning techniques have been developed for various types of applications. Although photolithography is the most common micro-patterning technique and may be superior to other patterning techniques in general, it still has several disadvantages and limitations for certain applications.

First of all, the photolithography is an expensive and complex process since it is based on indirect patterning. In most case, the final patterns of the material (metal, dielectric, semiconductor, etc...) should be transferred from the photoresist. Therefore, it requires several process steps such as application of photoresist, exposure under UV light, development of resist, evaporation of film materials, wet/dry etching, and lift-off. Second, it cannot be used with a wide range of materials, especially when complex organic or biological functional groups are involved because the chemical and physical processes involved in photolithography could damage or contaminate volatile materials. Third, the surface of substrate should be flat in photolithography since the gap between the photomask and substrate causes diffraction of UV light, and thus non-uniform and lower resolution patterning.

This dissertation follows the style of Journal of Micromechanics and Microengineering.

In addition, handling and processing a small substrate are very difficult in conventional photolithography process. The spin coating of resist involved in photolithography cause the problematic “edge bead” which limits the resolution when applied on a small substrate. Alternatively, non-photolithographic micro patterning methods, which would complement the photolithography, such as micro-contact printing, shadow mask lithography (stencil lithography), nanoimprint lithography (NIL), and dip-pen nanolithography (DPN) have been developed and demonstrated [7-10]. These techniques would ideally circumvent the limitations of photolithography, which are applicable to three dimensional structures, inexpensive, experimentally convenient, and compatible with a wide range of materials and surface chemistries.

Among these non-photolithographic patterning techniques, micro-contact printing is superior to other methods with respect to compatibility with a wide range of materials and surface chemistries. It uses the relief pattern on the surface of a PDMS stamp to form patterns of self-assembled monolayers (SAMs) on substrates by conformal contact. Micro-contact printing differs from other printing methods in the use of self-assembly to form micro-patterns and microstructures of various materials. The contact printing also benefits from the low cost and fast process which consists of several essential steps [7]: (1) replication of master structures to the elastomeric stamp; (2) loading the elastomeric stamp with inking materials (alkanethiols or other surfactant-like molecules) and (3) forming a conformal contact with a solid substrate. During the contact time with the solid surface, the “ink” reacts with the surface, and a monolayer of molecules is transferred from the elastomeric stamp.

Shadow mask lithography (also called stencil lithography) is an emerging parallel, resistless, micro- and nano-patterning technique based on the deposition of material through apertures in a shadow mask onto a substrate [11]. Shadow mask lithography can greatly circumvent the damage or contamination which is especially important when volatile materials (e.g. organic or biological materials) are involved since it does not require resists, high-temperature processing, or chemical solvents. In addition, the shadow mask lithography is capable of patterning on top of free standing structures or three-dimensional topographies when the shadow mask and substrate are separated by a gap. Main challenges in current shadow mask technologies are the fine alignment and the mask-substrate gap control as well as the resolution for a correct pattern transfer from shadow mask to substrate. The characteristics of several micro and nano-patterning techniques are compared in Table 1 (modified from [7]).

On the other hand, several embedding methods have been introduced for the integration of microstructures into the small chip substrate [12-14]. In conventional photolithography, a residual resist remains on the edge of a substrate after resist spin-coating process, which is called “edge-bead”. Although the “edge bead” can be removed by appropriate treatment (e.g. cotton swab), this greatly diminishes a possible processing area for the small substrate. An embedding system can effectively avoid this problem by extending processing area of the substrate, and thus, makes it possible to integrate complex MEMS (microelectromechanical system) components which may be even larger than the original substrate. In addition, it can be used for integration of microstructures onto the tip of fiber in micro optic application [15].

Table 1. Comparison among photolithography, micro-contact printing, and shadow mask lithography.

	Photolithography	Micro-contact Printing	Shadow Mask Lithography
Definition of patterns	Rigid photomask (patterned Cr supported on a quartz plate)	Elastomeric stamp or mold (a PDMS block patterned with relief features)	Shadow Mask (based on silicon wafer)
Materials that can be patterned directly	Photoresist (polymers with photosensitive additives) SAMs on Au and SiO ₂	SAMs on Au, Ag, Cu, GaAs, Al, Pd, and SiO ₂ Colloidal materials Organic and inorganic Polymer Biological molecules	Any kinds of materials that can be evaporated (e.g. Au, Ag, Cu, GaAs, Al, Pd, SiO ₂ ,)
Surfaces and structures that can be patterned	2-D structures Planar surfaces	Both 2-D and 3-D structures Both planar and nonplanar surfaces	Both 2-D and 3-D structures Both planar and nonplanar surfaces
Current limits of resolution (Minimum feature size)	< 50nm	< 50nm [16]	< 50nm [17]
Other advantages	More reliable process High accuracy of alignment	Low cost and fast process Variable size of patterns	Available with fragile or free standing structures No contamination

In this study, micro patterning techniques such as micro-contact printing and shadow mask lithography have been researched for the direct patterning of volatile functional materials (e.g. biological, organic materials). In addition, the novel embedding techniques are developed for integrating conventional patterning technique into advanced devices such as the CMOS VCO chip and the optical fiber.

In section 2, a flexible and versatile micro-contact printing process using a micromachined elastomeric PDMS (Poly-dimethylsiloxane) stamp with two-dimensional arrays of pyramidal tips will be introduced. Two-dimensional arrays of dot patterns with different dot size (from sub-micron to a few microns) and density can be readily printed with a single stamp.

In section 3, a shadow mask technique with simple and accurate self-alignment system is designed and demonstrated for direct patterning of volatile materials. As an application, the shadow mask method is successfully integrated into the fabrication of OTFTs (Organic thin film transistors), and the electrical properties of the OTFTs are characterized.

In section 4, novel embedding techniques will be introduced for enabling conventional photolithography to be used with a small substrate. First, the polymer embedding technique is demonstrated for efficient post-CMOS integration of a high Q vertical ring inductor onto a $2 \times 2 \mu\text{m}^2$ CMOS VCO chip. The performance of the vertical inductor was simulated numerically and experimentally characterized. In addition, silicon chip embedding technique is demonstrated for the integration of micro optical lens onto the tip of fiber.

2. MICRO-CONTACT PRINTING WITH VARIABLE DOT SIZE AND DENSITY*

2.1. INTRODUCTION

In many nano- and biotechnology applications, two dimensional (2D) arrays of dot chemical patterns with different dot size and density are necessary for parametric studies. For example, dot patterns of certain proteins can be used as “adhesive” for the attachment of cells and neurons on the target substrate. The shape, size and density of the dot patterns were found to significantly affect the morphology and functioning of the attached cells or neurons [18]. To generate such patterns, a commonly used method is micro-contact printing [7, 19]. Micro-contact printing utilizes an elastomer (e.g. PDMS) stamp to directly print chemical (“ink”) patterns on a substrate, providing excellent material compatibility with a wide range of chemicals or biochemicals, e.g. DNAs (deoxyribonucleic acids) and proteins [20].

* Reprinted with permission from “A micromachined elastomeric tip array for contact printing with variable dot size and density” by Jung Moo Hong, Fatih M Ozkeskin and Jun Zou, 2008. *J. Micromech. Microeng.* 18, 015003 (6pp), Copyright [2009] by IOP Publishing Ltd. (www.iop.org/journals/jmm)

2.1.1. Micro-contact Printing

Micro-contact printing is categorized into soft lithography which includes replica molding (REM), microtransfer molding (TM), micromolding in capillaries (MIMIC), and solvent-assisted micromolding (SAMIM) [7]. All these methods have the common feature of using a patterned elastomer as the stamp, mold, or mask (rather than a rigid photomask) to generate micropatterns and microstructures. Likewise, micro-contact printing uses a PDMS stamp to create micro patterns of SAMs of inks on the substrate through conformal contact. Although photolithography is a dominant technology, it is not always the best option for all applications. For example, it is an expensive technology; it is poorly suited for patterning nonplanar surfaces or three-dimensional micro patterns; and it is directly applicable only to a limited set of photosensitive materials (e.g. photoresists). The characteristic of photolithography is such that it is relatively little used for microfabrication based on materials other than photoresists; to work with other materials it is necessary to attach chromophores or add photosensitizers.

To illustrate the micro-contact printing procedure, the entire printing process of alkanethiols on gold was described in Figure 1. Micro-contact printing relies on (1, 2) replication of a patterned elastomeric stamp from a master to form an elastic stamp (3) that can be inked with a monolayer-forming ink (7) using either wet inking (4) or contact inking (5). The inked stamp is then used to print (6) a pattern that selectively protects the noble-metal substrate during the subsequent etch (8).

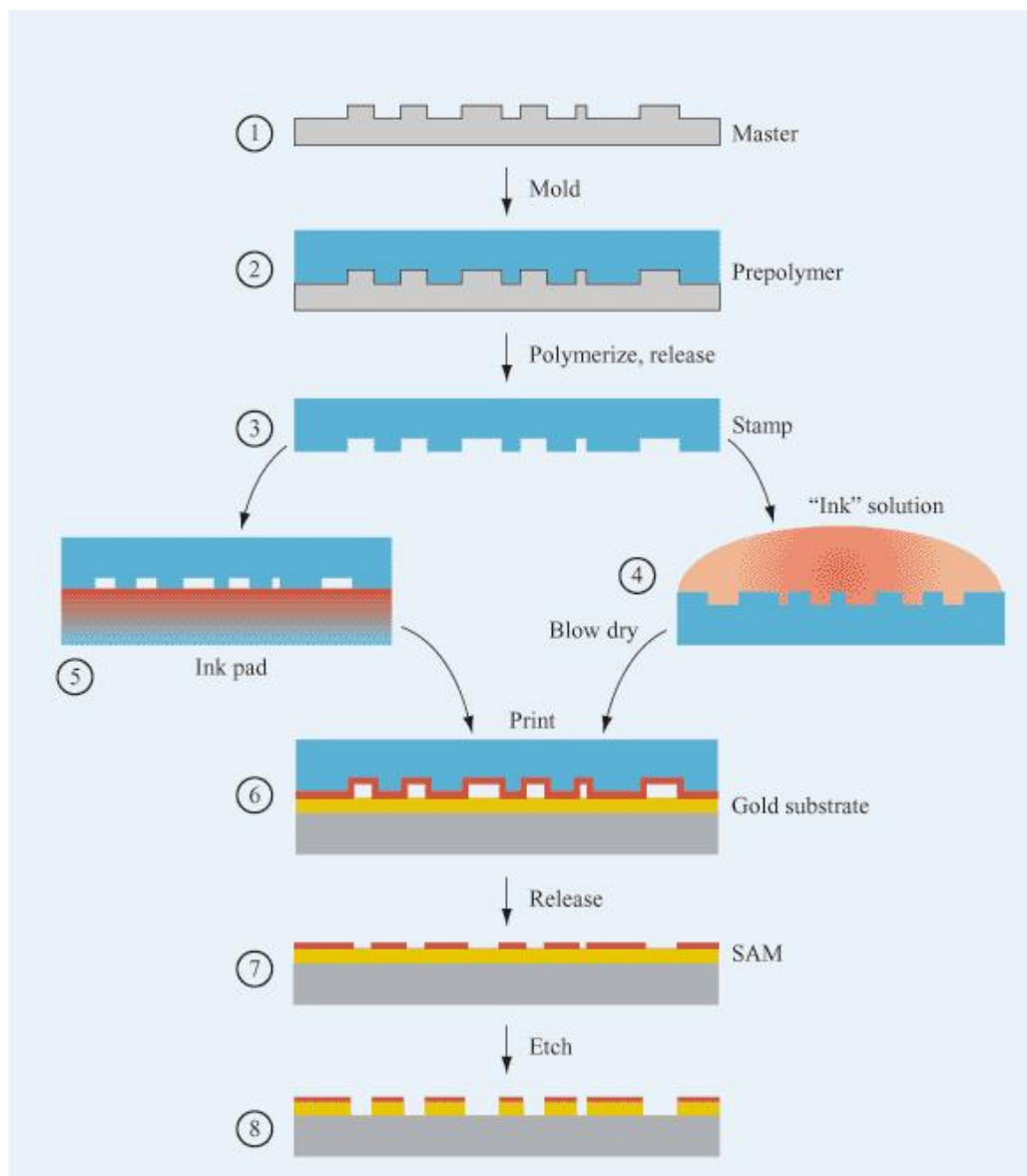


Figure 1. Schematic diagram of micro-contact printing: A prepolymer (2) covering the master (1) is cured by heat or light, and demolded to form an elastomeric stamp (3). The stamp is inked by immersion (4) or contacted with an ink pad (5), and printed onto the substrate (6), forming a SAM. The ink pattern (7) is then transferred into the substrate by a selective etch (8) [21].

2.1.2. Failure Modes in Micro-contact Printing

Stamp deformation can affect the dimensional stability of the micro-contact printing process. Since micro-contact printing uses soft elastomer as a stamp, several constraints might be imposed by stamp deformation according to the relief structures on the surface [22]. In order to explain the deformation of an elastomeric stamp, a simple stamp structure was assumed as shown in Figure 2.

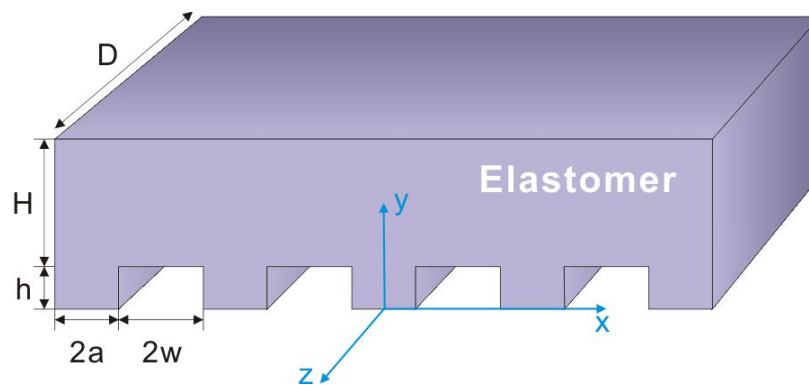


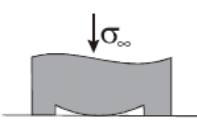
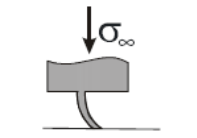
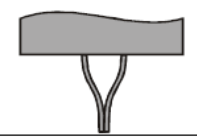
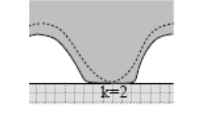
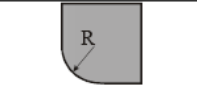
Figure 2. Schematic diagram of an elastomeric stamp.

The lateral dimension of the stamp, D is assumed to be much greater than its thickness H . In turn, H is much larger than the dimension of the surface features. The surface relief consists of identical micro size punches which are prisms with a rectangular cross section. The axes of these prisms are parallel to the z axis. The punches are equally spaced with spacing $2w$ along the x axis. Let h be the height of the

punch and $2a$ be its width. In this condition, the common failure modes which can be occurred during contact printing are summarized in Table 2.

$$D \gg H \gg h, w, a \dots\dots\dots (2.1)$$

Table 2. Summary of failure modes in micro-contact printing [22].

Description	Sketch	Result
1. Roof collapse: unwanted contact		$\frac{4\sigma_{\infty} w}{\pi E h} \left(1 + \frac{a}{w}\right) \cosh^{-1} \left[\cos \left(\frac{w\pi}{2(w+a)} \right) \right]^{-1} < 1$
2. Buckling		$\frac{-3\sigma_{\infty} h^2}{4\pi^2 E^* a^2} < \frac{1}{1+w/a}$
3. Lateral collapse		$\frac{h}{2a} \left(\frac{2\gamma_s}{3E^* a} \right)^{1/4} < \sqrt{w/a}$
4. Smooth surface asperities		$\frac{-\pi E^* h_a}{4\sigma_{\infty} a} < 1+w/a$
5. Radius of an edge rounded by surface tension		$R \sim \frac{\gamma}{2E}$

Where σ_{∞} is the remote stress which is related to the compressive load P acting on a punch and N is the number of punches per unit length in the x direction.

$$N = \frac{1}{2(a+w)} \dots\dots\dots (2.2)$$

$$P = \sigma_{\infty} / N = 2(a+w)\sigma_{\infty}$$

The elastomer is assumed to be homogeneous and isotropic with Young's modulus E and Poisson's ratio ν . Most elastomers are incompressible with $\nu \approx 0.5$ and E between 0.1 and 10 MPa. Here γ_s is the surface energy, and E^* is defined by

$$E^* = \frac{E}{1-\nu^2} \approx \frac{4}{3}E \dots\dots\dots (2.3)$$

As described above, if the aspect ratio of h to $2a$ is too low, all surfaces of the stamp can be deformed into contact with the substrate (roof collapse). On the other hand, when the aspect ratio is too large, the punches can collapse under their own weight (buckling). Also, neighboring punches may adhere to each other because of the capillary force experienced by the punches during the inking process (lateral collapse). In addition, surface tension forces can deform the sharp corners of the punches. This effect is particularly important for high resolution patterns less than 1 μm . Therefore, a stable and reliable elastomer stamp can be obtained by considering the conditions of failure modes.

2.1.3. Preliminary Work

Micro-contact printing has been conducted by standard PDMS stamps with pillar arrays and line structures. In order to prepare PDMS stamps, silicon wafer with photoresist patterns was used for a master.

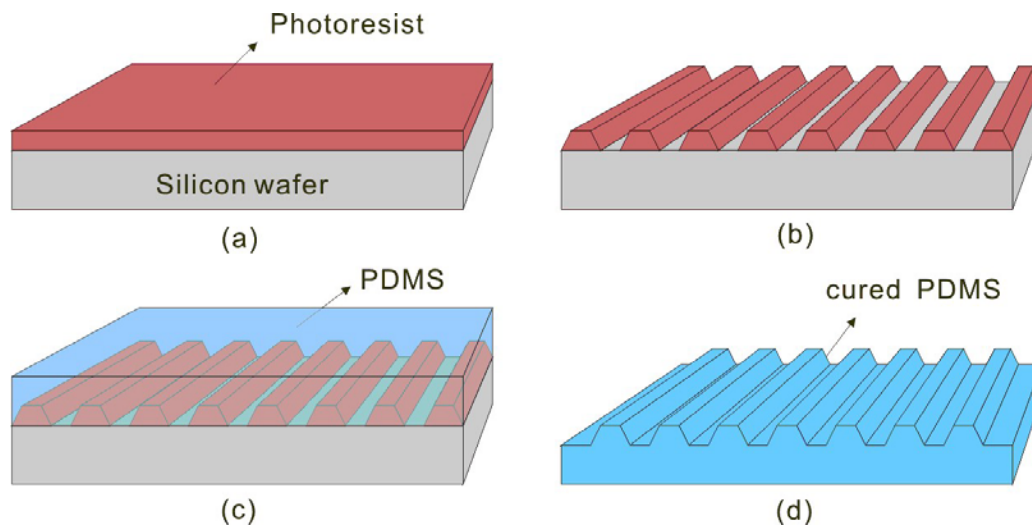


Figure 3. The fabrication steps for PDMS molding. (a) Spin coating of photoresist on the silicon wafer. (b) Photoresist was patterned by photolithography. (c) PDMS solution was poured onto the silicon wafer. (d) PDMS was cured and detached from the silicon wafer.

Figure 3 shows the fabrication process of PDMS stamp. The photoresist was first spin coated and patterned by photolithography (Figure 3a and Figure 3b). Second, the PDMS base and curing agent was mixed with the ratio of 10 to 1 uniformly, and poured on the silicon wafer with photoresist patterns (Figure 3c). Third, bubbles inside the

PDMS were removed in the vacuum jar for 1hr. Next, the entire piece was baked in the oven at 90°C for 1hr for curing the PDMS. Finally, the PDMS mold was detached from the master of silicon wafer (Figure 3d). Figure 4 shows the SEM (scanning electron microscope) images of cylindrical pillar arrays (Figure 4a and Figure 4c) and line structures (Figure 4b and Figure 4d). Here, the center to center distance between two near patterns (pillar or line structures) was designed to 10 μ m. The sidewall slopes of PDMS structures were caused by the original shape of the photoresist patterns.

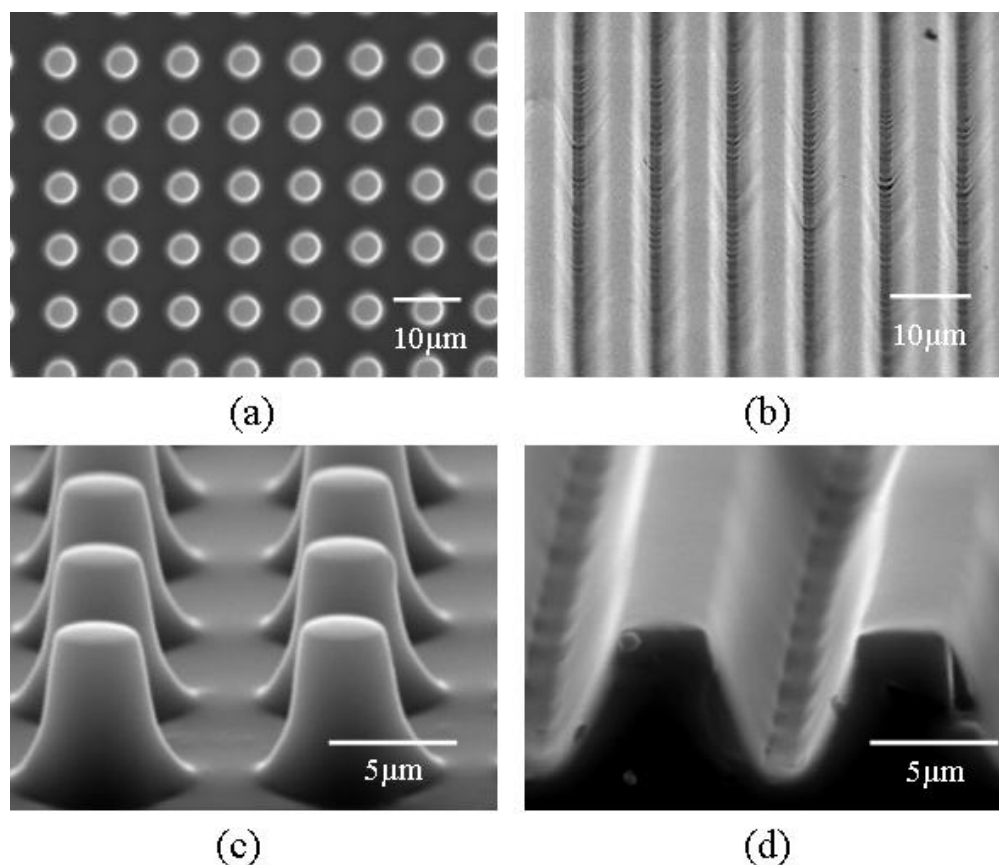


Figure 4. Scanning electron microscope images of PDMS stamps (a), (c) cylindrical pillar array. (b), (d) parallel line structures.

Micro-contact printing using fabricated PDMS stamp has been conducted with a fluorescent dye (fluorescein sodium salt; Sigma Aldrich, Saint Louis, MO), which has 460nm of excitation wavelength and 515nm of emission wavelength. The characteristics of fluorescein sodium salt have been described in APPENDIX 2 in detail. After the contact printing of fluorescent dye was performed on a slide glass substrate, the printed dye patterns were observed with a confocal microscope (Leica TCS SP5 Confocal Laser Scanning Microscopes). Figure 5 shows the fluorescent images of the printed dye patterns under the confocal microscope. The bright green area indicates the patterned fluorescent dye where the color corresponds to the emission wavelength of the dye.

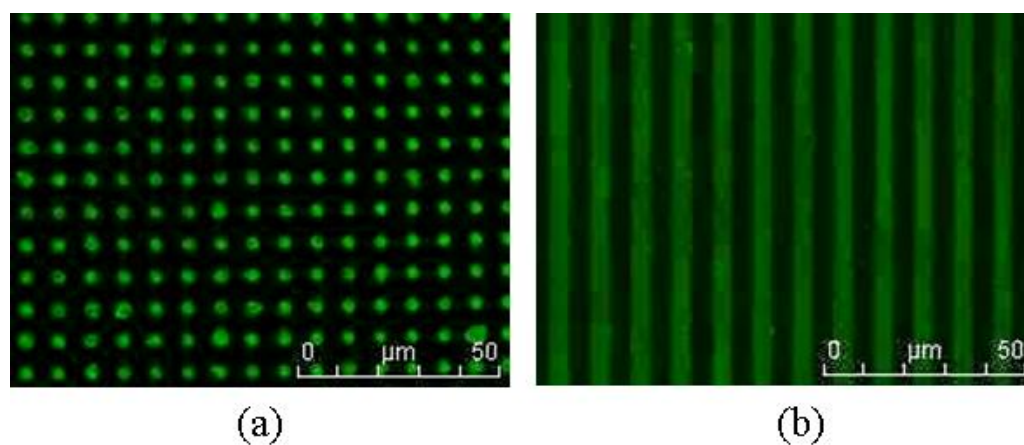


Figure 5. Confocal microscope images of printed fluorescent dye.

2.1.4. Motivation

Current micro-contact printing process generally follows a “one stamp for one pattern” paradigm. To print different patterns, multiple stamps have to be fabricated, which is not efficient and cost-effective. Also, to achieve submicron patterning, electron beam lithography is generally required to conduct stamp fabrication, which is a very expensive and slow process. During the past few years, certain effort has been made to address the above two intrinsic issues and extend the capability of micro-contact printing. To achieve different pattern size with single stamp, lateral stretching or compression, vertical compression (by applying different contact pressure) or swelling (by soaking in certain solvents) of the PDMS stamp was investigated [23]. However, these techniques can only generate small change of the dimensions and also requires special mechanical loading tool or chemicals, which would limited their application. Also, by using an AFM (atomic force microscope) testing grating as the master mold to make special V-shaped PDMS stamps, straight lines with sub-100 nm width was achieved without involving electron beam lithography process [24]. However, this method apparently lacks the generosity for contact printing of other shapes and density of patterns.

For the patterning with variable dot size and density, a novel micro-contact printing method was demonstrated using a single elastomeric stamp consisting of a 2D array of pyramidal PDMS tips. The PDMS tips were molded from a single-crystalline silicon master fabricated by photolithography and anisotropic bulk etching which are

relatively easy and low cost IC fabrication processes. Variable-dot-size printing (from sub-micron to a few microns) was achieved by applying different contact pressure to induce variable mechanical deformation and thus contact area of PDMS tips (Figure 6a). Different from the columnar structures in conventional PDMS stamps, which are subject to limited lateral deformation and mechanical instability issues [25, 26], the pyramidal shape of the PDMS tip ensures a stable mechanical deformation for a controllable wide-range pattern generation.

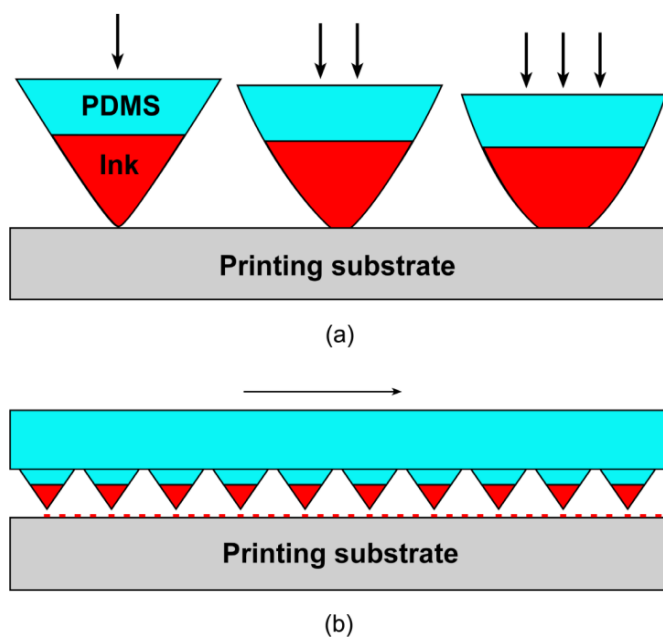


Figure 6. An illustration of micro-contact printing with pyramidal PDMS tip arrays: (a) Variable-dot-size printing by applying different pressures on the tips; (b) Variable-density printing in a “step-print” manner by using a transitional stage.

Variable-density printing was also achieved in a “step-print” manner by using a mask contact aligner which has the up-and-down stage in z-direction for stamping and

the x-y transitional stage for aligning each step stamping (Figure 6b) [27, 28]. As a result, 2D arrays of dot patterns with different dot size and density can be readily printed with a single stamp. This technique eliminates the need for the fabrication of multiple stamps (for different pattern size) and electron beam lithography (for sub-micron printing) and thus is especially useful for parametric study applications.

2.2. MODELING AND SIMULATION

2.2.1. Modeling and Simulation of PDMS Tip Deformation

To predict the contact area of the PDMS tip (thus dot size of printing) under different applied pressure, the mechanical deformation and contact pressure of the PDMS tip was simulated with finite element analysis (FEA) tool (CosmosWorks Designer© add-in under SolidWorks©). Second order solid tetrahedral mesh elements were used in the simulation, which allow proper mapping to curvilinear geometry which distributes the stress effectively. Here, the applied pressure refers to the external pressure or force exerted on the stamp to induce the mechanical deformation of PDMS tips. The contact pressure means the actual pressure existing at the contact of the deformed PDMS tips on the printing substrate.

Figure 7a and Figure 7b show the FEA model used in the simulation, illustrating the deformation and stress distribution corresponding to an applied pressure of 80 g/cm² and 320 g/cm² on a rigid contacted substrate (e.g. glass), respectively.

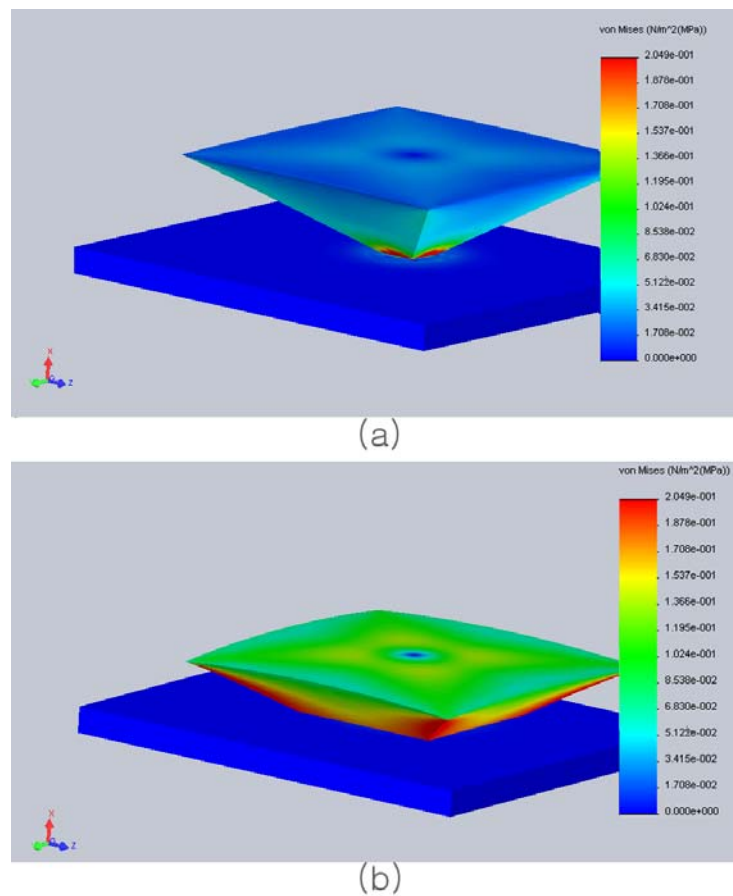


Figure 7. FEA model of a PDMS pyramidal tip showing its deformation and stress distribution under applied pressures of (a) 80 g/cm^2 and (b) 320 g/cm^2 .

To ensure the accuracy of the simulation, the actual Young's modulus of the PDMS stamp was experimentally characterized. A “compression” test of a PDMS block was conducted by putting different weights (uniformly distributed on the PDMS block) and monitoring the deformation (in thickness) with a digital indicator. An elastic

modulus of 0.67MPa was obtained, which is close to the nominal value of 0.75MPa for PDMS with a mixing ratio of 10:1 [29].

The size of the contact region and effective tip height of the PDMS tip were estimated from the simulated results (Figure 8a).

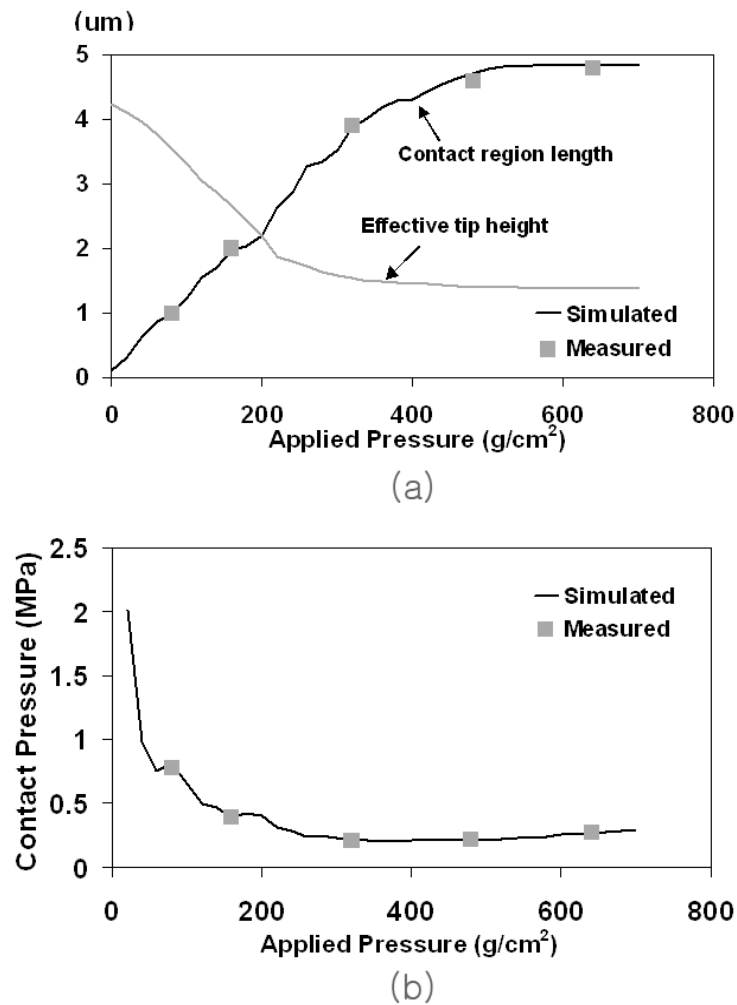


Figure 8. (a) Simulated contact region size and height of the PDMS tip under different applied pressure; (b) Estimated contact pressure of the PDMS tip under different applied pressures.

The size of the contact region first increases linearly with the applied pressure from 100 nm at zero applied pressure to 4.8 μm at 400g/cm² (39.2 kPa) and then starts to saturate due to excessive deformation under higher applied pressure. This indicates a total tuning range (theoretical) of 4800% for the dot size for PDMS pyramidal tips with a 6 \times 6 μm^2 base area.

The average contact pressure of the PDMS tip on the printing substrate was also determined based on the applied pressure and the simulated contact area (Figure 8b). It reaches its maximum (around 2MPa) at very low applied pressure when the tip remains sharp with a very small contact area. As the applied pressure increases, the tip deforms and the actual contact pressure drops quickly as a result of the increased contact area. At high applied pressure, the contact pressure increases linearly with the applied pressure due to the saturation in the deformation of the PDMS tip. The overall extremely low contact pressure makes it feasible to apply the variable dot size contact printing technique even on soft substrates (e.g. polymer).

With the built FEA model, the maximum strain of the PDMS tip under different applied pressure was also obtained. A maximum strain of 13% occurs when an excessive applied pressure of 700g/cm² (the tip deformation goes deep into saturation under this pressure). This value is still much smaller than the 20~30% yield strain of elastomer material, such as PDMS. Therefore, the tip deformation is deemed to be completely elastic and fully reversible to ensure the reproducibility of contact printing with PDMS tip array. Still, fatigue of the PDMS stamp might affect the reproducibility

under excessive usage. However, we believe this will not occur in most contact printing applications where a light to medium usage of stamps are normally encountered.

One common issue in contact printing is that PDMS stamps tend to collapse under high applied pressure especially when the aspect ratio of the stamp structures is below a certain value. For the tip array stamp, the smallest tip which can be created faithfully with conventional photolithography should have a base area of $1 \times 1 \mu\text{m}^2$ and a corresponding height of $0.7 \mu\text{m}$. Assuming the tip-to-tip spacing is $2 \mu\text{m}$ and the thickness of the stamp substrate is 2 mm , finite element simulation was conducted to study the possible stamp collapse. Under different applied pressure, the deformation of stamp substrate was negligible, compared with that of the PDMS tip. Stamp collapse doesn't happen because the dense pattern of the tips supports the substrate and distributes force uniformly. However, the possibility of stamp collapse increases with sparser tip pattern (larger tip-to-tip spacing) and thinner stamp substrate. For a given base size and height of the tips, the stamp collapse can be largely avoided when the tips are made dense enough. The thickness of the PDMS stamp substrate may also play a role in stamp collapse. For easy handling, the thickness of a PDMS stamp substrate is usually around $2 \sim 5 \text{ mm}$, which is much larger than the height of the PDMS tips (a few microns). In this case, most of the applying pressure and stamp deformation will be concentrated on the PDMS tips. Therefore, the thickness of the stamp substrate does not play a significant role in the tip-based contact printing process, as long as it is within the millimeter range. Only when the stamp substrate becomes very thin (comparable to the height of the tips), does the thickness start to affect the printing process.

2.2.2. Comparison with Columnar Pillar Structure

The deformation and contact pressure of the columnar structures in conventional PDMS stamp under different applied pressure was also simulated for comparison. A square stamp structure with the same base area ($6 \times 6 \mu\text{m}^2$) and height ($4.24 \mu\text{m}$) as those of the pyramidal tip was used in the simulation. As shown in Figure 9, the stamp structure was assumed to be pressed onto a rigid substrate with an applied pressure of 80 g/cm^2 and 320 g/cm^2 , respectively.

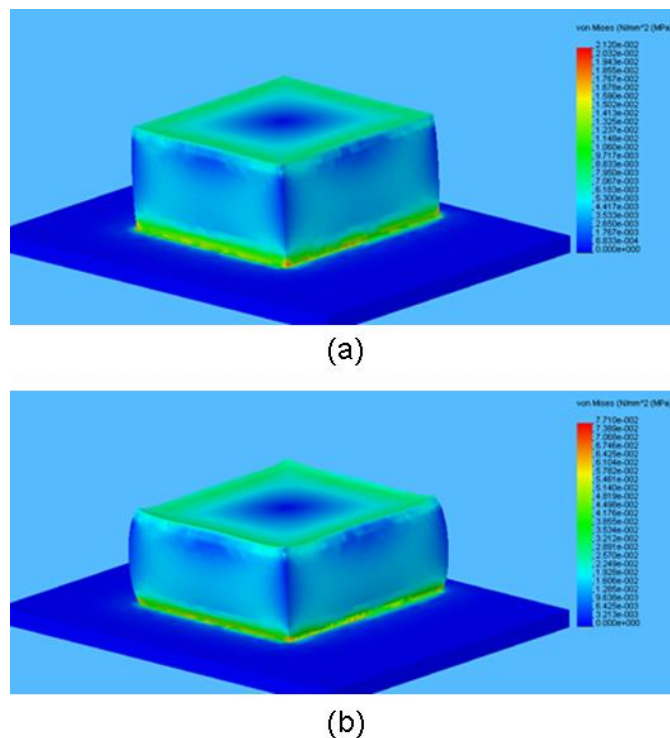


Figure 9. FEA model of a PDMS square pillar showing its deformation and stress distribution under applied pressures of (a) 80 g/cm^2 and (b) 320 g/cm^2 .

The size of the contact region and the effective height of the stamp structure were estimated from the simulated results (Figure 10a). It increases almost linearly with the applied pressure from 6 μm at zero applied pressure to 6.7 μm at 700 g/cm^2 (68.6 kPa), which indicates a total tuning range of only 11.6% for the dot size.

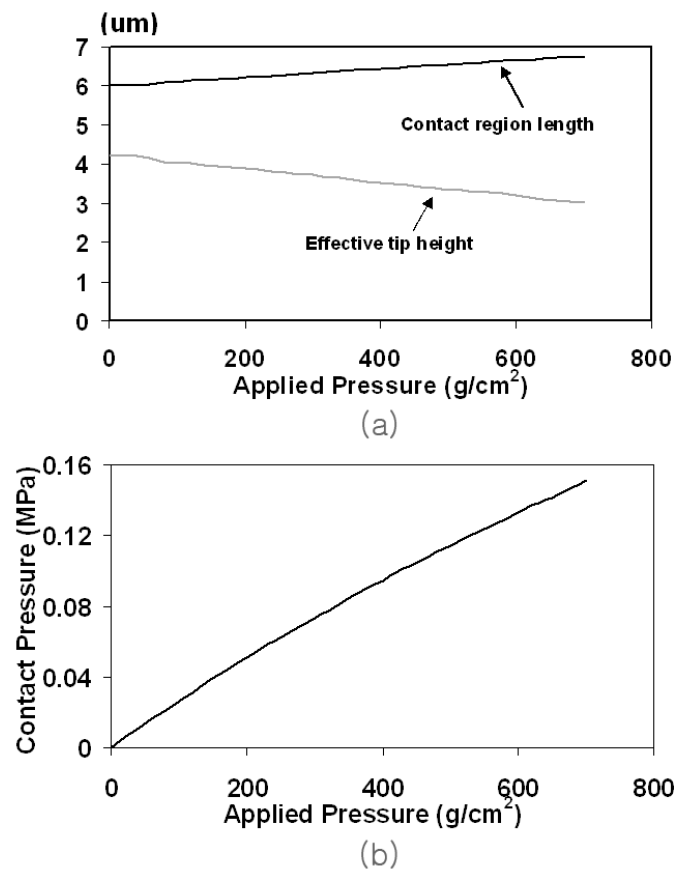


Figure 10. (a) Simulated contact region size and height of the PDMS square stamp under different applied pressures; (b) Estimated contact pressure of the PDMS square stamp under different applied pressures.

This result shows that conventional PDMS stamp structure does not facilitate the lateral deformation even under high applied pressure and thus is not effective for

achieving variable pixel size. The average contact pressure of the PDMS tip on the printing substrate was also determined based on the applied pressure and the simulated contact area (Figure 10b). Since the contact area increases very slowly with the applied pressure, the contact pressure assumes almost linear relationship with the applied pressure.

2.3. FABRICATION

2.3.1. Fabrication of Silicon Master

The design and fabrication process of the PDMS tip array is illustrated in Figure 11. To form the PDMS tip array single crystalline silicon master mold was first fabricated. The silicon wafer was first cleaned with piranha solution (Sulfuric acid: Hydrogen peroxide= 3:1) and immersed into buffered oxide etchant to remove the initial oxide layer. For the silicon etch mask, 1000Å of oxide layer was grown by dry oxidation at 1100°C for 1hr. The grown silicon oxide layer was patterned for making square opening arrays by photolithography and buffered oxide etching. The four sides of the square windows were aligned to the $\langle 110 \rangle$ crystal direction of silicon. In order to make pyramidal cavities, the $\{100\}$ silicon wafer was anisotropically etched by a solution of a concentration of 30% KOH by weight. The KOH etching was performed in the covered petri-dish (to maintain the concentration of KOH) on a magnetic stirring hotplate at 80°C, which terminated by itself when the $\{111\}$ crystal surfaces was

exposed [30]. Thus, a silicon mold consisting of a 2D array of uniform pyramidal cavities with atomic apex sharpness (bounded by the four $\{111\}$ crystal surfaces) can be readily obtained (Figure 11a). This fabrication of the silicon master mold does not require any complex process or special equipment, which results in a simple, straightforward and low cost fabrication process.

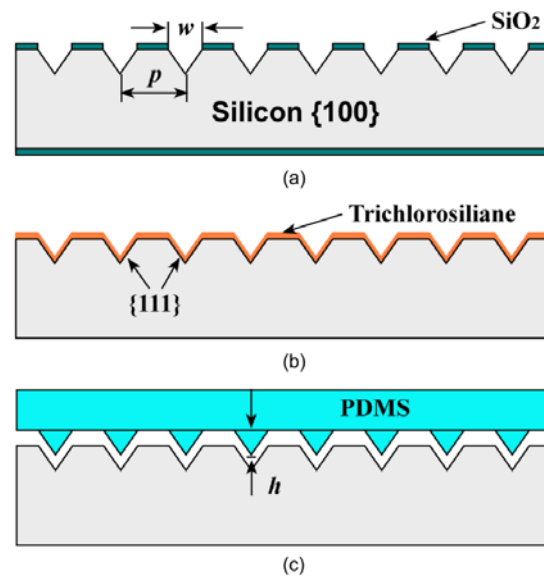


Figure 11. An illustration of the design and fabrication process of the pyramidal PDMS tip array (a) oxide layer patterning followed by anisotropic silicon etching, (b) anti-adhesive surfactant coating, (c) curing PDMS and detaching it from the substrate.

2.3.2. Fabrication of PDMS Stamp

To make the stamp, PDMS solution was prepared from a mixture of Sylgard® 184 silicon elastomer base and silicon elastomer curing agent (from Dow Corning) with a ratio of 10:1. To ensure easy detachment of PDMS stamp from the silicon mold after

PDMS curing, Tridecafluoro-1,1,2,2,-tetrahydrocetyl-1-trichlorsilane (from Sigma-Aldrich) was coated on the silicon mold as an anti-sticking surfactant (Figure 11b). Ideally, only a mono layer of the surfactant is needed and thick coating of the surfactant can cover the end-point of pyramidal cavities and thus reduce the sharpness of the molded PDMS tips. In order to obtain a thin layer in the etched cavities, vapor coating of surfactant was conducted, instead of spin-coating. Several drops of the surfactant were placed beside the silicon mold in a vacuum jar for 10 min for the surfactant to evaporate and condense on the silicon surface. Next, the mixed PDMS solution was poured on the silicon mold and cured in the oven for 1hr at 90°C. Finally, the cured PDMS stamp was directly peeled off from the silicon master mold (Figure 11c).

Figure 12 shows the scanning electron microscopic (SEM) images of some molded PDMS tips. The radius of curvature of the PDMS tip is estimated to be around 100 nm from the zoom-in SEM image. In the current design, a base size of $6 \times 6 \mu\text{m}^2$ and a tip-to-tip spacing of $10 \mu\text{m}$ were chosen as a balance of the tip density and height. Based on the fixed taper angle of the PDMS tip (70.5°) defined by the pyramidal cavity, the height of the PDMS tip is determined as $4.24 \mu\text{m}$. Other combination of tip base size and spacing can be also selected to suit the needs of different applications. Increasing tip base size and spacing will provide a wide tuning range of the dot size, however at the cost of dot density. On the other hand, smaller base size and spacing will result in higher dot density with smaller tuning range of the dot size.

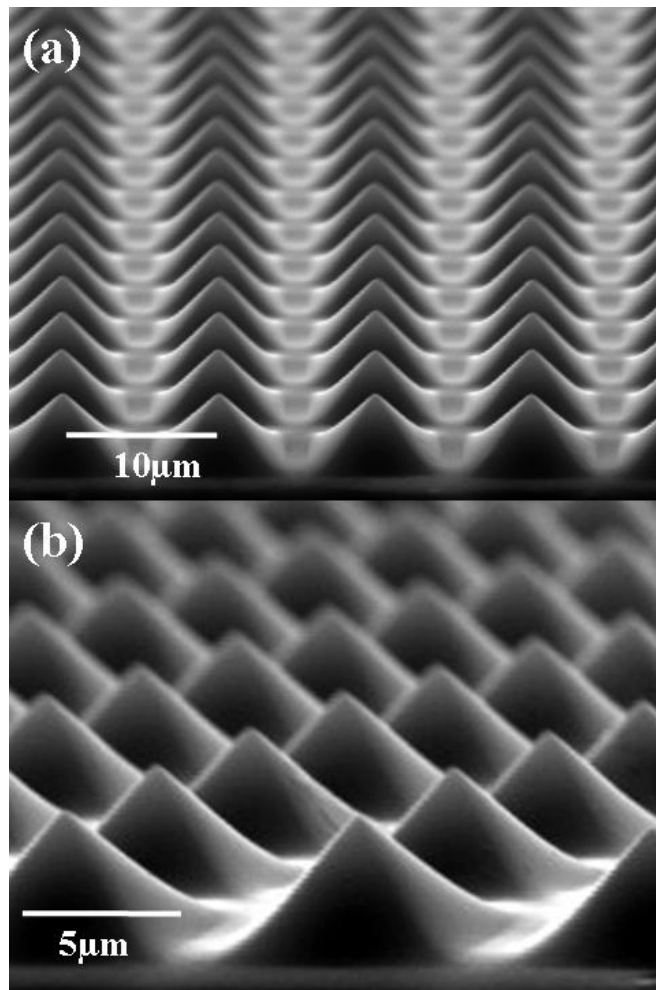


Figure 12. Scanning electron microscopic images of molded PDMS pyramid tips: (a) front view; (b) prospective view.

2.4. EXPERIMENTAL RESULTS

2.4.1. Micro-contact Printing with PDMS Stamp

To demonstrate the proposed contact printing concepts, a fluorescent dye (Rhodamine B; Sigma Aldrich, Saint Louis, MO) was used as an ink. Rhodamine B is

extensively used in biological applications and its pattern can be easily measured with fluorometer or confocal microscopes. Because of the good affinity of ethanol on PDMS surface, Rhodamine B was dissolved in ethanol with a concentration of 1 mg/ml. To ensure a uniform inking of the PDMS tips, a pre-cleaned glass slide was used as an inkpad [31, 32]. The schematic contact printing process was illustrated in Figure 13.

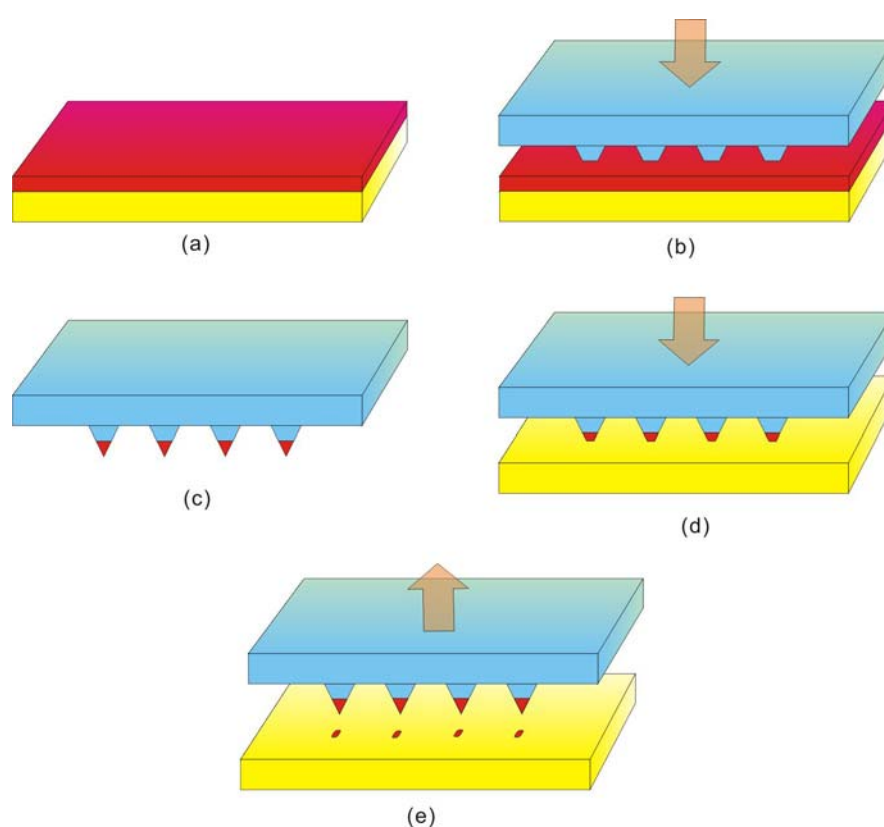


Figure 13. Micro-contact printing process using inking pad method; (a) spin-coating of fluorescent dye solution on the slide glass, (b) inking PDMS stamp, (c) inked PDMS tip array, (d) contact printing with external pressure, (e) remove the PDMS stamp from the substrate.

After spinning the Rhodamine B solution onto the glass slide (one inch square) at 2000 rpm for 15 seconds, the inking of the PDMS stamp was conducted by contacting

the stamp onto the glass slide with its own weight for 20 seconds (Figure 13a). To demonstrate variable-dot-size printing, the inked PDMS stamp was pressed onto another pre-cleaned glass slide with different applied pressure, which was controlled by putting different weights onto the PDMS stamp (Figure 13b). A contact time of 20 seconds was used for all the experiments.

Micro-contact printing of two types of fluorescent dyes (Rhodamine B and Fluorescein sodium salt) has been conducted with the inking pad method. The pressure of $100\text{g}/\text{cm}^2$ was applied on the PDMS stamp after inking the PDMS tip arrays. Figure 14 shows the printed patterns of two fluorescent dyes with high contrast and uniformity. When the inking pad process was involved as shown above, the contrast and uniformity could be greatly improved with higher repeatability.

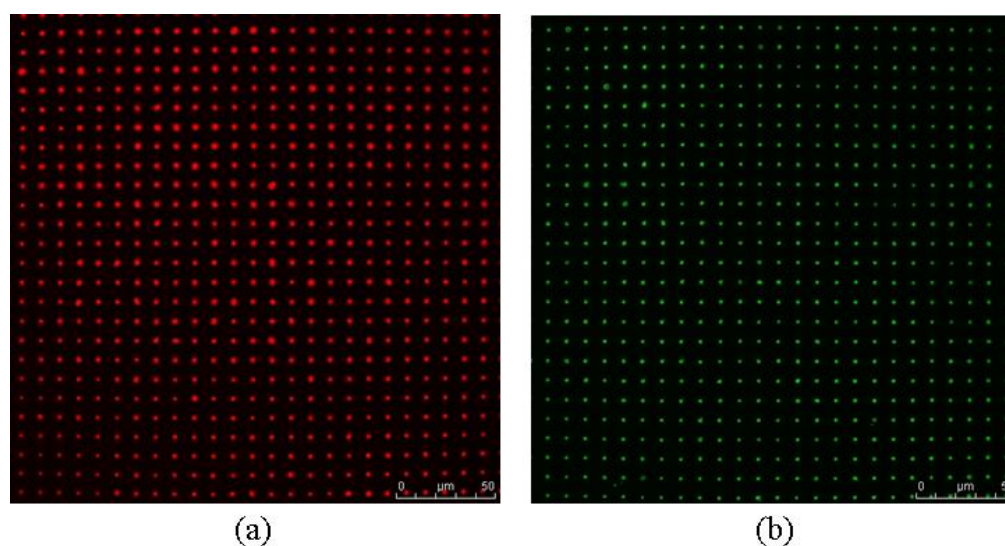


Figure 14. Micro-contact printing of fluorescent dyes using the inking pad process; (a) Rhodamine B, (b) Fluorescein sodium salt.

2.4.2. Contact Printing with Variable Dot Size

Since the PDMS is an elastomer, it can be easily deformed by external pressure. Especially the pyramidal tip array can be greatly deformed since the applying force is concentrated on the contact areas of the tip array. Therefore, the material characteristic of PDMS which is “soft” and the mechanical structure which has “smaller contact area” are considered to change the contact area, and thus the pattern size to be printed. The deformation and contact area of the PDMS tips were measured under an optical microscope. The printed Rhodamine B dot patterns were inspected under a confocal microscope (Leica[®] TCS SP5). As shown in Figure 15, the size of the (square) contact area of the PDMS tips on the glass slide is around $1\times 1\ \mu\text{m}^2$, $2\times 2\ \mu\text{m}^2$, and $4\times 4\ \mu\text{m}^2$ for an applied pressure of $80\ \text{g}/\text{cm}^2$, $160\ \text{g}/\text{cm}^2$, and $320\ \text{g}/\text{cm}^2$, respectively, which closely match the size of printed Rhodamine B patterns.

In our work, all the experiments were conducted by manually putting the stamp (and the weight) onto the printing substrate. The method doesn't offer a good control of the contact pressure. The minimum pattern size was slightly smaller than $1\times 1\ \mu\text{m}^2$, which was obtained when there was not additional weight applied on the stamp. This corresponds to a tuning range of around 400%, which is still much wider than that obtained with conventional stamp. By “putting” the PDMS tip onto a scanning probe and using an atomic force microscope to provide an accurate control of the contact force (pressure), a minimum pattern size of 80nm was achieved, which approaches the radius

curvature of the tip [33]. Therefore, when a good contact control setup is used, a minimum pattern size of 100nm could be expected using the tip array stamp, with a tip radius of curvature around 100nm. In this case, a much wider tuning range could be expected.

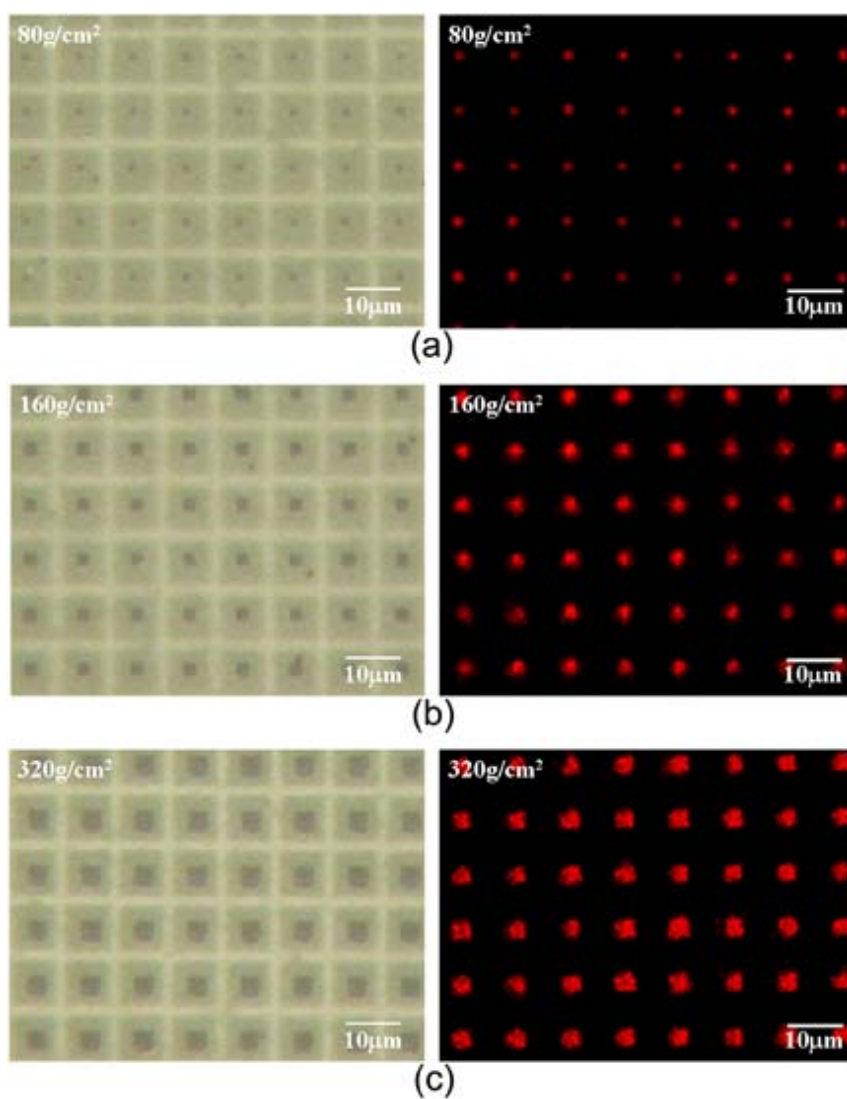


Figure 15. Optical microscopic images of deformed PDMS tips (left) and fluorescent images of printed Rhodamine B patterns (right) under different applied pressures: (a) 80g/cm²; (b) 160g/cm²; (c) 320g/cm².

By measuring the actual tip contact area under a microscope, the actual tip contact pressure can be determined. The measured tip contact area and contact pressure at different applied pressure is plotted in Figure 8 with the FEA simulated data, showing a good match between these two. This indicates the good accuracy of our FEA model and also the experimentally obtained value of the Young's modulus of PDMS. Also, to verify the excellent reliability of the tip array stamp predicted by FEA, a contact test was conducted when a tip array stamp was contacted a glass substrate with an applied pressure of $700\text{g}/\text{cm}^2$ for 100 times. The tip array stamp was inspected under an SEM before and after the tests, with no visible change of tip shape observed.

2.4.3. Contact Printing with Variable Density

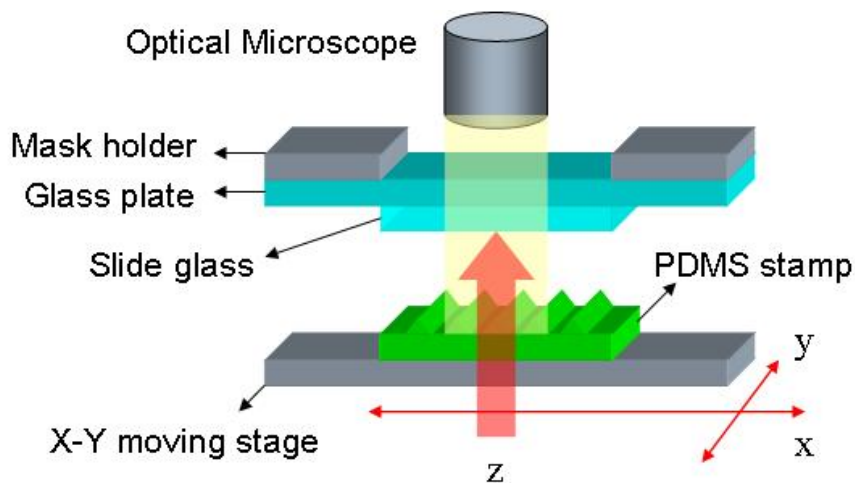


Figure 16. A schematic diagram of the multiple contact printing scheme with the x-y alignment stage and z-directional moving control.

With the PDMS tip array, variable-density contact printing of dot patterns was also demonstrated in a “step-print” manner using the x/y transitional stage of a contact mask aligner (Karl Suss[®] MJB-3). Figure 16 shows a schematic diagram of the step-printing system. The printing substrate (glass slide) was mounted on the mask chuck of the contact aligner, while the inked PDMS stamp was mounted on the wafer chuck with the tips facing up. After the PDMS stamp and the glass slide was brought into contact for the first printing, the wafer chuck is lowered to separate the PDMS stamp from the glass slide and shift to a new location for a second contact printing.

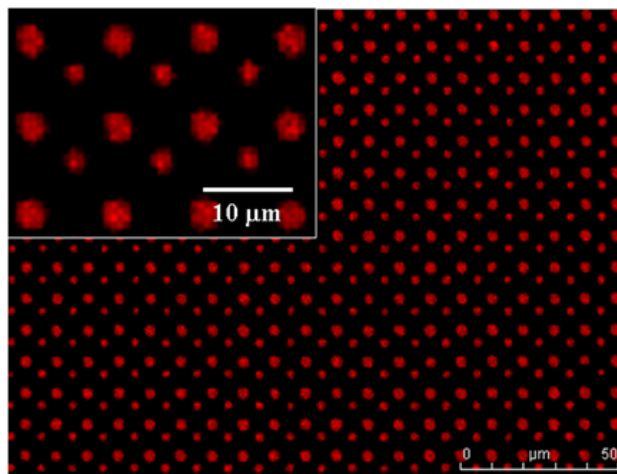


Figure 17. Fluorescent image of double printed Rhodamine B dot patterns under different contact pressures.

Figure 17 shows the printing results of Rhodamine B dot patterns created with two times of printing. Because the contact aligner does not have any contact control, the contact pressure associated in the two contact printing is inevitably different, which

causes the difference of the size of the printed patterns. It is expected that more uniform contact printing can be achieved when a better controlled pressure source is used.

2.5. CONCLUSIONS

In conclusion, a flexible and versatile micro-contact printing process using a PDMS stamp consisting of a 2D array of pyramidal tips was demonstrated. When equipped with a fine resolution x/y/z translation stage and controlled pressure source, this technique is expected to provide a simple, efficient, and low-cost method to create variable 2D arrays of dot chemical patterns for nano- and biotechnology applications. In addition, as shown in Figure 18, the micro-contact printing developed in this study enables SAMs of functional materials to be printed and patterned with variable size and density.

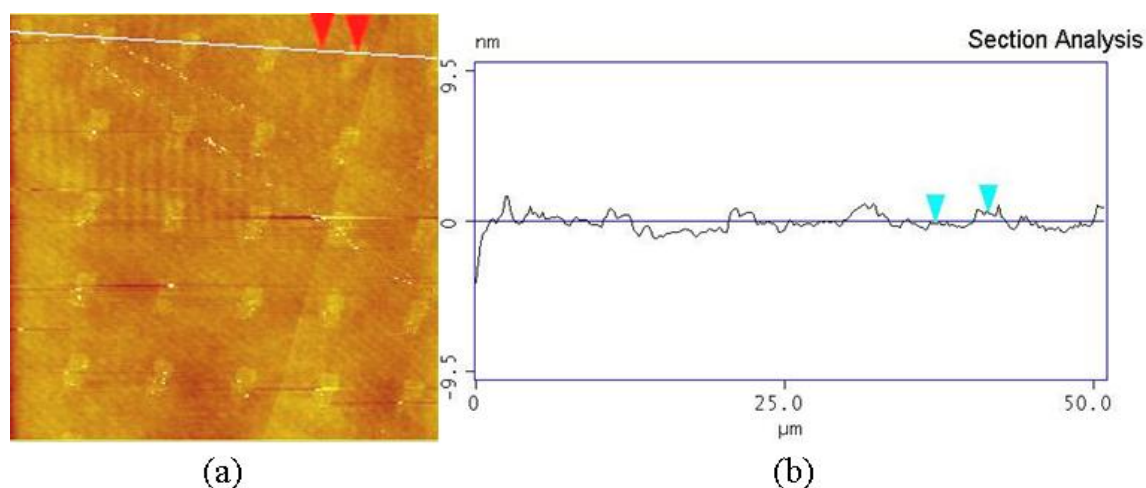


Figure 18. Atomic force microscope images of the printed fluorescent dye patterns; (a) top view of the printed patterns, (b) height profile of the patterns.

3. DIRECT PATTERNING OF VOLATILE MATERIALS USING SHADOW MASK METHOD*

3.1. INTRODUCTION

In microfabrication and micromachining, photolithography has been widely used for patterning thin-film materials for semiconductor device fabrication. However, the involvement of photoresist processing in a typical photolithography process makes it not suitable for patterning a wide range of organic materials. This is because the deposition, exposure, development and removal of photoresist would cause contamination, degradation or even damage to these materials. To address this issue, shadow masks are developed and used in vacuum deposition chambers to achieve direct material patterning without photolithography [34, 35] (Figure 19). A typical shadow mask consists of a thin flat substrate with open windows corresponding to the material patterns to be formed. After the vacuum deposition process starts, thin-film materials can be only deposited through the open windows.

* Reprinted with permission from “A novel micromachined shadow mask system with self-alignment and gap control capability” by Jung Moo Hong and Jun Zou, 2008. *J. Micromech. Microeng.* 18, 055002 (7pp), Copyright [2009] by IOP Publishing Ltd. (www.iop.org/journals/jmm)

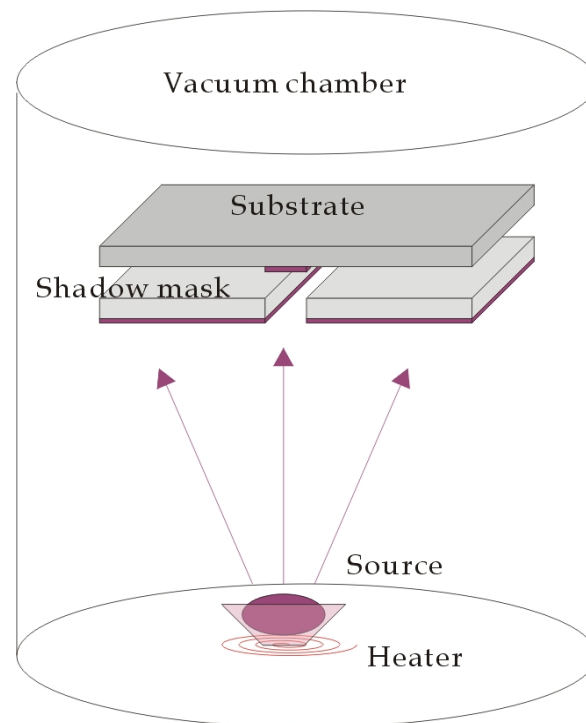


Figure 19. Schematic diagram of material deposition and patterning through a shadow mask.

Since the shadow mask technique can directly create a patterned thin-film layer in one process step, the possible material contamination, degradation and damage associated with photoresist handling can be largely avoided. This feature also makes the shadow-mask technique very useful for selective material deposition on micromachined substrates with delicate free-standing structures on the surface, such as micro cantilevers and membranes.

3.1.1. Shadow Mask Lithography (Stencil Lithography)

The shadow mask technique is a promising tool for micro- and nano-patterning of volatile functional materials. It is based on selective deposition of material through apertures in the shadow masks. The advantage of this technique is that it does not rely on photoresist processes. Although photolithography is still the main method used for creating micro- and nanostructures in thin films, it requires several process steps, for example, spin-coating of photoresist, thermal baking, mask alignment, exposure, development, evaporation of a thin film, and lift off. On the other hand, the shadow mask method can create a structured thin film in two process steps; alignment and deposition steps. The deposited structures can either be used directly, transferred into a sub-layer, combined by lift-off processes, or refined by self assembly or other growth processes.

The shadow mask method typically uses stainless steel or solid-state membranes with apertures from micro- to nano-meter range (< 100 nm). These patterns can be transferred to a substrate in a single process step, potentially in a non-contact mode. These characteristics make the shadow mask method applicable to surfaces that are either mechanically unstable free standing structures, such as cantilevers and membranes, or functionalized for organic and biological applications. Figure 20. shows a schematic process flow of the shadow mask lithography.

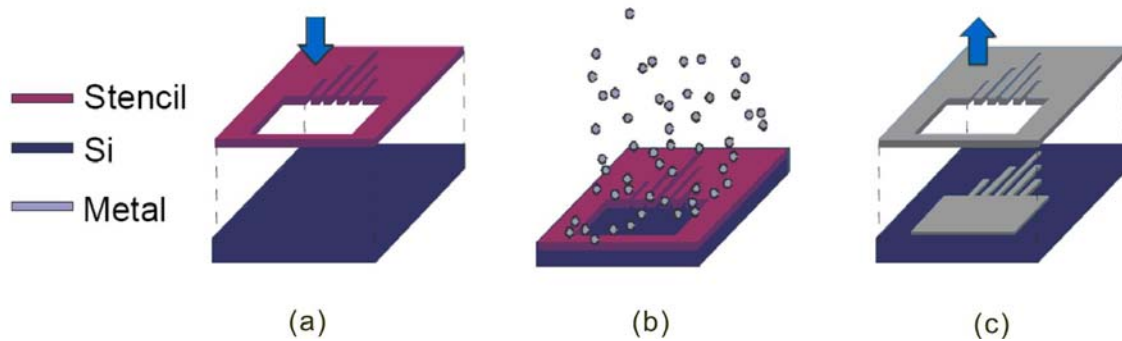


Figure 20. A schematic process flow of the shadow mask lithography; (a) placing and aligning the stencil with the substrate (b) deposition through the stencil (c) remove the stencil from the substrate.

The main advantages of stencil lithography are: (1) Clean process without involving resist, development, baking, and harmful chemicals, (2) Compatibility with pre-patterned, fragile, non-planar, functionalized, CMOS, MEMS substrates because of its non-contact process, (3) Re-usable, (4) Rapid and low-cost patterning, (5) Wide range of size features (micro and nanostructuring in a single step), (6) High flexibility of materials (metals, oxides, piezoelectrics, organic molecules, SAMs).

3.1.2. Motivation

Currently, shadow masks made of thin stainless-steel plates are most commonly used. However, their mechanical stability and resolution are generally not adequate for micron-size patterning, which limits their application mainly to the creation of large patterns (e.g. sub-millimeter). This is because the conventional machining techniques used for making the stainless-steel shadow mask are difficult to reach micron-size resolution. Also, the shadow mask will become very flexible and easy to deform when it

is thin (to facilitate its fabrication), causing distortion in the created patterns. To address the above issues, shadow masks made of silicon substrates have been investigated to benefit from the mechanical stability of silicon wafer and higher resolution provided by microfabrication and micromachining [36-39]. However, in order to use shadow masks to conduct layer-by-layer device fabrication, accurate alignment and gap control between the shadow mask and fabrication substrate will be also required, which otherwise has been a challenging issue in current shadow mask techniques. First, due to the unavailability of the optical alignment systems (similar to those used in photolithography), the alignment of shadow mask with the fabrication substrate largely has to rely on the use of mechanical fixtures, which are subject to issues such as complex alignment process, mechanical robustness, low repeatability or large alignment errors. Second, a proper mask-substrate gap is important to prevent loss of patterning fidelity (due to a large gap) and possible damage to any delicate structures (due to a hard contact caused by a small gap). Unfortunately, a straightforward and precise control of mask-substrate gap has not been obtained up to date.

In this study, a new silicon shadow mask system was reported, which is capable of simple and accurate mask-substrate alignment and gap control. The shadow mask was fabricated with photolithography and anisotropic bulk etching of {100} silicon wafer. By using steel spheres and bulk-etched pyramidal cavities as alignment structures, accurate and robust self-alignment and gap control have been achieved. As an application of the new shadow mask technique, organic thin film transistor (OTFT) have been also fabricated and tested successfully.

3.2. DESIGN OF SHADOW MASK SYSTEM

3.2.1. Design for Self-Alignment

As shown in Figure 21, the new silicon shadow mask system consists of three main components: (1) the shadow mask wafer, (2) the carrier wafer, and (3) steel spheres placed between. The shadow mask wafer has through-wafer holes (formed by either bulk etching or deep reactive ion etching (DRIE)) as open windows for pattern generation.

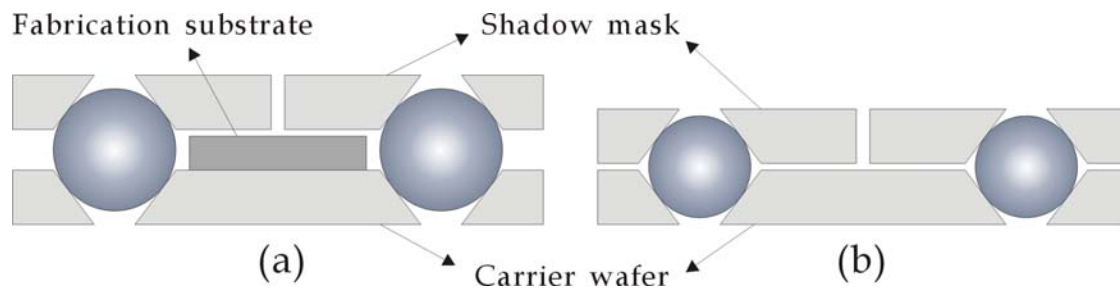


Figure 21. Schematic diagram of the new shadow mask system: (a) The fabrication substrate is fixed on the carrier wafer; and (b) the carrier wafer is directly used as the fabrication substrate.

The carrier wafer is used for mechanical support of the fabrication substrate (e.g. flexible polymer films). During material deposition, the fabrication substrate will be fixed on and thus aligned to the shadow mask through the carrier wafer (Figure 21a). If

necessary, the carrier wafer can be directly used as fabrication substrate by itself (Figure 21b). To achieve the self-alignment and gap control capability, matching pairs of pyramidal cavities are created in both the shadow mask wafer and the carrier wafer to fit with the steel spheres.

It is well known that wet bulk etching of $\{100\}$ silicon with a square opening will create a symmetrical pyramidal cavity bound by four sloped sidewalls ($\{111\}$ crystal planes), which form a fixed 54.7° angle with the silicon substrate surface ($\{100\}$ plane). The symmetric axis of the pyramidal cavity passes through the apex of the cavity and is perpendicular to the substrate surface. When a sphere is placed in a bulk-etched pyramidal cavity and their surface are in full contact, the center of the sphere will be automatically aligned onto the symmetric axis of the cavity.

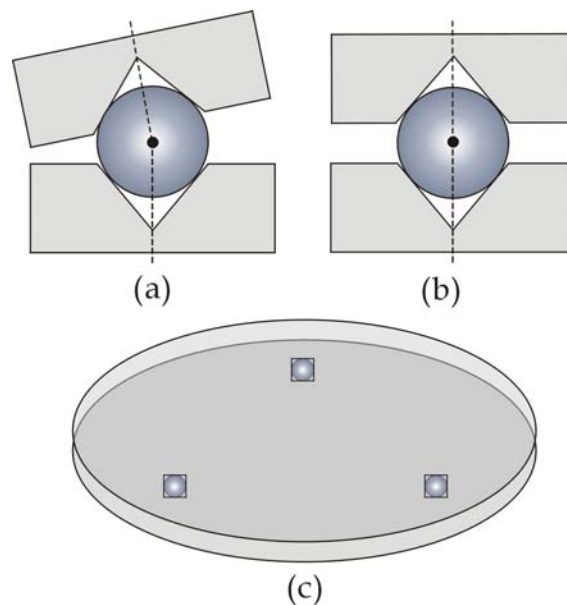


Figure 22. Illustration of self-alignment of two silicon substrates using two bulk etched cavities and a steel sphere.

As a result, when two of such silicon substrates are in contact with the same sphere, their symmetric axes will both pass through the center of the sphere, even though the size of the two pyramidal cavities would be different (Figure 22a). When the two silicon substrates are in parallel, the symmetric axes of the two pyramidal cavities will merge into one (Figure 22b). By using three identical groups of alignment structures (two cavities and one sphere) to ensure the parallel position of the two substrates, accurate self-alignment of the two substrates can be readily achieved (Figure 22c). In practice, the actual alignment accuracy will be mainly affected by the irregularity and non-uniformity of the steel spheres and pyramidal alignment cavities, which otherwise can be well controlled with fabrication of the cavities. By involving microfabrication techniques of the silicon substrate, high alignment accuracy of the two silicon substrates (e.g. shadow mask wafer and carrier wafer) can be expected.

3.2.2. Design for Gap Control

The self-alignment structure (two cavities and one sphere) can also facilitate the gap control between the shadow mask and the device substrate. As shown in Figure 23, the gap (g) between the shadow mask and the fabrication substrate can be determined as

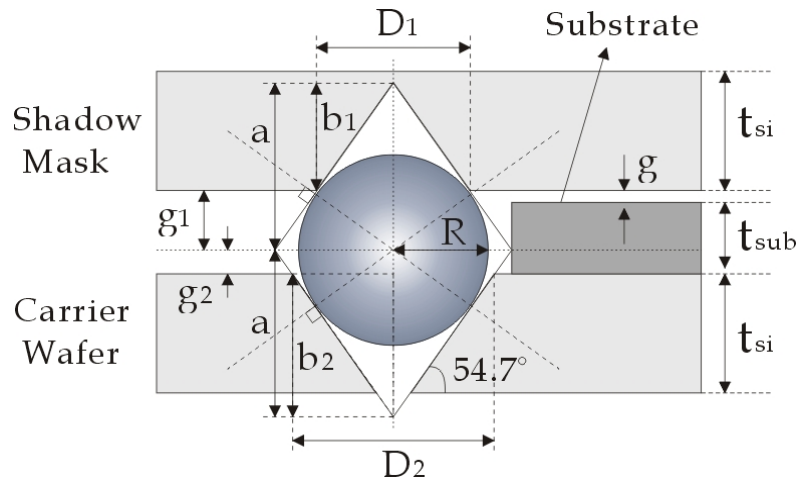


Figure 23. Design parameters for mask-substrate gap control.

$$g_{1,2} = a - b_{1,2} = \frac{R}{\cos 54.7^\circ} - \frac{D_{1,2}}{2} \tan 54.7^\circ \quad \dots\dots\dots (3.1)$$

$$\begin{aligned} g &= g_1 + g_2 - t_{sub} \\ &= \frac{2R}{\cos 54.7^\circ} - \frac{D_1 + D_2}{2} \cdot \tan 54.7^\circ - t_{sub} \quad \dots\dots\dots (3.2) \end{aligned}$$

Where R is the radius of the steel sphere, and t_{sub} is the thickness of the fabrication substrate. D_1 and D_2 are the base sizes of the two matching pyramidal cavities in the shadow mask and carrier wafer, respectively. Once the shadow mask and carrier wafer are fabricated, the mask-substrate gap (g) will only depend on the radius of the sphere (R), the base size of two pyramidal cavities for self-alignment (D_1 and D_2), and the thickness of the fabrication substrate (t_{sub}). As a result, even for fabrication substrates

with different thickness, a desirable mask-substrate gap can be readily obtained by using steel spheres and pyramidal cavities with suitable size.

3.3. FABRICATION OF SHADOW MASK AND CARRIER WAFER

To realize self-alignment and gap control, pyramidal cavities are needed in both the shadow mask and carrier wafer. In addition, through-wafer openings are also required in the shadow mask wafer for material deposition and patterning. The silicon bulk etching of double-sided (100) silicon wafer and single-sided (100) silicon wafer was conducted to fabricate the shadow mask and carrier wafer, respectively. The fabrication process flow is shown in Figure 24.

First, a silicon oxide layer was thermally grown on the silicon wafers and square windows were patterned by photolithography and buffered oxide etching (Figure 24a). Next, silicon bulk etching was conducted to form the pyramidal alignment cavities. A commercial preferential etchant (PSE-300 from Transene Company, MA) was used, which is ethylenediamine-based preferential silicon etchant for <100> crystal orientation. The PSE-300 has a moderate etch rate of silicon (25 $\mu\text{m/hr}$ at 100°C) while it makes negligible attack on SiO_2 (Figure 24b). The alignment cavities on the shadow mask and the carrier wafer form mirror images, so that they can align with each other. After the pyramidal alignment cavities have been fabricated, the same process steps were conducted on the backside of shadow mask wafer to form through-wafer open windows for material deposition and patterning (Figure 24c and Figure 24d). However, the sloped

side walls inevitably limit the density of created patterns. To address this issue, deep reactive ion etching (DRIE) of silicon could be used as an alternative to create more dense patterns (Figure 24d'). The fabrication of the shadow mask and carrier wafer does not require any complex process or special equipment, which results in a simple, straightforward and low-cost fabrication process (Figure 24f).

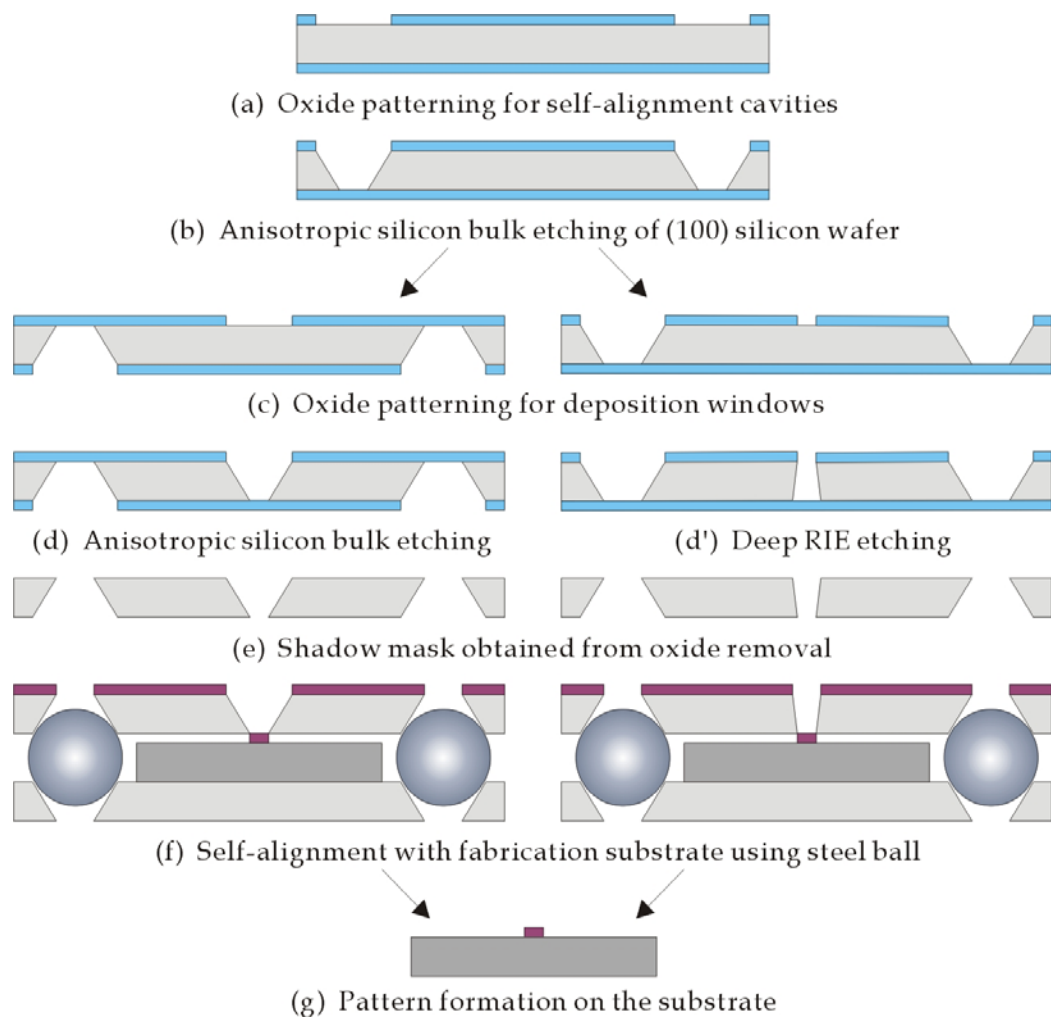


Figure 24. Schematic diagram of the fabrication process and application of the shadow mask system.

Figure 25a shows a self-aligned shadow mask (seen from the front-side) with a carrier wafer using four steel spheres (purchased from McMaster-Carr Supply Company). The steel spheres were easily placed in the four pyramidal cavities with tweezers. Although theoretically three spheres should be adequate for the alignment, the use of one additional sphere offers more mechanical support to the shadow mask wafer, thus resulting in a more stable and robust deposition process.

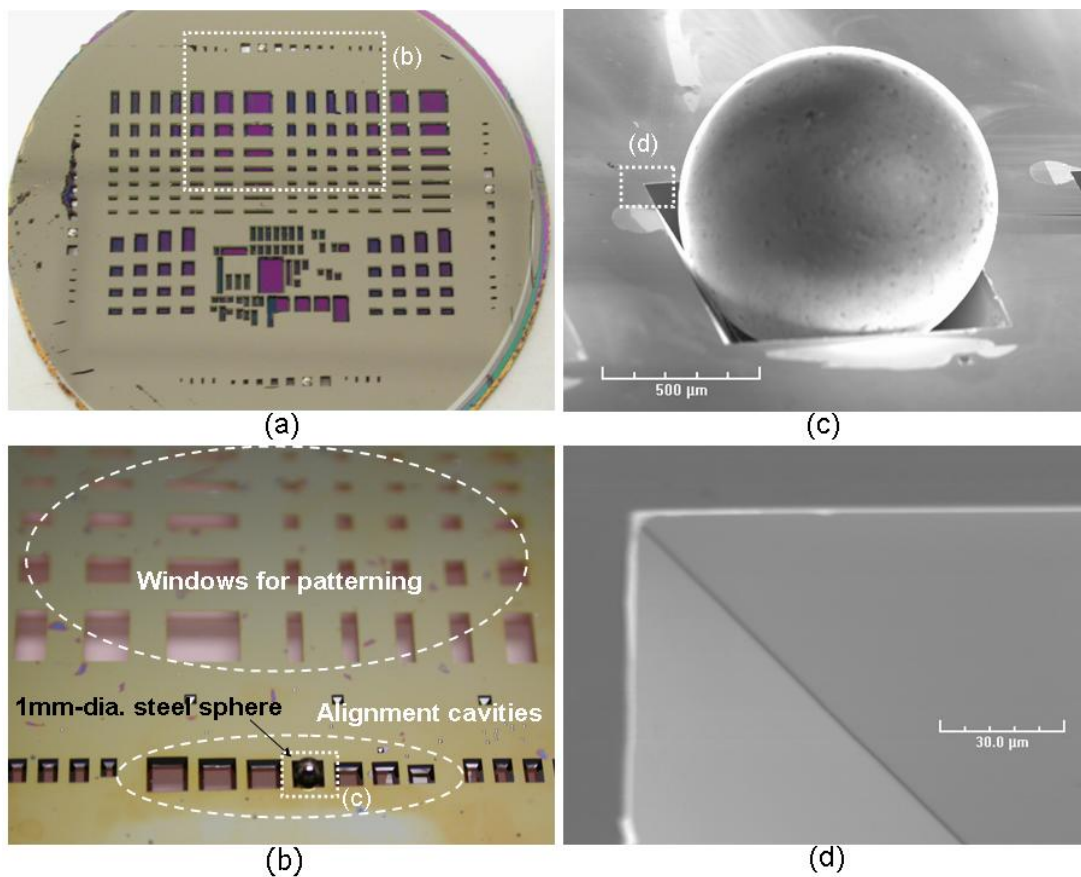


Figure 25. (a) The shadow-mask is seen from the front-side aligning with the carrier wafer by four steel spheres between; (b) A close-in view of a fabricated shadow mask seen from the back-side; (c) Scanning electron microscope (SEM) image of a steel sphere placed on the cavity; (d) SEM image of the cavity edge.

Figure 25b shows a close view of the shadow mask (seen from the back-side) with bulk-etched alignment cavities, deposition windows, and a steel sphere with diameter of 1 mm. For efficient gap control, alignment cavities with different size were fabricated on the shadow mask wafer and the carrier wafer. Close-in scanning electron micrographs of a steel sphere and an alignment cavity are shown in Figure 6c and 6d, respectively. The steel sphere is well situated in the center of the cavity and the surface of the steel sphere and the etched cavity is quite smooth. The surface roughness has very small influence on the alignment accuracy when compared with the irregularity of the etched cavity and steel sphere. According to the manufacturer's product specification, the diameter tolerance and sphericity of the steel sphere are 2.5 μm and 0.6 μm , respectively, which translate into a small gap variation of 1.5 μm from Equation (2).

3.4. EXPERIMENTAL CHARACTERIZATION

To characterize the self-alignment accuracy, the shadow mask wafer and the carrier wafer shown in figure 6a were used to conduct two-layer deposition on three independent fabrication substrates. Photoresist (AZ5214) was used as the adhesive (both of them worked) to fix a fabrication substrate on its carrier wafer separately. After the application of photoresist (with hand pasting), the two wafers were baked on the hotplate for 1min at 110°C. The shadow mask wafer and the carrier wafer were aligned and

mounted on the wafer chuck of an electron-beam evaporator to deposit a chromium layer (~50 nm thick) (refer to Figure 19).

To simulate the real scenario of layer-by-layer device fabrication, the carrier wafer was detached from and re-aligned with the shadow mask wafer to deposit a silicon oxide layer (~80 nm thick) on top of the chromium layer. The transparency of the silicon oxide layer makes it easy to inspect the misalignment of these two layers under an optical microscope, while the different thickness of the two layers facilitate the differentiation of the two layers in topographic measurements. After the deposition, the fabrication substrate was detached from the carrier wafer by soaking into acetone to completely dissolve the photoresist adhesion layer. Figure 26b shows the optical microscopic image of four two-layer patterns at the corners of a $1 \times 1 \text{ cm}^2$ area on the fabrication substrate, which indicates misalignment of a few microns.

For very small misalignment (e.g. $\sim 1 \text{ }\mu\text{m}$), it is difficult to achieve accurate estimation since the smallest resolution of the optical microscope is around $1 \text{ }\mu\text{m}$. To address this issue, topographic images of the two-layer patterns in both x and y directions were obtained with an atomic force microscope (AFM) as a supplement (Figure 26c). The alignment error and its deviation at 8 different points (Figure 26a) are summarized in Table 3 to show the distribution of alignment error and its deviation across the entire substrate. Since the alignment errors in each direction showed similar values, the angular alignment error is then negligible. Both the small transitional and angular alignment errors indicate that simple and accurate self-alignment can be achieved with the new shadow mask system.

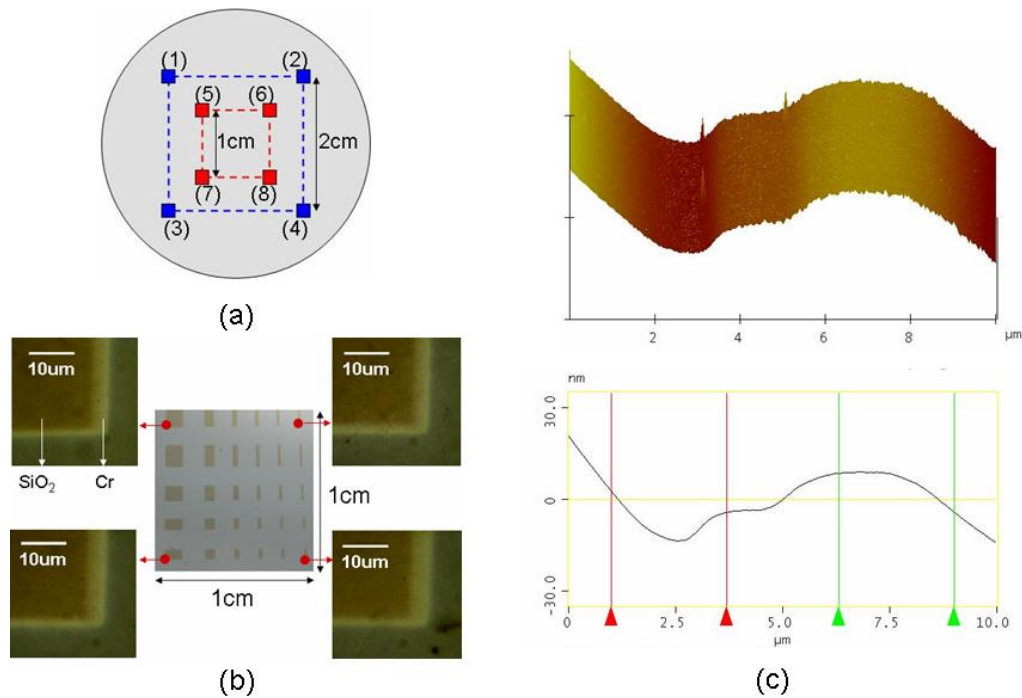


Figure 26. (a) 8 different patterns in $1 \times 1 \text{ cm}^2$ and $2 \times 2 \text{ cm}^2$ boxes for alignment accuracy estimation; (b) Optical microscopic image of four corner patterns of a $1 \times 1 \text{ cm}^2$ box on the fabrication substrate. (c) 3-D topographic image and cross-section line plot of the (x) edge profile of a two layered pattern.

In addition to the alignment accuracy, the fidelity of pattern formation was also evaluated. Although the window opening sizes were designed ranging from $20 \text{ }\mu\text{m}$ to $1000 \text{ }\mu\text{m}$, the actual opening sizes in the shadow mask range from $88 \text{ }\mu\text{m}$ to $1087 \text{ }\mu\text{m}$. This could be due to a number of factors: 1) errors in thickness estimation of the silicon substrate (a larger window needs to be opened to compensate the 54.7° slope for a given wafer thickness), 2) the use of a low-resolution transparent film mask, 3) undercutting of the oxide patterns which were used to protection layer, and 4) undercutting on the $\langle 111 \rangle$

surfaces. A better control of these parameters could further improve the fidelity of pattern formation. On the other hand, the dimension of deposited patterns was found quite close to the actual opening size of the shadow mask within 5 μm of error range (refer to Table 3).

Table 3. Alignment error and its deviation at 8 different points of $1\times 1\text{ cm}^2$ and $2\times 2\text{ cm}^2$ boxes on three different fabrication substrates.

	Δx (μm)	Δy (μm)	Δw (μm)	Δh (μm)
(1)	0.3 ± 0.9	0.1 ± 3.9	-0.6 ± 0.6	-2.4 ± 0.6
(2)	-0.5 ± 2.3	0.1 ± 1.3	-0.9 ± 0.3	-1.1 ± 0.2
(3)	0.1 ± 4.8	0.3 ± 4.2	-5.1 ± 0.3	-6.0 ± 0.6
(4)	0.6 ± 4.8	0.4 ± 0.8	0.9 ± 6.3	-0.5 ± 1.7
(5)	0.4 ± 1.9	1.5 ± 0.3	-2.5 ± 1.8	-0.9 ± 0.4
(6)	0.3 ± 1.8	1.7 ± 0.1	-2.5 ± 1.8	-0.9 ± 0.4
(7)	-0.8 ± 2.9	1.5 ± 0.1	-3.1 ± 1.8	-1.9 ± 1.2
(8)	-0.6 ± 2.7	1.1 ± 0.8	-3.4 ± 2.1	-1.3 ± 0.6

The transitional misalignment and change in the size of the patterns are caused by not only the existence of irregularity in the steel spheres and alignment cavities, but also the geometric configuration in the deposition system, which create both pattern shift

and broadening. Figure 27 shows the pattern shift and broadening phenomena which can be occurred in the conventional deposition chamber.

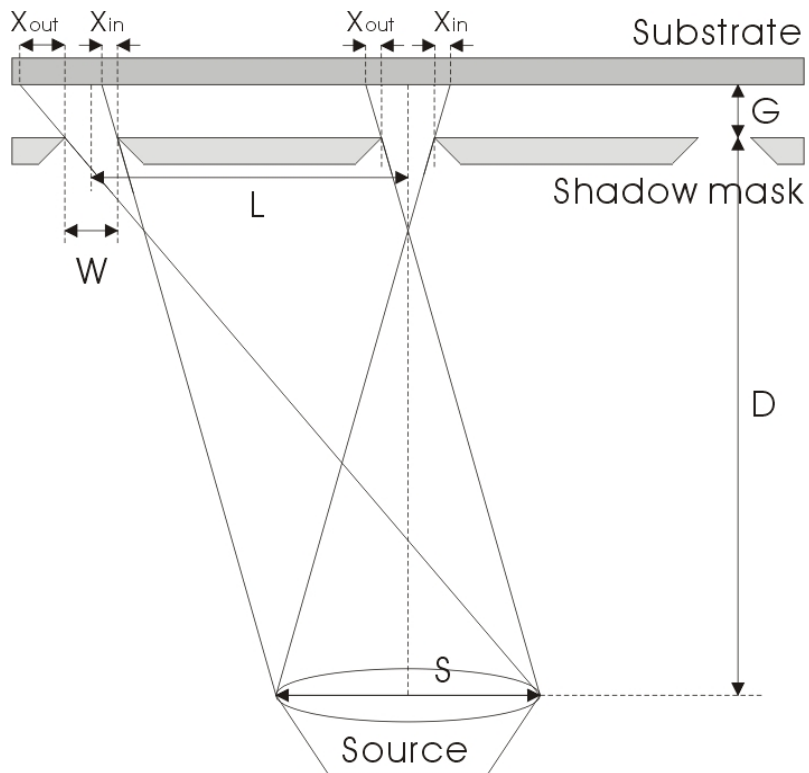


Figure 27. Geometric parameters for the estimation of alignment accuracy in the developed shadow mask system.

The pattern shift (ΔX) and broadening (ΔW) can be derived as

$$\begin{aligned} \left(L - \frac{S+W}{2}\right) / D &= X_{in} / G \\ \left(L + \frac{S+W}{2}\right) / D &= X_{out} / G \end{aligned} \quad \dots\dots\dots (3.3)$$

$$\begin{aligned} X_{in} &= G \cdot \frac{L - (S + W)/2}{D} \approx G \cdot \frac{L - S/2}{D} \\ X_{out} &= G \cdot \frac{L + (S + W)/2}{D} \approx G \cdot \frac{L + S/2}{D} \end{aligned} \quad \dots\dots\dots (3.4)$$

$$W_P = W + X_{out} - X_{in} = W + G \cdot \frac{S + W}{D} \approx W + \frac{G \cdot S}{D} \quad \dots\dots\dots (3.5)$$

$$\begin{aligned} \text{Pattern shift: } \Delta X &= \frac{X_{in} + X_{out}}{2} = \frac{G \cdot L}{2D} \\ \text{Pattern broadening: } \Delta W &= W_P - W = \frac{G \cdot (S + W)}{D} \approx \frac{G \cdot S}{D} \end{aligned} \quad \dots\dots\dots (3.6)$$

Here, W is the window size of the shadow mask and W_P is the width of deposited pattern. In our evaporation system, $S = 2$ cm, $D = 46$ cm, $L = 6$ cm, and $G = 33$ μm . For 1×1 cm^2 box area, L is 6 ± 0.5 cm and ΔX and ΔW can be determined as 2.4 ± 0.2 μm and 1.4 μm , respectively. For a 2×2 cm^2 box area is considered ($L = 1$ cm), ΔX and ΔW can be determined as 2.4 ± 0.4 μm and 1.4 μm , respectively.

3.5. APPLICATION TO ORGANIC THIN FILM TRANSISTOR

In recent years, organic electronics has attracted great attention due to its potential low cost, light weight, and mechanical flexibility [40, 41]. The critical component in organic electronics is the OTFTs, which use either small-molecule or

polymer-based organic semiconductors as active material. Typical OTFTs consist of gate, gate dielectric, source and drain, and organic semiconductor layer (Figure 28).

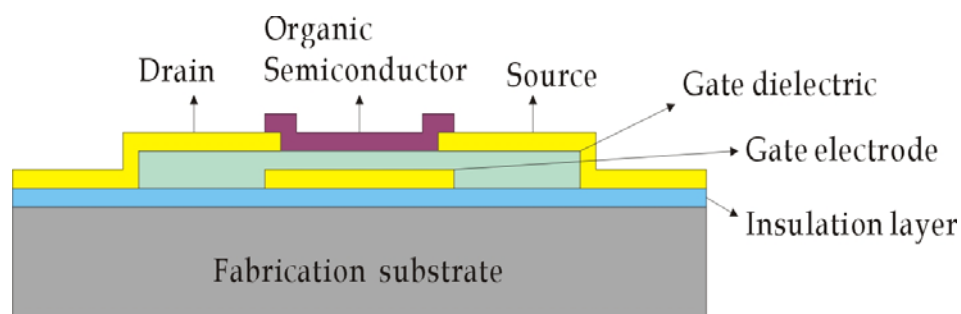


Figure 28. Schematic diagram of the OTFT.

Although polymer-based organic semiconductor materials have been constantly improved and may provide ultimate solution for low-cost fabrication, the small-molecule materials (e.g. pentacene) still offer the advantage of superior electronic properties and material stability [42-45]. To make OTFTs and more complex circuits with small-molecule organic semiconductor, the organic semiconductor layer has to be properly deposited and patterned. As an example of the application of the developed shadow mask system, pentacene OTFTs have been successfully fabricated and tested on silicon substrates.

To simplify the fabrication process, the carrier wafer was directly used as the device substrate and all the material layers (except pentacene) were patterned with lift-off process. First, a gold layer (1000Å thick) was deposited and patterned to form the gate. Next, a silicon oxide (5000Å thick) layer was deposited and patterned to form the

gate dielectric. A second gold layer (1500Å thick) was deposited and patterned to form the source and drain. Finally, the pentacene layer (4500 Å thick) was deposited and patterned using the self-aligned shadow mask to complete the OTFT fabrication. Figure 29 shows the optical microscopic image of the OTFTs.

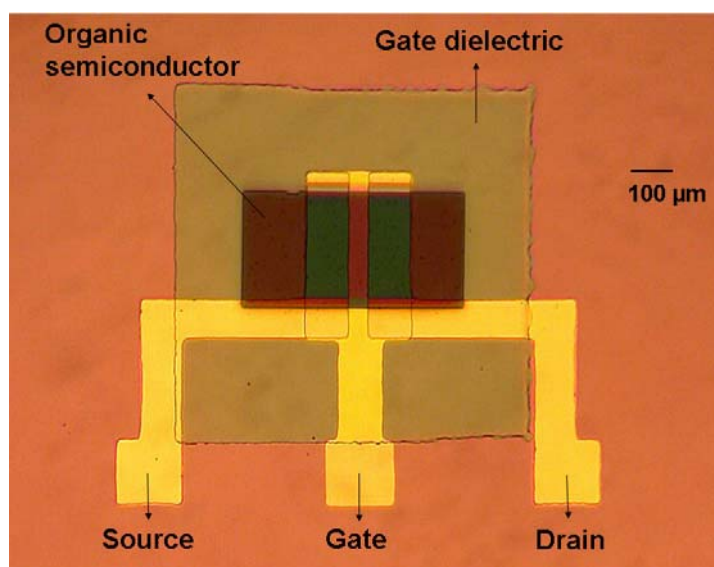


Figure 29. Optical microscopic image of a fabricated OTFT.

The rectangular patterns of pentacene layer were well aligned with drain/source electrodes. The electrical properties of the pentacene OTFTs were characterized using a HP[®] 4155B semiconductor parameter analyzer. Figure 30 shows the drain-source current (I_{DS}) as a function of drain-source bias voltage (V_{DS}) and gate-source bias voltages (V_{GS}) for an OTFT with a channel length and width of 50 μm and 250 μm, respectively, which clearly indicates the field effect. Since the pentacene is p-type semiconductor, an increasing negative V_{GS} tends to accumulate more charge carriers

(holes) at the interface between the pentacene layer and the gate oxide and thus result in higher I_{DS} .

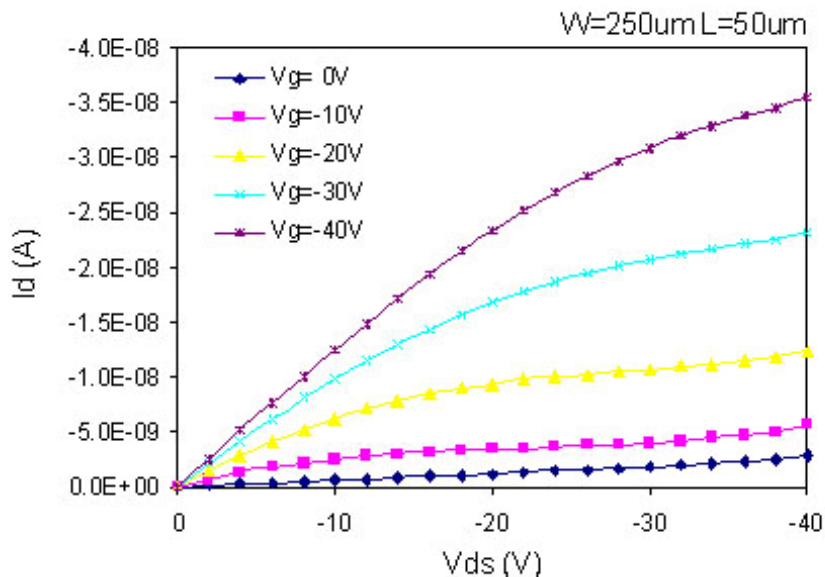


Figure 30. The Drain-source current (I_{DS}) as a function drain-source bias voltage (V_{DS}) and gate-source bias voltages (V_{GS}) for the OTFT shown in Figure 29.

3.6. CONCLUSIONS

A novel shadow mask system with accurate self-alignment and gap control capability has been demonstrated. The matching pairs of steel spheres and pyramidal cavities provide a simple and easy way to achieve self-alignment and gap control without using sophisticated setup. Silicon micromachining plays a key role in creating the needed pyramidal cavities in a straightforward and precise manner. When working

with a robot in vacuum deposition chambers, this shadow mask technique is expected to be capable of a layer-by-layer deposition and direct-patterning in a continuous fashion without breaking the vacuum to significantly save the fabrication cost and time. Compared with conventional shadow masks (with an overall alignment accuracy of 10s of microns), the new shadow mask technique with high accuracy of self-alignment and gap control can be readily adapted to enable higher density of integration and thus higher performance of organic microelectronics.

4. INTEGRATION OF MICRO-PATTERNING TECHNIQUE INTO THE SMALL SUBSTRATE

4.1. INTRODUCTION

In recent years, the trend for miniaturization in electronics and optics has strongly affected the electrical/optical components. As the components industry started to reduce package sizes more and more, the post integration of microstructures with the small chips become much more difficult especially when complex fabrications are involved. As a result, the photolithography, a conventional micro-patterning technique, will not be compatible with the small advanced devices (electronic or optical devices). For example, integration of MEMS (Microelectromechanical systems) into the CMOS circuits is challenging issue due to the incompatibilities of MEMS fabrication with the standard IC foundry processes [14]. On the other hand, monolithic integration of micro optical lens with the optical fiber is also challenging for miniaturized optical systems [46]. However, current microfabrication techniques are not compatible with the optical fiber and other advanced devices. In this section, novel embedding techniques will be discussed for enabling integration of complex microstructures with those advance devices mentioned above.

The integrated microsystems with CMOS (Complementary metal–oxide–semiconductor) circuits have attracted great attention due to system miniaturization,

efficient interconnection, and higher performance [47]. However, it has been always a challenging issue to achieve efficient integration due to the incompatibilities of MEMS (Microelectromechanical systems) fabrication with the standard IC foundry processes. To overcome this problem, a post-CMOS integration strategy is often adopted, in which the CMOS circuits are first fabricated and the MEMS components are built either into or onto the finished CMOS substrates as add-on components [48, 49]. However, current CMOS chips are dramatically shrinking in size for higher component density and lower fabrication cost. This miniaturization makes an individual finished CMOS chip extremely difficult to handle and further process. This situation has become a fundamental bottle-neck issue in post-CMOS integration of MEMS components.

Embedding the small CMOS chip is a good way to solve this problem. As shown in Figure 31, an embedding technique which uses four silicon supporting pieces surrounding a small CMOS chip has been introduced [50].

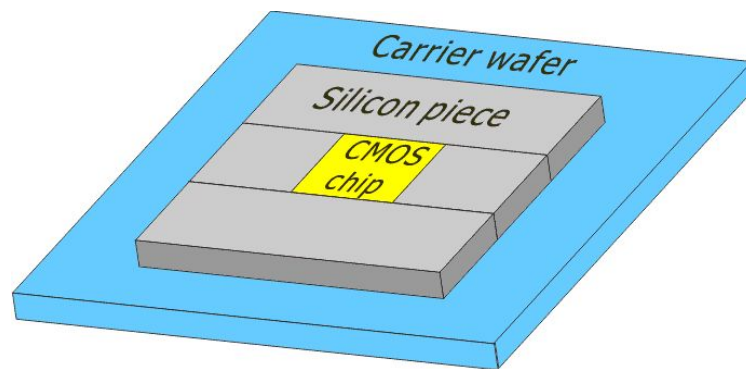


Figure 31. An example of the embedding technique for post processing on the small CMOS chip [50].

This approach could effectively avoid the edge-bead phenomenon in the spin-casting process which is a serious problem for the small chip substrate [12]. However, there are still critical issues in terms of planarization of surface. First, the height of the CMOS chip might be different from the silicon pieces slightly since the every silicon wafer has a few micrometers of variance in height. In addition, the several micrometers of gap between the CMOS chip and silicon pieces are inevitable in practical applications. These height mismatch and gap make it impossible to fabricate large micro structures across the boundary of the chip. To address this issue, the development and application of a novel and straightforward polymer embedding technique was reported, which is capable of significantly extending the effective processing surface area of an originally small CMOS chip, thus enabling efficient post-CMOS integration of various MEMS components, which can be very complex or (more importantly) even larger than the CMOS chip itself (Figure 32).

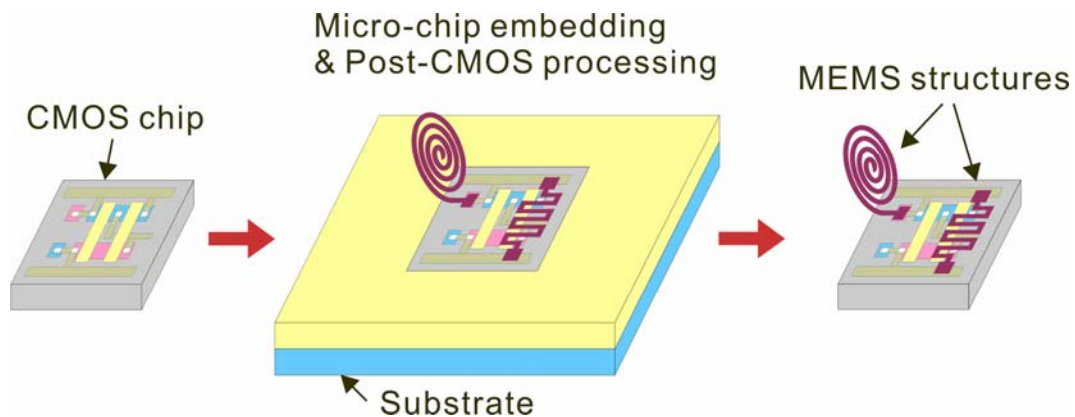


Figure 32. Schematic diagram of post-CMOS integration technique using polymer embedding technique.

This embedding technique can also be applied to integration of microstructures with optical components. The interest in fiber optic biosensor has continuously grown due to improvement of passive optical components and optical fibers. Since optical fiber is a passive component of a fiber-optic sensing system, it contains neither moving parts nor electrical circuitry and is therefore completely immune to all forms of electrical interference. This characteristic makes it possible to isolate the sensing system from electrical interference. Furthermore, there is no possibility of a spark, and thus no danger of shock, allowing its safe use for biomedical application. However, conventional fiber optic systems suffer from coupling loss and complexity of the fiber positioning system [15]. Here, a novel micro patterning technique was proposed for fabricating microstructures on the optical fiber with simple and straightforward fabrication process. The micro-Fresnel lens was fabricated on the tips of optical fiber for collimating and refocusing the light beams with excellent positioning accuracy.

4.2. POST CMOS INTEGRATION WITH THE SMALL VCO CIRCUIT CHIP

4.2.1. Polymer Embedding Technique

A novel polymer embedding process was demonstrated for planarization of the small CMOS chip. In order to test the small chip embedding process, a dummy silicon chip which has the same dimension with a real CMOS chip was used. Figure 33 shows a schematic process flow of the polymer embedding technique. SU-8 resists was chosen as

the filling material for the small chip embedding due to its simple processing and excellent mechanical strength and chemical stability after curing.

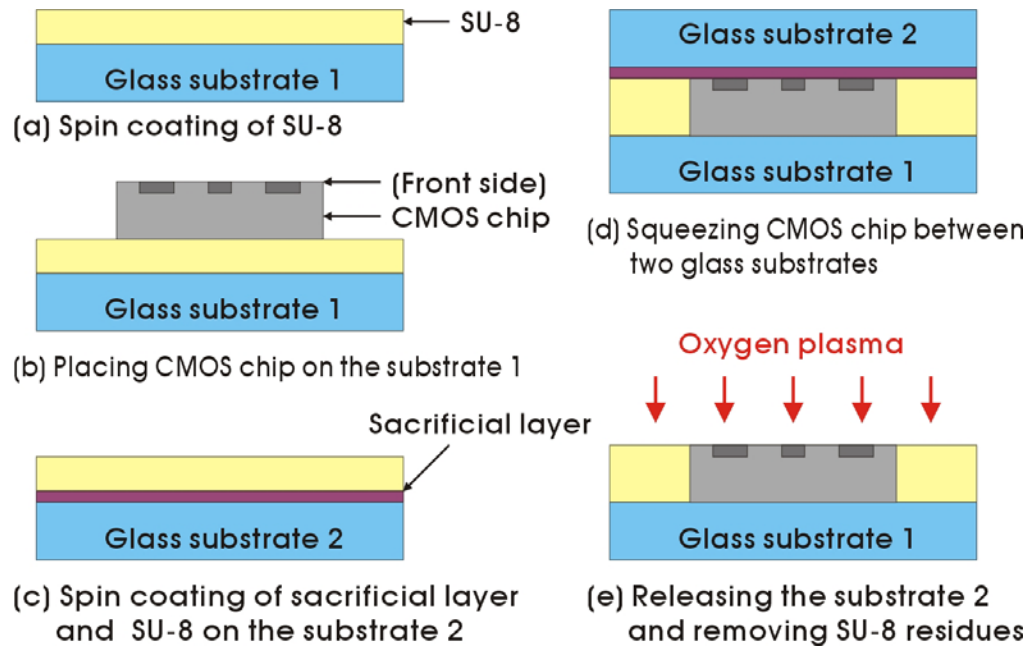


Figure 33. Schematic process flow of the new micro-chip embedding technique using SU-8 as the filling material.

For embedding the silicon chip, approximately 1ml of SU-8 100 was applied on the first glass substrate ($1 \times 1 \text{ in}^2$) and spin-coated (Figure 33a). The spin coating of SU-8 100 consists of two steps; spread cycle and spin cycle. In the spread cycle step, the spin speed ramped to 500 rpm at 100 rpm/second acceleration and was held at this speed for 7 seconds to allow the resist to cover the entire surface. In the spin cycle, the spin speed ramped to 1500rpm at an acceleration of 300 rpm/second and was held for a total of 30 seconds. The spin coating of SU-8 100 effectively removed the bubbles inside SU-8,

which could be carried out in the vacuum jar alternatively. At this condition, the thickness of SU-8 is around 180 μm according to manufacturer's data.

Then the dummy silicon chip to be embedded was placed on the SU-8 coated glass substrate (Figure 33b). As the second process, MicroChem's OmniCoat was spin coated on the second glass substrate ($1 \times 1 \text{ in}^2$) as a sacrificial layer at 1000 rpm for 30 sec with acceleration of 100 rpm/s, and then baked on the hotplate at 200°C for 1min. Next, the SU-8 100 was spin coated on the second glass substrate in the same manner (Figure 33c). As the third process, the two glass substrates were soft baked on the hotplate at 65°C for 20min and 95°C for 1hr. Then, the two glass substrates were placed face to face and pressed together with the silicon chip inside (Figure 33d). In the fourth step, the front side of entire stack was then exposed to UV light at $12\text{mW}/\text{cm}^2$ for 1min, and post baked on the hotplate at 65°C for 1min and 95°C for 20min. Finally, the whole stack was immersed in MicroChem's Remover PG for removing the sacrificial layer. And the second glass substrate was detached from the silicon chip and the first glass substrate. Any SU-8 residue on the surface of the embedded silicon chip could be cleaned by the oxygen plasma in reactive ion chamber (Figure 33e).

Figure 34 shows optical microscopic images of the silicon chip embedded in SU-8 before and after oxygen plasma cleaning. To check the planarization of SU-8 surface with the silicon chip, the surface profile was measured with the Dektak surface profiler. Excellent smoothness and height match ($\leq 0.2 \mu\text{m}$) of the extended SU-8 surface have been achieved, which make it suitable for microfabrication purposes (Figure 35).

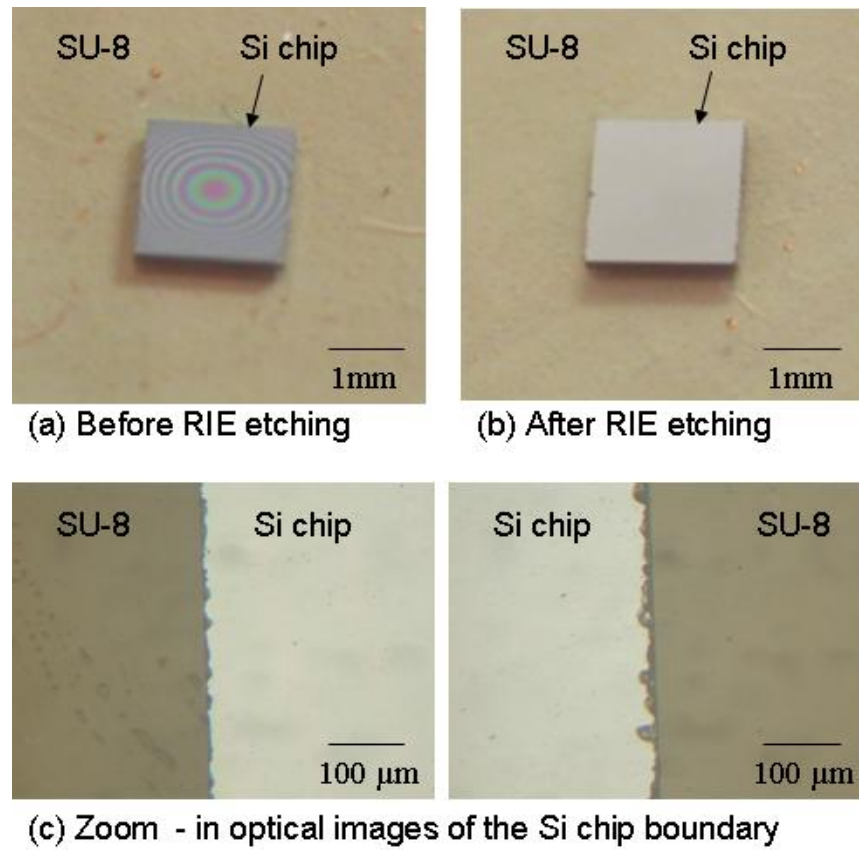


Figure 34. Optical images of a dummy silicon chip ($2 \times 2 \text{mm}^2$) embedded in SU-8.

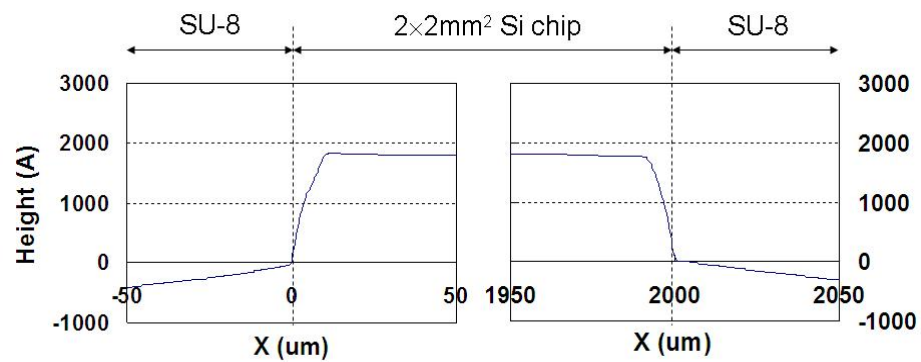


Figure 35. Surface profiles at the interface between the embedded silicon chip and SU-8 after plasma cleaning.

4.2.2. CMOS VCO Circuit

As an application of the novel micro-chip embedding technique, the on-chip integration of a complex MEMS structure was demonstrated on a small CMOS VCO (Voltage-controlled oscillator) chip. On-chip integration of high performance RF (radio frequency) passive components is critical for the development of next generation wireless communication systems with higher operating frequencies, lower noise level and reduced power consumption [51]. However, this has been a challenging issue due to the limited quality factors (Q) and large footprint of current on-chip passive components (e.g. inductors [51, 52]) which are constructed horizontally on circuit substrates. Therefore, building the passive components vertically is expected to significantly reduce the substrate loss and parasitics as well as the footprint [53]. However, there are still two fundamental issues in this application which limit conventional post CMOS processing. First, the CMOS VCO chip ($2 \times 2 \mu\text{m}$) is too small to be processed with conventional photolithography. Second, the vertical ring inductor requires a large processing area that outreaches the boundary of the CMOS VCO chip although it has a small footprint in the final structure. By using the developed micro-chip embedding system, the vertical ring inductor was successfully integrated onto the 5.8 GHz CMOS VCO chip.

Figure 36 shows the schematic of the differential 5.8 GHz CMOS VCO circuit, which consists of a VCO core and an output buffer for driving a 50 Ohm load by either of its differential outputs.

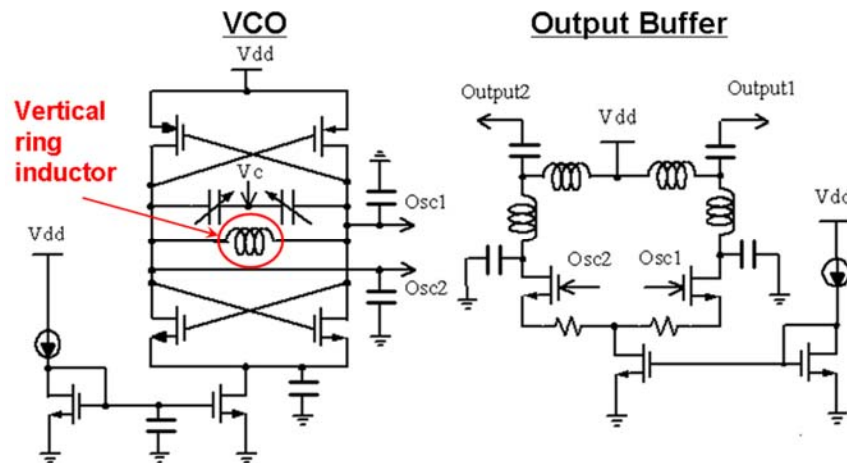


Figure 36. Schematic of the 5.8 GHz VCO circuit and output buffer.

The VCO core has a passive LC parallel tank and two complementary cross coupled NFET and PFET pairs. The oscillation frequency of the VCO is preliminarily determined by the resonance frequency of the tank. In our design, an inductance of 1nH is necessary for 5.8 GHz oscillation. A high-Q vertical ring inductor was developed and integrated to reduce the loss of the LC tank, which is expected to result in a stronger oscillation, lower phase noise in frequency domain and smaller jitter in time domain [54].

4.2.3. Design of Ring Inductors

The vertical ring inductor was designed to realize the inductance of 1nH with minimum substrate parasitics and loss, and still have the simplicity with which it can be fabricated and integrated on the VCO chip. Different from conventional 2D inductor design, trade-offs among electrical performances, mechanical stability and ease of

fabrication were considered. Although ring inductors have lower inductance density and larger form factors than the commonly used spiral inductors, they have much simpler structure for easier fabrication and integration. As the operation frequency of RF ICs goes higher, the required inductance/capacitance values will drop accordingly. As a result, ring inductors could also become a viable and preferable candidate for on-chip inductors. Meanwhile, very small substrate occupancy can be also achieved when the ring inductor is built vertically. As shown in Figure 37, the ring inductor consists of both circular and straight portions. The circular portion forms the ring inductor, while the straight one separates the ring inductor from the substrate to increase electrical isolation and also facilitate the inductor fabrication.

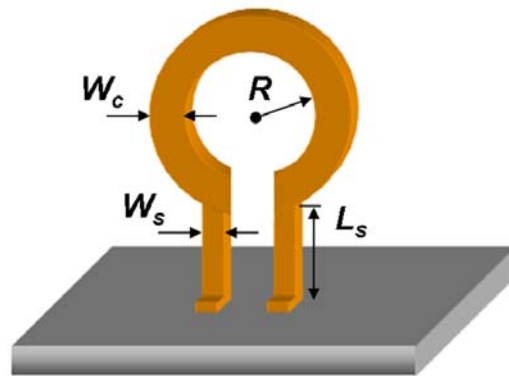


Figure 37. Schematic of vertical ring inductor.

Due to its high electrical conductivity and mechanical ductility, copper was chosen as the structural material of the inductor. Ring inductors with different geometric parameters were designed. While the total inductance value of the inductor is mainly

determined by the total length and circular/straight ratio of the conductor line, its width and thickness are critical factors to affect the Q factor. Generally, a wider and thicker (up to certain extent limited by the skin depth) conductor line would result in lower resistance and thus higher Q factor. This also leads to a stiffer inductor structure with better mechanical stability. However, if the inductor structure becomes too stiff, it will be difficult to realize the vertical placement of the inductor on chip. The structural stability of the vertical ring inductor under mechanical shock occurring in the most vulnerable direction (perpendicular to the inductor plane) was also estimated using cantilever beam theory [55]. Based on our previous experience in the mechanical testing, a thickness of $6\ \mu\text{m}$ was chosen for the inductor fabrication.

The S_{11} parameters of different inductor designs were simulated with Sonnet® and the inductance and quality factors were extracted. Figure 38 and Figure 39 shows characteristics of ring inductors according to the design parameters.

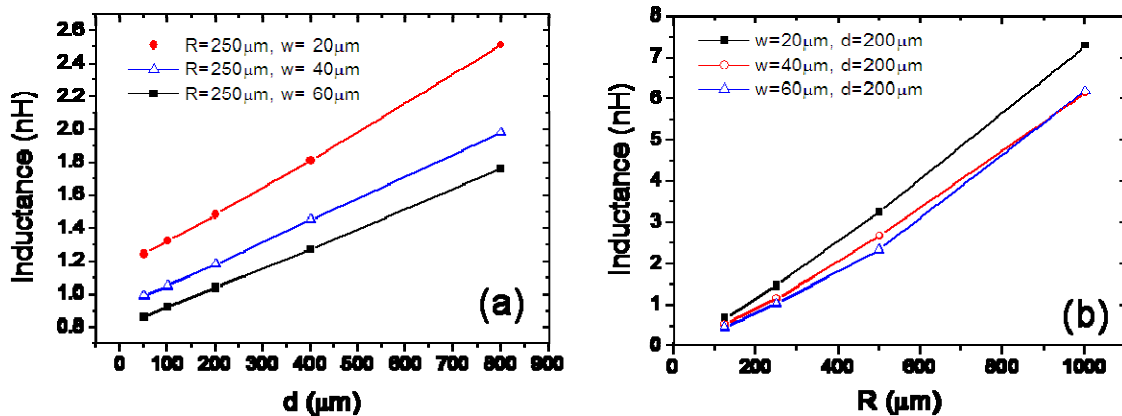


Figure 38. Simulated inductances according to the length of straight (a) and circular (b) portions.

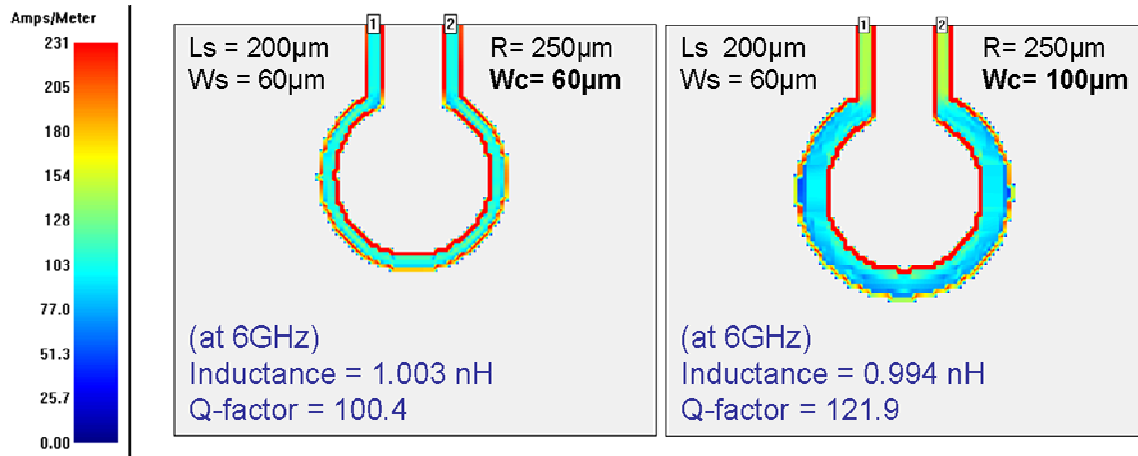


Figure 39. Inductor performance according to structural design parameters.

The inductance of ring inductor was linearly increased according to the length of straight and circular portions as expected. In order to achieve 1nH of inductance, 250um of ring radius and 200um of straight portion were selected. On the other hand, wider ring inductor provides low resistance, and thus higher quality factor. However, wider width of the straight portion requires large force to bend the ring inductor vertically, which may cause separation of the ring structure from the substrate. Figure 40 shows the inductance and Q factor of an optimal inductor design ($R = 250\mu\text{m}$, $w_c = 100\mu\text{m}$, $l_s = 200\mu\text{m}$, $w_s = 60\mu\text{m}$). Meanwhile, the maximum angular deflection (at the free end) of the vertical ring inductor structure under mechanical shock was estimated to be only 0.002° per g (9.8m/s^2), which shows its excellent mechanical stability.

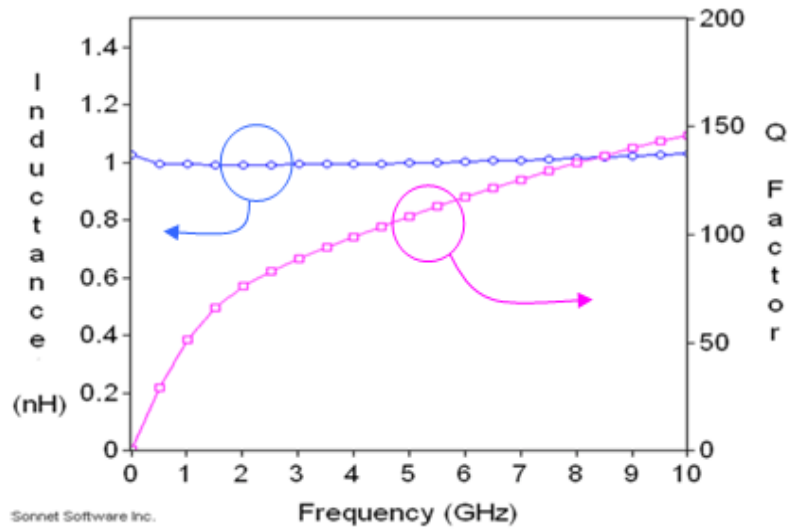


Figure 40. Simulated inductance value and quality factor of an optimal vertical ring inductor design.

4.2.4. Post CMOS Integration of Vertical Ring Inductors

As an application of the new embedding technique, an integrated 5.8GHz VCO with MEMS vertical inductors was demonstrated on a $2 \times 2 \text{mm}^2$ CMOS chip. The VCO chip was first prepared using TSMC $0.25 \mu\text{m}$ CMOS process, which include two interfacing pads for integrating vertical inductor. Employing MEMS vertical inductors in RFIC design could save expensive circuit “estate” while significantly reducing substrate loss and parasitics. However, building the inductors vertically requires much more complex fabrication process, which is almost impossible to carry out on such a small chip [56]. With the new embedding technique, the integration of MEMS vertical inductor has been achieved successfully.

To achieve vertical ring inductors, planar ring inductors were first fabricated on the substrate and then bent vertically using plastic deformation magnetic assembly (PDMA) [56]. PDMA exploits the behavior of magnetic materials in a transverse magnetic field and uses it to raise materials off the substrate. It provides a robust and controllable method to build vertical microstructures in a parallel and batch-scale fashion. However, the original PDMA process involves a “blanket” etching of either silicon oxide or aluminum as the “sacrificial” material for the implementation of PDMA. Although this is compatible with bare silicon substrates, it will cause problems with CMOS substrates since silicon oxide and aluminum are construction materials for on-chip CMOS circuits and the etching will inevitably destroy the prefabricated circuit components.

To address this issue, different materials have been tested and finally zinc oxide was chosen as the “sacrificial” material, since it can be easily deposited and etched, which is compatible with CMOS substrates. The CMOS VCO chip was embedded in SU-8 using the novel micro-chip embedding technique for enabling conventional semiconductor process and extending possible processing area (Figure 33). The entire on-chip integration process of the vertical ring inductor has been conducted as the following steps (Figure 41):

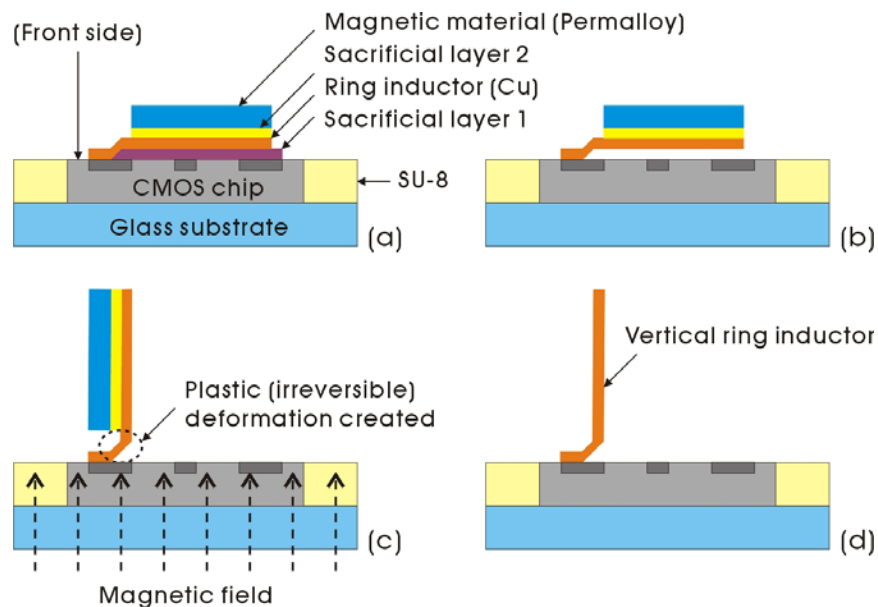


Figure 41. Schematic process flow for the fabrication of MEMS vertical inductors on CMOS substrates.

- 1) The ring inductor (6- μm -thick copper layer) was fabricated on the chip substrate using thermal evaporation and electroplating. The inductor structure was separate from the substrate by the first sacrificial layer (zinc oxide) (Figure 41a).
- 2) To implement PDMA, a magnetic material piece (20- μm -thick permalloy) was deposited onto the ring inductor structure. The permalloy piece was separate from the ring inductor structure by the second sacrificial layer (photoresist) (Figure 41a).
- 3) After completely removing the zinc oxide layer (Figure 41b), a magnetic field was applied underneath the substrate to conduct PDMA. The magnetization of the permalloy piece created a torque to lift the ring inductor structure and created irreversible and thus permanent bending to hold the ring inductor in its vertical position (Figure 41c).

4) After PDMA, the second sacrificial layer was completely removed to detach the permalloy piece from the ring inductor structure (Figure 41d).

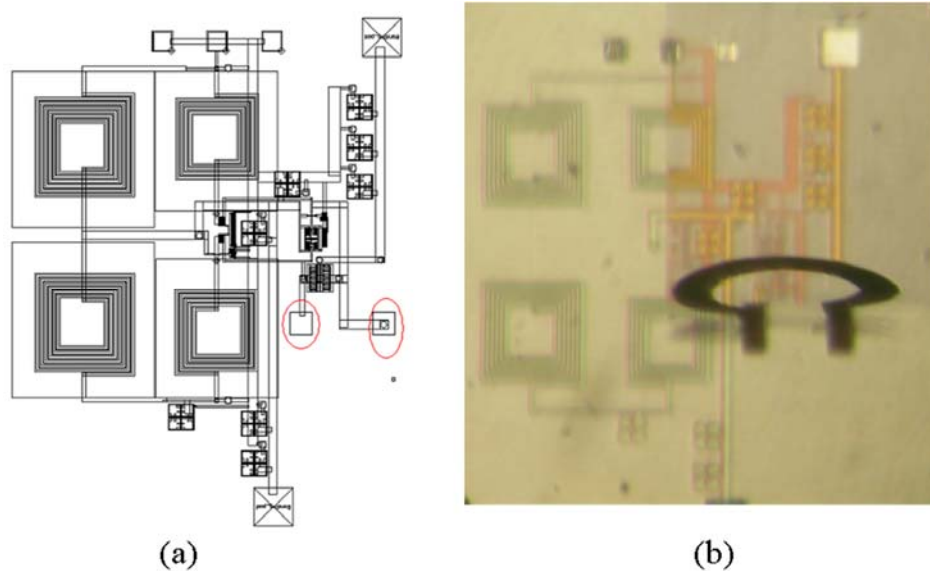


Figure 42. (a) Layout design of the 5.8 GHz VCO. The two contact pads circled in red were used to interface with the vertical ring inductor. (b) Optical microscopic image of the integrated vertical ring inductor on the $2 \times 2 \text{mm}^2$ VCO chip.

Finally, the integration of the vertical ring inductor was successfully carried out on the CMOS VCO chip using the developed micro-chip embedding technique. Figure 42 shows the layout design of the VCO circuit and the microscopic image of the complete VCO circuit integrated the vertical ring inductor. Here, two contact pads were designed to interface with the vertical ring inductor. The size and separation of the two contact pads are two important design parameters for the on-chip integration, which is essentially a trade-off between the mechanical robustness and electrical performance of the inductor. Larger contact pads and separation provide better mechanical adhesion and

stability of the vertical inductor structure, while at the cost of increased footprint and potential higher parasitics. Based on our previous experience and EM simulation, a pad size of $50\mu\text{m}\times 50\mu\text{m}$ and separation of $220\mu\text{m}$ were selected to ensure both satisfactory mechanical and electrical performance of the vertical ring inductor.

4.2.5. Testing

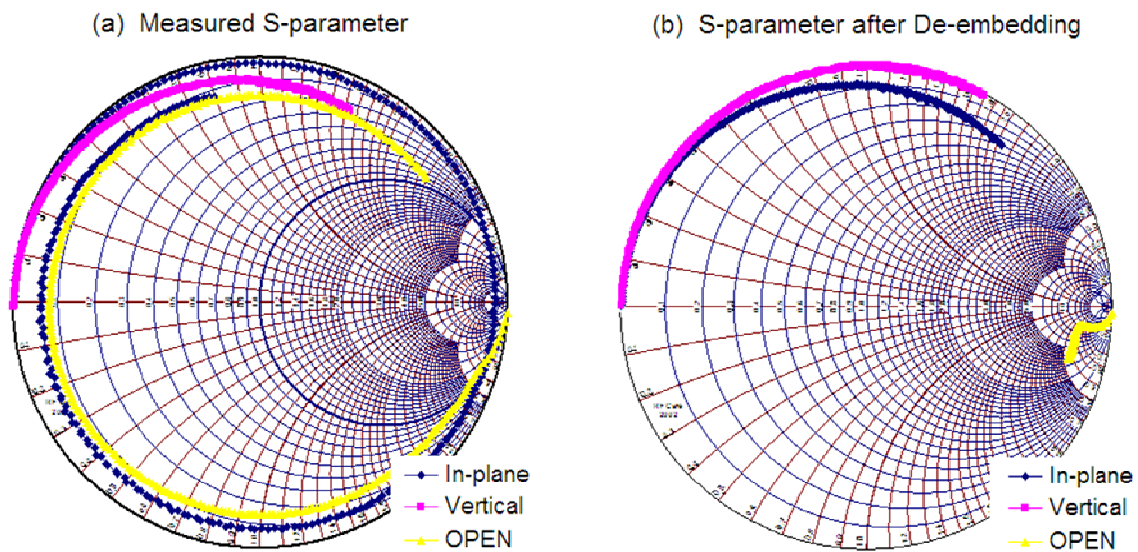


Figure 43. Comparison of Smith charts for measured S-parameter (a) and S-parameter after De-embedding.

The S_{11} parameters of the fabricated vertical ring inductor were measured up to 8.1GHz using HP[®] 8510 network analyzer. After de-embedding the contact pads, both the inductance and Q factor were extracted from the S_{11} measurement results. The measured and de-embedded S-parameters were plotted in the Smith chart and compared as shown in Figure 43.

Here, the vertical ring inductor was compared with in-plane inductor to estimate the improvement of quality factor. From the smith chart, the inductance (L) and quality factor (Q) can be obtained by one-port network analysis (APPENDIX D).

$$L = \frac{Z_0}{2\pi f} \cdot \frac{2s_I}{(1-s_R)^2 + s_I^2}$$

$$Q = \frac{Z_I}{Z_R} = \frac{\omega L}{R} = \frac{2s_I}{1-s_R^2 - s_I^2}$$

Where s_R and s_I are the real and imaginary parts of de-embedded S-parameter, and Z_0 and f are the characteristic impedance and frequency, respectively.

Figure 44 shows the extracted inductance value and Q factor for the vertical ring inductor based on the optimal design, which closely match the simulation results shown in Figure 40. The inductor achieved an inductance of 1nH over a wide range of frequency and its Q factor reaches ~110 at 5.8 GHz, indicating a superior performance over conventional on-chip 2D inductors with Q factors around 10.

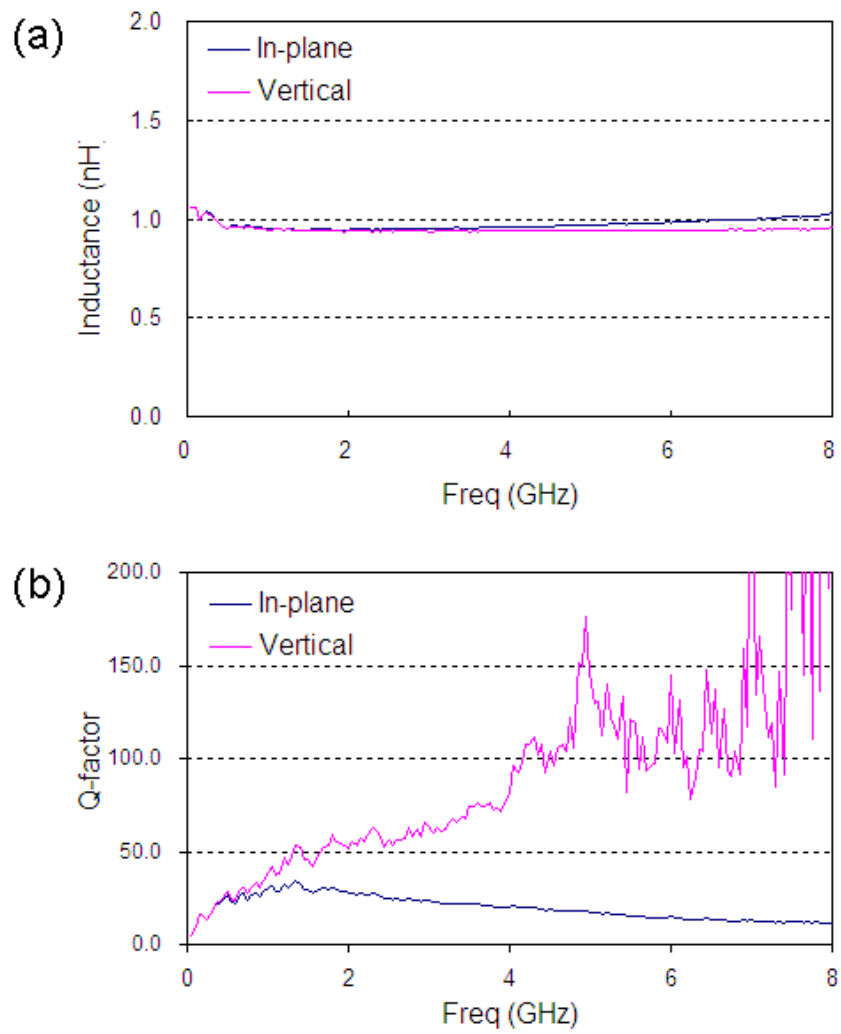


Figure 44. Inductance and quality factor of the in-plane and vertical ring inductors extracted from de-embedded S_{11} parameters.

4.3. MICRO PATTERNING ONTO THE OPTICAL FIBER END

4.3.1. Design of the Fresnel Zone Plate

Figure 45. shows the schematic diagram of the Fresnel zone plate (FZP) structure, where a zone plate center being opaque, was fabricated by Chrome patterning on the fused silica. The dimensions of the FZP are obtained from the classical equation used in designing conventional FZP as follow:

$$r_n = \sqrt{n\lambda f + \frac{n^2 \lambda^2}{4}} \dots\dots\dots (4.1)$$

where f is the focal length, λ an incident wavelength, and n an integer starting from 1.

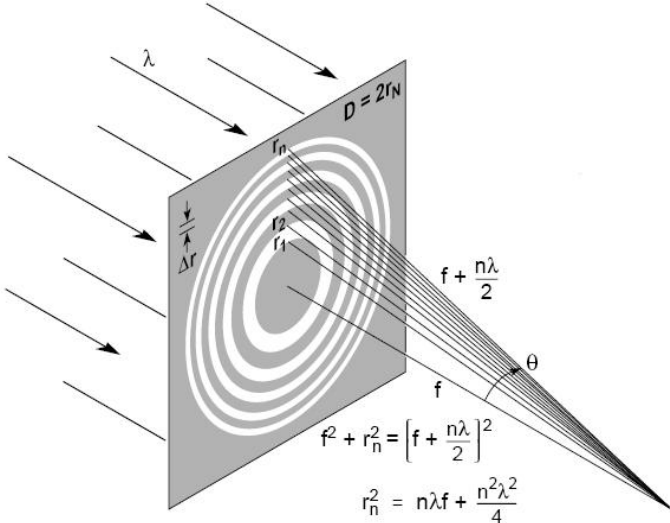


Figure 45. A Fresnel zone plate lens with plane wave illumination, showing only the convergent (+1st) order of diffraction [57].

The core diameter of optical fiber limits the radius of zone and thus the number of zones. According to eq. (4.1), the width of ring is decreasing in outer region. This indicates that the outmost ring should be very narrow to ensure enough number of rings. However, the minimum line width of the ring patterns was limited to about 2 μm because of the critical dimension limits in photolithography. Regarding these factors, the optical fiber with 200 μm of core diameter was chosen to ensure enough number of zones for focusing the light. The focusing properties of the FZP are simulated and analyzed by TEMPEST, a Maxwell equation solver based on 3D finite-difference time-domain (FDTD) method.

Due to the limitation of memory size of our workstation, we used shorter focal length (5 μm and 10 μm). The thickness of Chrome film is approximately one order thicker than skin-depth (corresponding to $t_{\text{Cr}} = 200 \text{ nm}$). We used 0.633 μm as incident light obtained from He-Ne lasers and the focal lengths were chosen to 5 μm and 10 μm . The dielectric permittivity of Cr and fused silica at this wavelength is $\epsilon_{\text{Cr}} = -1.28 + i20.46$ and $\epsilon_{\text{fused silica}} = 2.13$, respectively [58], and circularly polarized light is illuminated from the bottom of the fused silica. Figure 46. (a) and (b) show the distribution of the transmitted field intensity on the xz -plane for $f = 5 \text{ }\mu\text{m}$ and $f = 10 \text{ }\mu\text{m}$, respectively.

It is clear that the simulation results are identical to what we expected when the FZP was designed by the equation of conventional FZP. Based on this simulation results, we can image the results of extend focal length (i.e., $f = 2 \text{ mm}$). According to changing of focal length, the size of transparent zones was shown in Figure 46. (c) and (d) in which focal length was 5 μm and 10 μm , respectively.

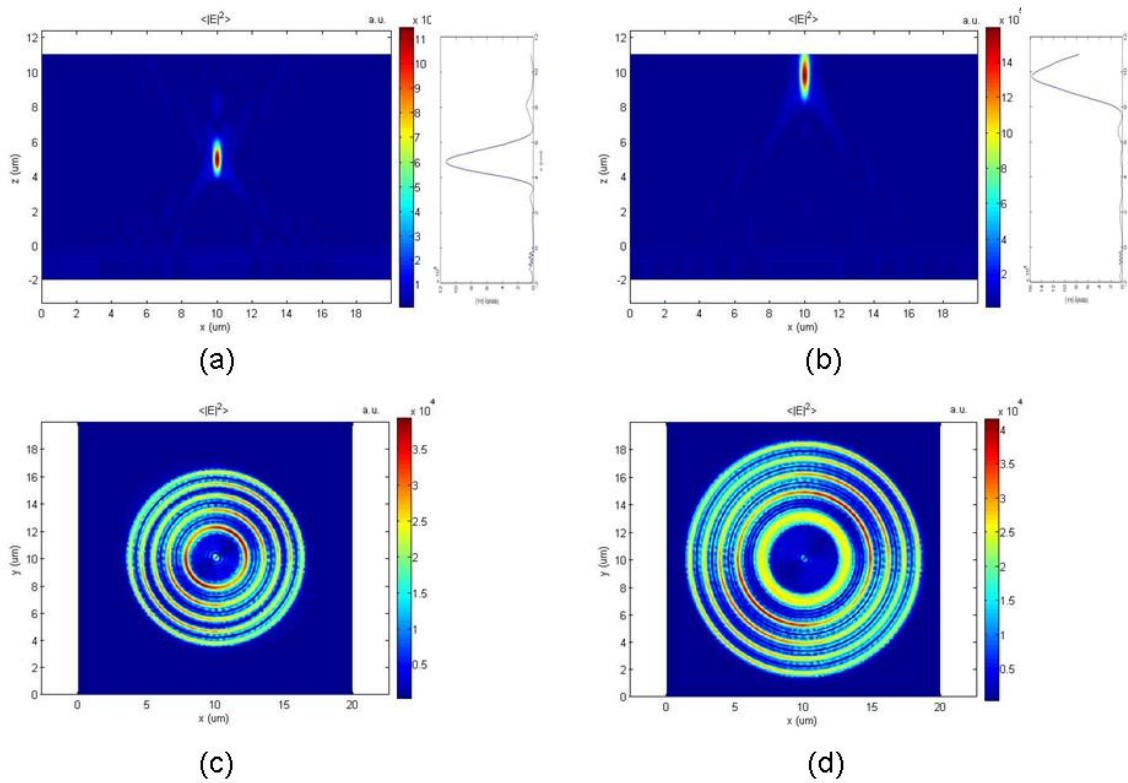


Figure 46. Simulated field distributions of the transmitted field in x-z plane: (a) $f = 5$ μm and (b) $f = 10$ μm , and simulated field distributions of Cr exit plane (x-y plane): (c) $f = 5$ μm and (d) $f = 10$ μm (Courtesy of Hyun-Chul Kim).

4.3.2. Optical Fiber Embedding with a Silicon Holder

A novel fabrication technique was demonstrated for integrating Fresnel lens into the optical fiber using a silicon holder with deep etched holes. The optical fibers can be fixed to the silicon holder with a fiber jacket or by itself. Here, the outer diameters of the cladding and fiber jacket are 230 μm and 500 μm , respectively. The two types of

silicon holders were designed for holding an optical fiber with or without the optical fiber jacket (Figure 47).

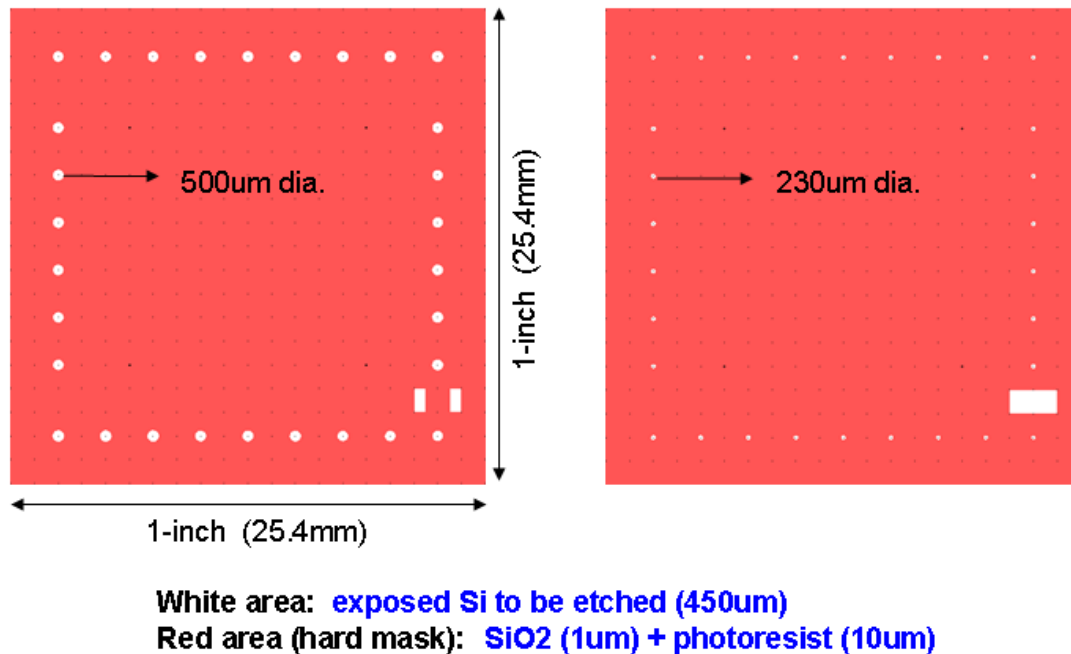


Figure 47. Mask layout designs for silicon wafer holders for fixing the optical fibers. (a) with 500um of hole diameter. (b) with of 230um of hole diameter.

The optical fiber holders were fabricated by conventional microfabrication processes. First, 100nm of silicon dioxide layer was thermally grown to the silicon wafer (Figure 48a). In order to protect silicon wafer underneath during longer etching, the thick photoresist (AZ 4620) was spin-coated at 2000 rpm for 40sec, which gives 10um thick film (Figure 48b). Then, the photoresist film was exposed in UV light with a photomask and finally developed (Figure 48c). The underneath oxide layer was etched through the patterned photoresist film (Figure 48d). The deep reactive ion etching

(DRIE) was conducted to etch through the silicon wafer using Bosch process (Figure 48e). Finally, the photoresist and oxide layers have been entirely removed by acetone and buffered oxide (Figure 48f).

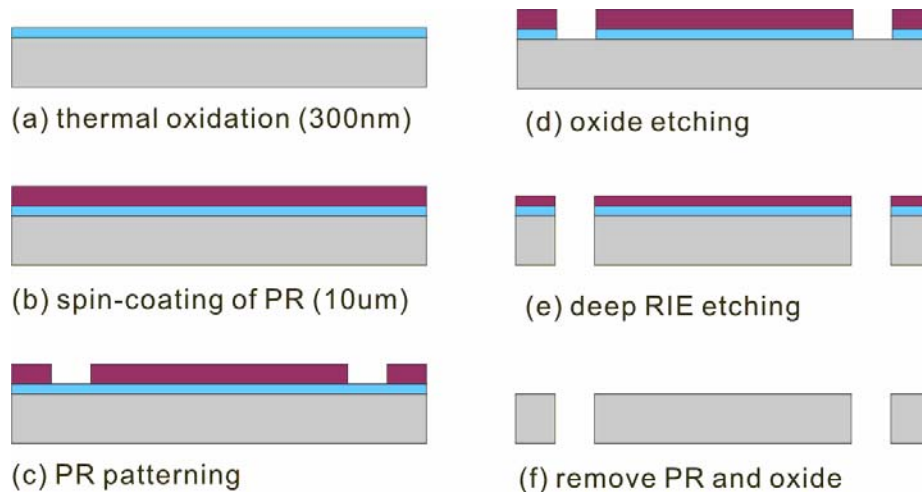


Figure 48. Fabrication steps of the optical fiber holder.

The fabricated silicon substrate with cylindrical holes was shown in Figure 49a. The dimension of the silicon holder is $1 \times 1 \text{ in}^2$. Next we rolled the optical fibers and fixed with tapes to avoid detaching from the substrate during the spin coating or mask alignment. Then the optical fibers were inserted into the holes in the silicon substrate and fixed by super glue (Figure 49b). Since the silicon holder has multiple holes, a batch process with multiple fibers is also available.

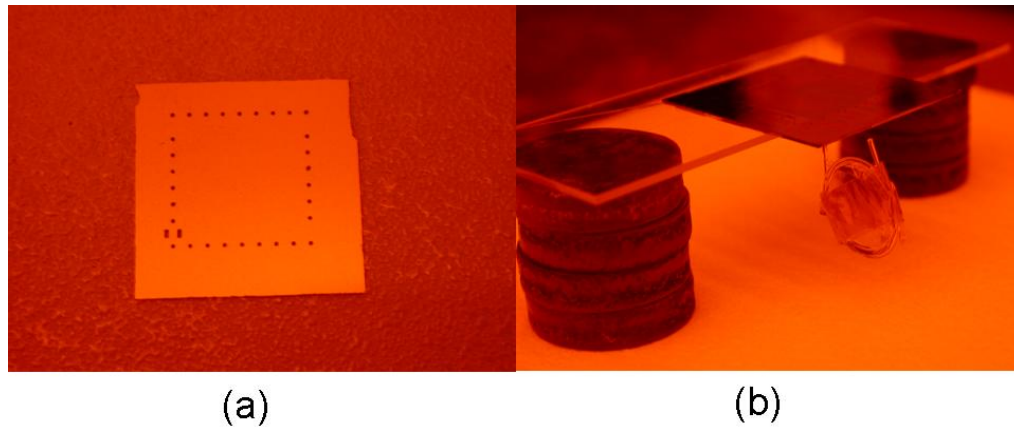


Figure 49. (a) Silicon substrate with micro-circular holes for fixing optical fibers (b) Image of silicon substrate with a rolled optical fiber.

4.3.3. Micro Patterning on the Optical Fiber

Since the photolithography process requires flat surfaces for accurate patterning, the optical fiber end was polished with silicon holder (Figure 50).

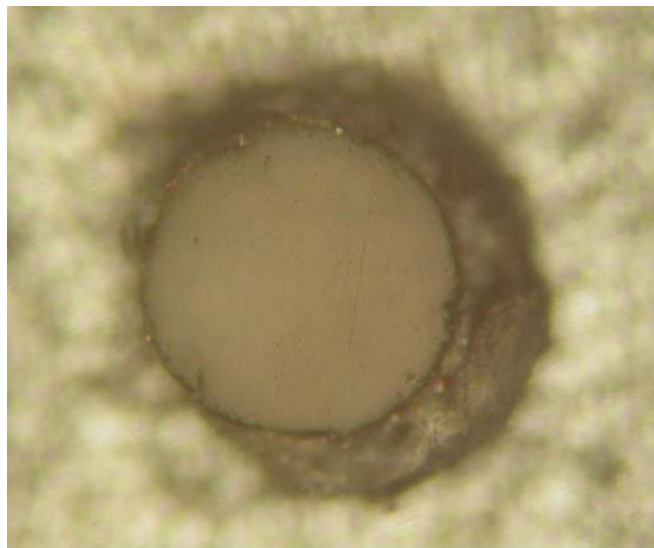


Figure 50. Optical image of the polished optical fiber with the silicon substrate

The silicon holder with optical fibers was spin coated with photoresist (AZ 5214) and baked in the oven. After UV exposure with a FZP patterned photomask, the photoresist was developed (Figure 51a). Next, Cr was deposited on the tips of fibers, and finally the photoresist was removed for lift-off of Cr. The Fresnel zone plate with Cr was successfully fabricated on the optical fiber tips as shown in Figure 51b.

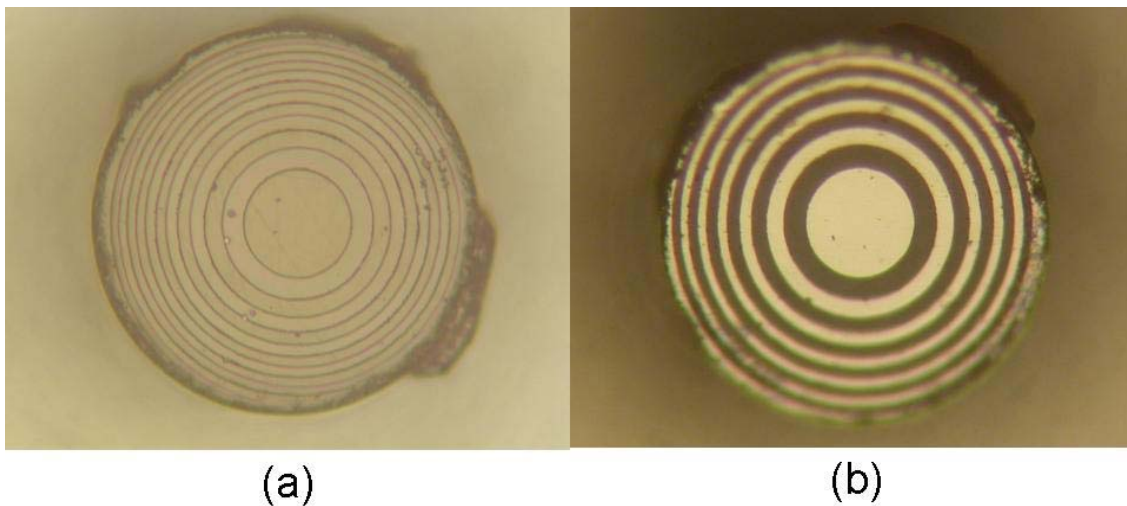


Figure 51. (a) Photoresist patterns of Fresnel zone plate on the optical fiber (b) Cr patterns after lift-off process

4.4. CONCLUSIONS

The novel embedding techniques were demonstrated for integration of microstructures with the CMOS VCO chip and the optical fiber. The SU-8 resist was chosen as the filling material for CMOS-chip embedding due to its simple processing

and excellent mechanical strength and chemical stability after curing. A novel post CMOS integration of the $2 \times 2 \text{ mm}^2$ VCO chip was demonstrated using the SU-8 embedding system. The vertical ring inductor was successfully fabricated and integrated on the CMOS VCO circuit chip, which have superior performance and very smaller substrate space occupancy.

In addition, a new embedding technique was demonstrated for the micro-fabrication on the optical fiber tips. In order to embed the optical fiber, silicon holders were fabricated by deep silicon etching with protecting layer. The optical fiber could be successfully embedded and fixed into the holes in the silicon holder. By using this embedding technique, the conventional photolithography could be used for micro patterning on the tips of fiber. Combined with conventional semiconductor processes, Fresnel lens (Fresnel zone plate) was monolithically integrated with the optical fiber tips. The novel embedding techniques developed in this work could be readily adapted to achieve efficient integration of large and complex components with tiny CMOS circuit chips or other advanced devices.

5. SUMMARY AND CONCLUSIONS

Integration of micro patterning techniques into volatile materials and advanced devices has demonstrated in this study. A novel micro-contact printing and shadow mask method were demonstrated for the patterning of volatile materials which cannot be patterned with the conventional photolithography. On the other hands, the novel embedding techniques were introduced to complement the conventional photolithography for integration of microstructures with the small substrates.

A flexible and versatile micro-contact printing process using a micromachined elastomeric PDMS stamp with two-dimensional arrays of pyramidal tips has been introduced. 2-dimensional array of pyramidal PDMS tips was molded from a bulk-etched single-crystalline silicon master. Variable-dot-size printing (from sub-micron to a few microns) was achieved by applying different contact pressure to induce variable mechanical deformation and thus contact area of PDMS tips. On the other hand, variable-density printing was also achieved in a “step-print” manner by using a mask contact aligner which has the up-and-down stage in z-direction for stamping and the x-y transitional stage for aligning each step stamping. As a result, 2-dimensional arrays of dot patterns with different dot size and density can be readily printed with a single stamp. This technique is expected to be useful in many nano- and biotechnology applications, including single cell and neuron studies.

A shadow mask technique with simple and accurate self-alignment system was demonstrated for the direct patterning of volatile materials. Pyramidal cavities have been made in both the shadow mask and substrate by anisotropic bulk etching of (100) silicon wafer. By involving 1mm-diameter steel balls in between the cavities of the shadow mask and the substrate, the accurate and stable self-alignment system could be demonstrated. In this alignment system, the gap between the shadow mask and the substrate could be controlled by the size of cavities or steel-balls. In order to create the patterns of organic semiconductor material, “pentacene”, which is volatile and cannot be patterned with photolithography, the shadow mask method was successfully integrated into the fabrication of OTFTs. The electrical properties of the pentacene OTFTs were characterized using a HP[®] 4155B semiconductor parameter analyzer.

Novel embedding techniques were demonstrated for enabling integration of complex microstructures with the small substrates. First, a polymer embedding technique was introduced for efficient post-CMOS integration of complex micromechanical components. Although several post-CMOS integration techniques have been introduced, the post integration of relatively large microstructures on the small individual CMOS chip has been a still challenging issue. In order to make post-CMOS processing capable on the small CMOS chip, the CMOS chip was embedded with polymer between two glass plates. By leveling the polymer surface with the CMOS chip, post CMOS process could be conducted with extended processing areas. As an application of the developed polymer embedding system, on-chip integration of a high Q vertical ring inductor was demonstrated onto a $2 \times 2 \mu\text{m}^2$ CMOS VCO chip. After the

VCO chip was embedded in SU-8, the vertical inductor was successfully integrated on the VCO chip by involving PDMA (Plastic deformation magnetic assembly). On the other hand, both numerical simulation and experimental characterization of the vertical inductor performance have been conducted. The vertical ring inductor manifests a stable inductance value and a high quality factor of 110 at the operation frequency of the VCO (5.8 GHz). In addition, a new embedding technique was demonstrated for integration of Fresnel lens on the optical fiber tips. The optical fiber could be embedded in the silicon holder which was fabricated by deep silicon etching with protecting layer. The embedding system enables the conventional photolithography to be applied for micro patterning on the tips of fiber. Finally, Fresnel lens (Fresnel zone plate) could be fabricated on the optical fiber tips. The novel embedding techniques developed in this study could be applied to other advanced devices for efficient integration of large and complex components.

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APPENDIX A

ANISOTROPIC SILICON WET ETCHING

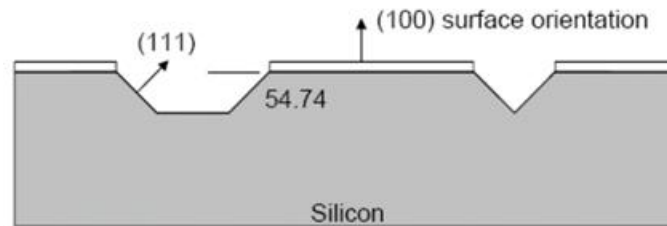


Figure 52. Schematics of anisotropically etched silicon substrate.

Table 4. Comparison of anisotropic silicon etchants [30].

Etchant		KOH (44%, 85°C)	TMAH (25%, 80°C)	EDP (115°C)
Etch rate ratio	(100) / (111)	300	37	20
	(110) / (111)	600	68	10
Etch rate (absolute)	(100)	1.4 $\mu\text{m}/\text{min}$	0.8 $\mu\text{m}/\text{min}$	1.25 $\mu\text{m}/\text{min}$
	(110)	2 $\mu\text{m}/\text{min}$	1.4 $\mu\text{m}/\text{min}$	> 0.6 $\mu\text{m}/\text{min}$
	Si_3N_4	< 1 $\text{\AA}/\text{min}$	< 1 $\text{\AA}/\text{min}$	< 1 $\text{\AA}/\text{min}$
	SiO_2	45 nm/min	2 $\text{\AA}/\text{min}$	2 $\text{\AA}/\text{min}$
	B doped Si ($>10^{20}\text{cm}^{-3}$)	70 nm/min	3 nm/min	5 nm/min
Advantage		<ul style="list-style-type: none"> Strongly anisotropic 	<ul style="list-style-type: none"> Neither toxic nor harmful Metal ion free 	<ul style="list-style-type: none"> Metal ion free Metallic hard masks possible
Disadvantage		<ul style="list-style-type: none"> Metal ion containing 	<ul style="list-style-type: none"> Weak anisotropy 	<ul style="list-style-type: none"> Anisotropy toxic

Remarks

- If EDP reacts with oxygen, the liquid turns to a red-brown color, and it loses its useful properties
- Higher concentration of TMAH \rightarrow lower etch rate, lower etch ratio (100/111), less roughness

APPENDIX B

LIFT-OFF PROCESS

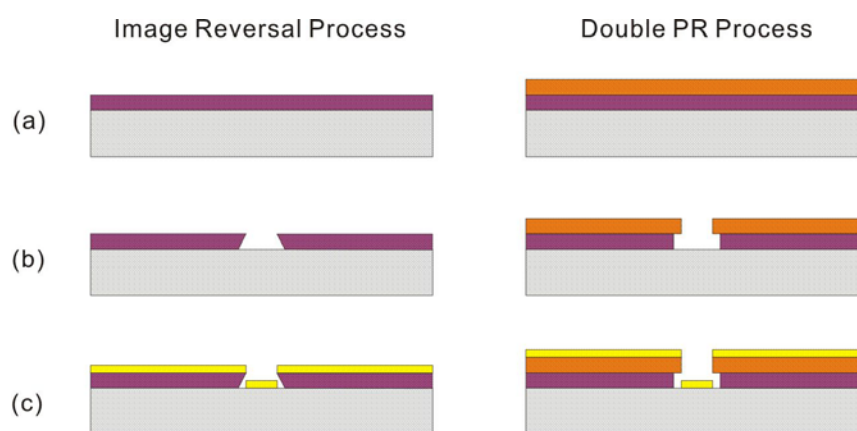


Figure 53 Schematic diagrams of Lift-off process; image reversal and double PR processes (a) Spin coating of PR, (b) Patterning PR with image reversal or double PR processes, (c) Deposition and lift-off.

Image Reversal Process	Double PR Process
1. Spin HMDS (3000rpm, 40sec)	1. Spin HMDS (3000rpm, 40sec)
2. Spin AZ 5214 (2000rpm, 40sec)	2. Spin AZ 4330 (6000rpm, 40sec)
3. Baking on hot plate at 110°C for 2min	3. Baking on hot plate at 110°C for 1min
4. UV exposure at 15mW/cm ² for 6sec	4. Flat UV exposure (w/o photomask) at 15mW/cm ² for 30sec
5. Post baking on hot plate at 110°C for 3min	5. Spin AZ 5214 (4000rpm, 30sec) w/o increasing speed step
6. Flat UV exposure(w/o photomask) at 15mW/cm ² for 30sec	6. Baking on hot plate at 110°C for 1min
7. Developing in AZ 400K (1:1 diluted) for 2min	7. UV exposure at 15mW/cm ² for 6sec
	8. Developing in AZ 400K (1:1) for 2min

APPENDIX C

ELECTROPLATING SETUP

- **Cu bath** : CuSO_4 (125g) + DI water (1L) + HSO_4 (98g)

Etchant for oxidized Cu layer : HSO_4 (100mL) + DI water (900mL)

- **NiFe bath**

1) Fill large beaker with DI water (1L)

2) Add followings to DI water (pH ~ 3.8)

$\text{NiCl}_2 \cdot 6\text{H}_2\text{O}$ (39g), $\text{NiSO}_4 \cdot 6\text{H}_2\text{O}$ (16.3g), H_3BO_3 (25g), Sodium Saccharin (1.5g), NaCl (25g)

3) Adjust pH of above solution to 2.6~2.7 by adding several (~40) drops of diluted HCl

(1·HCl : 5·DI water) → To prevent dissolution of $\text{FeSO}_4 \cdot 7\text{H}_2\text{O}$

4) Put 1.4g $\text{FeSO}_4 \cdot 7\text{H}_2\text{O}$ (pH → 2.65)

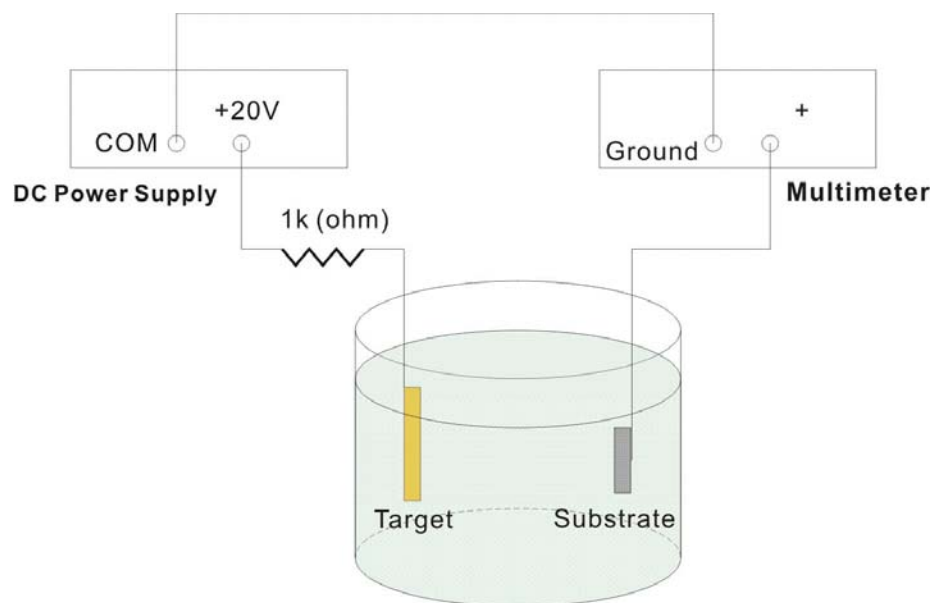


Figure 54. Schematic diagram of electroplating setup.

APPENDIX D
ONE-PORT S-PARAMETERS ANALYSIS

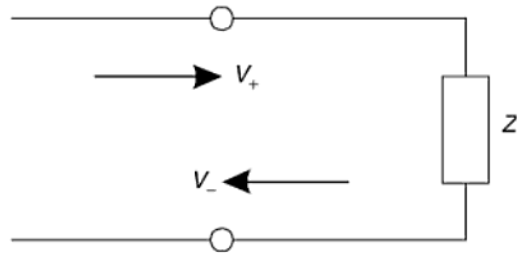


Figure 55. Transmission line terminated in a mismatched load [59].

If the transmission line is terminated by a load Z (Figure 55), which is not perfectly matched with the transmission line, then some of the incident waves will be reflected back from the load. In terms of voltage and current along the line, at a point z ,

$$V(z) = V_+ e^{-j\beta z} + V_- e^{+j\beta z} \dots\dots\dots (1)$$

$$I(z) = I_+ e^{-j\beta z} - I_- e^{+j\beta z} \dots\dots\dots (2)$$

where $Z_0 = \frac{V_+}{I_+} = \frac{V_-}{I_-}$

At $z = 0$, the reflection coefficient (s) can be defined by

$$s = \frac{V_-}{V_+} \dots\dots\dots (3)$$

From Ohm's law,

$$Z = \frac{V}{I} \dots\dots\dots (4)$$

Substituting (1) and (2) into (4) gives the well-known relationship between the reflection coefficient of the termination and its impedance

$$Z = Z_0 \frac{V_+ + V_-}{V_+ - V_-} = Z_0 \frac{1 + s}{1 - s} \dots\dots\dots (5)$$

Here, the reflection coefficient is a complex number, which can be expressed by

$$s = s_R + i \cdot s_I \dots\dots\dots (6)$$

Substituting (6) into (5) gives the complex form of the impedance

$$\begin{aligned} Z &= Z_0 \frac{1 + s_R + i \cdot s_I}{1 - s_R - i \cdot s_I} = Z_0 \frac{(1 + s_R + i \cdot s_I)(1 - s_R + i \cdot s_I)}{(1 - s_R)^2 + s_I^2} \\ &= Z_0 \frac{(1 + i \cdot s_I)^2 - s_R^2}{(1 - s_R)^2 + s_I^2} = Z_0 \frac{1 - s_R^2 - s_I^2 + 2i \cdot s_I}{(1 - s_R)^2 + s_I^2} \end{aligned}$$

Therefore, the impedance can be divided into real and imaginary parts as follows,

$$Z = Z_R + i \cdot Z_I = Z_0 \frac{1 - s_R^2 - s_I^2}{(1 - s_R)^2 + s_I^2} + i \cdot Z_0 \frac{2s_I}{(1 - s_R)^2 + s_I^2}$$

Since $Z = R + i\omega L$, the inductance (L) and the quality factor (Q) can be determined by

$$\begin{aligned} L &= \frac{Z_0}{2\pi f} \cdot \frac{2s_I}{(1 - s_R)^2 + s_I^2} \\ Q &= \frac{Z_I}{Z_R} = \frac{\omega L}{R} = \frac{2s_I}{1 - s_R^2 - s_I^2} \end{aligned}$$

VITA

Jung Moo Hong was born in Seoul, South Korea. He received his Bachelor of Science and Master of Science degrees in electronic materials and devices engineering at Inha University, Incheon, South Korea in 2000 and 2002, respectively. Before joining the doctoral program, he worked as a research scientist in the photonic research center at Korea Institute of Science and Technology, Seoul, South Korea. He started his doctoral program in electrical and computer engineering at Texas A&M University in September 2004 and received his Doctor of Philosophy degree in May 2009. His research interests include integration of micro-patterning techniques into volatile functional materials and advanced devices.

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The chair, Dr. Jun Zou, is a reference and he will know where to reach Mr. Hong.

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