YIELD LEARNING WITH LINE WIDTH, SAMPLE SIZE AND BRIDGE RESISTANCE VARIATION

A Thesis

by

WAJID HUSSAIN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 1997

Major Subject: Electrical Engineering

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ABSTRACT

Yield Learning with Line Width, Sample Size and Bridge Resistance Variation.

(December 1997)

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Rapid failure analysis and continuous monitoring of the fabrication line are required in order to maximize the slope of the semiconductor manufacturing yield ramp. Metrology costs are the fastest rising expense occurring in the fabrication line. In addition, many of the defects can only be detected using electrical methods. Hence the use of simulation-based models for defect diagnosis is on the increase. We have used an already available methodology of defect-fault dictionary building and have observed the effects of certain noise sources such as line width variation, sample size and bridge resistance on yield learning, and determined how to account for them.

In this research we will show that since line width variation is not random on a few wafer samples, its effect on defect Pareto predictions is profound and must be corrected. We will show that a linear model is sufficient to correct for the sensitivity of defect density to line width variation and shall also confirm this experimentally.

We have examined the effect of various defect sample sizes on the resolution of the defect-fault dictionary and hence on the diagnosibility. We will show that the dictionary construction costs can be reduced by using relatively small sample sizes without a significant reduction in Pareto accuracy. We shall also show that a distribution of bridge resistance does not effect the Pareto accuracy.

Our observations and correction model allow us to make accurate defect Pareto predictions in the presence of these noise sources.

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I. INTRODUCTION

An important element of a semiconductor product life cycle and time-to-market is the yield learning period. As shown in the Figure 1, yields are low in the development phase, then grow quickly and stabilize in the production phase. This growth of yields should be quick in order to maximize profits and these yields should be maintained once achieved.

Rapid yield learning is the set of those activities which are aimed at increasing the slope of the yield ramp and maintenance of high yields. Yield learning can be successfully performed if it is accompanied by **yield monitoring** [1,2,3,4,5] during all phases of VLSI manufacturing. Whenever any variation of defect density is observed, then an appropriate corrective procedure should be applied at that particular phase of manufacturing.

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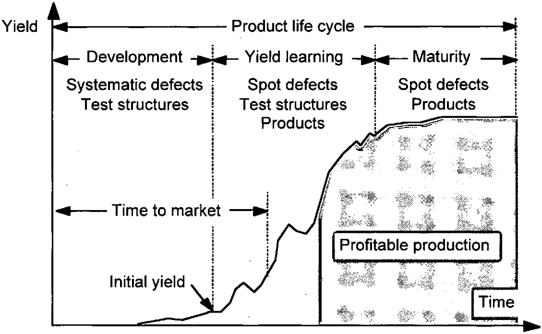

Figure 1: Typical yield learning curve

A. Yield Loss

It is not possible to obtain 100% yield even when all the processing parameters are within the desired range wherein the circuit would perform satisfactorily. The reason for this yield loss is a set of yield detractors. These detractors can be local [6,7,8,9] or global. Local defects include spot defects [6,10] and oxide pinholes and they affect the topology of the circuit and are dominant in causing functional yield loss. Hence local defects are called catastrophic defects.

Global detractors influence all the IC elements across the die in a similar way and are called parametric, global and systematic defects. We shall assume that local defects primarily cause functional failures and global defects cause parametric faults even though there is some interaction between the two types of yield detractors. However it is assumed in this research that these dependencies are negligible and parametric defects are detected in the rudimentary stages of manufacture and corrected [11].

From Figure 1 we see that systematic defects are the primary cause of yield loss in the development phase, whereas spot defects are dominant in the yield learning and volume production phases. Yield loss due to processing issues should be addressed in terms of efficient process monitoring, thus increasing the slope of the yield ramp and maintaining high yields once reached.

B. Research Goals

Previous research [1] has shown that indirect measurement of defect densities, can be performed using production functional testing data. This scheme is based on previous work on functional yield modeling with the DEFAM and VLASIC simulators [11,12,13]. These simulators help in yield learning by predicting the circuit fault probabilities and the functional yield on the basis of certain defect models, thus relating the yield loss to certain process phases.

Functional yield monitoring is achieved by using the simulators to build a probability map between defects and test vector failures [1]. Fault simulation is performed using the fault list generated by the defect simulators with the production functional test set. This helps us to obtain the frequencies of possible patterns of circuit failures. Observed failure patterns along with the defect to test failure probability matrix are used to estimate different types of defect densities. This provides information about the catastrophic defects during the yield ramp, and volume production thereby allowing more efficient yield enhancement and maintenance.

In this research we shall show that for different types of circuits and technology considered a typical range of line width variation would have a significant influence on the predicted defect Paretos and therefore must be filtered out. The effect of simultaneous multiple line width variation on predicted defect density is also examined.

We shall analyze whether we can reduce the dictionary construction cost by using a relatively small defect sample sizes. The effects of various sample sizes on the defect to fault dictionary resolution and the diagnosibility of circuits are explored.

Bridging failures are the most common faults present in mature CMOS integrated processes. Hence the detection of faults introduced by bridging defects is required in order to perform an acceptable IC test. We shall examine whether bridge resistance affects the Pareto accuracy.

Our general approach to these problems will be to run some initial experiments, postulate an answer, confirm with experiments, and generalize to all designs.

C. Thesis Outline

The rest of the thesis is organized as follows. The background section II briefly describes the defect, fault simulations and process monitored oriented testing. Section III introduces the overall defect monitoring methodology used in our research and the application of VLASIC and IRSIM simulators with respect to this methodology is explained. Section IV gives in detail all the steps involved in this experimentation (details of defect and fault simulation and Pareto extraction) plus the procedure we have adopted to perform yield learning with variations in line width, sample size and bridge resistance. Section V describes the experimental results and section VI concludes.

II. BACKGROUND

Realistic defect extraction and simulation [2,6,7,10,11,12,13] employ techniques which establish relationship between disturbance manifestation and its origin and physical characteristics. In the ensuing sections we will briefly review theories and concepts relating to defect and fault simulation, process monitoring oriented testing and direct measurement of yield loss.

A. Defect Simulation

Analytical approaches have been developed in the past to predict the number of circuit faults on any chip. However these analytical models found limited use in the VLSI industry because of the fact that they are unable to accurately model the relationship between physical causes of the yield loss and the resultant circuit failures. The majority of the models [11,14,15] depend on the chip size and the defect density distributions, but not on the layout. To accurately model yield loss and thereby estimate the manufacturability of an IC design, several software tools for defect and yield simulation have been developed [11,12,13,16,17,18,19,20,21,23,24].

Prior to chip fabrication, yield loss is predicted by automatic extraction of circuit faults caused by catastrophic defects. VLASIC employs a **Monte Carlo** method of generating, placing and analyzing defects on a chip layout. Defect random number generators are used to create and place defects on the layout with the desired diameter and spatial distribution.

VLASIC models defects resulting from extra or missing material as circles. A $1/x^3$ distribution [21] is used for defect size variation for extra and missing material defects. Defects are placed uniformly within a die. After placement of defects is accomplished, VLASIC performs fault analysis to determine if a defect has caused any circuit faults [11].

B. Fault Simulation

IRSIM [25] is a switch-level fault simulator which is used in this research to observe the effect of defects on given circuits. IRSIM uses a resistive switch model to approximate timing and voltage division, and incremental simulation to minimize the effort to resimulate in the presence of small circuit changes. The switch model assumes the switch is in the X state when the control voltage V is $V_L < V < V_H$. Therefore resistive bridges can generate X values.

C. Process Monitoring Oriented Testing

The idea of using the relation between the disturbance manifestation and the physical origin of the defects has been extensively used for process monitoring using SRAM cells as test structures [2,18,26,27]. A framework for the systematic analysis of yield losses has been suggested in [2]. The classification is hierarchical in the form of a tree wherein every node represents a group of reasons having certain similar characteristics, the ensuing levels have these categories of reasons further divided into sub categories. The vital elements of this classification are global and local disturbances. Examples for this kind of yield diagnosis framework are available in [28]. A process monitoring oriented testing scheme based on this framework has been proposed in [29].

A defect localization methodology has been suggested in [30]. The set of defects targeted for localization are limited to include only those defects that cause unique similar node faults. It has also been shown that a small number of randomly selected tests can provide good diagnostic resolution among the two node bridging defects. The levels of diagnostic resolution are greatly improved by observing abnormal IDDQ currents during test [31]. The efficiency and quality of SRAM based process monitoring techniques was evaluated in [27,32].

III. METHODOLOGY

The failure patterns of production test vectors can be utilized to predict the reason for failure of chips at the functional tester. Figure 2 shows such a defect monitoring methodology [1]. Provided the test vector, circuit structure details and layout are known, defect statistics can be estimated with the help of a **probability matrix**. The probability of failure (POF) matrix helps us to map from test failure to defects by relating defects to faults and faults to test failures. Failure patterns are also collected from the production functional tests and the frequency of each pattern is counted. The individual defect densities can be estimated by $d = P^{-1} \cdot t$, where P is the POF matrix, t is the failure pattern frequencies observed from the production test and d is defect densities.

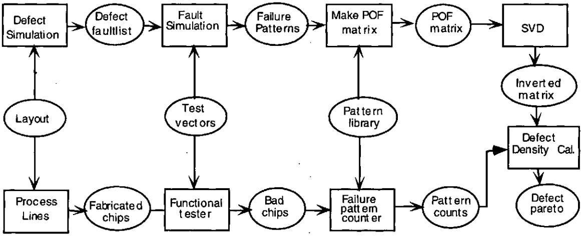

Figure 2 : Defect monitoring methodology

The upper portion of Figure 2 to the POF matrix step indicates the mapping procedure from defects to faults and faults to test failures. In our research the mapping between defects to faults was done using the defect simulator VLASIC [16]. Given a circuit layout and the defect types the simulator generates a fault list with frequencies proportional to the critical areas [11]. A switch level simulator IRSIM [25] for voltage based testing is used to map from faults to test failures.

As every fault has a corresponding output pattern, we can classify and combine the results from fault simulation. Ideally, test failure patterns corresponding to different faults should be distinguishable but in reality this is not the case. Therefore the testing method may need to be modified in order to obtain a set of failure patterns with good diagnosibility. We can satisfy this need by observing the test procedure until certain stopping criteria are met. The terminology for describing the stopping criteria are shown in Table 1, with examples in Table 2.

We have used stopping criteria 1n, 1p, 2n and 2p in our research. The 1n criteria states that the failure pattern is the number of the first failed vector. The 2n criteria refers to a failure pattern composed of the first two failed test vector numbers. The 1p method refers to a failure pattern composed of the number of the failed vector plus the output pattern.

Previous research [1] shows relatively little benefit to using more complex stopping criteria, and in particular, recording more failing vectors is more effective than Iddq testing. Table 3 shows the results obtained by applying three types of stopping criteria to the voltage tests for benchmark circuit c17 (1n, 1p and 2n). The more complex criteria cause the failure patterns to split apart, resulting in better diagnosability. The column under the heading counts gives the total number of defects causing a particular failure pattern.

A POF matrix can be generated by counting the frequency of each pattern in the fault simulations. Figure 3 illustrates a sample POF matrix with the 1n criteria applied for c17. The first row of the POF matrix is for the type of defects and the second gives us the number of each type of defect placed on the chip during defect simulation (100,000 of each type induced for this example). The types of defects [12] that we have used in this research are extra metal1 (POSMF), extra metal2 (POSMS), extra poly (POSPG) and poly-metal1, metal1-metal2 oxide pinholes (PIN1 and PIN2). The last two columns of the matrix refer to the count of a failure pattern and its pattern as given in the example. Each element of the matrix refers to the probability that a defect of that type causes a corresponding failure pattern. The diagnosibility of the POF matrix increases as the number of unique failure patterns increases.

POSMF	POSPG	POSMS	PIN1	PIN2	COUNT	ID
100,000	100,000	100,000	100,000	100,000		
0.00876	0.01240	0.00782	0.00607	0.02042	5,547	1:
0.00267	0.00683	0.00121	0.00513	0.00953	2.537	2:
0.00073	0.00012	0.00000	0.00000	0.00147	232	3:
0.00286	0.00280	0.00252	0.00045	0.00251	1,114	4:
0.00099	0.00089	0.00147	0.00075	0.00645	1,055	5:
0.00004	0.00035	0.00014	0.00000	0.00148	201	6:

Figure 3: POF matrix with criterion 1n.

When the frequency of each pattern is obtained from the production test, the defect statistics of the fabrication line are estimated in the form of a Pareto chart [33]. The procedure for analysis is shown in Figure 2.

The individual defect densities can be estimated by $d = P^{-1} \cdot t$ where P is the POF matrix, t is the patterns observed from the production testing and d is the defect density.

Figure 4 shows a Pareto chart in which defect types are classified and plotted in descending order of their defect densities. This Pareto shows the predicted defect density E(x) (defects/cm^2), and upper and lower confidence limits (CL).

Certain failure patterns can be caused by more than one type of defect, so there would be no direct way to distinguish between defect types. Usually the POF matrices do not have an inverse, because the number of failure patterns greatly exceeds the number of defect types. Therefore it is necessary to use singular value decomposition (SVD) methods [34,35] in order to find the least square fit for the POF inverse.

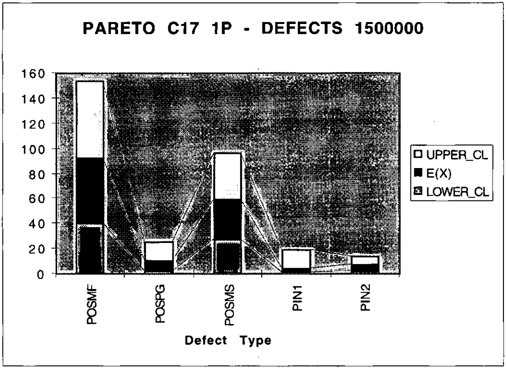

Figure 4 : Pareto chart

Table 1: Stopping criteria terminology

ID	Criteria
prefix-number	Stop at the number-th test vector.
n	Record the failing test vector number.
p	Record the failing test number and output values.
z	Perform an IDDQ current testing at final failing test. Record the failing test number, output pattern and IDDQ result.
c	Perform an IDDQ current testing at every failing test. Record the failing test number, output pattern and IDDQ result.
x, h, l, r	Interpret each intermediate voltage value as an X, logical high, logical low or random value (default: X).
m, o, u	Interpret each oscillating output as a special mark, value at specific time or random value (default: special mark).
postfix-number	Categorize faulty IDDQ current values in number different levels.

Table 2: Examples of stopping criteria

Sample	Effect
1 n	Stop at the first failure. Record the test number.
1 p	Stop at the first failure. Record the test number and the output.
1 z 3	Stop at the first failure. Perform an IDDQ current testing at the failing test. Record the test number, output and IDDQ test. Keep intermediate voltages as X. Categorize IDDQ current values in 3 different levels.
k n	Run test vectors until k-th failure. Record all k failing test numbers.
k p	Run test vectors until k-th failure. Record all failing k test numbers and output values. Keep intermediate voltages as X.
k z 5	Run test vectors until k-th failure. Perform an IDDQ current testing at each failing test. Record all failing k test numbers and outputs and the IDDQ result in 5 different levels. Keep intermediate voltages as X.
all n	Run all test vectors. Record all failing test numbers.
all p	Run all test vectors. Record all failing test numbers and output values. Keep intermediate voltages as X.

Table 3: Failure patterns with different criteria

Criterion 1n		Criterion 2n		Criterion 1p	
Pattern	**Count**	**Pattern**	**Count**	**Pattern**	**Count**
1:	5,547	1:2	3,980	1-00:	2,115
		1:3	883	1-10:	11
		1:4	597	1-11:	1.915
		1:5	1	1-0X:	395
		1:6	86	1-1X:	1
				1-X1:	1,031
				1-XX:	79
2:	2,537	2:	153	2-01:	1009
		2:3:	925	2-11:	608
		2:4:	798	2-0X:	378
		2:5:	639	2-XX:	542
		2:6:	22		
3:	232	3:4:	232	3-01:	232
4:	1,114	4:	180	4-00:	682
		4:5:	432	4-11:	1
		4:6:	502	4-XX:	431
5:	1,055	5:	854	5-00:	596
		5:6:	201	5-01:	201
				5-10:	258
6:	201	6:	201	6-11:	201

IV. EXPERIMENTAL DETAIL

The detailed procedures for the different experiments carried out in this research are explained in this chapter. The following sections describe the benchmark circuits, defect statistics, and tools with algorithms. We then decide the procedure for considering line width variation, defect sample size, and bridging resistance

A. Benchmarks

Table 4 gives us gives us the details of the benchmarks such as layouts, test vectors . As shown in the table we have considered MCNC CMOS standard cell layouts of the ISCAS 85 benchmarks [36]. In order to maintain similar testing and process environments the test vectors that are used in production testing have been applied to the simulation. ATALANTA [37] an automatic test pattern generator for combinational circuits for stuck-at faults is used in our experiments. Other test vectors can also be supplied so long as they have sufficient fault coverage. Certain faults cannot be detected by the stuck at fault test set even in the gate level circuits, however most of two node bridging faults can be detected by these test sets if combined with IDDQ testing. A test set that gives a satisfactory stuck-at fault coverage can give good diagnostic resolution when combined with IDDQ testing [38], hence a production test set that is developed to optimize the stuck-at fault coverage can be used itself as a diagnostic test set.

Table 4 : Benchmarks

Circuit	**c17**	**c432**
Layout area (cm^2)	0.00015928	0.00600288
No. of primary inputs	5	36
No. of primary outputs	2	7
No. of nodes	20	402
No. of transistors	26	728
No. of test vectors	6	56

B. VLASIC (Defect Simulator)

Five different types of several million defects are introduced into the layouts. Figure 5 shows the flowchart for the defect simulations and the label mapping [1].

A layout when given will be read into the MAGIC layout editor to extract into a CIF format for ENTICE and VLASIC and into EXT format for IRSIM. The CIF layout is fed into the ENTICE circuit extractor, so that all the net geometry is extracted containing all the net numbers.

The ENTICE file is fed into VLASIC to generate a fault list. VLASIC determines the probability that each defect type causes a fault. We assume that defects within a cell will have a uniform spatial distribution and do not interfere with one another (all defects being sampled equally).

We must map each electrical node in the circuit between defect and fault simulations. The mapping is done by giving the node labels from the circuit extractors universal labels. Figure 5 shows that the node labels from IRSIM and VLASIC are compared and a mapping table is created. This table is then utilized to convert each label in the IRSIM simulation and command files, and the VLASIC defect to fault lists. The next step is to supply the defect to fault list to the fault simulation phase.

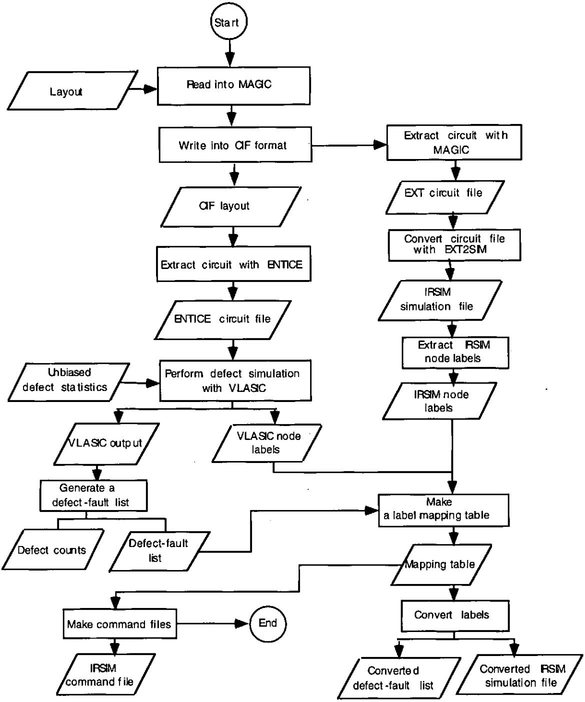

Figure 5 : Defect simulation and label mapping [1]

C. IRSIM (Fault Simulator)

Figure 6 shows the procedure for conducting the fault simulations for each fault in the defect to fault list for a given stopping criterion [1]. We have considered bridging faults since they are more common and easier to simulate. A Similar methodology can also be applied to other fault models. The circuit is modified corresponding to the characteristics of each bridging fault as shown in the defect to fault list generated by the defect simulator. Then simulation is carried out with a set of test vectors to determine the failure patterns for a particular fault type with a given stopping criterion. Consider the case where the 1n stopping criteria is applied. In this case the output is checked serially until we get the first failing vector. When the first failing vector is detected, the test vector ID is recorded. In the worst case the testing will continue until all the vectors in the test set are exhausted and that fault would be marked as undetected.

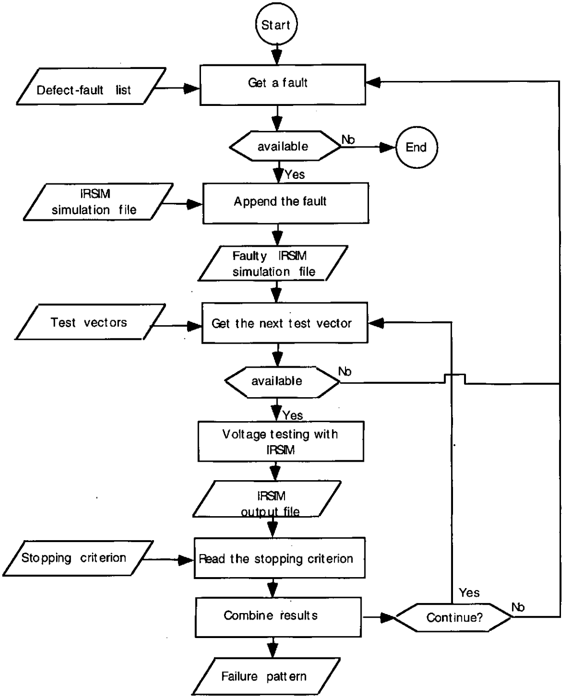

Figure 6: Fault simulation flow chart [1]

D. Intermediate Voltage Values

Our failure pattern dictionary could consist of unrealistic failure patterns due to inaccurate fault simulations [1]. An 'X' value is used to represent intermediate voltage values on a primary output in voltage testing. However the production test results will not contain X values.

We could deal with these 'X' values in the following ways: 1) match them to a close pattern or 2) discard them or 3) convert them to a new pattern. When the simulator observes oscillations at the output then the output should be either categorized as undetected or detected (with a particular output value) at a certain time interval. In our research we will consider these 'X' values as new patterns.

E. Calculation of Defect Density

Figure 7 shows the flowchart for the defect density calculation [1]. When the stopping criterion is specified the test results from the fault simulations are categorized to obtain the failure patterns and the POF matrix. The same criteria are also applied to the production testing to obtain similar failure patterns. When a failure pattern from the production testing matches a pattern in the dictionary, its count is recorded to produce a count of failure patterns.

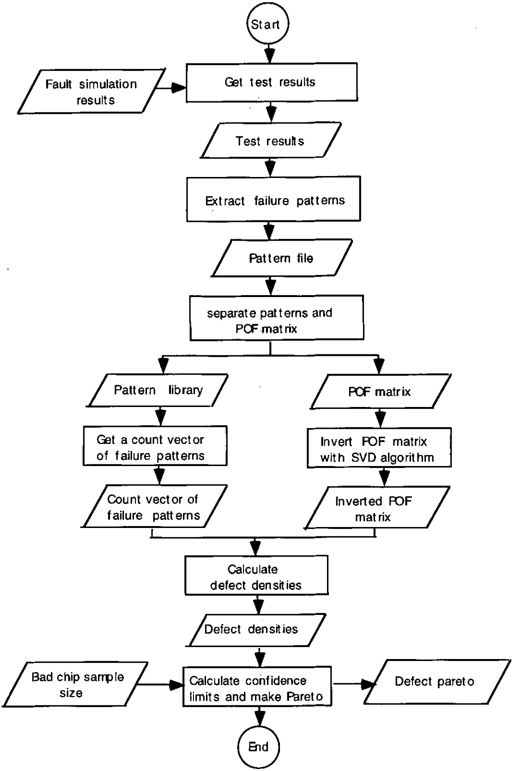

Figure 7 : Defect density calculation [1]

If an unmodeled pattern occurs it is discarded or it is matched to a closer pattern or it is converted to a new pattern. This count vector which is obtained by matching the results from the production test and simulation is multiplied by the inverted POF matrix (obtained from simulation), to give us the defect density Pareto .

We use the same notation as [1].

Sets are denoted by capital letters, matrices and row vectors are shown in bold face capital letters, column vectors are represented by bold face lower case letters, and scalars correspond to lower case letters. The transpose of a vector v is denoted $\mathbf{v}^{-1}$. Also we assume that there are m different defect types and k different failure patterns. Thus M = {i : i = 1,2,...,m} represents the set of defect types and K = {j : j = 1,2,...,k} the set of failure patterns.

$\mathbf{Pareto} = [\mathbf{Pareto}_1, \mathbf{Pareto}_2, \ldots, \mathbf{Pareto}_i, \ldots, \mathbf{Pareto}_m]$,

Where,

$\text{Pareto}_i = [\min\{d_{ij} : d_{ij} \in \mathbf{d_j}, \mathbf{i} \in M, j \in K\}, d_{i0}, \max\{ d_{ij} : d_{ij} \in \mathbf{d_j}, \mathbf{i} \in M, j \in K\}]$

$d_j = P^{-1}.q_{j,}$

$d_0 = P^{-1}.q_j,$

$q_j = [p_1, p_2, \ldots, p_j \pm c_j, \ldots, p_k]^T,$

$q_0 = [p_1, p_2, \ldots, p_{j, \ldots,} p_k]^T,$

$c_j = z_{1-\alpha/2}.\sqrt{}(p_j(1- p_j)/n)$,

$z_{1-\alpha/2}$ = the $(1-\alpha/2)$ quantile of an unit normal variate,

α = the significance level,

n = the number of bad chips sampled,

$p_j = r_j / \Sigma_j r_j$,

r_j = roundoff(t_j) ,

t = the count vector of the failure patterns from $t = P \cdot d$,

P = the POF matrix,

P^{-1} = the inverted POF matrix,

d = the defect count vector.

When a random count vector of defect densities **d** with m different types and a POF matrix P are given, a sample of failure pattern counts t with k different types is generated. After calculating the 95% confidence interval of each failure pattern t_j, an estimate of defect densities d_j is computed by multiplying the inverted POF matrix P^{-1} and the pattern count vector q using the upper or lower limits, $+c_j$ and $-c_j$. The worst values from k different estimations of defect densities are selected as the confidence limits of the calculated values. This calculation gives a Pareto of defect densities, upper and lower confidence limits. Note that since each confidence limit is computed separately, it is conservative.

F. Line Width Variation

Given below in bold letters is the procedure for line width, sample size and bridge resistance variation and subsequent steps of experimentation and result collection. As we can see the defect monitoring methodology discussed in chapter III is presented here with some modifications. The details of defect and fault simulations can be obtained from the Figures 5 and 6 respectively. Prior to defect simulation the defect statistics and size are altered so that the desired number of defects are placed on the chip and required line widths are obtained.

The defect size is biased up to simulate larger line width and down to simulate smaller line width. The line widths are varied by up to 30% of the minimum line widths as specified by the design rules (this is 300 centimicrons for metal1 and metal2 and 200 centimicrons for poly). The variation in line widths that we have applied to our layouts are +/- 80 centimicrons. These variations are applied to the metal1, metal2 and poly layers. Note that besides changing the probability of intralayer shorts line width variation will cause the POF to vary for pinholes, interlayer shorts.

The following is the procedure for experiments conducted for the line width variation case:

1. **Vary the line width of any one layer by +/- 80 centimicrons in steps of 4 centimicrons.**
2. **Perform defect and fault simulations for each step with suitable sample size, default bridge resistance setting (100Ω) and 1n, 1p, 2n and 2p stopping criteria.**
3. **Draw plots with the 40 data points obtained for each layer, for each criteria.**
4. **Apply linear regression to get a best fit curve for the plots drawn. Hence this is a linear model.**
5. **Analytical explanation and theory.**
6. **From the analytical study we find that cross terms are negligible, so an additive linear model is adequate.**
7. **Confirm this by conducting experiments with simultaneous variation of line widths for more than one layer at a time.**

G. Defect Sample Size

In the earlier experiments concerned with line width variation we could select a suitable defect sample size which would be one that would minimize the affect of sampling noise in the plots obtained and give us a linear model. Defect sample sizes affect the overall Pareto accuracy. A larger sample size would imply a decrease in the mean error, and variance in the POF matrix entries.

The following is the procedure for the defect sample size estimation:

1. **Conduct experiments with different defect sample sizes for a particular circuit at nominal line width and bridge resistance .**
2. **Obtain the Paretos and study the affect of defect sample size variation on mean error and confidence interval length.**
3. **Observe that an increase in defect sample size would imply a decrease in the confidence interval, mean error and variance in the POF matrix entries.**
4. **Observe that beyond a particular defect sample size the number of test failures that could be added to the POF matrix decreases significantly.**
5. **Perform an analytical study of results obtained.**

6. **We can say that if experiments were conducted with a defect sample size X then with a sample size Y (where $Y > X$) the number of failures added to the POF matrix would help us to estimate a suitable defect sample size.**
7. **The suitable defect sample size would be one that would help diagnose most of the bad chips, with the confidence interval due to the finite number of bad chips greater than the interval due to defect sampling noise.**

H. Bridge Resistance

Bridge resistance variation is random within a wafer. Low resistances will cause test failure pattern 1. High resistances will not cause a test failure. It is sometimes possible for intermediate resistances to cause other test failure patterns, due to different gate logical thresholds. These patterns may alias to another defect type, reducing the effectiveness of the POF matrix, and resulting in larger confidence intervals than predicted for a POF matrix built with only low-resistance bridging faults.

The following is the procedure for analyzing bridge resistance variation and its effect:

1. **Postulate that a distribution in bridging resistance has little effect on Pareto accuracy. Explain why this is so using a theoretical analysis.**
2. **Run simulations with a distribution of bridge resistance to confirm this.**
3. **Any variation if observed is explained to be due to the Monte Carlo nature of simulations only and not due to bridge resistance distribution.**

V. EXPERIMENTAL RESULTS

The procedures described in the earlier chapters are carried out and results are obtained at the different stages of experimentation. A benchmark layout was first input to the circuit extractor which extracts the connectivity of the circuit and labels all the geometry, then the resulting file was given to VLASIC (defect simulator). As many as 1 defect/μm^2 were introduced into the layout. Whenever any circuit fault occurred, the defect simulator extracted it and classified it according to the fault type. Thus a defect to fault list was obtained. Then fault simulations were carried on to get a relationship between circuit faults and failure patterns. We have limited ourselves to the consideration of bridging faults in this research. Voltage testing was applied for the detection of these faults. A probability matrix was generated by combining the relationship between defects to faults, faults to failure patterns and a given stopping criteria. Then a Pareto showing the defect densities was obtained by multiplying the inverse of the POF matrix and the count vector. Table 5 shows the number of faults generated for the defect simulation (with the specified number of defects) for the benchmark circuits.

Table 5 : Fault statistics following defect simulation

Layout name	**c17**			**c432**		
# Total defects induced	79,640			3,001,440		
% Killer defects	2.86%			3.65%		
# Total faults generated	2274	507	-	109644	20691	-
# Bridging faults	2060	314	111	100236	12909	5488
# Open faults	129	118	-	5010	4342	-
# new gate device faults	85	75	-	4398	3440	-
CPU time for simulation	0 : 00 : 21			0 : 27 : 11		

The three columns in Table 5 correspond respectively to the total number of killer defects which landed in the critical area for each defect type in the layout given and caused a circuit fault, the number of unique faults which caused an electrical fault in the same set of two or more nodes.

For the case of line width variation for metal1, metal2 and poly the defect size is biased up to simulate larger line width and down to simulate smaller line width. the line widths are varied by upto 30% of the minimum line widths. Then defect and fault simulations were carried out followed by generation of Paretos for different defect types. Simulations were carried out with varying defect sample sizes to overcome the noise problem.

The POF matrices obtained for the simulations carried out with different defect sample sizes were analyzed. A distribution of bridge resistance was applied to the benchmarks and the effects of this on POF matrices and Paretos was studied.

A. Line Width Variation

Pattern sensitivity, random process variations and limitations in lithography optics cause line widths to deviate as much as 30% from the nominal. This in turn causes an effective variation in the critical area for extra material defects to cause shorts, and thus the corresponding values in the POF matrix. The technology with which we are working is λ = 2 microns and the minimum spacing and width of the metal lines is 3 microns. In our experiments we have varied the line widths from +80 centimicrons through -80 centimicrons, which is roughly 30 % of the minimum width/spacing. The line widths are varied by varying the defect bias in VLASIC. Increasing the bias is equivalent to increasing line width, reducing the bias is equivalent to reducing the line width. The variation of these widths can be understood as moving the edges of the layout. Therefore a + 88 centimicron bias (-88 centimicron decrease in the line width) would be the same as moving all the edges of the polygons into the interior by 44 centimicrons.

Then defects are placed and the corresponding electrical faults are recorded. Only defects with edges in the region swept by the changing line widths can be affected by a change in line width. Thereafter the fault simulation is carried out and the mapping from faults to failure patterns is completed. From this defect to fault, fault to failure pattern dictionary the POF matrix is generated, and eventually the Pareto generated. The Pareto obtained gives us the variation in the predicted defect density for each defect type after alteration of the line widths. The line widths are varied individually for each defect type and the results are observed. Then variation of more than one defect type is carried out simultaneously and the effect of this variation on the defect densities is studied.

We try to check for cross terms that could exist when more than one defect type is simultaneously varied and whether they are negligible enough to overlook them.

Figures 8-22 show the sensitivity of defect density to line width variation and the corresponding X variable line fit plots for different layers (circuit c17).

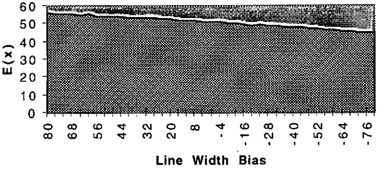

Figure 8(a) Predicted POSMF (first metal) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

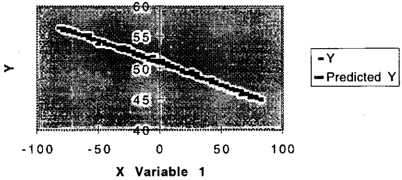

Figure 8(b) X variable line fit plot for curve shown in Figure 8(a) with correlation 0.9925.

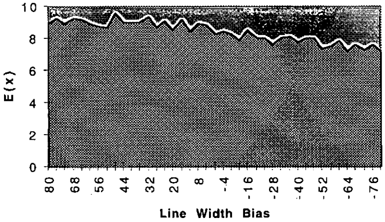

Figure 9(a) Predicted POSPG (poly) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

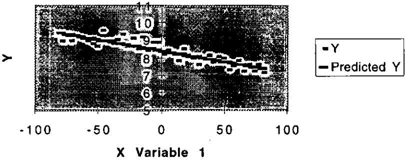

Figure 9(b) X variable line fit plot for curve shown in Figure 9(a) with correlation 0.8164.

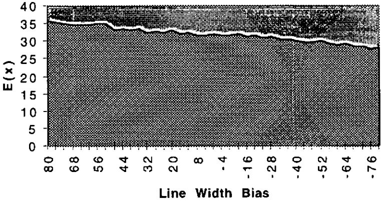

Figure 10(a) Predicted POSMS (second metal) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

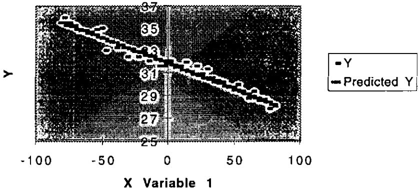

Figure 10(b) X variable line fit plot for curve shown in Figure 10(a) with correlation 0.9652 .

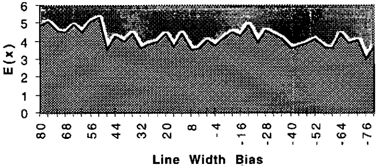

Figure 11(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

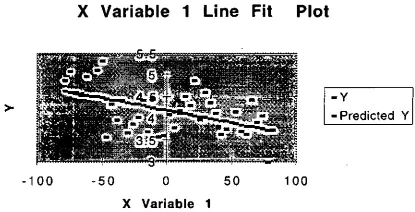

Figure 11(b) X variable line fit plot for curve shown in Figure 11(a) with correlation 0.2937.

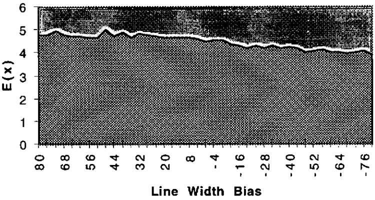

Figure 12(a) Predicted PIN2 (metal 1-metal2 pinhole) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

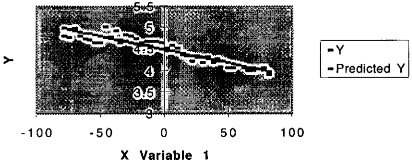

Figure 12(b) X variable line fit plot for curve shown in Figure 12(a) with correlation 0.8757.

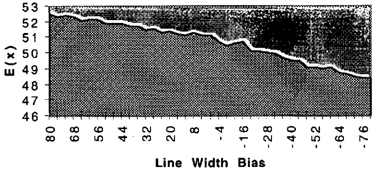

Figure 13(a) Predicted POSMF (first metal) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

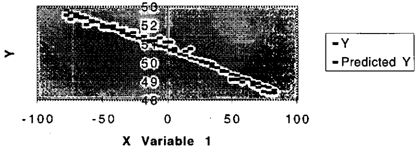

Figure 13(b) X variable line fit plot for curve shown in Figure 13(a) with correlation 0.9725.

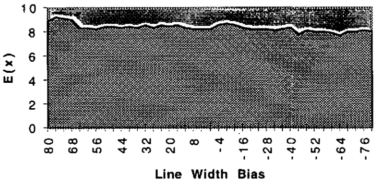

Figure 14(a) Predicted POSPG (poly) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

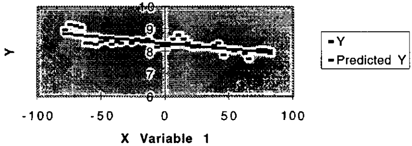

Figure14(b) X variable line fit plot for curve shown in Figure 14(a) with correlation 0.6006.

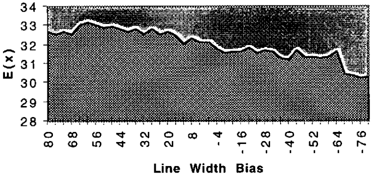

Figure 15(a) Predicted POSMS (second metal) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

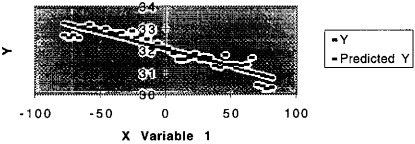

Figure 15(b) X variable line fit plot for curve shown in Figure 15(a) with correlation 0.8495.

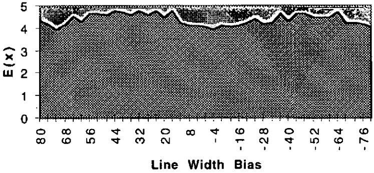

Figure 16(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n

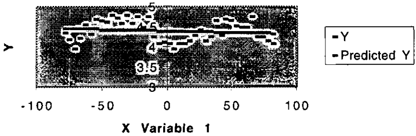

Figure 16(b) X variable line fit plot for curve shown in Figure 16(a) with correlation 0.1950.

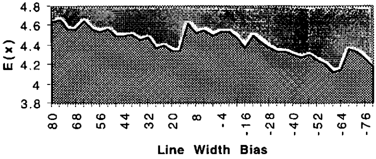

Figure 17(a) Predicted PIN2 (metal 1-metal2 pinhole) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

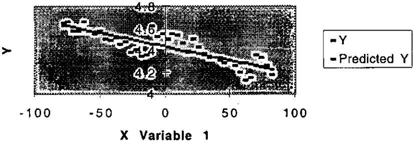

Figure 17(b) X variable line fit plot for curve shown in Figure 17(a) with correlation 0.6974.

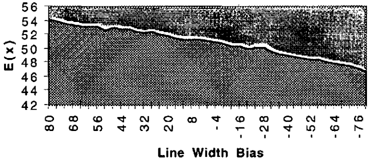

Figure 18(a) Predicted POSMF (first metal) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

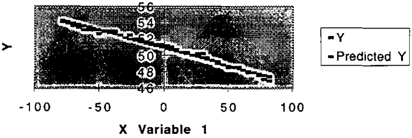

Figure 18(b) X variable line fit plot for curve shown in Figure 18(a) with correlation 0.9858.

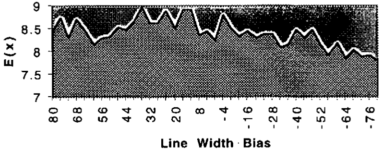

Figure 19(a) Predicted POSPG (poly) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

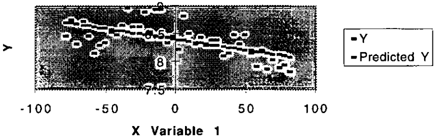

Figure 19(b) X variable line fit plot for curve shown in Figure 19(a) with correlation 0.3819.

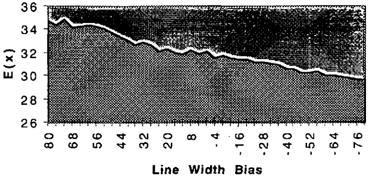

Figure 20(a) Predicted POSMS (second metal) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

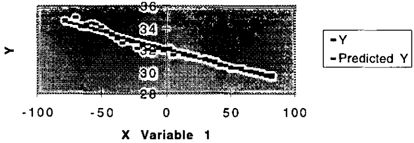

Figure 20(b) X variable line fit plot for curve shown in Figure 20(a) with correlation 0.9698.

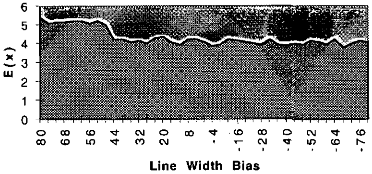

Figure 21(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n

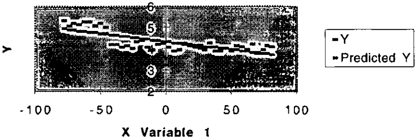

Figure 21(b) X variable line fit plot for curve shown in Figure 21(a) with correlation 0.5829.

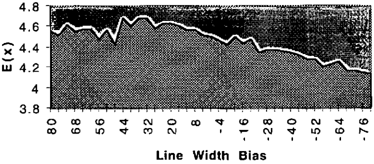

Figure 22(a) Predicted PIN2 (metal 1-metal 2 pinhole) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n

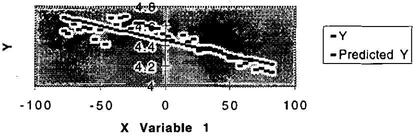

Figure 22(b) X variable line fit plot for curve shown in Figure 22(a) with correlation 0.7403.

The curves as shown in these figures are essentially linear with a very small quadratic factor. Note that some curves have significant noise, this is due to the nominal Pareto we have used in our simulation experiments. This Pareto causes first metal to have the most defects then second metal, poly, pin1 and pin2. This explains the increasing noise in curves for layers in the following order first metal, second metal, poly, pin1 and pin2. We observe a shift in the slopes of some curves, making them piecewise linear. This can be explained as follows: if we have two parallel lines, and they are spaced 3 um apart for length L1, and 4 um apart for length L2, then as the defect size rises (our bias value), the critical area will first appear in the 3 um section, rises from 0 with slope L1 from 3 um to 4 um, and then after 4 um, the slope rises as L1+L2. Similarly when the defect is shrinking.

The lines in the layouts are 3 um wide except at contacts where they are 4 um wide, then assuming the contacts are centered, and spacing is 7 um center to center (4 um contact + 3 um space), we have two spacings - 3 um and 4 um. However if we just make small changes around a given defect size, we essentially stay on the same section and same slope, but farther away we add or drop critical areas, changing the slope.

Now this discussion has been in the context of critical area at a defect size. However we must consider the entire distribution of sizes. The defect density is actually a convolution of the defect size distribution with the critical area as a function of defect size.

Assuming the defect size distribution is 1/x^3 and the critical area function is approximately piecewise linear as described above, then the result is piecewise quadratic. Changing the bias is effectively shifting the size distribution relative to the critical area function, and so can be approximated as piecewise linear. But as noted above, the range of variation is small enough that a linear model is sufficient

A method of best curve fitting by linear regression was applied. From these plots for all the three cases of varying different layer widths we observe experimentally that a linear model is sufficient as shown by the high correlation values.

Another design (ISCAS 85 benchmark circuit c432) was also considered to confirm the validity of the linear model.

Figures 23-37 show the sensitvity of defect density to line width variation and the corresponding X variable line fit plots for different layers (circuit c432).

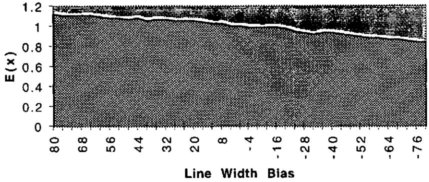

Figure 23(a) Predicted POSMF (first metal) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

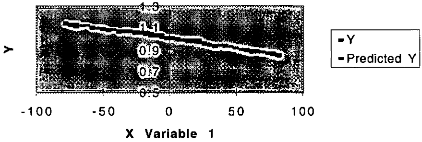

Figure 23(b) X variable line fit plot for curve shown in Figure 23(a) with correlation 0.9811.

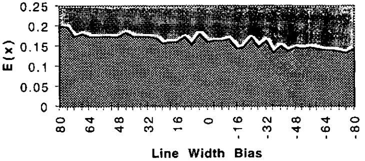

Figure 24(a) Predicted POSPG (poly) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

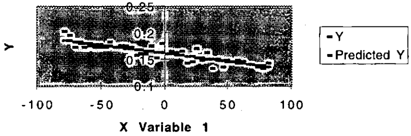

Figure 24(b) X variable line fit plot for curve shown in Figure 24(a) with correlation 0.7617.

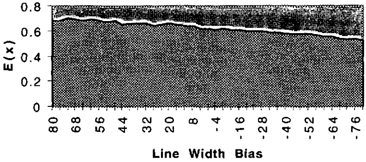

Figure 25(a) Predicted POSMS (second metal) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

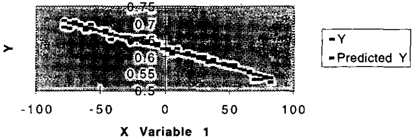

Figure 25(b) X variable line fit plot for curve shown in Figure 25(a) with correlation 0.9728.

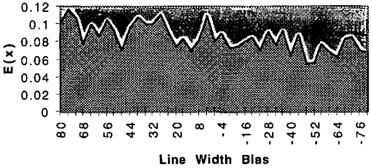

Figure 26(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

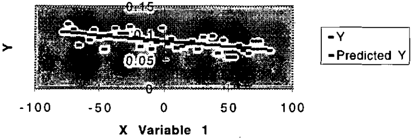

Figure 26(b) X variable line fit plot for curve shown in Figure 26(a) with correlation 0.4020.

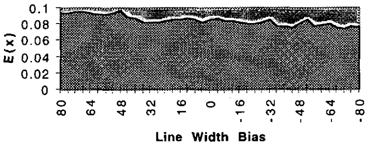

Figure 27(a) Predicted PIN2 (metal 1-metal 2 pinhole) defect density vs. metal 1 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n

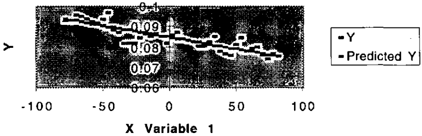

Figure 27(b) X variable line fit plot for curve shown in Figure 27(a) with correlation 0.7778.

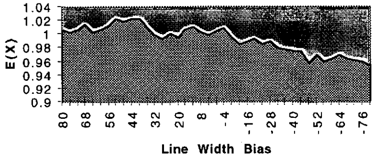

Figure 28(a) Predicted POSMF (first metal) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

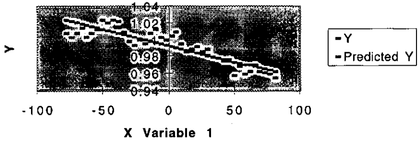

Figure 28(b) X variable line fit plot for curve shown in Figure 28(a) with correlation 0.7979.

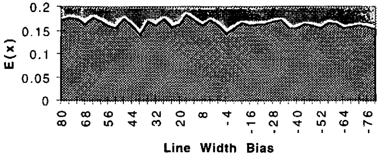

Figure 29(a) Predicted POSPG (poly) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

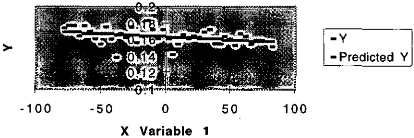

Figure 29(b) X variable line fit plot for curve shown in Figure 29(a) with correlation 0.1503.

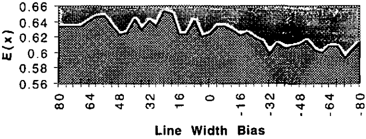

Figure 30(a) Predicted POSMS (second metal) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

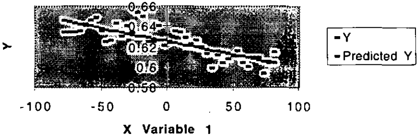

Figure 30(b) X variable line fit plot for curve shown in Figure 30(a) with correlation 0.6520.

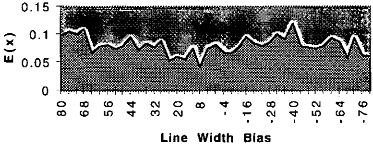

Figure 31(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

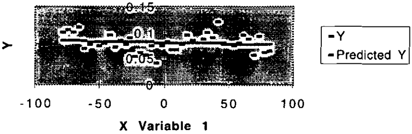

Figure 31(b) X variable line fit plot for curve shown in Figure 31(a) with correlation 0.0207.

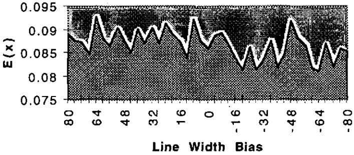

Figure 32(a) Predicted PIN2 (metal 1-metal 2 pinhole) defect density vs. poly line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

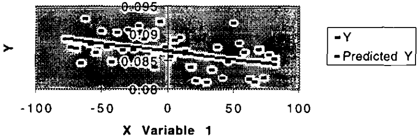

Figure 32(b) X variable line fit plot for curve shown in Figure 32(a) with correlation 0.2006.

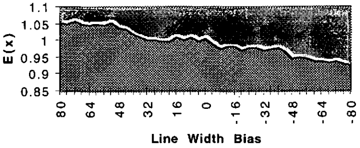

Figure 33(a) Predicted POSMF (first metal) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

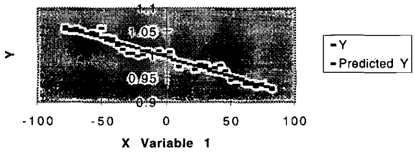

Figure 33(b) X variable line fit plot for curve shown in Figure 33(a) with correlation 0.9575.

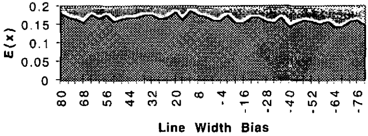

Figure 34(a) Predicted POSPG (poly) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

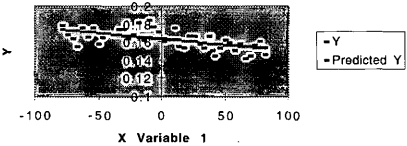

Figure 34(b) X variable line fit plot for curve shown in Figure 34(a) with correlation 0.3583.

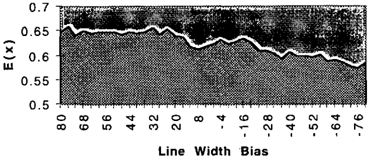

Figure 35(a) Predicted POSMS (second metal) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

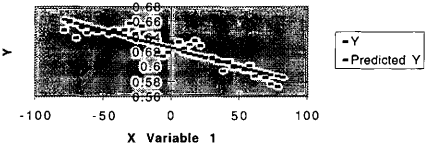

Figure 35(b) X variable line fit plot for curve shown in Figure 35(a) with correlation 0.8648.

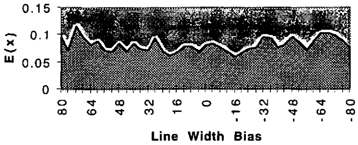

Figure 36(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

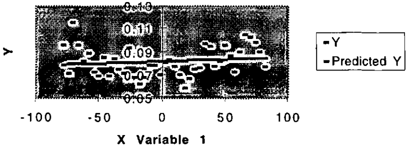

Figure 36(b) X variable line fit plot for curve shown in Figure 36(a) with correlation 0.0185.

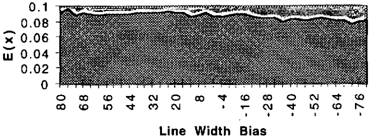

Figure 37(a) Predicted PIN2 (metal 1-metal 2 pinhole) defect density vs. metal 2 line width variation (+80 to -80 centimicrons) for circuit c432 with a chip sample size of 1000 and stopping criterion 1n.

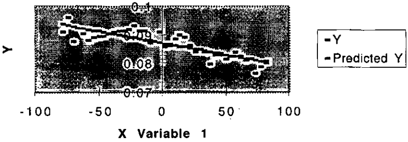

Figure 37(b) X variable line fit plot for curve shown in Figure 37(a) with correlation 0.7395.

Experiments were conducted to study the effects of cross terms when line widths of multiple defect types were simultaneously varied. We found that the cross term factor was negligible and the resultant Figures 38-42 confirmed a linear relationship.

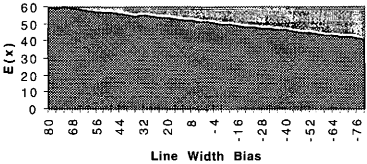

Figure 38(a) Predicted POSMF (first metal) defect density vs. metal 1 and metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

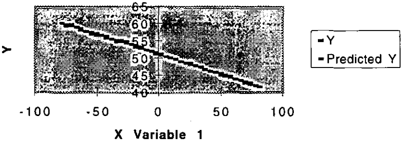

Figure 38(b) X variable line fit plot for curve shown in Figure 38(a) with correlation 0.9978.

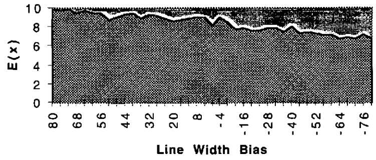

Figure 39(a) **Predicted POSPG (poly) defect density vs. metal 1 and metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.**

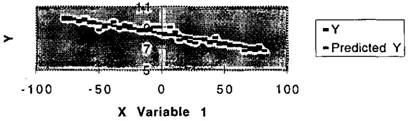

Figure 39(b) **X variable line fit plot for curve shown in Figure 39(a) with correlation 0.9179.**

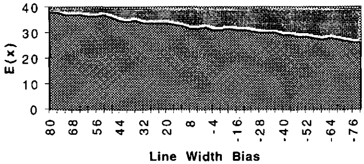

Figure 40(a) Predicted POSMS (second metal) defect density vs. metal 1 and metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

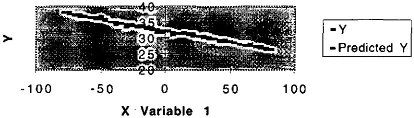

Figure 40(b) X variable line fit plot for curve shown in Figure 40(a) with correlation 0.9856.

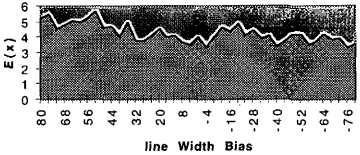

Figure 41(a) Predicted PIN1 (metal 1-poly pinhole) defect density vs. metal 1 and metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

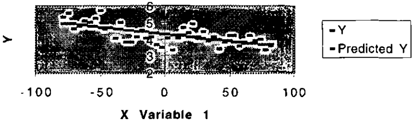

Figure 41(b) X variable line fit plot for curve shown in Figure 41(a) with correlation 0.4522.

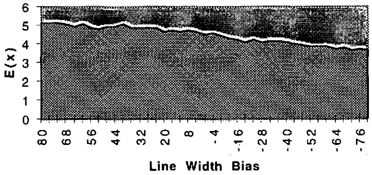

Figure 42(a) Predicted PIN2 (metal 1-metal 2 pinhole) defect density vs. metal 1 and metal 2 line width variation (+80 to -80 centimicrons) for circuit c17 with a chip sample size of 1000 and stopping criterion 1n.

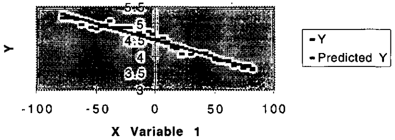

Figure 42(b) X variable line fit plot for curve shown in Figure 42(a) with correlation 0.9599.

Analysis of the behavior of the Pareto prediction

The following is an analysis of the behavior of the Pareto prediction done to confirm the additive linear behavior seen on the examples:

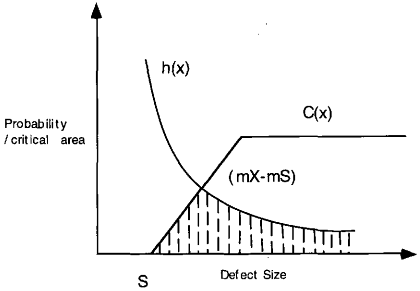

Figure 43 : Critical area and defect size curves

The Figure 43 gives us the critical area vs. defect size curves, a convolution of these curves gives the probability of a particular defect type to cause a failure.

S is the nominal spacing between the lines of a particular layer.

m is the sensitivity of defect density of the layer whose line widths are being varied.

$h(X) = A/X^3$ is the defect size function: (1)

$C(X) = m \cdot X - m \cdot S$ is the critical area function. (2)

$=> \int_S^\infty A\cdot(mX-mS)/X^3\cdot dX$ [defect size X critical area] (3)

$=> A\cdot m\cdot \int_S^\infty X/X^3\cdot dX - A\cdot m\cdot S \int_S^\infty 1/X^3\cdot dX$

$=> P = A\cdot m/ 2\cdot S$ (4)

$=> \partial P/\partial S = -A\cdot m/2\cdot S^2$ (5)

Therefore using (4) and (5) for our case where the defect density of a particular layer is sensitive to line width variation of any layer.

We get :

$P_{ijk} = C_{ijk} + N_{ijk}\cdot X_i$ (6)

Where,

X_i is the shift from the nominal spacing

$C_{ijk} = A\cdot m/ 2\cdot S$ (7)

$N_{ijk} = -A\cdot m/2\cdot S^2$ (8)

P_{ijk} is an entry in the POF matrix.

i is the defect type whose probability to cause a failure pattern is being considered.

k is a test failure pattern.

j is the layer whose line widths are being varied.

Now let us a consider a case where two defect types have caused two fault types.

We get a POF matrix P of the form :

$$\begin{vmatrix} C_{11} + N_{11}.X_1 & C_{21} + N_{21}.X_2 \\ C_{12} + N_{12}.X_1 & C_{22} + N_{22}.X_2 \end{vmatrix}$$

In the above POF matrix we have not applied the general description given by the subscripts in the equation (6) for the entries of the POF matrix. We have assumed for simplification purposes that each layer is affected by line width variations in the same layer only.

In the POF matrix subscripts 1 2 attached to the C and N terms refer to the effect of line width variation of layer 1 on intralayer 1 shorts thus causing a failure pattern 2.

We have obtained the above expression for probability of a particular defect type to cause a certain failure pattern. Intuitively we know that the line width variation in any one layer cannot alter the critical area for another layer. However changes in line width variation alter the overlap area in the case of pinhole defects. Hence the piecewise linear behavior of the results obtained for pinhole defects for line width variation of any layer can be explained.

Let d be the defect density vector and d_1, d_2 be the densities for the two defect types.

$$\begin{vmatrix} d_1 \\ d_2 \end{vmatrix}$$

We get the test count vector from $t = P \cdot d$.

Let the elements of P be expressed as:

$$\begin{vmatrix} P_1 & P_2 \\ P_3 & P_4 \end{vmatrix}$$

Then t can be written as:

$$\begin{vmatrix} P_1.d_1 + P_2.d_2 \\ P_3.d_1 + P_4.d_2 \end{vmatrix}$$

By applying elementary matrix operations we get P^{-1} as shown below:

$$\begin{vmatrix} \dfrac{P_4}{P_1.P_4-P_3.P_2} & \dfrac{-P_3}{P_1.P_4-P_3.P_2} \\ \dfrac{P_2}{P_1.P_4-P_3.P_2} & \dfrac{P_1}{P_1.P_4-P_3.P_2} \end{vmatrix}$$

The defect density vector d can be obtained by performing $P^{-1} \cdot t$ to give:

$$\left|\begin{array}{c} \dfrac{P_4(P_1.d_1+P_2.d_2) - P_3(P_3.d_1+P_4.d_2)}{P_1.P_4-P_3.P_2} \\ \\ \dfrac{-P_2(P_1.d_1+P_2.d_2)+P_1(P_3.d_1+P_4.d_2)}{P_1.P_4-P_3.P_2} \end{array}\right|$$

Substituting the values of P_1, P_2, P_3 and P_4 we get d_1':

$$\frac{\begin{array}{l} d_2.N_{21}.N_{22}.X_2^2-d_1.N_{12}^2.X_1^2+(d_1.N_{11}.N_{22}-d_2.N_{12}.N_{22})X_1.X_2+[(C_{22}.N_{11}-2C_{12}.N_{12})d_1 \\ -d_2.C_{22}.N_{12}]X_1+[(C_{11}.N_{22}+C_{22}.N_{21}+C_{21}.N_{22})d_1-d_2.C_{12}.N_{22}]X_2+(C_{11}.C_{22}-C_{12}^2)d_1+ \\ (C_{21}.C_{22}-C_{12}.C_{22})d_2 \end{array}}{\begin{array}{c} N_{11}.N_{22}X_1.^2+[C_{22}.N_{11}-C_{12}.N_{11}-C_{11}.N_{12}]X_1+C_{11}.N_{22}.X_2+N_{11}.N_{22}.X_1.X_2+(C_{11}.C_{22}- \\ C_{11}.C_{12}) \end{array}}$$

This would be sufficient to examine what factors the defect density depends upon. When we are varying only layer 1, the terms that contain X_2, $X_1 \cdot X_2$ and X_2^2 vanish (since $X_2 = 0$) and only X_1 and X_1^2 terms remain both in the numerator as well as the denominator. However if we recall some of the theory we went over earlier, we know that the N terms are comparatively much smaller than the C terms. The value of N term is $-A \cdot m/2 \cdot S^2$ and the value of C term is $A \cdot m/ 2 \cdot S$ as given by (3) and (4) respectively. If we examine the coefficient of the X_1^2 term we find that it is $-d_1 \cdot N_{12}^2$ which is comparatively very much less than the (C·N) terms that exist as coefficients for X_1.

So the overall expression will be of the form $a_1 \cdot X_1 + b_1 / a_2 \cdot X_1 + b_2$ where $a_1 > a_2$ and $b_1 > b_2$, since a_1 and b_1 contain d terms while a_2 and b_2 do not contain any d terms. This explains the linearity observed in our results.

For the case of line width variation for two layers we can observe that the defect density also has some cross terms e.g. $X_1 \cdot X_2$. We notice that the $X_1.X_2$ terms have the product of two N terms as coefficient. This makes the effect of cross terms negligible. The same also applies to the quadratic terms. Thus the overall relationship is linear since the X_1 and X_2 terms have the largest coefficients. The same theory would apply for more than two layers if varied simultaneously.

Let us consider an example in which there are two different layers M1 and M2 and two sets of parallel lines for each layer, each set having different length.

<u>For the two layers M1 and M2</u>:

Let the two sets of parallel lines for layer M1 have the following lengths:

L1 = 3000 centimicrons , L2 = 3000 centimicrons

Let the two sets of parallel lines for layer M2 have the following lengths:

L3 = 3000 centimicrons , L4 = 5000 centimicrons

Spacing S = 300 centimicrons

The defect size X_o at which the peak defect frequency occurs = 100 centimicrons

Let a short in the lines with length L1, L3 cause fault 1 and short in the lines with length L2, L4 cause fault 2.

We get $N = -X_o^2 \cdot L/4 \cdot S^2$ and $C = X_o^2 \cdot L/4.S$ by substituting $A = X_o^2/2$ and $m \approx L$ in (8) and (7) respectively.

$d_1 = d_2 = 1000$ defects / sq. cm.

Following the notation provided earlier in this section we get

$N_{11} = N_{12} = N_{21} = -83.33$, $N_{22} = -138.89$

$C_{11} = C_{12} = C_{21} = 25000$, $C_{22} = 41666.67$

substituting these values we get the defect density for M1 as given below

$$\frac{0.1157\,X_2^2 - 0.6944\,X_1^2 - 208.325\,X_1 - 694.4334\,X_2 + 41666.675}{0.0019\,X_1^2 + 0.0694\,X_1 - 0.3472\,X_2 + 0.0012\,X_1.X_2 + 41.667}$$

$$\approx 1000 + 5X_1 - 16.667\,X_2$$

Clearly we can neglect the $X_1 \cdot X_2$, X_1^2 and X_2^2 terms thus the defect density is linear in X_1 and X_2.

B. Defect Sample Size

The suitable defect sample size for building the POF matrix would be one that would help diagnose most of the bad chips, with the confidence interval due to the finite number of bad chips to be greater than the interval due to defect sampling noise in the POF matrix entries. Obviously a large defect sample size would help us to overcome the noise problem and give us a dictionary with very good diagnosibility.

But the construction costs for a dictionary associated with such a large defect sample size would be too expensive in terms of time and memory space. This section introduces us to the theory which would help us to achieve some balance between large dictionary construction costs and very low defect sampling noise, high diagnosibility.

As we increase the defect sampling size the number of different types of failure patterns also increases. When there are fewer than 5 patterns of a particular type, a Beta distribution is a better approximation than a binomial distribution for the sample mean.

The Beta distribution is given by :

$\mu_i = (Y_i + 1)/(n+2)$

$\sigma_i^2 = (Y_i + 1)(n - Y_i + 1)/(n+2)^2(n+3)$

The Binomial distribution is given by :

$\mu_i = Y_i / n$

$\sigma_i^2 = Y_i.(1-Y_i)/n^2.(n-1)$

where,

Y_i = number of faults of type i.

n = number of defects in sample.

μ_i = sample mean.

σ_i^2 = sample variance.

The rate of increase in the number of different types of patterns depends upon the type of design under consideration. The design could be random logic or memory array or some combination of the two. The distribution of critical area sizes is a crucial factor which affects this rate. For random logic there is a distribution of sizes, with a relatively small fraction accounting for most failures.

Thus a relatively small defect sample size will generate most patterns. In an array, the critical area sizes are evenly distributed, so the number of patterns is more proportional to the number of defects, until a much larger sample is used.

The rate of increase of failure patterns decreases with larger sample size. The figure 44 gives us the percentage of all test failure patterns that can occur on a chip versus the sampling size for a typical random logic design and array.

The climb shown in Figure 44 depends upon the type of the design under consideration i.e. the critical area distribution by test failure pattern.

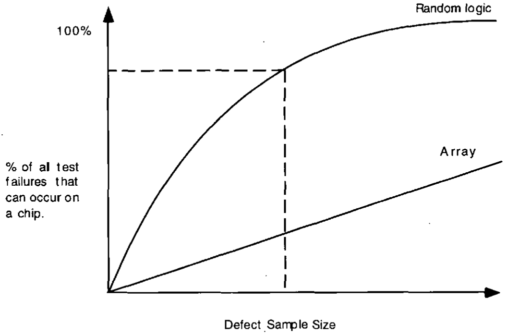

Figure 44: Typical defect sample size vs. number of failures curve

We have conducted experiments with different defect sample sizes for our random logic design c17 to confirm the theory discussed above. Table 6 gives us the probabilities for different failure patterns with different defect sample sizes. Clearly we can see that the rate of increase of failure patterns decreases beyond a threshold defect sample size.

Table 7 gives us the mean ± standard deviation values for circuit c17 with 10000, 100000, 700000 and 1500000 sample sizes respectively. From the table we find that the confidence interval, the mean error falls as the sample size increases.

Table 6: Probabilities for different failures with different sample sizes

Pattern	10,000	100,000	700,000	1,500,000
1-00	0.0165	0.0195	0.0212	0.0210
1-0X	0.0015	0.0044	0.0040	0.0041
1-10	0.0005	0.0002	0.0002	0.0002
1-11	0.0175	0.0142	0.0198	0.0196
1-1X	0	0.00005	0.00001	0.00002
1-X1	0.0160	0.0098	0.0102	0.00098
1-XX	0.0005	0.0006	0.0007	0.0007
2-01	0.0115	0.0090	0.0101	0.0101
2-0X	0.0030	0.0034	0.0039	0.0039
2-11	0.0070	0.0062	0.0059	0.0058
2-XX	0.0075	0.0050	0.0054	0.0053
3-01	0.0030	0.0034	0.0039	0.0039
4-00	0.0080	0.0080	0.0069	0.0071
4-XX	0.0020	0.0041	0.0045	0.0044
4-11	0	0	0.00002	0.000003
5-00	0.0100	0.0050	0.0055	0.0053
5-01	0.0020	0.0017	0.0020	0.0021
5-10	0.0035	0.0027	0.0029	0.0026
6-11	0.0035	0.0024	0.0024	0.0022

Table 7: Mean ± standard deviation values for circuit c17 with varying defect sample sizes and chip sample size of 1000

Defect	10,000	100,000	700,000	1,500,000
POSMF	51.5663± 6.3983	51.568 ± 13.6581	51.3672± 14.8302	51.3483± 15.1257
POSPG	8.5341± 3.9213	8.3980± 7.8398	8.46312± 9.3598	8.4058± 9.411
POSMS	32.5114± 5.7776	32.1477± 8.0539	32.1313± 6.3819	31.9957± 6.1622
PIN1	5.6663± 8.0133	7.1514± 10.1136	7.0201± 9.9279	7.5072± 10.6168
PIN2	4.5907± 2.9431	4.5071± 3.4479	4.4587± 2.6708	4.5037± 2.7071

For defect Pareto calculation we have to multiply the test count vector with the inverted POF matrix. The SVD algorithm [34,35] is used to invert the POF matrix. However the SVD algorithm effectively neglects the low probability terms in the POF matrix.

Therefore if we do not have failure patterns with low probabilities in our POF matrix this would not affect the accuracy of the Pareto calculation. Hence the optimum defect sample size would be the one very close to the threshold sample size. Thereby saving us the time and memory expense which would have incurred with large defect sample sizes. This would give us a dictionary with good diagnosibility and less construction cost since the dictionary does not contain the low probability failure patterns.

The issue that remains is to identify when our defect sample size is close to the threshold value. For our case we started with an arbitrary defect sample size of 10,000 defects and then checked to see how many of the total failure patterns are those with high probability. If they comprise a bulk of the total number of failure patterns generated by the sample size in consideration and a very few patterns have comparatively less probability then our starting defect sample size is adequate. We then take another defect sample size greater (here we took 100,000) than the starting sample size and check how many high probability failure patterns there are and whether the high probability patterns generated by the previous sample have higher probability than before with the new defect sample size or whether they have remained stable or decreased in value.

If they have a higher value then the rate of percent increase in probability vs. percent increase in sample size should be calculated for the high probability terms. We can also check how may new patterns are being added with the increasing sample size and what their probabilities are along with the percent of all possible failure patterns covered up to this point. The total number of failure patterns depends upon the number of test vectors and the stopping criterion applied. In the case of bridging faults the number of failure patterns can be roughly proportional to the number of nets (for stopping criteria kp k = 1,2,... ; for 1n it is proportional to the number of test vectors). So if we are approaching the total number of failure patterns that could exist then we could establish that the sample size we have used to obtain this number of failure patterns is sufficient to overcome the noise problem. For a memory structure the total number of failure patterns can be bounded by O(n) (where n is the number of bits).

All these factors combined together help us to get an idea about our design and allow us to estimate an optimum defect sample size. However a more exact method of estimation of an optimum defect sample size which would answer problems like dictionary construction cost and diagnosibility would be to apply the beta distribution. First of all we can set goals such as the error should be less than chip sampling error, we should be able to diagnose 90% of the chips etc.

Substituting $Y_i = 0$ (for 0 entries) and n the total number of defects placed on the chip we get

$\mu_i = 1/(n+2)$

$\mu_i \sim 1/n$

$\sigma_i^2 = (n-1)/(n+2)^2(n+3)$

$\sigma_i \sim 1/n$

and if we use 1.96σ as an upper bound we get

The sample mean would be $\sim 3\mu_i$

$\Rightarrow 3/n$

The probability of unseen patterns can be calculated by multiplying $3\mu_i$ by the total number of failure patterns.

If the total probability of available patterns for a particular defect sample size is much higher than the probability of unseen patterns (by a factor of 10) then we have reached our adequate defect sample size, otherwise we have to use a larger sample size that would give us a value closer to the desired probability.

The Figure 45 gives us the number of all failure patterns covered vs. the defect sample size for c432. We can see that at roughly 700K defects the rate of increase in the number of failure patterns with sample size decreases significantly. Figure 46 shows the number of unique faults covered vs. defect sample size. We can see how the slope of the curve decreases after a defect sample size of 700K .

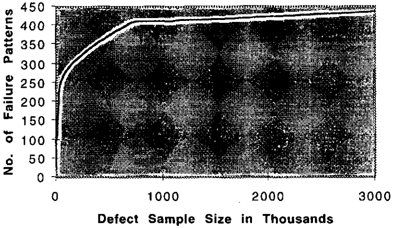

Figure 45: No. of failure patterns vs. defect sample size in thousands for c432

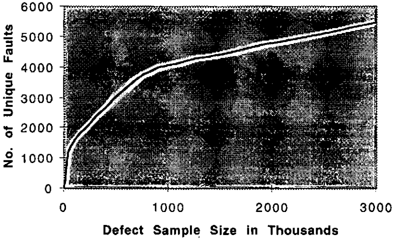

Figure 46: No. of unique faults vs. defect sample size in thousands for c432

The total probability of available patterns at a defect sample size of 700K is 0.0337. The probability of unseen patterns can be calculated by multiplying the mean value given by $\mu_i \sim 1/n$ ($\mu_i \sim 3/n$ would give us a conservative value) with the number of estimated unseen failure patterns (where n is 700K and the estimated total number of failure patterns is 4320, assuming there are $k = 10$ failure patterns per net). Thus we get the probability for unseen patterns equal to 0.0056. From this information we estimate that 85.8% of all failure patterns are covered with a defect sample size of 700K.

Note that we do not calculate the number of failure patterns by substituting design information like the number of test vectors 'v' and the number of primary outputs 'po' in $v \cdot 2^{po}$, since this would give us a conservative value for the number of failure patterns.

Figure 47 shows the actual percentage of failure patterns covered vs. the predicted percentage of failure patterns covered for a distribution of defect sample sizes for c432. We see that our predicted values differ from the actual only by a small amount. This difference depends upon the k value that we have considered. The number of failure patterns is almost linearly proportional to the number of nets in memory arrays and can be given by $k \cdot no.\ of\, nets$ for 1p test stopping criterion, this number would be obviously very conservative for stopping criterion 1n.

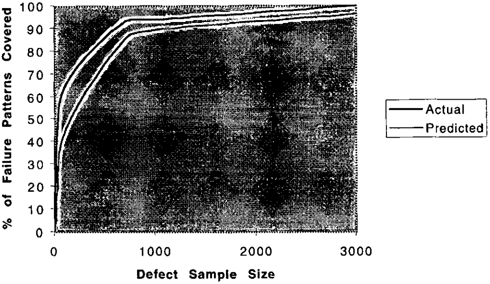

Figure 47: Percentage of actual vs. predicted failure patterns covered for a distribution of defect sample size in thousands for c432.

Table 8 gives the mean and standard deviation values for circuit c432 with varying defect sample sizes and chip sample size of 10000. The standard deviation values were calculated analytically. We observe that there is not much increase in the standard deviation from 700K defects onwards and the mean also converges. This further confirms our method of estimation of an adequate defect sample size.

We can also estimate the defect sample size by considering the probabilities of failure patterns covered for a defect sample size X and then analyzing the probabilities for failure patterns for defect sample size Y (where Y > X). If there is not much increase in the probability values then we can conclude that we have arrived at the desired number of defects.

Table 8: Mean ± standard deviation values for circuit c432 with varying defect sample sizes and chip sample size of 10000

Defect	1,000	10,000	100,000	700,000	1,000,000	3,001,440
POSMF	0.8789± 0.0472	0.9221± 0.0535	0.9689± 0.06236	0.9995± 0.0757	1.0001± 0.0765	1.0012± 0.0922
POSPG	0.1448± 0.0743	0.1517± 0.0389	0.1580± 0.0509	0.1561± 0.0970	0.2310± 0.0464	0.1642± 0.1094
POSMS	0.5514± 0.1389	0.5826± 0.0520	0.6039± 0.0564	0.6317± 0.0927	0.6238± 0.1111	0.6260± 0.0803
PIN1	0.0724± 0.0379	0.0777± 0.1312	0.0774± 0.1085	0.0810± 0.1389	0.0803± 0.1329	0.0833± 0.1220
PIN2	0.0758± 0.0176	0.0795± 0.0353	0.0864± 0.0381	0.0912± 0.0384	0.0867± 0.0412	0.0908± 0.0423

C. Bridge Resistance

Bridging failures are the most common defects present in mature CMOS integrated processes. Hence the detection of faults introduced by bridging defects is required in order to perform an acceptable test of an IC. Bridge resistance variation is random across a few wafer samples. Most of the bridging faults have low resistance. But roughly half have resistance higher than 500Ω, with the percentage varying from lot to lot [39].

We shall begin by postulating that a distribution of bridging resistance does not affect Pareto accuracy. For almost every fault we postulate that increasing the bridge resistance from 0Ω to ∞ causes the test failure to change from the faulty pattern to a fault free pattern. If the test set has high fault coverage then the test sequence detects bridges over nearly their entire resistance range where they can cause a fault.

In some cases [40,41], as the bridge resistance is increased , additional test failure patterns may occur. If these alias to patterns associated with other defect types, then a dictionary built using a fixed 100Ω may incorrectly predict a Pareto for chips with these overlapping patterns. Also from [1] we know that if all X values (intermediate voltage values) at the outputs were mapped to some existing patterns then the overall error in the accuracy would not be more than 6 %. This further strengthens our views regarding bridge resistance and its small effect on Pareto accuracy.

The maximum resistance upto which the fault is detectable depends upon the threshold of the gate which is receiving the fault . This threshold is in turn dependent upon the threshold of the driving gates, nodal voltages, power supply etc. Please refer to Figure 48 which illustrates the detectability of faults with variation in bridge resistance.The curves shown in this figure correspond to the voltage values of the two nodes which are bridged together, at a given power supply voltage and bridge resistance varying from 0Ω to higher values. We can see that the fault remains detectable for a small range of bridge resistance values and then becomes undetectable over a higher range

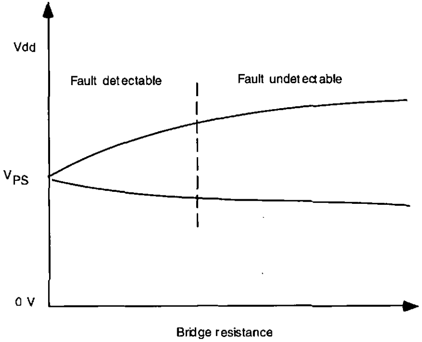

Figure 48: Fault detectability for varying bridge resistance

If the number of outputs is small for a given circuit then as we increase the bridge resistance we do not find much decrease in the number of failure patterns that are detectable. This is because all the different possible failure patterns for a small number of outputs is already small. This implies that a large number of faults would fall into one failure pattern type which is unlike the case of a circuit having a larger number of outputs which would have a larger number of failure patterns and therefore the number of faults that would fall into one failure type would be relatively small.

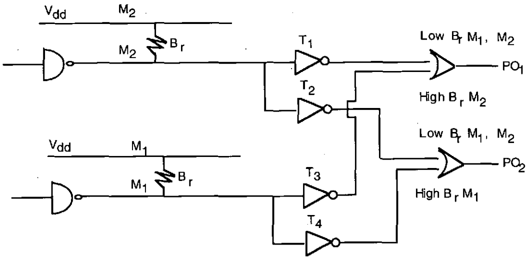

Figure 49: Circuit level explanation of the effect of bridging resistance on fault detectability

Generally we see that at lower bridge resistances most of the faults are detectable. If we consider portion of a circuit as shown in Figure 49, the shorts between both M_1 (metal1) layers and M_2 (metal2) layers propagate to the primary outputs PO_1 and PO_2 at lower resistances. However at higher resistances we find only the bridging fault between M_2 layers propagated to PO_1 and only the bridging fault between M_1 layers propagated to PO_2.

This explains how the number of detectable faults corresponding to a particular failure pattern decreases as we increase the bridge resistance.

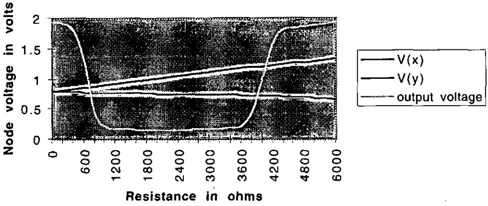

Figure 50: Fault detection at a higher bridge resistance - XOR gate with inputs bridged, test vector 0001 at Vdd = 2V.

The Figure 50 shows a particular case where at a higher bridge resistance we are able to detect a bridging fault [40].This fault was detectable even for a higher bridge resistance since a required environment was set up. This required a number of conditions to be met like a particular test sequence, device parameters, nodal voltages etc.

We have conducted experiments for the c17 and c432 ISCAS benchmark circuits and have found what we had postulated earlier to be true i.e., the bridging resistance does not have any effect on Pareto accuracy. Table 9 shows that the number of detectable faults decreases with increase in bridge resistance.

Table 9: Failure counts for different defect types (c17, c432)

c432	**POSMF**	**POSPG**	**POSMS**	**PIN1**	**PIN2**	**TOTAL**
6000Ω	590	714	436	58	374	2172
1500Ω	3295	3035	2858	2130	9072	20390
500Ω	3348	3089	2915	2134	9126	20612
100Ω	3349	3089	2915	2134	9126	20613
c17	**POSMF**	**POSPG**	**POSMS**	**PIN1**	**PIN2**	**TOTAL**
4000Ω	1377	2053	1311	939	3174	8854
1500Ω	2223	3226	2421	1314	5888	15072
500Ω	2223	3226	2421	1314	5888	15072
100Ω	2223	3226	2421	1314	5888	15072

The number of overlapping patterns for c17 as we change the bridge resistance from 100Ω to 500Ω, 100Ω to 1500Ω and 100Ω to 4000Ω is 462, 605 and 2629 respectively. In the Table 10 the **100Ω** column refers to the mean + standard deviation values of the Pareto generated for the 100Ω resistance , the column marked **Replaced** next to the **100Ω** column refers to the mean and standard deviation values of the Pareto generated from the POF matrix for the 100Ω case whose pattern counts were replaced with counts of similar patterns occurring in the POF matrix generated for the 4000Ω case.

The **4000Ω** column refers to the mean + standard deviation values of the Pareto generated for the 4000Ω resistance, the column marked **Replaced** next to the **4000Ω** column refers to the mean and standard deviation values of the Pareto generated from the POF matrix for the 4000Ω resistance whose pattern counts were replaced with counts of similar patterns occurring in the POF matrix generated for the 100Ω case. From the Table 10 we see that there is not much difference in the Paretos when higher bridge resistance is considered.

Table 10: Paretos with pattern counts exchanged for overlapping patterns

Defect	**100Ω**	**Replaced**	**4000Ω**	**Replaced**
POSMF	51.3672± 14.8302	51.8398± 11.8597	86.709± 26.7088	97.7516± 29.6609
POSPG	8.46312± 9.3598	8.6860± 8.8526	14.6577± 12.3373	15.9779± 22.3394
POSMS	32.1313± 6.3819	32.4811± 11.9883	54.3283± 16.5727	60.5474± 16.3816
PIN1	7.0201± 9.9279	5.9708± 8.4440	11.245± 15.9028	17.1486± 24.2518
PIN2	4.4587± 2.6708	4.4696± 2.6707	7.6883± 6.8695	8.4730± 7.3531

VI. CONCLUSION

A. Summary

We arrived at the following conclusions following experimentation and study conducted in the given topics:

Line width variation

- For the types of circuits and technology considered, a +/- 30% variation in line width causes a significant variation (e.g. +/- 10%) in predicted defect Paretos, and so must be modeled and corrected.
- An additive linear model is adequate for correcting for the line width effect. The actual response may be PWL or quadratic, but the additional accuracy of a more complicated model is not worth the additional calibration effort.
- The larger defect sample sizes during model building are required to reduce the sampling noise to the point that a good model can be fit.

Defect sample size

- We can reduce the dictionary construction costs by using relatively small defect sample sizes.
- If experiments were conducted with a defect sample size X then with a sample size Y (where $Y > X$) the number of failures added to the POF matrix would help us to estimate a suitable defect sample size.

Bridge resistance distribution

- A distribution in bridging resistance has little effect on Pareto accuracy.
- Very few failures alias to existing patterns with an increase in resistance. Hence they should not affect the Pareto accuracy.
- The detectability of faults decreases with an increase in bridging resistance.

B. Future work

For the experiments we conducted concerned with line width variation we chose to use large defect sample sizes to eradicate the sampling noise. In our experimentation the defect sampling was uniform across the whole chip. The way to deal with this "correctly" is to change the defect sampling to be nonuniform across the chip, just sampling where the edges are moving. Since we are biasing the lines up and down, the obvious thing to do is to try and have all defects have an edge in the range where change occurs. This area is a region around all polygons on a layer. For this we have to randomly decide where to place the defect in those regions. One approach is to look at the edges of the geometry and randomly place the defects in the region around that. This could be determined by using polygon operations on the mask geometry. The hard part is changing the random number generators to randomly place in this region. Probably the way to do it would be to concatenate all the periphery of all polygons into a line, and randomly choose a coordinate on that line, and then offset into the region.

We have considered random logic for our experiments and were able to decipher what an adequate defect sample size was by observing certain details in the POF matrix. A general and exact method applicable to different designs has to be uncovered. Several questions would have to be answered by this strategy. For example we assumed in our research that the defect sample size which would cover failures close to the total would be appropriate, but we did not answer how many percent of the total failures should be covered by an adequate defect sample size.

For our experiments we found that roughly 3-10% of the total number of failures were overlapped patterns for distribution of bridge resistance. It may be of interest to study some other designs and check to see what are the different reasons that lead to detectability of faults at higher bridge resistances.

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