FAST HIGH-ORDER VARIATION-AWARE IC INTERCONNECT ANALYSIS

A Thesis

by

XIAOJI YE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2007

Major Subject: Computer Engineering

FAST HIGH-ORDER VARIATION-AWARE IC INTERCONNECT ANALYSIS

A Thesis

by

XIAOJI YE

Approved by:

Chair of Committee,   Peng Li
Committee Members,   Jiang Hu
                     Duncan Henry M. Walker

Head of Department,   Costas N. Georghiades

August 2007

Major Subject: Computer Engineering

ABSTRACT

Fast High-Order Variation-Aware IC Interconnect Analysis. (August 2007)

Xiaoji Ye, B.E., Wuhan University

Chair of Advisory Committee: Dr. Peng Li

Interconnects constitute a dominant source of circuit delay for modern chip designs. The variations of critical dimensions in modern VLSI technologies lead to variability in interconnect performance that must be fully accounted for in timing verification. However, handling a multitude of inter-die/intra-die variations and assessing their impacts on circuit performance can dramatically complicate the timing analysis.

In this thesis, three practical interconnect delay and slew analysis methods are presented to facilitate efficient evaluation of wire performance variability. The first method is described in detail in Chapter III. It harnesses a collection of computationally efficient procedures and closed-form formulas. By doing so, process variations are directly mapped into the variability of the output delay and slew. This method can provide the closed-form formulas of the output delay and slew at any sink node of the interconnect nets fully parameterized, in-process variations. The second method is based on adjoint sensitivity analysis and driving point π model. It constructs the driving point model of the driver which drives the interconnect net by using the adjoint sensitivity analysis method. Then the driving point model can be propagated through the interconnect network by using the first method to obtain the closed-form formulas of the output delay and slew. The third method is the generalized second-order adjoint sensitivity analysis. We give the mathematical derivation of this

method in Chapter V. The theoretical value of this method is it can not only handle this particular variational interconnect delay and slew analysis, but it also provides an avenue for automatical linear network analysis and optimization.

The proposed methods not only provide statistical performance evaluations of the interconnect network under analysis but also produce delay and slew expressions parameterized in the underlying process variations in a quadratic parametric form. Experimental results show that superior accuracy can be achieved by our proposed methods.

To my parents and Biwei

ACKNOWLEDGMENTS

First I want to take this opportunity to express my deepest gratitude to my advisor, Dr. Peng Li. He gave me the opportunity to work with him initially. He patiently taught me the fundamentals and guided me into this research field. He is always willing to spend time working closely with me. It is always a pleasure to sit together with him and discuss challenging problems. Besides the tremendous help and support I received from Dr. Li in the academic world, he is also a mentor for my career and life. For all of these, thank you! Dr. Li.

I would like to thank my committee members, Dr. Walker and Dr. Hu. They spent time looking at my research work, pointed out possible issues, and provided me with challenging future directions.

Finally, I want to thank my parents and my wife, Biwei. They always believe in me no matter where I am and what I do. I gain my confidence from them. As I am crossing this very important milestone of my life, I thank their unconditional support and help.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

A. Introduction

Interconnect parasitics are the dominant source of on-chip circuit delays for modern VLSI technologies. To efficiently account for wire delays in the design process, interconnect modeling, particularly the model order reduction of passive linear networks, has been an active topic of research in CAD community for more than a decade (e.g. [1, 2, 3, 4]).

Asymptotic waveform evaluation (AWE) [1] uses moment matching technique to generate the reduced order model for the interconnect network. It uses 2q moments to generate a q pole transfer function approximation of the interconnect network. However, when applied to practical examples where a large number of dominant poles are needed, AWE may become less effective because of the ill-conditioning nature of the moment generation procedure. Krylov-subspace technique [2] is better numerically conditioned. But stability is still a problem, meaning the reduced-order model generated by the Krylov-subspace technique may have unstable poles, which could result in oscillation of the circuit response in practical cases. Passive reduced-order interconnect macromodeling algorithm (PRIMA) [3] is a projection based method which can guarantee the stability and passivity of the reduced order model. Compared with AWE. q-th order PRIMA approximation matches only q moments. PRIMA works especially well for the cases where high order reduced order models are needed. All these model order reduction techniques are for nominal case interconnect analysis, meaning they do not consider variations in the interconnect network.

_____

The journal model is *IEEE Transactions on Automatic Control.*

As modern VLSI technologies approach the nanoscale manufacturing regime, it is becoming increasingly difficult to control systematic/random fluctuations introduced in the fabrication process, leading to growing variations in the critical dimensions and material properties of metal and dielectric layers [5]. These process variations inevitably introduce performance variations in interconnects, which must be fully accounted for during timing verification. Hence, variational reduced-order interconnect models must be constructed to capture impacts of multiple variations accurately over a wide perturbation range. The need for addressing the nano-scale IC manufacturing reality necessitates the development of statistical analysis and optimization methodologies. However, the realization of such statistical frameworks such as SSTA critically relies on the availability of variation-based models for interconnects. The existing variational interconnect models are plagued by their inherent inefficiencies and/or high computational complexity that prevent them from being practically employed in newly developed statistical analysis frameworks. To realistically evaluate the variability in interconnects and its impact on circuit performance and yield, compact variational interconnect models must be developed to enable an affordable inclusion of the inter-die and intra-die process variations into statistical circuit simulation. The major challenge for achieving this goal lies in constructing compact variation-based interconnect models that are accurate over multiple and large-scale parametric variations, and at the same time, computational efficient.

B.   Contributions

A set of practical variation-aware interconnect analysis methodologies which can accurately and efficiently capture a wide range of variations of the interconnect delay and slew are proposed in this thesis. And some of the methods proposed in this the-

sis can find their applications in a much wider range of areas. For example, adjoint sensitivity analysis method is a general circuit analysis technique which can be used in many other areas such as circuit optimization, signal integrity and noise analysis.

The major contributions of this thesis are as follows:

- A practical variation-aware interconnect analysis methodology is presented to provide efficient delay and slew calculations for statistical timing analysis. In this approach, process variations of the interconnect network and input signal variations are translated into output delay and slew variations without extracting a "full-blown" variational reduced order model and subsequently performing sampling. While gaining improved efficiency by avoiding extracting a "full-blown" model, through a noticeable collection of technical deployments and numerical methods, we also avoid losing any significant accuracy in terms of delay and slew, which may be challenging to achieve via a purely delay/slew metric based approach.

- We propose to use adjoint sensitivity analysis method to construct the driving point model and compute driving point waveform. In our adjoint sensitivity analysis method, we use linearized MOSFET model to handle the driver of the interconnect net. The driving-point model is used with the linearized MOSFET model to calculate delay and slew at the driving point of the interconnect.

- We extend the classical adjoint sensitivity analysis method up to second order. Our method can capture much wider range of variations of the linear network compared with the original first order adjoint method. And we extend the application of adjoint sensitivity analysis from linear network to nonlinear circuits which makes this method more powerful.

Parts of the research work in this thesis have been published in [6, 7].

C. Thesis organization

This thesis is organized as follows:

Background In Chapter II, we introduce the concept, problem formulation and objective of variational interconnect analysis. Then a literature survey is given for some of the prior work of variational interconnect analysis.

Variational interconnect analysis In Chapter III, we present our methodology for variational interconnect analysis. First, we go through the overall analysis flow of our methodology. Then we explain each steps of our variational interconnect analysis in detail including: parametric moment computation, slew rate computation, parametric two-pole model and parametric high-order analysis. Parametric moment computation is based on a set of closed-form formulas which can compute the second order parametric moments efficiently. Parametric slew rate computation is based on the PERI metric [8]. And by clarifying "near-end node" and "far-end node" for the interested sink nodes, we use either parametric two-pole model for the former or parametric high-order model for the latter. And we then convert the variation in the output response at a certain time point into the variation in delay, by doing so we avoid using nonlinear iterations over a large number of circuit instances to find the delay variation.

Driving point model and adjoint sensitivity analysis In Chapter IV, we first go through the basic ideas of driving point pi model construction. Then we introduce first order adjoint sensitivity analysis method, its origin, derivation and application in the interconnect analysis. Then we present the procedures of using driving point pi model and adjoint sensitivity analysis method to computing the driving point waveform and its sensitivities with respect to variation sources. This driving point waveform can then be propagated by using the methods in Chapter III to complete

the variation-aware interconnect analysis flow.

Conclusion In Chapter V, I conclude this thesis with the discussions of the methods presented in this thesis and future directions of this research topic.

CHAPTER II

BACKGROUND

As integrated circuit feature sizes continue to scale into the sub-100nm regime, the number of transistors incorporated on a chip are above one billion [9]. Meanwhile, the amount of interconnect is growing with the transistor counts. Due to the die size limitation, interconnect dimensions are scaling down with the feature sizes. Therefore, the relative error of variations introduced during the fabrication step will have more and more effect on the performance of integrated circuits. It is imperative to consider variation effects on the circuit performance during the circuit simulation/modeling/optimization to provide meaningful results.

A. Objective of variational interconnect analysis

Statistical static timing analysis (SSTA) [10, 11, 12, 13] has been recently proposed to handle variability during timing verification of integrated circuits. Instead of using one fixed delay values for gates, SSTA uses first/second order canonical delay models which take into account correlated/random variations during the timing verification. By traversing the timing graph of the circuit in a breadth-first manner, canonical delay expressions are propagated from source nodes to sink nodes. During the propagation, there are two atomic operations needed: *sum* and *max*. The *max* operation in [10, 11, 13] are based on Clark's algorithm [14], the *max* operation in [12] is based on moment matching technique. First order SSTA uses the canonical first order expression 2.1 for all the gate delays, arrival times, required arrival times, slacks and slews:

$$T_d = T_{d,0} + \alpha_d^T \rho, \tag{2.1}$$

where $T_{d,0}$ is the nominal delay, $\rho = [\rho_1, \rho_2, \cdots, \rho_{N_\rho}]^T$ represent N_ρ principal components of variation sources [1], α_d is a $N_\rho \times 1$ vector representing the first order sensitivities with respect to principal components.

Some recent work about statistical static timing analysis also use the second order canonical expression 2.2 for the gate delays etc.

$$T_d = T_{d,0} + \alpha_d^T \rho + \rho^T \Gamma_d \rho, \tag{2.2}$$

where $T_{d,0}$ is the nominal delay, $\rho = [\rho_1, \rho_2, \cdots, \rho_{N_\rho}]^T$ represent N_ρ principal components of variation sources, α_d is a $N_\rho \times 1$ vector representing the first order sensitivities with respect to principal components, Γ_d is a $N_\rho \times N_\rho$ matrix representing the second order sensitivities with respect to second order variation terms. Since second order canonical expression 2.2 is essentially a higher order Taylor series expansion of the delay, it is more accurate than the first order canonical expression, especially for the cases where variation ranges are large. In this thesis, I use the second order canonical expression for most of the timing/intermediate quantities during the circuit analysis.

Fig. 1 illustrates a simple combinational circuit. In most of the existing SSTA work, gate/wire delays are propagated from input to output pins. First/second order gate delay model can be extracted from SPICE simulation. But delay model for wires can not be easily extract from SPICE simulation. [13] suggests to use Elmore delay model to estimate the wire delay, which is essentially the first order moment of the impulse response. From the timing verification perspective, Elmore delay is not accurate enough. So interconnect delay model which is accurate and easy to generate

---

[1]Principal component analysis (PCA) is used to transfer the original set of correlated random variables into an uncorrelated set of principal components ρ
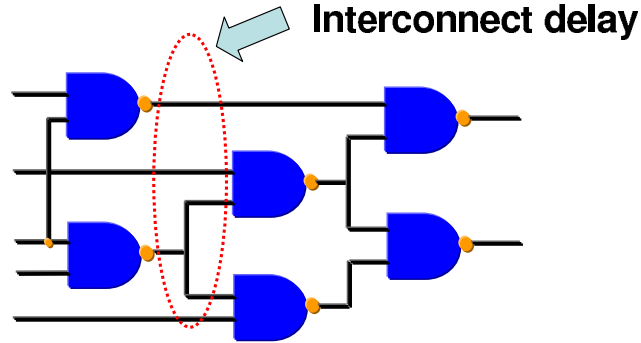
Fig. 1. Number of extra adjoint circuit run equals to number of parameters.

and at the same time can be facilitated into the statistical timing analysis flow is desired. One of the major objectives of variational interconnect analysis in this thesis is to build the second order canonical delay/slew model for the interconnects.

There are many other applications where variational interconnect analysis can be utilized. For example, in the wire sizing problem, circuit designers want to find the optimal wire size parameters to meet some given timing constraints. If the sensitivities of the wire delay/slew with respect to design parameters can be computed, circuit designers can easily find out which design parameter can be changed in order to meet the timing constraint. In this particular optimization problem, variational interconnect analysis is served as an simulation engine which needs to be called again and again during the optimization loop. So the efficiency of variational interconnect analysis is also very important.

B.   Prior work

In the past, a significant amount of work has emerged to address interconnect variability via various avenues through variational interconnect model order reduction [15, 16, 17, 18, 19, 20, 21], or via statistical/variational interconnect analysis [19, 22, 23].

While the above approaches are instrumental in terms of providing principles and methodologies for variational reduced-order modeling of dynamical systems and statistical circuit analysis, practical challenges still need to be addressed under the context of timing analysis. Modern chip designs contain an overwhelmingly large number of interconnect networks that must be analyzed efficiently. As such, efficiency of variational interconnect analysis is ultimately crucial to facilitate an feasible statistical timing flow. To this end, it is worth noting that general variational reduced interconnect models do not directly offer the standard timing measures, namely, delay and slew, as well as their variability, which are needed in existing timing analysis flows [10, 11]. The variational model order reduction in [15] is based on two projection-based model order reduction techniques: PRIMA [3] and PACT [24]. And the variational analysis in [15] is based on matrix perturbation theory [25]. [16, 17] are based on the balanced truncation technique. However, standard timing quantities such as delay and slew are not calculated. A significant cost will be incurred in order to evaluate the reduced-order models over a large number of samples to provide such delay and slew statistics, thereby making the cost of statistical timing analysis intractable. [22] first calculates the circuit moments under variation, then moments are mapped to delay metrics in order to get the circuit delay under variation. Physical synthesis oriented delay/slew metrics are extremely efficient, however, they are not completely suitable to accurate timing verification. These metrics tend to give inaccurate delay estimation, especially for near-end nodes in the interconnect network, making it more difficult to apply for capturing delay variations.

C.   Overview of our approach

Given a RC network with a single input, N circuit nodes and N_s sink nodes, the objective of our approach is to compute the delay $T_{d,i}$ and slew rate $T_{s,i}$ at sink node i, $i = 1...N_s$ while considering the variations of RC elements due to a set of N_ρ process variables, $\rho = [\rho_1, \rho_2, \cdots, \rho_{N_\rho}]^T$ and the input variation, modeled as variation in the input slew. Without loss of generality, delay and slew are defined as 50% propagation delay and 20-80% slew time, respectively. To be accurate over a wide range of process variations, each delay is expressed in terms of a second order polynomial in process variables $\rho'_i s$ as

$$T_d = T_{d,0} + \alpha_d^T \rho + \rho^T \Gamma_d \rho, \tag{2.3}$$

where $T_{d,0}$ is the nominal delay, α_d is a $N_\rho \times 1$ vector representing the first order delay sensitivities, Γ_d is a $N_\rho \times N_\rho$ matrix representing the second order terms. For the same purpose, the 2nd-order parametric form is used as a standard form to represent most of circuit quantities during the analysis.

CHAPTER III

VARIATIONAL INTERCONNECT ANALYSIS

In Chapter III, we present a practical interconnect analysis methodology to provide efficient delay and slew calculation for statistical timing analysis. In this approach, process and input signal variations are propagated into the output delay and slew variations without computing a complete variational reduced order model and performing subsequent statistical sampling as some of the existing approaches did. Fig. 2 uses a simple RC interconnect nets to illustrate the problem definition.

While gaining improved efficiency by avoiding computing the complete variational reduced order models, we also develop specific techniques to avoid losing any significant accuracy in delay and slew variations, which is difficult to achieve by delay/slew metric based approaches. As a standard practice, we assume that an accurate nominal-case interconnect analysis technique such as high-order AWE [1, 26] is used for the nominal timing verification, as part of a variational interconnect analysis flow. Based on the result of the nominal timing analysis, each circuit node under analysis will be identified either as a "far-end" or a "near-end" node. For both, a "small-scale" parametric reduced order model will be computed. The avenue for doing so will be through fast closed-form formulas for the former and efficient perturbation analysis method for the latter. It is shown that the proposed techniques offer accurate variational interconnect delay and slew computation over a wide range of process variations, regardless of the nature of circuit nodes (e.g. far ends vs. near ends). It directly produces parametric expressions of delay and slew in the underlying process variables, and hence constitutes a useful analysis infrastructure for statistical timing analysis.
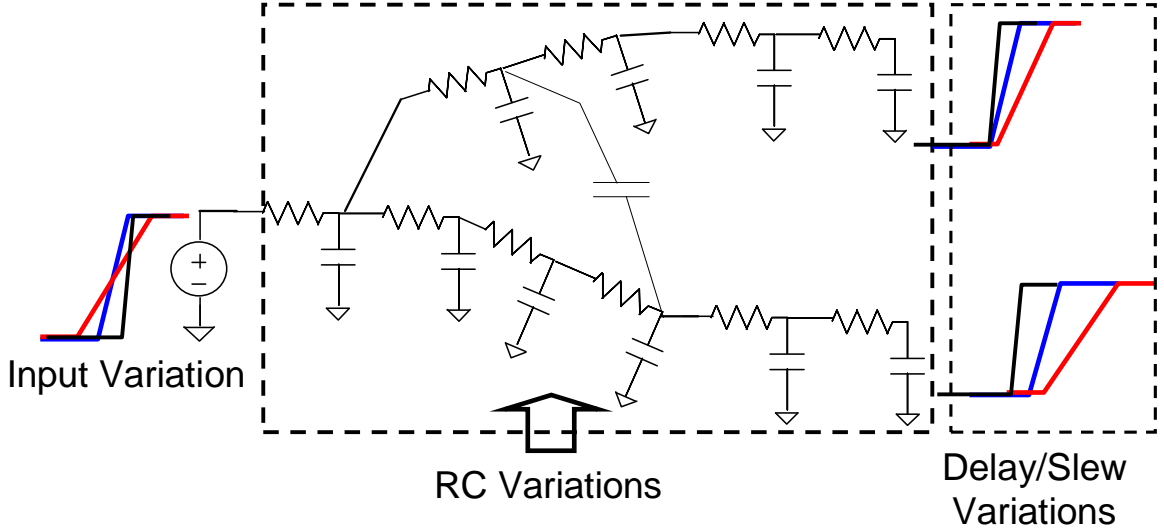
Fig. 2. Propagation of RC and input variations.

A.   Analysis flow

In order to capture a wide range of process variations, every timing quantity is expressed in terms of a second order polynomial in process variables $\rho_i's$ as

$$T = T_0 + \alpha_d^T \rho + \rho^T \Gamma_d \rho, \tag{3.1}$$

where T_0 is the nominal value, α_d is a $N_\rho \times 1$ vector representing the first order sensitivities with respect to variations, Γ_d is a $N_\rho \times N_\rho$ matrix representing the second order sensitivities with respect to variations.

The input slew can be dependent on the same or different set process parameters since it is impacted by the preceding driving stage. For simplicity of notation, we include all the process parameters in ρ. In this fashion, the statistical correlation between different circuit stages can be naturally captured. It should be noted that upon getting these parametric forms, the statistical distributions of delay and slew can be easily obtained by propagating distributions of the underlying process parameters

through these quadratic expressions. As the dependency of timing quantities on process variation is kept, these parametric forms can be directly incorporated into a statistical timing analysis flow [10, 11, 12, 13].

The proposed analysis flow is outlined in Fig. 3. The variational interconnect analysis follows the accurate high-order AWE analysis applied for the nominal case. By examining the poles and residues of the nominal case AWE model, a sink node can be identified as a "near end" or a "far end" node. Here, a node is said to be near end if the AWE model has two obviously dominant pairs of poles and residues such that a two-pole model will be sufficient for analyzing delay and slew. Based on the parametric moment computation, parametric output slews are obtained by extending the existing moment-based nominal slew metric while considering the input slew variations [8, 27]. To more reliably compute the delay, a parametric two-pole (for "far" end nodes) or high order reduced model (for "near" end nodes) is computed. Finally, parametric forms of the delay is generated by evaluating the parametric reduced model. The efficiency of the proposed approach is archived by adopting a) an efficient variational transfer function moments computation procedure; b) a simple and yet accurate (parametric) moment-based slew metric; c) efficient closed-form formulas (far-end nodes) and numerically efficient perturbation analysis (near-end nodes) for variational delay analysis. In Fig. 3, shaded steps are performed using closed-form formulas while others are achieved using efficient numerical computation. Each of these steps is described in details as follows.
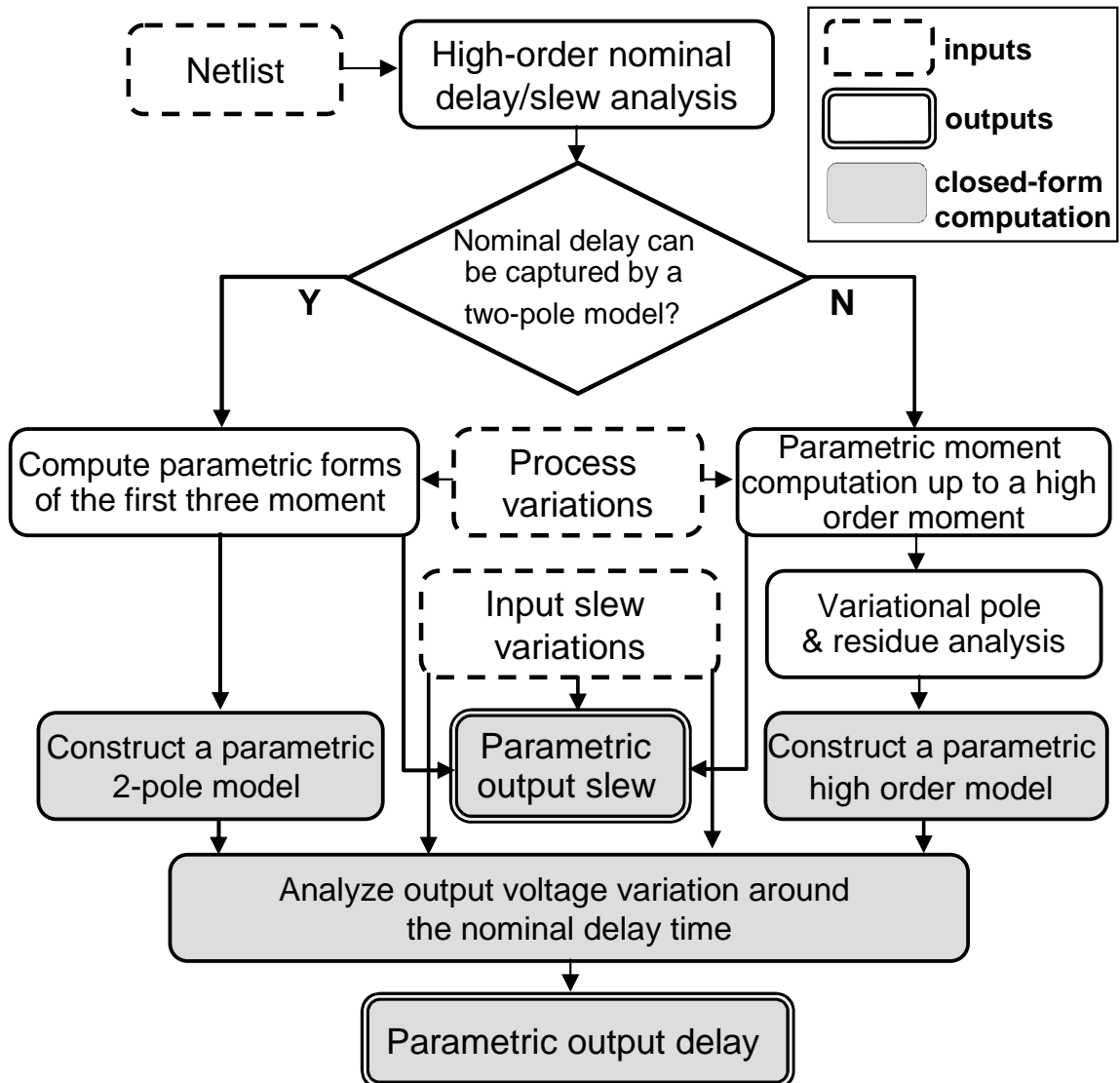
Fig. 3. Variational delay and slew computation.

B.   Parametric moment analysis

An RC network with a single voltage input can be described using the following system equations

$$C\frac{dx}{dt} + Gx = bu, \ y = L^T x, \tag{3.2}$$

where $G, C \in \mathbf{R}^{N \times N}$ are the conductance and capacitance matrices, u is the voltage source, $x \in \mathbf{R}^{N \times 1}$ is the unknown vector consisting of the node voltages and the voltage source current, $b \in \mathbf{R}^{N \times 1}$ is a vector linking the input to the RC circuit, and $L \in \mathbf{R}^{N \times M}$ is the output matrix used to select the sink node voltages $y \in \mathbf{R}^{M \times 1}$ from x. Throughout this paper, the notation (G, C, b, L) is used to denote a single-input RC network commonly encountered in timing analysis.

Variations of G and C matrices are modeled by quadratic dependency on the process parameters ρ. Without loss of generality, we only consider a linear dependency for simplicity of notation as follows

$$G = G_0 + \sum_{i=1}^{N_\rho} G_i \rho_i, \ C = C_0 + \sum_{i=1}^{N_\rho} C_i \rho_i, \tag{3.3}$$

where G_i and C_i are sensitivity matrices and can be obtained during the parasitics extraction. The zero-th order moment of a RC network without any grounded resistance is given by $m^0 \in \mathbf{R}^{N \times 1}$ is given as $m^0 = G^{-1} b = [1 \ 1 \cdots 1 \ 0]^T$ regardless of process variations. In the following, the quadratic parametric forms of the next three moments are derived.

The quadratic parametric form of the ith order moment $m^i \in \mathbf{R}^{N \times 1}$ vector is represented in the following form

$$m^i = m_0^i + \sum_{j=1}^{N_\rho} \alpha_j^i \rho_j + \sum_{j=1}^{N_\rho} \sum_{k=1}^{N_\rho} \gamma_{j,k}^i \rho_j \rho_k, \tag{3.4}$$

where m_0^i is the nominal value, $\alpha_j^i \in \mathbf{R}^{N \times 1}$ and $\gamma_{j,k}^i \in \mathbf{R}^{N \times 1}$ are the first and second

order coefficients. Since circuit moments are computed recursively in an ascending order, it will suffice to show how the next moment vector m^{i+1} is computed given m^i. Assuming that the parametric form of m^i as in (3.4) is available, m^{i+1} can be obtained as

$$m^{i+1} = -G^{-1}Cm^i = -(G_0 + \sum_{i=1}^{N_\rho} G_i \rho_i)^{-1}(C_0 + \sum_{i=1}^{N_\rho} C_i \rho_i)m^i, \tag{3.5}$$

where the matrix inversion can be expanded using Taylor series since the perturbation term is assumed to be small

$$
(G_0 + \sum_{i=1}^{N_\rho} G_i \rho_i)^{-1} = \Big(I - \sum_{i=1}^{N_\rho} G_i \rho_i + (\sum_{i=1}^{N_\rho} G_i \rho_i)^2
$$
$$
- (\sum_{i=1}^{N_\rho} G_i \rho_i)^3 + \cdots \Big) G_0^{-1}. \tag{3.6}
$$

Substituting (3.4) and (3.6) into (3.5) and retaining only up to the quadratic terms gives

$$m^{i+1} = m_0^{i+1} + \sum_{j=1}^{N_\rho} \alpha_j^{i+1} \rho_j + \sum_{j=1}^{N_\rho} \sum_{k=1}^{N_\rho} \gamma_{j,k}^{i+1} \rho_j \rho_k, \tag{3.7}$$

where

$$
\begin{aligned}
m_0^{i+1} &= -G_0^{-1} C_0 m_0^i \\
\alpha_j^{i+1} &= G_0^{-1} G_j G_0^{-1} C_0 m_0^i - G_0^{-1} C_0 \alpha_j^i - G_0^{-1} C_j m_0^i \\
\gamma_{j,k}^{i+1} &= \gamma_{j,k}^{i+1,1} + \gamma_{j,k}^{i+1,2}.
\end{aligned} \tag{3.8}
$$

In (3.8), the second order coefficient $\gamma_{j,k}^{i+1}$ is split into two parts which are given by

$$
\begin{aligned}
\gamma_{j,k}^{i+1,1} &= -G_0^{-1} G_j G_0^{-1} G_k G_0^{-1} C_0 m_0^i + G_0^{-1} G_j G_0^{-1} C_0 \alpha_k^i \\
&\quad - G_0^{-1} G_j G_0^{-1} C_k m_0^i - G_0^{-1} C_k \alpha_j^i,
\end{aligned} \tag{3.9}
$$

$$\gamma_{j,k}^{i+1,2} = -G_0^{-1} C_0 \gamma_{j,k}^i, \tag{3.10}$$

where the second order coefficient $\gamma_{j,k}^i$ (for $\rho_j\rho_k$) of m^i is defined recursively as in (3.8). For the zero-th order moment m^0, it is true that $\alpha_j^i = \gamma_{j,k}^0 = 0$.

A few key observations are due here. Starting from $m^0 = G^{-1}b = [1\ 1\cdots 1\ 0]^T$, the parametric forms of the first few moments can be computed using (3.5, 3.8, 3.9, 3.10). As in (3.4), the N_ρ sensitivity vectors α_j^i's can be computed using the standard sensitivity analysis, achievable by reusing the LU factor of G_0 or applying path tracing (RICE [26]) with mild computational cost. The large number $(O(N_\rho^2))$ of second order coefficients are more expensive to compute in (3.4). To speedup, we exploit the observation: in a typical RC signal net, the number of sink nodes, N_s, is typically much less than the number of circuit unknowns N. Hence, efficiency of analysis can be improved if the second order analysis is only conducted for the sink nodes. In our implementation, the nominal moments and first-order sensitivity vectors are computed for all N circuit nodes while the second order coefficients are only computed for N_s sink nodes. As an example, let us consider the term in (3.10). Instead of computing the complete $\gamma_{j,k}^{i+1,2}$, we seek the entries of the sink nodes of interest. We multiply $\gamma_{j,k}^{i+1,2}$ with L^T ($L \in \mathbf{R}^{N\times N_s}$) from left to select just what corresponds to N_s sink nodes

$$L^T\gamma_{j,k}^{i+1,2} = -L^T G_0^{-1} C_0 \gamma_{j,k}^i = \Phi^T \gamma_{j,k}^i, \tag{3.11}$$

where $\Phi = -\Theta^T C_0$ and $\Theta = (G_0^T)^{-1}L$ is obtained via solving the adjoint linear system defined by G_0^T by reusing the same LU factor of G_0. Considering only N_s sink nodes changes the cost from $O(N_\rho^2)$ linear system solutions/matrix-vector multiplications to $O(N_s N_\rho^2)$ vector inner products. When N_s is small, the latter can be performed faster using vector operations. It should be noted in evaluating (3.11), vector $\gamma_{j,k}^i \in \mathbf{R}^{N\times 1}$ is not formed directly either since there exist also $O(N_\rho^2)$ of them. Instead, $\Phi^T \gamma_{j,k}^i$ is evaluated.

C. Slew rate computation

The variation of the slew at any given sink node say, j, is analyzed based on the parametric moments computed in the previous section. Here, slew is computed on a per sink node basis, thus it only involves scalar computations while considering parametric variations. Unlike delay computation, there do exist simple moment-based slew metrics that are accurate for both the near and far end nodes [28, 29].

In [8], the PERI metric is used to estimate the sink node slew for a given input slew

$$slew_{ramp} = \sqrt{slew_{step}^2 + slew_{input}^2},$$
(3.12)

where $slew_{input}$ is the slew of the ramp input, $slew_{step}$ is the output slew for a step input, and $slew_{ramp}$ is the output slew for the ramp input. It is shown that the above metric can correlate fairly accurately the ramp input slew with the output slew if an accurate metric for $slew_{step}$ is used. In this paper, it is assumed that the nominal output slew $slew_{ramp}^0$ has been accurately obtained. Then, the variation of $slew_{step}$ around $slew_{step}^0$ is estimated as

$$slew_{step} = \frac{m_j^1 \cdot slew_{step,0}}{m_{j,0}^1},$$
(3.13)

where m_j^1 and $m_{j,0}^1$ are first order moment and its nominal value at the sink node j. In the above, the (variational) Elmore delay of the node is normalized with respect to the nominal slew to provide a variational step-input slew metric. Let us assume that the variational forms of $slew_{in}$ and $slew_{step}$ are cast into

$$slew_{in} = \alpha_i + \beta_i^T \rho + \rho^T \Gamma_i \rho, \;\; slew_{step} = \alpha_s + \beta_s^T \rho + \rho^T \Gamma_s \rho,$$
(3.14)

where α_i and α_s are scalars, β_i^T and β_s^T are $N_\rho \times 1$ vectors, Γ_i and Γ_s are $N_\rho \times N_\rho$ matrices. Substituting (3.14) into (3.12) and expanding about the nominal ramp-

input output slew gives the following variational form of $slew_{ramp}$

$$slew_{ramp} = \sqrt{\alpha_s^2 + \alpha_s^2}(1 + \beta_r^T \rho + \rho^T \Gamma_r \rho), \qquad (3.15)$$

where

$$\begin{aligned} \beta_r &= \frac{\alpha_i \beta_i + \alpha_s \beta_s}{\alpha_i^2 + \alpha_s^2} \\ \Gamma_r &= \frac{\beta_i \beta_i^T + \beta_s \beta_s^T + 2(\alpha_i \Gamma_i + \alpha_i \Gamma_i)}{2(\alpha_i^2 + \alpha_s^2)} - \frac{1}{8}\beta^T \beta_r^T. \end{aligned} \qquad (3.16)$$

We have found in our experiments that the above variational slew metric is very accurate. It is also possible to use the two-moment slew metric proposed in [28]. The computation of the parametric form of the output slew can be similarly conducted.

D. Variational delay analysis

Unlike the slew analysis, simple moment-based interconnect delay metrics tend to be inaccurate for near end nodes, making it not completely suitable for variation analysis. We propose to analyze the output voltage response variation at the nominal delay point (e.g. $50\%V_{dd}$ crossing point) and then convert the variation in response to variation in delay.

As shown in Fig. 3, each sink node is identified either as a "near" end node or a "far" end node by examining the results of the nominal analysis. For a "far" end node, a parametric two-pole AWE model is constructed to evaluate its voltage response variation while for a "near" end node, perturbation analysis of poles and residues is conducted to construct a more accurate parametric high-order AWE model. The strategy here is that majority of nodes (those are of far-end in nature) can be processed rather efficiently using simple two-pole models and a smaller number of near-end nodes are analyzed using high-order models. When using only the nominal

analysis result to decide the nature of a sink node, we have assumed that process variations do not make a near-end node behave like a far-end node and vice versa. This is a quite reasonable assumption since for bounded process variations the nature of a circuit node is determined by its location. For an arbitrary sink node, let us assume that a set of N_r pole and residue pairs, $p_{nom,i}$ and $k_{nom,i}$ are computed in an accurate high-order AWE analysis used for the nominal case timing analysis. From this analysis, the nominal $50\%V_{dd}$ crossing time is assumed to be t_{nom}. Then, the portion of output response at time t_{nom} attributed to the two most dominant low frequency poles, say, $p_{nom,1}$ and $p_{nom,2}$, is computed as V_l. For a given user-specified tolerance ε ($\varepsilon < 1$), the sink node is identified as a far-end node if

$$|0.5V_{dd} - V_l| < 0.5\varepsilon V_{dd}. \tag{3.17}$$

Otherwise, it is identified as a near-end node.

1. Parametric two-pole model

We describe how a parametric two-pole model can be efficiently constructed for far-end nodes. A second order AWE model parameterizable in the same quadratic parametric form is computed. This goal can be achieved by propagating the parametric moment expressions derived in the previous sections though the moment matching procedure. Since the order of moment matching is low, it is possible to derive closed-form formulas. As an example, let us consider the characteristic function of a 2nd order AWE model

$$b_2 p^2 + b_1 p + 1 = 0, \tag{3.18}$$

where b_1 is determined by the moment matching process using circuit moments

as $b_1 = \frac{-m_0 m_3 + m_1 m_2}{m_0 m_2 - m_1^2}$. Notice that the parametric form of these moments can be computed using the procedure described in the previous sections. Denote the parametric expressions for the first four moments as

$$m_i = \alpha_{m,i} + \beta_{m,i}^T \rho + \rho^T \Gamma_{m,i} \rho, i = 0, 1, 2, 3. \tag{3.19}$$

Substituting (3.19) into (3.18) and keeping up to the 2nd order parametric terms gives

$$b_1 \approx \frac{f_1}{f_2}, \tag{3.20}$$

where

$$
\begin{aligned}
f_1 &= (\alpha_{m,1}\alpha_{m,2} - \alpha_{m,0}\alpha_{m,3}) + \\
&\quad (\alpha_{m,1}\beta_{m,2}^T + \alpha_{m,2}\beta_{m,1}^T - \alpha_{m,0}\beta_{m,3}^T)\rho + \\
&\quad \rho^T(\alpha_{m,1}\Gamma_{m,2} + \beta_{m,1}\beta_{m,2}^T + \alpha_{m,2}\Gamma_{m,1} - \alpha_{m,0}\Gamma_{m,3})\rho,
\end{aligned} \tag{3.21}
$$

$$
\begin{aligned}
f_2 &= (\alpha_{m,0}\alpha_{m,2} - \alpha_{m,1}^2) + (\alpha_{m,0}\beta_{m,2}^T - 2\alpha_{m,1}\beta_{m,1}^T)\rho + \\
&\quad \rho^T(\alpha_{m,0}\Gamma_{m,2} - 2\alpha_{m,1}\Gamma_{m,1} - \beta_{m,1}\beta_{m,1}^T)\rho.
\end{aligned} \tag{3.22}
$$

Here, b_1 is in the form of a ratio of two quadratic forms. In our implementation, analytical expressions have been derived to convert such a ratio into a standard quadratic form. Going though similar derivations, b_2 as well as two pole/residue pairs of the two-pole model, k_1, p_1, k_2, p_2, can be obtained in the same parametric quadratic form. Essentially, by passing parametric moments to a set of pre-stored closed-form formulas, a parametric two-pole model can be computed very efficiently for any given

circuit node.

2. Parametric high-order model

For sinks that are identified as near-end nodes, a two-pole model is not accurate enough to analyze the variation in the voltage response. Instead, we seek an accurate parametric high-order AWE model. The order of parametric model can be set to what is used in the nominal case timing analysis. Unlike a simple two-pole model, it is not possible to derive closed-form expressions to relate the circuit moments to a high order model. Hence, we first numerically compute the parametric variations of the characteristic function of the AWE model and then perform perturbation analysis on system poles and residues to produce the desired parametric model. Without loss of generality, consider the correspondence between the circuit moments and the coefficients of the characteristic function in a 4-th order AWE model

$$
\begin{bmatrix} m_0 & m_1 & m_2 & m_3 \\ m_1 & m_2 & m_3 & m_4 \\ m_2 & m_3 & m_4 & m_5 \\ m_3 & m_4 & m_5 & m_6 \end{bmatrix} \begin{bmatrix} b_4 \\ b_3 \\ b_2 \\ b_1 \end{bmatrix} = - \begin{bmatrix} m_4 \\ m_5 \\ m_6 \\ m_7 \end{bmatrix}. \tag{3.23}
$$

To simplify the notation, we denote the Hankel matrix in the above equation as F, its nominal matrix as F_0, its first sensitivity w.r.t the i-th process variable ρ_i as F_i and its second order dependency on $\rho_i\rho_j$ as $F_{i,j}$. Notice that F_i and $F_{i,j}$ can be obtained by replacing each moment in F by its first order sensitivity w.r.t ρ_i and second order dependency w.r.t $\rho_i\rho_j$, respectively. We further denote $[b_4\ b_3\ b_2\ b_1]^T$ as $\mathtt{b}$, $[m_4\ m_5\ m_6\ m_7]^T$ as $\mathtt{m}$, and their nominal values as $\mathtt{b_0}$ and $\mathtt{m_0}$, respectively. We define $\mathtt{b_i}$, $\mathtt{m_i}$, $\mathtt{b_{i,j}}$ and $\mathtt{m_{i,j}}$ as in the case of F. A standard sensitivity analysis gives
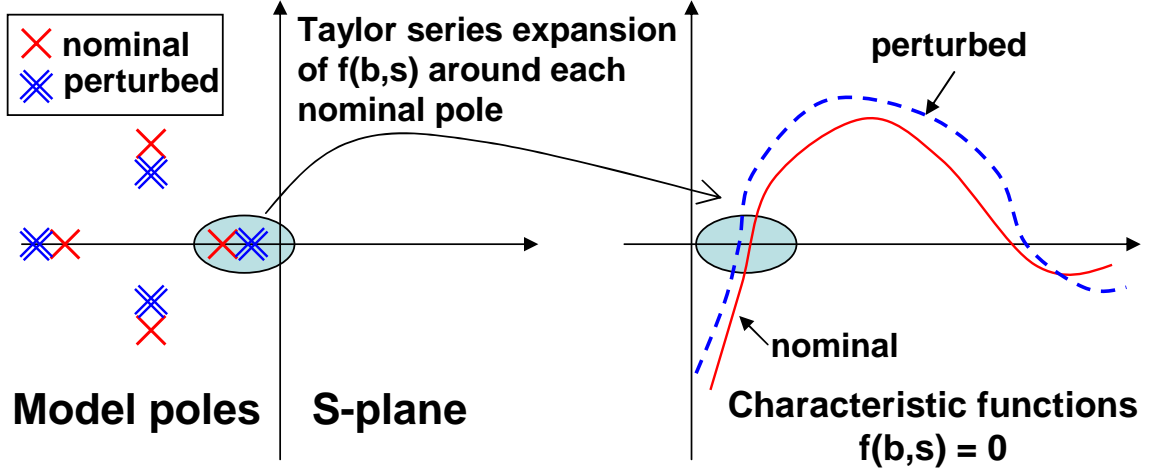
Fig. 4. Perturbation analysis of model poles.

$$\mathtt{b_i} = F_0^{-1}(-\mathtt{m_i} - F_i \mathtt{b_0}). \qquad (3.24)$$

Matching the second order terms from the both sides of (3.23) leads to

$$\mathtt{b_{i,j}} = F_0^{-1}(-\mathtt{m_{i,j}} - F_i \mathtt{b_j} - F_{i,j} \mathtt{b_0}). \qquad (3.25)$$

Using the parametric moments already computed, the parametric forms of $\mathtt{b}$ can be obtained by solving multiple linear matrix problems defined by the nominal Hankel matrix.

With the parametric dependency of the characteristic function (defined by $\mathtt{b}$) computed, we proceed to analyze the variation of the system poles. For general high-order models, no closed-form expressions are available for poles. To make the problem of analyzing parametric variations of transfer function poles tractable, perturbation analysis is applied in the neighborhood of each nominal model pole, as illustrated in Fig. 4.

To capture the variation of a pole of the high-order AWE model around its

nominal value, say $p_{nom,i}$, the characteristic function

$$f(\mathbf{b}, s) = 1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 = 0 \tag{3.26}$$

is expanded into a quadratic function at $s = p_{nom,i}$ as

$$f(\mathbf{b}, \Delta p_i) = q_0 + q_1 \Delta p_i + q_2 \Delta p_i^2 = 0, \tag{3.27}$$

where, Δp_i is the variation of the i-th pole and

$$
\begin{aligned}
q_0 &= 1 + b_1 p_{nom,i} + b_2 p_{nom,i}^2 + b_3 p_{nom,i}^3 + b_4 p_{nom,i}^4 \\
q_1 &= b_1 + 2b_2 p_{nom,i} + 3b_3 p_{nom,i}^2 + 4b_4 p_{nom,i}^3 \\
q_2 &= b_2 + 3b_3 p_{nom,i} + 6b_4 p_{nom,i}^2.
\end{aligned}
\tag{3.28}
$$

Notice that since $\mathbf{b}$ has parametric variations, q_0 in (3.28) is not necessarily zero. Using the parametric expressions of $\mathbf{b}$, $q_i's$ in the above equation can be cast in the following quadratic forms in the process variables

$$q_i = q_{i,0} + q_{i,1}^T \rho + \rho^T Q_{i,2} \rho \tag{3.29}$$

Plugging $\Delta p_i = p_{i,1}^T \rho + \rho^T P_{i,2} \rho$ into (3.27) gives

$$p_{i,1} = -q_{0,1}/q_{1,0}, \ P_{i,2} = -(q_{0,2} + q_{1,1} p_{i,1}^T + q_{2,0} p_{i,1} p_{i,1}^T)/q_{1,0}. \tag{3.30}$$

After the perturbation analysis is completed for all poles, the resulting parametric expressions are employed to compute the parametric forms of residues $(k_i's)$ that leads to a complete parametric circuit model. Given a N_m-th order parametric model, the variation of the time-domain voltage response $y(t)$ at any time t under a saturated ramp input can be evaluated using

$$
\begin{aligned}
y(t) \;=\; & \sum_{i=1}^{N_m} \frac{a k_i}{p_i^2} [(-1 - p_i t + e^{p_i t}) U(t) - \\
& (-1 - p_i(t - t_1) + e^{p_i(t - t_1)}) U(t - t_1)],
\end{aligned}
\tag{3.31}
$$

where a is the slope of the ramp input, $t_1 = V_{dd}/a$, and $U(\cdot)$ is the step function. Utilizing the parametric poles/residues, expanding $y(t)$ around its nominal value leads to a second order parametric expression of the voltage response.

E. Delay variation

In the nominal case delay analysis, typically, a reduced order model is computed to obtain the analytical solution of the voltage response at a sink node under the saturated ramp input. To find the output delay, nonlinear Newton iterations are applied to find the time t_{nom} at which the output voltage crosses $50\% V_{dd}$. However, applying nonlinear iterations over a large number of circuit instances to find the delay variation is prohibitively expensive. To facilitate a feasible variational delay analysis, in our approach, we convert the variation in the output response at t_{nom}, namely, ΔV, to the variation in delay. As shown in Fig. 5, the rationale behind is that although finding a particular voltage crossing point is intrinsically difficult, evaluating variation of the response at a given time is rather straightforward. The latter is achieved by using the parametric two-pole or high-order AWE model developed in the previous sections.

To this end, two fixed time points t_a and t_b are selected in the neighborhood of t_{nom}: $t_a < t_{nom} < t_b$. The voltage response at these two points can be similarly obtained from the parametric model computed previously. The slope of the voltage response around t_{nom} can be approximated as
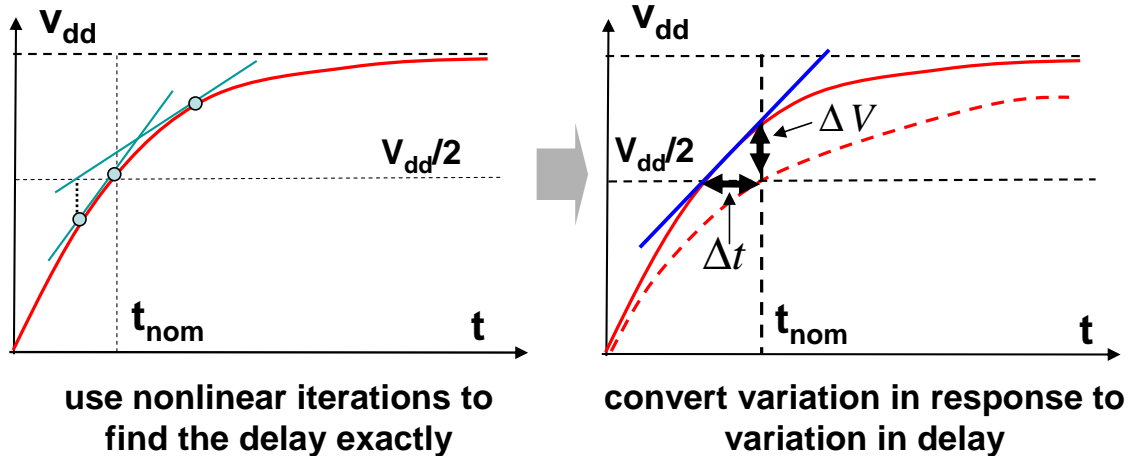
Fig. 5. Avoiding nonlinear iterations by converting voltage response variation to delay variation.

$$slope(t_{nom}) = \frac{y(t_b) - y(t_a)}{t_b - t_a}. \tag{3.32}$$

Using (3.32), the delay variation is estimated as

$$t_d = t_{nom} - \frac{\Delta V(t_b - t_a)}{y(t_b) - y(t_a)}, \tag{3.33}$$

which can be finally converted to a standard quadratic parametric form. It should be noted that in (3.33) the variation of $slope(t_{nom})$ is also reflected in the delay variation.

F. Experimental results

We first demonstrate the accuracy issue of variational interconnect analysis using two circuit examples. In Fig. 6, a ramp input is applied to a RC circuit and a far end node is selected to examine the voltage response. We compare the direct transient simulation and the 2nd order AWE model for the original circuit and the perturbed circuit where RC values are varied to mimic the impact of process variation. As

can be seen, for this far end node the 2nd order AWE model is very accurate for both the original circuit and the perturbed one. Therefore, it is well expected that delay/slew variation can be accurately captured if a parametric 2nd order AWE model is extracted. We conduct a similar comparison for a near end node selected from another RC circuit in Fig. 7. This near end node is located close to the driving voltage input therefore resistive shielding effect is noticeable in this case. It is clearly seen that the 2nd order AWE model cannot capture well the variation of the output response. However, a 4th order model can. This implies that for near end nodes, delay/slew variations cannot be well captured by a low order model. For a case like this, the perturbation analysis will be invoked in the proposed variational analysis flow to produce a high-order parametric model to ensure the accuracy.

Next, we demonstrate the accuracy of the proposed analysis on a near-end node chosen from a RC circuit with 124 nodes and 234 RC elements, as shown in Fig. 8 and Fig. 9. This circuit is driven by a saturated ramp signal with a nominal input slew rate of 200ps. 10 independent RC variation sources are considered so is the variation in the input slew. In practice, near end nodes are usually difficult to estimate using moment-based delay metrics. However, in the proposed technique, this node is identified to be a near-end node in the nominal case timing analysis. When performing the variational analysis, the perturbation analysis is invoked to generate a 4-th order parametric AWE model and the quadratic parametric forms are computed for delay and slew. 500 circuit samples are randomly generated and we directly compute the output delay and slew of each sample by applying transient analysis. For comparison, the parametric delay and slew expressions obtained from our proposed technique are evaluated for these 500 circuit samples. In Fig. 8 and Fig. 9, the relative errors of delay and slew of the proposed variational technique are shown. In this case, the maximum errors are 4.2% and 2.7% for delay and slew,
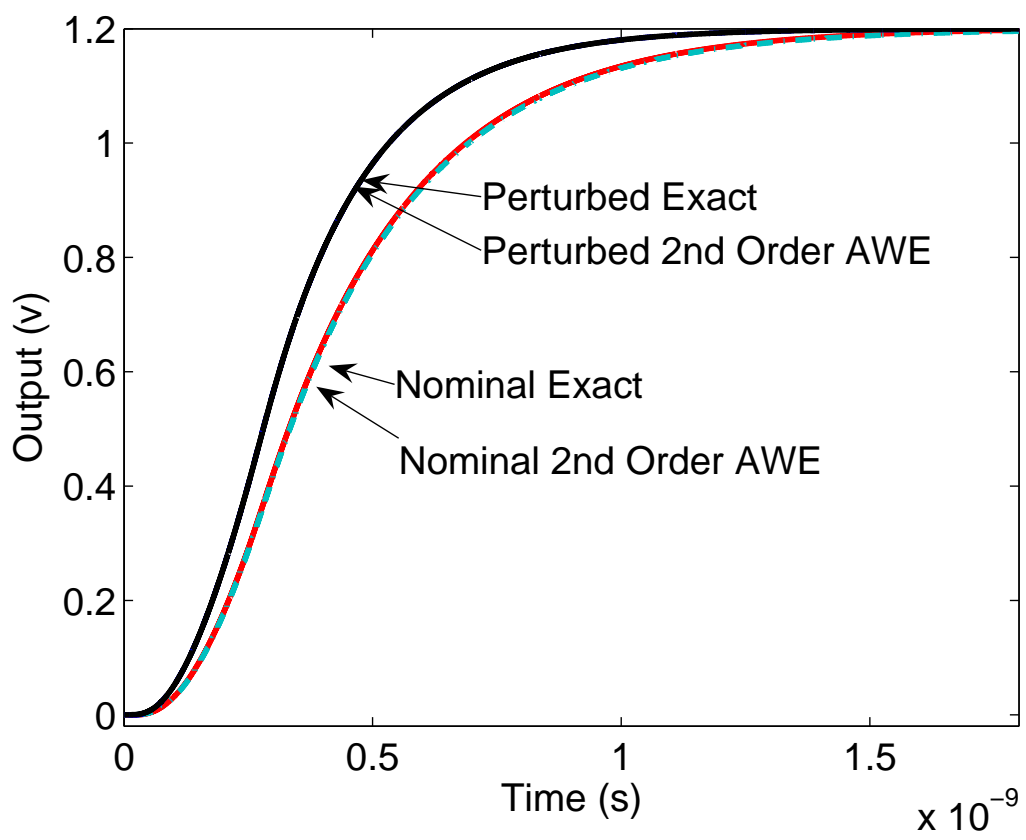
Fig. 6. Nominal and variational analysis for a far-end node.
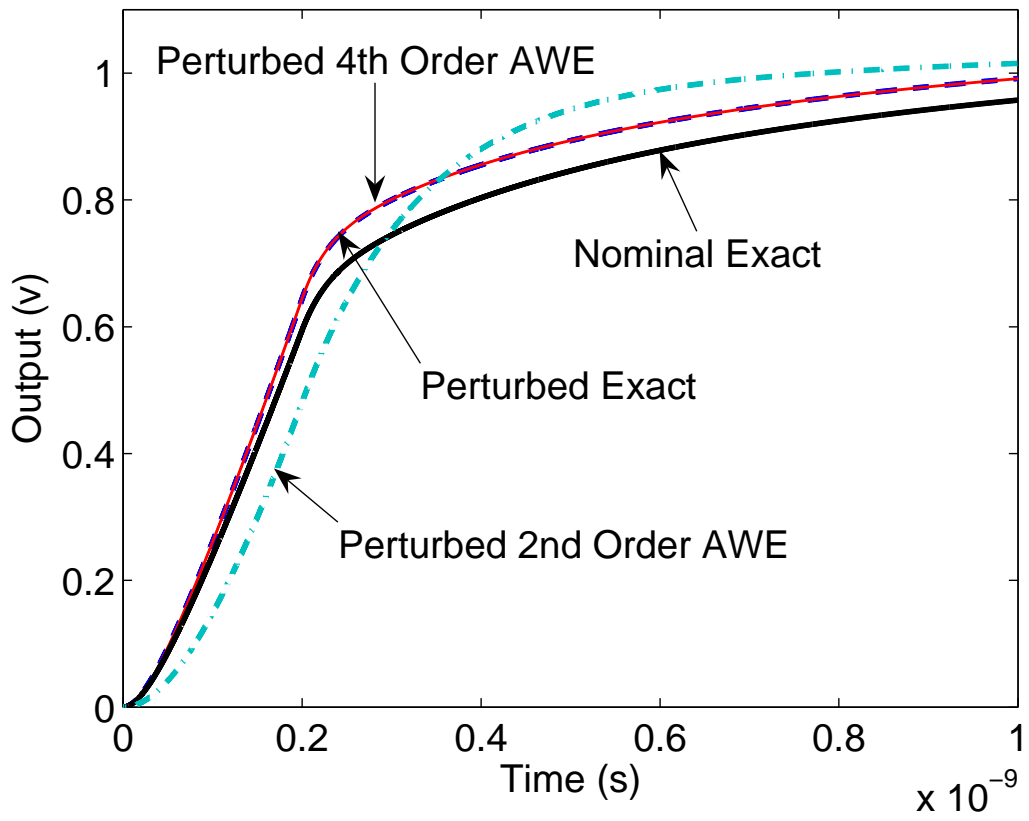
Fig. 7. Nominal and variational analysis for a near-end node.
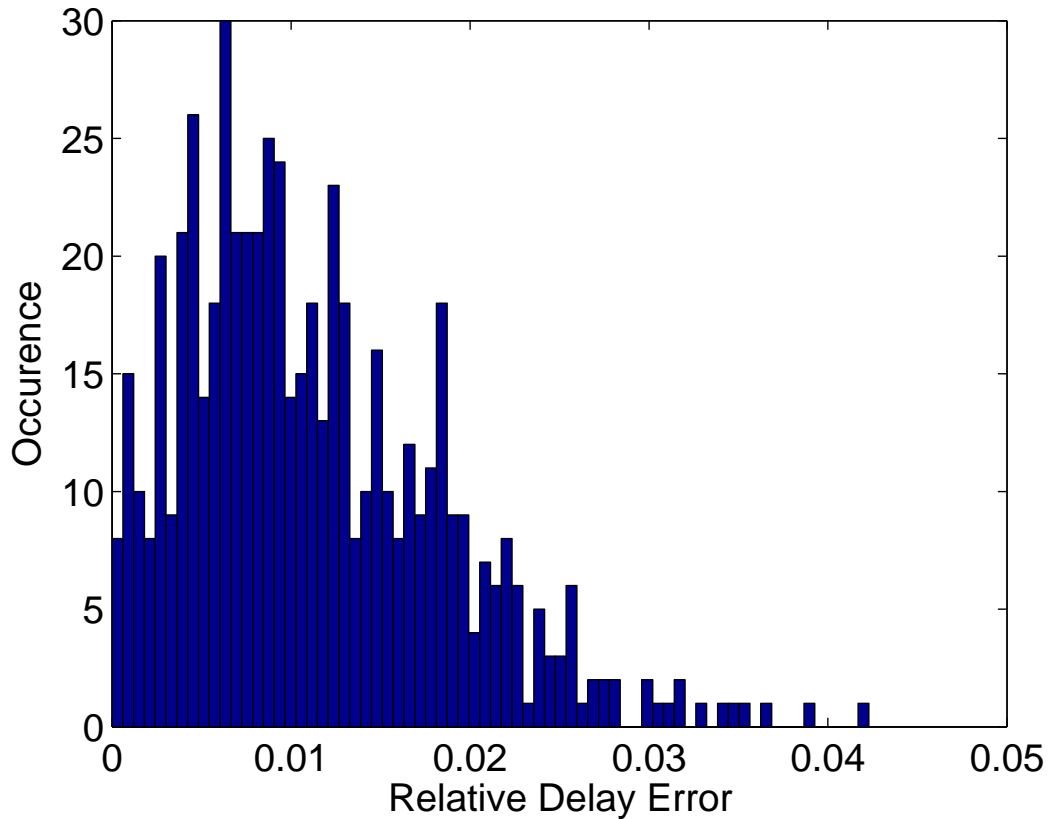
Fig. 8. Relative delay error distribution for a near-end node.

respectively.

Next, we examine the statistical distributions of the interconnect delay and slew in a RC circuit. For this case, 10 independent process parameters are considered and a fixed ramp input with a 50ps slew is applied to each circuit instance. The PDFs of the delay and the slew at one circuit node are examined in Fig. 10 and Fig. 11. As clearly seen from the figure, the PDFs of our variational analysis match very well with those computed by the corresponding 8-th order AWE model for each case.

For more extensive verification of the proposed techniques, we consider a set of RC nets with different sizes ranging from a few ten nodes to a few hundred nodes and several hundred circuit elements, in Table I and Table II. For each circuit, a

Fig. 9. Relative slew error distribution for a near-end node.

Fig. 10. PDF of the interconnect delay.

Fig. 11. PDF of the interconnect slew.

circuit node is arbitrarily chosen as one sink node for comparison. Again, 10 independent process parameters are considered which are perturbed with various degrees to generate 500 samples for each circuit. In Table I, the inp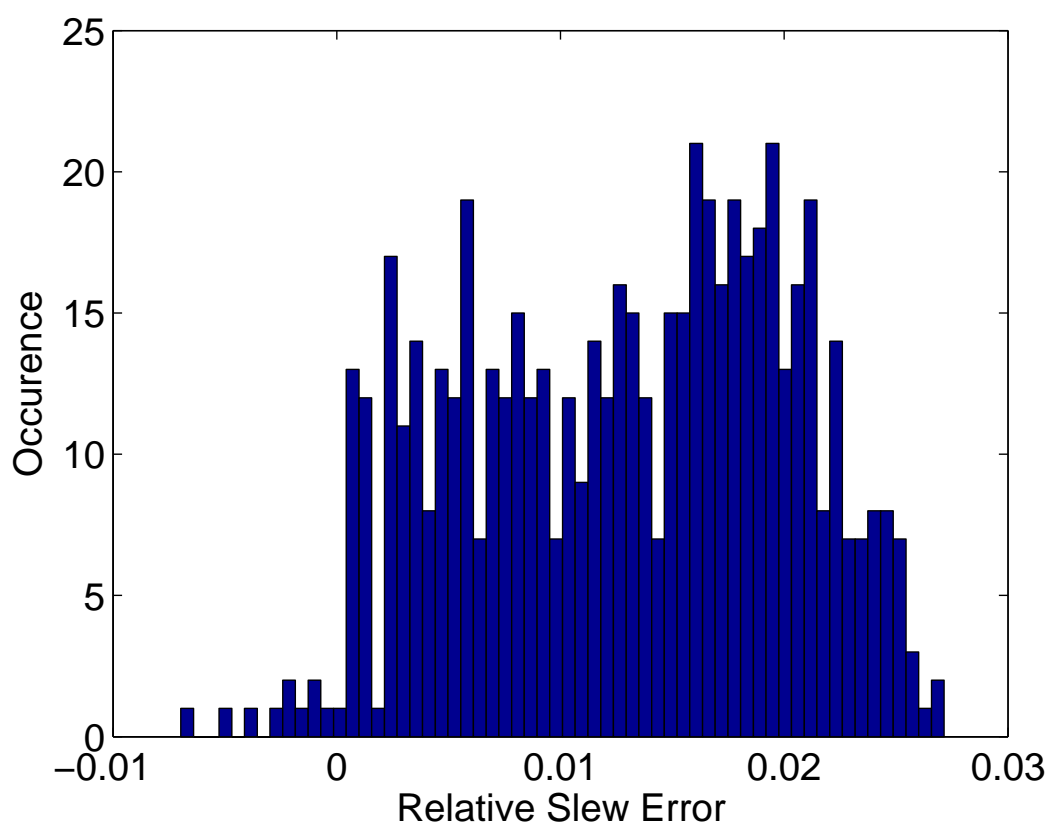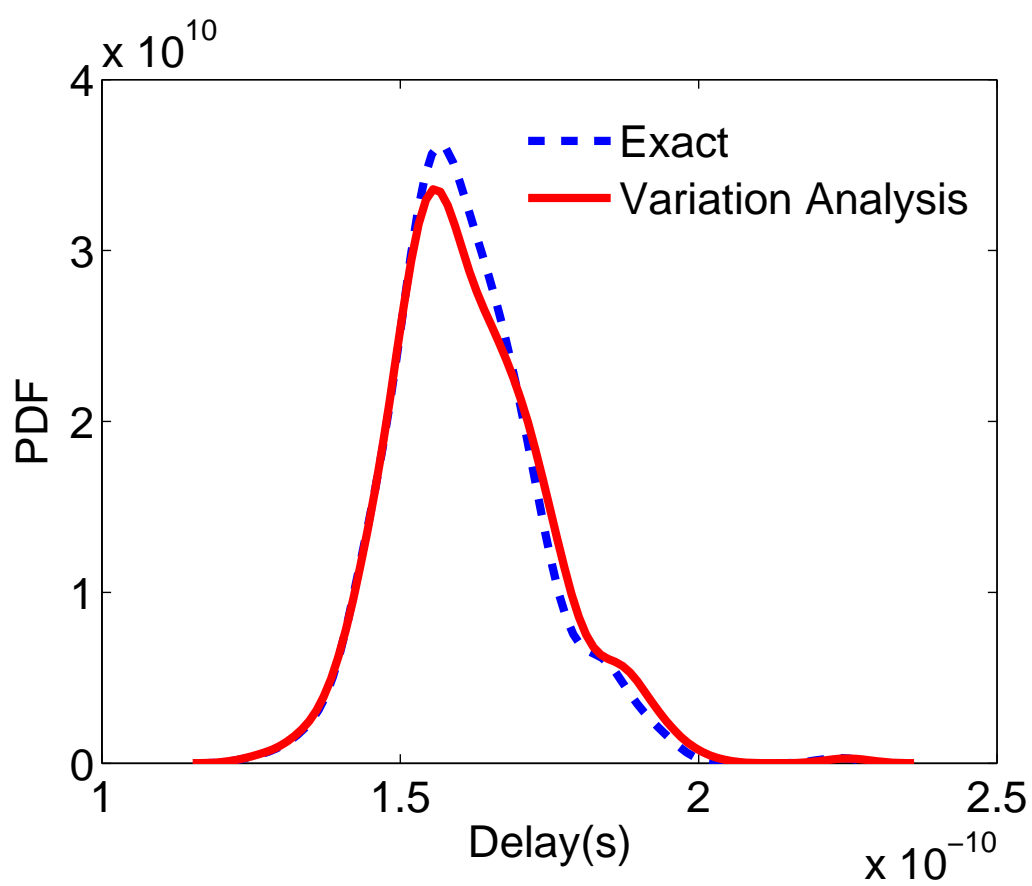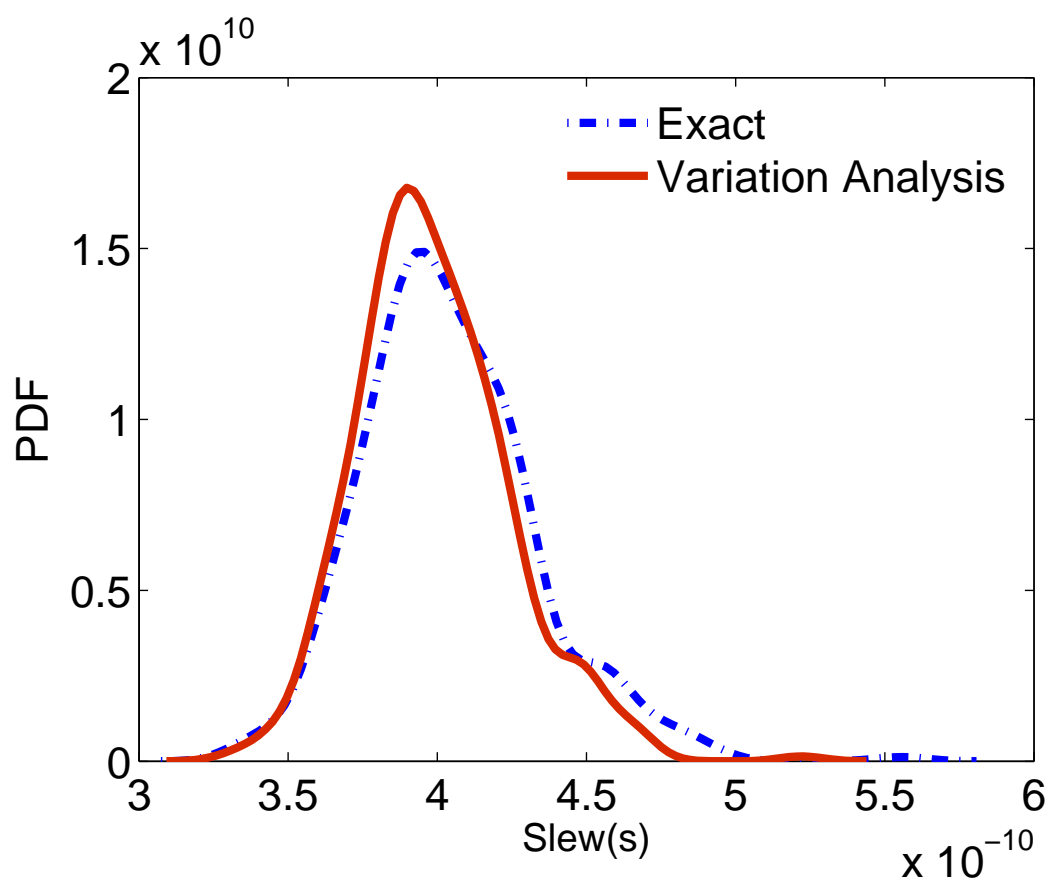ut to all the nets is a fixed ramp input with 50ps slew rate while the input in Table II has a nominal slew of 200ps and varies with the same 10 process parameters. In the second columns of the both tables, the maximum percentages of delay and slew variations (with respect to the nominal values) seen across the 500 samples are listed to indicate the degree of variability. In both tables, we list the maximum and average relative errors for delay and slew for each of these circuits and compare the 2nd-order parametric analysis (5th/6th columns) with the first-order sensitivity analysis (3rd/4th columns). As a reference, a high order AWE model and nonlinear iterations are applied to compute the delay and slew for each sample, which are regarded as the exact solution. In the table, "-" indicates the cases where the corresponding analysis generates a significant error in estimating delay or slew. It can be clearly seen from these tables that for a wide range of delay/slew variations, the presented 2nd-order parametric analysis can maintain very good accuracy. It should be noted that for some cases, the first-order analysis completely fails to capture the large variability.

G. Conclusions

In this chapter, a practical variation-aware methodology is presented to analyze interconnect performance variations. Specific techniques have been developed such that a 2nd-order parametric analysis can be done efficiently for on-chip RC interconnects for a large number of process variations manifesting in terms of RC value perturbations and input slew variations. The proposed variational analysis can accurately capture wide variations of interconnect delay and slew even under the cases where the

simpler first-order sensitivity analysis completely fails. Since the proposed technique produces parametric expressions for delay and slew, it is expected that the technique and its extensions can be incorporated easily into a statistical timing environment as an interconnect delay calculator.

Table I. Variational interconnect analysis results: fixed input slew (50ps)

Net	Max D/S Var.%	1st: Max/Ave%		2nd: Max/Ave%	
		Delay E.	Slew E.	Delay E.	Slew E.
1	34.6/36.8	81.0/7.0	17.1/2.2	2.8/0.9	11.1/1.1
2	59.5/64.7	49.3/8.5	23.5/2.4	2.2/0.7	13.1/1.1
3	31.2/33.8	32.8/6.2	15.4/2.3	5.2/0.9	8.5/0.9
4	45.9/49.7	33.1/8.3	14.5/2.9	3.4/0.9	6.9/1.0
5	61.9/62.1	93.7/16.0	-/-	5.0/1.1	4.2/0.5
6	61.1/62.2	98.6/16.2	-/-	6.3/1.1	4.4/0.5
7	29.6/31.3	37.8/5.5	10.0/1.8	2.7/0.8	3.0/0.7
8	17.6/17.1	32.3/4.2	5.5/1.0	2.5/0.7	2.4/0.6
9	26.7/28.1	9.4/3.1	11.3/13.2	3.4/0.5	4.6/0.8
10	27.9/29.2	11.1/3.4	11.9/3.3	3.2/0.4	3.8/0.7
11	31.7/35.8	19.0/3.9	19.8/3.9	7.1/0.5	9.6/0.9
12	40.6/41.9	16.5/3.9	19.7/3.7	6.3/0.8	10.6/0.9
13	50.9/47.7	20.3/2.9	18.8/2.7	8.0/0.5	8.5/0.6
14	27.3/29.7	17.2/3.5	18.8/3.3	5.7/0.6	7.2/0.8
15	21.7/23.2	13.3/3.6	47.9/3.4	3.0/0.6	5.3/0.9
16	32.9/33.0	14.6/3.6	14.0/3.3	3.9/0.5	4.1/0.7

Table II. Variational interconnect analysis results: w/ input slew variations (nominal slew 200ps)

Net	Max D/S Var.%	1st: Max/Ave%		2nd: Max/Ave%	
		Delay E.	Slew E.	Delay E.	Slew E.
1	30.9/28.5	43.9/5.5	9.9/2.4	3.47/0.5	5.7/1.3
2	46.9/32.1	48.8/6.9	9.2/1.4	3.8/0.4	6.4/1.3
3	21.9/19.2	24.7/4.3	8.7/2.9	2.7/0.8	4.6/1.5
4	12.5/13.5	15.6/4.3	4.8/1.2	2.3/0.7	2.1/0.6
5	76.7/93.6	59.9/10.1	-/-	6.9/1.3	5.0/4.6
6	79.1/13.8	6.9/10.0	-/-	7.4/1.1	7.2/6.0
7	18.9/19.0	28.8/5.3	8.0/2.9	3.1/0.6	4.3/1.5
8	16.3/16.4	25.1/4.0	8.1/2.2	2.3/0.5	3.1/1.3
9	55.9/49.5	18.1/3.4	12.1/2.4	7.8/1.8	6.9/3.1
10	27.4/22.7	9.7/0.8	5.8/1.7	3.6/1.3	5.8/2.8
11	32.6/42.7	14.0/1.7	15.7/2.0	5.9/2.1	11.0/2.1
12	11.6/12.1	4.1/0.6	3.6/0.9	2.6/0.5	2.7/1.2
13	17.3/16.8	5.1/0.7	4.4/0.8	2.5/0.6	3.2/1.3
14	33.0/35.1	9.0/1.2	6.8/1.0	4.4/1.2	3.5/1.5
15	37.9/29.4	9.4/1.4	9.2/1.1	4.9/1.3	4.3/1.4
16	36.4/34.0	8.1/1.1	5.7/1.0	4.2/1.1	2.7/1.3

CHAPTER IV

DRIVING POINT MODEL AND ADJOINT SENSITIVITY ANALYSIS

In the variational interconnect timing analysis flow, the signal delay and slew at sink nodes are analyzed in two steps. In the first step, a reduced-order *driving-point model* of the interconnect network is first constructed (e.g. a three-element π-model). The driving-point model is used with the gate delay model to calculate delay and slew at the driving point of the interconnect. In the second step, the delay and slew at the fan-out nodes are calculated based on their corresponding reduced-order transfer functions. Chapter III is primarily describing the second step. In this chapter, I present techniques to construct the driving point model and compute driving point waveform.

A. Variational interconnect analysis flow

The complete interconnect timing analysis flow is outlined in Fig. 12. The parametric π-model is constructed based on the parametric form of the first three admittance moments. The parametric π-model and the nonlinear gate model can be analyzed using adjoint sensitivity analysis to calculate the 2nd order variational model of delay and slew at the driving point of the interconnect network. After the driving point delay and slew model are calculated, they can be propagated to any sink nodes by using the methodology presented in Chapter III. The efficiency of the proposed analysis methodology is archived via the following steps:

- A reduced-order π-model is used as the driving-point model. Since there are only three parameters in the circuit, the adjoint sensitivity analysis and its second order extension can be carried out quite efficiently.

- For N_ρ process parameters, the first-order parametric dependency of circuit moment vectors are computed directly using sensitivity analysis incorporated in the standard recursive moment computation procedure. However, computing $O(N_\rho^2)$ second-order parametric dependency for each moment vector is rather expensive. To reduce the analysis complexity, an algorithm is developed to only compute the second-order dependency for the moments of the sink nodes where the delay and slew analysis is performed.

- The parametric form of the each output slew is obtained by applying simple and yet accurate slew metric and the computed parametric moments.

- The parametric computation of delay is achieved by constructing a parametric reduced order model for each sink. For "far" end nodes, this is accomplished by using closed-form formulas while for the "near" end nodes, numerically efficient perturbation analysis is applied to produce the parametric reduced model. Then, the reduced model is evaluated using closed-form expressions to obtain the variation of the voltage response of each sink node. Finally, the variation in the voltage response is converted directly to delay variation in the quadratic parametric form, thereby avoiding the application of nonlinear iterations otherwise required in finding a specific delay point.

B. Driving point π-model

A common driving point model is the three-element π-model as shown in Fig. 13, which is widely accepted for its accuracy for RC interconnect structures. The values of the three elements in the model are calculated as follows[30]:
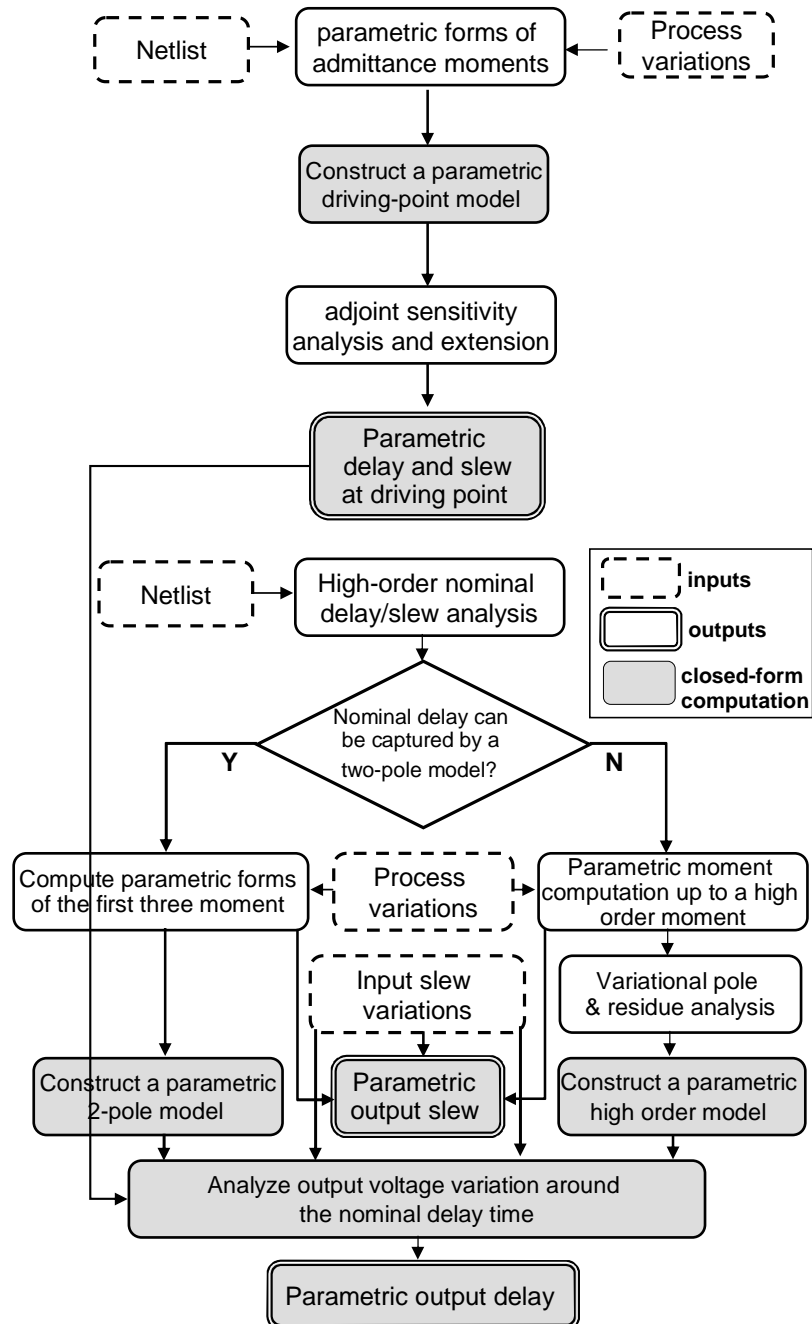
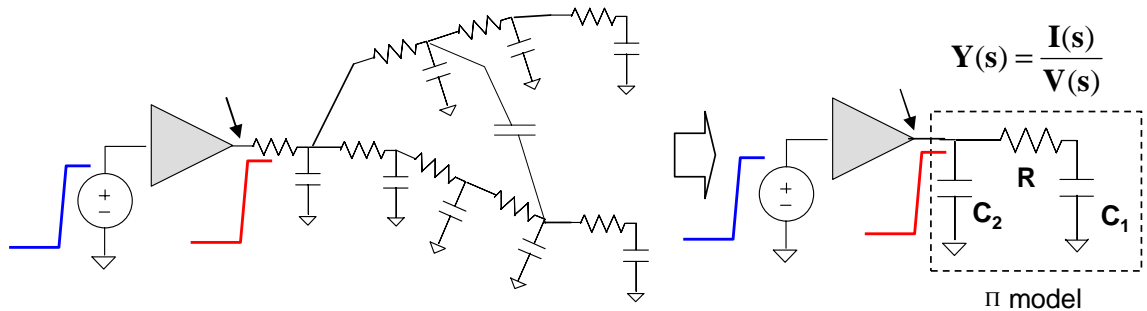Fig. 12. Complete variational interconnect analysis flow.

Fig. 13. Downstream interconnect is modeled as a π model.

$$C_1 = y_2^2/y_3$$
$$C_2 = y_1 - C_1 \qquad (4.1)$$
$$R = -y_3^2/y_2^3$$

where y_1, y_2 and y_3 are the first three moments of the admittance of the interconnect network, seen from the driving point:

$$Y(s) = \frac{I(s)}{V(s)} = y_0 + y_1 s + y_2 s^2 + y_3 s^3 + \cdots \qquad (4.2)$$

From circuit analysis point of view, the admittance is the current drawn from the driving point when unit driving point voltage is applied. Thus it is readily available after the circuit analysis described in the previous section is performed. The parametric form of the driving point model is calculated by applying parametric admittance moments in Eqn. (4.2).

In order to calculate the delay and slew at the driving point, the parametric driving point model needs to be analyzed with the gate delay model. Following previous discussion, we use a quadratic equation as the parametric delay model, as shown in Eqn. (3.1). In the context of 50% delay point, the first term in the equation

can be expressed as:

$$\alpha_d = (\frac{\partial T_d}{\partial p_1}, \frac{\partial T_d}{\partial p_2}, \cdots, \frac{\partial T_d}{\partial p_n}) \tag{4.3}$$

while the second order effects can be captured by:

$$\Gamma_d = \begin{bmatrix} \frac{\partial^2 T_d}{\partial p_1^2} & \cdots & \frac{\partial^2 T_d}{\partial p_1 p_n} \\ \frac{\partial^2 T_d}{\partial p_2 p_1} & \cdots & \frac{\partial^2 T_d}{\partial p_2 p_n} \\ \vdots & & \vdots \\ \frac{\partial^2 T_d}{\partial p_n p_1} & \cdots & \frac{\partial^2 T_d}{\partial p_n^2} \end{bmatrix} \tag{4.4}$$

Without loss of generality, we only consider 50% delay point. To calculate the 1st order sensitivities in Eqn. (4.3), we have:

$$V(T_d, \rho) = Vdd/2 \tag{4.5}$$

If we take partial derivatives with respect to the variations ρ, we have:

$$\frac{\partial V}{\partial T_d} \frac{\partial T_d}{\partial \rho} + \frac{\partial V}{\partial \rho} = 0 \tag{4.6}$$

which leads to

$$\frac{\partial T_d}{\partial \rho} = -\frac{\partial V/\partial \rho}{\partial V/\partial T_d} \tag{4.7}$$

In the above equation, the denominator is the slope of the waveform at the crossing point T_d and is available after a nominal timing analysis. The numerator is the sensitivity of the waveform with respect to the variations. In a timing analysis flow, the driving point π-model is analyzed with nonlinear delay model at gate level or transistor level. Therefore the parameters of both linear π-model and the gate model will affect the waveform. However, in the experimental result section, we will only demonstrate our variational interconnect delay analysis techniques by computing de-

lay/slew dependencies on the circuit element variations in the interconnect networks. To ensure the generality of our method, we use adjoint sensitivity analysis to calculate the first and second order parameters.

C.   Adjoint sensitivity analysis for driving point π-model

The classical adjoint sensitivity analysis was originally derived from Tellegen's theorem [31]. The sensitivity of the circuit performance (delay, slew and noise, etc) with respect to every circuit element can be computed efficiently by just running two transient analyses. The basic flow is as follows: suppose we want to compute the sensitivity of the delay at a sink node A with respect to every circuit element. First, we need to do a standard transient analysis for the original circuit, and save the branch voltage for every capacitor and branch current for every resistor in a certain duration of time. Second, an adjoint circuit is constructed based on the topology of the original circuit, and an input impulse excitation for the adjoint circuit is set at node A, all the other excitations in the original circuit are set to be zero. We perform another transient analysis on the adjoint circuit, save the branch voltage for every capacitor and branch current for every resistor in the same duration of time. Third, for each capacitor, we do a convolution between the derivative of branch voltage of the original circuit and the branch voltage of the adjoint circuit, the number we get will be the sensitivity of the original voltage response at node A with respect to the value of that capacitor, the sensitivity with respect to parameters can be computed easily by using the chain rule. For each resistor, the convolution is between the branch current in the original circuit and the branch current in the adjoint circuit, and the result of the convolution is the sensitivity of the original voltage response at node A with respect to the value of that resistor.

To derive the equations for first order adjoint sensitivity computation, we begin with the very basic circuit equations. Given two topologically identical circuits, their topological constraints are the same, so their KCL and KVL equations can be written in terms of the same reduced incidence matrix A:

$$KCL: Ai_b = 0 \quad and \quad A\phi_b = 0 \tag{4.8}$$

$$KVL: v_b = A^T v_n \quad and \quad \psi_b = A^T \psi_n \tag{4.9}$$

The meaning of the above notations are: v_b and i_b are branch voltages and branch currents of the original circuit, ψ_b and ϕ_b are branch voltages and branch currents of the adjoint circuit. Then the general form of Tellegen's theorem can be written as follows:

$$\sum_b v_b \phi_b \equiv 0 \tag{4.10}$$

$$\sum_b i_b \psi_b \equiv 0 \tag{4.11}$$

Equation 4.10 and 4.11 can be derived from the topological constraints.

$$v_b^T \phi_b = (A^T v_n)^T \phi_b = v_n^T A \phi_b = 0 \tag{4.12}$$

$$\psi_b^T i_b = (A^T \psi_n)^T i_b = \psi_n^T A i_b = 0 \tag{4.13}$$

When there are variations in the original circuit, both branch currents and voltages in the original circuit are subject to changes: $v_B(t) + \delta v_B(t)$ and $i_B(t) + \delta i_B(t)$. It can be shown that the following relationship holds:

$$\sum_B [\delta v_B(t)\phi_B(\tau) - \delta i_B(t)\psi_B(\tau)] = 0 \tag{4.14}$$

Besides the nominal transient simulation on the original circuit, another transient simulation is required on the adjoint circuit with zero initial conditions. Note that

the adjoint transient simulation is done backward in time. And the results of adjoint transient and nominal transient has to be convoluted to compute the sensitivities. Note although the sensitivity analysis can also capture the sensitivity to the input signal changes, in our approach, we can null them out since we are not interested in those changes. We provide more details on the formulation of resistors, capacitors and nonlinear devices in the adjoint circuit the remaining part of this section:

1.   Resistors in the adjoint circuit

Consider the following resistive branch in the original circuit:

$$V_R(t) = R \cdot i_R(t) \tag{4.15}$$

If we introduce a variation on the resistance, we have:

$$V_R(t) + \delta V_R(t) = (R + \delta R) \cdot (i_R(t) + \delta i_R(t)) \tag{4.16}$$

It is obvious that the variation of the branch voltage can be expressed as:

$$\delta V_R(t) = R \cdot \delta i_R(t) + \delta R \cdot i_R(t) + \delta R \cdot \delta i_R(t) \tag{4.17}$$

The contributions of all resistive branches in the adjoint sensitivity equation Eqn. (4.14) is:

$$\sum_R [\phi_R(R\delta i_R + i_R\delta R) - \psi_R \delta i_R] = 0 \tag{4.18}$$

since we choose the same resistance for the same resistive branch in the original and adjoint circuit, it is obvious that $\phi_R R = \psi_R$ in the adjoint circuit. Thus the first and last terms in Eqn. (4.18) cancel each other. The contributions of all resistive branches in the adjoint sensitivity is:

$$\sum_R \phi_R i_R \delta R = 0 \tag{4.19}$$

2. Capacitors in the adjoint circuit

The relationship between branch current and branch voltage in the original circuit can be expressed as follows:

$$i_C(t) = C \cdot \dot{v}_C(t) \tag{4.20}$$

the variation of the branch current can then be expressed as:

$$\delta i_C(t) = C \cdot \delta \dot{v}_C(t) + \dot{v}_C(t) \cdot \delta C \tag{4.21}$$

the contributions of capacitive branches in the adjoint circuit can be shown as:

$$\int_{t_0}^{t_f} [\phi_C(\tau)\delta v_C(t) - \psi_C(\tau)(C\delta \dot{v}_C(t) + \dot{v}_C(t)\delta C)]\, dt \tag{4.22}$$

we can integrate the above equation by part and only keep the first order terms. By taking into consideration that the capacitance stays the same in the adjoint circuit, e.g., $\phi_C(\tau) = C\psi_C(\tau)$, the above expression can be simplified as:

$$-C\psi_C(t)\delta v_C(t)|_{t_0}^{t_f} + \int_{t_0}^{t_f} [-\psi_C \tau)(C\delta \dot{v}_C(t)]\, dt \tag{4.23}$$

The simplification can be achieved by assuming that $\phi_C(\tau) = -C\dot{\psi}_\tau$. In order to avoid negative energy storage device in the adjoint circuit, we need to choose τ such that $\tau = t_0 + t_f - t$. To further simplify the expression in Eqn. (4.23), we choose initial conditions to be zero:

$$\delta v_C(t_0) = 0 \tag{4.24}$$

$$\psi_C(t_0) = 0 \tag{4.25}$$

then the contributions of the capacitance in the adjoint sensitivity is:

$$-\int_{t_0}^{t_f} \psi_C(\tau)\dot{v}_C(t)\, dt \tag{4.26}$$

3.   MOSFET devices in the adjoint analysis

In sensitivity analysis, the sensitivity with respect to nonlinear devices are handled via the linearizion. In a timing analysis flow, it may be possible to use compact nonlinear driver models to speed up the analysis and impose sensitivity analysis on the driver models. However, due to the scope of this interconnect analysis work, we assume that transistor-level description is used for each nonlinear driver. After the convergence of nonlinear iteration at each time point for the complete nonlinear circuit, the linearized self conductances (e.g., G_{ds}) will remain the same in the adjoint circuit. The controlling conductance (e.g., G_m) will also remain the same in the adjoint circuit, although the controlling branches and controlled branches are swapped, to reflect the fact that that MNA matrices of the original and adjoint circuit are transposed. Fig. 14 shows the schematic of a simple inverter driving a π-model. It also shows the linearized circuit as well as adjoint circuit for sensitivity analysis. Note that in order to introduce voltage branches in the original and adjoint circuit, we need to add several zero valued current sources in the original circuit.

As can be seen in Fig. 14, it turns out that to compute the sensitivities for the voltage response of a particular point of time, say T_d, an impulse current source needs to be applied at the driving point in the adjoint circuit, but at time $T - T_d$ along the axis of τ, as illustrated in the figure.

4.   Second order sensitivity

In order to calculate the 2nd order sensitivity of the driving point waveform, we apply finite-difference method. Each of the three element values of the π-model is perturbed by a small amount and the adjoint sensitivity analysis is performed. By doing so, we can calculate one column (or row) in Eqn. (4.4) with each additional adjoint
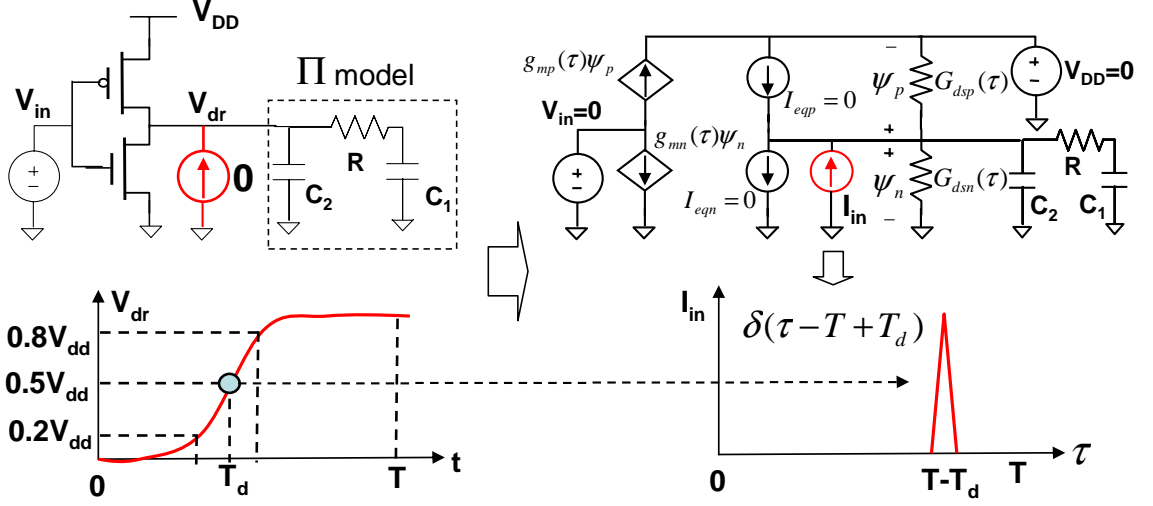
Fig. 14. An inverter drives a π-model. The linear time-varying adjoint circuit used to compute the sensitivities of the 50% delay w.r.t π-model elements is shown. For illustration, device capacitive parasitics are not included.

sensitivity analysis. Since we are only interested in the second order sensitivities of the three elements in the driving point π-model, the cost of the operation is quite manageable. More specifically, assume the adjoint sensitivity analysis of the original circuit yields sensitivity as follows:

$$\alpha_d = \left(\frac{\partial T_d}{\partial p_1}, \frac{\partial T_d}{\partial p_2}, \frac{\partial T_d}{\partial p_3} \right) \tag{4.27}$$

We then introduce a small amount of variation into p_1 as $p_1 + \delta p_1$. After another adjoint sensitivity analysis, we obtain the updated sensitivities:

$$\alpha_d = \left(\frac{\partial \tilde{T}_d}{\partial p_1}, \frac{\partial \tilde{T}_d}{\partial p_2}, \frac{\partial \tilde{T}_d}{\partial p_3} \right) \tag{4.28}$$

then we can calculate the second order sensitivities as:

$$\frac{\partial^2 T_d}{\partial p_1^2} \approx \frac{\frac{\partial \tilde{T}_d}{\partial p_1} - \frac{\partial T_d}{\partial p_1}}{\delta p_1}$$

$$\frac{\partial^2 T_d}{\partial p_1 \partial p_2} \approx \frac{\frac{\partial \tilde{T}_d}{\partial p_2} - \frac{\partial T_d}{\partial p_2}}{\delta p_1} \tag{4.29}$$

$$\frac{\partial^2 T_d}{\partial p_1 \partial p_3} \approx \frac{\frac{\partial \tilde{T}_d}{\partial p_3} - \frac{\partial T_d}{\partial p_3}}{\delta p_1}$$

This operation is quite efficient because one additional adjoint sensitivity analysis generates one row in the second order sensitivity matrix Eqn. (4.4). In our driving point model, only three additional adjoint sensitivity analyses are required.

It should be noted that from a theoretical point of view, the 2nd order sensitivities can be computed without applying finite difference approximation. Due to the scope limitation of this work, we will not discuss such a possibility in the present paper. Furthermore, the above sensitivity-based analysis has been described under the context of a particular delay point, say $50\% V_{dd}$ crossing point. The same procedure can be applied to the 20% and $80\% V_{dd}$ crossings such that a quadratic parameter forms can be computed for the driving point slew. Finally, utilizing the sensitivities computed above and applying chain rule, quadratic parametric models in terms of process parameters can be computed for the driving point delay and slew.

D.   Experimental results

To demonstrate the variational analysis of interconnects while including nonlinear drivers, we first consider the case where an inverter is driving a RC network. The inverter is designed using a $0.13um$ CMOS technology, and a fixed ramp input with $30ps$ slew (20% to $80\% V_{dd}$) is applied to the input of the inverter. A sink node is selected and the delay and slew at the node are examined. Fig. 15 and 16 show the relative error distributions for the delay based on 500 circuit samples. The results of both the 1st and 2nd order analyses are shown. The reference delay values are obtained by analyzing the each circuit sample using nonlinear transient analysis,
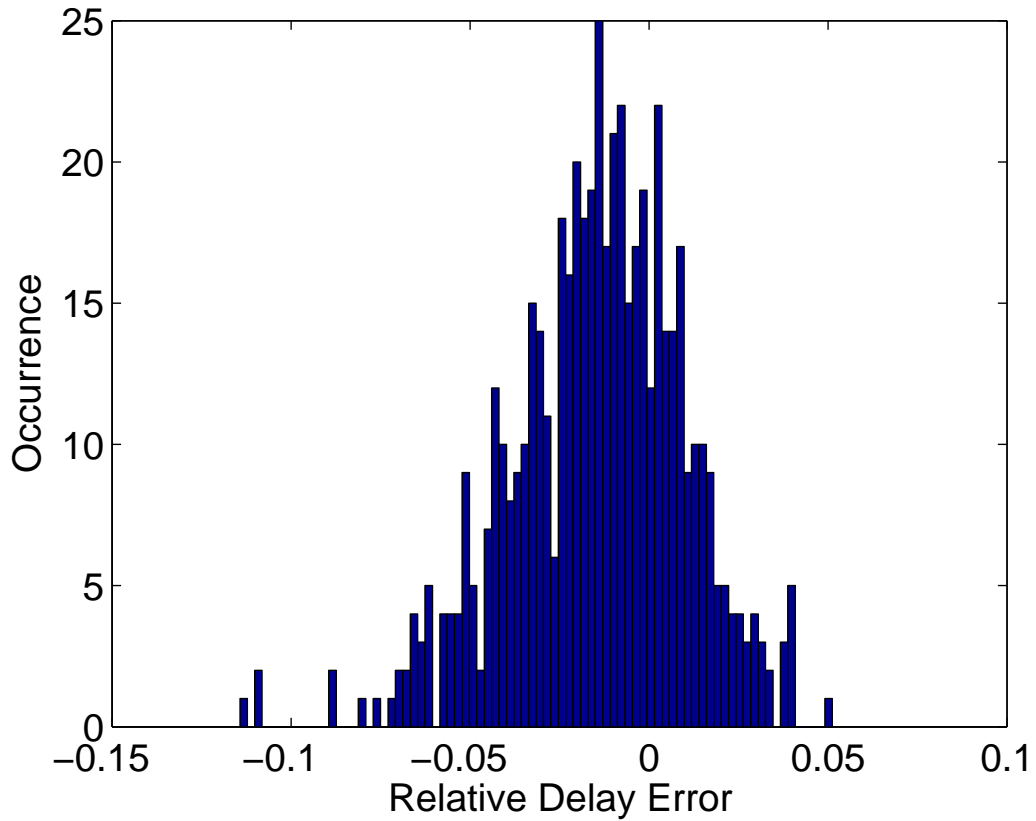
Fig. 15. Relative delay error of the 1st order analysis.

where a high-order reduced interconnect model is used to speedup the analysis. Our parametric analysis results are based on computing the parametric delay expressions first and then sampling directly these parametric forms. As can be seen in Fig. 15 and 16, both analyses are reasonably accurate with the 2nd order analysis providing more favorable results by reducing the maximum error of the 1st order analysis from 11% to 6%.

The same comparison is made for slew and the results are shown in Fig. 17 and 18. A similar conclusion can be drawn here.

For a more complete comparison, in Table III, a set of ten RC circuits driven by the inverter are considered. The nature of these ten RC circuits are similar to
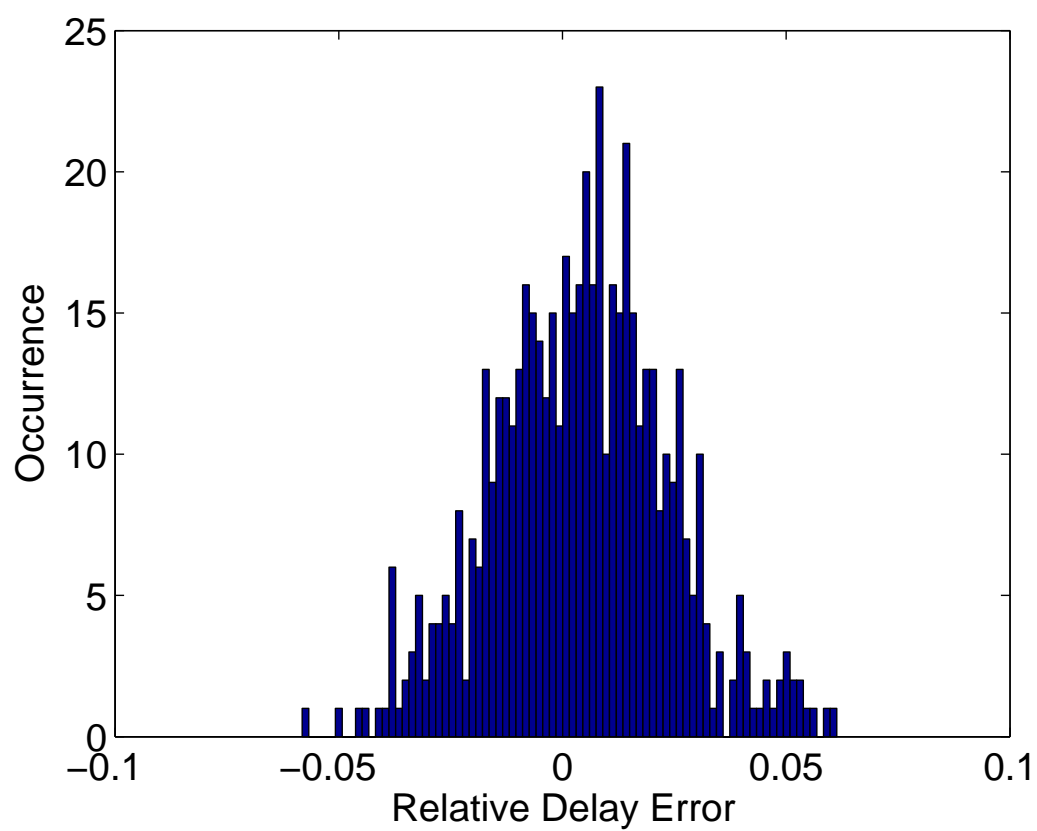
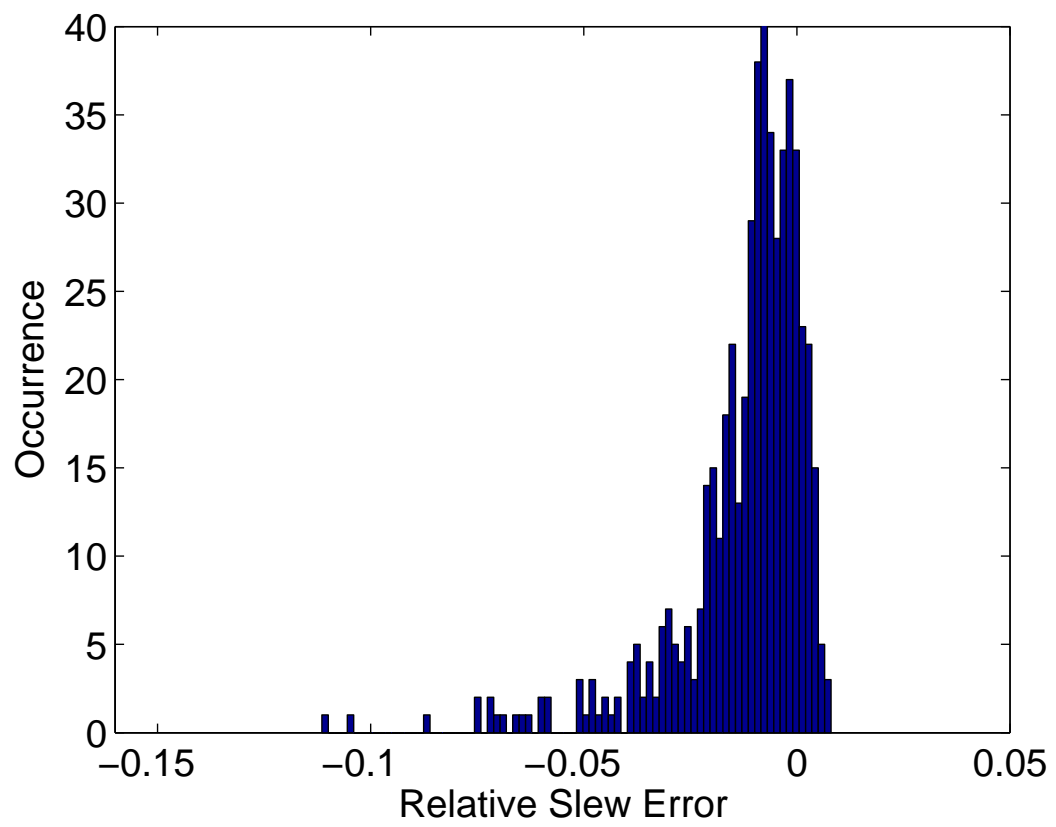Fig. 16. Relative delay error of the 2nd order analysis.

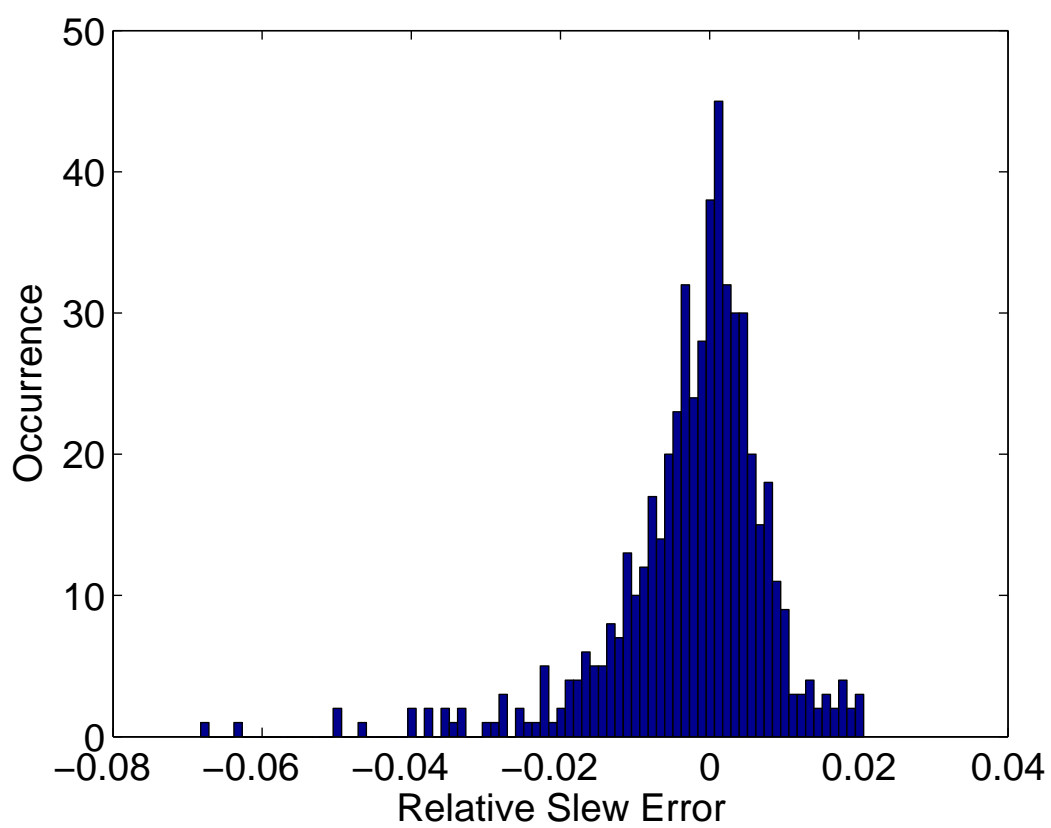Fig. 17. Relative slew error of the 1st order analysis.

Fig. 18. Relative slew error of the 2nd order analysis.

what we use for the interconnect analysis in Chapter III. The input slew is again set to be 30*ps*. In Table IV, three RC circuits driven by an two-input NAND gate are analyzed. Here, data are organized in the same way as in Table I. As can be seen from these tables, the average errors of both analyses are quite small. Furthermore, the 2nd order analysis brings notable improvement over the 1st order analysis, especially in terms of the maximum error.

Table III. Variational interconnect delays/slews of RC circuits driven by an inverter: inverter input slew (30ps)

Design	Max D/S Var.%	1st order: Max/Ave%		2nd order: Max/Ave%	
		Delay E.	Slew E.	Delay E.	Slew E.
1	22.9/18.9	7.8/1.6	6.2/2.0	5.4/1.3	3.9/1.1
2	33.3/23.9	11.4/2.2	11.2/1.3	6.1/1.6	6.8/0.7
3	14.1/10.7	3.3/0.8	4.5/2.3	3.7/0.7	3.3/1.9
4	22.9/21.7	8.8/1.4	9.0/3.2	4.2/0.8	4.4/2.2
5	27.4/29.5	9.8/1.8	7.5/2.3	6.0/1.4	2.9/1.2
6	16.5/16.1	6.5/1.2	9.2/2.2	3.5/0.8	5.7/1.4
7	28.5/26.6	9.3/2.3	8.2/2.2	8.1/1.9	3.5/1.1
8	22.4/21.2	9.3/1.7	7.2/2.1	5.1/1.3	3.8/1.0
9	21.4/21.0	8.2/1.9	8.2/2.5	5.8/1.4	4.1/1.4
10	15.3/11.6	8.2/1.3	5.1/2.0	3.5/0.8	2.6/1.2

In Fig. 19 and 20, the normalized runtimes (w.r.t the nominal case) of the 2nd order analysis are shown. In Fig. 19, three interconnects are considered and it can be seen that the runtime shows the expected quadratic dependency on the number of parameters. In Fig. 20, the same three interconnects are driven by an inverter and the adjoint sensitivity approach is applied. The interconnects in the first two circuits

Table IV. Variational interconnect delays/slews of RC circuits driven by a two-input NAND: NAND gate input slew (30ps)

Design	Max D/S Var.%	1st order: Max/Ave%		2nd order: Max/Ave%	
		Delay E.	Slew E.	Delay E.	Slew E.
1	22.5/22.8	6.8/1.5	9.1/1.9	4.4/0.8	4.1/0.9
2	33.4/30.7	13.8/3.0	11.6/2.7	8.5/2.3	5.8/1.1
3	30.3/24.9	12.8/2.4	8.8/1.7	7.3/1.8	4.9/0.8

are relatively small, therefore the runtime is dominated by the transient analyses in the adjoint sensitivity analysis. The runtime of the last circuit exhibits the same quadratic dependency because the circuits is dominated by the interconnect.

E. Conclusion

In this chapter, the complete variational interconnect timing analysis flow is presented. The variational driving point waveform including first and second sensitivities with respect to process variations are computed by combining the driving point π-model and adjoint sensitivity analysis method. Then the variational driving point waveform is propagated through the interconnect nets by using the methodology introduced in Chapter III to get the second order parametric expressions of delay and slew at any sink nodes. Experimental results show that second order variational analysis can achieve much better accuracy compared with first order analysis, while the runtime of our analysis is still under control.
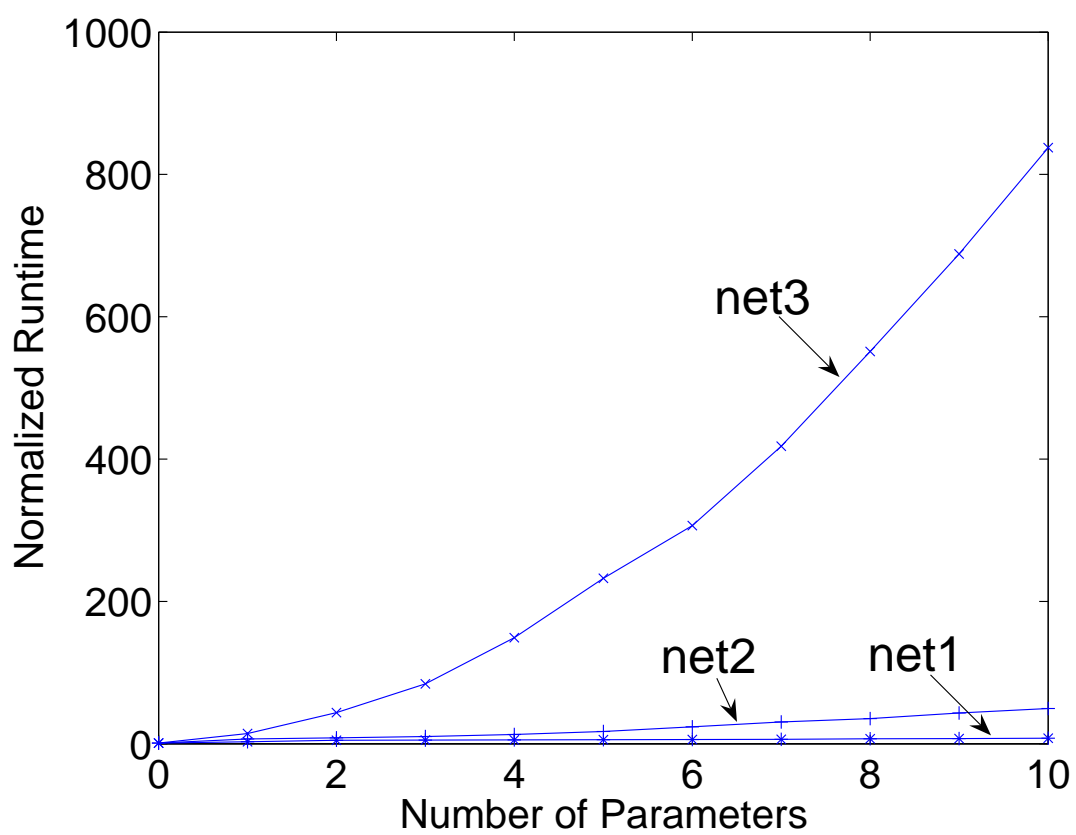
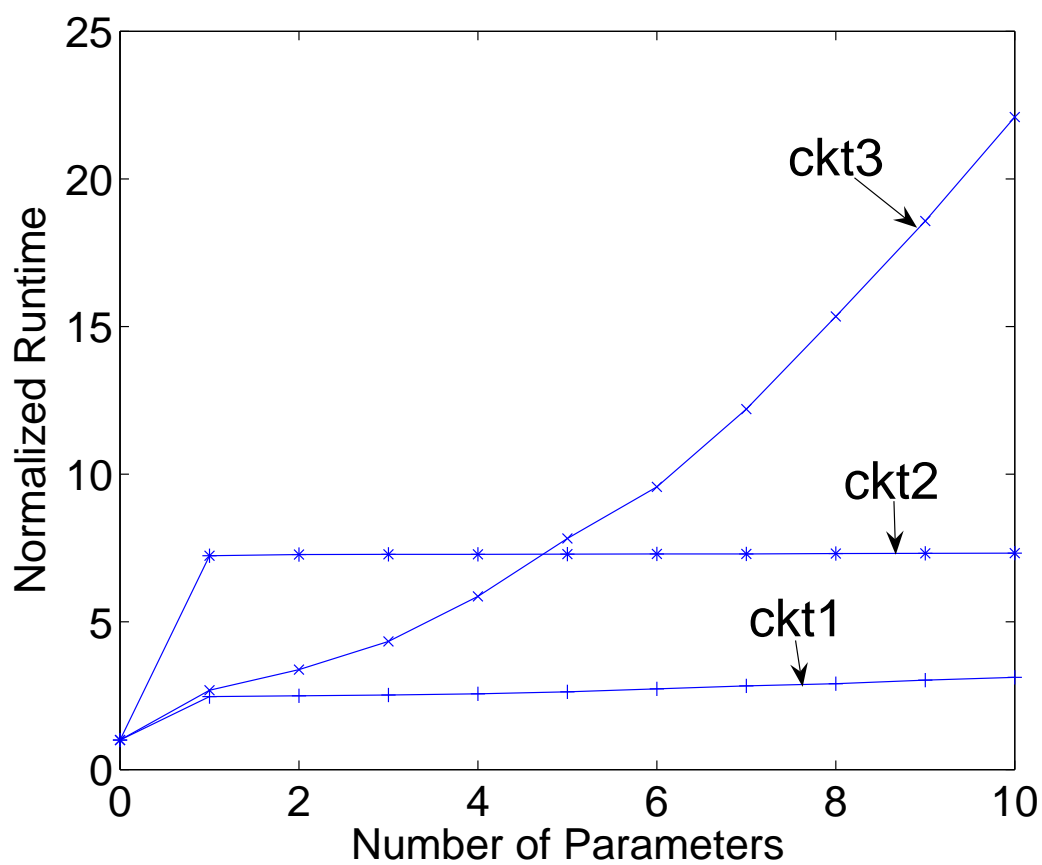Fig. 19. Runtime vs number of parameters plot for 2nd order analysis of three inter-connect nets.

Fig. 20. Runtime vs number of parameters plot for 2nd order analysis of three nets driven by an inverter .

CHAPTER V

CONCLUSION AND FUTURE WORK

A. Conclusion

In this thesis, the complete variational interconnect timing analysis flow is presented. A set of practical circuit analysis and simulation techniques are included in this flow. Our variational interconnect analysis method can translate the interconnect and input signal variations into the output delay and slew variations efficiently and accurately. And we also propose to use adjoint sensitivity analysis method to construct the driving point waveform model. In the step of computing the driving point waveform, we combine the driving point π-model and the extension of adjoint sensitivity analysis method in order to handle second order dependency of the driving point waveform with respect to process variations. Since this proposed analysis flow produces parametric expressions for delay and slew of any sink nodes in a typical circuit which contains a interconnect net driven by a nonlinear gate, it is expected that this flow can be incorporated easily into a statistical timing environment as an interconnect delay calculator.

B. Future work

In the variational timing analysis flow, the variations of nonlinear parts of the circuit are not considered, a natural extension of this flow is to include the variations from the nonlinear parts of the circuit. Then this flow can be extended as a general circuit simulator which can do variational/sensitivity analysis for both linear and nonlinear circuits. It can provide another powerful tool for the statistical timing analysis/optimization purpose.

In this thesis, second order adjoint analysis method is utilized only for the driving point π-model, so another possible research direction is to extend the second order adjoint analysis method to the entire circuit. Since adjoint sensitivity analysis is a general analysis/simulation method, it can be used in many other applications other than variational circuit analysis such as: noise/signal integrity analysis, circuit optimization etc.

REFERENCES

[1] L. Pillage and R. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 352–366, April 1990.

[2] P. Feldmann and R. Freund. "Efficient linear circuit analysis by padé approximation via the lanczos process." *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 639–649, May 1995.

[3] A. Odabasioglu, M. Celik, and L. Pileggi. "Prima: passive reduced-order interconnect macromodeling algorithm." *IEEE Trans. Computer-Aided Design*, vol. 17(8), pp. 645–654, August 1998.

[4] J. Phillips, L. Daniel, and L. Silveira. "Guaranteed passive balancing transforms for model order reduction." *IEEE Trans. Computer-Aided Design*, vol. 22(8), pp. 1027–1041, August 2003.

[5] S. Nassif, "Modeling and analysis of manufacturing variations," in *IEEE Custom Integrated Circuits Conf.*, 2001.

[6] X. Ye, P. Li, F. Liu. "Practical variation-aware interconnect delay and slew analysis for statistical timing verification." in *Proc. IEEE/ACM ICCAD*, 2006.

[7] X. Ye, F. Liu, P. Li, . "Fast variational interconnect delay and slew computation using quadratic models." *IEEE Trans. on VLSI*, to appear.

[8] C. Kashyap, C. Alpert, F. Liu, and A. Devgan. "Closed-form expressions for extending step delay and slew metrics to ramp inputs for rc trees." *IEEE Trans. Computer-Aided Design*, vol. 23(12), pp. 1661–1669, April 2004.

[9] R. Shiveley. "Dual-Core Intel Itanium 2 Processors Deliver Unbeatable Flexibility and Performance to the Enterprise." *Technology@Intel Magazine*, www.intel.com/technology/magazine/, August 2006.

[10] C. Visweswariah, K. Ravindran, K. Kalafala, S. Walker, and S. Narayan. "First-order incremental block-based statistical timing analysis." in *Proc. IEEE/ACM DAC*, 2004.

[11] H. Chang, S. Sapatnekar. "Statistical timing analysis considering spatial correlations using a single pert-like traversal." in *Proc. IEEE/ACM ICCAD*, 2003.

[12] Y. Zhan, A. Strojwas, X. Li, L. Pileggi, D. Newmark, M. Sharma. "Correlation-aware statistical timing analysis using non-gaussian delay distributions ." in *Proc. IEEE/ACM DAC*, 2005.

[13] L. Zheng, W. Chen, Y. Hu, J. Gubner, C. Chen. "Correlation-preserved non-gaussian statistical timing analysis with quadratic timing model." in *Proc. IEEE/ACM DAC*, 2005.

[14] C. Clark. "The greatest of a finite set of random variables." *Operations Research*, pp. 145–162, March-April 1961.

[15] Y. Liu, L. Pileggi, and A. Strojwas, "Model order-reduction of rc(l) interconnect including variational analysis," in *Proc. IEEE/ACM Design Automation Conf.*, 1999.

[16] P. Heydari and M. Pedram, "Model reduction of variable-geometry interconnects using variational spectrally-weighted balanced truncation," in *Proc. IEEE/ACM ICCAD.*, 2001.

[17] R. Phillips, "Variational interconnect analysis via pmtbr." in *Proc. IEEE/ACM ICCAD.*, 2004.

[18] L. Daniel, O. Siong, L. Chay, K. Lee, and J. White, "A multi-parameter moment-matching model-reduction approach for generating geometrically parameterized interconnect performance models." *IEEE Trans. Computer-Aided Design*, vol. 23(5), pp. 678–693, May 2004.

[19] J. Ma and R. Rutenbar. "Interval-valued reduced order statistical interconnect modeling." in *Proc. IEEE/ACM ICCAD*, 2004.

[20] P. Li, Y. Liu, X. Li, L. Pileggi, and S. Nassif. "Modeling interconnect variability using efficient parametric model order reduction." in *Proc. IEEE/ACM DATE*, 2005.

[21] X. Li, P. Li, and L. Pileggi. "Parameterized interconnect order reduction with explicit-and-implicit multi-parameter moment matching for inter/intra-die variations." in *Proc. IEEE/ACM ICCAD*, 2005.

[22] K. Agarwal, D. Sylvester, D. Blaauw, F. Liu, S. Nassif, and S. Vrudhula. "Variational delay metrics for interconnect timing analysis." in *Proc. IEEE/ACM DAC*, 2004.

[23] J. Wang, P. Ghanta, and S. Vrudhula. "Stochastic analysis of interconnect performance in the presence of process variations." in *Proc. IEEE/ACM ICCAD*, 2004.

[24] K. Kerns and A. Yang, "Stable and efficient reduction of large, multiport RC networks by pole analysis via congruence transforms." *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 734–744, July 1997.

[25] G. W. Stewart, J. G. Sun. "Matrix perturbation theory." San Diego, CA: Academic Press, Inc., 1990.

[26] C. Ratzlaff and L. Pillage. "Rice: rapid interconnect circuit evaluation using awe." *IEEE Trans. Computer-Aided Design*, vol. 13(6), pp. 763–776, June 1994.

[27] C .Alpert, A. Devgan, and C. Kashyap. "Rc delay metrics for performance optimization." *IEEE Trans. Computer-Aided Design*, vol. 20, pp. 571–582, May 2001.

[28] K. Agarwal, D. Sylvester, and D. Blaauw. "Simple metrics for slew rate of rc circuits based on two circuit moments." in *Proc. IEEE/ACM DAC*, 2003.

[29] H. B. Bakoglu. "Circuits, interconnections and packaging for VLSI." Boston, MA: Addison-Wesley, 1990.

[30] P. O'Brien and T.L. Savarino. "Modeling the driving-point characteristics of resistive interconnect for accurate delay estimation." in *Proc. IEEE/ACM ICCAD*, 1989.

[31] S. W. Director and R. A. Rohrer. "The generalized adjoint network and network sensitivities." *IEEE Trans. on Circuit Theory*, vol. CT-16, no. 3, August 1969.

VITA

Xiaoji Ye received the Bachelor of Engineering degree in electronics and information science from Wuhan University, Wuhan, China in 2004. In January 2006, he started to study toward his master of science degree in the Computer Engineering group, Texas A&M University.

His research interests include circuit simulation and modeling, timing analysis, leakage analysis and optimization as well as organic transistor modeling.

Mr. Ye may be contacted through Texas A&M University, Department of Electrical and Computer Engineering, 111 Wisenbaker Engineering Research Center, College Station, TX 77843.

The typist for this thesis was Xiaoji Ye.