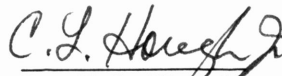
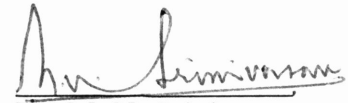


Evaluating the Quality of Small Drilled Holes In Printed Circuit Boards

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Abstract

As the spacing between components on printed circuit boards decreases, it becomes desirable to mount components in holes of ever decreasing size. Drilling these small holes presents a special problem for the PCB manufacturer. The holes must be made cleanly, with no defects, yet they must be drilled in as little time as possible. Currently, manufacturers adjust their drilling machinery manually, until they are drilling holes with an acceptable rate of rejects. The process of optimizing the drilling operation would be easier if they could predict how adjusting drilling factors would affect the resulting hole quality. In this study the relation between hole quality responses and drilling condition factors was investigated. A series of holes was drilled under different combinations of speed and feed, with temperature and force data recorded for selected holes. The holes were sectioned and photographed with a scanning electron microscope. Quality factors such as smearing, nail heading and void formation were quantized from the photographs. The statistical relationships between the quality responses and the drilling factors was examined. Void formation was inversely proportional to the temperature of the drill bit. The amount of debris found packed into the wall of the holes increased as the chip load increased. Smearing of the innerplanes decreased as chip loads and feed rates increased. Nail heading and burring were proportional to the feed rate.

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Definitions

- Burr- A ridge or lip left on the surface of the hole.
- Chip Load- Refers to the relative size of the chips being removed by the drill bit. Relative chip load may be determined by dividing feed by speed.
- Debris- Loose material left on the hole wall.
- Debris Pack- Debris deposited in a void and partially melted.
- Delamination- A physical separation between layers of substrate, or the substrate and the copper layers.
- Feed- The rate at which the drill bit moves through the material. Measured in inches per minute (IPM).
- GLM- General Linear Model. A SAS procedure.
- IPM- Inches Per Minute. A measure of feed rate.
- Nail Heading- An internal burr.
- Pressure Foot- A device on the drilling machine to ensure the work piece does not move while the bit is in contact with it. It adds to the total force being measured.
- SAS- Statistical Analysis System. A commercial statistical analysis package.
- SFM- Surface Feet per Minute. The speed at which the edge of the drill bit passes over the work piece. A measure of speed.
- Smear- Melted epoxy mechanically moved over the copper layers of the board.

- Speed- The surface speed of the drill bit, or its cutting speed. A measure of how fast the bit is cutting the material. Measured in surface feet per minute (SFM).
- Substrate- The epoxy layers that separate copper planes. These layers are made of fiber bundles layered at cross directions.
- Void- A gap in the hole wall caused by tearing out a bundle of fiber strands.

Evaluating the Quality of Small Drilled Holes In Printed Circuit Boards

I Introduction

The requirements for drilling holes in printed circuits boards (PCBs) have changed as components become increasingly miniaturized. Automated drilling machines can make thousands of holes in an hour. The operating settings of these machines are typically determined by trial and error, until an acceptable rate of defects is achieved. Manufacturers would like to be able to completely automate the drilling operation. In order to do this they must develop a model of the drilling process, and identify the controlling parameters and indications. There are good analytical models for drilling homogeneous metals with large bits, but there have been few studies into the problems of drilling PCBs.

The PCB is a composite of epoxy and copper layers that is not as easy to drill as a homogeneous material. Not only must the hole be placed accurately, with acceptably smooth walls and minimal burring, but the epoxy must not become excessively melted. The small drill bit must be prevented from bending as it drills through a stack made up of multiple boards. Minimizing the bending of the bit will ensure that the exit hole is not enlarged, and reduces bit breakage. The layers must be prevented from separating, or delaminating. Epoxy layers are made up from alternating bundles of fibers. These bundles must be kept intact, neither becoming loosened, with stray fibers or snapping off to form a void in the hole wall.

This report documents some of the research being performed at the Machining Research Laboratory in the Mechanical Engineering Department at Texas A&M University. The laboratory is conducting research designed to produce a more accurate model of the printed circuit board drilling process. To better understand the relationships between drilling factors, monitored indications, and hole quality responses, ten series of test holes was drilled under different drilling conditions. The quality of the holes was evaluated using an electron scanning microscope. Then the relationships between the factors, indication, and responses were explored.

II Background

As electronic components have become smaller, it has become desirable to locate these components closer together on a printed circuit board (PCB). This requires that large numbers of relatively small holes be drilled accurately and efficiently into the PCB (Flatt, 1988). The drilling process must not only avoid damaging the surrounding board, but must minimize any melting of the epoxy substrate material. Once melted, the epoxy can be smeared over the copper contact surfaces by the drill bit, resulting in a poor electrical connection when plated. There are other drilling defects that the PCB manufacturer tries to minimize. A rough hole that has rifling marks, or voids in the substrate material can have uneven or incomplete plating. Excessive numbers of loose fibers or debris, especially if they are packed into a void, is also a concern during the plating operation. Burrs and nail heading (internal burring) should similarly be minimized. Perhaps the most serious defect (and easiest to recognize) is a delamination defect, where the layers of the substrate become separated from each other or the surrounding copper. It is difficult and time consuming to examine all of these hole quality factors quantitatively during manufacturing operations, and few manufacturers have even attempted this task (Berlin, 1983). Usually holes are inspected visually and determined to be either "good" or "bad."

Typically, manufacturers control their drilling operations by a combination of two methods. Test coupons are included on circuit boards for regular inspection by quality control personnel. If the holes are unsatisfactory the drilling parameters are adjusted. Another method of monitoring drilling operations involves the wear of the drill bit (Deitz, 1983). If bits wear or break excessively, the drilling parameters are modified. This approach is based on the premise that a worn bit cannot drill satisfactory holes, and that ensuring that the drill bits are in good condition ensures that good holes are drilled. For drilling operations in large, homogeneous materials, this is a good approach. The theory of machining for a large size, uniform material has received considerable attention. The relationships between feed, speed, and other drilling factors have been empirically determined for a wide number of drilling conditions, and may be utilized when analyzing similar situations. However, the application of the large scale theory to the small scale situation has not produced entirely satisfactory results. The effects of the composite layers and the low glass transition temperatures affect drilling in ways not predicted by the large scale theory. To build a more reliable model, more data is needed on the relationship between drilling factors and the resulting holes when a printed circuit board is drilled.

The objective of this project is to examine the relationship between drilling parameters and hole quality factors. This information will be useful in monitoring drilling operations (Archer-Burton, 1984). It may be possible to use several easily monitored variables (such as temperature and force) to control the drilling process instead of continually monitoring test coupons and drill bit wear. A study by the Laminating Company of America concluded that there was a positive relation between burr size and overall hole quality (Yasumatsu, 1989).

III The Research Project

A. Machining Research Laboratory

Installed in the Machining Research Laboratory at Texas A&M is an Excellon Mark III automated printed circuit board drilling machine. This machine, donated to Texas A&M by International Business Machines (Austin Plant), is used to conduct research into printed circuit board manufacturing at Texas A&M (see Figure 1). Dr C. L. Hough leads the circuit board project, with Mr. Bob Bolton, a doctoral student, being the primary researcher .

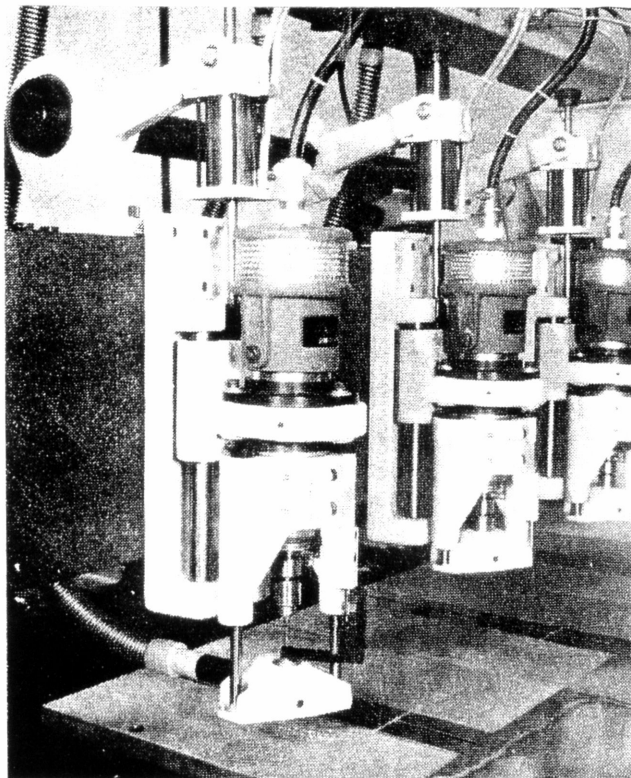


Figure 1. Excellon Drilling Machine (From Excellon Drilling Machine Manual)

The drilling machine has four spindles that are mounted above an X-Y positioning table. When the table has moved the circuit board to the desired location, the spindle is lowered until the drill bit makes the required hole. The temperature of the drill bit is monitored by a Vanzetti fiber optic sensor as the bit enters and exits the printed circuit board. A Kistler dynamometer is positioned under the board to monitor drill forces. The force measured by the Kistler includes the force produced by the pressure foot of the drilling machine, which holds down the board during drilling, as well as the bit forces. Pressure foot force is considerably greater than bit drilling force, which makes the determination of bit force difficult. Mr. Bolton is attempting to isolate bit force from the total force measured by the Kistler. However, no reliable bit forces were available for statistical analysis in this study.

B. Projects in Progress at the Machining Laboratory

The machining laboratory is conducting a research project whose purpose is to evaluate and develop sensor monitoring systems for measurement of temperature and force during drilling (Bolton, January 1991). Using the sensor data the lab hopes to be able to optimize and control the drilling process in real time in order to produce better circuit boards. Currently, the main effort of the project is to develop a model of the drilling process that can predict the resulting quality of the circuit board from the drilling configuration and the sensor response data. Mr. Bolton's analysis, of all the holes drilled by the project, show that bit wear and speed have quantifiable effects on bit temperatures. The effect of chip load and feed rate has not been determined. Some data indicates a reduction of bit temperatures at higher feed rates due to less time in the hole (Bolton, March 1991).

In order to evaluate the drilling process, it is necessary to establish some criteria to evaluate the quality of the holes in the circuit boards being drilled. This is the subject of this report. One company, The Laminating Company of America, has published an evaluation method, based on the condition of the copper and the substrate in the drilled hole (Berlin, 1983). The quality responses that L.C.O.A. has identified, including amount of delamination, amount of burring and nail heading, and the fraction of copper surfaces covered by smear were selected to evaluate the quality of the copper layers in the holes. The condition of the substrate layers were evaluated by examining the amount of voids

present, the amount of loose debris present, and the amount of debris packed in voids. These substrate quality responses are similar to those recommended by L.C.O.A.

Having decided on an evaluation criteria, it is possible to compare the impact of the drilling factors on the resulting hole quality. A preliminary test plan was designed to generate quality data under a wide range of drilling conditions. The relationships observed between the drilling factors and the quality responses will be considered when designing further experiments.

C. Design of the Drilling Test Plan

A drilling test plan was developed by Dr. Hough and Mr. Bolton to yield the greatest possible range of test data. It is difficult to remove the effects of wear on the drill bits being used from any drilling experiment without making a large number of replications of the experiment. The test plan was designed to avoid this problem by taking advantage of the wear behavior of the drill bit (see Figure 2). When a bit is first used, it wears rapidly, until it is broken in. During its useful lifetime, the wear of the bit, on average, is proportional to the number of holes drilled with the bit. Most 42 mil bits are changed out after drilling more than 7000 holes. With only 5000 holes in the study, all of the data was taken during the useful life of the bit. Only at the end of its normal lifetime does the wear rate increase. By repeating the initial set of drilling conditions near the end of the test, it was possible to see the effect of bit wear on hole quality. This permits a qualitative analysis of the effects of varying the drilling factors on the resulting hole quality. However, quantitative analysis is not reliable without drilling a larger sample of holes. A computer failure in the drilling machine has delayed drilling any holes beyond this preliminary test plan.

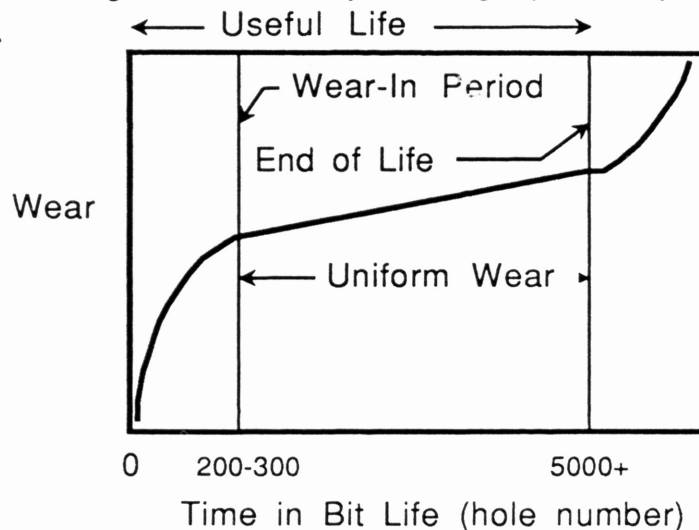


Figure 2. Typical Bit Wear Pattern, 42 mil bit

D. The Drilling Test Plan

The drilling test plan was designed to investigate the effects of speed and chip load on hole quality, while monitoring drilling force and bit temperature (see Table 1 and Table 2). Chip load is a term that describes the relative size of chips that are removed during machining. As the drill feed rate increases, larger chips are removed during one revolution of the bit. Increasing the speed of the drill bit, which is independent of the feed rate, forms smaller chips, lowering the chip load. The drill speed was set at each of three speeds (500, 600, 700 SFM) and the feed rate was varied to produce chips at three relative chip loads (2, 3, 4 mils/revolution of the drill bit). The middle combination (600 SFM, 3 mils/rev) was drilled first for a break-in block, then repeated later in bit life. The other eight combinations of speed and chip load were drilled in random order. This generated 10 sets of drilling test data, at nine different combinations of drilling factors.

Table 1. Summary of Drilling Factors

Drilling Factor	Level
Speed	500, 600, 700 SFM
Chip Load	three relative sizes- 2, 3, 4 mils/rev (feed rates 91-254 IPM)

Table 2. Monitored Indications

Indication	Monitoring Device
Bit Entry and Exit Temperature	Vanzetti fiber optic probe
Drilling Forces	Kistler dynamometer

In industry multiple boards are typically stacked together and drilled simultaneously. In this study stacks made up of IBM-two power plane boards were selected for drilling. The stack was covered with a piece of LCOA EO+ entry material, and backed up with a LCOA 50 mil phenolic board. A 42 mil Kemmer SIFI carbide bit was used to drill the holes on the Excellon drilling machine. This is a configuration similar to that used at the IBM Austin facility. The Excellon drilling machine was programmed to drill ten sets of test holes. Each set of 500 test holes was laid out in an identical pattern to

ensure that the drill bit spent the same amount of time between holes. This ensured that the drill bit did not cool off differently while drilling different test sets (see Table 3).

Table 3. Summary of Constant Drilling Parameters

Drilling Parameter	State
Drill Bit	42 mil Kemmer SIFI
Circuit Board Stack	two IBM-2 power plane boards
Entry Material	LCOA EO+ laminated aluminum
Backup Material	LCOA 50 mil phenolic
Holes per Drilling Combination	500

The circuit boards used in the study were production boards which had wire runs laid out in them. The drilling pattern was a uniformly spaced matrix of holes that did not attempt to select locations with uniform composition. This caused some variation in the hole appearance and a large variation in the temperature data. If a large number of copper layers was drilled through, the temperature was cooler and the hole appearance was quite different than if a location with few copper layers was drilled through. For hole quality evaluations, holes were selected that had identical compositions (two power planes, no circuits cut through, see Figure 3).

IV Examination of Test Holes

A stack containing two circuit boards was drilled using the above described test plan. Ten series of 500 holes on the bottom board in this stack were used for hole quality analysis. The circuit board was sectioned to expose the first 20 and last 19 holes in a test series. Sectioning was performed by cutting the holes with a diamond saw blade. Loose debris was removed with compressed air. These holes were examined with an optical microscope to select representative holes for electron microscopy. Forty-two representative holes were photographed using a scanning electron microscope at X50 magnification (overall view of hole), X200 magnification (selected ends), and at X750 magnification (selected innerplanes). A JEOL T-230 scanning electron microscope was used in the investigation. Specimens were lowered to the greatest focal distance to obtain the greatest depth of focus over the curved hole surface. A beam accelerated to 30 KV was

used to generate backscattered electrons from the gold coated specimen for monitoring. Photographs were taken with Polaroid type 52 or type 54 instant film.

Hole quality measurements were made from these photographs. Hole quality measurements were made for both the substrate and the copper areas. The copper areas were categorized by the amount of smearing over the copper (none, light, or heavy) (Table 4). Light smear appeared as a slight unevenness of the innerplane surface as if there was small bubbles on the surface. Heavy smearing was characterized by a lumpy mass of epoxy extending out from the substrate layers (see Figure 4). At higher electron beam acceleration voltages (> 20 KV), it was possible to detect the innerplane layer below the smear. At lower acceleration voltages the smear obscured the innerplane below. The size of the largest burr and the largest nail head (internal burr) were also measured from the photographs. In Figure 4 there is a large nailhead at the lower right corner of the innerplane. In Figure 5 there is a nailhead under the 1 in the 10 micrometer scale. Substrate area defects were categorized into areas with voids in the substrate and areas with packed debris in the substrate (see Figure 6 and Figure 7). Using an acetate overlay the photographs were gridded into eighth inch square sections. The sections were sorted by quality parameter and the total number of sections of each type was recorded (see table 5).

Table 4. Summary of Copper Quality Responses

Quality Factor	Evaluation Method
Smearing- Heavy Light None	% of area covered by smearing was measured by counting grid areas
Debris	% of area covered by loose debris was measured by counting grid areas
Nail heading	Size of largest nail head measured
Burring	Size of largest burr measured

Table 5. Summary of Substrate Quality Responses

Quality Factor	Evaluation Method
Largest Void	Diameter of the largest void measured
Voids	% area covered by voids measured by counting grid areas
Packed Debris	% area covered by debris packed into voids measured by counting grid areas
Debris	% area covered by loose debris measured by counting grid areas

Some holes were examined without sectioning the board. A test section was cut from the surrounding board with tin snips. These smaller sections were coated with gold for examination under the electron scanning microscope. When under the microscope, these sections were tilted at an angle of 45 degrees. This allowed them to be photographed without cutting the hole wall and potentially disturbing the surface. Photographs of these holes have a distinctive curvature to them, but are otherwise similar to the sectioned photographs (see Figures 8 and 9).

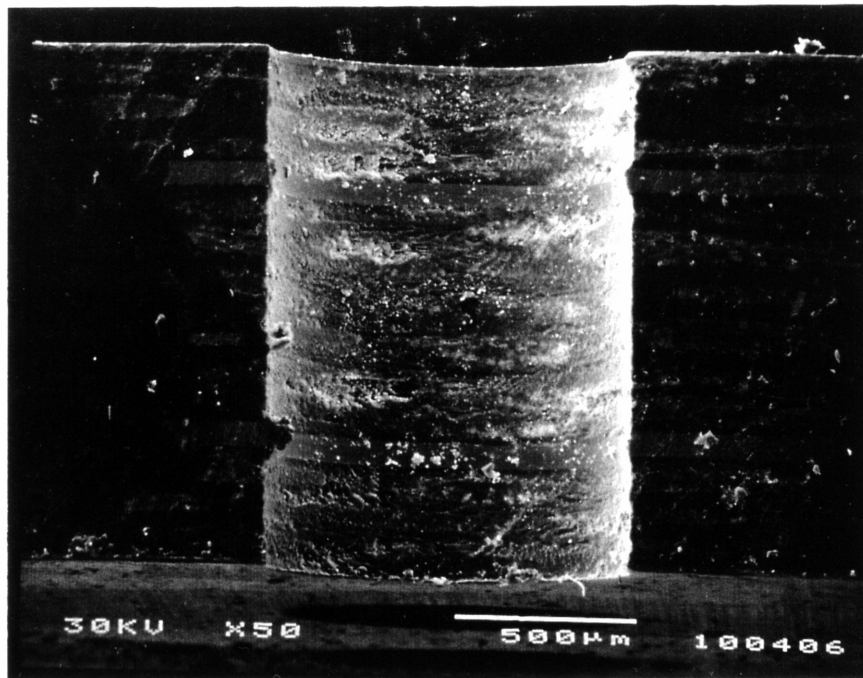


Figure 3. Typical Hole Cross Section

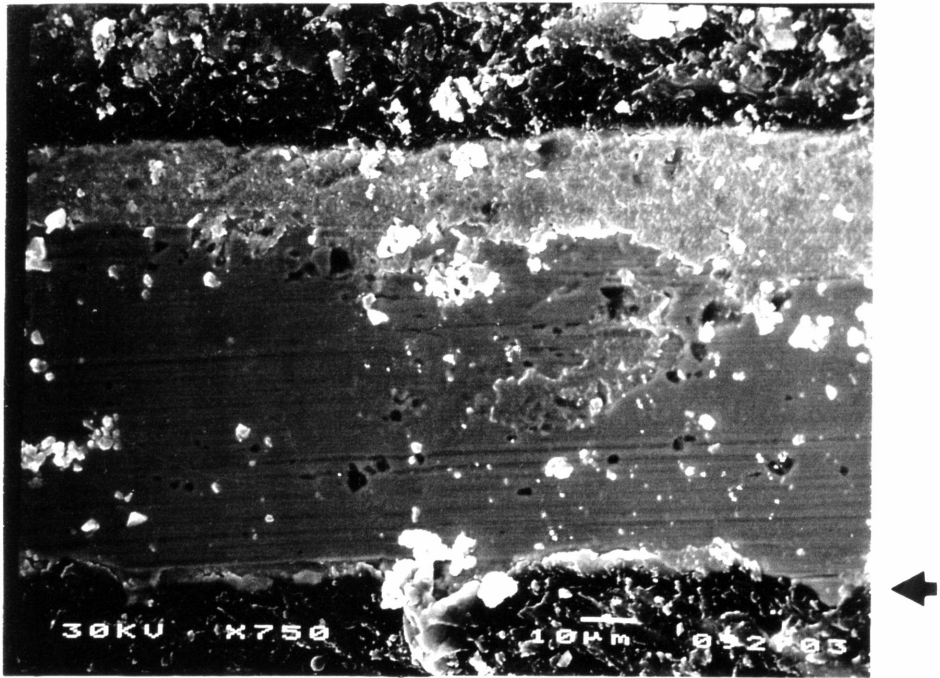


Figure 4. Example of Smearing

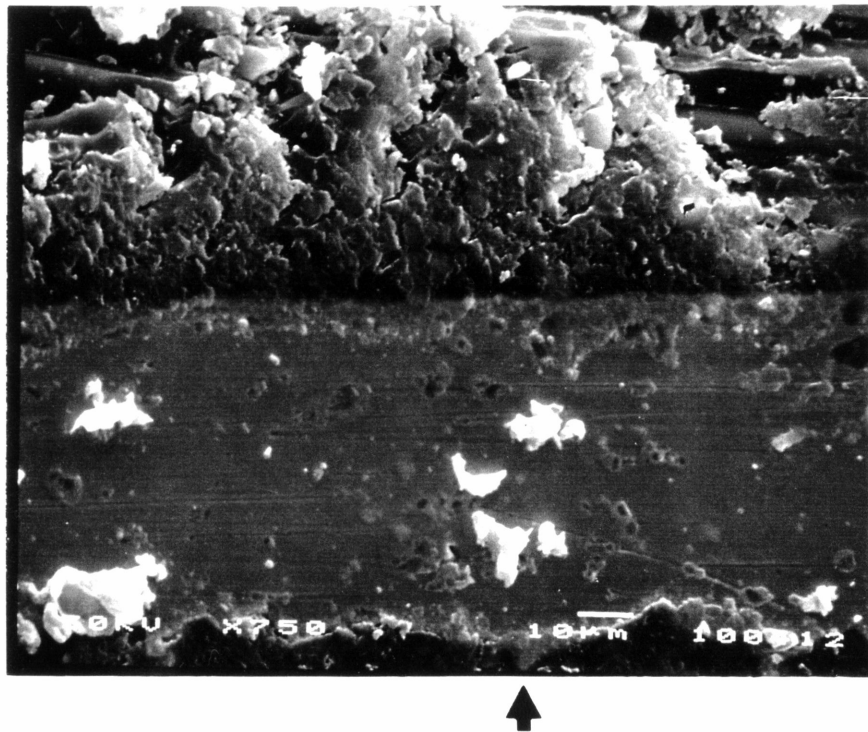


Figure 5. Example of Nail heading

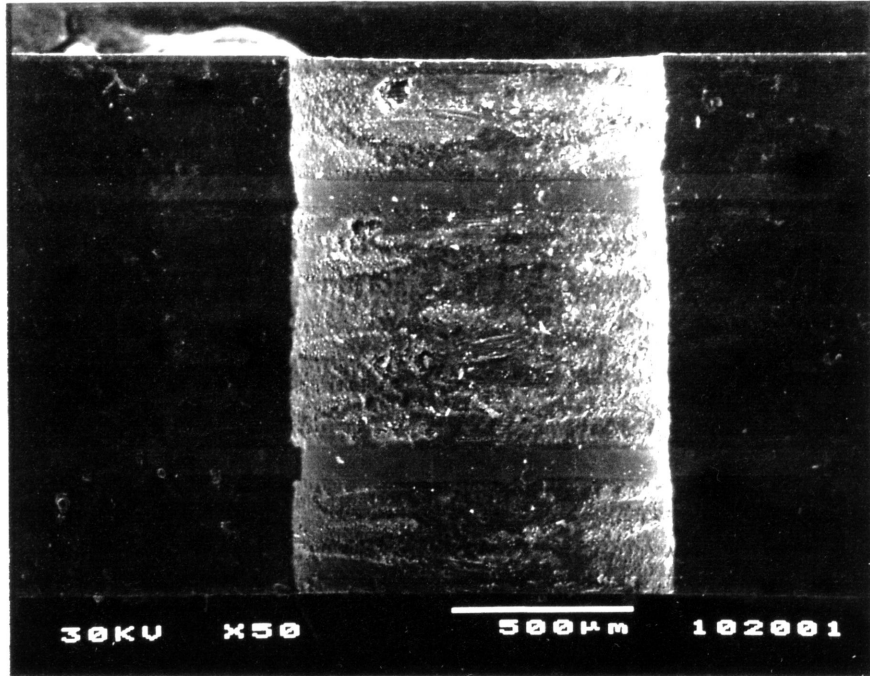


Figure 6. Example of Void

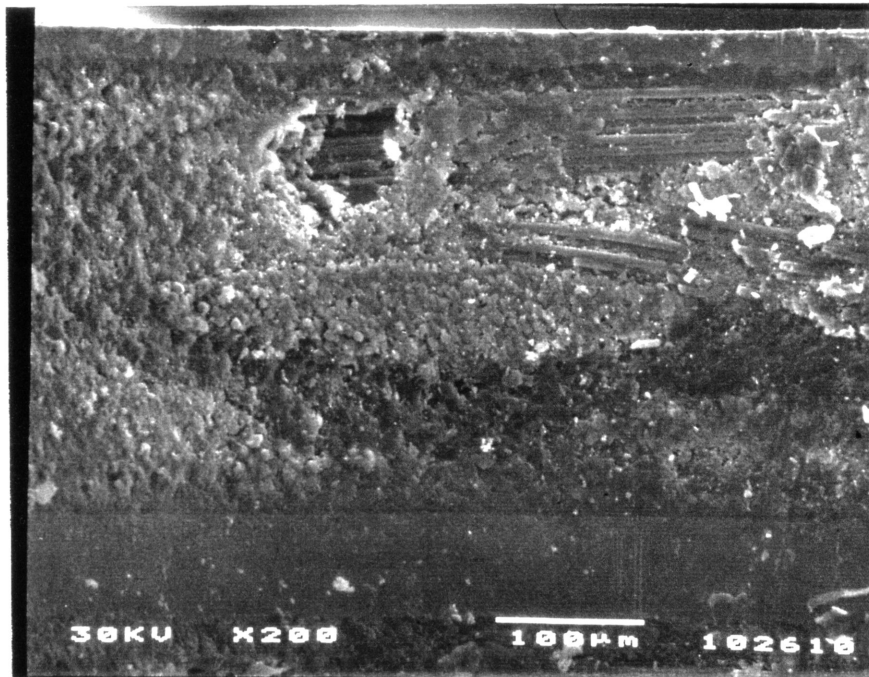


Figure 7. Detail of Void

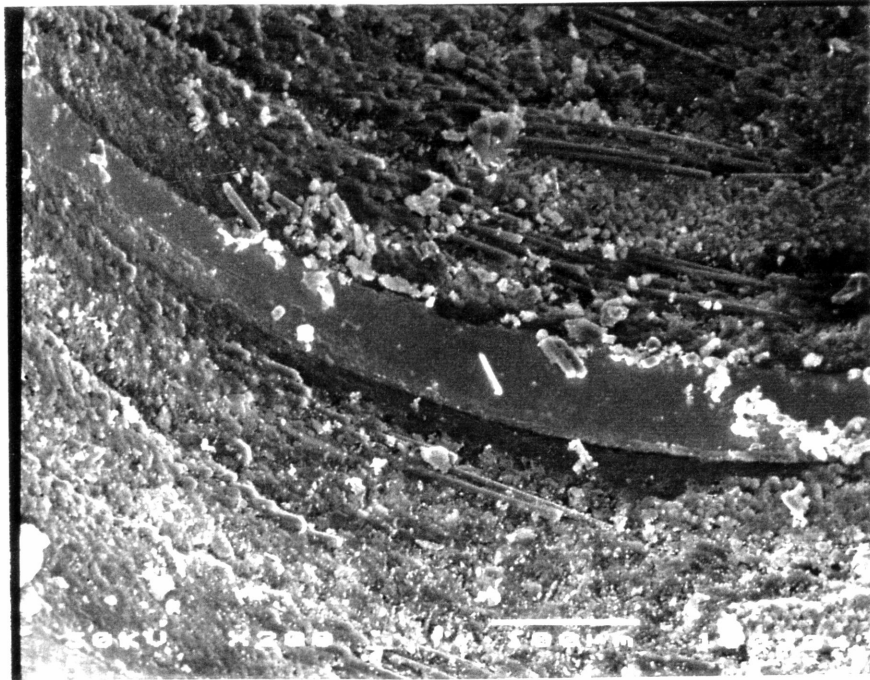


Figure 8. Example of Tilted Hole (X200)

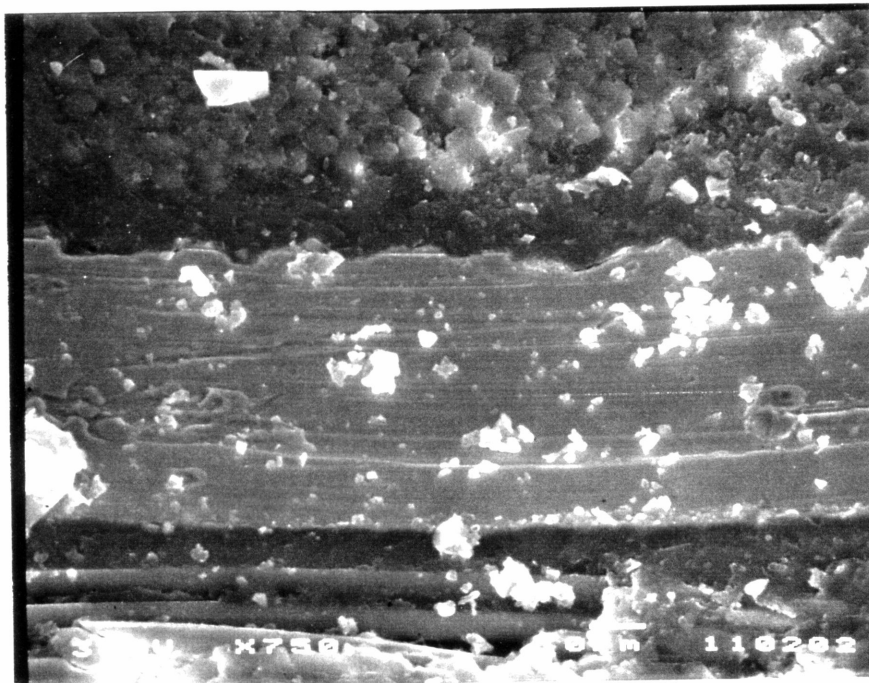


Figure 9. Example of Tilted Hole (X750)

V Results

The quality data was stored in spreadsheet form. In order to determine the correlations between the variables, a statistical model was employed. An analysis of variance was made using the General Linear Model (GLM) PC SAS routine. The limited amount of data has significant dependencies between the drilling factors introduced by the test procedure and wear. This complicates the quantification of the effect of any one drilling factor on hole quality. However, by examining a scatter plot of two selected variables, bit exit temperature and speed, along with the SAS output, one can postulate the relationship that exists (see Figure 10). The low $P > [T]$ value at the bottom of the Figure 11 SAS output indicates a low risk (Type I) of falsely concluding that speed has an effect on temperature. Relevant SAS results and scatter plots for the remaining results are contained in the appendix. For void relationships, examples of test data (averaged over several neighboring holes) are plotted for selected conditions, where only one drilling condition variable varied significantly.

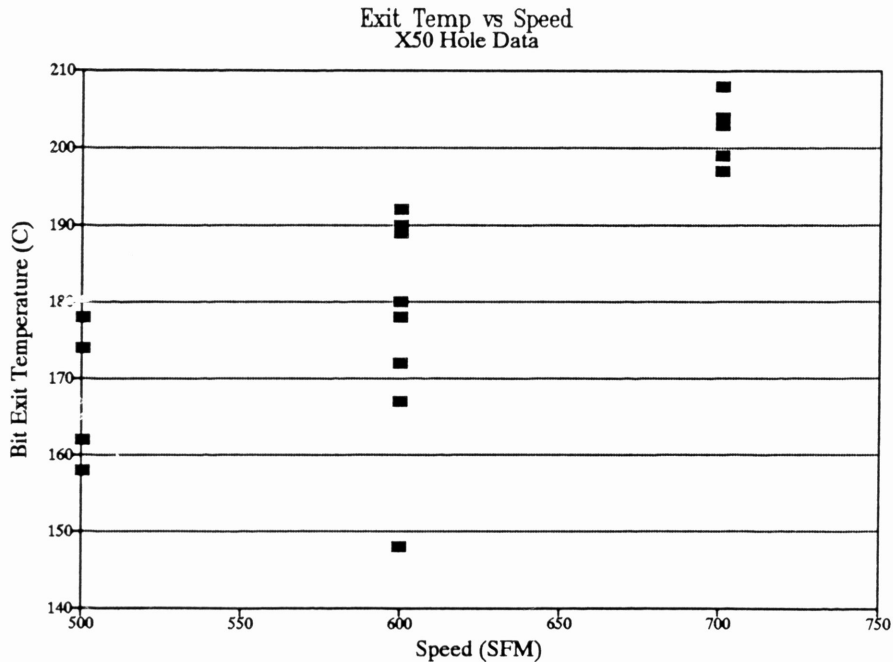


Figure 10. Scatter Plot of Temperature-Speed Relationship

General Linear Models Procedure

Dependent Variable: TOUT

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	2	5732.612464	2866.306232	23.28	0.0001
Error	36	4432.361895	123.121164		
Corrected Total	38	10164.974359			

R-Square	C.V.	Root MSE	TOUT Mean
0.563957	6.095843	11.09600	182.025641

Source	DF	Type I SS	Mean Square	F Value	Pr > F
CHIPL	1	1758.426679	1758.426679	14.28	0.0006
SPEED	1	3974.185785	3974.185785	32.28	0.0001

Source	DF	Type III SS	Mean Square	F Value	Pr > F
CHIPL	1	374.799541	374.799541	3.04	0.0896
SPEED	1	3974.185785	3974.185785	32.28	0.0001

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	100.9113703	4.84	0.0001	20.83883674
CHIPL	-4.5851510	-1.74	0.0896	2.62797043
SPEED	1.7287763	5.68	0.0001	0.30428537



Figure 11. SAS Output For Temperature-Speed Relationship

A. Temperature Relations

This is a summary of the observed temperature relations in the holes selected for hole quality measurements. A more detailed analysis of the temperature data for all the holes drilled is contained in the project report (Bolton, January 1991).

There was a strong relation observed between the temperature of the drill bit, both entering and exiting the circuit board, with the surface speed of the drill bit and the hole sequence number. As surface speed increased the bit temperature increased. A higher surface speed causes the bit face to move over the hole surface at higher speeds. This would create more friction in the hole, resulting in higher bit temperatures.

Bit temperatures also increased over the life of the bit. Some of this temperature rise was due to the order in which the sections were drilled, and some of it was due to the wear of the bit. In his report, Mr. Bolton has demonstrated that bit temperature does increase over the life of the bit, but it is not possible to isolate that relationship using this test data. As the bit was used, it was worn down. A worn bit will not cut as well as a new bit, with the chips being formed by plastic deformation, instead of cleanly shearing off. This increased deformation in the formation of chips could also increase the temperature of the drill bit.

One further factor had a significant effect on the drill bit temperature. This was the relative chip load. An increasing chip load could have either a positive or negative effect on the bit temperature, depending on the exact values selected for the speed and hole number relationships. The size of the chips could be expected to have an affect on the rate of heat removal from the drill bit, affecting bit temperature.

B. Void Relationships

The voids observed in the hole walls share some common features. Typically the void would be shaped like a swimming pool, with one end of the void being deeper than the other end. Strands of epoxy fibers run parallel to the void bottom. At the deep end of the void, the epoxy fibers are sheared off perpendicular to the void surface. It seems reasonable that a fiber bundle has been caught by the drill bit and been snapped off instead of being cut by the bit (see Figure 7). Only at the edge of these fiber bundles, where the bit has cut most of the bundle do these voids seem to form.

The factor that had the strongest correlation to void formation was temperature. As bit temperature increased, the fraction of the hole surface that contained voids decreased. A hotter bit temperature indicates that the hole was hotter during the drilling process. A hotter bit would be more likely to cut a fiber bundle instead of just catching and pulling on it. This could explain why voids were less common at higher temperatures (see Figure 12). In this graph data averaged from the first and last holes in a test block (hole numbers range from 2007 to 2483) are compared to isolate the effect of temperature.

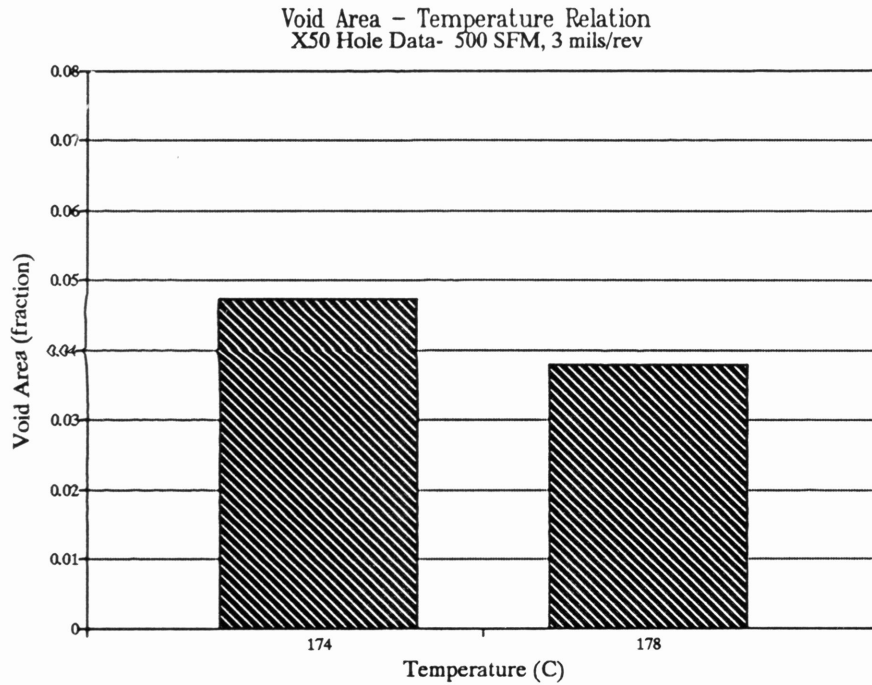


Figure 12. Example of Temperature Effect on Void Area

The other variables that were related to void formation were the same variables that affected drill bit temperature (hole number, speed, and chip load). The effect of these variables on void formation was consistent with their effect on temperature. For example, as bit speed increased, temperature increased and void formation decreased. It was not possible to separate the effect of these factors had on void formation that was not caused by the change in drilling temperature (see Figures 13, 14, 15). These plots generated by taking the average of void area data where the desired variable was approximately constant. They represent typical relations and are not intended to indicate numerical relations, only trends in the data.

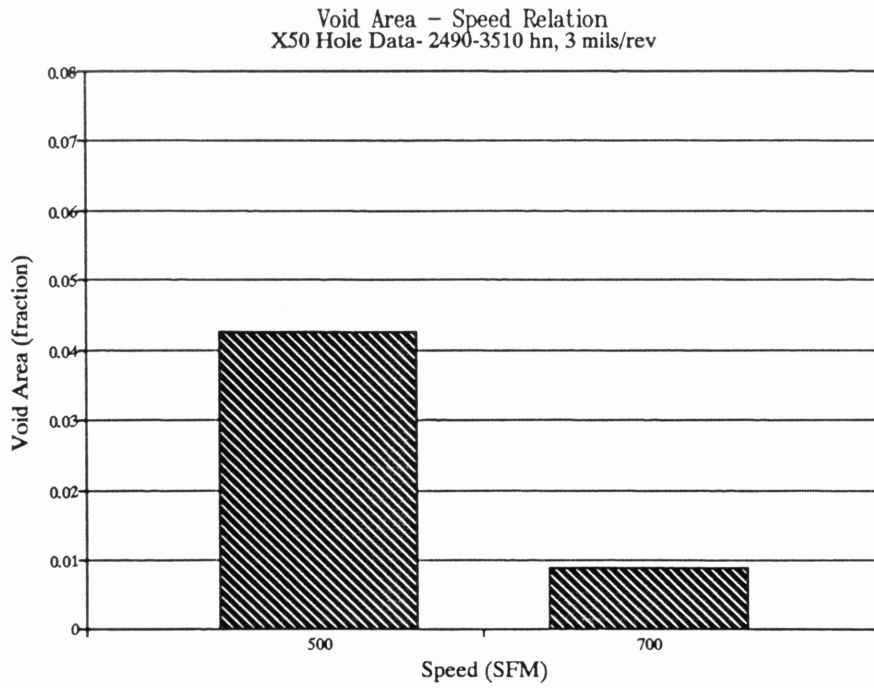


Figure 13. Example of Speed Effect on Void Area

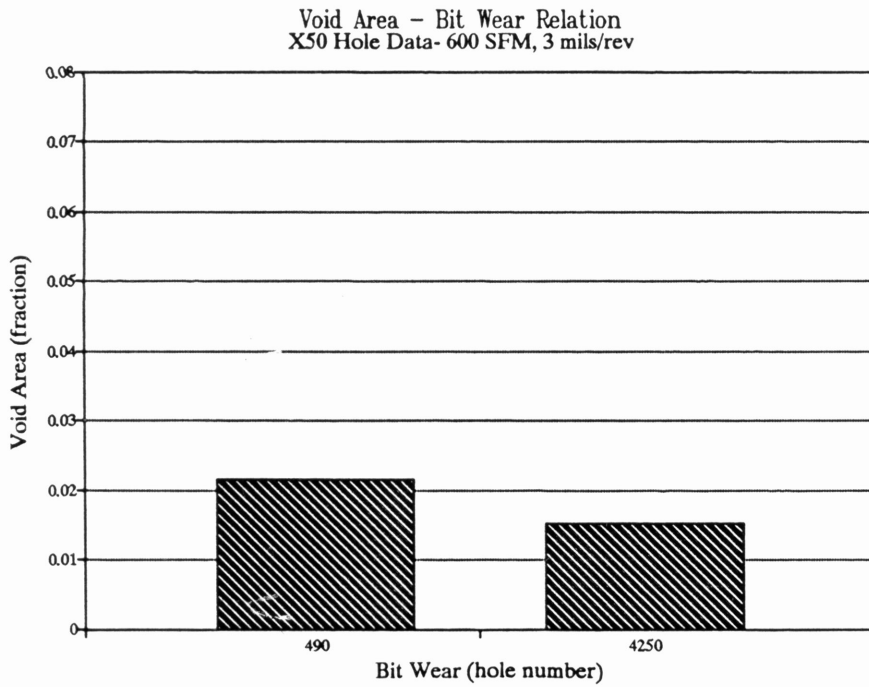


Figure 14. Example of Bit Life Effect on Void Area

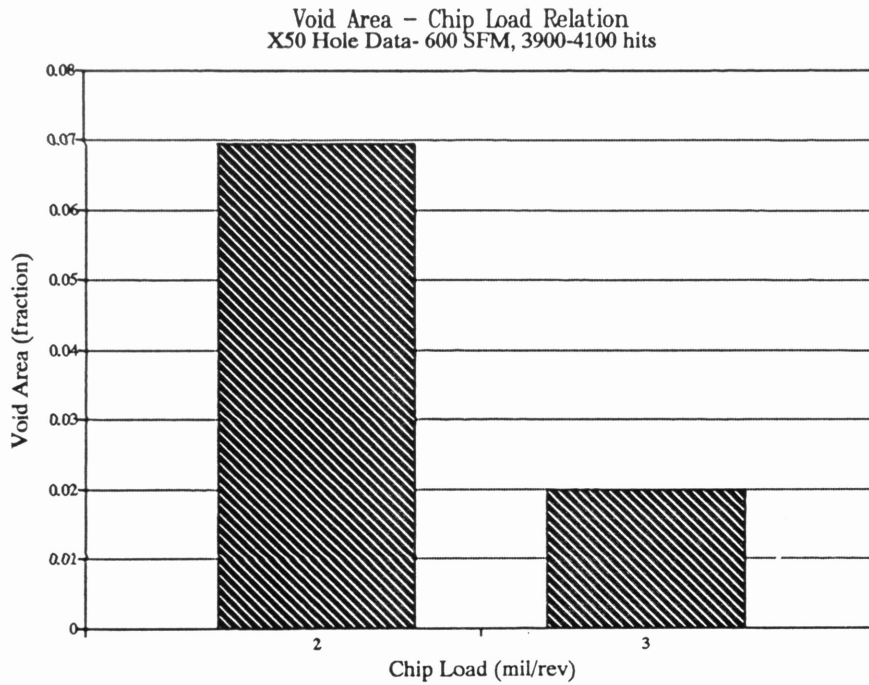


Figure 15. Example of Chip Load Effect on Void Area

The effect of the wear-in of the drill bit is very significant. The fraction of surface area covered by voids fell significantly in the first set of holes drilled. This reduction in voids corresponds with an rapid increase in bit temperature over the first 300 holes. No other series of holes had as much variation in the amount of void area over the 500 holes in the block (see Figure 16).

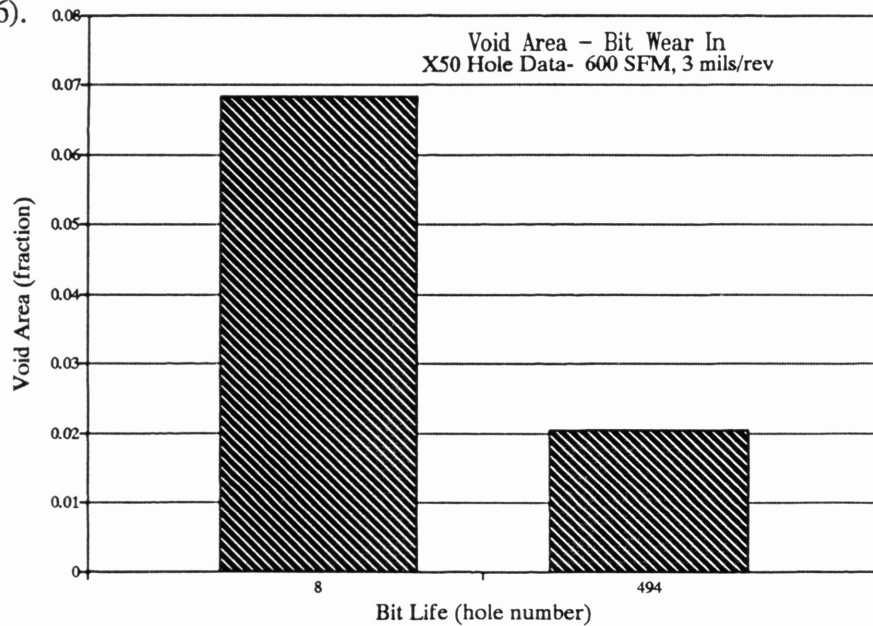


Figure 16. Wear-In of Bit: Effect on Void Area

C. Packed Debris Relations

On many holes there were some voids that contained packed debris. This debris was similar in size and shape to the loose debris that was not in voids. The amount of packed debris was related to two primary factors, chip load and bit temperature.

The factor with the greatest effect on packed debris was chip load. As chip load increased, the amount of packed debris increased. Smaller chips would be less likely to be trapped in a void, contributing to the amount of packed debris. Also, removing larger chips would make it more likely to break a number of fibers in a strand, without totally separating the strand. These damaged strands would appear as packed debris. The effects of increasing feed, a component of chip load, were consistent with those of increasing chip load.

An increasing bit temperature caused the amount of packed debris to decrease. A hotter bit would be more likely to entrain debris in its wake as it was retracted from the hole.

D. Heavy Smear Relations

Two observations can be made in relation to the presence of heavy smearing of the innerplane. Firstly, the smear observed was always heavier on the lower portion of any innerplane. It appeared to have been carried on to the innerplane by the bit as the bit was retracted. There was heavy smear on top surfaces of many innerplanes, but it was approximately 10% of the size of the smear from the bottom of the innerplane.

Secondly, the amount of heavy smear decreased as the chip load and feed rates increased. Larger chips would have a higher thermal mass, and would be less likely to melt together. A larger chip would be more likely to be removed by the drill bit as it was retracted.

There were no significant effect on smearing that was directly relatable to the changing bit temperature, however, feed rate observed to be a significant factor in the amount of heavy smearing present. As the feed rate of the drill bit was decreased, the

amount of heavy smearing increased. This result can be understood if one remembers that the melting of the epoxy is a function of the total energy radiated from the drill bit, and not the bit temperature alone. The total energy passed from the bit to the hole is a function of the rate of power transmission and the time in the hole. A lower feed rate would keep a hot drill bit in the hole longer, radiating more energy into the substrate. The feed rate was varied by a factor of three during testing, explaining why it had a significant effect on the smearing found. Bit temperatures varied by 30 to 40 degrees Celsius. On an absolute scale, this is a variation of only seven percent. Such a small variation would have correspondingly small effects on the amount of smearing produced. With the limited amount of data available, it was not possible to detect this effect.

E. Burr and Nail heading Relationships

All of the holes that were examined had some burring and nail heading. The only drilling factor found to be related to the size of the nail heading and burring was the feed rate. As feed rate increased, the observed nail heads and burrs became larger. A nail head or burr is created by the drill bit pushing a piece of copper from its normal location in the hole wall, and represents a failure of the bit to cut the copper before the copper is deformed. A higher feed rate increases the force applied to the circuit board, making it more likely that the copper would be deformed into a nail head or a burr instead of being cut.

F. Remarks

These results are summarized in Table 6. The relationships observed can be quantized as more data becomes available for analysis.

Table 6. Summary of Observed Relationships

Variable	Related Variable	Relationship
Temperature- entering - exit	Speed	Directly
	Time in bit life	Directly (?)
	Chip Load	Weak
Voids	Temperature (both)	Inversely
	<i>Speed</i>	<i>Inversely</i>
	<i>Time in bit life</i>	<i>Inversely</i>
Packed Debris	Chip Load	Directly
	<i>Feed</i>	<i>Directly</i>
	Temperature (both)	Inversely
Heavy Smear	Chip Load	Inversely
	Feed	Inversely
Burring and Nail Heading	Feed	Directly

Note: Italicized quantities are secondary relations, their contribution is contained in the primary relation, which is directly above. (ie. *Feed* is a secondary relation of Chip Load in Packed Debris, but both Feed and Chip Load are primary relations for Heavy Smear.) The related variables are ordered by the strength of their effect on the Hole Quality Variable, with the strongest variables being first in each section.

VI Recommendations

There are a number of recommendations that can be drawn from this project for use in designing further experiments. The examination of the hole quality of the samples using the electron scanning microscope could be improved. A sectioned 42 mil test sample was found not to give better data than a test sample that was merely tilted. Tilting the section under consideration allows the researcher to view the hole without damaging the wall, and reduces the number of operations in the evaluation process. Tilting may not be feasible for holes smaller than 42 mils, due to the difficulty of viewing the innerplane.

It was possible to identify hole quality features using the optical microscope. A color image was especially useful in determining the amount of copper debris relative to the amount of epoxy debris. The problems with this technique was that the microscope could only focus on a small section of the curved hole, and that the smear obscured the innerplane. Smear over the innerplane made it difficult to measure the exact amount of smear, and to separate nailheading from smearing. These shortcomings could be fixed if the microscope was equipped with a vision system and a dynamic focusing routine. The innerplane could be compared to a reference innerplane to determine the extent of smearing.

The condition of the drill bit, or the number of holes drilled with any particular bit seems to have a significant effect on the resulting hole quality, and the bit temperature. The data obtained does not show any of the characteristics that would indicate that the end of the drill bit life was approached during the test. It would be desirable to perform a test that investigated the effect that bit wear (life) has on both of these variables. It would be especially interesting to determine the wear-in period and the end of useful life for a number of drill bits. Monitoring the condition of the drill bit would be necessary to ensure that the bit condition is reflected in the bit performance (hole quality and temperature). In the lab this could be done by photographing the bit at selected points during drilling. This will not be a satisfactory solution for the manufacturing process.

Further studies should consider isolating the effects that drilling material has on the hole quality. If the circuit boards were of uniform make-up without any circuits between layers, or if the drilling pattern was selected to hit areas of uniform composition, then it would be easier to relate quality information to the drilling factors. Drilling sets of boards

with varying numbers of innerplanes would yield data on how the composition of the board affects drilling performance.

VII Summary and Conclusions

One must keep in mind that the test data represents the results of drilling with only a single 42 mil bit, without replications of the test plan. Testing was performed in the wear-in and uniform life of the bit. From this test data the following relationships were observed:

1. More voids form at lower drill bit temperatures.
2. Packed debris increases with increasing chip loads.
3. The formation of heavy smear on innerplane layers can be decreased by increasing chip load and feed rates.
4. A higher feed rate increases the size of burrs and nailheads.

If this data can be generalized to other circuit board drilling situations then there are a number of implications for printed circuit board drillers. A major conclusion is that bit temperature cannot be exclusively used to predict the hole quality of drilled circuit board. The temperature can be useful in avoiding excessive numbers of voids, but it is a poor predictor of heavy smearing, and burring problems. In fact, a higher bit temperature had no adverse effects on the holes examined. An increase in smearing may eventually result from a rising bit temperature, but a changing feed rate had a greater effect on the amount of the smear. It may not be necessary, from a hole quality standpoint, to aggressively cool the drill bit, by employing a vacuum board or lowered the time between hits.

There is a trade-off in the various quality factors when drilling holes in printed circuit boards. This is the major implication for printed circuit board manufacturers. One can reduce the amount of any particular hole quality defect by modifying the drilling factors, but this will create more of another type of defect. For example, one can decrease the number of voids by increasing the drilling feed and speed. However, this will increase the likelihood of having packed debris, nail heading, and burring problems. No single prescription can cure all hole quality problems.

An observation is related to hole quality. At many plants, the drilling process is monitored by visually inspecting drill bits. If a bit is unacceptable worn, then it is replaced. The holes are only checked after they have been plated. As these results show, it is possible to have a perfectly good drill bit producing defective holes due to a selection of adverse drilling factors. Manufacturers should consider periodically checking their circuit boards after drilling and prior to plating. This would allow them to be sure that problems in holes are not produced by factors unrelated to bit wear.

The methodology employed in this test, with the possible exception of the tilting technique, could be used in a more extensive study, with more replications and greater variation of test factors. This could generate the quantitative results needed to optimize the drilling process in printed circuit boards.

References

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Appendix- SAS Results

Understanding SAS Results

The GLM procedure attempts to fit a linear curve between the dependent variable (DV) and the independent variables (IV). The form of the solution is:

$$DV = \text{Intercept} + (IV_1)(\text{Slope}_1) + (IV_2)(\text{Slope}_2) + (IV_3)(\text{Slope}_3) + \dots$$

The values of the intercept and the slopes for the independent variables are calculated using a least squares type routine. They are printed at the bottom of the SAS printout with the value of the variable being listed in the Estimate column. The value of one standard deviation is listed in the Std Error of Estimate column. A qualitative measure of the "goodness" of the fit is reflected by the F Value. A higher F Value indicates a better fit. The F Value is displayed for the model as a whole at the top of the printout, the fit of each of the independent variables is printed in the center of the page (Type I is order dependent, Type III is order independent). For more information see the SAS manual.

Results Included

Scatter plots and SAS results are included for variables discussed in the results section of the report.

SEQUEL	RC	HL	SP	ST	SM	SM	SM		
15 D F	102606	4 2	3990	109 54.5	2 115 192	2.6316	73.6842	23.6842	0.00000
16 D F	102605	4 2	3990	109 54.5	2 115 192	2.6316	71.0526	26.3158	0.00000
17 E 1	101110	3 1	2007	136 45.5	3 110 174	92.1053	7.8947	0.0000	0.84211
18 E 1	101109	3 1	2007	136 45.5	3 110 174	84.2105	13.1579	2.6316	0.63158
19 E F	101902	3 1	2485	136 45.5	3 109 178	76.3158	21.0526	2.6316	1.05263
20 E F	101901	3 1	2485	136 45.5	3 109 178	21.0526	71.0526	7.8947	0.42918
21 F 1	100406	3 2	513	182 45.5	4 99 158	64.1026	25.6410	10.2564	2.73684
22 F 1	100407	3 2	513	182 45.5	4 99 158	47.3684	42.1053	10.5263	1.75055
23 F F	100410	3 2	999	182 45.5	4 102 162	76.3158	18.4211	5.2632	1.68421
24 F F	100411	3 2	999	182 45.5	4 102 162	41.6667	58.3333	0.0000	2.07039
25 G 1	92911	2 1	4007	164 54.5	3 121 190	5.2632	42.1053	52.6316	0.00000
26 G 1	92903	2 1	4007	164 54.5	3 121 190	0.0000	44.7368	55.2632	0.00000
27 G F	100401	2 1	4483	164 54.5	3 121 189	65.7895	23.6842	10.5263	0.00000
28 G F	100402	2 1	4483	164 54.5	3 121 189	17.8571	60.7143	21.4286	0.00000

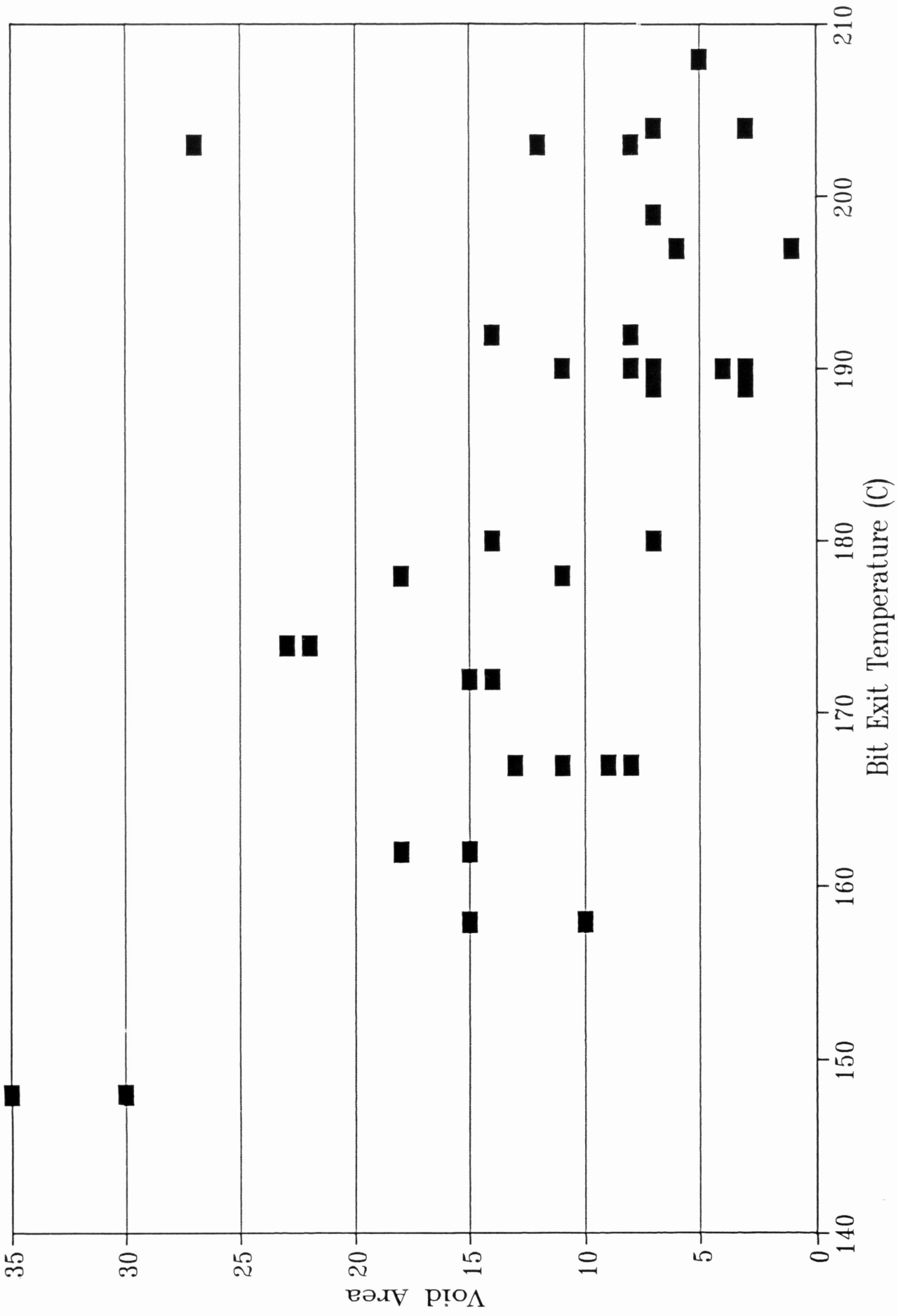
DEBSA	V	DI	SM	TEA	SM	SM	SM	SM	SM
15 1.26316	2.94737	n	n	400	77	76.316	97.368	1.26316	2.94737
16 0.63158	1.68421	n	y	300	77	73.684	97.368	0.63158	1.68421
17 1.68421	4.63158	y	y	250	64	100.000	7.895	2.52632	5.47368
18 2.10526	4.84211	y	n	250	64	97.368	15.789	2.73684	5.47368
19 0.63158	3.78947	n	n	275	69	97.368	23.684	1.68421	4.84211
20 0.42918	3.86266	y	y	225	69	92.105	78.947	0.85837	4.29185
21 1.47368	2.10526	y	y	275	59	89.744	35.897	4.21053	4.84211
22 1.75055	3.28228	n	y	250	59	89.474	52.632	3.50109	5.03282
23 2.73684	3.15789	n	y	125	60	94.737	23.684	4.42105	4.84211
24 3.51967	3.72671	y	y	250	60	100.000	58.333	5.59006	5.79710
25 5.26316	1.68421	n	y	150	69	47.368	94.737	5.26316	1.68421
26 4.21053	2.31579	n	n	300	69	44.737	100.000	4.21053	2.31579
27 2.27790	1.59453	n	n	200	68	89.474	34.211	2.27790	1.59453
28 1.09409	0.65646	n	n	150	68	78.571	82.143	1.09409	0.65646


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S
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Q
U
E
O N C F I 0 0 R C H O F S P H T S C H I T O A A R A S M E A A S M E D
B C F I 0 0 E E E P I U R A S M E A A R R C E B E
S E L D W L N D D L N T A . . . . . O.00000
42 C F 100606 4 1 3498 191 63.7 3 128 204 . . . . . O.42105
43 D 1 102002 4 2 3506 109 54.5 2 115 190 . . . . .
V V D S M E A R B C . . . . . O.21053 0.63158
I I I S S A T D A R B C . . . . . 1.05263 1.05263
S B N V D I R A B C . . . . .
D E 0 I R I I F F . . . . .
S A D R L D F . . . . .
42 O.21053 0.63158 n n 150 76
43 O.63158 0.63158 n n 175 75

```

Void Area vs Exit Temperature
X50 Hole Data



General Linear Models Procedure

Dependent Variable: VOID

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	1	34.24649687	34.24649687	20.22	0.0001
Error	37	62.67199633	1.69383774		
Corrected Total	38	96.91849320			

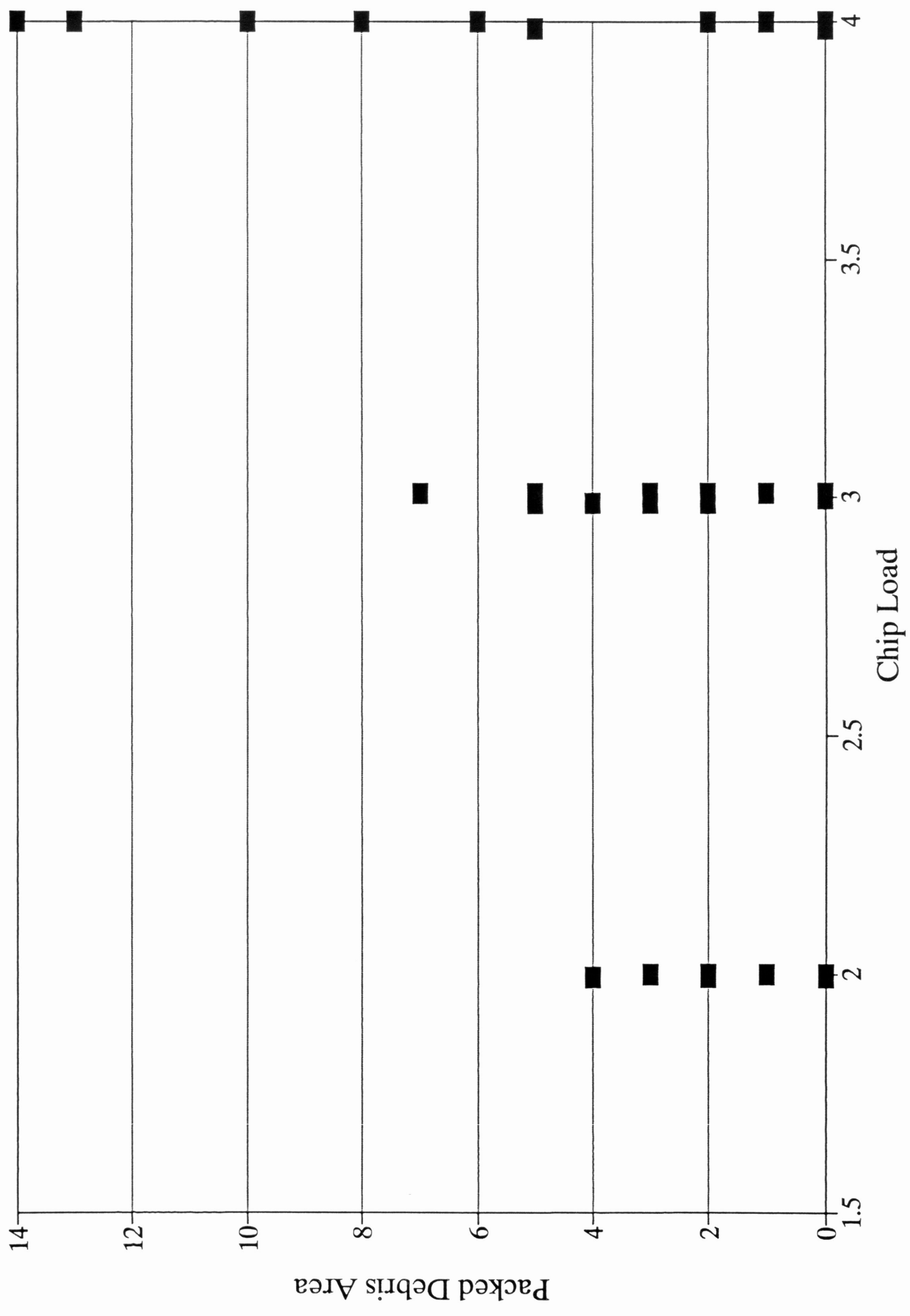
R-Square	C.V.	Root MSE	VOID Mean
0.353354	51.28482	1.301475	2.53773984

Source	DF	Type I SS	Mean Square	F Value	Pr > F
TOUT	1	34.24649687	34.24649687	20.22	0.0001
Source	DF	Type III SS	Mean Square	F Value	Pr > F
TOUT	1	34.24649687	34.24649687	20.22	0.0001

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	13.10317775	5.55	0.0001	2.35893956
TOUT	-0.05804368	-4.50	0.0001	0.01290871

Packed Debris vs Chip Load

X50 Hole Data



General Linear Models Procedure

Dependent Variable: DEBP

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	3	8.55973184	2.85324395	7.60	0.0004
Error	39	14.64641761	0.37554917		
Corrected Total	42	23.20614945			

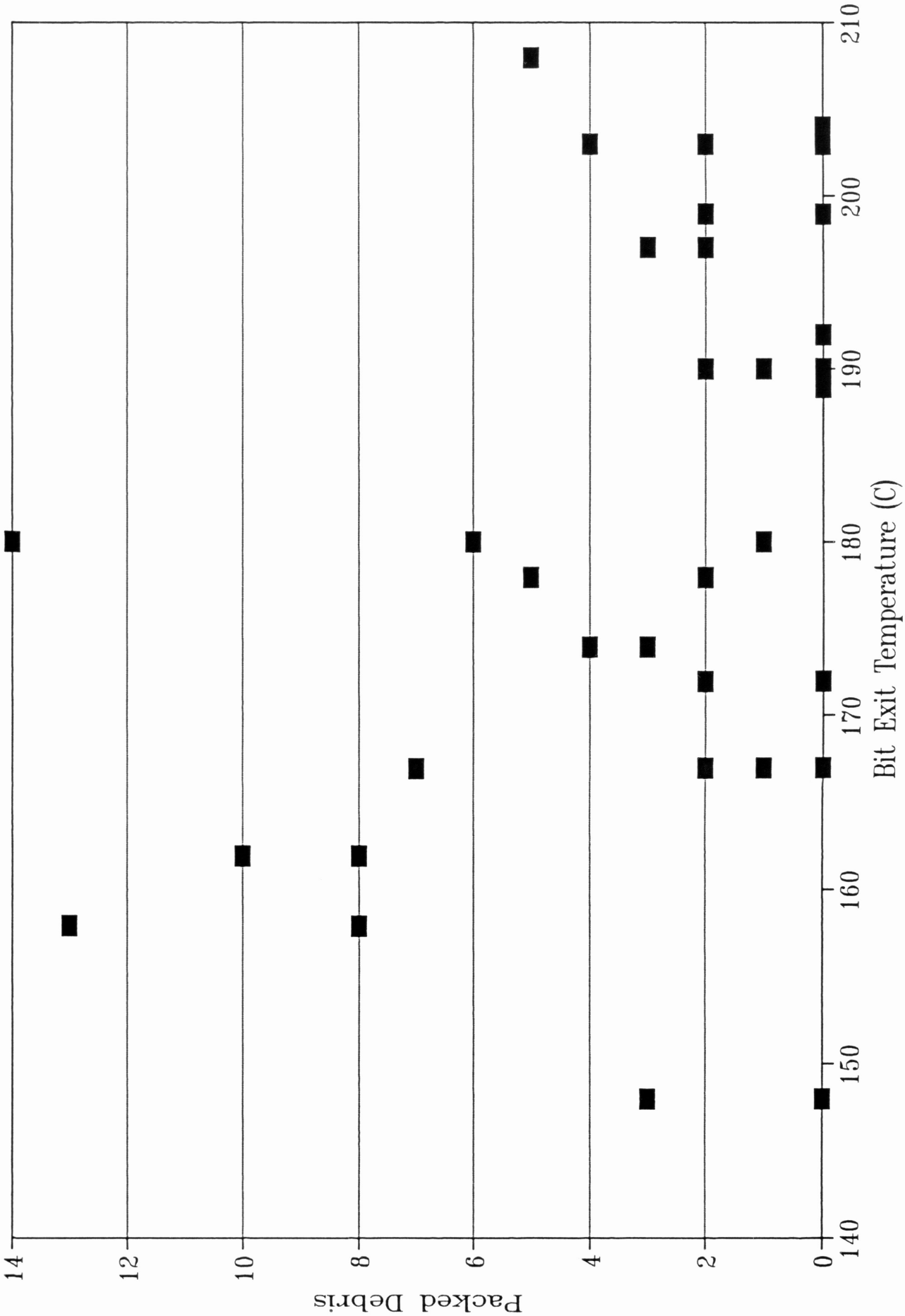
R-Square 0.368856
 C.V. 104.8903
 Root MSE 0.612821
 DEBP Mean 0.58424920

Source	DF	Type I SS	Mean Square	F Value	Pr > F
HOLEN	1	4.00289766	4.00289766	10.66	0.0023
CHIPL	1	3.95459714	3.95459714	10.53	0.0024
SPEED	1	0.60223704	0.60223704	1.60	0.2129

Source	DF	Type III SS	Mean Square	F Value	Pr > F
HOLEN	1	0.77857563	0.77857563	2.07	0.1579
CHIPL	1	4.06839956	4.06839956	10.83	0.0021
SPEED	1	0.60223704	0.60223704	1.60	0.2129

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	0.6591733675	0.73	0.4716	0.90671320
HOLEN	-0.0001100655	-1.44	0.1579	0.00007644
CHIPL	0.4307087355	3.29	0.0021	0.13085951
SPEED	-0.0203017992	-1.27	0.2129	0.01603187

Packed Debris vs Exit Temperature
X50 Hole Data



General Linear Models Procedure

Dependent Variable: DEBP

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	1	3.56409516	3.56409516	7.03	0.0117
Error	37	18.76015112	0.50703111		
Corrected Total	38	22.32424628			

R-Square 0.159651
 C.V. 114.3727
 Root MSE 0.712061
 DEBP Mean 0.62257975

Source	DF	Type I SS	Mean Square	F Value	Pr > F
TOUT	1	3.56409516	3.56409516	7.03	0.0117
Source	DF	Type III SS	Mean Square	F Value	Pr > F
TOUT	1	3.56409516	3.56409516	7.03	0.0117

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	4.031007332	3.12	0.0035	1.29061948
TOUT	-0.018724986	-2.65	0.0117	0.00706259

General Linear Models Procedure

Dependent Variable: SMEARC

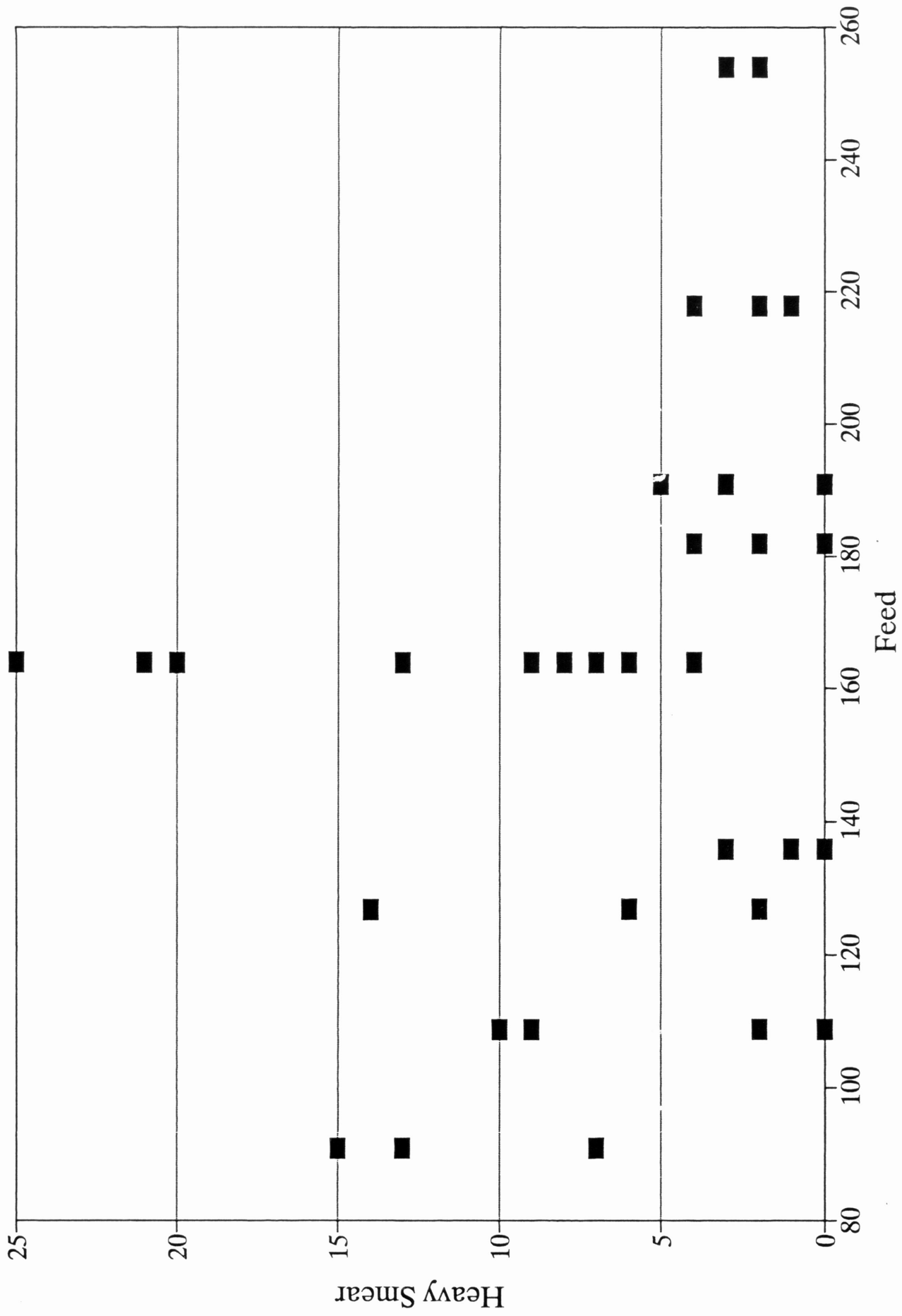
Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	2	1358.042449	679.021224	2.74	0.0776
Error	37	9162.999876	247.648645		
Corrected Total	39	10521.042324			

R-Square	C.V.	Root MSE	SMEARC Mean
0.129079	93.08184	15.73686	16.9064731

Source	DF	Type I SS	Mean Square	F Value	Pr > F
CHIPL	1	1267.700037	1267.700037	5.12	0.0296
SPEED	1	90.342412	90.342412	0.36	0.5495
Source	DF	Type III SS	Mean Square	F Value	Pr > F
CHIPL	1	1321.432417	1321.432417	5.34	0.0266
SPEED	1	90.342412	90.342412	0.36	0.5495

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	51.98364856	2.19	0.0349	23.73443998
CHIPL	-7.61897139	-2.31	0.0266	3.29831282
SPEED	-0.23038306	-0.60	0.5495	0.38143688

Heavy Smear vs Feed X50 Hole Data



General Linear Models Procedure

Dependent Variable: SMEARC

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	3	1250.390050	416.796683	1.62	0.2021
Error	36	9270.652274	257.518119		
Corrected Total	39	10521.042324			

R-Square	C.V.	Root MSE	SMEARC Mean
0.118847	94.91850	16.04737	16.9064731

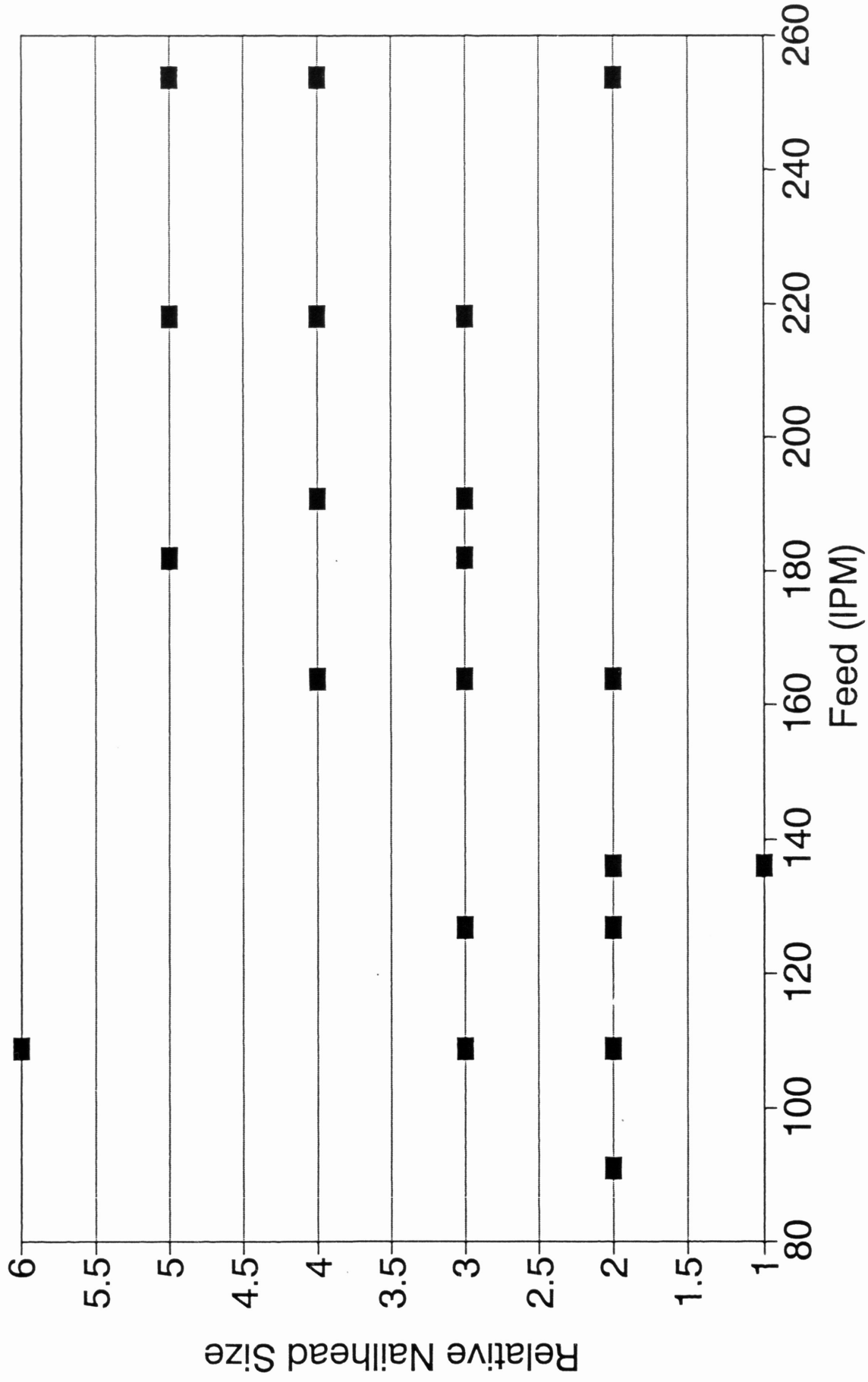
Source	DF	Type I SS	Mean Square	F Value	Pr > F
HOLEN	1	33.286083	33.286083	0.13	0.7213
FEED	1	1110.361392	1110.361392	4.31	0.0450
SPEED	1	106.742575	106.742575	0.41	0.5238

Source	DF	Type III SS	Mean Square	F Value	Pr > F
HOLEN	1	124.678761	124.678761	0.48	0.4910
FEED	1	1201.670070	1201.670070	4.67	0.0375
SPEED	1	106.742575	106.742575	0.41	0.5238

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	25.81745367	1.19	0.2436	21.77988229
HOLEN	-0.00142503	-0.70	0.4910	0.00204801
FEED	-0.13780820	-2.16	0.0375	0.06379495
SPEED	0.30246185	0.64	0.5238	0.46979205

Nail Heading vs Feed

X750 Hole Data



General Linear Models Procedure

Dependent Variable: NAIL

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	2	3.16521968	1.58260984	1.05	0.3663
Error	23	34.68093417	1.50786670		
Corrected Total	25	37.84615385			

R-Square	C.V.	Root MSE	NAIL Mean
0.083634	39.90845	1.227952	3.07692308

Source	DF	Type I SS	Mean Square	F Value	Pr > F
FEED	1	3.11147297	3.11147297	2.06	0.1643
SPEED	1	0.05374671	0.05374671	0.04	0.8519
Source	DF	Type III SS	Mean Square	F Value	Pr > F
FEED	1	2.24986161	2.24986161	1.49	0.2343
SPEED	1	0.05374671	0.05374671	0.04	0.8519

Parameter	Estimate	T for H0: Parameter=0	Pr > T	Std Error of Estimate
INTERCEPT	1.609190737	0.85	0.4027	1.88766989
FEED	0.006344444	1.22	0.2343	0.00519394
SPEED	0.007060116	0.19	0.8519	0.03739533