A DELAY-EFFICIENT RADIATION-HARD DIGITAL DESIGN APPROACH USING CODE WORD STATE PRESERVING (CWSP) ELEMENTS

A Thesis

by

CHARU NAGPAL

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2008

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Sunil Khatri
Committee Members,	Jiang Hu
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	Kevin Nowka
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ABSTRACT

A Delay-efficient Radiation-hard Digital Design Approach
Using Code Word State Preserving (CWSP) Elements. (May 2008)
Charu Nagpal, B.E., University of Delhi
Chair of Advisory Committee: Dr. Sunil Khatri

With the relentless shrinking of the minimum feature size of VLSI Integrated Circuits (ICs), reduction in operating voltages and increase in operating frequencies, VLSI circuits are becoming more vulnerable to radiation strikes. As a result, this problem is now important not only for space and military electronics but also for consumer ICs. Thus, the design of radiation-hardened circuits has received significant attention in recent times.

This thesis addresses the radiation hardening issue for VLSI ICs. In particular, circuit techniques are presented to protect against Single Event Transients (SETs). Radiation hardening has long been an area of research for memories for space and military ICs. In a memory, the stored state can flip as a result of a radiation strike. Such bit reversals in case of memories are known as Single Event Upsets (SEUs). With the feature sizes of VLSI ICs becoming smaller, radiation-induced glitches have become a source of concern in combinational circuits also. In combinational circuits, if a glitch due to a radiation event occurs at the time the circuit outputs are being sampled, it could lead to the propagation of a faulty value. The current or voltage glitches on the nodes of a combinational circuit are known as SETs. When an SET occurring on a node of a logic network is propagated through the gates of the network and is captured by a latch as a logic error, it is transformed to an SEU.

The approach presented in this thesis makes use of Code Word State Preserving

(CWSP) elements at each flip-flop of the design, along with additional logic to trigger a recomputation in case a SET induced error is detected. The combinational part of the design is left unaltered. The CWSP element provides 100% SET protection for glitch widths up to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$, where D_{min} and D_{max} are the minimum and maximum circuit delay respectively. Δ_1 and Δ_2 are extra delays associated with the proposed SET protection circuit. The CWSP circuit has two inputs - the flip flop output signal and the same signal delayed by a quantity δ. In case an SET error is detected at the end of a clock period i, then the computation is repeated in clock period $i+1$, using the correct output value, which was captured by the CWSP element in the i^{th} clock period. Unlike previous approaches, the CWSP element is i) in a secondary computational path and ii) the CWSP logic is designed to minimally impact the critical delay path of the design. It was found through SPICE simulations that the delay penalty of the proposed approach (averaged over several designs) is less than 1%. Thus, the proposed technique is applicable for high-speed designs, where the additional delay associated with the SET protection must be kept at a minimum.

To my family

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First and foremost, I would like to thank my advisor Dr. Sunil Khatri. I am grateful to him for his academic guidance, continued support and being a source of inspiration all along. His perpetual energy and enthusiasm in research is contagious and keeps everyone in the group motivated. The amount of time Prof. Khatri gives to each of his students is commendable.

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CHAPTER I

INTRODUCTION

I-A. Need of radiation-hardened design

In recent times, there has been an increased interest in the radiation immunity of electronic circuits [1] - [13]. This has been an area of significant interest and research for space or military electronics [11, 12, 14, 15] for many years, due to the significantly larger rate of radiation strikes in such applications. For space applications, neutrons, protons and heavy cosmic ions which are trapped in geomagnetic belts [14] produce intense showers of such radiation. When such ions strike diffusion regions in VLSI designs, they can deposit a charge, resulting in a voltage spike on the affected circuit node. If the magnitude of this spike is sufficiently large, an erroneous value may be computed by the circuit. This is particularly problematic for memories, since the stored state can flip as a result of such a radiation strike. In case of memories, these errors are referred to as Single Event Upsets (SEUs). Although SEU induced errors in sequential elements continue to be problematic, it is expected that the soft errors in combinational logic will dominate in future technologies [16, 17, 8]. In a combinational circuit, if the glitch occurs at the time the circuit outputs are being sampled, it can lead to an incorrect value being latched. Such radiation strikes in combinational logic are referred to as Single Event Transients (SETs).

With the relentless shrinking of the minimum feature size of VLSI Integrated Circuits (ICs), there is a corresponding reduction in the dimensions of the diffusion nodes of the MOSFETS. This results in a reduced diffusion capacitance, and hence, if charge is dumped on the diffusion node as a consequence of a radiation strike, a

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large voltage spike may be generated. With operating voltages getting smaller, this problem is further aggravated. As a result, modern VLSI ICs are significantly more prone to SET problems [13]. Even though it is true that the amount of radiation received on the surface of the earth is lower than that in space, the shrinking of process feature sizes makes terrestrial VLSI ICs susceptible to SET problems [13]. Hence, there has been a significant increase in interest in radiation-tolerant VLSI ICs in the recent past.

I-B. SEU/SET measurement and modeling

In the radiation community, Linear Energy Transfer (LET) is commonly used to measure the charge deposition rate. LET is defined as the amount of energy deposited in a material per unit of distance traveled, normalized to the material's density [18]. Cosmic ions have varying LETs, and they result in the deposition of a charge Q in a semiconductor diffusion region by the following formula [15].

$$Q = 0.01036 \cdot L \cdot t \tag{1.1}$$

Here L is the LET of the ion (expressed in MeV-cm^2/mg), t is the depth of the collection volume (expressed in microns), and Q is charge in pC. To derive the above formula, note that $3.6eV$ of energy is needed to create an electron-hole pair in silicon. The density of silicon is 2.42gm/cm^3. Thus, for a track length (t) of $1\mu m$, the LET (= energy in MEV/ density of the material $\times$ track length) corresponding to $3.6eV$ of energy is equal to $(3.6 \times 10^{-6})/(2.42 \times 10^3 \times 10^{-4}) = 1.49 \times 10^{-5}$MeV-cm^2/mg. Now, charge of one electron is equal to $1.60 \times 10^{-7}pC$. Thus, an LET of 1MeV-cm^2/mg will deposit approximately ($1.60 \times 10^{-7}/1.49 \times 10^{-5}=$) 0.01pC of charge along a track of $1\mu m$ [19], which is in agreement with the relationship between

Q, L and t given in Equation 1.1. For terrestrial electronics, the LET for ionized particles in silicon is typically below 15MeV [1]. Also, the charge collection depth for 180nm and higher bulk silicon process technologies is relatively constant and equal to $2\mu m$ [1, 19]. Thus, from Equation 1.1, the maximum charge deposited for 180nm technology is 0.3pC. For uniform technology scaling, the doping density increase by $\sqrt{2}$ in successive process technologies [20]. In [21], it was empirically found that the charge deposited in a bulk silicon device is inversely related to the doping density. Thus, the maximum charge deposited for 130nm, 100nm and 70nm processes would be 0.21pC, 0.15pC and 0.11pC respectively [1].

The amount of charge that is required to cause a bit to be sampled incorrectly is referred to as the critical charge, Q_C [22]. With diminishing process feature sizes, reduced supply voltages and higher operating frequencies, SET problems are a concern even for terrestrial electronics today, particularly for mission critical applications. Atmospheric neutrons as well as alpha particles which are created by unstable isotopes in the IC packaging materials can also cause SET problems.

The current pulse that results from a particle strike is traditionally expressed as a double exponential function [23, 24]. The expression for this pulse is

$$I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{1.2}$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the charge collection time constant for the junction and τ_β is the ion track establishment constant. The τ_β value is in the range of 10-50ps, while τ_α is of the order of 200ps [1, 17]. For $\tau_\alpha = 200ps$, $\tau_\beta = 50ps$ and Q as given above, it was verified that a minimum sized inverter (in the 130nm, 100nm and 90nm technologies) resulted in a glitch large enough to cause incorrect computation.

I-C. Introduction to the approach used in this thesis

The approach of this thesis uses the Code Word State Preserving (CWSP) circuit of [3] to achieve SET tolerance. The work of [3] will be described in detail in Chapter II. In this thesis, the normal circuit computation path is referred to as the *functional* path, while the alternative path used to detect and correct SET errors is called the *secondary* circuit path. The detection of a faulty computation (due to an SET event) is done on the secondary path by a watchdog circuit, which uses CWSP elements. In case of an SET event, the correct value (which is computed by the CWSP element) is used to repeat the computation, after appropriately introducing a bubble in the computation pipeline. The main advantages of this approach are:

- This approach achieves SET tolerance for glitches of duration up to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$, where D_{min}, D_{max} are the minimum and maximum delays of the design and Δ_1, Δ_2 are additional delay in the secondary circuit path. Since the CWSP elements are connected on a secondary path as opposed to the functional computation path of the circuit, there is a minimal (less than 1% on average) speed penalty. This is achieved since the secondary circuit path containing the watchdog circuit is connected to the inputs and outputs of the functional circuit in a manner that additional parasitic capacitances are minimized.

- The results with this approach are better than another approach which uses CWSP elements [3], which has a delay overhead of 28.65%, (compared to about 1% for the proposed scheme). Also, [3] handles smaller glitches (0.45ns) compared to the approach of this thesis (which handles glitches of width 0.5ns and 0.6ns for Q=100fC and 150fC [1] respectively). Contrasted with an approach that employs gate resizing [1], the average circuit areas with the proposed ap-

proach are comparable, while the delay penalties (0.54%) are much smaller than those of [1] (which has a delay penalty of about 2.8%).

- The proposed approach achieves 100% SET protection (for a glitch of Q up to 150ps with $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$) which is not the case for [1], which guarantees 90% circuit protection for the same values of Q, τ_α and τ_β.

I-D. Thesis outline

The remainder of this thesis is organized as follows. Chapter II discusses some previous work in this area. A classification of various techniques available for radiation hardening is given. The work of [2, 3] is explained in detail. The CWSP element approach of [2, 3] is exploited and augmented in the work presented in this thesis.

Chapter III explains the approach of this thesis in detail. In Chapter III, the system level design is first explained, then the circuit level details are provided. An analysis of the radiation tolerance of the proposed approach follows. Also, the derivation of the maximum tolerable glitch width is presented in this chapter.

In Chapter IV, experimental results are provided. Finally, this thesis is concluded in Chapter V.

CHAPTER II

PREVIOUS WORK

There has been a great deal of work on radiation-tolerant circuit design. In this chapter, the work done in this field is broadly classified into two categories. In section II-A, the approaches which provide an analysis of soft errors and their effects are presented. In section II-B, design approaches for radiation hardening are presented. In subsections II-B.1 and II-B.2, the design approaches of [1] and [2, 3] respectively are explained in greater detail as the results in this thesis are compared with these contemporary approaches. The motivation for using these approaches for comparison was that amongst the SET-tolerant design approaches reviewed, [1] and [2, 3] had the best results in terms of delay and area respectively.

II-A. SEU/SET analysis approaches

One area of study in the field of radiation-hardened circuit design employs device physics to model radiation strikes accurately. This involves analyzing the SET and SEU faults using circuit layout information and 3D modeling of the MOSFET devices [25, 26]. These simulators allow a precise characterization of SETs, but they are computationally intensive. To reduce the computational cost, circuit level techniques for SET characterization are commonly used. The circuit level techniques model SETs with a transient current source. The double exponential function which is typically used to model this transient current source was provided in Equation 1.2 [23]. The approaches of [27, 28, 24] involve mathematically solving the non-linear equations to derive an analytical model for radiation-induced transients. These techniques aim at finding a fast and accurate analytical model to determine the impact of a radiation strike. This information may be used by the designer to test the resilience of the

design and achieve the level of protection required.

Historically, the study of soft errors was mostly limited to space and military electronics, due to the significantly large rate of radiation strikes in these applications. Several papers report the experimental studies on SEU in space electronics for SRAMs [15, 22], DRAMs [29], SRAM based Virtex FPGAs [7, 10, 11], flash memory based FPGAs [12], etc. Even though it is true that the amount of radiation received on the surface of the earth is lower than in space, the shrinking of process feature sizes makes contemporary terrestrial VLSI ICs susceptible to SET problems [30] as well.

Earlier, SEUs were considered problematic mainly for memories [13, 31], because SEU events can flip the stored state of a memory element. Also, the probability of a radiation strike is higher in memories as they have the largest number and density of bits [32]. In [13], the authors provide a built-in current sensor (BICS) to detect SEU events in an SRAM. The work of [31] studies the SEUs in DRAMs due to the alpha particles generated by the packaging material of semiconductor devices [33]. Although SEU induced errors in sequential elements continue to be problematic, it is expected that the soft errors in combinational logic will dominate in future technologies [16, 17, 8].

A particle strike resulting in a bit-flip on some node in a circuit may be inconsequential because of logical [34], electrical [35] and temporal masking [36]. Logical masking occurs when the effect of a glitch is not propagated to the circuit outputs. For example, if one input of an AND gate is always zero, then a glitch on the second input of the AND gate is inconsequential. Electrical masking is the attenuation of a radiation induced glitch as it propagates through a series of digital gates along a circuit path. Temporal masking occurs when an SET in combinational logic occurs outside the clocking window of a latch/flip-flop and is therefore silently ignored. An

analysis of SEU error rates is presented in [34] and [35]. These approaches account for logical and electrical masking respectively. An analysis as well as a hardening approach based on temporal masking is presented in [36].

II-B. Radiation-hardened design approaches

As mentioned in section II-A, soft errors were historically considered to be of importance mostly for space and military applications [15]. Also, soft errors were considered problematic mostly for memories [32]. As a result, most of the radiation-hardened design techniques in the past were developed for space and military applications [37, 10, 11] and/or focused on radiation tolerance of memories [38]. However, with the reducing minimum feature size of VLSI Integrated Circuits (ICs), reduction in operating voltages and increase in operating frequencies, radiation-hardened circuit design has become important both for terrestrial applications [30] and combinational circuits [17, 8].

The radiation hardened design approaches can be classified as device level, circuit level and system level [1, 32]. The device level approaches involve a fundamental change or enhancement of the fabrication process to improve the radiation immunity of a design [39]. Circuit level hardening is achieved by using special circuit design techniques that reduce the vulnerability of a circuit to radiation strikes. Transistor sizing [4] is an example of this category. The concept of [4] is combined with logical masking and applied at gate level in [1], which is explained in detail in section II-B.1. The device and circuit level approaches are typically fault avoidance approaches, while system level approaches typically involve use of fault detection and tolerance mechanisms. Triple modular redundancy (TMR) [40] is a classical example of a system level design approach. However, it has an area overhead of 200%. A recent approach

uses Code Word State Preserving (CWSP) elements [2, 3] to achieve the protection realized by TMR [40] with a much lower average area overhead. This approach is explained in detail in section II-B.2.

II-B.1. Gate sizing to radiation harden combinational logic [1]

Although gate resizing [4, 1] is orthogonal to the method described in this thesis, the results obtained for the proposed method are compared with [1] as well. It is important to understand how radiation hardening can be obtained with gate sizing. When a cosmic ray passes through the drain of a transistor, a short is momentarily created between the drain and the substrate [18]. This results in a current spike for a short duration of time (which is modeled by Equation 1.2 described earlier). The charge deposited depends on the track length (Equation 1.1) which is independent of the device size. Thus, the maximum amount of charge deposited for a given technology will be the same regardless of the size of the device. Now, an upsized gate has a higher drive strength and it will discharge the charge deposited due to the radiation event faster, resulting in a smaller glitch. Thus, radiation hardening can be achieved by sizing up the gates sufficiently so that they can tolerate the worst case charge (Q) for a particular technology. However, protecting all the gates in this manner can lead to an extremely high area overhead. For instance, for a 70nm technology, an inverter driving another inverter of the same drive strength needs to be sized up to 7X (11X) to tolerate Q, τ_α and τ_β values of 100fC (150fC), 200ps and 50ps respectively. These values of Q, τ_α and τ_β are appropriate for 70nm and are used by [1]. The selective sizing approach of [1] limits the area overhead to 42.95%, but guarantees only 90% protection. Note that the probability of an SEU strike is lower for a smaller device because the area exposed is less. However, if there is an SEU event on a smaller device, it results in a glitch of greater magnitude. Thus, a

minimum sized inverter is used for any worst case simulations.

The approach of [1] limits the area overhead to 42.95% by using selective sizing based on logical masking. In [1], the probability of logical masking ($P_{logicalmasking}$) at a gate is computed as

$$P_{logicalmasking} = 1 - P_{sensitization}$$

where $P_{sensitization}$ is the probability of sensitization i.e. the probability that there exists a functionally sensitized path from the gate to the primary output(s) or memory element(s). $P_{sensitization}$ is obtained by applying random input patterns and using fault simulation to check which gates can be sensitized. The next step is to process the gates in the decreasing order of $P_{sensitization}$ (increasing order of logical masking) until the coverage objective is met. The processing step involves upsizing the gate for SET resilience and the coverage is calculated as the sum of $P_{sensitization}$ of the hardened gates divided by the sum of $P_{sensitization}$ of all the gates in the circuit. Once the coverage reaches the objective (of 90% in [1]), the remaining gates are not hardened.

II-B.2. The CWSP-based approach [2, 3]

In this section, the approach of [2, 3] is explained in detail.

Figure II.1 illustrates how CWSP elements are utilized in a circuit, using the approach of [2]. For the moment, assume that the CWSP element tolerates SET glitches of width up to δ, on any internal circuit node.

Consider a gate G which drives the flip-flop in the original design, as shown in Figure II.1 (a). In the CWSP-based SET-resilient design approach of [2], each gate whose output is connected to a flip-flop input is replaced by a corresponding CWSP element, as shown in Figure II.1 (b). For a k input gate, the corresponding CWSP element has $2k$ inputs. One set of k inputs are connected to the inputs of the gate

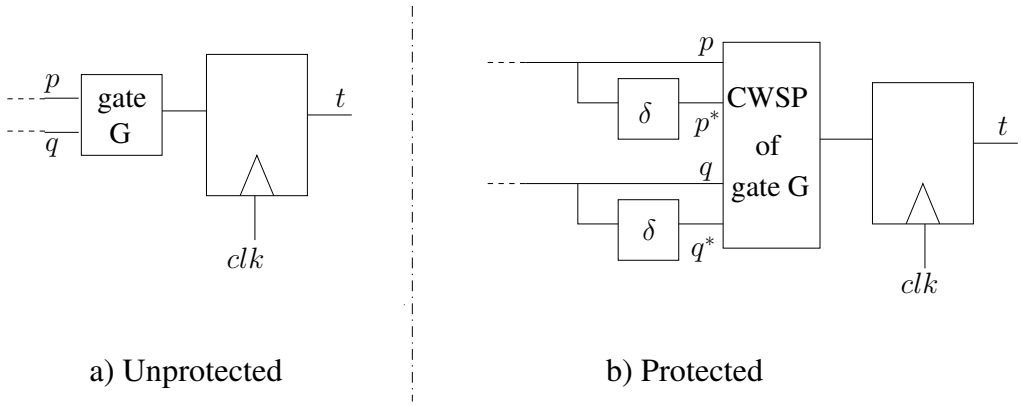


Fig. II.1. CWSP based SET tolerance of [2]

that the CWSP element replaces. The other set of k inputs are connected to the delayed version (by a delay value δ) of the first set of k inputs. This is illustrated in Figure II.1 (b). The resulting circuit of Figure II.1 (b) tolerates SET glitches of width up to δ.

How the CWSP element tolerates glitches of width up to δ is explained next. Figure II.2 illustrates the CWSP circuits for an inverter and a NAND2 gate. In Figure II.2, the inputs a and b are the un-delayed inputs, while the inputs a^* and b^* are delayed versions of a and b respectively (delayed by δ time units). Consider the CWSP element of either the INVERTER or the NAND2 gate. When the input $a = a^*$, and $b = b^*$, each CWSP element behaves normally, and the outputs are resistively driven to $\overline{a}$ and $\overline{a \cdot b}$ for the INVERTER and the NAND2 gate respectively. However, whenever there is an SET event which results in a glitch on any input, the gate stops driving the output resistively, since both the pullup and pulldown paths are disabled. At this point the output is held to its last correct value, with a high impedance.

The problem with this approach is that the CWSP element which replaces a k-

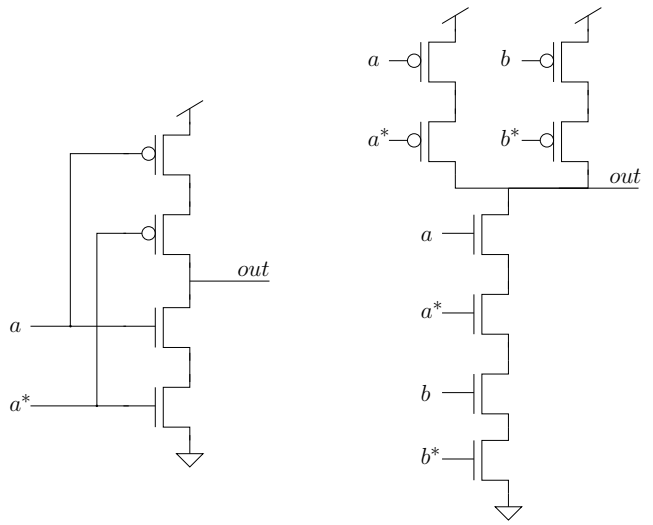


Fig. II.2. CWSP elements for INVERTER and NAND2 gates

input NAND or NOR gate requires $2k$ series devices, making the approach impractical for gates with more than 2 inputs. This is because in bulk CMOS technologies, it is not practical to connect more than 4-5 devices in series, due to body effect [20]. The use of CWSP elements with $k > 2$ results in the gate becoming quite slow and utilizing a large circuit area. A modification of [2] which takes care of these issues is shown in Figure II.3 [3]. The new approach uses only one type of CWSP element. In particular, this is the CWSP element of an inverter. The additional inversion that is thus introduced in Figure II.3 (b) is absorbed into the combinational circuit functionality to yield a logically identical design as Figure II.3 (a).

In Figure II.3, one of the inputs to the CWSP element is driven directly from the combinational circuit, while the other input is the same output, delayed by δ. The combinational circuit is implemented to generate the complement of the required

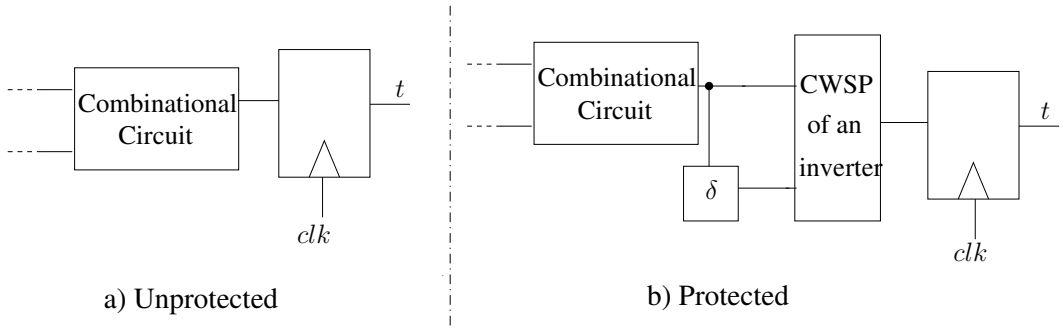


Fig. II.3. Improvement over the CWSP-based approach of [2] by [3]

output, and the CWSP element provides another inversion. Since the CWSP element used in Figure II.3 has at most 2 series devices, the delay and area overhead is kept at a minimum. This approach also averts the need to have a unique CWSP element for each library gate in the circuit, reducing the design time and cost (in terms of area, delay and power). However, in both [3, 2], the delay of the circuit is increased significantly since CWSP elements are introduced before every flip-flop in the design. In particular, if an SET event results in a glitch of width δ at the un-delayed input to the CWSP element, it will attain its correct value after time δ. The delayed input attains its correct value after another delay of δ. Thus, the output of the CWSP element is guaranteed to be correct after a delay of 2δ. This causes a delay penalty of 2δ in the functional circuit delay. In [3], an additional delay is introduced by the CWSP element (D_{CWSP}) being added to the circuit path. The delay overhead is therefore given by:

$$Delay = 2\delta + D_{CWSP}$$

The above equation shows that the delay penalty of the approach is larger than

twice the SET tolerance achieved, which can be quite large.

The work of this thesis avoids this delay penalty by connecting the CWSP element off the delay-critical primary circuit path. Also, the work of [3] does not take into account a possible SET strike at the output of the CWSP element, which is handled in the approach presented in this thesis, as described in the Chapter III.

CHAPTER III

APPROACH

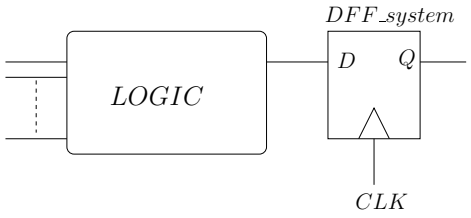
The approach presented in this thesis uses CWSP elements [3] to achieve 100% SET tolerance to glitches induces by radiation transients with a specified value of Q, τ_α and τ_β. In case of an SET event, the correct value is always computed by the CWSP element (which is connected in a secondary path, off the functional circuit critical path). This correct value is used to repeat the computation in case of an SET event, by introducing a pipeline bubble in the computation. SET tolerance is achieved for glitches of duration up to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$. Also, there is no added design cost associated with altering the combinational portion of the original design. The CWSP element is connected to the flip-flop inputs and outputs, in a manner that the additional parasitic capacitances on the functional circuit path are minimized.

This chapter is divided into three sections. Section III-A describes the proposed approach at an architectural or system level. In section III-B, the proposed approach is explained at the circuit level, along with a discussion of the radiation tolerance of each of the components of the proposed approach. An analysis of the maximum tolerable glitch width is presented in section III-C.

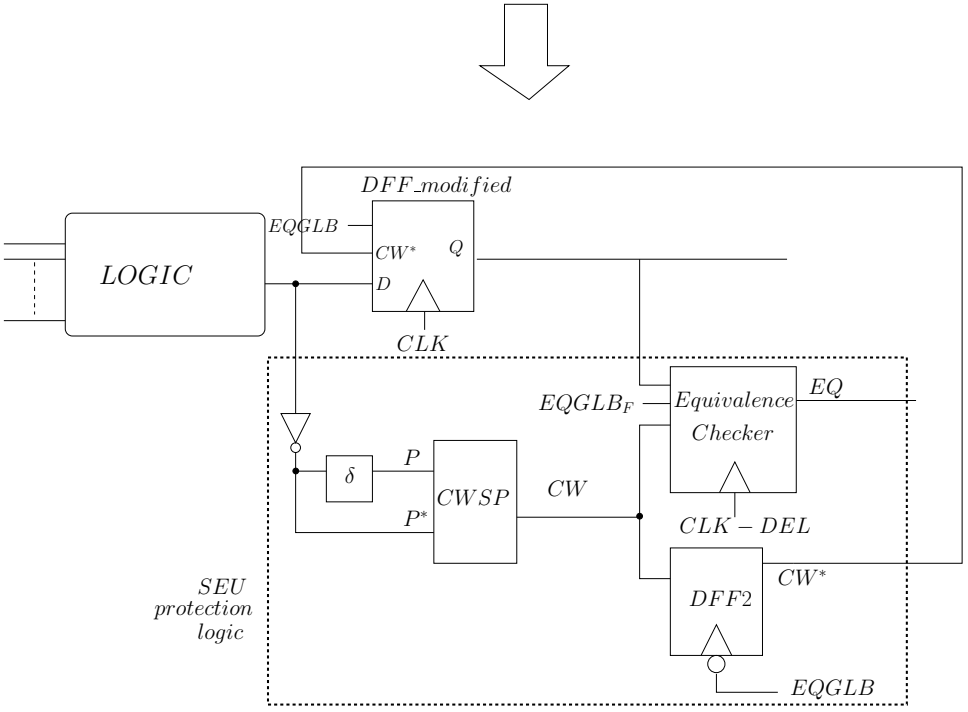
III-A. System level design

Consider a fragment of the original design, shown in Figure III.1 (a). This consists of a combinational output which is connected to a flip-flop labeled *DFF_system*. This flip-flop is in the functional circuit path of the design.

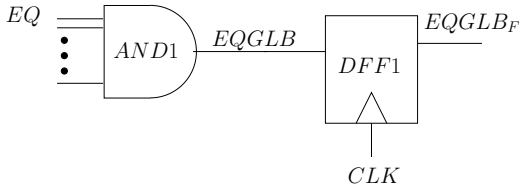
The CWSP based modification as per the proposed scheme is shown in Figure III.1 (b). The original combinational logic is left intact, except that the flip-flop



a) Original Circuit



b) Modified Circuit



c) $EQGLB_F$ Circuit

Fig. III.1. Architectural view of the proposed SET tolerant design

is redesigned (this design is discussed later). In addition, the values of the D and Q signals of the flip-flop are read by the SET protection logic shown in Figure III.1 (b). This logic is on a secondary path, and hence the functional delay is impacted only minimally. The D input of the flip-flop is connected to a minimum-sized inverter, whose output is fed directly to a CWSP element. Note that the functional D flip-flop is slightly modified, and labeled as *DFF_modified*. The other input of the CWSP element is the delayed version of the inverter output (delayed by δ). The output of the CWSP element (called CW) is compared with the Q output of the system flip-flop using a rising-edge triggered equivalence checking circuit, with an output EQ. As explained earlier, the output of the CWSP element is guaranteed to be correct after a delay equal to the sum of 2δ and the delay of the CWSP element. Thus, the equivalence check is triggered after the rising edge of CLK, delayed by the sum of 2δ and the delay of the CWSP element. This delayed clock signal is referred to as CLK_DEL. Under normal operation, EQ is high, since Q is equal to CW. When there is an SET event, these values can be different causing EQ to fall. In this case, the current computation is redone using the output of the CWSP element (which is guaranteed to be correct) as the input to *DFF_modified* in the next clock cycle.

Note that if an SET event is detected at any flip-flop in a design, the computation needs to be redone for all the flip-flops in the design. Consider a design that has n flip-flops. If the EQ signal of any of these flip flops becomes low, the computation needs to be redone for all the flip-flops. A logical AND of all the EQ signals is therefore computed to obtain a global EQ signal (called $EQGLB$). If the signal $EQGLB$ falls, the value of CW (for each of the n flip-flops) is latched into a flip-flop *DFF2*, whose output is CW^*. This value is guaranteed to be error-free[1], and is now

[1] if there is an error on CW^*, this error is silently ignored by the circuit.

used in the next cycle as the input to *DFF_modified*, so that the current computation is redone in the next cycle.

The purpose of the flip-flop used to latch the value of $EQGLB$ to produce the signal $EQGLB_F$ is explained next. Suppose there is an SET event in the clock cycle i which causes the output Q_i of the *DFF_modified* to be different from the input D_i. This will cause EQ, and thereby $EQGLB$ to fall. In the next $(i+1)^{th}$ clock cycle, CW^* (which is equal to D_i) will be latched by the system flip-flop *DFF_modified*. However, CW is computed using D_{i+1}, which can be different from D_i. In the absence of the flip-flop which generates $EQGLB_F$, EQ (and $EQGLB$) will remain low in the cycle $i+1$, again triggering a recomputation in the next cycle. This recomputation could go on indefinitely. The likelihood of two strikes on the proposed SET tolerant design in two consecutive clock cycles is extremely low[2]. Hence, if there was an SET event in clock cycle i which resulted in EQ to be low, it can be safely assumed that there will be no SET event in clock cycle $i+1$ that will make EQ low. As a result, the EQ and $EQGLB$ signals can be ignored in the $(i+1)^{th}$ cycle. This can be done by making EQ and $EQGLB$ high in the next clock cycle. To achieve this, the value of $EQGLB$ is latched to $EQGLB_F$ at the positive edge of CLK. Following an SET error in cycle i, a low value on $EQGLB$ leads to CW^* being used as the input to *DFF_modified* for cycle $i+1$. In the *Equivalence Checker* (Figure III.3), in cycle $i+1$, $EQGLB_F$ being low will make EQ high and no recomputation will be triggered in cycle $i+2$. At the architectural level, the decision to reapply the primary inputs (and trigger a recomputation) is made if the value of $EQGLB$ is low at the rising edge of

As per [41, 42], the maximum solar proton fluence for particles of energy > 1MeV based on the JPL- 1991 model is $2.91 \times 10^{11}/cm^2/year$ with 99% confidence. The maximum area and time period for the testcases run was seen to be $473.4 \times 10^{-8} cm^2$ and $5.5ns$ respectively. Using these values, it can be shown that the maximum number of particle strikes in the testcases run in two consecutive cycles is 4.78×10^{-10}.

CLK. This ensures proper handling of glitches.

In Figure III.2, the working of the proposed radiation-hardening approach is illustrated with the help of timing waveforms. The solid lines correspond to the circuit operation in fault-free (no SET) state. The broken lines correspond to the case when there is a negative glitch on the D-input of the modified system flip-flop *DFF_modified*. The waveforms at all the nodes in the circuit are first explained for the fault-free case. At time t_1, which is just before the positive edge of CLK, there is a low to high transition on D. This causes the Q output of *DFF_modified* to become high for the clock cycle i. P^*, which is the inverted copy of D, falls at time t_1. P is the delayed version of P^*, so it falls after an additional delay of δ after P (at time t_2 in Figure III.2). At time t_2, P and P^* are both low, so CW becomes high. Now, since there was no radiation strike, Q and CW are identical, and so EQ will remain high. Note that EQ is registered by CLK_DEL (the delay for CLK_DEL is derived in section III-C). Since EQ is high, $EQGLB$ remains high. Since CW^* is registered at the falling edge of $EQGLB$, it will be in an unknown state since $EQGLB$ remains high. In the next clock cycle, since $EQGLB$ is high, the normal operation continues. D will be used as the input to *DFF_modified* D becomes low before the next positive edge of CLK causing Q to fall and all other signals in our circuit are updated in a similar manner.

Now, consider the case when there is a negative glitch on D at time t_1. D becomes high at time $t_2 = t_1 + \delta$ as indicated by the broken line. An incorrect value gets registered in the flip-flop *DFF_modified*, making Q low. In comparison to the case when there was no radiation strike, the D signal is delayed by δ, hence P^*, P and thus CW are also delayed by δ. Now, Q (low) being different from CW (high) makes EQ low. $EQGLB$ falls once EQ becomes low. A falling transition on $EQGLB$ registers the value of CW to CW^*. In the next clock cycle, a low value on $EQGLB$

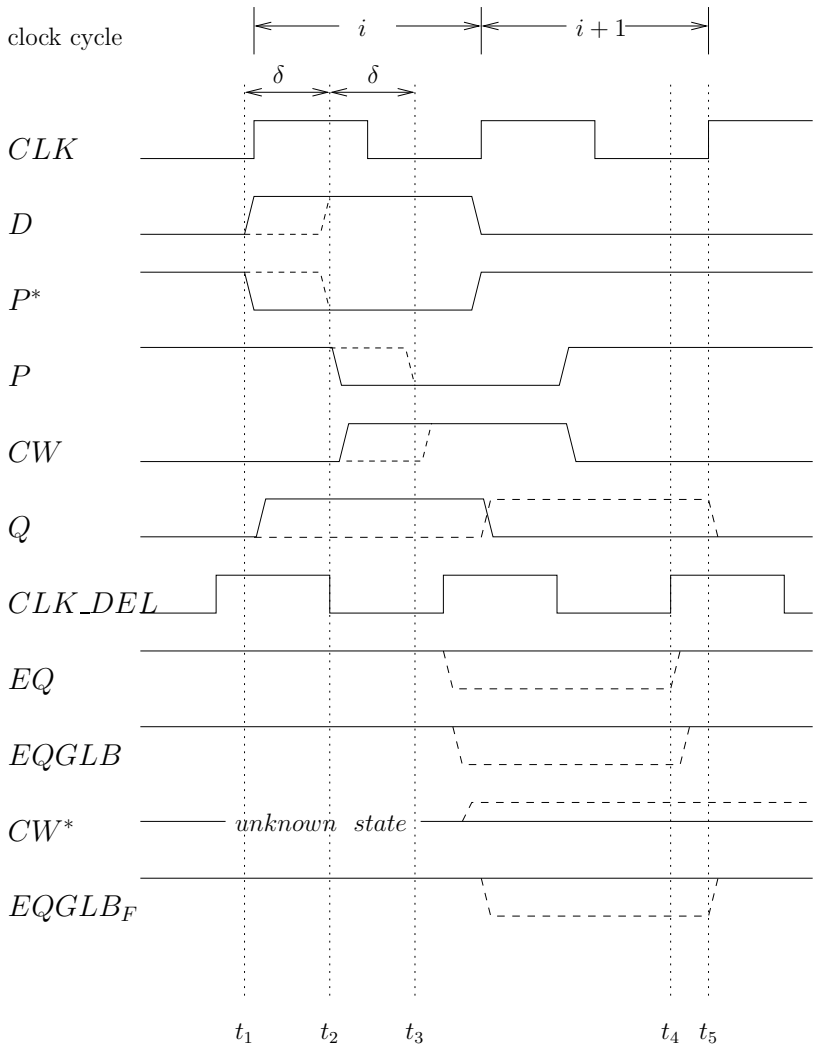


Fig. III.2. Timings signals for the proposed SET tolerant design

causes CW^* to be used as the system input. Thus, Q registers the value of CW^* and becomes high, even though the input D is low (this is the desired functionality as a recomputation is done in the clock cycle $i+1$, and hence the value of D from clock cycle i is used as the input). The entire pipeline is delayed by one clock cycle. Now, in clock cycle $i+1$, note that $CWSP$ uses the value of D in clock cycle $i+1$ which may be different from CW^* (as indicated in Figure III.2). Thus, CW become low, while Q is high. This could have incorrectly made EQ low, signaling an SET-error in clock cycle $i+1$, in the absence of the $EQGLB_F$ signal explained above. So, the data on the D input for cycle $i+1$ will get reapplied in cycle $i+2$. In the proposed design, a low value on $EQGLB$ caused $EQGLB_F$ to fall in the clock cycle $i+1$. Now, a low value on $EQGLB_F$ pulls EQ up in the clock cycle $i+1$, thus no recomputation is triggered in cycle $i+2$, as desired.

The CWSP element is upsized to ensure that it is protected against a radiation strike on the CW node. Note that when a gate is upsized, its drive strength increases, also the capacitance at the output of the gate increases and both of these properties contribute in increasing the resilience of the gate against a radiation strike. Thus, the gate needs to be driven (not floating) to be protected against a radiation strike. So, upsizing the CWSP element protects its output against a radiation strike only when it is driven (i.e when both its inputs are identical). A timing constraint on the minimum combinational delay D_{min} of the circuit (discussed in section III-C) ensures that CW is not floating when its value is being used. Apart from radiation hardening, the upsizing of the CWSP devices also helps ensure that the capacitances at its nodes are high enough that the CWSP element is able to hold its last correct state when there is an SET event resulting in a glitch on one of its inputs. If the delay value of the delay elements shown in Figure II.1 is δ, then the circuit can be made SET tolerant by sizing the CWSP element to withstand a glitch of width δ.

Since the output of the CWSP element is floating whenever its inputs are different, it is important to analyze the impact of coupling noise on the CW node when it is floating. As explained above, the CWSP element is upsized to protect against a radiation strike on its output, and thus it has a high capacitance. In particular, for the values of Q, τ_β and τ_α used in our experiments, the CWSP element was upsized to $6\times$ (to $8\times$). This results in a high capacitance of 3.63fF at the output of the CWSP element. Also, to ensure that the coupling capacitance of the CW wire (to any of its neighboring wires) is low, the length of the wire connecting the CWSP element to its fanouts is kept low. Assume that Metal 1 wire of $1\mu m$ length is used to connect the output of the CWSP element to its fanouts. This results in a coupling capacitance of 0.05fF [43]. It was experimentally verified, via SPICE simulations that a transition on neighboring wires did not result in any glitch even when CW is floating.

This approach corrects 100% of the SET events. To validate this claim, several cases were considered. Each of these were analyzed and simulated to confirm that this approach indeed provides 100% SET tolerance. Note that it is reasonable to assume that there will not be more than one SET event occurring simultaneously. Thus, all the nodes in the proposed protection scheme are analyzed independent of the others.

- Suppose there is an SET event which results in a glitch on the inputs of the CWSP circuit, the CWSP element protects against this glitch, as discussed.

- If there is a radiation strike at the output of the CWSP element, it can result in a glitch only if the CW node is floating. The D_{min} constraint explained in section III-C ensures that the glitch-free value of CW is used to compute the EQ signal. Also, the value of CW is registered to CW^* on the falling edge of the $EQGLB$ signal. Since the likelihood of more than one SET strikes in two consecutive clock cycles is extremely low, if the $EQGLB$ signal is low (because

of a radiation strike in the circuit), there cannot be a radiation strike on CW. Thus, if the CW node is floating at the time it is registered to CW^*, it will retain its correct value.

- If there is an SET event in the transitive fan-in of P or P^*, then this would have caused the values of P and P^* to be different in the worst case, causing the CWSP element to protect against the glitch.

- If the glitch is caused on Q, then the set of flip-flops that are sequentially adjacent to *DFF_modified* are responsible for protecting against it. Since *all* flip-flops are implemented with CWSP elements, this causes no erroneous computations. Further, if a glitch on Q causes EQ to be driven low, then the current computation is redone (albeit needlessly). However, no incorrect computation is performed.

- If an SET event in the *Equivalence Checker* circuit or the AND gate $AND1$ causes EQ and thereby $EQGLB$ to become low, there are two scenarios to be considered.

  - If the glitch is present at the positive edge of CLK, it will lead to a recomputation. Since only one SET glitch can occur at a time, the value of CW^* will be correct, so the correct computation is redone (albeit needlessly).
  - A glitch on $EQGLB$ at any other time is neither latched to $EQGLB_F$ nor it is used to determine the input to *DFF_modified* for the next clock cycle. It is therefore silently ignored. Also, since the decision to trigger a bubble in the pipeline at the architectural level is made if $EQGLB$ is low at the positive edge of CLK, no recomputation will be triggered.

- If there is an SET event in *DFF1*, it may lead to $EQGLB_F$ being low. This will ensure that EQ becomes high in the next clock cycle, which is benign considering that the probability of two strikes in two consecutive clock cycles is extremely low, as discussed earlier.

- If there is an SET event in DFF2, it might result in a glitch at CW^*. However, in that case, EQ would be high, and input D of the system flip-flop would be used for the computation. Thus, the glitch at CW^* is inconsequential.

The key feature of the technique presented in this thesis is that it achieves 100% SET tolerance, unlike [1]. The SET correction circuitry is connected on a secondary path (not on the functional path), and hence the delay penalty is extremely small (much smaller than [1, 3]). The system requires recomputations in case of an SET event. The above analysis of the CWSP element based SET tolerance circuitry guarantees radiation tolerance of the design. In particular, the technique can tolerate SET glitches up to a width $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$, where Δ_1 and Δ_2 are fixed delays associated with the SET protection circuitry. The expressions for Δ_1 and Δ_2 are derived in section III-C.

It is also possible to modify the proposed approach for detection purposes only and use an alternative scheme for correction, in case an SET-induced error was detected. For example, the entire pipeline can be flushed whenever an error condition is found (triggered by $EQGLB$ signal being low). This will increase the recovery time, but the area overhead will be lower. The area overhead for this case was studied as well, and is presented in section IV-E. Note that the recovery mechanism of the proposed approach is better than flushing the entire pipeline in case the probability of a radiation strike is very high. Consider that the pipeline depth of a design is twelve and hypothetically, consider that there is a radiation strike every 12 clock

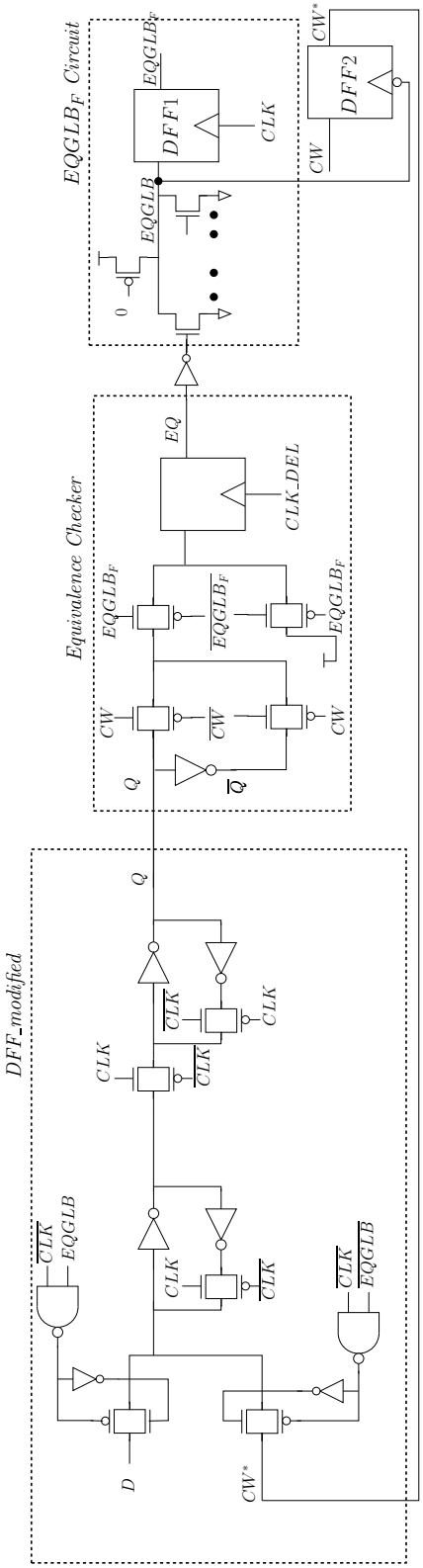


Fig. III.3. Gate Level View of the proposed SET tolerant design

cycles. Note that the actual probability of a radiation strike is much lower for our design in a 70nm process (used for our experiments) and it was computed earlier in this section. However, with technology scaling, the probability of radiation strikes is expected to increase. Suppose the radiation strike induces an error in a flip-flop belonging to the last pipeline stage of a design. If the pipeline is flushed, it will take 12 clock cycles to restore the design to the state it was in just before the radiation strike had occurred. At this time, there is another radiation strike which again causes the pipeline to be flushed. This process could go on forever and the circuit computation will not progress. However, with the proposed recovery mechanism of our approach, only one clock cycle is lost every time there is an SET induced error. So, the circuit will continue to do the correct computation, with only one extra clock cycle for recomputation each time an error is detected.

III-B. Circuit level design

Figure III.3 describes the proposed technique at the gate level. The circuit blocks (*DFF_modified*, *Equivalence Checker* and $EQGLB_F$ *Circuit*) from Figure III.1 are marked with a dotted outline in this figure. The CWSP element and its delay circuitry is not shown in Figure III.3.

The *Equivalence Checker* block consists of an XNOR gate, followed by a MUX with $EQGLB_F$ as the select signal. The purpose of this MUX was explained in section III-A. The output of the MUX is fed to a flip-flop, which is clocked by the rising edge of CLK_DEL (CLK delayed by $2\delta + D_{CWSP}$). A logical AND of the EQ outputs of all the flip-flops in the design is used to generate the $EQGLB$ signal. Instead of using an AND gate, it is more area efficient to achieve the same functionality by performing a NOR of the inverted EQ signals. It was experimentally

seen (using SPICE simulation) that the delay of the pseudo NMOS NOR gate with up to 30 inputs is reasonable (about 80ps). For designs with more than 30 flip-flops (EQ signals), a multilevel AND structure was used. Our experiment results account for the extra delay and area overhead of the multilevel AND gates. For $EQGLB$ signal, to keep the layout-induced delays low, all the flip-flops that provide input to the AND gate which generates the $EQGLB$ signal should be placed close to each other. Note that even if the delay of the AND gate generating the $EQGLB$ signal is high, this results in an increase in the delay in the secondary path and the functional path is not impacted. Thus, the delay overhead of the proposed approach will be unaltered by an increase in the delay for the $EQGLB$ signal. The Master latch of *DFF_modified* is modified so that when $EQGLB$ is high, the Master latch input is connected to D. When $EQGLB$ is low (in case of an equivalence check mismatch in one of the flip-flops), then the Master latch input is connected to CW^* (the guaranteed error-free value).

Devices in the SET protection circuitry are minimum-sized (except in the CWSP element), to minimize the area overhead required to achieve SET protection. PMOS gate widths are made the same as NMOS gate widths, for the same reason. The protection circuit was simulated in SPICE to verify for correct operation. There was a 66mV reduction in the noise margin of an inverter in the protection logic due to the skewed sizing approach. However, since this skewed sizing is *only* used in the secondary path, and all the nodes in the protection circuitry are SET immune based on the discussion of section III-A, this is not a problem. The functional path is not impacted by this skewed sizing.

The delay elements for generating the delayed input P and delayed clock CLK_DEL (Figure III.1) are obtained by connecting a high resistivity POLY2 wire in series with the input of a minimum-sized inverter (with its PMOS device width equal to the width

of the NMOS device). For the following discussion, one POLY2 resistor followed by an inverter is defined as a *segment*. For $\tau_\beta = 50$ps, $\tau_\alpha = 200$ps and $Q = 100fC$, 4 segments are needed to achieve a delay δ, and 8 segments to implement the delay element for CLK_DEL. For $Q = 150fC$ (same values of τ_α and τ_β), 4 and 10 segments can be utilized to achieve a delay of δ and CLK_DEL respectively. A higher delay is obtainable with 4 segments for $Q = 150fC$ compared to $Q = 100fC$ by increasing the value of the POLY2 resistors used. Note that the delay element can be modified to provide different values of delay by either changing the number of segments or the value of the resistors. The value of the resistors is limited since the output of the resistors should transition between VDD and GND within a duration equal to the segment delay.

Note that in the proposed approach, the Master latch of the system flip-flop needs to multiplex its input from the combinational logic (if there was no SET induced error) or from the CW^* signal (in case there was an SET induced error). To minimize the delay overhead, the MUX is folded into the Master latch itself. This results in a minimal delay penalty. The modified Master latches used in the RAZOR approach [44, 45, 46] add a MUX in the critical delay path.

III-C. Maximum tolerable glitch width

The maximum width of a SET induced glitch that can be protected by the proposed radiation hardening scheme is determined as the minimum of two quantities ($1/2(D_{min} - \Delta_1)$ and $1/2(D_{max} - \Delta_2)$). D_{min} and D_{max} are the minimum and maximum delays of the combinational logic respectively. This section provides the analysis that yields these two conditions.

In Figure III.1*b*), consider an SET glitch of width δ at the D input of the system

flip-flop (*DFF_modified*). Let us assume that the glitch begins just before the rising edge of CLK. In an unprotected circuit, this could have led to incorrect system evaluation. The input P^* to the CWSP element is at its correct value after time δ. The second input to the CWSP element attains its correct value after an additional delay of δ. Thus, the output of the CWSP element is guaranteed to be correct only after a delay of $2\delta + D_{CWSP}$, Thus, the P^* input to the CWSP element or the D input of the *DFF_modified* should be stable for a time duration of at least 2δ (i.e. the new value of D must not be computed before 2δ) to ensure that CW has acquired the correct value of D. Note that D_{min} delay after the positive edge of CLK, the D input may switch causing P and P^* inputs of the CWSP element to be different, thereby causing CW to float. As mentioned in section III-A, CW is susceptible to a radiation strike when it is floating. This could be a problem between t_3 and the rising edge of CLK_DEL (see Figure III.2). However, the difference between rising edge of CLK_DEL and t_3 is the time taken for the combinational part of the *Equivalence Checker* circuit to set up to CLK_DEL. Thus, to ensure that the guaranteed glitch-free value of CW is being used to compute EQ, a small guard-band delay (termed Δ_1) is required to be added to D_{min}. Δ_1 was experimentally found to be equal to 20ps. Thus, to protect the circuit up to a glitch of magnitude δ, the circuit should have $D_{min} \geq 2\delta + \Delta_1$. In other words, the maximum width of a SET induced glitch that can be protected by the proposed approach is less than or equal to $(D_{min} - \Delta_1)/2$.

$$\delta \leq (D_{min} - \Delta_1)/2 \tag{3.1}$$

As described above, the CW signal attains its correct value after a delay of $2\delta + D_{CWSP}$, where D_{CWSP} is the delay of the CWSP element. Additionally, delay is introduced by the XNOR gate used for comparison and the MUX with $EQGLB_F$ as the select signal. Thus, CLK_DEL should be delayed (compared to the system

clock CLK) by:

$$delay\_for\_CLK\_DEL = 2\delta + D_{CWSP} + delay\_of\_XNOR + delay\_of\_MUX + T_{SETUP\_EQ} \tag{3.2}$$

where T_{SETUP_EQ} is the setup time of the flip-flop in the *Equivalence Checker* design.

Now, the CW signal should not be floating (so that a radiation-strike on CW does not result in a glitch on CW) when its value is being used to compute the EQ signal. Since, the EQ signal is registered by CLK_DEL, CW signal should not be floating at the positive edge of CLK_DEL. Thus, the input P^* to the CWSP element should be stable till the positive edge of CLK_DEL. after a delay of $delay\_for\_CLK\_DEL$ after the system clock CLK, After CLK_DEL becomes high, if the EQ signal goes low, $EQGLB$ is pulled low and the CW value is latched to CW^*. In the next clock cycle, CW^* would be used as the input for the system flip-flop. Thus, CW^* should attain its stable value before the next rising edge of the system clock CLK. Therefore, the minimum time period required for the design to protect a glitch of width δ is given by the right hand side of Equation 3.3

$$\begin{aligned} D_{max} + T_{SETUP\_SYS} + T_{CLK\_OUT\_SYS} \geq\ & delay\_for\_CLK\_DEL \\ + T_{CLK\_OUT\_EQ} + delay\_of\_AND1 + T_{CLK\_OUT\_DFF2} + T_{SETUP\_SYS} & \end{aligned} \tag{3.3}$$

where $T_{CLK\_OUT\_EQ}$, $T_{CLK\_OUT\_DFF2}$ and $T_{CLK\_OUT\_SYS}$ are the clock to output delays of the flip-flop in the *Equivalence Checker*, *DFF2* and the system flip-flop respectively. T_{SETUP_SYS} is the setup time for the system flip-flop. Note that the setup time for*DFF2*is not added to the right hand side of Equation 3.3, because CW attains its stable value before the rising edge of CLK_DEL. The left hand side of Equation 3.3 is the minimum duration of the system clock CLK, in terms of the maximum combinational delay D_{max} and the setup and clock-to-output times of the system flip-flop

DFF_modified. This minimum system clock duration must be larger than the right hand side of Equation 3.3 for the output CW^* to be correctly latched in every clock cycle.

Using Equations 3.2 and 3.3, the maximum duration of the SET induced glitch δ which the circuit protects against is:

$$\begin{aligned}\delta \leq 1/2(D_{max} - (T_{CLK\_OUT\_EQ} + T_{CLK\_OUT\_DFF2} + D_{CWSP} \\ - T_{CLK\_OUT\_SYS} + delay\_of\_XNOR + delay\_of\_MUX + T_{SETUP\_EQ} \\ + delay\_of\_AND1)) \\ = 1/2(D_{max} - \Delta_2)\end{aligned} \tag{3.4}$$

For a circuit with a given maximum delay D_{max}, Equation 3.4 can be used to find the value of the maximum SET induced glitch that the circuit can tolerate using this approach. The left hand side of Equation 3.3 is the minimum time period of the design. Thus, if the time period T is directly specified, substituting the expression of $delay\_for\_CLK\_DEL$ from Equation 3.2 to Equation 3.3, the constraint on δ can be obtained as:

$$\begin{aligned}\delta \leq 1/2(T - (T_{CLK\_OUT\_EQ} + T_{CLK\_OUT\_DFF2} + delay\_of\_XNOR \\ + delay\_of\_MUX + T_{SETUP\_SYS} + D_{CWSP} + T_{SETUP\_EQ} + delay\_of\_AND1))\end{aligned} \tag{3.5}$$

In order to compare the results of the approach of this thesis with [1], the circuits presented in the experimental section were designed to tolerate glitches induced by an SET strike with charge Q = 100fC and 150fC and with τ_β = 50ps and τ_α = 200ps. These values of Q, τ_α and τ_β were experimentally simulated using SPICE [47], and found to cause glitches of widths 500ps and 600ps respectively when they strike a minimum-sized inverter. In order to protect the circuit from SET induced glitches of

duration 500ps and 600ps, the circuit should have $D_{min} \geq$ 1020ps and 1220ps respectively (from Equation 3.1, using $\Delta_1 = 20$ps which was experimentally computed). It should also have a D_{max} value satisfying Equation 3.4.

It is also important to analyze the affect of clock skew. First, the D_{min} constraint of Equation 3.1 is analyzed. As explained earlier in this section, to protect against a glitch of size δ, the D input of *DFF_modified* should be stable for at least 2δ. Consider the circuit is working with the minimum time period required for correct functionality ($= D_{max} + T_{SETUP\_SYS} + T_{CLK\_OUT\_SYS}$ as mentioned in Equation 3.3). The worst case scenario for the constraint of Equation 3.1 happens when, between any two flip-flops, the D_{max} path is sensitized in the i^{th} clock cycle and the D_{min} path is sensitized in the $i + 1^{th}$ clock cycle. In this scenario, the D input of *DFF_modified* attains its correct value for the i^{th} clock cycle just before the positive edge of CLK. Now, the value of D for the $i + 1^{th}$ clock cycle will be updated after a delay of D_{min}. Thus, the value of D for the i^{th} clock cycle is stable only a duration of D_{min}. This gives the constraint of Equation 3.1. Now, if there is a skew between any two sequentially adjacent flip-flops, the D_{min} as well as the D_{max} will both be altered by the amount of skew. The time for which the D input of *DFF_modified* is stable still provides the lower bound on D_{min}. Thus, the constraint of Equation 3.1 is not impacted by skew.

Next, the constraint on the time period or D_{max} (Equation 3.3) is analyzed. This constraint ensures that if there is an SET event in the clock cycle i, CW^* is equal to the correct value of D in the i^{th} cycle and is ready before the $i + 1^{th}$ clock cycle. Consider any two flip-flops in a design hardened using the proposed approach. Suppose the signals D_1, CLK_1, CLK_DEL_1, EQ_1, CW_1^* correspond to the first flip-flop and the signals D_2, CLK_2, CLK_DEL_2, EQ_2 and CW_2^* correspond to the second flip-flop (these signals have the same meaning as the D, CLK, CLK_DEL, EQ and CW^* nets of Figure III.1 which were analyzed in section III-A). Without

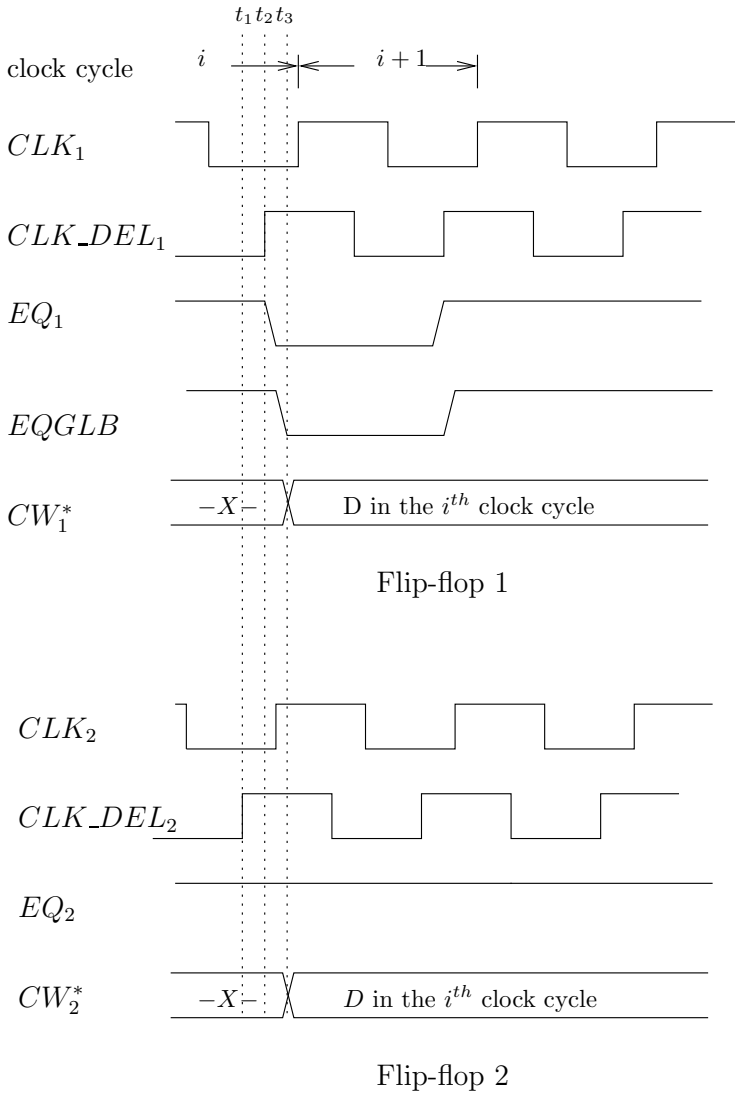


Fig. III.4. Analysis of clock skew on the proposed SET tolerant design

loss of generality, consider the case when the skew between the two flip-flops causes CLK_1 (CLK_DEL_1) to be delayed compared to CLK_2 (CLK_DEL_2). This is shown in Figure III.4. The EQ signals are registered at the positive edge of CLK_DEL, thus EQ_1 will be registered after a delay equal to the amount of skew compared to EQ_2. Suppose there is an SET event in the i^{th} clock cycle which causes EQ_1 to fall. As shown in Figure III.4, this causes $EQGLB$ (which is the logical AND of all the EQ signals) to become low. A falling edge on $EQGLB$ registers the value of D_1 in the i^{th} clock cycle to CW_1^* and the value of D_2 in the i^{th} clock cycle to CW_2^*. Now, CW_1^* is ready before the next positive edge of CLK_1. However, CW_2^* is not ready before the positive edge of CLK_2. This is because the minimum time needed for the value of CW^* to be updated in time for the next clock cycle is not met for the second flip-flop. Thus, the maximum amount of clock skew should be added to the right hand side of Equation 3.3, to incorporate the clock skew. Thus, the time period or the D_{max} constraint is impacted by the maximum clock skew and becomes tighter by the amount of skew.

CHAPTER IV

EXPERIMENTAL RESULTS

IV-A. Stimulus and model card for the experiments

The SET tolerance of the radiation-hardened circuit structures proposed in this thesis (Figures III.1 and III.3) was tested by SPICE [47] simulations. A 65nm BPTM [48] model card was used, with $VDD = 1V$ and $V_{T_N} = |V_{T_P}| = 0.22V$. The benchmark circuits for the simulations were chosen from the LGSynth93 [49] and the ISCAS85 [50] design suites.

The radiation strike was modeled as a current source described as $I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}$ $(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})$ [23, 24].

IV-B. Results using Q, τ_α and τ_β of [1]

In order to compare the experimental results using the approach of this thesis with [1], the experiments were performed using $\tau_\beta = 50ps$, $\tau_\alpha = 200ps$ and $Q = 100fC$ and $150fC$. These values were used in [1] as well. Firstly, a radiation event with these values of Q, τ_α and τ_β is used to strike a minimum-sized inverter, and the width of the voltage glitch is experimentally measured. The results from this simulation are shown in Figure IV.1. Note that the voltage of the node rapidly rises, before saturating at 1.6V. This occurs due to the turning on of junction diodes in the devices (which turn on at ∼0.6V above VDD). The resulting maximum glitch widths were found to be 500ps and 600ps (for $Q = 100fC$ and $150fC$ respectively).

Based on this information, the delay elements were designed to have a delay value δ (for delaying the D signal of *DFF_modified*) and $2\delta + D_{CWSP} + T_{SETUP\_EQ}$ (for deriving CLK_DEL). The delay circuit was constructed as discussed in section III-B.

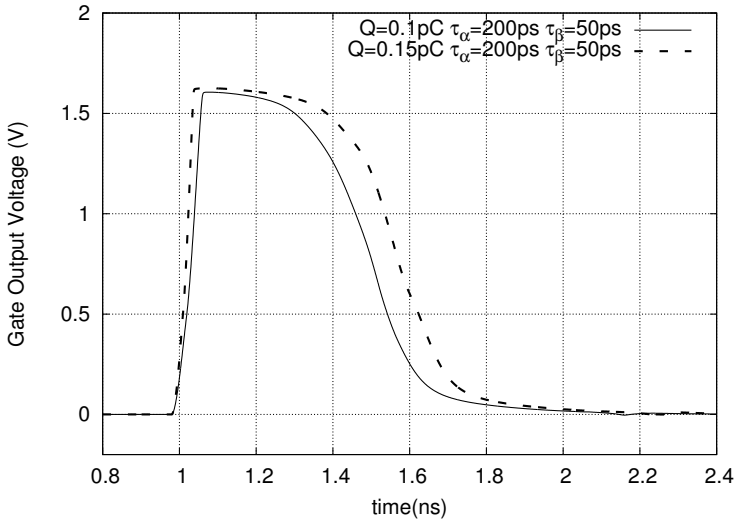


Fig. IV.1. Voltage glitch waveform

Also, the CWSP element of the proposed design should be SET tolerant for voltage glitches induced by a radiation strike which has $\tau_\beta = 50ps$, $\tau_\alpha = 200ps$, $Q = 100fC$ and $150fC$. The exercise of determining the sizing of the CWSP devices was conducted via SPICE [47] simulations. The CWSP element for 100fC SET tolerance was sized 30/12[1]. For 150fC SET tolerance, the CWSP element was sized 40/16.

According to the discussion of section III-C, in order to protect a glitch of maximum width δ, the minimum value of D_{max} can be computed using Equation 3.3. The only variable quantity in this equation is $delay\_of\_AND1$. For a 30-input NOR gate, to protect a circuit from glitches of widths 500ps and 600ps, the minimum value of D_{max} was found to be 1405ps and 1605ps respectively. For the testcases with more than 30 outputs, a multi level gate was used to ensure that the D_{max} constraint is met. Also, the minimum value of D_{min} can be computed using Equation 3.1. The minimum D_{min} value is 1020ps and 1220ps for $Q = 100fC$ and $150fC$ ($\tau_\beta = 50ps$,

[1] A size of X/Y indicates that all the PMOS devices were X times minimum sized, and the NMOS devices were Y times minimum.

Table IV.1. Area overhead for $Q = 0.15pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

	Area overhead		
Circuit	Regular (μm^2)	Hardened (μm^2)	%Ovh.
alu2	28.25	37.29	32.00
alu4	53.88	65.88	22.27
apex2	399.67	404.28	1.15
C3540	97.83	130.53	33.43
C6288	223.59	271.09	21.24
seq	421.60	473.53	12.32
C7552	187.68	347.62	85.23
C880	36.15	74.78	106.83
Average			39.31

$\tau_\alpha = 200ps$) respectively.

The SET tolerant portion of the design proposed in this thesis is not in the critical path of the system computation. It is sized carefully, so as to add minimal parasitic capacitances to the system flip-flop delay path. Based on SPICE simulations, the CLK-to-Q delay ($T_{CLK\_OUT\_SYS}$) increased to 76ps using the proposed approach (compared to 69ps). However, the setup time (T_{SETUP_SYS}) decreased by 2ps (from 40ps to 38ps). Additionally, the increased load on the D input of the Master system latch resulted in an increase in the delay (by D_{INPUT_LOAD} = 6.5ps) of the combinational output of the design. As a consequence, the total delay penalty associated with adding the proposed SET tolerant circuit is 11.5ps per flip-flop. These values have been used to calculate the delays as per the left hand side of equation 3.3. For

Table IV.2. Delay overhead for $Q = 0.15pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

	Delay overhead			
Circuit	D_{max} (ps)	Regular (ps)	Hardened (ps)	%Ovh.
alu2	1624.54	1733.54	1745.04	0.66
alu4	1700.28	1809.28	1820.78	0.64
apex2	2069.55	2178.55	2190.05	0.53
C3540	1931.05	2040.05	2051.55	0.56
C6288	5141.06	5250.06	5261.56	0.22
seq	2936.80	3045.80	3057.30	0.38
C7552	2472.79	2581.79	2593.29	0.45
C880	1692.80	1801.80	1813.30	0.64
Average				0.51

the protected case, the extra 6.5ps due to the increased load on the D input of the Master system latch (explained above) was also included.

Table IV-B shows the area overheads and Table IV-B shows the delay overheads associated with the proposed approach, for several examples. These tables quantify the overheads for SET tolerance of up to 150fC. In Table IV-B, Column 1 describes the circuit under consideration. Columns 2 and 3 report the active area in μm^2 for regular design and a design hardened by the proposed approach. Column 4 reports the percentage area overhead of this approach. In Table IV-B, Column 1 lists the circuits under consideration. Column 2 provides the D_{max} value for the circuits. As required, all the testcases in Table IV-B have a $Dmax$ value greater than 1605ps. Columns 3 and 4 report the delays for a regular design and a design hardened with

the approach of this thesis. Column 5 reports the percentage delay overhead of the approach of this thesis. Table IV-B and Table IV-B show the corresponding results for $Q = 100$fC.

Table IV.3. Area overhead for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

	Area overhead		
Circuit	Regular (μm^2)	Hardened (μm^2)	%Ovh.
alu2	28.25	36.38	28.78
alu4	53.88	64.66	20.02
apex2	399.67	403.82	1.04
C1908	43.66	77.01	76.38
C3540	97.83	127.19	30.02
C6288	223.59	266.23	19.07
C7552	187.68	331.22	76.48
C880	36.15	70.83	95.91
seq	421.60	468.22	11.06
C5315	152.17	315.63	107.42
dalu	65.59	87.00	32.63
Average			45.34

As per [51], industrial circuits are typically balanced to have roughly equal longest and shortest path lengths. This is done in order to avoid hold-time violations. State of the art technology mapping tools ensure that the D_{min} is about 80% of D_{max} [51]. Based on this, D_{min} was taken to be 80% of D_{max}. Note that the $\delta \leq min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$ constraint is satisfied for all the circuits in

Table IV.4. Delay overhead for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

	Delay overhead			
Circuit	D_{max} (ps)	Regular (ps)	Hardened (ps)	%Ovh.
alu2	1624.54	1733.54	1745.04	0.66
alu4	1700.28	1809.28	1820.78	0.64
apex2	2069.55	2178.55	2190.05	0.53
C1908	1562.65	1671.65	1683.15	0.69
C3540	1931.05	2040.05	2051.55	0.56
C6288	5141.06	5250.06	5261.56	0.22
C7552	2472.79	2581.79	2593.29	0.45
C880	1692.80	1801.80	1813.30	0.64
seq	2936.80	3045.80	3057.30	0.38
C5315	1475.91	1584.91	1596.41	0.73
dalu	1489.09	1598.09	1609.59	0.72
Average				0.56

Tables IV-B through IV-B.

The difference in the SET protection circuit (Figure III.1) for $Q = 100fC$ and $150fC$ is the delay element and the size of the CWSP element. The path through the system flip-flop remains unaltered. Therefore, the delay penalty in both the cases is same. Based on the results in Table IV-B and Table IV-B, the average area overhead is found to be 45.34% (39.31%) for $Q = 150fC$ ($Q = 100fC$). However, the corresponding delay penalty is 0.56% (0.51%) which is extremely small. Hence, the proposed SET protection approach has a negligible delay penalty.

Table IV.5. Summary of results compared to the approach of [1] and [3]

Technique	Area overhead (%)	Delay overhead (%)	Protection
Our Approach	42.33	0.54	100%
[1]	42.95	2.80	90%
[3]	17.60	28.65	100%

IV-C. Comparison with existing techniques

Table IV-C summarizes the results using the approach of this thesis in comparison to the results of [1] and [3]. The approach of [1] reports average area overheads which are comparable, and larger average delay overheads (about 2.8%). Also, the approach of [1] provides 90% protection to SET induced glitches, while the proposed approach provides 100% protection. For high speed, mission critical applications, the reduced delay of the proposed scheme could be extremely crucial, especially when it comes with a no additional area penalty compared to [1]. In [3], the calculated average area overheads were about 17.6%. However, the average delay penalty was quite substantial (28.65%). Therefore, the proposed approach provides an attractive design point.

IV-D. Smaller values of glitch compared to section IV-B

For the cases in which D_{max} is less than 1405ps (corresponding to $Q = 100fC$), protection can be provided against SET induced glitches of width up to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$. To achieve this, in the circuit for SET protection scheme shown in Figure III.1, the delay element needs to be changed to a value $\delta = min\{(D_{min}$

Table IV.6. Area overhead of the proposed protection approach for glitch width up to $\delta = min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$

	Area overhead		
Circuit	Regular (μm^2)	Hardened (μm^2)	%Ovh.
apex4	200.03	225.41	12.69
apex3	139.13	208.59	49.93
b11_opt_C	55.43	104.70	88.90
C1355	46.01	88.65	92.67
C432	15.12	24.58	62.54
C499	46.01	88.65	92.67
ex5p	178.18	264.90	48.67
k2	88.53	151.36	70.97
apex1	111.43	174.26	56.39
ex4p	17.59	24.40	38.66
Average			61.41

$-\Delta_1)/2, (D_{max} - \Delta_2)/2\}$. This can be achieved by reducing the value of the POLY2 resistors used for the delay element, or by reducing the number of segments used to construct the delay elements (a discussion on segments and how they are used to construct the delay elements was presented in section III-B . Also, the CWSP element can be made smaller as well, since it needs to tolerate a glitch of lesser width (compared to $Q = 100fC$). However, we use the SET protection circuit for $Q = 100fC$ is used to compute the area overheads shown in Table IV-D. Therefore, this is an upper bound on the actual area overhead. All the columns in this table have the same

meaning as the columns of Tables IV-B and IV-B. The delay overhead is presented in Table IV-D. The delay overhead is calculated in the manner discussed earlier in this section and all the columns in Table IV-D have the same meaning as those of Table IV-B. The maximum width of the SET induced glitch (δ) that the proposed technique can protect these circuits against is shown in Table IV-D. It is equal to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$ as per the analysis given in section III-C. For this computation, D_{min} was taken to be 80% of D_{max} [51]. The value of Δ_2 used was the same as the value used for the experiments with $Q = 100fC$, which was equal to 405ps. From Tables IV-D and IV-D, it can be seen that the delay overhead is minimal (0.99%) with an area overhead of 61.41%. Note that this area overhead is an overestimate of the true area overhead (as discussed above).

IV-E. Error recovery using alternative approaches

A mentioned in section III-A, it is possible to modify the proposed approach and use it for SET-induced error detection *only* and use an alternative approach (such as pipeline flushing) for recovery. This will reduce the area overhead of our scheme since the circuit for recomputation is no longer needed. In Table IV-E, Column 1 lists the circuits under consideration, Column 2 provides the area overhead in case both detection and recovery were provided (this is same as the area overhead provided in Table IV-B). Column 3 provides the area overhead of the proposed circuit if it is used for detection only (for $Q = 0.15pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$). Note that the reduction in area overhead is very small if we remove the recovery-related circuitry. Thus, it seems that our approach is best used for detection as well as recovery. Similar results are provided for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$ (Table IV-E) and for smaller values of Q (Table IV-E).

Table IV.7. Delay overhead of the proposed protection approach for glitch width up to $\delta = min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$

	Delay overhead			
Circuit	D_{max} (ps)	Regular (ps)	Hardened (ps)	%Ovh
apex4	1396.65	1505.65	1517.15	0.76
apex3	1230.12	1339.12	1350.62	0.86
b11_opt_C	1270.95	1379.95	1391.45	0.83
C1355	1012.19	1121.19	1132.69	1.03
C432	1385.39	1494.39	1505.89	0.77
C499	1012.19	1121.19	1132.69	1.03
ex5p	1195.08	1304.08	1315.58	0.88
k2	1170.34	1279.34	1290.84	0.90
apex1	982.90	1091.90	1103.40	1.05
ex4p	630.38	739.38	750.88	1.56
Average				0.99

IV-F. Power overhead

In this section, the power overhead for our protection scheme is provided. The results in this section are not compared with [2, 3, 1] since these efforts did not quantify their power overhead. Typically, it is well known that the power overhead is roughly equal to the area overhead. To validate this, we computed the increase in average power (when there is no radiation strike) and the area for a single flip-flop with the proposed approach. This experiment was carried out for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$ and the results are shown in Table IV-F. In Table IV-F, the first column

Table IV.8. Maximum glitch width $\delta = min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$ for the circuits of Tables IV-D and IV-D

Circuit	D_{max} (ps)	Max. Glitch Width δ (ps)
apex4	1396.65	495.83
apex3	1230.12	412.56
b11_opt_C	1270.95	432.97
C1355	1012.19	303.60
C432	1385.39	490.19
C499	1012.19	303.60
ex5p	1195.08	395.04
k2	1170.34	382.67
apex1	982.90	288.95
ex4p	630.38	112.69

reports the quantity measured (area, dynamic power and leakage power), the second column provides the data for an unprotected flip-flop while the third column provides the data for a flip-flop protected by our approach (using the circuit of Figure III.1). Column 4 provides the overhead. The area overhead is 6.3×, while the dynamic and leakage power overhead is 5.5 and 7.3 times respectively. Under normal operation, note that the portion of our circuit used for recovery is not exercised. Thus, the dynamic power overhead is slightly less than the area overhead. However, the leakage power overhead is minimally higher.

Table IV.9. Area overhead for detection only using the proposed approach for $Q = 0.15pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

Circuit	%Ovh. (Detection & Recovery)	%Ovh. (Detection only)
alu2	32.00	30.58
alu4	22.27	21.53
apex2	1.15	1.05
C3540	33.43	33.02
C6288	21.24	21.06
seq	12.32	12.22
C7552	85.23	85.01
C880	106.83	105.72
Average	39.31	38.77

IV-G. Process and volatge variations

To test the robustness of our circuit under PVT variations, Monte Carlo simulations were done by varying *i*) V_T, *ii*) VDD and *iii*) $Lmin$. For each parameter, we assumed the μ to be the nominal value of each parameter. The σ was chosen to be such that $3\sigma = 0.1 \times \mu$. Each parameter was assumed to be normally distributed. Given the large number of transistors in the circuit, we assumed that all devices in the design shared the same value of VDD, V_T and $Lmin$. A total of 500 SPICE simulations were performed for each parameter. The minimum time period required for the circuit to work correctly was found, across these variations. As mentioned in section IV-B, for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$, the proposed approach nominally protects against a radiation strike on any node in the circuit as long as the D_{min} is

Table IV.10. Area overhead for detection only using the proposed approach for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

Circuit	%Ovh. (Detection & Recovery)	%Ovh. (Detection only)
alu2	28.78	27.35
alu4	20.02	19.27
apex2	1.04	0.94
C1908	76.38	75.46
C3540	30.02	29.61
C6288	19.07	18.89
C7552	76.48	76.27
C880	95.91	94.80
seq	11.06	10.96
C5315	107.42	107.16
dalu	32.63	32.01
Average	45.34	46.54

more than 1020ps and D_{max} is greater than 1405ps. With our approach, a D_{max} of 1405ps corresponds to a clock period of ($T = D_{max} + T_{SETUP\_SYS} + T_{CLK\_OUT\_SYS} + D_{INPUT\_LOAD} = 1405 + 79 + 38 + 6.5 =$) 1528.5ps. We would like to know the amount by which the clock period and Q values are derated due to process and supply voltage variations.

Our circuit was designed so that it can operate with the minimum time period. When variations are applied, a guard band is needed since a) the worst case delay with variations is higher than the nominal delay, so the minimum time period for which

Table IV.11. Area overhead for detection only using the proposed protection approach for glitch width up to $\delta = min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$

Circuit	%Ovh. (Detection & Recovery)	%Ovh. (Detection only)
apex4	12.69	12.49
apex3	49.93	49.64
b11_opt_C	88.90	88.17
C1355	92.67	91.80
C432	62.54	59.89
C499	92.67	91.80
ex5p	48.67	48.45
k2	70.97	70.52
apex1	56.39	56.02
ex4p	38.66	36.38
Average	61.41	60.51

the circuit can operate correctly increases b) The delays in the circuit do not scale by the same amount for all the paths in the design. In particular, consider the case when the devices in the circuit slow down due to variations. Thus, CW (Figure III.1 described in section III-A) takes longer to achieve its correct value. However, it was experimentally noticed that the delay for CLK_DEL increases by a smaller amount. Thus, EQ gets registered before CW achieves its correct value. To resolve this issue, we propose to design the circuit (in the nominal case) for a larger value of charge than we are required to protect against. This is explained next. In a circuit designed to handle a radiation strike with charge Q, suppose there is a radiation strike with a

Table IV.12. Area and power overhead for a single flip-flop for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$

Metric	Regular	Hardened	Ovh.
Area	0.28 μm^2	$1.77\mu m^2$	6.3×
Dynamic power	$1.41e^{-5}$	$6.11e^{-5}$	5.5×
Leakage power	$0.014e^{-5}$	$0.102e^{-5}$	7.3×

smaller magnitude of charge Q' (τ_α and τ_β remaining the same). Suppose the worst case glitch induced by Q' is δ'. Since Q' is less than Q, the glitch δ' induced by Q' will be smaller than the glitch δ induced by Q. Under the influence of variations, CW will achieve its correct value after a delay of $\delta + \delta'$, which is earlier than the 2δ delay corresponding to a radiation strike with charge Q (in the circuit designed under nominal conditiond). So, if we strike our circuit designed nominally for a radiation strike with charge Q, with variations, it can effectively protect the design up to a smaller value Q'. Similarly, the nominal clock period of the circuit (T) increases to a value (T') under the influence of variations.

We first calculated the minimum time period T' and the Q' for which our circuit (designed for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$ with a nominal time period T = 1528.5ps) operates correctly under 3σ variation in the process and supply volatge parameters. The results from this experiment are shown in Table IV-G. If VDD, V_T and $Lmin$ are varied independently, the minimum time period T' was found to be 1680ps, 1590ps and 1740ps respectively and the value of Q' was 76fC, 90fC and 72fC respectively. Thus, the change in V_T had a least impact, while a change in $Lmin$ has the maximum effect. In Table IV-G, the last row provides the results when VDD, V_T

Table IV.13. Minimum time period and charge for which the circuit designed for $Q = 0.10pC$, $\tau_\alpha = 200ps$ and $\tau_\beta = 50ps$ operates correctly

Variation	Q' (fC)	Time period (ps)
VDD	76	1680
V_T	90	1590
$Lmin$	72	1710
consolidated	63	1750

Table IV.14. μ and σ of the time period from Monte Carlo simulations

Variation	μ(ps)	σ(ps)
VDD	1519.7	50.1
V_T	1526.1	14.5
$Lmin$	1514.2	52.9
consolidated	1525.1	53.1

and $Lmin$ were varied together. The minimum time period for this case was observed to be 1750ps, and is higher than the previous 3 cases, as expected. Also, the Q' was found to be 63fC.

For Monte Carlo simulations, we simulated our circuits with the Q' and T' values provided in Table IV-G. For the cases when VDD, V_T and $Lmin$ are varied independently, 500 Monte Carlo simulations were done and the resulting time period was observed for each of these simulations. The results from these simulations are provided in Table IV-G. A shown in Table IV-G, the μ and σ of the time period was

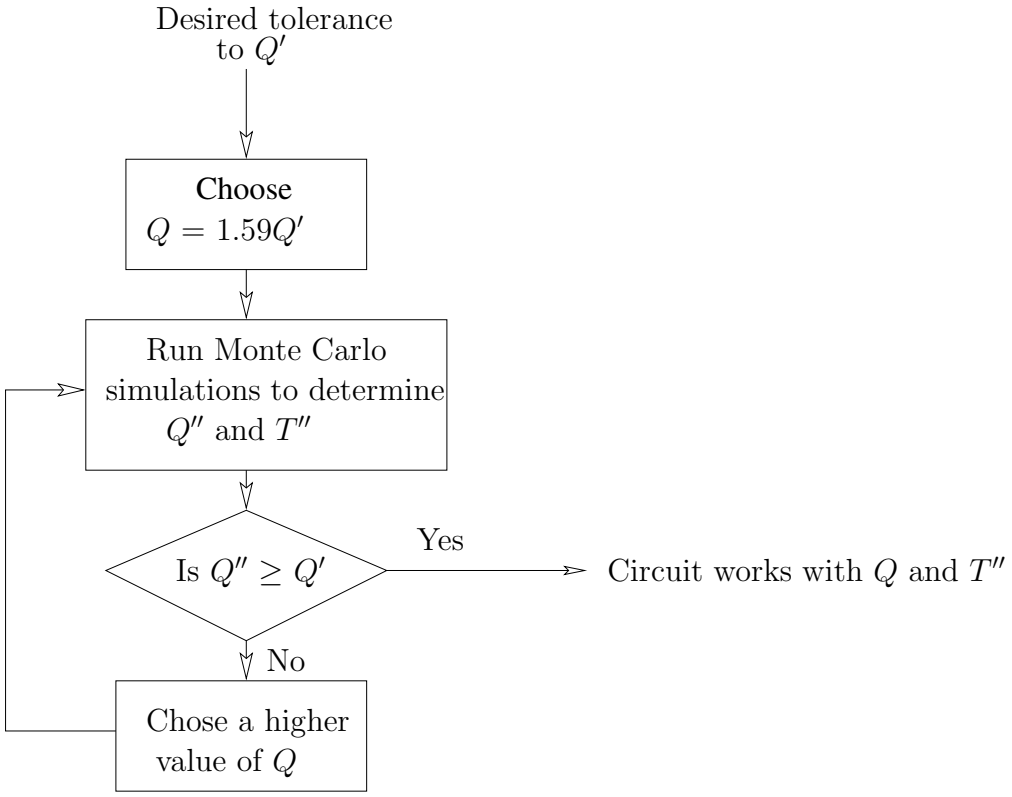


Fig. IV.2. Flowchart to determine the value of Q and time period the circuit needs to be designed with such that it is process variations tolerant against a radiation strike with charge Q'

found to be 1519.7ps and 50.1ps for VDD, 1526.1ps and 14.5ps for V_T and 1514.2ps and 52.9ps for $Lmin$ variations. For the case when VDD, V_T and $Lmin$ are varied together, 1500 Monte Carlo simulations were done and the resulting μ and σ values are 1525.1ps and 53.1ps respectively. The μ of the time period is close to the nominal time period for all the simulations. The σ is maximum for the case when all the parameters are varied together and minimum for V_T variations. In all the 3000 simulations, the correct operation was observed under all possible strike conditions, as expected.

In order to design a circuit to protect against a radiation strike with charge Q' and also be variation tolerant, we propose to design the circuit for a larger value of charge Q. Q can be computed by using an iterative process which is described in the flowchart shown in Figure IV.2. As mentioned in Table IV-G, for the case when VDD, V_T and $Lmin$ are varied together, the circuit designed nominally for $Q = 100fC$ operates correctly for $Q = 63fC$ under variations. This indicates that a circuit needs to be designed for roughly (100/63 =) 1.59 times the charge it is required to protect against. As indicated in the flowchart of Figure IV.2, first choose $Q = 1.59 * Q'$. Design the circuit to protect against a nominal value of Q. Use Monte Carlo simulations to determine the value Q'' and clock period T'' for which the circuit operates correctly with variations. If $Q'' \geq Q'$, it means that the circuit will operate correctly with Q' and clock period T'' (to reduce the area overhead, you can try reducing the value of Q to determine if there is a smaller Q with which your circuit can operate correctly under variations). If $Q'' < Q'$, it means that the circuit is still not protected against a radiation strike with charge Q'. In this case, increase Q and repeat the procedure described above.

By using the approach outlined above, the higher value of Q can be derived along with the new increased clock period T.

CHAPTER V

CONCLUSIONS

In this thesis, a novel radiation-hardened digital design approach is presented. This approach uses Code Word State Preserving (CWSP) elements at each flip-flop of the design, leaving the combinational portion of the design unaltered. Since the CWSP elements are connected off the critical delay path in the design, the proposed SET tolerant approach has negligible delay overheads. The proposed CWSP based approach provides 100% protection for SET induced glitches of widths up to $min\{(D_{min} - \Delta_1)/2, (D_{max} - \Delta_2)/2\}$. In case an SET error is detected, then the current computation is repeated, using the correct output, which is generated later in the same clock period by the CWSP element. The CWSP logic is designed to minimally impact the critical delay path of the design, with a delay penalty (averaged over several designs) of less than 1%. Thus, the proposed technique is applicable for high-speed designs, where the additional delay associated with SET protection must be kept at a minimum.

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