NEW LEADING/TRAILING EDGE MODULATION STRATEGIES FOR TWO-STAGE PFC AC/DC ADAPTERS TO REDUCE DC-LINK CAPACITOR RIPPLE CURRENT

A Thesis

by

JING SUN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,   Prasad Enjeti
Committee Members, Sunil Khatri
                    Chanan Singh
                    Sing-Hoi Sze
Head of Department, Costas N. Georghiades

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ABSTRACT

New Leading/Trailing Edge Modulation Strategies for Two-Stage PFC AC/DC Adapters

to Reduce DC-Link Capacitor Ripple Current.

(May 2007)

Jing Sun, B.E., Shanghai Jiao Tong University, Shanghai, China

Chair of Advisory Committee: Dr. Prasad Enjeti

AC/DC adapters mostly employ two-stage topology: Power Factor Correction (PFC) pre-regulation stage followed by an isolated DC/DC converter stage. Low power AC/DC adapters require a small size to be competitive. Among their components, the bulk DC-link capacitor is one of the largest because it should keep the output voltage with low ripple. Also, the size of this capacitor is penalized due to the universal line voltage application. Synchronization through employing leading edge modulation for the first PFC stage and trailing edge modulation for the second DC/DC converter stage can significantly reduce the ripple current and ripple voltage of the DC-link capacitor. Thus, a smaller DC-link capacitance can be used, lowering the cost and size of the AC/DC adapter.

Benefits of the synchronous switching scheme were already demonstrated experimentally. However, no mathematical analysis was presented. In this thesis, detailed mathematical analyses in per-unit quantity are given to facilitate the calculation of the DC-link capacitor ripple current reduction with Leading/Trailing Edge Modulation strategies.

One of the limitations of leading/trailing edge modulation is that the switching frequencies of the two stages need to be equal to achieve the best reduction of the DC-link capacitor ripple current. The DC-link capacitor ripple current will become larger if the switching frequency of the DC/DC converter is larger than that of the PFC pre-regulator, which blocks us to employ higher frequency for isolated DC/DC converter to reduce its transformer size. This thesis proposed a new Leading/Trailing Edge Modulation strategy to further reduce the DC-link bulk capacitor ripple current when switching frequency of DC/DC converter stage is twice the switching frequency of PFC stage. This proposed pulse width modulation scheme was verified by simulation. Experimental results obtained through digital control based on FPGA are also presented in this thesis.

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CHAPTER I

INTRODUCTION

1.1 Introduction

AC/DC adapters are a widely extended application due to the great number of equipment fed from the AC mains that consume low power. This type of devices is used in mobile phones, CD players, PDAs, small home appliances, etc. Mostly in an AC/DC adapter, a cascaded two-stage topology is employed as shown in Figure 1.1. The first stage is power factor correction stage, which regulates the input line current to achieve a high power factor and reduce its harmonic contents. The second stage is usually an isolated DC/DC converter, which provides high frequency isolation and meanwhile step down the high dc output voltage of the first power factor correction stage.
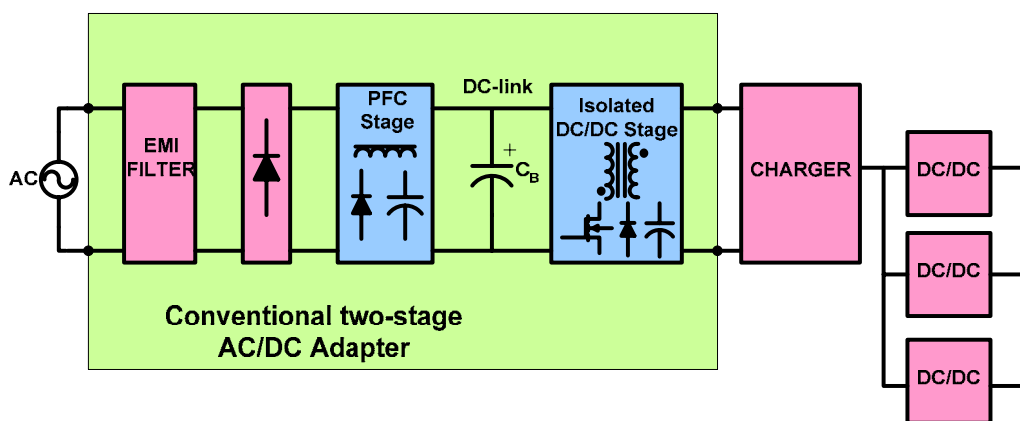
Figure 1.1 Typical structure of AC/DC adapters

This thesis follows the style and format of *IEEE Transactions on Industry Applications.*

1.2 Review of power factor correction techniques

Conventionally, most of the power conversion equipment employs either diode rectifier or thyristor rectifier with a bulk capacitor to converter AC voltage to DC voltage before processing it. Such rectifiers produce input current with rich harmonic content, which pollute the power system and the utility lines. Power quality is becoming a major concern for many electrical users. For example, Figure 1.2(a) shows the circuit diagram of a diode-capacitor rectifier, in which L_K represents the source impedance and C_B is the bulk energy-storage capacitor. Figure 1.2(b) shows that the input current waveform has narrow conduction angle and strong distortion. Figure 1.3 illustrates the harmonic spectrum of the line current.

(a)
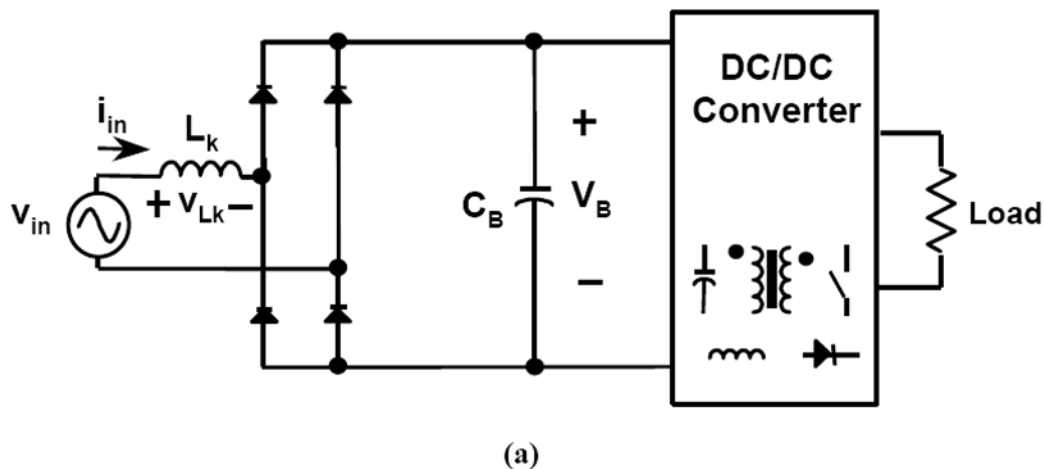
Figure 1.2 Circuit diagrams of the conventional diode rectifier and its conceptual waveforms: (a) circuit diagram, and (b) key line-cycle waveforms
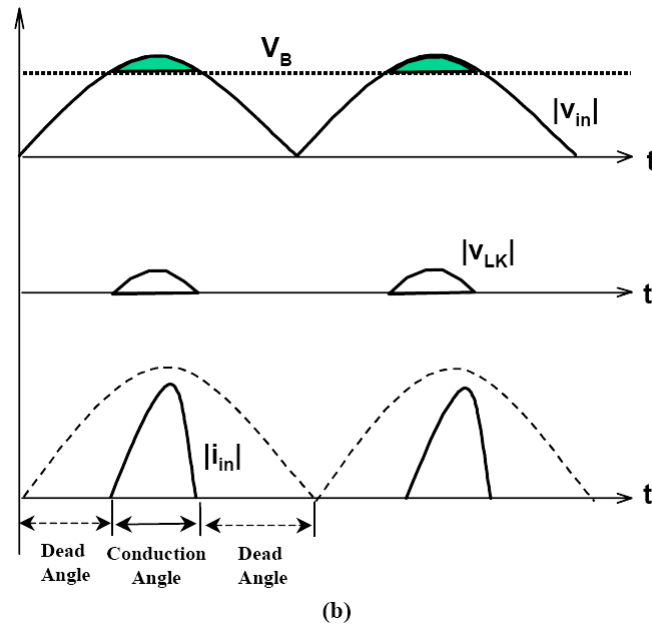
Figure 1.2 Continued
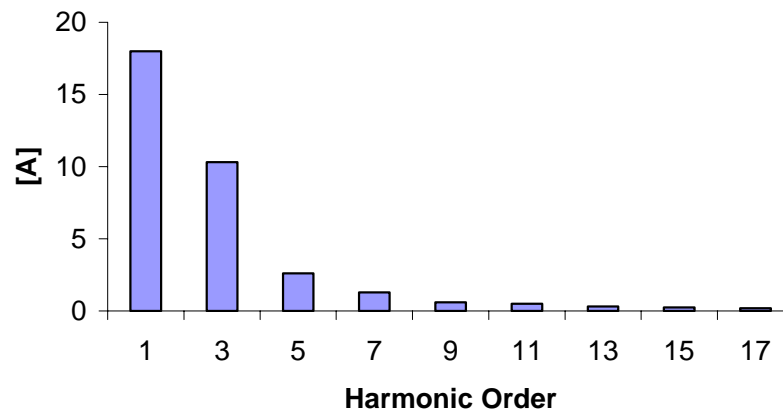
Figure 1.3 Harmonic spectrum of line current

To measure the quality of input power of electrical equipment, power factor (PF) is a widely used term, which is defined as the ratio of average power to apparent power at an AC terminal. The power factor of an off-line equipment can be expressed as the product of two components: the displacement factor $\cos\theta$, which is caused by the phase

difference between the fundamental component of the input current and the sinusoidal input voltage, and the distortion factor, which can be presented by the total-harmonic-distortion (THD) of the input current [1]. In fact, the greatest concern of the off-line rectifier's impact on the power system is not the displacement between the voltage and current, but the input current distortion and current harmonics, since they pollute the power system and causes interference among off-line utilities. To limit the input current harmonics drawn by the off-line equipment, several international regulations such as the IEC 61000-3-2 [2] and its corresponding Japanese regulation have been proposed. These specifications have prompted many power supply manufacturers to intensify their efforts towards finding simple and cost-effective solutions for complying with the specifications. As a result, the techniques for reduction of input current harmonics reduction have been intensively introduced and studied in recent years. Although the main objective is really input-current-shaping (ICS), most people refer their work as power-factor-correction (PFC). In this thesis, the term "PFC" will be used to comply with the common usage.

To comply with the line harmonics standards, a variety of passive and active PFC techniques have been proposed. The passive techniques normally use a simple line-frequency LC filter to both extend the current conduction angle and reduce the THD of the input current of the diode-capacitor rectifier. Due to its simplicity, the passive LC filter could be the high-efficiency and low-cost PFC solution to meet the IEC 61000-3-2 class D specifications in the low power range [3]. However, the passive LC filter has a major drawback, which is its heavy and bulky low-frequency filter inductor.

To reduce the size and weight of the filter inductor, the active PFC techniques have been introduced. In an active PFC converter, the filter inductor "sees" the switching

frequency, which is normally in the 10 kHz to hundreds of kHz range. Therefore, the size and weight of the power converter can be significantly reduced by using a high-frequency inductor. The cost of the active PFC approach can also be lower than that of the passive filter approach if the conversion power increases. The most popular implementation of active PFC is to insert a PFC power stage into the existing equipment to satisfy the regulation. This is referred as the two-stage PFC approach.

1.3 Review of active two-stage power factor correction technique

The single-phase active PFC techniques can be divided into two categories: the two-stage approach and the single-stage approach.

The two-stage approach is most commonly used. In this kind of converters, an active PFC stage is adopted as the front-end to force the line current to track the line voltage, and therefore achieve unity input power factor. The PFC front-end stage converts the AC-input voltage into DC voltage on a bulk energy-storage capacitor. Then a conventional DC/DC converter is used as the second output stage to provide isolation and regulated low output voltage.

Figure 1.4 shows the general structure of the two-stage PFC converter with two independent power stages. The first stage can be buck, boost or flyback converter topologies. Among these three basic power converter topologies), the boost converter shown in Figure 1.5 is the one most suitable for power factor correction applications. This is because the inductor is in series with the line input terminal through the diode rectifier, which gives lower line current ripple and continuous input current can be obtained with an average current mode control chip like UC3854. As a result, a small line

input filter can be used. Furthermore, the power switch is in shunt with the main power flow so that the converter operates efficiently. The buck converter is seldom used as a power factor correction application [4-5], since the input current is discontinuous and it loses control when the line input voltage is lower than the output voltage. The buck-boost and flyback converters are able to control the average line input current [6]. However, the power handling capability is smaller because of its higher voltage and current stresses. Therefore, the boost converter is currently the most popular PFC topology. To achieve unity power factor, the input power is the squared sine waveform while the output power is usually constant for most applications. Thus, the power is unbalanced between the input and the output over half the line cycle. This unbalanced power has to be stored in an energy storage element, like the bulk capacitor. For a boost converter, the output filter capacitor, which is the only bulk capacitor, can deal with this unbalanced power. Therefore, the output voltage has 2nd order line ripple, which is undesirable for many applications. Furthermore, the output voltage is higher than the input voltage, which is unsuitable for step-down applications. Therefore, another DC/DC converter has to be cascaded with this PFC converter to obtain the desired output voltage and tightly regulate the output voltage.
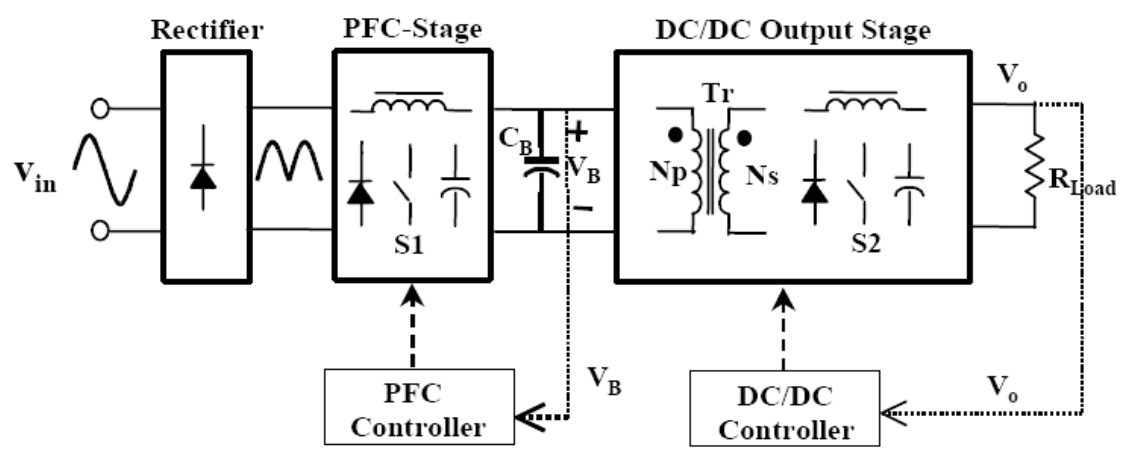
Figure 1.4 General structure of the two-stage PFC approach
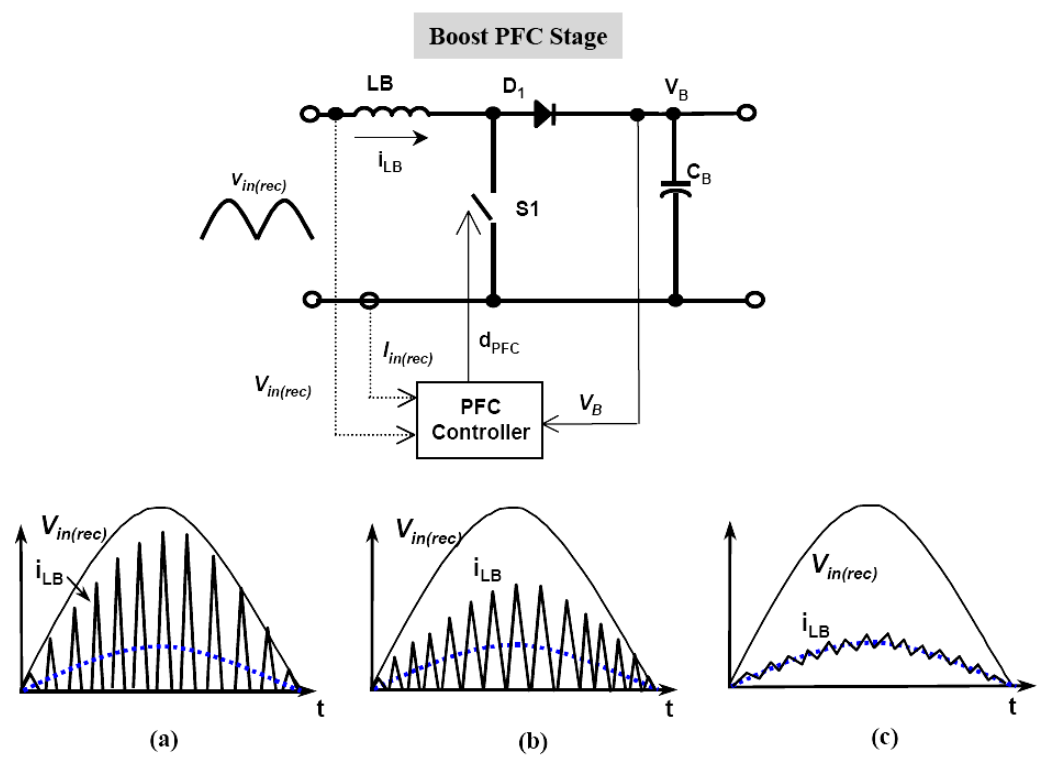
Figure 1.5 Typical boost PFC stage in different operations:

(a) DCM mode; (b) critical (boundary) mode; and (c) CCM mode

Figure 1.5 shows a typical boost PFC stage of the two-stage converter with different implementations. Figures 1.3(a)-(c) show that the boost inductor can be operated in several different conduction modes, such as discontinuous-conduction-mode (DCM), variable-frequency critical (boundary) conduction mode, and continuous-conduction-mode (CCM). In terms of control implementation, the DCM PFC approach requires the simplest control: the PFC switch is operated with a constant duty-cycle and fixed frequency during a half-line cycle, without sensing the input voltage or current. This provides a low-cost solution for low-power applications. The drawback of the DCM boost rectifier is its high input inductor current ripple, which causes high current stress on the semiconductor switch and requires a large electromagnetic-interference (EMI) filter.

To reduce the input current ripple, the critical mode PFC could be a good compromise with a slightly more complicated control, for input power of up to 500-600 W. In the critical mode PFC, the boost switch is operated with a variable switching frequency in a half-line cycle [7], which keeps the inductor operating at the boundary of DCM and CCM. The boost inductor current ripple has a peak value of twice that of the average input current. The variable frequency control also spreads the noise spectrum in the wide frequency range, which can further reduce the EMI filter size. However, the wide switching frequency range causes problems for design optimization and implementation [8]. Besides, the input current ripple is still large. To further reduce the current ripple and EMI filter size, the CCM PFC approach is widely adapted in the power range from hundreds of watts to several kilowatts. The CCM PFC performs well, but it requires complicated control implementation.

In summary, the active two-stage PFC converter has good input power factor and can be used in wide ranges of input voltage and output power. This technique is mature and the converter has good performance.

1.4 Active two-stage power factor correction technique application in AC-DC adapters

Currently most AC-DC adapters employ active two-stage PFC techniques. Figure 1.6 shows a typical two-stage topology used in AC-DC adapters.
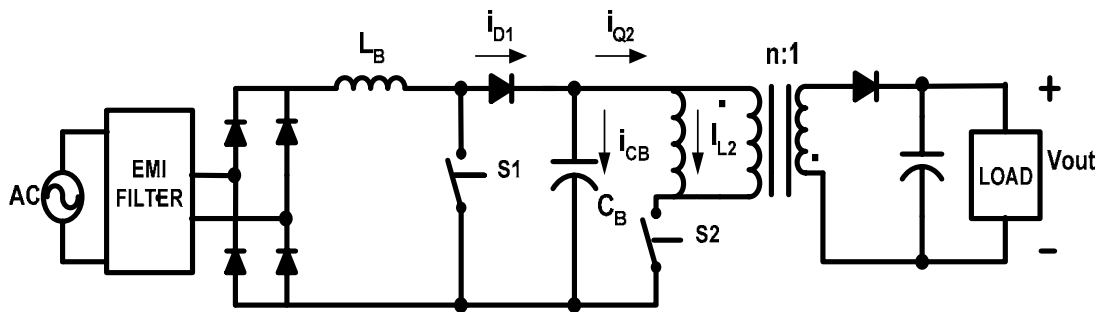
Figure 1.6 Schematic of the typical two-stage PFC circuit in AC-DC adapters

There are two tendencies in the market:

(i)   Reduce the cost by using a simple circuit like Single-stage PFC (S^{2}PFC) [9-11]

(ii)   Reduce the size and weight by means of novel techniques

In any AC/DC adapter, due to the fact that a low power level is obtained from the input when line voltage is near to 0 Volts, it is necessary to include an energy-storage element in order to feed the output during this interval. Moreover, in many computer-

related applications, additional energy must be stored because the power supply has to maintain its output voltage after a dropout of the line voltage during a time known as hold-up time. Consequently, a large DC-link capacitance is required with high energy storage capability. Moreover, the DC-link voltage is usually restricted to equal or more than 380 Volts interfacing a wide range line input voltage. For safe operation a capacitor with a voltage rating of at least 400V is necessary. It is well known that the capacitor size is increased both with the capacitance value and the rated voltage. The high voltage rating and high capacitance finally induce a large DC-link capacitor size. Furthermore, capacitor cost increases with the size increase. All of these factors make it become one of the decisive aspects for the cost and size of the AC/DC adapter. In usual notebook AC/DC adapters, the DC-link bulk capacitor captures nearly 1/5 of the whole volume.

Due to the large capacitance requirement, aluminum electrolytic capacitor is used in typical AC/DC adapters. Aluminum electrolytic capacitor is not an ideal capacitor and has a larger ESR. As we know, there is a ripple current in PFC converter caused by PWM control, which flows in and out of the output capacitor. Ripple Current in output capacitor will not only cause voltage ripple in DC output, but also results in heating of capacitor resulting from its ESR. It will further shortening expectancy of aluminum electrolytic capacitor and lower the system efficiency [12].

Proper synchronization of two power stages can significantly reduce the ripple current and ripple voltage of the DC-link capacitor, which allows the reduction of the DC-link capacitance [13, 14]. In addition, self-heating of the bulk capacitor will be reduced and its life will be extended.

The straightforward way to realize synchronization of the two power stages is employing Leading Edge Modulation (LEM) for PFC and Trailing Edge Modulation (TEM) for DC/DC converter. With this control scheme, switch of the first stage turns on and switch of the second stage turns off at the same instant, which minimizes the momentary no load period, thus lowering ripple current generated by the switching action.

1.5 Previous work

The synchronization scheme was introduced as a combo IC a few years ago and billed as the "industry's first leading edge/ trailing edge modulation scheme" PFC/PWM controller IC. Such ICs like UCC2851x family from TI [15] and ML4824-1/ ML4824-2 from Fairchild [16], employ leading edge modulation for the first PFC stage and trailing edge modulation for the second DC-DC PWM stage. In this way, both power stages can use only one single fixed clock and PFC stage turns on at the very same moment as the PFC starts to turn off, which is an out of phase synchronization in that sense. Experimental demonstration were already presented. However, no mathematical analysis is given yet to facilitate calculation of DC-link capacitor ripple current reduction. Furthermore, one of the limitations of leading/trailing edge modulation is that the switching frequencies of two stages need to be equal to achieve the best reduction of DC-link capacitor ripple current [15]. If the switching frequency of DC/DC converter is larger than the switching frequency of PFC pre-regulator, the DC-link capacitor ripple current will be larger than that under same switching frequency.

1.6 Research objective

The objective of this thesis is to investigate the synchronization of PFC pre-regulator and the DC-DC converter in AC-DC adapters. The pulse width modulation strategies employed to realize synchronization are studied. The synchronization Mathematical analysis in per-unit is presented to facilitate calculation of DC-link capacitor ripple current reduction with leading/trailing edge modulation strategies. A new leading/trailing modulation scheme is proposed in this thesis to further reduce the DC-link capacitor ripple current when PFC stage and DC-DC converter switch at different frequencies. This new PWM scheme is implemented by digital control based on FPGA.

1.7 Thesis outline

Chapter I of this thesis presents the basic review of power factor correction techniques. Passive power factor correction and active power factor correction techniques are introduced and compared. Major part of this chapter is devoted to an overall review of active two-stage power factor correction technique. Different conventional PFC control methods are also presented and discussed. The following part this chapter is the discussion of the application of active two-stage power factor correction in AC/DC adapters and its challenge and potential solutions. Finally, current techniques devoted to solve such problems for AC/DC adapter and the research objectives of this thesis are given.

Chapter II focuses on the description of current pulse width modulation schemes for synchronizing the PFC stage and DC/DC converter stage. Basic introduction of mechanisms of three different pulse width modulation methods is presented. Current

leading/trailing edge modulation scheme is introduced and its benefits are analyzed. To compare the traditional trailing edge modulation and the leading/trailing edge modulation and their effect to the dc-link capacitor ripple current, mathematical analysis is presented, which also provided the theoretical proof for the reduction of dc-link capacitor ripple current by using the leading/trailing edge modulation. Finally, a design example in per-unit is given to implicitly explain the advantage of synchronization through leading/trailing edge PWM modulation.

Chapter III discusses the proposed new leading/trailing edge modulation scheme for synchronization to further reduce the dc-link capacitor ripple current and capacitor size when two power stages switch at different frequencies. A mathematical analysis is conducted to provide theoretical proof for the benefit of the proposed new PWM scheme and a comparison with the regular leading/trailing edge PWM scheme is also made. In the end of this chapter, the method to realize this proposed PWM scheme and the simulation results based on this method are presented.

Chapter IV presents the design and implementation of the proposed the PWM scheme for synchronization of two power stages of AC/DC adapters. The detailed digital controller design procedure is given. The remaining part of this chapter presents the experiment results obtained using digital control based on FPGA.

Chapter V concludes this thesis by presenting the general conclusion of this work.

CHAPTER II

SYNCHRONIZATION OF PFC STAGE AND DC-DC

CONVERTER

2.1 Introduction

In many instances the power supply system must interface to a wide range input voltage (90-270V) requiring the DC-bus voltage to be equal to or greater than 380VDC. For safe operation a capacitor with a voltage rating of at least 400V is necessary. Traditional cascaded power stages require large bulk capacitance values to store instant power difference and minimize peak to peak ripple voltage. Together these requirements result in a costly capacitor.

To understand why the bulk capacitor requirements are traditionally so stringent consider the circuit shown in Figure 2.1, a PFC power stage with resistive load. The bulk capacitor C_B must supply load current I_o when SW is on, storing energy in the boost inductor L_B. It must also "absorb" the peak current from L_B each time SW switches off. The result of these currents into and out of C_B is a large ripple voltage across it. It is this large current with steep wavefronts that place the high demand on C_B's bulk capacitance to minimize output ripple.
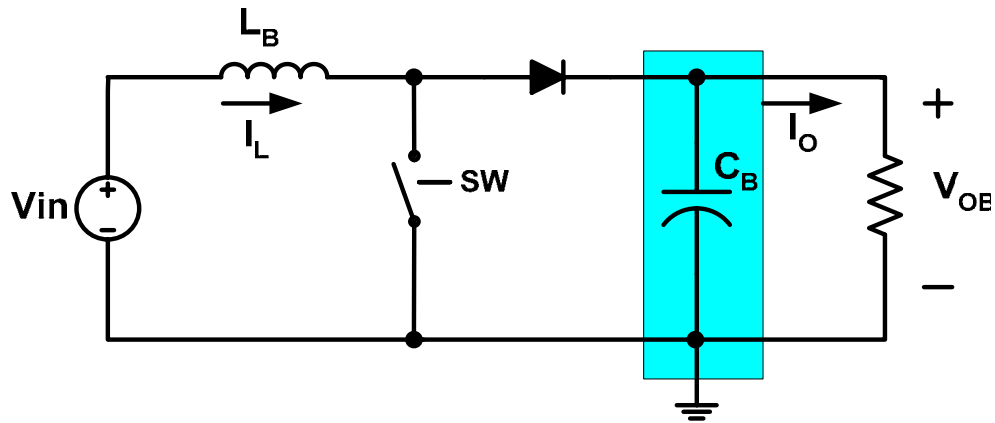
Figure 2.1 A single boost stage with a resistive load

Next, consider Figure 2.2, a two-stage PFC: a boost PFC stage followed by a PWM DC-DC stage (boost converter followed by Buck converter). To achieve unity power factor, the input power is the squared sine waveform while the output power is usually constant for most applications. Due to the fact that a low power level is obtained from the input when line voltage is near to 0 Volts, it is necessary to include an energy-storage element in order to feed the output during this interval. Moreover, in many computer-related applications, additional energy must be stored because the power supply has to maintain its output voltage after a dropout of the line voltage during a time known as hold-up time. Therefore, a large DC-link capacitor at the boost converter output side is required.
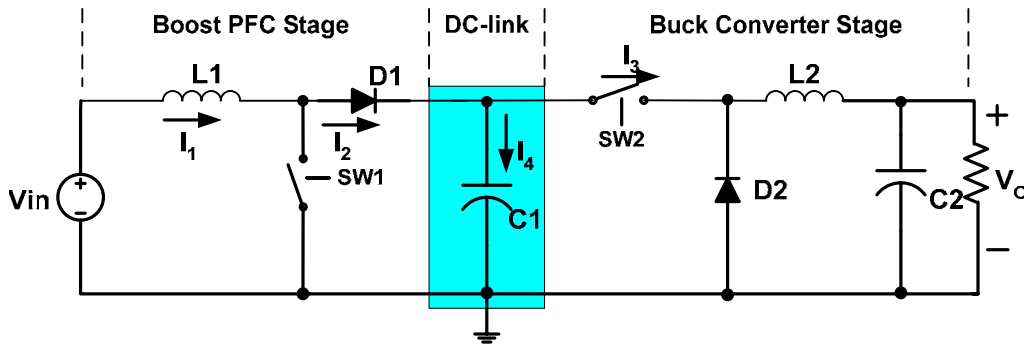
Figure 2.2 Cascaded power stages: boost converter followed by a buck converter

In this thesis, the terms "unsynchronized" and "synchronized" are used to describe the switching action of the two power switches operating from the same system clock. The switches are "synchronized" when one of them (SW2) turns on when the other (SW1) turns off. They are "unsynchronized" when both are switched on at the same time. Here SW1 and SW2 are switched on and off at the same time. The peak currents and therefore the ripple voltage are less than a PFC stage with a resistive load. Even further reductions are possible by "synchronizing" the two stages.

Synchronizing the two power stages can be realized through special pulse width modulation strategy, which will be introduced in the following sections.

2.2 Benefits of synchronization of two power stages

Synchronization of these two power stages was proved to significantly reduce the ac ripple current of the DC-link capacitor, which will induce less peak to peak DC-link output voltage ripple [12, 13]. In this situation, a smaller value of DC-link capacitor with less ESR can be used. Then the bulk capacitor self-heating can be significantly lowered, which will reduce the requirements for heat sinks and reduce their size. The capacitor life

can also be extended in this way. Less DC-link ripple current will reduce EMI noise and lower filtering requirements.

Moreover, the cost of capacitor is closely related to its size. For the same voltage rating, a smaller capacitance means a smaller size. Reducing the capacitor's size can significantly reduce its cost.

Furthermore, synchronization of the two power stages can also reduce the momentary no-load condition and push the trouble poles which are located near RHPZ (Right Half Plane Zero) of boost Converter further out in frequency, allowing unity gain crossover frequency to be placed at as high as one-half the line frequency. This renders a possibility of a faster control loop and a better system dynamic performance [16].

In summary, the following benefits of synchronizing two power stages were demonstrated.

(i)   Smaller DC-link capacitance and cost reduction

(ii) Noise reduction and stability [13]

(iii) DC-link capacitor's self-heating reduction

(iv) DC-link capacitor life extension [12]

2.3 Review of pulse width modulation techniques

2.3.1 Introduction

Pulse width Modulation is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal, which in actually is the control voltage from the error amplifier. The square wave pulse generated by Pulse Width Modulation will go through a gate driver and work as the gate control signal of the

switching transistors. The switching transistor is on more of the time for a high-amplitude

signal and off more of the time for a low-amplitude signal, thus controlling the amount of

power sent to a load and controlling the output voltage.

The simplest way to generate a PWM signal is the intersective method, which requires

only a sawtooth or a triangle waveform (easily generated using a simple oscillator) and a

comparator, which is depicted as Figure 2.3. When the value of the reference signal (the

green sine wave in Figure 2.4) is more than the modulation waveform (blue), the PWM

signal (magenta) is in the high state, otherwise it is in the low state.
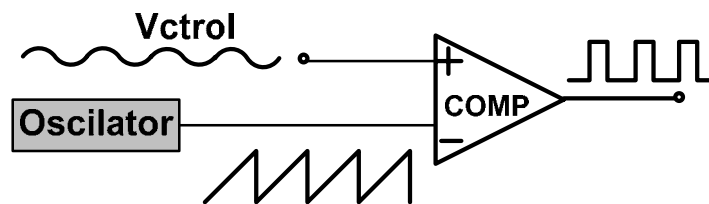
Figure 2.3 Circuit of typical pulse width modulator
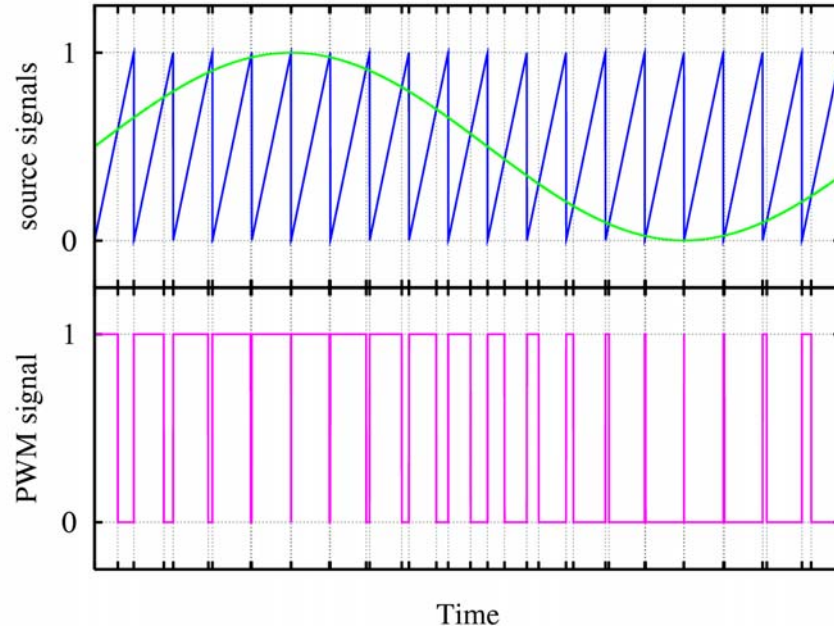
Figure 2.4 A simple method to generate the PWM pulse train corresponding to a

given signal

There are three types of pulse-width modulation (PWM) usually employed in the controller ICs (see Figure 2.5).

1. Trailing Edge Modulation: the leading edge can be held at the lead edge of the window and the tailing edge modulated.

2. Leading Edge Modulation: the trailing edge can be fixed and the leading edge modulated.

3. Double Edge Modulation: the pulse center may be fixed in the center of the time window and both edges of the pulse moved to compress or expand the width.
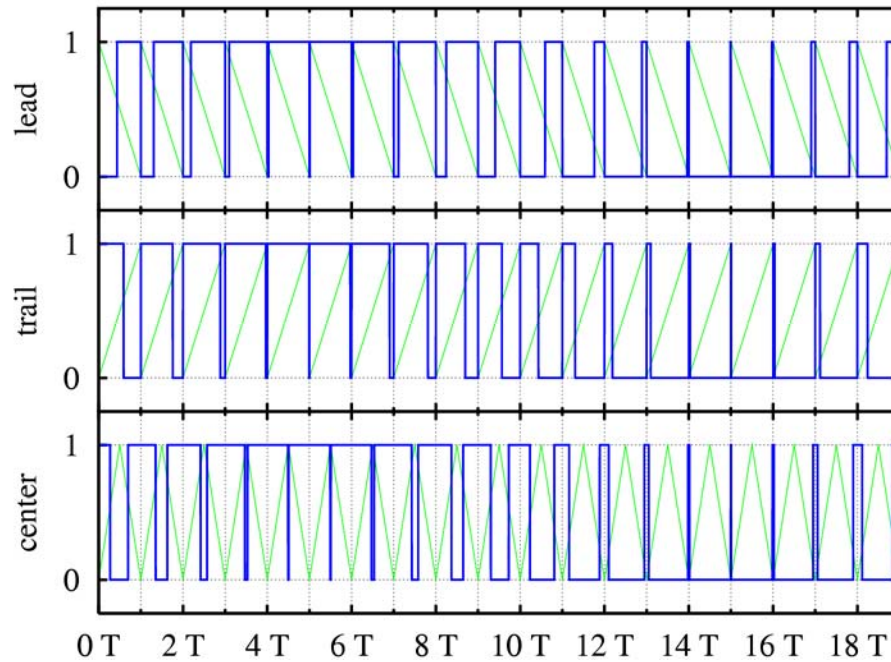
Figure 2.5 Three types of PWM signals

2.3.2 Trailing Edge Modulation

Conventional pulse width modulation (PWM) employs Trailing Edge Modulation (TEM) in which the switch will turn on right after the trailing edge of the system clock. Then the error amplifier output voltage is compared with the modulating ramp [16]. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 2.6 shows a typical trailing edge control scheme.
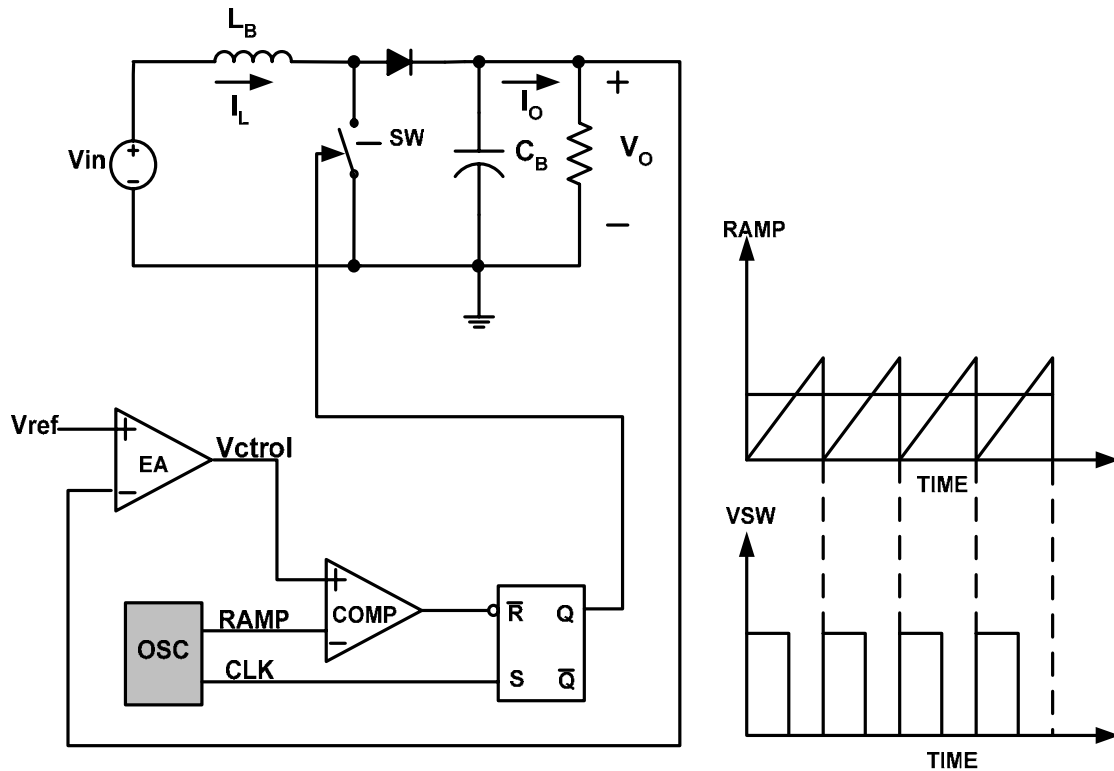
Figure 2.6 Trailing Edge Modulation control scheme

2.3.3 Leading Edge Modulation

In the case of Leading Edge Modulation (LEM), the switch is turned OFF right at the leading edge of the system clock; when the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch [16]. Figure 2.7 shows a leading edge control scheme.
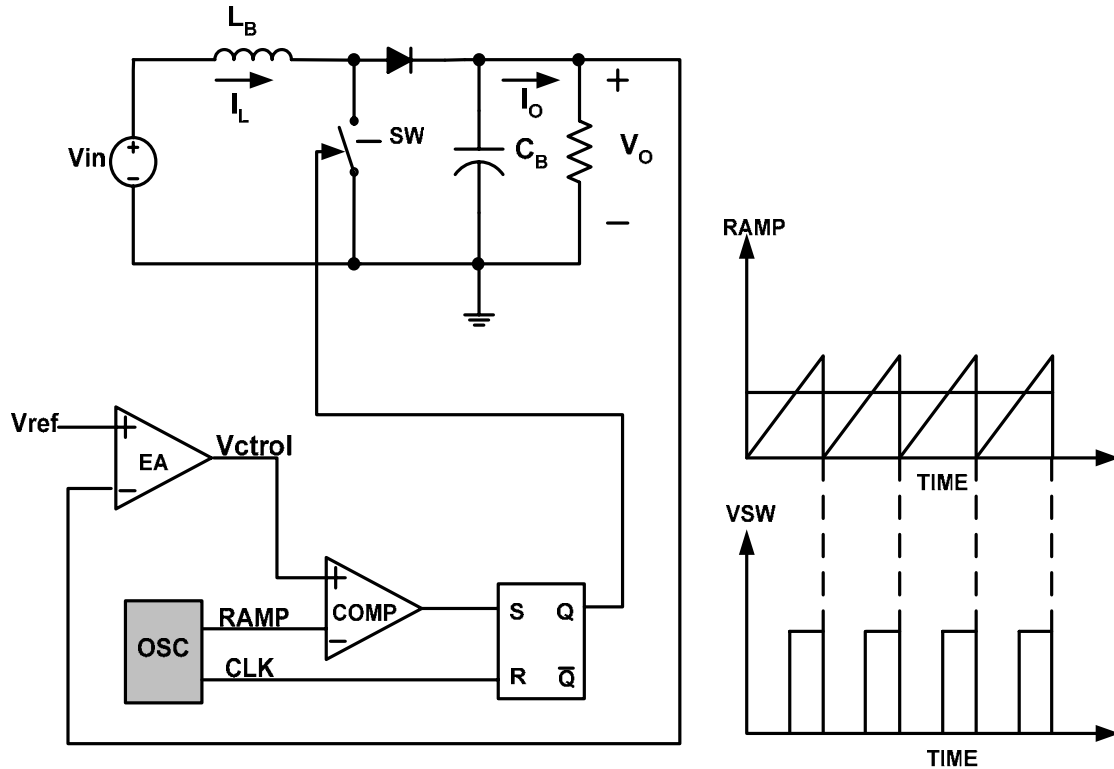
Figure 2.7 Leading Edge Modulation control scheme

2.4 Conventional Trailing Edge Modulation without synchronous switching

2.4.1 Introduction

In the conventional control scheme for cascaded power stages, both converters employ trailing edge modulation and turn on at the same instant under the same system clock. Figure 2.8 helps highlight switching actions of the two switches in one switching periods Ts. The DC-link capacitor will have its highest ripple current. This is because while both switches are ON, all the line current being shunted to ground while the DC/DC converter is pulling its current out of the boost output capacitor [14]. Discharging the boost output capacitor then will cause boost output voltage drop and induce higher

peak to peak voltage ripple. A simplified power stage shown in Figure 2.9 helps illustrate the current flowing paths under Trailing/Trailing edge modulation control scheme.
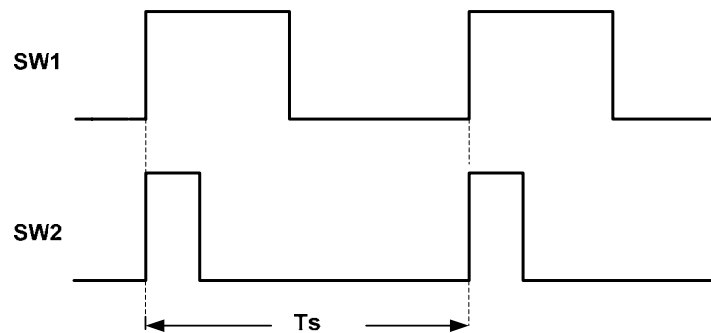
Figure 2.8 Switching actions of two switches under TEM/TEM control scheme
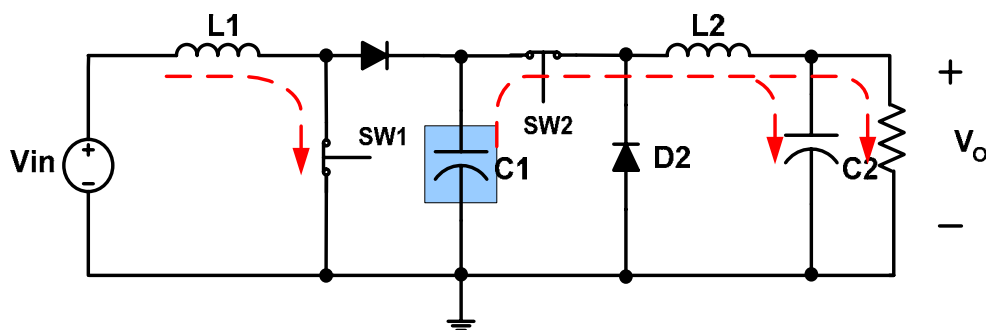
Figure 2.9 Current flowing paths for TEM/TEM

Moreover, Traditional trailing edge modulation results in a momentary no-load condition when the buck switch is turned off. This condition makes loop compensation difficult as it results in 2 poles located close to the RHPZ (Right Half Plane Zero) already in play because the boost inductor operates in continuous conduction current mode [17].

2.4.2 Mathematical analysis of DC-link capacitor ripple current under TEM/TEM

strategy

Mathematical analysis of DC-link ripple current with same switching frequencies for
two stages is given as following. We assume both stages are in the Continuous
Conduction Mode (CCM). That's because in the Critical Conduction Mode (CRM) case,
the capacitor current is a little more complex. Since the frequency is varying throughout
the line cycle, the overlap of diode current and downstream converter current is very
difficult to predict. The rms calculation for the CCM case is a good approximation since
the rms value is relatively insensitive to the higher turn-off slope [18]. If a more exact
answer is desired, simulation or measurement is the best approach.

The circuit schematic of the two-stage PFC circuit employed in usual AC-DC
adapters is given as Figure 2.10. The first stage is the boost PFC pre-regulator and the
second stage is the flyback converter which steps down the DC output voltage of first
stage and also provides isolation from the high input voltage source. Since the output DC
voltage of boost PFC stage is regulated at 380~400 V to guarantee the boost converter
work for a wide input line voltage and the flyback converter output voltage is usually
stepped down to a low level like 19V or 12V, the duty cycle of flyback converter will as
low as 0.2. Furthermore, we assume I_{L2}, duty cycle of SW2, D_2, to be constant for all
practical purposes. And also the diode current i_{ac} can also be assumed to be constant in a
very short period. Figure 2.11 illustrates the switching action and capacitor current during
one duty cycle. Although the duty cycle of the boost PFC stage D1 varies with the input

line voltage, the calculation according to the relationship of the switching pulses of the two power stage can still give us a good approximation.
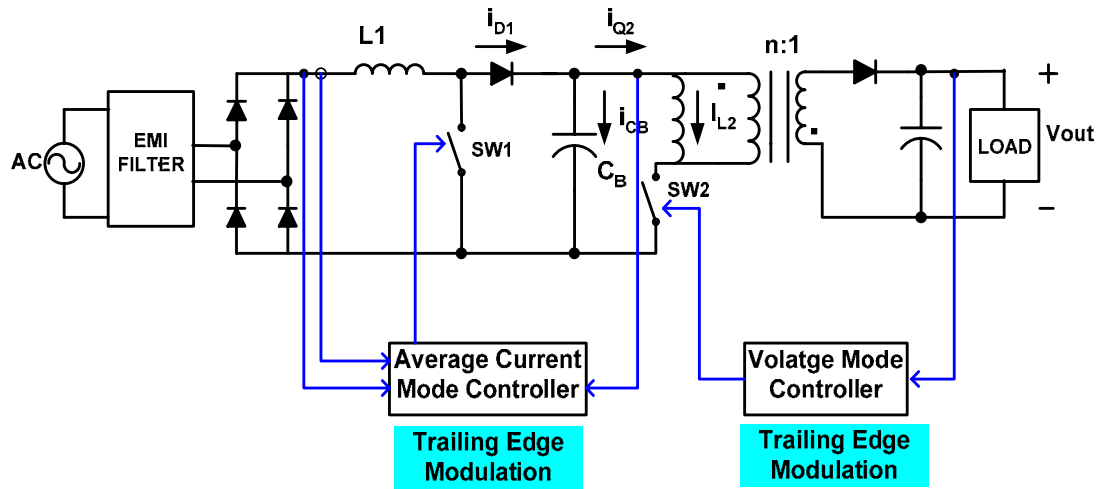
Fig 2.10 Schematic of the two stage PFC under analysis
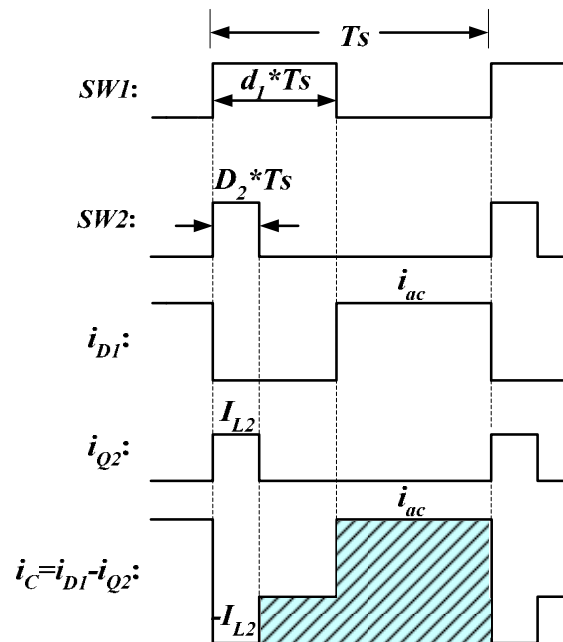
Fig 2.11 Capacitor ripple current for conventional TEM/TEM control scheme in one switching period

For the boost converter, the average square value of the boost output capacitor current $i_c^2(t)$ over one switching period is,

$$
\begin{aligned}
<i_c^2>_{T_s} &= \frac{1}{T_s} \int_t^{t+T_s} i_c^2(t)dt \\
&= I_{L2}^2 D_2 + i_{ac}^2(t)d_1(t)
\end{aligned}
\tag{2-1}
$$

where T_s is the switching period and $i_{ac}(t)$ is the instant input AC current.

If the rectified input voltage is given by

$$
v_{ac}(t) = V_M \left| \sin \omega t \right|
\tag{2-2}
$$

the input current is

$$
i_{ac}(t) = \sqrt{2} I_{ac\_rms} \left| \sin \omega t \right|
\tag{2-3}
$$

With a constant boost output voltage V_B, the transistor SW1 duty cycle must obey the relationship

$$
\frac{V_B}{V_{ac}(t)} = \frac{1}{1-d_1(t)}
\tag{2-4}
$$

This assumes that the converter dynamics are fast compared to the ac line frequency. Substitution of Eq. (2-2) into (2-4) and solution for d1(t) is,

$$
d_1(t) = 1 - \frac{V_M \left| \sin \omega t \right|}{V_B}
\tag{2-5}
$$

Substitution of (2-3) and (2-5) into (2-1) yields the following expression

$$
<i_c^2>_{T_s} = I_{L2}^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \omega t (1 - \frac{V_M}{V_B} \left| \sin \omega t \right|)
\tag{2-6}
$$

Then the RMS value of the ripple current of bulk capacitor will be,

$$I_{Crms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} < i_c^2 >_{T_s} dt} \qquad (2\text{-}7)$$

$$= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} [I_{L2}^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \omega t (1 - \frac{V_M}{V_B}|\sin \omega t|)]dt}$$

which can be further simplified to

$$I_{Crms} = \sqrt{\frac{2}{T_{ac}} \int_0^{T_{ac}/2} [I_{L2}^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \omega t (1 - \frac{V_M}{V_B}|\sin \omega t|)]dt}$$

$$= \sqrt{\frac{1}{\pi} \int_0^{\pi} [I_{L2}^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \theta (1 - \frac{V_M}{V_B}|\sin \theta|)]d\theta} \qquad (2\text{-}8)$$

$$= \sqrt{I_{L2}^2 D_2 + I_{ac\_rms}^2 - \frac{8}{3\pi} I_{ac\_rms}^2 \frac{V_M}{V_B}}$$

For the flyback converter, the input current has the following relationship with the output current.

$$I_{L2} = \frac{1}{1-D_2} \cdot \frac{1}{n} \cdot I_{out} = \frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}} \qquad (2\text{-}9)$$

where n is turn ratio of flyback transformer and I_{out}, V_{out}, P_{out} are the output DC current, DC voltage and output power of flyback converter.

By substitution of (2-9) into (2-8), we will obtain the final RMS value of the ripple current of the TEM/TEM scheme as following.

$$I_{Crms} = \sqrt{(\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}})^2 D_2 + I_{ac\_rms}^2 - \frac{8}{3\pi} I_{ac\_rms}^2 \frac{V_M}{V_B}} \qquad (2\text{-}10)$$

2.5 Synchronous switching with Leading/Trailing Edge Modulation

2.5.1 Introduction

The synchronization scheme was introduced as a PFC/PWM combo controller IC a few years ago, in which synchronization is achieved through implementing leading edge

modulation of the PFC stage and trailing edge modulation of the DC-DC converter stage.

Figure 2.12 shows the diagram of Texas Instruments' UCC 2851x PFC/PWM combo

controller IC controlled boost PFC and flyback converter system [15].
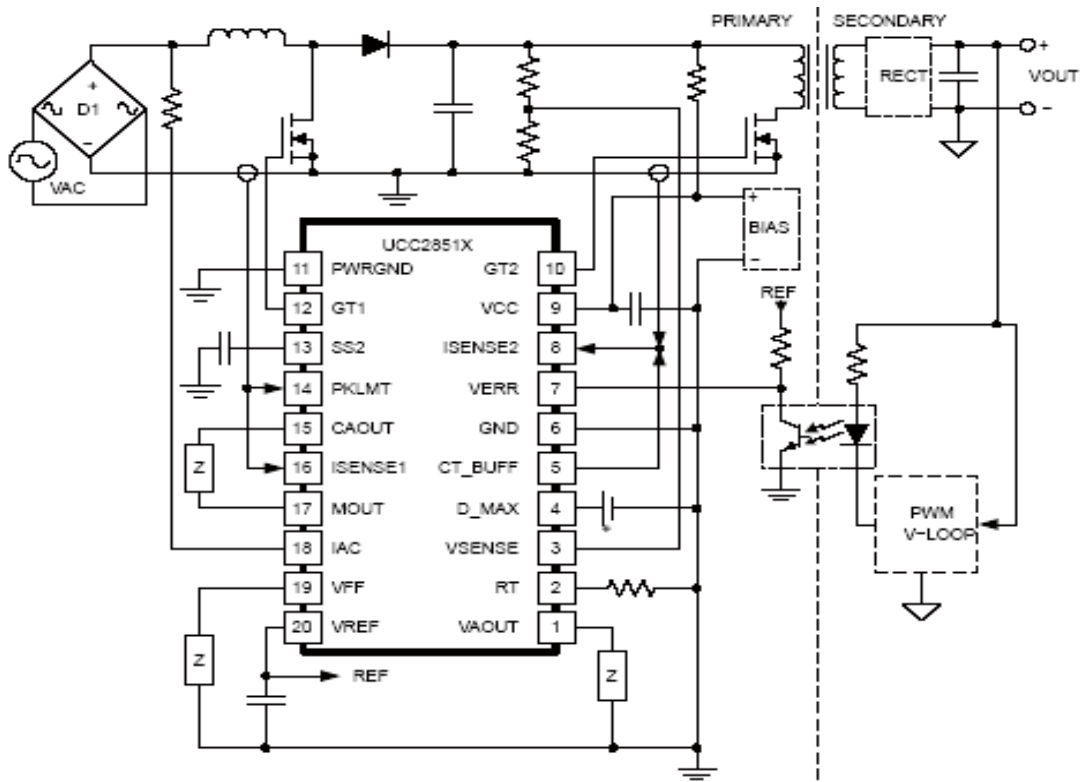
Figure 2.12 Diagram of TI UCC2851x controlled boost PFC and flyback converter

system

With Leading/Trailing Edge Modulation, DC-DC converter switch SW2 turns on at

the very some moment as PFC switch SW1 turns off. This is an out-of-phase

synchronization in that sense. In this way, we could expect that the freewheeling current

(coming out of the PFC diode) would head straight into the DC-DC converter stage

without having to recycling through the bulk capacitor, thus the bulk capacitor ripple

current can be significantly reduced. Figure 2.13 helps highlight switching actions of the

two switches in one switching period Ts. A simplified power stage shown in Figure 2.14 helps illustrate current flowing paths under LEM/TEM synchronous switching.

Such combo IC has a single clock of fixed frequency, and whereas the PWM switch would turn on at the clock edge, the PFC would switch off at the same edge.
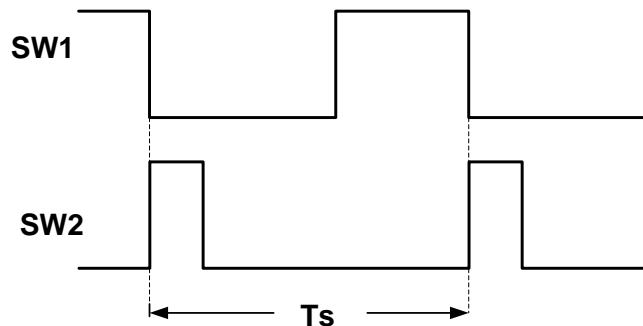
Figure 2.13 Switching actions of two switches in one switching period
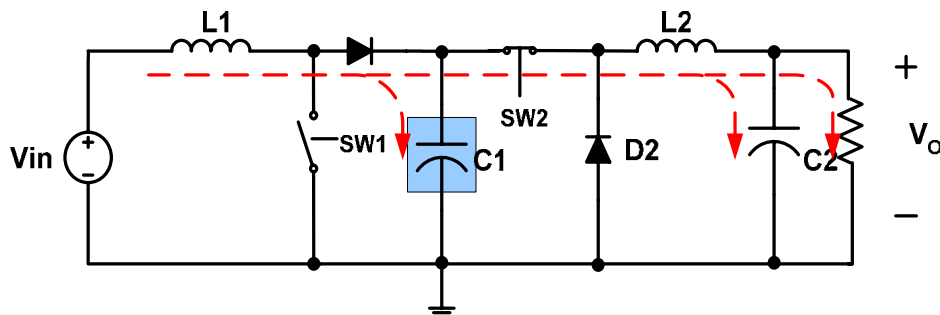
Fig 2.14 Current flowing paths for LEM/TEM control scheme

The best reduction of DC-link capacitor ripple current is achieved while the two stages switch at the same frequency. When the switching frequency of DC-DC converter is twice the switching frequency of PFC pre-regulator, there will be more overlaps of their on-time periods and the ripple current of boost capacitor will become larger than same switching frequency synchronization [15].

Synchronous switching techniques employing Leading Edge Modulation for PFC stage and Trailing Edge Modulation for DC-DC converter stage can also push the two troublesome poles near RHPZ caused by momentary no-load condition further out in frequency, allowing unity gain crossover frequency to be placed at as high as one-half the line frequency [16].

2.5.2 Mathematical analysis of DC-link capacitor ripple current under LEM/TEM strategy

To implicitly explain why Leading/Trailing edge modulation has the advantage of reducing dc-link capacitor ripple current, mathematical analysis is given as following. The power stage under analysis is shown as Figure 2.15. I_{L2} and duty cycle of SW2, $D_{2,}$ is assumed to be constant for all practical purposes. Figure 2.16 helps illustrate the switching actions and dc-link capacitor ripple current in one switching period.
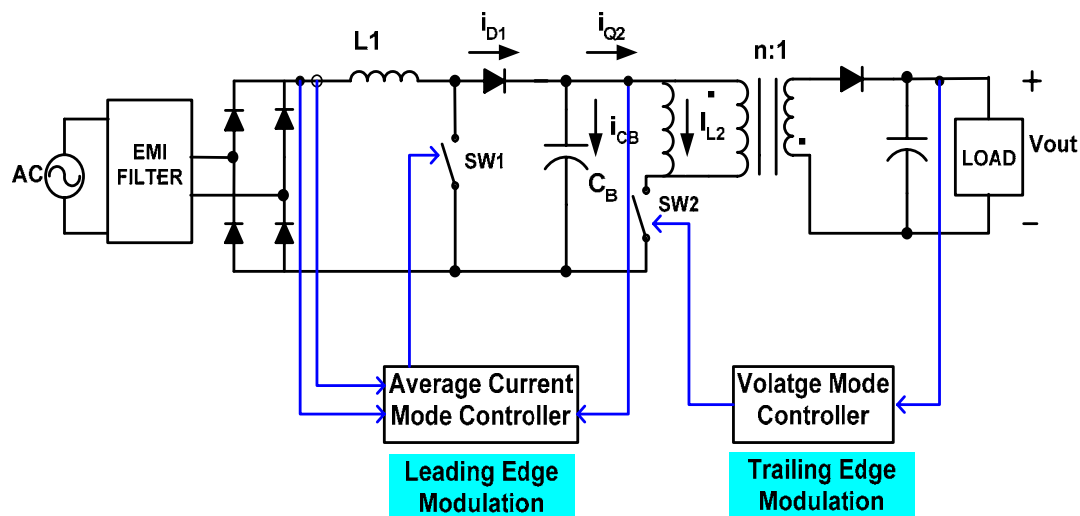
Figure 2.15 Schematic of the two-stage PFC under analysis
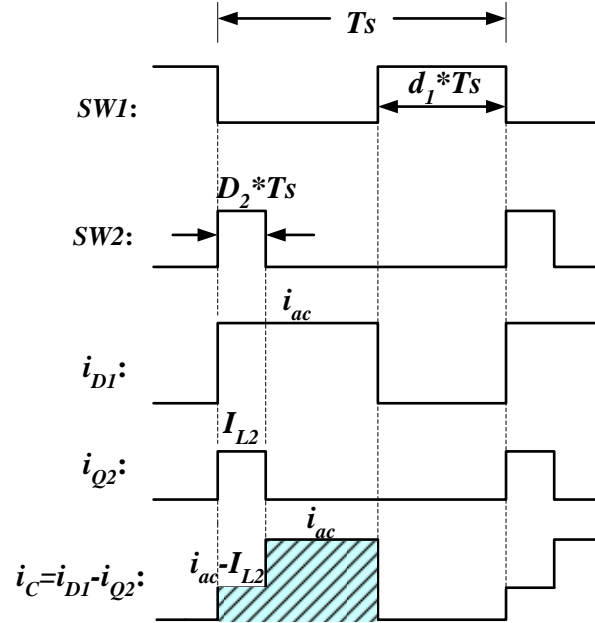
Figure 2.16 Capacitor ripple current for LEM/TEM control scheme in one switching period

The average value of $i_c^2(t)$ over one switching period can be derived as

$$<i_c^2>_{T_s} = \frac{1}{T_s}\{[i_{ac}(t) - I_{L2}]^2 t_{on2} + i_{ac}(t)^2(t_{on1} - t_{on2})\}$$
$$= i_{ac}(t)^2 d_1(t) + I_{L2}^2 D_2 - 2i_{ac}(t)I_{L2}D_2$$

(2-11)

where, t_{on1} is the on-time of SW1 and t_{on2} is the on-time of Q2.

If the rectified input voltage is given by

$$v_{ac}(t) = V_M |\sin \omega t|$$

(2-12)

the input current is

$$i_{ac}(t) = \sqrt{2}I_{ac\_rms} |\sin \omega t|$$

(2-13)

With a constant boost output voltage V_B, the transistor SW1 duty cycle must obey the relationship,

$$\frac{V_B}{V_{ac}(t)} = \frac{1}{1-d_1(t)} \tag{2-14}$$

This assumes that the converter dynamics are fast compared to the ac line frequency. Substitution of Eq. (2-12) into (2-14) and solution for

$$d_1(t) = 1 - \frac{V_M |\sin \omega t|}{V_B} \tag{2-15}$$

Substitution of equations (2-9), (2-13) and (2-15) into (2-11) yields the equation as below:

$$<i_c^2>_{T_s} = (\frac{1}{n(1-D_2)}\frac{P_{out}}{V_{out}})^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \omega t(1-\frac{V_M}{V_B}|\sin \omega t|) - 2\sqrt{2}I_{ac\_rms}\sin \omega t(\frac{1}{n(1-D_2)}\frac{P_{out}}{V_{out}})D_2$$

$$\tag{2-16}$$

Then the RMS value of ripple current of boost output capacitor with LEM/TEM synchronization will be,

$$I_{Crms} = \sqrt{\frac{1}{\pi}\int_0^\pi [(\frac{1}{n(1-D_2)}\frac{P_{out}}{V_{out}})^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \theta(1-\frac{V_M}{V_B}|\sin \theta|) - 2\sqrt{2}I_{ac\_rms}\sin \theta(\frac{1}{n(1-D_2)}\frac{P_{out}}{V_{out}})D_2]d\theta}$$

$$= \sqrt{(\frac{1}{n(1-D_2)}\frac{P_{out}}{V_{out}})^2 D_2 + I_{ac\_rms}^2 - \frac{8}{3\pi}I_{ac\_rms}^2\frac{V_M}{V_B} - \frac{4\sqrt{2}}{\pi}I_{ac\_rms}\cdot\frac{D_2}{n(1-D_2)}\frac{P_{out}}{V_{out}}}$$

$$\tag{2-17}$$

Comparing (2-10) and (2-17), we can see that RMS value of boost output capacitor ripple current will be smaller with LEM/TEM synchronization than without synchronization.

2.6 Design example

A 90W two-stage AC/DC adapter is analyzed mathematically in per unit quantities to present the advantages of synchronous Leading/Trailing Edge Modulation over conventional non-synchronous Trailing/Trailing Edge Modulation.

The base values selected for its parameters are as below.

$$P_{base} = 90 \ W \tag{2-18}$$

$$V_{base} = 120 \ V \tag{2-19}$$

$$I_{base} = \frac{P_{base}}{V_{base}} = 0.75 \ A \tag{2-20}$$

The specifications of the AC-DC adapter under study are listed in Table 2.1.

Table 2.1 Parameters of the AC-DC adapter under study

Parameters	Original Value	Value in per-unit
AC Line Voltage, V_{ac}	90Vac~270Vac	0.75 p.u.~ 2.2 p.u.
Output Power, P_{out}	90W	1 p.u.
DC- bus Voltage, V_B	380 V	3.17 p.u.
Turn Ratio of flyback Transformer, n:1	8:1	8:1

In Figure 2.17, we have plotted the DC-link capacitor ripple currents for 90Vac versus the DC-DC converter stage duty cycle. We can see that synchronization can significantly reduce the DC-link ripple current compared to non-synchronization.
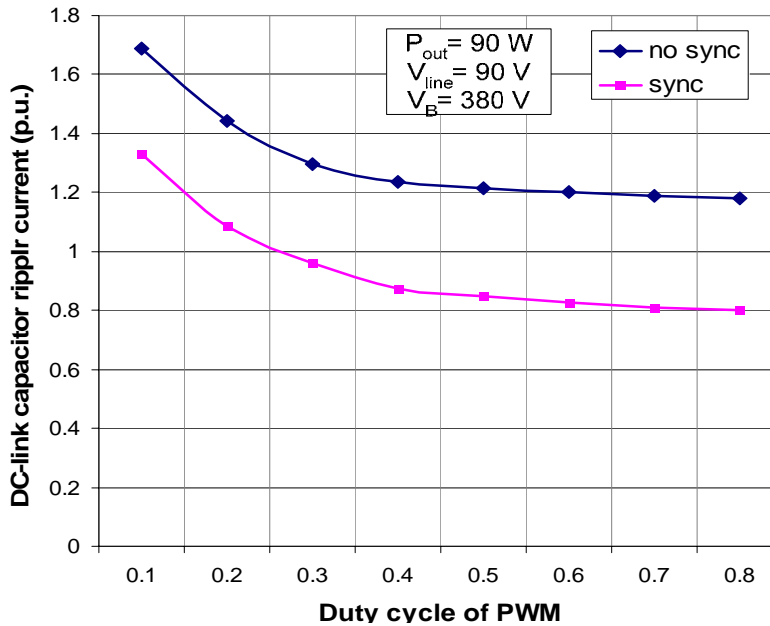
Figure 2.17 DC-link capacitor ripple current for 90Vac versus the duty cycle of the

PWM stage

For the 19V dc output, the duty cycle of the DC-DC converter stage is 0.286. The calculated rms values of DC-link capacitor ripple current under different input line voltages for LEM/TEM verses traditional TEM/TEM are summarized in Table 2.2.

Table 2.2 Effects of LEM/TEM vs. TEM/TEM on DC-link capacitor ripple current

	Vin=90Vac	Vin=150Vac	Vin=210Vac	Vin=270Vac
TEM/TEM	1.27 p.u.	0.83 p.u.	0.68 p.u.	0.57 p,u.
LEM/LEM	0.65 p.u.	0.48 p.u.	0.41 p.u.	0.39 p.u.
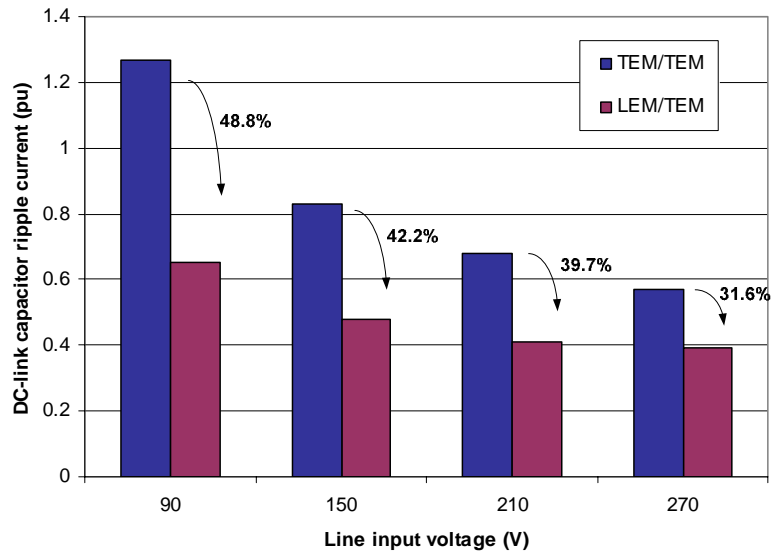
Figure 2.18 DC-link capacitor ripple current for LEM/TEM verses traditional

TEM/TEM under different line input voltages

Figure 2.18 illustrates that the DC-link capacitor ripple current can be reduce by about 50% at low line and about 30% at high line with the LEM/TEM synchronization scheme. The DC-link capacitance value can be significantly reduced if the ripple current is limited or the capacitor life can be increased as a result. In cost sensitive designs where hold-up time is not critical, this is a significant advantage.

CHAPTER III

PROPOSED LEADING/TRAILING EDGE MODULATION STRATEGY

3.1 Limitation of current Leading/Trailing Edge Modulation strategy

One of the limitations of current leading/trailing edge modulation strategy is that the switching frequencies of two stages need to be equal to achieve the best reduction of boost capacitor ripple current [12]. When the switching frequencies of the two power stages are different, for example f1:f2=1:2, the reduction of dc-link capacitor will be much less than the situation of f1:f2= 1:1. This is because when the two power stages switch at different frequencies; there will be more overlaps of their switches' turn-on time. In this situation, the second DC/DC converter stage will experience pulling current from the dc-link capacitor for more time, which causes larger peak to peak dc-link output voltage ripple and forces us to using a larger capacitance value than the same switching frequency situation to maintain a certain voltage ripple. Figure 3.1 helps illustrate this problem. The existence of this problem will block employing higher frequency for the isolated DC/DC converter to reduce its transformer size.
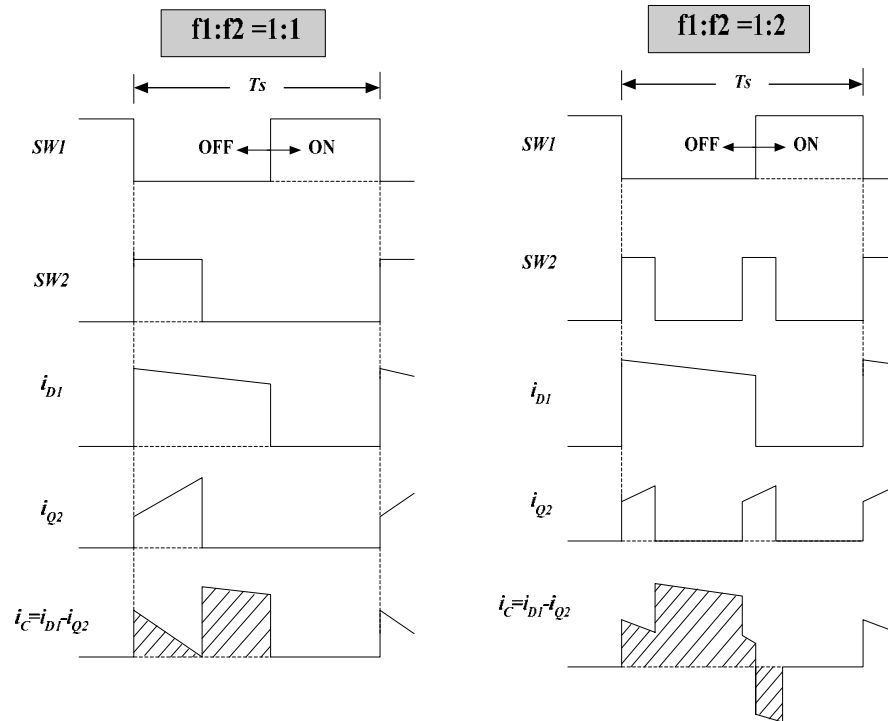
Figure 3.1 DC-link capacitor ripple current for f1:f2=1:1 vs. f1:f2=1:2

3.2 Proposed Leading/Trailing Edge Modulation strategy for 1:2 switching frequency

One solution for this problem encountered when two power stages switch at different frequencies is to employ a proper PWM modulation strategy which can effectively reduce the overlap of their turn-on time. Based on this, we propose a new Leading/Trailing Edge Modulation for the situation that the ratio of two stages' switching frequency is f1:f2=1:2 to further reduce the on-time overlaps and DC-link capacitor ripple current.

The proposed PWM strategy still employs Leading Edge Modulation (LEM) for boost PFC stage. But for the DC-DC converter stage, a nonlinear Trailing Edge Modulation is used to generate gating pulses. In this non-linear Trailing Edge Modulation, the two sequential narrow turn-on pulses are pulled closer to guarantee that

they can be located as much as possible at the OFF period of the boost PFC stage's switch. In this way, the overlaps of their ON periods will be effectively reduced and the DC-link capacitor ripple current will also become smaller. Figure 3.2 shows the comparison of the switching actions of two power stages under regular Leading/Trailing Edge Modulation strategy and under proposed strategy.

(a)

(b)
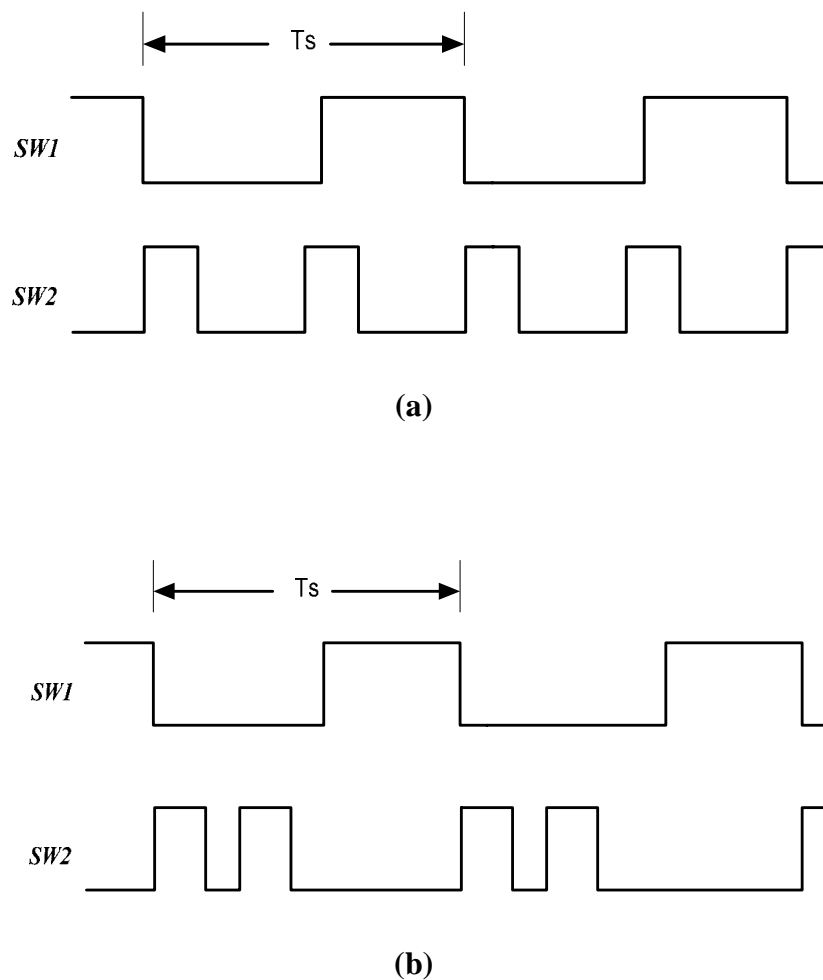
Figure 3.2 Switching actions of two power stages: (a) Using regular Leading/Trailing Edge Modulation strategy (b) Using proposed new Leading/Trailing Edge Modulation strategy

3.3 Mathematical analysis of the proposed Leading/Trailing Edge Modulation strategy

Figure 3.3 helps highlight the switching actions of the two stages and boost capacitor ripple current in one switching period when employing proposed PWM strategy, where Ts is the switching period of boost PFC and the switching period of DC-DC converter is Ts/2. In this analysis we still assume as I_{L2} duty cycle of SW2, D_2, to be constant for all practical purposes.
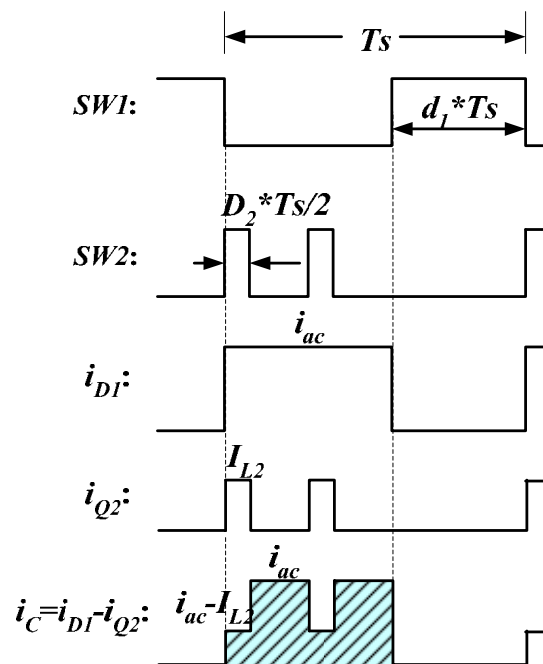
Figure 3.3 Switching actions and DC-link capacitor ripple current in one switching period under proposed PWM strategy

To demonstrate the advantages of the proposed scheme, the mathematical analysis of the boost capacitor ripple current is conducted as following.

The average of $i_c^2(t)$ over one switching period is

$$<i_c^2>_{T_s} = \frac{1}{T_s}\{[i_{ac}(t)-I_{L2}]^2 \cdot 2t_{on2} + i_{ac}(t)^2(t_{on1}-2t_{on2})\}$$

(3-1)

Since the switching frequency ratio of boost and flyback converters $f_1 : f_2 = 1:2$, the

duty cycle of flyback converter is

$$D_2 = \frac{2t_{on2}}{T_s}$$

(3-2)

Then, the average of $i_c^2(t)$ over one switching period is

$$<i_c^2>_{T_s} = i_{ac}(t)^2 d_1(t) + I_{L2}^2 D_2 - 2i_{ac}(t)I_{L2}D_2$$

(3-3)

If the rectified input voltage is given by

$$v_{ac}(t) = V_M |\sin \omega t|$$

(3-4)

the input current is

$$i_{ac}(t) = \sqrt{2}I_{ac\_rms} |\sin \omega t|$$

(3-5)

With a constant boost output voltage V_B, the transistor SW1 duty cycle must obey the

relationship

$$\frac{V_B}{V_{ac}(t)} = \frac{1}{1-d_1(t)}$$

(3-6)

This assumes that the converter dynamics are fast compared to the ac line frequency.

Substitution of Eq. (2) into (4) and solution for

$$d_1(t) = 1 - \frac{V_M |\sin \omega t|}{V_B}$$

(3-7)

For the flyback converter, the input current has the following relationship with the

output current.

$$I_{L2} = \frac{1}{1-D_2} \cdot \frac{1}{n} \cdot I_{out} = \frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}} \tag{3-8}$$

Substitution of equations (3-4), (3-7) and (3-8) into (3-3) yields the equation as below:

$$<i_c^2>_{T_s} = (\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}})^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \omega t (1 - \frac{V_M}{V_B} |\sin \omega t|) - 2\sqrt{2} I_{ac\_rms} \sin \omega t (\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}}) D_2$$

$$\tag{3-9}$$

Then the RMS value of ripple current of boost output capacitor with LEM/TEM synchronization will be

$$I_{Crms} = \sqrt{\frac{1}{\pi} \int_0^\pi [(\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}})^2 D_2 + 2I_{ac\_rms}^2 \sin^2 \theta (1 - \frac{V_M}{V_B} |\sin \theta|) - 2\sqrt{2} I_{ac\_rms} \sin \theta (\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}}) D_2] d\theta}$$

$$= \sqrt{(\frac{1}{n(1-D_2)} \frac{P_{out}}{V_{out}})^2 D_2 + I_{ac\_rms}^2 - \frac{8}{3\pi} I_{ac\_rms}^2 \frac{V_M}{V_B} - \frac{4\sqrt{2}}{\pi} I_{ac\_rms} \cdot \frac{D_2}{n(1-D_2)} \frac{P_{out}}{V_{out}}}$$

$$\tag{3-10}$$

We can see that this is the same approximation result as that obtained in the situation that two stages has the same switching frequency.

Therefore, with the proposed scheme, the DC-link capacitor ripple current with 1:2 switching frequencies can reach approximately very close to that of synchronization with 1:1 switching frequencies. That is to say, with the proposed PWM strategy, better reduction of DC-link capacitor ripple voltage and capacitor size will be achieved. In this way, using the proposed PWM strategy, a higher switching frequency can be employed for flyback converter while still maintaining a small DC-link voltage ripple and capacitor size.

3.4 Realization method of proposed PWM strategy

Figure 3.4 shows the two-stage AC/DC adapter system configuration. In this configuration, the PWM modulator of boost PFC stage employs regular Leading Edge Modulation while the DC-DC converter PWM modulator employs nonlinear Trailing Edge Modulation strategy to realize the proposed PWM scheme.
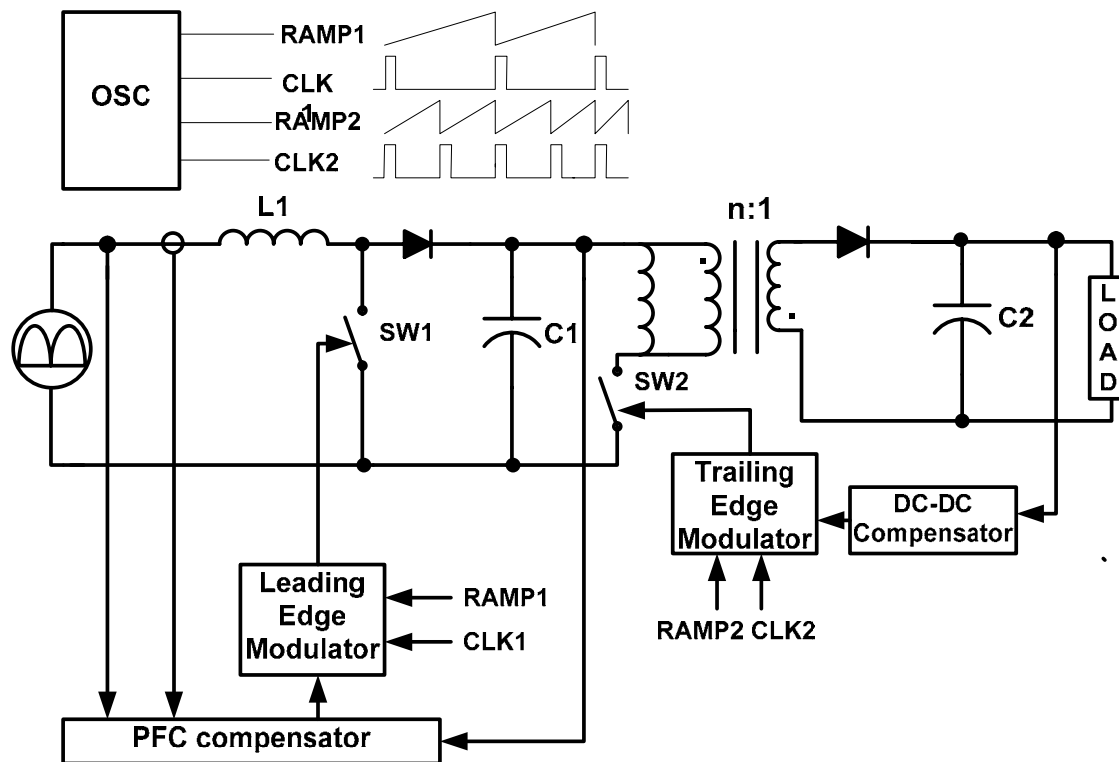
Figure 3.4 Two-stage AC/DC adapter system configuration using proposed PWM strategy

Figure 3.5 illustrates the proposed nonlinear Trailing Edge Modulator, in which the control voltage from the voltage compensator (which actually is the duty cycle D_2 if the ramp peak value is one) is divided by 2 before it is fed into the PWM comparator. The

pulse signal out of the comparator then goes to two parallel regular Trailing Edge Modulators. These two Trailing Edge Modulators will produce a PWM pulse whose width is actually $D_2T_s/2$. Through inserting a phase delay which is much less than the switching period of the DC-DC converter between these two PWM pulses and adding them together, we can get a PWM pulse series whose frequency is still f_{s2} and ON time during every two cycles is unchanged. In this way, the output voltage will not be affected while two sequent ON pulses can get much closer to be located as much as possible in the OFF period of the PWM pulse of PFC stage.
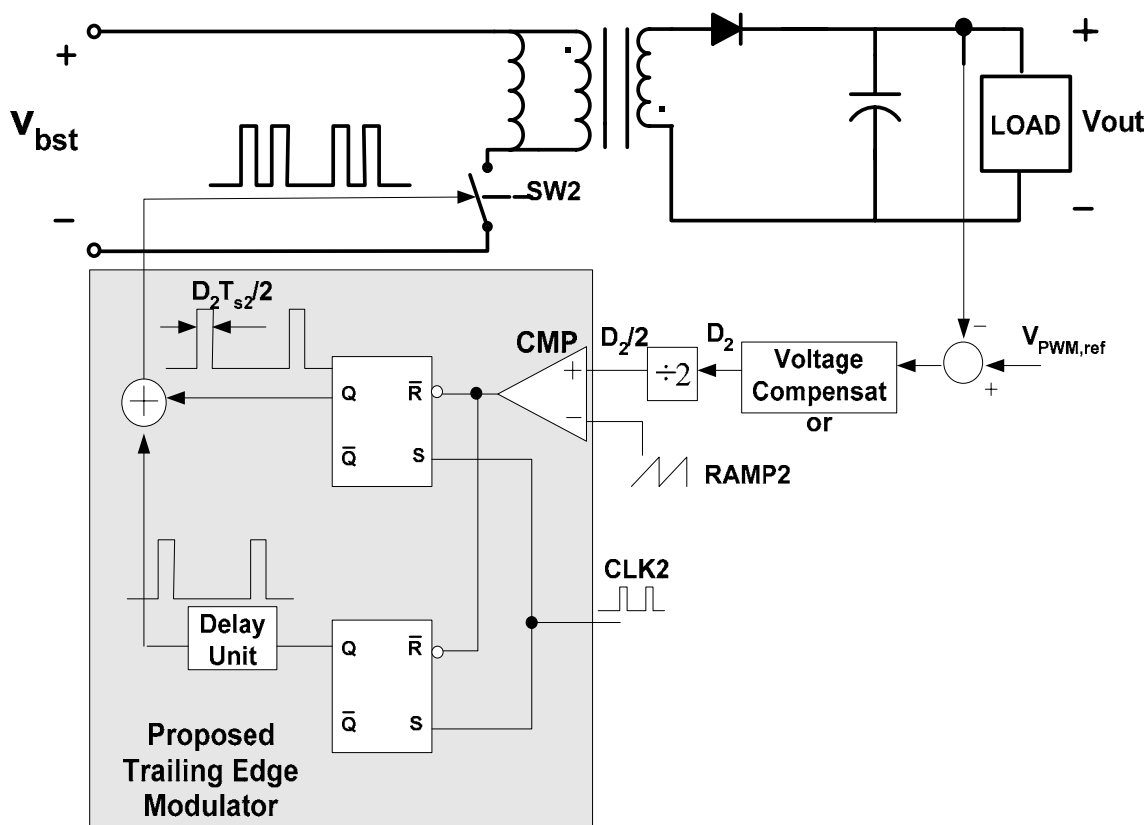
Figure 3.5 Proposed Trailing Edge Modulator for DC-DC converter stage

This proposed nonlinear Trailing Edge Modulation strategy can be easily implemented using digital control. Chapter IV will present the implementation of this proposed PWM strategy based on FPGA.

3.5 Simulation results

A two-stage AC/DC adapter employing proposed new Leading/Trailing Edge Modulation scheme is simulated in the software *Saber*. The DC-link capacitor using in the simulation is 30uF and other parameters are the same as those given in the beginning of this chapter. The boost PFC stage and flyback converter are controlled by the controllers designed above. The phase delay used in the proposed Trailing Edge Modulator is 1us. The simulation results are obtained with 110Vac line input voltage, 60Hz line frequency and 90W output power.

Figure 3.6 shows the simulated waveforms of gating signals of two switches and DC-link output voltage ripple using regular Leading/Trailing Edge Modulation scheme. Figure 3.7 shows the simulated waveforms of gating signals of two switches and DC-link output voltage ripple using proposed new Leading/Trailing Edge Modulation scheme.
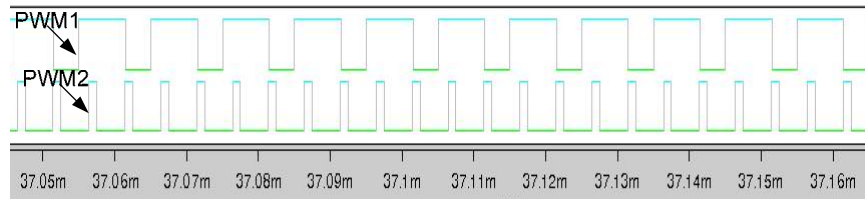
(a)
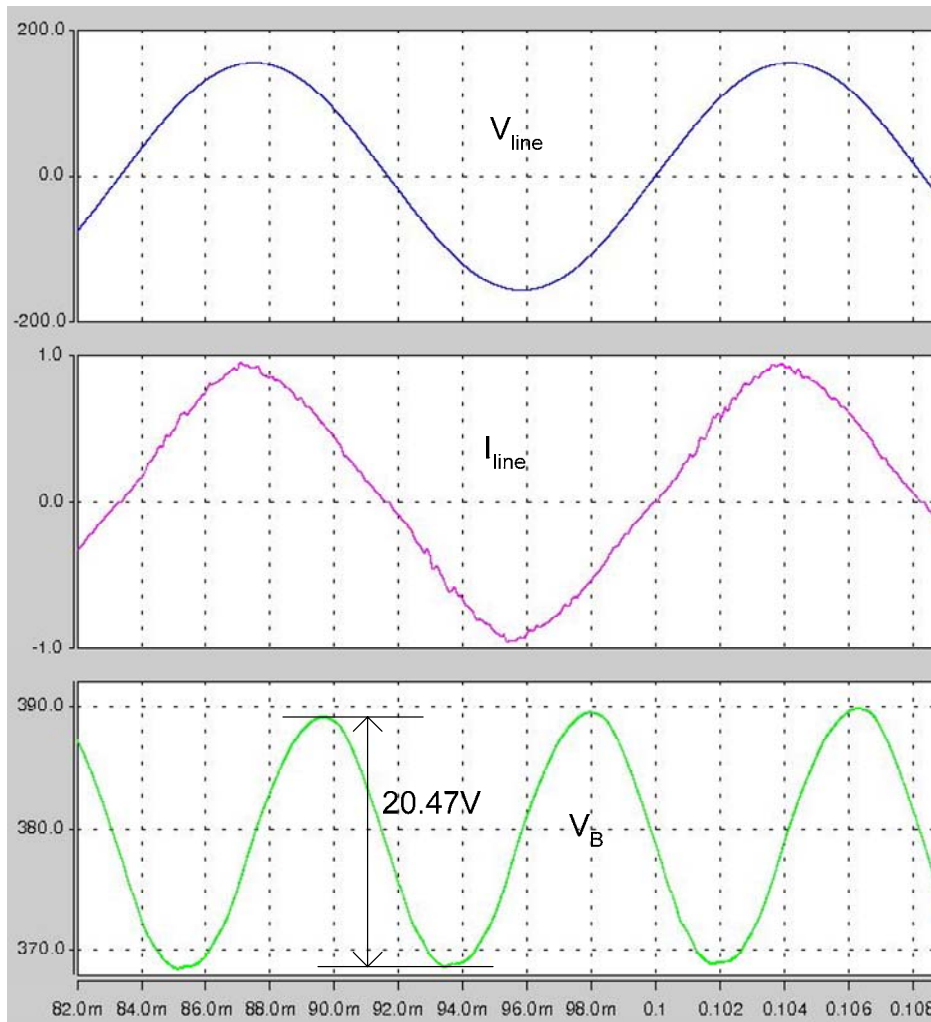
(b)

Figure 3.6 Simulated waveforms obtained using regular LEM/TEM: (a) Gating

signals of the two stages; (b) DC-link voltage, line voltage and line current
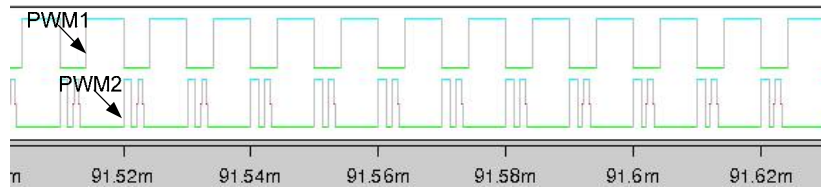
(a)
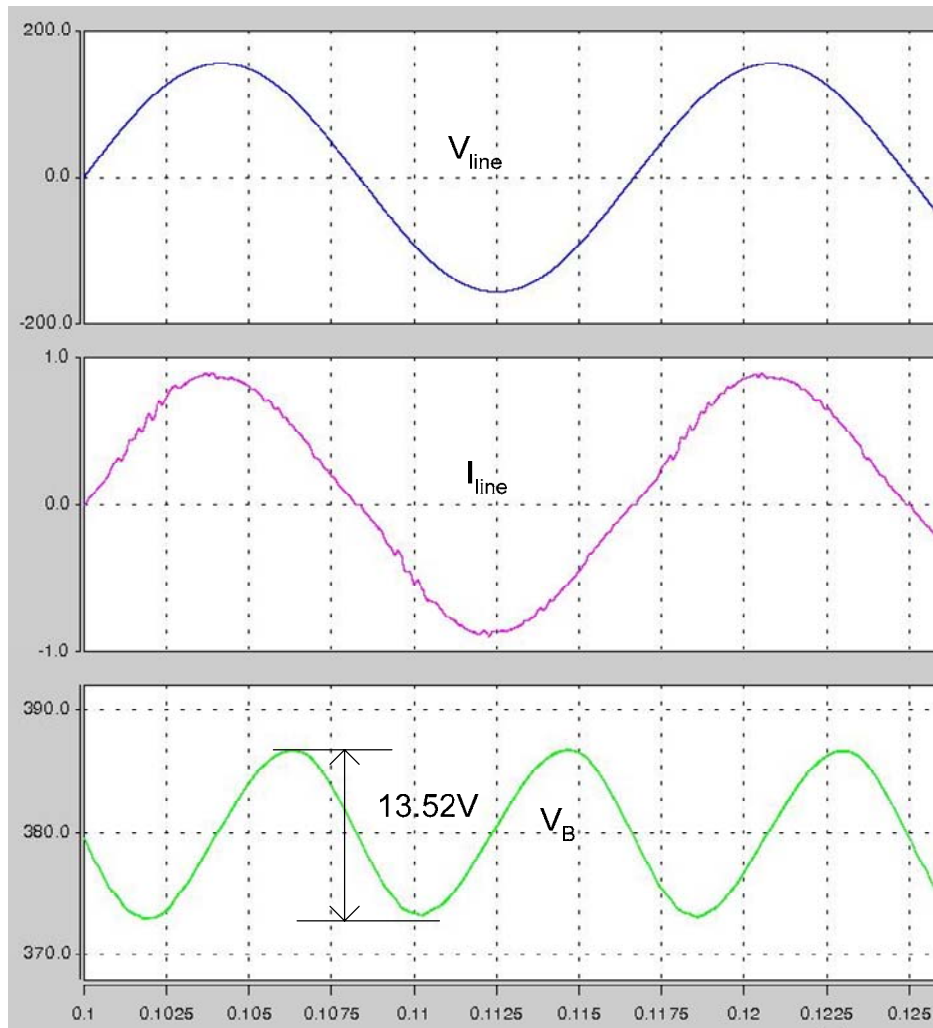
(b)

Figure 3.7 Simulated waveforms obtained using proposed LEM/TEM: (a) Gating

signals of the two stages; (b) DC-link voltage, line voltage and line current

Simulation results obtained show that using proposed PWM strategy for 1:2 switching can effectively reduce the DC-link voltage ripple without penalizing power factor. Consequently, a smaller DC-link capacitance can be used, allowing the size reduction of AC/DC adapters.

CHAPTER IV

IMPLEMENTATION OF A TWO-STAGE AC/DC ADAPTER USING

PROPOSED LEADING/TRAILING EDGE MODULATION STRATEGY

4.1 Digital control design for two-stage AC/DC adapter

4.1.1 Introduction

Although analog control is almost exclusively used in today's switching power supply, it can not meet requirement for today's power supplies. It has several disadvantages, such as large part count, low flexibility, low reliability and sensitive to the environmental influence such as thermal, aging and tolerance.

In addition, power converters are very complicated due to the nonlinear and time varying nature of switches, variation of parameters, fluctuations of input voltage and load current. Sometimes, it is difficult to get the accurate model of power converter system. In analog implementation, power converters are usually designed using linear models. Therefore, it is difficult to design the control algorithms with high performance by using the analog control method.

With the development of the DC power supply, attention began to be paid to digital control for PFC, DC/DC converters, and voltage regulation modules (VRMs). Compared with analog circuit, digital control system offers a numbers of advantages [19-23],

(1) Programmability

In digital control, all the control algorithms are realized by software. Therefore, the digital control system has high programmability. Different control algorithms can be easily implemented into the same hardware control system. When the design requirement

is changed, it is very easy and fast for digital controllers to change the corresponding software. The development time and cost will be greatly reduced.

(2) High Flexibility

Communication, protection, prevention and monitoring circuits could be easily built in the digital control system. Important operation data can be saved in the memory of digital control systems for diagnose. In addition, digital control system eases the ability to connect multiple controllers and power stages. The system integration becomes easier.

(3) Fewer components

In digital control system, fewer components are used compared with the analog circuit. Therefore, the digital control system is less susceptible to the environmental variations. Hence, digital control system has better reliability than analog circuits.

(4) Advanced control algorithms

Most importantly, it is much easier to implement the advanced control techniques into digital control system. Advanced control algorithms can greatly improve the dynamic performance of power converter system. These advanced control methods can be implemented easily using digital circuit, but not analog circuit. As a result, the system dynamic performance could be significantly improved.

Today, digital controllers are mostly implemented based on DSP. However, DSPs are not very common in high switching frequency or low cost applications. The main limitation of DSPs is their sequential operation, that is, instructions are executed one after the other.

In this thesis, we implement the proposed nonlinear Leading/Trailing Edge Modulation strategy based on an FPGA which allows concurrent operation (simultaneous

execution of all control procedures), enabling high performance and novel control methods [23].

Figure 4.1 shows the control structure of the digital controller for the two-stage AC/DC adapter under implementation, in which PFC stage employs average current mode control and flyback converter employs voltage mode control.
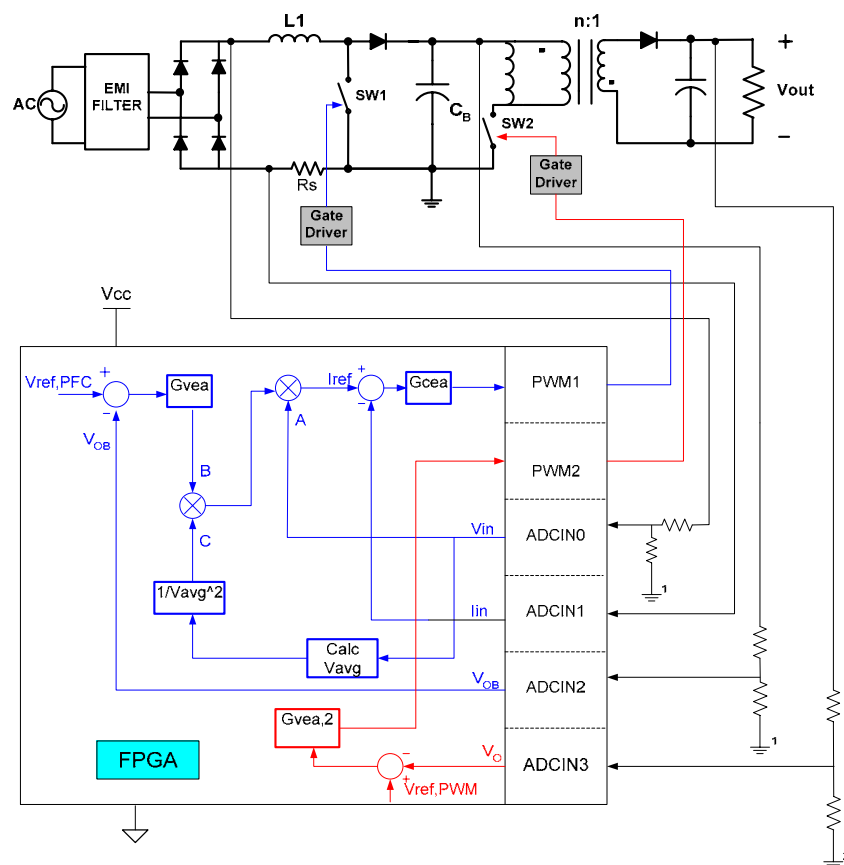
Figure 4.1 FPGA controlled two-stage AC/DC adapter

Parameters of the two-stage AC/DC adapter implemented in this thesis are:

1. Boost inductor: 400uH

2. DC-link capacitor: 120uF

3. Flyback transformer turn ratio: 8:1

4. Flyback transformer primary inductance: 220uH

5. Flyback output capacitor: 1000uF

System specifications are given as following:

1. Input voltage: 90~270 V, 50~60Hz

2. Boost PFC output voltage: 380V

3. Output power: 90W

4. Output voltage: 19V

5. Switching frequency: 100 kHz for boost PFC, 200 kHz for flyback converter

The sense gain parameters are:

1. Rectified input voltage sense gain: Kf = 1/410

2. Boost output voltage sense gain: Kd= 1/410

3. Input current sense gain: Ks= 0.2

4. Flyback output voltage sense gain: Ko=1/8

4.1.2 Digital control design for boost PFC stage

The first stage is an ac-dc boost PFC stage, which converts the ac input voltage to a high voltage dc bus and maintains sinusoidal input current at high input power factor. Figure 4.2 shows waveforms of input voltage, inductor current and output dc voltage of boost PFC stage. As indicated in Figure 4.1, three signals are required to implement the control algorithm. These are, the rectified input voltage Vin, the inductor current Iin, and the dc-link capacitor voltage V_{OB}. The converter has a three-loop control structure. The fast current loop keeps the input current the shape of the input voltage, which renders the unity PF [24]. The input voltage feed-forward loop is to compensate the input voltage

variation [24]. The voltage loop keeps the output voltage at 380V [24]. The voltage loop

is very slow to avoid introducing 2nd harmonic ripple into the current reference.

(a)

(b)
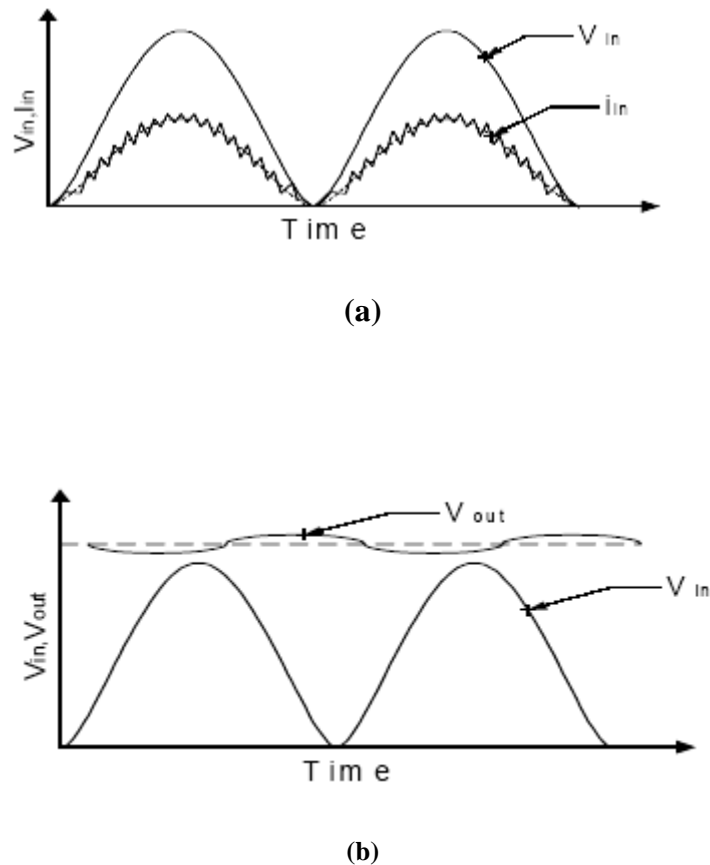
Figure 4.2 (a) Waveforms of input voltage and inductor current, (b) Waveforms of

input voltage and output voltage

The instantaneous signals Vin, Vo and Iin, are all sensed and conditioned by the

respective voltage and current sense circuits. The sensed signals are then fed back to the

FPGA via three ADC channels ADCIN0, ADCIN1, and ADCIN2 respectively. The rate

at which these signals are sensed and converted by the ADC is called the control loop

sampling frequency fs. The digitialized sensed bus voltage V_{OB} is compared to the

desired reference bus voltage Vref. The difference signal (Vref - Vo) is then fed into the

voltage loop controller Gvea. The digitized output of the controller Gvea, indicated as 'B', is multiplied by two other components, 'A' and 'C', to generate the reference current command for the inner current loop. The component 'C' is calculated as,

where, Vavg is the calculated average component of the sensed digitized signal Vin. In Fig 4.1, Iref is the reference current command for the inner current loop. Iref has the shape of a rectified sinewave and it's amplitude is such that it maintains the output dc voltage at a reference level Vref, against variation in load and fluctuation in line voltage. The sensed digitized inductor current Iin is compared with the reference current Iref. The difference between Iref and Iin is passed into the current controller Gca. The output of this controller is finally used to generate the PWM duty ratio command for the PFC switch.

There are two methods for designing a digital controller --direct digital design and digital redesign. Digital redesign is the simplest method to implement digital control. In this method, an analog controller is first designed in the continuous domain as if one were building continuous time control system, by ignoring the effects of sampling and hold associated with the AD converter and the digital PWM circuits. The analog controller is then converted to a discrete-time compensator by some approximate methods. There are many conversion methods, such as "backward integral," "Tustin" and "zero and pole matching [25]." Direct redesign is to design the digital controller in Z-domain employing the relation of z variable and s variable: where Ts is the sampling cycle. In this thesis, we use digital redesign method for digital controller design with "zero and pole matching" conversion.

Fig 4.3 shows the control loop block diagram of the boost PFC stage.

Figure 4.3 Control loop block diagram of the PFC stage

In this figure, the voltage and current sense/conditioning circuits are replaced by their respective gain blocks. These blocks are indicated as Kf, Ks, and Kd. The multiplier gain Km is also added to the control block. Km allows adjustments of the reference signal Iref based on the converter input operating voltage. The inner loop is the current loop, which is programmed by the reference current signal Iref. The input to the current loop power stage is the duty ratio command d and its output is the inductor current Iin. The current controller Gca is designed to generate the appropriate control output Uca such that the inductor current Iin follows the reference current Iref. The outer voltage loop is programmed by the reference voltage command Vref. The input to the voltage loop

power stage is Unv (voltage controller output) and its output is the dc bus voltage Vo. The voltage controller Gvea is designed to generate the appropriate Unv to control the amplitude of the reference current Iref such that for the applied load current and line voltage, the bus voltage Vo is maintained at the reference level. For this control implementation it is necessary to calculate these voltage and current controllers.

4.1.2.1 Current loop compensator design

The function of the current compensator is to force the current to track the current reference that is given by the multiplier and which has the same shape as the input voltage. So the current loop bandwidth must be higher than the reference bandwidth. For faithfully tracking a semi-sinusoidal waveform of 120 or 100Hz, the bandwidth of the current loop is usually set to 2-10 kHz [26].

Using the three terminal average models, a small-signal equivalent circuit of the current loop [25]is shown in Figure 4.4.
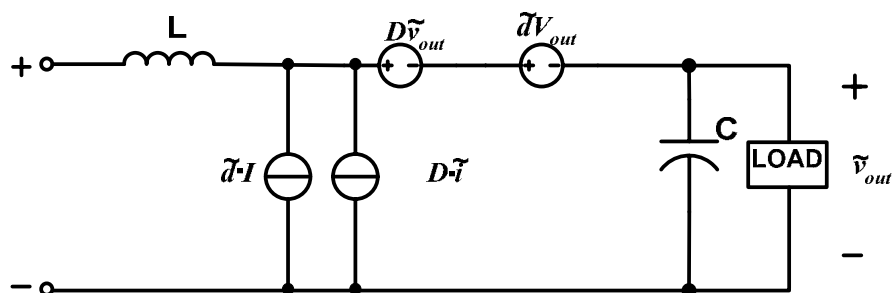
Figure 4.4 Small signal model of current loop

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} = \frac{2V_{out}}{R_L(1-D)^2} \cdot \frac{1 + \dfrac{sR_LC}{2}}{1 + \dfrac{sL}{R_L(1-D)^2} + \dfrac{s^2LC}{(1-D)^2}} \tag{4-1}$$

The high frequency approximation of the control to current transfer function can be derived as below,

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} = \frac{V_{out}}{sL} \tag{4-2}$$

Figure 4.5 shows Bode plot for duty-to-current transfer function for different input voltages and the high frequency approximation.

Figure 4.5 Bode plot for control-to-current transfer function

From the PFC control block diagram in Figure 4.3, the dc gain equation for the current loop is,

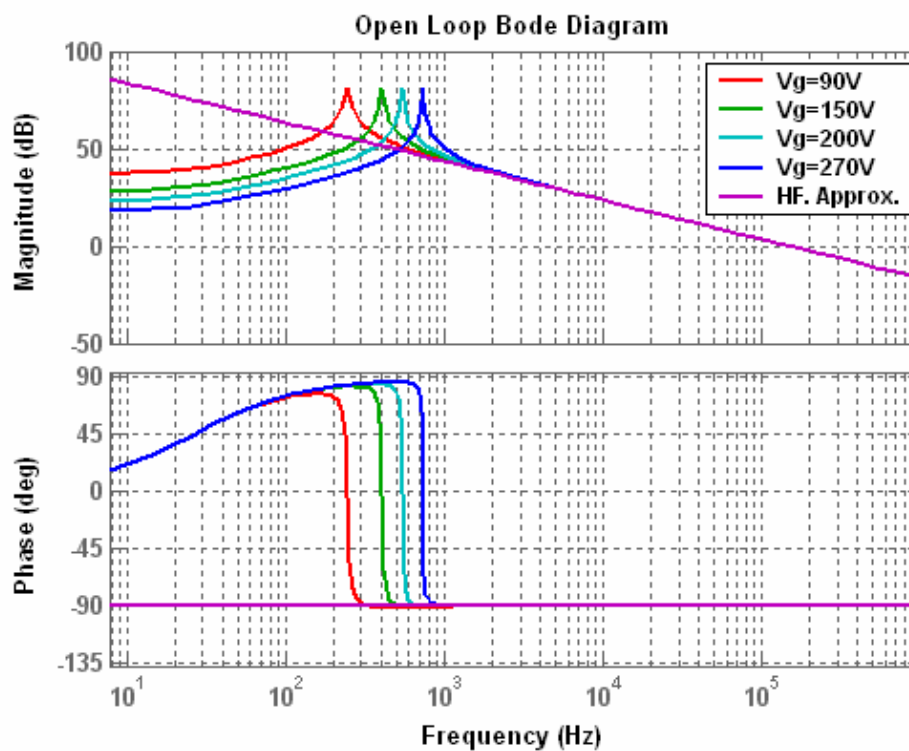$$Ti = G_{id} K_S G_{CA} Fm \tag{4-3}$$

where the modulator gain Fm=1.

For a current loop crossover frequency of fci, the required current compensator dc gain is

$$G_{CA} = \frac{2\pi f_{ci} L}{K_S V_{out}} \tag{4-4}$$

Select fci= 8kHz, the dc gain of the current compensator is G_{CA}=0.264. Set current loop PI compensator zero at 5kHz. So, the integral time constant for the current compensator is, $T_{IC} = 1/(2\pi \cdot 5000) = 3.183 \times 10^{-5}$. Therefore, the complete current loop controller is,

$$G_{CA}(s) = 0.264 \times \frac{1 + 3.183 \times 10^{-5} s}{3.183 \times 10^{-5} s} = 0.264 + \frac{8294}{s} \tag{4-5}$$

$$\Rightarrow \quad G_{CA}(s) = \frac{U_i(s)}{E_i(s)} = K_{Pi} + \frac{K_{Ii}}{s} = 0.264 + \frac{8294}{s} \tag{4-6}$$

Figure 4.6 shows the bode plot of current loop with compensation. The crossover frequency is 8kHz and phase margin is 60 degree (with the consideration of phase drop caused by the computation delay and zero-order-hold delay of digital control, the phase margin for analog controller should be designed at least 10 degrees more.) [27]
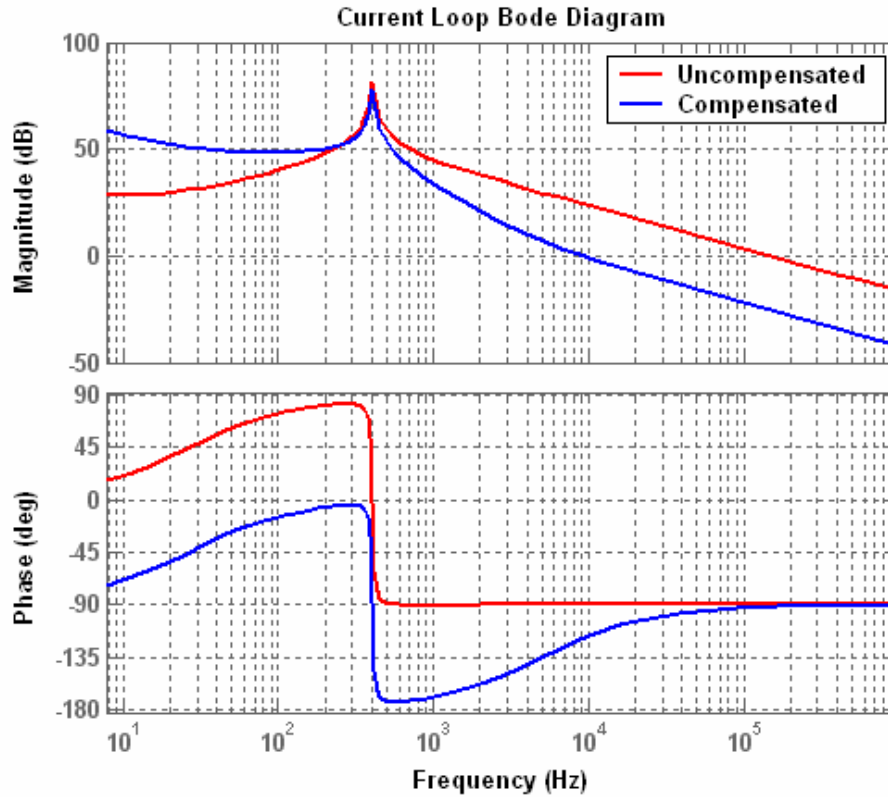
Figure 4.6 Bode plot of current loop gain

This analog controller $G_{CA}(s)$ can be discretised by any of the commonly used discrimination methods. Here, we use the Pole-Zero match method and the digital controller generated is,

$$G_{CA}(z) = \frac{U_i(z)}{E_i(z)} = \frac{0.3068z - 0.2241}{z-1} \tag{4-7}$$

Where, the sampling time is 1/fs=10us. In discrete form, the digital controller can be written as,

$$U_i(n) = U_i(n-1) - 0.3068E_i(n-1) + 0.2241E_i(n) \tag{4-8}$$

where, the quantities with (n) denote the sampled values for the current sampling cycle, the quantities with (n-1) denote one sample old values and so on.

4.1.2.2 Voltage loop compensator design

The low frequency small signal model of the voltage loop [25] is shown in Figure 4.7.
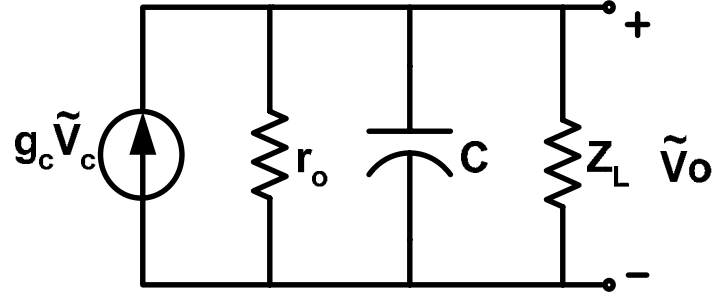
Figure 4.7 Low-frequency small signal model for voltage loop

The voltage loop power stage transfer function can be calculated as,

$$G_{VC}(s) = \frac{\tilde{V}_O}{\tilde{V}_c} = \frac{K_m}{2K_f K_s}\left[\frac{V\min}{V\max}\right]^2 \frac{Z_f}{V_o} \tag{4-9}$$

where, Z_f represents the equivalent impedance of the parallel branch consisting of the bus capacitor C_B, the PFC stage output impedance r_o and the load impedance Z_L, and is given by,

$$Z_f = \frac{1}{\dfrac{1}{r_o} + \dfrac{1}{Z_L} + sC} \tag{4-10}$$

For a constant power load Po, the load impedance Z_L and the output impedance r_o is related by,

$$Z_L = -\frac{V_O^2}{P_O} = -r_o \tag{4-11}$$

Then, voltage loop power stage transfer function is

$$G_{VC}(s) = \frac{6027.37}{s} \tag{4-12}$$

From the block diagram in Figure 4.3, the loop gain equation for the voltage loop is,

$$T_V = K_d G_{VEA} G_{VC} \tag{4-13}$$

Using this loop gain equation, for a voltage loop crossover frequency of fcv, the required voltage error amplifier compensator dc gain is,

$$G_{VEA} = \frac{2K_f K_s}{K_d K_m} \left[\frac{V\max}{V\min}\right]^2 \frac{V_o}{Z_f}\Big|_{f=f_{cv}} \tag{4-14}$$

For fcv=10Hz, the magnitude of voltage controller is, G_{VEA} = 4.27. Set the loop PI compensator zero at 6Hz. Then the integral time constant is, T_{IV}= 1/(2π·6)= 26.54 $\times 10^{-3}$. Therefore, the complete voltage loop controller is,

$$G_{VEA}(s) = 4.27 \times \frac{1 + 26.54 \times 10^{-3} s}{26.54 \times 10^{-3} s} \tag{4-15}$$

$$\Rightarrow \quad G_{CA}(s) = \frac{U_v(s)}{E_v(s)} = K_{Pv} + \frac{K_{Iv}}{s} = 4.27 + \frac{160.89}{s} \tag{4-16}$$

Figure 4.8 shows the Bode plots of the voltage loop without vs. with compensation of 59 degree phase margin.
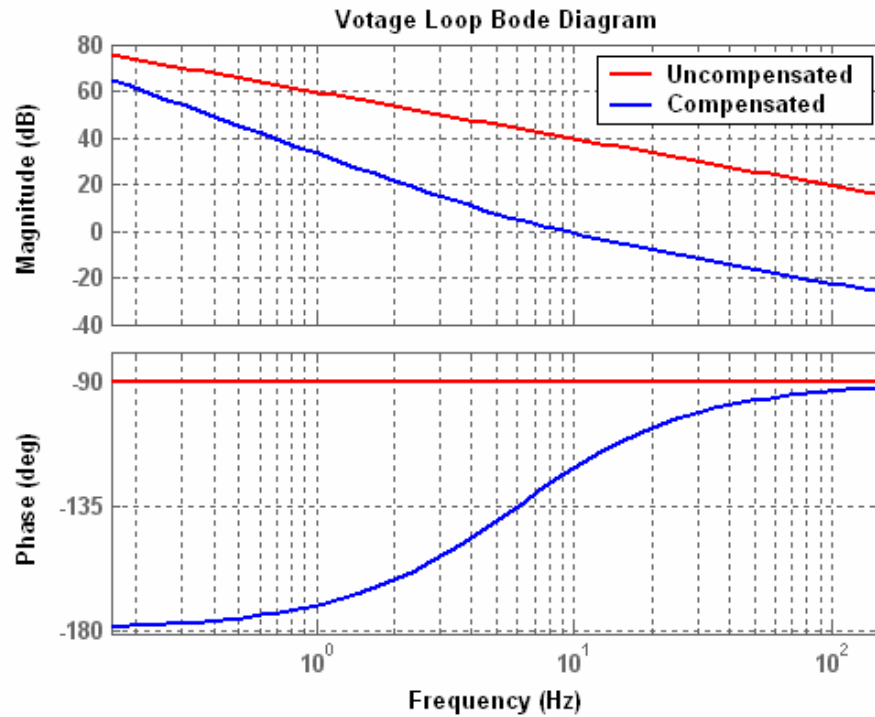
Figure 4.8 Bode plot of voltage loop gain

Then we can discretize the analog controller to digital controller using Pole-Zero match method. The digital controller generated is,

$$G_{CV}(z) = \frac{U_v(z)}{E_v(z)} = \frac{4.271z - 4.269}{z - 1} \qquad (4\text{-}17)$$

Where, the sampling time is 1/fs=10us. In discrete form, the digital controller can be written as,

$$U_v(n) = U_v(n-1) - 4.271E_v(n-1) + 4.269E_v(n) \qquad (4\text{-}18)$$

4.1.3 Digital controller design for flyback converter stage

The flyback converter operates at Continuous Conduction Mode (CCM). The control to output transfer function of the flyback converter is[28-29],

$$G_{CV}(s) = \frac{V_{in}}{D'^2 N} \frac{1 - \dfrac{s}{\omega_z}}{\left(\dfrac{s}{\omega_0}\right)^2 + 2\xi_0 \dfrac{s}{\omega_0} + 1} \tag{4-19}$$

Where, $D' = 1 - D$, $C = C_O / N$, $R = N^2 R_L$

$$\omega_z = \frac{D'^2 R}{L_m D}$$

$$\omega_0 = \sqrt{\frac{D'^2}{L_m C}}$$

$$\xi_0 = \frac{1}{2\omega_0 C R}$$

To compensate the loop gain, we use a controller, whose transfer function is as below,

$$G_{EA}(s) = 3.47 \times 10^4 \cdot \frac{(1 + 1.4 \times 10^{-5} s)(1 + 2.3 \times 10^{-4} s)}{s} \tag{4-20}$$

The crossover frequency selected is 8 kHz and phase margin is 70 degrees. The bode plots of open loop and close loop transfer functions are shown in Figure 4.9.
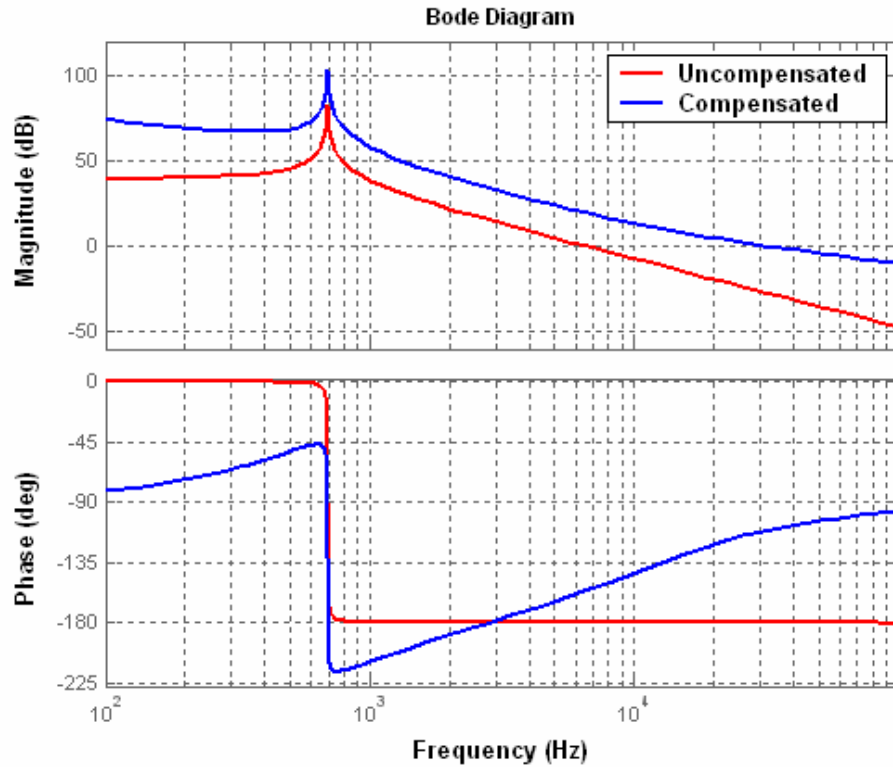
Figure 4.9 Bode plots of flyback converter open loop and close loop transfer

functions

Then we can discretize the analog controller to digital controller using Pole-Zero match method. The digital controller generated is,

$$G_{CV}(z) = \frac{U_v(z)}{E_v(z)} = \frac{15.5z^2 - 21.85z + 7.076}{z - 1} \qquad (4\text{-}21)$$

Where, the sampling time is 10us. In discrete form, the digital controller can be written as,

$$U_v(n) = U_v(n-1) - 15.5E_v(n-2) + 21.85E_v(n-1) - 7.706E_v(n) \qquad (4\text{-}22)$$

4.2 Experimental results of proposed PWM strategy

The design is implemented for 90W output power, 110V AC input. And switching frequency of the PFC stage is 100 kHz and the switching frequency of the flyback converter stage is 200 kHz.

The prototype constructed is controlled by National Instruments LabVIEW FPGA, which allows you to use graphical programming to configure the field programmable gate array (FPGA) on a NI RIO device. You can create a LabVIEW FPGA block diagram, compile it, and download it to a RIO device. This code simultaneously executes a 32-bit counter and pulse generator and a custom control algorithm [30]. Figure 4.10 shows the system diagram of the NI PFGA Module.
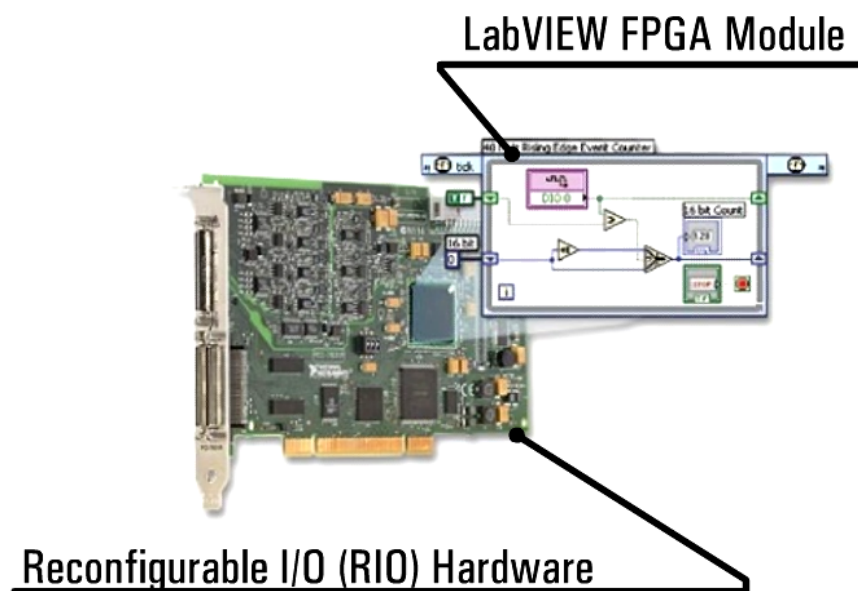

Figure 4.10 System diagram of NI FPGA Module

To provide proof that proposed Leading/Trailing Edge Modulation strategy can reduce more DC-link voltage ripple than the regular Leading/Trailing Edge Modulation

strategy, experiments were conducted both using regular LEM/TEM strategy and using proposed strategy.

Figure 4.11 shows the experimental results of gating signals and input line voltage, line current, DC-link voltage ripple obtained by employing typical Leading/Trailing Edge Modulation strategy that is introduced in Chapter II. The peak to peak DC-link voltage ripple is 6 V with a 120uF DC-link capacitor.

Figure 4.12 presents the experimental results obtained by using the proposed Leading Trailing Edge Modulation strategy, in which the peak to peak DC-link voltage ripple is only 3.8 V with the same DC-link capacitance, which is reduced by 36.7 %. We can see that proposed LEM/TEM strategy can further reduce the DC-link voltage ripple without penalizing the power factor, which will allow us to use an even smaller DC-link capacitor, providing a further reduction of the volume and weight of the AC/DC adapter.
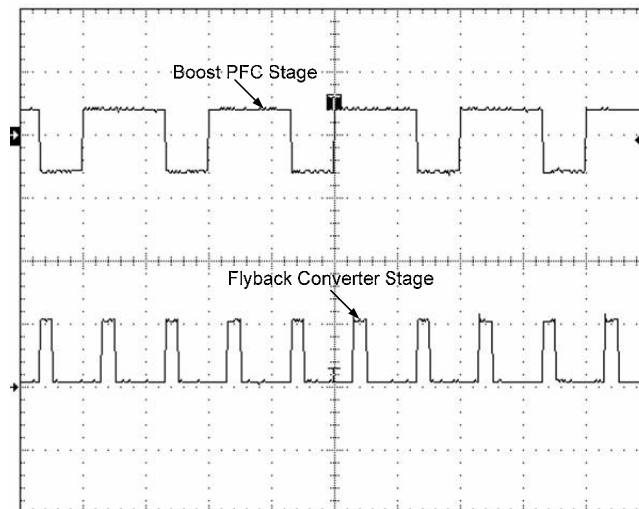
(a)
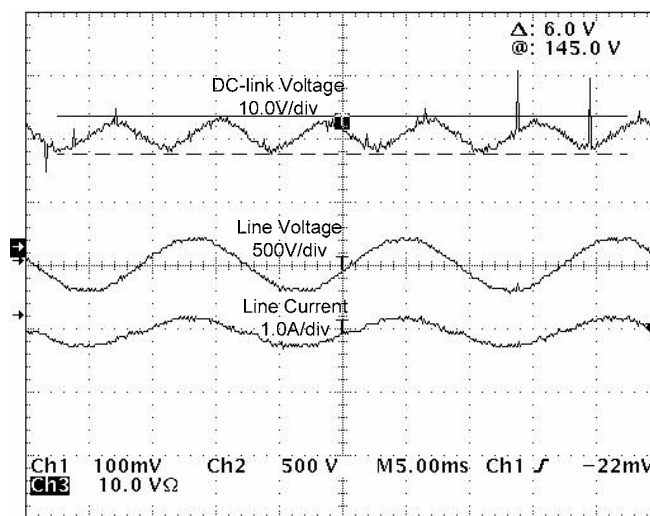
(b)

Figure 4.11 Experimental results obtained using regular LEM/TEM: (a) waveforms

of gating signals of two stages; (b) Waveforms of DC-link voltage, line voltage and
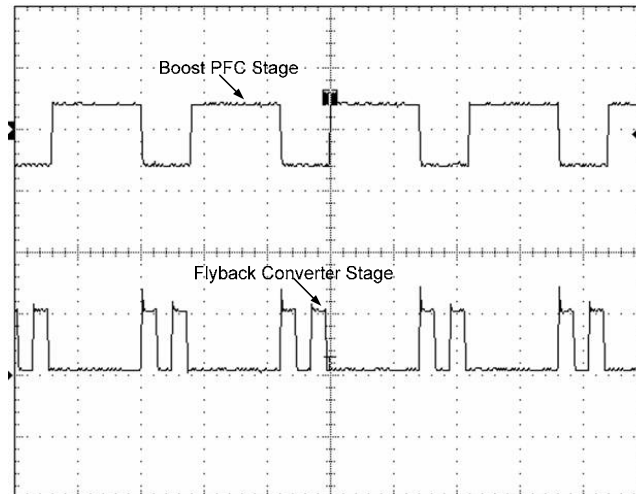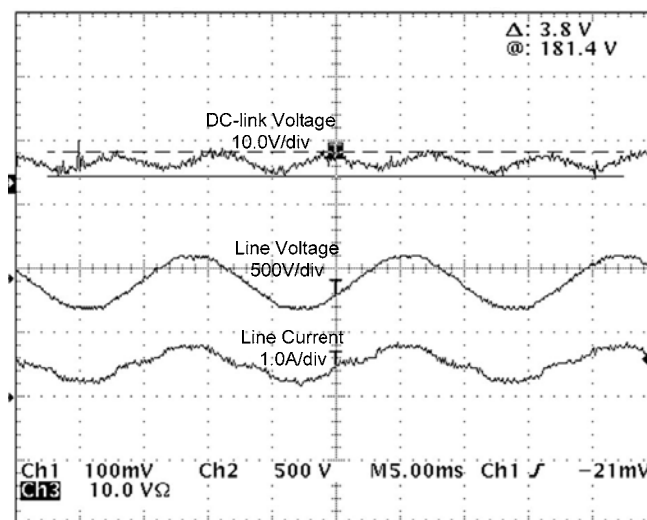
line current

(a)

(b)

Figure 4.12 Experimental results obtained using proposed LEM/TEM: (a) waveforms of gating signals of two stages; (b) Waveforms of DC-link voltage, line voltage and line current

Proposed LEM/TEM strategy's effect on self-heating reduction of the DC-link bulk capacitor was also investigated in the experiments. Temperature of the DC-link capacitor

while the prototype of AC/DC adapter was running was measured. Measurements were done under the same circumstances both using regular LEM/TEM scheme and using proposed LEM/TEM scheme. Figure 4.13 shows the temperature graphs of the DC-link bulk capacitor after the prototype of AC/DC adapter running for 30 minutes. And in Figure 4.14, graph of DC-link capacitor's averaged temperature variation with time under regular LEM/TEM strategy vs. proposed LEM/TEM strategy is presented.

(a)   **(b)**
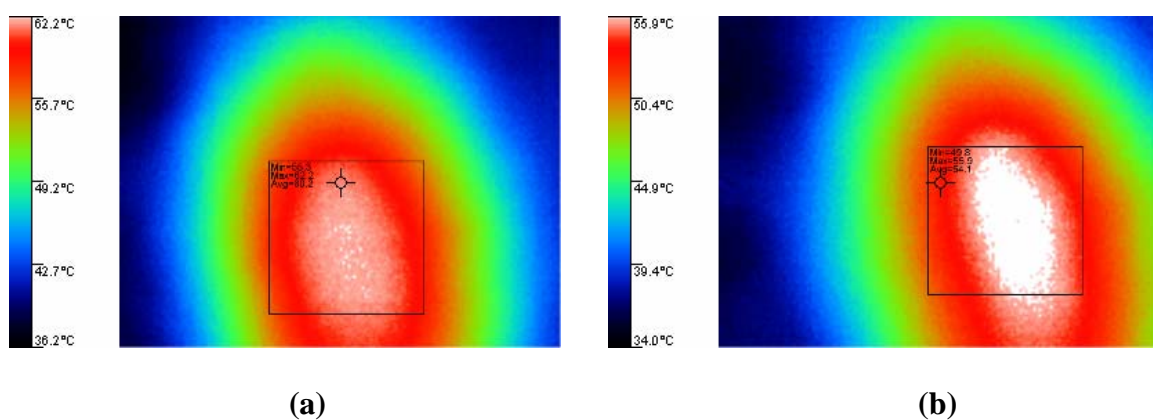
Figure 4.13 Graphs of DC-link capacitor's temperature after 30min: (a) Using regular LEM/TEM strategy (Avg.=60.0 $^{\circ}$C); (b) Using proposed LEM/TEM strategy (Avg. =54.1 $^{\circ}$C)
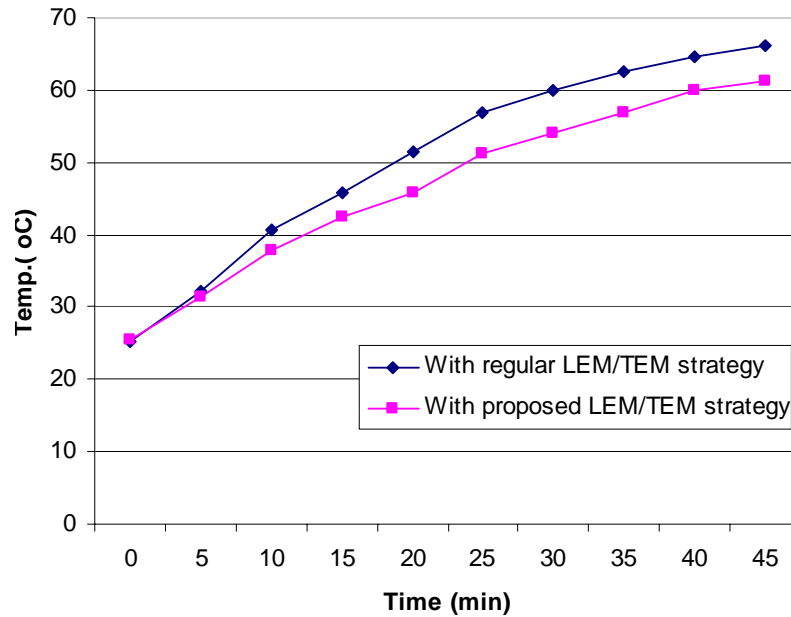
Figure 4.14 Graph of DC-link capacitor's averaged temperature variation with time

under regular LEM/TEM strategy vs. proposed LEM/TEM strategy

From Figure 4.13 and Figure 4.14, we can see that self-heating of DC-link capacitor is further reduced using the proposed strategy, which will help to mitigate the heating problem and power dissipation of AC/DC adapters.

CHAPTER V

CONCLUSIONS

AC -DC adapters require a large DC-link capacitor to store instant energy difference and minimize peak to peak ripple voltage. This bulk DC-link capacitor blocks the size and cost reduction of AC/DC adapters. Besides, due to the large capacitance requirement, aluminum electrolytic capacitor is used in typical AC/DC adapters. Aluminum electrolytic capacitor is not an ideal capacitor and has a larger ESR, which will result in the heating of capacitor. It will further shortening expectancy of aluminum electrolytic capacitor and lower the system efficiency.

Proper synchronization of the two power stages can significantly reduce the ripple current and ripple voltage of the boost output capacitor. Consequently, a smaller DC-link capacitance is achieved and its size and cost will be reduced. Besides, there are other benefits, such as less self-heating of the DC-link capacitor, capacitor life extension and less loss with improved efficiency.

One of the limitations of current leading/trailing edge modulation scheme is that the switching frequencies of two stages need to be equal to achieve the best reduction of boost capacitor ripple current. The DC-link capacitor ripple current will be larger if the switching frequency of DC/DC converter is larger than the switching frequency of PFC pre-regulator. Directed towards this limitation, this thesis proposes a new Leading/Trailing Edge Modulation strategy to further reduce the DC-link capacitor ripple current when switching frequency of DC-DC stage is twice switching frequency of PFC

stage. Chapter III gives mathematical proof of the advantage of the proposed PWM strategy and describes its realization method. Experimental results in Chapter IV shows that employing the proposed PWM synchronization scheme for AC/DC adapters can achieve better reduction of DC-link voltage ripple while DC/DC converter switches at twice the switching frequency of PFC pre-regulator, without penalizing the power factor. And meanwhile, smaller flyback transformer can be achieved while using higher switching frequency for flyback converter. Experimental results are obtained using digital control based on FPGA, which allow concurrent operation (simultaneous execution of all control procedures), enabling high performance and novel control methods.

The other contribution of this thesis is the presentation of detailed mathematical analyses in per-unit quantities to facilitate calculation of DC-link capacitor ripple current reduction with leading/trailing edge modulation strategies.

REFERENCES

[1]   W. F. Ray and R. M. Davis, "The Definition and Importance of Power Factor for Power Electronic Converters," in *Proc. European conference on Power Electronics and Applications (EPE)*, vol.1, pp.799-805, 1989.

[2]   M. Grotzbach, "Line Side Behavior of Uncontrolled Rectifier Bridges with Capacitive DC Smoothing," in *Proc. European Conference on Power Electronics and Applications (EPE)*, vol.1, pp.761-764, 1989.

[3]   K. K. Sen, A. E. Emanuel, "Unity Power Factor Single Phase Power Conditioning," in *Proc. IEEE Power Electronics Specialists Conference*, vol.2, pp.516-524, 1987.

[4]   Y. W. Lo and R. J. King, "High Performance Ripple Feedback for the Buck Unity Power Factor Rectifier," *IEEE Trans. on Power Electronics*, vol.10, pp.158-163, Mar 1995.

[5]   H. Endo, T. Yamashita and T. Sugiura, "A High Power Factor Buck Converter," in *Proc. IEEE Power Electronics Specialists Conference*, vol.2, pp.1071-1076, Jun. 1992.

[6]   R. Erickson, M. Madigan and S. Singer, "Design of A Simple High Power Factor Rectifier Based on the Flyback Converter," in *Proc. IEEE Applied Power Electronics Conference*, vol.1, pp.792-801, Mar. 1990.

[7]   M. Morimoto, K. Oshitani, K. Sumito, S. Sato, M. Ishida and S. Okuma, "New Single Phase Unity Power Factor PWM Converter-Inverter System," in *Proc. IEEE Power Electronics Specialists Conference* , vol.2, pp.585-589, Jun. 1989.

[8]   G. Choe and M. Park, "Analysis and Control of Active Power Filter with Optimized Injection," *IEEE Transactions on Power Electronics*, vol.4, pp.427-433, Oct. 1989.

[9]   A. Lharo, A. Barrado, J. Pleite, R. Vhquez, E. Olias, "New Family of Single-Stage PFC Converters with Series Inductance Interval," in *Proc. IEEE Power Electronics Specialists Conference*, vol.3, pp.1357-1362, Jun. 2002.

[10] M Daniele, P. Jain, "A Single Stage Single Switch Power Factor Corrected AC/DC Converter," in *Proc. IEEE Power Electronics Specialists Conference*, vol.1, pp.216-222, Jun. 1996.

[11] J. Zhang, F. C. Lee, M.M. Jovanovic, "Design and Evaluation of A 450W Single-Stage Power-Factor-Correction Converter with Universal-Line Input," in *Proc. IEEE Applied Power Electronics Conference*, vol.1, pp.357-362, Mar. 2001.

[12] D. Xu, J. Zhang , W. Chen, J. Liu, F. Lee, "Evaluation of Output Filter Capacitor Current Ripples in Single Phase PFC converters," in *Proc. IEEE Power Conversion Conference*, vol.3, pp.1226-1231, Apr. 2002.

[13] J.P. Noon and D. Dalal, "Practical Design Issues for PFC Circuits," in *Proc. IEEE Applied Power Electronics Conference*, vol.1, pp.51-58, Feb. 1997.

[14] J.P. Noon, "Designing High-power Factor Offline Power Supplies," Dallas: Texas Instruments.

[15] "Advanced PFC/PWM Combination Controllers," Data Sheet, Dallas: Texas Instruments.

[16] "Fairchild Semiconductor Application Note 42045," South Portland, ME: Fairchild Semiconductor.

[17] D.M. Sable, B.H. Cho, and R.B. Ridley, "Use of Leading-Edge Modulation to Transform Boost and Flyback Converters into Minimum Phase Zero Systems," *IEEE Trans. on Power Electronics*, vol. 6, No. 4, pp. 704-711, Oct 1991.

[18] B. Carsten, "Simplified Calculation of Magnetic and Electrical Losses in Unity Power Factor Boost Preregulators," Anaheim, CA: Micrometals. Inc.

[19] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-Frequency Digital PWM Controller IC for DC/DC Converters," *IEEE Trans. On Power Electronics*, vol.18, no.1, pp. 438-446, January 2003.

[20] A. V. Peterchev, J. Xiao, and S.R. Sanders, "Architecture and IC Implementation of A Digital PWM Controller," *IEEE Trans. on Power Electronics*, vol.18, no.1, pp. 356-364, Jan. 2003.

[21] A. Prodic, D. Maksimovic, "Digital PWM Controller and Current Estimator for A Low-Power Switching Converter," in *Proc. the 7ᵗʰ IEEE workshop on Computers in Power Electronics, C*OMPEL 2000, pp.123-129.

[22] T.W. Martin and S.S. Ang, "Digital Control of Switching Converters," *IEEE Symposium on Industrial Electronics*, vol. 2, pp. 480-484, 1995.

[23] P. Zumel, A. De Castro, O. Garcia, T. Riesgo, J.Uceda, "Concurrent and Simple Digital Controller of An AC/DC Converter with Power Factor Correction," in *Proc. IEEE Applied Power Electronics Conference*, vol.1, pp 469 -475, Mar 2002.

[24] L.H. Dixon, "Average Current Mode Control of Switching Power Supplies," in *Proc. Unitrode Power Supply Design Seminar*, vol.1, pp.204-217, Feb.1990.

[25] C.L. Phillips and H.T. Nagle, *Digital Control System Analysis and Design*, Englewood Cliffs, NJ: Prentice-Hall, Inc., 1984.

[26] R.B. Ridley, "Average Small-Signal Analysis of the Boost Power Factor Correction Circuit", in *Proc. the Virginia Power Electronics Center Seminar (VPEC)*, Blacksburg, VA, Sept 1989.

[27] S. Choudhury, *Designing a TMS320F280x Based Digitally Controlled DC - DC Switching Power Supply*, Dallas: Texas Instruments, Jul. 2005.

[28] H. Terashi, I. Cohen and T. Ninomiya, "Stability and Dynamic Response Improvement of Flyback DC-DC Converter by a Novel Control Scheme," in *Proc. IEEE Applied Power Electronics Conference*, vol.1, pp.389-394, Mar. 2002.

[29] T.H. Chen, W.L. Lin, C.M. Liaw, "Dynamic Modeling and Controller Design of Flyback Converter," *IEEE Trans. on Aerospace and Electronic Systems*, vol.35, no.4, pp.1230-1239, Oct. 1999.

[30] *LabVIEW FPGA Module User Manual*, Austin, TX: National Instruments, Mar. 2004.

VITA

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