DESIGN OF RF/IF ANALOG TO DIGITAL CONVERTERS FOR SOFTWARE RADIO COMMUNICATION RECEIVERS

A Dissertation

by

BHARATH KUMAR THANDRI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2006

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Design of RF/IF Analog to Digital Converters for Software Radio Communication Receivers. (May 2006)

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Software radio architecture can support multiple standards by performing analog-to-digital (A/D) conversion of the radio frequency (RF) signals and running reconfigurable software programs on the backend digital signal processor (DSP). A slight variation of this architecture is the software defined radio architecture in which the A/D conversion is performed on intermediate frequency (IF) signals after a single down conversion.

The first part of this research deals with the design and implementation of a fourth order continuous time bandpass sigma-delta (CT BP ΣΔ) ADC based on LC filters for direct RF digitization at 950 MHz with a clock frequency of 3.8 GHz. A new ADC architecture is proposed which uses only non-return to zero feedback digital to analog converter pulses to mitigate problems associated with clock jitter. The architecture also has full control over tuning of the coefficients of the noise transfer function for obtaining

the best signal to noise ratio (SNR) performance. The operation of the architecture is examined in detail and extra design parameters are introduced to ensure robust operation of the ADC. Measurement results of the ADC, implemented in IBM 0.25 μm SiGe BiCMOS technology, show SNR of 63 dB and 59 dB in signal bandwidths of 200 kHz and 1 MHz, respectively, around 950 MHz while consuming 75 mW of power from ± 1.25 V supply.

The second part of this research deals with the design of a fourth order CT BP ΣΔ ADC based on g_m-C integrators with an automatic digital tuning scheme for IF digitization at 125 MHz and a clock frequency of 500 MHz. A linearized CMOS OTA architecture combines both cross coupling and source degeneration in order to obtain good IM3 performance. A system level digital tuning scheme is proposed to tune the ADC performance over process, voltage and temperature variations. The output bit stream of the ADC is captured using an external DSP, where a software tuning algorithm tunes the ADC parameters for best SNR performance. The IF ADC was designed in TSMC 0.35 μm CMOS technology and it consumes 152 mW of power from ± 1.65 V supply.

DEDICATION

To Shakuntala, my late grandmother.

To all my teachers - from high school to graduate school

ACKNOWLEDGMENTS

As I come close to finishing my graduate studies, it has been a great learning experience and I would like to thank a lot of people who have helped me through various stages of my career.

I would like to thank my advisor Dr Jose Silva-Martinez, who has been a great source of inspiration and support throughout my graduate studies. When I first approached him to start my M.S. research, he accepted me as his student in spite of my limited knowledge in analog and mixed signal design owing to my prior computer science background during my Bachelor's program. The endless doubts from my side never bothered him and he patiently answered all my questions, which was one of the main reasons I decided to continue my PhD under his supervision. The long discussions with him have helped me to understand different aspects of analog design and I am greatly indebted to him for all his guidance during my graduate studies.

I would like to thank all my PhD committee members – Dr Aydin Karsilayan, Dr Takis Zourntos, Dr Shankar Bhattacharya and Dr Vinod Srinivasan, for agreeing to serve in my committee and reading my dissertation. Dr Takis Zourntos explained various aspects of behavioral models in Matlab which helped me speed up my research work. The graduate control theory course that I took under Dr Bhattacharya was very interesting and I would like to thank him for discussions on possible application of non-linear control theory to my research work. The courses that I took under other professors

in our AMSC group helped me to learn various aspects of IC design. Special mention and thanks goes to Dr Ugur Cilingiroglu - his courses on basic analog IC design, semiconductor devices and MOS modeling helped me tremendously because of his clear explanation of all basic concepts. Our group secretary, Ella Gallagher, has always been a tremendous help in all aspects of administrative work.

I would like to thank all my colleagues in the AMSC group for the great discussions and help throughout my stay. Special mention goes to Chinmaya Mishra who helped with the design of digital blocks for the RF ADC project and to Xuemei Liu who helped in the design and layout of the IF ADC project.

Looking back in my career, I realize that I'm deeply indebted to all my teachers (from high school to graduate school) who have helped me grow in both technical and personal aspects. Special mention goes to Mrs Shyla George and Mr C Subramanian (both high school teachers) and to Dr Santosh Kumar (professor during my Bachelor's degree), who were great mentors.

I'm always grateful for the love and support from my family. One person who has made the greatest impact in my life is my late grandmother – Shakuntala. I would like to thank my parents and my sister for their constant love, encouragement and their belief in me, which has been a great source of inspiration throughout my graduate studies. I would like to thank my wife Preethi, who is always there for me with her unconditional love and a smiling face all the time. She will always be the shining light in my life and a great motivating factor for all my endeavors.

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CHAPTER I

INTRODUCTION

1.1. Motivation

The wireless communication industry has experienced tremendous growth since the early 1990's throughout the world, especially in Europe, Asia and the USA. The wireless market is poised for more growth in the future, with the demand increasing due to addition of new services which provide more functionality for the end users. One of the main reasons for this growth has been the major progress in the field of radio frequency (RF) integrated circuit design and the design trend is slowly advancing towards a single chip transceiver with very few external components. The major developments in system-on-chip (SoC) design, which enables integration of analog and digital designs on the same chip has led to integration of analog RF, analog baseband and digital signal processors on the same chip. This has resulted in sleek and low power handset devices with multi-purpose functionality like videos, voice, pictures and internet access.

The number of wireless standards has also increased drastically along with the market growth, with each standard catering to specific market segments. The most common wireless communication applications along with some of their standards are shown in Fig. 1.1. The personal communication (cell phones) segment includes standards like GSM (global system for mobile communications), GPRS (general packet radio service), EDGE (enhanced data rate for GSM evolution), CDMA (code division

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This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

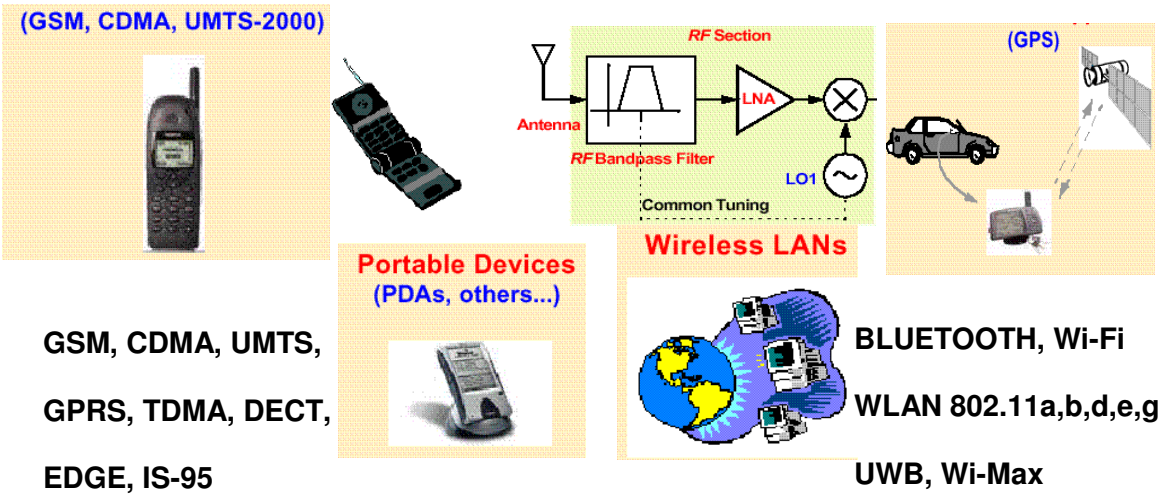


Fig. 1.1. Wireless communication applications and standards

multiple access), AMPS (advanced mobile phone systems), UMTS (universal mobile telecommunication system), PCS (personal communication service), TDMA (time division multiple access), DECT (digital European cordless telephone), IS-95 (digital version of AMPS) etc. The wireless local area network (WLAN) for laptops, desktops and PDA's include standards like IEEE 802.15, also known as Bluetooth, for the personal area network (PAN); IEEE 802.11 a/b/g and Wi-Fi for wireless home area networking, IEEE 802.16 a/e and Wi-Max for wide-area high speed wireless zones, in the wireless metropolitan Area Network (MAN) segment, and IEEE 802.20 for the wide area network (WAN). The satellite communication market segment comprising of navigation systems for locating position of objects (such as commercial systems used in cars) use the GPS (global positioning system) standard. Another wireless standard that is gaining popularity recently is IEEE 802.15.3a or UWB (Ultra wide band) for short range

high data rate applications in the local area network segment. The number of wireless standards is increasing everyday with committees being formed in all regions of worlds to define these standards.

The prominent differences between the wireless standards are the geographical area of usage, location in the frequency spectrum of the uplink and downlink channels for base stations and user handsets, channel spacing and the number of channels (total bandwidth of the standard), symbol and chip rates, type of multiple access techniques (time division, frequency division, code division multiple access or a combination of these techniques), type of modulation scheme [some examples include BPSK (binary phase shift keying), QPSK (quadrature phase shift keying), GMSK (gaussian minimum shift keying) etc..], specifications for minimum signal power delivered by the antenna (receiver sensitivity) and maximum transmit power at the transmit side, adjacent channel specifications (blocker specification), etc [1]. There are different governing bodies in each country which regulate the commercial usage of frequency spectrum, which has resulted in adoption of different standards in different regions of the world. The wireless communication service providers all over the world invest lot of infrastructure to support the wireless standards in base stations for their respective coverage areas. The end user devices (cell phones, wireless network cards etc) usually support transmission and reception of signals for only one standard. A major requirement of the next generation of wireless devices and base stations is a single chip set with minimum external components that can support multiple standards. This would enable a single wireless device which makes use of functionality that is supported by multiple service providers.

The support for multiple standards would increase the number of features supported by the mobile devices (internet access, voice, data, pictures etc) with a faster response time. There are many technical challenges, both at hardware and software level that needs to be overcome in order to realize such a multi-standard chip set.

Software radio architecture, which is described in detail in the next chapter, has been proposed as a solution for support of multiple wireless standards in the same chip. The main goal in a software radio transceiver is to perform the analog to digital (A/D) and digital to analog (D/A) conversion as close to the antenna as possible, with reconfigurable software programs running in the backend digital signal processor (DSP). This research deals with the design of analog to digital converters (ADC's) for use in software radio architectures.

1.2. Research contributions

The main aim of this research is to explore new design techniques for radio frequency (RF) and intermediate frequency (IF) ADC's that can be used for digitization in a software radio communication receiver. Different ADC architectures were analyzed and a continuous time bandpass sigma-delta ($\Sigma\Delta$) ADC architecture was found to be the best choice for this application. The main drawbacks of ADC's that have been previously reported in literature were identified and new design techniques are proposed both at architectural and circuit level to overcome these limitations. The integrated circuit implementations of the two ADC designs are then presented in detail.

The first part of this research presents the design of a direct radio frequency (RF) ADC at 950 MHz center frequency using 3.8 GHz clock in IBM 0.25 μm SiGe BiCMOS technology. A fourth order continuous time bandpass ΣΔ ADC with LC filter was implemented using a new architecture with only Non-Return to Zero (NRZ) digital to analog converter (DAC) to reduce SNR degradation due to clock jitter. The operation of the proposed ADC architecture is examined in detail and extra parameters are introduced in the design to improve the operating range of the ADC. Power optimization techniques are used both at architectural and circuit level to obtain good signal to noise ratio (SNR) with minimum power consumption. The ADC consumes 75 mW of power and measurement results indicate SNR of 63 dB and 59 dB in signal bandwidths of 200 kHz and 1 MHz, respectively around 950 MHz center frequency. The proposed ADC design's power consumption is reduced by a factor of 83, when compared to an ADC reported in the literature for similar SNR performance. The measurement results of the ADC show that high resolution narrowband direct digitization is possible at RF frequencies with low power consumption and enhances the state of art for continuous time bandpass sigma delta (CT BP ΣΔ) ADC's operating at GHz sampling frequencies.

The second part of this research deals with the design of an intermediate frequency (IF) ADC at 125 MHz center frequency and 500 MHz clock in TSMC 0.35 μm CMOS technology. The fourth order continuous time bandpass ΣΔ ADC uses an architecture with only Non-Return to Zero (NRZ) DAC and gm-C (transconductance-C) filter, which is ideal for integrated implementation at intermediate frequencies. The gm-C filter uses a novel OTA (operational transconductance amplifier) design which combines cross

coupling and source degeneration to enhance its linearity performance at 125 MHz. A new automatic digital tuning algorithm is proposed to tune the ADC at the system level in order to guarantee the performance over process, voltage and temperature (PVT) variations. The digital bit stream is captured using an external digital signal processor (DSP) and the noise transfer function (NTF) is measured using Fast Fourier Transform (FFT) in the DSP. This information is used to tune the center frequency and quality factor (Q) of the gm-C bandpass filter, and the DAC currents, which maximizes the SNR performance for the ADC. The postlayout simulation of the fourth order modulator show SNR of 50 dB in 1 MHz bandwidth around 125 MHz, while consuming 152 mW of power from supply voltage of ± 1.65 V.

1.3. Organization

The main aspects of analog to digital converters in communication receivers are presented in Chapter II. The different types of architectures for communication receivers are discussed, followed by an analysis of possible ADC architectures for a software radio communication receiver. Chapter III presents an overview of continuous time bandpass (CT BP) ΣΔ ADC's, which are well suited for use in a software radio communication receiver. The design approach, advantages and disadvantages of CT BP ΣΔ ADC's are discussed and main drawbacks of implementations reported in literature are identified. A fourth order LC bandpass ΣΔ ADC which performs direct digitization of RF signals around 950 MHz with 3.8 GHz clock is presented in Chapter IV. The proposed ADC architecture is analyzed in detail and the circuit implementation of the

ADC building blocks are then presented. A detailed description of the test setup and discussion of the measurement results are given at the end of the chapter. A fourth order gm-C bandpass ΣΔ ADC for digitization of IF signals around 125 MHz with 500 MHz clock is presented in Chapter V. The architecture, circuit implementation and the digital tuning scheme of the IF ADC are described in detail, followed by simulation and measurement results. The final chapter draws some conclusion and provides a summary of this research work, together with possible future research directions for ADC's in software radio receivers.

CHAPTER II

ANALOG TO DIGITAL CONVERSION IN COMMUNICATION RECEIVERS

2.1. Receiver architectures

The main objective of a receiver for wireless communication applications is to recover the base band signals that are modulated on a carrier wave at radio frequencies. The up converted base band signals are transmitted at over air (channel) using power amplifiers and the signal power at the transmitter output is very high, usually in the Watt range. The carrier signals are corrupted by noise and adjacent band interferers (that coexist in the electromagnetic spectrum) as they propagate through the channel and the signal power at the receiver input (after the antenna) is very low, usually in the nano-watt range. The two main considerations for signals as they pass through the receiver are noise and distortion. The lower bound of the signal is determined by the noise floor and the upper bound is dictated by the distortion components [2]. The lowest signal that can be detected at the input of the receiver is defined as the sensitivity of the receiver and is given by

$$\text{Sensitivity (dBm)} = -174 \text{ dBm/Hz} + \text{NF (dB)} + 10\log(\text{BW}) + \text{SNR}_{min}(\text{dB}) \quad (2.1)$$

where the NF is the noise figure of the receiver, BW is the bandwidth of the signal and SNR_{min} is the minimum signal to noise ratio required at the output of the receiver for a given bit error rate (BER). The sum of the first three terms gives the total integrated noise of the system and is usually referred to as the noise floor. Noise figure is a measure of how much noise the system adds to the signal as it passes through it and is defined as

$$NF = \frac{SNR_{input}}{SNR_{output}} \tag{2.2}$$

The signal bandwidth, SNR_{min} and sensitivity are usually specified for a wireless standard and the required noise figure of the receiver can be calculated from (2.1).

The nonlinear behavior of receiver gives rise to distortion components and metrics such as P_{1dB} (1 dB input compression point), IIP3 (third order input intercept point), IM3 (third order intermodulation distortion), cross modulation etc are used to define the linearity requirements of a receiver. Due to device and component nonlinearities, the signals from adjacent channel mix together with the signal in the required bandwidth, which causes in-band distortion at the output. The wireless standards have desensitization or blocking specifications to determine how strong an adjacent band carrier can exist without corrupting the in-band signal. At the antenna, the power of the desired signal maybe in the order of -112 dBm (0.56 μV_{rms} in a 50 Ω impedance) while the power of the interfering signals in adjacent bands maybe in the order of 30-60 dB higher. Following detection of signals at the antenna, the receiver must amplify the signals, suppress the interferers, translate the RF signals to base band and extract the desired information. The two main metrics that are used to evaluate the performance of a receiver are sensitivity and selectivity. A receiver with a high sensitivity can process weak desired signals in the presence of noise while a receiver with high selectivity can process a desired signal in presence of strong interferers at adjacent frequencies. The specifications of most wireless communication standards require receivers to have both high sensitivity and selectivity performance. In general,

the filters determine the selectivity and the other analog building blocks determine the sensitivity of the receiver. Along with these stringent specifications, all portable wireless devices have an additional requirement of low power dissipation in order to increase the battery life, which adds extra complexity to the receiver design.

The design of a high performance, low power integrated RF receiver in mainstream silicon technologies (CMOS, BiCMOS) is a very challenging task involving numerous tradeoffs during the design process, especially between noise, linearity and power consumption. The first step in the receiver design is to derive the system level performance requirements from the wireless standard specifications. The next step would be the choice of the best architecture for the receiver implementation. Then, the specifications for each building block of the receiver can be determined based on the receiver architecture and system level specifications.

This chapter presents an overview of different types of receiver architectures that are suitable for integrated circuit implementation. The chapter starts with a description of the superheterodyne architecture, which is the most widely used receiver architecture, followed by the direct conversion receiver architecture. The requirements of next generation of wireless communication devices is a single chip receiver that can support multiple standards, but superheterodyne or direct conversion architectures are not well suited for implementing more than one standard. The software radio architecture, which has been proposed as an alternative to the traditional architectures for implementing multiple standards in the same chip, is reviewed in detail. Intermediate frequency (IF) digitization or software defined radio architecture, which is practically feasible for

implementation in current silicon technologies, is also analyzed. The output of all the receiver architectures is in digital format, which can be readily given as input to the digital signal processor (DSP) following the receiver. Different ADC architectures for possible use in software radio implementation are analyzed to identify their advantages and disadvantages for this application. The chapter ends with a survey of ADC's that have been reported in literature for radio frequency and intermediate frequency digitization of signals in communication receivers.

2.1.1. Superheterodyne architecture

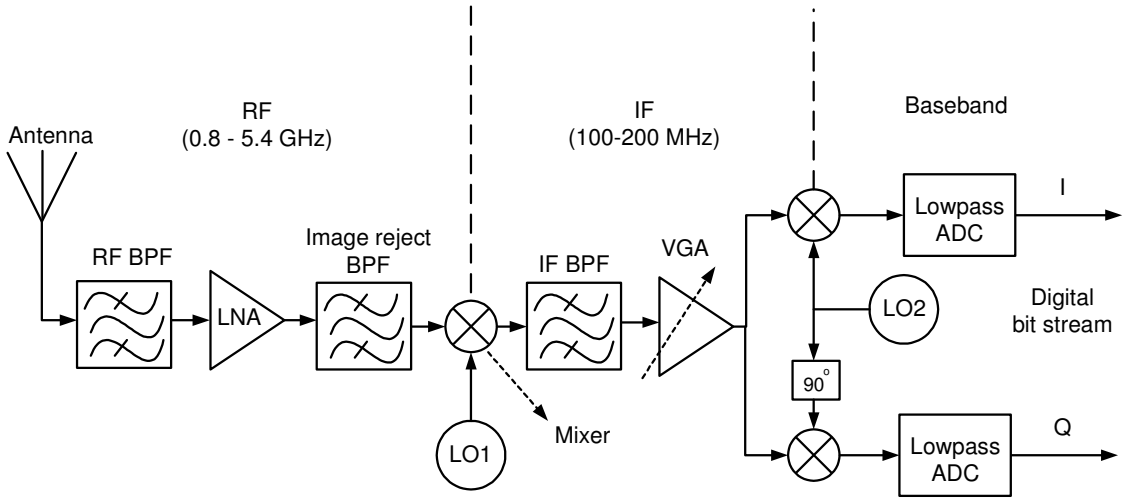


Fig. 2.1. Superheterodyne receiver architecture

The concept of superheterodyne architecture was introduced by Edwin Armstrong in 1918, where the incoming high frequency signal is down converted to a

lower frequency using a mixer and processed at lower frequencies. This architecture has many advantages for processing a high frequency input signal. The channel selection is implemented by varying the frequency of the local oscillator and range of signals that can be handled is determined by the tuning range of the oscillator. The down conversion of signals reduces the design requirements of receiver implementation as amplification and filtering of signals is easier to achieve at low frequencies rather than at high frequencies [3]. The basic architecture proposed by Armstrong has evolved over the years with minor variations and it is the most popular receiver architecture for wireless communication receivers.

The block diagram of a typical superheterodyne architecture used in modern communication receivers is shown in Fig. 2.1, where the RF signal is converted to base band in multiple frequency translation steps. The incoming signal at the antenna is pre-selected by off-chip RF bandpass filter (BPF), which is tuned to the RF carrier frequency. The quality factor of the BPF is very high and is usually implemented using off-chip SAW (surface acoustic wave) filters. The signal is then amplified by a low noise amplifier (LNA), followed by an image reject BPF before the down conversion to an intermediate frequency by the first local oscillator (LO1). The IF signal is further filtered by IF BPF and amplified by the variable gain amplifier (VGA) before being frequency translated to base band into parallel in-phase (I) and quadrature (Q) signals by the second local oscillator (LO2). The baseband analog signals are then converted into digital signals using low pass analog to digital converters (ADC) for both I and Q paths.

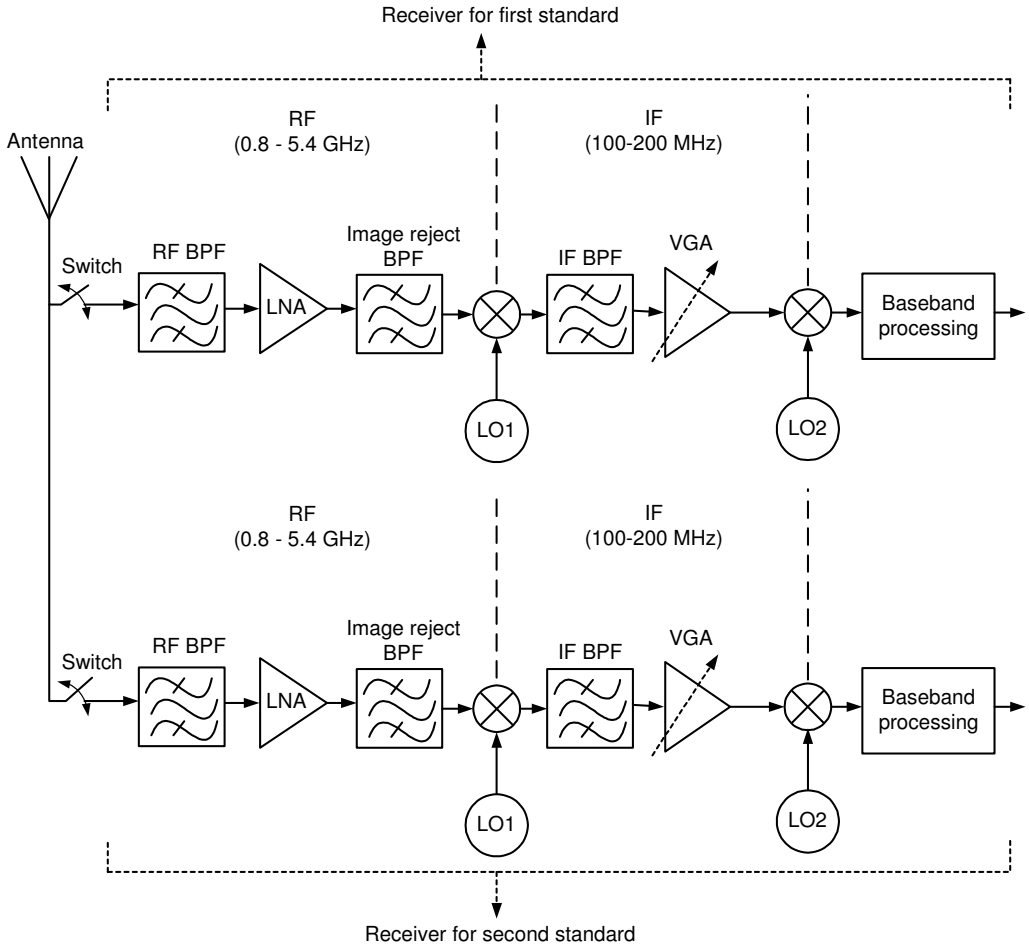


Fig. 2.2 Implementation of multiple standards using the superheterodyne architecture

The location of the intermediate frequency (f_{IF}) is related to the image problem that arises during the down conversion process. The desired signal centered at carrier frequency (f_c) is down converted to intermediate frequency f_{IF} using local oscillator frequency ($f_c + f_{IF}$). However, the signal centered at image frequency ($f_c + (2*f_{IF})$) is also down converted to f_{IF}, thereby corrupting the desired signal. A higher location of IF helps to provide the maximum attenuation of the image frequencies from the image reject BPF, while a lower IF relaxes the filtering and amplifier requirements for the IF

BPF and the VGA. A minor variation of the superheterodyne architecture such as Weaver image reject [4] architectures has been proposed to overcome the image problem. The current focus of research in RF receiver design is to support multiple standards in the same chip. The typical approach for implementing a multi standard receiver using superheterodyne architecture is to replicate paths for each standard and multiplex it in time using analog switches, as shown in Fig. 2.2. The main problem is that most of the blocks are analog in nature and have to be redesigned for each standard. There is minimal reuse of the components which results in large area and power consumption overhead. This approach becomes impractical as the requirement for number of standards increases and a more reasonable solution is required.

2.1.2. Direct conversion architecture

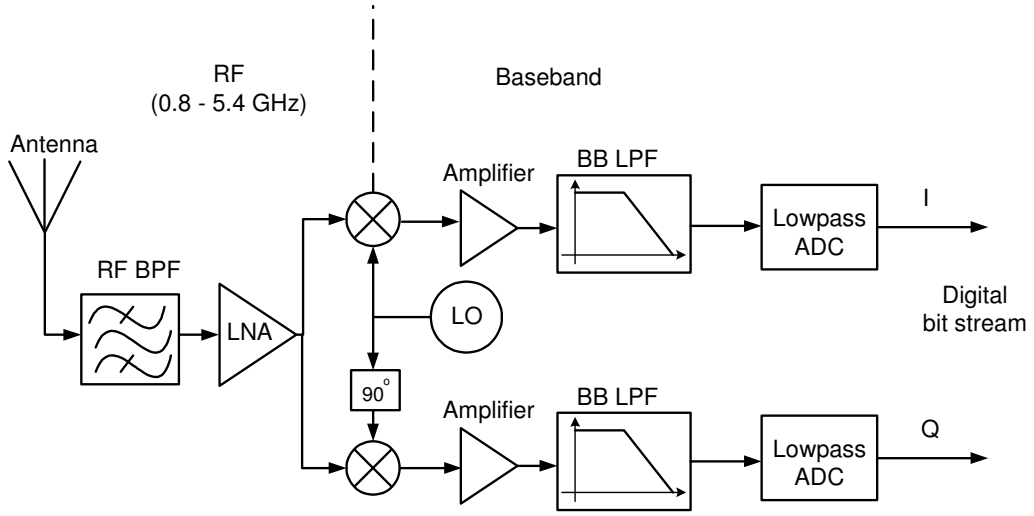


Fig. 2.3. Direct conversion or homodyne architecture

The direct conversion receiver architecture directly down converts the signal to baseband rather than converting it into an IF first, and image rejection is no longer necessary in this approach. The block diagram of a direct conversion or homodyne architecture is illustrated in Fig. 2.3. The RF signal that comes out of the antenna is filtered by the RF BPF and amplified by the LNA before being down converted directly to baseband along parallel in-phase (I) and quadrature (Q) signals. The frequency translation is performed by using two mixers using 0° and 90° phase shifted local oscillator (LO) signals. The I and Q base band signals are amplified and low pass filtered before the A/D conversion. This architecture eliminates all intermediate frequency components and their associated design challenges, especially the image reject problem. However, two practical implementation problems that have limited the use of direct conversion architectures are DC offset and flicker noise [5]. DC offsets saturate the base band circuits and if uncorrected, degrade the bit error rate (BER) performance of the system. The power spectral density flicker noise of transistors is inversely proportional to frequency and it severely degrades the performance of base band circuits in direct conversion receivers. Direct conversion architectures are also not well suited for implementing multiple standards, as each block has to be replicated for every standard.

2.1.3. Software radio architecture

The term “software radio” is used to define a broad class of radio transceivers where key operations such as modulation and demodulation of signals is done in software and the fundamental aspects of the radio operation can be reconfigured by

upgrading that software [6] . The concept of software radio was introduced by Joseph Mitola III in 1991 [7] and the block diagram of ideal software radio transceiver architecture is shown in Fig 2.4. The input RF signal is multiplexed in time between the transmit and receive paths through the T/R (transmit/receive) switch. The digital signal information from the DSP is converted to RF output frequencies by the DAC and driven to the channel by the linear power amplifier in the transmit path. In the receive path, the RF input signals are directly sampled and digitized by the ADC. The digital bit stream is given to the backend DSP, where demodulation and other signal processing algorithms results in recovery of the transmitted base band signal.

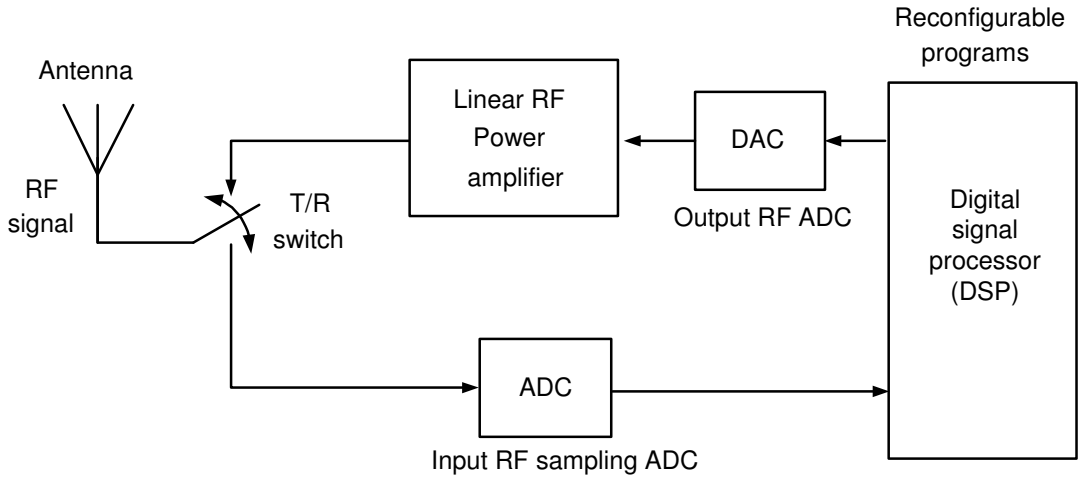


Fig. 2.4. Ideal software radio architecture

The ideal software radio receiver architecture shown in Fig. 2.4 has some very stringent requirements which cannot be implemented using currently available silicon IC technologies. The input RF signal power varies from a few μW to milli Watts, which

together with distortion and noise specifications translates to receiver dynamic range of around 120 dB. The ADC would require greater than 20 bits of resolution at GHz sampling frequencies, to satisfy the receiver's dynamic range requirement [6]. A modified form of the software radio architecture, shown in Fig. 2.5, greatly reduces the ADC resolution requirements and it is considered for this research. The input RF signal is processed by the RF BPF and amplified by the LNA. The variable gain amplifier (VGA) controls the signal amplitude variations to reasonable levels at the input of ADC. The ADC converts the RF signal to digital output and the analog processing blocks preceding it greatly reduces its dynamic range requirement.

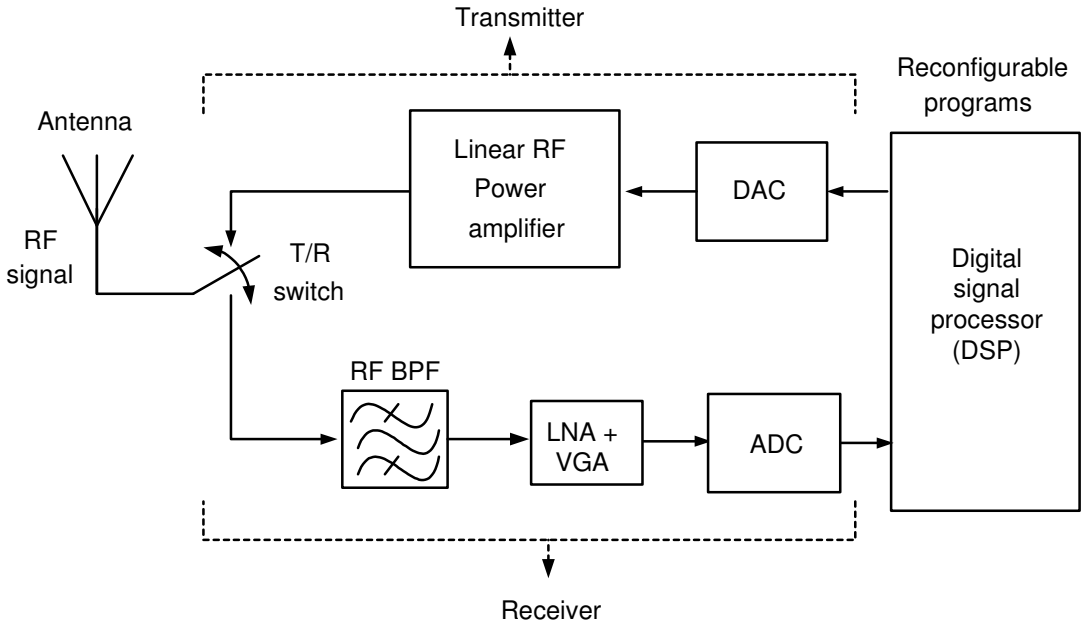


Fig. 2.5. Modified software radio architecture

The two main components of software radio receiver are the RF front end blocks and the back end software platform and algorithms running on the DSP. The main emphasis in a software radio receiver is to perform the A/D and D/A conversion as close to the antenna as possible; the modulation/demodulation schemes, protocols, equalization etc for both transmit/receive paths are all determined in software that runs in the digital signal processor (DSP) [7]. Software radio is the flexible and adaptive radio architecture that can provide multiple services, support multiple standards and multiple bands because it can be reconfigured and reprogrammed by the software programs that run in the DSP. This is a broad definition which includes all digital transceivers and software supported adaptability for multiple operations and environments [8]. The ultimate goal in radio receiver design is to directly digitize the RF signal at the output of the antenna and trends in receiver design have evolved towards this goal by incorporating digitization closer and closer to the receive antenna at increasingly higher frequencies and wider bandwidths [9]. The early digitization in the signal path also eliminates need for additional mixers (for down conversion), filters and analog processing blocks, which can result in significant savings in power and area. Additionally, the demodulation of in phase/quadrature (I/Q) in digital domain eliminates the problem of gain/phase mismatches between I/Q paths which occurs when the demodulation is done in analog domain. A new standard can be easily added by writing a software program for the radio interface and upper layer protocols, provided the first analog stage can provide a digitized version of the RF signal. This would require the use of a wideband and high resolution ADC and DAC to cover the frequency spectrum of all

standards and their respective channels [10]. The DSP can also be replaced by field programmable gate arrays (FPGA's), any general purpose microprocessors or a combination of these in order to run the required software programs at the data rate output of the ADC. The clock frequency of currently available commercial DSP's is in the 1-2 GHz range and the DSP technology is on pace to support software radio requirements.

2.1.4. Software defined radio architecture

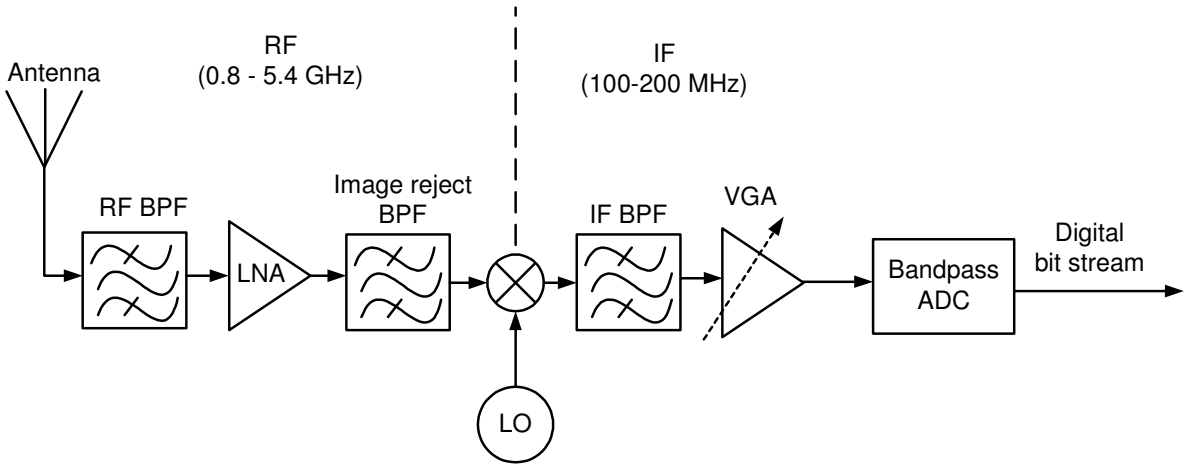


Fig. 2.6. Software defined radio (or) digital IF architecture

Software defined radio is the terminology used in literature to describe the idea of partial band digitization or intermediate frequency (IF) digitization. It is also sometimes referred to as digital radio receiver. The block diagram of a digital IF receiver architecture is shown in Fig. 2.6. The RF BPF selects the required channel(s) from the

signal appearing at the antenna. After amplification by the LNA, the signal is filtered by the image reject BPF to attenuate the components at image frequency. This operation is followed by down conversion to IF by the mixer and LO. The IF BPF further filters the signals and the VGA adjusts the signal strength to be processed by an IF bandpass ADC, which directly gives the digital output to DSP. There is no particular standard for the location of IF signals (though there are standards for location of input RF signals) and the choice of the intermediate frequency is based on the requirements of the IF circuits. The IF bandpass sampling solves flicker noise and DC offset problems which are usually present in base band ADC's. Though IF digitization has most of advantages of configuration of DSP programs, it needs additional analog components and usually supports only a single channel, with channel selection done by an analog filter.

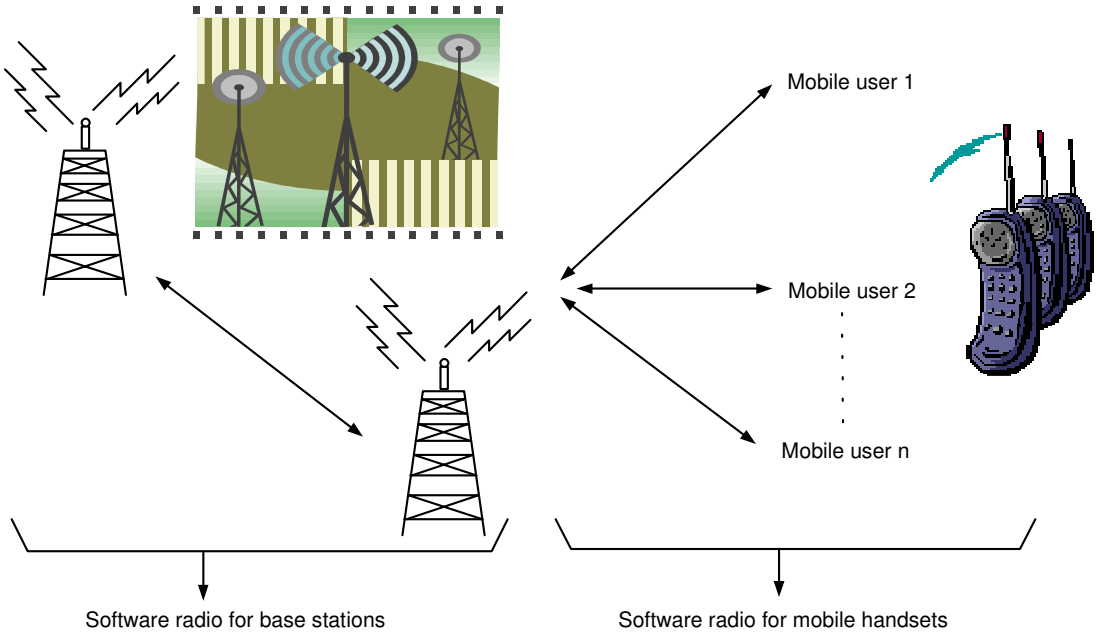


Fig. 2.7. Possible software radio implementations in wireless applications

The most common example of wireless communication application is the cell phone system. The wireless transmission coverage areas are usually divided into cells, with each cell covered by base stations. The hand sets transmit the information to the nearest base station and the signal goes through various base stations before reaching the target system. In this scenario, transmitters and receivers are required both in individual hand sets and in the base stations. A software radio receiver to support multiple standards can be implemented either in wireless base stations or in cellular handsets, as shown in Fig 2.7. Low power consumption is absolutely essential for mobile handsets, but is not a strict requirement for base stations. Large power consumption increases the temperature in base stations, and requires cooling systems to maintain a nominal temperature. The increase in temperature also raises the thermal noise floor (thermal noise is proportional to temperature), and degrades the overall signal to noise ratio (SNR). The thermal noise floor should be at the minimum level for high performance analog systems. To avoid these disadvantages, low power consumption is necessary even for chips operating in base stations.

There would be numerous benefits that would accompany the realization of a software radio architecture. The wide range of existing and new standards in the cellular and mobile marketplace has resulted in the adoption of wide range of hand set and base station architectures for different systems deployed around the world. The ability to develop and manufacture a single reconfigurable terminal, which can be configured at the final stage of manufacture to tailor it to a particular market, presents great benefits to equipment manufacturers. The mobile handset can be used worldwide if all wireless

standards, which are usually specific in one region, are supported in a single terminal. A powerful benefit of a software defined radio terminal, from the perspective of the network operator, is the ability to download new services to the terminal after it has been purchased and is operational on the network. The software radio can also guarantee compatibility between second generation and third generation networks [11]. Suppose a mobile device moves from 3G standard service area (like UMTS) to an area covered only by 2G standard (like GSM), then the device can still function if it supports both standards. This is very advantageous economically for service providers, since a large amount of money has been invested to install and maintain the base stations and the multi-standard support helps in reuse of existing infrastructure. The ability to adapt key transmission parameters to prevailing channel or traffic conditions is another important benefit of software radio. It is possible, for example, to reduce the complexity of the modulation format from 16-QAM (Quadrature amplitude modulation) to QPSK (quadrature phase shift keying) when channel conditions becomes poor, thereby improving noise immunity and decoding margin. It is also possible to adapt the channel coding scheme to prevent particular types of interference, rather than just Gaussian noise, as the device moves form one area to another. Many other parameters like data rate, channel and source coding, multiple access schemes and modulation type can be adapted dynamically to improve quality of wireless service [6]. Cognitive radio is a term used in literature to define an intelligent radio transceiver that makes use of RF spectrum dynamically based on its usage [12]. The functionality of cognitive radio encompasses

software radio together with some artificial intelligence embedded in it. A software radio solution will result in further research on intelligent radio architectures.

The main focus of this research work is to explore new design techniques at both architectural and circuit level for silicon implementation of analog to digital converters for use in software radio communication receivers. The software radio receiver, shown in Fig 2.8, is the target architecture and the ADC's are designed to operate in this framework. The RF ADC directly digitizes the RF signal after the VGA, while the IF ADC converts a frequency translated IF signal to digital output. The main goal of the design process is to obtain the maximum resolution (number of bits or SNR) for both the ADC's with minimum power consumption. The different possible ADC architectures are examined in detail next to identify the best architecture for this application.

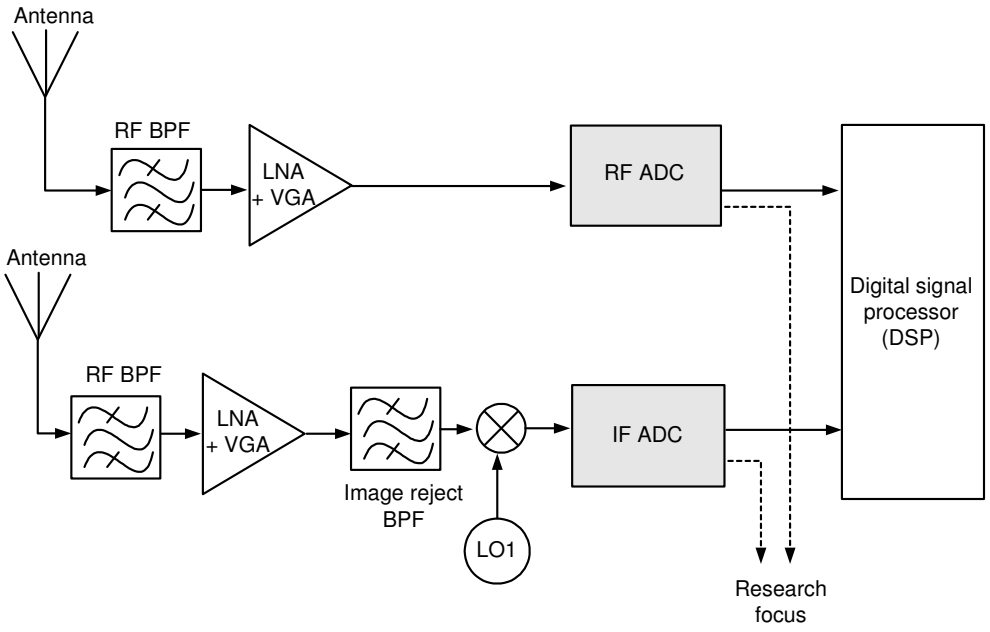


Fig. 2.8. ADC for software radio communication receivers

2.2. Overview of ADC architectures

Analog to digital converters are used to transform analog signals (continuous in time and amplitude) to digital signals (discrete in time with amplitude quantization). A generalized analog to digital conversion process is shown in Fig. 2.9. The input analog signal is sampled at a frequency F_s, which converts it into a discrete time signal. The quantizer block converts the discrete time signal into the nearest digital bit code and the encoder converts it to N-bit output code. The sampler, encoder and the quantizer blocks together form the ADC. The process of quantizing a signal is non- reversible and

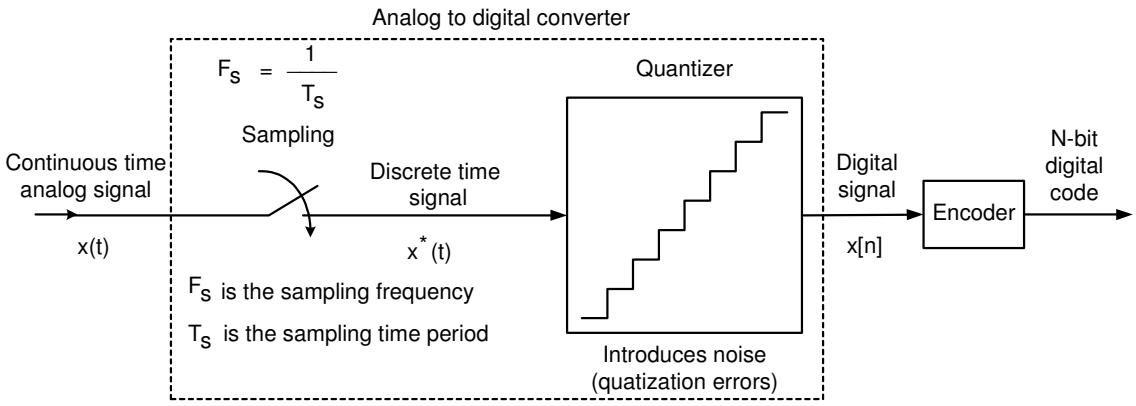


Fig. 2.9. Generalized analog to digital conversion process

it results in loss of information, usually accompanied by addition of quantization error. When the full scale voltage of value V_{FS} is applied to a N bit converter, the quantization step (Δ) is given by (V_{FS} / (2^N-1)) and the maximum quantization error is given by $\pm(\Delta/2)$. The quantization error has uniform probability density function, provided the quantization errors are sufficiently random in nature [13]. The quantization noise power

spectral density is uniformly distributed between ($-F_s/2$) and ($F_s/2$) with a magnitude of (Δ^2 /12). The main performance measure of an ADC, signal to noise ratio (SNR), is defined as the ratio of the signal power to the integrated noise power over the signal bandwidth (usually measured for a sinusoidal input). It is related to its resolution (number of bits, N) by the following equation [13]

$$\text{SNR (dB)} = 6.02*N + 1.76 \text{ dB} \qquad (2.3)$$

Another performance metric of an ADC is the dynamic range (DR), which is defined as the ratio between maximum input signal power with acceptable distortion to the minimum detectable input signal power level. A signal is said to be detectable if the signal power is just above the noise power (when SNR = 0 dB). Signal to noise + distortion ratio (SNDR) is defined as the ratio of the signal power to the sum of noise and distortion components over the required signal bandwidth. The fundamental limit of noise floor in circuits is given by the thermal noise. The quantization noise floor of the ADC is assumed to be above the thermal noise floor and therefore determines the performance of the ADC. The quantization noise usually dominates the noise floor for ADC's with narrow or small bandwidth, but for ADC's that handle large signal bandwidth, the integrated thermal noise floor limits the performance of the ADC.

The different categories of the ADC architectures based on their speed, resolution and power is shown in Fig. 2.10. The sampling frequency, number of bits and power consumption are three parameters which tradeoff with each other for all ADC architectures [14]. The flash, folding, sub-ranging and pipeline ADC architectures are in the very high speed and medium to low resolution category, while the successive

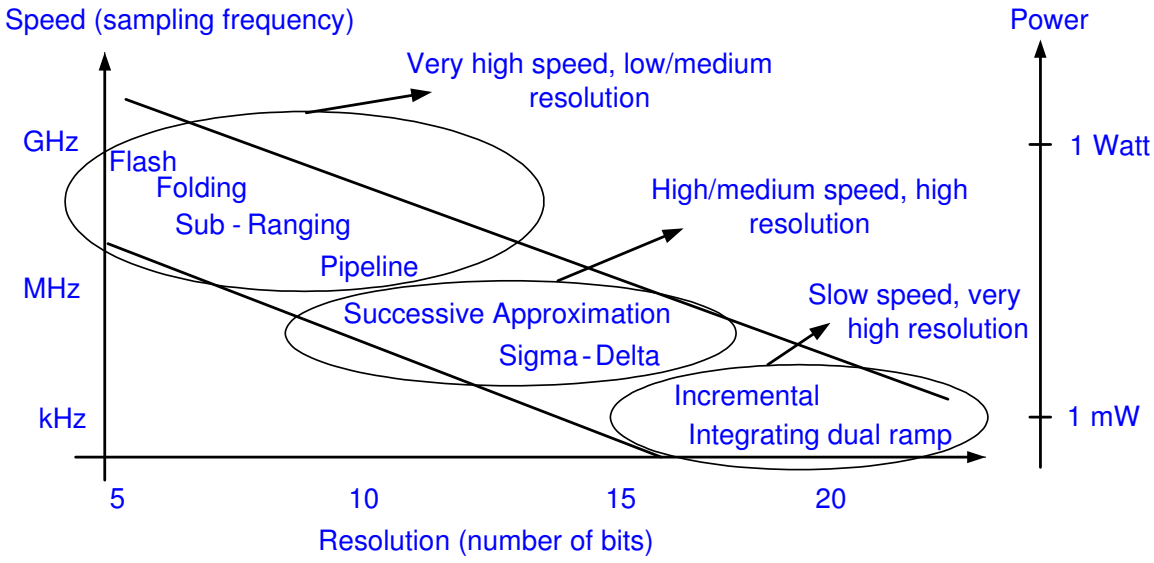


Fig. 2.10. Classification of ADC architectures based on speed and resolution

approximation and sigma-delta ADC architectures are in the high/medium speed and high resolution category. The incremental and integrating dual ramp ADC architectures fall in the slow speed and very high resolution category. The power consumption for all ADC's increases at higher sampling frequencies, and is usually in the Watt range for GHz sampling frequencies. The RF ADC for software radio would require sampling frequency in the GHz range while the IF ADC would require sampling frequency in the range of MHz. There are two broad classifications of ADC's based on the relation of their sampling frequency to the bandwidth of the input analog signal, namely Nyquist rate and oversampled ADC's. The sigma-delta ADC is the only architecture in the oversampled category, while all other architectures in Fig. 2.10 belong to the Nyquist rate category.

2.2.1. Nyquist rate analog to digital converters

The process of sampling of a continuous time analog signal x(t) at a frequency F_s (time period = T_s = $(1/F_s)$) in ADC is equivalent to multiplying the signal by impulse trains that repeat every T_s seconds. Mathematically, the sampled discrete time signal is given in time domain by

$$x^*(t) = \sum_{n=-\infty}^{+\infty} x(t)\delta(t - nT_s) \tag{2.4}$$

where n is integer and δ is the ideal impulse function. In frequency domain, the sampled discrete time signal is given by

$$X^*(f) = X(f) * \sum_{n=-\infty}^{+\infty} \frac{1}{T_s}\delta(f - n * F_s) \tag{2.5}$$

where X(f) is the Fourier transform of the signal x(t). The sampling function modulates x(t) by carrier signals having frequencies at F_s, $2F_s$, $3F_s$ ..etc and in frequency domain, this causes the spectrum of x(t) to be repeated at nF_s frequencies. The sampling process of an analog signal in time and frequency domain is shown in Fig. 2.11. When the analog signal has a band limited frequency $F_{in,}$ then it must be sampled at a rate that is greater than $2*F_{in}$ in order to avoid aliasing, where signal image components at higher frequencies fold back into the signal bandwidth. The Nyquist sampling theorem states that the sampling frequency should be at least $2*F_{in}$ in order to be able to recover the original signal perfectly from the sampled version. All Nyquist rate ADC architectures have sampling frequency of $2*F_{in}$.

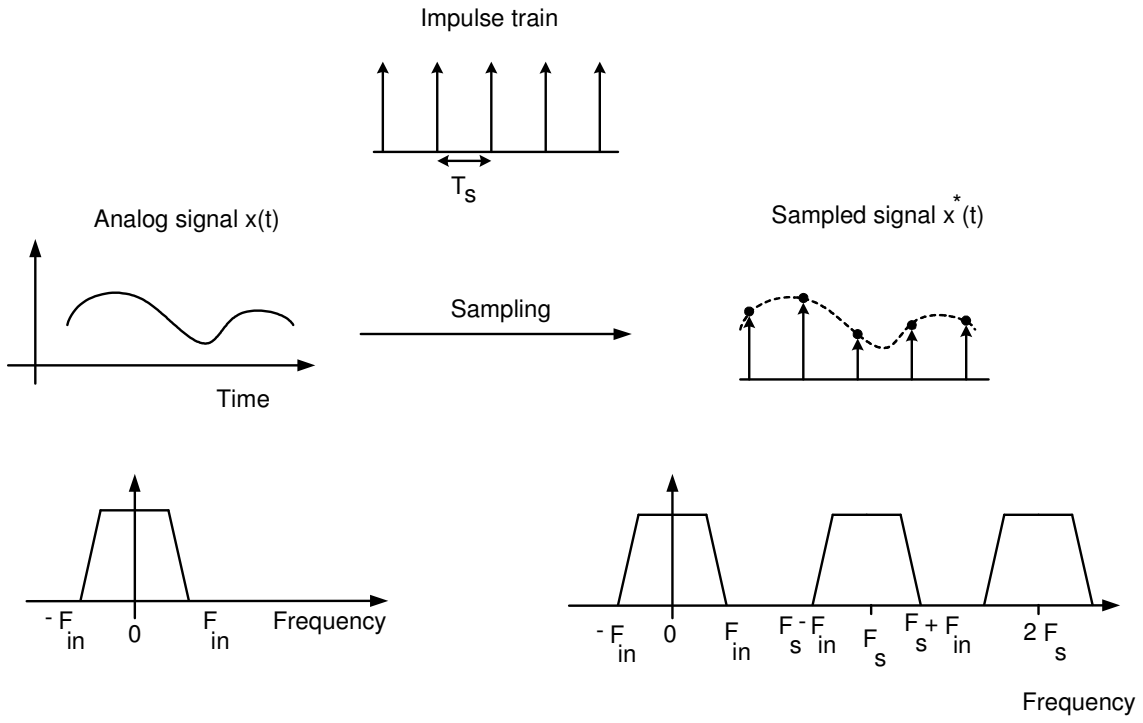


Fig. 2.11. Sampling in time and frequency domain

The general components of a Nyquist rate ADC consist of anti-alias filter (to limit the bandwidth of the input signals), sample and hold circuit and multi-bit quantizer. The quantization noise power of Nyquist rate ADC's extends in frequency from DC to $F_s/2$, as shown in Fig 2.12. The signals at the input of RF and IF ADC's are located around a center frequency and the bandwidth depends upon number of channels or standards that are required to be converted to digital output. For example, suppose the RF ADC digitizes signals of 1 MHz around 1 GHz, then the Nyquist rate ADC would have a sampling frequency of atleast 2 GHz and will digitize the entire band from DC to 1 GHz. Since there is no inherent filtering in a Nyquist rate ADC, a lot of power is wasted while trying to reduce the quantization noise in the entire Nyquist bandwidth,

which contains frequency components outside the required signal bandwidth. This disadvantage makes Nyquist rate ADC unattractive for software radio applications.

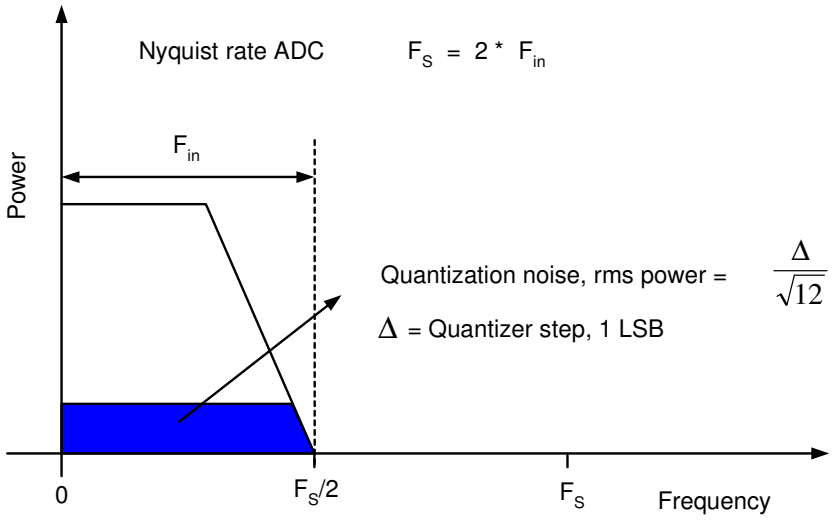


Fig. 2.12. Quantization noise in Nyquist rate converters

2.2.2 Oversampled analog to digital converters

The ADC architectures that have a sampling frequency much greater than the Nyquist sampling criterion belong to the category of oversampled ADC's ($F_s >> 2*F_{in}$, where F_{in} is the bandwidth of the input signal). The quantization noise power extends in frequency from DC to $F_s/2$ and its root mean square value is the same as that of Fig. 2.12. The main difference is that the in-band quantization noise power is reduced as compared to Nyquist rate since the same power is spread over a much greater frequency range. The oversampling ratio (OSR) of the ADC is defined as Fs/(2*Fin) and a 2x increase in sampling frequency results in 3 dB improvement of the ADC's SNR. A

sigma-delta (ΣΔ) ADC combines oversampling with noise shaping (using negative feedback loop), which greatly reduces the in-band quantization noise power and results in a high SNR within the signal bandwidth [15]. The negative feedback together with oversampling results in a SNR improvement of 9 dB (1.5 bits) for a 2x increase in the sampling frequency. The frequency spectrum of quantization noise in ΣΔ (oversampled) ADC is shown in Fig. 2.13.

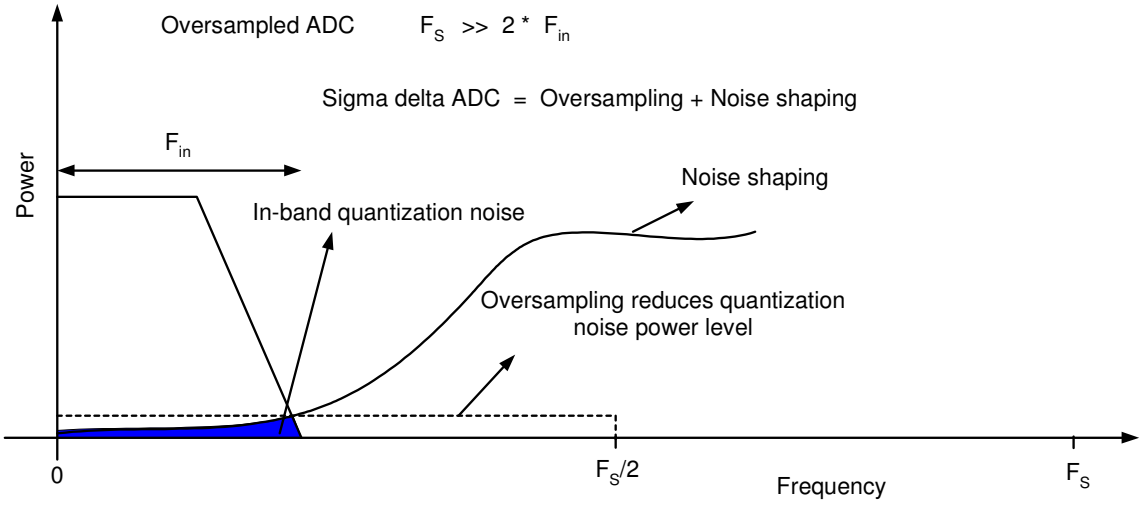


Fig. 2.13. Quantization noise in oversampled converters

The basic components of a ΣΔ ADC is shown in Fig. 2.14, and it includes a loop filter in the forward loop followed by a comparator, with a feedback digital to analog converter (DAC) completing the negative feedback loop. While considering a small signal model (a linearized model is used for the non-linear comparator block) and

assuming a unity transfer function for the DAC and comparator, the output (D_{out}) is given by

$$D_{out} = STF * V_{in} + NTF * Q_n \tag{2.6}$$

where Qn is quantization noise, STF and NTF are the signal and noise transfer functions. The STF and NTF of the ADC are given by

$$STF = \frac{D_{out}}{V_{in}} = \frac{H(z)}{1+H(z)}, NTF = \frac{D_{out}}{Q_n} = \frac{1}{1+H(z)} \tag{2.7}$$

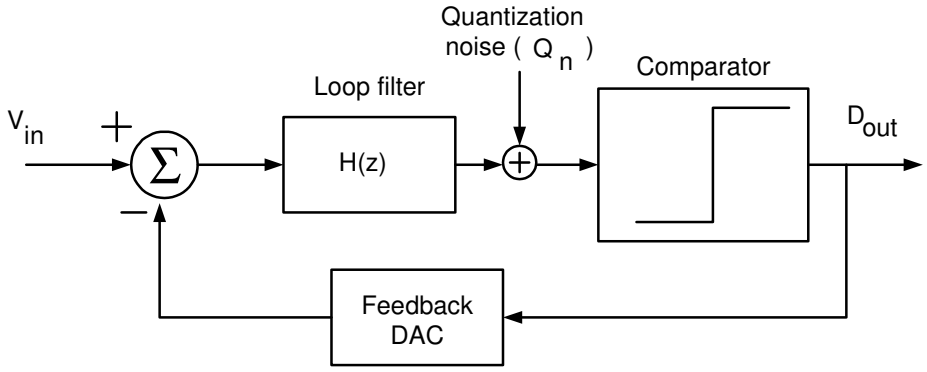


Fig. 2.14. Block diagram of a sigma-delta ADC

The digital output (D_{out}) then passes through decimation and digital filter blocks, where down sampling is performed to get the final output. The loop filter H(z) is usually implemented a low pass filter and results in a low pass ΣΔ ADC. When H(z) is a first order discrete time integrator (low pass filter), the loop filter, STF and NTF is given by

$$H_{LP}(z) = \frac{z^{-1}}{1-z^{-1}}, STF = z^{-1}, NTF = \left(1-z^{-1}\right) \tag{2.8}$$

The NTF has a zero at DC and the quantization noise is high-pass filtered at the output, while the signal is delayed by one clock cycle at the output. The low pass ΣΔ ADC's offer the advantage of high resolution in a narrow signal bandwidth, but they are still not suitable for RF/IF ADC's in Fig. 2.8 as the quantization noise is shaped over a wide range of frequencies (from DC to the signal bandwidth). The easy solution is to use a loop filter with a bandpass transfer function which results in the ideal ADC architecture for software radio application and is discussed in the next section.

2.2.3. Bandpass sigma-delta analog to digital converters

A bandpass ΣΔ ADC is obtained by replacing H(z) in Fig. 2.14 with a bandpass filter. The following general discrete time low pass to bandpass transformation may be used to obtain a bandpass filter from a low pass prototype [15].

$$z^{-1} \to -z^{-1}\frac{z^{-1}-\alpha}{1-\alpha z^{-1}} \quad -1<\alpha<1 \tag{2.9}$$

This general transformation moves the zero of the NTF from zero to an arbitrary location below the sampling frequency F_s. For the case when $\alpha = 0$, (2.9) becomes $z^{-1} \to -z^{-2}$. This transformation is widely used because it preserves the properties of the low pass modulator and it is convenient for integrated implementation. If the order of the low pass filter is n, then the transformation results in a bandpass filter of order 2n. Using this transformation, the loop filter, STF and NTF of a 2nd order bandpass ADC is given by

$$H_{BP}(z)=\frac{-z^{-2}}{1+z^{-2}}, STF = z^{-2}, NTF = \left(1+z^{-2}\right) \tag{2.10}$$

The zeros of the NTF are moved from DC to $\pm(F_s/4)$, and the STF delays the signal by two clock cycles. The quantization noise is shaped by a notch transfer function around $\pm(F_s/4)$, while the input signals have a bandpass transfer function. This noise shaping results in a high SNR in the signal bandwidth around the center frequency of the bandpass filter [16]. The oversampling ratio (OSR) for a bandpass ADC is defines as $(F_s/(2*F_{in}))$, where F_{in} is the bandwidth of the signals around the center frequency.

The analog signals that have to be digitized in software radio receivers are located at center frequency F_o (which can be at RF or IF) and the signal bandwidth is F_B. The quantization noise is attenuated only in the required signal bandwidth instead of the whole Nyquist bandwidth (DC to $F_s/2$), which implies lesser power consumption to obtain similar dynamic range as compared to a Nyquist converter. Bandpass ΣΔ ADC architecture is the best choice for digitization in software radio receivers, as shown in Fig. 2.15.

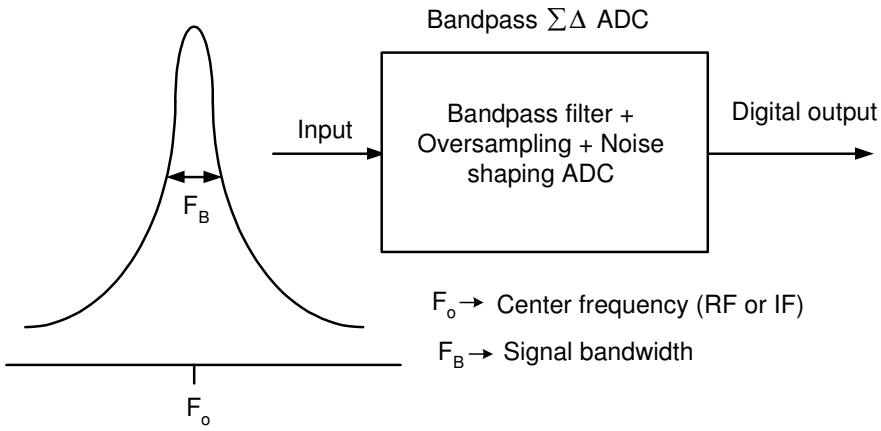


Fig. 2.15. Best ADC architecture for software radio

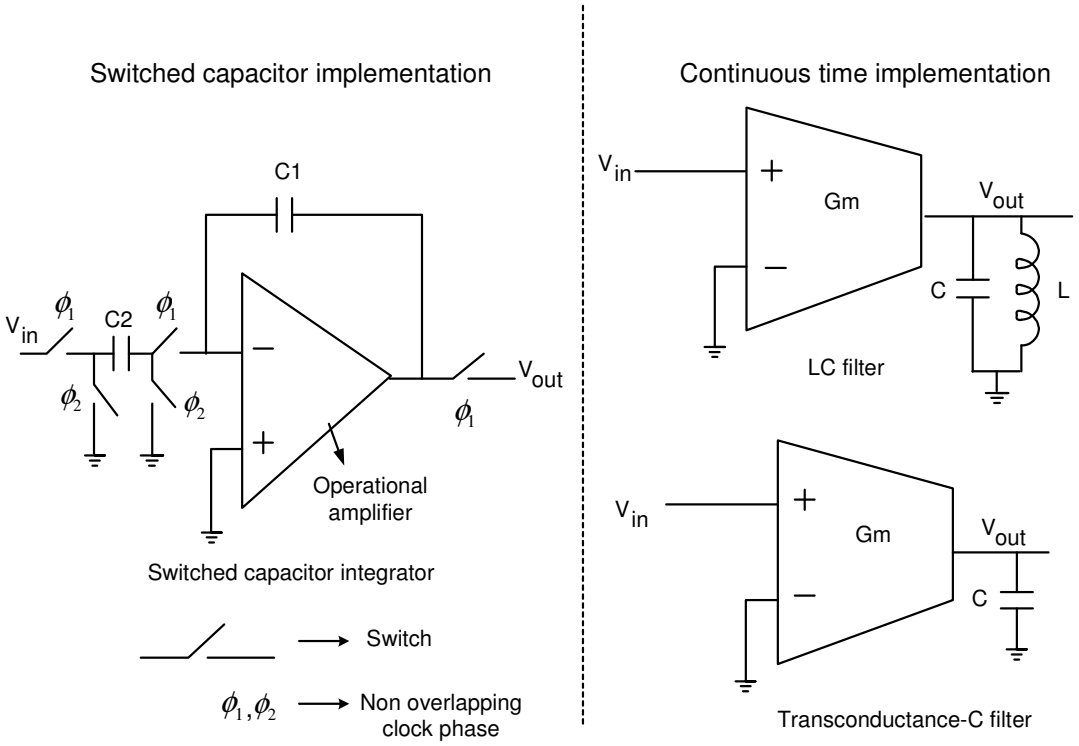


Fig. 2.16. Different implementations of integrated bandpass filters

The bandpass loop filter in ΣΔ ADC's can be implemented either in switched capacitor (discrete time) or continuous time mode, as shown in Fig. 2.16. The switched capacitor integrator (basic building block of resonator) is realized using capacitors, switches and operational amplifier with local feedback. The center frequency of a switched capacitor bandpass filter is fixed by capacitor ratios (which are very accurate) and it does not require any automatic tuning scheme. The DC gain of the amplifier should be high to guarantee proper closed loop operation of the amplifier. The switching scheme uses two non-overlapped clock phases and the amplifier should settle to the final value within one-half of the clock period. The settling time specification requires the

amplifier which is working in closed loop to have gain bandwidth (GBW) product in the range of 10-20 times the clock frequency [17]. For a clock frequency of 2 GHz, the gain bandwidth requirements would be greater than 20 GHz. The power consumption of such an amplifier would be so huge (> 5 Watts) in mainstream silicon technologies that it is almost impossible to design a system with these building block specifications. It is also difficult to combine both high DC gain and GBW in an amplifier because of contrasting design approaches. Finally, the switches that can be implemented using CMOS or BJT transistors do not operate properly at GHz sampling frequencies. Due to all these limitations, switched capacitor bandpass ΣΔ ADC's are usually not preferred above sampling frequencies of 200 MHz. To illustrate this point further, design overview and measurement results of a switched capacitor BP ΣΔ ADC which was done in the initial phase of this research is presented in the next section.

2.3. IF switched capacitor bandpass ΣΔ ADC design

Switched capacitor bandpass (SC BP) modulators widely used for direct digitization of narrowband signals around an intermediate frequency in a radio receiver. The main emphasis of research in bandpass ΣΔ ADC's is to increase the center frequency with a negligible increase in power consumption. The maximum achievable center frequency is directly related to the clock frequency, which is typically limited by the speed of the switched capacitor integrator. Various architectural level techniques such as two-path architecture [18], double sampling resonator [19], double sampling with pseudo two paths [20] and double delay resonator [21] have been proposed to

improve the effective clock frequency of SC BP ΣΔ modulators. These architectural techniques relax the requirements of the amplifier performance. The limitations of switched capacitor circuits are examined and a compensation technique is proposed to improve the speed of the amplifier. The amplifier is used in the design of a high speed SC BP ΣΔ ADC.

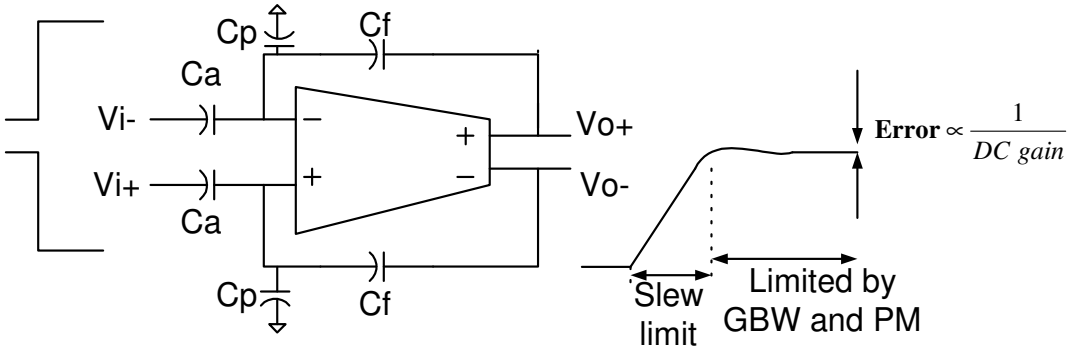


Fig. 2.17. Closed loop operation of a switched capacitor integrator

The SC integrator is the basic building block of a SC resonator (bandpass filter) and the overall speed of the filter is determined by the settling performance of the SC integrator. A switched capacitor (SC) integrator in feedback operation during the integrating clock phase is shown in Fig. 2.17. The closed loop transfer function during the integrating phase is given by

$$\frac{V_0}{V_i} \cong \frac{\alpha A_{v0}\omega_p}{s+(1+\beta A_{v0})\omega_p} \tag{2.11}$$

where

$$\alpha = \frac{C_a}{C_a + C_f + C_p} \ , \beta = \frac{C_f}{C_a + C_f + C_p} \qquad (2.12)$$

α is the feed forward factor, β is the feedback factor, A_{v0} is the open loop DC gain of the amplifier, ω_p is the dominant pole of the open-loop amplifier, C_p is the sum of all parasitic capacitances at the input node of amplifier and C_a ,C_f are the input and feedback capacitors. Assuming an amplifier with an equivalent single pole response, as shown in (2.11), the output step response of the SC integrator after the slewing phase is given by

$$V_{out}(t) = -\left(\frac{\frac{C_a}{C_f}}{1 + \frac{1}{\beta A_{v0}}} \right) \left(1 - e^{-\beta . \omega_{GBW} . t}\right) V_{in} + V_o(t_0) \qquad (2.13)$$

where ω_{GBW} ($=A_{v0}\omega_p$) is the open-loop gain-bandwidth product of the amplifier and $V_o(t_0)$ is the initial condition at the output node. The amplifier's settling consists of two phases: slew rate and linear settling dictated by the ω_{GBW} and phase margin of the amplifier [22]. The error in the final settling is inversely proportional to amplifier's DC gain and speed in the linear region is determined by ω_{GBW}. For a good settling performance, the amplifier must have a high gain along with high ω_{GBW} and good phase margin. The exponential term in (2.10), $\beta\omega_{GBW}$, should be large such that the output settles properly within one-half of the clock period (T_{clock}). For the worst case operating condition of the SC integrator and a clock frequency of 100 MHz, the amplifier f_{GBW} should be greater than 980 MHz and 1.3 GHz for a settling accuracy of 0.25 % and 0.033%, respectively. Assuming that the system settles properly within the integrating

phase, the settling error is ultimately determined by the factor βA_{v0}. For a settling error below 0.1 %, βA_{v0} must be greater than 60 dB; hence for β around 0.2 (-14 dB), A_{v0} must be greater than 74 dB for good settling performance.

It is difficult to design an amplifier with both high gain and GBW because of contradicting design requirements. High gain amplifiers use cascode and multi-stage architectures, low bias currents and long channel devices, whereas high bandwidth amplifiers use single-stage architectures, high bias currents and short channel devices [23]. Two basic approaches for designing a high gain amplifier are cascode or vertical approach and cascade or horizontal approach. The signal swing in cascode amplifiers is constrained by the power supply voltage, which is a problem for low voltage designs. In cascaded amplifiers, each amplifier stage contributes a pole. Traditional Miller compensation schemes trade bandwidth for stability. The No Capacitor Feed Forward (NCFF) compensation scheme [24] has been proposed to overcome the limitations of Miller compensation schemes. A feedforward path, which has the same phase shift as the direct path, produces a left half plane (LHP) zero. The positive phase shift of LHP zero is used to cancel the negative phase shift of pole, resulting in a good phase margin. This scheme shows a great improvement in bandwidth, along with a high gain and good phase margin. The schematic of the differential amplifier designed in TSMC 0.35 technology using the NCFF compensation scheme is shown in Fig. 2.18. The post-layout simulations of the amplifier show DC gain of 80 dB, GBW of 1.4 GHz, phase margin of 62° and a 0.1% settling time of 2 ns while consuming 4.6 mA of current from a ± 1.25V power supply.

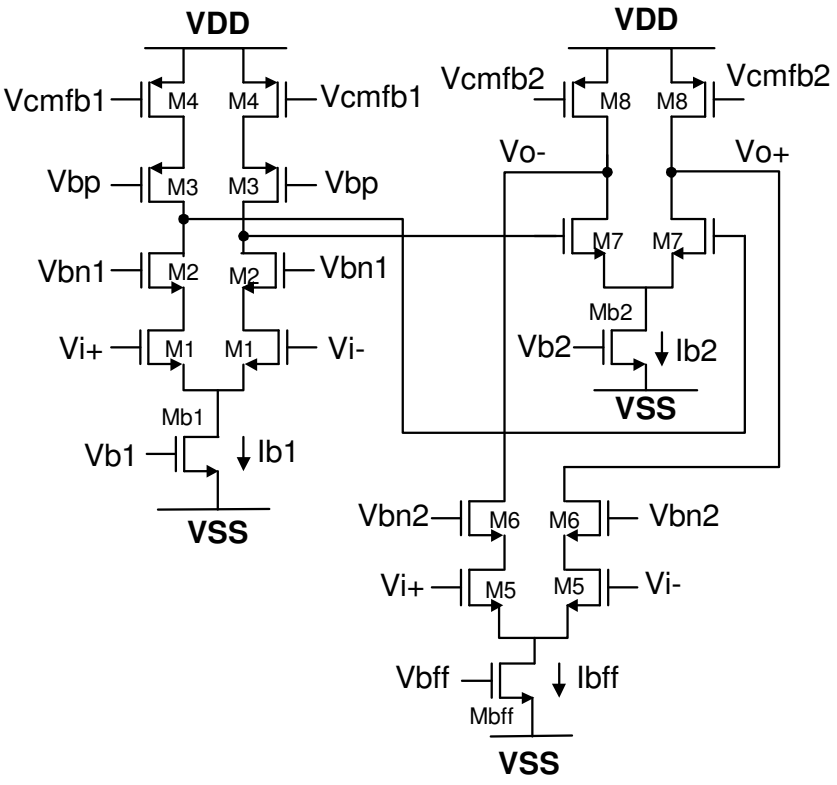


Fig. 2.18. Schematic of the differential amplifier using NCFF compensation scheme

The architecture used for the modulator's implementation is a fourth order cascade of resonators in feedback (CRFB) [25]. The center frequency is located at ¼ of the sampling frequency, for ease of digital demodulation. The coefficients are optimized based on tradeoff between signal swing in the internal nodes, capacitance spread and the maximum SNR attainable with stable operation. The value of capacitor in the first stage is important as its kT/C noise contribution dominates the overall noise performance. The out of band gain of the noise transfer function (NTF) is an important parameter for stability; in this design, this parameter is chosen to be 1.5, giving some margin for PVT variations. Simulations were done in Simulink and Matlab to verify the stability of the

Table 2.1 Coefficient values for the CRFB architecture

Coefficients	Value
a1,a2,a3,a4	-0.3122, 0, 0.5316, 0.5316
b1,b2,b3	-0.25, 0.25, 0.125
c1,c2,c3	1, 1, 1
g1,g2	2, 2

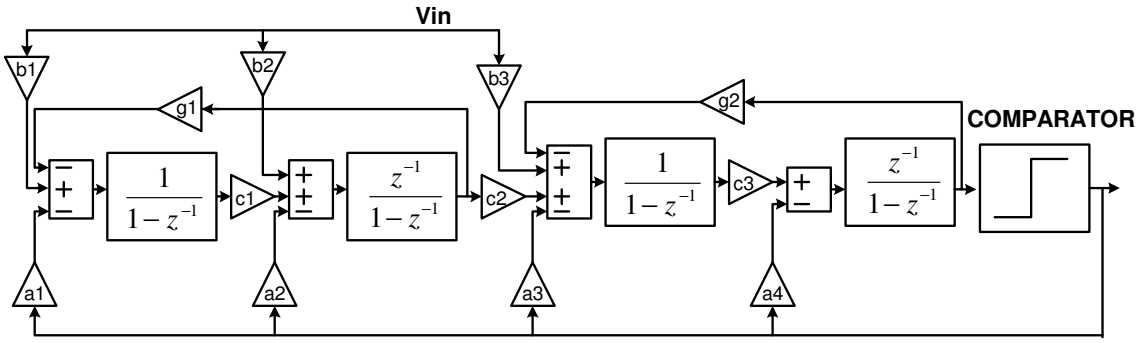


Fig. 2.19. Block diagram of the CRFB architecture for the SC modulator

architecture over typical component variations. The block diagram of the architecture is shown in Fig. 2.19 and the optimized coefficients used in the modulator implementation are given in Table 2.1. Switches are implemented using only NMOS transistors with a boosted clock voltage to reduce the switch resistance. The comparator is a two–stage structure, with a low gain first stage followed by a latch. A single-bit DAC is used to feedback the digital output; the reference voltage used was 0.25 V.

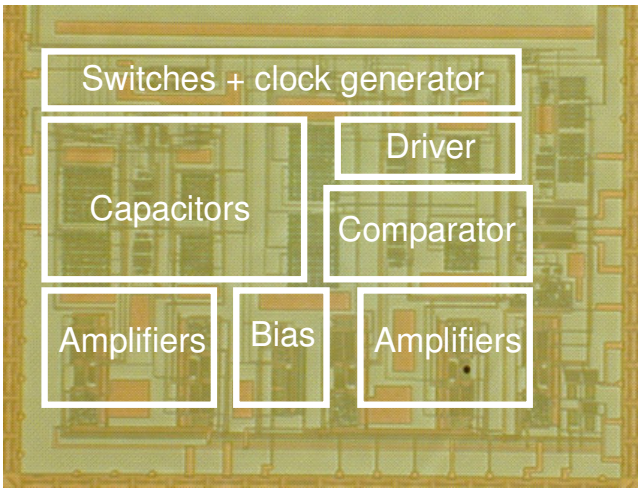


Fig. 2.20. Microphotograph of the switched capacitor bandpass ΣΔ ADC

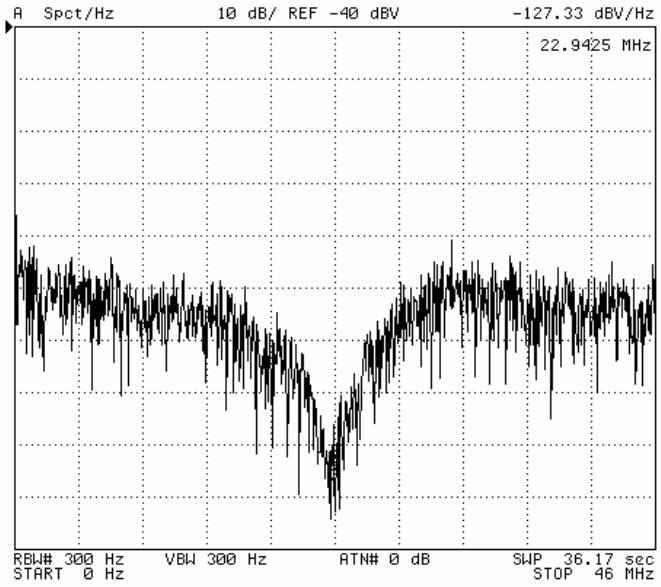


Fig. 2.21. Measured noise transfer function of the SC ADC

The microphotograph of the SC BP ΣΔ ADC designed in TSMC 0.35 µm CMOS technology is shown in Fig. 2.20 and it occupies an area of 1.25 mm^2 . The bandpass modulator was characterized by directly injecting the output digital bit stream into a

spectrum analyzer. The clock frequency is at 92 MHz and the IF signal is at 23 MHz. The NTF of the modulator measured by grounding the inputs is shown in Fig. 2.21. The noise floor of the modulator is at –127 dB. This level is determined not only by the noise shaping of the sigma-delta modulator and thermal noise of the transistors, but also the noise added to the digital levels (from noisy supply voltages) since the output is directly injected into the spectrum analyzer.

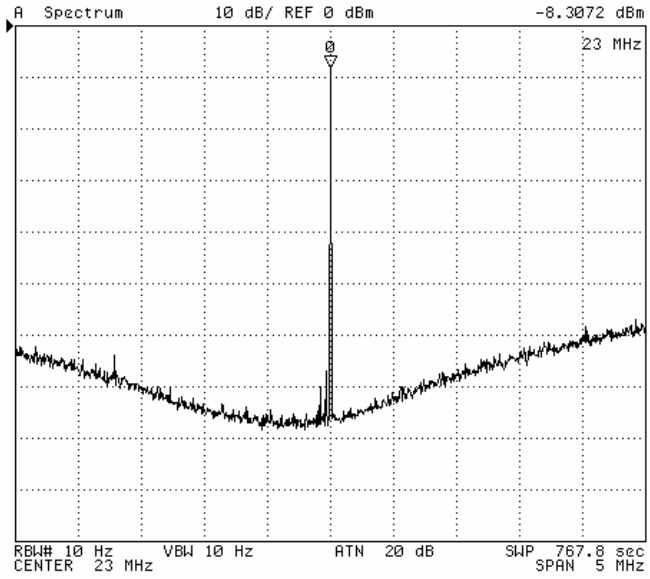


Fig. 2.22. Output spectrum of the SC ADC for 5 MHz span

The output spectrum of the ADC for 5 MHz span with a single tone input at 23 MHz is shown in Fig. 2.22. The noise level increases mainly due to the noise contribution of the signal generators used. The two-tone test for signals 200 kHz apart in the band (22.9 MHz and 23.1 MHz) are shown in Fig. 2.23. IM3 is less than –58 dB for two-tone input signals, each at -11 dBr (normalized with respect to the reference voltage of 0.25 V).

The peak SNR of the modulator was 80 dB and 54 dB for bandwidth of 270 KHz and 3.84 MHz, respectively. The plot of SNR of ADC for various input values is shown in Fig. 2.24. The modulator consumes 47.5 mW of from ± 1.25 V power supply.

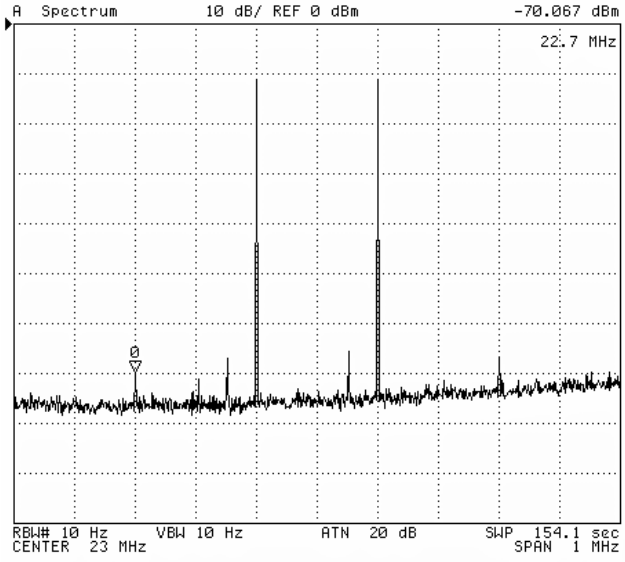


Fig. 2.23. Two tone IMD test for -11 dBr input signal

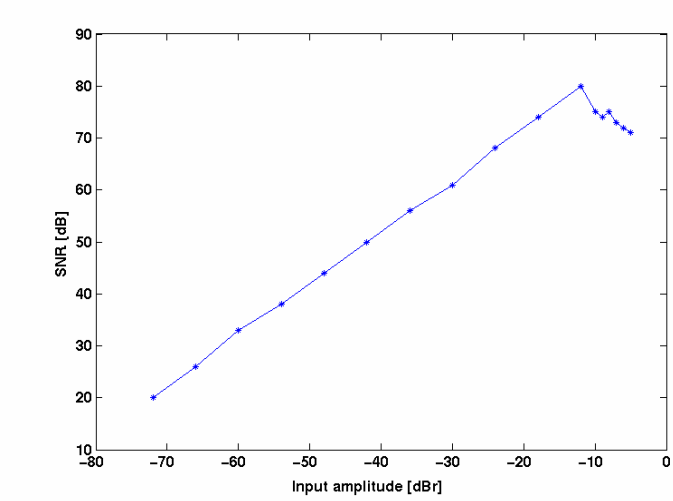


Fig. 2.24. Plot of SNR vs input amplitude for 270 kHz bandwidth

The measurement results of the ADC show that high performance IF digitization can be implemented using SC BP ΣΔ modulators. The maximum clock frequency is limited by the amplifier requirements and for implementations with more advanced CMOS technologies cannot exceed 200 MHz for high SNR performance. The linearity of the switches degrades at high clock frequencies and limits the maximum speed of operation of the system.

2.4. Literature survey

Continuous time filters such as transconductance-C and LC filter do not have stringent requirements on DC gain and GBW requirements of amplifier as compared to the switched capacitor filters. For ex, Operation transconductance amplifiers (OTA) or gm-cells used in continuous time filters usually require GBW to be the same value as the sampling frequency. The relaxed requirements help in implementing a continuous time filter with lower power consumption at higher signal frequencies, which is one of the main reasons why continuous time bandpass filters are preferred over switched capacitor filters. Continuous time bandpass (CT BP) ΣΔ ADC's offer many advantages for low power digitization in software radio communication receivers and will be used for both the RF/IF ADC implementations in this research. A brief survey of bandpass ADC's that have been reported in literature for RF/IF digitization in communication receivers is shown in Table 2.2 [26]-[35]. The first five entries in the table are ADC's which perform direct RF digitization (input signals are from 0.8 to 1.3 GHz) and other ADC's perform IF digitization (input signals are from 90 MHz to 200 MHz).

Table 2.2. Literature survey of RF/IF bandpass ADC's

Ref	Type	Center freq (GHz)	Clock freq (GHz)	SNR @ BW= 1 MHz*	Power (mW)	Technology
[26]	4th order CT BP ΣΔ	1.3	4.3	62 dB	6200	InP HBT
[27]	4th order CT BP ΣΔ	1	4	59 dB	350	0.5 µm SiGe
[28]	4th order CT BP ΣΔ	1	4	50 dB	450	0.5 µm SiGe
[29]	2nd order LP-ΣΔ & mixer	0.9	0.1	25 dB	30	0.25 µm CMOS
[30]	4th order CT BP ΣΔ	0.8	3.2	55 dB	1800	GaAs
[31]	4th order CT BP ΣΔ	0.2	4	78 dB	3500	InP HBT
[32]	4th order CT BP ΣΔ	0.2	0.8	61 dB	64	SiGe Bipolar
[33]	4th order CT BP ΣΔ	0.18	4	76 dB	3200	GaInAs HBT
[34]	4th order CT/DT BP ΣΔ with mixer	0.1	0.4	47 dB	330	0.35 µm CMOS
[35]	10th order CT BP ΣΔ	0.09	2.5	87 dB	6000	InP HBT

*SNR is extrapolated to 1MHz BW when reported for other bandwidths

From Table 2.2, it is clear that continuous time bandpass (CT BP) ΣΔ ADC is the dominant choice of architecture for both RF and IF A/D conversion. The RF ADC's with sampling frequencies in the GHz range (3.2 – 4.3 GHz) have been implemented in SiGe, InP, and GaAs technologies. A switched-capacitor CMOS low pass ΣΔ ADC with an

integrated mixer is reported in [29] and in spite of low power consumption, it has limited signal to noise + distortion radio (SNDR) because it has a mixer integrated in the loop and all harmonics from the mixer directly appear at the digital output. Subsampling is another technique that has been proposed for RF A/D conversion, but it has the disadvantage of poor SNDR due to aliasing of high frequency components into the signal bandwidth [36]. The power consumption of the reported RF ADC's is high (from 0.45 to 6.2 watts) for obtaining good resolution (> 10 bits). The IF ADC's with sampling frequencies in the GHz range (0.4 – 4 GHz) have been implemented in SiGe, InP, GaInAs and CMOS technologies with high power consumption.

The main drawback of the high resolution ADC's in Table 2.2 is that they have large power consumption, which makes them unsuitable for use in portable wireless devices. The main aim of this research is to explore new design techniques for RF/IF continuous time bandpass sigma-delta ADC's to obtain good SNR performance with low power consumption.

CHAPTER III

OVERVIEW OF CONTINUOUS TIME BANDPASS SIGMA-DELTA ANALOG TO DIGITAL CONVERTERS

3.1. Introduction

The block diagram of a continuous time bandpass sigma-delta (CT BP ΣΔ) ADC is shown in Fig. 3.1. The loop filter is a N^{th} order continuous time bandpass filter and the comparator together with the DAC completes the feedback path. The center frequency of the bandpass filter is f_o, and the input signals with bandwidth f_{in} is located around the

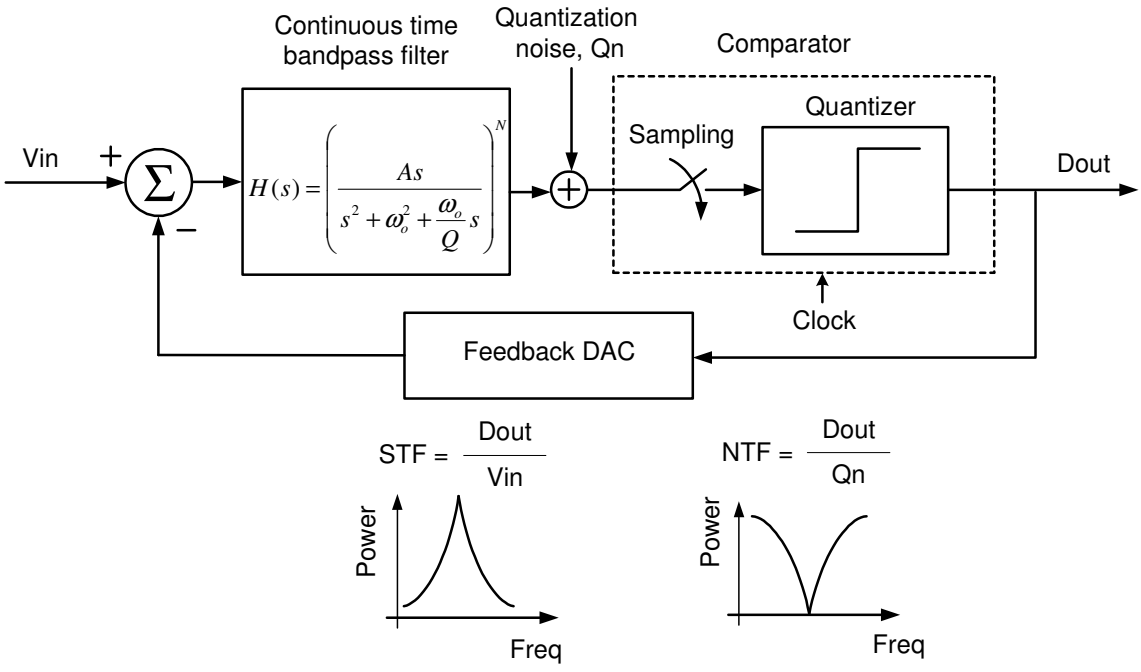
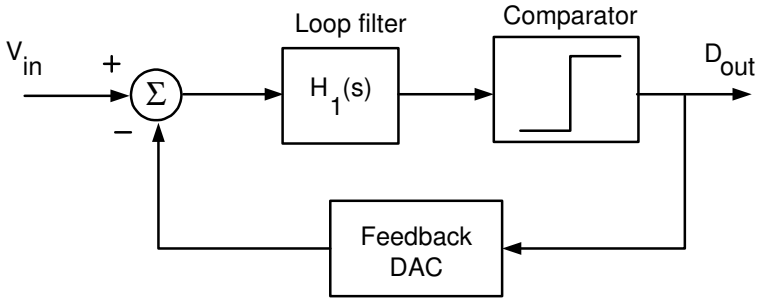


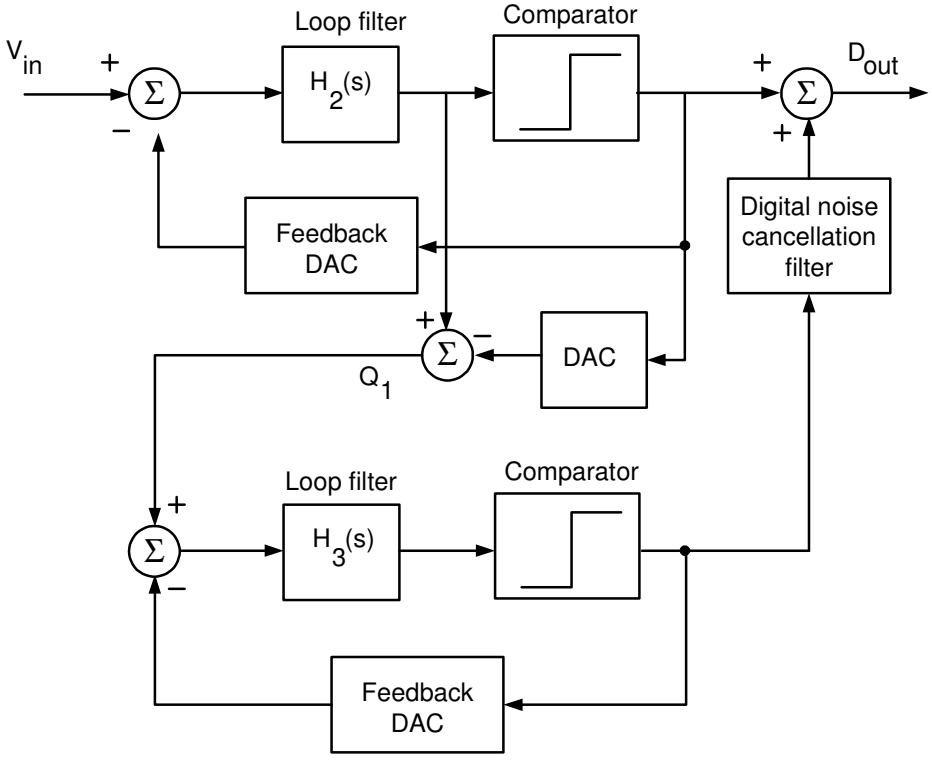
Fig. 3.1. Block diagram of a continuous time bandpass ΣΔ ADC

center frequency. The negative feedback loop causes the quantization noise (assumed to be injected at the comparator input) to have a notch transfer function around f_o, while the signals have a bandpass transfer function. The comparator is the only discrete-time block, while the filter and DAC's are continuous time blocks. The sampling operation occurs inside the loop and the loop filter provides inherent anti-alias filtering of the input signals, which is one of the main advantages of a CT BP ΣΔ ADC, along with low power consumption and higher frequency of operation [37].

The main design considerations for CT BP ΣΔ ADC are choice of architecture, order and type of continuous time loop filter, clock frequency and resolution of the comparator. The two most common architectures are single loop and MASH (multi stage noise shaping, also called cascaded) ΣΔ ADC. The block diagram of a generic single bit and a cascaded ΣΔ ADC architecture is shown in Fig. 3.2. The single loop architecture, as the name suggests, has only one feedback loop with a loop filter ($H_1(s)$) and they have a very simple implementation. However, single loop ΣΔ ADC's with higher order loop filters (order > 2) exhibit unstable behavior [15]. The signal swing at the output of the filter increases when a higher order filter is used and can saturate the input node of the comparator. This condition is called comparator overload and causes the digital output to stay at a constant logic value. When this condition occurs, the negative feedback loop is disabled and the ADC operates in open loop, which causes potential stability problems. A cascaded ΣΔ ADC architecture, shown in Fig. 3.2 (b), overcomes the stability problem by using a cascade of lower order filters (in this case $H_2(s)$ and $H_3(s)$), which achieves an equivalent higher order ADC while maintaining the signal swing at all internal nodes.



(a) Single loop architecture



(b) Cascaded loop architecture

Fig. 3.2. Block diagram of single loop and cascaded ΣΔ ADC architecture

The quantization noise of the first stage (Q_1) is calculated and is given as input to the cascaded second stage. The output of the second stage is added to the first stage after

being processed by a digital noise cancellation filter. The main disadvantage of multi-stage architecture is that it is very sensitive to mismatch of filter transfer functions [15]. The digital noise cancellation filter has to be matched perfectly with the analog loop filters ($H_2(s)$ and $H_3(s)$) and a slight mismatch causes a considerable reduction in the SNR performance. The strict matching requirement becomes more difficult to implement at high operating frequencies, which restricts the use of cascaded architectures to low clock frequencies (< 100 MHz).

The choice of the order of the loop filter, clock frequency and the comparator resolution affect the SNR of the ADC. The SNR of a generic N^{th} order, single loop bandpass ΣΔ ADC is given by [38]

$$SNR_{\max} = 10 * \log_{10}\left(\frac{1.5(N+1)OSR^{(N+1)}}{\pi^N}\right) + 6.02(B-1)\ \ dB \qquad (3.1)$$

where OSR is the oversampling ratio (OSR = f_s / (2*f_{in}); f_s is the clock frequency, f_{in} is the bandwidth of the input signal) and B is the number of bits in the comparator. The order of loop filter determines the overall order of the modulator (N in (3.1)) and SNR increases for a high order loop filter. The OSR of the ADC can be increased by increasing the clock frequency, which results in a higher SNR according to (3.1). The SNR of the ADC increases by 6 dB for a 1 bit increase in the comparator resolution, which is evident from (3.1). The disadvantages of using a multi-bit comparator is that it results in higher power consumption together with increased accuracy requirements for the DAC in the feedback loop. The linearity of the multi-bit DAC in the feedback path has to be in the same order as the required SNR at the ADC output. A one bit DAC is

inherently linear, while an elaborate dynamic element matching (DEM) scheme is requited to obtain the desired linearity for a multi-bit DAC [15]. The different types of possible continuous time loop filter implementations include transconductor-C (gm-C), LC and active-RC filters. The choice of the type of loop filter depends upon various factors such as frequency of operation, power consumption and ease of on-chip implementation of the required building blocks.

A brief review of the main design issues of a CT BP ΣΔ ADC is presented in this chapter, followed by discussion of the main non-idealities and their impact on the ADC performance. A comprehensive overview of the design procedure and a detailed analysis of the non-idealities in a CT BP ΣΔ ADC is presented in [37] and the readers are encouraged to read the book for further understanding of the concepts. The main advantages and drawbacks of CT BP ΣΔ ADC architecture that have reported in literature for RF digitization is presented in the last section.

3.2. Discrete time ADC equivalence

The analysis of a CT BP ΣΔ ADC is not straightforward since it requires both continuous and discrete time domain techniques for its full description. The analysis becomes easy when a CT BP ΣΔ ADC can be transformed into equivalent switched capacitor (SC) BP ΣΔ ADC, since there exists many design tools and techniques to design SC architectures [37]. The equivalence between a discrete time and continuous time ΣΔ ADC is illustrated in Fig. 3.3. The main difference between the two architectures is that signal is sampled right at the input for a SC ΣΔ ADC, whereas the

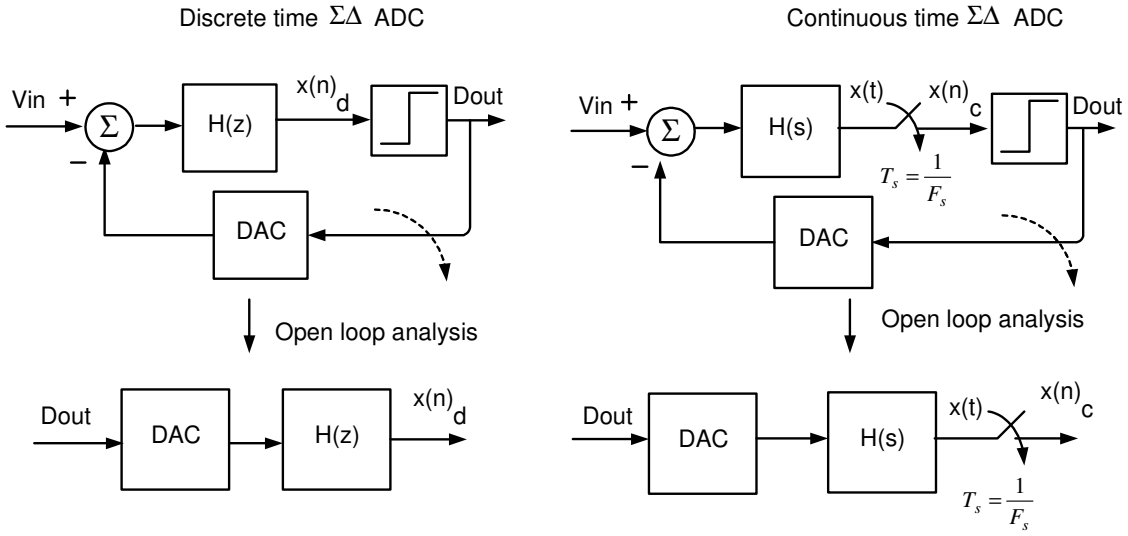


Fig. 3.3. Open loop equivalence of continuous and discrete time ΣΔ ADC

signal is sampled inside the loop before the comparator in a CT ΣΔ ADC. The two ADC architectures are equivalent if the output bit stream is the same when the same inputs are applied at their inputs, which can be guaranteed when the input to the two comparators are same at the sampling time instants every clock period ($x(n)_d = x(n)_c$).

The open loop structure for both ADC's is obtained by breaking the feedback loop at the DAC inputs, as shown in Fig. 3.3. The value of $x(n)_c$ is obtained by sampling x(n), and condition for equivalence is given by

$$x(n)_d = x(t)|_{t=nT_s} \tag{3.2}$$

This can be guaranteed if the impulse response of both the open loop structures is same at the sampling time instants. In frequency domain, it can be expressed as

$$Z^{-1}\left[H(z)\right] = L^{-1}\left[R_{dac}(s)H(s)\right]|_{t=nT_s} \tag{3.3}$$

L^{-1} and Z^{-1} are the inverse Laplace and inverse Z transforms. In time domain, the equivalence is given by

$$h(n) = \left[r_{dac}(t) * h(t)\right]|_{t=nT_s} \tag{3.4}$$

where h(n), $r_{dac}(t)$ and h(t) are impulse responses of H(z), DAC and H(s), respectively. This transformation between CT and DT domain is called impulse invariant transformation as they require the open loop impulse responses to be similar [39]. The first step in the design procedure is to identify a SC BP ΣΔ ADC architecture which gives the desired SNR with stable performance. This helps in identifying H(z) and DAC coefficients for the discrete time modulator. Then, H(s) and DAC coefficients in time domain can be obtained by using (3.3) and the properties of both the structures (like dynamic range, stability etc) are the same because of the impulse invariant transformation.

3.3. DAC pulse shapes

The choice of the DAC pulse shape is an important design consideration in the design of a CT BP ΣΔ ADC as it affects most of the important performance metrics of the modulator. The different types of DAC pulse shapes that can be used in the modulator are shown in Fig. 3.4. The non return to zero (NRZ) DAC pulse has a transition (from high to low or vice versa) only when there is a change in the polarity of the comparator output. During the clock cycles when there is no change in the bit polarity, the previous value of the bit stream is maintained in a NRZ DAC pulse stream.

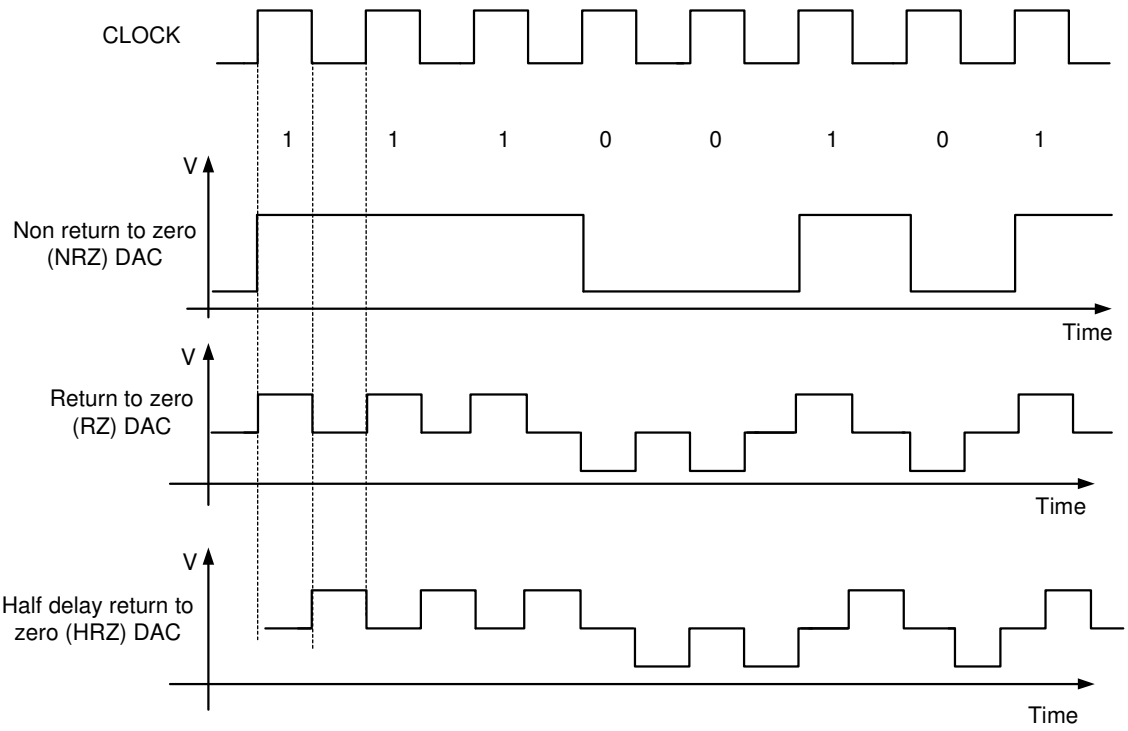


Fig. 3.4. Different types of DAC pulse shapes

The return to zero (RZ) DAC pulse has the value of the bit (low or high) for half a clock period and returns to zero value for the other half of the clock period. The half return to zero (HRZ) exhibits the same behavior as RZ pulse with the difference that it is shifted in time by ½ of the clock period.

The loop transfer function depends on the type of DAC pulse shape, which is evident from the $R_{dac}(s)$ term in (3.3). The NTF of a CT BP ΣΔ ADC is determined by the type of the DAC pulse shape and it plays an important role in determining the ADC performance. The representation of the different DAC pulse shapes in time domain and frequency domain is shown in Fig. 3.5. The conceptual difference between the DAC pulse shapes is the fraction of clock period for which current (charge) is injected back to

the loop filter. The type of DAC pulse also affects the non-idealities of the modulator and is explained in detail in the next section.

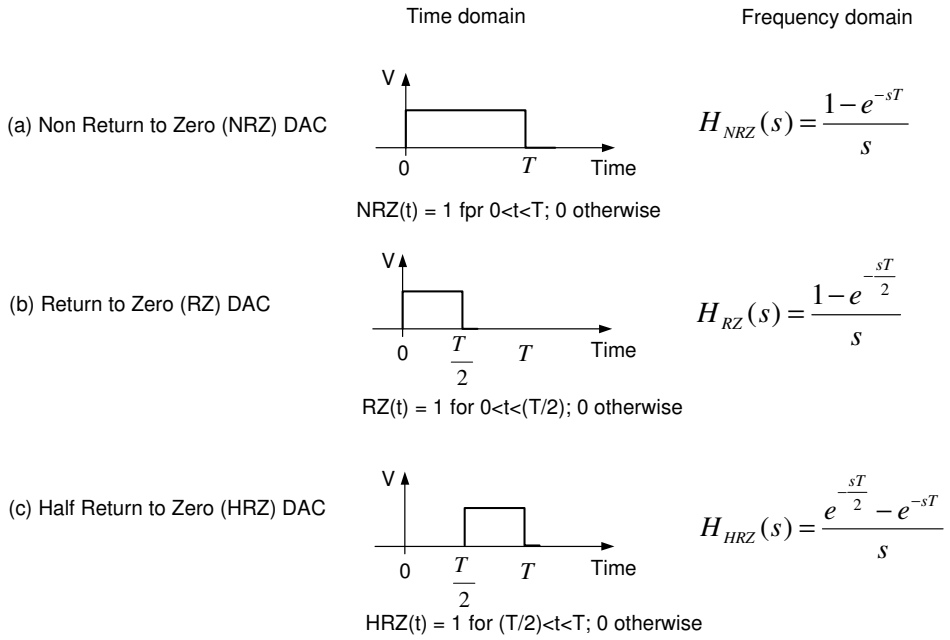


Fig. 3.5. Representation of DAC pulses in time and frequency domain

3.4. Non-idealities of continuous time bandpass ΣΔ ADC

The transfer function of the quantization noise (notch function) is degraded by non-idealities in a CT BP ΣΔ ADC which results in an increase in the integrated noise power over the required signal bandwidth and a decrease in SNR at the ADC output. The non-idealities also results in distortion components, which reduces the dynamic range of the ADC. The non-idealities may also lead to loss of stability in certain cases (clipping in the internal nodes), which makes it necessary to take the non-idealities into account during the design process.

3.4.1. Clock jitter

The ideal clock signal is periodic in nature with consecutive rising and falling edges separated in time from each other by exactly Ts seconds. There are many non-idealities (noise, bandwidth limitations etc.) which cause the clock signal to deviate from ideal behavior and the clock edges occur at time instants of [n*Ts ± t_j] seconds (n is an integer). The deviation of edges from ideal behavior every cycle (± t_j seconds) is known as clock jitter and it is usually specified as rms (root mean square) value by considering the jitter samples over a large number of clock cycles. The clock jitter causes an error in the sampling time and it is reflected in the ADC output as a noise component, similar to the quantization noise. When the noise component due to jitter is uncorrelated with quantization noise, then their noise power add directly and raises the noise floor at the ADC output. As the clock sampling frequency increases, clock jitter becomes an increasing fraction of the time period and becomes the dominant limit in the SNR performance of the ADC's. A simple analytical formula was derived in [40] for a Nyquist rate ADC, where the maximum number of bits achievable considering only jitter error is given by

$$B_{\max,jitter\_Nyquist} = \left[\log_2 \left(\frac{2}{\sqrt{3}\pi f_{clock} \tau_j} \right) - 1 \right] bits \qquad (3.5)$$

where f_{clock} is the clock frequency and τ_j is the rms value of clock jitter.

Clock jitter raises the in-band noise floor of CT BP ΣΔ modulators, similar to the effect of Nyquist rate ADC's. At high sampling frequencies, the in-band noise component due to jitter has a flat spectral shaping (white noise) and the advantages of

noise-shaping are absent. The edge of DAC current pulses which are fed back to the loop filter vary in time due to clock jitter and the clock jitter noise undergoes a similar transfer function as the signal (especially for the DAC connected to the first stage), which causes the jitter noise to directly appear at the ADC output. The effects of clock jitter for the different DAC pulse shapes in shown in Fig. 3.6. The clock jitter causes a small error every cycle during rising or falling clock edges and the power of the error term depends on the rms value of clock jitter (σj). The error term due to NRZ is much lower than the error term due to RZ/HRZ DAC's and is evident from the sum of the shaded areas for both the cases in Fig. 3.6.

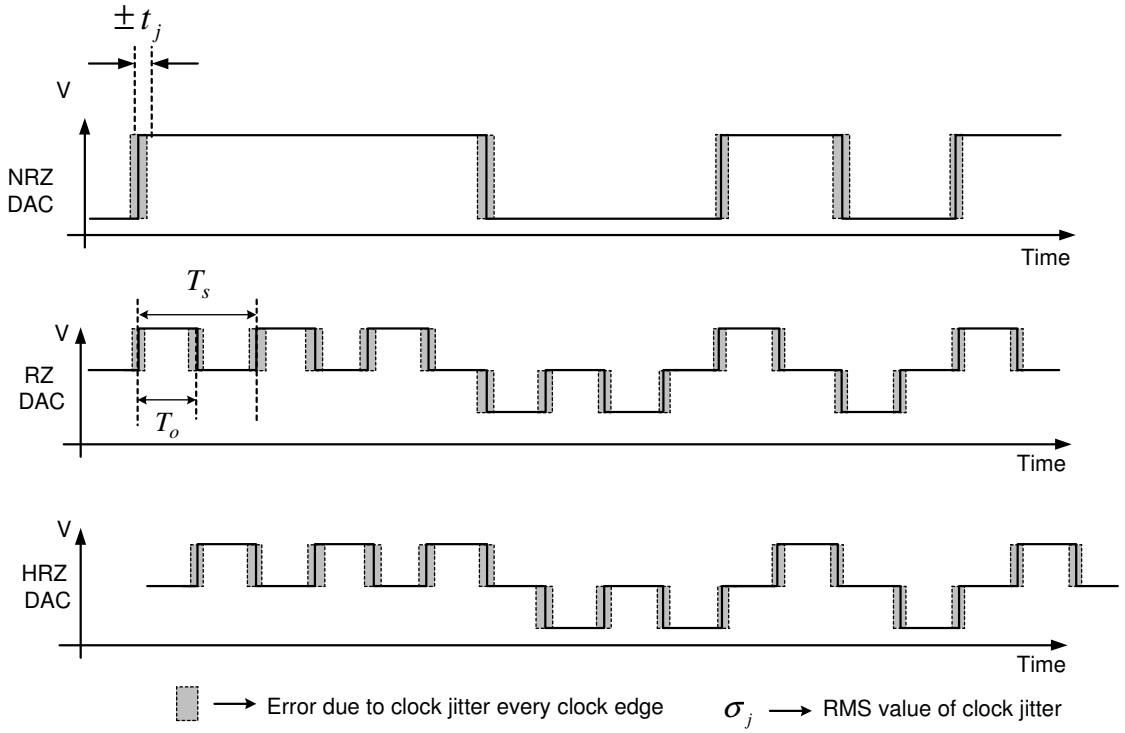


Fig. 3.6. Effect of clock jitter on the DAC pulse shapes

The SNR of a CT BP ΣΔ ADC with different DAC waveforms in the presence of clock jitter has been derived analytically in [41], where jitter is assumed to be a small perturbation in the sampling instant with a first order expansion of the non-linear effects of jitter. The power of the jitter noise in the feedback DAC pulses is calculated for a sinusoidal input signal and then multiplied by the signal transfer function to obtain the noise power due to jitter at the ADC output. The SNR for CT BP ΣΔ ADC architecture with only NRZ DAC is given by (3.6), while the SNR for the ADC architecture with only RZ/HRZ DAC is given by (3.7).

$$SNR_{NRZ} = 10\log_{10}\left(\frac{\mathrm{OSR} * \mathrm{V}_{in}^2 * \mathrm{sinc}^2\left(\frac{\omega_o \mathrm{T}_s}{2}\right)}{4\left(\frac{\sigma_j}{\mathrm{T}_s}\right)^2}\right) \tag{3.6}$$

$$\mathrm{SNR}_{\mathrm{RZ/HRZ}} = 10\log_{10}\left(\frac{\mathrm{OSR} * \mathrm{V}_{\mathrm{in}}^2 * \mathrm{sinc}^2\left(\frac{\omega_{\mathrm{o}} \mathrm{T}_{\mathrm{o}}}{2}\right)}{4\left(\frac{\mathrm{T}_{\mathrm{s}}}{\mathrm{T}_{\mathrm{o}}}\right)^2\left(\frac{\sigma_{\mathrm{j}}}{\mathrm{T}_{\mathrm{s}}}\right)^2}\right) \tag{3.7}$$

where OSR is the oversampling ratio, V_{in} is the amplitude of input signal, ω_o is the center frequency of the bandpass filter, Ts is the time period of sampling clock, To is the time for which RZ DAC pulse is high (usually 50% of Ts) and σ_j is the rms value of clock jitter. The sinc function appears in the numerator of (3.6) and (3.7) because the signal transfer function of a CT BP ΣΔ ADC is shaped by a sinc function, when evaluated in a small region around the center frequency [41]. When To = 0.5*Ts, the SNR for NRZ DAC is 6 dB higher than RZ/HRZ DAC, assuming the same value of σ_j in

both cases. NRZ DAC waveforms make a transition only when the bit value changes while RZ DAC waveforms have a transition every cycle, which results in a higher error power introduced due to clock jitter for the RZ case. For the architecture which uses a combination of both RZ and HRZ DAC, the error power term doubles and the SNR of the architecture with only NRZ DAC improves by 9.3dB (1.5 bits), as compared to the RZ/HRZ architecture [42]. Simulation results performed in Matlab validate this analysis and SNR improvement of roughly 2 bits (12 dB) is obtained by using NRZ DAC over RZ/HRZ DAC architectures. This improvement is significant when the clock frequencies are in the GHz range and the clock jitter becomes an increasing fraction of the overall time period.

3.4.2. Comparator metastability

The comparator is usually implemented as a cascade of a gain amplifier and a regenerative latch. The regenerative latch is a positive feedback circuit which amplifies the voltage difference at the input to a digital output of maximum positive value (+1) or maximum negative value (-1). The regenerative circuit of the digital latch can be modeled as a single pole system where the voltage difference at the input increases exponentially with a time constant that is inversely proportional to the gain bandwidth (GBW) product of the latch. When the input to the comparator is very small, the regeneration time of the latch becomes a significant part of the clock period and the output of the comparator cannot reach one of the decision levels (1 or -1). This causes the zero crossing time of the output (propagation delay of the latch) to be a variable

quantity depending on the input value. This effect is called metastability and it causes uncertainty in the comparator output. The comparator output drives the DAC's and the comparator metastability has the same effect as clock jitter in that it causes a random variation of the rising/falling edges and increases the noise floor. The metastability problem in CT ΣΔ ADC has been analyzed in detail in [37], [42] and it results in degradation of the SNR at the ADC output. Since the metastability has an effect similar to the clock jitter, the amount of SNR degradation can be estimated by calculating an effective rms value for the edge variations in DAC pulses due to metastability only (σ_j seconds) and substituting that value of σ_j in (3.6) and (3.7). The most common approach to overcome this problem is to use a cascade of latch stages in order to provide more positive feedback (gain) for the regeneration process, which results in lower uncertainty of the digital output. The main drawback of this approach is that an additional half cycle delay ($z^{-1/2}$) in the feedback loop results by the addition of two digital latch stages, each driven by opposite differential clock phases. This problem of additional delay can be overcome by considering the delay in the loop transfer function of H(z) while using the impulse invariant transform given by (3.3) for obtaining H(s) [37].

3.4.3. Excess loop delay

The rising edge of the comparator clock starts the process of sampling and quantization, and the comparator drives the DAC to inject current pulses back to the continuous time bandpass filter. The ideal response of the DAC current pulses is delayed in time due to finite switching time of transistors in the feedback path (comparator and

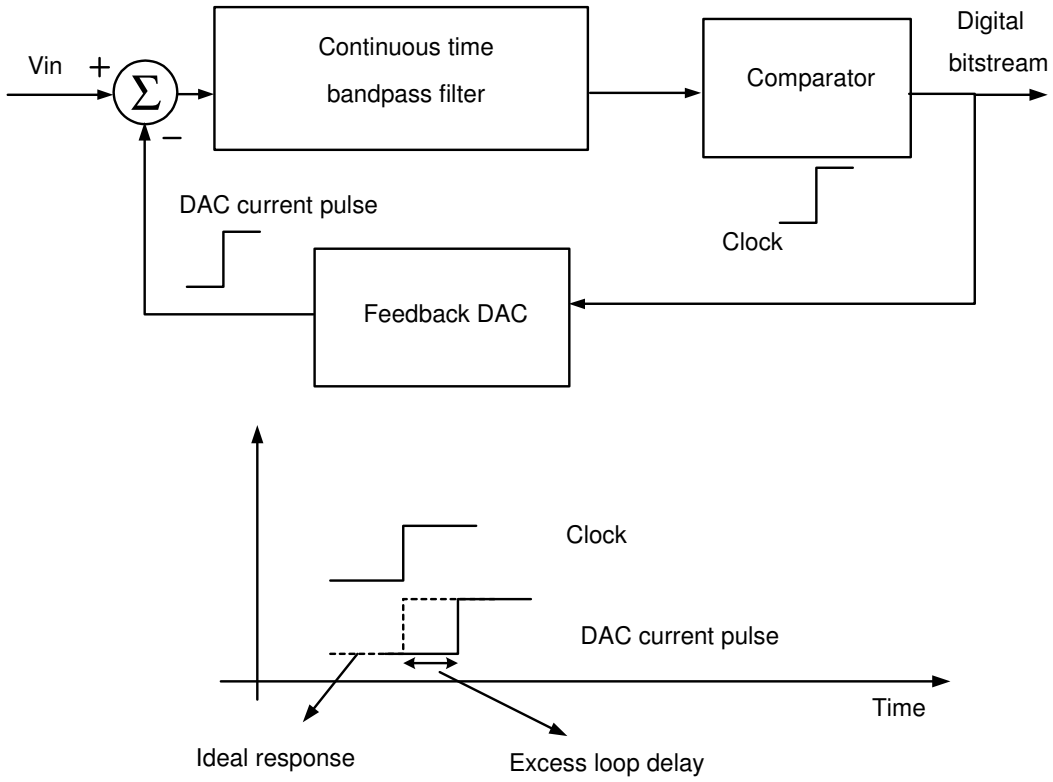


Fig. 3.7. Excess loop delay in continuous time bandpass ΣΔ ADC

DAC blocks). The delay (in time) between the ideal response and the actual response of the DAC current pulses is called excess loop delay and is illustrated in Fig. 3.7.

A time delay (d seconds) block can be represented in continuous time domain as e^{-sd} and in discrete domain as $z^{-(d/Ts)}$, where Ts is the time period of the clock. The effect of delay can be modeled by including the delay block representation in cascade with the loop transfer function (H(s) or H(z)) of (3.3) , which includes the delay effect while calculating the impulse invariant transform. The effect of excess loop delay CT BP ΣΔ ADC has been analyzed in detail in [37] and [43]. The excess loop delay modifies the loop transfer function and its effect is observed at the ADC output in two ways. The

quantization noise floor in a CT BP ΣΔ ADC increases with excess loop delay and degrades the noise floor. The amount of SNR degradation depends on lot of factors like the order of ADC, value of delay in each of the DAC feedback paths (each path affects the SNR differently as they modify the transfer function differently), type pf DAC pulse shape etc. Another harmful effect of excess loop delay is that it increases the order of the modulator when the impulse invariant transform of (3.3) includes the delay block. The increase in the order of the ADC can lead to stability problems when the amount of delay is very high, which should be carefully taken into account in simulations and the design process. One possible solution to avoid excess loop delay problems is to adjust the ADC coefficients of the CT BP ΣΔ ADC in order to restore the loop transfer function which is modified by the loop delay. Another solution is to decrease the out-of-band gain of the NTF during the design of the ADC architecture.

3.4.4. Finite quality factor of the bandpass loop filter

The fundamental definition of quality factor (Q) of an energy storage system with losses (example is a parallel LC tank with losses represented by resistor, R, in parallel with the tank) can be expressed as

$$Q = 2\pi * \frac{energy\ stored}{average\ power\ dissipated}\ per\ unit\ time \qquad (3.8)$$

Q is dimensionless and gives an indication of the amount of losses present in the system. When the value of Q is high, the losses in the system are low and vice versa. In a LC filter, the inductor stores magnetic energy and capacitor stores electrical energy and energy is exchanged between L and C every cycle in a resonator, with losses due to the

resistor. The quality factor for an LC tank can be derived by applying the definition of (3.8) to a LC tank and is given by

$$Q_{LC\tan k} = \frac{R}{\omega_0 L}; \omega_o = \sqrt{\frac{1}{LC}} \tag{3.9}$$

For bandpass filter, Q is also defined as the ratio of center frequency to the -3dB bandwidth of the bandpass filter. The Q of the bandpass filter affects the noise transfer function (NTF) of a CT BP ΣΔ ADC, and this point is illustrated by considering a second order ADC. The NTF of a second order CT BP ΣΔ ADC with finite Q is given by

$$NTF = \frac{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2 + As} \tag{3.10}$$

The magnitude of the NTF at the center frequency is given by

$$\left|NTF\right|_{@\, s=j\omega_o} = \frac{\omega_o}{\omega_o + AQ} \tag{3.11}$$

The value of (3.11) approaches zero for very high values of Q (it approaches large negative dB values in log magnitude). The effect of the bandpass filter's finite quality factor (Q) on the NTF of a CT BP ΣΔ ADC is shown in Fig. 3.8. The quantization noise floor for a CT BP ΣΔ ADC reduces for high Q values and results in high SNR. The gain of the bandpass filter at its center frequency ($s=j\omega_o$) is given by (AQ/ω_o), which increases for higher values of Q. The large results in increased signal swing in the internal nodes of the ADC (output node of the bandpass filter). The increased signal swing levels may cause clipping of the voltages and may result in unstable behavior.

Thus, the upper limit for the Q value is determined by the loop stability. The optimum value of Q is a tradeoff between the maximum attainable SNR and stable operation.

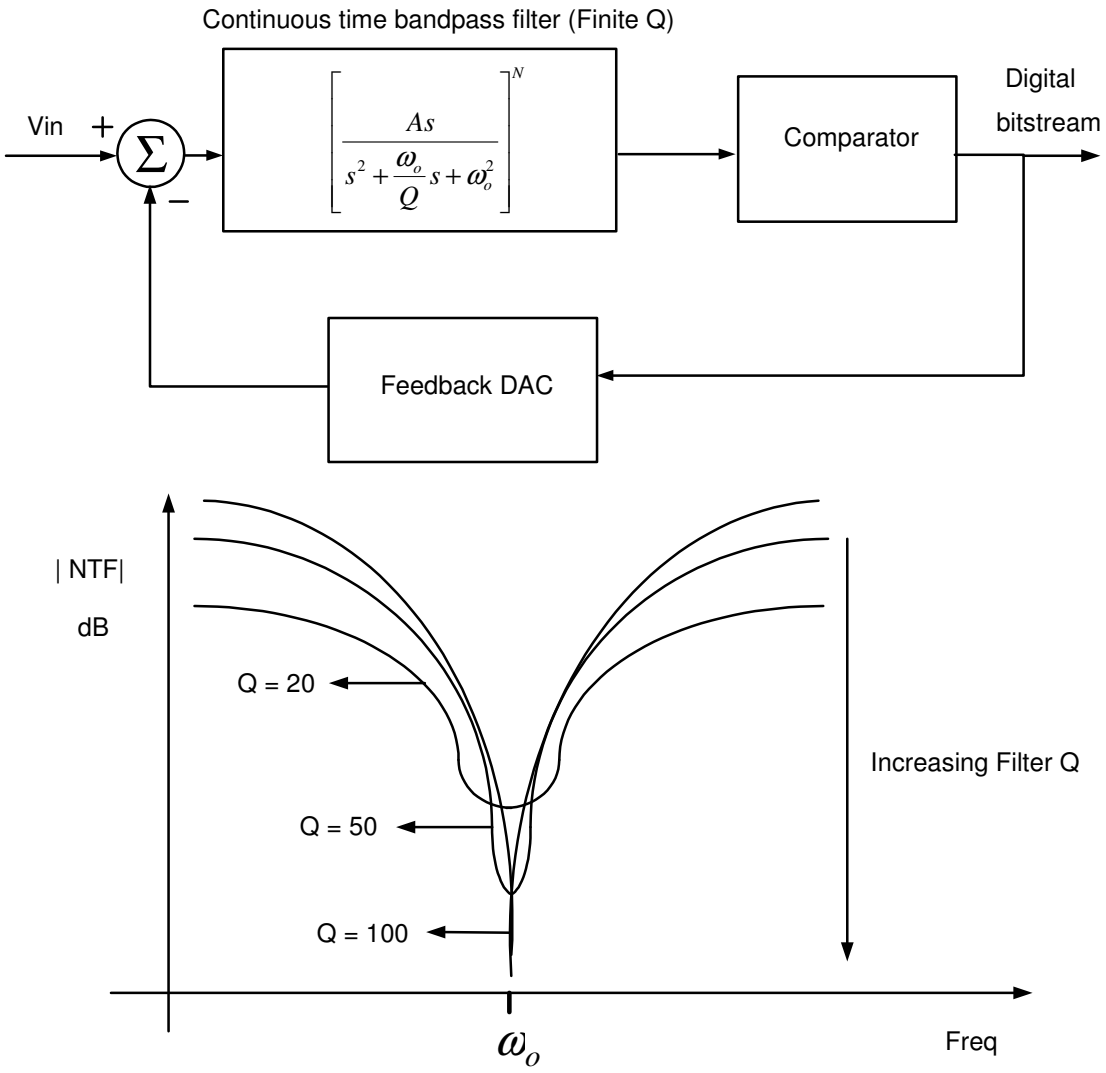


Fig. 3.8. Effect of the bandpass filter's finite quality factor (Q) on NTF

3.4.5. Unequal DAC pulse rise and fall time

The open loop transfer function of a CT BP ΣΔ ADC depends on the exact shape of the DAC pulse and non-idealities occur when the rise and fall time of the DAC pulse shapes are not equal [37]. This effect is shown in Fig. 3.9, where the rise time of the DAC pulse is high and the fall time is almost zero for two different bit patterns from

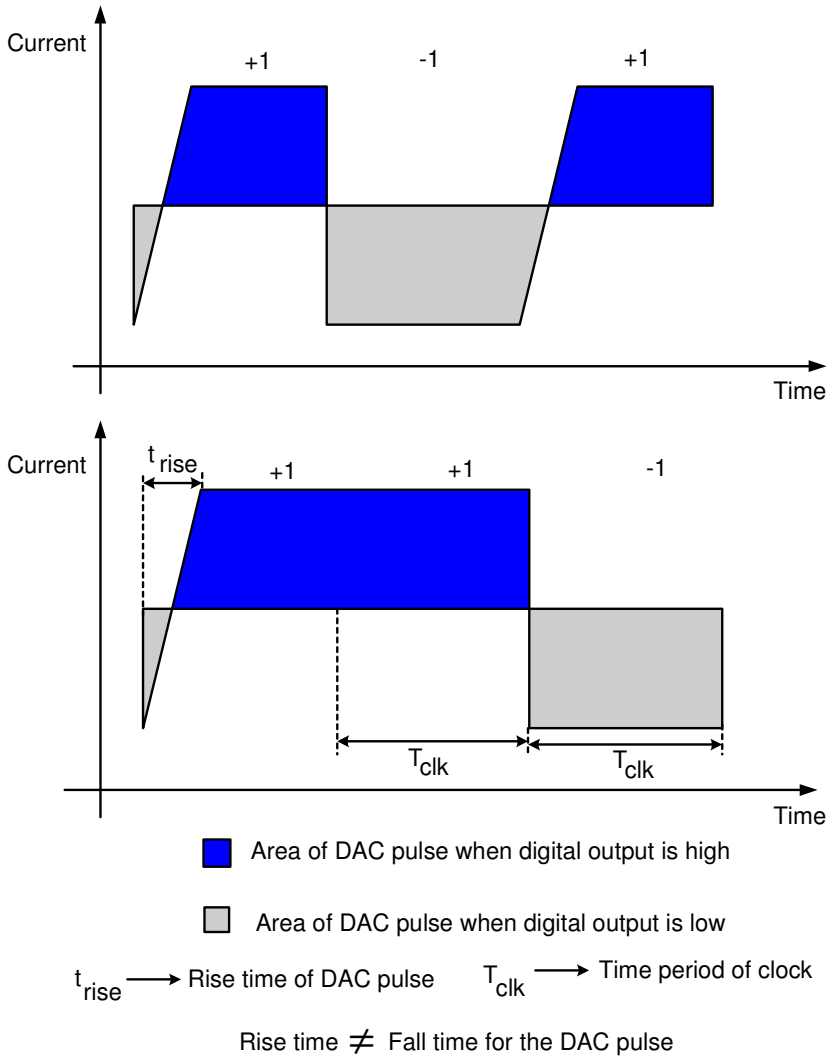


Fig. 3.9. Effect of unequal DAC pulse rise and fall times

the comparator output {+1,- 1,+1} and {+1,+1,-1}. The area of the DAC current pulses when the digital output is high (dark shaded region) and when the digital output is low (lightly shaded region) for the two bit patterns are different. This effect is also called inter symbol interference (ISI). The area is important because it represents the time the feedback DAC current is processed by the continuous time filter. Ideally, the ordering of the same set of bits should not change the area, but it differs when the rise and fall times are not the same. This error is injected directly at the input for the first stage DAC, which is not noise shaped by the feedback loop and results in performance degradation. Higher order modulators produce non-deterministic bit streams and hence, probabilistic estimates are required to analyze this effect. The effect of unequal rise/fall times of DAC pulses on CT ΣΔ ADC was done in [44] and it was shown that asymmetric DAC pulses results in white noise at the output spectrum, which reduces the quantization noise floor and the SNR. The rise/fall time of the DAC should satisfy the following condition for a desired SNR

$$t_{rise/\,fall} \leq \frac{4 * T_{clk} * \sqrt{OSR}}{SNR_{desired}} \tag{3.12}$$

where T_{clk} is the time period of the clock and OSR is the oversampling ratio. There are two approaches that have been proposed to overcome this problem. The first one is to use fully differential DAC rather than single-ended DAC outputs, as the sum of two asymmetric single-ended DAC waveforms produce a symmetric differential DAC waveform. The other approach is to use RZ DAC rather than NRZ DAC, since the area for different bit patterns are same in the case of RZ DAC because they have the property of returning to the zero value every clock cycle.

3.4.6. Frequency and Q tuning of continuous time loop filter

The center frequency and Q of a continuous time loop filter, unlike a switched capacitor filter, is heavily dependent of process, voltage and temperature (PVT) variations. The continuous time bandpass filter could have gm-C, LC or active RC implementations and all these filter types have a typical ±30% variation in the location of their center frequency and Q. An automatic tuning loop is usually needed to fix the center frequency and Q to the desired value [45]. The quantization noise floor is attenuated to the maximum possible extent only when the center frequency and Q are at the required value and any deviation will results in lower SNR. This issue is addressed in more detail in Section 5.3 of Chapter V.

3.5. Analysis of reported architectures

The design of a CT BP ΣΔ ADC starts with the choice of a switched capacitor (SC) architecture (H(z) and DAC coefficients in Fig. 3.3), which is used to derive an equivalent H(s) using the impulse invariant transformation. The important choices for the SC architecture are single loop or multi-stage (MASH), number of comparator bits and the relationship between clock frequency and the frequency of the input signal. The most common SC BP ΣΔ ADC is a single loop, fourth order cascade of resonator architecture. The choice of DAC pulse shape plays a very important role in the determining the performance and non-idealities of a CT BP ΣΔ ADC, which was discussed in detail in the preceding sections. The features of two reported CT BP ΣΔ

ADC architectures for RF digitization will be discussed to identify some of the main drawbacks of existing architectures.

The first topology that is analyzed is a fourth order, single loop, single bit CT BP ΣΔ ADC architecture that was reported in [28] for digitizing signals around 1 GHz with a 4 GHz clock frequency and LC bandpass filters were used for the loop filter implementation. The required H(s) is calculated using (3.3) from a fourth order SC BP ΣΔ cascade of resonator architecture by assuming a full clock period delay (z^{-1} delay) in the feedback path. The main issue in using only NRZ DAC in a LC bandpass ΣΔ ADC is the lack of enough injection nodes to realize the required notch NTF with full control over tuning of the coefficients. The LC filter is a second order block and has only one

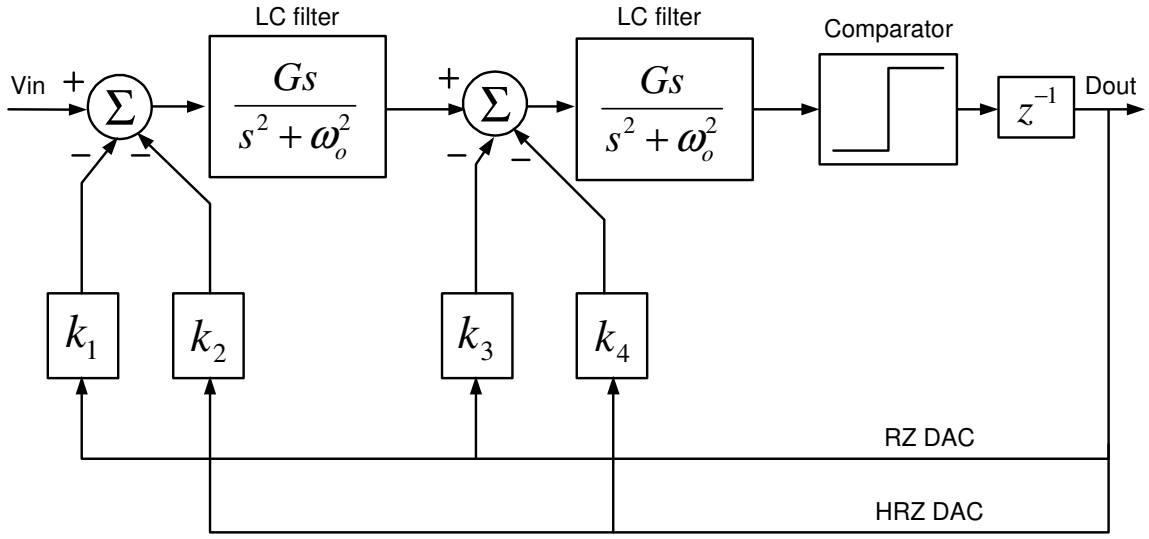


Fig. 3.10. Architecture used in implementation of Ref [28]

injection point where the feedback DAC can be connected in order to realize a transfer function, in contrast to a gm-C filter implemented using a two integrator loop, which has two injection points (this difference is explained further in section 4.1 of Chapter IV). This architecture overcame the problem by using a combination of both RZ and HRZ DAC's, as shown in Fig. 3.10. Two feedback paths have RZ DAC while the other two have HRZ DAC and this combination results in full control of tuning all the coefficients of the NTF. The main problem with this architecture is that a combination of RZ/HRZ DAC is more susceptible to clock jitter and it degrades the SNR of ADC by more than 12 dB (2 bits) as compared to only NRZ DAC. The ADC architecture with RZ/HRZ DAC implementation could potentially result in more power consumption as compared to the NRZ DAC implementation. The measured SNR of the ADC reported in [28] was 50 dB in a 1 MHz bandwidth around 1 GHz, while dissipating 350 mW of power and it was implemented in 0.5 μm SiGe technology.

The second topology that is analyzed is a fourth order, single loop, three bit CT BP ΣΔ ADC architecture that was reported in [26] for digitizing signals around 1.3 GHz with a 4.3 GHz clock frequency and LC bandpass filters were used for the loop filter implementation. The architecture used for the ADC implementation is shown in Fig. 3.11. It uses only NRZ DAC and it overcomes the problem of control of NTF coefficients by using variable delays of $1.1*T_{clk}$, $1.6*T_{clk}$, T_{clk} and $0.7*T_{clk}$ in each of the DAC paths (T_{clk} is the time period of the clock used in the comparator). This approach is not practical since it becomes difficult to precisely control fractional delays at GHz clock frequencies. The time period of the clock used in this design was 230 ps and $0.1*T_{clk}$ is

23 ps. The implementation of this fractional delay which is necessary for accuracy of this architecture is not possible over PVT variations. The measured SNR of the ADC reported in [26] was 62 dB in a 1 MHz bandwidth around 1.3 GHz, while dissipating 6200 mW of power and it was implemented in Indium phosphide (InP) HBT technology.

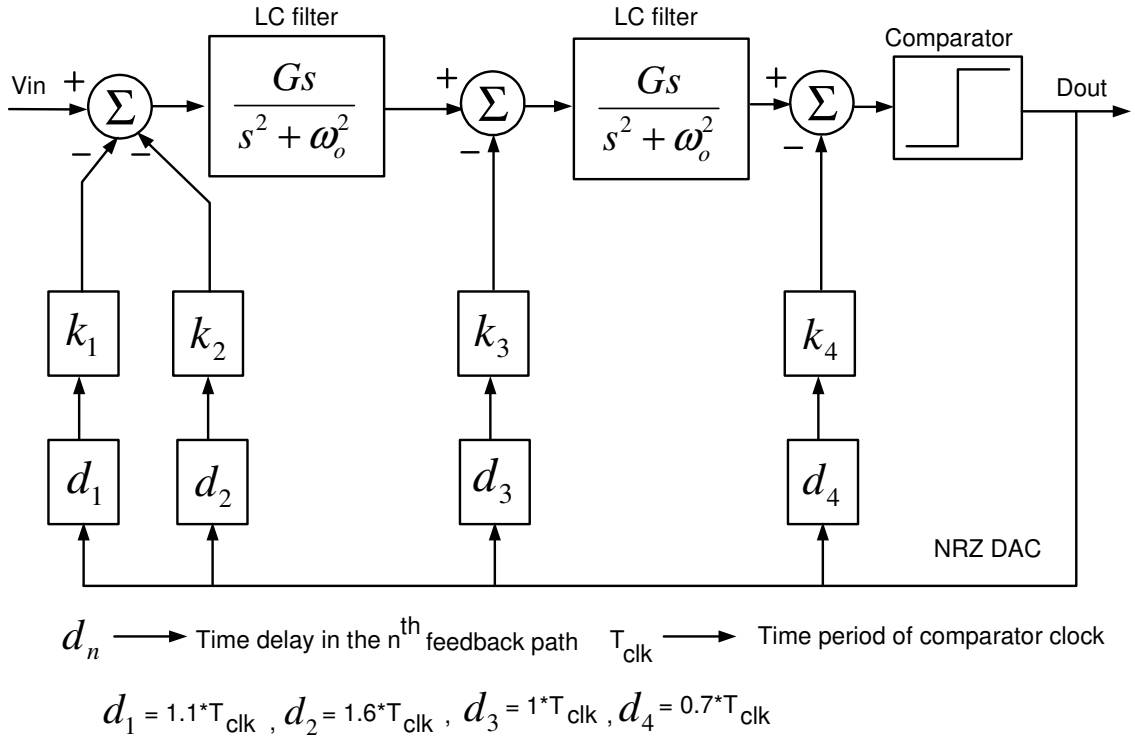


Fig. 3.11. Architecture used in implementation of Ref [26]

LC bandpass filters are not preferred for integrated implementations in the intermediate frequency range (50 MHz – 200 MHz) because large values of inductors and capacitors are required, which are accompanied by area penalty. The IF bandpass filters use gm-C or active-RC implementation which have two injection points and hence

can implement the required NTF (using only NRZ DAC) with full control of tuning the coefficients.

A brief overview of the design issues and main non-idealities in a CT BP ΣΔ ADC design was presented in this chapter. The design procedure of a CT BP ΣΔ ADC utilizes the impulse invariant transformation to derive a continuous time modulator from its discrete time equivalent architecture. The main advantages and non-idealities of the CT BP ΣΔ ADC were discussed and clock jitter is one of the main non-idealities that degrades the SNR at high sampling frequencies. The choice of DAC pulse shape changes the loop transfer function and it affects the performance and non-idealities of the ADC. The NRZ DAC pulse shape is the optimum choice for a CT BP ΣΔ ADC and it is used for both the RF and IF ADC designs in this research work.

CHAPTER IV

A 3.8 GHz ADC FOR DIRECT RF DIGITZATION OF BANDPASS SIGNALS AROUND 950 MHz

4.1. Introduction

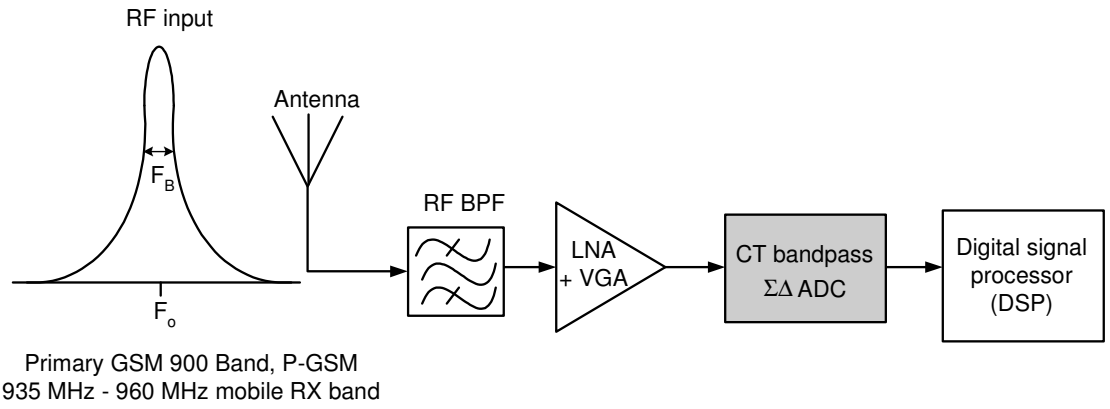


Fig. 4.1. Target application for the RF ADC design

The target application that is chosen for the ADC design is a software radio architecture operating in the GSM band and is shown in Fig. 4.1. The primary GSM 900 (P-GSM) standard occupies frequencies from 935 MHz to 960 MHz for its mobile receive (RX) band. The channel spacing (distance between the centers of two adjacent channels) is 200 kHz and the modulation format used is Gaussian minimum shift keying (GMSK), which is a frequency modulated signal preceded by a Gaussian low pass filter. The carrier amplitude in GMSK is not altered according to the digital bit stream and it uses a constant envelope modulation scheme. The bandwidth specification of the ADC

depends on the total number of channels that have to be digitized at its input. The maximum bandwidth for this case is 25 MHz (the whole band) and the minimum bandwidth is 200 KHz (single channel). The SNR requirement of the ADC can be calculated by considering the noise floor (sensitivity at receiver input), signal power and the required bit error rate (BER) at the receiver output. The required SNR of the ADC for a specified BER has been calculated in [46] and is given by

$$SNR_{ADC} = P_c - \left(PSD_{noise} + 10\log\left(\frac{BW}{m}\right)\right) - NF + 10\log(m) - 10\log(OSR) \quad (4.1)$$

where P_c is the power level of the carrier, BW is the bandwidth of all the channels, m is the number of channels, (BW/m) is the channel spacing, PSD_{noise} is the fundamental noise floor due to atmospheric noise at the antenna (-174 dBm/Hz at room temperature), NF is the total noise figure from the antenna to the ADC input and OSR is the oversampling ratio of the ADC. The OSR depends on the choice of the clock frequency, the noise figure depends on the implementation of the front end blocks (RF bandpass filter, LNA and VGA) and the other parameters in (4.1) are specified by the GSM standard.

The main drawbacks of ADC's reported in literature for RF digitization were discussed in Section 3.5. The power consumption is very high (0.45 to 6.2 Watts) and the CT BP ΣΔ architecture using LC filters cannot use NRZ DAC to reduce clock jitter effects. The two main objectives of this design is to obtain high resolution with low power consumption (in the mW range) and to explore alternate architectures for implementing CT BP ΣΔ ADC with reduced jitter effects. The ADC is implemented

using a fourth order, single loop and single bit CT BP ΣΔ architecture with LC filters. The fourth order architecture is chosen as an optimum choice between performance and stability considerations. Higher order modulator result in higher SNR, but are prone to unstable behavior [15]. The simple single loop, single bit architecture is chosen to keep the power consumption to a nominal value, which can increase for more complex architectures at GHz sampling frequencies.

According to Nyquist theorem, the center frequency of the CT BP ΣΔ ADC can be placed at any frequency between DC and $F_s/2$, where F_s is the sampling frequency of the clock. The input signals are located around center frequency F_o with bandwidth F_{in}, and the choice of the ratio F_o/F_s is a tradeoff among sampling frequency (related to speed of the whole system), anti-aliasing filter requirements and the OSR [47]. The optimal solution to the problem is to place the center frequency (F_o) at one-fourth of the sampling frequency. This selection of clock frequency offers two main advantages. The first advantage is that the loop filter implementation becomes simple by using the low pass to bandpass transformation ($z^{-1} \rightarrow -z^{-2}$). The second advantage is that the digital demodulation I/Q signals becomes easy as it involves simple multiplication by {1,0,-1}. The OSR (defined as $F_s/[2*F_{in}]$ for the BP ΣΔ modulator) of the ADC is fixed by the choice of the sampling frequency.

The choice of architecture and the noise transfer function (NTF) of the ADC depends on the bandwidth specifications of the ADC. The quantization noise is attenuated by the notch NTF as long as it is the dominant noise source at the output, which is true when a narrow bandwidth is under consideration. For a wide bandwidth

system, the integrated thermal noise floor will have a higher level than the quantization noise which necessitates a different design approach for obtaining the best SNR. The zeros of the NTF are all placed at a single frequency (center frequency of the filter) for a narrow bandwidth ADC, which ensures maximum possible reduction of the noise at the center frequency. The zeros of the NTF can be spread over the entire bandwidth for a wide bandwidth system, which results in an almost flat transfer function (combination of several closely spaced shallow notch functions) in the bandwidth of interest. Multi-bit comparator designs are also commonly used in wideband architectures at the cost of more power consumption. The digitization of the entire GSM band (25 MHz) is not considered because of power dissipation constraints. The two bandwidths that are considered in this design are 200 kHz (1 channel) and 1 MHz (5 channels), and both these specifications fall in the narrow bandwidth category.

Table 4.1 Specifications for the RF ADC

Parameter	**Value**
Center frequency (F_o)	950 MHz
Clock frequency	3.8 GHz ($4*F_o$)
Target SNR	> 60 dB
Bandwidth	200 kHz / 1 MHz
Technology	IBM 0.25 μm SiGe BiCMOS
Power	< 100 mW
Supply	± 1.25 V

The target specifications of the RF ADC design for software radio application in the GSM band is shown in Table 4.1. The maximum power level of the carrier (P_c) that is specified by the GSM standard is -13 dBm. The number of channels is one for 200 kHz bandwidth and five for a 1 MHz bandwidth. The OSR of the ADC is 9500 for a bandwidth of 200 kHz and 1900 for a bandwidth of 1 MHz. The combined noise figure (NF) of the all the blocks preceding the ADC depends on the implementation. The required SNR of the ADC can be calculated by substituting the values for the parameters in (4.1). Assuming a NF of around 3 dB, the SNR of the ADC should be greater than 64 dB for a 200 kHz bandwidth and greater than 74 dB for a 1 MHz bandwidth. The target power consumption is less than 100 mW and 0.25 μm IBM SiGe BiCMOS technology is chosen for the ADC implementation. The choice of the technology is based on two considerations – speed of operation and good software models to hardware correlation. The transition frequency (f_t) of the bipolar transistors in this technology is 47 GHz and they have the potential for high speed operation. The technology also offers the advantages and flexibility of using both bipolar and CMOS transistors. The models of the passive (inductors, resistors and capacitors) and active components have very good correlation with the measured values. This is a big advantage for the ADC implementation as accurate quality factor (Q) of the LC bandpass filter is essential for good performance. The combination of these advantages makes this technology a very good choice for the RF ADC implementation.

The design process of the CT BP ΣΔ ADC begins with identifying the best bandpass ΣΔ ADC architecture in the switched capacitor domain. The open loop transfer

function of the SC modulator is calculated and the open loop transfer function for the continuous time modulator is derived using the impulse invariant transformation, as discussed in Section 3.2. The process of calculation of the open loop transfer function for a CT BP ΣΔ modulator is shown in Fig. 4.2.

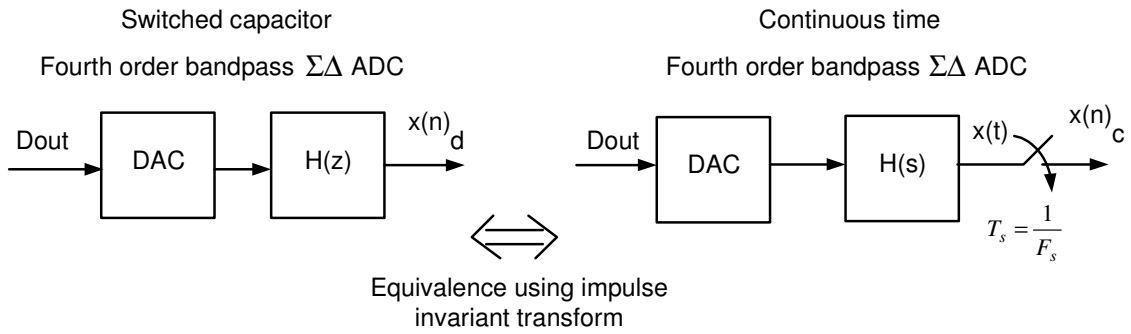


Fig. 4.2. Calculation of the open loop transfer function

A fourth order SC BP ΣΔ ADC can be realized by using a cascade of two second order resonator functions, as discussed in Section 2.2.3. The fourth order SC modulator can be derived from a fourth order low pass SC prototype by the substitution $z^{-1} \rightarrow -z^{-2}$, which transforms the zeros from DC to $F_s/4$, where Fs is the clock frequency. The unit delay element (z^{-1}) in the low pass filter is substituted by a two unit delay element (z^{-2}) with an inversion. The loop filter (H(z)) for the fourth order SC BP ΣΔ modulator is given by

$$H(z) = \frac{2z^{-2} + z^{-4}}{\left(1 + z^{-2}\right)^2} \tag{4.2}$$

There are two other design consideration which determine the open loop transfer function of the CT BP ΣΔ ADC. The first design consideration is the type of feedback DAC implementation – NRZ (non return to zero), RZ (return to zero) or HRZ (half return to zero) DAC, as discussed in Section 3.3. The second design consideration is the implementation of one clock period delay (z^{-1}) in digital domain after the comparator (this technique helps to reduce the metastability problem of the comparator, which is critical especially at GHz clock frequency). The z^{-1} delay can be accounted in the design procedure by factoring it out of (4.2). The modified H(z) that is used is given by (4.3), which together with the clock period delay results in the original transfer function.

$$H_{\mathrm{mod}ified}(z) = \frac{2z^{-1} + z^{-3}}{\left(1 + z^{-2}\right)^2} \tag{4.3}$$

NRZ DAC is used for the feedback DAC to mitigate the effects of clock jitter. Then, H(s) in Fig. 4.2 is derived using the modified H(z), the transfer function of NRZ DAC in the impulse invariant transform equation given by (3.3). For a fourth order CT BP ΣΔ ADC with one clock cycle delay in the feedback loop, the open loop transfer function (H(s)) calculated using impulse invariant transformation of an equivalent fourth order SC BP ΣΔ ADC has been derived in [48] and is given by

$$H(s) = \frac{\left(\frac{\pi}{2} - \frac{1}{4}\right)\frac{s^3}{T} + \left(\frac{3\pi^2}{16} + \frac{\pi}{4}\right)\frac{s^2}{T^2} + \left(\frac{\pi^3}{8} + \frac{\pi^2}{16}\right)\frac{s}{T^3} + \frac{3}{4} * \left(\frac{\pi}{2T}\right)^4}{\left(s^2 + \left(\frac{\pi}{2T}\right)^2\right)^2} \tag{4.4}$$

where T is the time period of the comparator clock and the center frequency of the bandpass filter, $\omega_o = (\pi/(2T))$. The out of band gain of the noise transfer function (NTF) is an important parameter which affects stability and as a rule of thumb, should be less than 2 [49]. In this design, the value is chosen to be 1.4, to give some room for PVT variations.

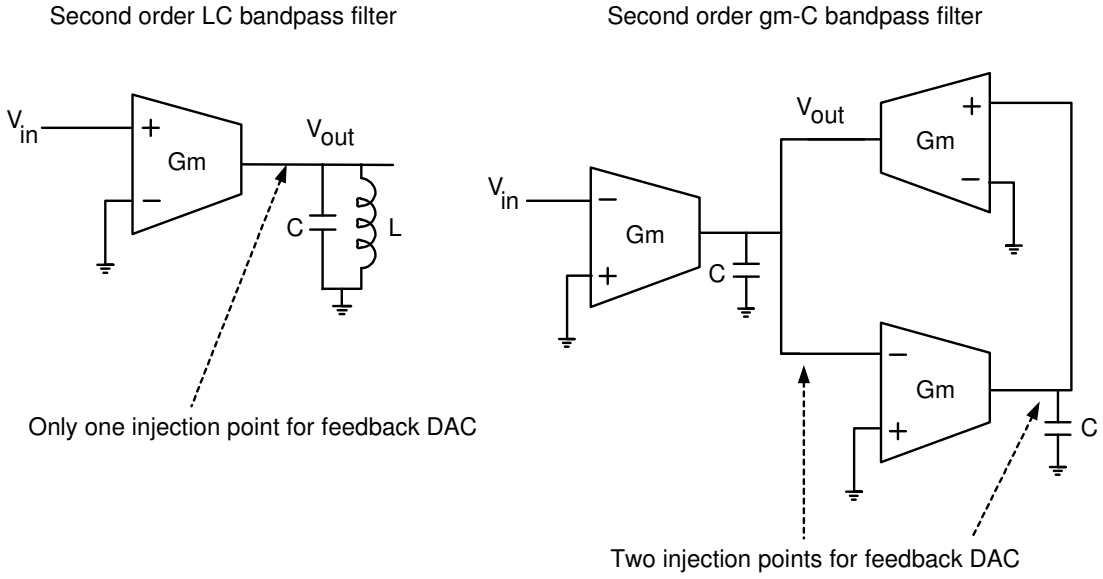


Fig. 4.3. Second order continuous time bandpass filter structures

The implementation of the transfer function given by (4.4) using LC filters and NRZ DAC with full tuning of the loop coefficients poses some practical problems, as discussed in Section 3.5. The problem in realizing this implementation is illustrated in Fig. 4.3, which shows two possible second order bandpass filter implementations – LC filter and gm-C filter. The second order LC filter just has one injection node where the feedback DAC current can be injected in order to implement a transfer function. This is

in contrast to a second order gm-C filter realized using two integrator loop, which has two injection nodes where the feedback DAC current can be injected to implement a transfer function. The lack of enough injection nodes for transfer function realization is the main reason why NRZ DAC cannot be used along with LC filters in a CT BP ΣΔ ADC. The new architecture that is proposed in this research work overcomes this problem and it is described in detail in the next section.

4.2. Proposed ADC architecture

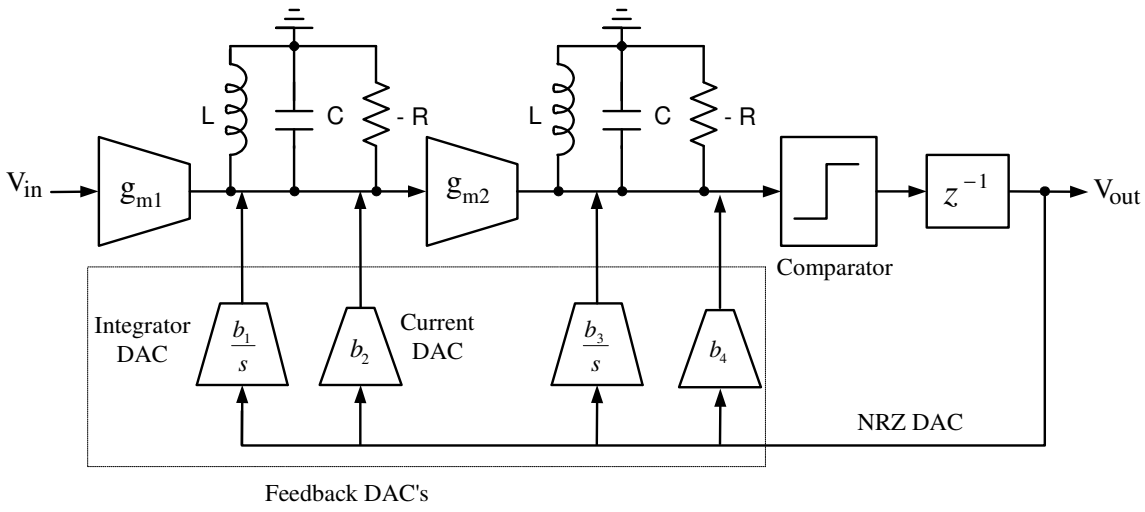


Fig. 4.4. Block diagram of the proposed RF ADC architecture

The block diagram of the proposed ADC architecture is shown in Fig. 4.4. The loop filter in the forward path is a fourth order continuous time LC bandpass filter that is implemented as a cascade of two second order LC filters. The LC tank has a Q enhancement block (negative resistor, -R) to replenish the losses in the inductor and

capacitor. The transconductance blocks, g_{m1} and g_{m2}, are used to convert the input voltage into current, which is then injected into the LC tank. The comparator samples the filter output and gives a single-bit digital bit stream as output. The feedback path is a linear combination of four paths; two quasi-lossless integrator DAC paths and two current DAC paths. The DAC blocks convert the digital output to current (analog domain), which is injected back into the LC tank. The main difference between a current DAC and the integrator DAC is that the latter is frequency dependent, which is evident from its transfer function.

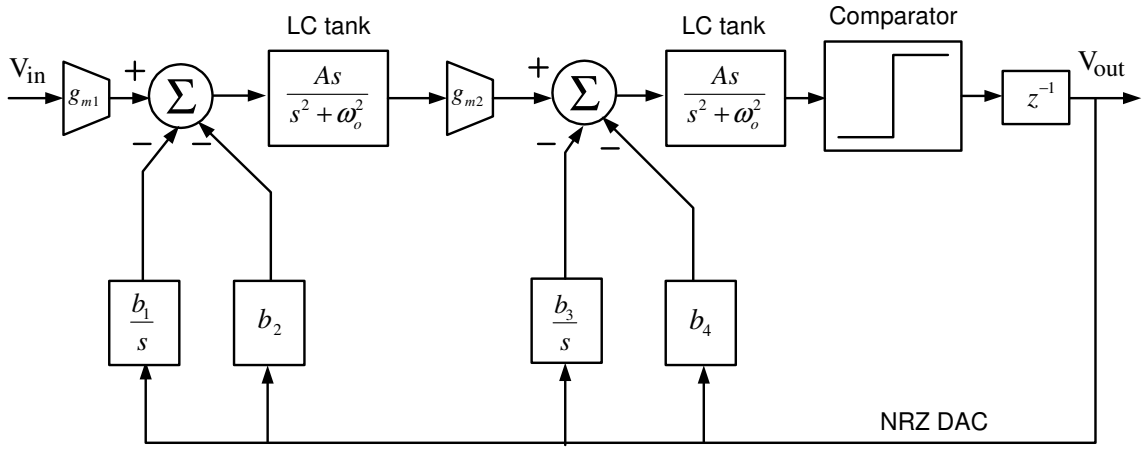


Fig. 4.5. Transfer function of the proposed RF ADC architecture

The transfer function of the proposed ADC architecture can be calculated from Fig. 4.5. Ignoring the losses in the LC tank, the open loop transfer function from the ADC output (V_{out}) to the comparator input (calculated by opening the loop) is given by

$$H_{loop}(s) = \frac{s^3 Ab_4 + s^2(A^2 g_{m2} b_2 + Ab_3) + s(A^2 g_{m2} b_1 + A\omega_o^2 b_4) + A\omega_o^2 b_3}{(s^2 + \omega_o^2)^2} \quad (4.5)$$

where

$$A = \frac{1}{C};\ \omega_o^2 = \frac{1}{LC} \quad (4.6)$$

The transconductance value of the first filter stage, g_{m1}, does not affect the loop characteristics since it doesn't appear in (4.5). The main role of g_{m1} is to transfer the input voltage into current and its value determines the dynamic range at the input of the ADC. The transconductance value of the second filter stage, g_{m2}, affects the output signal swing and the loop transfer function; its value is chosen as an optimum tradeoff between linearity, noise, signal swing and power consumption considerations. The center frequency of the bandpass filter (f_o) is at ¼ of the clock frequency, thereby reducing digital demodulation to simple multiplication by {-1, 0, 1}. The value of inductor (L) depends on technology and geometry, and is chosen to optimize its quality factor at the filter's center frequency. The value of A (determined by the capacitors) can be calculated from (4.6), when L and ω_o are known. One of the main features of this architecture is that it provides independent control for each of the terms in the numerator of (4.5) while using only NRZ DAC, which alleviates clock jitter problem. The s^3 and constant terms in numerator of (4.5) are controlled by coefficients b_4 and b_3, respectively. Once these two coefficients are fixed, the s^2 and s terms are controlled by coefficients b_2 and b_1, respectively. The value of each of the coefficients in the numerator of (4.5) affects the poles and zeros of the NTF, and the precise control of each

of the coefficients is required in order to guarantee the proper shape of the NTF. The individual control of each of these coefficients ensures good control of the NTF while tuning them, which results in good SNR. The open loop transfer function calculated using impulse invariant transformation of an equivalent fourth order SC BP ΣΔ ADC is given by (4.4). The loop coefficients b_1, b_2, b_3 and b_4 can be calculated by equating each coefficients of the numerator in (4.4) and (4.5) respectively. The main feature in the proposed ADC architecture is the introduction of the frequency dependent integrator DAC block which helps in realizing the required transfer function. The operation of the integrator DAC is examined in detail in the next section.

4.3. Operation of the integrator DAC

The integrator DAC in the proposed ADC architecture takes a digital NRZ bit stream as input and gives an integrated current pulse stream as output. The typical output waveform of an integrator DAC block is shown in Fig. 4.6 and the.

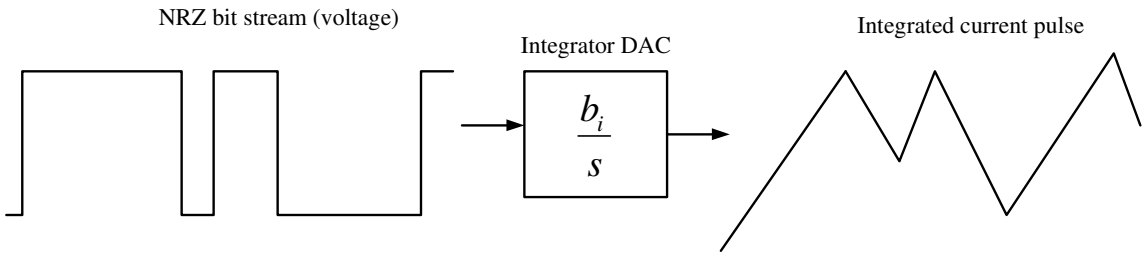


Fig. 4.6. Typical output waveform of the integrator DAC block

The integrator DAC shown in Fig. 4.6 has an ideal transfer function (b_i/s), but this representation poses some practical limitations. The ideal integrator has a pole at $\omega = 0$ and the phase shift at $j\omega = 0$ is 90°. It is difficult to implement ideal integrators due to finite DC gain of amplifiers and finite quality factor of integrated capacitors. The output swing of all internal nodes in the ADC should be within the supply voltages (Vdd/Vss) at all times for proper operation. The lossless integrators are prone to reach saturation levels, which poses a restriction on the operating range of the integrator.

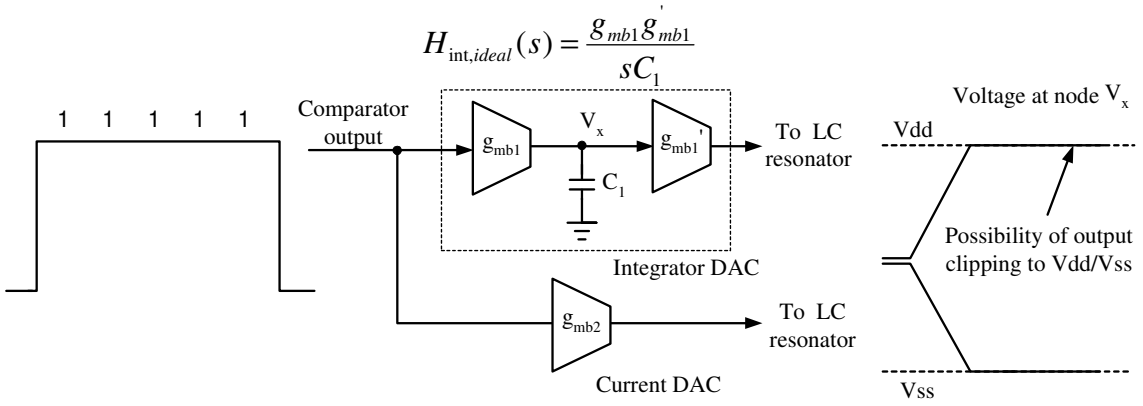


Fig. 4.7. Schematic of the feedback DAC blocks with ideal integrator DAC

The simplified schematic of an ideal integrator DAC along with its transfer function is shown in Fig. 4.7. The transconductor g_{mb1} converts the digital output to current, which is integrated by the capacitor C_1. The output voltage at node V_x has to be converted into current in order to be injected back into the LC tank, and the V-I conversion is performed by the transconductor g_{mb1}'. When a NRZ bit stream is given as input to an ideal integrator, its effective DC voltage is integrated at node V_x. When a

large consecutive number of 1's or 0's are present at the input, the output of the ideal integrator may clip to either of the supply voltages, as shown in Fig. 4.7. The hard clipping of the integrator output voltages at node V_x to either of the supply rails disables the integrator DAC's from the negative feedback loop and they either inject or extract a constant amount of current every clock cycle. When this condition occurs at node V_x, the loop transfer function of the ADC changes drastically and this results in SNR reduction at the ADC output.

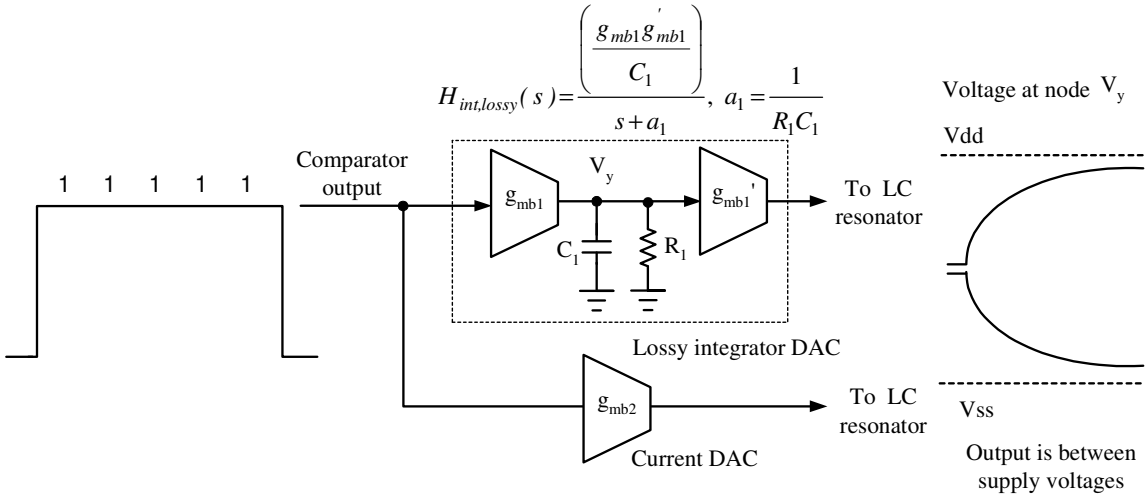


Fig. 4.8. Schematic of the feedback DAC blocks with lossy integrator DAC

The simplified schematic of a lossy integrator DAC along with its transfer function is shown in Fig. 4.8. The addition of the resistor R_1 to the ideal integrator adds extra losses and the lossy integrator has a pole at $\omega=1/(R_1*C_1)$. The use of lossy integrators, as shown in Fig. 4.8, instead of ideal integrators alleviates the hard clipping issues as it decreases the integration step and reduces the probability of clipping for the

same number of consecutive 1's or 0's at the integrator output node V_y. The probability of clipping at the integrator output is directly related to the integration step (incremental step of output voltage every clock cycle), which is dependent on the circuit parameters. For every cycle that the digital input is high(low), a certain amount of current is injected (extracted) to the capacitor, which causes an increase (decrease) in the output voltage. Thus, the integration step depends on the value of g_{mb1}, C_1 and the losses. A larger step every cycle will cause the output to clip for a relatively short number of consecutive 1's or 0's, and vice-versa for a smaller integration step. This concept can be understood better by considering the time domain response for ideal and lossy integrators to a step input (consecutive 1's or 0's in time domain). The output at node V_x for a unity step input (u(t)) at any given time, t, is given by

$$V_x(t) = V_x(0) + \frac{g_{mb1}}{C_1}\int_0^t dt = V_x(0) + \frac{g_{mb1}}{C_1}t \tag{4.7}$$

where $V_x(0)$ is the initial condition of the output at t = 0. The linear ramp eventually hits the saturation limit (supply voltages) and disables this feedback path. Similarly, the output at node V_y for a unity step input at any given time, t, is given by

$$V_y(t) = V_y(0) + \frac{g_{mb1}}{C_1}e^{-\left(\frac{1}{R_1C_1}\right)t} \tag{4.8}$$

where $V_y(0)$ is the initial condition of the output at t = 0. The exponential time constant settling effect in (4.8) causes the lossy integrator output to have soft clipping, rather than hard clipping and this extends the operating range of the integrator. The difference in time domain behavior can be summarized by the following statement – if the output

given by (4.7) clips to the supply rail for n consecutive 1's or 0's, then the output given by (4.8) would clip for at least twice the number (2*n) of consecutive 1's or 0's. The output of the lossy integrator to a step input (consecutive 0's or 1's) is given by (4.8), which is similar to the response of an RC network. The step response of an RC network settles to 63.2% of its final value in one time constant (τ = RC seconds), to 86.6% of the final value in 2*τ seconds and to 99.3% of the final value in 5*τ seconds. The output of the lossless integrator to a step input is given by (4.7), which is a linear ramp. Let us consider the case when the ramp signal (output of the lossless integrator) hits the rail in τ seconds (τ seconds = "n" consecutive 1's or 0's). When losses (resistor) are introduced in the integrator such that the time constant of the RC network at its output is τ, then the output reaches only 87% of the final value in 2*τ seconds (the output doesn't clip for atleast 2*τ seconds = "2*n" consecutive 1's or 0's) . The addition of extra losses (resistor R_1) improves the ADC's operating range for good SNR performance and makes it more robust. The operating range of the ADC refers to the integrator DAC tolerating a wide variety of input bit patterns without undergoing hard clipping at its output. The effect of the losses in the integrator DAC on the ADC performance was verified using behavioral simulations. A behavioral model of the proposed ADC architecture was simulated in Simulink with both ideal and lossy integrator DAC's and the output spectrum of the ADC (calculated using Fast Fourier transform (FFT) of the digital bit stream) for both cases is shown in Fig. 4.9 where amplitude of the input signal is 120 mV. The ideal integrators are assumed to have infinite DC gain, while the lossy

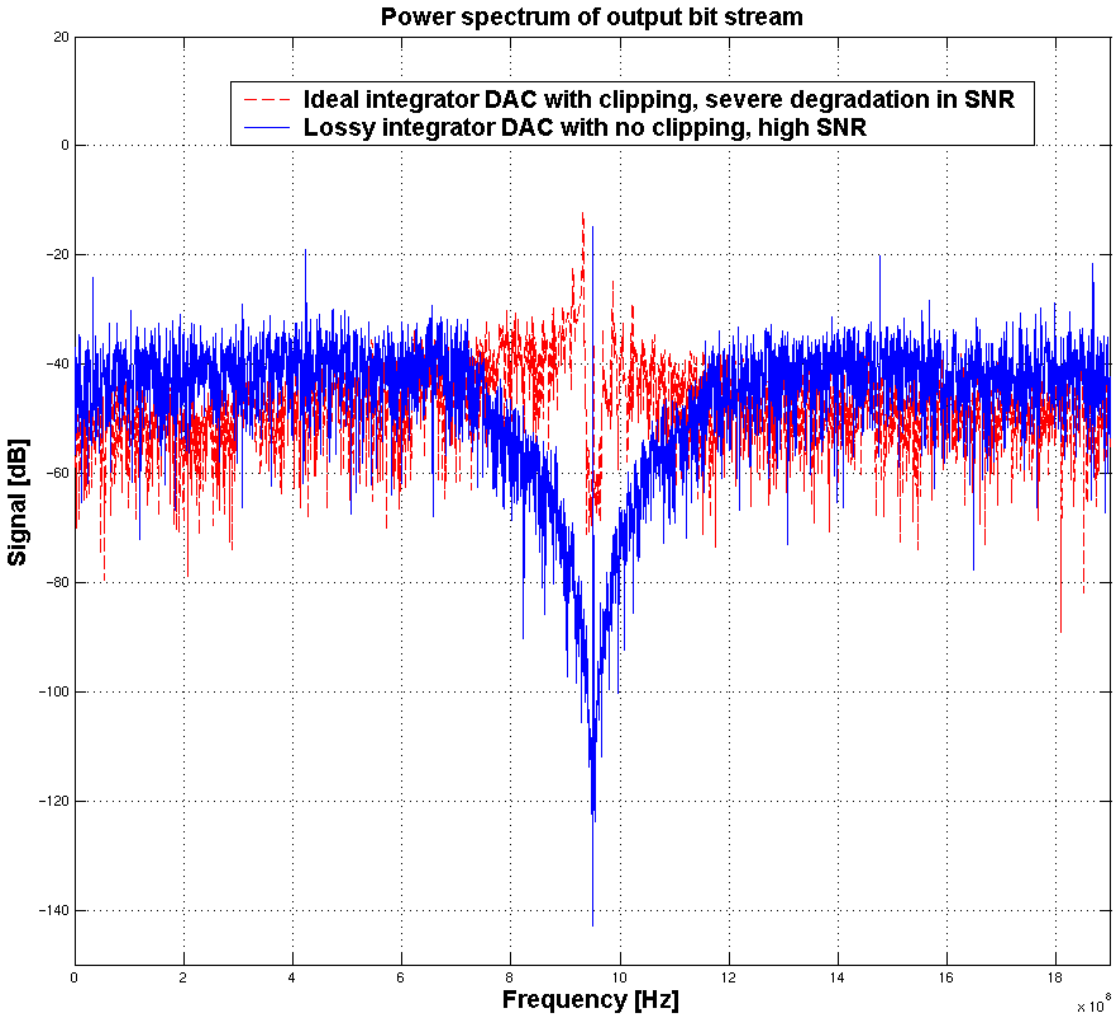


Fig. 4.9. Output spectrum of the ADC architecture with and without integrator losses

integrators have a nominal DC gain of about 40 dB. The behavioral model contains non-idealities that would be present in a circuit implementation like finite Q of bandpass filter, limited signal swing at all internal nodes, clipping of node voltages when it reaches the supply voltages etc. The solid line in Fig. 4.9 shows the output spectrum of the ADC with lossy integrator DAC while the dotted line is the output spectrum of the

ADC with ideal integrator DAC. For the case when the output of ideal integrator clips (especially for large signals), the loop transfer function changes drastically and increases the in-band noise floor, resulting in a severe degradation of SNR at the output of the ADC.

There are two other approaches to decrease the integration step at node V_x in Fig 4.8. The first approach is to increase the value of the capacitor (C_1), while maintaining the value of g_{mb1}. The value of the loop coefficient is given by $(g_{mb1}*g_{mb1}')/C_1$ and in order to get the required coefficient, the value of g_{mb1}' has to be increased simultaneously. The integrated implementation of large capacitor values is not possible due to area constraints, which usually limit the capacitor to a reasonable value. The second approach is to decrease g_{mb1} and simultaneously increase g_{mb1}' such that the overall coefficient remains constant. g_{mb1} cannot be scaled down arbitrarily as its lower limit is determined by noise considerations and proper operation at the clock frequency (in the GHz range). Due to the limitations of these two approaches, the more practical approach of introducing losses through resistors is used to decrease the integration step at node V_x.

There are two non-idealities that modify the required open loop transfer function of the proposed architecture, given by (4.5). The first non-ideality is the finite Q of the bandpass filters and its main effect is the increase of the quantization noise floor, as discussed in Section 3.4.4. The other non-ideality which modifies the open transfer function is the introduction of losses in the integrator DAC. The ideal integrator DAC transfer functions in Fig. 4.4 ((b_1/s) and (b_3/s)) are replaced by the lossy integrator DAC

transfer functions ($(b_1/(s+a_1))$ and $(b_3/(s+a_2))$, a_1 and a_2 represent the losses in the integrator). The loop transfer function is calculated from the ADC output to the comparator input and the modified open loop transfer function due to the use of lossy integrator DAC's can be expressed as

$$H_{modified,loop}(s) = H_{loop}(s) + H_{error}(s) \tag{4.9}$$

$H_{loop}(s)$ is given by (4.5) and the error transfer function is given by

$$H_{error}(s) = -\left[\frac{s^3 a_2 A b_3 + s^2 a_1 (a_2 A b_3 + A^2 g_{m2} b_1) + s a_2 (a_1 A^2 g_{m2} b_1 + A\omega_o^2 b_3) + a_2 a_1 A \omega_o^2 b_3}{(s^2 + \omega_o^2)^2 (s + a_1)(s + a_2)}\right] \tag{4.10}$$

where a_1 and a_2 represent losses in the two integrator DAC's, $a_i = 1/R_iC_i$, refer to Fig. 4.8, ω_o and A are given by (4.6). For operation in a narrow bandwidth around the center frequency, the error transfer function can be simplified under the assumption that a_1, $a_2 << \omega_o$ (a_1, a_2 can be neglected in the denominator, numerator terms which are divided by s or s^2 can be neglected). The simplified error function is given by

$$H_{error}(s) \cong -\left[\frac{s\ a_2 A b_3 + a_1 (a_2 A b_3 + A^2 g_{m2} b_1)}{(s^2 + \omega_o^2)^2}\right] \ around\ \ \omega = \omega_0 \tag{4.11}$$

The error transfer function given by (4.11) represents a small deviation from the required loop transfer function provided the values of a_1 and a_2 are small. The earlier analysis of clipping at integrator outputs led to the conclusion that relatively large value of a_1 and a_2 is required in order to prevent clipping at the integrator output for robust ADC operation. The value of a_1 and a_2 used in this design is a tradeoff between these two opposing considerations and is chosen after extensive behavioral simulations. The value of a_1 and a_2 used in the ADC implementation is $6.67*10^8$ rad/sec. At the resonant frequency, the

main effects are small deviations of the first two coefficients in the loop transfer function, as shown in (4.11). These errors can be accounted for by changing the values of the loop coefficients (b_1, b_2, b_3 and b_4) in order to get the required values in (4.5) and are taken into account when the component values are calculated in the design. The behavioral simulations of the proposed ADC architecture was used to optimize the coefficients for best SNR and low power consumption (coefficient scaling) while maintaining reasonable signal swing at all internal nodes. The details of the behavioral simulation setup are given in the next section.

4.4. Behavioral simulations

Simulink and Matlab software simulation tools were used for the behavioral simulation of the CT BP ΣΔ ADC. The representation of the proposed ADC architecture in Simulink for behavioral simulations is shown in Fig 4.10. The model uses sub-blocks available from Simulink library to obtain the required loop transfer function. The s-domain (continuous time) transfer function block is used to realize the bandpass filters. For the resonator, d1 = ω_o/Q, d2 = ω_o^2 = 1/(L*C) and A = (1/C), where ω_o is the center frequency and Q is the quality factor of the bandpass filter. The integrator DAC with losses is implemented using the integrator sub-block, and current DAC is implemented using a simple multiplier block with the required coefficient to convert the digital bit into current. The saturation block is used at the output of bandpass filters and integrator blocks to limit the signal swing to the supply voltages (Vdd/Vss). The saturation block is

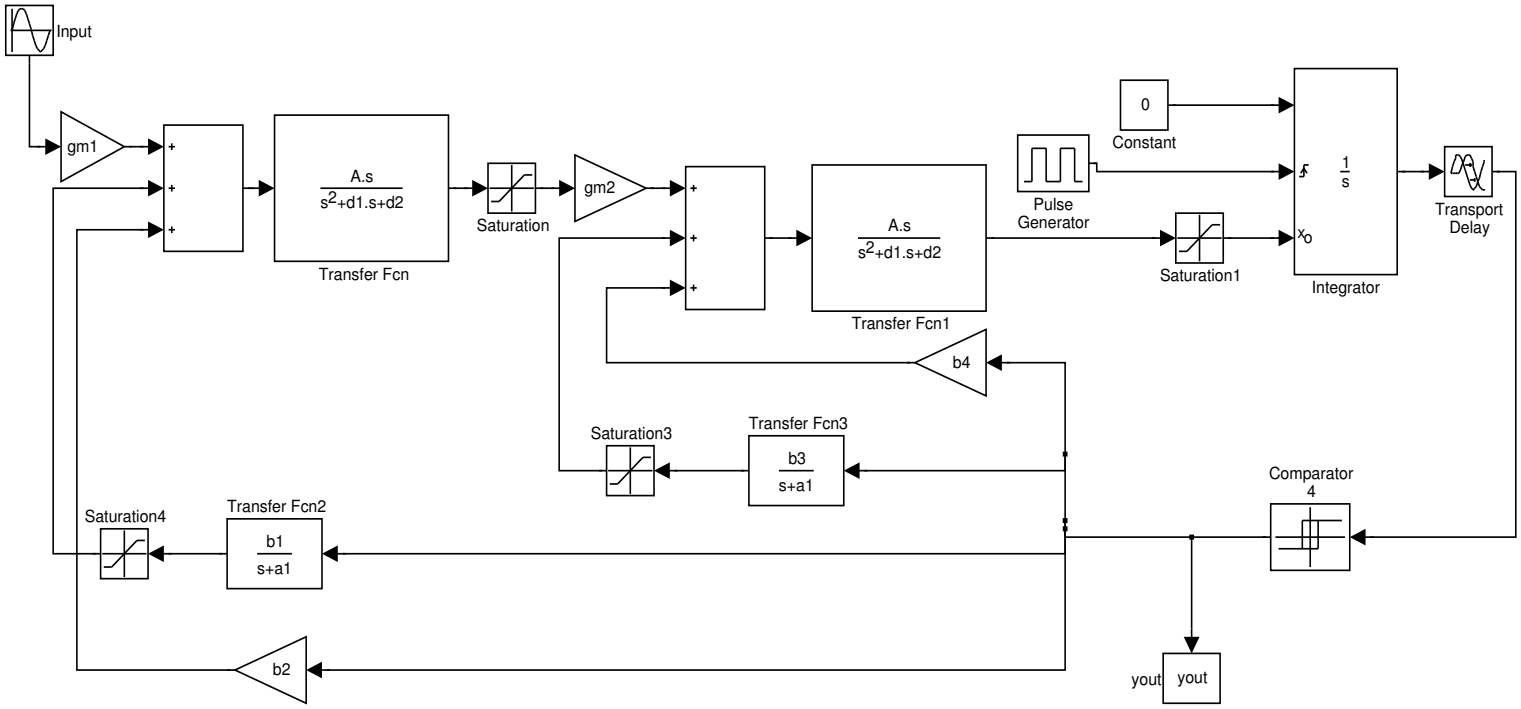


Fig. 4.10. RF ADC architecture in Simulink for behavioral simulations

not required for the current DAC as its output is a digital current pulse stream that follows the bit stream input. The summation of signals before each bandpass resonator occurs in current domain, which matches with the circuit implementation. The summation of the signals for the feedback path has a positive sign in the model, though the ADC is a negative feedback loop system. The main reason for this implementation is due to the fact that the overall phase shift of signals in the loop (together with the one clock period delay) ensures negative feedback.

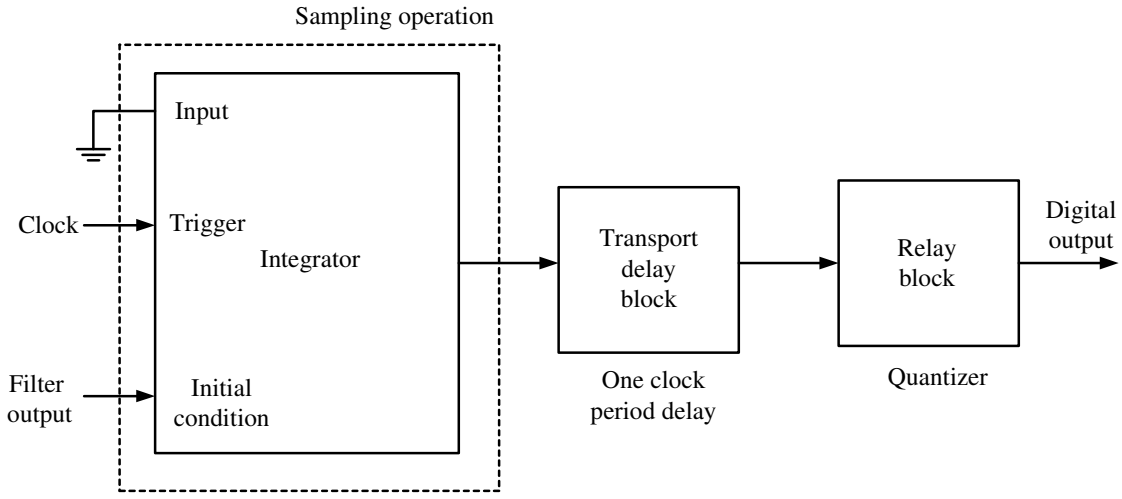


Fig. 4.11. Behavioral model of comparator in Simulink

The comparator is the only block which operates in discrete time mode and it performs the sampling and quantization operations every clock cycle. The behavioral model of the comparator in Simulink is shown in Fig. 4.11. The sampling operation is performed by grounding the input of an integrator block and using the bandpass filter

output as the initial condition. The rising edge of the clock signal is used as a trigger to capture the value of the filter output as the initial condition and since the input is zero, the output effectively samples the initial condition every clock cycle [50]. The z^{-1} delay (one clock period) is implemented using the transport delay block and the single bit quantizer is implemented using the relay block.

The input signal is a sine wave at 950 MHz and the sampling clock frequency is 3.8 GHz. The initial values of the coefficients are calculated by equating each coefficients of the numerator in (4.4) and (4.5) respectively (the initial values of the coefficients b_1, b_2, b_3 and b_4 calculated using this approach are $5.53*10^7$, 0.0098, $7.9*10^7$ and 0.0146, respectively). The behavioral simulation in Simulink has various parameters which determine whether the simulation is in continuous time or discrete time domain. The continuous time ode5 (Dormant-Prince) solver is used with fixed step option and the size of the step determines the accuracy of the simulation. A step size of 0.05*Ts seconds (Ts is the time period of the clock) is used for the model, which ensures very good accuracy of the behavioral simulations. At the architectural level, the loop coefficients and filter gain can be scaled down to reduce power consumption. The scaling of these two values results in scaling down of the signal swing at all the internal nodes of the ADC. The lower limit for scaling is determined by the noise level for the required dynamic range at the output of the ADC. For the integrator DAC's, the main consideration is the amount of losses required to ensure that the output doesn't clip a certain number of consecutive 1's or 0's. The behavioral simulations of the CT BP ΣΔ ADC is done for various values of amplitude for the input sine wave signal. The lowest

level is the input amplitude when the output SNR is zero dB (signal power is equal to the noise power), while the largest level is the input amplitude when the total power of the distortion components is higher than the noise power (integrated over the signal bandwidth). The signal swing at all internal nodes of the ADC must be within the supply voltages over the entire input signal range. This ensures stable operation of the ADC and is verified by extensive behavioral simulations.

Table 4.2. Values of optimized loop coefficients for the RF ADC

Coefficient	**Value**
b_1	$5.13*10^7$(Amps*rad/Volt*sec)
b_2	0.0091 (Amps/Volt)
b_3	$7.44*10^7$ (Amps*rad/Volt*sec)
b_4	0.0139 (Amps/Volt)
a_1, a_2	$6.67*10^8$ rad/sec

The SNR of the output bit stream is calculated by dividing the power of signal over the quantization noise power in frequency spectrum. The power spectrums are estimated using the fft function in Matlab, and the bit stream is first preprocessed using a Hanning window in order to prevent the leakage in frequency spectrum caused by taking the Fourier transform of a truncated bit stream. The value of the optimized loop coefficients that is used in the implementation of the ADC is shown in Table 4.2. The

optimization process involved scaling down the coefficients and transconductance values, which decreases the power consumption and also brings down the signal levels closer to the noise floor. The optimization process should also maintain reasonable signal swing at all internal nodes of the ADC for all possible values of the input signal. The coefficients were optimized as tradeoff between power and noise, while obtaining the best SNR at the output of the ADC. The circuit implementation and simulation results of the ADC are presented in the next section.

4.5. Circuit implementation and simulation results

The main building blocks of the CT BP ΣΔ ADC are the LC bandpass filter, integrator DAC, current DAC and the comparator. The details of the circuit implementation and post layout simulations results of these building blocks are presented in this section. The ADC is implemented in IBM 0.25 μm SiGe BiCMOS technology, which offers the flexibility of using both bipolar and MOS transistors. High speed bipolar junction transistors (BJT) of this technology have a transition frequency (f_T) of 47 GHz and are used for transistor implementation in the signal path.

4.5.1. Q-enhanced LC bandpass filter

The input voltage to the bandpass filter is converted to current using a transconductance stage and then injected into the LC tank. The differential output voltage (V_{od}) of a BJT differential pair without any linearization is given by

$$V_{od} = \frac{\beta}{1+\beta} I_{tail} R_L \tanh\left(\frac{V_{id}}{2V_T}\right) \tag{4.12}$$

where β is the collector current gain of the BJT, V_{id} is the input differential voltage, I_{tail} is the tail current, R_L is the load resistor and V_T is the thermal voltage (V_T = kT/q = 26 mV at room temperature, K is the Boltzman constant, T is the temperature and q is the electronic charge). The main considerations in the design of the transconductor are linearity, noise and power consumption. The nominal input voltage range (V_{id}) for linear operation is around 20 mV_{p-p} and emitter degeneration resistors (R_e) are used to enhance the input linear range. The effective transconductance of a emitter degenerated BJT differential pair is given by

$$g_{m,diffpair} = \frac{g_m}{1+g_m R_e} \tag{4.13}$$

where $g_m = (I_c/V_T)$, I_c is the collector current ($I_c = I_{tail}/2$) and g_m*R_e is called the emitter degeneration factor. When $g_m*R_e >> 1$, the effective transconductance of the linearized differential pair is $(1/R_e)$. The third harmonic distortion (HD3) of a emitter degenerated BJT differential pair is given by

$$HD3 = \frac{1}{24}\left(\frac{V_{id}}{(1+g_m R_e)V_T}\right)^2 \tag{4.14}$$

The third order intermodulation distortion (IM3) is three times the value of HD3 [3]. The HD3 decreases by a factor of $(1+ g_m*R_e)^2$ as compared to a differential pair without any linearization, at the cost of higher noise and power consumption. The addition of resistors R_e also increases the noise floor of the differential pair. The total input referred noise for the emitter degenerated BJT differential pair is given by

$$V_{in,noise}^2 = \frac{8qV_T^2}{I_{tail}}(1 + g_m R_e) + 8kTr_b \tag{4.15}$$

where r_b is the base resistance of the BJT. The first term of (4.15) refers to the shot noise contribution of the BJT, which increases by a factor of (1+ g_m*R_e) as compared to the case without any degeneration. The emitter degeneration factor used in this design is 5 as an optimum tradeoff between noise, linearity and power consumption, which results in an input linear range of 120 mV_{p-p} for the BJT differential pair.

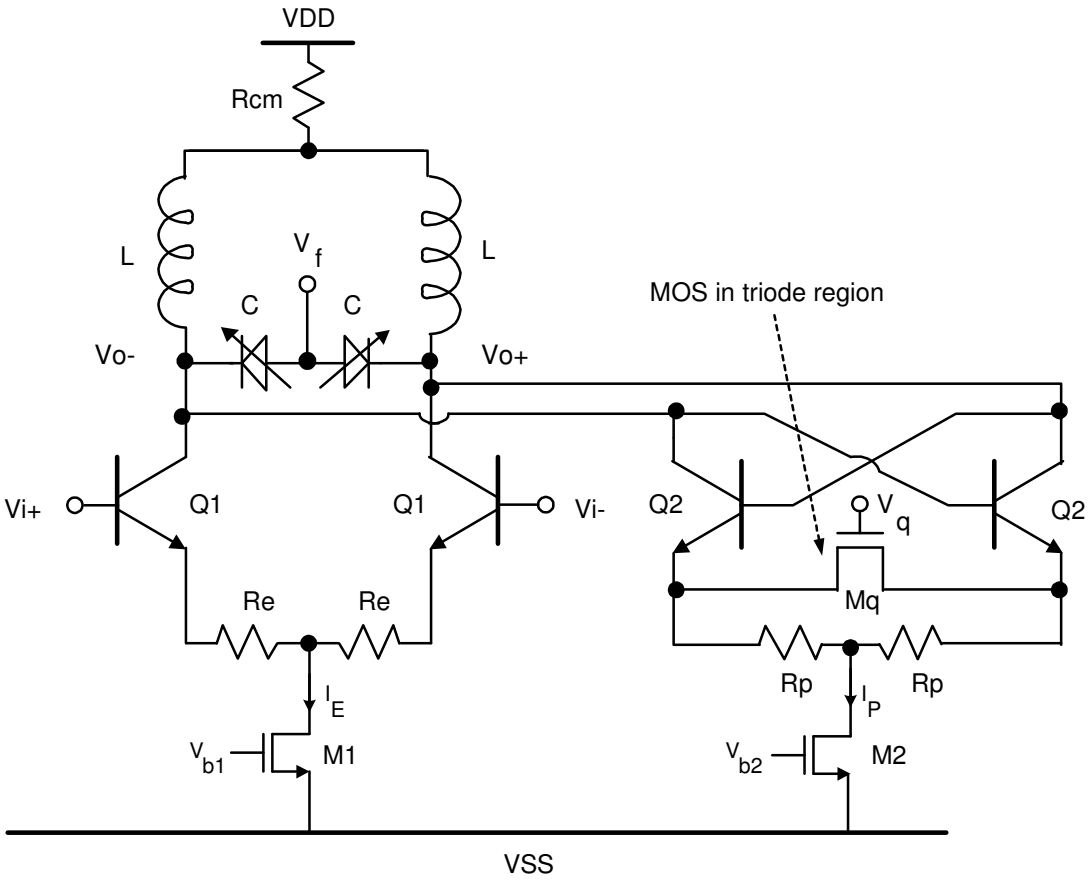


Fig. 4.12. Schematic of the second order Q-enhanced LC bandpass filter

The schematic of the second order Q-enhanced LC bandpass filter is shown in Fig. 4.12. The differential pair formed by transistors Q1 performs linear V-I conversion and the current is injected into the LC tank. The Q-enhancement block to replenish the losses in the LC tank is realized using a cross-coupled BJT differential pair formed by transistors Q2, which have emitter degeneration (R_p in parallel with triode transistor) to enhance its linearity. The linearization minimizes the distortion components that are introduced in the LC tank from the cross-coupled pair, but reduces the quality factor (Q) tuning range of the bandpass filter. The gate control voltage (V_q) of a NMOS transistor (Mq) operating in triode region is used to tune the Q of the bandpass filter. M_q is connected in parallel with a linear resistor to avoid linearization degradation due to the non-linear operation of the triode connected transistor. The resistance of M_q operating in triode region is given by

$$R_{Mq} = \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}\left(V_{gs} - V_{th}\right)} \tag{4.16}$$

where μ_n is the majority carrier mobility in the n-channel, C_{ox} is the oxide capacitance, W_n and L_n are the width and length of the NMOS transistor, V_{gs} is the gate source voltage and V_{th} is the threshold voltage. The value of negative resistance of the cross coupled pair, as seen from the collectors of transistors Q2 is given by

$$R_{neg} = -\frac{2}{g_{m,eff}} \tag{4.17}$$

where

$$g_{m,eff} = \frac{g_{m2}}{1 + g_{m2}\left(R_p \parallel \frac{R_{Mq}}{2}\right)} \tag{4.18}$$

The Q-enhancement block increases the noise floor of the differential pair, with shot noise and base resistance thermal noise contribution from Q2, thermal noise contribution from triode transistor M_q and resistor R_p. For both the linearized differential pairs, the tail current is placed between the two degeneration resistors, R_e (and R_p). This ensures that the noise contribution of transistors M1 (and M2) becomes common mode noise and is rejected at the differential output, but the disadvantage is that additional voltage drops of 0.5*Ie*Re (and 0.5*Ip*Rp) have to be tolerated in the design. This voltage drop, along with V_{be} of transistor Q1 (Q2) and V_{dsat} of current mirror transistor M1 (M2), restrict the voltage swings while maintaining the transistors in the proper region of operation. The common mode voltage at the filter output is given by $V_{o,cm}$ = VDD - I_t*R_{cm}, where I_t = [I_e + I_p + sum of DAC currents connected to the resonator]. The resistor R_{cm} sets the common mode voltage of the filter and also for the DAC blocks that are connected to the resonator.

The value of the inductor and its quality factor (Q) depends on various factors such as geometry (shape, number of turns etc) and technology parameters (thickness and conductivity of metal layers and insulators, resistivity of substrate etc.) [51]. The IBM 0.25 μm SiGe technology offers custom inductors with a pre-determined shape on metal layers and some variable parameters (number of turns, distance between metal turns, hollowness etc) that are restricted to a certain range of values. The design of inductors in this process is simplified by these restrictions, which narrows the design space during

the optimization process where the Q of inductor is optimized at the filter's center frequency (950 MHz) while occupying minimum area. The value of the important parameters for the spiral inductor design is given in Table 4.3. The optimum value of inductance (L) in Fig. 4.12 for these parameters is 5.1 nH, which results in maximum Q at 950 MHz. The topmost metal layer is used in order to minimize the capacitance between the metal and the substrate. A mesh layer is used to shield the spiral inductor from the substrate, which increases the resistivity of the substrate beneath the spiral and decreases the inductor losses.

Table 4.3. Parameter values for spiral inductor design

Parameter	**Value**
Outer dimension	300 μm
Spiral width	15 μm
Number of turns	4.75
Underpass width	15 μm
Metal layer	6 (topmost layer)
Shape	Octagon

The variable capacitor in Fig. 4.12 is implemented using reverse-biased P-N junction varactors. The center frequency of the LC filter is tuned by varying the control voltage (V_f), which changes the reverse bias voltage ($V_r = V_o - V_f$) of the varactors. The depletion layer capacitance of the P-N junction under reverse bias conditions is given by

$$C_{dep} = \frac{C_{j0}}{\left(1 - \frac{V_r}{V_{bp}}\right)^{\frac{1}{n}}} \tag{4.19}$$

where C_{j0} is the capacitance for zero bias voltage, the value of n is a fitting parameter with a value between 2 and 3, V_{bp} is the built-in potential of the P-N junction . The nominal value of the differential varactor is 2.75 pF (2*C, C according to Fig. 4.12). The varactors can be tuned by a value of ± 20% from the nominal value by varying the control voltage (V_f). The parasitic capacitance at the output of the resonator (due to all components connected at the resonator output) and is around 110 fF. The overall Q of the LC filter is usually limited by the Q of the standalone inductor. The Q of the standalone varactor is around 40, while the Q of the inductors is around 7. The fourth order LC bandpass filter is implemented as a cascade of two second order LC filters. The component and current values used in the circuit implementation for the two LC filter blocks is shown in Table 4.4. The value of R_{cm} is different for the two filters as the transconductance of each stage and the value of feedback DAC currents that connect to them are different. A large shunt capacitor (40 pF) is added in parallel to R_{cm} in order to minimize the noise injection into the LC tank. This technology has certain metal density rules (each of the 5 metal layers need to be present at a certain density in the layout), and the extra space required to satisfy the density rules are used to implement the shunt capacitor. Though the area occupied by the shunt capacitor is large, it comes at no extra penalty and it improves the noise rejection (with the exception of noise from the power supply). The transconductance of the first stage does not affect the loop transfer function

Table 4.4. Component and current values for the LC bandpass filter

Parameter	First LC filter	Second LC filter
Q1, Q2 (emitter length)	3.1 µm, 2 µm	3.3 µm, 2 µm
R_e	110 Ω	100 Ω
R_p	325 Ω	325 Ω
R_{cm}	65 Ω	30 Ω
M1 (W/L)	180 µm / 0.5µm	200 µm / 0.5µm
M2 (W/L)	100 µm / 0.5µm	100 µm / 0.5µm
M_q (W/L)	15 µm / 0.25 µm	15 µm / 0.25 µm
I_E	2.3 mA	2.5 mA
I_P	0.95 mA	0.95 mA
$L_{nominal}$	5.1 nH	5.1 nH
$C_{nominal}$	2.75 pF	2.75 pF

and the required dynamic range at the ADC input determines the maximum range that it can be scaled down. When the ADC is used in a software radio system, similar to the one shown in Fig. 4.1, the output of LNA/VGA is usually in current mode and could be directly injected into the LC tank. This approach results in elimination of the first transconductor, which would further reduce the power consumption of the ADC.

The dynamic range of the ADC is mainly determined by the dynamic range of the input transconductance, Q-enhancement block and the DAC's that are connected to

the first resonator. The lowest signal that can be handled is limited by the total input noise contribution of these stages, while the maximum signal that can be handled properly is limited by the distortion components. The extracted simulations for the center

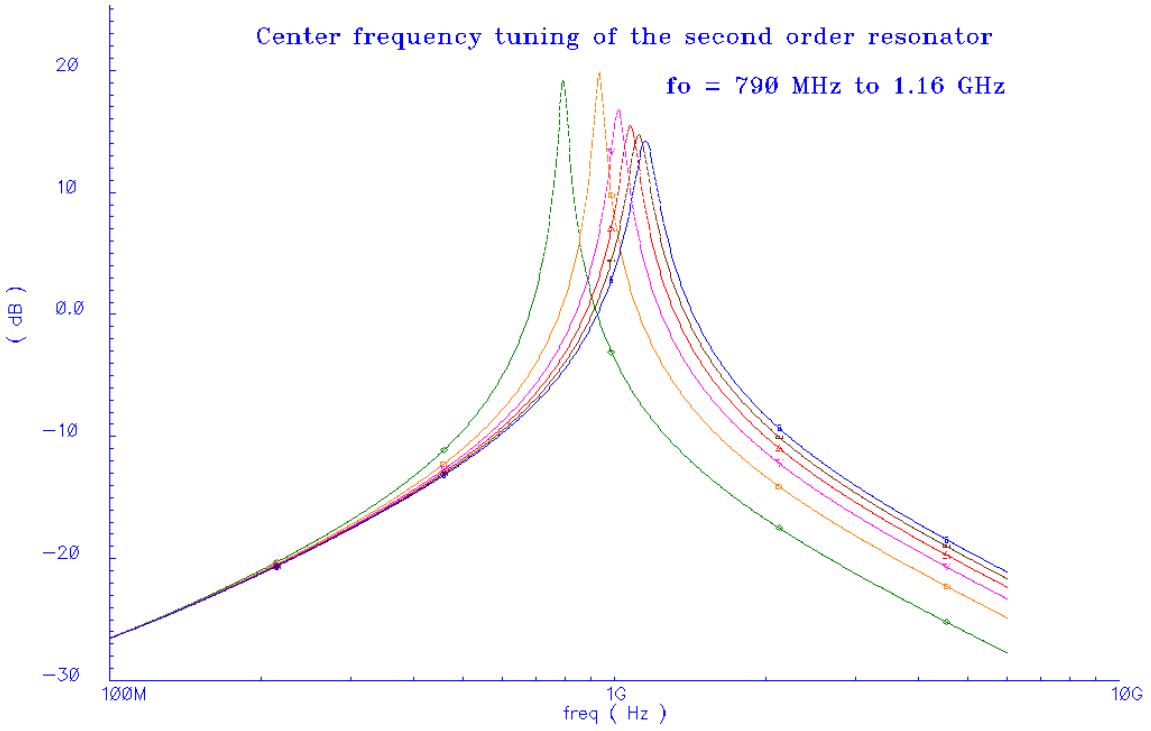


Fig. 4.13. Post-layout simulation of the bandpass filter – center frequency tuning

frequency tuning of the second order resonator is shown in Fig. 4.13 and the center frequency can be tuned from 790 MHz to 1.1.6 GHz. The post-layout simulation result for the Q tuning of the second order resonator is shown in Fig. 4.14 and the Q of the resonator can be varied from a value of 7 to 26 using the gate voltage of the triode transistor.

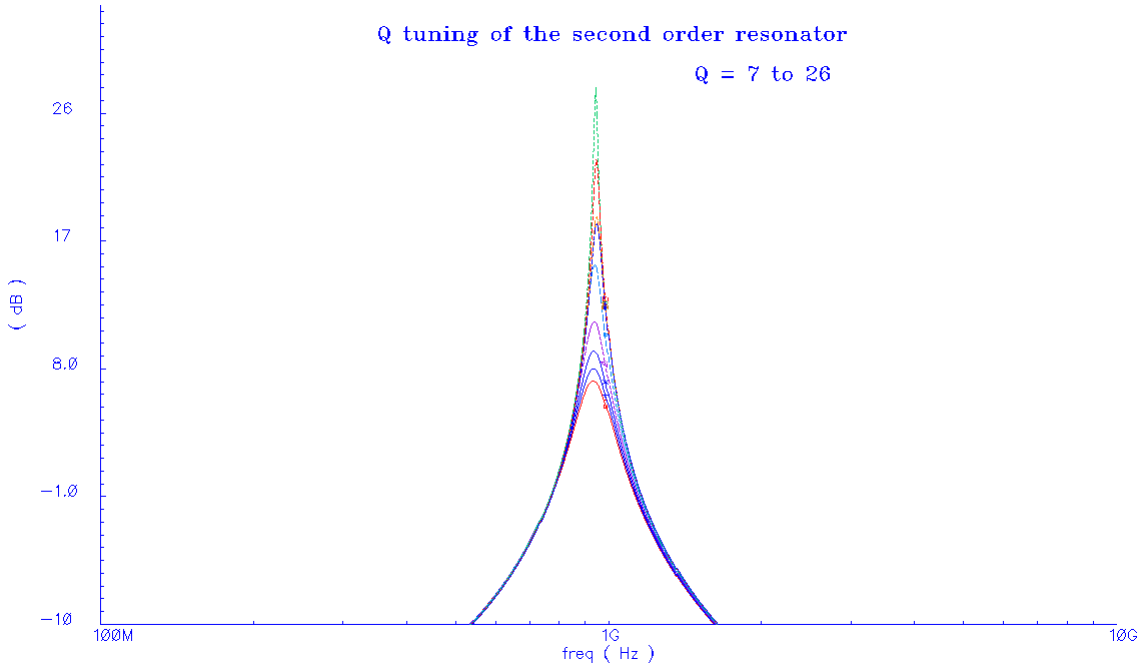


Fig. 4.14. Post-layout simulation of the bandpass filter – Q tuning

The distortion performance of the filter was calculated by applying two tone input (each -7 dBm at 949 MHz and 951 MHz) to the second order resonator and the post-layout simulation result is shown in Fig. 4.15, which indicate IM3 value of 63 dB. The simulation was performed by injecting the two tones at the input with the output nodes shorted by voltage sources with proper DC bias and the output current is plotted in Fig. 4.15 (power levels denote power of output current). The combined noise level of the input transconductance and Q-enhancement block measured from post-layout simulations, integrated in a 200 kHz and 1 MHz bandwidth around 950 MHz are 0.683 µV and 1.527 µV, respectively.

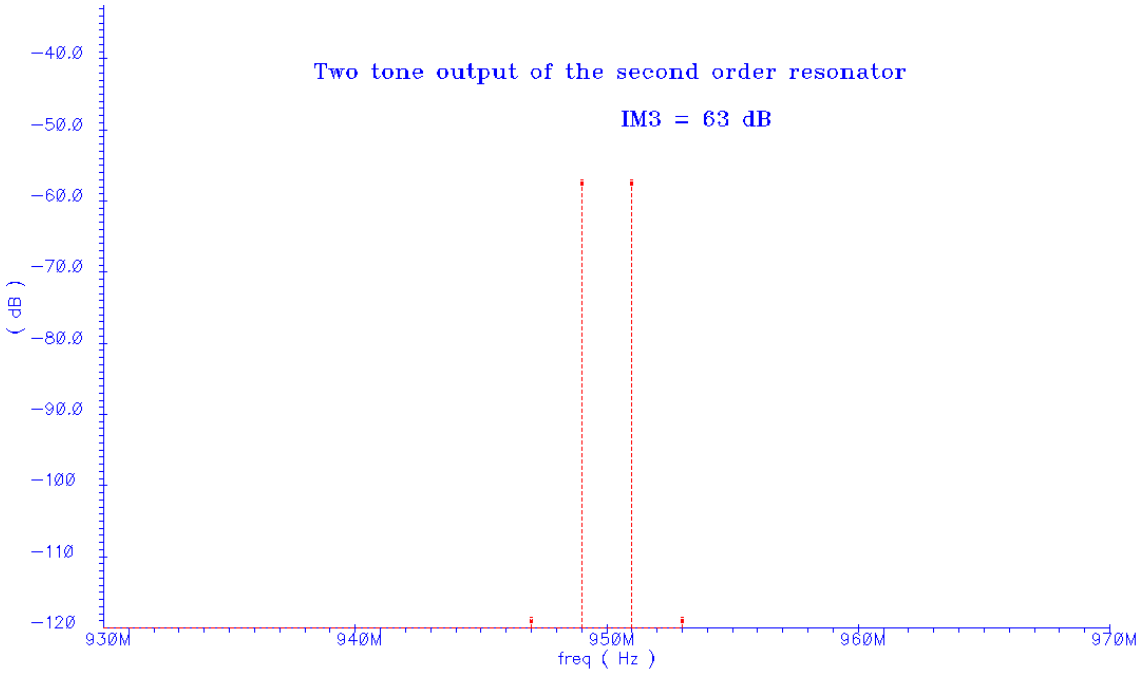


Fig. 4.15. Post-layout simulation of the bandpass filter – two tone test

4.5.2. Integrator DAC

The schematic of the integrator DAC is shown in Fig. 4.16. The digital NRZ bit stream from the comparator outputs is converted into current by the differential pair formed by transistor Q3, and the current is integrated by capacitor C1. Finite gain of the differential pair (g_{m3}*[r_{o3} ‖ r_{ds4}]) makes this a lossy integrator, but as explained in Section 4.3, extra losses are required to introduce soft clipping and improve the operating range. The resistors R1 are added at the output of the integrator to introduce extra losses and they also set the output common mode voltage (Vcm, applied at the

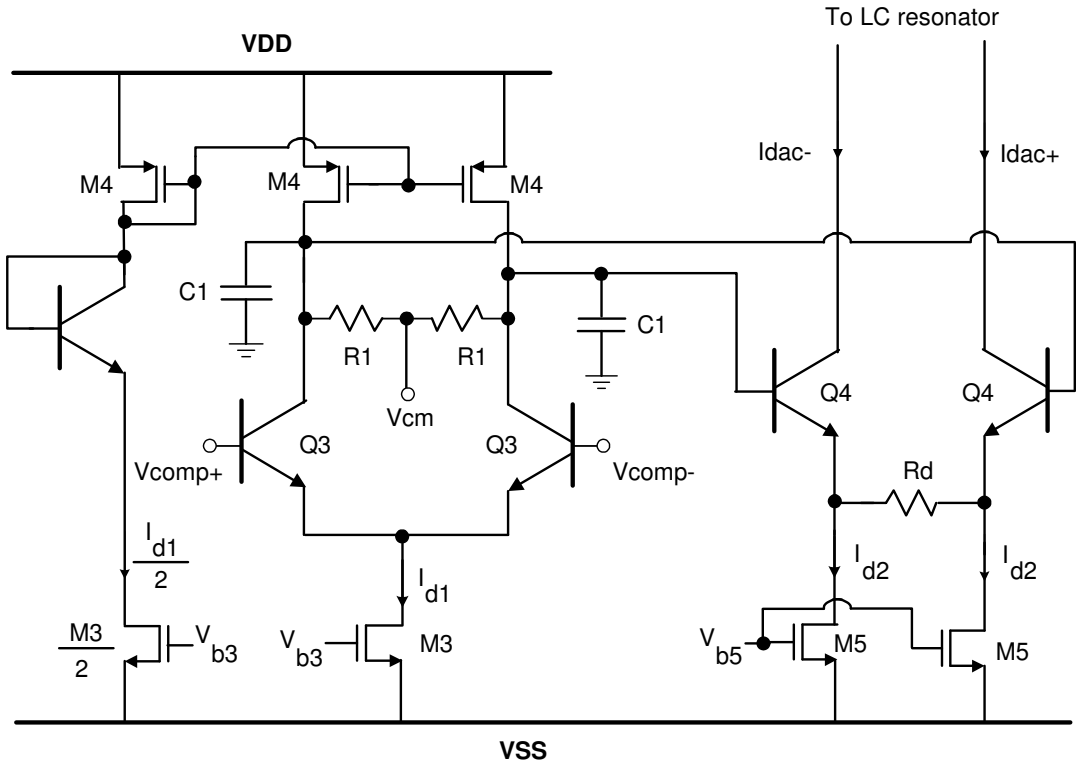


Fig. 4.16. Schematic of the integrator DAC

node between the two resistors R1) of the differential integrator. The output of the integrator is in voltage mode, and it needs to be converted into current in order to be injected back into the LC resonator. This V to I conversion has to be very linear, especially when the current is injected back into the first LC tank where it directly mixes with the input signal. Any non-linearity that is introduced by the integrator DAC connected to the first stage is not suppressed by the feedback loop and it directly appears at the ADC output. A differential pair (formed by transistors Q4) with emitter degeneration resistor Rd is used to convert the integrated output to current; a large tail

current (3 mA) is used in this stage to maintain its linearity. The overall transfer function for the integrator DAC is given by

$$\left(\frac{i_{out}}{V_{in}}\right)_{IDAC} = \frac{I_{dac+} - I_{dac-}}{V_{comp+} - V_{comp-}} \cong I_{d1}\left(\frac{R1}{1+s(R1*C1)}\right)\left(\frac{g_{m4}}{1+\frac{g_{m4}Rd}{2}}\right) sign(V_{in}) \quad (4.20)$$

where sign(Vin) denotes the polarity of the digital output bit stream (+1 for high and -1 for low). The value of coefficients (b1 and b3) of the integrator DAC's from Table 4.2 can be used to determine the component values for the circuit implementation. The value of I_{d1} is chosen based on the maximum integration step that can be accommodated

Table 4.5. Component and current values for the integrator DAC

Parameter	**DAC connected to first resonator**	**DAC connected to the second resonator**
Q3, Q4 (emitter length)	1.1 µm, 2.5 µm	1.1 µm, 2.5 µm
R1	1.5 kΩ	1.5 kΩ
R_d	250 Ω	178 Ω
C1	1 pF	1 pF
M3 (W/L)	120 µm / 0.8µm	120 µm / 0.8µm
M4 (W/L)	50 µm / 0.5µm	50 µm / 0.5µm
M5 (W/L)	240 µm / 0.8µm	240 µm / 0.8µm
I_{d1}	1 mA	1 mA
I_{d2}	1.5 mA	1.5 mA

during each clock cycle for proper operation of the ADC. The tuning of the integrator DAC coefficient is achieved by changing the value of the current I_{d1}. The emitter degenerated differential pair is not used for tuning the coefficient because the tuning range obtained by varying I_{d2} (varying g_{m4}) is very small. A triode transistor could be used for the implementation of R_d which will provide a variable resistance for the coefficient tuning, but the downside is that the non-linearity of the triode transistor will appear at the ADC output (which is critical especially for the integrator DAC that is connected to the first resonator). The component and current values used in the circuit implementation for the two integrator DAC blocks is shown in Table 4.5.

4.5.3. Current DAC

The schematic of the current DAC is shown in Fig. 4.17. The digital NRZ bit stream from the comparator outputs is converted into current by the differential pair formed by transistors Q5, and the current is directly injected into the LC resonator. The current DAC acts like a simple switch by simply injecting/extracting the tail current for logic 1 or 0 value. The value of coefficients (b2 and b4, which are represented as a

Table 4.6. Component and current values for the current DAC

Parameter	DAC connected to the first resonator	DAC connected to the second resonator
Q5 (emitter length)	1.2 μm	1.2 μm
M6 (W/L)	120 μm / 0.8μm	150 μm / 0.8μm
I_{d3}	1.33 mA	1.77 mA

fraction of the transconductances of LC filter blocks to which they are connected) for the current DAC's from Table 4.2 can be used to determine values of the tail current. The current DAC coefficient can be tuned by directly changing the value of the current I_{d3}. The component and current values used in the circuit implementation for the two integrator DAC blocks is shown in Table 4.6.

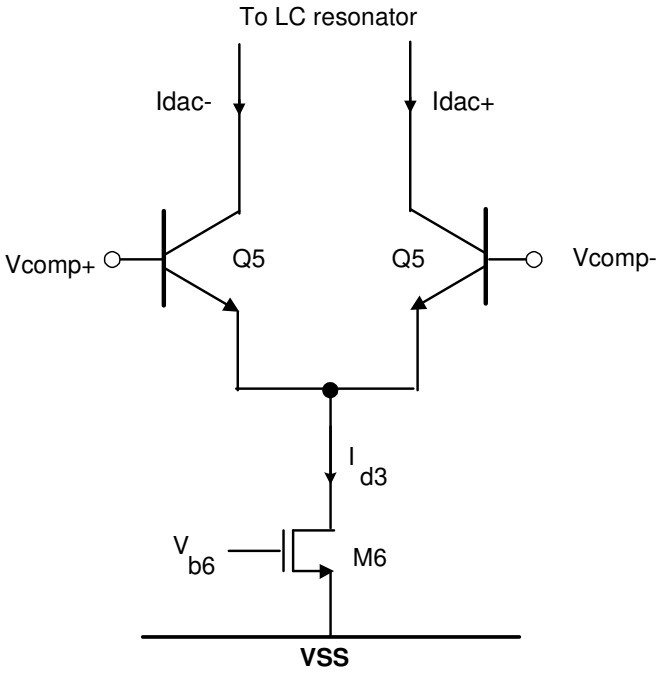


Fig. 4.17. Schematic of the current DAC

4.5.4. Comparator

The single-bit NRZ comparator samples the output of the fourth order filter and quantizes the sampled value to logic 1 or 0. Both the input and output of the comparator block are fully differential, which implies a threshold of ground (power supply is ± 1.25

V) for the quantizer. The block diagram for the circuit implementation of the comparator is shown in Fig. 4.18. The preamplifier gain stage is a simple gain stage and provides extra amplification for signals before the quantizer. The switching action in the comparator causes the comparator output to couple back to the input (to the filter bandpass in this case), which degrades the signal in the form of transient noise. This phenomenon is called kickback effect and it degrades the signal at the comparator input (thereby causing errors in the operation of the comparator) for high clock frequencies [13]. Emitter follower stages are used to isolate the gain stages, and before the DAC to provide isolation and minimize the comparator kickback effect. The signal swing in the comparator should be within the power supply (± 1.25 V) and a DC level shifter is required before the gain stage and the first latch to maintain all transistors in proper operating region. The latch block samples the filter's output and also performs the quantization operation. Extra latch stages are introduced to decrease metastable behavior and the extra delay is already accounted in the loop transfer function.

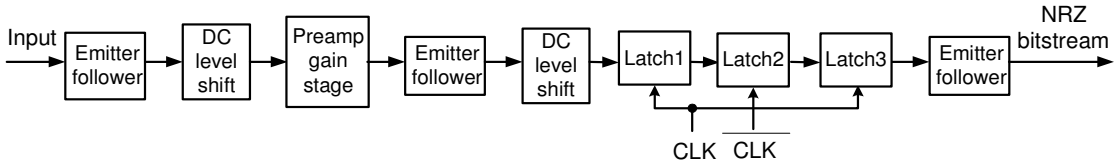


Fig. 4.18. Block diagram of the comparator implementation

The schematic of the preamplifier gain stage is shown in Fig. 4.19 and it consists of a simple BJT differential pair with load resistors. The DC level shift is achieved by

using a C-R high pass network, where the series capacitor 10 pF is used for AC coupling of signals and the required DC voltage is applied through a 2 KΩ resistor. The pole created by this high pass network ($f = \frac{1}{2\pi RC}$) is at 8 MHz, and is chosen such that all signals propagating through the comparator lie above this frequency. The choice of this pole location is a tradeoff due to area constraints. The input referred offset of the preamplifier gain stage should be minimized but it doesn't degrade the performance of

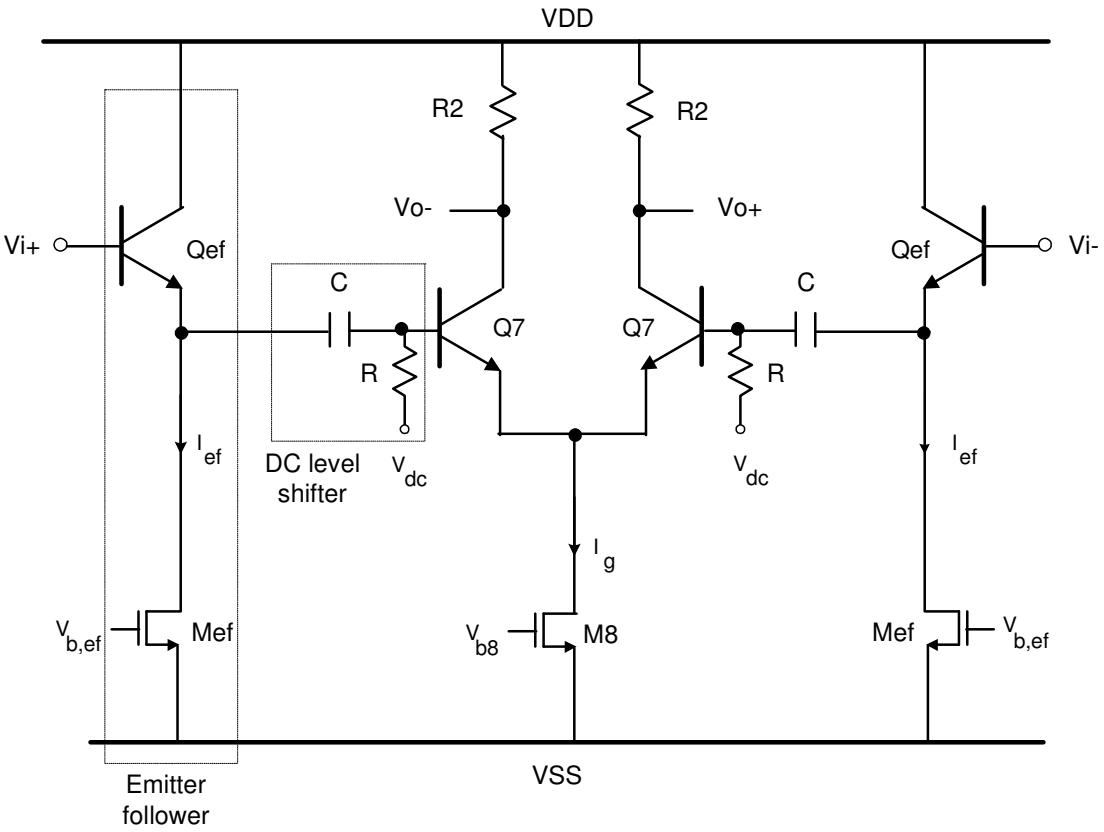


Fig. 4.19. Schematic of the preamplifier gain stage

the ADC as it is rejected by the noise shaping feedback loop, similar to the effect of the quantization noise. However, a signal dependent offset would introduce distortion components at the ADC output.

The schematic of the latch implementation is shown in Fig. 4.20. When the differential clock signal is high, the differential pair formed by transistors Q8 is active and it amplifies the input signal. At the time instant of the falling clock edge, the signal is sampled and the value at that time instant becomes the initial condition for the next clock phase. When the clock is low, the positive feedback cross coupled differential pair formed by transistors Q9 is active and the output reaches either logic 0 or 1. The

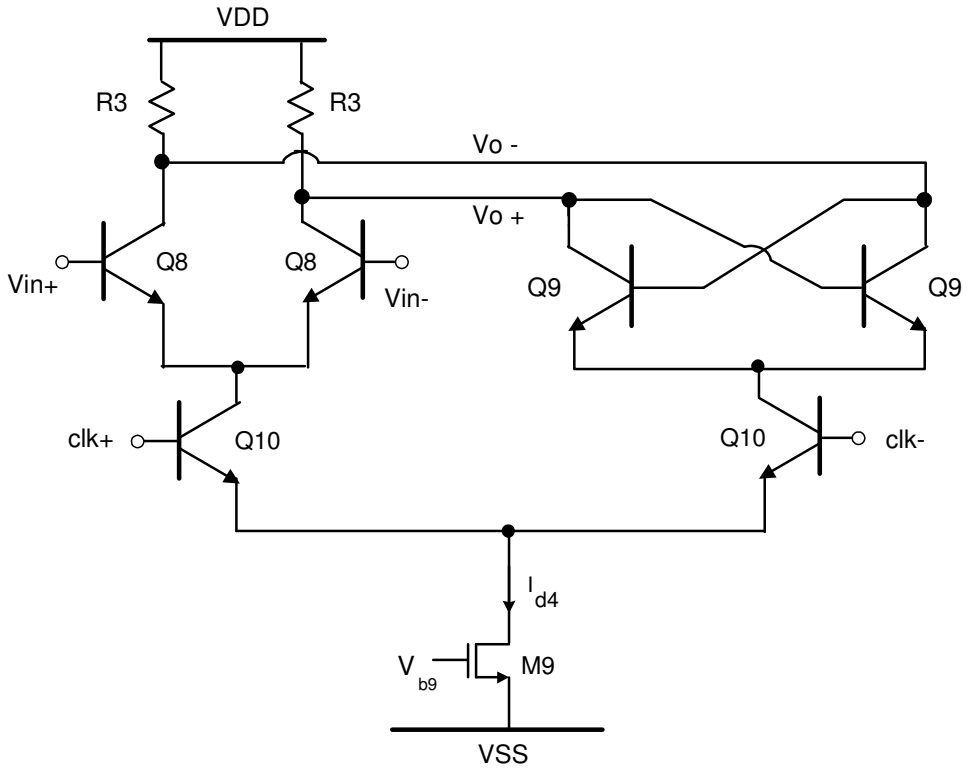


Fig. 4.20. Schematic of the latch

regeneration time of the latch, defined as the time taken for the output to reach a logic decision is given by [13]

$$T_{regeneration} = \frac{\tau_{\text{latch}}}{g_{m9}R_3 - 1} \ln\left(\frac{V_{o,latch}}{V_{latch,t=0}}\right) \tag{4.21}$$

where τ_{latch} is the time constant of the latch (equal to the product of resistance and the total capacitance at the output node), $V_{o,\text{latch}}$ is the output voltage for either logic 0 or 1 and $V_{\text{latch},t=0}$ is the initial condition at the output. The regeneration time increases for very small value of inputs and it can be decreased by increasing g_{m9} (increase in I_{d4}), which results in higher power consumption. The value of resistor, R3, cannot be increased arbitrarily as it affects the output signal swing. A cascade of three latches driven by different clock phases results in $z^{-1/2}$ delay. The propagation delay in comparator, DAC's and routing parasitics adds to this delay and the resulting worst case total delay (from simulations) is less than one clock period (z^{-1} delay). This approach of incorporating circuit propagation delays (carefully adjusted according to post layout simulations) in the required overall delay helps to overcome the excess loop delay problem in this design. The blocks that can be optimized at circuit level are the comparator and transconductor of the first LC filter, as the current consumption of other blocks are determined by the loop transfer function. The currents in the comparator are scaled down as much as possible while maintaining proper operation (no bit error) at 3.8 GHz clock frequency (time period of 263 ps). The third latch consumes higher current in order to drive the parasitic capacitance at the base of the emitter follower, which is its subsequent block.

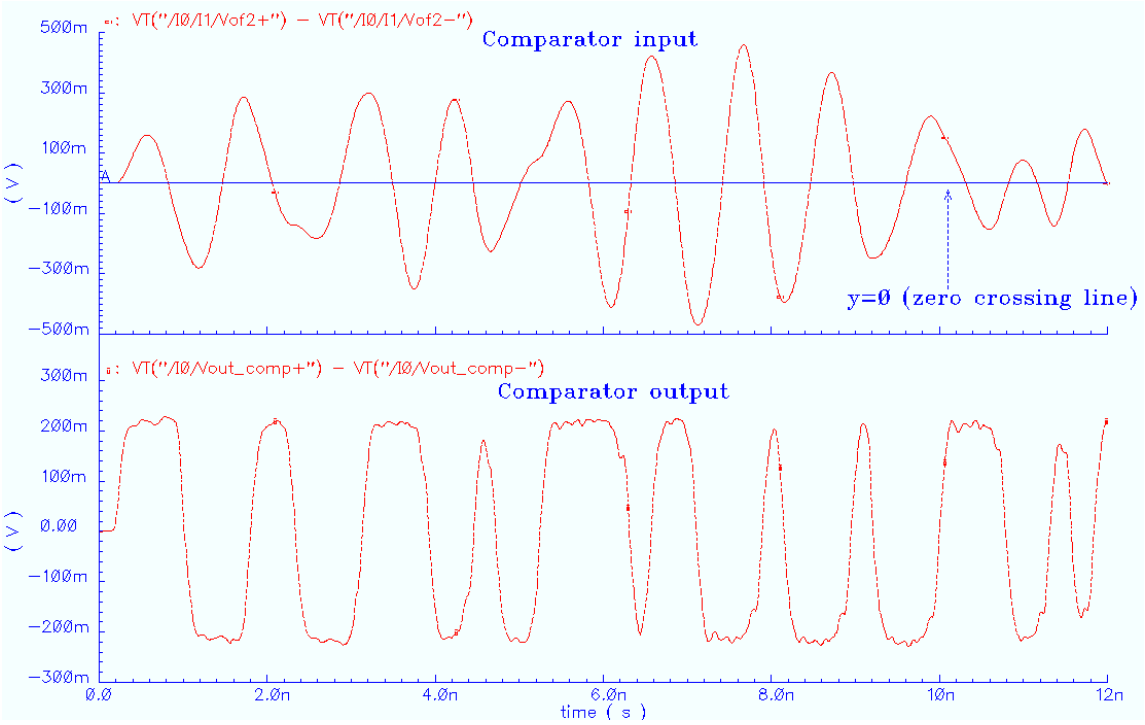


Fig. 4.21. Transient post-layout simulation result of the comparator

The input and output waveforms of the comparator from post-layout simulations are shown in Fig. 4.21. The differential output swing of the comparator is around ± 200 mV, which is sufficient to drive the subsequent DAC stages. The differential offset at the comparator input is around 0.4 mV and the time delay in the comparator (regeneration time of the latches) was around 40 ps (both values are from post-layout simulations). The comparator can resolve input signals greater than 1 mV without any errors at its output. The output of the comparator has to drive an external load (50 Ω of spectrum analyzer) for measurement purpose and an output buffer is used to properly drive the bit stream. The component and current values for the preamplifier and the latch blocks of the comparator are shown in Table 4.7 and Table 4.8, respectively.

Table 4.7. Component and current values for the preamplifier gain stage

Parameter	Value
Q7, Qef (emitter length)	1.2 µm, 1.5 µm
R2	600 Ω
R	2 KΩ
C	10 pF
M8 (W/L)	50 µm / 0.4 µm
Mef (W/L)	60 µm / 0.4 µm
I_g	0.9 mA
I_{ef}	1.2 mA

Table 4.8. Component and current values for the latch stages

Parameter	Latch1	Latch 2	Latch 3
Q8, Q9, Q10 (emitter length)	1.3 µm, 1.3 µm, 1.2 µm	1.3 µm, 1.3 µm, 1.2 µm	1.4 µm, 1.4 µm, 1.5 µm
R3	400 Ω	400 Ω	325 Ω
M9 (W/L)	40 µm / 0.4 µm	40 µm / 0.4 µm	60 µm / 0.4 µm
I_{d4}	1.15 mA	1.15 mA	1.6 mA

4.5.5. Output and clock buffer

The output buffer is used to drive the differential bit stream into the spectrum analyzer load and the clock buffer is used to drive the input clock signal to the comparator. The schematic of the output buffer is shown in Fig. 4.22 and the clock

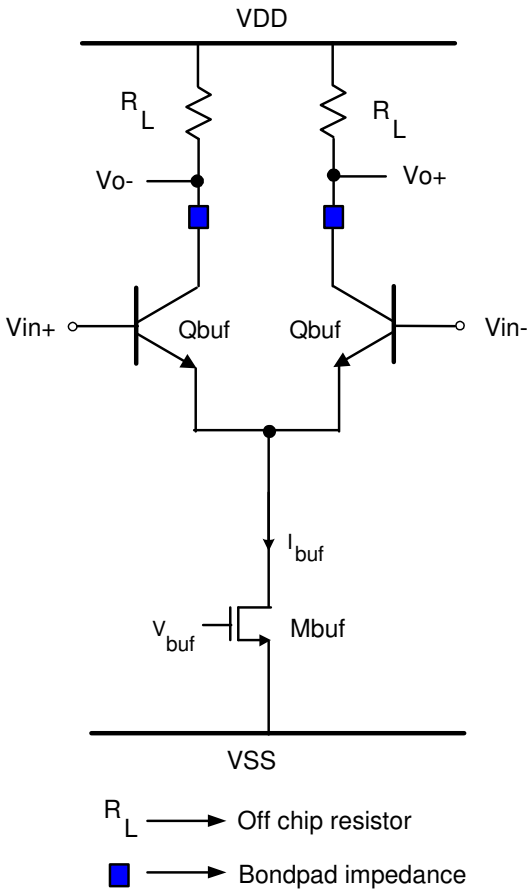


Fig. 4.22. Schematic of the output buffer

buffer has a similar implementation, except that the load resistors (R_L) are implemented on-chip and the bond pad impedance appears before the input rather than at the output. DC level shifting blocks, similar to the one shown in Fig. 4.19, are used to set the correct

DC bias at the input and output of both the clock and output buffers. The component and current values for the circuit implementation of the output and clock buffers are shown in Table 4.9.

Table 4.9. Component and current values for the buffer stages

Parameter	Output buffer	Clock buffer
Qbuf (emitter length)	4.2 μm	2.5 μm
R_L	150 Ω	40 Ω
Mbuf (W/L)	50 μm / 0.24 μm	25 μm / 0.24μm
I_{buf}	5 mA	2.6 mA

4.6. Top level simulations

The individual blocks described in Sections 4.5.1 to 4.5.5 are connected together according to the architecture shown in Fig. 4.5, in order to obtain the top level circuit implementation of the ADC. The transient simulation of the ADC is performed in Cadence by applying a test input signal at 950 MHz. Impedance matching blocks are used both at the input and output to ensure proper coupling of all signals. The output bit stream is written to a file using the "printvs" command available in Analog artist calculator tool. The output bit stream file is processed in Matlab and the SNR of the ADC is calculated by using the FFT command. The power spectrum at the ADC output from post-layout simulations is shown in Fig. 4.23. The number of samples used is 16384 and the output SNR was 56 dB in a 1 MHz bandwidth around 950 MHz. The

number of samples is restricted by the limited computing resources, since a top level extracted simulation can take about 5 days to generate 16384 samples. A higher number of samples (65536 samples) are required to get a more accurate estimate of signal and

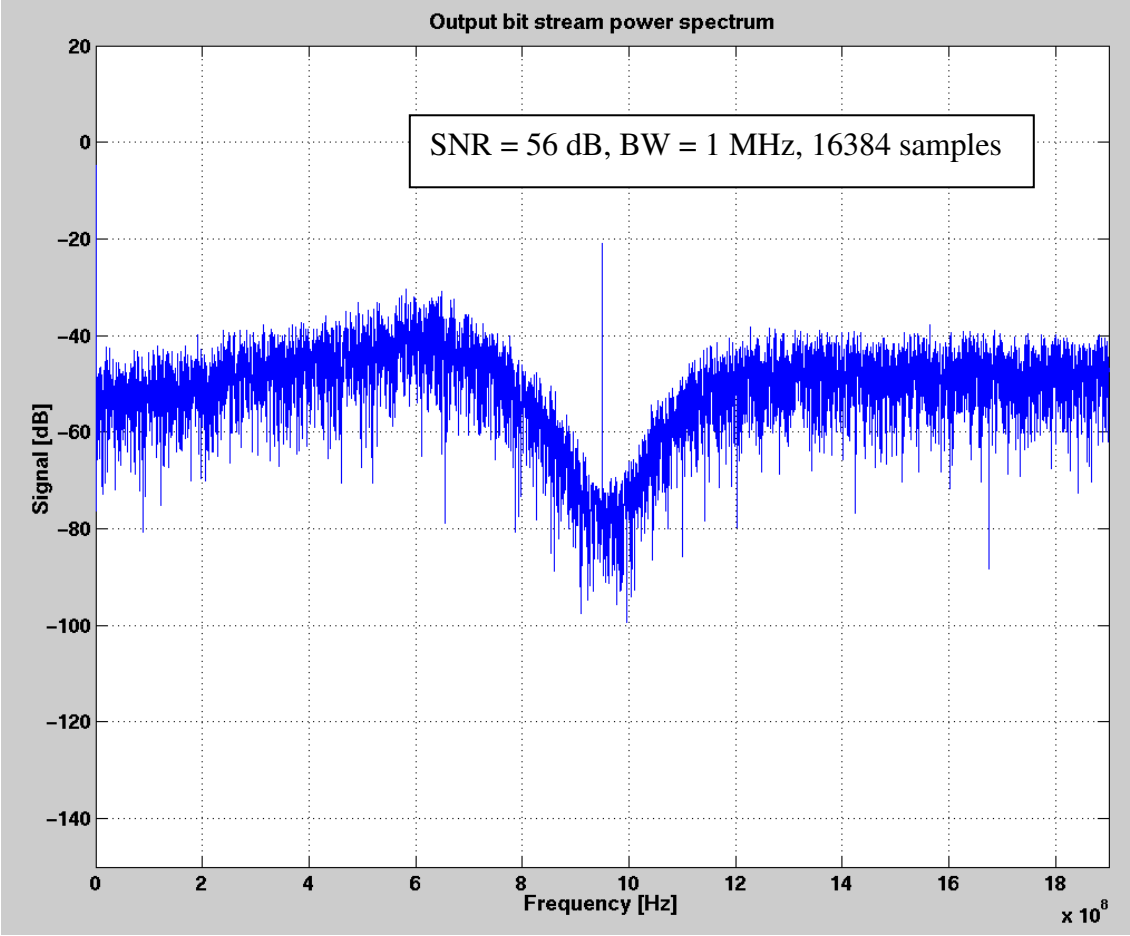


Fig. 4.23. Post-layout simulation of the ADC – output spectrum

noise power values. The current consumption of the different ADC blocks is shown in Table 4.10. The largest share of power consumption is from the comparator block and is about 41%. The stringent linearity requirements increases the power consumption in

both the bandpass filter and the integrator DAC's. Power optimization is done both at architecture and circuit level while maintaining the dynamic range and stability of the ADC. A very straightforward way to increase the signal bandwidth while maintaining the same resolution in ΣΔ converters is to use a multi-bit architecture. In this design, increasing the single bit comparator to a two bit comparator would require four comparators instead of one, along with more digital blocks for encoding the bit stream. From Table 4.10, it can be seen that this would increase the overall power consumption by more than 125%. This increase in power consumption is accompanied only by a 6 dB increase in SNR (increasing the comparator by 1 bit increases the SNR by 6 dB). This indicates that increasing the comparator resolution is not a power efficient technique for ADC's working with GHz clock frequencies.

Table 4.10. Current consumption of different ADC blocks

Block	**Current consumption**	**Percentage of overall power**
Bandpass filter + Q enhancement	6.7 mA	22.3 %
Integrator DAC's	8 mA	26.7 %
Current DAC's	3.1 mA	10.3%
Comparator with z^{-1} delay	12.2 mA	40.7 %
TOTAL	30 mA	100 %

4.7. Measurement results

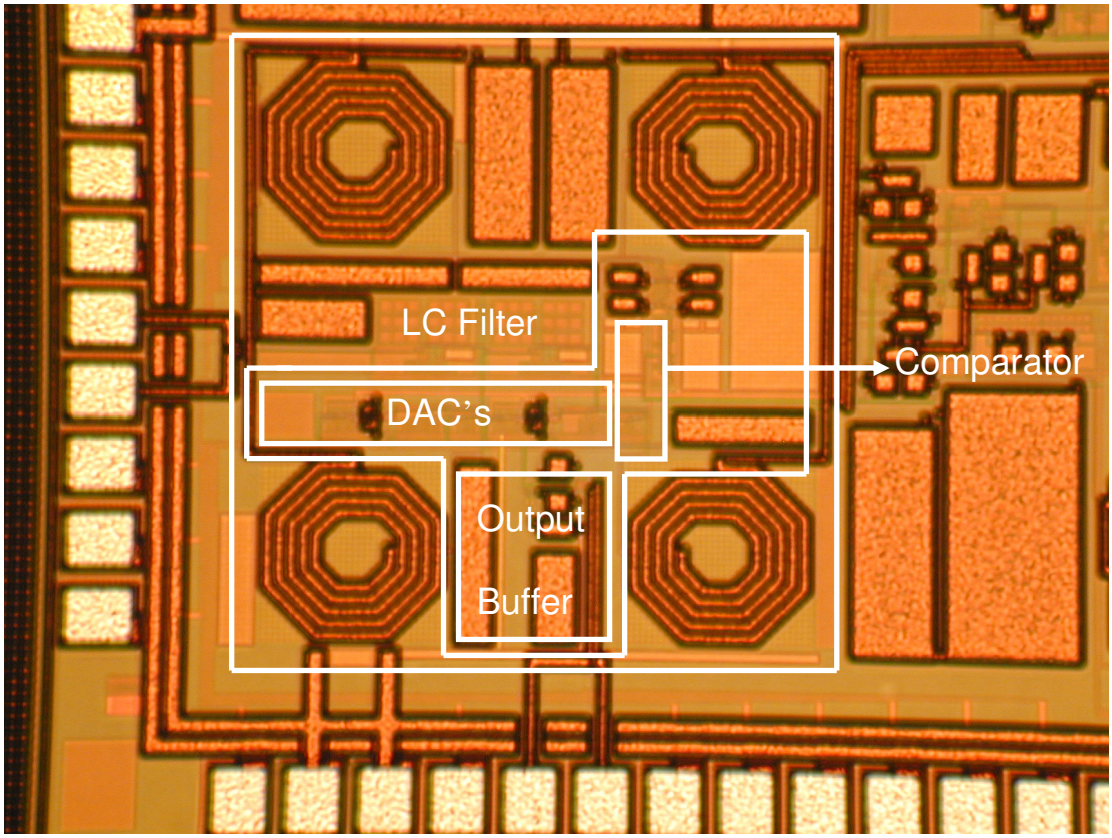


Fig. 4.24. Chip microphotograph of the RF ADC

The core ADC consumes 30 mA from ± 1.25 V and it is designed in IBM 0.25µm SiGe BiCMOS technology (f_T = 47 GHz) through the MOSIS educational program. The QFN64A package available from IPAC is used for this chip, which is a high speed package that can easily process the maximum frequency of 3.8 GHz without significant degradation of the signal. The chip micrograph is shown in Fig. 4.24 and the ADC occupies an area of 1.08 mm^2. The four inductors (each 5.1 nH) used in the two

LC filters occupy the largest percentage of area (around 40 %). The inductors are placed atleast 250 μm from each other in order to minimize any mutual coupling between them. The floor plan of the layout was designed to minimize the interconnect lengths between the various ADC blocks. This is critical, especially for the routing path from the output of the filter through the comparator and DAC's and back to the filter. Any parasitic resistors and capacitors created due to these metal connections increases the excess loop delay and have to be minimized as much as possible. Deep trench wells and protective guard rings are used extensively around every ADC building block to ensure that there is minimal coupling between them. This is especially critical for the comparator block, where the switching operating of the clock introduces noise, which can couple through substrate to other blocks.

The block diagram of the measurement setup is shown in Fig. 4.25. A narrow band balun (EHFFD1618 from Digikey) operating in the frequency range of 880 MHz to 960 GHz (GSM bandwidth) is used to for single-ended to differential conversion of input signals. The single ended clock generator signal is converted to fully differential signal using a narrowband balun (EHFFD1755T from Digikey), which operates in a frequency range of 3.4 to 4 GHz. The differential output bit stream is converted to a single ended signal using the a wideband balun (5315 A from Picosecond labs) which operates in the frequency range of 200 kHz to 17 GHz, which is then injected to the spectrum analyzer. The CT BP ΣΔ ADC bit stream is equivalent to a PWM (pulse width modulated) bit stream and its frequency content is spread over a large bandwidth, which

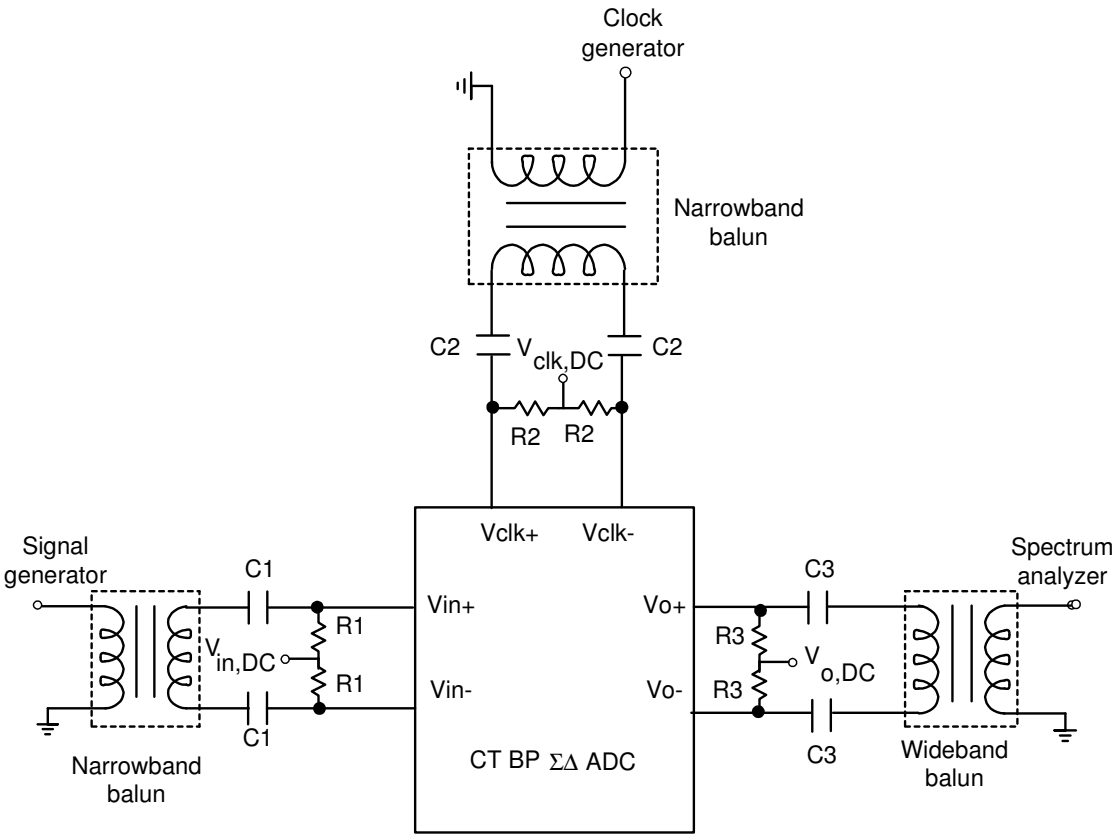


Fig. 4.25. Block diagram of the measurement setup

makes it necessary to use a wideband balun at the output to prevent loss of signal information during the measurement process. The value of the input and output impedance of the three baluns is 50 Ω and the impedances of the connecting blocks are matched for maximum power transfer. The DC voltages for the input, clock and output signals ($V_{in,DC}$, $V_{clk,DC}$ and $V_{o,DC}$) are applied through resistors R1, R2 and R3 respectively. The value of R1 and R2 is 50 Ω in order to match the output impedance of the two narrowband baluns. On-chip termination of 50 Ω is provided for the input and

clock signal paths (50 Ω resistors at the base of input transconductor and clock buffer blocks), which ensures proper coupling of signals into the chip. The value of resistor R3 at the ADC output is 150 Ω (3 times the nominal value is used to increase the signal swing at the output at the cost of increased reflections as an optimal tradeoff). Capacitors C1, C2 and C3 are used to couple the high frequency AC signals (series coupling) and provide DC blocking in the input and output ports. An on-chip output buffer that was described in Section 4.5.5 drives the bit stream into the spectrum analyzer. A printed circuit board (PCB) was fabricated in order to test the ADC and the photo of the measurement setup is shown in Fig. 4.26. The signal swing of the NRZ differential output bit stream at the input of the spectrum analyzer is around ± 100 mV, after the

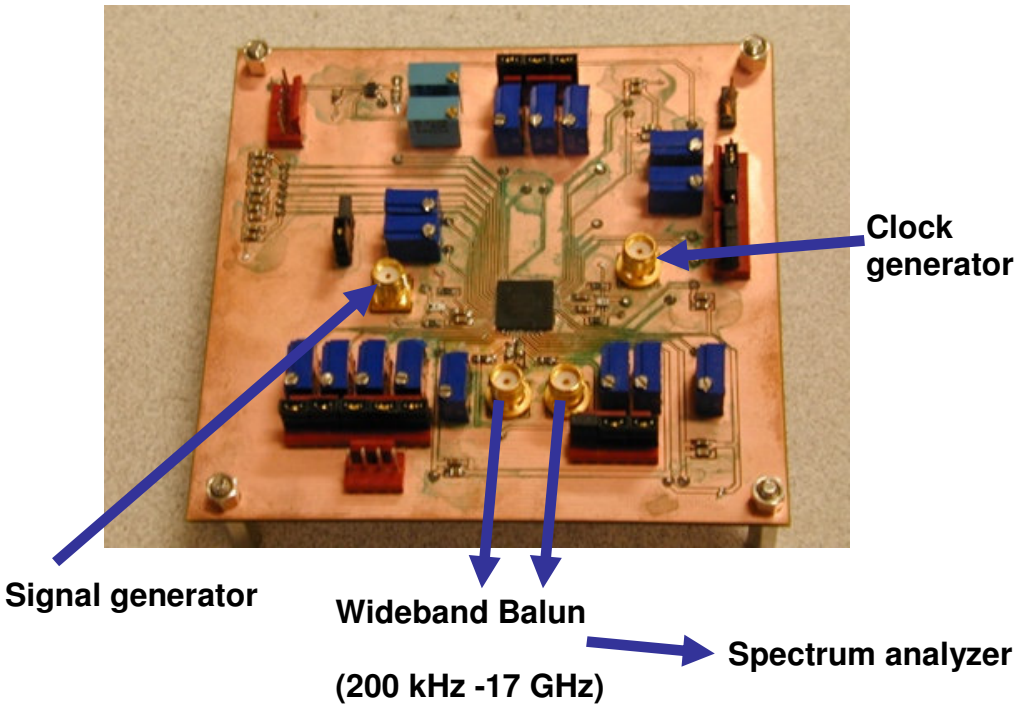


Fig. 4.26. Photo of the measurement setup

losses in the output balun. The value of the output swing scales the absolute value of both the signal and noise power in the spectrum analyzer (while SNR remains constant if the noise of the output balun is not dominant), which is the reason for attenuation of the signal power in the measurement plots.

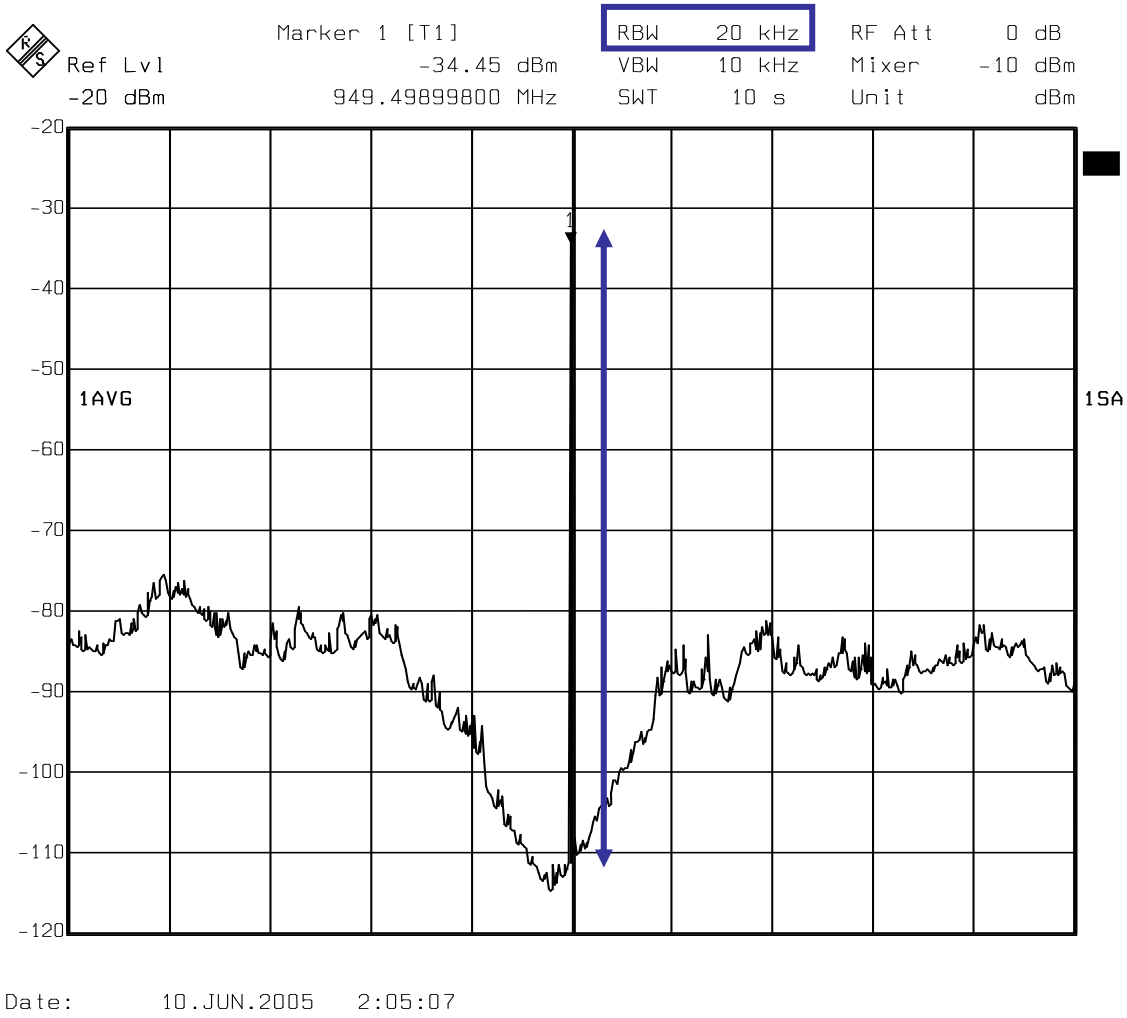


Fig. 4.27. Measured single tone output spectrum of the RF ADC

The single-tone output spectrum of the RF ADC is shown in Fig 4.27. The noise floor of the ADC (including the signal generator and measurement setup noise) integrated in a resolution bandwidth of 20 kHz was measured to be -113 dBm at 950 MHz. The output spectrum of the ADC for two input tones at 949 MHz and 951 MHz, each at -8 dBm, is shown in Fig. 4.28. A passive power combiner with a gain of -6 dB is used to combine the two-tone input signals. The IM3 of the ADC for the two tone input was measured to

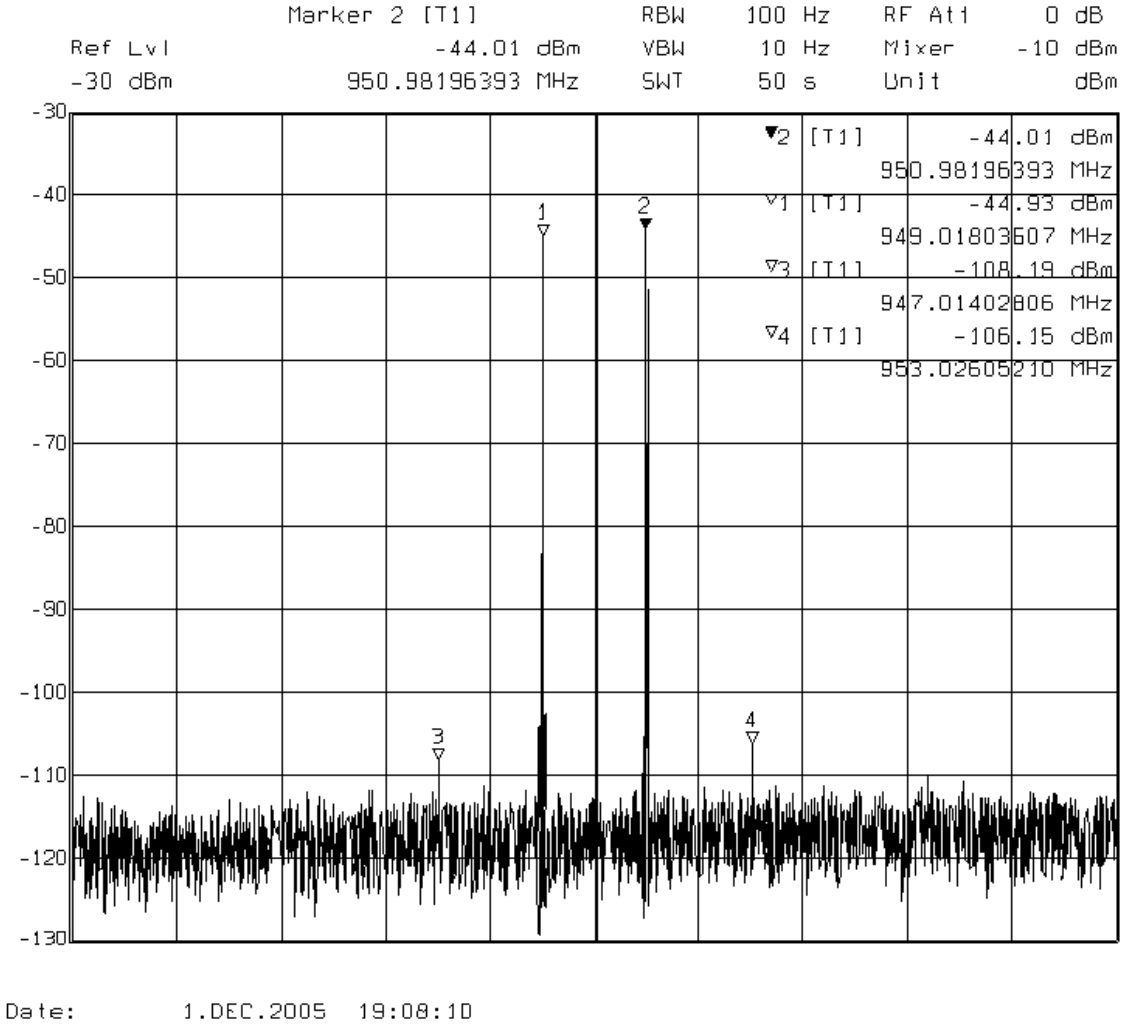


Fig. 4.28. Measured two tone output spectrum of the RF ADC

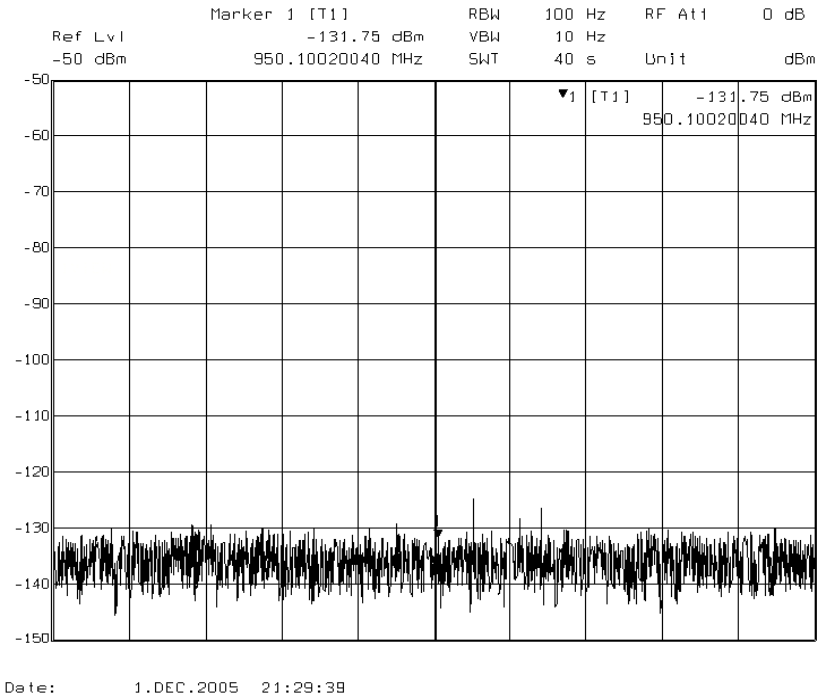


Fig. 4.29. Noise floor of the measurement setup with grounded inputs

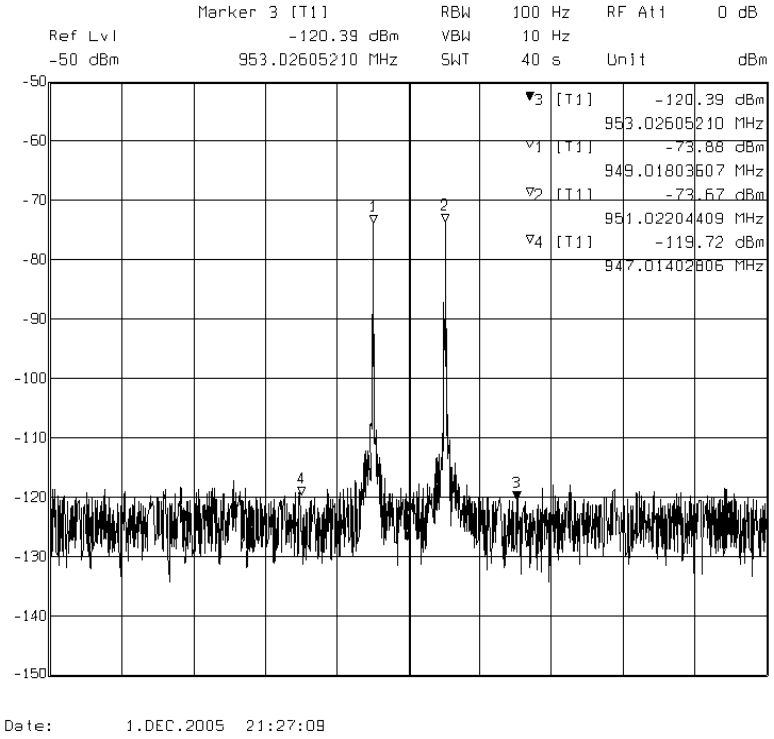


Fig. 4.30. Noise floor of the measurement setup for the two tone input test

be -62 dB; unfortunately the noise level of this characterization increases due to the noise contribution of the two signal generators used. Therefore, the SNR of the ADC is calculated by dividing the signal power of the two-tone test over the integrated noise power with a single tone test, while the distortion components are smaller than the noise level in the required signal bandwidth. The noise floor of the measurement setup with grounded inputs is shown in Fig. 4.29 and the value is around -132 dBm at 950 MHz. This plot includes the noise of the input and output baluns, ADC, output buffer and the PCB. The noise floor of the measurement setup for the two tone test is shown in Fig. 4.30. This plot includes the noise of the two signal generators in addition to the noise sources in Fig. 4.29. The noise floor increases to -121 dBm at 950 MHz due to the noise contribution of the signal generators.

The measured SNR is 63 dB and 59 dB for bandwidths of 200 kHz and 1 MHz respectively, around 950 MHz with a clock frequency of 3.8 GHz. The approach of directly measuring the SNR from the spectrum analyzer captures all noise in the analog domain that are not contributed by the ADC at 950 MHz, which increases the noise floor. Another disadvantage with this approach is that it does not capture the jitter effects properly. The noise from the jitter is added at the input of the comparator and the effect is similar to the quantization noise because it is rejected at the output of the ADC. Since the jitter noise is rejected by the noise shaping effect of the feedback loop, the effect of jitter is not measured accurately by this approach. A better approach would have been to capture the bit stream using a logic analyzer or data acquisition board, but this was not performed due to lack of measurement equipment at GHz clock frequency. The plot of

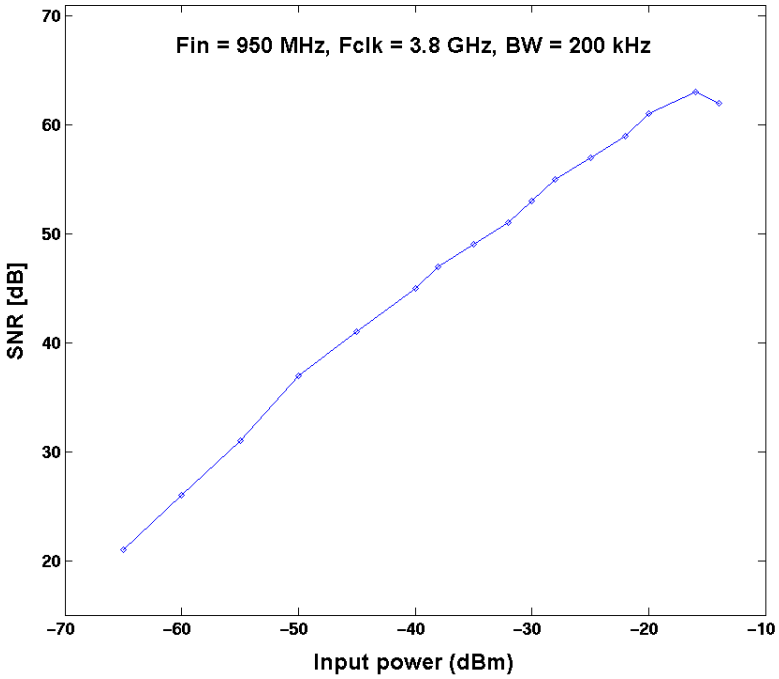


Fig. 4.31. Plot of measured SNR of ADC vs input power for the RF ADC

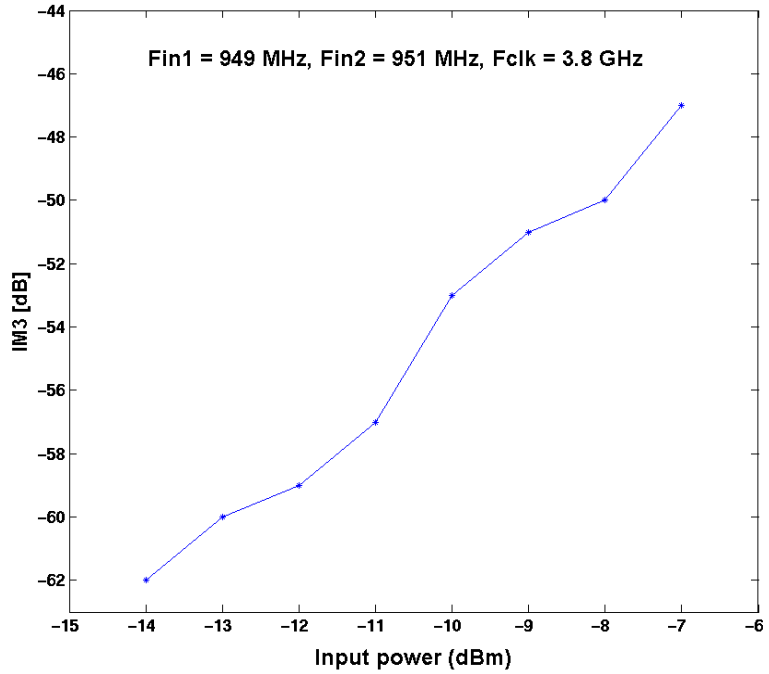


Fig. 4.32. Plot of the measured IM3 vs input power for the RF ADC

output SNR over 200 kHz bandwidth vs input power is shown in Fig. 4.31 and the plot of measured IM3 vs the input power is shown in Fig. 4.32. The performance of the ADC is compared with previous implementations in Table 4.11. The proposed ADC architecture reduces clock jitter problems by using only NRZ DAC's and achieves good SNR performance with significant reduction in power consumption. When compared to Ref [26], this design has similar SNR performance, while the power consumption is further reduced by about two orders of magnitude. The significant reduction in power consumption is due to factors such as supply scaling and power optimization. The power supply is scaled down by a factor of four, which scales the power consumption but it

Table 4.11. Comparison of ADC performance

Parameter	**Ref [28]**	**Ref [26]**	**This work**
Center frequency	1 GHz	1.3 GHz	950 MHz
Sampling frequency	4 GHz	4.3 GHz	3.8 GHz
SNR (BW of 1 MHz)	50 dB	62 dB	59 dB
Power consumption	450 mW	6200 mW	75 mW
Supply voltage	5 V	± 5 V	± 1.25 V
Technology	0. 5 μm SiGe HBT	InP HBT	0.25 μm SiGe BiCMOS
Active area	1.36 mm^2	5.28 mm^2	1.08 mm^2

also results in design challenges due to limited room for signal swing. The power optimization techniques used in this design further improves the power consumption performance as compared to the designs that have been reported in literature. The ADC design in Ref [26] has a 3-bit comparator, while the ADC in this research work has a 1-bit comparator. Despite the difference in the comparator resolution, the current design achieves almost the same resolution as compared to Ref [26] in a 1-MHz bandwidth, while the power consumption is significantly reduced.

The measurement results of the ADC shows that high resolution narrowband A/D conversion is possible at RF frequencies with low power consumption. The performance metrics of the ADC improves the state of the art for data conversion at RF frequencies, but significant challenges still have to be overcome before the ADC can be used in a software radio transceiver. The design challenges and possible future research directions in this area are discussed in Chapter VI.

CHAPTER V

A 500 MHz ADC FOR BANDPASS IF DIGITIZATION AROUND 125 MHz USING DIGITAL TUNING SCHEME

5.1. Introduction

The IF ADC is designed to be used in a software defined radio architecture, as shown in Fig. 5.1. There is no specific standard for the location of the intermediate frequency in all wireless standards and the choice depends on the circuit implementation. A high IF (125 MHz) is chosen in this research work to push the state of art for the IF ADC design in CMOS technology. The bandwidth for the ADC depends on the number of channels and the type of wireless standard. The IF ADC is designed for the GSM

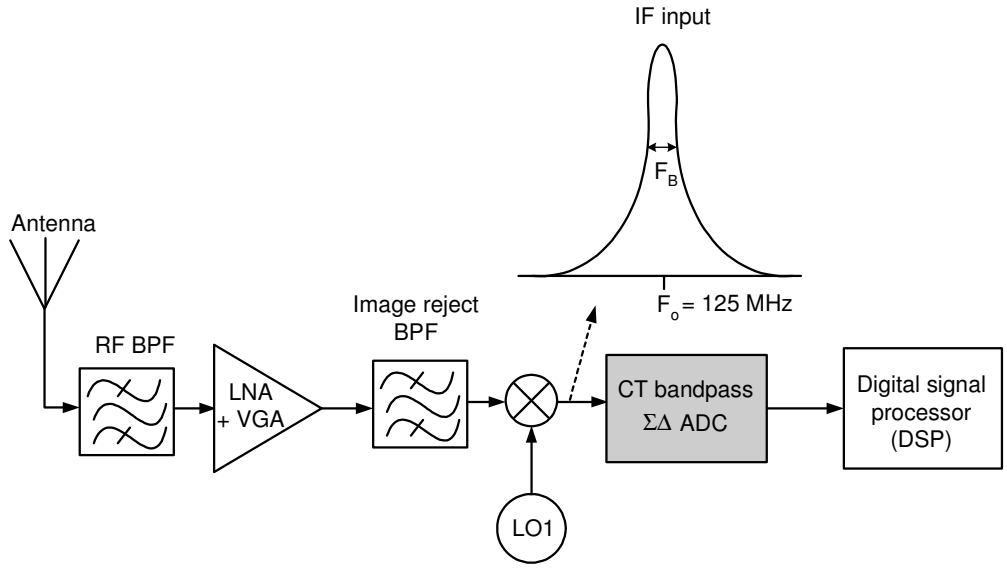


Fig. 5.1. Target application for the IF ADC design

standard (channel bandwidth of 200 kHz) and five channels are considered, which results in a 1 MHz ADC bandwidth.

There are no specifications for the location of intermediate frequency in a radio receiver, which has resulted in adoption of different IF frequency locations for the receiver implementation for the same wireless standard. The IF can usually vary from 5 MHz to 200 MHz, frequencies lower than 5 MHz are not preferred due to flicker noise problems whereas frequencies higher than 200 MHz tend to increase the power consumption for the IF circuits. The bandpass ADC's that have been reported in literature at intermediate frequencies (10 MHz – 40 MHz) are implemented using switched capacitor circuits, which are not suitable when higher values of IF are used in the receiver, as discussed in Section 2.2.3. The continuous time implementation is more suited for high IF receivers with low power consumption. The three types of possible continuous time filter implementations are LC, active RC and g_m-C filters. Integrated implementation of LC filters is not possible for this frequency range as large values of inductor and capacitor is required, which comes with huge area penalty. The active RC filter implementation requires high DC gain amplifiers with GBW in the GHz range, which comes with the penalty of large power consumption. The g_m-C filter is the best choice for low power implementation at the required IF frequency

The literature review of bandpass ADC's in Table 2.2 showed that high performance at IF frequencies required technologies like gallium arsenide (GaAs), indium phosphide (InP) and silicon germanium (SiGe) with large power consumption. The trend in wireless receiver design is to integrate the analog and digital signal

processing stages in CMOS technologies, which would results in significant reduction in overall area and power consumption. However, CT BP ΣΔ ADC implementations are not common in CMOS technologies above 50 MHz IF because of demanding specifications on the ADC building blocks, especially a linearized transconductance block. To the author's knowledge, only two instances of high IF CT BP ΣΔ ADC designed in CMOS technology have been reported in literature and their performance summary is shown in Table 5.1.

Table 5.1. Performance summary of high IF bandpass ADC's in CMOS technology

Parameter	**Ref [52]**	**Ref [53]**
Type	2^{nd} order CT BP ΣΔ	4^{th} order CT BP ΣΔ
Loop filter	Gm-C	SAW (surface acoustic wave)
Center frequency	70 MHz	47.3 MHz
Clock frequency	280 MHz	189.2 MHz
Bandwidth	200 kHz	200 kHz
SNDR	42 dB	54 dB
Power	39 mW	30 mW
Technology	0.5 μm CMOS	0.35 μm CMOS
Supply voltage	2.5 V	3.3 V

The main bottleneck in the implementation of CT BP ΣΔ ADC using g_m-C filters is the requirement of a highly linear transconductance stage, which is difficult to

implement at high IF with the constraint of low power consumption. The linearity of the OTA in the first stage is very important since its distortion components appear directly at the output without any noise shaping. The distortion components of the subsequent OTA stages are filtered by the loop and they have less stringent linearity requirements. The approach that has been adopted in continuous time low pass ΣΔ ADC designs is to use an active-RC filter only in the first stage for linearity enhancement and then use g_m-C filter in subsequent stages for low power consumption. This approach is not practical for high IF CT BP ΣΔ ADC as the active-RC stage requires a high gain amplifier with gain-bandwidth product in the GHz range, which results in huge power consumption. The center frequency and the quality factor of the continuous time loop filter in the ADC changes due to process, temperature and supply voltage (PVT) variations, which reduces the SNR at the output of the ADC. An automatic tuning loop is required to fix the center frequency and Q of the filter over PVT variations.

The main design specifications for the IF ADC are shown in Table 5.2. The center frequency of the ADC is 125 MHz and it uses a Fs/4 architecture (Fs is the sampling frequency), which results in a clock frequency of 500 MHz. The first objective of this design is to develop a very linear transconductor for the gm-C bandpass filter implementation with a center frequency of 125 MHz. The second objective of this design is to propose a system level digital tuning loop to automatically tune the filter's center frequency, Q and other loop parameters in order to obtain the best SNR performance for the ADC. The digital tuning approach offers several advantages over

other conventional approaches in the analog domain and can be easily integrated in standard CMOS technologies.

Table 5.2. Specifications for the IF ADC

Parameter	Value
Center frequency (f_o)	125 MHz
Clock frequency	500 MHz ($4*F_o$)
Target SNR	> 60 dB
Bandwidth	200 kHz / 1 MHz
Technology	TSMC 0.35 μm CMOS
Power consumption	< 150 mW
Power supply	± 1.65 V

The g_m-C bandpass filter can be derived from a LC bandpass filter by replacing the inductor with a gyrator, which emulates the action of inductive impedance for any input current or voltage. The implementation of a gyrator element using transconductor blocks (g_m) and capacitor is shown in Fig. 5.2. The value of the effective inductor is given by

$$L_{eff} = \frac{C}{g_m^2} \tag{5.1}$$

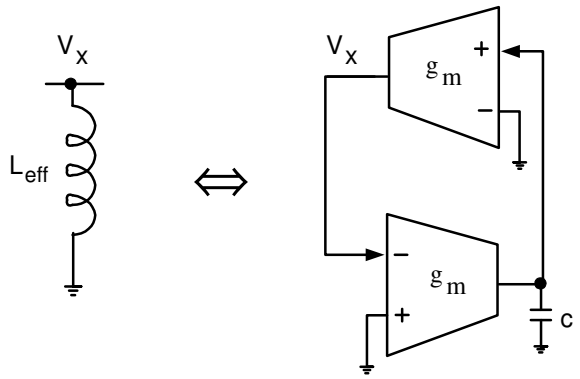


Fig. 5.2. Implementation of a gyrator

The implementation of a second order g_m-C bandpass filter using the gyrator block is shown in Fig. 5.3. Assuming ideal transconductance blocks (infinite output resistance and DC gain), the transfer function of the second order bandpass filter based on an active resonator in Fig.5.3 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{\left(\frac{g_{m1}s}{C_1}\right)}{s^2 + \left(\frac{g_{m2}^2}{C_1C_2}\right)} \tag{5.2}$$

The center frequency of the second order filter (ω_o) is given by

$$\omega_o = \frac{g_{m2}}{\sqrt{C_1C_2}} \tag{5.3}$$

where C_1 and C_2 represent the effective capacitance at the output and intermediate nodes (shown in Fig 5.3). The quality factor of the transfer function given by (5.2) is infinite, which reduces when the finite output resistance of the transconductor blocks is taken

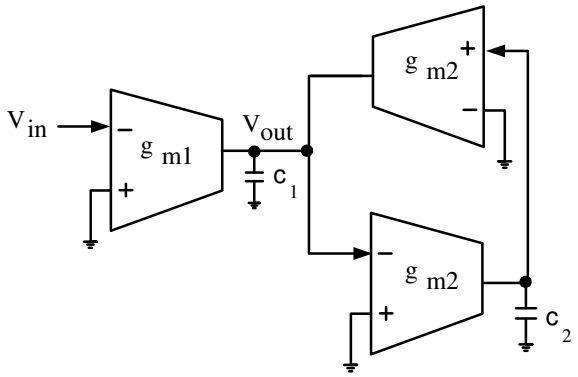


Fig. 5.3. Implementation of an ideal second order g_m-C resonator

into account. Assuming that each transconductor block in Fig. 5.3 has the same finite output conductance (g_o), (5.2) changes to

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}(sC_2 + g_o)}{s^2C_1C_2 + s(2C_1 + C_2)g_o + (2g_o^2 + g_{m2}^2)} \tag{5.4}$$

The center frequency of the filter, initially given by (5.3), changes to

$$\omega_o = \sqrt{\frac{2g_o^2 + g_{m2}^2}{C_1C_2}} \tag{5.5}$$

The quality factor of the filter, which was infinite in (5.2), is given by

$$Q = \frac{\sqrt{C_1C_2(2g_o^2 + g_{m2}^2)}}{g_o(2C_1 + C_2)} \tag{5.6}$$

The finite output impedance of the OTA modifies both the center frequency and Q of the filter. A higher order filter can be obtained by the cascade of the second order resonator blocks.

This design was a joint research work by the author and his colleague. The author was responsible for the design of the ADC architecture, digital tuning scheme and the circuit implementation of the comparator. The details of the architecture for the IF ADC design are described in the next section.

5.2. Architecture of the IF ADC

The choice of the ΣΔ ADC architecture depends on tradeoff between maximum signal to noise ratio (SNR) that can be obtained with limited signal swing at all internal nodes (related to stability). The main architectural level choices for the ADC that affects its performance include the following

i) Order of the ADC (order of the loop filter)

ii) Single-loop or MASH (multi-stage noise shaping)

iii) Single-bit or multi-bit (number of comparator bits)

The tradeoffs in performance between these parameters were discussed in detail in Chapter III. A fourth order, single-loop and single-bit architecture is chosen for the CT BP ΣΔ ADC implementation, which results in an optimum tradeoff between signal swing and SNR. A higher order loop filter increases the SNR, but it could suffer from potential stability problems as large signal swing may saturate the internal nodes. A single-loop and single-bit architecture is chosen over the multi-stage and multi-bit architecture as the former leads to simpler implementation, thereby resulting in lower power consumption as compared to the latter choices.

The first step in the design is to identify the transfer function of a switched capacitor BP ΣΔ ADC which has the desirable loop transfer function with the required SNR and good stability performance. The next step is to perform the impulse invariant transformation which transforms the z-domain (discrete-time) to s-domain (continuous time) transfer function, which is described in Section 3.2. The transformation ensures that the properties of both the structures are the same in terms of performance. A fourth order switched capacitor bandpass filter can be obtained from a low pass prototype by performing the substitution $z^{-1} \rightarrow -z^{-2}$, which transform a n^{th} order low pass filter to bandpass filter of order 2n. The transfer function of the bandpass loop filter obtained from the low pass filter is given by (4.2). A full clock cycle delay (z^{-1}) is used after the comparator, which gives more time for the comparator output to settle, thereby alleviating any problems with metastability. This z^{-1} delay is taken into account while the transfer function is calculated and the modified z-domain loop filter transfer function that is used in the design is given by (4.3). The choice of the DAC pulse shape affects the ADC performance, as discussed in Section 3.3. A Non Return to Zero (NRZ) DAC pulse shape is used for the IF ADC which reduces problems associated with clock jitter. The s-domain transfer function of the NRZ DAC (given in Fig. 3.4) and the z-domain loop filter transfer function given by (4.3) are used in the impulse invariant transform of (3.3) to find the open loop transfer function of the ADC. The open loop s-domain transfer function of the ADC calculated using the previous step is given by (4.4).

The block diagram of the CT BP ΣΔ ADC architecture for IF digitization is shown in Fig. 5.4. The loop filter in the forward path is a fourth order g_m-C bandpass

filter (cascade of two second order g_m-C resonators, the basic second order resonator is shown in Fig. 5.3). The comparator z^{-1} with delay samples the filter output and quantizes the sampled value to a single-bit output. The digital bit stream (voltage mode)

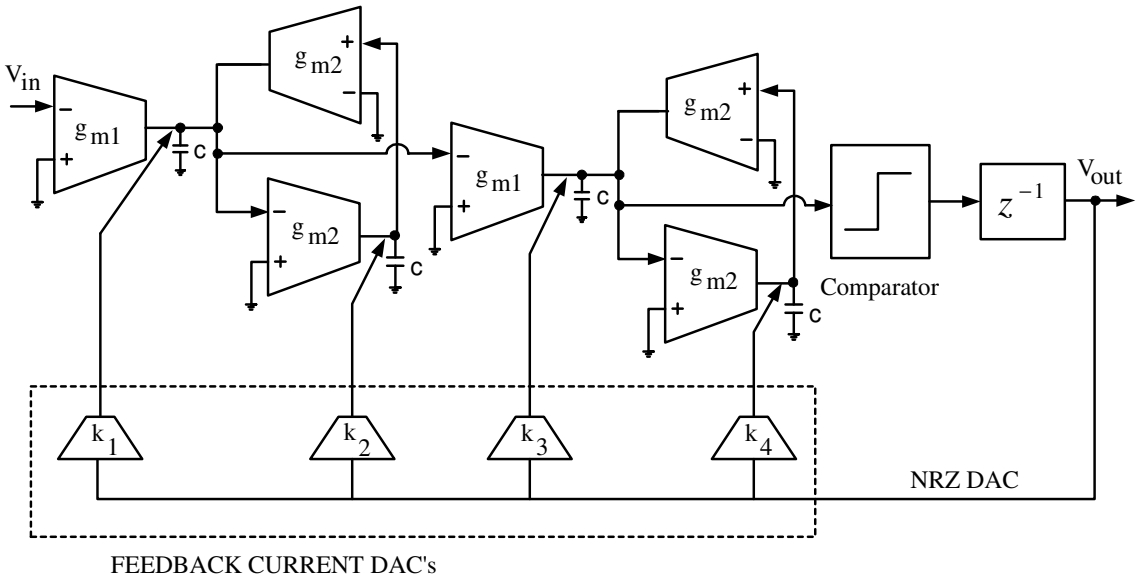


Fig. 5.4. Block diagram of the IF ADC architecture

is converted into current by the four current DAC's (k_1 – k_4) and injected back into the filter to complete the negative feedback loop. Assuming that the transconductance blocks (g_{m1}, g_{m2}) are ideal, the open loop transfer function from the ADC output (V_{out}) to the comparator input (calculated by opening the loop) is given by

$$H_{loop}(s) = \frac{s^3 A k_3 + s^2 (A^2 g_{m1} k_1 + A \omega_o k_4) + s(A^2 \omega_o g_{m1} k_2 + A \omega_o^2 k_3) + A \omega_o^3 k_4}{(s^2 + \omega_o^2)^2} \qquad (5.7)$$

$$A = \frac{1}{C}; \omega_o = \frac{g_{m2}}{C} \tag{5.8}$$

The transconductance of the input OTA (V-I converter at the filter input) does not affect the loop transfer function, but affects the dynamic range at the input of the ADC. This architecture provides individual control for tuning each of the terms in the numerator of (5.7). The s^3 and constant terms in numerator of (5.7) are controlled by coefficients k_3 and k_4, respectively. Once these two coefficients are fixed, the s^2 and s terms are controlled by coefficients k_1 and k_2, respectively. The noise transfer function (NTF) of the ADC assuming a linearized quantizer model is given by

$$NTF(s) = \frac{V_{out}}{Q_n} = \frac{1}{1 + H_{loop}(s)} \tag{5.9}$$

where Q_n is the quantization noise (assumed to be dominant and injected at the comparator input) and $H_{loop}(s)$ is given by (5.7). The shape of the NTF can be controlled precisely by tuning each of the numerator terms in the open loop transfer function, which results in the minimum possible integrated noise power over the entire bandwidth and good SNR. The transconductance value used in the filter (g_{m1}, g_{m2}) is chosen as an optimum tradeoff between linearity, noise, signal swing and power consumption considerations. The loop coefficients k_1, k_2, k_3 and k_4 can be calculated by equating each coefficients of the numerator in (4.4) and (5.7) respectively.

Simulink and Matlab software simulation tools were used for the behavioral simulation of the IF ADC. The Simulink behavioral model of the fourth order g_m-C bandpass IF ADC architecture is shown in Fig 5.5. The model uses sub-blocks available

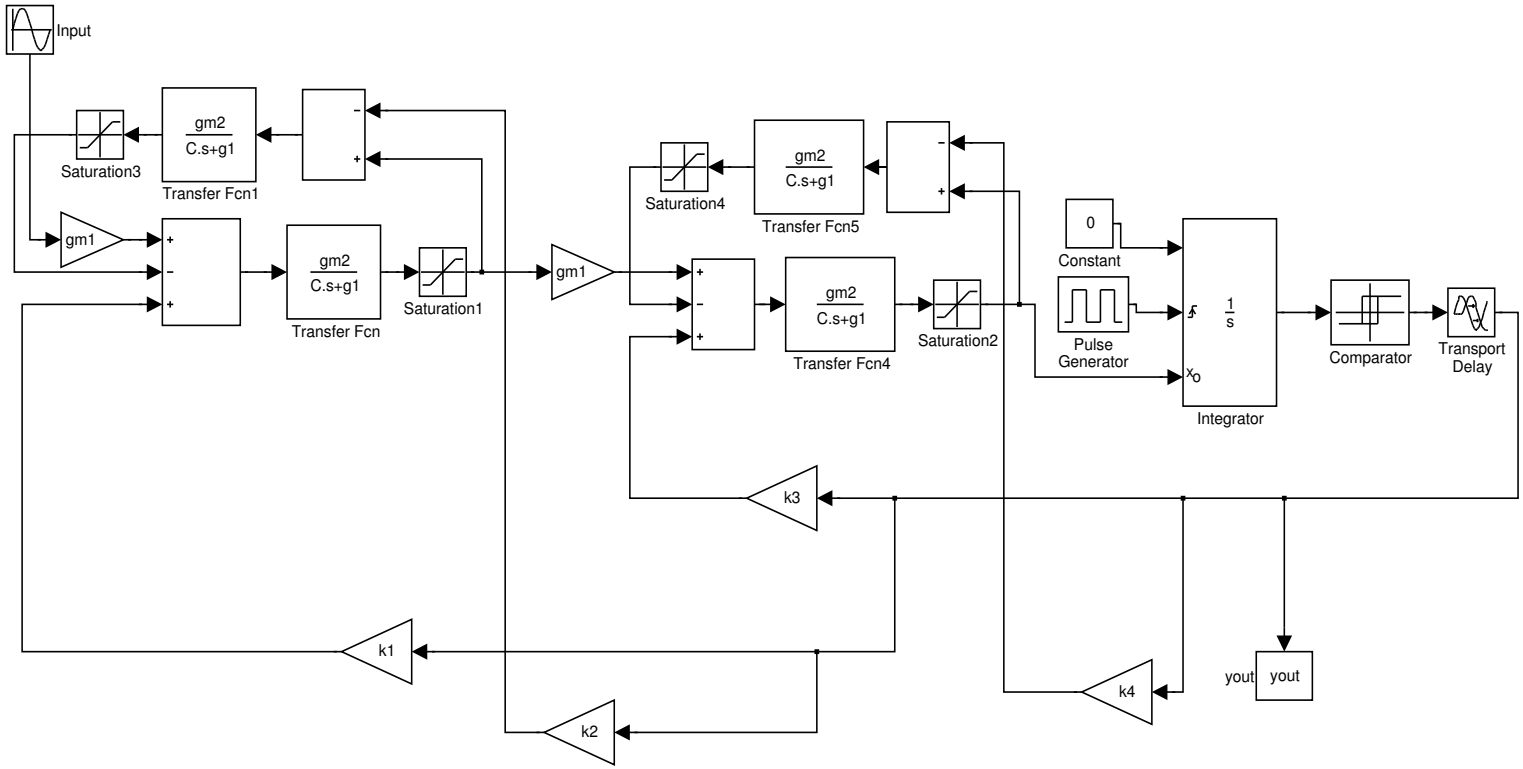


Fig. 5.5. Simulink behavioral model of the IF ADC architecture

from Simulink library to obtain the required loop transfer function. The s-domain (continuous time) transfer function block is used to realize the integrator blocks (1/s). The integrator blocks have finite DC gain, which is represented by the term g1 in the denominator of the integrator transfer function. The current DAC blocks (k_1, k_2, k_3 and k_4) are implemented using a simple multiplier block with the required coefficient to convert the digital bit into current. The saturation block is used at the output of the integrator blocks in order to limit the signal swing within the supply voltages (Vdd/Vss). The saturation block is not required for the current DAC as its output is a digital current pulse stream that follows the bit stream input. The implementation of the comparator block is similar to the approach shown in Fig. 4.11 and described in section 4.4. The z^{-1} delay (one clock period) is implemented using the transport delay block and the single bit quantizer is implemented using the relay block. The loop coefficients and the transconductance of each stage are scaled down for low power consumption while

Table 5.3. Values of optimized loop coefficients for the IF ADC

Coefficient	**Value**
k_1	0.3183
k_2	0.3183
k_3	0.8408
k_4	0.75

maintaining the required signal swing and dynamic range. The final values of the optimized loop coefficients that are used in the IF ADC are shown in Table 5.3. The power spectrum of the single bit output of the IF ADC is shown in Fig. 5.6. The input signal is a sine wave at 125 MHz and the sampling clock frequency is 500 MHz. The measured SNR at the output of the ADC was 85 dB in a bandwidth of 1 MHz. The SNR was calculated for 65536 samples and the simulation used finite DC gain of 40 dB for each of the g_m-C integrator blocks in Fig. 5.5. A step size of 0.05*Ts seconds (Ts is the time period of the clock) is used for the model, which ensures very good accuracy of the

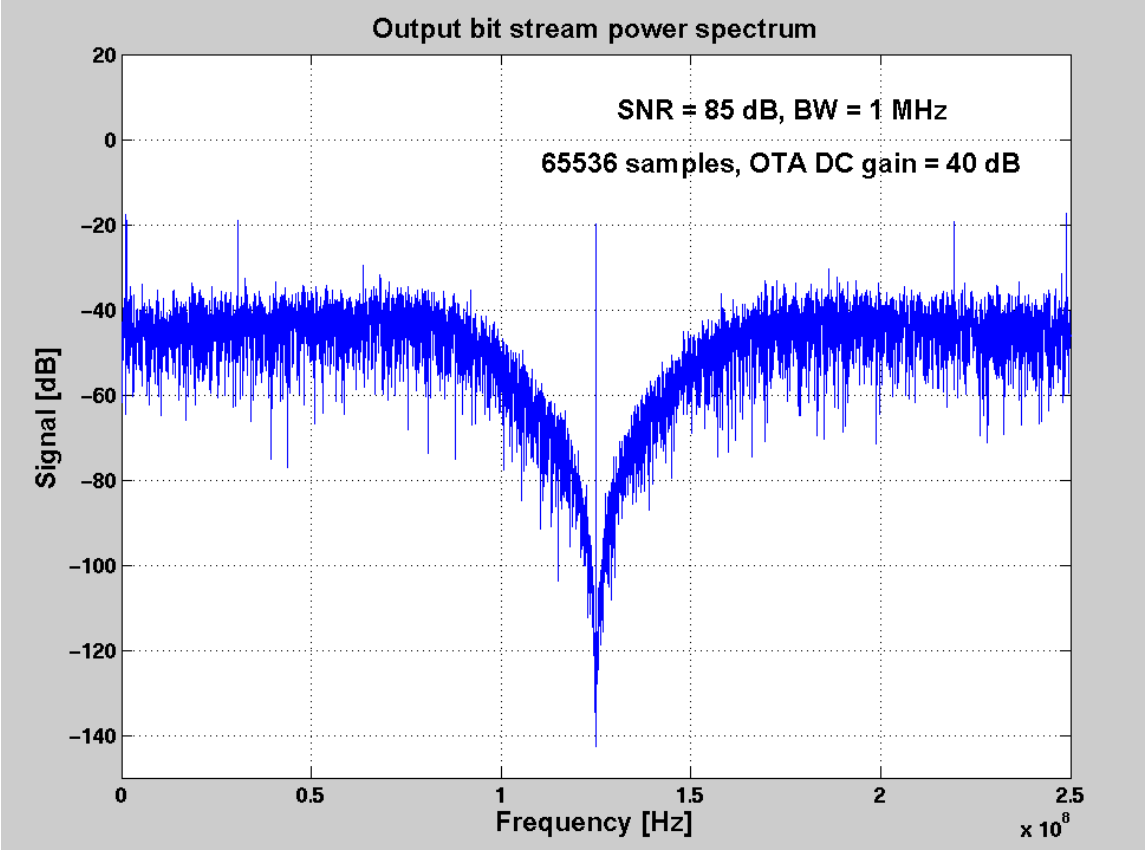


Fig. 5.6. Output spectrum of the IF ADC – behavioral simulations

behavioral simulations. The simulation parameters that are used for the Simulink model are similar to the ones described in Section 4.4.

5.3. Digital tuning loop for SNR optimization

The SNR of the CT BP ΣΔ ADC is calculated by dividing the signal power over the noise power in the required signal bandwidth and is given by

$$SNR_{ADC} = \frac{\int_{f_o-\frac{f_b}{2}}^{f_o+\frac{f_b}{2}} STF(f)}{\int_{f_o-\frac{f_b}{2}}^{f_o+\frac{f_b}{2}} NTF(f)} \tag{5.10}$$

where STF and NTF are the signal and noise transfer functions, f_o is the center frequency and f_b is the signal bandwidth. The power of STF is usually a constant value over the signal bandwidth and the SNR depends on the integrated noise power in the bandwidth. The ideal NTF of the ADC can be derived from (5.9) and is given by

$$NTF(s) = \frac{(s^2+\omega_o^2)^2}{(s^2+\omega_o^2)^2 + H_{num}(s)} \tag{5.11}$$

where $H_{num}(s)$ is the numerator of (5.7) and ω_o is given by (5.8). The magnitude of the ideal NTF at $s=j\omega_o$ is 0 (negative infinity in log scale), which leads to the best SNR performance. The effect of finite Q of the filter on the ADC performance was discussed in Section 3.4.4 and it increases the noise floor, which results in SNR degradation. The

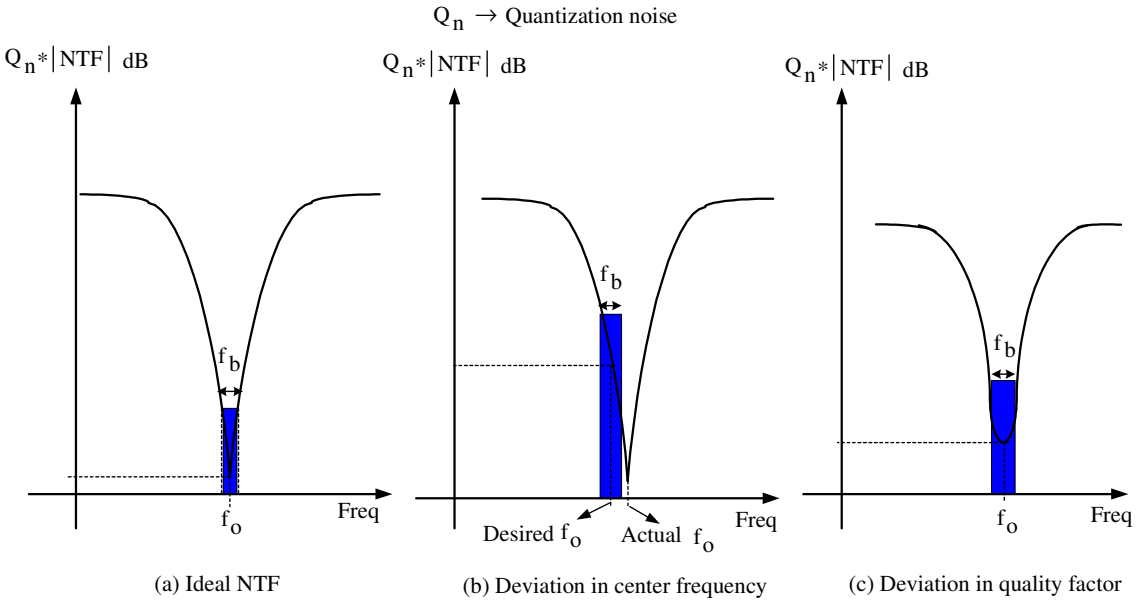


Fig. 5.7. Effect of deviations in center frequency and Q of filter on the NTF

effect of deviation in center frequency and Q of the filter on the integrated noise power is shown in Fig. 5.7, where the shaded area represents the noise power in the signal bandwidth. Fig. 5.7 (a) shows the ideal NTF (very high Q and accurate center frequency (f_o)), the noise power at f_o is very low and integrated noise power is at a minimum value. Fig. 5.7 (b) shows the NTF for high Q and a deviation in f_o, both the noise power at f_o and the integrated noise power in the signal bandwidth increases, which degrades the SNR. Fig. 5.7 (c) shows the NTF for correct f_o and a lower Q value, both the noise power at f_o and the integrated noise power in the signal bandwidth increases for this case too, resulting in lower SNR. The shape of NTF given by (5.11) also depends on the loop coefficients (k_1, k_2, k_3 and k_4); due to the presence of $H_{num}(s)$ in the denominator, and these coefficients can change the integrated noise power. Thus, the center frequency and

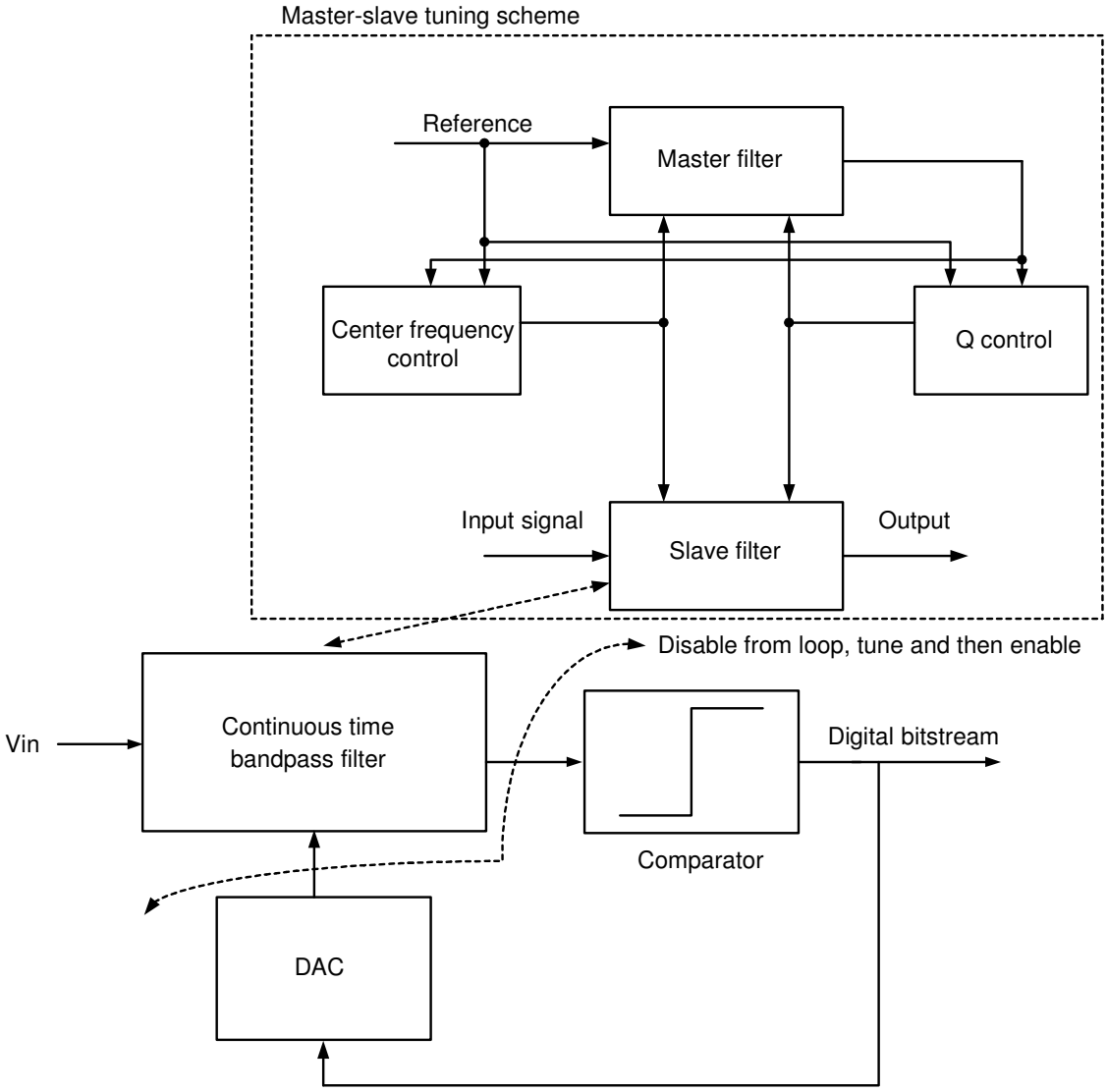


Fig. 5.8. Conventional tuning scheme of a CT BP ΣΔ ADC

Q of filter, together with the DAC coefficients have to be maintained at the desired value over PVT variations in order to obtain the best SNR performance.

The center frequency and Q of a g_m-C filter, given by (5.5) and (5.6), depends on the value of capacitor and OTA parameters (transconductance and output resistance). The center frequency and Q of the gm-C filter typically changes by ± 25% over PVT

variations and a tuning scheme is usually required to compensate for these variations. A comprehensive overview of typical automatic tuning schemes for obtaining the desired center frequency and Q of continuous time filters are presented in [54] and [55]. The most common approach to tune a CT BP ΣΔ ADC is shown in Fig. 5.8. The continuous time bandpass filter in the forward path is disabled from the feedback loop. The center frequency and Q of the standalone filter is set using typical tuning schemes (such as master-slave filter tuning scheme, refer to [54], [55] for more details) and the tuned filter is then enabled in the feedback loop. The main problem with this approach is that this does not guarantee the best SNR performance for the ADC because it does not compensate for any non-idealities in the feedback path (comparator and DAC blocks). The center frequency and Q of the NTF (which determines the SNR) may change from the required value, though the filter in the forward path has been tuned, due to other non-idealities like excess loop delay in comparator, incorrect DAC coefficients etc. A direct background digital tuning scheme was proposed in [56] and [57] to automatically tune the center frequency and Q of a CT BP ΣΔ ADC. The scheme was based on the spectral estimation of the digital output in background during the operation of the ADC. The main problem with such an approach is that it becomes difficult to correctly estimate the noise floor (power of NTF) and its frequency location when a strong signal component is present in its vicinity.

The block diagram of the proposed digital system level tuning scheme for the CT BP ΣΔ ADC is shown in Fig. 5.9. The output digital bit stream from the ADC is captured off chip using a data acquisition board. The captured bit stream is processed by

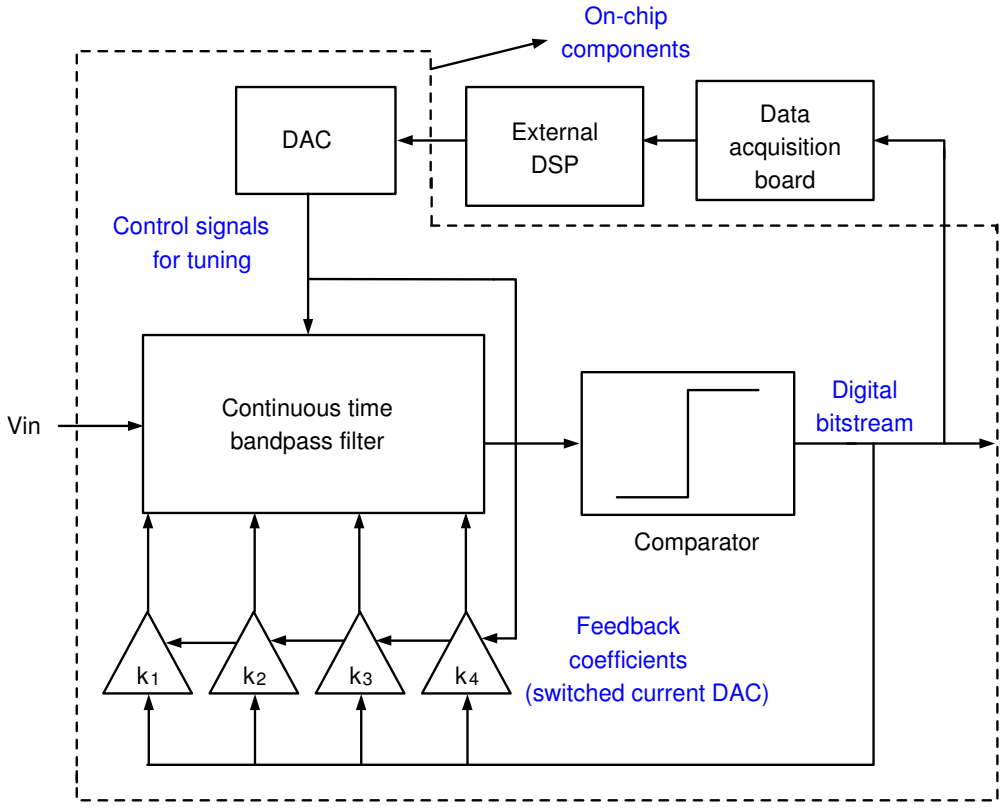


Fig. 5.9. Block diagram of the proposed digital tuning scheme

an external digital signal processor (DSP), where the center frequency and Q of the CT BP ΣΔ ADC is estimated using digital signal processing techniques. The difference between the estimated and required values of center frequency and Q of the ADC is calculated in order to generate the digital tuning control signal. The digital control word is converted into an analog signal using an on-chip DAC, which is used to tune the filter and the DAC currents for obtaining the best SNR performance of the ADC. This automatic digital tuning scheme uses a system level approach because of the fact that the filter, comparator and DAC non-idealities are taken into account when the output bit stream is used for estimation of the power spectrum. The data acquisition and DSP

functions are performed off-chip for ease of implementation for this proof of concept design, but these functionalities can be easily integrated in a CMOS implementation.

The system level implementation of the proposed digital tuning scheme is shown in Fig. 5.10. The input test tone at the required center frequency f_o is applied at the input of the comparator. The measured output spectrum directly gives the NTF of the ADC. The strength of the test tone can be very small and should be sufficient just to activate the loop. The Discrete Fourier transform (DFT) of a bit stream (x[n]) of length N is given by

$$X(\mathrm{k}) = \sum_{\mathrm{n=0}}^{\mathrm{N-1}} \mathrm{x[n]} e^{\frac{j2\pi nk}{N}}, k = 0...N-1 \tag{5.12}$$

The DFT can be implemented using the Fast Fourier transform (FFT) in a computer when N is a power of two. The periodogram, P(k), of the input bit stream of length N is used to estimate the power spectrum [58] and it is given by

$$\begin{aligned} P(0) &= \frac{1}{N^2}\left|X(0)\right|^2 \\ P(k) &= \frac{1}{N^2}\left[\left|X(k)\right|^2 + \left|X(N-k)\right|^2\right], k = 1...\left(\frac{N}{2}-1\right) \\ P\left(\frac{k}{2}\right) &= \frac{1}{N^2}\left|X\left(\frac{N}{2}\right)\right|^2 \end{aligned} \tag{5.13}$$

where X(k) is given by (5.12). The power spectrum given by the periodogram is defined at (N/2)+1 uniformly spaced frequency points between 0 and the Nyquist rate (F_s/2), which implies that the width of the frequency bins are (F_s/N). The estimated power

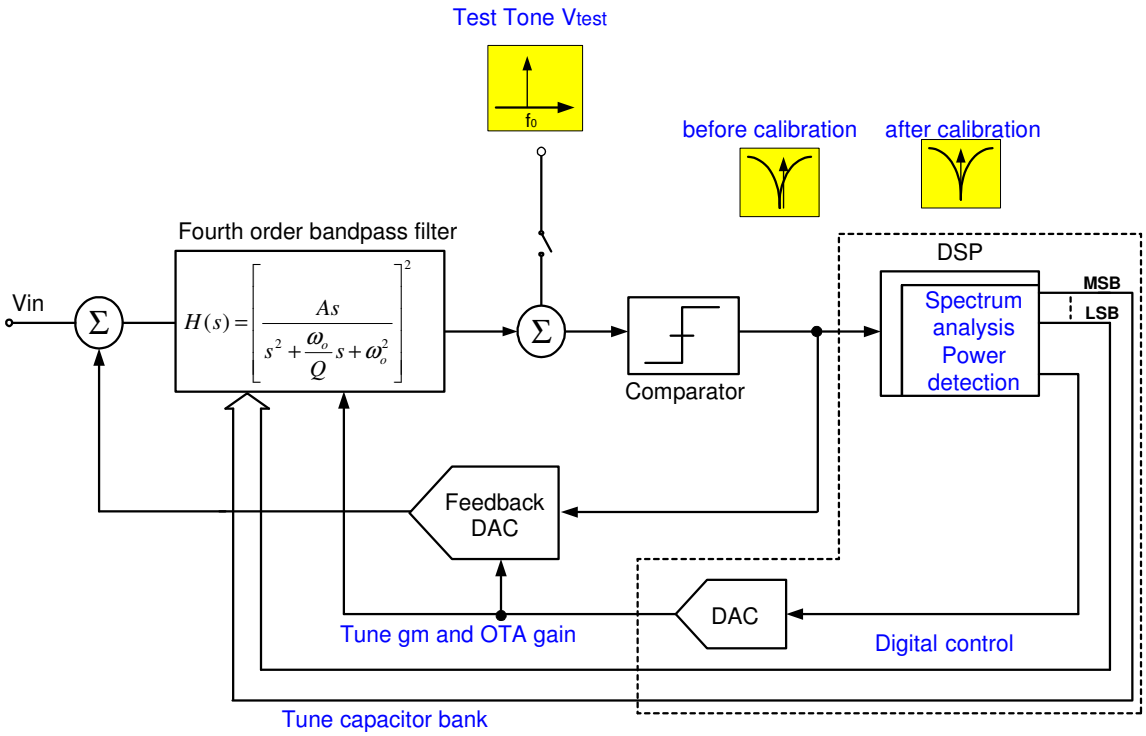


Fig. 5.10. System level implementation of the proposed digital tuning scheme

spectrum is used to determine the deviation from the required values and digital control signals are generated to tune the ADC. The coarse tuning of filter's center frequency is achieved by control of a capacitor bank using switches. The value of OTA's transconductance is changed for the fine tuning of the center frequency. The OTA gain is changed to vary the Q of the filter and the feedback DAC's are tuned by modifying their current values. The digital control signals are updated such that the tuning scheme converges to a final value, which is ensured by using the adaptive LMS (Least mean square) algorithm. The LMS algorithm tries to minimize the mean square error (MSE), which is given by

$$MSE = \frac{1}{2}\left(d(t) - y(t)\right)^2 \tag{5.14}$$

where d(t) is the desired response and y(t) is the actual response of the system in time domain. The rate of change of the tuning signal (W_i) during the i^{th} iteration determined by the LMS algorithm is given by

$$\frac{dW_i}{dt} = \mu\left[d(t) - y(t)\right]g_i(t) \tag{5.15}$$

where μ is the step size and $g_i(t)$ is the gradient of the tuning signal in time domain. The algorithm for the digital tuning scheme is given by the following steps :

i) Inject a test tone signal fo (required center frequency) at the comparator input.

ii) Compute the power spectrum of the captured output bit stream using (5.13), which gives the power in (N/2)+1 frequency bins. Increase "N" for a finer frequency resolution, at a cost of longer computation time.

iii) Find the j^{th} frequency bin which has the lowest power of all the frequency bins. This gives the estimate for the location of center frequency of the ADC's NTF. If needed, repeat (ii) in order to get an average value of estimated center frequency. This helps in averaging out any errors during the estimation process.

iv) The digital control tuning signal is calculated using (5.15) based on the difference between estimated and required center frequency. The step size μ is chosen such that the automatic tuning scheme converges within a required

time frame. Iterate (ii) – (iv) till the center frequency is tuned to the desired value

v) Calculate the power spectrum using (5.13) and find the lowest power value (P_{low}) of all frequency bins. Find the two frequency bins to the either side of the center frequency which has the power value (P_{low} + 3 dB), and their difference which gives the 3-dB bandwidth (f_{3dB}). The Q is estimated to be (f_o/ f_{3dB}). If needed, repeat (v) to get average estimate of Q.

vi) The digital control tuning signal is calculated using (5.15) based on the difference between estimated and required Q values. The step size μ is chosen such that the automatic tuning scheme converges within a required time frame. Iterate (v) – (vi) till the Q is tuned to the desired value

vii) The DAC current coefficients are fine tuned to reduce the noise power at the center frequency using the power estimation and correction steps, similar to the above two cases. This fine tuning should not change the center frequency and Q of the NTF that was already tune din steps (i) – (vi).

The convergence time for the tuning scheme depends on the value of N (number of output samples), step size (μ) and the speed of the DSP. The main disadvantage is that this is an offline tuning scheme and the ADC cannot be used while the tuning scheme is activated. The offline nature of the tuning scheme necessitates the tuning scheme convergence time to be minimized as much as possible.

5.4. Circuit implementation and simulation results

The circuit implementation and simulation results of the main building blocks of the ADC are discussed in this section. As mentioned earlier, the author was responsible only for the circuit implementation of the comparator. The other building blocks are described briefly and more details of the circuit implementation can be found in [59].

5.4.1. gm-C bandpass filter using linearized OTA

The fourth order bandpass filter in the forward path is implemented using a gm-C filter, as shown in Fig. 5.4. The main requirement for implementing the bandpass filter is a very linear OTA stage with high DC gain which operates properly at 125 MHz (center frequency of the bandpass filter). The target specifications of the OTA in order to obtain the required SNR of the ADC can be obtained from system level simulations. A brief summary of the required OTA specifications is shown in Table 5.4.

Table 5.4. Target specifications for the OTA

Parameter	Value
Transconductance (g_m)	2 mA/V
DC gain	> 30 dB
Excess phase @ 125 MHz	< 2°
IM3 @ 125 MHz (0.5 V_{p-p} input)	< -65 dB
Integrated noise (1 MHz BW around 125 MHz)	< 100 μV_{rms}

A review of the different types of OTA implementation and the different linearization techniques for extending their linear range of operation can be found in [60] and [61]. A complementary differential pair which utilizes both NMOS and PMOS transistors results in high frequency of operation without any increase in power consumption [62]. The most common choice of linearization technique of a differential pair is source degeneration, which extends the linear range at the cost of increased noise and power consumption. Non-linearity cancellation using cross-coupling is another technique to improve the linearity of OTA structures [63]. The proposed OTA structure combines the techniques used in [62] and [63] together with source degeneration in order to obtain good linearity performance at high frequency.

The schematic of the linearized fully differential OTA used in the IF ADC design is shown in Fig. 5.11. NMOS transistors M1 and PMOS transistors M2 together with resistors R1, R2 and the triode transistor M7 form the basic complementary differential pair with source degeneration. PMOS transistors M2 are cross coupled in the differential pair in order to obtain non-linearity cancellation [63]. The effective small signal transconductance of the proposed OTA structure is given by

$$g_{\mathrm{m,eff}} = \frac{g_{m1}}{1+N_n} - \frac{g_{m2}}{1+N_p} \tag{5.16}$$

where g_{m1} and g_{m2} are the small signal transconductances of transistors M1 and M2. Nn and Np are the source degeneration factors and are given by

$$N_{\mathrm{n}} = g_{m1}\left[R1 + \frac{R_{M7}}{2}\right] \tag{5.17}$$

$$N_{\mathrm{p}} = g_{m2}R_2 \tag{5.18}$$

where R_{M7} is the resistance of transistor M7 operating in triode region and is given by (5.19).

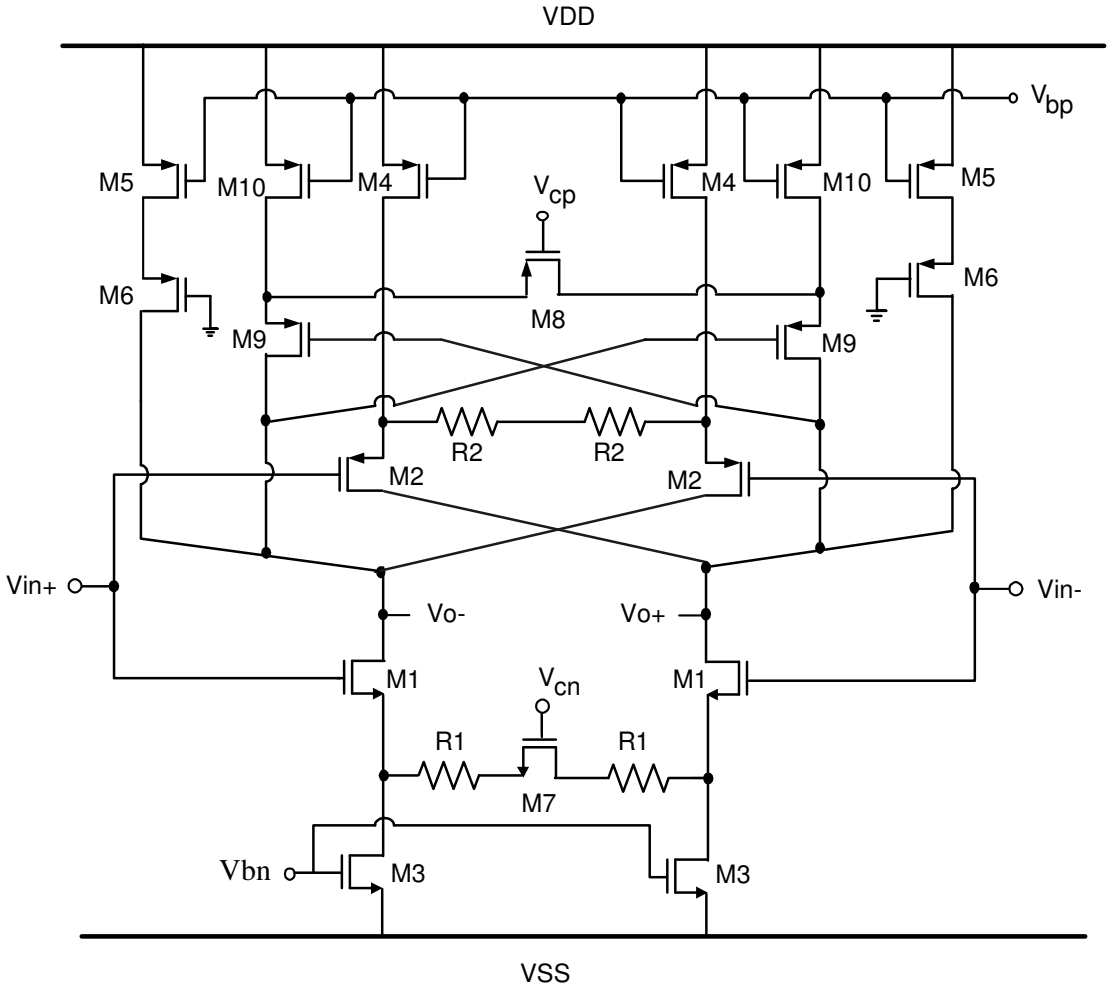


Fig. 5.11. Schematic of the linearized fully differential OTA

$$R_{M7} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M7}\left(V_{gs} - V_{th}\right)_{M7}} \tag{5.19}$$

where μ_n is the mobility of the NMOS transistor, C_{ox} is the gate oxide per unit area, W and L are the width and length of M7, V_{gs} is the gate source voltage and V_{th} is the threshold voltage of M7. The gate control voltage V_{cn} varies the resistor of M7, which in turns changes the effective transconductance ($g_{m,eff}$) of the OTA by about ± 5% without significant linearity degradation. PMOS transistors M9 are connected using positive feedback, which leads to negative resistance at the output. PMOS transistor M8 operates in triode region and its resistance is similar to (5.18), where the NMOS parameters are replaced by the PMOS parameters. The source degeneration triode transistor M8 provides linear operation for the negative resistance. The output resistance of the OTA is given by (5.20), the negative resistance term is given by (5.21) and the positive resistance term is given by (5.22).

$$R_{out} = \frac{1}{\left(\frac{1}{R_{pos}} - \frac{1}{R_{neg}}\right)} \tag{5.20}$$

$$R_{neg} = \frac{1}{g_{m9}}\left(1 + \frac{1}{2\mu_p C_{ox}\left(\frac{W}{L}\right)_{M8}\left(V_{gs} - V_{th}\right)_{M8}}\right) \tag{5.21}$$

$$R_{pos} = [g_{m2} r_{o2} (R2 // r_{o4})] // g_{m6} r_{o6} r_{o5} // \left[g_{m1} r_{o1} (R1 + \frac{1}{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{M7} (V_{gs} - V_{th})_{M7}}) \right] \quad (5.22)$$

where g_{mi} is the transconductance of the i^{th} transistor, r_{oi} is the output resistance of the i^{th} transistor and μ_p is the mobility of the PMOS transistor. The DC gain of the OTA is given by (5.23).

Table 5.5. Component and current values for the OTA design

Component	Value	Bias current (mA)
M1 (W/L)	76 µm /0.4 µm	1.5
M2 (W/L)	60 µm /0.4 µm	0.375
M3 (W/L)	100 µm /0.6 µm	1.5
M4 (W/L)	90 µm /0.6 µm	0.375
M5 (W/L)	180 µm /0.6 µm	0.75
M6 (W/L)	120 µm /0.4 µm	0.75
M7 (W/L)	86 µm /0.4 µm	0
M8 (W/L)	1.5 µm /0.4 µm	0
M9 (W/L)	60 µm /0.4 µm	0.375
M10 (W/L)	90 µm /0.6 µm	0.375
R1	425 Ω	-
R2	140 Ω	-

$$A_{\text{v,DC}} = g_{m,eff} R_{out} \tag{5.23}$$

where $g_{m,eff}$ is given by (5.16) and Rout is given by (5.20). The gate control voltage of triode transistor M8 is used to vary the DC gain of the OTA, which changes the Q of the bandpass filter. The component and current values for the linearized OTA design are shown in Table 5.5. The simulated transconductance of the OTA is around 2 mA/V, DC gain is greater than 30 dB, IM3 is less than -84 dB and the power consumption is around 10 mW for a supply of ± 1.65 V. The OTA shown in Fig. 5.11 is used for g_{m2} in Fig. 5.4, while the OTA without the negative resistance (without the cross coupling transistors M9) is used for g_{m1} in Fig 5.4 to construct the fourth order g_m-C bandpass filter. The coarse tuning of the center frequency is obtained by varying a bank of capacitors controlled by switches while the fine tuning is obtained by tuning the effective transconductance (gate control of V_{cn}). The Q of the filter is obtained by varying the gate control voltage of transistor M8 (V_{cp}). The tuning range of the center frequency of the bandpass filter from simulations was 82 MHz to 142 MHz, while the Q can be varied from the nominal value of 50 by ± 15%. The details of the OTA design, along with simulation results are discussed in detail in [59].

5.4.2 Current DAC

The schematic of the current DAC is shown in Fig. 5.12. It consists of a simple NMOS differential pair (transistors M1) with PMOS current load (transistors M2) which converts the digital bit stream into current pulses to be injected back into the filter. The

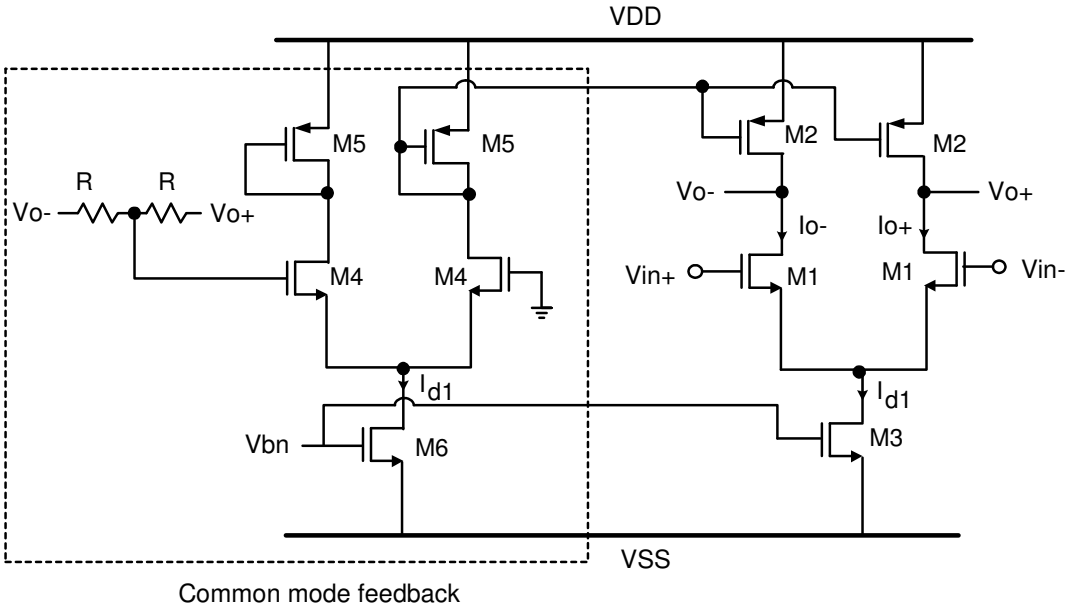


Fig. 5.12. Schematic of the current DAC

common mode feedback circuit is used to set the required common mode voltage of the differential pair. The output common mode voltage is sensed by resistors R, compared

Table 5.6. Component and current values for the current DAC design

Component	DAC1 & DAC2	DAC3	DAC4
I_{d1} (µA)	200	210	187.5
$V_{dsat,M1}$ (V)	0.115	0.116	0.118
M1,M4 (W/L)	35 µm/0.4 µm	36 µm /0.4 µm	32µm /0.4 µm
M3.M6 (W/L)	32 µm /0.8 µm	32 µm /0.8 µm	30 µm /0.8 µm
M2,M5 (W/L)	34 µm /0.4 µm	34 µm /0.4 µm	30 µm /0.4 µm

with the required reference voltage (gate of other transistor M4, zero in this case) and the control voltage (gate of diode transistor M5) is fed back to the gate of transistor M2. The value of R is around 20 KΩ and is chosen such that it doesn't affect the output resistance of the OTA (which is around 10 KΩ), since the DAC output is directly connected to the output of the OTA. The component and current values for the current DAC design is shown in Table 5.6. The DACi (i = 1 .. 4) block refers to the DAC of the ki^{th} coefficient in Fig. 5.4.

5.4.3. Comparator

The block diagram of the comparator implementation is shown in Fig. 5.13. The preamplifier gain stage provides moderate gain for the signals before they are processed by the latch. It also acts like a buffer between the filter and subsequent latches, which prevent the kickback effect [13]. The kickback effect occurs when the transient switching noise of the latch couples back to the input (and to the filter) through parasitic capacitors. The output voltage of the latches undergoes a DC level shift before they are injected into the DAC blocks. The schematic of the preamplifier gain stage is shown in Fig 5.14. It consists of a complimentary differential pair formed by NMOS transistors

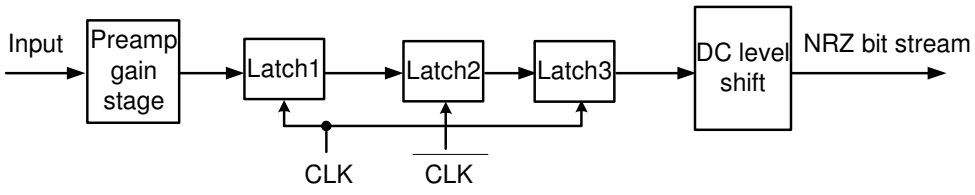


Fig. 5.13. Block diagram of the CMOS comparator

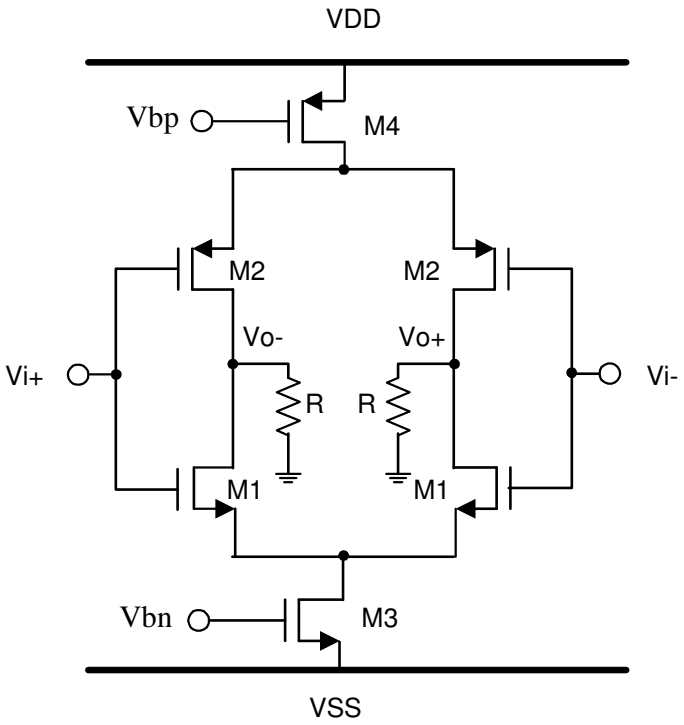


Fig. 5.14. Schematic of the preamplifier gain stage

M1 and PMOS transistors M2, along with current mirror transistors M3 and M4. The resistors R (with one input tied to output and the other grounded) are used to set the common mode voltage at the high impedance output node. The offset current due to mismatch in the differential pair flows into the resistor and sets the common mode voltage at the output node. The DC gain of the amplifier is given by

$$A_{\text{v,DC}} = (g_{m1} + g_{m2})(r_{o1} \parallel r_{o2} \parallel R) \tag{5.24}$$

where g_{mi} is the transconductance of the i^{th} transistor and r_{oi} is the output resistance of the i^{th} transistor. The value of R is 2.5 KΩ and is in the same range as the output

resistance of the differential pair. The component and current values used in the preamplifier gain stage is shown in Table 5.7.

Table 5.7. Component and current values for the preamplifier gain stage

Component	Value	Bias current (mA)
M1 (W/L)	30 µm /0.4 µm	0.775
M2 (W/L)	90 µm /0.4 µm	0.807
M3 (W/L)	200 µm /0.8 µm	1.55
M4 (W/L)	350 µm /0.8 µm	1.614

The schematic of the CMOS latch stage is shown in Fig. 5.15. It is implemented using current mode logic for high speed operation at the clock frequency of 500 MHz. The gate of the differential pair formed by transistors M7 controls the operation of the sampling and quantization phase. When the clock is high, the differential pair formed by transistors M5 is enabled as all the bias current is steered through it (other differential pair is off) and the input signals are amplified. When the clock goes low, the cross coupled differential pair formed by transistors M6 is enabled (differential pair is off), and the signals that were sampled at the falling edge of the clock are regenerated by the positive feedback to either a logic zero or one (quantization phase). The available regeneration time for the latch is 1 ns (one-half of the clock period) and the output settles to either of the logic values within that time period. The regenerative time constant of

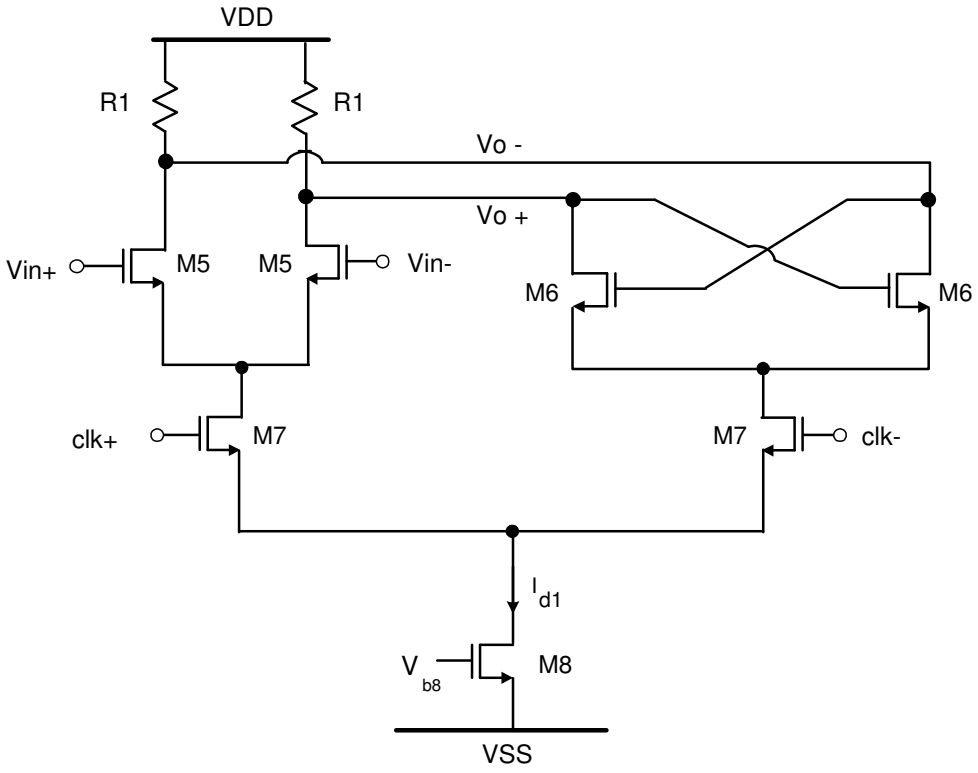


Fig. 5.15. Schematic of the latch

the latch determines time delay in the latch (the output settles within five time constants), and the regenerative time constant is given by

$$\tau_{\text{regeneration}} = \frac{2C_{tot,out}}{g_{m6}} \tag{5.25}$$

Where $C_{tot,out}$ is the sum of all parasitic capacitances at the output node and g_{m6} is the transconductance of transistor M6. g_{m6} is proportional to the square root of the bias current and the latch settles faster at the cost of higher power consumption. A cascade of three latches driven by different clock phases as shown in Fig. 5.13 results in $z^{-1/2}$ delay. The propagation delay in comparator, DAC's and routing parasitics adds to this delay

and the resulting worst case total delay (from simulations) is less than one clock period (z^{-1} delay). This approach of incorporating circuit propagation delays (carefully adjusted according to post layout simulations) in the required overall delay helps to overcome the excess loop delay problem in this design. The component and current values used in the comparator design is shown in Table 5.8. The power consumption of the latch was optimized for good performance (no error in single-bit detection), which involved

Table 5.8. Component and current values for the latch stages

Stage	Component	Value	Bias current (mA)
First latch	M5 (W/L)	20 µm /0.4 µm	0.775
	M6 (W/L)	40 µm /0.4 µm	
	M8 (W/L)	125 µm /1 µm	
	M7 (W/L)	25 µm /0.4 µm	
	R1	800 Ω	
Second latch	M5 (W/L)	20 µm /0.4 µm	0.775
	M6 (W/L)	40 µm /0.4 µm	
	M8 (W/L)	125 µm /1 µm	
	M7 (W/L)	25 µm /0.4 µm	
	R1	800 Ω	
Third latch	M5 (W/L)	40 µm /0.4 µm	1.55
	M6 (W/L)	50 µm /0.4 µm	
	M8 (W/L)	250 µm /1 µm	
	M7 (W/L)	50 µm /0.4 µm	
	R1	300 Ω	

optimizing the bias current of the latch for a specific regeneration time. A higher drive current is used in the third latch stage as it has to drive the subsequent DAC stages. A lower value of load resistor (R1) is used for the third stage to make sure the signal swing is within ± 400 mV for the required operation at 500 MHz clock frequency. The post-layout transient simulation of the comparator is shown in Fig. 5.16. The differential swing at the comparator output is around ±350 mV and the nominal regeneration time for the latch is around 180 ps for an input signal of 100 µV (preamplifier adds gain to this signal before the latch). The DC level shifting block is implemented using C-R network, similar to the one shown in Fig. 4.19.

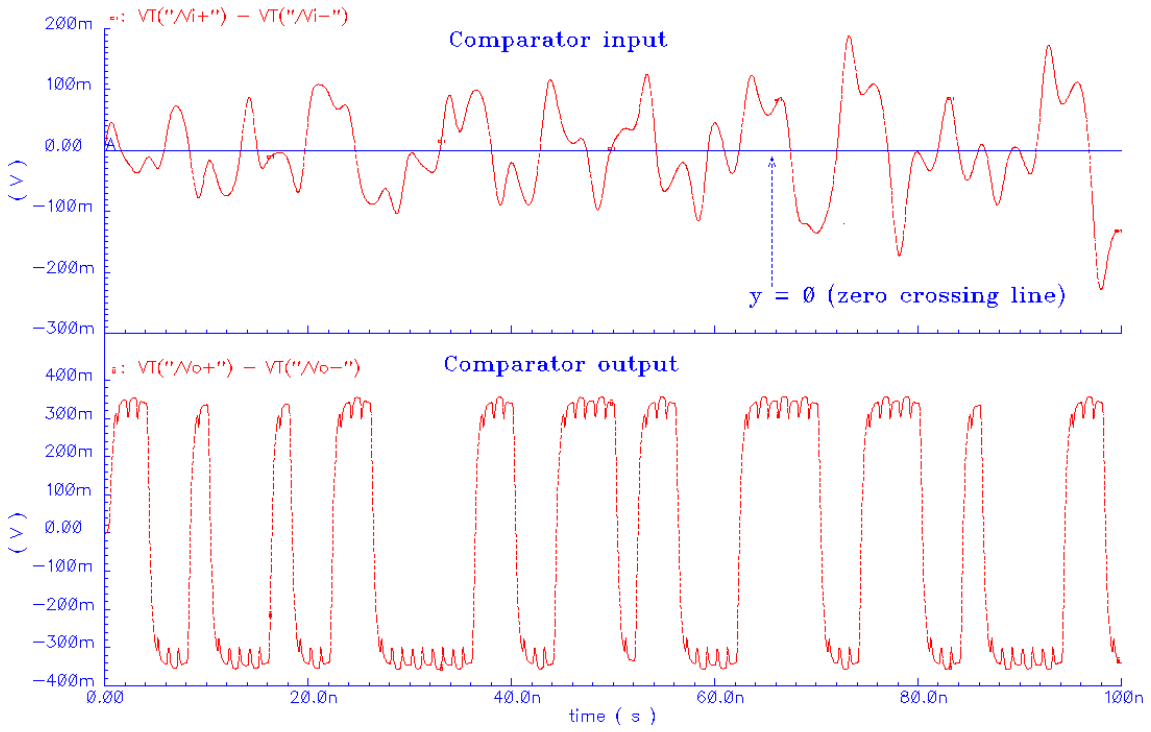


Fig. 5.16. Post-layout transient simulation of the comparator

5.5. Top level simulations

The top level circuit implementation of the IF ADC is obtained by connecting the circuit implementation of all the building blocks according to the architecture shown in Fig. 5.4. The microphotograph of the IF ADC chip (core ADC + digital blocks) is shown in Fig. 5.17 and it occupies an area of 4.16 mm^2. The chip was designed in TSMC 0.35 µm CMOS technology through the MOSIS educational program. The OTA, DAC and the comparator blocks form the core of the ADC design. The capacitor array is used

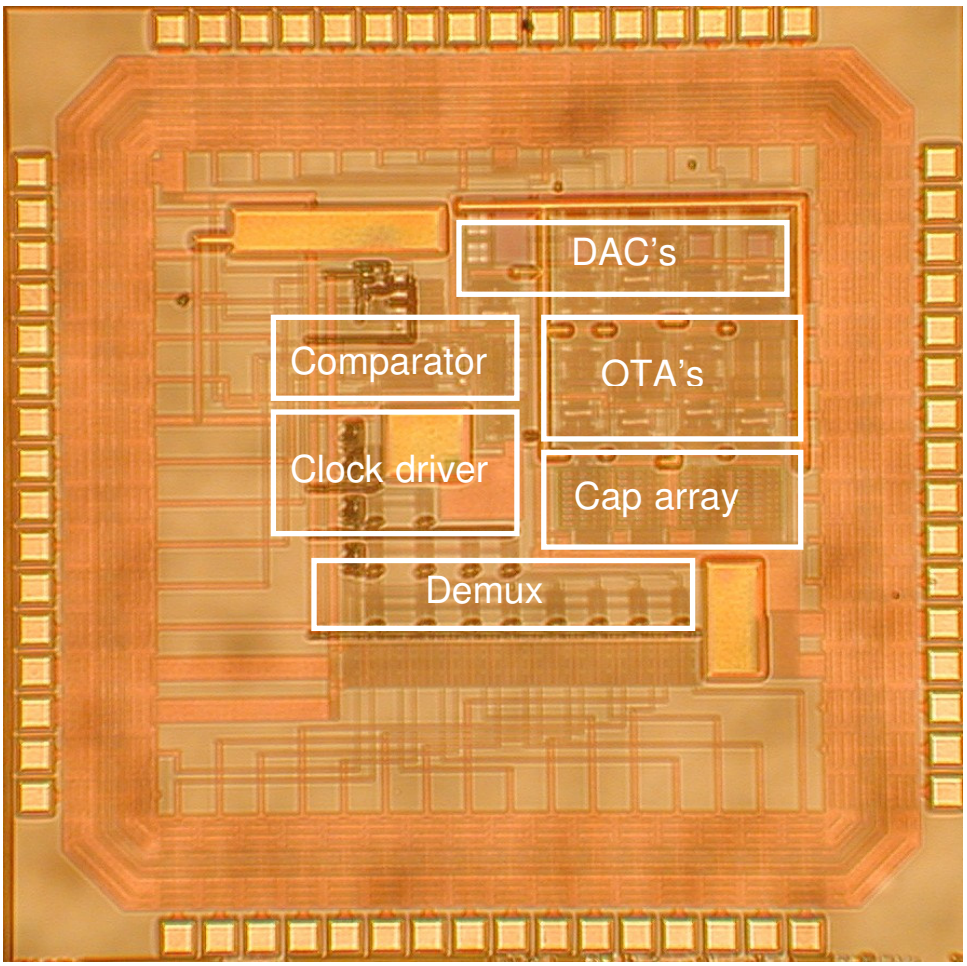


Fig. 5.17. Chip microphotograph of the IF ADC

for coarse tuning of the center frequency of the bandpass filter and the digital blocks include the clock driver and the demultiplexer (Demux). The clock driver is used to drive an external clock signal to the comparator and the demultiplexer performs a serial to parallel conversion (higher to lower clock rate) of the output bit stream for external capture using a data acquisition board.

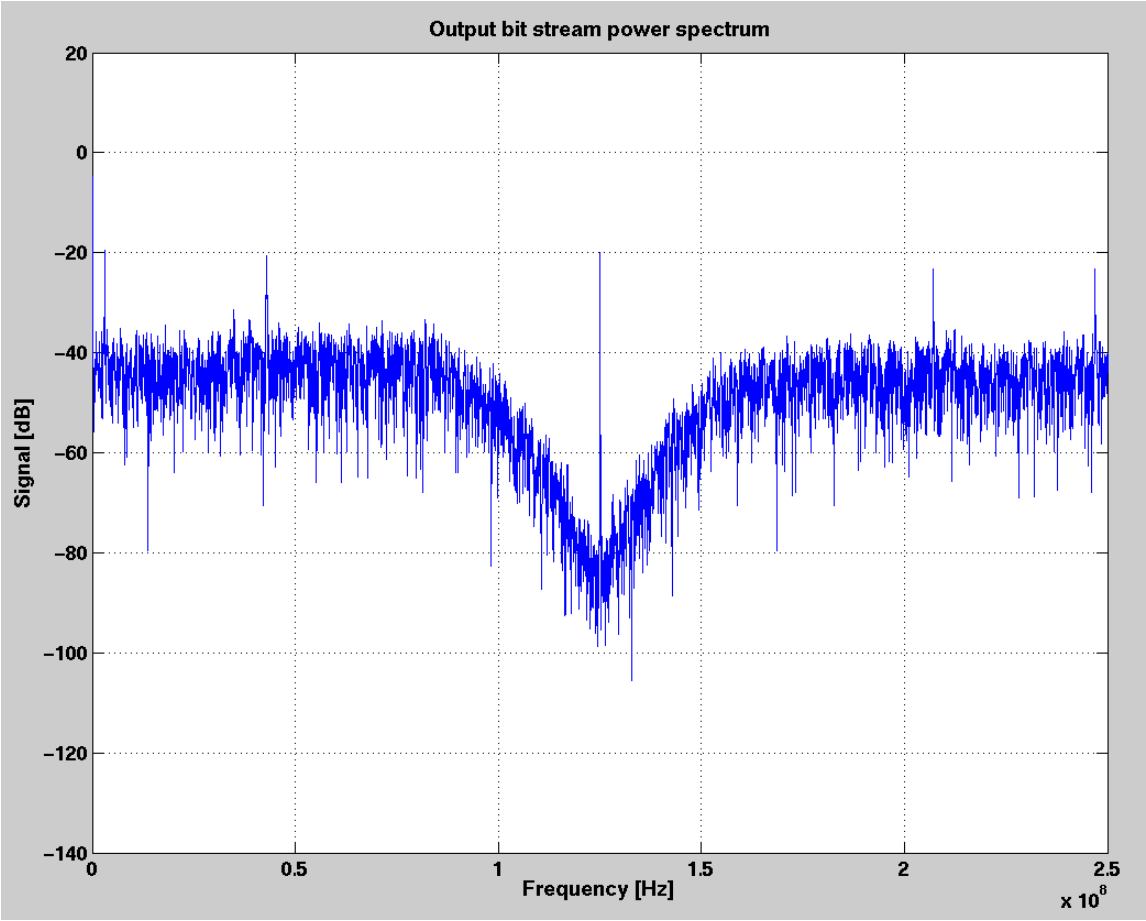


Fig. 5.18. Output spectrum of the IF ADC from post-layout simulations

The transient simulation of the ADC is performed in Cadence by applying a test input signal at 125 MHz. The output bit stream file is processed in Matlab and the SNR of the ADC is calculated by using the FFT command. The power spectrum of the output bit stream of the ADC from post-layout simulations is shown in Fig. 5.18. The number of samples used is 16384 and the output SNR was 50 dB in a 1 MHz bandwidth around 125 MHz. The number of samples is restricted by the limited computing resources, since a top level extracted simulation can take about 5 days to generate 16384 samples. A higher number of samples (65536 samples) are required to get a more accurate estimate of signal and noise power values. The ADC designed in TSMC 0.35 μm CMOS technology consumes 152 mW of power from ± 1.65 V power supply. The chip is currently under characterization and measurement results were not available at the time this dissertation was written.

5.6. Conclusions

The design of a fourth order CT BP ΣΔ ADC for IF digitization around 125 MHz was presented in this chapter. The continuous time loop filter in the forward path was implemented using g_m-C filter and a NRZ DAC pulse shape was used to minimize the effects of clock jitter. The design and simulation of the ADC architecture was presented. A new system level automatic digital tuning scheme was proposed to overcome problems associated with analog tuning techniques. The tuning scheme captures the output bit stream using an external data acquisition board and it is processed in a DSP in order to tune the center frequency and Q of the NTF of the ADC for good SNR

performance. The circuit implementation of a new linearized OTA architecture which gives good linearity performance at 125 MHz was discussed, along with other building blocks of the ADC.

CHAPTER VI

CONCLUSIONS

6.1. Summary

The strong growth in the wireless communications industry has led to the development of a large number of wireless standards for various market segments (cell phones, wireless networking, global positioning etc.). The main requirement of the next generation wireless devices is the support of multiple standards on the same chipset with negligible increase in power consumption and this issue is addressed in this work.

A brief introduction to the different wireless market segments and the different standards was presented in Chapter I. The role of analog to digital converter blocks in communication receivers was discussed in Chapter II. The different types of traditional receiver architectures (superheterodyne, direct conversion) were analyzed and found to be ineffective for supporting multiple standards. The software radio architecture has been proposed as an alternative to the traditional receiver architectures and it can support multiple standards by performing A/D conversion of the RF signals and running reconfigurable software programs on the backend digital signal processor. A slight variation of this architecture is the software defined radio architecture (also called digital IF architecture) where the A/D conversion is performed on IF signals after a single down conversion. The main types of A/D converter architectures were examined to determine the optimal choice for a software radio application. A switched capacitor bandpass ΣΔ ADC design in TSMC 0.35 μm CMOS technology using a feedforward compensated

operational amplifier achieved SNR of 80 dB in 200 KHz bandwidth around a center frequency of 23 MHz. The clock frequency used was 92 MHz and the power consumption is 47.5 mW from a supply voltage of ± 1.25 V. The switched capacitor bandpass ΣΔ ADC implementation has the potential to achieve high resolution, but the clock frequency cannot exceed 200 MHz even if more advanced silicon technologies are used. A continuous time bandpass ΣΔ ADC architecture is found to a good choice for digitization of IF and RF signals with higher clock frequencies, which makes it suitable for both software radio and digital IF architectures. A literature survey of ADC's for RF and IF digitization was presented in the last section of Chapter II. Though the reported RF/IF ADC implementations achieve high resolution, the main bottleneck is high power consumption (in the Watt range) and they are not suitable for use in portable wireless devices.

A brief overview of the design procedure and various non-idealities of a CT BP ΣΔ ADC was presented in Chapter III. The design procedure uses an impulse invariant transformation to derive the continuous time bandpass ΣΔ architecture from its equivalent discrete time (switched capacitor) ΣΔ architecture. The effect of various non-idealities (clock jitter, excess loop delay, comparator metastability, finite quality factor of the bandpass loop filter, unequal rise/fall time of DAC pulses) on the performance of a CT BP ΣΔ ADC were examined, followed by a discussion of design techniques to minimize their effects. The final section of Chapter III reviews some of the reported architectures for direct RF digitization and identifies some of their major problems that affect the performance of the ADC.

The design of a fourth order CT BP ΣΔ ADC based on LC filters for direct RF digitization at 950 MHz center frequency was presented in Chapter IV. A new architecture based on a combination of integrator DAC's and current DAC's in the feedback path is proposed which enables the use of non return to zero (NRZ) DAC pulses with full control of tuning all the coefficients in the noise transfer function (NTF). The NRZ DAC pulse in the feedback path minimizes the effects of clock jitter and the tuning of NTF coefficients ensures good SNR performance. The effect of using ideal integrator DAC in the proposed architecture is examined in detail and the analysis showed that the SNR performance degrades when long string of consecutive 1's or 0's were present in the output bit stream. A modified version of the architecture using lossy integrator DAC's is proposed to ensure robust operation of the ADC. Power optimization techniques were used both at the architectural and at the circuit level to minimize the overall power consumption of the ADC. The proposed ADC architecture was implemented in IBM 0.25 μm SiGe BiCMOS technology and measurement results show SNR of 63 dB and 59 dB for bandwidths of 200 kHz and 1 MHz respectively, around 950 MHz with a clock frequency of 3.8 GHz. The IM3 of the ADC was measured to be -62 dB for -8 dBm two input tones at 949 MHz and 951 MHz. The ADC consumed 75 mW of power from a supply voltage of ± 1.25 V.

The design of a fourth order CT BP ΣΔ ADC based on g_m-C filters with an automatic digital tuning scheme for IF digitization at 125 MHz center frequency was presented in Chapter V. The architecture uses a cascade of two g_m-C resonators with four current DAC's in the feedback path, which gives full control over tuning of all

coefficients in the NTF. A linearized CMOS OTA architecture combines both cross coupling and source degeneration in order to obtain good IM3 performance at 125 MHz. A system level automatic digital tuning scheme is proposed to tune the ADC performance over PVT variations. A test signal is applied at the input of the comparator rather than the ADC input, which helps to estimate the NTF directly by analyzing the output bit stream. The bit stream is captured using an off-chip data acquisition board and processed by an external DSP. The tuning algorithm runs on the DSP and it generates the required control signals to tune the center frequency and Q of the filter. Additionally, the tuning scheme also changes the feedback DAC coefficients to ensure the best possible SNR at the ADC output. One of the main advantages of this tuning scheme is that the estimation and correction process takes into account the non-idealities of all the blocks (filter, comparator and DAC) in the loop, which results in the best performance for the ADC. The ADC was designed in TSMC 0.35 μm CMOS technology and it consumes 152 mW of power from ± 1.65 V power supply. The simulation results show SNR of 50 dB for a 1 MHz bandwidth around 125 MHz for a clock frequency of 500 MHz and the chip is still under characterization.

6.2. Future research work

The measurement results of the RF ADC designed in this research work shows that high resolution narrowband (200 kHz – 1 MHz) direct RF digitization is possible with low power consumption. However, the ADC design falls short of meeting the requirements of software radio architecture described in Chapter II. The main

requirement of the ideal software radio architecture is a wideband ADC design with variable bandwidth and low power consumption, which is not feasible in currently available IC technologies. The next step in this research would be to explore techniques for a wideband ADC design with the constraint of low power consumption. Another interesting topic of research is to explore methods for obtaining both variable loop bandwidth and center frequency in order to support multiple standards. The current trend in transceiver design is to develop a single chip CMOS transceiver which integrates analog, RF and digital base band circuits in the same chip (system on chip approach). The ADC design in this research work was done in SiGe BiCMOS technology and only bipolar junction transistors (BJT) were used in the signal path. The RF ADC design can be ported to a more advanced CMOS technology (like 90 nm CMOS), which is another good research topic. The main problem in CMOS RF ADC design is the requirement of a very linear CMOS transconductor block with good performance at 1 GHz. In BJT's, the transconductance is proportional to the emitter current whereas the transconductance of a MOS device is proportional to the square root of drain current. This difference in transconductance values makes the CMOS transconductor design with low power consumption constraint a very challenging task at GHz frequency range. The output of the single-bit RF ΣΔ ADC has to be processed (decimation filter, down sampling or a combination of both) before it can be given to the ADC. The implementation of these post-processing blocks at GHz frequencies with low power constraint is another interesting research topic. There are many significant technical hurdles at the hardware

implementation level which have to be overcome to develop a comprehensive software radio solution.

The digital tuning scheme for the IF ADC design currently uses several tuning parameters in the algorithm. The detailed study of the sensitivity of parameters is an interesting topic for future research. Based on the sensitivity, the tuning algorithm can be adapted to simplify the tuning approach which decreases the overall time required for tuning. The time required for tuning is an important parameter as this is an offline tuning scheme (which requires disabling of the ADC during the tuning time) and any improvement in the algorithm to reduce the time for tuning offers a significant advantage for the proposed tuning scheme. Another possibility that could be explored in the IF ADC design is the potential use of an active-RC implementation only in the first stage, which has much better linearity as compared to a g_m-C filter. This approach is usually used in CT low pass ΣΔ ADC's where the inherent feedback around the operational amplifier in the active RC stage provides a linear block for the first stage. The bandpass filter works at higher frequency and would require demanding specifications for the operational amplifier to ensure proper closed loop behavior.

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