SYSTEM-LEVEL DESIGN AND RF FRONT-END IMPLEMENTATION FOR A 3-10GHZ MULTIBAND-OFDM ULTRAWIDEBAND RECEIVER AND BUILT-IN TESTING TECHNIQUES FOR ANALOG AND RF INTEGRATED CIRCUITS

A Dissertation

by

ALBERTO VALDES GARCIA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2006

Major Subject: Electrical Engineering

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ABSTRACT

System-level Design and RF Front-end Implementation for a 3-10GHz MultiBand-OFDM UltraWideBand Receiver and Built-in Testing Techniques for Analog and RF Integrated Circuits. (May 2006)

Alberto Valdes Garcia, B.S. (Hons.), ITESM Campus Toluca

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

This work consists of two main parts: a) Design of a 3-10GHz UltraWideBand (UWB) Receiver and b) Built-In Testing Techniques (BIT) for Analog and RF circuits.

The MultiBand OFDM (MB-OFDM) proposal for UWB communications has received significant attention for the implementation of very high data rate (up to 480Mb/s) wireless devices. A wideband LNA with a tunable notch filter, a down-conversion quadrature mixer, and the overall radio system-level design are proposed for an 11-band 3.4-10.3GHz direct conversion receiver for MB-OFDM UWB implemented in a 0.25μm BiCMOS process. The packaged IC includes an RF front-end with interference rejection at 5.25GHz, a frequency synthesizer generating 11 carrier tones in quadrature with fast hopping, and a linear phase baseband section with 42dB of gain programmability. The receiver IC mounted on a FR-4 substrate provides a maximum gain of 67-78dB and NF of 5-10dB across all bands while consuming 114mA from a 2.5V supply.

Two BIT techniques for analog and RF circuits are developed. The goal is to reduce the test cost by reducing the use of analog instrumentation. An integrated frequency

response characterization system with a digital interface is proposed to test the magnitude and phase responses at different nodes of an analog circuit. A complete prototype in CMOS 0.35μm technology employs only 0.3mm^2 of area. Its operation is demonstrated by performing frequency response measurements in a range of 1 to 130MHz on 2 analog filters integrated on the same chip. A very compact CMOS RF RMS Detector and a methodology for its use in the built-in measurement of the gain and 1dB compression point of RF circuits are proposed to address the problem of on-chip testing at RF frequencies. The proposed device generates a DC voltage proportional to the RMS voltage amplitude of an RF signal. A design in CMOS 0.35μm technology presents and input capacitance <15fF and occupies and area of 0.03mm^2. The application of these two techniques in combination with a loop-back test architecture significantly enhances the testability of a wireless transceiver system.

To you

For whom the soil became feathers,
for whom the feathers fell to become burnt and broken

To you

To your silent words,
your absent gaze,
your empty presence

To the boundaries of this void that still outline your shape

To the shadow of your light

To you

with

~ anything that remains from my almost extinct ~

Love-Devotion

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The development and test of the UWB receiver was possible through the support from different individuals and technical groups at Texas Instruments (TI) Dallas. I thank Dr. Anuj Batra, Dr. Jaiganesh Balakrishnan, Dr. Nathan Belk and Dr. Antonio F. Mondragon-Torres from the DSPS Research and Development Center of TI for helpful discussions, and the RF Wireless Group of TI, Dallas for testing facilities.

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CHAPTER I

INTRODUCTION

Information transfer, storage, and processing have been some of the major driving forces of scientific development in recent years. In particular, wireless communication devices have shown a very significant advancement in sophistication, miniaturization and performance. The work presented in this dissertation addresses three of the most important problems in the development of integrated circuits for wireless communications. These are: (1) To map the specifications of a communication standard into an architecture and specifications for the building blocks to optimize the performance of the system. (2) To design and implement circuits operating at GHz frequencies that serve as the front-end of the communication device with the channel. (3) To improve the testability of the analog and RF circuit components that form a communication system to reduce its overall cost and accelerate its time-to-market. For the first two items, the focus is on Ultra Wide Band (UWB), a communication technology that has received a continuously increasing attention in recent years.

1.1. Short range wireless systems and UWB technology

Recent wireless technologies like Bluetooth and Wi-Fi have joined cellular standards (CDMA, GPS) in a great variety of commercial successful applications with ever increasing data rate demands. The mentioned technologies share a common property: all

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This dissertation follows the style of *IEEE Transactions on Microwave Theory and Techniques.*

of them are narrowband systems, which means that the bandwidth they use is much smaller than their carrier frequencies. For example, Bluetooth employs a carrier frequency of 2.4GHz and a channel bandwidth of 2MHz. The required technology for such systems (integrated circuit implementation, digital signal processing, software, etc.) has been developing continuously for the last 20 years and has reached a certain degree of maturity.

54Mbps is the maximum data rate for the IEEE 802.11g standard and is the highest data rate achieved so far by a commercial narrow band wireless technology. However, existing and emerging applications in the wireless personal area network (WPAN) space (less than 10 meters) demand data rates from 50Mbps to 1Gbps. To expand the data rate capabilities of wireless communications demands to go beyond the traditional narrow band approach. In February 2002, the U.S. Federal Communications Commission (FCC) licensed the frequency spectrum from 3.1 to 10.6 GHz for use by ultra wide band UWB devices [1], opening new possibilities for medical, radar, surveillance, vehicular, and personal communication applications.

Due to its high channel capacity, a UWB system is an attractive solution for the implementation of very high data rate (>100Mbps) short-range wireless networks. Among the different options for the efficient use of the available UWB spectrum in personal computer and consumer electronic applications, the multiband (MB) orthogonal frequency division multiplexing (OFDM) approach has received a strong support from several industrial organizations [2]. In the MB-OFDM proposal the 7500 MHz UWB spectrum is divided into 14 bands of 528 MHz each. The bands are grouped into 5 band

groups and only the first band group, corresponding to the lower part of the spectrum (3.1-4.8 GHz), is considered as mandatory by the current standard proposal. The remaining band groups have been defined and left as optional to enable a structured and progressive expansion of the system capabilities. Chapter II provides an overview of MB-OFDM technology. Current efforts from semiconductor companies for the implementation of UWB devices focus on the first band group (which represents only 25% of the available spectrum) to achieve a faster time-to-market and affordable power consumption with current CMOS and BiCMOS technologies. An experimental 7-band UWB receiver covering the range of 3-8GHz has been demonstrated but it is not integrated in a package. To attain a fully integrated and packaged implementation of a UWB receiver covering the 3-10GHz spectrum licensed by the FCC is a challenge that opens a number of research opportunities at both system and circuit levels.

An integrated and packaged UWB receiver that covers 78% of the spectrum licensed by the FCC in 11 bands has been developed and evaluated experimentally. Chapter III discusses the system-level design considerations. The design of the RF front-end circuits is described in Chapter IV. The experimental results from the receiver IC fabricated in SiGe BiCMOS technology are presented in Chapter V.

1.2 Built-in testing techniques for cost-efficient IC development

The development of modern systems on chip (SoC) and systems in package (SiP) has witnessed a continuous increase in the amount and diversity of the integrated components, which include memory, processor cores, sensors, analog/RF circuits, etc.

As the complexity of these systems has grown, their testing at both, the product development and mass-production phases, has become increasingly challenging and one of the major portions of the overall cost. While solutions for the automated test of very large memory and digital cores are relatively well established, the challenges associated with the observability and test-cost of embedded analog/RF blocks remain an important bottleneck to guarantee the cost efficiency of contemporary and future integrated systems.

Conscious of these evolving challenges for the semiconductor industry, the most recent (2003) edition of the International Technology Roadmap for Semiconductors (ITRS) [3] calls for the development/improvement of solutions for different test problems. Some of the most important are: (1) Development of SoC test methodology, including test reusability and analog/digital built-in self-test (BIST). (2) Design-for-test (DfT) methods to localize failures and enable both development and production testing. (3) Wafer-level test and known good die (KGD) test methodologies. (4) Analog DfT and BIST techniques that simplify test interface requirements and slow ever increasing instrument capability trends.

Two of the most important challenges that test engineering faces to make a wireless product competitive are (1) to accelerate the time-to-market by providing a fast fault diagnosis during the product development process and (2) to reduce the cost of testing for high-volume manufacturing. For these reasons, the development of efficient testing techniques for analog/RF systems and components has drawn significant attention in recent years. Several BIST and DFT techniques for analog and RF circuits have been

developed in recent years; [4-6] present a comprehensive summary of these efforts. Most of these reported techniques have been discussed only through simulation results and important issues related to their integrated implementation have not been addressed. A few on-chip testing schemes have been demonstrated experimentally with integrated prototypes, however, solutions with smaller area overhead, lower off-chip data processing and higher frequency of operation are required.

A robust technique for magnitude and phase response characterization based on an analog multiplier is proposed. Based on that approach a complete integrated frequency response characterization system (FRCS) is developed. The goal of this system is to test the most important specifications of integrated analog circuits (gain and phase shift at different frequencies) by using very compact and simple test circuitry that communicates with automatic test equipment (ATE) through a low-speed digital interface. The application focus is on continuous time circuits operating in the range of tenths to hundreds of MHz, which are the most common building blocks for baseband signal processing in SoCs. The design and experimental results for this system are described in Chapter VI.

One of the most difficult challenges in the implementation of BIT techniques for integrated RF components and systems is to observe high frequency signal paths without affecting the performance of the attached RF building blocks and with low area overhead. The practical on-chip observation of signals in the GHz range through DC measurements can significantly improve the effectiveness and cost-efficiency of the testing of modern integrated communication systems. To address this problem, a very

compact CMOS RF RMS detector and a methodology for its use in the built-in measurement of the gain and 1dB compression point of RF circuits are proposed. This BIT technique is described in Chapter VII

Chapter VIII presents an overall testing strategy for an integrated wireless transceiver with basis on the two techniques described above and a loop-back architecture. The objective is to detect and locate major catastrophic and parametric faults at the wafer level avoiding the use of RF instrumentation and through a low-cost interface of digital signals and DC voltages.

Finally, Chapter IX summarizes the contributions of this dissertation and discussed future work.

CHAPTER II

OVERVIEW OF MULTI-BAND OFDM ULTRAWIDEBAND TECHNOLOGY

2.1 Short-range wireless standards

The need for sending large volumes of data over very long distances and at very high speeds, while providing good quality service to a large number of users all at the same time, serves as the driving force for the ever growing RF and wireless industry. The above mentioned attributes of a system are not achievable simultaneously, owing to the constraints posed by physical laws and the non-ideal wireless medium. Hence tradeoffs are inevitable in any wireless system, and this fact has led to the increasing interest in short range wireless systems, (less than 10 meters) which sacrifices distance for improving other characteristics. Short-range wireless is a complementary class of emerging technologies meant primarily for indoor use over short distances [7]. The growth of short-range wireless systems is primarily driven by: (1) Higher data rate capabilities in portable devices at lower cost and power. (2) Congestion in the radio frequency spectrum that is allocated in traditional ways. (3) Increasing growth of high speed wired access to the internet in enterprises, homes, and public spaces. (4) Shrinking cost and power consumption of semiconductor-based signal processing.

The first two factors are in favor of systems that offer higher bit rates along with high spatial capacity (defined as bits per second per square meter or bps/m^2). The third factor has paved the way for the launch of short-range wireless standards such as

Bluetooth, Wi-Fi (the leading technologies for wireless PANs and LANs respectively), and an emerging technology called Ultra Wide Band (UWB). The fourth factor helps in implementing sophisticated signal processing techniques in portable devices. So far, more importance has been given to the range of a wireless system than to its spatial capacity. A higher spatial capacity can be achieved by a wireless system by reducing its transmission power and consequently its range. The goal of UWB technology is to provide very high data rates (up to 480Mbps) at modest cost and low power consumption. Table 2.1 presents a summary of the characteristic of current short-range wireless communication technologies. As it will be described in section 2.3, there are different ways of implementing a UWB communication system. The data included in the UWB column of Table 2.1 corresponds to the particular case of a MB-OFDM system.

Table 2.1 Overview of short-range wireless standards

Characteristic	Bluetooth	IEEE 802.11b	IEEE 802.11g	IEEE 802.11a	UWB
Max. data rate	1 Mb/s	11 Mb/s	54 Mb/s	24 and 54 Mb/s	480 Mb/s
Max. distance	10 m	100 m	100 m	50 m	10 m
Frequency allocation	2.4 GHz	2.4 GHz	2.4 GHz	5.15-5.35GHz and 5.725-5.825 GHz	3.1-10.6 GHz
Channel bandwidth	1 MHz	25 MHz	25 MHz	20 MHz	Min. 500 MHz Max. 7.5 GHz
Modulation	GFSK	QPSK with CCK coding	CCK	COFDM BPSK, 16 QAM	BPSK, QPSK
Spreading	DS-FH	CCK	OFDM	OFDM	Multiband, OFDM
Max. transmit power	0 dBm	30 dBm	30 dBm	0.05, 0.25 & 1W	-41 dBm/MHz
Maximum Sensitivity	-70 dBm BER < 10^{-3}	-76 dBm BER <10^{-5}	-76 dBm FER <8×10^{-2}	-82 dBm FER <10^{-5}	-73 dBm

The US Federal Communication Commission (FCC) defines UWB signals as having a fractional bandwidth greater than 0.25 or a UWB bandwidth greater than 500MHz. The UWB bandwidth is defined as the frequency band bounded by the points that are 10dB below the highest radiated emission [1]. The FCC ruling allows UWB communication devices to operate at low power (an EIRP of –41.3 dBm/MHz) in a spectrum from 3.1 to 10.6 GHz, this is illustrated in Fig. 1.1. The low emission limits for UWB are to ensure that UWB devices do not cause harmful interference while coexisting with other licensed services. Because of their very low radiated power, UWB systems are impractical for long range communication use, but they appear ideal for short-range and high data rate wireless applications, particularly in the WPAN range of less than 10 meters. From Fig. 1.1 it is important to note the overlap between the Unlicensed National Information Infrastructure (U-NII) band from 5.15-5.825 GHz and the UWB spectrum. While the maximum output power of a UWB transmitter can reach –10 dBm when using 1584 MHz of bandwidth (three bands of 528 MHz), the devices operating in the mentioned U-NII band can have a transmit power of 16 dBm or higher. The interference from WLAN radios using the IEEE 802.11a standard are of particular concern due to their widespread use. This is one of the main reasons why the current efforts from semiconductor companies in the area of UWB communications focus only in the band of 3-5GHz.

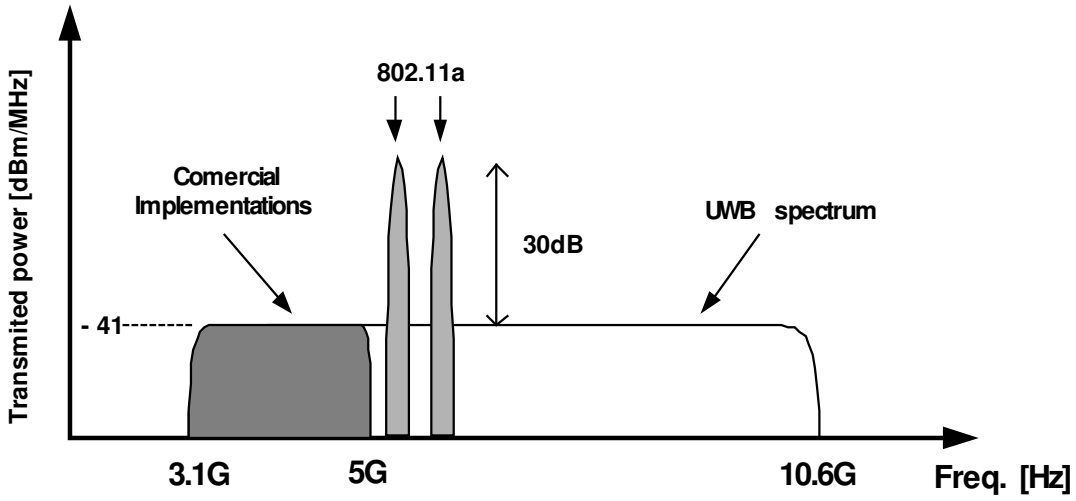


Fig. 1.1 Licensed spectrum for UWB communications

2.2 Potential high data rate applications for UWB technology

This section outlines the existing data rate requirements of some existing and emerging applications in the WPAN space [7-8]. A wireless technology with high data rate capabilities (>50MB/s), such as UWB, is demanded by this wide range of applications.

Video conferencing: This application involves a set of wireless peripherals (at a range of approximately 4m) using video, audio, and application sharing over a broadband connection. The requirements from these devices are listed in Table 2.2.

Table 2.2 Data rate requirements of video conferencing

Component	Data	Maximum data rate
Video camera	Video without compression	150Mb/s
Monitor	Video with varying compression	1Gb/s
Mass storage		240 Mb/s
Mouse, keyboard and audio		~ 100 Kb/s
Total		>1.3 Gb/s

Home theater system: This application involves a set of wireless consumer electronics devices at range of about 10m. The key focus of this collection of devices is the video and audio signals, the data rate requirements are presented in Table 2.3

Table 2.3 Data rate requirements for a home theater system

Component	Data	Max data rate
Monitor/Projector	High definition video	20 Mb/s
Audio equipment	24 bit 5.1 to 10.2 channels	30 Mb/s
Total		~50 Mb/s

Content downloading: In these applications the objective is to reduce the required amount of time to download large amounts of information, such as video, audio and digital images from a computer to or from a portable device. The data rate requirements for these applications are presented in Table 2.4

Table 2.4 Required data rated for content downloading

Downloaded content	Data format	Data rate
Audio	MP3	60 Mb/s
	CD quality	90 Mb/s
Images		90 Mb/s
Movies	Digital Video	>100 Mb/s

2.3 Essential concepts and techniques for UWB communications

2.3.1 Fundamentals and historical perspective of UWB

Due to its recent promotion for consumer electronic devices, UWB technology is often regarded as new. Nevertheless, the use of experimental, scientific and military electric devices that use a wide bandwidth (relative to their center frequency of operation), extends as far as the first experiments with electromagnetic signals in the late 1800s. Amplitude modulation (AM) and frequency modulation (FM) are examples of two well known techniques that have been used to transmit information over a single carrier frequency and using a narrow bandwidth. In contrast, the term 'ultra wideband' has been historically employed to describe those devices that employ short-term pulses (which have a wide spectrum in the frequency domain) and techniques associated with their time-domain properties. UWB signals have been employed for medical imaging systems, measurement systems, and a wide variety of radars: surveillance, military and ground penetrating.

The fundamental advantages of UWB signals for communication applications can be understood by the Shannon capacity theorem, which is one of the most important results

from communication theory. This theorem establishes a relationship between the maximum capacity (C in bits/second) of a communication channel, the signal power (S in watts), the noise power (N in watts) and the channel bandwidth (B in Hz), which can be expressed as:

$$C = B \cdot \log\left(1 + \frac{S}{N}\right) \tag{2.1}$$

Equation 2.1 indicates that the capacity of a channel grows linearly with the used bandwidth while only logarithmically with the signal to noise ratio S/N. In this way, by significantly increasing the signal bandwidth with respect to existent narrowband technologies, UWB can achieve a higher channel capacity with a lower power spectral density (PSD) and hence becomes an effective solution to the ever-increasing data rate demands in the space of wireless personal area networks (WPAN).

Even though UWB technology has been manly associated with time-domain techniques throughout the years, there are also different frequency domain techniques that can be employed to transmit information over a large bandwidth. Three main approaches have been recently proposed for the implementation of very high data rate UWB communication devices. These are: (1) Direct sequence spread spectrum (DS-SS), (2) time-domain / frequency division multiple access (TD/FDMA) and Multiband-OFDM. (MB_OFDM). The first two are described briefly in sub-sections 2.32 and 2.33. The third approach has received the strongest support from the consumer electronics industry and is the one considered by the receiver presented in this dissertation and is described with more detail in section 2.4.

2.3.2 Direct sequence spread spectrum (DS-SS) UWB

In this proposal for UWB communications, the available spectrum is dived into two main bands; one from 3.1 to 5.15 GHz and another from 5.8 to 10.6GHz. The transmitted signal consists of non-sinusoidal wavelets, which are tailored to span the desired spectrum. Multiple users share the same bandwidth and are separated by the digital codes that are employed to perform the spreading of the signal. The employed modulation is multi-level bi-orthogonal keying (M-BOK) in combination with QPSK. These techniques, in combination with forward error correction are meant to combat multi-path propagation and reach a maximum transmission speed of 448Mb/s.

2.3.3 Time-domain / frequency division multiple access (TD/FDMA) UWB

This is the approach for high data rate communications that most resembles the traditional notion of UWB. In this technique, the information is transmitted through pulses that are 3ns long and that are spaced by 550MHz in their time-domain representation. Different users can transmit information at different frequencies and the multi-path is mitigated by the time interval between the pulses that appear on the same channel.

2.4 The multi-band OFDM approach for UWB

Orthogonal frequency division multiplexing (OFDM) is a technology that has been employed successfully in multiple wired and wireless communication systems such as, asymmetric digital subscriber live (ADSL), and 802.11a WLAN. In this modulation

technique, the information is distributed along a set of carriers, which are orthogonal to each other in frequency. Each individual sub-carrier is modulated in phase and amplitude according to a given constellation format such as QPSK or 16-QAM. The employed bandwidth can grow with the number of sub-carriers employed in an efficient manner.

To divide the available UWB spectrum into several sub-bands in combination with OFDM modulation is an effective technique to capture multi-path energy, achieve spectral efficiency and gain tolerance to narrow-band interferences for a very high data rate (>200Mbps) system [2]. This approach, known as multiband OFDM (MB-OFDM), has received a strong support from several academic and commercial organizations and was approved as an industrial standard in December 2005 [9]. In this standard, meant for consumer electronic and personal communication applications, the 7500 MHz UWB spectrum is divided into 14 bands of 528 MHz each. The bands are grouped into 5 band groups. Only the first group of 3 bands, corresponding to the lower part of the spectrum (3.1-4.8 GHz), is considered as mandatory. The remaining band groups have been defined and left as optional to enable a structured and progressive expansion of the system capabilities. For the OFDM symbol, the standard considers 128 carriers, from which 100 tones contain information and the rest are either guard tones or pilot sub-carriers which are employed for synchronization. Each sub-carrier is modulated with a QPSK constellation. The standard takes into account different specifications, coding characteristics, and modulation parameters for different data rates from 55Mb/s to 480Mb/s, which are meant to support transmission distances from 10m to 2m,

respectively. Table 2.5 summarizes the specifications and OFDM symbol parameters that the MB-OFDM UWB standard considers for its highest data rate.

Table 2.5 Summary of MB-OFDM standard specifications for 480Mb/s transmission

Constellation	QPSK
Number of sub-carriers	128
Coding rate	3/4
Symbol length	312.5ns
Cyclic Prefix p	60.6ns
Guard interval	9.5ns
Average transmitted power	-10.3dBm
Packet error rate	8%
Required sensitivity	-70.4dBm
Transmission distance	2m

CHAPTER III

3-10GHZ MB-OFDM UWB RECEIVER: SYSTEM DESIGN

Current efforts from semiconductor companies for the implementation of integrated UWB devices [10-11] focus on the 3-band mandatory mode of the standard to achieve a fast time-to-market. An experimental 7-band receiver has also been implemented and measured through wafer probes [12]. The use of 3 bands may be sufficient for current multimedia applications with communication among few devices. However, the accomplishment of the full potential of UWB technology, the implementation of very high data rate WPANs with multiple devices, demands radio implementations that can use as many bands ad possible. The allocated UWB spectrum overlaps with Unlicensed National Information Infrastructure (U-NII) band from 5.15-5.825 GHz, which is used by Wi-Fi devices. These devices can have a transmit power 26dB higher than the allowed power for a commercial UWB device. Since MB-OFDM and Wi-Fi radios target similar applications they will coexist in most environments. This prevents the use of a band group that overlaps with the U-NII band. Hence, 11 bands (4 band groups) is the maximum number that a practical MB-OFDM UWB radio can cover. For the same reason, on-chip rejection of interference in the U-NII band becomes necessary.

This chapter describes the architecture, specifications and system-level design considerations for an 11 band MB-OFDM receiver that enables very high speed wireless communication in 78% of the UWB spectrum licensed by the FCC.

3.1 Receiver architecture

Fig. 3.1 shows a block diagram of the proposed direct-conversion UWB receiver. The RF front-end is fully differential; it presents input match to 50Ω for an off-chip antenna and provides a nominal conversion gain of 35dB. The LNA includes an embedded notch-filter that provides an attenuation of 10-20dB in the range of 5.15-5.35GHz. The center frequency of the filter is guaranteed by a tuning mechanism implemented in the receiver. The 3rd order band-selection LPF is implemented by the buffer at the output of the mixer and a 2nd order Gm-C biquad. At the end of the receiver chain, a programmable gain amplifier (PGA) provides a gain in the range of 0-42dB that can be set in steps of 2-dB through a digital control. The gain, frequency response and group-delay characteristics of the baseband section are designed for a subsequent 1Gs/s ADC. The DC-offset is cancelled at the output of the mixer a passive RC HPF with a cut-off frequency of around 5MHz. Since the first (lower frequency) sub-carriers of the OFDM symbol are pilot tones that do not carry any information [9], the spectral content suppressed by the HPF does not result in any performance degradation.

The fast-hopping frequency synthesizer included in this receiver generates 11 frequency tones according to the band plan proposed in [13]. Nevertheless, the presented receiver chain is compatible with any other band plan that uses bands of 528MHz in the range of 3-10GHz such as the one from the MB-OFDM standard [9].

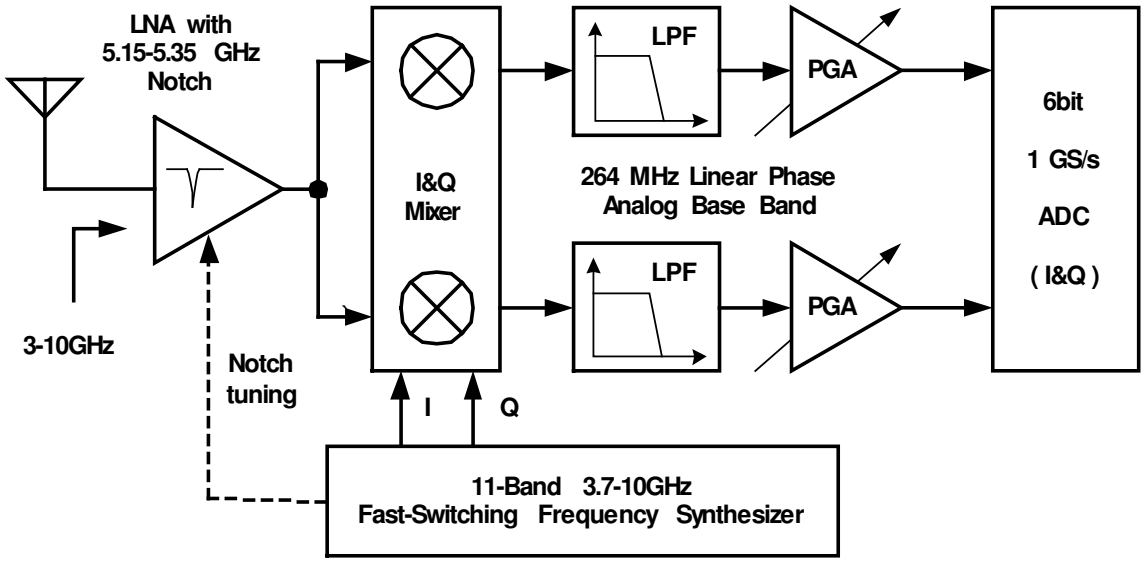


Fig. 3.1 Proposed direct conversion MB-UWB receiver architecture

3.2 Frequency band plan and synthesizer architecture

3.2.1 Choice of frequency band plan

The frequency band plan proposed in the MB-OFDM standard [9] is shown in Fig. 3.2. Each band in any band group is 528 MHz away from its adjacent band. According to the standard, when two UWB devices communicate they do so using the three (or two) adjacent frequencies of a band group. This implies that the synthesizer needs to hop very fast only between the frequencies of a particular band group. Due to the extremely fast hopping time required (9.5ns), a conventional PLL-based frequency synthesizer is not a feasible option. A relatively simple solution for the synthesis of these frequencies is to generate a reference tone for each band group and the adjacent frequencies through an up or down-conversion by 528 MHz. In this way, for the generation of any band

frequency in a given band group, the 528 MHz tone always needs to be available in addition to the corresponding reference tone.

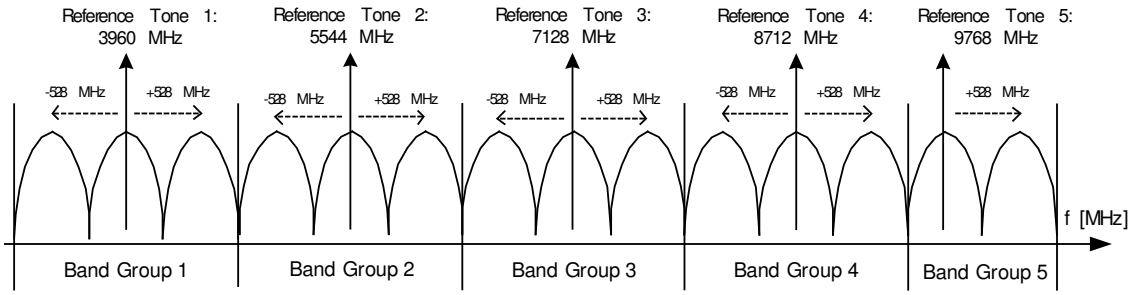


Fig. 3.2 Frequency band plan from the MB-OFDM UWB standard

A practical implementation for this frequency generation approach involves a PLL based architecture where the output frequency of the PLL is fixed and the reference tones in the different band groups and the 528 MHz tone are generated (either directly or indirectly) from the frequencies generated in the process of deriving the PLL reference frequency from the VCO output, namely auxiliary frequencies. The division ratio and the dividers used in the PLL implementation determine the specific auxiliary frequencies available. Based on this strategy, a synthesizer architecture for the generation of the frequencies in band groups 1, 3, 4 and 5 is proposed in [13] (band group 2 is avoided due to the overlap with the U-NII band as explained before). This architecture involves several mixers and requires dedicated band pass filtering for the suppression of spurious

tones. The relationship between the frequency band plan and the synthesizer architecture is further investigated to obtain an efficient synthesizer solution.

Assuming that a divide by 2 and a divide by 3 circuits serve as the basic cells in the division loop of a PLL, a frequency tree diagram that shows the different possible VCO frequencies that can result in a 528 MHz tone by successive division by 2, 3 or both. This is shown in Fig. 3.3. The tree also shows the different auxiliary frequencies generated in the PLL during the process of generation of the 528 MHz tone. The reference frequency of the PLL could be further derived from the 528 MHz.

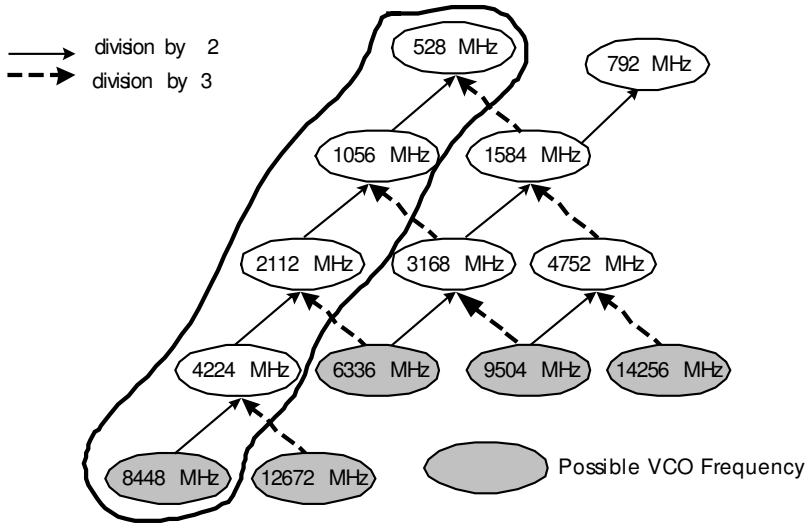


Fig. 3.3 Frequency tree diagram

In order to further reduce the number of mixers and filters to generate the required frequencies, a branch in the frequency tree can be selected such that most of the

reference tones are directly generated in the divider chain (path from the selected VCO frequency to the 528 MHz tone). Starting from the band plan depicted in Fig. 3.2, by moving the first three bands in band group 1 by 264 MHz to the higher side of the frequency spectrum and moving the band groups 3, 4 and 5 by 264 MHz to the lower side of the spectrum the frequency plan in Fig. 3.4 is obtained.

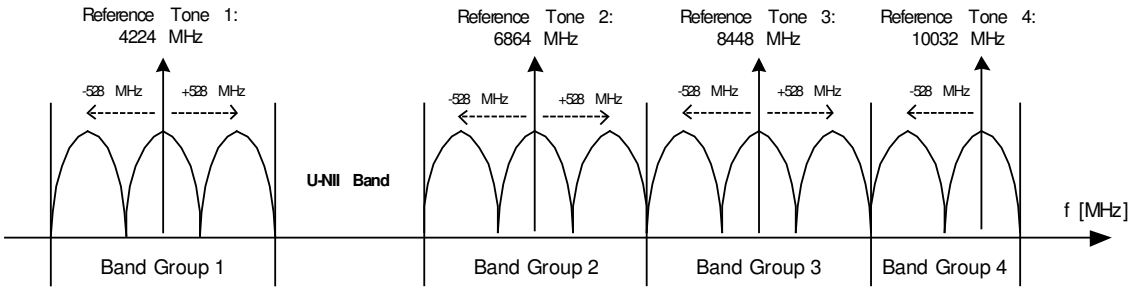


Fig. 3.4 Frequency plan for the proposed MB-OFDM UWB receiver

In this modified band plan, which is proposed in [13], two of the reference tones (8448 MHz and 4224 MHz) are generated in the divider chain of the PLL, which completely eliminates the need of any multiple frequency output mixer for the generation of any reference frequency. The corresponding set of auxiliary frequencies for the modified band plan is enclosed with a solid line in the frequency tree of Fig. 3.3. It is important to mention that this proposed modification in the band plan overlaps with the radio astronomy bands in Japan, however, it does not introduce any overlap with the U-NII band in the United States.

3.2.2 Frequency synthesizer architecture

Fig. 3.5 presents a block diagram of the employed fast-switching frequency synthesizer; it is derived from the band plan, and the frequency tree diagram presented in section 3.21. This compact and effective UWB synthesizer solution uses only divide by two circuits, single sideband (SSB) quadrature up/down converters and multiplexers to generate the 11 frequencies in quadrature from a single frequency source. The generation of frequencies in the proposed architecture relies on the fact that the fast band switching occurs between the bands within a particular band group. The principle of operation involves generating a reference tone f in every band group and then obtaining the sidebands $f \pm 528$ MHz by SSB mixing. Accuracy of intermediate quadrature signals required for SSB mixing is ensured by the usage of only divide-by-2 circuits. Harmonics and sidebands are attenuated using intermediate low pass filtering of the divided signals and minimizing quadrature imbalance in the layout. The use of intermediate band pass filters is avoided to reduce the area and the complexity since these filters normally require the use of inductors and on-chip tuning mechanism. The synthesizer also provides a tone at 5280MHz to serve as a test tone for the notch circuit in the LNA as it will be described in section 4.1. This test tone is generated by mixing 4224MHz with 1056MHz in a SSB mixer, which is not shown for simplicity.

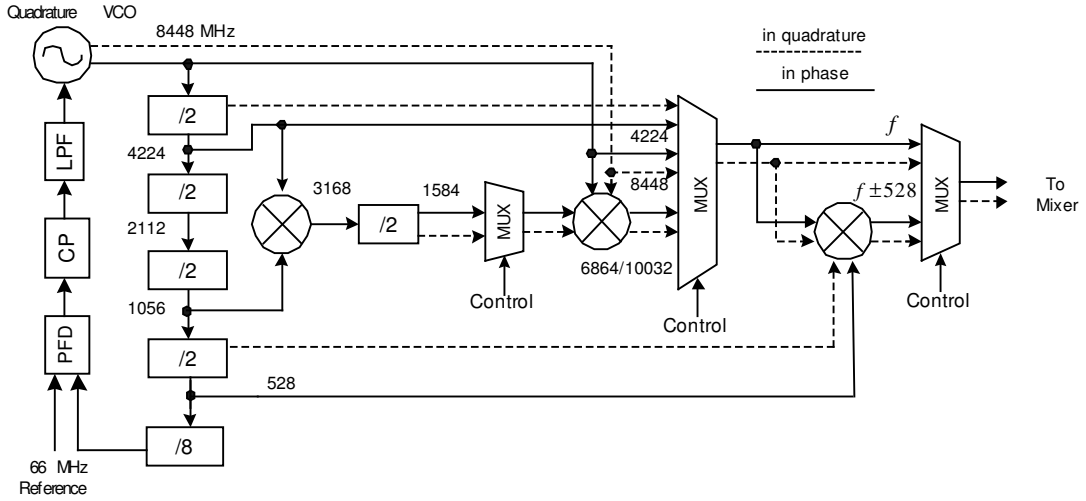


Fig. 3.5 UWB frequency synthesizer architecture

3.3 Receiver specifications

The overall procedure to map the standard requirements into specifications for the receiver and its building blocks is illustrated by the flow diagram in Fig. 3.6. As it can be observed, this is not a linear process. Even though some of the most important top-level specifications can be derived directly from the standard, the assignment of the specifications for the individual building blocks is an iterative procedure that takes place throughout the design process. The next subsections describe how the different specifications for the receiver were obtained making use of diverse resources such as mathematical analysis, BER system level simulations, computations using MATLAB, analysis of implementation trade-offs, etc.

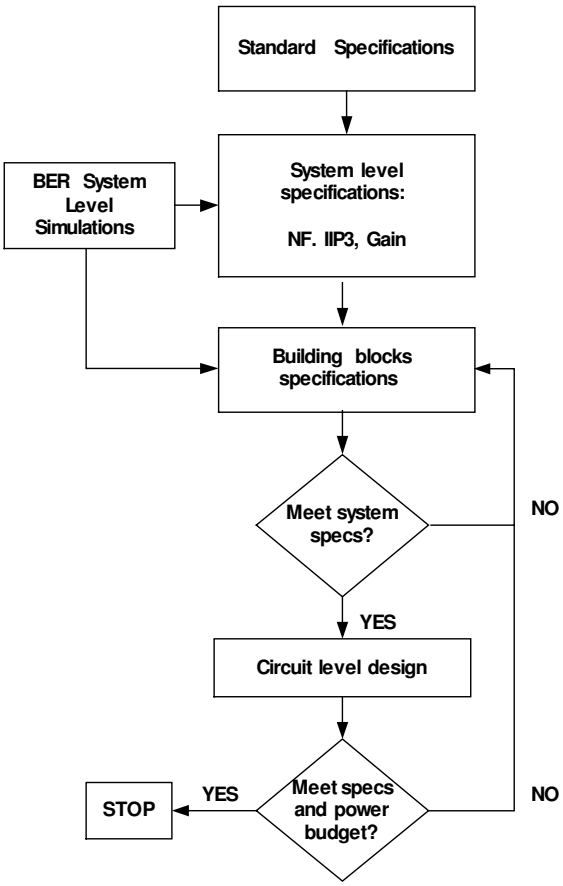


Fig. 3.6 System-level design procedure

System-level simulations were performed to analyze the effect of different receiver characteristics and non-idealities on the bit-error-rate (BER) performance of the receiver. These results are employed to determine the receiver and building blocks specifications as described in Fig. 3.6. A conceptual description of the macromodel built in SystemVue for the BER simulations is presented in Fig. 3.7. The model uses the OFDM symbol parameters described in [9] for a 480Mb/s data transmission (highest rate) over an additive white Gaussian noise (AWGN) channel. An uncoded quadrature phase-shift keying (QPSK) constellation is considered for the individual sub-carriers. For a packet

error rate of 8% with a 1024 byte packet, the target BER when using a coding rate R = 3/4 is 10^{-5}, which corresponds to an un-coded BER of approximately 10^{-2}. The next subsections describe the system-level design considerations for each section of the receiver.

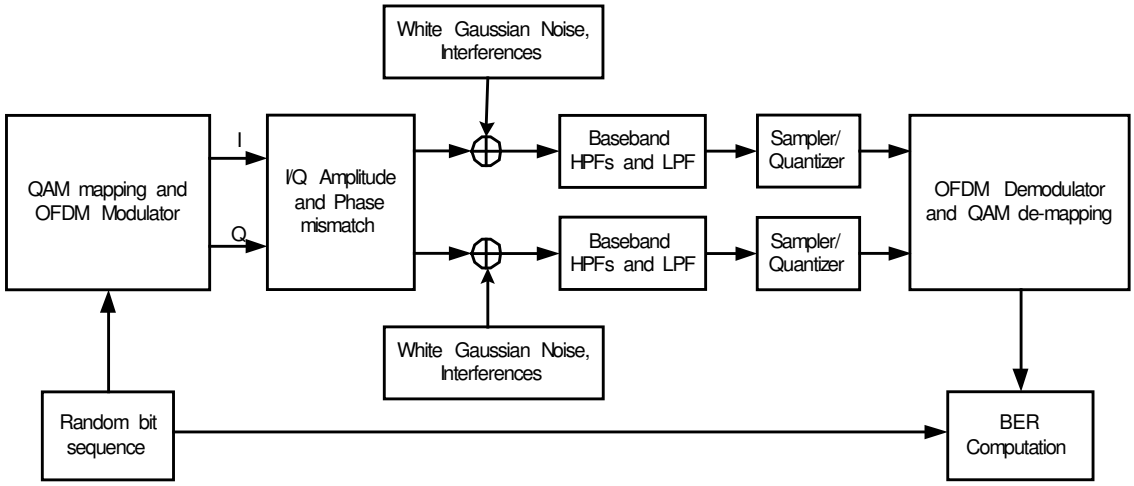


Fig. 3.7 Conceptual description of the employed system-level simulation model

3.3.1 Receiver gain, linearity and noise figure

The MB-OFDM standard specifies a sensitivity of –70.4dBm for the highest data rate of 480MB/s over AWGN. Considering the coding gain, a NF of about 9 is required for the receiver. In order to account for degradation in the demodulator sensitivity due to non-idealities such as I/Q imbalance, finite ADC quantization, down-converted peer interference due to spurs from the synthesizer, etc. a margin of 3dB is added to set the NF specification for the receiver as 6dB. In order to deliver an amplitude of 500mV

peak-to-peak to the input of the ADC (approximately equivalent to 2dBm in 50Ω) a receiver gain of 68dB is required.

The input match and frequency response characteristics of the LNA limit its gain to 15dB. In order to relax the NF requirements from the baseband LPF, the down-conversion mixer gain is set 20dB for an overall conversion gain of 35dB. The LPF provides 0dB of gain across the passband. The maximum gain from the PGA is set to 42dB (9 dB higher than required for a total receiver gain of 68dB) to account for gain variations in the front-end across the UWB spectrum and in order to support the lower sensitivity levels required at lower data rates.

In receiver design, the overall linearity specifications are usually derived from the standard requirements related to adjacent channel interference. The MB-OFDM UWB standard does not include any specific interference rejection scenario. It has been left to IC manufacturers to define their own interference rejection characteristics to create a factor of difference among different UWB products. In general, in comparison to commonly used wireless standards for cell phone and WPAN applications, the linearity (in the sense of interference robustness) specifications of a UWB radio are expected to be relaxed due to the lower transmitted power and also due to the fact that very high data rate UWB networks are not expected to have a few number of devices, at least in the first few years of the use of this technology.

Considering that the maximum transmitted power of a UWB device is –10dBm and that the path loss at 0.1m of distance is approximately 25dB (for carrier frequencies in band group 1), it is estimated that an input 1dB compression of –25dBm (corresponding

to an IIP3 of about –15dBm) is appropriate for the receiver. This takes into account that an off-chip band select filter and the on-chip notch filter provide sufficient attenuation to narrow band interferences from other standards.

Appendix A details the MATLAB code employed to compute the overall receiver specifications from the specifications of each building block. Table 3.1 presents a summary of the most important specifications for each building block of the receiver. As discussed before, these specifications are assigned after taking into account the feedback from circuit-level simulation results in different aspects such as the power consumption and area that it takes to achieve a certain performance.

Table 3.1 Major specifications per building block

Parameter	LNA	Mixer and 1st pole	2nd order LPF	PGA
Maximum gain	15	20	0	42
NF	3	16	36	25
IIP3	-9	5	18	12
Attenuation at 792MHz	0	5	20	3

With these specifications the total maximum receiver gain is 72dB, the total receiver NF is 6.3dB, the out-of-band (at 792MHz offset) receiver IIP3 for a 0dB PGA gain is –13dBm, the total in-band group delay variation is 0.6ns and the total adjacent band (starting at a 792MHz offset) is greater than 25dB. Figs. 3.8 and 3.9 show the resultant SNR behavior across the receiver chain for the proposed specifications.

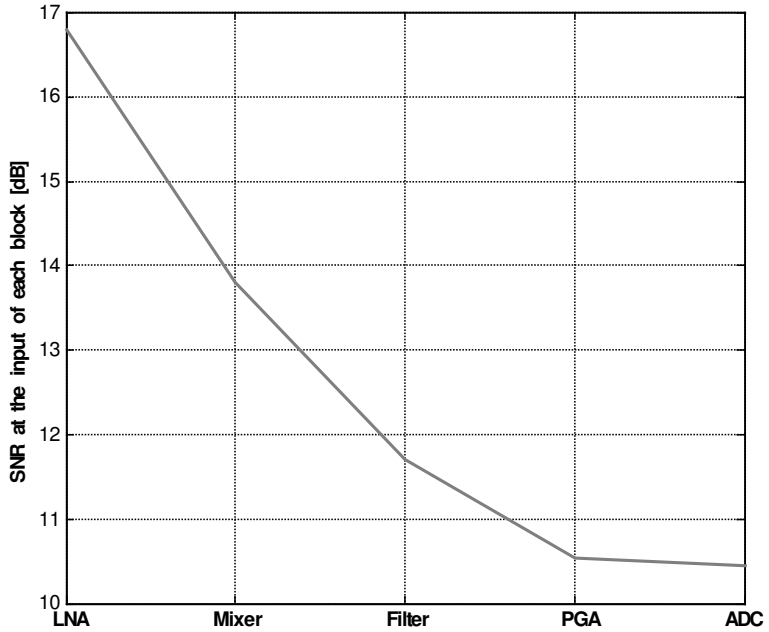


Fig. 3.8 SNR at different stages of the receiver

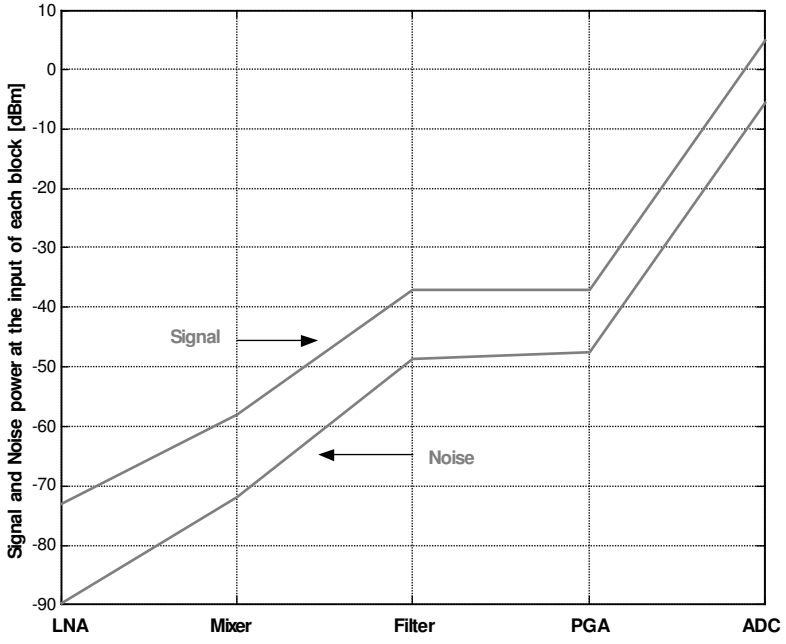


Fig. 3.9 Power of the received signal and noise at different stages of the receiver

3.3.2 Trade-off between ADC sampling rate and LPF attenuation

The use of OFDM modulation in a wideband communication system provides significant advantages such as spectral efficiency and robustness to frequency selective channels and narrow-band interferers. However, due to the multi-path characteristics of an in-door channel, the individual sub-carriers from the OFDM symbol may experience different delays, resulting in the loss of orthogonality among them and BER degradation. To counteract this effect, the symbol duration is extended for a period of time known as the cyclic prefix. In the MB-OFDM standard, the total symbol duration is 312.5ns including a cyclic prefix extension of 60.6ns (listed as prefix length in Table 2.6). The in-band group delay variation across the analog portion of the radio receiver, consumes a portion of the cyclic prefix and hence reduces the overall system robustness against multi-path.

Current MB-OFDM UWB receivers [10-12] employ high order (>=5) and relatively sharp baseband filters to implement all of the adjacent channel rejection in the analog domain. This is necessary if the ADC has a sampling rate of 500Hz. The implementation of high order analog filters for the required signal bandwidth (aprox. 264MHz) has the disadvantages of introducing a relatively large in-band group delay variation, large area if a passive implementation is used [12], and increased noise and power for an active implementation. In contrast, if a 1GS/s ADC follows the receiver, the 2X over-sampling ratio allows the implementation of linear phase filtering in the digital domain. In this scenario, the required attenuation by the analog filter is relaxed allowing an implementation with insignificant group delay variations. Hence, at the expense of

power in the ADC, the overall robustness of the system against multi-path and peer interference is enhanced. This LPF and ADC combination is chosen in the proposed system.

The LPF specifications are chosen to provide sufficient attenuation to the alternate band (1056MHz away from the band of interest) that transforms into an interferer due to the aliasing from the ADC sampling. A 3rd order linear phase Bessel filter achieves a group delay variation of less than 0.3ns (5% of the cyclic prefix) and attenuates the alternate band by more than 30dB. Another 0.3ns of group delay variation are allocated for the rest of the receiver chain to achieve a total variation of 0.6ns, which is approximately 10% of the cyclic prefix.

BER simulations show that a 4-bit quantization (including 5dB of clipping in the peak to average ratio) to the OFDM signal at 480MB/s introduces a loss in sensitivity of only 0.1dB. Therefore, to account for possible signal variations a 6 bit 1GS/s ADC with 4-5 ENOB up to 500MHz is suitable for the MB-OFDM UWB system. To clarify this trade-off in the increase of the ADC sample rate, it is worth mentioning that a recently reported 6-bit ADC in standard digital CMOS technology consumes 90mW at 600MS/s and 160mW at 1.2GS/s [14].

3.3.3 Impact of I&Q mismatch

In an OFDM system, the amplitude and phase imbalance between the I and Q channels transform the received time-domain vector **r** into a corrupted vector $\mathbf{r}_{iq}$ which

consists of a scaled version of the original vector combined with a term proportional to its complex conjugate $\mathbf{r}^*$. This transformation can be written as [15]:

$$\mathbf{r}_{iq} = \alpha \cdot \mathbf{r} + \beta \cdot \mathbf{r}^* \tag{3.1}$$

where α and β are complex constants which depend on the amount of IQ imbalance. This alteration on the received symbols can have a significant impact on the system performance. The effect of a phase mismatch in the quadrature LO signal on the BER vs. SNR performance of the receiver was evaluated considering the system characteristics outlined at the beginning of this section and using a model built in SystemView. Simulation results for un-coded data over an AWGN channel showed that the degradation in the sensitivity is 0.6 dB for 5° of mismatch. This degradation can be reduced with the use of coding and compensation techniques [15].

3.3.4 Effect of frequency synthesizer phase noise

The phase noise from the local oscillator in an OFDM receiver has two different effects on the received symbols. It introduces a phase rotation of the same magnitude in all of the sub-carriers and creates inter-carrier interference (ICI) [16]. The first undesired effect is eliminated by introducing pilot carriers with a known phase, in addition to the information carriers. On the other hand, phase noise produces ICI in a similar way as adjacent-channel interference in narrow band systems. Assuming that the data symbols on the different sub-carriers are independent, the ICI may be treated as Gaussian noise. The power spectral density (PSD) of a locked PLL can be modeled by a Lorenzian spectrum described by:

$$\left|\Phi(f)\right|^2 = \frac{1}{\pi} \cdot \frac{\beta}{f^2 + \beta^2} \tag{3.2}$$

where β is the 3 dB bandwidth of the PSD which has a normalized total power of 0 dB. The degradation (D in dB) in the SNR of the received sub-carriers due to the phase noise of the local oscillator in an OFDM system can be approximated as [17]:

$$D \cong \frac{11}{6\ln 10} \cdot 4\pi \cdot \beta \cdot T \cdot \frac{E_s}{N_o} \tag{3.3}$$

where T is the OFDM symbol length in seconds (without the cyclic extension), β defines the Lorenzian spectrum described above and Es/No is the desired SNR for the received symbols (in a linear scale, not in dB). For this system, 1/T=4.1254 MHz and the Es/No for the target coded BER of 10^{-5} is 5.89 (7.7 dB). For D=0.1 dB and the mentioned parameters, β can be computed with (3.2) and is 7.7 KHz. The corresponding Lorenzian spectrum has a power of –86.5 dBc/Hz @ 1 MHz.

This phase noise specification is to be met by the LO signal at the input of the down-conversion mixer. As shown in Fig. 3.5, the employed UWB synthesizer architecture involves a source PLL followed by a series of up and down conversions that will affect the phase noise of the source oscillation. For this reason, the phase noise specification provided in the previous paragraph does not directly correspond to the phase noise at the output of the employed source PLL. General guidelines for the analysis of phase noise in component cascades are provided in [18]. For this application, the most relevant components for phase noise degradation are the mixers employed in the frequency translation operations across the synthesizer architecture. For a given offset

frequency Δf , the phase noise at the output of a mixer can be estimated as the rms sum of the individual input noise contributions. Hence, given phase noise relative power densities $L_1\{\Delta f\}$ and $L_2\{\Delta f\}$ (in dBc/Hz) at the input of each port of the mixer, the output phase noise can be expressed as:

$$L\{\Delta f\} = 10 \cdot \log\left(10^{\left(\frac{L_1\{\Delta f\}}{10}\right)} + 10^{\left(\frac{L_2\{\Delta f\}}{10}\right)}\right) \tag{3.4}$$

Even though in this case the two signals are indirectly derived from the same reference, their noise can be assumed in general to be uncorrelated since the delay from the PLL to each input of a given mixer would be significantly different. The size of an integrated implementation would be small in comparison to the wavelengths involved but the frequency dividers and the poles in the signal path introduce a delay. As it can be noted from Fig. 3.5, there is at least 1 frequency divider between the inputs of each mixer. The gain or loss of the mixer amplifies or attenuates all of the frequency components around the frequency of operation by the same amount and hence does not affect the phase noise. Moreover, due to the relatively large amplitude (tens of mV) of the signals within the synthesizer, the contribution of the thermal noise of the mixers to the phase noise is negligible.

Equation 3.4 is used to find the VCO phase noise specification for the most critical case, which is the generation of the tones in band groups 2 and 4. These frequencies involved the operation of three cascaded mixers. In the worst-case assumption that the there is no change in the phase noise from the input to the output of the frequency

dividers it is found that a VCO phase noise of at least –92.5dBc at 1MHz offset is required to comply with the overall LO phase noise specification of –86.5dBc at 1MHz.

3.3.5 Effect of spurious tones from the frequency synthesizer

As in other communication systems, the most harmful spurious components of a LO signal are those at an offset equal to multiples of the frequency spacing between adjacent bands (528 MHz in this case), since they directly down-convert the transmission of a peer device on top of the signal of interest. In order to gain understanding on the impact of unwanted tones from the synthesizer, the effect of an uncorrelated down-converted peer interferer in the BER performance of a MB-OFDM UWB receiver is evaluated through the baseband equivalent model depicted in Fig. 3.7. BER curves are obtained for different relative power levels of the interferer signal and the performance degradation is measured for each of them. Fig. 3.10 summarizes these results, it shows the degradation (increase) in the minimum signal to noise ratio (SNRmin) required at the demodulator input to meet the target BER (10^{-2}) as a function to the signal to interference ratio (SIR). For a given spur performance and interference scenario, Fig. 3.10 can be employed to estimate the degradation in the receiver sensitivity. For example, a spur at -15dBc that down-converts a peer interferer of the same power level as the signal of interest results in SIR of 15dB and 1dB degradation in SNRmin. However, bit interleaving and forward error correction techniques employed in a complete MB-OFDM radio [2] are expected to further reduce the SNR degradation due to interference from peer UWB devices.

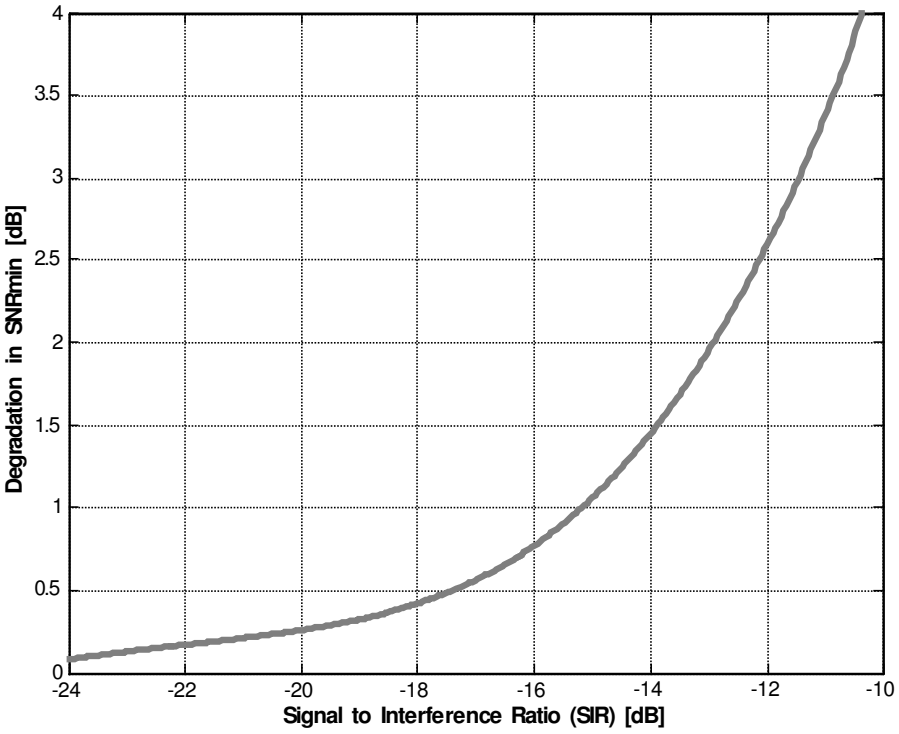


Fig. 3.10 Degradation in the minimum required SNR with SIR at baseband

CHAPTER IV

3-10GHZ MB-OFDM UWB RECEIVER: RF-FRONT END IMPLEMENTATION

A key component of a wireless receiver is the RF Front-End (LNA and Down-Conversion Mixer), which amplifies the incoming signal from the antenna and down-converts the desired channel to base-band (0-264MHz in this case). The design of the front-end for the proposed UWB receiver presents several challenges which demand the development of circuit techniques different from the ones employed in conventional narrow-band receivers.

The UWB LNA must attain input impedance matching in the entire band of operation (3 to 10 GHz). This specification is particularly difficult to meet if a commercial (relatively cheap) package is used for the IC because its parasitics become significant and may dominate the input impedance, especially at such high frequencies. Another major issue in the design of this LNA is its ability to reject the strong interferers in the 5-6 GHz band. These interferers can be even 20 dB stronger than the desired information, forcing to increase LNA linearity unless those interferers are suppressed. To use an off-chip notch filter to reject the signals in the 5-6 GHz band is possible, but an expensive option. To have a notch filter embedded in the LNA is a desirable feature.

For the design of the down-conversion mixer, circuit topologies that are inherently broadband exist. However, to attain a relatively constant performance of the bandwidth of interest with affordable power consumption is a significant challenge. The conversion

gain and NF of the down-converter depend strongly on the signal amplitude of the local oscillator (LO). In this receiver, the buffer between the frequency synthesizer and the down-conversion mixer must assure the amplitude of the LO signal over the entire 3-10GHz and therefore becomes a critical component of the front-end implementation. In addition, this buffer is also a multiplexer that performs the fast (<9ns) commutation between the tones generated by the frequency synthesizer.

Fig. 4.1 presents a block diagram of the implemented RF front-end. It consists of the UWB LNA with an embedded notch filter, a quadrature down-conversion mixer and a multiplexer/buffer that is the interface between the synthesizer and the mixer. The buffers that couple the output of the mixer with the linear phase 2nd order active LPF (analog baseband) implement the first pole of the overall 3rd order LPF. The next subsections detail the design of each component of this UWB RF front-end.

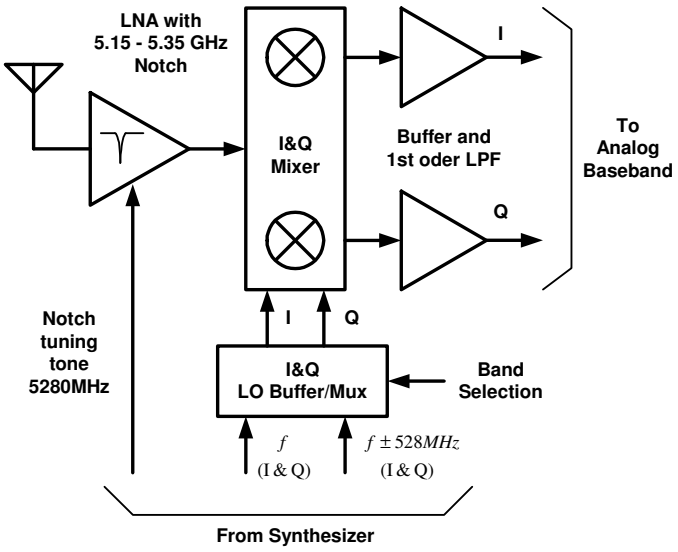
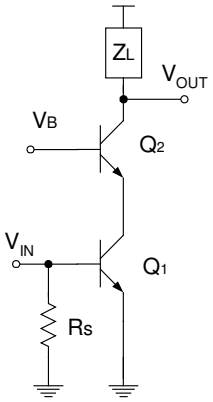


Fig. 4.1 Block diagram of the RF front-end for the UWB receiver

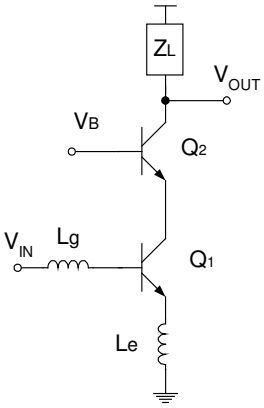
4.1 UWB LNA design

4.1.1 Overview of LNA design techniques

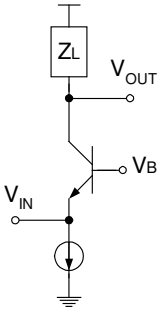
Figure 4.2 shows the 4 most common configurations for an LNA. Bipolar transistors are employed in the schematics but corresponding MOS configurations exist as well and the same general trade-offs apply. Topology (b) is the only one inherently narrowband because its input matching characteristic is narrowband. The other topologies are usually made narrowband with the use of a resonant tank as load (Z_L) or wideband with a resistive or inductive-resistive load. The fundamental design trade-offs between these topologies are described in Table 4.1. For a giving operating frequency, bipolar implementations will require a smaller bias current than the their MOS counterparts due to their higher f_T and g_m. On the other hand, at the expense of higher power, MOS versions may achieve a better linearity and noise performance.



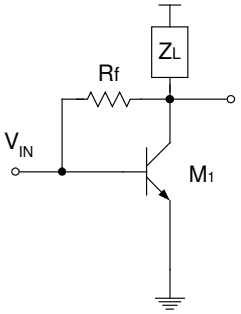
(a) Common emitter (CE) with input resistance



(b) CE with inductive degeneration



(c) Common base (CB)



(d) CE with feedback

Fig. 4.2. Common LNA topologies

Table 4.1 Summary of properties for common LNA topologies

	a	b	c	d
Z_{IN}	Rs	$\frac{1}{sC_\pi}+s(L_g+L_e)+\frac{g_m L_e}{C_\pi}$	$\frac{1}{g_m}$	$\frac{R_f+Z_L}{g_m \cdot Z_L}$
NF	worst	best	moderate	moderate
Linearity	Poor. May be improved with degeneration at the expense of power.	Improved due to the degeneration inductance.	Poor	Improved due to the feedback resistance
Advantages	Stable and broadband input matching.	Real part of the input impedance is created through a noiseless element (L_g). Superior NF makes it the most commonly used narrow-band LNA.	Broadband input matching. To a first order, its gain and noise performance are independent of frequency, which makes it a better choice in high GHz range.	Broadband input matching with moderate NF. Popular choice for optical comm.
Disadvantages	Large NF prevents its practical use.	Increased area due to the need of on-chip inductors. Performance depends on the Q of the inductors and it degrades as the operation frequency approaches f_T	Low gain and reduced design flexibility: I_C is fixed by the matching requirement.	For a given bias current, gain is reduced with respect to a and b.

An additional option for the implementation of a wideband LNA is to use a distributed configuration. Distributed amplifiers are fundamentally different from the topologies discussed above (which in the context of distributed circuits are generically label as ‘lumped’ circuits). A basic distributed RF amplifier is shown in Fig. 4.3; it consists of two transmission lines and multiple transistors providing gain through multiple signal paths. Termination resistors are employed to prevent reflections. The key feature of a distributed amplifier is to make an efficient use of the multiple available

parallel signal paths. In contrast, lumped amplifiers may have at most 2 signal paths, and their performance is based on the cascading (serial connection) of various stages.

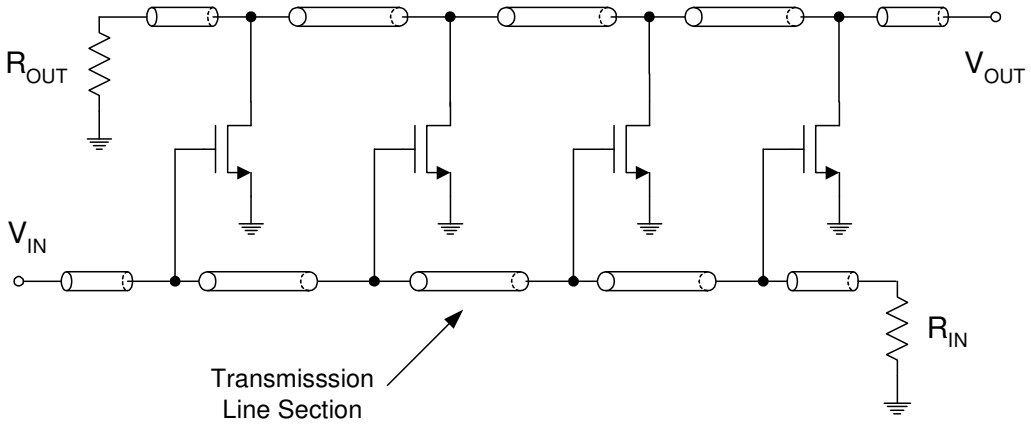


Fig. 4.3. Distributed amplifier with CMOS transistors

A distributed amplifier can provide an overall gain larger than 1 even for frequencies where each transistor has a gain of less than 1. This is because the individual gain contributions of the transistors add on the output line. In addition, the parasitic capacitances of the transistors are absorbed into the transmission lines, further improving the bandwidth requirements. Another important feature of distributed circuits, which can be an advantage for certain applications, is that they are broadband in nature. The physical size of a distributed amplifier does not have to be comparable to the wavelength of the involved signals: The transmission lines may be replaced with lumped inductors, which, together with the parasitic capacitances of the transistors from an LC ladder low

pass filter. In this case the frequency response is limited by the Q factor of the employed inductors.

Distributed amplifiers employ a large silicon area and show a relatively poor NF performance. For these reasons, despite their clear advantage in frequency response, distributed amplifiers have not replaced their lumped counterparts in practical applications.

4.1.2 Existing UWB LNA solutions

Table 4.2 presents a summary of the recently reported LNAs for UWB applications in the range of 3-10GHz including their basic topology and the most important performance metrics. None of these LNAs have been demonstrated in a package and they do not include in-band filtering for interference rejection.

Table 4.2 Current state of the art in 3-10GHz UWB LNA implementations

Reference	Topology	Gain [dB]	NF [dB]	Power [mW]	Technology
[19]	Common source LC matching network	9.3	<9.5	9	0.18µm CMOS
[20]	Common emitter LC matching network	21	<4.2	30	0.18µm SiGe BiCMOS
[21]	Resistive feedback	21.3	<4.5	42.5	0.25µm SiGe BiCMOS
[22]	Common base	22	<3.9	13.2	0.25µm SiGe BiCMOS
[23]	Differential	10	<6.5	5.4	0.35µm SiGe BiCMOS

In addition to the above-mentioned stand alone amplifiers, two RF front-ends (including LNA and down-conversion mixer) for 3-10GHz UWB applications have been reported recently [24-25] and they have been characterized in a package. [24] has a poor match performance in the upper half of the band. [25] does not show measurement results for the input match. This front-end also includes an in-band notch filter, however, since no tuning scheme was incorporated, the measured response is significantly shifted. So far there is no reported 3-10GHz UWB LNA solution that has either accomplished adequate input match in a commercial package or a tunable in-band notch filter.

4.1.3 Proposed UWB LNA with embedded notch filter

The circuit schematic of the proposed UWB LNA is shown in Fig. 4.4 A fully-differential topology is chosen mainly because it allows to have an inductance degeneration value (which is very important to accomplish the broadband matching) independent from the package + bonding wire inductance. The design of the input matching network is described in Section 4.1.4. The cascode transistors Q2 provide reverse isolation and reduce the Miller capacitance at the base of Q1 (which degrades the matching performance). The base of Q2 is tied to VDD so that Q1 has the largest possible collector to base voltage which optimizes the f_T performance of the bipolar transistor.

NMOS transistors are employed for the tail current because of they reduced VDS requirement in comparison to the VCE of a Bipolar to remain in saturation. In addition, biasing through NMOS transistors results in considerable power savings since the

external bias current (Ibias) can be made a fraction (one tenth in this case) of the desired bias current. A relatively flat gain over the band of interest is accomplished through an R-L load. It is important to note that the loading parasitics of the mixer are taken into account in the design and simulations.

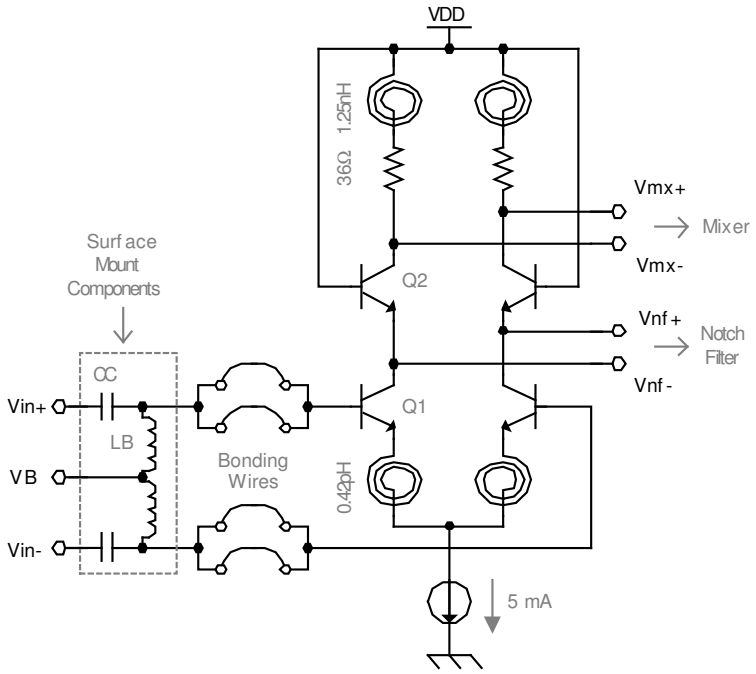


Fig. 4.4 Circuit schematic of the LNA core

The embedded notch filter is formed by a Q-enhanced LC series circuit that presents a small impedance at its resonant frequency. In this way, at the frequency of interest for suppression, the output current from the input differential pair is absorbed by the notch filter instead of being converted into voltage at the load. To include a resonant

impedance at the output of a differential pair has been employed in the past for image rejection [26]. In a narrow-band amplifier, the voltage gain for frequencies above the image frequencies is not a major concern, the main objective is just to reject the image band. In this case, however, the notch should placed in-band and the gain after the interference frequency (in this case for channel 2 starting at 6.3GHz) should not be affected. This requirement sets a trade-off between the maximum achievable interference rejection and the ripple in the bands of interest. Thus, the notch should have the highest Q possible. The employed Q-enhanced series LC filter is shown in Fig. 4.5

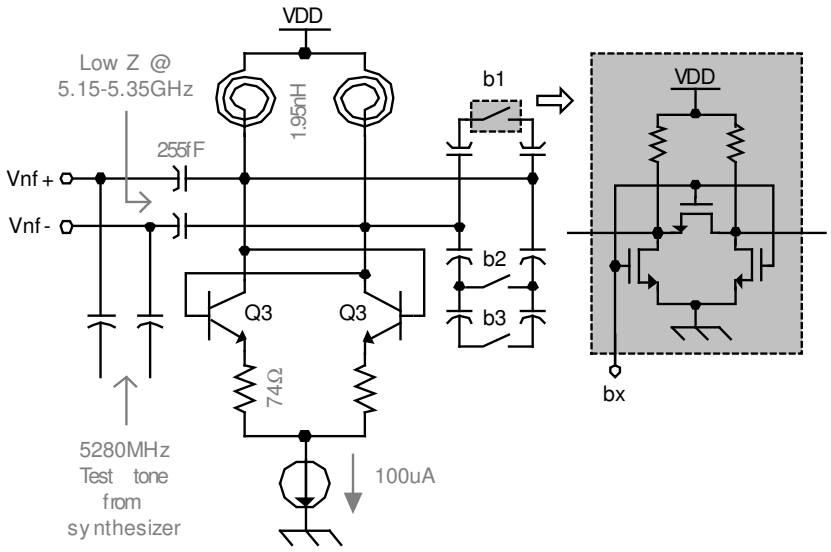


Fig. 4.5 Circuit schematic of the embedded notch filter

A bank of discrete capacitors is included to provide tuning to the filter and compensate for possible process variations. A bank of discrete capacitors is included to

provide tuning to the filter and compensate for possible process variations. The tuning mechanism is described in Fig. 4.6. In tuning mode, a 5280MHz test tone (provided by the frequency synthesizer) is applied at the input of the series LC circuit with the LO signal set at 4752MHz. At baseband, the down-converted test tone at 528MHz shows the smallest amplitude for the correct control word.

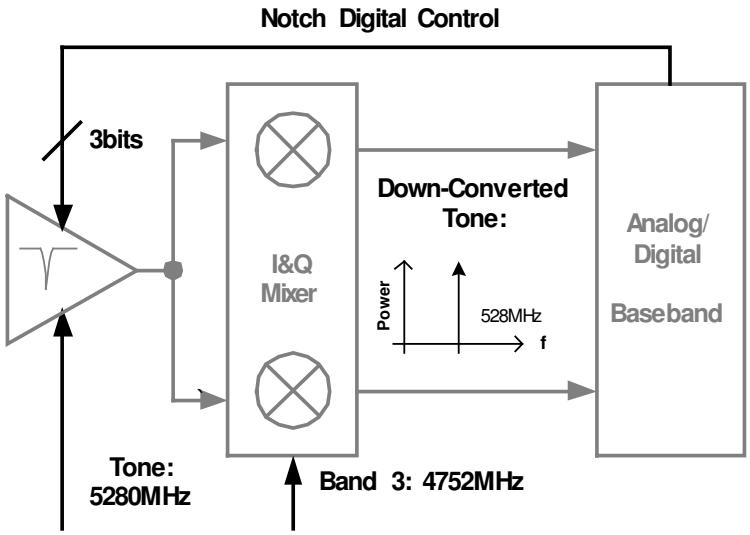


Fig. 4.6 Conceptual description of the proposed tuning mechanism

Fig. 4.7 presents the post-layout simulation results of the proposed UWB LNA with notch filter taking into account the load of the down-conversion mixer. In the band of interest, the voltage gain is higher than 15dB and the NF less than 3dB. The IIP3 is higher than –8dB. From corner simulations, after tuning the notch filter, the expected attenuation in the range of 5.15-5.35GHz is 10dB.

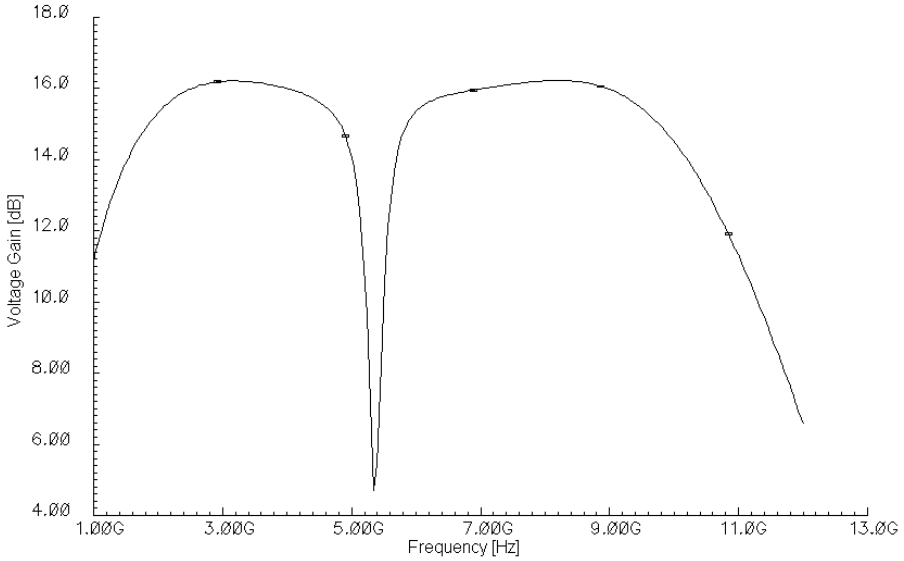


Fig. 4.7 Post-layout simulation results of the LNA voltage gain

4.1.4 Input matching network analysis

The input matching network of the proposed LNA is an LC bandpass filter structure formed by an inductively degenerated differential pair, double bonding wires and the off-chip biasing components as shown in the circuit schematic of Fig. 4.4. Even though the circuit is fully differential and matched to 50Ω, the matching network can be analyzed as single-ended circuit matched to 25Ω. The proposed circuit model for this analysis is presented in Fig. 4.8. The inductively degenerated bipolar transistor forms the resistive part of the termination impedance. Overall, the structure approximates a third order Chebyshev LC bandpass filter. Table 4.3 summarizes the values for the employed components. It is important to mention that LW represents the equivalent parallel inductance of two bonding wires with a length of 1.5mm each. An inductance of 1nH/mm is assumed for the bond wires.

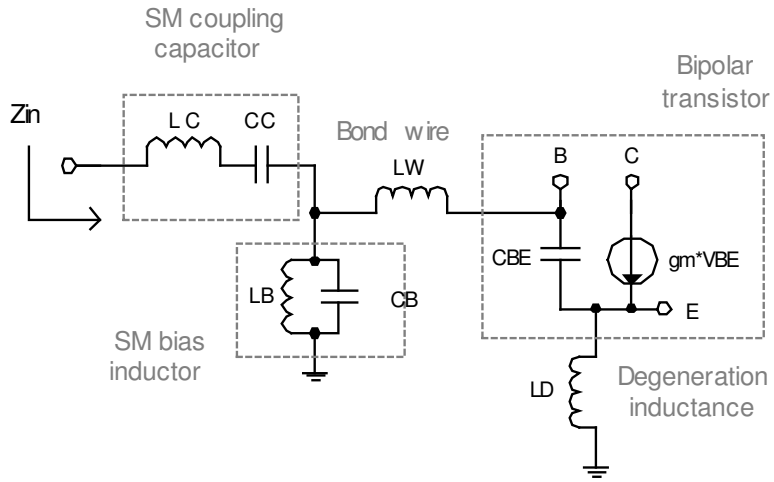


Fig. 4.8 Simplified schematic of the input LC network

Table 4.3 Components of the input matching network

Component	Value	Description
LC	1 nH	Parasitic inductance associated with the AC coupling capacitance and its PCB connections
CC	0.85 pF	Off-chip SM AC coupling capacitance
LB	1.05 nH	Off-chip SM bias inductance
CB	0.8 pF	Parasitic capacitance associated with the bias inductance and its PCB connections
LW	0.75 nH	Bond wire inductance
CBE	0.75 pF	Base to emitter capacitance of bipolar transistor
LD	400 pH	On-chip degeneration inductor
gm	80 mA/V	Transistor transconductance

The most significant factor of uncertainty during the design of the matching network was the length of the bond wires (and thus their inductance) since it depends on the final size and position of the die within the package. For this reason the matching network is

design to be as robust as possible to variations in LW. To attain the required, relatively large base to emitter capacitance, the longest possible emitter length allowed by the technology for a single transistor was employed. This length is 40µm.

Figure 4.9 shows the calculated input reflection coefficient of Zin in Fig. 4.8 with respect to 25Ω. As it can be observed, a relatively good match performance (S11<-8dB) can be achieved in the band of interest even with variations of +/- 20% in the effective inductance(length) of the bond wires.

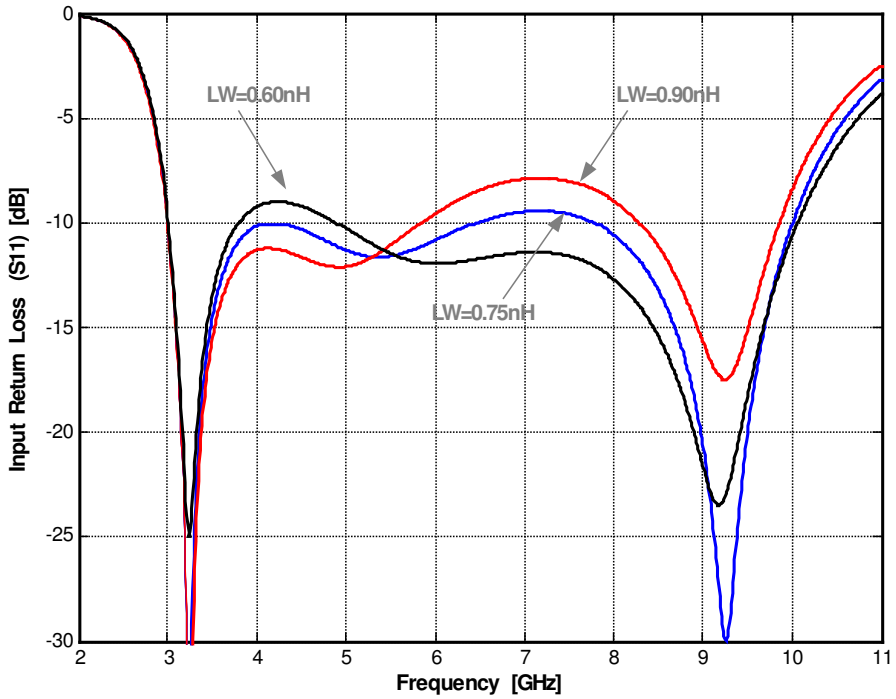


Fig. 4.9. Calculated input return loss for different bond wire inductance values

After the design with the simplified model shown in Fig. 4.8, the matching network is implemented and optimized at the schematic and post-layout levels taking into account all the additional parasitic components such as the capacitance of the bond pad and the frequency response of the on-chip degeneration inductance LD. It is worth mentioning that even though the matching network can be model reasonably well by a third order LC band pass filter structure, all the additional parasitic components make the actual network to be of a higher order. Fig. 4.10 shows the post-layout simulation results for the input return loss (S11) of the LNA (in differential mode with respect to 50Ω) in the range of 3-11GHz. The S11 parameter forms a circle around the center of the Smith chart, which is the expected behavior for a wide-band matching network.

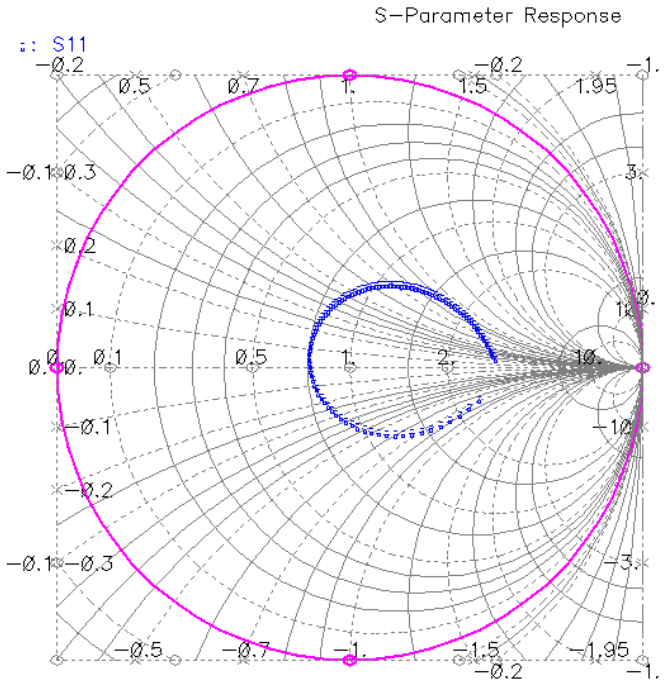


Fig. 4.10 Pos-layout simulation results for the input match on a Smith chart

4.2 UWB down-conversion mixer design

Fig. 4.11 shows the proposed quadrature down-conversion mixer for the UWB receiver. The output current of the LO switching transistors is mirrored and converted to voltage in 2Kohm resistor loads. Current steering is used in the 1:1 mirrors. This mixer topology is chosen to maximize the achievable conversion gain without compromising noise and linearity.

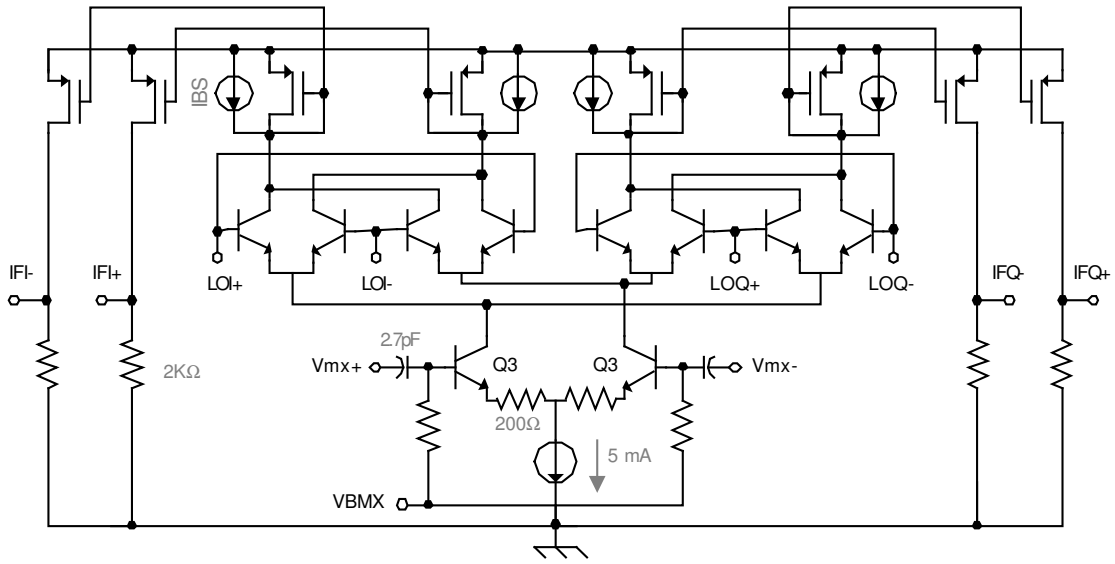


Fig. 4.11 Circuit schematic of the quadrature down-conversion mixer

Post-layout simulations for the performance of the down-conversion mixer across the band of interest are shown in Fig. 4.12. For these simulations a sinusoidal waveform of 100mV of peak differential amplitude is used to drive the LO transistors.

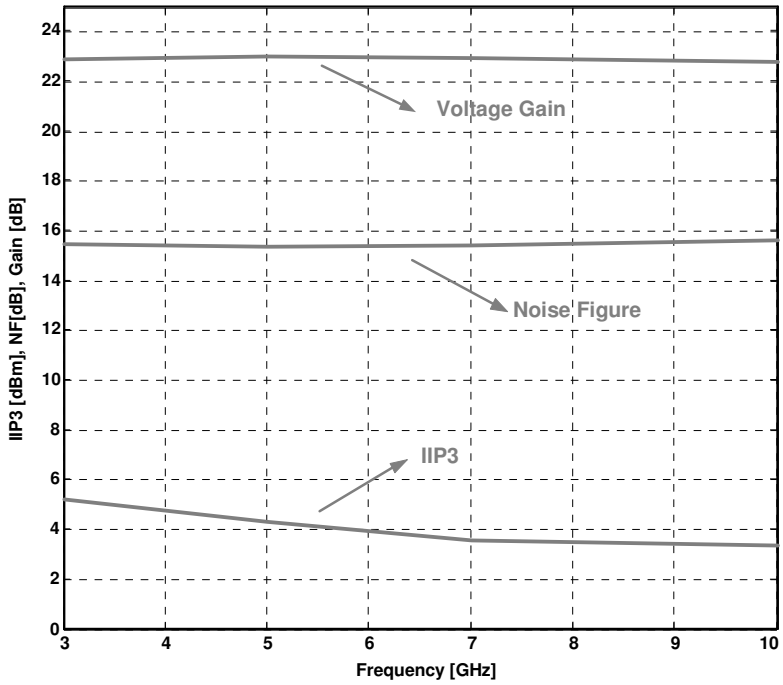


Fig. 4.12 Post-layout simulation results for the down-conversion mixer

Four, single-transistor buffers in the emitter-follower configuration are employed to couple the mixer output to the input of a second order LPF which is implemented as a second order Gm-C biquad structure. The output impedance from the buffers and the input parasitic capacitance of the filter form a low pass pole. The total frequency response of the cascaded buffer and biquad is optimized as a third order linear phase Bessel filter with a in in-band (0-264MHz) group delay variation of 0.3ns and an attenuation of approximately 25 dB at 792MHz.

4.3 Buffer-multiplexer design

As shown in Fig. 4.1, the switching between adjacent bands (which must occur in less than 9ns) at the output of the synthesizer is performed by a multiplexer that at the

same time serves as a buffer to drive the LO input of the down-conversion mixer. Fig. 4.13 shows the circuit that performs these functions for each channel (I or Q). The circuit consists of two differential pairs sharing a common load. One of the two input differential signals (Va and Vb) is connected to the output Vo while the other one is isolated. The desired signal is selected by a digital control (d0, d1). Each bipolar differential pairs in the circuit has cascode transistors to reduce feed through from the adjacent differential pair. The cascode transistors and the tail current of the differential pairs are simultaneously switched on or off through d0 and d1 to completely connect or isolate a particular differential pair to the load. The load in the final multiplexer that feeds the quadrature mixer in the RF front-end has inductive peaking to boost the signal amplitude at high frequencies.

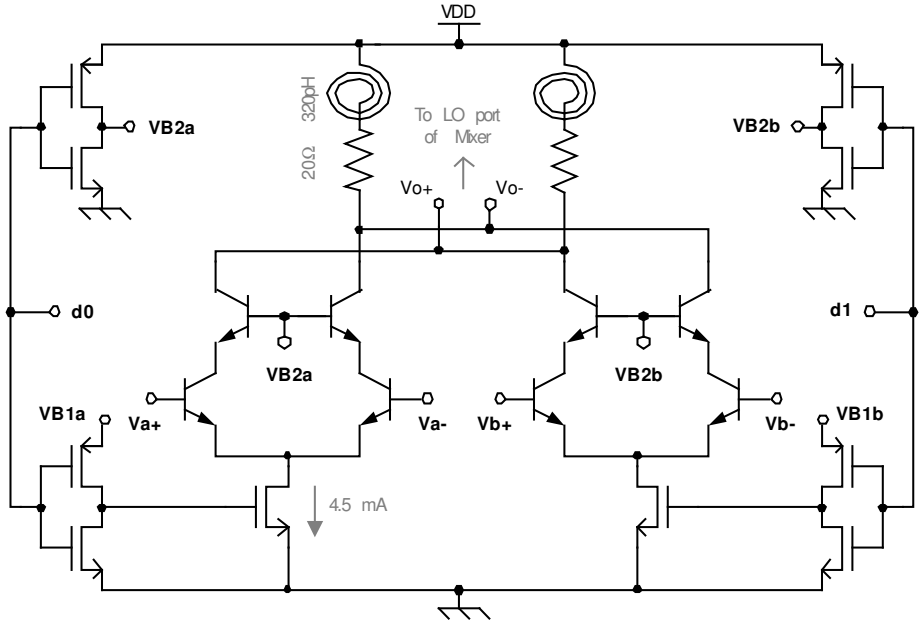


Fig. 4.13 Circuit schematic of the multiplexer/buffer

Post-layout simulations of the frequency synthesizer show a decreasing output amplitude as the frequency of the generated band increases. This is due to the lowpass nature of the employed final up-conversion mixer. To compensate for this loss of amplitude, which may seriously degrade the NF of the mixer, the multiplexer/buffer is designed to have a high-pass characteristic within the band of interest. Fig. 4.14 shows the post-layout simulation results for the AC voltage gain response of the buffer connected to the down-conversion mixer.

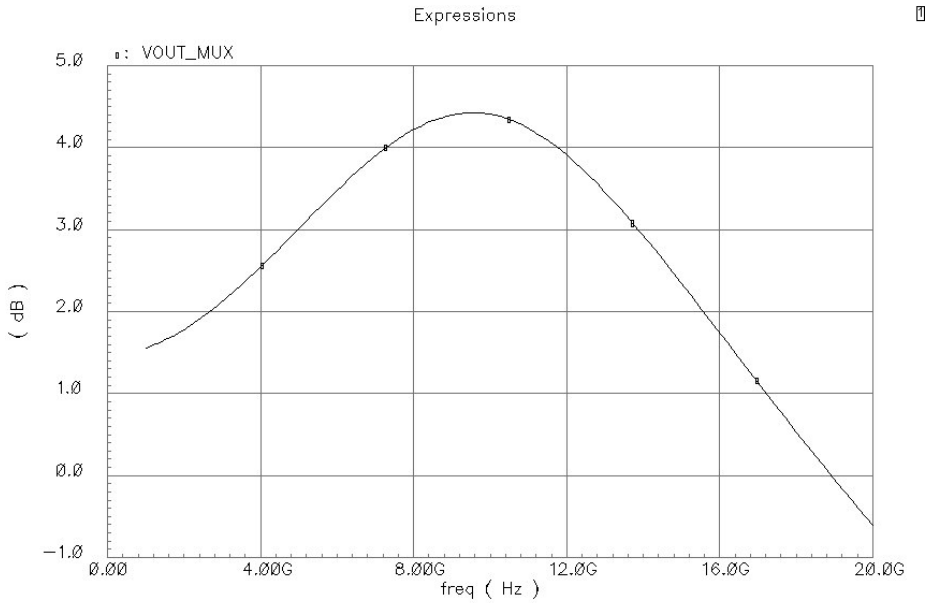


Fig. 4.14 Voltage gain of the multiplexer/buffer (post-layout simulation results)

The switching performance of the multiplexer is also evaluated. As shown in Fig. 4.15, the input signal to the LO port of the down-conversion mixer can change from one frequency to another in less than 5ns.

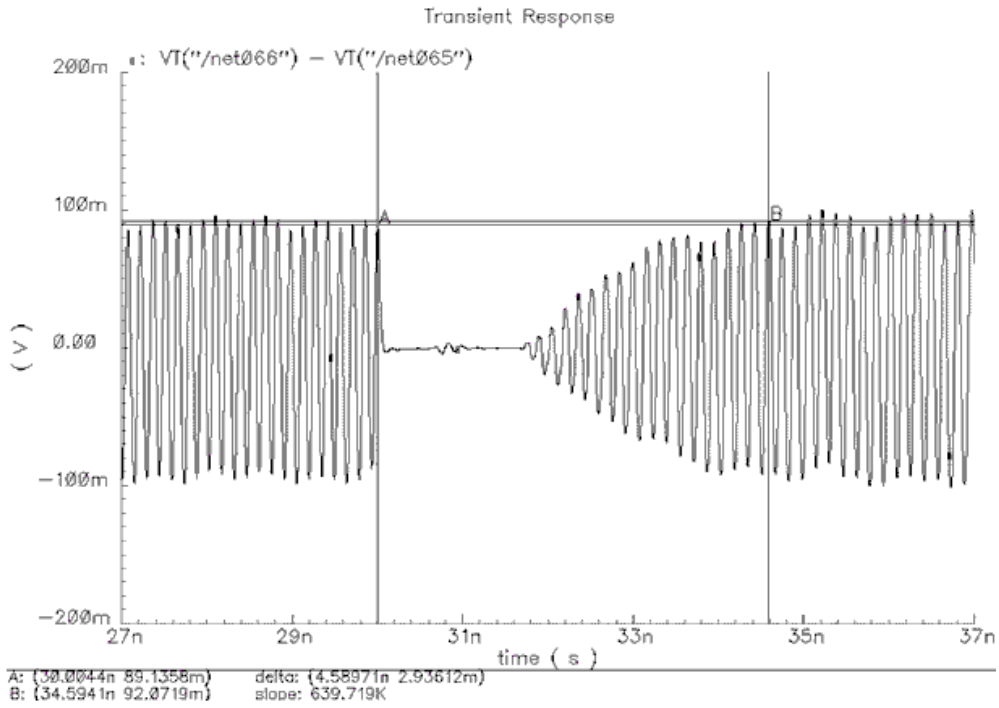


Fig. 4.15 Switching speed of the multiplexer (post-layout simulation results)

4.4 Front-end integration

The complete layout of the RF front-end in the receiver is shown in Fig. 4.16. As it can be observed, the distance between the LNA and the mixer and between the buffer and mixer is made as short as possible.

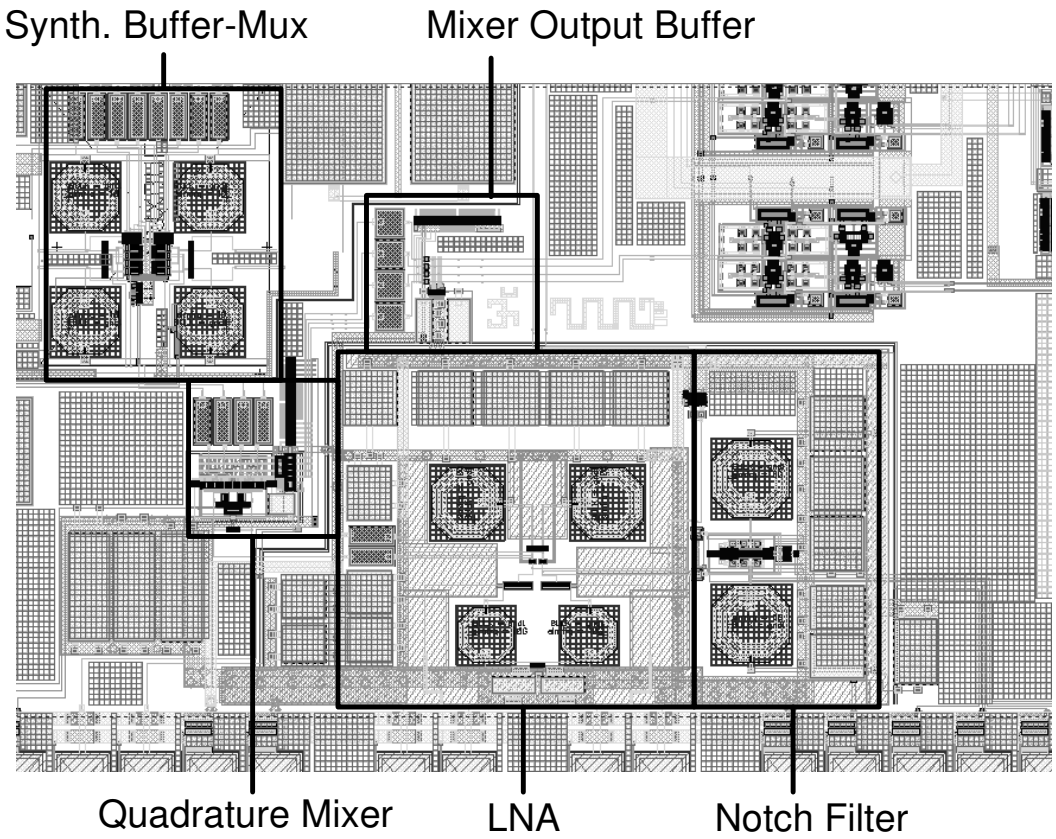


Fig. 4.16 Layout of the complete front-end in the UWB receiver

The design of each building block is re-optimized after the parasitics of the connections (which depend on the final distance between adjacent blocks) are extracted. Fig. 4.17 shows the post-layout simulation results of the NF of the buffer-mixer integration at 10GHz. Curve a represents the original NF performance when the mixer is driven directly by a sinusoidal waveform with a peak differential amplitude of 100mV. Curve b, c and d represent the NF performance when the mixer is driven by the buffer and a sinusoidal signal with a peak differential amplitude of 70mV, 90mV and 100mv, respectively is applied at the input of the buffer.

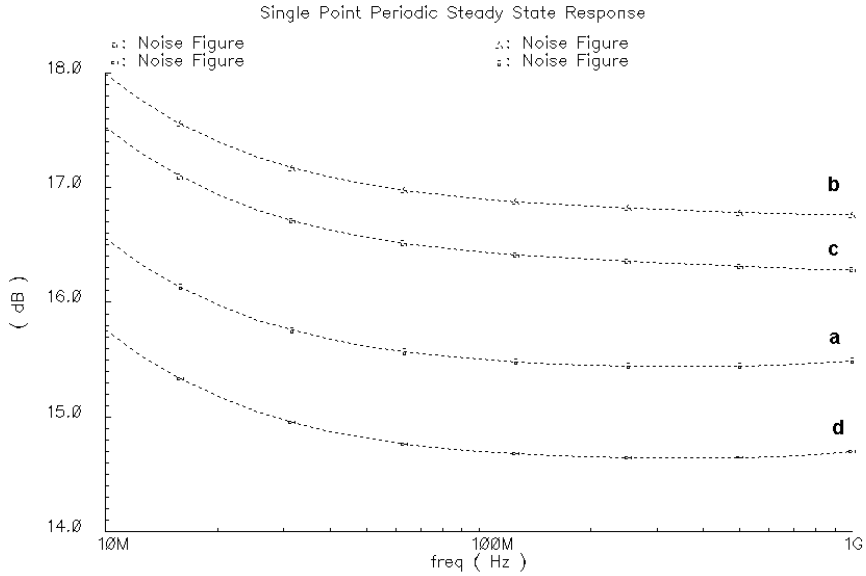


Fig. 4.17 Mixer noise figure as a function of the LO amplitude

CHAPTER V

3-10GHZ MB-OFDM UWB RECEIVER: EXPERIMENTAL RESULTS

Two different IC prototypes were implemented to evaluate the performance of the proposed circuits. Both were fabricated using IBM 0.25μm BiCMOS technology through the MOSIS service. The first IC consist of the most critical RF circuits (LNA, frequency synthesizer and quadrature VCO) for the evaluation of their individual performance. The second IC is the 3-10GHz MB-OFDM UWB receiver system integrating the RF front-end, frequency synthesizer, basband filter and PGA.

5.1 Experimental results for the stand-alone LNA with embedded notch filter

Fig. 5.1 depicts the microphotogrpah of the IC prototype with individual UWB RF circuits. This section describes the experimental results for the LNA with notch filter.

Due to the attenuation introduced by the output buffer and PCB, it is not possible to evaluate the voltage gain of the LNA and the NF that would be perceived in the integrated receiver (i.e. when the LNA is directly connected to the down-conversion mixer). The objective of this individual LNA implementation is to evaluate the input match with the QFN package and the performance of the notch filter, which are the 2 most distinctive features of the proposed design.

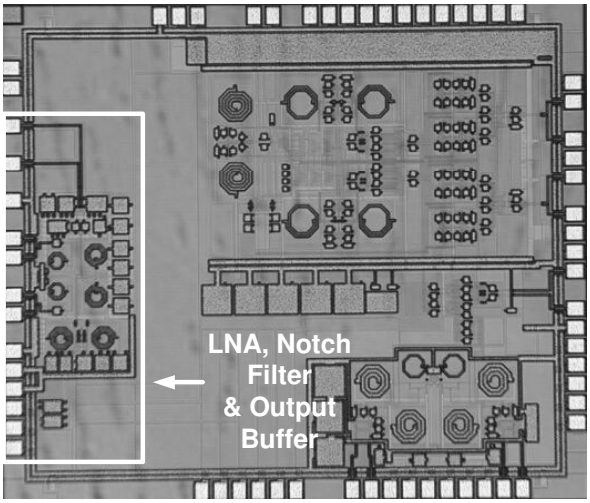


Fig. 5.1 Microphotograph of IC prototype with UWB RF Circuits

5.1.1 PCB and experimental setup

The fabricated chip, in a QFN64 package is mounted on a PCB using standard FR4 substrate. A network analyzer is employed to perform S-parameter measurements on the test fixture, Fig. 5.2 presents a block diagram of the test setup.

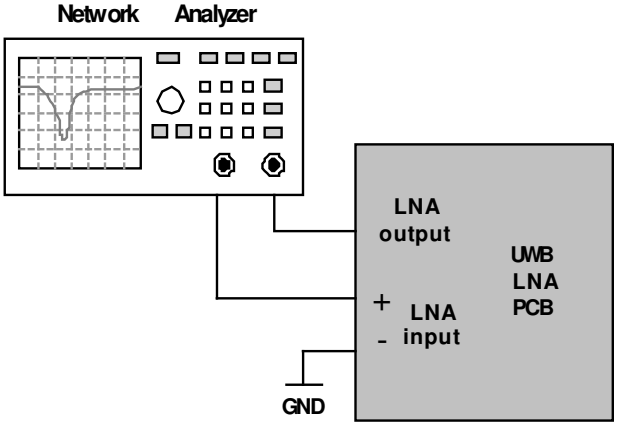


Fig. 5.2 Experimental setup for the characterization of the UWB LNA

The fabricated circuits are fully differential while the employed network analyzer supports only single-ended ports. To perform differential measurements, the use of a balun is required. Commercial baluns that operate in this frequency range show a typical attenuation of 8dB. This attenuation can significantly alter the s-parameter measurements, especially in the case of the S11 test. For this reason, it is decided to perform the measurements in a single-ended way, by connecting one of the inputs to the LNA to ground as shown in Fig. 5.2. In turn, only one of the outputs of the buffer (i.e. Vout+) is taken to the output port. The other output is AC coupled to a 50ohm load, and in this way, the buffer perceived a balanced differential load impedance. Fig. 5.3 shows a photograph of the employed PCB. Note that the trace for the input of the LNA is directly connected to the package without any external component.

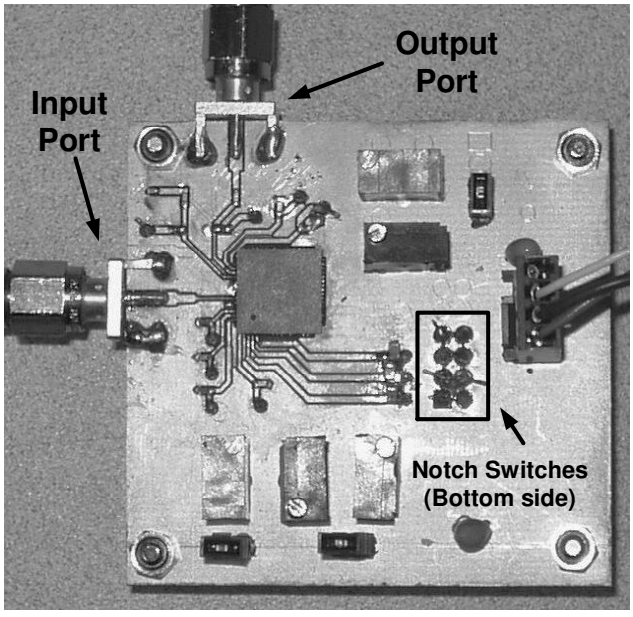


Fig. 5.3 UWB LNA test PCB photograph

5.1.2 LNA input match

For the measurement of the return loss (S11) at the input LNA, the calibration plane is placed at the point in which the package makes contact with the PCB, in this way, the effect of the input PCB trace is discarded. The purpose is to have the most accurate measurement possible of the input impedance of the LNA as seen from the package. To perform the calibration, open, short and 50ohm load conditions are set on the PCB at the point where the package terminals corresponding to the input of the LNA make contact. This is done, naturally, before the package is mounted on the PCB. Fig. 5.4 shows the measured S11. An input match of at least -10dB is attained between 3.6 and 9.6GHz, which is in good agreement with the simulation results.

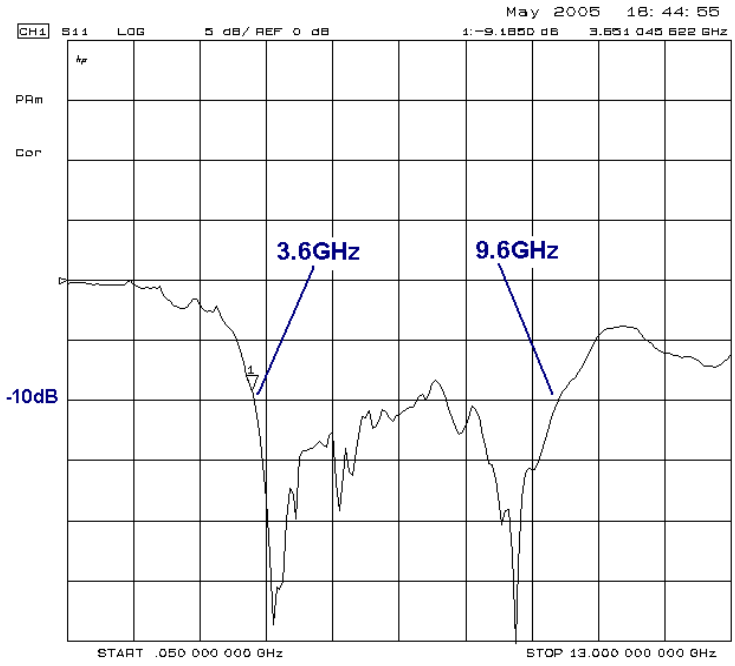


Fig. 5.4 Measured S11 of the UWB LNA

It is important to emphasize that this S11 performance is obtained without any external component. Hence, the input match of the receiver is expected to be even better since external components are used, which provide additional degrees of freedom and completes the input LC bandpass filter structure described in Section 4.1.4. The most important conclusions that are drawn from this measurement are: (1) The proposed wideband matching technique for a commercial package works as expected and (2) The employed package model is reasonably accurate for the range of frequencies considered.

5.1.3 Notch filter tuning

The measured S21 of the LNA+buffer combination mounted on the PCB, in a range of 3.5 to 11.5GHz is shown in Fig. 5.5. Even though the buffer and PCB traces for the output port introduce attenuation and variations to the frequency response, the relative attenuation introduced by the notch filter can be evaluated. From this wideband S21 measurement it can be observed that the attenuation at 5.2GHz is about 20dB with respect to the average gain in the rest of the band of interest. In addition, the S21 response does not present a significant roll-off up to 10GHz, which indicates the wideband nature of the amplifier.

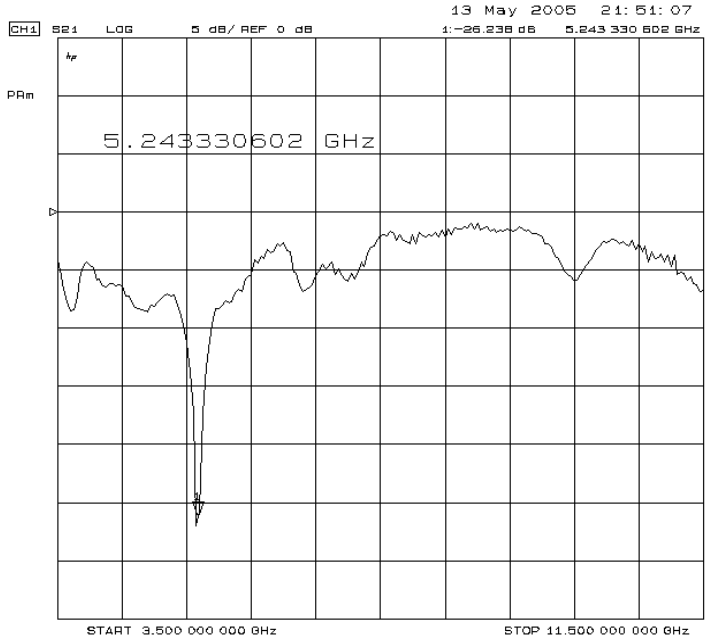


Fig. 5.5 Measured S21 response of the UWB LNA

To evaluate the proposed discrete tuning mechanism for the notch filter, S21 measurements within the tuning range of the filter are performed for different tuning settings and over-imposed in a single plot. The result of this characterization is shown in Fig. 5.6. For clarity, only 5 of the 8 different tuning conditions are shown. The relatively wideband nature of the notch and the tuning resolution (about 100MHz per step) are such that a minimum attenuation of 10dB over a given bandwidth of 200MHz (e.g. the UNII band between 5.15-5.35GHz) can be obtained.

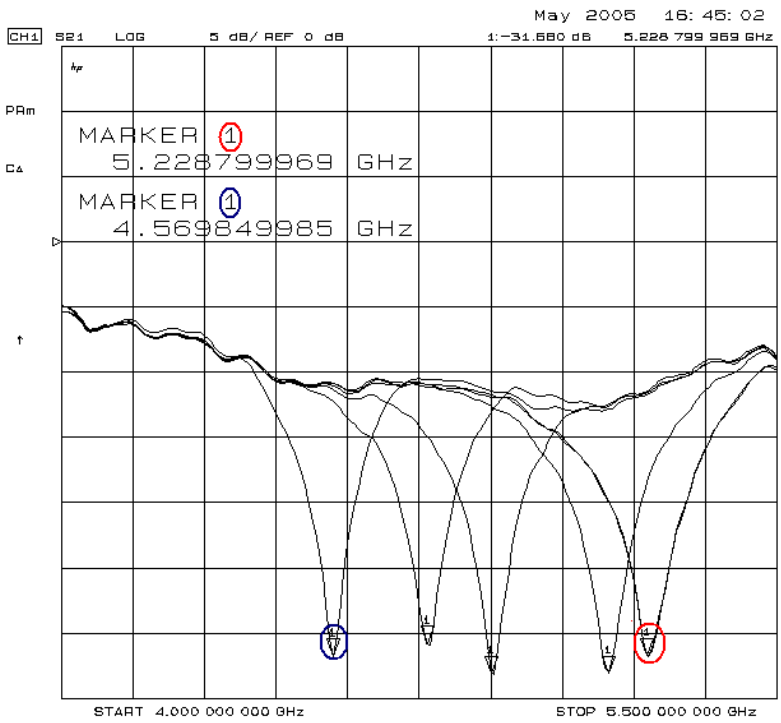


Fig. 5.6 Measured tuning range of the notch filter

Simulation results for the filter with nominal models showed a tuning range within 4.8 to 5.8GHz. However it was observed that under process corners for the employed inductors and capacitors, the tuning range could be shifted to lower frequencies. Thanks to the proposed tuning mechanism, despite process variations, the center frequency for the notch can be placed at the desired frequency.

5.2 Experimental results for the MB-OFDM UWB receiver

Fig. 5.7 shows the microphotograph of the proposed 3-10GHz UWB receiver IC. The total area of the implemented blocks is 5.6mm^2 including pads. The next subsections detail the different measurements performed on the system.

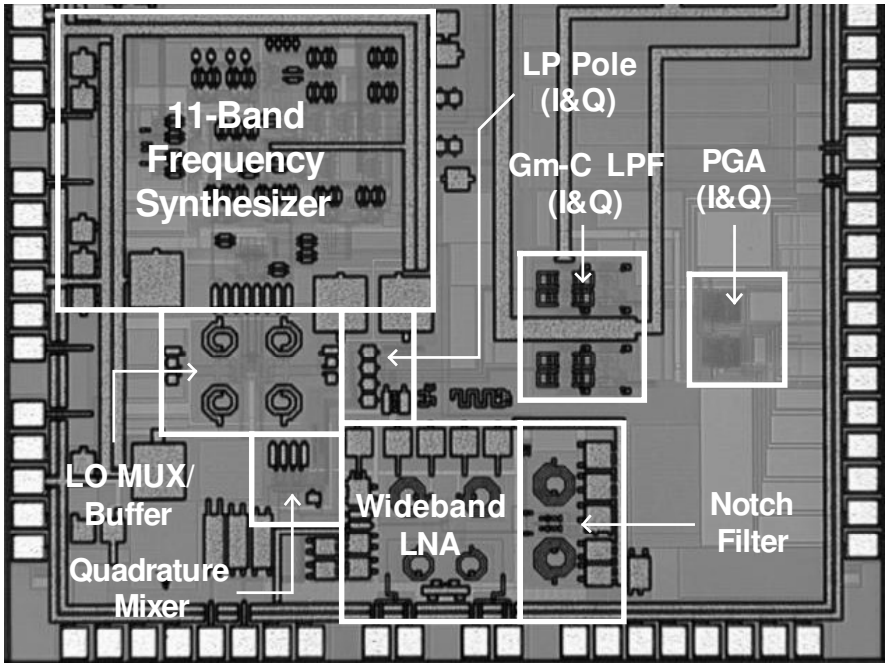


Fig. 5.7 UWB Receiver chip microphotograph

5.2.1 UWB receiver PCB design

Fig. 5.8 shows a photograph of the PCB employed for the test of the UWB receiver system. This PCB was fabricated on a standard FR-4 substrate. For the layout of the PCB, the highest priority was to set the connectors of the microwave signals (input of the frequency synthesizer at 8.448GHz and input to the receiver from 3-10GHz) as close as possible to the package. PCB traces that have a comparable order of magnitude to the wavelength of the signal of interest introduce undesired loss and make the adjustment of the matching networks more difficult. This is especially true in low-cost materials such as FR-4, which do not have an accurate impedance control.

The SM components employed for the matching networks and the biasing of the RF circuits have a 0603 or 0402 footprint and self-resonance frequencies beyond 10GHz.

SM AC filtering capacitors of 8pF (with self resonant frequency of about 11GHz) were placed as closed as possible to all of the voltage supplies and to the current biasing inputs of the RF circuits to minimize high-frequency bouncing and undesired coupling among these terminals. Vias are frequently employed across the board to assure the presence of an adequate ground plane in all areas. This is important to reduce undesired signal coupling by providing a low impedance path to ground for the EM fields. As it can be observed, ceramic baluns are employed close to BNC connectors to perform the differential to single-ended conversion of the baseband signals.

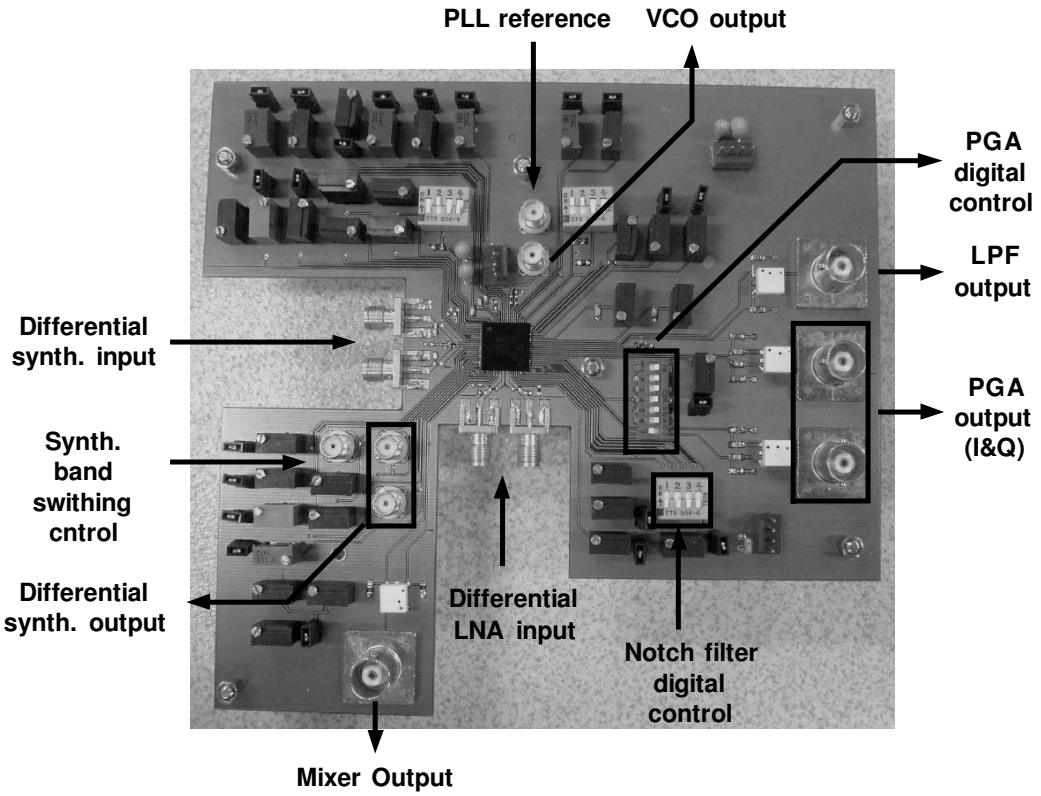


Fig. 5.8 Photograph of the PCB for the test of the UWB receiver

5.2.2 Input match measurement

As in the stand-alone LNA prototype, the input match in this case is also measured in a single-ended configuration following the same LNA input connection as shown in Fig. 5.2 The difference in this case, as it can be observed from Fig. 5.8, is that the AC coupling capacitors and bias inductors are external components and form part of the input matching network.

In the evaluation of the LNA prototype the objective was to evaluate the impedance as seen from the terminals of the package. In this case, however, the goal is to evaluate the input match as it would be seen from the location of the antenna. For this reason, in this measurement the calibration plane is left at the SMA connector and the setup (network analyzer + cables) is calibrated using the standard calibration kit from the equipment. The measured S11 response is shown in Fig. 5.9. With the exception of a small region at 6.2GHz (pointed by the measurement marker), the input match is better than –10dB from 3.5 to 11GHz. As expected, this input match performance is better than the one observed in the PCB that does not use external components. Between 7.5 and 10.5GHz approximately the input match is better than –15dB, which is better than what was expected from simulations. This can be the resulted of having bond wires shorter than expected and/or having increasing power loss in the PCB for frequencies beyond 7GHz. As it will be discussed in the next sections, the second hypothesis is supported by other measurements as well.

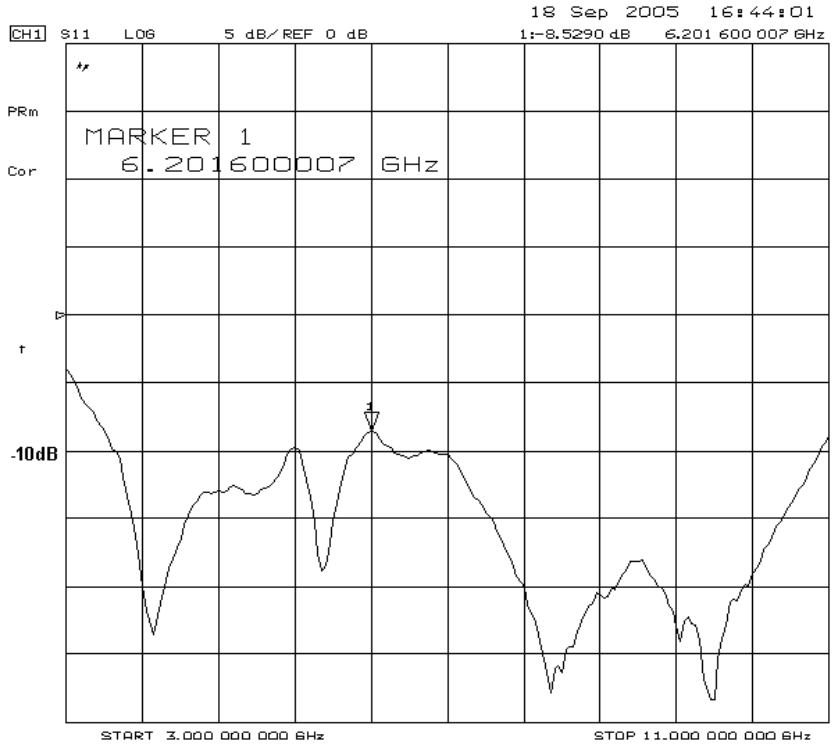


Fig. 5.9 Measured receiver input S11

5.2.3 Frequency synthesizer performance

As it can be observed form Fig. 5.8, a separate output is provided to evaluate the performance of the frequency synthesizer. The important aspects to evaluate are the capability of the synthesizer to generate the required 11 different tones, the relative power of the generated spurs and the switching speed. Fig. 5.10 describes the employed experimental setup. The 8448MHz input tone to the synthesizer as well as the input signal to the receiver are provided through a 5315A baluns from Picosecond Pulse Labs. These baluns cover a bandwidth from 200KHz to 17GHz with a loss of 8dB.

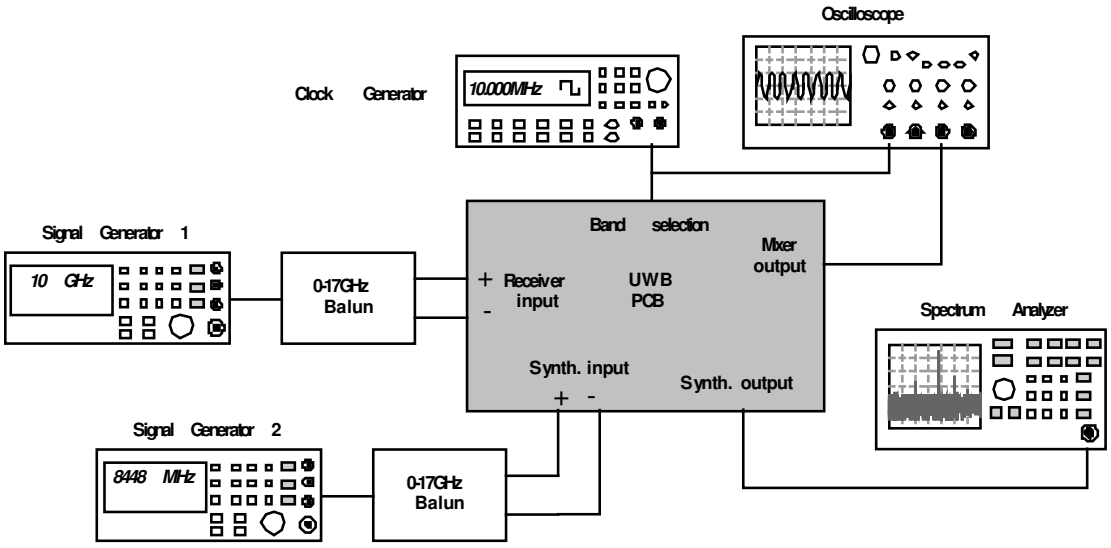


Fig. 5.10 Experimental setup for the characterization of the frequency synthesizer

It is important to mention that the impedance match at the input of the synthesizer was adjusted through the external SM components before performing the tests. The signal power at the input of the PCB is approximately 0dBm and the coupling to the synthesizer output was measured as -35dB with the IC powered off. An open collector buffer with external SM inductor as its load is used to observe the output of the synthesizer. Figure 5.11 shows the output spectrum of the synthesizer in the generation of the tone at 6864MHz. In this case, the in-band spurs are below –25dBc. In general, the in-band spurs were observed to be -20dBc for most of the bands.

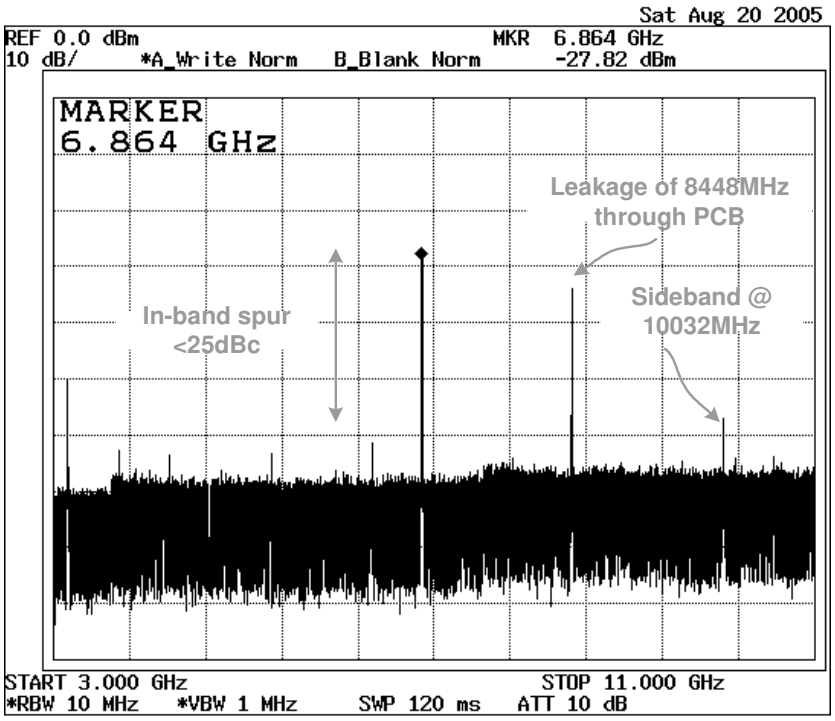


Fig. 5.11 Output spectrum of the synthesizer for the 6864 MHz tone

To evaluate the switching speed of the synthesizer between adjacent bands, the control input of the multiplexer at the output of the synthesizer is switched by applying an external clock signal. The synthesizer output is captured during the transition using a 20Gs/s oscilloscope. Fig. 5.12 shows the captured oscilloscope screen. The measured switching time is 7.3ns. The applied switching signal is over-imposed as a reference. Note that both, the switch signal and the output of the synthesizer, are delayed through the package and the PCB and that the effective switching is expected to be even faster inside the receiver.

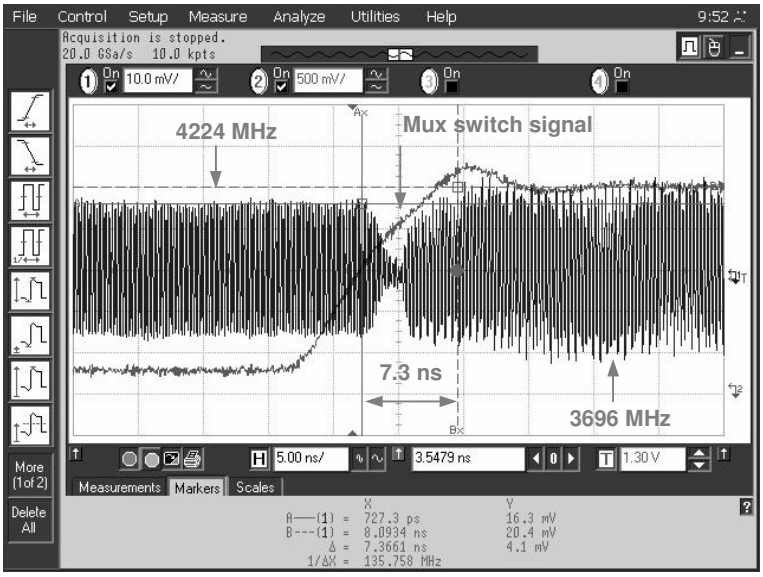


Fig. 5.12 Measured switching behavior of the synthesizer

While the switching speed of the synthesizer is important, a more meaningful performance metric is how fast the commutation between two adjacent bands is perceived at the baseband of the receiver. To perform this test the RF input to the LNA was fixed at 4.124GHz and the LO frequency was switched from 4.224GHz to 3.696GHz resulting in a baseband output switching from 100MHz to 428MHz respectively. Both the switching signal and the output of the down-conversion mixer are observed by the high-speed sampling oscilloscope as described in Fig. 5.10. As shown in Fig. 5.13, the effective switching time as seen at the output of the mixer is less than 7ns in both directions of the transition between adjacent bands.

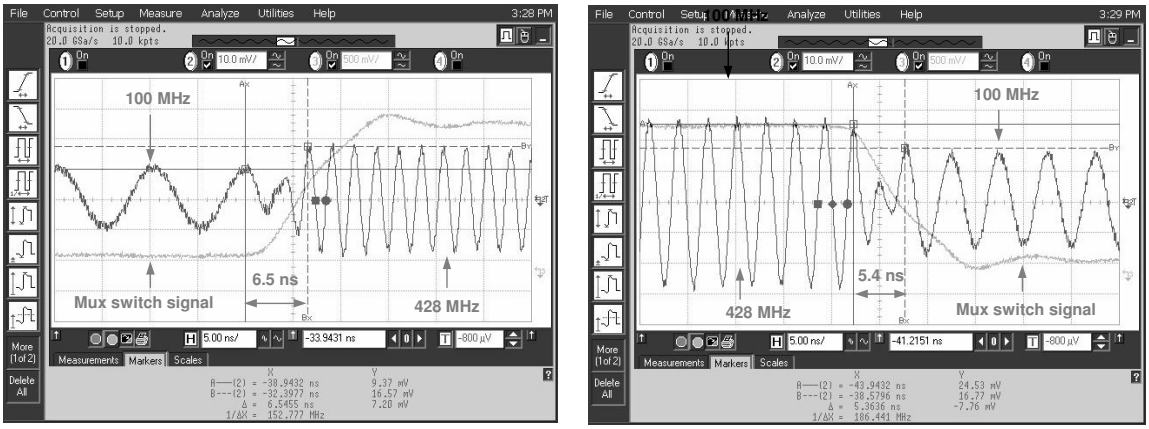


Fig. 5.13 Switching time of the receiver as seen from the mixer output

5.2.4 Frequency response of the receiver

The frequency response of the entire receiver chain is measured by sweeping the frequency of RF input of the LNA and observing the output of the receiver at a fixed LO frequency. Fig. 5.14 illustrates this test setup, which is also employed to perform the measurements of gain, linearity and noise figure on the receiver.

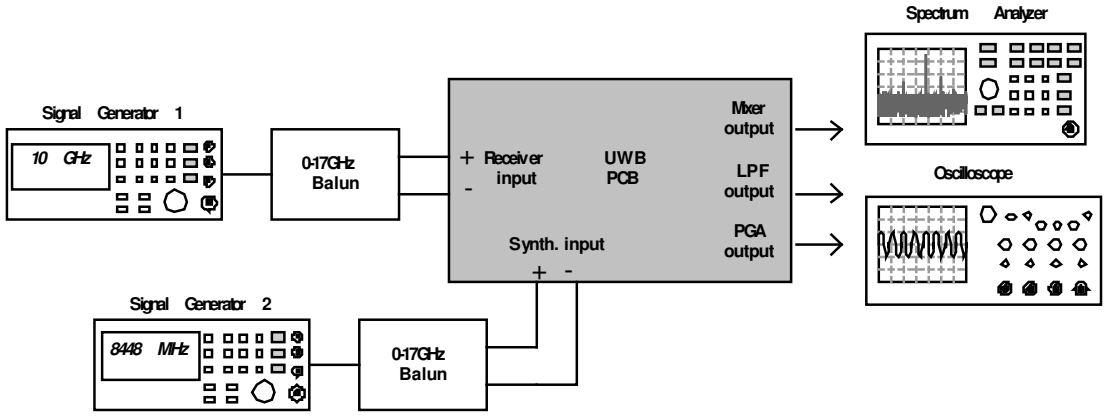


Fig. 5.14 Experimental setup for the characterization of the UWB receiver chain

The measured frequency response is shown in Fig. 5.15. The observed variations are mainly due to changes in the amplitude of the signal generator. Within a range of 500MHz, the frequency response from the LNA input to the current output of the RF transistors from the down-conversion mixer is expected to remain essentially constant. The frequency response of the receiver within a given band is expected to be dominated by the baseband filter. In Fig. 5.15 the measurement is compared against the simulated frequency response from the input (in current) of the current mirrors of the down-conversion mixer to the output of the filter.

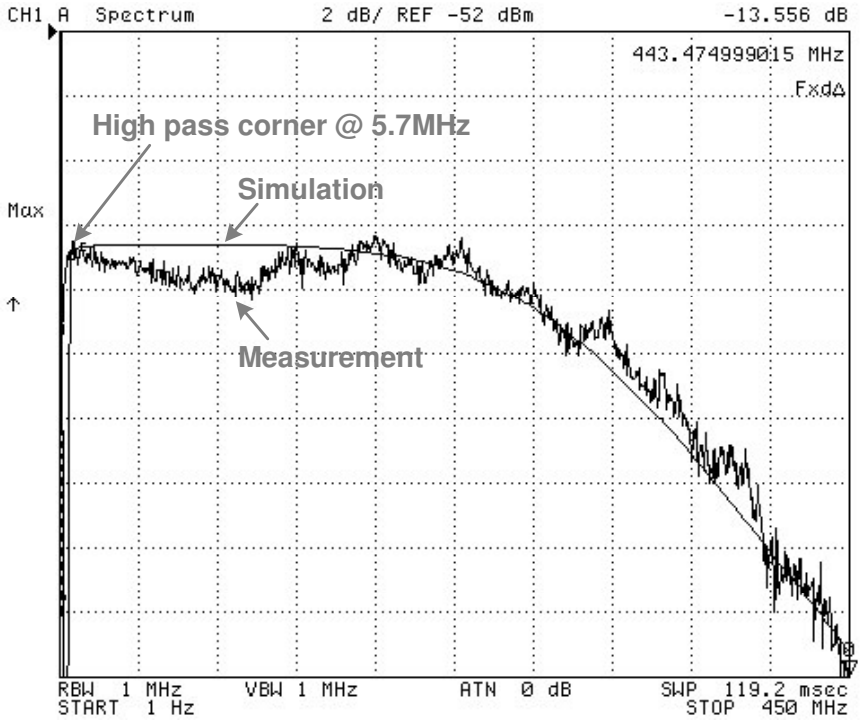


Fig. 5.15 Measured frequency response of the receiver

Fig. 5.16 shows the group delay of the LPF. This is measured by comparing the delay between the output of the mixer and the output of the filter at different frequencies. The observed variation over the pass band of the filter is 0.315ps, which is also in good agreement with the simulation result.

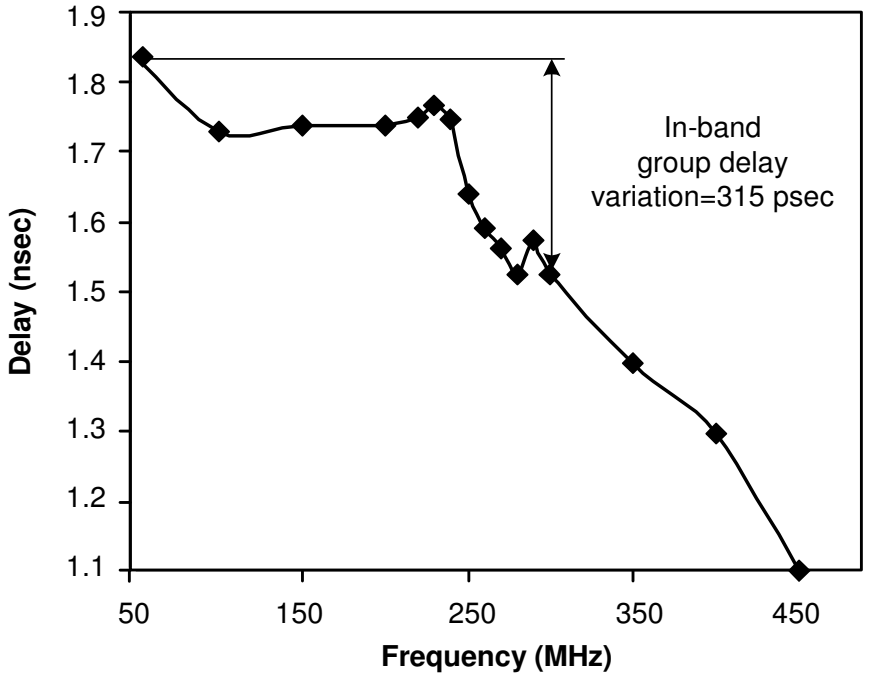


Fig. 5.16 Measured group delay variation of the baseband filter

The effect of the notch filter in the frequency response of the receiver chain was also measured. In this case, the RF input frequency to the LNA is swept from 4.7GHz to 5.7GHz (so that it crosses the center frequency of the tuned notch filter, 5.25GHz) and the output of the down-conversion mixer is observed from 0-1GHz. The result of this

measurement is shown in Fig. 5.17. The notch filter adds an attenuation of at leas 10dB in the band of interest (5.15-5.35GHz) and shows a peak attenuation of about 20dB. These results are in good agreement with the measurements of the LNA prototype presented in Section 5.1.3.

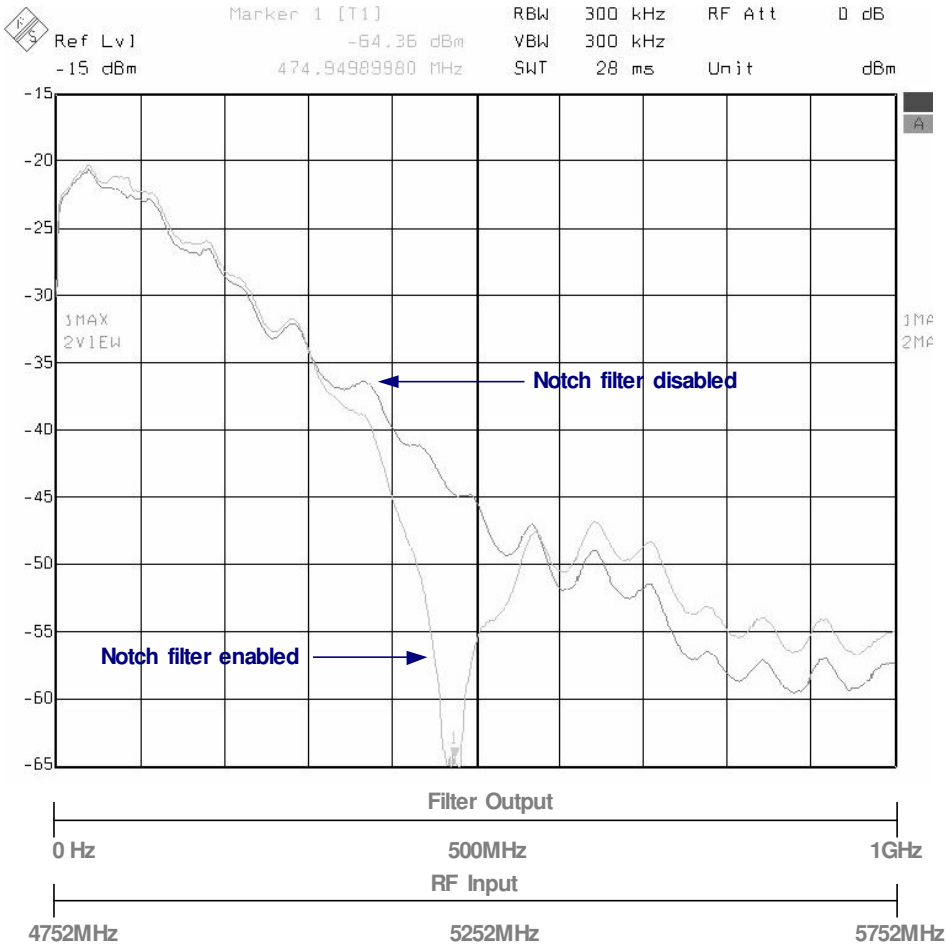


Fig. 5.17 Measured notch filter attenuation in the frequency response of the receiver

5.2.5 Noise figure

One of the most important figures of merit for the receiver is the NF, as it determines the expected sensitivity. Fig. 5.18 shows a screen capture from the spectrum analyzer showing the noise floor at the output of the PGA when the synthesizer operates at 4224MHz. It is important to observe that, as it can be expected, the noise spectrum follows a low-pass behavior approximately following the response of the LPF. From this measurement the NF is calculated as 5dB, which is in agreement with the simulation results.

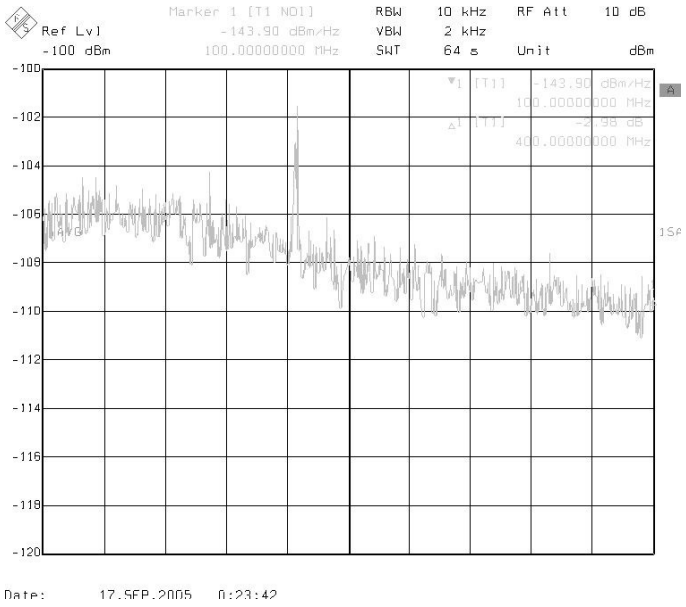


Fig. 5.18 Noise floor at the output of the receiver

The same measurement is repeated for different bands. At the highest frequency of operation (10.1GHz) the NF increases to 10dB. This degradation is attributed to losses in the PCB traces at the input of the LNA and a reduction in the amplitude of the LO signal to the down-conversion mixer.

5.2.6 Linearity

To measure the linearity of the receiver a two-tone test is performed. Each tone is taken from a separate RF signal generator and a power combiner is used to add them. The combined two-tone signal is applied to the receiver through the balun.

This test is performed first, for a frequency that yields baseband tones within the passband of the LPF (i. e. around 60MHz) to measure the in-band linearity and then for a frequency at the adjacent band (780MHz) to measure the out of band linearity. Figs. 5.19 and 5.20 show the measurement results for each of these two cases. The effective power (of each tone) at the input of the receiver is –48dBm and and –23dBm respectively. IM3 measurements are performed at different power levels. The extrapolated IIP3 is –29dBm in-band and –9dBm out-of-band.

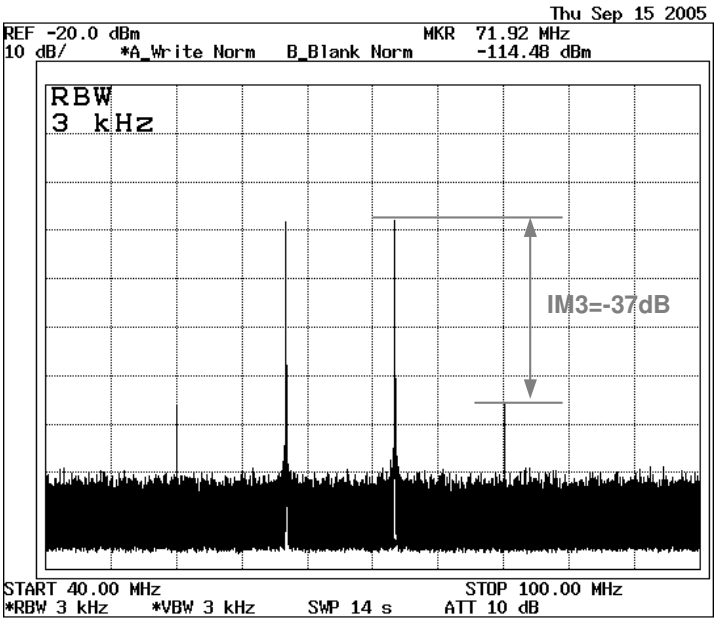


Fig. 5.19 Measured in-band IM3 performance

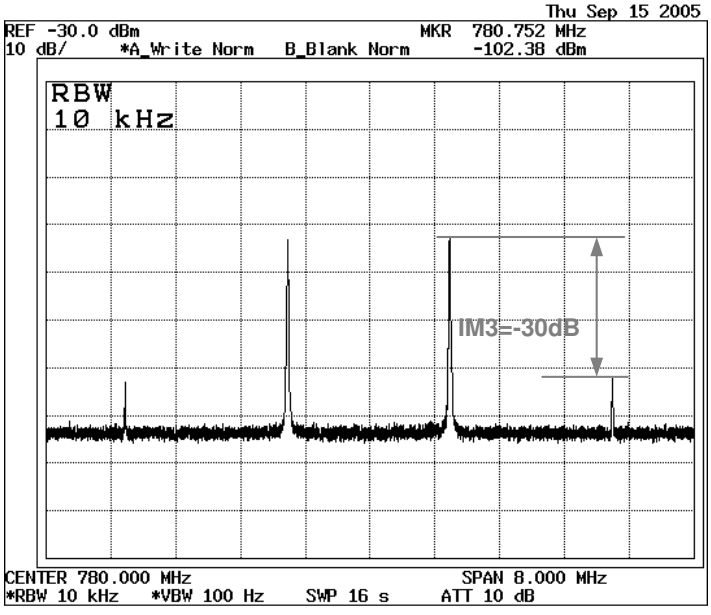


Fig. 5.20 Measured out of-band IM3 performance

5.2.7 Gain programmability

To measure the gain programmability, the output of the PGA amplifier is observed and its digital control is set for different gains. Fig. 5.21 shows the obtained amplitude variations at output of the PGA in steps of 2dB.

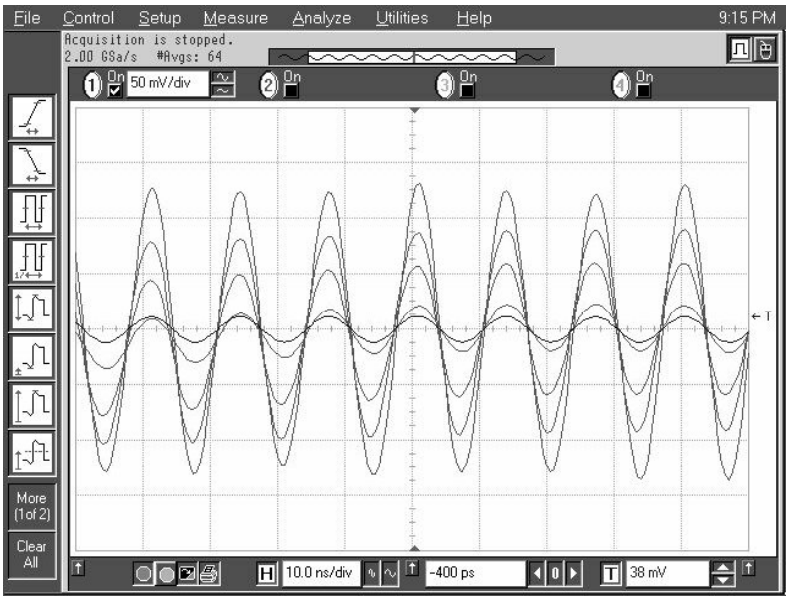


Fig. 5.21 Signal amplitude control at the output of the PGA

5.2.8 I & Q mismatch

To measure the mismatch between the I&Q channels of the receiver, the output of each PGA (I & Q) are captured with an oscilloscope. Fig. 5.22 shows an example of this characterization. In this case, the synthesizer operates at 4224MHz and input to the LNA is set to 4304MHz (80MHz offset frequency). The observed phase mismatch is 2.1° and the amplitude mismatch is 1.05dB.

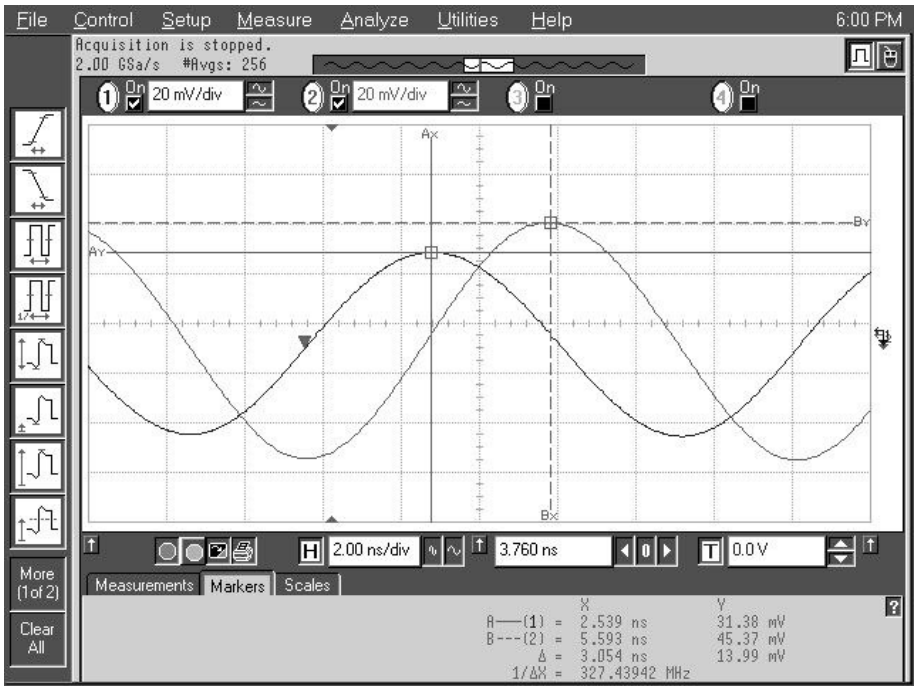


Fig. 5.22 In-phase and quadrature outputs of the receiver

5.2.9 Performance summary

In the MB-OFDM approach, subsequent bits of information are spread across the 3 bands of the band group in use. This spectral distribution of the information provides robustness against fading, interference and receiver non-idealities. For this reason, from the point of view of the complete communication system, the relevant performance of the receiver is its average behavior across the band group. Table 5.1 presents a summary of the measured results for each band group. The input 1dB compression is measured at a gain of 0dB in the PGA

Table 5.1. Measured performance per band-group

Band group	Maximum gain [dB]	Input 1dB comp. [dBm]	NF [dB]
1	78	-25dBm	5
2	77	-27dBm	6
3	71	-21dBm	8
4	67	-18dBm	10

Table 5.2 presents a summary of the current and area consumed by each block in the receiver. The IC operates from a 2.5V supply and the total power consumption is 285mW. This power does not include the buffers employed to observe the output of the frequency synthesizer off-chip.

Table 5.2. Current consumption and area contributions per block

Block	Current consumption (mA)	Area (mm^2)
LNA with Notch + Mixer	11	1.1
Frequency Synthesizer	80	2.4
LPF (I&Q)	15	0.34
PGA (I&Q)	8	0.32
Total	114	5.6 (with pads)

Table 5.3 summarizes all of the measurement results. The receiver IC mounted on a FR-4 substrate provides a maximum gain of 67-78dB and NF of 5-10dB. Post-layout simulation results for the LNA with the load of the mixer, showed a gain reduction of

3dB at the highest frequency band group. The additional gain variation in the receiver cross bands is attributed to a reduction in the LO amplitude and loss on the PCB.

Table 5.3. Performance summary

Maximum conversion gain across bands	78-67 dB
Noise figure across bands	5-10 dB
IIP3 for band group 1 (worst case)	-9 dBm
Baseband group delay variation	<0.6 nS
Active area	5.6 mm^2 including pads
Current consumption	114 mA
Supply voltage	2.5 V
Package	QFN
Technology	IBM 6HP 0.25μm SiGe BiCMOS

To place the achieved results in perspective, Table 5.4 presents a summary of the currently reported MB-OFDM UWB radios. Even though the power consumption is about 50% higher, the frequency range is the highest and the implementation is done in a slower (lower f_T , lower cost) technology. So far, this is the first 3-10GHz MB-OFDM UWB receiver and the first UWB receiver operating beyond 5GHz demonstrated in package. This IC demonstrates the feasibility of low cost and very high data rate radios capable of maximizing the use of the available UWB spectrum.

Table 5.4 Current state-of-the art in MB-OFDM radios

Reference	# of Bands / Freq. Range	Current / Vdd	Technology/Peak f_T	Comments
[10]	3 / 3 - 5GHz	74mA / 2.7V	0.25µm SiGe / 70GHz	Packaged
[11]	3 / 3 - 5 GHz	70mA / 1.5V	0.13µm CMOS / -	Packaged
[12]	7 / 3.1 - 8.2 GHz	88mA / 2.7V	0.18µm SiGe / -	Probed
This Work	11 / 3.4 - 10.2 GHz	114mA / 2.5V	0.25µm SiGe / 47GHz	Packaged

CHAPTER VI

FREQUENCY RESPONSE CHARACTERIZATION SYSTEM FOR ANALOG TESTING

The most important specifications of a continuous time (CT) analog circuit such as a filter, programmable gain amplifier, buffer or equalizer are related to their frequency response; it is desired that these devices attain a certain gain and/or phase shift at specific frequencies. The majority of the reported BIT and DFT techniques for those circuits have proposed indirect testing methods for the detection of faults and do not verify the target specifications directly [4, 5, 27, 28]. In this chapter, a BIT technique for the magnitude and phase response characterization of a CUT is presented. First, the principle of operation of this technique and a procedure for its application are described. Two IC implementations are proposed to evaluate the usefulness of this strategy. In the first one, the IC acts as a tester chip for the characterization of an external CUT and its operation is demonstrated in the testing of a commercial chip for ADSL applications. The second implementation is a complete test system that enables the magnitude and phase response characterization of a CUT integrated on the same chip through a completely digital interface. The design considerations and experimental results for each implementation are presented.

6.1. Principle of operation

At a given test frequency (ω_0), the transfer function of a CUT ($H(\omega_0)$) can be obtained by comparing the amplitude and phase between the signals at its input and output. By implementing a signal generator (tunable over the bandwidth of interest for the characterization) and an amplitude and phase detector (APD), a built-in transfer function characterization system can be obtained as shown in Fig 6.1.

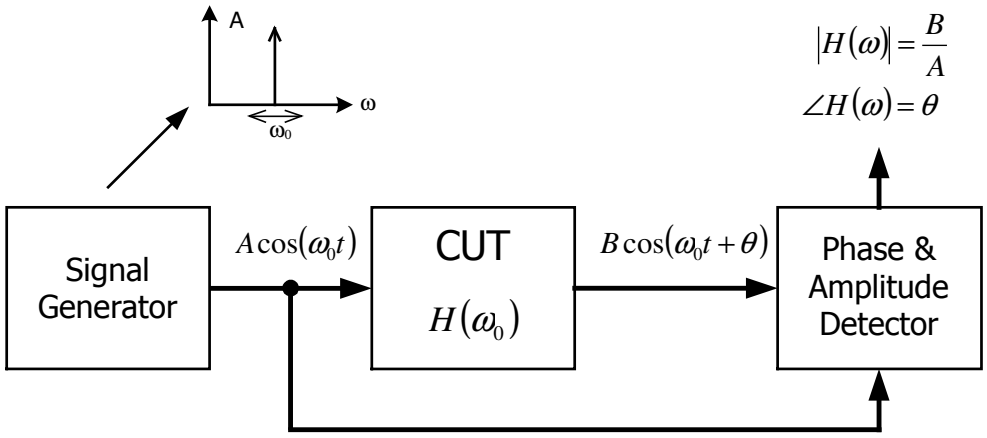


Fig. 6.1 Conceptual description of the proposed system

A block diagram of the proposed technique for phase and amplitude detection is depicted in Fig. 6.2. An analog multiplier sequentially performs three multiplications between the input and output signals from the CUT. For each operation, a DC voltage and a frequency component at $2\omega_0$ are generated; the latter is suppressed by a low-pass filter (LPF) at the output of the multiplier.

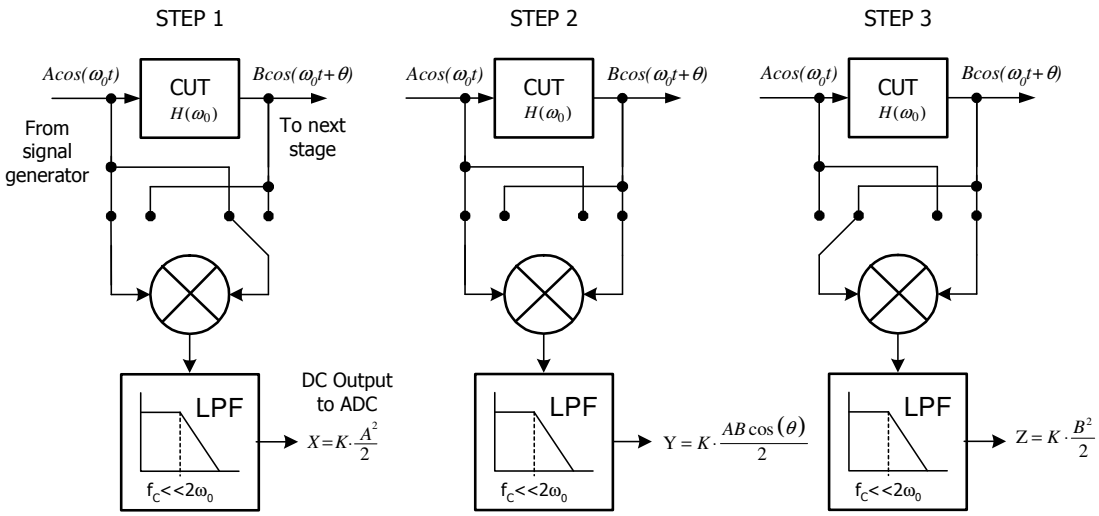


Fig. 6.2. Operation of the amplitude and phase detector

The following three DC voltages are obtained:

$$X = K\frac{A^2}{2} \tag{6.1}$$

$$Y = \frac{1}{2}K \cdot A \cdot B \cdot \cos(\theta) \tag{6.2}$$

$$Z = K \cdot \frac{B^2}{2} \tag{6.3}$$

where K is the gain of the multiplier, A and B are the amplitude of the signals at the input and output of the CUT, respectively, and θ is the phase-shift introduced by the CUT at ω_0. From these DC outputs, an off-chip device can evaluate the transfer function of the CUT at ω_0 by performing the following simple operations:

$$\theta = \cos^{-1}\left(\frac{Y}{\sqrt{X \cdot Z}}\right) \tag{6.4}$$

$$\frac{B}{A} = \sqrt{\frac{Z}{X}} \tag{6.5}$$

It is important to note that these operations do not imply the need of sophisticated off-chip equipment. Various inexpensive modern 8-bit microcontrollers have the capability of working with trigonometric functions and other mathematical operations. The proposed technique for the measurement of the magnitude and phase responses is inherently robust to the effect that process variations can have on the main performance characteristics of the building blocks. From equations 6.4 and 6.5 note that for the computation of the parameters of interest (B/A and θ), neither the amplitude of the signal generator (A) nor the gain of the multiplier (K) need to be set or known a priori. Hence, these parameters that can be affected b process variations; do not require an accurate control. Moreover, if the cut-off frequency (ω_c) of the LPF is sufficiently small, its variations will also have a negligible effect on the accuracy of the measurements.

The effect of the spectral content of the test signal is now analyzed. Let HD_i, be the relative amplitude of the i^{th} harmonic component (i = 2, 3, …n) with respect of the amplitude A of the fundamental tone. In the pessimistic assumption that the CUT does not introduce any attenuation or phase shift to neither of these frequency components, the DC error voltage (E) introduced by the harmonic distortion components to each of the voltages X, Y and Z is given by:

$$E = K \cdot \frac{A^2}{2} \cdot \sum_{i=2}^{n} (HD_i)^2 = K \cdot \frac{A^2}{2} \cdot (THD)^2 = X \cdot (THD)^2 \tag{6.6}$$

where THD is the total harmonic distortion of the signal generator. If THD is as high as 0.1 (10%), even in this pessimistic scenario the error voltage would be equivalent to only

0.01 (1%) of X. This tolerance to harmonic components is an important advantage since it eliminates the need for a high precision sinusoidal signal generator.

6.2. Testing methodology

This section presents an algorithm for the automated test of a CUT using the proposed BIT scheme. The control and output variables involved in the testing process are summarized in Table 6.1.

Table 6.1 Test variables

F	Frequency of the signal applied to CUT
A	Amplitude of the signal applied to CUT
B	Amplitude of the signal at the output of the CUT
MAG	Magnitude response of the CUT (B/A) at F
PHI	Phase shift introduced by the CUT at F
DC1	DC voltage proportional to $A^2/2$
DC2	DC voltage proportional to $B^2/2$
DC3	DC voltage proportional to AB·cos(PHI)

From the specifications of the CUT, a set of N test frequencies [F1 F2 … FN] is defined. Through adequate fault modeling, the smaller N to attain the desired fault coverage can be found. Even though the amplitude and phase detection is independent from the amplitude of the on-chip signal generator, an appropriate amplitude [Ai] for the

input signal (which not necessarily has to be different for each frequency) should be chosen to avoid saturation in the CUT. As described in the previous section, MAG and PHI can be computed from the outputs of the phase and amplitude detector (DC1, DC2, DC3). From the expected magnitude and phase responses of the CUT, each test vector [Fi Ai] is associated with acceptable boundaries for the output vector [MAGi PHIi]. Using the described test parameters, the algorithm shown in Fig. 6.3 can be employed for the efficient functional verification of the CUT.

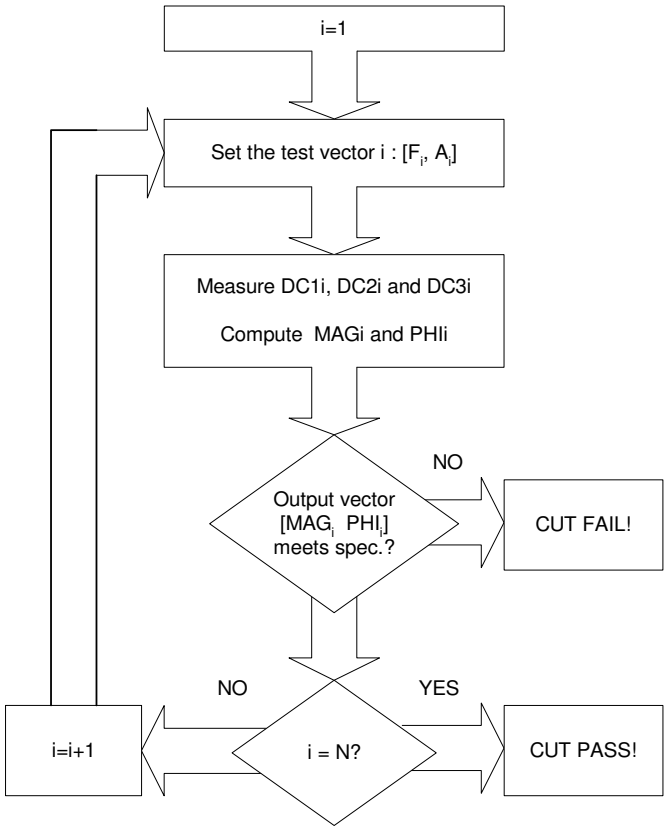


Fig. 6.3 Testing procedure

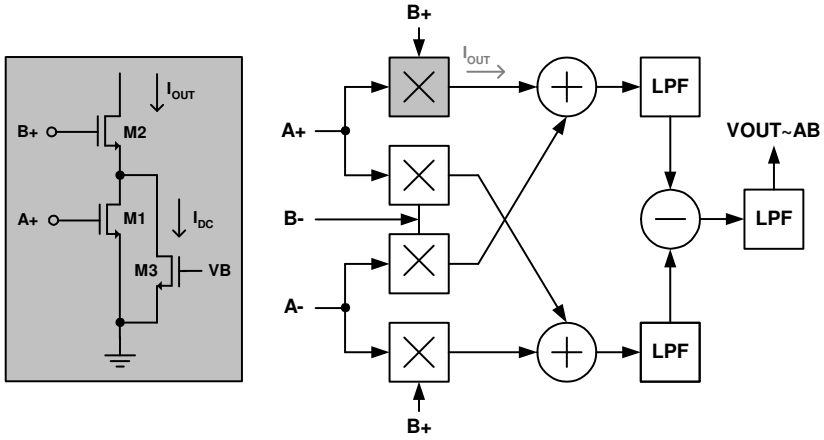
6.3. Circuit implementation as tester chip

6.3.1 Analog multiplier

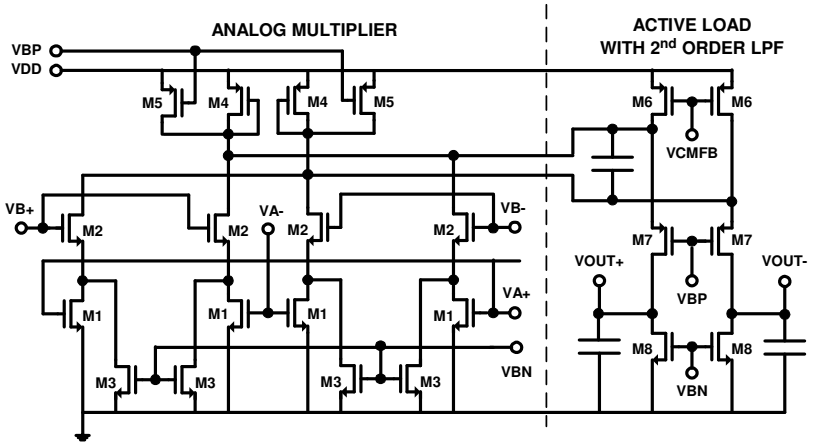
The circuit schematic for the analog multiplier with a cascaded LPF used in the APD is shown in Fig. 6.4. The inputs are the differential voltages VA and VB and the output is the differential DC voltage VOUT. The core of the four-quadrant multiplier (transistors M1 and M2) is based on the one in figure 7(c) in [29]. Transistors M1 operate in the triode region; the multiplication operation takes place between their gate-to-source and drain-to-source voltages. Transistors M2 act as source followers. Ideally, the voltage at the source of transistors M2 should be just a DC shifted version of the voltage signal applied to their gates (B+ and B-). However, the drain current of transistors M1 and M2 is the result of the multiplication, and its variations affect the operation of the source followers, introducing an undesired phase shift on the voltage signals applied to the drain of transistors M1. This effect significantly degrades the phase detection accuracy of the multiplier. To overcome this problem, the addition of transistors M3 (which operate in the saturation region) to the original multiplier core is proposed. These additional transistors provide a fixed DC current to the source followers, improving their transconductance and reducing their sensitivity to the AC current variations. This improvement to the multiplier circuit results in a high-resolution analog phase detector.

An active load and a common-mode feedback (CMFB) circuit (not shown for simplicity) are added to the multiplier core to provide a voltage output (instead of the

current output of the multiplier core) and implement two low-pass poles which filter out the high frequency products of the multiplication.



(a)



(b)

Fig. 6.4. Proposed analog multiplier. (a) Conceptual description. (b) Circuit schematic

6.3.2 Signal generator

As mentioned in section 6.1, the proposed BIT technique is inherently tolerant to relatively high levels of harmonic distortion in the stimulus applied to the CUT. For the on-chip signal generator, a compact analog voltage controlled oscillator (VCO) can be employed. The oscillation frequency can be set with an external or on-chip loop. Ring oscillators are preferred for clock signal generation due to their simplicity and low power consumption. However, their harmonic distortion is very high and their amplitude is fixed; both characteristics are undesirable for this application. LC-based oscillators have a superior linearity and phase noise performance but their required area can become prohibitively large for frequencies below 1GHz. For signal generation in the range of tenths to few hundreds of MHz, a transconductance-capacitance (OTA-C) oscillator structure [30] offers amplitude control and low distortion in a compact implementation, and hence is chosen for this design. Fig. 6.5 shows a block diagram of the designed differential quadrature oscillator. The oscillation frequency is determined by the ratio $g_m\omega/C$. The signal frequency is determined by the ratio $g_m\omega/C$ and can be controlled through V_{CF}. The oscillation amplitude can be adjusted through V_{CA}. For this implementation C=400fF.

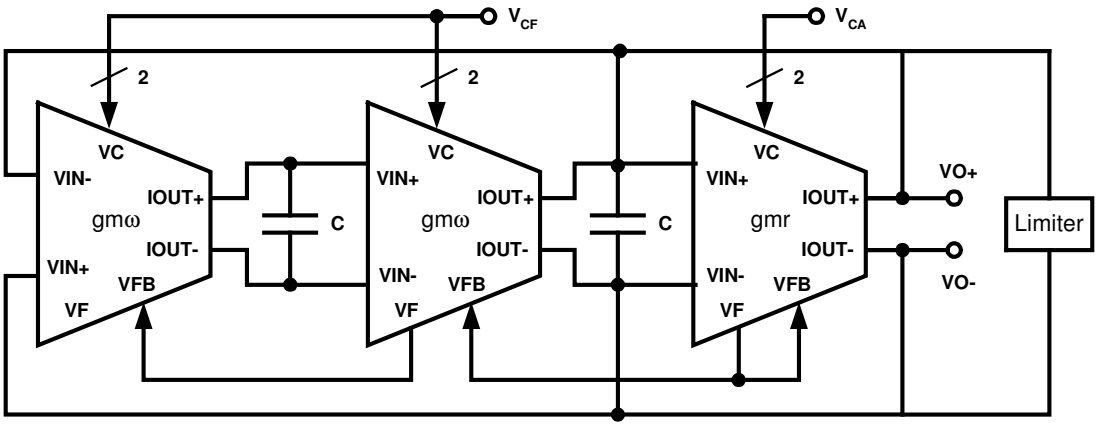


Fig. 6.5. OTA-C signal generator

The employed limiting mechanism is simple and assures a low-distortion output; it consists of diode connected transistors. The amplitude of the output signal can be controlled by the negative resistance (1/gmr) through V_{CA}. A linear oscillation frequency (f_{OSC}) Vs. frequency control voltage (V_{CF}) is convenient for the overall PLL performance and attained through the use of OTAs with linear transconductance control.

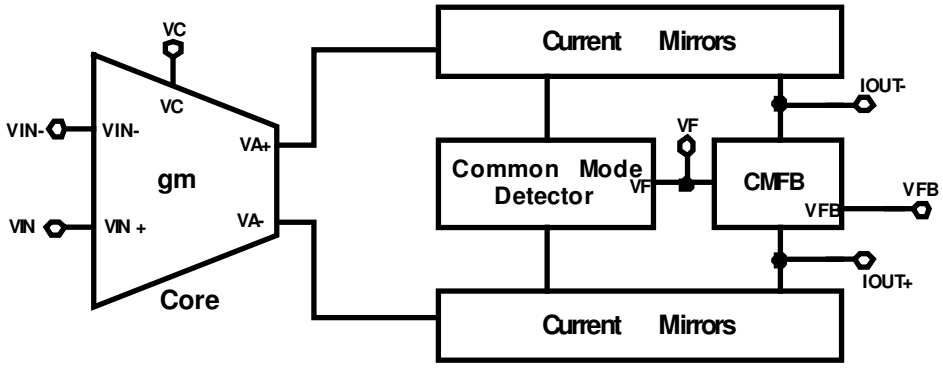
The employed OTA is described with a block diagram in Fig. 6.6(a). The detailed circuit schematic is shown in Fig, 6.6(b). The transconductance operation is carried out by transistors M1 which operate in the linear region. The drain to source voltage (V_{DS}) of these transistors is determined by the differential voltage VC through transistors M2; in this way the effective transconductance is a linear function of VC.

An inherent CMFB detection mechanism [31] is employed to control the DC level of the output nodes. This mechanism takes advantage of the fact that cascaded OTAs are used in the oscillator architecture. The DC level of the previous OTA is sensed by transistors M1. This DC level will impact the current flowing through transistors M3 and

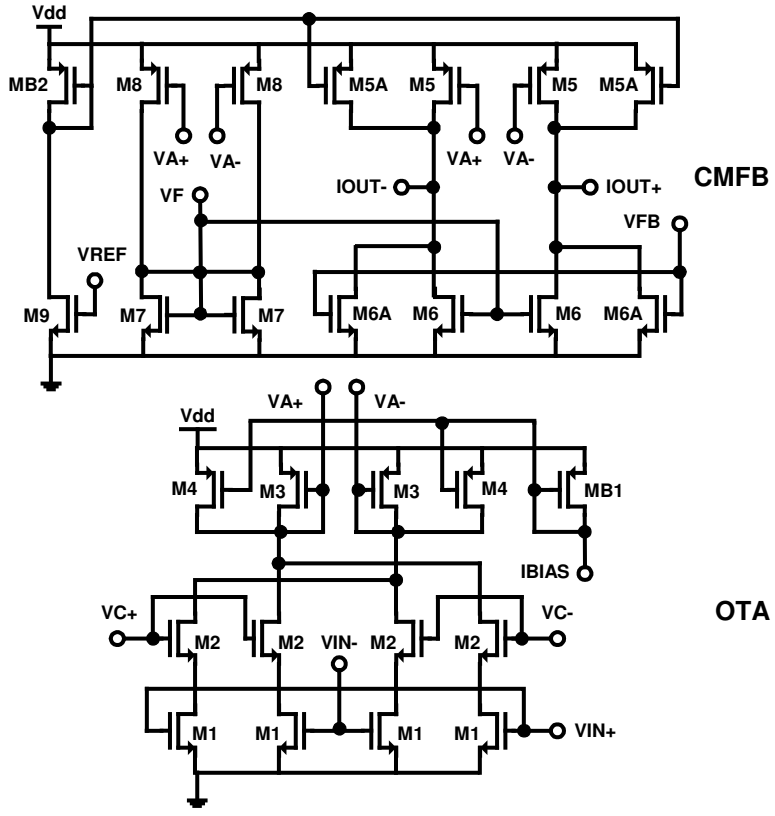
M8. Since transistors M7 are diode connected and their gate terminals attached, only the common mode variations will have an impact on the node VF; this voltage is fed back to the previous OTA. In turn, the following OTA will detect the common mode DC level at the output nodes and will feedback this information through the node VFB. The current flowing through transistors M6A is compared with the current provided by transistors M5A. This current comparison forces VFB (and hence the DC level at the output nodes) to be very close to VREF.

For an OTA-C oscillator, a relatively high output resistance (R_{OUT}) is desired from the OTA. An important disadvantage of the inherent CMFB detection mechanism proposed in [31] is that the addition of transistors M5A and M6A degrades R_{OUT} significantly since they must have the same aspect ratio as the transistors to which they are connected in parallel. This effect worsens when two or more OTAs should be connected to the same node. This R_{OUT} issue is addressed in this design in the following way: First, it should be noted that in the differential current mirror formed by transistors M3 and M5 we are interested in transferring the AC information only. To optimize the frequency response, a multiplying factor of 2 is desired for these current mirrors, which would imply to double the DC current, further degrading R_{OUT}. To avoid this problem, transistors M5A are added. They provide most of the DC current required by the input stage. Transistors M3 are biased by only a small portion of the DC current and, since they are diode connected, copy the AC variations to transistors M5. In this way, the transistors at the output branch are biased with a relatively small DC current that does

not depend on the transconductance magnitude. An OTA with a sufficiently high and tuning invariant R_{OUT} is obtained, improving the linearity and tuning range of the VCO.



(a)



(b)

Fig. 6.6 Voltage controlled transconductor. (a) Block diagram. (b) Circuit schematic

6.4. Tester chip experimental results

To demonstrate the feasibility of the proposed BIT technique, the described phase and amplitude detector and signal generator were fabricated in standard TSMC CMOS 0.35µm technology. The chip microphotograph is shown in Fig. 6.7. The circuit operates from a 3.3V supply and uses an area of 540X370µm^2.

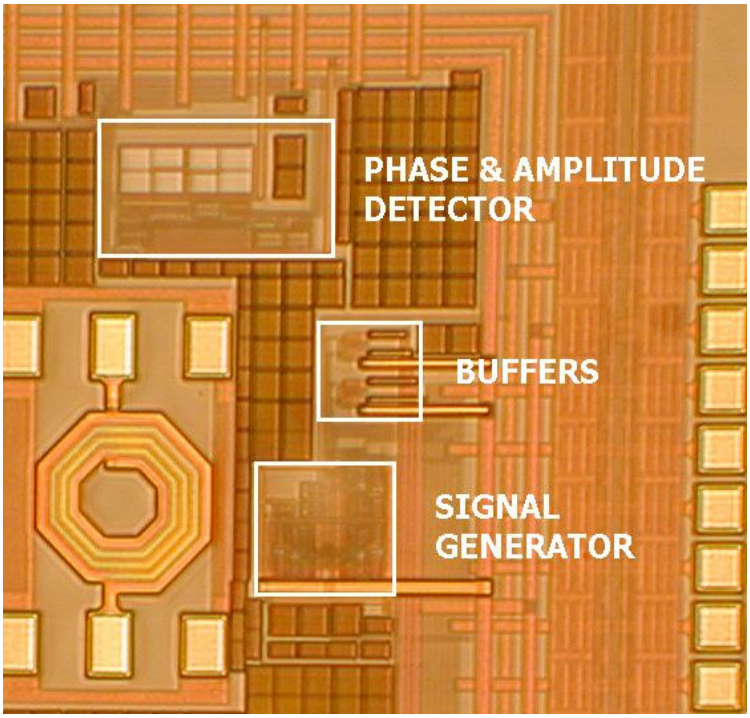


Fig. 6.7 Chip microphotograph

6.4.1 Phase and amplitude detector performance

In order to evaluate the accuracy of the phase detection feature of this circuit, the relative phase between the input signals to the multiplier is swept from 0° to 360° (using

two phase-locked signal generators). The phase computed from the output of the LPF using equation 4 is compared against the actual phase to obtain the error plot. For the test results shown in Fig. 6.8, the peak amplitude of the differential signals (A and B) is 250mV and the frequency is 80MHz.

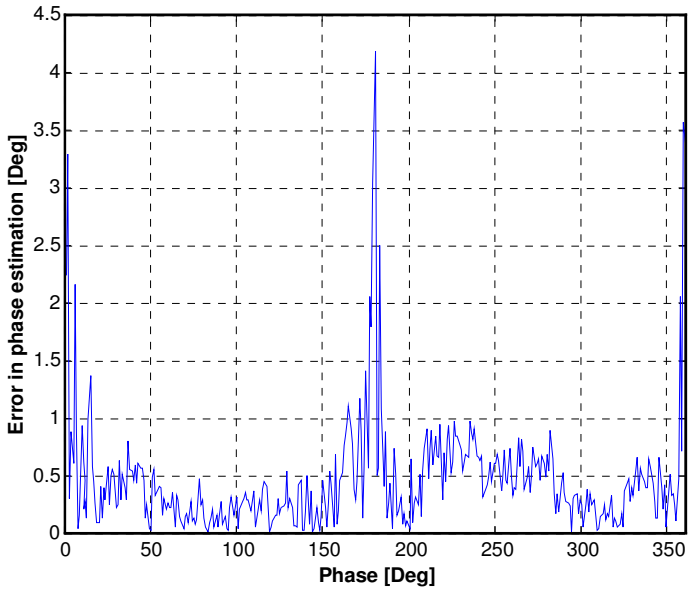


Fig. 6.8 Phase detection experimental results

Due to a differential offset caused by the mismatch between transistors M2 an error in phase estimation of more than 1° is present in a range of ±3° around 0° and 180°. However, the phase measurement error is <1° over 95% of the overall 360° range and the average error is <0.5°. The resolution attained for phase detection in this design is better than that of a recent commercial gain and phase detection system [32]. These

results prove the effectiveness of the proposed improvement to the multiplier to enhance phase detection accuracy.

For the evaluation of the amplitude detection feature, the amplitude of one of the input signals to is swept from 0 to 500mV and the amplitude computed from the output of the LPF is plotted along with the actual amplitude. The test results for a 50MHz input signal are shown in Fig. 6.9. The mentioned differential offset limits the minimum detectable signal to around 8mV. A summary of results is presented in Table 6.2.

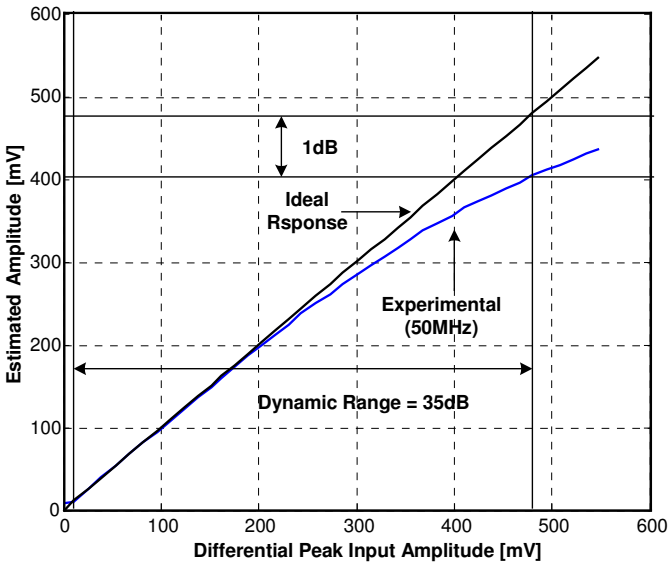


Fig. 6.9 Amplitude detection experimental results

Table 6.2 Experimental results for phase and amplitude detector

Conversion Gain (K)	5 V/V^2
Average error in phase measurement for A=B=500mVpp differential 80MHz input signals	0.4°
Maximum operating frequency for DR>30dB and average error in phase detection<0.5°	120MHz
Dynamic Range at 50MHz input	35dB
Power consumption	6mW
Silicon area	320×170μm^2

6.4.2 On-chip signal generator performance

Fig. 6.10 depicts the measured tuning characteristic of the on-chip signal generator. As it was expected the oscillation frequency is a linear function of the control voltage for most of the tuning range. Fig. 6.11 shows the obtained output signal at two different frequencies close to the limits of the tuning range.

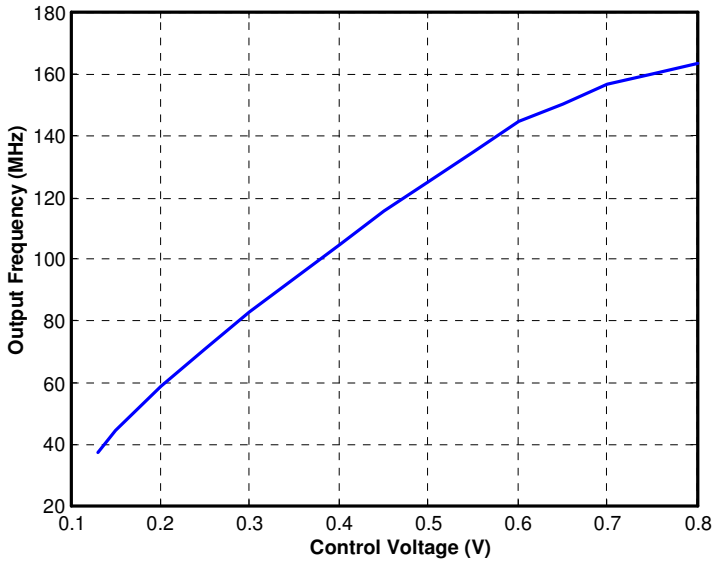


Fig. 6.10 Measured VCO tuning range

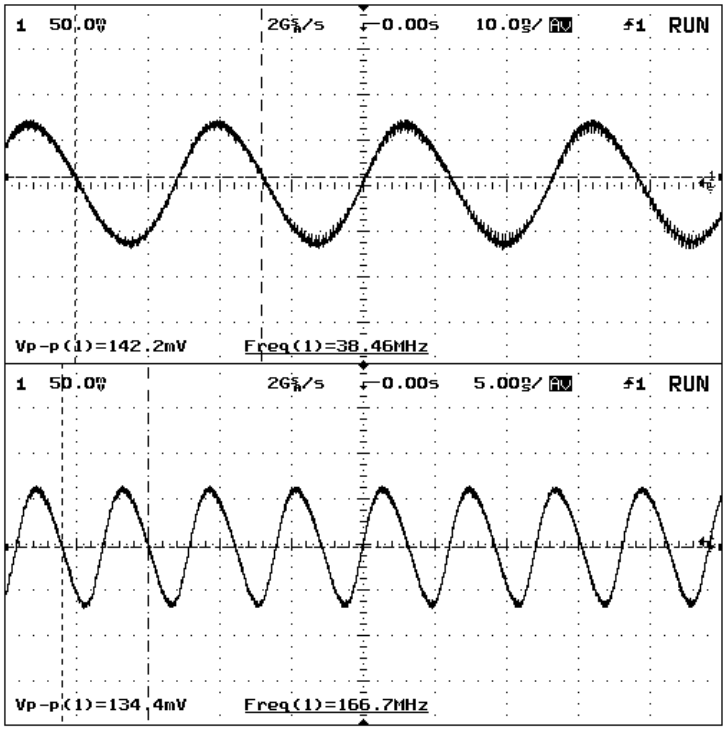


Fig. 6.11. Transient output of quadrature oscillator

The measured 2nd and 3rd order harmonic distortion are below -35dBc across the tuning range. Fig. 612 presents the output spectrum of the VCO for an output frequency of 59MHz. A summary of results for the signal generator is presented in Table 6.3.

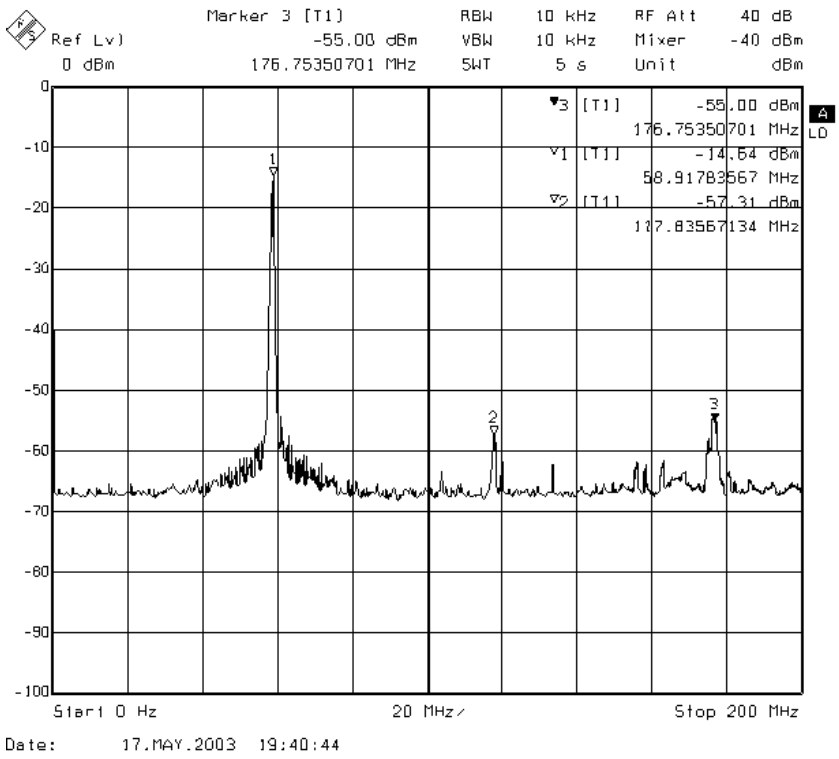


Fig. 6.12 Output spectrum of the on-chip signal generator

Table 6.3. Experimental results for the signal generator

Tuning range	38 to 167 MHz
HD3 (from 40 to 150MHz)	<-39dB
Power consumption	69mW
Active area	220×200 μm^2

6.4.3 Characterization of a commercial analog product

The THS7001 IC from Texas Instruments [33], (PGA for ADSL applications) is chosen to demonstrate the applicability of the proposed BIT system in the characterization of a commercial analog IC. This PGA has 8 different digitally programmable gain settings and a small signal bandwidth of around 60MHz to 80MHz

depending on the operating conditions. The employed setup for the characterization of the THS7001 is depicted in Fig. 6.13.

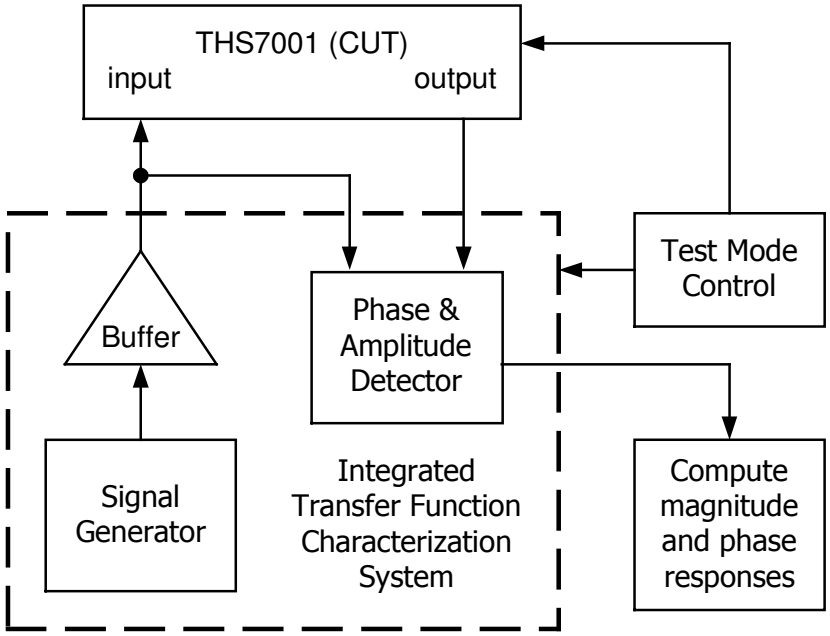


Fig. 6.13 Test setup for the proposed system as a tester chip

Fig. 6.14 shows the experimental results for the verification of the gain programmability of the THS7001 at 40MHz using the proposed testing scheme. Fig. 6.15 shows the magnitude response characterization experimental results. For this test, the DC gain of the PGA is set to 2dB. The results are in good agreement with the typical circuit characteristics from figures 34 and 35 in the product data sheet [33]. A small peak in the magnitude response around 40MHz is expected for DC gain settings between 2 and 14dB. This effect is properly detected by the proposed test system. The phase

response characterization results are shown in Fig. 6.16 for the same test conditions as in the magnitude response. No data about the phase response is provided in the product data sheet.

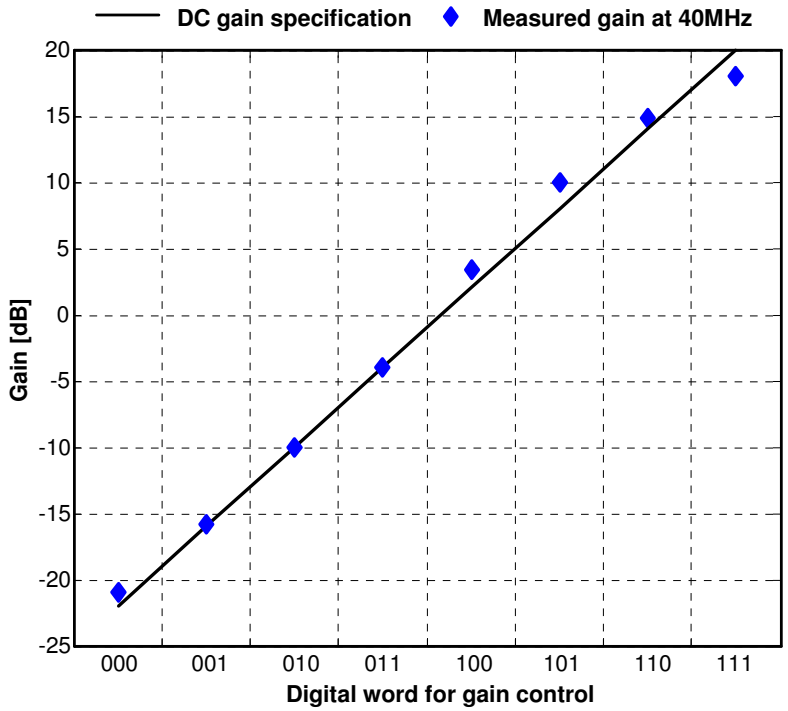


Fig. 6.14 Gain programmability characterization

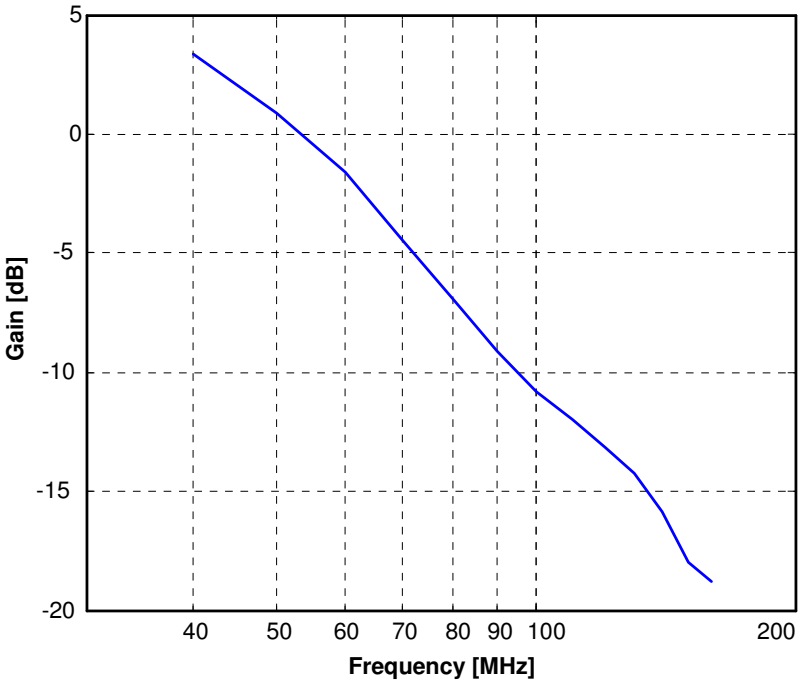


Fig. 6.15 Magnitude response characterization

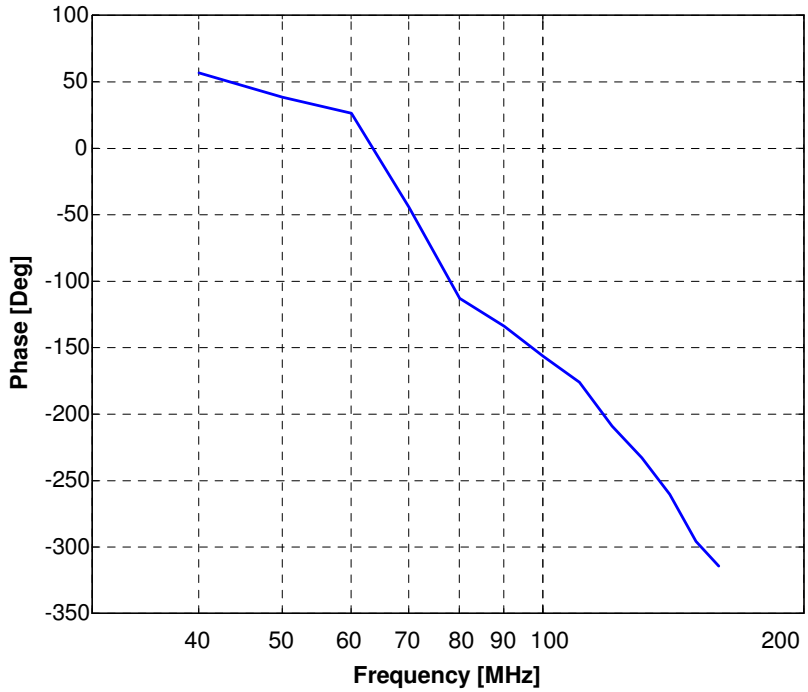


Fig. 6.16 Phase response characterization

6.5 Implementation as a complete on-chip test system with digital interface

A general analog system, such as a line driver, equalizer or the baseband chain in a receiver consists of a cascade of building blocks or stages. At a given frequency ω_o each stage is expected to show a gain or loss and a delay (phase shift) within certain specifications; these characteristics can be described by a frequency response function $H(\omega_o)$. An effective way to detect and locate catastrophic and parametric faults in a given analog system is to test the frequency response $H(\omega)$ of each of its building blocks. However, the observability of embedded analog blocks is very limited and the required equipment adds extra cost to the test process. It is desirable to count with on-chip testing circuitry such that the entire SoC (both analog and digital sections) can be tested with a single digital ATE. The proposed system is meant to perform these functions as shown in Fig. 6.17. The test architecture consists of a frequency synthesizer, an amplitude and phase detector (APD), a demultiplexer that serves as an interface between the CUT and the APD, and ADC that digitizes the output of the APD which consists of DC voltages.

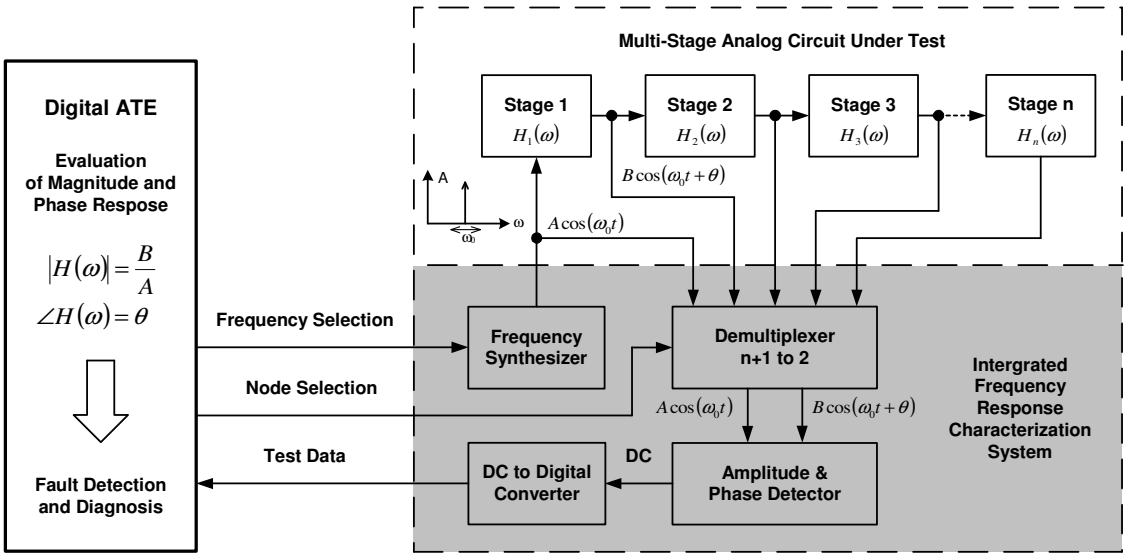


Fig 6.17 Architecture of the proposed frequency response characterization system

6.5.1 Analog multiplier for amplitude and phase detection

The analog multiplier core showed on the right side of Fig. 6.4(b) is also used in this implementation. However, to simplify the output stage, instead of a cascode load with CMFB, a differential to single-ended converter is employed. The circuit schematic of the complete analog multiplier is shown in Fig. 6.18. The second pole of the LPF is implemented by the capacitor C2 and the passive resistor R1. Note that the DC operating point of VOUT can be set through VBO and hence, no other active circuitry is required to set this voltage.

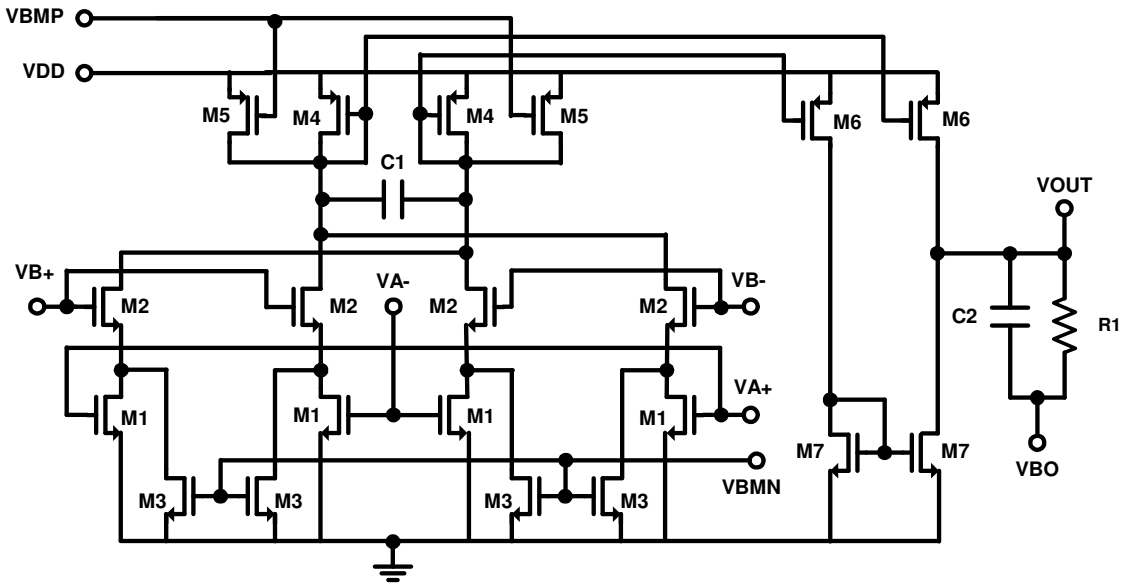


Fig. 6.18 Analog multiplier for the on-chip test system

6.5.2 Demultiplexer-buffer for interface with CUT

An important component of the proposed system is the interface between the CUT and the phase and amplitude detector. As shown in Fig. 6.17, through a demultiplexer, the frequency response at different stages of the CUT can be characterized. In addition, the multiplexer should present a high input impedance (so that the performance of the CUT is not affected) and provide the appropriate DC bias voltages to the phase and amplitude detector. The proposed circuit to comply with these functions is depicted in Fig. 6.19. The differential pair with active load composed by transistors M8 and M9 form a buffer with unity gain. The output of the buffers (differential voltages VA and VB) are connected to the corresponding inputs of the phase and amplitude detector. The DC operating point of the output is easily set through the bias voltages VBA and VBB.

The input capacitance of the multiplexer, as seen from the input of the switches in the on state, is approximately 50fF.

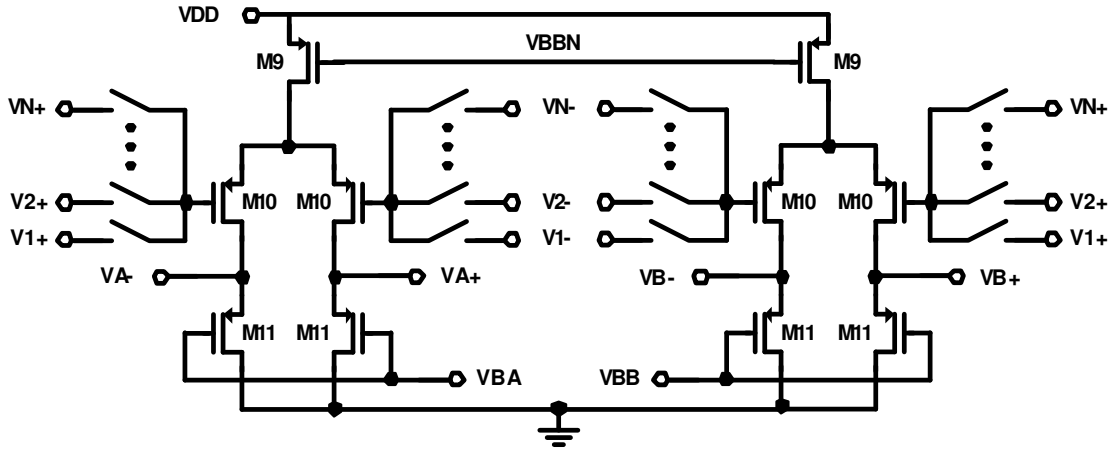


Fig 6.19 Multiplexer/buffer circuit schematic

6.5.3 Frequency synthesizer and VCO

The employed frequency synthesizer for the generation of the input signal to the CUT is a type-II PLL with a 7 bit programmable counter, spanning a range of 128MHz in steps of 1MHz. The block diagram is shown in Fig. 6.20(a). One of the main advantages of employing a PLL in this application is that to generate the internal stimulus, only a relatively low frequency signal (f_{REF} = 1 MHz in this case) is required as a reference. In contrast, a sigma-delta based signal generator requires a clock that runs at a significantly higher speed than the generated signal. In this PLL design, the loop filter is implemented with off-chip elements to reduce the silicon area. These passive

components can be easily incorporated into the test board of the chip. Moreover, in an SoC implementation, the reference signal can be obtained from an internal clock. An alternate implementation is shown in Fig. 6.20(b), in this case the loop is closed externally. The ATE receives the output of the divider and sets the control voltage of the VCO. This approach uses the same number of pins (a 1MHz digital signal and a DC voltage) but further reduces the amount of on-chip components and enables an independent verification of the loop operation.

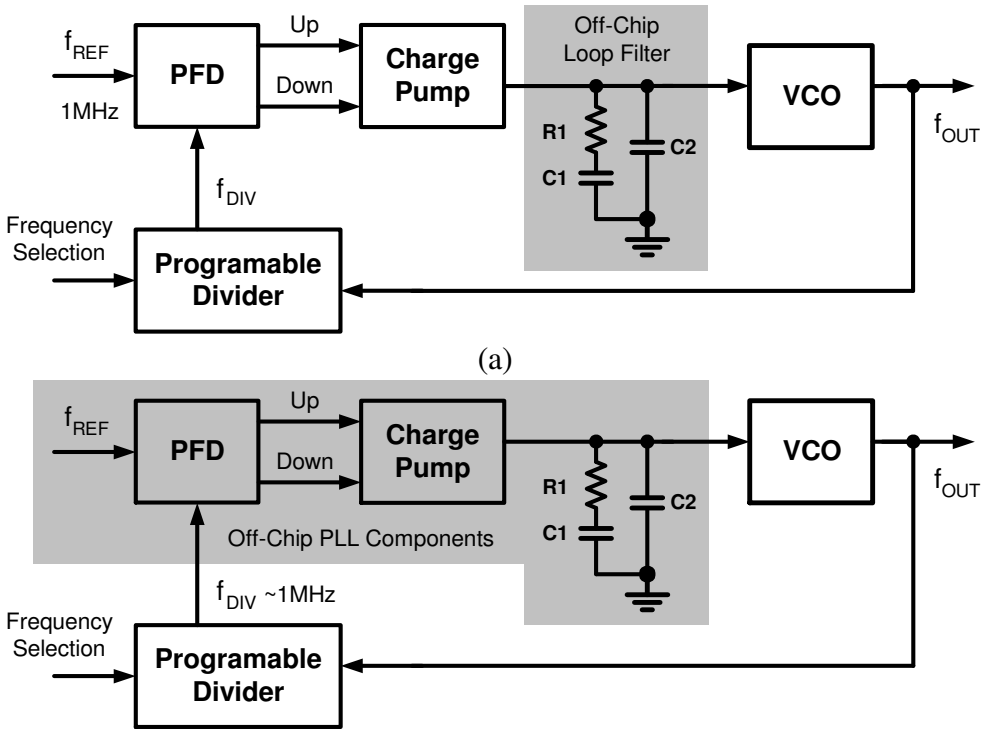


Fig. 6.20 PLL-based frequency synthesizer for the FRCS. (a) Implemented circuit. (b) Alternate implementation

The proposed voltage controlled oscillator (VCO) is shown in Fig. 6.21 It is based on a multi-vibrator [34] which employs 3 pairs of transistors (M11-M13) and one capacitor (C1). A differential, tunable first order low-pass filter (LPF) is added to the VCO. The LPF is formed by transistors M14-M15 and capacitor C1. The VCO and LPF are tuned simultaneously through VC to keep the oscillation amplitude relatively constant over the entire frequency tuning range (within 3dB of variation) and a THD of less than 10%.

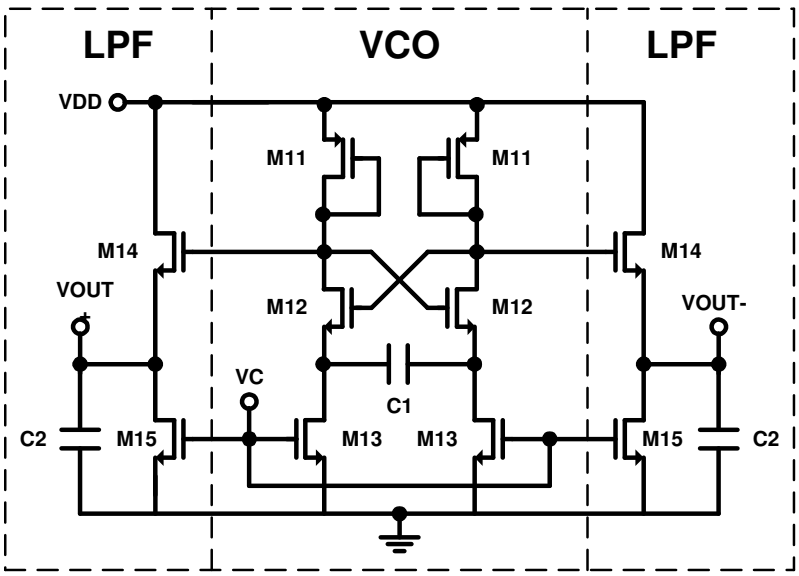


Fig. 6.21 Multivibrator-based VCO schematic

6.5.4 Algorithmic analog-to-digital converter

As discussed earlier, the output of the APD is a DC voltage; leading us to the fact that a low speed ADC can be used. This conclusion excludes bulky and high speed architectures as Flash converters and Pipeline converters. A DC-ADC can be used for

various on-chip testing and calibration purposes applications such as monitoring the DC operating points at different nodes of an SoC [35]. For these applications, low power consumption and compact architectures are required.

Simple architectures for low power ADC are presented in the literature [35-36]. Further decrease in the power and area can be done on the expense of the speed of the ADC. Successive approximation converters are the optimum choice for their simple architectures, small area and low power consumption. Equation 6.7 describes the basic operation of a general successive approximation ADC. Where, V_{in} is the analog input, V_a is the analog equivalent for the estimated digital output, and <> denotes the comparison operation.

$$V_{in} - V_a <> 0 \tag{6.7}$$

However, the subtraction in equation 7 is done through the two inputs of a comparator, which usually requires offset compensation techniques to have precise output. In an ADC architecture introduced in [36], the subtraction is done inherently in a resistor ladder, thus the non-inverting input of the comparator has a constant voltage. This facilitates the offset cancellation of the comparator, by proper bias of this input.

Equation 6.7 [36] is derived from the basic operation of the successive approximation ADC. Where, D is the digital code generated by the successive approximation register, and Vref is the upper limit of the input dynamic range. In that reported architecture, n comparators, n(n+3) resistors, and (n-1) output buffers are used to form the n-bit ADC. These components increase the power consumption and silicon area. Equation 6.8 is a recursive equation, where the bits are calculated from the MSB

down-to the LSB. Each bit uses the information of previously calculated bits. The output is taken in parallel and is ready after the last bit is calculated.

$$\frac{V_{in} + \overline{D}V_{ref}}{2} <> \frac{2^n - 1}{2^{n+1}} V_{ref} \tag{6.8}$$

Based on the described concept of inherent subtraction [36], a compact architecture is proposed here to decrease the ADC area by reducing the number of components and reduce its power consumption. In this architecture and for n-bit ADC, only one comparator, one resistor ladder with (2n+2) resistors and (2n-1) switches, and a simple digital controller are used. Fig. 6.22(a) shows the architecture for the 7-bit ADC. The control signals for the switches are time shifted pulses as shown in Fig. 6.23. Its generation is done using a 3-bit binary counter with a simple 3-to-8 decoder. This generates the 7 control signals and the EOC (End Of Conversion) pulse. The employed comparator used follows the architecture of an input stage, a regenerative comparator, and an SR latch proposed in [37].

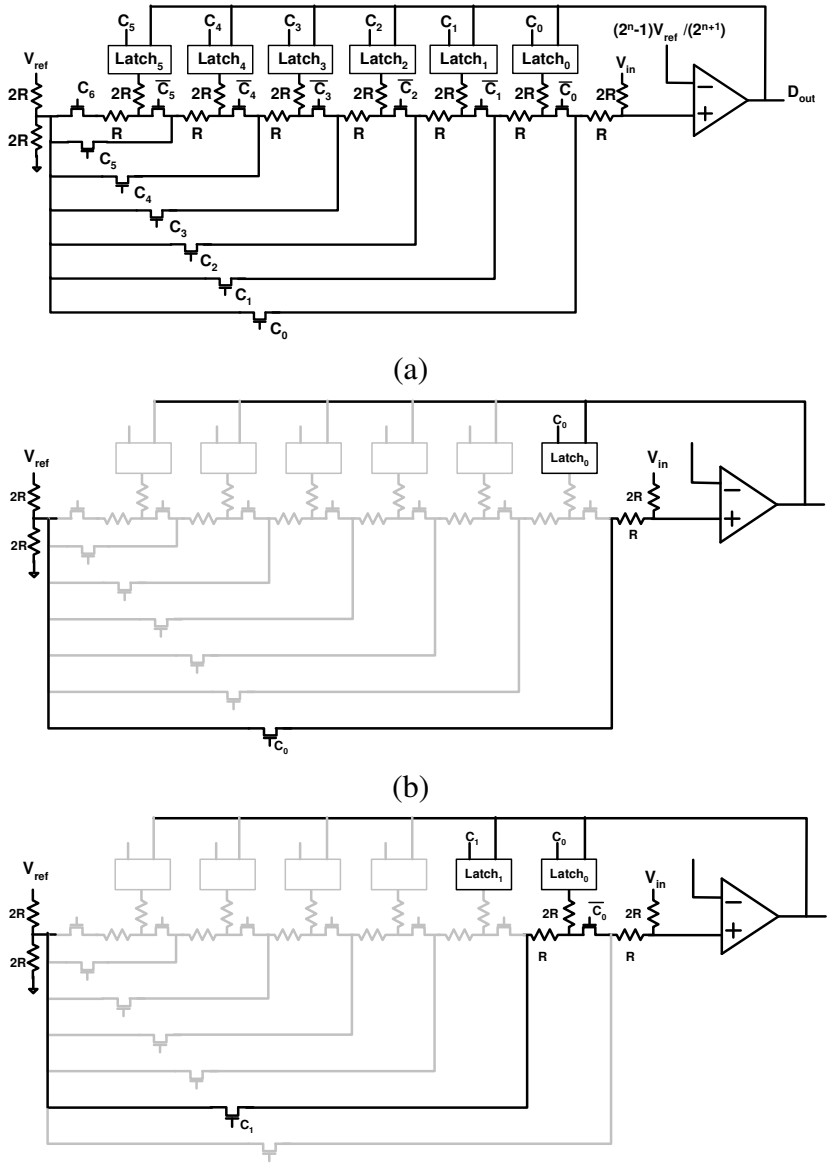


Fig. 6.22 Successive approximation ADC and its operation. (a) Proposed ADC architecture. (b) MSB detection. (c) 2nd bit detection

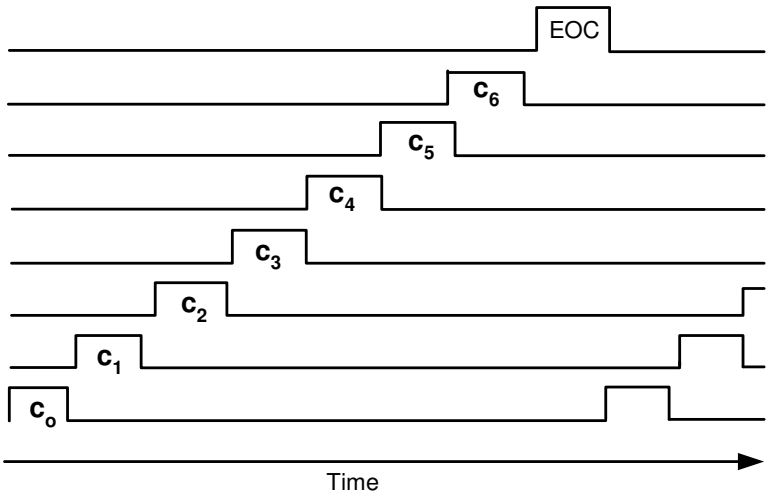


Fig. 6.23 Control signals for the ADC

Equation 6.9 represents the general operation of the proposed ADC using different control lines to generate the different bits in a recursive manner.

$$D_i = \begin{cases} 1 \; if \; \dfrac{v_{in}}{2} + \left[\dfrac{\overline{D}_7 V_{ref}}{4} + \dfrac{\overline{D}_6 V_{ref}}{8} + \; \ldots \; + \dfrac{\overline{D}_{i+1} V_{ref}}{2^{8-i}} \right] + \dfrac{V_{ref}}{2^{9-i}} > \left(\dfrac{2^n - 1}{2^{n+1}} \right) V_{ref} \\ 0 \;\; otherwise \end{cases}$$

$$where \; i = 7,6,...,1 \; and \; D_i = 1 \forall \, i > 7 \tag{6.9}$$

The MSB is generated by comparing the input signal with half the input dynamic range. While the second bit can be detected using information of the first bit, and so on untill the LSB is detected. The digital bits are calculated one at a time and the output is taken serially in this case (MSB down-to LSB). By changing the status of the control signals, the resistor ladder is reshaped to calculate the corresponding bit. Fig. 6.22(b) and (c), shows the first and the second time intervals to calculate the first and the second bits respectively. Thus 8 clock periods are needed for a complete conversion process.

Due to its reduced number of components, this ADC architecture can make use of the existing circuitry in an IC compliant with the IEEE 1149.1 standard for a mixed-signal test bus [38]. In this standard, each test pin has an Analog Boundary Module (ABM) through which its DC voltage can be set, shorted to the supply, or compared with a threshold and latched as a logic value by the boundary scan test. The ABM has a comparator, switches and a set of storage cells (Flip Flops) [38]. By introducing a small programmability, these components can be used together with an resistor ladder to form this compact ADC for DC signals using only one ABM. This modification in the ABM leads to more accurate results in testing, where each pin value is digitized (n-bit ADC) rather than compared with a single threshold (1-bit ADC). The proposed ADC operates up to 100KHz clock frequency corresponding to 12.5KHz conversion rate. Large resistor values are used in the resistor ladder (150KΩ) to make the switch ON-resistance as negligible as possible, thus preserving on accurate resistance ratios and consequently accurate calculations and better performance. If the conversion speed needs to be increased, the ladder parasitic poles should be pushed to higher frequencies. This can be done by decreasing the resistor values and increasing the switch size or using a transmission gate switch.

6.6. Experimental results for the on-chip test system

The proposed system is implemented in standard TSMC CMOS 0.35μm technology and fabricated through the MOSIS service. Two different 4^{th} order OTA-C filters are included as CUTs; a bandpass filter (BPF) with a center frequency of 11MHz and a low-

pass filter (LPF) with a cutoff frequency of 20MHz. These filter's characteristics are common in the baseband section of communication systems. The chip microphotograph is shown in Fig. 6.24. The total area of the testing circuitry (frequency synthesizer, ADC and APD) is $0.3mm^2$.

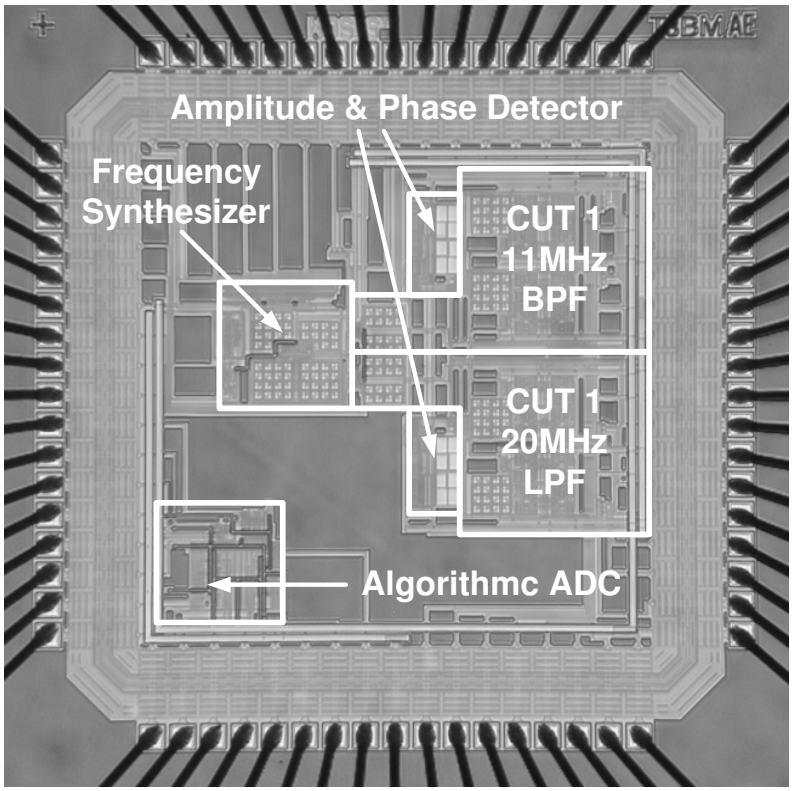


Fig. 6.24. FRCS chip microphotograph

Fig. 6.25 shows a photograph of the PCB employed for the evaluation of the prototype IC, with exception of the ADC which was mounted on a separate PCB. The

next subsections discuss the measurement results for each component of the system as well as for the on-chip test of the integrated CUTs.

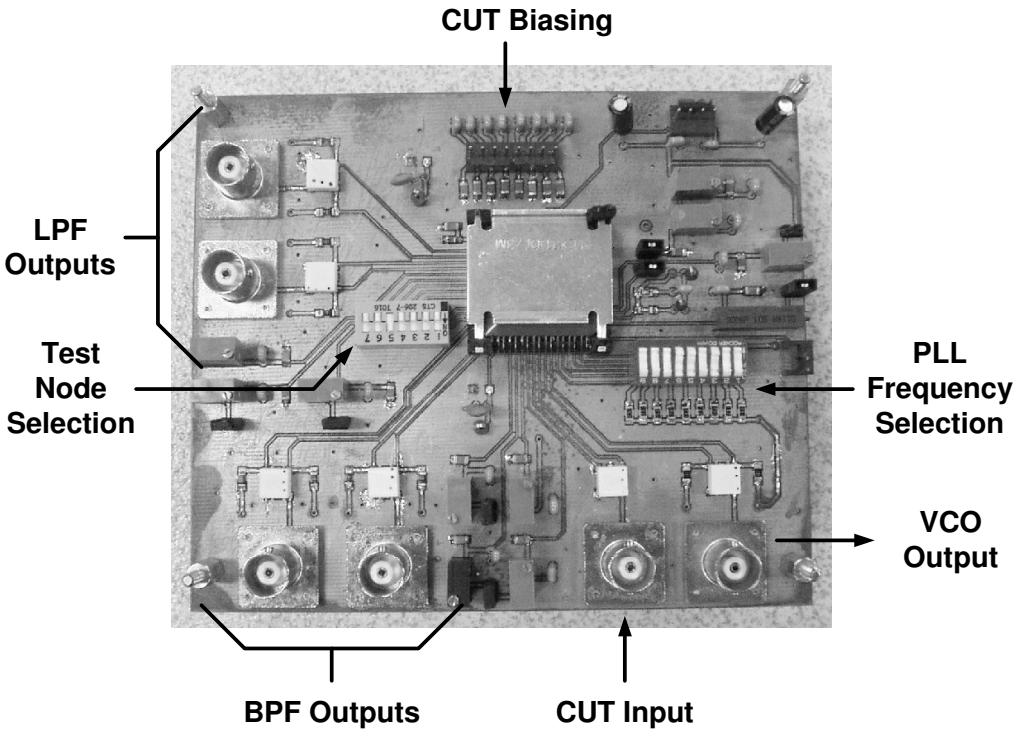


Fig. 6.25 Photograph of the PCB employed for the evaluation of the FRCS

The performance of the stand-alone APD is evaluated using external signal generators for frequencies up to 130MHz. The relative difference between the amplitude of two signals can be measured in a range of 30dB with an error of less than 1dB. The relative difference in phase can be measured with an average error of less than 1º. The

complete APD with the input demultiplexer occupies an area of 310µm×180µm and draws 3mA from the 3.3V supply.

6.6.1 VCO and frequency synthesizer

Experimental results for the VCO are shown in Figs. 6.26 and 6.27 The output frequency varies from 0.5 to 140MHz and the amplitude variations are within 3.5dB. Fig. 6.28 presents the harmonic distortion measurements for an output frequency of 15MHz. Throughout the tuning range, the harmonic distortion components are always below -20dBc. According to the analysis presented in section II, this harmonic distortion would cause relative errors in the magnitude and phase measurements of less than 1%.

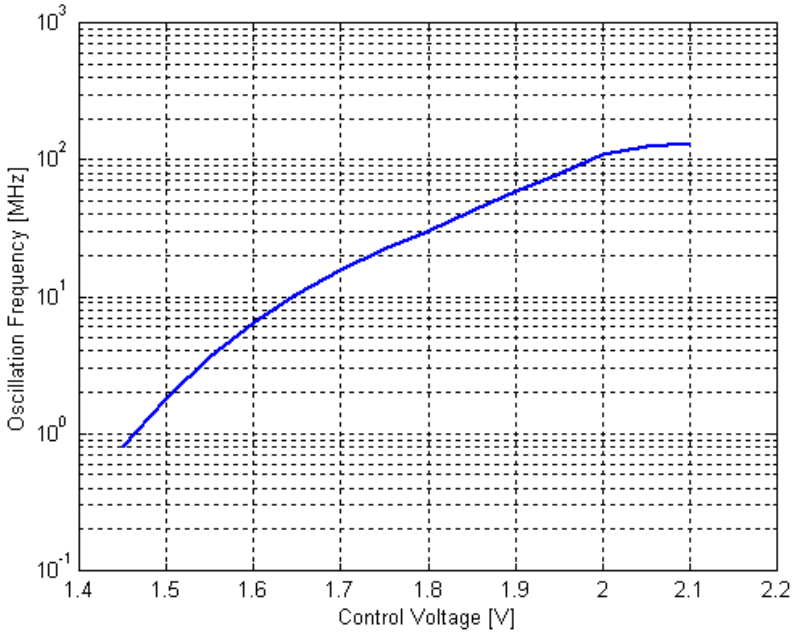


Fig. 6.26 Tuning range of the VCO in the integrated test system

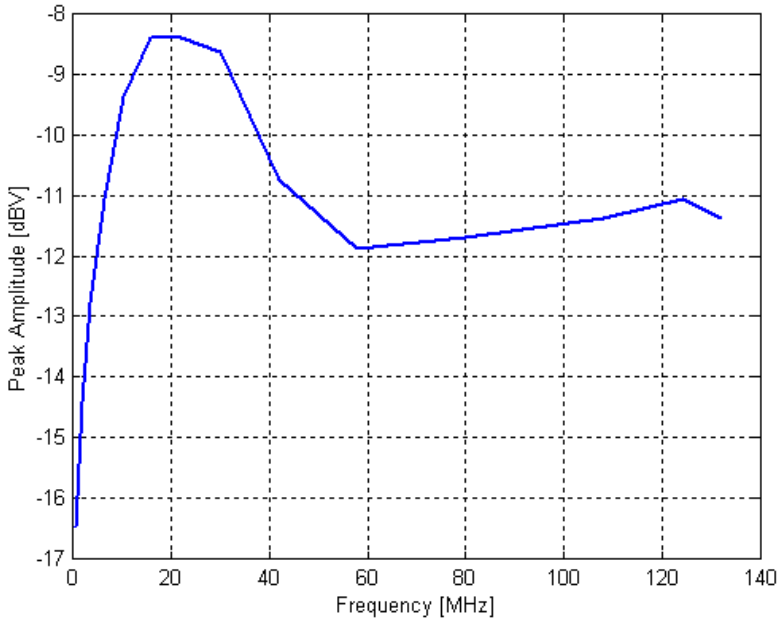


Fig. 6.27 Measured VCO amplitude over its tuning range

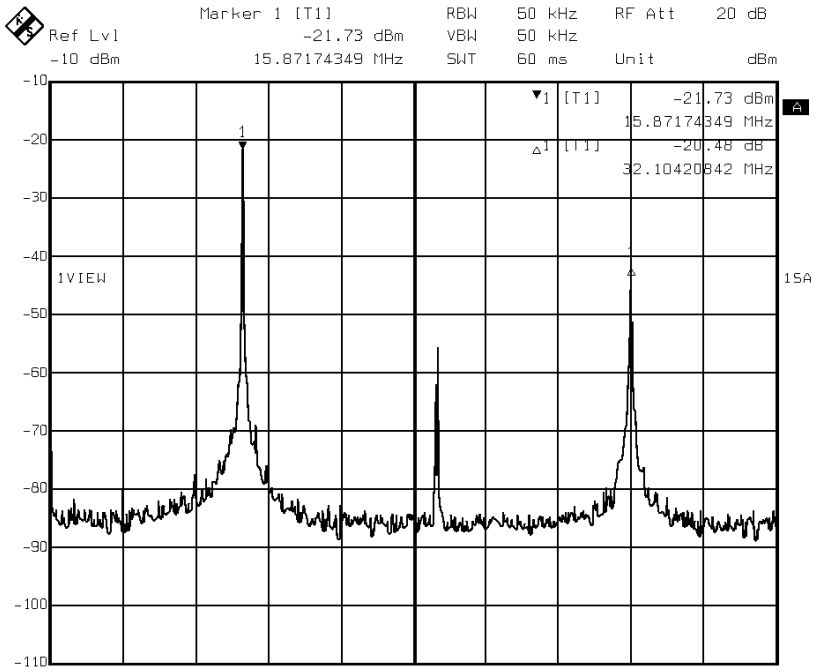


Fig. 6.28 Output spectrum of the on-chip signal generator

The complete frequency synthesizer is operated with a reference frequency of 1MHz and through the 7-bit programmable counter covers a range from 1 to 128MHz in steps of 1MHz. The output spectrum of the PLL in the locked state at 128MHz is shown in Fig. 6.29. The reference spurs are below -36dBc. The area of the entire synthesizer is 380μm×390μm and the current consumption changes from 1.5 to 4mA as the output frequency increases.

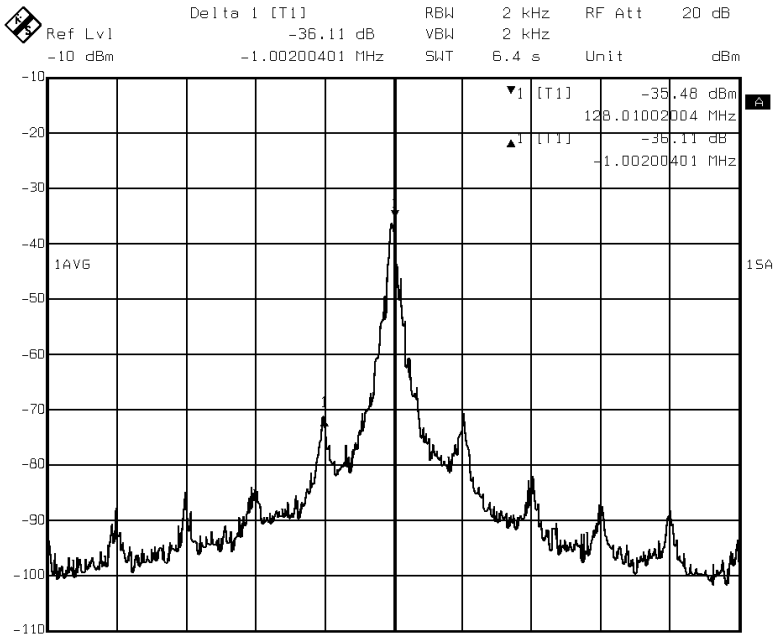


Fig. 6.29 PLL output spectrum in the locked state at 128MHz

6.6.2 Analog-to-digital converter

For the test of the ADC, a 2-v input dynamic range (0.65-v to 2.65-v) is considered. Fig. 6.30 shows the measured peak INL and DNL Vs. input clock frequency. The ADC

operates at a 100KHz clock frequency (80μsec conversion time) with a peak INL of 1.4 LSB and a peak DNL of 0.45 LSB. Fig. 6.31 shows an oscilloscope screen capture showing the End of Conversion signal, the 10KHz clock signal and the serial output data for a DC input signal of 2.07 V. An average power of 200 μW is consumed by the ADC and its area is 380μm×390μm.

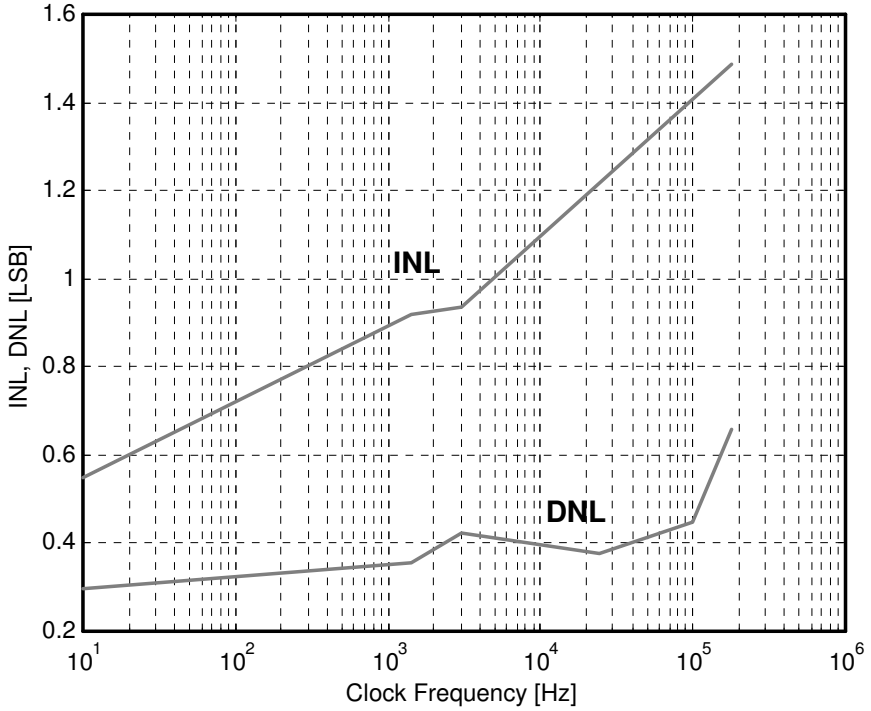


Fig. 6.30 INL and DNL of the ADC versus clock frequency

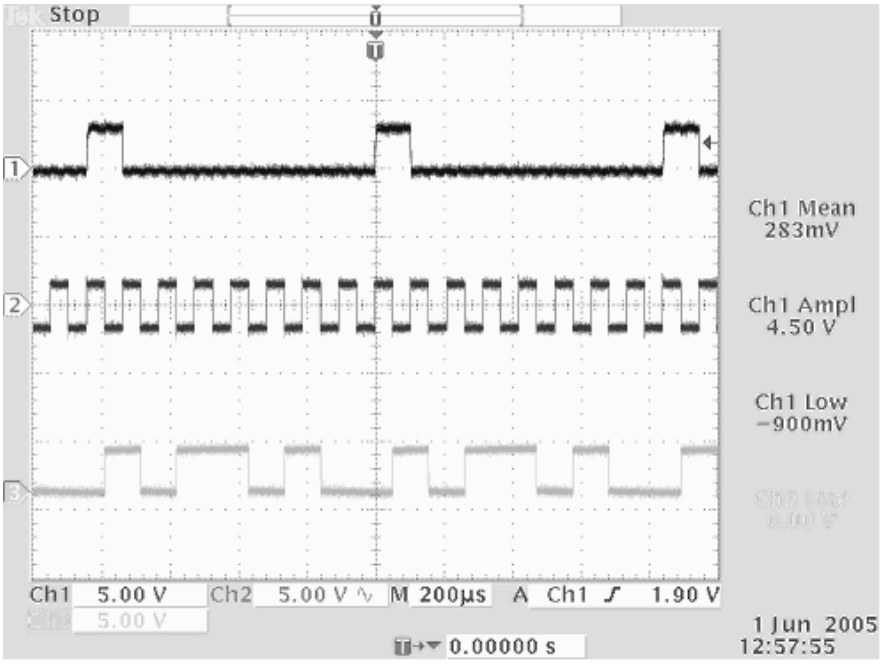


Fig. 6.31 EOC, CLK, and serial output data of the ADC

6.6.3 Evaluation of the complete system in the test of CUTs in the same chip

Fig. 6.32 describes the experimental setup for the evaluation of the entire system in the test of the integrated CUTs. Each 4th order filter consists of two OTA-C biquads, and each biquad has two nodes of interest, namely bandpass (BP) node and lowpass (LP) node. Nodes 2 and 4, the outputs of the biquads, are BP nodes in the 11MHz BPF (CUT 1) and LP nodes in the 20MHz LPF (CUT 2). Buffers are added to the output node of each biquad so that their frequency response can be evaluated with an external network analyzer.

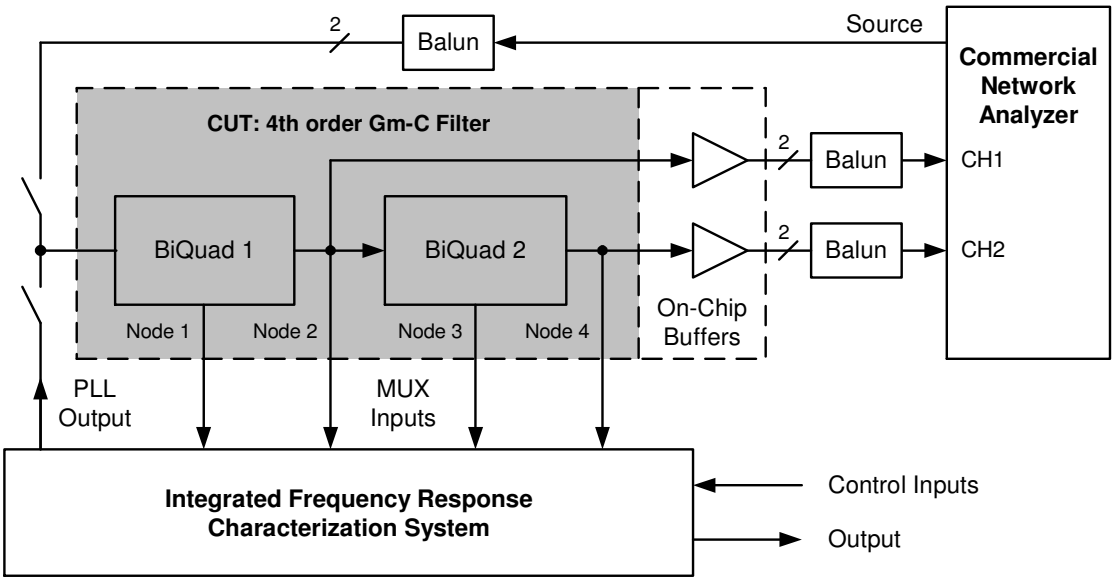
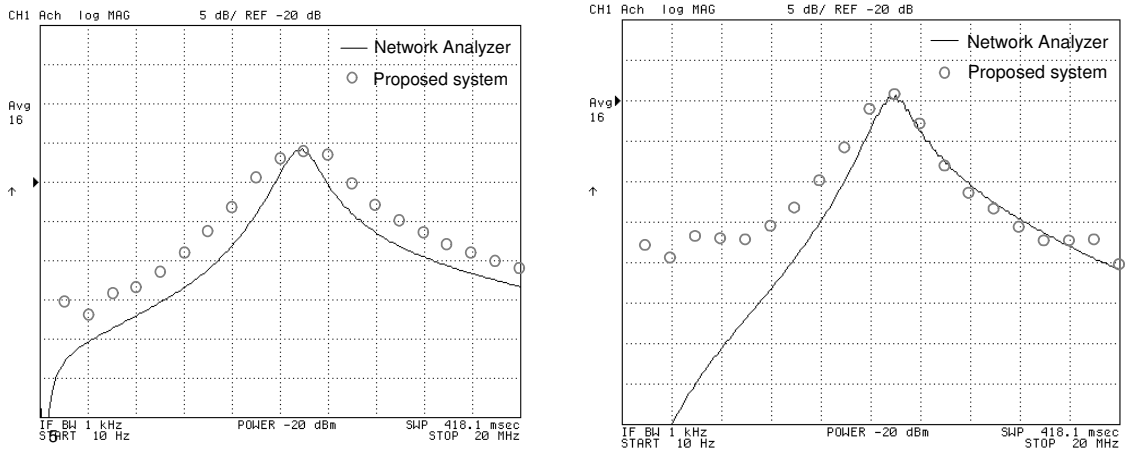


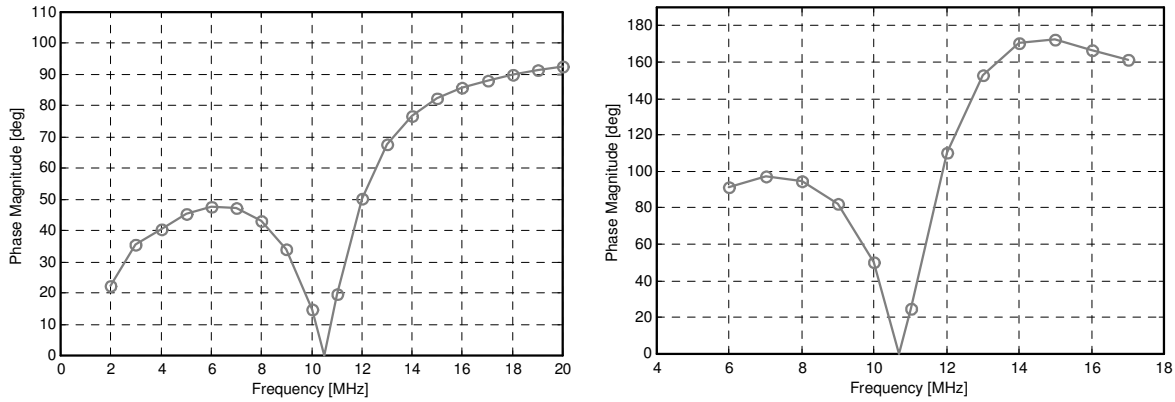
Fig. 6.32. Experimental setup for the evaluation of the FRCS

The results of the operation of the entire FRCS in the magnitude response characterization of the 11MHz BPF at its two BP outputs are shown in Fig. 6.33. These results are compared against the characterization performed with a commercial network analyzer. In this measurement, the dynamic range of the system is limited by the resolution of the ADC to about 21dB. The phase response of the filter as measured by the FRCS is shown in Fig. 6.34



(a) (b)

Fig. 6.33 Magnitude response test of the 11MHz BPF. (a) Results for the first biquad (2^{nd} order filter). (b) Results for the complete 4^{th} order filter

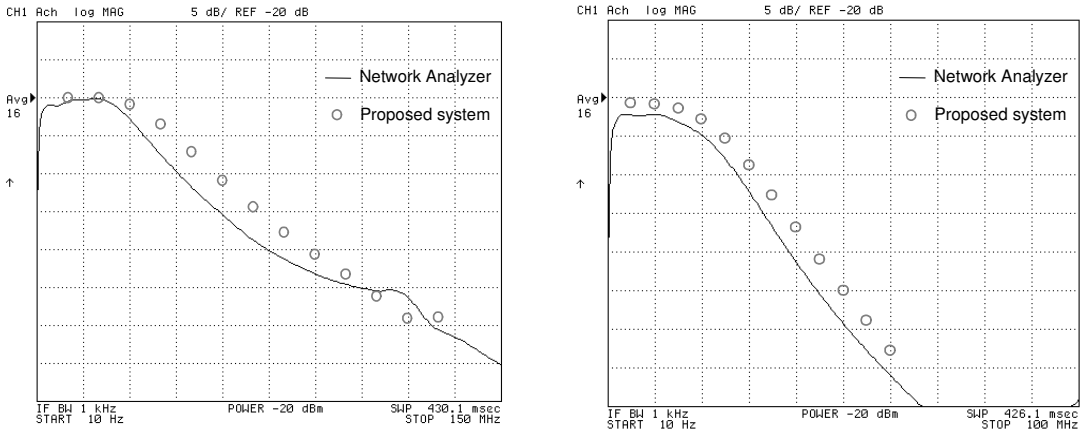


(a) (b)

Fig. 6.34 Phase response test of the 11MHz BPF. (a) Results for the first biquad (2^{nd} order filter). (b) Results for the complete 4^{th} order filter

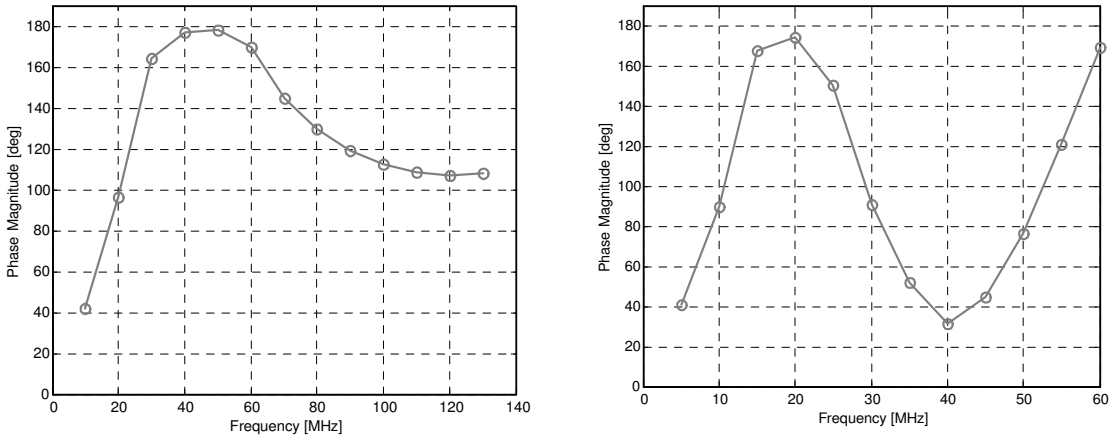
The corresponding results for the characterization of the 20MHz LPF are presented in Figs. 6.35 and 6.36 In this case, the DC output of the APD is measured through a data acquisition card with an accuracy of 10 bit. As it can be observed, the APD is able to

track the frequency response of the filter and perform phase measurements in a dynamic range of 30dB up to 130MHz.



(a) (b)

Fig. 6.35 Magnitude response test of the 20MHz BPF. (a) Results for the first biquad 2nd order filter). (b) Results for the complete 4th order filter



(a) (b)

Fig. 6.36 Phase response test of the 20 MHz BPF. (a) Results for the first biquad (2nd order filter). (b) Results for the complete 4th order filter

On average, in the test of both CUTs, the magnitude response measured by the off-chip equipment is about 2dB below the estimation of the FRCS. This discrepancy is mostly due to the loss of the employed buffers and baluns. Table 6.4 presents the performance summary of the proposed test system.

Table 6.4 FRCS performance summary

Technology	TSMC 0.35μm CMOS
Dynamic range for measurement of magnitude response	30dB
Resolution for phase measurements	1 deg
Frequency Range	1-130MHz
Digital Output Resolution	7 bits
Supply	3.3 V
Power Consumption (at 130MHz)	20mW
Area	0.3 mm^2

Table 6.5 presents an area overhead analysis for the FRCS with respect to reported analog systems which are suitable CUT candidates. Note that this area comparison is a pessimistic estimation since it is made with respect to circuits that are fabricated in technologies with smaller minimum feature sizes.

Table 6.5 Area overhead analysis for the FRCS

Reference	System	Technology	Area	Overhead of FRCS
[39]	IF Baseband strip for GSM	0.25μm CMOS	1.9 mm^2	15.8%
[40]	2 MHz IQ receiver for Bluetooth	0.18μm CMOS	5.6mm^2	5.4%
[41]	Line driver for ADSL	0.25μm CMOS	5.3mm^2	5.7%

In order to place the achieved results into perspective, Table 6.6 presents a summary of the on-chip testing techniques that have been so far (up to the author's knowledge) demonstrated experimentally with integrated prototypes. The mixed-signal test core presented in [42] is versatile, mostly digital and has the advantage of capturing signals in the GHz range through sub-sampling. Nevertheless, due to the use of oversampling techniques for its signal generator, frequency response measurements with this system are limited to only a fraction of the employed clock frequency (20MHz). It is also important to mention that the required analog filter for the signal generator is not included in the reported area and that supplemental FFT processing is required to perform the frequency response characterization [42]. Oscillation based test (OBT) is a well documented strategy in the literature [5]. The CUT is re-configured in an oscillation mode and its performance is estimated from the characteristics of the obtained signal; [43] presents a technique to evaluate the characteristics of the output waveform from the CUT on-chip. The on-chip spectrum analyzer presented in [44] has the advantage of performing harmonic distortion measurements in addition to frequency response characterizations. The use of switched capacitor techniques improve the robustness of the system but limit its application to the range of few MHz.

Table 6.6 Current state-of-the-art in integrated solutions for analog test

Reference	System	Functions	Technology	Area
[42]	Integrated Mixed-Signal Test Core	Frequency response, DC transfer characteristic and THD measurements at a clock speed of 20MHz. Capture of analog signals through sub-sampling at an effective sampling rate of 4GHz.	0.35µm CMOS	0.67 mm^2
[43]	On-Chip Evaluation of Oscillation-Based Test	Extraction of the amplitude, frequency and DC level from the output of a CUT in oscillation mode. Demonstrated on an integrated CUT for an oscillation frequency < 1KHz .	0.6µm CMOS	?
[44]	Switched Capacitor Spectrum Analyzer	Measurement of frequency response and harmonic distortion. Demonstrated up to 10KHz on an off-chip CUT.	0.5µm CMOS	0.5 mm^2
This Work	Frequency Response Characterization System	Measurement of magnitude and phase responses over frequency through a digital interface. Demonstrated up to 130MHz on integrated CUTs	0.35µm CMOS	0.3 mm^2

CHAPTER VII

CMOS RF RMS DETECTOR FOR BUILT-IN TESTING OF RF CIRCUITS

Most of the reported testing techniques for RF circuits have focused on the early detection of catastrophic faults as well as on the time and cost reduction of the overall system verification [45-47]. However, the characterization of individual building blocks is desirable to detect parametric faults, improve the fault coverage and accelerate the product development phase. Towards this end, BIT techniques are potentially useful, even though their implementation becomes especially difficult for RF circuits. The embedded testing of RF components through alternate test has been explored recently [48-49]. Moreover, in [50-51], the use of embedded RMS detectors has been shown to be an effective method to test a receiver at the board level.

7.1 Transceiver testing through on-chip RMS detection

RF RMS detectors [52] and RF power detectors [53-54] generate a DC voltage proportional to the amplitude and power of an RF signal, respectively. By using them, the main performance metrics of RF circuits such as gain, output power and 1dB compression point can be tested with reasonable accuracy by measuring DC voltages. These testing devices have been employed as key components of a low-cost tester architecture for an RF system [51] and their use in the embedded test of a receiver with discrete components has also been explored [50].

For the embedded test of the RF blocks in an integrated transceiver, to include on-chip buffers to monitor the RF signal paths through an external spectrum or network analyzer is not a practical test strategy. The cost of the required equipment and the area overhead due to the extra circuitry and output pads would be unaffordable. Therefore, it is desirable to have an on-chip RMS detector to monitor the voltage magnitude of RF signals through DC measurements. Such a testing device can enable the functional verification of the RF blocks in a system using a low-cost tester and/or analog-to-digital conversion and digital processing circuitry available on-chip. Multiple nodes could be observed from a single output pad since DC voltages can be multiplexed easily.

To use power dividers to connect matched RMS detectors to the RF signal path as in the example shown in [50] might not a suitable option to test an integrated transceiver since the performance is affected and the power dividers require extra area. The desired characteristics of a practical integrated RF RMS detector should be: (1) A high input impedance at the frequency of test to prevent loading and performance degradation of the RF circuit under test. (2) Minimum area overhead. (3) A dynamic range suitable for the target building blocks. Other figures of merit such as power consumption and temperature stability are not a priority since the RMS detector will not be used during the normal operation of the system under test. A conceptual description of the proposed RF test strategy through an embedded RMS detector is shown in Fig. 7.1.

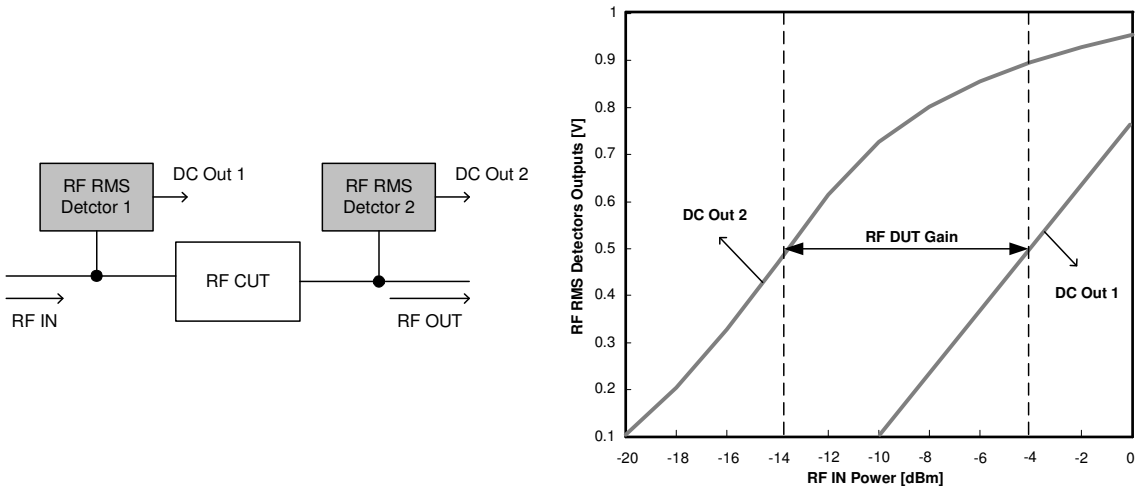


Fig. 7.1 Conceptual description of the proposed technique for on-chip RF testing

7.2 Gain and 1dB compression point measurement with RMS detectors

To illustrate the proposed method to measure the gain and 1dB compression point of an integrated RF device, a macromodel is built and simulated in SystemView. The model of the RF RMS detector consists of an amplifier with high input impedance followed by a half-wave rectifier and a 2nd order low-pass filter (see Fig. 7.3 in the next section). Two different LNA models are considered as circuit under test. LNA1 has a gain of 10dB, output 1dB compression point of -3dBm, output IP3 of 7dBm and noise figure of 4dB. LNA2 represents a faulty LNA with a gain of 8dB, output 1dB compression of -5dBm and the same IP3 and NF as LNA1. An RF RMS detector is used at the input of the LNA and another at the output (as in Fig. 7.1). The amplitude of the sinusoidal signal at the input of the LNA (and the first detector) is swept from -20 to 0dBm in steps of 2dB. Fig. 7.2 shows the simulation results. For a given input amplitude, the gain of the LNA can be measured as the distance in dB from the response

of the detector at the output to the reference response (output of the detector at the input). As it can be observed, the input amplitude (and corresponding output amplitude) for which the gain decreases by 1dB can be easily extrapolated.

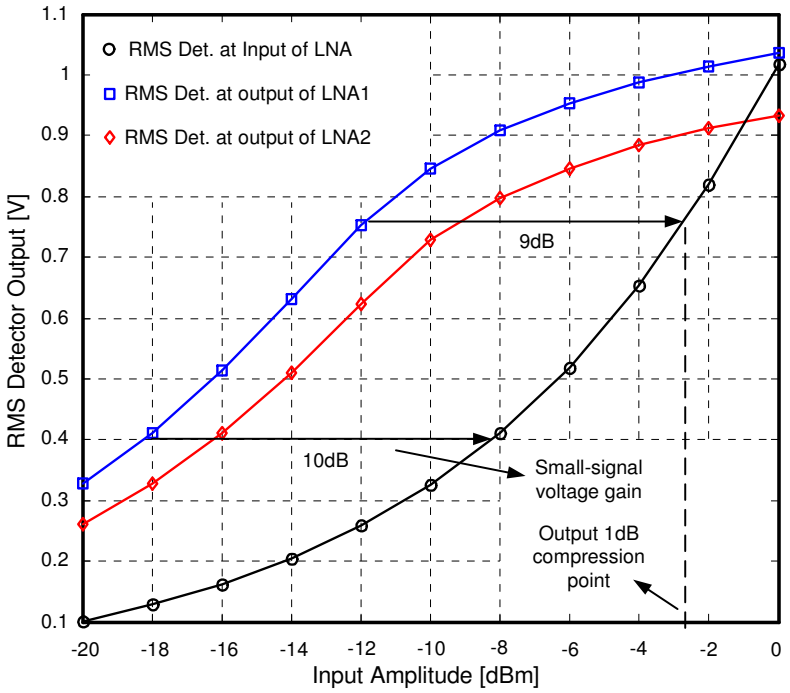


Fig. 7.2 LNA test example

It is important to note, that with the use of the reference response, the absolute gain and the nonlinearity of the RMS detector response do not affect the characterization. In this way, process variations do not affect the measurement accuracy significantly. The mismatch between the gains of the different detectors would be the only remaining source of error. It is also important to mention that the DC offset that may be present at

the output of the detectors is not a matter of concern since it can be measured (when no signal is present at the input) before the characterization process.

7.3. CMOS RF RMS detector design

CMOS technology has been preferred for the implementation of most commercial wireless transceivers due to its lower cost and the possibility to integrate the RF/Analog front-end and the digital base-band on a single chip. Previously reported circuits for RF to DC conversion using bipolar transistors have obtained relatively high accuracy and dynamic range [52, 53]. However, purely CMOS solutions are necessary. The first RF power detector on silicon using a MOSFET was reported in [54]; it requires an area of $1mm^2$ and achieves 25dB of dynamic range. A 450 MHz power detector in CMOS 0.35μm technology is described in [55]; it has a high dynamic range (50dB) and uses $0.5mm^2$. Due to their relatively large area, among other considerations, none of these previously reported RF to DC converters are suitable options for on-chip testing applications.

The proposed RF RMS detector consists of three stages; a conceptual block diagram is depicted in Fig 7.3. The first stage presents a high-impedance to the RF signal path, converts the sensed voltage to a current signal, and amplifies it. The second stage is a half-wave rectifier. The rectified waveform is filtered in the last stage to obtain its average value. The output is then a DC voltage proportional to the amplitude of the RF signal at the input of the detector.

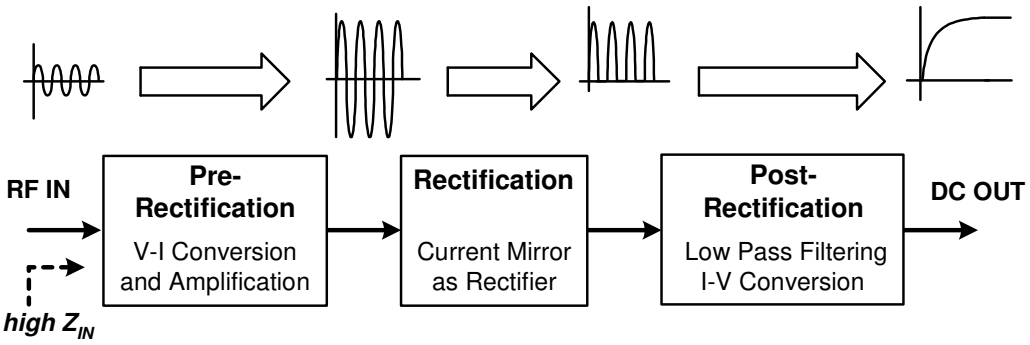


Fig. 7.3 Block diagram of the RF RMS detector

The target frequency of operation for this design is 2.4 GHz, since this is the ISM band employed by widely used wireless standards such as Bluetooth, 802.11b/g and 802.15.4. The circuit schematic for the proposed RF testing device is shown in Fig. 7.4. The DC current mirrors employed for the generation of the bias currents are not shown for simplicity. Next the design considerations for each stage are described in detail.

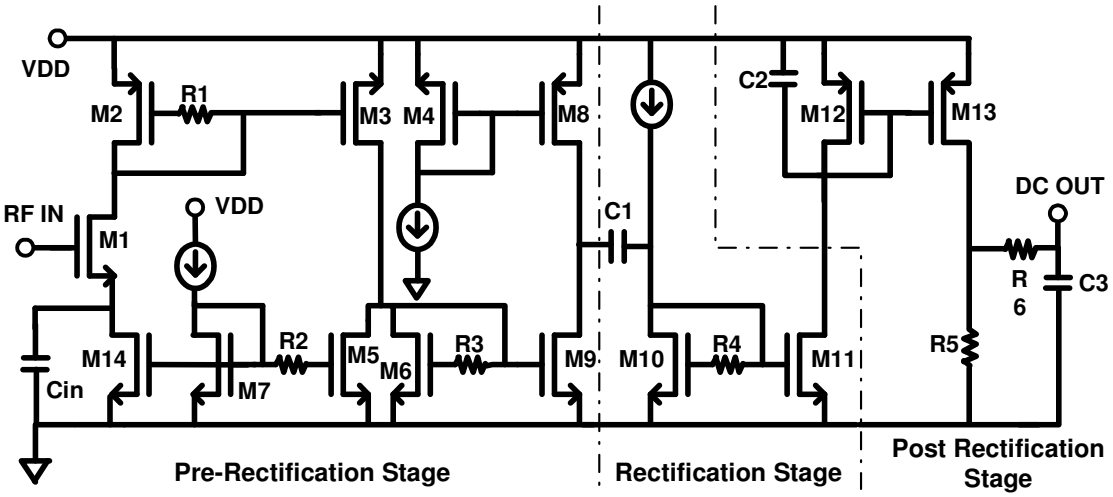


Fig. 7.4 Schematic of the proposed RF RMS detector

7.4.1 Pre-rectification stage

The pre-rectification stage acts as a transconductor. Transistor M1 performs the voltage to current conversion and it is followed by a PMOS (M2, M3) and an NMOS (M6, M9) current amplifiers. The current amplification is needed since the input transistor cannot provide the required transconductance for proper rectifying action and low input capacitance at the same time. Transistor M14 provides a constant DC bias current for M1, in this way, the operating point of the input transistor becomes independent (for most of the supply voltage range) from the DC voltage at the RF node to be observed. The capacitor Cin is placed to reduce the effective source degeneration impedance at RF frequencies. Resistors R1 and R3 are employed to enhance the bandwidth of the current amplification (according to the technique described in [56]) and make their operation at 2.4GHz possible. A DC current subtractor (M5) is used in the intermediate stage to minimize the unwanted DC current magnification.

7.4.2 Rectification stage

The basic rectification stage is a NMOS current mirror formed by transistors M10 and M11, its operation is described in detail in Fig. 7.5. M10 is biased with a small DC current source so that it is always in the weak inversion region. This reduces the time for the re-formation of the channel, enhancing the speed of the rectification. During the positive cycle, the AC current coming from the coupling capacitor C1 moves M10 to the saturation region (i.e. the transistor is turned on). This current is mirrored and amplified

through M11, which is now also operating in saturation region. The parasitic capacitances (Cpar) get charged during this cycle. During the negative cycle, M10 and M11 go to the cut-off region (off state) and the AC current is extracted from the bias current and Cpar. A significant current swing is observed at the output only during the positive cycle and, in this way, half-wave rectification is accomplished.

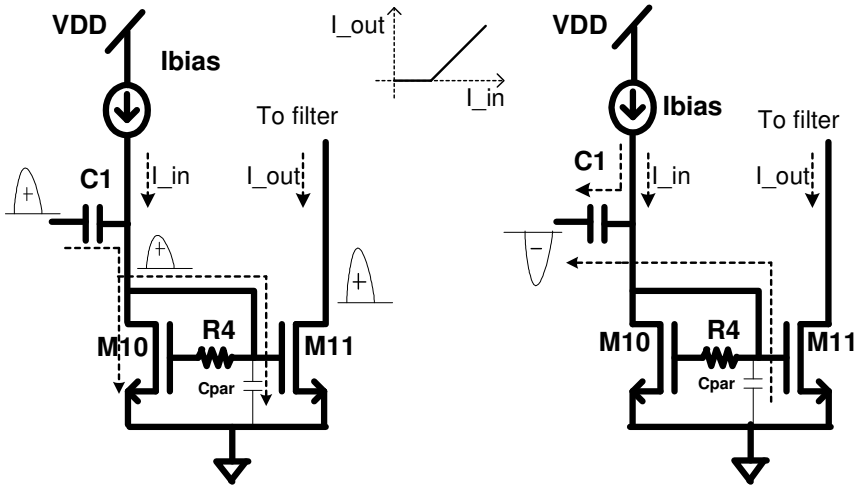


Fig. 7.5 Rectifying action: positive cycle (left) and negative cycle (right)

7.4.3 Post-rectification stage

The post-rectification stage consists of a second order low-pass filter with current to voltage conversion. The first pole is implemented in the PMOS current mirror load with M12 and C_2. R_5 provides the current to voltage conversion while R_6 and C_3 provide the second. For the design of these passive components, a compromise exists between the time constant of the settling response and the ripple in the output voltage. The settling

time of the detector is an important criterion since it will impact the overall testing time. Pole locations in the order of 10MHz were chosen to guarantee (under normal process variations) a settling time of less than 50ns with less than 1% of ripple in the output voltage. It is important to note that since the RF signal processing is done in current throughout the detector, the voltage swings are kept relatively small, which reduces the amount of substrate noise injection.

7.5. Post-layout simulation results

The layout of the proposed RMS detector in standard CMOS 0.35µm technology is depicted in Fig. 7.6. The employed area is only 150µm by 90µm. The passive resistors are realized using N-Well to reduce the area and substrate stray capacitance. Guard rings are added to shield substrate noise.

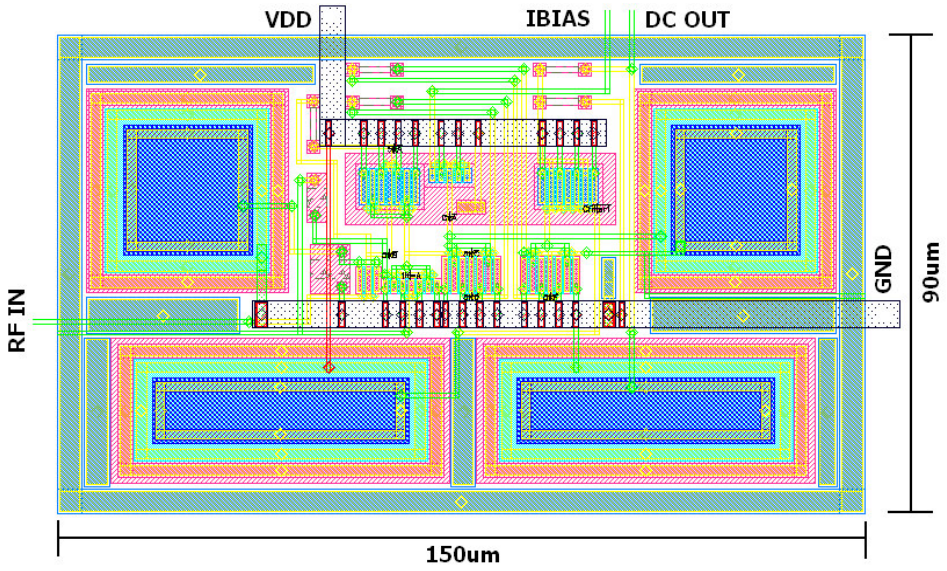


Fig. 7.6 Layout of the CMOS RF RMS detector

After the extraction of the layout with parasitics, post-layout simulations were performed using Cadence SpectreS. The transient simulation results presented in this section are for input signals at 2.4GHz. As discussed earlier, the effective input impedance of the RMS detector must be large to avoid affecting the performance of the circuits under test. As shown in Fig. 7.7, the RMS detector (including the parasitics of the input connection) presents an equivalent input capacitance of 22.5 fF, which represents more than 2.5Kohms at 2.4GHz.

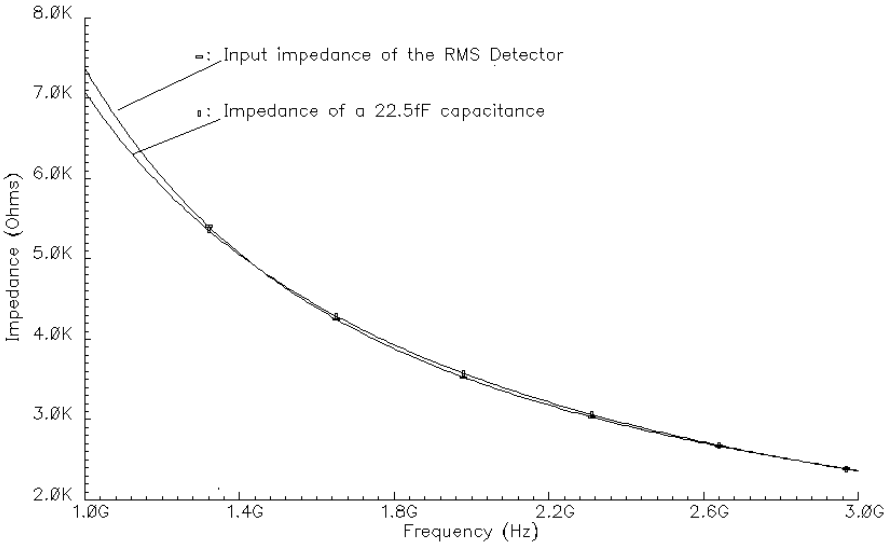


Fig. 7.7 RMS detector input impedance

Fig. 7.8 shows the RF input Vs. DC output response of the RMS detector. The X axis represents the RMS input voltage amplitude normalized to power in dBm with respect to 50ohms. A straight line is superimposed as reference of a linear transfer characteristic.

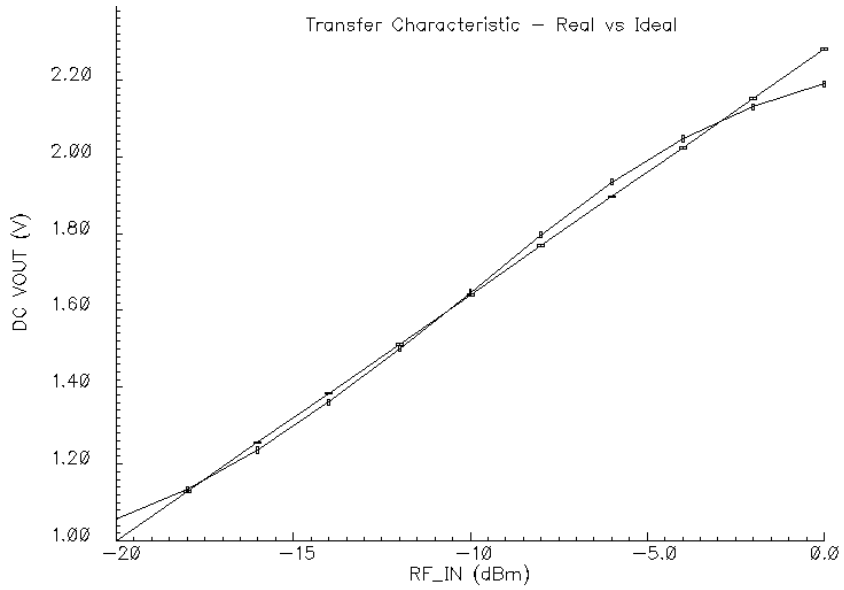


Fig. 7.8 DC output vs. input amplitude

The relative error of the output voltage with respect to the linear characteristic is given in Fig. 7.9. The dynamic range of the RMS detector for a deviation of less than 5% with respect to the linear response is -20dBm to 0dBm (20mV to 200mV approx.). Front-end building blocks for transceivers typically show gain compression within this range. For example, the LNA in [57] shows an output 1dB compression point of -3dBm. The noise floor of the detector is in the range of microvolts and therefore does not limit the dynamic range. The settling behavior of the RMS detector for different input voltage amplitudes is given in Fig. 7.10. A settling time of less than 40ns is achieved while the ripple at the output voltage is less than 1mV.

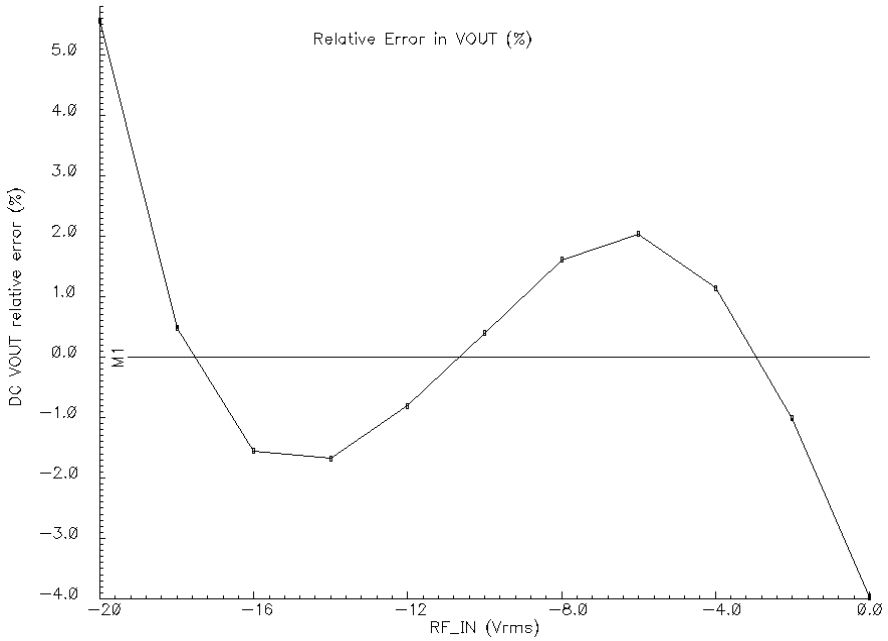


Fig. 7.9 Relative output error of the RF detector

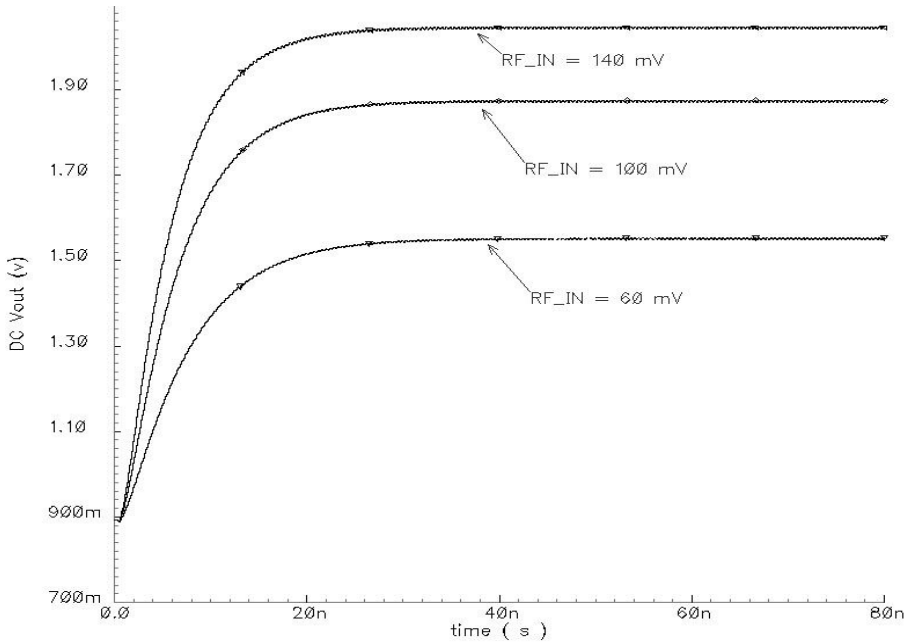


Fig. 7.10 Settling behavior of the RMS detector

The area overhead of one RMS detector with respect to two receiver implementations and different building blocks of a transceiver is given in Table 7.1. For an appropriate comparison with the proposed circuit, only implementations in CMOS 0.35µm technology were selected from the literature [58-62]. From this analysis it can be concluded that, in general, the use of ten RMS detectors in different test points would result in an area overhead of around 2% for an entire transceiver.

Table 7.1 RMS detector area overhead analysis

Reference	Description	Area [mm^2]	Overhead of 1 RMS Det.
[58]	Bluetooth Receiver	6.25	0.22%
[59]	Power Amplifier	2.60	0.52%
[60]	GPS Front-End	0.84	1.6%
[61]	CDMA Frequency Synthesizer	5.00	0.27%

Table 7.2 gives the performance summary of the RMS detector. It is worth to mention that the dynamic range of this RMS detector is comparable to the one of a commercial stand-alone power detector implemented with bipolar transistors [62].

Table 7.2. RMS detector performance summary

Technology	TSMC 0.35µm
Area	0.0135mm^2
Gain	60mV/dBm
Linear Dynamic Range	20dB
Supply Voltage	3.3 V
Power Consumption	10mW
Settling time	<40ns

CHAPTER VIII

BUILT-IN TESTING ARCHITECTURE FOR WIRELESS TRANSCEIVERS

In the contemporary competitive market, the incorporation of a comprehensive testing strategy into the design flow of a wireless module is indispensable for its timely development and economic success [47, 51, 63]. Modern transceivers are highly integrated systems. The diverse nature of their specifications and components, as well as the ever increasing frequencies involved, makes their testing progressively more complex and expensive. To increase the effectiveness and cost efficiency of analog and RF tests in integrated systems is a wide problem that has been addressed at different levels. Recent efforts span defect modeling, development of algorithms for automated test, functional verification through alternate tests, design for testability (DfT) techniques [45, 64], and built-in testing (BIT) techniques [46, 65].

In particular, BIT can become a high impact resouce due to the following reasons: (1) To reduce the complexity and cost of the external automatic test equipment (ATE) and its interface to the device under test (DUT) it is desirable to move some of the testing functions to the test board and into the DUT itself [51, 63], (2) the increase in packaging costs demands “known good die” (KGD) testing solutions that can be implemented at the wafer-level [46] and, (3) BIT can offer fault diagnosis capabilities (i.e. to identify a faulty block in the system) which provide valuable feedback for yield enhancement, thus accelerating the development of the product. Nevertheless, several

challenges such as robustness, transparency to DUT operation and area overhead must be overcome to make the use of BIT effective for systems with RF/Analog components.

This chapter presents an integral testing strategy for integrated wireless transceivers with basis on the BIT techniques discussed in Chapter VI and Chapter VII and a loop-back architecture. The objective is to enable the characterization of the major performance metrics of the transceiver and its building blocks at the wafer level avoiding the use of RF instrumentation. Fig. 8.1 illustrates this approach. The embedded testing devices communicate with the ATE through an interface of digital signals and DC voltages. From the extracted information on the transceiver performance at different intermediate stages, catastrophic and parametric faults in the system can not only be detected but also located and diagnosed.

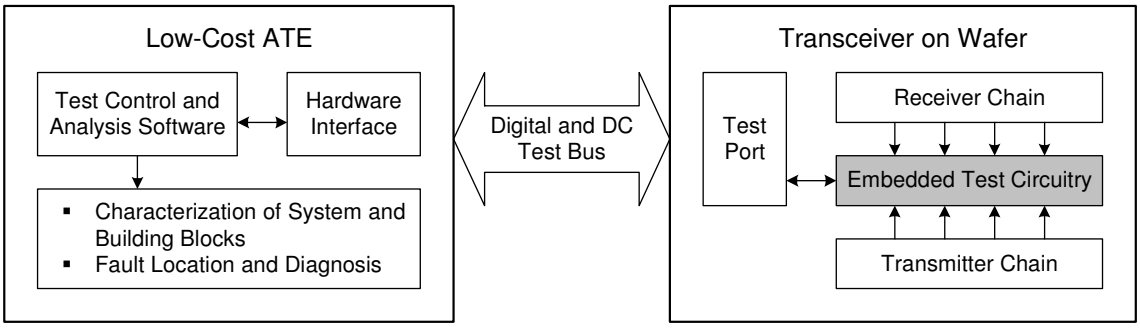


Fig. 8.1 Objective of the proposed set of on-chip testing techniques

8.1 Switched loop-back architecture

A loop-back connection between the transmitter and receiver chains is one of the earliest strategies to test the functionality of wireless and wire-line communication systems [45]. It does not require an external stimulus and is effective to detect catastrophic faults in the complete signal path. Fig. 8.2(a) depicts this testing scheme for a transceiver architecture with direct up-conversion. In a complete realization the base band sections include in-phase (I) and quadrature (Q) paths but in this block diagram only one path is shown for simplicity.

In the loop-back configuration, the baseband section of the transmitter generates a tone or a modulated signal with a center frequency f_B. With the input from the local oscillator (LO) at a frequency f_{RF} the up-converter generates a tone at $f_B + f_{RF}$. The loop-back connection must attenuate the output of the PA to make it suitable for the dynamic range of the LNA. After the down-conversion with the same tone from the LO, the resultant signal at the receiver baseband is centered at f_B. The characteristics of the demodulated or digitized signal form a digital signature of the receiver, which can be analyzed by the ATE to evaluate the performance of the transceiver. In this configuration, the range of values that f_B can take is limited by the transmitter baseband.

Recent radio implementations use transmitter architectures in which the modulation of the transmitted signal is directly performed on the VCO [66, 67], avoiding the up-conversion. As shown in Fig. 8.2(b), the direct application of loop back test is not practical in this kind of transceiver. A DC decoupling mechanism is generally included at one or more points in the baseband section of the receiver to prevent that DC offsets

saturate the demodulator or ADC. Since the signal at the output of the PA has the same frequency as the one used in the down-conversion, only a DC voltage will be obtained after the mixer and this information is lost. To overcome this limitation of the loop-back test in a VCO modulating transceiver, [46] proposes to introduce a delay in the loop-back connection as well as a digital DfT modification in the modulator. This strategy can be used to detect catastrophic faults and measure some of the important performance metrics of the transceiver. However, the required delay is implemented off-chip. This demands the flow of an RF signal outside the wafer, which increases the cost and complexity of the setup.

Fig. 8.2(c) illustrates the principle of operation of the proposed switched loop-back technique applied to a transceiver with direct VCO modulation. If the signal in the loop-back path is switched at a frequency of $f_{SW,}$ two additional tones are created at frequencies $f_{RF}\pm f_{SW}$. After the mixing with f_{RF} in the receiver, both tones are down-converted to f_{SW}. In this way, the frequency of the signal that controls the switch determines the frequency of the signal at the baseband chain. Conceptually, this is equivalent to introducing a mixer in the loop-back path; however, a simple switch is a suitable frequency translation device in this application. As shown in Figure 8.2(c), an important practical consideration is that in the “off” state, the switch must connect the input of the LNA to a 50Ω resistor and not directly to ground to preserve the stability of the LNA.

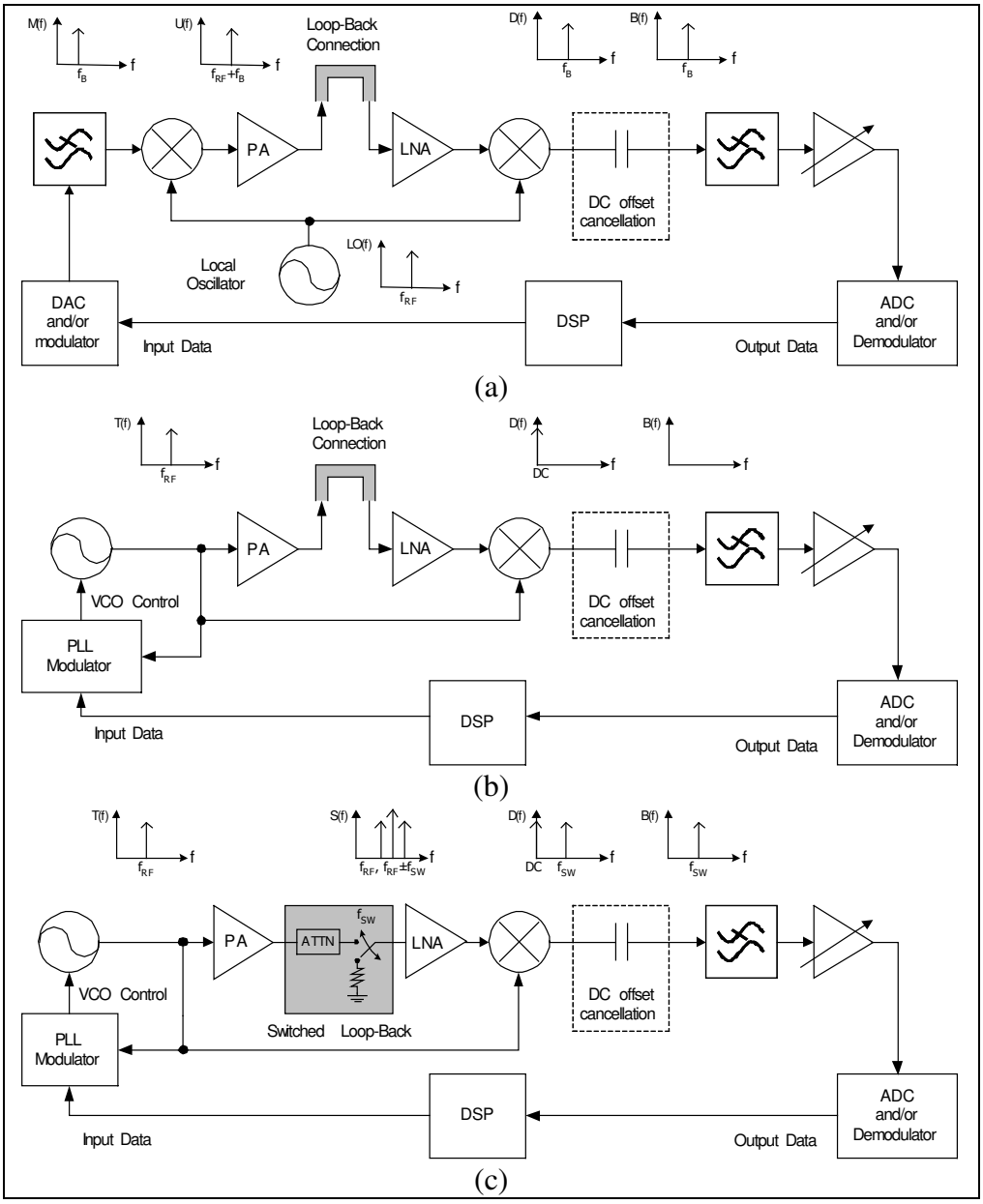


Fig. 8.2 Loop-back architectures. (a) Standard technique in an up-conversion transmitter. (b) Standard technique in a direct VCO modulation transmitter. (c) Proposed switched configuration

The operation of the switch on the signal from the PA can be modeled as a multiplication between the RF signal and square wave from 0 to 1. Such a train of pulses can be described in the time domain as:

$$P(t)=\sum_{n=0}^{\infty}K_n\cdot\cos(n\omega_{SW}t+\theta_n)=K_0+K_1\cdot\cos(\omega_{SW}t+\theta_1)+K_2\cdot\cos(2\omega_{SW}t+\theta_2)+\ldots \quad (8.1)$$

where $\omega_{SW}=2\pi f_{SW}$ and K_n, θ_n are constants that define the amplitude and phase of each frequency component respectively. The product of P(t) and the RF signal with amplitude A and frequency f_{RF} results in the switched signal S(t):

$$\begin{aligned}S(t)&=\left[\sum_{n=0}^{\infty}K_n\cos(n\omega_{SW}t+\theta_n)\right]\cdot A\cos(\omega_{RF}t)\\&=\frac{A}{2}[2K_0\cos(\omega_{RF}t)+K_1\cos((\omega_{RF}-\omega_{SW})t+\phi_1)+K_1\cos((\omega_L+\omega_{SW})t+\phi_2)\\&\quad+K_2\cdot\cos((\omega_{RF}+3\omega_{SW})t+\phi_3)+K_2\cdot\cos((\omega_{RF}-3\omega_{SW})t+\phi_4)+\ldots\end{aligned} \quad (8.2)$$

where ϕ_1, ϕ_2… ϕ_n are the phases corresponding to each of the new frequency components. Finally, after the second multiplication at the mixer of the receiver, the down-converted signal D(t) becomes:

$$\begin{aligned}D(t)&=\left[\sum_{n=0}^{\infty}K_n\cos(n\omega_{SW}t+\theta_n)\right]\cdot A\cos(\omega_{RF}t)\cdot B\cos(\omega_{RF}t+\alpha)\\&=C_0+C_1\cos(\omega_{SW}t+\beta_1)+C_2\cos(3\omega_{SW}t+\beta_2)+C_3\cos(5\omega_{SW}t+\beta_3)+\ldots\\&\quad+E_1\cos((2\omega_{RF}+\omega_{SW})t+\gamma_1)++E_1\cos((2\omega_{RF}-\omega_{SW})t+\gamma_2)+\ldots\end{aligned} \quad (8.3)$$

where α, β_n and γ_n are phase constants. The final amplitude of each frequency component (C_n, E_n) depends on the amplitude B of the local oscillator as well as on the conversion gain of the mixer. The DC component C_0 is blocked by the DC offset cancellation circuitry and the frequency components located around $2f_{RF}$ will have a negligible amplitude since the output of a down-conversion mixer shows a low-pass characteristic. In addition, C_2, C_3, … C_n depend on the non-dominant frequency components of S(t) and hence will be small in comparison to C_1.

One of the most important advantages of this approach is that the loop-back connection can have a simple on-chip implementation. A programmable attenuator can be implemented with switches and a bank of resistors or capacitors and a simple CMOS switch can perform the commutation of the signal at the input of the LNA. The switching signal is a digital clock with frequency f_{SW} in the range of MHz which can be easily applied to the transceiver on wafer. The ATE can have a direct control over f_{SW} and in this way frequency response of the transmitter and receiver chains can be performed independently without any other modification to the transceiver architecture.

One of the limitations of a stand-alone loop-back test is that it is not able to identify the location of catastrophic faults (e.g. an open in the signal path) and some important parametric faults can pass undetected. For example, a higher gain in the PA or mixer can mask a lower gain in the LNA. In this sense, a more effective testing strategy incorporates means of verifying the receiver operation at different intermediate stages of the signal path and not only at its end points.

8.2 Overall testing strategy

The joint application of the techniques described above can act in a synergetic way to improve the testability of an entire integrated system. Fig. 8.3 depicts the block diagram of a transceiver using a direct conversion transmitter with a switched loop-back connection, RF RMS detectors (RFD) in the RF section and a TFCS in the baseband section. The DCDC acts as an interface between the on-chip testing circuitry and a digital port of the ATE.

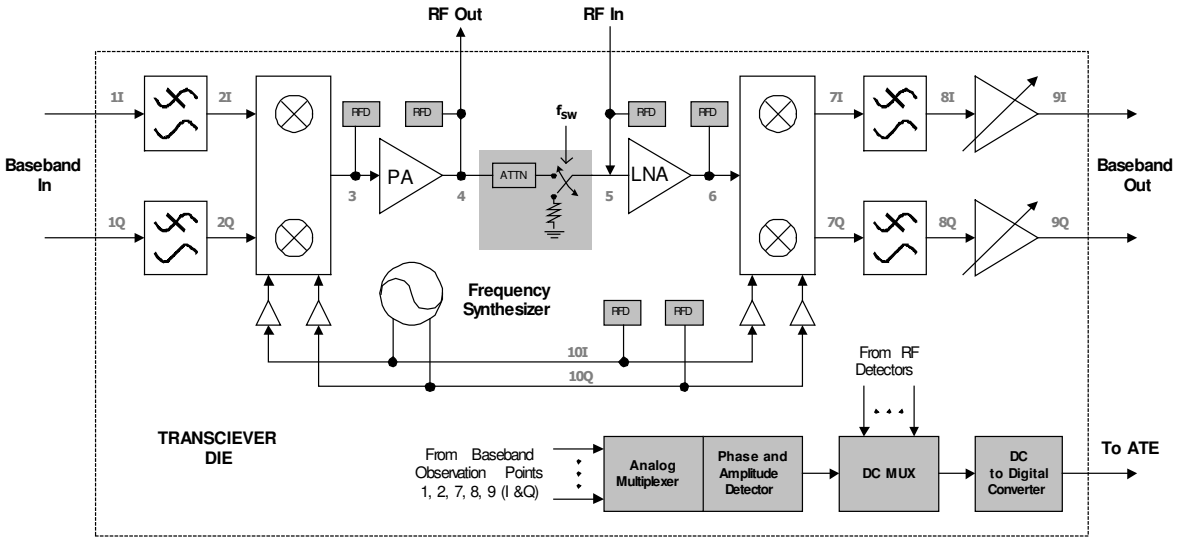


Fig. 8.3 Integrated transceiver with improved testing capabilities

With the exception of the baseband circuitry at the transmitter, the entire transceiver chain can be tested by using the LO signal and the switched loop-back connection. A complete end-to-end test requires the application of a low-frequency signal at the input of the transmitter either from the ATE or from an on-chip signal generator like the one proposed for the TFCS. The switch loop back connection guarantees the flow of a test stimulus throughout the transceiver path that can be used by the embedded testing devices to evaluate different performance metrics at different intermediate points of the system.

By providing independent control of the frequency of the signals across the transmitter and receiver chains, and providing access to internal points in the RF and baseband sections, the testability of the receiver is improved. Table 8.1 describes the different tests that can be performed in the proposed architecture. A complete testing

solution for a given transceiver may not have to perform all of the possible tests. The presented transceiver architecture with enhanced testability is meant to serve as a basis of a comprehensive testing strategy in which test optimization, and alternate testing techniques can be applied to optimize the fault coverage and the time/cost test efficiency.

Table 8.1 Transceiver testing with the proposed techniques

Test	Test device and method to be employed	Observation Nodes
LNA gain and 1dB comp. point.	RFDs. The input power to the LNA is swept by changing the transmitter output power or the loop-back attenuator loss.	5, 6
PA gain and 1dB comp. point.	RFDs. The input power to the PA is swept by varying the up-converter gain.	2
Up-converter operation and output power.	RFD	3
Synthesizer operation and output power for I &Q branches.	RFD	10 (I&Q)
Phase and magnitude mismatch between the I and Q base-band channels.	TFCS	7, 8, 9 (I&Q)
Transmitter filter transfer function.	TFCS. Input frequency to the transmitter is swept across the desired characterization range.	
Channel selection filter transfer function.	TFCS. f_{SW} is swept across the desired characterization range.	7, 8 (I&Q)
Adjacent channel rejection	TFCS. f_{SW} is set at the adjacent channel frequency.	8 or 9
Base band amplifier gain programmability	TFCS	8, 9 (I&Q)

The flow diagram in Fig. 8.4 describes a hierarchical testing strategy. As a first step, from an end-to end test which would not involve the internal test devices it can be determined if a catastrophic fault is present. In this case the test vector to the second step of the procedure would focus on finding the fault location. When no major fault is found, the results from the overall system tests can be used to determine the internal building blocks to characterize in detail. Table 8.2 presents an analysis of the area overhead that the addition of the proposed set of on-chip testing circuitry represents with respect to the size of recently reported 2.4GHz transceivers for various standards. Despite the fact that the area for the testing devices is taken from prototypes in CMOS 0.35μm technology, the area overhead is less than 10%.

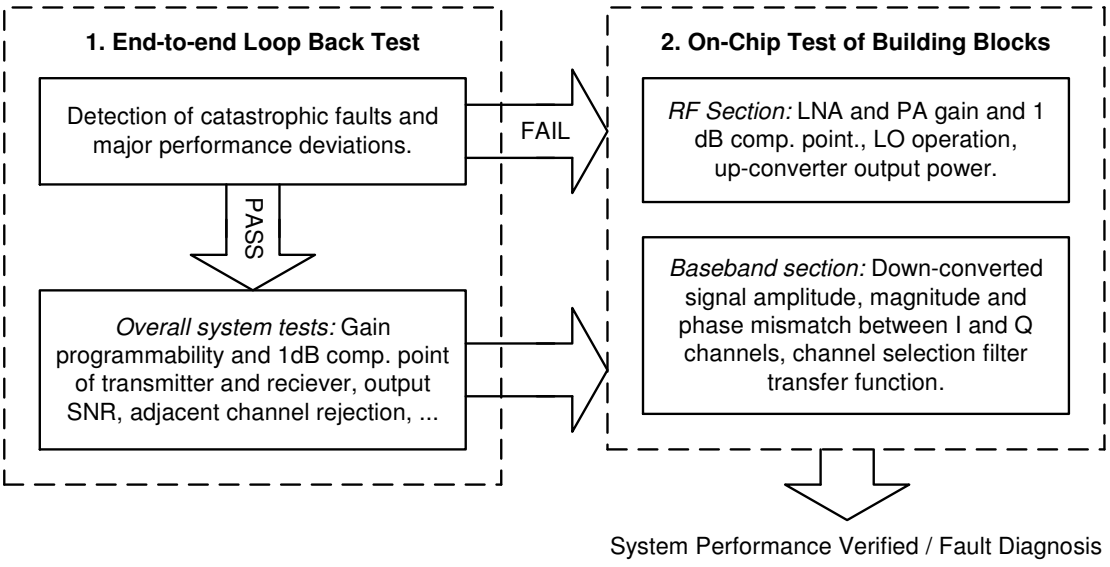


Fig. 8.4 Flow diagram of the proposed testing strategy

Table 8.2 Area overhead analysis for reported transceivers

Reference	Standard	Analog Area [mm^2]	CMOS Process	Overhead of 6 RF RMS Detectors, TFCS and DCDC (0.45mm^2)
[66]	Bluetooth	5.9	0.18μm	7.6%
[67]	DECT	9.4	0.25μm	4.8%
[68]	802.15.4 (ZigBee)	8.75	0.18μm	5.1%
[69]	Dual: Bluetooth/802.11b	16	0.18μm	2.8%

8.3 Simulation results

A macromodel for the transceiver architecture shown in Fig. 8.3, including the switched loop-back connection and the RF RMS detectors is built in Systemview to analyze the performance of the proposed testing scheme. The components employed for the model include the most important non-idealities expected from an integrated implementation such as noise, compression, non-linearity and finite isolation between terminals. Table 8.3 summarizes the specific characteristics of the modeled architecture, which are taken from the transceiver reported in [68].

Table 8.3 Characteristics of modeled ZigBee transceiver

RF Frequency	2.4 GHz
Transmitter Architecture	Direct Conversion
Transmitter Power	0 dBm
PA Gain	15dB
Receiver Architecture	Low-IF, IF Frequency = 4MHz
Sensitivity	-82 dBm
RF Front-End IIP3	-4dBm
RF Front-End Gain	30dB (LNA 15dB + Mixer 15dB)
Baseband Filter	5^{th} order bandpass polyphase

An IEEE 802.15.4 implementation is chosen for the example because this standard is targeted for very low-cost applications. The attenuator in the loop-back connection has a loss of 25dB to bring the 0dBm output of the PA within the linear range of the receiver. The RF RMS detectors are modeled according to the characteristics of the device presented in chapter VII.

Fig. 8.5 shows the simulation results for a transceiver meeting specifications. The frequency for the loop-back switching is 4MHz, since this is the center frequency of the baseband filter. Fig. 8.5(a) and (b) show the switched signal at the input of the LNA in the time and frequency domains, respectively. Observe that the frequency components of interest (2400±4MHz) are at least 10dB above other tones. Figs. 8.5(c), (d) and (e) show the outputs of the RF RMS detectors at the output of the PA, the LNA input, and LNA output respectively. Finally, the expected 4MHz signal at the output of the baseband filter is shown in Fig. 8.5(f).

Even though the output of the RF RMS detectors placed after the switch is intermittent, the gain of the LNA can still be estimated provided that the DCDC samples their output at the appropriate rate. In the presented model, the DCDC has around 100nS to sample the output of each detector. In a given scenario where the DCDC is slower, f_{SW} can be set first to a lower value (so that the RFDs hold their output for a longer time) to test the LNA, and then shift to a higher value to test the rest of the receiver chain.

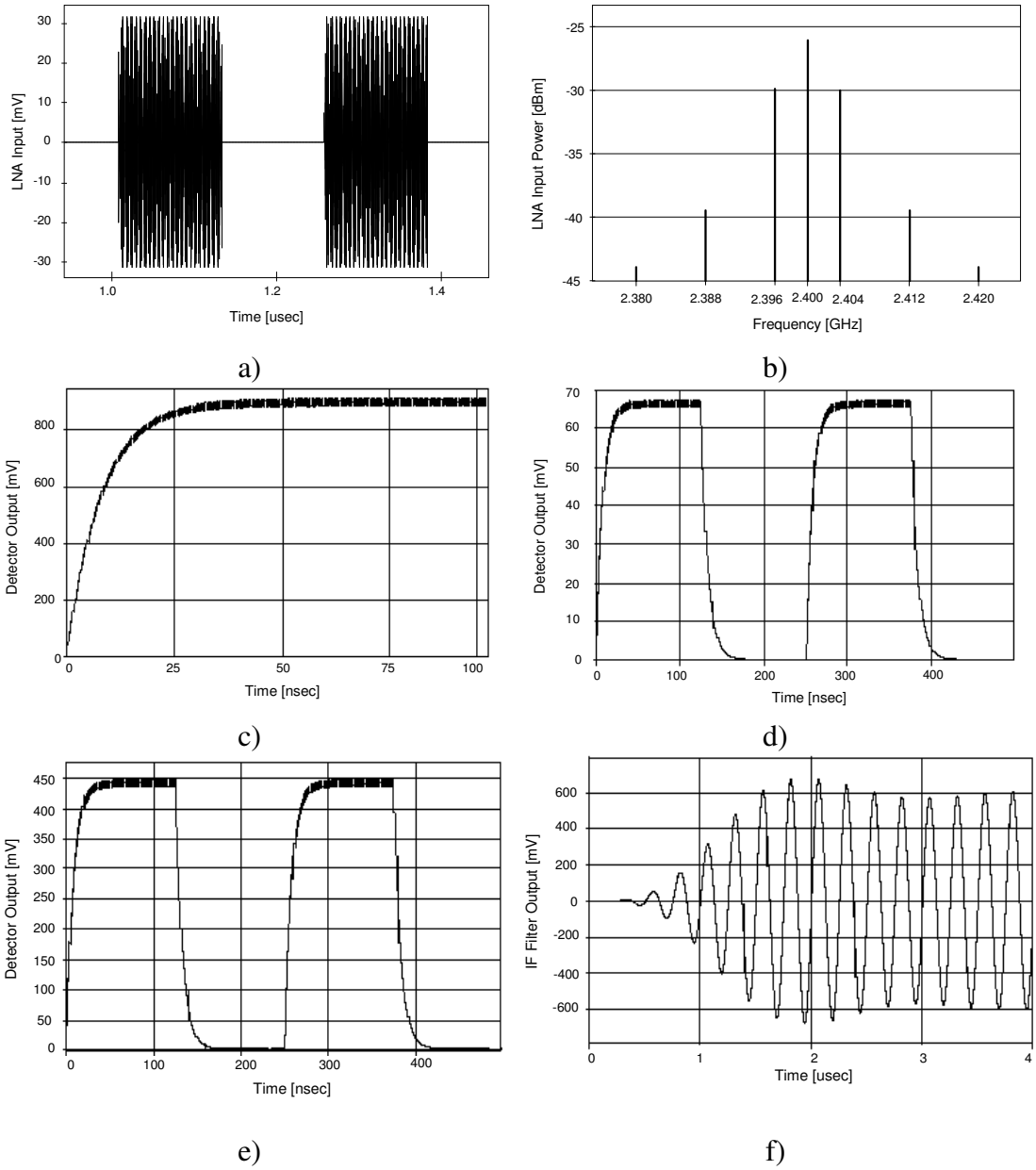


Fig. 8.5 Simulation results for a transceiver meeting specifications. a) Input of the LNA in the time domain. b) Input of the LNA in the frequency domain. c) Output of the RFD at the output of the PA. d) Output of the RFD at the input of the LNA. e) Output of the RFD at the output of the LNA. f) Output of the baseband filter

Fig. 8.6 shows the simulation results for a transceiver in which some of the individual building blocks do not meet the target specifications. The PA has 2dB higher gain (12dB total), the LNA has 5dB less gain (10dB total) and the channel selection filter is not centered at 4MHz but at 4.5MHz. Figs. 8.6(a) and (b) show the output of the RFDs at the outputs of the PA and LNA, respectively. It can be readily noticed that these final values are different from the ones in the case of Fig. 8.5. Figs. 8.6(c) and (d) show the output of the channel selection filter for f_{SW}=4MHz and f_{SW}=4.5MHz. Note that through a stand-alone end-to-end test, it would not be possible to determine the cause of a reduced amplitude at the end of the receiver baseband. Moreover, if both PA and LNA exhibit a higher gain, the output of the receiver could show the expected amplitude even if the filter has a deviated center frequency. If this transceiver was tested with a conventional loop-back test without the switch, by changing the input frequency to the transmitter it could be determined that the fault is occurring at the baseband but not if it is on the transmitter or receiver side. With the proposed scheme, parametric faults of different sections of the system can be detected and located.

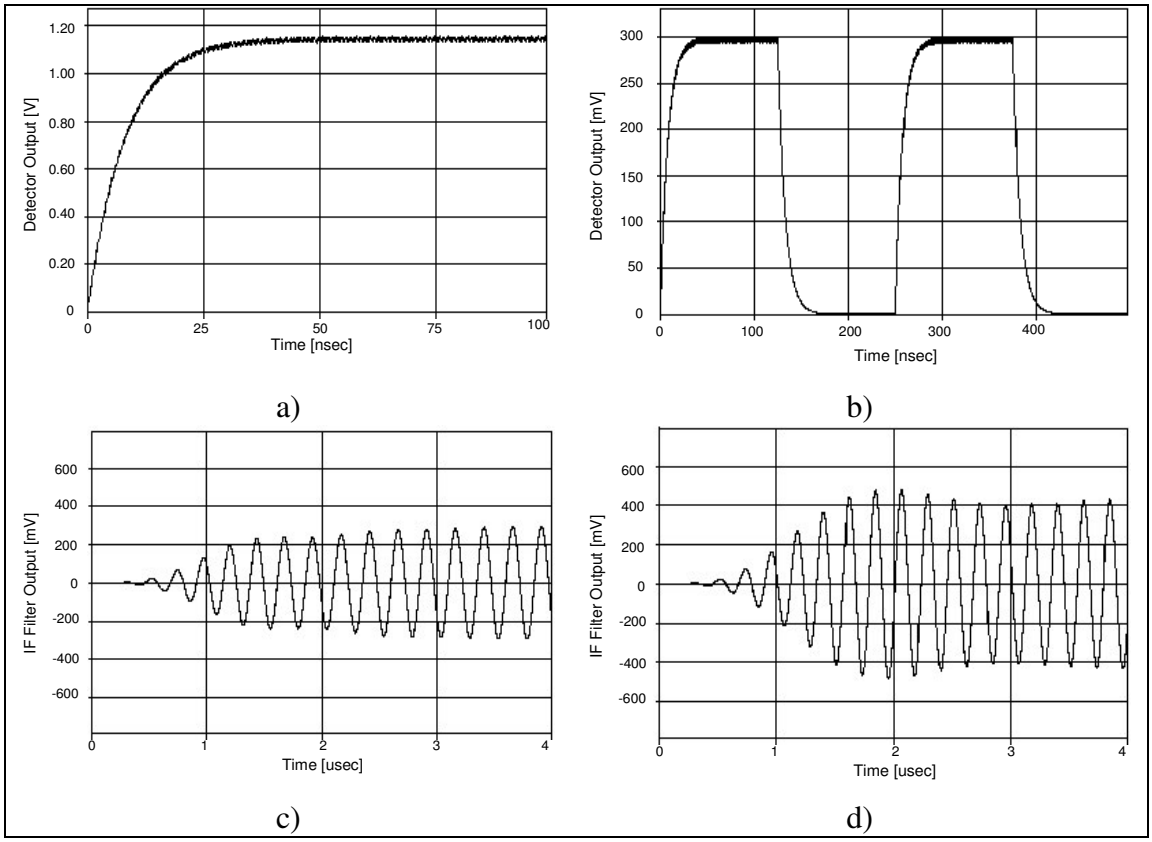


Fig. 8.6 Simulation results for transceiver not meeting specifications. a) Output of the RFD at the output of the PA. b) Output of the RFD at the output of the LNA. c) Output of the baseband filter for f_{SW}=4MHz. d) Output of the baseband filter for f_{SW}=4.5MHz.

CHAPTER IX

SUMMARY

An integrated receiver for MB-OFDM UWB communications operating in the range of 3-10GHz has been demonstrated. Important challenges for the practical use of UWB receivers have been addressed such as: operation in multiple band groups, on-chip rejection of interference in the range of 5.15-5.35GHz and implementation in a commercial package and standard PCB substrate. In the evolution of integrated UWB receiver solutions, the implemented system represents a step forward in the reduction of area and complexity with respect to number covered bands. The proposed MB-OFDM receiver is the first of its kind to cover the 3-10GHz spectrum and the first UWB receiver operating beyond 5GHz demonstrated in a package. The integrated receiver mounted on a standard PCB substrate demonstrates the feasibility of low cost and very high data rate (>100Mbps) radios capable of maximizing the use of the available UWB spectrum.

A compact integrated system for analog testing has been developed and evaluated experimentally. The magnitude and phase responses over frequency of an analog circuit or sub-system can be evaluated without the use of analog instrumentation. The simplicity and low-bandwidth of its digital interface make the proposed test core suitable for wafer-level test and compatible with the IEEE 1149.4 test standard. With respect to existent on-chip test solutions implemented in similar technologies, this system presents the smallest area, the highest frequency range in terms of frequency response characterization, and the advantage of presenting a low processing overhead.

From an area overhead analysis, it is estimated that this system requires less than 10% of extra-area for typical analog signal processing subsystems such as an ADSL driver or the baseband section of a transceiver, which are suitable test candidates. The proposed system is an effective and area-efficient solution for low-cost testing of analog circuits.

A practical RF RMS detector design is proposed and designed in a standard CMOS technology. Its very small area, input capacitance and frequency of operation make it suitable for the embedded test and calibration of CMOS RF components of modern communication systems. An effective technique to perform the on-chip measurement of the gain and 1dB compression point of an RF CUT using the on-chip RF detectors has also been introduced.

The developed on-chip testing devices show that the direct, on-chip observation of analog and RF building blocks at MHz and GHz frequencies can be performed in a CMOS process and with a minimum area and parasitic loading overhead.

The combination of a switched loop-back architecture with the use of the above mentioned built-in testing techniques significantly enhances the testability of an RF transceiver. The proposed strategy enables the characterization of the entire wireless system and its individual building blocks at the wafer level through digital information, allowing the implementation of a practical and cost effective test solution.

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APPENDIX A

MATLAB CODE FOR SYSTEM-LEVEL CALCULATIONS

A. 1. UWB Receiver system-level design MATLAB code

```
%UWB receiver system level design%
%Alberto Valdes Garcia%

%Constants
K = 1.38e-23;       % Boltzmann constan
T = 300;            % room temperature

%Standard specifications
Eb_No=5;            % dB
Sensitivity = -73;  % dBm
max_signal = -4;    % dBm
Rb = 480e6;         %Mbps
BW=264e6;           %MHz

% General parameters
Signal_ADC_max = 10;        % maximum signal level at ADC input(dBm) (400mVpp)

% Required system specifications

NF_margin = 3;
Req_syst_NF = Sensitivity - (-174+10*log10(Rb)) - Eb_No - NF_margin
Rx_Gain_max = Signal_ADC_max-Sensitivity;
Rx_Gain_min = Signal_ADC_max-max_signal;

% Block specifications

NB=6;          %number of blocks
RF_filter = 1; %indeces
ADC_SNR = 30; % dB
ADC_NF = Signal_ADC_max - ADC_SNR - 10*log10(4*K*T*BW/2*1000)

%                RF_filter  LNA     Mixer     Filter     PGA    ADC

NF         =     [  0        3        16        36        25        0]      % NF in dB referenced to 50 Ohm
Gain_max =       [  0       15        21        0         42        0]       % max gain in dB
IIP3       =     [  100      -9       5         18        12        100]     % input referred IP3 in dBm
Atten_792M =     [  0        0        5         20        3         0 ]
```

```
%  Computarion of system performance

for i=0:NB
   Gain_max_accum(i+1) = sum(Gain_max(1:i));  % accumulated voltage gain from antenna to each block input
end

% Computation of gain at the adjacent band

for i=0:NB-1
   Int_atten_accum(i+1) = sum(Atten_792M(1:i));              % accumulated voltage gain from antenna
end                                                          % to block input for the interferer

IIP3_eff = IIP3+3*Int_atten_accum;            %Effective IP3 after taking the interference attenuation into account
NF_IR_Lin = (10.^(NF/10)-1)./10.^(Gain_max_accum(1:NB)/10)+1; %Input referred NF in linear units
Syst_NF = 10*log10(sum(NF_IR_Lin-1)+1)                       % System NF in dB
IIP3_IR_Lin = 10.^((IIP3_eff-Gain_max_accum(1:NB))/10);      % IIP3 referred to the Rx input in SQRT(mW)
Syst_IIP3 = 10*log10(1/sum(1./IIP3_IR_Lin))                  % System IIP3 in dBm

% Sensitivity test

Sig_level_IR = Sensitivity;                                  % signal level at antenna (Rx input referred)
Noise_level_IR = -174+10*log10(BW);                          % Thermal noise at antenna (Rx input referred)
Sig_level(1:NB) =  Sig_level_IR+Gain_max_accum(1:NB); % Signal level at each block input
for i=0:NB-1
   NF_IR_accum_Lin(i+1)=sum(NF_IR_Lin(1:i)-1)+1;
End


Noise_level(1:NB) = 10*log10(10.^((Noise_level_IR+Gain_max_accum(1:NB))/10).*NF_IR_accum_Lin);
SNR = Sig_level-Noise_level;

%Plot sensitivity test

figure
plot([0:NB-2],Sig_level(2:end), 'k-o',[0:NB-2], Noise_level(2:end), 'k-s')
set(gca,'XTick',[0:NB])
set(gca,'XTickLabel',{'LNA';'Mixer';'Filter';'PGA';'ADC'})
grid on
title('Sensitivity test')
ylabel('Signal and Noise power at the input of each block [dBm]')
legend('Signal level','Noise level',0)

figure
plot([0:NB-2], SNR(2:end), 'k-d')
set(gca,'XTick',[0:NB])
set(gca,'XTickLabel',{'LNA';'Mixer';'Filter';'PGA';'ADC'})
grid on
title('Sensitivity test')
ylabel('SNR at the input of each block [dB]')
legend('SNR',0)
```

APPENDIX B

LIST OF PUBLICATIONS BASED ON THIS DISSERTATION

B.1. Journal Papers

1. C. Mishra, A. Valdes-Garcia, F. Bahmani, A. Batra, E. Sanchez-Sinanencio and J. Silva-Martinez, "Frequency Planning and Synthesizer Architectures for Multi-band UWB Radios", *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 12, pp. 3744-3756, Dec. 2005.
2. A. Valdes-Garcia, J. Silva-Martinez and E. Sánchez-Sinencio, "On-Chip Testing Techniques for Wireless RF Transceivers", Invited for *IEEE Design & Test of Computers*, To appear.
3. A. Valdes-Garcia, F. Hussein, J. Silva-Martinez and E. Sanchez-Sinencio, "An Integrated Transfer Function Characterization System with a Digital Interface for Analog Testing", Under evaluation by *IEEE Journal of Solid-State Circuits.*
4. C. Mishra, A. Valdes-Garcia, E. Sánchez-Sinencio and J. Silva-Martinez, "A 3.7-10 GHz 11-Band Frequency Synthesizer for MB-OFDM UWB Radios in 0.25µm SiGe BiCMOS", Under evaluation by *IEEE Transactions on Microwave Theory and Techinques.*
5. A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez and E. Sánchez-Sinencio, "An 11-Band 3-10GHz Receiver in SiGe BiCMOS for MB-OFDM UWB Communication", *In preparation for IEEE IEEE Journal of Solid-State Circuits.*

B.2. Conference Papers

1. A. Valdes-Garcia, M. G. Mendez Rivera, J. Silva-Martinez and E. Sanchez-Sinencio, "On-Chip Spectrum Analyzers for Analog BIST", *SRC TECHCON Conference*, August 2003.

2. A. Valdes-Garcia, J. Silva-Martinez and E. Sanchez-Sinencio, “An On-Chip Transfer Function Characterization System for Analog Built-In Testing”, *IEEE VLSI Test Symposium*, pp. 261-266, April 2004.

3. A. Y. Valero-Lopez, A. Valdes-Garcia and E. Sanchez-Sinencio “Frequency Synthesizer for On-Chip Testing and Automated Tuning”, *IEEE Int. Symposium on Circuits and Systems*, pp. 565-568, June 2004.

4. A. Valdes-Garcia, R. Venkatasubramanian, R. Srinivasan, J. Silva-Martinez and E. Sanchez-Sinencio, “A CMOS RF RMS Detector for Built-in Testing of Wireless Transceivers”, *IEEE VLSI Test Symposium*, pp. 249-254, May 2005.

5. A. Valdes-Garcia, J. Silva-Martinez and E. Sanchez-Sinencio, “Implementation of Built-In Testing Techniques for Analog and RF Integrated Circuits”, SRC TECHCON Conference, October 2005.

6. C. Mishra, A. Valdes-Garcia, E. Sánchez-Sinencio and J. Silva-Martinez, "A carrier frequency generator for multi-band UWB radios", To appear in *Proc. of IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

7. A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez and E. Sánchez-Sinencio, “An 11-Band 3.4 to 10.3 GHz MB-OFDM UWB Receiver in 0.25µm SiGe BiCMOS”, To appear in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, June 2006.

8. A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez and E. Sanchez-Sinencio, “A 0.9-2.4GHz CMOS Amplitude Detector for On-Chip RF Test”, Under evaluation by *IEEE International Test Conference*, October 2006.

VITA

Alberto Valdes Garcia was born in 1978, and lived in San Mateo Atenco, Mexico. He received the B.S. degree in Electronic Systems Engineering from the Monterrey Institute of Technology (ITESM), Campus Toluca, Mexico in 1999 (Highest Honors) and the Ph.D. degree in Electrical Engineering from Texas A&M University in 2006.

In 2000 he was a Design Engineer with Motorola, Broadband Communications Sector. From 2001 to 2004 he was a Semiconductor Research Corporation (SRC) research assistant at the Analog & Mixed-Signal Center (AMSC), Texas A&M University, working on the development of analog and RF built-in testing techniques. In the summer of 2002 he was with the Read Channel Design Group at Agere Systems working on RF circuit design for mass storage applications. During the summer of 2004 he was with the Communication Technologies Department at the IBM T. J. Watson Research Center, where he joined as a Research Staff Member in 2006. His present research is on integrated circuit design for millimeter-wave communication systems.

From 2000 to 2005, Alberto was the recipient of a scholarship from the Mexican National Council for Science and Technology (CONACYT). He represented Mexico in the 1994 Odyssey of the Mind world creativity competition celebrated in Ames, Iowa and in the 1997 International Exhibition for Young Scientists celebrated in Pretoria, South Africa. He is the winner of the 2005 Best Doctoral Thesis Award presented by the IEEE Test Technology Technical Council (TTTC).